INTEGRATED CIRCUITS

DATA HANDBOOK

Data Communications

BOOK IC19 1991

Signetics

Philips Components

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IC013 DATA COMMUNICATIONS 1991

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Data Communication Products

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LIFE SUPPORT APPLICATIONS

Signetics Products are not designed for use in life support appliances, devices, or systems where malfunction of a Signetics Product can reasonably be expected to result in a personal injury. Signetics customers using or selling Signetics Products for use in such applications do so at their own risk and agree to fully indemnify Signetics for any damages resulting from such improper use or sale.

Signetics registers eligible circuits under
the Semiconductor Chip Protection Act.

Preface

Data Communication Products

Applications for our data communications products continue to grow as the microprocessor-based systems proliferate. In addition to servicing the traditional function, we recognize the need to offer improved features and performance while at the same time we retain a cost-effective product. To achieve this goal we have installed manufacturing capability that takes advantage of our technology development effort particularly in the CMOS arena. The new products resulting from this activity will not only complement the existing family, but will also allow the designer to enhance the system capabilities and performance very economically.

Our entire focus in Data Communications is to continue to play a major role in the market through constant attention to performance and economics using innovation and technology development.

Product Status

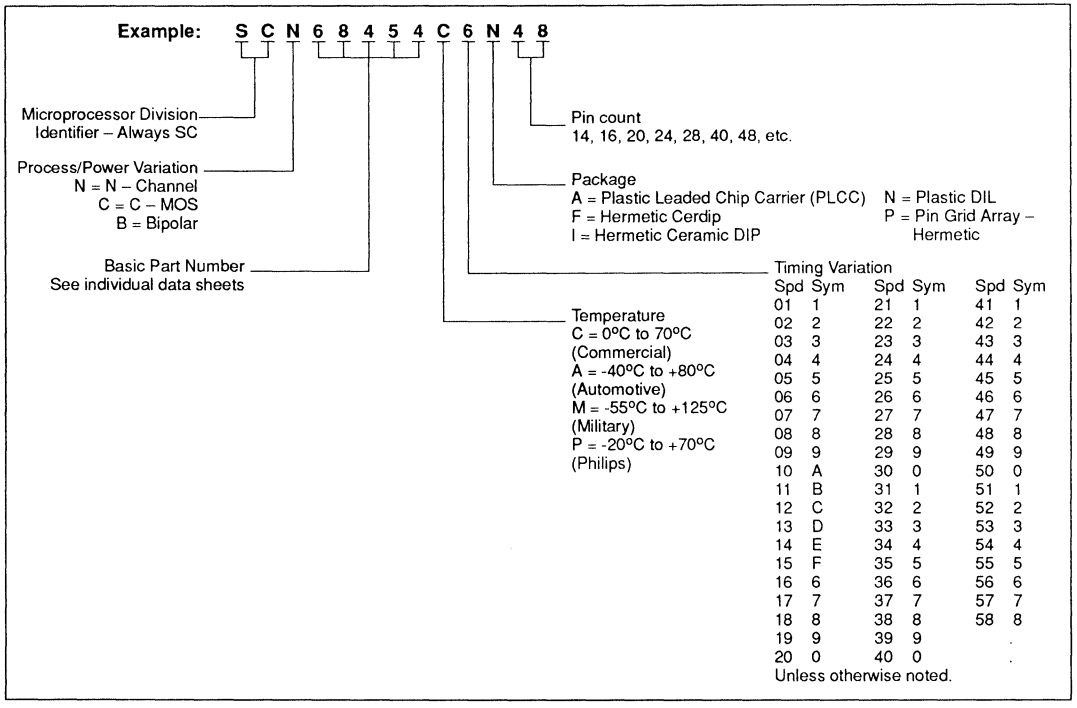
Data Communication Products

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Ordering Information

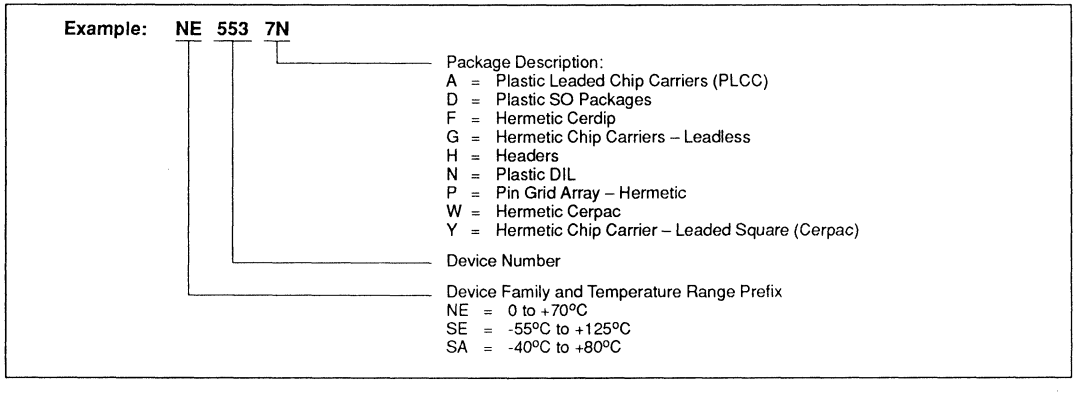
Data Communication Products

DATA COMMUNICATION PRODUCTS PART NUMBERING SYSTEM



Spd	Sym	Spd	Sym	Spd	Sym
01	1	21	1	41	1
02	2	22	2	42	2
03	3	23	3	43	3
04	4	24	4	44	4
05	5	25	5	45	5
06	6	26	6	46	6
07	7	27	7	47	7
08	8	28	8	48	8
09	9	29	9	49	9
10	A	30	0	50	0
11	B	31	1	51	1
12	C	32	2	52	2
13	D	33	3	53	3
14	E	34	4	54	4
15	F	35	5	55	5
16	6	36	6	56	6
17	7	37	7	57	7
18	8	38	8	58	8
19	9	39	9		
20	0	40	0		

Unless otherwise noted.



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Section 1
Quality and Reliability

Quality and Reliability

Data Communication Products

SIGNETICS QUALITY

Signetics has put together winning processes for manufacturing. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The data communications produced in the Standard Products Group must meet rigid criteria as defined by our design rules and as evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 amps/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from –55°C to +125°C and at ± 10% supply voltage.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 — QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available upon request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. Samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One-hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: T_J = 150°C, 1000 hours, static biased or dynamic operation, as appropriate (worst case bias configuration is chosen)
- High Temperature Storage: T_J = 150°C, 1000 hours
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static biased
- Temperature Cycling (Air-to-Air): –65°C to +150°C, 1000 cycles

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15psig, 121°C, 100% saturated steam).

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Quality and Reliability

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the Data Communication SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors
- Device or generic group failure rate studies
- Advanced environmental stress development
- Failure mechanism characterization and corrective action/prevention reporting

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in the evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits which are derived from quality products can be summed up in the words, *lower cost of ownership.*

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals, inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction fo achieving a high level of quality. Special programs are targeted on specific quality issues. For example, in 1978 a program to reduce electrically defective units for a major automotive manufacturer improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100ppm (parts per million), down from an industry practice of 10,000ppm, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees, from the R and D laboratory to the shipping dock. In short, from a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality (see Figure 1).

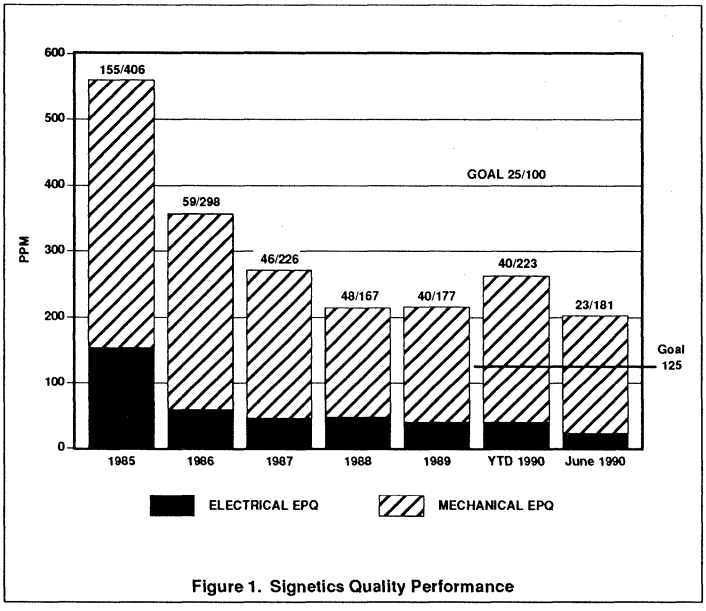

Figure 1. Signetics Quality Performance

Quality and Reliability

ONGOING QUALITY PROGRAM

The quality improvement program at Signetics is based on "Do It Right the First Time". The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by all technical and administrative functions equally.

This program extends into every area of the company, and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is continuous improvement.

QUALITY COLLEGE

Almost continously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" — ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing issues.

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

PRODUCT QUALITY PROGRAM

To reduce defects in outgoing products, we created the Product Quality Program. This is managed by the Product Engineering Council, composed of the top product engineering and test professionals in the company. This group:

1. Sets aggressive product quality improvement goals;
2. provides corporate-level visibility and focus on problem areas;
3. serves as a corporate resource for any group requiring assistance in quality improvement; and
4. drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent.

Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 2. Simultaneously, waivers of incoming material have been eliminated.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions:

- Manufacturing quality control
- Product assurance testing and qualification
- Laboratory facilities – failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers. Or, write on your letterhead directly to the corporate VP of quality at the corporate address shown at the back of this manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels.
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This teamwork with you will allow us to achieve our mutual goal of improved product quality.

Quality and Reliability

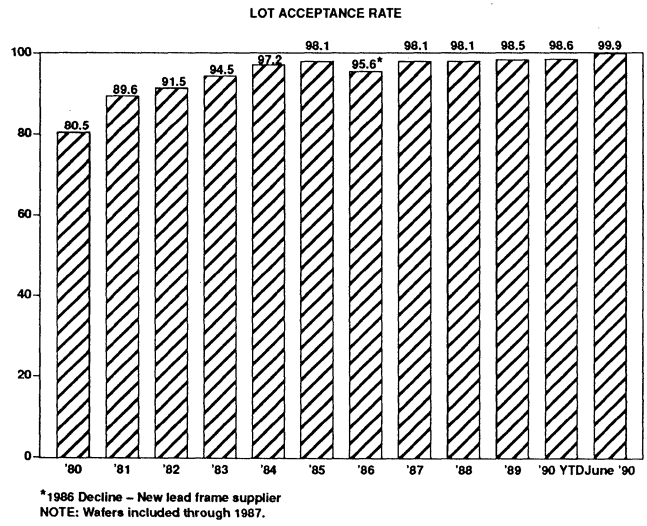

Figure 2. Incoming Direct Materials Quality

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time", a key concept of the quality improvement program. Key changes included such things as implementing 100% temperature testing on all products as well as upgrading test handlers to insure 100% positive binning. Some of the other changes and additions were to tighten the outgoing QA lot acceptance criteria to the tightest in the industry, with zero defect lot acceptance sampling across all three temperatures.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading quality supplier of data communications. These achievements have also led to our participation in several Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

Section 2
Digital Data Communication Products

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Philips Components–Signetics

Document No.	853–0083
ECN No.	77351
Date of Issue	February 20, 1985
Status	Product Specification
Data Communication Products	

SCN2651
Programmable communications interface (PCI)

DESCRIPTION

The Signetics SCN2651 PCI is a universal synchronous/asynchronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Signetics SCN2650 microprocessor and may be used in a polled or interrupt driven system environment. The SCN2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The SCN2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

FEATURES

- Synchronous operation
  - 5- to 8-bit characters
  - Single or double SYN operation
  - Internal character synchronization
  - Transparent or non-transparent mode
  - Automatic SYN or DLE-SYN insertion
  - SYN or DLE stripping
  - Odd, even, or no parity
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
- Asynchronous operation
  - 5- to 8-bit characters
  - 1, 1-1/2 or 2 stop bits
  - Odd, even, or no parity
  - Parity, overrun and framing error detection
  - Line break detection and generation
  - False start bit detection
  - Automatic serial echo mode
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps
    (1X clock)
    DC to 62.5kbps (16X clock)
    DC to 15.625kbps
    (64X clock)

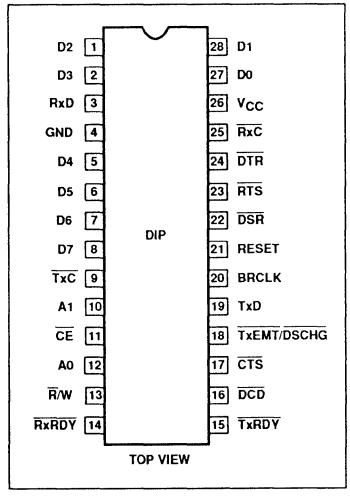
OTHER FEATURES

- Internal or external baud rate clock
- 16 internal rates – 50 to 19,200 baud
- Double buffered transmitter and receiver
- Full or half duplex operation
- TTL compatible inputs and outputs
- Single 5V power supply
- No system clock required
- 28-pin dual in-line package

APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Computer to computer links
- Serial peripherals

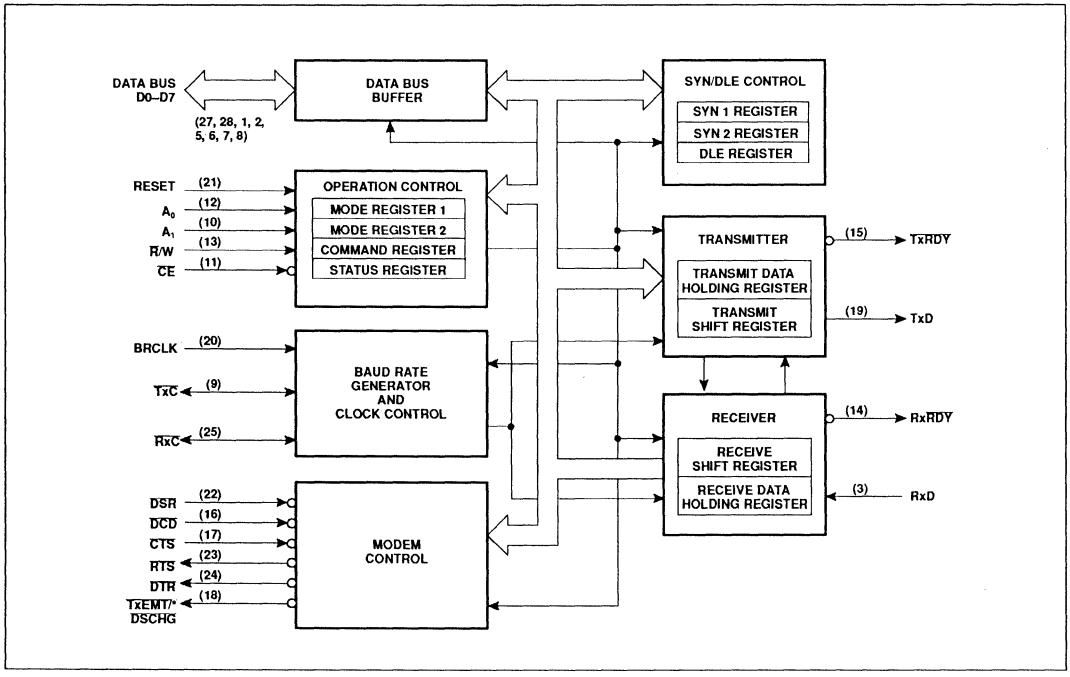
PIN CONFIGURATIONS



ORDERING CODE

PACKAGES	V_{CC} = 5V ±5%	
	Commercial	Automotive
	0°C to +70°C	-40°C to +85°C
CERDIP	SCN2651CC1F28	SCN2651CA1F28
Plastic DIP	SCN2651CC1N28	Not available
Plastic LCC	SCN2651CC1A28	Not available

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	Note 4	°C
Storage temperature	-65 to +150	°C
All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
Output voltage						
V_{OL}	Low	I_{OL} = 1.6mA			0.4	V
V_{OH}	High	I_{OH} = -100µA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to 5.25V	-10		10	µA
3-State output leakage current						
I_{LH}	Data bus high	V_O = 4.0V	-10		10	µA
I_{LL}	Data bus low	V_O = 0.45V	-10		10	µA
I_{CC}	Power supply current				150	mA

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels for testing are 0.45V and 2.4V.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.

CAPACITANCE T_A = 25°C, V_{CC} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Capacitance						
C_{IN}	Input				20	pF
C_{OUT}	Output	f_C = 1MHz			20	pF
$C_{I/O}$	Input/Output	Unmeasured pins tied to ground			20	pF

AC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Pulse width						
t_{RES}	Reset		1000			ns
t_{CE}	Chip enable		300			ns
Set-up and hold time						
t_{AS}	Address setup		20			ns
t_{AH}	Address hold		20			ns
t_{CS}	R/$\overline{W}$ control setup		20			ns
t_{CH}	R/$\overline{W}$ control hold		20			ns
t_{DS}	Data setup for write		225			ns
t_{DH}	Data hold for write		0			ns
t_{RXS}	RX data setup		300			ns
t_{RXH}	RX data hold		350			ns
t_{DD}	Data delay time for read	C_L = 100pF			250	ns
t_{DF}	Data bus floating time for read	C_L = 100pF			150	ns
t_{CED}	$\overline{CE}$ to $\overline{CE}$ delay		700			ns
Input clock frequency						
f_{BRG}	Baud rate generator		1.0	5.0688	5.0738	MHz
$f_{R/T}$[6]	$\overline{TxC}$ or $\overline{RxC}$		dc		1.0	MHz
Clock width						
t_{BRH}[5]	Baud rate high		70			ns
t_{BRL}[5]	Baud rate low		70			ns
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ high		500			ns
$t_{R/TL}$[6]	$\overline{TxC}$ or $\overline{RxC}$ low		500			ns
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	C_L = 100pF			650	ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[4]	C_L = 100pF		0		ns

NOTES:

1. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels for testing are 0.45V and 2.4V.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. Parameter applies when internal transmitter clock is used.
5. Under test conditions of 5.0688MHz, f_{BRG}, t_{BRH}, and t_{BRL} measured at V_{IH} and V_{IL} respectively.
6. $t_{R/T}$ and $t_{R/TL}$ shown for all modes except local loopback. For local loopback mode $f_{R/T}$ = 0.7MHz and $t_{R/TL}$ = 700ns min.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
27, 28, 1, 2, 5–8	D_0–D_7	8-bit data bus	I/O
21	RESET	Reset	I
12, 10	A_0–A_1	Internal register select lines	I
13	$\overline{R/W}$	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	$\overline{TxEMT/DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$	Transmitter clock	I/O
25	$\overline{RxC}$	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I

Table 1. Baud Rate Generator Characteristics Crystal Frequency = 5.0688MHz

BAUD RATE	THEORETICAL FREQUENCY 16X CLOCK	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
50	0.8KHz	0.8KHz	–	6336
75	1.2	1.2	–	4224
110	1.76	1.76	–	2880
134.5	2.152	2.1523	0.016	2355
150	2.4	2.4	–	2112
300	4.8	4.8	–	1056
600	9.6	9.6	–	528
1200	19.2	19.2	–	264
1800	28.8	28.8	–	176
2000	32.0	32.081	0.253	158
2400	38.4	38.4	–	132
3600	57.6	57.6	–	88
4800	76.8	76.8	–	66
7200	115.2	115.2	–	44
9600	153.6	153.6	–	33
19200*	307.2	316.8	3.125	16

NOTE:
*Error at 19200 can be reduced to zero by using crystal frequency 4.9152MHz.
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X.

BLOCK DIAGRAM

The PCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing and protocol are presented in the PCI programming section of this data sheet.

Timing

The PCI contains a baud rate generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full-duplex operation. See Table 1.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

INTERFACE SIGNALS

The PCI interface signals can be grouped into two types: the CPU-related signals (shown in Table 2), which interface the SCN2651 to the microprocessor system, and the device-related signals (shown in Table 3), which are used to interface to the communications device or system.

Table 2. CPU-Related Signals

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
V_{CC}	26	I	+5V supply input
GND	4	I	Ground
RESET	21	I	A high on this input performs a master reset on the SCN2651. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
$A_1 - A_0$	10, 12	I	Address lines used to select internal PCI registers.
R/W	13	I	Read command when low, write command when high.
CE	11	I	Chip enable command. When low, indicates that control and data lines to the PCI are valid and that the operation specified by the R/W, A_1 and A_0 inputs should be performed. When high, places the D_0–D_7 lines in the 3-State condition.
$D_7 - D_0$	8, 7, 6, 5 2, 1, 28, 27	I/O	8-bit, three-state data bus used to transfer commands, data and status between PCI and the CPU. D_0 is the least significant bit, D_7 the most significant bit.
TxRDY	15	O	This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
RxRDY	14	O	This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
TxEMT/ DSCHG	18	O	This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the DSR or DCD inputs has occurred. This output goes high when the status register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

OPERATION

The functional operation of the SCN2651 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the PCI programming section of the data sheet.

After programming, the PCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The SCN2651 is conditioned to receive data when the DCD input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit-time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit(s) have been assembled. The data is then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the RxRDY output is asserted. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of RxC corresponding to the received character boundary. If a break condition is detected (RxD is low for the entire character as well as the stop bit[s]), only one character consisting of all zeros (with the FE status bit set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins.

When the PCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the receiver shift register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN detect status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN detect bit to be set. Otherwise, the PCI returns to the hunt mode. (Note that the sequence SYN1–SYN1–SYN2 will not achieve synchronization.) When synchronization has been achieved, the PCI continues to assemble characters and transfer them to the holding register, setting the RxRDY status bit and asserting the RxRDY output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN detect status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

Table 3. Device-Related Signals

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
BRCLK	20	I	5.0688MHz clock input to the internal baud rate generator. Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1X the programmed baud rate.*
$\overline{TxC}$	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, the pin becomes an output at 1X the programmed baud rate.*
RxD	3	I	Serial data input to the receiver. "Mark" is high, "Space" is low.
TxD	19	O	Serial data output from the transmitter. "Mark" is high, "space" is low. Held in mark condition when the transmitter is disabled.
$\overline{DSR}$	22	I	General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{DCD}$	16	I	Data carrier detect input. Must be low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{CTS}$	17	I	Clear to send input. Must be low in order for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register will be transmitted before termination.
$\overline{DTR}$	24	O	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.
$\overline{RTS}$	23	O	General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send.

NOTE:
*$\overline{RxC}$ and $\overline{TxC}$ outputs have short circuit protection max. C_L = 100pF

Transmitter

The PCI is conditioned to transmit data when the $\overline{CTS}$ input is Low and the TxEN command register bit is set. The SCN2651 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated. Data is transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the send break command bit high.

In the synchronous mode, when the SCN2651 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the PCI unless the CPU fails to send a new character to the PCI by the time the transmitter has completed sending the previous character.

Since synchronous communication does not allow gaps between characters, the PCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1–SYN2 doublets, or DLE–SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the transmit data holding register. If the send DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the THR.

PCI PROGRAMMING

Prior to initiating data communications, the SCN2651 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The PCI can be reconfigured at any time during program execution. However, if the change has an effect on the reception of a character the receiver should be disabled. Alternatively if the change is made 1 1/2 RxC periods after RxRDY goes active it will affect the next character assembly. A flowchart of the initialization process appears in Figure 1.

The internal registers of the PCI are accessed by applying specific signals to the $\overline{CE}$, R/$\overline{W}$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in table 4.

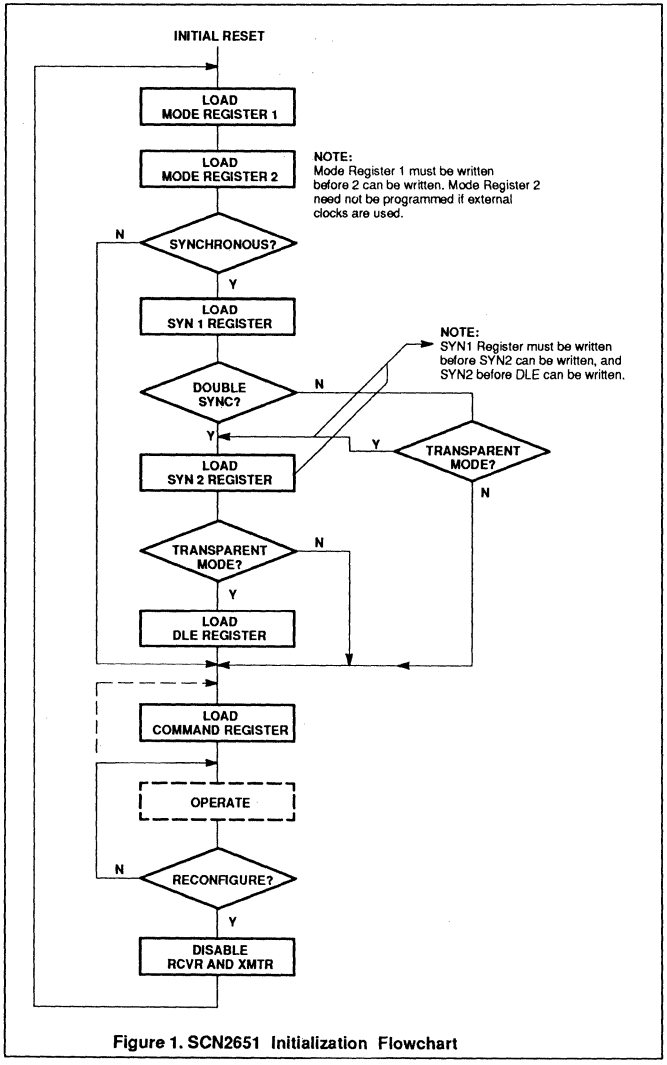


Figure 1. SCN2651 Initialization Flowchart

Table 4. SCN2651 Register Addressing

$\overline{CE}$	A_1	A_0	R/$\overline{W}$	FUNCTION
1	X	X	X	3-State data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1/2
0	1	0	1	Write mode registers 1/2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE:
See AC Characteristics section for timing requirements.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions $A_1 = 0$, $A_0 = 1$, and R/$\overline{W}$ = 1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses mode register 1, and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a "read command register" operation, but are unaffected by any other read or write operation.

The SCN2651 register formats are summarized in Tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the PCI, while the command register controls the operation within this basic framework. The PCI indicates its status in the status register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates mode register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 1X baud rate is programmed, 1.5 stop bits default to 1 stop bit on transmit.) In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1–SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE–SYN1 is used for character fill and SYN detect, but he normal synchronization sequence is used. Also DLE stripping and DLE detect (with MR14 = 0) are enabled.

Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21, and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable. When driven by a 5.0688MHz input at the BRCLK input (pin 20), the BRG output has zero error except at 134.5 2000, and 19,200 baud, which have errors of +0.016%, +0.235%, and +3.125% respectively.

MR25 and MR24 select either the BRG or the eexternal inputs $\overline{TxC}$ and $\overline{RxC}$ as the clock source for the transmitter and receiver, respectively. If the BRG clock is selected, the baud rate factor in asynchronous mode is 16X regardless of the factor selected by MR11 and MR10. In addition, the corresponding clock pin provides an output at 1X the baud rate.

Table 5. Mode Register 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
		Parity Type	**Parity Control**	**Character Length**		**Mode and Baud Rate Factor**	
Async: Stop bit length 00 = Invalid 01 = 1 Stop bit 10 = 1 1/2 Stop bits 11 = 2 Stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 Bits 01 = 6 Bits 10 = 7 Bits 11 = 8 Bits		00 = Synchronous 1X rate 01 = Asynchronous 1X rate 10 = Asynchronous 16X rate 11 = Asynchronous 64X rate	
Sync: Number of SYN char 0 = Double SYN 1 = Single SYN	**Sync: Transparency control** 0 = Normal 1 = Transparent						

NOTE:
Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

Table 6. Mode Register 2 (MR2)

MR27	MR26	MR25	MR24	MR23	MR22	MR21	MR20
		Transmitter Clock	**Receiver Clock**	**Baud Rate Selection**			
Not used		0 = External 1 = Internal	0= External 1 = Internal	0000 = 50 Baud 0001 = 75 0010 = 110 0011 = 134.5 0100 = 150 0101 = 300 0110 = 600 0111 = 1200		1000 = 1800 Baud 1001 = 2000 1010 = 2400 1011 = 3600 1100 = 4800 1101 = 7200 1110 = 9600 1111 = 19,200	

Table 7. Command Register (CR)

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		**Request to Send**	**Reset Error**		**Receive Control (RxEN)**	**Data Terminal Ready**	**Transmit Control (TxEN)**
00 = Normal operation 01 = Async: automatic echo mode Sync: SYN and/or DLE stripping mode 10 = Local Loopback 11 = Remote Loopback		0 = Force $\overline{RTS}$ output high 1 = Force $\overline{RTS}$ output low	0 = Normal 1 = Reset error flag in status reg (FE, OE, PE/DLE DETECT)	**Async: Force Break** 0 = Normal 1 = Force break **Sync Send DLE** 0 = Normal 1 = Send DLE	0 = Disable 1 = Enable	0 = Force $\overline{DTR}$ output high 1 = Force $\overline{DTR}$ output low	0 = Disable 1 = Enable

Table 8. Status Register (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT/ DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ input is high 1 = $\overline{DSR}$ input is low	0 = $\overline{DCD}$ input is high 1 = $\overline{DCD}$ input is low	**Async:** 0 = Normal 1 = Framing ERROR **Sync:** 0 = Normal 1 = SYN char detected	0 = Normal 1 = Overrun error	**Async:** 0 = Normal 1 = Parity error **Sync:** 0 = Normal 1 = Parity error or DLE char received	0 = Normal 1 = Change in $\overline{DSR}$ or $\overline{DCD}$, or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register empty

Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high) while $\overline{TxRDY}$ and $\overline{TxEMT}$ will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected.

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs is the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the transmit data holding register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the transmit data holding register. CR3 should be reset in response to the next TxRDY.

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit.

The PCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational submode is determined by CR7 and CR6. CR7 – CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the mode and status register instructions.

In asynchronous mode, CR7 – CR6 = 01 places the PCI in the automatic echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected.

The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ output = **1.**
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7 – CR6 = 01 places the PCI in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17 – MR16 = 10), characters in the data stream matching SYN1 are not transferred to the receive data holding register (RHR).
2. In the non-transparent, double SYN mode (MR17 – MR16 = 00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred the RHR. However, only the first SYN1 of an SYN1 – SYN1 pair is stripped.
3. In transparent mode (MR16 = 1), character in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE–DLE pair is stripped.

Note that automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

Two diagnostic submodes can also be configured. In local loopback mode (CR7 – CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the PCI.

The second diagnostic mode is the remote loopback mode (CR7 – CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data is sent to the local CPU, but he error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high.
5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the status register (as shown in Table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit shift register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is low. In the automatic echo and remote loopback modes, the output is held high.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG condition is enabled when TxEN = 1 or RxEN = 1. If the status register is read twice and SR2 = 1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. It is cleared when the status register is read by the CPU. When SR2 is set, the $\overline{\text{TxEMT/DSCHG}}$ output is low.

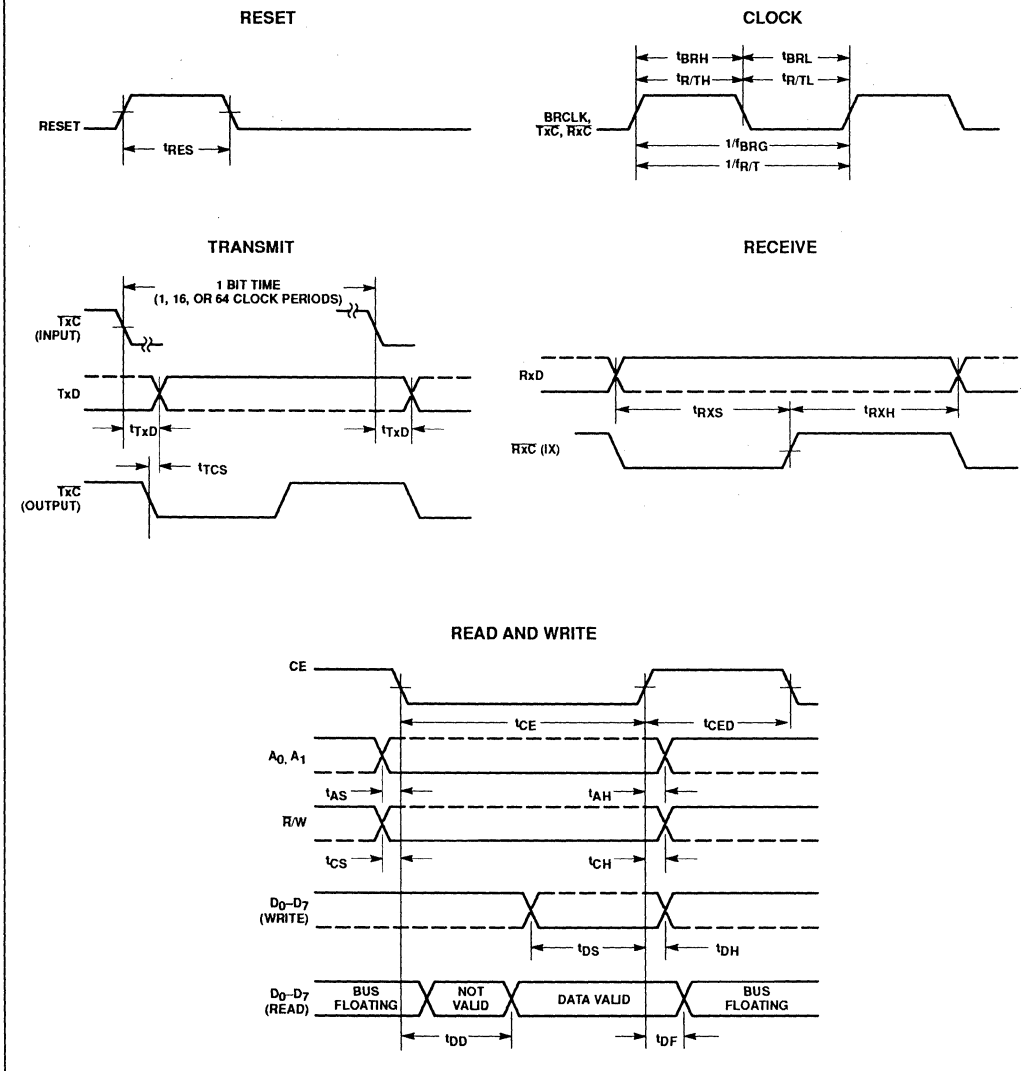
SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching the DLE register has been received. However, only the first DLE of two successive DLEs will set SR3. This bit is cleared when the receiver is disabled and by the reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the reset error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by the programmed number of stop bits. (If 1.5 stop bits are programmed, only the first stop bit is checked.) If RHR = 0 when SR5 = 1, a break condition is present. In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1 – SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1 – SYN2) and, after synchronization has been achieved, when a DLE–SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, and when the status register is read by the CPU in the synchronous mode.

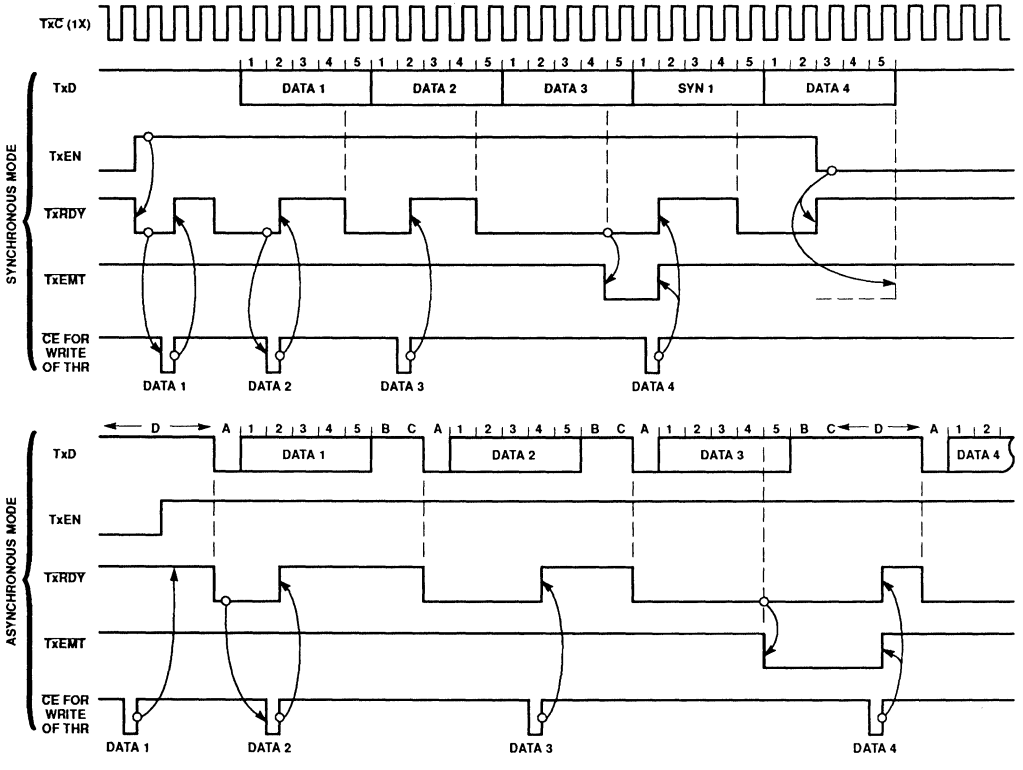
SR6 and SR7 reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs respectively. A low input sets its corresponding status bit and a high input clears it.

TIMING DIAGRAMS



TIMING DIAGRAMS (Continued)

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

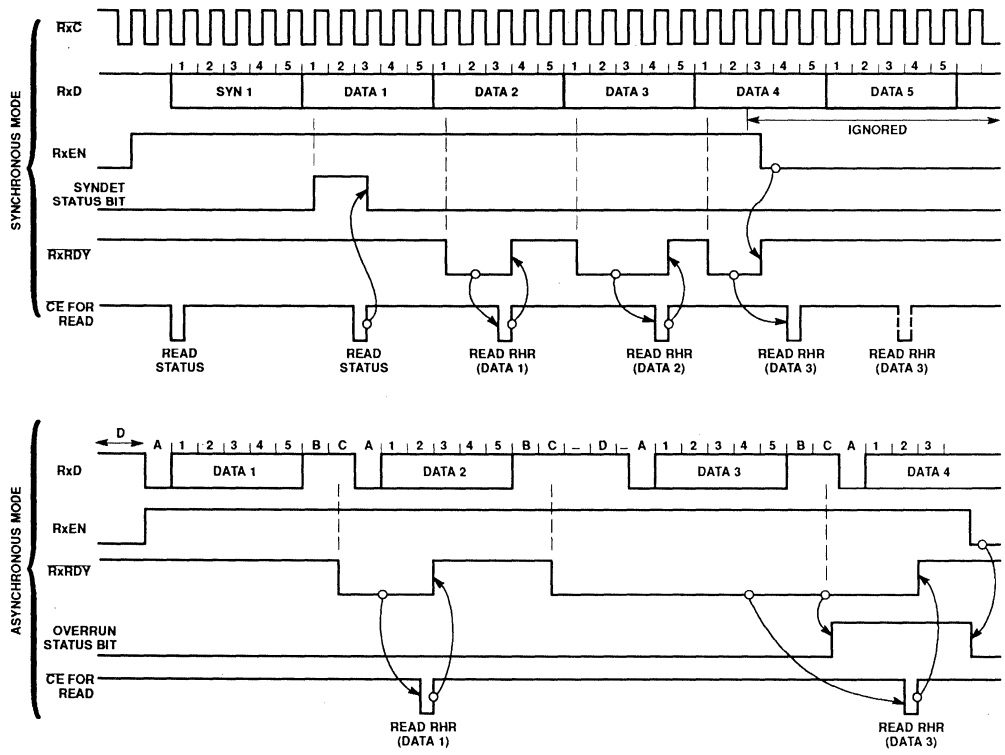


NOTES:

A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

TIMING DIAGRAMS (Continued)

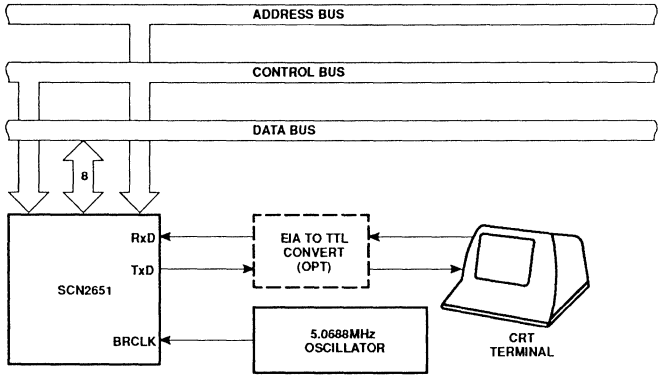
RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



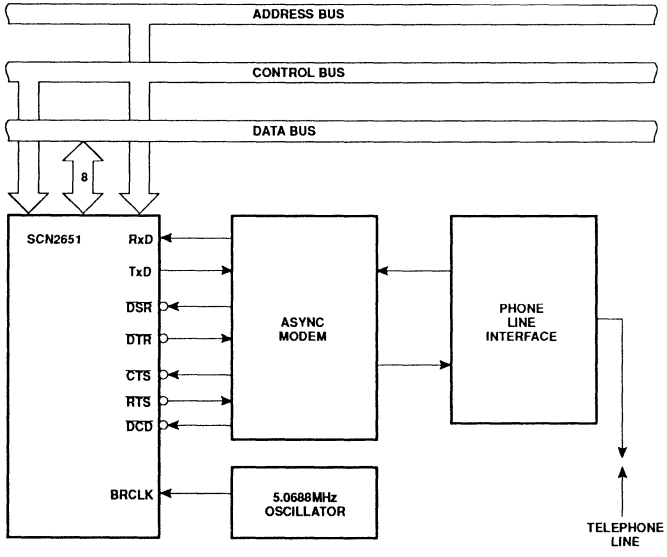
NOTES:
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TYPICAL APPLICATIONS

ASYNCHRONOUS INTERFACE TO CRT TERMINAL

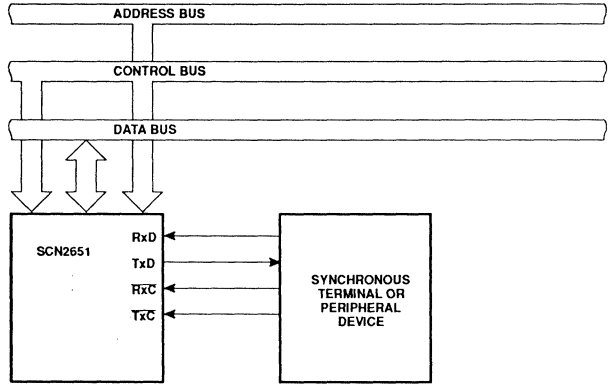


ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

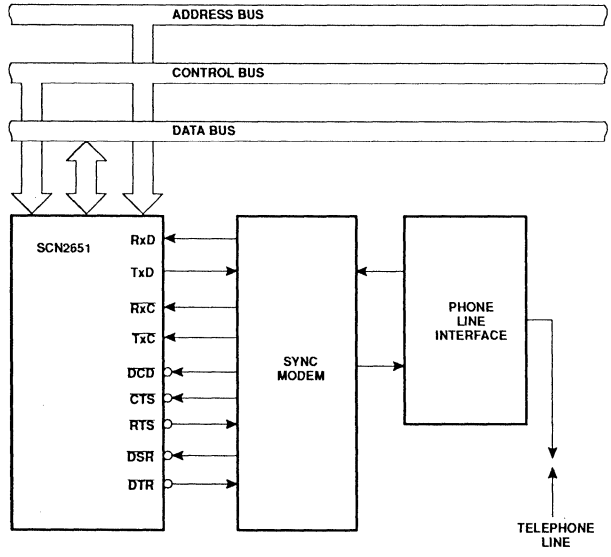


TYPICAL APPLICATIONS (Continued)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



Philips Components–Signetics

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Status	Product Specification
Data Communication Products	

SCN2652/SCN68652

Multi-protocol communications controller (MPCC)

DESCRIPTION

The SCN2652/68652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus.

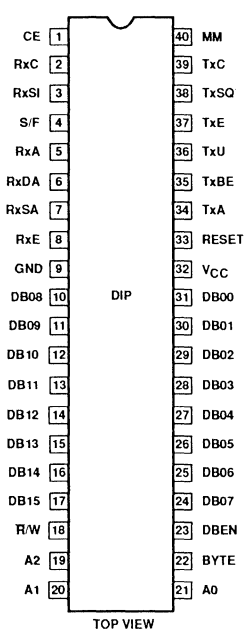
FEATURES

- DC to 1Mbps or 2Mbps data rate
- Bit-oriented protocols (BOP): SDLC, ADCCP, HDLC
- Byte-control protocols (BCP): DDCMP, BISYNC (external CRC)
- Programmable operation
  - 8 or 16-bit tri-state data bus
  - Error control – CRC or VRC or none
  - Character length – 1 to 8 bits for BOP or 5 to 8 bits for BCP
  - SYNC or secondary station address comparison for BCP-BOP
  - Idle transmission of SYNC/FLAG or MARK for BCP-BOP
- Automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA
- Zero insertion and deletion for BOP
- Short character detection for last BOP data character
- SYNC generation, detection, and stripping for BCP
- Maintenance mode for self-testing
- TTL compatible
- Single +5V supply

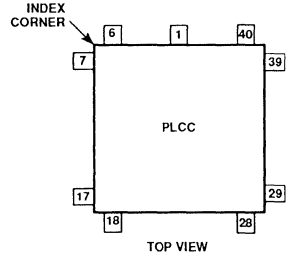
APPLICATIONS

- Intelligent terminals
- Line controllers
- Network processors
- Front end communications
- Remote data concentrators
- Communication test equipment
- Computer to computer links

PIN CONFIGURATION



TOP VIEW



TOP VIEW

Pin	Function	Pin	Function
1	NC	23	NC
2	CE	24	A0
3	RxC	25	BYTE
4	RxSI	26	DBEN
5	S/F	27	DB07
6	RxA	28	DB06
7	RxDA	29	DB05
8	RxSA	30	DB04
9	RxE	31	DB03
10	GND	32	DB02
11	DB08	33	DB01
12	NC	34	NC
13	DB09	35	DB00
14	DB10	36	V_{CC}
15	DB11	37	RESET
16	DB12	38	TxA
17	DB13	39	TxBE
18	DB14	40	TxU
19	DB15	41	TxE
20	R/W	42	TxSQ
21	A2	43	TxC
22	A1	44	MM

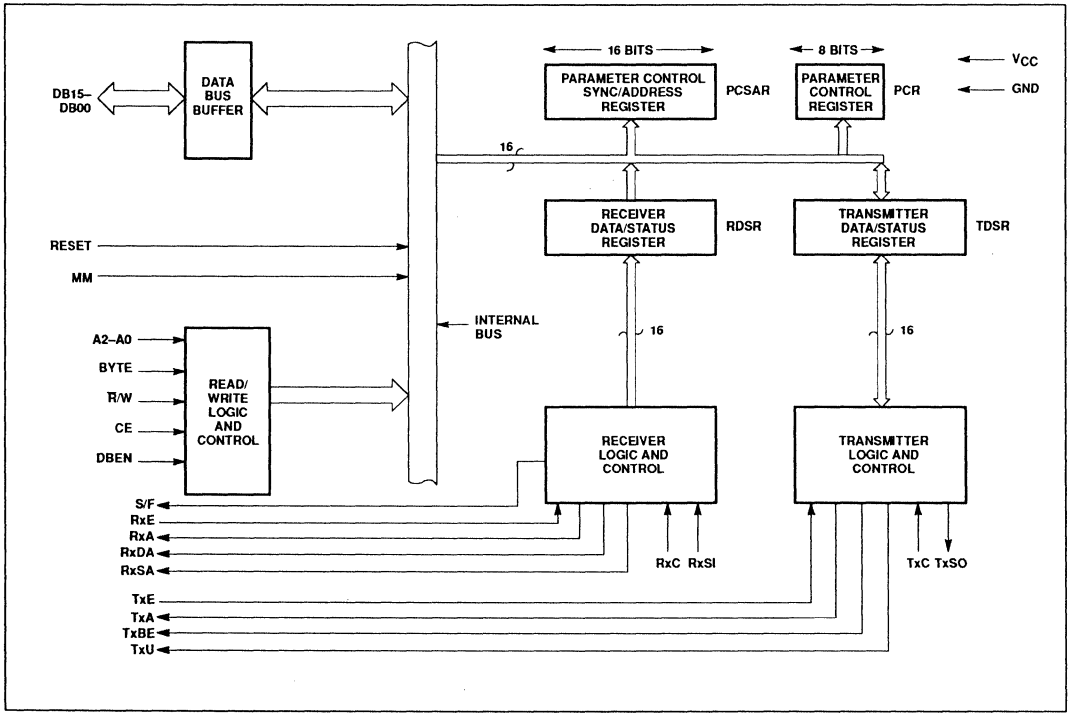
NOTE: 00 is least significant bit, highest number (that is, DB15, A2) is most significant bit.

ORDERING CODE

PACKAGES		V_{CC} = 5V ±5%		
		Commercial	Automotive	Extended
		0°C to +70°C	–40°C to +85°C	–55°C to +125°C
Ceramic DIP	2MHz	SCN2652AC2F40	SCN2652AA2F40	SCN2652AM2F40
Plastic DIP	2MHz	SCN2652AC2N40	Contact Factory	Not Available
Plastic LCC	2MHz	SCN2652AC2A44	Contact Factory	Not Available

NOTE:
SCN68652 is identical to SCN2652. Order using part numbers shown above.

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB15–DB00	17–10 24–31	I/O	**Data Bus:** DB07–DB00 contain bidirectional data while DB15–DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be wire OR'ed onto an 8-bit bus. The data bus is floating if either CE or DBEN are low.
A2–A0	19–21	I	**Address Bus:** A2–A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	**Byte:** Single byte (8-bit) data bus transfers are specified when this input is high. A low level specifies 16-bit data bus transfers.
CE	1	I	**Chip Enable:** A high input permits a data bus operation when DBEN is activated.
R/W	18	I	**Read/Write:** R/W controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register. A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	**Data Bus Enable:** After A2–A0, CE, BYTE and R/W are set up, DBEN may be strobed. During a read, the 3-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed.
RESET	33	I	**Reset:** A high level initializes all internal registers (to zero) and timing.
MM	40	I	**Maintenance Mode:** MM internally gates TxSO back to RxSI and TxC to RxC for off line diagnostic purposes. The RxC and RxSI inputs are disabled and TxSO is high when MM is asserted.
RxE	8	I	**Receiver Enable:** A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing.
RxA	5	O	**Receiver Active:** RxA is asserted when the first data character of a message is ready for the processor. In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if strip-SYNC ($PCSAR_{13}$) is set, the first non-SYNC character is the first data character; if strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA. In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	**Receiver Data Available:** RxDA is asserted when an assembled character is in $RDSR_L$ and is ready to be presented to the processor. This output is reset when $RDSR_L$ is read.
RxC	2	I	**Receiver Clock:** RxC (1X) provides timing for the receiver logic. The positive going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	**SYNC/FLAG:** S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected.
RxSA*	7	O	**Receiver Status Available:** RxSA is asserted when there is a zero to one transition of any bit in $RDSR_H$ except for RSOM. It is cleared when $RDSR_H$ is read.
RxSI	3	I	**Receiver Serial Input:** RxSI is the received serial data. Mark = '1', space = '0'.
TxE	37	I	**Transmitter Enable:** A high level input enables the transmitter data path between $TDSR_L$ and TxSO. At the end of a message, a low level input causes TxSO = 1(mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output on TxSO.
TxA	34	O	**Transmitter Active:** TxA is asserted after TSOM ($TDSR_8$) is set and TxE is raised. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxSO.
TxBE*	35	O	**Transmitter Buffer Empty:** TxBE is asserted when theTDSR is ready to be loaded with new control information or data. The processor should respond by loading theTDSR which resets TxBE.
TxU*	36	O	**Transmitter Underrun:** TxU is asserted during a transmit sequence when the service of TxBE has been delayed for one character time. This indicates the processor is not keeping up with the transmitter. Line fill depends on $PCSAR_{11}$. TxU is reset by RESET or setting of TSOM ($TDSR_8$), synchronized by the falling edge of TxC.
TxC	39	I	**Transmitter Clock:** TxC (1X) provides timing for the transmitter logic. The positive going edge shifts data out of the TxSR to TxSO.
TxSO	38	O	**Transmitter Serial Output:** TxSO is the transmitted serial data. Mark = '1', space = '0'.
V_{CC}	32	I	**+5V:** Power supply.
GND	9	I	**Ground:** 0V reference ground.

*Indicates possible interrupt signal

Table 1. Glossary

REGISTERS		NO. OF BITS	DESCRIPTION*
Addressable			
PCSAR	Parameter control sync/ address register	16	$PCSAR_H$ and PCR contain parameters common to the receiver and transmitter. $PCSAR_L$ contains a programmable SYNC character (BCP) or secondary station address (BOP).
PCR	Parameter control register	8	
RDSR	Receive data/status register	16	$RDSR_H$ contains receiver status information. $RDSR_L$ = RxDB contains the received assembled character.
TDSR	Transmit data/status register	16	$TDSR_H$ contains transmitter command and status information. TDSRL = TxDB contains the character to be transmitted
Internal			
CCSR	Control character shift register	8	These registers are used for character assembly (CSSR, HSR, RxSR), disassembly (TxSR), and CRC accumulation/generation (RxCRC, TxCRC).
HSR	Holding shift register	16	
RxSR	Receiver shift register	8	
TxSR	Transmitter shift register	8	
RxCRC	Receiver CRC accumulation register	16	
TxCRC	Transmitter CRC generation register	16	

NOTES:
*H = High byte – bits 15–8
L = Low byte – bits 7–0

FUNCTIONAL DESCRIPTION

The MPCC can be functionally partitioned into receiver logic, transmitter logic, registers that can be read or loaded by the processor, and data bus control circuitry. The register bit formats are shown in Figure 1 while the receiver and transmitter data paths are depicted in Figures 2 and 3.

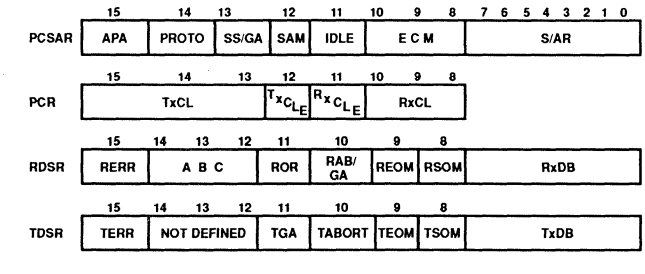
Table 2. Error Control

CHARACTER	DESCRIPTION
FCS	Frame check sequence is transmitted/received as 16 bits following the last data character of a BOP message. The divisor is usually CRC–CCITT ($X^{16} + X^{12} + X^5 + 1$) with dividend preset to 1's but can be other wise determined by ECM. The inverted remainder is transmitter as the FCS.
BCC	Block check character is transmitted/received as two successive characters following the last data character of a BCP message. The polynomial is CRC–16 ($X^{16} + X^{15} + X^2 + 1$) or CRC–CCITT with dividend preset to 0's (as specified by ECM). The true remainder is transmitted as the BCC.

Table 3. Special Characters

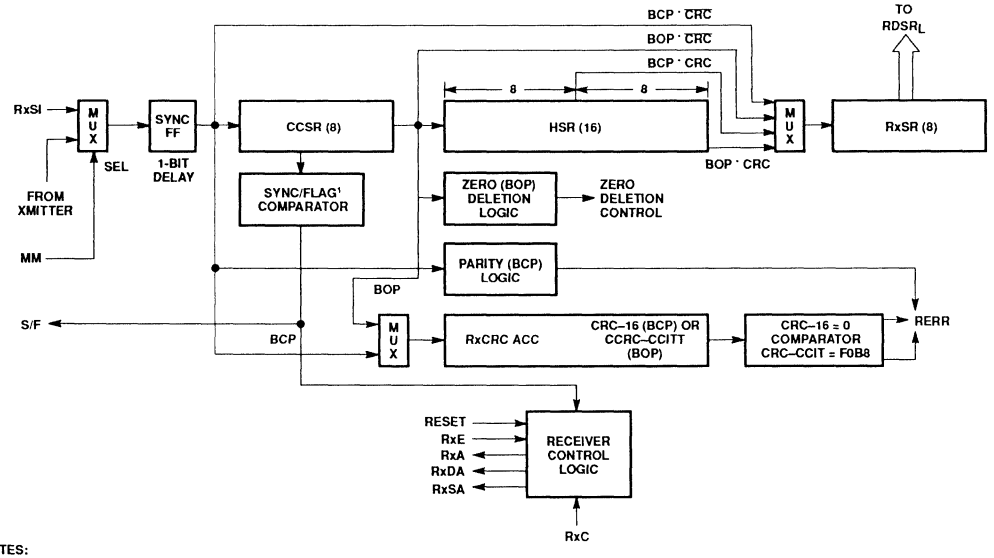
OPERATION	BIT PATTERN	FUNCTION
BOP		
FLAG	0 1 1 1 1 1 1 0	Frame message
ABORT	1 1 1 1 1 1 1 1 generation 0 1 1 1 1 1 1 1 detection	Terminate communication
GA	0 1 1 1 1 1 1 1	Terminate loop mode repeater function
Address	$(PCSAR_L)$[1]	Secondary station address
BCP		
SYNC	$(PCSAR_L)$ or (TxDB)[2] generation	Character synchronization

NOTES:
1. ( ) = contents of.
2. For IDLE = 0 or 1 respectively.



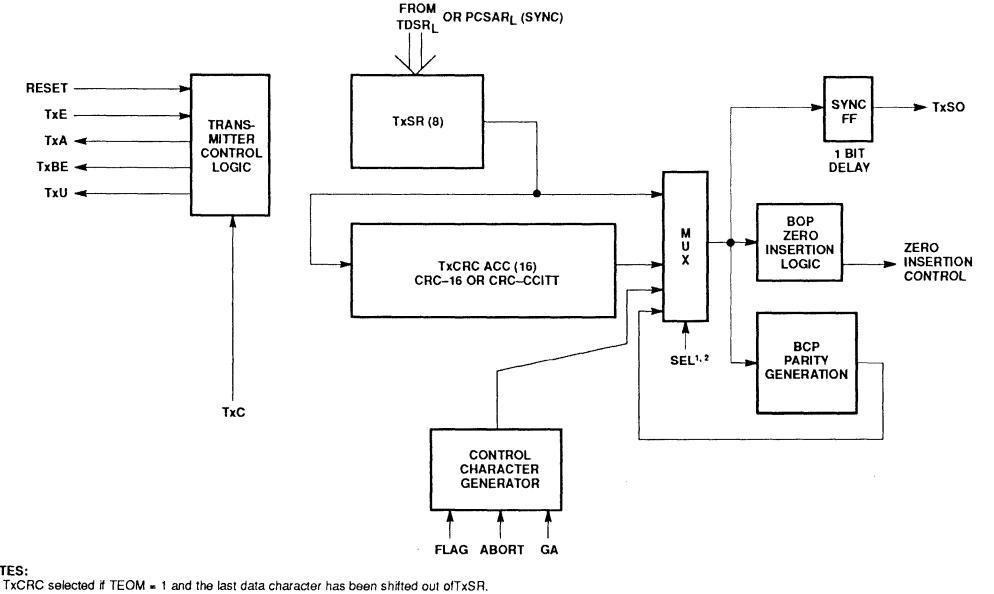
NOTE:
Refer to Register Formats for mnemonics and description.

Figure 1. Short Form Register Bit Formats



NOTES:
1. Detected in SYNC FF and 7 MS bits of CCSR.
2. In BOP mode, a minimum of two data characters must be received to turn the receiver active.

Figure 2. MPCC Receiver Data Path



NOTES:
1. TxCRC selected if TEOM = 1 and the last data character has been shifted out of TxSR.
2. In BCP parity selected will be generated after each character is shifted out of TxSR.

Figure 3. MPCC Transmitter Data Path

RECEIVER OPERATION

General

After initializing the parameter control registers (PCSAR and PCR), the RxE input must be set high to enable the receiver data path. The serial data on the RxSI is synchronized and shifted into an 8-bit Control Character Shift Register (CCSR) on the rising edge of RxC. A comparison between CCSR contents and the FLAG (BOP) or SYNC (BCP) character is made until a match is found. At that time, the S/F output is asserted for one RxC time and the 16-bit Holding Shift Register (HSR) is enabled. The receiver then operates as described below.

BOP Operation

A flowchart of receiver operation in BOP mode appears in Figure 4. Zero deletion (after five ones are received) is implemented on the received serial data so that a data character will not be interpreted as a FLAG, ABORT, or GA. Bits following the FLAG are shifted through the CCSR, HSR, and into the Receiver Shift Register (RxSR). A character will be assembled in the RxSR and transferred to the $RDSR_L$ for presentation to the processor. At that time the RxDA output will be asserted and the processor must take the character no later than one RxC time after the next character is assembled in the RxSR. If not, an overrun ($RDSR_{11} = 1$) will occur and succeeding characters will be lost.

The first character following the FLAG is the secondary station address. If the MPCC is a secondary station ($PCSAR_{12} = 1$), the contents of RxSR are compared with the address stored in $PCSAR_L$. A match indicates the forthcoming message is intended for the station; the RxA output is asserted, the character is loaded into $RDSR_L$, RxDA is asserted and the Receive Start of Message bit (RSOM) is set. No match indicates that another station is being addressed and the receiver searches for the next FLAG.

If the MPCC is a primary station, ($PCSAR_{12} = 0$), no secondary address check is made; RxA is asserted and RSOM is set once the first non-FLAG character has been loaded into $RDSR_L$ and RxDA has been asserted. Extended address field can be supported by software if $PCSAR_{12} = 0$.

When the 8 bits following the address character have been loaded into $RDSR_L$ and RxDA has been asserted, RSOM will be cleared. The processor should read this 8-bit character and interpret it as the Control field.

Received serial data that follows is read and interpreted as the information field by the processor. It will be assembled into character lengths as specified by PCR_{8-10}. As before, RxDA is asserted each time a character has been transferred into $RDSR_L$ and is cleared

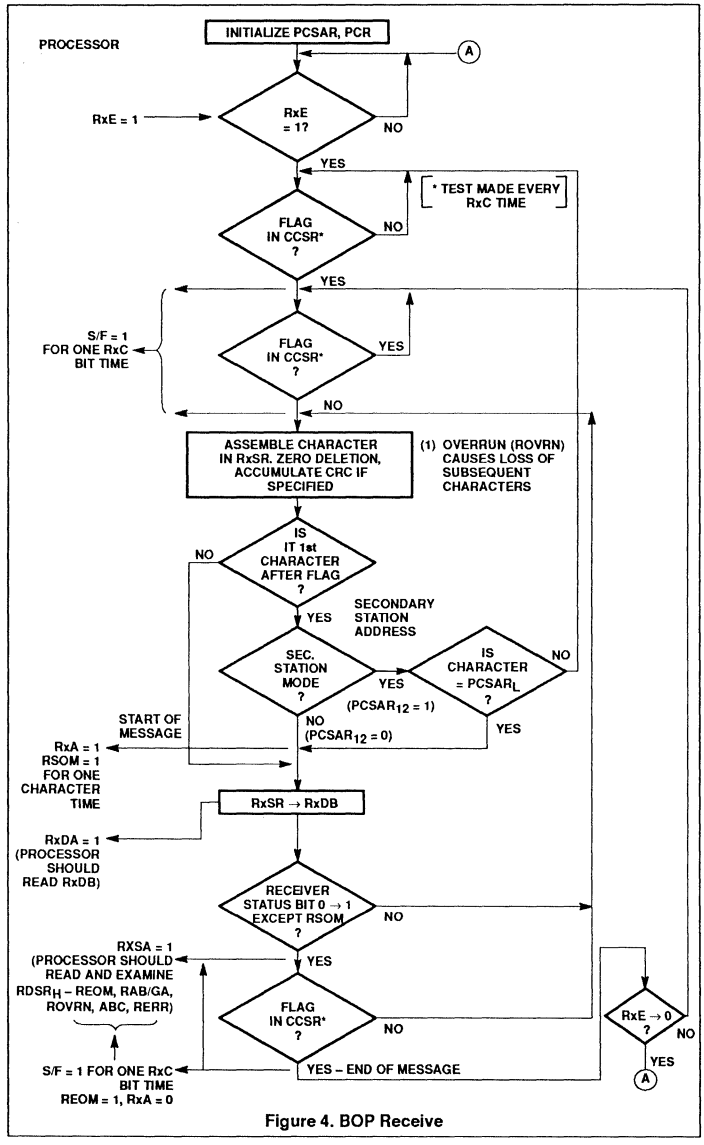


Figure 4. BOP Receive

when $RDSR_L$ is read by the processor. $RDSR_H$ should only be read when RxSA is asserted. This occurs on a zero to one transition of any bit in $RDSR_H$ except for RSOM. RxSA and all bits in $RDSR_H$ except RSOM are cleared when $RDSR_H$ is read. The processor should check $RDSR_{9-15}$ each time RxSA is asserted. If $RDSR_9$ is set, then $RDSR_{12-15}$ should be examined.

Receiver character length may be changed dynamically in response to RxDA: read the character in RxDB and write the new character length into RxCL. The character length will be changed on the next receiver character boundary. A received residual (short) character will be transferred into RxDB after the previous character in RxDB has been read, i.e. there will not be an overrun. In general the last two characters are protected from overrun.

The CRC–CCITT, if specified by $PCSAR_{8-10}$, is accumulated in RxCRC on each character following the FLAG. When the closing FLAG is detected in the CCSR, the received CRC is in the 16-bit HSR. At that time, the Receive End of Message bit (REOM) will be set; RxSA and RxDA will be asserted. The processor should read the last data character in $RDSR_L$ and the receiver status in $RDSR_{9-15}$. If $RDSR_{15} = 1$, there has been a transmission error; the accumulated CRC–CCITT is incorrect. If $RDSR_{12-14} \neq 0$, last data character is not of prescribed length. Neither the received CRC nor closing FLAG are presented to the processor. The processor may drop RxE or leave it active at the end of the received message.

BCP Operation

The operation of the receiver in BCP mode is shown in Figure 5. The receiver initially searches for two successive SYNC characters, of length specified by PCR_{8-10}, that match the contents of $PCSAR_L$. The next non-SYNC character or next SYNC character, if stripping is not specified ($PCSAR_{13} = 0$), causes RxA to be asserted and enables the receiver data path. Once enabled, all characters are assembled in RxSR and loaded into $RDSR_L$. RxDA is active when a character is available in $RDSR_L$. RxSA is active on a 0 to 1 transition of any bit in $RDSR_H$. The signals are cleared when RDSRl or $RDSR_H$ are read respectively.

If CRC–16 error control is specified by $PCSAR_{8-10}$, the processor must determine the last character received prior to the CRC field. When that character is loaded into $RDSR_L$ and RxDA is asserted, the received CRC will be in CCSR and HSR_L. To check for a transmission error, the processor must read the receiver status ($RDSR_H$) and examine $RDSR_{15}$. This bit will be set for one character time if an error free message has been received. If $RDSR_{15} = 0$, the CRC–16 is in error. The state of $RDSR_{15}$ in BCP CRC mode does not set RxSA. Note that this bit should be examined only at the end of a message. The accumulated CRC will include all characters starting with the first non-SYNC character if $PCSAR_{13} = 1$, or the character after the opening two SYNCs if $PCSAR_{13} = 0$. This necessitates external CRC generation/checking when supporting IBM's BISYNC. This can be accomplished using the Signetics SCN2653 Polynomial Generator/Checker. See Typical Applications.

If VRC has been selected for error control, parity (odd or even) is regenerated on each character and checked when the parity bit is received. A discrepancy causes $RDSR_{15}$ to be set and RxSA to be asserted. This must be sensed by the processor. The received parity bit is stripped before the character is presented to the processor.

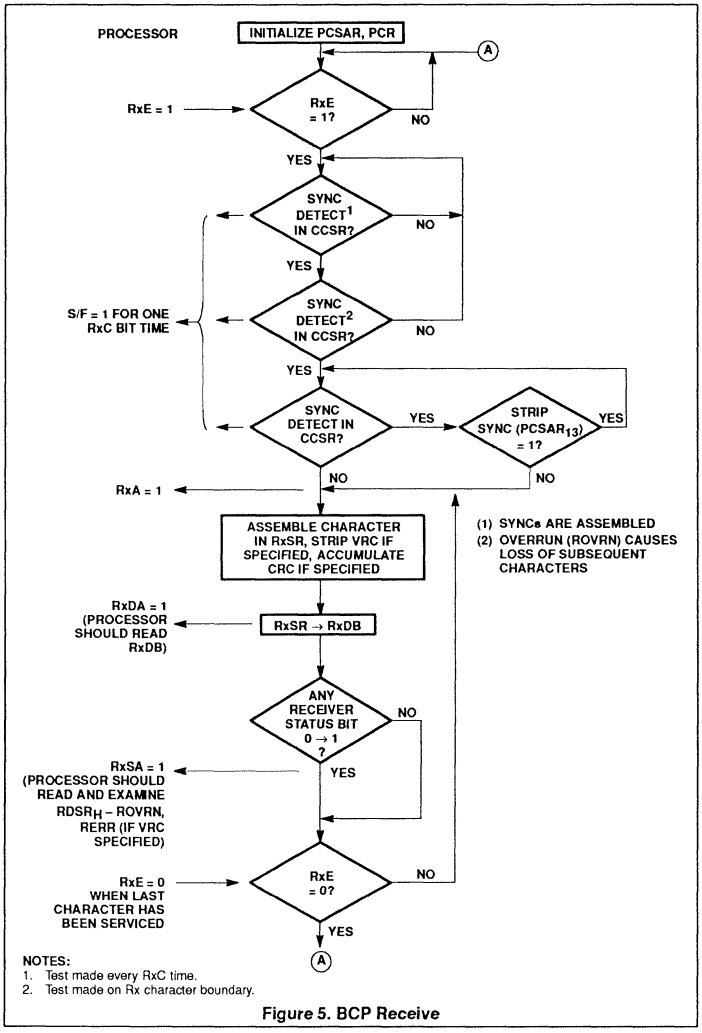


Figure 5. BCP Receive

When the processor has read the last character of the message, it should drop RxE which disables the receiver logic and initializes all receiver registers and timing.

TRANSMITTER OPERATION

General

After the parameter control registers (PCSAR and PCR) have been initialized, TxSO is held at mark until TSOM ($TDSR_8$) is set and TxE is raised. Then, transmitter operation depends on protocol mode.

BOP Operation

Transmitter operation for BOP is shown in Figure 6. A FLAG is sent after the processor sets the Transmit Start of Message bit (TSOM) and raises TxE. The FLAG is used to synchronize the message that follows. TxA will also be asserted. When TxBE is asserted by the MPCC, the processor should load $TDSR_L$ with the first character of the message. TSOM should be cleared at the same time $TDSR_L$ is loaded (16-bit data bus) or immediately thereafter (8-bit data bus). FLAGS are sent as long as TSOM = 1. For counting the number of FLAGs, the processor

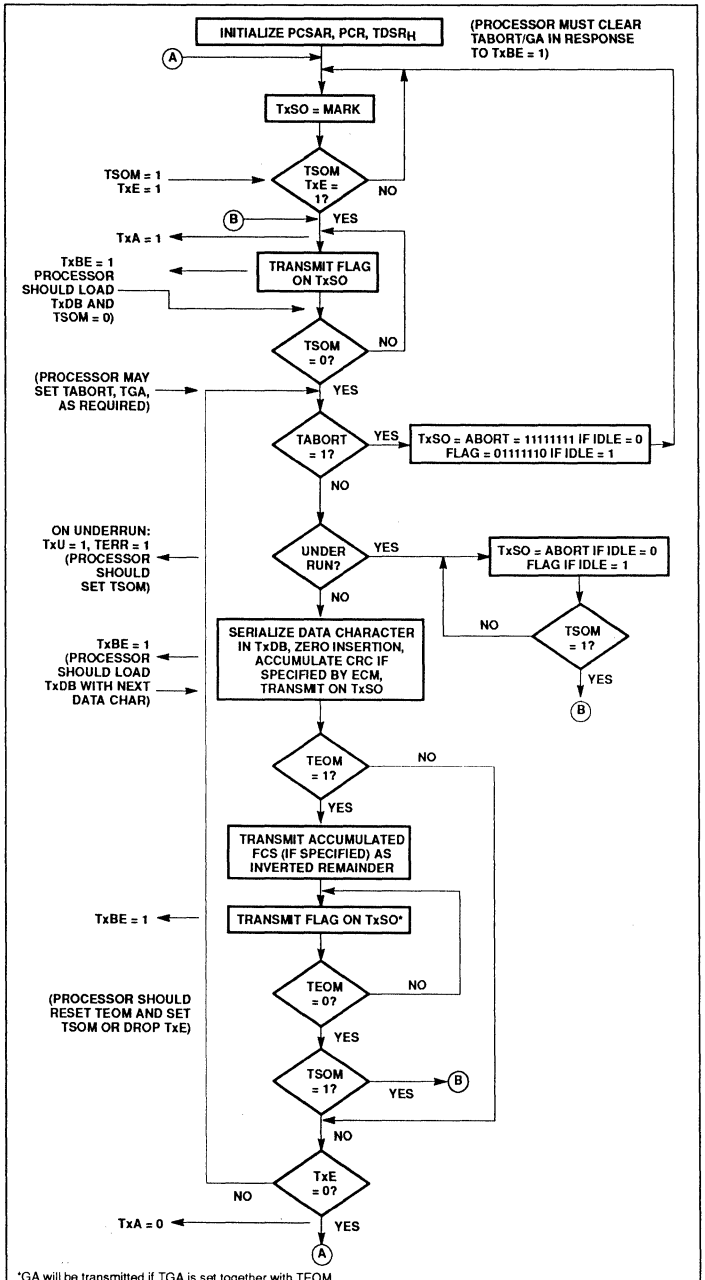


Figure 6. BOP Transmit

should reassert TSOM in response to the assertion of TxBE.

All succeeding characters are loaded into TDSR$_L$ by the processor when TxBE = 1. Each character is serialized in TxSR and transmitted on TxSO. Internal zero insertion logic stuffs a "0" into the serial bit stream after five successive "1s" are sent. This insures a data character will not match a FLAG, ABORT, or GA reserved control character. As each character is transmitted, the Frame Check Sequence (FCS) is generated as specified by Error Control Mode (PCSAR$_{8-10}$). The FCS should be the CRC–CCITT polynomial ($X^{16} + X^{12} + X^5 + 1$) preset to 1s. If an underrun occurs (processor is not keeping up with the transmitter), TxU and TERR (TDSR$_{15}$) will be asserted with ABORT or FLAG used as the TxSO line fill depending on the state of IDLE (PCSAR$_{11}$). The processor must set TSOM to reset the underrun condition. To retransmit the message, the processor should proceed with the normal start of message sequence.

A residual character of 1 to 7 bits may be transmitted at the end of the information field. In response to TxBE, write the residual character length into TxCL and load TxDB with the residual character. Dynamic alteration of character length should be done in exactly the same sequence. The character length will be changed on the next transmit character boundary.

After the last data character has been loaded into TDSR$_L$ and sent to TxSR (TxBE = 1), the processor should set TEOM (TDSR$_9$). The MPCC will finish transmitting the last character followed by the FCS and the closing FLAG. The processor should clear TEOM and drop TxE when the next TxBE is asserted. This corresponds to the start of closing FLAG transmission. When TxE has been dropped. TxA will be low 1 1/2 bit times after the last bit of the closing FLAG has been transmitted. TxSO will be marked after the closing FLAG has been transmitted.

If TxE and TEOM are high, the transmitter continues to send FLAGs. The processor may initiate the next message by resetting TEOM and setting TSOM, or by loading TDSR$_L$ with a data character and then simply resetting TSOM (without setting TSOM).

BCP Operation

Transmitter operation for BCP mode is shown in Figure 7. TxA will be asserted after TSOM = 1 and TxE is raised. At that time SYNC characters are sent from PCSAR$_L$ or TDSR$_L$ (IDLE = 0 or 1) as long as TSOM = 1. TxBE is asserted at the start of transmission of the first SYNC character. For counting the number of SYNCs, the processor should reassert TSOM in response to the assertion of TxBE. When TSOM = 0 transmission is from TDSR$_L$, which must be loaded with characters from the processor each time TxBE is asserted. If this loading is delayed for more than one character time, an underrun results: TxU and TERR are asserted and the

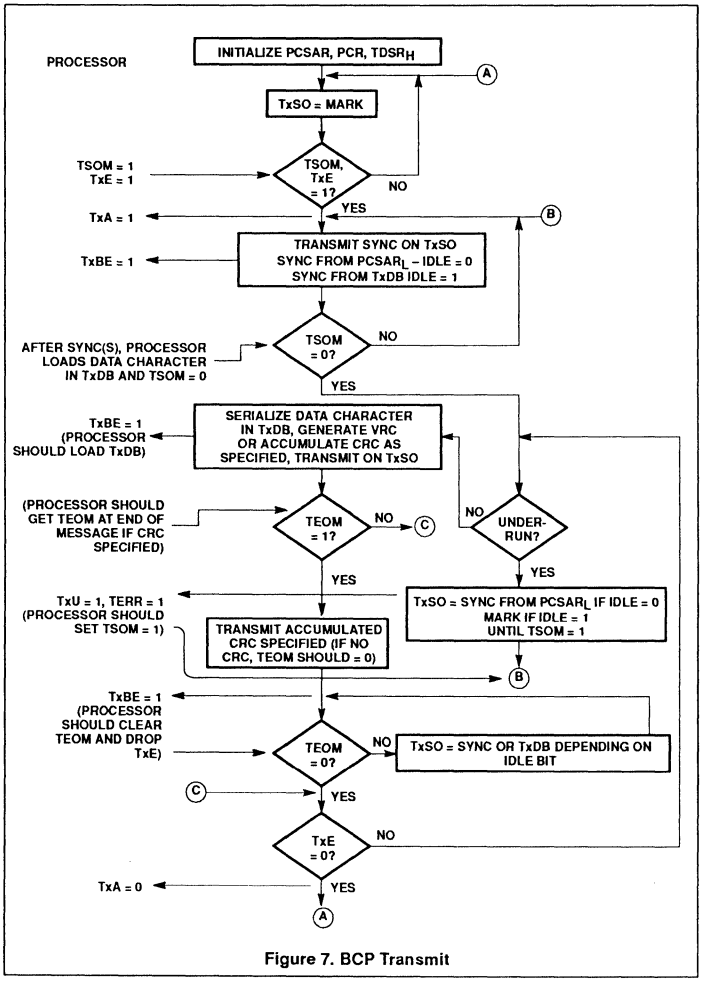


Figure 7. BCP Transmit

TxSO line fill depend on IDLE ($PCSAR_{11}$). The processor must set TSOM and retransmit the message to recover. This is not compatible with IBM's BISYNC, so that the user must not underrun when supporting that protocol.

CRC–16, if specified by $PCSAR_{8-10}$, is generated on each character transmitted from $TDSR_L$ when TSOM =0. The processor must set TEOM = 1 after the last data character has been sent to TxSR (TxBE = 1). The MPCC will finish transmitting the last data character and the CRC–16 field before sending SYNC characters which are transmitted as long as TEOM = 1. If SYNCs are not desired after CRC–16 transmission, the processor should clear TEOM and lower TxE when the TxBE corresponding to the start of CRC–16 transmission is asserted. When TEOM = 0, the line is marked and a new message may be initiated by setting TSOM and raising TxE.

If VRC is specified, it is generated on each data character and the data character length must not exceed 7 bits. For software LRC or CRC, TEOM should be set only if SYNC's are required at the end of the message block.

Special Case

The capability to transmit 16 spaces is provided for line turnaround in half duplex mode or for a control recovery situation. This is achieved by setting TSOM and TEOM, clearing TEOM when TxBE = 1, and proceeding as required.

PROGRAMMING

Prior to initiating data transmission or reception, PCSAR and PCR must be loaded with control information from the processor. The contents of these registers (see Register Format section) will configure the MPCC for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is disabled.

The default value for all registers is zero. This corresponds to BOP, primary station mode, 8-bit character length, FCS = CRC–CCITT preset to 1s.

For BOP mode the character length register (PCR) may be set to the desired values during system initialization. The address and control fields will automatically be 8-bits. If a residual character is to be transmitted, TxCL should be changed to the residual character length prior to transmission of that character.

DATA BUS CONTROL

The processor must set up the MPCC register address (A2–A0), chip enable (CE), byte select (BYTE), and read/write (R/W) inputs before each data bus transfer operation.

During a read operation (R/W = 0), the leading edge of DBEN will initiate an MPCC read cycle. The addressed register will place its contents on the data bus. If BYTE = 1, the 8-bit byte is placed on DB15–08 or DB07–00 depending on the H/L status of the register addressed. Unused bits in $RDSR_L$ are zero. If BYTE = 0, all 16 bits (DB15–00) contain MPCC information. The trailing edge of DBEN will reset RxDA and/or RxSA if $RDSR_L$ or $RDSR_H$ is addressed respectively.

DBEN acts as the enable and strobe so that the MPCC will not begin its internal read cycle until DBEN is asserted.

During a write operation (R/W = 1), data must be stable on DB_{15-08} and/or DB_{07-00} prior to the leading edge of DBEN. The stable data is strobed into the addressed register by DBEN. TxBE will be cleared if the addressed register was $TDSR_H$ or $TDSR_L$.

Table 4. MPCC Register Addressing

	A2	A1	A0	REGISTER
BYTE = 0	16-BIT DATA BUS = $DB_{15} - DB_{00}$			
	0	0	X	RDSR
	0	1	X	TDSR
	1	0	X	PCSAR
	1	1	X	PCR*
BYTE = 1	8-BIT DATA BUS = DB_{7-0} or DB_{15-8}**			
	0	0	0	$RDSR_L$
	0	0	1	$RDSR_H$
	0	1	0	$TDSR_L$
	0	1	1	$TDSR_H$
	1	0	0	$PCSAR_L$
	1	0	1	$PCSAR_H$
	1	1	0	PCR_L*
	1	1	1	PCR_H

NOTES:
* PCR lower byte does not exist. It will be all "0"s when read.
** Corresponding high and low order pins must be tied together.

Table 5. Parameter Control Register (PCR)–(R/W)

BIT	NAME	MODE	FUNCTION
00–07	Not Defined		
08–10	RxCL	BOP/BCP	Receiver character length is loaded by the processor when RxCLE = 0. The character length is valid after transmission of single byte address and control fields have been received. 10 9 8 — Char length (bits) 0 0 0 — 8 0 0 1 — 1 0 1 0 — 2 0 1 1 — 3 1 0 0 — 4 1 0 1 — 5 1 1 0 — 6 1 1 1 — 7
11	RxCLE	BOP/BCP	Receiver character length enable should be zero when the processor loads RxCL. The remaining bits of PCR are not affected during loading. Always 0 when read.
12	TxCLE	BOP/BCP	Transmitter character length enable should be zero when the processor loads TxCL. The remaining bits of PCR are not affected during loading. Always 0 when read.
13–15	TxCL	BOP/BCP	Transmitter character length is loaded by the processor when TxCLe = 0. Character bit length specification format is identical to RxCL. It is valid after transmission of single byte address and control fields.

Table 6. Parameter Control SYNC/Address Register (PCSAR)–(R/W)

BIT	NAME	MODE	FUNCTION
00–07	S/AR	BOP	SYNC/address register. Contains the secondary station address if the MPCC is a secondary station. The contents of this register is compared with the first received non-FLAG character to determine if the message is meant for this station.
		BCP	SYNC character is loaded into this register by the processor. It is used for receive and transmit bit synchronization with bit length specified by RxCL and TxCL.
08–10	ECM	BOP/BCP	**Error Control Mode** / **10** / **9** / **8** / **Suggested Mode** / **Char. length** CRC–CCITT preset to 1's 0 0 0 BOP 1–8 CRC–CCITT preset to 0's 0 0 1 BCP 8 Not used 0 1 0 — CRC–16 preset to 0's 0 1 1 BCP 8 VRC odd 1 0 0 BCP 5–7 VRC even 1 0 1 BCP 5–7 Not used 1 1 0 — No error control 1 1 1 BCP/BOP 5–8 ECM should be loaded by the processor during initialization or when both data paths are idle.
11	IDLE		Determines line fill character to be used if transmitter underrun occurs (TxU asserted and TERR set) and transmission of special characters for BOP/BCP.
		BOP	IDLE = 0, transmit ABORT characters during underrun and when TABORT = 1. IDLE = 1, transmit FLAG characters during underrun and when TABORT = 1.
		BCP	IDLE = 0 transmit initial SYNC characters and underrun line fill characters from theS/AR. IDLE = 1 transmit initial SYNC characters from TxDB and marks TxSO during underrun.
12	SAM	BOP	Secondary Address Mode = 1 if the MPCC is a secondary station. This facilitates automatic recognition of the received secondary station address. When transmitting, the processor must load the secondary address into TxDB. SAM = 0 inhibits the received secondary address comparison which serves to activate the receiver after the first non-FLAG character has been received.
13	SS/GA		Strip SYNC/Go Ahead. Operation depends on mode.
		BOP	SS/GA = 1 is used for loop mode only and enables GA detection. When a GA is detected as a closing character, REOM and RAB/GA will be set and the processor should terminate the repeater function. SS/GA = 0 is the normal mode which enables ABORT detection. It causes the receiver to terminate the frame upon detection of an ABORT or FLAG.
		BCP	SS/GA = 1, causes the receiver to strip SYNC's immediately following the first two SYNC's detected. SYNC's in the middle of a message will not be stripped. SS/GA = 0, presents any SYNC's after the initial two SYNC's to the processor.
14	PROTO		Determines MPCC Protocol mode
		BOP	PROTO = 0
		BCP	PROTO = 1
15	APA	BOP	All parties address. If this bit is set, the receiver data path is enabled by an address field of '11111111' as well as the normal secondary station address.

Table 7. Transmit Data/Status Register (TDSR) (R/W except TDSR15)

BIT	NAME	MODE	FUNCTION
00–07	TxDB	BOP/BCP	Transmit data buffer. Contains processor loaded characters to be serialized in TxSR and transmitted on TxSO.
08	TSOM		Transmitter start of message. Set by the processor to initiate message transmission provided TxE = 1.
		BOP	TSOM = 1 generates FLAGs. When TSOM = 0 transmission is from TxDB and FCS generation (if specified) begins. FCS, as specified by $PCSAR_{8-10}$, should be CRC–CCITT preset to 1's.
		BCP	TSOM = 1 generates SYNCs from $PCSAR_L$ or transmits from TxDB for IDLE = 0 or 1 respectively. When TSOM = 0 transmission is from TxDB and CRC generation (if specified) begins.
09	TEOM		Transmit end of message. Used to terminate a transmitted message.
		BOP	TEOM = 1 causes the FCS and the closing FLAG to be transmitted following the transmission of the data character in TxSR. FLAGs are transmitted until TEOM = 0. ABORT or GA are transmitted if TABORT or TGA are set when TEOM = 1.
		BCP	TEOM = 1 causes CRC–16 to be transmitted (if selected) followed by SYNCs from $PCSAR_L$ or TxDB (IDLE = 0 or 1). Clearing TEOM prior to the end of CRC–16 transmission (when TxBE = 1) causes TxSO to be marked following the CRC–16. TxE must be dropped before a new message can be initiated. If CRC is not selected, TEOM should not be set.
10	TABORT	BOP	Transmitter abort = 1 will cause ABORT or FLAG to be sent (IDLE = 1 or 1) after the current character is transmitted. (ABORT = 11111111)
11	TGA	BOP	Transmit go ahead (GA) instead of FLAG when TEOM = 1. This facilitates repeater termination in loop mode. (GA = 01111111)
12–14	Not Defined		
15	TERR	Read only	Transmitter error = 1 indicates the TxDB has not been loaded in time (one character time–1/2 TxC period after TxBE is asserted) to maintain continuous transmission. TxU will be asserted to inform the processor of this condition. TERR is cleared by setting TSOM. See timing diagram.
		BOP	ABORT's or FLAG's are sent as fill characters (IDLE = 0 or 1)
		BCP	SYNC's or MARK's are sent as fill characters (IDLE = 0 or 1). For IDLE = 1 the last character before underrun is not valid.

Table 8. Receiver Data/Status Register (RDSR)–(Read Only)

BIT	NAME	MODE	FUNCTION
00–07	RxDB	BOP/BCP	Receiver data buffer. Contains assembled characters from the RxSR. If VRC is specified, the parity bit is stripped.
08	RSOM	BOP	Receiver start of message = 1 when a FLAG followed by a non-FLAG has been received and the latter character matches the secondary station if SAM = 1. RxA will be asserted when RSOM = 1. RSOM resets itself after one character time and has no affect on RxSA.
09	REOM	BOP	Receiver end of message = 1 when the closing FLAG is detected and the last data character is loaded into RxDB or when an ABORT/GA character is received. REOM is cleared on reading $RDSR_H$, reset operation, or dropping of RxE.
10	RAB/GA	BOP	Received ABORT or GA character = 1 when the receiver senses an ABORT character if SS/GA = 0 or a GA character if SS/GA = 1. RAB/GA is cleared on reading $RDSR_H$, reset operation, or dropping of RxE. A received abort does not set RxDA.
11	ROR	BOP/BCP	Receiver overrun = 1 indicates the processor has not read last character in the RxDB within one character time + 1/2 RxC period after RxDA is asserted. Subsequent characters will be lost. ROR is cleared on reading $RDSR_H$, reset operation, or dropping of RxE.
12–14	ABC	BOP	Assembled bit count. Specifies the number of bits in the last received data character of a message and should be examined by the processor when REOM = 1(RxDA and RxSA asserted). ABC = 0 indicates the message was terminated (by a flag or GA) on a character boundary as specified by PCR_{8-10}. Otherwise, ABC = number of bits in the last data character. ABC is cleared when $RDSR_H$ is read, reset operation, or dropping RxE. The residual character is right justified in$RDSR_L$.
15	RERR	BOP/BCP	Receiver error indicator should be examined by the processor when REOm = 1 in BOP, or when the processor determines the last data character of the message in BCP with CRC or when RxSA is set in BCP with VRC. CRC–CCITT preset to 1's/0's as specified by $PCSAR_{8-10}$: RERR = 1 indicates FCS error (CRC ≠ F0B8 or ≠ 0) RERR = 0 indicates FCS received correctly (CRC = F0B8 or = 0) CRC–16 preset to 0's on 8-bit characters specified by $PSCAR_{8-10}$: RERR = 1 indicates CRC–16 received correctly (CRC = 0). RERR = 0 indicates CRC–16 error (CRC≠0) VRC specified by $PCSAR_{8-10}$: RERR = 1 indicates VRC error RERR = 0 indicates VRC is correct.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
T_A	Operating ambient temperature[2]	Note 4	°C
T_{STG}	Storage temperature	–65 to +150	°C
	Input or output voltages with respect to GND[3]	–0.3 to +15	V
V_{CC}	With respect to GND	–0.3 to +7	V

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2]

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage					V
V_{IL} Low				0.8	
V_{IH} High		2.0			
Output voltage					V
V_{OL} Low	I_{OL} = 1.6mA			0.4	
V_{OH} High	I_{OH} = −100µA	2.4			
I_{CC} Power supply current	V_{CC} = 5.25V, T_A = 0°C			150	mA
Leakage current					µA
I_{IL} Input	V_{IN} = 0 to 5.25V			10	
I_{OL} Output	V_{OUT} = 0 to 5.25V			10	
Capacitance					pF
C_{IN} Input	V_{IN} = 0V, f = 1MHz			20	
C_{OUT} Output	V_{OUT} = 0V, f = 1MHz			20	

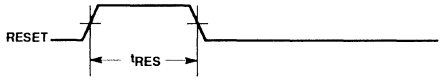
AC ELECTRICAL CHARACTERISTICS[1, 2, 3]

PARAMETER	1MHz CLOCK VERSION			2MHz CLOCK VERSION			UNIT
	Min	Typ	Max	Min	Typ	Max	
Set-up and hold time							ns
t_{ACS} Address/control set-up	50			50			
t_{ACH} Address/control hold	0			0			
t_{DS} Data bus set-up (write)	50			50			
t_{DH} Data bus hold (write)	0			0			
t_{RXS} Receiver serial data set-up	150			150			
t_{RxH} Receiver serial data hold	150			150			
Pulse width							ns
t_{RES} RESET	250			250			
t_{DBEN} DBEN	250		m[4]	250		m[4]	
Delay Time							ns
t_{DD} Data bus (read)			200			170	
t_{TxD} Transmit serial data			325			250	
t_{DBEND} DBEN to DBEN delay	200			200			
t_{DF} Data bus float time (read)			150			150	ns
f Clock (RxC, TxC) frequency			1.0			2.0	MHz
t_{CLK1} Clock high (MM = 0)	340			165			ns
t_{CLK2} Clock high (MM = 1)	490			240			
t_{CLK0} Clock low	490			240			

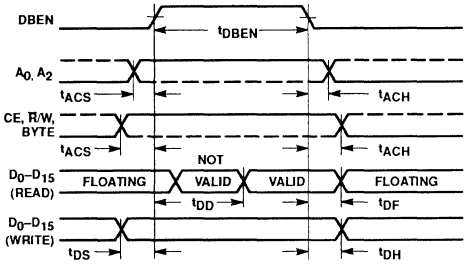
NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground. All time measurements are at 0.8V or 2.0V. Input voltage levels for testing are 0.4V and 2.4V.
3. Output load C_L = 100pF.
4. m = TxC low and applies to writing to $TDSR_H$ only.

TIMING DIAGRAMS

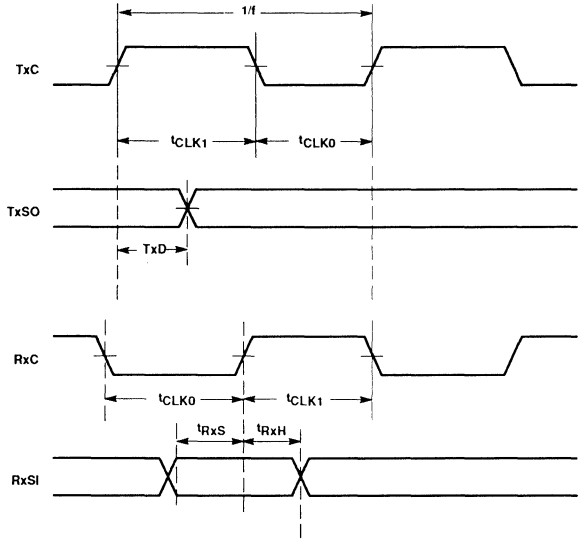
RESET



RESET AND WRITE DATA BUS

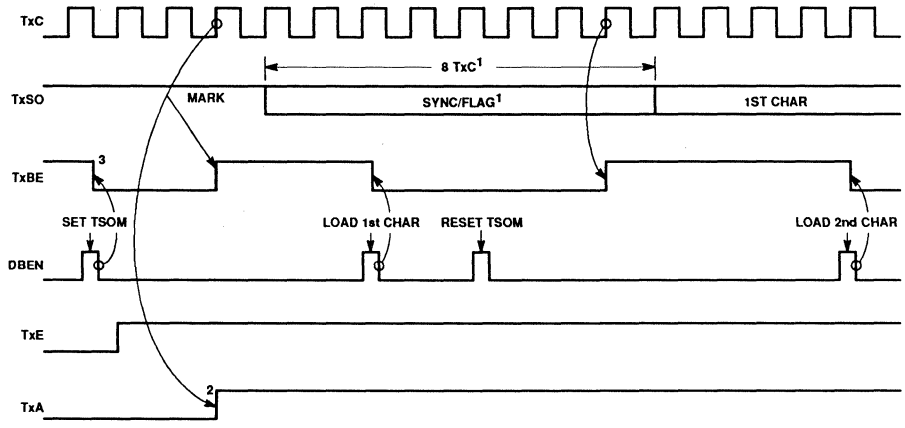


CLOCK



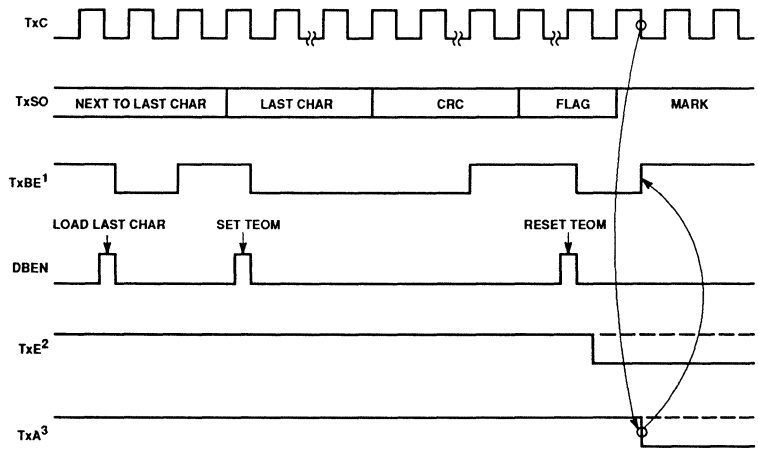
TIMING DIAGRAMS (Continued)

TRANSMIT – START OF MESSAGE



NOTES:
1. SYNC may be 5 to 8 bits and will contain parity bit as specified.
2. TxA goes high relative to TxC rising edge after TSOM has been set and TxE has been raised.
3. TxBE goes low relative to DBEN falling edge on the first write transfer into TDSR. It is reasserted 1 TxC time before the first bit of the transmitted SYNC/FLAG. TxBE then goes low relative to DBEN falling edge when writing into $TDSR_H$ and/or $TDSR_L$. It is reasserted on the rising edge of the TxC that corresponds to the transmission of the last bit of each character, except in BOP mode when the CRC is to be sent as the next character (see Transmit Timing–End of Message).

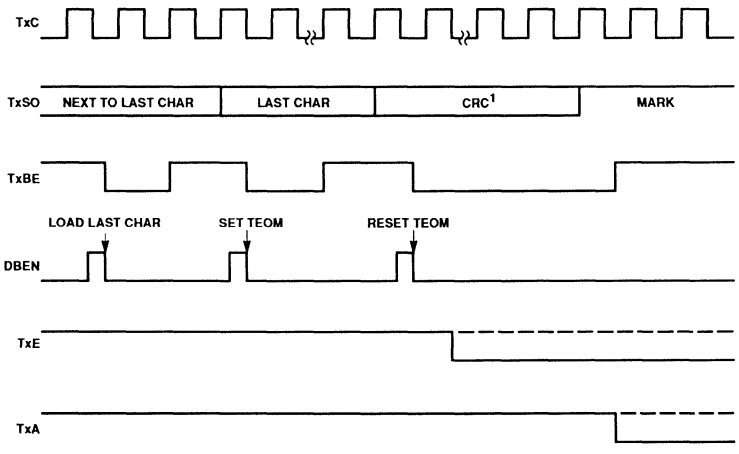
TRANSMIT – END OF BOP MESSAGE



NOTES:
1. TxBE goes low relative to the falling edge of DBEN corresponding to loading $TDSR_{H/L}$. It goes high one TxC before character transmission begins and also when TxA has been dropped.
2. TxE can be dropped before resetting TEOM if TxBE (corresponding to the closing FLAG) is high. Alternatively TxE can remain high and a new message initiated.
3. TxA goes low after TxE has been dropped and 1 1/2 TxC's after the last bit of the closing FLAG has been transmitted.

TIMING DIAGRAMS (Continued)

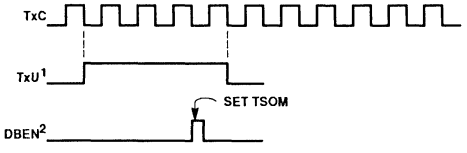
TRANSMIT TIMING – END OF BCP MESSAGE



NOTE:

1. When SCN2652 generated CRC is not required. TEOM should only be set if SYNCs are to follow the message block. In that case, TxE should be dropped in response to TxBE (which corresponds to the start of transmission of the last character). When CRC is required, TxE must be dropped before CRC transmission is complete. Otherwise, the contents of TxDB will be shifted out on TxSO. This facilitates transmission of contiguous messages.

TRANSMIT UNDERRUN

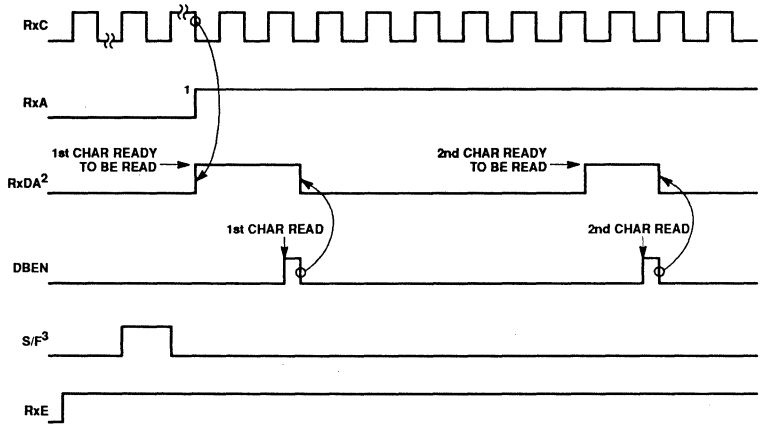


NOTES:

1. TxU goes active relative to TxC falling edge if TxBE has not been serviced after n-1/2 TxC times (where n = transmit character length). TxU is reset on the TxC falling edge following assertion of the TSOM command.
2. An underrun will occur at the next character boundary if TEOM is reset and the transmitter remains enabled, unless the TSOM command is asserted or a character is loaded into the TxDB.

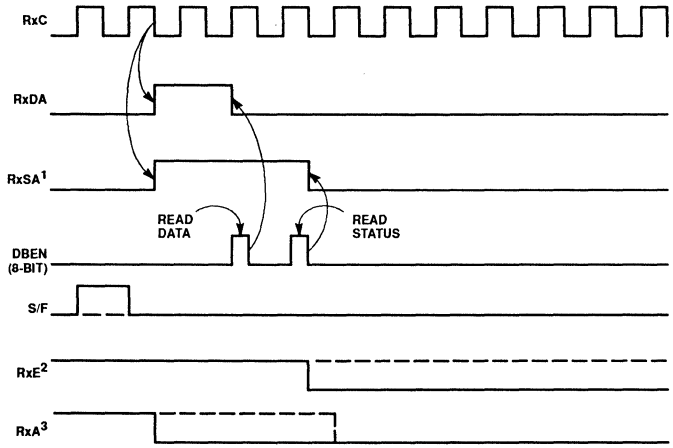
TIMING DIAGRAMS (Continued)

RECEIVE – START OF MESSAGE



NOTES:
1. RxA goes high relative to falling edge of RxC when RxE is high and: a. A data character following two SYNC's is in RxDB (BCP mode). b. Character following FLAG is in RxDB (BOP primary station mode). c. Character following FLAG is in RxDB and character matches the secondary station address or all parties address (BOP secondary station mode).
2. RxDA goes high on RxC falling edge when a character in RxDB is ready to be read. It comes up before RxSA and goes low on the falling edge of DBEN when RxDB is read.
3. S/F goes high relative to rising edge of RxC anytime a SYNC (BCP) or FLAG (BOP) is detected.

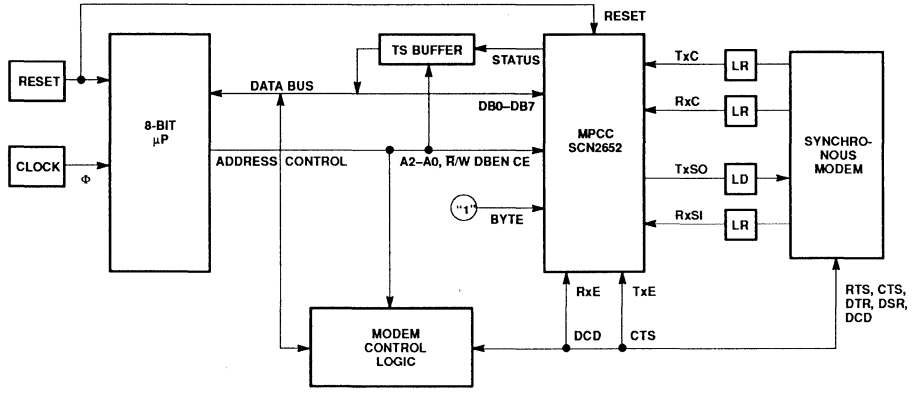
RECEIVE END OF MESSAGE



NOTES:
1. At the end of a BOP message, RxSA goes high when FLAG detection (S/F 1) forces REOm to be set. Processor should read the last data character ($RDSR_L$) and status ($RDSR_H$) which resets RxDA and RxSA respectively. For BCP end of message, RxSA may not be set and S/F = 0. The processor should read the last data character and status.
2. RxE must be dropped for BCP with non-contiguous messages. It may be left on at the end of a BOP message (see BOP Receive Operation).
3. RxA is reset relative to the falling edge of RxC after the closing FLAG of a BOP message (REOM = 1 and RxSA active.) or when RxE is dropped.

TYPICAL APPLICATIONS

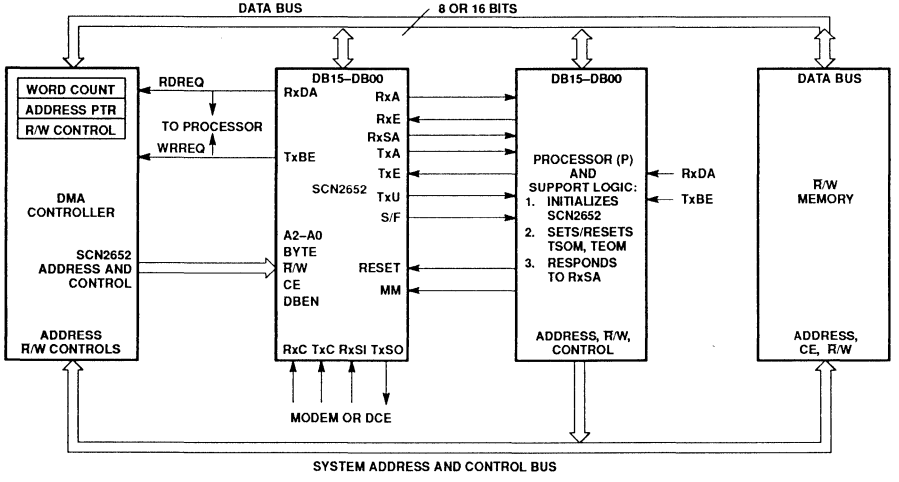
SCN2652 MPCC MICROPROCESSOR INTERFACE



NOTES:

1. Possible µP interrupt requests are: RxDA RxSA TxBE TxU
2. Other SCN2652 status signals and possible uses are S F line idle indicator, frame delimiter. RxA handshake on RxE, line turn around control. TxA handshake on TxE, line turn around control.
3. Line drivers/receivers (LD/LR) convert EIA to TTL voltages and vice-versa.
4. RTS should be dropped after the CRC (BCP) or FLAG (BOP) has been transmitted. This forces CTS low and TxE low.
5. Corresponding high and low order bits of DB must be OR tied.

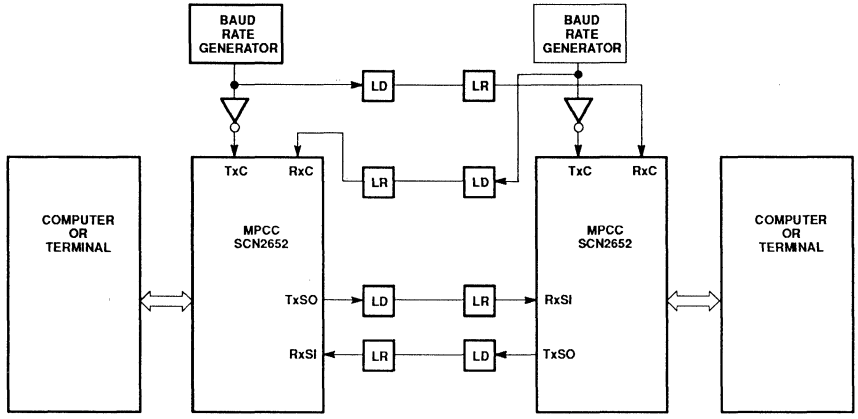
DMA/PROCESSOR INTERFACE



For non-DMA operation TxBE and RxDA are set to the processor which then loads or reads data characters as required.

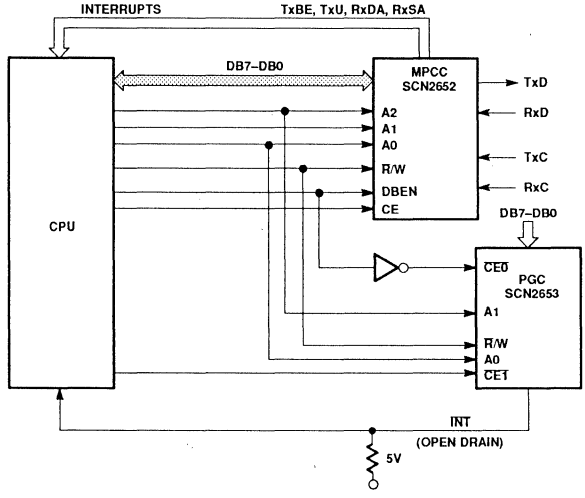
TYPICAL APPLICATIONS (Continued)

CHANNEL INTERFACE



No Modem – DC Baseband Transmission

SCN2652/SCN2653 INTERFACE TYPICAL PROTOCOLS:
BISYNC, DDCMP, SDLC, HDLC



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Data Communication Products	

SCN2661/SCN68661

Enhanced programmable communications interface (EPCI)

DESCRIPTION

The Signetics SCN2661 EPCI is a universal synchronous/asynchronous data communications controller chip that is an enhanced version of the SCN2651. It interfaces easily to all 8-bit and 16-bit microprocessors and may be used in a polled or interrupt driven system environment. The SCN2661 accepts programmed instructions from the microprocessor while supporting many serial data communications disciplines —synchronous and asynchronous — in the full- or half-duplex mode. Special support for BISYNC is provided.

The EPCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The SCN2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (A, B, C) has a different set of baud rates.

FEATURES

- Synchronous operation
  - 5- to 8-bit characters plus parity
  - Single or double SYN operation
  - Internal or external character synchronization
  - Transparent or non-transparent mode
  - Transparent mode DLE stuffing (Tx) and detection (Rx)
  - Automatic SYN or DLE-SYN insertion SYN, DLE and DLESYN stripping
  - Odd, even, or no parity
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
- Asynchronous operation
  - 5- to 8-bit characters plus parity
  - 1, 1-1/2 or 2 stop bits transmitted
  - Odd, even, or no parity
  - Parity, overrun and framing error detection
  - Line break detection and generation
  - False start bit detection
  - Automatic serial echo mode (echoplex)
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
    DC to 62.5kbps (16X clock)
    DC to 15.625kbps (64X clock)

OTHER FEATURES

- Internal or external baud rate clock
- 3 baud rate sets
- 16 internal rates for each set
- Double-buffered transmitter and receiver
- Dynamic character length switching
- Full- or half-duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short-circuit protected
- Single +5V power supply
- No system clock required

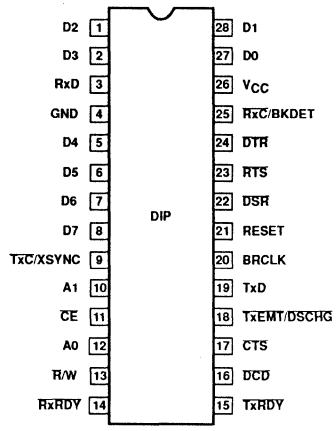
APPLICATIONS

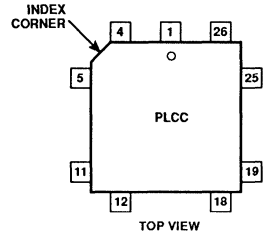
- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Computer-to-computer links
- Serial peripherals
- BISYNC adaptors

Enhanced programmable communications interface (EPCI)

SCN2661/SCN68661

PIN CONFIGURATIONS





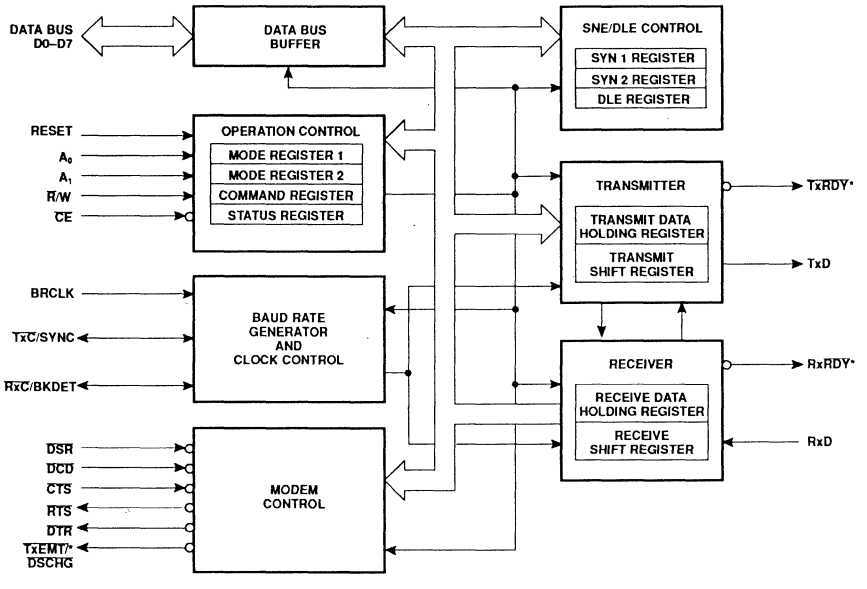
NOTE:
Pin Functions the same as 28-pin DIP.

ORDERING CODE

PACKAGES	V_{CC} = +5V ±5%		
	Commercial	Automotive	Military
	0°C to +70°C	-40°C to +85°C	-55°C to +125°C
Ceramic DIP 28-Pin 0.6" Wide	SCN2661AC1F28 SCN2661BC1F28 SCN2661CC1F28	SCN2661AA1F28 SCN2661BA1F28 SCN2661CA1F28	SCN2661AM1F28 SCN2661BM1F28 SCN2661CM1F28
Plastic DIP 28-Pin 0.6" Wide	SCN2661AC1N28 SCN2661BC1N28 SCN2661CC1N28	Contact Factory	Not Available
Plastic LCC	SCN2661AC1A28 SCN2661BC1A28 SCN2661CC1A28	Contact Factory	Not Available

Enhanced programmable communications interface (EPCI) SCN2661/SCN68661

BLOCK DIAGRAM



NOTES:
* Open–drain output pin.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	Note 4	°C
Storage temperature	-65 to +150	°C
All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum function temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Over recommended free-air operating temperature range and supply voltage range unless otherwise specified. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
Output voltage						
V_{OL}	Low	I_{OL} = 2.2mA			0.4	V
V_{OH}[4]	High	I_{OH} = -400µA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to 5.5V			10	µA
3-State output leakage current						
I_{LH}	Data bus high	V_O = 4.0V			10	µA
I_{LL}	Data bus low	V_O = 0.45V			10	µA
I_{CC}	Power supply current				150	mA

NOTES:
1. Over recommended free-air operating temperature range and supply voltage range unless otherwise specified. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All voltages measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels swing between 0.4V and 2.4V, with a transition time of $\leq$ 20ns maximum.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. $\overline{INTR}$, $\overline{TxRDY}$, $\overline{RxRDY}$ and $\overline{TxEMT/DSCHG}$ outputs are open-drain.

CAPACITANCE T_A = 25°C, V_{CC} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Capacitance						
C_{IN}	Input				20	pF
C_{OUT}	Output	f_C = 1MHz			20	pF
$C_{I/O}$	Input/Output	Unmeasured pins tied to ground			20	pF

AC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Pulse width						
t_{RES}	Reset		1000			ns
t_{CE}	Chip enable		250			ns
Setup and hold time						
t_{AS}	Address setup		10			ns
t_{AH}	Address hold		10			ns
t_{CS}	R/W control setup		10			ns
t_{CH}	R/W control hold		10			ns
t_{DS}	Data setup for write		150			ns
t_{DH}	Data hold for write		10			ns
t_{RXS}	RX data setup		300			ns
t_{RXH}	RX data hold		350			ns
t_{DD}	Data delay time for read	C_L = 150pF			200	ns
t_{DF}[7]	Data bus floating time for read	C_L = 150pF			100	ns
t_{CED}	CE to CE delay		600			ns
Input clock frequency						
f_{BRG}	Baud rate generator (2661A, B)		1.0	4.9152	4.9202	MHz
f_{BRG}	Baud rate generator (2661C)		1.0	5.0688	5.0738	MHz
$f_{R/T}$[6]	$\overline{TxC}$ or $\overline{RxC}$		dc		1.0	MHz
Clock width						
t_{BRH}[5]	Baud rate High (2661A, B)		75			ns
t_{BRH}[5]	Baud rate High (2661C)		70			ns
t_{BRL}[5]	Baud rate Low (2661A, B)		75			ns
t_{BRL}[5]	Baud rate Low (2661C)		70			ns
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ High		480			ns
$t_{R/TL}$[6]	$\overline{TxC}$ or $\overline{RxC}$ Low		480			ns
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	C_L = 150pF			650	ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[4]	C_L = 150pF		0		ns

NOTES:

1. Over recommended free-air operating temperature range and supply voltage range unless otherwise specified. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All voltages measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels swing between 0.4V and 2.4V, with a transition time of $\leq$ 20ns maximum.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. Parameter applies when internal transmitter clock is used.
5. Under test conditions of 5.0688MHz f_{BRG} (68661) and 4.9152MHz f_{BRG} (68661A, B), t_{BRH} and t_{BRL} measured at V_{IH} and V_{IL}, respectively.
6. In asynchronous local loopback mode, using 1X clock, the following parameters apply: $f_{R/T}$ = 0.83MHz max and $t_{R/TL}$ = 700ns min.
7. See AC load conditions.

BLOCK DIAGRAM

The EPCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing and protocol are presented in the EPCI programming section of this data sheet.

Timing

The EPCI contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full-duplex operation. See Table 1.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modern control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Table 1. Baud Rate Generator Characteristics

68661A (BRCLK = 4.9152MHz)

MR23–20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6144
0001	75	1.2	—	4096
0010	110	1.7598	–0.01	2793
0011	134.5	2.152	—	2284
0100	150	2.4	—	2048
0101	200	3.2	—	1536
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	—	256
1010	1800	28.7438	–0.19	171
1011	2000	31.9168	–0.26	154
1100	2400	38.4	—	128
1101	4800	76.8	—	64
1110	9600	153.6	—	32
1111	19200	307.2	—	16

68661B (BRCLK = 4.9152MHz)

MR23–20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	—	6144
0010	75	1.2	—	4096
0011	110	1.7598	–0.01	2793
0100	134.5	2.152	—	2284
0101	150	2.4	—	2048
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1200	19.2	—	256
1001	1800	28.7438	–0.19	171
1010	2000	31.9168	–0.26	154
1011	2400	38.4	—	128
1100	4800	76.8	—	64
1101	9600	153.6	—	32
1110	19200	307.2	—	16
1111	38400	614.4	—	8

68661C (BRCLK = 5.0688MHz)

MR23–20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6336
0001	75	1.2	—	4224
0010	110	1.76	—	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	—	2112
0101	300	4.8	—	1056
0110	600	9.6	—	528
0111	1200	19.2	—	264
1000	1800	28.8	—	176
1001	2000	32.081	0.253	158
1010	2400	38.4	—	132
1011	3600	57.6	—	88
1100	4800	76.8	—	66
1101	7200	115.2	—	44
1110	9600	153.6	—	33
1111	19200	316.8	3.125	16

NOTE:
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

OPERATION

The functional operation of the 68661 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the EPCI programming section of the data sheet.

After programming, the EPCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The 68661 is conditioned to receiver data when the $\overline{DCD}$ input is Low and the RxEN bit in the commands register is true. In the asynchronous mode, the receiver looks for High-to-Low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit-time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data are then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the High order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit timer interval. If a break condition is detected (RxD is Low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit SR5 set) will be transferred to the holding register. The RxD input must return to a High condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go High. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the Break Detection Timing Diagram.

When the EPCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data are shifted into the receiver shift register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization.) When synchronization has been achieved, the EPCI continues to assemble characters and transfer then to the holding register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1–SYN2, and DLE–SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxD. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Table 2. CPU-Related Signals

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
RESET	21	I	A High on this input performs a master reset on the 68661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A0, A1	12,10	I	Address lines used to select internal EPCI registers.
R/W	13	I	Read command when Low, write command when High.
CE	11	I	Chip enable command. When Low, indicates that control and data lines to the EPCI are valid and that the operation specified by the R/W, A1 and A0 inputs should be performed. When High, places the D0–D7 lines in the 3-State condition.
D0–D7	27,28,1,2,5–8	I/O	8-bit, 3-State data bus used to transfer commands, data and status between EPCI and the CPU. D0 is the least significant bit, D7 the most significant bit.
TxRDY	15	O	This output is the complement of status register bit SR0. When Low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes High when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open-drain output which can be used as an interrupt to the CPU.
RxRDY	14	O	This output is the complement of status register bit SR1. When Low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes High when the RHR is read by the CPU, and also when the receiver is disabled. It is an open-drain output which can be used as an interrupt to the CPU.
TxEMT/ DSCHG	18	O	This output is the complement of status register bit SR2. When Low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the DSR or DCD inputs has occurred. This output goes High when the status register is ready by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open-drain output which can be used as an interrupt to the CPU. See Status Register (SR2) for details.

Table 3. Device-Related Signals

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
BRCLK	20	I	Clock input to the internal baud rate generator (see Table 1). Not required if external receiver and transmitter clocks are used.
RxC/BKDET	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin.
TxC/XSYNC	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input.
RxD	3	I	Serial data input to the receiver. "Mark" is High, "space" is Low.
TxD	19	O	Serial data output from the transmitter. "Mark" is High, "Space" is Low. Held in mark condition when the transmitter is disabled.
DSR	22	I	General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a Low output on TxEMT/DSCHG when its state changes if CR2 or CR0 = 1.
DCD	16	I	Data carrier detect input. Must be Low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a Low output on TxEMT/DSCHG when its state changes if CR2 or CR0 = 1. If DCD goes High while receiving, the RxC is internally inhibited.
CTS	17	I	Clear to send input. Must be Low in order for the transmitter to operate. If it goes High during transmission, the character in the transmit shift register will be transmitted before termination.
DTR	24	O	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.
RTS	23	O	General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. See Command Register (CR5) for details.

Transmitter

The EPCI is conditioned to transmit data when the $\overline{CTS}$ input is Low and the TxEN command register bit is set. The 68661 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated. Data are transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (High) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous Low (BREAK) condition by setting the send break command bit (CR3) High.

In the synchronous mode, when the 68661 is initially conditioned to transmit, the TxD output remains High and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the EPCI unless the CPU fails to send a new character to the EPCI by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the EPCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1–SYN2 doublets, or DLE–SYN1 doubles, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the transmit data holding register. If the send DLE bit in the commands register is true, the DLE character is automatically transmitted prior to transmission of the message character in the THR.

EPCI PROGRAMMING

Prior to initiating data communications, the 68661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The EPCI can be reconfigured at any time during program execution. A flowchart of the initialization process appears in Figure 1.

The internal registers of the EPCI are accessed by applying specific signals to the $\overline{CE}$, R/$\overline{W}$, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1 = 0, A0 = 1, and R/$\overline{W}$ = 1. The first operation loads the SYN1 register. The next loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses mode register 1, and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a read command register operation, but are unaffected by any other read or write operation.

The 68661 register formats are summarized in Tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the EPCI, while the command register controls the operation within this basic framework. The EPCI indicates its status in the status register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates mode register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7 or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14. In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 2X baud rate is programmed, 1.5 stop bits defaults to 1 stop bits on transmit.) In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1–SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE–SYN1 is used for character fill and SYN detect, but the normal synchronization sequence is used to establish character sync. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also, DLE stripping and DLE detect (with MR14 = 0) are enabled.

The bits in the mode register affecting character assembly and disassembly (MR12–MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore in synchronous mode, changes should be made only in half-duplex mode (RxEN = 1 or TxEN = 1, but not both simultaneously = 1). In asynchronous mode, character changes should be made when RxEN and TxEN = 0 or when TxEN = 1 and the transmitter is marking in half-duplex mode (RxEN = 0).

To effect assembly/disassembly of the next received/transmitted character, MR12 – 15 must be changed within n bit times of the active going state of $\overline{RxRDY/TxRDY}$. Transparent and non-transparent mode changes (MR16) must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active. (n – smaller of the new and old character lengths.)

Table 4. 68661 Register Addressing

$\overline{CE}$	A_1	A_0	R/$\overline{W}$	FUNCTION
1	X	X	X	3-State data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode register 1/2
0	1	0	1	Write mode register 1/2
0	1	1	0	Read command register
0	1	1	1	Write command register

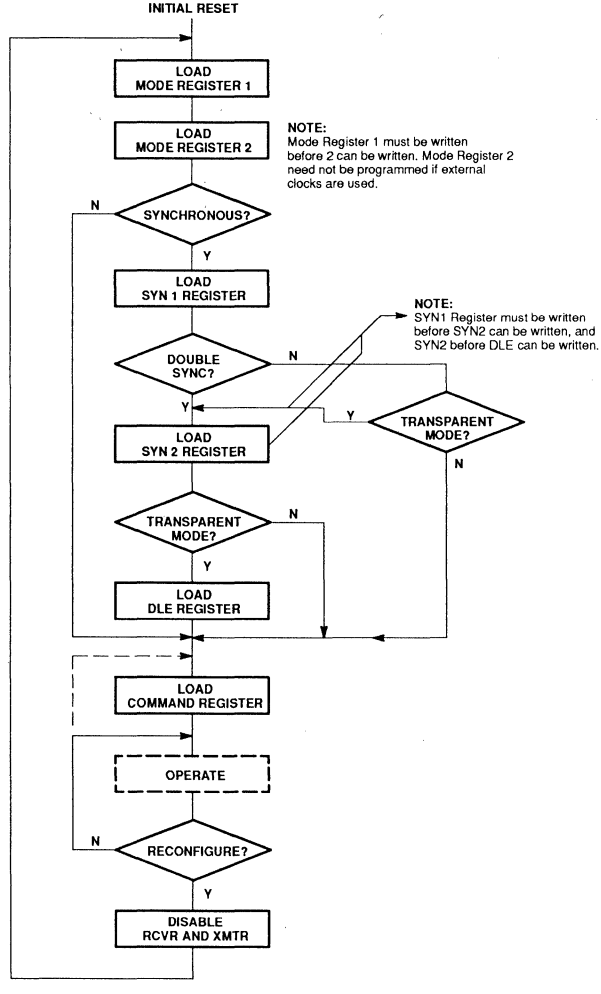


Figure 1. 68661 Initialization Flowchart

Table 5. Mode Register 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Sync/Async		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
Async: Stop bit length 00 = invalid 01 = 1 stop bit 10 = 1 1/2 stop bits 11 = 2 stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits		00 = Synchronous 1X rate 01 = Asynchronous 1X rate 10 = Asynchronous 16X rate 11 = Asynchronous 64X rate	
Sync: Number of SYN char 0 = Double SYN 1 = Single SYN	**Sync: Transparency control** 0 = Normal 1 = Transparent						

NOTE: Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

Table 6. Mode Register 2 (MR2)

MR27 – MR24										MR23 – MR20
	TxC	RxC	Pin 9	Pin 25		TxC	RxC	Pin 9	Pin 25	Mode	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	XSYNC*	RXC/TxC	sync	
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	async	
0010	I	E	1X	RxC	1010	I	E	XSYNC*	RxC	sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	async	See baud rates in Table 1.
0100	E	E	TxC	RxC	1100	E	E	XSYNC*	RxC/TxC	sync	
0101	E	I	TxC	16X	1101	E	I	TXC	BKDET	async	
0110	I	E	16X	RxC	1110	I	E	XSYNC*	RxC	sync	
0111	I	I	16X	16X	1111	I	I	16X	BKDET	async	

NOTES:
* When pin 9 is programmed as XSYNC input, SYN1, SYN1–SYN2, and DLE–SYN1 detection is disabled.
E = External clock
I = Internal clock (BRG)
1X and 16X are clock outputs.

Table 7. Command Register (CR)

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error	Sync/Async	Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = Normal operation 01 = Async: Automatic Echo mode Sync: SYN and/or DLE stripping mode 10 = Local loopback 11 = Remote loopback		0 = Force $\overline{RTS}$ Output High one clock time after TxSR serialization 1 = Force $\overline{RTS}$ output Low	0 = Normal 1 = Reset error flags in status reg. (FE,OE,PE/ DLE detect.)	**Async:** Force Break 0 = Normal 1 = Force break **Sync** **Send DLE** 0 = Normal 1 = Send DLE	0 = Disable 1 = Enable Not applicable in	0 = Force $\overline{DTR}$ output High 1 = Force $\overline{DTR}$ output Low	0 = Disable 1 = Enable

Table 8. Status Register (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ input is High 1 = $\overline{DSR}$ input is Low	0 = $\overline{DCD}$ input is High 1 = $\overline{DCD}$ input is Low	**Async:** 0 = Normal 1 = Framing error **Sync:** 0 = Normal 1 = SYN detected	0 = Normal 1 = Overrun error	**Async:** 0 = Normal 1 = Parity error **Sync:** 0 = Normal 1 = Parity error or DLE received	0 = Normal 1 = Change in $\overline{DSR}$ or $\overline{DCD}$, or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register empty

Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each EPCI version (–1,–2,–3). Versions 1 and 2 specify a 4.9152MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688MHz input which is identical to the Signetics 2651. MR23 – 20 are don't cares if external clocks are selected (MR25 – MR24 = 0). The individual rates are given in Table 1.

MR24 – MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to Table 6.

Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0–to–1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go High (inactive). If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (High) while $\overline{TxRDY}$ and $\overline{TxEMT}$ will go High (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. A 0–to–1 transition of CR2 will initiate start bit search (async) or hunt mode (sync).

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output Low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go High for at least one bit time before beginning transmission of the next character in the transmit data holding register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the transmit data holding register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE-non-DLE character sequences.

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared; this is a one time command. There is no internal latch for this bit.

When CR5 (RTS) is set, the $\overline{RTS}$ pin is forced Low. A 1–to–0 transition of CR5 will cause $\overline{RTS}$ to go High (inactive) one TxC time after the last serial bit has been transmitted. If a 1–to–0 transition of CR5 occurs while data is being transmitted, $\overline{RTS}$ will remain Low (active) until both the THR and the transmit shift register are empty and then go High (inactive) one TxC time later.

The EPCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7 – CR6 = 00 is the normal mode, with the transmitter and receive operating independently in accordance with the mode and status register instructions.

In asynchronous mode, CR7 – CR6 = 01 places the EPCI in the automatic echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed.

The TxD output will go High until the next valid start is detected. The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ **output = 1.**
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7 – CR6 = 01 places the EPCI in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17 – MR16 = 10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding register (RHR).
2. In the non-transparent, double SYN mode (MR17 – MR16 = 00), character in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred the RHR.
3. In transparent mode (MR16 = 1), character in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE–DLE pair is stripped.

Note that automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In local loopback mode (CR7 – CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held High.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 (DTR) and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the EPCI.

The second diagnostic mode is the remote loopback mode (CR7 – CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receiver clock.
3. No data are sent to the local CPU, but he error status conditions (PE, FE) are set.
4. The $\overline{\text{RxRDY}}$, $\overline{\text{TxRDY}}$, and $\overline{\text{TxEMT}}$/$\overline{\text{DSCHG}}$ outputs are held High.
5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the status register (as shown in Table 8) indicates receiver and transmitter conditions and modem/data set status.

SR0 is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0–, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit register. If set equal to 1, it indicates that the holding register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is Low. In the automatic echo and remote loopback modes, the output is held High.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is Low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs (when CR2 or CR0 = 1) or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG conditions is enabled when TxEN = 1 or RxEN = 1. It is cleared when the status register is read by the CPU. If the status register is read twice and SR2 – 1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. When SR2 is set, the $\overline{\text{TxEMT}}$/$\overline{\text{DSCHG}}$ output is Low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching DLE register was received and the present character is neither SYN2 or DLE. This bit is cleared when the next character following the above sequence is loaded into RHR, when the receiver is disabled, or by a reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not ready the CPU at the time of new received character was transferred into it. This bit is cleared when the receiver is disabled or by the reset error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by a stop bit; i.e., only the first stop bit is checked. If RHR = 0 when SR5 = 1, a break condition is present. In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1 – SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN or SYN1 – SYN2) and, after synchronization has been achieved, when a DLE–SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, or when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs, respectively. A Low input sets its corresponding status bit, and a High input clears it.

Table 9. 68661 EPCI vs 2651 PCI

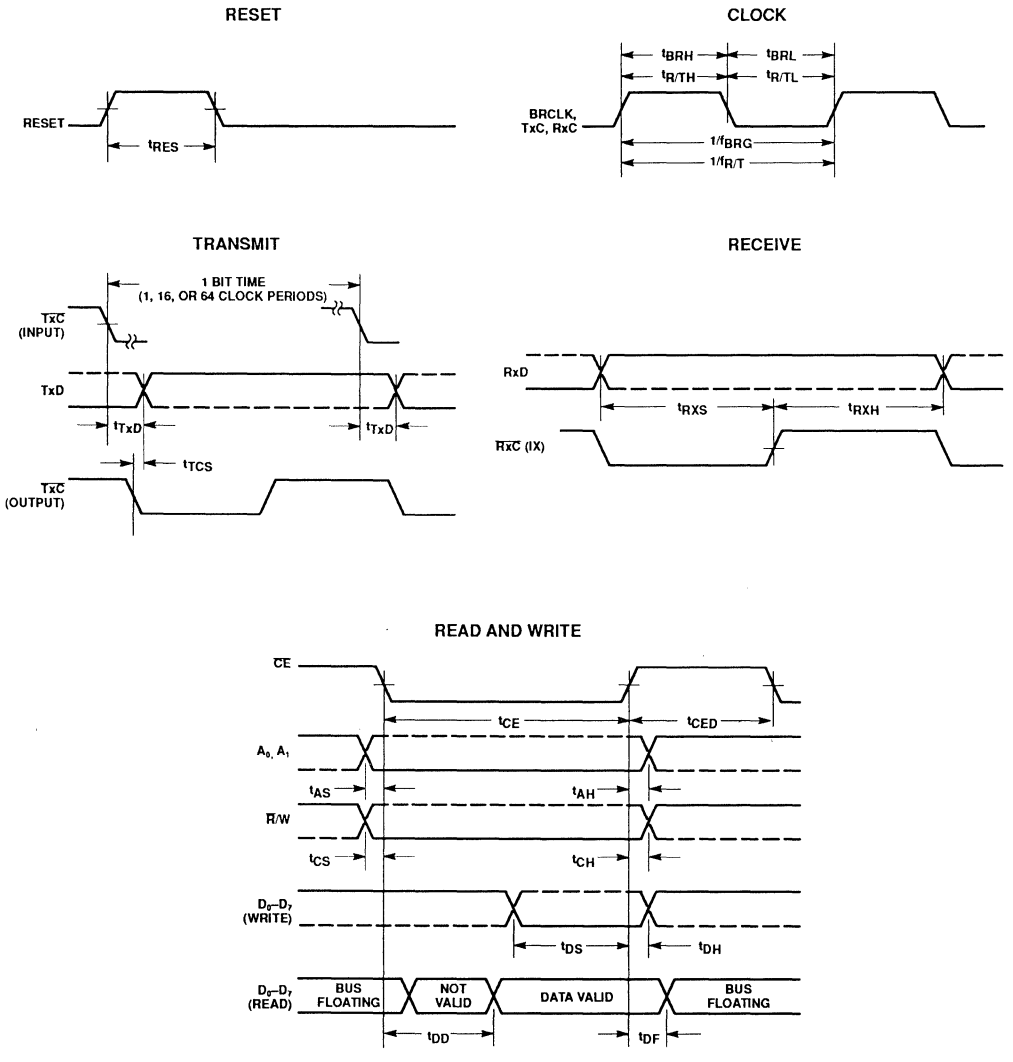
FEATURE	EPCI	PCI
1. MR2 BIT 6, 7	Control pins 9, 25	Not used
2. DLE detect – SR3	SR3 = 0 for DLE–DLE, DLE – SYN1	SR3 = 1 for DLE–DLE, DLE – SYN1
3. Reset of SR3, DLE detect	Second character after DLE, or receiver disable, or CR4 = 1	Receiver disable, or CR4 = 1
4. Send DLE – CR3	One time command	Reset via CR3 on next $\overline{\text{TxRDY}}$
5. DLE stuffing in transparent mode	Automatic DLE stuffing when DLE is loaded except if CR3 = 1	None
6. SYN1 stripping in double sync non-transparent mode	All SYN1	First SYN1 of pair
7. Baud rate versions	Three	One
8. Terminate ASYNC transmission (drop RTS)	Reset CR5 in response to $\overline{\text{TxEMT}}$ changing from 1 to 0	Reset CR0 when $\overline{\text{TxEMT}}$ goes from 1 to 0. Then reset CR5 when $\overline{\text{TxEMT}}$ goes from 1 to 0
9. Break detect	Pin 25*	FE and null character
10. Stop bit searched	One	Two
11. External jam sync	Pin 9**	No
12. Data bus timing	Improved over 2651	—
13. Data bus drivers	Sink 2.2mA Source 400µA	Sink 1.6mA Source 100µA

NOTES:
* Internal BRG used for RxC.
** Internal BRG used for TxC.

AC LOAD CONDITIONS

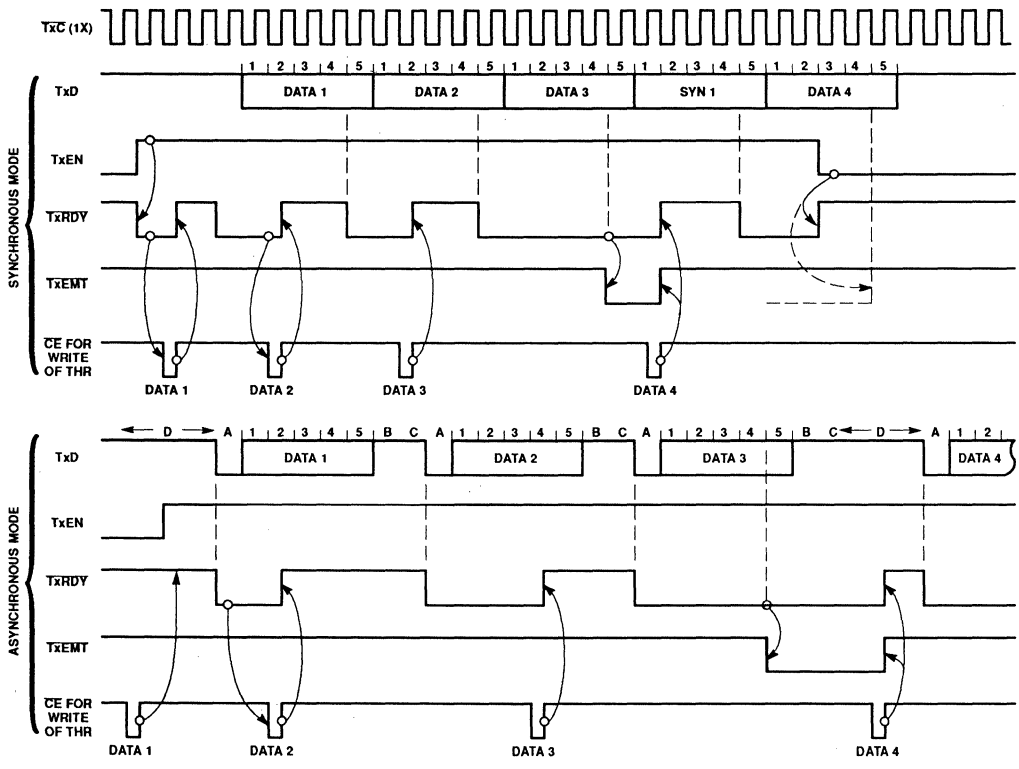
NOTES:
Open-drain outputs.
C_L = Load capacitance includes JIG and probe capacitance.

TIMING DIAGRAMS



TIMING DIAGRAMS (Continued)

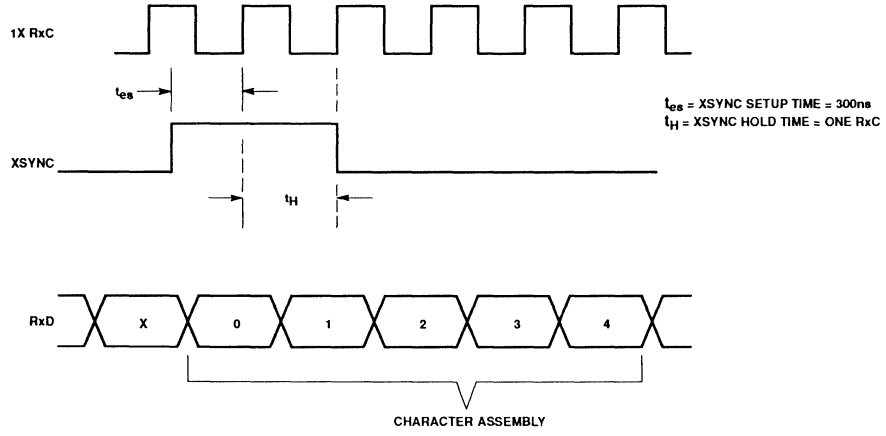
TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



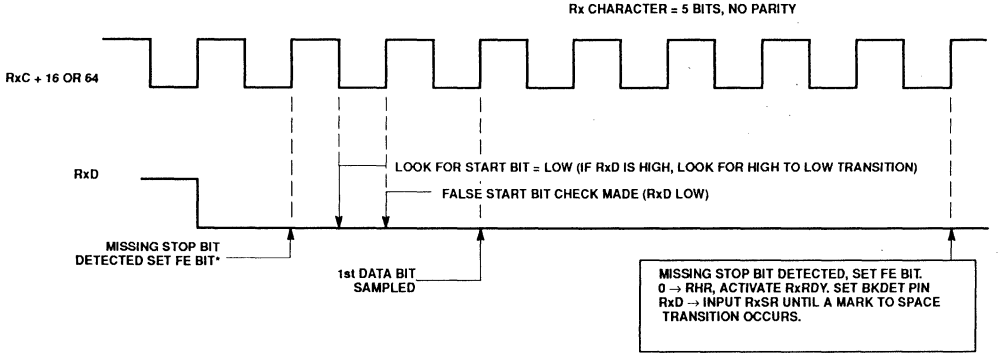
NOTES:
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

TIMING DIAGRAMS (Continued)

EXTERNAL SYNCHRONIZATION WITH XSYNC



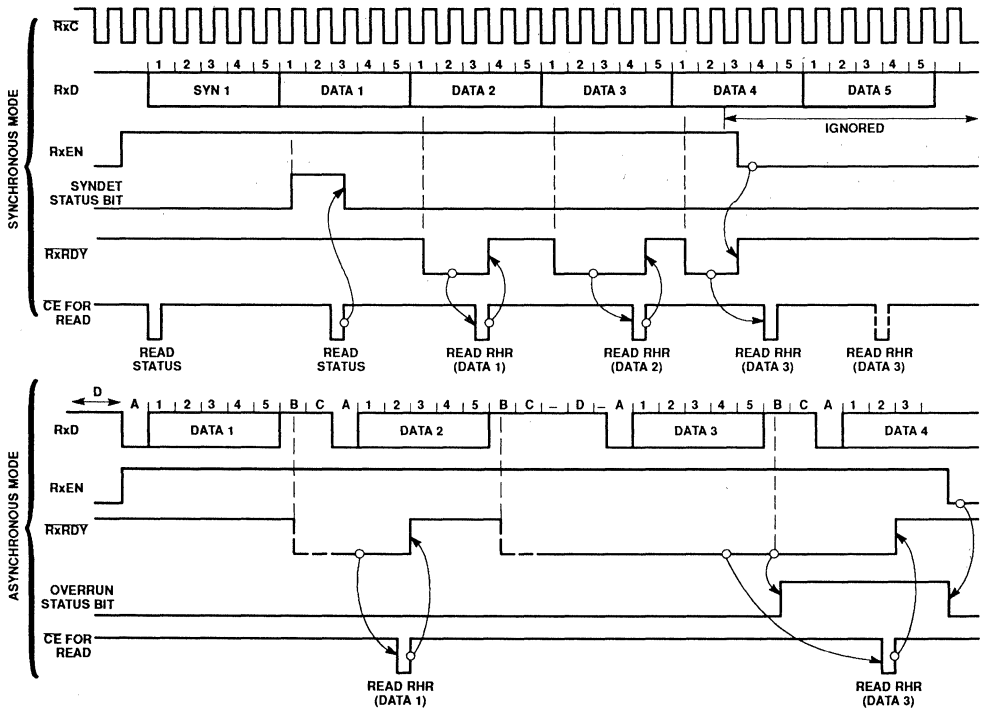
BREAK DETECTION TIMING



NOTE:
* If the stop bit is present, the start bit search will commence immediately.

TIMING DIAGRAMS (Continued)

RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

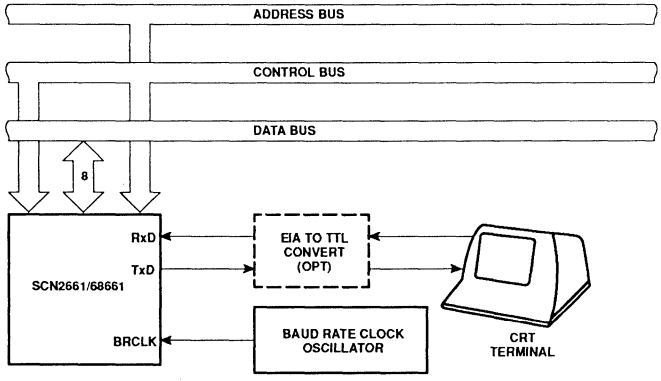


NOTES:

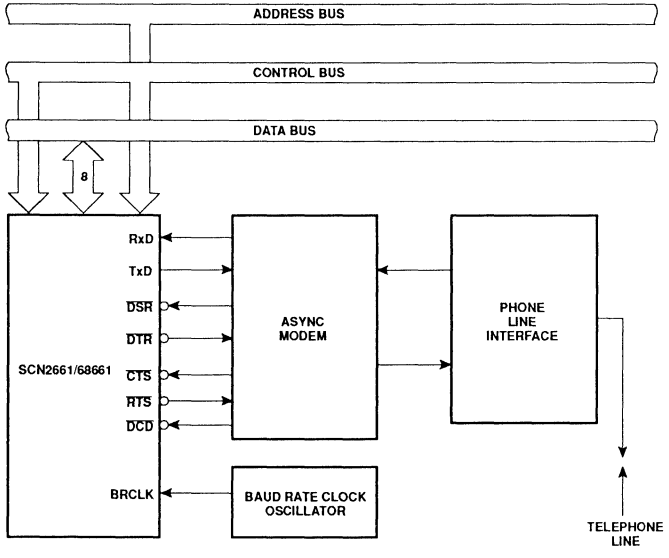
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
Only one stop bit is detected

TYPICAL APPLICATIONS

ASYNCHRONOUS INTERFACE TO CRT TERMINAL

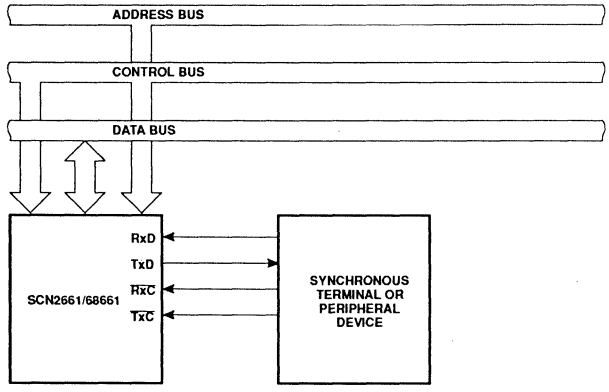


ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

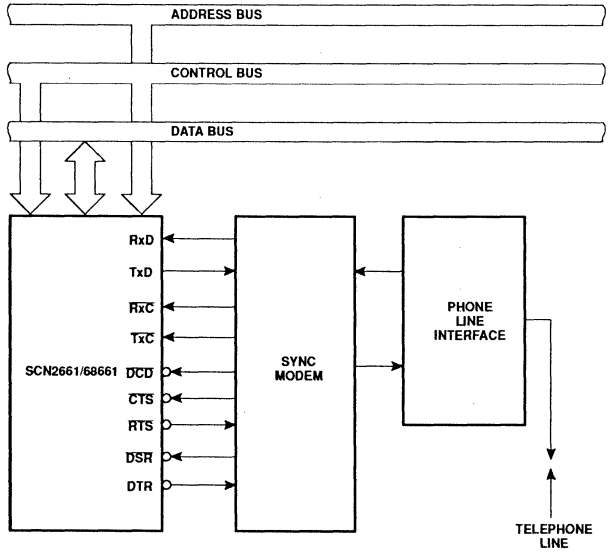


TYPICAL APPLICATIONS (Continued)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



Philips Components–Signetics

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Data Communication Products	

SCN2681

Dual asynchronous receiver/transmitter (DUART)

DESCRIPTION

The Signetics SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

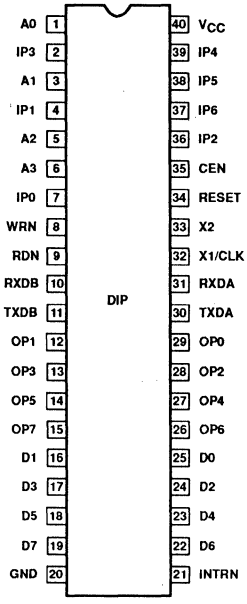
Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

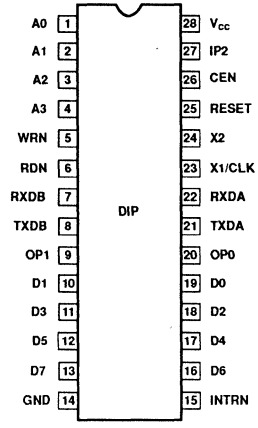
FEATURES

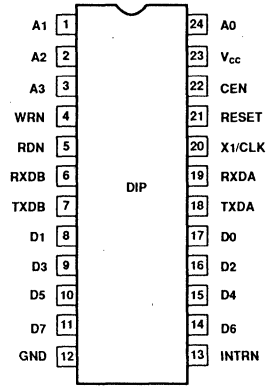
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable timer/counter
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer:
  1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available
- DIP and PLCC packages

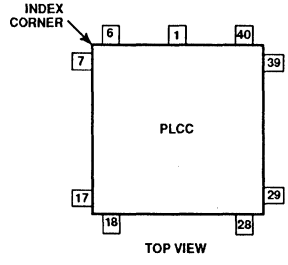
Dual asynchronous receiver/transmitter (DUART) SCN2681

PIN CONFIGURATIONS









PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

Also provided on the SCN2681 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SCN2681 is available in three package versions: 40-pin and 28–pin, both 0.6" wide DIPs; a compact 24-pin 0.4" wide DIP; and a 44-pin PLCC.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE					
	V_{CC} = +5V ±5%, T_A = 0°C to +70°C				V_{CC} = +5V ±10%, T_A = -40°C to +85°C	
	24-Pin[1]	28-Pin[2]	40-Pin[2]	44-Pin	40-Pin[2]	44-Pin
Ceramic DIP	Not available	SCN2681AC1F28	SCN2681AC1F40	Not available	SCN2681AE1F40	Not available
Plastic DIP	SCN2681AC1N24	SCN2681AC1N28	SCN2681AC1N40	Not available	SCN2681AE1N40	Not available
Plastic LCC	Not available	Not available	Not available	SCN2681AC1A44	Not available	SC2681AE1A44

NOTES:
1. 400mil-wide DIP
2. 600mil-wide DIP

PIN DESCRIPTION

SYMBOL	APPLICABLE			TYPE	NAME AND FUNCTION
	40/44	28	24		
D0–D7	X	X	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	X	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	X	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state.
INTRN	X	X	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	X	X		I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
RxDA	X	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	X	X	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	X	X	O	**Channel B Transmitter Serial Data Output:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP0	X	X		O	**Output 0:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	X		O	**Output 1:** General purpose output or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP2	X			O	**Output 2:** General purpose output or open-drain, active-Low counter/timer output, or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP3	X			O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X			O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output.
OP5	X			O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output.
OP6	X			O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output.
OP7	X			O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYB output.
IP0	X			I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	X			I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	X	X		I	**Input 2:** General purpose input or counter/timer external clock input.
IP3	X			I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.

PIN DESCRIPTION (Continued)

SYMBOL	APPLICABLE			TYPE	NAME AND FUNCTION
	40/44	28	24		
IP4	X			I	**Input 4:** General purpose input or Channel B receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X			I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X			I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X		I	**Power Supply:** +5V supply input.
GND	X	X		I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	See Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[5]		2			V
V_{IH}	Input high voltage (except X1/CLK)[4]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		4			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except o.d. outputs)[5]	I_{OH} = -400µA	2.4			V
V_{OH}	Output high voltage (except o.d. outputs)[4]	I_{OH} = -400µA	2.9			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	-10		10	µA
I_{LL}	Data bus 3-stage leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 grounded	-4	-2	0	mA
		V_{IN} = 0, X2 floated	-3	-1.5	0	mA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 grounded	-1	0.2	1	mA
		V_{IN} = V_{CC}, X2 floated	0	3.5	10	mA
I_{X2L}	X2 low input current	V_{IN} = 0, X1/CLK floated	-100	-30	0	µA
I_{X2H}	X2 high input current	V_{IN} = V_{CC}, X1/CLK floated	0	+30	100	µA
I_{OC}	Open-collector output leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{OCC}	Power supply current					
	0°C to +70°C version				150	mA
	-40°C to +85°C version				175	mA

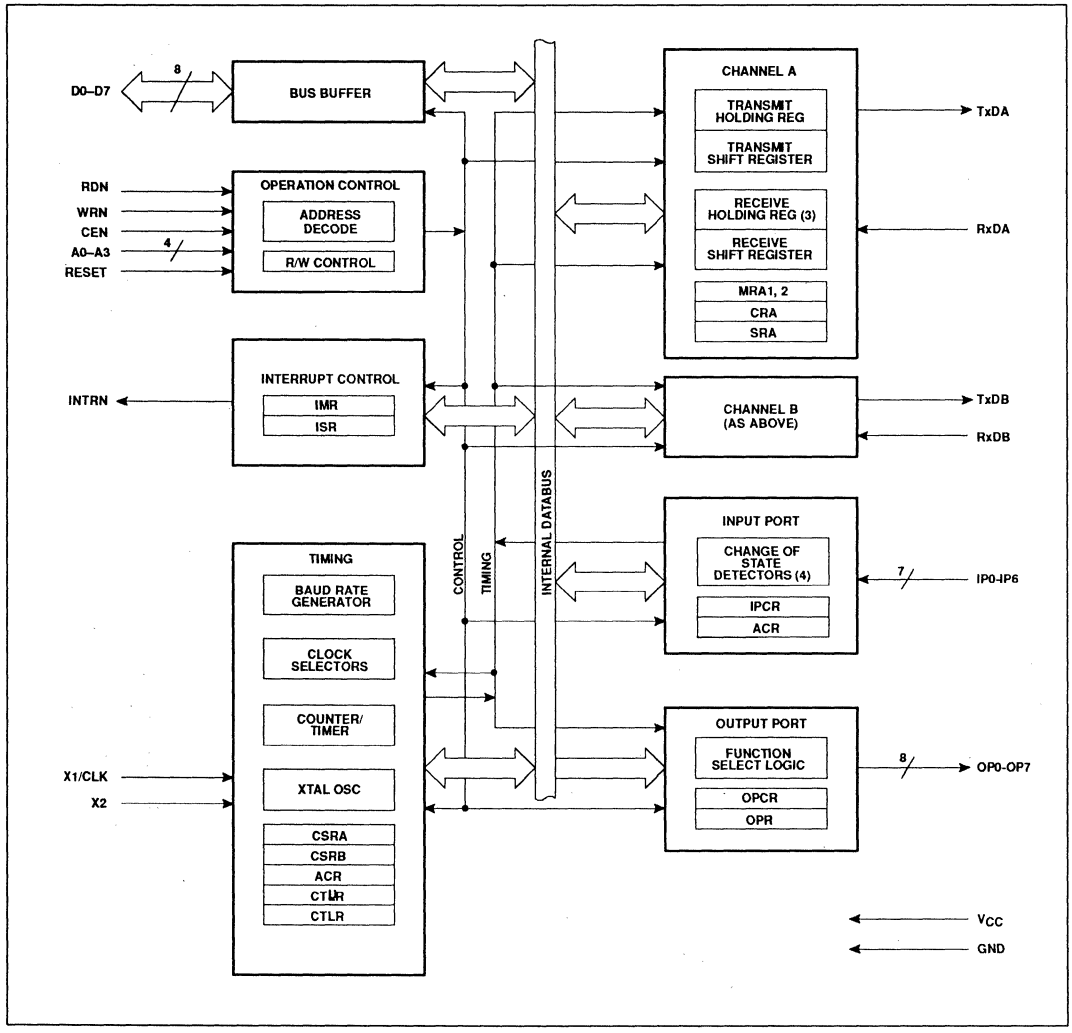
NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. T_A < 0°C
5. $T_A \geq$ 0°C

AC CHARACTERISTICS T_A = -55°C to +125°C[1], V_{CC} = +5.0V ± 10%[2, 3, 4, 5]

SYMBOL	PARAMETER	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Reset Timing (Figure 1)					
t_{RES}	RESET pulse width	1.0			µs
Bus Timing (Figure 2)[6]					
t_{AS}	A0-A3 setup time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 hold time from RDN, WRN High	0			ns
t_{CS}	CEN setup time to RDN, WRN Low	0			ns
t_{CH}	CEN hold time from RDN, WRN High	0			ns
t_{RW}	WRN, RDN pulse width	225			ns
t_{DD}	Data valid after RDN Low			175	ns
t_{DF}	Data bus floating after RDN High			100	ns
t_{DS}	Data setup time before WRN High	100			ns
t_{DH}	Data hold time after WRN High	20			ns
t_{RWD}	High time between READs and/or WRITE[7, 8]	200			ns
Port Timing (Figure 3)[6]					
t_{PS}	Port input setup time before RDN Low	0			ns
t_{PH}	Port input hold time after RDN High	0			ns
t_{PD}	Port output valid after WRN High			400	ns
Interrupt Timing (Figure 4)					
t_{IR}	INTRN (or OP3-OP7 when used as interrupts) negated from:				
	Read RHR (RxRDY/FFULL interrupt)			300	ns
	Write THR (TxRDY interrupt)			300	ns
	Reset command (delta break interrupt)			300	ns
	Stop C/T command (counter interrupt)			300	ns
	Read IPCR (input port change interrupt)			300	ns
	Write IMR (clear of interrupt mask bit)			300	ns
Clock Timing (Figure 5)					
t_{CLK}	X1/CLK High or Low time	100			ns
f_{CLK}	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	CTCLK (IP2) High or Low time	100			ns
f_{CTC}	CTCLK (IP2) frequency	0		4.0	MHz
t_{RX}[9]	RxC High or Low time	220			ns
f_{RX}[9]	RxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
t_{TX}[9]	TxC High or Low time	220			ns
f_{TX}[9]	TxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
Transmitter Timing (Figure 6)					
t_{TXD}[9]	TxD output delay from TxC Low			350	ns
t_{TCS}[9]	Output delay from TxC Low to TxD data output	0		150	ns
Receiver Timing (Figure 7)					
t_{RXS}[9]	RxD data setup time to RxC High	240			ns
t_{RXH}[9]	RxD data hold time from RxC High	200			ns

NOTES:
1. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
2. Parameters are valid over specified temperature range.
3. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of ≤ 20ns. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
4. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
5. Test condition for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 21.7kΩ to V_{CC}.
6. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
7. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
8. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
9. This parameter is not applicable to the 28-pin device.

BLOCK DIAGRAM



BLOCK DIAGRAM

The SCN2681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the block diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, both X1 and X2 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4k baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCN2681 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address D16. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs lasting longer than 25 – 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

Output Port

The 8-bit multipurpose port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address E16 with the accompanying data specifying the bits to be set (1 = set, 0 = no change).

Likewise, a bit is reset by a write at address F16 with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SCN2681 is conditioned to transmit data when the transmitter is enabled through the command register. The SCN2681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter

can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCN2681 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7 1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, overrun error and received break state (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Table 1. SCN2681 Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	*Reserved*	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	*Reserved*	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	*Reserved*	*Reserved*
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3| – Channel A Parity Mode Select

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] + 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	RxINT SELECT	ERROR MODE	PARITY MODE	PARITY TYPE	BITS PER CHARACTER
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3 BIT 2 BIT 1 BIT 0			
	CHANNEL MODE	TxRTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
	RECEIVER CLOCK SELECT	TRANSMITTER CLOCK SELECT
CSRA CSRB	See Text	See Text

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		MISCELLANEOUS COMMANDS	DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
CRA CRB	Not used – must be 0	See Text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	11 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP 3 INT	DELTA IP 2 INT	DELTA IP 1 INT	DELTA IP 0 INT
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP 3	DELTA IP 2	DELTA IP 1	DELTA IP 0	IP 3	IP 2	IP 1	IP 0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been retransmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OPO) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Verify the message is sent by waiting until the transmit ready status (TxRDY) is asserted. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes Low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of .563 TO 1 AND .563 to 2 bits. In increments of 0.625 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1.0625 to 2 stop bits can be programmed in increments of .0625 bit.

The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled) in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode registers 1 and 2 are identical to the bit definitions for MRA and MR2A except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A receiver as follows:

CSRA[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4k	19.2k
1101	Timer	Timer
1110	IP4–16X	IP4–16X
1111	IP4–1X	IP4–1X

The receiver clock is always a 16X clock except for CSRA[7] = 1111.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as per CSR[7:4] except as follows:

CSRA[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3–16X	IP3–16X
0111	IP3–1X	IP3–1X

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as per CSRA[7:4] except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP6–16X	IP6–16X
0111	IP6–1X	IP6–1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as per CSRA[7:4] except as follows:

CSRB[3:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5–16X	IP5–16X
0111	IP5–1X	IP5–1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[6:4] – Channel A Miscellaneous Command
The encoded value of this field may be used to specify a single command as follows:

CRA[6:4]	COMMAND
000	No command.
001	Reset MR pointer. Causes the Channel A MR pointer to point to MR1.

010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.

100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel B transmitter interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an Open-Collector output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1:	50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2:	75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 3.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
this field selects the operating mode of the counter/timer and its clock source as shown in Table 4.

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Current State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU read the RHR. IF after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is 0002_{16}. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the CT generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR.

If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = 1111). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

On power up and after reset, the timer/counter runs in timer mode and can only be restarted. Because it cannot be shut off or stopped, and runs continuously in timer mode, it is recommended that at initialization, the output port (OP3) should be masked off through the OPCR[3:2] = 00 until the T/C is programmed to the desired operational state.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a counter command. Upon reaching terminal count (0000_{16}), the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU.

It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

Table 3. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

NOTE: Duty cycle of 16x clock is 50% ± 1%.

Table 4. ACR 6:4 Field Definition

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or external clock (x1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (x1/CLK)
111	Timer	Crystal or external clock (x1/CLK) divided by 16

TIMING DIAGRAMS

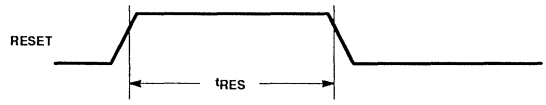


Figure 1. Reset Timing

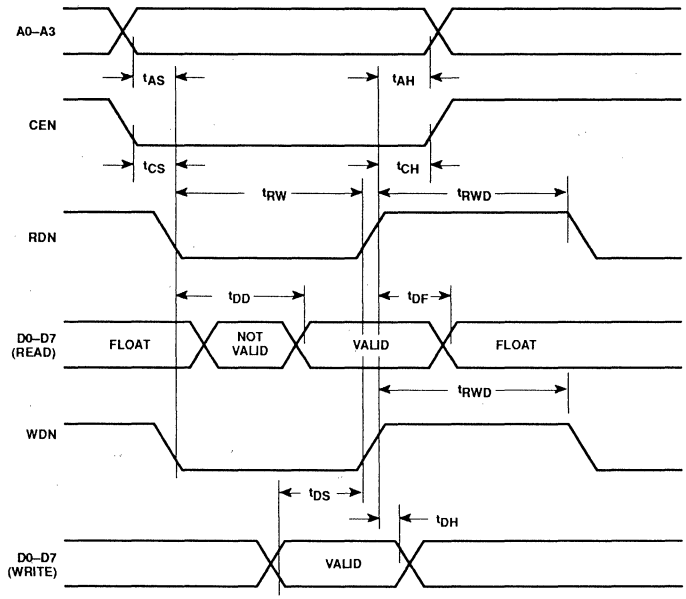


Figure 2. Bus Timing

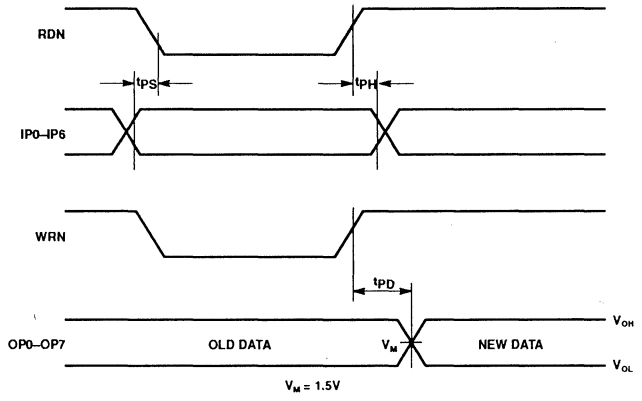
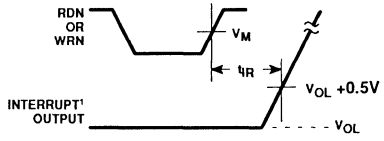


Figure 3. Port Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from themidpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing

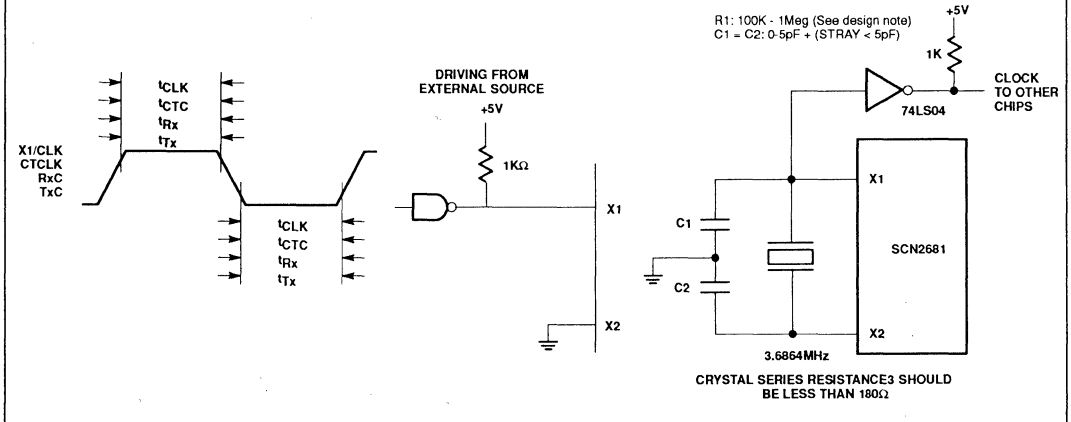


Figure 5. Clock Timing

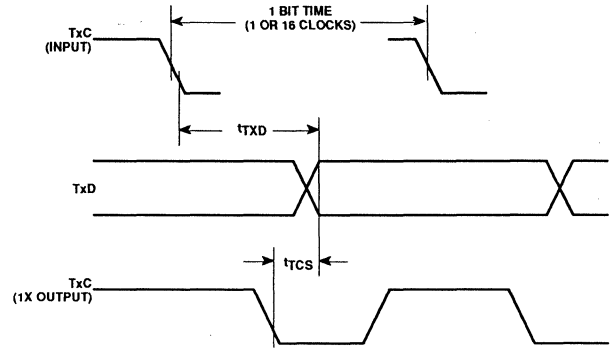


Figure 6. Transmit

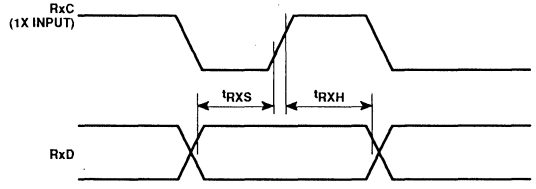
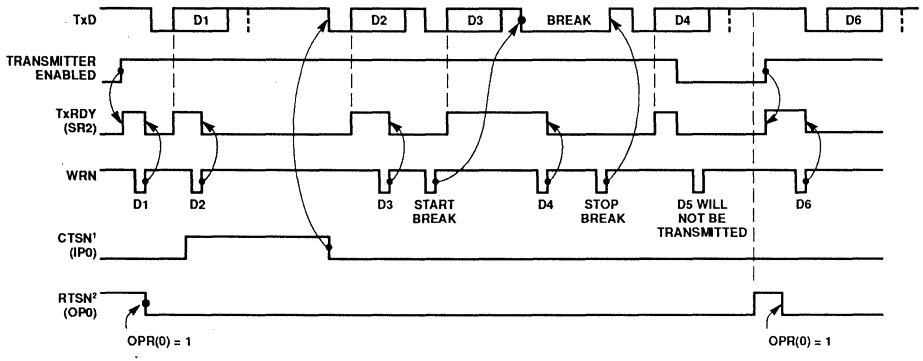
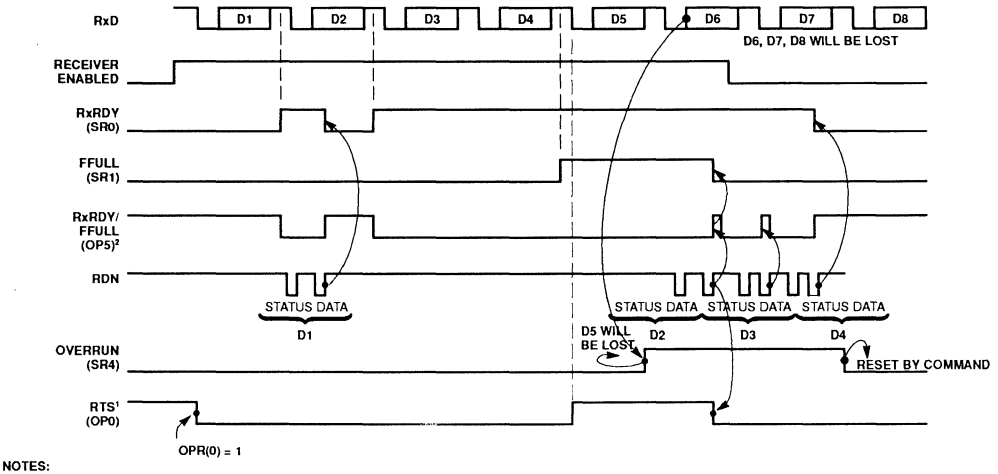


Figure 7. Receive



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR(6) = 0.

Figure 9. Receiver Timing

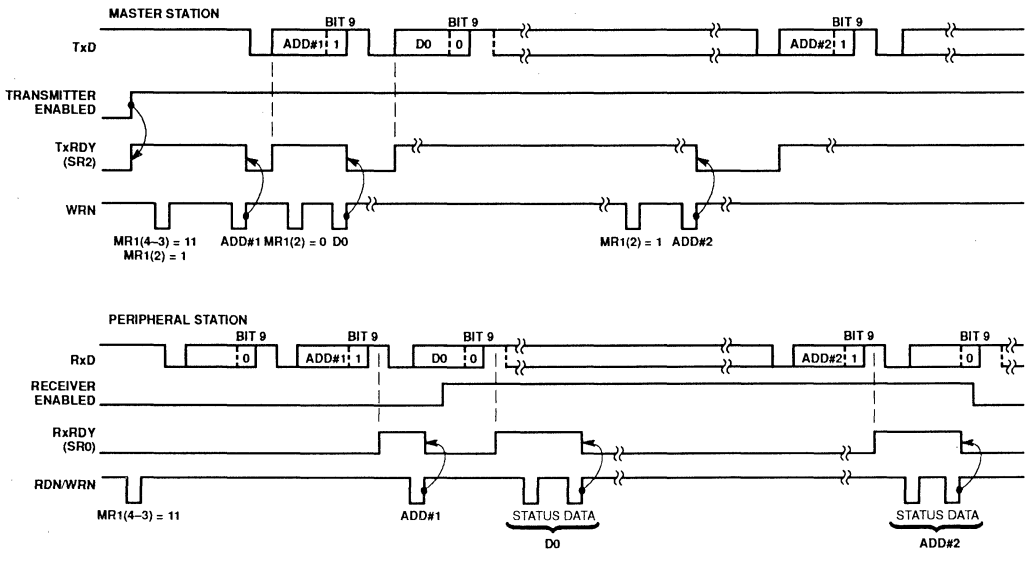


Figure 10. Wake-Up Mode

Philips Components–Signetics

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Status	Product Specification
Data Communication Products	

SCN2681T

Dual asynchronous receiver/transmitter (DUART)

DESCRIPTION

The Signetics SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. The SCN2681T features a faster bus cycle time than the standard SCN2681. The quick bus cycle eliminates or reduces the need for wait states with fast CPUs and permits high throughput in I/O intensive systems. Higher external clock rates may be used with the transmitter, receiver and counter timer which in turn provide greater versatility in baud rate generation. The SCN2681T interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCN2681T are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

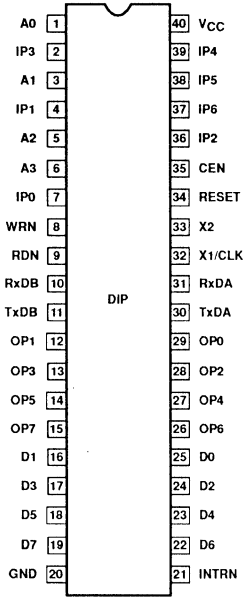
For a complete functional description and programming information for the SCN2681T, refer to the SCN2681 product specification.

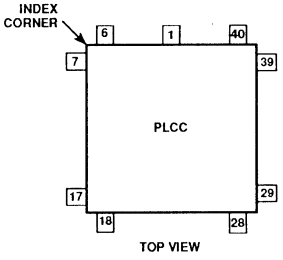
FEATURES

- Fast bus cycle times reduce or eliminate CPU wait states
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X – 1MB/sec transmitter and receiver; 16X – 500kB/sec receiver and 250kB/sec transmitter
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available

Dual asynchronous receiver/transmitter (DUART) SCN2681T

PIN CONFIGURATIONS



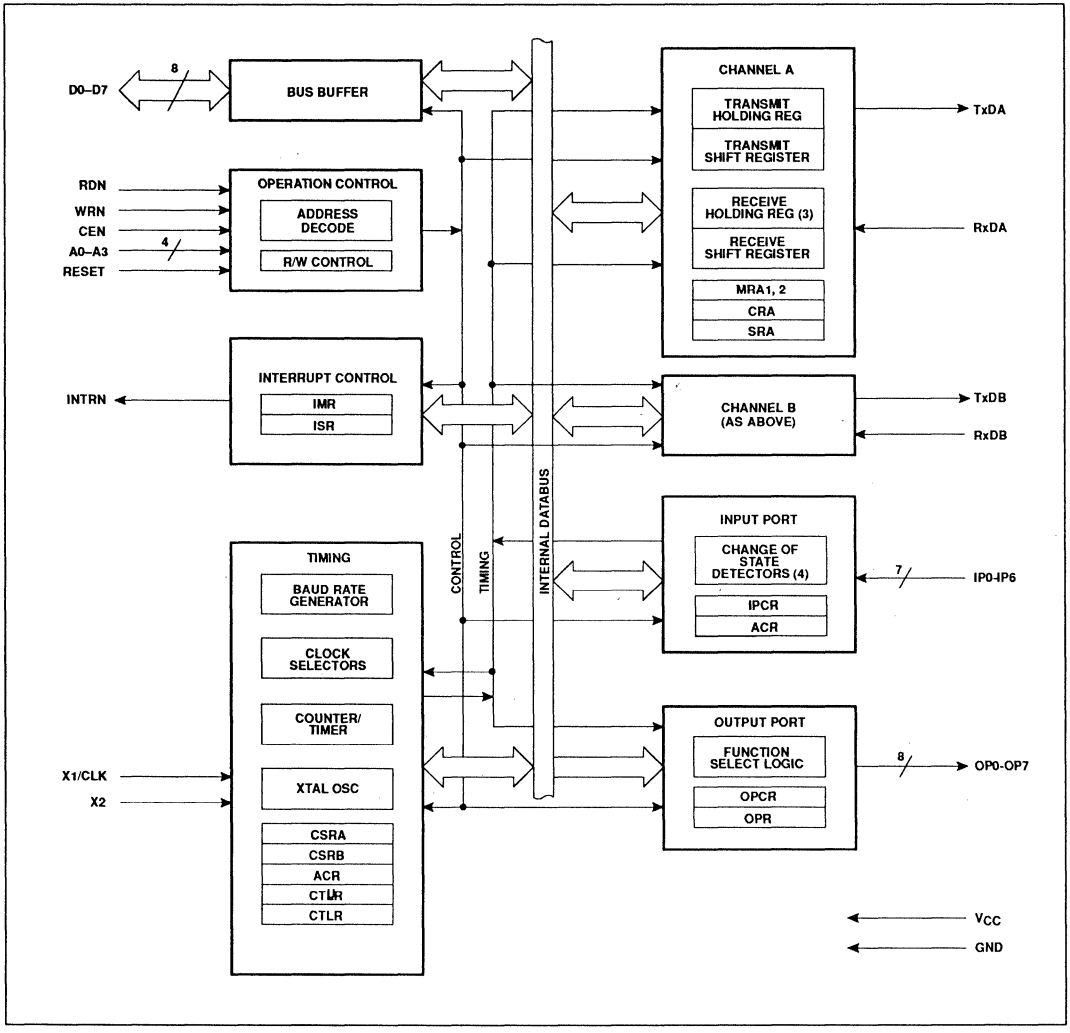


PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0°C to +70°C
40-Pin Plastic DIP (600mil-wide DIP)	SCN2681TC1N40A
44-Pin Plastic LCC	SCN2681TC1A44A

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
D0–D7	I/O	**Data Bus:** Bidirectional three-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	**Chip Enable:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN, and A0–A3 inputs. When CEN is high, the DUART places the D0–D7 lines in the three-state condition.
WRN	I	**Write Strobe:** When low and CEN is also low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	I	**Read Strobe:** When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	I	**Reset:** A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state.
INTRN	O	**Interrupt Request:** Active-low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	I	**Crystal 2:** Connection for other side of crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). If X1/CLK is driven from an external source, this pin should be grounded.
RxDA	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
RxDB	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
TxDA	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
TxDB	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
OP0	O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active-low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active-low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	O	**Output 3:** General purpose output, or open-drain, active-low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	O	**Output 4:** General purpose output, or channel A open-drain, active-low, RxRDYA/FFULLA output.
OP5	O	**Output 5:** General purpose output, or channel B open-drain, active-low, RxRDYB/FFULLB output.
OP6	O	**Output 6:** General purpose output, or channel A open-drain, active-low, TxRDYA output.
OP7	O	**Output 7:** General purpose output, or channel B open-drain, active-low TxRDYB output.
IP0	I	**Input 0:** General purpose input, or channel A clear to send active-low input (CTSAN).
IP1	I	**Input 1:** General purpose input, or channel B clear to send active-low input (CTSBN).
IP2	I	**Input 2:** General purpose input, or counter/timer external clock input.
IP3	I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.

PIN DESCRIPTION (Continued)

MNEMONIC	TYPE	NAME AND FUNCTION
IP5	I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	I	**Input 6:** General purpose input, or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	I	**Power Supply:** +5V supply input.
GND	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All voltages with respect to GND[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)		2.0			V
V_{IH}	Input high voltage (X1/CLK)		3.5			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except o.c. outputs)[4]	I_{OH} = -400µA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	-10		10	µA
I_{LL}	Data bus 3-state leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 grounded	-4	-2	0	mA
		V_{IN} = 0, X2 floated	-3	-1.5	0	mA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 = grounded	-1	0.2	1	mA
		V_{IN} = V_{CC}, X2 floated	0	3.5	10	mA
I_{X2L}	X2 low input current	V_{IN} = 0, X1/CLK floated	-100	-30	0	µA
I_{X2H}	X2 high input current	V_{IN} = V_{CC}, X1/CLK floated	0	+30	100	µA
I_{OC}	Open-collector output leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{CC}	Power supply current[5]					
	0°C to +70°C version				150	mA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4]

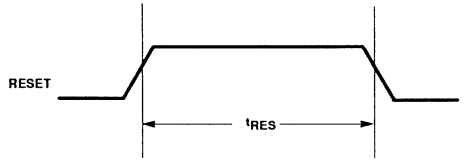


Figure 1. Reset Timing

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RES}	Reset pulse width	1.0		µs

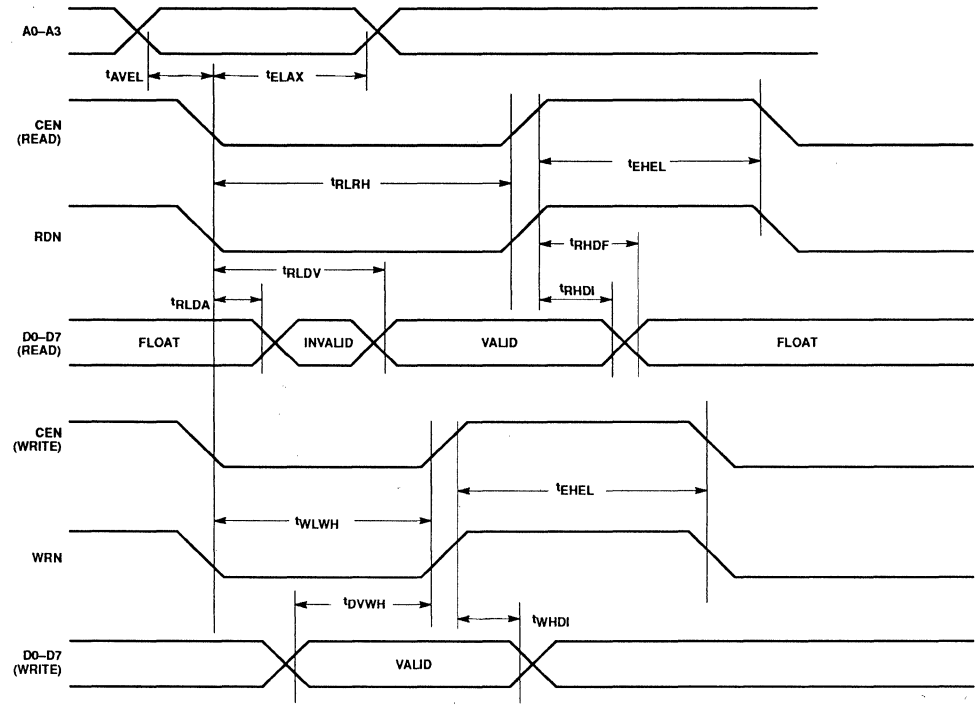


Figure 2. Bus Timing

SYMBOL	PARAMETER[1]	LIMITS Min	LIMITS Max	UNIT
t_{AVEL}	A0–A3 setup to RDN and CEN, or WRN and CEN low	0		ns
t_{ELAX}	RDN and CEN, or WRN and CEN low to A0–A7 invalid	100		ns
t_{RLRH}	RDN and CEN low to RDN or CEN high	120		ns
t_{EHEL}	CEN high to CEN low[2, 3]	110		ns
t_{RLDA}	CEN and RDN low to data outputs active	15		ns
t_{RLDV}	CEN and RDN low to data valid		100	ns
t_{RHDI}	CEN or RDN high to data invalid	10		ns
t_{RHDF}	CEN or RDN high to data outputs floating		65	ns
t_{WLWH}	WRN and CEN low to WRN or CEN high	75		ns
t_{DVWH}	Data input valid to WRN or CEN high	35		ns
t_{WHDI}	WRN or CEN high to data invalid	15		ns

NOTES:

1. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
2. If CEN is used as the 'strobing' input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{EHEL} to guarantee that any status register changes are valid. As a consequence, this minimum time must be met for the RDN input even if the CEN is used as the strobing signal for bus operations.
3. Consecutive write operations to the same command register require at least three rising edges of the X1 clock between writes.

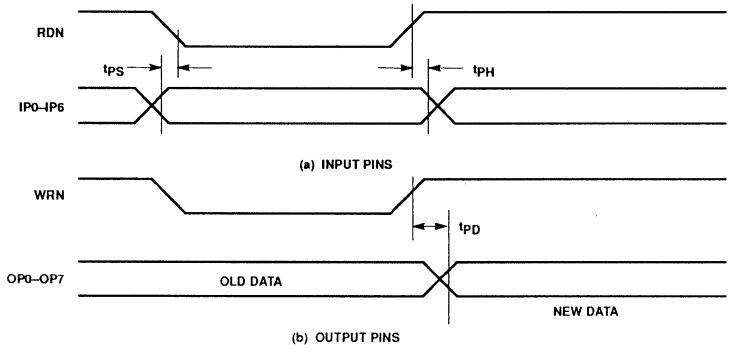
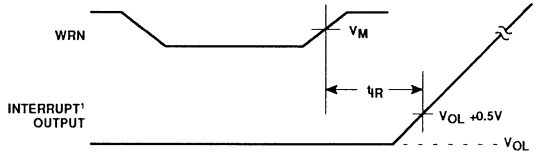


Figure 3. Port Timing

SYMBOL	PARAMETER[1]	LIMITS Min	LIMITS Max	UNIT
t_{PS}	Port input setup time before RDN low	0		ns
t_{PH}	Port input hold time after RDN high	0		ns
t_{PD}	Port output valid after WRN high		200	ns

NOTE:
1. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing

SYMBOL	PARAMETER	LIMITS Min	LIMITS Max	UNIT
t_{IR}	INTRN (or OP3–OP7 when used as interrupts) negated from:			
	Read RHR (RxRDY/FFULL interrupt)		200	ns
	Write THR (TxRDY i nterrupt)		200	ns
	Reset command (delta break interrupt)		200	ns
	Stop C/T command (counter interrupt)		200	ns
	Read IPCR (input port change interrupt)		200	ns
	Write IMR (clear of interrupt mask bit)		200	ns

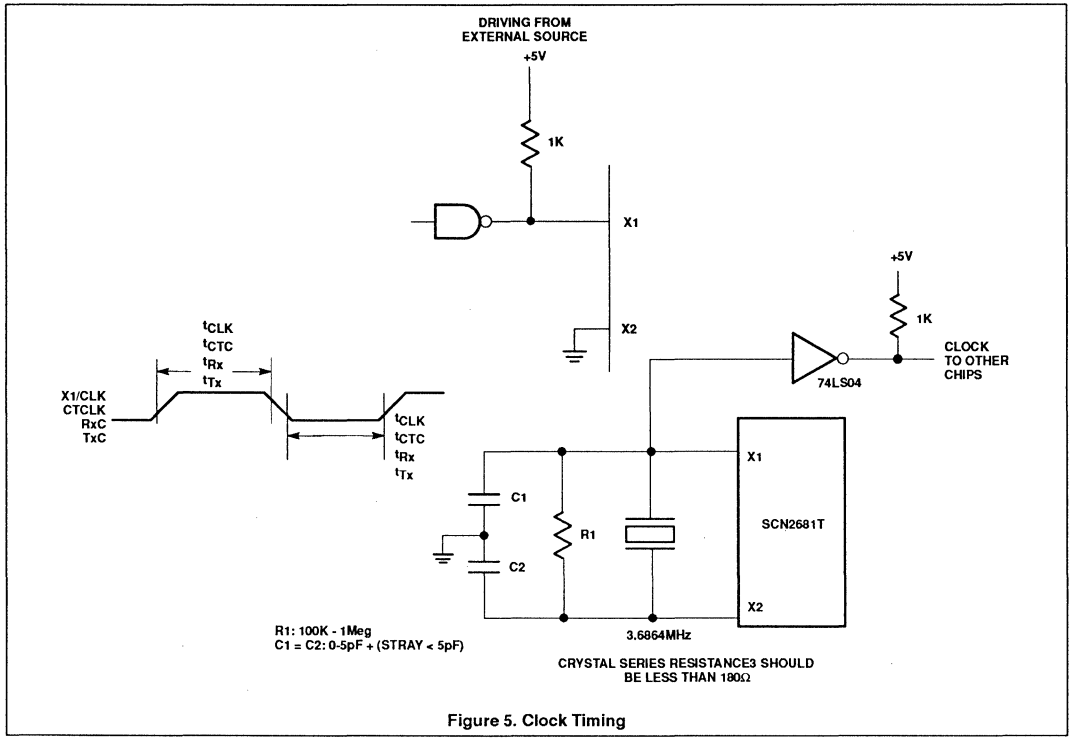


Figure 5. Clock Timing

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{CLK}	X1/CLK high or low time	90			ns
f_{CLK}	X1/CLK frequency	2	3.686	4	MHz
t_{CTC}	CTCLK (IP2) high or low time	55	4		ns
f_{CTC}	CTCLK (IP2) frequency[1]	0		8	MHz
t_{RX}	RxC high or low time	55			ns
f_{RX}	RxC frequency (16X)[1]	0		8	MHz
t_{TX}	(1X)[1]	0		1	MHz
f_{TX}	TxC high or low time	110			ns
	TxC frequency (16X)[1]	0		4	MHz
	(1X)[1]	0		1	MHz

NOTE:
1. Minimum frequencies are not tested but are guaranteed by design.

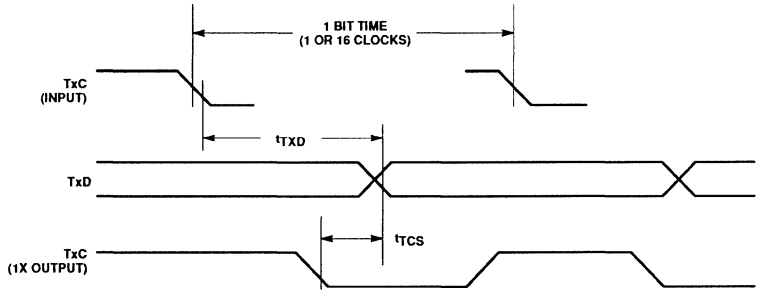


Figure 6. Transmit

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{TXD}	TxD output delay from TxC low		300	ns
t_{TCS}	Output delay from TxC low to TxD data output	0	100	ns

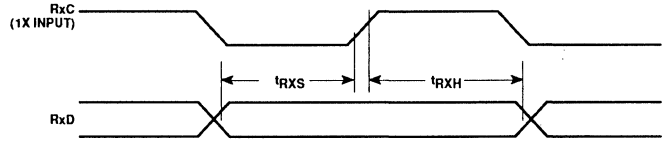
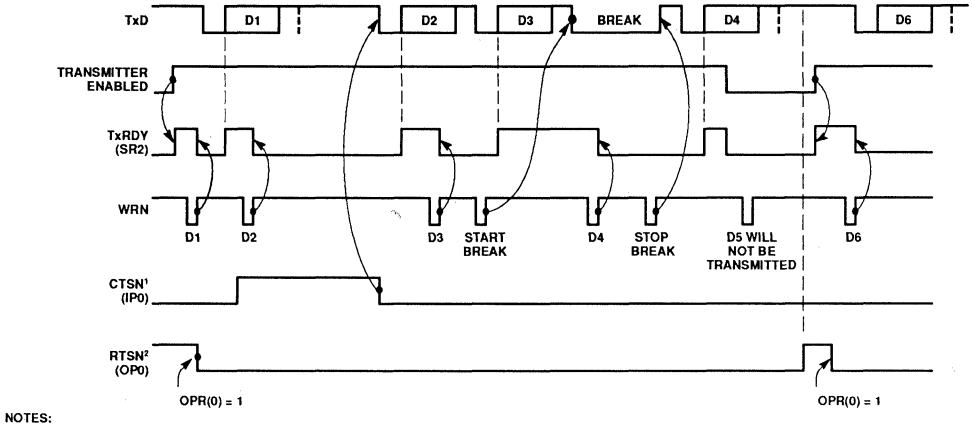


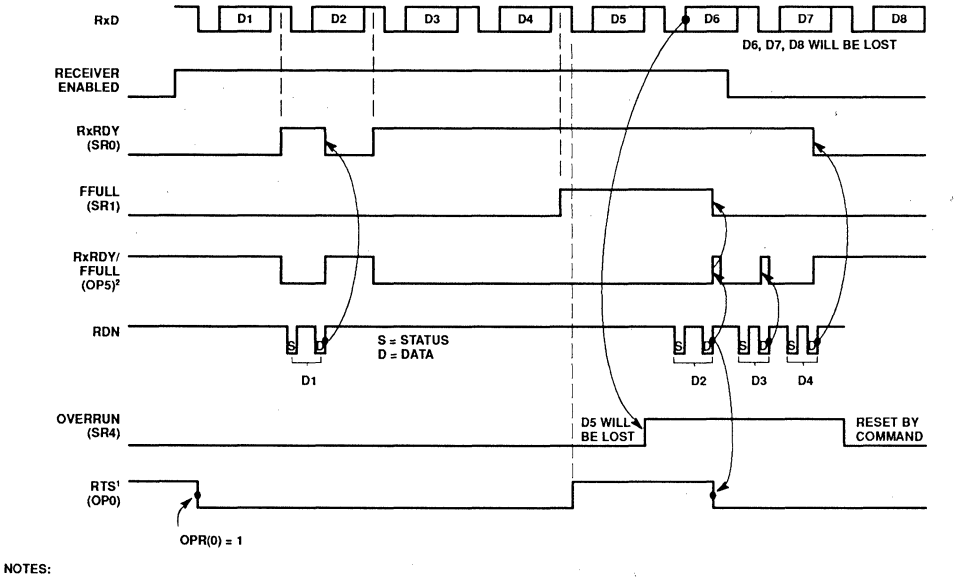
Figure 7. Receive

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RXS}	RxD data setup time to RxC high	200		ns
t_{RXH}	RxD data hold time from RxC high	25		ns



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR1(6) = 0.

Figure 9. Receiver Timing

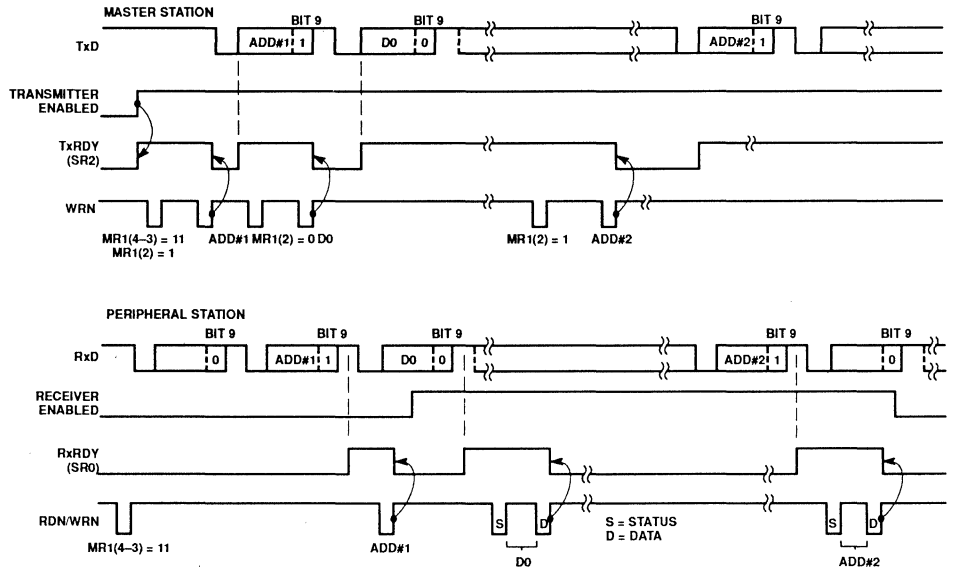


Figure 10. Wake-Up Mode

Philips Components–Signetics

Document No.	853–1083
ECN No.	00933
Date of Issue	November 5, 1990
Status	Product Specification
Data Communication Products	

SCN68681
Dual asynchronous receiver/transmitter (DUART)

DESCRIPTION

The Signetics SCN68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices, and can also interface easily with other microprocessors. The DUART can be used in polled or interrupt driven systems.

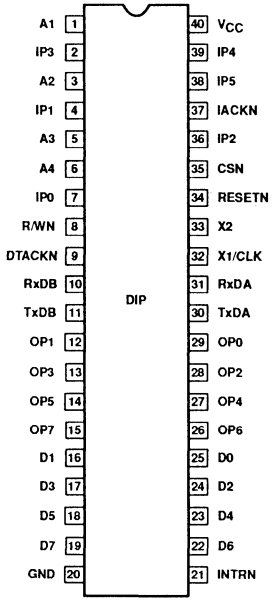
The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

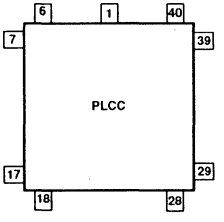
FEATURES

- S68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 6-bit input port
  - Can serve as clock or control inputs
  - Change-of-state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Interrupt vector output on interrupt acknowledge
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X - 1MB/sec, 16X - 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available
- DIP and PLCC packages

Dual asynchronous receiver/transmitter (DUART) SCN68681

PIN CONFIGURATIONS





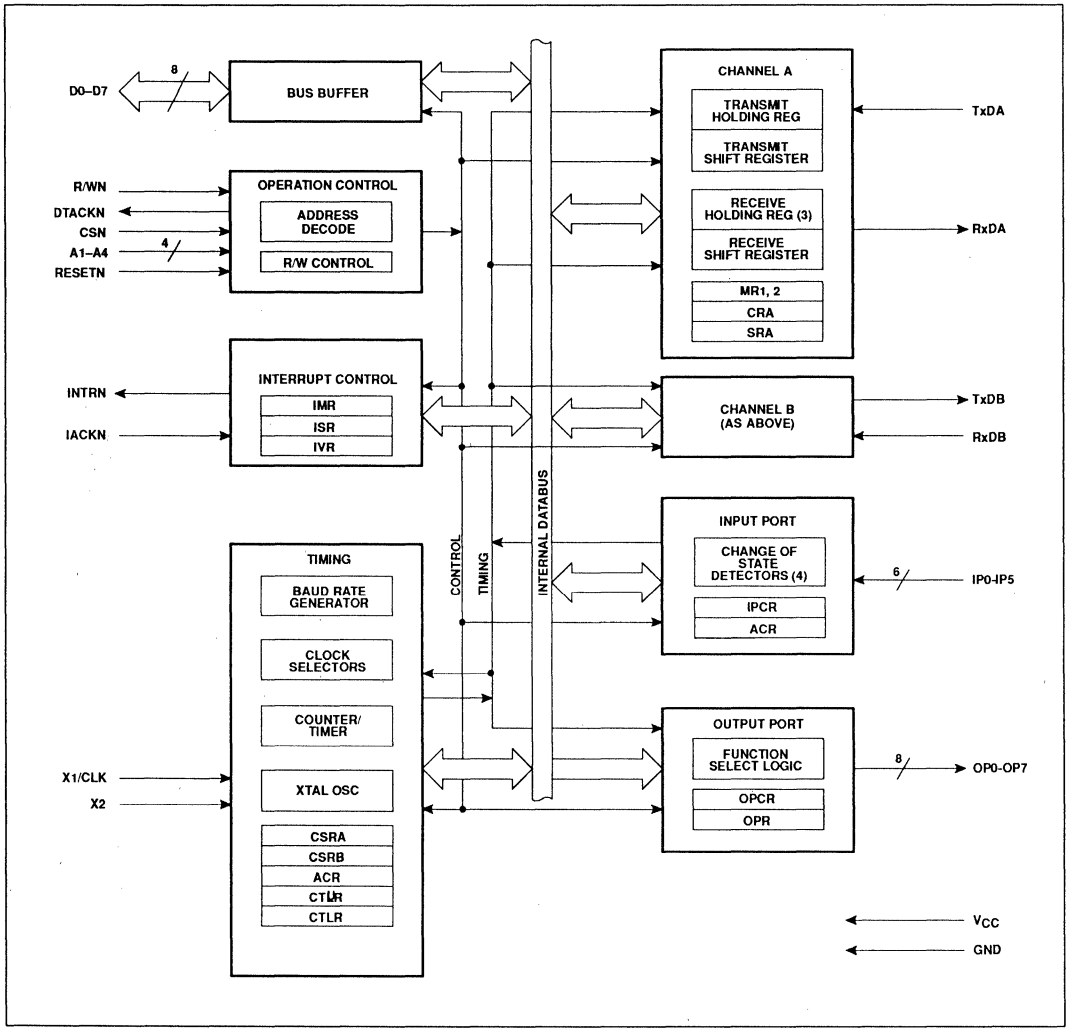
PIN/FUNCTION

1	NC	16	OP5	31	OP2
2	A1	17	OP7	32	OP0
3	IP3	18	D1	33	TxDA
4	A2	19	D3	34	NC
5	IP1	20	D5	35	RxDA
6	A3	21	D7	36	X1/CLK
7	A4	22	GND	37	X2
8	IP0	23	NC	38	RESETN
9	R/WN	24	INTRN	39	CSN
10	DTACKN	25	D6	40	IP2
11	RxDB	26	D4	41	IACKN
12	NC	27	D2	42	IP5
13	TxDB	28	D0	43	IP4
14	OP1	29	OP6	44	VCC
15	OP3	30	OP4		

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	V_{CC} = +5V +5%, T_A = 0°C to +70°C	V_{CC} = +5V +10%, T_A = 40°C to +85°C
40-Pin Ceramic DIP	SCN68681C1F40	SCN68681E1F40
40-Pin Plastic DIP	SCN68681C1N40	SCN68681E1N40
44-Pin Plastic LCC	SCN68681CIA44	SCN68681E1A44

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
D0-D7	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	I	**Chip Select:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the R/WN, RDN and A1-A4 inputs. When High, places the D0-D7 lines in the 3-State condition.
R/WN	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1-A4	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	I	**Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0-OP7 in the High state, stops the coutner/timer, and puts Channel A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state.
DTACKN	O	**Data Transfer Acknowledge:** Three-state active Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	I	**Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. If a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If an external clock is used, this pin should be grounded.
RxDA	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output.
OP5	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output.
OP6	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output.
OP7	O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYB output.
IP0	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	**Input 2:** General purpose input, or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP3	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	I	**Power Supply:** +5V supply input.
GND	I	**Ground:**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	See Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[5]		2			V
V_{IH}	Input high voltage (except X1/CLK)[4]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		4			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except o.d. outputs)[5]	I_{OH} = -400µA	2.4			V
V_{OH}	Output high voltage (except o.d. outputs)[4]	I_{OH} = -400µA	2.9			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	–10		10	µA
I_{LL}	Data bus 3-State leakage current	V_O = 0.4 to V_{CC}	–10		10	µA
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 grounded	-4	-2	0	mA
		V_{IN} = 0, X2 floated	-3	-1.5	0	mA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 grounded	-1	0.2	1	mA
		V_{IN} = V_{CC}, X2 floated	0	3.5	10	mA
I_{X2L}	X2 low input current	V_{IN} = 0, X1/CLK floated	-100	-30	0	µA
I_{X2H}	X2 high input current	V_{IN} = V_{CC}, X1/CLK floated	0	+30	100	µA
I_{OC}	Open-collector output leakage current	V_O = 0.4 to V_{CC}	–10		10	µA
I_{CC}	Power supply current					
	0°C to +70°C version				150	mA
	-40°C to +85°C version				175	mA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. T_A < 0°C
5. $T_A \geq$ 0°C

AC CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10% [1, 2, 3, 4]

SYMBOL	PARAMETER	LIMITS Min	Typ[3]	Max	UNIT
Reset Timing (See Figure 1)					
t_{RES}	RESETN pulse width	1.0			µs
Bus Timing (See Figures 2, 3 4)					
t_{AS}	A i-A4 setup time to CSN Low	10			ns
t_{AH}	A1-A4 hold time from CSN High	0			ns
t_{RWS}	RWN setup time to CSN High	0			ns
t_{RWH}	RWN holdup time to CSN High	0			ns
t_{CSW}	CSN High pulse width	90			ns
t_{CSD}[5]	CSN or IACKN High from DTACKN Low	20			ns
t_{DD}	Data valid from CSN or IACKN Low			175	ns
t_{DF}	Data bus floating from CSN or IACKN High[7]			100	ns
t_{DS}	Data setup time to CLK High	100			ns
t_{DH}	Data hold time from CSN High	0			ns
t_{DAL}	DTACKN Low from read data valid	0			ns
t_{DCR}	DTACKN Low (read cycle) from CLK High			125	ns
t_{DCW}	DTACKN Low (write cycle) from CLK High			125	ns
t_{DAH}	DTACKN High from CSN or IACKN High			100	ns
t_{DAT}	DTACKN High imepdance from CSN or IACKN High			125	ns
t_{CSC}[6]	CSN or IACKN setup time to clock High	90			ns
Port Timing (See Figure 5)					
t_{PS}	Port input setup time to CSN Low	0			ns
t_{PH}	Port input hold time from CSN High	0			ns
t_{PD}	Port output valid from CSN High			400	ns
Interrupt Reset Timing (See Figure 6)					
	INTRN or OP3-OP7 when used as interrupts negated from:				
	Read RHR (RxRDY/FFULL interrupt)			300	ns
	Write THR (TxRDY interrupt)			300	ns
t_{IR}	Reset command (delta break interrupt)			300	ns
	Stop C/T command (counter interrupt)			300	ns
	Read IPCR (input port change interrupt)			300	ns
	Write IMR (clear of interrupt mask bit)			300	ns
Clock Timing (See Figure 7)					
t_{CLK}	X1/CLK High or Low time	100			ns
f_{CLK}	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	CTCLK High or Low time	100			ns
f_{CTC}	CTCLK frequency	0		4.0	MHz
t_{RX}	RxC High or Low time	220			ns
f_{RX}	RxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
t_{TX}	TxC High or Low time	220			ns
f_{TX}	TxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
Transmitter Timing (See Figure 8)					
t_{TXD}	TxD output delay from TxC Low			350	ns
t_{TCS}	Output delay from TxC Low to TxD data output			150	ns
Receiver Timing (See Figure 9)					
t_{RXS}	RxD data setup time to RxC High	240			ns
t_{RXH}	RxD data hold time from RxC High	200			ns

NOTES:

1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
6. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
7. This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

Also provided on the SCN68681 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

BLOCK DIAGRAM

The SCN68681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR), the Auditary Control Register(ACR) and the Interrupt Vector Register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR regsiter on the data bus and asserting DTACKN.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART. If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4k baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCN68681 comprises a full-duplex asynchronous receiver/transmitter (DUART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (assuming that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee a true change in level has occurred, requires that two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. The 50µs time refers to the situation in which the change of state is just missed and the first change of state is not detected until 25µs later.

Input Port

The inputs to this unlatched 6-bit port can be read by the CPU by performing a read operation at address D16. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1 and D6 will reflect the level of IACKN. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

Output Port

The 8-bit multipurpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR[n] = 1 results in OP[n] = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SCN68681 is conditioned to transmit data when the transmitter is enabled through the command register. The SCN68681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCN68681 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect oper-

ate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'OA' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. SCN68681 Register Addressing

A4	A3	A2	A1	READ (R/WN = 1)	WRITE (R/WN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	*Reserved*	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	*Reserved*	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.

3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Verify the message is sent by waiting until the transmit ready status (TxRDY) is asserted. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

MR2A[4] – Channel A Clear-to-Send Control

If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IP0) each time it is ready to send a character. If IP0 is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

MR2A[3:0] – Channel A Stop Bit Length Select

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled), in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	**RxINT SELECT**	**ERROR MODE**	**PARITY MODE**	**PARITY TYPE**	**BITS PER CHARACTER**
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE	**TxRTS CONTROL**	**CTS ENABLE Tx**	**STOP BIT LENGTH***			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 - 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
	RECEIVER CLOCK SELECT	**TRANSMITTER CLOCK SELECT**
CSRA CSRB	See Text	See Text

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MISCELLANEOUS COMMANDS	**DISABLE Tx**	**ENABLE Tx**	**DISABLE Rx**	**ENABLE Rx**
CRA CRB	See Text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	**FRAMING ERROR***	**PARITY ERROR***	**OVERRUN ERROR**	**TxEMT**	**TxRDY**	**FFULL**	**RxRDY**
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	11 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	**COUNTER/TIMER MODE AND SOURCE**	**DELTA IP3 INT**	**DELTA IP2 INT**	**DELTA IP1 INT**	**DELTA IP0 INT**
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]
IVR								

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A receiver. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3-16X	IP3-16X
1111	IP3-1X	IP3-1X

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

Table 3. Baud Rate Clock = 3.6864 MHz

CSRA[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4k	19.2k
1101	Timer	Timer
1110	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP2-16X	IP2-16X
1111	IP2-1X	IP2-1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5-16X	IP5-16X
1111	IP5-1X	IP5-1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[6:4] – Miscellaneous Commands
The encoded value of this field may be used to specify a single command as follows:

CRA[6:4]	COMMAND
000	No command.
001	Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
010	Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
011	Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
100	Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
101	Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
110	Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
111	Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.,

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

NOTE:
Duty cycle of 16x clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR 6:4 Field Definition

ACR [6:4]	MODE	CLOCK SOURCE
000	Counter	External (IP2)*
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or external clock (x1/CLK) divided by 16
100	Timer	External (IP2)*
101	Timer	External (IP2) divided by 16*
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

NOTE:
* In these modes, the Channel B receiver clock should normally be generated from the baud rate generator.

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit

is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Current State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU read the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is 0002_{16}. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A4-A1 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR. The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A4-A1 = 1111). The command, however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

On power-up and after reset, the counter/timer runs in timer mode and can only be restarted. Because it cannot be shut off or stopped, and runs continuously in timer mode, it is recommended that at initialization, the output port, OP3, should be masked off through the OPCR[3:2] = 00 until the C/T is programmed to the desired operational state.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count 0000_{16}, the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

IVR – Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.

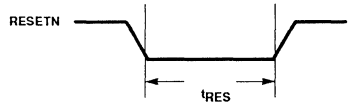


Figure 1. Reset Timing

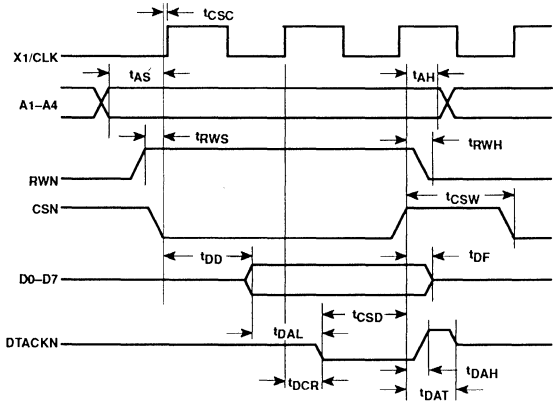


Figure 2. Bus Timing (Read Cycle)

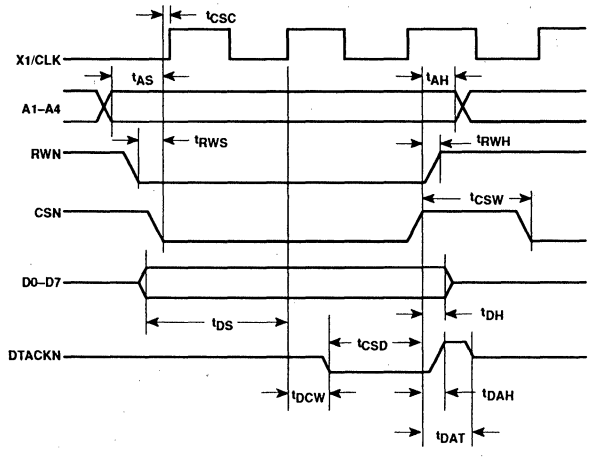


Figure 3. Bus Timing (Write Cycle)

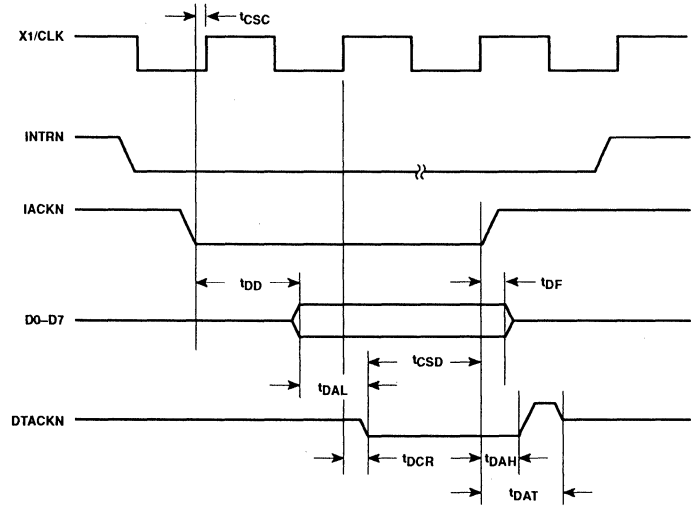


Figure 4. Interrupt Cycle Timing

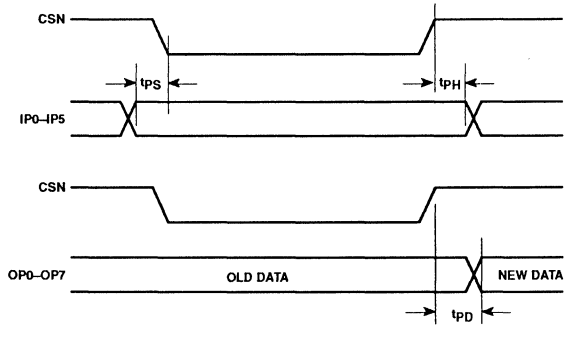
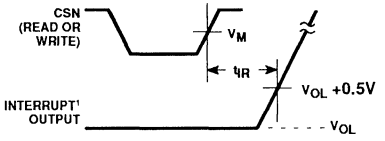


Figure 5. Port Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from themidpoint of the switching signal, V_M, to a point 0.5 volts above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 6. Interrupt Timing

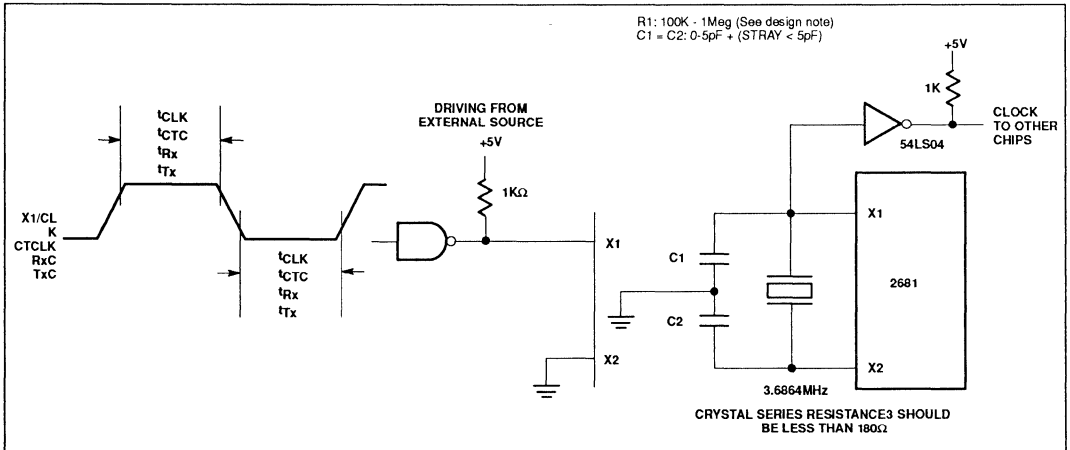


Figure 7. Clock Timing

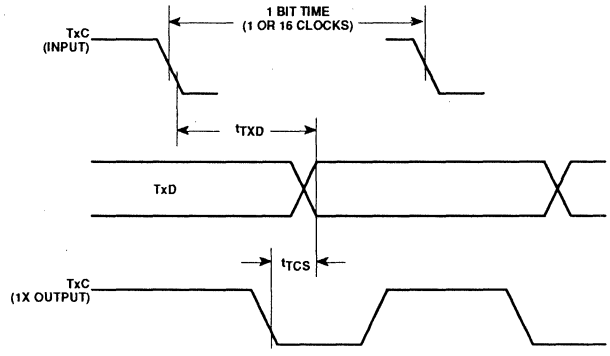


Figure 8. Transmit Timing

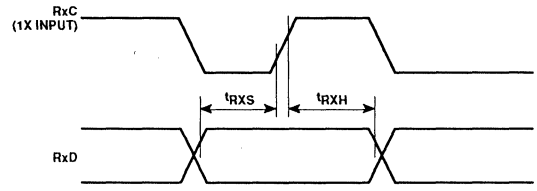
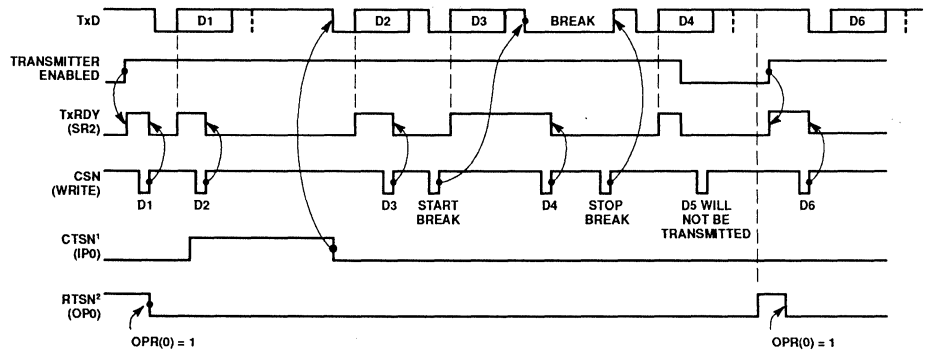
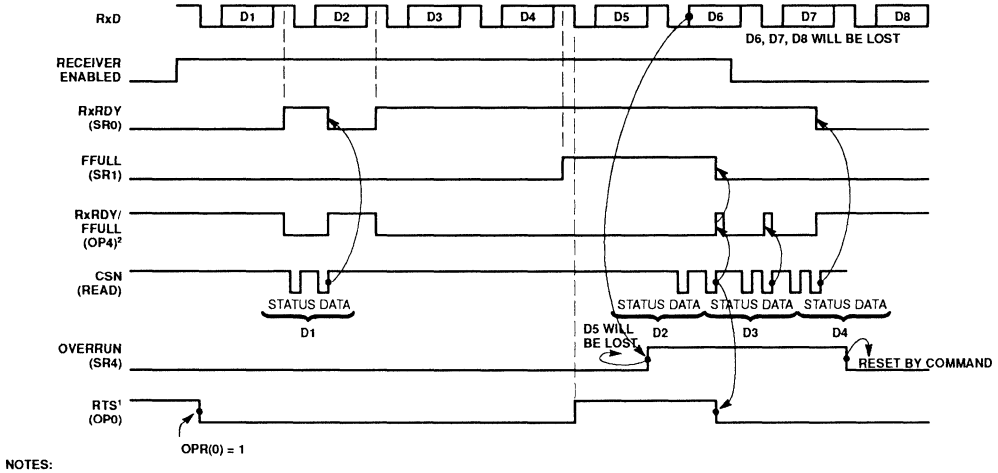


Figure 9. Receive Timing



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 10. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) and MR1(6) = 0.

Figure 11. Receiver Timing

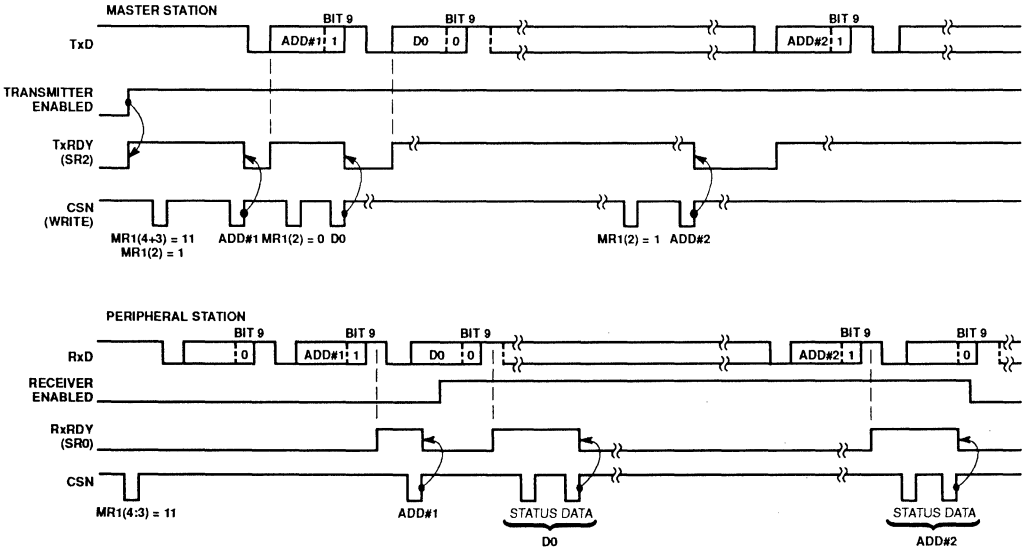


Figure 12. Wake-Up Mode

Philips Components–Signetics

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Data Communication Products	

SCC2691

Universal asynchronous receiver/transmitter (UART)

DESCRIPTION

The Signetics SCC2691 Universal Asynchronous Receiver/Transmitter (UART) is a single-chip CMOS-LSI communications device that provides a full-duplex asynchronous receiver/transmitter. It is fabricated with Signetics CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of the receiver and transmitter can be selected independently as one of 18 fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

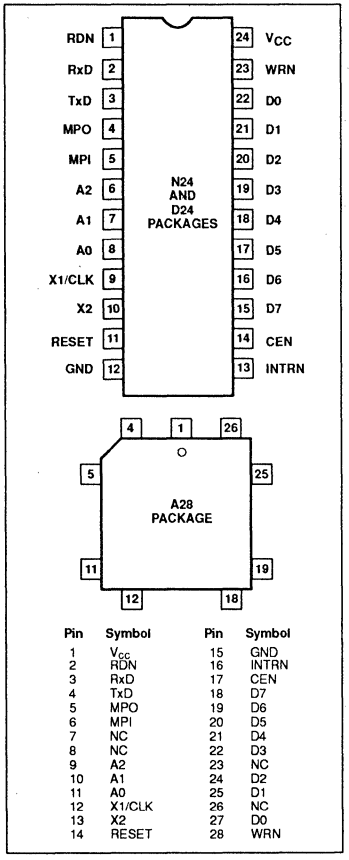
The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes.

The UART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- Full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud
  - One user-defined rate derived from programmable timer/ counter
  - External 1X or 16X clock
- Parity, framing, and overrun detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote Loopback
- Multi-function programmable 16-bit counter/timer
- Single interrupt output with seven maskable interrupting conditions
- On-chip crystal oscillator
- Low power mode
- TTL compatible
- Single +5V power supply
- Commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature versions available
- SOL, PLCC and 300 mil wide DIP packages available

PIN CONFIGURATIONS

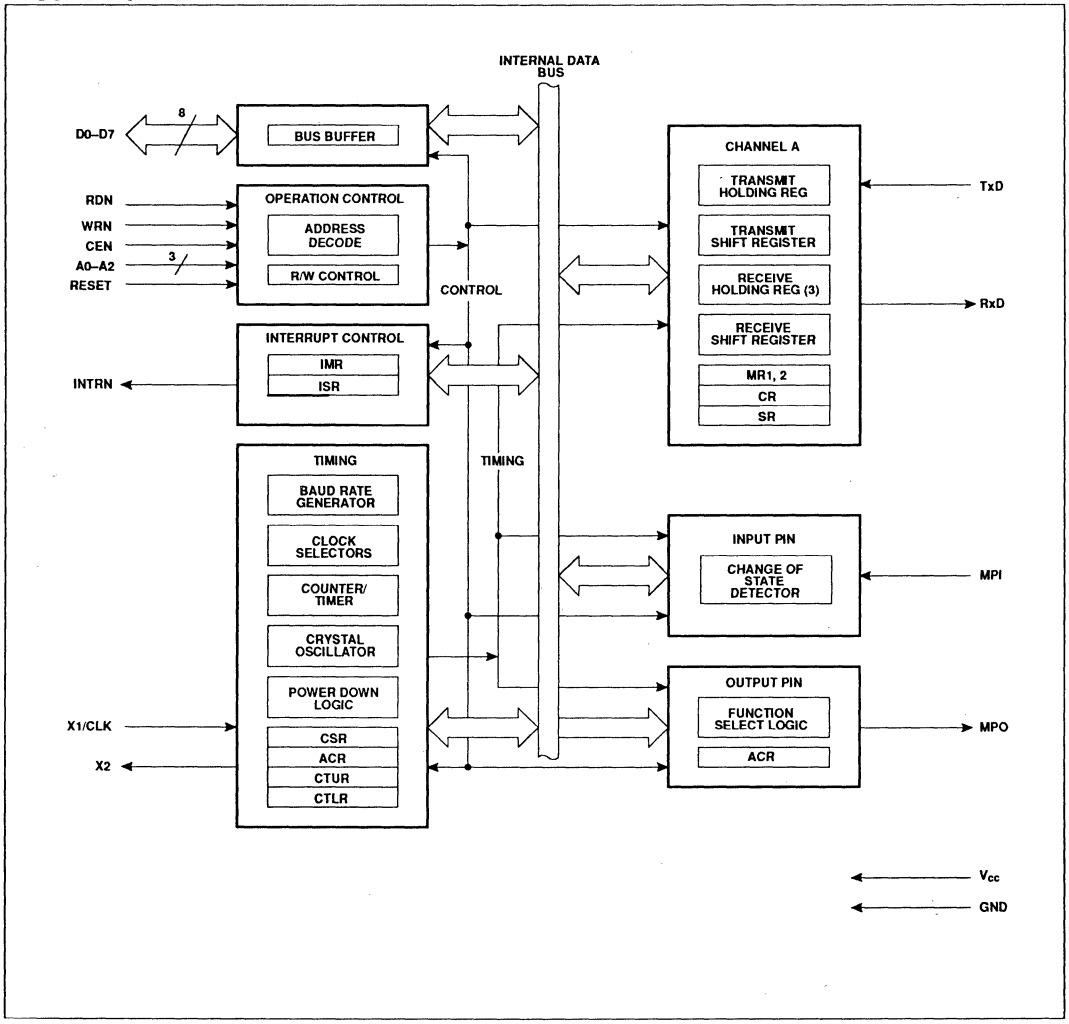


Pin	Symbol	Pin	Symbol
1	V_{CC}	15	GND
2	RDN	16	INTRN
3	RxD	17	CEN
4	TxD	18	D7
5	MPO	19	D6
6	MPI	20	D5
7	NC	21	D4
8	NC	22	D3
9	A2	23	NC
10	A1	24	D2
11	A0	25	D1
12	X1/CLK	26	NC
13	X2	27	D0
14	RESET	28	WRN

ORDERING INFORMATION

PACKAGES	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	V_{CC} = +5V ±10%, T_A = –40°C to +85°C
Plastic DIP	SCC2691AC1N24	SCC2691AE1N24
Plastic LCC	SCC2691AC1A28	SCC2691AE1A28
Plastic SOL	SCC2691AC1D24	

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
D0–D7	22–15	27, 25, 24, 22–18	I	**Data Bus:** Active-high 8-bit bidirectional 3-State data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is high, the data bus is in the 3-State condition.
CEN	14	17	I	**Chip Enable:** Active-low input. When low, data transfers between the CPU and the UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A2 inputs. When CEN is high, the UART is effectively isolated from the data bus and D0–D7 are placed in the 3-State condition.
WRN	28	28	I	**Write Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the data bus to be transferred to the register selected by A0–A2. The transfer occurs on the trailing (rising) edge of the signal.
RDN	1	2	I	**Read Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the register selected by A0–A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN.
A0–A2	8–6	11–9	I	**Address Inputs:** Active-high address inputs to select the UART registers for read/write operations.
RESET	11	14	I	**Reset:** Master reset. A high on this pin clears the status register (SR), the interrupt mask register (IMR), and the interrupt status register (ISR), sets the mode register pointer to MR1, and places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (high) state.
INTRN	13	16	O	**Interrupt Request:** This active-low output is asserted upon occurrence of one or more of seven maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s). This open-drain output requires a pull-up resistor.
X1/CLK	9	12	I	**Crystal 1:** Crystal or external clock input. When using the crystal oscillator, this pin serves as the connection for one side of the crystal. If a crystal is not used, an external clock is supplied at this input. An external clock (or crystal) is required even if the internal baud rate generator is not utilized. This clock is used to drive the internal baud rate generator, as an optional input to the timer/counter, and to provide other clocking signals required by the chip.
X2	10	13	I	**Crystal 2:** Connection for other side of crystal. If an external source is used instead of a crystal, this connection should be open.
RxD	2	3	I	**Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock.
TxD	3	4	O	**Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (high) condition when the transmitter is idle or disabled and when the UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock.
MPO	4	5	O	**Multi-Purpose Output:** One of the following functions can be selected for this output pin by programming the auxiliary control register: **RTSN** – Request to send active-low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full. **C/TO** – The counter/timer output. **TxC1X** – The 1X clock for the transmitter. **TxC16X** – The 16X clock for the transmitter. **RxC1X** – The 1X clock for the receiver. **RxC16X** – The 16X clock for the receiver. **TxRDY** – The transmitter holding register empty signal. Active-low output. **RxRDY/FFULL** – The receiver FIFO not empty/full signal. Active-low output.
MPI	5	6	I	**Multi-Purpose Input:** This pin can serve as an input for one of the following functions: **GPI** – General purpose input. The current state of the pin can be determined by reading the ISR. **CTSN** – Clear-to-send active-low input. **CTCLK** – Counter/timer external clock input. **RTCLK** – Receiver and/or transmitter external clock input. This may be a 1X or 16X clock as programmed by CSR[3:0] or CSR[7:4].
V_{CC}	24	1	I	**Power Supply:** +5V supply input.
GND	12	15	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to + 7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} ±10%	V
P_D	Power Dissipation	300	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperature, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See Ordering Information table for applicable operating temperature and V_{CC} supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage					
	All except X1/CLK		2			V
	X1/CLK		$0.8V_{CC}$		V_{CC}	V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}[4]	Output high voltage					
	(except open drain outputs)	I_{OH} = –400µA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	–10		10	µA
I_{LL}	Data bus 3-State leakage current	V_O = 0.4 to V_{CC}	–10		10	µA
I_{OD}	Open-drain output leakage curent	V_O = 0.4 to V_{CC}	–10		10	µA
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 floated	–100	–30	0	µA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 floated	0	30	100	µA
I_{X2L}	X2 low output current	V_{OUT} = 0, X1/CLK = V_{CC}	–100			µA
I_{X2H}	X2 high output current	V_{OUT} = V_{CC}, X1/CLK = 0V			100	µA
I_{CCA}	Power supply current, active					
	0°C to +70°C			0.8	2.0	mA
	–40°C to +85°C			1.0	2.5	mA
I_{CCD}	Power down current				500	µA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering Information table for applicable operating temperature and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0V and 2.8V with a transition time of 20ns max. For X1/CLK, this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2V and output voltages of 0.8V and 2V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kohms to V_{CC}.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4]

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Reset timing (Figure 1)					
t_{RES}	Reset pulse width	100			ns
Bus timing (Figure 2)[5]					
t_{AS}	A0–A2 setup time to RDN, WRN low	10			ns
t_{AH}	A0–A2 hold time from RDN, WRN high	0			ns
t_{CS}	CEN setup time to RDN, WRN low	0			ns
t_{CH}	CEN hold time from RDN, WRN high	0			ns
t_{RW}	WRN, RDN pulse width	150			ns
t_{DD}	Data valid after RDN low			125	ns
t_{DF}	Data bus floating after RDN high			110	ns
t_{DS}	Data setup time before WRN high	50			ns
t_{DH}	Data hold time after WRN high	30			ns
t_{RWD}	Time between reads and/or writes[6, 7]	150			ns
MPI and MPO timing (Figure 3)[5]					
t_{PS}	MPI input setup time before RDN low	30			ns
t_{PH}	MI input hold time after RDN low	30			ns
t_{PD}	MPO output valid after WRN high			370	ns
Interrupt timing (Figure 4)					
t_{IR}	INTRN negated				
	Read RHR (RxRDY/FFULL interrupt)			370	ns
	Write THR (TxRDY, TxEMT interrupt)			370	ns
	Reset command (break change interrupt)			370	ns
	Reset command (MPI change interrupt)			370	ns
	Stop C/T command (counter interrupt)			370	ns
	Write IMR (clear of interrupt mask bit)			270	ns
Clock timing (Figure 5)					
t_{CLK}	X1/CLK high or low time	100			ns
f_{CLK}	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	Counter/timer clock high or low time	100			ns
f_{CTC}	Counter/timer clock frequency	0[11]		4.0M	Hz
t_{RX}	RxC high or low time	220			ns
f_{RX}	RxC frequency (16X)	0[11]		2.0M	Hz
	RxC frequency (1X)	0[11]		1.0M	Hz
t_{TX}	TxC high or low time	220			ns
f_{TX}	TxC frequency (16X)	0[11]		2.0M	Hz
	TxC frequency (1X)	0[11]		1.0M	Hz
Transmitter timing (Figure 6)					
t_{TXD}	TxD output delay from TxC low			350	ns
t_{TCS}	TxC output delay from TxD output data	0		150	ns
Receiver timing (Figure 7)					
t_{RXS}	RxD data setup time to RxC high	100			ns
t_{RXH}	RxD data hold time from RxC high	100			ns

NOTES:

1. Parameters are valid over specified temperature range. See Ordering Information table for applicable operating temperature and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0V and 2.8V with a transition time of 20ns max. For X1/CLK, this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2V and output voltages of 0.8V and 2V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kohms to V_{CC}.
5. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN. CEN and RDN (also CEN and WRN) are ORed internally. As a consequence, this signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, this parameter defines the minimum high time between one CEN and the next. The RDN signal must be negated for t_{RWD} guarantee that any status register changes are valid.
7. Consecutive write operations to the command register require at least three rising edges of the X1 clock between writes.

BLOCK DIAGRAM

As shown in the block diagram, the UART consists of: data bus buffer, interrupt control, operation control, timing, receiver and transmitter.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and UART.

Interrupt Control

A single interrupt output (INTRN) is provided which may be asserted upon occurrence of any of the following internal events:

- Transmit holding register ready
- Transmit shift register empty
- Receive holding register ready or FIFO full
- Change in break received status
- Counter reached terminal count
- Change in MPI input
- Assertion of MPI input

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR can be programmed to select only certain of the above conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. However, the bits of the ISR are not masked by the IMR.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers 1 and 2 are accessed via an auxiliary pointer. The pointer is set to MR1 by RESET or by issuing a reset pointer command via the command register. Any read or write of the mode register while the pointer is at MR1 switches the pointer to MR2. the pointer then remains at MR2 so that subsequent accesses are to MR2, unless the pointer is reset to MR1 as described above.

Table 1. Register Addressing

A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	MR1, MR2	MR1, MR2
0	0	1	SR	CSR
0	1	0	Reserved*	CR
0	1	1	RHR	THR
1	0	0	Reserved*	ACR
1	0	1	ISR	IMR
1	1	0	CTU	CTUR
1	1	1	CTL	CTLR

NOTE;
*Reserved registers should never be read during operation since they are reserved for internal diagnostics.
ACR = Auxiliary control register
CR = Command register
CSR = Clock select register
CTL = Counter/timer lower
CTLR = Counter/timer lower register
CTU = Counter/timer upper
CTUR = Counter/timer upper register
MR = Mode register A
SR = Status register
THR = Tx holding register

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and two clock selectors.

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1/CLK is driven using a configuration similar to the one in Figure 5. In this case, the input high-voltage must be capable of attaining the voltage specified in the DC Electrical Characteristics. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied if the internal BRG is not used.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Thirteen of these are available simultaneously for use by the receiver and transmitter. Eight are fixed, and one of two sets of five can be selected by programming ACR[7]. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection by the receiver and er of any of these baud rates or an external timing signal.

The C/T operation is programmed by ACR[6:4]. One of eight timing sources can be used as the input to the C/T. The output of the C/T is available to the clock selectors and can be programmed by ACR[2:0] to be output on the MPO pin.

In the timer mode, the C/T generates a square wave whose period is twice the number of clock periods loaded into the C/T upper and lower registers. The counter ready bit in the ISR is set once each cycle of the square wave. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be affected. In this mode the C/T runs continuously and does not recognize the stop counter command (the command only resets the counter ready bit in the ISR). Receipt of a start C/T command causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR. Counting begins upon receipt of a start C/T command. Upon reaching terminal count, the counter ready bit in the ISR is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state and the counter ready bit is cleared when the counter is stopped by a stop counter command. the CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command following a stop counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter are read. However, a subsequent start counter command causes the counter to begin a new count cycle using the values in CTUR and CTLR.

Receiver and Transmitter

The UART is a full-duplex asynchronous receiver/transmitter. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input. Registers associated with the communications channel are: the mode registers (MR1 and MR2), the clock select register (CSR), the command reg-

ister (CR), the status register (SR), the transmit holding register (THR), and the receive holding register (RHR).

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the THR. In the 16X clock mode, this also resynchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

The transmitter can be forced to send a break (continuous low condition) by issuing a start break command via the CR. The break is terminated by a stop break command.

If the transmitter is disabled, it continues operating until the character currently being transmitted and the character in the THR, if any, are completely sent out. Characters cannot be loaded in the THR while the transmitter is disabled.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU. The receiver looks for a high-to-low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled high, the start bit is invalid and the search for a valid start bit begins again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one sop bit has been detected. The data is then transferred to the RHR and the RxRDY bit in the SR is set to a 1. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point(one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

RECEIVER FIFO

The RHR consists of a first-in-first-out (FIFO) queue with a capacity of three characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three queue positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in mode register 1. In the character mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set upon receipt of the start bit of the new (overrunning) character.

WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the UART incorporates a special mode which provides automatic wake-up of the receiver through address frame recognition for multi-processor communications. This mode is selected by programming bits MR1[4:3] to '11'.

In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, whose receivers are normally disabled, examine the received data stream and 'wake-up' the CPU [by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1[2]. MR1[2] = 0 transmits a zero in the A/D bit position which identifies the corresponding data bits as data, while MR1[2] = 1 transmits a one in the A/D bit position which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits in the THR.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RHR FIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RHR. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

MULTI-PURPOSE INPUT PIN

The MPI pin can be programmed as an input to one of several UART circuits. The function of the pin is selected by programming the appropriate control register (MR2[4]), ACR[6:4], CSR [7:4, 3:0]). Only one of the functions may be selected at any given time. If CTS or GPI is selected, a change of state detector provided with the pin is activated. A high-to-low or low-to-high transition of the inputs lasting longer than 25–50μs sets the MPI change-of-state bit in the interrupt status register. The bit is cleared via a command. The change-of-state can be programmed to generate an interrupt to the CPU by setting the corresponding bit in the interrupt mask register.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This produces a sampling period of slightly more than 25μs (assuming a 3.6864MHz oscillator input). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two

successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. The 50µs time refers to the condition where the change of state is just missed and the first change of state is not detected until after an additional 25µs.

MULT-PURPOSE OUTPUT PIN

This pin can be programmed to serve as a request-to-send output, the counter/timer output, the output for the 1X or 16X transmitter or receiver clocks, the TxRDY output or the RxRDY/FFULL output (see ACR[2:0] – MPO Output Select).

REGISTERS

The operation of the UART is programmed by writing control words in the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is as described in Table 1.

The contents of certain control registers are initialized to zero on reset (see RESET pin description). Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. The contents of the MR, the CSR, and the ACR should only be changed while the receiver and transmitter are disabled, and certain changes to the ACR should only be made while the C/T is stopped. The bit formats of the UART are shown in Table 2.

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via the CR. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Control

The bit controls the deactivation of the RTSN output (MPO) by the receiver. This output is normally asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is reasserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input of the transmitting device.

MR1[6] – Receiver Interrupt Select

This bit selects either the receiver ready status (RxRDY) or the FIFO full status (FFULL) to be used for CPU interrupts.

MR1[5] – Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis. The status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

MR1[4:3] – Parity Mode Select

If with parity or force parity is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR![4:3] = 11 selects the channel to operate in the special wake-up mode.

MR1[2] – Parity Type Select

This bit selects the parity type (odd or even) if the with parity mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the force parity mode is programmed. It has no effect if the no parity mode is programmed. In the special wake-up mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits Per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select

The UART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

When switching in and out of the various modes, the selected mode is activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of auto-echo or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated in auto-echo by assertion o fRxRDY), and the transmitter is enabled, the transmitter is enabled, the transmitter will remain in auto-echo mode until one full stop bit has been retransmitted.

MR2[5] – Transmitter Request-to–Send Control

This bit controls the deactivation of the RTSN output (MPO) by the transmitter. This output is normally asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the THR (if any) are completely transmitted (including the programmed number of stop bits) if the transmitter is not enabled. This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Disable transmitter after the last character of the message is loaded in the THR.
6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

Table 2. Register Bit Formats

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MR1 (Mode Register 1)							
RxRT Control	**RxINT Select**	**Error Mode**	**Parity Mode**		**Parity Type**	**Bits per Character**	
0 = no 1 = yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With parity 01 = Force parity 10 = No parity 11 = Special mode		0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8	
MR2 (Mode Register 2)							
Channel Mode		**TxRTS Control**	**CTS Enable Tx**	**Stop Bit Length***			
00 = Normal 01 = Auto echo 10 = Local loop 11 = Remote loop		0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 =1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000
NOTE: *Add 0.5 to values shown for 0–7 if channel is programmed for 5 bits/character.							
CSR (Clock Select Register)							
Receiver Clock Select				**Transmitter Clock Select**			
See Text				See Text			
CR (Command Register)							
Miscellaneous Commands				**Disable Tx**	**Enable Tx**	**Disable Rx**	**Enable Rx**
See Text				0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes
SR (Channel Status Register)							
Received Break	**Framing Error**	**Parity Error**	**Overrun Error**	**TxEMT**	**TxRDY**	**FFULL**	**RxRDY**
0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes
NOTE: *These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4;0]. These bits are cleared by a reset error status command. In character mode they are reset when the corresponding data character is read from the FIFO.							
ACR (Auxiliary Control Register)							
BRG Set Select	**Counter/Timer Mode and Source**			**Power-Down Mode**	**MPO Pin Function Select**		
0 = Set 1 1 = Set 2	See Text			0 = On 1 = Off	000 = RTSN 001 = C/TO 010 = TxC (1X) 011 = TxC (16X)	100 = RxC (1X) 101 = RxC (16X) 110 = TxRDY 111 = RxRDY/FFULL	
ISR (Interrupt Status Register)							
MPI Pin Change	**MPI Pin Current State**	**Not used**	**Counter Ready**	**Delta Break**	**RxRDY/ FFULL**	**TxEMT**	**TxRDY**
0 = No 1 = Yes	0 = Low 1 = High		0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

Table 2. Register Bit Formats (Continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IMR (Interrupt Mask Resister)							
MPI Change Interrupt	MPI Level Interrupt	Not used	Counter Ready Int	Delta Break Interrupt	RxRDY/FFULL Interrupt	TxEMT Interrupt	TxRDY Interrupt
0 = Off 1 = On	0 = Off 1 = On		0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On
CTUR (Counter/Timer Upper Register)							
C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTLR (Counter/Timer Lower Register)							
C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

MR2[4] – Clear-to-Send Control

The sate of this bit determines if the CTSN input (MPI) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (low), the character is transmitted. If it is negated (high), the TxD output remains in the marking state and the transmission is delayed until CTSN goes low. Changes in CTSN while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a mark condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled). If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmittted.

CSR – Clock Select Register

CSR[7:4] – Receiver Clock Select

This field selects the baud rate clock for the receiver as shown in Table 3. The baud rates listed are for a 3.6864MHz crystal or external clock.

CSR[3:0] – Transmitter Clock Select

This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3.

Table 3. Baud Rate Selection

CSR[3:0]/ [7:4]	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	50
0 0 0 1	110	110
0 0 1 0	134.5	134.5
0 0 1 1	200	150
0 1 0 0	300	300
0 1 0 1	600	600
0 1 1 0	1,200	1,200
0 1 1 1	1,050	1,050
1 0 0 0	2,400	2,400
1 0 0 1	4,800	4,800
1 0 1 0	7,200	1,800
1 0 1 1	9,600	9,600
1 1 0 0	38.4k	19.2k
1 1 0 1	Timer	Timer
1 1 1 0	MPI – 16X	MPI – 16X
1 1 1 1	MPI–1X	MPI–1X

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111.

CR – Command Register

CR is used to write commands to the UART. Multiple commands can be specified in a single write to CR as long as the commands are non-conflicting, e.g., the enable transmitter and reset transmitter commands cannot be specified in a single command word.

CR[7:4] – Miscellaneous Commands

The encoded value of this field may be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the MR pointer to point to MR1.

0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disable and the FIFO is flushed.

0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied

0100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.

0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[3]) to be cleared to zero.

0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the THR, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break

0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

1000 Start C/T. In counter or timer modes, causes the contents of CTUR/CTLR to be preset into the counter/timer and starts the counting cycle. In timer mode, any counting cycle in progress when the command is issued is terminated. In counter mode, has no effect unless a stop C/T command was issued previously.

1001 Stop counter. In counter mode, stops operation of the counter/timer, resets the counter ready bit in the ISR, and forces the MPO output high if it is programmed to be the output of the C/T. In timer mode, resets the counter ready bit in the ISR but has no effect on the counter/timer itself or on the MPO output.

1010 Assert RTSN. Causes the RTSN output (MPO) to be asserted (low).

1011 Negate RTSN.Causes the RTSN output (MPO) to be negated (high).

1100 Reset MPI change interrupt. Causes the MPI change bit in the interrupt status register (ISR[7]) to be cleared to zero.

1101 Reserved.

111x Reserved.

CR[3] – Disable Transmitter
This command terminates operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CR[2] – Enable Transmitter
Enables operation of the channel A transmitter. The TxRDY status bit will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately; a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wake-up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

The status register is updated while RDN is negated. Therefore, the bus interface used with this device must not use a static RDN line. The RDN line must be pulsed to allow status register updates.

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxD line returns to the marking state for at least one half bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the change in break bit in the ISR (ISR[3]) is set. ISR[3] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character time in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the with parity or force parity mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In special wake-up mode, the parity error bit stores the received A/D bit.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SR[3] – Transmitter Empty (TxEMT)
This bit will be set when the transmitter underruns, i.e., both the transmit holding register (THR) and the transmit shift register are empty. However, this bit is not set until at least one character has been transmitted. It is set after transmission of the last stop bit of a character, If no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU, or when the transmitter is disabled.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded in the THR while the transmitter is disabled will not be transmitted.

SR[1] – FIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL will be reset by the CPU read and then set by the transfer of the character to the FIFO, which causes all three FIFO positions to be occupied.

SR[0] – Receiver Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, and no more characters are in the FIFO.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select

This bit selects one of two sets of baud rates generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the receiver and transmitter. See Table 4 for characteristics of the BRG.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as follows:

ACR [6:4]	Mode	Clock Source
0 0 0	Counter	MPI pin
0 0 1	Counter	MPI pin divided by 16
0 1 0	Counter	TxC–1X clock of the transmitter
0 1 1	Counter	Crystal or external clock (X1/CLK) divided by 16
1 0 0	Timer	MPI pin
1 0 1	Timer	MPI pin divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3] – Power-Down Mode Select
This bit, when set to zero, selects the power-down mode. In this mode, the SCC2691 oscillator is stopped and all functions requiring this clock are suspended. The contents of all registers are saved. It is recommended that the transmitter and receiver be disabled prior to placing the SCC2691 in this mode. Note that this bit must be set to a logic 1 after reset.

When the power-down mode is enabled, internal circuitry forces the X1/CLK pin to the low state and the X2 pin to the high state. If an external clock is being used to drive the device, it is recommended that the clock source be three-stated or forced low while the UART is in power-down mode in order to prevent the clock driver from being short circuited.

Table 4. BRG Characteristics

Crystal or Clock = 3.6864MHz

Nom Rate (Baud)	Actual 16X* Clock (kHz)	Error (%)
50	0.8	0
75	1.2	0
110	1.759	–0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	–0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

*Duty cycle of 16X clock is 50% ±1%

ACR[2:0] – MPO Output Select
This field programs the MPO output pin to provide one of the following:

000 Request-to-send active-low output (RTSN). This output is asserted and negated via the command register. RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted out or when the receiver FIFO and receiver shift register are full using MR2[5] and MR1[7], respectively.

001 The counter/timer output. In the timer mode, this output is a square wave with a period of twice the value (in clock periods) of the contents of the CTUR and CTLR. In the counter mode, the output remains high until the terminal count is reached, at which time it goes low. the output returns to the high state when the counter is stopped by a stop counter command.

010 The 1X clock for the transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a non-synchronized 1X clock is output.

011 The 16X clock for the transmitter. This is the clock selected by CSR[3:0] = 1111.

100 The 1X clock for the receiver, which is the clock that samples the received data. If data is not being received, a non-synchronized 1X clock is output.

101 The 16X clock for the receiver. This is the clock selected by CSR[7:4], and is a 1X clock if CSR[7:4] = 1111.

110 The transmitter register empty signal, which is the complement of SR[2]. Active low output.

111 The receiver ready or FIFO full signal (complement of ISR[2]). Active-low output.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output is asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR. This register is cleared when the device is reset.

ISR[7] – MPI Change-of-State
This bit is set when a change-of-state occurs at the MPI input pin. It is reset by a reset change interrupt command.

ISR[6] – MPI Current State
This bit provides the current state of the MPI pin. This information is latched and reflects the state of the pin at the leading edge of the ISR ready cycle.

ISR[4] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[3] – Change in Break
This bit, when set, indicates that the receiver has detected the beginning or end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[2] – Receiver Ready or FIFO Full
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the FIFO is read and there is no character in the receive shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[1] – Transmitter Empty
This bit is a duplicate of TxEMT (SR[3]).

ISR[0] – Transmitter Ready
This bit is a duplicate of TxRDY (SR[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the INTRN output is asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded is 0002_{16}.

In the timer (programmable divider) mode, the C/T generates a square wave whose period is twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be.

The counter ready status bit (ISR[4]) is set once each cycle of the square wave. The bit is reset by a stop counter command. The command, however, does not stop the C/T. The generated square wave is output on MPO if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR. Counting begins upon receipt of a start C/T command. Upon reaching the terminal count, the counter ready interrupt bit (ISR[4]) is set. the counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains high until the terminal count is reached, at which time it goes low.

The output returns to the high state and ISR[4] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

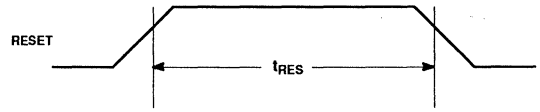


Figure 1. Reset Timing

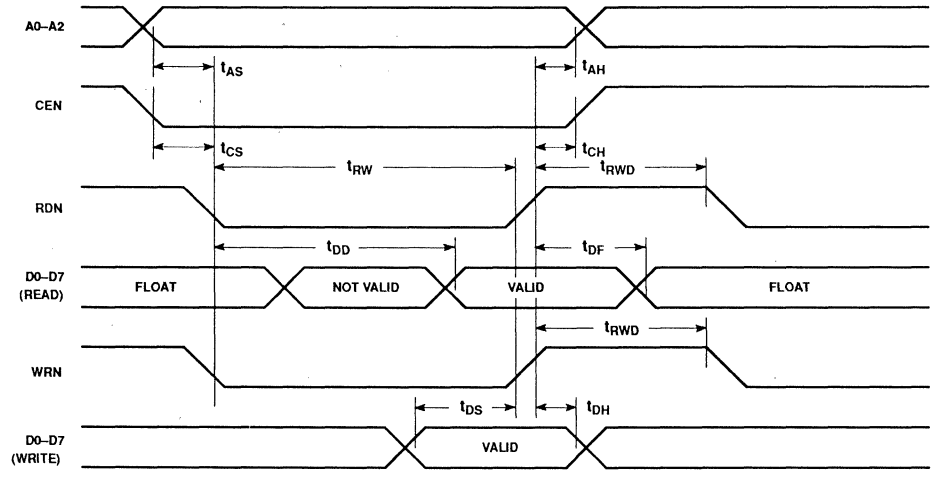


Figure 2. Bus Timing

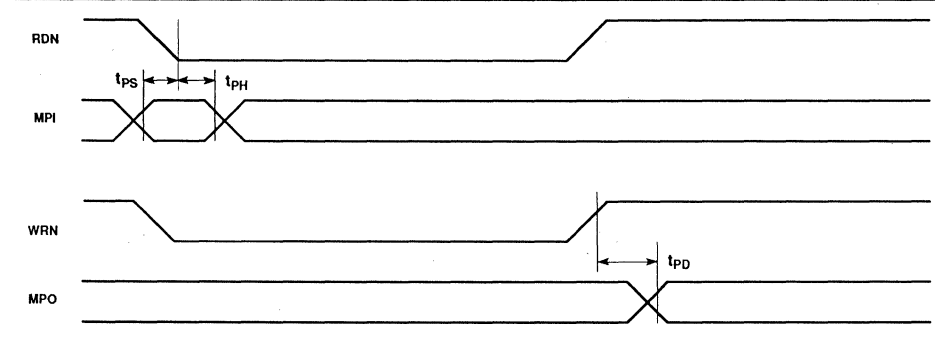
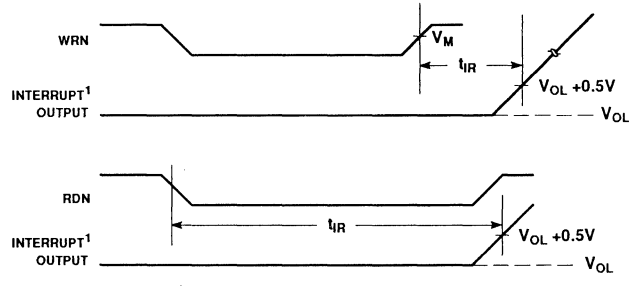


Figure 3. I/O Timing



NOTES:
1. INTRN or MPO when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing

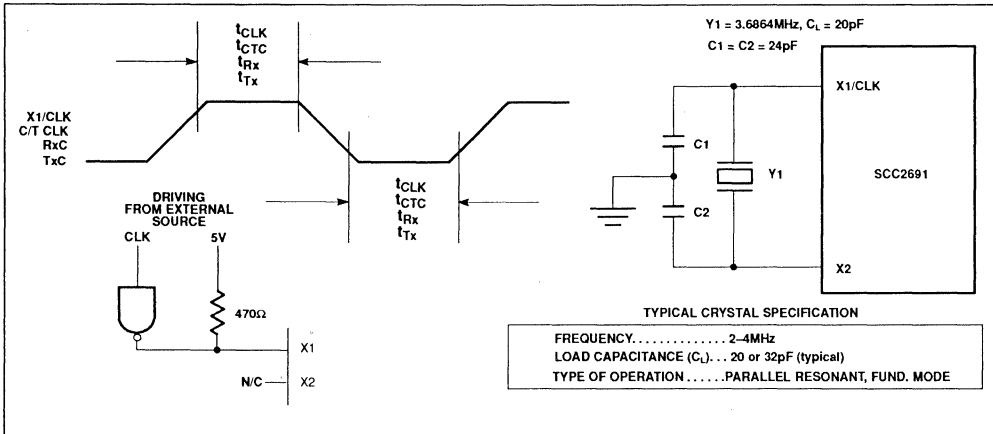


Figure 5. Clock Timing

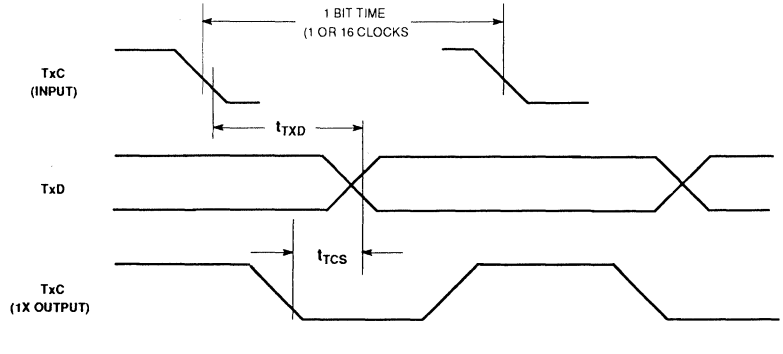


Figure 6. Transmit Timing

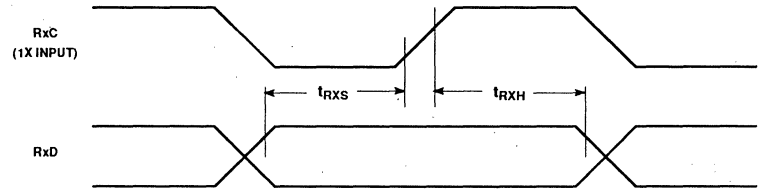
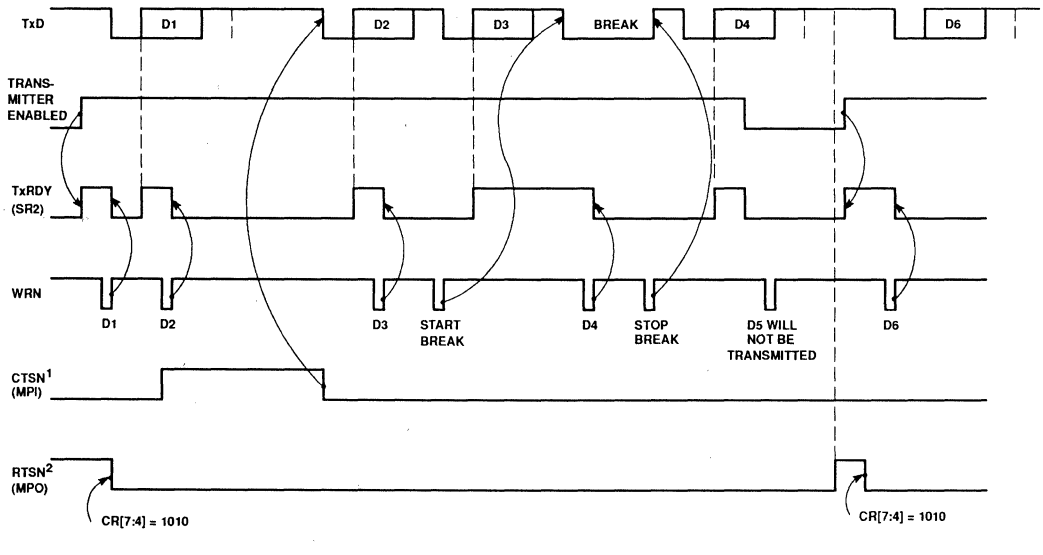


Figure 7. Receive Timing



NOTES:
1. TIMING SHOWN FOR MR2[4] = 1.
2. TIMING SHOWN FOR MR2[5] = 1.

Figure 8. Transmitter Timing

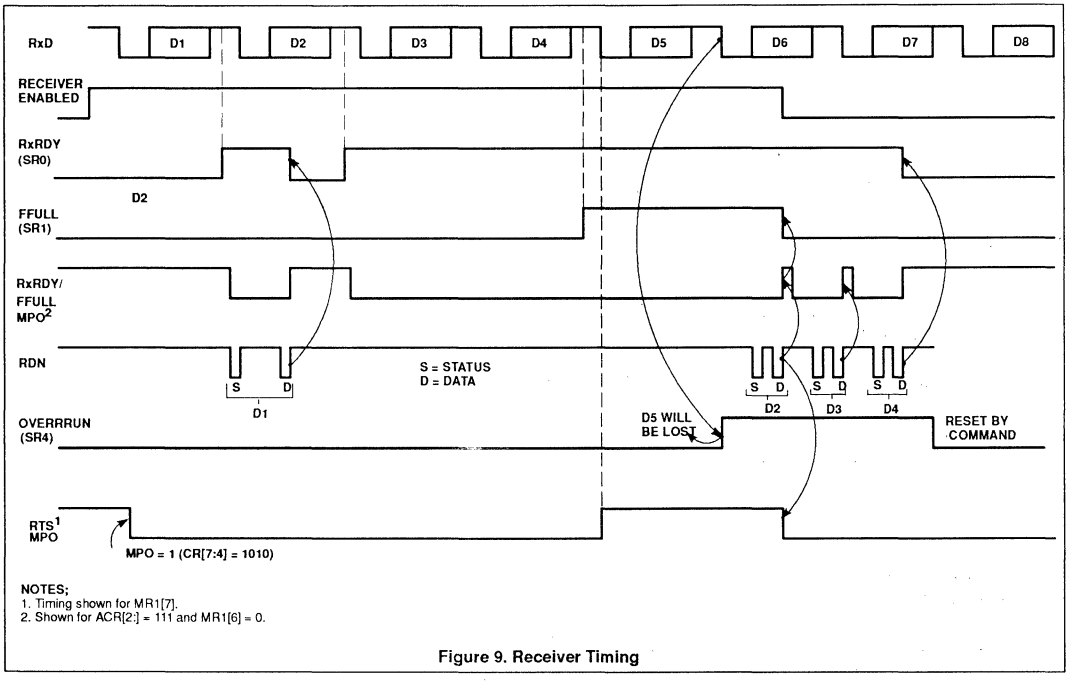


Figure 9. Receiver Timing

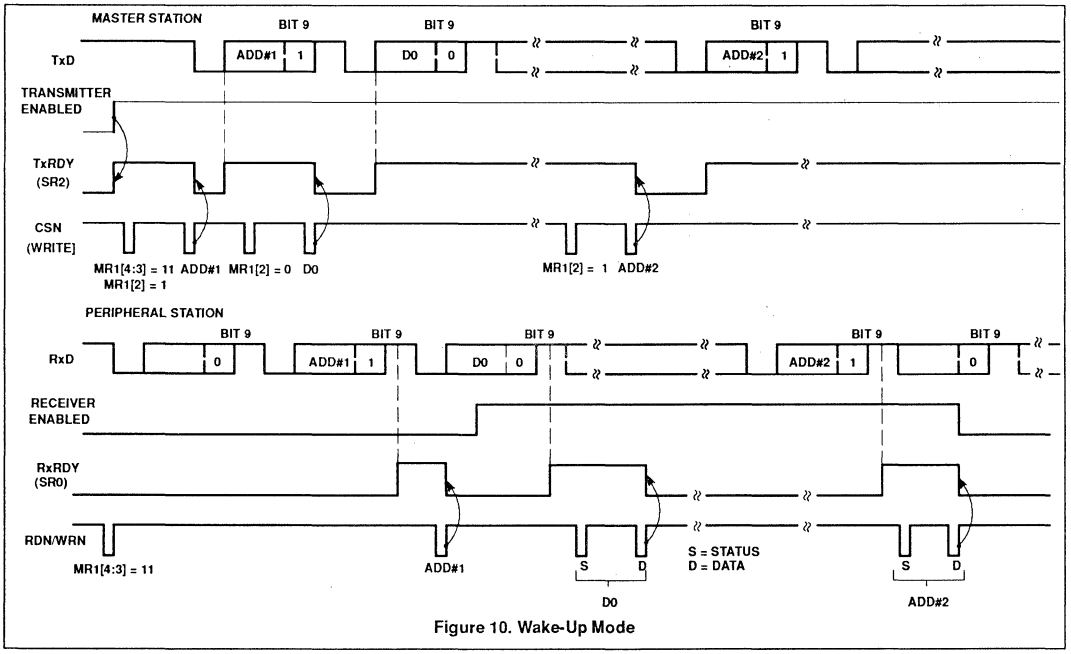


Figure 10. Wake-Up Mode

Philips Components–Signetics

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Date of Issue	November 5, 1990
Status	Product Specification
Data Communication Products	

SCC2692
Dual asynchronous receiver/transmitter (DUART)

DESCRIPTION

The Signetics SCC2692 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCC2692 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

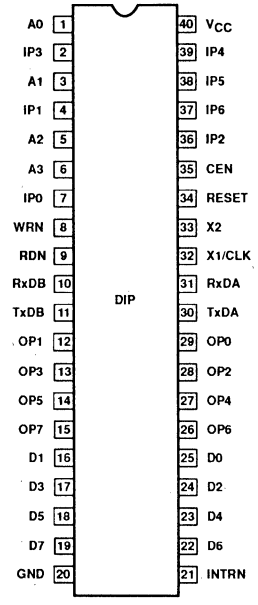
The SCC2692 is available in three package versions: 40-pin and 28-pin, 0.6" wide, DIPs and a 44-pin PLCC.

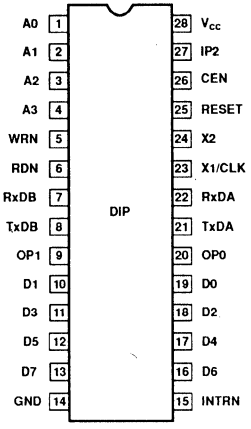
FEATURES

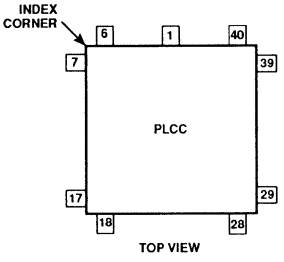
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial and industrial temperature range versions
- TTL compatible
- Single +5V power supply

Dual asynchronous receiver/transmitter (DUART) SCC2692

PIN CONFIGURATIONS







TOP VIEW

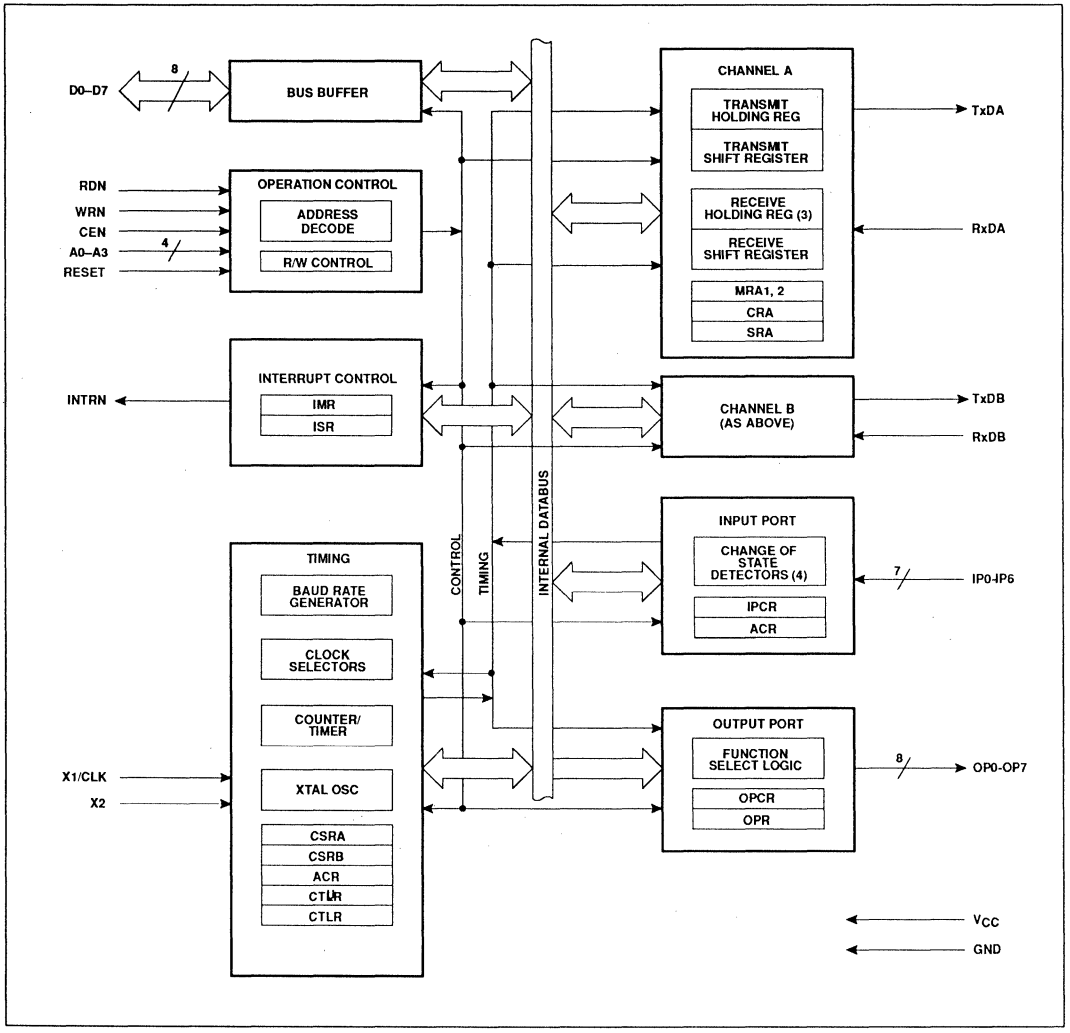
PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C
40-Pin Cerdip	SCC2692AC1F40	SCC2692AE1F40
28-Pin Cerdip	SCC2692AC1F28	SCC2692AE1F28
40-Pin Plastic DIP	SCC2692AC1N40	SCC2692AE1N40
28-Pin Plastic DIP	SCC2692AC1N28	SCC2692AE1N28
44-Pin Plastic LCC	SCC2692AC1A44	SCC2692AE1A44

Dual asynchronous receiver/transmitter (DUART) SCC2692

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	APPLICABLE		TYPE	NAME AND FUNCTION
	40,44	28		
D0-D7	X	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus are loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state.
INTRN	X	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	X	X	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). If X1/CLK is driven from an external source, this pin can be left open or connected to ground.
RxDA	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	X	X	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	X	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X		O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X		O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X		O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	X		O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	X		O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	X		O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYBN output.
IP0	X		I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	X		I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	X	X	I	**Input 2:** General purpose input or counter/timer external clock input.
IP3	X		I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.

PIN DESCRIPTION (Continued)

SYMBOL	APPLICABLE		TYPE	NAME AND FUNCTION
	40,44	28		
IP4	X		I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X		I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X		I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	I	**Power Supply:** +5V supply input.
GND	X	X	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	-0.5 to V_{CC} +0.5	V
P_D	Power dissipation	750	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{IL}	Input low voltage					V
V_{IH}	Input high voltage (except X1/CLK)[6]		2.0		0.8	V
V_{IH}	Input high voltage (except X1/CLK)[7]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		0.8 V_{CC}			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = -400µA	V_{CC} -0.5			V
I_{IX1PD}	X1/CLK input current - power down	V_{IN} = 0 to V_{CC}	-10		+10	µA
I_{ILX1}	X1/CLK input low current - operating	V_{IN} = 0	-75		0	µA
I_{IHX1}	X1/CLK input high current - operating	V_{IN} = V_{CC}	0		75	µA
I_{OHX2}	X2 output high current - operating	V_{OUT} = V_{CC}, X1 = 0	0		+75	µA
I_{OHX2S}	X2 output high short circuit current - operating	V_{OUT} = 0, X1 = 0	-10		-1	mA
I_{OLX2}	X2 output low current - operating	V_{OUT} = 0, X1 = V_{CC}	-75		0	µA
I_{OLX2S}	X2 output low short circuit current - operating and power down	V_{OUT} = V_{CC}, X1 = V_{CC}	1		10	mA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	-10		+10	µA
	Input port pins	V_{IN} = 0 to V_{CC}	-20		+10	µA
I_{OZH}	Output off current high, 3-state data bus	V_{IN} = V_{CC}			10	µA
I_{OZL}	Output off current low, 3-state data bus	V_{IN} = 0V	-10			µA
I_{ODL}	Open-drain output low current in off-state	V_{IN} = 0	-10			µA
I_{ODH}	Open-drain output high current in off-state	V_{IN} = V_{CC}			10	µA
	Power supply current[5]					
	Operating mode	TTL input levels			10	mA
I_{CC}		CMOS input levels			10	mA
	Power down mode	TTL input levels			3.0	mA
		CMOS input levels			2.0	mA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of V_{CC} -0.2V and V_{SS} + 0.2V.
6. $T_A \geq 0°C$
7. $T_A < 0°C$

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	PARAMETER	LIMITS Min	LIMITS Typ[3]	LIMITS Max	UNIT
Reset Timing (See Figure 1)					
t_{RES}	RESET pulse width	1.0			µs
Bus Timing[5] (See Figure 2)					
t_{AS}	A0-A3 setup time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 hold time from RDN, WRN Low	100			ns
t_{CS}	CEN setup time to RDN, WRN Low	0			ns
t_{CH}	CEN hold time from RDN, WRN High	0			ns
t_{RW}	WRN, RDN pulse width	225			ns
t_{DD}	Data valid after RDN Low			175	ns
t_{DA}	RDN Low to data bus active[7]	15			ns
t_{DF}	Data bus floating after RDN High			125	ns
t_{DI}	RDN High to data bus invalid[7]	20			ns
t_{DS}	Data setup time before WRN High	100			ns
t_{DH}	Data hold time after WRN High	5			ns
t_{RWD}	High time between reads and/or writes[5, 6]	200			ns

AC CHARACTERISTICS (Continued)[1, 2, 4]

SYMBOL	PARAMETER	LIMITS Min	Typ[3]	Max	UNIT
Port Timing[5] (See Figure 3)					
t_{PS}	Port input setup time before RDN Low	0			ns
t_{PH}	Port input hold time after RDN High	0			ns
t_{PD}	OP_n output valid from WRN High			400	ns
Interrupt Timing (See Figure 4)					
t_{IR}	INTRN (or OP3-OP7 when used as interrupts) negated from:				
	Read RHR (RxRDY/FFULL interrupt)			300[9]	ns
	Write THR (TxRDY interrupt)			300[9]	ns
	Reset command (break change interrupt)			300[9]	ns
	Stop C/T command (counter interrupt)			300[9]	ns
	Read IPCR (input port change interrupt)			300[9]	ns
	Write IMR (clear of interrupt mask bit)			300[9]	ns
Clock Timing (See Figure 5)					
t_{CLK}	X1/CLK High or Low time	100			ns
f_{CLK}	X1/CLK frequency	2	3.6864	4	MHz
t_{CTC}	CTCLK (IP2) High or Low time	100			ns
f_{CTC}	CTCLK (IP2) frequency[8]	0		4	MHz
t_{RX}	RxC High or Low time	220			ns
f_{RX}	RxC frequency (16X)[8]	0		2	MHz
	(1X)[8]	0		1	MHz
t_{TX}	TxC High or Low time	220			ns
f_{TX}	TxC frequency (16X)[8]	0		2	MHz
	(1X)[8]	0		1	MHz
Transmitter Timing (See Figure 6)					
t_{TXD}	TxD output delay from TxC Low			350	ns
t_{TCS}	Output delay from TxC Low to TxD data output	0		150	ns
Receiver Timing (See Figure 7)					
t_{RXS}	RxD data setup time to RxC High	240			ns
t_{RXH}	RxD data hold time from RxC High	200			ns

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ORed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
7. Guaranteed by characterization of sample units.
8. Minimum frequencies are not tested but are guaranteed by design.
9. 325ns maximum for T_A > 70°C.

BLOCK DIAGRAM

The SCC2692 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCC2692 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4KHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

The 8-bit multipurpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SCC2692 is conditioned to transmit data when the transmitter is enabled through the command register. The SCC2692 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR.

If the transmitter is disabled, it continues operating until the character currently being trans-

mitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCC2692 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Table 1. SCC2692 Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Reserved	Reserved
1	1	0	1	Input Port (IPR)	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1X by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1X, switches the pointer to MR2X. The pointer then remains at MR2X, so that subsequent accesses are always to MR2X unless the pointer is reset to MR1X as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select
If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select
Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 causes OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	RxINT SELECT	ERROR MODE	PARITY MODE	PARITY TYPE	BITS PER CHARACTER
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE	TxRTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
	RECEIVER CLOCK SELECT	TRANSMITTER CLOCK SELECT
CSRA CSRB	See Text	See Text

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MISCELLANEOUS COMMANDS	DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
CRA CRB	See Text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1X) 11 = RxCB(1X)	11 = OPR[2] 01 = TxCA(16X) 10 = TxCA(1X) 11 = RxCA(1X)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP 3 INT	DELTA IP 2 INT	DELTA IP 1 INT	DELTA IP 0 INT
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP 3	DELTA IP 2	DELTA IP 1	DELTA IP 0	IP 3	IP 2	IP 1	IP 0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select

This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select

This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP3-16X	IP3-16X
1111	IP3-1X	IP3-1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

Table 3. Baud Rate

CSRA[7:4]	ACR[7] = 0	ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4K	19.2K
1101	Timer	Timer
1110	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select

This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	ACR[7] = 1
1110	IP6-16X	IP6-16X
1111	IP6-1X	IP6-1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select

This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP5-16X	IP5-16X
1111	IP5-1X	IP5-1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7:4] – Miscellaneous Commands

The encoded value of this field may be used to specify a single command as follows:

CRA[6:4] COMMAND

0000 No command.

0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.

0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Not used.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued

1101 Not used.

1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. The contents of all registers will be saved while in this mode. . It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only.

1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

CRA[3] – Disable Channel A Transmitter

This command terminates transmitter operation and resets the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter

Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver

This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver

Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of comamnds "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break

This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1:	50, 110, 134.5, 200, 300, 600, 1.05K, 1.2K, 2.4K, 4.8K, 7.2K, 9.6K, and 38.4K baud.
Set 2:	75, 110, 134.5, 150, 300, 600, 1.2K, 1.8K, 2.0K, 2.4K, 4.8K, 9.6K, and 19.2K baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16X CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE:
Duty cycle of 16X clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR 6:4 Field Definition

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1X clock of Channel A transmitter
010	Counter	TxCB – 1X clock of Channel B transmitter
011	Counter	Crystal or external clock (X1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be

asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3-A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

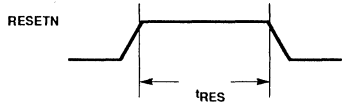


Figure 1. Reset Timing

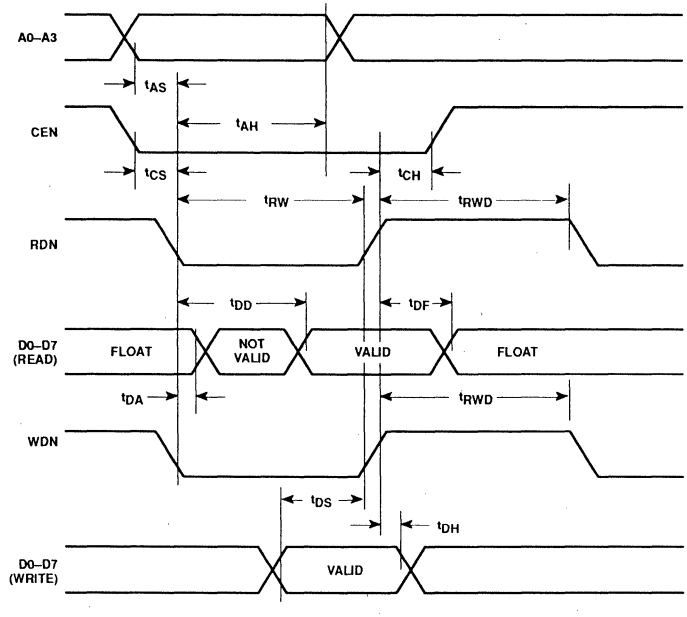


Figure 2. Bus Timing

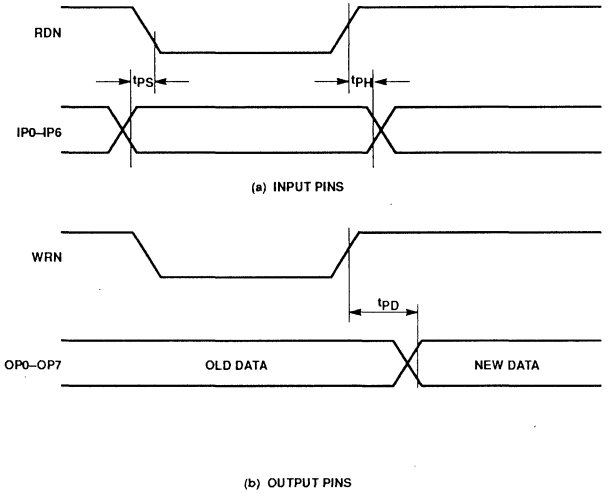
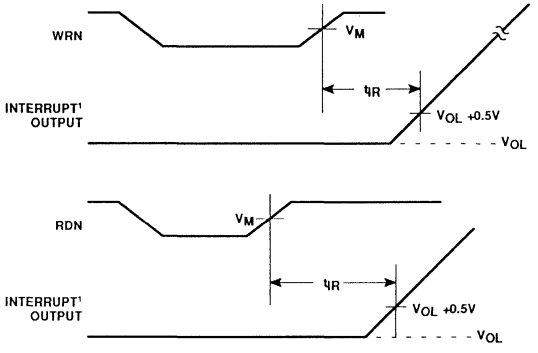
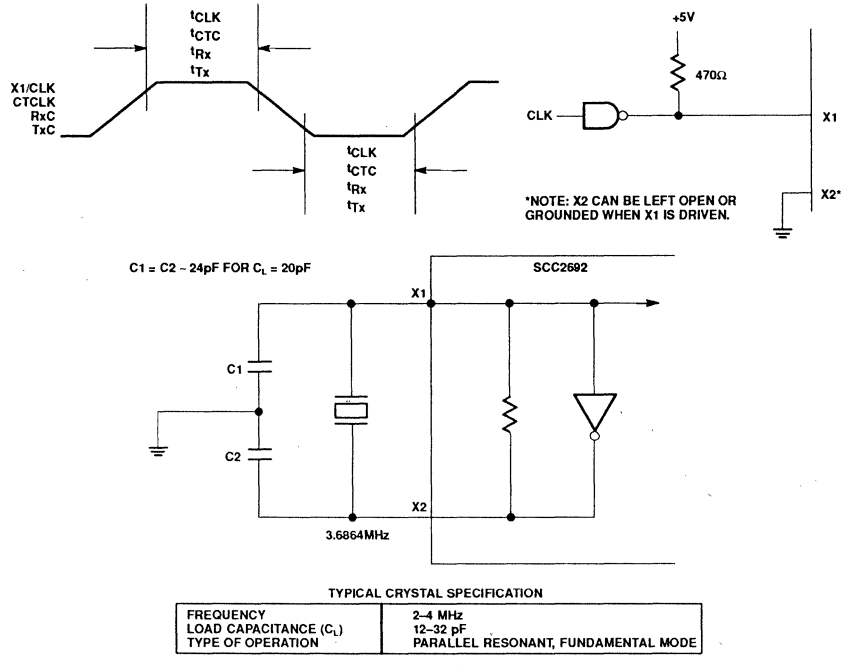


Figure 3. Port Timing



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing



TYPICAL CRYSTAL SPECIFICATION

FREQUENCY	2–4 MHz
LOAD CAPACITANCE (C_L)	12–32 pF
TYPE OF OPERATION	PARALLEL RESONANT, FUNDAMENTAL MODE

Figure 5. Clock Timing

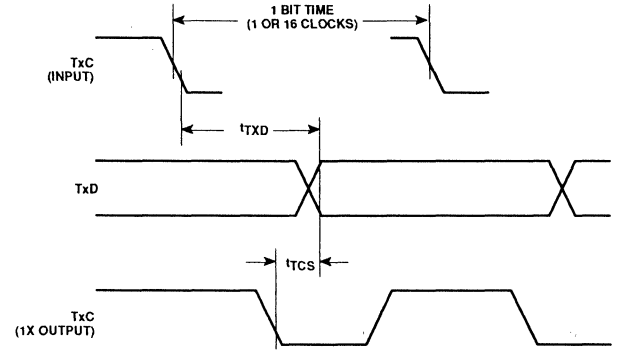


Figure 6. Transmitter External Clocks

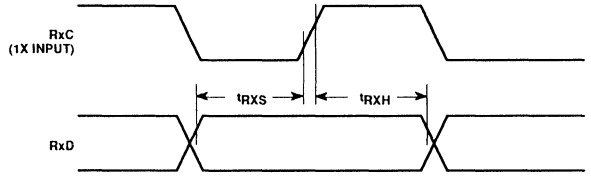
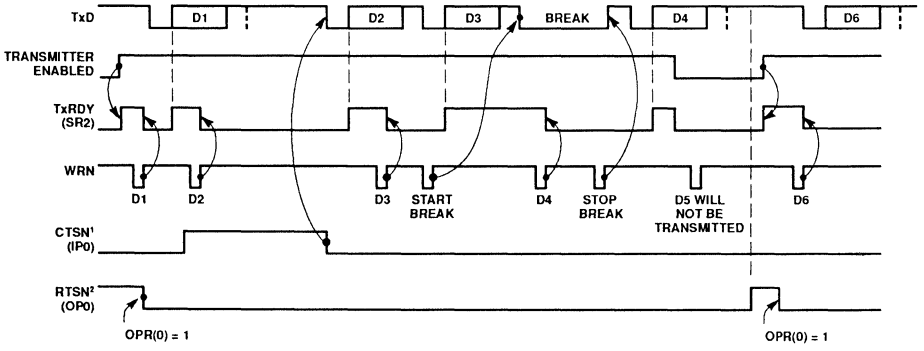
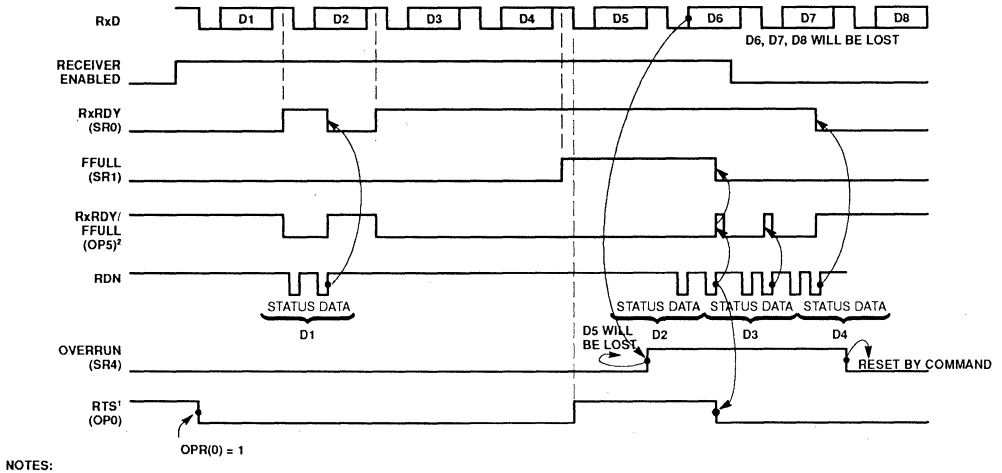


Figure 7. Receiver External Clock



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR(6) = 0.

Figure 9. Receiver Timing

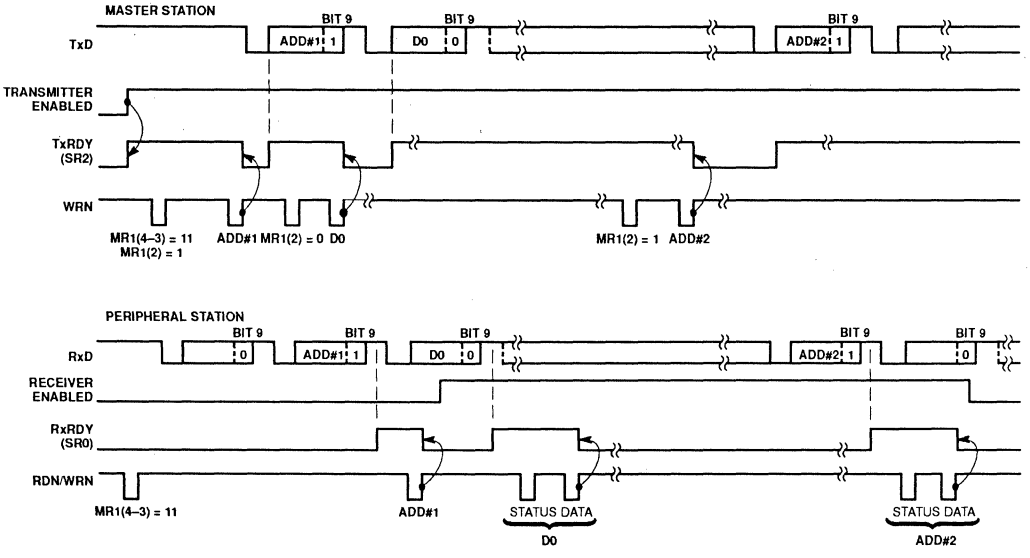


Figure 10. Wake-Up Mode

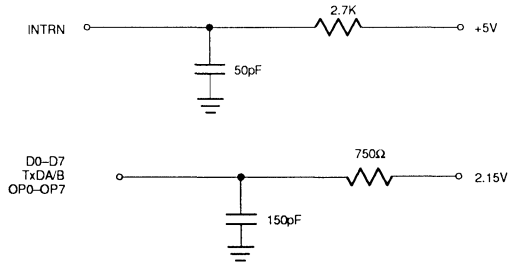


Figure 11. Test Conditions on Outputs

Philips Components–Signetics

Document No.	
ECN No.	
Date of Issue	November 12, 1990
Status	Preliminary Specification
Data Communication Products	

SC26C92

Dual asynchronous receiver/transmitter (DUART)

DESCRIPTION

The SC26C92 is a pin and function replacement for the 2692 with added features and deeper fifos. Its configuration on power up is that of the 2692. Its differences from the 2692 are: 8 character receiver, 8 character transmit fifos, receiver watch dog timer, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts.

The Signetics SC26C92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is buffered by eight character fifos to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC26C92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

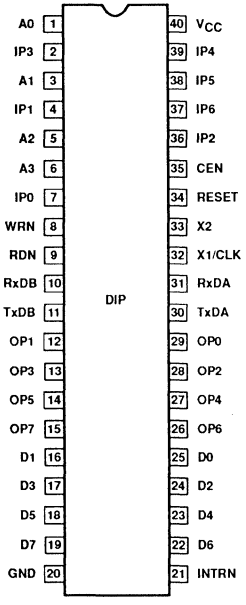
The SC26C92 is available in three package versions: 40-pin and 28-pin, 0.6" wide, DIPs and a 44-pin PLCC.

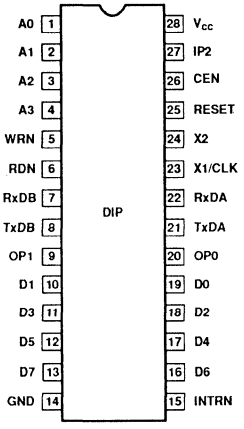
FEATURES

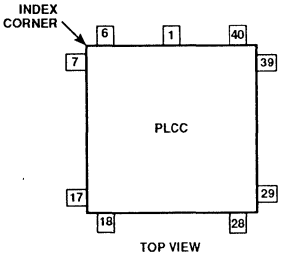
- Dual full-duplex independent asynchronous receiver/transmitters
- 8 character Fifos for each receiver and transmitter
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Other baud rates to 230.4k baud at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
  - Each fifo can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial, industrial and military temperature range versions
- TTL compatible
- Single +5V power supply

Dual asynchronous receiver/transmitter (DUART) SC26C92

PIN CONFIGURATIONS







TOP VIEW

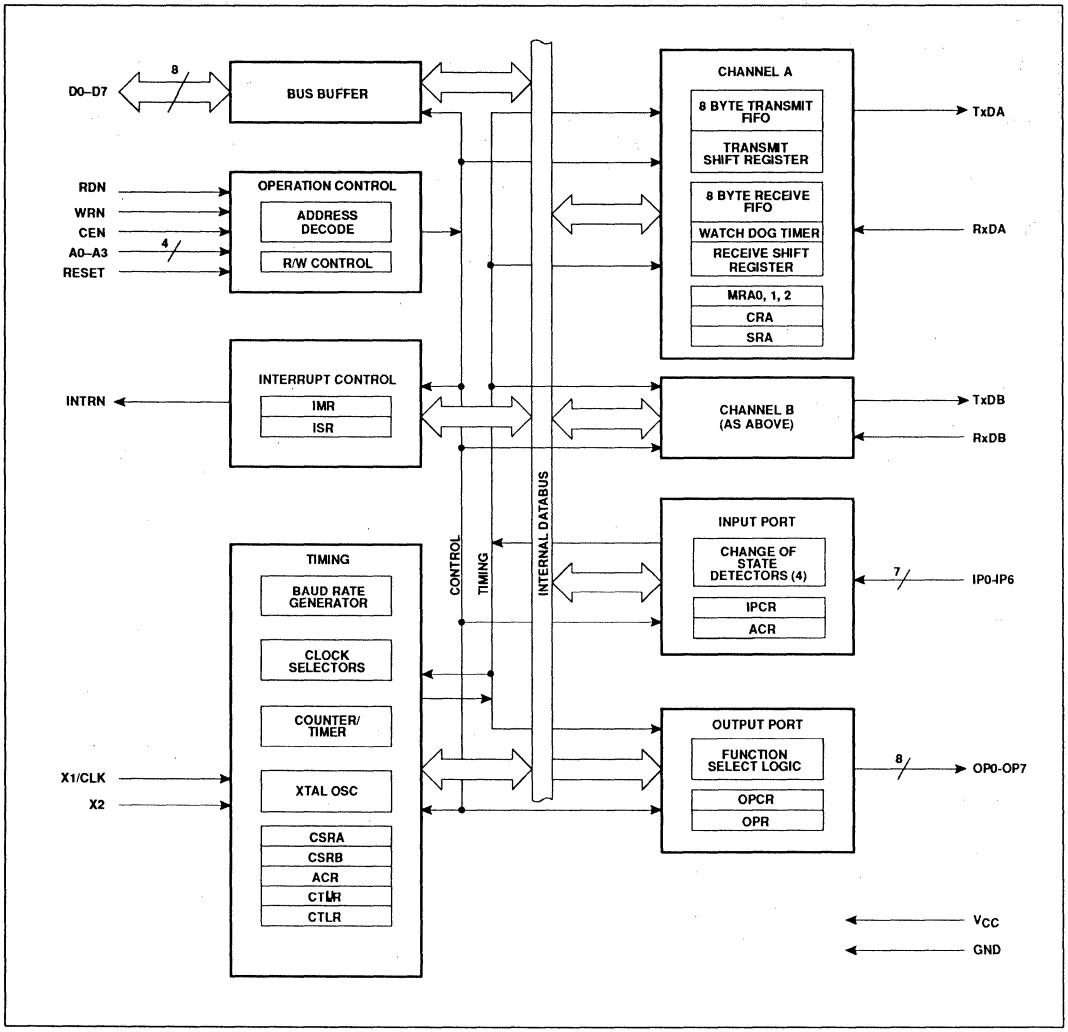
PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C
40-Pin Cerdip	SC26C92AC1F40	SC26C92AA1F40
28-Pin Cerdip	SC26C92AC1F28	SC26C92AA1F28
40-Pin Plastic DIP	SC26C92AC1N40	SC26C92AA1N40
28-Pin Plastic DIP	SC26C92AC1N28	SC26C92AA1N28
44-Pin Plastic LCC	SC26C92AC1A44	SC26C92AA1A44

Dual asynchronous receiver/transmitter (DUART) SC26C92

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	APPLICABLE		TYPE	NAME AND FUNCTION
	40,44	28		
D0-D7	X	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state.
INTRN	X	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	X	X	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). If X1/CLK is driven from an external source, this pin can be left open or connected to ground.
RxDA	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	X	X	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	X	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X		O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X		O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X		O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	X		O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	X		O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	X		O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYBN output.
IP0	X		I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	X		I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	X	X	I	**Input 2:** General purpose input or counter/timer external clock input.
IP3	X		I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.

PIN DESCRIPTION (Continued)

SYMBOL	APPLICABLE		TYPE	NAME AND FUNCTION
	40,44	28		
IP4	X		I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X		I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X		I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	I	**Power Supply:** +5V supply input.
GND	X	X	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	-0.5 to V_{CC} +0.5	V
P_D	Power dissipation[5]	750	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. Maximum power dissipation of the chip when outputs are loaded externally. For operating current, see DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)		2.0			V
V_{IH}	Input high voltage (X1/CLK)		0.8 V_{CC}			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = -400µA	V_{CC} -0.5			V
I_{IX1PD}	X1/CLK input current - power down	V_{IN} = 0 to V_{CC}	-10		+10	µA
I_{ILX1}	X1/CLK input low current - operating	V_{IN} = 0	-75		0	µA
I_{IHX1}	X1/CLK input high current - operating	V_{IN} = V_{CC}	0		75	µA
I_{OHX2}	X2 output high current - operating	V_{OUT} = V_{CC}, X1 = 0	0		+75	µA
I_{OHX2S}	X2 output high short circuit current - operating	V_{OUT} = 0, X1 = 0	-10		-1	mA
I_{OLX2}	X2 output low current - operating	V_{OUT} = 0, X1 = V_{CC}	-75		0	µA
I_{OLX2S}	X2 output low short circuit current - operating and power down	V_{OUT} = V_{CC}, X1 = V_{CC}	1		10	mA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	-10		+10	µA
	Input port pins	V_{IN} = 0 to V_{CC}	-20		+10	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			10	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0V	-10			µA
I_{ODL}	Open-drain output low current in off-state	V_{IN} = 0	-10			µA
I_{ODH}	Open-drain output high current in off-state	V_{IN} = V_{CC}			10	µA
	Power supply current[5]					
	Operating mode	TTL input levels			10	mA
I_{CC}		CMOS input levels			10	mA
	Power down mode	TTL input levels			3.0	mA
		CMOS input levels			TBD	µA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of V_{CC} -0.2V and V_{SS} + 0.2V.

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ[3]	Max	
Reset Timing (See Figure 1)					
t_{RES}	RESET pulse width	1.0			µs
Bus Timing[5] (See Figure 2)					
t_{AS}	A0-A3 setup time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 hold time from RDN, WRN Low	30			ns
t_{CS}	CEN setup time to RDN, WRN Low	0			ns
t_{CH}	CEN hold time from RDN, WRN High	0			ns
t_{RW}	WRN, RDN pulse width	110			ns
t_{DD}	Data valid after RDN Low				ns
t_{DA}	RDN Low to data bus active[7]			110	ns
t_{DF}	Data bus floating after RDN High			110	ns
t_{DI}	RDN High to data bus invalid[7]	20		45	ns
t_{DS}	Data setup time before WRN High	75			ns
t_{DH}	Data hold time after WRN High	0			ns
t_{RWD}	High time between reads and/or writes[5, 6]	55			ns

AC CHARACTERISTICS[1, 2, 4] (Continued)

SYMBOL	PARAMETER	LIMITS Min	Typ[3]	Max	UNIT
Port Timing[5] (See Figure 3)					
t_{PS}	Port input setup time before RDN Low	0			ns
t_{PH}	Port input hold time after RDN High	0			ns
t_{PD}	OP_n output valid from WRN High			110	ns
Interrupt Timing (See Figure 4)					
t_{IR}	INTRN (or OP3-OP7 when used as interrupts) negated from:				
	Read RHR (RxRDY/FFULL interrupt)			100	ns
	Write THR (TxRDY interrupt)			100	ns
	Reset command (break change interrupt)			100	ns
	Stop C/T command (counter interrupt)			100	ns
	Read IPCR (input port change interrupt)			100	ns
	Write IMR (clear of interrupt mask bit)			100	ns
Clock Timing (See Figure 5)					
t_{CLK}	X1/CLK High or Low time	80			ns
f_{CLK}	X1/CLK frequency	2	3.6864	4	MHz
t_{CTC}	CTCLK (IP2) High or Low time	60			ns
f_{CTC}	CTCLK (IP2) frequency[8]	0		8	MHz
t_{RX}	RxC High or Low time	220			ns
f_{RX}	RxC frequency (16X)[8]	0		2	MHz
	(1X)[8, 9]	0		1	MHz
t_{TX}	TxC High or Low time	220			ns
f_{TX}	TxC frequency (16X)[8]	0		2	MHz
	(1X)[8, 9]	0		1	MHz
Transmitter Timing (See Figure 6)					
t_{TXD}	TxD output delay from TxC Low			120	ns
t_{TCS}	Output delay from TxC Low to TxD data output	0		50	ns
Receiver Timing (See Figure 7)					
t_{RXS}	RxD data setup time to RxC High	100			ns
t_{RXH}	RxD data hold time from RxC High	100			ns

NOTES:

1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ORed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
7. Guaranteed by characterization of sample units.
8. Minimum frequencies are not tested but are guaranteed by design.
9. Clocks for 1X mode should be symetrical.

Dual asynchronous receiver/transmitter (DUART) SC26C92

BLOCK DIAGRAM

The SC26C92 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

When OP3 to OP7 are programmed as interrupts, their output buffers are changed to the open drain active low configuration.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Programming bit 0 of MR0 to a "1" gives additional baud rates of 57.6kB, 115.2kB and 230.4kB. These will be in the 16X mode. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SC26C92 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU via the receive FIFO. Three status bits (Break, Framing and Parity Errors) are also FIFOed with each data character.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4KHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

This 8-bit output port is a general purpose output and is controlled by the OPR and the OPCR registers. The OPR register is set and reset by writing to the SOPR and ROPR addresses. (See the description of the SOPR and ROPR registers). The output pins will drive the inverse data polarity of the OPR registers. The OPCR register conditions these output to be controlled by the OPR or by other signals in the chip.

OPERATION

Transmitter

The SC26C92 is conditioned to transmit data when the transmitter is enabled through the command register. The SC26C92 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When the transmitter is initially enabled the TxRDY and TxEMPTY bits will be set in the status register. When a character is loaded to the transmit fifo the TxEMPTY bit will be reset. The TxEMPTY will not set until: 1) the transmit fifo is empty and the transmit shift register has finished transmitting the stop bit of the last character written to the transmit fifo, or 2) the transmitter is disabled and then re-enabled. The TxRDY bit is set whenever the transmitter is enabled and the TxFIFO is not full. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in

the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SC26C92 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of eight characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all eight stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Timeout Mode

In addition to the watch dog timer described in the receiver section, the counter/timer may be used for a similar function. Its programmability, of course, allows much greater precision of time out intervals.

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will gen-

erate an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Each channel has 3 more registers (MR0, 1, 2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0 or 1 by MR control commands in the command register "Miscellaneous Commands". Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0 or 1 via the miscellaneous commands of the command register. The pointer is set to 1 on reset for compatibility with the SC26C92.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'OA' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. SC26C92 Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Reserved	Reserved
1	1	0	1	Input Port (IPR)	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

NOTE:
The three MR Registers are accessed via the MR Pointer and Commands lxh and dxh. (Where "x" represents receiver and transmitter enable/disable control)

The following named registers are the same for Channels A and B.			
Mode Register	MRnA	MRnB	R/W
Status Register	SRA	SRB	R only
Clock Select	CSRA	CSRB	W only
Command Register	CRA	CRB	W only
Receiver Fifo	RHRA	RHRB	R only
Transmitter Fifo	THRA	THRB	W only

These registers control the functions which service both Channels.		
Input Port Change Register	IPCR	R
Auxillary Control Register	ACR	W
Interrupt Status Register	ISR	R
Interrupt Mask Register	IMR	W
Counter Timer Upper Value	CTU	R
Counter Timer Lower Value	CTL	R
Counter Timer Preset Upper	CRUR	W
Counter Timer Preset Lower	CRLR	W
Input Port Register	IPR	R
Output Configuration Register	OPCR	W
Set Output Port Bits	SOPR	W
Reset Output Port Bits	ROPR	W

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR0A MR0B	Rx WATCH DOG 0 = Disable 1 = Enable	RxINT (2)	TxINT (1:0)	DON'T CARE Set to 0	TEST 1 Set to 0	TEST 2 Set to 0	BAUD RATE EXTEND 0 = Normal 1 = Extend

NOTE:
MR0B[3:0] are not implemented. When writing to MR0B set them to 0. A read of MR0B[3:0] returns 1111.

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
MR1A MR1B	Rx CONTROLS RTS 0 = No 1 = Yes	Rx INT BIT 1 0 = RxRDY 1 = FFULL	ERROR MODE 0 = Char 1 = Block	PARITY MODE 00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	PARITY TYPE 0 = Even 1 = Odd	BITS PER CHARACTER 00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE	Tx CONTROLS RTS	CTS ENABLE Tx	STOP BIT LENGTH*			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
	RECEIVER CLOCK SELECT	TRANSMITTER CLOCK SELECT
CSRA CSRB	See Text	See Text

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MISCELLANEOUS COMMANDS	DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
CRA CRB	See Text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1X) 11 = RxCB(1X)	11 = OPR[2] 01 = TxCA(16X) 10 = TxCA(1X) 11 = RxCA(1X)

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SOPR	0 = No Change 1 = Set							

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ROPR	0 = No Change 1 = Reset							

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE			DELTA IP 3 INT	DELTA IP 2 INT	DELTA IP 1 INT	DELTA IP 0 INT
ACR	0 = set 1 1 = set 2	See Table 4			0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP 3	DELTA IP 2	DELTA IP 1	DELTA IP 0	IP 3	IP 2	IP 1	IP 0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

REGISTER DESCRIPTIONS

Mode Registers

MR0 is accessed by setting the MR pointer to 0 via the command register command D.

MR0A

MR0[7] – This bit controls the receiver watch dog timer. 0 = disable, 1 = able. When enabled, the watch dog timer will generate a receiver interrupt if the receiver FIFO has not been accessed within 64 bit times of the receiver 1X clock. This is used to alert the control processor that data is in the RHR that has not been read. This situation may occur when the last part of a message is not large enough to generate an interrupt.

MR0[6] – Bit 2 of receiver FIFO interrupt level. This bit along with Bit 6 of MR1 sets the fill level of the 8 byte FIFO that generates the receiver interrupt.

MR0[6]	MR1[6]	Interrupt Condition
0	0	1 or more bytes in FIFO (Rx RDY)
0	1	3 or more bytes in FIFO
1	0	6 or more bytes in FIFO
1	1	8 or more bytes in FIFO (Rx FULL)

MR0[5:4] – Tx interrupt fill level.

MR0[5]	MR0[4]	Interrupt Condition
0	0	8 bytes empty (Tx EMPTY)
0	1	4 or more bytes empty
1	0	6 or more bytes empty
1	1	1 or more bytes empty (Tx RDY)

MR0[3] – Not used. Should be set to 0.

MR0[2:1] – Test 1 and Test 2. Used for factory test. Set to 0

MR0[0] – Baud rate extend. 0 = Normal baud rates. 1 = Extend baud rate. 57.6kB, 115.2kB, 230.4kB.

Note: MR0[3:0] are not used in channel B. They should be set to 0.

MR1A

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CR command 1. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1[6] – Bit 1 of the receiver interrupt control. See description under MR0[6].

MR1A[5] – Channel A Error Mode Select

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR0B – Channel B Mode Register 1

MR0B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR0 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR0B, the pointer will point to MR1B.

The bit definitions for this register are identical to MR0A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP3-16X	IP3-16X
1111	IP3-1X	IP3-1X

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

Table 3. Baud Rate

CSRA[7:4]	MR0[0] = 0		MR0[0] = 1	
	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	50	450
0001	110	110	110	110
0010	134.5	134.5	134.5	230.4K
0011	200	150	200	900
0100	300	300	1800	1800
0101	600	600	3600	3600
0110	1,200	1,200	7200	7,200
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	14.4K	14.4K
1001	4,800	4,800	28.8K	28.8K
1010	7,200	1,800	7,200	1,800
1011	9,600	9,600	57.6K	57.6K
1100	38.4K	19.2K	230.4K	115.2K
1101	Timer	Timer	Timer	Timer
1110	IP4-16X	IP4-16X	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X	IP4-1X	IP4-1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select

This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	ACR[7] = 1
1110	IP6-16X	IP6-16X
1111	IP6-1X	IP6-1X

The transmitter clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select

This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:4]	ACR[7] = 0	ACR[7] = 1
1110	IP5-16X	IP5-16X
1111	IP5-1X	IP5-1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7:4] – Miscellaneous Commands

The encoded value of this field may be used to specify a single command as follows:

CRA[6:4] COMMAND

0000 No command.

0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.

0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Not used.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued

1101 Set MR pointer to "0".

1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. The contents of all registers will be saved while in this mode. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only.

1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

CRA[3] – Disable Channel A Transmitter

This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of comamnds "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled or reset.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the transmit FIFO is not full and ready to be loaded with another character. This bit is cleared when the transmit FIFO is loaded by the CPU and there are (after this load) no more empty locations in the FIFO. It is set when a character is transferred to the transmit shift register. TxRDYA is reset when the transmitter is disabled and is set when the transmitter is first enabled, VIZ., characters loaded into the transmit FIFO while the transmitter is disabled or reset will not be transmitted. This bit has different meaning from ISR0.0

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the receive FIFO. If a character is waiting in the receive shift register because the FIFO is full, FFULLA will not be reset when the CPU reads the receive FIFO. This bit has different meaning from ISR1 when MR1 6 is programmed to a '1'.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receive FIFO, only if (after this read) there are no more characters in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter

mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.

- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:

- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

SOPR – Set the Output Port Bits (OPR)

SOPR[7:0] – Ones in the byte written to this register will cause the corresponding bit positions in the OPR to set to 1. Zeros have no effect.

ROPR – Reset Output Port Bits (OPR)

ROPR[7:0] – Ones in the byte written to the ROPR will cause the corresponding bit positions in the OPR to set to 0. Zeros have no effect.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05K, 1.2K, 2.4K, 4.8K, 7.2K, 9.6K, and 38.4K baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2K, 1.8K, 2.0K, 2.4K, 4.8K, 9.6K, and 19.2K baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16X CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE:
Duty cycle of 16X clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR 6:4 Field Definition

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1X clock of Channel A transmitter
010	Counter	TxCB – 1X clock of Channel B transmitter
011	Counter	Crystal or external clock (X1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Rx RDY/FULL
This bit indicates that the channel B receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

ISR[4] – Tx RDY/FULL
This bit indicates that the channel B transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has

a different meaning than the Tx RDY bit in the status register.

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Rx RDY/FULL
This bit indicates that the channel A receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

ISR[0] – Tx RDY/FULL
This bit indicates that the channel A transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3-A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

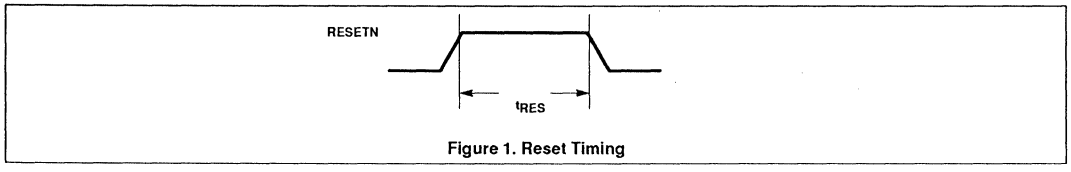


Figure 1. Reset Timing

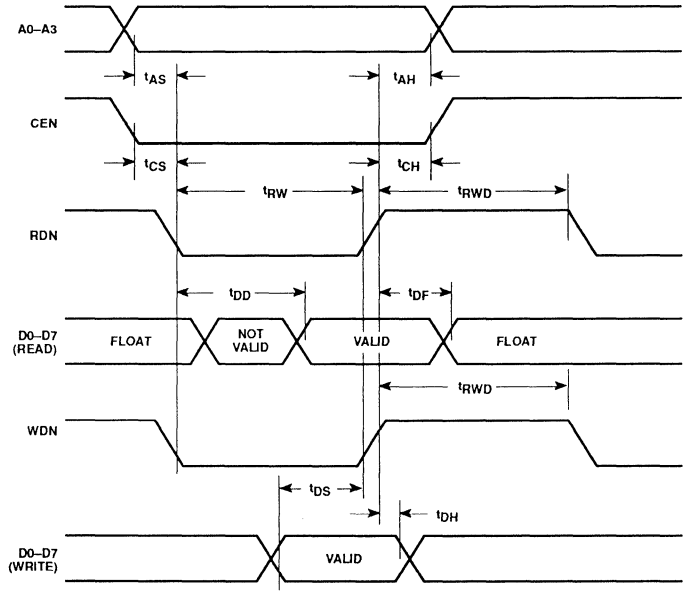


Figure 2. Bus Timing

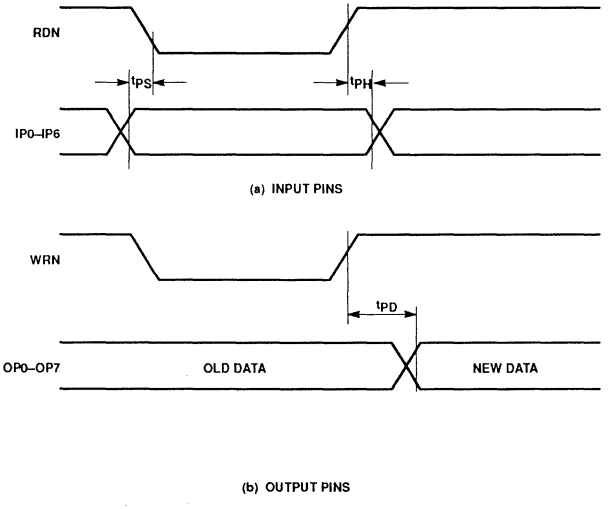
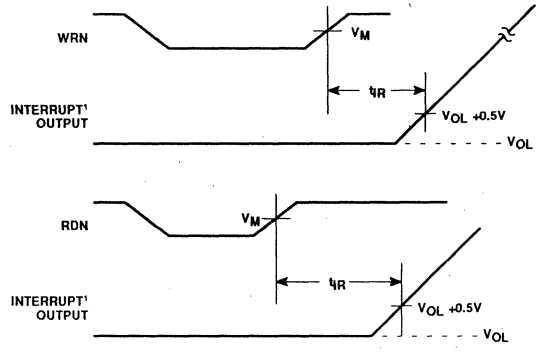
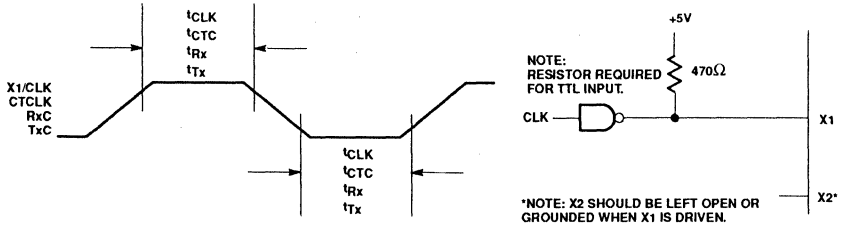


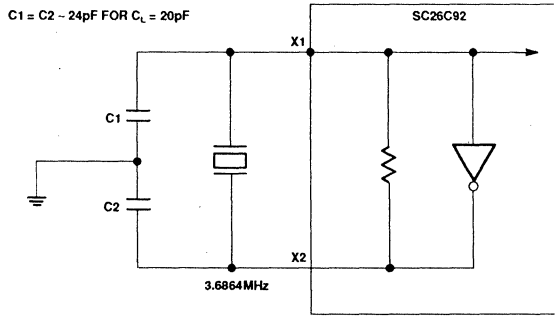
Figure 3. Port Timing



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing





TYPICAL CRYSTAL SPECIFICATION

FREQUENCY	2–4 MHz
LOAD CAPACITANCE (C_L)	12–32 pF
TYPE OF OPERATION	PARALLEL RESONANT, FUNDAMENTAL MODE

Figure 5. Clock Timing

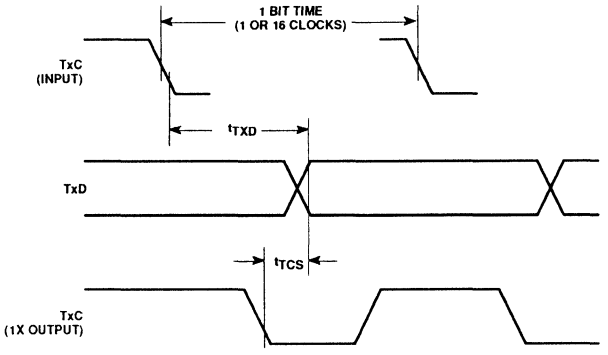


Figure 6. Transmitter External Clocks

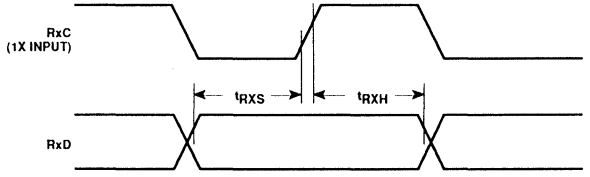
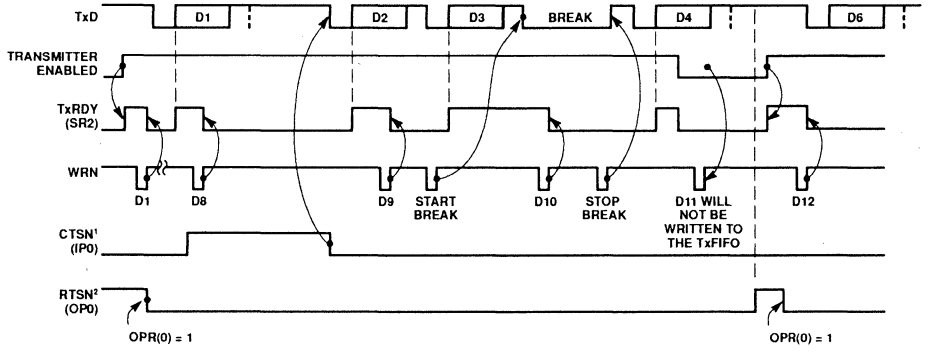
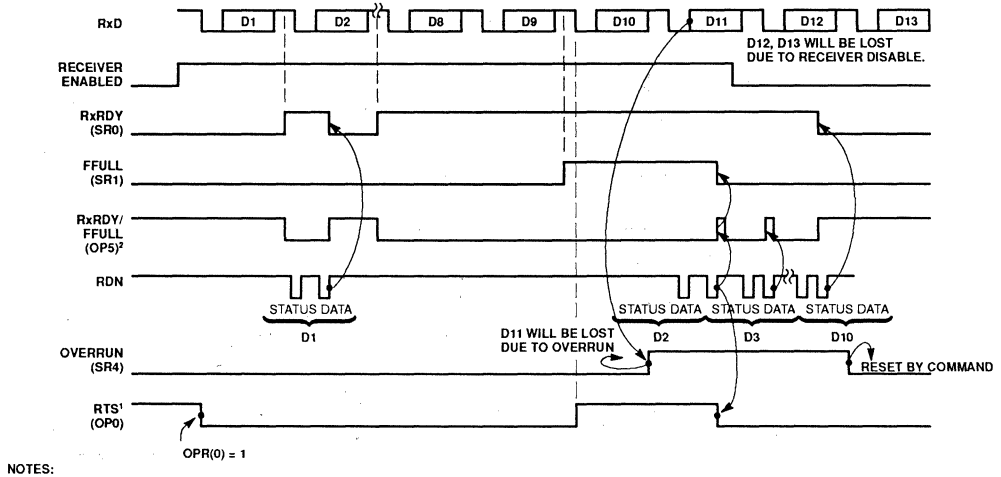


Figure 7. Receiver External Clock



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR(6) = 0.

Figure 9. Receiver Timing

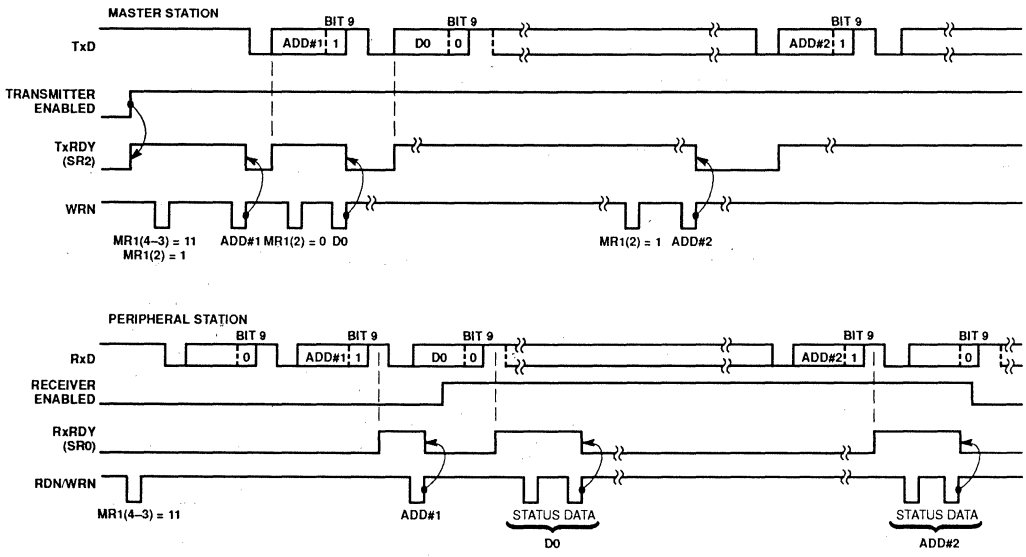


Figure 10. Wake-Up Mode

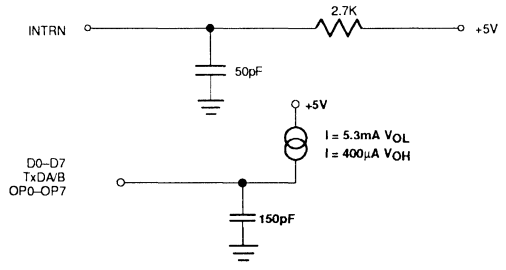


Figure 11. Test Conditions on Outputs

Philips Components–Signetics

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Date of Issue	November 5, 1990
Status	Product Specification
Data Communication Products	

SCC68692
Dual asynchronous receiver/transmitter (DUART)

DESCRIPTION

The Signetics SCC68692 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices and can also interface easily with other microprocessors. The DUART can be used in a polled or interrupt driven systems.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

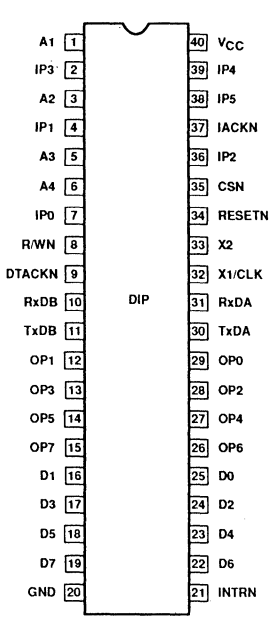
Also provided on the SCC68692 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

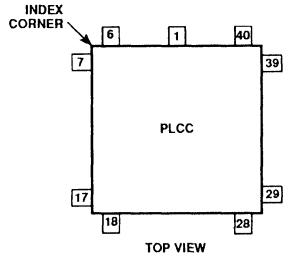
FEATURES

- S68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function 6-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Interrupt vector output on interrupt acknowledge
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial and Industrial temperature range versions
- TTL compatible
- Single +5V power supply

Dual asynchronous receiver/transmitter (DUART) SCC68692

PIN CONFIGURATIONS





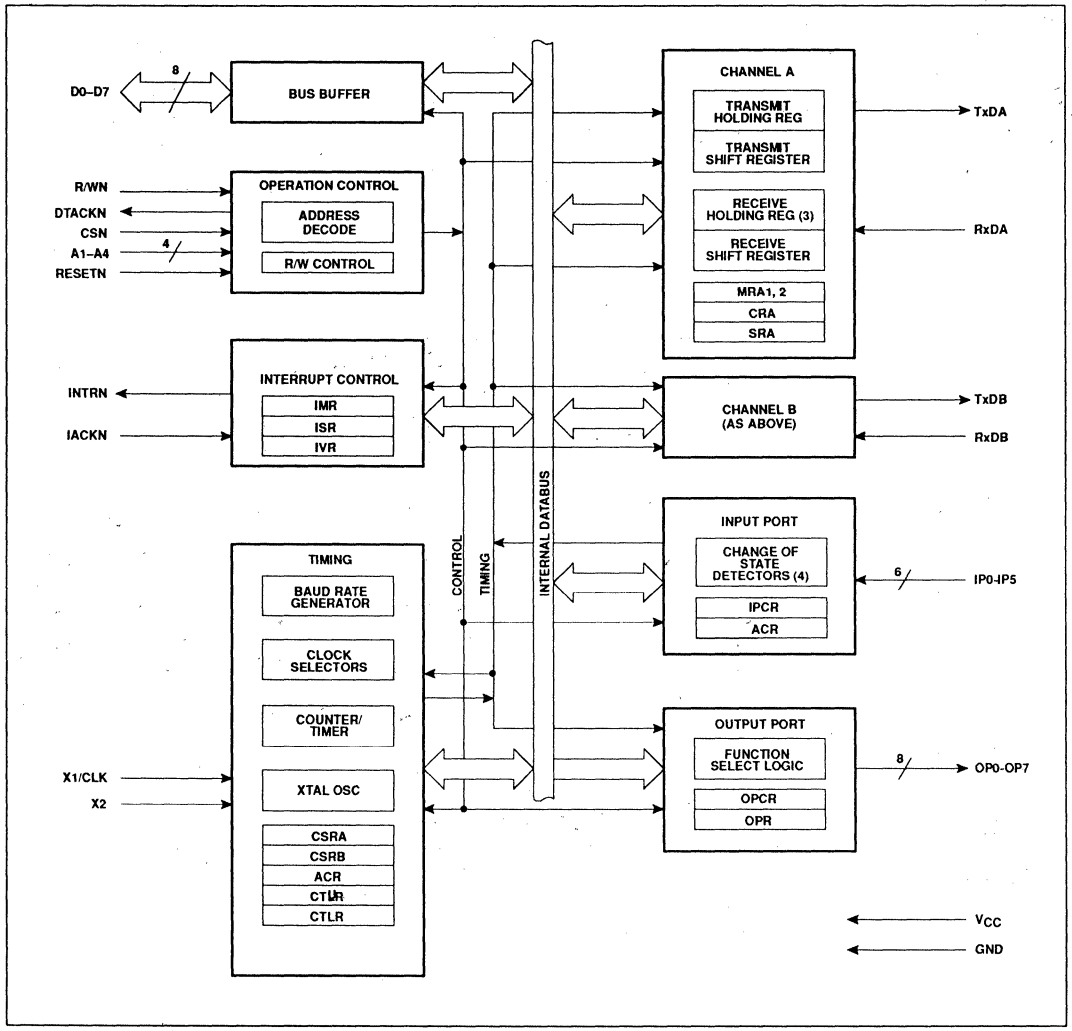
TOP VIEW

PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A1	24	INTRN
3	IP3	25	D6
4	A2	26	D4
5	IP1	27	D2
6	A3	28	D0
7	A4	29	OP6
8	IP0	30	OP4
9	R/WN	31	OP2
10	DTACKN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CSN
18	D1	40	IP2
19	D3	41	IACKN
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C
40-Pin Cerdip	SCC68692C1F40	SCC68692E1F40
40-Pin Plastic DIP	SCC68692C1N40	SCC68692E1N40
44-Pin Plastic LCC	SCC68692C1A44	SCC68692E1A44

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NO.	TYPE	NAME AND FUNCTION
D0–D7	25,16,24,17 23,18,22,19	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	35	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A1–A4 inputs. When CEN is High, the DUART places the D0–D7 lines in the 3-State condition.
R/WN	8	I	**Read/Write:** A High input indicates a read cycle and a low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1–A4	1,2,5,6	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	34	I	**Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state.
DTACKN	9	O	**Data Transfer Acknowledge:** 3-State active-Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	21	O	**Interrupt Request:** Active-Low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	37	I	**Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	32	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	33	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin can be left open.
RxDA	31	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	10	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	30	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	11	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	29	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	12	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	28	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	13	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	27	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	14	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	26	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	15	O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYBN output.
IP0	7	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	4	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	36	I	**Input 2:** General purpose input or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP3	2	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	39	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	38	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	40	I	**Power Supply:** +5V supply input.
GND	20	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation	750	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[6]		2.0			V
V_{IH}	Input high voltage (except X1/CLK)[7]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		0.8V_{CC}			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = –400µA	V_{CC} –0.5			V
I_{IX1PD}	X1/CLK input current – power down	V_{IN} = 0 to V_{CC}	–10		+10	µA
I_{ILX1}	X1/CLK input low current – operating	V_{IN} = 0	–75		0	µA
I_{IHX1}	X1/CLK input high current – operating	V_{IN} = V_{CC}	0		75	µA
I_{OHX2}	X2 output high current – operating	V_{OUT} = V_{CC}, X1 = 0	0		+75	µA
I_{OHX2S}	X2 output high short circuit current – operating	V_{OUT} = 0, X1 = 0	–10		–1	mA
I_{OLX2}	X2 output low current – operating	V_{OUT} = 0, X1 = V_{CC}	–75		0	µA
I_{OLX2S}	X2 output low short circuit current – operating and power down	V_{OUT} = V_{CC}, X1 = V_{CC}	1		10	mA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	–10		+10	µA
	Input port pins	V_{IN} = 0 to V_{CC}	–20		+10	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			10	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0V	–10			µA
I_{ODL}	Open-drain output low current in off State	V_{IN} = 0	–10			µA
I_{ODH}	Open-drain output high current in off State	V_{IN} = V_{CC}			10	µA
I_{CC}	Power supply current[5]					
	Operating mode	TTL input levels			10	mA
		CMOS input levels			10	mA
	Power down mode	TTL input levels			3.0	mA
		CMOS input levels			2.0	mA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of V_{CC} –0.2V and V_{SS} + 0.2V.
6. $T_A \geq 0°C$
7. $T_A < 0°C$

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	FIGURE	PARAMETER	LIMITS Min	LIMITS Typ[3]	LIMITS Max	UNIT
Reset Timing						
t_{RES}	1	RESET pulse width	1.0			µs
Bus Timing[5]						
t_{AS}	2,3,4	A1–A4 setup time to CSN Low	10			ns
t_{AH}	2,3,4	A1–A4 hold time from CSN Low	100			ns
t_{RWS}	2,3,4	RWN setup time to CSN High	0			ns
t_{RWH}	2,3,4	RWN holdup time to CSN High	0			ns
t_{CSW}[8]	2,3,4	CSN High pulse width	160			ns
t_{CSD}[9]	2,3,4	CSN or IACKN High from DTACKN Low	20			ns
t_{DD}	2,3,4	Data valid from CSN or IACKN Low			175	ns
t_{DA}	2	RDN Low to data bus active[8]	15			ns
t_{DF}	2,3,4	Data bus floating from CSN or IACKN High[8]			125	ns
t_{DI}	2	RDN High to data bus invalid[8]	20			ns
t_{DS}	2,3,4	Data setup time to CLK High	100			ns
t_{DH}	2,3,4	Data hold time from CSN High	0			ns
t_{DAL}	2,3,4	DTACKN Low from read data valid	0			ns
t_{DCR}	2,3,4	DTACKN Low (read cycle) from CLK High			125	ns
t_{DCW}	2,3,4	DTACKN Low (write cycle) form CLK High			125	ns
t_{DAH}	2,3,4	DTACKN High from CSN or IACKN High			100	ns
I_{DAT}[7]	2,3,4	DTACKN High impedance from CSN or IACKN High			125	ns
t_{CSC}[7]	2,3,4	CSN or IACKN setup time to clock High	90			ns
Port Timing[5]						
t_{PS}	5	Port input setup time to CSN Low	0			ns
t_{PH}	5	Port input hold time from CSN High	0			ns
t_{PD}	5	Port output valid from CSN High			400	ns
Interrupt Timing						
t_{IR}	6	INTRN (or OP3–OP7 when used as interrupts) negated from:				
		Read RHR (RxRDY/FFULL interrupt)			300[10]	ns
		Write THR (TxRDY interrupt)			300[10]	ns
		Reset command (break interrupt)			300[10]	ns
		Stop C/T command (counter interrupt)			300[10]	ns
		Read IPCR (input port change interrupt)			300[10]	ns
		Write IMR (clear of interrupt mask bit)			300[10]	ns
Clock Timing						
t_{CLK}	7	X1/CLK High or Low time	100			ns
f_{CLK}	7	X1/CLK frequency	2	3.6864	4	MHz
t_{CTC}	7	CTCLK (IP2) High or Low time	100			ns
f_{CTC}	7	CTCLK (IP2) frequency[9]	100		4	MHz
t_{RX}	7	RxC High or Low time	220			ns
f_{RX}	7	RxC frequency (16X)[9]	100		2	MHz
		(1X)[9]	100		1	MHz
t_{TX}	7	TxC High or Low time	220			ns
f_{TX}	7	TxC frequency (16X)[9]	0		2	MHz
		(1X)[9]	0		1	MHz
Transmitter Timing						
t_{TXD}	8	TxD output delay from TxC Low			350	ns
t_{TCS}	8	Output delay from TxC Low to TxD data output			150	ns
Receiver Timing						
t_{RXS}	9	RxD data setup time to RxC High	240			ns
t_{RXH}	9	RxD data hold time from RxC High	200			ns

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
6. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
7. This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.
8. Guaranteed by characterization of sample units.
9. Minimum frequencies are not tested but are guaranteed by design.
10. 325ns maximum for T_A > 70°C.

BLOCK DIAGRAM

The SCC68692 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR), the Auxiliary Control Register (ACR), and the Interrupt Vector Register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR register on the data bus and asserting DTACKN.

Outputs OP3–OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCC68692 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 6-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always be read as a logic 1 and D6 will reflect the level of IACKN. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 – 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a

true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

The 8-bit multipurpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also be individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SCC68692 is conditioned to transmit data when the transmitter is enabled through the command register. The SCC68692 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCC68692 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7–1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No addi-

tional characters can be received until the receiver is enabled again.

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Reserved	Interrupt Vector Register (IVR)
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.

3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been retransmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	**RxINT SELECT**	**ERROR MODE**	**PARITY MODE**	**PARITY TYPE**	**BITS PER CHARACTER**
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE	**TxRTS CONTROL**	**CTS ENABLE Tx**	**STOP BIT LENGTH***			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVER CLOCK SELECT				**TRANSMITTER CLOCK SELECT**			
CSRA CSRB	See Text				See Text			

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MISCELLANEOUS COMMANDS				**DISABLE Tx**	**ENABLE Tx**	**DISABLE Rx**	**ENABLE Rx**
CRA CRB	See Text				0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	**FRAMING ERROR***	**PARITY ERROR***	**OVERRUN ERROR**	**TxEMT**	**TxRDY**	**FFULL**	**RxRDY**
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	11 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INT
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]
IVR								

MR2A[4] – Channel A Clear-to-Send Control

If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

MR2A[3:0] – Channel A Stop Bit Length Select

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select

This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select

This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3–16X	IP3–16X
1111	IP3–1X	IP3–1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

Table 3. Baud Rate

CSRA[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4k	19.2k
1101	Timer	Timer
1110	IP4–16X	IP4–16X
1111	IP4–1X	IP4–1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select

This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP6–16X	IP6–16X
1111	IP6–1X	IP6–1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select

This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5–16X	IP5–16X
1111	IP5–1X	IP5–1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7:4] – Miscellaneous Commands

The encoded value of this field may be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.

0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Not used.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the

timeout mode, a 'Stop Counter' command should be issued

1101 Not used.

1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only. Design Note: The part will not output DTACKN while in power down mode. Use automatic DTACKN generation.

1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of comamnds "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In the special multidrop mode, the parity error bit stores the received A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL BAUD RATE	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	–0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	–0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

NOTE:
Duty cycle of 16x clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR [6:4] Field Definition

[6:4]	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or external clock (x1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

IVR – Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.

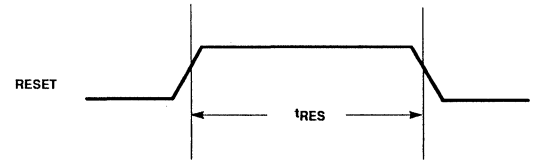


Figure 1. Reset Timing

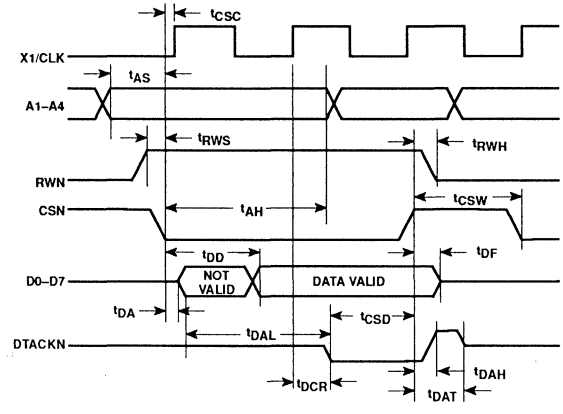


Figure 2. Bus Timing (Read Cycle)

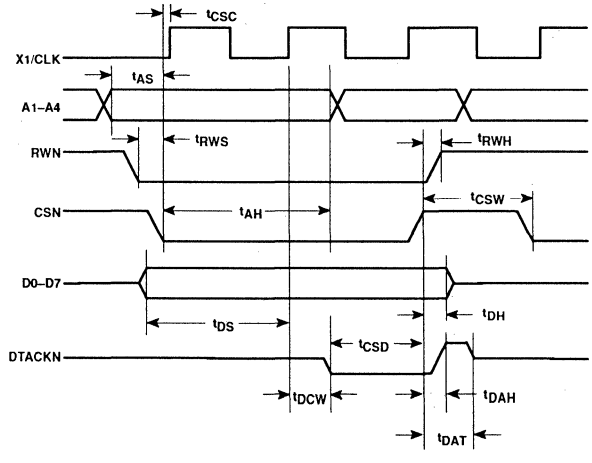


Figure 3. Bus Timing (Write Cycle)

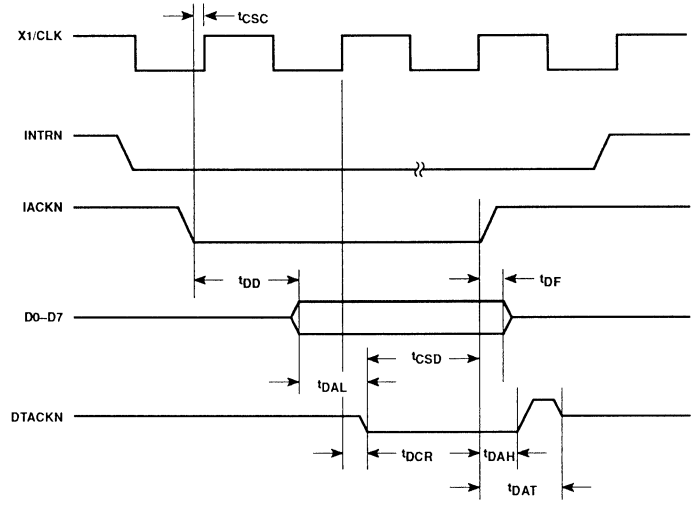


Figure 4. Interrupt Cycle Timing

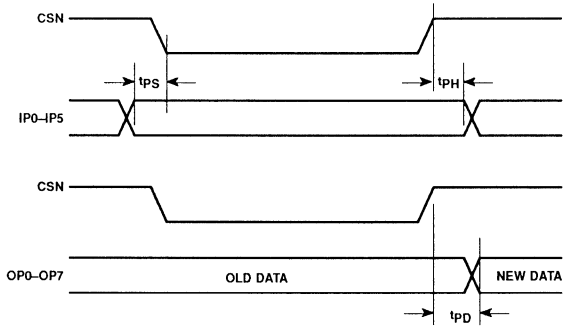
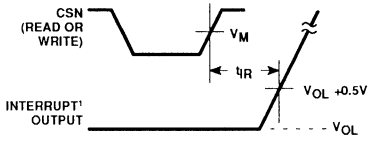


Figure 5. Port Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from themidpoint of the switching signal, V_M, to a point 0.5 volts above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 6. Interrupt Timing

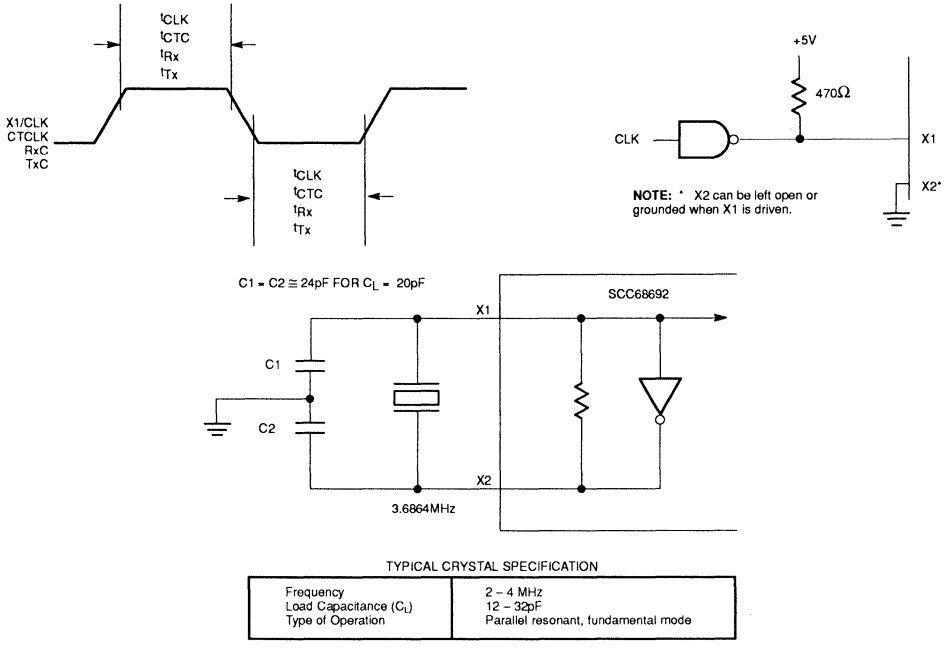


Figure 7. Clock Timing

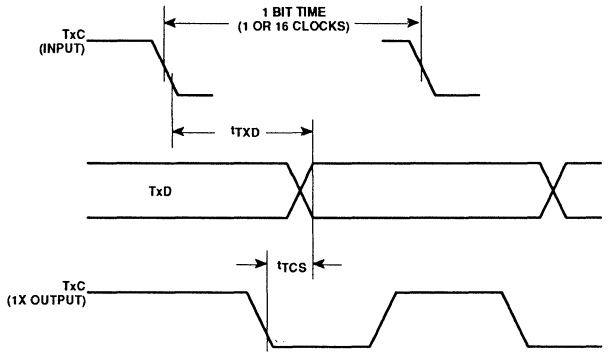


Figure 8. Transmit Timing

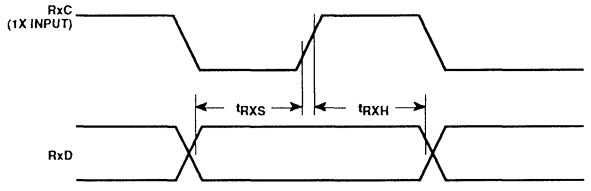
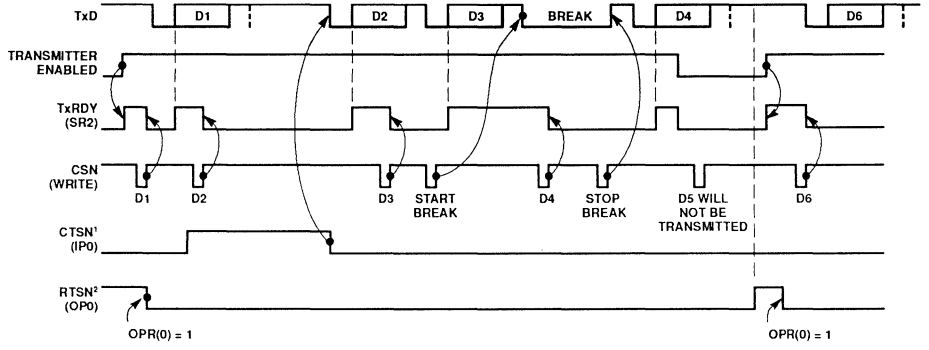
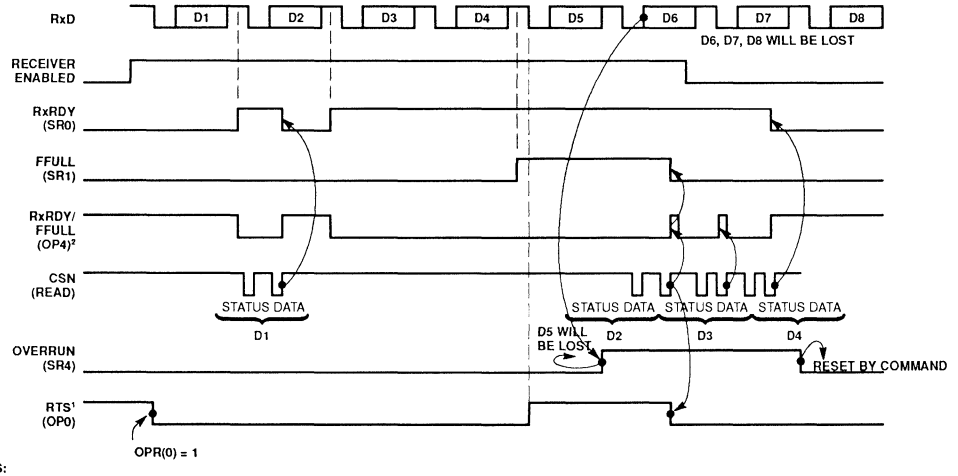


Figure 9. Receive Timing



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 10. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) and MR1(6) = 0.

Figure 11. Receiver Timing

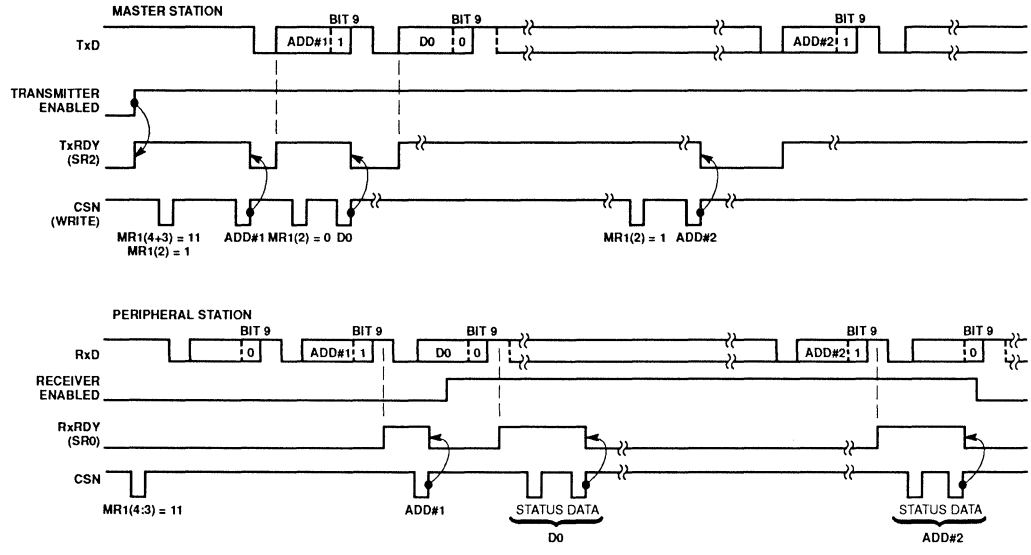


Figure 12. Wake-Up Mode

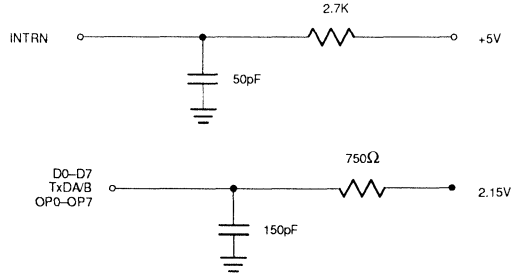


Figure 13. Test Conditions on Outputs

Philips Components–Signetics

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Data Communication Products	

SC68C92

Dual asynchronous receiver/transmitter (DUART)

DESCRIPTION

The SC68C92 is a pin and function replacement for the SCC68692 with added features and deeper fifos. Its configuration on power up is that of the SCC68692. Its differences from the SCC68692 are: 8 character receiver, 8 character transmit fifos, receiver watch dog timer, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts.

The Signetics SC68C92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is buffered by eight character fifos to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC68C92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

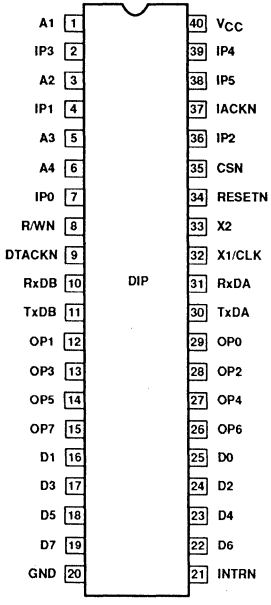
The SC68C92 is available in three package versions: 40-pin and 28-pin, 0.6" wide, DIPs and a 44-pin PLCC.

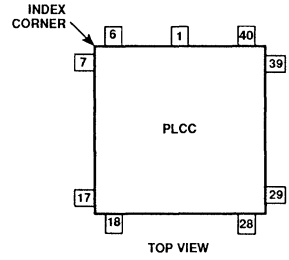
FEATURES

- S6800 bus compatible
- Dual full-duplex independent asynchronous receiver/transmitters
- 8 character fifos for each receiver and transmitter
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Other baud rates to 230.4k baud at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
  - Each fifo can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial, industrial and military temperature range versions
- TTL compatible
- Single +5V power supply

Dual asynchronous receiver/transmitter (DUART) SC68C92

PIN CONFIGURATIONS





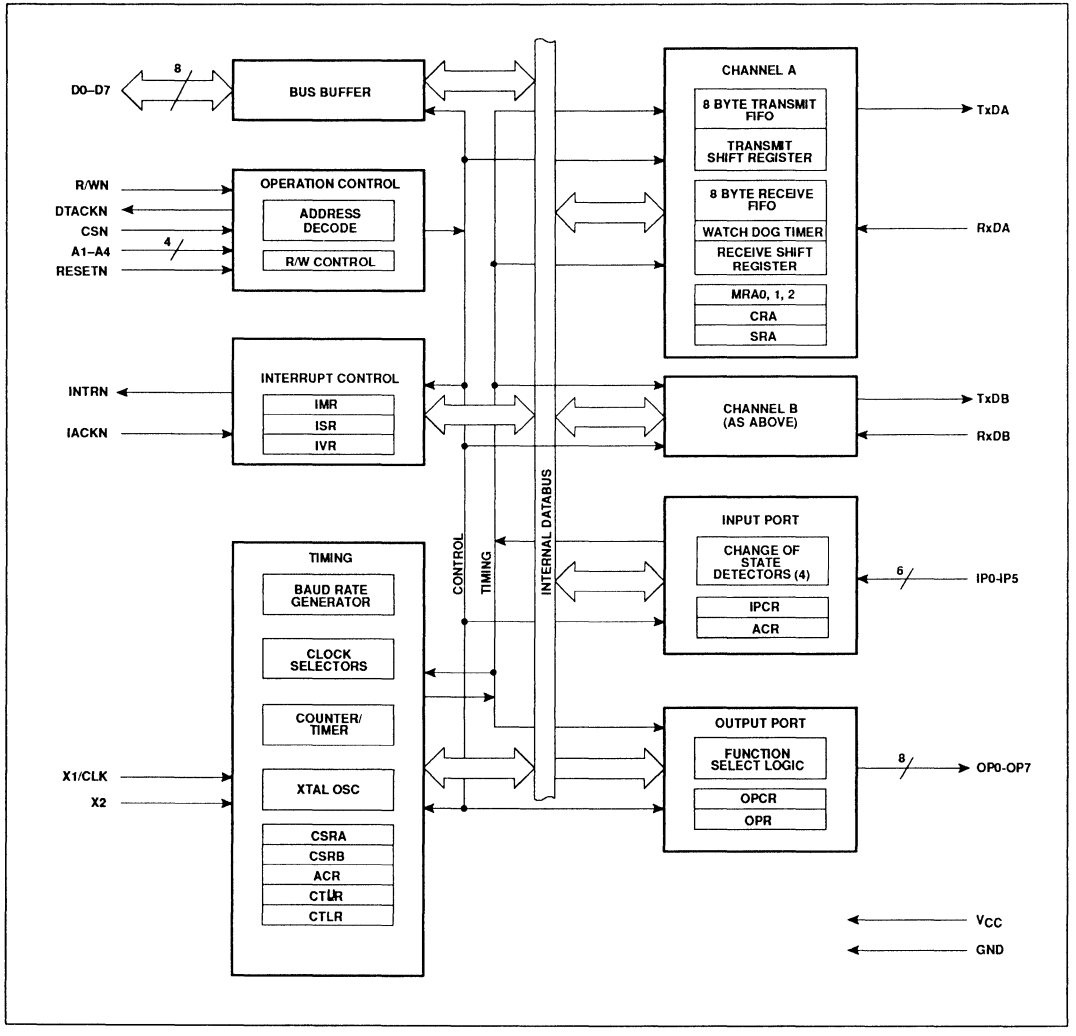
PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A1	24	INTRN
3	IP3	25	D6
4	A2	26	D4
5	IP1	27	D2
6	A3	28	D0
7	A4	29	OP6
8	IP0	30	OP4
9	R/WN	31	OP2
10	DTACKN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CSN
18	D1	40	IP2
19	D3	41	IACKN
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	VCC

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C
40-Pin Cerdip	SC68C92C1F40	SC68C92E1F40
40-Pin Plastic DIP	SC68C92C1N40	SC68C92E1N40
44-Pin Plastic LCC	SC68C92C1A44	SC68C92E1A44

Dual asynchronous receiver/transmitter (DUART) SC68C92

BLOCK DIAGRAM



Dual asynchronous receiver/transmitter (DUART) SC68C92

PIN DESCRIPTION

SYMBOL	PIN NO.	TYPE	NAME AND FUNCTION
D0–D7	25,16,24,17 23,18,22,19	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	35	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A1–A4 inputs. When CEN is High, the DUART places the D0–D7 lines in the 3-State condition.
R/WN	8	I	**Read/Write:** A High input indicates a read cycle and a low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1–A4	1,2,5,6	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	34	I	**Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state.
DTACKN	9	O	**Data Transfer Acknowledge:** 3-State active-Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	21	O	**Interrupt Request:** Active-Low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	37	I	**Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	32	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	33	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin can be left open.
RxDA	31	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	10	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	30	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	11	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	29	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	12	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	28	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	13	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	27	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	14	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	26	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	15	O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYBN output.
IP0	7	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	4	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	36	I	**Input 2:** General purpose input or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP3	2	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	39	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	38	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	40	I	**Power Supply:** +5V supply input.
GND	20	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation[5]	750	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. Maximum power dissipation of the chip when outputs are loaded externally. For operating current, see DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[6]		2.0			V
V_{IH}	Input high voltage (except X1/CLK)[7]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		$0.8V_{CC}$			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = –400µA	V_{CC} –0.5			V
I_{IX1PD}	X1/CLK input current – power down	V_{IN} = 0 to V_{CC}	–10		+10	µA
I_{ILX1}	X1/CLK input low current – operating	V_{IN} = 0	–75		0	µA
I_{IHX1}	X1/CLK input high current – operating	V_{IN} = V_{CC}	0		75	µA
I_{OHX2}	X2 output high current – operating	V_{OUT} = V_{CC}, X1 = 0	0		+75	µA
I_{OHX2S}	X2 output high short circuit current – operating	V_{OUT} = 0, X1 = 0	–10		–1	mA
I_{OLX2}	X2 output low current – operating	V_{OUT} = 0, X1 = V_{CC}	–75		0	µA
I_{OLX2S}	X2 output low short circuit current – operating and power down	V_{OUT} = V_{CC}, X1 = V_{CC}	1		10	mA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	–10		+10	µA
	Input port pins	V_{IN} = 0 to V_{CC}	–20		+10	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			10	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0V	–10			µA
I_{ODL}	Open-drain output low current in off State	V_{IN} = 0	–10			µA
I_{ODH}	Open-drain output high current in off State	V_{IN} = V_{CC}			10	µA
I_{CC}	Power supply current[5]	TTL input levels			10	mA
	Operating mode	CMOS input levels			10	mA
		TTL input levels			3.0	mA
	Power down mode	CMOS input levels			TBD	µA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of V_{CC} –0.2V and V_{SS} + 0.2V.
6. $T_A \geq 0°C$
7. $T_A < 0°C$

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ[3]	Max	
Reset Timing						
t_{RES}	1	RESET pulse width	1.0			µs
Bus Timing[5]						
t_{AS}	2,3,4	A1–A4 setup time to CSN Low	10			ns
t_{AH}	2,3,4	A1–A4 hold time from CSN Low	30			ns
t_{RWS}	2,3,4	RWN setup time to CSN High	0			ns
t_{RWH}	2,3,4	RWN holdup time to CSN High	0			ns
t_{CSW}[8]	2,3,4	CSN High pulse width	50			ns
t_{CSD}[9]	2,3,4	CSN or IACKN High from DTACKN Low	20			ns
t_{DD}	2,3,4	Data valid from CSN or IACKN Low			110	ns
t_{DA}	2	RDN Low to data bus active[8]	15			ns
t_{DF}	2,3,4	Data bus floating from CSN or IACKN High[8]			45	ns
t_{DI}	2	RDN High to data bus invalid[8]	20			ns
t_{DS}	2,3,4	Data setup time to CLK High	75			ns
t_{DH}	2,3,4	Data hold time from CSN High	0			ns
t_{DAL}	2,3,4	DTACKN Low from read data valid	0			ns
t_{DCR}	2,3,4	DTACKN Low (read cycle) from CLK High			45	ns
t_{DCW}	2,3,4	DTACKN Low (write cycle) form CLK High			45	ns
t_{DAH}	2,3,4	DTACKN High from CSN or IACKN High			30	ns
t_{DAT}	2,3,4	DTACKN High impedance from CSN or IACKN High			45	ns
t_{CSC}[7]	2,3,4	CSN or IACKN setup time to clock High	30			ns
Port Timing[5]						
t_{PS}	5	Port input setup time to CSN Low	0			ns
t_{PH}	5	Port input hold time from CSN High	0			ns
Interrupt Timing						
t_{IR}	6	INTRN (or OP3–OP7 when used as interrupts) negated from:				
		Read RHR (RxRDY/FFULL interrupt)			100[10]	ns
		Write THR (TxRDY interrupt)			100[10]	ns
		Reset command (break interrupt)			100[10]	ns
		Stop C/T command (counter interrupt)			100[10]	ns
		Read IPCR (input port change interrupt)			100[10]	ns
		Write IMR (clear of interrupt mask bit)			100[10]	ns
Clock Timing						
t_{CLK}	7	X1/CLK High or Low time	80			ns
f_{CLK}	7	X1/CLK frequency	1	3.6864	4	MHz
t_{CTC}	7	CTCLK (IP2) High or Low time	60			ns
f_{CTC}	7	CTCLK (IP2) frequency[9]	100		8	MHz
t_{RX}	7	RxC High or Low time	220			ns
f_{RX}	7	RxC frequency (16X)[9]	100		2	MHz
		(1X)[9]	100		1	MHz
t_{TX}	7	TxC High or Low time	220			ns
f_{TX}	7	TxC frequency (16X)[9]	0		2	MHz
		(1X)[9]	0		1	MHz
Transmitter Timing						
t_{TXD}	8	TxD output delay from TxC Low			120	ns
t_{TCS}	8	Output delay from TxC Low to TxD data output			50	ns
Receiver Timing						
t_{RXS}	9	RxD data setup time to RxC High	100			ns
t_{RXH}	9	RxD data hold time from RxC High	100			ns

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
6. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
7. This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.
8. Guaranteed by characterization of sample units.
9. Minimum frequencies are not tested but are guaranteed by design.
10. 325ns maximum for T_A > 70°C.

BLOCK DIAGRAM

The SC68C92 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR), the Auxiliary Control Register (ACR), and the Interrupt Vector Register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR register on the data bus and asserting DTACKN.

Outputs OP3–OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Programming bit 0 of MR0 to a "1" gives additional baud rates of 57.6kB, 115.2kB and 230.4kB. These will be in the 16X mode. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SC68C92 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 6-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always be read as a logic 1 and D6 will reflect the level of IACKN. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 – 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The

detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

The 8-bit multipurpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also be individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SC68C92 is conditioned to transmit data when the transmitter is enabled through the command register. The SC68C92 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When the transmitter is initially enabled the TxRDY and TxEMPTY bits will be set in the status register. When a character is loaded to the transmit fifo the TxEMPTY bit will be reset. The TxEMPTY will not set until: 1) the transmit fifo is empty and the transmit shift register has finished transmitting the stop bit of the last character written to the transmit fifo, or 2) the transmitter is disabled and then re-enabled. The TxRDY bit is set whenever the transmitter is enabled and the TxFIFO is not full. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first.

Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SC68C92 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7–1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of eight characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all eight stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. Register Addressing

A4	A3	A2	A1	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Reserved	Interrupt Vector Register (IVR)
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

REGISTER DESCRIPTIONS

Mode Registers

MR0 is accessed by setting the MR pointer to 0 via the command register command D.

MR0A

MR0[7] – This bit controls the receiver watch dog timer. 0 = disable, 1 = able. When enabled, the watch dog timer will generate a receiver interrupt if the receiver FIFO has not been accessed within 64 bit times of the receiver 1X clock. This is used to alert the control processor that data is in the RHR that has not been read. This situation may occur when the last part of a message is not large enough to generate an interrupt.

MR0[6] – Bit 2 of receiver FIFO interrupt level. This bit along with Bit 6 of MR1 sets the fill level of the 8 byte FIFO that generates the receiver interrupt.

MR0[6]	MR1[6]	Interrupt Condition
0	0	1 or more bytes in FIFO (Rx RDY)
0	1	3 or more bytes in FIFO
1	0	6 or more bytes in FIFO
1	1	8 or more bytes in FIFO (Rx FULL)

MR0[5:4] – Tx interrupt fill level.

MR0[5]	MR0[4]	Interrupt Condition
0	0	8 bytes empty (Tx EMPTY)
0	1	4 or more bytes empty
1	0	6 or more bytes empty
1	1	1 or more bytes empty (Tx RDY)

MR0[3] – Not used. Should be set to 0.

MR0[2:1] – Test 1 and Test 2. Used for factory test. Set to 0

MR0[0] – Baud rate extend. 0 = Normal baud rates. 1 = Extend baud rate. 57.6kB, 115.2kB, 230.4kB.

Note: MR0[3:0] are not used in channel B. They should be set to 0.

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.

2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:
1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:
1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been retransmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:
1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR0A MR0B	**Rx WATCH DOG**	**RxINT (2)**	**TxINT (1:0)**	**DON'T CARE**	**TEST 1**	**TEST 2**	**BAUD RATE EXTEND**
	0 = Disable 1 = Enable			Set to 0	Set to 0	Set to 0	0 = Normal 1 = Extend

NOTE:
MR0B[3:0] are not implemented. When writing to MR0B set them to 0. A read of MR0B[3:0] returns 1111.

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	**RxINT SELECT**	**ERROR MODE**	**PARITY MODE**	**PARITY TYPE**	**BITS PER CHARACTER**
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3 BIT 2 BIT 1 BIT 0			
	CHANNEL MODE	**TxRTS CONTROL**	**CTS ENABLE Tx**	**STOP BIT LENGTH***			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CSRA CSRB	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
	See Text				See Text			

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CRA CRB	MISCELLANEOUS COMMANDS				DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
	See Text				0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	11 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE			DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INT
ACR	0 = set 1 1 = set 2	See Table 4			0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]
IVR								

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3–16X	IP3–16X
1111	IP3–1X	IP3–1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

Table 3. Baud Rate

	MR0[0] = 0		MR0[0] = 1	
CSRA[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	50	450
0001	110	110	110	110
0010	134.5	134.5	134.5	230.4K
0011	200	150	200	900
0100	300	300	1800	1800
0101	600	600	3600	3600
0110	1,200	1,200	7200	7,200
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	14.4K	14.4K
1001	4,800	4,800	28.8K	28.8K
1010	7,200	1,800	7,200	1,800
1011	9,600	9,600	57.6K	57.6K
1100	38.4K	19.2K	230.4K	115.2K
1101	Timer	Timer	Timer	Timer
1110	IP4-16X	IP4-16X	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X	IP4-1X	IP4-1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select

This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP6–16X	IP6–16X
1111	IP6–1X	IP6–1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select

This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5–16X	IP5–16X
1111	IP5–1X	IP5–1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7:4] – Miscellaneous Commands

The encoded value of this field may be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.

0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Set MR pointer to 0.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued

1101 Not used.

1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only. Design Note: The part will not output DTACKN while in power down mode. Use automatic DTACKN generation.

1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

CRA[3] – Disable Channel A Transmitter

This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter

Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver

This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver

Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of comamnds "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break

This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In the special multidrop mode, the parity error bit stores the received A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

SOPR – Set the Output Port Bits (OPR)

SOPR[7:0] – Ones in the byte written to this register will cause the corresponding bit positions in the OPR to set to 1. Zeros have no effect.

ROPR – Reset Output Port Bits (OPR)

ROPR[7:0] – Ones in the byte written to the ROPR will cause the corresponding bit positions in the OPR to set to 0. Zeros have no effect.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL BAUD RATE	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	–0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	–0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

NOTE:
Duty cycle of 16x clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR [6:4] Field Definition

[6:4]	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or external clock (x1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

IVR – Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.

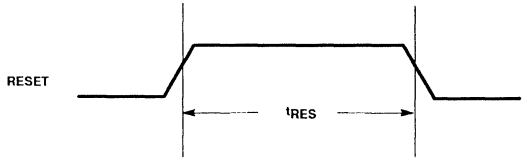


Figure 1. Reset Timing

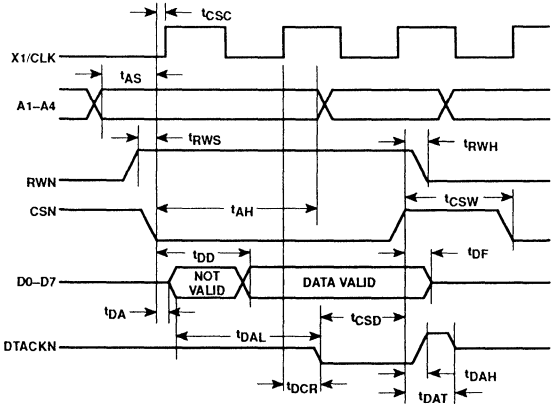


Figure 2. Bus Timing (Read Cycle)

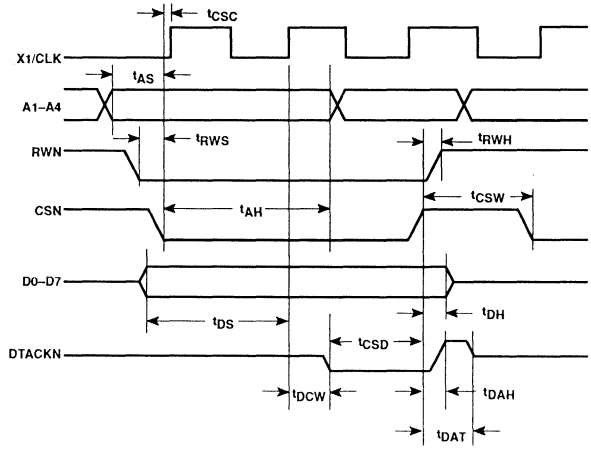


Figure 3. Bus Timing (Write Cycle)

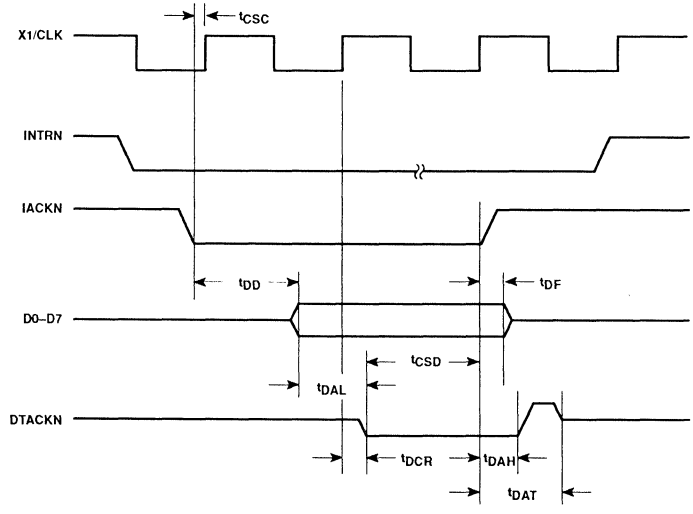


Figure 4. Interrupt Cycle Timing

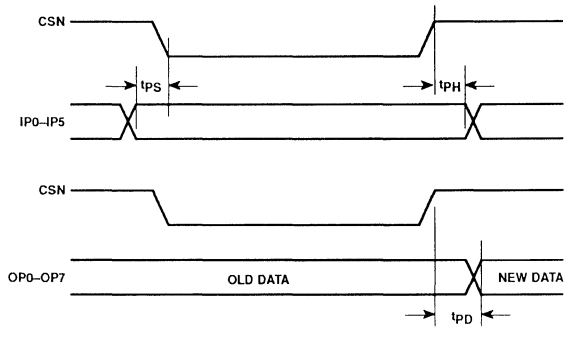
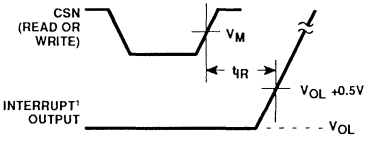


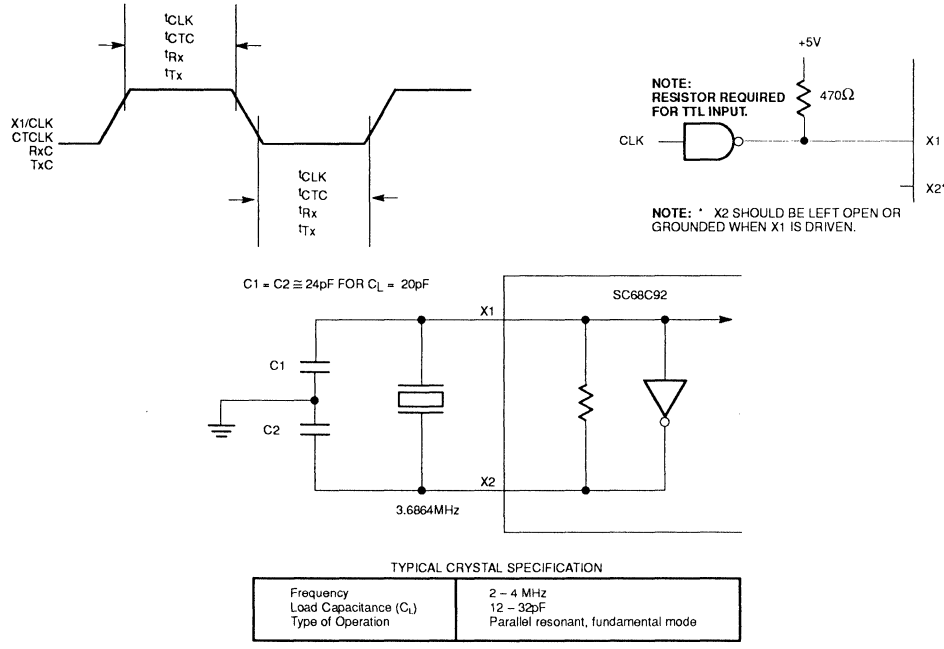
Figure 5. Port Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from themidpoint of the switching signal, V_M, to a point 0.5 volts above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 6. Interrupt Timing



TYPICAL CRYSTAL SPECIFICATION

Frequency	2 – 4 MHz
Load Capacitance (C_L)	12 – 32pF
Type of Operation	Parallel resonant, fundamental mode

Figure 7. Clock Timing

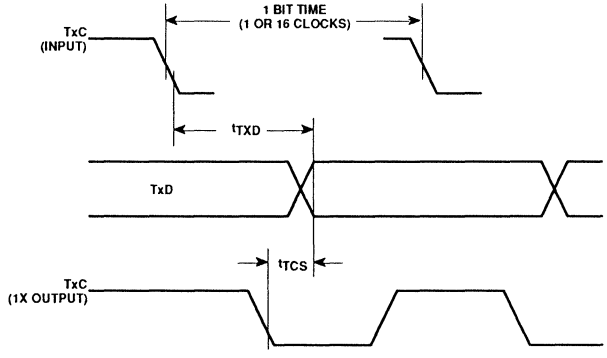


Figure 8. Transmit Timing

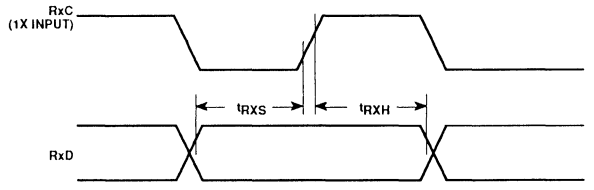
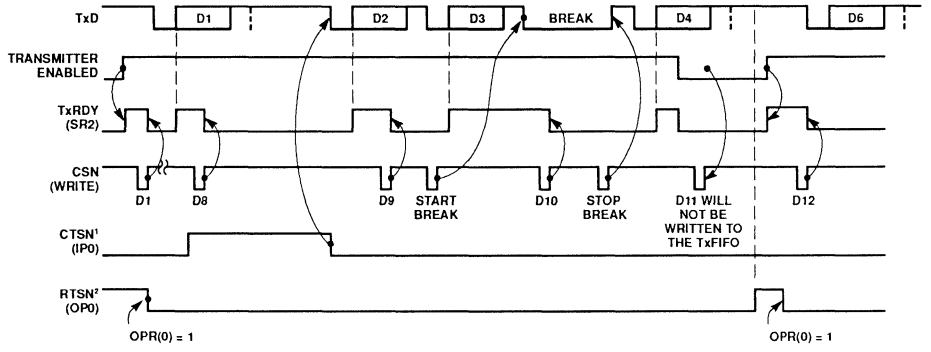
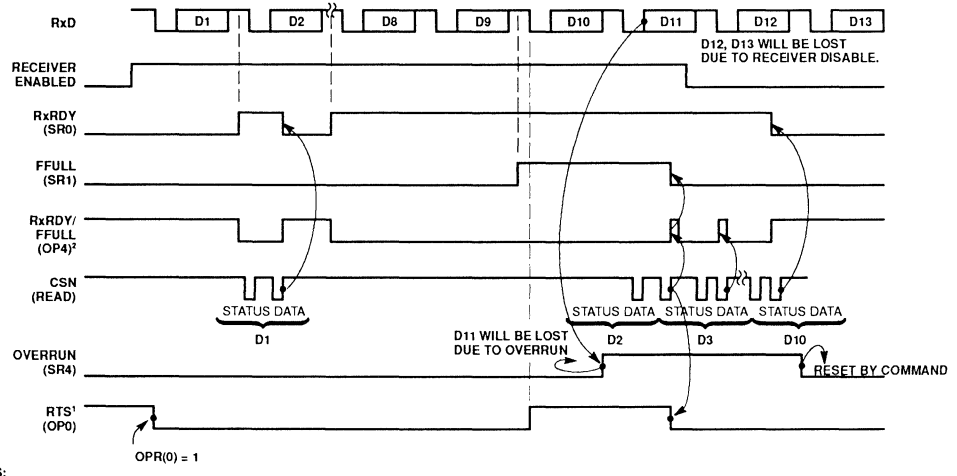


Figure 9. Receive Timing



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 10. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) and MR1(6) = 0.

Figure 11. Receiver Timing

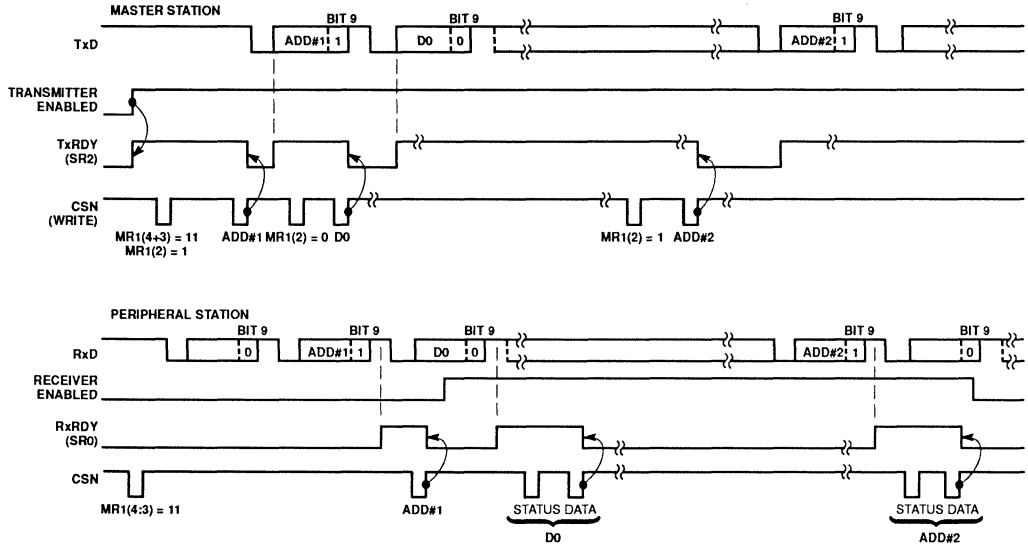


Figure 12. Wake-Up Mode

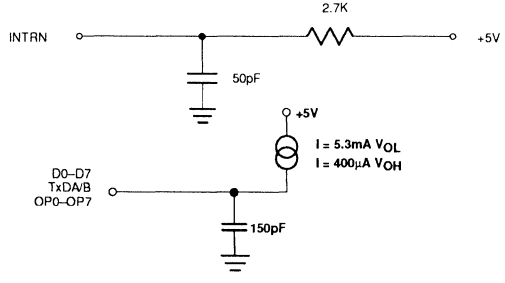


Figure 13. Test Conditions on Outputs

Philips Components–Signetics

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Data Communication Products	

SC26C94/SC68C94

Quad universal asynchronous receiver/transmitter (QUART)

DESCRIPTION

The SC26C94/SC68C94 quad universal asynchronous receiver/transmitter (QUART) combines four enhanced Signetics industry-standard UARTs with an innovative interrupt scheme that can vastly minimize host processor overhead. It is implemented using Signetics' high-speed CMOS process that combines small die size and cost with low power consumption.

The operating speed of each receiver and transmitter can be selected independently at one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the Octal UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

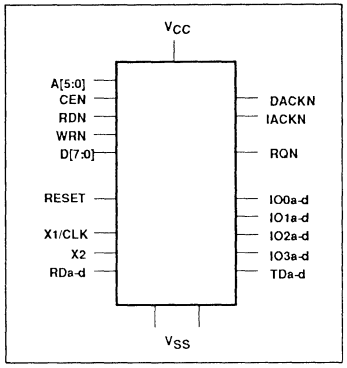
Each receiver is buffered with eight character FIFOs (first-in-first-out memories) and one shift register to minimize the potential for receiver overrun and to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full. (RTS control)

The SC26C94/SC68C94 provides a power-down mode in which the oscillator is stopped and the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The Octal UART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- Four Signetics industry-standard UARTs
- Eight byte receive FIFOs for each UART
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud Non-standard rates to 230.4K baud
  - User-defined rates from the programmable counter/timer associated with each block
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Eight byte transmit FIFOs for each UART
- Programmable interrupt priorities
- Identification of highest priority interrupt
- Global interrupt register set provides data from interrupting channel
- Vectored interrupts with programmable vector format
- IACKN and DTACKN signals
- Built-in baud rate generator with choice of 18 rates

PIN CONFIGURATIONS



- Four I/O pins per UART for modem controls, clocks, etc.
- Power down mode
- High-speed CMOS technology
- 52-pin PLCC and 48-pin DIP
- Commercial and industrial temperature ranges available
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply
- Two multifunction programmable 16-bit counter/timers
- 1MHz 16X mode operation
- 45ns data bus release time
- "Watch Dog" timer for each receiver

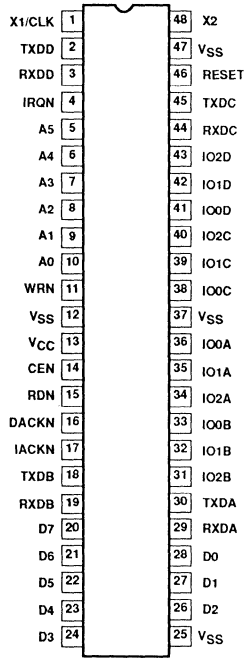
Quad universal asynchronous receiver/transmitter (QUART) SC26C94/SC68C94

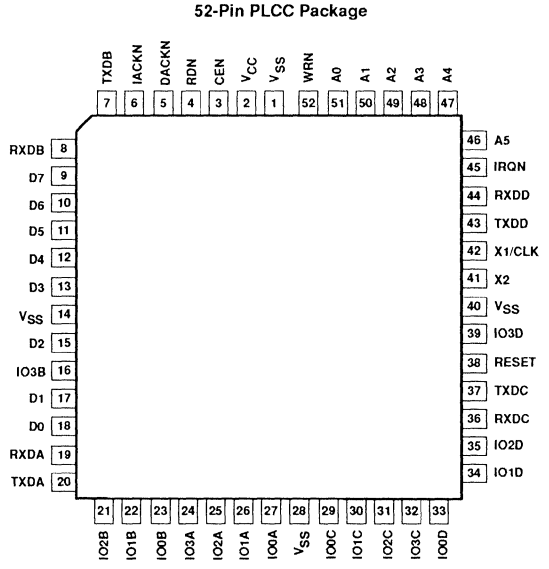
ORDERING INFORMATION

PACKAGES	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	V_{CC} = +5V ±10%, T_A = –40°C to +85°C
Plastic Dual In-Line Package	SC26C94C1N48	SC26C94A1N48
Plastic Leaded Chip Carrier	SC26C94C1A52	SC26C94A1A52

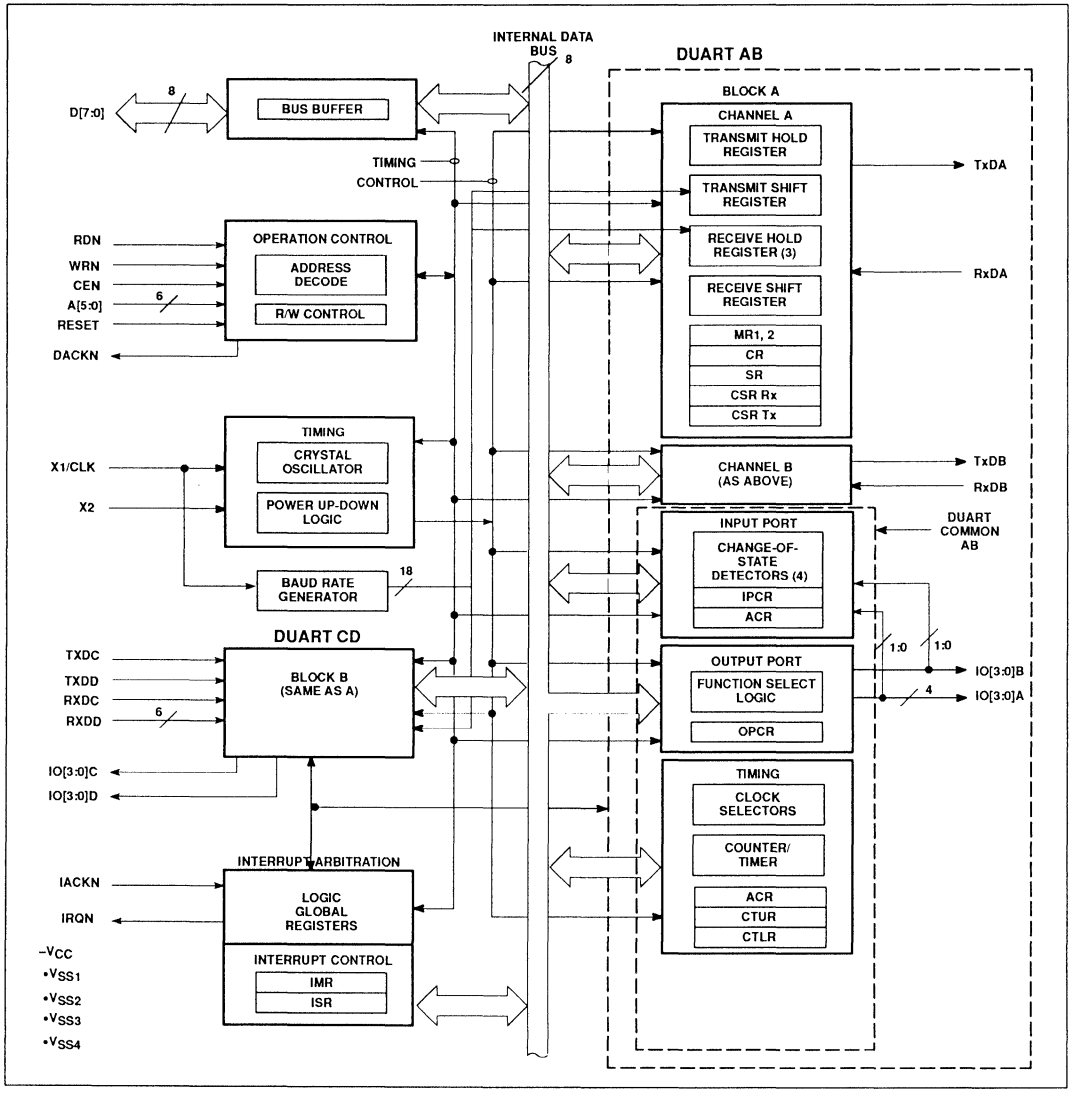
NOTE:
Pin Grid Array (PGA) package version is available from Philips Components Military Division.

PIN CONFIGURATIONS





BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
CEN	I	**Chip Select:** Active low input that, in conjunction with RDN or WRN, indicates that the control processor is trying to access a QUART register.
A5:0	I	**Address Lines:** These inputs select a SC26C94/SC68C94 register to be read or written by the control processor.
D7:0	I/O	**8-bit Bidirectional Data Bus:** Used by the control processor to read and write SC26C94/SC68C94 registers.
RDN	I	**Read Strobe:** Active low input. When this line is asserted simultaneously with CEN, the SC26C94/SC68C94 places the contents of the register selected by A[5:0] on the D[7:0] lines.
WRN	I	**Write Strobe:** Active low input. When this line is asserted simultaneously with CEN, the SC26C94/SC68C94 writes the data on D[7:0] into the register selected by A[5:0].
DACKN	O	**Data ACKnowledge:** Active low, open-drain output to the control processor, which is asserted subsequent to a read or write operation. For a read operation, assertion of DACKN indicates that register data is valid on D[7:0]. For a write operation, it indicates that the data on D[7:0] has been captured into the indicated register. This signal corresponds to READYN on 80x86 processors and DTACKN on 680x0 processors.
IRQN	O	**Interrupt Request:** This active low open-drain output to the control processor indicating that one or more of the UART channels has reached an interrupt value which exceeds that pre-programmed by host software. The IRQN can be used directly as a 680x0 processor input; it must be inverted for use as an 80x86 interrupt input. This signal requires an external pull-up resistor.
IACKN	I	**Interrupt ACKnowledge:** Active low input indicating that the control processor is acknowledging an interrupt requested by this device. The SC26C94/SC68C94 responds to the assertion of this signal by placing an interrupt vector on D[7:0] and asserting DACKN.
TDa-d	O	**Transmit Data:** Serial outputs from the four UARTs.
RDa-d	I	**Receive Data:** Serial inputs to the four UARTs/
I/O0a-d	I/O	**Input/Output 0:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, Clear to Send inputs, 1X or 16X Transmit Clock outputs or general purpose outputs. Change-of-state detection is provided for these pins.
I/O1a-d	I/O	**Input/Output 1:** A multi-use input or output signal for each UART. These pins can be used as general purpose or 1X or 16X transmit clock inputs, or general purpose 1X or 16X receive clock outputs. Change-of-state detection is provided for these pins. In addition, I/O1a and I/O1c can be used as Counter/Timer inputs and I/O1b and I/O1d can be used as Counter/Timer outputs.
I/O2a-d	I/O	**Input/Output 2:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X receive clock inputs, general purpose outputs, RTS output or 1X or 16X receive clock outputs.
I/O3a-d	I/O	**Input/Output 3:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X transmit clock inputs, general purpose outputs, or 1X or 16X transmit clock outputs.
RESET	I	**Master Reset:** Active high reset for the SC26C94/SC68C94 logic. Must be asserted at power-up, may be asserted at other times that the system is to be reset and restarted. Registers reset. MR pointer, CIR, IRQN, DTACKN, IVR Interrupt Vector, Power Down, Test registers, FIFO pointers, Baud rate generator, Error Status, Watch Dog Timers, IMR, Change of State detectors, counter/timer to timer, Transmitter and Receiver controllers.
X1/CLK	I	**Crystal 1 or Communication Clock:** This pin can be connected to one side of a 3.6864MHz or a 7.3728MHz crystal, or can be connected to a TTL-level clock with the same frequency.
X2	O	**Crystal 2:** If a crystal is used, this pin should be connected to its other terminal. If a TTL-level clock is applied to X1, this pin should be left unconnected.

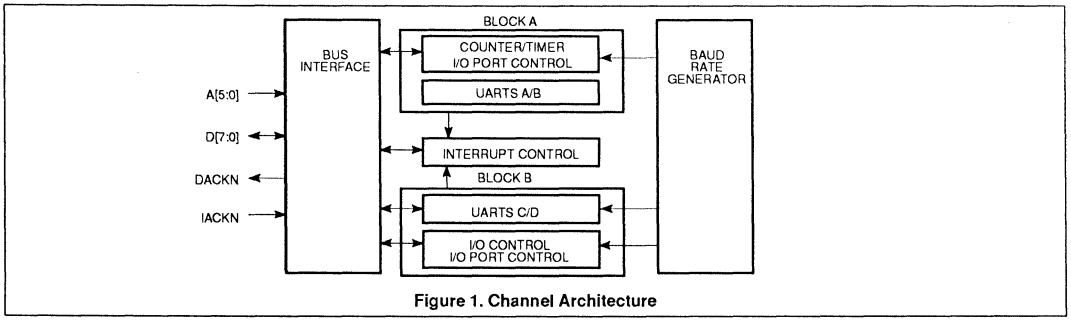


Figure 1. Channel Architecture

Table 1. QUART Registers

A5:0	READ (RDN = Low)	WRITE (WRN = Low)
000000	Mode Register a (MR0a, MR1a, MR2a)	Mode Register a (MR0a, MR1a, MR2a)
000001	Status Register a (SRa)	Clock Select Register a (CSRa)
000010	Reserved	Command Register a (CRa)
000100	Receive Holding Register a (RxFIFOa)	Transmit Holding Register a (TxFIFOa)
001000	Input Port Change Reg ab (IPCRab)	Auxiliary Control Reg ab (ACRab)
000101	Interrupt Status Reg ab (ISRab)	Interrupt Mask Reg ab (IMRab)
000110	Counter/Timer Upper ab (CTUab)	Counter/Timer Upper Reg ab (CTURab)
000111	Counter/Timer Lower ab (CTLab)	Counter/Timer Lower Reg ab (CTLRab)
001000	Mode Register b (MR0b, MR1b, MR2b)	Mode Register b (MR0b, MR1b, MR2b)
001001	Status Register b (SR1b, SR2b)	Clock Select Register b (CSRb, CSRb)
001010	Reserved	Command Register b (CRb)
001011	Receive Holding Register b (RxFIFOb)	Transmit Holding Register b (TxFIFOb)
001100	Output Port Register ab (OPRab)	Output Port Register ab (OPRab)
001101	Input Port Register ab (IPRab)	I/O Port Register a (IOPRa)
001110	Start Counter ab	I/O Port Register b (IOPRb)
001111	Stop Counter ab	Reserved
010000	Mode Register c (MR0c, MR1c, MR2c)	Mode Register c (MR0c, MR1c, MR2c)
010001	Status Register c (SRc)	Clock Select Register c (CSRc)
010010	Reserved	Command Register c (CRc)
010011	Receive Holding Register c (RxFIFOc)	Transmit Holding Register c (TxFIFOc)
010100	Input Port Change Reg cd (IPCRcd)	Auxiliary Control Reg cd (ACRcd)
010101	Interrupt Status Reg cd (ISRcd)	Interrupt Mask Reg cd (IMRcd)
010110	Counter/Timer Upper cd (CTUcd)	Counter/Timer Upper Reg cd (CTURcd)
010111	Counter/Timer Lower cd (CTLcd)	Counter/Timer Lower Reg cd (CTLRcd)
011000	Mode Register d (MR0d, MR1d, MR2d)	Mode Register d (MR0d, MR1d, MR2d)
011001	Status Register d (SRd)	Clock Select Register d (CSRd)
011010	Reserved	Command Register d (CRd)
011011	Receive Holding Register d (RxFIFOd)	Transmit Holding Register d (TxFIFOd)
011100	Output Port Register cd (OPRcd)	Output Port Register cd (OPRcd)
011101	Input Port Register cd (IPRcd)	I/O Port Register c (IOPRc)
011110	Start Counter cd	I/O Port Register d (IOPRd)
011111	Stop Counter cd	Reserved
100000	Bidding Control Register a (BCRa)	Bidding Control Register a (BCRa)
100001	Bidding Control Register b (BCRb)	Bidding Control Register b (BCRb)
100010	Bidding Control Register c (BCRc)	Bidding Control Register c (BCRc)
100011	Bidding Control Register d (BCRd)	Bidding Control Register d (BCRd)
100100	Reserved	Power Down
100101	Reserved	Power Up
100110	Reserved	Disable DACKN
100111	Reserved	Enable DACKN
101000	Current Interrupt Register (CIR)	Reserved
101001	Global Interrupt Channel Reg (GICR)	Interrupt Vector Register (IVR)
101010	Global Int Byte Count Reg (GIBCR)	Update CIR
101011	Global Receive Holding Reg (GRxFIFO)	Global Transmit Holding Reg (GTxFIFO)
101100	Interrupt Control Register (ICR)	Interrupt Control Register (ICR)
101101	Reserved	Test 3
101101	Reserved	Set X1/CLK Normal
101111	Reserved	Set X1/CLK to divide by two
110000–111000	Reserved	Reserved
111001	Test Mode	Test Mode
111010–111111	Reserved	Reserved

FUNCTIONAL BLOCKS

The QUART is composed of four Signetics industry-standard UARTs, each having a separate transmit and receive channel.

The Basic UART cells in the QUART are configured with 8-byte Receive FIFOs and 8-byte Transmit FIFOs. Hardware supports interrupt priority arbitration based on the number of bytes available in the transmit and receive FIFOs. Attempts to push a full FIFO or pop an empty FIFO do not affect the count.

Baud Rate Generator

The baud rate generator used in the QUART is the same as that used in other Signetics industry standard UARTs. It provides 18 basic Baud rates from 50 baud to 38,400 baud. It has been enhanced to provide to provide other baud rates up to 230,400 baud based on a 3.6364MHz clock. With a 7.272800MHz clock 460,800 baud is available.

BLOCK DIAGRAM

As shown in the block diagram, the QUART consists of: data bus buffer, interrupt control, operation control, timing, and four receiver and transmitter channels. The four channels are divided into two different blocks, each block independent of the other (see Figure 1).

Channel Blocks

There are two blocks (Figure 1), each containing two sets of receiver/transmitters. In the following discussion, the description applies to Block A which contains channels a and b. However, the same information applies to all channel blocks.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the QUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the control processor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers (MR) 0, 1 and 2 are accessed via an address counter. This counter is set to one (1) by reset for compatibility with other Signetics UARTs. It is set to 0 via a command to the Command Register (CR). The address counter is incremented with each access to the MR until it reaches 2 at which time it remains at 2. All subsequent accesses to the MR will be to MR2 until the MR counter changed by a reset or an MR counter command.

The Mode Registers control the basic configuration of the UART channels. There is one for each UART. (Transmitter/receiver pair)

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer for each block, and two clock selectors.

Oscillator

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1 must be driven and X2 left floating as shown in Figure 8. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied even if the internal BRG is not used.

Baud Rate Generator

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Thirteen of these are available simultaneously for use by the receiver and transmitter. Eight are fixed, and one of two sets of five can be selected by programming ACR[7]. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection, by the receiver and transmitter, of any of these baud rates or an external timing signal.

Counter/Timer (C/T)

The counter timer is a 16-bit programmable divider that operates in one of three modes: counter, timer, time out. In the timer mode it generates a square wave. In the counter mode it generates a time delay. In the time out mode it monitors the time between received characters. In this mode it is acting as a programmable watch dog timer.

The C/T uses the numbers loaded into the Counter/Timer Lower Register (CTLR) and the Counter/Timer Upper Register (CTUR) as its divisor.

There are two counter/timers in the QUART; one for each DUART. The counter/timer clock source and mode of operation (counter or timer) is selected by the Auxiliary Control Register bits 6 to 4 (ACR[6:4]). The output of the counter/timer may be used for a baud rate and/or may be output to the I/O pins for some external function that may be totally unrelated to data transmission. The counter/timer also sets the counter/timer ready bit in the Interrupt Status Register (ISR) when its output transitions from 1 to 0.

A register read address is reserved to start counter/timer command and a second register read address is reserved to issue a stop command. The START command always loads the contents of CTUR, CTLR, to the counting registers. The STOP command always resets the ISR[3] bit in the interrupt status registers. See Table 1.

Timer Mode

In the timer mode a symmetrical square wave is generated whose half period is equal in time to division of the selected counter/timer clock frequency by the 16-bit number loaded in the CTLR CTUR. Thus, the frequency of the counter/timer output will be equal to the counter/timer clock frequency divided by twice the value of the CTUR CTLR. While in the timer mode the ISR bit 3 (ISR[3]) will be set each time the counter/timer transitions from 1 to 0. (High to low) This continues regardless of issuance of the stop counter command. ISR[3] is reset by the stop counter command. NOTE: Reading of the CTU and CTL registers in the timer mode is not meaningful.

Counter Mode

In the counter mode the counter/timer counts the value of the CTLR CTUR down to zero and then sets the ISR[3] bit and sets the counter/timer output from 1 to 0. It then rolls over to 65,365 and continues counting with no further observable effect.

Reading the C/T in the counter mode outputs the present state of the C/T. If the C/T is not stopped, a read of the C/T may result in changing data on the data bus.

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. If the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO

is full, the CPU will not be interrupted for the remaining characters in the RxFIFO.

By programming the C/T such that it would time out in just over one character time, the above situation could be avoided. The processor would be interrupted any time the data stream had stopped for more than one character time. NOTE: This is very similar to the watch dog timer controlled by MR0. The difference is in the programmability of the delay time.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at a time.

The timeout mode disables the regular START/STOP counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after one C/T clock, reloaded with the value in CTUR and CTLR and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx='Ax', will also clear the counter ready bit and stop the counter until the next character is received.

The counter timer is controlled with six commands: Start/Stop C/T, Read/Write Counter/Timer lower register and Read/Write Counter/Timer upper register. These commands have slight differences depending on the mode of operation. Please see the detail of the commands under the CTLR CTUR Register descriptions.

Receiver and Transmitter

The QUART has four full-duplex asynchronous receiver/transmitters. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

Registers associated with the communications channel are the mode registers (MR0, MR1 and MR2) Clock Select Register (CSR), Command Register (CR), Status Register (SR), Transmit FIFO (TxFIFO), and the Receive FIFO (RxFIFO). The transmit and receive FIFOs are each eight characters deep. The receive FIFO also stores three status bits with each character.

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the TxFIFO. In the 16X clock mode, this also re-synchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

The transmitter can be forced to send a break (continuous Low condition) by issuing a start break command via the CR. The break is terminated by a stop break command. If the transmitter is disabled, it continues operating until the characters currently being transmitted and the character in the TxFIFO, if any, are completely sent out. Characters cannot be loaded in the TxFIFO while the transmitter is disabled.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode).

If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver samples the input. This continues at one bit time intervals, at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The data is then transferred to the RxFIFO and the RxRDY bit in the SR is set to a one. If the character length is less than eight bits, the most significant unused bits in the RxFIFO are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

RECEIVER FIFO

The RxFIFO consists of a first-in-first-out (FIFO) with a capacity of eight characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read, and a FFULL status bit is set if all eight stack positions are filled with data. The number of filled positions is encoded into a 3-bit value. This value is sent to the interrupt bidding logic where it is used to generate an interrupt. A read of the RxFIFO, outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

NOTE: The number of filled positions in the RxFIFO is coded as one (1) less than the actual number. Thus, three filled positions is coded as two, 8 filled is coded as 7, etc.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RxFIFO is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the

shift register is lost and the overrun error status bit, SR[4], will be set upon receipt of the start bit of the new (overrunning) character.

A "watch dog" timer is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer to alert the control processor that characters are in the RxFIFO which have not been read. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the Receive shift register to the RxFIFO.

WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the QUART incorporates a special mode which provides automatic "wakeup" of a receiver through address frame (or character) recognition for multi-processor or multi-station communications. This mode is selected by programming MR1[4:3] to '11'.

In this mode of operation a 'master' station transmits an address character to the several 'slave' stations on the line. The address character is identified by setting its parity bit to 1. The slave stations will usually have their receivers partially enabled as a result of setting MR1[4:3] to 11. When the receivers see a parity bit set to one they will load that character to the RxFIFO and set the RxRDY bit in the status register. The user would usually set the receiver interrupt to occur on RxRDY as well. (All characters whose parity bits are set to 0 will be ignored). The local processor at the slave station will read the 'address' character just received. The master will normally follow an address character(s) with data characters. Since the data characters transmitted by the master will have their parity bits set to zero, stations other than the addressed one(s) will ignore the data.

A transmitted character consists of a start bit, the programmed number of data and stop bits and an "address/data" bit. The parity bit is used as the address or data indicator. The polarity of the A/D bit is selected by setting MR1[2] to zero or one; zero indicates that the current byte is data, while one indicates that the current byte is addresses. The desired polarity of the A/D bit (parity) should be programmed before the TxFIFO is loaded.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RxFIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RxFIFO. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

INPUT OUTPUT (I/O) PINS

There are 16 multi-use pins; four for each UART. These pins are accessed and controlled via the Input Port Register (IPR), I/O Port Control Register (IOPCR), Input Port Change Register (IPCR), and Output Port Register (OPR). They may be individually programmed to be inputs or outputs.

I/O0x and I/O1x pins have change of state detectors. The change of state detectors sample the input ports every 26.04µs and set the change bit in the IPCR if the pin has changed since it was last read. Whether the pins are programmed as inputs or outputs the change detectors still operation and report changes accordingly. See the register descriptions of the I/O ports for the detailed use of these features.

Interrupt Priority Logic

The interrupt logic compares all active interrupts in the QUART, periodically selecting the highest priority interrupt for comparison to an Interrupt Threshold value. User programmabie register fields allow the system programmer to tailor which interrupt conditions are more important than others. Programmable interrupt priorities allow timely response to critical interrupts or simply allow a single CPU to service a greater number of interrupt situations than it could using more conventional methods.

Overview

The interrupt logic produces a numeric code that identifies the highest priority interrupt condition currently pending. This code is compared against a programmable Interrupt Threshold register which determines whether the IRQN pin is asserted. If the code is currently greater than the programmed value, IRQN is asserted. In the QUART there are 18 interrupt sources:

1. Four receiver data transfer/space filled functions
2. Four receiver break detected conditions
3. Four transmitter FIFO space available events
4. Two counter timer interrupts
5. Four change of state detectors

Each interrupt source is enabled or disabled by the appropriate Interrupt Mask Register (IMR) bit as Signetics UARTs have always been (the receiver timeout function is enabled by a bit in the new MR0 register). Those interrupt sources that are enabled provide the interrupt priority logic with an 8 bit value, considered as an unsigned integer for purposes of this discussion. Those interrupt sources that are disabled do not provide a value to the arbitration logic. This can be accomplished by forcing an all zero value of by inhibiting the EVAL signal, described below, in the disabled interrupt sources.

This integer (called a "bid" since each interrupt is vying for attention) is a concatenation of fixed fields and user programmable fields. The fixed fields are channel number, interrupt type and (for receiver and transmitter types) byte count values. During the "bid arbitration" process, all the bids from enabled sources are presented, simultaneously, to an internal Interrupt Bus. The bidding system and formats are discussed in more detail in the following sections.

The interrupt arbitration logic insures that the interrupt with the numerically largest "bid" value will be the only source driving the Interrupt Bus at the end of the arbitration period. The winner must continue to drive the Interrupt Bus long enough to insure capture by the Interrupt Bus Latches. At the beginning of the next arbitration cycle, all "enabled bidders" drive their current values onto the Interrupt Bus.

The value of the winning bid is compared to the Interrupt Threshold field of the Interrupt Control register which determines if an interrupt should be generated by asserting IRQN. Winning bids with values below the interrupt threshold do not generate an interrupt.

Priority Arbitration and Bidding

Each of the five "types" of interrupts has slightly different "bid" value, as follows:

Receivers

# rcv'd	rEr	1	1	Chan #
3	1	1	1	2

Transmitters

0	# avail	1	0	Chan #
1	3	1	1	2

Break Detect

Programmable	1	0	0	Chan #
3	1	1	1	2

Change of State

Programmable	0	0	1	Chan #
3	1	1	1	2

Counter/Timer

Programmable	0	1	0	1	Chan #
2	1	1	1	1	2

Bits shown above as '0' or '1' are hard-wired inputs to the arbitration logic. Their presence allows determination of the interrupt type and they insure that no bid will have a value of all zeros (a condition that is indistinguishable from not bidding at all). They also serve to set a default priority among the non-receive/transmit types when the programmable fields are all zeros.

The channel number always occupies the two LSBs. Inclusion of the channel number insures that a bid value generated will be unique and that a single "winner" will drive the Interrupt Bus at the end of the arbitration interval. The channel number portion of each UARTs bid is hard-wired with UARTa being channel number 0 and so forth.

As can be seen above, bits 4:2 of the winning bid value can be used to identify the type of interrupt, including whether data was received correctly or not. Like the Channel number field, these bits are hard-wired for each interrupt source.

The "# rcv'd" and "# avail" fields indicate the number of bytes present in the receiver FIFO and the number of empty bytes in the transmitter FIFO, respectively. For both these fields, the count is one less than the actual number of bytes available.

NOTE: When there are zero bytes in the receiver's FIFO, it does NOT bid. Similarly, a full transmitter FIFO makes NO bid. In the case where all bids have been disabled by the Interrupt Mask Register or as a result of their byte counts, the active-low Interrupt Bus will return FFh. This value always indicates no interrupt source is active and IRQN should be negated.

The high order bit of the transmitter "bid" is always zero. An empty transmit FIFO is, therefore, fixed at a lower interrupt priority than a 5/8 full receive FIFO. Bit 4 of a receiver bid is the Receiver Error Bit (RER). The RER is the OR of the parity, framing and overrun error conditions. The RER does little to modify the priority of receiver interrupts vs. transmitter interrupts. It is output to the Interrupt Bus to allow inclusion of good data vs. problem data information in the Current Interrupt Register.

The high order bits of bids for received break, CoS (Change of State) and Counter/Timer events are all programmable. By programming ones in these fields, the associated interrupt source can be made more significant than most receiver and all transmitter interrupts. Values near zero in these fields makes them lower priority classes of interrupt.

As shown in Figure 2, the bid arbitration process is controlled by the EVAL/HOLDN signal derived from the oscillator clock.

Receipt of an IACKN signal from the control processor latches the latest "winning bid" from the latched Interrupt Bus into the Current Interrupt Register (CIR). This logic is diagrammed in Figure 3.

If the IACKN falling edge of Figure 1 occurs during EVAL time, the result from the last arbitration (captured by the Interrupt Bus latches) is stored in CIR. Otherwise, the next EVAL pulse is inhibited and the value in the Interrupt Bus Latches is stored in CIR.

Clearing the Interrupt

Activities which change the state of the ISR will cause the IRQN to assert or negate. In addition, the accessing of a global or local RxFIFO or TxFIFO reduces the associated byte count for transmitter and receiver data interrupts. If the byte count falls below the threshold value, the interrupt request is withdrawn. Other interrupt conditions are cleared as on previous Signetics UARTs.

Once the interrupts is cleared or its byte count value is reduced by one of the methods listed above, a different bidder (or no bidder at all) will win the on-going arbitration. When the winning bid drops below the Interrupt Threshold Register's value, the IRQN pin will negate.

Interrupt Priority Arbitration Hardware

The hardware that resolves which interrupt has the highest priority is shown conceptually in Figure 3. The rising edge of the EVAL signal begins an arbitration. All interrupt sources drive their "bid" onto the active-low Interrupt Bus. An open drain buffer is employed at each bit position. Interrupt sources that are not participating in the arbitration, i.e., those that are disabled, do not assert their Interrupt Bus drivers.

Each interrupt source in the QUART has its own arbitration logic like that shown in Figure 3. Note that a one in a bit of a bid value corresponds to a low on the Interrupt Bus line to low (1), the result is a low (1) on that Interrupt Bus bit regardless of what the other interrupt sources are doing with respect to that line. Thus each line acts as a wired OR.

At each bit position, the arbitration logic compares the value of that bit of its bid value against the OR'd result on that bit of the Interrupt Bus. If it did not drive the line to low, but the result on the interrupt bus line was low, the logic disables less significant bits, if any, from driving the interrupt bus. In effect, the logic of all the active interrupt sources acts together as a combinatorial network to determine the highest priority active interrupt. This network is best understood as acting from the most significant bit of the interrupt bus, in sequence down to the least significant bit. After a suitable settling time, the value on the interrupt bus reflects the numerically highest bid value among the active interrupt sources. However, while the overall logic network is settling, the logic at what what proves to be the final winning interrupt source may find itself temporarily losing at some of the less significant bits.

The winning value is captured on the trailing edge of EVAL; the pulse with of EVAL must be long enough for a worst-case combination of bid values to resolve.

Arbitration - Aftermath

At the end of the arbitration, i.e., the falling edge of EVAL, the winning interrupt source is driving its Channel number, number of bytes (if applicable) and interrupt type onto the Interrupt Bus. These values are captured into a latch by the trailing edge of EVAL. The output of this latch is used by the Interrupt Threshold comparator; the winning value is captured into another set of latches called the Current Interrupt Register (CIR) at the time of an Interrupt Acknowledge cycle.

The Current Interrupt Register and associated read logic is shown in Figure 3. Interrupting channel number and the three bit interrupt type code are readable via the Internal Data Bus.

The contents of the appropriate receiver or transmitter byte "counter", as captured at the time of IACKN assertion, make up bits 7:5 of the CIR. If the interrupt type stored in the Current Interrupt Register is not a receiver or transmitter data transfer type, the CIR[7:5] field is read as the programmable fields of their respective bid formats.

The buffers driving the CIR to the DBUS also provide the means of implementing the Global Interrupting Channel and Global Byte Count Registers, described in a later section.

The winning bid channel number and interrupt type fields can also be used to generate part of the Interrupt Acknowledge (IACK) Vector, as defined by the Interrupt Control Register.

Interrupt Context

The channel number of the winning "bid" is used by the address decoders to provide data from the interrupting UART channel via a set of Global pseudo-registers. The interrupt Global pseudo-registers are:

1. Global Interrupting Byte Count
2. Global Interrupting Channel
3. Global Receive Holding Register
4. Global Transmit Holding Register

The first two Global "registers" are provided by Current Interrupt Register fields as shown in Figure 3. The interrupting channel number latched in CIR modifies address decoding so that the Receive or Transmit Holding Register for the interrupting channel is accessed during I/O involving the Global Receive and Transmit Holding Registers. Similarly, for data interrupts from the transmitter and receiver, the number of characters available for transfer to the CPU or the number of transmit FIFO positions open is available by reading the Global Interrupt Byte Count Register. For non-data interrupts, a read of the Global Interrupt Byte Count Register yields an undefined value.

In effect, once latched by an IACK, the winning interrupt channel number determines the contents of the global registers. All Global registers will provide data from the interrupting UART channel.

Interrupt Threshold Calculation

The state of IRQN is determined by comparison of the winning "bid" value to the Interrupt Threshold field of the Interrupt Control Register.

The logic of the bidding circuit is such that when no interrupt source has a value greater than the interrupt threshold then the interrupt is not asserted and the CIR (Current Interrupt Register) is set to all ones. When one or more of the 18 interrupt sources which are enabled via the IMR (Interrupt Mask Register) exceed the threshold then the interrupt threshold is effectively disconnected from the bidding operation while the 18 sources now bid against each other. The final result is that the highest bidding source will disable all others and its value will be loaded to the CIR and the IRQN pin asserted low. This all occurs during each cycle of the X1,X2 crystal clock.

Interrupt Note on 26C94.
For the receivers and transmitters, the bidding of any particular unit may be held off unless one of four FIFO fill levels is attained. This is done by setting the RxINT and TxINT bits in MR0 and MR1 to non-zero values. This may be used to prevent a receiver or transmitter from generating an interrupt eventhough it is filled above the bid threshold. Although this is not in agreement with the idea that each enabled interrupt source bid withe qual authority, it does allow the flexibility of giving particular receiver or transmitters more interrupt importance than others.

Receiver interrupt fill level.

MR0[6]	MR1[6]	Interrupt Condition
0	0	1 or more bytes in FIFO (Rx RDY) default
0	1	3 or more bytes in FIFO
1	0	6 or more bytes in FIFO
1	1	8 or more bytes in FIFO (Rx FULL)

MR0[5:4] – Tx interrupt fill level.

MR0[5]	MR0[4]	Interrupt Condition
0	0	8 bytes empty (Tx EMPTY) default
0	1	4 or more bytes empty
1	0	6 or more bytes empty
1	1	1 or more bytes empty (Tx RDY)

Vectored Interrupts

The QUART responds to an Interrupt Acknowledge (IACK) initiated by the host MCU by providing an Interrupt Acknowledge Vector on D7:0. The interrupt acknowledge cycle is terminated with a DACKN pulse. The vector provided by the QUART can have one of the three forms under control of the IVC control field (bits 1:0 of the Interrupt Control Register):

With IVC = 00 (IVR only)

IVR7:0
8

With IVC = 01 (channel number)

IVR7:2	Chan #
6	2

With IVC = 10 (type & channel number)

IVR7:5	Type	Chan #
3	3	2

A code of 11 in the Interrupt Vector Control Field of the ICR results in NO interrupt vector being generated. The external data bus will be held in a high impedance state throughout the IACK cycle. A DACKN will be generated normally for the IACK cycle, however.

REGISTERS

The operation of the QUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is described in Table 1.

The bit formats of the QUART registers are depicted in Table 2.

MR0 – Mode Register 0

Mode Register 0 (MR0) is part of the UART configuration registers. It controls the watch dog timer and the encoding of the number of characters received in the RxFIFO. The lower four bits of this register are not implemented in the hardware of the chip. MR0 should be set to only 80h or 00h. A read of this register will return 1111 (Fh) in the lower four bits. See note in Interrupt Threshold Calculation.

The MR0 register is accessed by setting the MR Pointer to zero (0) via the command register command 1011 (Bh).

MR0[7]: This bit enables or disables the RxFIFO watch dog timer.
MR0[7] = 1 enable timer
MR0[7] = 0 disable timer
MR0[6:4]: These bits should always be set to zero.
MR0[3:0]: These bits are not implemented in the chip. They could be used to control hardware external to the chip.

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via the CR. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Control
This bit controls the deactivation of the RTSN output (MPO) by the receiver. This output is manually asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is re-asserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input of the transmitting device.

MR1[6] – Receiver Interrupt Select 1
This bit is reserved and should be set to 0. See note in Interrupt Threshold Calculation.

MR1[5] – Error Mode Select
This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

MR1[4:3] – Parity Mode Select
If 'with parity' or 'force parity' is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1[4:3] = 11 selects the channel to operate in the special wake-up mode.

MR1[2] – Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special 'wake-up' mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select

The QUART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.

Table 2. Register Bit Formats

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

MR0 (Mode Register 0)

Rx Watch-dog Timer	RxINT2 bit	TxINT Control	These bits not implemented. May be used for external control (Reserved for future upgrades)			
0 = off 1 = on	These bits should be set to 0		x	x	x	x

MR1 (Mode Register 1)

RxRTS Control	RxINT1 Select	Error Mode	Parity Mode	Parity Type	Bits per Character
0 = No 1 = Yes	Always set to 0	0 = Char 1 = Block	00 = With parity 01 = Force parity 10 = No parity 11 = Special mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

MR2 (Mode Register 2)

Channel Mode	TxRTS Conrol	CTS Enable Tx	Stop Bit Length*
00 = Normal 01 = Auto-echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 4 = 0.813 8 = 1.563 C = 1.813 1 = 0.625 5 = 0.875 9 = 1.625 D = 1.875 2 = 0.688 6 = 0.938 A = 1.688 E = 1.938 3 = 0.750 7 = 1.000 B = 1.750 F = 2.000

NOTE:
Add 0.5 to values shown above for 0–7, if channel is programmed for 5 bits/char.

CSR (Clock Select Register)

Receiver Clock Select	Transmitter Clock Select
See text	See text

CR (Command Register)

Miscellaneous Commands	Disable Tx	Enable Tx	Disable Rx	Enable Rx
See text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

SR (Status Register)

Rec'd. Break	Framing Error	Parity Error	Overrun Error	TxEMT	TxRDY	FFULL	RxRDY
0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. In character mode, they must be reset when the corresponding data character is read from the FIFO.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is re-clocked and retransmitted on the TXD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

When switching in and out of the various modes, the selected mode is activated at the completion of all transmitted and received characters. Likewise, if a mode is deselected, the device will switch out of the mode at the completion of all transmit and/or receive characters.

MR2[5] – Transmitter Request-to–Send Control

This bit controls the deactivation of the RTSN output (MPO) by the transmitter. This output is manually asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the TxFIFO (if any) are completely transmitted (includes the programmed number of stop bits if the transmitter is not enabled). This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Verify the next to last character of the message is being sent by waiting until transmitter ready is asserted. Disable transmitter after the last character of the message is loaded in the TxFIFO.

Table 2. Register Bit Formats (Continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

ACR (Auxiliary Control Register)

BRG Set Select	Counter/Timer Mode and Source			Delta IO1b	Delta IO0b	Delta IO1a	Delta IO0a
0 = set 1 1 = set 2	See text			0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

IPCR (Input Port Change Register)

Delta IO1b	Delta IO0b	Delta IO1a	Delta IO0a	IO1b	IO0b	IO1a	IO0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

ISR (Interrupt Status Register)

IO Port Change	Delta BREAKb	RxRDY/ FFULLb	TxRDYb	Counter Ready	Delta BREAKa	RxRDY/ FFULLa	TxRDYa
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

IMR (Interrupt Mask Register)

IO Port Change INT	Delta BREAKb INT	RxRDY/ FFULLb INT	TxRDYb INT	Counter Ready INT	Delta BREAKa INT	RxRDY/ FFULLa INT	TxRDYa INT
0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

CTUR (Counter/Timer Upper Register)

C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTLR (Counter/Timer Lower Register)

C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

IPR (Input Port Register)

IO3b	IO2b	IO3a	IO2a	IO1b	IO0b	IO1a	IO0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

MR2[4] – Clear-to-Send Control

The sate of this bit determines if the CTSN input (IO) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (Low), the character is transmitted. If it is negated (High), the TxD output remains in the marking state and the transmission is delayed until CTSN goes Low. Changes in CTSN, while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a mark condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled). If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmitted.

CSR – Clock Select Register

CSR[7:4] – Receiver Clock Select
When using a 3.6864MHz crystal or external clock input, this field selects the baud rate clock for the receiver as shown in Table 3.

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111. IO2x is external input.

CSR[3:0] – Transmitter Clock Select
This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3, except as follows:

CSR[3:0]	ACR[7] = 0	ACR[7] = 1
1 1 1 0	IO3x – 16X	IO3x – 16X
1 1 1 1	IO3x – 1X	IO3x – 1X

Table 3. Baud Rate

CSR[7:4]	Test 3 = 0		Test 3 = 1	
	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75	50	450
0 0 0 1	110	110	110	110
0 0 1 0	134.5	38.4K	134.5	230.4K
0 0 1 1	200	150	200	900
0 1 0 0	300	300	1800	1,800
0 1 0 1	600	600	3,600	3,600
0 1 1 0	1,200	1,200	7,200	7,200
0 1 1 1	1,050	2,000	1,050	2,000
1 0 0 0	2,400	2,400	14.4K	14.4K
1 0 0 1	4,800	4,800	28.8K	28.8K
1 0 1 0	7,200	1,800	7,200	1,800
1 0 1 1	9,600	9,600	57.6K	57.6K
1 1 0 0	38.4K	19.2K	230.4K	115.2K
1 1 0 1	Timer	Timer	Timer	Timer
1 1 1 0	IO2 – 16X	IO2 – 16X	IO2 – 16X	IO2 – 16X
1 1 1 1	IO2 – 1X	IO2 – 1X	IO2 – 1X	IO2 – 1X

CR – Command Register

CR is used to write commands to the Octal UART.

CR[7:4] – Miscellaneous Commands
The encoded value of this field can be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the MR pointer to point to MR1.

0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO pointer is reset to the first location.

0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]}. Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.

0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2 or 6]) to be cleared to zero.

0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the TxFIFO, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break

0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The register in this channel will restart the C/T as each receive character is transferred from the shift register to the RxFIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Reserved.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued.

1101 Set MR pointer to 0.

111x Reserved for testing.

CR[3] – Disable Transmitter
This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the TxFIFO when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CR[2] – Enable Transmitter
Enables operation of the transmitter. The TxRDY status bit will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wake–up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half bit time (two successive edges of the internal or external 1x clock).

When this bit is set, the change in break bit in the ISR (ISR[6 or 2]) is set. ISR[6 or 2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In special 'wake-up mode', the parity error bit stores the received A/D bit.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SR[3] – Transmitter Empty (TxEMT)
This bit will be set when the transmitter underruns, i.e., both the transmit holding register and the transmit shift register are empty. This bit and TxRDY are set when transmitter is first enabled after a disable transmitter command or reset. It is set after transmission of the last stop bit of a character, if no character is in the TxFIFO awaiting transmission. It is reset when the TxFIFO is loaded by the CPU, or when the transmitter is disabled.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the TxFIFO is ready to be loaded with a character. This bit is cleared when the TxFIFO is full and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded in the TxFIFO while the transmitter is disabled will not be transmitted.

SR[1] – FIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL is not reset after reading the FIFO once.

SR[0] – Receiver Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RxFIFO, and no more characters are in the FIFO.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, 19.2k, and 38.4k baud.

The selected set of rates is available for use by the receiver and transmitter.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source (see Table 4).

Table 4. ACR[6:4] C/T Clock and Mode Select

[6:4]	Mode	Clock Source
0 0 0	Counter	IO pin
0 0 1	Counter	IO pin divided by 16
0 1 0	Counter	TxC–1X clock of the transmitter A or C
0 1 1	Counter	Crystal or external clock (X1/CLK) divided by 16
1 0 0	Timer	IO pin
1 0 1	Timer	IO pin divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – IO1b, IO0b, IO1a, IO0a Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register, ISR[7], to be set. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IO1b, IO0b, IO1a, IO0a Change-of-State
These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IO1b, IO0b, IO1a, IO0a Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the inputs pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output is asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR.

ISR[7] – IO Change-of-State
This bit is set when a change-of-state occurs at the IO1b, IO0b, IO1a, IO0a input pins. It is reset when the CPU reads the IPCR.

ISR[6] – Channel b Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[5] – Receiver Ready or FIFO Full Channel b
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read.

If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receiver shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[4] – Transmitter Ready Channel b
This bit is a duplicate of TxRDY (SR[2]).

ISR[3] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. It is initialized to '0' when the chip is reset.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[2] – Channel a Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[1] – Receiver Ready or FIFO Full Channel a
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be ready by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receiver shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[0] – Transmitter Ready Channel a
This bit is a duplicate of TxRDY (SR[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the INTRN output is asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a subsequent start counter command causes the C/T to terminate the current timing cycle and to begin a new cycle using the values in the CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command read with A3–A0 = H'F'). The command, however, does not stop the C/T. The generated square wave is output on an IO pin if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching the terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If IO is programmed to be the output of the C/T, the output remains High until the terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter is read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

I/O LOGIC

Another difference between the QUART and most other Signetics UART products is that the QUART has four pins for each channel which can be inputs or outputs, while previous Signetics UART devices have varying number of fixed-direction input pins and output pins.

IPR (for DUART ab)

3b	2b	3a	2a	1b	0b	1a	0a
1	1	1	1	1	1	1	1

The state of all eight pins for each DUART can always be read via the IPR.

IPCR (for DUART ab)

Δ1b	Δ0b	Δ1a	Δ0a	1b	0b	1a	0a
1	1	1	1	1	1	1	1

IPR and IPCR are analogous to registers of the same name in the SCC2698.

IOPCR (for DUART ab)

IO3x use	IO2x use	IO1x use	IO0x use
2	2	2	2

The configuration of I/O pins as inputs or outputs in each UART channel is controlled by a register called IOPCR (I/O Port Control Register). This register generally replaces the OPCR (Output Port Control Register) of previous Signetics UARTs. The coding of the IOPCR control fields is shown in Figure 4.

OPR (for DUART ab)

3b	2b	3a	2a	1b	0b	1a	0a
1	1	1	1	1	1	1	1

For I/O pins that are selected for output port control in IOPCR, this register controls their

state. The OPRs are read/write at address 0Ch and 1Ch. Read/write output registers optimize the changing of some bits without affecting the state of other bits in the register.

Each of a channel's 4 I/O lines are configured to be inputs upon reset. Each UART channel has two inputs, IO0 and IO1, that are equipped with change detection. The ACR (Auxiliary Control Register) controls interrupt generation by change of state of these inputs. ACR[0] enables change of state interrupt on IO0a, ACR[1] on IO1a, ACR[2] on IO0b and ACR[3] on IO1b.

IOPCR Control of IO3:0 Pins for Each Channel

IOPCR7 IOPCR6	IOPCR5 IOPCR4	IOPCR3 IOPCR2	IOPCR1 IOPCR0
IO3x Control	**IO2x Control**	**IO1x Control**	**IO0x Control**
00 = GPI or TxC in	00 = GPI or RxC in	00 = (Note 2)	00 = GPI or CTS in
01 = OPR3 out	01 = OPR2 (Note 1)	01 = OPR1 out	01 = OPR0 out
10 = TxC16X out	10 = RxC1X out	10 = (Note 3)	10 = TxC1X out
11 = TxC1X out	11 = RxC16X out	11 = RxC1X out	11 = TxC16X out

Note 1: Bit 2 of the OPR is the Request to Send function that is affected by the Assert and Negate RTS commands in CRA or CRB, and by the TxRTS feature if MR2x5 is 1, as well as by writing OPR. The RxRTS function, which is activated if MR1x7 is 1, does not affect OPR2 but merely blocks the output signal whenever the Rx FIFO is full.

Note 2: As for the other three pins, a 00 value in this field makes the IO1 pin an input. IO1 can always be used as a General Purpose Input (GPI). IO1a and IO1c can be used as CTI depending on how ACR6:4 is programmed. If OPCR7:6 is not 00, IO1 can be used as TxC depending on how CSRx3:0 is programmed.

Note 3: A 10 value in this field makes IO1b and IO1d output the CTO signal, and makes IO1a and IO1c output RxC16x.

QUART REGISTERS vs 2698B

As shown in Table 1, registers present in the SCC2698's first four channels are present in the QUART. Furthermore, they retain the same addresses and functionally that they possess in the 2698. Thus, the QUART is compatible with existing software except for the multi-purpose I/O and some interrupt related functions.

Revised Formats for Existing Registers

The function of bit 6 of the MR1 register (RxINT Select) has been superseded by the new interrupt priority logic. This bit is now reserved.

The ACR has analogous but slightly different functions for bits 3:0 as described in the I/O Logic section.

The new format of the IOPCR, shown above, does not provide for the power down bit. The power down function is now set by a write to QUART address 24H; power up is a write to address 25H.

New Registers Required

Current Interrupt Register (CIR)

# Bytes	Type	Chan #
3	3	2

The Channel # field indicates which of the four UARTs has the highest priority interrupt currently outstanding, while the Type field indicates its source within the UART. The Type field is encoded as follows:

000 No Interrupt
001 Change of State
x10 Transmit available
011 Receive available, no error
100 Receiver break change
101 Counter/Timer
111 Receive available, w/errors

With Type = x11, the # Bytes field indicates the count of received bytes available for reading, while with Type = x10 it indicates the number of bytes that can be written to the transmit FIFO. With Type = x0x, the # Bytes field is undefined.

The CIR is Read only at address 28H.

Global Interrupt Byte Count (GIBC)

00000	# Bytes
5	3

The GIBC is not an actual register but simply outputs the interrupting UART's transmit or receive byte counter value. The count, accurate at the time IACKN asserts, is captured in the CIR. The high order 5 bits are read as '0'. The GIBC is read only at address 2AH.

Global Interrupt Byte Count (GIBC)

Received Data
8

Like the GIBC,, no physical register implementation exists. The correct receiver's FIFO is popped based on the value of the interrupting channel field of the Current Interrupt Register.

If a receiver is not the cause of the current interrupt, a read of the Global RxFIFO will yield a byte containing all ones and NONE of the UART channels' receive FIFOs will be popped. (IMPORTANT)

The GRxFIFO is Read only at address 2BH.

Global Transmit Holding Register (GTHR)

Data to be Sent
8

Similar to the GRxFIFO, no physical register implementation exists. The byte is pushed into the correct transmitter's FIFO based on the interrupting channel field of the Current Interrupt Register.

If a transmitter is not the cause of the current interrupt, a write to the Global TxFIFO has no effect.

The GTxFIFO is Write only at address 2BH.

Global Interrupting Channel (GICR)

000000	Chan #
6	2

Like the other Global pseudo-registers no hardware register exists. The Channel number field of the Current Interrupt Register padded with leading zeros is output as the GICR. The GICR is Read only at address 29H.

Interrupt Control (ICR)

Threshold	IVC
6	2

The Threshold Field is used by the interrupt comparator to determine if a winning interrupt "bid" should result in interrupting the control processor. This field resets to 3Fh.

The IVC field controls what kind of vector the QUART returns to the control processor during an Interrupt Acknowledge cycle:

00 Output contents of Interrupt Vector Register
01 Output 6 MSBs of IVR and Channel number as 2 LSBs
10 Output 3 MSBs of IVR and Channel number and Interrupt Type
11 Disable generation of vector during IACK cycle

This field reset to 00 and is read/write at address 2CH.

Bidding Control Registers (BCRs)

Rcv'd Break	State Change	C/T
3	3	2

The 3 MSBs determine the priority of Received Break Interrupts; they are reset to 001.

Bits 4:2 determine the priority of Change of Input State interrupts, and are reset to 00.

There is one BCR per UART channel; they can be read or written at addresses 20-23H.

Interrupt Vector (IVR)

Always Used	with IVC = 0x	w/IVC > 00
3	3	2

Holds the constant bits of the interrupt acknowledge vector. As shown, the three MSBs are always used, while the less significant bits can be replaced by the interrupt type code and/or Channel code bits. The IVR is write only at address 29H.

OPEN ISSUES

This specification is Preliminary. Final performance values will follow characterization. AC parameters have been taken from first fabrication lots.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{DD} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation	1	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{IL} V_{IH} V_{IH}	Input low voltage Input high voltage (except X1/CLK) Input high voltage (X1/CLK)		 2.0 0.8V_{CC}		0.8	V V V
V_{OL} V_{OH}	Output Low voltage Output High voltage (except OD outputs)	I_{OL} = 4.0mA I_{OH} = –400µA	 0.8V_{CC} 0.9V_{CC}		0.4	V V V
I_{IL} I_{IH}	Input current Low, I/O ports Input current High, I/O ports	V_{IN} = 0 V_{IN} = V_{CC}	–10		 1	µA µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	–1		1	µA
I_{ILX1} I_{IHX1}	X1/CLK input Low current X1/CLK input High current	V_{IN} = GND, X2 = open V_{IN} = V_{CC}, X2 = open	–100		 100	µA µA
I_{OZH} I_{OZL}	Output off current High, 3-State data bus Output off current Low, 3-State data bus	V_{IN} = V_{CC} V_{IN} = 0	 –1		10 1	 µA
I_{ODL} I_{ODH}	Open-drain output Low current in off state: IRQN Open-drain output Low current in off state: IRQN	V_{IN} = V_{CC} V_{IN} = 0	–10		 1	 µA
I_{CC}	Power supply current Operating mode	TTL input levels 25°C with X1 = 4MHz			50	mA
	Power down mode				TBD	µA

NOTES:

1. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of V_{IL} and V_{IH}, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4] T_A = 20°C; V_{CC} = 5V ± 10%, unless otherwise specified.

SYMBOL	FIGURE	PARAMETER	LIMITS Min	Typ	Max	UNIT
Reset timing						
t_{RES}	5	Reset pulse width	200			ns
IO Port timing[8]						
t_{PS}	6	IO input setup time before RDN Low	0			ns
t_{PH}	6	IO input hold time after RDN High	0			ns
Interrupt timing						
t_{IR}	7	INTRN negated or IO output High from: (With respect to a 3.6864MHz clock on pin X1/CLK)				
		Read RHR (RxRDY/FFULL interrupt)			100	ns
		Write THR (TxRDY interrupt)			100	ns
		Reset command (break change interrupt)			100	ns
		Reset command (IO change interrupt)			100	ns
		Stop C/T command (counter interrupt)			100	ns
		Write IMR (clear of interrupt mask bit)			100	ns
Clock timing						
t_{CLK}	8	X1/CLK low time/high time	125/100			ns
t_{CLK}	8	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	8	Counter/timer clock high or low time	60			ns
f_{CTC}	8	Counter/timer clock frequency	0[11]		8	MHz
t_{RX}	8	RxC high or low time	30			ns
f_{RX}	8	RxC frequency (16X)	0[11]		16	MHz
		RxC frequency (1X)	0[11]		1.0	MHz
t_{TX}	8	TxC high or low time	200			ns
f_{TX}	8	TxC frequency (16X)	0[11]		16	MHz
		TxC frequency (1X)	0[11]		1.0	MHz
Transmitter timing						
t_{TXD}	9	TxD output delay from TxC low 16X			120	ns
t_{TCS}	9	TxD output delay from TxC output	0		50	ns
Receiver timing						
t_{RXS}	10	RxD data setup time to RxC high	100			ns
t_{RXH}	10	RxD data hold time from RxC high	100			ns

NOTES:

1. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of V_{IL} and V_{IH}, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for interrupt and IO outputs: C_L = 50pF, forced current for V_{OL} = 5.3mA; forced current for V_{OH} = 400µA, R_L = 2.7kΩ to V_{CC}. Test conditions for rest of outputs: C_L = 150pF.

AC ELECTRICAL CHARACTERISTICS (PRELIMINARY)[4] T_A = 20°C; V_{CC} = 5V ± 10%, unless otherwise specified.

NO.	FIGURE	CHARACTERISTIC	LIMITS Min	Typ	Max	UNIT
1	1a	Setup: A[5:0] valid to CEN low	10			ns
2	1a	Hold: A[5:0] valid after CEN low	30			ns
3	1a	Access: Later of CEN low and RDN low, to Dnn valid (read)			110	ns
		Later of CEN low and (RDN or WRN as applicable) low, to DACKN low Normal Operation:			70 + 2 X1 edges	ns
4	1a	From Power Down:			150	ns
5	1a	Earlier of CEN high or RDN high, to Dnn released (read)[1]	0		45	ns
6	1a	Earlier of CEN high or (RDN or WRN as applicable) high, to DACKN released	0		30	ns
7	1a	Earlier of CEN high or (RDN or WRN as applicable) high, in one cycle, to later of CEN low and (RDN or WRN as applicable) low, for the next cycle	55			ns
8	1a	Setup, Dnn valid (write) to later of CEN low and WRN low[2]	–30			ns
9	1a	Later of CEN low and WRN low, to earlier of CEN high or WRN high	110			ns
10	1a	Hold: Dnn valid (write) after DACKN low, CEN high or WRN high[3]	0			ns

NOTES:
1. The minimum time indicates that read data will remain valid until the bus master drives CEN and/or RDN to high.
2. The fact that this parameter is negative means that the Dnn line may actually become valid after CEN and WRN are both low.
3. In a Write operation, the bus master must hold the write data valid either until drives CEN and/or WRN to high, or until the QUART drives DACKN to low, whichever comes first.
4. Test condition for interrupt and IO outputs: C_L = 50pF, forced current for V_{OL} = 5.3mA; forced current for V_{OH} = 400µA, R_L = 2.7kΩ to V_{CC}. Test conditions for rest of outputs: C_L = 150pF.

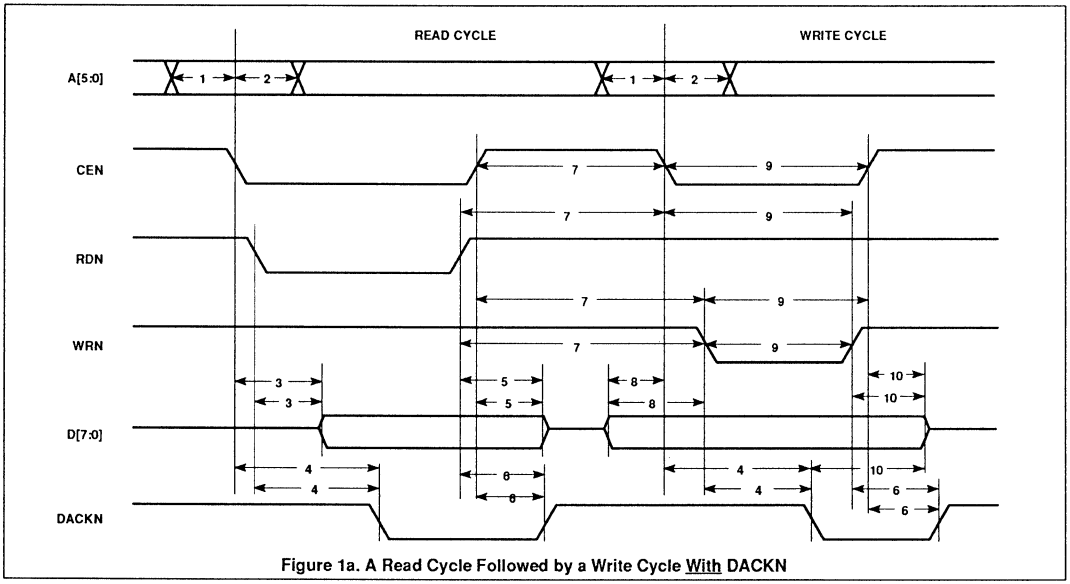


Figure 1a. A Read Cycle Followed by a Write Cycle With DACKN

AC ELECTRICAL CHARACTERISTICS (PRELIMINARY)[1] $T_A = 0°C$; $V_{CC} = 5V \pm 10\%$, unless otherwise specified.

NO.	FIGURE	CHARACTERISTIC	LIMITS			UNIT
			Min	Typ	Max	
1	1b	A[5:0] Setup time to RDN WRN Low	10			ns
2	1b	A[5:0] Hold time from RDN WRN Low	30			ns
3	1b	CEN Setup time to RDN WRN Low[2]	0			ns
4	1b	CEN Hold time from RDN WRN High[2]	0			ns
5	1b	RDN WRN Pulse width Low	110			ns
6	1b	D[7:0] Data Valid after CEN and RDN Low			110	ns
7	1b	D[7:0] Data bus floating after RDN or CEN High			45	ns
8	1b	D[7:0] Data bus setup time before WRN or CEN High	75			ns
9	1b	D[7:0] Hold time after WRN or CEN High	0			ns
10	1b	Time between Reads and/or Writes[3]	55			ns

NOTES:
1. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
2. The RDN signal must be negated for t_{RWD} guarantee that any status register changes are valid.
3. Consecutive write operations to the command register require at least three rising edges of the X1 clock between writes.

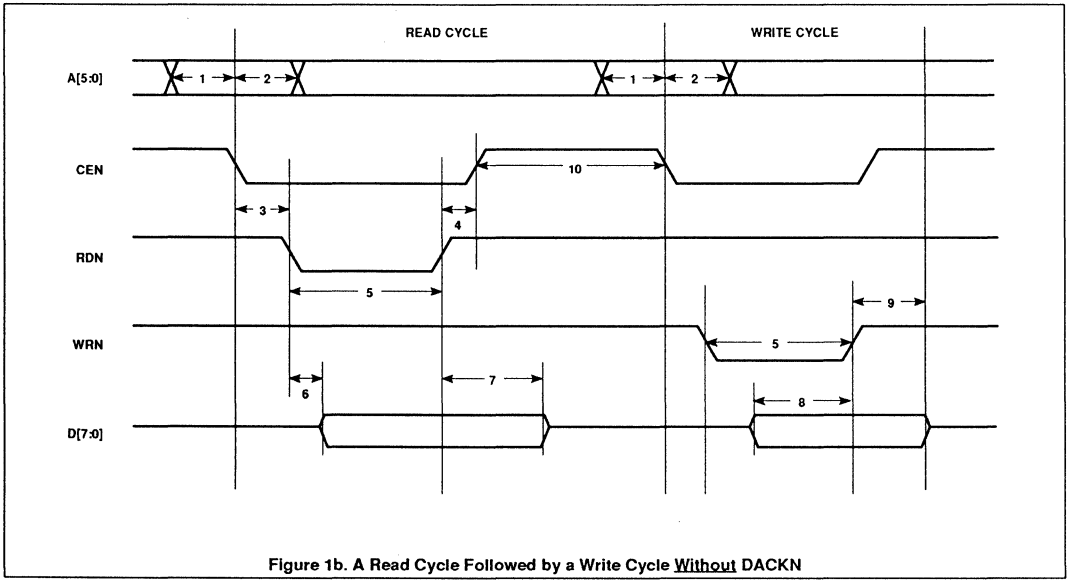


Figure 1b. A Read Cycle Followed by a Write Cycle Without DACKN

AC ELECTRICAL CHARACTERISTICS (PRELIMINARY) $T_A = 0°C$; $V_{CC} = 5V \pm 10\%$, unless otherwise specified.

NO.	FIGURE	CHARACTERISTIC	LIMITS			UNIT
			Min	Typ	Max	
1	1c	D[7:0] Valid after IACKN Low			110	ns
2	1c	DACKN Low after IACKN Low	30		10 + 2 X1 edges	ns
3	1c	D[7:0] floating after IACKN High			45	ns
4	1c	DACKN High after IACKN High			45	ns

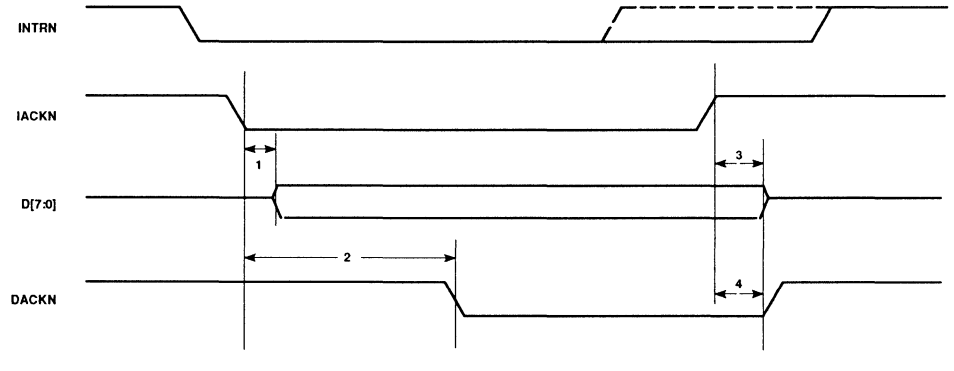


Figure 1c. Interrupt Knowledge (IACKN) Timing

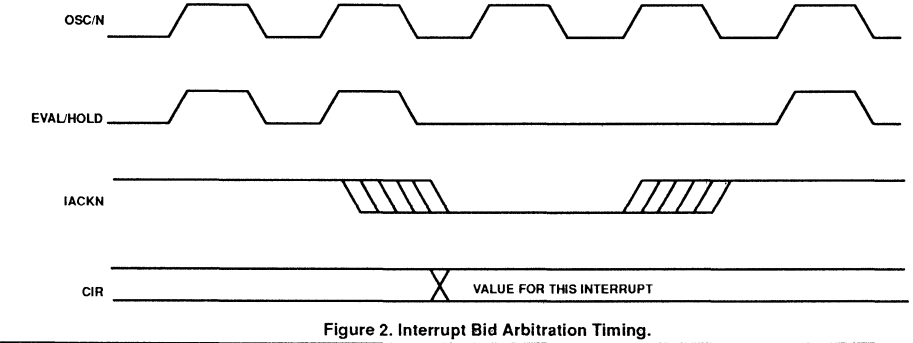


Figure 2. Interrupt Bid Arbitration Timing.

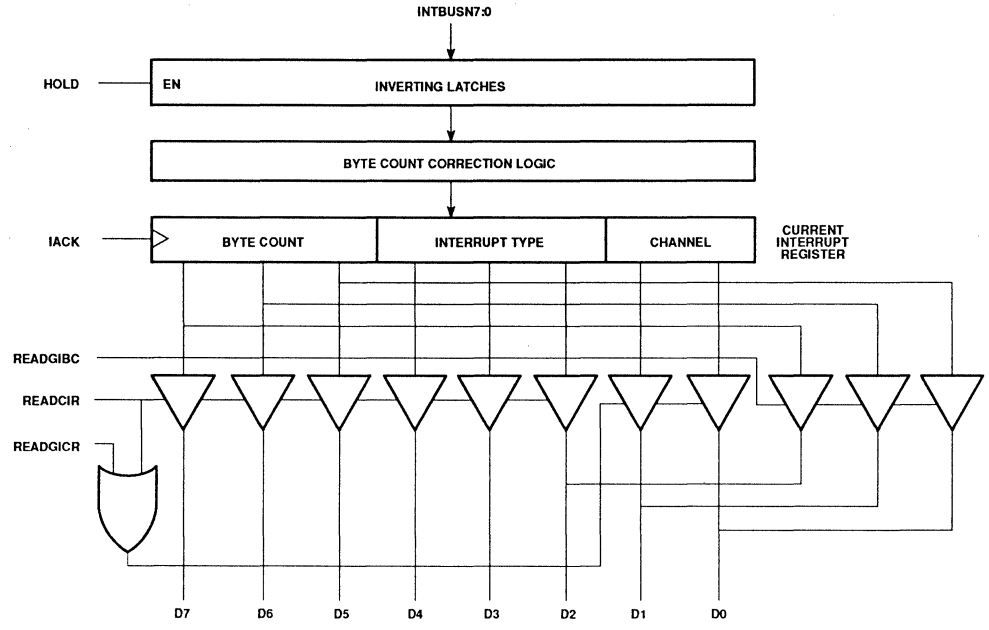


Figure 3. Current Interrupt Register Logic

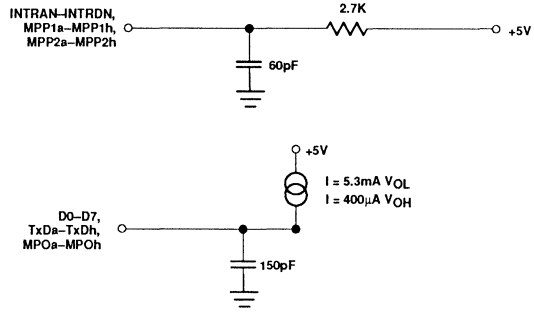


Figure 4. Test Conditions on Outputs

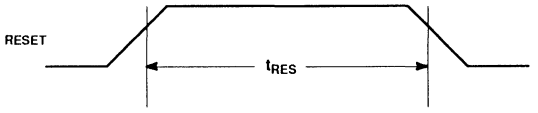


Figure 5. Reset Timing

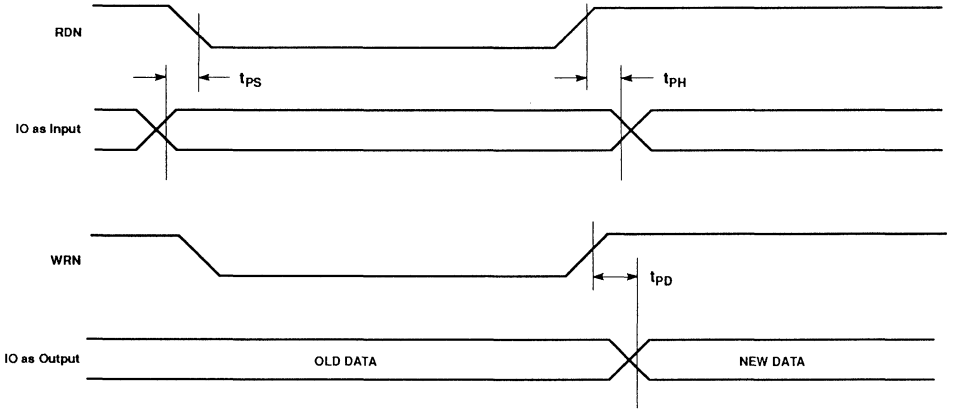
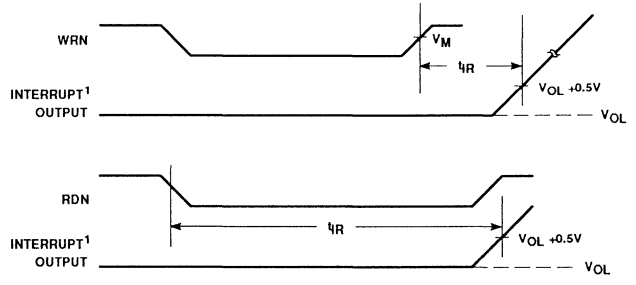


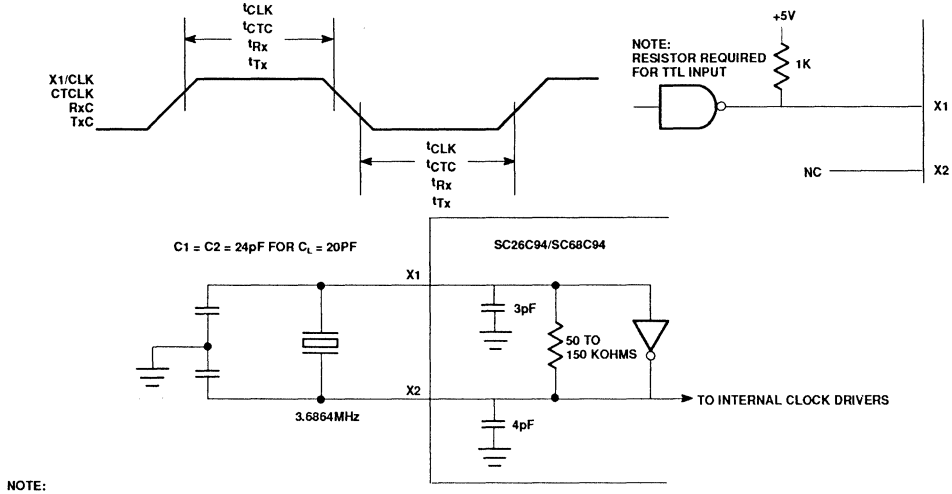
Figure 6. IO Port Timing



NOTES:

1. Includes IO when used as TxRDY or RxDY/FFULL outputs as well as INTRN.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This Point Represents Noise Margin That Assures True Switching Has Occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 7. Interrupt Timing



NOTE:
C1 and C2 should be based on manufacturer's specification.
X1 and X2 parasitic capacitance is 1-2pF and 3-5pF, respectively.

TYPICAL CRYSTAL SPECIFICATION

FREQUENCY:	2 – 4MHZ
LOAD CAPACITANCE (C_L):	12 – 32pF
TYPE OF OPERATION:	PARALLEL RESONANT, FUNDAMENTAL MODE

Figure 8. Clock Timing

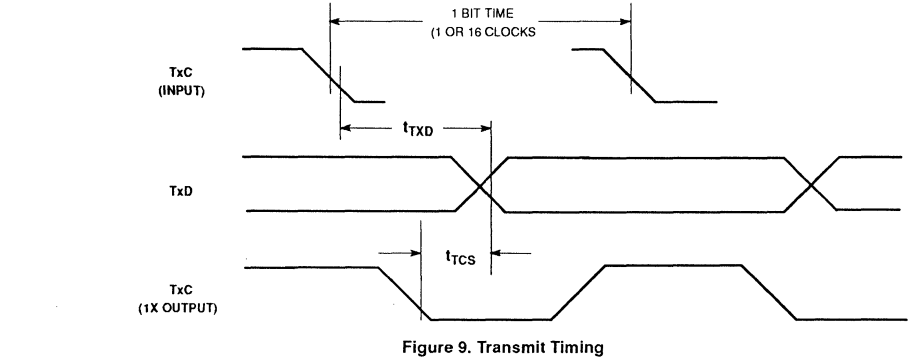


Figure 9. Transmit Timing

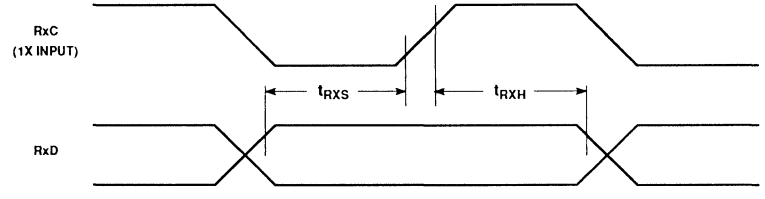


Figure 10. Receive Timing

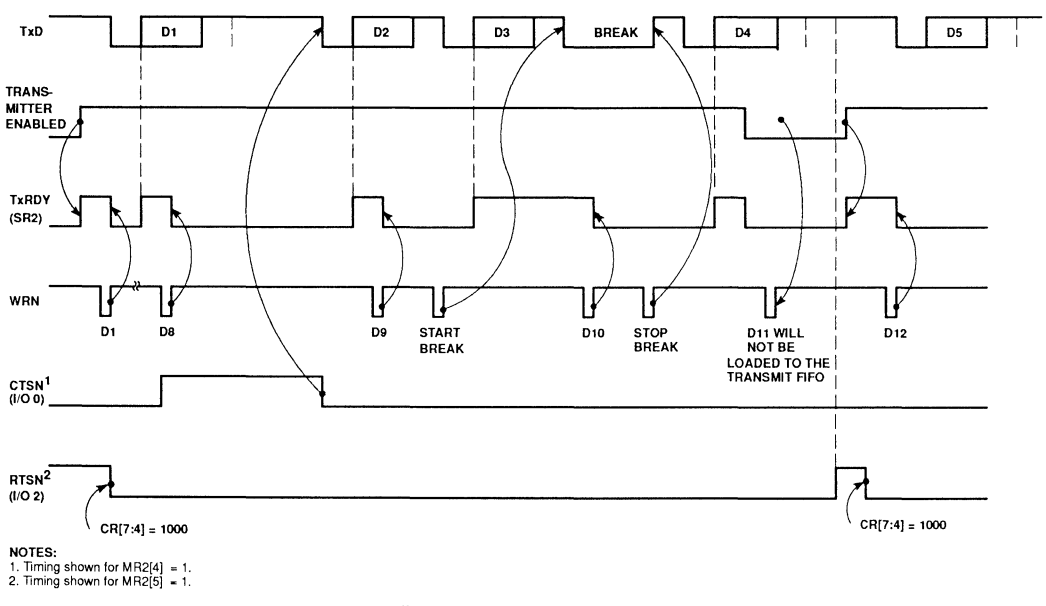


Figure 11. Transmitter Timing

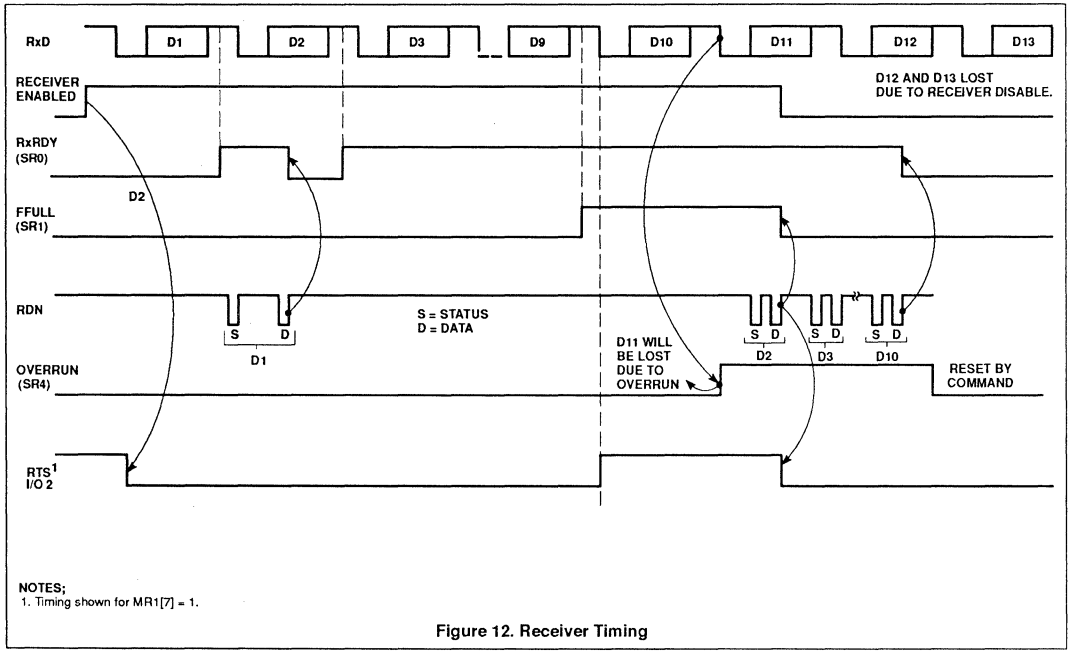


Figure 12. Receiver Timing

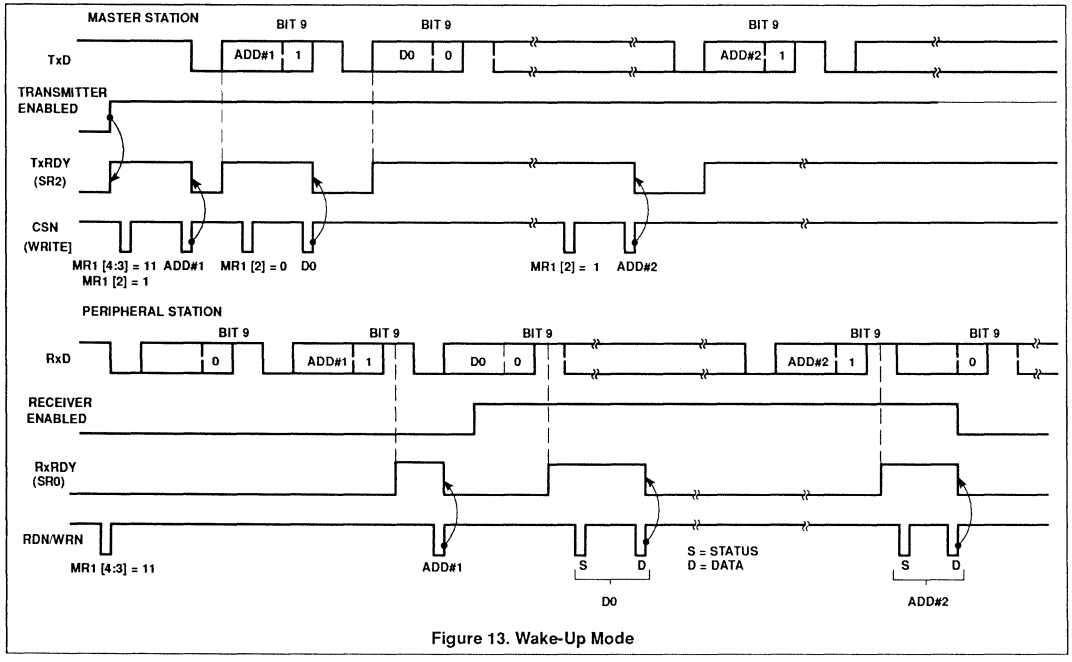


Figure 13. Wake-Up Mode

Philips Components-Signetics

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Date of Issue	November 12, 1990
Status	Product Specification
Data Communication Products	

SCC2698B

Enhanced octal universal asynchronous receiver/transmitter (Octal UART)

DESCRIPTION

The SCC2698B Enhanced Octal Universal Asynchronous Receiver/Transmitter (Octal UART) is a single chip MOS-LSI communications device that provides eight full-duplex asynchronous receiver/transmitter channels in a single package. It is fabricated with CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of each receiver and transmitter can be selected independently as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the Octal UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The Octal UART is fully TTL compatible and operates from a single +5V power supply.

The SCC2698B is an upwardly compatible version of the 2698A Octal UART. In PLCC packaging, it is enhanced by the addition of receiver ready or FIFO full status outputs, and transmitter empty status outputs for each channel on 16 multipurpose I/O pins. The multipurpose I/O pins of the SCC2698B were inputs only on the SCC2698A.

FEATURES

- Eight full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud Non-standard rates to 115.2K baud
  - User-defined rates from the programmable counter/timer associated with each of four blocks
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Four multi-function programmable 16-bit counter/timers
- Four interrupt outputs with eight maskable interrupting conditions for each output
- Receiver ready/FIFO full and transmitter ready status available on 16 multi-function pins in PLCC package
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply with low power mode

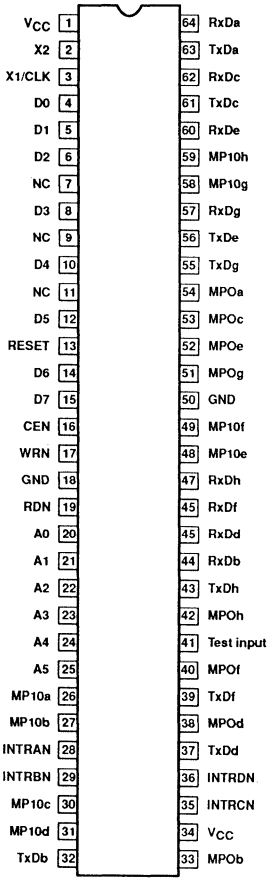
ORDERING INFORMATION

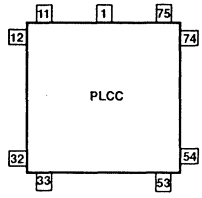
PACKAGES	V_{CC} = +5V ±5%, T_A = 0°C to +70°C	V_{CC} = +5V ±5%, T_A = –40°C to +85°C
Plastic DIP	SCC2698BC1N64	SCC2698BA1N64
Plastic Leaded Chip Carrier	SCC2698BC1A84	SCC2698BA1A84

NOTE:
Pin Grid Array (PGA) package version is available from Philips Components Military Division.

Enhanced octal universal asynchronous receiver/transmitter SCC2698B

PIN CONFIGURATIONS

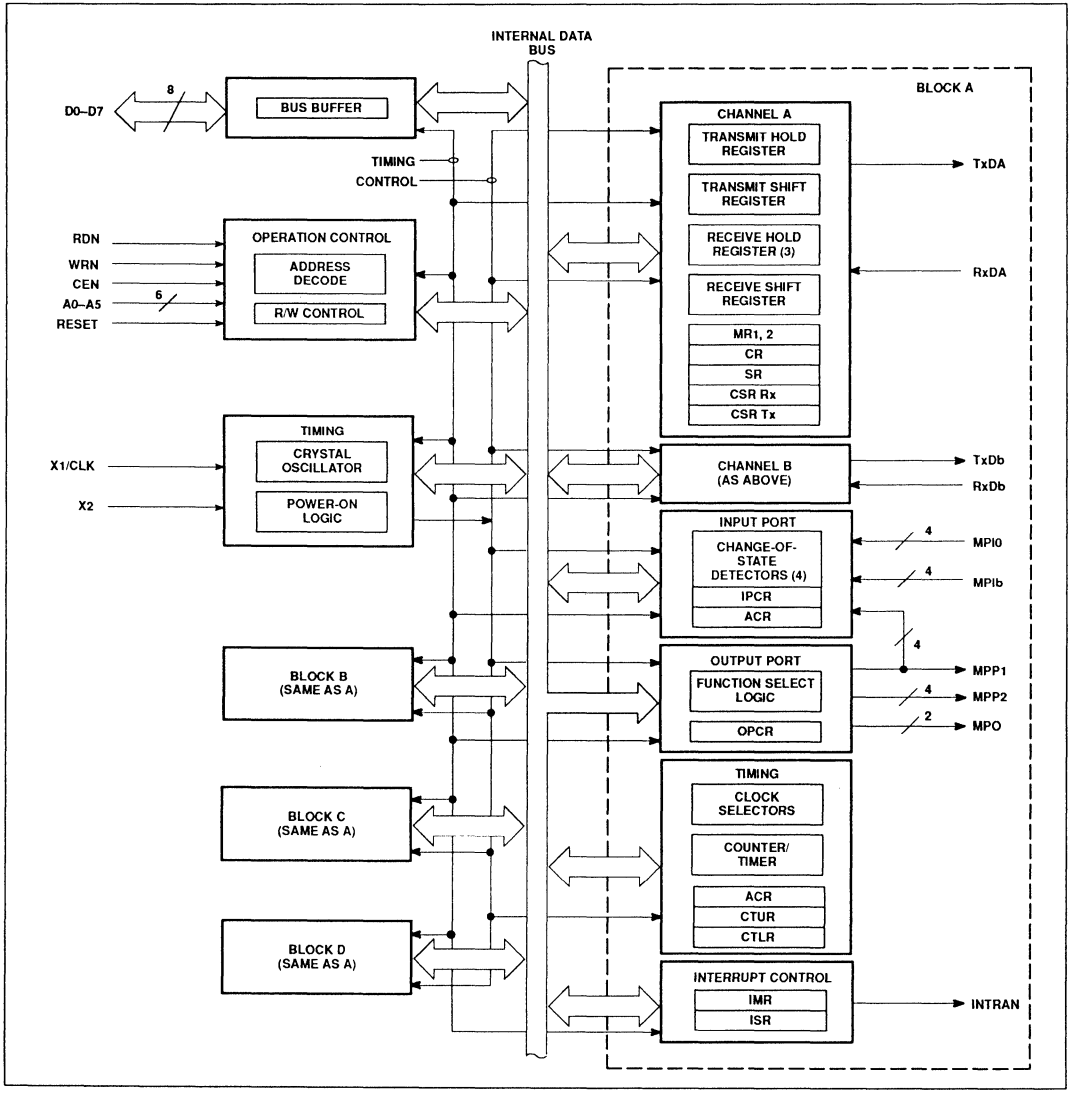




Pin	Function	Pin	Function	Pin	Function
1	TxDa	29	A3	57	RxDd
2	MPP2g	30	MPP2b	58	RxDf
3	RxDa	31	A4	59	RxDh
4	MPP2h	32	A5	60	MPI1e
5	V_{CC}	33	MPI0a	61	MPI0e
6	X2	34	MPI0b	62	MPI1f
7	X1/CLK	35	INTRAN	63	MPI0f
8	D0	36	INTRBN	64	MPP1e
9	D1	37	MPI0c	65	GND
10	D2	38	MPI1c	66	MPP1f
11	D3	39	MPI0d	67	MPOg
12	D4	40	MPI1d	68	MPP2e
13	D5	41	TxDb	69	MPOe
14	MPI1a	42	MPP1c	70	MPP2f
15	RESET	43	MPOb	71	MPOc
16	D6	44	MPP1d	72	MPOa
17	D7	45	V_{CC}	73	TxDg
18	CEN	46	INTRCN	74	TxDe
19	WRN	47	INTRDN	75	RxDg
20	GND	48	MPP2c	76	MPI0g
21	MPI1b	49	TxDd	77	MPI0h
22	RDN	50	MPP2d	78	MPI1g
23	A0	51	MPOd	79	RxDe
24	MPP1a	52	TxDf	80	MPIh
25	A1	53	MPOf	81	TxDc
26	MPP1b	54	MPOh	82	MPP1g
27	A2	55	TxDh	83	RxDc
28	MPP2a	56	RxDb	84	MPP1h

Enhanced octal universal asynchronous receiver/transmitter SCC2698B

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	LDCC		
D0–D7	4–6, 8, 10, 12, 14, 15	8–13, 16, 17	I/O	**Data Bus:** Active–High 8-bit bidirectional 3-State data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the Octal UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is High, the data bus is in the 3-State condition.
CEN	16	18	I	**Chip Enable:** Active-Low input. When Low, data transfers between the CPU and the Octal UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A5 inputs. When CEN is High, the Octal UART is effectively isolated from the data bus and D0–D7 are placed in the 3-State condition.
WRN	17	19	I	**Write Strobe:** Active-Low input. A Low on this pin while CEN is Low causes the contents of the data bus to be transferred to the register selected by A0–A5. The transfer occurs on the trailing (rising) edge of the signal.
RDN	19	22	I	**Read Strobe:** Active-Low input. A Low on this pin while CEN is Low causes the contents of the register selected by A0–A5 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN.
A0–A5	20–25	23, 25, 27, 29, 31, 32	I	**Address Inputs:** Active-High address inputs to select the Octal UART registers for read/write operations.
RESET	13	15	I	**Reset:** Master reset. A High on this pin clears the status register (SR), clears the interrupt mask register (IMR), clears the interrupt status register (ISR), clears the output port configuration register (OPCR), places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (High) state, and stops the counter/timer. Clears power-down mode and interrupts.
INTRAN–INTRDN	28, 29, 35, 36	35, 36, 46, 47	O	**Interrupt Request:** This active-Low open drain output is asserted on occurrence of one or more of eight maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s).
X1/CLK	3	7	I	**Crystal 1:** Crystal or external clock input. When using the crystal oscillator, this pin serves as the connection for one side of the crystal. If a crystal is not used, an external clock is supplied at this input. An external clock (or crystal) is required even if the internal baud rate generator is not utilized. This clock is used to drive the internal baud rate generator, as an optional input to the timer/counter, and to provide other clocking signals required by the chip.
X2	2	6	I	**Crystal 2:** Connection for other side of crystal. If an external source is used instead of a crystal, this connection should be left open (see Figure 7).
RxDa–RxDh	64, 44, 62, 45, 60, 46, 57, 47	3, 56, 83, 57, 79, 58, 75, 59	I	**Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock. If internal clock is used, the RxD input is sampled on the rising edge of the RxC1x signal as seen on the MPO pin.
TxDa–TxDh	63, 32, 61, 37, 56, 39, 55, 43	1, 41, 81, 49, 74, 52, 73, 55	O	**Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is idle or disabled and when the Octal UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock. If internal clock is used, the TxD output changes on the falling edge of the TxC1x signal as seen on the MPO pin.
MPOa–MPOh	54, 33, 53, 38, 52, 40, 51, 42	72, 43, 71, 51, 69, 53, 67, 54	O	**Multi-Purpose Output:** Each of the four DUARTS has two MPO pins. One of the following eight functions can be selected for this output pin by programming the OPCR (output port configuration register). Note that reset conditions MPO pins to RTSN. **RTSN –** Request to send active-Low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full. RTSN is an internal signal which normally represents the condition of the receiver FIFO not full, i.e., the receiver can request more data to be sent. However, it can also be controlled by the transmitter empty and the commands 8h and 9h written to the CR (command register). **C/TO –** The counter/timer output. **TxC1X –** The 1X clock for the transmitter. **TxC16X –** The 16X clock for the transmitter. **RxC1X –** The 1X clock for the receiver. **RxC16X –** The 16X clock for the receiver. **TxRDY –** Transmitter holding register empty signal. **RxRDY/FFULL –** Receiver FIFO not empty/full signal.
MPI0a–MPI0h	26, 27, 30, 31, 48, 49, 58, 59	33, 34, 37, 39, 61, 63, 76, 77	I	**Multi-Purpose Input 0:** This pin (one in each UART) is programmable. Its state can always be read through the IPCR bit 0, or the IPR bit 0. **CTSN:** By programming MR2[4] to a 1, this input will also control the clear-to-send functions. It is active low. This pin is provided with a change-of-state detector.

Enhanced octal universal asynchronous receiver/transmitter SCC2698B

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	LDCC		
MPI1a–MPI1h	NC	14, 21, 38, 40, 60, 62, 78, 80	I	**Multi-Purpose Input 1:** This pin (one for each unit) is programmable. Its state can always be determined by reading the IPCR bit 1 or IPR bit 1. **C/TCLK** – By programming MR2[5] to a 1, this input will serve as the external clock for the counter/timer 2. This occurs only for channels a, c, e, and g since there is one counter/timer 2 for each DUART block. This pin is provided with a change-of-state detector.
MPP1a–MPP1h	NC	24, 26, 42, 44, 64, 66, 82, 84	I/O	**Multi-Purpose Pin 1:** This pin (one for each UART) is programmed to be an input or an output according to the state of OPCR[7]. (0 = input, 1 = output). The state of the multi-purpose pin can always be determined by reading the IPR. When programmed as an input, it will be the transmitter clock (TxCLK). It will be 1x or 16x according to the clock select registers (CSR[3.0]). When programmed as an output, it will be the status register TxRDY bit. As an output, it will be an open drain.
MPP2a–MPP2h	NC	28, 30, 48, 50, 68, 70, 2, 4	I/O	**Multi-Purpose Pin 2:** This pin (one for each UART) is programmed to be an input or an output according to the state of OPCR[7]. (0 = input, 1 = output). The state of the multi-purpose pin can always be determined by reading the IPR. When programmed as an input, it will be the receiver clock (RxCLK). It will be 1x or 16x according to the clock select registers (CSR[7:4). When programmed as an output, it will be the status register RxRDY/FIFO full bit. As an output, it will be an open drain.
Test Input	41	–	I	**Test Input:** This pin is used as an input for test purposes at the factory while in test mode. This pin can be treated as 'N/C' by the user. It can be tied high, tied low, or left open.
V_{CC}	1, 34	5, 45	I	**Power Supply:** +5V supply input.
GND	18, 50	20, 65	I	**Ground**

BLOCK DIAGRAM

As shown in the block diagram, the Octal UART consists of: data bus buffer, interrupt control, operation control, timing, and eight receiver and transmitter channels. The eight channels are divided into four different blocks, each block independent of each other (see Figure 1).

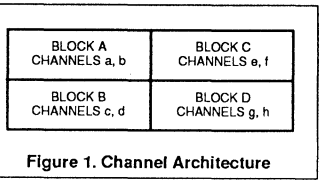


Figure 1. Channel Architecture

Channel Blocks

There are four blocks (Figure 1), each containing two sets of receiver/transmitters. In the following discussion, the description applies to Block A which contains channels a and b. However, the same information applies to all channel blocks.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the Octal UART.

Interrupt Control

A single interrupt output per block (INTRN) is provided which is asserted on occurrence of any of the following internal events:

–Transmit holding register ready for each channel

–Receive holding register ready or FIFO full for each channel

–Change in break received status for each channel

–Counter reached terminal count

–Change in MPI input

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR can be programmed to select only certain conditions, of the above, to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. However, the bits of the ISR are not masked by the IMR. The transmitter ready status and the receiver ready or FIFO full status can be provided on MPP1a, MPP1b, MPP2a, and MPP2b by setting OPCR[7]. these outputs are not masked by IMR.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers 1 and 2 are accessed via an auxiliary pointer. The pointer is set to MR1 by RESET or by issuing a reset pointer command via the command register. Any read or write of the mode register while the pointer is at MR1 switches the pointer to MR2. The pointer then remains at MR2 so that subsequent accesses are to MR2, unless the pointer is reset to MR1 as already described.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer for each block, and two clock selectors.

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1 must be driven and X2 left floating as shown in Figure 7. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied even if the internal BRG is not used.

Table 1. Register Addressing

Units A and B								Units E and F							
A5	A4	A3	A2	A1	A0	READ (RDN=0)	WRITE (WRN=0)	A5	A4	A3	A2	A1	A0	READ (RDN=0)	WRITE (WRN=0)
0	0	0	0	0	0	MR1a, MR2a	MR1a, MR2a	1	0	0	0	0	0	MR1e, MR2e	MR1e, MR2e
0	0	0	0	0	1	SRa	CSRa	1	0	0	0	0	1	SRe	CSRe
0	0	0	0	1	0	Reserved*	CRa	1	0	0	0	1	0	Reserved*	CRe
0	0	0	0	1	1	RHRa	THRa	1	0	0	0	1	1	RHRe	THRe
0	0	0	1	0	0	IPCRA	ACRA	1	0	0	1	0	0	IPCRC	ACRC
0	0	0	1	0	1	ISRA	IMRA	1	0	0	1	0	1	ISRC	IMRC
0	0	0	1	1	0	CTUA	CTURA	1	0	0	1	1	0	CTUC	CTURC
0	0	0	1	1	1	CTLA	CTLRA	1	0	0	1	1	1	CTLC	CTLRC
0	0	1	0	0	0	MR1b, MR2b	MR1b, MR2b	1	0	1	0	0	0	MR1f, MR2f	MR1f, MR2f
0	0	1	0	0	1	SRb	CSRb	1	0	1	0	0	1	SRf	CSRf
0	0	1	0	1	0	Reserved*	CRb	1	0	1	0	1	0	Reserved*	CRf
0	0	1	0	1	1	RHRb	THRb	1	0	1	0	1	1	RHRf	THRf
0	0	1	1	0	0	Reserved*	Reserved*	1	0	1	1	0	0	Reserved*	Reserved*
0	0	1	1	0	1	Input port A	OPCRA	1	0	1	1	0	1	Input port C	OPCRC
0	0	1	1	1	0	Start C/T A	Reserved*	1	0	1	1	1	0	Start C/T C	Reserved*
0	0	1	1	1	1	Stop C/T A	Reserved*	1	0	1	1	1	1	Stop C/T C	Reserved*
Units C and D								**Units G and H**							
0	1	0	0	0	0	MR1c, MR2c	MR1c, MR2c	1	1	0	0	0	0	MR1g, MR2g	MR1g, MR2g
0	1	0	0	0	1	SRc	CSRc	1	1	0	0	0	1	SRg	CSRg
0	1	0	0	1	0	Reserved*	CRc	1	1	0	0	1	0	Reserved*	CRg
0	1	0	0	1	1	RHRc	THRc	1	1	0	0	1	1	RHRg	THRg
0	1	0	1	0	0	IPCRB	ACRB	1	1	0	1	0	0	IPCRD	ACRD
0	1	0	1	0	1	ISRB	IMRB	1	1	0	1	0	1	ISRD	IMRD
0	1	0	1	1	0	CTUB	CTURB	1	1	0	1	1	0	CTUD	CTURD
0	1	0	1	1	1	CTLB	CTLRB	1	1	0	1	1	1	CTLD	CTLRD
0	1	1	0	0	0	MR1d, MR2d	MR1d, MR2d	1	1	1	0	0	0	MR1h, MR2h	MR1h, MR2h
0	1	1	0	0	1	SRd	CSRd	1	1	1	0	0	1	SRh	CSRh
0	1	1	0	1	0	Reserved*	CRd	1	1	1	0	1	0	Reserved*	CRh
0	1	1	0	1	1	RHRd	THRd	1	1	1	0	1	1	RHRh	THRh
0	1	1	1	0	0	Reserved*	Reserved*	1	1	1	1	0	0	Reserved*	Reserved*
0	1	1	1	0	1	Input port B	OPCRB	1	1	1	1	0	1	Input port D	OPCRD
0	1	1	1	1	0	Start C/T B	Reserved*	1	1	1	1	1	0	Start C/T D	Reserved*
0	1	1	1	1	1	Stop C/T B	Reserved*	1	1	1	1	1	1	Stop C/T D	Reserved*

NOTE:
*Reserved registers should never be read during normal operation since they are reserved for internal diagnostics.

ACR = Auxiliary control register
CR = Command register
CSR = Clock select register
CTL = Counter/timer lower
CTLR = Counter/timer lower register
CTU = Counter/timer upper
CTUR = Counter/timer upper register
MR = Mode register
SR = Status Register
THR = Tx holding register
RHR = Rx holding register
IPCR = Input port change register
ISR = Interrupt status register
IMR = Interrupt mask register
OPCR= Output port configuration registerr

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Thirteen of these are available simultaneously for use by the receiver and transmitter. Eight are fixed, and one of two sets of five can be selected by programming ACR[7]. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection, by the receiver and transmitter, of any of these baud rates or an external timing signal.

There are four C/Ts in the Octal UART, one for each block. The C/T operation is programmed by ACR[6:4]. One of eight timing sources can be used as the input to the C/T. The output of the C/T is available to the clock selectors and can also be programmed by OPCR[2:0] for channel a and OPCR[6:4] for channel b, to be output on the MPOa or MPOb pin respectively.

A register read address is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop counter/timer command for each timer. For example, to issue a stop counter command for the counter-timer in block B, a read of address '1F' must be performed. See Table 1 for register addressing.

In the timer mode, the C/T generates a square wave whose period is twice the number of clock periods loaded into the C/T upper and lower registers. The counter ready bit in the ISR is set once each cycle of the square wave. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be affected. In this mode the C/T

runs continuously and does not recognize the stop C/T command (the command only resets the counter ready bit in the ISR). Receipt of a start C/T command causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR. Counting begins upon receipt of a start counter command. Upon reaching terminal count, the counter ready bit in the ISR is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and the counter ready bit is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command following a stop counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter are read. However, a subsequent start counter command causes the counter to begin a new count cycle using the values in CTUR and CTLR.

Receiver and Transmitter

The Octal UART has eight full-duplex asynchronous receiver/transmitters. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

Registers associated with the communications channel are the mode registers (MR1 and MR2), the clock select register (CSR), the command register (CR), the status register (SR), the transmit holding register (THR), and the receive holding register (RHR).

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the THR. In the 16X clock mode, this also resynchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

The transmitter can be forced to send a break (continuous Low condition) by issuing a start break command via the CR. The break is terminated by a stop break command. If the transmitter is disabled, it continues operating until the characters currently being transmitted and the character in the THR, if any, are completely sent out. Characters cannot be loaded in the THR while the transmitter is disabled.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode).

If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver samples the input. This continues at one bit time intervals, at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The data is then transferred to the RHR and the RxRDY bit in the SR is set to a one. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

TIMEOUT MODE

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know when there is data left in the FIFO, The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after one C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx='Ax', will also clear the counter ready bit and stop the counter until the next character is received.

RECEIVER FIFO

The RHR consists of a first-in-first-out (FIFO) with a capacity of three characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The

RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR, outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit, SR[4], will be set upon receipt of the start bit of the new (overrunning) character.

WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the Octal UART incorporates a special mode which provides automatic wake-up of the receiver through address frame recognition for multiprocessor communications. This mode is selected by programming bits MR1[4:3] to '11'.

In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, whose receivers are normally disabled, examine the received data stream and 'wake-up' the CPU [by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1[2]; MR1[2] = 0 transmits a zero in the A/D bit position which identifies the corresponding data bits as data; MR1[2] = 1 transmits a one in the A/D bit position which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits in the THR.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RHR FIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RHR. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

MULTI-PURPOSE INPUT PIN AND MULTI-PURPOSE I/O PINS

The inputs to this unlatched 8-bit port for each block can be read by the CPU, by performing a read operation as shown in Table 1. A High input results in a logic one, while a Low input results in a logic zero. When the input port pins are read on the 84-pin LLCC, they will appear on the data bus in alternating pairs (i.e., DB0 = MP10a, DB1 = MPI1a, DB2 = MPI0b, DB3 = MPI1b, DB4 = MPP1a, DB5 = MPP2a, DB6 = MPP1b, DB7 = MPP2b. Although this example is shown for input port 'A', all ports will have a similar order).

The MPI pin can be programmed as an input to one of several Octal UART circuits. The function of the pin is selected by programming the appropriate control register. Change-of-state detectors are provided for MPI0 and MPI1 for each channel in each block. A High-to-Low or Low-to-High transition of the inputs lasting longer than 25 to 50µs sets the MPI change-of-state bit in the interrupt status register. The bit is cleared via a command. The change-of-state can be programmed to generate an interrupt to the CPU by setting the corresponding bit in the interrupt mask register.

The input port pulse detection circuitry uses a 38.4KHz sampling clock, derived from one of the baud rate generator taps. This produces a sampling period of slightly more than 25µs (assuming a 3.6864MHz oscillator input). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples be observed at the new logic level. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. (The 50µs time refers to the condition where the change-of-state is just missed and the first change of state is not detected until after an additional 25µs.)

The multi-purpose pins can be programmed as inputs or outputs using OPCR[7]. When programmed as inputs, the functions of the pins are selected by programming the appropriate control registers. When programmed as outputs, the two MPP1 pins (per block) will provide the transmitter ready (TxRDY) status for each channel and the MPP2 pins will provide the receiver ready or FIFO full (RxRDY/FFULL) status for each channel.

MULTI-PURPOSE OUTPUT PIN

This pin can be programmed to serve as a request-to-send output, the counter/timer output, the output for the 1X or 16X transmitter or receiver clocks, the TxRDY output or the RxRDY/FFULL output (see OPCR[2:0] and OPCR[6:4] – MPO Output Select).

REGISTERS

The operation of the Octal UART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is described in Table 1.

The bit formats of the Octal UART registers are depicted in Table 2. These are shown for block A. The bit format for the other blocks is the same.

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via the CR. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Control

This bit controls the deactivation of the RTSN output (MPO) by the receiver. This output is manually asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is reasserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input of the transmitting device.

MR1[6] – Receiver Interrupt Select

This bit selects either the receiver ready status (RxRDY) or the FIFO full status (FFULL) to be used for CPU interrupts.

MR1[5] – Error Mode Select
This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

MR1[4:3] – Parity Mode Select
If 'with parity' or 'force parity' is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1[4:3] = 11 selects the channel to operate in the special wake-up mode.

MR1[2] – Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special 'wake-up' mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select

The Octal UART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled.

Table 2. Register Bit Formats

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

MR1 (Mode Register 1)

RxRTS Control	RxINT Select	Error Mode	Parity Mode	Parity Type	Bits per Character
0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With parity 01 = Force parity 10 = No parity 11 = Special mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

MR2 (Mode Register 2)

Channel Mode	TxRTS Conrol	CTS Enable Tx	Stop Bit Length*
00 = Normal 01 = Auto-echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 4 = 0.813 8 = 1.563 C = 1.813 1 = 0.625 5 = 0.875 9 = 1.625 C = 1.875 2 = 0.688 6 = 0.938 A = 1.688 E = 1.938 3 = 0.750 7 = 1.000 B = 1.750 F = 2.000

NOTE:
*Add 0.5 to values shown above for 0–7, if channel is programmed for 5 bits/char.

CSR (Clock Select Register)

Receiver Clock Select	Transmitter Clock Select
See text	See text

CR (Command Register)

Miscellaneous Commands	Disable Tx	Enable Tx	Disable Rx	Enable Rx
See text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

SR (Status Register)

Rec'd. Break	Framing Error	Parity Error	Overrun Error	TxEMT	TxRDY	FFULL	RxRDY
0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. In character mode, they must be reset when the corresponding data character is read from the FIFO.

OPCR (Output Port Configuration Register)

MPP Function Select	MPOb Pin Function Select	Power–Down Mode	MPOa Pin Function Select
0 = input 1 = output	000 = RTSN 001 = C/TO 010 = TxC (1X) 011 = TxC (16X) 100 = RxC (1X) 101 = RxC (16X) 110 = TxRDY 111 = RxRDY/FF	0 = Off 1 = On *	000 = RTSN 001 = C/TO 010 = TxC (1X) 011 = TxC (16X) 100 = RxC (1X) 101 = RxC (16X) 110 = TxRDY 111 = RxRDY/FF

NOTE:
*Only OPCR[3] in block A controls the power-down mode.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TXD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

When switching in and out of the various modes, the selected mode is activated at the completion of all transmitted and received characters. Likewise, if a mode is deselected, the device will switch out of the mode at the completion of all transmit and/or receive characters.

MR2[5] – Transmitter Request-to–Send Control

This bit controls the deactivation of the RTSN output (MPO) by the transmitter. This output is manually asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the THR (if any) are completely transmitted (includes the programmed number of stop bits if the transmitter is not enabled). This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Verify the next to last character of the message is being sent by waiting until transmitter ready is asserted. Disable transmitter after the last character of the message is loaded in the THR.

Table 2. Register Bit Formats (Continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

ACR (Auxiliary Control Register)

BRG Set Select	Counter/Timer Mode and Source		Delta MPI1bINT	Delta MPI0bINT	Delta MPI1aINT	Delta MPI0aINT
0 = set 1 1 = set 2	See text		0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

IPCR (Input Port Change Register)

Delta MPI1b	Delta MPI0b	Delta MPI1a	Delta MPI0a	MPI1b	MPI0b	MPI1a	MPI0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

ISR (Interrupt Status Register)

MPI Port Change	Delta BREAKb	RxRDY/ FFULLb	TxRDYb	Counter Ready	Delta BREAKa	RxRDY/ FFULLa	TxRDYa
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

IMR (Interrupt Mask Register)

MPI Port Change INT	Delta BREAKb INT	RxRDY/ FFULLb INT	TxRDYb INT	Counter Ready INT	Delta BREAKa INT	RxRDY/ FFULLa INT	TxRDYa INT
0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

CTUR (Counter/Timer Upper Register)

C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTUR (Counter/Timer Lower Register)

C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

IPR (Input Port Register)

MPP2b	MPP1b	MPP2a	MPP1a	MPI1b	MPI0b	MPI1a	MPI0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

MR2[4] – Clear-to-Send Control

The sate of this bit determines if the CTSN input (MPI) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (Low), the character is transmitted. If it is negated (High), the TxD output remains in the marking state and the transmission is delayed until CTSN goes Low. Changes in CTSN, while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a mark condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled). If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one

stop bit and MR2[3] = 1 selects two stop bits to be transmittted.

CSR – Clock Select Register

CSR[7:4] – Receiver Clock Select
When using a 3.6864MHz crystal or external clock input, this field selects the baud rate clock for the receiver as shown in Table 3.

Table 3. Baud Rate

CSR[7:4]	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75
0 0 0 1	110	110
0 0 1 0	134.5	38.4k
0 0 1 1	200	150
0 1 0 0	300	300
0 1 0 1	600	600
0 1 1 0	1,200	1,200
0 1 1 1	1,050	2,000
1 0 0 0	2,400	2,400
1 0 0 1	4,800	4,800
1 0 1 0	7,200	1,800
1 0 1 1	9,600	9,600
1 1 0 0	38.4k	19.2k
1 1 0 1	Timer	Timer
1 1 1 0	MP2 – 16X	MP2 – 16X
1 1 1 1	MP2 – 1X	MP2 – 1X

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111. When MPP2 is selected as the input, MPP2a is for channel a and MPP2b is for channel b.

CSR[3:] – Transmitter Clock Select
This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3, except as follows:

CSR[3:0]	ACR[7] = 0	ACR[7] = 1
1 1 1 0	MPP1 – 16X	MPP1 – 16X
1 1 1 1	MPP1 – 1X	MPP1 – 1X

When MPP1 is selected as the input, MPP1a is for channel a and MPP1b is for channel b.

CR – Command Register

CR is used to write commands to the Octal UART.

CR[7:4] – Miscellaneous Commands
The encoded value of this field can be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the MR pointer to point to MR1.

0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO pointer is reset to the first location.

0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.

0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2 or 6]) to be cleared to zero.

0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the THR, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break

0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The register in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Reserved.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued.

1101 Reserved.

111x Reserved for testing.

CR[3] – Disable Transmitter
This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CR[2] – Enable Transmitter
Enables operation of the transmitter. The TxRDY status bit will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wake–up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half bit time (two successive edges of the internal or external 1x clock).

When this bit is set, the change in break bit in the ISR (ISR[6 or 2]) is set. ISR[6 or 2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In special 'wake-up mode', the parity error bit stores the received A/D bit.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SR[3] – Transmitter Empty (TxEMT)
This bit will be set when the transmitter underruns, i.e., both the transmit holding register and the transmit shift register are empty. It is set after transmission of the last stop bit of a character, If no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU, or when the transmitter is disabled.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded in the THR while the transmitter is disabled will not be transmitted.

SR[1] – FIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL is not reset after reading the FIFO once.

SR[0] – Receiver Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, and no more characters are in the FIFO.

OPCR – Output Port Configuration Register

OPCR[7] – MPP Function Select
When this bit is a zero, the MPP pins function as inputs, to be used as general purpose inputs or as receiver or transmitter external clock inputs. When this bit is set, the MPP pins function as outputs. MPP1 will be a TxRDY indicator, and MPP2 will be an RxRDY/FFULL indicator.

OPCR[6:4] – MPOb Output Select
This field programs the MPOb output pin to provide one of the following:

000 Request-to-send active-Low output (RTSN). This output is asserted and negated via the command register. Mode RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted out or when the receiver FIFO and receiver shift register are full using MR2[5] and MR1[7], respectively.

001 The counter/timer output. In the timer mode, this output is a square wave with a period of twice the value (in clock periods) of the contents of the CTUR and CTLR. In the counter mode, the output remains high until the terminal count is reached, at which time it goes low. The output returns to the High state when the counter is stopped by a stop counter command.

010 The 1X clock for the transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a non-synchronized 1X clock is output.

011 The 16X clock for the transmitter. This is the clock selected by CSR[3:0], and is a 1X clock if CSR[3:0] = 1111.

100 The 1X clock for the receiver, which is the clock that samples the received data. If data is not being received, a non-synchronized 1X clock is output.

101 The 16X clock for the receiver. This is the clock selected by CSR[7:4], and is a 1X clock if CSR[7:4] = 1111.

110 The transmitter register empty signal, which is the same as SR[3].

111 The receiver ready or FIFO full signal.

OPCR[3] – Power Down Mode Select
This bit, when set, selects the power-down mode. In this mode, the 2698B oscillator is stopped and all functions requiring this clock are suspended. The contents of all registers are saved. It is recommended that the transmitter and receiver be disabled prior to placing the 2698B in this mode. This bit is reset with RESET asserted. Note that this bit must be set to a logic 1 after power up. Only OPCR[3] in block A controls the power-down mode.

OPCR[2:0] – MPOa Output Select
This field programs the MPOa output pin to provide one of the same functions as described in OPCR[6:4].

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, 19.2k, and 38.4k baud.

The selected set of rates is available for use by the receiver and transmitter.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source (see Table 4).

The MPI pin available as the clock source is MPI a,c,e, and g only.

Table 4. ACR[6:4] Operating Mode

[6:4]	Mode	Clock Source
0 0 0	Counter	MPI pin
0 0 1	Counter	MPI pin divided by 16
0 1 0	Counter	TxC–1XA clock of the transmitter
0 1 1	Counter	Crystal or external clock (X1/CLK) divided by 16
1 0 0	Timer	MPI pin
1 0 1	Timer	MPI pin divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register, ISR[7], to be set. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State
These bits are set when a change of state, as defined in the Input Port section of this data

sheet, occurs at the respective pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the inputs pins during the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output is asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR.

ISR[7] – MPI Change-of-State
This bit is set when a change-of-state occurs at the MPI1b, MPI0b, MPI1a, MPI0a input pins. It is reset when the CPU reads the IPCR.

ISR[6] – Channel b Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[5] – Receiver Ready or FIFO Full Channel b
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read.

If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receiver shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[4] – Transmitter Ready Channel b
This bit is a duplicate of TxRDY (SR[2]).

ISR[3] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. It is initialized to '0' when the chip is reset.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[2] – Channel a Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[1] – Receiver Ready or FIFO Full Channel a
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be ready by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receiver shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[0] – Transmitter Ready Channel a
This bit is a duplicate of TxRDY (SR[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the INTRN output is asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at adddress A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a subsequent sttart counter command causes the C/T to terminate the current timing cycle and to begin a new cycle using the values in the CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command read with A3–A0 = H'F'). The command, however, does not stop the C/T. The generated square wave is output on MPO if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching the terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains High until the terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter is read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{DD} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation	1	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)		2.0			V
V_{IH}	Input high voltage (X1/CLK)		$0.8V_{CC}$			V
V_{OL}	Output Low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output High voltage (except OD outputs)	I_{OH} = –400µA	$0.8V_{CC}$			V
		I_{OH} = –100µA	$0.9V_{CC}$			V
I_{IL}	Input current Low, MPI and MPP pins	V_{IN} = 0	–50			µA
I_{IH}	Input current High, MPI and MPP pins	V_{IN} = V_{CC}			20	µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	–10		10	µA
I_{ILX1}	X1/CLK input Low current	V_{IN} = GND, X2 = open	–100			µA
I_{IHX1}	X1/CLK input High current	V_{IN} = V_{CC}, X2 = open			100	µA
I_{OZH}	Output off current High, 3-State data bus	V_{IN} = V_{CC}			10	
I_{OZL}	Output off current Low, 3-State data bus	V_{IN} = 0	–10			µA
I_{ODL}	Open-drain output Low current in off state: IRQN	V_{IN} = V_{CC}	–10			
I_{ODH}	Open-drain output Low current in off state: IRQN	V_{IN} = 0			10	µA
I_{CC}	Power supply current Operating mode				30	mA
	Power down mode				2.0	mA

NOTES:
1. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of V_{IL} and V_{IH}, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for interrupt and MPP outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}. Test conditions for rest of outputs: C_L = 150pF.
5. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{RWD} guarantee that any status register changes are valid.
7. Consecutive write operations to the command register require at least three rising edges of the X1 clock between writes.
8. This value is not tested, but is guaranteed by design.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4]

SYMBOL	FIGURE	PARAMETER	LIMITS Min	Typ	Max	UNIT
Reset timing						
t_{RES}	3	Reset pulse width	200			ns
Bus timing[5]						
t_{RES}	4	A0–A5 setup time to RDN, WRN Low	10			ns
t_{RES}	4	A0–A5 hold time from RDN, WRN High	100			ns
t_{CS}[6]	4	CEN setup time to RDN, WRN Low	0			ns
t_{CH}[6]	4	CEN hold time from RDN, WRN High	0			ns
t_{RW}	4	WRN, RDN pulse width Low	225			ns
t_{DD}	4	Data valid after RDN Low			200	ns
t_{DF}	4	Data bus floating after RDN High			80	ns
t_{DS}	4	Data setup time before WRN High	100			ns
t_{DH}	4	Data hold time after WRN High	10			ns
t_{RWD}[7]	4	Time between reads and/or writes	100			ns
MPI and MPO timing[5]						
t_{PS}	5	MPI or MPP input setup time before RDN Low	0			ns
t_{PH}	5	MPI or MPP input hold time after RDN High	0			ns
t_{PD}	5	MPO output valid from WRN High RDN Low			 250 250	 ns ns
Interrupt timing						
t_{IR}	6	INTRN negated or MPP output High from: Read RHR (RxRDY/FFULL interrupt) Write THR (TxRDY interrupt) Reset command (break change interrupt) Reset command (MPI change interrupt) Stop C/T command (counter interrupt) Write IMR (clear of interrupt mask bit)			 270 270 270 270 270 270	 ns ns ns ns ns ns
Clock timing						
t_{CLK}	7	X1/CLK high or low time	120			ns
t_{CLK}	7	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	7	Counter/timer clock high or low time	120			ns
f_{CTC}	7	Counter/timer clock frequency	0[8]		4.0	MHz
t_{RX}	7	RxC high or low time	200			ns
f_{RX}	7	RxC frequency (16X) RxC frequency (1X)	0[8] 0[8]		2.0 1.0	MHz MHz
t_{TX}	7	TxC high or low time	200			ns
f_{TX}	7	TxC frequency (16X) TxC frequency (1X)	0[8] 0[8]		2.0 1.0	MHz MHz
Transmitter timing						
t_{TXD}	8	TxD output delay from TxC low			350	ns
t_{TCS}	8	TxC output delay from TxD output data	0		150	ns
Receiver timing						
t_{RXS}	9	RxD data setup time to RxC high	50			ns
t_{RXH}	9	RxD data hold time from RxC high	100			ns

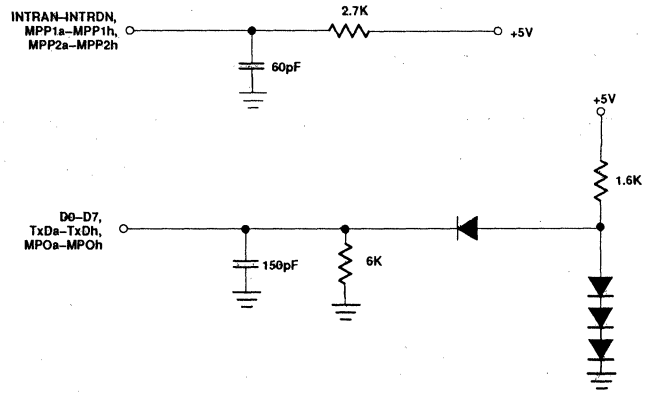


Figure 2. Test Conditions on Outputs

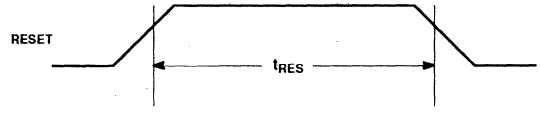


Figure 3. Reset Timing

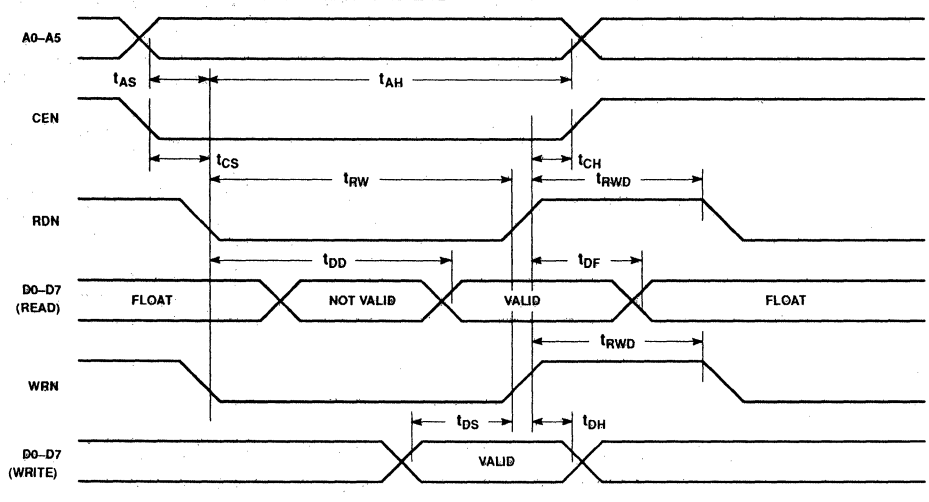


Figure 4. Bus Timing

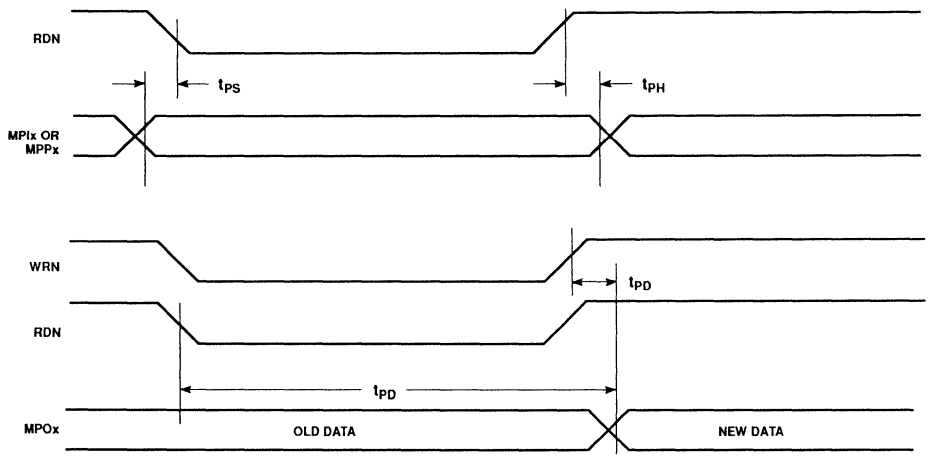
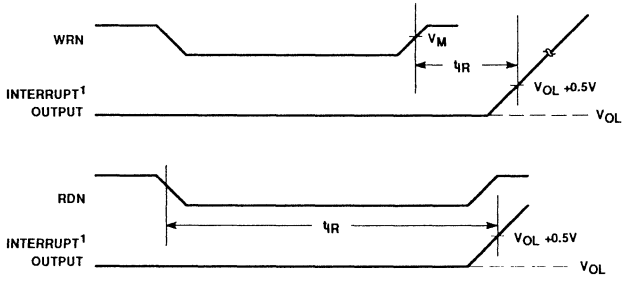
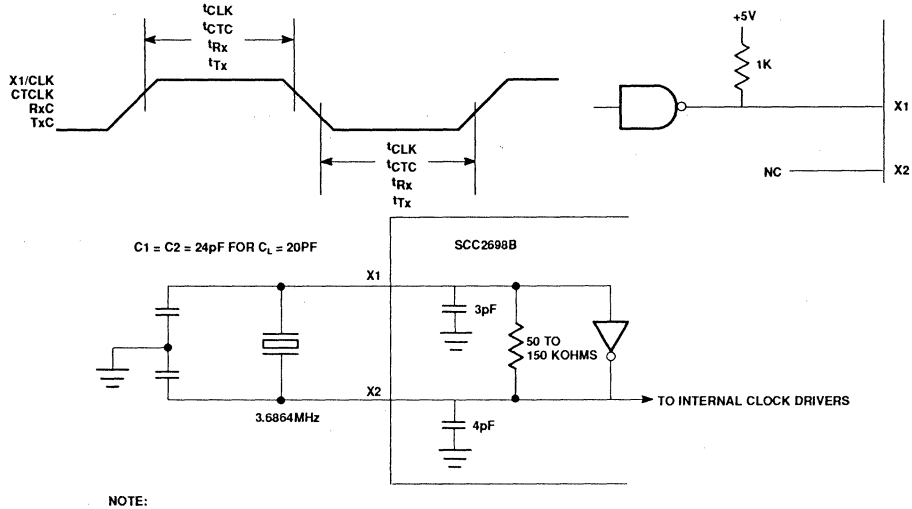


Figure 5. Port Timing



NOTES:
1. INCLUDES MPP WHEN USED AS TxRDY or RxDY/FFULL OUTPUTS AS WELL AS INTRN.
2. THE TEST FOR OPEN DRAIN OUTPUTS IS INTENDED TO GUARANTEE SWITCHING OF THE OUTPUT TRANSISTOR. MEASUREMENT OF THIS RESPONSE IS REFERENCED FROM THE MIDPOINT OF THE SWITCHING SIGNAL, V_M, TO A POINT 0.5V ABOVE V_{OL}. THIS POINT REPRESENTS NOISE MARGIN THAT ASSURES TRUE SWITCHING HAS OCCURRED. BEYOND THIS LEVEL, THE EFFECTS OF EXTERNAL CIRCUITRY AND TEST ENVIRONMENT ARE PRONOUNCED AND CAN GREATLY AFFECT THE RESULTANT MEASUREMENT.

Figure 6. Interrupt Timing



NOTE:
C1 AND C2 SHOULD BE BASED ON MANUFACTURER'S SPECIFICATION.

TYPICAL CRYSTAL SPECIFICATION

FREQUENCY:	2 – 4MHZ
LOAD CAPACITANCE (C_L):	12 – 32pF
TYPE OF OPERATION:	PARALLEL RESONANT, FUNDAMENTAL MODE

Figure 7. Clock Timing

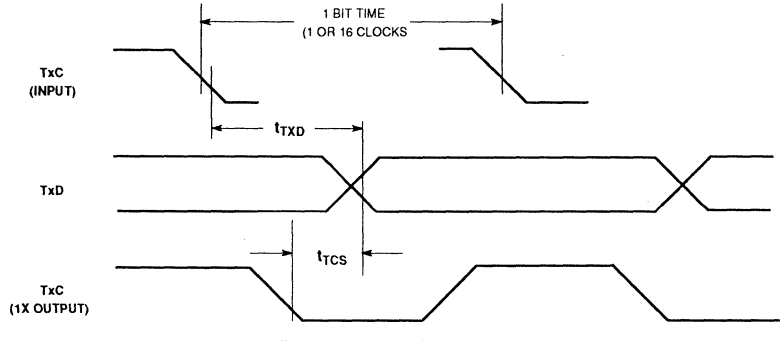


Figure 8. Transmit Timing

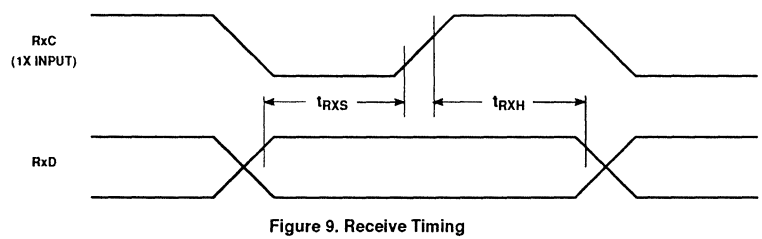


Figure 9. Receive Timing

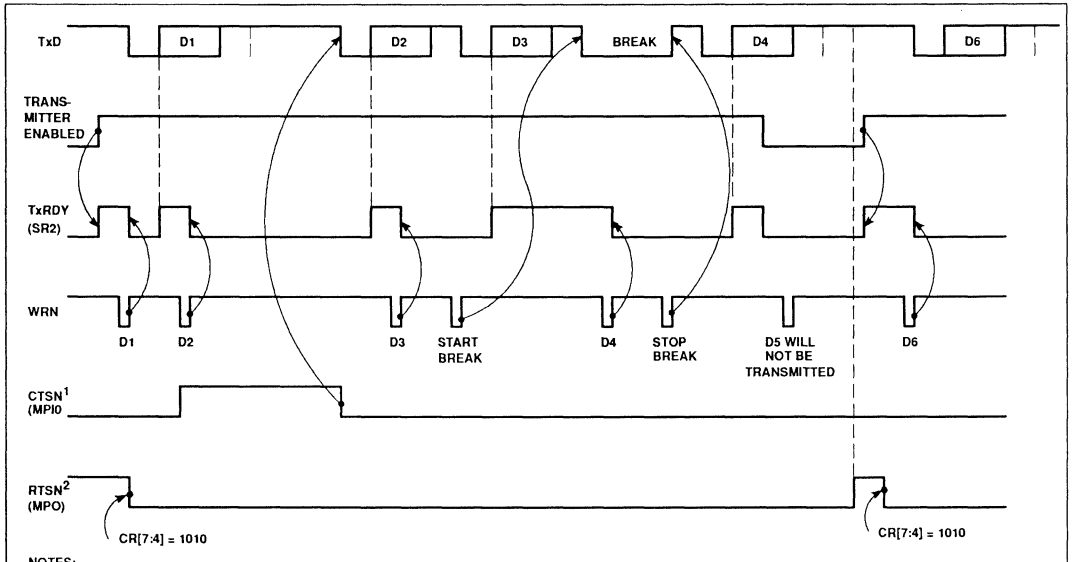


Figure 10. Transmitter Timing

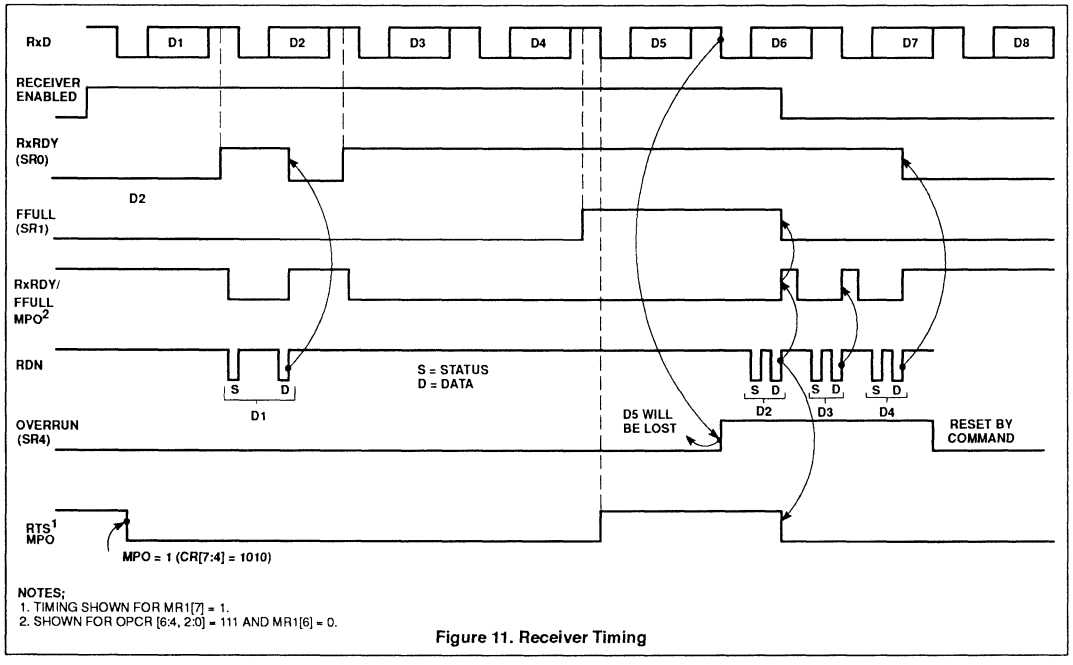


Figure 11. Receiver Timing

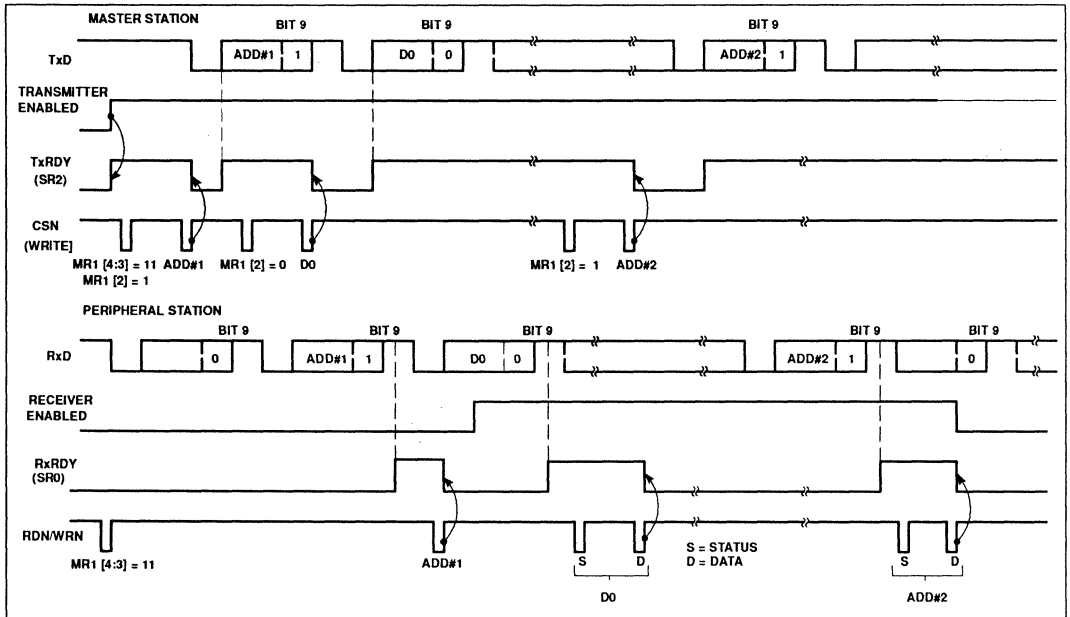


Figure 12. Wake-Up Mode

Philips Components–Signetics

Document No.	853–0307
ECN No.	94624
Date of Issue	October 30, 1990
Status	Product Specification
Data Communication Products	

SCN26562

Dual universal serial communications controller (DUSCC)

DESCRIPTION

The Signetics SCN26562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN26562 interfaces to synchronous bus MPUs and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

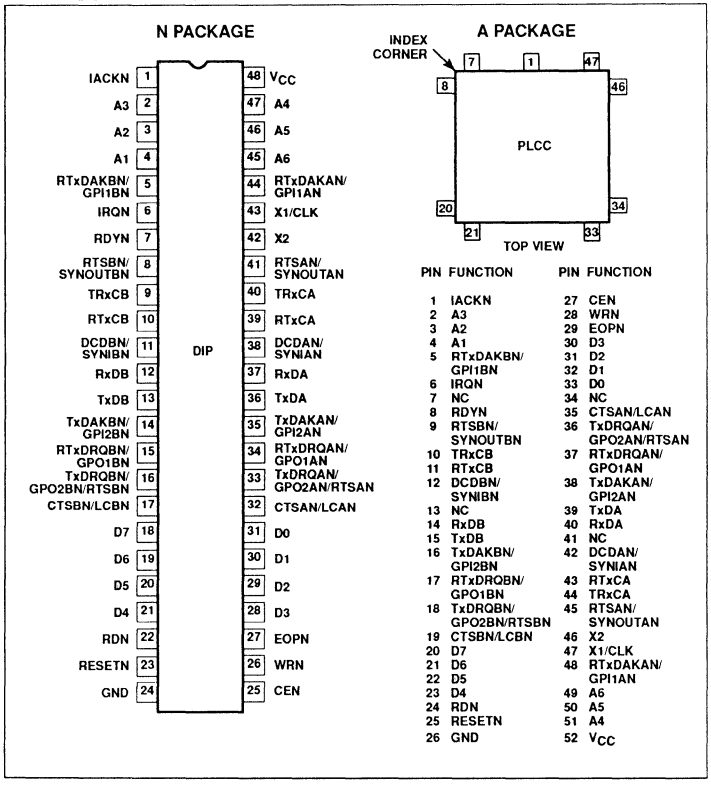
The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multi-function counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

This document contains the electrical specifications for the SCN26562.

PIN DESCRIPTIONS



PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CEN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RDYN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB	38	TxDAKAN/ GPI2AN
12	DCDBN/ SYNIBN	39	TxDA
13	NC	40	RxDA
14	RxDB	41	NC
15	TxDB	42	DCDAN/ SYNIAN
16	TxDAKBN/ GPI2BN	43	RTxCA
17	RTxDRQBN/ GPO1BN	44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5	49	A6
23	D4	50	A5
24	RDN	51	A4
25	RESETN	52	VCC
26	GND		

Dual universal serial communications controller (DUSCC) SCN26562

FEATURES

General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4Mbit/sec data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA EOPN input
- Interrupt capabilities
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbit/sec data rate
  Receives up to 2Mbit/sec data rate

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

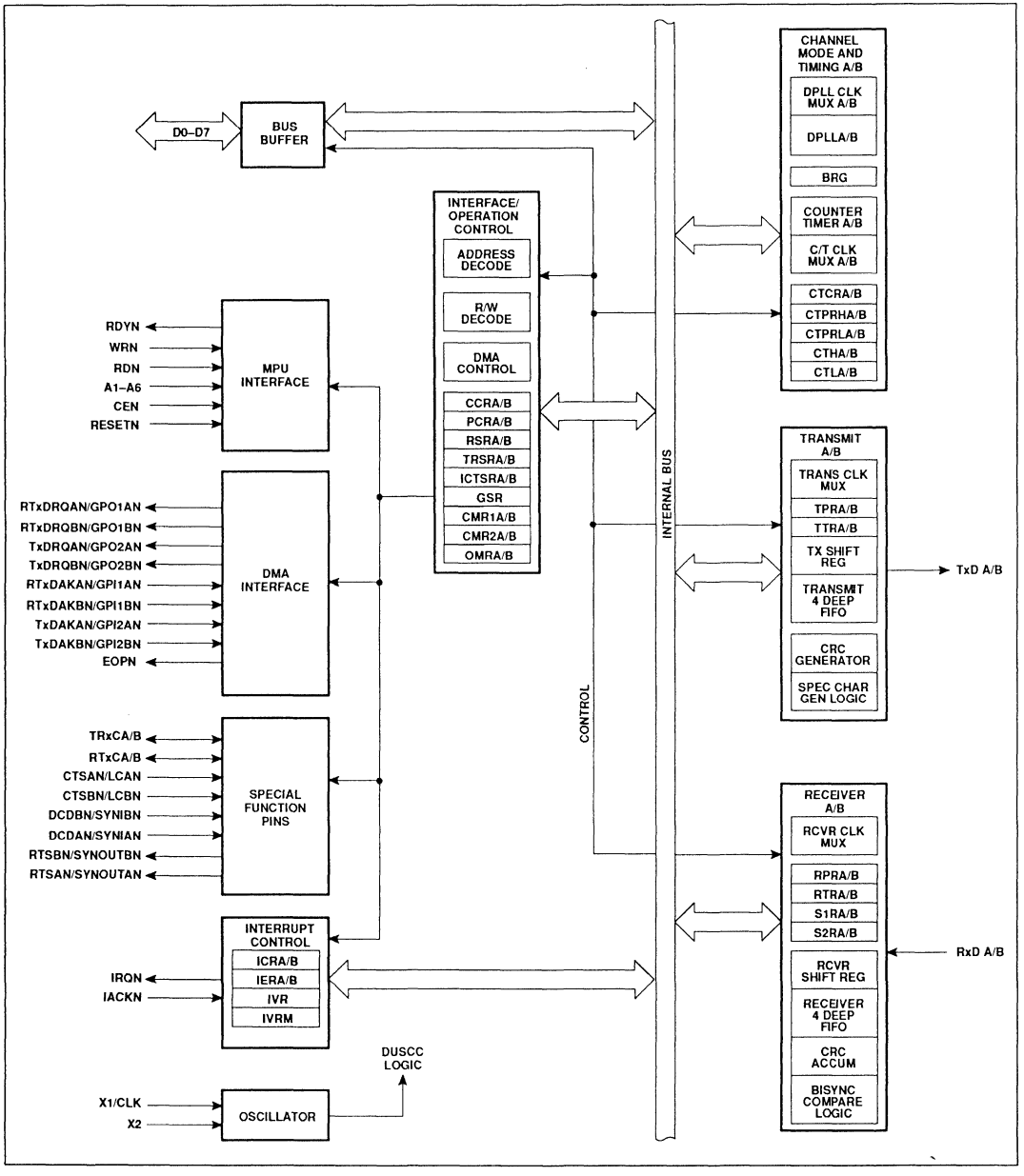
- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and detection
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs linefill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0°C to +70°C	
	Serial Data Rate = 2.5Mbps Maximum	Serial Data Rate = 4Mbps Maximum
48-Pin Plastic DIP	SCN26562C2N48	SCN26562C4N48
52-Pin PLCC	SCN26562C2A52	SCN26562C4A52

Dual universal serial communications controller (DUSCC) SCN26562

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4–2, 47–45	4–2, 51–49	I	Address lines.
D0–D7	31–28, 21–18	33–30, 23–20	I/O	Bidirectional data bus.
RDN	22	24	I	Read strobe.
WRN	26	28	I	Write strobe.
CEN	25	27	I	Chip select.
RDYN	7	8	O	Ready.
IRQN	6	6	O	Interrupt request.
IACKN	1	1	I	Interrupt acknowledge.
X1/CLK	43	47	I	Crystal 1 or external clock.
X2	42	46	I	Crystal 2.
RESETN	23	25	I	Master reset.
RxDA, RxDB	37, 12	40, 14	I	Channel A (B) receiver serial data.
TxDA, TxDB	36, 13	39, 15	O	Channel A (B) transmitter serial data.
RTxCA, RTxCB	39, 10	43, 11	I/O	Channel A (B) receiver/transmitter clock.
TRxCA, TRxCB	40, 9	44, 10	I/O	Channel A (B) transmitter/receiver clock.
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	Channel A (B) clear-to-send input or loop control output.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	Channel A (B) data carrier detected or external sync.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	Channel A (B) receiver/transmitter DMA service request or general purpose output.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	Channel A (B) transmitter DMA service request, general purpose output or request-to-send.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	Channel A (B) receiver/transmitter DMA acknowledge or general purpose input 1.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	Channel A (B) transmitter DMA acknowledge or general purpose input 2.
EOPN	27	29	I/O	DMA transfer complete.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	Channel A (B) request-to-send or Sync detect.
V_{CC}	48	52	I	Power input.
GND	24	26	I	Signal and power ground.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 36°C/W junction to ambient for ceramic DIP, 40°C/W for plastic DIP, and 42°C/W for PLCC.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 2] T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{IL}	Input low voltage:					
	All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage:					
	All except X1/CLK		2.0			V
	X1/CLK		2.4		V_{CC}	V
V_{OL}	Output low voltage:					
	All except IRQN	I_{OL} = 5.3mA			0.5	V
	IRQN	I_{OL} = 8.8mA			0.5	V
V_{OH}	Output high voltage:					
	(Except open drain outputs)	I_{OH} = –400µA	2.4			V
I_{ILX1}	X1/CLK input low current[4]	V_{IN} = 0, X2 = GND	–5.5		0.0	mA
I_{IHX1}	X1/CLK input high current[4]	V_{IN} = V_{CC}, X2 = GND			1.0	mA
I_{ILX2}	X2 input low current[4]	V_{IN} = 0, X1 = open	–100			µA
I_{IHX2}	X2 input high current[4]	V_{IN} = V_{CC}, X1 = open			100	µA
I_{IL}	Input low current RESETN, TxDAKN, RxDAKN	V_{IN} = 0	–40			µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	–5		5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	–5			µA
I_{ODL}	Open drain output low current in off state: EOPN	V_{IN} = 0	–120		–25	µA
	IRQN, RDYN		–5			µA
I_{ODH}	Open drain output high current in off state: EOPN, IRQN, RDYN	V_{IN} = V_{CC}			5	µA
I_{CC}	Power supply current	V_O = 0 to V_{CC}			275	mA
C_{IN}	Input capacitance[3]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[3]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[3]	V_{CC} = GND = 0			20	pF

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 2.8V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. These values were not explicitly tested; they are guaranteed by design and characterization data.
4. X1/CLK and X2 are not tested with a crystal installed.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4] T_A = 0°C to +70°C, V_{CC} = 5V ±5%

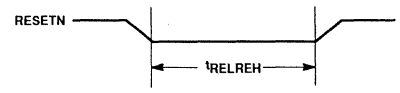
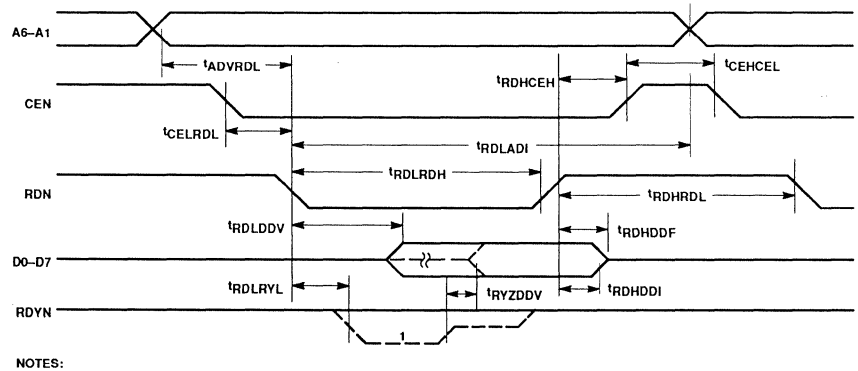


Figure 1. Reset Timing

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 2.8V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. See Figure 17 for test conditions for outputs.
4. Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2V above the actual output signal level. This point represents noise margin that assures true switching has occurred.

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RELREH}	RESETN low to RESETN high	1.2		1.2		µs

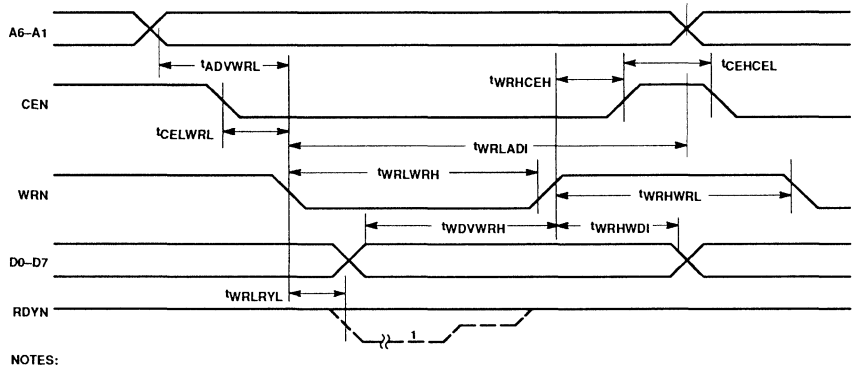


NOTES:
1. Wait on Rx. Receiver FIFO empty.
2. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

Figure 2. Read Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{ADVRDL}	Address valid to RDN low	10		10		ns
t_{CELRDL}	CEN low to RDN low	0		0		ns
t_{RDLADI}	RDN low to address invalid	150		150		ns
t_{RDLRYL}	RDN low to RDYN low		275		275	ns
t_{RDLDDV}	RDN low to read data valid		280		300	ns
t_{RDLRDH}	RDN low to RDN high	300		310		ns
t_{RYZDDV}	RDYN high impedance to read data valid		100		100	ns
t_{RDHCEH}	RDN high to CEN high	0		0		ns
t_{CEHCEL}	CEN high to CEN low	160		170		ns
t_{RDHDDI}	RDN high to read data invalid	10		10		ns
t_{RDHRDL}	RDN high to RDN low	160		170		ns
t_{RDHDDF}	RDN high to data bus floating		75		75	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

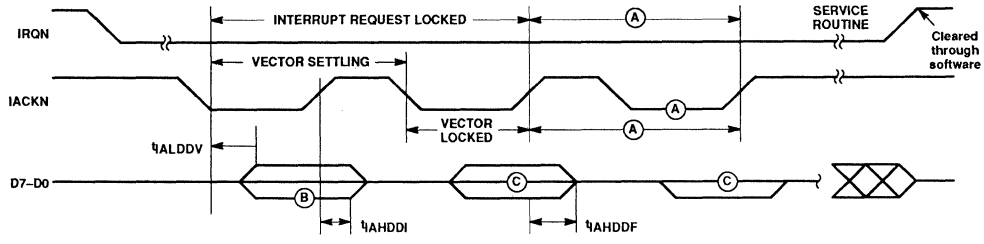


NOTES:
1. Wait on Tx. Transmitter FIFO full.
2. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

Figure 3. Write Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{ADVWRL}	Address valid to WRN low	10		10		ns
t_{CELWRL}	CEN low to WRN low	0		0		ns
t_{WRLRYL}	WRN low to READY low		275		275	ns
t_{WRHCEH}	WRN high to CEN high	0		0		ns
t_{WRLWRH}	WRN low to WRN high	300		310		ns
t_{WDVWRH}	Write data valid to WRN high	100		100		ns
t_{CEHCEL}	CEN high to CEN low	160		170		ns
t_{WRLADI}	WRN low to address invalid	150		150		ns
t_{WRHWRL}	WRN high to WRN low	160		170		ns
t_{WRHWDI}	WRN high to write data invalid	10		10		ns

AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) ICR[5:4] = 01 or 10 (mode 1 or mode 2)
(B) Call instruction (mode 2)
(C) ICR[5:4] = 11 (mode 3)

Figure 4. Interrupt Acknowledge Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{IALDDV}	IACKN low to data bus valid		280		280	ns
t_{IAHDDF}	IACKN high to data bus floating		150		150	ns
t_{IAHDDI}	IACKN high to data bus invalid	10		10		ns

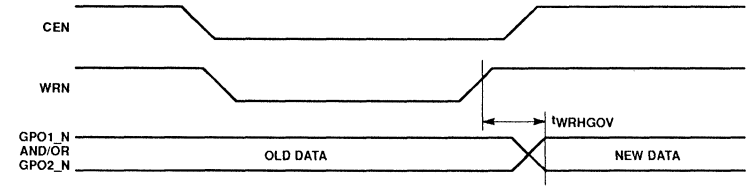


Figure 5. Output Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{WRHGOV}	WRN high to GPO output data valid		300		300	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

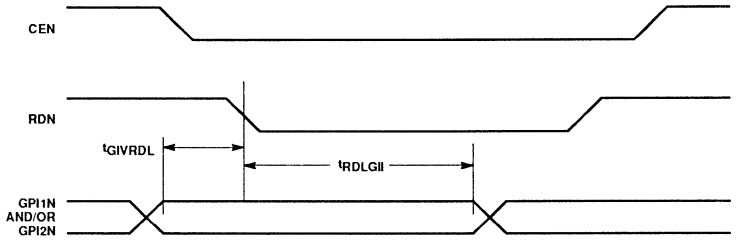


Figure 6. Input Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{GIVRDL}	GPI input valid to RDN low	20		20		ns
t_{RDLGII}	RDN low to GPI input invalid	100		100		ns

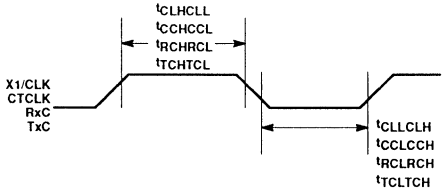


Figure 7. Clock Timing

SYMBOL	PARAMETER	LIMITS						UNIT
		SCN26562C4			SCN26562C2			
		Min	Typ	Max	Min	Typ	Max	
t_{CLHCLL}	X1/CLK high to low time	25			25			ns
t_{CLLCLH}	X1/CLK low to high time	25			25			ns
t_{CCHCCL}	C/T CLK high to low time	100			100			ns
t_{CCLCCH}	C/T CLK low to high time	100			100			ns
t_{RCHRCL}	RxC high to low time	110			150			ns
t_{RCLRCH}	RxC low to high time	110			150			ns
t_{TCHTCL}	TxC high to low time	110			150			ns
t_{TCLTCH}	TxC low to high time	110			150			ns
f_{CL}	X1/CLK frequency	2.0	14.7456	16.0	2.0	14.7456	16.0	MHz
f_{CC}	C/T CLK frequency	0		4.0	0		4.0	MHz
f_{RC}	RxC frequency (16X or 1X)	0		4.0	0		2.5	MHz
f_{TC}	TxC frequency (16X or 1X)	0		4.0	0		2.5	MHz

AC ELECTRICAL CHARACTERISTICS (Continued)

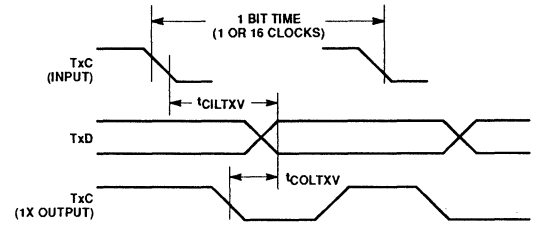


Figure 8. Transmit Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{CILTXV}	TxC input low (1X) to TxD output		240		240	ns
	TxC input low (16X) to TxD output		435		435	ns
t_{COLTXV}	TxC output low to TxD output		50		50	ns

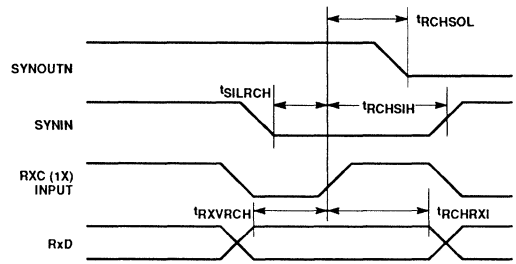
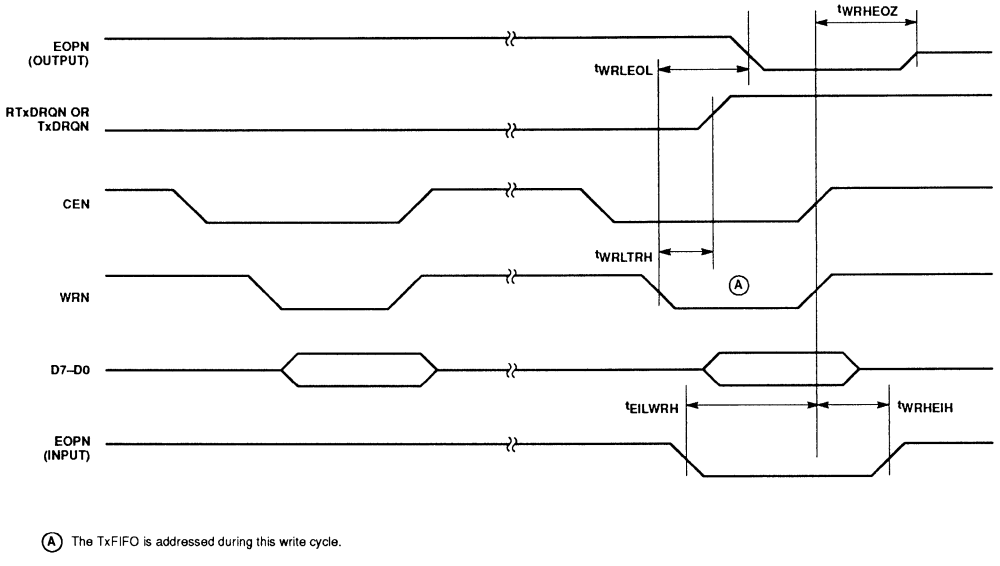


Figure 9. Receive Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RXVRCH}	RxD data valid to RxC high:					
	For NRZ data	50		50		ns
t_{RCHRXI}	For NRZI, Manchester, FM0, FM1 data	120		130		ns
	RxC high to RxD data invalid:					
	For NRZ data	50		50		ns
	For NRZI, Manchester, FM0, FM1 data	10		10		ns
t_{SILRCH}	SYNIN low to RxC high	100		100		ns
t_{RCHSIH}	RxC high to SYNIN high	50		50		ns
t_{RCHSOL}	RxC high to SYNOUT low		300		300	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

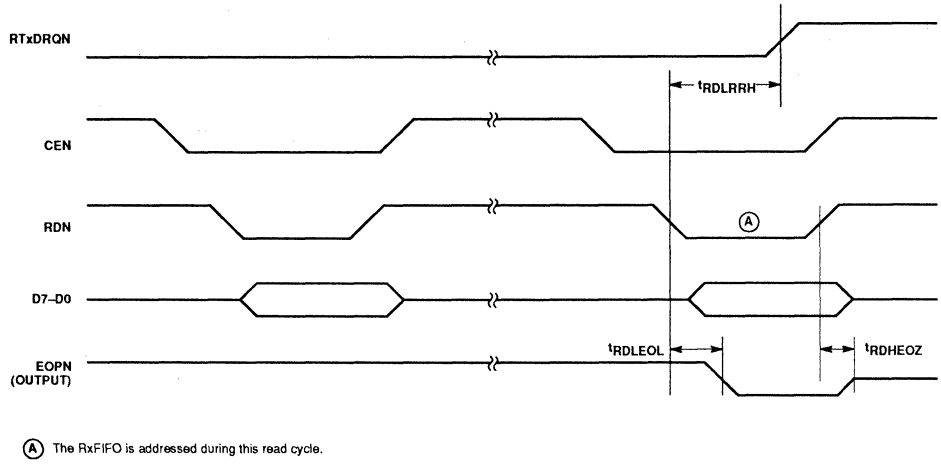


(A) The TxFIFO is addressed during this write cycle.

Figure 10. Transmit Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{WRLTRH}	WRN low to Tx DMA REQN high		320		320	ns
t_{WRLEOL}	WRN low to EOPN output low		225		225	ns
t_{WRHEOZ}	WRN high to EOPN output high impedance		225		225	ns
t_{EILWRH}	EOPN input low to WRN high	50		50		ns
t_{WRHEIH}	WRN high to EOPN input high	50		50		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

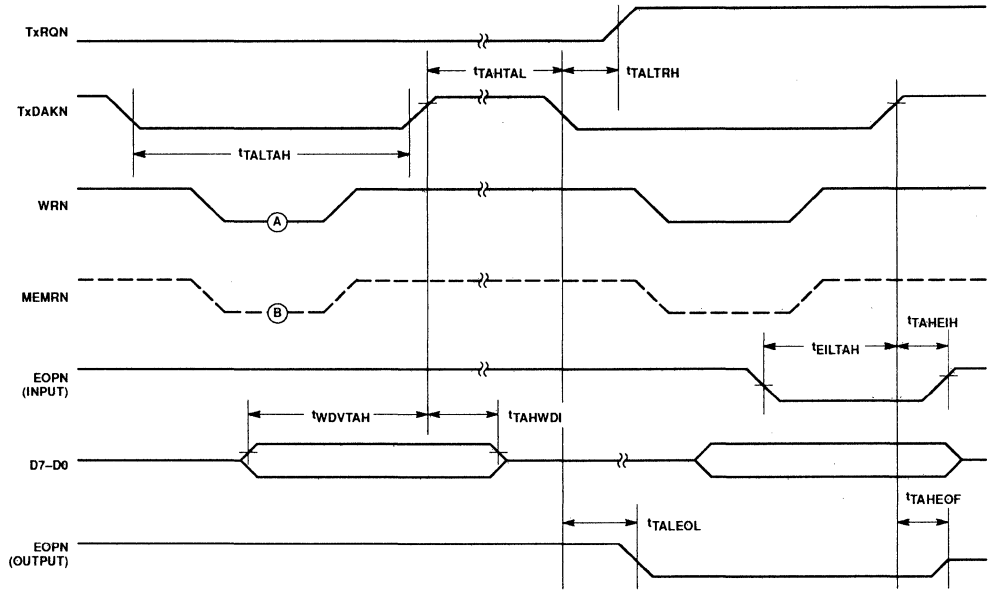


A The RxFIFO is addressed during this read cycle.

Figure 11. Receive Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RDLRRH}	RDN low to Rx DMA REQN high		320		320	ns
t_{RDLEOL}	RDN low to EOPN output low		300		300	ns
t_{RDHEOZ}	RDN high to EOPN output high impedance		225		225	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

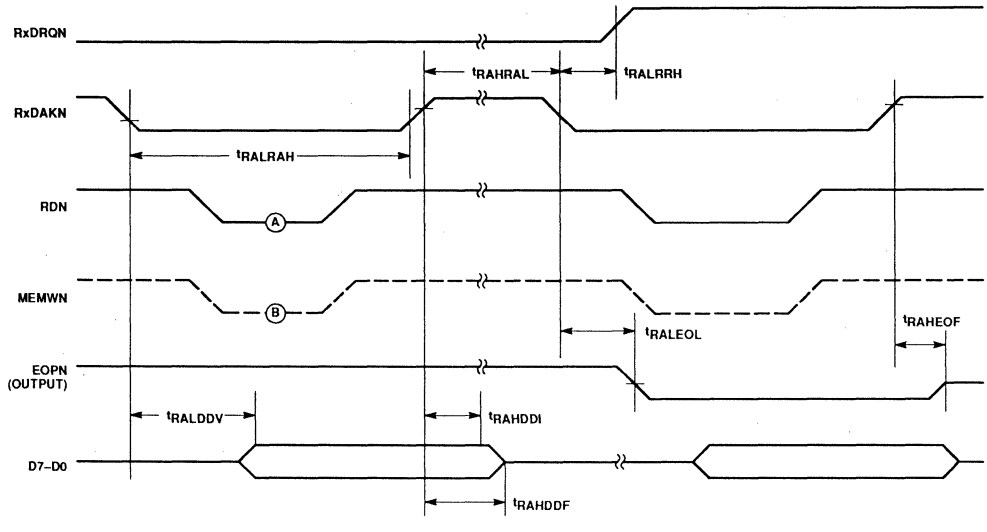


NOTES:
(A) Ignored by the DUSCC since CEN is not asserted, but it can be used externally to qualify TxDAKN.
(B) Memory read signal; not seen by DUSCC.

Figure 12. DMA–Transmit Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{TAHTAL}	Transmit DMA ACKN high to low time	100		100		ns
t_{TALTAH}	Transmit DMA ACKN low to high time	250		250		ns
t_{TALTRH}	Tx DMA ACKN low to Tx DMA REQN high		250		250	ns
t_{WDVTAH}	Write data valid to Tx DMA ACKN high	90		90		ns
t_{TAHWDI}	Tx DMA ACKN high to write data invalid	30		30		ns
t_{TALEOL}	Tx DMA ACKN low to EOPN output low		170		170	ns
t_{TAHEOF}	Tx DMA ACKN high to EOPN output float		200		200	ns
t_{EILTAH}	EOPN input low to Tx DMA ACKN high	50		50		ns
t_{TAHEIH}	Tx DMA ACKN high to EOPN input high	50		50		ns

AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) Ignored by the DUSCC bit; it can be used to qualify RxDAKN.
(B) Memory read signal; not seen by DUSCC.

Figure 13. DMA–Receive Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RAHRAL}	Receive DMA ACKN high to low time	160		160		ns
t_{RALRAH}	Receive DMA ACKN low to high time	250		250		ns
t_{RALRRH}	Rx DMA ACKN low to Rx DMA REQN high		320		320	ns
t_{RALEOL}	Rx DMA ACKN low to EOPN output low		200		200	ns
t_{RAHEOF}	Rx DMA ACKN high to EOPN output float		225		225	ns
t_{RALDDV}	Rx DMA ACKN low to read data valid		225		225	ns
t_{RAHDDI}	Rx DMA ACKN high to read data invalid	10		10		ns
t_{RAHDDF}	Rx DMA ACKN high to data bus float		125		125	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

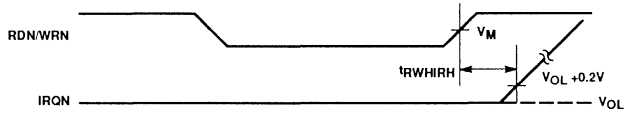


Figure 14. Interrupt Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RWHIRH}	RDN/WRN high to IRQN high for:					
	Read RxFIFO (RxRDY interrupt)		450		450	ns
	Write TxFIFO (TxRDY interrupt)		450		450	ns
	Write RSR (Rx condition interrupt)		400		400	ns
	Write TRSR (Rx/Tx interrupt)		400		400	ns
	Write ICTSR (counter/timer interrupt)		400		400	ns

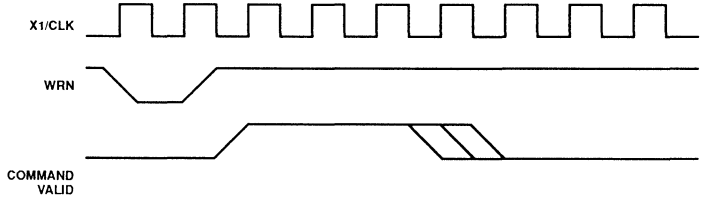


Figure 15. Command Timing

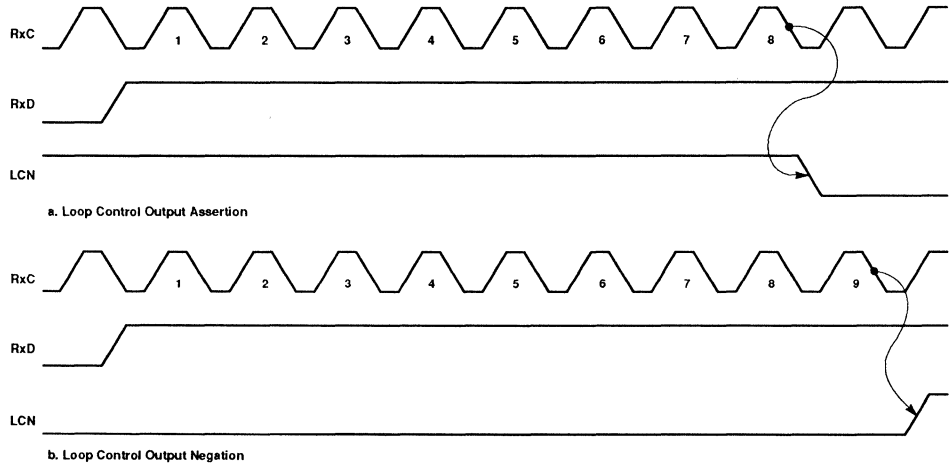
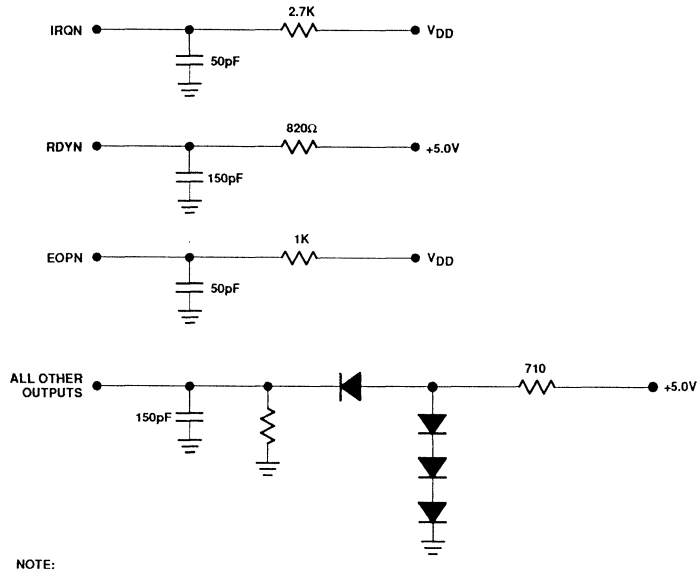


Figure 16. Relationship Between Received Data and the Loop Control Output



NOTE:
All C_L includes 50pF stray capacitance,
i.e., C_L = 150pF = 100pF discrete +50pF stray.

Figure 17. Test Conditions for Outputs

Philips Components–Signetics

Document No.	
ECN No.	
Date of Issue	November 8, 1990
Status	Preliminary Specification
Data Communication Products	

SC26C562/SC68C562

Dual universal serial communications controller (DUSCC)

Preliminary Features and Additions between NMOS and CMOS devices.
Familiarity with the DUSCC users guide is assumed.

DESCRIPTION

The Signetics Dual Universal Serial Communications Controller (DUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The new CMOS device (SC26C562/SC68C562) will be pin hardware and software compatible with the present SCN26562 and SCN68562. All design variances in the NMOS device had been corrected. However after power up the CMOS DUSCC will be configured to operate as the NMOS DUSCC.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4.0Mbits per second are supported.

The transmitter and receiver each contain a sixteen characters FIFOs with appended transmitter command and receiver status bits. This permits reading and writing of up to sixteen characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

Two versions of the DUSCC are available. The SC26C562 is optimized to interface with processors using a synchronous bus interface, such as the 8086, 80186 and 80286. The SC68C562 is optimized to interface with processors using an asynchronous bus interface, such as the 68000 and 68010. Both versions are capable of program-polled, interrupt-driven, block-move or DMA data transfers. The contents of this manual apply to both versions of the DUSCC, unless explicitly noted otherwise.

FEATURES

General Features

- Multi-protocol operation
- Sixteen character receiver and transmitter FIFOs. Nine status bits fifoed with each byte received.
- 0 to 10Mbit/sec. data rate
- Programmable bit rate for each receiver and transmitter
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- or half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- Single- or dual-address DMA transfers
- Two multi-function programmable 16-bit counter/timers
- On-chip oscillator for crystal

Asynchronous Mode

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmit up to 4.0Mbps and receive up to 2.0Mbps data rates

FEATURES (Continued)

Character-Oriented Protocols

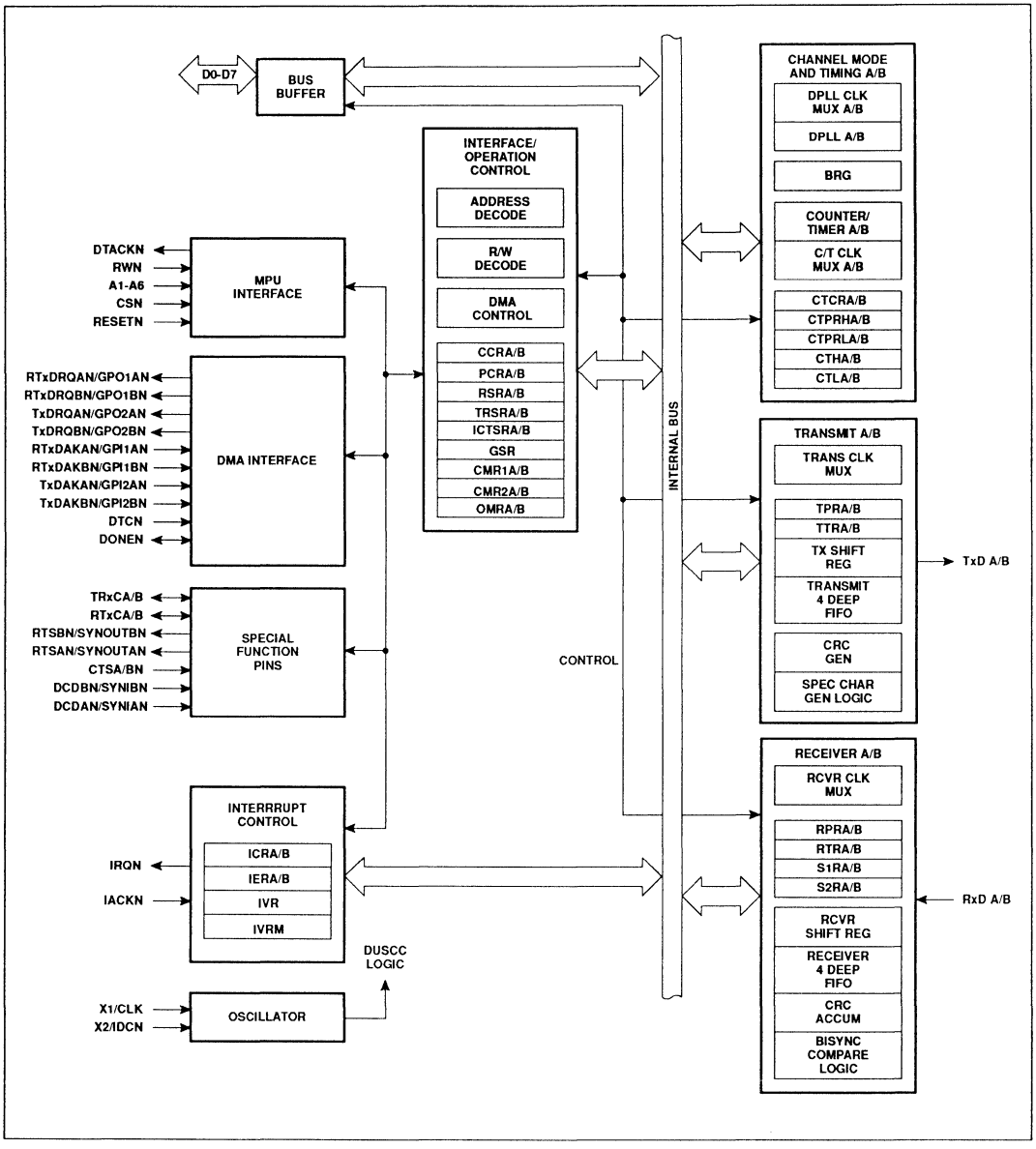
- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- SYN detection and optional stripping
- SYN or MARK linefill or underrun
- Idle in MARK or SYNs
- BISYNC submode

Bit-Oriented Protocol

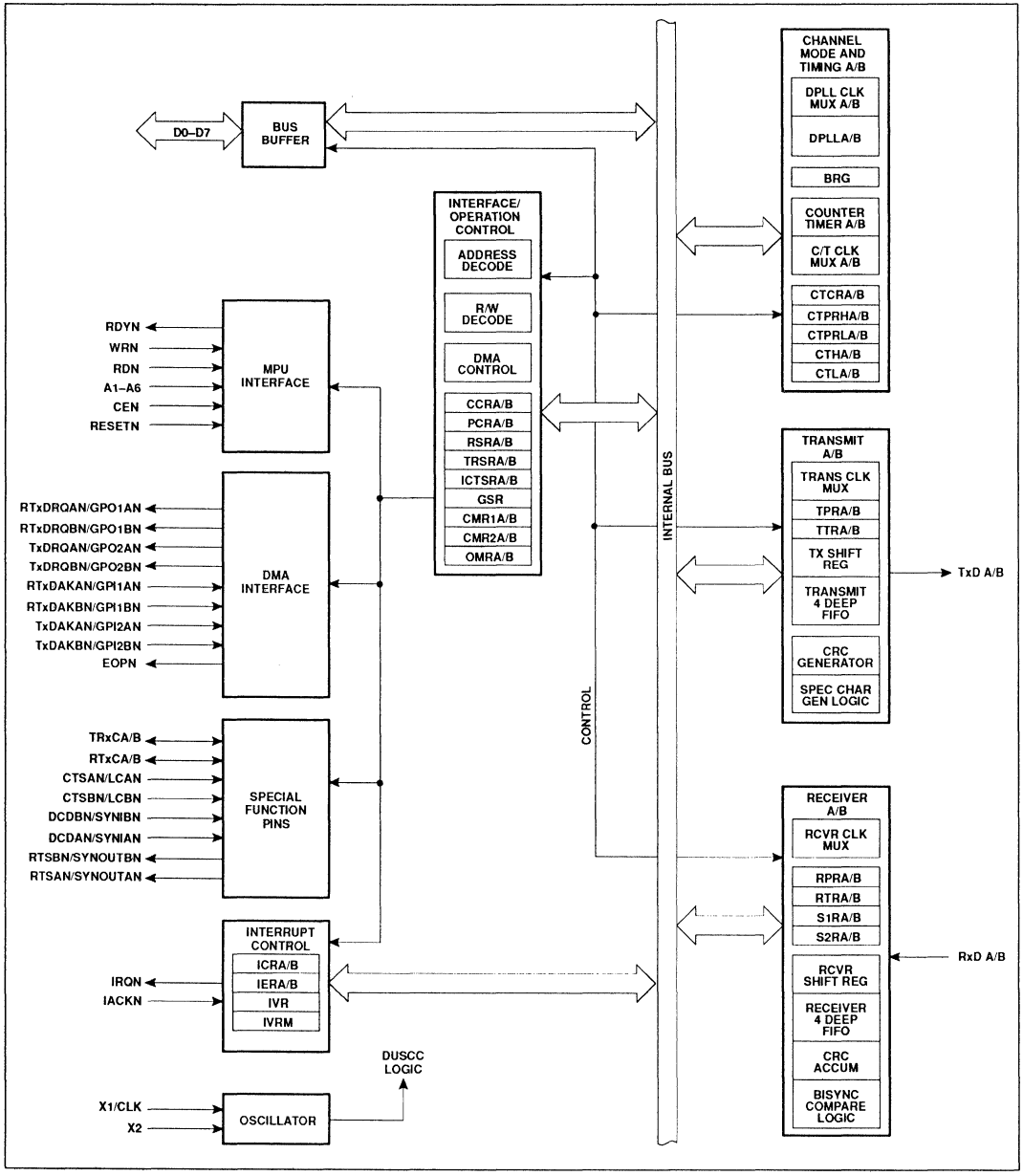
- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- ABORT, ABORT-FLAGs, or FCS-FLAGs linefill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- CRC generation and checking
- SDLC loop mode capability

Dual universal serial communications controller (DUSCC) SC26C562/SC68C562

BLOCK DIAGRAM — SC68C562



BLOCK DIAGRAM — SC26C562



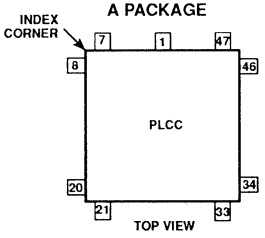
Dual universal serial communications controller (DUSCC) SC26C562/SC68C562

PIN CONFIGURATIONS — SC68C562

N PACKAGE

TOP VIEW

A PACKAGE

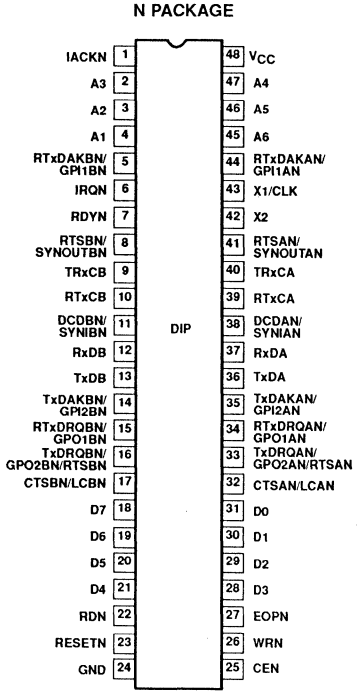


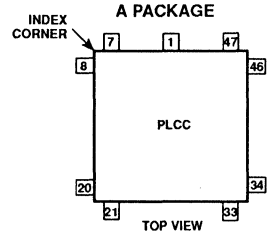
TOP VIEW

Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RESETN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2/IDCN
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	DTACKN	50	A5
25	DTCN	51	A4
26	GND	52	VDD

Dual universal serial communications controller (DUSCC) SC26C562/SC68C562

PIN CONFIGURATIONS — SC26C562





PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CEN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RDYN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	RDN	50	A5
25	RESETN	51	A4
26	GND	52	VCC

PIN DESCRIPTION

In this document, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. N at the end of a pin name signifies the signal associated with the pin is Active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by A/B after the name of the pin and the Active-Low state indicator, N, if applicable. A similar method is used for registers provided for both channels; these are designated by either an underline or by A/B after the name.

MNEMONIC	APPLIES TO		TYPE	NAME AND FUNCTION
	26C562	68C562		
A1–A6	X	X	I	**Address Lines:** Active-high. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	X	X	I/O	**Bidirectional Data Bus:** Active-high, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN (CEN) is low and during interrupt acknowledge cycles and single address DMA acknowledge cycles.
R/WN		X	I	**Read/Write:** A high input indicates a read cycle and a low input indicates a write cycle when a cycle is initiated by assertion of the CSN input.
CSN		X	I	**Chip Select:** Active-low input. When low, data transfers between the CPU and the DUSCC are enabled on D0–D7 as controlled by the R/WN and A1–A6 inputs. When CSN is high, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single address DMA transfers) and D0–D7 are placed in the 3-State condition.
DTACKN		X	O	**Data Transfer Acknowledge:** Active-low, 3-State. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. In a write bus cycle, input data is latched by the assertion (falling edge) of DTACKN or by the negation (rising edge) of CSN, whichever occurs first. The signal is negated when completion of the cycle is indicated by negation of CSN or IACKN input, and returns to the inactive state (3-State) a short period after it is negated. In a single address DMA mode, input data is latched by the assertion (falling edge) of DTCN or by the negation (rising edge) of the DMA acknowledge input, whichever occurs first. DTACK is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-State) a short period after it is negated. When inactive, DTACKN requires an external pull-up resistor.
RDN	X		I	**Read Strobe:** Active-low input. When active and CEN is also active, causes the content of the addressed register to be present on the data bus. RDN is ignored unless CEN is active.
WRN	X		I	**Write Strobe:** Active-low input. When active and CEN is also active, the content of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of WRN. WRN is ignored unless CEN is active.
CEN	X		I	**Chip Enable:** Active-low input. When active, data transfers between the CPU and the DUSCC are enabled on D7–D0 as controlled by RDN or WRN, and A6–A1. When CEN is high, the data lines are placed in the 3-State condition (except if IACKN is asserted or during a ddMA acknowledge cycle).
RDYN	X		O	**Ready:** Active-low, open drain. Used to synchronize data transfers between the master and the DUSCC. It is valid only during read and write cycles where the DUSCC is configured in 'wait on Rx', 'wait on Tx' or 'wait on Tx or Rx' modes, otherwise it is always inactive. RDYN becomes active o n the leading edge of RDN and WRN if the requested operation cannot be performed (viz, no data in RxFIFO in the case of a read or no room in the TxFIFO in the case of a write).
IRQN	X	X	O	**Interrupt Request:** Active-low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus.
IACKN		X	I	**Interrupt Acknowledge:** Active-low. When IACKN is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted.
IACKN	X		I	**Interrupt Acknowledge:** Active-low. When IACKN is asserted, the DUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	X	X	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. When a crystal is used, a capacitor must be connected from this pin to ground.

PIN DESCRIPTION (Continued)

MNEMONIC	APPLIES TO		TYPE	NAME AND FUNCTION
	26C562	68C562		
X2/IDCN		X	I/O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide an interrupt daisy chain active-low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2 is not used as an interrupt daisy chain output. When a crystal is used, a capacitor must be connected from this pin to ground.
X2	X		I	**Crystal 2:** Connection for other side of crystal. When a crystal is used, a capacitor must be connected from this pin to ground. If an external clock is used on X1, this pin must be grounded.
RESETN	X	X	I	**Master Reset:** Active-low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1. Reset is asynchronous, i.e., no clock is required.
RxDA, RxDB	X	X	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	X	X	O	**Channel A (B) Transmitter Serial Data Output:** The least signifiicant bit is transmitted first. This output is in the marking condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	X	X	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	X	X	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1/2).
CTSA/BN, LCA/BN	X	X	I/O	**Channel A (B) Clear-to-Send Input or Loop Control Output:** Active-low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	X	X	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-low input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the DUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-low external sync input, it is used in COP mode to obtain character synchronization for the receiver without receipt of a SYN character. This mode can be used in disc or tape controller applications.
RTxDRQA/BN, GPO1A/BN	X	X	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	X	X	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control (see Detailed Operation).
RTxDAKA/BN, GPI1A/BN	X	X	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-low. For half-duplex single address operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning. For full-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.

PIN DESCRIPTION (Continued)

MNEMONIC	APPLIES TO		TYPE	NAME AND FUNCTION
	26C562	68C562		
TxDAKA/BN, GPI2A/BN	X	X	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DTCN		X	I	**Device Transfer Complete:** Active-low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
DONEN		X	I/O	**Done:** Active-low, open-drain. DONEN can be used and is active in both DMA and non-DMA modes. See Detailed Operation for a description of the function of this pin.
EOPN	X		I/O	**Done (EOP):** Active-low, open-drain. EOPN can be used and is active in both DMA and non-DMA modes. See Detailed Operation for a description of the function of this pin.
RTSA/BN, SYNOUTA/BN	X	X	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{DD}	X	X	I	**+5V Power Input**
GND	X	X	I	**Signal and Power Ground Input**

Table 1. DUSCC Register Address Map (Present NMOS DUSCC and new CMOS DUSCC)

ADDRESS BITS[1]						ACRONYMS	REGISTER NAME	MODE	AFFECTED BY RESET
6	5	4	3	2	1				
c	0	0	0	0	0	CMR1	Channel mode register 1	R/W	Yes – 00
c	0	0	0	0	1	CMR2	Channel mode register 2	R/W	Yes – 00
c	0	0	0	1	0	S1R	SYN 1/secondary address 1 register	R/W	No
c	0	0	0	1	1	S2R	SYN 2/secondary address 2 register	R/W	No
c	0	0	1	0	0	TPR	Transmitter parameter register	R/W	Yes – 00
c	0	0	1	0	1	TTR	Transmitter timing register	R/W	No
c	0	0	1	1	0	RPR	Receiver parameter register	R/W	Yes – 00
c	0	0	1	1	1	RTR	Receiver timing register	R/W	No
c	0	1	0	0	0	CTPRH	Counter/timer preset register high	R/W	No
c	0	1	0	0	1	CTPRL	Counter/timer preset register low	R/W	No
c	0	1	0	1	0	CTCR	Counter/timer control register	R/W	Yes – 00
c	0	1	0	1	1	OMR **	Output and miscellaneous register	R/W	Yes – 00
c	0	1	1	0	0	CTH	Counter/timer high	R	No
c	0	1	1	0	1	CTL	Counter/timer low	R	No
c	0	1	1	1	0	PCR	Pin configuration register	R/W	Yes – 00
c	0	1	1	1	1	CCR **	Channel command register	R/W	No
c	1	0	0	X	X	TxFIFO	Transmitter FIFO	W	No
c	1	0	1	X	X	RxFIFO	Receiver FIFO	R	No
c	1	1	0	0	0	RSR **	Receiver status register	R/W[2]	Yes – 00
c	1	1	0	0	1	TRSR **	Transmitter and receiver status register	R/W[2]	Yes – 00
c	1	1	0	1	0	ICTSR **	Input and counter/timer status register	R/W[2]	Yes
d	1	1	0	1	1	GSR	General status register	R/W[2]	Yes – 00
c	1	1	1	0	0	IER	Interrupt enable register	R/W	Yes – 00
c	1	1	1	0	1		Not used		
0	1	1	1	1	0	IVR	Interrupt vector register – unmodified	R/W	Yes – 0F
1	1	1	1	1	0	IVRM	Interrupt vector register – modified	R	Yes – FF
0	1	1	1	1	1	ICR **	Interrupt control register	R/W	Yes – 00
1	1	1	1	1	1[3]	MRR	Master reset register	R/W	Yes[3]

NOTES:
1. c = 0 for channel A, c = 1 for channel B.
   d = don't care — register may be accessed as either channel.
   x = don't care — FIFOs are addressable at any of four adjacent addresses to allow them to be addressed as byte/word/long word.
2. A write to this register can perform a status resetting operation.
3. SC26C562 only. See Master Reset Register section for description of operation. Not used for SC68C562.
4. n/a = Not applicable
5. ** These registers are EDGE TRIGGERED. Others are read only or level triggered. Level triggered registers should not be changed while channel is active. NOTE: ICTSR for bits 6, 5, 4 only.

REGISTERS

The addressable registers of the DUSCC are shown in Table 1. The following rules apply to all registers:

1. A read from a reserved location in the map results in a read from the 'null register'. The null register returns all ones for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle without a write being performed.
2. Unused bits of a defined register are read as zeros, unless ones have been loaded after master reset.
3. Bits that are unused in the chosen mode but are used in others are readable and writable but their contents are ignored in the chosen mode.
4. All registers are addressable as 8-bit quantities. Addresses are ordered such that certain sets of registers may also be accessed as words or long words.

The operation of the DUSCC is programmmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The contents of certain control registers are initialized on RESET. Care should be exercised if the contents of a register are changed during

operation, since certain changes may cause operational problems, e.g., changing the channel mode at an inappropriate time may cause the reception or transmission of an incorrect character. In general, the contents of registers which control transmitter or receiver operation, or the counter/timer, should be changed only when they are not enabled.

The DUSCC registers can be separated into five groups to describe their usage:

1. Channel mode configuration and pin description registers.
2. Transmitter and receiver parameter and timing registers.
3. Counter/timer control and value registers.
4. Interrupt control and status registers.
5. Command register.

CMOS DUSCC OBJECTIVE SPEC

The CMOS DUSCC is a single-chip communication device that is a fully software compatible with Signetics' DUSCC chip with 16 deep FIFO, individual interrupt enable bits. It is implemented using high speed CMOS process and faster data bus timing.

Key Features

- Fully software and hardware compatible with NMOS DUSCC
- 8 bit data bus with 160ns bus cycle
- 0 to 10Mbit per second
- Rx FIFO
  - 16 x 8 data FIFO
  - RxRDY triggered by programmable filled level of FIFO
  - Watch dog timer
  - Status bits for the filled level of Rx FIFO
  - FIFO all of the error status bits
  - Provide DMA frame status byte
- Tx FIFO
  - 16 x 8 data FIFO
  - TxRDY triggered by programmable filled level of FIFO
  - Status bits for the empty level of Tx FIFO
- Baud Rate Generator—from 50bps up to 64Kbps
- Interrupt control
  - Individual interrupt enable bits
  - Support interrupt Daisy Chain—RDYN (DTACKN) is provided
- Support X.21 pattern recognition
- Lower power consumption

CMOS DUSCC Register Address Map (New registers available by setting internal A7 bit.)

ADDRESS BITS							ACRONYM	REGISTER NAME	MODE	AFFECTED BY RESET
7	6	5	4	3	2	1				
1	c	0	0	0	1	0	IER1	Interrupt enable register 1	R/W	Yes – 00
1	c	0	0	0	1	1	IER2	Interrupt enable register 2	R/W	Yes – 00
1	c	0	0	1	0	1	IER3	Interrupt enable register 3	R/W	Yes – 00
1	c	0	0	1	1	1	RCR	Rx command register	R/W	Yes – 00
1	c	0	1	1	1	0	RFLR	RxFIFO filled level register	R	Yes – 00
1	c	1	1	1	0	0	FTLR	FIFO threshold level register	R/W	Yes – C3
1	c	1	1	1	1	0	TRMR	Tx/Rx misc register	R/W	Yes – 00
1	c	1	1	1	1	1	TFLR	TxFIFO filled level register	R	Yes – 10
x	0	1	1	1	0	1	REA	Reset internal A7 to 0	W	A7 = 0
x	1	1	1	1	0	1	SEA	Set internal A7 to 1	W	A7 = 0
x	0	1	1	1	0	1	CID	Chip identification	R	A7 = 0

Register map — The internal A7 affects the following registers and all other registers are not affected by A7.

A7 = 0	A7 = 1
S1R	IER1
S2R	IER2
TTR	IER3
RTR	RCR
PCR	RFLR
IER	FTLR
IVR/IVRM	TRMR
ICR/MRR	TELR

TTR — Transmitter Timing Register

[3210] – This field selects an output from bit rate generator to be used by the transmitter circuits. Three extra bit rate are provided if new bit rates is chosen by RCR.

[3210] – Bit Rates

0000 50/14.4K. If RCR[1] is set, TTR[3:0] = [0000] chooses 14.4Kbps. If RCR[1] is reset, then it will switch back to default value, 50bps.

0001 75/56K. If RCR[1] is set, TTR[3:0] = [0001] chooses 56Kbps. If RCR[1] is reset, then it will switch back to default value, 75bps.

0010 110/64K. If RCR[1] is set, TTR[3:0] = [0010] chooses 64Kbps. If RCR[1] is reset, then it will switch back to default value, 110bps.

IER1 — Interrupt Enable Register 1.
This register is active only when individual interrupt enable mode is selected.

In ASYNC mode:

[7] Character Comparison

[6] RTS Negated

[5] Overrun

[4] Reserved

[3] BRK End

[2] BRK Start

[1] Frame Error

[0] Parity Error

In COP mode:

[7] EOM Detect

[6] PAD error

[5] Overrun

[4] Reserved

[3] Reserved

[2] SYN detect

[1] CRC/LRC Error

[0] Parity Error

In BOP/BOP LOOP modes:

[7] EOM Detect

[6] ABORT/EOP detect

[5] Overrun

[4] Short frame

[3] Idle/Turnaround Detect

[2] Flag detect

[1] CRC Error

[0] RCL not zero

IER2 — Interrupt Enable Register 2.
This register is active only when individual interrupt enable mode is selected.

In ASYNC mode:

[7] Tx path empty

[6] Reserved

[5] Tx Underrun

[4] CTS Underrun

[3] Send BRK ACK

[2] DPLL error

[1] Delta CTS detect

[0] Delta DCD detect

In COP mode:

[7] Tx path empty

[6] Tx Frame complete

[5] Tx Underrun

[4] CTS underrun

[3] Send SOM ACK

[2] DPLL error

[1] Delta CTS detect/LC detect

[0] Delta DCD detect

In BOP and BOP LOOP modes:

[7] Tx path empty

[6] Tx Frame Complete

[5] Tx Underrun

[4] CTS Underrun/Loop Sending

[3] Send SOM ACK

[2] DPLL error

[1] Delta CTS/LC detect

[0] Delta DCD detect

IER3 — Interrupt Enable Register 3.
This register is active only when individual interrupt enable mode is selected.

[7] Channel Master Interrupt Enable Bit.
This bit is used as ICR[1] or ICR[0] while A7 = 1. This bit is ignored when A7 = 0.

[6] TxRDY Interrupt Enable Bit.
This bit is ignored while original IER is being used.

0 Interrupt not enabled

1 Interrupt generated if TxRDY is asserted.

[5] RxRDY Interrupt Enable Bit.
This bit is ignored while original IER is being used.

0 Interrupt not enabled

1 Interrupt generated if RxRDY is asserted.

[4] Watch Dog Timer Interrupt Enable Bit.
Interrupt generated if no data is loaded into RxFIFO within 128 consecutive bit times after command is issued.

[3] Pattern Recognition Interrupt Enable Bit.
Interrupt generated if any of the pattern recognitions is set.

[2] Reserved

[1] Reserved

[0] Reserved

TRMR — Transmitter/Receiver Misc. Register. This register provides pattern recognition status bits and Tx path empty status bit.

[7:5] Reserved

[4] Tx Path Empty Status Bit.
This bit is set when the last bit of the data is being shifted out of TxD while no more character in the FIFO or in the whole transmitter data path. A '1' written to this bit can clear the status bit. This bit is also cleared if the Tx RESET or Master RESET is issued.

[3] Pattern 0 Status Bit.
This bit is set when Rx receives 16 contiguous 0's after pattern recognition is enabled. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

[2] Pattern 1 Status Bit.
This bit is set when Rx receives 16 contiguous 1's after pattern recognition is enabled. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

[1] Pattern Alternating 01 Status Bit.
This bit is set when Rx receives 16 contiguous alternating 01 or 10 after pattern recognition is enabled. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

[0] WTD Status Bit.
This bit is set whenever the WTD is time out. This bit is ORed together with RxRDY status bit in the GSR. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

RCR — Rx Command Register.

[7] – 0 Disable Watch Dog Timer.

1 Enable Watch Dog Timer. WTD status is set if no data is loaded into RxFIFO within 128 consecutive bit times after command is issued.

[6] – 0 Disable DMA status byte. See detail in DFSB.

1 Enable DMA status byte. The status byte for the whole frame is fifoed following last byte of frame while DMA is in progress.

[5] – 0 Disable Pattern Recognition all 0's.

1 Enable Pattern Recognition all 0's. This command will have the receiver start to hunt 16 consecutive 0's.

[4] – 0 Disable Pattern Recognition all 1's.

1 Enable Pattern Recognition all 1's. This command will have the receiver start to hunt 16 consecutive 1's. The status bit is shown in TRMR.

[3] – 0 Disable Pattern Recognition alternating 01.

1 Enable Pattern Recognition alternating 01. This command will have the receiver start to hunt 16 contiguous alternating 01 or 10. The status bit is shown in TRMR.

[2] – 0 Default mode. No individual interrupt enable mode.

1 Enable individual interrupt enable mode. In this mode, IER1 and IER2 are used and original IER is ignored.

[1] – 0 Default mode. No new bit rates can be selected.

1 Three additional new bit rates, 14.4k, 56k, and 64k can be chosen through TTR[3:0]. See TTR[3:0] for further information.

[0] Reserved

TELR — TxFIFO Empty Level Register.
This register indicates the TxFIFO empty level. A read from this register can tell the current available space(s) for the TxFIFO.

[7:5] Reserved

[4:0] This field selects the available location(s) for the TxFIFO.

00000 – 0 bytes empty (implies TxFIFO full)

00001 – 1 byte empty

00010 – 2 bytes empty
00011 – 3 bytes empty
00100 – 4 bytes empty
00101 – 5 bytes empty
00110 – 6 bytes empty
00111 – 7 bytes empty
01000 – 8 bytes empty
01001 – 9 bytes empty
01010 – 10 bytes empty
01011 – 11 bytes empty
01100 – 12 bytes empty
01101 – 13 bytes empty
01110 – 14 bytes empty
01111 – 15 bytes empty
10000 – 16 bytes empty (implies TxFIFO empty)

RFLR — RxFIFO Filled Level Register.
This register indicates the RxFIFO filled level. Nine status bits are fifoed with each byte received. A read from this register can tell the current FIFO filled level.

[7:5] Reserved

[4:0] This field selects the RxFIFO filled level.

00000 – 0 byte filled (implies RxFIFO empty)
00001 – 1 bytes filled
00010 – 2 bytes filled
00011 – 3 bytes filled
00100 – 4 bytes filled
00101 – 5 bytes filled
00110 – 6 bytes filled
00111 – 7 bytes filled
01000 – 8 bytes filled
01001 – 9 bytes filled
01010 – 10 bytes filled
01011 – 11 bytes filled
01100 – 12 bytes filled
01101 – 13 bytes filled
01110 – 14 bytes filled
01111 – 15 bytes filled
10000 – 16 bytes filled (implies RxFIFO full)

FTLR — FIFO Threshold Level Register.
This register indicates both TxFIFO and RxFIFO interrupt threshold level.

[7:5] This field selects the TxFIFO Threshold Level. To use threshold level to generate interrupt request, TxRDY activate bit on OMR could be set to '1' (FIFO empty). The default threshold level is 4 byte locations available. TxRDY does not clear until the TxFIFO is full or transmitter is disabled.

0000 – 1 byte empty (only one space available)
0001 – 2 bytes empty
0010 – 3 bytes empty
0011 – 4 bytes empty (default mode)
0100 – 5 bytes empty
0101 – 6 bytes empty
0110 – 7 bytes empty
0111 – 8 bytes empty
1000 – 9 bytes empty
1001 – 10 bytes empty
1010 – 11 bytes empty
1011 – 12 bytes empty
1100 – 13 bytes empty
1101 – 14 bytes empty
1110 – 15 bytes empty
1111 – 16 bytes empty (TxFIFO empty)

[4:0] This field selects the RxFIFO threshold level. To generate RxRDY interrupt or DMA request, the RxFIFO filled level must be equal or greater than the threshold level.

To use the threshold level to generate interrupt request, RxRDY activate bit on OMR could be set to '1' (FIFO full). The default threshold level is 4 characters. RxRDY is set when more than one byte is in the FIFO. It resets when the receiver FIFO is ready or the receiver is disabled.

0000 – 1 byte filled
0001 – 2 bytes filled
0010 – 3 bytes filled
0011 – 4 bytes filled (default mode)
0100 – 5 bytes filled
0101 – 6 bytes filled
0110 – 7 bytes filled
0111 – 8 bytes filled
1000 – 9 bytes filled
1001 – 10 bytes filled
1010 – 11 bytes filled
1011 – 12 bytes filled
1100 – 13 bytes filled
1101 – 14 bytes filled
1110 – 15 bytes filled
1111 – 16 bytes filled (Rx FIFO full)

REA — Reset Internal A7 to 0.
A write to this address set the address bit to 6 bits. This is the default mode. No new registers can be accessed. Data is ignored during the write cycle.

SEA — Set Internal A7 to 1.
A write to this register automatically extend address bit to 7 bits. Therefore all the new registers can be accessed. Data is ignored during the write cycle.

CID — Chip Identification.
A read operation provides software signature which can tell the part version.

DATA OUTPUT	PART VERSION
FFH	NMOS DUSCC
EFH	CMOS DUSCC Rev. A

DFSB — DMA Frame Status Byte.
In RxDMA cycle, this status byte can be attached to the FIFO following last byte of frame (last byte means data with EOM status bit set). This byte is updated frame by frame by logical 'OR-ing' of prior status bytes with the present status byte of the frame and only used for COP or BOP/BOPL modes while DMA transfers are in progress. The DONEN (EOPN) will not be set until this byte pops to the top of the FIFO.

To enable this mode user has to send the command through CCR. (**ABORT does NOT reset DFSB but RxReset does**)

COP mode

[7] Reserved

[6] Reserved

[5] Reserved

[4] PAD ERROR

[3] DPLL error

[2] Overrun

[1] BCC ERROR

[0] Parity error

BOP/BOPL mode

[7:5] Residual character length. Same as TRSR[2:0]

[4] ABORT

[3] DPLL error

[2] Overrun

[1] CRC error

[0] Short Frame

CCR — Channel Command Register.

76543210

01xx0100 Default mode. Disable new fifoed status bits.

01xx0101 Enable new fifoed status bits. In this mode all of the following status bits in RSR/TRSR reflect the status of the current character at the top of the RxFIFO.

ASYNC:	#	RSR[7]	— Character Compare
		RSR[5]	— Overrun
		RSR[2]	— BRK Start
	#	RSR[1]	— FE
	#	RSR[0]	— PE
COP :	#	RSR[7]	— EOM
		RSR[6]	— Pad Error
		RSR[5]	— Overrun
	#	RSR[1]	— LRC/CRC error
	#	RSR[0]	— PE
BOP/BOPL:	#	RSR[7]	— EOM
		RSR[6]	— ABORT/EOP
		RSR[5]	— Overrun
		RSR[4]	— Short frame
	#	RSR[1]	— CRC CRC error
	#	RSR[0]	— RCL not zero

: Fifoed status bits in NMOS DUSCC.

Since abort detect and short frame may not have data byte to attach, a dummy byte is provided for status attachment. This dummy byte includes the current data in the shift register. Therefore, whenever the abort or short frame occurs, the status bit is always attached to this dummy byte.

****NOTE**** In BOP/BOPL mode, TRSR[2:0] is always fifoed no matter what kind of command is issued.

GSR — General Status Register.
This register remain almost same as NMOS DUSCC's GSR except RxRDY and Rx/Tx status bits. For RxRDY status bit, it combines Rx WDT status bit with original Rx Ready together if Rx WDT is enabled. For the Tx/Rx status bit, it combines original Receiver/transmitter status bits with pattern recognition status bits and Tx path empty bit together if those functions are individually enabled.

[7] CH.B External or C/T status.

[6] CH.B Rx/Tx status. This bit is set whenever one of the following status bits is set. RSR[7:0], TRSR[7:3], Tx path empty, Pattern recognitions. The Tx path empty and Pattern recognitions can affect GSR[6] only if those functions are enabled individually.

[5] CH.B TxRDY.

[4] CH.B RxRDY. This bit is set either when Receiver Ready is active or when WDT status bit is set if the WDT is enabled.

[3] CH.A External or C/T status.

[2] CH.A Rx/Tx status. This bit is set whenever one of the following status bits is set. RSR[7:0], TRSR[7:3], Tx path empty, Pattern recognitions. The Tx path empty and Pattern recognitions can affect GSR[6] only if those functions are enabled individually.

[1] CH. A TxRDY.

[0] CH.A RxRDY. This bit is set either when Receiver Ready is active or when WDT status bit is set if the WDT is enabled.

BISYNC control:

CMR1 [5]	CMR [4:3]	
0	00	EBCDIC, NO parity, 8 bit data, 8 bit CTRL character.
1	00	ASCII, NO parity, 8 bit data, 8 bit CTRL character. Odd parity bit is generated by users. It's same as NMOS DUSCC. Receiver check the parity bit by loop-up table. If an LRC BCC is selected in CMR[2:0] then LRC-8 is used (the MSB of the LRC is the logical XOR of all MSBs in the frame.)
1	01	ASCII, No parity, 8 bit data, 8 bit CTRL character. The receiver only check 7 bits for the CTRL character and ignore the MSB of each character. If an LRC BCC is selected in CMR[2:0] then LRC-7 is used (the MSB of the LRC is 0).
1	10	ASCII, ODD parity, 7 bit data + 1 odd parity bit, 7 bit CTRL char + 1 odd parity bit. Parity bit is generated/checked by DUSCC. Any CTRL character as parity error will not be treated as a CTRL character. If an LRC BCC is selected in CMR[2:0] then LRC-7 is used. The MSB of the LRC will be the ODD PARITY value computed from the 7 other bits that comprise the LRC.
1	11	ASCII, EVEN parity. Similar to CMR[4:3] = 10 except parity bit is even.

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SCN68562

Dual universal serial communications controller (DUSCC)

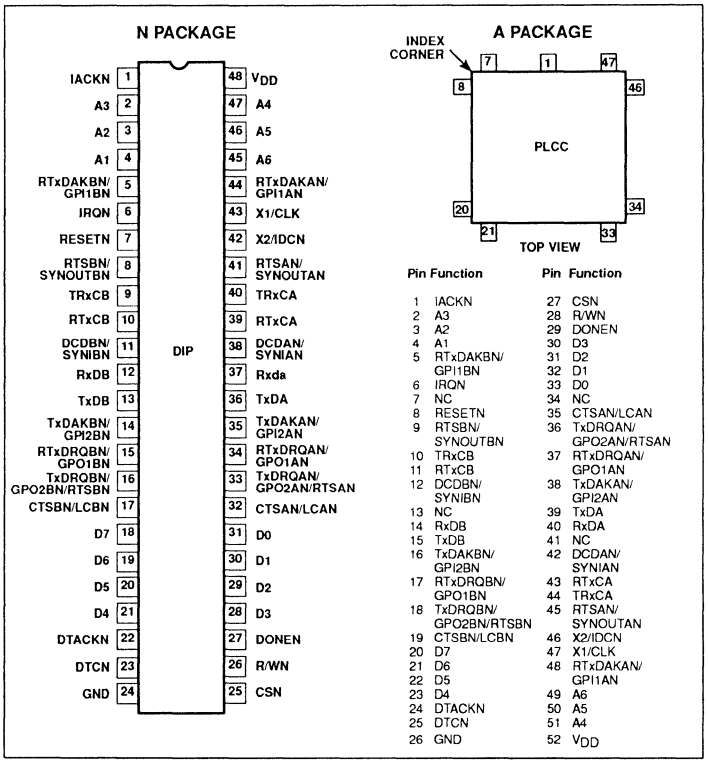
DESCRIPTION

The Signetics SCN68562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN68562 interfaces to the 68000 MPUs via asynchronous bus control signals and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RESETN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2/IDCN
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	DTACKN	50	A5
25	DTCN	51	A4
26	GND	52	VDD

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

Dual universal serial communications controller (DUSCC) SCN68562

FEATURES

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with the Signetics SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general I/O pins per channel
  - CTS and DCD programmable autoenables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbs and receive up to 2Mbps data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

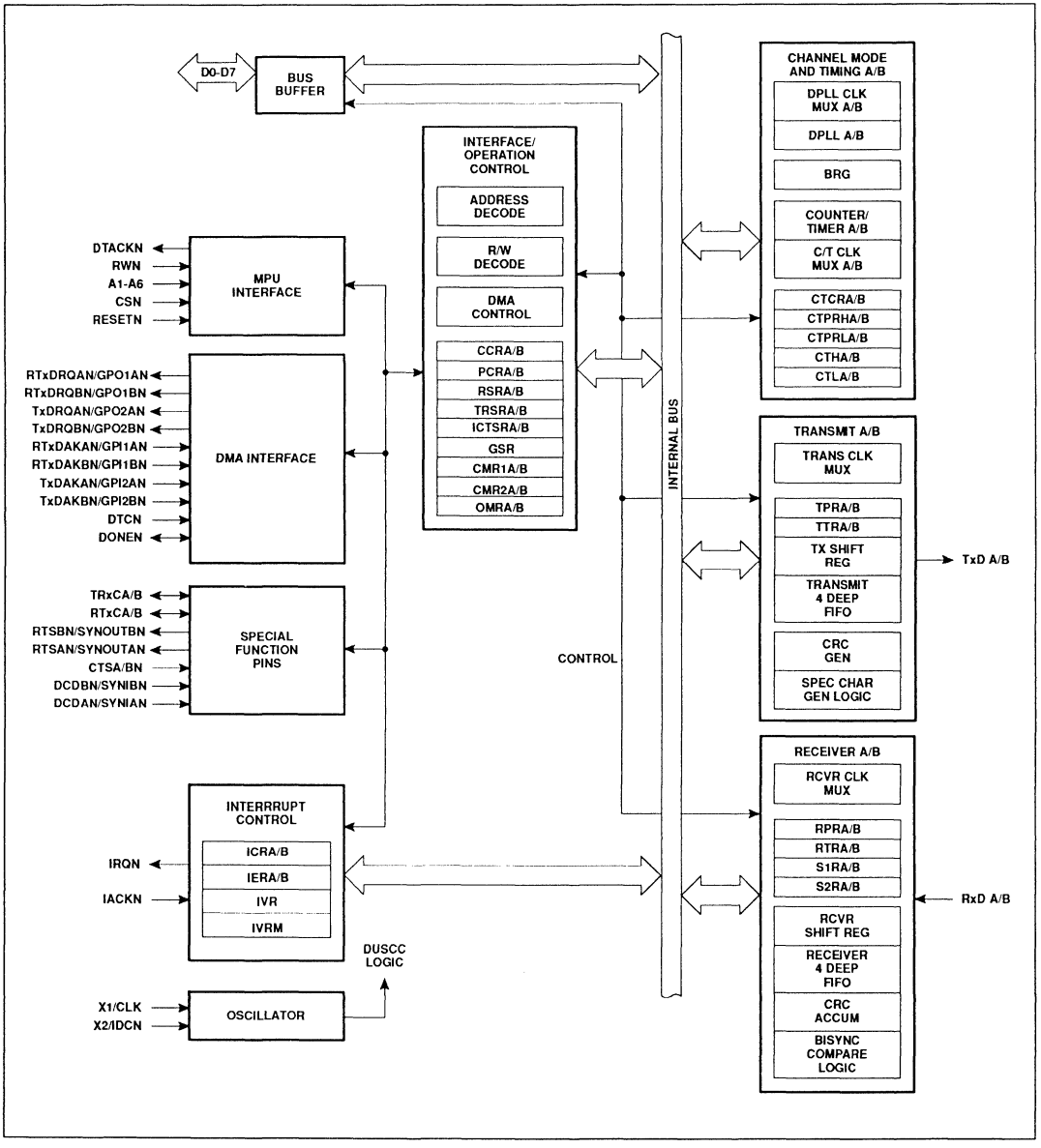
Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for 1 field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs linefill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0°C to +70°C	
	Serial Data Rate = 2.5Mbps Maximum	Serial Data Rate = 4Mpbs Maximum
48-Pin Plastic DIP	SCN68562C2N48	SCN68562C4N48
52-Pin PLCC	SCN68562C2A52	SCN68562C4A52

BLOCK DIAGRAM



PIN DESCRIPTION

In this data sheet, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. N at the end of a pin name signifies the signal associated with the pin is active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by A/B after the name of the pin and the active-Low state indicator, N, if applicable. A similar method is used for registers provided for both channels: these are designated by either an underline or by A/B after the name.

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
A1 – A6	4-2, 45-47	I	**Address Lines:** Active-High. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0 – D7	31-28, 21-18	I/O	**Bidirectional Data Bus:** Active High, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN is Low, during interrupt acknowledge cycles and single-address DMA acknowledge cycles.
R/WN	26	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle when a cycle is initiated by assertion of the CSN input.
CSN	25	I	**Chip Select:** Active-Low input. When Low, data transfers between the CPU and the DUSCC are enabled on D0 – D7 as controlled by the R/WN and A1 – A6 inputs. When CSN is High, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single-address DMA transfers) and D0 – D7 are placed in the 3-State condition.
DTACKN	22	O	**Data Transfer Acknowledge:** Active-Low, 3-State. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. The signal is negated when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive state (3-State) a short period after it is negated. In a single address DMA mode, data is latched with the falling edge of DTCN. DTACKN is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-State) a short period after it is negated. When negated, DTACKN becomes an open-drain output and requires an external pull-up resistor.
IRQN	6	O	**Interrupt Request:** Active-Low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus.
IACKN	1	I	**Interrupt Acknowledge:** Active-Low. When IACKN is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted.
X1/CLK	43	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, and external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals.
X2/IDCN	42	I/O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide and interrupt daisy chain active-Low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2, is not used as an interrupt daisy chain output.
RESETN	7	I	**Master Reset:** Active-Low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1. Reset in asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	O	**Channel A (B) Transmitter Serial Data Output:** The least signifiicant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X). The maximum external receiver/transmitter clock frequency is 4MHz.

PIN DESCRIPTION (Continued)

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
TRxCA, TRxCB	40, 9	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1/2). The maximum external receiver/transmitter clock frequency is 4MHz.
CTSA/BN, LCA/BN	32, 17	I/O	**Channel A (B) Clear-To-Send Input or Loop Control Output:** Active-Low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the COP loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-Low input, it acts as an enable for the receiver or can be used as a general purpose input for the DCD function, the DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. As an active-Low external sync input, it is used in COP modes to obtain character synchronization without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-Low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-Low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control (see Detailed Operation).
RTxDAKA/BN, GPI1A/BN	44, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. For half-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO or load transmitter FIFO) is beginning. For full-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GP12A/BN	35, 14	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DTCN	23	I	**Device Transfer Complete:** Active-Low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
DONEN	27	I/O	**Done:** Active-Low, open-drain. See Detailed Operation for a description of the function of this pin.
RTSA/BN, SYNOUTA/BN	41, 8	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-Low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{DD}	48	I	+5V ± 10% power input.
GND	24	I	Signal and power ground input.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage Temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	-0.5 to V_{CC} +0.5	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 40°C/W for plastic DIP and 42°C/W for PLCC.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 2, 5] T_A = 0 to +70°C, V_{CC} = 5.0V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage:					
	All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage:					
	All except X1/CLK		2.0			V
	X1/CLK		2.4		V_{CC}	V
V_{OL}	Output low voltage:					
	All except IRQN, DONEN	I_{OL} = 5.3mA			0.5	V
	IRQN, DONEN	I_{OL} = 8.8mA			0.5	V
	Output high voltage:					
V_{OH}	(Except open drain outputs)	I_{OH} = -400µA	2.4			V
I_{ILX1}	X1/CLK input low current[4]	V_{IN} = 0, X2 = GND	-5.5		0.0	mA
I_{IHX1}	X1/CLK input high current[4]	V_{IN} = V_{CC}, X2 = GND			1.0	mA
I_{ILX2}	X2 input low current[4]	V_{IN} = 0, X1 = open	-100			µA
I_{IHX2}	X2 input high current[4]	V_{IN} = V_{CC}, X1 = open			100	µA
I_{IL}	Input low current					
	DTCN, TxDAKA/BN, RTxDAKA/BN	V_{IN} = 0	-40			µA
I_L	Input leakage current	V_{IN} = 0 to V_{CC}	-5		5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	-5			µA
I^{ODL}	Open drain output low current in off	V_{IN} = 0				
	state: DONEN		-120		-25	µA
	IRQN, DTACKN		-5			µA
I_{ODH}	Open drain output high current in off	V_{IN} = V_{CC}				
	state: DONEN, IRQN, DTACKN				5	µA
I_{CC}	Power supply current	V_O = 0 to V_{CC}			275	mA
C_{IN}	Input capacitance[3]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[3]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[3]	V_{CC} = GND = 0			20	pF

NOTES:
1. Parameters are valid over specified temperature and voltage range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0V and 2.8V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. These values were not explicitly tested; they are guaranteed by design and characterization data.
4. X1/CLK and X2 are not tested with a crystal installed.
5. This specification applies to revision C, revision E and later revisions.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4] T_A = -55 to +110°c, V_{CC} = 5V ± 10%

NO.	FIGURE	PARAMETER	LIMITS Min	Typ	Max	UNIT
1	12	RESETN pulse width	1.2			µS
2	13,15	A1 - A6 set-up time to CSN Low	10			nS
3	13.15	A1 - A6 hold time from CSN High	0			nS
4	13,15	RWN set-up time to CSN Low	0			nS
5	13,15	RWN hold time to CSN High	0			nS
6	13,15	CSN High pulse width[4]	160			nS
7	13,16	CSN or IACKN High from DTACKN Low	30			nS
7A	16	IACKN High to DTACKN High			200	nS
8	13,16	Data valid from CSN or IACKN Low			300	nS
9	13	Data bus floating from CSN High[7]			100	nS
10	15	Data hold time from DTACKN Low[5]	0			nS
11	13,16	DTACKN Low from read data ready	0			nS
12	13,15	DTACKN Low from CSN Low			560	nS
12A	15	CSN Low to write data valid			50	nS
13	13,15	DTACKN High from CSN High			150	nS
14	13,15	DTACKN high impedance from CSN High			185	nS
15	16	DTACKN Low from IACKN Low			550	nS
16	17	GPI input set-up time to CSN Low	20			nS
17	17	GPI input hold time from CSN Low	100			nS
18	17	GPO output valid from DTACKN Low			300	nS
19	18	IRQN High from:				
		Read RxFIFO (RxRDY interrupt)			450	nS
		Write TxFIFO (TxRDY interrupt)[8]			450	nS
		Write RSR (Rx condition interrupt)[8]			400	nS
		Write TRSR (Rx/Tx interrupt)[8]			400	nS
		Write ICTSR (port change and CT int.)[8]			400	nS
20	19	X1/CLK High or Low time	25			nS
		X1/CLK frequency	2.0	14.745	16	MHz
		CTCLK High or Low time	100	6		nS
		CTCLK frequency	0		4	MHz
		RxC High or Low time	110			nS
		RxC frequency (16X or 1X)[9]	0		4	MHz
		TxC High or Low time	110			nS
		TxC frequency (16X or 1X)	0		4	MHz
21	20	TxD output from TxC input Low (1X)			240	nS
		(16X)			435	nS
22	20	TxD output from TxC output Low			50	nS
23	21	RxD data set-up time to RxC High	50			nS
24	21	RxD data hold time from RxC High	50			nS
25	22	IACKN Low to daisy chain Low			200	nS
26	24	Data valid from receive DMA ACKN			300	nS
27	23,24	DTCN width	100			nS
28	23,24	RDYN Low to DTCN Low	80			nS
29	24	Data bus float from DTCN Low[7]			200	nS
30	23,24	DMA ACKN Low to RDYN (DTACKN) Low			360	nS
31	23,24	RDYN High from DTCN Low			230	nS
32	23,24	RDYN High impedance from DTCN Low			250	nS
33	24	Receive DMA REQN High from DMA ACKN Low			325	nS
34	24	Receive DMA ACKN width	150			nS
35	23,24	Receive DMA ACKN Low to DONEN Low			250	nS
36	23	Data set-up to DTCN Low	50			nS
37	23	Data hold from DTCN Low[6]	50			nS
38	23	Transmit DMA REQN High from ACKN Low			340	nS
39	23	Transmit DMA ACKN width	150			nS
40	23	Transmit DMA ACKN Low to DONEN Low output			250	nS
40A	23	DTCN Low DONEN output High			260	nS
41	25	CSN Low to transmit DONEN Low output			300	nS
42	25	CSN Low to transmit DMA REQ negated			400	nS
43	25	CSN Low to receive DONEN Low			300	nS
44	25	CSN Low to receive DMA REQ negated			400	nS

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For D.C. and functional testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 4.4V All time measurements are referenced at input voltages of 0.2V and 2.4V for all inputs. Output levels are referenced at 1.5V.
3. Test conditions for outputs: C_L = 150pF, except open-drain outputs. Test condition for open-drain outputs: C_L = 50pF to GND, R_L = 2.7kΩ to V_{CC} except DTACKN whose RL - 820Ω to V_{CC} and C_L = 150pF to GND and DONEN which requires C_L = 50pF to GND and RL = 1kΩ to V_{CC}.
4. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus cycles are not performed.
5. Execution of the valid command (after it is latched) requires three falling edges of X1 (see Figure 14).
6. In single address DMA mode write operation, data is latched by the falling edge of DTCN.
7. These values were not explicitly tested, they are guaranteed by design and characterization data.
8. These timings are from the falling edge of DTACKN (not CSN rising).
9. X1/CLK frequency must be at least four times the receiver serial data rate.

REGISTERS

The addressable registers of the DUSCC are shown in Table 1. The following rules apply to all registers:

1. A read from a reserved location in the map results in a read from the 'null register'. The null register returns all ones for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle without a write being performed.
2. Unused bits of a defined register are read as zeros, unless ones have been loaded after master reset.
3. Bits that are unused in the chosen mode but are used in others are readable and writable but their contents are ignored in the chosen mode.
4. All registers are addressable as 8-bit quantities. To facilitate operation with the 68000 MOVEP instruction, addresses are ordered such that certain sets of registers may also be accessed as words or long words.

The operation of the DUSCC is programmmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The contents of certain control registers are initialized on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems, e.g., changing the channel mode at an inappropriate time may cause the reception or transmission of an incorrect character. In general, the contents of registers which control transmitter or receiver operation, or the counter/timer, should be changed only when they are not enabled.

The DUSCC registers can be separated into five groups to facilitate their usage:

1. Channel mode configuration and pin description registers.
2. Transmitter and receiver parameter and timing registers.
3. Counter/timer control and value registers.
4. Interrupt control and status registers.
5. Command register.

This arrangement is used in the following description of the DUSCC registers.

Channel Mode Configuration and Pin Description Registers

There are five registers in this group for each channel. The bit format for each of these registers is contained in Table 2. The primary function of these registers is to define configuration of the channels and the function of the programmable pins. A channel cannot be dynamically reconfigured. Do not write to CMR1 or CMR2 if the receiver or transmitter is enabled.

Channel Mode Register 1 (CMR1A, CMR1B)

[7:6] Data Encoding — These bits select the data encoding for the received and transmitted data:

00 If the DPLL is set to NRZI mode (see DPLL commands), it selects positive logic (1 = High, 0 = Low). If the DPLL is set to FM mode (see DPLL commands), Manchester (bi-phase level) encoding is selected.

01 NRZI. Non-return-to-zero inverted.

10 FM0. Bi-phase space.

11 FM1. Bi-phase mark.

[5] Extended Control (BOP) —

0 No. A one-octet control field follows the address field.

1 Yes. A two-octet control field follows the address field.

[5] Parity (COP/ASYNC), Code Select (BISYNC) —

0 Even parity if with parity is selected by [4:3] or a 0 in the parity bit position if force parity is selected by [4:3]. In BISYNC protocol mode, internal character comparisons are made using EBCDIC coding.

1 Odd parity if with parity is selected by [4:3] or a 1 in the parity bit position if force parity is selected by [4:3]. In BISYNC protocol mode, internal character comparisons are made using 7-bit plus odd parity ASCII coding. (Note: The receiver should be programmed for 7-bit characters, RPR[1:0] = 11, with no parity, CMR1[4:3] = 00.)

[4:3] Address Mode (BOP) — This field controls whether a single octet or multiple octets follow the opening FLAG(s) for both the receiver and the transmitter. This field is activated by selection of BOP secondary mode through the channel protocol mode bits CMR1[2:0] (see Detailed Operation).

00 Single-octet address.

01 Extended address.

10 Dual-octet address.

11 Dual-octet address with group.

[4:3] Pairty Mode (COP/ASYNC) — This field selects the parity mode for both the receiver and the transmitter. A parity bit is added to the programed character length if with parity or force parity is selected:

00 No pairty. Required when BISYNC protocol mode is programmed.

01 Reserved.

10 With parity. Odd or even parity is selected by [5].

11 Force parity. The parity bit is forced to the state selected by [5].

[2:0] Channel Protocol Mode — This field selects the operational protocol and submode for both the receiver and transmitter:

000 BOP Primary. No address comparison is performed. For receive, all characters received after the opening FLAG(s) are transferred to the FIFO.

001 BOP Secondary. This mode activates the address modes selected by [4:3]. Except in the case of extended address ([4:3] = 01), and address comparison is performed to determine if a frame should be received. Refer to Detailed Operation for details of the various addressing modes. If a valid comparison occurs, the receiver is activated and the address octets and all subsequent received characters of the frame are transferred to the receive FIFO.

010 BOP Loop. The DUSCC acts as a secondary station in a loop. The GO-ON-LOOP and GO-OFF-LOOP commands are used to cause the DUSCC to go on and off the loop. Normally, the TxD output echos the RxD input with a two-bit time delay. If the transmitter is enabled and the 'go active on poll' command has been asserted, the transmitter will begin sending when an EOP sequence consisting of a zero followed by seven ones is detected. The DUSCC changes the last one of the EOP to zero, making it another FLAG, and then operates as described in the Detailed Operation section. The loop sending status bit (TRSR[6]_ is asserted concurrent with the beginning of transmission. The frame should normally be terminated with an EOM followed by an echo of the marking RxD line so that secondary stations further down the loop can append their messages to the messages from up-loop stations by the same process. If the 'go active on poll' command is not asserted, the transmitter remains inactive (other than echoing the received data) even when the EOP sequence is received.

011 BOP Loop without address comparison. Same as normal loop mode except that address field comparisons are disabled. All received frames are transmitted to the CPU.

Table 1. DUSCC Register Address Map

ADDRESS BITS* 6 5 4 3 2 1	ACRONYM	REGSITER NAME	MODE	AFFECTED BY RESET
c 0 0 0 0 0	CMR1	Channel Mode Register 1	R/W	Yes—00
c 0 0 0 0 1	CMR2	Channel Mode Register 2	R/W	Yes—00
c 0 0 0 1 0	S1R	SYN 1/Secondary Address 1 Register	R/W	No
c 0 0 0 1 1	S2R	SYN 2/Secondary Address 2 Register	R/W	No
c 0 0 1 0 0	TPR	Transmitter Parameter Register	R/W	Yes—00
c 0 0 1 0 1	TTR	Transmitter Timing Register	R/W	No
c 0 0 1 1 0	RPR	Receiver Parameter Register	R/W	Yes—00
c 0 0 1 1 1	RTR	Receiver Timing Register	R/W	No
c 0 1 0 0 0	CTPRH	Counter/Timer Preset Register High	R/W	No
c 0 1 0 0 1	CTPRL	Counter/Timer Preset Register Low	R/W	No
c 0 1 0 1 0	CTCR	Counter/Timer Control Register	R/W	Yes—00
c 0 1 0 1 1	OMR	Output and Miscellaneous Register	R/W	Yes—00
c 0 1 1 0 0	CTH	Counter/Timer High	R	No
c 0 1 1 0 1	CTL	Counter/Timer Low	R	No
c 0 1 1 1 0	PCR	Pin Configuration Register	R/W	Yes—00
c 0 1 1 1 1	CCR	Channel Command Register	R/W	No
c 1 0 0 X X	TxFIFO	Transmitter FIFO	W	No
c 1 0 1 X X	RxFIFO	Receiver FIFO	R	No
c 1 1 0 0 0	RSR	Receiver Status Register	R/W**	Yes—00
c 1 1 0 0 1	TRSR	Transmitter and Receiver Status Register	R/W**	Yes—00
c 1 1 0 1 0	ICTSR	Input and Counter/TImer Status Register	R/W**	Yes
d 1 1 0 1 1	GSR	General Status Register	R/W**	Yes—00
c 1 1 1 0 0	IER	Interrupt Enable Register	R/W	Yes—00
c 1 1 1 0 1		Not used		
0 1 1 1 1 0	IVR	Interrupt Vector Register— Unmodified	R/W	Yes—0F
1 1 1 1 1 0	IVRM	Interrupt Vector Register— Modified	R	Yes—0F
0 1 1 1 1 1	ICR	Interrupt Control Register	R/W	Yes—00
1 1 1 1 1 1		Not used		

NOTES:

* c = 0 for Channel A, c = 1 for Channel B.
d = don't care — register may be accessed as either channel.
x = don't care — FIFOs are addressable at any of four adjacent addresses to allow them to be addressed as byte/word/long word with the 68000 MOVEP instruction.

** A write to this register may perform a status resetting operation.

100 COP Dual SYN. Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R and S2R (SYN1-SYN2), including parity bits if any.

101 COP Dual SYN (BISYNC). Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R and S2R (SYN1-SYN2). In this mode, special transmitter and receive logic is activated. Transmitter and receiver character length must be programmed to 8 bits and no parity (see Detailed Operation).

110 COP Single SYN. Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R (SYN1), including parity bit if any. This mode is required when the external sync mode is selected (see description of RPR[4], BOP/COP).

111 Asynchronous. Start/stop format.

Channel Mode Register 2 (CMR2A, CMR2B)

[7:6] Channel Connection — This field selects the mode of operation of the channel. The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character.

00 Normal mode. The transmitter and receiver operate independently in either half- or full-duplex, controlled by the respective enable commands.

01 Automatic echo mode. Automatically retransmits the received data with a half-bit time delay (ASYNC, 16X clock mode) or a two-bit time delay (all other modes). The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxD output.
2. The receiver clock is used for the transmitter for ASYNC 16X clock mode. For other modes the transmitter clock must be supplied.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and underrun status bits are inactive.
5. The received parity and/or FCS are checked if required, but are not regenerated for transmission, i.e., transmitted parity and/or FCS are as received.
6. In ASYNC mode, character framing is checked, but the stop bits are retransmitted as received. A received break is echoed as received.
7. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

10 Local loopback mode. In this mode:

1. The transmitter data output and clock are internally connected to the receiver.
2. The transmit clock is used for the receiver if NRZI or NRZ encoding is used. For FM or Manchester encoding because the receiver clock is derived from the DPLL, the DPLL source clock must be maintained.
3. The TxD output is held High.
4. The RxD input is ignored.
5. The receiver and transmitter must be enabled.
6. CPU to transmitter and receiver communications continue normally.

11 Reserved.

[5:3] Data Transfer Interface— This field specifies the type of data transfer between the DUSCC's Rx and TxFIFOs and the CPU. All interrupt and status functions operate normally regardless of the data transfer interface programmed. Refer to Detailed Operation for details of the various DMA transfer interfaces.

000 Half-duplex single address DMA.

001 Half-duplex dual address DMA.

010 Full-duplex single address DMA.

011 Full-duplex dual address DMA.

100 Wait on receive only. In this mode a read of a non-empty receive FIFO results in a normal bus cycle. However, if the receive FIFO of the channel is empty when a read Rx FIFO cycle is initiated, the DTACKN output remains negated until a character is received and loaded into the FIFO. DTACKN is then asserted and the cycle is completed normally.

101 Wait on transmit only. In this mode a write to a non-full transmit FIFO results in a normal bus cycle. However, if the transmit FIFO of the channel is full when a write TxFIFO cycle is initiated, the DTACKN output remains negated until a FIFO position becomes available for the new character. DTACKN is then asserted and the cycle is completed normally.

110 Wait on transmit and receive. As above for both wait on receive and transmit operations.

111 Polled or interrupt. DMA and wait function of the channel are not activated. Data transfers to the Rx and TxFIFOs are via normal bus read and write cycles in response to polling of the status registers and/or interrupts.

[2:0] Frame Check Sequence Select — This field selects the optional frame check sequence (FCS) to be appended at the end of a transmitted frame. When CRC is selected in COP, then no pairty and 8-bit character length must be used. The selected FCS is transmitted as follows:

1. Following transmission of a FIFOed character tagged with the 'send EOM' command.
2. If underrun control (TPR[7:6]) is programmed for TEOM, upon occurrence of an underrun.
3. If TEOM on zero count or done (TPR[4]) is asserted and the counter/timer is counting transmitted characters, after transmission of the character which causes the counter to reach zero count.
4. In DMA mode with TEOM on zero count or done (TPR[4]) set, after transmission of a character if DONEN is asserted when that character was loaded into the TxFIFO by the DMA controller.

000 No frame check sequence.

001 Reserved

010 LRC8: Divsior = $x^8 + 1$, dividend preset to zeros. The Tx sends the calculated LRC non-inverted. The Rx indicates and error if the computed LRC is not equal to 0. Valid for COP modes only.

011 LRC8: Divisor = $x^8 + 1$, dividend preset to ones. The Tx sends the calculated LRC non-inverted. The Rx indicates an error if the computed LRC is not equal to 0. Valid for COP modes only.

100 CRC16: Divisor - $x^{16} + x^{15} + x^2 + 1$, dividend preset to zeros. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the comuted CRC is not equal to 0. Not valid for ASYNC mode.

101 CRC16: Divisor = $x^{16} + x^{15} + x^2 + 1$, dividend preset to ones. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the computed CRC is not equal to 0. Not valid for ASYNC mode.

110 CRC-CCITT: Divisor = $x^{16} + x^{12} + x^5 + 1$, dividend preset to zeros. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the computed CRC is not equal to 0. Not valid for ASYNC mode.

111 CRC-CCITT: Divisor = $x^{16} + x^{12} + x^5 + 1$, dividend preset to ones. The Tx sends the calculated CRC inverted. The Rx indicates an error if the computed CRC is not equal to H'F0B8'. Not valid for ASYNC mode.

SYN1/Secondary Address 1 Register (S1RA, S1RB)

[7:0] Character Compare — In ASYNC mode this register holds a 5- to 8-bit long bit pattern which is ocmpared with received characters. if a match occurs, the character compare status bit (RSR[7]) is set. This field is ignored if the receiver is in a break condition.

In COP modes, this register contains the 5- to 8-bit SYN1 bit pattern, right justified. Parity bit need not be included in the value placed in the register even is parity is specified in CMR1[4:3]. However, a character received with parity error, when parity is specified, will not match. In ASYNC, or COP modes, if parity is specified, then any unused bits in this register must be programmed to zeros. In BOP secondary mode it contains the address used to compare the first received address octet. The register is not used in BOP primary mode or secondary modes where address comparisons are not made, such as when extended addressing is specified.

SYN2/Secondary Address 2 Register (S2RA, S2RB)

[7:0] — This register is not used in ASYNC, COP single SYN, BOP primary modes, BOP secondary modes with single address field, and BOP secondary modes where address comparisons are not made, such as when extended addressing is specified.

In COP dual SYN modes, it contains the 5- to 8-bit SYN2 bit pattern, right justified, Parity bit need not be included in the value placed in the register even if parity is specified in CMR1[4:3]. However, a character received with parity error, when parity is specified, will not match. If parity is specified, then any unused bits in this register must be programmed to zeros. In BOP secondary mode using two address octets, it contains the partial address used to compare the second received address octet.

Pin Configuration Register (PCRA, PCRB)

This register selects the functions for multipurpose I/O pins.

[7] X2/IDC — This bit is defined only for PCRA. It is not used in PCRB.

0 The X2/IDCN pin is used as a crystal connection.

1 The X2/IDCN pin is the interrupt daisy chain output.

[6] GPO2/RTS — The function of this pin is programmable only when not operating in full-duplex DMA mode.

Table 2. Channel Configuration/Pin Definition Registers Bit Formats

CHANNEL MODE REGISTER 1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Data Encoding		Extended Control	Address Mode (BOP)		Channel Protocol Mode		
(CMR1A, CMR1B)	00 — NRZ/Manchester 01 — NRZI 10 — FM0 11 — FM1		BOP only 0 — no 1 — yes	00 — 8-bit 01 — extended address 10 — 16-bit 11 — 16-bit w/group		000 — BOP primary 001 — BOP secondary 010 — BOP loop 011 — BOP loop – no adr. comp.		
			Parity*	Parity Mode (COP/ASYNC)				
			0 — even 1 — odd	00 — no parity 01 — reserved 10 — with parity 11 — force parity		100 — COP dual SYN 101 — COP dual SYN (BISYNC) 110 — COP single SYN 111 — asynchronous		

NOTE:
* In BISYNC protocol mode, 0 = EBCDIC, 1 = ASCII coding.

CHANNEL MODE REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Channel Connection		Data Transfer Interface			Frame Check Sequence Select		
(CMR2A, CMR2B)	00 — normal 01 — auto echo 10 — local loop 11 — reserved		000 — half-duplex single address DMA 001 — half-duplex dual address DMA 010 — full-duplex single address DMA 011 — full-duplex dual address DMA 100 — wait on Rx only 101 — wait on Tx only 110 — wait on Rx or Tx 111 — polled or interrupt			000 — none 001 — reserved 010 — LRC8 preset 0s 011 — LRC8 preset 1s 100 — CRC 16 preset 0s 101 — CRC 16 preset 1s 110 — CRC CCITT preset 0s 111 — CRC CCITT preset 1s		

SYN1/SECONDARY ADDRESS REGISTER 1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(S1RA, S1RB)	ASYNC — Character compare (5 – 8 bits) COP — SYN1 (5 – 8 bits) BOP — First address octet							

Table 2. Channel Configuration/Pin Definition Registers Bit Formats (Continued)

SYN2/SECONDARY ADDRESS REGISTER 2

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(S2RA, S2RB)	ASYNC — not used COP — SYN2 (5 – 8 bits) BOP — Second address octet							

PIN CONFIGURATION REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	X2/IDS	GPO2/RTS	SYNOUT/RTS	RTxC Pin		TRxC Pin		
(PCRA, PCRB)	* 0 — X2 1 — IDC	0 — GPO2 1 — RTS	0 — SYNOUT 1 — RTS	00 — input 01 — C/T 10 — TxCLK 1X 11 — RxCLK 1X		000 — input 001 — XTAL/2 010 — DPLL 011 — C/T	100 — TxCLK 16X 101 — RxCLK 16X 110 — TxCLK 1X 111 — RxCLK 1X	

NOTE:
* PCRA only. Not used in PCRB.

0 The TxDRQN/GPO2N/RTSN pin is a general purpose output. It is Low when OMR[2] is a 1 and High when OMR[2] is a 0.

1 The pin is a request-to-send output (see Detailed Operation). The logical state of the pin is controlled by OMR[0]. When OMR[0] is set, the output is Low.

[5] SYNOUT/RTS —

0 The SYNOUTN/RTSN pin is an active-Low output which is asserted one bit time after a SYN pattern (COP modes) in HSRH/HSRL or FLAG (BOP modes) is detected in CCSR. The output remains asserted for one receiver clock period. See Figure 1 for receiver data path.

1 The pin is a request-to-send output (see Detailed Operation). The logical state of the pin is controlled by OMR[0] when OMR[0] is set, the output is Low.

[4:3] RTxC —

00 The pin is an input. It must be programmed for input when used as the input for the receiver or transmitter clock, the DPLL, or the C/T.

01 The pin is an output for the counter/timer. Refer to CTCRA/B description.

10 The pin is an output for the transmitter shift register clock.

11 The pin is an output for the receiver shift register clock.

[2:0] TRxC —

000 The pin is an input. It must be programmed for input when used as the input for the receiver or transmitter clock, the DPLL, or the C/T.

001 The pin is an output from the crystal oscillator divided by two.

010 The pin is an output for the DPLL output clock.

011 The pin is an output for the counter/timer. Refer to CTCRA/B description.

100 The pin is an output for the transmitter BRG at 16X the rate selected by TTR [3:0].

101 The pin is an output for the receiver BRG at 16X the rate selected by RTR [3:0].

110 The pin is an output for the transmitter shift register clock.

111 The pin is an output for the receiver shift register clock.

Transmitter and Receiver Parameter and Timing Registers

This set of five registers contains the information which controls the operation of the transmitter and receiver for each channel. Table 3 shows the bit map format for each of these registers. The registers of this group are:

1. Transmitter parameter and timing registers (TPRA/B and TTRA/B)
2. Receiver parameter and timing registers (RPRA/B and RTRA/B)
3. Output and miscellaneous register (OMRA/B).

The first and second group of registers define the transmitter and receiver parameters and timing. Included in the receiver timing registers are the programming parameters for the DPLL. The last register of the group, OMR contains additional transmitter and receiver information and controls the logical state of the output pins when they are not used as a part of the channel configuration.

A channel cannot be dynamically reconfigured. Do not write to the RPR if the receiver is enabled, and do not write to the TPR if the transmitter is enabled.

Table 3. Transmitter and Receiver Parameter and Timing Register Bit Format

TRANSMITTER PARAMETER REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TPRA, TPRB)	**Underrun Control**		**Idle**	**TEOM on Zero Cnt or Done**	**Tx RTS Control**	**CTS Enable Tx**	**Tx Character Length**	
COP	00 — FCS-idle 01 — reserved 10 — MARKs 11 — SYNs		0 — MARKs 1 — SYNs	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	00 — 5 bits 01 — 6 bits 10 — 7 bits 11 — 8 bits	
	Underrun Control		**Idle**	**TEOM on Zero Cnt or Done**				
BOP	00 — FCS-FLAG-idle 01 — reserved 10 — ABORT-MARKs 11 — ABORT-FLAGs		0 — MARKs 1 — FLAGs	0 — no 1 — yes				
	Stop Bits Per Character							
ASYNC	9/16 to 1, 17/16 to 1.5, 25/16 to 2 programmable in 1/16-bit increments							

TRANSMITTER TIMING REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TTRA, TTRB)	**External Source**	**Transmitter Clock Select**			**Bit Rate Select**			
	0 — RTxC 1 — TRxC	000 — 1X external 001 — 16X external 010 — DPLL 011 — BRG 100 — 2X other channel C/T 101 — 32X other channel C/T 110 — 2X own channel C/T 111 — 32X own channel C/T			one of sixteen rates from BRG			

RECEIVER PARAMETER REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RPRA, RPRB)	not used	not used	not used	**Rx RTS Control**	**Strip Parity**	**DCD Enable Rx**	**Rx Character Length**	
ASYNC				0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	00 — 5 bits 01 — 6 bits	
COP	**SYN Strip**	**FCS to FIFO**	**Auto Hunt & Pad Chk**	**Ext Sync**	**Strip Parity**		10 — 7 bits 11 — 8 bits	
	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes			
	not used	**FCS to FIFO**	**Overrun Mode**	not used	**All Parity Address**			
BOP		0 — no 1 — yes	0 — hunt 1 — cont		0 — no 1 — yes			

Table 3. Transmitter and Receiver Parameter and Timing Register Bit Format (Continued)

RECEIVER TIMING REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RTRA, RTRB)	External Source	Receiver Clock Select			Bit Rate Select			
	0 — RTxC 1 — TRxC	000 — 1X external 001 — 16X external 010 — BRG 011 — C/T of channel 100 — DPLL, source = 64X X1/CLK 101 — DPLL, source = 32X External 110 — DPLL, source = 32X BRG 111 — DPLL, source = 32X C/T		ASYNC protocol mode only	one of sixteen rates from BRG			

OUTPUT AND MISC REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(OMRA, OMRB)	Tx Residual Character Length			TxRDY Activate	RxRDY Activate	OUT 2	OUT 1	RTS
	000 — 1 bit 001 — 2 bits 010 — 3 bits 011 — 4 bits 100 — 5 bits 101 — 6 bits 110 — 7 bits 111 — same as TPR[1:0]			0 — FIFO not full 1 — FIFO empty	0 — FIFO not empty 1 — FIFO full	Bit Pin 0 — H 1 — L	Bit Pin 0 — H 1 — L	Bit Pin 0 — H 1 — L

Transmitter Parameter Register (TPRA, TPRB)

[7:6] Underrun Control — In BOP and COP modes, this field selects the transmitter response in the event of an underrun (i.e., the TxFIFO is empty).

00 Normal end of message termination. In BOP, the transmitter sends the FCS (if selected by CMR2[2:0]) followed by a FLAG and then either MARKs or FLAGs, as specified by [5]. In COP, the transmitter sends the FCS (if selected by CMR2[2:0]) and then either MARKs or SYNs, as specified by [5].

01 Reserved.

10 In BOP, the transmitter sends an ABORT (11111111) and then places the TxD output in a marking condition until receipt of further instructions. In COP, the transmitter places the TxD output in a marking condition until receipt of further instructions.

11 In BOP, the transmitter sends an ABORT (11111111) and then sends FLAGs until receipt of further instruction. In COP, the transmitter sends SYNs until receipt of further instructions.

[5] Idle — In BOP and COP modes, this bit selects the transmitter output during idle. Idle is defined as the state following a normal end of message until receipt of the next transmitter command.

0 Idle in marking condition.

1 Idle sending SYNs (COP) or FLAGs (BOP).

[4] Transmit EOM on Zero Count or Done — In BOP and COP modes, the assertion of this bit causes the end of message (FCS in COP, FCS-FLAG in BOP) to be transmitted upon the following events:

1. If the counter/timer is counting transmitted characters, after transmission of the character which causes the counter to reach zero count. (DONEN is also asserted as an output if the channel is in a DMA operation.)
2. If the channel is operating in DMA mode, after transmission of a character if DONEN was asserted when that character was loaded into the TxFIFO by the DMA controller.

[7:4] Stop Bits per character — In ASYNC mode, this field programs the length of the stop bit appended to the transmitted character as shown in Table 4.

Table 4. Stop Bits — Transmitted Character

[7:4]	5 BITS/ CHAR	6, 7 or 8 BITS/CHAR
0000	1.063	0.563
0001	1.125	0.625
0010	1.188	0.688
0011	1.250	0.750
0100	1.313	0.813
0101	1.375	0.875
0110	1.438	0.938
0111	1.500	1.000
1000	1.563	1.563
1001	1.625	1.625
1010	1.688	1.688
1011	1.750	1.750
1100	1.813	1.813
1101	1.875	1.875
1110	1.938	1.938
1111	2.000	2.000

Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16-bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16-bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled) in all cases.

If an external 1X clock (or a 2X clock for counter/timer) is used for the transmitter, [7] = 0 selects one stop bit and [7] = 1 selects two stop bits to be transmitted. If Manchester, NRZI, or FM data encoding is selected, only integral stop bit lengths should be used.

[3] Transmitter Request-to-Send Control — This bit controls the deactivation of the RTSN output by the transmitter (see Detailed Operation).

0 RTSN is not affected by status of transmitter.

1 RTSN changes state as a function of transmitter status.

[2] Clear-to-Send Enable Transmitter — The state of this bit determines if the CTSN input controls the operation of the channel's transmitter (see Detailed Operation). The duration of CTS level change is described in the discussion of ICTSR[4].

0 CTSN has no affect on the transmitter.

1 CTSN affects the state of the transmitter.

[1:0] Transmitted Bits per Character — This field selects the number of data bits per character to be transmitted. The character length does not includes the start, parity, and stop bits in ASYNC or the parity bit in COP. In BOP modes the character length for the address and control field is always 8 bits, and the value of this field only applies to the information (I) field, except for the last character of the I field, whose length is specified by OMR[7:5].

Transmitter Timing Register (TTRA, TTRB)

[7] External Source — This bit selects the RTxC pin or the TRxC pin of the channel as the transmitter clock input when [6:4] specifies external. When used for input, the selected pin must be programmed as an input in the PCR [4:3] or [2:0].

0 External input form RTxC pin.

1 External input from TRxC pin.

[6:4] Transmitter Clock Select — This field selects the clock for the transmitter.

000 External clock from TRxC or RTXC at 1X the shift (baud) rate.

001 External clock from TRXC or RTxC at 16X the shift rate.

010 Internal clock from the phase-locked loop at 1X the bit rate. It should be used only in half-duplex operation since the DPLL will periodically resync itself to the received data if in full-duplex operation.

011 Internal clock from the bit rate generator at 32X the shift rate. The clock signal is divided by two before use in the transmitter which operates at 16X the baud rate. Rate selected by [3:0].

100 Internal clock from counter/timer of other channel. The C/T should be programmed to produce a clock at 2X the shift rate.

101 Internal clock from counter/timer of other channel. The C/T should be programmed to produce a clock at 32X the shift rate.

110 Internal clock from the counter/timer of own channel. The C/T should be programmed to produce a clock at 2X the shift rate.

111 Internal clock from the counter/timer of own channel. The C/T should be programmed to produce a clock at 32X the shift rate.

[3:0] Bit Rate Select — This field selects an output from the bit rate generator to be used by the transmitter circuits. The actual frequency output from the BRG is 32X the bit rate shown in Table 5. With a crystal or external clock of 14.7456MHz the bit rates are as given in Table 5 (this input is divided by two before being applied to the oscillator circuit).

Table 5. Receiver/Transmitter Baud Rates

[3:0]	BIT RATE	[3:0]	BIT RATE
0000	50	1000	1050
0001	75	1001	1200
0010	110	1010	2000
0011	134.5	1011	2400
0100	150	1100	4800
0101	200	1101	9600
0110	300	1110	19.2K
0111	600	1111	38.4K

Receiver Parameter Resgister (RPRA, RPRB)

[7] SYN Stripping — This bit controls the DUSCC processing in COP modes of SYN 'character patterns' that occur after the initial character synchronization. Refer to Detailed Operation of the receiver for details and definition of SYN 'patterns', and their accumulation of FCS.

0 Strip only leading SYN 'patterns' (i.e. before a message).

1 Strip all SYN 'patterns' (including all odd DLE's in BISYNC transparent mode).

[6] Transfer Received FCS to FIFO — In BISYNC and BOP modes, the assertion of this bit causes the received FCS to be loaded into the RxFIFO. When this bit is set, BOP mode operates correctly only if a minimum of two extra FLAGs (without shared zeros) are appended to the frame. If the FCS is specified to be transferred to the FIFO, the EOM status bit will be tagged onto the last byte of the FCS instead of to the last character of the message.

0 Do not transfer FCS to RxFIFO.

1 Transfer FCS to RxFIFO.

[5] Auto-Hunt and Pad Check (BISYNC) — In BISYNC mode, the assertion of this bit causes the receiver to go into hunt for character sync mode after detecting certain End-Of-Message (EOM) characters. These are defined in the Detailed Operations section for COP receiver operation. After the EOT and NAK sequences, the receiver also does a check for a closing PAD of four 1s.

0 Disable auto-hunt and PAD check.

1 Enable auto-hunt and PAD check.

[5] Overrun Mode (BOP) — The state of this control bit determines the operation of the receiver in the event of a data overrun, i.e., when a character is received while the RxFIFO and the Rx shift register are both full.

0 The receiver terminates receiving the current frame and goes into hunt phase, looking for a FLAG to be received.

1 The receiver continues receiving the current frame. The overrunning character is lost. (The five characters already assembled in the RxFIFO and Rx shift register are protected).

[4] Receiver Request-to-Send Control (ASYNC) — See Detailed Operation.

0 Receiver does not control RTSN output.

1 Receiver can negate RTSN output.

[4] External Sync (COP) — In COP single SYN mode, the assertion of this bit enables external character synchronization and receipt of SYN patterns is not required. In order to use this feature, the DUSCC must be programmed to COP single SYN mode, CMR 1[2:0] = 110, which is used to set up the internal data paths. In all other respects, however, the external sync mode operation is protocol transparent. A negative signal on the DCDN/SYNIN pin will cause the receiver to establish synchronization on the next rising edge of the receiver clock. Character assembly will start at this edge with the RxD input pin considered to have the second bit of data. The sync signal can then be negated. Receipt of the Active-High external sync input causes the SYN detect status bit (RSR[2]) to be set and the SYNBOUTN pin to be asserted for one bit time. When this mode is enable, the internal SYN (COP mode) detection and special character recognition (e.g., IDLE, STX, ETX, etc.) circuits are disabled. Character assembly begins as if in the I-field with character length as programmed in RPR[1:)]. Incoming COP frames with parity specified optionally can have it stripped by programming RPR[3]. The user must wait at least eight bit times after Rx is enabled before applying the SYNIN signal. This time is required to flush the internal data paths. The receiver remains in this mode and further external sync pulses are ignored until the receiver is disabled and then reenabled to resynchronize or to return to normal mode. See Figure 2.

0 External sync not enabled.

1 External sync enabled.

Note that EXT SYNC and DCD ENABLE Rx cannot be asserted simultaneously since they use the same pin.

[3] Strip Parity — In COP and ASYNC modes with parity enabled, this bit controls whether the received parity bit is stripped from the data placed in the receiver FIFO. It is valid ony for programmed character lengths of 5, 6, and 7 bits. If the bit is stripped, the corresponding bit in the received data is set to zero.

0 Transfer parity bit as received.

1 Stop parity bit from data.

[3] All Parties Address — In BOP secondary modes, the assertion of this bit causes the receiver to 'wake-up' upon receipt of the address H'FF' or H'FF, FF', for single- and dual-octet address modes, respectively, in addition to its normal station address. This feature allows all stations to receive a message.

0 Don't recognize all parties address.

1 Recognize all parties address.

[2] DCD Enable Receiver — If this bit is asserted, the DCDN/SYNIN input must be Low in order for the receiver to operate. If the input is negated (goes High) while a character is being received, the receiver terminates receipt of the current message (this action in effect disables the receiver). If DCD is subsequently asserted, the receiver will search for the start bit, SYN pattern, or FLAG, depending on the channel protocol. (Note that the change of input can be programmed to generate an interrupt; the duration of the DCD level change is described in the discussion of the input and counter/timer status register (CTSR[5]).

0 DCD not used to enabled receiver.

1 DCD used to enabled receiver.

EXT SYNC and DCD ENABLE Rx cannot be asserted simultaneously since they use the same pin.

[1:0] Received Bits per Character — This field selects the number of data bits per character to be assembled by the receiver. The character length does not include the start, parity, and stop bits in the ASYNC or the parity bit in COP. In BOP modes, the character length for the address and control field is always 8 bits, and the value of this field only applies to the information field. If the number of bits assembled for the last character of the I-field is less than the value programmed in this field, RCL not zero (RSR[0]) is asserted and the actual number of bits received is given in TRSR[2:0].

Receiver Timing Register (RTRA, RTRB)

[7] External Source — This bit selects the RTxC pin or the TRxC pin of the channel as the receiver or DPLL clock input, when [6:4] specifies external. When used for input, the selected pin must be programmed as an input in the PCR [4:3] or [2:0].

0 External input form RTxC pin.

1 External input form TRxC pin.

[6:4] Receiver Clock Select — This field selects the clock for the receiver.

000 External clock from TRxC or RTxC at 1X the shift (baud) rate.

001 External clock fromTRxC or RTxC at 16X the shift rate. Used for ASYNC mode only.

010 Internal clock from the bit rate generator at 32X the shift rate. Clock is divided by two before used by the receiver logic, which operates at 16X the baud rate. Rate selected by [3:0]. Used for ASYNC mode only.

011 Internal clock from counter/timer of own channel. The C/T should be programmed to produce a clock at 32X the shift rate. Clock is divided by two before use in the receiver logic. Used for ASYNC mode only.

100 Internal clock from the digital phase-locked loop. The clock for the DPLL is a 64X clock from the crystal oscillator or system clock input. (The input to the oscillator is divided by two).

101 Internal clock from the digital phase-locked loop. The clock for the DPLL is an external 32X clock from the RTxC or TRxC pin, as selected by [7].

110 Internal clock from the digital phase-locked loop. The clock for the DPLL is a 32X clock from the BRG. The frequency is programmed by [3:0].

111 Internal clock from the digital phase-locked loop. The clock for the DPLL is a 32X clock from the counter/timer of the channel.

[3:0] Bit Rate Select — This field selects an output from the bit rate generator to be used by the receiver circuits. The actual frequency output from the BRG is 32X the bit rate shown in Table 5.

Output and Miscellaneous Register (OMRA, OMRB)

[7:5] Transmitted Residual Character Length — In BOP modes, this field determines the number of bits transmitted for the last character in the information field. This length applies to:

- The character in the transmit FIFO accompanied by the FIFOed TEOM command.
- The character loaded into the FIFO by the DMA controller if DONEN is simultaneously asserted and TPR[4] is asserted.
- The character loaded into the FIFO which causes the counter to reach zero count when TPR[4] is asserted.

The length of all other characters in the frame's information field is selected by TPR[1:0]. If this field is 111, the number of bits in the last character is the same as programmed in TPR[1:0].

[4] TxRDY Activate Mode —

0 FIFO not full. The channel's TxRDY status bit is asserted each time a character is transferred from the transmit FIFO to the transmit shift register. If not reset by the CPU, TxRDY remains asserted until the FIFO is full, at which time it is automatically negated.

1 FIFO empty. The channel's TxRDY status bit is asserted when a character transfer from the transmit FIFO to the transmit shift register causes the FIFO to become empty. If not reset by the CPU, TxRDY remains asserted until the FIFO is full, at which time it is negated.

If the TxRDY status bit is reset by the CPU, it will remain negated regardless of the current state of the transmit FIFO, until it is asserted again due to the occurrence of one of the above conditions.

[3] RxRDY Activate Mode —

0 FIFO not empty. The channel's RxRDY status bit is asserted each time a character is transferred from the receive shift register to the receive FIFO. If not reset by the CPU, RxRDY remains asserted until the receive FIFO is empty, at which time it is automatically negated.

1 FIFO full. The channel's RxRDY status bit is asserted when a character transfer from the receive shift register to the receive FIFO causes the FIFO to become full. If not reset by the CPU, RxRDY reamins asserted until the FIFO is empty, at which time it is negated.

The RxRDY status bit will also be asserted, regardless of the receiver FIFO full condition, when an end-of-message character is loaded in the RxFIFO (BOP/BISYNC), when a BREAK condition (ASYNC mode) is detected in RSR[2], or when the counter/timer is programmed to count received characters and the character which causes it to reach zero is loaded in the FIFO (all modes). (Refer to the Detailed Operation of the receiver.)

If reset by the CPU, the RxRDY status bit will remain negated, regardless of the current state of the receiver FIFO, until it is asserted again due to one of the above conditions.

[2] General Purpose Output 2 — This general purpose bit is used to control the TxDRQN/GPO2/RTSN pin, when it is used as an output. The output is High when the bit is a 0 and is Low when the bit is a 1.

[1] General Purpose Output 1 — This bit is used to control the RTxDRQN/GPO1N output, which is a general purpose output when the channel is not in DMA mode. The output is High when the bit is a 0 and is Low when the bit is a 1.

[0] Request-to-Send Output — This bit controls the TxDRQN/GPO2N/RTSN and SYNOUTN/RTSN pin, when either is used as a RTS output. The output is High when the bit is a 0 and is Low when the bit is a 1.

Counter/Timer Control and Value Registers

There are five registers in this set consisting of the following:

1. Counter/timer control register (CTCRA/B).
2. Counter/timer preset Highland Low registers (CTPRHA/B, CTPRLA/B).
3. Counter/timer (current value) High and Low registers (CTHA/B, CTLA/B)

The format of each of the registers of this set is contained in Table 6. The control register contains the operational information for the counter/timer. The preset registers contain the count which is loaded into the counter/timer circuits. The third group contains the current value of the counter/timer as it operates.

Counter/Timer Control Register (CTCRA/CTCRB)

[7] Zero Detect Interrupt — This bit determines whether the assertion of the C/T ZERO COUNT status bit (ICTSR[6]) causes an interrupt to be generated.

0 Interrupt disabled.

1 Interrupt enabled if master interrupt enabled (ICR[1] or ICR[0]) is asserted.

[6] Zero Detect Control — This bit determines the action of the counter upon reaching zero count.

0 The counter/timer is preset to the value contained in the counter/timer preset registers (CTPRL, CTPRH) at the next clock edge.

1 The counter/timer continues counting without preset. The value at the next clock edge will be H'FFFF'.

[5] Counter/Timer Output Control — This bit selects the output waveform when the counter/timer is selected to be output on TRxC or RTxC.

1 The output is a single clock positive width pulse each time the C/T reaches zero count. (The duration of this pulse is one clock period.)

0 The output toggles each time the C/T reaches zero count. The output is cleared to Low by either of the preset counter/timer commands.

[4:3] Clock Select — This field selects whether the clock selected by [2:0] is prescaled prior to being applied to the input of the C/T.

00 No prescaling.

01 Divide clock by 16.

10 Divide clock by 32.

11 Divide clock by 64.

[2:0] Clock Source — This field selects the clock source for the counter/timer.

000 RTxC pin. Pin must be programmed as input.

001 TRxC pin. Pin must be programmed as input.

010 Source is the crystal oscillator or system clock input divided by four.

011 This selects a special mode of operation. In this mode the counter, after receiving the 'start C/T' command, delays the start of counting until the RxD input goes Low. It continues counting until the RxD input goes High, then stops and sets the C/T zero count status bit. The CPU can use the value in the C/T to determine the bit rate of the incoming data. The clock is the crystal oscillator or system clock input divided by four.

100 Source is the 32X BRG output selected by RTR[3:0] of own channel.

101 Source is the 32X BRG output selected by TTR[3:0] of own channel.

110 Source is the internal signal which loads received characters from the receive shift register into the receiver FIFO. When operating in this mode, the FIFOed EOM status bit (RSR[7]) shall be set when the character which causes the count to go to zero is loaded into the receive FIFO.

111 Source is the internal signal which transfers characters from the data bus into the transmit FIFO. When operating in this mode, and if the TEOM on zero count or done control bit (TPR[4]) is asserted, the FIFOed send EOM command will be automatically asserted when the character which causes the count to go to zero is loaded into the transmit FIFO.

Table 6. Counter/Timer Control and Value Register Bit Formats

COUNTER/TIMER CONTROL REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTCRA, CTCRB)	Zero Detect Interrupt	Zero Detect Control	Output Control	Prescaler		Clock Source		
	0 — disable 1 — enabled	0 — preset 1 — continue	0 — square 1 — pulse	00 — 1 01 — 16 10 — 32 11 — 64		000 — RTxC pin 001 — TRxC pin 010 — X1/CLK divided by 4 011 — X1/CLK divided by 4 gated by RxD 100 — Rx BRG 101 — Tx BRG 110 — Rx characters 111 — Tx characters		

COUNTER/TIMER PRESET REGISTER HIGH

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTPRHA, CTPRHB)	Most significant bits of counter/timer preset value.							

COUNTER/TIMER PRESET REGISTER LOW

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTPRLA, CTPRLB)	Least significant bits of counter/timer preset value.							

COUNTER/TIMER REGISTER HIGH

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTHA, CTHB)	Most significant bits of counter/timer.							

COUNTER/TIMER REGISTER LOW

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTLA, CTLB)	Least significant bits of counter/timer.							

Counter/Timer Preset High Register (CTPRHA, CTPRHB)

[7:0] MSB — This regsiter contains the eight most significant bits of the value loaded into the counter/timer upon receipt of the load C/T from preset regsiter command or when the counter/timer reaches zero count and the zero detect control bit (CTCR[6]) is negated. The minimum 16-bit counter/timer preset value is H'0002'.

Counter/Timer Preset Low Register (CTPRLA, CTPRLB)

[7:0] LSB — This register contains the eight least significant bits of the value loaded into the counter/timer upon receipt of the load C/T from preset register command or when the counter/timer reaches zero count and the zero detect control bit (CTCR[6]) is negated. The minimum 16-bit counter/timer preset value is H'0002'.

Counter/Timer High Register (CTHA, CTHB)

[7:0] MSB — A read of this 'register' provides the eight most significant bits of the current value of the counter/timer. It is recommended that the C/T be stopped via a stop counter command before it is read in order to prevent errors which may occur due to the read being performed while the C/T is changing. This count may be continued after the register is read.

Counter/Timer Low Register (CTLA, CTLB)

[7:0] LSB — A read of this 'register' provides the eight least significant bits of the current value of the counter/timer. It is recommended that the C/T be stopped via a stop counter command before it is read, in order to prevent errors which may occur due to the read being performed while the C/T is changing. This count may be continued after the register is read.

Interrupt Control and Status Registers

This group of registers define mechanisms for communications between the DUSCC and the processor and contain the device status information. Four registers, available for each channel, and four common device registers comprise this group which consists of the following:

1. Interrupt Enable Register (IERA/B).
2. Receiver Status Register (RSRA/B).
3. Transmitter and Receiver Status Register (TRSRA/B).
4. Input and Coutner/Timer Status Register (ICTSRA/B).
5. Interrupt Vector Register (IVR) and Modified Interrupt Vector Register (IVRM).
6. Interrupt control register (ICR).
7. General status register (GSR)

See Table 7 for bit formats and Figure 3 for table relationships.

Interrupt Enable Register (IERA, IERB)

This register controls whether the assertion of bits in the channel's status registers causes an interrupt to be generated. An additional condition for an interrupt to be generated is that the channel's master interrupt enabled bit, ICR[0] or ICR[1], be asserted.

[7] DCD/CTS —

0 Interrupt not enabled.

1 Interrupt generated if ICTSR[4] or ICTSR[5] are asserted.

[6] TxRDY —

0 Interrupt not enabled.

1 Interrupt generated if TxRDY (GSR[1] or GSR[5] for Channels A and B, respectively) is asserted.

[5] TRSR 73 —

0 Interrupt not enabled.

1 Interrupt generated if bits 7, 6, 5, 4 or 3 of the TRSR are asserted.

[4] RxRDY —

0 Interrupt not enabled.

1 Interrupt generated if RxRDY (GSR[0] or GSR[4] for Channels A and B, respectively) is asserted.

[3] RSR 76 —

0 Interrupt not enabled.

1 Interrupt generated if bits 7 or 6 of the RSR are asserted.

[2] RSR 54 —

0 Interrupt not enabled.

1 Interrupt generated if bits 5 or 4 of the RSR are asserted.

[1] RSR 32 —

0 Interrupt not enabled.

1 Interrupt generated if bits 3 or 2 of the RSR are asserted.

Table 7. Interrupt Control and Status Register Bit Format

RECEIVER STATUS REGISTER

	*BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RSRA, RSRB) ASYNC	# Char compare	RTS negated	Overrun error	not used	BRK end detect	BRK start detect	# Framing error	# Parity error
COP	# EOM detect +	PAD error +	Overrun error	not used	not used	Syn detect	# CRC error	# Parity error
BOP	# EOM detect	Abort detect	Overrun error	Short frame detect	Idle detect	Flag detect	# CRC error	# RCL not zero
LOOP	# EOM detect	Abort/EOP detect	Overrun error	Short frame detect	Turn-around detect	Flag detect	# CRC error	# RCL not zero

NOTES:
Status bit is FIFOed.
+ COP BISYNC mode only
* All modes indicate character count complete.

TRANSMITTER AND RECEIVER STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TRSRA, TRSRB) ASYNC	Transmitter empty	CTS underrun	not used	Send break ack	DPLL error	not used	not used	not used
COP	Transmitter empty	CTS underrun	Frame complete	Send SOM ack	DPLL error	not used	Rx hunt mode	Rx xpnt mode
BOP	Transmitter empty	CTS underrun / Loop sending*	Frame complete	Send SOM/ abort ack	DPLL error	**Rx Residual Character Length**: 000 — 0 bit, 001 — 1 bits, 010 — 2 bits, 011 — 3 bits, 100 — 4 bits, 101 — 5 bits, 110 — 6 bits, 111 — 7 bits		

NOTE:
* Loop mode only.

Table 7. Interrupt Control and Status Register Bit Format (Continued)

INPUT AND COUNTER/TIMER STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(ICTSRA, ICTSRB)	C/T running	C/T zero count	Delta DCD	Delta CTS/LC	DCD	CTS/LC	GPI2	GPI1

INTERRUPT ENABLE REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(IERA, IERB)	DCD/CTS	TxRDY	TRSR [7:3]	RxRDY	RSR[7:6]	RSR [5:4]	RSR [3:2]	RSR [1:0]
	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes

INTERRUPT VECTOR REGISTER AND INTERRUPT VECTOR MODIFIED REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(IVR, IVRM)	8-bit interrupt vector							

GENERAL STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(GSR)	Channel B				Channel A			
	External or C/T Status	Rx/Tx status	TxRDY	RxRDY	External or C/T status	Rx/Tx status	TxRDY	RxRDY

INTERRUPT CONTROL REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(ICR)	Channel A/B Interrupt Priority		Vector Mode		Bits to Modify	Vector Includes Status	Channel A Master Int Enable	Channel B Master Int Enable
	00 — Channel A 01 — Channel B 10 — interleaved A 11 — interleaved B		00 — vectored 01 — vectored 10 — vectored 11 — non vectored		0 — 2:0 1 — 4:2	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes

[0] RSR 10 —

0 Interrupt not enabled.

1 Interrupt generated if bits 1 or 0 of the RSR are asserted.

Receiver Status Register (RSRA, RSRB)

This register informs the CPU of receiver status. Bits indicated as 'not used' in a particular mode will read as zero. The logical OR of these bits is presented in GSR[2] or GSR[6] (ORed with the bits of TRSR) for Channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only be performing a write operation to the status register with the bits to be reset being ones in the accompanying data word, or when the RESETN input is asserted, or when a 'reset receiver' command is issued.

Certain status bits are specified as being FIFOed. This means that they occupy positions in a status FIFO that correspond to the data FIFO. As the data is brought to the top of the FIFO (the position read when the RxFIFO is read), the FIFOed status bits are logically ORed with the previous contents of the corresponding bits in the status register. This permits the user to obtain status either character by character or on a block basis. For character by character status, the SR bits should be read and then cleared before reading the character data from RxFIFO. For block status, the status register is initially cleared and then read after the message is received. Asserted status bits can be programmed to generate an interrupt (see Interrupt Enable Register).

[7] Character Count Complete (All Modes), Character compare (ASYNC), EOM (BISYNC/BOP/LOOP) — If the counter/timer is programmed to count received characters, this bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. It is also asserted to indicate the following conditions:

ASYNC The character currently at the top of RxFIFO matched the contents of S1R. A character will not compare if it is received with parity error even if the data portion matches.

BISYNC The character currently at the top of the FIFO was either a text message terminator or a control sequence received outside of a text or header field. See Detailed Operation of COP Receiver. If transfer FCS to FIFO (RPR[6]) is set, the EOM will instead be tagged onto the last byte of the FCS. Note that if an overrun occurs during receipt of a message, the EOM character may be lost, but this status bit will still be asserted to indicate that an EOM was received. For 2 byte EOM comparisons, only the second byte is tagged (assuming the CRC is not transferred to the FIFO).

BOP, LOOP The character currently at the top of the FIFO was the last character of the frame. If trnasfer FCS to FIFO (RPR[6]) is asserted, the EOM will be tagged instead onto the last byte of the FCS. Note that if an overrun occurs, the EOM character may be lost, but this status bit will still be asserted to indicate that an EOM was received. This bit will not be set when an abort is received.

[6] RTS Negated (ASYNC), PAD Error (BISYNC), ABORT (BOP) —

ASYNC The RTSN output was negated due to receiving the start bit of a new character while the RxFIFO was full (see RPR[4]).

BISYNC PAD error detected (see RPR[5]).

LOOP An ABORT sequence consisting of a zero followed by seven ones was received after receipt of the first address octet but before receipt of the closing FLAG. The user should read RxFIFO until it is empty and determine if any valid characters from a previous frame are in the FIFO. If no character with a tagged EOM detect ([7]) is found, all characters are from the current frame and should be discarded along with any previously read by the CPU. An ABORT detect causes the receiver to automatically go into search for FLAG state. An abort during a valid frame does not cause the CRC to reset; this will occur when the next frame begins.

LOOP Performs the ABORT detect function as described for BOP without the restriction that the pattern be detected during an active frame. A zero followed by seven ones is the end-of-poll sequence which allows the transmitter to go active if the 'go active on poll' command has been invoked.

[5] Overrun Error (All Modes) — A new character was received while the receive FIFO was full and a character was already waiting in the receive shift register to be transferred to the FIFO. the DUSCC protects the five characters previously assembled (four in RxFIFO, one in the Rx shift register) and discards the overrunning character(s). After the CPU reads the FIFO, the character waiting in the RxSR will be loaded into the available FIFO position. This releases the RxSR and a new character assembly will start at the next character boundary. In this way, only valid characters will be assembled, i.e., no partial character assembly will occur regardless of when the RxSR became available during the incoming data stream.

[4] Short Frame (BOP/LOOP) —

ASYNC Not used

COP Not used

BOP, LOOP A closing flag was received with missing fields in the frame. See detailed operation for BOP receiver.

[3] BREAK End Detect (ASYNC), IDLE (BOP), Turnaround (LOOP) —

ASYNC 1X clock mode: The RxD input has returned to the marking state for at least one period of the 1X receiver clock after detecting a BREAK.

16X clock mode: The RxD input has returned to the marking (High) state for a least one-half bit time after detecting a BREAK. A half-bit time is defined as eight clock cycles of the 16X receiver clock.

COP Not used.

BOP An IDLE sequence consisting of a zero followed by fifteen ones was received. During a valid frame, an abort must precede an idle. However, outside of a valid frame, an idle is recognized and abort is not.

LOOP A turnaround sequence consisting of eight contiguous zeros was detected outside of an active frame. This should normally be used to terminate transmitter operation and return the system to the 'echoing RxD' mode.

[2] BREAK Start Detect (ASYNC), SYN Detect (COP), FLAG Detect (BOP/LOOP) —

ASYNC An all zero character, including parity (if specified) and first stop bit, was received. The receiver shall be capable of detecting breaks which begin in the middle of a previous character. Only a single all-zero character shall be put into the FIFO when a break is detected. Additional entries to the FIFO are inhibited until the end of break has been detected (see above) and a new character is received.

COP A SYN pattern was received. Refer to Detailed Operation for definition of SYN patterns. Set one bit time after detection of SYN pattern in HSRH, HSRL. See Figure 1 for receiver data path.

BOP, LOOP A FLAG frequency (01111110) was received. Set one bit time after FLAG is detected in CCSR. See Figure 1 for receiver data path.

[1] Framing Error (ASYNC), CRC Error (COP/BOP/LOOP) —

ASYNC At the first stop bit position the RxD input was in the Low (space) state. The receiver only checks for framing error at the nominal center of the first stop bit regardless of the number of stop bits programmed in TPR[7:4]. This bit is not set for BREAKS.

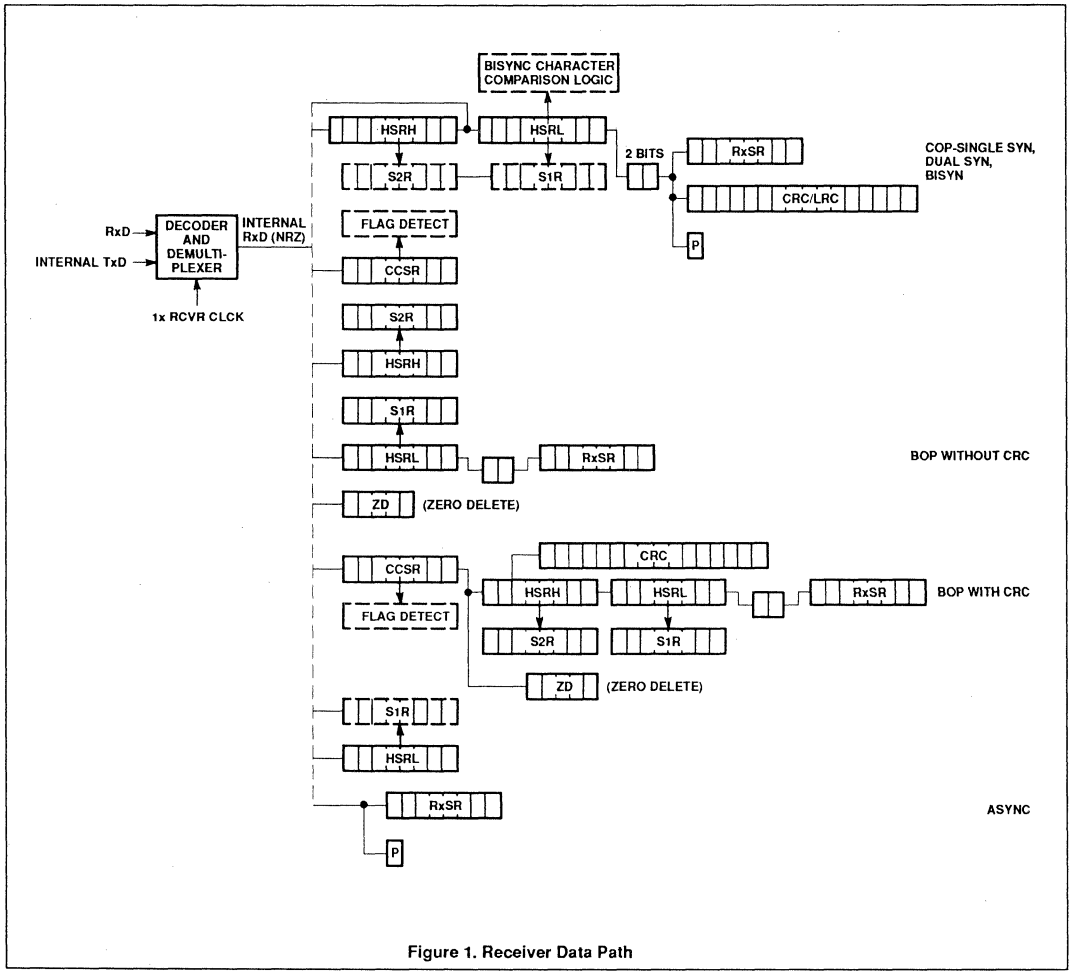


Figure 1. Receiver Data Path

COP In BISYNC COP mode, this bit is set upon receipt of the BCC byte(s), if any, to indicate that the received BCC was in error. The bit is normally FIFOed with the last byte of the frame (the character preceding the first BCC byte). However, if transfer FCS to FIFO (RPR[6]) is asserted, this bit is FIFOed with the last BCC byte. The value of this bit should be ignored for non-test messages or if the received frame was aborted via an ENQ. In non-BISYNC COP modes, the bit is set with each received character if the current value of the CRC checker is not equal to the non-error value (see CMR2[2:0]).

BOP, LOOP This bit is set upon receipt of the FCS byte(s), if any, to indicate that the received FCS was in error. The bit is normally FIFOed with the last byte of the I field (the character preceding the first FCS byte). However, if transfer FCS to FIFO (RPR[6]) is asserted, this bit is FIFOed with the last FCS byte.

[0] Parity Error (ASYNC/COP), RCL Not Zero (BOP/LOOP) —

ASYNC The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated.

COP The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated. A SYN or other character received with parity error is treated as a data character. Thus, a SYN with parity error received while in SYN search state will not establish character sync. Characters received with parity error while in the SYN search state will not set the error bit.

BOP, LOOP — The last character of the I field did not have the character length specified in RPR[1:0]. The actual received character length of this byte can be read in TRSR[2:0]. This bit is FIFOed with the EOM character but TRSR[2:0] is not. An exception occurs if the command to transfer the FCS to the FIFO is active. In this case, the bit will be FIFOed with the last byte of the FCS, i.e., with REOM. In the event that residual characters from two consecutive frames are received and are both in the FIFO, the length in TRSR[2:0] applies to the last received residual character.

Transmitter/Receiver Status Register (TRSRA, TRSRB)

This register informs the CPU of transmitter and receiver status. Bits indicated as not used in a paritcular mode will read as zero, except for bits [2:0], which may not be zero. The logical-OR of bits [7:3] is presented in GSR[2] or GSR[6] (ORed with the bits of RSR) for channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only:

1. By performing a write operation to the status register with the bits to be reset being ones in the accompanying data word [7:3].
2. When the RESETN input is asserted.
3. For [7:4], when a 'reset transmitter' command is issued.
4. For [3:0], when a 'reset receiver' command is issued.
5. For [2:0], see description in BOP mode.

Asserted status bits in [7:3] can be programmed to generate an interrupt. See IER.

[7] Transmitter Empty — Indicates that the transmit shift register has completed serializing a character and found no other character to serialize in the TxFIFO. The bit is not set until at least one character from the transmit FIFO (not including PAD characters in synchronous modes) has been serialized. The transmitter action after transmitter empty depends on operating mode:

ASYNC — The TxD output is held in the MARK state until another character is loaded into the TxFIFO. Normal operation then continues.

COP — Action is specified by TPR[7:6].

BOP, LOOP — Action is specified by TPR[7:6].

[6] CTS Underrun (ASYNC/COP/BOP), Loop sending (LOOP) —

ASYNC, COP, BOP — This bit is set only if CTS enable Tx (TPR[2]) is asserted. It indicates that the transmit shift register was ready to begin serializing a character and found the CTSN input negated. In ASYNC mode, this bit will be reasserted if cleared by the CPU while the CTSN input is negated.

LOOP — Asserted when the go active on poll command has been invoked and an EOP sequence has been invoked and an EOP sequence has been detected, causing the transmitter to go active by changing the EOP to a FLAG (see Detailed Operation of transmitter).

[5] Frame Complete (COP/BOP) —

ASYNC — Not used.

COP — Asserted at the beginning of transmission of the end of message sequence invoked by which is either a TEOM command, or when TPR[4] = 1, or TPR[7:6] = 00. The CPU can invoke the TSOM command after this bit is set to control the number of SYNs between transmitted frames.

BOP — Asserted at the beginning of transmission of the end of message sequence which is invoked by either a TEOM command, or when TPR[4] = 1, or TPR[7:6] = 00. The CPU can invoke the TSOM command after this bit is set to control the number of FLAGs between transmitted frames.
In COP/BOP modes, the frame complete status bit is set during the next-to-last bit (on TxD pin) of the last character in the data/information field. In BOP mode, if a 1-bit residual character is selected through OMR[7:5], then this bit is set during the next-to-last bit (on TxD pin) of the last full length character of the information field.

[4] Send Break Ack (ASYNC)/Send SOM ACK (COP)/Send SOM-Abort Ack (BOP —

ASYNC — Set when the transmitter begins transmission of a break in response to the send break command. If the command is reinvoked, the bit will be set again at the beginning of the next character time. The user can control the length of the break by counting character times through this mechanism.

COP — Set when the transmitter begins transmission of a SYN pattern in response to the TSOM or TSOMP command. If the command is reinvoked, the bit will be set again at the beginning of the next transmitted SYN pattern. The user can control the number of SYNs which are sent through this mechanism.

BOP — Set when the transmitter begins transmission of a FLAG/ABORT in response to the TSOM or TSOMP or TABRK command. If the command is reinvoked, the bit will be set again at the beginning of the next transmitted FLAG/ABORT. The user can control the number of FLAGs/ABORTs which are sent through this mechanism.

[3] DPLL Error — Set while the DPLL is operating in FM mode to indicate that a data transition was not detected within the detection window for two consecutive bits and that the DPLL was forced into search mode. This feature is disabled when the DPLL is specified as the clock source for the transmitter via TTR[6:4].

[2:0] Received Residual Character Length (BOP) —

BOP — This field should be examined to determine the length of the last character of the I field (character tagged with REOM status bit) if RSR[0] is set to indicate that the length was not equal to the character length specified in RPR[1:0]. This field is negated when a reset receiver or disabled receiver command is issued, or when the first control character for the next frame of data is in HSRL (see Figure 1). Care must be taken to read TRSR[2:0] before these bits are cleared.

[1] Receiver in Hunt Mode (COP) —

COP — This bit is asserted after the receiver is reset or disabled. It indicates that the receiver is in the hunt mode, searching the data stream for a SYN sequence to establish character synchronization. The bit is negated automatically when character sync is achieved.

[0] Receiver in Transparent Mode (BISYNC) —

COP — Indicates that a DLE-STX sequence was received and the receiver is operating in BISYNC transparent mode. Set two bit times after detection of STX in HSRL. See Figure 1 for receiver data path. Transparent mode

operation is terminated and the bit is negated automatically when one of the terminators for transparent text mode is received (DLE-ETX/ETB/ITB/ENQ).

Input and Counter/Timer Status Register (ICTSRA, ICTSRB)

This register informs the CPU of status of the counter/timer and inputs. The logical-OR of bits [6:4] is presented in GSR[3] or GSR[7] for Channels A and B, respectively. Unless otherwise specified, bits of this register are reset only:

1. By performing a write operation to the status register with the bits to be reset (ones in the accompanying data word for bits [6:4] only).
2. When the RESETN input is asserted (bits [7:4]) only.

[7] Counter/Timing Running — Set when the C/T is started by start C/T command and reset when it is stopped by a stop C/T command.

[6] Counter/Timer Zero Detect — Set when the counter/timer reaches zero count, or when the bit length measurement is enabled (CTCR [2:0] = 011) and the RxD input has returned High. The assertion of this bit causes an interrupt to be generated if ICTCR[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

[5] Delta DCD — The DCD input is sampled approximately every 6.8µs using the 32X, 4800 baud output from the BRG. After synchronizing with the sampling clock, at least two consecutive samples at the same level are required to establish the level. As a consequence, a change of state at the DCD input, lasting at least 17µs, will set this bit. The reset circuitry initializes the sampling circuits so that a change is not falsely indicated at power on time. The assertion of this bit causes an interrupt to be generated if IER[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

[4] Delta CTS/LC — When not in loop mode, the CTS input is sampled approximately every 6.8µs using the 32X, 4800 baud output form the BRG. After synchronizing with the sampling clock, at least two consecutive samples at the same level are required to establish the level. As a consequence, a change of state at the CTS input, lasting at least 17µs, will set this bit. The reset circuitry initializes the sampling circuits so that a change is not falsely indicated at power on time. The assertion of this bit causes an interrupt to be generated if IER[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

In SDLC loop mode, this bit is set upon transitions of the LC output. LC is asserted in response to the 'go on-loop' command when the receiver detects a zero followed by seven ones, and negated in response to the 'go off-loop' command when the receiver detects a sequence of eight ones.

[3:2] State of DCD and CTS — ICTSRx[3] reflects the state of the DCDxN input pin, while ICTSRx[2] reflects the state of CTSxN. When the bits are 0, the inputs are High, when they are 1, the pins are Low.

[1:0] Current State of GPI2 and GPI1 — These fields provide the current state of the channels general purpose input pins. The bits valve are latched at the beginning of the read cycle.

Interrupt Vector Register (IVR) and Modified Vector Register (IVRM)

[7:0] Register Content — If ICR[2] = 0, the content of IVR register is output on the data bus when the DUSCC has issued an interrupt request and the responding interrupt acknowledge (IACKN) is received. The value in the IVR is initialized to H'0F' on master reset. If 'vector includes status' is specified by ICR[2] = 1, bit [2:0] or [4:2] (depending on ICR[3]), of the vector are modified as shown in Table 9 to indicate the highest priority interrupt currently active. The priority is programmable through the ICR. This modified vector is stored in the IVRM. When ICR[2] = 1, the content of the IVRM is output on to the data bus on the interrupt acknowledge. The vector is not modified, regardless of the value of ICR[2], if the CPU has not written an initial vector into this register.

Either the modified or unmodified vector can also be read by the CPU via a normal bus read cycle (see Table 1). The vector value is locked at the beginning of the IACK or read cycle until the cycle is completed. If no interrupt is pending, an H'FF' is output when reading the IVRM or the IVR.

Interrupt Control Register (ICR)

[7:6] Channel A/B Interrupt Priority — Selects the relative priority between Channels A and B. The state of this bit determines the value of the interrupt vector (see Interrupt Vector Register). The priority within each channel, from highest to lowest, is as follows:

0 Receiver ready.

1 Transmitter ready

2 Rx/Tx status.

3 External or C/T status.

00 Channel A has the highest priority. The DUSCC interrupt priorities from highest to lowest are as follows: A(0), A(1), A(2), A(3), B(0), B(1), B(2), B(3).

01 Channel B has the highest priority. the DUSCC interrupt priorities from highest to lowest are as follows: B(0), B(1), B(2), B(3), A(0), A(1), A(2), A(3).

10 Priorities are interleaved between channels, but Channel A has the highest priority between events of equal channel priority. The DUSCC interrupt priorities from highest to lowest are as follows: A(0), B(0), A(1), B(1), A(2), B(2), A(3), B(3)

11 Priorities are interleaved between channels, but Channel B has the highest priority between events of equal channel priority. The DUSCC interrupt priorities from highest to lowest are as follows: B(0), A(0), B(1), A(1), B(2), A(2), B(3), A(3).

Table 8. Interrupt Status Encoding

IVRM [2:0]/ [4:2]	HIGHEST PRIORITY INTERRUPT CONDITION
000	Channel A receiver ready
001	Channel A transmitter ready
010	Channel A Rx/Tx status
011	Channel A external or C/T status
100	Channel B receiver ready
101	Channel B transmitter ready
110	Channel B Rx/Tx status
111	Channel B external or C/T status

[5:4] Vector Mode — The value of this field determines the response of the DUSCC when the interrupt acknowledge (IACKN) is received from the CPU.

00 or 01 or 10 Vectored mode. Upon interrupt acknowledge, the DUSCC locks its current interrupt status until the end of the acknowledge cycle. If it has an active interrupt pending, it responds with the appropriate vector and then asserts DTACKN. If it does not have

an interrupt, it propagates the acknowledge through its X2/IDCN output if this function is programmed in PCRA[7]. Otherwise, the IACKN is ignored. Locking the interrupt status at the leading edge of IACKN prevents a device at High position in the interrupt daisy chain from responding to an IACK issued for a lower priority device while the acknowledge is being propagated to that device.

11 Non-vectored mode. The DUSCC ignores an IACK if one is received; the interrupt vector is not placed on the data bus. The internal interrupt status is locked when a read of the IVR or IVRM is performed. Except for the absence of the vector on the bus, the DUSCC performs as it does in vectored mode — the vector is prioritized and modified if programmed.

[3] Vector Bits to Modify — Selects which bits of the vector stored in the IVR are to be modified to indicate the highest priority interrupt pending in the DUSCC. See Interrupt Vector Register.

0 Modify bits 2:0 of the vector.

1 Modify bits 4:2 of the vector.

[2] Vector Includes Status — Selects whether the modified (includes status) (IVRM) or unmodified vector (IVR) is output in response to an interrupt acknowledge (see Interrupt Vector Register).

0 Unmodified vector.

1 Modified vector.

[1] Channel A Master Interrupt Enable —

0 Channel A interrupts are disabled.

1 Channel A interrupts are enabled.

[0] Channel B Master Interrupt Enable —

0 Channel B interrupts are disabled.

1 Channel B interrupts are enabled.

General Status Register (GSR)

This register provides a 'quick look' at the overall status of both channels of the DUSCC. A write to this register with 1s at the corresponding bit positions causes TxRDY (bits 5 and 1) and/or RxRDY (bits 4 and 0) to be reset. The other status bits can be reset only by resetting the individual status bits that they point to.

[7] Channel B External or Coutner/Timer Status — This bit indicates that one of the following status bits is asserted: ICTSRB[6:4].

[6] Channel B Receiver or Transmitter Status — This bit indicates that one of the following status bits is asserted: RSRB[7:)], TRSRB[7:3].

[5] Channel B Transmitter Ready — The assertion of this bit indicates that one or more characters may be loaded into the Channel B transmitter FIFO to be serialized by the transmit shift register. See description of OMR[4]. This bit can be asserted only when the transmitter is enabled. Disabling or resetting the transmitter negates TxRDY.

[4] Channel B Receiver Ready — The assertion of this bit indicates that one or more characters are available in the Channel B receiver FIFO to be read by the CPU. See description of OMR[3]. RxRDY is initially reset (negated) by a chip reset or when a 'reset Channel B receiver' command is invoked.

[3] Channel A External or Counter/Timer Status — This bit indicates that one of the following status bits is asserted: ICTSRA[6:4].

[2] Channel A Receiver or Transmitter Status — This bit indicates that one of the following status bits is asserted: RSRA[7:0], TRSRA[7:3].

[1] Channel A Transmitter Ready — The assertion of this bit indicates that one or more characters may be loaded into the Channel A transmitter FIFO to be serialized by the transmit shift register. See description of OMR[4]. This bit can be asserted only when the transmitter is enabled. Disabling or resetting the transmitter negates TxRDY.

[0] Channel A Receiver Ready — The assertion of this bit indicates that one or more characters are available in the Channel A receiver FIFO to be read by the CPU. See description of OMR[3]. RxRDY is initially reset (negated) by a chip reset or when a 'reset Channel A receiver' command is invoked.

Channel Command Register (CCRA, CCRB) — Commands to the DUSCC are entered through the channel command register. The format of that register is shown in Table 9. A read of this register returns the last invoked command (with bits 4 and 5 set to 1).

Transmitter Commands

0000 Reset transmitter. Causes the transmitter to cease operation immediately. The transmit FIFO is cleared and the TxD output goes into the marking state. Also clears the transmitter status bits (TRSR[7:4]) and resets the TxRDY status bit (GSR[1] or GSR[5] for Channels A and B, respectively). The counter/timer and other registers are not affected.

0001 Resest transmit CRC. This command is appended to and FIFOed along with the next character loaded into the transmit FIFO. It causes the transmitter CRC generator to be reset to its initial state prior to beginning transmission of the appended character.

0010 Enable transmitter. Enables transmitter operation, conditioned by the state of the CTS ENABLE Tx bit, TPR[2]. Has no effect if invoked when the transmitter has previously been enabled.

0011 Disable transmitter. Terminates transmitter operation and places the TxD output in the marking state at the next occurrence of a transmit FIFO empty condition. All characters currently in the FIFO, or any loaded subsequently prior to attaining an empty condition, will be transmitted.

0100 Transmit start of message. Used in COP and BOP modes to initiate transmission of a frame after the transmitter is first enabled, prior to sending the contents of the FIFO. Can also be used to precisely control the number of SYN/FLAGs at the beginning of transmission or in between frames.

When the transmitter is first enabled, transmission will not begin untill this command (or the transmit SOM with PAD command, see below) is issued. The command causes the SYN (COP) or FLAG (BOP) pattern to be transmitted. SEND SOM ACK (TRSR[4]) is set when transmission of the SYN/FLAG begins. The CPU may then reinvoke the command if multiple SYN/FLAGs are to be transmitted. Transmission of the FIFO characters begin when the command is no longer invoked. If the FIFO is empty, SYN/FLAGs continue to be transmitted until a character is loaded into the FIFO, but the status bit (TRSR[4]) is not set. Insertion of SYN/FLAGs between frames can be accomplished by invoking this command after the frame complete status bit (TRSR[5]) has been asserted in re-

sponse to transmission of the end-of message sequence.

0101 Transmit start of message with opening PAD. Used in COP and BOP modes after the transmitter is first enabled to send a bit pattern for DPLL synchronization prior to transmitting the opening SYN (COP) or FLAG (BOP). the SYN/FLAG is sent at the next occurrence of a transmit FIFO empty condition. All characters currently in the FIFO, or any loaded subsequently prior to attaining an empty condition, will be transmitted. While the PAD characters are transmitted, the character length is set to 8 bits, (regardless of the programmed length), and parity generation (COP), zero insertion (BOP) and LRC/CRC accumulation are disabled. SEND SOM ACK (TRSR[4]) is set when transmission of the SYN/FLAG begins. The CPU may then invoke the transmit SOM command if multiple SYN/FLAGs are to be transmitted.

The TSOM/TSOMP commands, described above, are sampled by the controller in alternate bit times of the transmitter clock. As a consequence, the first bit time of a COP/BOP frame will be transmitted on the TxD pin, after a maximum of three bit times, after the command is issued. (The additional 1-bit delay in the data path is due to the data encoding logic.)

0110 Transmit end-of-message. This command is appended to the next character loaded into the transmit FIFO. It causes the transmitter to send the end-of message sequence (selected FCS in COP modes, FCS-FLAG in BOP modes) after the appended character is transmitted. Frame complete (TRSR[5]) is set when transmission of the FCS begins. This command is also asserted automatically if the TEOM on zero count or one control bit (TPR[4]) is asserted, and the counter/timer is programmed to count transmitted characters when the character which causes the count to go to zero is loaded into the transmit FIFO. TEOM is not recognized if the transmitter FIFO is full.

0111 Transmit Abort BOP/Transmit Break ASYNC. In BOP modes, causes an abort (eight ones) to be transmitted after transmission of the character currently in the shift register is completed. The transmitter then sends MARKs or FLAGs depending on the state of underrun control (TPR[7:6]). Send SOM/abort ack (TRSR[4]) is set when the transmission of the abort begins. If the command is reasserted before transmission of the previous ABORT is completed, the process will be repeated. This can be used to send the idle sequence. The 'transmit SOM' command must be used to initiate transmission of a new message. In either mode, invoking this command causes the transmit FIFO to be flushed (characters are not transmitted).

In ASYNC mode, causes a break (space) to be transmitted after transmission of the character currently in the shift register is completed. Send break ack (TRSR[4]) is set when the transmission of the break begins. The transmitter keeps track of character times. If the command is reasserted, send break ack will be set again at the beginning of the next character time. The user can use this mechanism to control the length of the break in character time multiples. Transmission of the break is terminated by issuing a 'reset Tx' or 'disableTx' command.

1000 Transmit DLE. Used in COP modes only. This command is appended to and FIFOed with the next character loaded into the transmitter FIFO. It causes the transmitter to send a DLE, (EBCDIC H'10', ASCII H'10') prior to transmitting the appended character. If the transmitter is operating in BISYNC transparent mode, the transmitter control logic automatically causes a second DLE to be transmitted whenever a DLE is detected at the top of the FIFO. In this case, the TDLE command should not be invoked. An extra (third) DLE, however, will not be sent if the transmit DLE command is invoked.

1001 Go active on poll. Used in BOP loop mode only. Causes the transmitter, if it is enabled, to begin sending when an EOP sequence consisting of a zero followed by seven ones is detected. The last one of the EOP is changed to zero, making it another FLAG, and then the transmitter operates as described in the detailed operation section. The loop sending status bit (TRSR[6]) is asserted concurrent with the beginning of transmission.

1010 Reset go active on poll. Clears the stored 'go active on poll' command.

1011 Go on-loop. Used in BOP loop mode to control the assertion of the LCN output. This output provides the means of controlling external loop interface hardware to go on-loop and off-loop. When the command is asserted, the DUSCC will look for the receipt of a zero followed by seven ones, at which time it will assert the LCN output and set the delta DCD/LC status bit (ICTSR[4]). This allows the DUSCC to break into the loop without affecting loop operation. This command must be used to initiate loop mode operation.

1100 Go off-loop. Used in BOP loop mode to control the negation of the LCN output. This output provides the means of controlling external loop interface hardware to go on-loop and off-loop. When the command is asserted, the DUSCc will look for the receipt of eight contiguous ones, at which time it will negate the LCN output and set the delta DCD/LC status bit (ICTSR[4]). This allows the DUSCC to get off the loop operation. This command is normally used to terminate loop mode operation.

1101 Exclude from CRC. This command is appended to and FIFOed along with the next character loaded into the transmit FIFO. It causes the transmitter CRC generator to be disabled while the appended character is being transmitted. Thus, that character is not included in the CRC accumulation.

Receiver Commands

0000 Reset Receiver. Causes the receiver to cease operation, clears the receiver FIFO, clears the data path, and clears the receiver status (RSR[7:0], TRSR[3:0], and either GSR[0] or GSR[4] for Channels A and B, respectively). The counter/timer and other registers are not affected.

0001 Reserved.

0010 Enable receiver. Causes receiver operation to begin, conditioned by the state of the DCD ENABLED Rx bit, RPR[2]. Receiver goes into START, SYN, or FLAG search mode depending on channel protocol mode. Has no effect if invoked when the receiver has previously been enabled.

0011 Disable receiver. Terminates operation of the receiver. Any character currently being assembled will be lost. Does not affect FIFO or any status. While in COP mode, disabling the receiver does not clear the data path; in all other cases, it does.

Counter/Timer Commands

0000 Start. Starts the counter/timer and prescaler.

0001 Stop. Stops the counter/timer and prescaler. Since the command may be asynchronous with the selected clock source, the counter/timer and/or prescaler may count one or more additional cycles before stopping.

0010 Preset to FFFF. Presets the counter timer to H'FFFF' and the prescaler to its initial value. This command causes the C/T output to go Low.

0011 Preset from CTPRH/CTPRL. Transfers the current value in the counter/timer preset registers to the counter/timer and presets the prescaler to its initial value. This command causes the C/T output to go Low.

Digital Phase-Locked Loop Commands

0000 Enter Search Mode. This command causes the DPLL counter to be set to the value 15 and the clock output will be forced Low. The counter will be disabled until a transition on the data line is detected, at which point it will start incrementing. After the counter reaches a count of 31, it will reset to zero and cause the clock output to go from Low to High. The DPLL will then continue normal operaton. This allows theDPLL to be locked onto the data without pre-frame transitions. This command should not be used if the DPLL is programmed to supply the clock for the transmitter is active.

0001 Disable DPLL. Disables operation of the DPLL.

0010 Set FM Mode. Sets the DPLL to the FM mode of operation, used when FM0, FM1, or Manchester (NMRZ) is selected by CMR1[7:6].

0011 Set NRZI Mode. Sets the DPLL to the NRZI mode of operation, used when NRZ or NRZI is selected by CMR1[7:6].

0100 Reserved for test.

0101 Reserved for test.

Table 9. Command Register Bit Format

CHANNEL COMMAND REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CCRA, CCRB)	00 = Transmitter CMD		don't care	don't care	**Transmitter Command** 0000 — reset Tx 0001 — reset TxCRC* 0010 — enable Tx 0011 — disable Tx 0100 — transmit SOM (TSOM) 0101 — transmit SOM with PAD (TSOMP) 0110 — transmit EOM (TEOM)* 0111 — transmit ABORT/BREAK (TABRK) 1000 — transmit DLE (TDLE)* 1001 — go active on poll 1010 — reset go active on poll 1011 — go on-loop 1100 — go off-loop 1101 — exclude form CRC*			
	01 = Receiver CMD		don't care	don't care	**Receiver Command** 0000 — reset Rx 0001 — reserved 0010 — enable Rx 0011 — disable Rx			
	10 = C/T CMD		don't care	don't care	**Counter/Timer Command** 0000 — start 0001 — stop 0010 — preset to FFFF 0011 — preset from CTPRH/CTPRL			
	11 = DPLL CMD		don't care	don't care	**DPLL Command** oooo — enter search mode 0001 — disable DPLL 0010 — set FM mode 0011 — set NRZI mode 0100 — reserved for test 0101 — reserved for test			

DETAILED OPERATION

Interrupt Control

A single interrupt output (IRQN) is provided which is activated upon the occurrence of any of the following conditions:

Channel A external or C/T special condition

Channel B external or C/T special condition

Channel A Rx/Tx error or special condition

Channel B Rx/Tx error or special condition

Channel A TxRDY

Channel B TxRDY

Channel A RxRDY

Channel B RxRDY

Each of the above conditions occupies a bit in the General Status Register (GSR). If ICR[2] is set, the eight conditions are encoded into three bits which are inserted into bits [2:0] or [4:2] of the interrupt vector register. This forms the content of the IVRM during an interrupt acknowledge cycle. Unmodified and modified vectors can read directly through specified registers. Two of the conditions are the inclusive OR of several other maskable conditions:

- External or C/T special condition: Delta DCD, Delta CTS or C/T zero count (ICTSR[6:4]).
- Rx/Tx error or special condition: any condition in the Receiver Status Register (RSR[7:0]) or a transmitter or DPLL condition in the Transmitter and Receiver Status Register (TRSR[7:3]).

The TxRDY and RxRDY conditions are defined by OMR[4] and OMR[3], respectively. Also associated with the interrupt system are the Interrupt Enable Register (IER), one bit in the Counter/Timer Control Register (CTCR), and the Interrupt Control Register (ICR).

The IER is programmed to enable specified conditions or groups of conditions to cause an interrupt by asserting the corresponding bit. A negated bit prevents an interrupt from occurring when the condition is active and hence masks the interrupt. In addition to the IER, CTCR[7] could be programmed to enable or disable an interrupt upon the C/T zero count condition. The interrupt priorities within a channel are fixed. Priority between channels is controlled by ICR[7:6]. Refer to Table 8 and ICR[7:6].

The ICR contains the master interrupt enables for each channel (ICR[1] andICR[0]) which must be set if the corresponding channel is to cause an interrupt. The CPU vector mode is specified by ICR[5:4] which selects either vectored or non-vectored operation. If vectored mode is selected, the content of the IVR or IVRM is placed on the data bus when IACK is activated. If ICR[2] is set, the content of IVRM is output which contains the content of IVR and the encoded status of the interrupting condition.

Upon receiving an interrupt acknowledge, the DUSCC locks its current interrupt status until the end of the acknowledge cycle. If it has an active interrupt pending, it responds with the appropriate vector and then asserts DTACKN. If it does not have an interrupt, it propagates the acknowledge through its X2/IDCN output if this function is programmed in PCRA[7]; otherwise, the IACKN is ignored. Locking the interrupt status at the leading edge of IACKN prevents a device at a High position in the interrupt daisy chain from responding to an IACK issued for a lower priority device while the acknowledge is being propagated to that device.

DMA Control

The DMA control section provides the interface to allow the DUSCC to operate with an external DMA controller. One of four modes of DMA can be programmed for each channel independently via CMR2[5:3]:

- Half-duplex single address. In this mode, a single pin provides both DMA read and write requests. Acknowledgement of the requests is via a single DMA acknkowledge pin. The data transfer is accomplished in a single bus cycle — the DMA controller places the memory address of the source or destination of the data on the address bus and then issues the acknowledge signal, which causes the DUSCC to either write the data into its transmit FIFO (write request) or to output the contents of the top of the recieve FIFO (read request). The cycle is completed when the DTCN input is asserted by the DMA controller. This mode can be used when channel operation is half-duplex (e.g., BISYNC) and allows a single DMA channel to service the receiver and transmitter. The receiver and transmitter should not be enabled at the same time when half-duplex mode is programmed.
- Half-duplex dual address. In this mode, a single pin provides both DMA read and write requests. Acknowledgement of the requests is via normal bus read and write cycles. The data transfer requires two bus cycles — the DMA controller acquires the data from the source (memory for a Tx DMA or DUSCC for a Rx DMA) on the first cycle and deposits it at the destination (DUSCC for a Tx DMA or memory for a Rx DMA) on the second bus cycle. This mode is used when channel operation is half-duplex (e.g., BISYNC) and allows a single DMA channel to service the receiver and transmitter.
- Full-duplex single address. This mode is similar to half-duplex single address mode but provides separate request and acknowledge pins for the receiver and transmitter.
- Full-duplex dual address. This mode is similar to half-duplex dual address mode but provides duplex dual address mode and provides separate request pins for the receiver and transmitter

Figures 4 through 7 describe operation of the DUSCC in the various DMA environments. Table 10 summarizes pins used for the DMA request and acknowledge function for the transmitter and receiver for the different DMA modes.

The DMA request signals are functionally identical to the TxRDY and RxRDY status signals for each serial channel except that the DMA request signals are negated on the leading edge of the acknowledge signal when the subsequent transfer causes the FIFO to become full (transmitter request) or empty (receiver request).

In non-DMA operation TxRDY and RxRDY signals are automatically negated only after the transfer is completed. The DMA read request can be programmed through OMR[3] be asserted either when any character is in the receive FIFO or only when the receive FIFO is full. Likewise, the DMA write request can be programmed through OMR[4] to be asserted either when the transmit FIFO is not full or only when the transmit FIFO is empty (The transmitter must be enabled for a DMA request to be asserted). The request signals are automatically negated when the respective data transfer cycle is completed and the FIFO becomes full (transmitter request) or empty (receiver request). If a transfer is completed and the FIFO is not left full (transmitter) or empty (receiver), the request stays Low. The request may be negated by the CPU with a status reset write cycle. (Although DONEN terminates all DMA transfers, it has no effect on the requests. The requests are a function of the FIFO status, but they can be negated by writing into the GSR.) When the serial channel is not operating in DMA mode, the request and acknowledge pins for the channel can be programmed for other functions (see Pin Descriptions).

DMA DONEN Operation

As an input, DONEN is asserted by the DMA controller concurrent with the corresponding DMA acknowledge to indicate to the DUSCC that the character being transferred into the TxFIFO is the last character of the transmission frame. In synchronous modes, the DUSCC can be programmed through TPR[4] to automati-

cally transmit the frame termination sequence (e.g., FCS-FLAG in BOP mode) upon receipt of this signal.

As an output, DONEN is asserted by the DUSCC under the following conditions:

a. In response to the DMA acknowledge for a receiver DMA request if the FIFOed RECEIVED EOM status bit (RSR[7]) is set for the character being transferred.

b. In response to the DMA acknowledge for a receiver DMA request if the counter/timer has been programmed to count transmitted characters and the terminal count has occurred.

Block Transfers Using DTACK

The DTACKN line may be used to synchronize data transfers to and from the DUSCC utilizing a 'wait' state. Either the receive or the transmitter or both may be programmed for this mode of operation, independently for each channel, via CMR2[5:3].

In this mode, if the CPU attempts a write to the transmit FIFO and an empty FIFO position is not available, the DTACKN line will remain negated until a position empties. The data will then be written into the FIFO and DTACKN will be asserted to signify that the transfer is complete.

Similarly, a read of an empty receive FIFO will be held off until data is available to be transferred. Potentially, this mode can cause the microcomputer system to hang up if, for example, a read request was made and no further data was available.

Table 10. DMA REQ and ACK Pins for Operational Modes

FUNCTION	HALF DUPLEX SINGLE ADDR DMA	HALF DUPLEX DUAL ADDR DMA	FULL DUPLEX SINGLE ADDR DMA	FULL DUPLEX DUAL ADDR DMA
RCVR REQ	RTxDRQN	RTxDRQN	RTxDRQN	RTxDRQN
TRAN REQ	Same as RCVR REQ	Same as RCVR REQ	TxDRQN	TxDRQN
RCVR ACK	RTxDAKN	Normal read RCVR FIFO	RTxDAKN	Normal read RCVR FIFO
TRAN ACK	Same as RCVR ACK	Normal write TRAN FIFO	TxDAKN	Normal write TRAN FIFO

Timing Circuits

The timing block for each channel consists of a crystal oscillator, a Bit Rate Generator (BRG), a Digital Phase-Locked Loop (DPLL) and a 16-bit Counter/Timer (C/T) (see Figure 8).

Crystal Oscillator

The crystal oscillator operates directly from a crystal (normally 14.7456MHz if the internal BRG is to be used) connected across the X1/CLK and X2/IDCN pins with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to the X1/CLK pin. This signal is divided by two to provide the internal system clock.

Bit Rate Generator

The BRG operates from the oscillator or external clock and is capable of generating 16-bit rates. These are available to the receiver, transmitter, DPLL, and C/T. The BRG output is at 32X the base bit rate. Since all sixteen rates are generated simultaneously, each receiver and transmitter may select its bit rate independently. The transmitter and receiver timing registers include a 4-bit field for this purpose (TTR[3:0], RTR[3:0]).

Digital Phase-Locked Loop

Each channel of the DUSCC includes a DPLL used in synchronous modes to recover clock information from a received data stream. The DPLL is driven by a clock at nominally 32 times the data rate. This clock can be programmed, via RTR[7:4], to be supplied from an external input, from the receiver BRG, from the C/T, or directly from the crystal oscillator.

The DPLL uses this clock, along with the data stream to construct a data clock which may then be used as the DUSCC receive clock, transmit clock, or both. The output of the DPLL is a square wave at 1X the data rate. The derived clock can also be programmed to be output on a DUSCC pin; only the DPLL receiver output clock is available at the TRxC pin. Four commands are associated with DPLL operation: Enter search mode, set FM mode, set NRZI mode, and disable DPLL. The commands are described in the Command Register Description. Waveforms associated with the DPLL are illustrated in Figure 9.

DPLL NRZI Mode Operation — This mode is used with NRZ and NRZI data encoding. With this type of encoding, the transitions of the data stream occur at the beginning of the bit cell. The DPLL has a six-bit counter which is incremented by a 32X clock. The first edge detected during search mode sets the counter to 16 and begins operation. The DPLL output clock then rises at a count of 0 and falls at 16. Data is sampled on the rising edge of the clock. When a transition in the data stream is detected, the count length is adjusted by one or two counts, depending on the counter value when the transition occurs (see Table 11). A transition detection at the roll-over point (third column in Figure 11) is treated as a transition occurring at zero count.

The count length adjustments cause the rising edge of the DPLL output block to converge to the nominal center of the bit cell. In the worst case, which occurs when a DPLL pulse is coincident with the data edge, the DPLL converges after 12 data transitions.

For NRZ encoded data, a stream of alternating ones and zeros should be used as a synchronizing pattern. For NRZI encoded data, a stream of zeros should be used.

Table 11. NRZI Mode Count Length

COUNT WHEN TRANSITION DETECTED	COUNT LENGTH ADJUSTMENT	COUNTER RESET AFTER COUNT REACHES
0 — 7	-2	29
8 — 15	-1	30
16 — 23	+1	32
24 — 30	+2	33
None detected	0	31

DPLL FM Mode Operation — FM operation is used with FM0, FM1, and Manchester data encoding. With this type of encoding, transitions in the data stream always occur at the beginning of the bit cell for FM0 and FM1, or at the center of the bit cell for Manchester. The DPLL 6-bit counter is incremented by a 32X clock. The first edge detected during search mode sets the counter to 16 and begins operation. The DPLL receiver clock then rises on a count of 8 and falls on 24. (The DPLL transmitter clock output falls on a count of 16. It rises on a count of 0 if a transition has been detected between count of 16 and 23. For other cases, it rises 1/2 count of the 32X input clock sooner.) This provides a 1X clock with edges positioned at the nominal centers of the two halves of the bit cell. The transition detection circuit is enabled between counts of 8 and 23, inclusive. When a transition is detected, the count length is adjusted by one, depending on when the transition occurs (see Table 12).

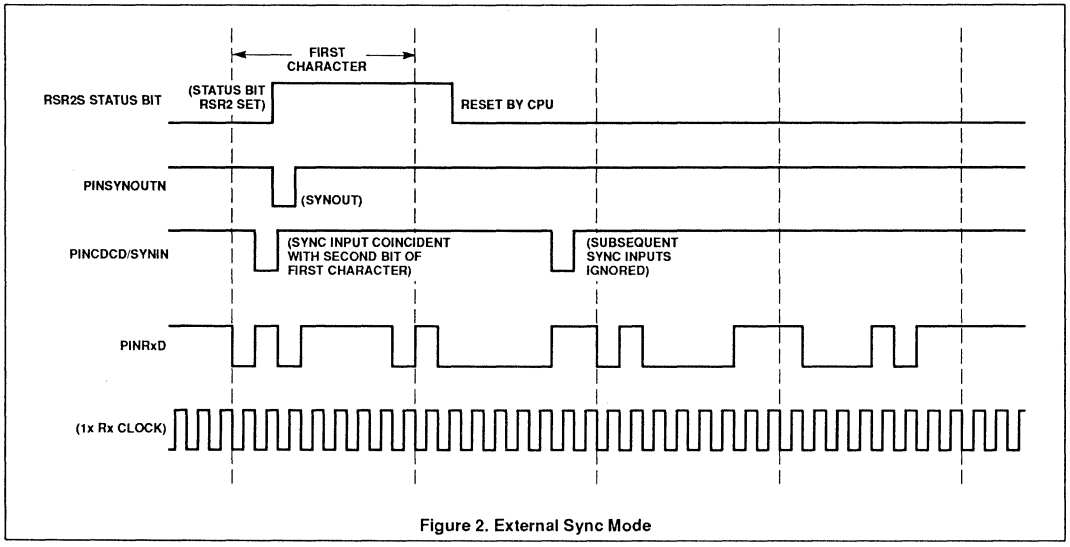


Figure 2. External Sync Mode

If a transition is not detected for two consecutive data bits, the DPLL is forced into search mode and the DPLL error status bit (TRSR[3]) is asserted. This feature is disabled when the DPLL output is used only as the transmitter clock.

To prevent the DPLL from locking on the wrong edges of the data stream, an opening PAD sequence should be transmitted. For FM0, a stream of at least 16 ones should be sent initially. For FM1, a minimum stream of 16 zeros should be sent and for Manchester encoding the initial data stream should consist of alternating ones and zeros.

Table 12. FM Mode Count Length

COUNT WHEN TRANSITION DETECTED	COUNT LENGTH ADJUSTMENT	COUNTER RESET AFTER COUNT REACHES
8 — 15	-1	30
16 — 23	+1	32
24 — 7	Disabled	
None detected	0	31

Counter/Timer

Each channel of the DUSCC contains a Counter/Timer (C/T) consisting of a 16-bit down counter, a 16-bit preset register, and associated control circuits. Operation of the counter/timer is programmed via the Counter/Timer Control Register (CTCR). There are also four commands associated with C/T operation, as described in the Command Description section.

The C/T clock source, clock prescaling, and operating mode are programmed via CTCR[2:0], CTCR[4:3], and CTCR[6], respectively. The preset register is loaded with minimum of 2 by the CPU and its contents can be transferred into the down counter by a command, or automatically upon reaching terminal count if CTCR[6] is negated. Commands are also available to stop and start the C/T and to preset it to an initial value of FFFF. Counting is triggered by the falling edge of the clocking input. The C/T zero count status bit, ICTSR[6], is set when the C/T reaches the terminal count of zero and ICTSR[7] indicates whether the counter is currently enabled or not.

An interrupt is generated upon reaching zero count if CTCR[7] and the channel's master interrupt enable are asserted. The output of the C/T can be programmed to be output on the channel's RTxC or TRxC pin (via PCR[4:0]) as either a single pulse or a square wave, as programmed in CTCR[5]. The contents of the C/T can be read at any time by the CPU, but the C/T should normally be stopped before this is done. Several C/T operating modes can be selected by programming of the counter/timer control register. Typical applications include:

1. Programmable divider. The selected clock source, optionally prescaled, is divided by the contents of the preset register. The counter automatically reloads itself each time the terminal count is reached. In this mode, the C/T may be programmed to be used as the Rx or Tx bit rate generator, as the input to the DPLL, or it may be output on a pin as either a pulse or a square wave. The C/T interrupt should be disabled in this mode.
2. Periodic interrupt generator. This mode is similar to the programmable divider mode, except that the C/T interrupt is enabled, resulting in a periodic interrupt to the CPU.
3. Delay timer. The counter is preset from the preset register and a clock source, optionally prescaled, is selected. An interrupt is generated upon reaching terminal count. The C/T continues counting without reloading itself and its contents may be read by the CPU to allow additional delay past the zero count to be determined.
4. Character counter. The counter is preset to FFFF by command and the clock source becomes the internal signal used to control loading of the Rx or Tx characters. This operation is selected by CTCR[2:0]. The C/T counts characters loaded into the RxFIFO by the receiver or loaded into the transmit FIFO by the CPU, respectively. The current character count can be determined by the CPU by reading the contents of the C/T and taking its ones complement. Optionally, a preset number may be loaded into the counter and an interrupt generated when the count is exhausted. When counting Tx characters, the terminal count condition can be programmed through TPR[4] to cause an end of message sequence to be transmitted. When counting received

characters, the FIFOed EOM status bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. The channel's 'reset Tx' or 'reset Rx' commands have no effect on the operation of the C/T.

5. External event counter. The counter is preset to FFFFF by command and an external clock source is selected. The current count can be determined by the CPU by reading the contents of the C/T and taking its ones complement. Optionally, a preset number may be loaded into the counter and an interrupt generated when the count is exhausted.
6. Bit length measurement. The counter is preset to FFFF by command and the X1/CLK/4 clock input gated by RxD mode (optionally prescaled) is programmed. The C/T starts counting when RxD goes Low and stops counting when RxD goes High. At this time, ICTSR[6] is set and an interrupt (if enabled) is generated. The resulting count in the counter can be read by the CPU to determine the bit rate of the input data. Normally this function is used for asynchronous operation.

Communication Channels A and B

Each communication channel of the DUSCC is a full-duplex receiver and transmitter that supports ASYNC, COP, and BOP transmission formats. The bit rate clock for each receiver and transmitter can be selected independently to come from the bit rate generator, C/T, DPLL, or an external input (such as a modem generated clock).

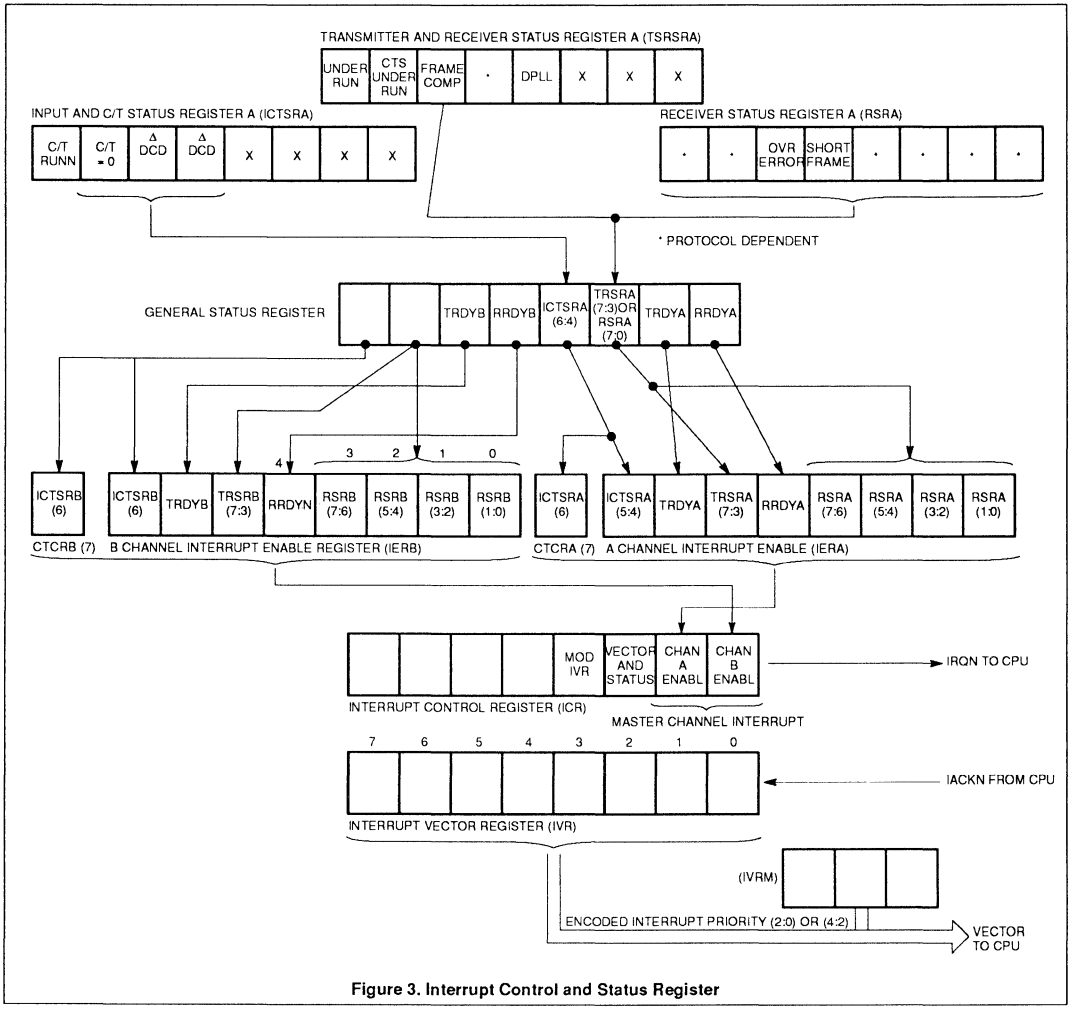


Figure 3. Interrupt Control and Status Register

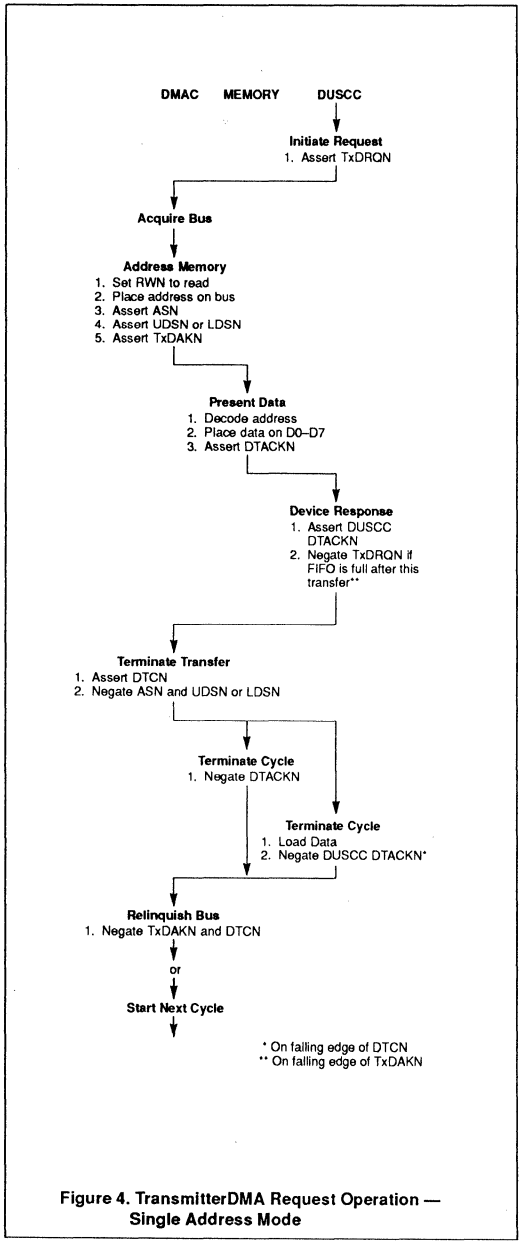


Figure 4. TransmitterDMA Request Operation — Single Address Mode

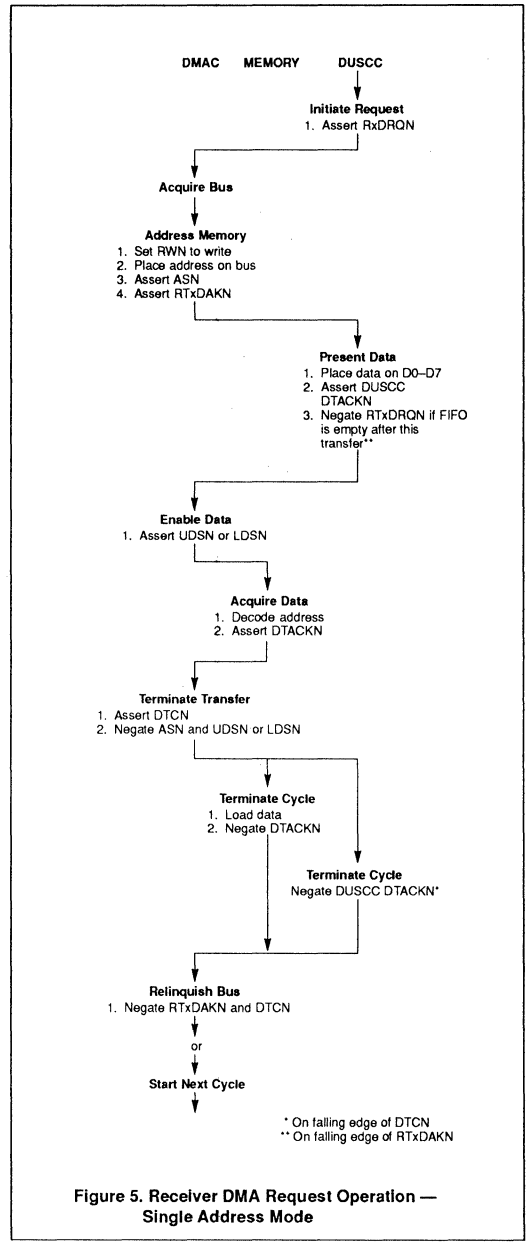


Figure 5. Receiver DMA Request Operation — Single Address Mode

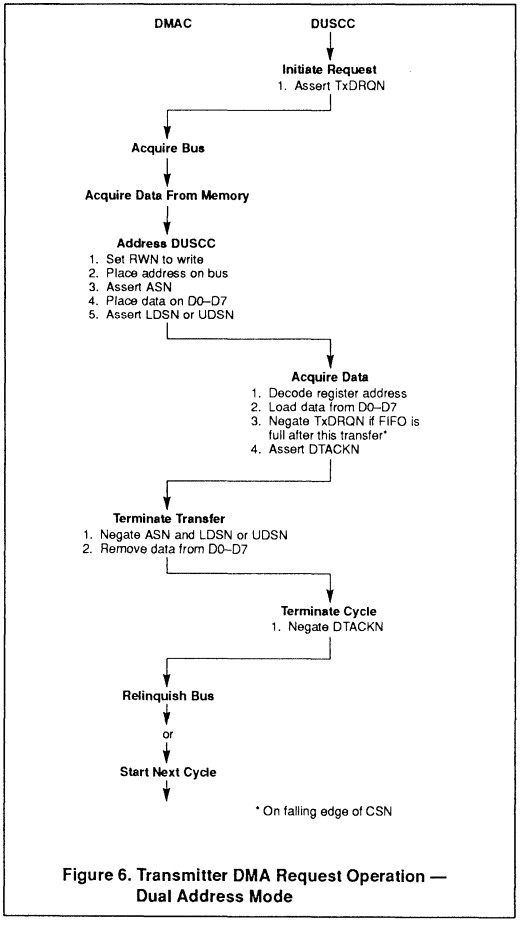


Figure 6. Transmitter DMA Request Operation — Dual Address Mode

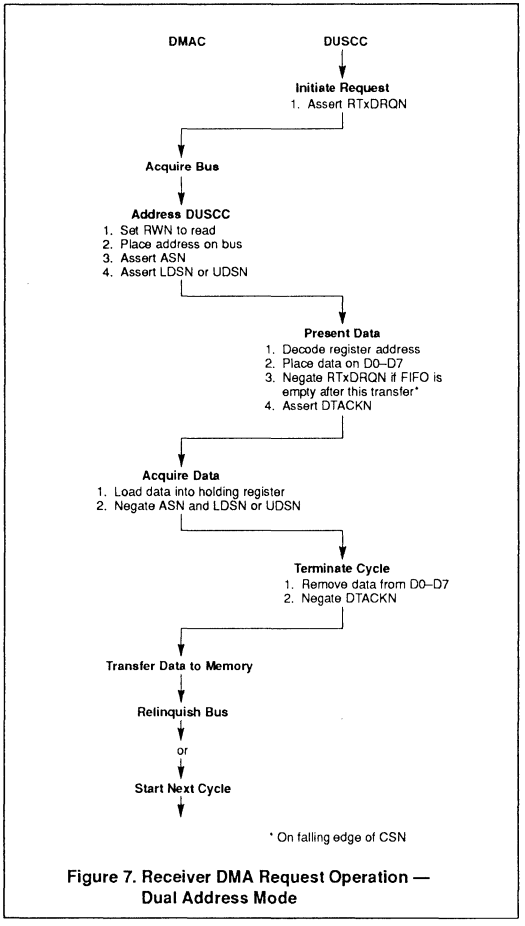


Figure 7. Receiver DMA Request Operation — Dual Address Mode

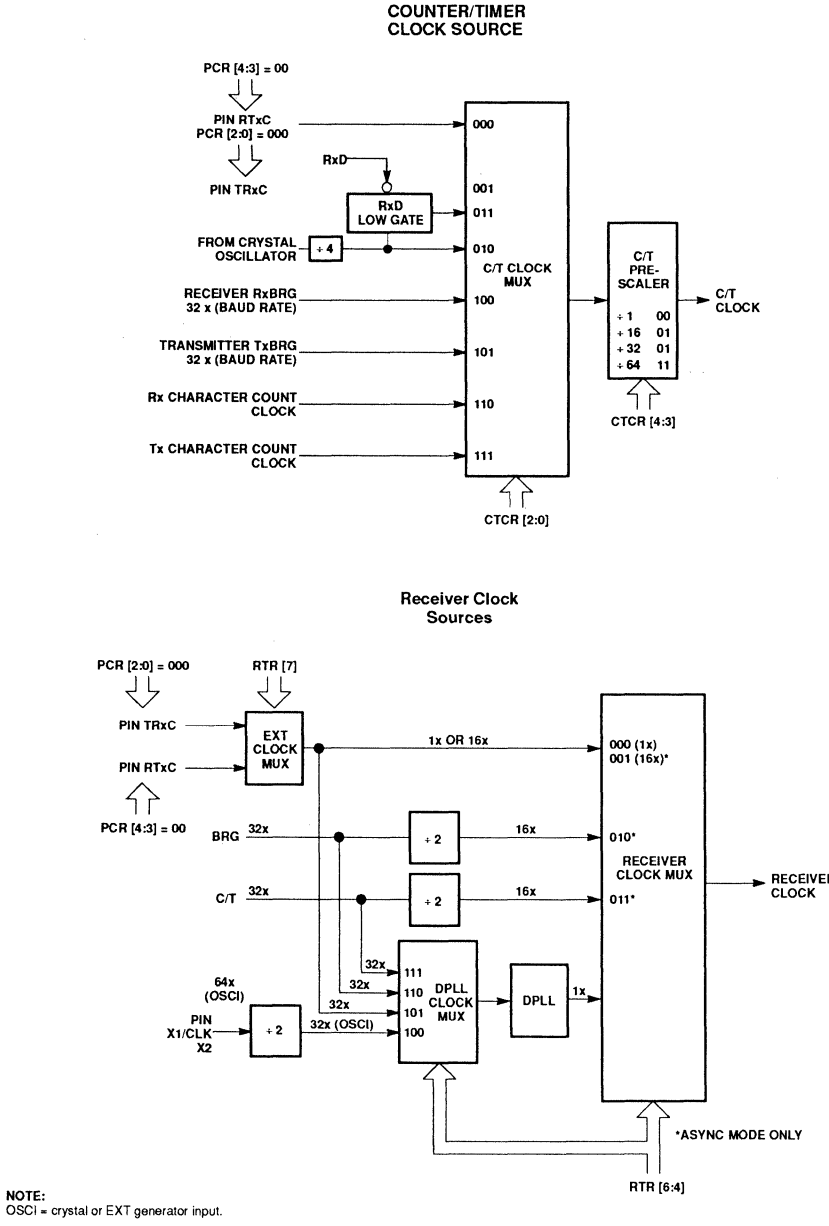
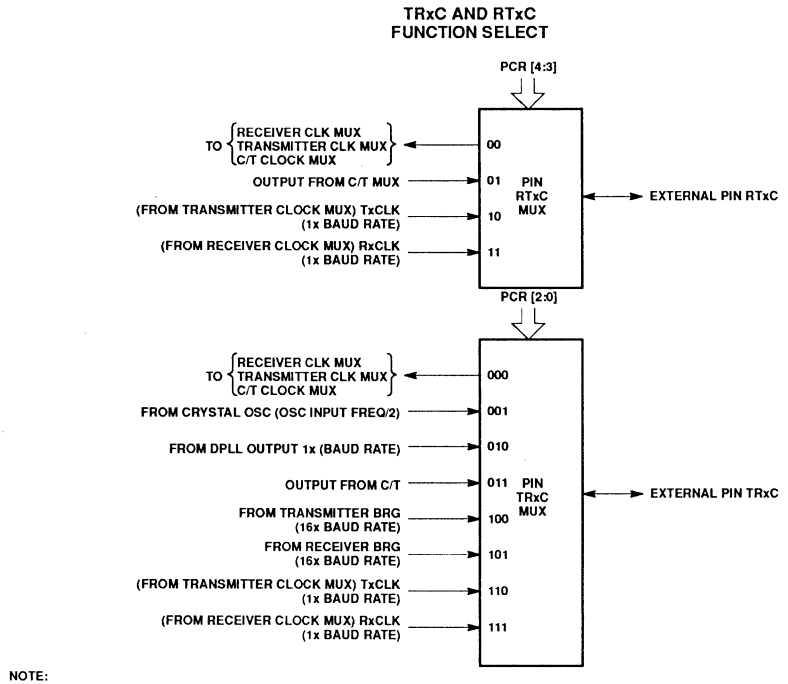


Figure 8. Timing Block



NOTE:
OSCI = crystal or EXT generator input.

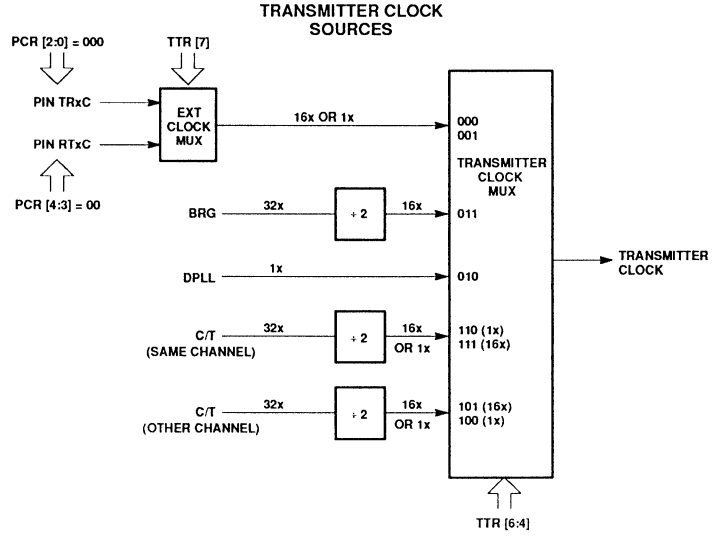


Figure 8. Timing Block (Continued)

TRANSMITTER

Transmitter TxFIFO and TxRDY

The transmitter accepts parallel data from the data bus and loads it into the TxFIFO, which consists of four 8-bit holding registers. This data is then moved to the Transmitter Shift Register (TxSR) which serializes the data according to the transmission format programmed. The TxSR is loaded from the TxFIFO, from special character logic, or from the CRC/LRC generator. The LSB is transmitted first, which requires right justification of characters by the CPU. TxRDY (GSR[5] or GSR[1]) and underrun (TRSR[7]) indicate the state of the TxFIFO. The TxFIFO may be addressed at any of four consecutive locations (see Table 1) to allow use of multiple byte work instructions. A write to any valid address always writes data to the next empty FIFO location.

TxRDY is set when the transmitter is enabled and there is an empty position in the TxFIFO (OMR[4] = 0) or when the TxFIFO becomes empty (OMR[4] = 1). The CPU may reset TxRDY through a status reset write cycle. If this is done, it will not be reasserted until a character is transferred to the TxST (OMR[4] = 0) or when the TxFIFO becomes empty again (OMR[4] = 1). The assertion of TxRDY, enabling of the IER [6] and the enabling of the channel master interrupt ICR[0] or [1] allow an interrupt to be generated.

If DMA operation is programmed, either RTxDRN (half-duplex) or TxDRQN (full-duplex) follows the state of TxRDY if the transmitter is enabled. These operations differ from normal ready in that the request signal is negated on the leading edge of the DMA acknowledge signal when the subsequent transfer causes the transmit FIFO to become full, while the TxRDY signal is negated only after the transfer is completed. Underrun status TRS[7] set indicates that one or more data character (not PAD characters) have been transmitted and the TxFIFO and TxSR are both empty.

In 'wait on Tx', a write to a full FIFO causes the write cycle to be extended until a FIFO position is available. DTACKN is asserted to acknowledge acceptance of the data. In non-wait modes, if an attempt is made to load data into a full TxFIFO, the TxFIFO data is preserved and the overrun data character(s) is lost. A normal DTACKN will be issued, and no indication of this occurrence is provided. The transmitter is enabled by the enable transmitter command. When the disable transmitter command is issued, the transmitter continues to operate until the TxFIFO becomes empty. The TxRDY does not become valid until the transmitter is enabled. Characters can be loaded into the FIFO while disabled. However, if the FIFO is full when the transmitter is enabled, TxRDY is not asserted.

TxRTS Control

If TxRTS CONTROL, TPR[3], is programmed, the channel's RTS output is negated 5-bit times after the last bit (stop bit in ASYNC mode) of the last character is transmitted. RTS is normally asserted and negated by writing to OMR[0]. Setting of TPR[3] causes RTS to be reset automatically (if the transmitter is not enabled) after all characters in the transmitter FIFO (if any) are transmitted and five bit times after the 'last character' is shifted out. This feature can be used to automatically terminate the transmission of a message as follows:

- Program auto-reset mode: TPR[3] = 1.
- Enable transmitter.
- Assert RTSN: OMR[0] = 1.
- Send message.
- Disable transmitter after the last character is loaded into the TxFIFO.
- The last character will be transmitted and OMR[0] will be reset five bit times after the last bit, causing RTSN to be negated. The TxD output will remain in the marking state until the transmitter is enabled again.

The 'last bit' in ASYNC is simply the last stop bit of the character. In BOP and COP, the last character is defined either explicitly by either appending it with TEOM or implicitly through the selection of the frame underrun control sequence, TPR[7:6] (Transmitter Parameter Register). Table 13 summarizes the relationship of the selected underrun sequence and the protocol mode.

Tx CTS Operation

If CTS enable Tx, TPR[2], is set, the CTSN input must be asserted for the transmitter to operate. Changes in CTSN while a character is being transmitted do not affect transmission of that character. However, if the CTS input becomes negated when TPR[2] is set and the transmitter is enabled and ready to start sending a new character, CTS underrun, TRSR[6], is asserted and the TxD output is placed in the marking (High) state. In ASYNC mode, operation resumes when CTSN is asserted again. In COP and BOP modes, the transmission of the message is terminated and operation of the transmitter will not resume until CTS is asserted and a TSOM or TSOMP command is invoked. Prior to issuing the command and retransmitting the message, the transmitter must be reset. After a change-of-state STS is established by the input sampling circuits (refer to the description of ICTSR[4], it is sampled by the Tx controller 1-1/2 bit times before each new character is serialized out of the Tx shift register. (This is 2-1/2 bits before the LSB of the new character appears on the TxD pin; there is an additional 1-bit delay in the transmitter data path due to the data encoding logic.)

Tx Special Bit Pattern Transmission

The DUSCC provides features transmit special bit patterns (see Table 14).

The TxD pin is held marking after a hardware reset, a reset Tx command, when the transmitter is not enabled, and during underrun/idle, if this feature is selected through TPR[7:5]. The TxD pin is also held marking if the transmitter is enabled, and the TxFIFO is empty (ASYNC), or if a TSOM or TSOMP command has not been issued (SYNC modes).

The following command bits can be appended to characters in the TxFIFO: TEOM, TDLE, exclude from CRC, and reset TxCRC. An invoked command(s) is appended to the next character loaded into the TxFIFO and follows the character through the FIFO until that character is ready to be loaded into the TxSR. The transmitter for the various protocols.

Tx ASYNC Mode

Serialization begins when the TxFIFO data is loaded into the TxSR. The transmitter first sends a start bit, then the programmed number of bits/character (TPR[1,0]), a parity bit (if specified), and the programmed number of stop bits. following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output goes to marking and the underrun condition (TRSSR[7]) is set.

Transmission resumes when the CPU loads a new character into the TxFIFO or issues a send break command. The send break command clears the TxFIFO and forces a continuous space (Low) on the TxD output after the character in TxSR (if any) is serialized. A send break acknowledge (TRSR[4]) is returned to the CPU to facilitate reassertion of the send break command in order to send an integral number of break characters. The send break condition is cleared when the reset Tx or disable Tx command is issued.

Tx COP Modes

Transmitter commands associated with all COP modes are: transmit SOM (TSOM, transmit start of message), transmit SOM with PAD (TSOMP0, transmit EO (TEOM, transmit end of message), reset TxCRC, exclude from CTC, and transmit DLE.

A TSOM or send TSOMP command must be issued to start COP transmission. TSOM (without PAD) causes the TxCRC/LRC generator to be initialized and one or two SYN characters from S1R/S2R to be loaded into the TXSR and shifted out on the TxD output. A parity bit, if specified, is appended to each SYN character after the MSB. Send SOM acknowledge (TRSR[4]) is asserted when the SYN output begins. The user may reinvoke the command to

cause multiple SYNs to be transmitted. If the command is not reinvoked and the TxFIFO is empty, SYN patterns continue to be transmitted until the TxFIFO is loaded. If data is present in the FIFO, the first character is loaded into the TxSR and serialization of the data begins. Note that the TxFIFO may be preloaded with data before the TSOM is issued.

The TSOMP command causes all characters in the TxFIFO (PAD characters) to be loaded into the TxSR and serialized if the Tx is enabled. Unlike the transmit SOM without PAD command, data (non-PAD characters) cannot be preloaded into the TxFIFO. While the PAD is transmitted, parity is disabled and character length is automatically set to 8 bits regardless of the value in TPR[1:0]. When the TxFIFO becomes empty after the PAD, the TxCRC/LRC generator is initialized, the SYN character(s) are transmitted with optional parity appended, and send SOM acknowledge asserted. Operation then proceeds in the same manner as the TSOM command; the user has the option to invoke the TSOM command to cause multiple SYNs to be transmitted.

After the TSOM/TSOMP command is executed, characters in the TxFIFO are loaded into the TxSR and shifted out with a parity bit, if specified, appended after the MSB. If, after the opening SYN(s) and at least one data has been transmitted, the TxFIFO is empty, a data underrun condition results and TRSR[7] is asserted. The transmitter's action on data underrun is determined by TPR[7:6] and the COP protocol. If TRP[7:6] = '10', the transmitter line fills with MARK characters until a character is loaded into the FIFO. I TRP[7:6] and the COP protocol. If TPR[7:6] = '11' is selected, the transmitter line fills with SYN, SYN1-SYN2, or DLE-SYN1 for monosync, dual sync, and BISYNC transparent modes, respectively. If TPR[7:6] = '00', the BCC characters are transmitted and frame complete (TRSR[6]) is set. TxD then assumes the programmed idle state (TPR[5]) of MARKs or SYN1/SYN1-SYN2.

Operation resumes with the transmission of a SYN sequence when a TSOM command is invoked. A TSOMP command is ignored unless the transmitter is disabled and then reenabled.

An appended TEOM command also terminates the frame as described above. It occurs after transmission of the character to which the TEOM is appended. The TEOM command can be explicitly asserted through the channel command register. If TPR[4] = '1', the TEOM is automatically appended to a character in DMA mode, if the DONEN input is asserted when that character is loaded into the TxFIFO, or if the counter/timer is counting transmitted characters when the character which causes the counter to reach zero count is loaded.

The TDLE command when appended to a character in the TxFIFO, causes the DLE character to be loaded into the the TxSR and serialized before the TxFIFO character is loaded into the TxSR and serialized. This feature is particularly useful for BISYNC operation. The DLE character will be excluded from the CRC accumulation in BISYNC transparent mode (see below), but will be included in all other COP modes.

In BISYNC mode, transmission of a DLE-STX character sequence (either via a send TDLE command appended to the STX character, or via DLE and STX loaded into the TxFIFO) puts the transmitter into the transparent test mode of operation. In this mode, normally restricted character sequences can be transmitted as 'normal' bit sequences. The switch occurs after transmission of the two characters, so that the DLE and STX are included in the BCC accumulation. If the DLE-STX is to be excluded from the CRC, the user should issue a 'reset CRC' command prior to loading the next character.

Another method of excluding the two characters from the CRC is to invoke the 'exclude from CRC' command prior to loading the character(s) into the FIFO. While in transparent mode, the transmitted line fills with DLE-SYN1 and automatically transmits an extra DLE if it finds a DLE in the TxFIFO ('DLE stuffing'). The transmitter reverts to non-transparent mode when the frame complete status is set in TRSR[5].

CRC/LRC accumulation can be specified in all COP modes; the type of CRC is specified via CMR2[2:0]. The TSOM/TSOMP commands set the CRC/LRC accumulator to its initial state and accumulation begins with the first non-SYN character after the initial SYN(s) are transmitted. PAD characters are not subject to CRC accumulation. In non-BISYNC or BISYNC normal modes, all transmitted characters except linefill characters (SYNs or MARKs) are subject to accumulation. In BISYNC transparent mode, odd (stuffed) DLEs and the DLE-SYN1 linefill are excluded from the accumulation. Characters can be selectively excluded from the accumulation by invoking the 'exclude form CRC' command prior to loading the character into the FIFO.

Accumulation stops when transmission of the first character of the BCC begins. The CPU can set the accumulator to its initial state prior to the transmission of any character by using the appended reset CRC command. The CRC generator is also automatically initialized after the EOM is sent.

Table 13. Abort Sequence — Protocol Mode

TPRA[7:6]	PROTOCOL	LAST CHARACTER
00	BOP	FLAG following either FCS (if selected) or last data character
	COP	Last byte of FCS before line begins SYN or MARKing
10	BOP	Abort sequence (11111111) prior to MARKing
	COP	Last byte of FCS before line begins SYN or MARKing
11	BOP	Abort sequence (11111111) prior to FLAG
	COP	First SYN of SYN sequence

Table 14. Special Bit Patterns

PROTOCOL	BIT PATTERN
ASYNC-BREAK	An all 0's character including parity bit (if specified) and stop bits. Used for send break command.
COP-SYN	Contained in S1R (single SYN mode) or in S1R/S2R (dual SYN modes). Used for TSOM and TSOMP commands and for non-transparent mode linefill and IDLE.
COP-DLE	Used for TDLE command and for BISYNC transparent mode linefill and to generate BISYNC control sequences.
COP-CRC	16/8 bits from the CRC/LRC accumulator used for TEOM command or for auto-EOM modes.
BOP-FLAG	01111110. Used for TSOM, TSOMP, and TEOM commands, for auto-EOM modes, and as an IDLE line fill.
BOP-ABORT	11111111. Used for send ABORT command or during TxFIFO underrun.
BOP-CRC	16 bits from the CRC accumulator used for TEOM command or for auto-EOM modes.
BOP/COP MARK	All 1's pattern on data line.

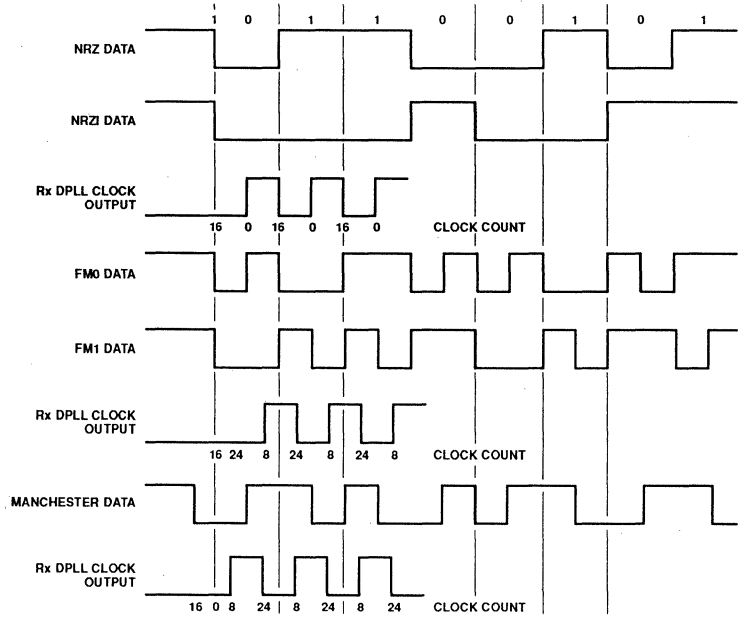


Figure 9. DPLL Waveforms

TxBOP Modes

Transmitter commands associated with BOP modes are TSOM, TSOMP, TEOM, and transmit ABORT (TABRK). The TSOM and TSOMP commands are identical to COP modes except that a FLAG character (01111110) is used as the start of message sequence instead of the SYNs, and FLAG(s) that continue to be sent until the TxFIFO is loaded. There is no zero insertion (see below) during transmission of the PAD characters, and they are not preceded by a FLAG or accumulated in the CRC. Character length is automatically set to 8 bits regardless of TPR[1:0].

The first characters loaded into the TxSR from the TxFIFO are the address and control fields, which have fixed character lengths of eight bits. The number of address field bytes is determined by CMR1[4:3]. If extended address field is specified, the field is terminated if the first address octet is H'00' or if the LSB of the octet is a 1. The number of control field bytes is selected by CMR1[5]. If any information field characters follow the control field (forming an I field), they are transmitted with the number of bits per character programmed in TPR[1:0]. The TEOM command can be appended to the last character whether explicitly or automatically as described for COP mode. When the character with the appended TEOM is loaded from the TxFIFO, it is transmitted with the character length specified by OMR[7:5]. In this way, a residual character of 1 - 8 bits is transmitted without requiring the CPU to change the Tx character length for this last character.

After opening the FLAG and first address octet have been transmitted, an underrun occurs (TRSR[7] = 1) if the TxFIFO is empty when the transmitter requires a new character. The underrun control bits (TPR[7:6]) determine whether the transmitter line fills with either ABORT-MARKs, ABORT-FLAGs (see below), or ends transmission with the 'normal' end of message sequence.

EOM on underrun is functionally similar to EOM due to an appended TEOM command. If the EOM is due to underrun, the normal character length applies to the last data character. After the last character is transmitted, the FCS (inverted CRC) and closing FLAG are sent, frame complete (TRSR[5]) is set, and the TxCRC is initialized. If the TxFIFO is empty after the closing FLAG has been sent, TXD will assume the programmed idle state of FLAGs or MARKs (TPR[5]) and wait for a character to be loaded into the FIFO or for a TSOM command to be issued. If the TXFIFO is not empty at that time, the TxFIFO data will be loaded into the TxSR and serialized. In that case, the closing FLAG is the opening FLAG of the next frame.

The user can control the number of FLAGs between frames by invoking the TSOM command after frame complete is asserted. The DUSCC then operates in the same manner as for transmission of multiple FLAGs at the beginning of a frame. When the command is no longer reinvoked, transmission of the TxFIFO data will begin. If the FIFO is empty, FLAGs continue to be transmitted.

The DUSCC provides automatic zero insertion in the data stream to prevent erroneous transmission of the FLAG sequence. All data characters loaded into the TxSR from the TxFIFO and characters transmitted from the CRC generator are subject to zero insertion. For this feature a zero is inserted in the serial data stream each time five consecutive ones (regardless of character boundaries) have been transmitted.

A send ABORT command clears the TxFIFO and inserts an ABORT character of eight ones (not subject to zero insertion) into the TxSR for transmission after the current character has been serialized. A send abort ack (TRSR[4]) facilitates reassertion of send abort by the user to guarantee transmission of multiple abort characters. This feature can be used to send the 15-ones idle sequence.

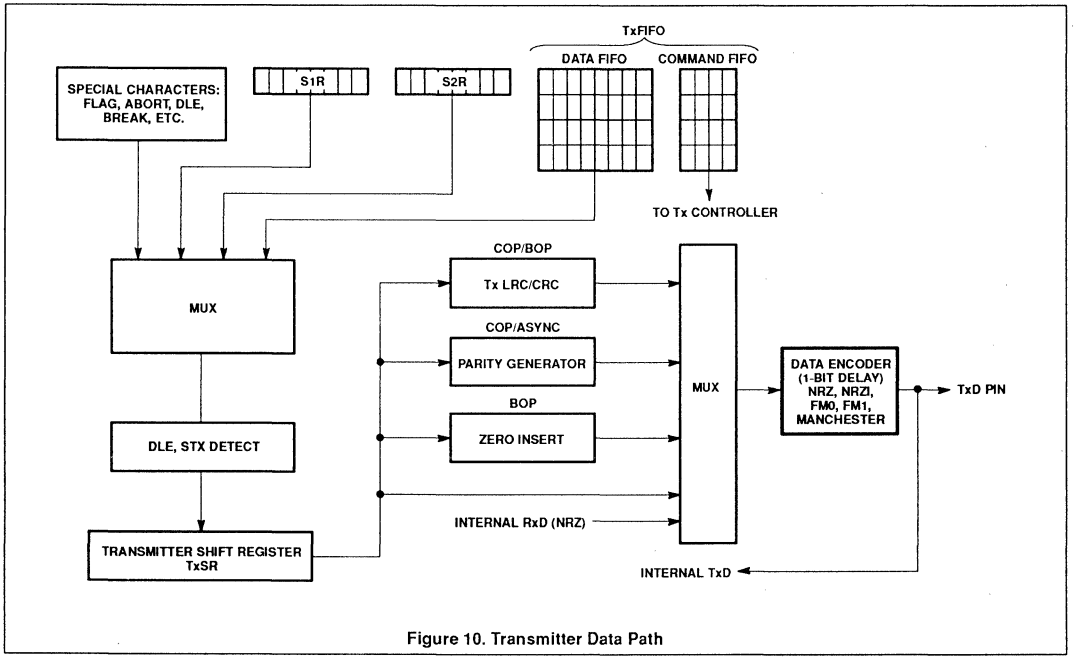


Figure 10. Transmitter Data Path

The transmitter sends either marks or FLAGs after the abort character(s) has been transmitted, depending on TPR[7:6]. Operation resumes with the transmission of a FLAG when a TSOM command is invoked. A TSOMP command is ignored unless the transmitter is disabled and then reenabled.

CRC accumulation can be specified in all BP modes. The type of CRC is specified via CMR2[2:0], and is normally selected as CRC-CCITT preset to ones, although any option is valid. Note that LRC8 option is not allowed in BOP modes.

The TSOM/TSOMP command sets the CRC accumulator to its initial state and accumulation begins with the first address octet after the initial FLAG(s). Accumulation stops when transmission of the first character of the FCS begins. The CPU can set the accumulator to its initial state prior to the transmission of any character by using the appended reset CRC command and can exclude any character from the accumulation by use of the exclude from CRC command, but these features would not normally be used in BOP modes. The CRC generator is also automatically initialized after the EOM or an ABORT are sent.

TxBOP Loop Mode

The loop modes are used by secondary stations on the loop, while the primary station operates in the BOP primary mode. Both the transmitter and receiver must be enabled and should be programmed to use the same clock source. Loop operation is initiated by issuing the 'go on-loop' command. The receiver looks for the receipt of seven contiguous ones and then asserts the LCN output to cause external loop control hardware to put the DUSCC into the loop, with the TxD output echoing the RxD input with a 2-bit time delay. The echoing process continues until a Go Active on Poll (GAP) command is invoked. The DUSCC then looks for receipt of an EOP bit pattern (a zero followed by seven ones, 11111110) and changes the last one of the EOP into a zero making it an opening FLAG. Loop sending (TRSR[6]) is asserted at that same time. The action of the transmitter after sending the initial FLAG depends on the status of the transmit FIFO.

If the transmit FIFO is not empty, a normal frame transmission begins. The operation is then similar to normal BOP operation with the following differences:

1. An ABORT command, an underrun, or receipt of the turnaround sequence (H'00') or FLAG cause the transmitter to cease operation and to revert to echoing the RxD input with a 2-bit time delay. A new transmission cannot begin until the GAP command is reinvoked and a new EOP sequence is received.
2. Subsequent to sending the EOM sequence of FCS-FLAG, the DUSCC examines the internal GAP flip-flop. If it is not set (having been reset by the 'reset GAP' command, the DUSCC reverts to echoing the received data. If the internal GAP flip-flop is still set, transmission of a new frame begins, with the user having control of sending multiple FLAGs between frames by use of the 'send SOM' command. If the FIFO is empty at this time, the DUSCC continues to send FLAGs until the data is loaded into the FIFO or until GAP is reset. If the latter occurs, it reverts to echoing RxD.

   When the DUSCC reverts to echoing RxD in any of the above cases, the last transmitted zero and seven ones will form an EOP for the next station down the loop.

   If the TxFIFO is empty when the EOP is recognized, the transmitter continues to send FLAGs until there is data in the FIFO. If a turnaround sequence or the reset GAP command is received before the FIFO is loaded, the transmitter switches to echoing RxD without any data transmission. Otherwise a frame transmission begins as above when a character is loaded into the FIFO. The mechanism provides time for the CPU to examine the received frame (the frame preceding the EOP) to determine if it should respond or not, while holding its option to initiate a transmission.

Termination of operation in the loop mode should be accomplished by use of the 'go off-loop' command. When the command is invoked, the DUSCC looks for the receipt of eight contiguous ones. It then negates the LCN output to cause the external loop control hardware to remove the DUSCC from the loop without affecting operation of other units remaining on the loop.

RECEIVER

The receiver data path includes two 9-bit holding registers, HSRH and HSRL, an 8-bit character comparison register, CCSR, two synchronizing flip-flops, a receiver shift register, RxST, the programmable SYN comparison registers, S1R and S2R, and BISYNC character comparison logic. The DUSCC configures the circuitry and utilizes it according to the operational mode selected for the channel through the two mode registers CMR1 and CMR2. For all data paths, character data is assembled according to the character bit count, in the RxSR, and is moved to the RxFIFO with any appended statuses when assembly is completed. Figure 1 depicts the four data paths created in the DUSCC for the previous protocols.

Receiver RxFIFO, RxRDY

The receiver converts received serial data on RxD (LSB first) into parallel data according to the transmission format programmed. Data is shifted through a synchronizing flip-flop and one or more shift registers, the last of which is the 8-bit receiver shift register (RxST). Bits are shifted into the RxSR on the rising edge of each 1X receive clock until the LSB is in RxSR[0]. Hence, the received character is right justified, with all unused bits in the RxSR cleared to zero. A receive character length counter generates a character boundary signal for synchronization of character assembly, character comparisons, break detection (ASYNC), and RxSR to RxFIFO transfers (except for BOP residual characters). During COP and BOP hunt phases, the SYN/GLAG comparison is made each receive bit time, as abort, and idle comparisons in BOP modes.

An internal clock from the BRG, the DPLL or the counter/timer, or an external 1X or 16X clock may be used as the receiver clock in ASYNC mode. The BRG or counter/timer cannot be used directly for the receiver clock in synchronous modes, since these modes require a 1X receive clock that is in phase with the received data. This clock may come externally from the RTxC or TRxC pins, or it may be derived internally from the DPLL. Received data is internally converted to NRZ format for the receiver circuits by using clock pulses generated by the DPLL.

When a complete character has been assembled in the RxSR, it is loaded into the receive FIFO with appended status bits. The most significant data bits of the character are set to zero if the character length is less than eight bits. In ASYNC and COP modes the user may select, via RPR[3], whether the data transferred to the FIFO includes the received parity bit or not. The receiver indicates to the CPU or DMA controller that it has data in the FIFO by asserting the channel's RxRDY status bit (GSR[4] or GSR[0] and, if in DMA mode, the corresponding receiver DMA request pin.

The RxFIFO consists of four 8-bit holding registers with appended status bits for character count complete indications (all modes), character compare indication (ASYNC), EOM indication (BISYNC/BOP), and parity, framing, and CRC errors. Data is loaded into the RxFIFO from the RxSR and extracted (read) by the CPU or DMA controller via the data bus. AN RxFIFO read create an empty RxFIFO position for new data from the RxSR.

RxRDY assertion depends on the state of OMR[3]:

1. If OMR[3] is 0 (FIFO not empty), RxRDY is asserted each time a character is transferred form the receive shift register to the receive FIFO. If it is not reset by the CPU, RxRDY remains asserted until the receive FIFO becomes empty, at which time it is automatically negated. If it is reset by the CPU, it will remain negated, regardless of the current state of the receive FIFO, until a new character is transferred from the RxSR to the RxFIFO.
2. If OMR[3] is 1 (FIFO full), RxRDY is asserted:

a. When a character transfer from the receive shift register to the receive FIFO causes it to become full.

b. When a character with a tagged EOM status bit is loaded into the FIFO (BISYNC or BOP) regardless of RxFIFO full condition.

c. When the counter/timer is programmed to count received characters and the character which causes it to reach zero count is loaded into the FIFO (ICTSR[6]).

d. When the beginning of break is detected in ASYNC mode regardless of the RxFIFO full condition.

If it is not reset by the CPU, RxRDY remains asserted until the FIFO becomes empty, at which time it is automatically negated. If it is reset by the CPU, it will remain negated regardless of the current state of the receive FIFO, until it is asserted again due to one of the above conditions.

The assertion of RxRDY causes an interrupt to be generated if IER[4] and the channel's master interrupt enable (ICR[0] or ICR[1]) are asserted.

When DMA operation is programmed, the RxRDY status bit is routed to the DMA control circuitry for use as the channel receiver DMA request. Assertion of RxRDY results in assertion of RTxDRQN output.

Several status bits are appended to each character in the RxFIFO. When the FIFO is read, causing it to be 'popped', the status bits associated with the new character at the top of the RxFIFO are logically ORed into the RSR. Therefore, the user should read RSR before reading the RxFIFO in response to RxRDY activation. If character-by character status is desired, the RSR should be read and cleared each time a new character is received. The user may elect to accumulate status over several characters or over a frame by clearing RSR at appropriate times. This mode would normally also be used when operating in DMA mode. If the RxFIFO is empty when a read is attempted, and wait mode as specified in CMR2[5:3], is not being used, a H'FF' is output on the data bus.

In all modes, the DUSCC protects the contents of the FIFO and the RxSR from overrun. If a character is received while in FIFO is full and a character is already in the RxSR waiting to be transferred into the FIFO, the overrunning character is discarded and the OVERRUN status bit (RSR[5]) is asserted. If the overruning character is an end-of-message character, the character is lost but the FIFOed EOM status bit will be asserted when the character in the RxSR is loaded into the FIFO.

Operation of the receiver is controlled by the enable receiver command. When this command is issued, the DUSCC goes into the search for start bit state (ASYNC), search for SYN state (COP modes), or search for FLAG state (BOP modes). When the disable receiver command is issued, the receiver ceases operation immediately. The RxFIFO is cleared on master reset, or by a rest receiver command. However, disabling the receiver does not affect the RxFIFO, RxRDY, or DMA request operation.

Receiver DCD and RTS Controls

If DCD enable Rx, RPR[2], is asserted, the DCD input must be asserted and the sampling circuit detects that the DCD input has been negated, the receiver ceases operation immediately. Operation resumes when the sampled DCD is asserted again. A change of state detector is provided on the DCD input of each channel. The required duration of the DCD level change is described in the discussion of ICTSR[5]. The user may program a change of state to cause an interrupt to be generated (master interrupt enable ICR[0] or [1] and IER[7] must be set) so that appropriate action can be taken.

In ASYNC mode, RPR[4] can be programmed to control the deactivation of the RTSN output by the receiver. RTSN can be manually asserted and negated by writing to OMR[0]. However, the assertion of RPR[4] causes RTS to be negated automatically upon receipt of a valid start bit if the channel's receive FIFO is already full. When this occurs, the RTSN negated status bit, RSR[6], is set. This may be used as a flow control feature to prevent overrun in the receiver by using the RTSN output signal to control the CTSN input of the remote transmitter. The new character will be assembled in the RxSR, but its transfer to the FIFO will be delayed until the CPU reads the FIFO, making the FIFO position available for the new character.

Once enabled, receiver operation depends on channel protocol mode. The following describes the receiver operation for the various protocols.

RxASYNC Mode

When first enabled, the receiver goes into the search for start bit state, looking for a High-to-Low (mark-to-space) transition of the start bit on the RxD input. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 71/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again.

If RxD is still Low, a valid start bit assumed and the receiver continues to sample the input at one bit time intervals (16 periods of the 16X Rx clock; one period of the 1X Rx clock) at the theoretical center of the bit, until the proper number of data bits and the parity bit (if specified) have been assembled, and the first stop bit has been detected.

The assembled character is then transferred to the RxFIFO with appended parity error (if parity is specified) and framing error status bits. The DUSCC can be programmed to compare this character to the contents of S1R. The appended character compare status bit, RSR[7], is set if the data matches and there is no parity error.

After the stop bit is sampled, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e., framing error) and RxD remains Low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

If a break condition is detected (RxD Low for entire character time including optional parity and first stop bit), only one character consisting of all zeros will be loaded into the RxFIFO and break start detect, RSR[2], will be set. The RxD input must return to a High condition for at least one half of a bit time (16X clock mode) or for one bit time (1X clock mode) before the break condition is terminated and the search for the next start bit begins. At that time, the break end detect condition, RSR[3], is set. Note that the maximum speed in the receiver when in asynchronous mode must not exceed 2Mbs.

Rx COP Modes

When the receiver is enabled in COP modes, it first goes into the SYN hunt phase, testing the received data each bit time for receipt of the appropriate SYN bit pattern, Plus parity if specified, to establish character boundaries. Receipt of the SYN bit pattern terminates hunt phase and places the receive in the data phase, in which all leading SYNs are stripped and the RxFIFO begins to load starting with the first non-SYN character. In COP single SYN protocol mode, S1R contains the SYN character required to establish character synchronization. In COP dual SYN and BISYNC protocol modes, S1R and S2R contain the first and second SYN characters, respectively, required to

establish character synchronization. The SYN character length is the same as the character length programmed in RPR[1:0], plus the parity bit if parity is specified. SYN characters received with a parity error, when parity is specified, are considered invalid and will not cause synchronization to be achieved.

In COP mode, resetting the receiver clears the receiver data path, while disabling the receiver does not. If not reset, partial sync patterns remaining in the receiver will be recognized when it is enabled.

If external synchronization is programmed (RPR[4] = 1), the internal SYN detection and special character recognition logic are disabled and receipt of SYN characters is not required. A pulse on the SYNI input pin will establish character synchronization and terminate hunt phase. The SYNI pin is ignored after the first input on the SYNIN pin is received. The receiver must be disabled and then reenabled to resynchronize or to return to normal mode. This must be programmed in conjunction with CMR1[2:0] = 110. Refer to the description of RPR[4] for further details

The SYN detect status bit RSR[2], is set whenever SYN1, SYN1-SYN2, or DLE-SYN1 is detected for single SYN, dual SYN/BISYNC normal, and BISYNC transparent modes, respectively, and the SYNOUT pin will go active for one receive clock period one bit time after SYN detection in HSRH/HSRL. After character sync has been attained, the receiver enters the data phase and assembles characters in the RxSR, beginning with the first non-SYN character, with the least significant bit received first. It computes the BCC if specified, checks parity if specified, and checks for overrun errors.

The operation of the BCC (CRC/LRC) logic depends on the particular COP mode in use. The BCC is initialized upon first entering the data phase. For non-BISYNC modes, all received characters after entering data phase are included in the BCC computation, except for leading SYNs and SYNs which are specified to be stripped by RPR[7]. As each received character is transferred from the RxSR to the FIFO, the current value of the BCC characters is checked and the CRC ERROR status bit (RSR[1]) is set if the value of the CRC remainder is not the expected value. RSR[1] gets set when the character reaches the top of the FIFO. The EOM status bit, RSR[7], is not set since there is no defined end-of-message character. The receiver computes the BCC for test messages automatically when operating in BISYNC protocol mode.

BISYNC Features

The DUSCC provides support for both BISYNC normal and transparent operations. The following summarizes the features provided. Both EBCDIC and ASCII text messages can be handled by the DUSCC as selected by CMR1[5]. The receiver has the capability of recognizing special characters for the BISYNC protocol mode (see Table 15).

All sequences in Table 15, except SOH and STX, when detected explicitly cause a status to be affected. The following describes the conditions when this occurs.

The first character received when entering data phase for a header or text message should be an SOH, an STX, or a DLE-STX two-character sequence. Receipt of any of these initializes the CRC generator and starts the CRC accumulation. The SOH places the receiver in header mode, receipt of the STX places it in text mode, the receipt of the DLE-STX sequence (at any time) automatically places the receiver in transparent mode and sets the XPNT mode status bit, TRSR[0]. There is no explicit status associated with SOH and STX. If any characters are received when entering the data phase, the message is treated as a control message and will not be accumulated in CRC.

After the data phase is established, the receiver searches the data stream for an end of message control character(s):

Header field: ENQ, ETB, or ITB

Normal text field: ENQ, ETX, ETB, or ITB

Transparent text field: DLE-ENQ, DLE-ETX, DLE-ETB, or DLE-ITB

Control message field: EOT, NAK, ACK0, ACK1, WACK, RVI or TTD

Detection of any one of these sequences causes the EOM status bit, RSR[7], to be set. Also if RPR[5] is set and the receiver does not detect a closing PAD (four 1's) after the 'EOT' or 'NAK', the PAD error status bit, RSR[6], is set. When the abort sequence ENQ or DLE-ENQ is detected, the character is tagged with an EOM status and transferred to the FIFO, but the appended CRC error status bit should be ignored. For the other EOM control sequences, the receiver waits for the next two bytes (the CRC bytes) to be received, checks the value of the CRC generator, and tags the transferred character with a CRC error, RSR[1], if the CRC remainder is not correct. See Figure 11 for an example of BCC accumulation in various BISYNC messages.

The CRC bytes are normally not transferred to the FIFO, unless the transfer FCS to FIFO control bit, RPR[6], is asserted. In this case the EOM and CRC error status bits will be tagged onto the last byte of the last FCS byte instead of to the last character of the message. After detecting one of the End-Of-Message (EOM) character sequences and setting RSR[7], the receiver automatically goes into auto hunt mode for the SYNC characters and PAD check if RPR[5] is set.

SYN Pattern Stripping

Leading SYNs (before a message) are always stripped and excluded from the FCS, but SYN patterns within a message are treated by the receiver according to the RPR[7] bit. SYN character patterns are defined for the various COP modes as follows:

COP single SYN mode — SYN1

COP dual SYN mode — SYN1, and SYN2 when immediately preceded by SYN1.

BISYNC normal mode — SYN1, and SYN2 when immediately preceded by SYN1. SYN1 is always stripped, even if it is not followed by SYN2 when stripping is selected.

BISYNC transparent mode — DLE-SYN1, where the DLE is the last of an odd number of consecutive DLEs.

0 Strip only RPR[7] leading the SYN and do not accumulate in FCS.

1 Strip all SYNs. Additionally, strip odd DLEs when operating in BISYNC transparent mode. Do not accumulate stripped characters in FCS.

Processing of the SYN patterns is determined by the RPR[7] bit, the COP mode, and the position of the pattern in the frame. This is summarized in Table 16.

The value of the RPR[7] field does not affect the setting of the SYN DETECT status bit, RSR[2], and the generation of a SYNOUT pulse when a SYN pattern is received.

RxBOP Mode

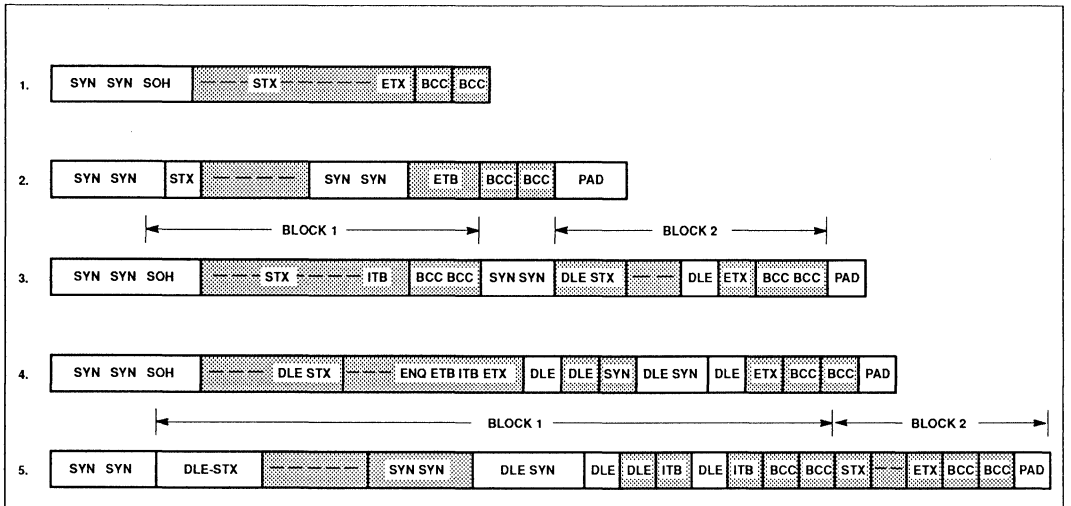
In BOP protocol mode, the receiver may be in any one of four phases: hunt phase, address field (A) phase, control field (C) phase, or information field (I) phase. The character length for the A and C phases is always 8 bits. The I field character length is specified in RPR[1:0].

Note that if the residual character length is not zero, the unused most significant bits in the receiver FIFO are not necessarily zero. the unused bits should be ignored, this will not cause a CRC error.

After an enable receiver command is executed, the receiver enters hunt phase, in which a comparison for the string (01111110) is done every Rx bit time. The FLAG delineates the beginning (and end) of a received frame and establishes the character boundary. Each FLAG match in CCSR causes the FLAG detect status bit (RSR[2]) to be set and SYNOUTN pin to be activated one bit time later for one receive clock period. FLAGs with an overlapping zero will be detected. All FLAGs are deleted from the data stream.

Table 15. BISYNC Features

BISYNC — Single-Character Sequences			
Sequences	**ASCII**	**EBCDIC**	**Description**
SOH	H'01'	H'01'	Start of header
STX	H'02'	H'02'	Start of text
ETX	H'83'	H'03'	End of text
EOT	H'04'	H'37'	End of transmission
ENQ	H'85'	H'2D'	Enquiry
DLE	H'10'	H'10'	Data link escape
NAK	H'15'	H'3D'	Negative ack
ETB	H'97'	H'26'	End of transmission block
ITB	H'1F'	H'1F'	End of intermediate transmission block
BISYNC — Two-Character Sequences			
Sequence	**ASCII**	**EBCDIC**	**Description**
ACK0	H'10,B0'	H'10,70'	Acknowledge 0
ACK1	H'10,31'	H'10,61'	Acknowledge 1
WACK	H'10,3B'	H'10,6B'	Wait before transmit positive ack
RVI	H'10,BC'	H'10,7C'	Reverse interrupt
TTD	H'02,85'	H'02,2D'	Temporary text delay
BISYNC — (Transparent Text Mode) — Two-Character Sequences			
Sequence	**ASCII**	**EBCDIC**	**Description**
DLE-ENQ	H'10,85'	H'10,2D'	Enquiry
DLE-ITB	H'10,1F'	H'10,1F'	End of intermediate transmission block
DLE-ETB	H'10,97'	H'10,26'	End of transmission block
DLE-ETX	H'10,83'	H'10,03'	End of text
DLE-STX	H'10,02'	H'10,02'	Start of transparent text mode



NOTES:
The BCC accumulator is stopped after the end of message character sequence is accumulated. All shaded areas are accumulated.
ENQ (DLE - ENQ) in a text message should be treated as an abort.
Opening SYNs will be stripped by the receiver.

Figure 11. Example of BCC Accumulation in Various BISYNC Messages

Table 16. SYN Pattern Processing

MODE	RPR [7]	LEADING SYNs	WITHIN A MESSAGE
BISYNC	0	no FCS no FIFO	no FCS Pattern into FIFO
	1	no FCS no FIFO	no FCS no FIFO
COP	0	no FCS no FIFO	Accumulate in FCS Pattern into FIFO
	1	no FCS no FIFO	no FCS no FIFO

Once a FLAG has been detected, the receiver will exit hunt phase and enter address phase. The handling of the address field is determined by the values programmed in CMR1[2:0], which selects one of the BOP modes. The BOP secondary address modes are selected by CMR1[4:3] and function as in the description that follows.

Single-Octet Address

For receive, the address comparison for a secondary station is made on the first octet following the opening FLAG. A match occurs if the first octet after the FLAG matches occurs if the first octet after the FLAG matches the contents of S1R, or if all parties address (RPR[3]) is asserted and the first octet is equal to H'FF'.

Dual Octet Address

For receive, the address comparison for a secondary station is made on the first two octets following the opening FLAG.

A match occurs if the first two octets after the FLAG match the contents of S1R and S2R respectively, or if all parties address (RPR[3]) is asserted and the first two octets are equal to H'FF, FF'.

Dual Address with Group Mode

For receive, the address comparison for a secondary station is made on the first two octets following the opening FLAG. A match occurs for one of three possible conditions. If the first two octets after the FLAG match the contents of S1R and S2R, respectively, or if the first octet is H'FF' and the second matches the contents of S2R (group mode), or when all parties address (RPR[3]) is asserted and the first two octets are equal to H'FF,FF'. The second condition (group mode) allows a selected group of stations to receive a message.

Extended Address Mode

Extend address field to the next octet if the LSB of the current address octet is zero. Address field is terminated if the LSB of the address is a one. The address field will be terminated after the first octet if the null address H'00' is received/transmitted as the first address octet. For this mode the receiver does not perform an address comparison (all received characters after the opening FLAG are transferred to the FIFO) but does determine when the address field is terminated.

The length of the A field may be a single octet, a dual octet, or more octets, as described above. A primary station or an extended address secondary station does not perform an address comparison, and all characters in the A, C, and I fields after the flag are transferred to the FIFO. Although address field comparisons are not performed, the length of the address field is still determined by CMR1[4:3]. For the other secondary address modes, if there is a match, or the received character(s) match either of the other enabling conditions (group or all-parties address), all characters in the A, C, and I field are transferred to the FIFO. If there is no match, the receiver returns to the FLAG hunt phase.

C phase begins after A phase is terminated. The receiver receives one or two control characters, CMR1[5]. After this phase is terminated, the character length is switched automatically from 8 bits to the number of bits specified in RPR[1:0] and the information field phase is entered.

The frame is terminated when a closing FLAG is detected. The same FLAG can also serve as the opening FLAG of the next frame. The 16 bits received prior to the closing FLAG form the frame check sequence (if an FCS is specified in CMR2[2:0]). All non-FLAG characters of the frame are accumulated in the CRC checker and the result is compared to the expected remainder. Failure to match will cause a CRC error. EOM detect RSR[7], RCL not zero RSR[0], and CRC error RSR[1] are normally FIFOed with the last character of the I field. RCL not zero RSR[0] is set if the length of the last character of the I field does not have the length programmed in RPR[1:0]. The residual character length in TRSR[2:0] is also valid at that time. The CRC characters themselves are normally not passed to the RxFIFO. However, if the transfer FCS to FIFO control bit RPR[6] is asserted, the FCS bytes will be transferred to the FIFO. In this case the EOM, CRC error, and RCL not zero status bits will be tagged onto the last byte of the CRC sequence instead of to the last character of the message.

If the closing FLAG is received prior to receipt of the appropriate number of A field, C field as programmed in CMR1[5:3], and FCS field octets, a short frame will be detected and RSR[4] will be set. The I field need not be present in a valid frame. An abort (11111110) comparison is done after an opening FLAG has been received and up to receipt of the closing FLAG. A match causes the abort detect status bit (RSR[6]) to be set. The receiver then enters FLAG search mode. The abort is stripped from the received data stream.

If a zero followed by 15 contiguous ones is detected, the idle detect status bit RSR[3] is set. This comparison is done whenever the receiver is enabled. Therefore, it can occur before or after a received frame.

Zero deletion is performed during BOP receive. A zero after 5 contiguous ones is deleted from the data stream regardless of character boundaries. Deleted zeros are not subject to CRC accumulation. FLAG, ABORT, and IDLE comparisons are done prior to zero deletion.

If external synchronization is programmed (RPR[4] - 1), the internal FLAG detection and address comparison logic is disabled and receipt of FLAGs is not required. In this arrangement, a pulse on the SYNI-N input pin will establish synchronization and terminate hunt phase. The receiver will then go immediately into the I-field mode with zero deletion disabled, assembling and transferring characters into the FIFO with the character length specified in RPR[1:)]. The SYNI-N pin is ignored after the first input on the SYNI-N pin is received. The receiver must be disabled and then reenabled to resynchronize or to return to normal operating mode.

This mode must be programmed in conjunction with CMR1[2:0] = 110. Refer to the description of RPR[4] for further details.

BOP Loop Mode

Operation of the receiver in BOP loop protocol mode is similar to operation in other BOP modes, except that only certain frame formats are supported. Several character detection functions that interact with the operation of the transmitter commands are added:

1. When the 'go on-loop' command is invoked, the receiver looks for the receipt of a zero followed by seven ones and then asserts the LCN output.
2. When the 'go off-loop' command is invoked, the receiver looks for the receipt of eight contiguous ones and then negates the LCN output.
3. The TxD output normally echoes the receive input with a two bit time delay. When the 'go active on poll' command is asserted, the receiver looks for an EOP (a zero followed by seven ones) and then switches the TxD output line to the normal transmitter output. Receipt of an EOP or an ABORT sets RSR[6].
4. Receipt of a turnaround sequence (eight contiguous zeros) terminates the transmitter operation, if any, and returns the TxD output to echoing the RxD input. RSR[3] is set if a turnaround is received.

See transmitter operation for additional details.

SUMMARY OF COP FEATURES

COP Dual SYN Mode	
SYN detect	SYN1-SYN2
Linefill	SYN1-SYN2
SYN stripping	SYN1-SYN2 used to establish character sync, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 and SYN1-SYN2 if stripping is specified by RPR[7].
Excluded form FCS**	SYN1 and SYN1-SYN2 before beginning of message, i.e., leading SYNs and, if SYN stripping is specified by RPR[7] anywhere else in the message for the Rx; linefill SYN1-SYN2 for Tx regardless of RPR[7]. (If SYN stripping is not specified, then SYNs within a message will be included in FCS by Rx.)
BISYNC normal mode	
SYN detect	SYN1-SYN2
Linefill	FYN1-SYN2
SYN stripping	SYN1-SYN2 used to establish character sync, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 and SYN1-SYN2 if stripping is specified by RPR[7].
Excluded from FCS	All SYNs either before or within a message, regardless of RPR[7], plus additional characters as required by the protocol.
BISYNC transparent mode	
SYN detect	*DLE-SYN1
Linefill	*DLE-SYN1
SYN/DLE stripping	*DLE-SYN1 and odd DLEs if stripping is specified by RPR[7].
Excluded from FCS	*DLE-SYN1 and odd DLEs, regardless of RPR[7] plus additional characters as required by the protocol.
COP single SYN mode	
SYN detect	SYN1
Linefill	SYN1
SYN stripping	SYN1 used to establish character sync, i.e., leading SYNs. Subsequent to this, SYN1 if stripping is specified by RPR[7].
Excluded from FCS**	SYN1 before beginning of message, i.e., leading SYNs, and if SYN stripping is specified by RPR[7], anywhere else in the message for the Rx; linefill SYN1 for Tx regardless of RPR[7]. (If SYN stripping is not specified, then SYNs within a message will be included in FCS by Rx.)

NOTES:

* DLE indicates last DLE of an odd number of consecutive DLEs.

** In non-BISYNC COP modes (single or dual SYN case), if SYN stripping is off, i.e., RPR[7] = 0, then SYNs within a message will be included in FCS by receiver. Therefore, the remote DUSCC transmitter should be careful not to let the TxFIFO underrun since the linefill SYN characters are not accumulated in FCS by the transmitter regardless of RPR[7]. Letting the TxFIFO underrun will result in a CRC error in the receiver.

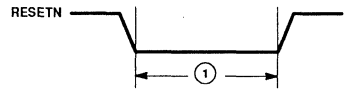


Figure 12. Reset Timing

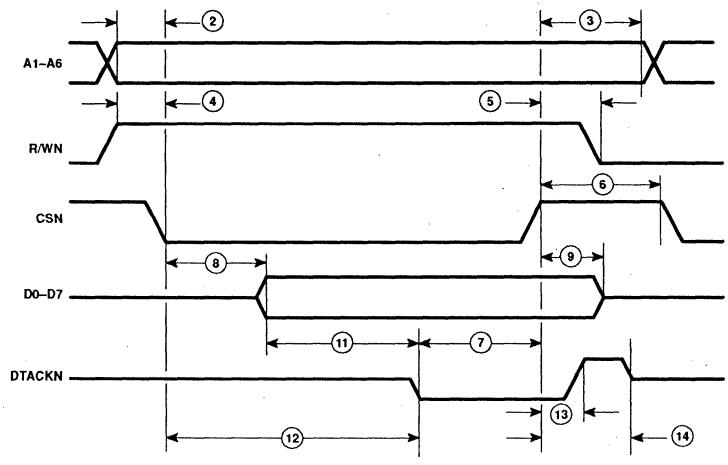


Figure 13. Bus Timing (Read Cycle)

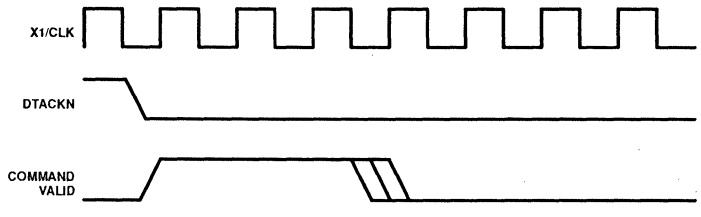


Figure 14. Command Timing

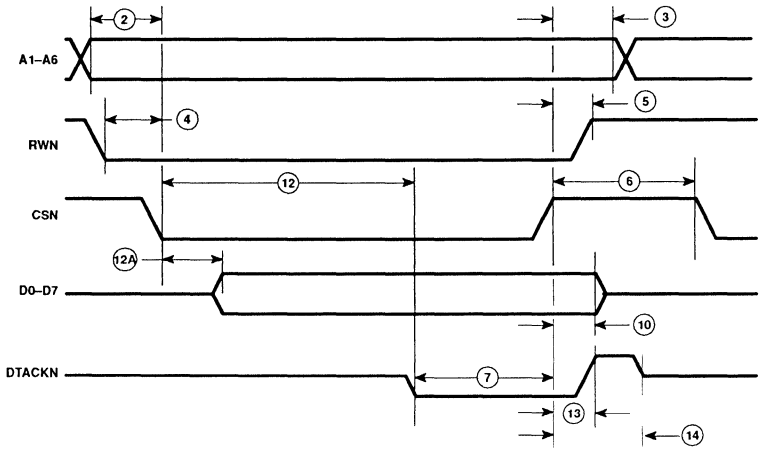


Figure 15. Bus Timing (Write Cycle)

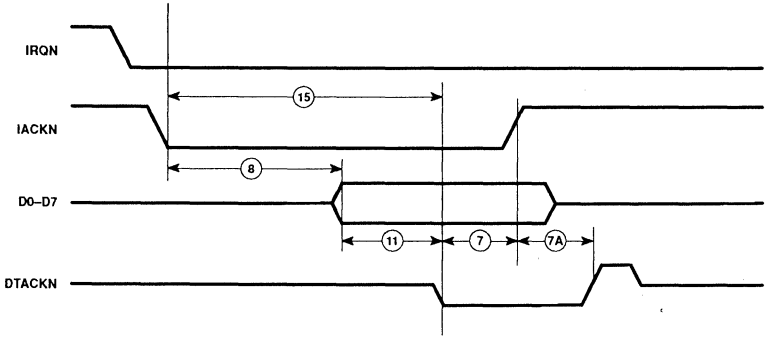


Figure 16. Interrupt Cycle Timing

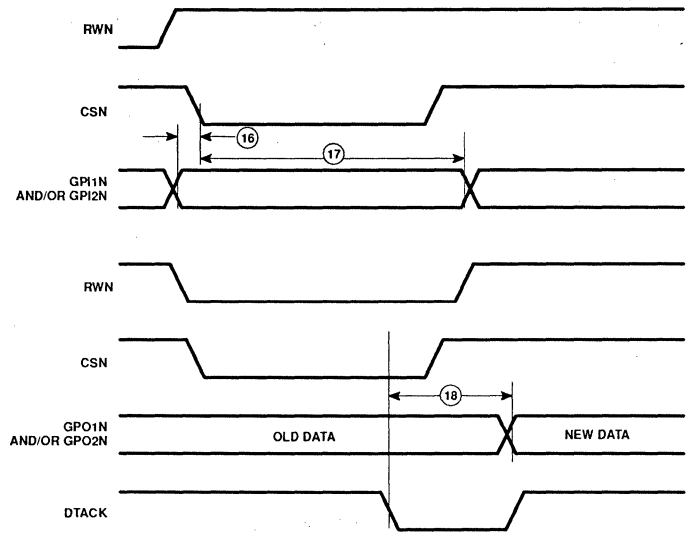


Figure 17. Port Timing

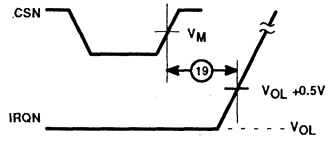


Figure 18. Interrupt Timing

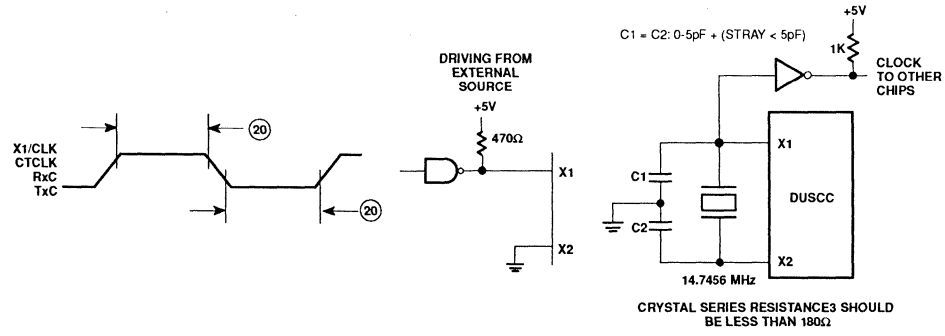


Figure 19. Clock Timing

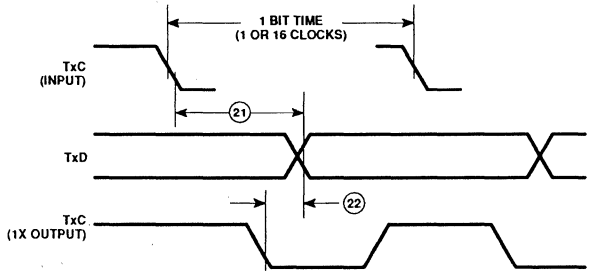


Figure 20. Transmit Timing

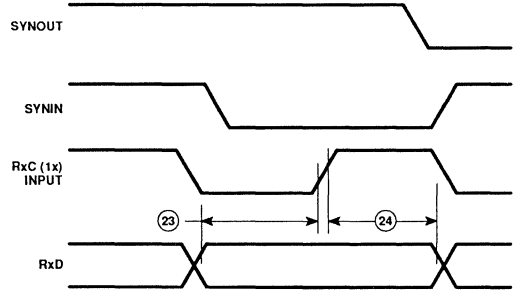


Figure 21. Receive Timing

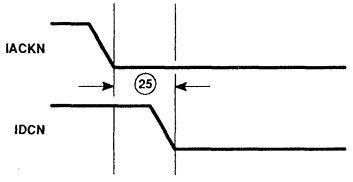


Figure 22. Interrupt Daisy Chain Timing

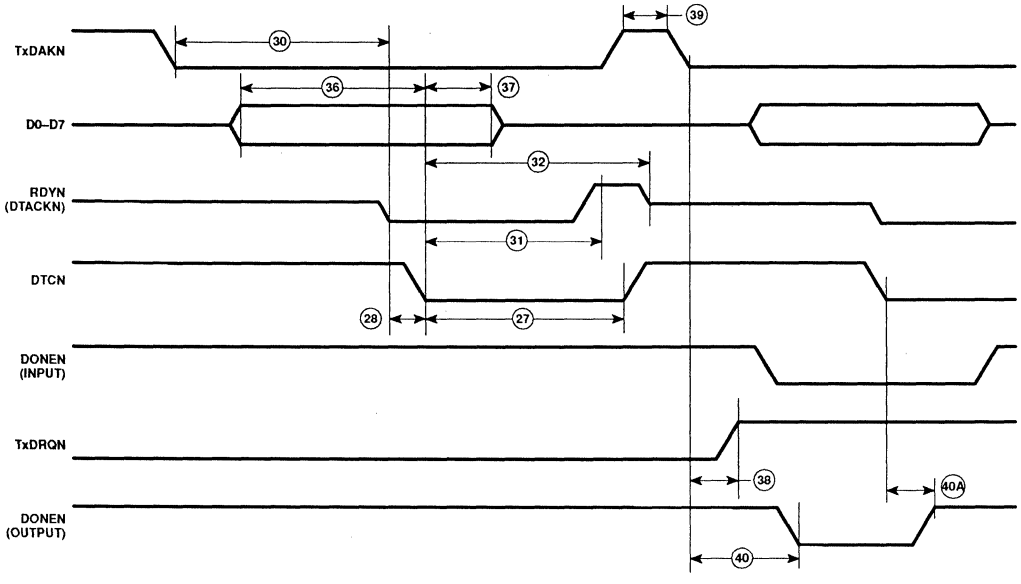


Figure 23. DMA Transmit Write Timing — Single Adress DMA Mode

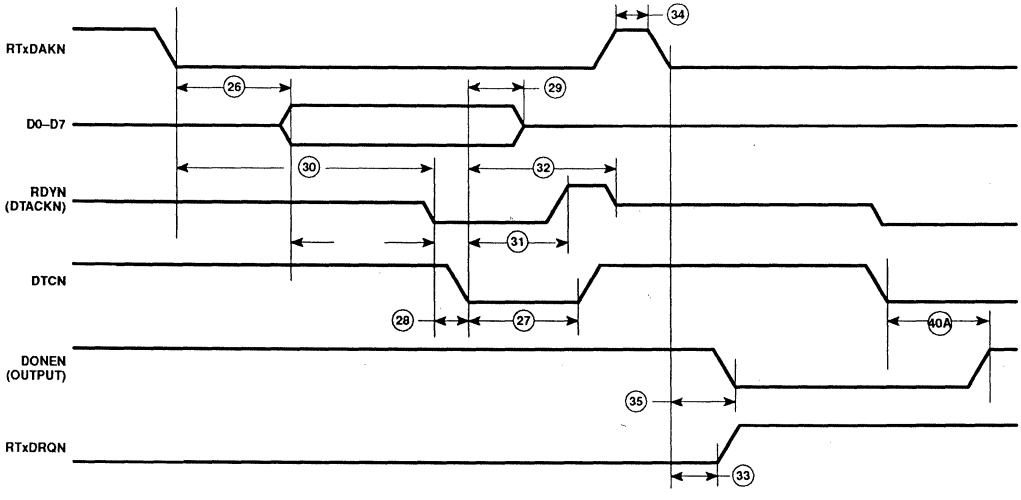


Figure 24. DMA Receiver Read Timing — Single Address DMA Mode

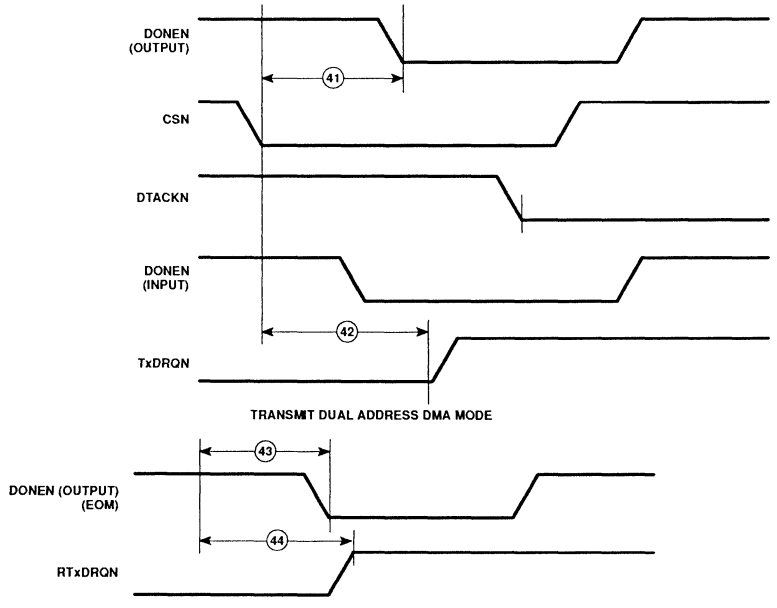


Figure 25. Dual Address DMA Mode Timing

Philips Components–Signetics

Document No.	
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Date of Issue	November 1989
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Data Communication Products	

SC26C460

Input/output processor (IOP)

DESCRIPTION

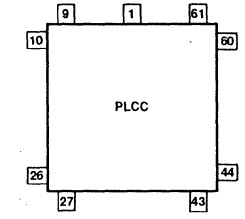
The Signetics SC26C460 I/O Processor (IOP) is a 32-channel Direct Memory Access (DMA) processor that functions with external peripheral devices. The external peripheral devices used with the IOP do not have to be designed specifically for DMA use. The IOP is especially desirable for use with multi-channel peripherals such as the Signetics 2698 OCTART.

The SC26C460 stores and fetches binary data with the least significant byte at the lowest-addressed memory or I/O location. This arrangement is similar to the Intel processors.

FEATURES

- 32 channel DMA processor
- Separate memory address and length for each channel
- Separate I/O device address for each channel
- Separate channel program entry point for each channel
- Programmable to handle virtually all types of peripherals
- Custom instruction set
- Can interpret peripheral status for channel selection, error checking
- Can interpret data characters for buffer termination checking, control sequence transformation
- 8- or 16-bit data transfers
- 24-bit memory addresses: 16Mbyte address space
- 2-level interrupt queue minimizes host microprocessor overhead
- High-speed CMOS technology
- 68-pin PLCC

PIN CONFIGURATION



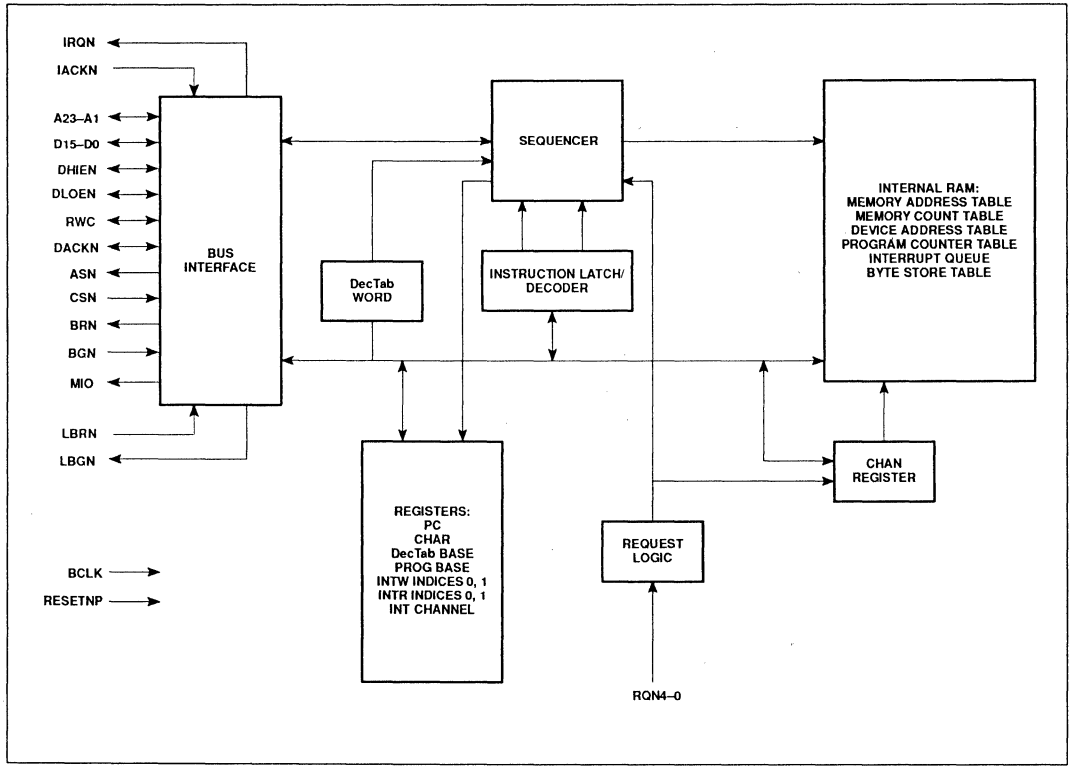
Pin	Function	Pin	Function
1	D10	35	A21
2	D9	36	V_{SS}
3	D8	37	A20
4	D7	38	A19
5	D6	39	A18
6	D5	40	A17
7	D4	41	A16
8	D3	42	A15
9	D2	43	A14
10	D1	44	A13
11	D0	45	A12
12	RQ0N	46	A11
13	RQ1N	47	V_{SS}
14	RQ2N	48	A10
15	RQ3N	49	A9
16	RQ4N	50	A8
17	BRN	51	A7
18	V_{SS}	52	A6
19	V_{CC}	53	V_{SS}
20	BGN	54	V_{CC}
21	LBRN	55	A5
22	IRQN	56	A4
23	IACKN	57	A3
24	CSN	58	A2
25	V_{SS}	59	A1
26	LBGN	60	D15
27	DACKN	61	D14
28	MIO	62	D13
29	RWC	63	D12
30	DHIEN	64	D11
31	DLOEN	65	V_{SS}
32	ASN	66	BCLK
33	A23	67	RESETNP
34	A22	68	V_{CC}

I/O Processor (IOP) SC26C460

ORDERING INFORMATION

PACKAGE	V_{CC} = 5V ± 10%, T_A = 0°C to 70°C
Plastic PLCC	SC26C460A68

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
RQ4N–RQ0N	16–12	I	**Request Lines:** A set of active-low inputs from external peripheral devices handled by the IOP. Typically, these will be the "interrupt request" lines from the peripherals. If there are 5 peripheral lines or less, they can be directly connected to these pins. Otherwise, the lines must be externally encoded. The IOP interprets the "all high" state on these lines as "no request". These input request lines are internally synchronized. When the IOP is idle, and it detects the stable active state on these lines on two consecutive falling edges of BCLK, it begins activity for the indicated channel.
CSN	24	I	**Chip Select:** An active-low input indicating that the host MPU is trying to access a register or RAM location on the IOP. CSN is not asserted until all of the signals, A8–A1, DHIEN, DLOEN, and RWC are valid (this eliminates signalling differences among host MPUs). This, in turn, implies that in a system in which IOP has its own "local bus", CSN should be qualified with LBGN.
A23–A1	33–35, 37–46, 48, 49, 50–52, 55–59	O O O I/O I/O	**Address Lines:** When the IOP is a bus master, these lines carry the address to be accessed, which may be in memory or in a peripheral device. When the IOP is a bus slave, A8–A1 selects an internal location in the IOP to be read or written by the host MPU.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
D15–D0	60–64, 1–11	I/O	**Bidirectional Data Bus:** 16-bit data bus for the IOP, memory, peripherals, and the host MPU.
MIO	28	O	**Memory/Input-Output Control:** When the IOP is a bus master, this tri-state output is driven high to indicate an access to memory, and low to indicate an access to a peripheral device. MIO has the same timing as A23–A1. When the IOP is a bus slave, this output is tri-stated.
ASN	32	O	**Address Strobe:** When the IOP is bus master, this is an output indicating that a transfer cycle is in progress on the bus, and, in particular, that a valid address has been placed on A23–A1. This signal is not driven at other times.
DHIEN, DLOEN	30, 31	I/O	**Data High/Low Enable:** When the IOP is a bus master, theses pins are outputs. DHIEN low in a master read cycle indicates that the memory or peripheral selected by A23–A1 should read a byte and place its contents on D15–D8, while DLOEN low has the same meaning for the D7–D0 lines. In a master write cycle, DHIEN (DLOEN) low indicates that the IOP has placed valid data on D15–D8 (D7–D0), and that the memory or peripheral selected by A23–A1 should write the data into the appropriate byte(s). When both signals are low in a master cycle, a 16-bit word should be transferred. When the IOP is not a bus master, these lines are inputs from the host MPU. These two signals are internally ANDed. Either signal goes active, along with CSN active, will cause the IOP to be accessed.
RWC	29	I/O	**Read/Write Control:** When the IOP is a bus master, this output controls the direction of data transfer on D15–D0. On the IOP, this signal is high for a write and low for a read. and corresponds to W/$\overline{R}$ on the 80386 and to $\overline{ST}$ on the 80286. When the IOP is not the current bus master, RWC is an input from the host MPU, with the same meaning.
DACKN	27	I/O	**Data Acknowledge:** When the IOP is a bus master, this is an input signal from memory and peripherals, acknowledging that the requested bus transfer has been completed. When the IOP is a bus slave, this is an open-drain output to the host MPU, with the same meaning. This signal corresponds to $\overline{READY}$ on the 80236 and 80386.
BRN	17	O	**Bus Request:** An active-low totem-pole output to the host MPU or other bus arbiter, requesting the use of the MPU bus. It must be inverted to produce HOLD in an "Intel" system. BRN is not open-drain because if the host MPU is the arbiter and the IOP is the only other master, a totem-pole output eliminates the need for a pull-up resistor. Also, if there are other masters contending with the IOP for bus grants, the arbitration mechanism needs a separate request signal from each master to decide which one is to receive each grant.
BGN	20	I	**Bus Grant:** An active-low input from the host MPU or other arbiter, granting use of the MPU bus to the IOP. If there are no bus masters other than the IOP and host MPU, BGN can be inverted from the HLDA output of an Intel processor.
LBRN	21	I	**Local Bus Request:** An active-low input used in systems in which the MPU and IOP have separate buses, whereby the MPU can request access to the use of resources on the IOP's bus, including the IOP itself. It should be wired to a logic high in a system in which the MPU and IOP share the same bus. First MPU access to the IOP without asserting this signal will lock the IOP in one bus mode until reset.
LBGN	26	O	**Local Bus Grant:** LBGN is an active-low output by means of which the IOP responds to LBRN, and grants the host MPU access to resources on the IOP's bus.
IRQN	22	O	**Interrupt Request:** An active-low open-drain output to the host MPU, indicating that a channel program has requested an interrupt for one or more of the IOP channels. It must be inverted in an Intel style system. It requires an external pull-up resistor.
IACKN	23	I	**Interrupt Acknowledge:** An active-low input indicating the the host MPU is acknowledging the interrupt requested by IRQN. The IOP responds to the assertion of this signal by placing an interrupt vector on D7–D0, asserting DTACKN, and releasing IRQN if there is no further interrupt request for any channel.
BCLK	66	I	**Bus Clock:** The clock signal for the IOP.
RESETNP	67	I	**Master Reset:** Active-low reset for the IOP. Must be asserted at power-up; may be asserted at other times the system is to be reset and restarted.
V_{CC}	19, 54, 68	I	**Power**
V_{SS}	18, 25, 36, 47, 53, 65	I	**Ground**

FUNCTIONAL DESCRIPTION

Note that parenthesis around the name of a register or RAM location indicates "the contents of". The name of a RAM table, followed by the name of a register in brackets, indicates the location in the RAM table which is selected by indexing into it using the contents of the register as the index (e.g. PCT[CHAN]).

Programming Model

Figure 1 shows the IOP register map as it appears to the host microprocessor. The individual registers and RAMs in the map are described in the following sections. All registers/RAM location must be accessed in word.

Decision Table Base Register (DTBR)

This 11-bit register provides the high-order address bits when a decision table is read. The IOP can use up to 16 decision tables, each having 256 words (512 bytes). Decision tables reside in external memory that is 16 x 512 (8192) bytes size.

Program Counter Base Register (PCBR)

This 13-bit register provides the high-order address bits when fetching instructions from a channel program. All channel programs used by the IOP must reside in external memory that is 1024 words (2048 bytes) size.

Memory Address Table (MAT)

MAT is an on-chip RAM containing memory addresses. There is one 24-bit entry for each channel. In addition, in 2 bus systems in which the IOP has its own local bus separate from the host processor's bus, the bit position that would correspond to A31 is used to indicate whether the memory location in question is on the local bus or the system bus. Thus, the MAT is composed of 32 x 25 (800) bits of on-chip RAM.

Memory Count Table (MCT)

MCT is an on-chip RAM containing 14-bit length counts for the memory areas addressed by MAT, plus two bits defining whether 8- or 16-bit transfers should be done for the device and memory, respectively. There is one 16-bit entry for each channel. The MCT is composed of 32 x 16 (512) bits of on-chip RAM.

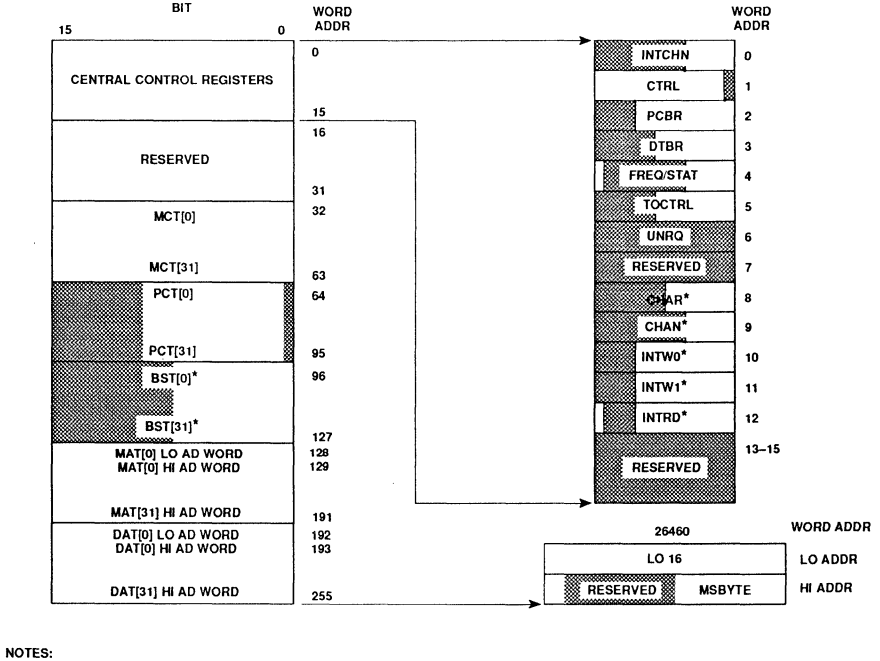
The two most significant bits of the words that the host processor writes and reads for MCT are flags defining whether the peripheral device for this channel has a data width of 8- or 16-bits, and whether data should be packed or unpacked between the device and the memory, as follows:

00 Byte device, byte memory transfers
01 Byte device, word memory transfers
10 Not allowed
11 Word device, word memory transfers

The packing feature can significantly decrease the traffic generated by the IOP on the host processor's bus, as described further in a subsequent section.

Device Address Table (DAT)

DAT is an on-chip RAM containing the address of each channel's device. There is one 24-bit entry for each channel. In addition, in systems in which the IOP has its own local bus separate from the host processor's bus, the bit position that would correspond to A31 is used to indicate whether the peripheral device in question is on the local bus or the system bus. The DAT is composed of 32 x 25 (800) bits of on-chip RAM.



NOTES:
*Host MPU software typically does not need to access to these registers/RAM locations.
▨ = Not implemented for writing and are read back as zeros.

Figure 1. IOP Register Map

Program Counter Table (PCT)
PCT is an on-chip RAM containing the location of the first instruction for each channel, The contents of a PCT entry are used relative to (concatenated below) the contents of PCBR. The PCT is composed of 32 x 10 (320) bits of on-chip RAM.

Byte Store Table (BST)
BST is an on-chip RAM that can store one data byte and one flag bit (BSTO flag) for each channel. This facility provides the packing and unpacking between a 16-bit memory and an 8-bit device.

CHAN Register
This 5-bit register is used as an index into MAT, MCT, DAT, and BST. When service is started for a channel, CHAN is loaded with a number derived from the request logic, and the contents of PCT[CHAN] becomes the starting point for execution. CHAN can thereafter be modified by the INTERP instruction.

TCHAN Register
This internal register is similar to CHAN and is used by the LDPCT and RELOAD instructions.

CTRL Register
This register is programmable by the host processor to control the basic operation of the IOP. Its contents are discussed in a later section.

CHAR Register
This 8-bit register is a temporary store for characters in transit between a device and memory, or for a status value from a device.

SVCHAR, SVBST Registers
These internal registers function as stores. They are accessible by some instructions.

Force/Status Register

F	0		CHANNEL
1	1	9	5

If the host MPU write this register with F = 1, the IOP will respond by executing instructions starting at the address in the PCT entry selected by the channel number written into the 5 low order bits of this register. It is done as if a request was asserted for the channel number. Writing this register with F = 0 will update previous writing with F = 1, if the forced request has not yet been revised.

If the IOP is already executing a channel program (or has already made an internal decision to do so) when the host MPU writes this register with F = 1, response will be delayed until after the channel program has ended. In any case, service for the channel written into this register has priority over starting new service in response to the RQn lines.

When the IOP begins service for the channel, it clears the F flag. If there is any possibility that the host MPU software might want to write another channel number for this register, before service for a previously written channel could be started, then the software must read this register and check for F = 0, before writing F = 1 and the new channel number.

Bit 14 of this register must be programmed with 0.

The Interrupt FIFO
The FIFO is used to maintain an interrupt queue for the host MPU. It includes 32 entries of 13 bits each, and can be programmed in the CTRL register to function as a single FIFO with 32 entries, or it can be divided into two FIFOs with 16 entries each, corresponding to two levels of interrupt priority.

INTCHN Register
INTCHN is a 5-bit read only register accessible to the host MPU, from which the number of the current (most recent) interrupting channel can be read. See description of the INT instruction.

INTRD
This read only register is an interrupt polling register. It can be read by MPU software at the end of servicing an IOP interrupt, to determine whether another interrupt is pending. The data read has the following format.

V		NEXT INTCHN	NEXT VECTOR
1	2	5	8

If V bit is 1, the other two fields are valid and are supplied from the interrupt FIFO. INTRD is also used for device testing.

INTW0, INTW1
These two write-only registers are used for device testing, and allow entries to be written into the interrupt FIFO. Both register locations have the format:

	INTCHN	VECTOR
3	5	8

If the nL bit in the CTRL register is 0, indicating a signal-level interrupt queue, writing either register places the data in the 32-entry FIFO. If the nL bit is 1, writing INTW0 puts data in the lower-priority FIFO and writing INTW1 puts data in the higher-priority FIFO.

TOCTRL
This register control the IOP's bus time-out logic, and has the following format:

	TIMEOUT	VECTOR
5	3	8

The TIMEOUT field controls how long the IOP will wait for a DACKN response when it is running a bus cycle. If this time is exceeded, the IOP places the current channel number and the VECTOR field in the interrupt FIFO, as if an INT instruction had been executed. See Bus Time-out for further details.

UNRQ
This register is used to specify how many clock cycles the IOP would have to wait after finish servicing a channel and the external RQns show the same channel is still requesting for service. The register has the following format:

	CHANNEL
	5

The "count" field is the binary number of clocks the IOP waits. The time programmed in the register allows slow peripherals the time to clear its interrupt condition. If the request inputs RQns remain the same after the count expires, the IOP would service the channel again.

If the RQns change before the count expires (either during the count or before the count begins), the count will be stopped and the IOP will immediately service the new channel (or idle if all RQns go to 1's).

Programming this register with count = 0 means the IOP will not wait after the current channel service is completed. It is up to the user to make sure that any "request clearing" sequence performed by the IOP will not extend beyond the end of the channel service.

Channel Reloading
The instruction set discussed in a later section provides a means for a channel program for a peripheral device to interrupt the host processor when an I/O buffer area in memory has been "exhausted". Such exhaustion may occur in one of two ways: If the byte count for the I/O buffer is decremented to zero, or if a status or data byte's value indicates that the buffer should be (prematurely) terminated.

If an I/O buffer is exhausted, but the peripheral device has or will have more data to transfer for this channel, then the MAT and MCT entries (the memory address and byte count) for each channel have to be reloaded before further data can be transferred. Such reloading can occur in one of two ways:

1. By means of the processor responding to the interrupt and directly rewriting the MAT and MCT entries in the IOP. This approach is suitable for situations in which the processor responds to an interrupt fast enough to satisfy the needs of the peripheral, namely

a. If the peripheral device is not subject to "underrun" or "overrun" conditions based on the response time. For example, an asynchronized comm line meets this criterion with respect to output, but not with respect to input. A synchronous comm line does not met this criterion in either direction.

b. Or, if the data rate is slow enough, and/or the device contains sufficient data buffering, to guarantee that the processor's interrupt response time will be fast enough to prevent underrun or overrun. for example, a 300 baud comm line might meet this criterion but a 19,200 baud line might not.

2. For a peripheral channel that needs faster reloading than the host processor guarantees to provide, the IOP can automatically reload the next buffer address and count. To do this, two of the IOP's channel are dedicated to the peripheral channel; one of them handles the peripheral data, while the second is used to reload addresses and counts for the first channel. Only 16 peripheral channels of this type can be handled by one IOP.

A peripheral channel, for which reloading can be handled by host processor interrupt response, requires only one IOP channel; thus, 32 such peripheral channels can be handled by a single IOP.

Single and Dual Bus Applications

Applications of the IOP can be divided into two major categories called single and dual bus. In the single bus application shown in Figure 2, the IOP is on the same bus as the host processor, and must request and be granted the bus control before it can perform any bus cycle. This is a simple and low cost type of application, but does not yield the highest possible IOP performance.

Dual bus systems have the structure shown in Figure 3. Here, the IOP has its own local bus, on which resides the memory that contains channel programs and decision tables, and on which may also reside I/O buffers and/or peripheral devices. A set of hardware transceivers forms the interface between the IOP's local bus and the host processor's bus or an interboard backplane bus.

The transceivers are under the control of the bus grant signal (BGN), by which the outside world grants use of the system bus to the IOP, and the local bus grant signal (LBGN), by which the IOP grants the host processor or other master use of the local bus. After a reset, the IOP detects that it is in a dual-bus system if/when LBRN goes low.

In a two-bus system, the IOP monitors the state of the LBRN input continuously. When it detects an LBRN asserted, it tri-states its bus signals and then asserts LBGN. This occurs immediately if the IOP is not performing a cycle on the local bus.

In a dual bus system, the IOP does not assert BRN, nor does it wait for BGN for memory accesses for instruction or decision table fetching. These are assumed to be on the local bus. It may assert BRN and wait for BGN before an access to a data buffer in memory or to a peripheral device, depending on the state of the MSB ("A31" position) of the MAT or DAT entry for the channel, respectively.

If the bit that would correspond to A31 of the MAT or DAT entry has been set to 1 by MPU software, or a RELOAD instruction, the IOP does not assert BRN, nor does it wait for BGN. If the bit is cleared to 0, the IOP asserts BRN and waits for the MPU to return BGN low before proceeding to drive ASN low. While the IOP is waiting for BGN, it remains sensitive to the LBRN input. If LBRN goes low, the IOP defers the bus cycle, tri-states A23–A1 and the other bus control pins, and responds with LBGN low. When the cycle is completed and LBRN is released, the IOP reruns its bus cycle. This feature prevents a system deadlock if the IOP and MPU both request access to resources on each other's buses.

Dual bus applications tend towards higher performance by allowing the IOP to perform most of its bus cycles without stopping host processor execution, or without using the system's backplane bus. However, in this case the host processor must request control of the local bus in order to access memory or peripherals on the local bus, or to access IOP registers/RAM.

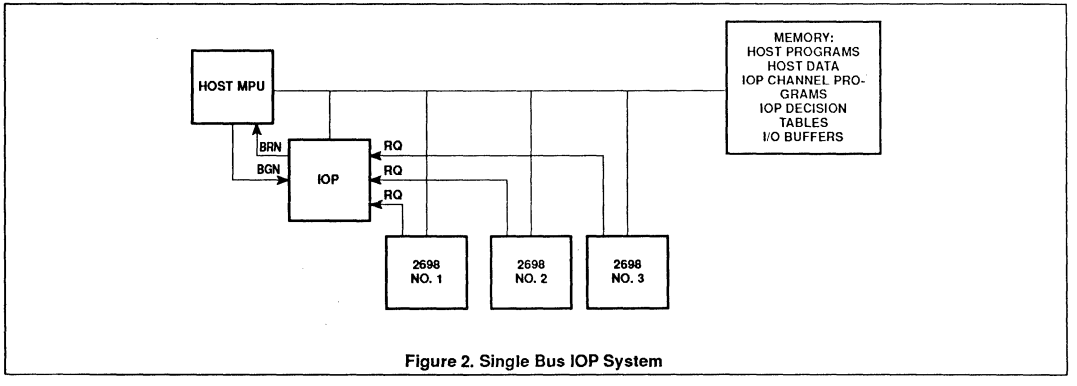


Figure 2. Single Bus IOP System

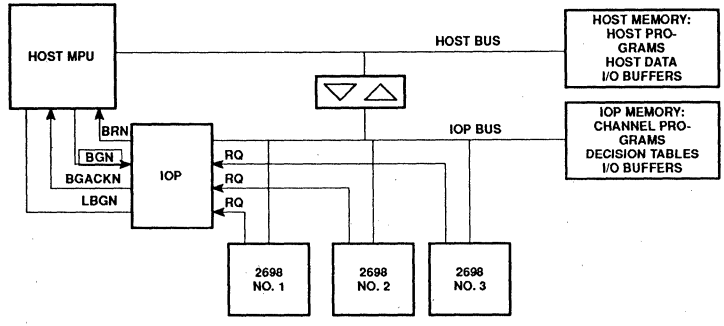


Figure 3. Two Bus IOP System

Byte Ordering

The 16-bit reads and writes are performed so that the more significant part of the value is taken from or placed on D15–D8 and the least significant part on D7–D0. For a byte read in master mode, data is taken from D15–D8 or D7–D0 depending on the state of A0, as shown in Table 1. Note that a byte written in master mode follows the same convention.

The MPU must access IOP register and memory locations as 16-bit words.

The IOP on-chip memories that are more than 16-bits wide (MAT and DAT) are accessed by the MPU by means of two consecutive 16-bit addresses. Table 1 also shows the relationship between the two parts of the MAT or DAT location and the state of the A1 line for the IOP.

Interfacing an 8-Bit Peripheral to a 16-Bit Bus

8-bit peripherals can be interfaced to the IOP's 16-bit data bus in one of two ways:

1. An 8-bit peripheral can be connected to one of the two halves of the data bus, and its A0–An inputs can be connected to the A1 – A <n + 1> lines of the bus.

   In this case, the peripheral appears to host software and IOP channel programs as occupying every other byte within its address range. The relationship between A0, and the data lines to which the peripheral is connected is as shown in Table 2. This method has the advantage of hardware simplicity but the disadvantage is that the 6-bit "device displacement" values in the IOP instructions can only span 32 register bytes.

2. Or, a peripheral's 8-bit bus can be interfaced to the 16-bit data bus using two octal transceivers, and its A0–An inputs can be connected to the A0–An lines on the bus (if A0 exists, otherwise A1–An signals). In this case, the peripheral appears to the host software or IOP channel program as a contiguous set of bytes as described in its data sheet. 6-bit "device displacement" values in the IOP instructions can span 64 byte location.

   In this case, one of the two transceivers is enabled according to A0 (see Table 2).

Table 1. Byte and Word Ordering for IOP

For a Byte Cycle With:	IOP Takes Data From:	For a Word Cycle With:	IOP Accesses:
A0 = 0	D7–D0	A1 = 0	LS 16 bits (bits 15–0)
A0 = 1	D15–D8	A1 = 1	MS 16 bits (bits 31–16)

Table 2. 8-Bit Peripheral Attachment for the IOP

If an 8-Bit Peripheral is Connected to:	Then the IOP addresses the peripheral with:	If an 8-Bit Peripheral is Connected to Both Halves of the Data Bus, then for a Cycle With:	Intel System Enables the Transceivers on:
D15–D8	Odd addresses	A0 = 0	D7–D0
D7–D0	Even addresses	A0 = 1	D15–D8

8- and 16-Bit Devices and Memories

The IOP requires a 16 (or 32) bit memory for its channel programs and decision tables, but can transfer data to and from memory either 8 or 16 bits at a time. It can also handle peripheral devices that transfer 8 or 16 bits of data at a time. the only exception to this facility is that only 8 bits of data can be interpreted at a time using a decision table. Several types of transfer sequences are possible during INPUT and OUTPUT instructions.

1. 8-bit device, 8-bit memory transfers. Each byte is read from the source (device or memory), placed in the CHAR register, optionally interpreted through a decision table. and then written to the destination (memory or device).
2. 16-bit device, 16-bit memory transfers. Each 16-bit word is read from the source, placed in CHAR and the BST entry for the channel, and then written to the destination. Either one of the two bytes in the word can be interpreted as part of the INPUT or OUTPUT command. If both bytes need to be interpreted, multiple instructions are needed.
3. 8-bit device. 16-bit memory transfers, INPUT instruction. In general, bytes destined for even-addressed memory locations are stored in the byte store table until the byte for the following odd-addressed location is available from the device. The composite 16-bit word is then written to memory. Each byte can be interpreted just after being read from the device.

4. 8-bit device, 16-bit memory transfers, OUTPUT instruction. In general, 16-bit words are read from memory. Each word's even-addressed byte is immediately sent to the device, while the odd-addressed byte is saved in the BST until the device is ready for it. Each byte can be interpreted just before it is sent to the device.

The BST and BSTO flags are included in the IOP to allow it to handle cases 3 and 4 above. While this adds on-chip RAM, operation in this mode is advantageous because it reduces the total number of cycles used on the bus.

CTRL Register

This register is programmable by the host processor to control the basic operation of the IOP (See Figure 4). Note that the contents of the CTRL register represents system-level constants that are intended to be programmed once, at system initialization time. The only bit that can be re-programmed thereafter is dE.

Bus Time-Out Facility

Whenever the IOP is accessing external memory or peripheral, it waits for DAcKN to be asserted. In case of certain system malfunctions, this response may never occur. Therefore, the IOP includes a time-out counter that operates whenever it is waiting for DACKN (but not when it is waiting for BGN). The time-out field of the TOCTRL register should be programmed to the host MPU before the IOP operation is enabled, to reflect a time-out longer than the longest valid DACKN response time that is possible in the system. The IOP will wait for DACKN for 2^{t+7} CLK periods, where t is the value of the 3-bit time-out field. Thus, a time-out field value of 0 will cause the IOP to wait up to 128 CLK periods. A 1 designates waiting 256 CLK periods, and so forth through the maximum time-out value of 7 which will cause the IOP to wait up to 16,384 CLK periods. At a CLK frequency of 16MHz, these correspond to a range of 8 microseconds to 1 millisecond.

If the time-out value is exceeded, the IOP internally simulates an INT instruction, using the higher priority level if there are two levels, using the vector field of the TOCTRL register as the vector value. Thus, it asserts the IRQN pin if it had not been asserted previously. After doing this, it clears the dE bit in the CTRL register so that it no longer responds to any further request signals. The vector from TOCTRL should cause the host MPU to investigate the problem and take appropriate corrective action.

Typical Execution

The next section describes the IOP instructions. For the instructions, the following general rules apply for channel program execution.

1. A peripheral device asserts its "interrupt request" output. This signal is either directly connected to one of the IOP's RQn inputs, or is encoded externally to make the value on RQ4–RQ0.

2. The request is serviced when no higher-priority peripheral is making a request.

3. The IOP begins service for this peripheral by transferring the encoded channel number to the CHAN and TCHAN registers, and then loads the value in the corresponding entry from the PCT RAM into its program counter (PC). It then executes the "channel program" that starts at the location in external memory.

   Note that the PCT entry for a channel is initially loaded by the host MPU, and can be changed by a channel program thereafter, in response to changing status of the peripheral device.

4. A channel program will typically start with an INTERP instruction that reads a status register on the peripheral and then uses the status byte as an index to read a word from a "decision table" in memory.

5. The contents of the word from the decision table may cause the IOP to do either, both, or neither of two things: change (add to) the value in the CHAN register, and/or branch, i.e. reload the PC with a value in the decision table word or from PCT [new CHAN].

   The two actions above correspond to the kinds of information that a peripheral status byte may convey: in a multi-channel peripheral device, it identifies which channel needs service, and/or it identifies any exceptional conditions (e.g. errors) involved in its "interrupt request".

   For example, in a peripheral with separate input and output channels, the decision table words corresponding to an "output request" might be coded to add 2 to (CHAN) and branch, while those corresponding to an "input request" might do neither of those things.

   Note that a priority between such input and output channels is determined by coding of words corresponding to "both requests". Also that while the decision table mechanism might be considered wasteful in memory, it improves performance by processing a whole status bye "in parallel" to make a decision that an MPU interrupt service routine might make by means of a series of "bit test" and "branch" instructions.

6. With some peripheral devices, several status registers may have to be read to determine what is to be done. For example, with the 2698 each DUART has an individual interrupt request line, but within each one, each UART has its own status register. In such cases, the channel program might begin with several consecutive INTERP instructions, one for each status register. The decision table words could be set up to:

   a. if the status register value indicates there is something to be done, branch to a routine to do it, or

   b. if there is nothing to be done, increment CHAN to the value that corresponds to the next status register, and don't branch.

7. After the INTERP instruction(s) have routed control to the appropriate branch of the channel program based on the peripheral status, a branch that transfers data will use an INPUT or OUTPUT instruction to transfer data between memory and (one of) the peripheral's data register(s).

8. INPUT and OUTPUT instructions can also use the decision table structure, for applications in which data byte values affect what is to be done. For example, in receiving from a datacomm line, reception of a carriage return (CR) character might mean that the current input buffer in memory is "complete" and that the host MPU should be notified.

   Decision table processing for INPUT and OUTPUT instructions is slightly different from that for INTERP. As with INTERP, certain data characters can cause a branch, but instead of CHAN adjustment, decision table words for data are coded to control whether the byte is transferred to the destination (to memory for INPUT, to the device for OUTPUT).

CTRL	dE	rE	0	MAX ON	MIN OFF	UPri	nL	
	1	1	1	4	4	3	1	1

dE — This bit enable the overall operation of the IOP. If it is zero, the IOP ignores the RQn lines. dE resets to zero; host MPU software should set up the various registers and RAM locations in the IOP before programming this bit to 1.

rE — This bit indicates how the RQ lines are interpreted by the IOP and how the starting CHAN value for service is derived from them. If the request code on RQ4–RQ0 is externally encoded, then rE should be programmed to 0, in which case the IOP treats the RQn lines as carrying a channel number. If (5 or less) devices "interrupt request" signals are directly connected to the RQ lines, then rE should be programmed to 1, in which case the IOP encodes the state of RQ4–RQ0 to obtain a channel number. In this encoding, RQ4 has the highest priority and RQ0 the lowest. A table in the request logic section indicates the starting CHAN value for each of the five devices (RQ lines) when rE is 1.

Max On, Min Off — These fields are used only in single-bus applications. Max On controls the maximum length of time the IOP will retain control of the bus after being granted it, while Min Off controls the length of time for which the IOP will refrain from requesting the bus again, after it has given it up. Together, these two values constitute a "throttle" control on how much of the overall bus bandwidth an IOP will use. These times are measured in terms of the CLK input divided by 4. Max On = 0 indicates that the IOP will run only one bus cycle per grant. Note that in dual-bus application, the IOP will always give up control of the system bus after using it for one cycle, so that these values do not apply.

UPri — UPri assigns the starting channel number for each RQn input in the internal encoded mode (rE = 1). In this assignment, the lower the starting channel, the higher the priority. The effect of UPri on starting channel numbers is as follows:

← STARTING CHANNEL NUMBER →

INTERNALLY ENCODED RQ's

UPri	RQ4	RQ3	RQ2	RQ1	RQ0
000	8	12	16	20	24
001	0	12	16	20	24
010	0	4	16	20	24
011	0	4	8	20	24
100	0	4	8	12	24
101	0	4	8	12	16

nL — This bit controls how the interrupt FIFO is configured. If nL is 0, it is treated as a single FIFO of 32 entries, which are all at the same level of priority. If nL is 1, it is divided into 2 FIFOs each having 16 entries, representing two priority levels.

Figure 4. CTRL Register

9. An INPUT and OUTPUT instruction will typically be written so that it ends servicing for the channel unless a decision table causes a branch, or the byte count for the I/O buffer in memory is decremented to zero.

10. When an I/O buffer is completed, the channel program will typically interrupt the host MPU. Such interrupts are stored in a queue on the IOP, so that the host MPU is interrupted once for each time any IOP channel program posts an interrupt.

11. In addition to interrupting the host when an I/O buffer is completed, the channel program can either use a RELOAD instruction to get another I/O buffer from a circular list of such buffers, or send a command byte to the device to tell it to stop asserting its "interrupt request" line for this channel, until the host MPU responds to the interrupt posted by the channel program.

INSTRUCTION SET

INTERP

0100	0	DecTab#	S	devdisp
4	1	4	1	6

This instruction is used fro examining status bytes and similar data.

1. If devdisp is not "all ones", data is read from an external device at the address formed as follows:

   A23–0 (DAT[CHAN] XOR devdisp

   Bit 15 of MCT[CHAN] determines the size of data read from the device:

a. If this bit indicates a 16-bit peripheral, a word is read from the device. The units bit of the address has no effect on the cycle with the device, but rather serves to identify which byte of the word is interpreted. The byte selected by the units bit of the address is placed in CHAR and the other byte is placed in BST[CHAN]. The units bit of the address is saved in the internal SVA0 flag in case the word needs to be reconstituted later.

   If the S bit of the instruction is 1, the selected byte is also stored in the internal SVCHAR register, and the other byte is stored in the internal SVBST register, for later retrieval and reinterpretation.

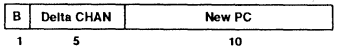
b. IF bit 15 of MCT[CHAN] indicates an 8-bit peripheral, a byte is read and placed in CHAR. If the S bit of the instruction is 1, the byte is also stored in the SVCHAR register, for later retrieval and reinterpretation.

2. If devdisp = all ones, (CHAR) from a previous instruction is used in the following steps, and the S bit of the instruction has no effect.

3. A word is read from a decision table at the address formed as follows:

   A23–13: (DTBR)
   A12–9: DecTab#
   A8–1 (CHAR)
   A0: 0 for word access.

   This word is interpreted as follows:

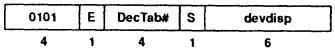


Note that this is the only instruction that can use DecTab# 0.

4. The Delta CHAN value is added to (CHAN), the result being new contents for the CHAN register.

5. If B = 1, the IOP tests whether the new PC value is "all ones". If so, it loads (PCT[CHAN]) into the PC, otherwise it loads the New PC value in the decision table word into the PC. In either case, the IOP executes its next instruction from the new location. If B = 0, the next instruction is performed.

INPUT



This instruction provides the basic data transfer mechanism from devices to memory areas.

1. If devdisp is not "all ones", data is read from an external device at the address formed as follows:

   A23–0: (DAT[CHAN]) XOR devdisp.

   Bit 15 of MCT[CHAN] determines the size of data read from the device.

a. If this bit indicates a 16-bit peripheral, a word is read from the device. The units bit of the address has no effect on the cycle with the device, but rather serves to identify which byte of the word is interpreted in the next phase of instruction operation. The byte selected by the units bit of the address is placed in CHAR and the other byte is placed in BST[CHAN]. The units bit of the address is saved in the SVA0 flag in case the word needs to be reconstituted later.

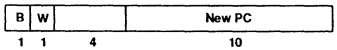
   If the S bit of the instruction is 1, the selected byte is also stored in the SVCHAR register, and the other byte is stored in the SVBST register, for later retrieval and reinterpretation.

b. If bit 15 of MCT[CHAN] indicates an 8-bit peripheral, a byte is read and placed in CHAR. If the S bit of the instruction is 1, the byte is also stored in the SVCHAR register, for later retrieval and reinterpretation.

2. If devdisp = all ones, (CHAR), and (BST [CHAN]) if applicable, from a previous instruction are use in the following steps, and the S bit of the instruction has no effect.

3. If DecTab# > 0, a word is read from a decision table at the address formed as follows:

   A23–13: (DTBR)
   A12–9: DecTab#
   A8–1: (CHAR)
   A0: 0 for word access.
   This word is interpreted as follows:



If DecTab# = 0, the IOP performs the following steps as if B = 0 and W = 1.

4. If the W bit is 1, bits 15 and 14 of MCT [CHAN] determine how the data is transferred to memory:

a. If these bits indicate an 8-bit peripheral and 8-bit memory transfers, the byte in CHAR is written to memory at the address in MAT[CHAN]. The address is incremented by 1, and the count in MCT[CHAN] is decremented by 1.

b. If MCT[CHAN] bits 15–14 indicate a 16-bit peripheral and 16-bit memory (SVA0) so that the word is written in the same way it was read from the device. The address is incremented by 2, and the count in MCT[CHAN] is decremented by 2.

c. If MCT[CHAN] bits 15–14 indicate an 8-bit peripheral and 16-bit memory transfers:

i. If the address in MAT[CHAN] is not 0001, the byte in CHAR is placed in BST[CHAN], and the BSTO[CHAN] flag is set.

ii. If the address is even and the count is 0001, (CHAR) is written to memory as a byte.

iii. If the address is odd and the BSTO[CHAN] flag is set, a word is written to memory. Its even-addressed byte is obtained from BST [CHAN] and its odd-addressed byte is obtained from CHAR.

iv. If the address is odd and the BSTO[CHAN] flag is not set, (CHAR) is written to memory. This will only occur for the first byte in a buffer that starts at an odd address.

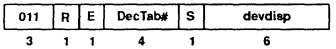
Regardless of how (CHAR) is handled, the address in MAT[CHAN] is decremented by 1, and the count in MCT[CHAN] is decremented by 1.

5. If the B bit is 1 and the "new PC" value is all ones, (PCT[CHAN]) is loaded in the PC, and execution continues from that address. If B is 1 and the "new PC" is not all ones, the "new PC" is loaded into the PC, and execution continues from that address.

6. If the count was not decremented to 0 in step 5, and B is 0, and E is 1, the service for this device is completed.

7. If the count was decremented to 0 in step 5 or (B is 0 and E is 0), execution continues at the next instruction.

OUTPUT



The instruction provides the basic data transfer mechanism from memory areas to devices.

1. If R = 1, bit s 15 and 14 of MCT[CHAN] determine how memory data is obtained for transfer to the peripheral:

a. If these bits indicate an 8-bit peripheral and 8-bit memory transfers, a byte is read from memory at the address in MAT[CHAN] and is placed in the CHAR register. The address in MAT[CHAN] is incremented by 1, and the count in MCT[CHAN]] is decremented by 1.

   If the S bit of the instruction is 1, the byte placed in CHAR is also stored in the SVCHAR register, for later retrieval and reinterpretation.

b. If MCT[CHAN] bits 15 and 14 indicate a 16-bit peripheral and 16-bit memory transfers, a word is read from memory at the address in MAT[CHAN]. The units bit of the address has no effect on the memory cycle but rather serves to select which byte can be interpreted in the next phase of instruction operation. The byte selected by the units bit of the address is placed in CHAR, the other byte is placed in BST[CHAN], and the units bits is saved in the SVA0 bit so the word can be reconstituted later. The address in MAT[CHAN] is incremented by 2, and the count in MCT[CHAN] is decremented by 2.

   If the S bit of the instruction is 1, the byte placed in CHAR is also stored in the SVCHAR register, and the other byte is stored in the SVBST register, for later retrieval and reinterpretation.

c. If MCT[CHAN] bits 15 and 14 indicate an 8-bit peripheral and 16-bit memory transfers, a byte is obtained in one of the following ways and is placed in CHAR:

i. If the address in MAT[CHAN] is even and (MCT[CHAN]) is not 0001, a word is read from that address. Its even-addressed byte is placed in CHAR, its odd-addressed byte is placed in BST[CHAN], and the BSTO[CHAN] flag is set.

ii. If the address is even and the count in MCT[CHAN] is 0001, a byte is read from the address.

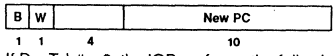
iii. If the address is odd and the BSTO[CHAN] flag is set, the byte in BST[CHAN] is transferred to CHAR.

iv. If the address is odd and the BSTO[CHAN] flag is not set, a byte is read from the address. This will only occur for the first byte in a buffer that starts at an odd address.

Regardless of how the byte is obtained, the address in MAT[CHAN] is incremented by 1, and the count in MCT[CHAN] is decremented by 1. If the S bit of the instruction is 1, the byte placed in CHAR is also stored in the SVCHAR register, for later retrieval and reinterpretation.

2. If R = 0, (CHAR) and (BST[CHAN]) from a previous instruction are used in the following steps, and the S bit of the instruction has no effect.

3. Unless DecTab# = 0, a word is read from a decision table at the address formed as follows:
   A23–13: (DTBR)
   A12–9: DecTab#
   A8–1: (CHAR)
   A0: 0 for word access.
   This word is interpreted as follows:



If DecTab# = 0, the IOP performs the following steps as if B = 0 and W = 1.

4. If devdisp is not "all ones" and the W-bit is 1, data is sent to an external device at the address formed as follows:

   A23–0: (DAT[CHAN]) XOR devdisp

   Bit 15 of MCT[CHAN] determines how much data is sent:

a. If this bit indicates a 16-bit peripheral, a word is sent to the device. The data is comprised of (BST[CHAN]) and (CHAR), arranged according to (SVA0) so that the word is written in the same way it was read from memory.

b. If bit 15 of MCT[CHAN] indicate an 8-bit peripheral, (CHAR) is sent to the device

5. If the B bit is 1 and the "new PC" value is all ones, (PCT[CHAN]) is loaded in the PC, and execution continues from that address.

   If B is 1 and the "new PC" is not all ones, (PCT[CHAN]) is loaded into the PC, and execution continues from that address.

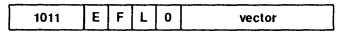
   If B is 1 and the "new PC" is not all ones, the "new PC" is loaded in the PC, and execution continues from that address.

6. If the count was not decremented to 0 and B is 0, and E is 1, the service for this device is completed.

7. If the count was decremented to 0, or (B is 0 and E is 0), execution continues at the next instruction.

Note that an OUTPUT instruction with R = 0, DecTab# = 0, devdisp = 1111111, (MCT) > 0, and E = 1 does nothing other than completing the current service. Same conditions with E = 0 can be used as NOP instructions.

INT



When the command is executed, the following steps are performed:

1. If the F bit is 1 and the BSTO[CHAN] flag is set, then the current buffer is "closed" as follows:

a. (BST[CHAN]) is written to memory at the address in MAT[CHAN] minus one. (The address in MAT[CHAN] is always odd when BSTO is set, so this is accomplished by simply forcing A0 to 0.) The operation is actually a word write, with the data written to the odd-addressed byte being undefined. Since the byte in BST[CHAN] would not have been placed there if MCT[CHAN] indicated it was destined for the last byte available in the buffer, a word write is always permissible.

b. The address in MAT[CHAN] in not incremented, and the count in MCT[CHAN] is not decremented (these two operations already occurred for this byte when it was placed in BST).

c. The BSTO[CHAN] flag is cleared.

2. 'vector' and (CHAN) are written into the interrupt FIFO. If nL in the CTRL register is 1 and L is 0, they are placed in the lower-priority queues. If nL in the CTRL register is 1 and L is 1, they are placed in the higher-priority queue. If nL is 0, there is only one 32-entry queue, and the L bit is ignored.

3. The IRQN pin is asserted (if it was not already asserted).

4. If E is 1, service for this channel is concluded; otherwise the next instruction is performed.

When the host processor responds by asserting the IACKN pin, or by polling the INTRD register, the following steps are performed:

1. If nL is 1 and there is at least one entry in the higher-priority FIFO, the higher-priority FIFO is selected. If nL is 1 and the higher-priority FIFO is empty, the lower-priority FIFO is selected. If nL is 0, the single 32-entry FIFO is selected.

2. The vector byte from the top entry in the selected FIFO is placed on the external data pins (D7–D0), and DACKN is asserted.

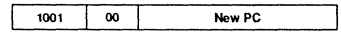
3. The channel number for the top entry in the selected FIFO is copied to the INTCHN register, from which it can be read by the host MPU.

4. The selected FIFO is "popped", that is, its top entry is removed.

5. IF nL is 1 and both FIFOs are now empty, or nL is 0 and the (single) FIFO is now empty, the IRQN pin is negated.

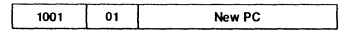
By the mechanism described above, the IOP maintains two internal interrupt priority levels at which a channel program can post an interrupt to the host MPU. All interrupts with L = 1 have a higher priority than any interrupts with L = 0, but within each level interrupts are presented to the host MPU in the order that they were posted by the channel program(s). For example, for external UARTs, all "receive" and "error" interrupts might be posted at level 1 while "transmit" interrupts are posted at level 0.

JC0



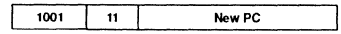
If the count in MCT[CHAN] is zero, then the value "new PC" is loaded in the PC and these becomes the address of the next instruction executed. Otherwise, the next instruction is executed.

JNC0



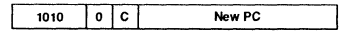
If the count in MCT[CHAN] is zero, then the value "new PC" is loaded in the PC and thus becomes the address of the next instruction executed. Otherwise, the next instruction is executed.

JUMP



The value "new PC" is unconditionally loaded in the PC and thus becomes the address of the next instruction executed.

LDPCT

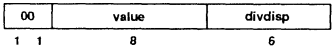


The value "New PC" is loaded in a PC entry and thus becomes the starting point for execution for future device service. If C is 0, the vale is loaded in PCT[TCHAN], where TCHAN is the channel number at which execution was started for the current device (i.e., the request code of the current device). If C is 1, the value is loaded in PCT[CHAN]. Note that CHAN may have been changed by INTERP instructions since the start of execution.

The TCHAN register is also used by the RELOAD instruction. If both a RELOAD instruction

and a LCPCT instruction with C = 0 are to be done during the same execution, the LDPCT must be executed first.

SEND2DEV

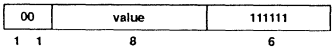


"value" is sent to an external device at the address

A23–0: (DAT[CHAN]) XOR devdisp.

This instruction is useful for sending fixed byte values (e.g., commands) to devices. (CHAR) is not used or changed by this instruction. for SEND2DEV, devdisp may not be all ones, because this value identifies the instruction as SEND2MEM.

SEND2MEM



The "value" byte is written to memory as if it had been received from the device in an INPUT instruction. Bit 14 of MCT[CHAN] determines how the data is transferred to memory.

1. If MC T[CHAN]14 = 0, indicating 8-bit memory transfers, "value" is written as a byte at the address in MAT[CHAN].

2. If MCT[CHAN]14 = 1, indicating 16-bit memory transfers, the IOP proceeds as follows:

a. If the address in MAT[CHAN] is even and the count in MCT[CHAN] is not 0001, "value" is placed in BST[CHAN], and the BSTO[CHAN] flag is set.

b. If the address is even and the count is 0001, "value" is written to memory as a byte.

c. If the address is odd and the BSTO[CHAN] flag is set, a word is written to memory. Its even-addressed byte is obtained from BST[CHAN] and its odd-addressed byte is "value".

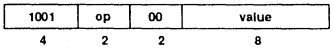
d. If the address is odd and the BSTO[CHAN] flag is not set, "value" is written to memory as a byte.

Regardless of the memory width and how "value" is handled, the address in MAT[CHAN] is incremented by 1, and the count in MCT[CHAN] is decremented by 1.

An example of use of this instruction is to substitute an error code when a character with a parity error is received from a comm link.

If device data is also 16 bits wide, SEND2MEM instructions should be done in pairs so as to store 16-bit values in memory. If a single SEND2MEM is performed during service for a channel for a 16-bit device, its data byte may be written to memory immediately, or the byte may be lost, or the byte may be written to memory after intervening words stored by INPUT instructions. Careful examination of the procedure described above, and the description for INPUT, will clarify the various possibilities.

LDCHAR



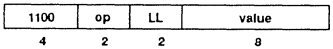
"value" is loaded into CHAR and/or SVCHAR depending on "op" as follows:

op	Operation
00	CHAR: = value
01	SVCHAR, CHAR: = value IF MCT[CHAN] 15 = 1, BST[CHAN]: = (SVBST)
10	BST[CHAN]: = (CHAR); CHAR: = value. SVA0: = 0
11	as 10 except SVA0: = 1

With op = 00, the 8-bit immediate value is simply placed in CHAR for use by subsequent instructions. With op = 01, the value is placed in both SVCHAR and CHAR, and if the channel involves a 16-bit peripheral, the contents of SVBST are retrieved and placed in BST [CHAN]. the latter characteristic of operation with op = 01 is by symmetry with the next group of (logic) instructions. No specific application of this characteristic is foreseen.

With op = 1x, the previous contents of CHAR are sent to BST[CHAN], the new value is placed in CHAR, and the SVA0 flag is set as indicated. As noted in a subsequent section, one LDCHAR with op = 00 can be followed by one with op = 1x to set up to a "16-bit immediate value" that can then be sent to a 16-bit device in one operation by an OUTPUT command.

ORCHAR, ANDCHAR, XORCHAR



The logical combination indicated by LL, between "value" and (CHAR), (SVCHAR), or (BST[CHAN]), is formed and then placed in CHAR and/or SVCHAR. LL values are as follows:

LL	Function
01	ANDCHAR
10	ORCHAR
11	XORCHAR

while "op" values are as follows:

op	Operation
00	CHAR: = value LL CHAR
01	SVCHAR, CHAR: = value LL SVCHAR; IF MCT[CHAN] 15 = 1, BST[CHAN]: = (SVBST)
10	tmp: = value LL BST[CHAN]; BWT[CHAN]: = (CHAR); CHAR: = tmp; SVA0: = 0
11	same as 10 except SVA0: = 1

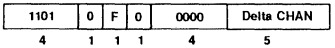
These instructions, with op = 00, can be used by a channel program to produce a "command" value from a "status" value from a peripheral. In particular, command/status bytes for some peripherals include a collection of information for multiple sub-devices/channels. In such cases, it is necessary to modify certain bits in the byte value while preserving other bits "as is".

With op = 01, these instructions can be used to retrieve (SVCHAR), potentially modified, back into CHAR for use by a subsequent INTERP instruction having an all ones "devdisp" field. If a status register contains multiple event flags, this facility can be used to handle the events one by one. If the channel involves a 16-bit peripheral, BST[CHAN] is also retrieved from SVBST.

With op = 1x, the instructions can be used to more or less exchange (BST[CHAN]) and (CHAR), with modification, which may be useful in conjunction with handling 16-bit data or status values for 16-bit devices.

Note that ORCHAR with value = 0 comprises a "move" operation.

RELOAD



1. If the F bit is 1 and the BSTO[CHAN] flag is set, then the current buffer is "closed" as follows:

a. (BST[CHAN]) is written to memory at the address in MAT[CHAN] minus one. (The address in MAT[CHAN] is always odd when BSTO is set, so this is accomplished by simply forcing A0 to 0). The operation is actually a word write, with the data written to the odd-addressed byte being undefined. Since the byte in BST[CHAN] would not have been placed there if MCT[CHAN] indicated it was destined for the last byte available in the buffer, a word write is always permissible.

b. The address in MAT[CHAN] is not incremented, and the count in MCT[CHAN] is not decremented (these two operations already occurred for this byte when it was placed in BST).

c. The BSTO[CHAN] flag is cleared.

2. The sum (CHAN) + Delta CHAN is formed and placed in the TCHAN register. A second IOP channel is selected by (TCHAN). The 24-bit contents of MAT[CHAN], with 8 high-order zeros, are written into memory by means of two consecutive 16-bit writes starting at the address in MAT[TCHAN], followed by one 16-bit write of 0000. MAT[TCHAN] is incremented and MCT [TCHAN] is decremented as these words are written, for a total increment/decrement of 6 (bytes).

3. If MCT[TCHAN] is zero at the conclusion of these writes, then the contents of DAT [TCHAN] are copied into MAT[TCHAN], and the contents of PCT[TCHAN] are copied into the 10 LSBs of MCT[TCHAN]. This feature allows a wraparound "ring" of buffer addresses and counts, containing DAT [TCHAN] / 6 entries.

Note that while PC entries contain less bits than MCT entries, 10 bit are more than enough to contain the length of the buffer address table used for reloading.

4. Whether or not such a wraparound occurs, the IOP saves (MAT[TCHAN], then reads two words from memory at the new address in MAT[TCHAN] and places the contents in MAT[CHAN], and then read the next word and places its contents in MCT[CHAN]. Finally it restores MAT[TCHAN] to the saved value, so that it once again points to the first word of the address in memory.

If there are only a few buffers in the ring (e.g. 2), and the processor takes a long time from servicing interrupts, it is possible that all the buffers in the ring may be exhausted. This can be tested by a JC0 or JNC0 instruction following the RELOAD.

Figure 5 shows the effect of two different executions of a RELOAD instruction with CHAN = 7 and Delta CHAN = 2. Channel 7 has a ring of three I/O buffers and is reloaded via channel 9. The first RELOAD is issued after "n" bytes have been transferred from or to buffer area 1', at which time the host MPU is "Current" in that it has provided the addresses and counts of buffers 2 and 3. The other RELOAD is executed some time later; "m" bytes have been transferred from or to buffer 3, and the host MPU is a little "behind" in that it has refreshed the address and count for buffer 1 but has not yet done so for buffer 2.

Host Software Constraints

The count loaded in the MCT and PCT entries, for an IOP channel that is used for reloading, must be a multiple of 6.

In analyzing the contents of a buffer that was "prematurely terminated" because of interpreting a status or data byte, system software does not have access to the residual count for the buffer. However, since the address in a MAT entry is always incremented whenever the count in the corresponding MCT entry is decremented, the stored address conveys the same information in a slightly less convenient form.

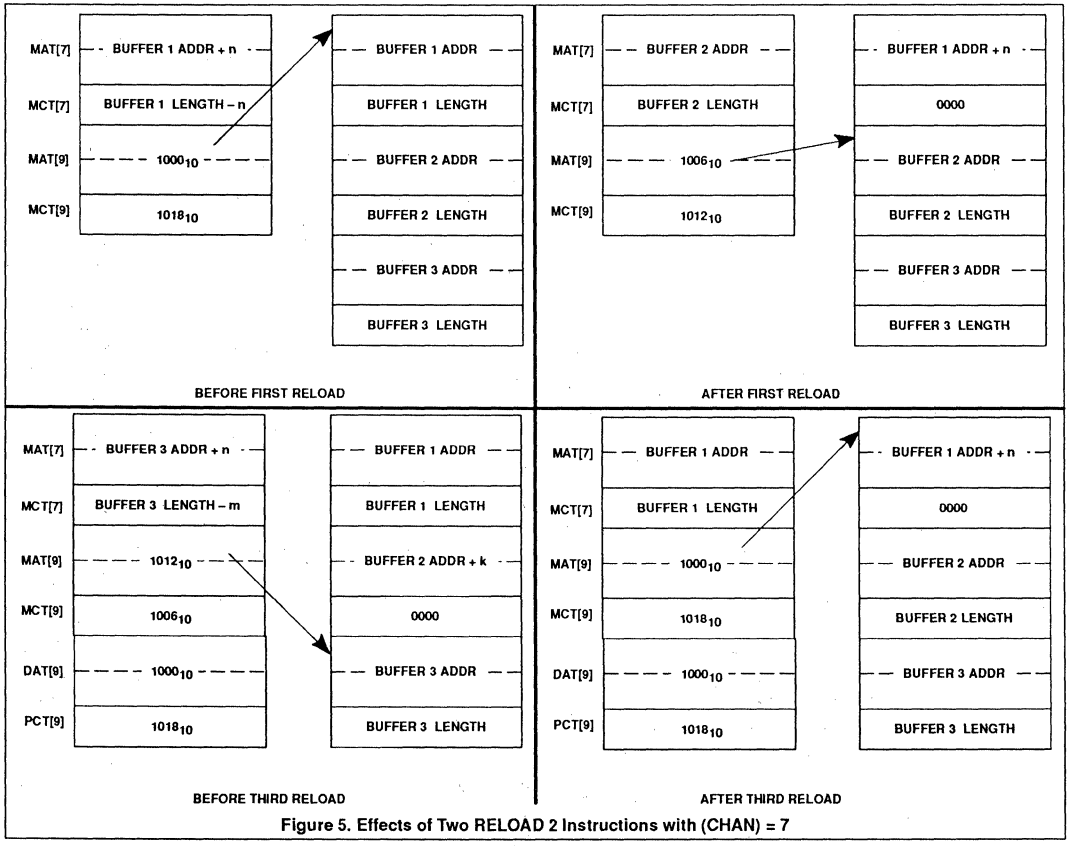


Figure 5. Effects of Two RELOAD 2 Instructions with (CHAN) = 7

Some Applications

This section provides a few examples of how various IOP instructions can be combined.

Sending a Word to a Device

SEND2DEV only send an 8-bit byte to a device. If a 16-bit word must be sent to a 16-bit device in a single write operation, a sequence like the following can be used:

```
LDCHAR  value1
LDCHAR  value2, op=1x
OUTPUT  R = 0, decTab#=0
```

Interpreting a 16-Bit Status Value

To interpret both bytes in a status value from a 16-bit device, without re-reading the word:

```
INTERP TAB1,statreg_offset
OR 0, op=1x
INTERP TAB2, X"3F'
```

Interpreting a 16-Bit Data Value

As the previous example, but the 16-bit value should be written to memory if both bytes "pass" interpretation:

```
INTERP TABA,datareg_offset
OR 0, op=1x
INPUT TABB, X"3F'
```

Additional Notes

Since the IOP maintains its addresses and buffer length in on-chip RAM, it can service any of its channels without having to fetch this data from external memory.

The best-case service time for a channel is when its channel program consists of a single INPUT or OUTPUT instruction, with neither status nor data interpretation. In this case, servicing the channel takes three bus cycles: one to fetch the instruction, one to read the memory or peripheral, and one to write to the peripheral or memory.

Perhaps more typical is the case when peripheral status needs to be interpreted. In this case, an instruction read, a status read and a decision table read are added before the transfer instruction is read, for a total fo six bus cycles.

In the 2698 OCTART handler shown in Listing 1, there are tow separate status registers that may need to be read. Thus, a single character can be handled in either six or nine bus cycles, or an average of 7.5. However, when the receive FIFO is full, the handler uses the 2698's flag indication to process 4 received characters in 18 or 21 cycles, an average of 4.875 bus cycles per character. Similarly, when the transmitter is completely empty, the handler processes 2 transmitted characters in 10 or 13 bus cycles, an average of 5.75 bus cycles per character.

If data is to interpreted as well as status, another decision table read is performed between the data read and write cycles, for a total of (at least) seven bus cycles.

All of these figures assume that decision table reads do not indicate any exceptional action such as buffer termination or error handling, and that the buffer count does not expire. Such (rare) occurrences may add substantially to the number of cycles and the time to service a channel.

Listing 1. Sample of IOP Service Routine for a 2698

```
                                ; IOPC HANDLER FOR 2698
                    0000        ;       BEGIN_PROG

                                ; OFFSETS OF 2698 REGISTERS, TIMES 2 FOR BYTE DEVICE
00000002            0000        SR      -       2       ; STATUS
00000004            0000        CR      -       4       ; COMMAND
00000006            0000        RHR     -       6       ; RECEIVE DATA
00000006            0000        THR     -       6       ; TRANSMIT DATA
                                ; COMMAND CODE IN CR
00000008            0000        DTX     -       8       ; DISABLE TX

                                ; DECISION TABLE FORWARD REFERENCES
00000000            0000        SRTAB   -       0

                                ; 2698 CHANNEL PROGRAM STARTS HERE
                                ;  (HOST PUTS STRT98 IN 4 PCT ENTRIES
                                ; THE FOLLOWING INTERPS BRANCH IF THE SR OF A UART IS NON-ZERO,
                                ;  OTHERWISE THEY STEP CHAN +2 AND CONTINUE TO THE NEXT INSTRUCTION
        4002        0000        STRT98: INTERP  SR,SRTAB    ; TEST UART #1 STATUS
        4002        0002                INTERP  SR,SRTAB    ; TEST UART #2 STATUS

                                ; FLAG ERROR:
                                ;       BOTH STATUS REGS ZERO,
                                ;       FFULL WITHOUT RXRDY,
                                ;       TXEMT WITHOUT TXRDY
        B816        0004        FLGERR: INT     22,END      ; 22 IS VECTOR FOR WEIRD THINGS

                                ; RECEIVE 4 CHARACTERS (INTERP BRANCHES HERE IF FFULL)
        5006        0006        RCV4    INPUT   RHR         ; ONE
        900A'       0008                JC0     RCVEND
        5006        000A                INPUT   RHR         ; TWO
        900A'       000C                JC0     RCVEND
        5006        000E                INPUT   RHR         ; THREE
        900A'       0010                JC0     RCVEND

                                ; RECEIVE 1 CHARACTER (INTERP BRANCHES HERE IF RXRDY, NO FFULL)
        5806        0012        RCV:    INPUT   RHR,,END    ; READ RHR, WRITE MEMORY
        B818        0014        RCVEND  INT     24, END

                                ; TRANSMIT 2 CHARACTERS (INTERP BRANCHES HERE IF TXEMT, NO RXRDY)
        7006        0016        XMIT    OUTPUT  THR         ; ONE
        900E'                           JC0     XMITEND

                                ; TRANSMIT 1 CHARACTER (INTERP COMES HERE IF TXRDY, NO RXRDY NOR TXEMT)
        7806        001A        XMIT:   OUTPUT  THR, END    ; READ MEMORY, WRITE THR
        0204        001C        XMITENC SEND2DEV CR, DTX    ; DISABLE THE TRANSMITTER
        B819        001E                INT     25, END

                                ; RECEIVER ERROR(S) (INTERP BRANCHES HERE IF ANY OF 4 HIGH SR BITS)
        B817        0020        RCVERR: INT     23, END

                                ; ----------------------
                    0022                BEGIN_DTABS

                                ; DECISION TABLE FOR 2698 SR
        0000                            DTAB    SRTAB
        0800        0000                IDTE    ,2          ; IF STATUS = 0, NO BRANCH, STEP CHAN +2
        8009        0002                IDTE    RCV         ; RXRDY
        8002        0004                IDTE    FLGERR      ; FFULL, NO RXRDY IS IMPOSSIBLE
        8003        0006                IDTE    RCV4        ; FFULL, RXRDY
        840D        0008                IDTE    XMIT,1      ; TXRDY (STEP CHAN +1)
        8009        000A                IDTE    RCV         ; TXRDY, RXRDY
        8002        000C                IDTE    FLGERR      ; FFULL, NO RXRDY IS IMPOSSIBLE
        8003        000E                IDTE    RCV4        ; TXRDY, FFULL, RXRDY
        8002'       0010                IDTE    FLGERR,,4   ; TXEMT, NO TXRDY IS IMPOSSIBLE
        840B        0018                IDTE    XMIT2,1     ; TXEMT, TXRDY (STEP CHAN +1)
        8009        001A                IDTE    RCV         ; TXEMT, TXRDY, RXRDY
        8002        001C                IDTE    FLGERR      ; FFULL, NO RXRDY IS IMPOSSIBLE
        8003        001E                IDTE    RCV4        ; TXEMT, TXRDY, FFULL, RXRDY
        8010'       0020                IDTE    RCVERR,,240 ; RECEIVE ERRORS
        8010'       0028
(ETC. . .)
```

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating ambient temperature range	0 to +70	°C
Storage temperature range	–65 to +150	°C
Supply voltage to ground	–0.5 to +6.5	V
Power dissipation		

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperature, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS	TENTATIVE LIMITS		UNIT
			Min	Max	
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
V_{OL}	Output low voltage	I_{OL} = 2.4mA		0.4	V
V_{OH}	Output high voltage (except open-drain outputs)	I_{OH} = –400µA	2.4		V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	10	10	µA
I_{LL}	Data bus 3-State leakage current	V_{IN} = 0 to V_{CC}	10	10	µA

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10%[1]

NO.	FIGURE	PARAMETER	TENTATIVE LIMITS		UNIT
			Min	Max	
1	6	BCLK period (t_{BCLK})	60	600	ns
2	6	BCLK width high	25		ns
3	6	BCLK width low	25		ns
4	6	RESETN width low	1000		ns
Master Arbitration					
5	7	BCLK high to BRN low		50	ns
6	7	BRN low to BGN low	0		ns
7[1]	7	Setup, BGN low to BCLK low	10		ns
8	7	BCLK high to drivers enabled	2		ns
9	7	BCLK high to BRN high		50	ns
10	7	BRN high to drivers disabled	0	20	ns
11	7	BRN high to BGN high	0		ns
12[1]	7	Setup, BGN high to BCLK low	10		
Master Operation					
20	8, 9	BCLK high to A23:1 change	0		ns
21	8, 9	BCLK high to A23:1 valid		50	ns
22	8, 9	BCLK high to RWC valid	0	50	ns
23	8, 9	BCLK high to M/IO valid	0	50	ns
24	8, 9	A23:1. RWC. and M/IO valid to ASN low	20		ns
25	8, 9	BCLK high to ASN low	4	45	ns
26	8, 9	BCLK high to DHIEN and/or DLOEN low	4	45	ns
27	8	D15:0 valid (read) to DACKN low	0		ns
28[1]	8, 9	Setup, DACKN low to BCLK high	10		ns
29	8, 9	BCLK low to ASN high		50	ns
30	8, 9	BCLK low to DHIEN and DLOEN high		50	ns
31	8	Hold, read data valid after DHIEN and DLOEN high	0		ns
32	8, 9	DHIEN and DLOEN high to DACKN high (to avoid acknowledging next cycle)		t_{BCLK}	ns
34	9	BCLK high to data bus drivers enabled (write)	0		ns
35	9	BCLK high to write data valid		60	ns
36	9	Write data valid to DHIEN and/or DLOEN low	10		ns
37	9	Hold, write data valid after BCLK high	10		ns
38	9	BCLK high to data bus released (end of write)		40	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

NO.	FIGURE	PARAMETER	TENTATIVE LIMITS Min	TENTATIVE LIMITS Max	UNIT
Slave Arbitration (Two Bus System)					
39[1]	10	Setup, LBRN low to BCLK low	10		ns
40	10	BCLK high to LBGN low		45	ns
41	10	BCLK high to IOP drivers disabled		30	ns
42	10	LBGN low to IOP drivers disabled		20	ns
43[1]	10	Setup, LBRN high to BCLK low	10		ns
44	10	LBRN high to LBGN high		40	ns
45	10	BCLK high to IOP drivers enabled	10		ns
Slave Operation					
47	11, 12	Setup, A8:1 valid to CSN low	0		ns
48	11, 12	Setup, RWC valid to CSN low	0		ns
49	11, 12	Setup, DHIEN and/or DLOEN low to CSN low	0		ns
50[1]	12, 13	Setup, CSN low to BCLK low	10		ns
51[3]	11, 12, 13	IOP response latency	$3t_{BCLK}$	$11t_{BCLK}$	ns
53	11, 12	BCLK low to data bus valid (read or IACK)		65	ns
54	11, 12, 13	BCLK low to DACKN low		40	ns
55	11, 12	DACKN low to CSN high or (DHIEN and DLOEN high)	0		ns
56	11	Hold, data bus valid after CSN high or (DIEHN and DLOEN high)	10		ns
57	11	CSN high or (DHIEN and DLOEN high) to data bus released		30	ns
58	11, 12	CSN high or (DHIEN and CLOEN high) to DACKN released		25	ns
59	11, 12	Hold, A8:1 valid after CSN high or (DHIEN and DLOEN high)	0		ns
60	11, 12	Hold, RWC valid after CSN high or (DHIEN and DLOEN high)	0		ns
61	11, 12	CSN width high (intercycle)	t_{BCLK}		ns
62	12	Setup, data bus valid (write) to CSN low	0		ns
63	13	Hold, write data valid after CSN high or (DHIEN and DLOEN high)	0		ns
64[1]	13	Setup, IACKN low to BCLK low	10		ns
65	13	BCLK low to IRQN released			ns
66	13	DACKN low to IACKN high	0	50	ns
67[1]	13	Setup, IACKN high to BCLK low	10		ns
68	13	Hold, data bus valid after IACKN high	10		ns
69	13	IACKN high to data bus released		30	ns
70	13	IACKN high to DACKN released		25	ns

NOTES:

1. If the subject input signal meets this setup time, the IOP is guaranteed to recognize its new state at the subject edge of BCLK. If this setup time is not met, recognition may occur at the subject clock edge, or one BCLK later.
2. The maximum rating of this parameter should be as short as is consistent with device characterization, so as to maximize the compatibility of the IOP with processors that re-arbitrate and re-grant if BR is kept low after a first grant.
3. This parameter defines the number of clock cycles (wait states) between the BCLK falling edge at which CSN or IACKN is sampled and the falling edge from which the IOP responds with DACKN low, which is a function of the IOP's internal state and activity. For accesses to DMA processor registers when the IOP is idle, 3 BCLK cycles are required. For accesses to DUART registers when the IOP is idle, 5 BCLK cycles are required. If the IOP is internally active at the same time CSN or IACKN goes low, up to 11 BCLK cycles may be needed.

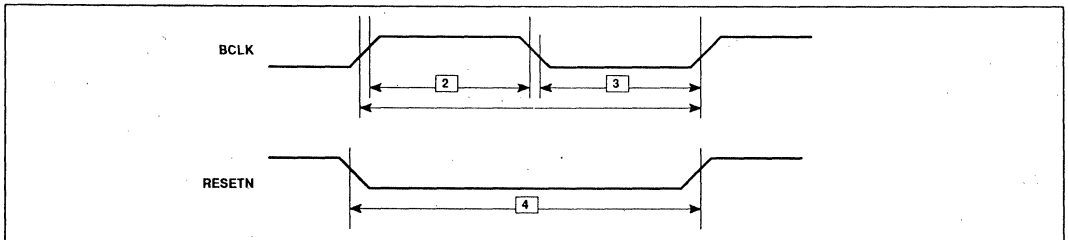


Figure 6. Clock and Reset Timing

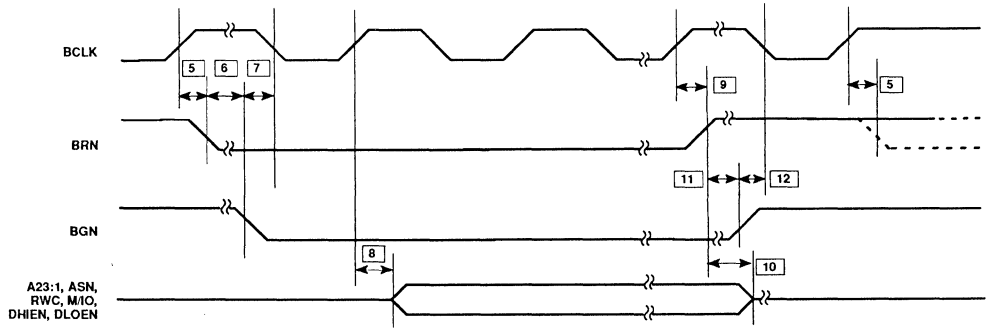


Figure 7. Two Wire Master Arbitration

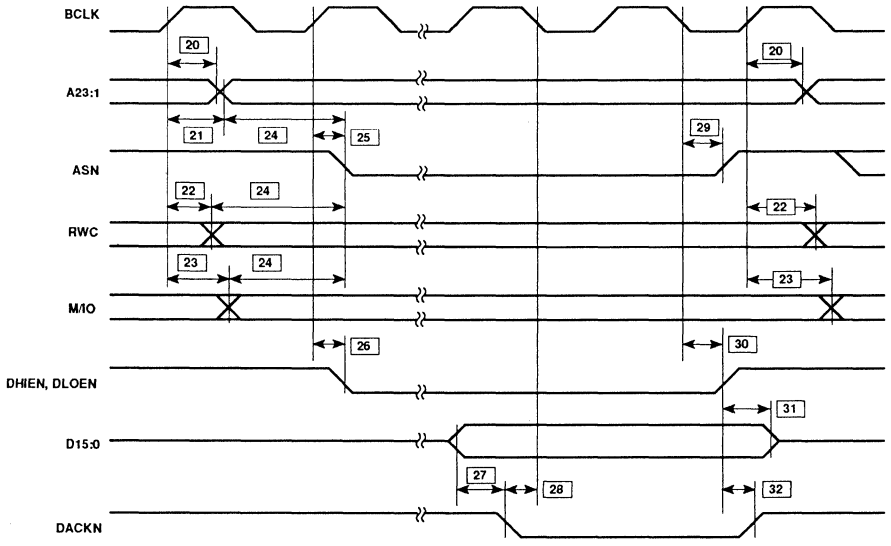


Figure 8. IOP Read From External Peripheral or Memory

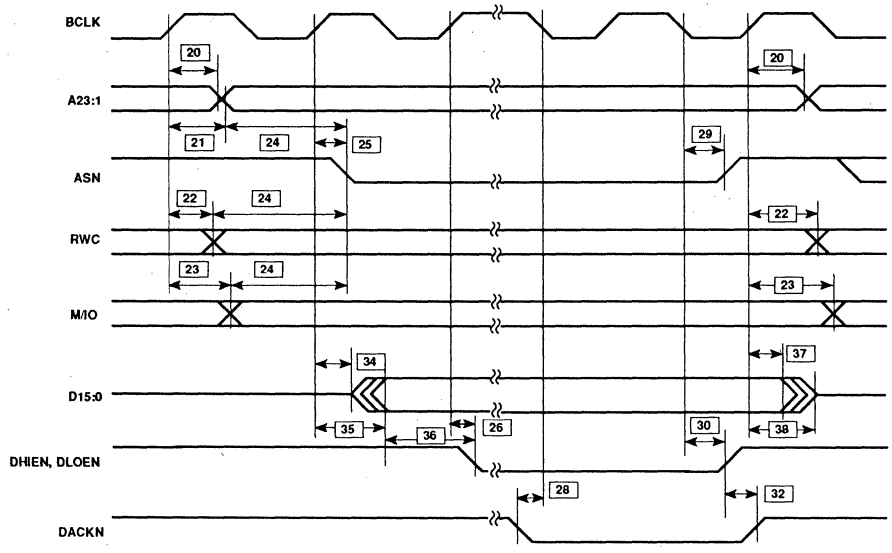


Figure 9. IOP Write to External Peripheral or Memory

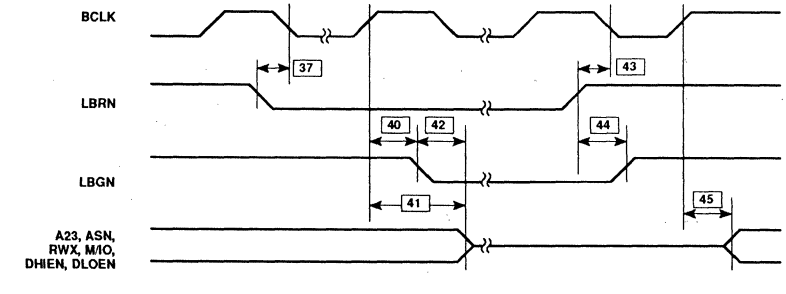


Figure 10. Dual Bus "Slave" Arbitration

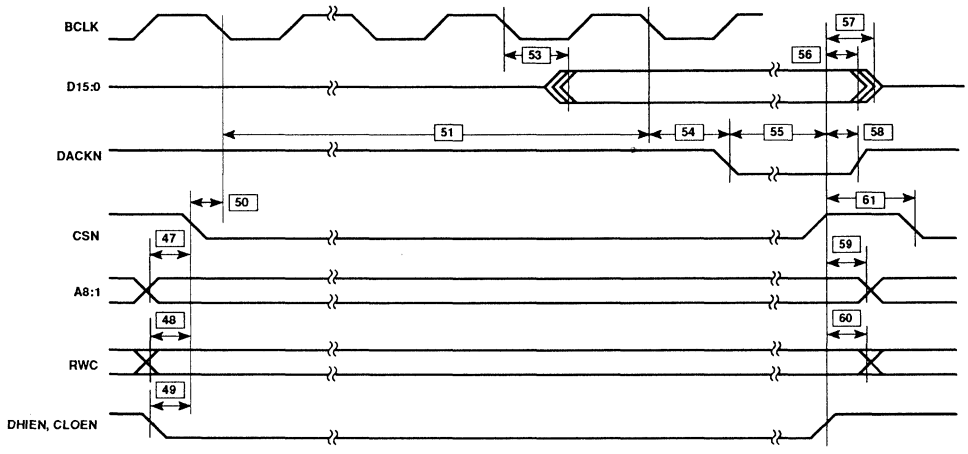


Figure 11. Host MPU Read from IOP

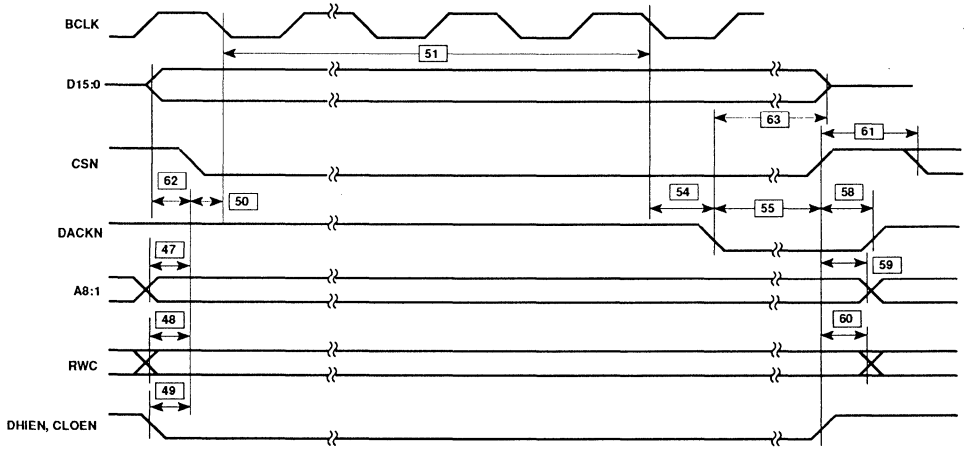


Figure 12. Host MPU Write to IOP

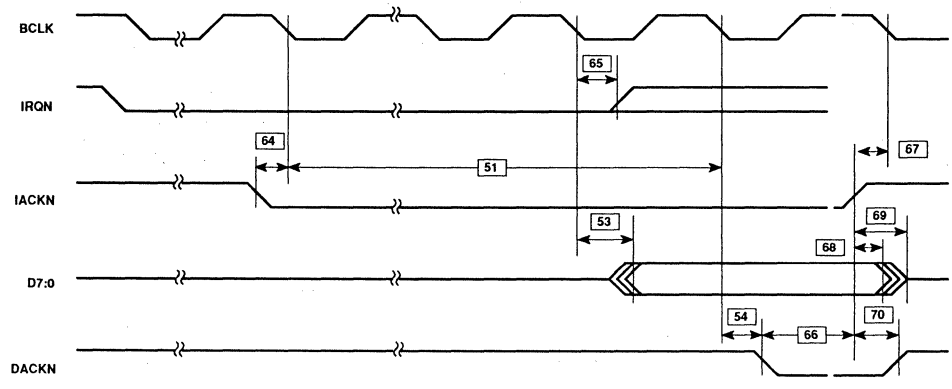


Figure 13. Interrupt Acknowledge Cycle by Host MPU

Section 3
Wired Data Communication Products

Data Communication Products

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Philips Components–Signetics

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Date of Issue	November 29, 1989
Status	Product Specification
Data Communication Products	

AM26LS30

Dual differential RS-422 party line/quad single-ended RS-423 line driver

DESCRIPTION

The AM26LS30 is a line driver designed for digital data transmission. A mode control input provides a choice of operation either as two differential line drivers which meet all the requirements of EIA Standard RS-422 or as four independent single-ended RS-423 line drivers.

In the differential mode, the outputs have individual 3-State controls. In the high impedance state, these outputs will not clamp the line over a common mode transmission line voltage of ±10V. A typical full duplex system consists of the AM26LS30 differential line driver and up to twelve AM26LS32 line receivers, or the AM26LS32 line receiver and up to thrity-two AM26LS30 differential drivers.

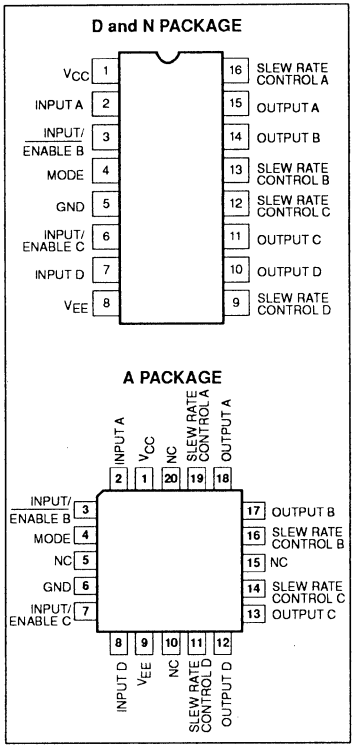
A slew control pin allows the use of an external capacitor to control slew rate for suppression of near-end cross-talk to receivers in the cable.

The AM26LS30 is constructed using high speed oxide isolated bipolar processing.

FEATURES

- Dual RS-422 line driver or quad RS-423 line driver
- Driver outputs do not clamp line with power off or in high impedance state
- Individual 3-State controls when used in differential mode
- Low I_{CC} and I_{EE} power consumption
- RS-422 differential mode: 35mW/ driver typ
- RS-423 single-ended mode: 26mW/ driver typ
- Individual slew rate control for each output
- 50Ω transmission line drive capability (RS-422 into virtual ground)
- Low current PNP inputs compatible with TTL, MOS and CMOS
- High capacitive load drive capability
- Exact replacement for DS16/3691
- High speed oxide isolated bipolar processing

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	AM26LS30CN
16-Pin Plastic SO	0°C to +70°C	AM26LS30CD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS30IN
16-Pin Plastic SO	–40°C to +85°C	AM26LS30ID
20-Pin PLCC	0°C to +70°C	AM26LS30CA

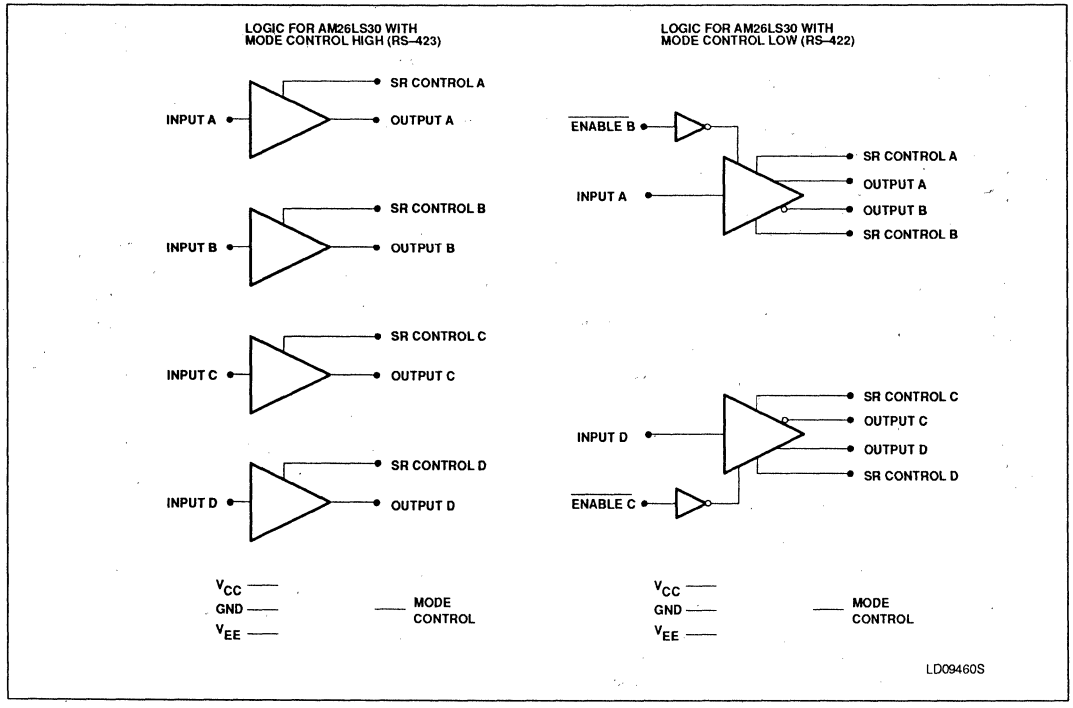
Dual differential RS-422 party/line quad single-ended RS-423 line driver

AM26LS30

FUNCTION TABLE

	INPUTS		OUTPUTS	
MODE	A(D)	B(C)	A(D)	B(C)
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

BLOCK DIAGRAM



Dual differential RS-422 party/line quad single-ended RS-423 line driver

AM26LS30

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage V+		6	V
V_{EE}	V–		–6	V
V_{IN}	Input voltage		–0.5V to V_{CC}	V
V_{OUT}	Output voltage (Power Off)		±13.5	V
T_A	Ambient temperature range	AM26LS30C	0 to +70	°C
		AM26LS30I	–40 to +85	°C
T_{STG}	Storage temperature range		–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)		300	°C
θ_{JA}	Thermal impedance			°C/W

PACKAGE POWER DISSIPATION DERATING TABLE

PACKAGE	POWER DISSIPATION AT T_A = 25°C	DERATING FACTOR ABOVE T_A
N	1,488mW	11.9mW/°C
D	1,262mW	10.1mW/°C

DC ELECTRICAL CHARACTERISTICS

Over the operating temperature range. The following conditions apply unless otherwise specified: AM26LS30C, T_A = 0 to 70°C, V_{CC} = 5.0V ±5%, V_{EE} = GND; AM26LS30I, T_A = –40 to +85°C, V_{CC} = 5.0V ±5%, V_{EE} = GND, RS–423 Connection Mode Voltage ≤2.0V.

SYMBOL[2]	PARAMETER	TEST CONDITIONS[3]		LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
V_O	Differential output	$R_L = \infty$	V_{IN} = 2.0V		3.6	6.0	V
$\overline{V_O}$	Voltage, $V_{A,B}$		V_{IN} = 0.8V		–3.6	–6.0	V
V_T	Differential output	R_L = 100Ω	V_{IN} = 2.0V	2.0	2.4		V
$\overline{V_T}$	Voltage, $V_{A,B}$		V_{IN} = 0.8V	–2.0	–2.4		V
V_{OS}, $\overline{V_{OS}}$	Common mode offset voltage	R_L = 100Ω			2.5	3.0	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in common mode output voltage	R_L = 100Ω			0.005	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in common mode offset voltage	R_L = 100Ω			0.005	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	R_L = 100Ω		4.0	4.8		V
V_{CMR}	Output voltage common mode range	$V_{\overline{ENABLE}}$ = 2.4V		±10			V
I_{XA}	Output leakage current	V_{CC} = 0V	V_{CMR} = 10V		0.5	20	µA
I_{XB}			V_{CMR} = 10V		–0.5	–20	µA
I_{OX}	Off-state (hi-Z) output current	V_{CC} = MAX	$V_{CMR} \leq$ 10V		0.5	20	µA
			$V_{CMR} \geq$ –10V		–0.5	–20	µA
I_{OX}	Off-state (hi-Z) output current	V_{CC} = MAX	$V_{CMR} \leq$ 5V		0.03	1	µA
			$V_{CMR} \geq$ –5V		–0.03	1	µA
I_{SA}, I_{SB}	Output short circuit current	V_{IN} = 2.4V	V_{OA} = 0V		–75	–150	mA
			V_{OB} = 6V		100	150	mA
		V_{IN} = 0.4V	V_{OA} = 0V		100	150	mA
			V_{OB} = 6V		–75	–150	mA

Dual differential RS-422 party/line quad single-ended RS-423 line driver

AM26LS30

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL[2]	PARAMETER	TEST CONDITIONS[3]	LIMITS			UNIT
			Min	Typ[1]	Max	
I_{CC}	Supply current			18	30	mA
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
I_{IH}	High level input current	V_{IN} = 2.4V		0.3	40	µA
		$V_{IN} \leq V_{CC}$		0.3	100	µA
I_{IL}	Low level input current	V_{IN} = 0.4V		–10	–200	µA
V_I	Input clamp voltage	I_{IN} = –12mA			–1.5	V

NOTES:
1. Typical limits are at V_{CC} = 5V, V_{EE} = GND, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-422 where applicable.
3. R_L connected between each output and its complement.

AC ELECTRICAL CHARACTERISTICS EIA RS-423 Connection, V_{CC} = 5.0V, V_{EE} = –5V, Mode = 2.4V, T_A = 25°C.

SYMBOL[2]	PARAMETER	TEST CONDITIONS[3]	LIMITS			UNIT
			Min	Typ[1]	Max	
t_R	Rise time	R_L = 100Ω, C_L = 500pF, Figure 1		80	200	ns
t_F	Fall time	R_L = 100Ω, C_L = 500pF, Figure 1		110	200	ns
t_{PDH}	Output propagation delay	R_L = 100Ω, C_L = 500pF, Figure 1		90	200	ns
t_{PDL}	Output propagation delay	R_L = 100Ω, C_L = 500pF, Figure 1		95	200	ns
t_{PLZ}	Output enable to output	R_L = 450Ω, C_L = 500pF, Figure 2			0.8	ns
t_{PHZ}				60	350	ns
t_{PZL}	Output enable to output	R_L = 450Ω, C_L = 500pF, Figure 2		140	350	ns
t_{PZH}				120	300	ns

NOTES:
1. Typical limits are at V_{CC} = 5V, V_{EE} = GND, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-422 where applicable.
3. R_L connected between each output and its complement.

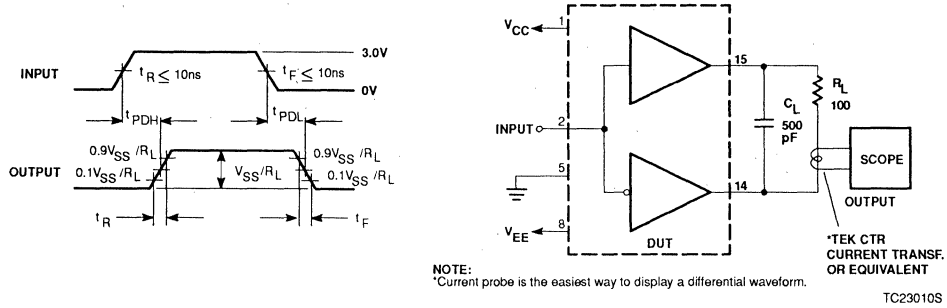


Figure 1. Switching Time Waveforms and AC Test Circuits for EIA RS-422 Connection

Dual differential RS-422 party/line quad single-ended RS-423 line driver

AM26LS30

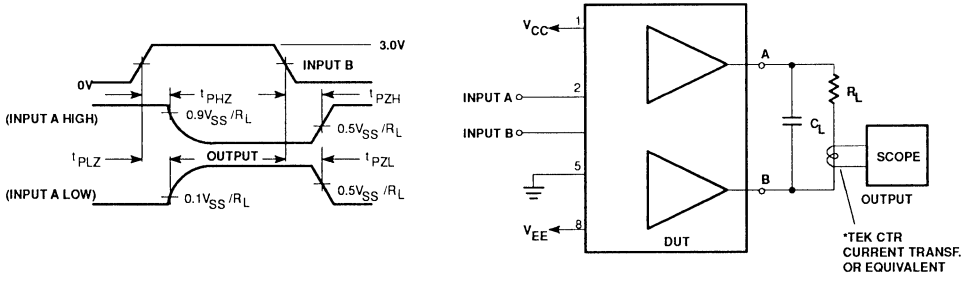


Figure 2. 3-State Delays

DC ELECTRICAL CHARACTERISTICS

Over the operating temperature range. The following conditions apply unless otherwise specified: AM26LS30C, T_A = 0 to 70°C, V_{CC} = 5.0V ±5%, V_{EE} = GND; AM26LS30I, T_A = –40 to +85°C, V_{CC} = 5.0V ±5%, V_{EE} = GND, RS-422 Connection Mode Voltage ≤0.8V.

SYMBOL[2]	PARAMETER	TEST CONDITIONS		LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
V_O	Output voltage	$R_L = \infty$[3] $\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$	V_{IN} = 2.4V	4.0	4.1	6.0	V
$\overline{V_O}$		= 4.75V	V_{IN} = 0.4V	–4.0	–4.2	–6.0	V
V_T	Output voltage	R_L = 450Ω $\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$	V_{IN} = 2.4V	3.6	3.9		V
$\overline{V_T}$		= 4.75V	V_{IN} = 0.4V	–3.6	–3.9		V
$\lvert V_T\rvert - \lvert \overline{V_T}\rvert$	Output unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, R_L = 450Ω			0.05	0.4	V
I_{X+}	Output leakage power off	$V_{CC} = V_{EE}$ = 0	V_O = 6V		0.5	20	µA
I_{X-}			V_O = –6V		–0.5	–20	µA
I_{S+}	Output short circuit current	V_O = 0V	V_{IN} = 2.4V		–75	–150	mA
I_{S-}			V_{IN} = 0.4V		100	150	mA
I_{SLEW}	Slew control current	$V_{SLEW} = V_{EE}$ + 0.9V			±125	20	µA
I_{CC}	Positive supply current	V_{IN} = 0.4V, $R_L = \infty$			18	30	mA
I_{EE}	Negative supply current	V_{IN} = 0.4V, $R_L = \infty$			–8	–22	mA
V_{IH}	High level input voltage			2.0			V
V_{IL}	Low level input voltage					0.8	V
I_{IH}	High level intput current	V_{IN} = 2.4V			0.3	40	µA
		$V_{IN} \le V_{CC}$			0.3	100	µA
I_{IL}	Low level input current	V_{IN} = 0.4V			–10	–200	µA
V_I	Input clamp voltage	I_{IN} = –12mA				–1.5	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, V_{EE} = –5V, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9V minimum and –3.9V minimum at –40°C.

Dual differential RS-422 party/line quad single-ended RS-423 line driver

AM26LS30

AC ELECTRICAL CHARACTERISTICS

EIA RS-422 Connection, V_{CC} = 5.0V, V_{EE} = GND, Mode = 0.4V, T_A = 25°C.

SYMBOL[2]	PARAMETER	TEST CONDITIONS[3]		LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
t_R	Rise time	R_L = 450Ω, C_L = 500pF, Figure 3	C_C = 0pF		110	300	ns
			C_C = 50pF		3.0		µs
t_F	Fall time	R_L = 450Ω, C_L = 500pF, Figure 3	C_C = 0pF		120	300	ns
			C_C = 50pF		3.0		µs
S_{RC}	Slew rate coefficient	R_L = 450Ω, C_L = 500pF, Figure 3			0.06		µs/pF
t_{PDH}	Output propagation delay	R_L = 450Ω, C_L = 500pF, Figure 3, C_C = 0pF			110	300	ns
t_{PDL}	Output propagation delay	R_L = 450Ω, C_L = 500pF, Figure 3, C_C = 0pF			120	300	ns

NOTES:
1. Typical limits are at V_{CC} = 5.0V, V_{EE} = –5V, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9V minimum and –3.9V minimum at –40°C.

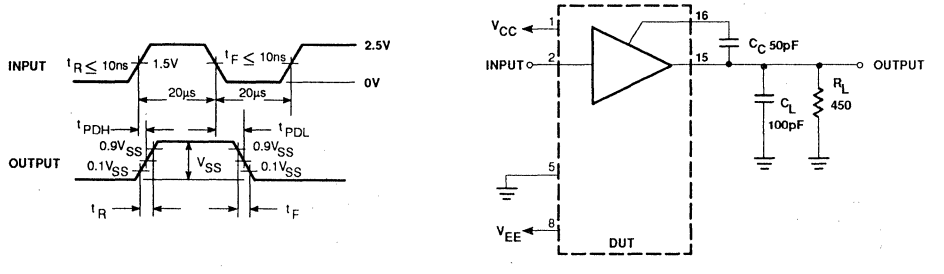


Figure 3. Switching Time Waveforms and AC Test Circuits for EIA RS-423 Connection

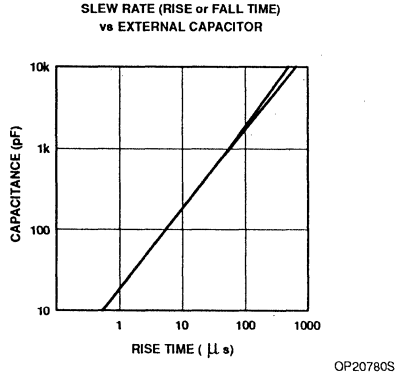


Figure 4.

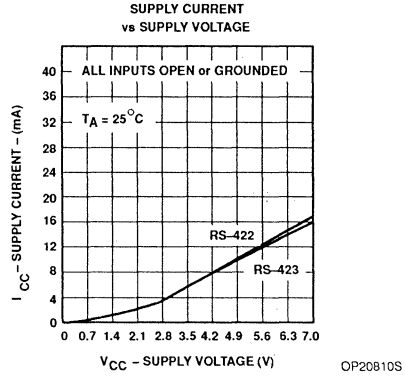


Figure 5.

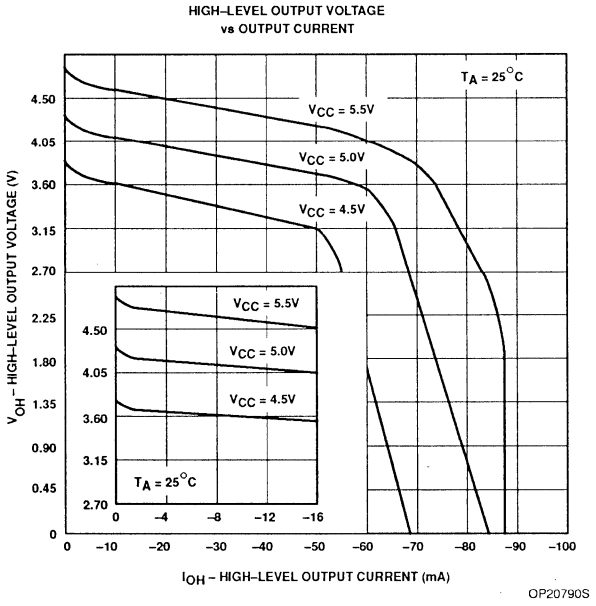


Figure 6.

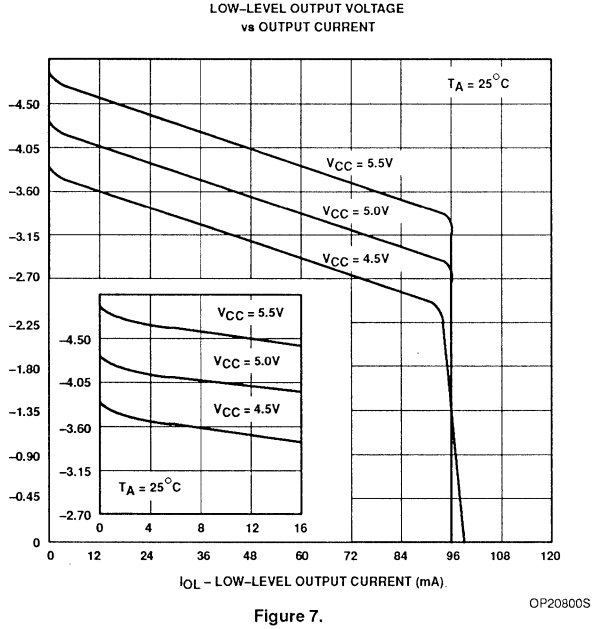


Figure 7.

Philips Components–Signetics

Document No.	853–1272
ECN No.	93196
Date of Issue	May 5, 1988
Status	Product Specification
Data Communication Products	

AM26LS31

Quad high-speed differential line driver

DESCRIPTION

The AM26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The AM26LS31 meets all the requirements of EIA standard RS-422 and Federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The circuit provides an enable and disable function common to all four drivers. The AM26LS31 features 3-State outputs and logical ORed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The AM26LS31 is constructed using advanced Low Power Schottky processing.

FEATURES

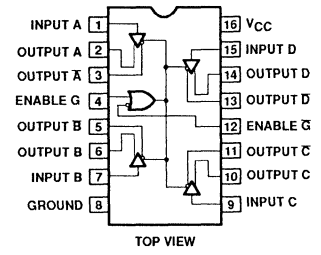
- Output skew of 2.0ns typical
- Input to output delay: 12ns
- Operation from single +5V
- 16-pin DIP and SO packages
- Four line drivers in one package
- Output short-circuit protection
- Complementary outputs
- Meets EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low power Schottky processing
- Outputs won't load line when V_{CC} = 0V

APPLICATIONS

- Data communications equipment
- Computer peripherals
- Workstations
- Automatic test equipment

PIN CONFIGURATION

D, F, and N Packages



TOP VIEW

FUNCTION TABLE (Each Driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	A	$\overline{A}$
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

NOTES:
H = High level
L = Low level
X = Irrelevant
Z = High-impedance (OFF)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	AM26LS31CN
16-Pin SO	0°C to +70°C	AM26LS31CD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS31IN
16-Pin SO	–40°C to +85°C	AM26LS31ID
16-Pin Plastic DIP	–55°C to +125°C	AM26LS31MN

Quad high-speed differential line driver | AM26LS31

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, T_A = –55 to +125°C for AM26LS31MF and AM26LS31MN;
V_{CC} = 5V ±5%, T_A = –40 to +85°C for AM26LS31IN and AM26LS31ID;
V_{CC} = 5V ±5%, T_A = 0 to +70°C for AM26LS31CN and AM26LS31CD,
unless otherwise specified.

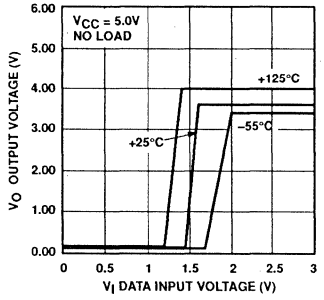
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
V_{OH}	Output High voltage	V_{CC} = Min., I_{OH} = –20mA	2.5	3.0		V
V_{OL}	Output Low voltage	V_{CC} = Min., I_{OL} = 20mA		0.3	0.5	V
V_{IH}	Input High voltage	V_{CC} = Min.	2.0			V
V_{IL}	Input Low voltage	V_{CC} = Max.			0.8	V
I_{IL}	Input Low current	V_{CC} = Max., V_{IN} = 0.4V		–0.26	–0.36	mA
I_{IH}	Input High current	V_{CC} = Max., V_{IN} = 2.7V		0.001	20	µA
I_I	Input reverse current	V_{CC} = Max., V_{IN} = 7.0V		0.001	0.1	mA
I_O	OFF-state (high-impedance) output current	V_{CC} = Max., V_O = 5.5V V_O = 0.5V		0.6 –0.050	20 –20	µA µA
V_I	Input clamp voltage	V_{CC} = Min., I_{IN} = –18mA		–0.8	–1.5	V
I_{SC}	Output short-circuit current	V_{CC} = Max.	–30		–150	mA
I_{CC}	Power supply current	V_{CC} = Max; all outputs disabled		40	80	mA
t_{PLH}	Input to output	T_A = 25°C, load[2]		9	20	ns
t_{PHL}	Input to output	T_A = 25°C, load[2]		9	20	ns
SKEW	Output to output	T_A = 25°C, load[2]		2	6	ns
t_{LZ}	Enable to output	T_A = 25°C, C_L = 10pF		17	35	ns
t_{HZ}	Enable to output	T_A = 25°C, C_L = 10pF		12	30	ns
t_{ZL}	Enable to output	T_A = 25°C, load[2]		14	45	ns
t_{ZH}	Enable to output	T_A = 25°C, load[2]		12	40	ns

NOTES:
1. All typical values are T_A = +25°C; V_{CC} = 5.0V.
2. C_L = 30pF; V_{IN} = 1.3V to V_{OUT} = 1.3V; V_{PULSE} = 0V to 3.0V.

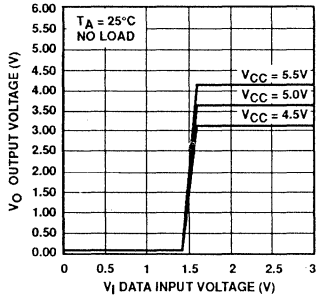
Quad high-speed differential line driver | AM26LS31

TYPICAL PERFORMANCE CHARACTERISTICS

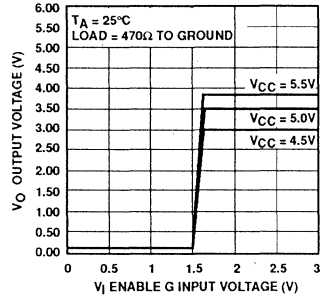
Output Voltage vs Data Input Voltage



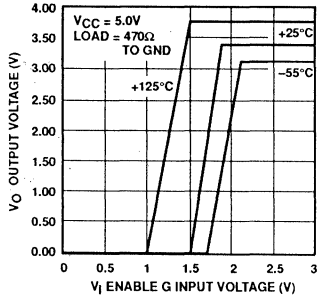
Output Voltage vs Data Input Voltage



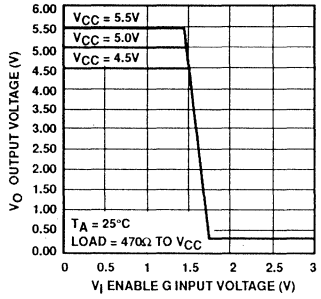
Output Voltage vs Enable G Input Voltage



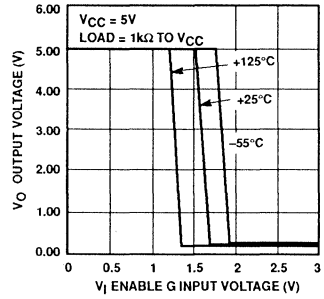
Output Voltage vs Enable G Input Voltage



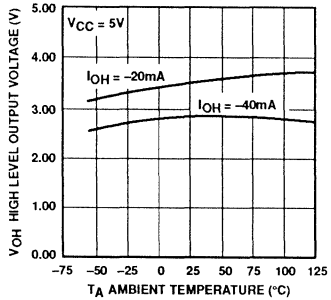
Output Voltage vs Enable G Input Voltage



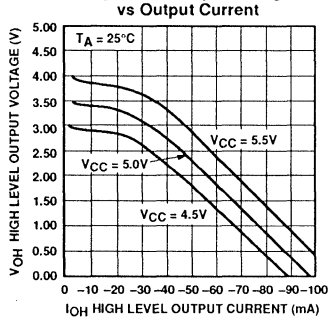
Output Voltage vs Enable G Input Voltage



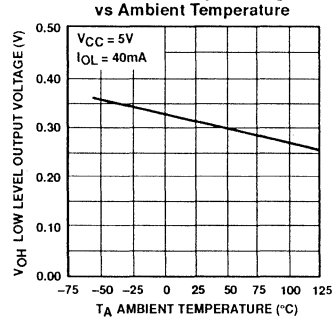
High Level Output Voltage vs Ambient Temperature



High Level Output Voltage vs Output Current



Low Level Output Voltage vs Ambient Temperature



Philips Components–Signetics

Document No.	853–1520
ECN No.	01085
Date of Issue	November 15, 1990
Status	Product Specification
Data Communication Products	

AM26LS32/AM26LS33

Quad high-speed differential line receivers

DESCRIPTION

The AM26LS32 and AM26LS33 are quad line receivers with the AM26LS32 designed to meet all of the requirements of RS-422 and RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The AM26LS32 features an input sensitivity of ±200mV over the common mode input range of ±7V.

The AM26LS33 features an input sensitivity of ±500mV over the common mode input voltage range of ±15V.

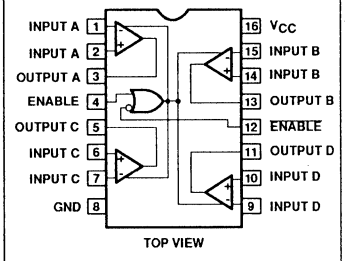
The AM26LS32 and AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-State outputs with 8mA sink capability and incorporate a fail-safe input-output relationship which forces the outputs high when the inputs are open.

FEATURES

- Input voltage range of 15V (differential or common mode) on AM26LS33; 7V (differential or common mode) on AM26LS32
- ±0.2V sensitivity over the input voltage range on AM26LS32
- ±0.5V sensitivity on AM26LS33
- 6kΩ minimum input impedance
- The AM26LS32 meets all the requirements of RS-422 and RS-423
- Operation from single +5V supply
- Fail safe input-output relationship. Output always high when inputs are open
- 3-State drive, with choice of complementary output enables, for receiving directly onto a data bus
- 3-State outputs disabled during power up and power down

PIN CONFIGURATION

F, D and N Packages



TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	AM26LS32CN
16-Pin SO	0°C to +70°C	AM26LS32CD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS32IN
16-Pin SO	–40°C to +85°C	AM26LS32ID
16-Pin Plastic DIP	–55°C to +125°C	AM26LS32MN
16-Pin Plastic DIP	0°C to +70°C	AM26LS33CN
16-Pin SO	0°C to +70°C	AM26LS33CD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS33IN
16-Pin SO	–40°C to +85°C	AM26LS33ID
16-Pin Plastic DIP	–55°C to +125°C	AM26LS33MN

Quad high-speed differential line receivers | AM26LS32/AM26LS33

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	7	V
V_{IN}	Power supply	7	V
	Output sink current	50	mA
	Common mode range	±25	V
V_{TH}	Differential input voltage	±25	V
T_{STG}	Storage temperature range	–65 to +150	°C

DISSIPATION OPERATING TABLE

PACKAGE	POWER DISSIPATION	DERATING FACTOR	ABOVE T_A
F	1,524mW	12.19mW/°C	25°C
N	1,275mW	10.2mW/°C	25°C
D	1,262W	10.1mW/°C	25°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10% for AM26LS32/33MX, V_{CC} = 5.0V ±5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS AM26LS32/33 Min	Typ[1]	Max	UNIT
V_{TH}	Differential input voltage	$V_{OUT} = V_{OL}$ or V_{OH} AM26LS32, $-7V \le V_{CM} \le +7V$		–0.2	0.06	0.2	V
		AM26LS33, $-15V \le V_{CM} \le +15V$		–0.5	0.06	0.5	V
R_{IN}	Input resistance	$-15V \le V_{CM} \le +15V$ (One input AC ground)		6.0	9.8		kΩ
I_{IN}	Input current (under test)	$V_{IN} = +15V$ Other input $-10V \le V_{IN} \le +15V$				2.3	mA
I_{IN}	Input current (under test)	$V_{IN} = -15V$ Other input $+10V \le V_{IN} \le -15V$				–2.8	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., I_{OH} = –440µA ΔV_{IN} = +1.0V $V_{\overline{ENABLE}}$ = 0.8V	Com'l	2.7	3.4		V
			Mil	2.5	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = Min., $V_{\overline{ENABLE}}$ = 0.8V ΔV_{IN} = +1.0V	I_{OL} = 4.0mA		0.3	0.4	V
			I_{OL} = 8.0mA			0.45	V
V_{IL}	Enable LOW voltage					0.8	V
V_{IH}	Enable HIGH voltage			2.0			V
V_I	Enable clamp voltage	V_{CC} = Min., I_{IN} = –18mA				–1.5	V
I_O	Off state (high impedance) output current	V_{CC} = Max.	V_O = 2.4V			20	µA
			V_O = 0.4V			–20	µA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 5.0V ±10% for AM26LS32/33MX, V_{CC} = 5.0V ±5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

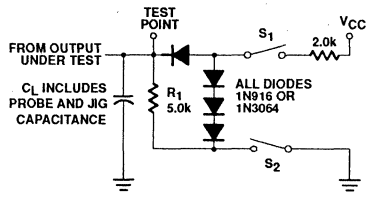
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS AM26LS32/33 Min	Typ[1]	Max	UNIT
I_{IL}	Enable LOW current	V_{IN} = 0.4V			–0.2	–0.36	mA
I_{IH}	Enable HIGH current	V_{IN} = 2.7V			0.5	20	µA
I_I	Enable input HIGH current	V_{IN} = 5.5V			1	100	µA
I_{SC}	Output short circuit current	V_{CC} = Max., ΔV_{IN} = +1V, V_{OUT} = 0V		–15	–60	–85	mA
I_{CC}	Power supply current	V_{CC} = Max.; All V_{IN} = GND outputs disabled			52	70	mA
V_{HYST}	Input hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V	AM26LS32		120		mV
			AM26LS33		120		mV
t_{PLH}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			10	25	ns
t_{PHL}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			10	25	ns
t_{LZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			15	30	ns
t_{HZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			12	22	ns
t_{ZL}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			8	22	ns
t_{ZH}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF			9	22	ns

NOTE:
1. All typical values are T_A = 25°C, V_{CC} = 5.0V.

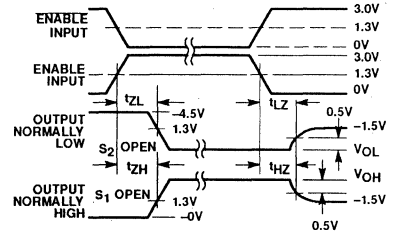
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES E	ENABLES $\overline{E}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	X	L	L
	H	X	X
X	L	H	Z

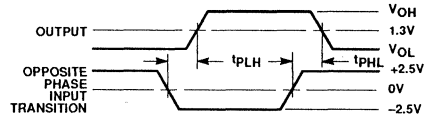
NOTES:
H = High level, L = Low level, X = Irrelevant
Z = High impedance (off), ? = Indeterminate
E = Enable, $\overline{E}$ = $\overline{\text{Enable}}$



Load Test Circuit for 3-State Outputs



Enable and Disable Tmes[2, 3, 4]



Propagation Delay[1, 4]

NOTES:

1. Diagram shown for $\overline{\text{Enable}}$ Low.
2. Enable is tested with $\overline{\text{Enable}}$ High; $\overline{\text{Enable}}$ is tested with Enable Low.
3. S_1 and S_2 of Load Circuit are closed except where shown.
4. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

Philips Components–Signetics

Document No.	
ECN No.	
Date of Issue	July 20, 1990
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Data Communication Products	

AM26LS32B

Quad high-speed differential line receivers

DESCRIPTION

The AM26LS32B is a quad line receiver designed to meet all of the requirements of RS-422 and RS-423, CCITT V.10 and V.11 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The AM26LS32B features an input sensitivity of ±100mV over the common mode input voltage range of 0V to +5V and ±200mV over the common mode input voltage range of –7V to +12V.

The AM26LS32B guarantees a minimum hysteresis and propagation delay skew resulting in a higher noise margin and better system performance.

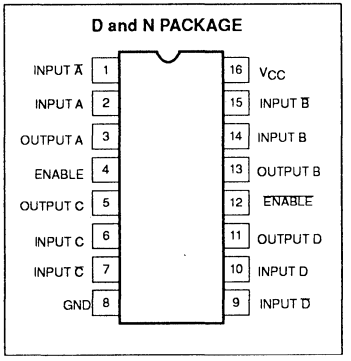
The AM26LS32B provides an enable and disable function common to all four receivers. It features 3-State outputs with 24mA sink capability and incorporates a fail-safe input-output relationship which keeps the outputs high when the inputs are open.

FEATURES

- ±100mV sensitivity over the input range of 0V to 5V
- ±200mV sensitivity over the V_{CM} range
- Typical input voltage hysteresis of 120mV
- 3V maximum open circuit voltage
- Three state outputs disabled power up and power down
- All AC and DC parameters guaranteed over operating temp range
- Single +5V supply
- Advance low-power Schottky processing

PIN CONFIGURATION

D and N PACKAGE



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	AM26LS32BCN
16-Pin SO	0°C to +70°C	AM26LS32BCD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS32BIN
16-Pin SO	–40°C to +85°C	AM26LS32BID
16-Pin Plastic DIP	–55°C to +125°C	AM26LS32BMN

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	7	V
V_{IN}	Enable voltage	7	V
	Output sink current	50	mA
	Common mode range	±25	V
V_{TH}	Differential input voltage	±30	V
T_{STG}	Storage temperature range	–55 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	300	°C
θ_{JA}	Thermal impedance		°C/W

PACKAGE POWER DISSIPATION DERATING TABLE

PACKAGE	POWER DISSIPATION AT T_A = 25°C	DERATING FACTOR ABOVE T_A
N	1,275mW	10.2mW/°C
D	1,262mW	10.1mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10% for AM26LS32BMX, V_{CC} = 5.0V ±5% for AM26LS32BCX over operating temperature range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{TH}	Differential input voltage	$V_{OUT} = V_{OL}$ or V_{OH}	$0V \le V_{CM} \le 5V$	–100		+100	mV
			$-7V \le V_{CM} \le +12V$	–200		+200	mV
R_{IN}	Input resistance	$-15V \le V_{CM} \le +15V$ (one input AC ground)		6.0			kΩ
I_{IN}	Input current (under test)	$V_{IN} = +15V$ Other input $-15V \le V_{IN} \le +15V$				2.3	mA
I_{IN}	Input current (under test)	$V_{IN} = -15V$ Other input $+15V \le V_{IN} \le -15V$		–2.8			mA
V_{OH}	Output HIGH voltage	V_{CC} = min., ΔV_{IN} = +1.0V	I_{OH} = –12mA	2.0			V
		$V_{\overline{EN}}$ = 0.8V	I_{OH} = –1mA	2.4			V
V_{OL}	Output LOW voltage	V_{CC} = min., ΔV_{IN} = –1.0V	I_{OH} = 16mA			0.4	V
		$V_{\overline{EN}}$ = 0.8V	I_{OH} = 24mA			0.5	V
V_{IL}	Enable LOW voltage	V_{CC} = max				0.8	V
V_{IH}	Enable HIGH voltage			2.0			V
V_I	Enable clamp voltage	V_{CC} = min, I_{IN} = –1.8mA		–1.5			V
I_O	Off state (high impedance) output current	V_{CC} = max	V_O = 2.4V			20	µA
			V_O = 0.4V			–20	µA
I_{IL}	Enable LOW current	V_{IN} = 0.4V				–0.36	mA
I_{IH}	Enable HIGH current	V_{IN} = 2.7V				20	µA
I_I	Enable input HIGH current	V_{IN} = 5.5V				100	µA

Quad high-speed differential line receivers | AM26LS32B

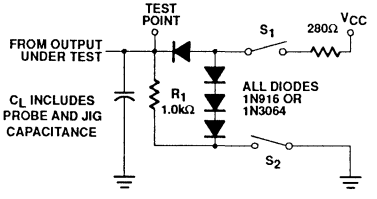
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_{SC}	Output short circuit current	V_{CC} = max, ΔV_{IN} = +1V, V_{OUT} = GND	–30		–120	mA
I_{CC}	Power supply current	V_{CC} = max, all V_{IN} = GND outputs disabled			70	mA
V_{HYST}	Input hysteresis	V_{CC} = 5.0V, V_{CM} = 0V	80		200	mV
V_{IOC}	Open circuit input voltage		1		3	V

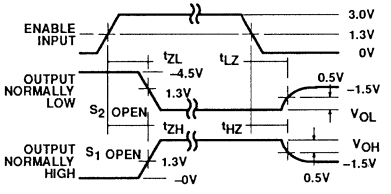
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			ROOM TEMPERATURE[2]		COMMERCIAL/ MILITARY[1]		
			Typ	Max	Typ	Max	
t_{PLH}	Propagation delay, input to output	C_L = 50pF (see test circuit)		21		26	ns
t_{PHL}				21		26	ns
t_{SKEW}	Propagation delay skew, $t_{PLH} - t_{PHL}$			3.0		4.0	ns
t_{ZL}	Output enable time, EN to OUTPUT			22		33	ns
t_{ZH}				16		22	ns
t_{LZ}	Output disable time, EN to OUTPUT	C_L = 5pF (see test circuit)		18		27	ns
t_{HZ}				18		27	ns

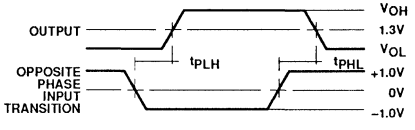
NOTES:
1. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
2. V_{CC} = 5V



SWITCHING TEST CIRCUIT FOR THREE STATE OUTPUTS



ENABLE AND DISABLE TIMES (Notes 2 and 3)



PROPAGATION DELAY (Notes 1 and 3)

NOTES:
1. Diagram thown for Enable LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

Figure 1.

Philips Components–Signetics

Document No.	853–1430
ECN No.	99588
Date of Issue	May 15, 1990
Status	Product Specification
Data Communication Products	

MC145406

EIA-232-D/V.28 driver/receiver

DESCRIPTION

The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of standards EIA-232-D and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate limited output, 300Ω power-off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25V while presenting 3 to 7kΩ impedance. Hysteresis in the receiver aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-D and V.28 applications.

FEATURES

Drivers

- ±5 to ±12V supply range
- 300Ω power-off source impedance
- Output current limiting
- TTL compatible
- Maximum slew rate = 30V/μs

Receivers

- ±25V input voltage range over the full supply range
- 3 to 7kΩ input impedance
- Hystersis on input switchpoint

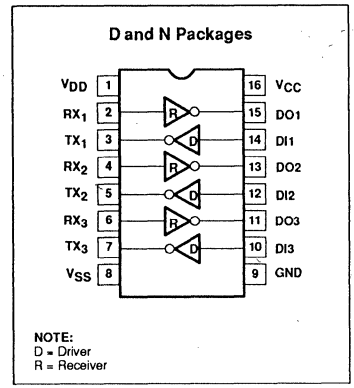
General

- Very low supply currents for long battery life
- Operation is independent of power supply sequencing

APPLICATIONS

- Modem interface
- Voice/data telephone interface
- Lap-top computers
- UART interface

PIN CONFIGURATION

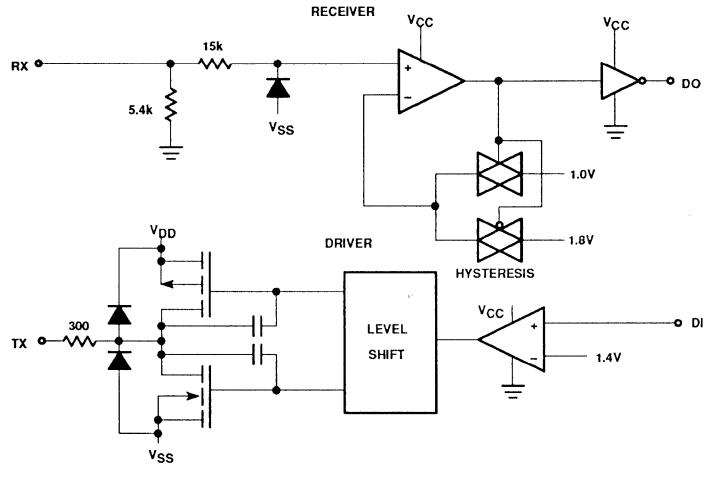


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	MC145406N
16-Pin SOL	0°C to +70°C	MC145406D

EIA-232-D/V.28 driver/receiver | MC145406

BLOCK DIAGRAM



PIN NO.	SYMBOL	PIN DESCRIPTION
1	V_{DD}	**Positive power supply**. The most positive power supply pin, which is typically 5 to 12 volts.
8	V_{SS}	**Negative power supply.** The most negative power supply pin, which is typically –5 to –12 volts.
16	V_{CC}	**Digital power supply**. The digital supply pin, which is connected to the logic power supply (maximum +5.5V).
9	GND	**Ground.** Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (Pin 7) as well as to the logic power supply ground.
2, 4, 6	RX_1, RX_2, RX_3	**Receive Data Input.** These are the EIA-232-D receive signal inputs whose voltages can range from +25 to –25V. A voltage between +3 and +25 is decoded as a space and causes the corresponding DO pin to swing to ground (0V); a voltage between –3 and –25V is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8V above ground, and includes 800mV of hysteresis for noise rejection. The nominal input impedance is 5kΩ. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.
11, 13, 15	DO1, DO2, DO3	**Data Output.** These are the receiver digital output pins, which swing from V_{CC} to GND. A space on the RX pin causes DO to produce a logic zero; a mark produces a logic one. Each output pin is capable of driving one LSTTL input load.
10, 12, 14	DI1, DI2, DI3	**Data Input.** These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4V above ground. However, 5V CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and GND.
3, 5, 7	TX1, TX2, TX3	**Transmit Data Output.** These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corresponding TX output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30V/μs. When the MC145406 is off (V_{DD} = V_{SS} = V_{CC} = GND), the minimum output impedance is 300Ω.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +6.0	V
V_{DD}	Supply voltage	–0.5 to +13.5	V
V_{SS}	Supply voltage	+0.5 to –13.5	V
V_{IR}	Input voltage range RX_{1-3} inputs DI_{1-3} inputs	 $(V_{SS} - 15)$ to $(V_{DD} + 15)$ –0.5 to $(V_{CC} + 0.5)$	V
	DC current per pin	±100	mA
P_D	Power dissipation (package)	1.0	W
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	–65 to +150	°C
θ_{JA}	Thermal impedance N package D package	80 105	°C/W

NOTE: This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{DD} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the RX pin should be constrained to ±25V, and TX should be constrained to $V_{SS} \leq V_{TX1-3} \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for RX).

DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
DC supply voltage						
V_{DD}			4.5	5 to 12	13.2	V
V_{SS}			–4.5	–5 to –12	–13.2	V
V_{CC}			4.5	5.0	5.5	V
Quiescent supply current (outputs unloaded, inputs low)						
I_{DD}		V_{DD} = +12V		20	400	µA
I_{SS}		V_{SS} = –12V		280	600	µA
I_{CC}		V_{CC} = +5V		260	450	µA

RECEIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{DD} = +5 to +12V; V_{SS} = –5 to –12V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
V_{ON}	Input turn-on threshold	RX_{1-3}	$V_{DO1-3} = V_{OL}$, V_{CC} = 5.0V ±5%	1.35	1.80	2.35	V
V_{OFF}	Input turn-off threshold	RX_{1-3}	$V_{DO1-3} = V_{OH}$, V_{CC} = 5.0V ±5%	0.75	1.00	1.25	V
V_{ON}–V_{OFF}	Input threshold hysteresis	RX_{1-3}	V_{CC} = 5.0V ±5%	0.6	0.8		V
R_{IN}	Input resistance	RX_{1-3}	$(V_{SS}–15V) \leq V_{RX1-3} \leq (V_{DD}+15V)$	3.0	5.0	7.0	kΩ
V_{OH}	High level output voltage	DO_{1-3}	I_{OH} = –20µA, V_{CC} = +5.0V	4.9	5.0		V
	V_{RX1-3} = –3V to $(V_{SS}–15V)$[1]		I_{OH} = –1mA, V_{CC} = +5.0V	3.8	4.4		V
V_{OL}	Low level output voltage	DO_{1-3}	I_{OL} = +20µA, V_{CC} = +5.0V		0.005	0.1	V
	V_{RX1-3} = +3V to $(V_{DD}+15V)$[1]		I_{OL} = +2mA, V_{CC} = +5.0V		0.15	0.5	V
			I_{OL} = +4mA, V_{CC} = +5.0V		0.3	0.7	V

NOTE:
1. This is the range of input voltages as specified by EIA-232-D to cause a receiver to be in the high or low logic state.

DRIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
V_{IL}	Digital input voltage	DI_{1-3}	Logic 0			0.8	V
V_{IH}	Digital input voltage	DI_{1-3}	Logic 1	2.0			V
I_{IN}	Input current	DI_{1-3}	$V_{DI1-3} = V_{CC}$			±1.0	µA
V_{OH}	Output high voltage V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = –5.0V	3.5	4.1		V
			V_{DD} = +6.0V, V_{SS} = –6.0V	4.3	5.0		V
			V_{DD} = +12.0V, V_{SS} = –12.0V	9.2	10.4		V
V_{OL}	Output low voltage[1] V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = –5.0V	–4.0	–4.3		V
			V_{DD} = +6.0V, V_{SS} = –6.0V	–4.5	–5.2		V
			V_{DD} = +12.0V, V_{SS} = –12.0V	–10.0	–10.3		V
	Off source resistance Figure 1	TX_{1-3}	$V_{DD} = V_{SS}$ = GND = 0V, V_{TX1-3} = ±2.0V	300			Ω
I_{SC}	Output short-circuit current V_{DD} = +12.0V, V_{SS} = –12.0V	TX_{1-3}	TX_{1-3} shorted to GND[2]		±22	+60	mA
			TX_{1-3} shorted to ±15.0V[3]		±60	±100	mA

NOTE:
1. The voltage specifications are in terms of absolute values.
2. Specification is for one TX output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.
3. This condition could exceed package limitations.

SWITCHING CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; V_{CC} = +5V ±5%, unless otherwise specified.
(See Figures 2 and 3)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Drivers							
t_{PLH}	Propagation delay time	TX_{1-3}	Low-to-High R_L = 3kΩ, C_L = 50pF		300	500	ns
t_{PHL}	Propagation delay time	TX_{1-3}	High-to-Low R_L = 3kΩ, C_L = 50pF		300	500	ns
SR	Output slew rate (minimum load)	TX_{1-3}	R_L = 7kΩ, C_L = 0pF, V_{DD} = 6 to 12.0V, V_{SS} = –6 to –12V		±6	±30	V/µs
	Output slew rate (maximum load)	TX_{1-3}	R_L = 7kΩ, C_L = 2500pF, V_{DD} = 12V, V_{SS} = –12V		±3.0		V/µs
Receivers (C_L = 50pF)							
t_{PLH}	Propagation delay time	DO_{1-3}	Low-to-High		150	425	ns
t_{PHL}	Propagation delay time	DO_{1-3}	High-to-Low		150	425	ns
t_R	Output rise time	DO_{1-3}			120	400	ns
t_F	Output fall time	DO_{1-3}			40	100	ns

EIA-232-D/V.28 driver/receiver | MC145406

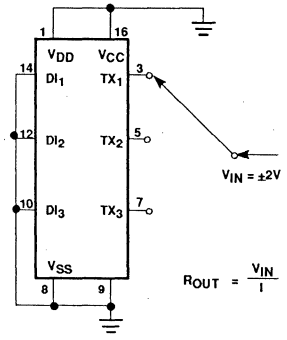


Figure 1. Power-Off Source Resistance (Drivers)

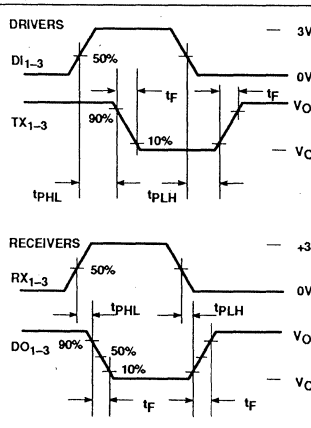


Figure 2. Switching Characteristics

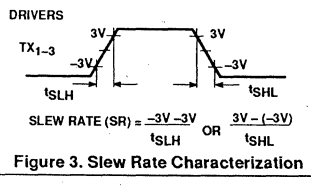


Figure 3. Slew Rate Characterization

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA-232-D/CCITT V.28 and as such, defines the elctrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads, which allow the transfer of timing, data, control, and test signals. The MC145406 provides the necessary level shifting between the TTL/CMOS logic levels and the high voltage levels of EIA-232-D (ranging from ±3 to ±25V).

DRIVERS

As defined by the specification, an EIA-232-D driver presents a voltage of between ±5 to ±15V into a load of between 3 to 7kΩ. A logic one at the driver input results in a voltage of between –5 to –15V. A logic zero results in a voltage between ±5 to ±15V. When operating at ±7 to ±12V, the MC145406 meets this requirement. When operating at ±5V, the MC145406 drivers produce less than ±5V at the output (when terminated), which does not meet the EIA-232-D specification. However, the output voltages when using a ±5V power supply are high enough (around ±4V) to permit proper reception by an EIA-232-D receiver, and can be used in applications where strict compliance to EIA-232-D is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA-232-D cable. The worst-case condition that is permitted by EIA-232-D is a ±15V source that is current limited to 500mA. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300Ω output impedance needed to satisfy the EIA-232-D driver requirements. This will reduce the short circuit current to under 40mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30V/µs.

RECEIVERS

The job of an EIA-232-D receiver is to level-shift voltages in the range of –25 to +25V down to TTL/CMOS logic levels (0 to +5V). A voltage of between –3 and –25V on RX_1 is defined as a mark and produces a logic one at DO_1. A voltage between +3 and +25V is a space and produces a logic zero. While receiving these signals, the RX inputs must present a resistance between 3 and 7kΩ. Nominally, the input resistance of the RX_{1-3} inputs is 5.0kΩ.

The input threshold of the RX_{1-3} inputs is typically biased at 1.8V above ground (GND) with typically 800mV of hysteresis included to improve noise immunity. The 1.8V bias forces the appropriate DO pin to a logic one when its RX input is open or grounded as called for in EIA-232-D specification. Notice that TTL logic levels can be applied to the RX inputs in lieu of normal EIA-232-D signal levels. This might be helpful in situations where access to the modem or computer through the EIA-232-D connector is necessary with TTL devices. However, it is important not to connect the EIA-232-D outputs (TX_1) to TTL inputs since TTL operates off +5V only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from the digital power supply. The TX and RX sections are independently powered by V_{DD} and V_{SS} so that one may run logic at +5V and the EIA-232-D signals at ±12V.

POWER SUPPLY CONSIDERATIONS

The Signetics MC145406 is not sensitive to power supply sequencing and does not require the special protection circuitry of other designs.

Philips Components–Signetics

Document No.	853–0933
ECN No.	86552
Date of Issue	November 14, 1986
Status	Product Specification
Data Communication Products	

MC1488
Quad line driver

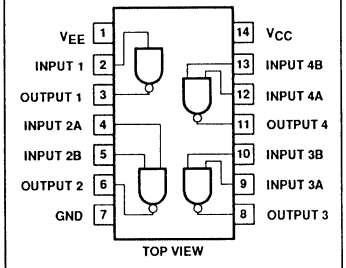
DESCRIPTION
The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

FEATURES
- Current limited output: ±10mA Typ
- Power-off source impedance: 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

APPLICATIONS
- Computer port driver
- Digital transmission over long lines
- Slew rate control
- TTL/DTL-to-MOS translation

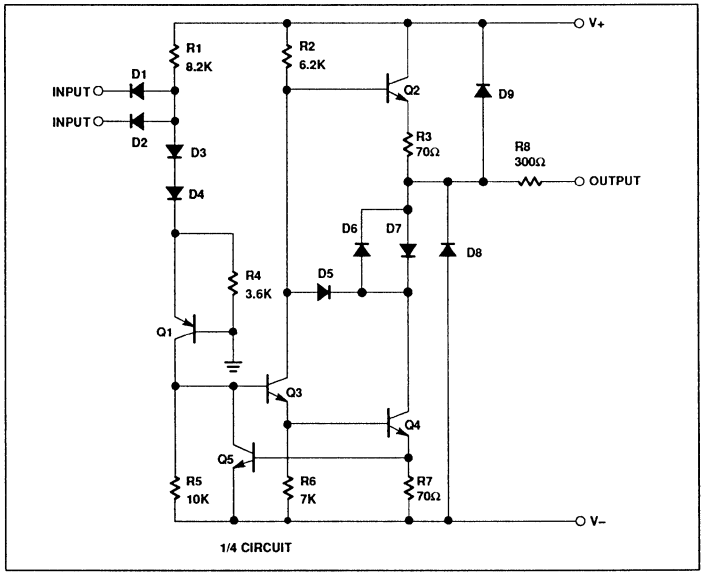
PIN CONFIGURATION

D, F, N Packages



TOP VIEW

CIRCUIT SCHEMATIC



1/4 CIRCUIT

Quad line driver | MC1488

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0°C to +75°C	MC1488D
14-Pin Plastic DIP	0°C to +75°C	MC1488N
14-Pin Ceramic DIP	0°C to +75°C	MC1488F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage V+	+15	V
	V–	–15	V
V_{IN}	Input voltage	$-15 \leq V_{IN} \leq 7.0$	V
V_{OUT}	Output voltage	±15	V
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating ambient temperature range	0 to +75	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTE:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.
   D package at 8.3mW/°C.

DC AND AC ELECTRICAL CHARACTERISTICS

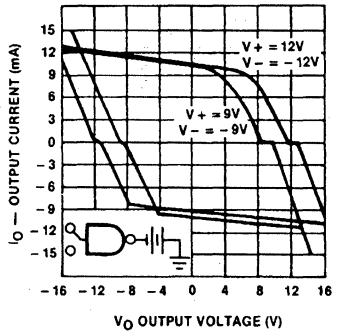
$V+ = +9.0V \pm 1\%$, $V- = -9.0V \pm 1\%$, $T_A = 0°C$ to $+75°C$, unless otherwise specifed. All typicals are for $V+ = 9.0V$, $V- = -9.0V$, and $T_A = 25°C$[1]

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{IH} V_{IL}	Logic "0" input current Logic "1" input current	$V_{IN} = 0V$ $V_{IN} = +5.0V$			−1.0 0.005	−1.6 10.0	mA μA
V_{OH}	High level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 0.8V$	$V+ = 9.0V$ $V- = -9.0V$	6.0	7.0		V
			$V+ = 13.2V$ $V- = -13.2V$	9.0	10.5		V
V_{OL}	Low level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 1.9V$	$V+ = 9.0V$ $V- = -9.0V$	−6.0	−6.8		V
			$V+ = 13.2V$ $V- = -13.2V$	−9.0	−10.5		V
I_{SC+}	High level output short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
I_{SC-}	Low level output short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 1.9V$		5.0	10.0	12.0	mA
R_{OUT}	Output resistance	$V+ = V- = 0V$ $V_{OUT} = \pm 2V$		300			Ω
I+	Positive supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V, V- = -9.0V$ $V+ = 12V, V- = -12V$ $V+ = 15V, V- = -15V$		15.0 19.0 25.0	20.0 25.0 34.0	mA mA mA
		$V_{IN} = 0.8V$	$V+ = 9.0V, V- = -9.0V$ $V+ = 12V, V- = -12V$ $V+ = 15V, V- = -15V$		4.5 5.5 8.0	6.0 7.0 12.0	mA mA mA
I−	Negative supply current (output open)	$V_{IN} = 1.9V$	$V+ = 9.0V, V- = -9.0V$ $V+ = 12V, V- = -12V$ $V+ = 15V, V- = -15V$		−13.0 −18.0 −25.0	−17.0 −23.0 −34.0	mA mA mA
		$V_{IN} = 0.8V$	$V+ = 9.0V, V- = -9.0V$ $V+ = 12V, V- = -12V$ $V+ = 15V, V- = -15V$		−1 −1 −0.01	−15 −15 −2.5	μA μA mA
P_D	Maximum power dissipation, $T_A = 25°C$ (still–air)[2] F package N package D package					 1190 1420 1040	 mW mW mW
t_{PD1}	Propagation delay to "1"	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			275	560	ns
t_{PDD}	Propagation delay to "0"	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			70	175	ns
t_R	Rise time	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			75	100	ns
t_F	Fall time	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			40	75	ns

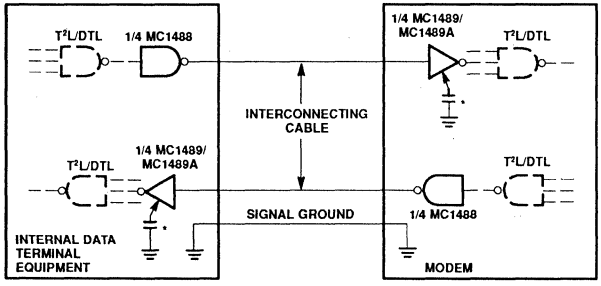
NOTES:
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C.
   N package at 11.4mW/°C.
   D package at 8.3mW/°C.

Quad line driver | MC1488

TYPICAL PERFORMANCE CHARACTERISTICS



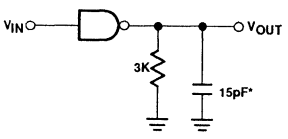
Output Voltage and Current-Limiting Characteristics



NOTE:
*Optional for noise filtering

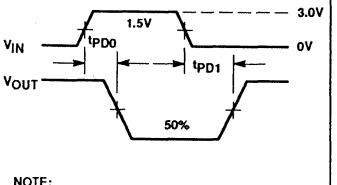
RS-232C Data Transmission

AC LOAD CIRCUIT



NOTE:
*C_L includes probe and jig capacitance.

SWITCHING WAVEFORMS



NOTE:
t_R and t_F are measured between 10% and 90% of the output waveform.

APPLICATIONS

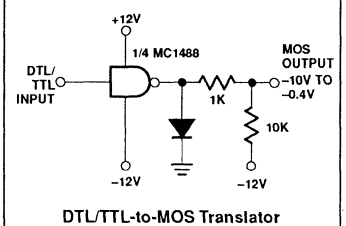
By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current–limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC}(\Delta T/\Delta V)$$

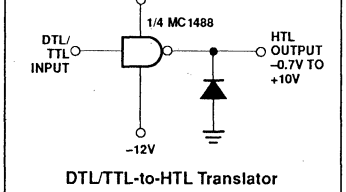
where C is the required capacitor, I_{SC} is the short–circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS–232C specifies that the output slew rate must not exceed 30V/μs. Using the worst–case output short–circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

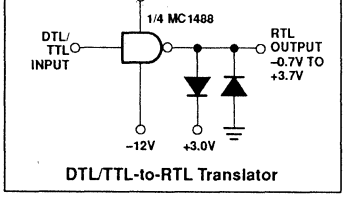
TYPICAL APPLICATIONS



DTL/TTL-to-MOS Translator



DTL/TTL-to-HTL Translator



DTL/TTL-to-RTL Translator

Philips Components–Signetics

Document No.	853–0934
ECN No.	91023
Date of Issue	October 20, 1987
Status	Product Specification
Data Communication Products	

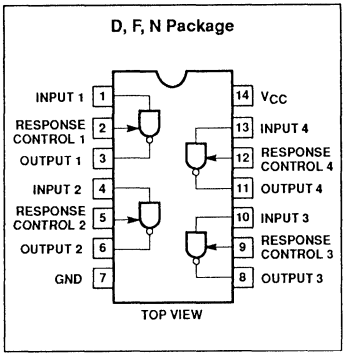
MC1489/MC1489A
Quad line receivers

DESCRIPTION
The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS-232C.

FEATURES
- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

APPLICATIONS
- Computer port inputs
- Modems
- Eliminating noise in digital circuitry
- MOS-to-TTL/DTL translation

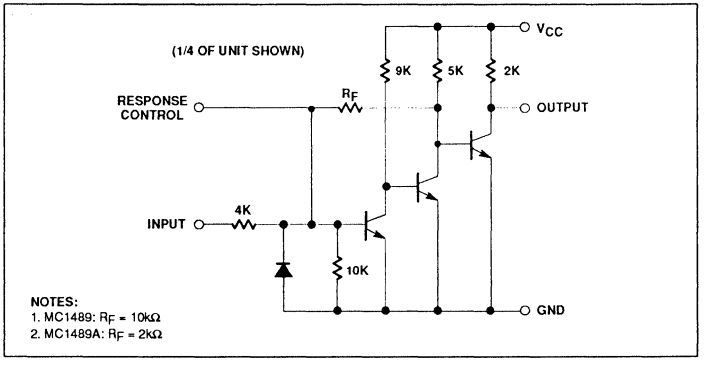
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0°C to +70°C	MC1489N
14-Pin Plastic DIP	0°C to +70°C	MC1489AN
14-Pin Cerdip	0°C to +70°C	MC1489F
14-Pin Cerdip	0°C to +70°C	MC1489AF
14-Pin Plastic SO	0°C to +70°C	MC1489D
14-Pin Plastic SO	0°C to +70°C	MC1489AD

EQUIVALENT SCHEMATIC

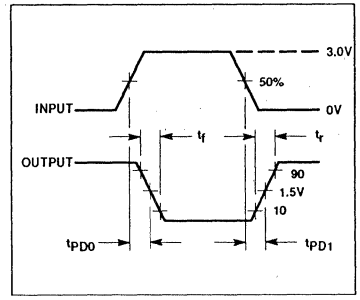


ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	10	V
V_{IN}	Input voltage range	±30	V
I_{OUT}	Output load current	20	mA
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

VOLTAGE WAVEFORMS



DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±1%, 0°C ≤ T_A ≤ +75°C, unless otherwise specified.[1,2]

SYMBOL	PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input high threshold voltage	T_A = 25°C, V_{OUT} ≤ 0.45V, I_{OUT} = 10mA	1.0		1.5	1.75		2.25	V
V_{IL}	Input low threshold voltage	T_A = 25°C, V_{OUT} ≥ 2.5V, I_{OUT} = –0.5mA	0.75		1.25	0.75		1.25	V
I_{IN}	Input current	V_{IN} = +25V	+3.6	+5.6	+8.3	+3.6	+5.6	+8.3	mA
		V_{IN} = –25V	–3.6	–5.6	–8.3	–3.6	–5.6	–8.3	
		V_{IN} = +3V	+0.43	+0.53		+0.43	+0.53		
		V_{IN} = –3V	–0.43	–0.53		–0.43	–0.53		
V_{OH}	Output high voltage	V_{IN} = 0.75V, I_{OUT} = –0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
		Input = Open, I_{OUT} = –0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
V_{OL}	Output low voltage	V_{IN} = 3.0V, I_{OUT} = 10mA		0.33	0.45		0.33	0.45	V
I_{SC}	Output short-circuit current	V_{IN} = 0.75V		3.0			3.0		mA
I_{CC}	Supply current	V_{IN} = 5.0V		20	26		20	26	mA
P_D	Power dissipation	V_{IN} = 5.0V		100	130		100	130	mW

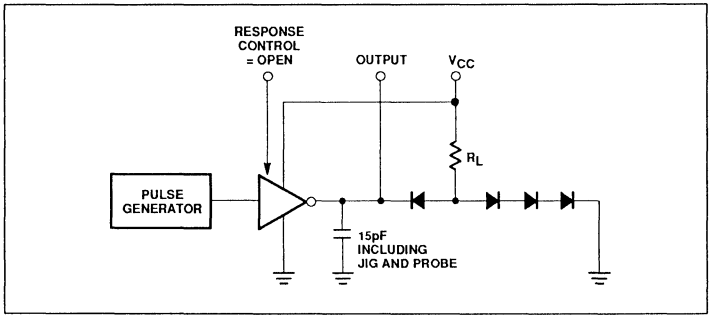
NOTES:
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±1%, T_A = 25°C, unless otherwise specified.[1,2]

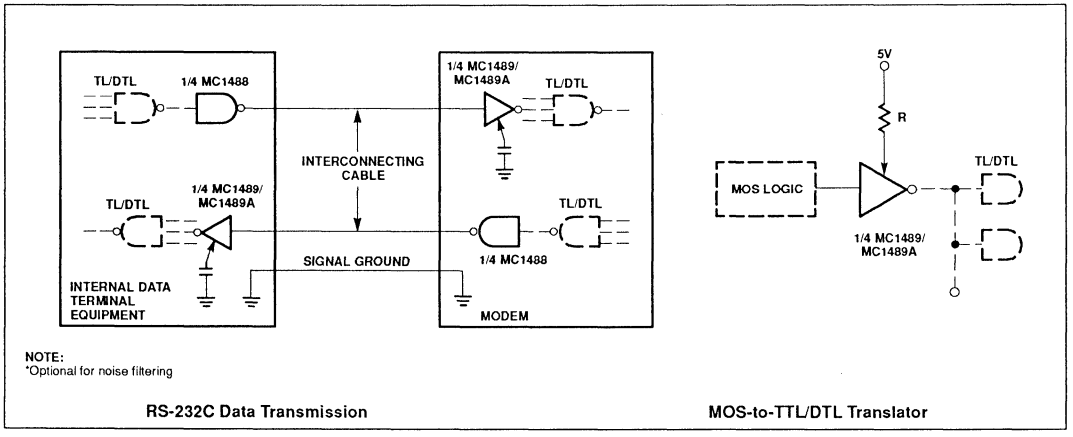
SYMBOL	PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{PD1}	Input to output "high" Propagation delay	R_L = 3.9kΩ (AC test circuit)		25	85		25	85	ns
t_{PD0}	Input to output "low" Propagation delay	R_L = 390Ω (AC test circuit)		20	50		20	50	ns
t_R	Output rise time	R_L = 3.9kΩ (AC test circuit)		110	175		110	175	ns
t_F	Output fall time	R_L = 390Ω (AC test circuit)		9	20		9	20	ns

NOTES:
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC TEST CIRCUIT



TYPICAL APPLICATIONS



NOTE:
*Optional for noise filtering

RS-232C Data Transmission

MOS-to-TTL/DTL Translator

Philips Components–Signetics

Document No.	
ECN No.	
Date of Issue	December 1988
Status	Preliminary Specification
Data Communication Products	

NE5080

High-speed FSK modem transmitter

DESCRIPTION

The NE5080 is the transmitter chip, of a two-chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single-Channel" Phase-Continuous-FSK Token Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies is normally at 1.67 to 1.00 at any center frequency; however, it can be varied externally. (See AN1950.)

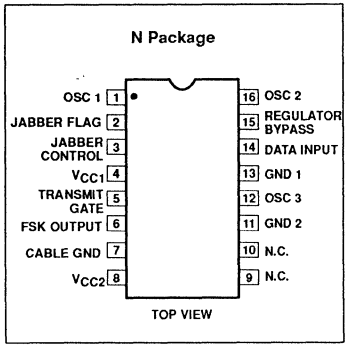
FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Jabber function on-chip

APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

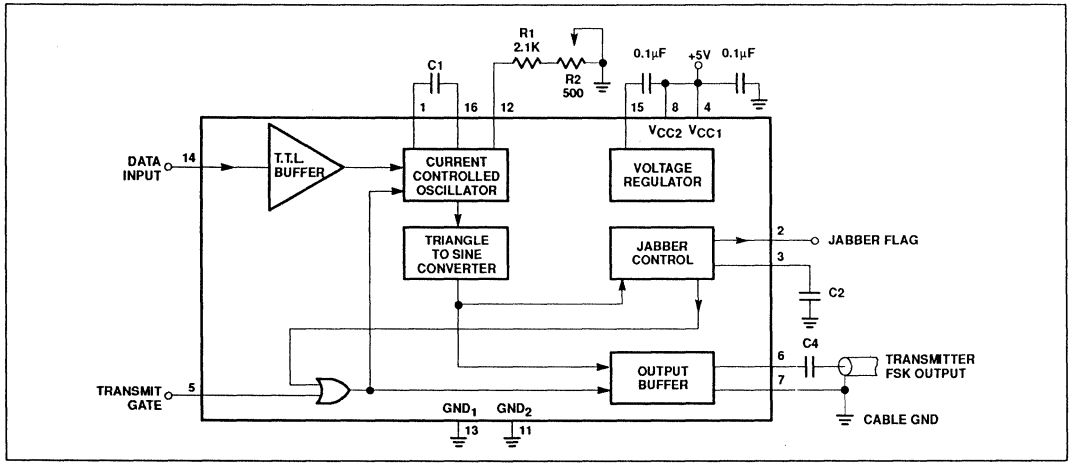
PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	NE5080N

BLOCK DIAGRAM



High-speed FSK modem transmitter NE5080

GENERAL DESCRIPTION

The NE5080 is designed to transmit high frequency asynchronous data on coaxial cable, at rates from DC to 2M baud (see Note 1). The chip accepts serial data and transmits it as a periodic signal whose frequency depends on whether the data is high or low.

The device is meant to operate at a frequency of 6.25MHz for a logic high and 3.75MHz for a logic low (see Note 2). The frequency is set up by external trimming components; however, the ratio of the high and low frequencies is set internally and cannot be altered.

The FSK output can be turned off by use of the transmit gate pin. When turned off, the transmitter has a high output impedance and the oscillator is disabled.

The length of time a transmitter can transmit can be controlled by the use of the Jabber control pin (see description of Jabber Control Pin).

Jabber Control Pin

During the time the transmitter is transmitting, this pin sources a current. This current can be used to set the maximum time that the transmitter can be on. There are three options that can be used:

1. Use the current to charge a capacitor. When the voltage across the cap gets to approximately 1.4V, the transmitter will turn off. A logic low applied to Pin 3 will reset the Jabber function; an open collector output should be used for this purpose. A logic high applied to the pin will disable the transmitter.

2. Use to externally sense the current and have external circuitry to control the length of time the transmitter is on.

3. The pin can be tied to ground and is then not active. Transmission is then controlled solely by the signal at the transmit gate pin.

Jabber Flag Pin

This pin will go to a logic high when the Jabber Control pin is used to shut off the transmitter. It will latch and can be reset by applying a logic low to the Jabber Control pin.

NOTES:
1. The NE5080 is capable of transmitting up to 1M baud of differential Manchester code at a center frequency of 5MHz.
2. Although the chip is designed to meet the requirements of IEEE standard 802.4 (Token-Passing Single-Channel Phase-Continuous-FSK Bus), it can be used at other frequencies.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply Voltage	+6	V
V_{IN}	Input voltage range (Data, Gate)	–0.3 to V_{CC}	V
P_D	Power dissipation	800	mW
T_A	Operating temperature range	0 to +70	°C
T_J	Maximum junction temperature	+150	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C

NE5080 PIN FUNCTION

PIN	FUNCTION
1	**OSC 1:** One end of the external capacitor used to set the carrier frequency.
2	**Jabber Flag:** This pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function.
3	**Jabber Control:** Used to control transmit time. See note on Jabber function.
4	**V_{CC1}:** Voltage supply.
5	**Transmit Gate:** A logic flow on this pin will enable the transmitter; a logic high will disable it.
6	**Transmitter FSK Output**
7	**Cable Ground:** The shield of the coax cable should be connected to this pin and to Pin 11.
8	**V_{CC2}:** Connect to Pin 4 close to device.
9	**No Connection**
10	**No Connection**
11	**Ground 2:** Connect to Analog ground close to device.
12	**OSC 3:** A variable resistor between this point and ground is used to set the carrier frequencies.
13	**Ground 1:** Connect to Analog close to device.
14	**Data Input**
15	**Regulator Bypass:** A bypass capacitor between this pin and V_{CC1} is required for the internal voltage regulator function.
16	**OSC 2:** One end of a capacitor that is between Pin 1 and Pin 16 and is used to set the carrier frequency.

High-speed FSK modem transmitter | NE5080

DC ELECTRICAL CHARACTERISTICS $V_{CC1,2}$ = 4.75–5.25V, T_A = 0°C to +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
f_1	Output frequency (Logic high)	Data input ≥2.0V (See Note 1)	6.17	6.25	6.33	MHz
f_0	Output frequency (Logic low)	Data input ≤0.8V (See Note 1)	3.67	3.75	3.83	MHz
V_O	Output amplitude	Data input ≥2.0V or ≤0.8V Output Load = 37.5Ω	0.5		1.0	V_{RMS}
R_{OFF}	Output impedance (gated off)	Transmit gate ≥2.0V	100			kΩ
R_{ON}	Output impedance (gated on)	Transmit gate ≤0.8V			37.5	Ω
C_O	Output capacitance	Transmit gate ≥2.0V or ≤0.8V			10	pF
V_F	Feedthrough	Transmit gate ≥2.0V 2.0MHz sq. wave (TTL levels) input			1	mV_{RMS}
I_J	Jabber current	Transmit gate ≤0.8V Input ≥2.0V or ≤0.8V		1.25		µA
I_{CC}	Supply current	V_{CC1} connected to V_{CC2}		75	100	mA
Logic levels						
	Data Input					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	V_{IN} = 2.4V			40	µA
I_{IL}	Input current	V_{IN} = 0.4V			−1.6	mA
	Transmit gate					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	VG = 2.4V			40	µA
I_{IL}	Input current	VG = 0.4V			−1.6	mA
	Jabber flag					
V_{OH}	Logic high	I_{OH} = −400µA	2.4			V
V_{OL}	Logic low	I_{OL} = 4.0mA			0.4	V
	Jabber control					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V

NOTE:
1. Tuned per instructions in AN195.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_S	Setup time	Data in	Gate on	Figure 1	2	0.1		µs
t_A	Delay time	Output freq. change	Data transition	Figure 2			150	ns
t_B	Delay time	Output disabled	Gate off	Figure 3		0.4	2	µs
t_C	Delay time	Output disabled	Jabber control	Figure 4			100	ns
t_D	Delay time	Jabber flag	Jabber control	Figure 5			100	ns
	Jabber control reset Pulse width (Logic low)				100			ns

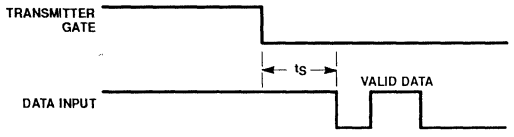


Figure 1. Setup Time, t_S

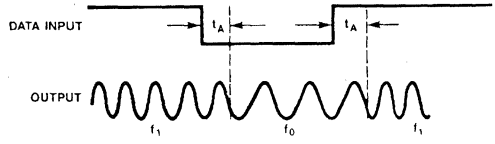


Figure 2. Delay Time, t_A

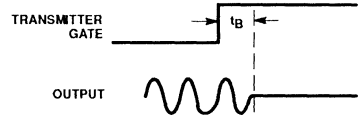


Figure 3. Delay Time, t_B

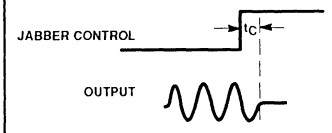


Figure 4. Delay Time, t_C

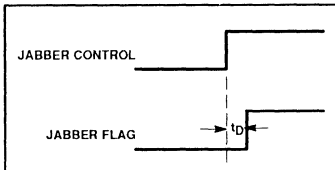


Figure 5. Delay Time, t_D

Philips Components–Signetics

Document No.	
ECN No.	
Date of Issue	December 1988
Status	Preliminary Specification
Data Communication Products	

NE5081

High-speed FSK modem receiver

DESCRIPTION

The NE5081 is the receiver chip of a two-chip set designed to operate as an FSK modem (the NE5080 is the transmitter chip). The chips are compatible with the IEEE 802.4 standard for a "Single-Channel Phase-Continuous- FSK Token Bus." The specifications given in this data sheet are those guaranteed when the receiver is tuned to the frequencies given in the 802 standard. However, the receiver will work at other frequencies.

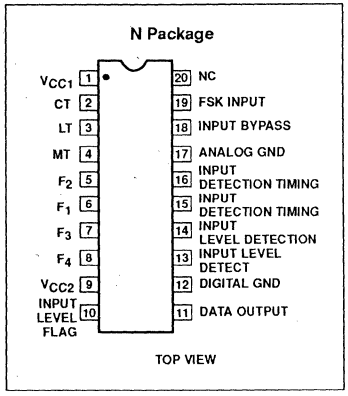
FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Low bit rate error (10^{-12} typical)

APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

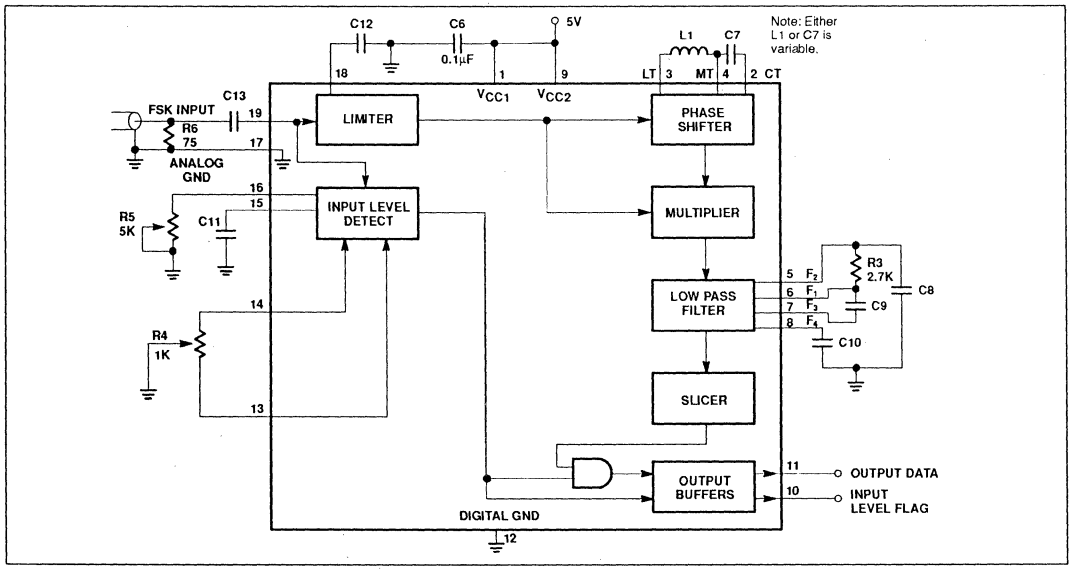
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0°C to +70°C	NE5081N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range	–0.3 to $+V_{CC}$	V
I_{DO}	Output (Data, Level detect) Max sink current	20	mA
P_D	Maximum power dissipation, $T_A = 25°C$, (still-air)[1] N package	1690	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C
	Max differential voltage between analog and digital grounds	100	mV

NOTE:
1. Derate above 25°C as follows:
   N package at 13.5mW/°C.

DC ELECTRICAL CHARACTERISTICS $V_{CC1,2} = 4.75–5.25V$. External LC circuit tuned to 5MHz. Input level detect set at $16mV_{RMS}$, $T_A = 0°C$ +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
f_0	Logic Low Frequency	External LC tuned to 5MHz	3.67	3.75	3.83	MHz
f_1	Logic High Frequency	External LC tuned to 5MHz	6.17	6.25	6.33	MHz
IN_{DL}	Minimum Input Detect Level	Minimum input level that is detected as carrier (See Note 2 in General Description)	5		50	mV_{RMS}
	Logic Levels:					
V_{OL}	Data Output	$I_{OL} = 4.0mA$ $V_{IN} > 16mV_{RMS}$ Freq = f_0			0.4	V
V_{OH}	Data Output	$I_{OH} = -400\mu A$ $V_{IN} > 16mV_{RMS}$ Freq = f_1	2.4			V
V_{OH}	Data Output	$I_{OH} = -400\mu A$ $V_{IN} < 5mV_{RMS}$ Freq = f_0	2.4			V
V_{OL}	Input Detect Flag	$I_{OL} = 4.0mA$ $V_{IN} = 0V_{RMS}$			0.4	V
V_{OH}		$I_{OH} = -400\mu A$ $V_{IN} > 16mV$	2.4			V
I_{CC}	Supply Current	$V_{CC} = 5.25V$ (V_{CC1} connected to V_{CC2}) $V_{IN} = 1.0V_{RMS}$ Freq = f_1 or f_0			50	mA
BER	Bit Error Rate	Input Signal > $16mV_{RMS}$ maximum in-band noise = $1.6mV_{RMS}$		10^{-12}	10^{-9}	

High-speed FSK modem receiver | NE5081

AC ELECTRICAL CHARACTERISTICS (AN195, Figure 5 with a 100KHz $1V_{P-P}$)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_B	Delay Time	Input Level Detect Flag	Input On	Figure 1		0.05	1	µs
t_C	Delay Time	Input Level Detect Flag	Input Off	Figure 1	0.5	1.5	2.5	µs
t_D	Delay Time	Output Enabled	Input On	Figure 2			2	µs
t_E	Delay Time	Output Disabled	Input Off	Figure 2	0.5	1.5	2.5	µs
	Required Delay	Carrier Turn Off	Valid Data End		2			µs

GENERAL DESCRIPTION

The NE5081 will accept an FSK-encoded signal and provide the demodulated digital data at the output. It is optimized to work at frequencies specified in IEEE 802.4—Token-Passing Single-Channel Phase-Continuous-FSK Bus—(i.e., 3.75MHz and 6.25MHz). However, it will work at other frequencies.[1]

Its normal acceptable input signal level range is from $16mV_{RMS}$ to $1V_{RMS}$. This can be adjusted.[3]

The receiver will yield an undetected "Bit Error Rate" of 10^{-9} or lower when receiving signals with a 20dB signal-to-noise ratio. It has a maximum output Jitter of ± 40ns.[3]

NOTES:

1. The receiver can be tuned to accept different frequencies by adjustment of the LC circuit shown in Figure 7. However, the external components have been optimized for 3.75MHz and 6.25MHz. See "Determining Component Values" for use at other frequencies.
2. Input Level Detect
   This is a method of turning off the output of the receiver when the input signal falls below an acceptable level. This level is adjustable within the range given in the electrical specification section. The purpose of this function is to minimize the effect of noise on receiver performance and to indicate when there is an acceptable signal present at the input. All specifications given in this data sheet are with the input level detection set at $16mV_{RMS}$.
3. Jitter (Definition)
   This is a measure of the ability of the receiver to accurately reproduce the timing of its FSK-coded digital input. The spec indicates the error band in the timing of a logic level change.

NE5081 PIN FUNCTION

PIN	FUNCTION
1	**V_{CC1}:** Should be connected to the 5V supply and Pin 9.
2	**CT:** One end of an external capacitor tthat is used to tune the receiver.
3	**LT:** One end of an indicator that is used to tune the receiver.
4	**MT:** The junction of the capacitor and inductor used for tuning the receiver.
5	**F2**
6	**F1** } Pins 5, 6, 7, 8 are used for a low-pass filter to remove carrier
7	**F3** } harmonics from the data output.
8	**F4**
9	**V_{CC2}:** Connect to Pin 1 (see Pin 1 function) close to the device.
10	**Input Level Flag:** This pin is used to indicate when there is a signal at the input that is greater than the level set by the input level detection circuitry. A logic high indicates an input greater than the set level.
11	**Data Output:** Supplies T^2L level data that corresponds to the FSK input received.
12	**Digital Ground:** Should be connected to digital ground.
13 and 14	**Input Level Detect:** These pins are used to set the level of input signal that the device will accept as valid.
15	**Input Detection Timing:** An external capacitor between this pin and ground is used to determine the time from carrier turn-off to output disable.
16	**Input Detection Timing:** Same as Pin 15, except that a resistor goes between this pin and ground. The values of the C and R depend on the carrier frequency. The values given in this data sheet are for a 5MHz carrier center frequency.
17	**Analog Ground:** Connect to analog ground close to the device.
18	**Input Bypass:** A capacitor between this pin and ground is used to bypass the input bias circuitry.
19	**Input:** The FSK signal from the cable goes to this pin.
20	**No Connection.**

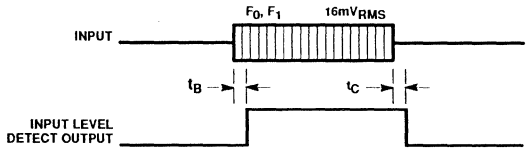


Figure 1. Delay Time, t_B, t_C

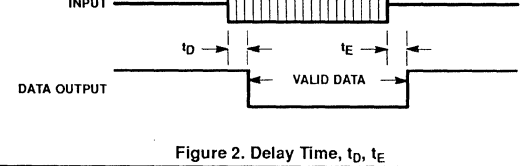


Figure 2. Delay Time, t_D, t_E

Philips Components–Signetics

Document No.	
ECN No.	
Date of Issue	February 1987
Status	Preliminary Specification
Data Communication Products	

NE5170
Octal line driver

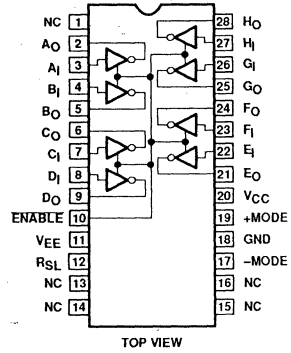
DESCRIPTION
The NE5170 is an octal line driver which is designed for digital communications with data rates up to 100kb/s. This device meets all the requirements of EIA standards RS-232C/RS-423A and CCITT recommendations V.10/X.26. Three programmable features: (1) output slew rate, (2) output voltage level, and (3) three-state control (high-impedance) are provided so that output characteristics may be modified to meet the requirements of specific applications.

FEATURES
- Meets EIA RS-232C/423A and CCITT V.10/X.26
- Simple slew rate programming with a single external resistor
- 0.1 to 10V/μs slew rate range
- High/low programmable voltage output modes
- TTL compatible inputs

APPLICATIONS
- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

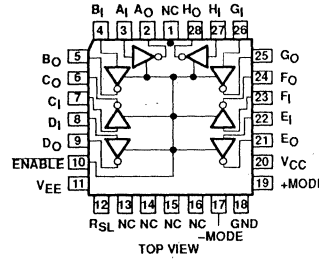
PIN DESCRIPTION

N Package



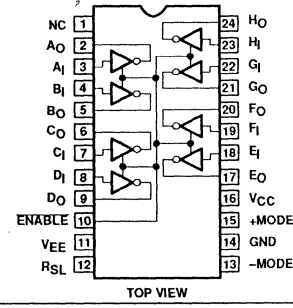
TOP VIEW

A Package



TOP VIEW

D Package



TOP VIEW

FUNCTION TABLE

ENABLE	LOGIC INPUT	OUTPUT VOLTAGE (V)		
		RS-423A[1]	RS-232C	
			Low Output Mode[1]	High Output Mode[2]
L	L	5 to 6V	5 to 6V	≥ 9V
L	H	–5 to –6V	–5 to –6V	≤ –9V
H	X	High-Z	High-Z	High-Z

NOTES:
1. V_{CC} = +10V and V_{EE} = –10V; R_L = 3kΩ
2. V_{CC} = +12V and V_{EE} = –12V; R_L = 3kΩ

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0°C to +70°C	NE5170N
28-Pin PLCC	0°C to +70°C	NE5170A
28-Pin SO package	0°C to +70°C	NE5170D

Octal line driver | NE5170

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage and + MODE	15	V
V_{EE}	Supply voltage and – MODE	–15	V
I_{OUT}	Output current[1]	±150	mA
V_{IN}	Input voltage ($\overline{Enable}$, Data)	–1.5 to +7	V
V_{OUT}	Output voltage[2]	±15	V
	Minimum slew resistor[3]	1	kΩ
P_D	Power dissipation	1200	mW

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. High impedance mode.
3. Minimum value of the resistor used to set the slew rate.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ±10%; V_{EE} = –10V ±10%; ±MODES = 0V; R_{SL} = 2kΩ, 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{OH}	Output high voltage	V_{IN} = 0.8V R_L = 3kΩ[2]	5	6	V
		R_L = 450Ω[2]	4.5	6	
		R_L = 3kΩ[3], C_L = 2500pF	V_{CC}–3		
V_{OL}	Output low voltage	V_{IN} = 2.0V R_L = 3kΩ[2]	–6	–5	V
		R_L = 450Ω[2]	–6	–4.5	
		R_L = 3kΩ[3], C_L = 2500pF		V_{EE}+3	
V_{OU}	Output unbalance voltage	V_{CC} = |V_{EE}|, R_L = 450Ω[2]		0.4	V
I_{CEX}	Output leakage current	|V_O| = 6V, ENABLE = 2V or V_{CC} = V_{EE} = 0V	–100	100	µA
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IL}	Logic "0" input current	V_{IN} = 0.4V	–400	0	µA
I_{IH}	Logic "1" input current	V_{IN} = 2.4V	0	40	µA
I_{OS}	Output short circuit current[1]	V_O = 0V	–150	150	mA
V_{CL}	Input clamp voltage	I_{IN} = –15mA	–1.5		V
I_{CC}	Supply current	NO LOAD		35	mA
I_{EE}		NO LOAD	–45		mA

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. V_{OH}, V_{OL} at R_L = 450Ω will be ≥ 90% of V_{OH}, V_{OL} at R_L = ∞.
3. High Output Mode; +MODE pin = V_{CC}; –MODE pin = V_{EE}; 9V ≤ V_{CC} ≤ 13V; –9V ≥ V_{EE} ≥ –13V.

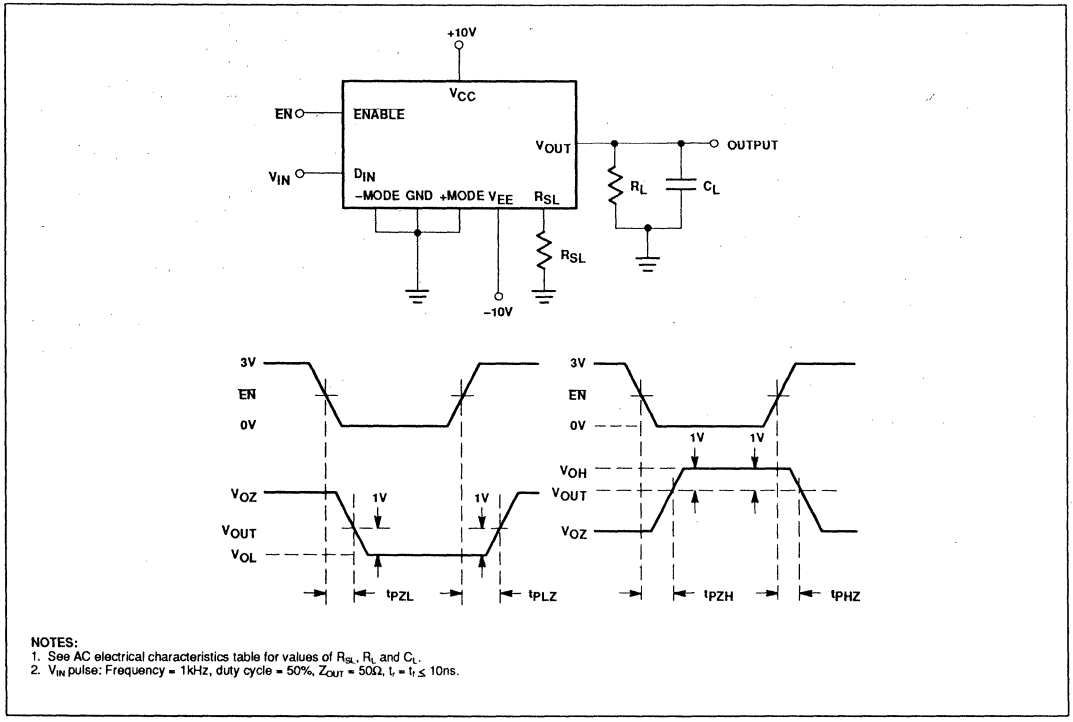
Octal line driver | NE5170

AC ELECTRICAL CHARACTERISTICS V_{CC} = +10V; V_{EE} = –10V; Mode = GND, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PHZ}	Propagation delay output high to high impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	µs
t_{PLZ}	Propagation delay output low to high impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	µs
t_{PZH}	Propagation delay high impedance to high output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	µs
t_{PZL}	Propagation delay high impedance to low output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	µs
SR	Output slew rate[1]	R_{SL} = 2k	8	12	V/µs
		R_{SL} = 20k	0.8	1.2	
		R_{SL} = 200k	0.06	0.14	

NOTE:
SR: Load condition. (A) For R_{SL} < 4kΩ use R_L = 450Ω; C_L = 50pF; (B) for R_{SL} > 4kΩ use either R_L = 450Ω, C_L = 50pF or R_L = 3kΩ, C_L = 2500pF.

AC PARAMETER TEST CIRCUIT AND WAVEFORMS



NOTES:
1. See AC electrical characteristics table for values of R_{SL}, R_L and C_L.
2. V_{IN} pulse: Frequency = 1kHz, duty cycle = 50%, Z_{OUT} = 50Ω, $t_r = t_f \leq$ 10ns.

Octal line driver | NE5170

SLEW RATE PROGRAMMING

Slew rate for the NE5170 is set using a single external resistor connected between the R_{SL} pin and ground. Adjustment is made according to the formula:

$$R_{SL}\ (\text{in k}\Omega) = \frac{20}{\text{Slew Rate}}$$

where the slew rate is in V/μs. The slew resistor can vary between 2 and 200kΩ which gives a slew rate range of 10 to 0.1V/μs. This adjustment of the slew rate allows tailoring output characteristics to recommendations for cable length and data rate found in EIA standard RS–423A. Approximations for cable length and data rate are given by:

Max. data rate (in kb/s) = 300/t

Cable length (in feet) = 100×t

where t is the rise time in microseconds. The absolute maximum data rate is 100kb/s and the absolute maximum cable length is 4000 feet.

OUTPUT MODE PROGRAMMING

The NE5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS–423A and RS–232C. The high output mode meets the specifications of RS–232C only, since higher output voltages result from programming this mode. The high output mode provides the greater output voltages where higher attenuation levels must be tolerated. Programming the high output mode is accomplished by connecting the +MODE pin to V_{CC} and the –MODE pin to V_{EE}. The low output mode results when both of these pins are connected to ground.

APPLICATION

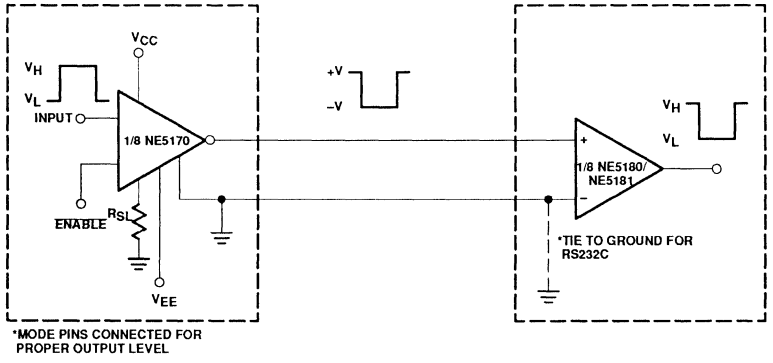


Figure 1. RS-232C/RS-423A Data Transmission

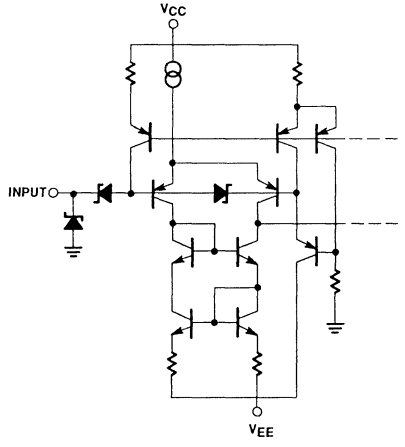


Figure 2. Input Stage Schematic

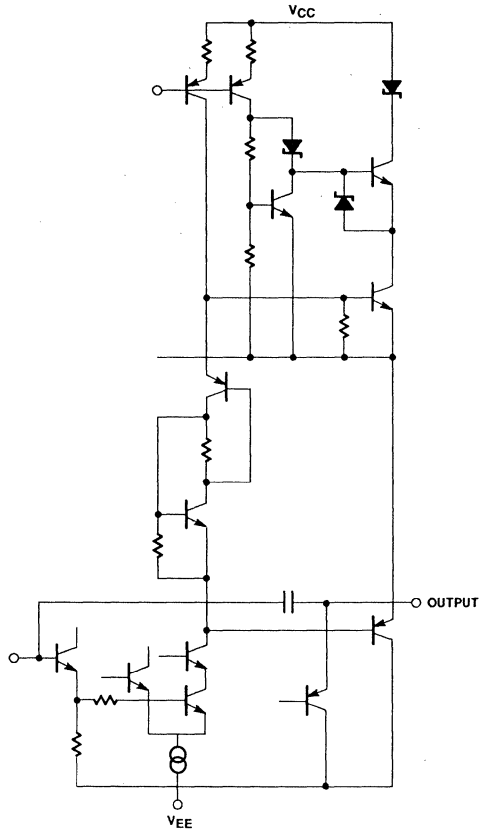


Figure 3. Output Stage Schematic

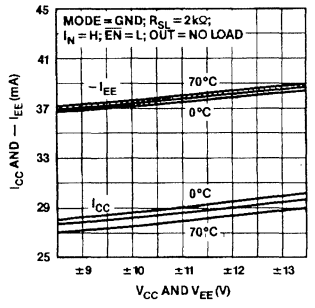


Figure 4. Typical I_{CC} and I_{EE} vs Supply Voltages

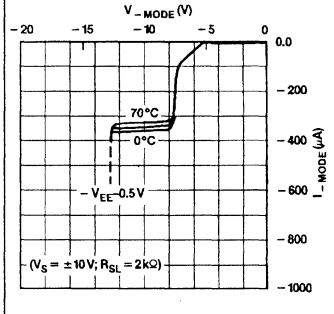


Figure 7. Typical –MODE Current vs –MODE Voltage

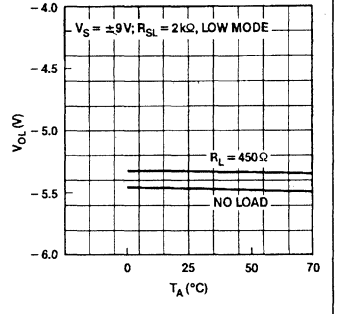


Figure 10. Typical Output Low Voltage vs Temperature

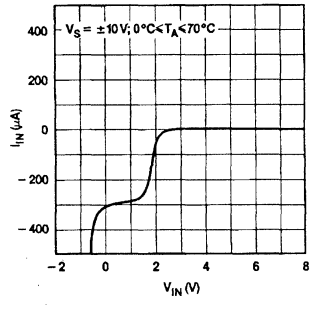


Figure 5. Typical Input Current vs Input Voltage

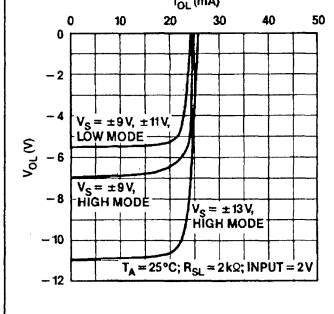


Figure 8. Typical Output Low Voltage vs Load Current

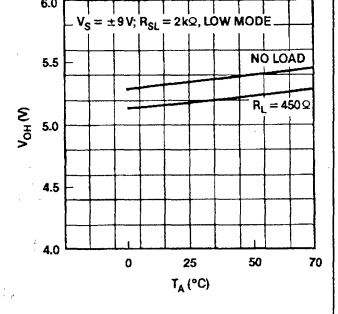


Figure 11. Typical Output High Voltage vs Temperature

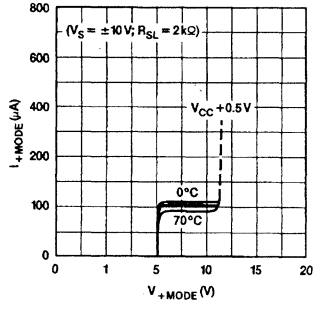


Figure 6. Typical +MODE Current vs +MODE Voltage

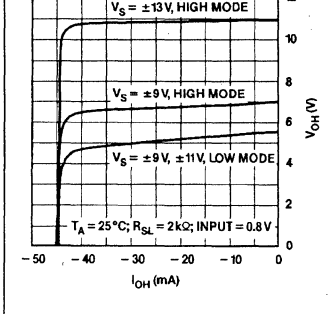


figure 9. Typical Output High Voltage vs Load Current

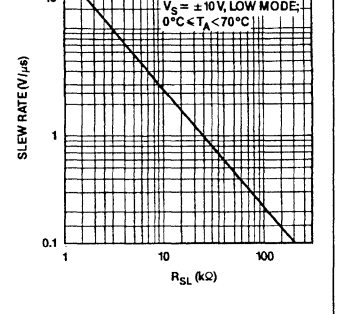


Figure 12. Typical Slew Rate vs R_{SL}

Philips Components–Signetics

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Data Communication Products	

NE5180/NE5181

Octal differential line receivers

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS-232C, RS-423A, RS-422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

FEATURES

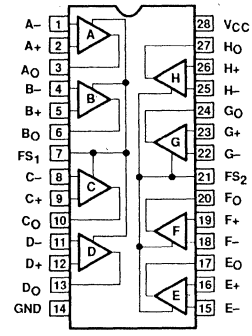
- Meets EIA RS-232C/423A/422A and CCITT V.10, V.11, V.28
- Single +5V supply—TTL compatible outputs
- Differential inputs withstand ±25V
- Failsafe feature
- Input noise filter (NE5180 only)
- Internal hysteresis
- Available in SMD PLCC

APPLICATIONS

- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

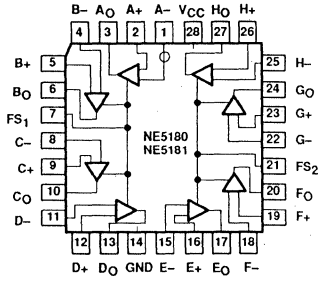
PIN DESCRIPTION

N Package



TOP VIEW

A Package



TOP VIEW

FUNCTION TABLE

INPUT	FAILSAFE INPUT	LOGIC OUTPUT
$V_{ID} > 200mV^1$	X	H
$V_{ID} < -200mV^1$	X	L
Both inputs open or grounded	0V	L
	V_{CC}	H

NOTE:
1. V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0°C to +70°C	NE5180N
28-Pin Plastic DIP	0°C to +70°C	NE5181N
28-Pin PLCC	0°C to +70°C	NE5180A
28-Pin PLCC	0°C to +70°C	NE5181A

Octal differential line receivers | NE5180/NE5181

ABSOLUTE MAXIMUM RATINGS T_A = +25°C

SYMBOL	PARAMETER	RATING	UNIT
P_D	Power dissipation	800	mW
V_{CC}	Supply voltage	7	V
V_{CM}	Common-mode range	±15	V
V_{ID}	Differential input voltage	±25	V
I_{SINK}	Output sink current	50	mA
V_{FS}	Failsafe voltage	–0.3 to V_{CC}	V
I_{OS}	Output short-circuit time	1	sec

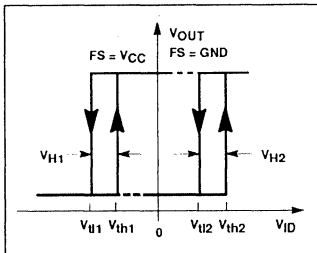


Figure 1. V_{tl}, V_{th}, V_H Definitions

DC ELECTRICAL CHARACTERISTICS V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C, input common-mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS		NE5180 Min	NE5180 Max	NE5181 Min	NE5181 Max	UNIT
R_{IN}	DC input resistance	3V ≤ $\|V_{IN}\|$ ≤ 25V		3	7	3	7	kΩ
V_{OFS}	Failsafe output voltage	Inputs open or shorted to GND	0 ≤ I_{OUT} ≤ 8mA, $V_{failsafe}$ = 0V		0.45		0.45	V
			0 ≥ I_{OUT} ≥ –400µA, $V_{failsafe}$ = V_{CC}	2.7		2.7		
V_{TH}	Differential input high[4] threshold	V_{OUT} ≥ 2.7V, I_{OUT} = –440µA	R_S = 0[1]		0.2		0.2	V
			R_S = 500[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	V_{OUT} ≤ 0.45V, I_{OUT} = 8mA	R_S = 0[1]	–0.2		–0.2		V
			R_S = 500[1]	–0.4		–0.4		
V_H	Hysteresis[4]	FS = 0V or V_{CC} (See Figure 1)		50	140	50	140	mV
V_{IOC}	Open-circuit input voltage				2		2	V
C_I	Input capacitance				30		30	pF
V_{OH}	High level output voltage	V_{ID} = 1V, I_{OUT} = –440µA		2.7		2.7		V
V_{OL}	Low level output voltage	V_{ID} = –1V	I_{OUT} = 4mA[2]		0.4		0.4	V
			I_{OUT} = 8mA[2]		0.45		0.45	
I_{OS}	Short-circuit output current	V_{ID} = 1V, Note 3		20	100	20	100	mA
I_{CC}	Supply current	4.75V ≤ V_{CC} ≤ 5.25V, V_{ID} = –1V; FS = 0V			100		100	mA
I_{IN}	Input current	Other inputs grounded	V_{IN} = +10V		3.25		3.25	mA
			V_{IN} = –10V	–3.25		–3.25		

NOTES:
1. R_S is a resistor in series with each input.
2. Measured after 100ms warm-up (at 0°C).
3. Only 1 output may be shorted at a time and then only for a maximum of 1 second.
4. See Figure 1 for threshold and hysteresis definitions.

AC ELECTRICAL CHARACTERISTICS V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C

SYMBOL	PARAMETER	TEST CONDITIONS	NE5180 Min	NE5180 Max	NE5181 Min	NE5181 Max	UNIT
t_{PLH}	Propagation delay—low to high	C_L = 50pF, V_{ID} = ±1V		500		100	ns
t_{PHL}	Propagation delay—high to low	C_L = 50pF, V_{ID} = ±1V		500		100	ns
f_a	Acceptable input frequency	Unused input grounded, V_{ID} = ±200mV[1]		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, V_{ID} = ±500mV	5.5		NA		MHz

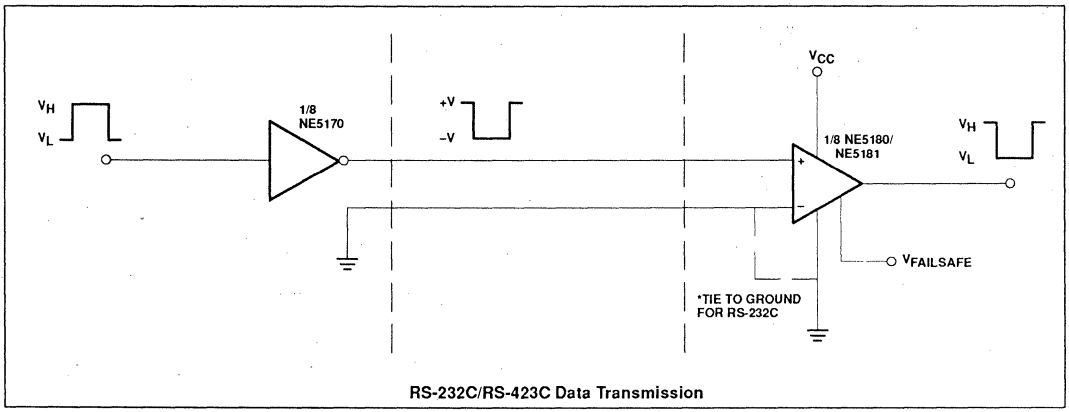
NOTE:
1. V_{ID} = ±1V for NE5181.

Octal differential line receivers | NE5180/NE5181

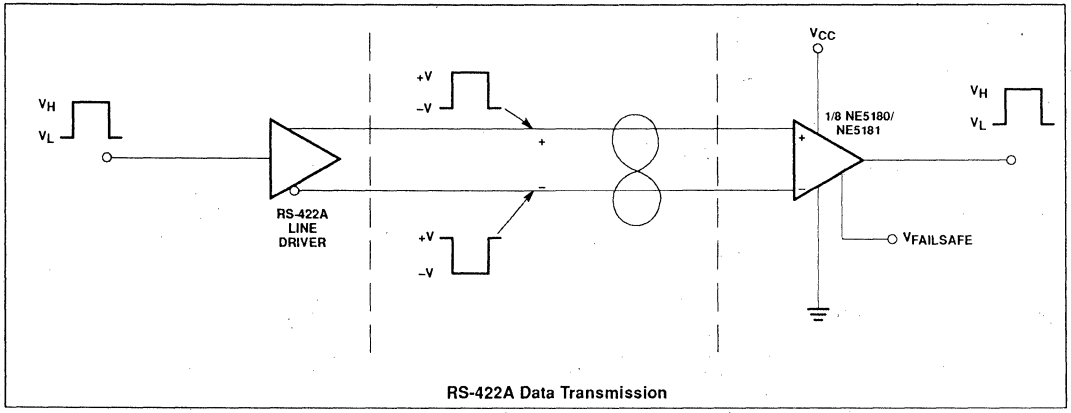
FAILSAFE OPERATION

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS-422A and RS-423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to

APPLICATIONS

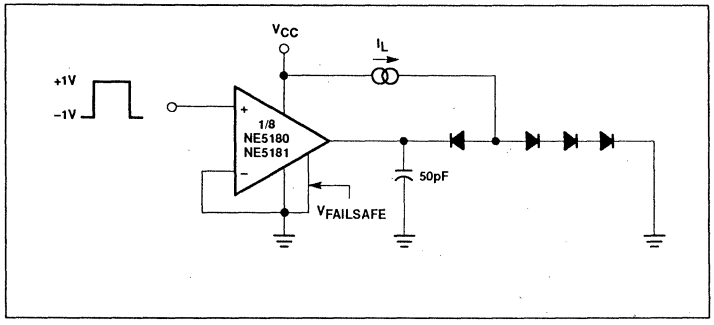


RS-232C/RS-423C Data Transmission

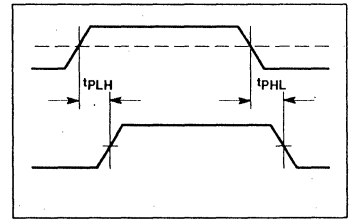


RS-422A Data Transmission

AC TEST CIRCUIT



VOLTAGE WAVEFORMS



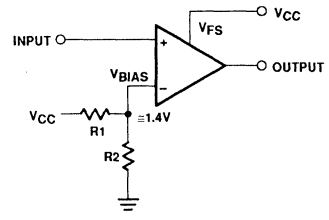
V_{CC} provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

RS-232 FAILSAFING

The internal failsafe circuitry works by providing a small input offset voltage which can be polarity-switched by using the failsafe control pins. This offset is kept small (approximately 80mV) to avoid degradation of the ±200mV input threshold for RS-423 or RS-422 operation. If the positive and negative inputs to any receiver are both shorted to ground or open circuited, the internal offset drives that output to the programmed failsafe state. If only one input open circuits (as may be the case for RS-232 operation), that input will rise to the "input open circuit voltage" (approximately 700mV). Since this is much greater than the 200mV threshold, the output will be driven to a state that is independent of the failsafe programming. Failsafe programming can be achieved for non-inverting single-ended applications by raising or lowering the unused input bias voltage as shown in Figure 2. For $V_{BIAS} \cong 1.4$, an open (or grounded) INPUT line will be approximately 700mV (0V) and the output will failsafe low. If the resistor divider is not used and V_{BIAS} is connected to ground, the output will failsafe high due to the internal failsafe offset for the INPUT grounded and the 700mV "open circuit input voltage" for the INPUT open circuited. Similar operation holds for an inverting configuration, with V_{BIAS} applied to the positive input and V_{FS} = ground.

INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ±500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).



NOTE:
Two silicon diodes may be used in place of R2.

Figure 2. Single-Input Failsafe Programming

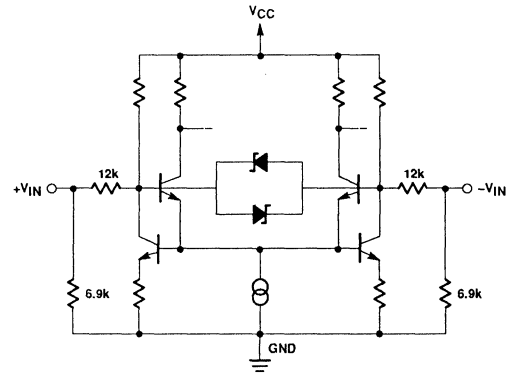


Figure 3. Differential Input Stage

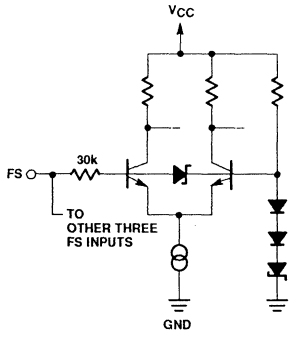


Figure 4. Failsafe Input Stage

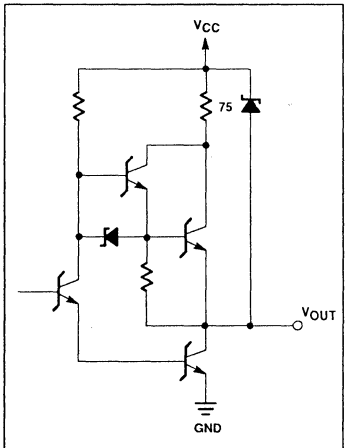


Figure 5. Output Stage

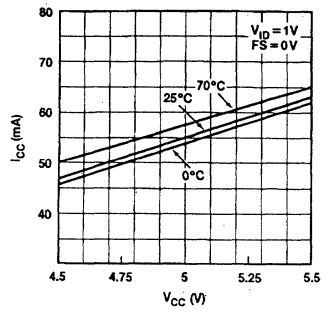


Figure 6. Typical Supply Current vs Supply Voltage

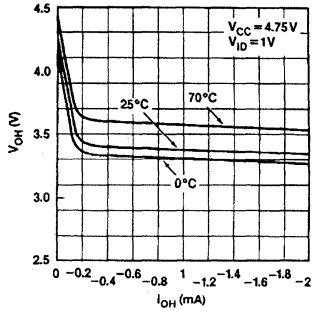


Figure 7. Typical High Level Output Voltage vs Output Current

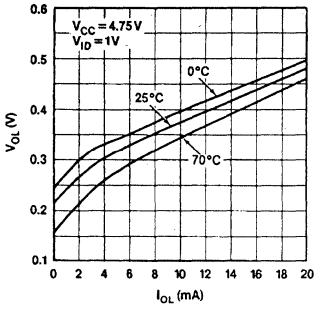
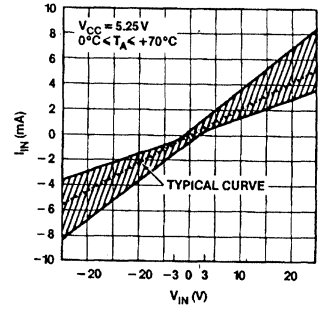


Figure 8. Typical Low Level Output Voltage vs Output Current



*This graph applies for all receiver inputs, provided that the opposite polarity input of the amplifier being measured is grounded.

Figure 9. Input Current vs Input Applied Voltage*

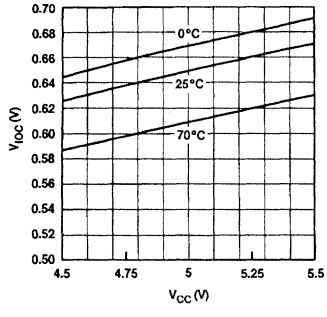


Figure 10. Typical V_{IOC} vs V_{CC}

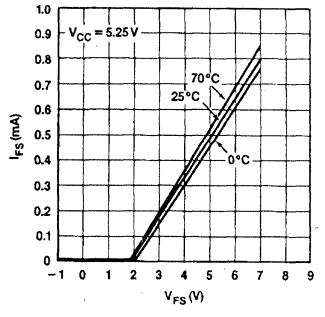


Figure 11. Typical FS Input Current vs FS Applied Voltage

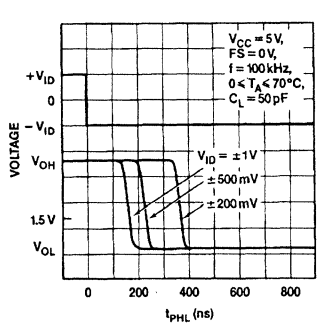


Figure 12. NE5180: Propagation Delay at Various Input Amplitudes

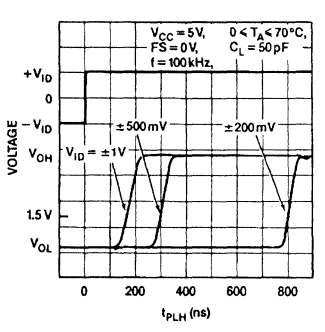


Figure 13. NE5180: Propagation Delay at Various Input Amplitude

Section 4
Local Area Network Products

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Philips Components–Signetics

Document No.	853–1449
ECN No.	99960
Date of Issue	July 11, 1990
Status	Product Specification
Data Communication Products	

NE502A
Ethernet encoder/decoder

DESCRIPTION

The NE502A is an Ethernet™ encoder/decoder designed to meet all the requirements of the IEEE 802.3 and Ethernet/Thin Ethernet specification and fabricated with high-speed ECL and Schottky TTL technology.

The encoder converts serial binary data into complementary Manchester code. The decoder converts Manchester code into binary data and synchronous clock signals. The decoding method is a digital phase locked loop with dual bandwidth which allows both fast lock-on and low jitter. Typical acquisition is eight bits or better. A key feature of the decoder design is its capability to recover distorted input signals. The NE502A is packaged in a standard 24-pin ceramic DIP.

The NE502A is normally part of a 3-chip set that implements a complete Ethernet/Thin Ethernet interface for a DTE. The other chips are an Ethernet Data Link Controller (EDLC) such as the NE86950 and a coaxial transceiver interface (CTI) such as the NE8392A.

FEATURES

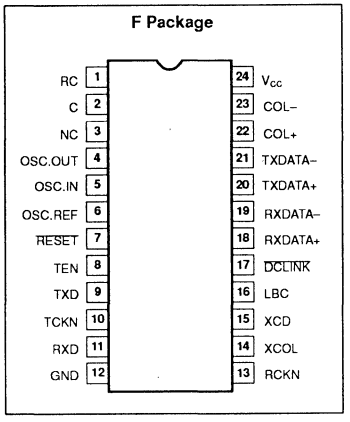
- Full Ethernet II, IEEE 802.3 10base5 and 10base2 compatibility
- Manchester encode and decode
- Level conversion: transceiver level to/from TTL level
- Carrier detection
- Large distortion recovery: ±20ns
- Dual bandwidth phase locked loop: allows fast acquisition
- Loopback "CONFIDENCE" test feature
- Built-in clock generator
- Small external parts count:
- High-speed ECL and Schottky TTL technology
- Single power supply: +5V
- Low power dissipation: 750mW typ.
- 24-pin standard dual in-line ceramic package

APPLICATION

- Workstations
- Terminals
- File servers
- Print servers

PIN CONFIGURATION

F Package

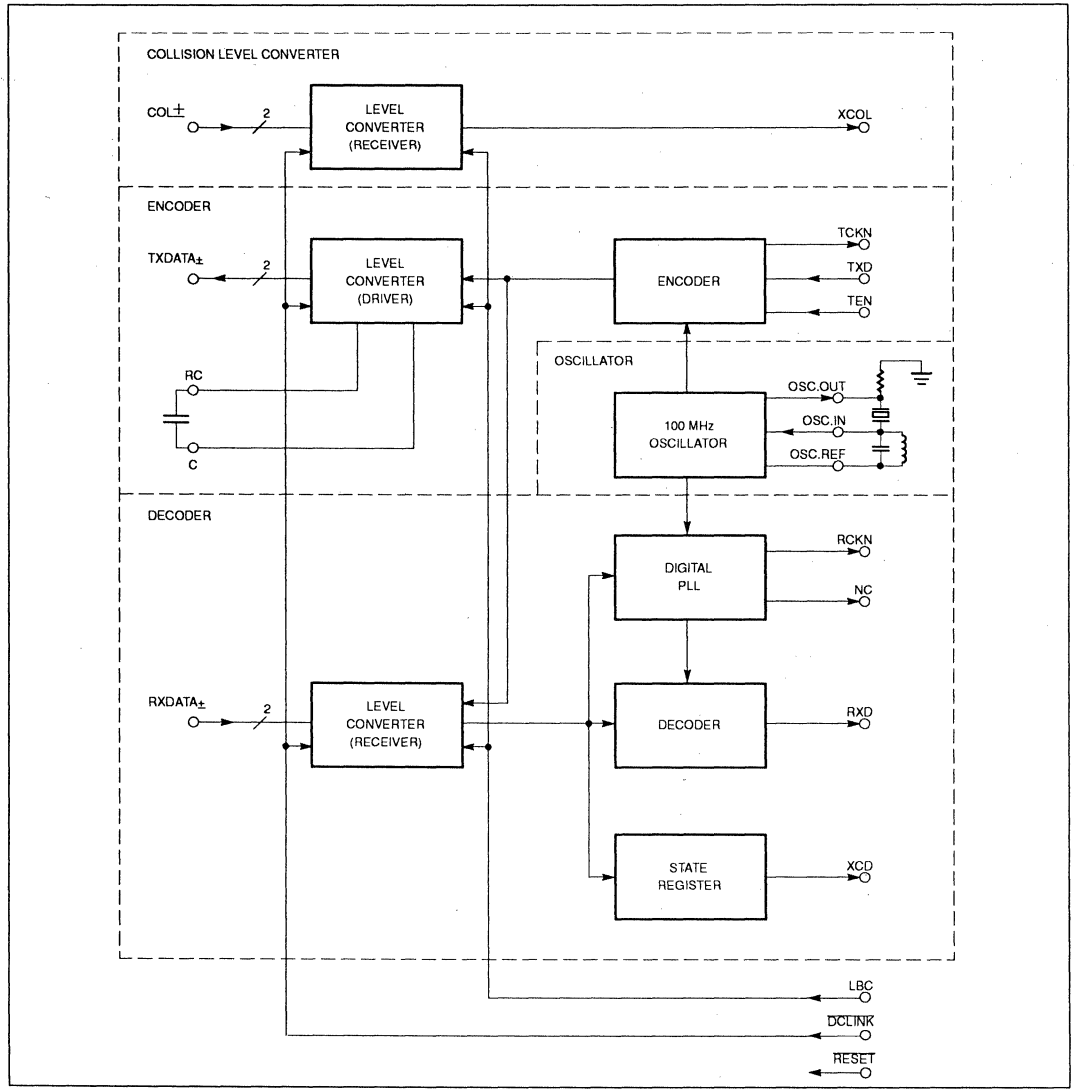


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Ceramic DIP	0°C to 70°C	NE502AF

*Ethernet™ is a Trade Mark of Xerox Corp., USA

BLOCK DIAGRAM



PIN ASSIGNMENT TABLE

PIN NO.	SYMBOL	PIN NAME	I/O	LEVEL	FUNCTION
Power Group					
12	GND	Power supply	I	—	Ground
24	V_{CC}	Power supply	I	—	+5V DC power Supply
Cable Group					
18 19	RXDATA+ RXDATA–	Receive data pair	I I	ECL differential	Interfacing to receive pair of the transceiver.
20 21	TXDATA+ TXDATA–	Transmit data pair	O O	ECL differential	Interfacing to transmit pair of the transceiver.
22 23	COL+ COL–	Collision presence pair	I I	ECL differential	Interfacing to collision presence pair of the transceiver.
EDLC Group					
8	TEN	Transmit encode enable	I	TTL	Input for encoding and TXDATA± enable.
9	TXD	Transmit serial data	I	TTL	Input for transmit data to be encoded onto the Ethernet coax.
10	TCKN	Transmit data clock	O	TTL	Stable 10MHz clock output for transmit bit stream.
11	RXD	Receive serial data	O	TTL	Output of received and decoded bit stream.
13	RCKN	Receive data clock	O	TTL	Clock output to strobe RXD.
14	XCOL	Collision presence	O	TTL	Duplication of the collision presence pair (COL±).
15	XCD	Receive carrier detect	O	TTL	Carrier detect function of the decoder.
16	LBC	Loopback command	I	TTL	Input to command the NE502A to operate in loopback mode.
Oscillator Group					
4 5 6	OSC. OUT OSC. IN OSC. REF	Oscillator pins	O I O	ECL	Pins for direct connection of discrete oscillator components.
Others					
1 2	RC C	Capacitor pins	— —	ECL —	Pins for direct connection of a capacitor.
3	NC	Non-connection (PLL test)	O	ECL	Output pin for PLL testing purpose only.
7	RESET	FF test	I	TTL	Input pin to initialize flip-flops for testing purpose only.
17	DCLINK	DC/AC coupling select for transceiver pairs	I	TTL	Input to select DC/AC coupling of transceiver cable pairs.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply Voltage	–0.3 to 7.0	V
V_{ITTL}	TTL Level Input Voltage	–0.3 to 7.0	V
V_{IR}	Receiver Input Voltage	–0.3 to V_{CC} + 0.3	V
V_{ODV}	Driver Output Voltage	V_{CC} (max)	V
I_{ODV}	Driver Output Current	–40.0 to 0	mA
V_{IOSC}	Oscillator Input Voltage	V_{CC}–4 to V_{CC} and < –0.3	V
I_{OOSC}	Oscillator Output Current	–20.0 to 0	mA
T_{OP}	Operating Temperature	–25 to 100	°C
T_{STG}	Storage Temperature	–65 to 125	°C

NOTE:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply Voltage		5.0V ± 5%	0°C to +70°C
I_{OH}	TTL High Level Output Current		–0.4mA to 0mA	
I_{OL}	TTL Low Level Output Current		0mA to 8mA	
V_{IR}	Receiver Input Voltage		0V to V_{CC}	
R_{LD}	Driver Terminator		270Ω	
R_{DLD}	Differential Load		78Ω	
R_{LOSC}	Oscillator Terminator		330Ω and 33pF parallel[1]	
f_{XTAL}	Crystal for Oscillator		100MHz ± 0.01%[2]	
C_{TX}	Capacitor placed between C and RC pins		470pF	
L_{OSC}	LC Tank Constant	Inductance	0.15µH	
C_{OSC}		Capacitance	33pF[1]	

NOTES:
1. The values of the oscillator capacitors may have to be tuned for a particular components layout. Both capacitors should be adjusted for maximum voltage at OSC.IN. However, once the correct values are determined for that layout, any more tuning will not be necessary for each board.
2. 5th overtone series resonant.

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	V_{CC} (V)	VALUE			UNIT
				Min	Typ	Max	
V_{IH}	High level input voltage[1]			2.0			V
V_{IL}	Low level input voltage[1]					0.8	V
V_{IC}	Input clamp voltage[1]	I_{IL} = –18mA	4.75	–1.5			V
V_{OH}	High level output voltage[2]	I_{OH} = –0.4mA	4.75	2.7			V
V_{OL}	Low level output voltage[2]	I_{OL} = 8mA	4.75			0.5	V
I_{IH}	High level input current[1]	V_{IH} = 2.7V	5.25			20	µA
I_{IL}	Low level input current[1]	V_{IL} = 0.4V	5.25	–100			µA
I_{OS}	Output short current[2]	V_O = 0V	5.25	–100		–20	mA
V_{IHD}	High level differential input voltage[3]	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 0V		0.2			V
V_{ILD}	Low level differential input voltage[3]	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 0V				–0.2	V
V_{IHD}	High level differential input voltage[4]	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V		–0.05			V
V_{ILD}	Low level differential input voltage[4]	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V				–0.4	V
V_{IHD}	High level differential input voltage[5]	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V		0.2			V
V_{ILD}	Low level differential input voltage[5]	$V_{IR+} - V_{IR-}$, $\overline{DCLINK}$ = 4.5V				–0.2	V
I_{IHR}	High level input current[3]	V_{IR} = 5.25V, $\overline{DCLINK}$ = 0V	5.25			0.7	mA
I_{ILR}	Low level input current[3]	V_{IR} = 0V, $\overline{DCLINK}$ = 0V	5.25	–1.5			mA
V_{OHTX}	High level output voltage[6]		5.0		4.1		V
V_{OLTX}	Low level output voltage[6]		5.0		3.3		V
V_{OHD}	High level differential output voltage[6]	$V_{O+} - V_{O-}$, $\overline{DCLINK}$ = 0V		0.55		1.0	
V_{OLD}	Low level differential output voltage[6]	$V_{O+} - V_{O-}$, $\overline{DCLINK}$ = 0V		–1.0		–0.55	
V_{BB}	Oscillator reference voltage[7]		5.0		3.7		V
I_{IHO}	High level input current[8]	V_{IH} = 4.1V	5.0			150	µA
V_{OHO}	High level output voltage[9]	OSC.IN is open	5.0		4.15		V
V_{OLO}	Low level output voltage[9]	V_{IOSC} = 4.1V	5.0		3.3		V
R_{RC}	RC internal resistor	V_{RC} = 0.5V	0.5	25	50	100	kΩ
I_{CC}	Power supply current	All signal pins are open.	5.25			220	mA

NOTES:
1. Applicable to TTL input pins. (TEN, TXD, LBC, $\overline{DCLINK}$ and $\overline{RESET}$)
2. Applicable to TTL output pins. (TCKN, RXD, RCKN, XCOL and XCD)
3. Applicable to COL± and RXDATA±.
4. Applicable to RXDATA± while XCD output is low (idle state) and COL±.
5. Applicable to RXDATA± while XCD output is high.
6. Applicable to TXDATA±. These pins are connected to ground through 270Ω resistors. A 78Ω resistor is placed between these pins.
7. Applicable to OSC.REF.
8. Applicable to OSC.IN.
9. Applicable to OSC.OUT. This pin is connected to ground through a 330Ω resistor.

AC CHARACTERISTICS Recommended operating conditions unless otherwise noted. V_{CC} = 5.0V. Transmit Timing (Figure 22)

SYMBOL	PARAMETER	CONDITION	VALUE			UNIT
			Min	Typ	Max	
Transmit timing (Figure 1)						
t_{CTTC}	TCKN cycle time	(Figures 2,3)	99.99	100.00	100.01	ns
t_{WLTC}	TCKN low time	(Figures 2,3)	40	50		ns
t_{WHTC}	TCKN high time	(Figures 2,3)	40	50		ns
t_{PDTX}	TXDATA± encode time	(Figures 2,3)		95		ns
t_{RTX}	TXDATA± output rise time	(Figures 5,6)		2.0		ns
t_{FTX}	TADATA± output fall time	(Figures 5,6)		2.0		ns
t_{LTX}	TXDATA– low level hold time	C_{TX} = 470pF $\overline{DCLINK}$ = V_{CC} (Figures 5,6)		3		µs
t_{RLTX}	TXDATA– idling rise time	C_{TX} = 470pF, (20% ~ 80%), $\overline{DCLINK}$ = V_{CC} (Figures 5,6)		0.8		µs
t_{SUTX}	TXD, TEN setup time	(Figures 4)	20			ns
t_{HDTX}	TXD, TEN hold time	(Figures 4)	0			ns
Receive timing (Figures 2, 3)						
t_{CTRC}	RCKN cycle time in idle	(Figures 2,3)	99.99	100.00	100.01	ns
t_{WLRC}	RCKN low time	(Figures 2,3)	35	50		ns
t_{WHRC}	RCKN high time	(Figures 2,3)	35	50		ns
t_{PHLRC}	RCKN delay time	(Figures 2,3,7)		120		ns
t_{PLHCD}	XCD ON delay time	(Figures 2,3,7)		80	110	ns
t_{PHLCD}	XCD OFF delay time	(Figures 2,3,7)		230		ns
t_{HDLCD}	XCD low hold time	(Figures 2,3)	0	10		ns
t_{HDHCD}	XCD high hold time	(Figures 2,3)		120		ns
t_{SULCD}	XCD Low setup time	(Figures 2,3)		80		ns
t_{SURXD}	RXD setup time	(Figures 2,3)	20	60		ns
t_{HDRXD}	RXD hold time	(Figures 2,3)	10	20		ns
Loopback timing[1] (Figure 4)						
t_{PGLBC}	LBC receiving data purge time	(Figures 2,3,4)		230		ns
t_{ACLBC}	LBC receiving data accept time	(Figures 2,3,4)		80		ns
t_{PHLTRU}	DATA through time	(Figures 2,3,4)		280		ns
t_{WTEN}	TEN wait time	(Figures 2,3,4)	0			ns
Collision timing (Figure 5)						
t_{PLH}	COL to XCOL Propagation Delay Time	$\overline{DCLINK}$ = 0V, (Figures 2,3,7)		9	30	ns
t_{PHL}	COL to XCOL Propagation Delay Time	$\overline{DCLINK}$ = 0V, (Figures 2,3,7)		11	30	ns

NOTE:

1. In Loopback mode operation, COL± and RXDATA± inputs are ignored, TXDATA+ and XCOL are high level, and XCD, RCKN and RXD functions are in the same manner as a normal receive operation.

FUNCTIONAL DESCRIPTION

The NE502A has five major functions: encode, decode, collision signal conversion, master clock generation and loopback.

Encode

The encoder section of the NE502A is a simple circuit which performs an appropriate exclusive-OR between the transmit clock and transmit data using latches to reduce the skew of TXDATA± outputs. The encoder sends the transmit clock (TCKN) to an Ethernet Data Link controller (EDLC) such as the NE86950. An encode enable signal (TEN) and data (TXD) are then returned from the EDLC.

Decode

The decoder performs three functions. First, it decodes data arriving at the RXDATA± inputs and passes it to the EDLC via the RXD output. Second, it signals to the EDLC that receive carrier is present by asserting the XCD output. Third, the receive clock is recovered and passed to the EDLC via the RCKN output. The RCKN is inhibited for 6 or 7 cycles during PLL acquisition, but, upon restarting, has the correct phase relationship with the recovered data.

The decoder PLL is a digital phase locked loop with excellent distortion handling capability. It is designed to recover data from ±20ns of jitter.

Collision

In the event of a collision, the 10MHz collision signal sent from the transceiver to the COL+ inputs is converted to a TTL 10MHz signal at the XCOL pin. The latching and timing functions for this signal are provided in the EDLC (NE86950).

Master Clock Generation

The oscillator generates a 100MHz master clock for the encoder and decoder.

Discrete oscillator components and a crystal are directly connected to the provided oscillator pins. The oscillation frequency must be 100MHz with a tolerance of less than ±0.01% to meet the IEEE 802.3 specification because one tenth of the oscillation frequency is the transmit bit rate.

Loopback

A loopback input (LBC) is provided to allow all encoding and decoding functions to be exercised without using the transceiver cable. During loopback operation, the encoded data is routed internally to the decoder, while transmit outputs remain idle and the receive and collision inputs are ignored.

SIGNAL PIN DESCRIPTION

Cable Group

RXDATA± (receive serial data pair, inputs): These are the inputs to the decoder. They receive Manchester coded signals from the transceiver. The input circuit is a differential receiver and with a common mode voltage range of 0 to V_{CC}. The differential receiver has two modes of operation: DC coupled operation and AC coupled operation, which are selected by the $\overline{DCLINK}$ input.

In DC coupled operation ($\overline{DCLINK}$ is low), the differential squelch threshold is typically –0V.

In AC coupled operation ($\overline{DCLINK}$ is high), the differential squelch threshold is typically –0.2V. This is the operating mode for coaxial Ethernet where an isolation transformer is used between the encoder/decoder and the transceiver.

In both DC and AC coupled operation, the differential zero crossing threshold for the received signal is 0V in order to minimize receive distortion. When RXDATA± are idle, the RXD output is a TTL high.

TXDATA± (transmit data pair, outputs): These are the outputs of the encoder. They transmit Manchester coded signals to the transceiver.

The driver output circuits are emitter followers and require pull-down resistors of 270Ω. They can drive a transceiver cable with differential impedance of 78Ω.

The differential transmitter outputs TXDATA± are normally connected directly to the primary of an isolating pulse transformer. In idle state they have a low offset voltage in order to minimize DC current through the transformer. When entering the idle state, at the end of a transmit packet, the transmitter outputs gradually return to a differential voltage of 0V across the transformer primary in order to prevent undershoot glitches at the transformer secondary. The returning time constant is determined by an external capacitor connected between the RC and C pins.

COL± (collision presence pair, inputs): This pair of inputs receive a 10MHz signal from the transceiver when a collision is detected.

The input circuit has the same common mode voltage range as the RXDATA± inputs. It also operates in DC or AC coupled modes, depending on whether $\overline{DCLINK}$ is low or high respectively, with the same differential squelch thresholds of 0V or –0.2V, respectively.

Unlike the RXDATA± inputs, the zero crossing threshold is –0.2V even when COL± are receiving a collision present signal.

When COL± are idle, the XCOL output is a TTL high.

EDLC Group

TEN (transmit encode enable, input): This is an input to the on-chip Manchester encoder and enables the TXDATA± pair. An input high enables the TXDATA± pair; an input low makes the TXDATA± pair idle (high).

TXD (transmit serial data, input): This is an input to the on-chip Manchester encoder and provides the data to be encoded.

Serial binary data must be supplied to this input synchronously with the falling edge of TCKN (transmit data clock).

This input is enabled when TEN (transmit encode enable) is high.

TCKN (transmit data clock, output): A 10MHz clock output for the transmit serial binary data. This is a stable clock of one-tenth of the master clock frequency. See TXD (transmit serial data) description.

RXD (receive serial data, output): This is an output of the on-chip Manchester decoder and provides decoded data to the EDLC.

This output is synchronous with the falling edge of RCKN (receive data clock).

RCKN (receive data clock, output): Clock output to strobe RXD (receive serial data). See RXD (receive serial data) description.

At the beginning of a packet, RCKN is inhibited for 6 or 7 clock cycles to allow the PLL to gain acquisition. At the end of a packet, RCKN is inhibited for 1 clock cycle.

During idle state, this output generates a 10MHz clock signal.

XCOL (collision presence, output): This is a TTL duplication of the collision signal at COL±. The transceiver connected to the Ethernet coax supplies a high level or differential voltage of 0V to COL± when a collision is not present on the coax. It supplies a 10MHz square wave signal to COL± when a collision is detected. Accordingly, XCOL outputs a high level when collision is not see and outputs a 10MHz square wave signal during collision presence.

XCD (receive carrier detect, output): This output provides the carrier detect function of the Manchester decoder. This signal is used by the receive section of the Data Link controller as a data acquisition enable signal and by the transmit section as transmission permission information.

Output is low when the Ethernet coax is idle.

LBC (loopback command, input): A high level input to this pin dictates loopback mode operation. During the loopback mode operation, XCOL output is a high level, TXDATA± outputs are high level, RXDATA± inputs are ignored. The data supplied to TXD (transmit serial data) when TEN (transmit encode enable) is high is encoded, internally routed back to the Manchester decoder and output from RXD (receive serial data), RCKN (receive data clock) and XCD (receive carrier detect).

Oscillator Group

OSC.OUT, OSC.IN, and **OSC.REF** (oscillator pins): A 100MHz crystal is placed between OSC.IN and OSC.OUT.

An LC tank circuit is placed between OSC.IN and OSC.REF to assure start-up at the proper harmonic of the crystal.

OSC.OUT is an emitter-follower output and requires a pull-down resistor (330Ω typ.). A phase adjusting capacitor is placed in parallel with the pull-down resistor to make the delay through the oscillator close to 10ns to increase the efficiency of the crystal.

As a design recommendation, connection wires should be as short as possible.

Others

RC and **C** (capacitor pins): A capacitor placed between these pins provides the timing for the active-to-idle time of the TXDATA± pair.

In AC coupled operation ($\overline{\text{DCLINK}}$ is high), after data transmission, TXDATA– goes high with rise time determined by the time-constant of the internal resistor and the connected capacitor. When a 470pF capacitor is connected, the rise time of TXDATA– is typically 0.8µs (20% to 80%).

Because pin C is connected to V_{CC} on chip, DC voltage must never be supplied to this pin.

$\overline{\text{DCLINK}}$ (DC/AC coupling select for transceiver pair): This input is to select DC/AC coupling of the transceiver cable pairs. A low level selects DC coupling; a high level selects AC coupling and makes both TXDATA± high during idle state to prevent the transformer core from saturating. See CABLE GROUP description.

This pin must be connected to a TTL high or low. It may be connected directly to V_{CC} or ground.

$\overline{\text{RESET}}$ (FF testing purpose only): This input pin is used to initialize flip-flops for testing purposes only and must be connected to V_{CC} or a TTL high level in a normal operation.

NC (non-connection): This output pin is for testing purposes only and must be left open in a normal operation.

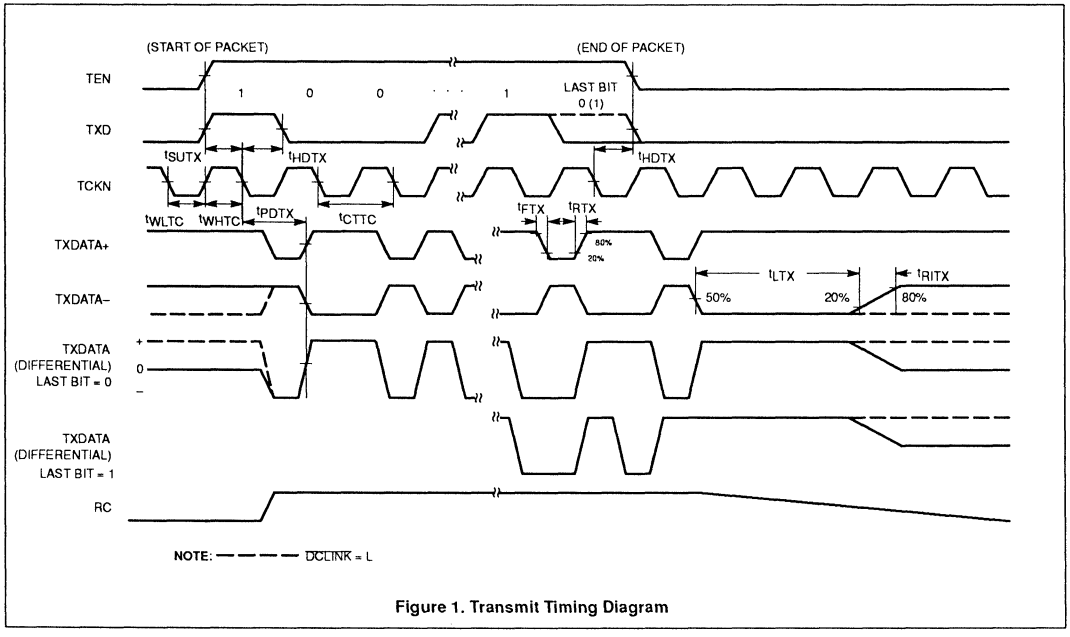


Figure 1. Transmit Timing Diagram

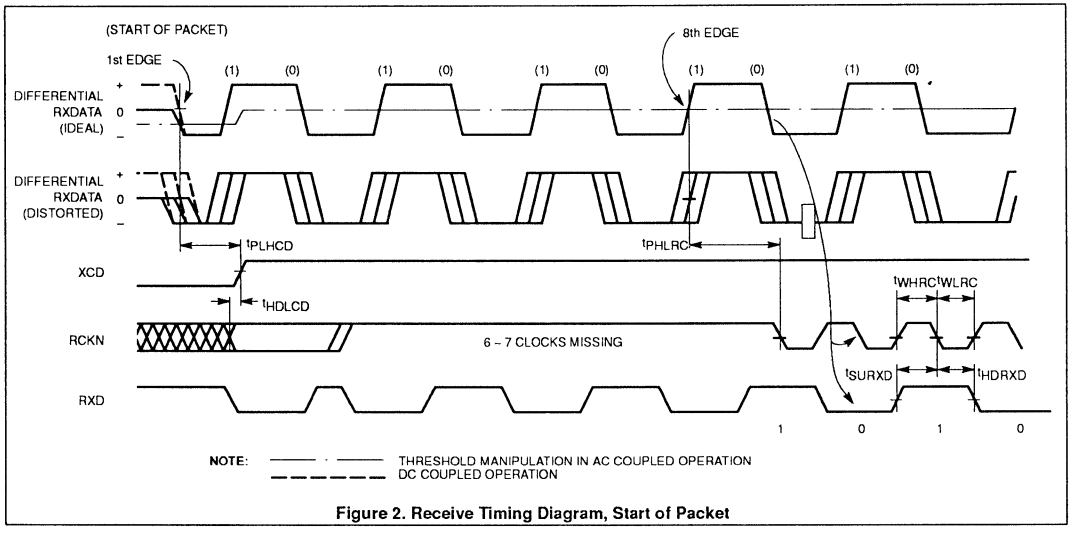


Figure 2. Receive Timing Diagram, Start of Packet

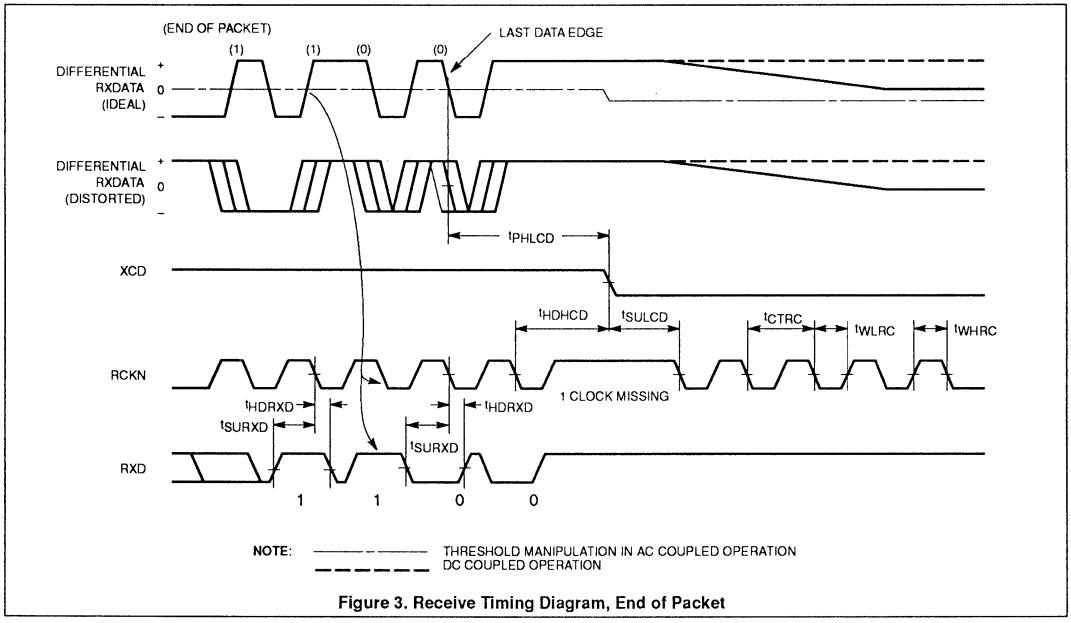
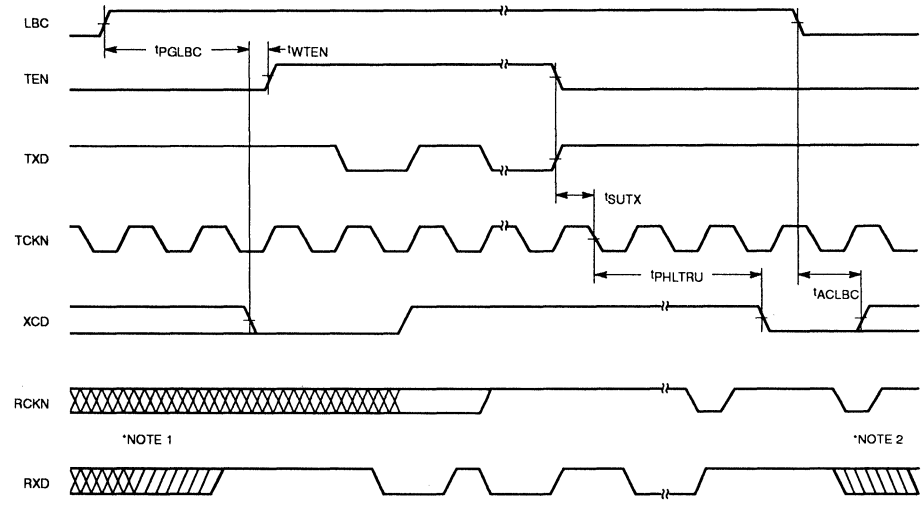


Figure 3. Receive Timing Diagram, End of Packet



NOTE 1: WHEN RXDATA± ARE RECEIVING A PACKET AT LBC RISING, THE RECEIVED DATA IS NOT COMPLETE.
NOTE 2: WHEN RXDATA± ARE RECEIVING AT LBC FALLING, THE PACKET MAY NOT BE DECODED CORRECTLY.

Figure 4. Loopback Timing Diagram

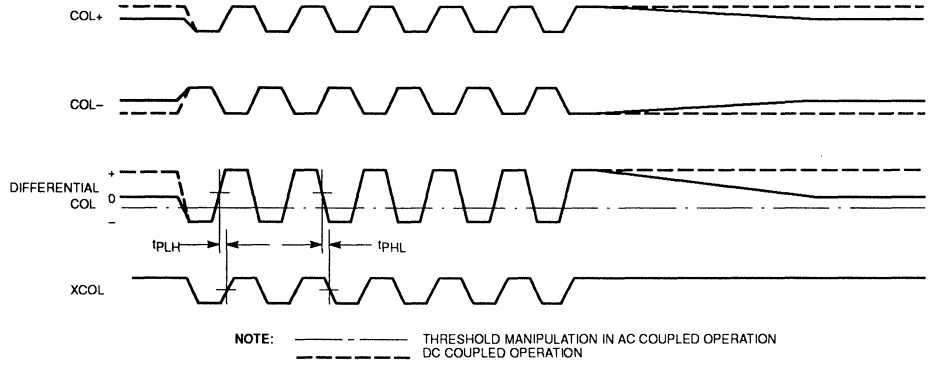


Figure 5. Collision Timing Diagram

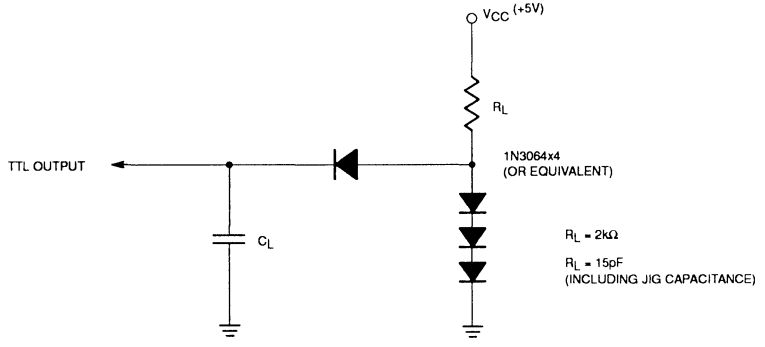


Figure 6. TTL Output Load Circuit

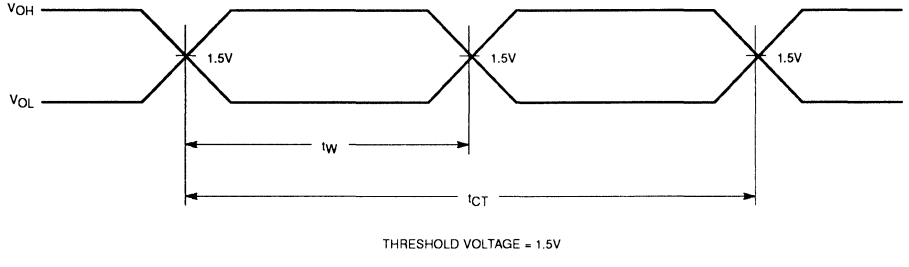


Figure 7. TTL Output Waveform

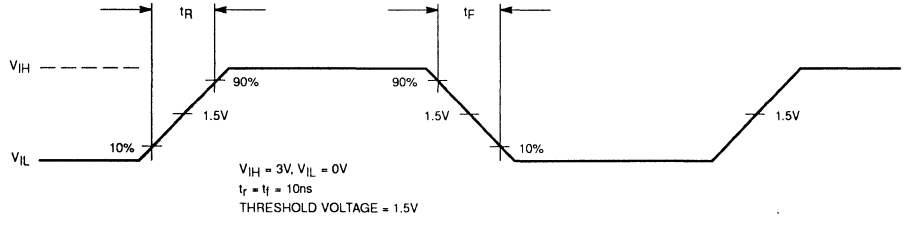


Figure 8. TTL Input Waveform

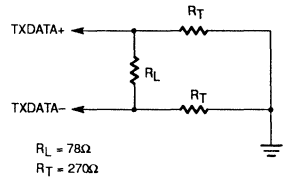


Figure 9. TXDATA± Output Load Circuit

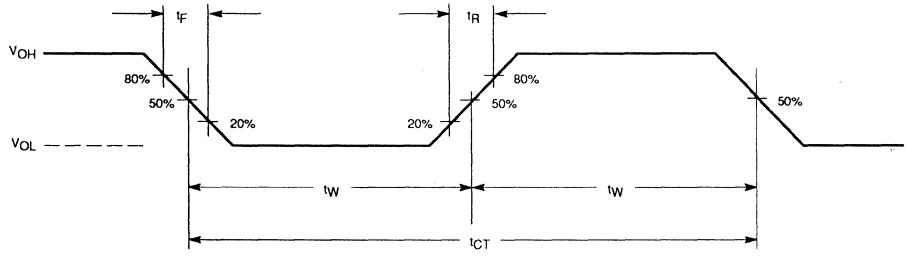


Figure 10. TXDATA± Output Waveform

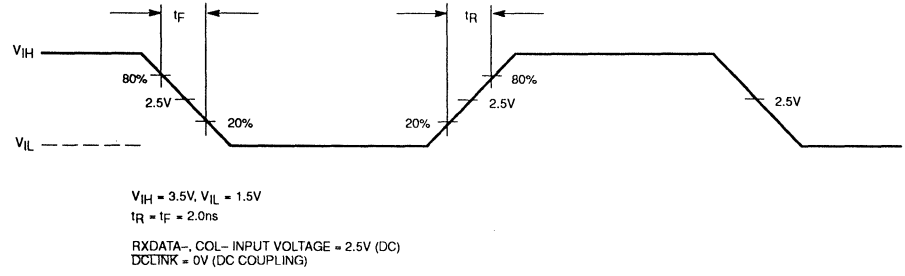


Figure 11. RXDATA+, COL+ Input Waveform

TYPICAL TIMING CHARACTERISTICS

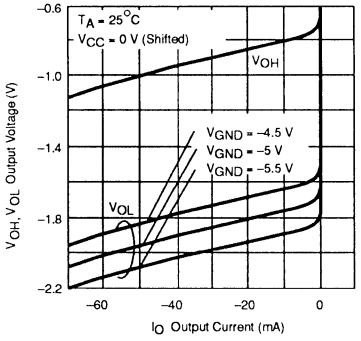


Figure 12. TXDATA± Output Voltage vs Output Current

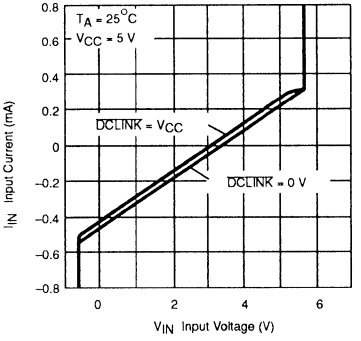


Figure 13. RXDATA±, COL± Input Current vs Input Voltage

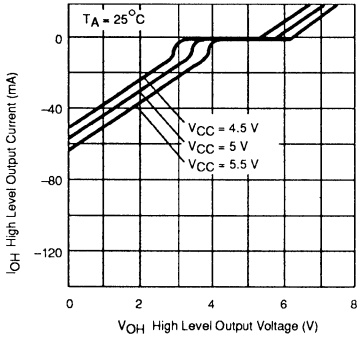


Figure 14. TTL-OUTPUT High Level Output Current vs High Level Output Voltage

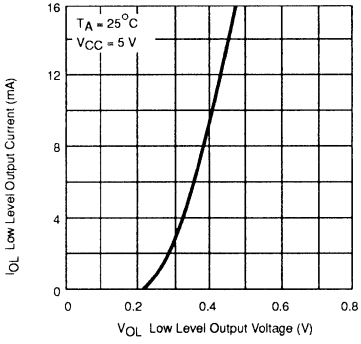


Figure 15. TTL-OUTPUT Low Level Output Current vs Low Level Output Voltage

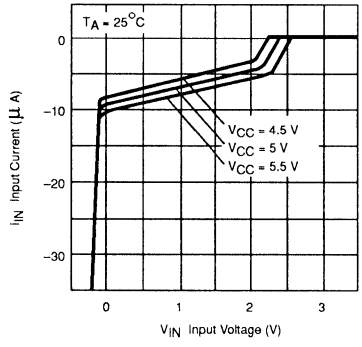


Figure 16. TTL-INPUT Input Current vs Input Voltage

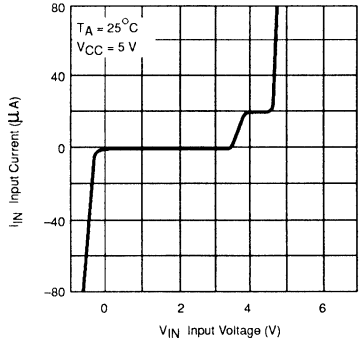


Figure 17. OSC.IN Input Current vs Input Voltage

TYPICAL TIMING CHARACTERISTICS

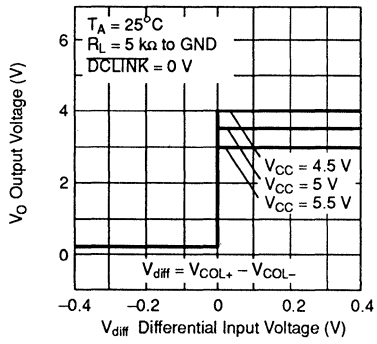


Figure 18. COL± to XCOL TRANSFER (Receiver Threshold) Output Voltage vs Differential Input Voltage

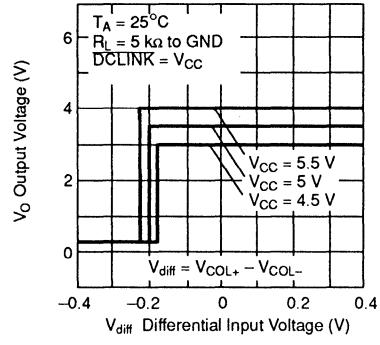


Figure 19. COL± to XCOL TRANSFER (Receiver Threshold) Output Voltage vs Differential Input Voltage

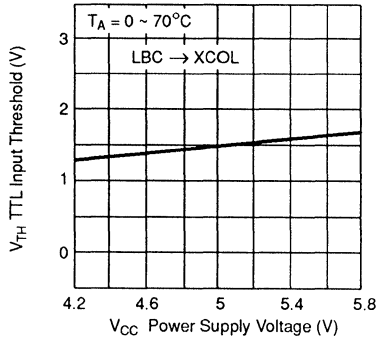


Figure 20. TTL-INPUT THRESHOLD TTL Input Threshold vs Power Supply Voltage

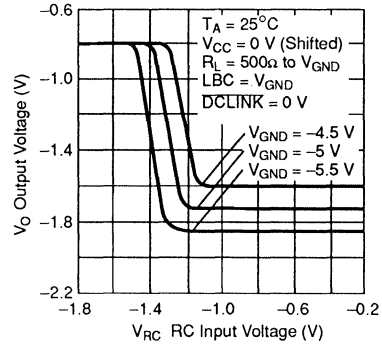


Figure 21. RC to TXDATA– TRANSFER Output Voltage vs RC Input Voltage

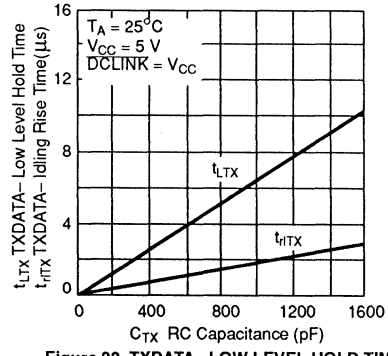


Figure 22. TXDATA– LOW LEVEL HOLD TIME TXDATA– Low Level Hold Time TXDATA– Idling Rise Time vs RC Capacitance

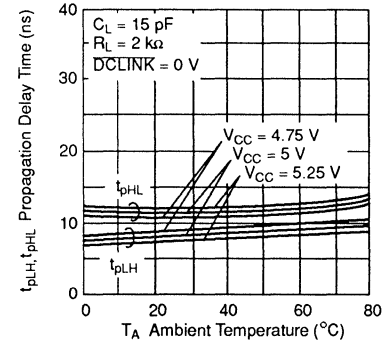
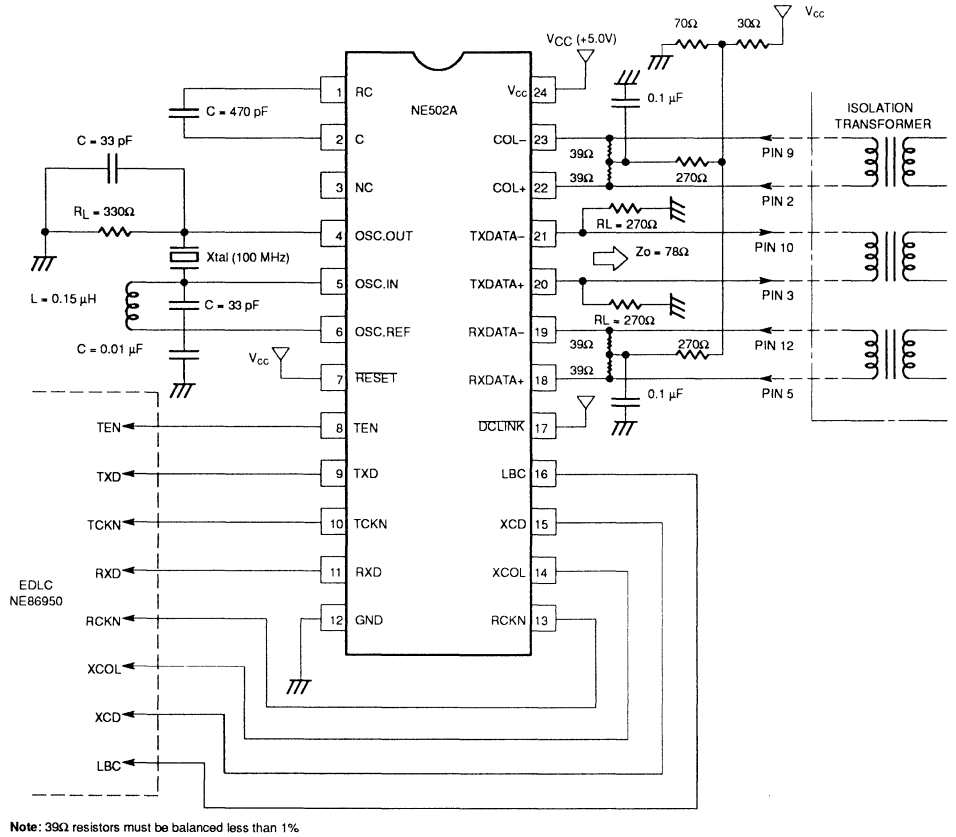


Figure 23. COL± to XCOL PROPAGATION DELAY TIME Propagation Delay Time vs Ambient Temperature



Note: 39Ω resistors must be balanced less than 1%

Figure 24. Typical Application Circuit

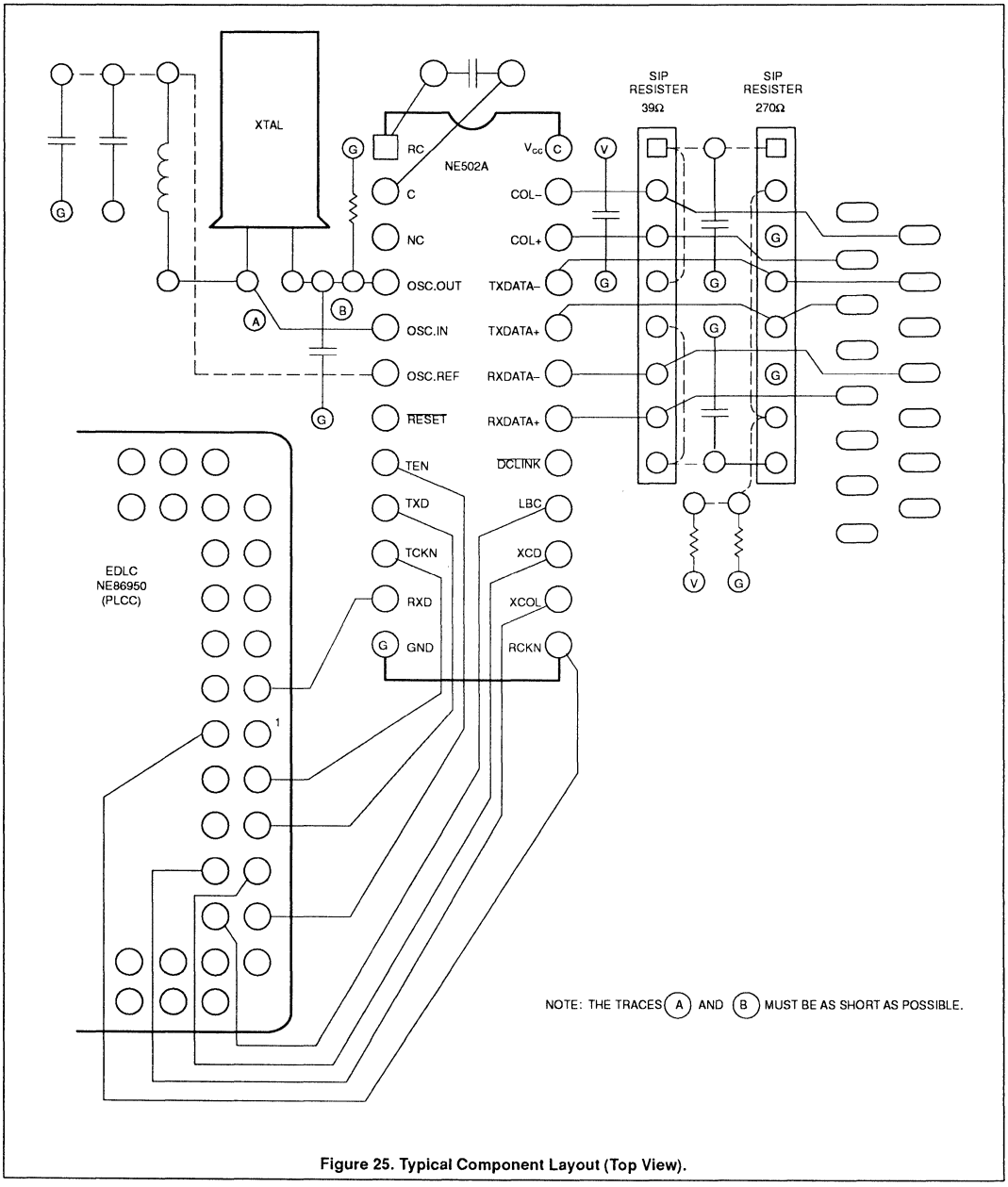


Figure 25. Typical Component Layout (Top View).

Philips Components–Signetics

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ECN No.	00665
Date of Issue	October 9, 1990
Status	Product Specification
Data Communication Products	

NE8392A

Coaxial transceiver interface for Ethernet/Thin Ethernet

DESCRIPTION

The NE8392A Coaxial Transceiver Interface (CTI) is a coaxial line driver/receiver for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers normally available in a standard 16-pin DIP. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer (see Figure 1, Connection Diagram).

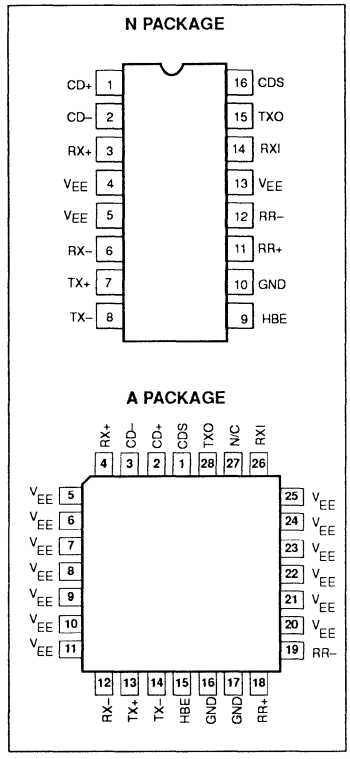
During transmission the jabber timer is initiated to disable the CTI transmitter in the event of a longer than legal length data packet. Collision detection circuitry monitors the signals on the coaxial cable to determine the presence of colliding packets and signals the DTE in the event of a collision. At the end of every transmission the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuitry is functioning correctly. The heartbeat function can be disabled for repeater applications.

The CTI is normally part of a three chip set that implements a complete Ethernet/ Thin Ethernet network interface for a DTE (see Figure 2, Interface Diagram). The other chips are a Serial Network Interface (SNI) and a Network Interface Controller (NIC). The SNI provides Manchester Encoding and Decoding while the NIC handles the media access protocol and buffer management tasks.

FEATURES

- Compatible with Ethernet II, IEEE 802.3 10base5 and 10base2, and ISO 8802/3 interface specifications
- Integrates all transceiver electronics except signal and power isolation
- Only one external resistor required for setting coaxial signaling current
- Jabber timer function integrated on chip
- Heartbeat generator can be externally disabled for operation as IEEE 802.3 compatible repeaters
- On-chip precision voltage reference for receive mode collision detection
- Squelch circuitry on all signal inputs rejects noise
- Full ESD protection
- Standard 16-pin DIP with special lead frame minimizes the operating die temperature
- Power-on reset prevents glitches on coaxial cable during power up.

PIN CONFIGURATION

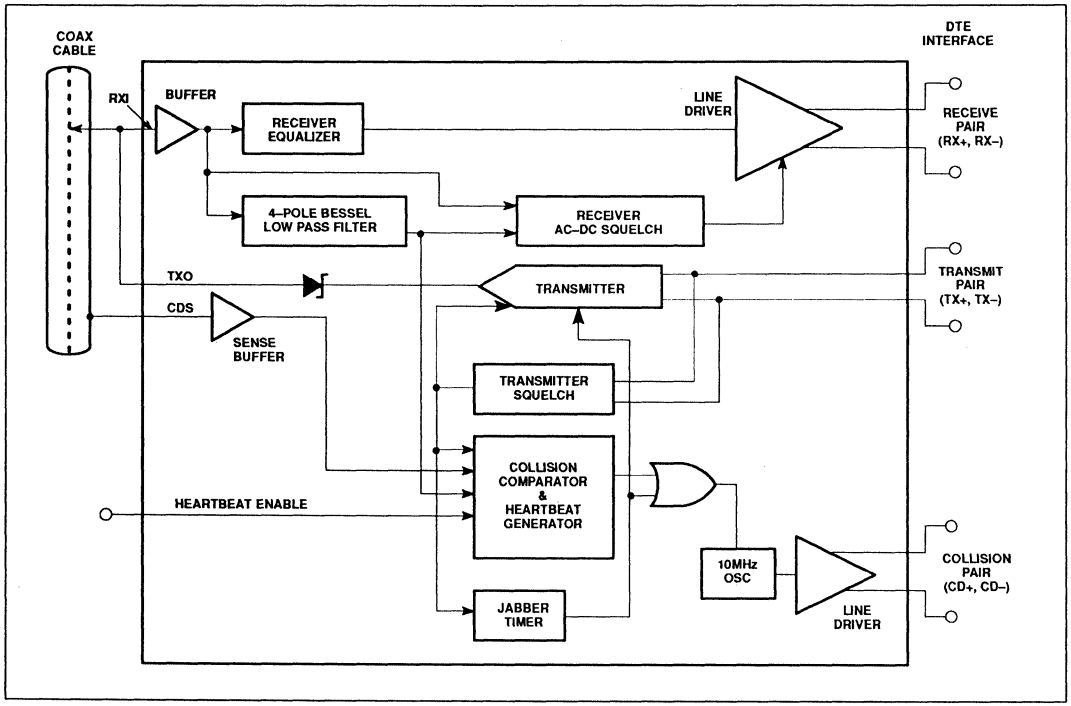


Coaxial transceiver interface for Ethernet/Thin Ethernet NE8392A

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	NE8392AN
28-Pin PLCC	0°C to +70°C	NE8392AA

BLOCK DIAGRAM



Coaxial transceiver interface for Ethernet/Thin Ethernet — NE8392A

PIN DESCRIPTIONS

PIN NO. N PKG	PIN NO. PLCC	SYMBOL	DESCRIPTION
1 2	2 3	CD+ CD–	Collision Outputs. Balanced differential line driver outputs which send a 10MHz oscillation signal to the DTE in the event of a collision, jabber interrupt or heartbeat test.
3 6	4 12	RX+ RX–	Receiver Outputs. Balanced differential line driver outputs which send the received signal to the DTE.
7 8	13 14	TX+ TX–	Transmitter Inputs. Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
9	15	HBE	Heartbeat Enable. The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR–	External Resistor. A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO. RR– is internally connected to V_{EE}.
14	26	RXI	Receiver Input. This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the $RX_{\pm}$ pins.
15	28	TXO	Transmitter Output. This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	Collision Detect Sense. Ground sense connection for the collision detection circuitry. This pin should be directly connected to the coaxial cable shield to prevent ground drops affecting the collision threshold voltage.
10	16 17	GND	Positive Supply Pin.
4 5 13	5 to 11 20 to 25	V_{EE}	Negative supply pins. These pins also serve as a low thermal resistance path for extracting heat from the die. They should, therefore, be connected to a large metal area on the PC board.

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage[1]	–12	V
V_{IN}	Voltage at any input[1]	0 to –12	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	+300	°C
T_J	Recommended max junction temperature[2]	+130	°C
θ_{JA}	Thermal impedance (N and A packages)	60	°C/W

NOTES:
1. 100% measured in production.
2. The junction temperature is calculated from the following expression:

$$T_J = T_A + \theta_{JA}[V_{EE}(0.075 + n \times 0.05/100) + 8(V_{EE} - 2) / R]$$

where
- T_A = Ambient temperature in °C.
- θ_{JA} = Thermal resistance of package.
- V_{EE} = Normal operating supply voltage in volts.
- n = Percentage transmitter duty cycle.
- R = Pull down resistors on the RX and CD pins in Ω.

The N package is specially designed to have a low θ_{JA} by directly connecting the four center Pins 4, 5, 12, and 13 to the die attachment area. These four pins then provide a conductive heat flow path from the die to the PCB where they should be soldered to a large area V_{EE} track. For the A package, Pins 5 to 11 and 19 to 25 should similarly be soldered to a large area V_{EE} and rack.

ELECTRICAL CHARACTERISTICS V_{EE} = –9V ±5%; T_A = 0°C to +70°C unless otherwise specified[1,2]. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{POR}	Power–on reset voltage. Transmitter disabled for $\|V_{EE}\| < \|V_{POR}\|$			–6.5		V
I_{EE}	Supply current non–transmitting			–80	–130	mA
	Supply current transmitting			–125	–180	mA
I_{RXI}	Receive input bias current	V_{RXI} = 0V	–2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+2	+6	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +1.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +0.4	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V		250	500	µA
I_{IL}	HBE input LOW current	V_{HBE} = V_{EE}		–500	–1000	µA
I_{TDC}	Transmit output DC current level[3]		–37		–45	mA
I_{TAC}	Transmit output AC current level[3]		±28		$\pm I_{TDC}$	mA
I_{TX10}	Transmit current	V_{TXO} = –10V	–250		+250	µA
V_{TCOM}	Transmitter output voltage compliance[4]				–3.7	V
V_{CD}	Collision threshold[5]	Measured by applying DC voltage at RXI	–1450	–1530	–1580	mV
V_{OD}	Differential output voltage – non idle at $RX_{\pm}$ and $CD_{\pm}$[6]		±600		±1200	mV
V_{OB}	Differential output voltage imbalance – idle at $RX_{\pm}$ and $CD_{\pm}$[7]				±40	mV
V_{OC}	Output common mode voltage at $RX_{\pm}$ and $CD_{\pm}$		–1.5	–2	–2.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC	–130	–250	–370	mV
V_{TS}	Transmitter squelch threshold	$(V_{TX+} - V_{TX-})$ peak	–175	–225	–300	mV
R_{RXI}	Shunt resistance at RXI non–transmitting		100			kΩ
C_{RXI}	Input capacitance at RXI			2		pF
R_{TXO}	Shunt resistance at TXO transmitting			10		kΩ

NOTES:

1. Currents flowing into device pins are positive. All voltages are referenced to ground unless otherwise specified. For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = –9V and T_A = 27°C.
3. I_{TDC} is measured as $(V_{MAX} + V_{MIN})/(2 \times 25)$ where V_{MAX} and V_{MIN} are the max and min voltages at TXO with a 25Ω load between TXO and GND. I_{TAC} is measured as $(V_{MAX} - V_{MIN})/(2 \times 25)$.
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is –3.7V.
5. Collision threshold for an AC signal is within 10% of V_{CD}.
6. Measured on secondary side of isolation transformer (see Connection Diagram, Figure 1). The transformer has a 1:1 turns ratio with an inductance between 30 and 100µH at 5MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS V_{EE} = –9V ±5%; T_A = 0 to 70°C, unless otherwise specified[1]. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{RON}	Receiver start up delay RXI to $RX_{\pm}$ (Figure 3) First received bit on $RX_{\pm}$	V_{RXI} = –2V peak			5	bits
	First validly timed bit on $RX_{\pm}$				t_{RON} +2	bits
t_{RD}	Receiver prop. delay RXI to $RX_{\pm}$	V_{RXI} = –2V peak		35	50	ns
t_{RR}	Differential output rise time on $RX_{\pm}$ and $CD_{\pm}$[2,3]			5		ns
t_{RF}	Differential output fall time on $RX_{\pm}$ and $CD_{\pm}$[2,3]			5		ns
t_{OS}	Differential output settling time on $RX_{\pm}$ and $CD_{\pm}$ to V_{OB} = 40mV[2] (see Figure 5)			1		µs
t_{RJ}	Receiver and cable total jitter			±3		ns
t_{RHI}	Receiver high to idle time	Measured to +210mV	150		850	ns
t_{RM}	Rise and fall time matching on $RX_{\pm}$ and $CD_{\pm}$	$t_{RF} - t_{RR}$		0.4		ns
t_{TST}	Transmitter start–up delay $TX_{\pm}$ to TXO (Figure 4)	$V_{TX\pm}$ = –1V peak				
	First transmitted bit on TXO			1	2	bits
	First validly timed bit				t_{TST} + 2	bits
t_{TD}	Transmitter prop delay $TX_{\pm}$ to TXO (see Figure 4)	$V_{TX\pm}$ = 1V peak		35	50	ns
t_{TR}	Transmitter rise time 10% to 90% (see Figure 4)			25		ns
t_{TF}	Transmitter fall time 10% to 90% (see Figure 4)			25		ns
t_{TM}	$t_{TF} - t_{TR}$ mismatch			±2		ns
t_{TS}	Transmitter added skew[4]			±2		ns
t_{TON}	Transmitter turn on pulse width (see Figure 4)	$V_{TX\pm}$ = 1V peak	10		40	ns
t_{TOFF}	Transmitter turn off pulse width (see Figure 4)	$V_{TX\pm}$ = 1V peak	150	250	340	ns
t_{CON}	Collision turn on delay (see Figure 6)	0V to –2V step at RXI			13	bits
t_{COFF}	Collision turn off delay (see Figure 6)	–2V to 0V step at RXI			16	bits
t_{CHI}	Collision high to idle time (see Figure 6)	Measured to +210mV	150		850	ns
f_{CD}	Collision frequency (see Figure 6)		8.0	10	12.5	MHz
t_{CP}	Collision signal pulse width (see Figure 6)		35		70	ns
t_{HON}	Heartbeat turn on delay (see Figure 7)		0.6		1.6	µs
t_{HW}	Heartbeat test duration (see Figure 7)		0.5		1.5	µs
t_{JA}	Jabber activation delay measured from $TX_{\pm}$ to $CD_{\pm}$ (see Figure 8)		20		60	ms
t_{JR}	Jabber reset delay measured from $TX_{\pm}$ to $CD_{\pm}$ (see Figure 8)		250		750	ms

NOTES:
1. All typicals are for V_{EE} = –9V and T_A = 27°C.
2. Measured on secondary side of isolation transformer (see Figure 1, Connection Diagram). The transformer has a 1:1 turn ratio with an inductance between 30 and 100µH at 5MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from –225mV to +225mV, or +225mV to –225mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

FUNCTIONAL DESCRIPTION

The NE8392A contains four main functional blocks (see Block Diagram). These are:

a. The receiver which takes data from the coaxial cable and sends it to the DTE.

b. The transmitter which receives data from the DTE and sends it onto the coaxial cable.

c. The collision detection and heartbeat generation circuitry which indicates to the DTE any collision on the coaxial cable and tests for collision circuitry functionality at the end of every transmission.

d. The jabber timer which disables the transmitter in the event of a longer than legal length data packet.

Receiver Functions

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter is lower than the DC squelch threshold. For normal signal levels this will take less than 500ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250ns and only enables the receiver again after approximately 1µs. Figures 3 and 5 illustrate receiver timing.

The differential line driver provides typically ±900mV signals to the DTE with less than 7ns rise and fall times. When in idle state (no received signal) its outputs provide <20mV differential voltage offset to minimize DC standing current in the isolation transformer. The line driver outputs are emitter followers and, for Ethernet applications where they drive a 78Ω transmission line, require a 500Ω pull-down resistor to V_{EE}. For Thin Ethernet applications where the AUI cable is not used, the pull-down resistor can be increased to 1.5kΩ to save power consumption.

Transmitter Functions

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25ns (±5ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the NE8392A meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled by negative-going differential signals of typically greater than 225mV in magnitude and 15ns in duration. The transmitter will be disabled at the end of a packet if there are no negative going signals of greater than 225mV for more than typically 250ns. Figure 4 illustrates transmitter timing.

Collision Functions

The collision detection scheme implemented in the NE8392A is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and non-repeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10MHz oscillation signal at the CD outputs and typically occurs within 700ns of the onset of the collision. The collision signal begins with a negative-going pulse and ends with a continuous high-to-idle state longer than 170ns. Figure 6 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. This pseudo collision consists of a 1µs burst of 10MHz oscillation at the line driver outputs approximately 1µs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to V_{EE}. This allows the CTI to be used in repeater applications. Figure 7 illustrates heartbeat timing.

As with the receiver outputs, the collision outputs also require a pull down resistor to V_{EE} and maintain <20mV differential voltage offset in the idle state to minimize DC standing current in the isolation transformers.

Jabber Functions

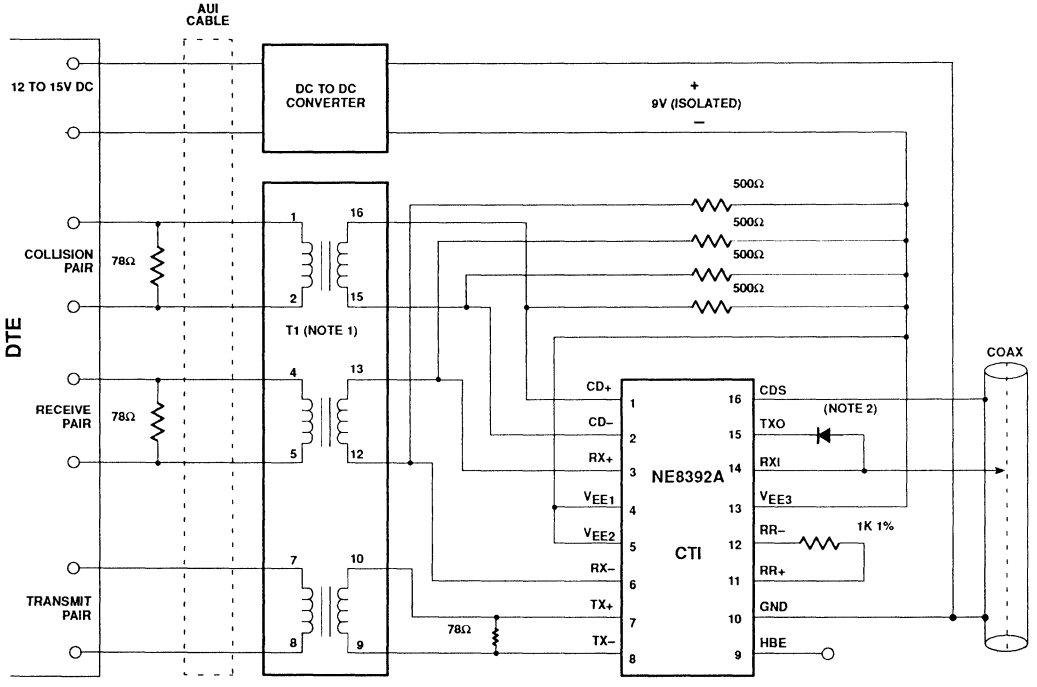
The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 6 illustrates jabber timing.

Detection of Coaxial Cable Faults

In the NE8392A there is no internal loopback path from the TX inputs to the RX outputs. This means that, when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX– if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs. An intelligent DTE can, therefore, detect this fault. If the fault is an open circuit, then a continuous collision signal will be sent to the DTE, provided the average DC voltage at the RXI pin is greater than the typical collision threshold of –1.53V.

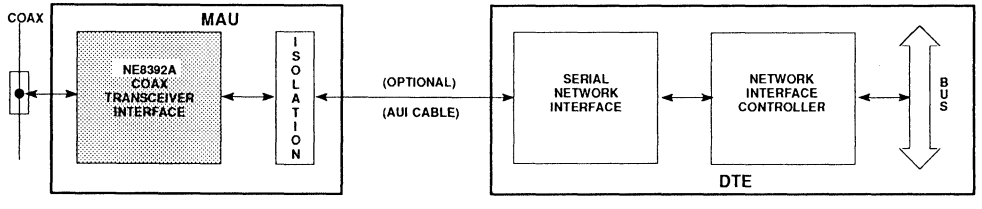
If a short or open circuit occurs elsewhere on the coaxial cable, the resulting reflections can result in an impedance at the CTI of any value between a short circuit and 50Ω, depending on the distance of the CTI from the fault. The upper limit of 50Ω results from the fact that the coaxial cable is terminated in 50Ω at both ends. Faults on the cable itself are, therefore, not guaranteed to be detected by simply monitoring the RX and CD pins when in the transmit mode, and more sophisticated schemes may be necessary.

Coaxial transceiver interface for Ethernet/Thin Ethernet NE8392A



NOTES:
1. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.
2. IN916 or equivalent for Ethernet, not required for Thin Ethernet.

Figure 1. Connection Diagram



MAU = Medium Attachment Unit
AUI Cable = Attachment Unit Interface Cable (not used in Thin Ethernet applications)

Figure 2. Interface Diagram for Ethernet/Thin Ethernet Local Area Network

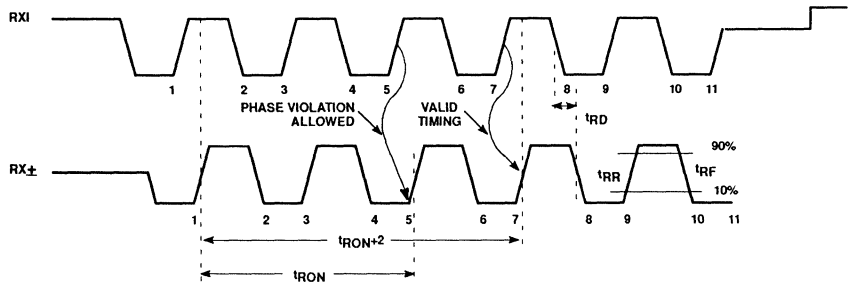


Figure 3. Receiver Timing

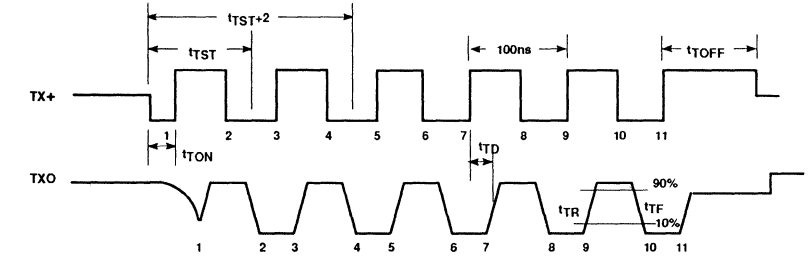


Figure 4. Transmitter Timing

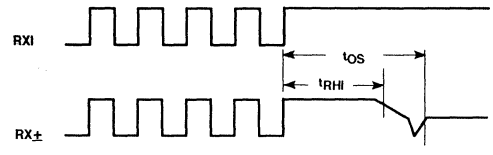


Figure 5. Receiver End-of-Packet Timing

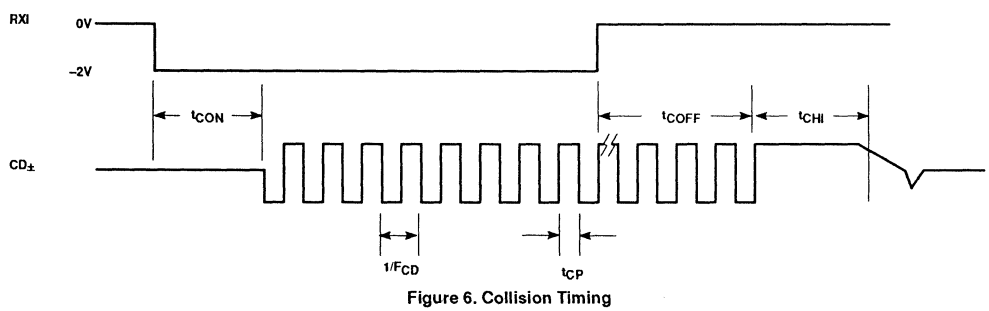


Figure 6. Collision Timing

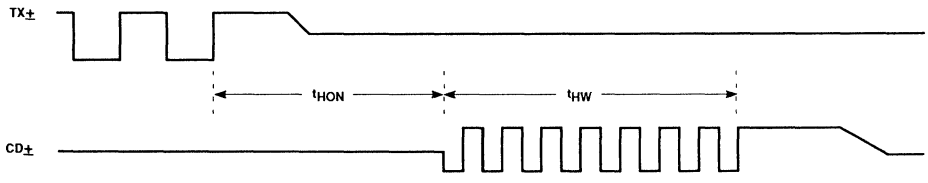


Figure 7. Heartbeat Timing

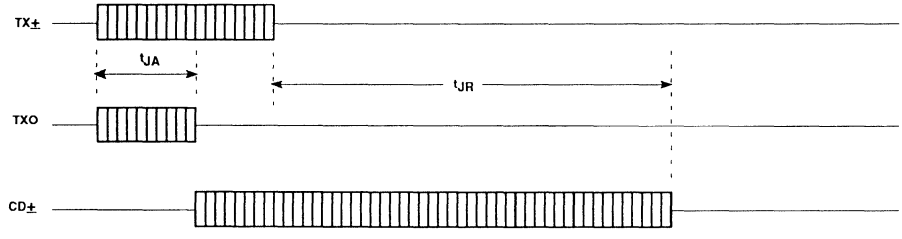


Figure 8. Jabber Timing

Philips Components-Signetics

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Date of Issue	July 23, 1990
Status	Product Specification
Data Communication Products	

NE86950

EtherStar™ Ethernet controller

DESCRIPTION

The NE86950 EtherStar™ is a highly integrated, local area network controller that supports both IEEE 802.3 CSMA/CD 10Mb/s Ethernet and 1Mb/s StarLAN™ protocols. Configurable for 8- or 16-bit wide bus interfaces, it links a host system bus to the local area network (LAN) transceiver or drivers in cost sensitive network applications such as personal computers, terminals, workstations, and other resource-sharing controllers with the minimum amount of controlling software and host system EtherStar interaction. Its design enables the controller to be connected directly on the main system bus without contention with the host CPU for the bus. Also, there is no need for a dedicated local CPU to handle data transfers.

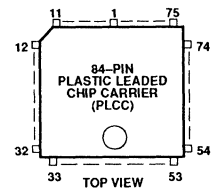
EtherStar is normally part of a three chip set that forms a complete Ethernet/Thin Ethernet interface for a Data Terminal Equipment. The EtherStar is the Network Interface Controller (NIC) and the other chips are a Serial Network Interface (SNI), such as the NE502A, and a Coaxial Transceiver Interface (CTI), such as the NE8392A. The SNI provides Manchester encoding and decoding while the CTI provides the physical attachment to the coaxial medium.

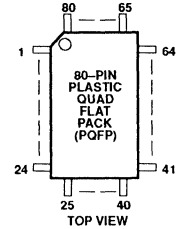
FEATURES

- IEEE802.3 CSMA/CD Ethernet/Thin Ethernet and StarLAN compatibility
- Configurable for 8-bit or 16-bit data path widths
- Unique buffer management architecture arbitrates all dedicated SRAM or DRAM memory data accesses and automatically allocates buffer memory area for incoming data frames
- Allows simultaneous transfer of data frames to/from host system and transmission/reception of data frames to/from LAN media
- Allows automatic retransmission of data packets during collisions, thus saving bus bandwidth
- Keeps track of all buffer memory area pointers internally in hardware to reduce software overhead
- Supports data transfers at up to 3.3 Mbytes or Mwords per second to the host system
- Addresses 8, 16, 32, or 64 Kbytes of dedicated SRAM or DRAM buffer memory. Dedicated buffer memory architecture allows data packet reception without using bus bandwidth
- Supports DMA transfers
- Available in 84-pin plastic J-bend PLCC or 80-pin plastic quad flat pack
- Dual metal, CMOS technology
- 25mA typical I_{CC} current

PIN CONFIGURATION

Packages





APPLICATIONS

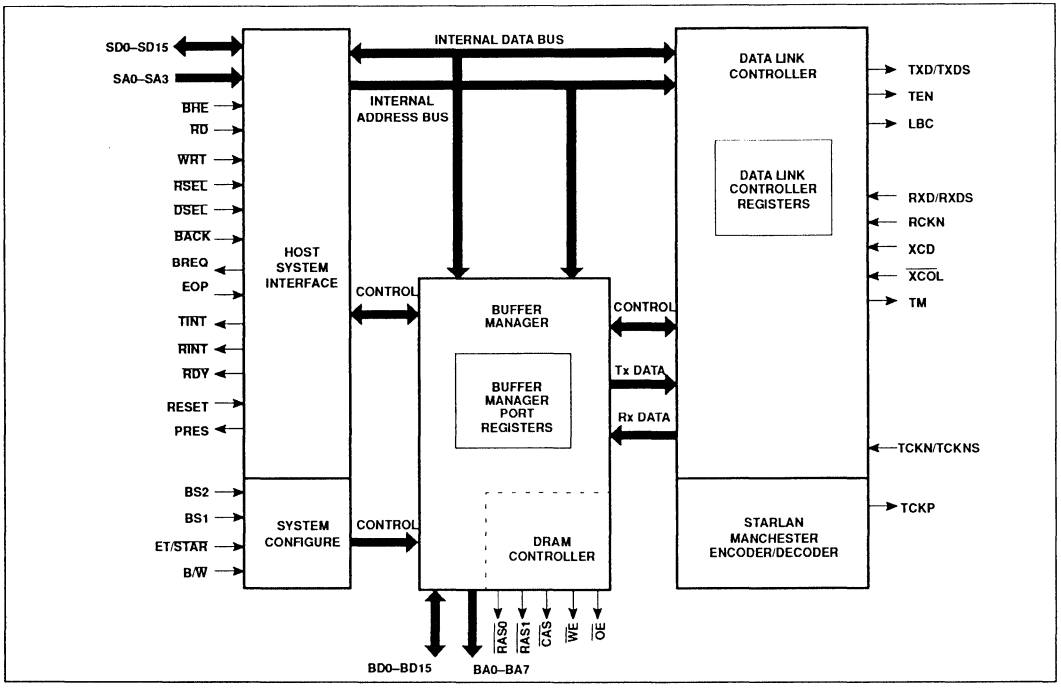
- Workstations
- Terminals
- File servers
- Print servers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
80-Pin Plastic Quad Flat Pack	0°C to +70°C	NE86950BB
84-Pin Plastic Leaded Chip Carrier	0°C to +70°C	NE86950BA

EtherStar™ Ethernet controller | NE86950

ETHERSTAR BLOCK DIAGRAM



PIN ASSIGNMENTS – PQFP

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	ET/STAR	15	RESET	29	EOP	43	SD10	57	BA3	71	BD8
2	B/W	16	SD7	30	SA3	44	SD11	58	BA4	72	PRES
3	BS0	17	SD6	31	SA2	45	SD12	59	BA5	73	V_{CC2}
4	BS1	18	SD5	32	TM	46	SD13	60	BA6	74	BD9
5	TEN	19	SD4	33	V_{CC1}	47	SD14	61	BA7	75	BD10
6	LBC	20	SD3	34	SA1	48	SD15	62	OE	76	BD11
7	XCD	21	SD2	35	SA0	49	WE	63	BD0	77	BD12
8	XCOL	22	SD1	36	BHE	50	RAS0	64	BD1	78	BD13
9	TXD/TXDS	23	SD0	37	RD	51	RAS1	65	BD2	79	BD14
10	TCKP	24	RDY	38	WRT	52	GND2	66	BD3	80	BD15
11	TCKN/TCKNS	25	TINT	39	BACK	53	CAS	67	BD4		
12	GND1	26	RINT	40	BREQ	54	BA0	68	BD5		
13	RCKN	27	RSEL	41	SD8	55	BA1	69	BD6		
14	RXD/RXDS	28	DSEL	42	SD9	56	BA2	70	BD7		

PIN ASSIGNMENTS – PLCC

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	GND1	15	$\overline{RINT}$	29	$\overline{BACK}$	43	GND3	57	BD3	71	BD14
2	RCKN	16	$\overline{RSEL}$	30	BREQ	44	$\overline{CAS}$	58	BD4	72	BD15
3	RXD/RXDS	17	$\overline{DSEL}$	31	SD8	45	BA0	59	BD5	73	ET/$\overline{STAR}$
4	RESET	18	EOP	32	SD9	46	BA1	60	BD6	74	B/$\overline{W}$
5	SD7	19	SA3	33	SD10	47	BA2	61	BD7	75	BS0
6	SD6	20	SA2	34	SD11	48	BA3	62	BD8	76	BS1
7	SD5	21	V_{CC1}	35	SD12	49	BA4	63	V_{CC2}	77	TEN
8	SD4	22	GND2	36	SD13	50	BA5	64	GND4	78	LBC
9	SD3	23	TM	37	SD14	51	BA6	65	PRES	79	XCD
10	SD2	24	SA1	38	SD15	52	BA7	66	BD9	80	$\overline{XCOL}$
11	SD1	25	SA0	39	$\overline{WE}$	53	$\overline{OE}$	67	BD10	81	TXD/TXDS
12	SD0	26	$\overline{BHE}$	40	$\overline{RAS0}$	54	BD0	68	BD11	82	TCKP
13	$\overline{RDY}$	27	$\overline{RD}$	41	$\overline{RAS1}$	55	BD1	69	BD12	83	TCKN/TCKNS
14	$\overline{TINT}$	28	$\overline{WRT}$	42	NC	56	BD2	70	BD13	84	NC

PIN DESCRIPTIONS

PIN NO.		SYMBOL	TYPE	DESCRIPTION
PLCC	PQFP			
Device Configuration Pins				
73	1	ET/$\overline{STAR}$	I	**NETWORK CONFIGURATION:** configures EtherStar for Ethernet (ET/$\overline{STAR}$ = 1) or StarLAN (ET/$\overline{STAR}$ = 0)
74	2	B/$\overline{W}$	I	**BYTE/WORD SELECT:** B/$\overline{W}$ = 1 configures EtherStar for an -bit data bus, B/$\overline{W}$ = 0 configures EtherStar to a 16-bit data bus.
75, 76	3, 4	BS1, BS0	I	**BUFFER SIZE SELECT LINES:** These inputs, together with B/$\overline{W}$, determine the size of the buffer memory supported by EtherStar. For word transfers, $\overline{BHE}$ should be asserted. Refer to the $\overline{BHE}$ signal description for more details.
Network Interface Pins				
77	5	TEN	O	**TRANSMIT ENABLE:** This pin becomes active when the first bit of the outgoing packet is valid and is held stable during transmission of data from the TXD/TXDS pin. This pin goes low after the last bit of the packet is clocked out. The TEN pin interfaces directly with the TEN pin of the Ethernet encoder/decoder, such as Signetics NE502A, in Ethernet configuration only.
78	6	LBC	O	**LOOPBACK CONTROL:** When LBC = 1, indicates that EtherStar is in the loopback mode. In Ethernet configurations, this pin connects to LBC on the encoder/decoder, and instructs it not to send data to the Ethernet medium but to send the original data packet back to EtherStar for validation. In StarLAN configurations, this also occurs but loopback occurs on-chip.
79	7	XCD	I	**CARRIER DETECT:** This signal is provided by the encoder/decoder. It indicates the presence of a carrier on the network media.
80	8	$\overline{XCOL}$	I	**COLLISION DETECT:** This active low input indicates that a collision has been detected on the network media. Signal is provided by the encoder/decoder for Ethernet configurations or as an optional pin for StarLAN configurations.
81	9	TXD/TXDS	O	**TRANSMIT DATA (Ethernet)/TRANSMIT DATA (StarLAN):** This pin is a dual function pin. In an Ethernet configuration, (ET/$\overline{STAR}$ = 1), TXD/TXDS is the serial data output to the encoder/decoder. In a StarLAN configuration (ET/$\overline{STAR}$ = 0), TXD/TXDS transmits Manchester encoded data to an RS-422 type transceiver.

BS1	BS0	B/$\overline{W}$ = 1	B/$\overline{W}$ = 0
0	0	8KB	4KW
0	1	16KB	8KW
1	0	32KB	16KW
1	1	64KB	32KW

PIN DESCRIPTIONS (Continued)

PIN NO. PLCC	PIN NO. PQFP	SYMBOL	TYPE	DESCRIPTION
Network Interface Pins (Continued)				
82	10	TCKP	O	**CRYSTAL OUTPUT**: This is the 10MHz output pin required if a crystal is used. It is available for StarLAN configurations only. The multiplexed pin TCKN/TCKNS is used as the OSCIN input in conjunction with the TCKP signal pin if a crystal is used.
83	11	TCKN/ TCKNS	I	**TRANSMIT CLOCK (Ethernet)/StarLAN CLOCK (StarLAN):** This pin is a dual function pin. In an Ethernet configuration, (ET/$\overline{\text{STAR}}$ = 1), TCKN/TCKNS is the input clock. Typically this clock is 10MHz and is generated by the external encoder/decoder. In a StarLAN configuration (ET/$\overline{\text{STAR}}$ = 0), TCKN/ TCKNS is a 10MHz clock required by the on-chip Manchester encoder/decoder.
2	13	RCKN	I	**RECEIVE DATA CLOCK:** This is the 10MHz synchronous receive data clock signal supplied by the encoder/decoder. Not used in StarLAN configurations.
3	14	RXD/ RXDS	I	**RECEIVE DATA (Ethernet)/RECEIVE DATA (StarLAN):** This pin is a dual function pin. In an Ethernet configuration, RXD/RXDS is the serial data input line from the external encoder/decoder. In a StarLAN configuration, RXD/RXDS is the input line that receives the asynchronous 1MHz Manchester encoded data from the LAN network.
System Interface Pins				
4	15	RESET	I	**HARDWARE RESET:** Active high. A minimum pulse of 2µs in duration is required. This pin resets EtherStar's internal pointers and registers to the appropriate state.
5-12 31–38	16-23 41-48	SD7-SD0 SD8-SD15	I/O	**SYSTEM DATA BUS:** All data, command and status transfers between the host system and EtherStar take place over this bidirectional, 3-state bus. The direction of the transfer is controlled by $\overline{\text{RD}}$ and $\overline{\text{WRT}}$. The type of transaction which is occuring is controlled by $\overline{\text{RSEL}}$, $\overline{\text{DSEL}}$, and $\overline{\text{BACK}}$. The portion of the data bus over which the transaction occurs is controlled by B/$\overline{\text{W}}$, $\overline{\text{BHE}}$, and SA0.
13	24	$\overline{\text{RDY}}$	O	**READY:** Active low. This output is asserted to indicate to the host system that EtherStar is ready to complete the requested read or write operation. It will also be asserted if the device is unable to respond to the request for a read or write within 2.4µs. In that case, EtherStar will also assert $\overline{\text{RINT}}$ and the bus read error status bit (DLCR2, bit 6) or $\overline{\text{TINT}}$ and the bus write error status bit (DLCR0, bit 0).
14	25	$\overline{\text{TINT}}$	O	**TRANSMIT INTERRUPT:** Active low. Indicates that EtherStar requires host system attention after successful transmission of a packet or if an error occurs during transmission. This interrupt is maskable and can be cleared by writing to DLCR1.
15	26	$\overline{\text{RINT}}$	O	**RECEIVE INTERRUPT:** Active low. Indicates that EtherStar requires host system attention after successful reception of a packet or during reception should any error conditions occur. This signal is maskable and can be cleared by writing to DLCR3.
16	27	$\overline{\text{RSEL}}$	I	**REGISTER SELECT:** Active low. Enables read/write operations between the 16 data link control registers (DLCR0-15) and the host system.
17	28	$\overline{\text{DSEL}}$	I	**DATA SELECT:** Active low. Enables read/write operation between the host system and EtherStar's buffer memory port (BMPR0) and buffer manager registers (BMPR2-4).
18	29	EOP	I	**END OF PROCESS:** Indicates that an entire packet has been transferred between the buffer memory and the host system. When the DMA controller asserts EOP, further assertions of EtherStar's bus request output, BREQ, will be discontinued.
19, 20 24, 25	30, 31 34, 35	SA3, SA2 SA1, SA0	I	**SYSTEM ADDRESS LINES:** Specifies which of the internal registers or ports of EtherStar is selected for read/write operations.
23	32	TM	O	**TEST MODE:** The signal on this pin is the complement of the value of the $\overline{\text{TM}}$ bit (DLCR4, bit 2). It is used to control external functions.
26	36	$\overline{\text{BHE}}$	I	**BYTE HIGH ENABLE:** Active low. This pin is the byte/word control line. It is used only when EtherStar is configured for a 16-bit data bus (B/$\overline{\text{W}}$ = 0). It allows word, upper byte only or lower byte only transfers. The address select pin SA0 is used with $\overline{\text{BHE}}$ for byte or word transfers as follows:

B/$\overline{\text{W}}$	$\overline{\text{BHE}}$	SA0	FUNCTION
0	0	0	Word transfer (BMPR0, BMPR2-3, 4 only).
0	0	1	Byte transfer on upper half of data bus (SD15-SD8)
0	1	0	Byte transfer on lower half of data bus (SD7-SD0)
0	1	1	Reserved
1	X	X	Byte (SD7-SD0)

PIN DESCRIPTIONS (Continued)

PIN NO.		SYMBOL	TYPE	DESCRIPTION
PLCC	PQFP			
System Interface Pins (Continued)				
27	37	$\overline{RD}$	I	**READ:** Active low input which specifies that the current transfer between EtherStar and the host system is a read from one of EtherStar's internal registers or its data port.
28	38	$\overline{WRT}$	I	**WRITE:** Active low input which specifies that the current transfer between EtherStar and the host system is a write to one of EtherStar's internal registers or its data port.
29	39	$\overline{BACK}$	I	**BUS ACKNOWLEDGE:** Active low. Indicates that the DMA controller is ready to transfer data between the host system and EtherStar's buffer memory.
30	40	BREQ	O	**BUS REQUEST:** Issued to the DMA controller to indicate that EtherStar has data available to be read in its receive buffer, or is ready to accept data into its transmit buffer.
65	72	PRES	O	**PACKET RESET:** This signal pin follows the RMT RST bit (DLCR2, bit 4) that indicates a complete special data packet with the data length field 0900H has been received. This is intended to be used as a hardware control function from other nodes in the network.
Buffer Memory Control Pins				
39	49	$\overline{WE}$	O	**WRITE ENABLE:** Active low. This output enables the DRAM memory buffer for write operations.
40 41	50 51	$\overline{RAS0}$, $\overline{RAS1}$	O	**ROW ADDRESS STROBE:** Active low. Outputs to the DRAM buffer memory.
44	53	$\overline{CAS}$	O	**COLUMN ADDRESS STROBE:** Active low. DRAM buffer memory column address strobe.
45-52	54-61	BA0-BA7	O	**BUFFER MEMORY ADDRESS:** These eight lines can address 64 Kbytes of DRAM buffer memory.
53	62	$\overline{OE}$	O	**OUTPUT ENABLE:** Active low. Used to enable the buffer memory during read operations.
54-62 66-72	63-71 74-80	BD0-BD8 BD9-BD15	I/O	**BUFFER MEMORY DATA:** Data lines between the DRAM buffer memory and EtherStar. This 3-state data bus is configurable for an 8-bit or 16-bit data size by the B/$\overline{W}$ input.
Device Power Pins				
1 22 43 64	12 52 -- --	GND1 GND2 GND3 GND4		**SYSTEM GROUND**
21 63	33 73	V_{CC1} V_{CC2}		**POWER SUPPLY:** A nominal +5VDC supply is required.

ABSOLUTE MAXIMUM RATINGS[1,4]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.3 to 6.0	V
V_{IN}	DC input voltage[2]	–0.3 to V_{CC} + 0.3	V
V_{OUT}	DC output voltage	–0.3 to V_{CC} + 0.3	V
T_{STG}	Storage temperature range	–40 to +150	°C
T_J	Maximum recommended junction temperature		°C
P_D	Power dissipation	500	mW
θ_{JA}	Thermal impedance A package B package		°C/W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is recommended that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
3. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
4. All voltage measurements are referenced to ground (GND). All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V. See Figure 13.

DC ELECTRICAL CHARACTERISTICS[1, 2] T_A = 0 to 70°C; V_{CC} = 5V ±5%, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Low level input voltage		0		0.8	V
V_{IH}	High level input voltage		2.2		V_{CC}	V
V_{OL}	Low level output voltage All except BREQ BREQ	 I_{OL} = 3.2mA I_{OL} = 12.8mA	 0 0		 0.4 0.4	 V V
V_{OH}	High level output voltage All except BREQ BREQ	 I_{OL} = –0.4mA I_{OL} = –10.0mA	 4.2 4.2		 V_{CC} V_{CC}	 V V
I_{LI}	Input leakage current	V_I = 0 or V_{CC}	–10		10	µA
I_{LZ}	Thre-state output leakage current	V_O = 0 or V_{CC}	–10		10	µA
I_{CC}[3]	Operating V_{CC} supply current	No output load; TCKN = 10MHz; RCKN = 10MHz		25	40	mA
I_{CCS}	Static V_{CC} supply current	All inputs static; V_I = 0 or V_{CC}			100	µA

NOTES:
1. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
2. All voltage measurements are referenced to ground (GND). All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V. See Figure 13.
3. Limited functional test patterns are performed during device testing for this parameter.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3] T_A = 0 to 70°C; V_{CC} = 5V ±5%, unless otherwise stated.

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ	Max	
t_{AVRL}	14, t1	Address, select control valid to read low	10			ns
t_{RHAI}	14, t2	Read high to address, select and control invalid	10			ns
t_{RLRL}	14, t3	Read low to $\overline{RDY}$ low[4]			35	ns
t_{RHRH}	14, t4	Read high to $\overline{RDY}$ high			35	ns
t_{RLDV}	14, t5	$\overline{RDY}$ low to data valid			22	ns
t_{RHDT}	14, t6	Read high to data three state	12		45	ns
t_{RDW}	14, t7	Read pulse width	35			ns
t_{AVWL}	15, t1	Address, select and control valid to write low	10			ns
t_{WHAI}	15, t2	Write high to address, select and control invalid	10			ns
t_{WRW}	15, t3	Write pulse width	35			ns
t_{DS}	15, t4	Write low to data valid			5	ns
t_{DH}	15, t5	Write high to data invalid	30			ns
t_{WLRL}	15, t6	Write low to $\overline{RDY}$ low[5]			35	ns
t_{WHRH}	15, t7	Write high to $\overline{RDY}$ high			35	ns
t_{WHBRH}	16, t1	Write high to bus request high	23		62	ns
t_{BALEH}	16, t2	Bus acknowledge low to end of process	10			ns
t_{EPW}	16, t3	End of process pulse width	20			ns
t_{ELBAH}	16, t4	End of process low to bus acknowledge high	10			ns
t_{BALBRL}	17, t1	Bus acknowledge low to bus request low			35	ns
t_{BAHBRH}	17, t2	Bus acknowledge high to bus request high[6]	8		50	ns
t_{BAWS}	17, t3	Bus acknowledge low to read/write low	10			ns
t_{BAWH}	17, t4	Read/write high to bus acknowledge high	10			ns
t_{RWLRL}	17, t5	Read/write low to $\overline{RDY}$ low			35	ns
t_{RWLRH}	17, t6	Read/write high to $\overline{RDY}$ high			35	ns
t_{LBCD}	18, t1	Loopback control delay	30		90	ns
t_{TMD}	18, t2	Test mode signal delay	30		80	ns
t_{INTD}	18, t3	Interrupt signal mask/clear delay	30		80	ns
t_{TEND}	18, t4	Transmit enable dealy[7]		2.3		µs
t_{CYC}	19	TCKN cycle		100		ns
t_{RC}	19	Random read/write cycle		300		ns
t_{RAC}	19	Access time from $\overline{RAS}$			150	ns
t_{CAC}	19	Access time from $\overline{CAS}$			100	ns
t_{OEA}	19	Access time from $\overline{OE}$			90	ns
t_{DBC}	19	Data hold before $\overline{CAS}$ high	–8			ns
t_{RP}	19	$\overline{RAS}$ precharge time	100			ns
t_{RAS}	19	$\overline{RAS}$ pulse width	165			ns
t_{CPN}	19	$\overline{CAS}$ precharge time	100			ns
t_{CAS}	19	$\overline{CAS}$ pulse width	160			ns
t_{ASR}	19	Row address setup time	45			ns
t_{RAH}	19	Row address hold time	23			ns
t_{ASC}	19	Column address setup time	11			ns
t_{CAH}	19	Column address hold time	166			ns
t_{WCS}	19	Write command setup time	50			ns
t_{WCH}	19	Write command hold time	108			ns

AC ELECTRICAL CHARACTERISTICS[1, 2, 3] (Continued)

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ	Max	
t_{WP}	19	Write command pulse width	185			ns
t_{DS}	19	Data to $\overline{CAS}$ setup time	55			ns
t_{DH}	19	Data from $\overline{CAS}$ hold time	120			ns
t_{OES}	19	$\overline{OE}$ to $\overline{RAS}$ inactive setup time	80			ns
t_{RCD}	19	$\overline{RAS}$ to $\overline{CAS}$ delay time	50		68	ns
t_{OEC}	19	$\overline{OE}$ to $\overline{CAS}$ high	6			ns
t_{CRS}	19	$\overline{CAS}$ to $\overline{RAS}$ setup time	55			ns
t_{RHC}	20, t15	Refresh cycle		15.5		µs
t_{RAS}	20, t16	$\overline{RAS}$ pulse width	165			ns
t_{ASR}	20, t17	Row address setup time	45			ns
t_{RAH}	20, t18	Row address hold time	150			ns
t_{TCL}	21-24, t1	Transmit clock low width	35	50		ns
t_{TCH}	21-24, t2	Transmit clock high width	35	50		ns
t_{TED}	21-24, t3	TCKN low to transmit enable			52	ns
t_{TDH}	21-24, t4	Transmit data hold	12			ns
t_{TEH}	21-24, t5	Transmit enable hold	13			ns
t_{TINT}	21-24, t6	Transmit interrupt to transmit enable low		1		TCKN cycles
t_{COLW}	21-24, t7	Collision detect width	20			ns
t_{COLS}	21-24, t8	Collision inactive spacing			200	ns
t_{COLL}	21-24, t9	Minimum collision length	520			ns
t_{JAM}	21-24, t10	Jam period[8]		32		TCKN cycles
t_{INTP}	21-24, t11p	Transmit interrupt when collision at preamble		5		TCKN cycles
t_{INTA}	21-24, t11a	Transmit interrupt when collision at data field		16		TCKN cycles
t_{CJ}	21-24, t12	Collision to first jam bit	4		12	TCKN cycles
t_{TDS}	21-24, t13	Transmit data setup	40			ns
t_{RCL}	25, t1	Receive clock low width	35	50		ns
t_{RCH}	25, t2	Receive clock high width	35	50		ns
t_{RDS}	25, t3	Receive data setup	10			ns
t_{RDH}	25, t4	Receive data hold	10			ns
t_{RCSS}	25, t5	Receive carrier sense setup	10			ns
t_{RCSH}	25, t6	Receive carrier sense hold	12		7	ns RCKN cycles
t_{RINTG}	25, t7	Last bit of good packet received to interrupt		40		RCKN cycles
t_{RINTE}	25, t8	Receive interrupt after bad packet		15		RCKN cycles
t_{TXS}	26, t1	Transmit width short	4.95		5.05	TCKN cycles
t_{TXL}	26, t2	Transmit width long	9.95		10.05	TCKN cycles
t_{RXS}	26, t3	Receive width short	4.1		5.9	TCKN cycles

AC ELECTRICAL CHARACTERISTICS[1, 2, 3] (Continued)

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ	Max	
t_{RXL}	26, t4	Receive width long	9.1		10.9	TCKN cycles
t_{CLTE}	26, t5	TCKN low to transmit enable			50	ns
t_{TAFM}	26, t6	TEN active to first bit Manchester code		10		TCKN cycles
t_{TWL}	26, t7	Transmit width length		10		TCKN cycles
t_{TILM}	26, t8	TEN inactive to last bit Manchester code		15		TCKN cycles

NOTES:
1. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
2. All voltage measurements are referenced to ground (GND). All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V. See Figure 13.
3. AC test condition: for bidirectional busses (SD0-SD15, BD0-BD15) C_L = 85pF, for all other outputs C_L = 60pF. See Figure 13.
4. When reading from the buffer memory port, BMPR0, a worst case time of 2.25µs may occur if the buffer manager is required to service simultaneous access requests from the system, the refresh controller, and the network (operating in loopback mode). The worst case time is 2.4µs if the system attempts to read an empty receive buffer memory. A BUS_RD_ERR will occur in the latter case.
5. When writing to the buffer memory port, BMPR0, a worst case time of 2.25µs may occur if the buffer manager is required to service simultaneous access requests from the system, the refresh controller, and the network (operating in loopback mode.) The worst case time is 2.4µs if the system attempts to write to a full transmit buffer memory. A BUS_WR_ERR will occur in the latter case.
6. A worst case time of 2.25µs may occur if the buffer manager is required to service simultaneous access requests from the system, the refresh controller, and the network (operating in loopback mode).
7. This timing assumes that the network is free.
8. The 32 jam bits include eight data bits and 24 '0' bits.

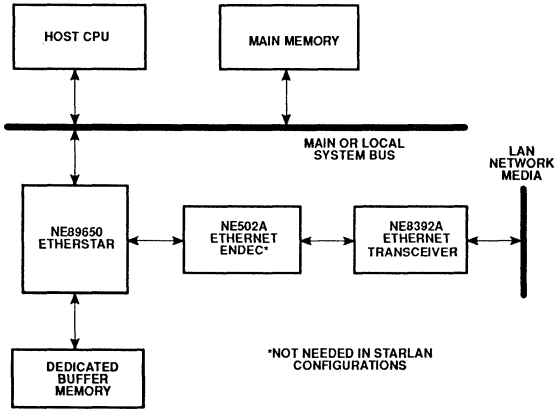


Figure 1. Typical System Configuration

GENERAL DESCRIPTION

The NE86950 EtherStar is a highly integrated, local area network controller that supports both IEEE 802.3 CSMA/CD 10Mb/s Ethernet and 1Mb/s StarLAN protocols. Configurable for 8- or 16-bit wide bus interfaces, it links a host system bus to the local area network (LAN) transceiver or drivers in cost sensitive network applications such as personal computers, terminals, workstations, and other resource-sharing controllers with the minimum amount of controlling software and host system-EtherStar interaction. Its design enables the controller to be connected directly on the main system bus without contention with the host CPU for the bus. Also, there is no need for a dedicated local CPU to handle data transfers.

EtherStar arbitrates access to a dedicated DRAM or SRAM buffer memory of up to 64 Kbytes in size. The transfer of data frames to/from the host system and the transmission/reception of data frames to/from the network media can occur simultaneously. EtherStar supports transfers to/from the system using programmed I/O or DMA. EtherStar integrates a data link controller (DLC), a 1Mb/s Manchester encoder/decoder, a dynamic memory controller (DMC), and a buffer manager to arbitrate simultaneous access to the buffer memory by the host system CPU and the data frames from the LAN media. The DLC block provides for automatic generation and stripping of the 64-bit preamble, 32-bit CRC generation/checking, serial and parallel data conversions, automatic retransmission, contention resolution by binary exponential back-off, and address recognition for 10Mb/s Ethernet and 1Mb/s StarLAN supporting IEEE 802.3 CSMA/CD specifications.

SYSTEM CONFIGURATION

A typical system configuration for the NE86950 EtherStar is shown in Figure 1. On the host side, EtherStar interfaces to the system bus to obtain configuration information for its internal control registers, to provide receive and transmit status information from its internal status registers, to move data packets to be transmitted from the host memory to EtherStar's dedicated buffer memory, and to deliver received data packets from the dedicated buffer memory to the host system. The network side connection depends on the protocol mode of operation. For Ethernet mode, EtherStar connects to the LAN media via an external Manchester encoder/decoder (such as Signetics' NE502A) and an Ethernet transceiver (such as the Signetics NE8392A). In StarLAN mode, the encoding/decoding function is performed internally, and EtherStar attaches to the LAN media via appropriate RS-422 drivers and receivers.

BUFFER MEMORY

As described above, the NE86950 uses a dedicated buffer memory for intermediate storage of data frames to be transmitted and of data frames received from the network. The BS0 and BS1 input pins configure EtherStar to operate with 8, 16, 32 or 64 Kbytes of buffer. This memory is partitioned into two separate address spaces: the first four Kbytes are reserved for transmit buffers, while the remainder of the memory is used for a receive buffer (see Figure 2).

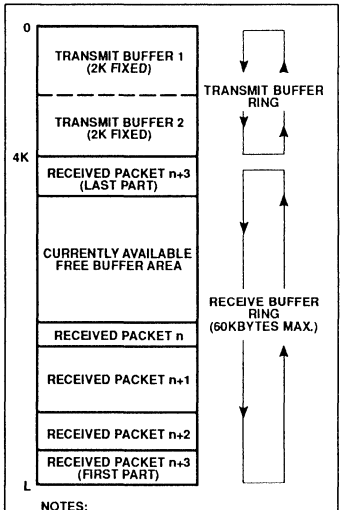


Figure 2. Buffer Memory Organization

EtherStar supports both programmed I/O and DMA transfers between the buffer memory and the host system. The host accesses the buffer memory by reading from or writing to EtherStar's buffer memory port register, designated BMPR0. The RDY signal synchronizes these transfers to accommodate other internal buffer access requests.

Access to the transmit and receive buffers is completely managed by EtherStar. As required, it updates its internal pointers to these buffers for the tasks of transmission, retransmission, reception, rejection of bad frames, and data transfers to and from the host. Thus, the host is relieved of these buffer management functions, making EtherStar extremely easy to operate and reducing firmware requirements substantially.

Transmit Buffer

The transmit buffer space is divided to form a ring structure of two transmit buffers, each two Kbytes in length. These function in a 'ping–pong' manner to permit one of the buffers to be loaded by the host while the contents of a previously loaded data frame are being transmitted to the network.

Internal pointers, managed by EtherStar, control which of the two buffers is selected for access by the host and which byte/word of that buffer is written to. At reset, the pointers are initialized to point to the beginning of one of the transmit buffers. Each time the host writes data to the buffer via BMPR0, an internal pointer is advanced to the next memory location within the transmit buffer. Once a data byte/word is written it cannot be read, and the internal pointer cannot be reversed. When the host has completed loading an outbound data packet into the buffer by successive writes to BMPR0, it initiates transmission of that data packet to the network by writing the length of the outbound packet to the packet length register within EtherStar. The internal pointers are then automatically set to point to the beginning of the second transmit buffer; that buffer is then available to be loaded with the next outbound packet. When the contents of the first data buffer are successfully transmitted, it again becomes available for use by the host.

Receive Buffer

Buffer memory from 4K through the end of memory is used for receiving packets from the network. This portion of the buffer is not partitioned into fixed length buffers, but is dynamically allocated as packets are received. Each received packet is preceded by a four byte header which provides packet status and the length of that data packet. All receive buffers are aligned on an eight byte boundary and are linked by internal pointers to form a ring structure.

A status bit in one of EtherStar's internal registers informs the host when one or more packets are resident in the receive buffer memory and available to be read. The host retrieves these packets from the buffer memory by successive reads of BMPR0.

Once a data byte/word is read from the buffer memory, internal pointers are advanced and that memory becomes available for reception of new packets.

If EtherStar detects a bad incoming packet (CRC error, etc.), it releases the buffer space in which that packet is contained and resets

its internal pointers so as to use that space for the next incoming packet. If an incoming packet requires more space than remains available in the buffer, that packet is automatically rejected.

NE86950 FUNCTIONAL DESCRIPTION

As illustrated in the block diagram, the NE86950 consists of five major functional blocks: system interface, buffer manager, DRAM controller, data link controller, and StarLAN encoder/decoder. The operation of these blocks is described below.

System Interface

The system interface block provides the connection between EtherStar and the host CPU. EtherStar supports both 8- and 16-bit bus architectures and byte or word transfers. It may be operated in I/O-mapped, memory mapped, or DMA modes. Two interrupt outputs, $\overline{TINT}$ and $\overline{RINT}$, are provided which may be programmed by the user to alert the host CPU of transmitter and receiver status conditions requiring host intervention.

Two sets of user accessible registers are contained within EtherStar: the data link control register set and the buffer memory port register set. Address decoding circuits within the system interface block select the appropriate register within the NE86950 for read and write transactions. All registers are accessible as bytes. Additionally, when the interface is configured for word mode ($B/\overline{W}$ = 0), the registers in the BMPR set can be accessed as bytes or as words.

Buffer Manager

The buffer manager automatically arbitrates, prioritizes and services requests for access to the buffer memory from the data link controller, the refresh timer within the DRAM controller, and the host system, in that order. It updates all buffer memory pointers, allocates memory space for incoming data packets, and controls pertinent bits within the status registers.

The arbitration mechanism interleaves the buffer memory accesses without loss of data, so that operation appears to be 'simultaneous': data can be written to or read from the buffer memory by the host via BMPR0 while data frames are retrieved for transmission and/or provided for storage by the data link controller. Thus, the buffer manager supports all the cases of 'simultaneous' access to the buffer memory, as conveyed in Figure 3 and as follows:

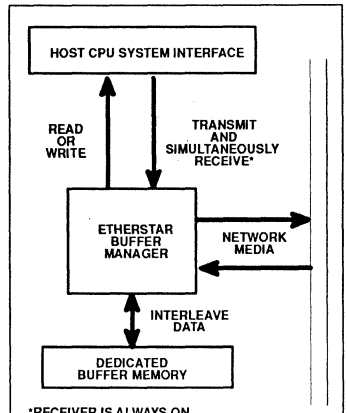


Figure 3. Simultaneous Operations Possible with EtherStar

1. The host can transfer a packet to a transmit buffer while data from the network is stored in a receive buffer.

2. The host can retrieve a packet from a receive buffer while data from a transmit buffer is obtained by the data link controller.

3. The data link controller can obtain data from a transmit buffer while the host loads the next packet into the second transmit buffer.

4. The data from the network is stored in a receive buffer while the host reads the data in another receive buffer.

5. The host retrieves a packet from a receive buffer while the network side stores data in a different receive buffer and obtains data from a transmit buffer (e.g., in loopback or broadcast address modes).

6. The host delivers a packet to a transmit buffer while the network side obtains data from the second transmit buffer and stores data in a receive buffer (e.g., in loopback or broadcast address modes).

DRAM Controller

The DRAM controller provides address multiplexing, timing and automatic refreshing for a DRAM dedicated buffer memory. In 8-bit bus mode ($B/\overline{W}$ = 1) EtherStar supports a memory of up to 64Kx8. In 16-bit bus mode ($B/\overline{W}$ = 0), a memory of up to 32Kx16 can be used.

Data Link Controller

The data link controller (DLC) fully implements the IEEE 802.3 CSMA/CD specification for 10Mb/s Ethernet and 1Mb/s StarLAN. It assembles data packets for transmission and disassembles received data packets. The DLC provides for automatic generation and stripping of the 64-bit preamble, 32- bit CRC generation and checking, contention resolution by binary exponential back-off, several modes of address recognition, and serial/parallel and parallel/serial conversions.

Receiver

The receiver includes a receive state machine, serial to parallel converter, preamble recognition circuitry, address comparison logic for the various modes of address recognition, CRC checker and a FIFO.

The receiver state machine provides sequencing of events for the receiver, including idle, address recognition, data, CRC check and hold. It detects various receive error conditions and sets appropriate bits within the DLC registers.

A six byte receive data FIFO provides a small elastic buffer for synchronization with the buffer manager timing, and to hold data in the event that the buffer manager is servicing another buffer memory access request.

All received bytes are delayed by four bytes so that the last four bytes of the packet can be trapped and checked for correct CRC. These CRC bytes are not transferred to the receive buffer.

During reception, packets are automatically rejected if space in the receive buffer is insufficient to hold the entire received frame or if certain error conditions are detected. Status bits in the receive status register are set to indicate these occurrences.

Transmitter

Circuits within the transmitter include a transmitter state machine, a FIFO, preamble generator, CRC generator, parallel to serial converter, back-off generator and a time domain reflectometer (TDR) counter.

The transmitter state machine provides sequencing of events for the transmitter, including idle, preamble, data, CRC, interframe gap, jam and back-off. It detects various transmit error conditions and sets appropriate bits within the DLC registers.

The two-byte FIFO provides a small amount of elastic buffering that the buffer manager can load with data to be transmitted. The CRC generator produces the standard Ethernet 32-bit CRC that is appended to the end of the packet data field.

A 17-bit pseudo-random number generator provides for the back-off function. This is clocked at the bit rate so that distances between stations become part of the

randomizing function. It is sampled at the time of collision and counted down at the slot-time rate (512 bits) defined in the Ethernet specification, which provides a binary exponential back-off from collisions.

The TDR function is provided by a 14-bit counter that counts the actual number of bits transmitted for each packet before a fault condition occurs. See DLCR7 and DLCR15 description for full details of operation.

If EtherStar detects a collision during transmission ($\overline{XCOL}$ input asserted in Ethernet mode, internal detection in StarLAN mode), it will automatically try to re-transmit the packet until sixteen attempts have been made. Status bits in the transmit status register are set in case of a collision and sixteen consecutive collisions.

Starlan Encoder/Decoder

This unit is operational when the NE86950 is set for StarLAN mode by tying the ET/$\overline{STAR}$ configuration pin LOW.

When transmitting data, the encoder section converts the 1Mb/s serial NRZ stream from the DLC to Manchester code and detects collisions. EtherStar monitors its receive input during transmission and assumes a collision has occurred if the received Manchester encoded data is not valid (i.e., anything but valid Manchester). However, this received data is not transferred to the data buffer unless the loopback mode has been enabled.

When receiving, a digital phase locked loop within the decoder section extracts a synchronized clock from the received data stream, while simultaneously converting the Manchester encoded data to NRZ form. The synchronized clock and data are then passed to the data link controller.

REGISTERS

The operation of the NE86950 is programmed prior to beginning operation by writing control words into appropriate registers within the device. Operational feedback is provided by status registers which can be read by the CPU. Certain bits in the control registers can also be manipulated during operation to change the device's operation, e.g., which status bits are enabled to cause interrupts. The user accessible registers within EtherStar are divided into two sets: the data link control register set and the buffer memory port register set. Table 1 defines the address decoding for these registers.

The data link control register set, consisting of the 16 registers DLCR0–DLCR15, contains transmit control and status registers, receive control and status registers, transmit and receive interrupt masks, and node ID registers. The registers within this set are byte aligned and byte accessible. The node ID registers (DLCR8–DLCR13) are protected; their contents can only be changed when the data link controller is disabled by setting the enable data link controller bit, DLCR6<7>, to a '1', or immediately after device reset.

The buffer memory port register set provides the host with the mechanism to access the transmit and receive buffers, as well as controlling DMA operation. This set contains the buffer memory port register (BMPR0), transmit packet length registers (BMPR2–BMPR3), and a DMA control register (BMPR4). These registers are word aligned and byte or word accessible. When the host reads from or writes to BMPR0, the $\overline{RDY}$ output synchronizes the data transfer, since there may be higher priority requests for access to the buffer memory pending from the data link controller and/or from the DRAM refresh controller. If the buffer manager cannot respond to the host's access request within 2.4µs, it sets an appropriate status bit (bus read error or bus write error) and then asserts $\overline{RDY}$ while simultaneously asserting the corresponding interrupt line ($\overline{RINT}$ or $\overline{TINT}$). This will not typically occur during normal operation, but only if the host attempts to read from an empty receive buffer or to write to a full transmit buffer.

In byte mode (B/$\overline{W}$ = 1), all registers are accessed as bytes. Note that when accessing the buffer memory in byte mode, successive bytes are read or written from BMPR0. When the interface is configured for word mode (B/$\overline{W}$ = 0), all transactions to the buffer memory port must be word transactions; successive words are read or written from BMPR0. The other registers in the BMPR set can be accessed as bytes or as words, depending on the state of the $\overline{BHE}$ and SA0 inputs, as described in the Pin Descriptions table.

Tables 2 and 3 provide an overview of the contents and functions of each register in the DLCR set and the BMPR set, respectively. Detailed descriptions of the registers are given in tables 4 and 5.

OPERATION

The operation of the NE86950 can be considered in four major operational phases: reset, initialization, packet transmission, and packet reception. Although described separately here, packet transmission and reception can be performed concurrently in actual operation. In the sections that follow, interrupt-driven operation is assumed.

Reset

A reset pulse with a minimum duration of 2µs is applied to the RESET input after power on, or at any other time, to reset the internal pointers and other logic within the NE86950. Reset disables the data link controller (effectively setting DLCR6<7> to a '1'), sets DLCR5<6>, BUF_EMP, to a '1', and clears the following bits:

DLCR0	5, 6, 7
DLCR1	0, 4, 6
DLCR2	4, 7
DLCR3	5, 6
DLCR5	5
BMPR4	0, 1, 2, 3

The state of all other bits within the registers after reset is indeterminate.

Initialization

Initialization is performed by software to place EtherStar into a known functional state. This includes setting the transmit and receive interrupt conditions, transmission and reception modes, and the node address that EtherStar responds to. A flow chart of the initialization process is shown in Figure 4.

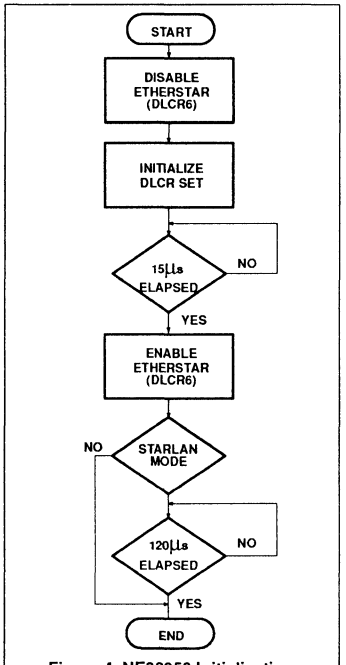


Figure 4. NE86950 Initialization

Before any initialization begins, EtherStar should be disabled by writing a value of H'80' to DLCR6. This disables the data link controller and enables access to the node ID

registers (DLCR8 through DLCR13). The DLCR register set is then initialized, in any order, based on the communication requirements. The basic programming is as follows:

DLCR0-Transmit Status: A value of H'0F' is written to clear all transmit errors.

DLCR1-Transmit Interrupt Masks: The transmit interrupts are disabled by writing a value of H'00' at initialization. Desired interrupts should be enabled prior to a packet transmission.

DLCR2-Receive Status: The value H'CF' is written to clear all receive errors.

DLCR3-Receive Interrupt Masks: Required receive interrupts are enabled by writing the appropriate value. These may be changed during operation, based on reception criteria.

DLCR4-Transmit Mode: Normally, a value of H'02' is written to disable chip test, test mode and loopback, and to enable carrier detect.

DLCR5-Receive Mode: A value is written per system requirements to enable/disable CRC testing, set the address size, enable/disable short packet reception, enable/disable remote reset packet reception, and to set the address recognition mode.

DLCR8 to DLCR13-Node ID Registers: The six byte address programmed into these registers must be unique. It is used in conjunction with the address match mode bits (DLCR5<1:0>) for packet reception.

If this initialization is part of an error recovery procedure, BMPR0 should be read twice to assure that certain internal pipeline registers are cleared. If a BUS_RD_ERR results from these read operations, it should be ignored.

When this initialization is completed, the data link controller is enabled by writing H'00' to DLCR6. A delay of 15µs, the time needed by EtherStar to complete internal initialization, must be guaranteed between the trailing edge of reset and clearing of DLCR6. In StarLAN mode only, an additional delay of 120µs after the DLC is enabled is required before EtherStar is ready to begin transmit or receive operations.

Packet Transmission

An outbound packet is transmitted in two phases. In phase one, the packet is transferred from host memory to a transmit buffer in EtherStar and the transmission is initiated. In phase two, a transmit interrupt is used to report successful transmission or a transmit error condition.

Transmit Initiation

The first phase is illustrated in Figure 5. To transmit a packet, the host loads the outbound packet into a transmit buffer, initiates transmission, waits for EtherStar to clear the TMT_OK bit, sets a transmit pending flag, and sets the transmit interrupt masks.

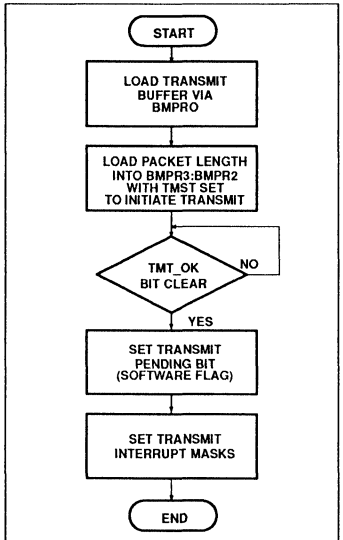


Figure 5. Transmit Initiation

A transmit packet, Figure 6, contains a six byte Destination Address, a six byte Source Address, a two byte Data Length, and data. EtherStar is capable of transmitting packets with a total packet length of six to 2,048 bytes, depending on the configuration set at initialization. (Software conforming to the IEEE 802.3 specification must guarantee that the total packet length is in the range of 64 to 1,518 bytes including the four-byte CRC, which is calculated by EtherStar and appended to the packet when it is transmitted.)

The packet is loaded into a transmit buffer using the buffer memory port register (BMPR0). At initialization or the initiation of a transmission, EtherStar's internal pointers are advanced to the beginning of the next available transmit buffer. The packet is transferred from the host to a transmit buffer by successive writes of data, starting at the beginning of the packet, to BMPR0. The internal pointers manage the placement of the data into the current transmit buffer. When the entire packet has been loaded, EtherStar is requested to send the packet by writing the total length of the transmit packet

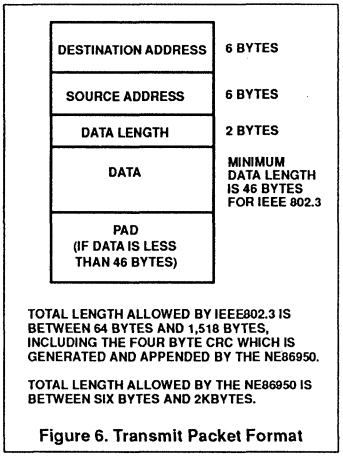


Figure 6. Transmit Packet Format

(with the TMST bit set) to the packet length register (BMPR3:BMPR2). Note that the packet length value is in bytes regardless of whether the NE86950 is configured in word mode or in byte mode. If operating in word mode, and the packet length is an odd value, the MS byte of the last word sent to the buffer will not be transmitted.

When the network is free and EtherStar actually begins transmitting the packet to the LAN, it will clear the TMT_OK bit. The TMT_OK_MSK bit must not be set until TMT_OK is cleared to prevent an erroneous transmit interrupt from being generated. The host can load the next packet into the second transmit buffer immediately after it sets TMST for the previous packet, but the TMST bit cannot be set for that second packet until the first packet has been successfully transmitted to the LAN.

When using a common interrupt service routine (ISR) to handle both transmit and receive interrupts, a transmit pending flag is required within the driver to distinguish whether TMT_OK was set to indicate the completion of a pending transmission or is the residue of a previous transmission, since the software does not have the ability to clear TMT_OK after completion of a pending transmission.

Once the transmit has been initiated and the TMT_OK bit is cleared by EtherStar, the transmit interrupt masks are set. Typically, a value of H'82' is written to the transmit masks register (DLCR1) to enable transmission interrupts based on transmit complete, and 16-collision error. The COL and underflow error interrupts may optionally be enabled.

Transmit Interrupt Routine
When a packet is successfully transmitted or a transmit error condition occurs which has its corresponding transmit interrupt mask set in DLCR1, a transmit interrupt ($\overline{TINT}$) is generated. A typical transmit interrupt service routine (ISR) to service this interrupt is shown in Figure 7.

On entering the ISR, the transmit interrupt masks are cleared by writing H'00' to DLCR1, to prevent nested interrupts. These masks may need to be saved and rewritten prior to exiting the ISR. If the transmit pending flag is set, the status of TMT_OK is checked. If it is set, the packet has been successfully transmitted; the routine clears the transmit pending flag and takes any other driver specific action. This may include signaling successful transmission to the upper layer network software and/or initiating another transmission.

The major error conditions which must be handled by the ISR are bus write error and 16-collision error. BUS_WRT_ERR is not the result of a transmission by the DLC, but indicates that an attempt was made to transfer data to a transmit buffer and the transmit buffer was full. The ISR clears the bit, increments a bus write error counter in the driver for diagnostic purposes, and performs any other driver specific recovery action. 16_COL indicates that sixteen collisions have occurred in the transmission of a single packet and that EtherStar has aborted attempting to transmit that packet. This error is handled by clearing the error bit, incrementing a 16-collision error counter in the driver for diagnostic purposes, and performing any driver specific recovery algorithms.

Note: If, after 16 collisions have occurred, the host wishes to attempt to transmit the same packet again, it must reload that packet into one of EtherStars' transmit buffers.

UDR_FLO will not occur during normal operation, but may be the result of some other error condition. This error is handled in a manner similar to 16_COL.

Setting of the collision error status bit, COL, indicates that at least one collision occurred in the transmission of a single packet. EtherStar will continue to re-transmit the packet up to sixteen times. Each time the packet fails to transmit due to collision, a collision counter in the transmit mode register (DLCR4<7:4>) is incremented. When the collision counter wraps around to 0, 16_COL is set and EtherStar will not retransmit. If COL is set and 16_COL is not set, the collision counter will contain the number of collisions encountered on that transmission. Recovery is accomplished by clearing the COL bit and incrementing a collision error counter if desired.

Prior to exiting the ISR, the transmit pending flag is checked to see if there is an outstanding transmission. If set, then the transmit interrupt masks, which were cleared on entering the ISR, must be written back to DLCR1 to interrupt when the transmission completes.

Packet Reception

Incoming packets are examined for a match in the destination address field of the Ethernet header. Reception is based on the address match mode bits and the ADD_SZE bit in the receive mode register (DLCR5) and the node ID (DLCR8 through DLCR13). When a packet matches the defined reception criteria, it is copied into a receive buffer and checked for overflow, CRC, alignment or short packet errors. If no errors are detected, PKT_RDY in the receive status register (DLCR2) is set and BUF_EMP in the receive mode register (DLCR5) is cleared if not already cleared. If an error is encountered, the packet is discarded, making the buffer memory occupied by that packet available for reception of another packet, and the appropriate error bits are set in DLCR2.

Addressing Modes
In addition to the normal single address match mode, where the incoming address is compared to the programmed node ID, the NE86950 supports three special receiver address match modes: promiscuous receive, multicast address, and multicast group address. These modes are enabled by setting the address match mode bits in the receive mode register appropriately, and may be changed by the driver at any time. It is also possible to set the transmit mode for loopback, so that transmitted packets are not sent the network, but are simply fed back into the receiver.

In promiscuous receive mode, all good incoming packets on the LAN are received into buffer memory. No matching is done on the destination address field of the packet. This can be useful for network monitoring applications and debugging.

A multicast address is identified by a value of '1' in the least significant bit of the destination address. Using multicast address mode will cause all packets having a multicast address to be received. Note that in this mode EtherStar does not provide any hashing on the multicast address and simply receives all multicast packets.

When multicast group address mode is set, packets will be received if the three least significant bytes of the address match the address in the node ID registers and the least significant bit of the destination address is '1'.

Receive Packet Structure
When a packet is successfully stored in the receive buffer memory, EtherStar attaches a four byte header in the front of the packet. The first byte is a copy of the receive status register (DLCR2) in which bit 5 is set and the PKT_RDY bit is invalid. The second byte is reserved. The third and fourth bytes contain the LS and MS bytes of the length of the packet, respectively. Note that the packet length value is in bytes regardless of whether EtherStar is configured in word mode or in byte mode.

Receive Interrupt Routine
A receive interrupt ($\overline{RINT}$) is generated when a packet is successfully stored in the receive buffer memory or a receive error condition occurs which has its corresponding interrupt mask set in DLCR3. A typical receive interrupt service routine (ISR) to service this interrupt is shown in Figure 8.

On entering the ISR, the receive interrupt masks are cleared by writing H'00' to DLCR3, to prevent nested interrupts. These masks may need to be saved and rewritten prior to exiting the ISR. If BUF_EMP is cleared, there is at least one valid packet in the receive buffer memory, and the ISR proceeds to transfer that packet to the host. First, PKT_RDY is cleared. Then, the receive status byte and reserved bytes are read from the buffer memory via BMPR0. (In this model, these bytes are unused, but must be read to advance internal pointers used to control the extraction of received packets.) The packet length is then extracted to determine the size of the actual received packet, and that packet is copied to host memory by successive reads of BMPR0. The ISR then checks BUF_EMP again to see if additional packets remain in the receive buffer memory and, if so, the steps described above are repeated until all available packets have been copied to the host.

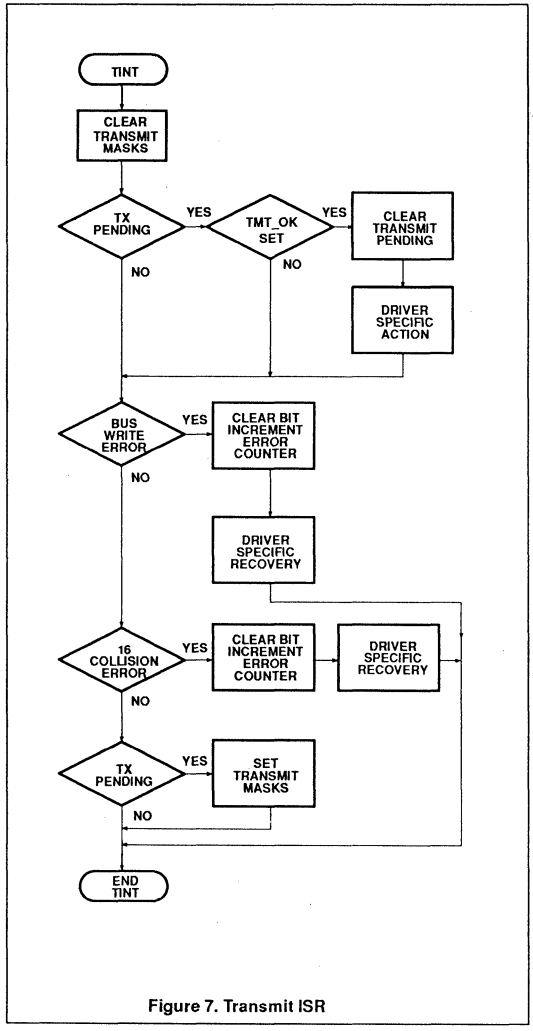


Figure 7. Transmit ISR

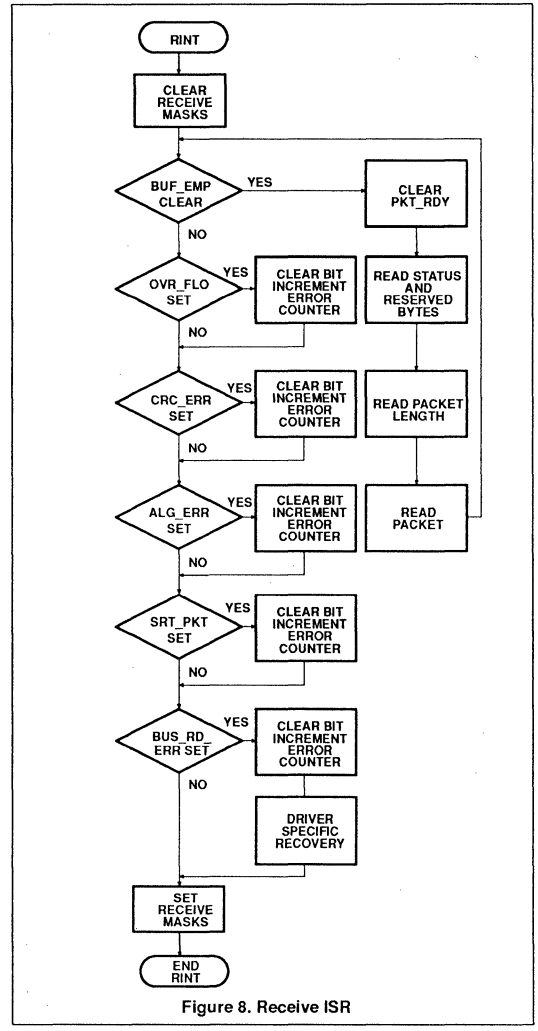


Figure 8. Receive ISR

Note: Reading more than the specified number of bytes extracts a portion of the next receive packet or causes a BUS_RD_ERR. Reading less than the specified number of bytes leaves garbage at the beginning of the next receive packet. These conditions can generate a fatal error condition.

Note: If operating in word mode, and the indicated packet length is an odd value, an extra byte of invalid data will be read out of the buffer on the last word read and should be ignored. There is no danger of reading the first byte of the next packet in this case because the packets in the buffer memory are aligned to start on an eight byte/four word boundary.

Note: When a packet has been completely read out of the buffer, EtherStar will re–assert PKT_RDY if any packets remain in the receive buffer. This feature can be used to cause an interrupt to be generated for each valid packet received and stored in the buffer.

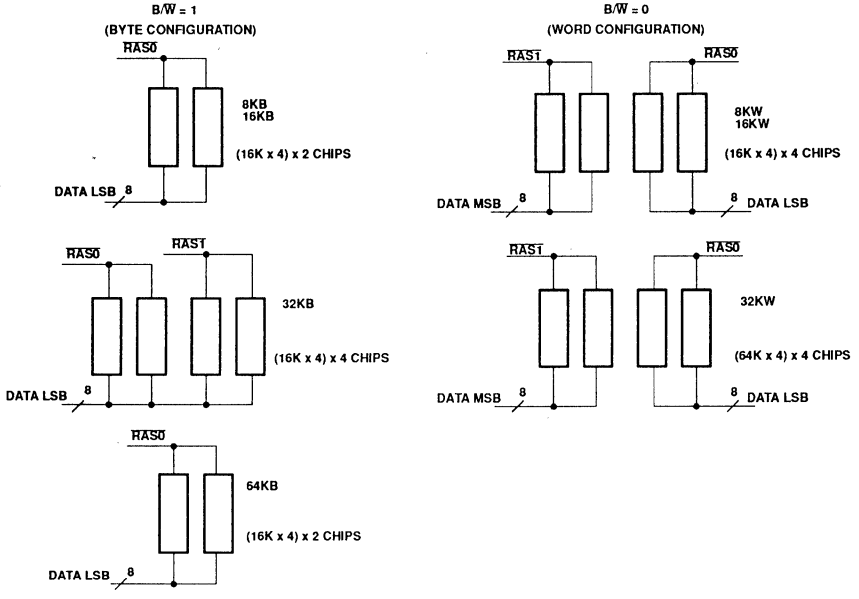


Figure 9. Buffer Memory Implementation with DRAM

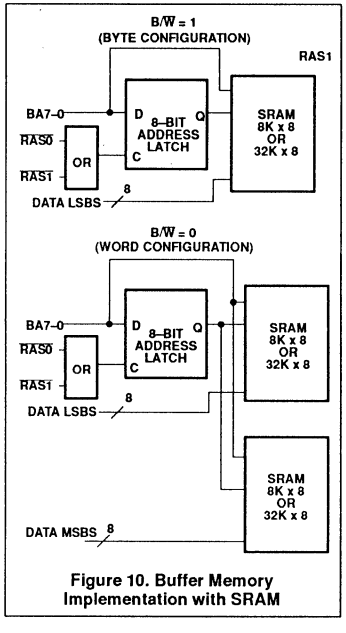


Figure 10. Buffer Memory Implementation with SRAM

The receive error conditions which can be programmed to cause an interrupt are bus read error, overflow, CRC error, alignment error, and short packet. All except the first do not require host intervention other than tallying the error for diagnostic purposes; EtherStar will automatically reject any packet in which any of these error conditions is detected.

BUS_RD_ERR indicates that an attempt was made to transfer data from a receive buffer to the host when the receive buffers are empty. This should be considered a fatal error, where the hardware or software is faulty. To recover, the ISR clears the BUS_RD_ERR bit, increments a bus read error counter, and performs any other driver specific recovery routine.

OVR_FLO denotes that an incoming packet from the LAN media was rejected because it was longer than the amount of free memory available in the receive buffer area. CRC_ERR indicates that the incoming packet's CRC did not match that calculated by EtherStar. ALG_ERR signifies that the incoming packet has a bad CRC at the last octet boundary and the number of bits were not divisible by eight. SRT_PKT indicates that the incoming packet does not meet the minimum length requirement of 60 bytes, or if the ENA_SRT_PKT bit in DLCR5 is set, six bytes. For these errors, the sample ISR takes no action other than clearing the error condition and incrementing a corresponding error counter.

Prior to exiting the ISR, the receive interrupt masks are restored to enable future receive interrupts.

DMA OPERATION

The NE86950 supports DMA operation for transfers of data between the host system and the dedicated buffer memory. The BREQ and $\overline{BACK}$ signals are used for handshaking between the external DMA controller and EtherStar.

DMA Write (Transmit)

TENA, BMPR4<0>, is set to a '1' to enable DMA write operation for transfers of data packets from the host memory to EtherStar's transmit data buffer. When it is ready to begin to accept data from the host, EtherStar will assert its Bus Request output, BREQ. The host responds by asserting $\overline{BACK}$ followed by $\overline{WRT}$ and placing the data on the data bus. EtherStar will negate BREQ and will assert its $\overline{RDY}$ output when it is ready to complete the current data transfer cycle. When the host negates $\overline{BACK}$ and $\overline{WRT}$, EtherStar accepts that data byte/word, moves its internal pointer to point to the next

byte/word, and then re-asserts BREQ to repeat the process. The DMA controller must assert the End of Process input, EOP, concurrent with the last byte/word data transfer to indicate that the entire packet has been transferred. EtherStar will then discontinue making further data requests.

To cause the packet to be transmitted, the host must load its packet length into BMPR3:BMPR2, asserting the TMST bit when the MS byte is loaded into BMPR3. TENA must be cleared when the packet transfer is completed, and set again when the host desires to begin loading another packet into the transmit buffer using DMA.

When EOP is asserted by the external DMA controller, the EOP status bit, BMPR4<2>, will be set to a '1' and will cause $\overline{RINT}$ to be asserted if BMPR4<3>, EOP_INT_MSK, is set. This interrupt can be used by the host to initiate the actions described in the paragraph above. The interrupt is cleared by writing to BMPR4 with bit 2 set, which can be done at the same time as TENA is cleared.

DMA Read (Receive)

Prior to beginning the transfer of a data packet from EtherStar's receive buffer memory to the host memory via DMA, the host must read the four-byte packet header to determine the number of bytes/words in the packet and should load that number into the counter in the external DMA controller. RENA, BMPR4<1>, is then set to a '1' to enable DMA read operation to transfer the actual packet to the host memory. When it is ready to begin, EtherStar will assert its Bus Request output, BREQ. The host responds by asserting $\overline{BACK}$ followed by $\overline{RD}$. EtherStar will negate BREQ and will assert its $\overline{RDY}$ output when it has placed the byte/word on the data bus and is ready to complete the data transfer cycle. When the host negates $\overline{BACK}$ and $\overline{RD}$, EtherStar moves its internal pointer to point to the next byte/word, and then re-asserts BREQ to repeat the process. The DMA controller must assert the End of Process input, EOP, concurrent with the last byte/ word data transfer to indicate that the entire packet has been transferred. EtherStar will then discontinue making further data requests. RENA must be cleared when the packet transfer is completed, and set again when the host desires to begin reading another packet from the receive buffer using DMA.

When EOP is asserted by the external DMA controller, the EOP status bit, BMPR4<2>, will be set to a '1' and will cause $\overline{RINT}$ to be asserted if BMPR4<3>, EOP_INT_MSK, is set. This interrupt can be used by the host to clear RENA. The interrupt is cleared by writing to BMPR4 with bit 2 set, which can be done at the same time as RENA is cleared.

BUFFER MEMORY IMPLEMENTATION

EtherStar is configured via the BS0 and BS1 inputs to support buffer memory sizes of 8, 16, 32 or 64 Kbytes. Figures 9 and 10 illustrate the typical implementation of the buffer memory for these options in both byte and word modes using industry standard DRAMs and SRAMs, respectively. Table 6 describes the relationship between the internal address lines A15:A0 and the multiplexed buffer addresses BA7:BA0.

Although not necessary for operational purposes, it is useful for debugging and diagnostic purposes to describe how the network side and the system side access the buffer.

Network Access

The network side always transfers a byte at a time to or from the buffer.

In word mode (B/$\overline{W}$ = 0), $\overline{RAS0}$ is asserted for each LS byte transferred to or from the buffer and $\overline{RAS1}$ is asserted for each MS byte transferred to or from the buffer.

In byte mode (B/$\overline{W}$ = 1), for 8, 16 or 64 Kbyte configurations, $\overline{RAS0}$ is asserted for every byte transferred to or from the buffer. For 32 Kbyte configuration, $\overline{RAS0}$ is asserted during even byte transfers (A0 = 0), while $\overline{RAS1}$ is asserted during odd byte transfers (A0 = 1).

System Access

The system side transfers either a byte at a time or a word at a time to or from the buffer, depending on the mode selected.

In word mode (B/$\overline{W}$ = 0, both $\overline{RAS0}$ and $\overline{RAS1}$ are asserted for each word transferred to or from the buffer. It is not possible to address the bytes separately for this mode.

In byte mode (B/$\overline{W}$ = 1), for 8, 16 or 64 Kbyte configurations, $\overline{RAS0}$ is asserted for every byte transferred to or from the buffer. For 32 Kbyte configuration, $\overline{RAS0}$ is asserted during even byte transfers (A0 = 0), while $\overline{RAS1}$ is asserted during odd byte transfers (A0 = 1).

LOOPBACK

A loopback capability is provided to allow operation of EtherStar to be exercised without sending signals onto the LAN media. The loopback function is invoked by clearing the $\overline{LBC}$ bit, DLCR4<1>, to a zero. The complement of this bit appears at the Loopback output, LBC. Operation is illustrated in Figure 11.

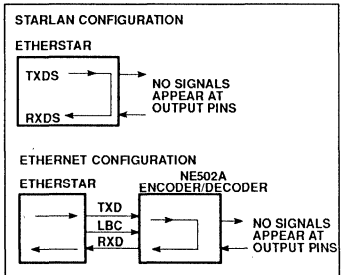


Figure 11. Loopback Operation

In StarLAN mode, the TXDS output is internally tied back to the RXDS input. The transmit data is blocked from appearing at the TXDS pin, and the RXDS and $\overline{XCOL}$ inputs are ignored. Data is routed from the transmit buffer, through the transmit section of the DLC, through the internal Manchester encoder, back to the Manchester decoder, through the receive section of the DLC, and is then stored in a receive buffer.

In Ethernet mode, operation is similar, except that the data is output on TXD and received at RXD. The external Manchester encoder/decoder, such as the NE502A, should respond to assertion of its LBC input by looping its transmitter output to its receiver input internally, and should block the transmit data from appearing at its output pin.

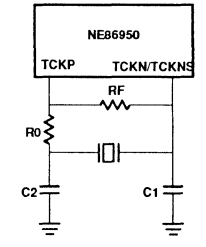


Figure 12. Crystal Connection for StarLAN Mode

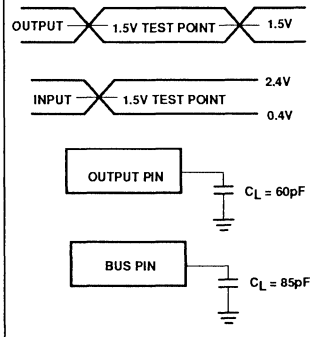


Figure 13. Test Conditions

CRYSTAL OSCILLATOR

The NE86950 requires a precise 10MHz clock source for proper operation. In Ethernet mode, this signal is normally supplied from the external encoder/decoder. In StarLAN mode, the signal may be supplied externally, or may be generated from a crystal by connecting the crystal as shown in Figure 12.

Table 1. Internal Register Address Map

BYTE/ WORD	$\overline{BACK}$	$\overline{DSEL}$	$\overline{RSEL}$	SA3	SA2	SA1	SA0	ADDRESS	DESCRIPTION
BYTE	1	1	0	0	0	0	0	DLCR0	Transmit Status
BYTE	1	1	0	0	0	0	1	DLCR1	Transmit Masks
BYTE	1	1	0	0	0	1	0	DLCR2	Receive Status
BYTE	1	1	0	0	0	1	1	DLCR3	Receive Masks
BYTE	1	1	0	0	1	0	0	DLCR4	Transmit Mode
BYTE	1	1	0	0	1	0	1	DLCR5	Receive Mode
BYTE	1	1	0	0	1	1	0	DLCR6	Software Reset
BYTE	1	1	0	0	1	1	1	DLCR7	TDR (LSB)
BYTE	1	1	0	1	0	0	0	DLCR8	Node ID0
BYTE	1	1	0	1	0	0	1	DLCR9	Node ID1
BYTE	1	1	0	1	0	1	0	DLCR10	Node ID2
BYTE	1	1	0	1	0	1	1	DLCR11	Node ID3
BYTE	1	1	0	1	1	0	0	DLCR12	Node ID4
BYTE	1	1	0	1	1	0	1	DLCR13	Node ID5
BYTE	1	1	0	1	1	1	0	DLCR14	Reserved
BYTE	1	1	0	1	1	1	1	DLCR15	TDR (MSB)
BOTH	1	0	1	0	0	0	0	BMPR0	Buffer Memory Port
BOTH	1	0	1	0	0	1	0	BMPR2	Packet Length LSB
BOTH	1	0	1	0	0	1	1	BMPR3	Packet Length MSB
BOTH	1	0	1	0	1	0	0	BMPR4	DMA Enable/Control
BOTH	0	1	1	X	X	X	X	BMPR0	Buffer Memory Port

Table 2. Data Link Controller Register Set Summary

DLCR	REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Transmit Status	READ	TMT OK	NET BSY	TMT REC	SRT PKT	UDR FLO	COL	16 COL	BUS WR ERR
		WRITE	—	—	—	—	CLR	CLR	CLR	CLR
1	Transmit Interrupt Masks	READ	MASK TMT OK	—	MASK TMTREC	—	MASK UDR FLO	MASK COL	MASK 16 COL	—
		WRITE	MASK TMT OK	—	MASK TMTREC	—	MASK UDR FLO	MASK COL	MASK 16 COL	—
2	Receive Status	READ	PKT RDY	BUS RD ERR	—	RMT RST	SRT PKT	ALG ERR	CRC ERR	OVR FLO
		WRITE	CLR	CLR	'0'*	—	CLR	CLR	CLR	CLR
3	Receive Interrupt Masks	READ	MASK PKT RDY	—	—	MASK RMTRST	MASK SRT PKT	MASK ALG ERR	MASK CRCERR	MASK OVR FLO
		WRITE	MASK PKT RDY	—	—	MASK RMTRST	MASK SRT PKT	MASK ALG ERR	MASK CRCERR	MASK OVR FLO
4	Transmit Mode	READ	COLCTR 3	COLCTR 2	COLCTR 1	COLCTR 0	CHP TST	$\overline{TM}$	$\overline{LBC}$	DSC
		WRITE	—	—	—	—	CHP TST	$\overline{TM}$	$\overline{LBC}$	DSC
5	Receive Mode	READ	TST	BUF EMP	BUF FUL	ADD SIZE	ENA SRT PKT	ENA REMRST	AM1	AM0
		WRITE	TST	—	—	ADD SIZE	ENA SRT PKT	ENA REMRST	AM1	AM0
6	Enable Data Link Controller		—	—	—	—	—	—	—	—
		WRITE ONLY	$\overline{ENA\ DLC}$	—	—	—	—	—	—	—
7	TDR (LSB)	READ ONLY	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
8	Node ID	READ WRITE	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0*
9	Node ID	READ WRITE	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
10	Node ID	READ WRITE	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
11	Node ID	READ WRITE	ID31	ID30	ID29	ID28	ID27	ID26	ID27	ID28
12	Node ID	READ WRITE	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
13	Node ID	READ WRITE	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
14	Reserved	—	—	—	—	—	—	—	—	—
15	TDR (MSB)	READ ONLY	—	—	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8

NOTES:
1. * A '1' should never be written into these bits.
2. The shaded bits indicate those that should be closely monitored/controlled by the host. Other status bits in DLCR2 and DLCR4 are automatically handled by EtherStar and are for information only, so thus may normally be masked.

Table 3. Buffer Memory Port Register Set Summary

BMPR	REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Buffer Memory Port	READ / WRITE	IN BYTE MODE, CONSECUTIVE **BYTES** ARE READ FROM OR WRITTEN TO THE BUFFER MEMORY BY READING/WRITING BMPR0. IN WORD MODE, CONSECUTIVE **WORDS** ARE READ FROM OR WRITTEN TO THE BUFFER MEMORY BY READING/WRITING BMPR0.							
2	Packet Length LSB	—	—	—	—	—	—	—	—	—
		WRITE ONLY	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0
3	Packet Length MSB	—	—	—	—	—	—	—	—	—
		WRITE ONLY	TMST	—	—	—	—	PL10	PL9	PL8
4	DMA Enable/Status	READ	—	—	—	—	EOP INT MASK *	EOP *	—	—
		WRITE	—	—	—	—	EOP INT MASK *	CLR EOP STATUS *	RENA	TENA

NOTE:
1. * These bits are not implemented in the NE86950A version of EtherStar.

Table 4. Data Link Controller Register Descriptions

DLCR0 –Transmit Status, Read/Write

This register provides transmit status to the host. The user may program the assertion of bits 7, 5, 3, 2 and 1 of this register to cause the assertion of the Transmit interrupt output ($\overline{TINT}$ = 0) by setting the corresponding bits in DLCR1. Assertion of bit 0 of this register will cause assertion of $\overline{TINT}$ –this bit is not maskable.
Bits <3:0> may be cleared individually or in any combination by writing a '1' to those bits. The state of bits written with a '0' is not affected. Bit <7:4> are cleared automatically as described below.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	TMT OK	NET BSY	TMT REC	SRT PKT	UDR FLO	COL	16 COL	BUS WR ERR
WRITE	—	—	—	—	CLR	CLR	CLR	CLR

BIT	SYMBOL	DESCRIPTION
0	BUS WR ERR	**BUS WRITE ERROR**: This error condition occurs if a $\overline{RDY}$ response cannot be issued within 2.4µs after the $\overline{WRT}$ signal is asserted by the host system when writing to the buffer memory port register, BMPR0. Occurs when the transmit buffer memory is full. This should not happen during normal operation.
1	16 COL	**16 COLLISION**: This bit is set after the sixteenth unsuccessful transmission of the same packet.
2	COL	**COLLISION**: This bit is set if a collision occurs during transmission of a data packet. The buffer manager will automatically attempt to transmit the current packet up to 16 times. The user may determine the number of consecutive collisions by reading the collision counter, DCLR4<7:4>.
3	UDR FLO	**UNDERFLOW**: This register is set when data from the transmit section of buffer memory is not available for serial transmission. EtherStar will continue to send out this data frame. This should not occur during normal operation.
4	SRT PKT	**SHORT PACKET**: Set if the Received Carrier Detect input (XCD) is negated during a packet transmission. This can be caused by a collision or a shorted LAN media. Automatically cleared as each transmission begins.
5	TMT REC	**TRANSMIT RECEIVED**: Indicates that a good packet was received by the receiver shortly after transmission was completed. This is used to indicate self–reception of the packet. This allows the software to take advantage of the hardware address matching even in systems which are designed for half duplex operation. This bit is cleared as each transmission begins.
6	NET BSY	**NET BUSY**: This is a copy of XCD, the Receive Carrier Detect pin.
7	TMT OK	**TRANSMIT OKAY**: This bit is set when a data packet is successfully transmitted. EtherStar clears this bit automatically as each transmission begins and sets it automatically at the finish of each data packet transmission.

Table 4. Data Link Controller Register Descriptions (Continued)

DLCR1 –Transmit Interrupt Masks, Read/Write

Bits 7, 5, 3, 2, 1 are the transmit interrupt masks. They can be set individually depending on system requirements. Setting a bit to a '1' causes the assertion of the corresponding bit in DLCR0 to assert $\overline{TINT}$.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ WRITE	MASK TMT OK	—	MASK TMT REC	—	MASK UDR FLO	MASK COL	MASK 16 COL	—

DLCR2 –Receive Status, Read/Write

This register provides receive status to the host. The user may program the assertion of bits 7 and <4:0> of this register to cause the assertion of the Receive Interrupt output ($\overline{RINT}$ = 0) by setting the corresponding bits in DLCR3. Assertion of bit 6 of this register will cause assertion of $\overline{RINT}$ –this bit is not maskable.
Bits <7:6> and <3:0> may be cleared individually or in any combination by writing a '1' to those bits. The state of bits written with a '0' is not affected. Bit 4 is cleared automatically as described below.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PKT RDY	BUS RD ERR	—	RMT RST	SRT PKT	ALG ERR	CRC ERR	OVR FLO
WRITE	CLR	CLR	'0'	—	CLR	CLR	CLR	CLR

BIT	SYMBOL	DESCRIPTION
0	OVR FLO	**OVERFLOW**: This bit is asserted if a received packet is discarded because there is insufficient memory space in the receive buffer memory to accommodate the complete data packet. The space remaining is made available for shorter data packets.
1	CRC ERR	**CRC ERROR**: This bit is set when the calculated CRC does not match the CRC at the end of the received packet.
2	ALG ERR	**ALIGNMENT ERROR**: Set if a packet has bad CRC at the last octet boundary and the number of bits are not divisible by eight.
3	SRT PKT	**SHORT PACKET**: Set if a data packet does not meet the minimum length requirements of 60 bytes or 6 bytes when the enable short packet bit, DLCR5<3>, is on.
4	RMT RST	**REMOTE RESET**: This bit will be set when the ENA RMT RST bit, DLCR5<2>, is on and a receive packet with the special data length 0900H is successfully received. The RMT RST bit, when set, will assert the PRES pin. The bit is cleared at the beginning of the next packet reception. This bit is set only if the node ID matches, not on multicast or broadcast addresses, in any address match mode (see DLCR5<1:0>).
5	—	**RESERVED**: Never write a "1" into this bit.
6	BUS RD ERR	**BUS READ ERROR**: This error condition occurs if a $\overline{RDY}$ response cannot be issued within 2.4µs after the $\overline{RD}$ signal is asserted by the system when reading the buffer memory port register, BMPR0. Occurs when trying to read when the receive buffer memory is empty.
7	PKT RDY	**PACKET READY**: Set after the successful reception of packet data into the receive buffer memory.

DLCR3 –Receive Masks, Read/Write

Bits 7and <4:0> are the receive interrupt masks. Setting a bit to a '1; causes the assertion of the corresponding bit in DLCR2 to assert $\overline{RINT}$.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ WRITE	MASK PKT RDY	—	—	MASK RMT RST	MASK SRT PKT	MASK ALG ERR	MASK CRC ERR	MASK OVR FLO

Table 4. Data Link Controller Registers Descriptions (Continued)

DLCR4 –Transmit Mode, Read/Write

This register controls certain transmit functions and provides the count of successive collisions on transmission attempts.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	COL CTR 3	COL CTR 2	COL CTR 1	COL CTR 0	CHP TST	$\overline{TM}$	$\overline{LBC}$	DSC
WRITE	—	—	—	—	CHP TST	$\overline{TM}$	$\overline{LBC}$	DSC

BIT	SYMBOL	DESCRIPTION
0	DSC	**DISABLE CARRIER DETECT**: When this bit is set the transmitter disregards XCD, the Carrier Detect signal.
1	$\overline{LBC}$	**LOOPBACK CONTROL**: This bit controls the loopback function of the external encoder/decoder in Ethernet mode, and the internal loopback function in StarLAN mode. The LBC pin signal value is the complement of the value of this bit, '0' = Loopback, '1' = No Loopback.
2	$\overline{TM}$	**TEST MODE**: A bit whose complement is available as singal pin TM. Used for controlling power to the transceiver or any other function external to the chip.
3	CHP TST	**CHIP TEST**: Signetics internal use. Always write a '0' to this bit for normal operation.
<7:4>	COL CTR	**COLLISION COUNTER**: Bits <7:4> keep track of the number of consecutive collisions during transmission of a data packet.

Table 4. Data Link Controller Register Descriptions (Continued)

DLCR5 –Receive Mode, Read/Write

This register controls certain receive functions and provides receive buffer memory status.

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	TST	BUF EMP	BUF FUL	ADD SZE	ENA SRT PKT	ENA REM RST	AM1	AM0
WRITE	TST	—	—	ADD SZE	ENA SRT PKT	ENA REM RST	AM1	AM0

BIT	SYMBOL	DESCRIPTION
<1:0>	AM1, AM0	**ADDRESS MATCH MODE**: These two bits control address recognition and matching. Bit 1 / Bit 0 / Function 0 / 0 / Accept no packets. 0 / 1 / Accept physical address, multicast–group addresses which match the first three bytes, and broadcast address. 1 / 0 / Accept physical address, all multicast addresses, and broadcast address. 1 / 1 / Accept all packets (promiscuous mode).
2	ENA RMT RST	**ENABLE REMOTE RESET**: This bit is used to enable/disable the receipt of packets with the special data length 0900H. See DLCR2<4>.
3	ENA SRT PKT	**ENABLE SHORT PACKET**: When set to "1", the receive section will receive packets as short as six bytes. When reset to "0", the receive section of buffer memory will receive between 60 bytes and two Kbytes.
4	ADD SZE	**ADDRESS SIZE**: When set, this bit reduces the node ID address match to five bytes rather than the normal six bytes. This is used where the node is used to perform some multiplex function on the least significant byte of the destination address.
5	BUF FUL	**BUFFER FULL**: This bit provides real–time status of the receive buffer memory. As a packet is being loaded into the buffer memory from the data link controller, this bit will be set if the empty space remaining becomes equal to or less than eight bytes. This bit will automatically clear when the space remaining becomes more than eight bytes due to a) the packet being rejected and sufficient memory freed by the buffer manager or b) the host reading enough data from the buffer.
6	BUF EMP	**BUFFER EMPTY**: Indicates that the buffer memory is empty. A "0" indicates that there is at least one good data packet in the receive section. A "1" indicates that the receive section is empty. This bit gives the host software an indication to continue reading additional data frames from the receive buffer after successful reading of a packet.
7	TST	**TEST**: This bit is used for testing purposes. When EtherStar is in the receive mode, this bit set to "1" fixes four bytes of the CRC to C7, 04, DD, 7B. This value is shifted into the CRC register and checked without being modified. When EtherStar is transmitting, the back–off algorithm is changed to $2e^{(n-1)} + 1$, where n is the number of collisions.

DLCR6 –Enable Data Link Controller, Write Only

RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WRITE ONLY	$\overline{\text{ENA DLC}}$	—	—	—	—	—	—	—

BIT	SYMBOL	DESCRIPTION
<6:0>	—	**Not used.**
7	$\overline{\text{ENA DLC}}$	**ENABLE DATA LINK CONTROLLER**: This bit must be cleared by writing a "0" into the location after the other DLC registers have been programmed. After this bit is cleared, EtherStar is ready to transmit and receive. At least 15µs must elapse between the end of the hardware reset pulse falling edge and the writing of $\overline{\text{ENA DLC}}$. "1" will release EtherStar from any activity on the network. Node ID registers DLCR8–13 read/write only when this bit is "1".

Table 4. Data Link Controller Register Descriptions (Continued)

DLCR7 –TDR Register LSBs, Read Only, DLCR15 – TDR Registers MSBs, Read Only

A Time Domain Reflectometer (TDR) function is provided by this 14–bit counter that counts the number of bits successfully transmtted for each packet. The purpose of this function is to provide a rough measure of the distance of the unit on the network to some media fault, either a short or an open.
The counter is cleared at the beginning of each transmission and counts bits from that time until the Carrier Detect input (XCD) negates or a collision is detected. The counter is also cleared after each successful data packet transmission. The LSBs are read from DLCR7, the MSBs from DLCR15.

	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DLCR7	READ ONLY	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
DLCR15	READ ONLY	—	—	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8

DLCR8:DLCR13 –Node ID Registers, Read/Write

The node ID is comprised of the six bytes contained in DLCR8 through DLCR13. EtherStar compares this node ID with the destination field of all packets on the LAN media to determine if there is a match. If the two addresses match, and the address match mode in DLCR5<1:0> allows reception, the packet is received into buffer memory. DLCR8 is the LS byte and DLCR13 is the MS byte of the node ID. The node ID is reduced to the five MS bytes (DLCR9 to DLCR13) if DLCR5<4> is set to a '1'.
These registers are accessible for read/write operation only when the data link controller has been disabled via DLCR6<7> or immediately after reset.

	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DLCR8	READ WRITE	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0*
DLCR9	READ WRITE	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
DLCR10	READ WRITE	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
DLCR11	READ WRITE	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
DLCR12	READ WRITE	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
DLCR13	READ WRITE	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40

*Do not program to '1'.

Table 5. Buffer Manager Port/Register Descriptions

DMPR0 –Buffer Memory Port Register, Read/Write

This register provides the host access to the buffer memory. Writing a byte/word to this port transfers that data to the currently addressed location in the transmit buffer and increments the transmit buffer pointer to point to the next byte/word. Reading a byte/word from this port transfers the contents of the currently addressed location in the receive buffer to the host and increments the receive buffer pointer to point to the next byte/word. See DLCR0<0>, DLCR2<6>, DLCR5<5> and DLCR5<6> for additional information.
This register is byte access only in byte mode and word access only in word mode (the upper and lower bytes cannot be accessed independently in word mode).

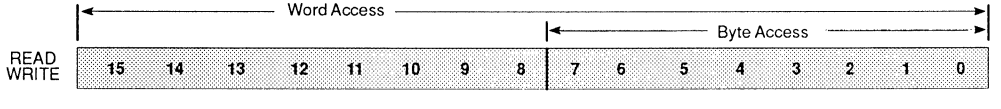


Table 5. Buffer Manager Port/Register Descriptions (Continued)

BMPR3:BMPR2 –Packet Length Registers, Write Only

The host writes to these registers to define the length of the packet which was loaded for transmission into the currently addressed transmit buffer. The LS byte is in the BMPR2, the MS bits are in BMPR3. The transmit start bit, TMST in BMPR3, is set when BMPR3 is written to inform the buffer manager that the data and packet length have been provided and that it should initiate transmission of that packet via the data link controller.
In byte access mode, the LS byte must be written first, followed by the MS bits and TMST in BMPR3.

	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BMPR2	WRITE ONLY	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0
BMPR3	WRITE ONLY	TMST	—	—	—	—	PL10	PL9	PL8

BMPR4 –DMA Control and Status Register, Read/Write

This register enables/disables DMA operation for accessing the buffer memory, and provides DMA status.

	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BMPR2	READ	—	—	—	—	EOP INT MASK	EOP	—	—
BMPR3	WRITE	—	—	—	—	EOP INT MASK	CLR EOP	RENA	TENA

BIT	SYMBOL	DESCRIPTION
0	TENA	**TRANSMIT DMA ENABLE**: A '1' enables DMA write operation between the host and the buffer memory. A '0' disables DMA write operation between the host and the buffer memory. Write only.
1	RENA	**RECEIVE DMA ENABLE**: A '1' enables DMA read operation between the host and the buffer memory. A '0' disables DMA read operation between the host and the buffer memory. Write only.
2	EOP	**END OF PROCESS**: Indicates that an entire packet has been transferred between the buffer memory and the host. Set to a '1' when the external DMA controller asserts the EOP input. The host should respond by clearing RENA or TENA. When this bit is set, the Receive Interrupt output, $\overline{RINT}$, will be asserted if this action has been enabled by setting bit 3 of this register. Writing a '1' to this bit clears the status bit, writing a '0' has no effect. Read/write. **NOTE:** This function is not implemented in the NE86950A version of EtherStar.
3	EOP INT MASK	**EOP INTERRUPT MASK**: Writing a '1' to this bit will cause $\overline{RINT}$ to be asserted when the EOP status bit, bit 2 of this register, is also set. Writing a '0' to this register masks $\overline{RINT}$ from being asserted by that condition. Read/write. **NOTE:** This function is not implemented in the NE86950A version of EtherStar.
<7:4>	—	**Not used.**

Table 6. Address Multiplexing on Buffer Address Outputs

External / Internal	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
RAS ADDRESS	A13	A12	A11	A10	A9	A8	A7	A6
CAS ADDRESS	A15	A5	A4	A3	A2	A1	A0	A14

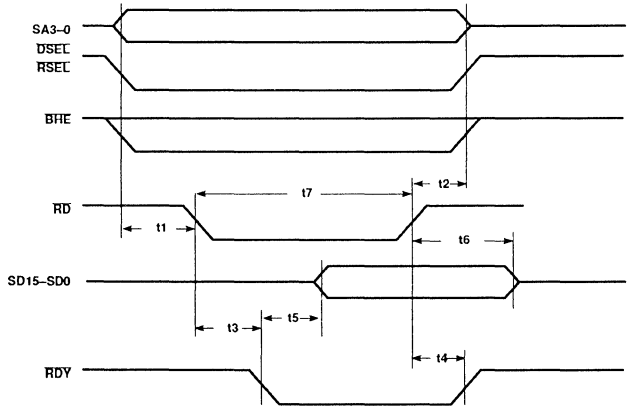


Figure 14. Read Timing

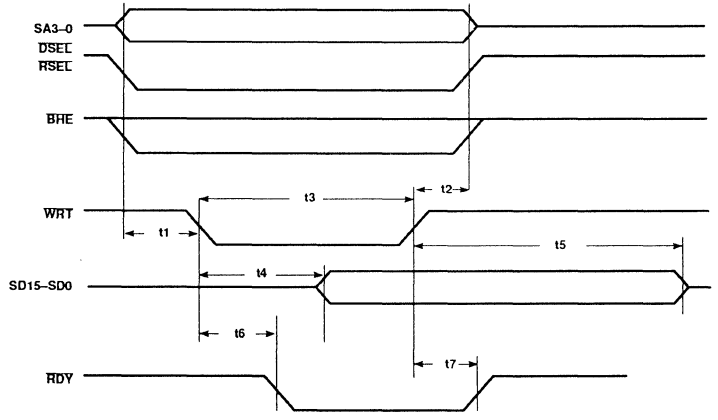


Figure 15. Write Timing

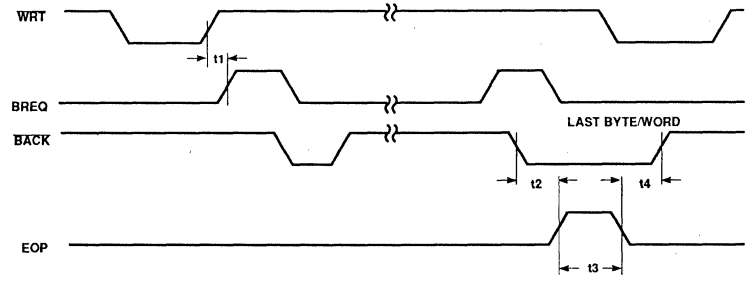


Figure 16. BREQ, BACK and EOP DMA Timing

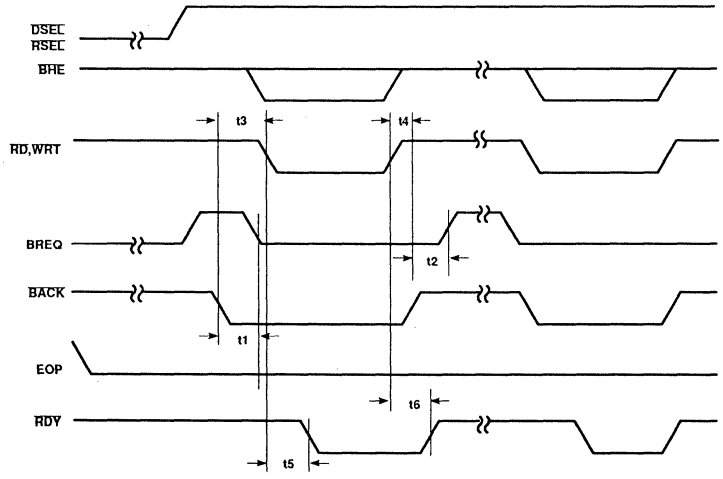


Figure 17. DMA Read and Write Timing

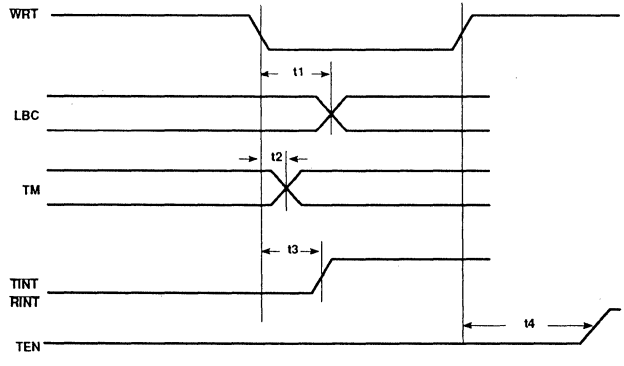


Figure 18. LBC, TM, TINT, and RINT Timing

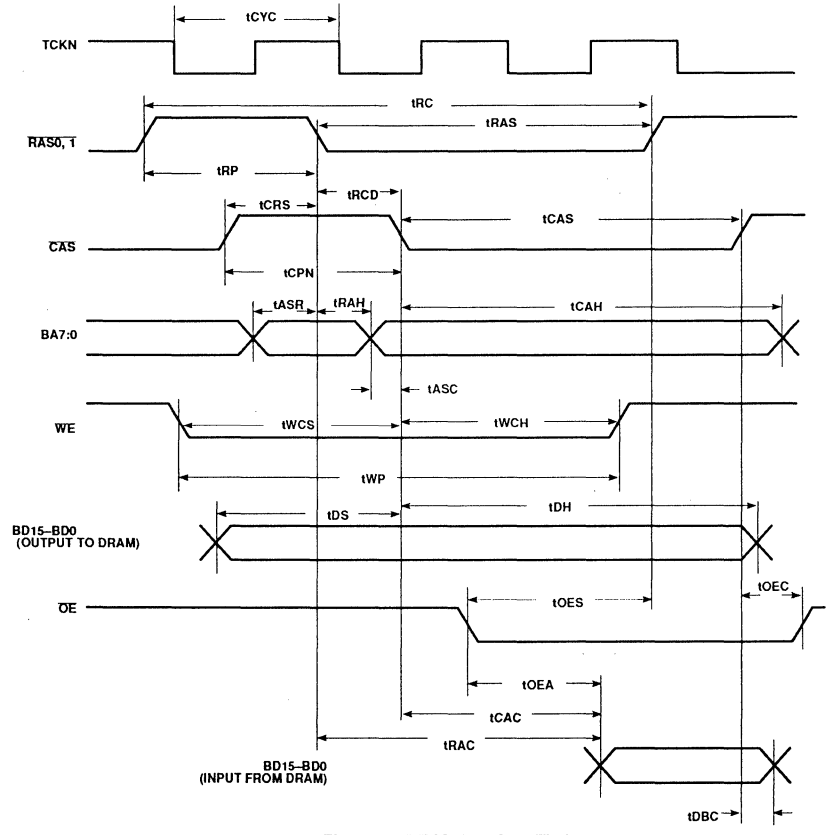


Figure 19. DRAM Interface Timing

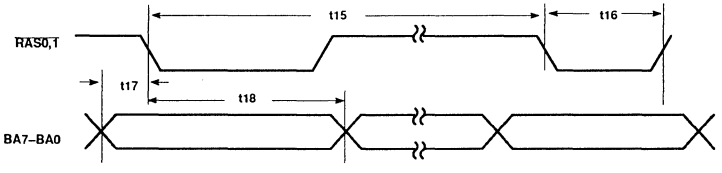


Figure 20. DRAM Refresh Timing

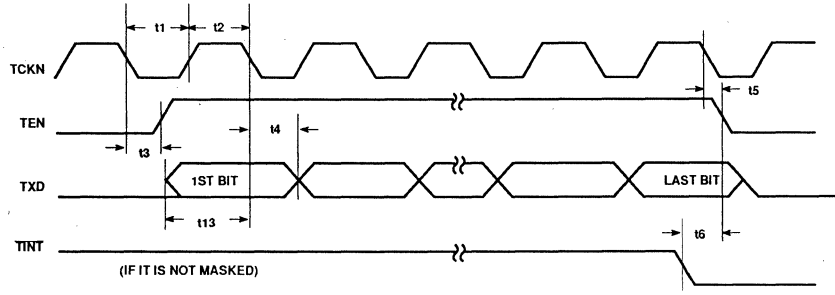


Figure 21. Transmit In Ethernet Configuration

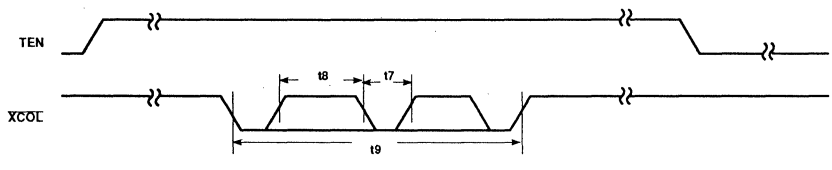


Figure 22. Collision Timing

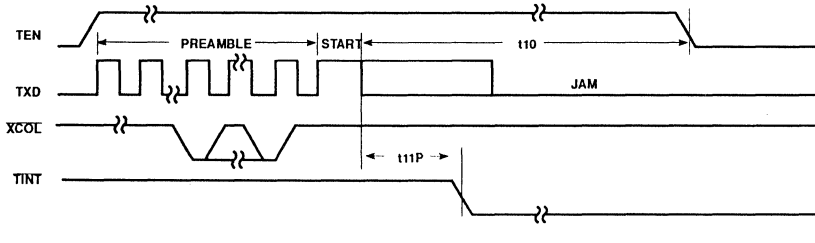


Figure 23. Collision at the Preamble Field

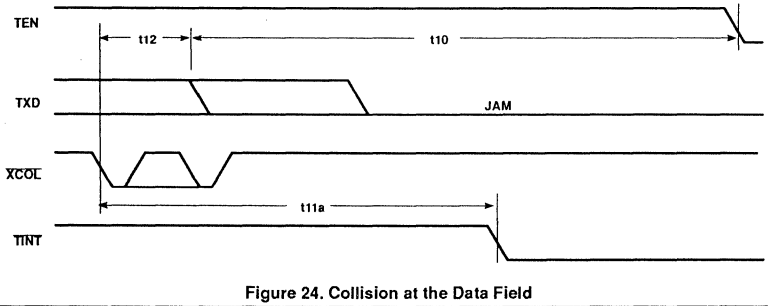


Figure 24. Collision at the Data Field

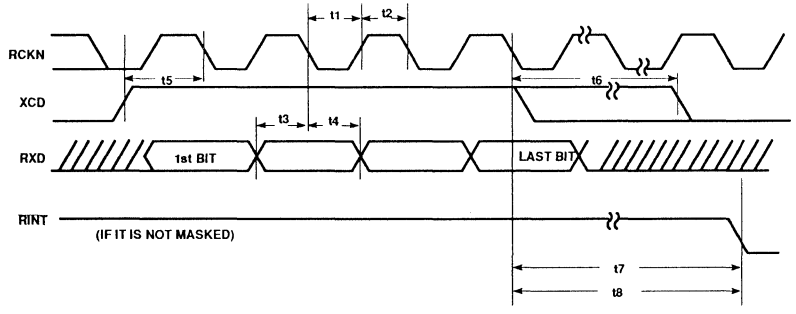


Figure 25. Receive in Ethernet Configuration

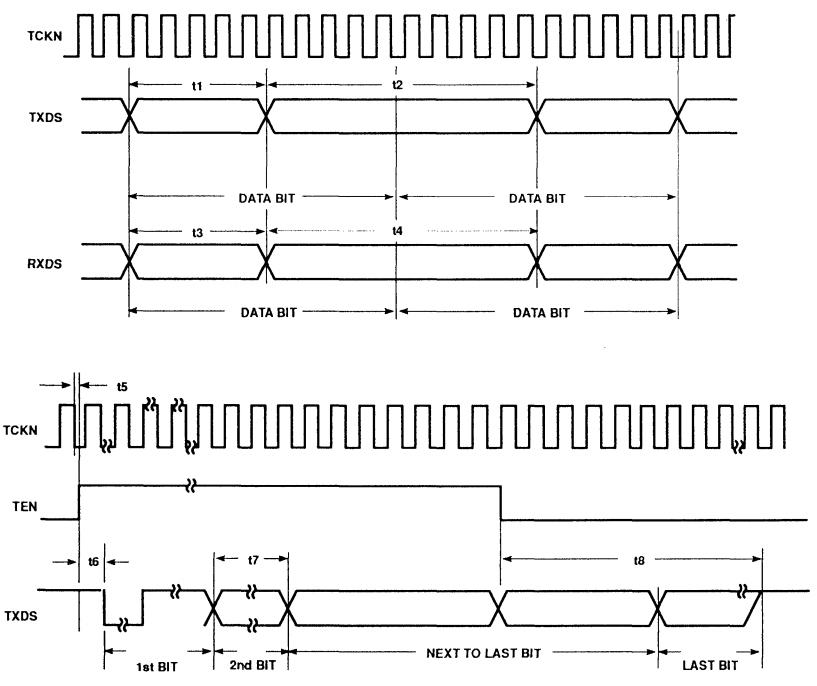


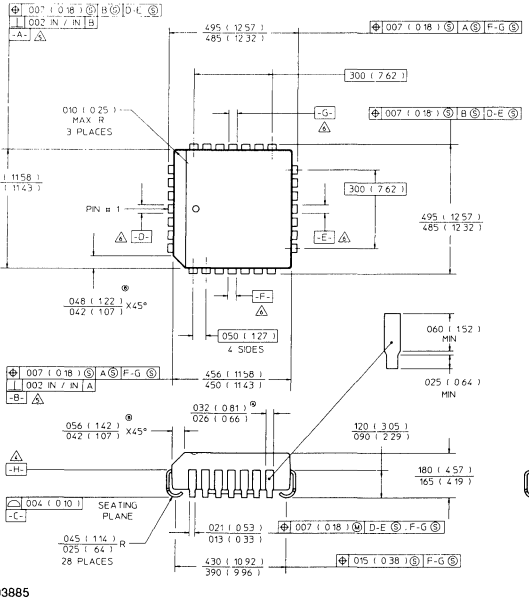
Figure 26. StarLAN Transmit and Receive Timing

Section 5
Package Outlines

Package Outlines

Data Communication Products

28-PIN PLASTIC LEADED CHIP CARRIER



NOTES

1 PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MO-047-AB FOR PLASTIC LEADED CHIP CARRIER 28 LEADS, .050 INCH LEAD SPACING, SQUARE (ISSUE A, 10/31/84)

2 CONTROLLING DIMENSIONS INCHES. METRIC DIMENSIONS IN mm ARE SHOWN IN PARENTHESES

3 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982

△4 DATUM PLANE -H- LOCATED AT THE TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD WHERE LEAD EXITS PLASTIC BODY

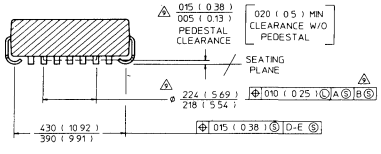
△5 LOCATION TO DATUM -A- AND -B- TO BE DETERMINED AT PLANE -H- THESE DATUMS DO NOT INCLUDE MOLD FLASH. MOLD FLASH PROTRUSION SHALL NOT EXCEED .006" (0.15 mm) ON ANY SIDE

△6 DATUM D-E AND F-G ARE DETERMINED WHERE THESE CENTER LEADS EXIT FROM THE BODY AT PLANE -H-

7 PIN NUMBERS CONTINUE COUNTERCLOCKWISE TO PIN 28 (TOP VIEW)

8 SIGNETICS ORDER CODE FOR PRODUCT PACKAGED IN A PLCC IS THE SUFFIX "A" AFTER THE PRODUCT NUMBER

△7 APPLICABLE TO PACKAGES WITH PEDESTAL ONLY

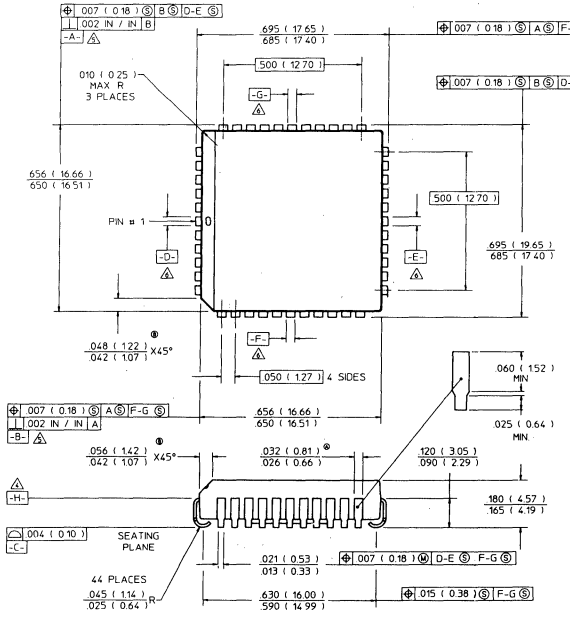


853-0401 93885

AQ1

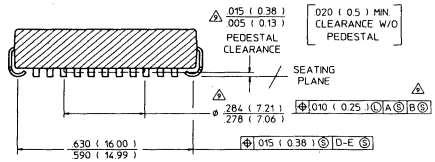
Package Outlines

44-PIN PLASTIC LEADED CHIP CARRIER



NOTES

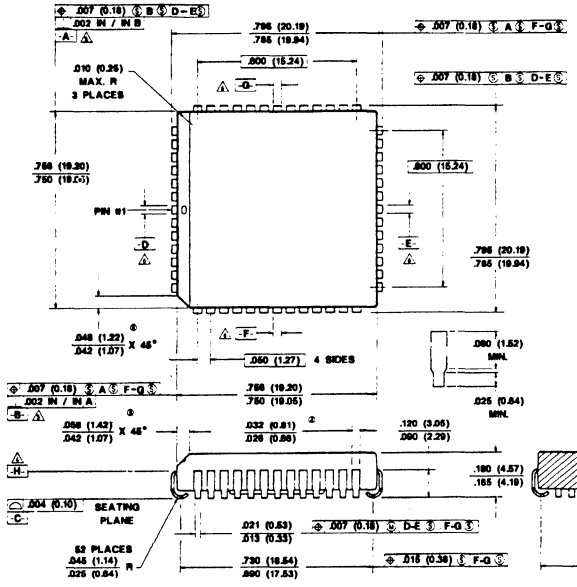
1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MO-047-AL FOR PLASTIC LEADED CHIP CARRIER 44 LEADS, .050 INCH LEAD SPACING, SQUARE. (ISSUE A, 10/31/84)
2. CONTROLLING DIMENSIONS: INCHES METRIC DIMENSIONS IN mm ARE SHOWN IN PARENTHESES.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
4. DATUM PLANE -H- LOCATED AT THE TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS PLASTIC BODY.
5. LOCATION TO DATUM -A- AND -B- TO BE DETERMINED AT PLANE -H-. THESE DATUMS DO NOT INCLUDE MOLD FLASH. MOLD FLASH PROTRUSION SHALL NOT EXCEED .006" (0.15 mm) ON ANY SIDE.
6. DATUM D-E AND F-G ARE DETERMINED WHERE THESE CENTER LEADS EXIT FROM THE BODY AT PLANE -H-.
7. PIN NUMBERS CONTINUE COUNTERCLOCKWISE TO PIN 44 (TOP VIEW).
8. SIGNETICS ORDER CODE FOR PRODUCT PACKAGED IN A PLCC IS THE SUFFIX "A" AFTER THE PRODUCT NUMBER.
9. APPLICABLE TO PACKAGES WITH PEDESTAL ONLY.



853-0403 93885 AX1

Package Outlines

52-PIN PLASTIC LEADED CHIP CARRIER



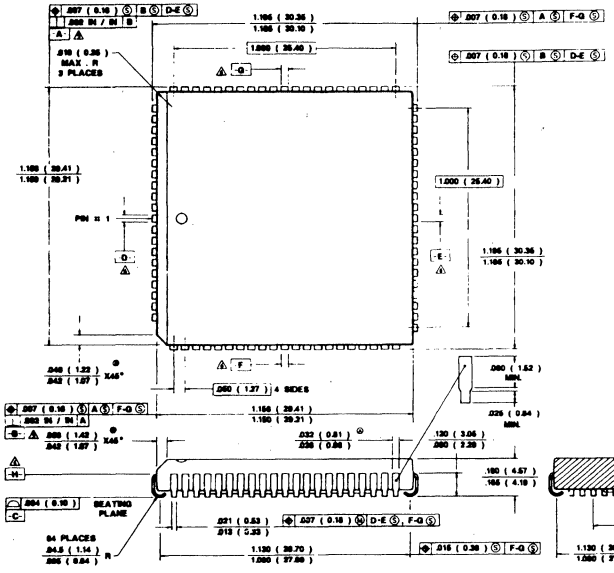
853-0397 93885 AA1

NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AD for plastic leaded chip carrier 52 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #52 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

Package Outlines

84-PIN SQUARE PLASTIC LEADED CHIP CARRIER



NOTES:

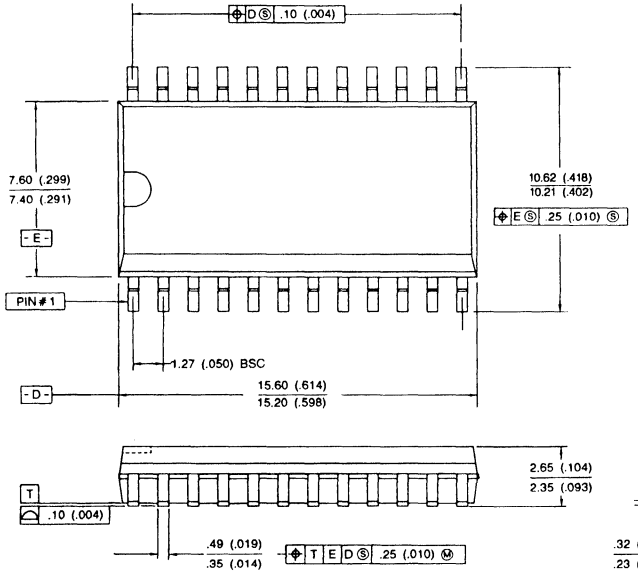
1. Package dimensions conform to JEDEC specification MO-047-AF for plastic leaded chip carrier 84 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #84 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

853-0399 93885

AC1

Package Outlines

24-PIN PLASTIC SOL



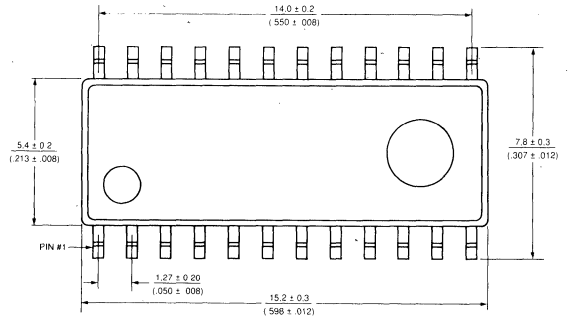
NOTES:

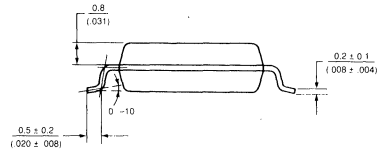
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0173 82949 DN2

Package Outlines

24-PIN PLASTIC SOL (EIAJ TYPE II OUTLINE)





NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm) DIMENSIONS IN PARENTHESES ARE IN INCHES.
2. PIN NUMBERS START WITH PIN #1 AND CONTINUE COUNTERCLOCKWISE TO PIN #24 WHEN VIEWED FROM TOP.

* THIS IS NOT A JEDEC OUTLINE FOR JEDEC SO 24 OUTLINE SEE DRAWING 853-0173

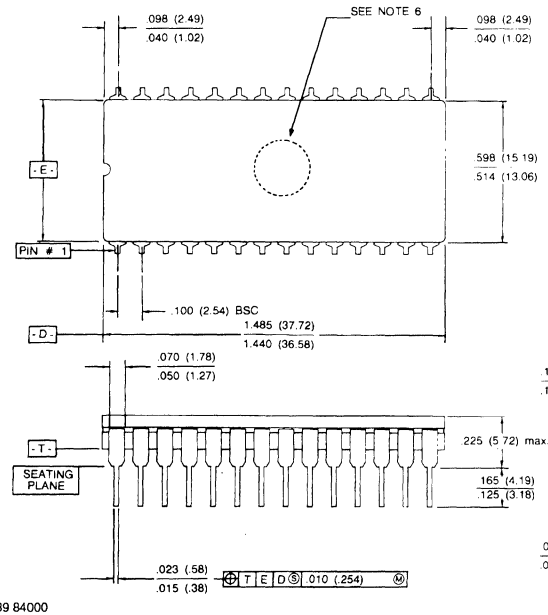
EIAJ Type II Outline

853-1460 000238

DNB

Package Outlines

28-PIN CERAMIC DIP (600 MILS WIDE)



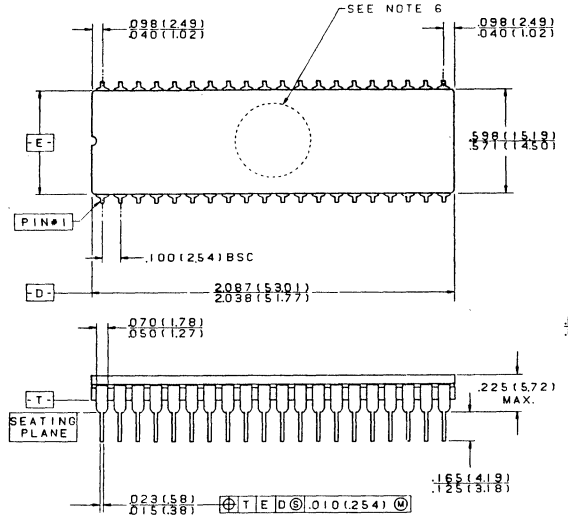
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.
6. Denotes window location for EPROM products (see FA package).

853-0589 84000

FQ3

Package Outlines

40-PIN CERAMIC DIP (600 MILS WIDE)



NOTES:

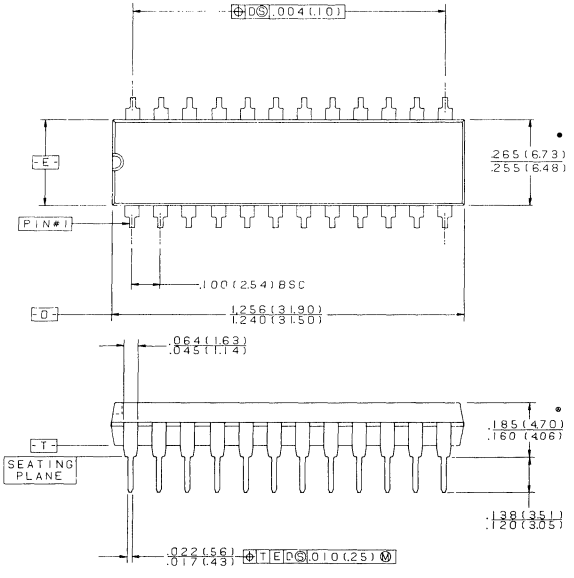
1. CONTROLLING DIMENSION: INCHES. MILLIMETERS ARE SHOWN IN PARENTHESIS.
2. DIMENSION AND TOLERANCING PER ANSI Y14.5M-1982.
3. "T", "D", AND "E" ARE REFERANCE DATUMS ON THE BODY AND INCLUDE ALLOWANCE FOR GLASS OVERRUN AND MENISCUS ON THE SEAL LINE, AND LID TO BASE MISMATCH.
4. THESE DIMENSIONS MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
5. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#40 WHEN VIEWED FROM THE TOP.
6. DENOTES WINDOW LOCATION FOR EPROM PRODUCTS.

853-0590 95528

FW3

Package Outlines

24-PIN PLASTIC DIP (300 MILS WIDE)



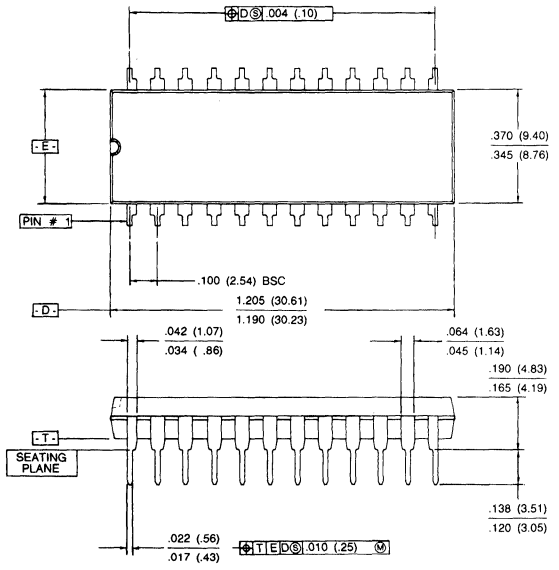
NOTES

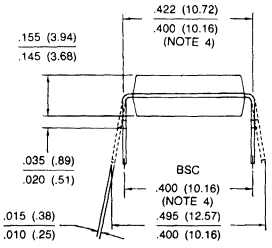
1. CONTROLLING DIMENSION: INCHES MILLIMETRIC ARE SHOWN IN PARENTHESES.
2. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-001-AF FOR STANDARD DUAL IN-LINE (DIP) PACKAGE .300 INCH ROW SPACING (PLASTIC) 24 LEADS (ISSUE B, 7/85)
3. DIMENSION AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D", AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (.25MM) ON ANY SIDE.
5. THESE DIMENSIONS MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#24 WHEN VIEWED FROM THE TOP.

853-0410 98727 NN1

Package Outlines

24-PIN PLASTIC DIP (400 MILS WIDE)





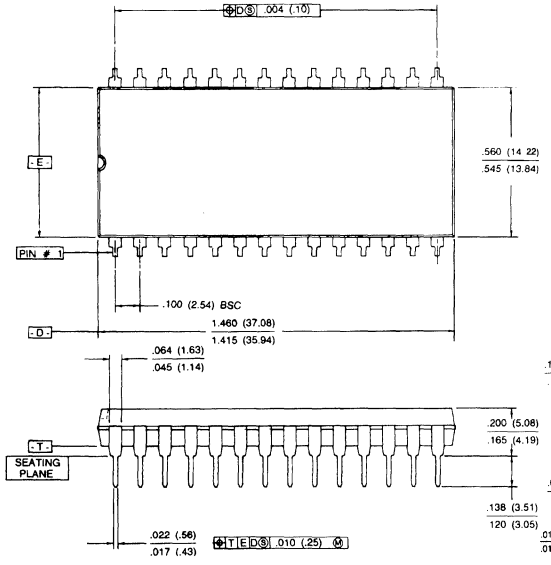
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14. 5M-1982.
3. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0411 81237

NN2

Package Outlines

28-PIN PLASTIC DIP (600 MILS WIDE)



NOTES:

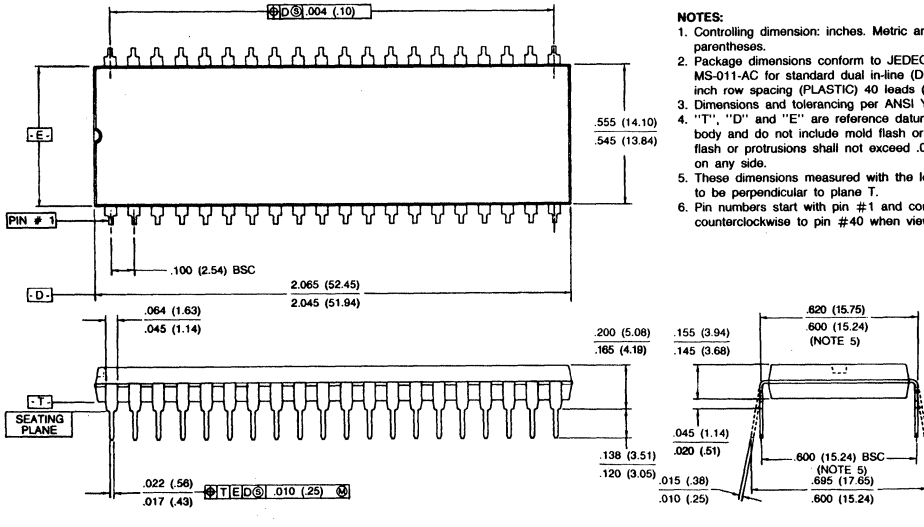
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

853-0413 84099

NQ3

Package Outlines

40-PIN PLASTIC DIP (600 MILS WIDE)

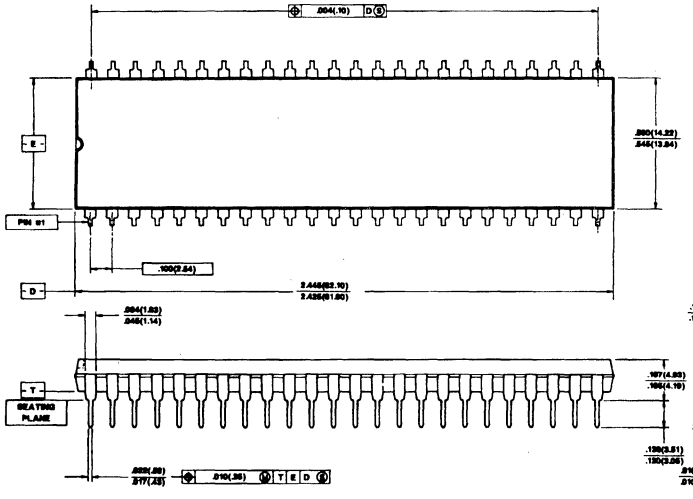


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AC for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 40 leads (issue B. 7/85)
3. Dimensions and toleranced per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #40 when viewed from the top.

853-0415 84971 NW3

Package Outlines

48-PIN PLASTIC DIP



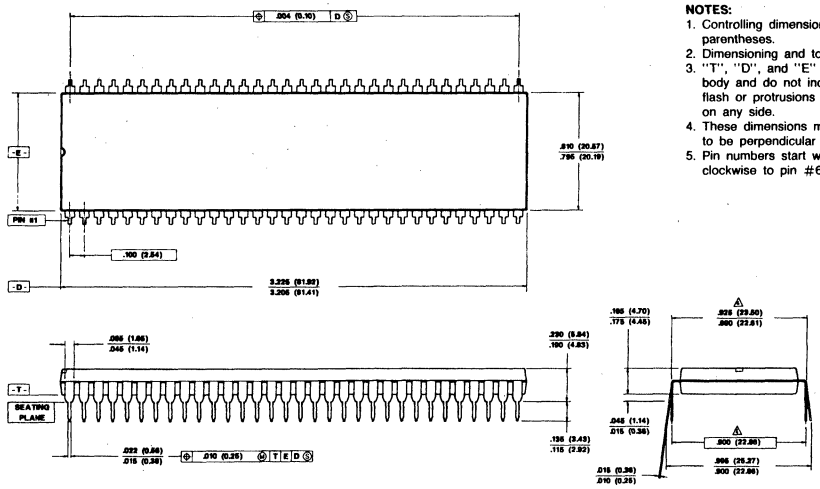
NOTES:
1. Controlling dimensions: inches. Metric are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y145M-1982.
3. "T", "D", and "E" are reference Datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (25mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to plane "T".
5. Pin numbers start with #1 and continue counter-clockwise to pin "48 when viewed from the top.

853-0416 93945

NY3

Package Outlines

64-PIN PLASTIC DIP



NOTES:
1. Controlling dimensions: inches. Metric are shown in parentheses.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "T", "D", and "E" are reference Datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (25mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to plane "T".
5. Pin numbers start with #1 and continue counter-clockwise to pin #64 when viewed from the top.

853-0414 93945 NS4

Section 6
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Sales Offices, Representatives & Distributors

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11/9/90

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages iii to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
Supplement to IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom** Bipolar, MOS Radio pagers Mobile telephones ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

current code	new code	handbook title
S1	**SC01**	**Diodes** High-voltage tripler units
S2a	**SC02***	**Power diodes**
S2b	**SC03***	**Thyristors and triacs**
S3	**SC04**	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07**	**Small-signal field-effect transistors**
S6	**SC08** **SC09**	**RF power transistors** **RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8a	**SC11***	**Light emitting diodes**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14**	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**
S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T8	**DC01**	**Colour display components**
T16	**DC02**	**Monochrome monitor tubes and deflection units**
C2	**DC03**	**Television tuners, coaxial aerial input assemblies**
C3	**DC04***	**Loudspeakers**
C20	**DC05**	**Flyback transformers, mains transformers and general-purpose FXC assemblies**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
C14	**PA01**	**Electrolytic capacitors; solid and non-solid**
C11	**PA02**	**Varistors, thermistors and sensors**
C12	**PA03**	**Potentiometers and switches**
C7	**PA04**	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08**	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T1	*	Power tubes for RF heating and communications
T2a	*	Transmitting tubes for communications, glass types
T2b	*	Transmitting tubes for communications, ceramic types
T3	PC01**	High-power klystrons
T4	*	Magnetrons for microwave heating
T5	PC02**	Cathode-ray tubes
T6	PC03**	Geiger-Müller tubes
T9	PC04**	Photo and electron multipliers
T10	PC05	Plumbicon camera tubes and accessories
T11	PC06	Circulators and Isolators
T12	PC07	Vidicon and Newvicon camera tubes and deflection units
T13	PC08	Image intensifiers
T15	PC09**	Dry reed switches
C8	PC10	Variable mains transformers; annular fixed transformers
	PC11	Solid state image sensors and peripheral integrated circuits

* These handbooks will not be reissued.
** Not yet issued with the new code in this series of handbooks.

MATERIALS

This series of data handbooks comprises:

current code	new code	handbook title
C4 C5	MA01*	**Soft Ferrites**
C16	MA02**	**Permanent magnet materials**
C19	MA03**	**Piezoelectric ceramics**

* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

** Not yet issued with the new code in this series of handbooks.

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