Signetics Linear Data and Applications Manual Vol. II 1985

Signetics

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Linear Data and Applications Manual 1985 Volume II

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Signetics

Linear Products

Preface

The Linear Division, one of five Signetics divisions, is a major supplier of a broad line of linear integrated circuits ranging from high-performance designs to many of the more popular industry standard devices and custom designs.

Employing Signetics' high quality processing and screening standards, the Linear Division is dedicated to providing high quality Linear products to our worldwide customers. Our full product line addresses the needs of the EDP, Automotive, Industrial, Consumer, and Communications markets.

The 1985 Linear Data and Applications Manual Volume II provides complete technical data on our full line of interface, communication, amplifier, power conversion and control, and video products. Among these you will find new entrants such as the NE5205 high frequency amplifier, NE5170 and NE5180/5181 octal line driver and receivers, the DAC800 12-Bit D/A Converter, TCA520 low voltage amplifier, and the TDA1520 20 watt amplifier.

Extensive Applications, Telephony, and Video sections and selector guides are also included in this volume.

Volume II is intended to be a companion to Volume I, published in October 1984. This present volume has a Table of Contents which contains a complete listing of all products in both Volumes I and II.

Although every attempt has been made to insure accuracy of information in this manual, Signetics assumes no liability for inadvertent errors.

Your suggestions for improvement in future editions are welcome.

Signetics

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Linear Products

*For up-to-date cross reference information, contact your local sales office.

Listings in bold face will be found in Volume II. Listings in regular face will be found in Volume I. Please contact your local sales office for a copy of Volume I.

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Linear Products

SO Availability

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*LF398D	SO-14	Sample and Hold Amp
LM1870D	SOL-20	Stereo Demodulator
LM2901D	SO-14	Quad Volt Comparator
LM2903D	SO-8	Dual Volt Comparator
LM311D	SO-8	Voltage Comparator
LM319D	SO-14	High Speed Dual Comparator
LM324AD	SO-14	Quad Op Amp
LM324D	SO-14	Quad Op Amp
LM339D	SO-14	Quad Volt Comparator
LM358D	SO-8	Dual Op Amp
LM393D	So-8	Dual Comparator
*MC1408-8D	SO-16	8-Bit D/A Converter
MC1458D	SO-8	Dual Op Amp
MC1488D	SO-14	Quad Line Driver
MC1489AD	SO-14	Quad Line Receiver
MC1489D	SO-14	Quad Line Receiver
MC3302D	SO-14	Quad Volt Comparator
MC3403D	SO-14	Quad Low Power Op Amp
NE4558D	SO-8	Dual Op Amp
*NE5008D	SO-16	8-Bit D/A Converter
*NE5018D	SOL-24	8-Bit D/A Converter
*NE5019D	SOL-24	8-Bit D/A Converter
*NE5036D	SO-14	6-Bit A/D Converter
NE5037D	SO-16	6-Bit A/D Converter
NE5044D	SO-16	Programmable 7-Channel Encoder
NE5045D	SO-16	7-Channel Decoder
NE5090D	SOL-16	Address Relay Driver
NE5205D	SO-8	High Frequency Amp
NE521D	SO-14	High Speed Dual Comparator
NE522D	SO-14	High Speed Dual Comparator
NE5230D	SO-8	Low Voltage Op Amp
NE527D	SO-14	High Speed Comparator
NE529D	SO-14	High Speed Comparator
NE532D	SO-8	Dual Op Amp
*NE544D	SOL-16	Servo Amp
*NE5512D	SO-8	Dual High Performance Op Amp
*NE5514D	SOL-16	Quad High Performance Op Amp
NE5517D	SO-16	Dual High Performance Amp
NE5520D	SOL-16	LVDT Signal Conditioner Circuit
*NE5532D	SOL-16	Dual Low Noise Op Amp
*NE5533D	SOL-16	Low Noise Op Amp
NE5534AD	SO-8	Low Noise Op Amp
NE5534D	SO-8	Low Noise Op Amp
*NE5537D	SO-14	Sample and Hold Amp
NE5539D	SO-14	High Frequency Wideband Amp
NE555D	SO-8	Single Timer
NE556D	SO-14	Dual Timer
NE5560D	SO-16	SMPS Control Circuit
NE5561D	SO-8	SMPS Control Circuit
NE5562D	SOL-20	SMPS Control Circuit
NE5568D	SO-8	SMPS Control Circuit

**Non-standard pinout.*
(Please check 1985 Linear Data Manual for additional pinout information.)
For information regarding additional SO products released since the publication of this document, contact your local Signetics sales office.

SO Availability

Part Number	SMD Package	Description
NE558D	SOL-16	Quad Timer
NE5592D	SO-14	Dual Video Amp
NE564D	SO-16	High Frequency Phase Locked Loop
*NE565D	SO-14	Phase Locked Loop
NE566D	SO-8	Function Generator
NE567D	SO-8	Tone Decoder Phase Locked Loop
NE571D	SOL-16	Compandor
NE572D	SOL-16	Programmable Compandor
*NE587D	SOL-20	7-Segment LED Driver (Anode)
*NE589D	SOL-20	7-Segment LED Driver (Cathode)
NE592D14	SO-14	Video Amp
NE592D8	SO-8	Video Amp
NE592HD14	SO-14	High Gain Video Amp
NE592HD8	SO-8	High Gain Video Amp
*NE594D	SOL-20	Vacuum Fluorescent Display Driver
NE602D	SO-8	Double Balanced Mixer/Oscillator
NE604D	SO-16	Low Power FM IF System
NE612D	SO-8	Double Balanced Mixer/Oscillator
NE614D	SO-16	Low Power FM IF System
PCA1122TD	VSO-40	LCD Watch Circuit
*PCD3311TD	SO-16	DTMF/Melody Generator
PCD3312TD	VSO-8	DTMF/Melody Generator
PCD3315TD	SO-28	Repertory Pulse Dialer
PCD3343TD	SO-28	Repertory Pulse Dialer
PCD3360TD	SO-16	Progressive Tone Ringer
PCD3361TD	SO-8	Progressive Tone Ringer
*PCD5101TD	SO-24	Static RAM
PCD5114TD	SO-20	4K Static RAM
PCD8571TD	SO-8	1K Serial RAM
PCF1171BTD	VSO-40	4-Digit LCD Car Clock
PCF1172BTD	VSO-40	3½-Digit Car Clock
PCF1251TD	SO-8	Micropower Voltage Detector
PCF2100TD	SO-28	LCD Duplex Driver (40)
PCF2110TD	VSO-40	LCD Duplex Driver (60)
PCF2111TD	VSO-40	LCD Duplex Driver (60)
PCF2112TD	VSO-40	LCD Duplex Driver (32)
PCF8570TD	SO-8	Static RAM (256 × 8)
PCF8573TD	SO-16	Clock/Timer
PCF8574TD	SO-16	Remote I/O Expander
PCF8576TD	VSO-56	MUX/Static Driver
PCF8577TD	VSO-40	32-/64-Segment LCD Driver
SA571D	SOL-16	Compandor
SA572D	SOL-16	Compandor
*SA594D	SOL-20	Vacuum Fluorescent Display Driver
SA602D	SO-8	Double Balanced Mixer/Oscillator
SA604D	SO-16	Low Power FM IF System
SAA1062ATD	SO-28	LCD Display Interface
SAA3004TD	SO-20	R/C Transmitter
SG3524D	SO-16	SMPS Control Circuit
TCA240DD	SO-16	Double Symmetrical Modulator/ Demodulator
TCA520DD	SO-8	Op Amp

**Non-standard pinout.*

For information regarding additional SO products released since the publication of this document, contact your local Signetics sales office.

SO Availability

Part Number	SMD Package	Description
TCA770DD	SO-14	FM IF
TDA0820TD	SO-14	Demodulator/Mixer
TDA1001BTD	SO-16	Noise Suppressor
TDA1005ATD	SO-16	Stereo Decoder
TDA7010TD	SO-16	FM Radio Circuit
TDA7020TD	SO-16	FM Radio Circuit
TDA7050TD	SO-8	Mono/Stereo Amp
TDB1080TD	SO-16	FM IF
TDD1742TD	SO-28	Frequency Synthesizer
TEA0653TD	SO-20	Dual Dolby B
TEA0665TD	SO-28	Dolby B/C Noise Reduction
TEA1010TD	SO-8	Touch Dimmer
TEA1058TD	SO-8	Touch Dimmer
ULN2003D	SO-16	Transistor Array
ULN2004D	SO-16	Transistor Array
μA723CD	SO-14	Voltage Regulator
μA741CD	SO-8	Single Op Amp
μA747CD	SO-14	Dual Op Amp

**Non-standard pinout.*

For information regarding additional SO products released since the publication of this document, contact your local Signetics sales office.

Ordering Information

FOR PREFIXES AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

ORDERING INFORMATION

Signetics' Linear LSI integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:
$1000 per order
$250 per line item per order

Military Product:
$250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that devices with a SE prefix (– 55°C to + 125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any Linear LSI product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

Table 1 PART NUMBER DESCRIPTION

PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
NE5537N	LF398	LIN	Sample & Hold Amp

NE5537N
- → Package Descriptions—See Table 2
- → Device Number
- → Device Family and Temperature Range Prefix—See Tables 3 & 4

LF398
- → Product Family { LIN Analog Products / MIL Military Products

Sample & Hold Amp
- → Description of Product Function

Table 2 PACKAGE DESCRIPTIONS

Old	New	PACKAGE DESCRIPTION
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package (SO)
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 3 SIGNETICS PREFIX AND DEVICE TEMPERATURE

PREFIX	DEVICE TEMPERATURE RANGE
N	0° to + 70°C
S	– 55° to + 125°C
NE	0° to + 70°C
SE	– 55° to + 125°C
SA	– 40° to + 85°C

Table 4 INDUSTRY STANDARD PREFIX

PREFIX	DEVICE FAMILY
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LF	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
ULN	Linear Industry Standard

Ordering Information

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

ORDERING INFORMATION

Signetics integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors.

Minimum Factory Order:

Commercial Product:
- $1000 per order
- $250 per line item per order

Table 1 provides part number information concerning Signetics Europroducts integrated circuits.

Table 2 provides package suffixes and descriptions for all presently existing types. Letters following the device number not used in Table 2 are considered to be part of the device number.

Table 3 provides explanations on the various prefixes employed in the part number descriptions. As noted in Table 3, Signetics Europroducts device operating temperature is defined by the appropriate prefix.

OPERATING TEMPERATURE:

The letters A to G give information about the operating temperature:

- A: Temperature range not specified. See data sheet.
  e.g.: TDA2541N
- B: 0 to +70°C
  e.g.: PCB8573PN
- C: −55 to +125°C
  e.g.: PCC2111PN
- D: −25 to +70°C
  e.g.: PCD8571PN
- E: −25 to +85°C
  e.g.: PCE2111PN
- F: −40 to +85°C
  e.g.: PCF2111PN
- G: −55 to +85°C
  e.g.: PCG2111PN

Table 1. PART NUMBER DESCRIPTION

Part Number	Cross Ref. Part No.	Product Family	Product Description
TDA2541N		LIN	Video I.F. Amplifier

TDA2541N
- LIN → Product Family Linear LSI
- Video I.F. Amplifier → Description of Product Function
- TDA2541N → Package Description — See Table 2
- TDA2541N → Device Number
- TDA2541N → Device Family and Temperature Range Prefix — See Tables 3 & 4

Table 2. PACKAGE DESCRIPTION

Suffix	Package Description
N	8,14,16,18,20,24,28,40 — lead plastic DIL
D	Microminiature Package (S.O.)
F	14,16,18,22,24 — lead ceramic DIL
U	Single-in-line plastic (SIL) and SIL power
H	Metal Can

Table 3. DEVICE PREFIX AND TEMPERATURE*

Prefix	Device Family
OM	Linear circuit
MAB,MAF	Microcomputer
MEA	Microcomputer peripheral
PCx	CMOS Circuit
PNx	NMOS Circuit
SAx	Digital circuit
TAx	Linear circuit
TBx	Linear circuit
TCx	Linear circuit
TDx	Linear circuit
TEx	Linear circuit

*NOTE:
The third letter of the prefix, in a three letter prefix, is the temperature designator.

Signetics

Quality and Reliability
Section 2

2

Linear Products

Quality and Reliability

SIGNETICS LINEAR QUALITY

Signetics has put together a winning process for manufacturing linear circuits. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The circuits produced in the Linear Division must meet rigid criteria as defined by our design rules and as evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 5 x 10(fifth) amps/cm(sq). Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 - QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. Samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One-hundred devices from each generic family are subjected to each of the following stresses every four weeks:

- **High Temperature Operating Life: T_J = 150°C, 1000 hours, static biased operation.**
- **High Temperature Storage: T_J = 150°C, 1000 hours**
- **Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static biased**

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 72 hours of pressure pot (20psig, 127°C, 100% saturated steam) and 300 cycles of thermal shock (–65°C to +150°C)

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

Quality and Reliability

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the Linear SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors.
- Device or generic group failure rate studies.
- Advanced environmental stress development.
- Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in some evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits which are derived from quality products can be summed up in the words, *lower cost of ownership.*

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals, inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction for achieving a high level of quality. Special programs are targeted on specific quality issues. For example, in 1978 a program to reduce electrically defective units for a major automotive manufacturer improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100PPM (parts per million), down from an industry practice of 10,000PPM, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees, from the R and D laboratory to the shipping dock. In short, from a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality (see Figure 1).

At Signetics, quality means more than working circuits. It means on-time delivery of the right product at the agreed upon price (see Figure 2).

ONGOING QUALITY PROGRAM

The Signetics quality improvement program steers its employees toward "Doing it Right the First Time." The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by all technical and administrative functions equally.

This program extends into every area of the company, and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

QUALITY COLLEGE

Almost continuously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" – ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

Quality and Reliability

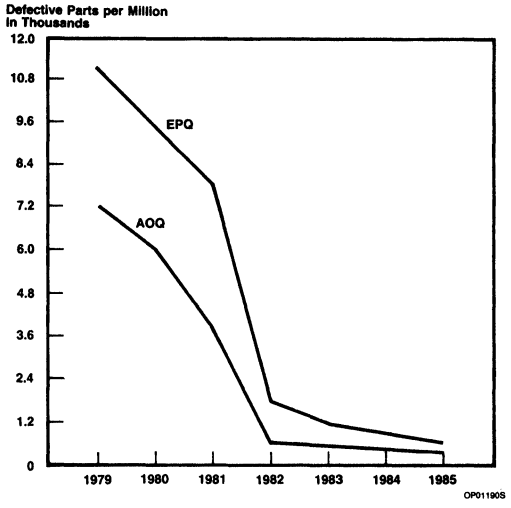


Figure 1. Signetics' Quality Progress – Estimated Process Quality and Average Outgoing Quality

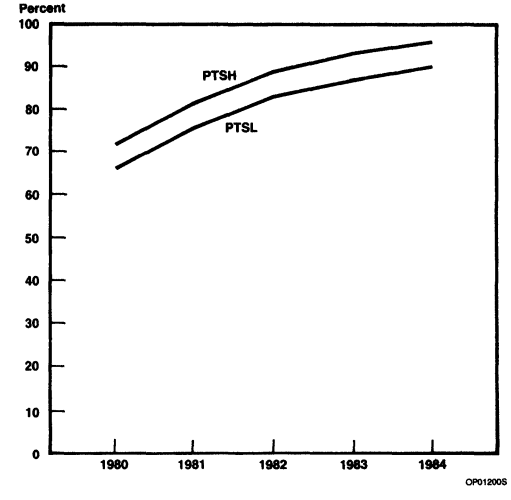


Figure 2. Performance To Schedule/On-Time Delivery – High and Low

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

PRODUCT QUALITY PROGRAM

To reduce defects in outgoing products, we created the Product Quality Program. This is managed by the Product Engineering Council, composed of the top product engineering and test professionals in the company. This group:

1. sets aggressive product quality improvement goals;
2. provides corporate-level visibility and focus on problem areas;
3. serves as a corporate resource for any group requiring assistance in quality improvement; and
4. drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent. Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated.

Higher incoming quality material to us ensures higher outgoing quality products.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities – failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will

Quality and Reliability

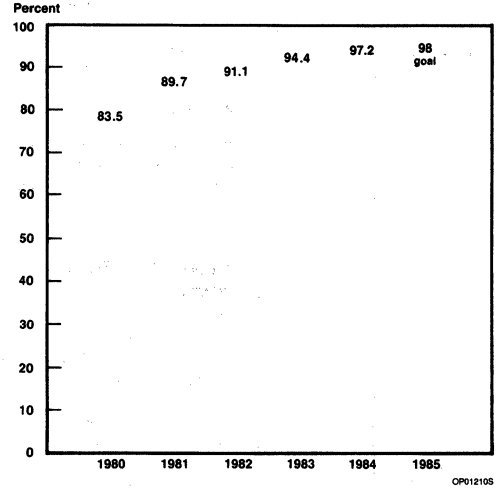


Figure 3. Lot Acceptance Rate From Signetics Vendors

MATERIAL WAIVERS
1985 – (0) (Goal)
1984 – 0
1983 – 0
1982 – 2
1981 – 134

establish continuity and build confidence levels.

- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

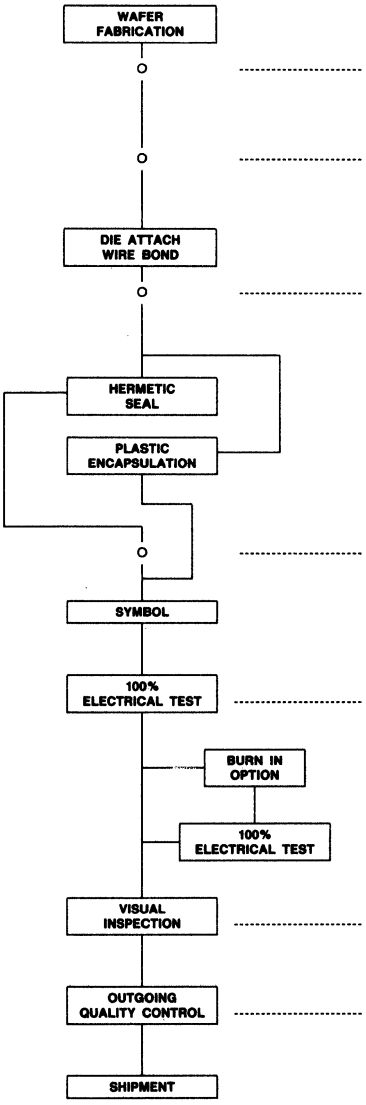
This team work with you will allow us to achieve our mutual goal of improved product quality.

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time," a key concept of the quality improvement program. During the development of the program many profound changes were made. Figure 4, *Linear Flow*, shows the results.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading Quality supplier of linear circuits. These achievements have also led to our participation in many Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

Quality and Reliability



SCANNING ELECTRON MICROSCOPE CONTROL

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

PRE-SEAL VISUAL ACCEPTANCE

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

SEAL TESTS

Hermetic package seal integrity is ensured by fine 100% gross leak testing.

SYMBOL

Devices are marked with the Signetics logo, device number and date code or custom symbol per individual specification requirements.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested to all data sheet parameters guaranteeing temperature specifications.

BURN IN (SUPR II LEVEL B OPTION)

Devices are burned in for 21 hours at 155°C maximum Junction Temperature.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested to all data sheet parameters guaranteeing temperature specifications.

VISUAL

All products are 100% visually inspected per the requirements specified in Signetics' or customer documents.

FINAL QUALITY ASSURANCE GATE

The final QA inspection step guarantees the specified mechanical and electrical AQL's. Every shipment is sealed and identified by QA personnel.

Figure 4. Linear Division Linear Process Flow

Quality and Reliability

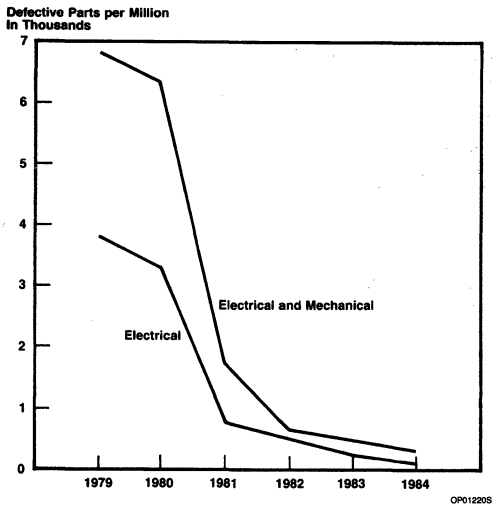


Figure 5. Linear AOQ Average Outgoing Quality

Signetics

Military
Section 3

Linear Products

Military Errata

Effective January 1, 1985, this section has been superseded by the 1985 Military Products Data Manual. Information regarding this manual can be obtained from the Military Division in Sacramento. (916) 925-6700.
Electrical specification herein as described for products with the "SE" prefix do not necessarily describe the performance characterization of military processed products.

Signetics

Interface Products
Section 4

Linear Products

D/A and A/D Converter—Symbols and Definitions

Absolute Accuracy Error

Absolute Accuracy Error is the difference between the theoretical analog input required to produce a given output code and the actual analog input required to produce the same code. The actual input is a range and the error is the midpoint of the measured band and the theoretical band.

Absolute Maximum Ratings

The Absolute Maximum Ratings are the operating safe zones. Exceeding these limits could cause permanent damage to the device. The device is NOT guaranteed to operate at these limits.

Conversion Speed

Conversion Speed is the speed at which a converter can make repetitive conversions.

Conversion Time

Conversion time is the time required for a complete conversion cycle of an ADC. Conversion time is a function of the number of bits and the clock frequency.

Differential Non-Linearity (DNL)

Differential Non-Linearity of a DAC is the deviation of the measured output step size from the ideal step size. In an ADC it is the deviation in the range of inputs from 1 LSB that causes the output to change from one given code to the next code. Excessive DNL gives rise to non-monotonic behavior in a DAC and missing codes in an ADC.

Differential Non-Linearity Tempco

Differential Non-Linearity Tempco is the temperature coefficient of DNL and specifies how DNL changes with temperature.

Full Scale Tempco

Full Scale Tempco in a DAC is the change of full scale output with a change of temperature. In an ADC it is the change in the input required to cause full scale transistion. Expressed in ppm/degree C.

Gain Error

Gain Error is the error of the slope of the line drawn through the midpoints of the steps of the transfer function as compared to the ideal slope. It is usually measured by determining the error of the analog input voltage to cause a full scale output word with the ideal value that should cause this full scale output. This gain error is usually expressed in LSB or in percent of full scale range.

Hysteresis Error

Hysteresis Error is the code transition voltage dependence relative to the direction from which the transistion is approached.

Integral Non-Linearity

Integral Non-Linearity is the difference between the ideal transfer characteristic and the actual characteristic.

Least Significant Bit (LSB)

The Least Significant Bit is the lowest order bit, or the bit with the least weight.

Missing Code

A Missing Code is a code combination that does not appear in the ADC's output range.

Monotonicity

A DAC is monotonic if its output either increases or remains the same when the input code is incremented from any code to the next higher code.

Most Significant Bit (MSB)

The Most Significant Bit is the highest order bit, or the one with the most weight.

Offset Error

Offset error is the constant error or shift from the ideal transfer characteristic of a converter. In a DAC it is the output obtained when that output should be zero. In an ADC it is the difference between the input level that causes the first code transistion and what that input level should be.

Output Voltage Compliance

Output Voltage Compliance of a current output DAC is the range of acceptable voltages at the DAC output for the DAC output current to remain within its specified limits.

Power Supply Sensitivity

Power Supply Sensitivity of a DAC is the change of output current or voltage with changes in the power supply voltage. In an ADC, it is the change in the transistion points from code to code with changes in the power supply voltage.

Quantizing Error

In an A/D converter there is an infinite number of possible input levels, but only 2^n output codes (n = number of bits). There will, therefore, be an error in the output code that could be as great as ½ LSB because of this quantizing effect. The greatest error occurs at the transistion point where the output state changes.

Relative Accuracy

Relative Accuracy is a measure of the difference of the theoretical output value with a given input after any offset and gain errors have been nulled out.

Resolution

Resolution is the number of bits at the input or output of an ADC or DAC. It is the number of discrete steps or states at the output and is equal to 2^n where in is the resolution of the converter. However, n bits of resolution does not guarantee n bits of accuracy.

Setting Time

Setting Time is the delay in a DAC from the 50 percent point on the change in the input digital code to the effected change in the output signal. It is expressed in terms of how long it takes the output to settle to and remain within a certain error band around the final value and is usually specific for full scale range changes.

Transfer Characteristic

The Transfer Characteristic is the relationship of the output to the input.

NOTE:
Refer to Section 9 (Interface Circuits) for an in-depth explanation of data converters and their applications.

Converter Selector Guides

D/A CONVERTERS

DEVICE	BITS	ACC. %	CONV. SPEED (μs)	OUTPUT		INT. REF.	INT. LATCH	PACKAGE			TEMPERATURE RANGE		COMMENTS
				V	I			N	D	F	Com'l.	Mil	
MC1408-7	8	0.39	0.07		X			X		X			
MC1408-8	8	0.19	0.07		X			X	X	X	X		
MC1508-8	8	0.19	0.07		X					X		X	
DAC08	8	0.19	0.07		X					X		X	
DAC08A	8	0.10	0.07		X					X		X	
DAC08C	8	0.39	0.07		X			X		X	X		
DAC08E	8	0.19	0.07		X			X	X	X	X		
DAC08H	8	0.10	0.07		X			X		X	X		
NE5018	8	0.19	0.2	X		X	X	X		X	X		
SE5018	8	0.19	0.2	X		X	X			X		X	
NE5019	8	0.10	0.2	X		X	X	X		X	X		
SE5019	8	0.10	0.2	X		X	X			X			
NE5118	8	0.19	2.3		X	X	X	X		X	X		
SE5118	8	0.19	2.3		X	X	X			X		X	
NE5119	8	0.10	2.3		X	X	X	X		X	X		
SE5119	8	0.10	2.3		X	X	X			X		X	
NE5020	10	0.10	5.0	X		X	X	X		X	X		
NE5410	10	0.05	0.25		X					X	X		±¼ LSB DNL
SE5410	10	0.05	0.25		X					X		X	±¼ LSB DNL
MC3410	10	0.05	0.25		X					X	X		±½ LSB DNL
MC3510	10	0.05	0.25		X					X		X	±½ LSB DNL
AM6012	12	0.05	0.25		X					X	X		±1 LSB DNL
TDA1540D	14	0.012	0.5		X	X	X			X	X		Serial Input ±½ LSB DNL

A/D CONVERTERS

DEVICE	BITS	ACC.%	CONV. SPEED (μs)	INPUT		THREE-STATE OUTPUT	INT. REF.	INT. CLOCK	PACKAGE			TEMPERATURE RANGE	
				V	I				N	F	FE	Com'l.	Mil
NE5034	8	0.19	17		X	X		X		X		X	
NE5036	6	0.78	23	X		X			X		X	X	
NE5037	6	0.78	9	X		X			X	X		X	
TDA1534	14	0.012	8.5		X		X	X	X			X	
ADC0801-1	8	0.10	73	X		X		X		X		X[1]	
ADC0802-1	8	0.19	73	X		X		X		X		X[1]	
ADC0803-1	8	0.19	73	X		X		X		X		X[1]	
ADC0804-1	8	0.39	73	X		X		X		X		X[1]	
ADC0805-1	8	0.39	73	X		X	X	X		X		X[1]	

Note:

1. **Automotive temperature range: – 40 to + 85°C**

10-Bit High Speed Microprocessor-Compatible Analog to Digital Converter

SE/NE5030

DESCRIPTION

The SE/NE5030 is a monolithic 10-bit, microprocessor compatible Analog-to-Digital Converter which is manufactured on a high speed bipolar process using thin film resistors. The conversion process is a new multi-step technique which combines parallel conversion and successive approximation, allowing complete 10-bit conversion in just 2.5 microseconds at the maximum 3MHz clock rate. The fast conversion rate makes the SE/NE5030 excellent for a wide range of applications where system throughput sampling rates up to 360KHz are required.

FEATURES

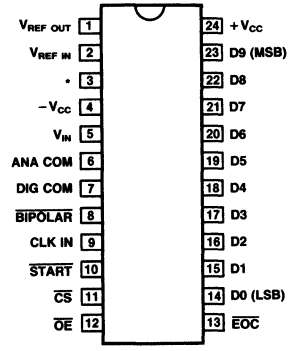
- **Microprocessor compatible**
- **Fast conversion (2.5μsec)**
- **Relative accuracy 1/4 LSB typical**
- **2.5 volt signal input range**
- **Accomodates either unipolar or bipolar input**
- **TTL compatible digital inputs/outputs**
- **No missing codes over temp range**
- **Three state outputs**
- **High impedance analog input**
- **Low TC internal reference (5ppm/°C typical)**

APPLICATIONS

- **Process control**
- **Test and measurement**
- **Machine tools**
- **Robotics**
- **Industrial monitoring**
- **High speed waveform digitizing**
- **High speed correlators**

PIN CONFIGURATION

F PACKAGE



TOP VIEW

CD01281S

* Make no external connection

ORDER NUMBERS
NE5030F, SE5030F

PIN #	DESIGNATION	FUNCTION
1	$V_{REF\ OUT}$	2.5V reference output voltage of the temperature compensated internal reference.
2	$V_{REF\ IN}$	Reference input for the converter. (Connect pin 1 to pin 2 or connect an external 2.500V reference voltage to pin 2.)
3		Make no external connection.
4	V_{EE}	-5V (±5%) negative supply pin.
5	V_{IN}	Analog input voltage. Unipolar range 0V to $+V_{REF}$ Bipolar range $-V_{REF}/2$ to $+V_{REF}/2$
6	ANA COM	Analog common point to which all Analog signals are to be referenced.
7	DIG COM	Digital common point to which all digital signals are to be referenced.
8	$\overline{BIPOLAR}$	Logic input for selecting either unipolar or bipolar mode of operation. Logic high selects unipolar mode Logic low selects bipolar mode
9	CLOCK	Single phase clock signal input
10	$\overline{START}$	Start signal input. Low-going edge initiates a conversion cycle.
11	$\overline{CS}$	Chip Select. Must be low to enable conversion or read output data. Logic low causes normal operation (enables operation) Logic high inhibits conversion and holds output data lines in high impedance mode
12	$\overline{OE}$	Output enable. Logic low when $\overline{CS}$ is low enables output buffers Logic high puts outputs into the high impedance state
13	$\overline{EOC}$	End of Conversion output signal. This output voltage goes low after the end of a conversion. This output voltage is reset to a logic high by a low level on the $\overline{OE}$ pin.
14-23	D0 - D9	Three-state buffer outputs (D9 is MSB, D0 is LSB). When $\overline{OE}$ is low, the converted data word is available at these pins.
24	V_{CC}	+5V (±5%) positive supply voltage pin.

4

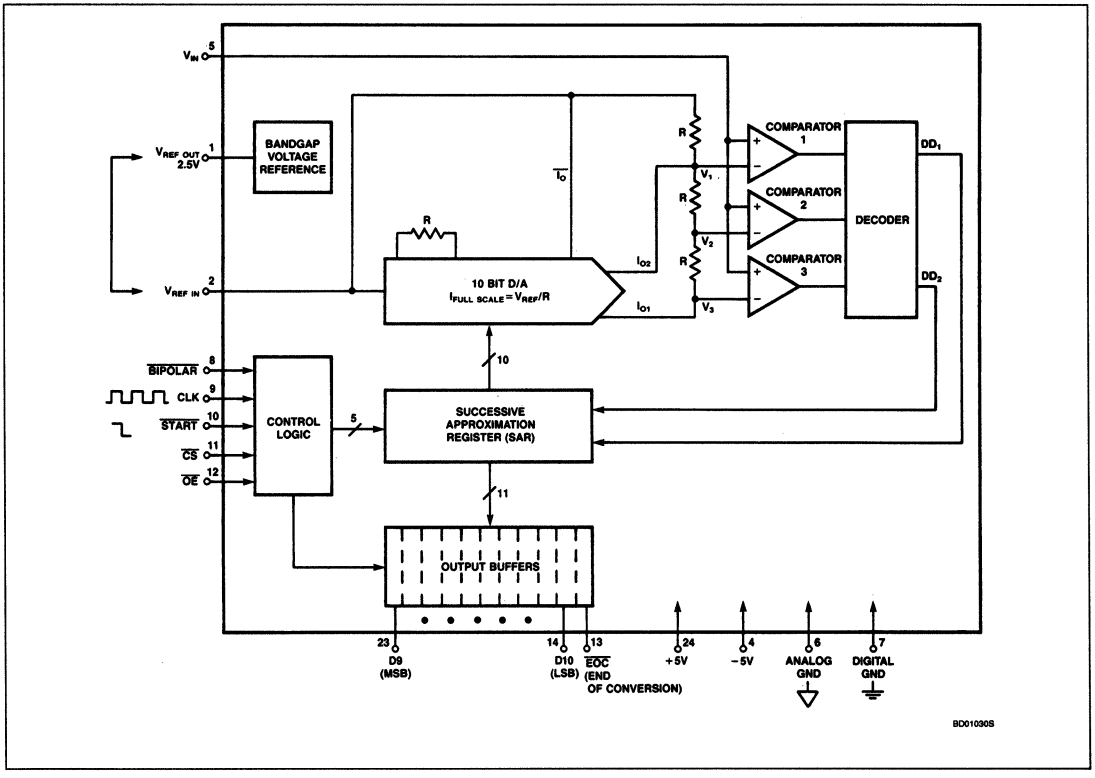
10-Bit High Speed Microprocessor-Compatible Analog to Digital Converter

SE/NE5030

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage	+8	V
Negative supply voltage	−8	V
Analog input range	±3.5	V
Digital input voltage	−0.5 to V_{CC}	V
Analog common to digital common	±1	V
$V_{REF\ OUT}$ short circuit to common	Indefinite	
$V_{REF\ OUT}$ short circuit to V_{CC}	60	seconds
$V_{REF\ IN}$ applied voltage	0 to 5	V
Digital output pins applied voltage to logic high outputs	−0.5 to V_{CC}	V
Digital output sink current	10	mA
Operating temperature range NE5030 SE5030	 0 to +70 −55 to +125	 °C °C
Storage temperature range	−60 to +150	°C
Power dissipation	600	mW

BLOCK DIAGRAM



10-Bit High Speed Microprocessor-Compatible Analog to Digital Converter

SE/NE5030

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V, V_{EE} = −5V, T_A = 0 to 70°C for NE5030, T_A = −55 to +125°C for SE5030, F_{CLK} ≤ 3MHz, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Resolution		10	10	10	Bits
	Relative accuracy error[1, 2]			±1/4	±1/2	LSB
DNL	Differential linearity error[3]				10	bits
	Code width error			±1/4	±1/2	LSB
E_{FS}	Full scale gain error	T_A = 25°C over operating temp range		±1 ±1	±2 ±5	LSB LSB
E_{UOS}	Unipolar offset error	T_A = 25°C over operating temp range			±0.5 ±1.0	LSB LSB
E_{BOS}	Bipolar offset error	T_A = 25°C over operating temp range			±0.5 ±1.0	LSB LSB
	Analog input range Unipolar Bipolar	 $\overline{BIPOLAR}$ = 2.0V $\overline{BIPOLAR}$ = 0.8V	 0 − $V_{REF}/2$		 + V_{REF} + $V_{REF}/2$	 V V
I_B	Analog input bias current			1	5	μA
Z_{IN}	Analog input impedance		1	3		Megohms
V_{REF}	Reference voltage output	T_A = 25°C	2.495	2.500	2.505	V
TC_{REF}	Reference voltage drift[4]	over operating temp range		±1.25 (±5)	±2.5 (±10)	mV (ppm/°C)
$I_{L\ (REF)}$	Reference external load		2	2.5		mA
$I_{REF\ IN}$	Reference input current	$V_{REF\ IN}$ = 2.5V		2	3	mA
V_{CC}	Pos supply operating range		4.75	5	5.25	V
V_{EE}	Neg supply operating range		−4.75	−5	−5.25	V
P_{SR}	Power supply rejection[5]	V_{CC} = 4.75 to 5.25V V_{EE} = −4.75 to −5.25V			±0.25	LSB
I_{CC}	Positive supply current	V_{CC} = 5.25V, V_{EE} = −5.25V		36	45	mA
I_{EE}	Negative supply current	V_{CC} = 5.25V, V_{EE} = −5.25V		50	60	mA
Logic inputs						
V_{IH}	Logic 1 input voltage		2.0			V
V_{IL}	Logic 0 input voltage				0.8	V
I_{IH}	Logic 1 input current	V_{IH} = 2.4V, T_A = 25°C V_{IH} = 2.4V, over operating temp range			10 20	μA μA
I_{IL}	Logic 0 input current	V_{IL} = 0.4V, T_A = 25°C V_{IL} = 0.4V, over operating temp range			200 400	μA μA
Logic outputs						
V_{OH}	Logic 1 output voltage	I_{OH} = −400μA, $\overline{CS}$ = $\overline{OE}$ = 0.8V	2.4	3.2		V
V_{OL}	Logic 0 output voltage	I_{OL} = 1.6mA, $\overline{CS}$ = $\overline{OE}$ = 0.8V		0.2	0.4	V
I_{OZ}	Three-state leakage	$\overline{OE}$ = 2.0V, V_{OL} = 0V or 5V, T_A = 25°C $\overline{OE}$ = 2.0V, V_{OL} = 0V or 5V, over temp		±10	±20 ±100	μA μA

NOTES:
1. Specifications given in LSB refer to the weight of the least significant bit at the 10-bit level, which is 0.1% of the full scale voltage.
2. Relative accuracy is defined as the deviation of the actual code transition points from a straight line drawn between the first code transition point and the final code transition point.
3. Resolution for which the device is guaranteed to have no missing codes.
4. Deviation of the reference voltage output over the operating temperature range from its 25°C value.
5. Maximum change in the final code transition point. This will also result in a linear change in all lower order codes.

10-Bit High Speed Microprocessor-Compatible Analog to Digital Converter

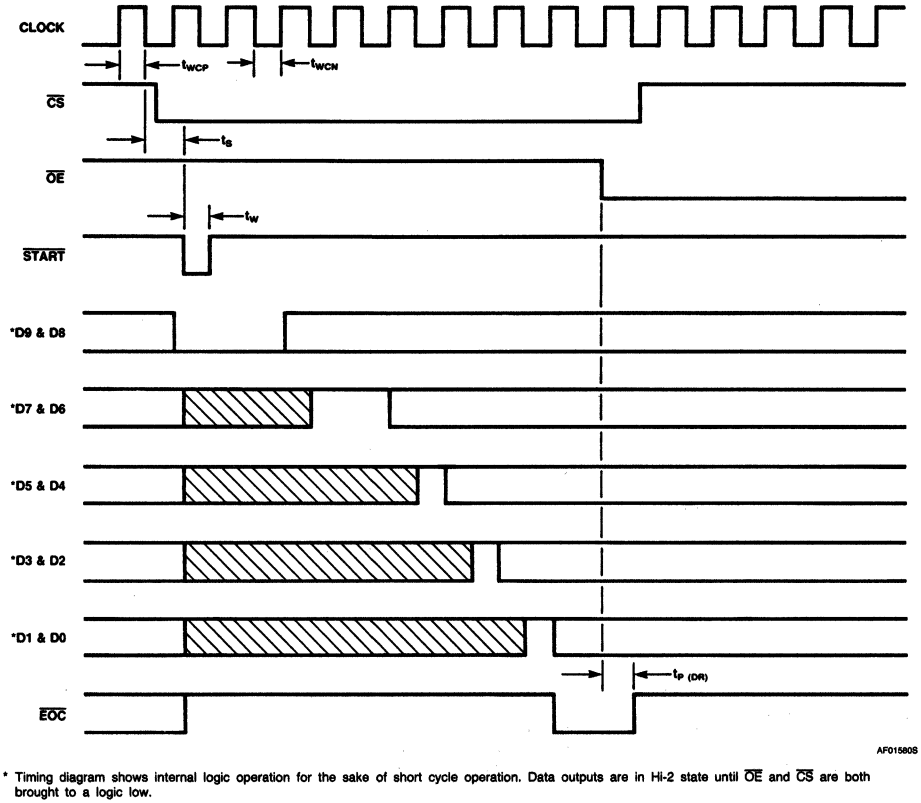
SE/NE5030

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V, V_{EE} = −5V, T_A = 25°C, F_{CLK} = 5MHz

	PARAMETER	TO	FROM	EDGE		MIN	TYP	MAX	UNITS
F_{CLK}	Max clock frequency					3.0[1]	4.0		MHz
t_{WCP}	Pos clk pulse width					90			nS
t_{WCN}	Neg clk pulse width					90			nS
t_{CONV}	Conversion time						$7.5/F_{CLK}$ [2]		nS
t_W	START pulse width					100			nS
t_S	Set-up time	CLK	$\overline{START}$	HI-LOW		tbd	tbd		nS
$t_{P\ (DATA)}$	Access time	DB0-DB9	$\overline{OE}$	HI-LOW			tbd	tbd	nS
$t_{P\ (3\text{-}STATE)}$	Disable time	hi-Z	$\overline{OE}$	LOW-HI			tbd	tbd	nS
$t_{P\ (EDC)}$	Propagation delay	$\overline{EOC}$ hi	$\overline{OE}$	HI-LOW			tbd	tbd	nS

NOTES:
1. Maximum clock frequency. Subject to change before product release.
2. Frequency in MHz.

TIMING DIAGRAM



* Timing diagram shows internal logic operation for the sake of short cycle operation. Data outputs are in Hi-2 state until $\overline{OE}$ and $\overline{CS}$ are both brought to a logic low.

10-Bit High Speed Microprocessor-Compatible Analog to Digital Converter

SE/NE5030

CIRCUIT DESCRIPTION

The SE/NE5030 is a microprocessor compatible, high speed, 10-bit Analog-to-Digital converter. The device uses a new multi-step parallel conversion scheme[1] which determines two bits of the digital word in each conversion step, permitting a fast 2.5 microsecond conversion time.

Refer to the block diagram. The fullscale current of the DAC is V_{REF}/R. When conversion is initiated, the successive approximation register (SAR) directs the two MSB currents of the DAC (I9 and I8) to $\overline{Io}$ and the remaining bit currents of the DAC (including the DAC R/2R termination current) to Io1. This divides the input signal range into four equal subranges. The three latched comparators determine into which of these subranges the input voltage falls. The decoded outputs of these comparators determine the two MSBs (D9 and D8), which are stored in the SAR.

In each subsequent step, the SAR controls the DAC such that the complement of the previously determined bits are directed through Io2; the bits currently being determined are directed through $\overline{Io}$, and the remainder of the bits are directed through Io1. In this manner the subrange containing the analog input voltage in the previous step is divided into four smaller subranges and two bits of the digital output are determined. At the end of five steps the SAR contains a 10-bit binary code which accurately represents the input signal to within ±1/2 LSB.

FUNCTIONAL DESCRIPTION

With an external clock signal connected to the CLOCK IN pin, $\overline{CS}$ at a logic low, and $\overline{OE}$ at a logic high, a conversion cycle is initiated with the application of an external start pulse applied to the $\overline{START}$ pin. The SAR sequences through the conversion as described above. At the end of the conversion, the end-of-conversion flag ($\overline{EOC}$) goes low. The $\overline{EOC}$ flag can be used to interrupt a microprocessor or otherwise notify a processor or controller that a conversion is completed. $\overline{OE}$ may then be forced low (while holding $\overline{CS}$ low), enabling the three-state output buffers so that the converted word may be read. Bringing the $\overline{OE}$ pin low while the $\overline{CS}$ pin is low also resets the $\overline{EOC}$ flag to a logic high. It is recommended that $\overline{OE}$ be brought to a logic high prior to the application of another $\overline{START}$ pulse. If $\overline{OE}$ were to remain low during a conversion, the output buffers would be enabled and would switch states during the conversion. This switching can couple into the analog input through parasitic capacitances, causing erroneous conversion results.

The application of another START pulse while a conversion is in progress will halt the conversion in progress and begin a new conversion cycle. If a $\overline{START}$ pulse is received while the $\overline{CS}$ input is at a logic high, that $\overline{START}$ pulse is ignored. The outputs will be in the high impedance state as long as either $\overline{CS}$ or the $\overline{OE}$ input is at a logic high.

LOGIC INPUTS AND OUTPUTS

All the logic inputs ($\overline{BIPOLAR}$, CLOCK IN, $\overline{START}$, $\overline{CS}$, $\overline{OE}$) respond to TTL level signals and present one LS TTL load to the driving source. The logic outputs are capable of driving two TTL loads. If long digital lines or a heavily loaded bus must be driven, external logic buffers are recommended.

VOLTAGE REFERENCE

The internal voltage reference (2.5V ± 0.2%) is of a second order-corrected design. The output voltage is trimmed at the wafer level by the "Zener zap" technique to have a temperature coefficient of less than ± 10 ppm/°C (average) over the operating temperature range. $V_{REF\ OUT}$ (pin 1) and $V_{REF\ OUT}$ (pin 2) are not internally connected and should be connected together close to the device. The voltage reference output (pin 1) can provide up to 2mA to an external load for other system applications. The current drawn by any external load *must remain constant* during a conversion.

ANALOG INPUT

The analog input voltage to ge digitized is connected between V_{IN} (pin 5) and Analog Common (pin 6). The device operates in either a unipolar mode (input range of 0 to V_{REF}) or in a bipolar mode (input range of $-V_{REF}/2$ to $+V_{REF}/2$). The TTL compatible $\overline{BIPOLAR}$ input is used to select the mode.

When the $\overline{BIPOLAR}$ input is high, the device operates in the unipolar mode. The input range is then 0 to $+V_{REF}$ (2.5V nominal). The nominal value of the LSB is 2.44mV. The SE/NE5030 is designed to have a 1/2 LSB offset so that the analog input exactly corresponding to a given code will fall in the center of that code's input range. Thus, the ideal input voltage to cause the first transition (from 00 0000 0000 to 00 0000 0001) will occur for an input voltage of 1.22mV, and the final transition (from 11 1111 1110 to 11 1111 1111) will ideally occur for an input voltage of 2496.34mV, or 1.5 LSB below the 2.5V reference.

For bipolar operation, the $\overline{BIPOLAR}$ input is set to a logic low. This shifts the transfer curve of the A/D by $V_{REF}/2$ so that the input voltage range is now $-(V_{REF}/2)$ to $+(V_{REF}/2)$, or (−1.25V to +1.25V nominal). The ideal transition of code from 00 0000 0000 to 00 0000 0001 occurs at an input of −1248.78mV, and the final code transition (11 1111 1110 to 11 1111 1111 occurs at 1246.34mV.

The high input impedance of the SE/NE5030 analog input simplifies the requirements of the signal source driving the SE/NE5030, eliminating the need for specialized drive circuitry.

POWER SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

Since one LSB of the SE/NE5030 input is just 2.44mV, good layout and grounding techniques are crucial to attaining optimum performance.

The power supplies should be filtered, well regulated, and free of high frequency noise. Use of noisy supplies will cause unstable output codes to be generated. The power supplies should be bypassed to Analog Common with tantalum or electrolytic capacitors in parallel with a small, high frequency bypass. Suitable bypasses would be 22μF electrolytic capacitors with 0.1μF ceramic capacitors in parallel with them. These capacitors should be located close to the device.

Analog Common and Digital Common are not connected internally and should be connected together as close to the device as possible. Low impedance analog and digital common returns are important for optimum performance. The power supply returns should be connected to the Digital Common of the device. The Analog Common is the ground reference point for the internal voltage and should be connected directly to the Analog Common reference point of the system.

Coupling between the digital lines and the Analog Input should be minimized by careful printed circuit board layout. The layout should attempt to locate the analog circuitry and their interconnections as far from the logic circuitry as is possible. Use of wire wrap techniques or plug-in type boards is not recommended.

NOTE:

1. M. Kolluri: "A Multi-Step Parallel 10-Bit 1.5μSec ADC," *ISSCC Digest of Technical Papers* , p 60 – 61; Feb 1984.

4

8-Bit A/D and D/A Converter — PCF8591

DESCRIPTION

The PCF8591 is a single chip, single supply, low power 8-bit CMOS data acquisition device. It contains an 8-bit successive approximation analog to digital converter, a four channel analog multiplexer and a digital to analog converter. The four analog inputs can be programmed as two differential inputs or four single-ended inputs. PCF8591 has a serial I^2C interface which allows for a maximum bus frequency of 100K bits per second.

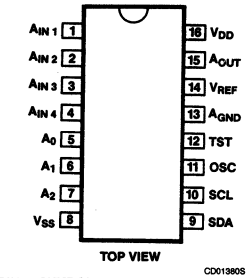
FEATURES

- **Single power supply**
- **Operating voltage 2.5V to 6V**
- **Low power consumption**
- **Serial I^2C bus**
- **Four analog inputs programmable as two differential or four single-ended**
- **On-chip sample and hold**

APPLICATIONS

- **Control systems**
- **Low power converter for remote data acquisition**
- **Automotive**
- **Audio and T.V.**

PIN CONFIGURATION



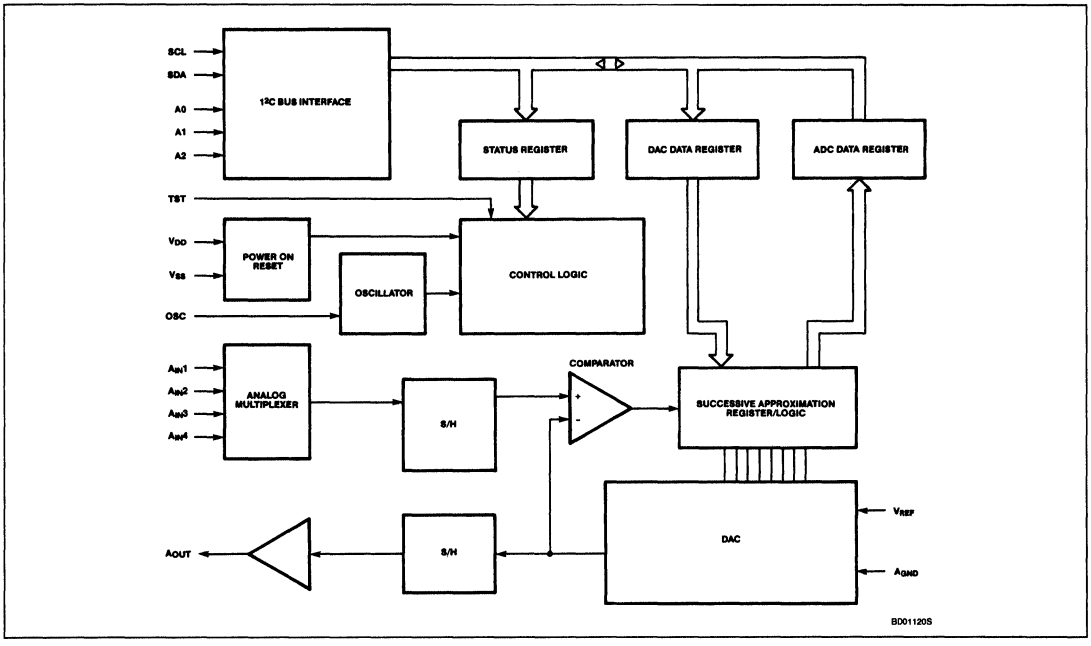
TOP VIEW

CD01380S

PIN	SYMBOL	FUNCTION
1	A_{IN} 1	Analog input (A/D converter)
2	A_{IN} 2	Analog input (A/D converter)
3	A_{IN} 3	Analog input (A/D converter)
4	A_{IN} 4	Analog input (A/D converter)
5	A_0	Hardware address pin
6	A_1	Hardware address pin
7	A_2	Hardware address pin
8	V_{SS}	Negative supply
9	SDA	I^2C Bus data line
10	SCL	I^2C Bus clock line
11	OSC	Oscillator
12	TST	Testpin
13	A_{GND}	Analog ground (reference ground)
14	V_{REF}	Reference voltage
15	A_{OUT}	Analog output (D/A converter)
16	V_{DD}	Positive supply

8-BIT A/D And D/A Converter PCF8591

BLOCK DIAGRAM



For additional information, consult the Applications Section.

7-Bit Analog to Digital Converter (ADC 7) PNA7507

GENERAL DESCRIPTION

The PNA7507 is a monolithic NMOS 7-bit analogue-to-digital converter (ADC) designed for video applications. The device converts the analogue input signal into 7-bit binary coded digital words at a sampling rate of 15 MHz.

The circuit comprises 129 comparators, a reference resistor chain, transcoder stages, and TTL output buffers which are positive edge triggered. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

- 7-bit resolution
- Digitizing rates up to 15 MHz
- No external sample and hold required
- High input impedance
- Binary or two's complement TTL outputs
- Overflow and underflow outputs
- Low reference current (200 μA typ.)
- Positive supply voltages (+ 5 V/+ 12 V)
- Low power consumption (350 mW typ.)
- Standard 24 pin package

Applications

- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

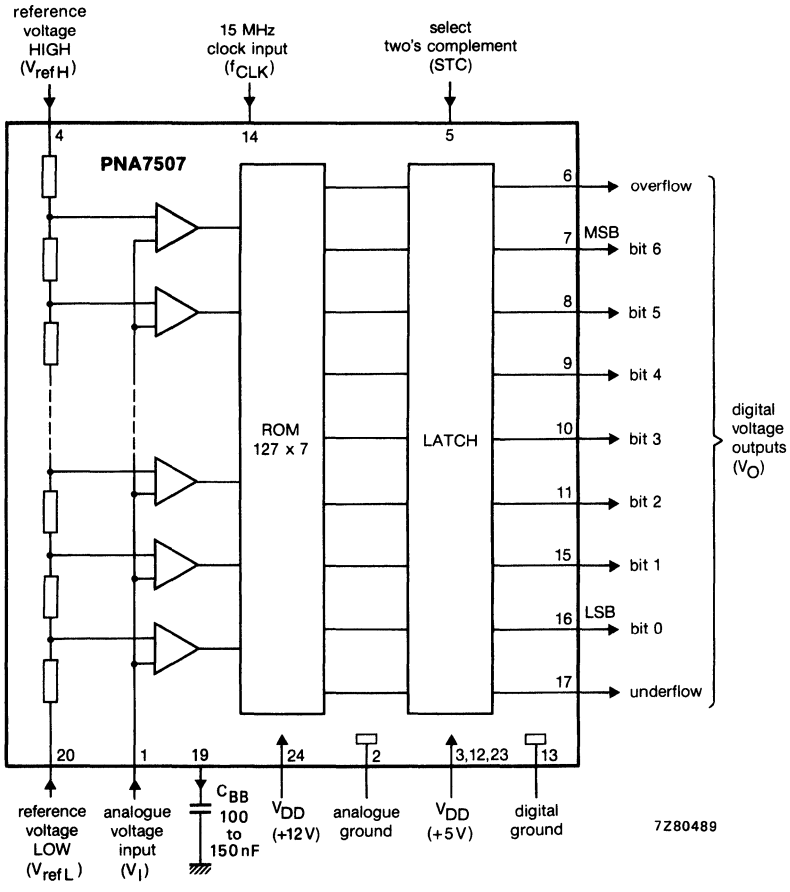
QUICK REFERENCE DATA

Supply voltage range (pins 3, 12, 23)	V_{DD}	4,75 to 5,25	V
Supply voltage range (pin 24)	V_{DD}	11,4 to 12,6	V
Supply current (pins 3, 12, 23)	I_{DD}	typ. 40	mA
Supply current (pin 24)	I_{DD}	typ. 12	mA
Reference voltage LOW (pin 20)	V_{refL}	min. 2,4	V
Reference voltage HIGH (pin 4)	V_{refH}	max. 5,2	V
Linearity (± 0,4% full scale)		± ½	LSB
Bandwidth (−3 dB)	B	min. 6	MHz
Clock frequency	f_{CLK}	max. 15	MHz
Total power dissipation	P_{tot}	typ. 350	mW

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

7-Bit Analog to Digital Converter (ADC 7) PNA7507



Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Fig. 1 Block diagram.

7-Bit Analog to Digital Converter (ADC 7) — PNA7507

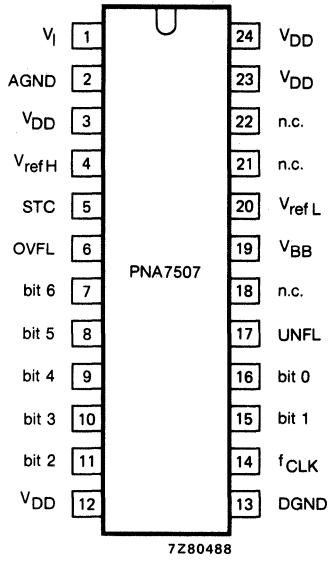


Fig. 2 Pinning diagram.

PINNING

1	V_I	analogue voltage input
2	AGND	analogue ground
3	V_{DD}	positive supply voltage (+ 5 V)
4	V_{refH}	reference voltage HIGH
5	STC	select two's complement
6	OVFL	overflow
7	bit 6	most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD}	positive supply voltage (+ 5 V)
13	DGND	digital ground
14	f_{CLK}	15 MHz clock input
15	bit 1	
16	bit 0	least-significant bit (LSB)
17	UNFL	underflow
18	n.c.	not connected
19	V_{BB}	back bias output
20	V_{refL}	reference voltage LOW
21	n.c.	not connected
22	n.c.	not connected
23	V_{DD}	positive supply voltage (+ 5 V)
24	V_{DD}	positive supply voltage (+ 12 V)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pins 3, 12, 23)	V_{DD}	−0,5 to	+ 7	V
Supply voltage range (pin 24)	V_{DD}	−0,5 to	+ 13,5	V
Input voltage range	V_I	−0,5 to	+ 7	V
Output current	I_O		5	mA
Total power dissipation	P_{tot}		tbf	mW
Storage temperature range	T_{stg}	−65 to	+ 150	°C
Operating ambient temperature range	T_{amb}	−10 to	+ 80	°C

HANDLING

Inputs and output are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

$V_{DD5} = V_{3, 12, 23-13} = 4{,}75$ to 5,25 V; $V_{DD12} = V_{24-2} = 11{,}4$ to 12,6 V; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pins 3, 12, 23)	V_{DD}	4,75	5,0	5,25	V
Supply voltage (pin 24)	V_{DD}	11,4	12,0	12,6	V
Supply current (pins 3, 12, 23)	I_{DD}	–	40	70	mA
Supply current (pin 24)	I_{DD}	–	12	20	mA
Reference voltages					
Reference voltage LOW (pin 20)	V_{refL}	2,4	2,5	2,6	V
Reference voltage HIGH (pin 4)	V_{refH}	5,0	5,1	5,2	V
Reference current	I_{ref}	120	200	280	μA
Inputs					
Clock input (pin 14)					
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	5,5	V
Digital input levels (STC, pin 5)*					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	5,5	V
Input leakage current (not STC)	I_{LI}	–	–	10	μA
Analogue input levels (pin 1) at $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V					
Input voltage amplitude (peak-to-peak value)	$V_{I(p-p)}$	–	2,6	–	V
Input voltage (underflow)	V_I	–	2,5	–	V
Input voltage (overflow)	V_I	–	5,1	–	V
Offset input voltage (underflow)	$V_I - V_{refL}$	–	10	–	mV
Offset input voltage (overflow)	$V_I - V_{refH}$	–	−10	–	mV
Input capacitance	C_{1-2}	tbf	40	tbf	pF
Outputs					
Digital voltage outputs (pins 6 to 11 and 15 to 17)					
Output voltage LOW at $I_O = 2$ mA	V_{OL}	0	–	−0,4	V
Output voltage HIGH at $-I_O = 0{,}2$ mA	V_{OL}	2,4	–	V_{DD5}	V

* When input voltage is LOW binary coding is selected; when input voltage is HIGH two's complement is selected; if pin 5 is open-circuit the input is HIGH. For output coding see Table 1.

Table 1 Output coding (V_{refL} = 2,5 V; V_{refH} = 5,08 V)

step	V_{1-2} (typ.)	UNFL	OVFL	binary bit 6 – bit 0	two's complement bit 6 – bit 0
underflow	< 2,51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2,51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2,53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
.	.	.	.	. . . .	. . . .
126	5,03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5,05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
overflow	⩾ 5,07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

steps 2 – 125

CHARACTERISTICS (continued)

$V_{DD5} = V_{3, 12, 23-13} = 5{,}0$ V; $V_{DD12} = V_{24-2} = 12{,}0$ V; $V_{refL} = 2{,}5$ V; $V_{refH} = 5{,}1$ V; $C_{BB} = 100$ nF; $T_{amb} = 0$ to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Timing (see also Fig. 3)					
Clock input (pin 14)					
Clock frequency	f_{CLK}	1	–	15	MHz
Clock cycle time LOW	t_{LOW}	22	–	–	ns
Clock cycle time HIGH	t_{HIGH}	22	–	–	ns
Input rise and fall times (note 1)					
rise time	t_r	–	–	3	ns
fall time	t_f	–	–	3	ns
Analogue input (pin 1)					
Bandwidth (–3 dB)	B	–	6	–	MHz
Aperture time delay (note 2)	t_{ad}	–	8	–	ns
Aperture jitter time	t_{aj}	–	0,2	–	ns
Digital outputs (note 3)					
Output hold time	t_{HOLD}	tbf	20	–	ns
Output delay time	t_d	–	35	50	ns
Internal delay	t_{CY}	–	3	–	clocks
Propagation delay time at f_{CLK} = 13,5 MHz	t_{pd}	tbf	–	272	ns
Transfer function					
Linearity, integral and differential (± 0,4% full scale)		–	–	± ½	LSB

Notes see next page.

Notes to timing characteristics

1. Clock input rise and fall times are at the maximum clock frequency (15 MHz).
2. The aperture time delay is referenced to the peak-to-peak value of the analogue input voltage at $V_{I(p-p)}$ = 2,6 V (full scale); f = 5 MHz.
3. The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1,5 V.

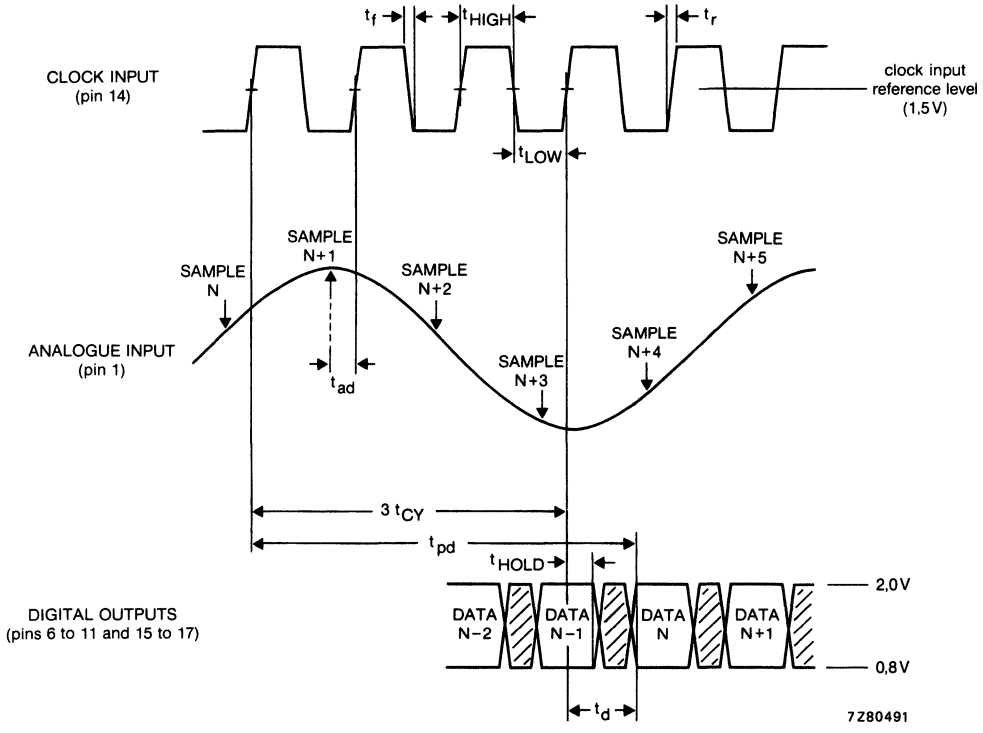


Fig. 3 Timing diagram.

7-Bit Analog to Digital Converter (ADC 7) — PNA7507

APPLICATION INFORMATION

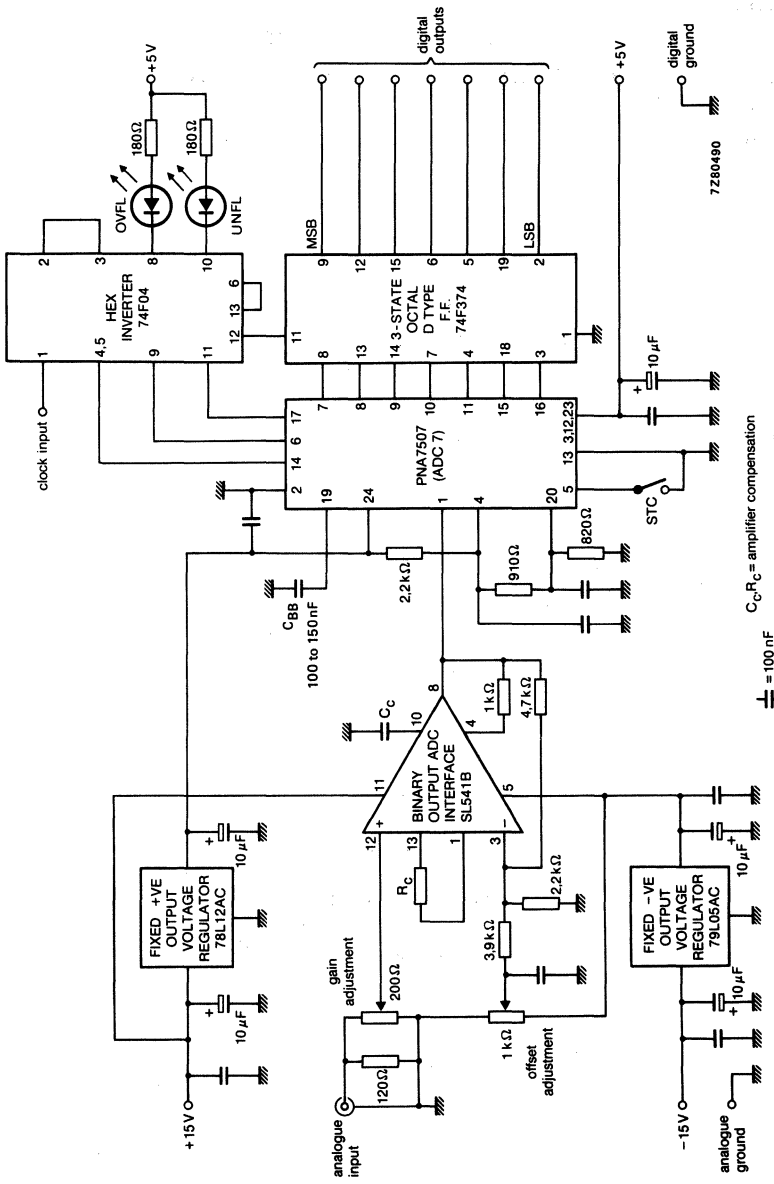


Fig. 4 Application circuit diagram.

14-Bit Analog to Digital Converter (Serial Output) TDA1534

DESCRIPTION

The TDA1534 is a monolithic 14-bit successive approximation Analog-to-Digital Converter (ADC) with internal reference and clock. The high linearity makes it suitable for Digital Signal Processing and the accurate, temperature stable reference makes it applicable for instrumentation purposes. The converter accepts either unipolar or bipolar input voltages. All digital outputs are TTL compatible and the digital output is in serial form.

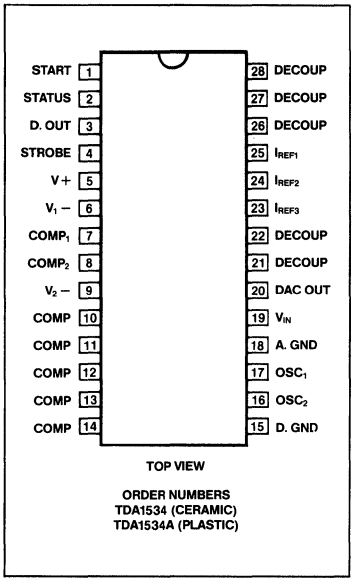
FEATURES

- **Accurate reference**
- **Internal clock**
- **¼ LSB linearity at 25°C**
- **½ LSB linearity over temp**
- **Meets quality audio specifications**
- **TTL compatible outputs**
- **High signal-to-noise ratio (85 dB typ)**

APPLICATIONS

- **Instrumentation**
- **DSP**
- **Correlators**
- **Digital audio**

PIN CONFIGURATION



TOP VIEW

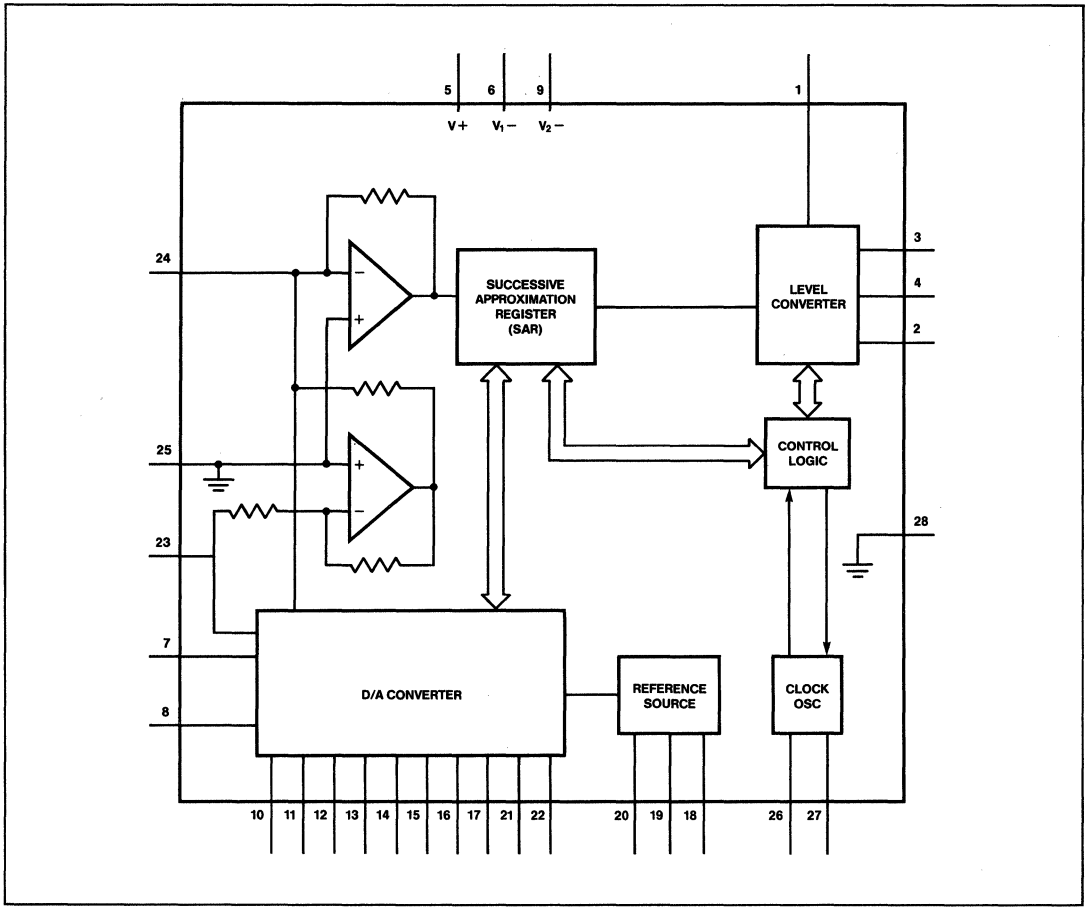
ORDER NUMBERS
TDA1534 (CERAMIC)
TDA1534A (PLASTIC)

REFERENCE DATA

PARAMETER	LIMIT	UNITS
Positive supply (pin 5)	5	V
Negative supply 1 (pin 6)	–5	V
Negative supply 2 (pin 9)	–17	V
Signal-to-noise ratio	84	dB
Linearity error	½	LSB
Resolution	14	bits

4

BLOCK DIAGRAM



12-Bit D/A Converter — DAC800

DESCRIPTION

The DAC800 is a single-chip converter with 12-bit linearity, obtained without trimming. It is pin compatible with the industry standard DAC80 (no external reference can be used) and has a faster settling time. This converter has thin film application resistors, a low temperature coefficient bandgap reference, and an output amplifier (V models).

The DAC800 provides for both bipolar and unipolar outputs. The V models allow output ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. The current models have an output range of either ±1mA or 0 to −2mA.

The DAC800 has a maximum nonlinearity error of ±½ LSB over the full temperature range, 0°C to 70°C. Additionally, the DAC800 offers maximum total error over the full temperature range of ±0.15% of full-scale for unipolar operation and ±0.12% of full-scale for bipolar operation. The total error includes the effects of gain, offset, and linearity drift with gain and offset errors adjusted to zero at 25°C.

FEATURES

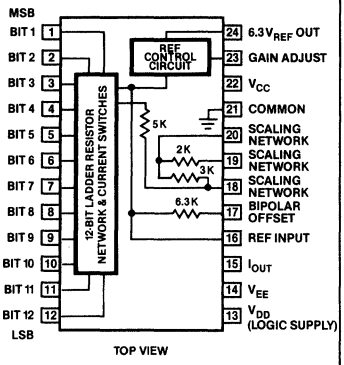
- **Maximum Nonlinearity ±½ LSB**
- **Guaranteed Monotonicity 0°C to 70°C**
- **Current or Voltage Output Models**
- **Internal Reference**
- **Unipolar and Bipolar Operation**
- **Compatible with TTL/LSTTL/CMOS**
- **No Laser Trimming**
- **Excellent Power Supply Rejection**

APPLICATIONS

- **Data Acquisition and Control Systems**
- **Analog-to-Digital Converter Systems**
- **Automatic Test Equipment**
- **Robotics**
- **Waveform Generation**

PIN CONFIGURATIONS

Current Model
F Package

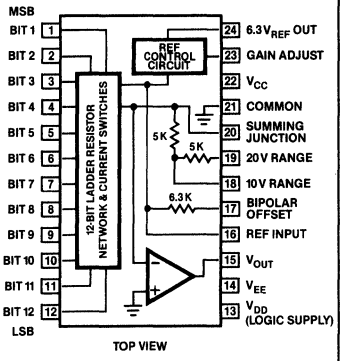


TOP VIEW

Order Number

DAC800IF

Voltage Model
F Package



TOP VIEW

Order Number

DAC800VF

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 15V, V_{EE} = -15V, V_{DD} = 5V, 0°C < T_A < 70°C$ (Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	Logic Input High		2		16.5	V
V_{IL}	Logic Input Low		0		0.8	V
I_{IH}	Logic High Input Current	$V_{IN} = 2.4V$			20	μA
I_{IL}	Logic Low Input Current	$V_{IN} = 0.4V$	−20			μA
	Power Supply Sensitivity V_{CC}, V_{EE}, V_{DD}			±0.0005	±0.001	% of FSR/%V
	V_{CC}, V_{EE}		±13.5	±15	±16.5	V
	V_{DD}[5]		4.5	5	16.5	V
	I_{CC}			11	14	mA
	I_{EE}		−20	−17		mA
	I_{DD}			6.5	8	mA

NOTES:
1. Adjustable to zero with external trim potentiometer.
2. To maintain drift specs internal resistors must be used on current output model.
3. FSR means full-scale range and is 20V for ±10V range, 10V for ±5V range, etc.
4. Includes the effects of gain, offset, and linearity drift. Gain and offset errors are adjusted to zero at 25°C.
5. Power dissipation is an additional 20mW when V_{DD} is operated at +15V.
6. $R_L = 2K$, $C_L = 200pF$, $T_A = 25°C$ for V models only.
7. $C_L = 10pF$, $T_A = 25°C$ for I models.
8. Typical operating conditions for Amplifier Duration Output Short Circuit to Ground is indefinite at this time.

POWER SUPPLY CONNECTIONS

Any noise present on the power supply pins of the DAC800 creates additional error. For optimum performance this noise should be limited as much as possible. This can be accomplished by bypassing the power supply pins with appropriate capacitors. Decoupling capacitors on the order of 1μF are recommended with the best types being tantalum or electrolytic. Electrolytic capacitors have poor high frequency characteristics and, if used, should be paralleled with a 0.01μF ceramic capacitor.

LOGIC INPUTS

The logic inputs of the DAC800 are compatible with TTL, LSTTL, and CMOS over the operating range of V_{DD} (5V to 15V) as well as over temperature (0°C to 70°C). The input switching threshold is TTL (about 1.4V) and is independent of the supply voltage, V_{DD}.

Logic input coding for the DAC800 is complementary. The specific code will be complementary straight binary (CSB) for unipolar output connections and complementary offset binary (COB) for bipolar output connections. For bipolar output connections, complementary two's complement (CTC) can be realized by inverting the MSB with an external inverter. The relationship between the digital input and analog output for the three codes is shown in Table 1.

VOLTAGE REFERENCE

The DAC800 has an internal 6.3V reference with a ±1% tolerance. The reference is connected internally to the converter and to the bipolar offset resistor and to pin 16 which does not allow the use of an external reference. The reference is brought out on pin 24 for external use, if needed, and can typically supply 2.5mA. If the external load varies, an external buffer is recommended in order to isolate the reference from load variations.

EXTERNAL GAIN/OFFSET ADJUSTMENTS

The gain and offset of the DAC800 can be adjusted with external potentiometers. The potentiometer configuration required for gain adjustment is shown in Figure 1. The 10MΩ resistor should have a tolerance of 20% or less and the potentiometer and 10MΩ resistor should have a temperature coefficient of 200ppm/°C or less.

The potentiometer configuration required for offset adjustment is shown in Figure 2 and its equivalent circuit in Figure 3. From the equivalent circuit it can be seen that this configuration adds/subtracts a current from the converter output current. The 3.9MΩ resistor should have a tolerance of 20% or less and the potentiometer and 3.8MΩ resistor should have a temperature coefficient of 200 ppm/°C or less. Both adjustment circuits should be located close to the DAC800 to prevent noise pickup. If full-scale accuracy is not required, then the gain adjust pin may be grounded to minimize noise pick-up.

The effects of gain and offset adjustment are shown in Figures 4 and 5. Figure 4 shows that gain adjustment rotates the transfer function about the origin and has no impact on the origin. Figure 5 shows that offset adjustment translates the transfer function along the ANALOG OUTPUT axis. Note that this changes the output for full-scale. The objective of the adjustment procedure is to fix the end points of the transfer function at the ideal points. For this reason the adjustment sequence must be to first adjust the offset and then the gain. Offset adjustment is accomplished by setting all logic inputs to a logic high ("1") and adjusting the offset so that the output corresponds to its most negative value (zero for unipolar outputs and −full-scale for bipolar outputs). Gain adjustment is accomplished by setting all logic inputs to a logic low ("0") and adjusting the gain such that the output corresponds to its most positive value (full-scale −1 LSB).

VOLTAGE MODEL OUTPUT CONNECTIONS

The DAC800 voltage models have internal scaling resistors which provide output ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. The use of the internal resistors minimizes gain and offset drift since excellent thermal tracking with other on-chip components limits this effect. Figures 6a, b and c show the different output configurations.

Table 1. Coding Relationships

DIGITAL INPUT	ANALOG OUTPUT		
	CSB	COB	CTC
MSB LSB			
000000000000	+Full-Scale −1 LSB	+Full-Scale −1 LSB	−1 LSB
011111111111	+½ Full-Scale	Zero	−Full-Scale
100000000000	+½ Full-Scale −1 LSB	−1 LSB	+Full-Scale −1 LSB
111111111111	Zero	−Full-Scale	Zero

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Temperature Range		
Operating	0 to 70	°C
Storage	−65 to +150	°C
Power Supply		
V_{CC}, V_{EE}	±16.5	V
V_{DD}	+16.5	V
Logic Levels		
High	+16.5	V
Low	0	V

NOTE:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 15V$, $V_{EE} = -15V$, $V_{DD} = 5V$, $0°C < T_A < 70°C$ (Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		12			Bits
	Monotonicity		12			Bits
NL	Nonlinearity				±½	LSB
DNL	Differential Nonlinearity			±½	±1	LSB
	Gain Error[1]	$T_A = 25°C$		±0.1	±0.2	% of FSR
	Gain Tempco			±10	±30	ppm/°C
	Offset Error[1]			±0.05	±0.15	% of FSR[3]
	Offset Tempco[2]	Unipolar Connection		±1	±3	ppm of FSR/°C
	Offset Tempco[2]	Bipolar Connection		±7	±15	ppm of FSR/°C
	Bipolar Drift	Full-Scale Drift for Bipolar Connection		±10	±25	ppm of FSR/°C
	Total Error[4]	Unipolar Connection		±0.06	±0.15	% of FSR
	Total Error[4]	Bipolar Connection		±0.05	±0.12	% of FSR
t_S	Settling Time to 0.01% of FSR[6]	20V Range		3	5	μs
t_S	Settling Time to 0.01% of FSR[6]	10V Range		2.5	4	μs
t_S	Settling Time to 0.01% of FSR[6]	1 LSB Change, Major Carry		1.5		μs
t_S	Settling Time to 0.01% of FSR[7]	10 to 100Ω Load		300		ns
t_S	Settling Time to 0.01% of FSR[7]	1kΩ Load		1		μs
	Full-Scale Current	I Model Only	1.7	2	2.3	mA
	Converter Output Impedance	I Model Only		10		MΩ
	Converter Output Compliance	I Model Only	−2.5		+2.5	V
	Amplifier Slew Rate[6]		10	15		V/μs
	Amplifier Output Current	V Model Only	±5			mA
	Amplifier DC Output Impedance	V Model Only		0.05		Ω
	Amplifier Duration Output Short Circuit to Ground[8]	V Model Only				
V_{REF}	Reference Voltage Output		6.23	6.30	6.37	V
	Reference Voltage Tempco			±10	±30	ppm/°C
	Reference Output Source Current		1.5	2.5		mA

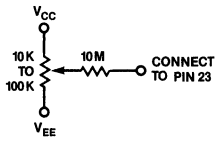


Figure 1. Gain Adjust Circuit

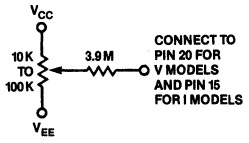


Figure 2. Offset Adjust Circuit

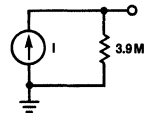


Figure 3. Offset Adjust Equivalent Circuit

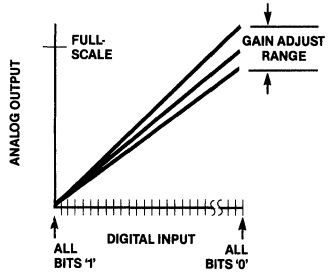


Figure 4. Gain Adjust Effects

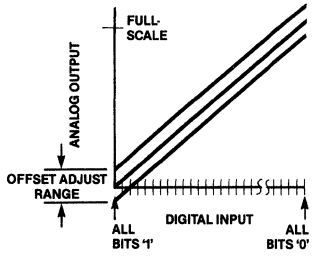
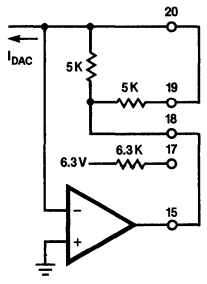
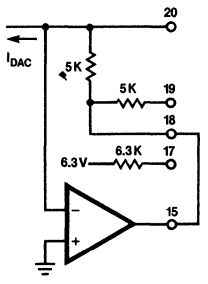


Figure 5. Offset Adjust Effects



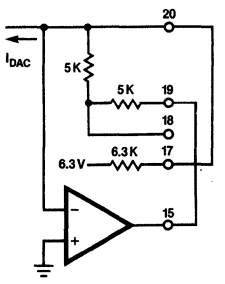
*Connect pin 17 to pin 20 for ±2.5V Range and to ground for 0 to 5V Range

a. Connections for 0 to 5V Range and ±2.5V Range (V model)



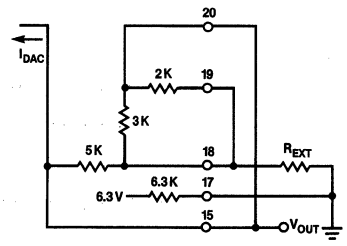
*Connect pin 17 to pin 20 for ±5V Range and to ground for 0 to 10V Range

b. Connections for 0 to 10V Range and ±5V Range (V model)

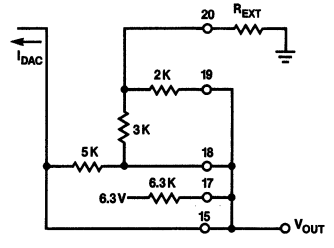


c. Connections for ±10V Range (V model)

Figure 6.



a. Connections for 0 to −2V Range (I model)



b. Connections for +1V Range (I model)

Figure 7.

CURRENT MODEL OUTPUT CONNECTIONS

Internal resistors are provided for the current models which can be used with an external op amp or configured as a resistive load for output ranges of 0 to −2V or ±1V. Use of these internal resistors is required to maintain gain and bipolar offset drift specifications.

Output ranges of 0 to −2V and ±1V are obtainable with the addition of a single external resistor (excluding the gain and offset adjustment components). Figures 7a and b show the necessary connections for these output ranges. The internal resistors of the DAC800 have wide tolerances and the external resistor, R_{ext} will have to be selected for each unit. Nominal values will be 32Ω for the unipolar connection and 0Ω for the bipolar connection.

The current output can also be used to drive the summing junction of an external op amp used as a voltage to current converter. This has the advantage of faster settling time than the voltage model. Figure 8 shows the general configuration and Table 2 lists the available output ranges and required connections.

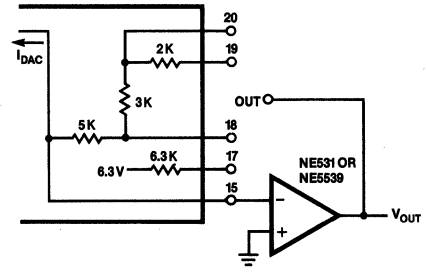


Figure 8. General Configuration for Current Model Using External Op Amp

Table 2. Current Model Connection for Various Output Ranges

OUTPUT RANGE	CONNECT		
	OUT TO	19 TO	17 TO
±10V	19	Out	15
±5V	18	NC	15
±2.5V	18	15	15
0 to +10V	18	NC	GND
0 to +5V	18	15	GND

8-Bit Microprocessor-Compatible D/A Converter | SE/NE5018

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

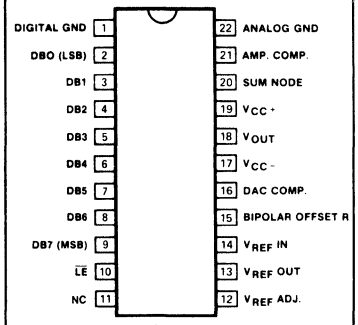
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/2 LSB (.19%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

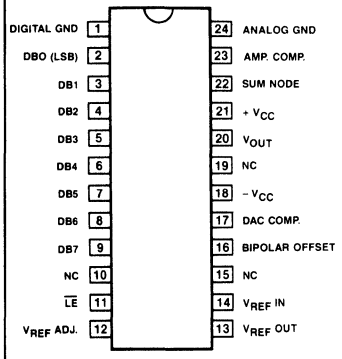
PIN CONFIGURATION

F,N PACKAGE



ORDER NUMBERS
SE/NE5018F,N

D² PACKAGE



TOP VIEW
ORDER NUMBER
NE5018D²

NOTES:
1. SOL-Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

BLOCK DIAGRAM

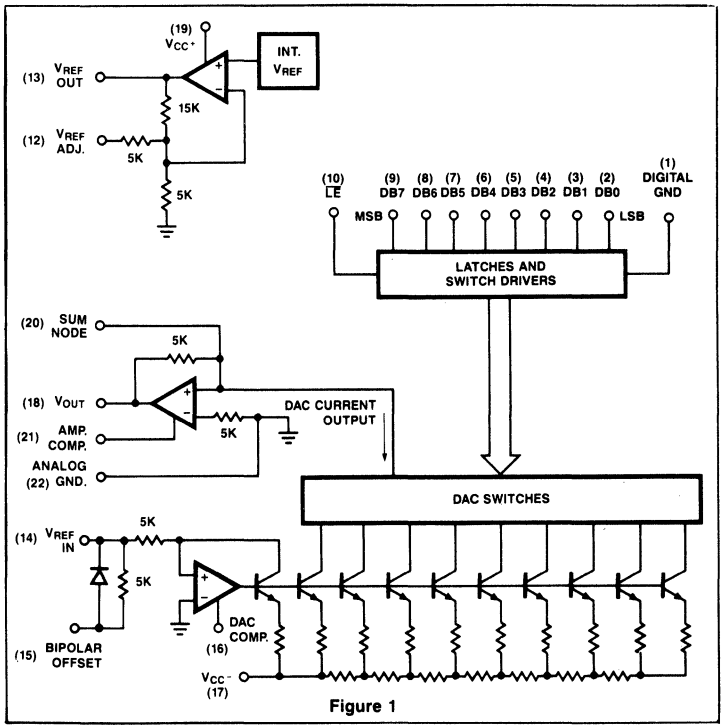


Figure 1

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
$I_{REF}SC$	Short-circuit current to ground at V_{REF} OUT	Continuous	
$I_{OUT}SC$	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5018	−55 to +125	°C
	NE5018	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018, $-55°C \leq T_A \leq 125°C$, NE5018, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1]
Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN}$ = 5.000V, T_A = 25°C	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN}$ = 5.000V, T_A = 25°C	4.5 -5.04	+4.961 −5.000	5.5 -4.960	4.5 5.04	+4.961 −5.000	5.5 4.960	V
V_{ZS}	Zero scale voltage		-30	5	+30	-30	5	+30	mV
I_{OS}	Output short circuit current	T_A = 25°C, V_{OUT} = 0V		15	40		15	40	mA
PSR+(out)	Output power supply rejection (+)	V− = −15V, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN}$ = 5.000V		.001	.01		.001	.01	%FS %VS
PSR−(out)	Output power supply rejection (−)	V+ = 15V, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN}$ = 5.000V		.001	.01		.001	.01	%FS %VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN}$ = 5.000V		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd)

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1]
Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE/5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$ $T_A = 25°C$		60			60		ppm/°C
Z_{IN}	DAC V_{REF} IN input impedance	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.15	5.0	5.85	4.15	5.0	5.85	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE
1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2]

$V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5018			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[3]		1.8		μs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[4]		2.3		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns

NOTES
2. Refer to Figure 3.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. See Figure 10.
8. For reference currents > 3mA, use of an external buffer is required.

DC PARAMETRIC TEST CONFIGURATION

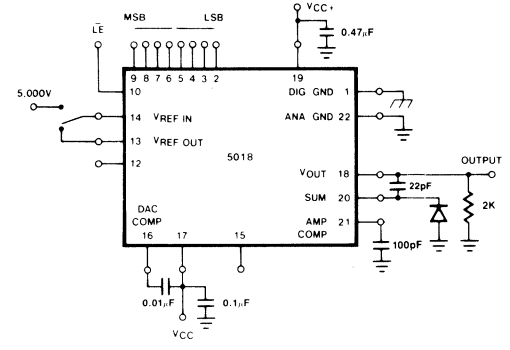


Figure 2

AC PARAMETRIC TEST CONFIGUTATION

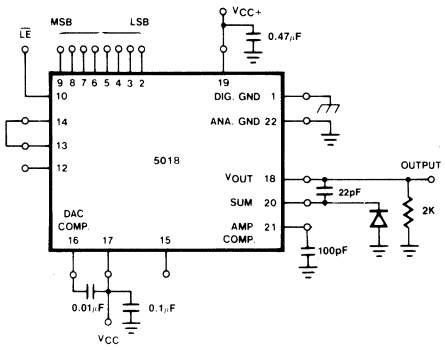


Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

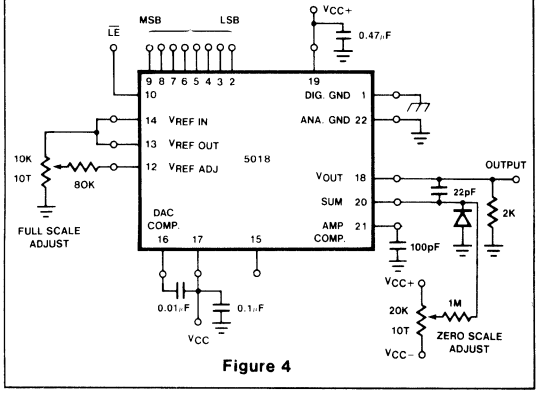


Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

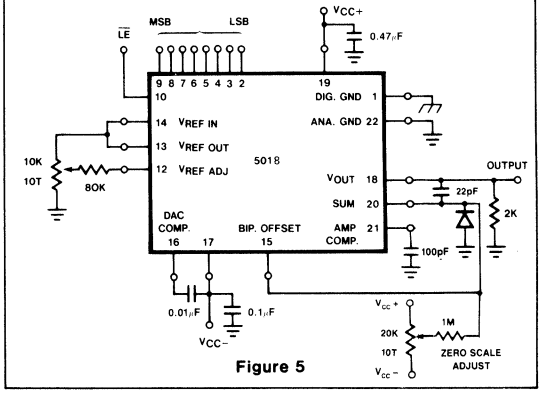


Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

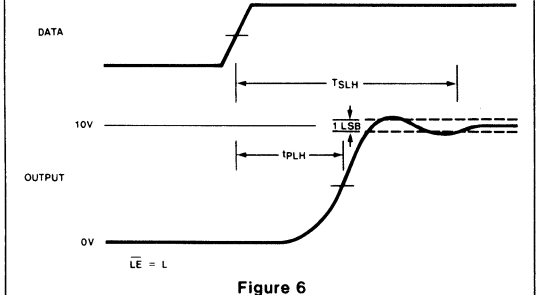


Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

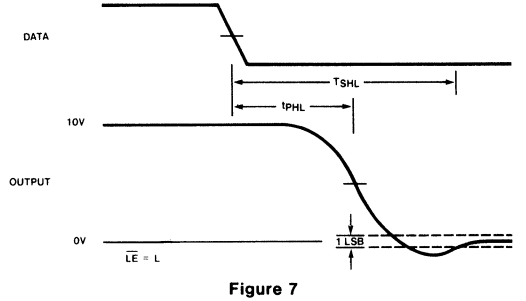


Figure 7

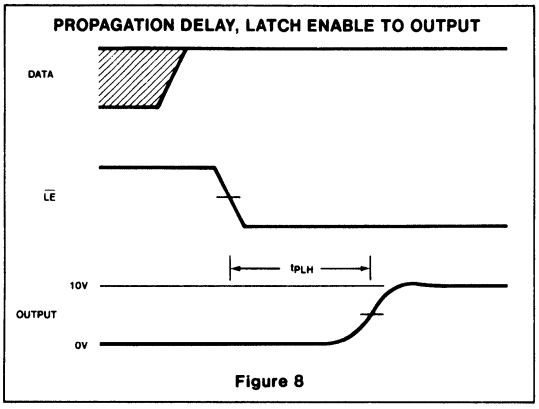


Figure 8

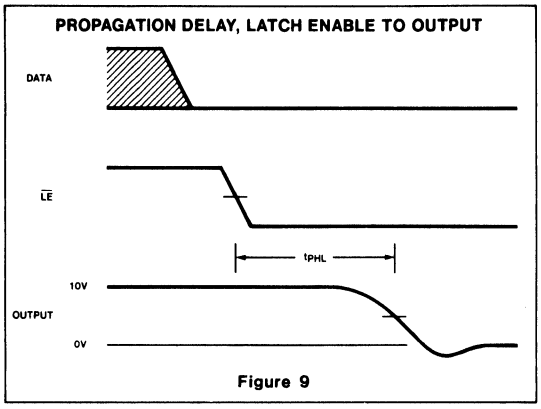


Figure 9

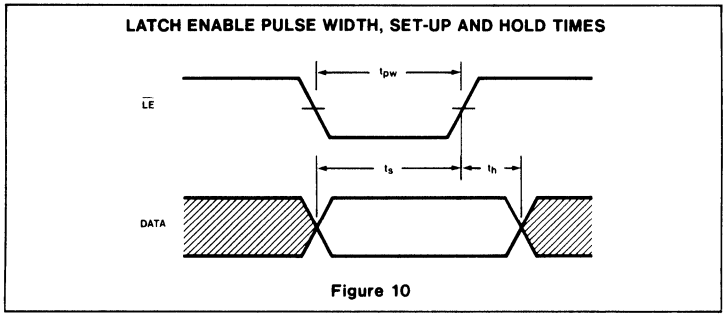


Figure 10

8-Bit Microprocessor-Compatible D/A Converter — SE/NE5019

DESCRIPTION

The NE5019 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

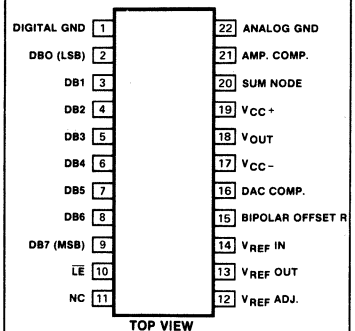
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

PIN CONFIGURATION

F,N PACKAGE



TOP VIEW

ORDER NUMBERS

NE5019F SE5019F
NE5019N

BLOCK DIAGRAM

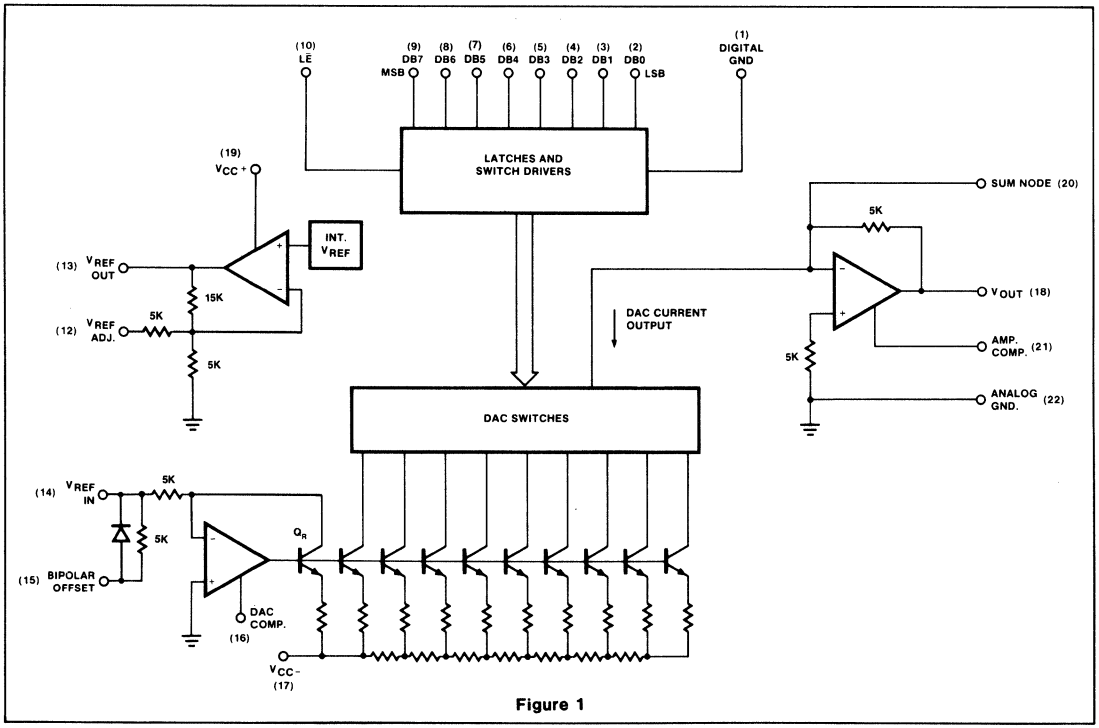


Figure 1

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5019	−55 to +125	°C
	NE5019	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1]
Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN}$ = 5.000V, T_A = 25°C	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN}$ = 5.000V, T_A = 25°C	4.5	+4.961	5.5	4.5	+4.961	5.5	V
			-5.040	−5.000	-4.960	-5.040	−5.000	-4.960	
V_{ZS}	Zero scale voltage		-30	5	+30	-30	5	+30	mV
I_{OS}	Output short circuit current	T_A = 25°C, V_{OUT} = 0V		15	40		15	40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	V− = −15V, 13.5V≤V+≤16.5V, external $V_{REF\ IN}$ = 5.000V		.001	.01		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	V+ = 15V, −13.5V≤V−≤−16.5V, external $V_{REF\ IN}$ = 5.000V		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN}$ = 5.000V		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

NOTE
1. Refer to Figure 2.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1]
Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$, $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/ %VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/ %VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$, $T_A = 25°C$		60			60		ppm/°C
Z_{IN}	DAC V_{REF}IN input impedance	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.15	5.0	5.85	4.15	5.0	5.85	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2]

$V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5019			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[3]		1.8		μs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[4]		2.3		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns

NOTES

2. Refer to Figure 3.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. See Figure 10.
8. For reference currents > 3mA, use of an external buffer is required.

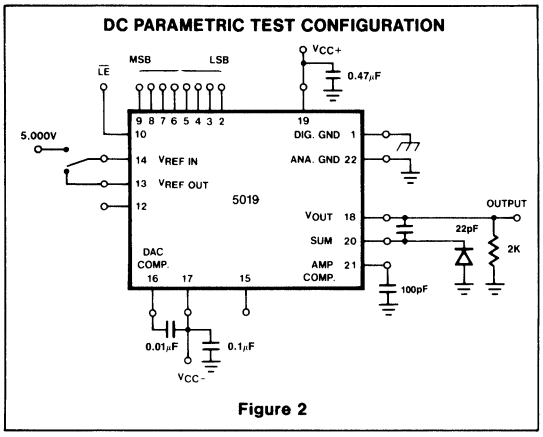


Figure 2

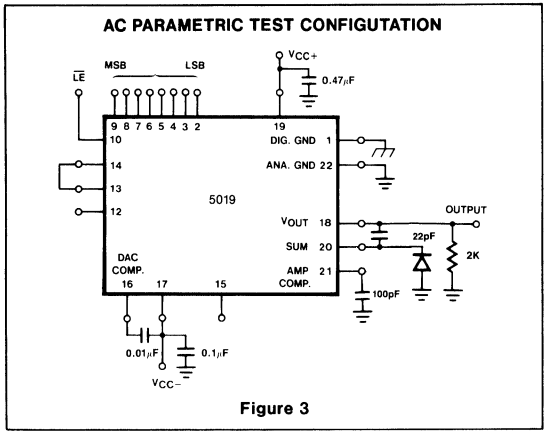


Figure 3

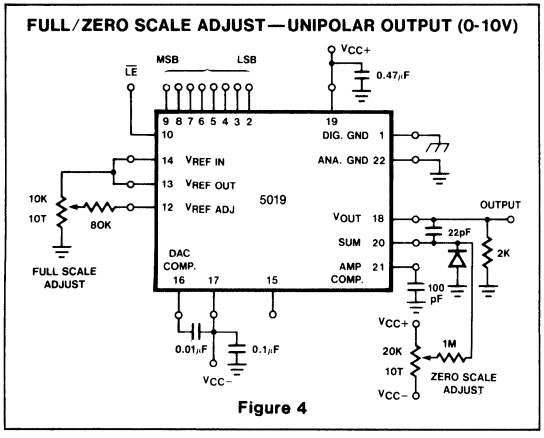


Figure 4

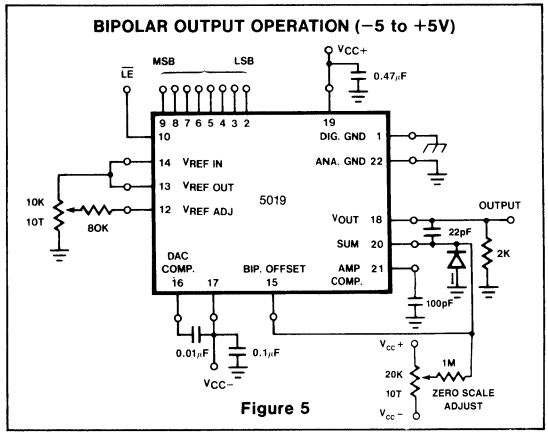


Figure 5

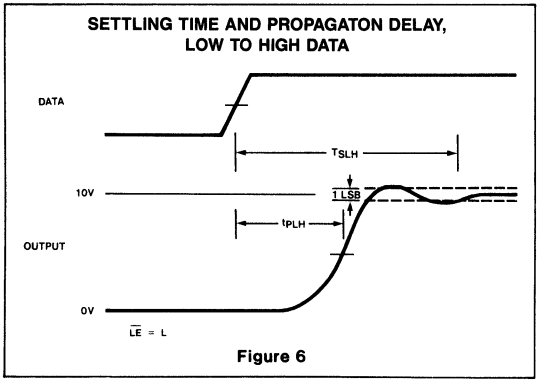


Figure 6

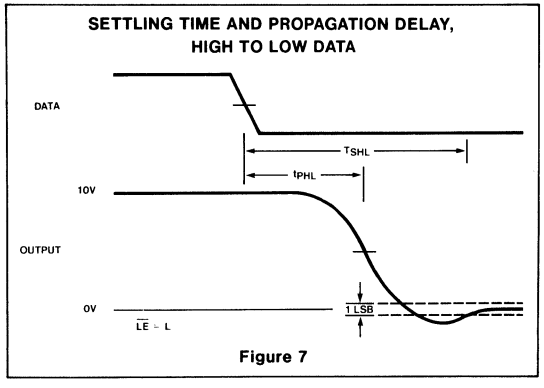


Figure 7

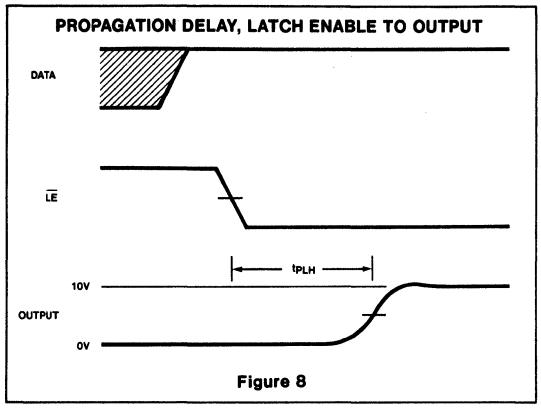


Figure 8

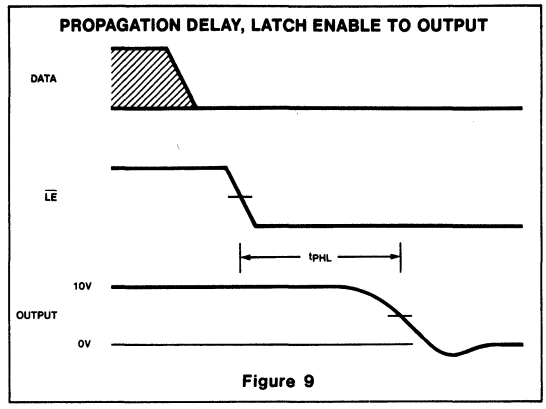


Figure 9

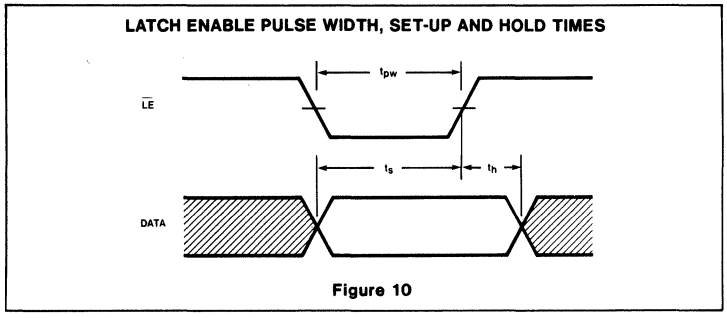


Figure 10

10-Bit Microprocessor-Compatible D/A Converter | SE/NE5020

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital to analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds and addressing capability allow the NE5020 to directly interface with most microprocessor and logic controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

FEATURES

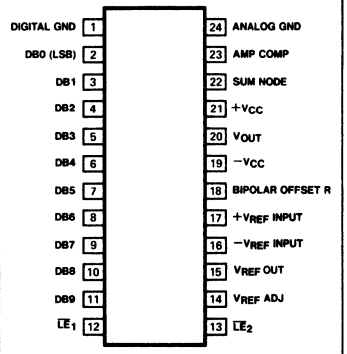
- **10-bit resolution**
- **Guaranteed monotonicity over operating range**
- **±0.1% relative accuracy**
- **Unipolar (0V to +10V) and Bipolar (±5V) output range**
- **Logic bus compatible**
- **5μsec settling time**

APPLICATIONS

- **Precision 10-bit D/A converters**
- **10-bit Analog to Digital converters**
- **Programmable power supplies**
- **Test equipment**
- **Measurement instruments**

PIN CONFIGURATION

F, N PACKAGE



ORDER NUMBERS
NE5020F
NE5020N

BLOCK DIAGRAM

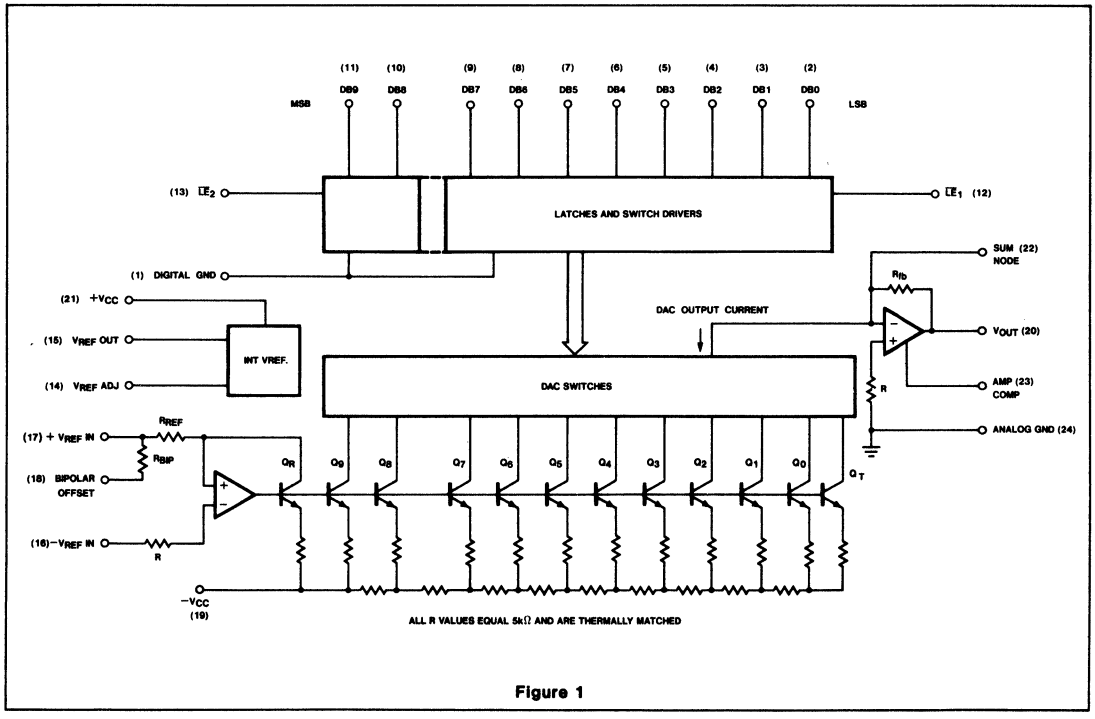


Figure 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at $+V_{REF}$ input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	F package	1000	mW
T_A	Operating temperature range NE5020	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1]
Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	NE5020			UNIT
			Min	Typ	Max	
	Resolution				10	Bits
	Monotonicity				10	Bits
	Relative accuracy				±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15	16.5	V
$V_{CC}-$	Negative supply voltage		−11.4	−15	−16.5	V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN}$ = 5.000V, T_A = 25°C	9.5	9.9902	10.5	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN}$ = 5.000V, T_A = 25°C	4.5	4.9902	5.5	V
V_{ZS}	Zero scale voltage	Unipolar operation	-5.040 -30	−5.000 5	-4.960 +30	mV
I_{OS}	Output short circuit current	T_A = 25°C V_{OUT} = 0V		±15	±40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	V− = −15V, 13.5V≤V+≤16.5V, external $V_{REF\ IN}$ = 5.000V		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	V+ = 15V, −13.5V≤V−≤−16.5V, external $V_{REF\ IN}$ = 5.000V		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN}$ = 5.000V		20		ppmFS/°C
TC_{ZS}	Zero scale temperature coefficient			5		ppmFS/°C

NOTE
1. Refer to Figure 2.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	NE5020			UNIT
			Min	Typ	Max	
I_{REF}[2]	Reference output current				3	mA
$I_{REF\ SC}$	Reference short circuit current	$T_A = 25°C$, $V_{REF\ OUT} = 0V$		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01	%VR/%VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60		ppm/°C
Z_{IN}	DAC V_{REF}IN input impedance	$I_{REF} = 1.0mA$		5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435	mW

NOTE

1. Refer to Figure 2.
2. For I_{REF} OUT greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS[3] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	NE5020			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[4]		5		μs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[5]		5		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[4]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[5]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[4,5]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[6]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[7]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	3, 8	100			ns
t_h	Hold time	Input	$\overline{LE}$	3, 8	50			ns
t_{pw}	Latch enable pulse width			3, 8	150			ns

NOTES

3. Refer to Figure 3.
4. See Figure 6.
5. See Figure 7.
6. See Figure 8.
7. See Figure 9.
8. See Figure 10.

DC PARAMETRIC TEST CONFIGURATION

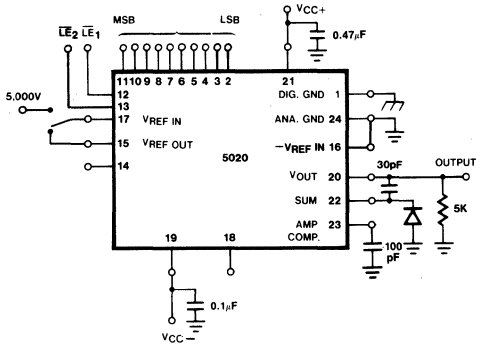


Figure 2

AC PARAMETRIC TEST CONFIGURATION

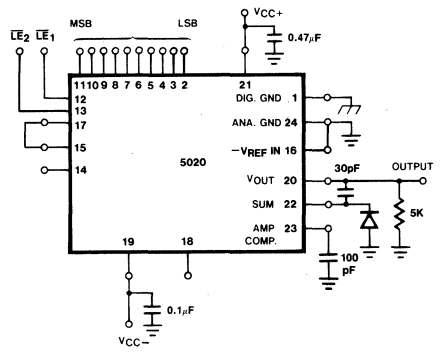


Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0–10V)

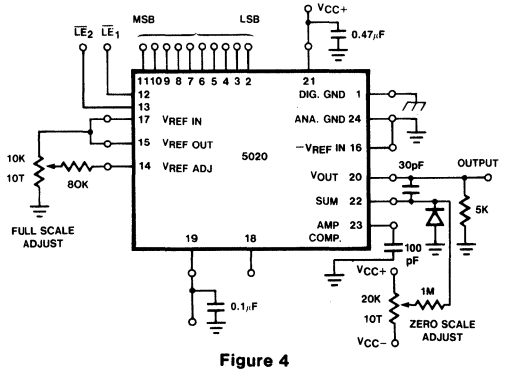


Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

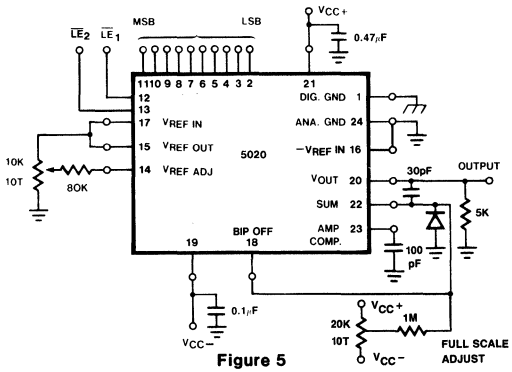


Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

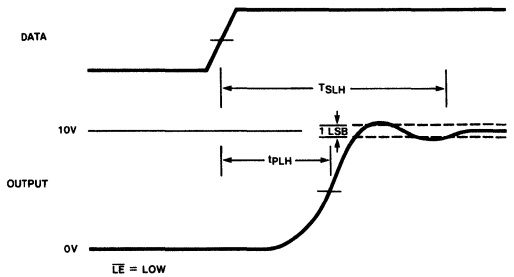


Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

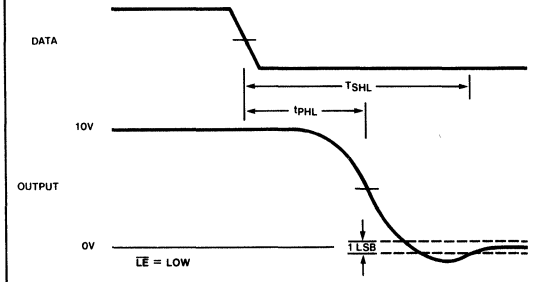


Figure 7

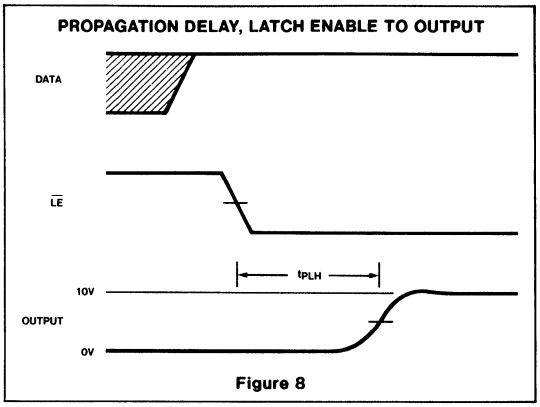


Figure 8

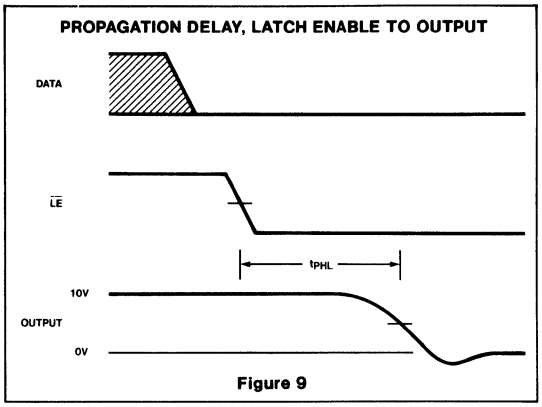


Figure 9

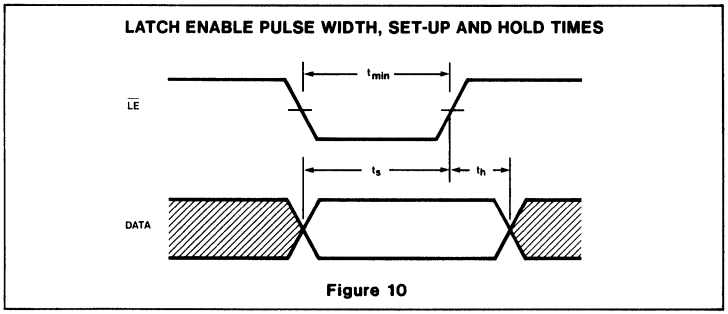


Figure 10

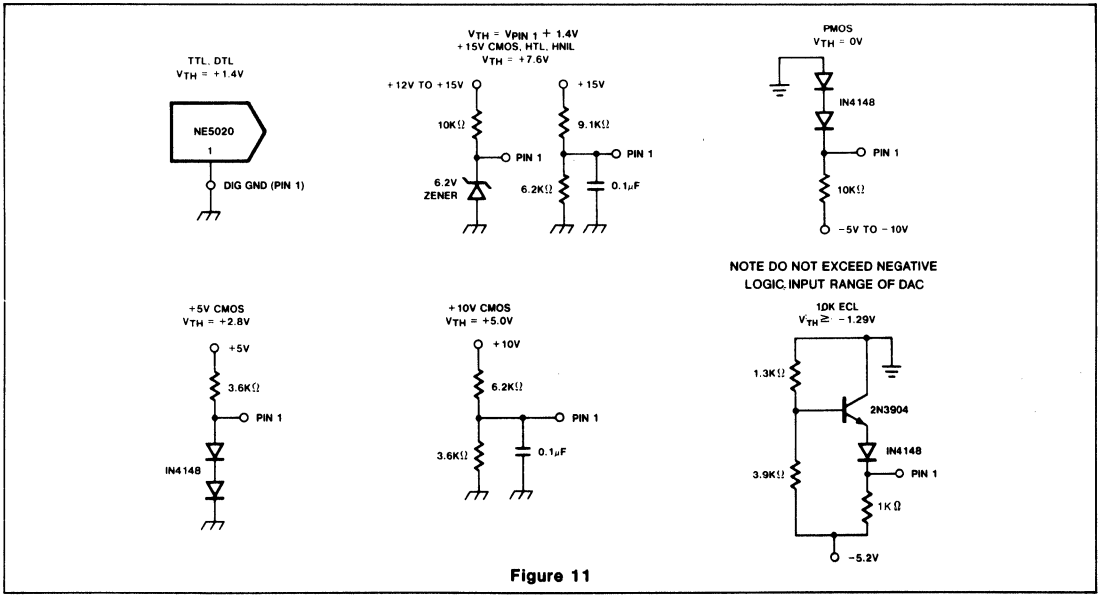


Figure 11

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage, in addition to the basic DAC components (see block diagram, figure 1).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports ($\overline{LE}_1$ and $\overline{LE}_2$) and ten data input latches. $\overline{LE}_2$ controls the two most significant bits of data (DB_9 and DB_8) while $\overline{LE}_1$ controls the eight lesser significant bits (DB_7 through DB_ϕ). Both the latch enable ports ($\overline{LE}$) and the data inputs are static and threshold sensitive. When the latch enable ports ($\overline{LE}$) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the $\overline{LE}$ with a low (Logic '0') the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on which $\overline{LE}$ goes high) 'memorize' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring $-2\mu A$ for low (.8V max) or $0.1\mu A$ for high (2.0V min)) when the $\overline{LE}$ is high. Any changes on the data bus with $\overline{LE}$ high will have no effect on the DAC output.

The digital logic inputs ($\overline{LE}$ and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (Pin 1). Figure 11 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus orientated system the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 10 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50nsec after $\overline{LE}$ is changed to a high state.

The independent $\overline{LE}$ ($\overline{LE}_1$ and $\overline{LE}_2$) lines allow for direct interface from an 8 bit data bus (see figure 12). Data for the two MSB's is supplied and stored when $\overline{LE}_2$ is activated low and returned high according to the NE5020 timing requirements. Then $\overline{LE}_1$ is activated low and the remaining eight LSB's of data are transferred into the DAC. With $\overline{LE}_1$ returning high the loading of ten bit data word from an eight bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16 bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8 bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 13 shows the circuit configuration.

After preloading (via $\overline{LE}$ pre-load) the external latch with the two MSB values, $\overline{LE}_2$ is activated low and the eight LSB's and the

NE5020 μP INTERFACE 8-BIT DATA BUS EXAMPLE

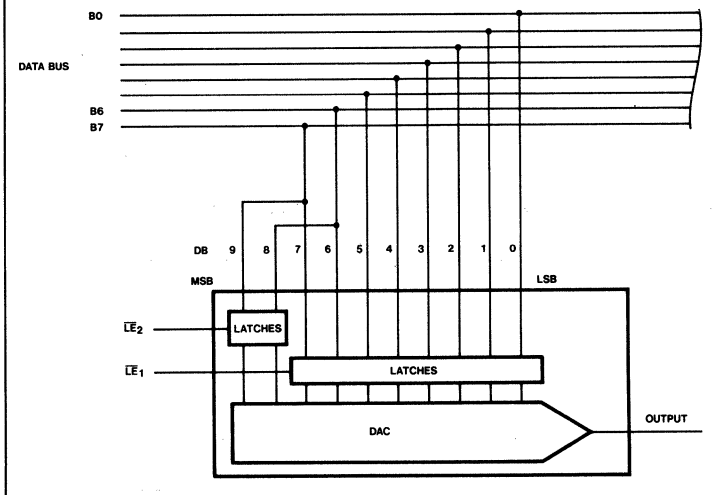


Figure 12

PRELOADING THE 2 MSB'S TO PROVIDE A SINGLE STEP OUTPUT

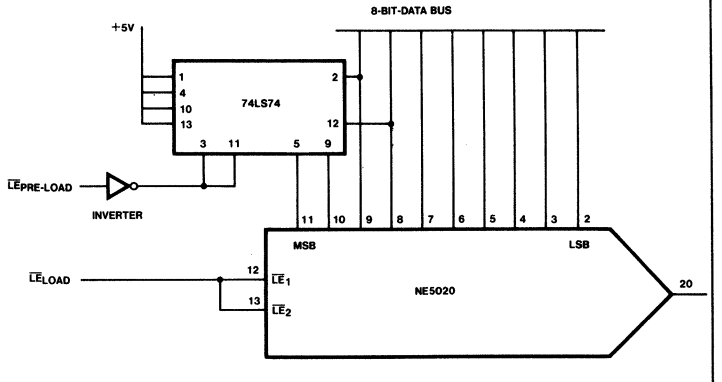


Figure 13

two MSB's are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5 volt reference output. Providing a V_{REF}ADJ (pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in figure 16 performs not only V_{REF} adjustment but also full scale output adjust. Notice that the V_{REF}ADJ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the V_{REF}ADJ pin and observing good layout practices.

The V_{REF} out node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier is used.

Input Amplifier

The DAC reference amplifier is a high gain internally compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

Figure 1 details the input reference amplifier and current ladder. The voltage to current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5 volt V_{REF}. This current sets the input bias to the ladder network. Data bit 9 (DB_9)(Q_9), when turned on, will mirror this current and will contribute 1mA to the output. DB_8 (Q_8) will contribute ½ of that value or 0.5mA and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}} \left(\frac{DB9}{2} + \frac{DB8}{4} + \frac{DB7}{8} + \frac{DB6}{16} + \frac{DB5}{32} + \frac{DB4}{64} + \frac{DB3}{128} + \frac{DB2}{256} + \frac{DB1}{512} + \frac{DB0}{1024} \right) .$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/μsec and source impedances at the $V_{REF\ INPUT}$ greater than 5kΩ should be avoided to maintain stability.

The $-V_{REF\ INPUT}$ pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF\ INPUT}$ is grounded and the negative reference is tied directly to the $-V_{REF\ INPUT}$. The $-V_{REF\ INPUT}$ contains a 5kΩ resistor that matches a like resistor in the $+V_{REF\ INPUT}$ to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on chip output op amp to eliminate the need for additional external active circuits. Its two stage design with feed forward compensation allows it to slew at 15V/μsec and settle to within ± ½LSB in 5μsec. These times are typical when driving the rated loads of $R_L \geq$ 5k and $C_L \leq$ 50pF with recommended values of C_{FF} = 1nF and C_{FB} = 30pF. Typical input offset voltages of 5mV and 50k open loop gain insure an accurate current to voltage conversion is performed when using the on chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at ± 15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short circuit and die temperature stabilization.

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP}, to offset the output voltage by 5 volts to obtain −5V to +5V output voltage range operation. This is accomplished by shorting pins 18 and 22 (see figure 14). This connection produces a current equal to ($V_{REF\ IN} - V_{sum\ node}$) ÷ R_{BIP}, (1mA nominal), which is injected into the sum node. Since full scale current out is approximately 2mA (1.9980mA), (2mA − 1mA)5k = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum mode and $V_{OUT} = -(5k)(1mA) = -5V$. Zero scale adjust and full scale adjust are performed as described below, noting that full scale voltage is now approximately +5 volts, zero scale adjust may be used to trim V_{OUT} = 0.00 with the MSB high or V_{OUT} = −5.0V with all bits off.

Zero Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in figure 15. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000 volts in the unipolar mode or −5.000 volts in the bipolar mode (see bipolar section) accomplishes this trim.

Full Scale Adjustment

A recommended full scale adjustment circuit when using the internal voltage reference is shown in figure 16. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accu-

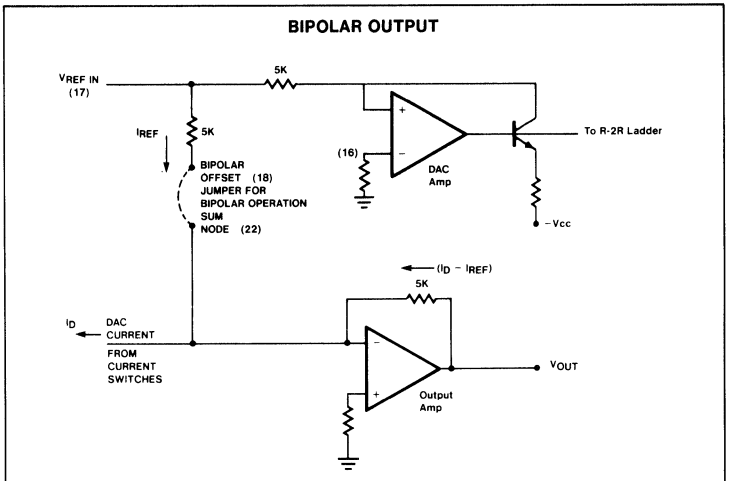


Figure 14

racy of full scale is of low importance when compared to the other system accuracy factors, then this adjustment circuit is optional.

As resistors R_{REF}, R_{fb} and R_{BIP} shown in figure 1 are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than ±0.3% which implies that typical full scale (or gain) error is less than ±0.3% of ideal full scale value.

ZERO SCALE ADJUSTMENT

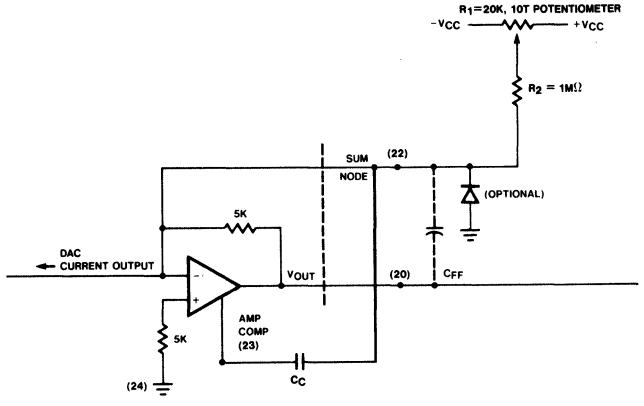


Figure 15

REFERENCE ADJUST CIRCUIT

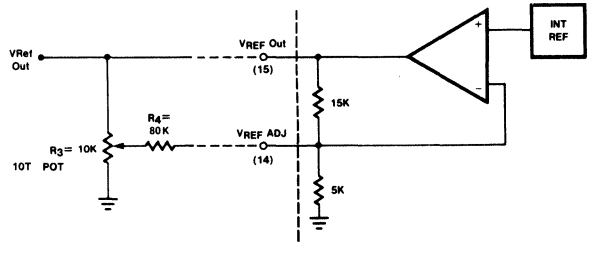


Figure 16

Triple 4-Bit RGB DAC

NE5150/NE5151

DESCRIPTION

The NE5150/5151 are triple 4-bit DAC's intended for use in graphic display systems. They are a high performance — yet cost effective — means of interfacing digital memory and a CRT. The NE5150 is a single integrated circuit chip containing special input buffers, an ECL static RAM, high-speed latches, and three 4-bit DAC's. The input buffers are *user* selectable as either ECL or TTL compatible. The RAM is organized as 16 x 12, so that 16 "color words" can be down loaded from the pixel memory into the chip memory. Each 12-bit word represents 4 bits of red, 4 bits of green and 4 bits of blue information. This system gives 4096 possible colors. The RAM is fast enough to completely reload during the *horizontal* retrace time. The latches resynchronize the digital data to the DAC's to prevent glitches. The DAC's include all the composite video functions to make the output waveforms meet RS170 and RS343 standards, and produce 1VPP into 75 ohms. The composite functions (reference white, bright, blank, and sync) are latched to prevent screen-edge distortions generally found on "video DAC's." External components are kept to an absolute minimum (bypass capacitors only as needed) by including all reference generation circuitry and termination resistors on chip, by building in high-frequency PSRR (eliminating separate V_{EE}'s and costly power supplies and filtering), and by using a single-ended clock. The guaranteed maximum operating frequency is 80MHz over the commercial temperature range. The device is housed in a standard 24-pin package and consumes less than 1W of power.

The NE5151 is a simplified version of the NE5150, including all functions except the memory. Maximum operating frequency is 150MHz.

FEATURES

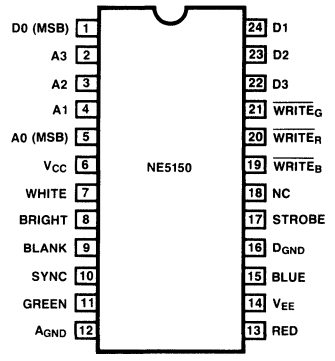
- **Single chip**
- **On-board ECL static RAM**
- **4096 colors**
- **ECL and TTL compatible**
- **80MHz update rate (NE5150)**
- **Low power and cost**
- **Drives 75-ohm cable directly**
- **Internal reference**
- **40dB PSRR**
- **No external components necessary**

APPLICATIONS

- **Bit-Map graphics**
- **Super high-speed DAC**
- **Home computers**
- **Raster-Scan displays**

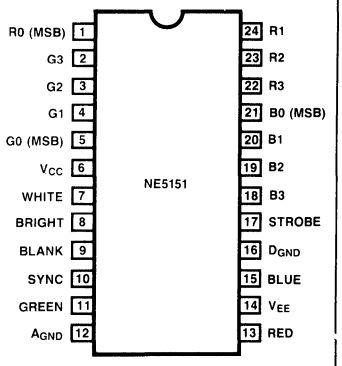
PIN CONFIGURATIONS

NE5150-F PACKAGE



TOP VIEW
Order Number
NE5150F

NE5151-F PACKAGE



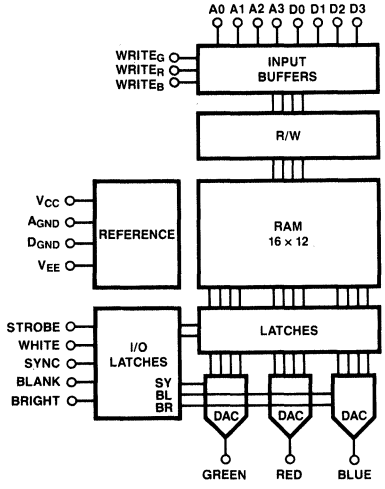
TOP VIEW
Order Number
NE5151F

4

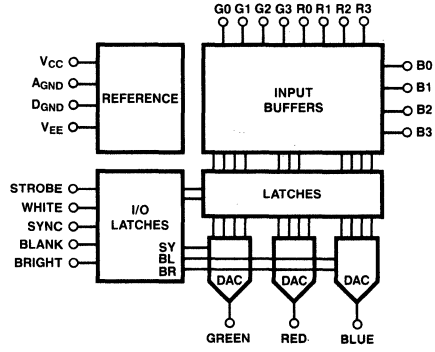
Triple 4-Bit RGB DAC | NE5150/NE5151

BLOCK DIAGRAMS

NE5150



NE5151



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Temperature range		
Operating	0 to 70	°C
Storage	– 65 to 150	°C
Power supply		
V_{CC}	7.0	V
V_{EE}	– 7.0	V
Logic levels		
TTL-high	5.5	V
TTL-low	– 0.5	V
ECL-high	0.0	V
ECL-low	0 to V_{EE}	V

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < 70°C, unless otherwise noted.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Resolution	4			bits
	Monotonicity	4			bits
NL	Nonlinearity		±1/16	±1/2	LSB
DNL	Differential nonlinearity		±1/8	±1	LSB
	Offset error (25°C) [1111] (BRT = 1)		±1/2	±1	LSB
	Gain error (25°C) [0000] (BRT = 1)		±1/2	±1	LSB
V_{CC}	Positive power supply (TTL mode) (ECL mode)	4.5 −0.1	5.0 0.0	5.5 0.1	V V
V_{EE}	Negative power supply (TTL or ECL mode)	−4.75	−5.0	−5.5	V
I_{CC}	Positive supply current		15	25	mA
I_{EE}	Negative supply current (NE5150) (NE5151)		175 145	210 175	mA mA
	Analog voltage range (ZS to FS)		603		mV
	Gain tracking (any two channels)			±1/4	LSB
	Least significant bit		40.2		mV
EWH	Enhanced white level absolute (25°C)		0		mV
BS	Bright shift (25°C) (0 to 1)		71.4		mV
EBL	Enhanced blanking level absolute (25°C)		−674		mV
ESY	Enhanced sync level absolute (25°C)		−960		mV
R_O	Output resistance (25°C)	67.5	75.0	82.5	Ω
V_{IH}	TTL logic input high	2.0			V
V_{IL}	TTL logic input low			0.8	V
I_{IH}	TTL logic high input current (V_{IN} = 2.4V)			20	μA
I_{IL}	TTL logic low input current (V_{IN} = 0.4V)			−1.6	mA
V_{IH}	ECL logic input high	−1.13			V
V_{IL}	ECL logic input low			−1.48	V
I_{IH}	ECL logic high input current (V_{IN} = −0.8V)			−1.0	mA
I_{IL}	ECL logic low input current (V_{IN} = −1.8V)			−1.0	mA

TEMPERATURE CHARACTERISTICS V_{CC} = 5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < 70°C

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	Offset TC[1]			±100	ppm/°C
	Gain TC[1]			±200	ppm/°C
	Gain tracking TC (any two channels)			±50	ppm/°C
	Enhanced white level TC[1]			±100	ppm/°C
	Bright shift TC			±200	ppm/°C
	Enhanced blanking level TC			±300	ppm/°C
	Enhanced sync level TC			±300	ppm/°C
	Output resistance TC			+1000	ppm/°C

NOTE:
1. Normalized to full scale (603mV).

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V (TTL), 0V (ECL), V_{EE} = −5V, 0°C < T_A < 70°C

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{MAX}	Maximum operating frequency (NE5150)	80			MHz
t_{WAS}	Write address setup (NE5150)		6		nsec
t_{WAH}	Write address hold (NE5150)		0		nsec
t_{WDS}	Write data setup (NE5150)		6		nsec
t_{WDH}	Write data hold (NE5150)		0		nsec
t_{WEW}	Write enable pulse width (NE5150)		6		nsec
t_{RCS}	Read composite[1] setup (NE5150)		4		nsec
t_{RCH}	Read composite[1] hold (NE5150)		2		nsec
t_{RAS}	Read address setup (NE5150)		8		nsec
t_{RAH}	Read address hold (NE5150)		0		nsec
t_{RSW}	Read strobe pulse width (NE5150)		8		nsec
t_{RDD}	Read DAC delay (NE5150)		8		nsec
f_{MAX}	Maximum operating frequency (NE5151)	150			MHz
t_{CS}	Composite[1] hold (NE5151)		4		nsec
t_{CH}	Composite[1] setup (NE5151)		2		nsec
t_{DS}	Data-bits setup (NE5151)		4		nsec
t_{DH}	Data-bits hold (NE5151)		2		nsec
t_{SW}	Strobe pulse width (NE5151)		4		nsec
t_{DD}	DAC delay (NE5151)		8		nsec
t_R	DAC rise time (10–90%)		3		nsec
t_S	DAC full-scale settling time[2]		10		nsec
C_{OUT}	Output capacitance (each DAC)		10		pF
S_R	Slew rate		200		V/μsec
G_E	Glitch energy			30	pV-sec
PSRR	Power supply rejection ratio (to red, green or blue outputs)				
	V_{EE} at 1kHz		43		dB
	V_{EE} at 10MHz		28		dB
	V_{EE} at 50MHz		14		dB
	V_{CC} at 1kHz		80		dB
	V_{CC} at 10MHz		50		dB
	V_{CC} at 50MHz		36		dB

NOTES:
1. Composite implies any of the WHITE, BRIGHT, BLANK or SYNC signals.
2. Settling to ± 1/2 LSB, measured from STROBE 50% point (rising edge). This time includes the delay through the strobe input buffer and latch.

PIN DESCRIPTION — NE5150

Write enable inputs use negative-true logic while all other inputs are positive-true. All inputs operate synchronously with the positive edge-triggered strobe input. When V_{CC} is taken high (5V), all inputs are TTL compatible. When V_{CC} is grounded, all inputs are ECL compatible. All DAC's are complementary, so that all ones is the highest absolute voltage and all zeroes is the lowest. All ones is called zero scale (ZS) and all zeroes is called fullscale (FS). The analog output voltage is approximately 0V (ZS) to – 1V (SYNC).

Pins 1, 24, 23, 22: **DATA** bits D0 (MSB) through D3, used to input digital information to the memory during the write phase. During this phase, the data bits are presented to the internal latches (noninverted) and the DAC's will output the analog equivalent of the stored word, unless overridden by WHITE, BLANK or SYNC.

Pins 5, 4, 3, 2: **ADDRESS** lines A0 (MSB) through A3, used for selecting a memory address to write to or read from.

Pin 7: **WHITE** command. Presets the latches to all ones [1111] and outputs 0V absolute on all DAC's. Can be modified to – 71mV absolute when BRIGHT is taken low. Will be overridden by either a BLANK or SYNC command.

Pin 8: **BRIGHT** command. A low input here turns on an additional – 71mV (10 IRE unit) switch, shifting all other levels downward. Not overridden by any other input.

Pin 9: **BLANK** command. Presets the latches to all zeroes [0000] and turns on an additional – 71mV (10 IRE unit) switch. Absolute output is – 671mV. Can be modified another – 71mV to – 742mV absolute when BRIGHT is taken low. Will override WHITE, and will be overridden by SYNC.

Pin 10: **SYNC** command. Presets the latches to all zeroes [0000] and turns on the BLANK switch. Additionally turns on a – 286mV (40 IRE unit) switch in the green channel only. Absolute output is – 671mV for the red and blue channels, and – 957mV for the green channel. All levels can be shifted – 71mV by taking BRIGHT low. Overrides WHITE and BLANK.

Pins 11, 13, 15: **GREEN, RED, BLUE.** Analog outputs with 75-ohm internal termination resistors. Can directly drive 75-ohm cable and should be terminated at the display end of the line with 75 ohms. Output voltage range is approximately 0V to – 1V independent of whether the digital inputs are ECL or TTL compatible. All outputs are simultaneously affected by the WHITE, BLANK, or BRIGHT commands. Only the GREEN channel carries SYNC information.

NOTE:
There are 100 IRE units from WHITE to BLANK. One IRE unit is approximately 7.1mV. Full scale is 90 IRE units and 10 IRE units is 1/9 of fullscale (e.g., BRIGHT function).

Pins 19, 20, 21: $\overline{\text{WRITE}}_B$, $\overline{\text{WRITE}}_R$, $\overline{\text{WRITE}}_G$. Write enable commands for each of the three 16 x 4 memories. When all write commands are high, then the *READ* operation is selected. This is the normal display mode. To write data into memory, the write enable pin is taken low. Data D0–D3 will be written into address A0–A3 of *each* memory when its corresponding write enable pin goes low.

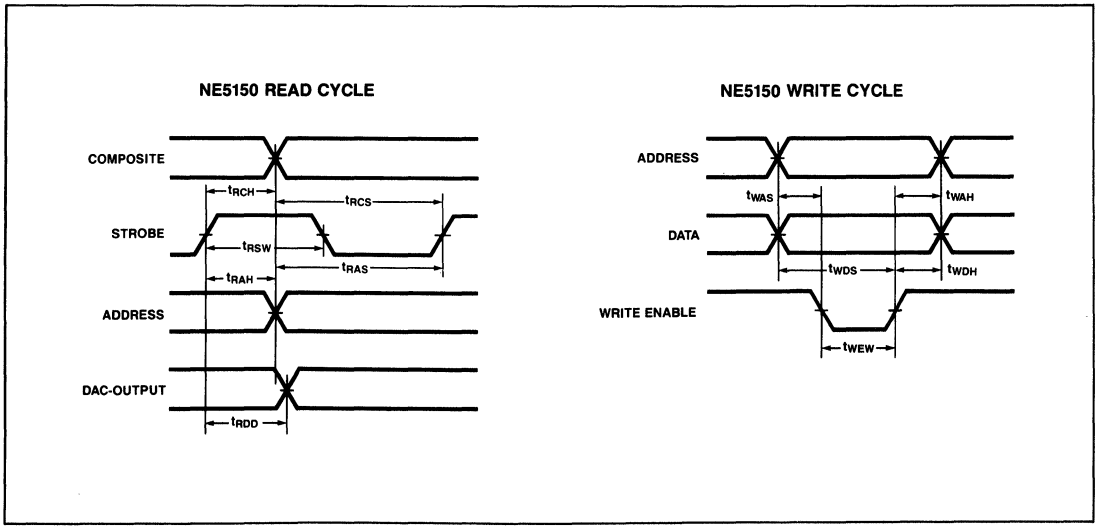
Pin 17: **STROBE.** The strobe signal is the main system clock and is used for resynchronizing digital signals to the DAC's. Preventing data skew eliminates glitches which would otherwise become visible color-distortions on a CRT display. The strobe command has no special drive requirements and is TTL or ECL compatible.

Pins 12, 16: A_{GND}, D_{GND}. Both **A**nalog and **D**igital ground carry a maximum of approximately 100mA of DC current. For proper operation, the difference voltage between A_{GND} and D_{GND} should be no greater than 50mV, preferably less.

Pin 14: V_{EE}. The negative power supply is the main chip power source. V_{CC} is only used for the TTL input buffers. As is usual, good bypassing techniques should be used. The chip itself has a good deal of power supply rejection — well up into the VHF frequency range — so no elaborate power supply filtering is necessary.

Pin 18: **N/C.** This unused pin should be tied high or low.

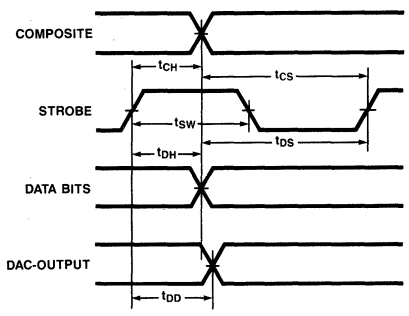
NE5150 TIMING DIAGRAMS



NE5151 PIN DESCRIPTIONS AND TIMING DIAGRAM

The eleven digital inputs D0–D3, A0–A3, $\overline{\text{WRITE}}$ G/R/B, and the unused pin 18 of the NE5150 are replaced in the NE5151 with the three 4-bit DAC digital inputs G0–G3, R0–R3, and B0–B3. All other pin functions (e.g., composite functions, power supplies, strobe, etc.) are identical to the NE5150.

NE5151 TIMING

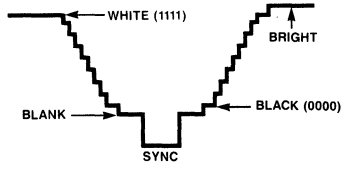


NE5150/NE5151 LOGIC TABLE

SYNC	BLANK	WHITE	BRIGHT	DATA	ADDRESS	OUTPUT	CONDITION
1	X	X	0	X	X	– 1031mV	SYNC[1]
1	X	X	1	X	X	– 960mV	Enhanced SYNC[1]
0	1	X	0	X	X	– 746mV	BLANK
0	1	X	1	X	X	– 674mV	Enhanced BLANK
0	0	1	0	X	X	– 71mV	WHITE
0	0	1	1	X	X	– 0mV	Enhanced WHITE
0	0	0	0	[0000]	Note 2	– 674mV	BLACK (FS)
0	0	0	1	[0000]	Note 2	– 603mV	Enhanced BLACK (EFS)
0	0	0	0	[1111]	Note 2	– 71mV	WHITE (ZS)
0	0	0	1	[1111]	Note 2	– 0mV	Enhanced WHITE (EZS)

NOTES
1. Green channel output only. RED and BLUE will output BLANK or Enhanced BLANK under these conditions.
2. For the NE5150 the DATA column represents the memory data accessed by the specific address. For the NE5151, the DATA is the direct digital inputs.

COMPOSITE VIDEO WAVEFORM



Six Function Analog Memory; Microcomputer Controlled

SAB3013

The SAB3013 is a MOS N-channel integrated circuit which provides 6 analogue memories controlled by a microcomputer.

Features

- 6-function analogue memory; D/A converter with 6-bit resolution.
- The output of the analogue values is pulse-width modulated with adjustable repetition rate (max. 21,8 kHz).
- Microcomputer-adapted asynchronous serial interface for data input (CBUS).
- Parallel operation of up to four SAB3013 circuits is possible.

4

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}	0 to	+70 °C
Clock frequency	f_{CLK}	<	1,4 MHz
Supply current; V_{DD} = 5 V; I_O = 0; T_{amb} = 25 °C	I_{DD}	typ.	15 mA

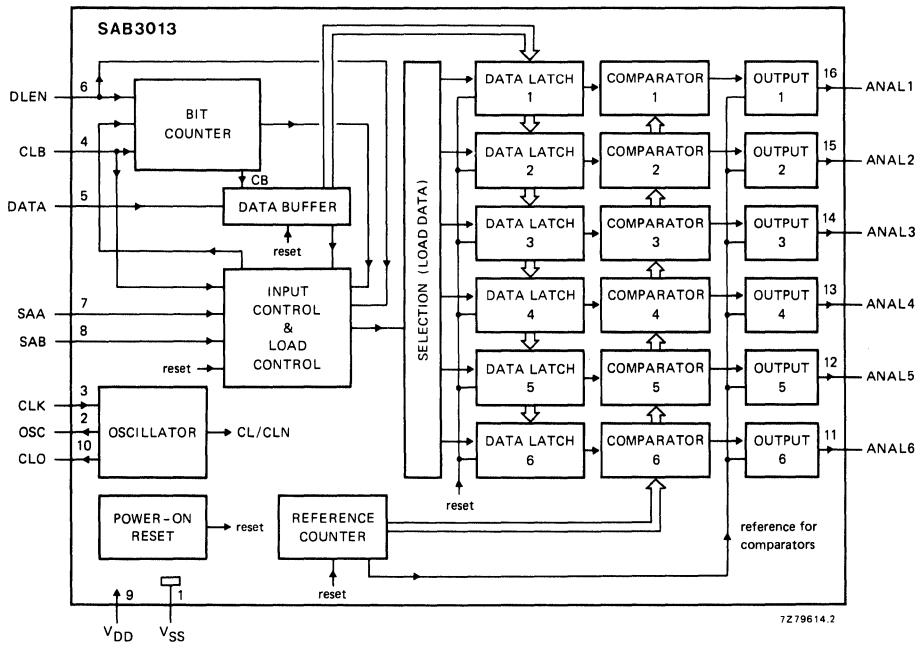


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

Six Function Analog Memory; Microcomputer Controlled

SAB3013

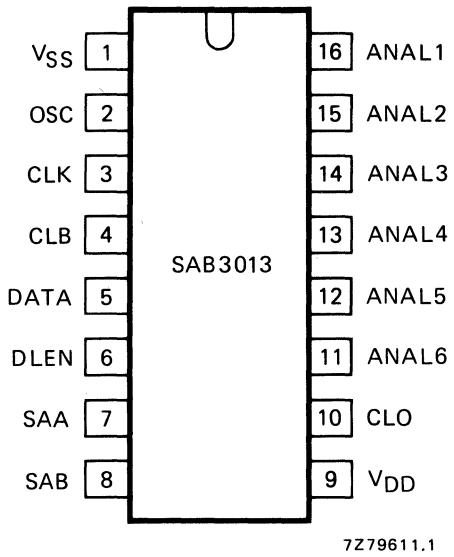


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)	
9	V_{DD}	positive supply	
4	CLB	asynchronous clock pulse	CBUS
5	DATA	data input	CBUS
6	DLEN	data line enable input	CBUS
7	SAA	address inputs	
8	SAB	address inputs	
2	OSC	oscillator output	
3	CLK	oscillator input (Schmitt-trigger)	
16	ANAL1	analogue outputs	
15	ANAL2	analogue outputs	
14	ANAL3	analogue outputs	
13	ANAL4	analogue outputs	
12	ANAL5	analogue outputs	
11	ANAL6	analogue outputs	
10	CLO	buffered oscillator output	

GENERAL DESCRIPTION

The SAB3013 is designed to deliver analogue values in microcomputer-controlled television receivers and radio receivers. The circuit comprises an analogue memory and D/A converter for 6 analogue functions with a 6-bit resolution for each. The information for the analogue memory is transfered by the microcomputer via an asynchronous serial data bus.

The SAB3013 accomplishes a word format recognition, so it is able to operate one common data bus together with circuits having different word formats.

The data word of the microcomputer used for the SAB3013 consists of information for addressing the appropriate SAB3013 circuit (2-bits), for addressing the analogue memories concerned (3-bits) and processing of the wanted analogue value (6-bits). The address of the circuit is externally programmable via two inputs. It is possible to address up to four SAB3013 circuits via one common bus.

The built-in oscillator can be used for a frequency between 30 kHz and 1,4 MHz. The analogue values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ (max. 21,8 kHz at f_{CLK} = 1,4 MHz), and the analogue values are determined by the ratio of the HIGH-time and the cycle time. A d.c. voltage proportional to the analogue value is obtained by means of an external integration network (low-pass filter).

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance to the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to +7,5	V
Input voltage range	V_I	−0,3 to +15	V
Input current	$\pm I_I$	max. 100	μA
Output voltage (open drain outputs)	V_O	V_{SS} to 15	V
Output current (open drain/push-pull outputs)	$\pm I_O$	max. 10	mA
Power dissipation per output	P_O	max. 25	mW
Total power dissipation per package	P_{tot}	max. 250	mW
Operating ambient temperature range	T_{amb}	0 to +70	°C
Storage temperature range	T_{stg}	−20 to +125	°C

CHARACTERISTICS

V_{SS} = 0; T_{amb} = 0 to +70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltage	V_{DD}	4,5	5	5,5	V	
Supply current	I_{DD}	–	–	35	mA	V_{DD} = 5,5 V
Inputs DATA, CLB, DLEN, SAA, SAB						
Input voltage LOW	V_{IL}	−0,3	–	0,8	V	
Input voltage HIGH	V_{IH}	2,0	–	12	V	
Input leakage current	I_{IR}	–	–	1	μA	V_I = −0,3 to +12 V
Outputs ANAL1 to ANAL6 (open drain)						
Output voltage LOW	V_{OL}	–	–	0,7	V	I_O = 6 mA
Output leakage current	I_{OR}	–	–	20	μA	V_{OH} = 15 V
Load capacitance	C_L	–	–	1000	pF	
Input CLK						
Input voltage LOW	V_{IL}	−0,3	–	0,8	V	
Input voltage HIGH	V_{IH}	3,5	–	12	V	
Input leakage current	I_{IR}	–	–	1	μA	V_I = −0,3 to 12 V
Pulse duration HIGH	t_{WH}	355	–	–	ns	
Pulse duration LOW	t_{WL}	355	–	–	ns	
Output CLO						
Output voltage LOW	V_{OL}	–	–	0,8	V	I_O 500 μA
Output voltage HIGH	V_{OH}	3,5	–	–	V	$-I_O$ = 100 μA
Inputs DATA, CLB						
Pulse duration HIGH	t_{WH}	450	–	–	ns	} see Fig. 3
Pulse duration LOW	t_{WL}	450	–	–	ns	
Input frequency CLB	f_{CLB}	0	–	1	MHz	
Internal oscillator CLK/OSC						
External resistor	R	27	–	1000	kΩ	
External capacitor	C	27	–	1000	pF	
Clock frequency	f_{CLK}	0,7	1,0	1,4	MHz	R = 27 kΩ; C = 27 pF
Frequency for external oscillator	f_{CLK}	0,03	–	1,4	MHz	

CHARACTERISTICS (continued)

V_{SS} = 0; T_{amb} = 0 to +70 °C; V_{DD} = 4,5 to 5,5 V; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Timing (see Fig. 3)						
Data set-up time DATA → CLB	t_{SUDA}	800	–	–	ns	measured with a voltage swing of min. V_{IH}–V_{IL}
Data hold time DATA → CLB	t_{HDDA}	300	–	–	ns	
Enable set-up time DLEN → CLB	t_{SUEN}	400	–	–	ns	
Disable set-up time CLB → DLEN	t_{SUDI}	400	–	–	ns	
Set-up time DLEN → CLB (load pulse)	t_{SULD}	1000	–	–	ns	

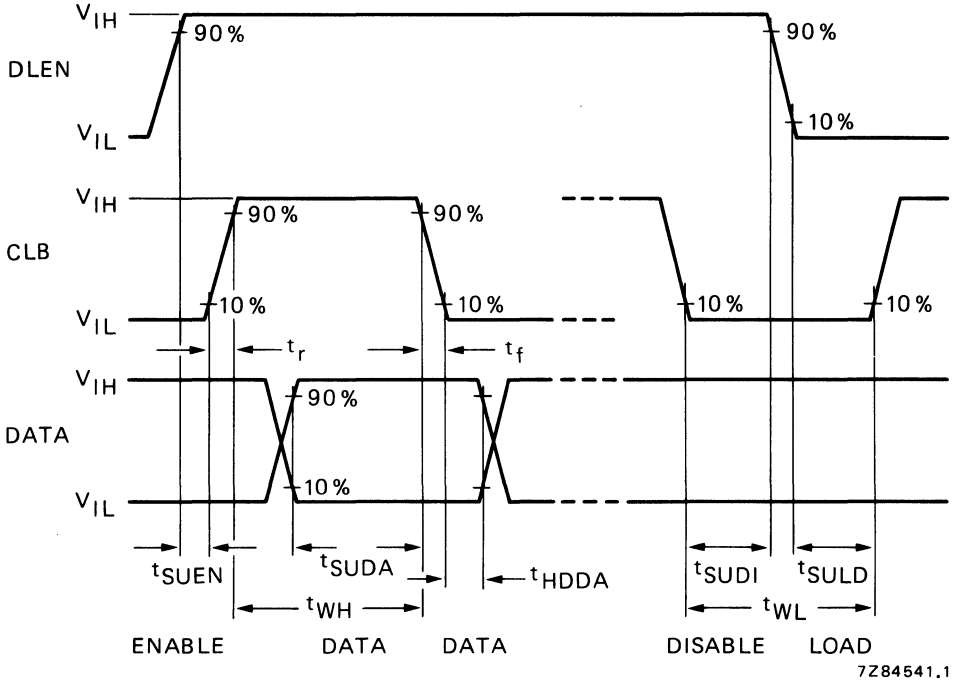


Fig. 3 CBUS timing.

OPERATION DESCRIPTION

The data input is achieved serially via the inputs DATA, DLEN and CLB. Clock pulses have to be applied at input CLB for data processing at input DATA. Data processing is only possible when DLEN = HIGH. The data from the data buffer is loaded directly into the output latch on receipt of a load pulse at input CLB (DLEN = LOW), provided the following conditions are met:

- 12 clock pulses must be received at input CLB (word format control) during transmission (DLEN = HIGH).
- The start-bit must be LOW.
- The system address bits must be A = SAA and B = SAB.
- The analogue address must be valid.

The data word for the SAB3013 consists of the following bits (see Fig. 4):

1 start-bit
2 system address bits (A and B)
3 address bits for selection of the required analogue memory
6 data bits for processing the analogue value

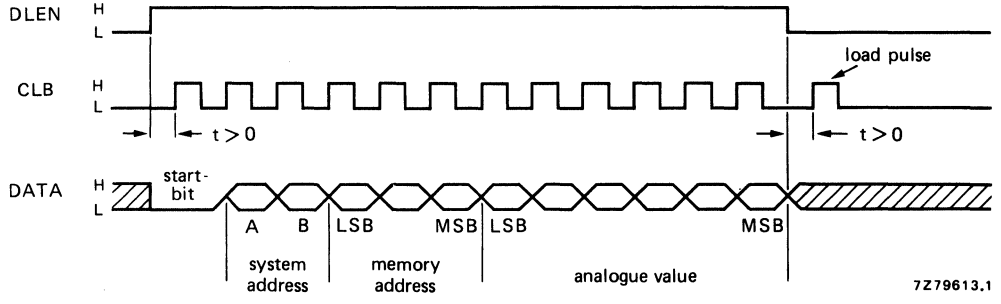


Fig. 4 Waveforms showing a CBUS transmission.

ADDRESS inputs (SAA, SAB)

The address of the SAB3013 is programmed at the inputs SAA and SAB. These inputs must be defined and not left open-circuit.

Reset

The circuit generates internally a reset-cycle with a duration of one clock cycle after switching on the supply. If a spike on the supply is likely to destroy data, a reset signal will be generated. All analogue memories are set to 50% (analogue value 32/64) after the reset cycle. The supply voltage rise dV_{DD}/dt must be max. 0,5 V/μs and min. 0,2 V/μs.

Oscillator inputs (CLK, OSC)
The oscillator frequency is determined by the external circuitry connected to the terminals CLK and OSC as shown in Fig. 5. Instead of this circuitry an externally generated oscillator signal can be connected to input CLK.

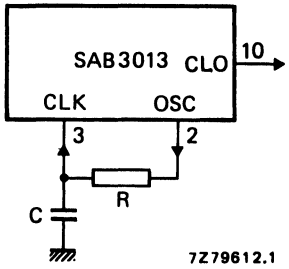


Fig. 5 Application advice for the oscillator.

At output CLO a buffered oscillator signal is available for control of other circuits.

For f_{CLK} = 0,7 to 1,4 MHz;
R = 27 kΩ; C = 27 pF.

4

Analogue outputs (ANAL1 to ANAL6)
The analogue values are generated as a pulse pattern with a repetition rate of $f_{CLK}/64$ at the outputs ANAL1 to ANAL6. The analogue value is determined by the ratio of the HIGH-time and the cycle time (values between 1/64 and 64/64 can be obtained).

Table 1 Addressing of the analogue data registers

R_A LSB	R_B	R_C MSB	addressing
0	0	0	not valid
1	0	0	ANAL1
0	1	0	ANAL2
1	1	0	ANAL3
0	0	1	ANAL4
1	0	1	ANAL5
0	1	1	ANAL6
1	1	1	not valid

Table 2 Correlation of analogue value to analogue output signal

analogue value	binary input data LSB ... MSB						duty cycle 'low'	duty cycle 'high'
lowest value	0	0	0	0	0	0	63/64	1/64
	1	0	0	0	0	0	62/64	2/64
power-on reset value	1	1	1	1	1	0	32/64	32/64
highest value	0	1	1	1	1	1	1/64	63/64
	1	1	1	1	1	1	0	64/64

8-Bit Multiplying DAC | PNA7518

GENERAL DESCRIPTION

The PNA7518 is a NMOS 8-bit multiplying digital-to-analogue converter (DAC) designed for video applications. The device converts a digital input signal into a voltage-equivalent analogue output at a sampling rate of 30 MHz.

The input signal is latched, then fed to a decoder which switches a transfer gate array (1 out of 256) to select the appropriate analogue signal from a resistor chain. Two external reference voltages supply the resistor chain.

The input latches are positive-edge triggered. The output impedance is approximately 0,5 kΩ depending on the applied digital code. An additional operational amplifier is required for the full bandwidth. Two's complement is selected when STC (pin 11) is HIGH or is not connected.

Features

- TTL input levels
- Positive-edge triggered
- Analogue voltage output at 30 MHz sampling rate
- Binary or two's complement input
- Output voltage accuracy to within ± ½ of the input LSB

QUICK REFERENCE DATA

Supply voltage range (pin 16)	V_{DD}	4,5 to 5,5	V
Supply current (pin 16)	I_{DD}	typ. 50	mA
Reference voltage LOW (pin 2)	V_{refL}	min. 0	V
Reference voltage HIGH (pin 9)	V_{refH}	max. 2	V
Linearity at R_L = 200 kΩ; V_O = 2 V (peak-to-peak value)		± ½	LSB
Bandwidth (−3 dB) at C_L = 6 pF	B	min. 12	MHz
Clock frequency	f_{CLK}	max. 30	MHz
Total power dissipation	P_{tot}	typ. 300	mW

Applications

- Video data conversion
- CRT displays
- Waveform/test signal generation
- Colour/black-and-white graphics

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38WE-1).

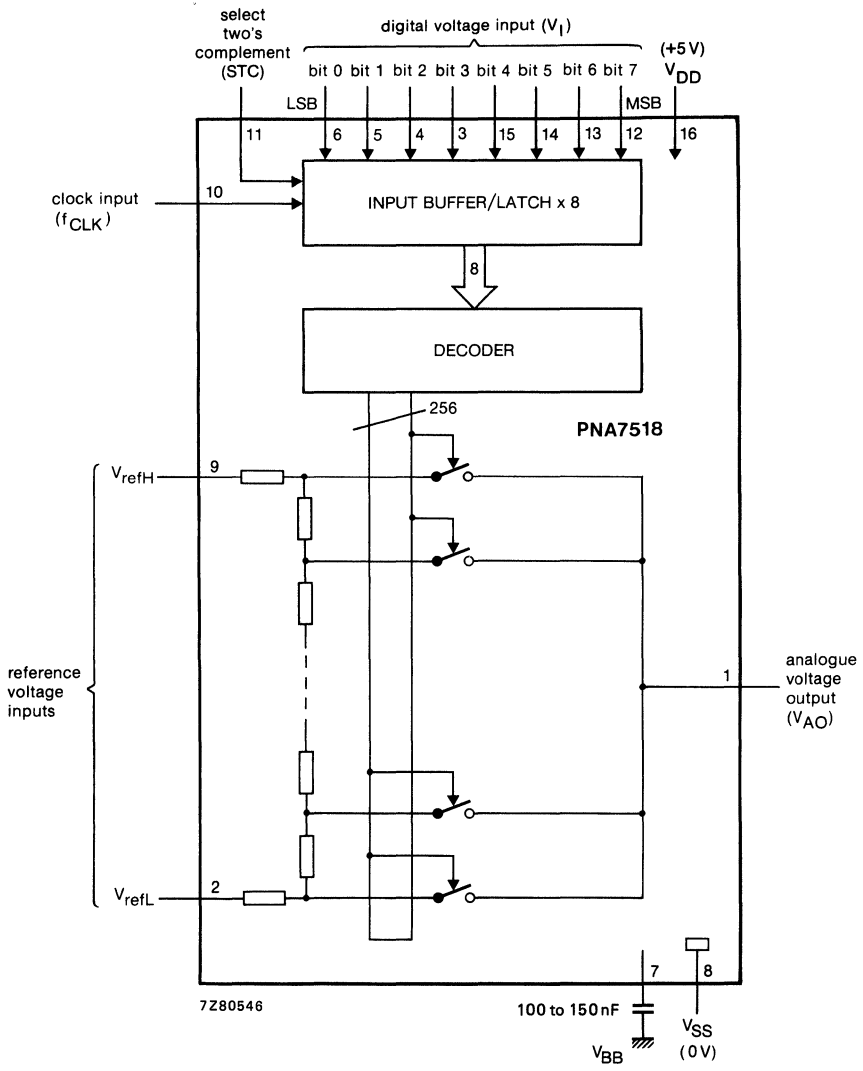


Fig. 1 Block diagram.

8-Bit Multiplying DAC | PNA7518

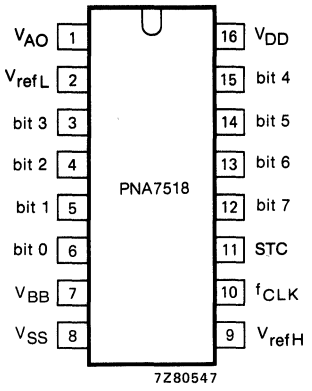


Fig. 2 Pinning diagram.

PINNING

1	V_{AO}	analogue output voltage
2	V_{refL}	reference voltage LOW
3	bit 3	digital voltage inputs (V_I)
4	bit 2	
5	bit 1	
6	bit 0	least-significant bit (LSB)
7	V_{BB}	back bias
8	V_{SS}	ground
9	V_{refH}	reference voltage HIGH
10	f_{CLK}	clock input
11	STC	select two's complement
12	bit 7	most-significant bit (MSB)
13	bit 6	digital voltage inputs (V_I)
14	bit 5	
15	bit 4	
16	V_{DD}	positive supply voltage

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 16)	V_{DD}	−0,5 to + 7 V
Input voltage range (pins 3, 4, 5, 6, 11, 12, 13, 14 and 15)	V_I	−0,5 to + 7 V
Output voltage range (pin 1)	V_{AO}	−0,5 to + 7 V
Total power dissipation	P_{tot}	max. 400 mW
Storage temperature range	T_{stg}	−65 to + 150 °C
Operating ambient temperature range	T_{amb}	0 to + 70 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

CHARACTERISTICS

V_{DD} = 4,5 to 5,5; V_{SS} = 0 V; C_{BB} = 100 nF; T_{amb} = 0 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	4,5	5	5,5	V
Supply current	I_{DD}	–	50	80	mA
Reference voltages					
Reference voltage LOW (pin 2)	V_{refL}	–0,1	–	+ 2,1	V
Reference voltage HIGH (pin 9)	V_{refH}	–0,1	–	+ 2,1	V
Reference ladder	R_{ref}	150	230	300	Ω
Inputs					
Digital input levels (TTL) (note 1)					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	5,25	V
input leakage current	I_{LI}	–	–	10	μA
Clock input (pin 10)					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	5,25	V
input leakage current	I_{LI}	–	–	10	μA
frequency	f_{CLK}	1	–	30	MHz
pulse width HIGH	t_{PWH}	10	–	–	ns
pulse width LOW	t_{PWL}	10	–	–	ns
input rise time at f_{CLK} = 30 MHz	t_r	–	–	3	ns
input fall time at f_{CLK} = 30 MHz	t_f	–	–	3	ns
Output					
Analogue voltage output (pin 1) at R_L = 200 kΩ)	V_{AO}	0	–	2	V
Bandwidth (–3 dB) at C_L = 6 pF	B	–	12	–	MHz
Switching characteristics (Fig. 3)					
Data set-up time	$t_{SU;DAT}$	3	–	–	ns
Data hold time	$t_{HD;DAT}$	4	–	–	ns
Propagation delay time, input to output	t_{PD}	t_{CLK} + 15	t_{CLK} + 22	t_{CLK} + 30	ns
Settling time: 10 to 90% full-scale change; C_L = 6 pF; R_L = 200 kΩ	t_{S1}	–	13	20	ns
Settling time to ± 1 LSB; C_L = 6 pF; R_L = 200 kΩ	t_{S2}	–	40	–	ns

parameter	symbol	min.	typ.	max.	unit
Output transients (glitches) (note 2 and Fig. 3)					
Glitch occurring at step 7F-80 (HEX):					
maximum amplitude for 1 LSB change area	V_g	–	3	–	LSB
		–	23	–	LSB.ns
Glitch occurring at step 00-AA (HEX):					
maximum amplitude for 1 LSB change area	V_g	–	5	–	LSB
		–	41	–	LSB.ns
Influence of clock frequency (note 2)					
Cross-talk at 2 x f_{CLK}					
amplitude		–	2	–	LSB
area		–	8	–	LSB.ns

Notes to the characteristics

1. Inputs bit 0 to bit 7 are positive-edge triggered and STC.
2. Measured at V_{refH}-V_{refL} = 2,0 V; 1 x LSB = 7,8 mV. The energy equivalent of output transients is given as the area contained by the graph of output amplitude (LSB) against time (ns). The glitch area is independent of the value of V_{ref}. Glitch amplitudes and clock cross-talk can be reduced by using a shielded printed circuit board.

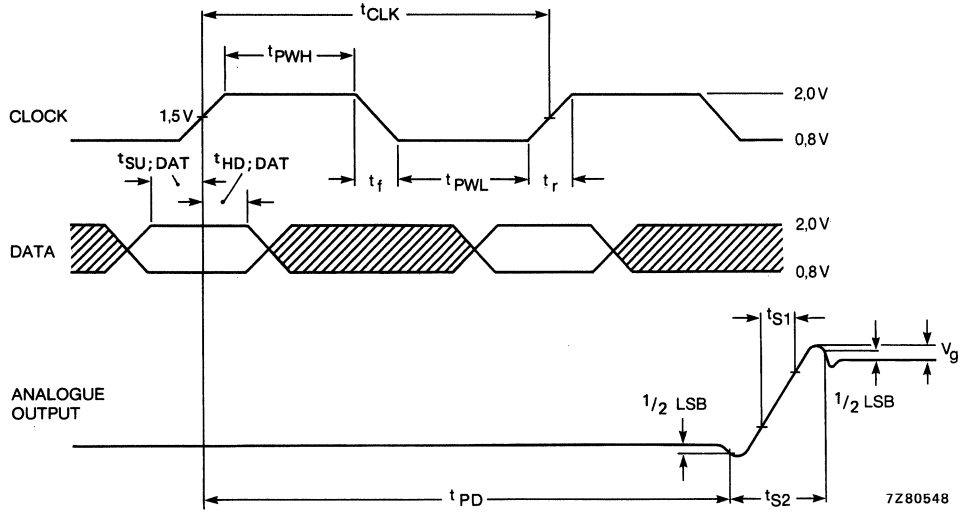


Fig. 3 Switching characteristics.

14-Bit DAC (Serial Output) TDA1540D, P

GENERAL DESCRIPTION

The TDA1540 is a monolithic integrated 14-bit digital to analogue converter (DAC). It incorporates a 14-bit input shift register with output latches, binary weighted current sources with switches and a reference source.

The IC features an improved switch circuitry which eliminates the need for a deglitcher circuit at the output. This results in a signal-to-noise ratio of typical 85 dB in the audio band.

QUICK REFERENCE DATA

Supply voltages				
pin 4	V_{P1}	typ.	5	V
pin 7	V_{N1}	typ.	−5	V
pin 11	V_{N2}	typ.	−17	V
Signal-to-noise ratio (full scale sine-wave) at analogue output (pin 22)	S/N	typ.	85	dB
Non-linearity at T_{amb} = −20 to + 70 °C		typ.	½ LSB	
Current settling time	t_{cs}	typ.	0.5	μs
Maximum input bit rate at data input (pin 1)	BR_{max}	min.	12	Mbit/s
Maximum clock frequency at clock input (pin 28)	$f_{cl\,max}$	min.	12	MHz
Full scale temperature coefficient at analogue output (pin 22)	TC_{FS}	typ.	$\pm 30 \cdot 10^{-6}$	K^{-1}
Operating ambient temperature range	T_{amb}		−20 to + 70	°C
Total power dissipation	P_{tot}	typ.	350	mW

PACKAGE OUTLINES

TDA1540D: 28-lead DIL; ceramic (cerdip) (SOT-135A).
TDA1540P: 28-lead DIL; plastic (SOT-117BE).

FUNCTIONAL DESCRIPTION

The binary weighted current sources are obtained by a combination of a passive divider and a time division concept. Figure 1a gives the diagram of one divider stage. The total emitter current 4 I of the passive divider is divided into four more or less equal output currents.

The output currents of the passive divider are now interchanged during equal time intervals generated by means of a shift register. The average output currents are exactly equal as a result of this operation. A ripple on the output current, caused by a mismatch of the passive divider, is filtered by an a.c. low-pass filter, requiring an external filter capacitor.

The outputs of the dividers are combined to obtain the output currents I ($\bar{I}_1$), I ($\bar{I}_2$) and 2I ($\bar{I}_3$) (see Fig. 1b). The current of the most significant bit is generated by an on-chip reference source. A binary weighted current network is formed by cascading the current division stages (see Fig. 2).

The interchanging pulses are generated by an on-chip oscillator and a 4-bit shift register. The binary currents are switched to the current output (pin 22) via diode-transistor switching stages; therefore, the voltage on the output pin must be 0 V ± 10 mV. The output current can be converted into a voltage by means of a summing amplifier.

Figure 3 represents the data input format, and an application circuit is given in Fig. 4.

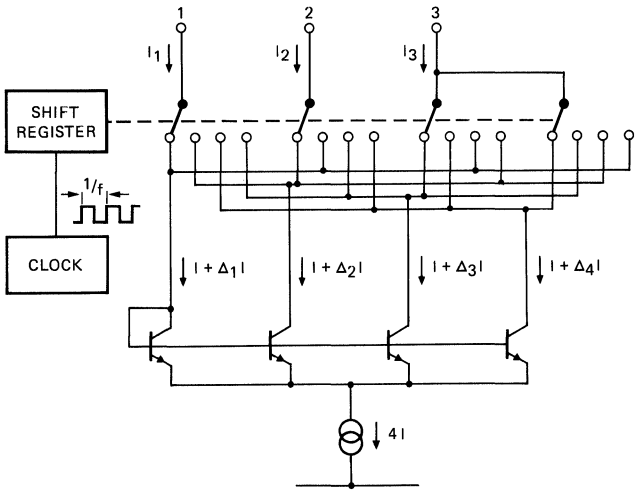


Fig. 1a Circuit diagram of one divider stage.

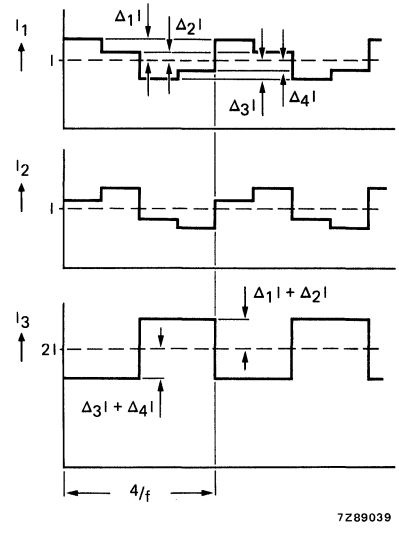


Fig. 1b Waveforms showing output currents I_1, I_2 and I_3 of Fig. 1a.

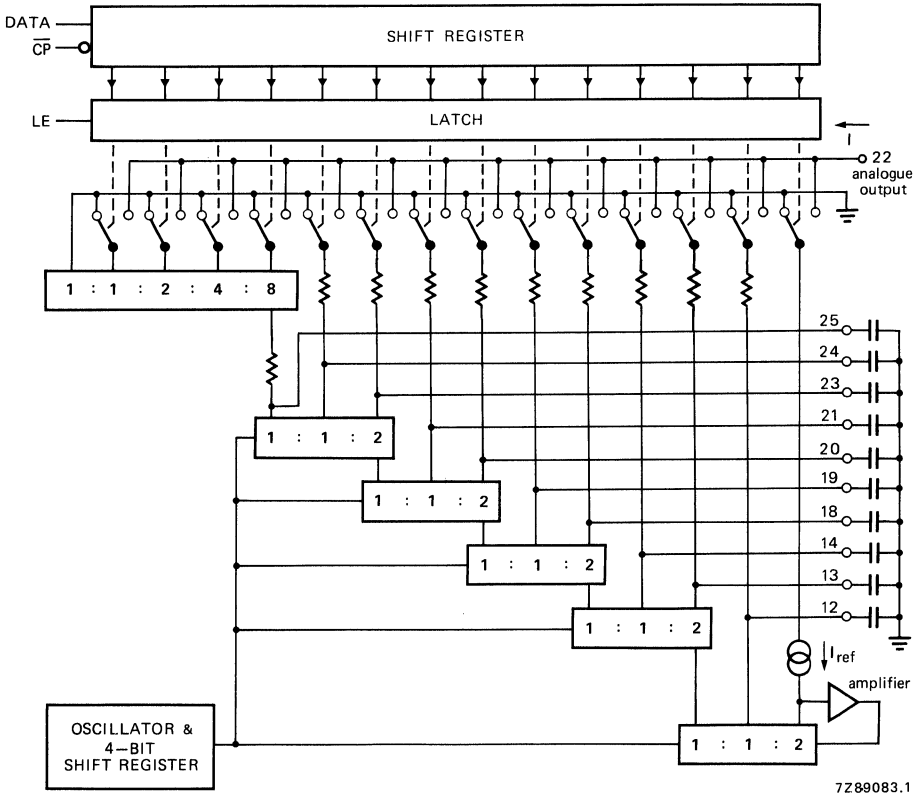


Fig. 2 Functional diagram showing cascading of current division stages.

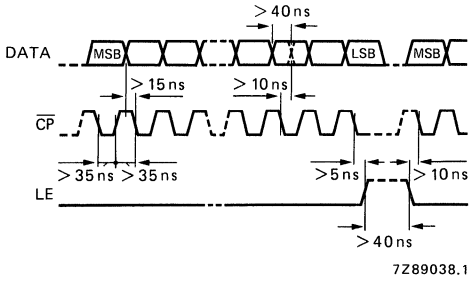


Fig. 3 Format of input signals.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages with respect to GND (pin 6)				
at pin 4	V_{P1}	max.	12	V
at pin 7	V_{N1}	max.	−12	V
at pin 11	V_{N2}	max.	−20	V
at pin 4 with respect to pin 11	$V_{P1}-V_{N2}$	max.	32	V
at pin 7 with respect to pin 11	$V_{N1}-V_{N2}$		−1 to + 20	V
Total power dissipation	P_{tot}	max.	600	mW
Storage temperature range	T_{stg}		−55 to + 125	°C
Operating ambient temperature range	T_{amb}		−25 to + 80	°C

CHARACTERISTICS (see application circuit Fig. 4)

T_{amb} = 25 °C; at typical supply voltages; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages with respect to GND (pin 6)					
at pin 4	V_{P1}	3	5	7	V
at pin 7	V_{N1}	−4.7	−5	−7	V
at pin 11	V_{N2}	−16.5	−17	−18	V
Supply currents					
at pin 4*	I_{P1}	–	12	14	mA
at pin 7	I_{N1}	–	−20	−24	mA
at pin 11	I_{N2}	–	−11	−13	mA
Power dissipation					
Total power dissipation	P_{tot}	–	350	410	mW
Temperature					
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

* When the output current is $\frac{1}{2}I_{FS}$ (½ full scale output current).

parameter	symbol	min.	typ.	max.	unit
Data input DATA (pin 1)					
Input voltage HIGH	V_{IH}	2.0	–	7.0	V
Input voltage LOW	V_{IL}	0	–	0.8	V
Input current HIGH at V_{IH}	I_{IH}	–	–	50	μA
Input current LOW at V_{IL}	$-I_{IL}$	–	–	0.2	mA
Maximum input bit rate	BR_{max}	12	–	–	Mbits/s
Latch enable input LE (pin 2)					
Clock input $\overline{CP}$ (pin 28)					
Input voltage HIGH	V_{IH}	2.0	–	7.0	V
Input voltage LOW	V_{IL}	0	–	0.8	V
Input current HIGH at V_{IH}	I_{IH}	–	–	50	μA
Input current LOW at V_{IL}	$-I_{IL}$	–	–	0.2	mA
Maximum clock frequency	f_{CPmax}	12	–	–	MHz
Oscillator (pins 8 and 9)					
Oscillator frequency at C_{8-9} = 820 pF	f_{osc}	100	160	200	kHz
Analogue output I_{out} (pin 22)					
Output voltage compliance	V_{OC}	−10	–	+ 10	mV
Full scale current	I_{FS}	3.8	4.0	4.2	mA
Zero scale current	$\pm I_{ZS}$	–	–	100	nA
Full scale temperature coefficient T_{amb} = −20 to + 70 °C	TC_{FS}	–	$\pm 30 \times 10^{-6}$	–	K^{-1}
Settling time to ± ½LSB all bits on or off	t_{cs}	–	0.5	–	μs
Signal-to-noise ratio*	S/N	80	85	–	dB

* Signal-to-noise ratio within 20 Hz and 20 kHz of a 1 kHz full scale sinewave, generated at a sample rate of 44 kHz.

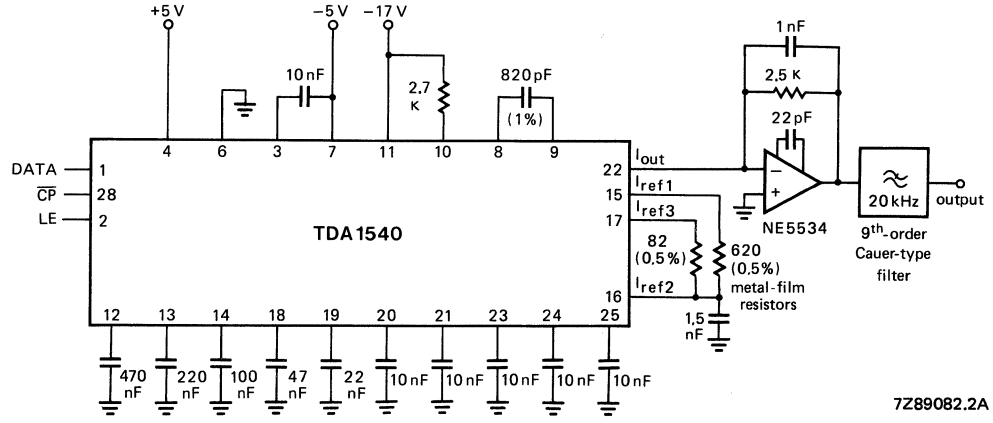


Fig. 4 Application circuit.

PINNING

1	DATA	data input
2	LE	latch enable input
3	V_{ref1}	voltage reference
4	V_{P1}	positive supply
5	i.c.*	frequency compensation on-chip operational amplifier
6	GND	ground
7	V_{N1}	negative supply
8	OSC1	oscillator capacitor
9	OSC2	oscillator capacitor
10	V_{ref2}	voltage reference
11	V_{N2}	negative supply
12	C1	decoupling binary weighted current sources
13	C2	decoupling binary weighted current sources
14	C3	decoupling binary weighted current sources
15	I_{ref1}	current reference sources
16	I_{ref2}	current reference sources
17	I_{ref3}	current reference sources
18	C4	decoupling binary weighted current sources
19	C5	decoupling binary weighted current sources
20	C6	decoupling binary weighted current sources
21	C7	decoupling binary weighted current sources
22	I_{out}	analogue output
23	C8	decoupling binary weighted current sources
24	C9	decoupling binary weighted current sources
25	C10	decoupling binary weighted current sources
26	i.c.*	voltage reference
27	i.c.*	voltage reference
28	$\overline{CP}$	clock pulse input

* i.c.: internally connected.

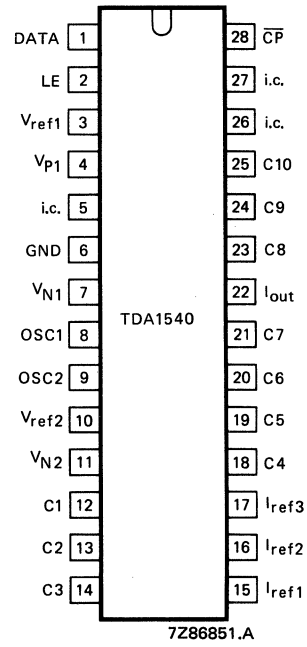


Fig. 5 Pinning diagram.

Selector Guide

COMPARATORS

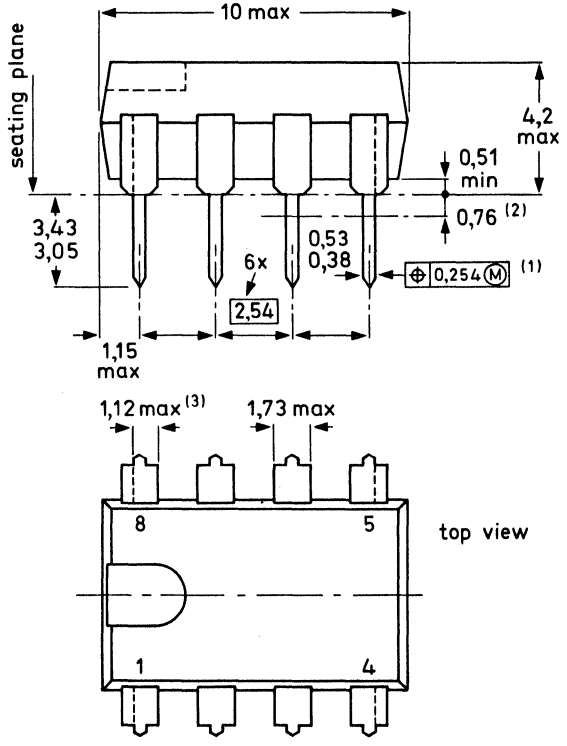
DEVICE	COM-PLEXITY	TEMP. RANGE*	MAX. INP. OFFSET VOLT (mV)	MAX. INP. CURRENT BIAS (μA)	MAX. INP. CURRENT OFFSET (μA)	SUPPLY VOLTAGE (V)	RESPONSE TIME (Typ.) (ns)	COMMON MODE VOLTAGE RANGE (V)	OUTPUT VOLTAGE V_{OL} Max. (V)	OUTPUT VOLTAGE V_{OH} Min. (V)	OUTPUT STRUCTURE	VOLTAGE GAIN (Typ.) V/mV	TTL FANOUT	MAX. DIFF. INPUT VOLTAGE (V)
LM111[1]	Single	M	4.00	0.15	0.02	±15	200	±14	0.4		O.C.	200	5	±30
LM211	Single	I	4.00	0.15	0.02	to	200	±14	0.4		O.C.	200	5	±30
LM311	Single	C	10.0	0.30	0.07	+5 and GND	200	±14	0.4		O.C.	200	5	±30
NE527[2]	Single	C	10.0	4.00	1.0	±5 to ±10	16	±5	0.5	2.7	TTL		5	±5
SE527	Single	M	6.00	4.00	1.00	and GND	16	±5	0.5	2.5	TTL		5	±5
NE529[5]	Single	C	10.0	50.0	15.0	±5 to ±10	12	±5	0.5	2.7	TTL		5	±5
SE529	Single	M	6.00	36.0	9.00	and GND	12	±5	0.5	2.5	TTL		5	±5
LM119[3]	Dual	M	7.00	1.00	0.10	±15	80	±13	0.4		O.C.	40	2	±5
LM219	Dual	I	7.00	1.00	0.10	to	80	±13	0.4		O.C.	40	2	±5
LM319	Dual	C	10.0	1.20	0.30	±5 and GND	80	±13	0.4		O.C.	40	2	±5
LM193[3]	Dual	M	9.00	0.30	0.10	±1 to ±18	1300	0 to V_S-2	0.7		O.C.	200	2	36
LM293	Dual	I	9.00	0.40	0.15	or	1300	0 to V_S-2	0.7		O.C.	200	2	36
LM393	Dual	C	9.00	0.40	0.15	+2 to +36 GND	1300	0 to V_S-2	0.7		O.C.	200	2	36
LM2903	Dual	I	15.0	0.50	0.20		1300	0 to V_S-2	0.7		O.C.	100	2	36
SE/NE521[4]	Dual	M/C	15/10.0	40.0	12.0	+5, −5, GND	8	±3	0.5	2.7	TTL		12	±6
SE/NE522	Dual	M/C	15/10.0	40.0	12.0	+5, −5, GND	10	±3	0.5		O.C.		12	±6
LM139[3]	Quad	M	9.00	0.30	0.10		1300	0 to V_S-2	0.7		O.C.	200	2	36
LM239	Quad	I	9.00	0.40	0.15	±1 to ±18 or	1300	0 to V_S-2	0.7		O.C.	200	2	36
LM339	Quad	C	9.00	0.40	0.15	+2 to +36	1300	0 to V_S-2	0.7		O.C.	200	2	36
LM2901	Quad	I	15.0	0.50	0.20		1300	0 to V_S-2	0.7		O.C.	100	2	36
MC3302[3]	Quad	I	40.0	1.00	0.30	+2 to +28 GND	2000	0 to V_S-2	0.7		O.C.	100	2	28

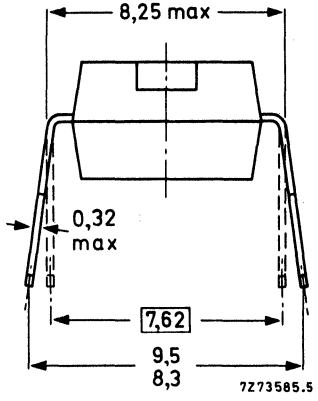
Notes:
1. With strobe, will work from single supply.
2. Complementary output gates with individual strobes.
3. Will operate from single or dual supplies.
4. Ultra-high speed.

*Temperature Range
I = Industrial
C = Commercial
M = Military

4

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97A)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

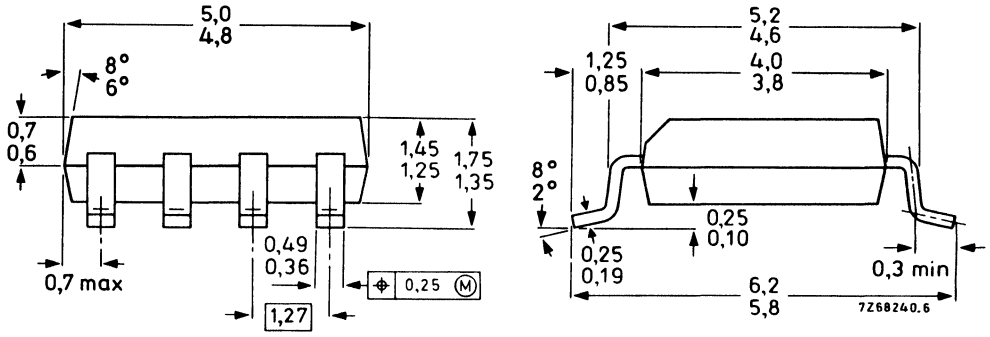
2. By dip or wave

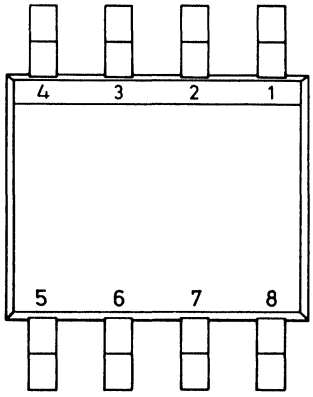
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96A)





top view

Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

DEVELOPMENT SAMPLE DATA

4

SOLDERING

1. Soldering iron or pulse heated solder tool

Apply the heating tool to the flat part of the pin only.
Limit the contact time to maximum 10 seconds up to 300 °C, or 5 seconds up to maximum 400 °C.
When using the proper tools, up to 20 pins (at one side of the device) can be soldered in one operation with 2 to 5 seconds and 270 to 320 °C.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C. The permissible total time of immersing the whole package in the bath is 10 seconds, if it is allowed to cool down to less than 150 °C within 6 seconds.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.
If the vertical part of the pin needs heating, reduce the soldering iron temperature to 260 °C.

Symbols and Definitions

Absolute Maximum Rating
Operating safe zones. Exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

BCD
Binary Coded Decimal.

$\overline{BI}$/RBO
Blanking Input or Ripple Blanking Output.

CE
Chip Enable.

CLR
Clear. Clear command will preset all internal circuits to a predetermined state.

Duty Cycle
Ratio of time on to time off. Generally expressed in percentage.

F_{MAX}
The maximum clock frequency: the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

I_B
Input Bias Current. Current into an analog circuit input, specified at a particular voltage level.

I_{CC} ($-I_{CC}$)
Supply Current. The current flowing into the $+V_{CC}$ ($-V_{CC}$) supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_{CEX}
Output Leakage Current. The current flowing out of or into a disabled (off) output with a specified High output voltage applied.

I_{IH}
Input High Current. The current flowing into or out of an input when a specified High level voltage is applied to that input.

I_{IL}
Input Low Current. The current flowing out of an input when a specified Low level voltage is applied to that input.

I_{OH}
Output Current Source the device can supply while maintaining a specified voltage output level.

I_{OL}
Output Low Current. The current flowing into an output when it is in the Low State.

I_{OS}
Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is shorted to ground.

I_S
Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

I_{SEG}
Segment Current. The amount of current supplied to each segment as a display. Current ratios are generally compared to segment 'b'.

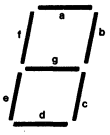
LED
Light Emitting Diode.

Package Type Designation
See full package designations in Appendix.

Power Dissipation
The power that the device can safely handle at 15°C. The dissipation must be derated as indicated for the individual package type.

$\overline{RBI}$
Ripple Blanking Input.

Segment Identification



T_A
Ambient temperature range. Allowable range of the surrounding environment of the operating device.

t_h
Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

T_J
Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

t_{PHL}
Propagation Delay Times. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH}
Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{rec}
Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_s
Setup Time. The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

Symbols and Definitions

DISPLAY DRIVER DEFINITIONS (Cont'd)

Truth Tables

0 is logic level low
1 is logic level high
X — don't care condition — has no effect under circuit conditions listed.

Typical Value

The typical value of a particular parameter at 25°C determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min-max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

V_{BR}

Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

V_F

Forward voltage drop of a device at a specified current level.

V_{IH}

Input High Voltage. The range of input voltages recognized by the device as a logic high.

V_{IL}

Input Low Voltage. The range of input voltages recognized by the device as a logic low.

V_{IN}

The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OH}

Output High Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}

Output Low Voltage. The maximum guaranteed low voltage at an output terminal sinking the specified load current I_{OL}.

V_{OUT}

The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

V_S

Source Voltage. A separate V_{CC} line depending on part type.

$\overline{XX}$

Negate Bar — when it appears over a function indicates that the "true" or valid condition of that function is a logic low level.
i.e. LE — would require a logic high level to cause a latch enable
$\overline{LE}$ — would require a logic low level to cause a latch enable.

4

Quad Line Driver | MC1488

DESCRIPTION

The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

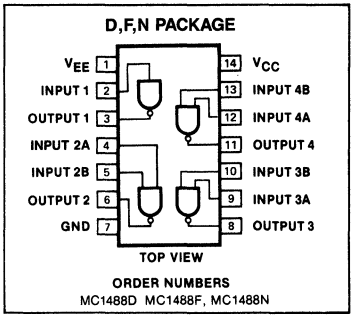
FEATURES

- **Current limited output: ±10mA Typ**
- **Power-off source impedance: 300Ω Min**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Inputs are DTL/TTL compatible**

APPLICATIONS

- **Computer port driver**
- **Digital transmission over long lines**
- **Slew rate control**
- **TTL/DTL to MOS translation**

PIN CONFIGURATION

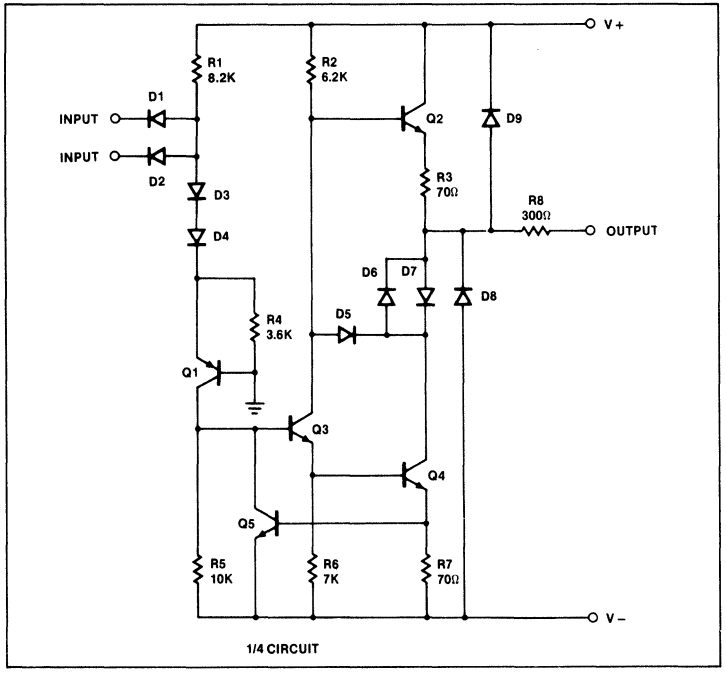


ORDER NUMBERS
MC1488D MC1488F, MC1488N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage V+	+15	V
V-	-15	V
Input voltage (V_{IN})	$-15 \leq V_{IN} \leq 7.0$	V
Output voltage	±15	V
Power dissipation:		
F package	1000	mW
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

CIRCUIT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

$V+ = +9.0V \pm 1\%$, $V- = -9.0V \pm 1\%$; $T_A = 0°C$ to $+75°C$ unless otherwise specified.
All typicals are for $V+ = 9.0V$, $V- = -9.0V$, and $T_A = 25°C$.*

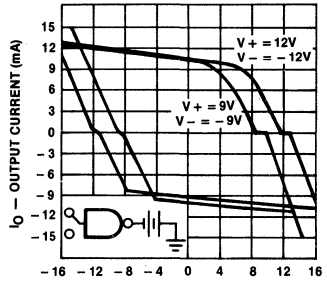
PARAMETER	TEST CONDITIONS		LIMITS			UNIT
			Min	Typ	Max	
Logic "0" input current	$V_{IN} = 0V$			-1.0	-1.6	mA
Logic "1" input current	$V_{IN} = +5.0V$			.005	10.0	μA
High level output voltage	$R_L = 3.0k\Omega$, $V_{IN} = 0.8V$	V+ = 9.0V, V- = -9.0V	6.0	7.0		V
		V+ = 13.2V, V- = -13.2V	9.0	10.5		V
Low level output voltage	$R_L = 3.0k\Omega$, $V_{IN} = 1.9V$	V+ = 9.0V, V- = -9.0V	-6.0	-6.8		V
		V+ = 13.2V, V- = -13.2V	-9.0	-10.5		V
High level output Short-circuit current	$V_{OUT} = 0V$, $V_{IN} = 0.8V$		-6.0	-10.0	-12.0	mA
Low level output Short-circuit current	$V_{OUT} = 0V$, $V_{IN} = 1.9V$		5.0	10.0	12.0	mA
Output resistance	$V+ = V- = 0V$, $V_{OUT} = \pm 2V$		300			Ω
Positive supply current (output open)	$V_{IN} = 1.9V$	V+ = 9.0V, V- = -9.0V		15.0	20.0	mA
		V+ = 12V, V- = -12V		19.0	25.0	mA
		V+ = 15V, V- = -15V		25.0	34.0	mA
	$V_{IN} = 0.8V$	V+ = 9.0V, V- = -9.0V		4.5	6.0	mA
		V+ = 12V, V- = -12V		5.5	7.0	mA
		V+ = 15V, V- = -15V		8.0	12.0	mA
Negative supply current (output open)	$V_{IN} = 1.9V$	V+ = 9.0V, V- = -9.0V		-13.0	-17.0	mA
		V+ = 12V, V- = -12V		-18.0	-23.0	mA
		V+ = 15V, V- = -15V		-25.0	-34.0	mA
	$V_{IN} = 0.8V$	V+ = 9.0V, V- = -9.0V		-1	-15	μA
		V+ = 12V, V- = -12V		-1	-15	μA
		V+ = 15V, V- = -15V		-.01	-2.5	mA
Power dissipation	V+ = 9.0V, V- = -9.0V			252	333	mW
	V+ = 12V, V- = -12V			444	576	mW
Propagation delay to "1" (t_{pd1})	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			275	560	ns
Propagation delay to "0" (t_{pd0})	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			70	175	ns
Rise time (t_r)	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			75	100	ns
Fall time (t_f)	$R_L = 3.0k\Omega$, $C_L = 15pF$, $T_A = 25°C$			40	75	ns

NOTE

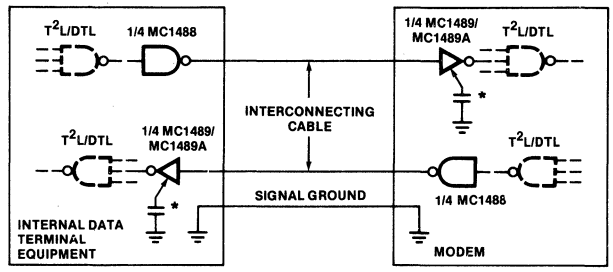
*Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS



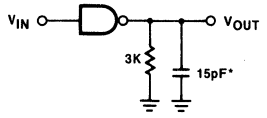
RS232C DATA TRANSMISSION



NOTE

*Optional for noise filtering

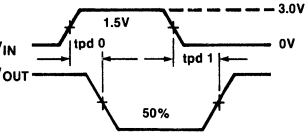
AC LOAD CIRCUIT



NOTE

*C_L includes probe and jig capacitance.

SWITCHING WAVEFORMS



NOTE

t_r and t_f are measured between 10% and 90% of the output waveform

APPLICATIONS

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

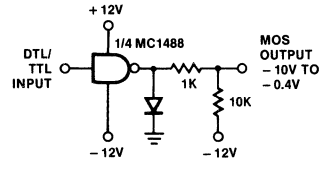
$$C = I_{SC}\ (\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

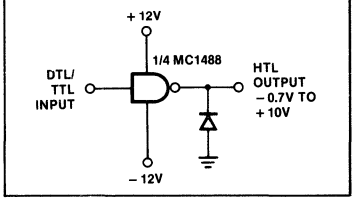
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

TYPICAL APPLICATIONS

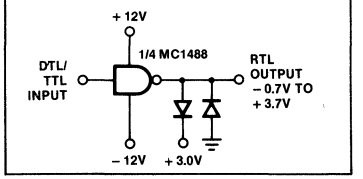
DTL/TTL-TO-MOS TRANSLATOR



DTL/TTL-TO-HTL TRANSLATOR



DTL/TTL-TO-RTL TRANSLATOR



Quad Line Receivers | MC1489/MC1489A

DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C.

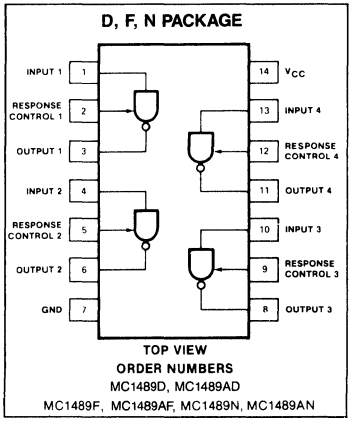
FEATURES

- **Four totally separate receivers per package**
- **Programmable threshold**
- **Built-in input threshold hysteresis**
- **"Fail safe" operating mode**
- **Inputs withstand ±30V**

APPLICATIONS

- **Computer port inputs**
- **Modems**
- **Eliminating noise in digital circuitry**
- **MOS to TTL/DTL translation**

PIN CONFIGURATION

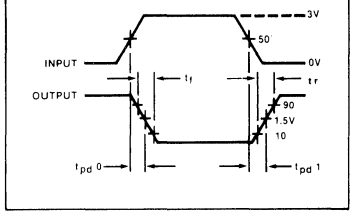


ORDER NUMBERS
MC1489D, MC1489AD
MC1489F, MC1489AF, MC1489N, MC1489AN

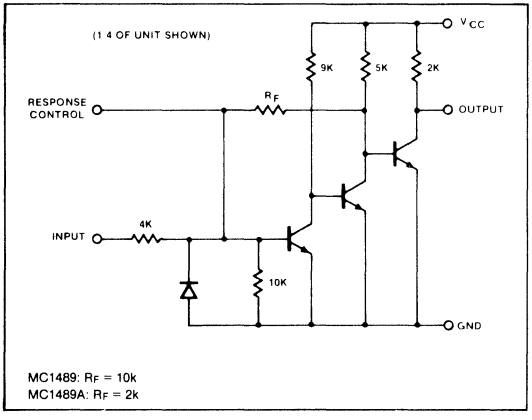
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	10	V
Input voltage range	±30	V
Output load current	20	mA
Power dissipation:		
F package	1	W
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C

VOLTAGE WAVEFORMS

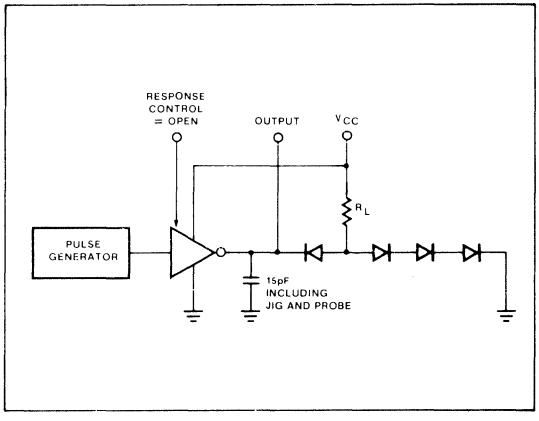


EQUIVALENT SCHEMATIC



MC1489: R_F = 10k
MC1489A: R_F = 2k

AC TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, 0°C ≤ T_A ≤ +75°C unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input high threshold voltage	T_A = 25°C, V_{OUT} ≤ 0.45V, I_{OUT} = 10mA	1.0		1.5	1.75		2.25	V
Input low threshold voltage	T_A = 25°C, V_{OUT} ≤ 2.5V, I_{OUT} = -0.5mA	0.75		1.25	0.75		1.25	V
	V_{IN} = +25V	+3.6	+5.6	+8.3	+3.6	+5.6	+8.3	mA
	V_{IN} = -25V	-3.6	-5.6	-8.3	-3.6	-5.6	-8.3	
Input current	V_{IN} = +3V	+0.43	+0.53		+0.43	+0.53		mA
	V_{IN} = -3V	-0.43	-0.53		-0.43	-0.53		
Output high voltage	V_{IN} = 0.75V, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
	Input = Open, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
Output low voltage	V_{IN} = 3.0V, I_{OUT} = 10mA		0.33	0.45		0.33	0.45	V
Output short circuit current	V_{IN} = 0.75V		3.0			3.0		mA
Supply current	V_{IN} = 5.0V		20	26		20	26	mA
Power dissipation	V_{IN} = 5.0V		100	130		100	130	mW

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, T_A = 25°C unless otherwise specified.[1,2]

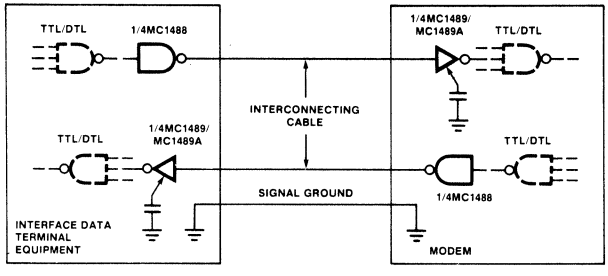
PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input to output "high" Propagation delay (t_{pd1})	R_L = 3.9kΩ (AC test circuit)		25	85		25	85	ns
Input to output "low" Propagation delay (t_{pd0})	R_L = 390Ω (AC test circuit)		20	50		20	50	ns
Output rise time	R_L = 3.9kΩ (AC test circuit)		110	175		110	175	ns
Output fall time	R_L = 390Ω (AC test circuit)		9	20		9	20	ns

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

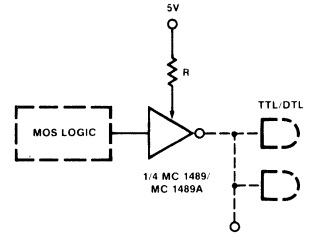
TYPICAL APPLICATIONS

RS232C DATA TRANSMISSION



*Optional for noise filtering

MOS TO TTL/DTL TRANSLATOR



Addressable Relay Driver | NE5090

DESCRIPTION

The NE5090 addressable relay driver is a high current latched driver, similar in function to the 9934 address decoder. The device has 8 open collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3 bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic "0" is applied. The device is packaged in a 16 pin plastic or CERDIP package.

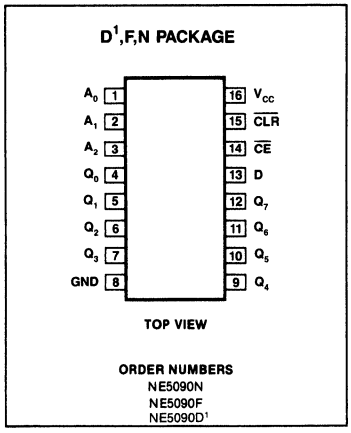
FEATURES

- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **Will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **Pin compatible with 9334**

APPLICATIONS

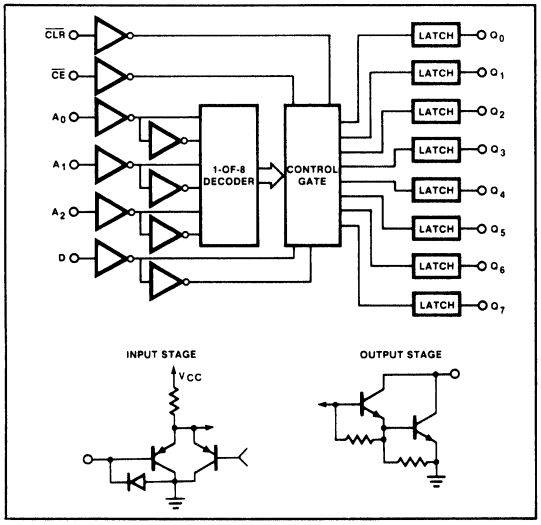
- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATION



NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage	−0.5 to +15	V
V_{OUT}	Output voltage	0 to +30	V
I_{GND}	Ground current	500	mA
I_{OUT}	Output current Each output	200	mA
P_D	Power dissipation[1]	1	W
Ambient temperature range			°C
T_A	NE5090	0 to +70	
T_J	Junction	150	
T_{STG}	Storage	−65 to +150	
T_{sold}	Lead soldering temperature (10 sec max)	300	°C

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1-3	A0-A2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	Q0-Q7	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	CE	The chip enable. When this input is low, the output latches will accept data. When CE goes high, all outputs will retain their existing state, regardless of address of data input conditions.
15	CLR	The clear input. When CLR goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

TRUTH TABLE

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} ⟶								Memory
H	L	L	L	L	L	H Q_{N-1} ⟶								Addressable Latch
H	L	H	L	L	L	L Q_{N-1} ⟶								
H	L	L	H	L	L	Q_{N-1} H Q_{N-1} ⟶								
H	L	H	H	L	L	Q_{N-1} L Q_{N-1}								
H	L	L	H	H	H	Q_{N-1} ⟶							H	
H	L	H	H	H	H	Q_{N-1} ⟶							L	

X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

DC ELECTRICAL CHARACTERISTICS V_{CC} = 4.75V to 5.25V, 0°C ≤ T_A ≤ 70°C unless otherwise specified (NE5090)[2].

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH} V_{IL}	Input voltage High Low		2.0		 0.8	V
V_{OL}	Output voltage Low	I_{OL} = 150mA, T_A = 25°C Over temperature		1.05	1.30 1.50	V
I_{IH} I_{IL}	Input current High Low	$V_{IN} = V_{CC}$ V_{IN} = 0V		<1.0 −3.0	10 −250	μA
I_{OH}	Leakage current	V_{OUT} = 28V,		5	250	μA
I_{CCL} I_{CCH}	Supply current All outputs low All outputs high	V_{CC} = 5.25V NE5090		35 22	60 50	mA

NOTES

1. Derate power dissipation as indicated above threshold ambient temperature
   NE5090 N at 9.3mW/°C above 85°C
   NE5090 F at 7.5mW/°C above 65°C
2. All typical values are at V_{CC} = 5V and T_A = 25°C

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$, $V_{OUT} = 5V$, $I_{OUT} = 100mA$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$

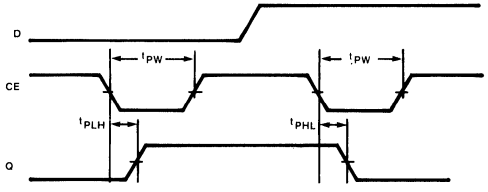
	PARAMETER	TO	FROM	Min	Typ	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay time Low to high[1] High to low[1]	Output	$\overline{CE}$		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low to high[2] High to low[2]	Output	Data		920 130	1850 260	ns
t_{PLH} t_{PHL}	Low to high[3] High to low[3]	Output	Address		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low to high[4] High to low[4]	Output	$\overline{CLR}$		920	1850	ns
SWITCHING SETUP REQUIREMENTS							
$t_{s(H)}$[5] $t_{s(L)}$[5]		Chip enable Chip enable	High data Low data	5 10	20 30		ns
$t_{s(A)}$[6]		Chip enable	Address	0	20		ns
$t_{h(H)}$[5] $t_{H(L)}$[5]		Chip enable Chip enable	High data Low data	+ 10 + 10	0 0		ns
$t_{pw(E)}$[1]	Chip enable pulse width[1]			0	20		ns

NOTES

1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

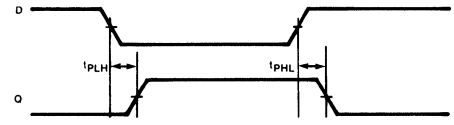
TIMING DIAGRAMS

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



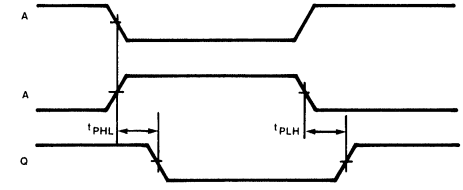
Other Inputs: $\overline{CLR}$ = H, A = Stable,

TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



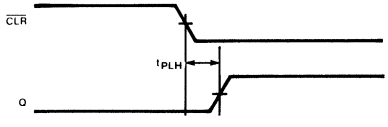
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = H, A = Stable

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

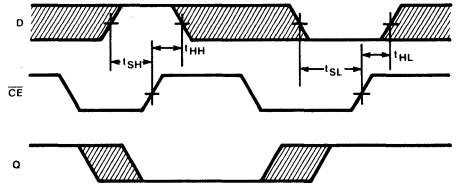
TURN-OFF DELAY, CLEAR TO OUTPUT



Other Inputs: $\overline{CE}$ = H,

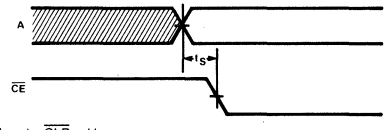
TIMING DIAGRAMS (Cont'd)

SETUP AND HOLD TIME, DATA TO ENABLE



Other Inputs: $\overline{CLR}$ = H, A = Stable.

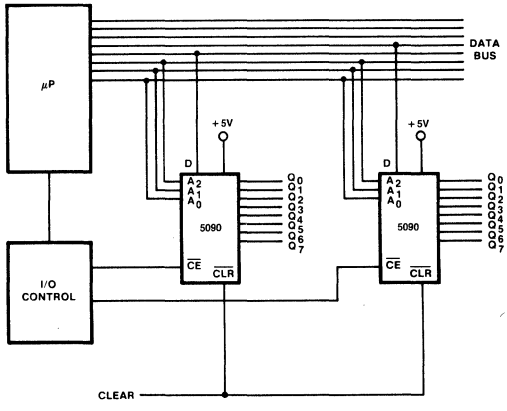
SETUP TIME, ADDRESS TO ENABLE



Other Inputs: $\overline{CLR}$ = H.

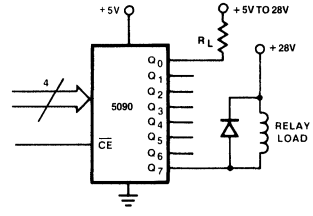
TYPICAL APPLICATIONS

INTERFACING WITH A MICROPROCESSOR SYSTEM

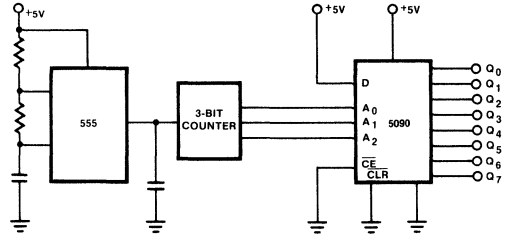


A_0, A_1, A_2, may be connected to the address bus if permitted by system design.

DRIVING SIMPLE LOADS

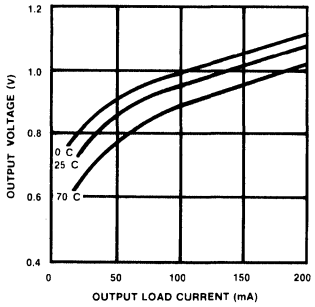


OPERATING IN DEMULTIPLEX MODE



TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE VS LOAD CURRENT



Octal Line Driver

NE5170

DESCRIPTION

The NE5170 is an octal line driver which is designed for digital communications with data rates up to 100Kb/s. This device meets all the requirements of EIA standards RS232C/RS423A and CCITT recommendations V.10/X.26. Three programmable features, (1) output slew rate (2) output voltage level, and (3) three-state control (high impedance) are provided so that output characteristics may be modified to meet the requirements of specific applications.

FEATURES

- **Meets EIA RS232C/423A and CCITT V.10/X.26**
- **Simple slew rate programming with a single external resistor**
- **0.1 to 10V/μs slew rate range**
- **High/low programmable voltage output modes**
- **TTL compatible inputs**

APPLICATIONS

- **High speed modems**
- **High speed parallel communications**
- **Computer I/O ports**
- **Logic level translation**

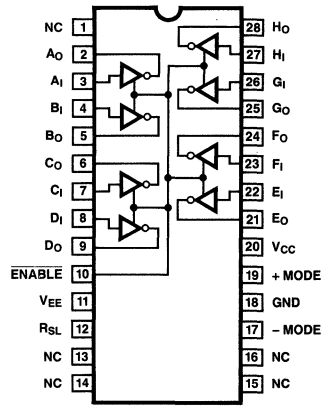
FUNCTION TABLE

$\overline{\text{ENABLE}}$	LOGIC INPUT	OUTPUT VOLTAGE (V)		
		RS423A[1]	RS232C	
			Low Output Mode[1]	High Output Mode[2]
L	L	5 to 6V	5 to 6V	≥ 9V
L	H	−5 to −6V	−5 to −6V	≤ −9V
H	X	High Z	High Z	High Z

NOTES:
1. V_{CC} = +10V and V_{EE} = −10V; R_L = 3KΩ
2. V_{CC} = +12V and V_{EE} = −12V; R_L = 3KΩ

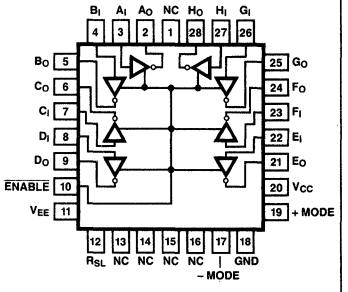
PIN CONFIGURATION

N Package



TOP VIEW
Order Number
NE5170N

G Package



TOP VIEW
Order Number
NE5170G

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Supply Voltage V_{CC}	15	V
Supply Voltage V_{EE}	– 15	V
Output Current[1]	± 150	mA
Input Voltage ($\overline{\text{Enable}}$, Data)	– 1.5 to + 7	V
Output Voltage[2]	+ 15	V
Minimum Slew Resistor[3]	1K	Ω
Power Dissipation	800	mW

DC ELECTRICAL CHARACTERISTICS V_{CC} (see notes 4, 5), $0°C \leq T_A \leq 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNITS
			Min	Max	
V_{OH}	Output high voltage	$V_{IN} = 0.8V$, $R_L = 3K\Omega$[4]	5	6	V
		$R_L = 450\Omega$[4]	4.5	6	
		$R_L = 3K\Omega$[5], $C_L = 2500pF$	$V_{CC} - 3$		
V_{OL}	Output low voltage	$V_{IN} = 2.4V$, $R_L = 3K\Omega$[4]	– 6	– 5	V
		$R_L = 450\Omega$[4]	– 6	– 4.5	
		$R_L = 3K\Omega$[5], $C_L = 2500pF$		$V_{EE} + 3$	
	Output unbalance voltage	$V_{CC} = \lvert V_{EE} \rvert$, $R_L = 450\Omega$[4]		0.4	V
I_{CEX}	Output leakage current	$\lvert V_O \rvert = 6V$, ENABLE = 2V or $V_{CC} = V_{EE} = 0V$	– 100	100	μA
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IL}	Logic "0" input current	$V_{IN} = 0.4V$	– 400	0	μA
I_{IH}	Logic "1" input current	$V_{IN} = 2.4V$	0	40	μA
I_{OS}	Output short circuit current	$V_O = 0V$	– 150	150	μA
V_{CL}	Input clamp voltage	$I_{IN} = -15mA$	– 1.5		V
I_{CC}	Supply current	NO LOAD		40	mA
I_{EE}		NO LOAD	– 40		mA

NOTES:

1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. High impedance mode.
3. Minimum value of the resistor used to set the slew rate.
4. V_{OH}, V_{OL} at $R_L = 450\Omega$ will be ≥90% of V_{OH}, V_{OL} at $R_L = \infty$.
5. High Output Mode; + MODE pin = V_{CC}; – MODE pin = V_{EE}; $9V \leq V_{CC} \leq 13V$; $-9V \geq V_{EE} \geq -13V$.

AC ELECTRICAL CHARACTERISTICS V_{CC} = +10V; V_{EE} = −10V; Mode = GND, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNITS
			Min	Max	
t_{PHZ}	Propagation delay output high to high impedance	R_L = 450, C_L = 50pF or R_L = 3K, C_L = 2500pF		5	μs
t_{PLZ}	Propagation delay output low to high impedance	R_L = 450, C_L = 50pF or R_L = 3K, C_L = 2500pF		5	μs
t_{PZH}	Propagation delay high impedance to high output	R_{SL} = 200K R_L = 450, C_L = 50pF or R_L = 3K, C_L = 2500pF		150	μs
t_{PZL}	Propagation delay high impedance to low output	R_{SL} = 200K R_L = 450, C_L = 50pF or R_L = 3K, C_L = 2500pF		150	μs
SR	Ouput slew rate[1]	R_{SL} = 2K ± 1%	8	12	V/μs
		R_{SL} = 20K ± 1%	0.8	1.2	
		R_{SL} = 200K ± 1%	0.073	0.127	

NOTE:
1. SR: Load condition. (A) For R_{SL} <4KΩ use R_L = 450Ω; C_L = 50pF; (B) For R_{SL} >4KΩ use either R_L = 450Ω, C_L = 50pF or R_L = 3KΩ, C_L = 2500pF.

SLEW RATE PROGRAMMING

Slew rate for the NE5170 is set using a single external resistor connected between the R_{SL} pin and ground. Adjustment is made according to the formula:

$$R_{SL} \text{ (in kilohms)} = \frac{20}{\text{Slew Rate}}$$

where the slew rate is in V/μs. The slew resistor can vary between 2 and 200 kilohms which gives a slew rate range of 10 to 0.1V/μs. This adjustment of the slew rate allows tailoring output characteristics to recommendations for cable length and data rate found in EIA standard RS423A. Approximations for cable length and data rate are given by:

Max. data rate (in Kb/s) = 300/t

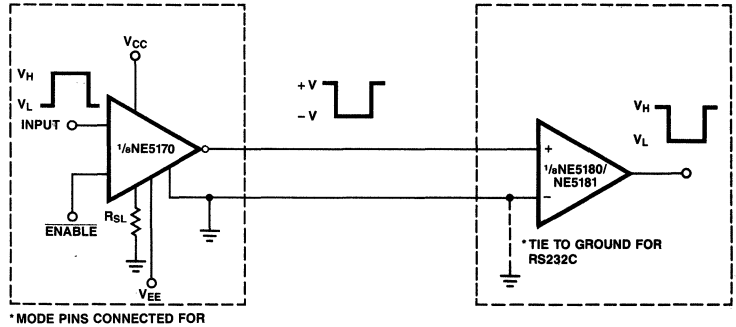
Cable length (in feet) = 100 × t

where t is the rise time in microseconds. The absolute maximum data rate is 100Kb/s and the absolute maximum cable length is 4000 feet.

OUTPUT MODE PROGRAMMING

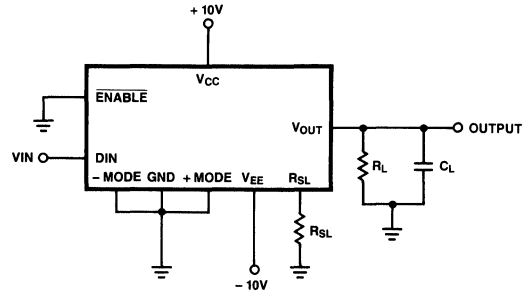
The NE5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS423A and RS232C. The high output mode meets the specifications of RS232C only since higher output voltages result from programming this mode. The high output mode provides the greater output voltages where higher attenuation levels must be tolerated. Programming the high output mode is accomplished by connecting the +MODE pin to V_{CC} and the −MODE pin to V_{EE}. The low output mode results when both of these pins are connected to ground.

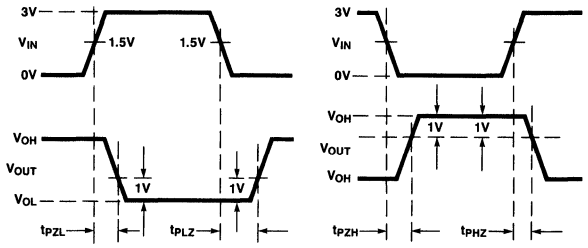
APPLICATIONS



RS232C/RS423A Data Transmission

AC PARAMETER TEST CIRCUIT AND WAVEFORMS





NOTES: 1) See AC electrical characteristics table for values of R_{SL}, R_L and C_L.
2) V_{IN} pulse: Frequency = 1kHz, duty cycle = 50%, $Z_{OUT} = 50\Omega$, $t_r = t_f \leq 10$ns.

4

Octal Line Receivers

NE5180/NE5181

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS232C, RS423A, RS422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 Kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

FEATURES

- **Meets EIA RS232C/423A/422A and CCITT V.10, V.11, V.28**
- **Single +5V supply — TTL compatible outputs**
- **Differential inputs withstand ±25V**
- **Failsafe feature**
- **Input noise filter (NE5180 only)**
- **Internal hysteresis**

APPLICATIONS

- **High speed modems**
- **High speed parallel communications**
- **Computer I/O ports**
- **Logic level translation**

FUNCTION TABLE

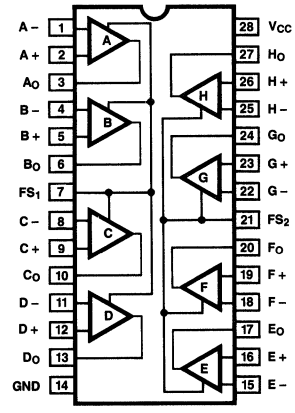
INPUT	FAILSAFE INPUT	LOGIC OUTPUT
$V_{ID} > 200$ mV[1]	X	H
$V_{ID} < -200$mV[1]	X	L

NOTE:

1. V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage.

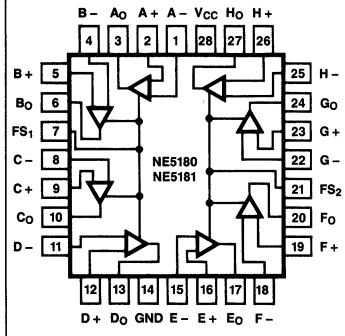
PIN CONFIGURATION

N Package



TOP VIEW
Order Numbers
NE5180N NE5181N

G Package



TOP VIEW
Order Numbers
NE5180G NE5181G

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Power Dissipation	800	mW
Supply Voltage (V_{CC})	7	V
Common Mode Range	±15	V
Differential Input Voltage (V_{ID})	±25	V
Output Sink Current	50	mA
Failsafe Voltage	−0.3 to V_{CC}	V
Output Short Circuit Time	1	sec

DC ELECTRICAL CHARACTERISTICS $V_{CC}=5V \pm 5\%$, $0°C \le T_A \le 70°C$, input common mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS		NE5180		NE5181		UNITS
				Min	Max	Min	Max	
R_{IN}	DC input resistance	$3V \le \lvert V_{IN}\rvert \le 25V$		3K	7K	3K	7K	Ω
V_{OFS}	Failsafe output voltage	Inputs open or shorted together	$0 \le I_{OUT} \le 8mA$, $V_{failsafe}=0V$		0.45		0.45	V
			$0 \ge I_{OUT} \ge -400\mu A$, $V_{failsafe}=V_{CC}$	2.7		2.7		
V_{th}	Differential input high[4] threshold	$V_{OUT}=2.7V$, $I_{OUT}=-440\mu A$	$R_S=0$[1]		0.2		0.2	V
			$R_S=500$[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	$V_{OUT}=0.45V$, $I_{OUT}=8mA$	$R_S=0$[1]	−0.2		−0.2		V
			$R_S=500$[1]	−0.4		−0.4		
V_H	Hysteresis[4]	$F_S=0V$ or V_{CC} (See Figure 1)		60	140	60	140	mV
V_{IOC}	Open circuit input voltage				2		2	V
C_I	Input capacitance				100		100	pF
V_{OH}	High level output voltage	$V_{ID}=1V$, $I_{OUT}=-440\mu A$		2.7		2.7		V
V_{OL}	Low level output voltage	$V_{ID}=-1V$	$I_{OUT}=4mA$[2]		0.4		0.4	V
			$I_{OUT}=8mA$[2]		0.45		0.45	
I_{OS}	Short circuit output current	Note 3		20	100	20	100	mA
I_{CC}	Supply current	$4.75V \le V_{CC} \le 5.25V$			125		125	mA
I_{IN}	Input current	Other inputs grounded	$V_{IN}=+10V$		3.25		3.25	mA
			$V_{IN}=-10V$	−3.25		−3.25		

NOTES:
1. R_S is a resistor in series with each input.
2. Measured after 100ms warm up (at 0°C).
3. Only 1 output may be shorted at a time and then only for a maximum of 1 sec.
4. See Figure 1 for threshold and hysteresis definitions.

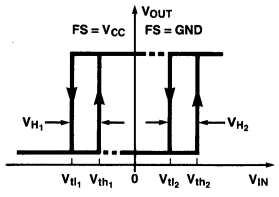


Figure 1. V_{tl}, V_{th}, V_H Definition

AC ELECTRICAL CHARACTERISTICS $V_{CC}=5V \pm 5\%$, $0°C \le T_A \le 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	NE5180		NE5181		UNITS
			Min	Max	Min	Max	
t_{PLH}	Propagation delay — low to high	$C_L=50pF$, $V_{IN}=\pm 1V$		300		70	ns
t_{PHL}	Propagation delay — high to low	$C_L=50pF$, $V_{IN}=\pm 1V$		300		70	ns
f_a	Acceptable input frequency	Unused input grounded, $V_{IN}=\pm 200mV$		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, $V_{IN}=\pm 500mV$	5.5		NA		MHz

Octal Line Receivers | NE5180/NE5181

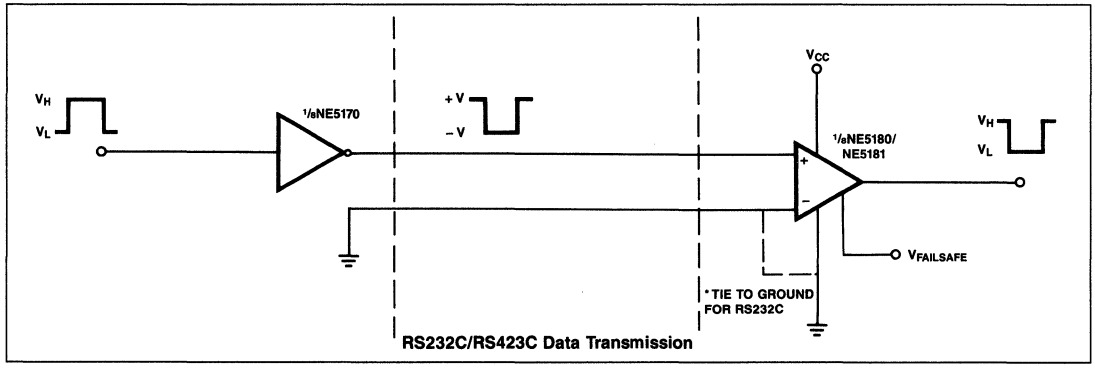
FAILSAFE OPERATION

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS422A and RS423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to V_{CC} provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

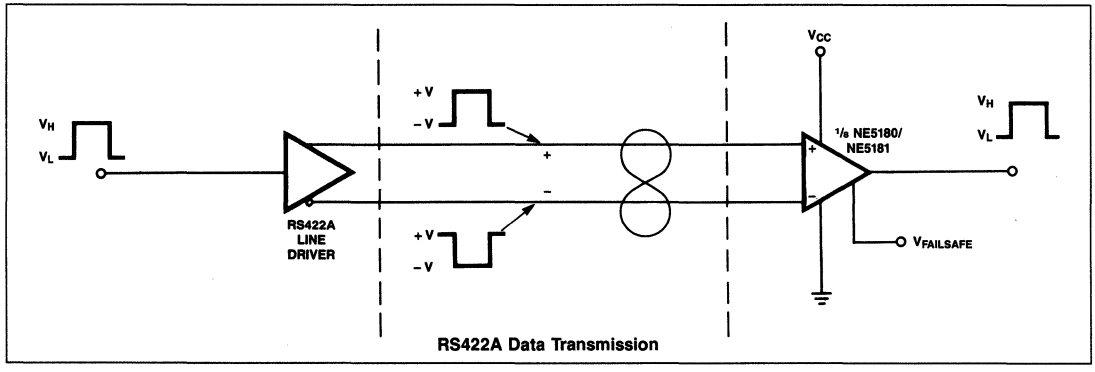
INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ±500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).

APPLICATIONS

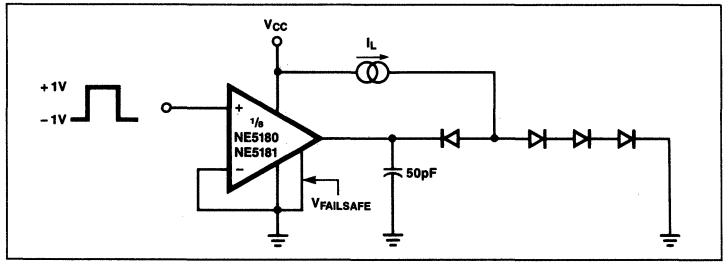


RS232C/RS423C Data Transmission

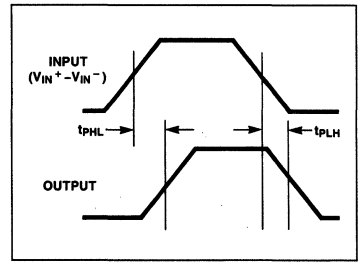


RS422A Data Transmission

AC TEST CIRCUIT



VOLTAGE WAVEFORMS



LED Decoder/Driver | NE587

DESCRIPTION

The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading and/or trailing edge zeros**

APPLICATIONS

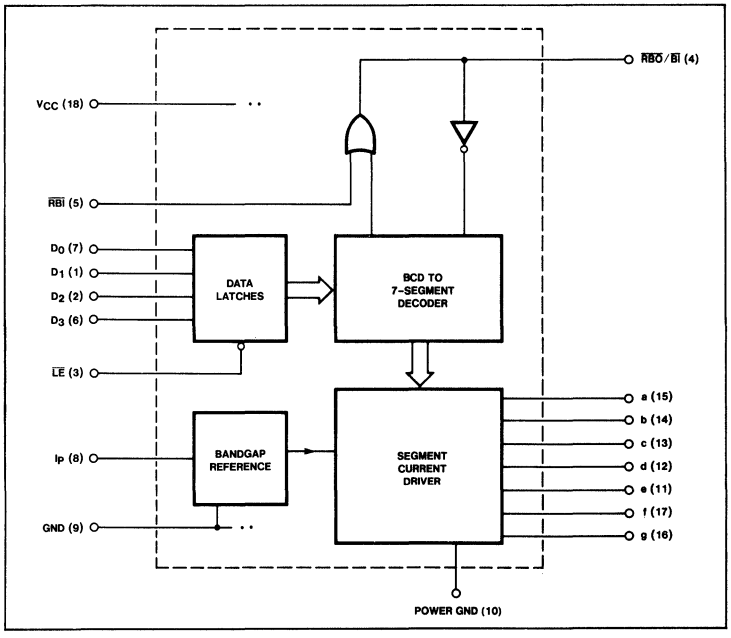
- **Digital panel meters**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage (D_0 - D_3, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10 sec. max)	300	°C

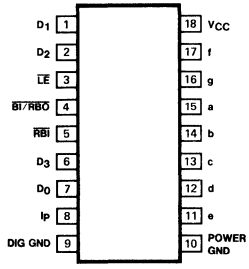
NOTE
Derate power dissipation as indicated
N package - 95°C/watt above 55°C
F package - 100°C/watt above 50°C

BLOCK DIAGRAM



PIN CONFIGURATIONS

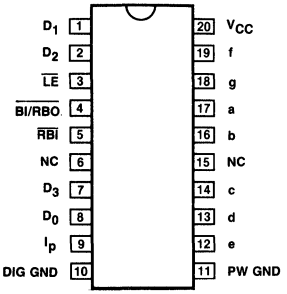
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE587F NE587N

D[2] PACKAGE



TOP VIEW
NE587D[2]

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

4

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C.
Typical values are at V_{CC} = 5V, T_A = 25°C, R_P = 1kΩ (±1%) unless otherwise stated.

PARAMETER		TEST CONDITIONS	NE587			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All Inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	I_{IN} = −12mA, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs D_0 −D_3, $\overline{LE}$, $\overline{RBI}$ V_{IN} = 2.4V V_{IN} = 15V Input $\overline{BI}$ (pin 4) $\overline{RBI}$ = H V_{IN} = V_{CC} = 5.25V		 1.0 15 10	 10 15 100	µA µA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs D_0 − D_3 $\overline{LE}$, $\overline{RBI}$		−5 −200		µA
		Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−0.7		mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ I_{out} = 3.0mA		.2	.5	V
V_{OH}	Output high voltage	Output $\overline{RBO}$ I_{OUT} = −50µA $\overline{RBI}$ = H	3.5	4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" thru "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" thru "g" V_{OUT} = 5.0V		20	250	µA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		33	55	mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		50	70	mA

NOTE
NE587 PROGRAMMING
The NE587 output current can be programmed, provided a program resistor, Rp, be connected between Ip (pin 8) and Ground (pin 9). The voltage at Ip (pin 8) is constant (≈1.3V). Thus, a current through Rp is $Ip \approx \frac{1.3V}{Rp}$, as shown in Figure 5. $\frac{Io}{Ip}$ is 20 in the 15 to 50mA output current range.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V T_A = 25°C. R_L = 130Ω, C_L = 30pF including probe capacity.

PARAMETER		TEST CONDITIONS	NE587			UNIT
			Min	Typ	Max	
$t_{D_{av.}}$	Propagation delay Figure 2	From data to output		135		ns
$t_{D_{av.}}$	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		30			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	20			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

NOTE

$t_{D_{av.}} = \frac{1}{2}(t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	*	X	X	X	X	STABLE							**	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	blank
**BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	blank

NOTES

H = HIGH voltage level, output is "OFF"

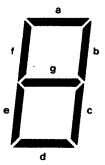
L = LOW voltage level, output is "ON"

X = Don't care

* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

** $\overline{RBO/BI}$ used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



NE587 PROGRAMMING

NE587 output current can be programmed by using a programming resistor, R_P, connected between r_P (pin 8) and Gnd (pin 9). The voltage at r_P (pin 8) is constant ($\approx$1.40V). A partial schematic of the voltage reference used in the NE587 is shown in figure 1.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

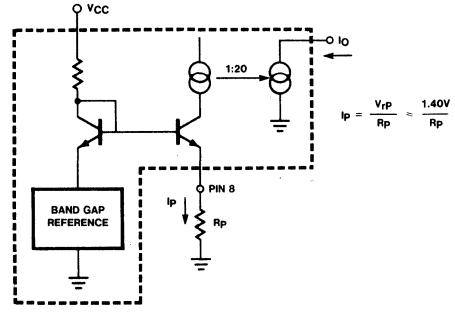


Figure 1

TIMING DIAGRAMS

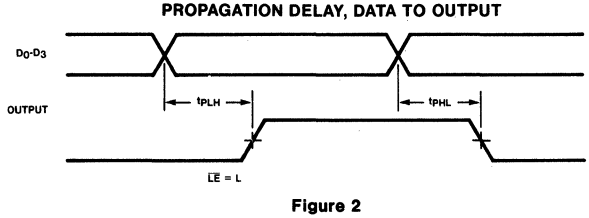


Figure 2

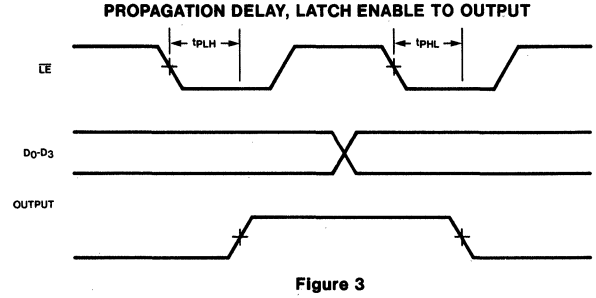


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDS are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 6, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC},	Supply voltage to driver
V_S,	Supply voltage to display
I_{CC},	Quiescent supply current of driver
I_{SEG},	LED segment current
V_F,	LED segment forward voltage at I_{seg}
K_{DC},	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)

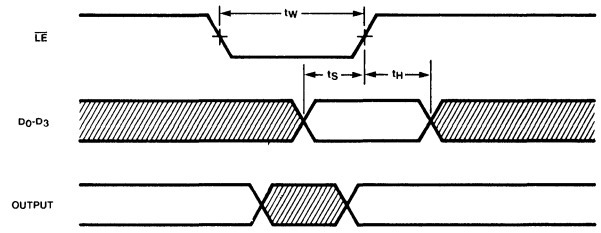


Figure 4

These voltages are all for single diode displays. Some early red displays had 2 series LEDS per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

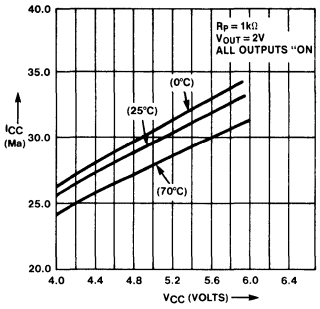
$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC}$ mW

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$
$P_{d\ max} = 5.25 \times 50 + 3.25 \times 7 \times 30$ mW
$= 945$ mW

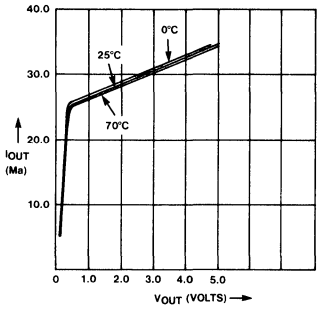
4

TYPICAL PERFORMANCE CURVES

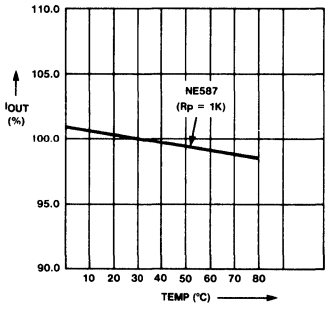
SUPPLY CURRENT VS SUPPLY VOLTAGE NE587



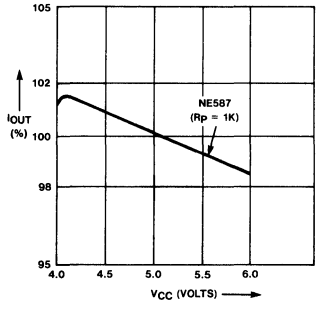
OUTPUT CURRENT VS OUTPUT VOLTAGE NE587 R_P = 1Kohms



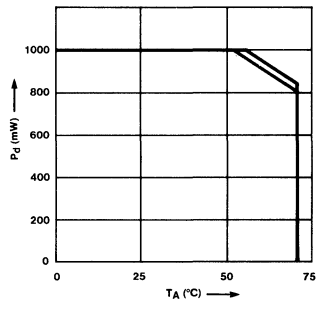
NORMALIZED OUTPUT CURRENT VS TEMPERATURE V_{CC} = 5.0V



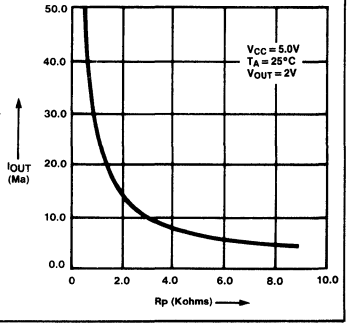
NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE V_O = 2V T_A = 25°C



MAXIMUM POWER DISSIPATION VS TEMPERATURE

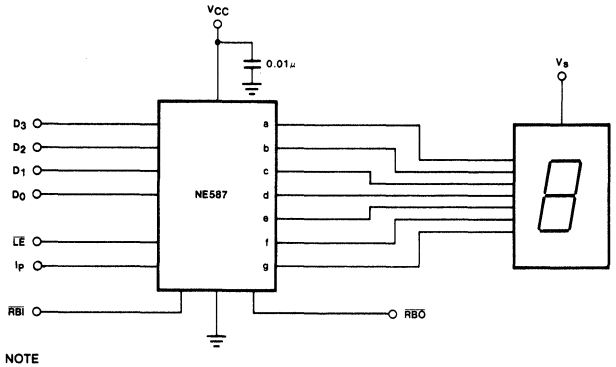


OUTPUT CURRENT VS PROGRAM RESISTOR



TYPICAL APPLICATIONS

DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on V_{CC} should be 0.01 μF ceramic

Figure 6

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$P_{d\,av}$ = 5.0 × 30 + 3.00 × 5 × 25 mW
= 525 mW

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics).

However, a major portion of this power dissipation ($P_{d\,max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \simeq 10\Omega\ (\tfrac{1}{2}\ W\ rating)$$

assuming worst case I_{seg} of 30 mA

Hence now $P_{d\,max}$ = $V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times I_{seg} \times K_{DC}$
= 5.25 × 50 + 1.25 × 7 × 30 mW
= 525 mW

and $P_{d\,av}$ = 5.0 × 30 + 1.25 × 5 × 25
= 306 mW

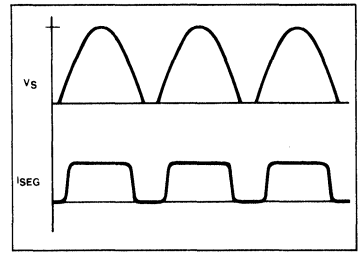
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d,\ V_D \simeq 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similiar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 9. For example a darlington PNP or NPN emitter follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
V_S = 4.9V pk.
V_F = 2.0V

The duty cycle is approximately 60%.

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT DISPLAY WITH BRIGHTNESS CONTROL AND LEADING EDGE RIPPLE BLANKING

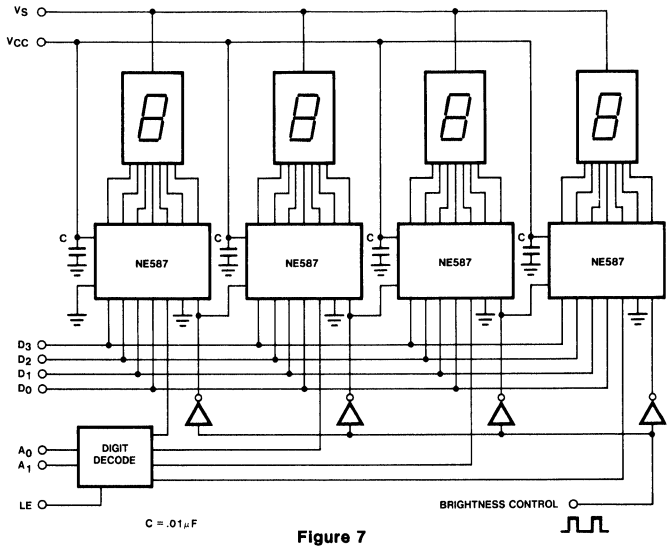


Figure 7

INTERFACING 8-DIGIT LED DISPLAY WITH μP BUS

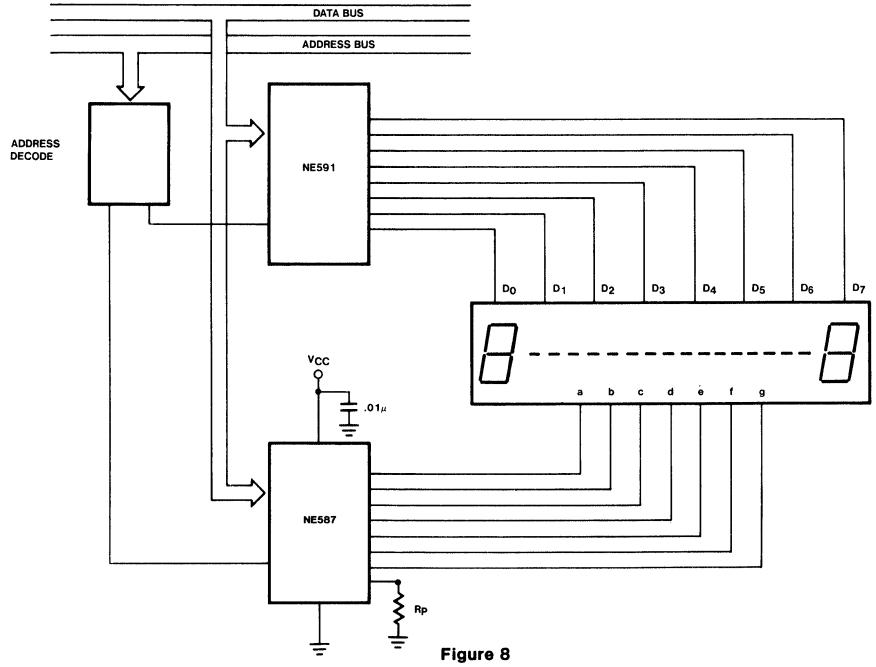


Figure 8

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT MULTIPLEXED LED DISPLAY

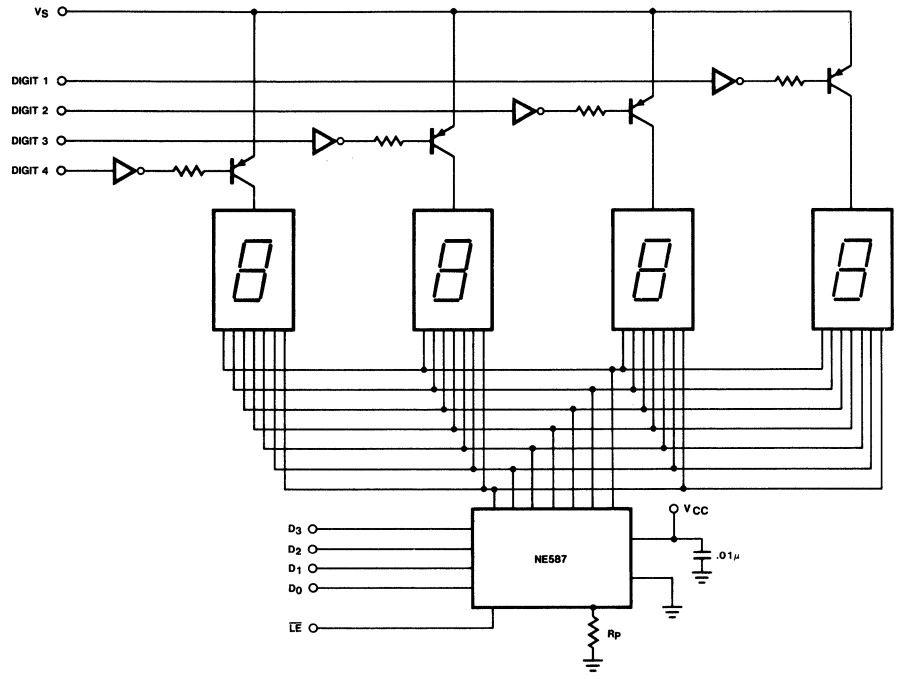


Figure 9

For additional information, refer to the Applications Section.

18-Element LCD BarGraph Display Driver | PCF1303T

DESCRIPTION

The PCF1303T is an LCD driver which drives 18 LCD segments in linear relation to a control voltage. The PCF1303T has 2 modes, one producing a continuous bar (thermometer mode), the other activating one LCD element (pointer mode). Maximum and minimum reference voltage is set via external circuitry.

FEATURES

- **18-element bar graph capability**
- **2 modes: thermometer and pointer mode**
- **Operating voltage 6.0V - 10.0V**
- **Operating temperature −40 to +85°C**
- **28 pin SO package**

APPLICATIONS

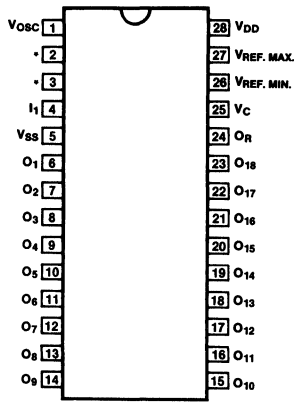
- **Gauges**
- **Volume/level indicators**
- **Thermometers**

FUNCTION TABLE

I_1	Mode
L	Pointer
H	Thermometer

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

PIN CONFIGURATION



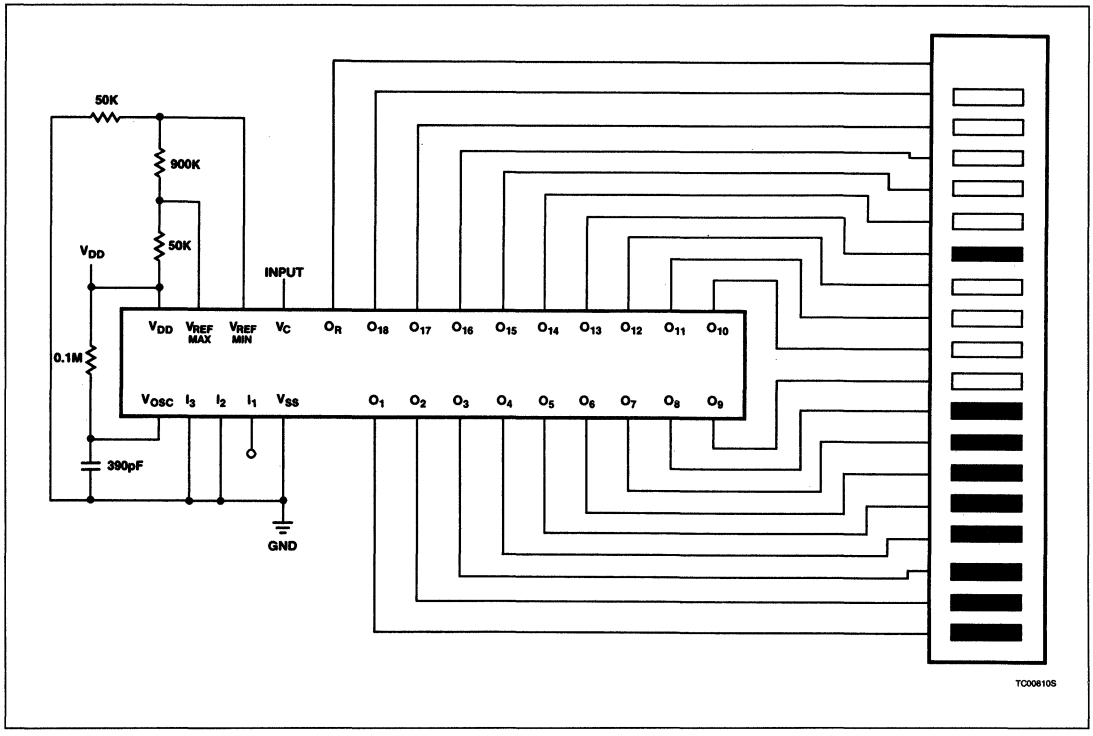
TOP VIEW

CD01320S

PIN	SYMBOL	FUNCTION
1	V_{OSC}	Oscillator terminal
2	*	Connect to V_{SS}
3	*	Connect to V_{SS}
4	I_1	Thermometer/pointer (Choice select input)
5	V_{SS}	Positive power supply
6	O_1	Bar output
7	O_2	Bar output
8	O_3	Bar output
9	O_4	Bar output
10	O_5	Bar output
11	O_6	Bar output
12	O_7	Bar output
13	O_8	Bar output
14	O_9	Bar output
15	O_{10}	Bar output
16	O_{11}	Bar output
17	O_{12}	Bar output
18	O_{13}	Bar output
19	O_{14}	Bar output
20	O_{15}	Bar output
21	O_{16}	Bar output
22	O_{17}	Bar output
23	O_{18}	Bar output
24	O_R	Back plate output
25	V_C	Control voltage input
26	$V_{ref.\ min}$	Reference voltage input
27	$V_{ref.\ max}$	Reference voltage input
28	V_{DD}	Negative power supply

4

TYPICAL SET-UP CONFIGURATION



Universal LCD Driver for Low Multiplex Rates PCF8576

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold(automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with Philips/Videlec chip-on-glass technology
- Manufactured in silicon gate CMOS process

4

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO-56; SOT-190).
PCF8576U: uncased chip in tray

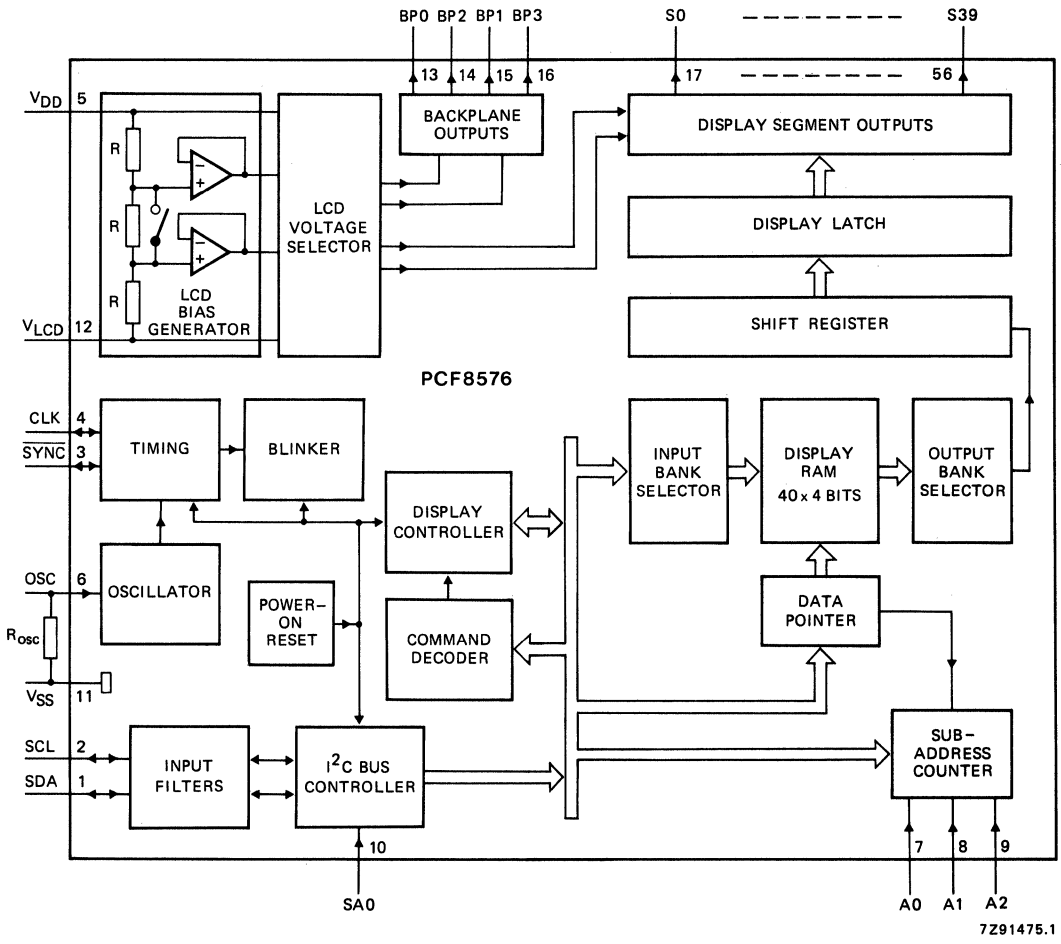


Fig. 1 Block diagram.

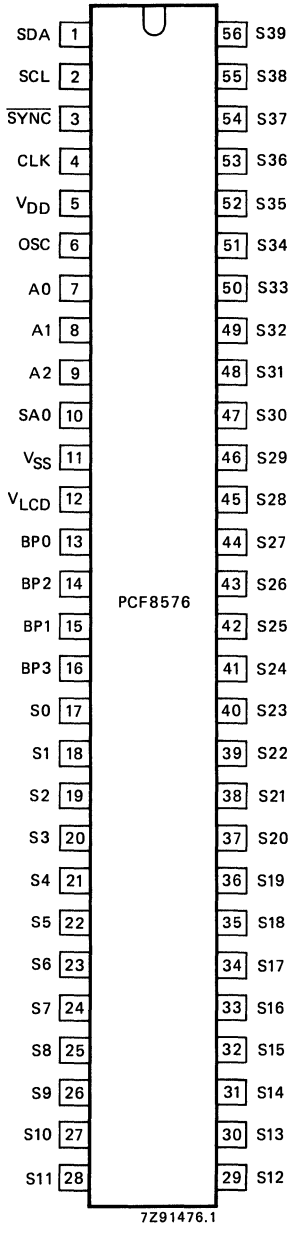


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

4

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segmenets	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor maintains the 2-line I²C bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

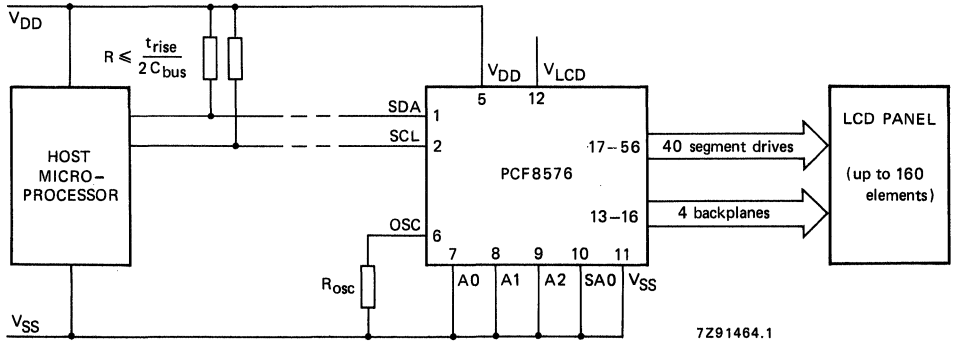


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{thLCD}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{thLCD}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3}$ = 1,732 for 1 : 3 multiplex or $\sqrt{21}/3$ = 1,528 for 1 : 4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\;V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

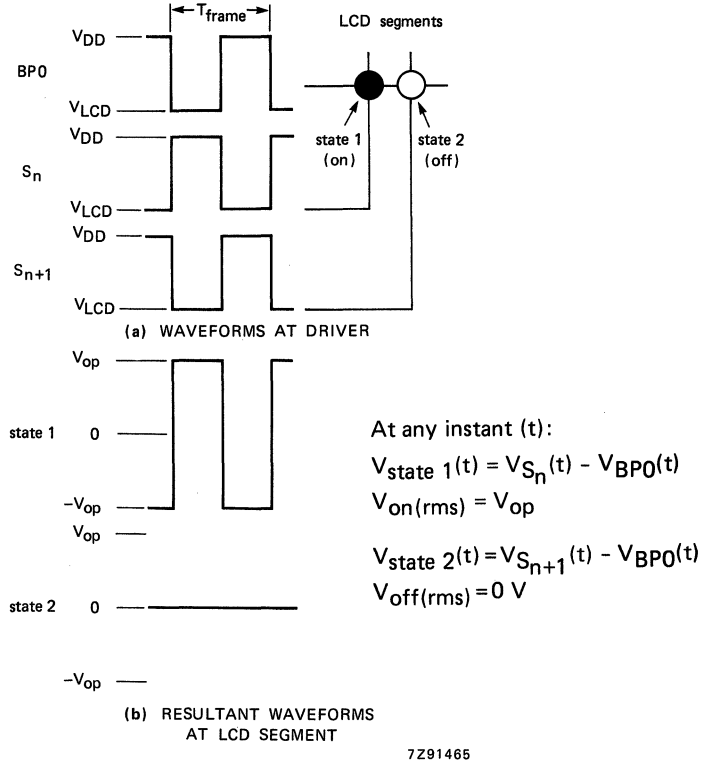


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

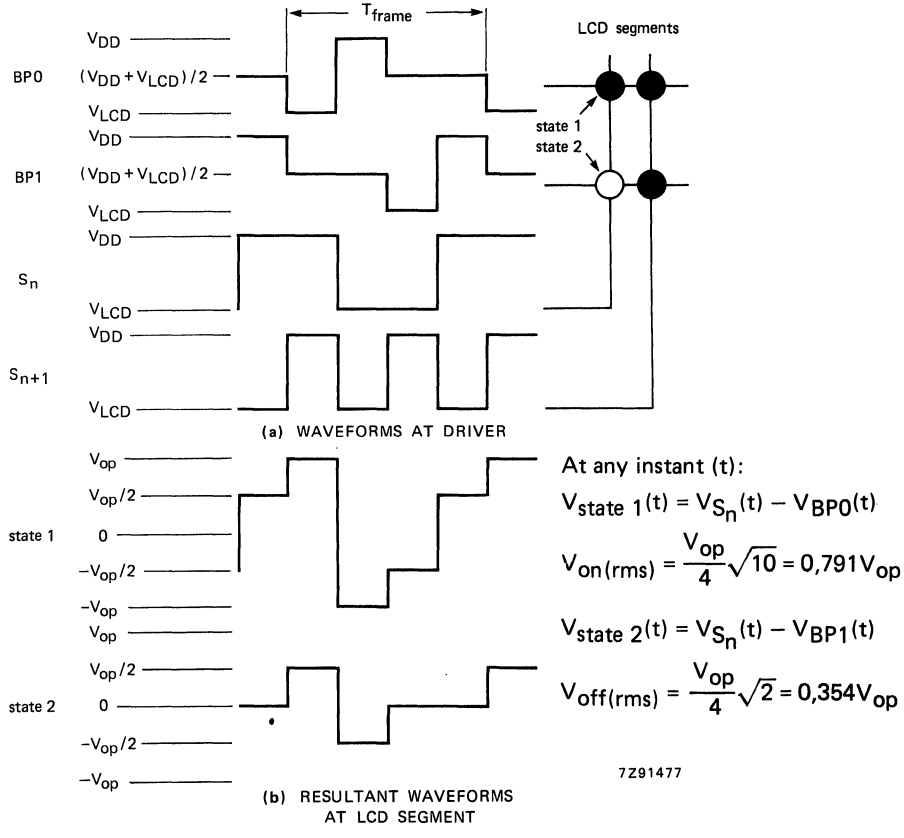


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

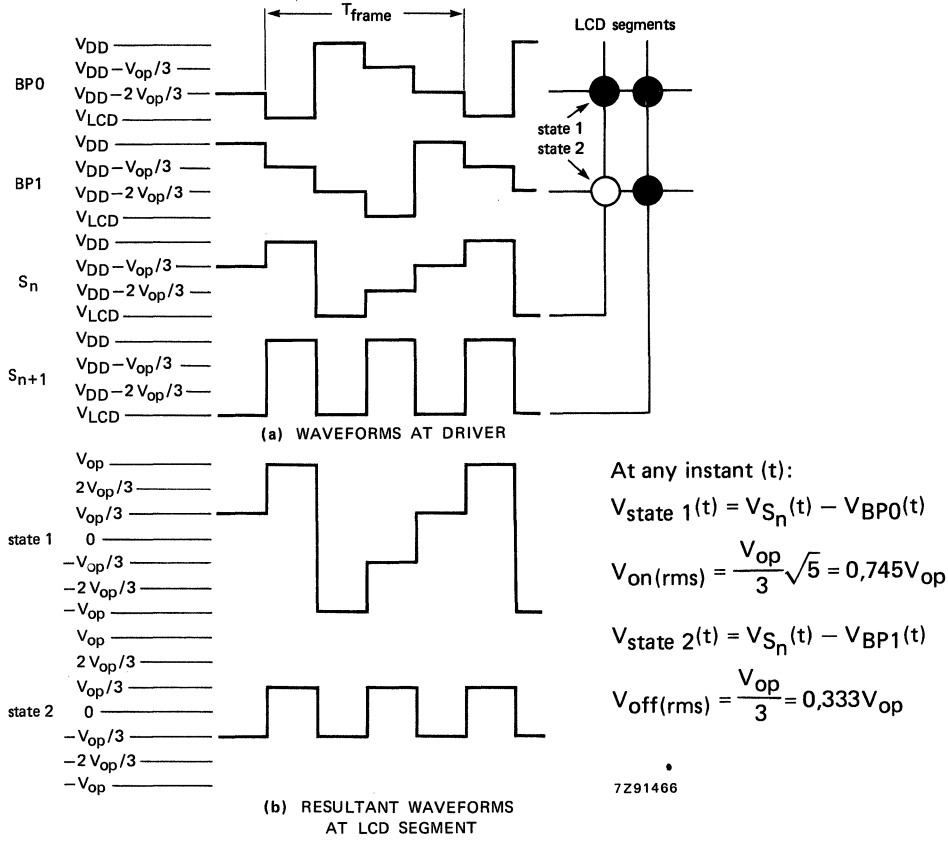


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

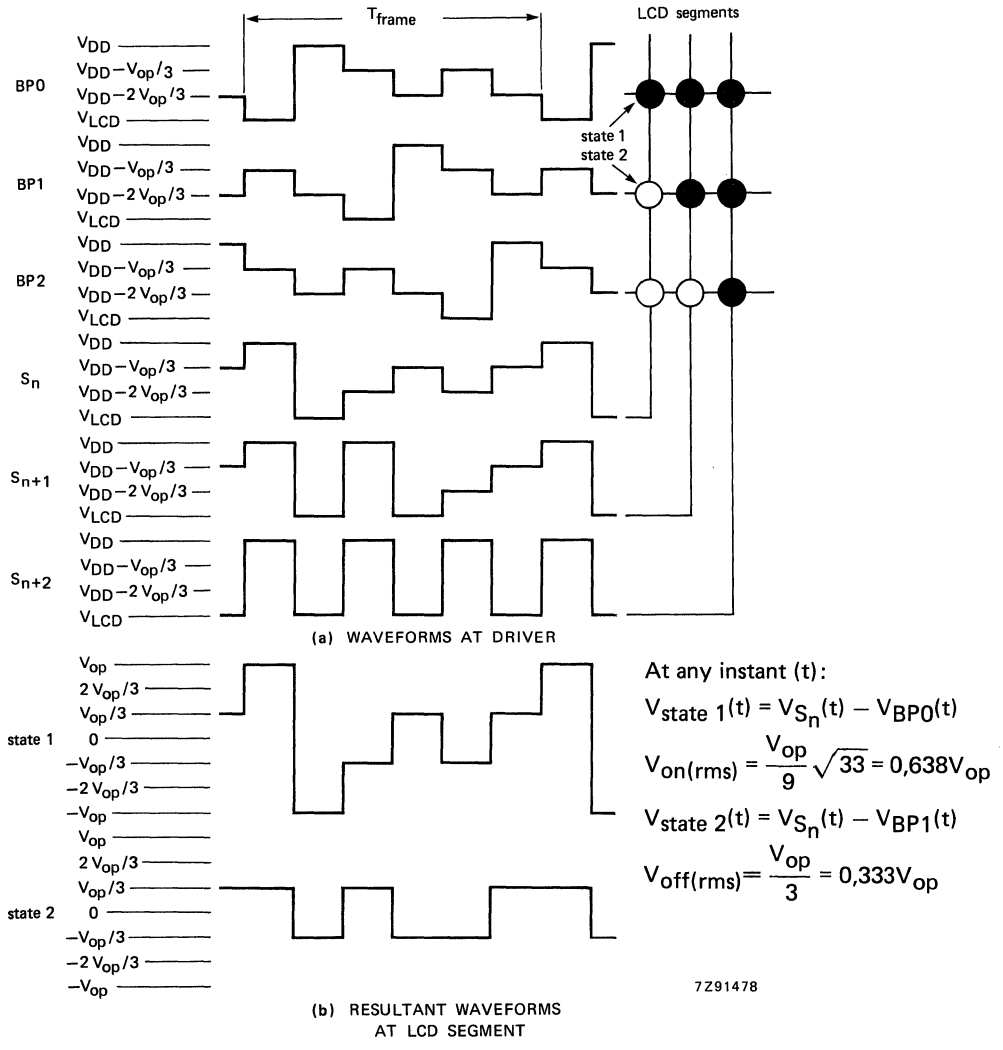


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

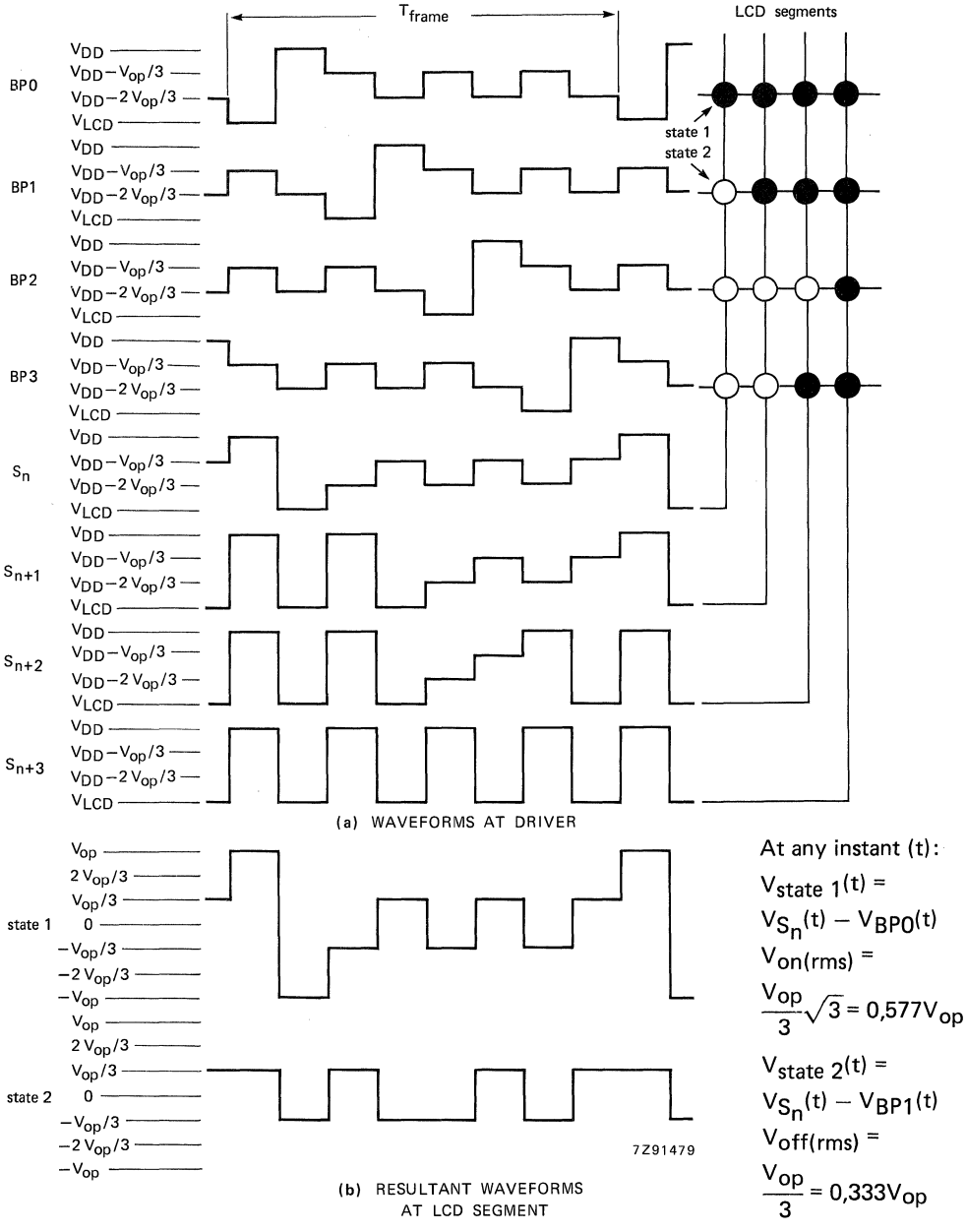


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

4

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig. 9. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

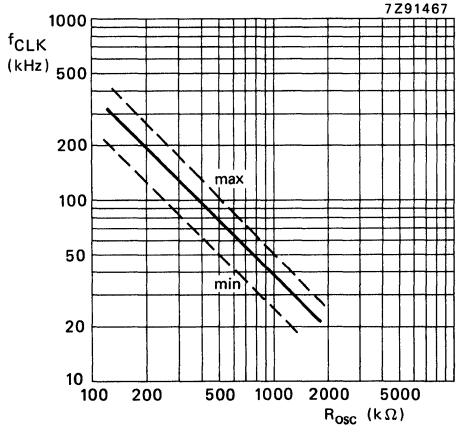


Fig. 9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3{,}6 \times 10^7 / R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	200	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{OSC} = 200 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{OSC} will be 1,2 MΩ. The reduced clock frequency and the increased value of R_{OSC} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig. 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

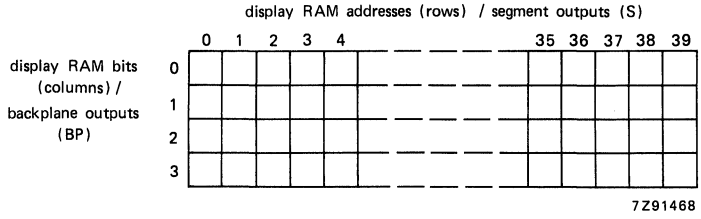


Fig. 10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

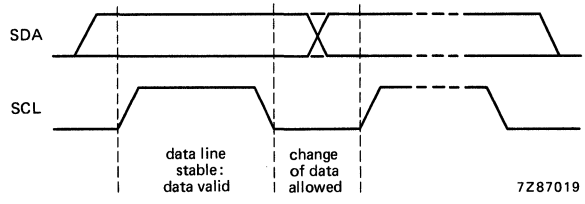


Fig. 12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

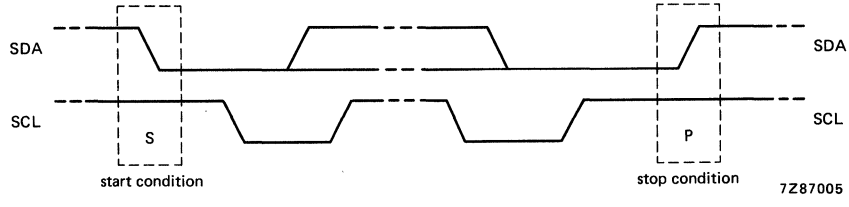


Fig. 13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

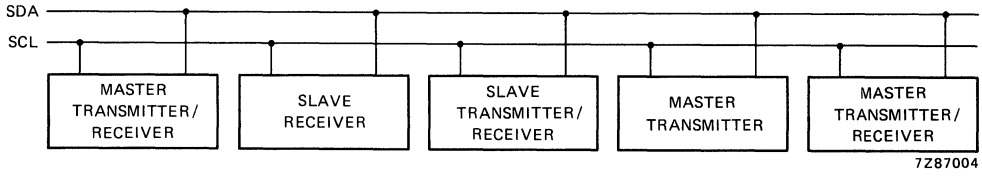


Fig. 14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

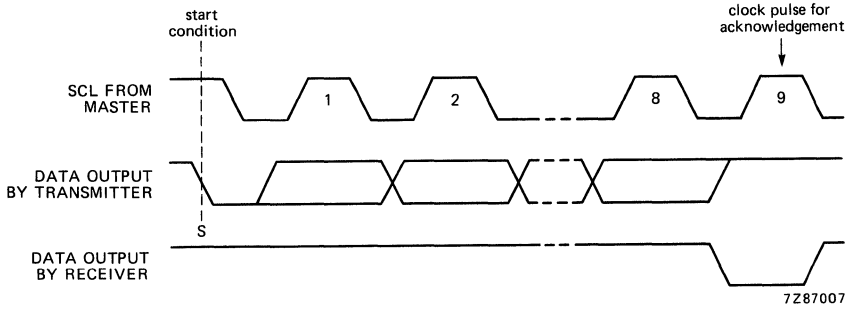


Fig. 15 Acknowledgement on the I²C bus.

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I²C bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8576s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 16. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C bus master issues a stop condition (P).

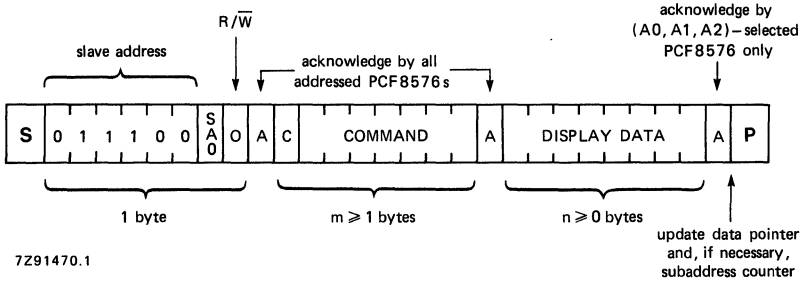


Fig. 16 I²C bus protocol.

4

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

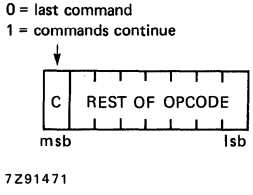


Fig. 17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>MODE SET

C 1 0 LP E B M1 M0</td><td>LCD drive mode | bits M1 M0
static (1 BP) | 0 1
1 : 2 MUX (2 BP) | 1 0
1 : 3 MUX (3 BP) | 1 1
1 : 4 MUX (4 BP) | 0 0

LCD bias | bit B
1/3 bias | 0
1/2 bias | 1

display status | bit E
disabled (blank) | 0
enabled | 1

mode | bit LP
normal mode | 0
power-saving mode | 1</td><td>Defines LCD drive mode

Defines LCD bias configuration

Defines display status
The possibility to disable the display allows implementation of blinking under external control

Defines power dissipation mode</td></tr>
<tr><td>LOAD DATA POINTER

C 0 P5 P4 P3 P2 P1 P0</td><td>bits P5 P4 P3 P2 P1 P0
6-bit binary value of 0 to 39</td><td>Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses</td></tr>
<tr><td>DEVICE SELECT

C 1 1 0 0 A2 A1 A0</td><td>bits A0 A1 A2
3-bit binary value of 0 to 7</td><td>Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses</td></tr>
</table>

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT

C | 1 1 1 1 0 | I | O</td><td>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
</td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK

C | 1 1 1 0 | A | BF1 BF0</td><td>
<table>
<tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr>
<tr><td>off</td><td>0</td><td>0</td></tr>
<tr><td>2 Hz</td><td>0</td><td>1</td></tr>
<tr><td>1 Hz</td><td>1</td><td>0</td></tr>
<tr><td>0,5 Hz</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><td>blink mode</td><td>bit A</td></tr>
<tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr>
</table>
</td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 18).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig. 19.

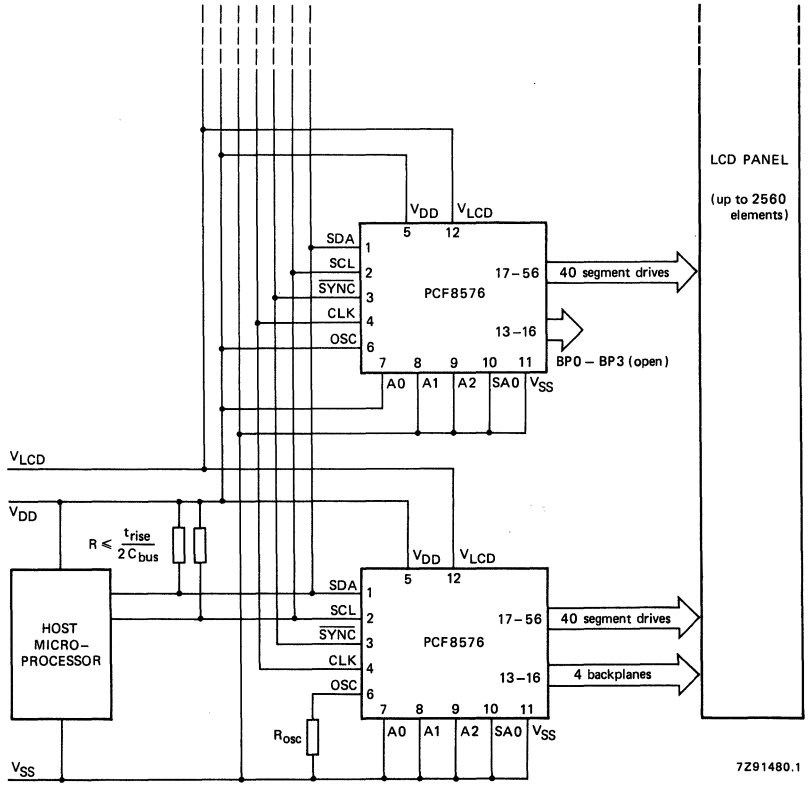


Fig. 18 Cascaded PCF8576 configuration.

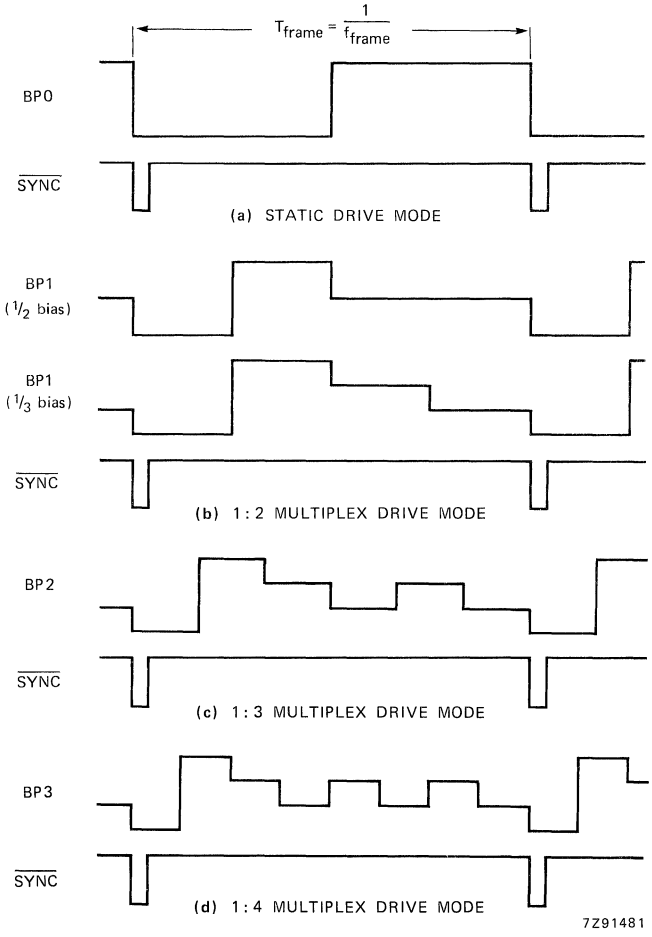


Fig. 19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see application information.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 11 V
LCD supply voltage range	V_{LCD}		V_{DD}−11 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S39; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}−2 to V_{DD}−9 V;
T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	–	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Operating supply current at f_{CLK} = 200 kHz (note 2)	I_{DD}	–	–	tbf	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	–	–	tbf	μA
LCD supply current at f_{CLK} = 200 kHz (note 2)	I_{LCD}	–	–	tbf	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	30	60	100	kΩ
Power-on reset level (note 3)	V_{REF}	0,8	1,2	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}-2$ to $V_{DD}-9$ V;
$T_{amb} = -40$ to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 200 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	200	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}-5$ V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I²C bus high-speed mode					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs
I²C bus low-speed mode					
Bus free time	t_{BUF}	105	–	–	μs
Start condition hold time	$t_{HD;STA}$	365	–	–	μs
SCL LOW time	t_{LOW}	105	–	155	μs
SCL HIGH time	t_{HIGH}	365	–	415	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	105	–	155	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	105	–	155	μs

Notes to characteristics

1. $V_{LCD} < V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty cycle; I²C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

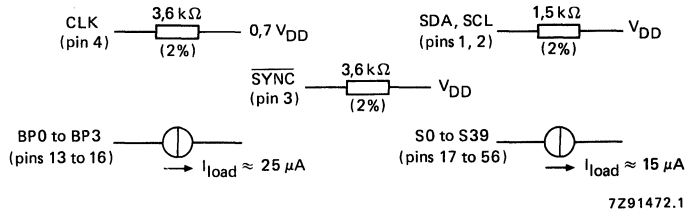


Fig. 20 Test loads.

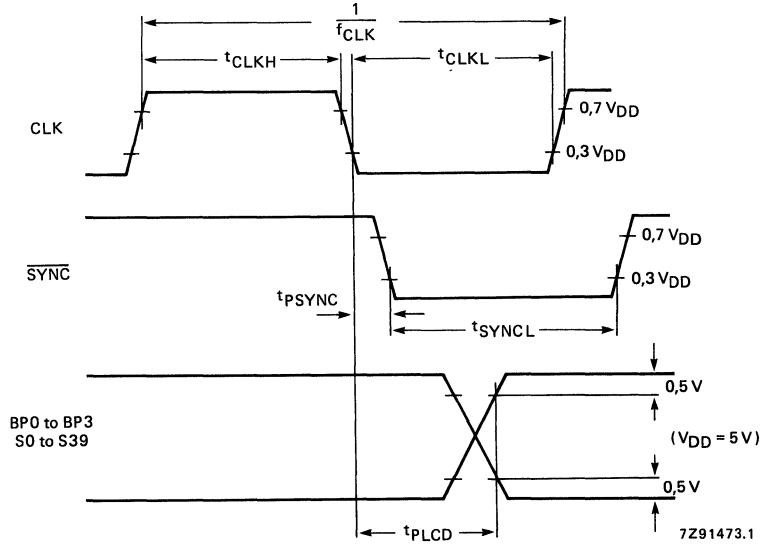


Fig. 21 Driver timing waveforms.

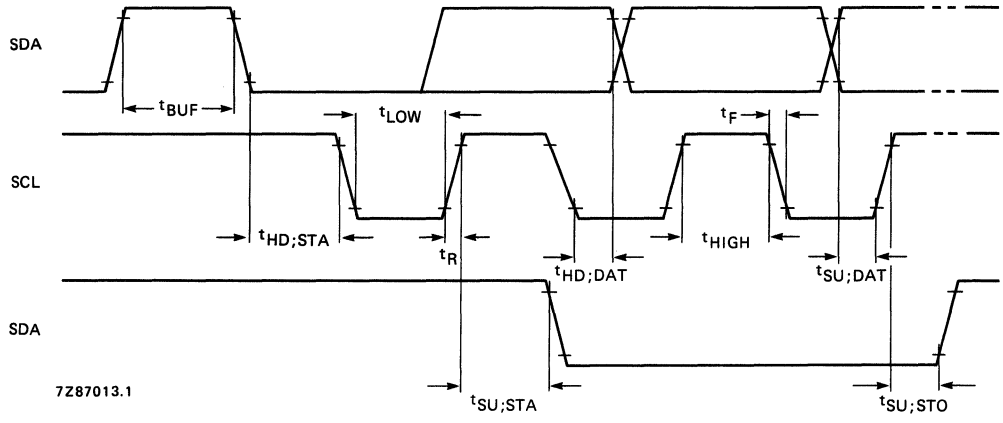


Fig. 22 I²C bus high-speed mode timing waveforms.

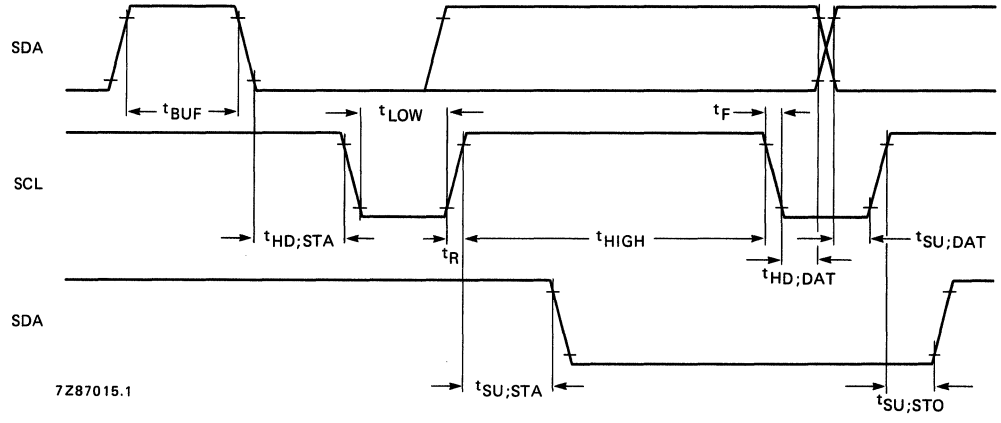


Fig. 23 I²C bus low-speed mode timing waveforms.

APPLICATION INFORMATION

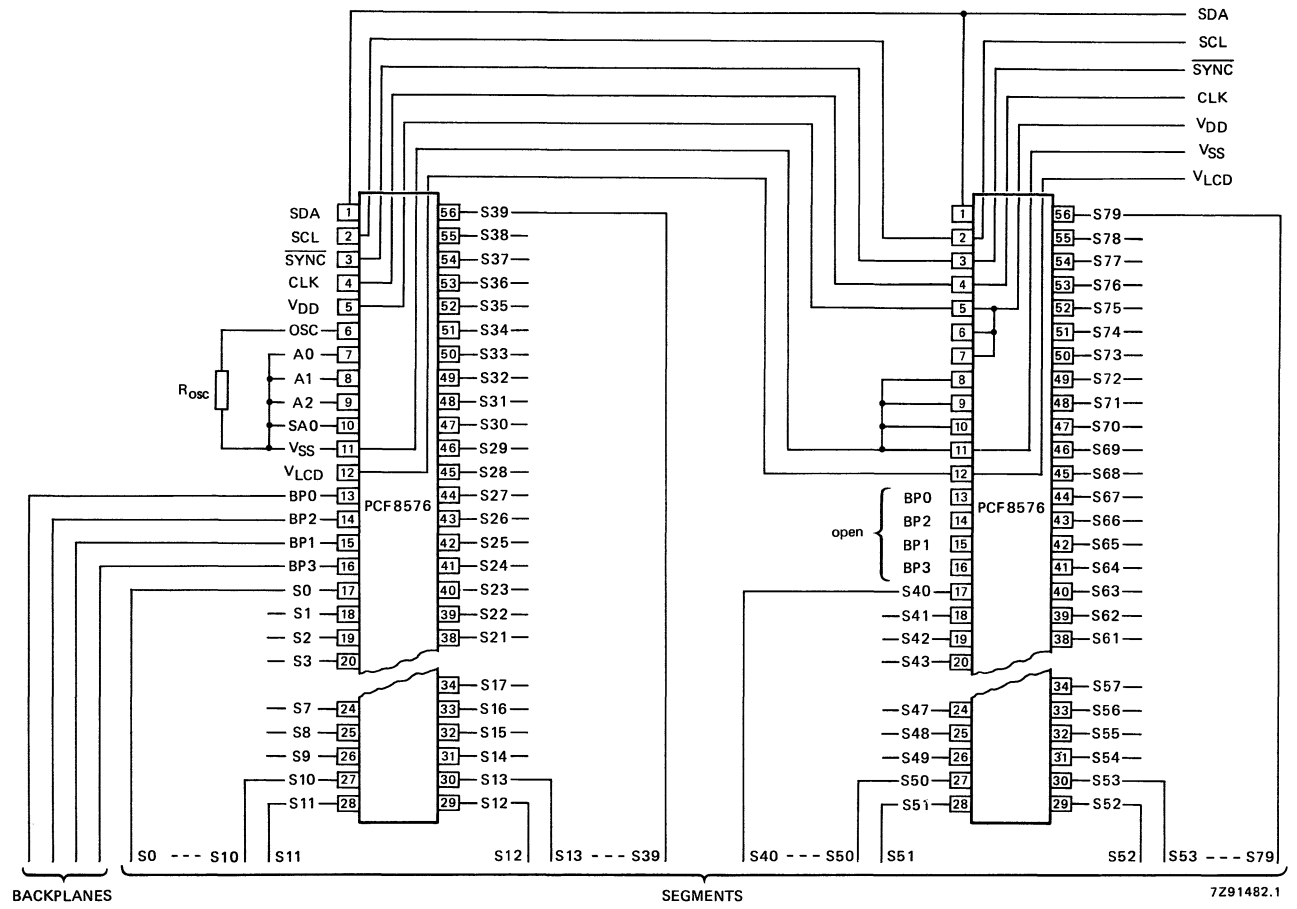


Fig. 24 Single plane wiring of packaged PCF8576s.

APPLICATION INFORMATION (continued)

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig. 25). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

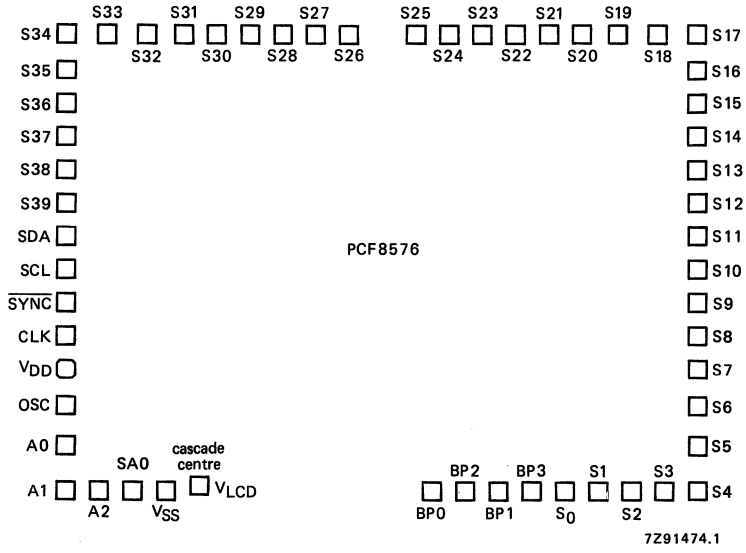


Fig. 25 PCF8576 bonding pad layout.

Fig. 26 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

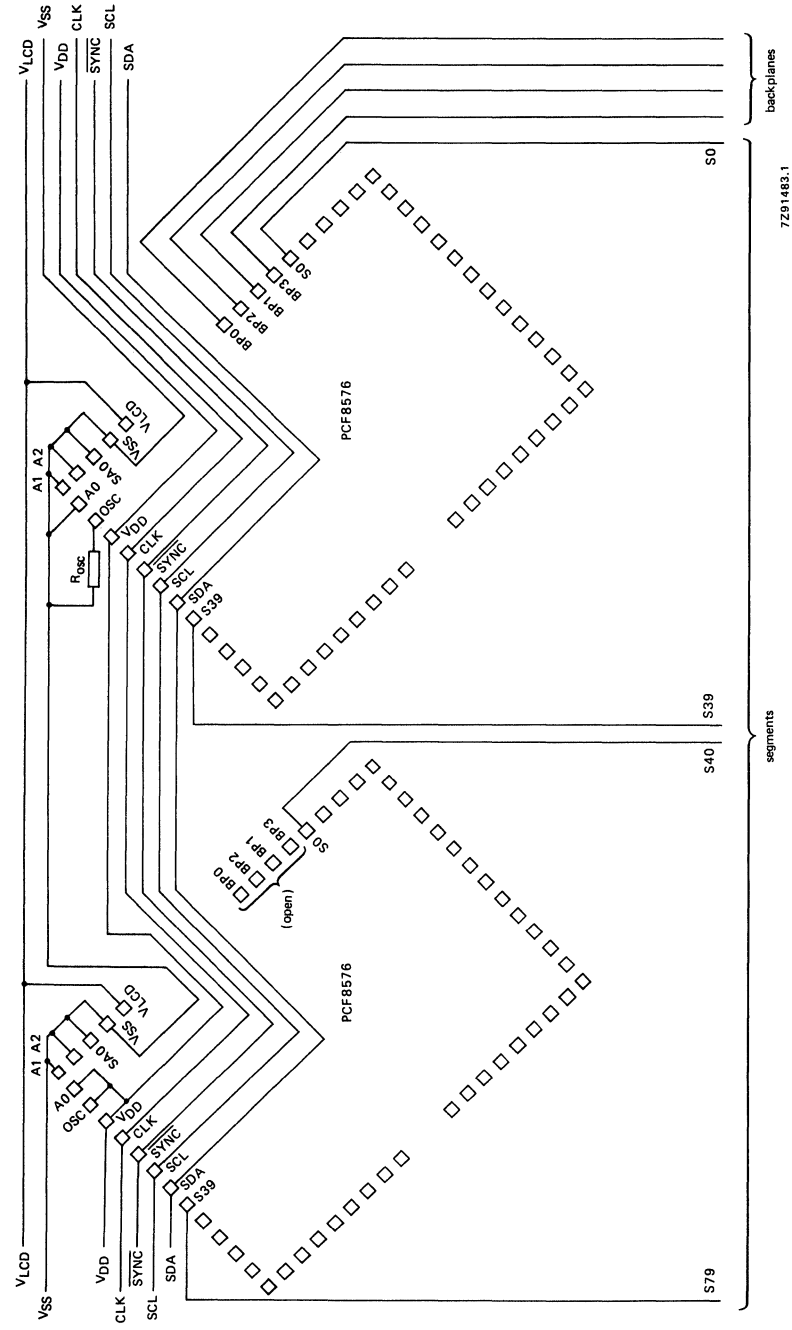


Fig. 26 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).

4

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Videlec is a joint venture of BBC Brown Boveri and Philips specializing in liquid crystal display technology to meet the requirements of original equipment manufacturers.

Videlec AG
Hardstrasse 5
Lenzburg CH5600
Switzerland.

32/64 Segment LCD Driver for Automotive — PCF8577

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I^2C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2,5 to 9 V
- Low power consumption
- I^2C bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device sub-address boundaries
- Display memory switching in direct drive mode
- May be used for I^2C bus output expander
- System expansion up to 256 segments
- Power-on-reset sets all segments off (to blank)

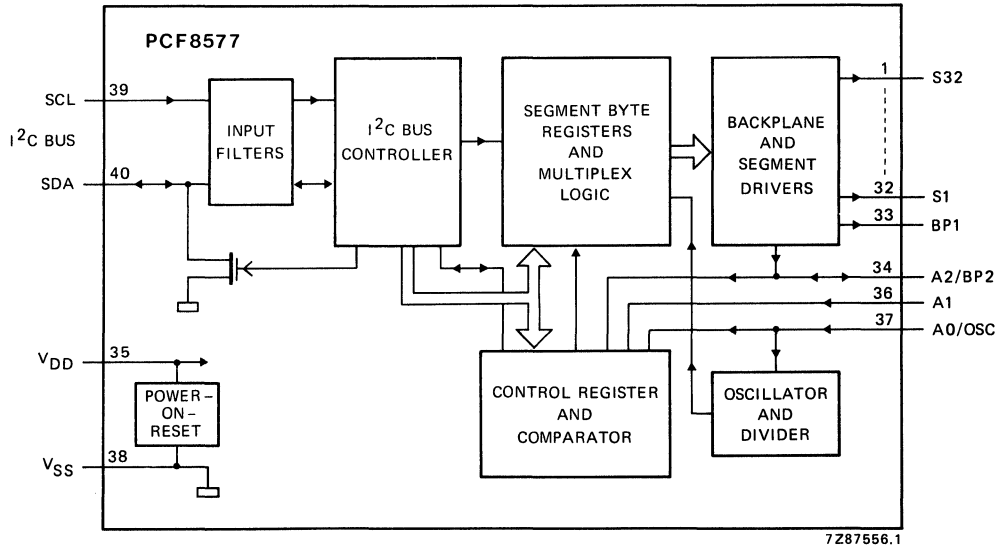


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8577P: 40-lead DIL; plastic (SOT-129).
PCF8577T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

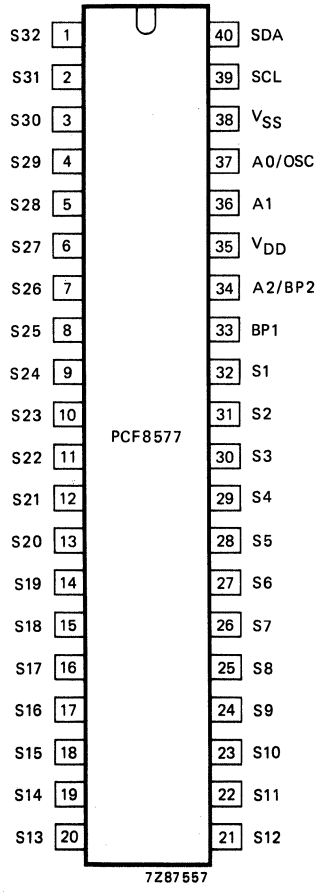


Fig. 2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C bus

40	SDA	I^2C bus data line
39	SCL	I^2C bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S1 – S32	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware sub-address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

4

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

All PCF8577 have the same slave address (see Fig. 14). All devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I^2C bus protocol Fig. 15).

The control register is shown in more detail in Fig. 3. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

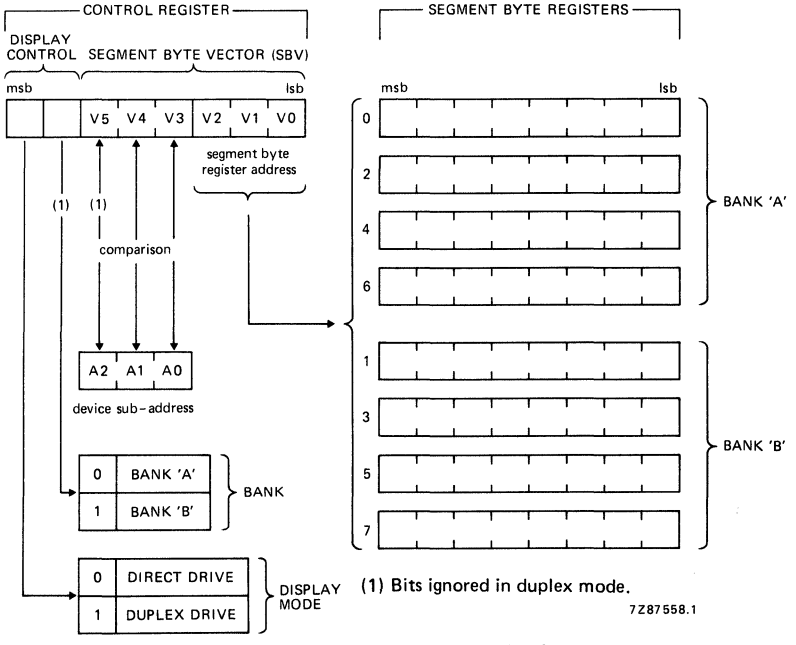


Fig. 3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

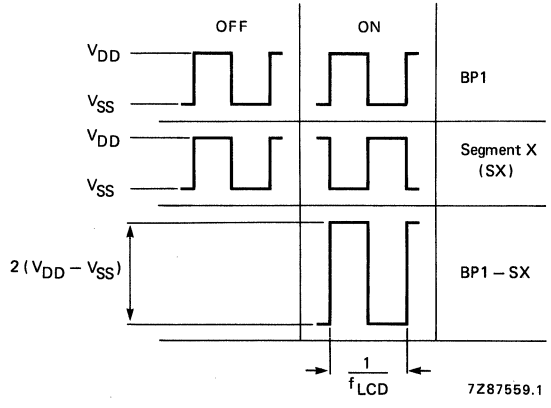
After each segment byte is loaded the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig. 4.



$V_{ON} = V_{DD} - V_{SS}$

$V_{OFF} = 0$

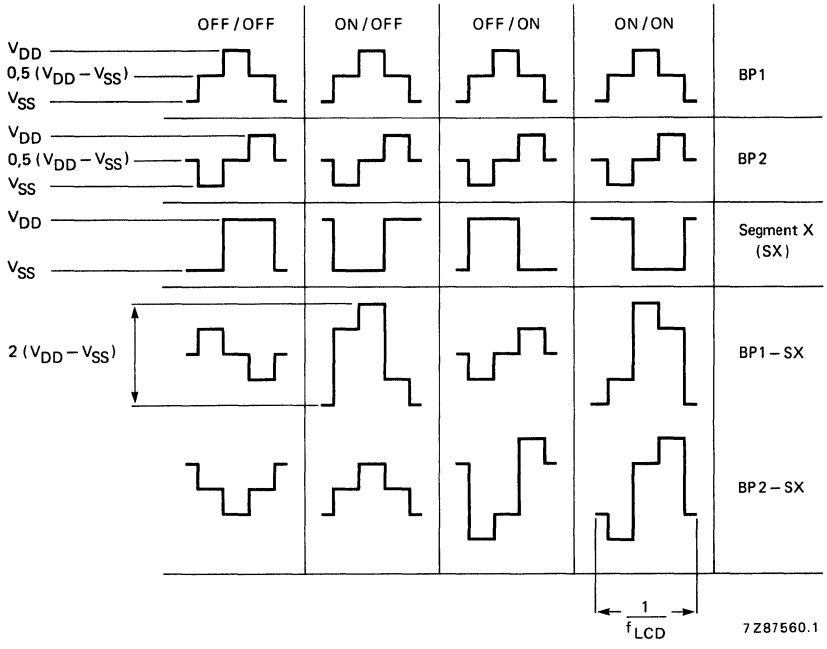
Fig. 4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig. 5.



$V_{ON} = 0{,}79\ (V_{DD} - V_{SS})$

$V_{OFF} = 0{,}35\ (V_{DD} - V_{SS})$

$\frac{V_{ON}}{V_{OFF}} = 2{,}26$

Fig. 5 Duplex mode display output waveforms.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

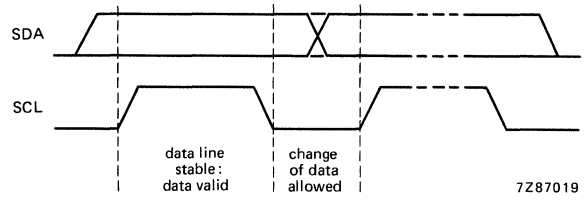


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

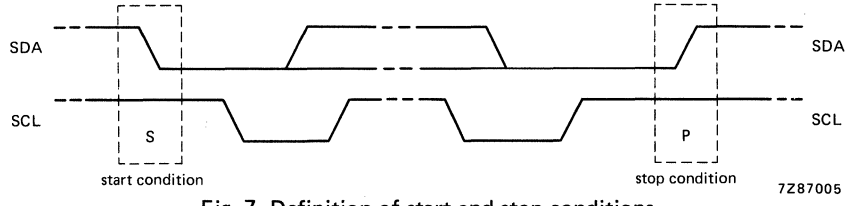


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

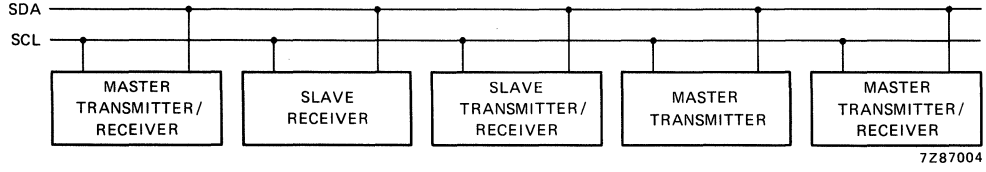


Fig. 8 System configuration.

4

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

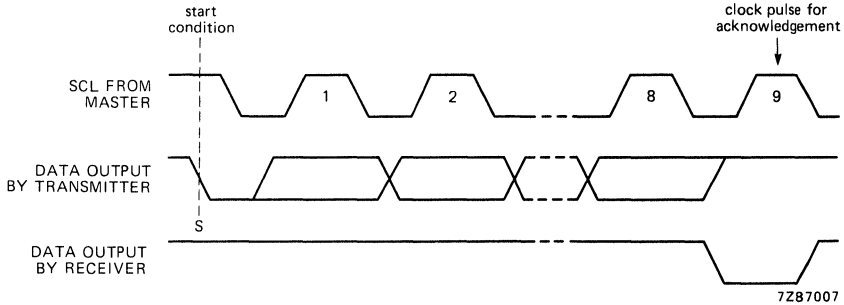


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8577 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

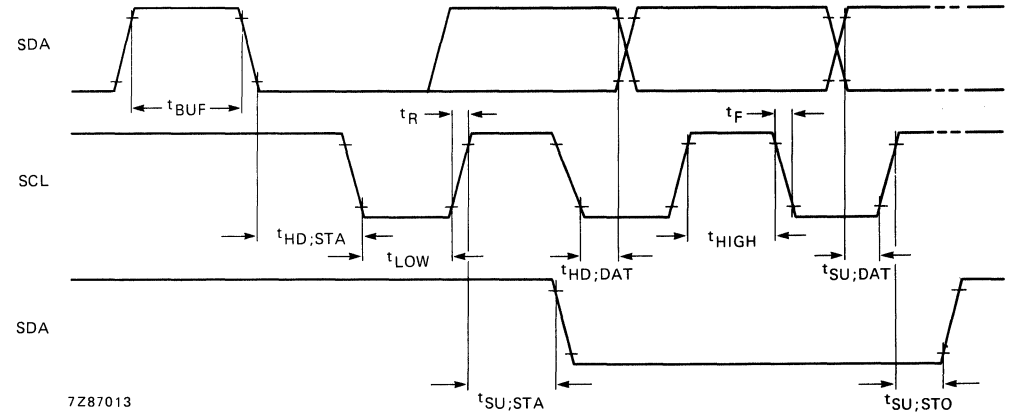


Fig. 10 Timing of the high-speed mode.

CHARACTERISTICS OF THE I²B BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

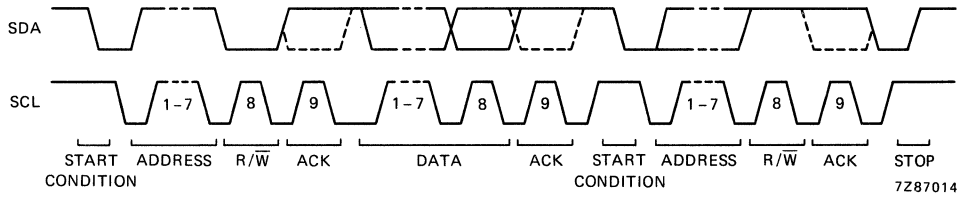


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

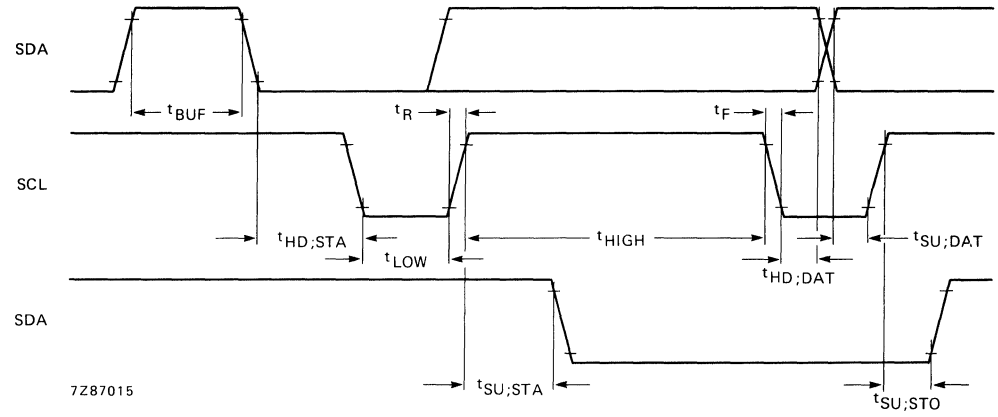


Fig. 12 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

CHARACTERISTICS OF THE I²C BUS (continued)

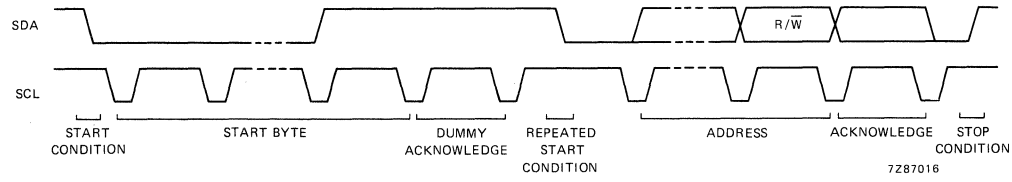


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The slave address for PCF8577 is shown in Fig. 14.

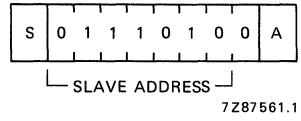


Fig. 14 PCF8577 slave address.

I²C bus protocol

The PCF8577 I²C bus protocol is shown in Fig. 15.

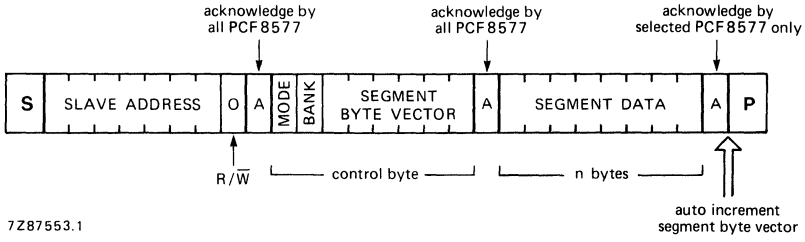


Fig. 15 I²C bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig. 14). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte – segment driver mapping in the direct drive mode

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

4

DISPLAY MEMORY MAPPING (continued)

Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte – segment driver mapping in the duplex mode

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 11	V
Voltage on any pin	V_I	V_{SS} − 0,8 to V_{DD} + 0,8	V
D.C. input current	$\pm I_I$	max. 20	mA
D.C. output current	$\pm I_O$	max. 25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$, I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 500*	mW
Power dissipation per output	P	max. 100	mW
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

* Derate 7,7 mW/K when $T_{amb} > 60$ °C.

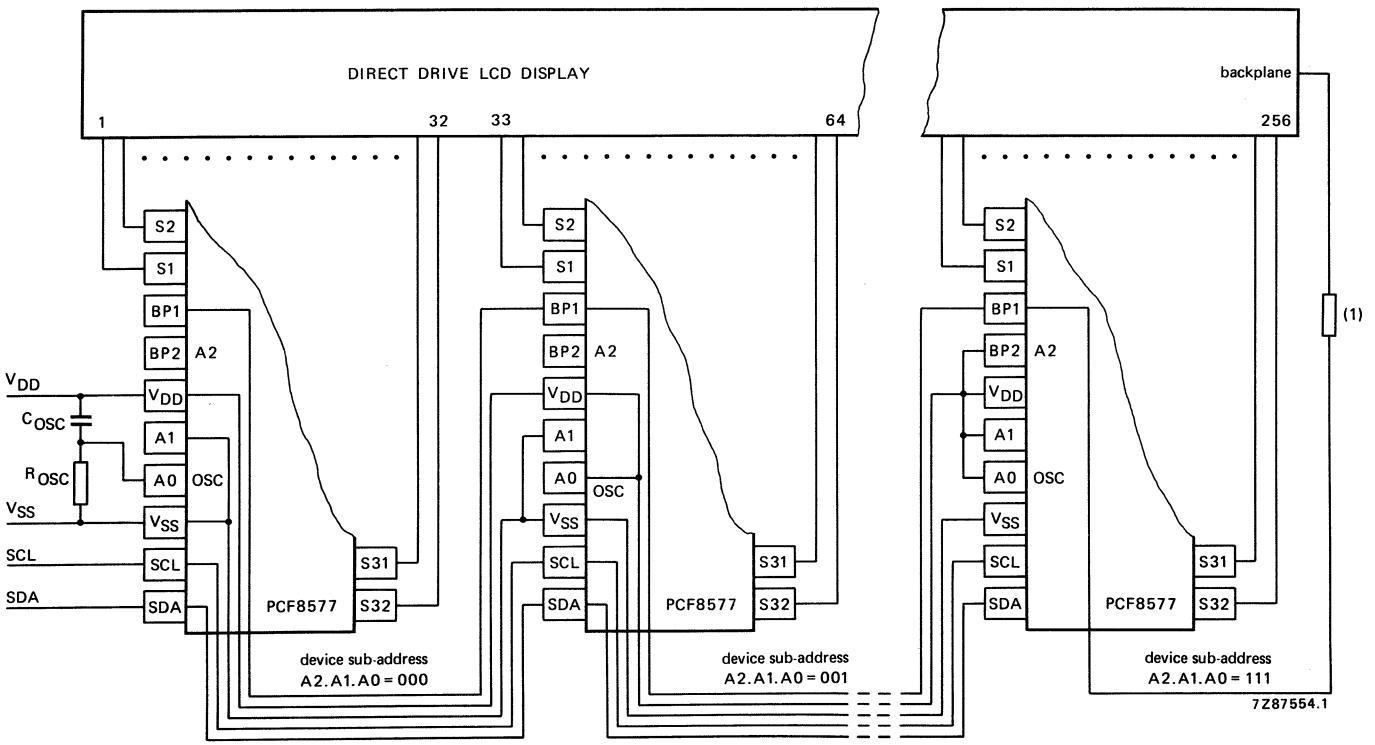
CHARACTERISTICS

V_{DD} = 2,5 to 9 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	2,5	–	9,0	V
Supply current at f_{SCL} = 100 kHz, no load, R_{OSC} = 1 MΩ	I_{DD}	–	–	250	μA
Power-on-reset level*	V_{REF}	0,9	1,3	2,0	V
Input SCL; input/output SDA					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	9,0	V
output current LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA
output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	100	nA
tolerable spike width on bus	t_{sw}	–	–	100	ns
input capacitance at $V_I = V_{SS}$	C_I	–	–	7	pF
A1 input leakage current at $V_I = V_{SS}$ or V_{DD}	I_I	–	–	100	nA
A2/BP2 input current at $V_I = V_{DD}$	I_I	–	5,0	–	μA
A0/OSC input current at $V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	5,0	–	μA
DC component of LCD driver	$\pm V_{BP}$	–	20	–	mV
Segment loads	C_{SX}	–	–	5	nF
	R_{SX}	1	–	–	MΩ
Segment output current at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL}	0,3	–	–	mA
Segment output current at $V_{OH} = V_{DD} - 0,4$ V; V_{DD} = 5 V	$-I_{OH}$	0,3	–	–	mA
Backplane load (direct drive)	C_{BP}	–	–	50	nF
	R_{BP}	100	–	–	kΩ
Backplane loads (duplex drive)	C_{BP}	–	–	35	nF
	R_{BP}	100	–	–	kΩ
Rise and fall times ($V_{BP} - V_{SX}$) at maximum load	t_r, t_f	–	–	200	μs
Display frequency at C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz

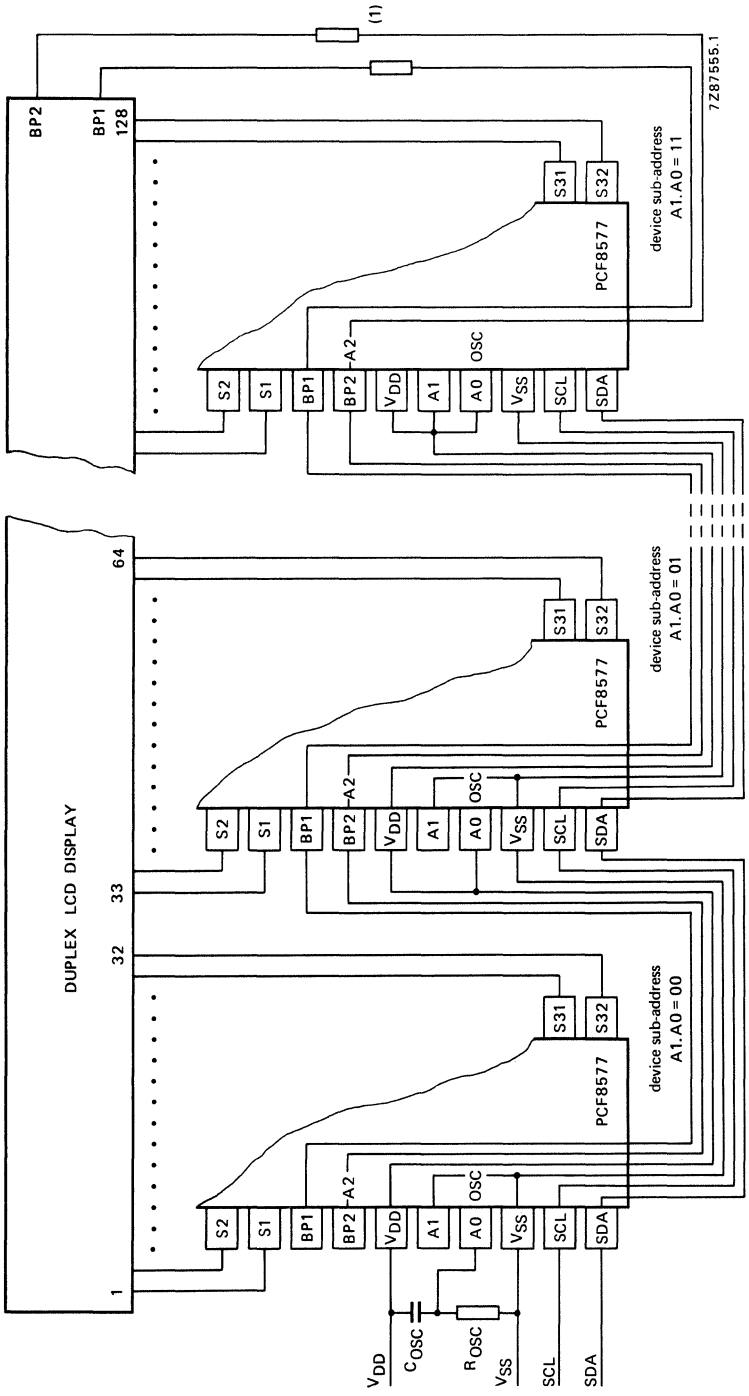
* The power-on-reset circuit resets the I^2C bus logic with $V_{DD} < V_{REF}$.

APPLICATION INFORMATION



(1) The series resistance of the display backplane must be greater than 1 kΩ.

Fig. 16 Direct drive display; expansion to 256 segments using eight PCF8577.



(1) The series resistances of the display backplanes must be greater than 1 kΩ.

Fig. 17 Duplex display; expansion to 2 x 128 segments using four PCF8577.

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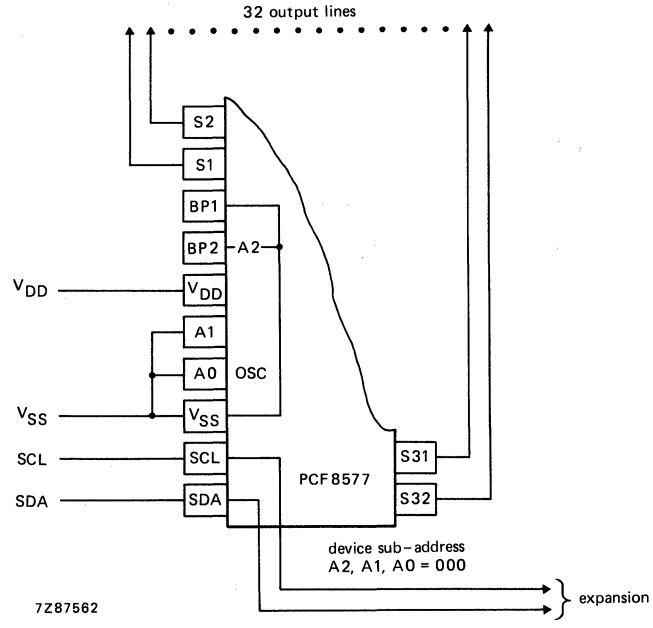
APPLICATION INFORMATION (continued)



Notes

1. MODE bit must always be set to 0 (direct drive)
2. BANK switching is permitted
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation)

Fig. 18 Use of PCF8577 as 32-bit output expander in I^2C bus application.

LED Display/Interface Circuit SAA1060

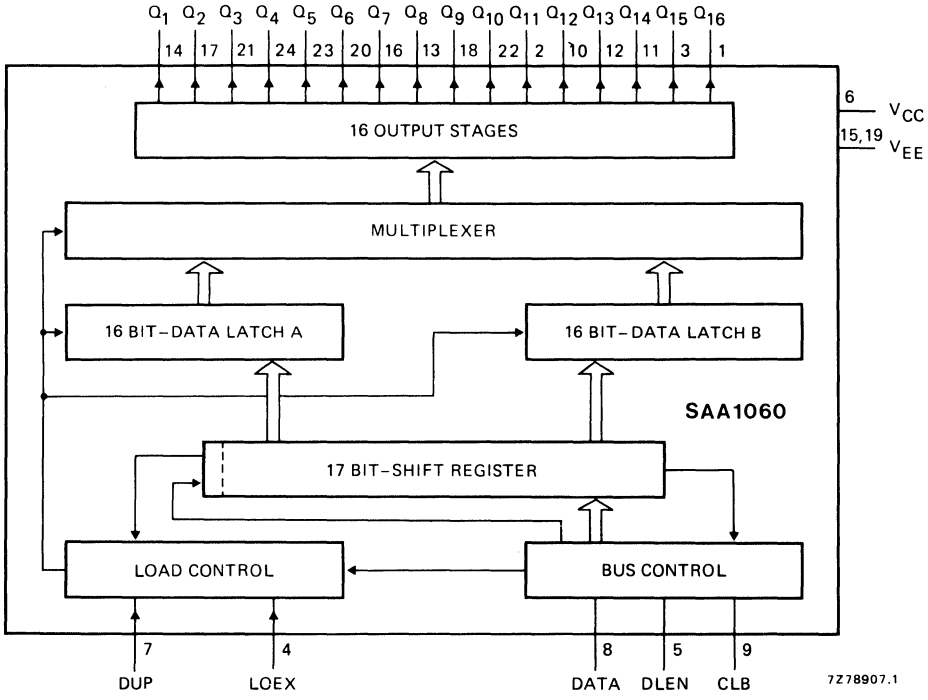


Fig. 1 Block diagram.

Features

- Driving 7, 14, 16-segment displays.
- Driving linear displays, bar graph displays for analogue functions.
- Serial to parallel decoder.
- Bus control for the selection of 18-bit words.
- 2 x 16-bit latch.
- Duplex operation for two modes of output: static (16 bit) or dynamic (2 x 16 bit).
- Data transfer control.
- 2 outputs for higher output current (80 mA).

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4 to 6 V
Operating ambient temperature range	T_{amb}		−20 to + 80 °C
Maximum input frequency	f_I	typ.	50 kHz
Supply current	I_{CC}	typ.	60 mA
Output current	I_Q	<	40 mA
Output current (Q_8 and Q_{16} only)	I_Q	<	80 mA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The integrated circuit SAA1060 is primarily designed to drive the display unit of a digital tuning system. It can also be used as a 16-bit serial to parallel decoder. Since the device has no decoder (this is handled by a microcomputer), it has many applications:

- driving 7-segment displays
- driving 14-segment displays
- driving linear displays, e.g. pointer, bar graph
- static output of switch-functions
- digital to analogue converter, with external R-2R network
- extension of the number of outputs for microprocessors or microcomputers.

Data transmission is initiated by means of a burst of clock pulses (CLB), a data line enable signal (DLEN) and the data signal (DATA). The bus control circuit distinguishes between interference and valid data by checking word length (17 bits) and the leading zero. This allows different bus information to be supplied on the same bus lines for other circuits (e.g. SAA1056 with 16 bits).

The last bit (bit 17) of the data word contains the information which of the two internal latches will be loaded. The input LOEX determines if the latched data of selected latches is presented directly to the outputs, or synchronized with the data select signal DUP.

The output stages are n-p-n transistors with open collectors. The current capability is designed for the requirements of duplex operation. Two of the outputs (Q_8 and Q_{16}) are arranged for double current, so that 2 x 2 segments can be connected in parallel.

OPERATION DESCRIPTION

Data inputs (DLEN, DATA)

The SAA1060 processes serially the 18-bit data words synchronized with the clock burst (CLB) and applied to the data input DATA. A command will be accepted only when the data line enable input (DLEN) is HIGH (see Fig. 3).

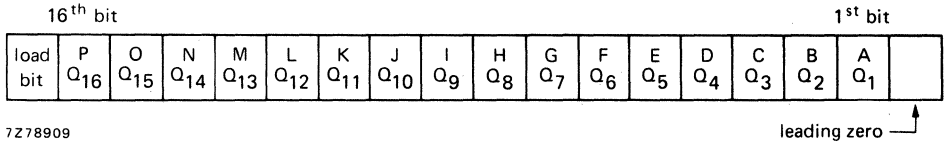


Fig. 2 Organization of a data word.

Condition for 17th bit:
0 = load data latch B
1 = load data latch A

The loading of the accepted information in one of the data latches is done by the 19th clock pulse, when DLEN is LOW.

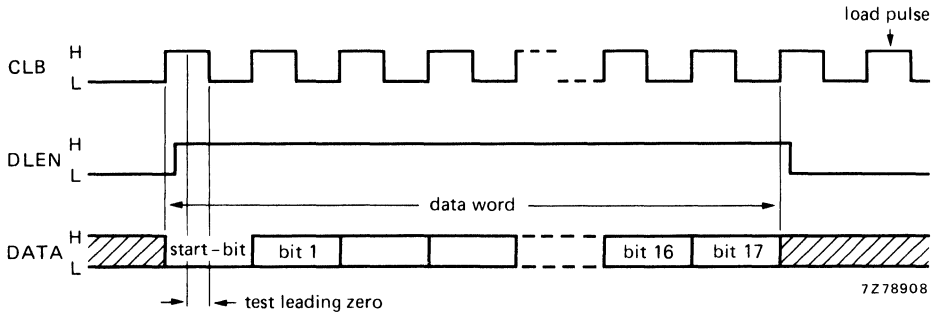


Fig. 3 Pulse diagram of the 16-bit data transmission.

Each data word must start with a leading zero. The SAA1060 checks the data word for the correct length (18 bits) and also for the leading zero.
The actual data is switched directly to the appropriate outputs. For switching on a segment, a '0' (LOW) is necessary at the appropriate data bit.

Data selection input (DUP)

The logic states at input DUP determine which of the two latch contents can be found on the output.

0 = latch A contents
1 = latch B contents

Load control input (LOEX)

Input LOEX determines the operation mode in which the device is able to work.

0 = duplex mode, i.e. output synchronized with the duplex signal
1 = d.c. mode, i.e. output direct from the by DUP selected data latch.

When operating in duplex mode at 50 Hz, the time between two data words to be transmitted must be > 21 ms.

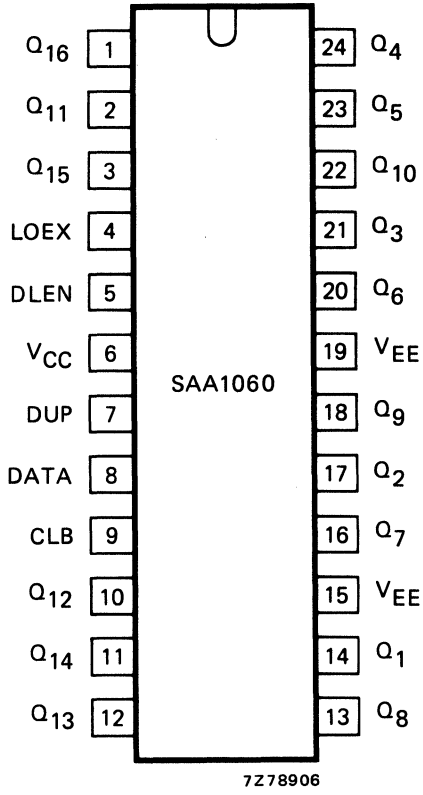


Fig. 4 Pinning diagram.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}	−0,3 to + 7	V
Total power dissipation	P_{tot}	max. 900	mW
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Storage temperature range	T_{stg}	−25 to + 125	°C

CHARACTERISTICS

V_{EE} = 0; T_{amb} = 25 °C; unless otherwise specified

	V_{CC} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{CC}	4	5	6	V	
Supply current	5	I_{CC}	–	60	–	mA	
Inputs DATA, CLB, DLEN, LOEX							
input voltage HIGH	5	V_{IH}	2	–	5	V	
input voltage LOW	5	V_{IL}	–	–	1	V	
input current LOW	5	$-I_{IL}$	–	–	20	μA	V_I = 0
maximum input frequency	5	f_I	–	50	–	kHz	
Input DUP							
input voltage HIGH	5	V_{IH}	0,8	–	12	V	
input voltage LOW	5	V_{IL}	–6	–	0,4	V	
input current HIGH	5	I_{IH}	0,01	–	12	mA	
maximum input frequency	5	f_I	–	50	–	kHz	
Outputs Q_1 to Q_7, Q_9 to Q_{15}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	I_{QH} = 0
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 40 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	60	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	20	40	mA	
Outputs Q_8 and Q_{16}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	I_{QH} = 0
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 80 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	120	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	40	80	mA	

16 Segment LED Driver — SAA1061

The SAA1061 is a MOS N-channel output port expander circuit, which converts serial input data into parallel output information. The IC is used in combination with a microcomputer.

Features

- Bus control for the selection of 18-bit words.
- 16-bit latch and low-ohmic driver outputs.
- Pin compatible with the SAA1060, except the SAA1061 has no duplex mode.
- Address selection inputs; up to four SAA1061 circuits can be operated from a common CBUS.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	typ.	5 V
Operating ambient temperature range	T_{amb}		−20 to +80 °C
Supply current	I_{DD}	typ.	9 mA
Output current per output	I_O	typ.	15 mA

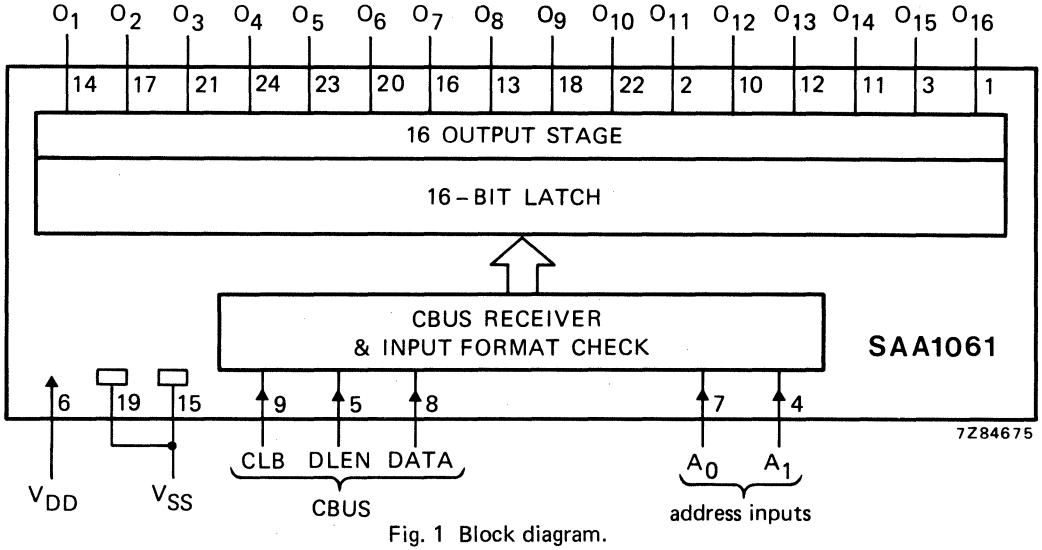


Fig. 1 Block diagram.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

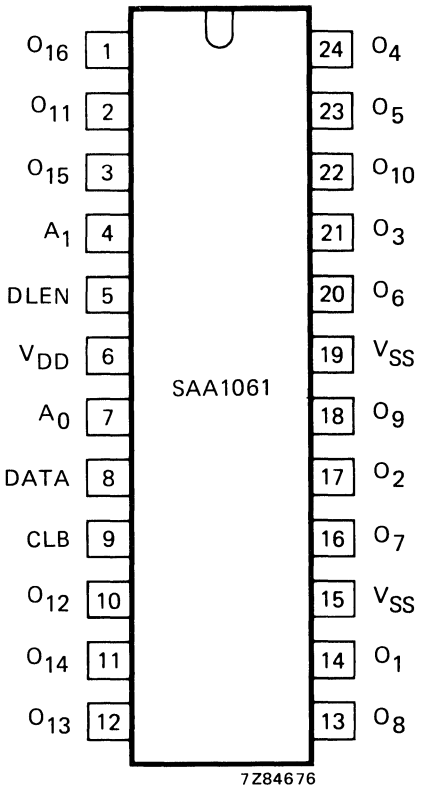


Fig. 2 Pinning diagram.

PINNING

6	V_{DD}	positive supply (+5 V)
15, 19	V_{SS}	ground (0 V)

Inputs

8	DATA	data word	CBUS
9	CLB	clock burst	CBUS
5	DLEN	data line enable	CBUS
7	A_0	address bit S0	
4	A_1	address bit S1	

Outputs

14	O_1	driver outputs O_1 to O_{16} corresponding with the data bits 1 to 16 of the data word
17	O_2	
21	O_3	
24	O_4	
23	O_5	
20	O_6	
16	O_7	
13	O_8	
18	O_9	
22	O_{10}	
2	O_{11}	
10	O_{12}	
12	O_{13}	
11	O_{14}	
3	O_{15}	
1	O_{16}	

4

GENERAL DESCRIPTION

The SAA1061 is an addressable output port expander for use in microcomputer controlled systems. It converts serial input data into parallel output information. The circuit comprises a CBUS receiver, logic to check input format, a 16-bit serial/parallel converter, latches and drivers for the parallel outputs.

This universal device can be used for e.g.:

- static output of switch-functions
- extension of the number of outputs for microcomputers or microprocessors
- driving maximum 16-segment LEDs; e.g. 7, 4 or 16-segment displays
- driving linear displays (pointer, bar graph)
- digital to analogue conversion with external resistor network.

The data is transmitted via the 3-line CBUS from the microcomputer. If the data transmission is valid, the data are transferred by a load pulse via the latch to the driver output. Each data transmission is checked for word length (18-bit) by the on-chip word format control circuitry. This allows different bus information to be supplied on the same bus lines for other circuits.

The address inputs A_0 and A_1 determine four address possibilities. A data transmission only takes place if the programmed addresses correspond with the address bits S0 and S1.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to +7,5	V
Input voltage range	V_I	−0,3 to +15	V
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,3 to +16,5	V
Output current per output	$\pm I_O$	max. 20	mA
Power dissipation per output	P_O	max. 7,5	mW
Total power dissipation per package	P_{tot}	max. 300	mW
Operating ambient temperature range	T_{amb}	−20 to +80	°C
Storage temperature range	T_{stg}	−20 to +125	°C

CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 5 V; T_{amb} = −20 to +80 °C; unless otherwise specified

	symbol	min.	typ.	max.	conditions
Supply voltage	V_{DD}	4,5	5	5,5 V	
Supply current	I_{DD}	–	–	20 mA	
Inputs CLB, DLEN, DATA, A_0, A_1					T_{amb} = 25 °C
Input voltage LOW	V_{IL}	−0,3	–	0,8 V	
Input voltage HIGH	V_{IH}	2,0	–	15 V	
Input leakage current	I_{IR}	–	–	1 μA	V_I = −0,3 to +15 V
Outputs O_1 to O_{16} (open drain)					
Output voltage LOW	V_{OL}	–	–	0,65 V	I_{OL} = 15 mA
Output leakage current HIGH	I_{OH}	–	–	20 μA	V_{OH} = 16,5 V
Rise and fall times	t_r, t_f	–	–	10 μs	V_{OL} = 1,5 V; V_{OH} = 13,5 V
CBUS timing					
Rise and fall times	t_r, t_f	–	–	2 μs	see Fig. 3
Data set-up time DATA → CLB	t_{SUDA}	400	–	– ns	see Fig. 3
Data hold time DATA → CLB	t_{HDDA}	250	–	– ns	see Fig. 3
Enable set-up time DLEN → CLB	t_{SUEN}	400	–	– ns	see Fig. 3
Disable set-up time CLB → DLEN	t_{SUDI}	600	–	– ns	see Fig. 3
Set-up time DLEN → CLB (load pulse)	t_{SULD}	400	–	– ns	see Fig. 3
CLB pulse width HIGH/LOW	t_{WH}, t_{WL}	450	–	– ns	see Fig. 3

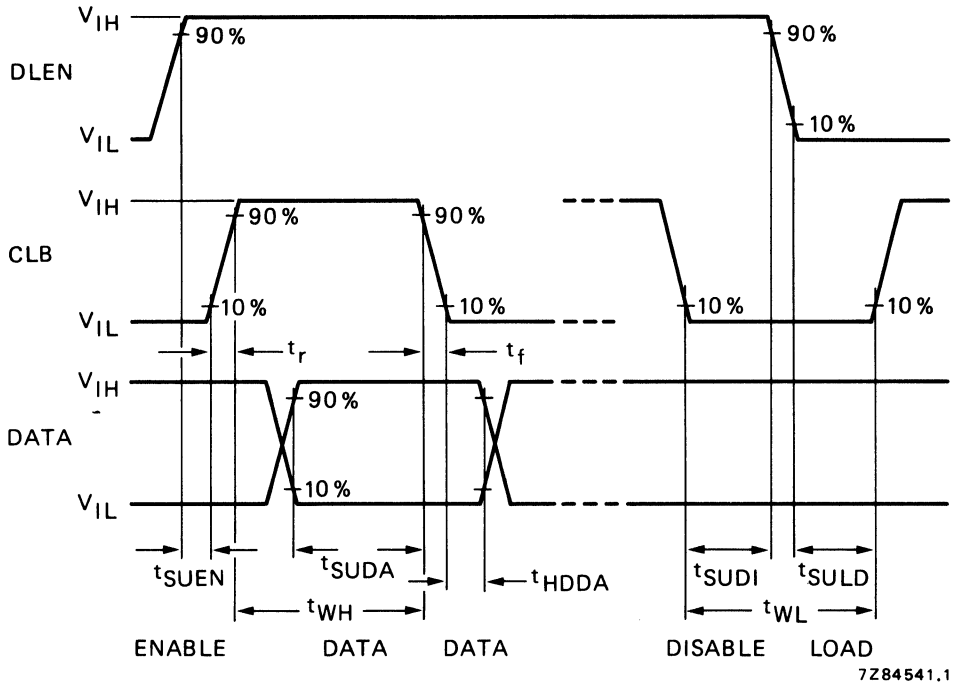


Fig. 3 CBUS timing.

OPERATION DESCRIPTION

1. CBUS transmission

The data words are entered via a serial CBUS interface. A clock burst of 18 clock periods is used to transmit the 16-bit data word, plus 2 identifier bits.

Serial data words, which are synchronized with the clock burst (CLB), are accepted if the enable input DLEN is HIGH at the same time. Each transmission is checked for word length (number of clock pulses during DLEN is HIGH) and the address bits S0 and S1.

The valid data flag is only set if:
1. Word length is correct; 2 address bits and 16 data bits.
2. Address bits S0 and S1 correspond with A_0 and A_1.

Loading the information into the selected latch register is done by the load pulse (first clock pulse after the HIGH-to-LOW transition of DLEN) if the address bits correspond with A_0 and A_1. The load pulse or a new LOW-to-HIGH transition of DLEN resets the valid data flag. Only after the valid data flag is reset, will new data be accepted.

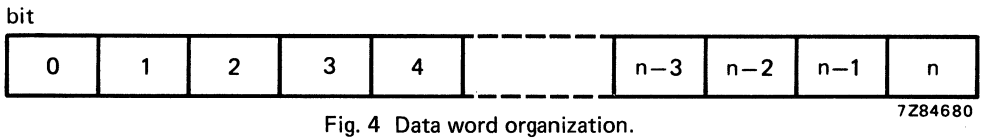


Fig. 4 Data word organization.

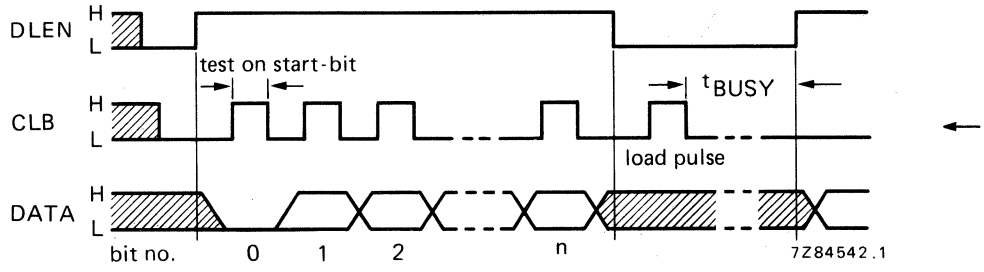


Fig. 5 CBUS data transmission.

Definitions to Figs 4 and 5:

- Word length: number of clock pulses during DLEN is active (HIGH); n + 1 bits = 18 bits.
- Bit number 0 is for the SAA1061 S0.
- Data bits: bit numbers 1 to n-1 (16-bits); bit no. n is S1.
- Load pulse: first clock pulse after DLEN returns to inactive (LOW).

2 Address inputs A_0 and A_1

The 1st bit (bit S0) and the 18th bit (bit S1) of the data word are the address bits.
Data is accepted only if the addresses correspond to the programmed addresses at inputs A_0 and A_1, that is for:

A_0 = S0 and A_1 = S1.

3 Data outputs O_1 to O_{16}

The outputs O_1 to O_{16} correspond with the data bits 1 to n-1 (16-bits). The open drain driver outputs (O_1 to O_{16}) are switched to ground (O_n = LOW), if the corresponding data bit is LOW,

4 Power-on reset

The circuit generates internally a reset-cycle after switching on the supply and the outputs become high-ohmic (HIGH).

LCD Display/Interface Circuit

SAA1062A
SAA1062AT

GENERAL DESCRIPTION

The SAA1062A is designed to drive a Liquid Crystal Display (LCD) of a digital tuning system. It contains a shift register with programmable length (18 or 21 bits), latches, both synchronized or static, exclusive-OR segment drivers (17 or 20 bits), an l.f. oscillator and a backplane driver for the LCD. The circuit is designed to be driven by a 3 bus structure from a microcomputer and can also be used as a programmable 17 or 20 bits serial-to-parallel decoder. It is also capable of storing 40 bits of information.

Features

- Driving 7 to 20-segment displays.
- Driving linear displays.
- Serial to parallel decoder of digital signals.
- Bus control for the selection of 18/21-bit words.
- 17/20-bit latch.
- A.C. segment drive.
- On-chip oscillator.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	4,2 to 5,5	V
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Maximum input frequency	f_i	typ. 50	kHz
Supply current	I_{CC}	typ. 3,5	mA
Output current (Q_1 to Q_{20})	I_Q	> 60	μA

PACKAGE OUTLINES

SAA1062A : 28-lead DIL; plastic (SOT-117).
SAA1062AT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

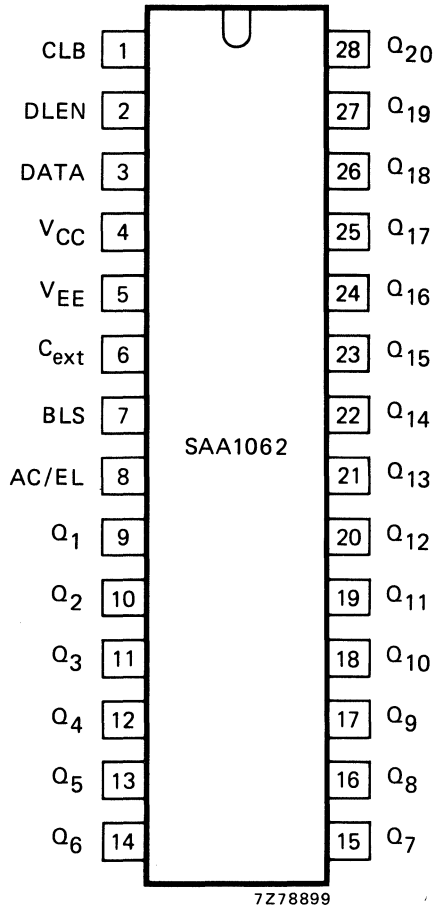


Fig. 1 Pinning diagram.

DEVELOPMENT SAMPLE DATA

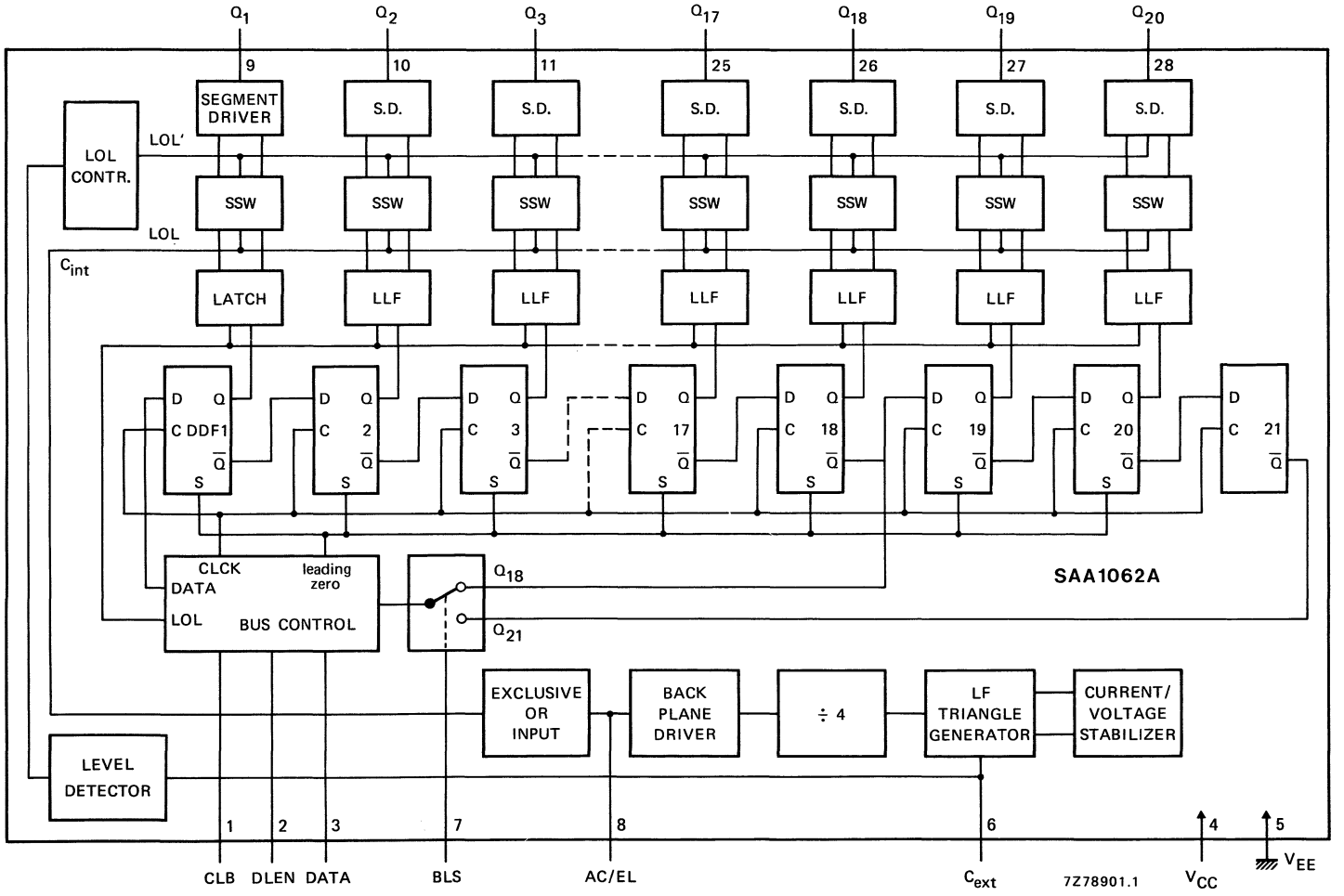


Fig. 2 Block diagram.

OPERATION DESCRIPTION

The input information for this device consists of a data bus with 18 or 21 bits words, an external clock synchronized with the data bus and an enable signal. The organization of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is made whether these signals are valid for the device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal is HIGH, during the first HIGH period of the clock signal. During the HIGH period of DLEN, the length control determines if the clock signal consists of the programmed number of pulses (18 or 21). This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device from accepting inferferences on the signal lines. While leading zero is detected, the shift register is set and for a proper leading zero the following data is shifted into this register. The Q_n position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input are correct. Incorrect length of the information is detected by checking the value of the last bit of the programmed register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOL).

This pulse enables the load control circuit to load the contents of the register into the output latch immediately. On the first edge of the backplane driver signal "AC out/EL in" following on this "LOL" pulse, the new information of this latch is transferred to the output driver which also contains a latch. With this ability it is possible to load the device with 20 bits and also to transfer this data to the segment outputs. Furthermore, the SR can be reloaded by a second complete load procedure without a load enable clock pulse. This causes the SR to contain 20 bits and the output latches another 20 bits of information.

The output driver also contains an EXCLUSIVE-OR which is driven by the backplane driver signal and the latch output. The segment driver output signal is in phase with the output of the backplane driver when the input data is HIGH ("1") and 180° out-of-phase when the input data is LOW ("0").

In the static or slave mode, the backplane output can be used as input by connecting pin 6 to ground or V_{CC}. The IC now can operate as a static driver or as a synchronized slave.

The l.f. oscillator consists of a triangle generator of the I-2I principle. It only needs an external capacitor to fix the frequency. As both amplitude and current are temperature compensated, this frequency is more or less independent of pn temperature. An internal switching signal of this generator is divided by 4 to attain a symmetrical output for the backplane driver (pin 8) of nominal 60 Hz for an external capacitor of 22 nF.

The backplane driver is able to drive a 40 bits display.

The bit length of the shift register is programmed with BLS (Bit Length Selector) (pin 7). If BLS is kept LOW the DATA bit length is 20; for BLS open or HIGH a DATA bit length of 17 is selected.

DEVELOPMENT SAMPLE DATA

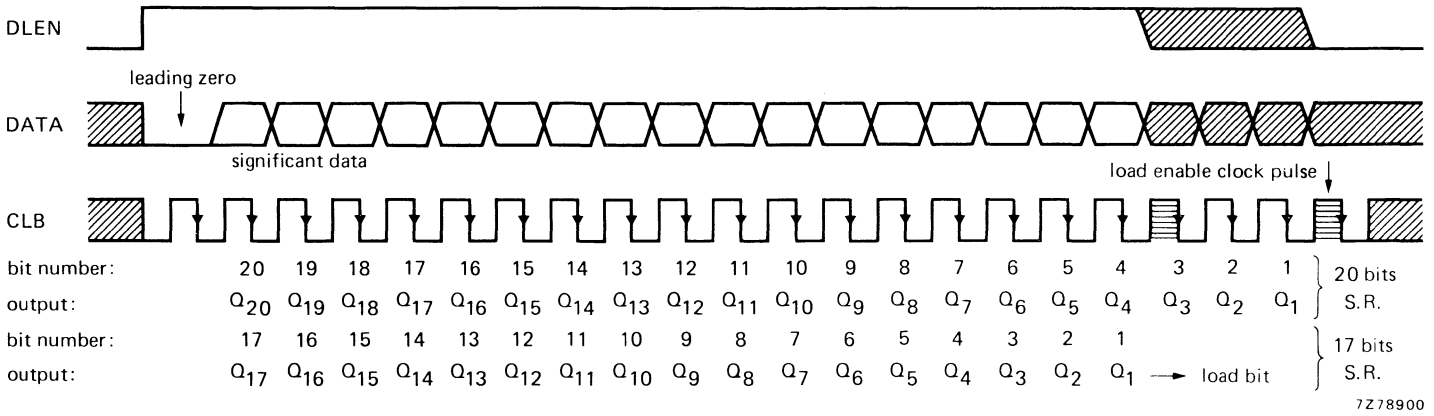


Fig. 3 Organization of 18 and 21 bit words; DATA = LOW means segment 'on'.

RATINGS (V_{EE} = 0)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	6 V
Total power dissipation at T_{amb} = 100 °C derate linearly with 0,02 W/°C	P_{tot}	max.	500 mW
Operating ambient temperature range	T_{amb}		−25 to + 125 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

CHARACTERISTICS

V_{EE} = 0; V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		condition
Supply voltage	V_{CC}	4,2	5	5,5	V	
Supply current	I_{CC}	–	3,5	–	mA	
Inputs CLB, DLEN, DATA, BLS						
input voltage HIGH	V_{IH}	1,6	–	V_{CC}	V	
input voltage LOW	V_{IL}	−1	–	+ 0,8	V	
maximum input frequency	f_I	–	50	–	kHz	
Input C_{ext}						
input voltage HIGH	V_{IH}	4,6	–	–	V	static mode
input voltage LOW	V_{IL}	−0,1	–	0,4	V	sync. slave mode
input current HIGH	I_{IH}	–	–	180	μA	
input current LOW	I_{IL}	–	–	−40	μA	
Input AC/EL (in slave mode)						
input voltage HIGH	V_{IH}	2,7	–	V_{CC}	V	
input voltage LOW	V_{IL}	−0,4	–	2,3	V	
Output C_{ext} (oscillator mode)						
oscillator frequency	f_{osc}	120	240	360	Hz	C = 22 nF
Output stage backplane (AC/EL)						
output current sink/source	I_O	2,4	–	–	mA	
Output Q_1 to Q_{20}						
output current sink/source	I_O	60	–	–	μA	
d.c. rest voltage between pin 8 (AC/EL) and one of the segment drivers (see Fig. 4)						
segment 'on' situation		–	–	25	mV	
segment 'off' situation		–	–	25	mV	

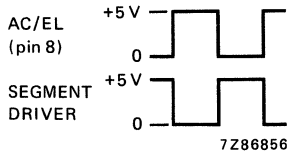


Fig. 4 AC/EL and segment driver pulses.
The d.c. voltage for segment 'on' is about 5 V.

Fluorescent Display/Interface Circuit SAA1063

GENERAL DESCRIPTION

The SAA1063 is designed to drive the display unit of a digital tuning system. It contains a 17-bit shift register, latches, display multiplexers and output stages, capable of driving 4½ decades of a 7 segment fluorescent display in duplex mode. The decoding for the display is carried out in the data input (microcomputer).

Features

- Driving 4½ decades of a seven segment display in duplex mode.
- Microcomputer compatible.
- 17-bit shift register.
- D.C. and duplex operation.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4 to 5,5	V
Operating ambient temperature range	T_{amb}		−20 to +80	°C
Maximum input frequency	f_i	min.	50	kHz
Supply current	I_{CC}	typ.	20	mA
Output current	I_Q	max.	1,5	mA
Maximum output voltage swing	V_{Qmax}	min.	34,5	V

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)

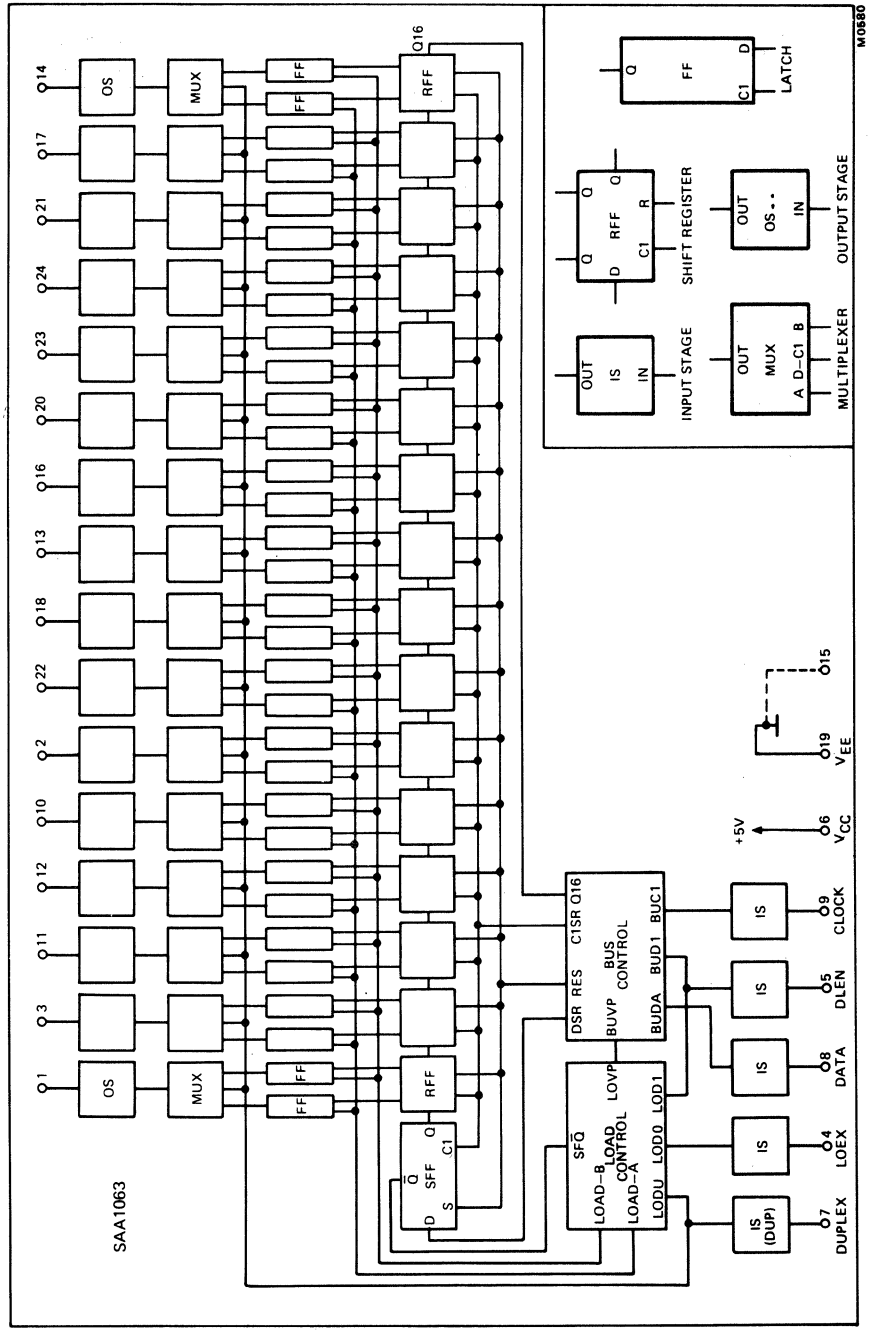


Fig. 1 Block diagram.
Insert indicates structure of logic elements.

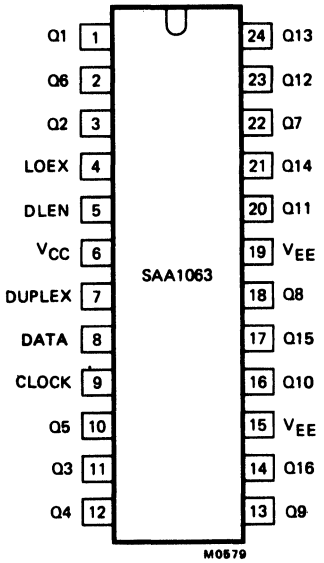


Fig. 2 Pinning diagram.

PINNING

1.	Q1		13.	Q9	segment drive outputs
2.	Q6	segment drive outputs	14.	Q16	
3.	Q2		15.	V_{EE}	ground
4.	LOEX	mode selection	16.	Q10	
5.	DLEN	bus enable	17.	Q15	segment drive outputs
6.	V_{CC}	+5 V power supply	18.	Q8	
7.	DUPLEX	duplex input	19.	V_{EE}	ground
8.	DATA	data input	20.	Q11	
9.	CLOCK	bus clock input	21.	Q14	
10.	Q5		22.	Q7	segment drive outputs
11.	Q3	segment drive outputs	23.	Q12	
12.	Q4		24.	Q13	

OPERATION DESCRIPTION

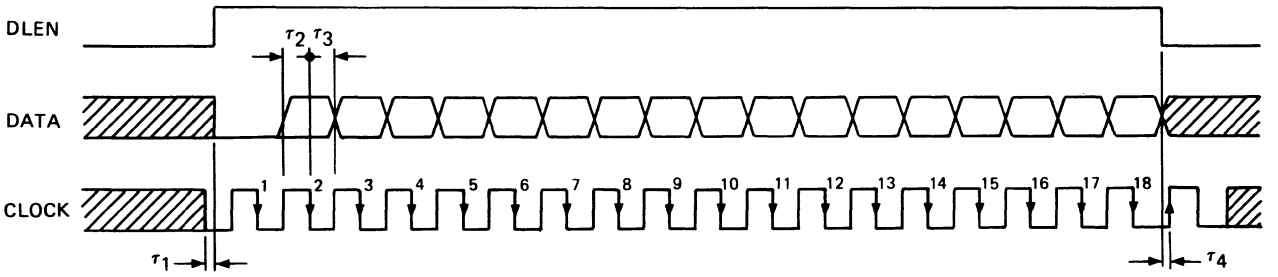
The input information for this device consists of a data bus with 17 bit words, an external clock synchronized with the data bus and an enable signal. The data format of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is taken as to whether these signals are valid for this device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal HIGH, during the first HIGH period of the clock signal. During the HIGH period of the DLEN signal, the length control determines if the clock signal consists of 18 pulses. This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device accepting interference on the signal lines. If leading zero is detected the shift register is reset and then the data is written into this register. The reset position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input is correct. Incorrect length of the information is detected by checking the value of the last bit of the register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOVP). This pulse enables the load control circuit to load the contents of the register into one of the two latches. When the load bit of the data word is HIGH the register contents are loaded into latch A; when this load bit is LOW the register contents are loaded into latch B. When the data information is accepted this load bit is written into the first bit of the shift register.

In duplex mode the load pulse is synchronised by the duplex signal, to avoid current transients in the output stages during the loading of the latches. The duplex mode operates in one of two mode conditions. When LOEX (pin 4) is LOW the duplex mode condition is selected; when LOEX is HIGH the d.c. mode condition is selected. The output stages are switched to the contents of latch A and latch B respectively.

When the duplex input (pin 7) is LOW the contents of latch A can be found on the output, when this input is HIGH the contents of latch B are found on the output.

In the duplex mode condition the output stages are capable of driving 32 duplexed segments of a fluorescent display. However, in the d.c. mode condition the output stages can only drive 16 segments of the display and two SAA1063 devices are required to drive a 4½ decade display unit.



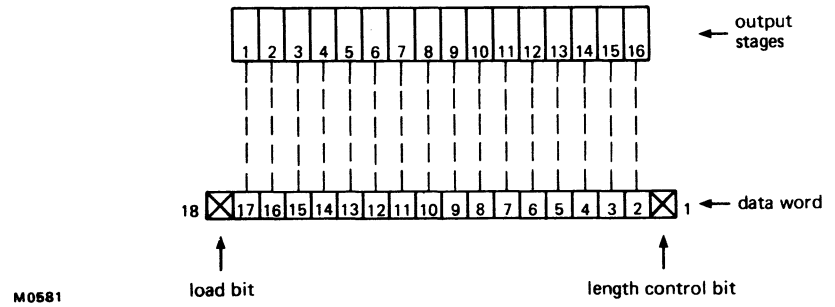


Fig. 3 Organisation of 18-bit data word.

Notes

1. The display segment is blanked by a HIGH data bit.
2. In duplex mode the period between the two data words must be greater than 21 ms.
3. Shaded timing periods are 'don't care' levels.
4. $\tau_1 > 4\ \mu s$ if a continuous clock is used. τ_2 and $\tau_3 > 4\ \mu s$. $\tau_4 > 2\ \mu s$.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	6	V
Total power dissipation at T_{amb} = 80 °C	P_{tot}	max.	900	mW
Operating ambient temperature range	T_{amb}		−20 to +80	°C
Storage temperature range	T_{stg}		−55 to +125	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.		conditions
Supply voltage	V_{CC}	4	5	5,5	V	
Supply current	I_{CC}	–	20	–	mA	
Inputs LOEX, DLEN, DATA, CLOCK						
input voltage HIGH	V_{IH}	2	–	5	V	
input voltage LOW	V_{IL}	0	–	0,8	V	
input current	$-I_{IH}$	–	–	20	μA	(V_I = 0 V)
max. input frequency	f_i	50	–	–	kHz	
DUPLEX						
input voltage HIGH	V_{IH}	0,8	–	20	V	
input voltage LOW	V_{IL}	−6	–	0,4	V	
input current HIGH	I_{IH}	0,01	–	12	mA	
input frequency	f_i	–	50	–	Hz	
Outputs Q1 to Q16						
output voltage HIGH	$-V_{OH}$	30	–	–	V	I_O < 0,7 μA
output voltage LOW	V_{OL}	4,5	–	–	V	I_O = 1 mA
output current	I_{OL}	–	–	1,5	mA	

LVDT Signal Conditioner

SE/NE5521

DESCRIPTION

The SE/NE5521 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDT's) and Rotary Variable Differential Transformers (RVDT's). The chip includes a low distortion, amplitude stable sine wave oscillator with programmable frequency to drive the primary of the LVDT/RVDT, a synchronous demodulator to convert the LVDT/RVDT output amplitude and phase to position information, and an output amplifier to provide amplification and filtering of the demodulated signal.

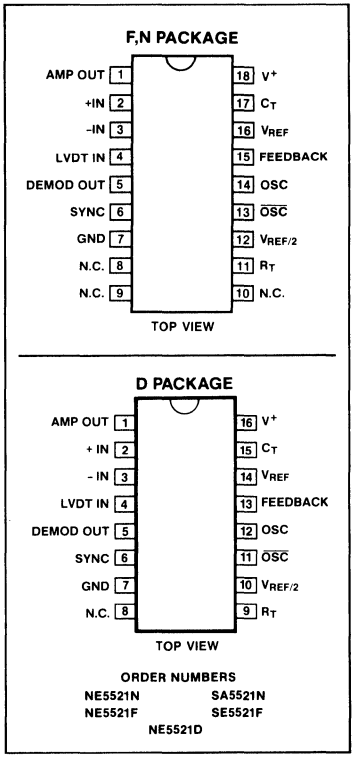
FEATURES

- **Low distortion**
- **Single supply 5V to 20V, or dual supply ±2.5V to ±10V**
- **Oscillator frequency 1kHz to 20kHz**
- **Capable of ratiometric operation**
- **Low power consumption (182mW typ)**

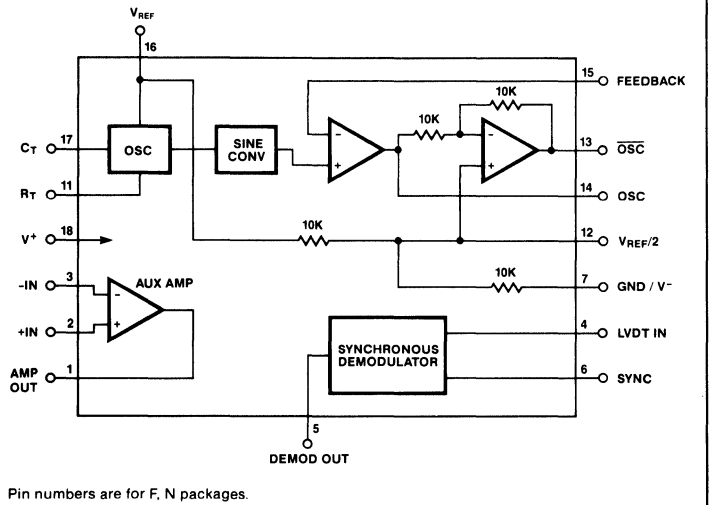
APPLICATIONS

- **LVDT signal conditioning**
- **RVDT signal conditioning**
- **LPDT signal conditioning**
- **Bridge circuits**

PIN CONFIGURATION



BLOCK DIAGRAM



Pin numbers are for F, N packages.

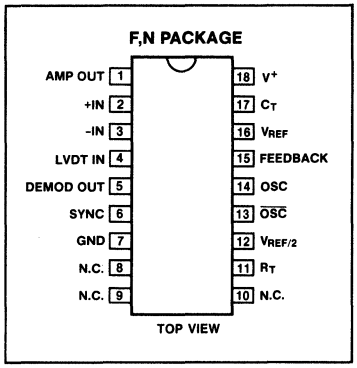
4

LVDT SIGNAL CONDITIONER — SE/NE5521

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+20	V
Split supply voltage	±10	V
Operating temperature range		
NE5521	0 TO +70	°C
SA5521	-40 TO +85	°C
SE5521	-55 TO +125	°C
Storage temperature range	-65 TO +150	°C
Power dissipation	840	mW

PIN CONFIGURATION



PIN DEFINITIONS

1	**Amp Out**	Auxiliary Amplifier Output.
2	**+IN**	Auxiliary Amplifier non-inverting input.
3	**-IN**	Auxiliary Amplifier inverting input.
4	**LVDT IN**	Input to Synchronous Demodulator from the LVDT/RVDT secondary.
5	**DEMOD OUT**	Pulsating DC output from the Synchronous Demodulator output. This voltage should be filtered before use.
6	**SYNC**	Synchronizing input for the Synchronous Demodulator. This input should be connected to the OSC or $\overline{OSC}$ output. Sync is referenced to $V_{REF}/2$.
7	**GND**	Device return. Should be connected to system ground or to the negative supply.
8	**NC**	No internal connection.
9	**NC**	No internal connection.
10	**NC**	No internal connection.
11	**R_T**	Oscillator frequency-determining resistor. A temperature stable 18K-ohm resistor should be connected between this pin and pin 7.
12	**$V_{REF}/2$**	A high impedance source of one half the potential applied to V_{REF} (pin 16). The LVDT/RVDT secondary return should be to this point. A bypass capacitor with low impedance at the oscillator frequency should also be connected between this pin and ground.
13	**$\overline{OSC}$**	Oscillator sinewave output that is 180° out of phase with the OSC signal at pin 14. The LVDT/RVDT primary is usually connected between OSC and $\overline{OSC}$ pins.
14	**OSC**	Oscillator sine wave output. The LVDT/RVDT primaries are usually connected between OSC and $\overline{OSC}$ pins.
15	**FEEDBACK**	Usually connected to the OSC (pin 14) output for unity gain. A resistor between this pin and OSC, and one between this pin and ground, can provide for a change in the oscillator output pin amplitudes.
16	**V_{REF}**	Reference voltage input for the oscillator and sine converter. This voltage MUST be stable and must never exceed V^+ supply voltage.
17	**C_T**	Oscillator frequency-determining capacitor. The capacitor connected between this pin and ground should be a temperature-stable type.
18	**V^+**	Positive supply connection.

LVDT SIGNAL CONDITIONER — SE/NE5521

ELECTRICAL CHARACTERISTICS $V+ = V_{REF} = 10V$, $T_A = 0$ to 70°C for NE5521, $T_A = -55$ to +125°C for SE5521, $T_A = -40$ to +85°C for SA5521, Frequency = 1kHz, unless otherwise noted.

PARAMETER	CONDITIONS	NE5521			SA/SE5521			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply current			12.9	20		12.9	18	mA
Reference current			5.3	8		5.3	8	mA
Reference voltage range		5		V^+	5		V^+	V
Power dissipation			182	280		182	260	mW
Oscillator Section								
Oscillator Output	R_L = 10K		$\frac{V_{REF}}{8.8}$			$\frac{V_{REF}}{8.8}$		V_{rms}
Sine wave distortion	No Load		1.5			1.5		%
Initial amplitude error	T_A = 25°C		0.4	±3		0.4	±3	%
Tempco of amplitude			0.005	0.01		0.005	0.01	% / °C
Init. accuracy of oscillator freq.	T_A = 25°C		±0.9	±5		±0.9	±5	%
Temperature coeff. of frequency[1]			0.05			0.05		% / °C
Voltage coeff. of frequency			2.5			3.3		% / $V(V_{REF})$
Min OSC to ($\overline{OSC}$) Load[2]		300	170		300	170		Ω
Demodulator Section								
Linearity error	5 V_{p-p} input		±0.05	±0.1		±0.05	±0.1	% FS
Maximum demodulator input			$\frac{V_{REF}}{2}$			$\frac{V_{REF}}{2}$		V_{p-p}
Demodulator offset voltage			±1.4	±5		±1.4	±5	mV
Demodulator offset voltage drift			5	25		5	25	μV / °C
Demodulator input current		-600	-234		-500	-234		nA
$V_R/2$ accuracy			±0.1	±1		±0.1	±1	%
Auxiliary Output Amplifier								
Input offset voltage			±0.5	±5		±0.5	±5	mV
Input offset drift			±2	±25		±2	±25	μV / °C
Input bias current		-600	-210		-500	-210		nA
Input offset current			9	50		9	50	nA
Gain		100	385		100	385		V/mV
Slew rate			1.3			1.3		V/μSec
Unity gain bandwidth product	A_V = 1		1.6			1.6		MHz
Output voltage swing	R_L = 10K	7	8.2		7	8.2		V
Output short circuit current to ground or to V_{cc}	T_A = 25°C		42	100		42	100	mA

NOTES
1. This is temperature coefficient of frequency for the device only. It is assumed that C_T and R_T are fixed in value and C_T leakage is fixed over the operating temperature range.
2. Minimum load impedance for which distortion is guaranteed to be less than 5%.

EXPLANATION OF TERMS

Oscillator Output	rms value of the AC voltage available at the oscillator output pin. This output is referenced to $V_{REF}/2$ and is a function of V_{REF}.
Sine Wave Distortion	The Total Harmonic Distortion (THD) of the oscillator output with no load. This is not a critical specification in LVDT/RVDT system. This figure could be 15% or more without affecting system performance.
Initial Amplitude Error	A measure of the interchangeability of SE/NE5521 parts, NOT a characteristic of any one part. It is the degree to which the oscillator output of a number of SE/NE5521 samples will vary from the median of that sample.
Initial Accuracy of Oscillator Frequency	Another measure of the interchangeability of individual SE/NE5521 parts. This is the degree to which the oscillator frequency of a number of SE/NE5521 samples will vary from the median of that sample with a given timing capacitor.
Tempco of Oscillator Amplitude	A measure of how the oscillator amplitude varies with ambient temperature as that temperature deviates from a 25°C ambient.
Tempco of Oscillator Frequency	A measure of how the oscillator frequency varies with ambient temperature as that temperature deviates from a 25°C ambient.
Voltage Coeffecient of Oscillator Frequency	The degree to which the oscillator frequency will vary as the reference voltage (V_{REF}) deviates from +10 volts.
Linearity Error	The degree to which the DC output of the demodulator/amplifier combination matches a change in the AC signal at the demodulator input. It is measured as the worst case nonlinearity from a straight line drawn between positive and negative full scale end points.
Maximum Demodulator Input	The maximum signal that can be applied to the demodulator input without exceeding the specified linearity error.

APPLICATION INFORMATION

$$\text{OSC frequency} = \frac{V_{REF} - 1.3V}{V_{REF}(R_T + 1.5K)C_T}$$

Symbols and Definitions

Acquisition Time

The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time

The time elapsed from the hold command to the opening of the switch.

Aperture Jitter

Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture Time

The delay required between "hold" command and an input analog transition, so that the transition does not affect the hold output.

Dynamic Sampling Error

The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Effective Aperture Delay

The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure Of Merit

The ratio of the available charging current during sample mode to the leakage current during hold mode.

Gain Error

The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold-Mode Droop

The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold-Mode Feed Through

This percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold Settling Time

The time required for the output to settle within 1mV of final value after the "hold" logic command.

Hold Step

The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Sample-To-Hold Offset Error

The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate

The fastest rate at which the sample & hold output can change (specified in V/μs).

Threshold

Level shall be defined as that level which causes the switch control to change state.

High Performance Sample-and-Hold Amplifier — TDA1535

DESCRIPTION

The TDA1535 is a monolithic high speed, high performance, sample-and-hold amplifier consisting of a high speed operational amplifier with two switchable JFET inputs and a wide band switchable class B output stage. The high accuracy makes this device suitable for data acquisition systems with resolution up to 16 bits.

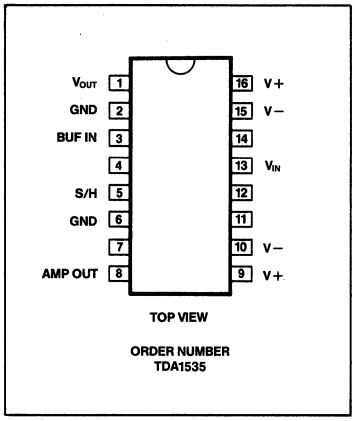
FEATURES

- **Low distortion (0.001%)**
- **High signal-to-noise ratio (110 dB)**
- **Low droop rate (5 V/sec)**
- **TTL compatible control input**

APPLICATIONS

- **Digital signal processing**
- **Digital audio**
- **Data acquisition**
- **Telemetry**

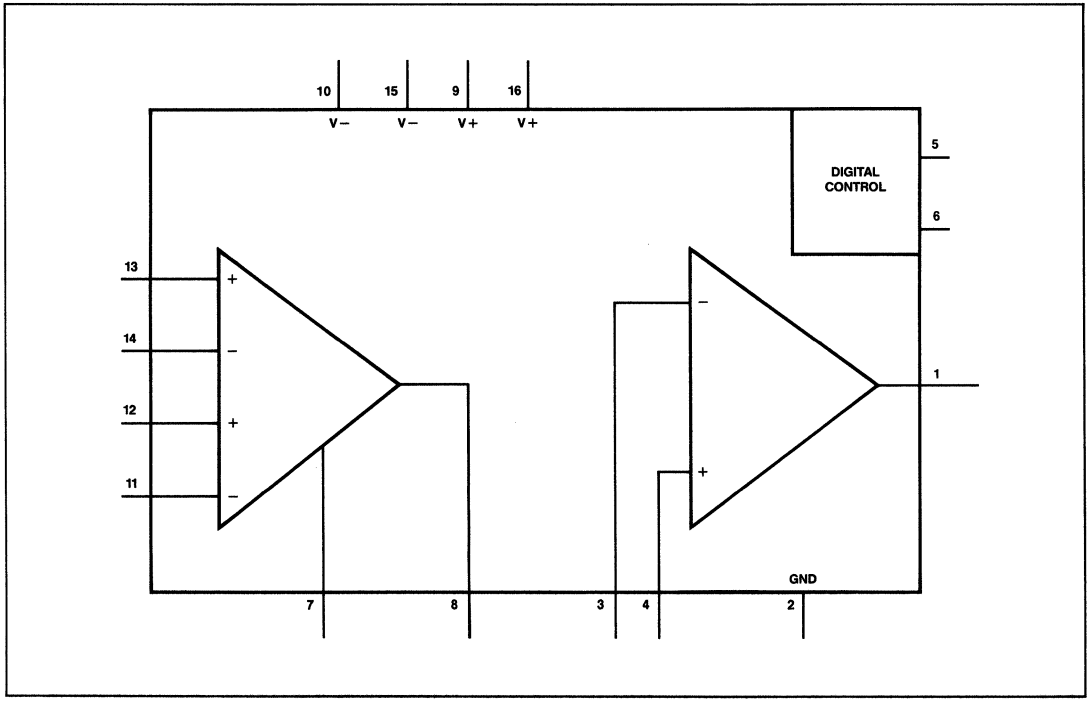
PIN CONFIGURATION



REFERENCE DATA

PARAMETER	LIMIT	UNITS
Positive supply (pins 9, 16)	5	V
Negative supply (pins 10, 15)	−5	V
Negative supply 2 (pin 9)	−17	V
Signal-to-noise ratio	110	dB
Distortion	0.001	%

BLOCK DIAGRAM



For additional information, consult the Applications Section.

Signetics

Communications
Section 5

Linear Products

Double Balanced Mixer and Oscillator SA/NE602

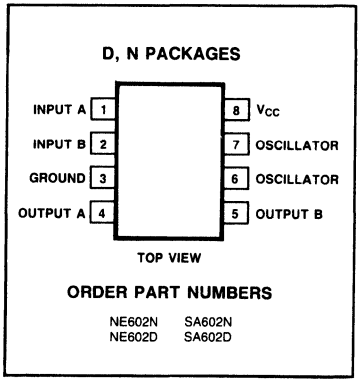
DESCRIPTION

The SA/NE602 is a monolithic Double Balanced Mixer with on-board oscillator and voltage regulator. The oscillator can be used as a buffer for external injection. The design is optimized for frequency conversion applications up to 200MHz and has excellent noise and 3rd order intermodulation performance. The SA/NE602 is available in a 8 lead dual in line plastic package and 8 lead SO (Surface mounted miniature package).

APPLICATIONS

- **HF and VHF frequency conversion**
- **Cellular radio mixer/oscillator**
- **Communication receivers**
- **Instrumentation frequency converters**
- **VHF walkie talkie**

PIN CONFIGURATION



FEATURES

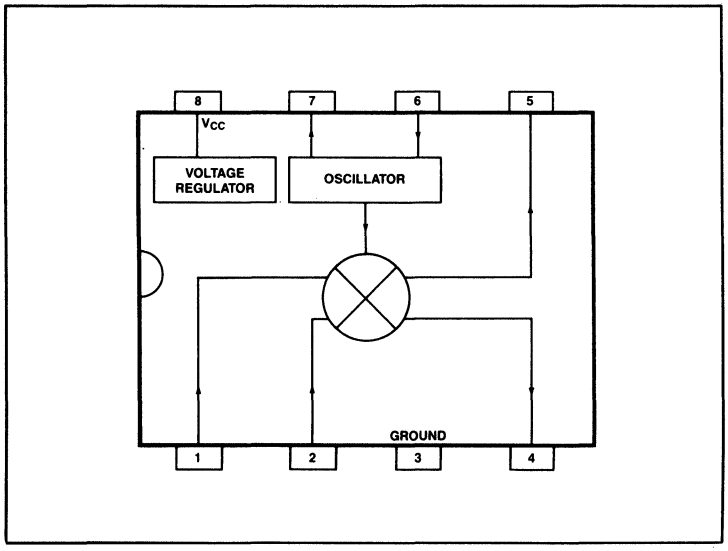
- **Low current consumption: 2.4mA typical**
- **High input and oscillator frequency operation up to 200MHz**
- **High third order intercept point: −15 dBm referred to matched input**
- **Excellent noise figure: 5.0dB typical at 45 MHz**
- **Low external count; suitable for crystal/ceramic filters**

5

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	−65 to +150	°C
Operating temperature		
NE602	0 to +70	°C
SA602	−40 to +85	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS: T_A = 25°C, V_{CC} = 6V.

SYMBOL AND PARAMETER	SA/NE602			UNIT
	Min	Typ	Max	
Power supply voltage range	4.5	—	8.0	V
D.C. current drain	—	2.4	2.7	mA
Input signal frequency	—	—	200	MHz
Oscillator frequency	—	—	200	MHz
Noise figure @ 45MHz	—	5.0	6	dB
Third order intercept point	—	−15	−17	dBm
Mixer input resistance	1.5	—	—	kΩ
Mixer input capacitance	—	3	3.5	pF
Mixer output resistance[1]	—	2 x 1.5	—	kΩ

NOTE:
1. Each output pin is internally connected to V_{CC} through a 1.5 (nominal) kΩ resistor.

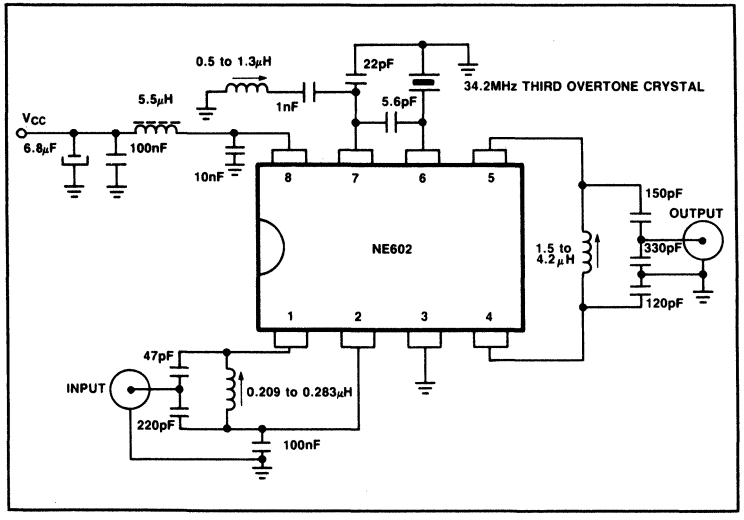
CIRCUIT DESCRIPTION

The NE602 utilizes an active double balanced mixer. The RF input port (pins 1 and 2) can be used in either a symmetrical or an asymmetrical configuration. The RF input port has a resistance of 1.5KΩ shunted by 3.0pF. In order to be used as an asymmetrical configuration, one of the two input pins (1 or 2) must be bypassed to ground with a capacitor. The RF input port does not need any external bias and should not be DC grounded. An external DC path between pins 1 and 2 is allowed.

The local oscillator is an emmitter-follower circuit and is capable of many types of oscillator configurations. Pin 6 (oscillator base) and pin 7 (oscillator emitter) do not need any external bias circuitry, but only pin 6 may have a DC path to V_{CC}. Pin 6 can be used for external oscillator or for frequency synthesizer injection.

The NE602 output pins can be used in a single-ended or push-pull configuration. There are internal 1.5KΩ resistors connected to V_{CC} for each output pin (4 and 5); therefore no external bias is needed. Pins 4 and/or 5 may have a DC path to V_{CC}.

TYPICAL APPLICATION



Low Power FM I.F. System — SA/NE604

DESCRIPTION

The SA/NE604 is a monolithic low power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The SA/NE604 is available in a 16 lead dual-in-line plastic package and 16 lead SO (surface mounted miniature package).

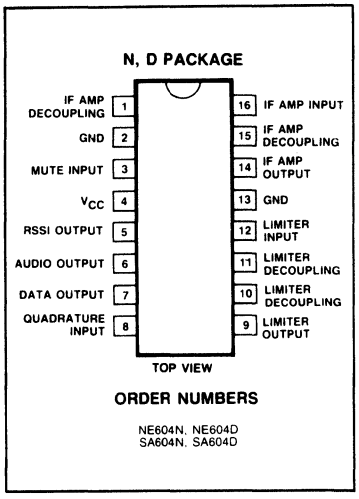
FEATURES

- **Low power consumption: 2.3mA typical**
- **Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.27 μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz**

APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 10.7MHz**
- **RF level meter**
- **Spectrum analyzer**

PIN CONFIGURATION



ORDER NUMBERS

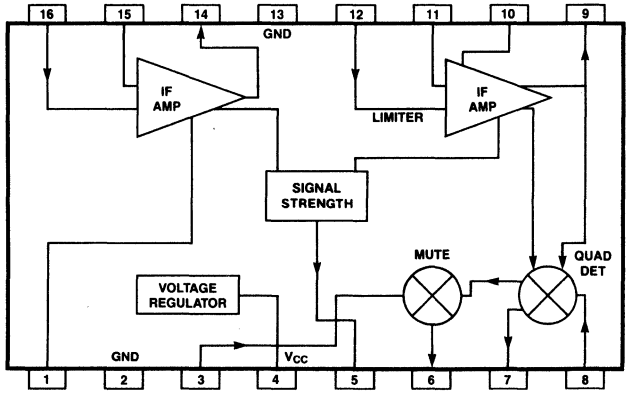
NE604N, NE604D
SA604N, SA604D

5

ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	−65 to +150	°C
Operating temperature		
NE604	0 to +70	°C
SA604	−40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +6$ volts, unless otherwise stated.

SYMBOL AND PARAMETER	SA/NE604			UNITS
	Min	Typ	Max	
Power supply voltage range	4.5	-	8.0	V
D.C. current drain	-	2.3	2.7	mA
I.F. frequency	-	-	10.7	MHz
RSSI range	TBD	90	-	dB
RSSI accuracy	-	±1.5	-	dB
I.F. input impedance	1.5	-	-	kΩ
I.F. output impedance	1.0	-	-	kΩ
Limiter input impedance	1.5	-	-	kΩ
Quadrature detector data output impedance	50	-	-	kΩ
Muted audio out impedance	-	50	-	kΩ
Mute - switch input threshold (on)	1.7	-	-	V
(off)	-	-	1.0	V

CIRCUIT DESCRIPTION

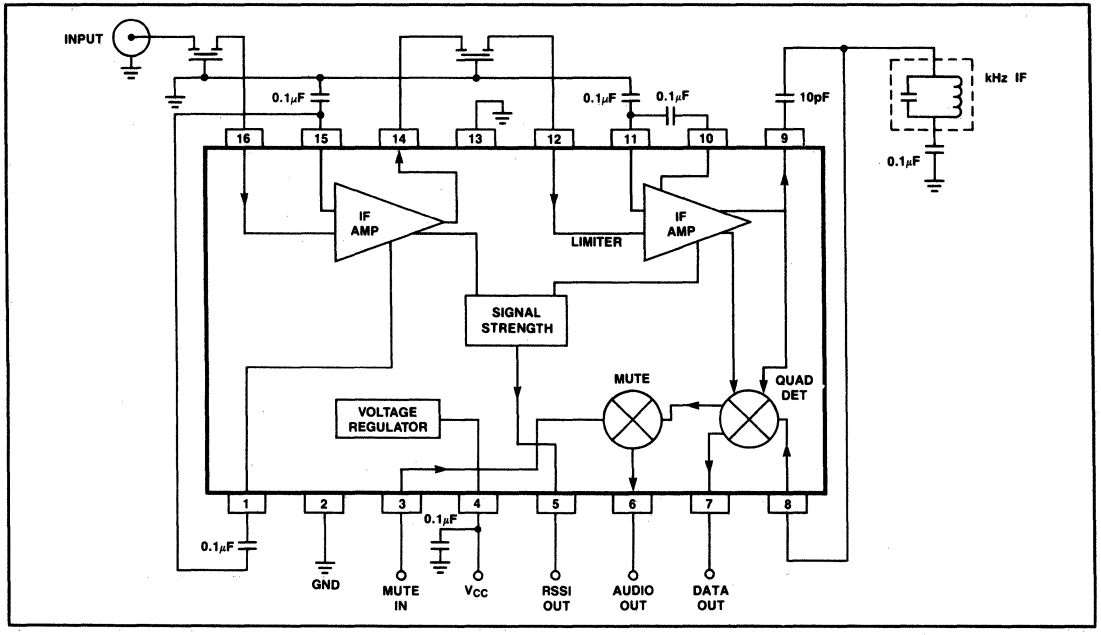
The SA/NE604's IF amplifier has a gain of 30dB, bandwidth of 15MHz, with an input impedance of 1.5KΩ and an output impedance of 1.0KΩ. The limiter has a gain of 60dB, bandwidth of 15MHz, and an input impedance of 1.5KΩ. An interstage filter between the IF Amplifier and Limiter is recommended to reduce wideband noise. The quadrature detector input (pin 8) impedance is 40KΩ.

The data (unmuted output) and audio (muted output) both have 50KΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

The logarithmic signal strength indicator is a current source output with maximum source current of 50 microamps. The signal strength indicator's transfer function is approximately 10 microamp per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

Pins 1, 16, 15, 14, 12, 11, 10, 9, and 8 do not need external bias and should not have a DC path.

TYPICAL APPLICATION



Low Voltage Dolby B/C Type IC — NE670

DESCRIPTION

The NE670 is a monolithic IC intended for use in low voltage Dolby* B & C type noise reduction applications. This IC design features both record and playback mode with all internal electronic switching.

FEATURES

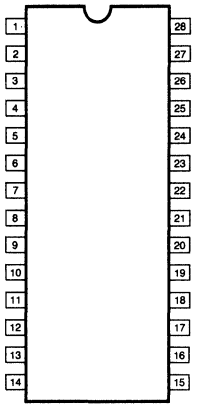
- **B and C type noise reduction**
- **Low voltage operation 1.8–8V**
- **Playback and record modes**
- **0dB (Dolby level) = 100mV**
- **Record input sensitivity 50mV**
- **Playback sensitivity 20mV**
- **All electronic switching**

APPLICATION

- **Portable tape recorders/players**

PIN CONFIGURATION

D PACKAGE



TOP VIEW
Order Numbers
NE670D

Pin	Function
1.	Test point
2.	Internal switch
3.	High-level stage side chain input
4.	High-level stage high pass
5.	High-level stage D-amp output
6.	High-level stage rectifier input
7.	High-level stage attack
8.	High-level stage decay
9.	Internal switch
10.	High-level stage output
11.	Low-level side chain input
12.	Low-level stage high pass
13.	Low-level stage D-amp output
14.	Low-level stage rectifier input
15.	Low-level stage attack
16.	Low-level stage decay
17.	Record output
18.	V_{CC}
19.	V_{REF}
20.	Anti-saturation network capacitor
21.	Mode switch
22.	Playback record switch
23.	Play input
24.	Ground
25.	Record input
26.	Compensation capacitor
27.	Line output
28.	Spectral skewing network

*Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.
Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California.

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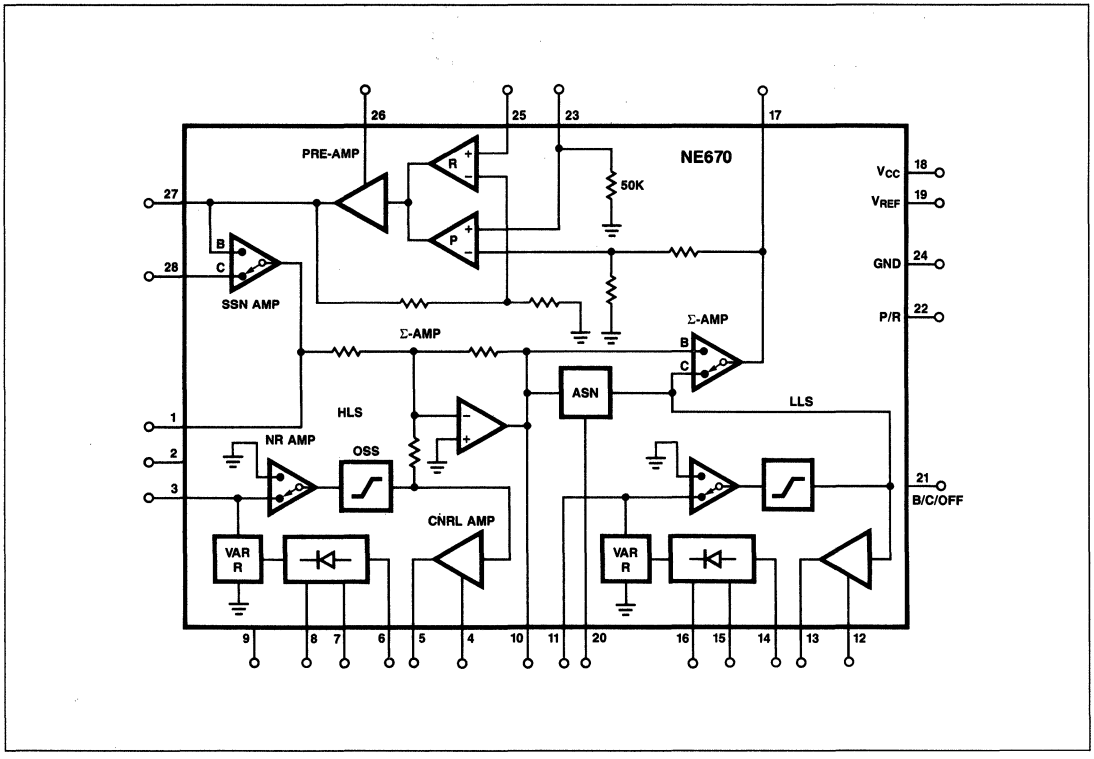
Low Voltage Dolby B/C Type IC NE670

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL & PARAMETER		RATING	UNIT
V_{CC}	Supply Voltage	8	V
	Temperature Range		
T_A	Operating	0 to +70	°C
T_{STG}	Storage	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

Standard Conditions: V_{CC} = 3V, T_A = 25°C.
All levels referenced to 0dB = 100mV at test point (TP).

SPECIFICATION	B/C	NR	MODE	CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Voltage range V_{CC}		Off	R		1.8	3	8	V
Min functional V_{CC}		Off	R	THD 1%		1.5		V
Distortion THD; 2nd and 3rd Harmonics	B	Off	R	0dB, f = 1kHz		0.02		%
	B	On	R			0.05	0.1	%
	C	On	R			0.1		%
Signal-to-Noise Ratio	B	Off	R	CCIR (DOLBY)		78		dB
		On	R	Rs = 10Kohms		74		dB
	C	On	R			66		dB
Supply current, I_{CC}	C	Off	R	0dB, f = 1kHz		7		mA
		On	R			9		mA
Signal handling	C	On	R	1% THD, V_{CC} = 1.8V	12			dB
	C	On	R	V_{CC} = 3V		14		dB
Input resistance				Pin 23	35	50	65	K
Frequency response (Referenced to test point)	B	On	R	f = 10kHz,0dB	−1.6	0.4	2.4	dB
	B	On	R	1kHz, −20dB	−17.8	−15.8	−13.8	dB
	B	On	R	5kHz, −30dB	−23.8	−21.8	−19.8	dB
	B	On	R	5kHz, −40dB	−31.7	−29.7	−27.7	dB
	C	On	R	10kHz, 0dB	−5.5	−3.5	−1.5	dB
	C	On	R	1kHz, −20dB	−16.1	−14.1	−12.1	dB
	C	On	R	5kHz, −40dB	−28.5	−26.5	−24.5	dB
	C	On	R	200Hz, −40B	−33.9	−31.9	−29.9	dB
Switching thresholds	B	Off			0	GND	0.1V_{CC}	V
						Open		V
	C				0.95V_{CC}	V_{CC}	V_{CC}	V
			P		0	GND	0.2	V
			R		0.7V_{CC}	V_{CC}	V_{CC}	V
Pre-Amp gain	B	Off	R			6		dB
			P			14		dB

NOTE:
R = record mode
P = play mode

Low Voltage Dolby B/C Type IC NE670

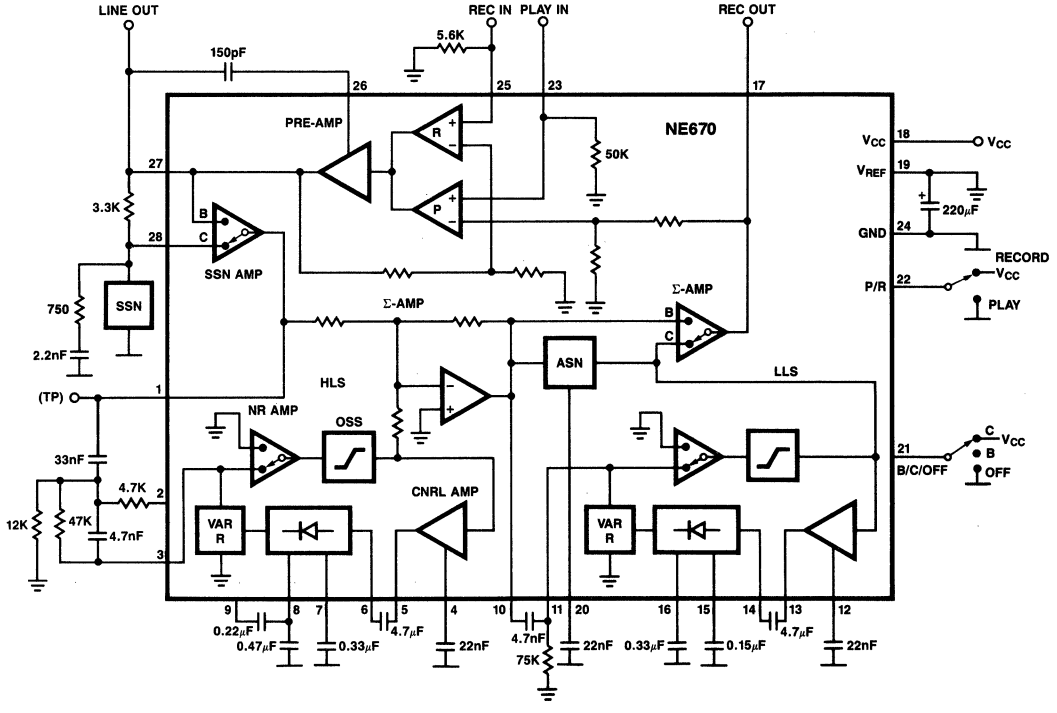


Figure 1. Test Circuit

Stereo Audio Switch | TDA1029

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

5

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

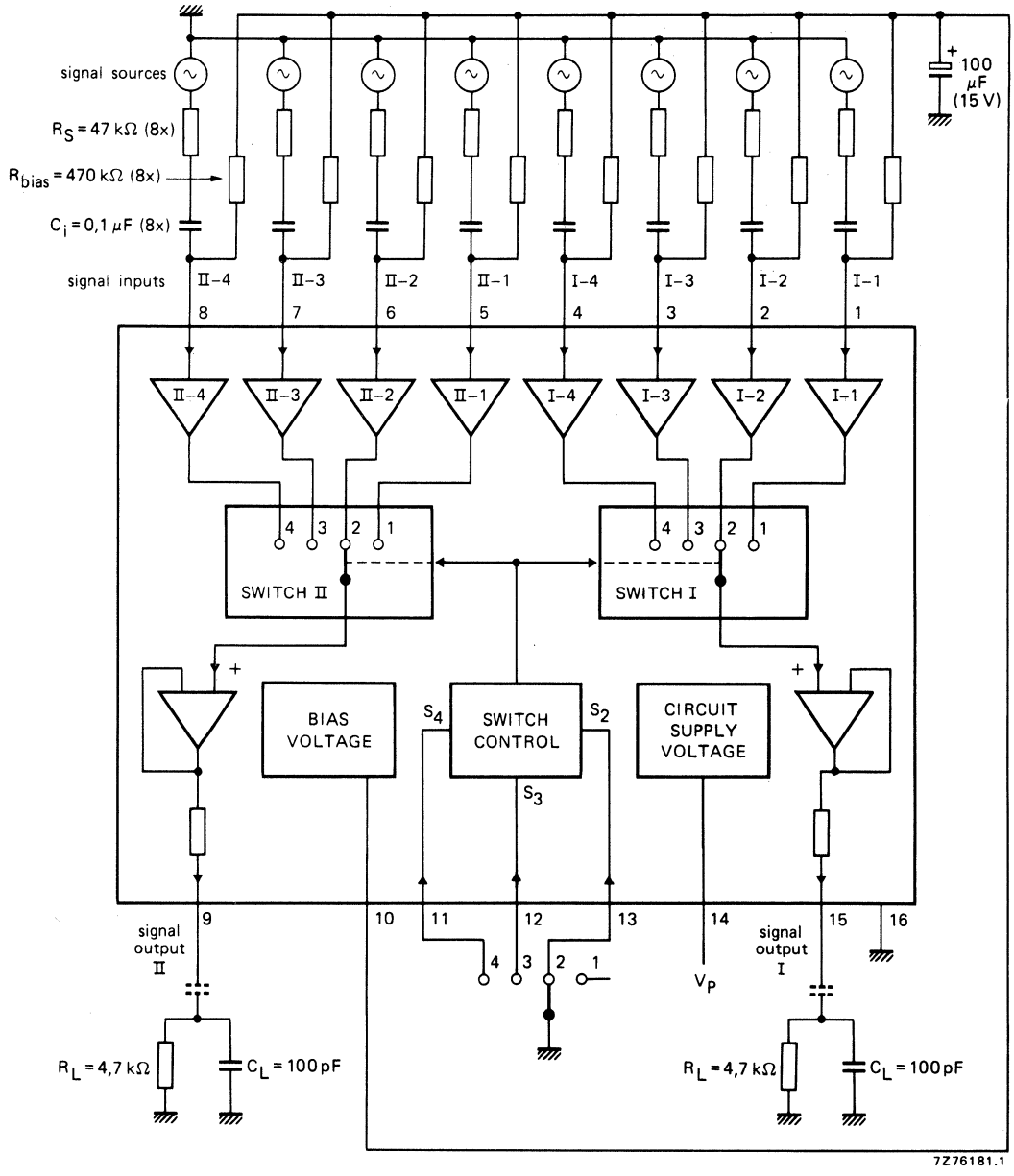


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

5

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption				
without load; $I_9 = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V
Signal inputs				
Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage R_S = 0; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at R_S = 1 kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_g = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_g; \pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{g-16}/\Delta t$; $\Delta V_{15-16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	V_{10-16}	typ.	11 V *
			10,2 to 11,8 V
Output resistance	R_{10-16}	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		V_{11-16}	V_{12-16}	V_{13-16}
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* V_{10-16} is typically $0{,}5 \cdot V_{14-16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5 dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 mV 100 mV
Total harmonic distortion			
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01 %
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02 %
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03 %
Output signal handling			
d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 V 5,3 V
Noise output voltage (unweighted)			
f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5 μV
Noise output voltage (weighted)			
f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12 μV
Amplitude response			
V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1 dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75 dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90 dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

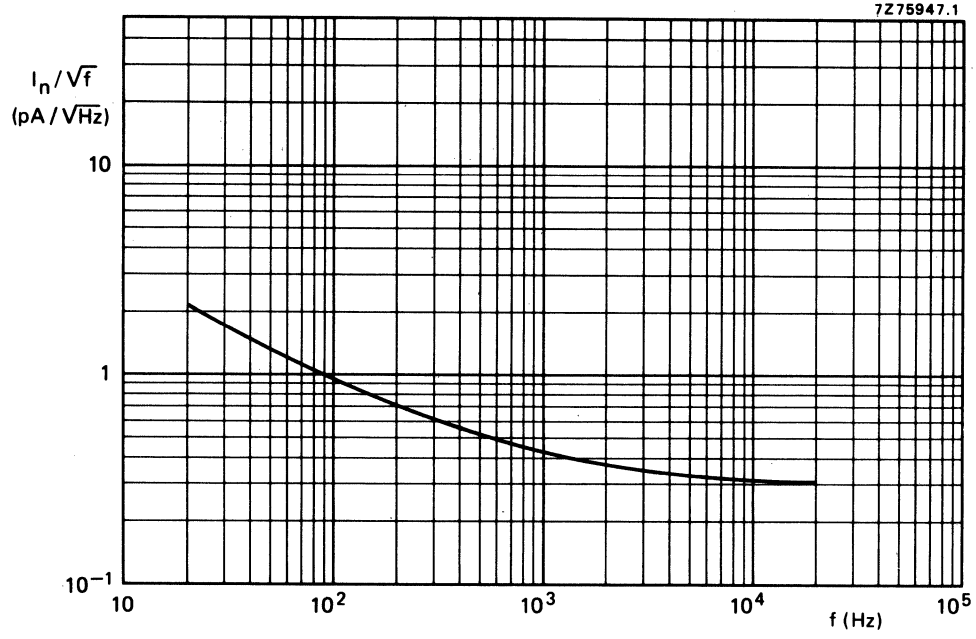


Fig. 2 Equivalent input noise current.

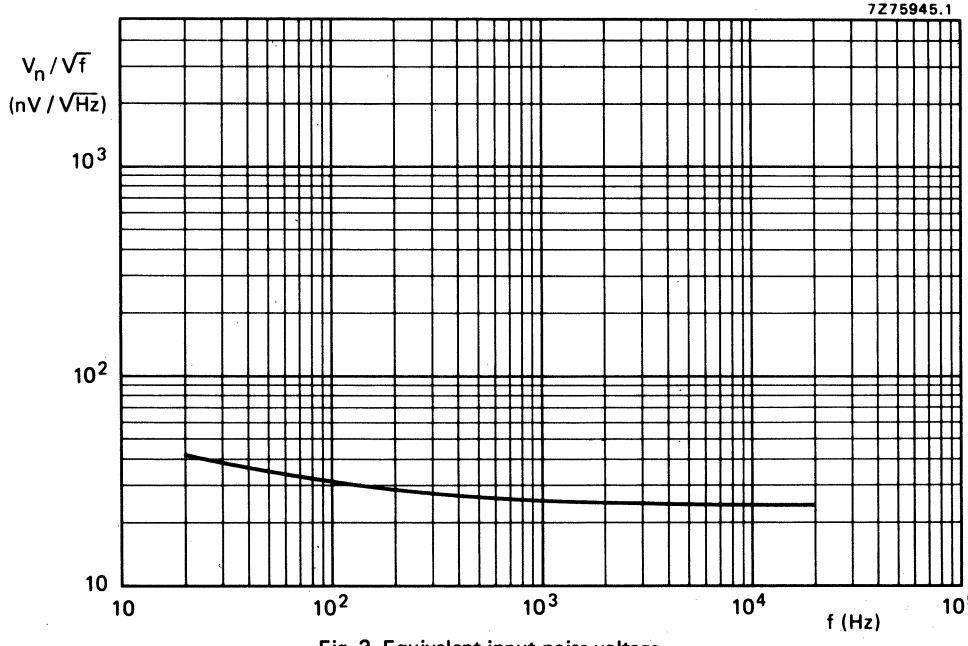


Fig. 3 Equivalent input noise voltage.

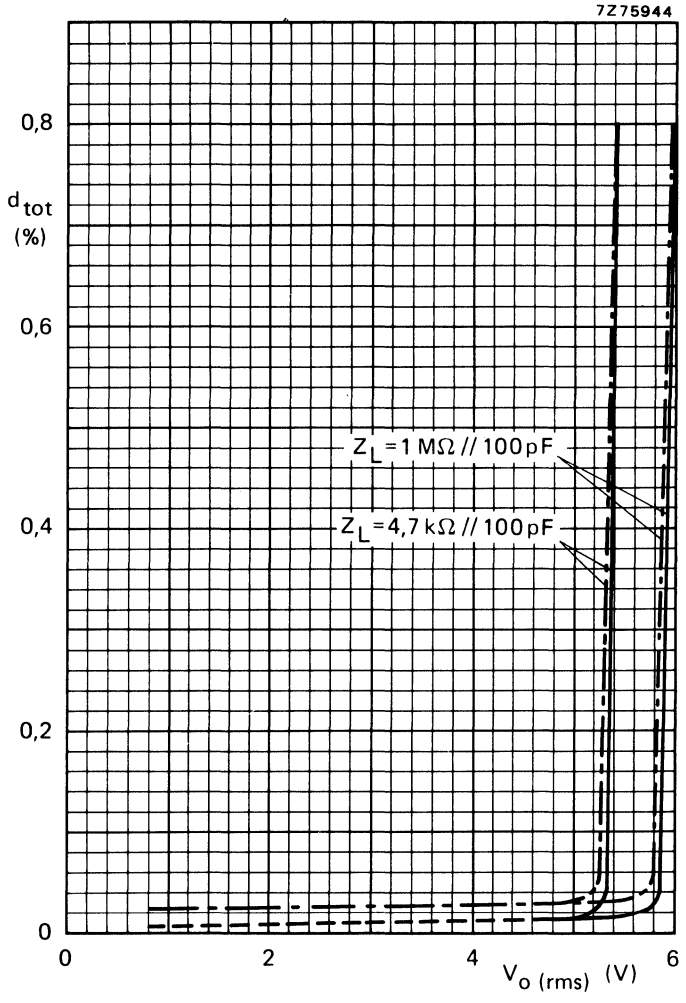


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — · — · f = 20 kHz.

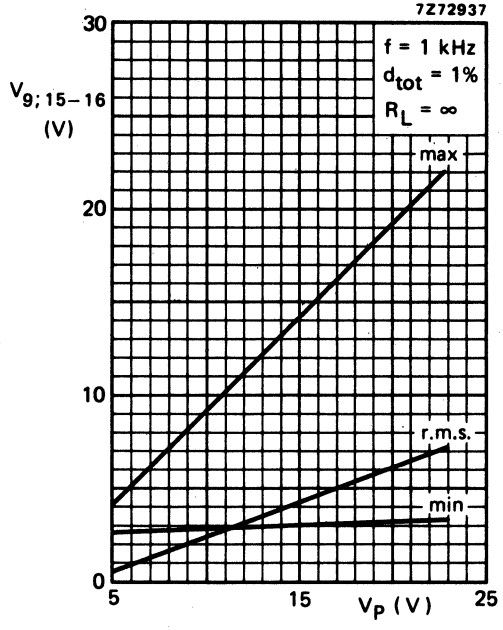


Fig. 5 Output voltage as a function of supply voltage.

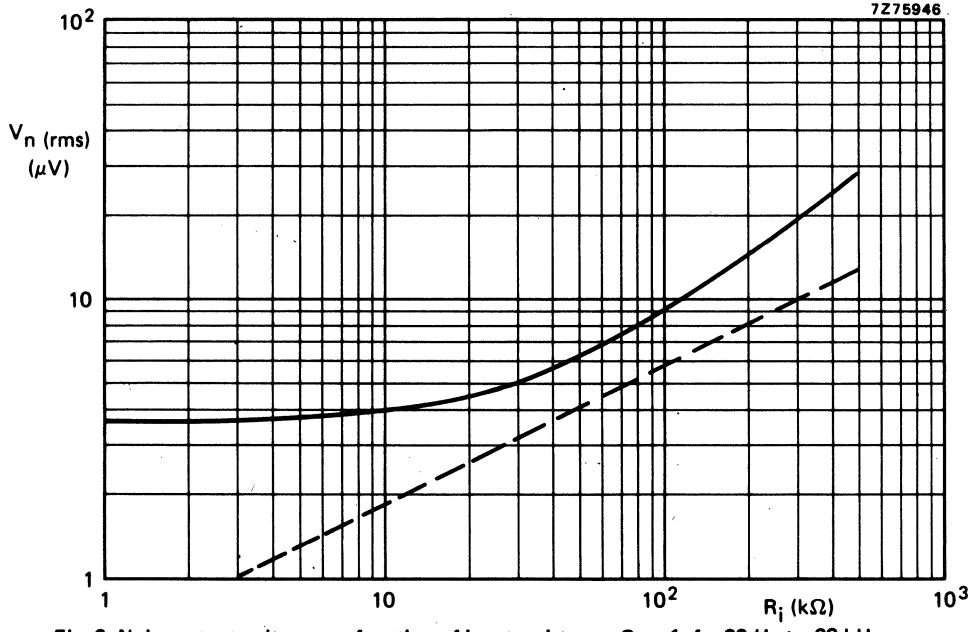


Fig. 6 Noise output voltage as a function of input resistance; G_v = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

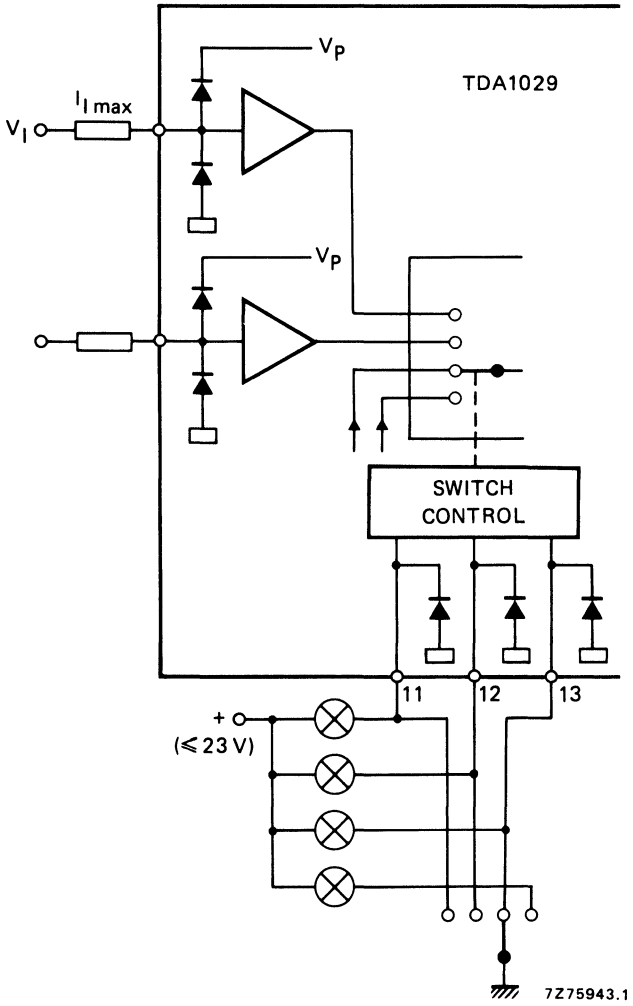


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

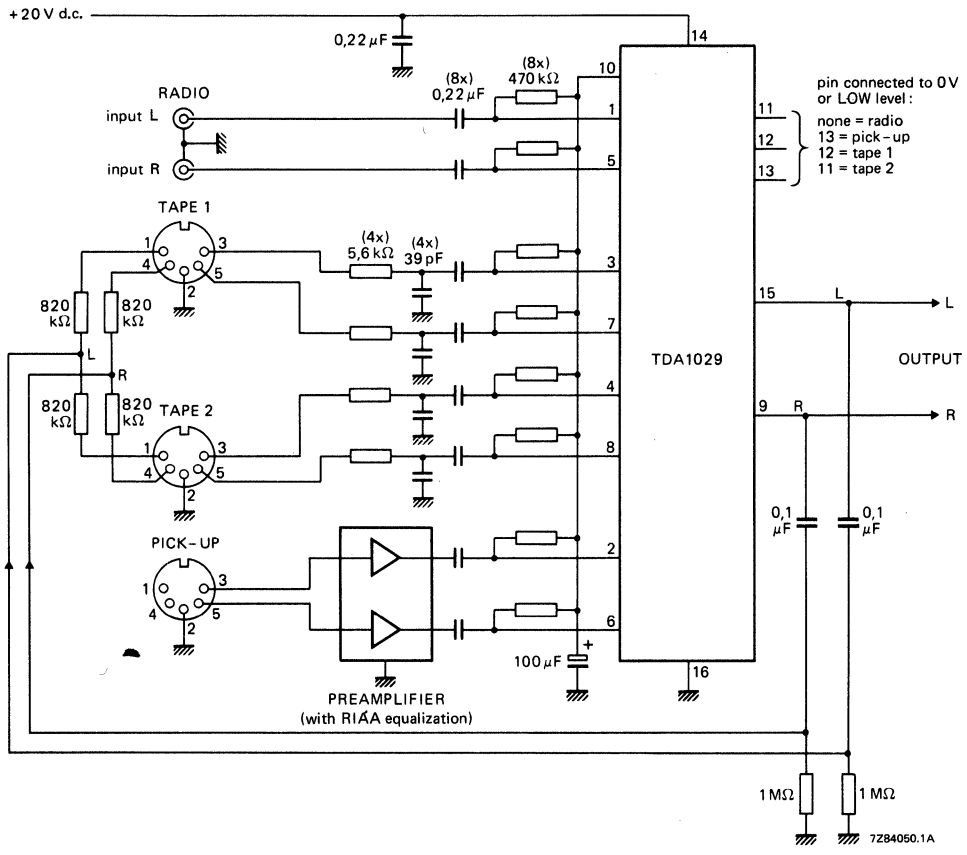


Fig. 8 TDA1029 connected as a four input stereo source selector.

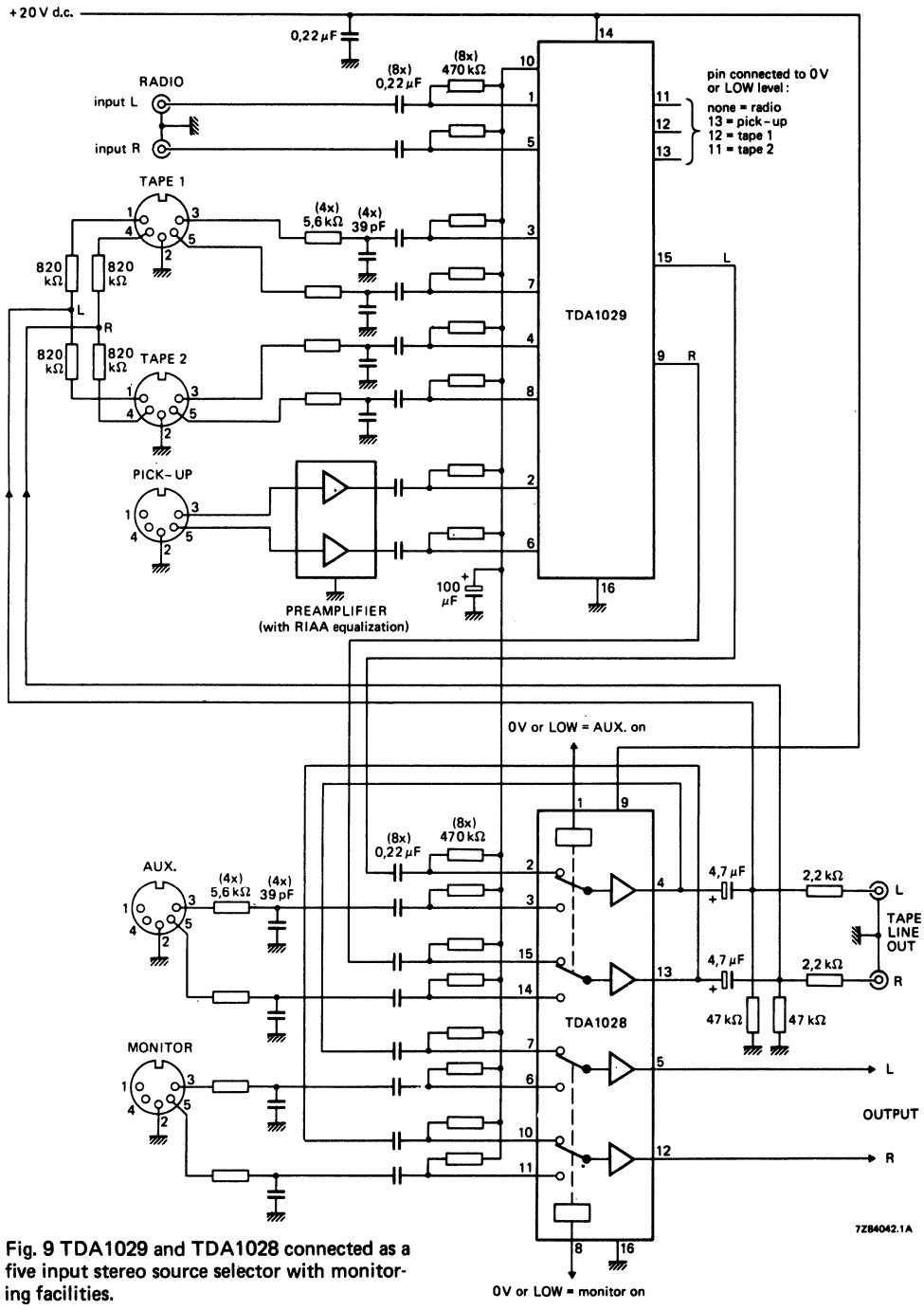


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

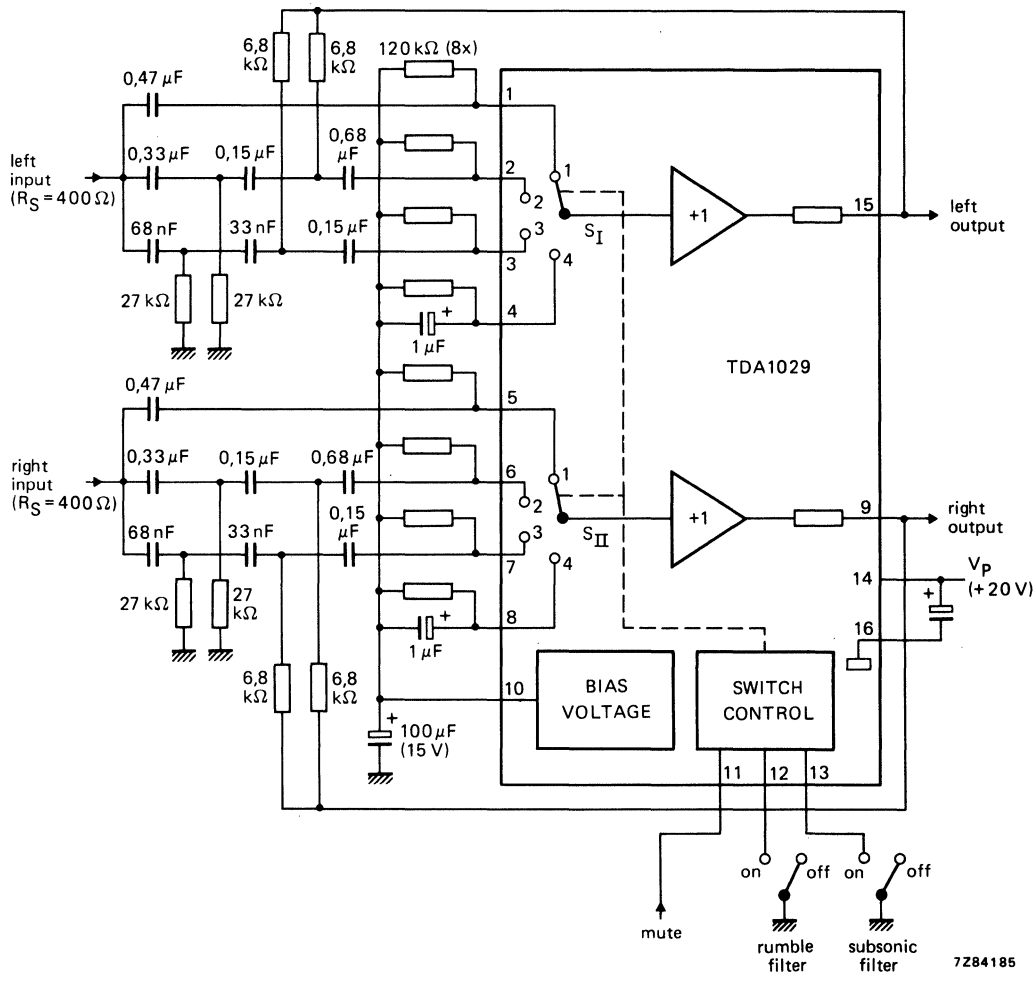


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

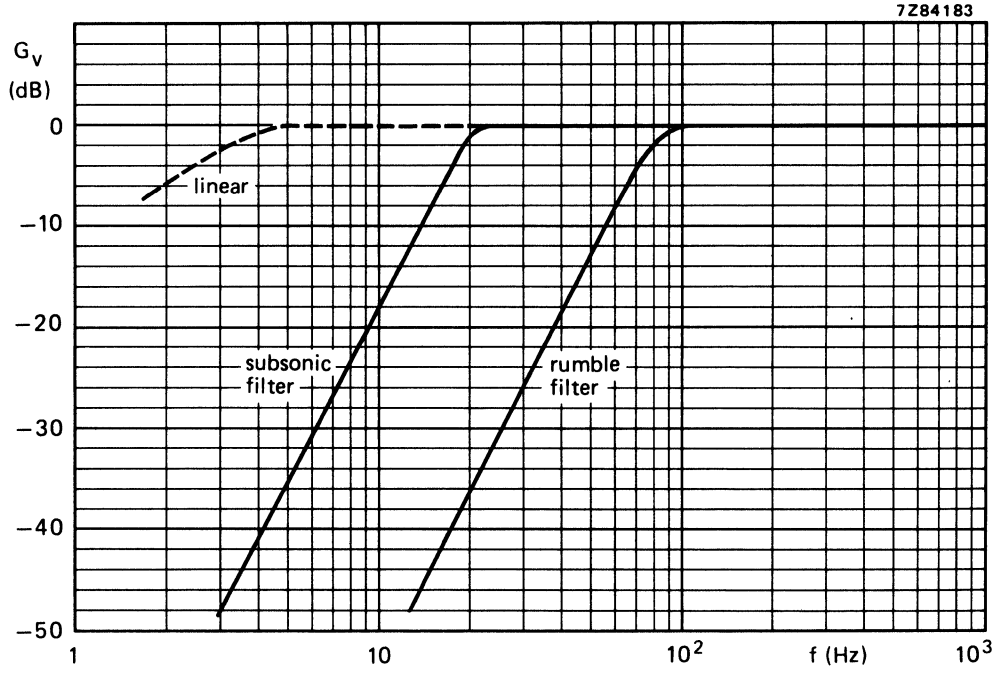


Fig. 11 Frequency response curves for the circuit of Fig. 10.

DC Controlled Dual Potentiometers — TDA1074A

GENERAL DESCRIPTION

The TDA1074A is a monolithic integrated circuit designed for use as volume and tone control circuit in stereo amplifiers. This dual tandem potentiometer IC consists of two ganged pairs of electronic potentiometers with the eight inputs connected via impedance converters, and the four outputs driving individual operational amplifiers. The setting of each electronic potentiometer pair is controlled by an individual d.c. control voltage. The potentiometers operate by current division between the arms of cross-coupled long-tailed pairs. The current division factor is determined by the level and polarity of the d.c. control voltage with respect to an externally available reference level of half the supply voltage. Since the electronic potentiometers are adjusted by a d.c. control voltage, each pair can be controlled by single linear potentiometers which can be located in any position dictated by the equipment styling. Since the input and feedback impedances around the operational amplifier gain blocks are external, the TDA1074A can performs bass/treble and volume/loudness control. It also can be used as a low-level fader to control the sound distribution between the front and rear loudspeakers in car radio installations.

Features

- High impedance inputs to both 'ends' of each electronic potentiometer
- Ganged potentiometers track within 0.5 dB
- Electronic rejection of supply ripple
- Internally generated reference level available externally so that the control voltage can be made to swing positively and negatively around a well-defined 0 V level
- The operational amplifiers have push-pull outputs for wide voltage swing and low current consumption
- The operational amplifier outputs are current limited to provide output short-circuit protection
- Although designed to operate from a 20 V supply (giving a maximum input and output signal level of 6 V), the TDA1074A can work from a supply as low as 7.5 V with reduced input and output signal levels

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	20 V
Supply current (pin 11)	I_P	typ.	22 mA
Input signal voltage (r.m.s. value)	$V_{i(rms)}$	max.	6 V
Output signal voltage (r.m.s. value)	$V_{o(rms)}$	max.	6 V
Total harmonic distortion	THD	typ.	0.05 %
Output noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	50 μV
Control range	$\Delta\alpha$	typ.	110 dB
Cross-talk attenuation (L/R)	α_{ct}	typ.	80 dB
Ripple rejection (100 Hz)	α_{100}	typ.	46 dB
Tracking of ganged potentiometers	ΔG_v	typ.	0.5 dB
Supply voltage range	V_P		7.5 to 23 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

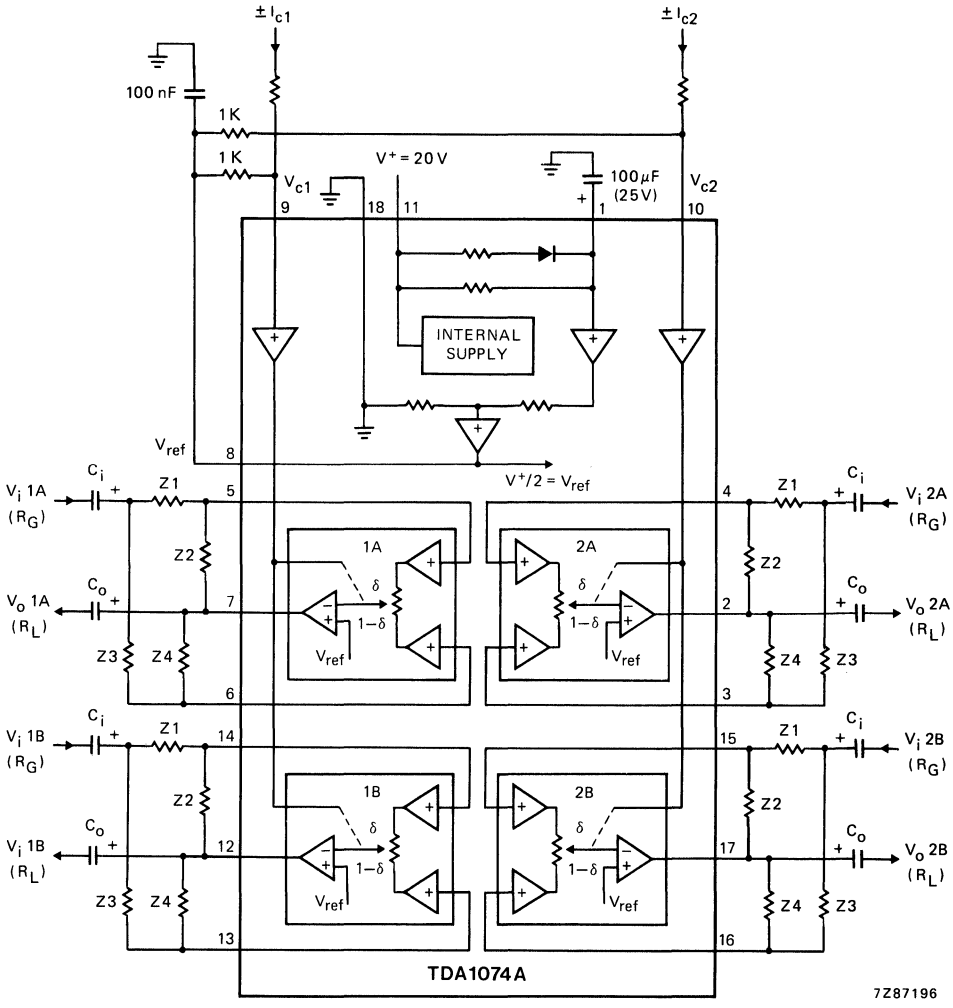


Fig. 1 Block diagram and basic external components; I_{c1} (at pin 9) and I_{c2} (at pin 10) are control input currents; V_{c1} (at pin 9) and V_{c2} (at pin 10) are control input voltages with respect to $V_{ref} = V_P/2$ at pin 8; Z1 = Z2 = Z3 = Z4 = 22 kΩ; the input generator resistance R_G = 60 Ω; the output load resistance R_L = 4.7 kΩ; the coupling capacitors at the inputs and outputs are C_i = 2,2 µF and C_o = 10 µF respectively.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	V_P	max.	23 V
Control voltages (pins 9 and 10)	$\pm V_{c1}; \pm V_{c2}$	max.	1 V
Input voltage ranges (with respect to pin 18) at pins 3, 4, 5, 6, 13, 14, 15, 16	V_i		0 to V_P V
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80 K/W

REMARK

The difference between the TDA1074 and its successor the TDA1074A is shown in Fig. 2 as the different component configuration at pin 8.

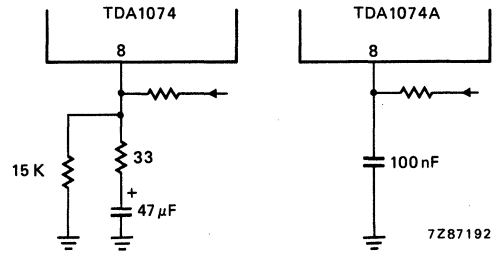


Fig. 2 Component configuration at pin 8 showing the difference between the TDA1074 and the TDA1074A.

APPLICATION INFORMATION

Treble and bass control circuit

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 3; R_G = 60 Ω; R_L > 4.7 kΩ; C_L < 30 pF; f = 1 kHz; with a linear frequency response (V_{c1} = V_{c2} = 0 V); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current (without load)	I_P	14	22	30	mA
Frequency response (−1 dB) V_{c1} = V_{c2} = 0 V	f	10	–	20 000	Hz
Voltage gain at linear frequency response (V_{c1} = V_{c2} = 0 V)	G_v*	–	0	–	dB
Gain variation at f = 1 kHz at maximum bass/treble boost or cut at ± V_{c1} = ± V_{c2} = 120 mV	ΔG_v*	–	± 1	–	dB
Bass boost at 40 Hz (ref. 1 kHz) V_{c2} = 120 mV		–	17.5	–	dB
Bass cut at 40 Hz (ref. 1 kHz) $-V_{c2}$ = 120 mV		–	17.5	–	dB
Treble boost at 16 kHz (ref. 1 kHz) V_{c1} = 120 mV		–	16	–	dB
Treble cut at 16 kHz (ref. 1 kHz) $-V_{c1}$ = 120 mV		–	16	–	dB
Total harmonic distortion at $V_{o(rms)}$ = 300 mV f = 1 kHz (measured selectively)	THD	–	0.002	–	%
f = 20 Hz to 20 kHz	THD	–	0.005	–	%
at $V_{o(rms)}$ = 5 V f = 1 kHz	THD	–	0.015	0.1	%
f = 20 Hz to 20 kHz	THD	–	0.05	0.1	%
Signal level at THD = 0.7% (input and output)	$V_{i;\,o(rms)}$	5.5	6.2	–	V
Power bandwidth at reference level $V_{o(rms)}$ = 5 V (−3 dB); THD = 0.1%	B	–	40	–	kHz
Output noise voltages signal plus noise (r.m.s. value); f = 20 Hz to 20 kHz	$V_{no(rms)}$	–	75	–	μV
noise (peak value); weighted to DIN 45 405; CCITT filter	$V_{no(m)}$	–	160	230	μV

* $G_v = V_o/V_i$.

Treble and bass control circuit

parameter	symbol	min.	typ.	max.	unit
Cross-talk attenuation (stereo)					
f = 1 kHz	α_{ct}	–	86	–	dB
f = 20 Hz to 20 kHz	α_{ct}	–	80	–	dB
Control voltage cross-talk to the outputs at f = 1 kHz; $V_{c1(rms)} = V_{c2(rms)} = 1$ mV	$-\alpha_{ct}$	–	20	–	dB
Ripple rejection at f = 100 Hz; $V_{P(rms)} < 200$ mV	α_{100}	–	46	–	dB

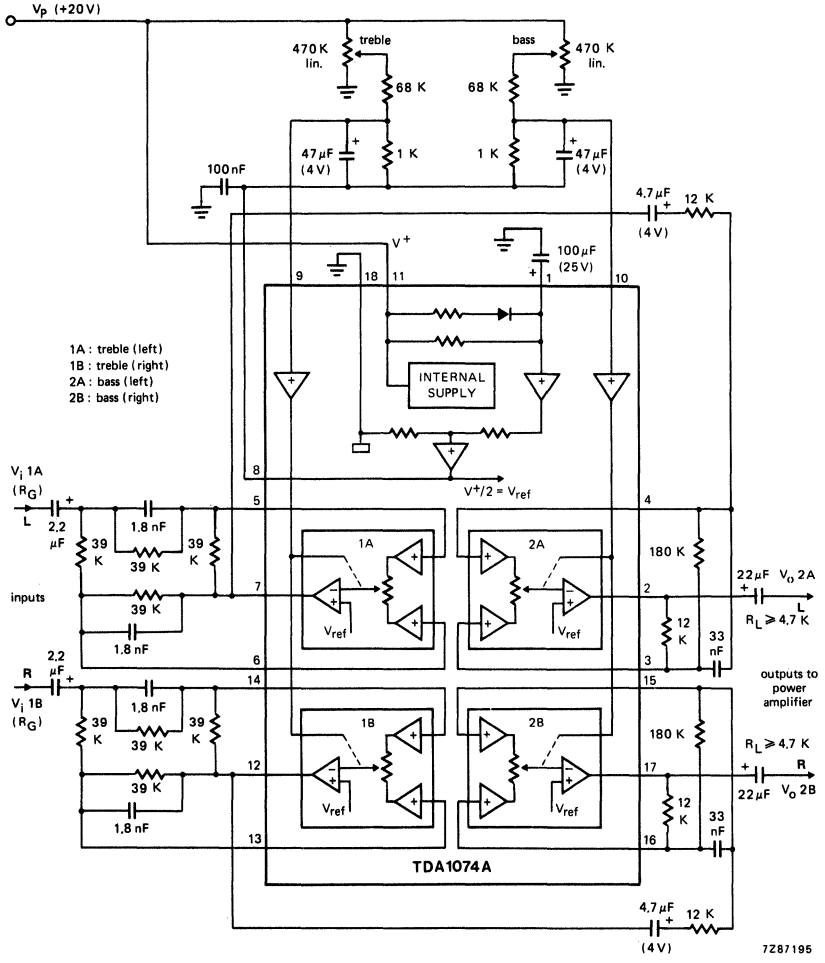


Fig. 3 Application diagram for treble and bass control.

APPLICATION INFORMATION (continued)

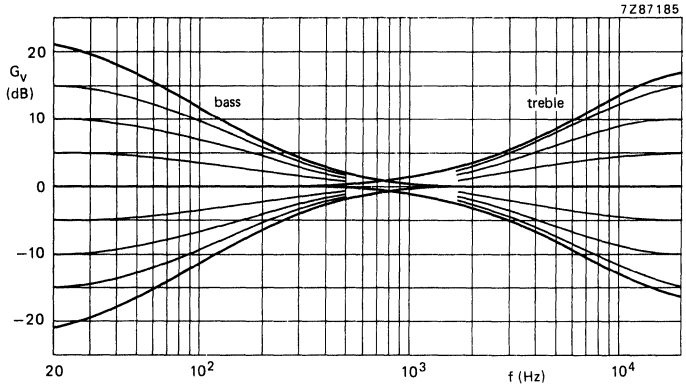


Fig. 4 Frequency response curves; voltage gain (treble and bass) as a function of frequency.

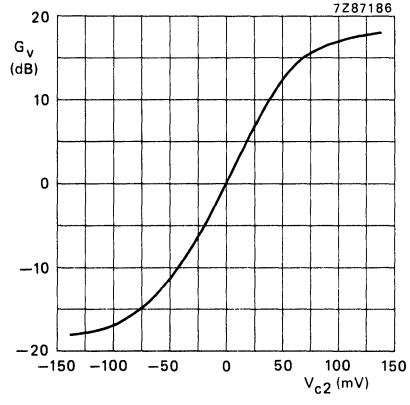


Fig. 5 Control curve; voltage gain (bass) as a function of the control voltage (V_{c2}); f = 40 Hz.

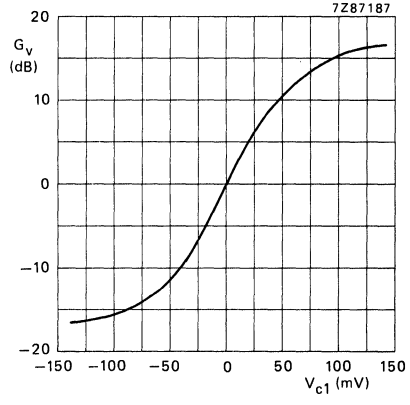
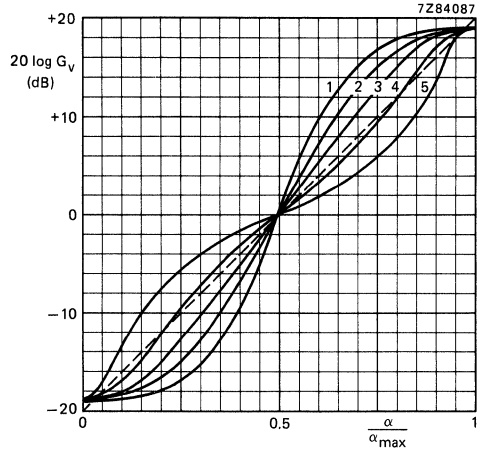


Fig. 6 Control curve; voltage gain (treble) as a function of the control voltage (V_{c1}); f = 16 kHz.



curve no.	value of R
1	10 kΩ
2	100 kΩ
3	220 kΩ
4	470 kΩ
5	1 MΩ

Fig. 7 Voltage gain ($G_V = V_o/V_i$) control curves as a function of the angle of rotation (α) of a linear potentiometer (R); for curve numbers see table above; f = 40 Hz to 16 kHz.

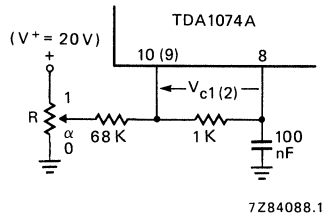


Fig. 8 Circuit diagram for measuring curves in Fig. 7.

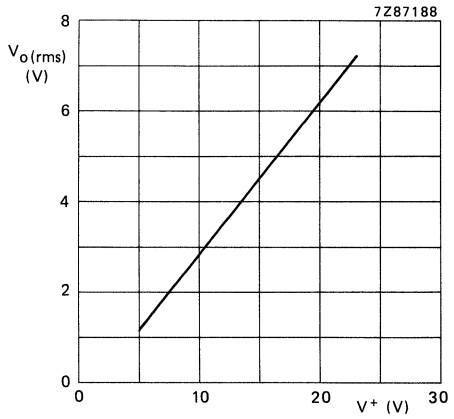


Fig. 9 Output signal level as a function of V_P; THD = 0.7%; f = 1 kHz; $V_{c1} = V_{c2} = 0$ V.

APPLICATION INFORMATION (continued)

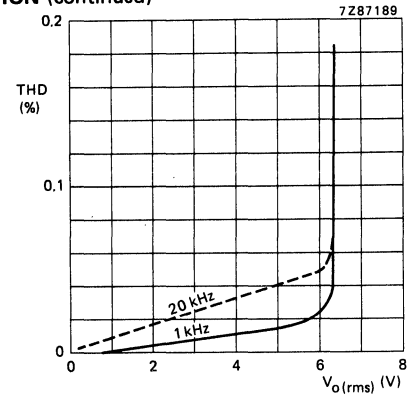


Fig. 10 Total harmonic distortion as a function of the output level; V_P = 20 V; R_L = 4.7 kΩ; $V_{c1} = V_{c2}$ = 0 V (linear, $G_{v\,tot}$ = 1). ——— f = 1 kHz; – – – – f = 20 kHz.

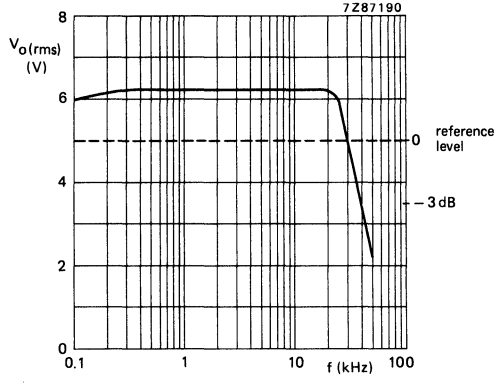


Fig. 11 Power bandwidth at THD = 0.1%; reference level is 5 V (r.m.s.).

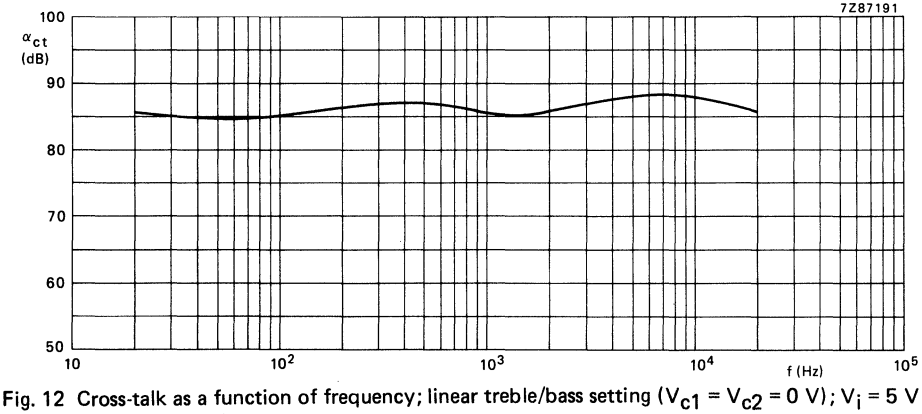
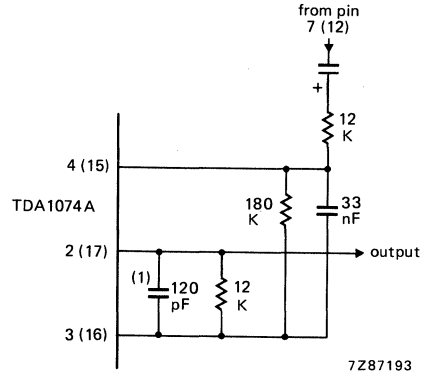


Fig. 12 Cross-talk as a function of frequency; linear treble/bass setting ($V_{c1} = V_{c2}$ = 0 V); V_i = 5 V; R_G = 60 Ω; R_L = 4.7 kΩ.

Application recommendations

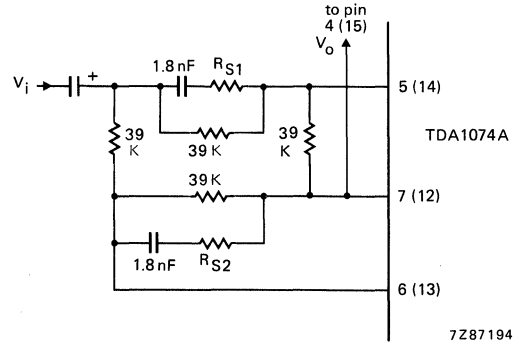
1. If one or more electronic potentiometers in an IC are not used, the following is recommended:
   a. Unused signal inputs of an electronic potentiometer should be connected to the associated output, e.g. pins 3 and 4 to pin 2.
   b. Unused control voltage inputs should be connected directly to pin 8 (V_{ref}).
2. Where more than one TDA1074A IC are used in an application, pins 1 can be connected together; however, pins 8(V_{ref}) may not be connected together directly.
3. Additional circuitry for limiting the frequency response in the ultrasonic range.



(1) $f_{-3\,dB}$ = 110 kHz at linear setting

Fig. 13 Circuit diagram for frequency response limiting.

4. Alternative circuitry for limiting the gain of the treble control circuit in the ultrasonic range.



For $R_{S1} = R_{S2}$ = 3.3 kΩ; $f_{-3\,dB} \cong$ 1 MHz at linear setting
For $R_{S1} = R_{S2}$ = 0 Ω; $f_{-3\,dB} \cong$ 100 kHz at linear setting

Fig. 14 Circuit diagram for limiting gain of treble control circuit.

Cassette Preamplifier TDA1522

GENERAL DESCRIPTION

The TDA1522 is a playback amplifier for car radio/cassette players.

Features

- Two independent amplifiers with open loop gain of typ. 90 dB
- Internal d.c. feedback via a 140 kΩ resistor from output to feedback point
- A.C. characteristics that can be determined externally by an RC network
- Electronic on/off switching with transient suppression for switch on
- Head input at d.c. ground that eliminates the input coupling capacitor
- Minimal external component requirement
- Stability down to a gain of 30 dB
- Low input noise
- Low distortion
- D.C. input current $< 2\ \mu A$
- Wide supply voltage range

5

QUICK REFERENCE DATA

Supply voltage range (pin 8)	V_P	7.5 to 23	V
Supply current (pin 8)	I_P	typ. 5	mA
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Total harmonic distortion	THD	typ. 0.05	%
Channel separation at R_S = 10 kΩ; L_S = 0	α	min. 45	dB

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142).

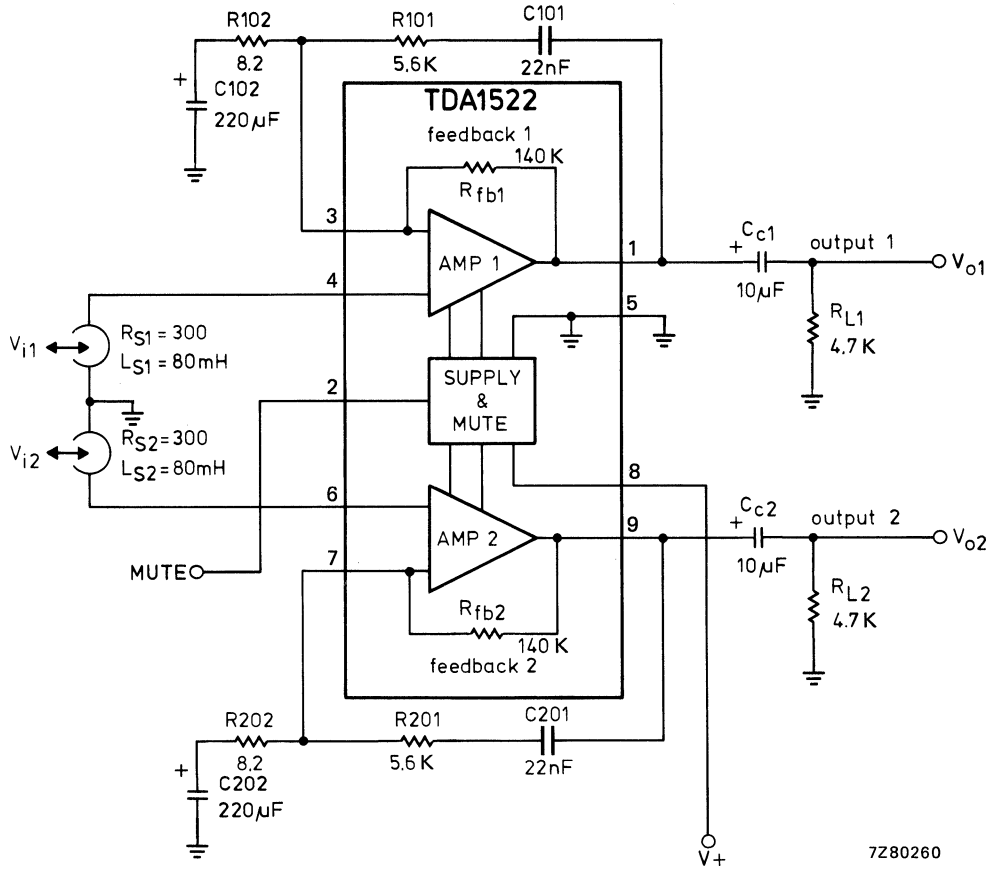


Fig. 1 Block diagram with external components; also used as test circuit.

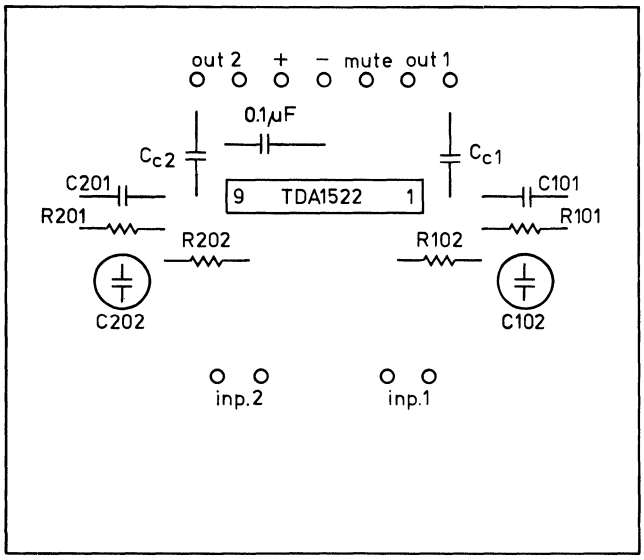


Fig. 2 Printed-circuit board component side, showing component layout for circuit of Figure 1.

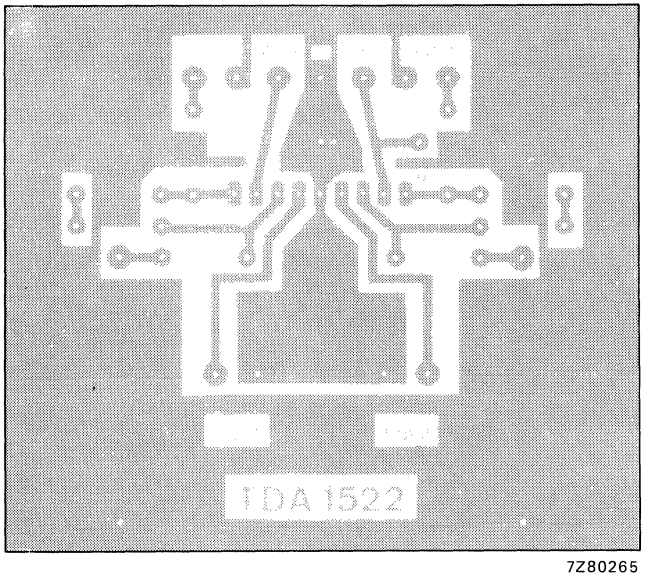


Fig. 3 Printed-circuit board, showing track side. Dimensions 75 mm x 65 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_P	7.5 to 23	V
Power dissipation	P_{tot}	max. 800	mW
Feedback current (pins 3 and 7)	I_{fb}	max. 10	mA
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range	T_{amb}	−30 to +85	°C

Note

All pins except 3 and 7 (feedback) can be connected to V_P (pin 8) or ground, (pin 5).

CHARACTERISTICS

V_P = 8.5 V; T_{amb} = 25 °C; test circuit Fig. 1 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage range	V_P	7.5	–	23	V
Supply current	I_P	–	5	–	mA
Inputs (pin 4 or 6)					
Noise input voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz*	$V_{n(rms)}$	–	1.6	–	μV
Noise input voltage at R_S = 0; f = 1 kHz*, **	V_n	–	5	–	$nV/\sqrt{Hz}$
Noise input current at f = 1 kHz*, ▲	I_n	–	1.2	–	$pA/\sqrt{Hz}$
D.C. input current at pins 4 and 6	$-I_4; -I_6$	–	–	2	μA
Outputs (pin 1 or 9)					
Output voltage at V_i = 0.3 mV; f = 315 Hz	V_o	–	0.72	–	V
at THD= 1%; f = 1 kHz	V_o	1.0	–	–	V
Output source current at $V_{2-5} \geqslant 7.5$ V; mute OFF	$-I_o$	5	10	–	mA
D.C. output voltage	V_o	–	3.7	–	V
Noise output voltage (weighted) at R_S = 300 Ω; L_S = 80 mH					
as DIN A (r.m.s. value)	$V_{n(rms)}$	–	700	–	μV
as CCITT (peak value)	$V_{n(m)}$	–	1200	–	μV
as CCIR (peak value)	$V_{n(m)}$	–	1600	–	μV
Noise output voltage (unweighted) at R_S = 300 Ω; L_S = 80 mH					
as DIN 45405 (peak value)	$V_{n(m)}$	–	1800	–	μV

* Measured in Fig. 4. ** See also Fig. 6. ▲ See also Fig. 7.

parameter	symbol	min.	typ.	max.	unit
Mute on/off characteristics (pin 2)*					
Mute ON voltage at mute switch closed	V_m	0	–	1	V
Mute ON current at mute switch closed or $V_{2-5} = 0$ V	I_m	–	2.7	–	μA
Mute OFF voltage at mute switch open	V_m	7.5	–	V_P	V
Impedance					
Input impedance** at f = 1 kHz	$\|Z_i\|$	200	–	–	kΩ
Output impedance** at f = 1 kHz	$\|Z_o\|$	–	–	1	kΩ
General					
Internal feedback resistor**	R_{fb}	100	140	180	kΩ
Open-loop voltage gain** at f = 315 Hz	G_v	–	90	–	dB
Channel separation at $R_S = 10$ kΩ; $L_S = 0$; (note 1)	α	45	–	–	dB
Power supply ripple rejection at $V_{P(rms)} = 0.1$ V; f = 100 Hz (note 2)	RR	90	95	–	dB
Total harmonic distortion at f = 1 kHz; $V_o = 0.72$ V (note 3)	THD	–	0.05	–	%

Notes

1. Frequency range 300 Hz to 20 kHz.
2. Referred to the input.
3. Measured selective.

* See also Fig. 5.
** Applies to each amplifier.

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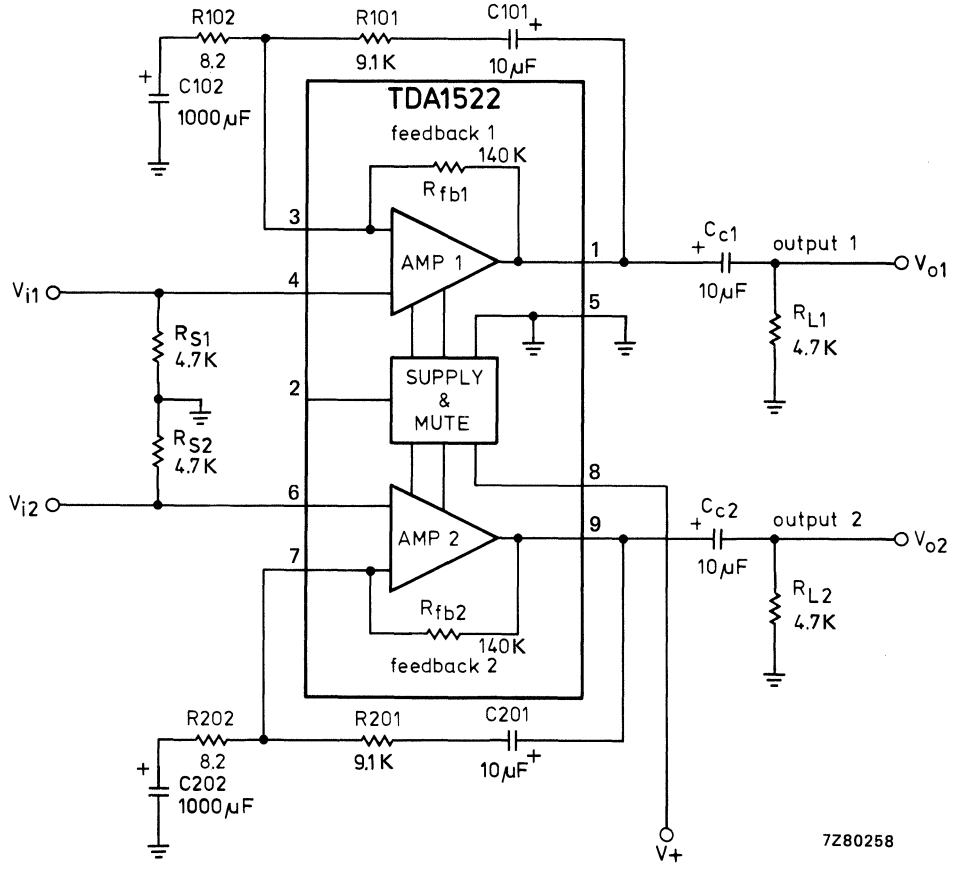


Fig. 4 Test circuit for noise measurement.

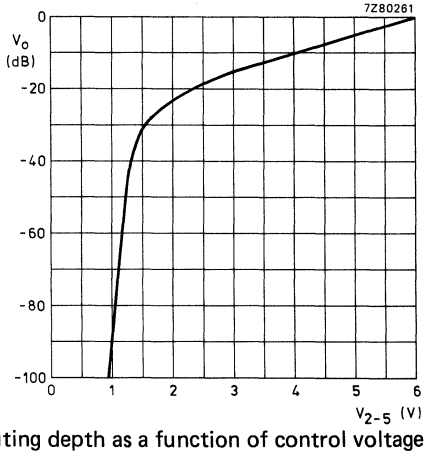


Fig. 5 Muting depth as a function of control voltage at pin 2.

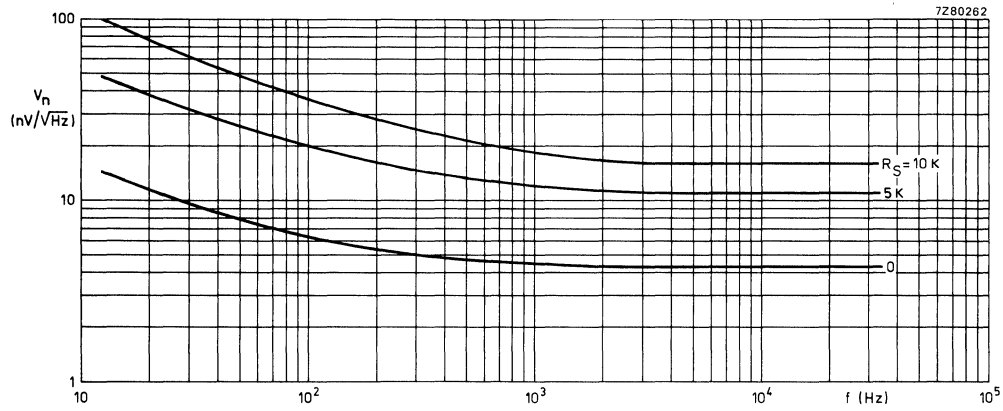


Fig. 6 Noise input voltage as a function of frequency.

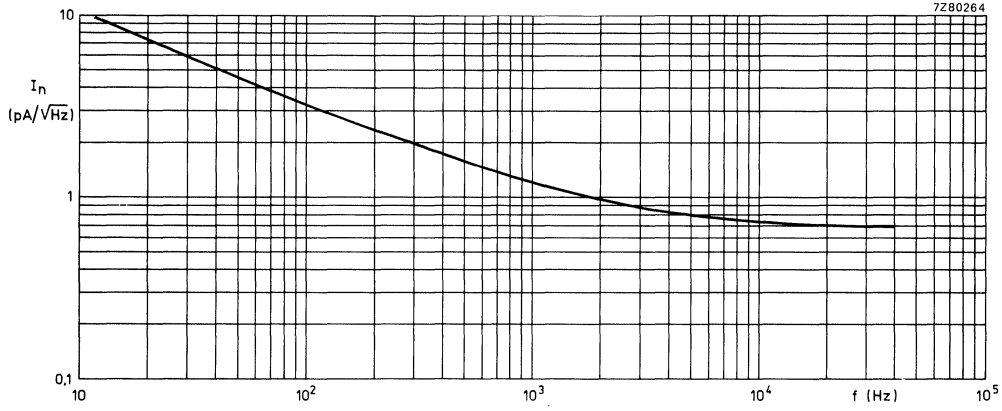


Fig. 7 Noise input current as a function of frequency.

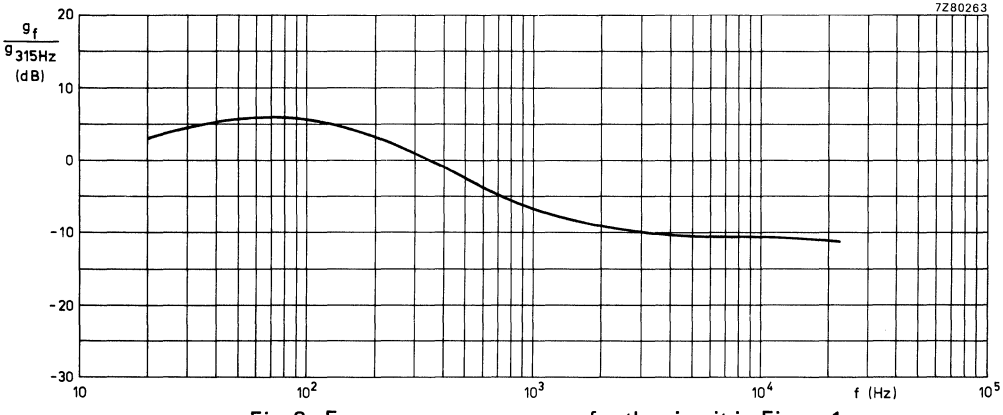


Fig. 8 Frequency response curve for the circuit in Figure 1.

APPLICATION INFORMATION

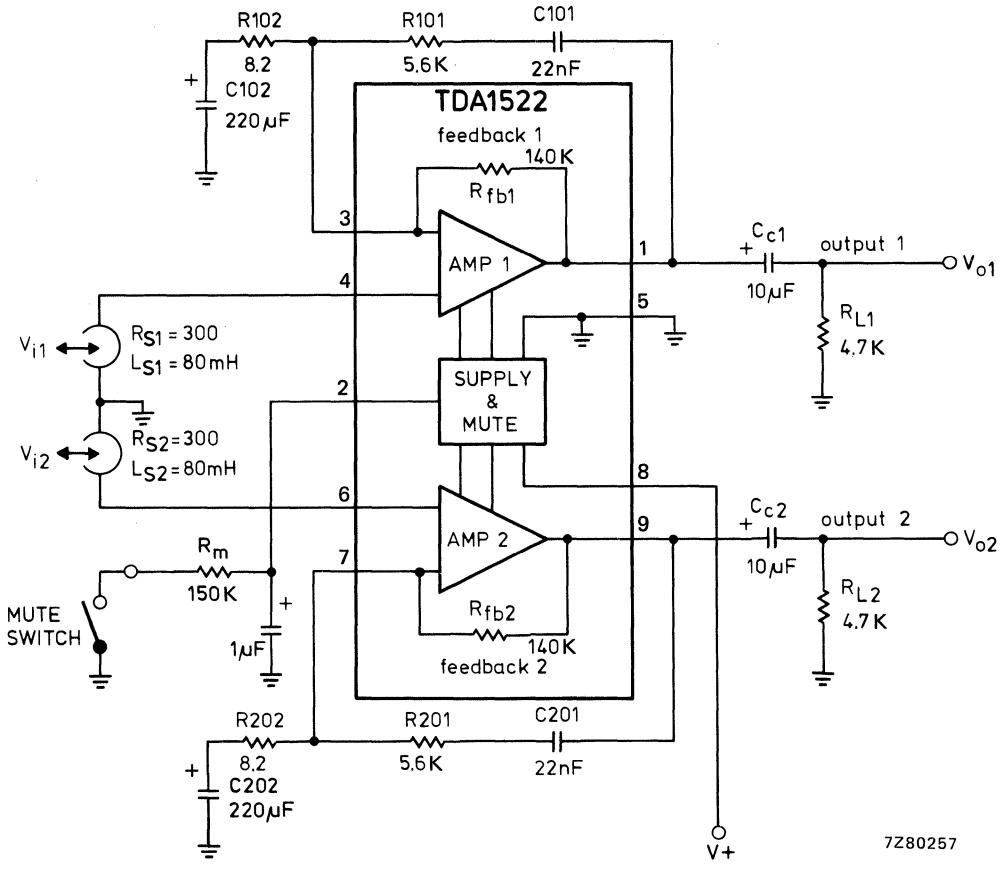


Fig. 9 Simple mute application.

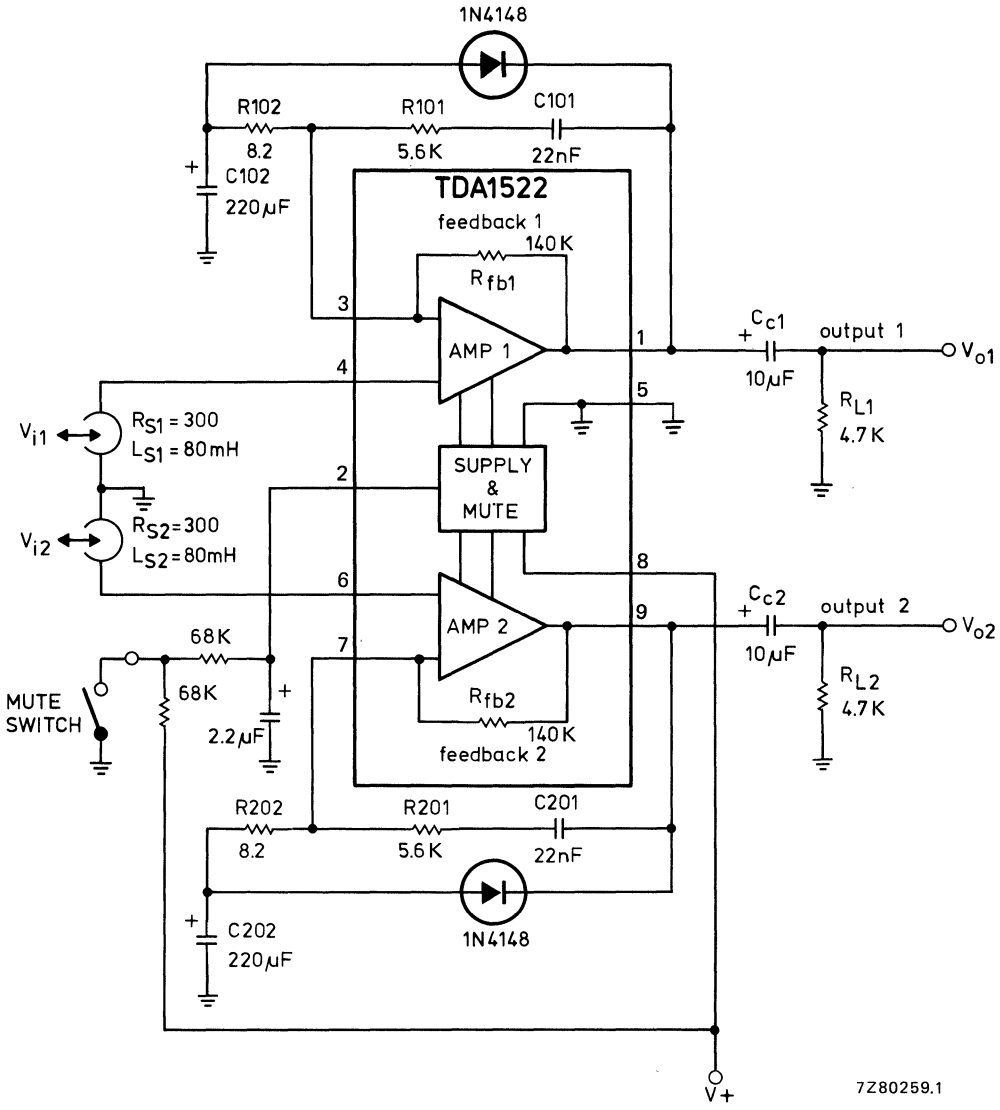


Fig. 10 Application for plop-free muting.

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

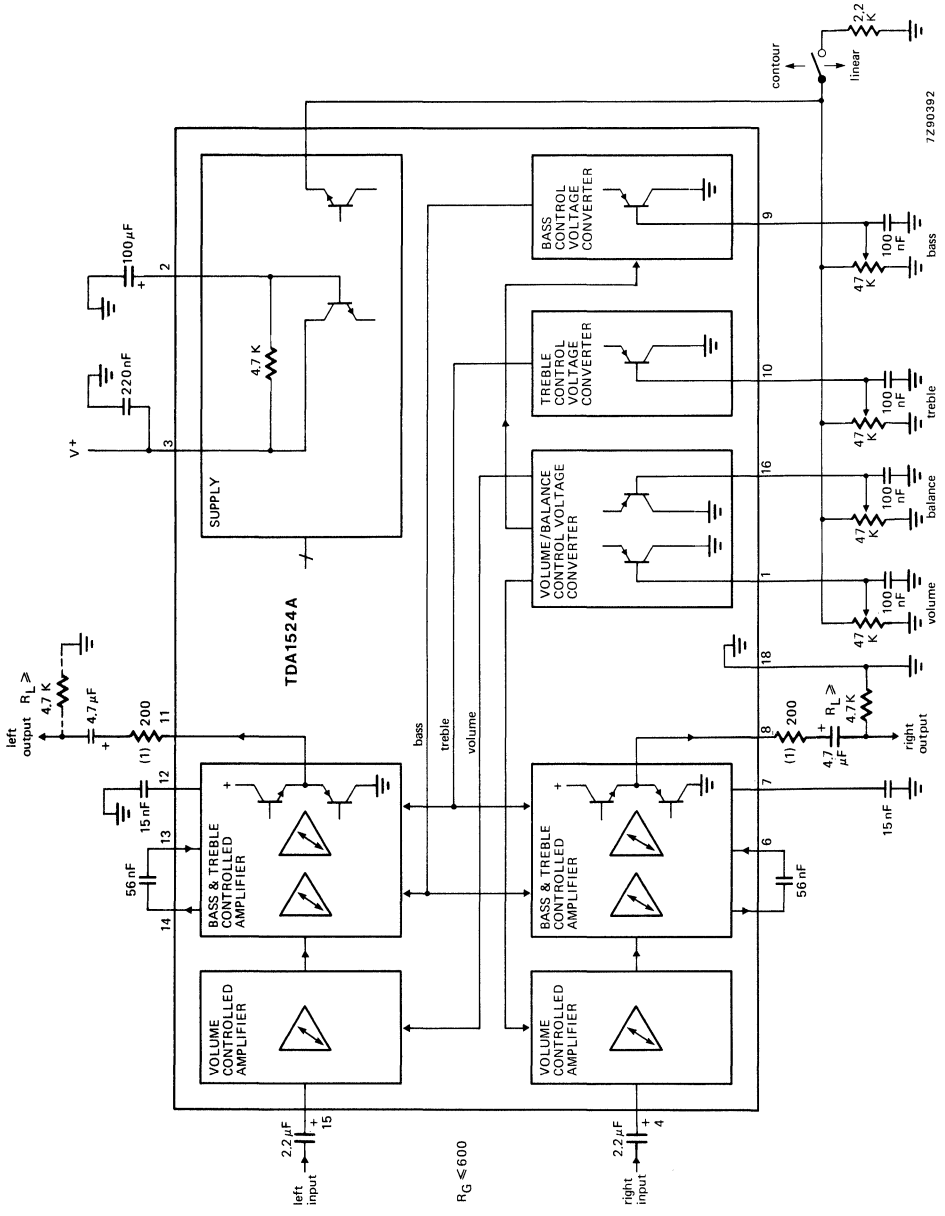
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3-18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2.5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	G_V		−80 to + 21.5 dB
Bass control range at 40 Hz	ΔG_V	typ.	± 15 dB
Treble control range at 16 kHz	ΔG_V	typ.	± 15 dB
Total harmonic distortion	THD	typ.	0.3 %
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; V_P = 12 V;			
for max. voltage gain	$V_{no(rms)}$	typ.	310 μV
for voltage gain G_V = −40 dB	$V_{no(rms)}$	typ.	100 μV
Channel separation at G_V = −20 to + 21.5 dB	α_{cs}	typ.	60 dB
Tracking between channels at G_V = −20 to + 26 dB	ΔG_V	max.	2.5 dB
Ripple rejection at 100 Hz	RR	typ.	50 dB
Supply voltage range (pin 3)	$V_P = V_{3-18}$		7.5 to 16.5 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

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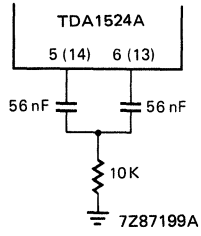

Fig. 2 Double-pole low-pass filter for improved bass-boost.

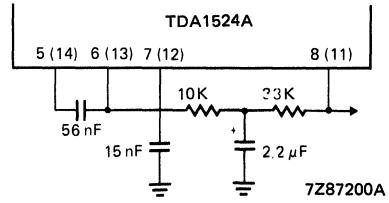

Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	max.	20	V
Total power dissipation	P_{tot}	max.	1200	mW
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

D.C. CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7.5	–	16.5	V
Supply current					
at $V_P = 8.5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at $V_P = 8.5$ V	$V_{4,15-18}$	3.8	4.25	4.7	V
at $V_P = 12$ V	$V_{4,15-18}$	5.3	5.9	6.6	V
at $V_P = 15$ V	$V_{4,15-18}$	6.5	7.3	8.2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at $V_P = 8.5$ V	$V_{8,11-18}$	3.3	4.25	5.2	V
at $V_P = 12$ V	$V_{8,11-18}$	4.6	6.0	7.4	V
at $V_P = 15$ V	$V_{8,11-18}$	5.7	7.5	9.3	V
Pin 17					
Internal potentiometer supply voltage					
at $V_P = 8.5$ V	V_{17-18}	3.5	3.75	4.0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0.5	mA
linear (switch closed)	$-I_{17}$	1.5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10.8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4.5	–	$V_P/2-V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1.0	–	4.25	V
using internal supply	$V_{1,9,10,16}$	0.25	–	3.8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

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A.C. CHARACTERISTICS

$V_P = V_{3-18} = 8.5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7\ k\Omega$; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{V\ max}$	20.5	21.5	23	dB
Volume control range; $G_{V\ max}/G_{V\ min}$	ΔG_V	90	100	–	dB
Balance control range; G_V = 0 dB (Fig. 6)	ΔG_V	–	–40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_V	± 12	± 15	–	dB
Treble control range at 16 kHz (Fig. 8)	ΔG_V	± 12	± 15	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: G_V = 20 dB	$R_{i4,15}$	10	–	–	kΩ
G_V = –40 dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at G_V = –20 to + 21.5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0.5\ V_{17-18}$	ΔG_V	–	–	± 3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0.5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1.5	dB
Tracking between channels					
for G_V = 21.5 to –26 dB					
f = 250 Hz to 6.3 kHz; balance adjusted at					
G_V = 10 dB	ΔG_V	–	–	2.5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling					
at V_P = 8.5 V; THD = 0.5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1.4	–	–	V
at V_P = 8.5 V; THD = 0.7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1.8	2.4	–	V
at V_P = 12 V; THD = 0.5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1.4	–	–	V
at V_P = 12 V; THD = 0.7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2.0	3.2	–	V
at V_P = 15 V; THD = 0.5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1.4	–	–	V
at V_P = 15 V; THD = 0.7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2.0	3.2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8.5 V; THD = 0.5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1.8	2.0	–	V
at V_P = 8.5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2.2	–	V
at V_P = 12 V; THD = 0.5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2.5	3.0	–	V
at V_P = 15 V; THD = 0.5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3.5	–	V
Noise performance (V_P = 8.5 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_V = −3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_V = −40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_V = −16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_V = −40 dB)	$V_{no(m)}$	–	400	–	μV

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parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_V = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405					
of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble					
(contour off; G_V = −40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_V}\ ;\ G_{V\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4.5 dB to r.m.s. values.

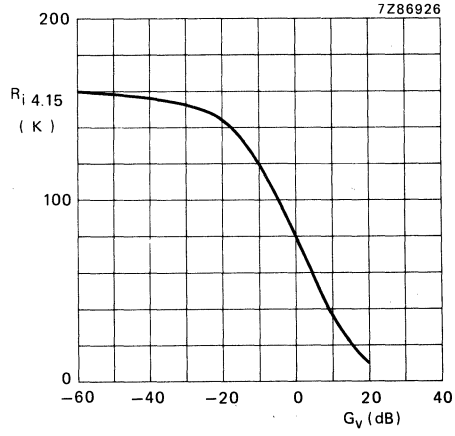

Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

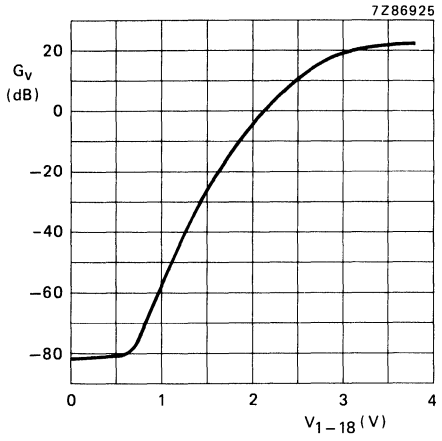

Fig. 5 Volume control curve; voltage gain (G_V) as a function of control voltage ($V_{1\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 1 kHz.

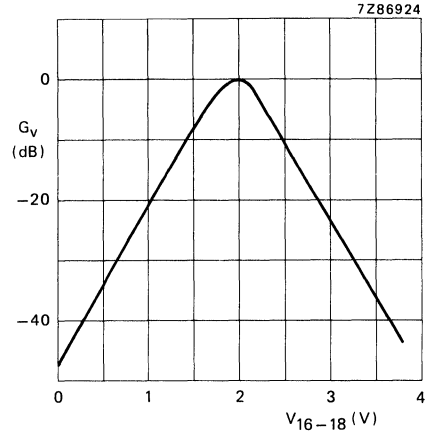

Fig. 6 Balance control curve; voltage gain (G_V) as a function of control voltage ($V_{16\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V.

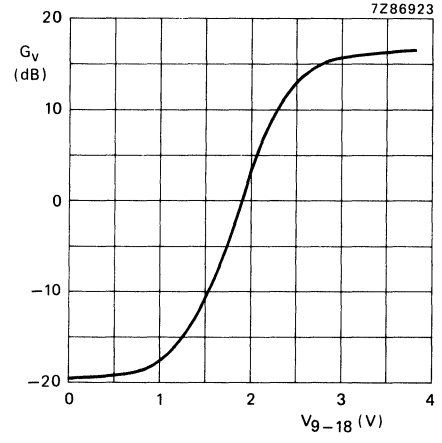

Fig. 7 Bass control curve; voltage gain (G_V) as a function of control voltage ($V_{9\text{-}18}$). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 40 Hz.

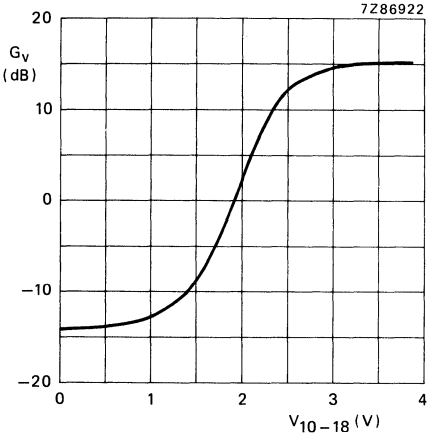

Fig. 8 Treble control curve; voltage gain (G_V) as a function of control voltage ($V_{10\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 16 kHz.

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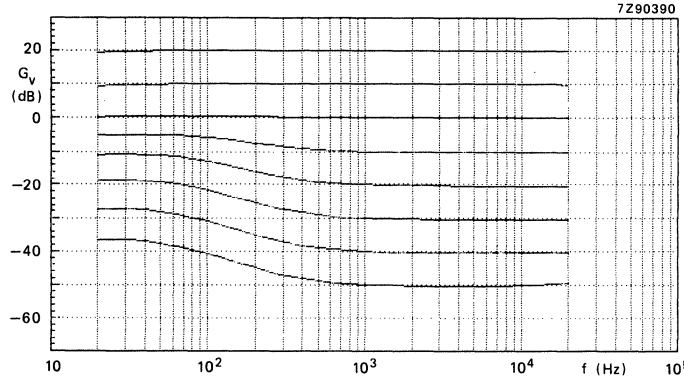


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8.5 V.

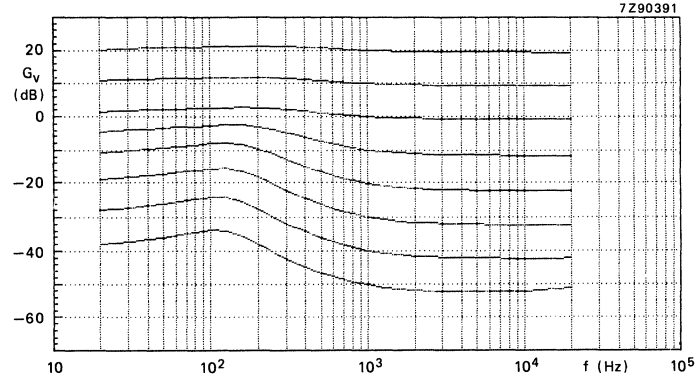


Fig. 10 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8.5 V.

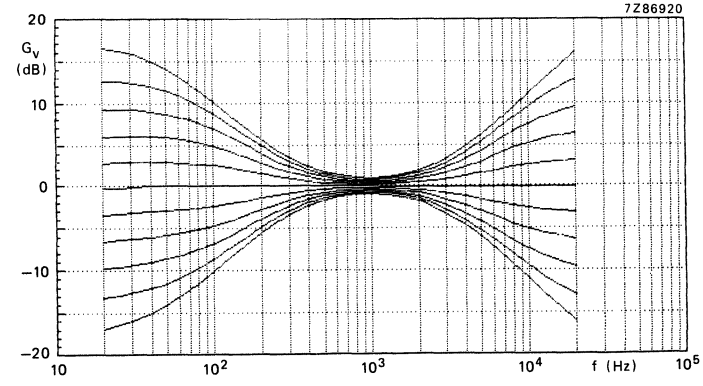


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8.5 V.

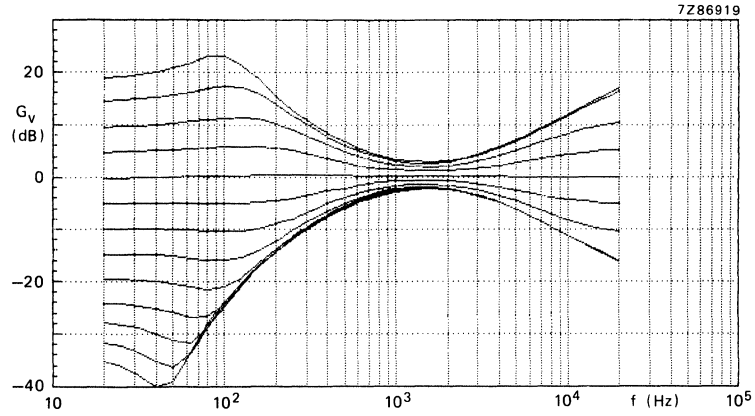


Fig. 12 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8.5 V.

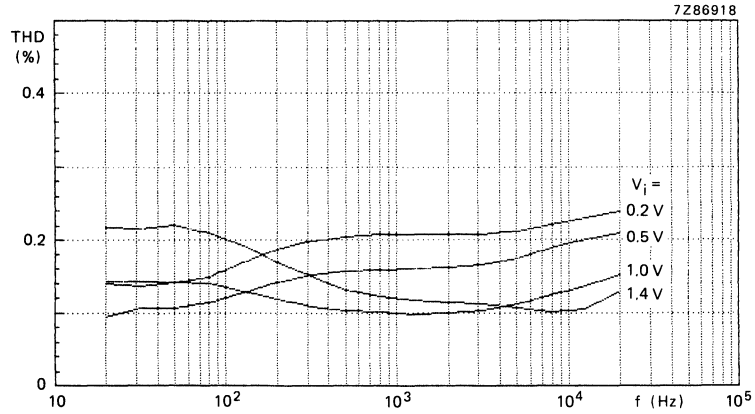


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8.5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

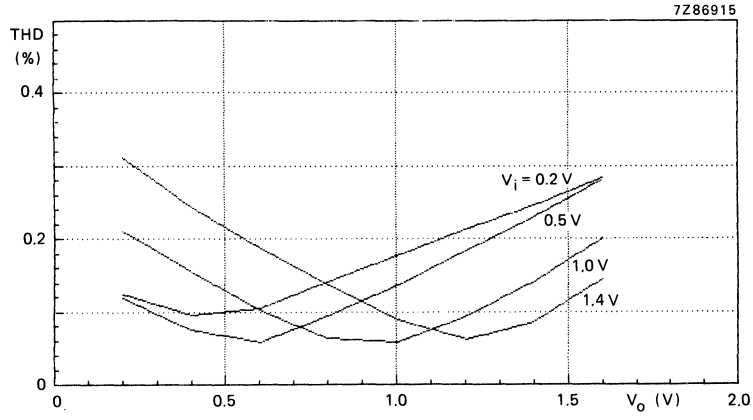
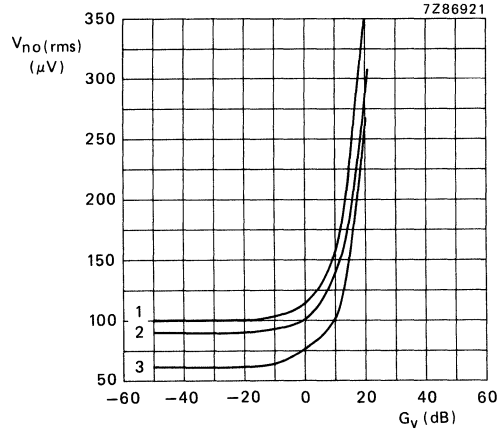


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig. 1; V_P = 8.5 V; f_i = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8.5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

PLL Stereo Decoder — TDA1578A

GENERAL DESCRIPTION

The TDA1578A is a PLL stereo decoder based on the time-division multiplex principle.

Features

- adjustable input and output voltage levels
- automatic mono/stereo switching with hysteresis, controlled by both pilot signal and field strength level
- analogue control of mono/stereo change over
- pilot indicator driver
- analogue muting control
- muting indicator driver
- oscillator with decoupled frequency measurement output
- electronic smoothing of the supply voltage

QUICK REFERENCE DATA

5

Measured with a frequency deviation $\Delta f = \pm 75$ kHz without pilot; $f_m = 1$ kHz					
Supply voltage (pin 8)	$V_P = V_{8-7}$	typ.	8,5	15	V
Supply current (pin 8)	$I_P = I_8$	typ.	21	30	mA
Multiplex input signal (adjustable)	$V_{MUX(p-p)}$	typ.	0,5	1	V
Input resistance (adjustable)	R_i	typ.	47		kΩ
A.F. output voltage (R = 15 kΩ)	V_o	typ.	0,75	1,5	V
Output resistance	R_o		low-ohmic		
Spread in gain	ΔG_v	⩽	1		dB
Channel separation	α	typ.	50		dB
Total harmonic distortion	THD	⩽	0,3	0,1	%
Signal-to-noise ratio	S/N	typ.	90		dB
Carrier and harmonic suppression					
pilot signal; f = 19 kHz	α_{19}	typ.	32		dB
subcarrier; f = 38 kHz	α_{38}	typ.	50		dB
f = 57 kHz	α_{57}	typ.	46		dB
f = 76 kHz	α_{76}	typ.	60		dB
traffic radio (V.W.F.); f = 57 kHz	$\alpha_{57(VWF)}$	typ.	70		dB
SCA (Subsidiary Communications Authorization); f = 67 kHz	α_{67}	typ.	70		dB
ACI (Adjacent Channel Interference); f = 114 kHz	α_{114}	typ.	80		dB
intermodulation; f = 10/13 kHz	α_2, α_3	typ.	70		dB
Supply voltage range (pin 8)	$V_P = V_{8-7}$		7,5 to 18		V
Operating ambient temperature range	T_{amb}		−30 to + 80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

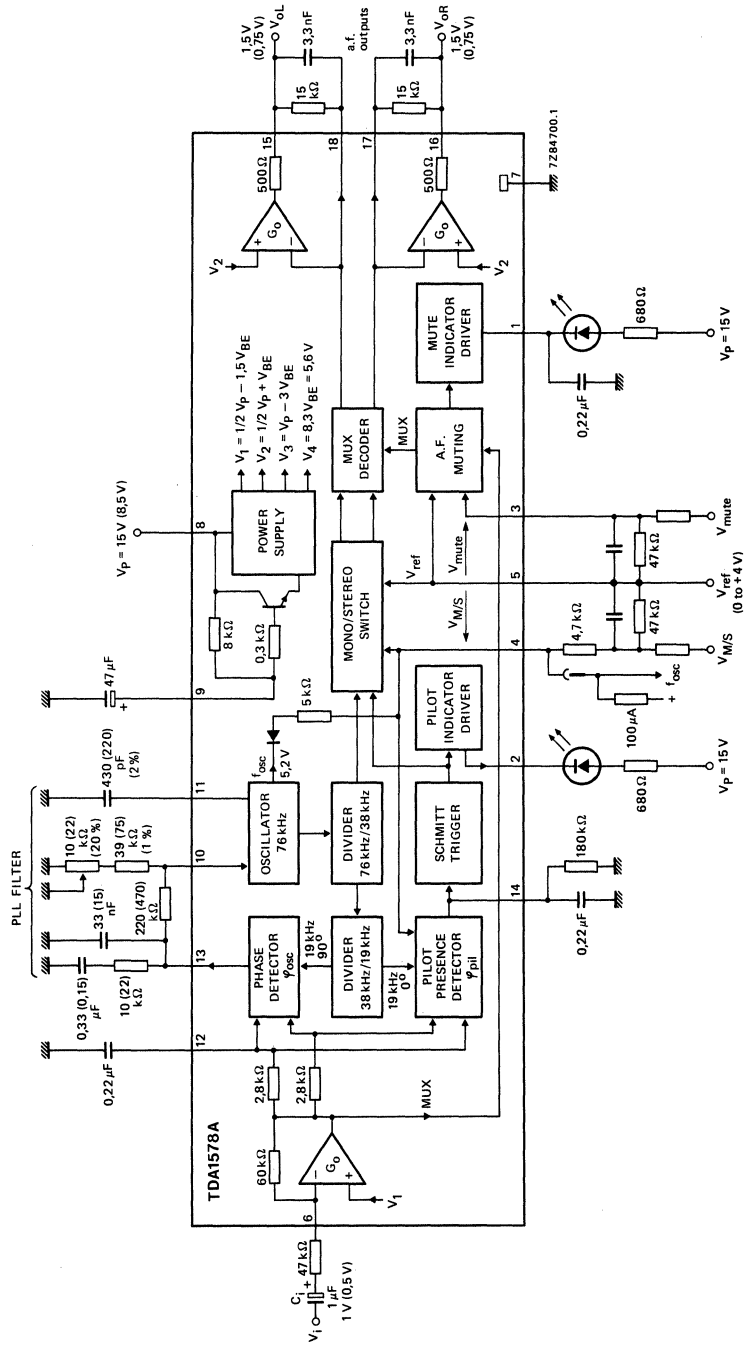


Fig. 1 Block diagram with external components; used as test circuit. Values given in parentheses are for V_P = 8,5 V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-7}$	max.	20	V
Input voltages (pins 3, 4 and 5)	$V_{3;4;5-7}$		0 to 12	V
Indicator driver output voltage	$V_{1;2-7}$	max.	24	V
Indicator driver output current	$I_1; I_2$	max.	30	mA
Total power dissipation at T_{amb} = 25 °C	P_{tot}	max.	1,2	W
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c-a}$	=	80	K/W

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CHARACTERISTICS (measured in Fig. 1)

Input signal: m = 100% ($\Delta f = \pm 75$ kHz); pilot signal: m = 9% ($\Delta f = \pm 6{,}75$ kHz); modulation frequency: 1 kHz; $V_{3-5} = V_{4-5} = 0$ V; de-emphasizing time: T = 50 μs; oscillator adjusted to f_{osc} at a pilot voltage $V_i = 0$ V; $T_{amb} = 25\ ^{o}C$; unless otherwise specified

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Supply voltage range (pin 8)	–	V_P	7,5	–	18	V
Supply current (except output and indicator) pin 8	8,5	I_P	–	21	–	mA
	15	I_P	–	30	40	mA
Nominal multiplex input voltage (peak-to-peak value)	8,5	$V_{MUX(p-p)}$	–	0,5	–	V
R_i = 47 kΩ	15	$V_{MUX(p-p)}$	–	1,0	–	V
Overdrive reserve of input						
at THD = 1 %	8,5		3	6	–	dB
at THD = 0,3 %	15		3	6	–	dB
A.F. output voltage (r.m.s. value; mono without pilot)						
$R_{15-18} = R_{16-17}$ = 15 kΩ	8,5	$V_{o(rms)}$	–	0,75	–	V
	15	$V_{o(rms)}$	–	1,5	–	V
$R_{15-18} = R_{16-17}$ = 24 kΩ	8,5	$V_{o(rms)}$	–	1,2	–	V
	15	$V_{o(rms)}$	–	2,4	–	V
Overdrive reserve of output $R_{15-18} = R_{16-17}$ = 24 kΩ	*		3	–	–	dB
Spread in output voltage levels	*	$\pm \Delta V_o/V_o$	–	–	1	dB
Difference of output voltage levels	*	$\pm \Delta V_{15-16}/V_o$	–	–	1	dB
Output resistance	*	R_o	low-ohmic			
Available output current pins 15 and 16	*	$\pm I_o$	–	–	–	mA
Modulation range at output (unloaded)	*	$V_{15;16-7}$	–	1 to $V_{9-7}-1$	–	V
Internal current limiting	*	I_o	–	15	–	mA
D.C. output voltage	8,5	$V_{15;16-7}$	3,6	4,1	4,6	V
$R_{15-18} = R_{16-17}$ = 24 kΩ	15	$V_{15;16-7}$	7,0	7,7	8,4	V
D.C. current	8,5	$-I_{17;18}$	–	33	–	μA
(pins 17 and 18)	15	$-I_{17;18}$	–	23	–	μA

* V_P = 8,5 or 15 V.

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Channel separation	8,5	α	32	50	–	dB
at V_{4-5} = 0 V	15	α	39	50	–	dB
Total harmonic distortion	8,5	THD	–	0,1	0,3	%
	15	THD	–	0,04	0,1	%
Signal-to-noise ratio	8,5	S/N	–	87	–	dB
f = 20 Hz to 16 kHz	15	S/N	–	90	–	dB
Carrier and harmonic suppression at the output						
pilot signal; f = 19 kHz	*	α_{19}	–	32	–	dB
subcarrier; f = 38 kHz	*	α_{38}	40	50	–	dB
f = 57 kHz	*	α_{57}	–	46	–	dB
f = 76 kHz	*	α_{76}	–	60	–	dB
intermodulation (note 1) f_m = 10 kHz; spurious signal f_s = 1 kHz						
PLL-filter Fig. 1	*	α_2	–	50	–	dB
PLL-filter Fig. 2	*	α_2	–	70	–	dB
f_m = 13 kHz; spurious signal f_s = 1 kHz	*	α_3	–	75	–	dB
traffic radio (V.W.F.); f = 57 kHz (note 2)	*	$\alpha_{57(VWF)}$	–	70	–	dB
SCA (Subsidiary Communications Authorization); f = 67 kHz (note 4)	*	α_{67}	–	70	–	dB
ACI (Adjacent Channel Interference) (note 3);						
f = 114 kHz	*	α_{114}	–	80	–	dB
f = 190 kHz	*	α_{190}	–	52	–	dB
Ripple rejection at the output; f = 100 Hz; $V_{P(rms)}$ = 100 mV (pin 8)	*	RR_{100}	40	43	–	dB
Voltage on filter capacitor without external load	*	V_{9-7}	–	V_P–0,25	–	V
Source resistance	*	R_{9-8}	6	8	10	kΩ

* V_P = 8,5 or 15 V.

CHARACTERISTICS (continued)

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Mono/stereo control						
Pilot threshold voltages (peak-to-peak values)						
for stereo 'ON'	8,5	$V_{i(p-p)}$	–	21	30	mV
	15	$V_{i(p-p)}$	–	43	61	mV
for mono 'ON'	8,5	$V_{i(p-p)}$	6	15	–	mV
	15	$V_{i(p-p)}$	12	30	–	mV
Switch hysteresis $V_{i\,ON}/V_{i\,OFF}$	*	ΔV_i	–	3	–	dB
Switching time at $C_{14-7} = 0{,}22\ \mu F$						
for stereo 'ON'	*	$t_{st\,ON}$	–	15	–	ms
for mono 'ON'	*	$t_{m\,ON}$	–	27	–	ms
External mono/stereo control (see Fig. 12 and note 5)						
Switching voltage for external mono control	8,5	V_{14-7}	–	–	0,7	V
	15	V_{14-7}	–	–	1,4	V
	*	or: $-V_{4-5}$	315	–	–	mV
Control voltage for channel separation: α = 6 dB	8,5	$-V_{4-5}$	–	120	–	mV
	15	$-V_{4-5}$	–	130	–	mV
	*	ΔV_{4-5}	–	–	± 20	mV
α = 26 dB	8,5	$-V_{4-5}$	–	70	–	mV
	15	$-V_{4-5}$	–	80	–	mV
Control voltage for mono 'ON'	8,5	$-V_{4-5}$	–	240	–	mV
	15	$-V_{4-5}$	–	270	–	mV
for stereo 'ON'	8,5	$-V_{4-5}$	–	220	–	mV
	15	$-V_{4-5}$	–	250	–	mV
Control voltage difference for α = 6 dB; stereo 'ON'	8,5	ΔV_{4-7}	80	100	120	mV

* V_P = 8,5 or 15 V.

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Muting circuit (see Fig. 13 and note 5)						
Control voltage for an attenuation: α = 3 dB	8,5	$-V_{3-5}$	–	140	–	mV
	15	$-V_{3-5}$	–	145	–	mV
	*	ΔV_{3-5}	–	± 20	–	mV
α = 26 dB	8,5	$-V_{3-5}$	–	255	–	mV
	15	$-V_{3-5}$	–	270	–	mV
Attenuation						
with V_{3-5} = 0 V	*	α	–	–	0,2	dB
with $-V_{3-5}$ = 450 mV	*	α	–	80	–	dB
LED driver output current at an attenuation: α = 3 dB	*	I_1	1,2	1,7	2,2	mA
Control voltage for I_1 = 200 μA	8,5	$-V_{3-5}$	–	150	–	mV
	15	$-V_{3-5}$	–	160	–	mV
Control inputs						
Recommended voltage range	*	$V_{3;4;5-7}$	0	–	4	V
Input bias current	*	$I_{3;4;5}$	–	10	100	nA
Indicator driver						
Output saturation voltages at I_1 = 20 mA; V_{3-5} = 0 V	*	V_{1-7sat}	–	1,2	1,8	V
at I_2 = 20 mA	*	V_{2-7sat}	–	0,5	1,0	V
Output leakage current at $V_{1;2-7}$ = 24 V	*	$I_{1;2}$	–	20	–	μA

* V_P = 8,5 or 15 V.

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CHARACTERISTICS (continued)

parameter	V_P (V)	symbol	min.	typ.	max.	unit
VCO						
Oscillator frequency adjustable with R_{10-7}	*	f_{osc}	–	76	–	kHz
Spread of free-running frequency at nominal external circuitry	*	f_{osc}	71	–	82	kHz
Free-running frequency dependency (note 6)						
with temperature	*	TC	–	1×10^{-4}	–	K^{-1}
with supply voltage	*	$\Delta f_{osc}/\Delta V_P$	–	–	400	Hz/V
Capture and holding range for a pilot input voltage $V_{pil} = 0{,}5 \times V_{pil\ nom}$	*	$\Delta f/f$	± 2	–	–	%
PLL control slope (total)	*	S_{tot}	–	4,5	–	kHz/μs
D.C. voltage at pin 10	*	V_{10-7}	–	2,1	–	V
		or:	–	$3{,}2\ V_{BE}$	–	V
Frequency measuring point; internal switching threshold	*	V_{4-7}	–	6	–	V
		or:	–	$9\ V_{BE}$	–	V
Output voltage (peak-to-peak value) at pin 4; R = 4,7 kΩ	*	$V_{4-7(p-p)}$	–	350	–	mV
Output resistance	*	R_{4-7}	–	5	–	kΩ

* V_P = 8,5 or 15 V.

Notes to the characteristics

1. Intermodulation suppression (BFC: Beat-Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 1\ kHz)};\ f_s = (2 \times 10\ kHz) - 19\ kHz$$

$$\alpha_3 = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 1\ kHz)};\ f_s = (3 \times 13\ kHz) - 38\ kHz$$

measured with: 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

2. Traffic radio (V.W.F.) suppression

$$\alpha_{57(VWF)} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 1\ kHz \pm 23\ kHz)}$$

measured with: 91% stereo signal; f_m = 1 kHz; 9% pilot signal; 5% traffic subcarrier (f = 57 Hz, f_m = 23 Hz AM, m = 60%).

3. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o\ (signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 4\ kHz)};\ f_s = 110\ kHz - (3 \times 38\ kHz)$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 4\ kHz)};\ f_s = 186\ kHz - (5 \times 38\ kHz)$$

measured with: 90% mono signal; f_m = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

4. SCA (Subsidiary Communications Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (at\ 1\ kHz)}{V_{o(spurious)}\ (at\ 9\ kHz)};\ f_s = (2 \times 38\ kHz) - 67\ kHz$$

measured with: 81% mono signal; f_m = 1 kHz; 9% pilot signal; 10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

5. Assuming $V_T = \frac{k \times T}{q}$ = 28,6 mV at T_j = 330 K.

6. The effects of external components are not taken into account.

5

APPLICATION NOTES

1. When mono/stereo control and muting control are not used, pins 3, 4 and 5 have to be grounded.
2. In a receiver, channel separation adjustment can be obtained by:
   a. A capacitor at pin 12 (C_{12-7}): phasing 19/38 kHz
   b. RC or LCR filter at the input: frequency response compensation ($V_G = f(\omega)$)
   c. Feeding the output signals of the output amplifier to the inputs of the other channel.
3. PLL-filter for reduced intermodulation (α_2); see Fig. 2.
4. External mono 'ON' switch; see Fig. 3.
5. Switching 'OFF' the oscillator; see Fig. 4.

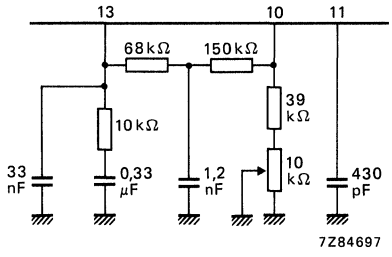


Fig. 2 PLL-filter for α_2 = 70 dB at V_P = 15 V (see also Fig. 1).

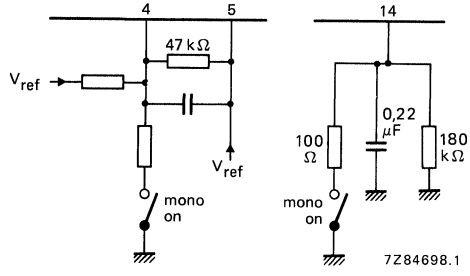


Fig. 3 (a) At pin 4; $-V_{4-5} > 300$ mV; (b) at pin 14.

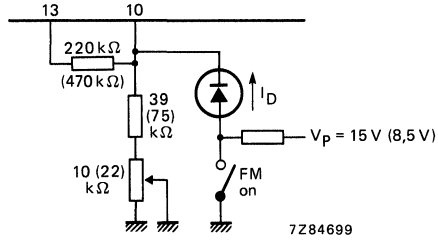


Fig. 4 The oscillator is switched-off when:
$I_D > 100$ µA (> 50 µA for V_P = 8,5 V) and $I_D < 1$ mA.

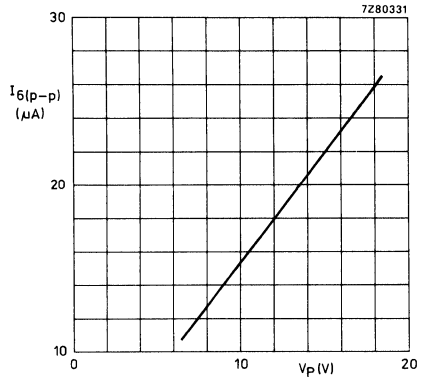


Fig. 5 Signal handling range at the input for I_{6nom} (± 75 kHz); $V_{9-7} = V_P$.

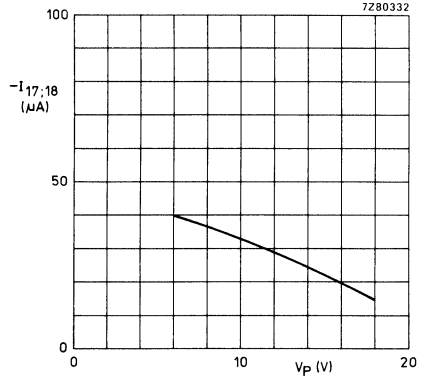
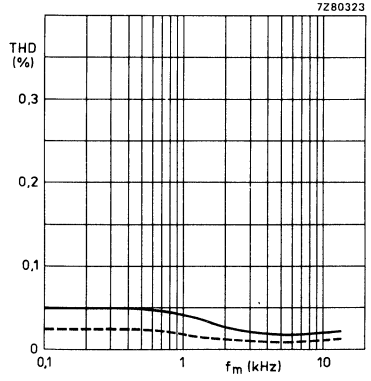


Fig. 7 D.C. current in the feedback loop of the output amplifier.



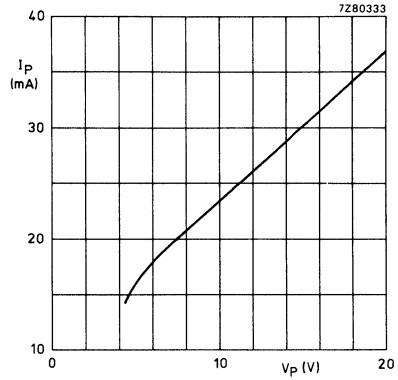


Fig. 6 Supply current comsumption at $V_{9-7} = V_P$.

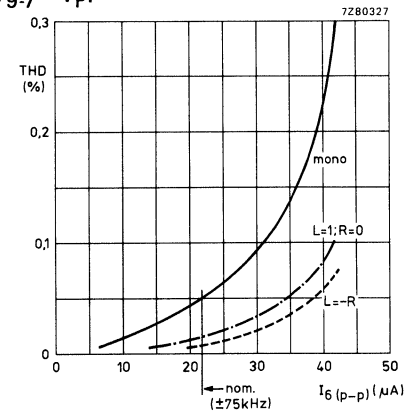


Fig. 8 Total harmonic distortion (THD) as a function of the peak-to-peak input current at pin 6; V_P = 15 V; f_m = 1 kHz; $V_{3-5} = V_{4-5}$ = 0 V.

Fig. 9 Total harmonic distortion (THD) as a function of the modulation frequency (f_m); V_P = 15 V; $I_{6(p-p)}$ = 21,5 μA.

———— mono

– – – – stereo; L = –R; 91% + 9% pilot signal.

5

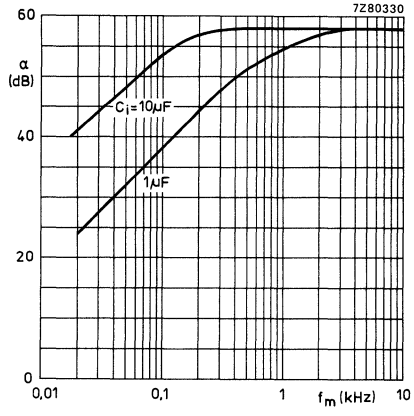


Fig. 10 Channel separation (α) as a function of the modulation frequency (f_m); V_P = 15 V; R_i = 47 kΩ; V_{4-5} = 0 V.

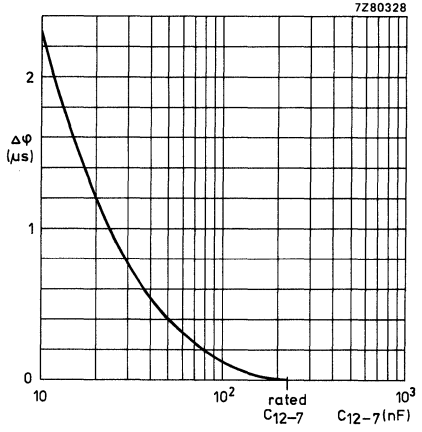


Fig. 11 Phase shift between pilot signal at the input and the internal carrier processing as a function of C_{12-7}.

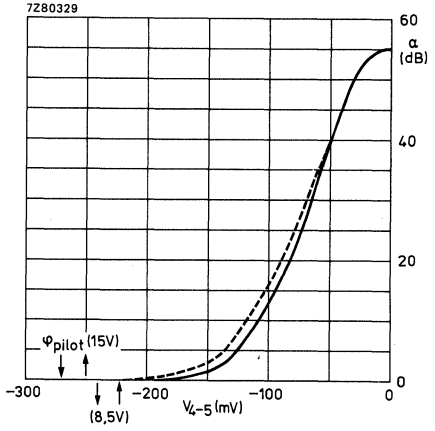


Fig. 12 Mono/stereo control at f_m = 1 kHz; α is the channel separation.
——— V_P = 8,5 V
– – – – V_P = 15 V

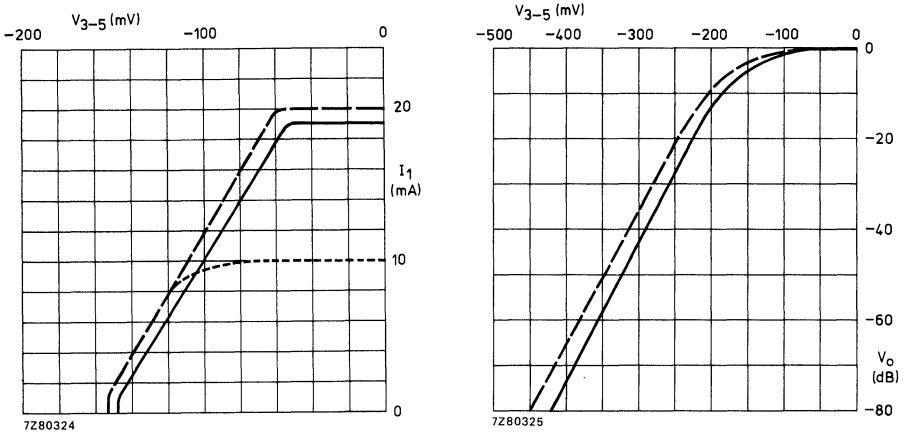


Fig. 13 Muting (V_o) and muting indicator current (I_1) as a function of V_{3-5}.

V_o in dB curves; ——— V_P = 8,5 V
– – – – V_P = 15 V

I_1 in mA curves for V_{PL}/R_{bias1} (pin 1); – – – – 22 V/1 kΩ
——— 14 V/680 Ω
- - - - - - - 10 V/680 Ω

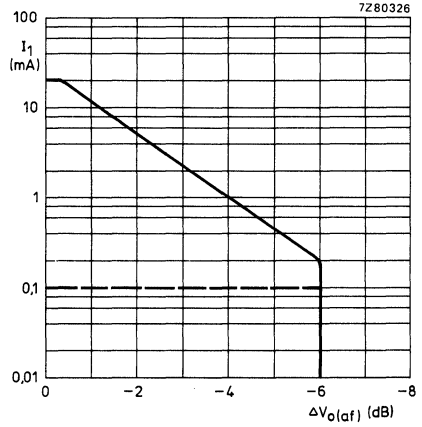


Fig. 14 Muting indicator current; V_P = 8,5 to 15 V; V_{PL} = 14 V.

——— R_{bias1} = 680 Ω
– – – – R_{bias1} = matched

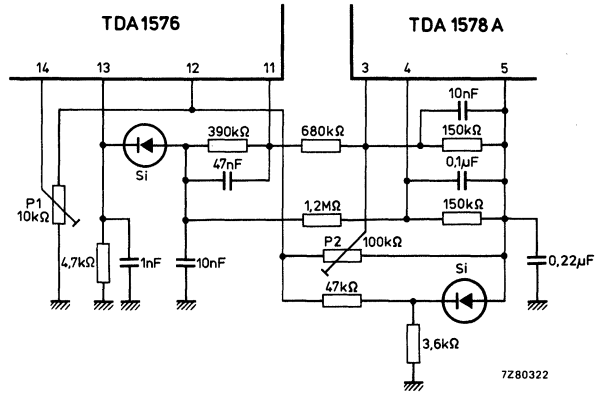


Fig. 15 Application information for external circuitry to provide external mono/stereo and muting control.

Adjustment recommendations:

at $V_{i(hf)}$ = 100 μV with P1 to α = 6 dB (channel separation),
at $V_{i(hf)}$ = 15 μV with P2 to $V_{o(af)}$ = −3 dB.

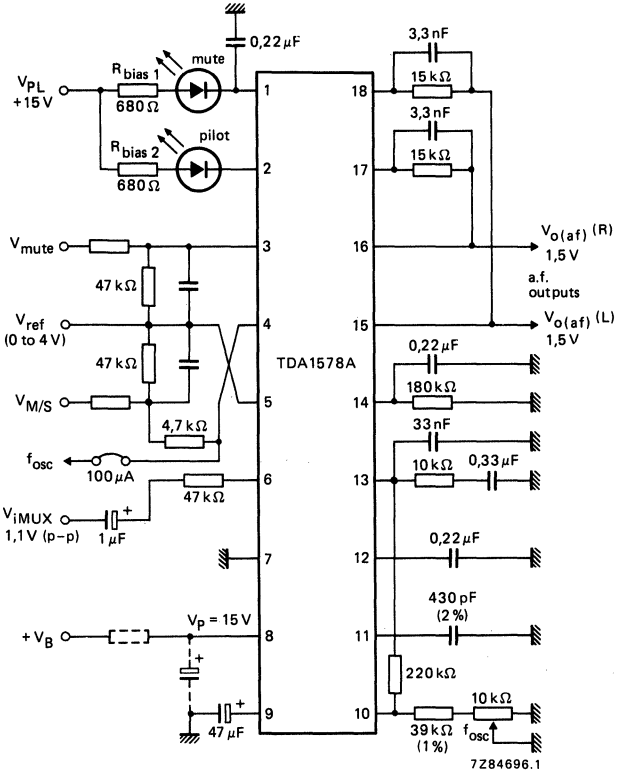


Fig. 16 Typical application circuit using TDA1578A for V_P = 15 V.

TV-Stereo Sound Decoder (Zenith Format) TDA3806

DESCRIPTION

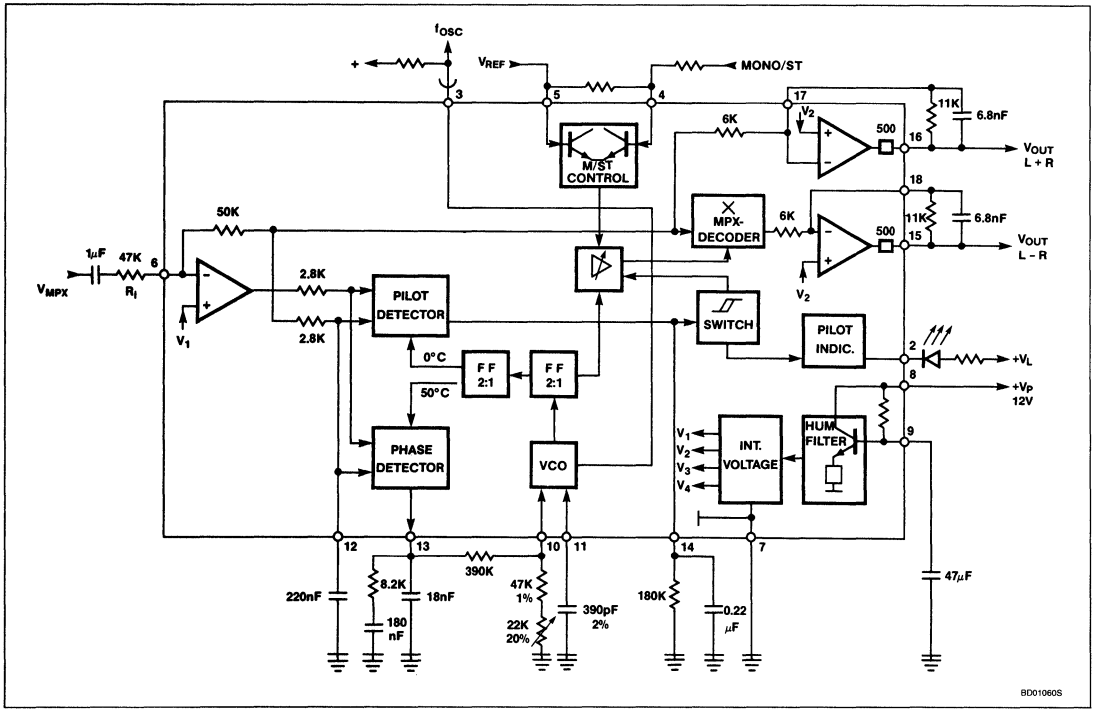
The TDA3806 is a monolithic integrated circuit for decoding TV stereo multiplex signal. The decoding signal is generated by a phase-locked loop system. The SAP and A.C.I. are suppressed by the internal circuitry; also this decoder has a main signal and a subsignal output. It is possible to apply a separate noise reduction system to the subsignal. The main signal and the noise reduced subsignal have to be combined at an external matrix to L resp. R.

FEATURES

- **Selectable gain by external resistors (separate for main and subsignal)**
- **DC input for smooth mono-stereo takeover control (without influencing the pilot indicator)**
- **Pilot dependent mono-stereo switch**
- **Pilot indicator driver**
- **PLL oscillator switch-off facility**
- **Buffered oscillator frequency measuring facility**
- **Internal suppression of SAP-distortion (5th harmonic of pilot)**
- **Suppression of A.C.I.-distortion (3rd harmonic of subcarrier, adjacent channel interference)**
- **Electronic hum filtering**

5

BLOCK DIAGRAM



REFERENCE DATA

PARAMETER	SYMBOL	LIMITS			UNIT
		Min	Nom	Max	
Supply voltage range, V_{8-7}		7.5	12	15	V
Supply current at $V_P = 12V$ (without indicator current), I_8		15	22	30	mA
Output voltage range, $V_{15/16-7}$, $(V_{8-7} - 1V)$		1		11	V
Voltage gain main signal, V_{out16}/V_{main}			19.5		dB
Harmonic distortion ($V_{OUT\ 15,16} = 1.25V$)	THD		0.1	0.5	%
SAP-suppression	SAP	60	75		dB
Nominal frequency	f_{osc}		63.4		kHz
Capture range	delta f/f	±2			%

Second Audio Program TDA3807

DESCRIPTION

The TDA3807 provides amplification, demodulation, indication and "no-signal" muting for processing the SAP facility of the multi-channel TV sound system.

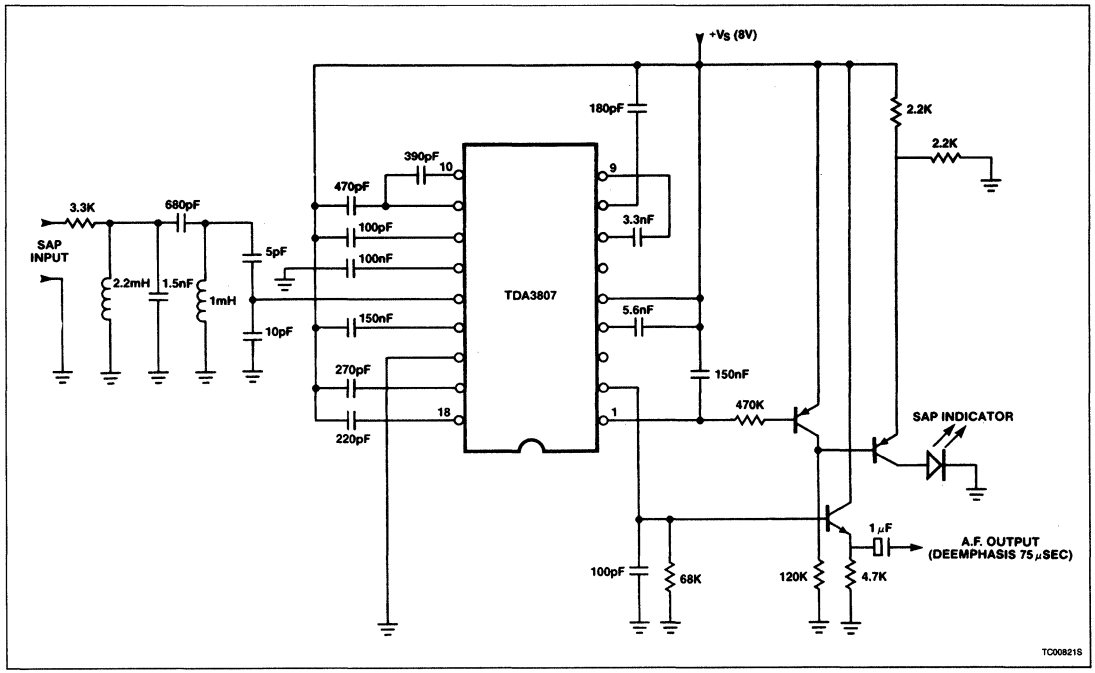
REFERENCE DATA

PARAMETER	SYMBOL	LIMITS			UNIT
		Min	Typical	Max	
Supply voltage	V_S		8		V
Supply current (indicator LED off)	I_S		13.5		mA
Input voltage for start of indication (f = 78.67kHz)	V_{IN}		12		μV
AF output voltage (AF V_{IN} = 2mV, f_{IN} = 78.67kHz f = ± 10kHz, f_{mod} = 1kHz)	V_{OUT}		630		mV
Output impedance			low ohmic (emitter follower)		
Signal to noise ratio at V_{IN} = 2mV	S/N		64		dB
AM supression at 2mV	α		52		dB
Total harmonic distortion AF f_{mod} = 1kHz, delta f = ± 10kHz	THD		1		%
AF-Bandwidth	B		9		kHz
Noise level (reference input signal = 2mV at V_{IN} < 1μV)	N		64		dB

5

Second Audio Program TDA3807

APPLICATIONS DIAGRAM



Spatial, Stereo, Pseudo-Stereo Processor TDA3810

DESCRIPTION

The TDA3810 is an integrated circuit which can provide three switched functions for radio and television equipment: spatial sound from a stereo source; stereo sound from a stereo source; pseudo-stereo sound from a mono source.

FEATURES

- **Three switched functions:**
  spatial
  stereo
  pseudo-stereo
- **Muting circuit prevents LED flickering**
- **LED driving outputs (pins 7 and 8)**
- **TTL compatible inputs for selecting operating mode**

ABSOLUTE MAXIMUM RATINGS

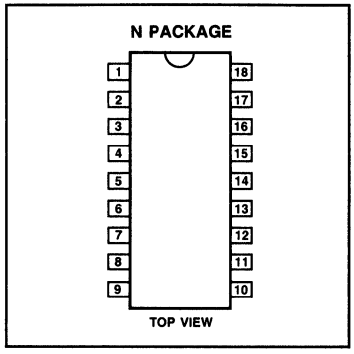
SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Supply voltage (pin 18)	18	V
I_{CC}	Supply current (pin 18)	12	mA
T_{STG}	Storage temperature range	−25 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C
Thermal Resistance			
$R_{th\ cr\text{-}a}$	From crystal to ambient	80	K/W

TRUTH TABLE

MODE	CONTROL INPUT STATE		LED SPATIAL	LED PSEUDO
	PIN 11	PIN 12	PIN 7	PIN 8
Mono pseudo-stereo	HIGH	LOW	Off	On
Spatial stereo	HIGH	HIGH	On	Off
Stereo	LOW	X	Off	Off

LOW = 0 to 0.8V (the less positive voltage)
HIGH = 2V to V_{CC} (the more positive voltage)
X = state is don't care

PIN CONFIGURATION



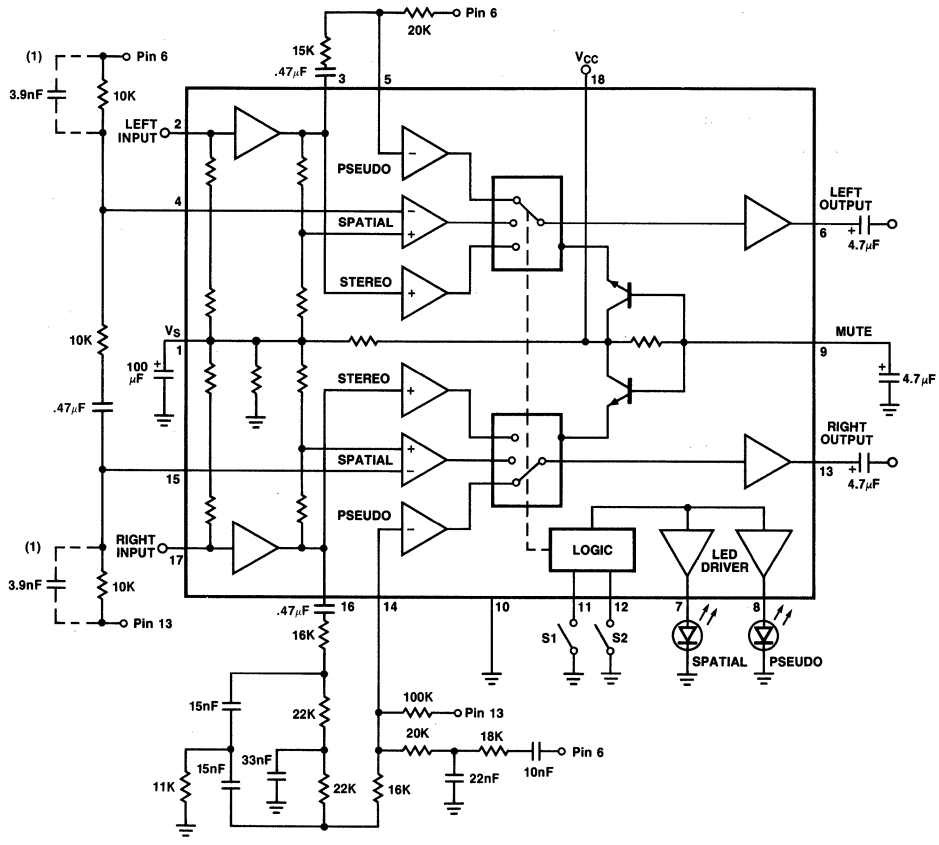
FUNCTIONAL PIN DESCRIPTION

PIN NO.	NAME AND FUNCTION
1	V_{REF}
2	Left channel input
3	Left channel buffer output
4	Left channel spatial feedback
5	Left channel pseudo feedback
6	Left channel output
7	Spatial indicator driver
8	Pseudo indicator driver
9	Mute
10	Ground
11	S1
12	S2
13	Right channel output
14	Right channel pseudo feedback
15	Right channel spatial feedback
16	Right channel buffer output
17	Right channel input
18	V_{DD}

5

Spatial, Stereo, Pseudo-Stereo Processor TDA3810

BLOCK DIAGRAM



(1) Recommended in spatial mode for correction of high frequency (optimal performance)

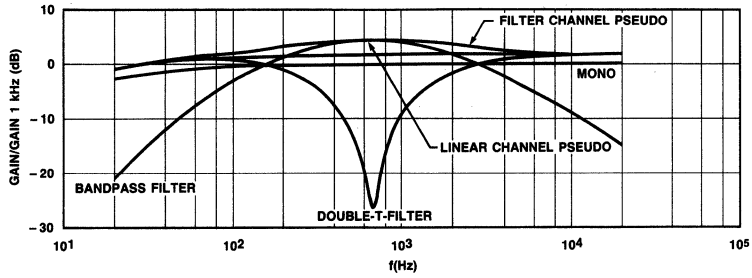
DC ELECTRICAL CHARACTERISTICS V_{CC} = 12V; T_A = 25°C; Test circuit Figure 1 stereo mode (pin 11 to ground) unless otherwise specified.

SYMBOL AND PARAMETER		TEST CONDITION	TDA3810			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range	(Pin 18)	4.5		16.5	V
V_{CC}	Supply current			6	12	mA
V_S	Reference voltage		5.3	6	6.7	V
$V_{i(rms)}$	Input voltage	(Pin 2 or 17) THD = 0.2%			2	V
R_i	Input resistance	(Pin 2 or 17)	50	75		kΩ
G_v	Voltage gain V_o/V_i			0		dB
α	Channel separation (R/L)		60	70		dB
THD	Total harmonic distortion	f = 40 to 16000 Hz; $V_{o(rms)}$ = 1V		0.1		%
RR	Power supply ripple rejection			50		dB
$V_{n(rms)}$	Noise output voltage	(Unweighted) left and right output)		10		μV
Spatial mode (Pins 11 and 12 HIGH)						
α	Antiphase crosstalk			50		%
G_v	Voltage gain		1.4	2.4	3.4	dB

PSEUDO-STEREO MODE The quality and strength of the pseudo-stereo effect is determined by external filter components.

SYMBOL AND PARAMETER		TEST CONDITION	TDA3810			UNIT
			Min	Typ	Max	
Control inputs		(Pins 11 and 12)				
R_i	Input resistance		70	120		kΩ
$-I_i$	Switching current			35	100	μA
LED drivers (Pins 7 and 8)						
$-I_o$	Output current for LED		10	12	15	mA
V_F	Forward voltage				6	V

Spatial, Stereo, Pseudo-Stereo Processor TDA3810



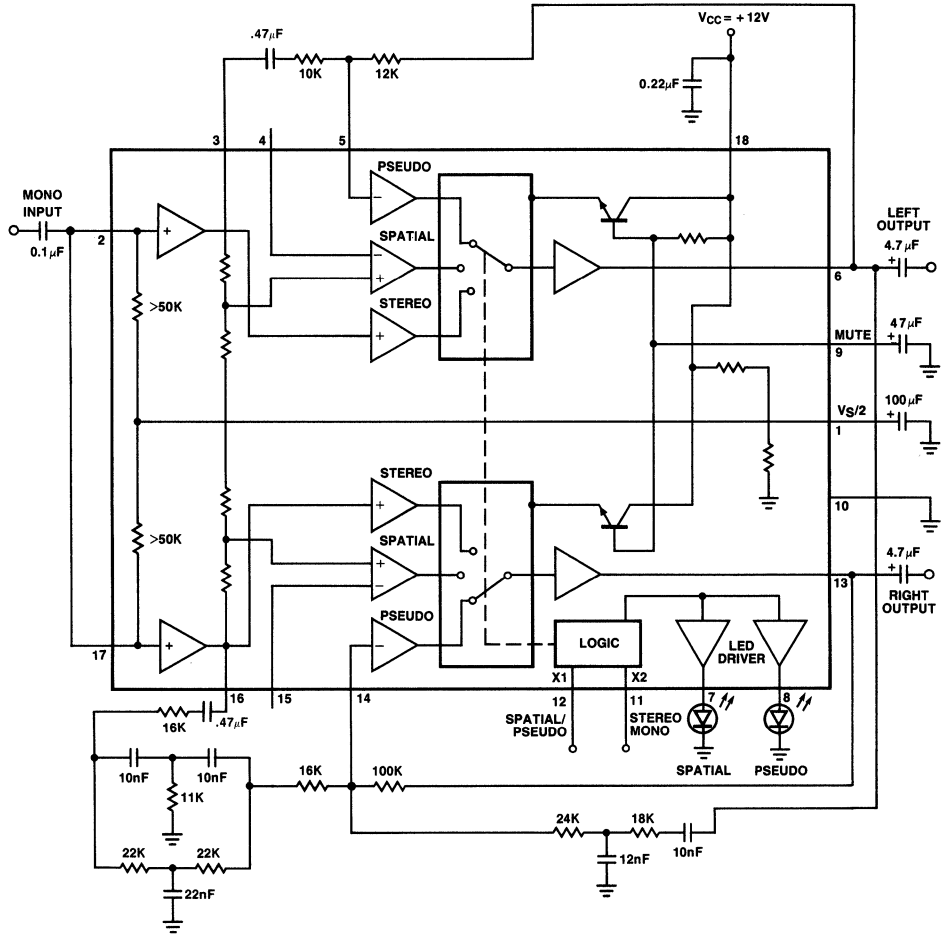


Figure 1. Pseudo Filter I

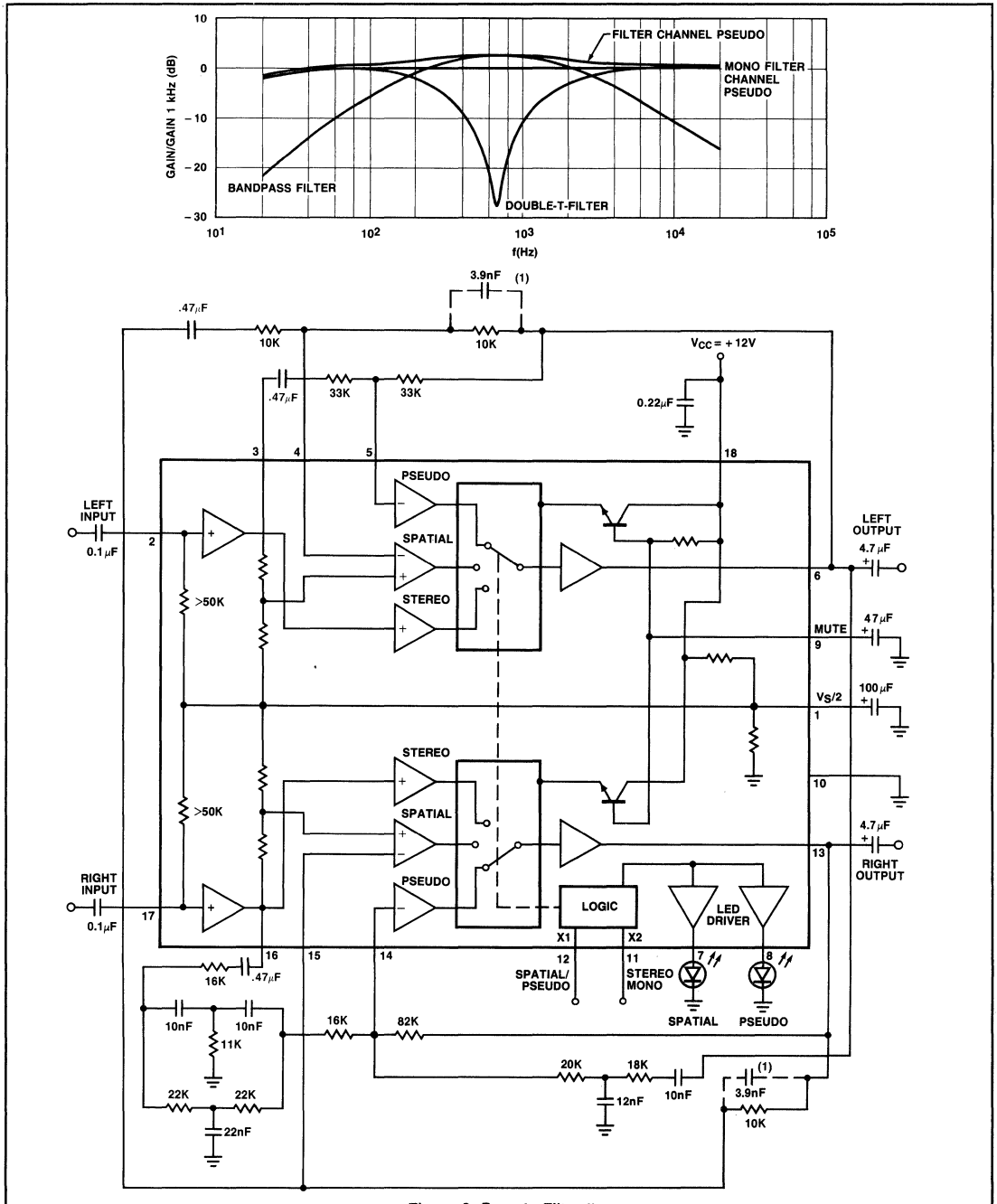


Figure 2. Pseudo Filter II

Spatial, Stereo, Pseudo-Stereo Processor TDA3810

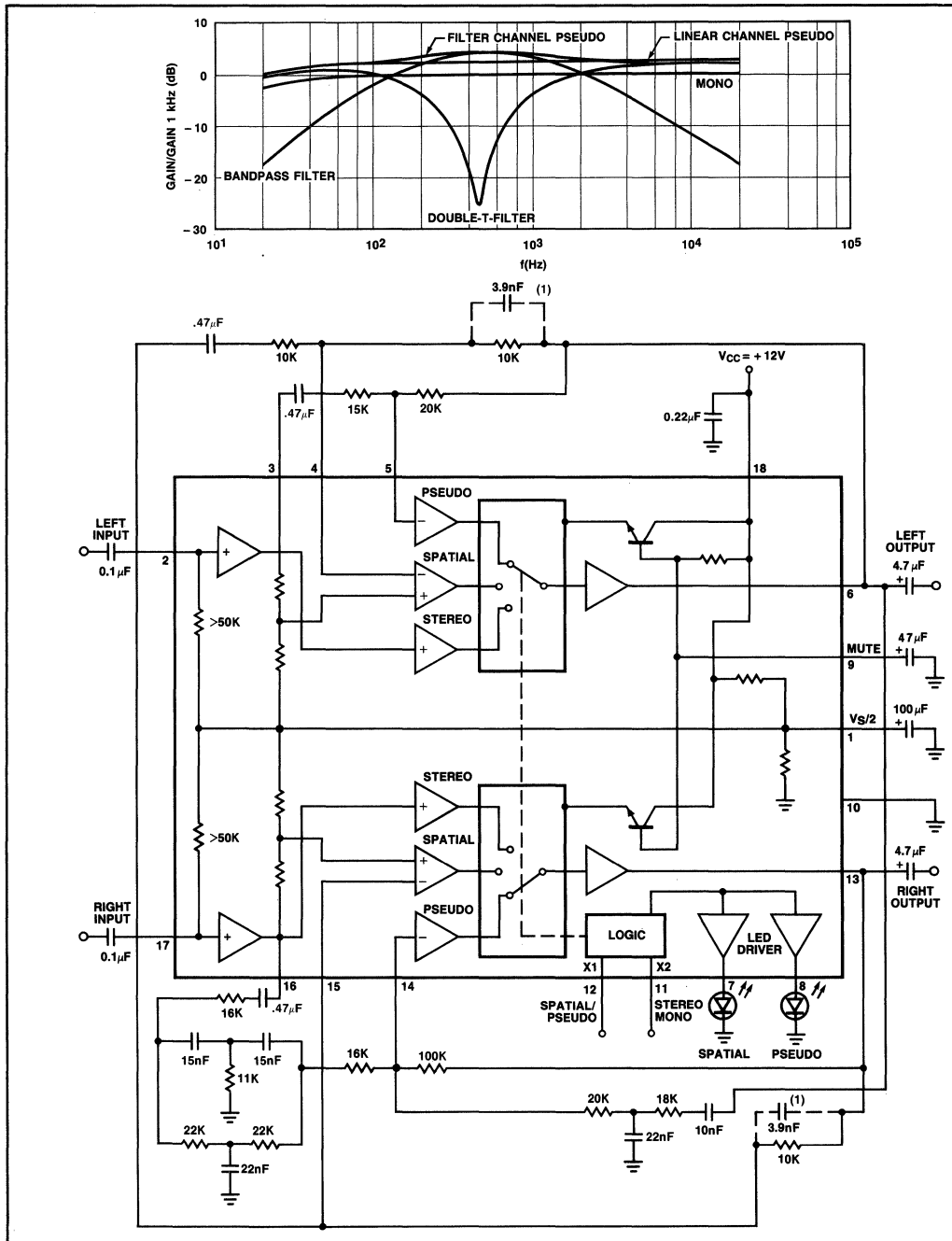


Figure 3. Pseudo Filter III

PLL Stereo Decoder TEA5580

The TEA5580 is a PLL stereo decoder. It is suitable for portable radios, radio recorders, medium-fi and car radio receivers. The circuit incorporates the following functions.

- **A voltage-controlled oscillator** (f = 228 kHz) from which the 19, 38, 57 and 114 kHz signals are obtained via I^2L logic.
- **A phase-locked-loop system** to lock the VCO to the 19 kHz pilot tone in the stereo signal. The phase detector in the loop system also suppresses phase distortion due to the 57 kHz pilot signal from VWF transmitters (traffic warning system in Germany).
- **A pilot presence detector and an automatic mono/stereo switch.**
- **Two demodulators**, one driven by the 38 kHz decoding signal for the stereo matrix, the second driven by a 114 kHz signal which suppresses the third harmonic of the multiplex signal (MUX). These prevent distortion caused by strong adjacent transmitters.
- **A matrix and two output buffers**, for the left and right output signals.
- **An input amplifier**, the gain of which can be adjusted by the external input resistor.
- **A pilot cancelling circuit**, for extra suppression of the pilot signal.
- **An SDS circuit (signal dependent stereo)** for a smooth changeover from stereo to mono on weak signals.
- **A driver output stage** for a stereo LED indicator.
- **A stabilizer**, for operation over a wide supply voltage range.

The stereo decoder is compensated for a typical i.f. filter with a roll-off frequency of 50 kHz (2 dB down at 38 kHz).

5

QUICK REFERENCE DATA

Applicable supply voltage range	V_S		3,6 to 16 V
Supply voltage (pin 9)	V_P	nom.	6 V
Ambient temperature	T_{amb}	typ.	25 °C
Total quiescent current	I_{tot}	typ.	10 mA
Measured at $V_{i(p-p)}$ = 1 V (MUX with 27 mV pilot)			
Overall gain	G_o	typ.	0 to 20 dB
Output channel unbalance	V_{1-5}/V_{2-5}	<	± 1 dB
Output voltage (r.m.s. value)	V_{1-5}/V_{2-5}	typ.	0,4 V
Total harmonic distortion (300 Hz to 20 kHz)	THD	typ.	0,2 %
Signal-to-noise ratio, DIN A-curve	S/N	typ.	80 dB
Channel separation	α	typ.	40 dB
Carrier suppression at: f = 19 kHz (adjusted)	α_{19}	typ.	50 dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

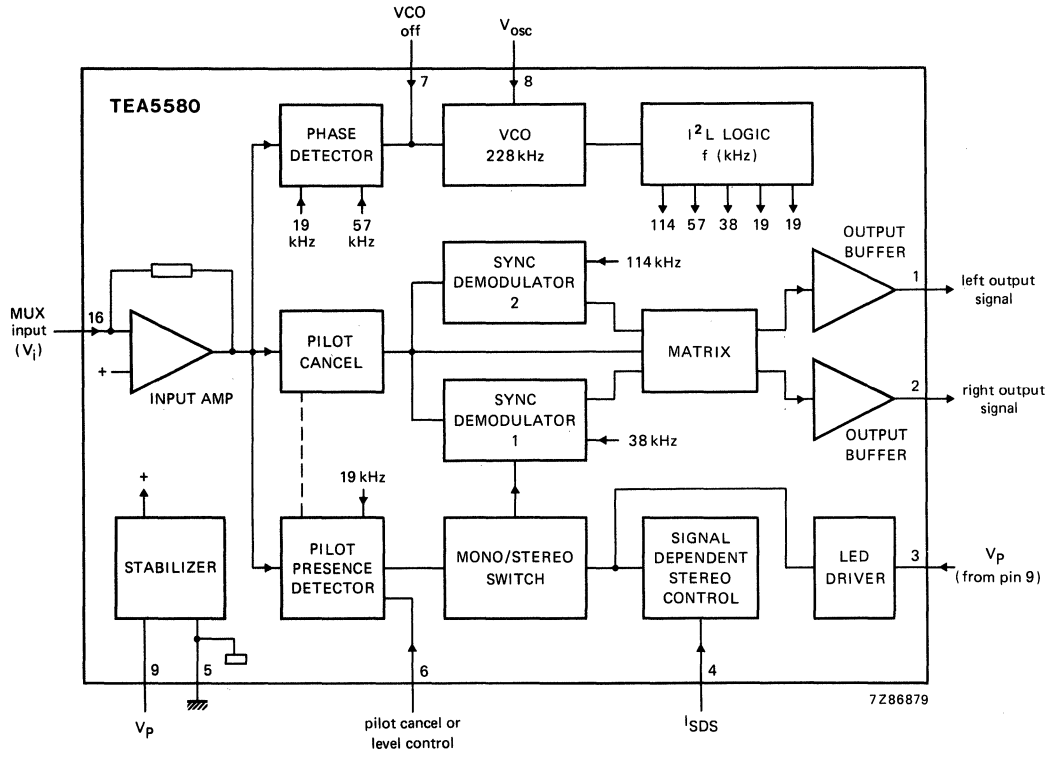


Fig. 1 Block diagram.

A.C. CHARACTERISTICS

Measured in circuit of Fig. 2 at V_P = 6 V, $V_{i(p-p)}$ = 1 V (MUX with 27 mV pilot)

Input impedance (external)	$\|Z_i\|$	typ.	47	kΩ
Output impedance (external)	$\|Z_o\|$	typ.	5,1	kΩ
Output voltage (r.m.s. value)	$V_{o(rms)}$	typ.	400	mV
Total harmonic distortion (300 Hz to 10 kHz) (mono, stereo and mono + pilot)	THD	typ.	0,2	%
Total harmonic distortion at $V_{o(rms)}$ = 0,6 V	THD	<	1	%
Signal-to-noise ratio (DIN A-curve)	S/N	typ.	80	dB
Channel separation (for L = 1 and R = 0)	α	typ.	40	dB
SDS control				
10 dB channel separation	I_4	typ.	50	μA
full stereo (channel separation ⩾ 26 dB)	I_4	>	100	μA
full mono (channel separation ⩽ 1 dB)	I_4	<	10	μA
Stereo/mono switch (for R2 = ▲kΩ)				
for switching to stereo	V_i	<	18	mV
for switching to mono	V_i	>	5	mV
		typ.	13	mV
hysteresis	ΔV_i	typ.	2,5	dB
VCO frequency (adjustable)	f_{VCO}	typ.	228	kHz
Capture range (deviation from 228 kHz centre frequency) V_{pilot} = 32 mV		typ.	3,5	%
Temperature coefficient (uncompensated)	TC	typ.	▲	kHz/K
VCO off switching voltage (pin 7)	V_{off}	>	3	V
Carrier suppression (adjusted by R2) at:				
f = 19 kHz	α_{19}	typ.	50	dB
f = 38 kHz	α_{38}	typ.	50	dB
f = 228 kHz	α_{228}	typ.	70	dB
ACI suppression at: *				
f = 114 kHz	α_{114}	typ.	80	dB
f = 190 kHz	α_{190}	typ.	60	dB
SCA suppression at f = 67 kHz	α_{67}	typ.	66	dB
VWF suppression**	α_{VWF}	typ.	70	dB
Ripple rejection at f = 100 Hz				
V_S = 3,6 V	RR	typ.	20	dB
V_S = 8 V	RR	typ.	26	dB

* ACI suppression: $\alpha_{114} = 20 \log \frac{V_o \text{ (at 1 kHz)}}{V_o \text{ (at 4 kHz)}}$.

90% S-signal (L = −R, f_m = 1 kHz); 9% pilot signal; 1% spurious signal (f = 110 kHz).

** VWF suppression: $\alpha_{VWF} = 20 \log \frac{V_o \text{ (at 1 kHz + 23 Hz)}}{V_o \text{ (at 1 kHz)}}$.

90% S-signal (L = −R, f_m = 1 kHz); 9% pilot signal; 5% VWF signal (f = 57 kHz, f_m = 23 Hz AM, m = 60%).

▲ Value to be established.

APPLICATION INFORMATION

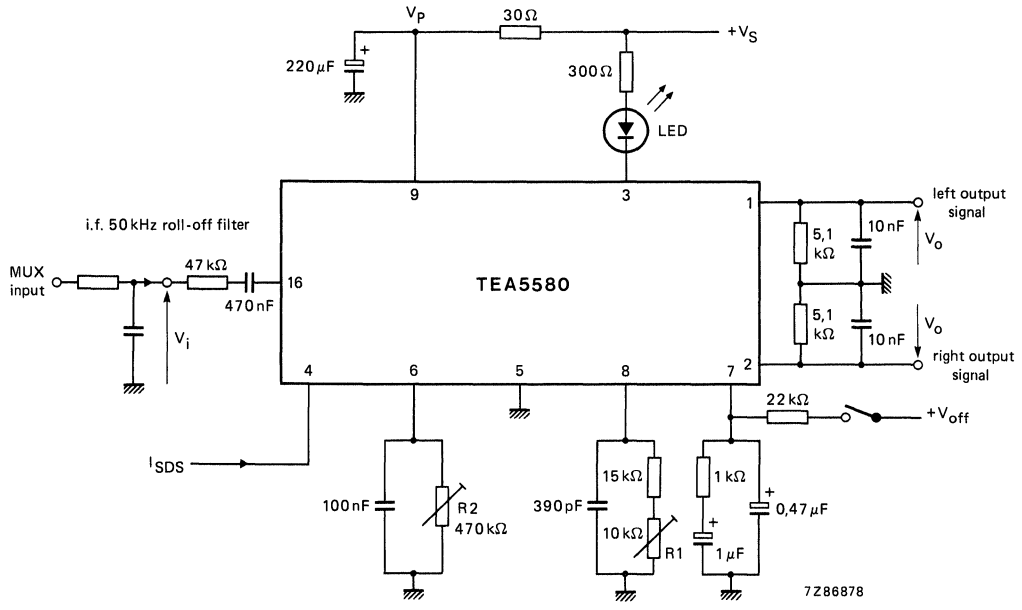


Fig. 2 Test and application diagram.

Notes

R1: VCO frequency adjustment; f = 228 kHz.
R2: pilot cancelling and pilot level.

PLL Radio Tuning Circuit SAA1057

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

5

QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}	3,6 to 12	V
	V_{CC2}	3,6 to 12	V
	V_{CC3}	V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ. 18	mA
	I_{CC3}	typ. 0,8	mA
Input frequency ranges			
at pin FAM	f_{FAM}	512 kHz to 32	MHz
at pin FFM	f_{FFM}	70 to 120	MHz
Maximum crystal input frequency	f_{XTAL}	> 4	MHz
Operating ambient temperature range	T_{amb}	−25 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

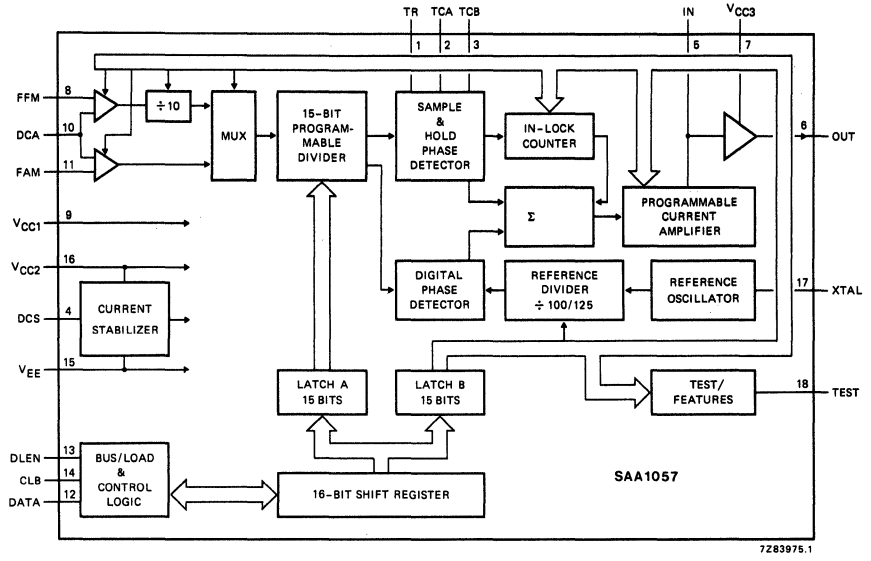


Fig. 1 Block diagram

GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.
The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM FM/AM selection; '1' = FM, '0' = AM

REFH reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)

CP3, CP2, CP1, CP0 control bits for the programmable current amplifier (see section Characteristics)

SB2 enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA load mode of latch A; '1' = synchronous, '0' = asynchronous

PDM1, PDM0 phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 test bit; must be programmed always '0'

T2 test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin

T1 test bit; must be programmed always '0'

T0 test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

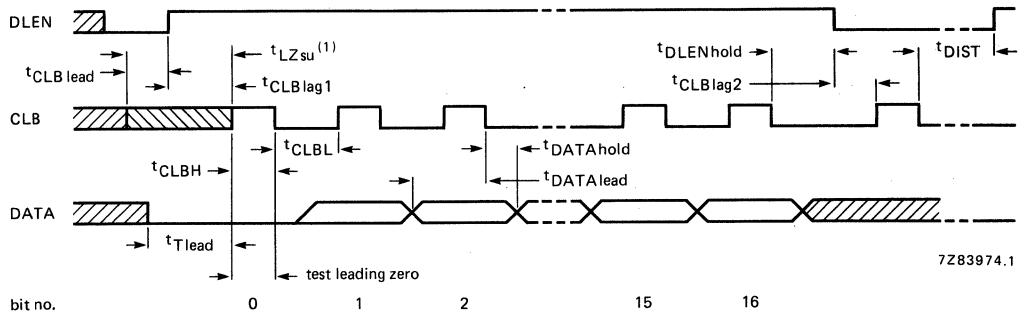


Fig. 2 BUS format.

(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I^2C bus is used for other devices on the same data and clock lines.

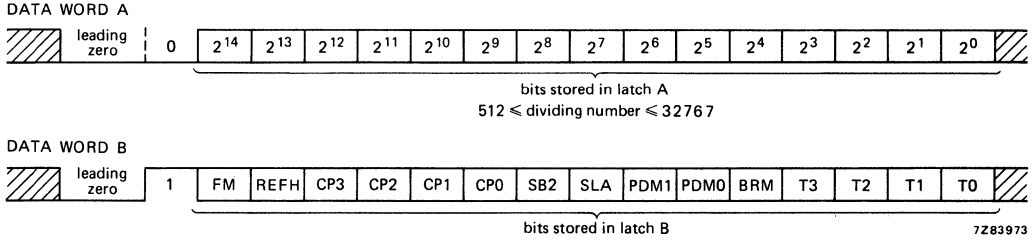


Fig. 3 Bit organization of data words A and B.

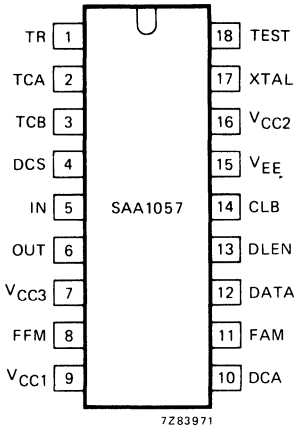


Fig. 4 Pinning diagram.

PINNING

1	TR	resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	BUS
13	DLEN	
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

5

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V_{CC1}; V_{CC2}	−0,3 to 13,2	V
Supply voltage; output amplifier	V_{CC3}	V_{CC2} to + 32	V
Total power dissipation	P_{tot}	max. 800	mW
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Storage temperature range	T_{stg}	−65 to + 150	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltages	V_{CC1}	3,6	5	12	V	
	V_{CC2}	3,6	5	12	V	
	V_{CC3}	V_{CC2}	–	31	V	
Supply currents*						
AM mode	I_{tot}	–	16	–	mA	$I_{tot} = I_{CC1} + I_{CC2}$ in-lock: BRM = '1'; PDM = '0'
FM mode	I_{tot}	–	20	–	mA	
	I_{CC3}	0,3	0,8	1,2	mA	I_{OUT} = 0
Operating ambient temperature	T_{amb}	−25	–	+ 80	°C	
RF inputs (FAM, FFM)						
AM input frequency	f_{FAM}	512 kHz	–	32	MHz	
FM input frequency	f_{FFM}	70	–	120	MHz	
Input voltage at FAM	V_i (rms)	30	–	500	mV	
Input voltage at FFM	V_i (rms)	10	–	500	mV	
Input resistance at FAM	R_i	–	2	–	kΩ	
Input resistance at FFM	R_i	–	135	–	Ω	
Input capacitance at FAM	C_i	–	3,5	–	pF	
Input capacitance at FFM	C_i	–	3	–	pF	
Voltage ratio allowed between selected and non-selected input	V_s/V_{ns}	–	−30	–	dB	
Crystal oscillator (XTAL)						see note 1
Maximum input frequency	f_{XTAL}	4	–	–	MHz	
Crystal series resistance	R_s	–	–	150	Ω	
BUS inputs (DLEN, CLB, DATA)						
Input voltage LOW	V_{IL}	0	–	0,8	V	
Input voltage HIGH	V_{IH}	2,4	–	V_{CC1}	V	
Input current LOW	$-I_{IL}$	–	–	10	μA	V_{IL} = 0,8 V
Input current HIGH	I_{IH}	–	–	10	μA	V_{IH} = 2,4 V

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
BUS inputs timing (DLEN, CLB, DATA)						see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	–	–	µs	
Lead time for DATA to the first CLB pulse	t_{Tlead}	0,5	–	–	µs	
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	–	–	µs	
CLB pulse width HIGH	t_{CLBH}	5	–	–	µs	
CLB pulse width LOW	t_{CLBL}	5	–	–	µs	
Set-up time for DATA to CLB	$t_{DATAlead}$	2	–	–	µs	
Hold time for DATA to CLB	$t_{DATAhold}$	0	–	–	µs	
Hold time for DLEN to CLB	$t_{DLENhold}$	2	–	–	µs	
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	–	–	µs	
Busy time from load pulse to next start of transmission	t_{DIST}	5	–	–	µs	next transmission after word 'B' to other device
Busy time asynchronous mode	t_{DIST}	0,3	–	–	ms	or next transmission to SAA1057 after word 'A' (see also note 5)
synchronous mode	t_{DIST}	1,3	–	–	ms	
Sample and hold circuit (TR, TCA, TCB)						see also notes 3; 4
Minimum output voltage	V_{TCA}, V_{TCB}	–	1,3	–	V	
Maximum output voltage	V_{TCA}, V_{TCB}	–	–	V_{CC2}–0,7	V	
Capacitance at TCA (external)	C_{TCA}	–	–	2,2	nF	REFH = '1'
	C_{TCA}	–	–	2,7	nF	REFH = '0'
Discharge time at TCA	t_{dis}	–	–	5	µs	REFH = '1'
	t_{dis}	–	–	6,25	µs	REFH = '0'
Resistance at TR	R_{TR}	100	–	–	Ω	external
Voltage at TR during discharge	V_{TR}	–	0,7	–	V	
Capacitance at TCB	C_{TCB}	–	–	10	nF	external
Bias current into TCA, TCB	I_{bias}	–	–	10	nA	in-lock

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CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

		CP3	CP2	CP1	CP0	symbol	min.	typ.	max.		conditions
Programmable current amplifier (PCA)											
Output current of the dig. phase detector						$\pm I_{dig}$	–	0,4	–	mA	
Current gain of PCA											
	P1	0	0	0	0	G_{P1}	–	0,023	–		$V_{CC2} \geqslant 5$ V (only for P1)
	P2	0	0	0	1	G_{P2}	–	0,07	–		
	P3	0	0	1	0	G_{P3}	–	0,23	–		
	P4	0	1	1	0	G_{P4}	–	0,7	–		
	P5	1	1	1	0	G_{P5}	–	2,3	–		
Ratio between the output current of S/H into PCA and the voltage on C_{TCB}						S_{TCB}	–	1,0	–	μA/V	
Offset voltage on TCB						ΔV_{TCB}	–	–	1	V	in-lock
Output amplifier (IN,OUT)											
Input voltage						V_{IN}	–	1,3	–	V	in-lock; equal to internal reference voltage
Output voltages											
minimum						V_{OUT}	–	–	0,5	V	$-I_{OUT}$ = 1 mA
maximum						V_{OUT}	$V_{CC3}-2$	–	–	V	I_{OUT} = 1 mA
maximum						V_{OUT}	$V_{CC3}-1$	–	–	V	I_{OUT} = 0,1 mA
Maximum output current						$\pm I_{OUT}$	5	–	–	mA	V_{OUT} = ½ V_{CC3}
Test output (TEST)*											
Output voltage LOW						V_{TL}	–	–	0,5	V	
Output voltage HIGH						V_{TH}	–	–	12	V	
Output current OFF						I_{Toff}	–	–	10	μA	V_{TH}
Output current ON						I_{Ton}	150	–	–	μA	V_{TL}
Ripple rejection**											
at f_{ripple} = 100 Hz											
$\Delta V_{CC1}/\Delta V_{OUT}$							–	77	–	dB	
$\Delta V_{CC2}/\Delta V_{OUT}$							–	70	–	dB	
$\Delta V_{CC3}/\Delta V_{OUT}$							–	60	–	dB	$V_{OUT} \leqslant V_{CC3}-3$ V

* Open collector output.

** Measured in Fig. 6.

NOTES

1. Pin 17 (XTAL) can also be used as input for an external clock.
   The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

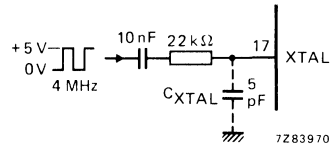


Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ V_{CC2}+0,3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ V_{CC2}+0,3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057.
   When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5 μs will be sufficient.

5

APPLICATION INFORMATION

Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/asynchronous operation

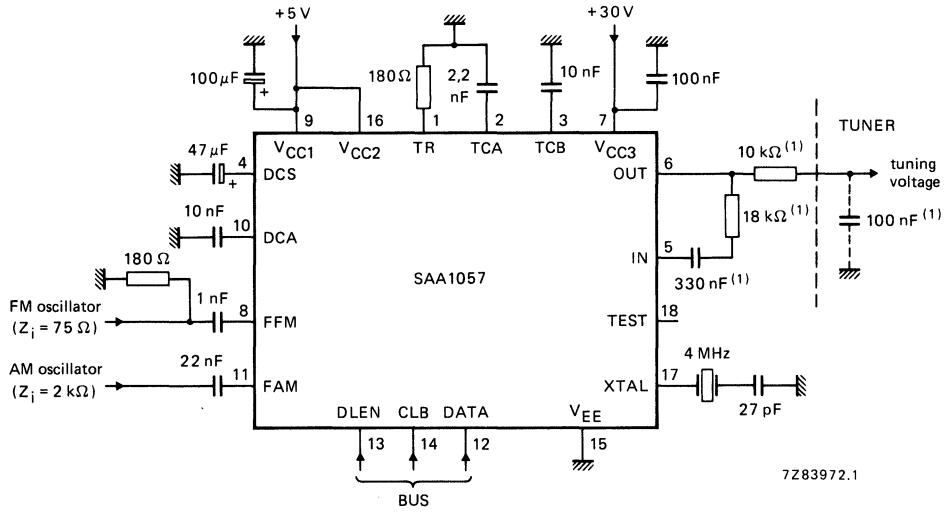
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced. ←



(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057PLL frequency synthesizer module.

Balanced Modulator/Demodulator TDA0820T

The TDA0820T is a monolithic integrated circuit for use at frequencies up to 650 MHz.
Typical applications are:

- modulator
- mixer
- switch/chopper
- a.m. synchronous demodulator
- f.m. quadrature demodulator
- phase comparator
- differential amplifier

The circuit is arranged to offer very flexible circuit design possibilities. The excellent matching and temperature tracking of the transistors in the circuit allow the use of circuit techniques which are not available when using discrete devices.

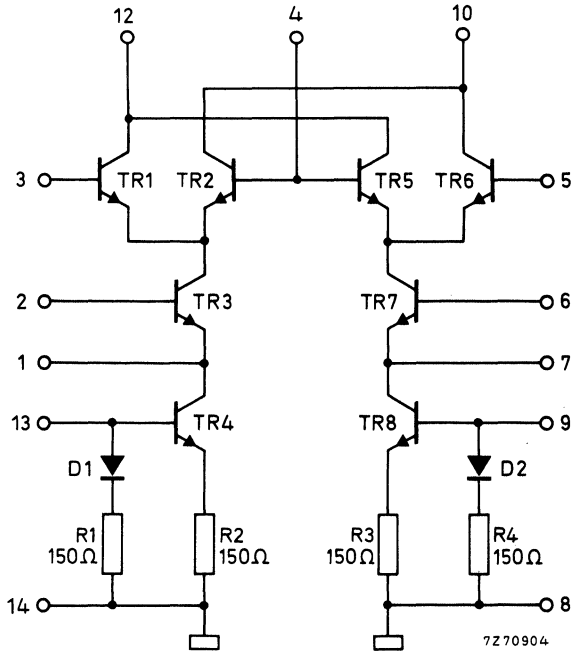


Fig. 1 Circuit diagram.

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO-14; SOT-108A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{10-8}; V_{10-14}; V_{12-8}; V_{12-14}	0 to 13,2	V
Voltages (each transistor)			
Collector-substrate voltage (open base) and emitter)	V_{CSO}	max. 15	V
Collector-base voltage (open emitter)	V_{CBO}	max. 12	V
Collector-emitter voltage (open base)	V_{CEO}	max. 10	V
Emitter-base voltage (open collector)	V_{EBO}	max. 5	V
Currents (each transistor)			
Emitter current	I_E	max. 10	mA
Base current	I_B	max. 10	mA
Total power dissipation when mounted on a printed-circuit board	P_{tot}	max. 250	mW
Storage temperature	T_{stg}	−55 to + 125	°C
Operating ambient temperature	T_{amb}	0 to + 70	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	= 220	K/W

CHARACTERISTICS

$V_{10-8} = V_{10-14} = V_{12-8} = V_{12-14} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 2

Supply current	$I_{10} + I_{12}$	typ. 2,5 < 3	mA mA
Input signals			
carrier signal (r.m.s. value)	$V_{3-4(rms)}$; $V_{5-4(rms)}$	< 100	mV
video signal; negative modulated (peak-to-peak value)	$V_{6-2(p-p)}$	< 1,4	V
Output signal at top sync over 75 Ω (peak-to-peak value)	$V_{10-12(p-p)}$	> 22	mV
Carrier suppression in balanced condition	V_{10-12}	> 38	dB
Differential phase		< 6°	
Differential gain		< 15	%
Distortion of video signal		< −38	dB

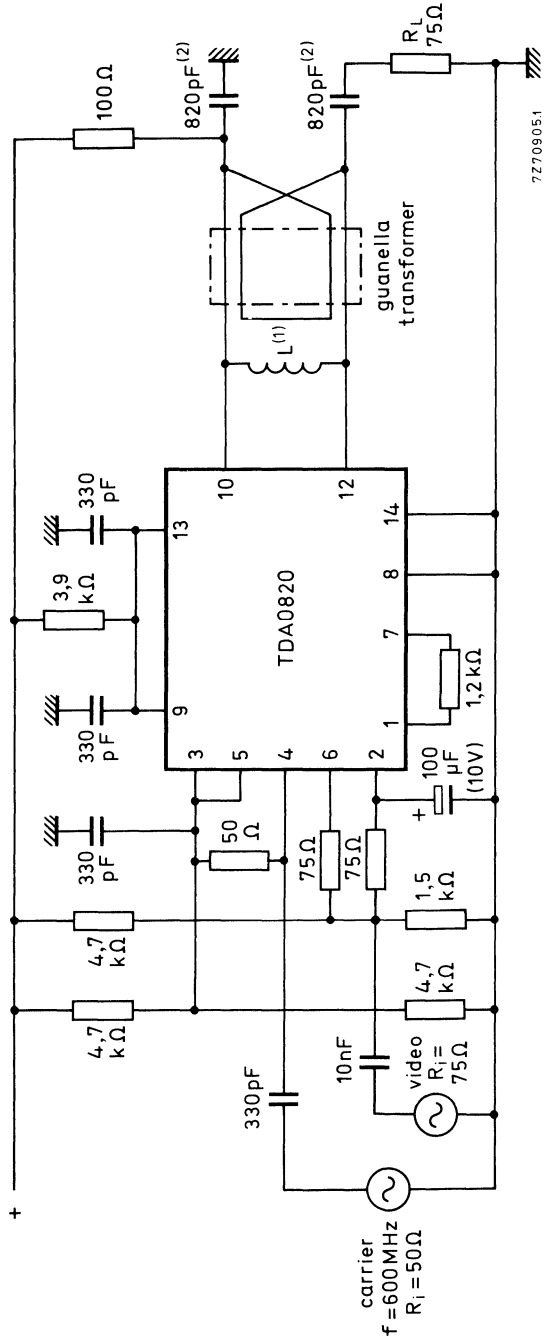


Fig. 2 Test circuit.

(1) L = air coil; 3 turns; ϕ 3 mm.
(2) U.H.F. decoupling capacitor 2212 669 98003.

5

AM Receiver Circuit TDA1072A

GENERAL DESCRIPTION

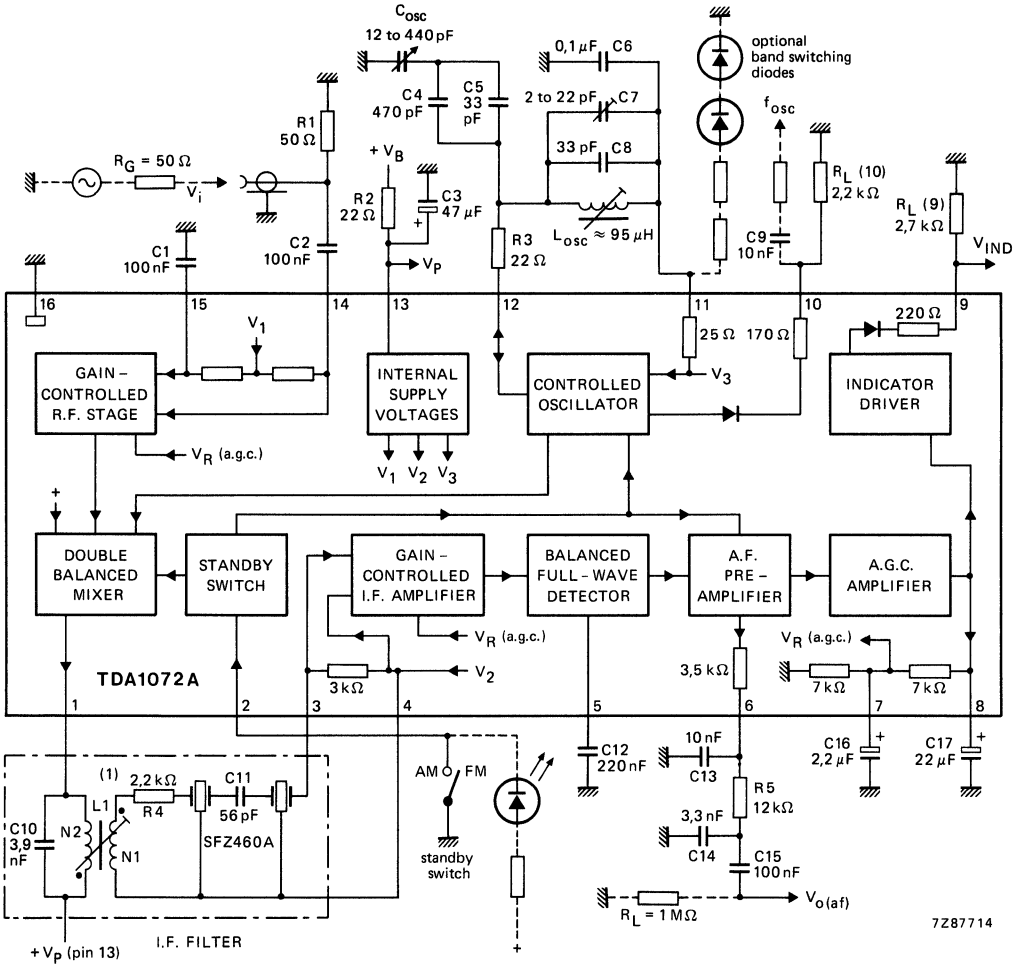
The TDA1072A integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle r.f. signals up to 500 mV. R.F. radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the i.f. amplifier.

Features

- Inputs protected against damage by static discharge
- Gain-controlled r.f. stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled i.f. stage with wide a.g.c. range
- Full-wave, balanced envelope detector
- Internal generation of a.g.c. voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- A.F. preamplifier with possibilities for simple a.f. filtering
- Electronic standby switch

QUICK REFERENCE DATA

Supply voltage range	V_P		7,5 to 18	V
Supply current range	I_P		15 to 30	mA
R.F. input voltage for S + N/N = 6 dB at m = 30%	V_i	typ.	1,5	μV
R.F. input voltage for 3% total harmonic distortion (THD) at m = 80%	V_i	typ.	500	mV
A.F. output voltage with V_i = 2 mV; f_i = 1 MHz; m = 30% and f_m = 400 Hz	$V_{o(af)}$	typ.	310	mV
A.G.C. range: change of V_i for 1 dB change of $V_{o(af)}$		typ.	86	dB
Field strength indicator voltage at V_i = 500 mV; $R_{L(9)}$ = 2,7 kΩ	V_{IND}	typ.	2,8	V



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_o = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_I = 4,8 kΩ.

Fig. 1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled r.f. stage and mixer

The differential amplifier in the r.f. stage employs an a.g.c. negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by a.g.c. delays at the various signal stages. Large signals are handled with low distortion and the S/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the i.f. output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{11\text{-}16}$. An extra buffered oscillator output (pin 10) is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

Gain-controlled i.f. amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the a.g.c. negative feedback network.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual i.f. carrier is blocked from the signal path by an internal low-pass filter.

A.F. preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for a.f. filtering.

A.G.C. amplifier

The a.g.c. amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the a.g.c. voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast a.g.c. settling time which is advantageous for electronic search tuning. The a.g.c. settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The a.g.c. voltage is fed to the r.f. and i.f. stages via suitable a.g.c. delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(9)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and a.f. preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage	$V_P = V_{13-16}$	max.	20	V
Total power dissipation	P_{tot}	max.	875	mW
Input voltage	$\|V_{14-15}\|$	max.	12	V
	$-V_{14-16}$, $-V_{15-16}$	max.	0,6	V
	V_{14-16}, V_{15-16}	max.	V_P	V
Input current	$\|I_{14}\|$, $\|I_{15}\|$	max.	200	mA
Operating ambient temperature range	T_{amb}	−40 to	+80	°C
Storage temperature range	T_{stg}	−55 to	+150	°C
Junction temperature	T_j	max.	+125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	80	K/W

5

DEVICE CHARACTERISTICS

$V_P = V_{13-16} = 8{,}5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{if} = 460$ kHz; measured in test circuit of Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_{13-16}$	7,5	8,5	18	V
Supply current	$I_P = I_{13}$	15	23	30	mA
R.F. stage and mixer					
Input voltage (d.c. value)	V_{14-16}, V_{15-16}	–	$V_P/2$	–	V
R.F. input impedance at $V_i < 300\ \mu V$	R_{14-16}, R_{15-16}	–	5,5	–	kΩ
	C_{14-16}, C_{15-16}	–	25	–	pF
R.F. input impedance at $V_i > 10$ mV	R_{14-16}, R_{15-16}	–	8	–	kΩ
	C_{14-16}, C_{15-16}	–	22	–	pF
I.F. output impedance	R_{1-16}	500	–	–	kΩ
	C_{1-16}	–	6	–	pF
Conversion transconductance before start of a.g.c.	I_1/V_i	–	6,5	–	mA/V
Maximum i.f. output voltage, inductive coupling to pin 1	$V_{1-13(p-p)}$	–	5	–	V
D.C. value of output current (pin 1) at $V_i = 0$ V	I_1	–	1,2	–	mA
A.G.C. range of input stage		–	30	–	dB
R.F. signal handling capability: input voltage for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0,6	–	60	MHz
Oscillator amplitude (pins 11 to 12)	$V_{11\text{-}12}$	–	130	150	mV
External load impedance	$R_{12\text{-}11(ext)}$	0,5	–	200	kΩ
External load impedance for no oscillation	$R_{12\text{-}11(ext)}$	–	–	60	Ω
Ripple rejection at $V_{P(rms)}$ = 100 mV; f_P = 100 Hz ($RR = 20 \log [V_{13\text{-}16}/V_{11\text{-}16}]$)	RR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE})	$V_{11\text{-}16}$	–	4,2	–	V
D.C. output current (for switching diodes)	$-I_{11}$	0	–	20	mA
Change of output voltage at ΔI_{11} = 20 mA (switch to maximum load)	$\Delta V_{11\text{-}16}$	–	0,5	–	V
Buffered oscillator output					
D.C. output voltage	$V_{10\text{-}16}$	–	0,7	–	V
Output signal amplitude	$V_{10\text{-}16(p\text{-}p)}$	–	320	–	mV
Output impedance	R_{10}	–	170	–	Ω
Output current	$-I_{10(peak)}$	–	–	3	mA
I.F., a.g.c. and a.f. stages					
D.C. input voltage	$V_{3\text{-}16}$, $V_{4\text{-}16}$	–	2,0	–	V
I.F. input impedance	$R_{3\text{-}4}$	2,4	3	3,9	kΩ
	$C_{3\text{-}4}$	–	7	–	pF
I.F. input voltage for THD = 3% at m = 80%	$V_{3\text{-}4}$	–	90	–	mV
Voltage gain before start of a.g.c.	$V_{3\text{-}4}/V_{6\text{-}16}$	–	68	–	dB
A.G.C. range of i.f. stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(af)}$; $V_{3\text{-}4(ref)}$ = 75 mV	$\Delta V_{3\text{-}4}$	–	55	–	dB
A.F. output voltage at $V_{3\text{-}4(if)}$ = 50 μV	$V_{o(af)}$	–	130	–	mV
A.F. output voltage at $V_{3\text{-}4(if)}$ = 1 mV	$V_{o(af)}$	–	310	–	mV
A.F. output impedance (pin 6)	$\lvert Z_o \rvert$	–	3,5	–	kΩ
Indicator driver					
Output voltage at V_i = 0 mV; $R_{L(9)}$ = 2,7 kΩ	$V_{9\text{-}16}$	–	20	150	mV
Output voltage at V_i = 500 mV; $R_{L(9)}$ = 2,7 kΩ	$V_{9\text{-}16}$	2,5	2,8	3,1	V
Load resistance	$R_{L(9)}$	1,5	–	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Standby switch					
Switching threshold at V_P = 7,5 to 18 V; T_{amb} = −40 to + 80 °C					
on-voltage	V_{2-16}	0	–	2,0	V
off-voltage	V_{2-16}	3,5	–	20	V
on-current at V_{2-16} = 0 V	$-I_2$	–	–	200	μA
off-current at V_{2-16} = 20 V	$\|I_2\|$	–	–	10	μA

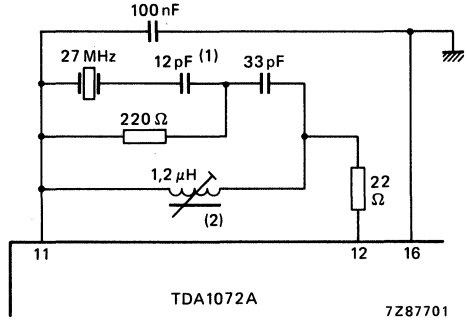
OPERATING CHARACTERISTICS

V_P = 8,5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity					
R.F. input required for S + N/N = 6 dB	V_i	–	1,5	–	μV
R.F. input required for S + N/N = 26 dB	V_i	–	15	–	μV
R.F. input required for S + N/N = 46 dB	V_i	–	150	–	μV
R.F. input at start of a.g.c.	V_i	–	30	–	μV
R.F. large signal handling					
R.F. input at THD = 3%; m = 80%	V_i	–	500	–	mV
R.F. input at THD = 3%; m = 30%	V_i	–	700	–	mV
R.F. input at THD = 10%; m = 30%	V_i	–	900	–	mV
A.G.C. range					
Change of V_i for 1 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	91	–	dB
Output signal					
A.F. output voltage at V_i = 4 μV; m = 80%	$V_{o(af)}$	–	130	–	mV
A.F. output voltage at V_i = 1 mV	$V_{o(af)}$	240	310	390	mV
THD at V_i = 1 mV; m = 80%	d_{tot}	–	0,5	–	%
THD at V_i = 500 mV; m = 30%	d_{tot}	–	1	–	%
Signal-to-noise ratio at V_i = 100 mV	(S + N)/N	–	58	–	dB
Ripple rejection at V_i = 2 mV; $V_{P(rms)}$ = 100 mV; f_P = 100 Hz ($RR = 20 \log [V_P/V_{o(af)}]$)	RR	–	38	–	dB

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of i.f. whistles at V_i = 15 μV; m = 0% related to a.f. signal of m = 30%					
at $f_i \approx 2 \times f_{if}$	α_{2if}	–	37	–	dB
at $f_i \approx 3 \times f_{if}$	α_{3if}	–	44	–	dB
I.F. suppression at r.f. input					
for symmetrical input	α_{if}	–	40	–	dB
for asymmetrical input	α_{if}	–	40	–	dB
Residual oscillator signal at mixer output					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1,1	–	μA

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0,1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; Q_0 = 80.

Fig. 2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

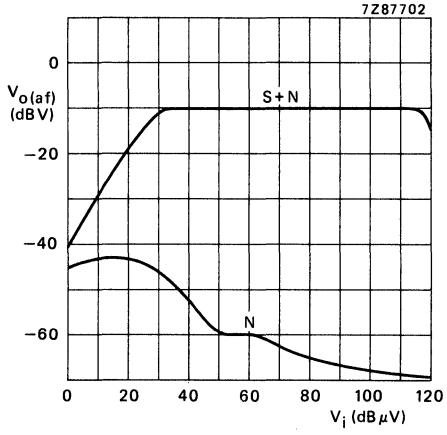


Fig. 3 A.F. output as a function of r.f. input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

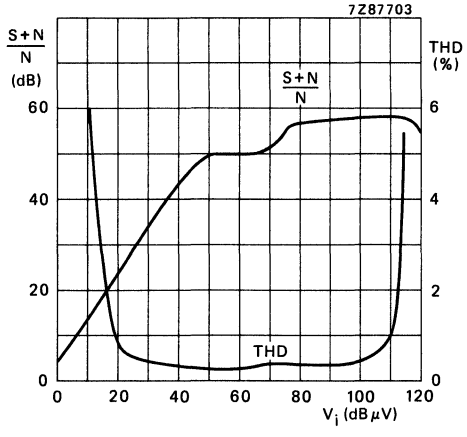


Fig. 4 Total harmonic distortion and (S + N)/N as functions of r.f. input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

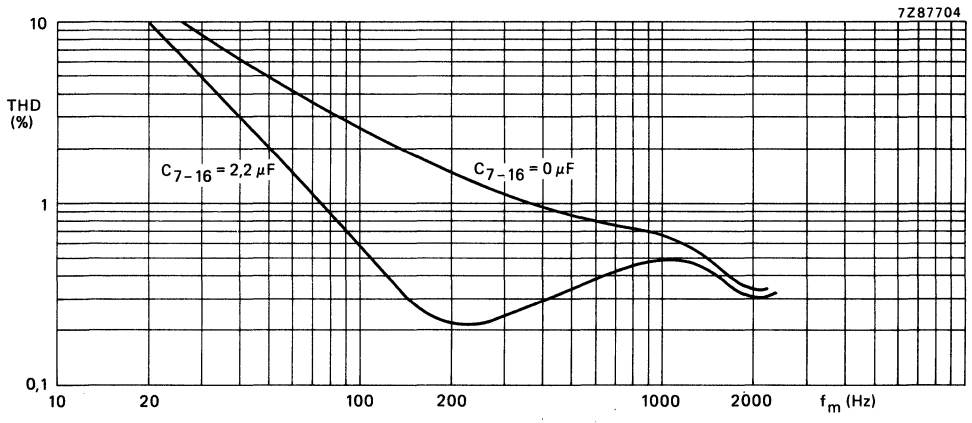


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7-16(ext)}$ = 0 μF and 2,2 μF.

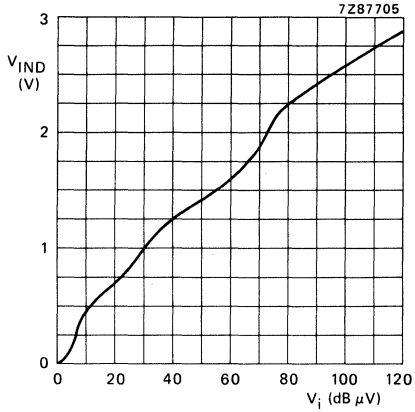


Fig. 6 Indicator driver voltage as a function of r.f. input in the circuit of Fig. 1.

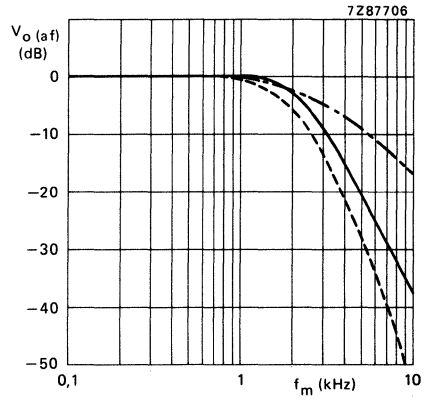


Fig. 7 Typical frequency response curves from Fig. 1 showing the effect of filtering as follows:
——— with i.f. filter;
— · — · — · — · with a.f. filter;
— — — — — with i.f. and a.f. filters.

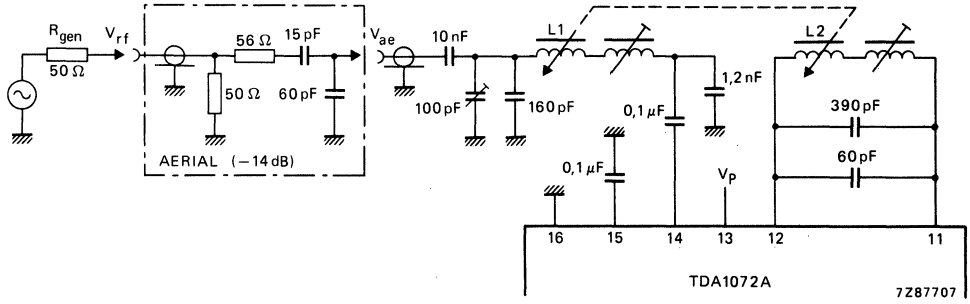


Fig. 8 Car radio application with inductive tuning.

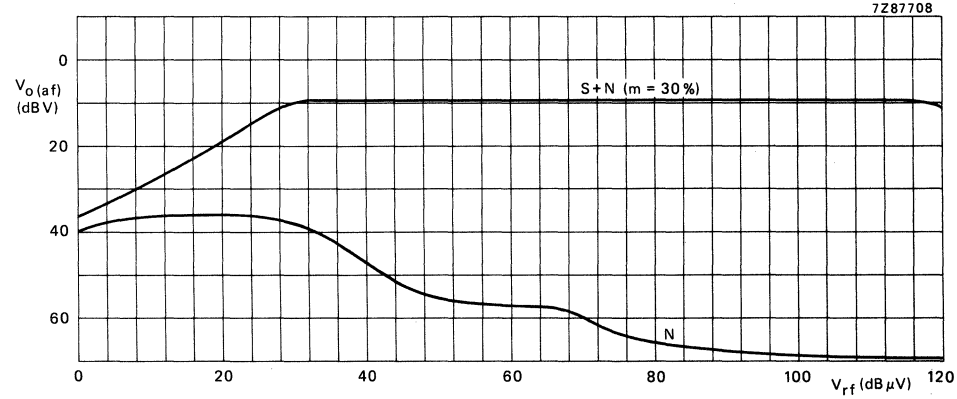


Fig. 9 A.F. output as a function of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

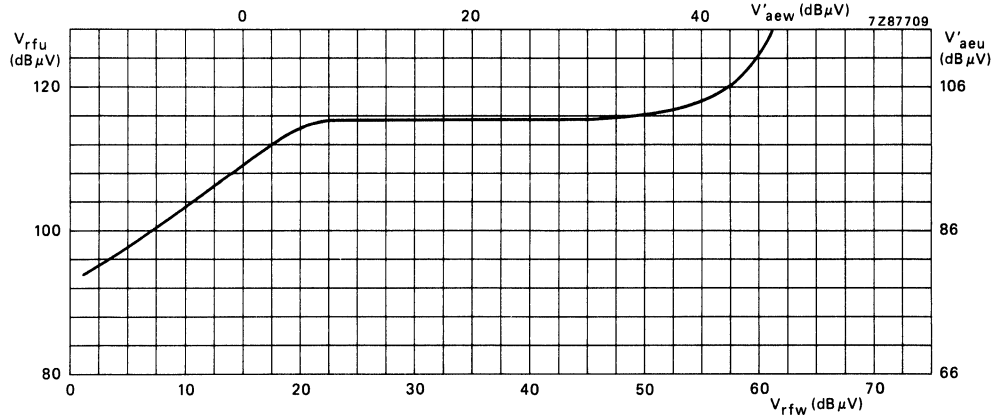


Fig. 10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig. 8 with the input circuit as shown in Fig. 11. Curve is for Wanted $V_{o(af)}$/Unwanted $V_{o(af)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

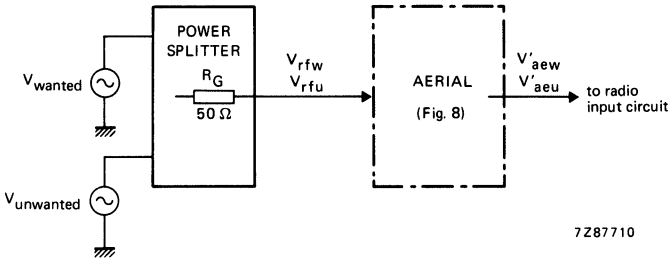


Fig. 11 Input circuit to show cross-modulation suppression (see Fig. 10).

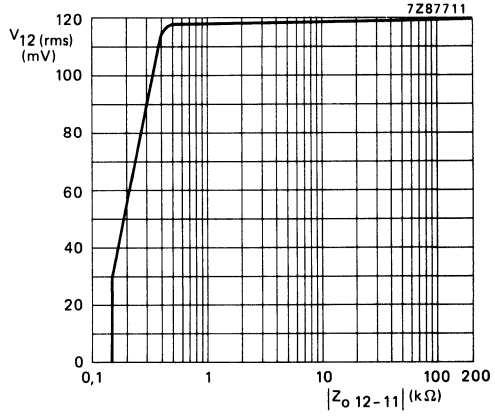


Fig. 12 Oscillator amplitude as a function of pin 11, 12 impedance in the circuit of Fig. 8.

5

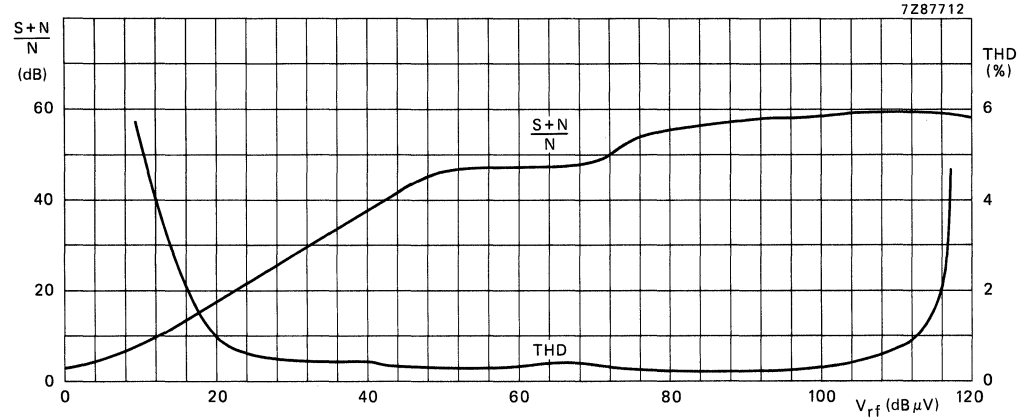


Fig. 13 Total harmonic distortion and (S + N)/N as functions of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

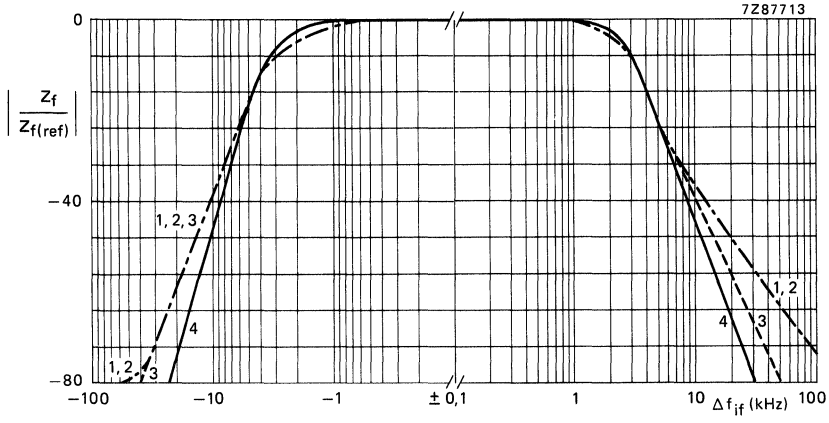


Fig. 14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig. 15; centre frequency = 455 kHz.

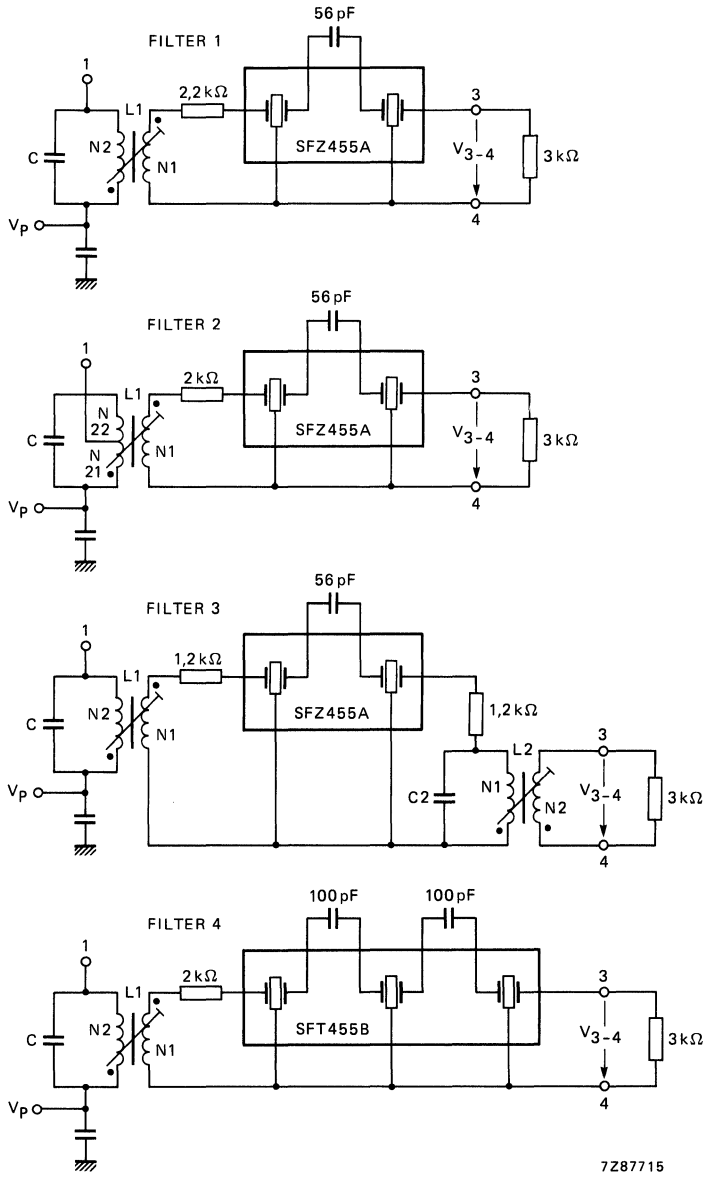
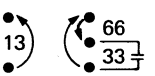
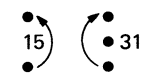
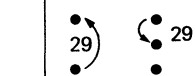


Fig. 15 I.F. filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

Table 1 Data for I.F. filters shown in Fig. 15. Criterium for adjustment is Z_F = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). See also Fig. 14.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0,09	0,08	0,09	0,08	0,09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings						
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4,2	4,2	4,2		4,5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4,8	3,8	4,2		4,8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0,70	0,67	0,68		0,68	kΩ
Bandwidth (−3 dB)	3,6	3,8	3,6		4,0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

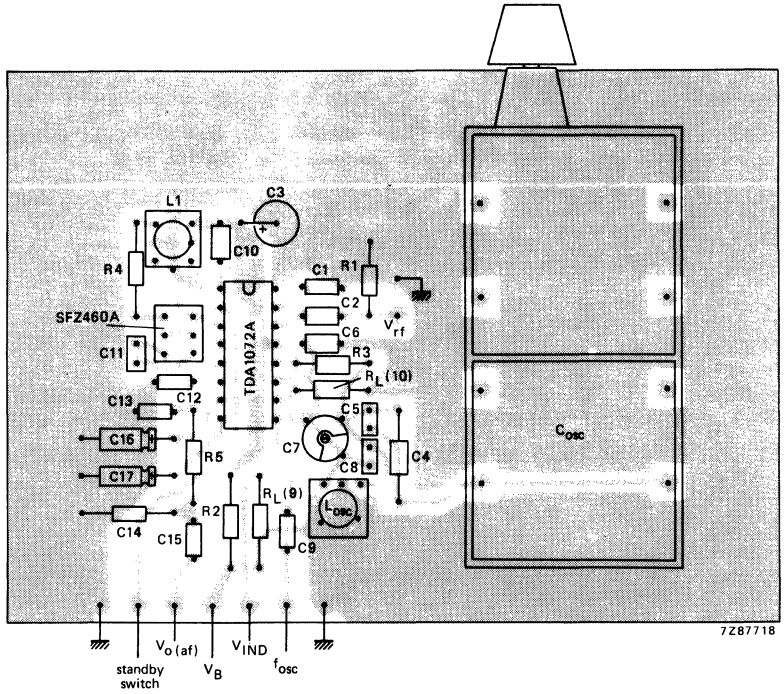


Fig. 16 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 1.

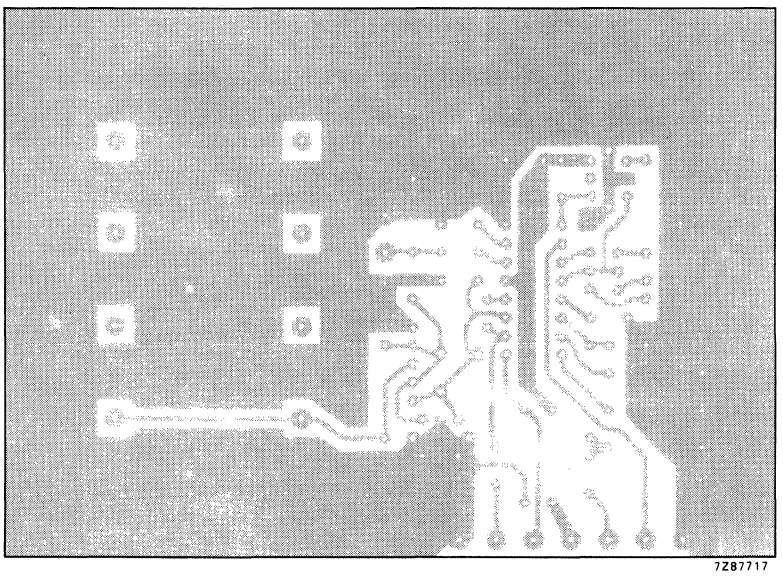
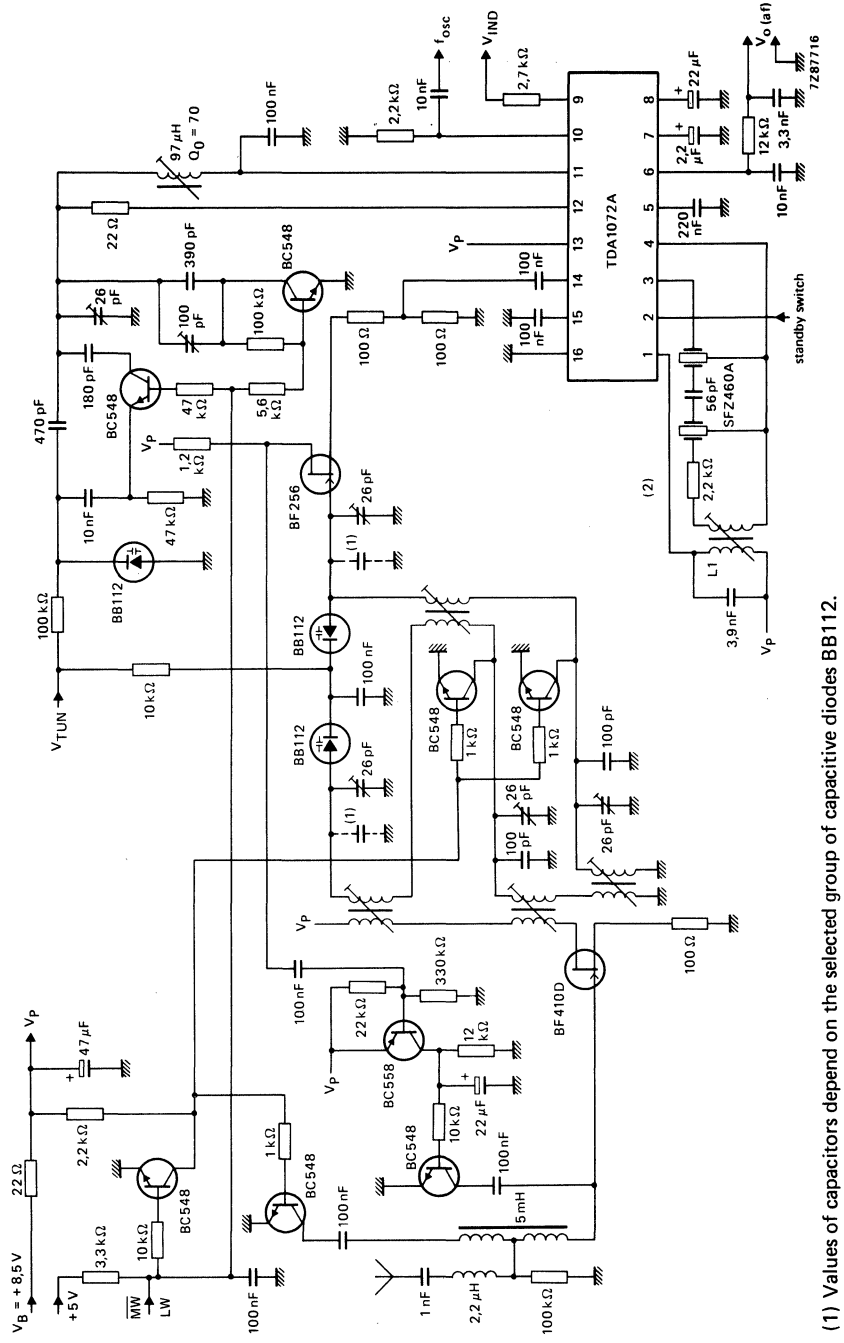


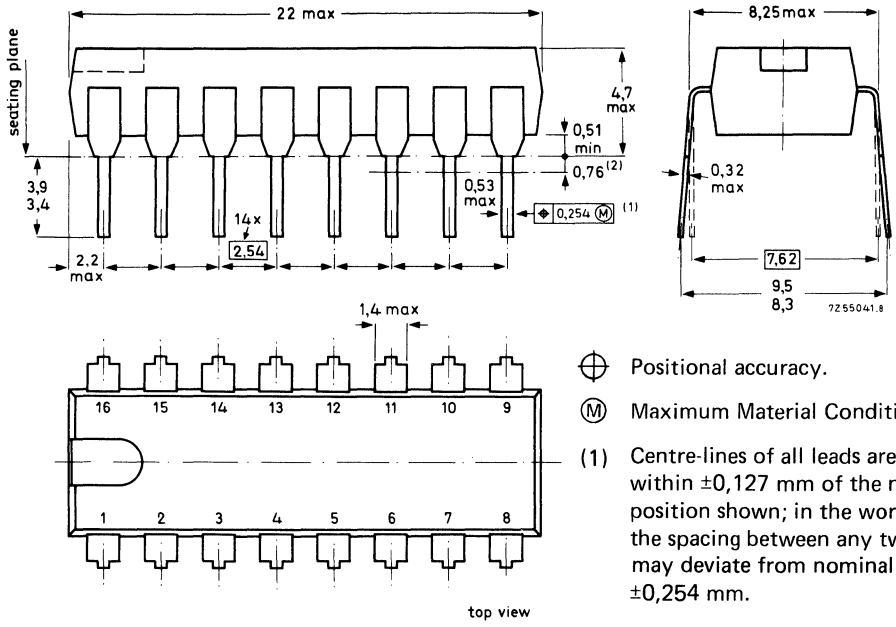
Fig. 17 Printed-circuit board showing track side.



(1) Values of capacitors depend on the selected group of capacitive diodes BB112.
(2) For i.f. filter and coil data refer to Fig. 1.

Fig. 18 Car radio application with capacitive diode tuning and electronic MW/LW switching. The circuit includes pre-stage a.g.c. optimised for good large-signal handling.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

5

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

AM Radio Circuit — TDA5550

The TEA5550 is an a.m. radio circuit, primarily intended for use in car radios.
The IC can reduce the costs in a car radio due to the following features:

- minimum periphery
- no extra r.f.-prestage is necessary
- ceramic i.f. filter is used
- simple on/off switching method allows inexpensive band switching in a.m./f.m. radios

The TEA5550 incorporates the following functions:

- a double balanced mixer with large signal handling range and common mode rejection properties
- a 'one-pin' oscillator, permitting the use of variable capacitance diode tuning
- an i.f. amplifier, designed for ceramic filters
- an a.m. envelope detector
- a.g.c. stages
- a voltage stabilizer, for supplying the internal circuit current and an external current up to 20 mA
- a simple d.c. switch for a.m./f.m. radios

QUICK REFERENCE DATA

Supply voltage range; unstabilized (pin 8)	V_P		10,2 to 18 V
Supply voltage; stabilized (pin 9)*	V_{stab}	typ.	7,5 to 9 V
Ambient temperature	T_{amb}	typ.	25 °C
Supply voltage (pin 8)	V_P	typ.	14,4 V
R.F. condition: f_i = 1 MHz; m = 0,3; f_m = 1 kHz			
R.F. input voltage (pin 1)			
V_o = 30 mV	V_i	typ.	4 μV
S/N = 26 dB	V_i	typ.	16 μV
S/N = 46 dB	V_i	typ.	160 μV
A.F. output voltage (pin 10)			
V_i = 10 mV	V_o	typ.	180 mV
Total harmonic distortion over most of the a.g.c. range; m = 0,8	THD	typ.	1,2 %
R.F. signal handling			
THD = 10%; m = 0,8	V_i	typ.	400 mV
A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference V_{i1} = 200 mV)	V_{i1}/V_{i2}	typ.	86 dB

* Pins 8 and 9 have to be short-circuited externally.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

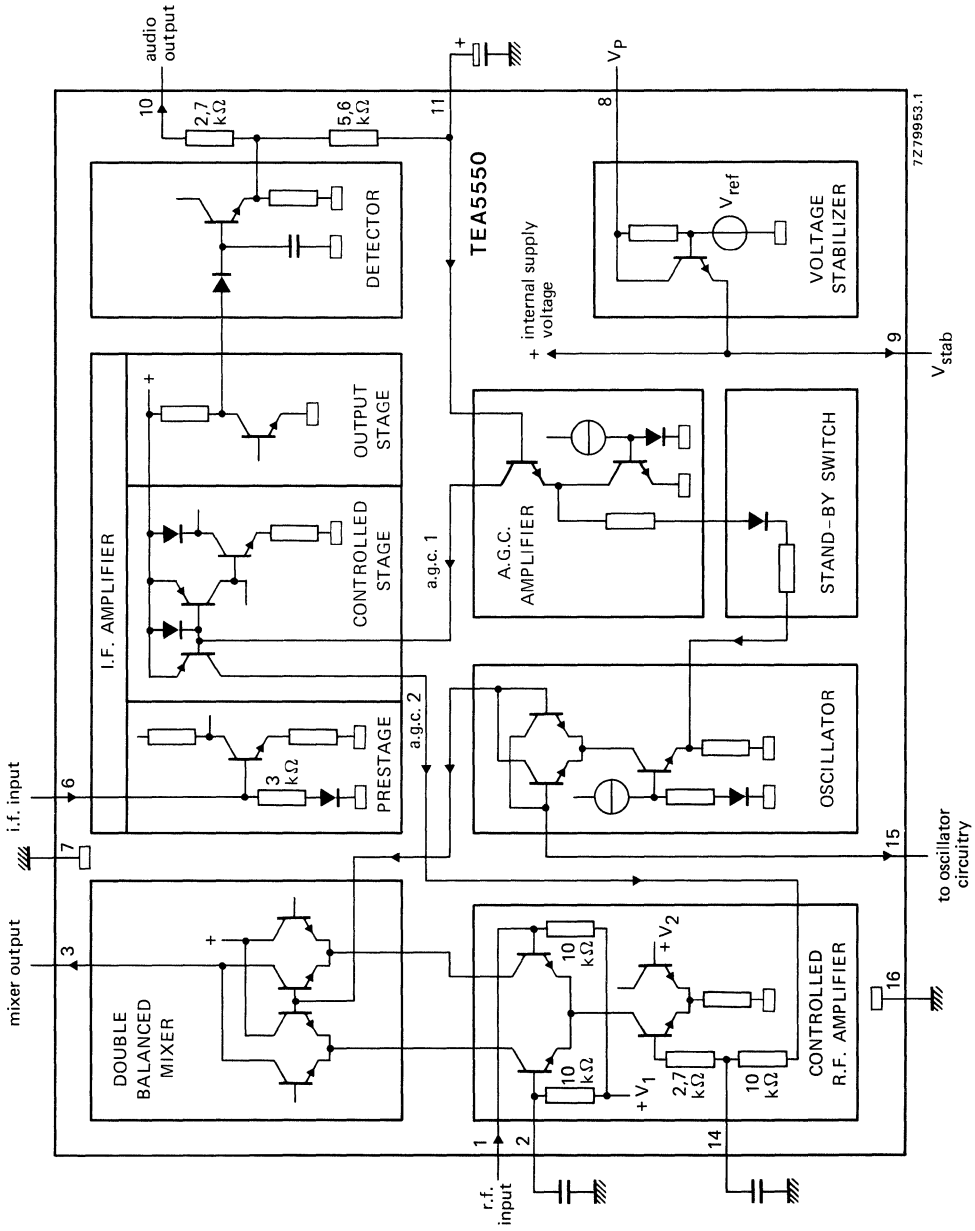


Fig. 1 Block diagram.

5

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages				
pin 8	$V_P = V_{8-16}$	max.	24	V
pin 3	V_{3-16}	max.	24	V
Non-repetitive peak output current (pin 9)	I_{9SM}	max.	100	mA
Total power dissipation	P_{tot}	max.	1100	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 85	°C

Note

Pins 4, 5, 12 and 13 are not allowed to be connected.

D.C. CHARACTERISTICS at $V_i = 0$

V_P = 14,4 V; T_{amb} = 25 °C; measured in Fig. 2

Supply voltage range (unstabilized)*	V_P		10,2 to 18	V
Voltage at pin 9; $-I_9 = 0$	$V_{9-16} = V_{stab}$	typ.	8,7	V
			8 to 9,2	V
Change in stabilization voltage (pin 9)				
at $-I_9$ = 0 to 20 mA	$\Delta V_{9-16} = \Delta V_{stab}$	typ.	50	mV
at V_P = 10,2 to 14,4 V	$\Delta V_{9-16} = \Delta V_{stab}$	typ.	300	mV
Voltage at pin 10	V_{10-16}	typ.	1,1	V
Voltage at pins 1 and 2	$V_{1-16} = V_{2-16}$	typ.	5,0	V
Voltage at pin 15	V_{15-16}	typ.	V_{stab}	
Total supply current; $-I_9 = 0$	I_{tot}	typ.	20	mA
Current drain				
pin 3	I_3	typ.	1	mA
pin 15	I_{15}	typ.	0,2	mA
Current supplied from pin 9	$-I_9$	<	20	mA
Power consumption; $-I_9 = 0$	P	typ.	300	mW

* A stabilized supply voltage of 7,5 to 9 V can also be applied at pin 9 (pin 8 short-circuited to pin 9).

A.C. CHARACTERISTICS

V_P = 14,4 V; T_{amb} = 25 °C; r.f. condition: f_i = 1 MHz, m = 0,3, f_m = 1 kHz; transfer impedance of the i.f. filter $Z_{tr} = v_6/i_3$ = 850 Ω (loaded with 3 kΩ); measured in Fig. 2; unless otherwise specified

R.F. input voltage; V_o = 30 mV	V_i	1,5 to 6,5	μV
R.F. sensitivity at R_S = 25 Ω for:			
S + N/N = 6 dB	V_i	typ. 1,3	μV
S + N/N = 20 dB	V_i	typ. 8	μV
S + N/N = 26 dB	V_i	typ. 16 < 20	μV μV
S + N/N = 46 dB	V_i	typ. 160	μV
S + N/N = 50 dB	V_i	typ. 350	μV
Input conductance at pin 1			
V_i = 0,1 mV	g_{ie}	typ. 0,2	mS
V_i = 100 mV	g_{ie}	typ. 0,1	mS
Input conductance at pin 6	g_{ie}	typ. 0,3	mS
Output capacitance at pin 15	C_{oe}	typ. 20	pF
A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference V_{i1} = 200 mV)	V_{i1}/V_{i2}	typ. 86	dB
A.F. output voltage			
V_i = 10 mV	V_o	> 140 typ. 180	mV mV
Spread of a.f. output voltage	ΔV_o	typ. ± 2	dB
A.F. output impedance (pin 10)	$\lvert Z_o \rvert$	typ. 2,7	kΩ
Total harmonic distortion at m = 0,8			
V_i = 16 μV	THD	< 2,5	%
over most of the a.g.c. range (see also Figs 3 and 10)	THD	typ. 1,2	%
V_i = 25 mV	THD	typ. 3,5	%
R.F. signal handling capability			
THD = 10%; m = 0,8	V_i	> 350 typ. 400	mV mV
I.F. suppression at V_o = 30 mV	α	> 20 typ. 35	dB* dB*
Oscillator voltage			
$V_{9\text{-}16}$ = 8 V; f_{osc} = 1468 kHz	$V_{15\text{-}8}$	typ. 250 < 300	mV mV

* $\alpha = 20 \log \frac{V_{ia}}{V_{ib}}$, where: V_{ia} is input voltage at f = 468 kHz and V_{ib} is input voltage at f = 1 MHz.

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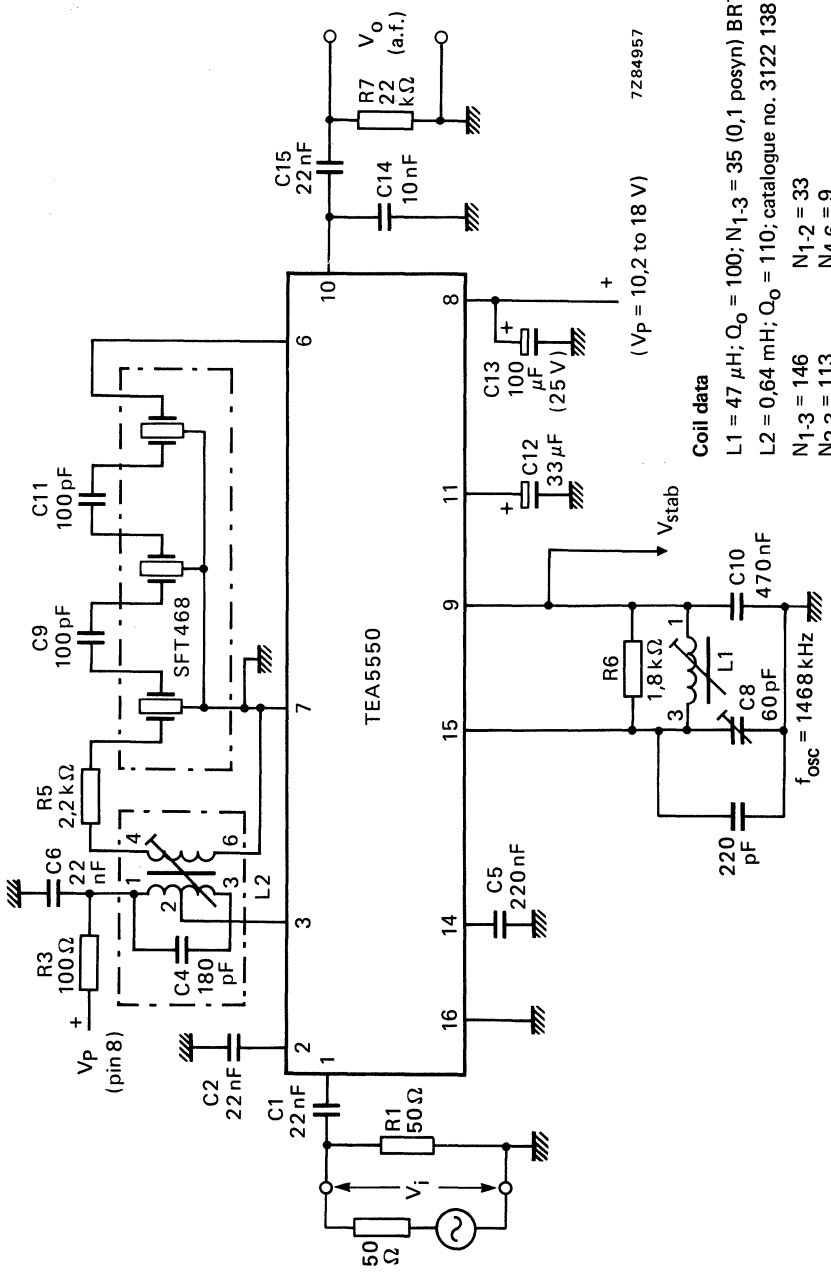

Coil data

L1 = 47 μH; Q_o = 100; $N_{1\text{-}3}$ = 35 (0,1 posyn) BR7

L2 = 0,64 mH; Q_o = 110; catalogue no. 3122 138 91481

$N_{1\text{-}3}$ = 146 $N_{1\text{-}2}$ = 33

$N_{2\text{-}3}$ = 113 $N_{4\text{-}6}$ = 9

The transfer impedance of the i.f. filter is:

$Z_{tr} = v_6/i_3 = 850\ \Omega\ (R_L = 3\ k\Omega)$.

Fig. 2 AM test circuit.

APPLICATION INFORMATION

Figures 4 and 7 show the circuit diagrams of single-tuned and double-tuned AM channels respectively, using the TEA5550 and an r.f.-tuning unit (type ALPS). The i.f. filter consists of a single-tuned coil in combination with a ceramic filter (type SFT468).

Typical performance (measured in Figs 4 and 7)

V_P = 14,4 V; T_{amb} = 25 °C; aerial signal conditions: f_o = 1 MHz; m = 0,3; f_m = 1 kHz (dummy aerial as shown in Figs 4 and 7)

		Fig. 4 single-tuning	Fig. 6 double-tuning	
R.F. input voltage for:				
S + N/N = 6 dB	V_i	4	4	μV
S + N/N = 26 dB	V_i	47	49	μV
A.F. output voltage (R_L = R6 = 22 kΩ)				
V_i = 1 mV	V_o	160	160	mV
Signal-to-noise ratio				
V_i = 1 mV	S/N	> 50	> 50	dB
A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference V_{i1} = 200 mV); see Figs 3 and 10	V_{i1}/V_{i2}	88	88	dB
R.F. signal handling capability THD < 10%; m = 0,8; see Figs 3 and 10	V_i	1,5	1,5	V
Total harmonic distortion (over most of the a.g.c. range); m = 0,8; see Figs 3 and 10	THD	1,2	1,2	%
Oscillator voltage measured across the tank circuit	V_{osc}	250	250	mV
Total selectivity (r.f. and i.f.)	S_9	44	46	dB
Total bandwidth (r.f. and i.f.)	B_{3dB}	4,1	4,4	kHz
I.F. suppression at V_i = 20 μV				
tuned frequency = 600 kHz	α	55	75	dB
= 1600 kHz	α	58	85	dB
Image rejection at V_i = 20 μV				
tuned frequency = 600 kHz		50	72	dB
= 1000 kHz		46	68	dB
= 1400 kHz		42	64	dB
Whistle at V_i = 5 mV				
2 x i.f.-tweet		−40	−40	dB
3 x i.f.-tweet		−48	−48	dB

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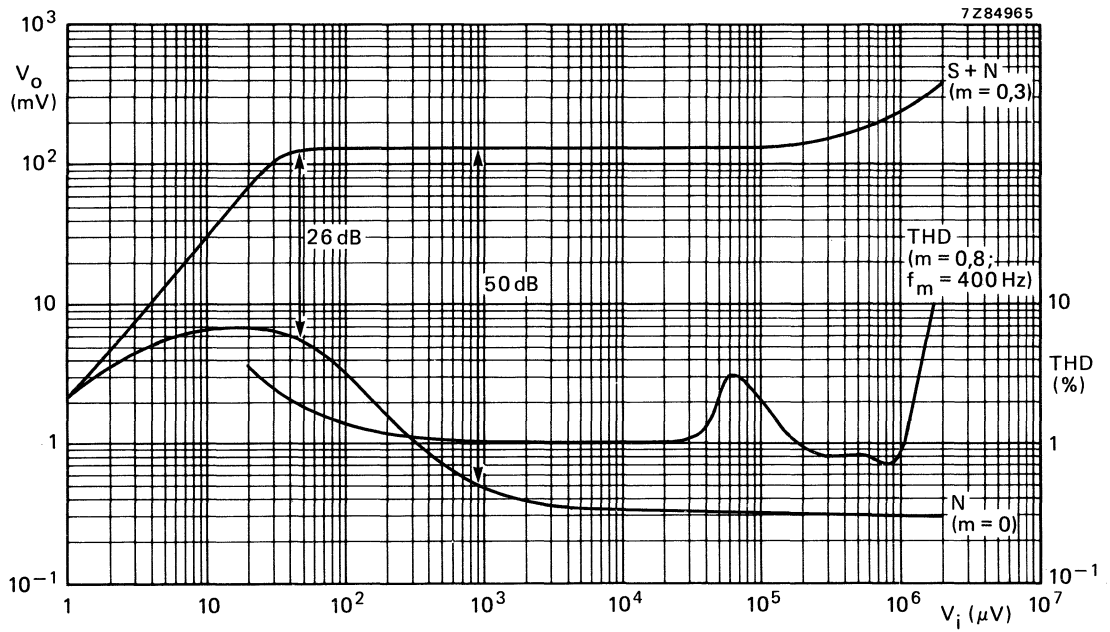

Fig. 3 Typical signal and noise output voltages (V_o is a.f. output voltage) as a function of the input voltage V_i. Also shown is the total harmonic distortion (THD). These curves are for a single-tuned AM channel; the dummy aerial is as shown in Fig. 4; f_o = 1 MHz; f_m = 1 kHz; m = 0,3 (unless otherwise specified).

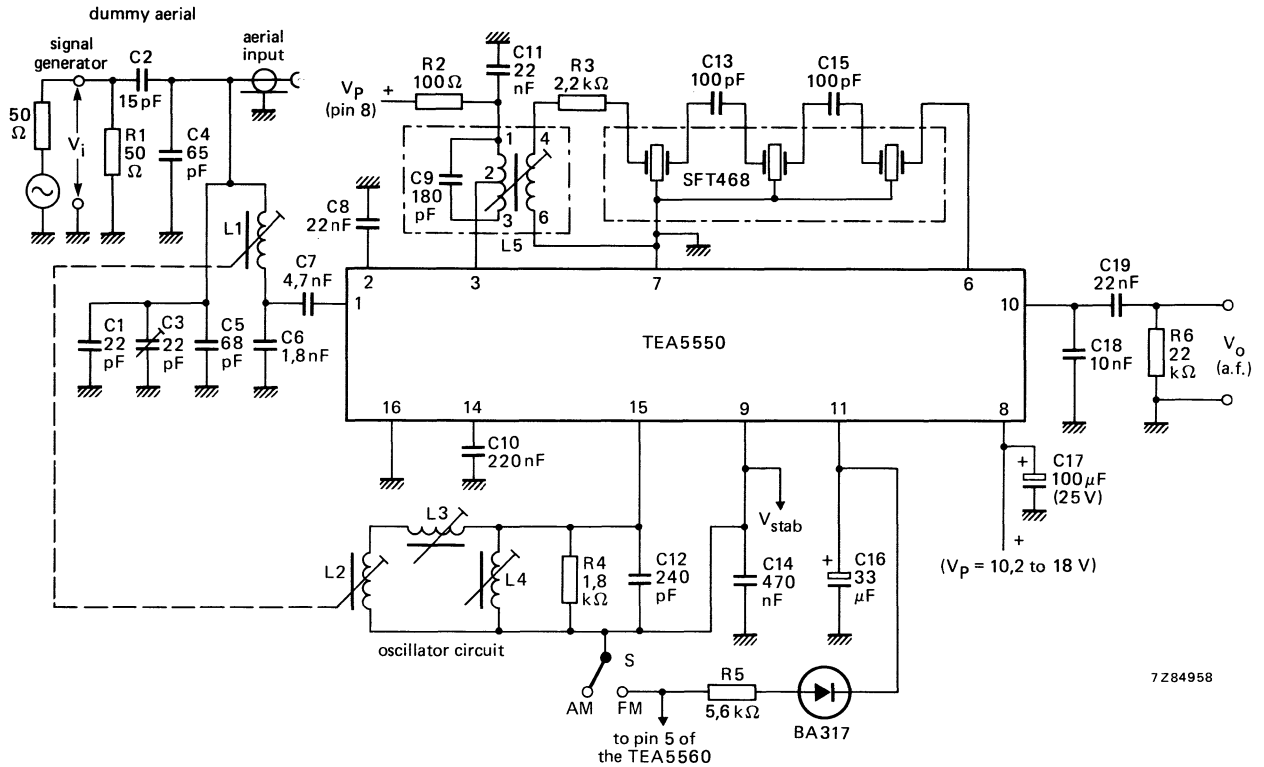

Fig. 4 Typical application circuit diagram for a single-tuned AM channel in car radio receivers using the TEA5550; S is AM/FM switch; for printed-circuit board see Figs 5 and 6.

Coil data: L1, L2 = tuning coils, ALPS unit MMK IIEII (for coil connections see Fig. 5)
L3 = trimming coil (4,7 μH); catalogue number 3122 138 27460
L4 = padding coil (200 μH); catalogue number 3111 118 23510
L5 = i.f. coil; catalogue number 3122 138 91481

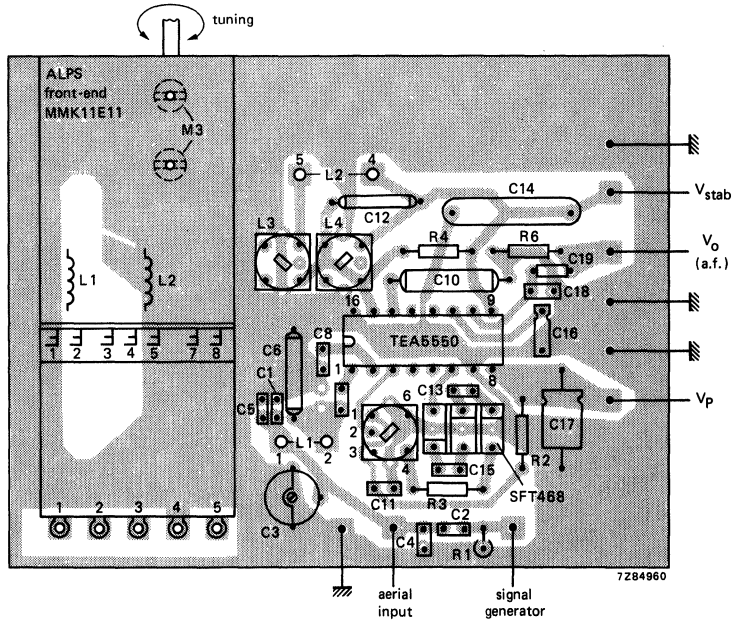

Fig. 5 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 4.

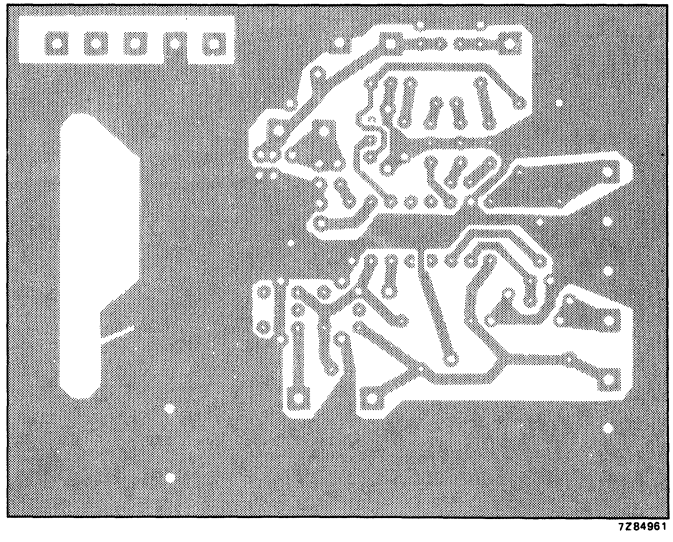

Fig. 6 Printed-circuit board showing track side.

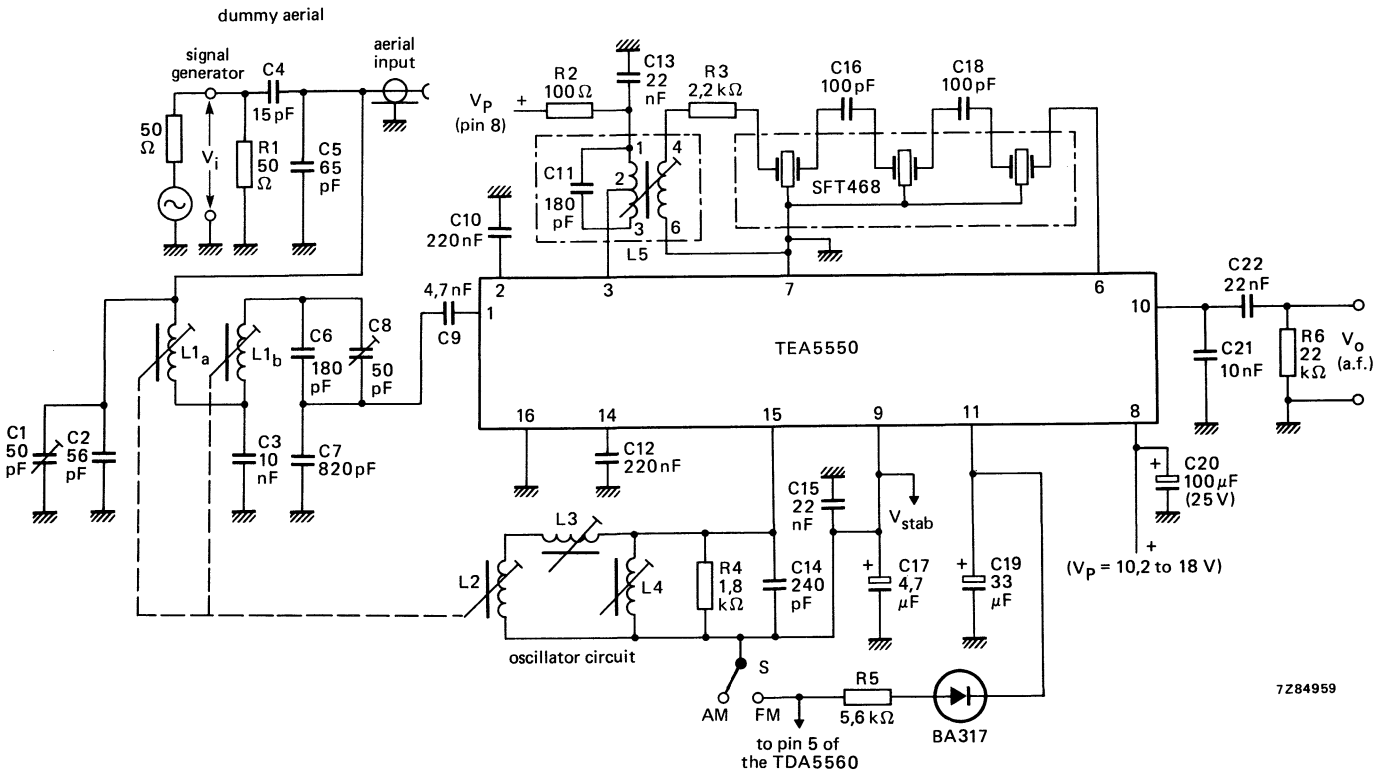

Fig. 7 Typical application circuit diagram for a double-tuned AM channel in car radio receivers using the TEA5550; S is AM/FM switch; for printed-circuit board see Figs 8 and 9.

Coil data: $L1_a$, $L1_b$, L2 = tuning coils, ALPS unit MMK IIEII (for coil connections see Fig. 8)
L3 = trimming coil (4,7 μH); catalogue number 3122 138 27460
L4 = padding coil (200 μH); catalogue number 3111 118 23510
L5 = i.f. coil; catalogue number 3122 138 91481

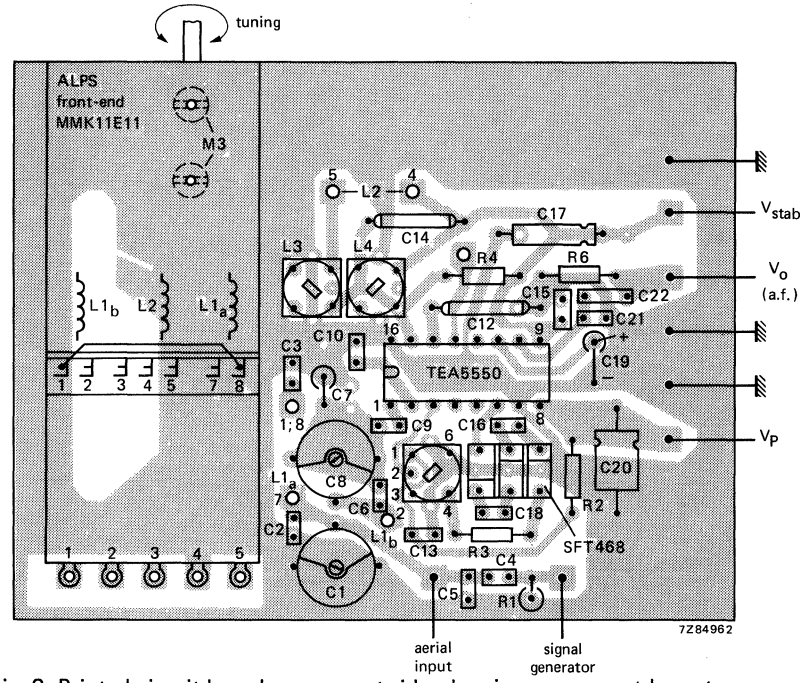

Fig. 8 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 7.

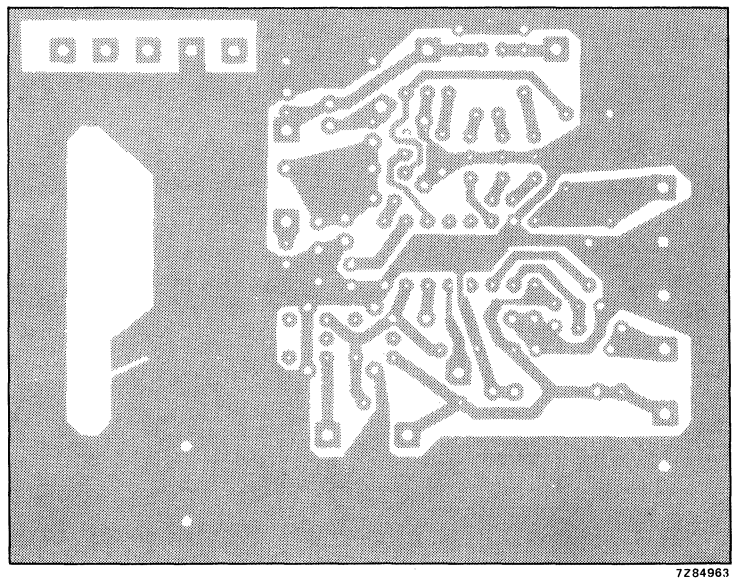

Fig. 9 Printed-circuit board showing track side.

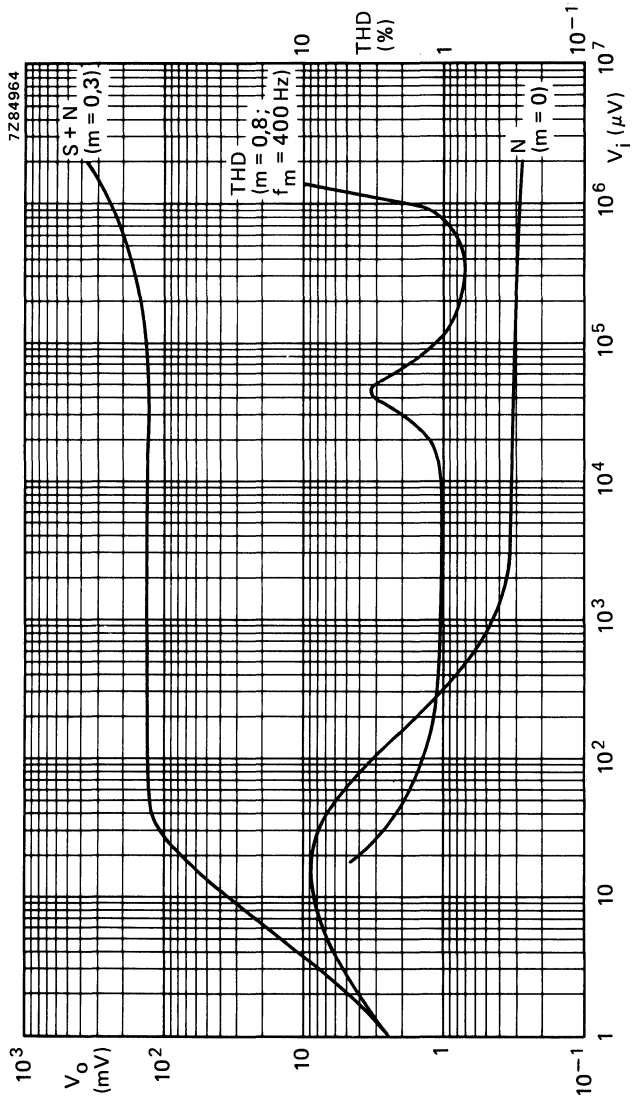

Fig. 10 Typical signal and noise output voltages (V_o is a.f. output voltage) as a function of the input voltage V_i. Also shown is the total harmonic distortion (THD). These curves are for a double-tuned AM channel; the dummy aerial is shown in Fig. 7; f_o = 1 MHz; f_m = 1 kHz; m = 0,3 (unless otherwise specified).

5

AM/FM Radio Receiver Circuit — TEA5570

GENERAL DESCRIPTION

The TEA5570 is a monolithic integrated radio circuit for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. Apart from the AM/FM switch function the IC incorporates for AM a double balanced mixer, 'one-pin' oscillator, i.f. amplifier with a.g.c. and detector, and a level detector for tuning indication. The FM circuitry comprises i.f. stages with a symmetrical limiter for a ratio detector. A level detector for mono/stereo switch information and/or indication complete the FM part.

Features

- Simple d.c. switching for AM to FM by only one d.c. contact to ground (no switch contacts in the i.f. channel, a.f. or level detector outputs)
- AM and FM gain control
- Low current consumption (I_{tot} = 6 mA)
- Low voltage operation (V_P = 2,7 to 9 V)
- Ability to handle large AM signals; good i.f. suppression
- Applicable for inductive, capacitive and diode tuning
- Double smoothing of a.g.c. line
- Short-wave range up to 30 MHz
- Lumped or distributed i.f. selectivity with coil and/or ceramic filters
- AM and a.g.c. output voltage control
- Distribution of PCB wiring provides good frequency stability
- Economic design for 'AM only' receivers

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

Supply voltage	$V_P = V_{7-16}$	typ.	5,4 V
Supply current	I_7	typ.	6,2 mA
AM performance (pin 2) for m = 0,3			
Sensitivity			
at V_o = 10 mV	V_i	typ.	1,7 μV
at S/N = 26 dB	V_i	typ.	16 μV
A.F. output voltage at V_i = 1 mV	V_o	typ.	100 mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,5 %
FM performance (pin 1) for Δf = ± 22,5 kHz			
limiting sensitivity, −3 dB	V_i	typ.	110 μV
Signal-to-noise ratio for V_i = 1 mV	S/N	typ.	65 dB
A.F. output voltage at V_i = 1 mV	V_o	typ.	100 mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,3 %
AM suppression at V_i = 10 mV	AMS	typ.	50 dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

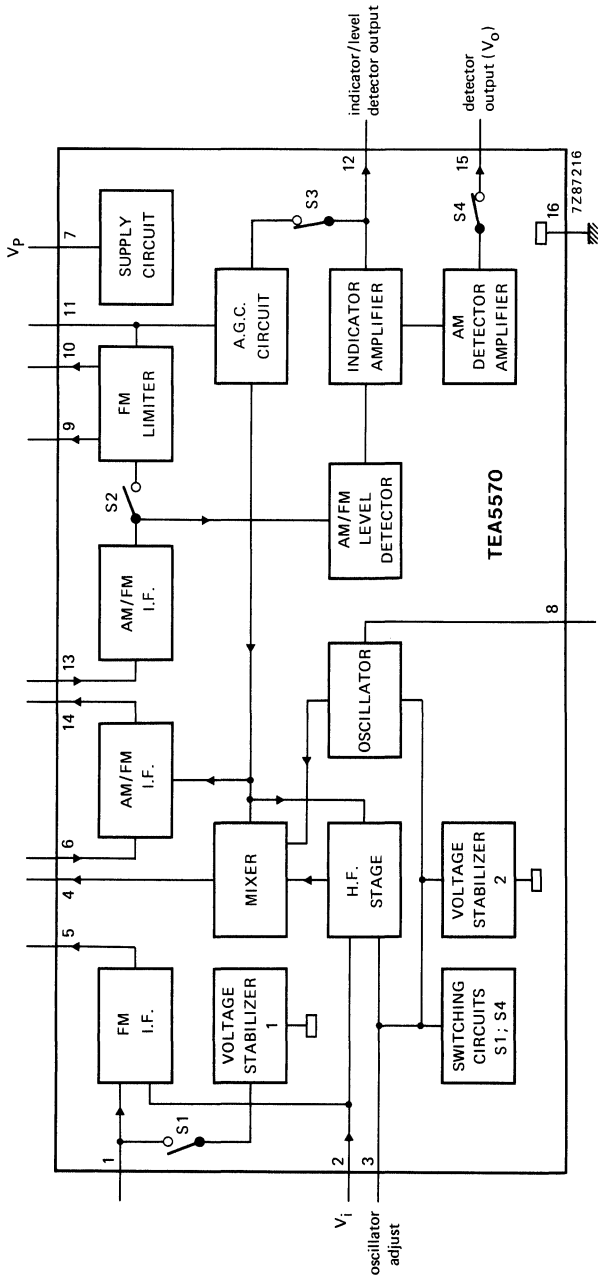

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-16}$	max.	12 V
Voltage at pins 4, 5, 9 and 10 to pin 16 (ground)	V_{n-16}	max.	12 V
Voltage range at pin 8	V_{8-16}		$V_P \pm 0{,}5$ V
Current into pin 5	I_5	max.	3 mA
Total power dissipation	P_{tot}	see Fig. 2	
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range	T_{amb}	−30 to +85	°C

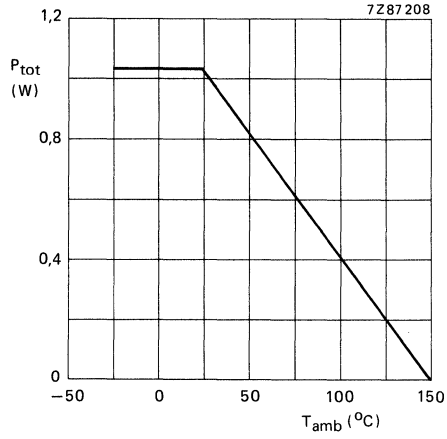

Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply voltage (note 1)	$V_P = V_{7-16}$	2,4	5,4	9,0	V
Voltages					
at pin 1 (FM)	V_{1-16}	–	1,42	–	V
at pin 1; $-I_1$ = 50 μA (FM)	V_{1-16}	–	1,28	–	V
at pins 2 and 3 (AM)	$V_{2,3-16}$	–	1,42	–	V
at pin 6	V_{6-16}	–	0,7	–	V
at pin 11	V_{11-16}	–	1,4	–	V
at pin 13	V_{13-16}	–	0,7	–	V
at pin 14	V_{14-16}	–	4,3	–	V
Currents					
Supply current	I_7	4,2	6,2	8,2	mA
Current supplied from pin 1 (FM)	$-I_1$	–	–	50	μA
Current supplied from pin 12	$-I_{12}$	–	–	20	μA
Current supplied from pin 15	$-I_{15}$	–	30	–	μA
Current into pin 4 (AM)	I_4	–	0,6	–	mA
Current into pin 5 (FM) (note 4)	I_5	–	0,35	–	mA
Current into pin 8 (AM)	I_8	–	0,3	–	mA
Current into pins 9, 10 (FM)	$I_{9,10}$	–	0,65	–	mA
Current into pin 14	I_{14}	–	0,4	–	mA
Power consumption	P	–	40	–	mW

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A.C. CHARACTERISTICS

AM performance

V_P = 6 V; T_{amb} = 25 °C; r.f. condition: f_i = 1 MHz, m = 0,3, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/I_4$ = 2,7 kΩ; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity (pin 2)					
at V_o = 30 mV	V_i	3,5	5,0	7,0	μV
at S + N/N = 6 dB	V_i	–	1,3		μV
at S + N/N = 26 dB	V_i	–	16	20	μV
at S + N/N = 50 dB	V_i	–	1	–	mV
Signal handling (THD ⩽ 10% at m = 0,8)	V_i	200	–	–	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion					
at V_i = 100 μV to 100 mV (m = 0,3)	THD	–	0,5	–	%
at V_i = 2 mV (m = 0,8)	THD	–	1,0	2,5	%
at V_i = 200 mV (m = 0,8)	THD	–	4,0	10	%
I.F. suppression at V_o = 30 mV (note 2)	α	26	35	–	dB
Oscillator voltage (pin 8; note 3)					
at f_{osc} = 1455 kHz	$V_{8\text{-}16}$	120	160	200	mV
Indicator current (pin 12) at V_i = 1 mV	I_{12}	–	200	230	μA

FM performance

V_P = 6 V; T_{amb} = 25 °C; i.f. condition: f_i = 10,7 MHz, Δf = ± 22,5 kHz, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/i_5$ = 275 Ω; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I.F. part					
I.F. sensitivity (adjustable; note 4)					
Input voltage					
at −3 dB before limiting	V_i	90	110	130	μV
at S + N/N = 26 dB	V_i	–	6	–	μV
at S + N/N = 65 dB	V_i	–	1	–	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion at V_i = 1 mV	THD	–	0,3	–	%
AM suppression (note 5)	AMS	–	50	–	dB
Indicator/level detector (pin 12)					
Indicator current	I_{12}	–	250	325	μA
D.C. output voltage					
at V_i = 300 μV	$V_{12\text{-}16}$	–	0,25	–	V
at V_i = 2 mV	$V_{12\text{-}16}$	–	1,0	–	V
AM to FM switch					
Switching current at $V_{3\text{-}16} < 1$ V	$-I_3$	–	–	400	μA

Notes to characteristics

1. Oscillator operates at $V_{7\text{-}16} > 2{,}25$ V.
2. I.F. suppression is defined as the ratio $\alpha = 20 \log \frac{V_{i1}}{V_{i2}}$ where: V_{i1} is the input voltage at f = 455 kHz and V_{i2} is the input voltage at f = 1 MHz.
3. Oscillator voltage at pin 8 can be preset by R_{osc} (see Fig. 10).
4. Maximum current into pin 5 can be adjusted by R1 (see Fig. 10);
   $I_5 = \frac{V_{3\text{-}16}}{R1}$ --I_3 when $V_{3\text{-}16} = 800$ mV; $I_3 = 400\ \mu$A.
5. AM suppression is measured with $f_m = 1$ kHz, m = 0,3 for AM; $f_m = 400$ Hz, $\Delta f = \pm 22{,}5$ kHz for FM.

Facility adaptation

Facility adaptation is achieved as follows (see Fig. 10):

Facility	Component
FM sensitivity	R1 fixes the current at pin 5 ($I_5 = \frac{V_{3\text{-}16}}{R1} - 400\ \mu$A) (gain adjustable ± 10 dB; see note 4)
AM sensitivity	R11 and coil tapping
AM oscillator biasing	R_{osc}
AM output voltage	R7, R11
AM a.g.c. setting	R7

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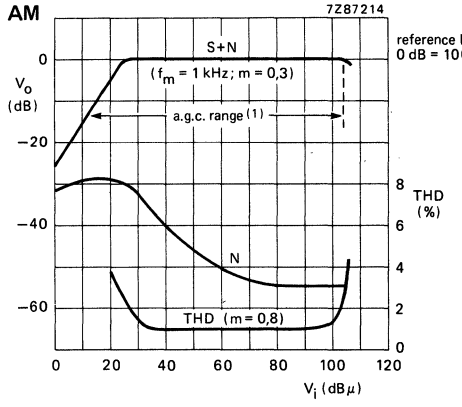
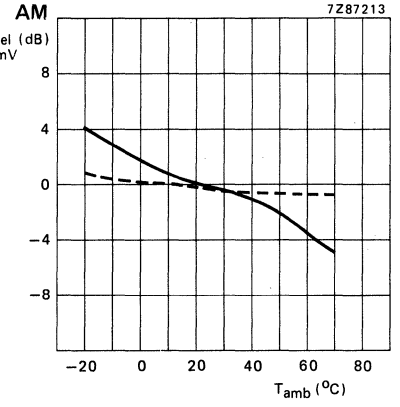
Typical graphs



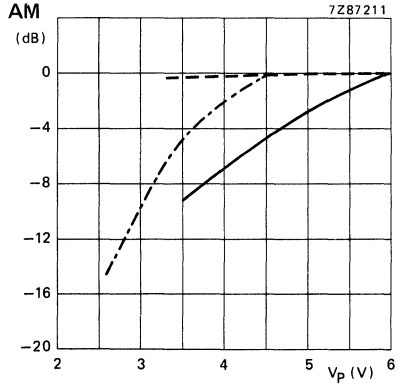
(1) A.G.C. range (figure of merit, FOM).

Fig. 3 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 mV; m = 0,3.
– – – – output voltage (V_o) at V_i = 2 mV; m = 0,3.

Fig. 4 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 V; m = 0,3: 6,0 V application.
–·–·– sensitivity (V_i) at V_o = 30 mV; m = 0,3: 4,5 V application.
– – – – output voltage (V_o) at V_i = 0,2 mV; m = 0,3.

Fig. 5 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 1 MHz in test circuit Fig. 10, for application V_P = 6 V. Also shown is the sensitivity for V_P = 4,5 V application (Fig. 16).

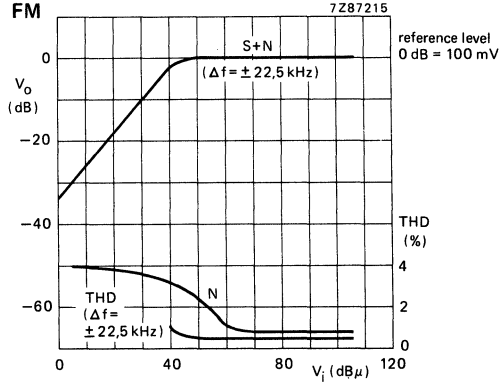
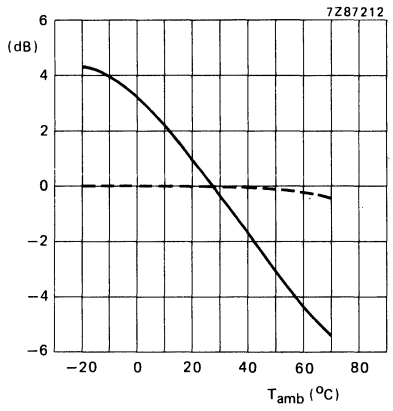


Fig. 6 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

FM



——— sensitivity at −3 dB limiting.
– – – – output voltage (V_o) at V_i = 1 mV; $\Delta f = \pm 22$ kHz.

Fig. 7 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

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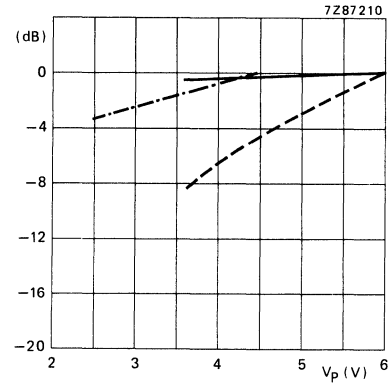
FM



——— sensitivity at −3 dB limiting: V_P = 6,0 V application.
–·–·– sensitivity at −3 dB limiting: V_P = 4,5 V application.
– – – – output voltage (V_o) at V_i = 1 mV; $\Delta f = \pm 22{,}5$ kHz.

Fig. 8 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

AM/FM

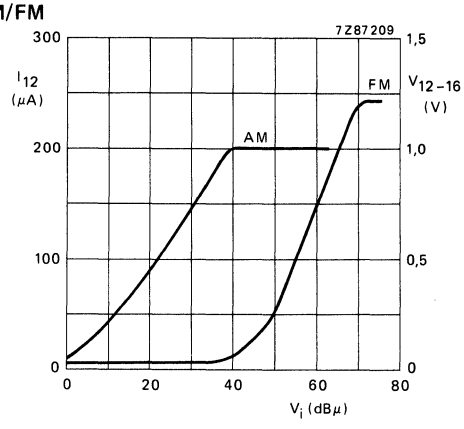


Fig. 9 Indicator output current (I_{12}) and d.c. output voltage ($V_{12\text{-}16}$): AM f_i = 1 MHz; FM f_i = 10,7 MHz as a function of input voltage (V_i). Measured in Fig. 10; V_P = 6 V; $R_{12\text{-}16}$ = 5 kΩ.

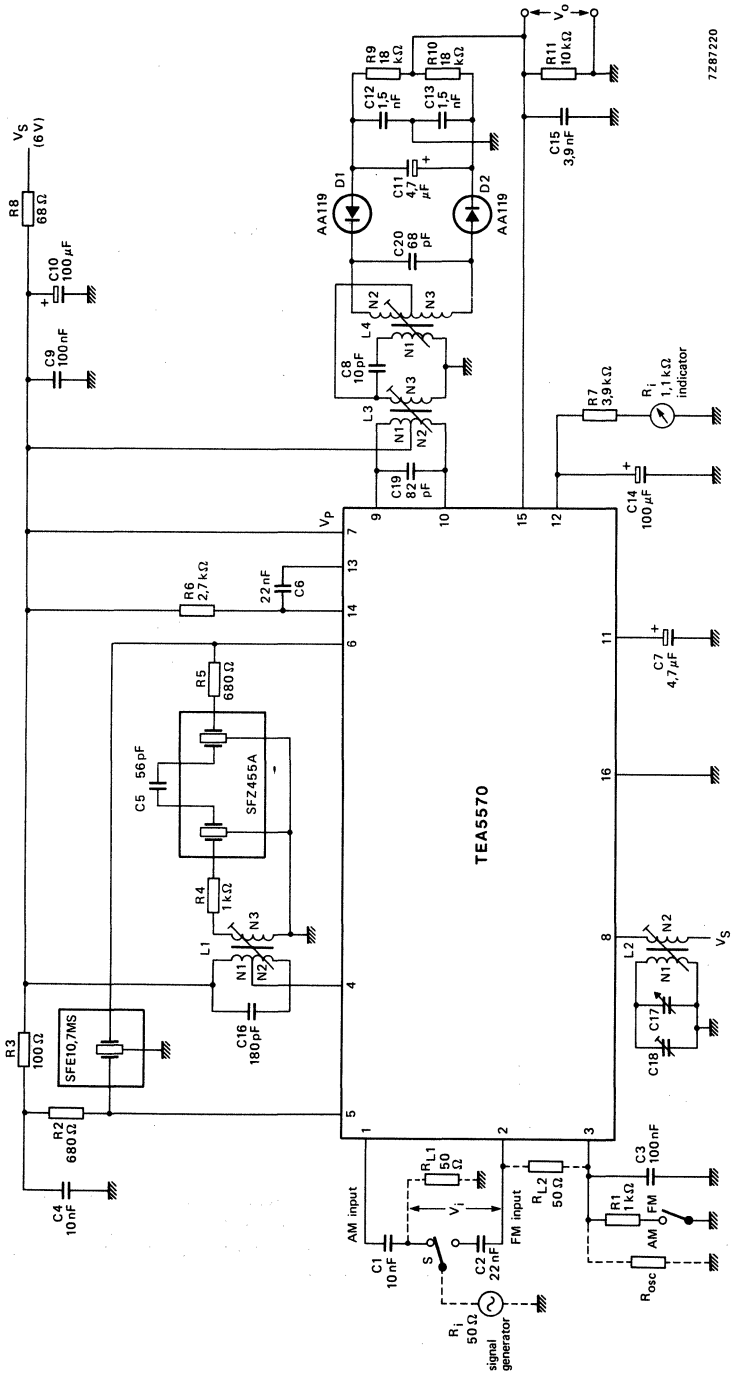


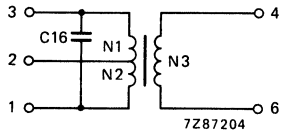
Fig. 10 Test circuit.

Coil data

The transfer impedance of the i.f. filter is:
AM: $|Z_{tr}| = v_6/i_4 = 2{,}7$ kΩ (SFZ 455A).
FM: $|Z_{tr}| = v_6/i_5 = 275$ Ω (SFE 10,7 MS).
See also Figs 11, 12, 13 and 14.

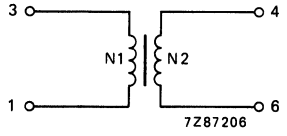
COIL DATA

AM i.f. coils (Fig. 10)



N1 = 73
N2 = 73
N3 = 9
C16 = 180 pF (internal)
Wire = 0,07 mm dia.

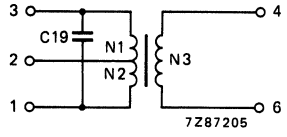
Fig. 11 I.F. bandpass filter (L1). TOKO sample no. 7 MC-7 P.



N1 = 90
N2 = 7
Wire = 0,07 mm dia.

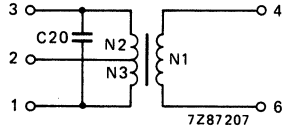
Fig. 12 Oscillator coil (L2). TOKO sample no. 7 BR-7 P.

FM i.f. coils (Fig. 10)



N1 = 5
N2 = 5
N3 = 4
C19 = 82 pF (internal)
Wire = 0,1 mm dia.

Fig. 13 Primary ratio detector coil (L3). TOKO sample no. 119 AN-7 P.

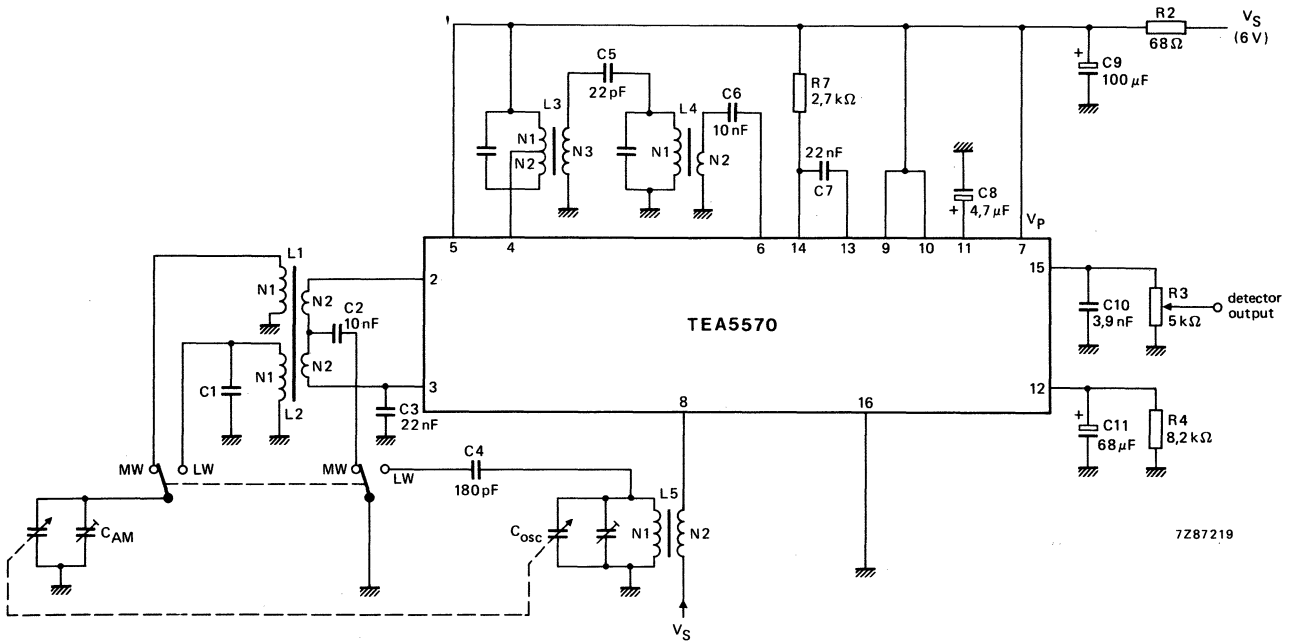


N1 = 2
N2 = 6
N3 = 6
C20 = 68 pF (internal)
Wire = 0,1 mm dia.

Fig. 14 Secondary ratio detector coil (L4). TOKO sample no. 119 AN-7 P.

APPLICATION INFORMATION

Figs 15 and 17 show the circuit diagrams for the application of 6 V AM MW/LW and 4,5 V AM/FM channels respectively, using the TEA5570. Fig. 16 shows the circuitry of the TEA5570.



Coil data

L3	N1 = 73	L4	N1 = 146	L5	N1 = 90
	N2 = 73		N2 = 9		N2 = 6
	N3 = 9		C = 180 pF		
	C = 180 pF				

Fig. 15 Typical application circuit for 6 V AM MW/LW reception using the TEA5570.

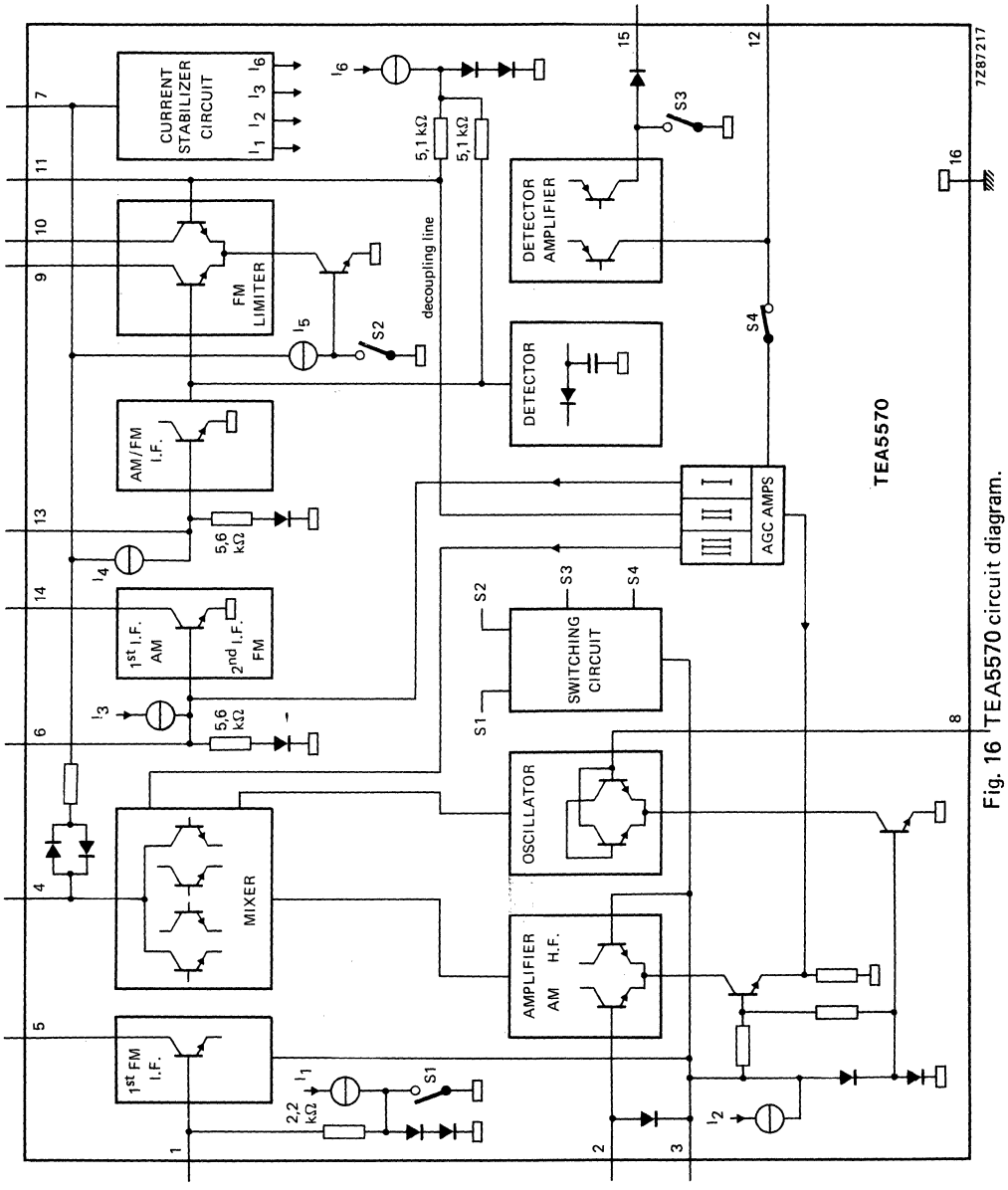


Fig. 16 TEA5570 circuit diagram.

APPLICATION INFORMATION (continued)

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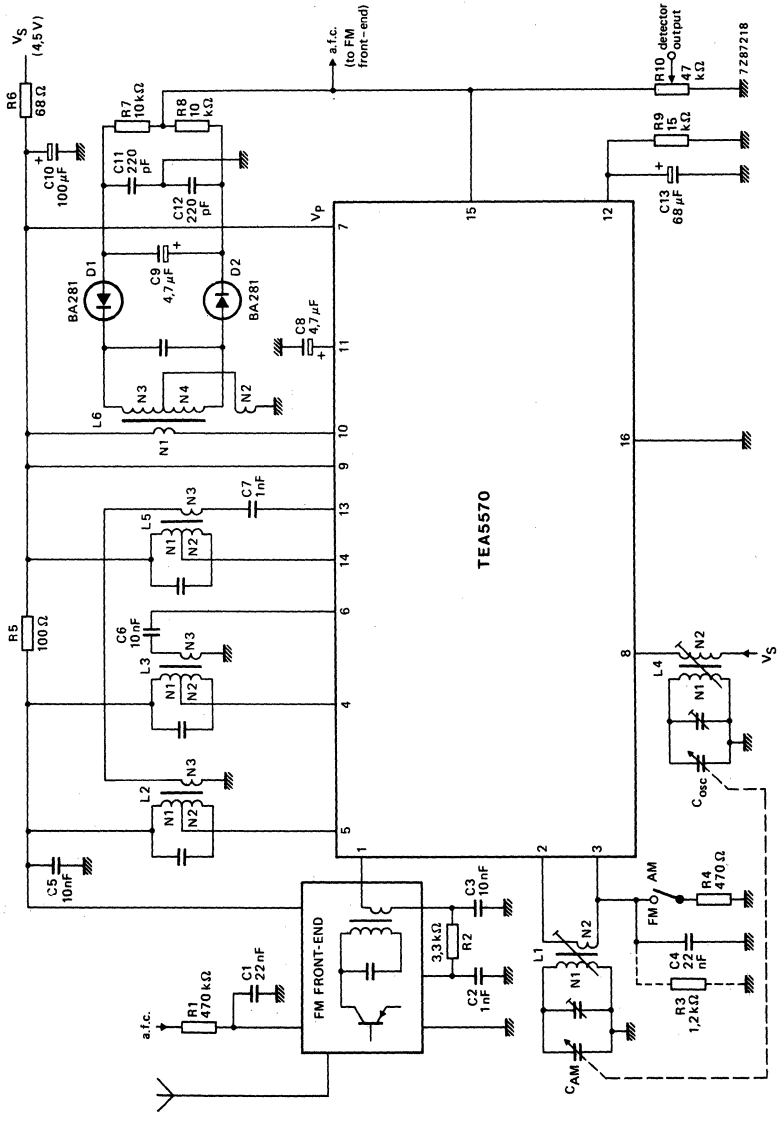

Fig. 17 Typical application circuit for 4,5 V AM/FM reception using the TEA5570 with coils and single-tuned ratio detector (with silicon diodes).

Interference Suppressor | TDA1001B, BT

GENERAL DESCRIPTION

The TDA1001B is a monolithic integrated circuit for suppressing interference and noise in FM mono and stereo receivers.

Features

- Active low-pass and high-pass filters
- Interference pulse detector with adjustable and controllable response sensitivity
- Noise detector designed for FM i.f. amplifiers with ratio detectors or quadrature detectors
- Schmitt trigger for generating an interference suppression pulse
- Active pilot tone generation (19 kHz)
- Internal voltage stabilization

QUICK REFERENCE DATA

Supply voltage (pin 9)	V_P	typ.	12 V
Supply current (pin 9)	I_P	typ.	14 mA
A.F. input signal handling (pin 1) (peak-to-peak value)	$V_{i(p-p)}$	typ.	1 V
Input resistance (pin 1)	R_i	min.	35 kΩ
Voltage gain (V_{1-16}/V_{6-16})	G_v	typ.	0,5 dB
Total harmonic distortion	THD	typ.	0,25 %
Bandwidth	B	typ.	70 kHz
Suppression pulse threshold voltage (peak value); $R_{13} = 0$	$V_{i(tr)OM}$	typ.	19 mV
Suppression pulse duration	t_s	typ.	27 μs
Supply voltage range (pin 9)	V_P		7,5 to 16 V
Operating ambient temperature range	T_{amb}		−30 to +80 °C

PACKAGE OUTLINE

TDA1001B: 16-lead DIL; plastic (SOT-38).
TDA1001BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

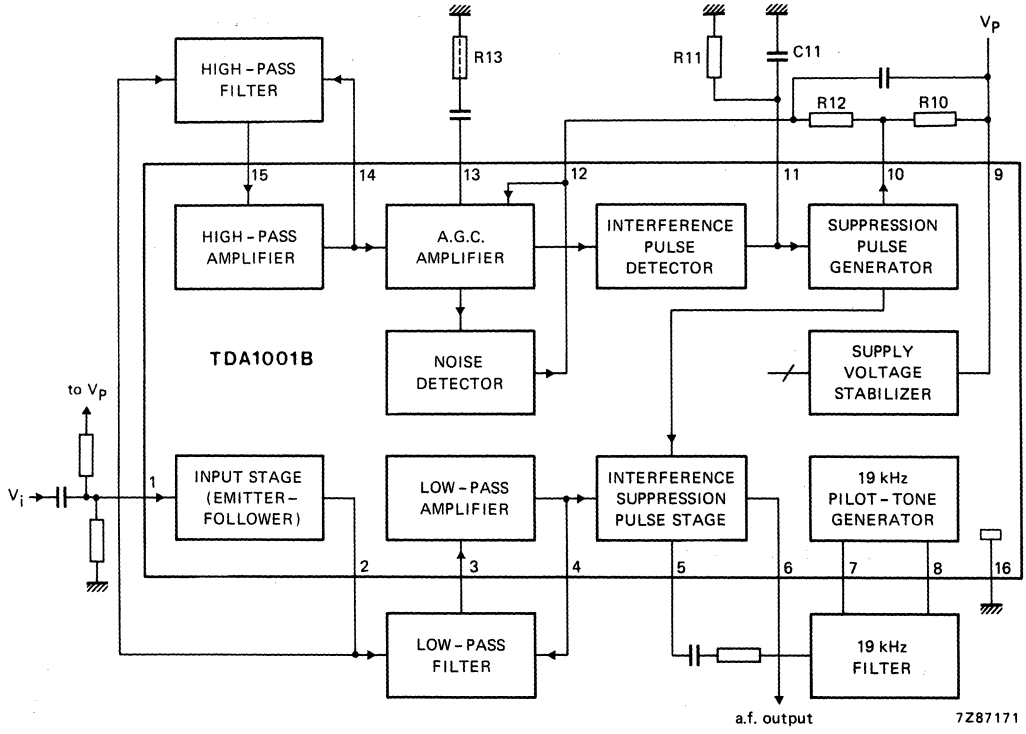

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	V_P	max.	18 V
Input voltage (pin 1)	V_{1-16}	max.	V_P V
Output current (pin 6)	I_6	max.	1 mA
	$-I_6$	max.	15 mA
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature range	T_{amb}	−30 to +80	°C

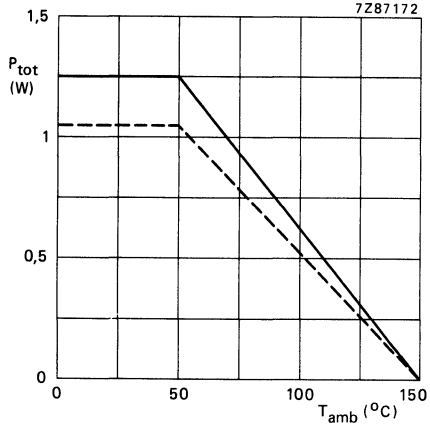

Fig. 2 Power derating curves.
——— in plastic DIL (SOT-38) package (TDA1001B)
– – – – – in plastic mini-pack (SO-16; SOT-109A) package (TDA1001BT); mounted on a ceramic substrate of 50 x 15 x 0,7 mm.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Input stage					
Input impedance (pin 1) f = 40 kHz	$\|Z_{i1}\|$	–	45	–	kΩ
Input resistance (pin 1) with pin 2 not connected	R_{i1}	–	600	–	kΩ
Input bias current (pin 1) $V_{1\text{-}16}$ = 4,8 V	I_{i1}	–	6	15	μA
Output resistance (pin 2) unloaded	R_{o2}		low-ohmic		
Internal emitter resistance	$R_{2\text{-}16}$	–	5,6	–	kΩ
Low-pass amplifier					
Input resistance (pin 3)	R_{i3}	10	–	–	MΩ
Input bias current (pin 3)	I_{i3}	–	–	7	μA
Output resistance (pin 4)	R_{o4}	–	–	5	Ω
Voltage gain (V_4/V_3)	$G_{v4/3}$	–	1,1	–	
Suppression pulse stage					
Input offset current at pin 5 during the suppression time t_s	I_{io5}	–	50	200	nA
Output stage					
Output resistance (pin 6)	R_{o6}		low-ohmic		
Internal emitter resistance	$R_{6\text{-}16}$	–	6	–	kΩ
Current gain (I_5/I_6)	$G_{i5/6}$	–	85	–	dB
Pilot tone generation (19 kHz)					
Input impedance (pin 8)	$\|Z_{i8}\|$	–	–	1	Ω
Output impedance (pin 7) pin 8 open	$\|Z_{o7}\|$	150	–	–	kΩ
Output bias current (pin 7)	I_{o7}	0,7	1	1,3	mA
Current gain (I_7/I_8)	$G_{i7/8}$	–	3	–	
High-pass amplifier					
Input resistance (pin 15)	R_{i15}	10	–	–	MΩ
Input bias current (pin 15)	I_{i15}	–	–	7	μA
Output resistance (pin 14)	R_{o14}	–	–	5	Ω
Voltage gain ($V_{14/15}$)	$G_{v14/15}$	–	1,4	–	

parameter	symbol	min.	typ.	max.	unit
A.G.C. amplifier; interference and noise detectors					
Internal resistance (pins 13 and 14)	$R_{13\text{-}14}$	1,5	2,0	2,5	kΩ
Operational threshold voltage (uncontrolled); peak value (pin 14) of the interference pulse detector	$\pm V_{14int\ m}$	–	15	–	mV
of the noise detector	$\pm V_{14n\ m}$	–	6,5	–	mV
Output voltage (peak value; pin 11)	$V_{11\text{-}16M}$	5,2	5,8	6,4	V
Output control current (pin 12) (peak value)	I_{12M}	150	200	250	μA
Output bias current (pin 12)	I_{o12}	–	2,5	6	μA
Input threshold voltage for onset of control (pin 12)	$V_{12\text{-}9}$	360	425	500	mV
($V_{i(tr)O}$ + 3 dB)	or:	–	$0{,}66V_{BE}$	–	mV
Suppression pulse generation (Schmitt trigger)					
Switching threshold (pin 11) 1: gate disabled	$V_{11\text{-}16}$	–	3,2	–	V
2: gate enabled	$V_{11\text{-}16}$	–	2,0	–	V
Switching hysteresis	$\Delta V_{11\text{-}16}$	–	1,2	–	V
Input offset current (pin 11)	I_{io11}	–	–	100	nA
Output current (pin 10) gate disabled; peak value	I_{o10M}	0,6	1	1,4	mA
Reverse output current (pin 10)	I_{R10}	–	–	2	μA
Sensitivity (pin 10)	$V_{10\text{-}16}$	2,5	–	–	V

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APPLICATION INFORMATION

V_P = 12 V; T_{amb} = 25 °C; f = 1 kHz; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 9)	V_P	7,5	12	16	V
Quiescent supply current (pin 9)	I_P	10	14	18	mA
Signal path					
D.C. input voltage (pin 1)	$V_{1\text{-}16}$	–	4,5	–	V
Input impedance (pin 1); f = 40 kHz	$\lvert Z_{i1}\rvert$	35	–	–	kΩ
D.C. output voltage (pin 6)	$V_{6\text{-}16}$	2,4	2,8	–	V
Output resistance (pin 6)	R_{o6}		low-ohmic		
Voltage gain (V_6/V_1)	$G_{v6/1}$	0	0,5	1	dB
–3 dB point of low-pass filter	$f_{(-3dB)}$	–	70	–	kHz
Sensitivity for THD < 0,5% (peak-to-peak value)	$V_{i(p\text{-}p)}$	1,2	1,8	–	V
Residual interference pulse after suppression (see Fig. 3); pin 7 to ground; $V_{i(tr)M}$ = 100 mV; (peak-to-peak value)	$V_{6\text{-}16(p\text{-}p)}$	–	–	3	mV
Interference suppression at R13 = 0; notes 5 and 6; $V_{i(rms)}$ = 30 mV; f = 19 kHz (sinewave); $V_{i(tr)M}$ = 60 mV; f_r = 400 Hz	α_{int}	20	30	–	dB
Interference processing					
Input signal at pin 1; output signal at pin 10					
Suppression pulse threshold voltage; control function OFF (pin 9 connected to pin 12); r.m.s. value; note 1					
measured with sinewave input signal f = 120 kHz; $-V_{10\text{-}9} > 1$ V at R13 = 0 Ω	$V_{i(tr)rms}$	8	11	14	mV
at R13 = 2,7 kΩ	$V_{i(tr)rms}$	18	28,5	40	mV
voltage difference for safe triggering/ non-triggering (r.m.s. value)	$\Delta V_{i(rms)}$	–	1	–	mV
measured with interference pulses f = 400 Hz (see Fig. 3); peak value at R13 = 0 Ω	$V_{i(tr)M}$	–	19	–	mV
at R13 = 2,7 kΩ	$V_{i(tr)M}$	–	45	–	mV
Suppression pulse duration (note 2)	t_s	24	27	30	μs

parameters	symbol	min.	typ.	max.	unit
Noise threshold feedback control (notes 1 and 3)					
Noise input voltage (r.m.s. value) f = 120 kHz sinewave					
for $V_{12\text{-}9}$ = 300 mV					
at R13 = 0 Ω	$V_{ni(rms)}$	2,3	3,3	4,3	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	8,2	–	mV
for $V_{12\text{-}9}$ = 425 mV ($V_{i(tr)O}$ + 3 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	–	7,3	–	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	16,5	–	mV
for $V_{12\text{-}9}$ = 560 mV ($V_{i(tr)O}$ + 20 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	33	45	57	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	107	–	mV
Amplification control voltage by interference intensity (note 4) $V_{i(rms)}$ = 50 mV; f = 19 kHz; $V_{i(tr)M}$ = 300 mV; r.m.s. value					
at repetition frequency f_r = 1 kHz	$V_{o6(rms)}$	49	–	56	mV
at repetition frequency f_r = 16 kHz	$V_{o6(rms)}$	45	–	65	mV

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Notes to application information

1. The interference suppression and noise feedback control thresholds can be determined by R13 or a capacitive voltage divider at the input of the high-pass filter and they are defined by the following formulae:
   $V_{i(tr)} = (1 + R13/R_S) \times V_{i(tr)O}$ in which $R_S = 2\ k\Omega$;
   $V_{ni} = (1 + R13/R_S) \times V_{niO}$ in which $R_S = 2\ k\Omega$.
2. The suppression pulse duration is determined by C11 = 2,2 nF and R11 = 6,8 kΩ.
3. The characteristic of the noise feedback control is determined by R12 (and R10).
4. The feedback control of the interference suppression threshold at higher repetition frequencies is determined by R10 (and R12).
5. The 19 kHz generator can be adjusted with $R_{7\text{-}16}$ (and $R_{7\text{-}8}$). Adjustment is not required if components with small tolerances are used e.g. $\Delta R < 1\%$ and $\Delta C < 2\%$.
6. Measuring conditions:
   The peak output noise voltage ($V_{no\ m}$, CCITT filter) shall be measured at the output with a deemphazing time T = 50 μs (R = 5 kΩ, C = 10 nF); the reference value of 0 dB is $V_{o\ int}$ with the 19 kHz generator short-circuited (pin 7 grounded).

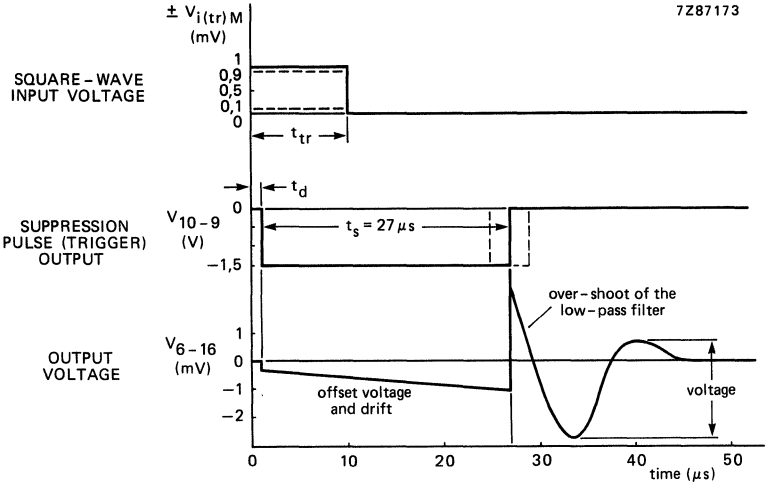


Fig. 3 Measuring signal for interference suppression; at the input (pin 1) a square-wave is applied with a duration of t_{tr} = 10 μs and with rise and fall times $t_r = t_f$ = 10 ns.

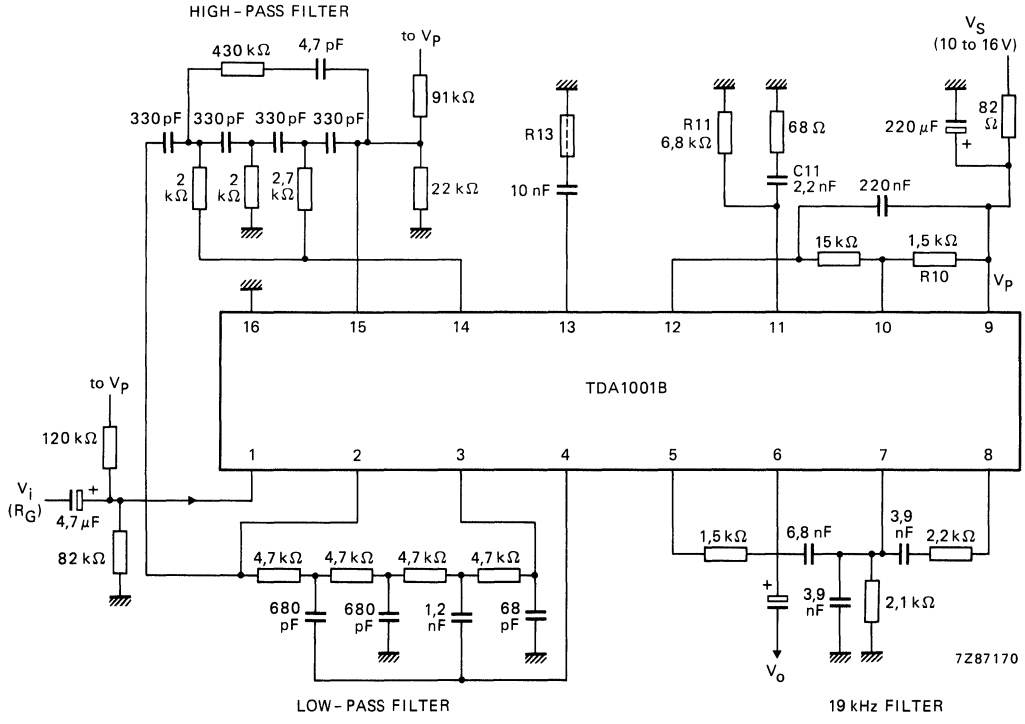


Fig. 4 Application circuit diagram.

FM Mixer Stage | TDA1571T

GENERAL DESCRIPTION

The TDA1571T is a monolithic integrated circuit which, due to the universal design, can be used in various applications such as:

- **Mixer**
- **Modulator**
- **Chopper**
- **AM synchronous demodulator**
- **FM quadrature detector**
- **Differential amplifier**

QUICK REFERENCE DATA

For application as a mixer in FM tuners; f_i = 98 MHz; f_{osc} = 108,7 MHz			
Supply voltage (pins 12 and 13)	V_P	typ.	15 V
Total supply current (from V_S)	I_S	typ.	6,5 mA
Input admittance			
at pins 2 and 7 for f = 98 MHz	y_{11}	typ.	3,8 + j5 mS
at pins 3 and 5 for f = 108,5 MHz	y_{11}	typ.	2,3 + j8 mS
Mixer gain	G_{mix}	typ.	19,5 dB
Mixer noise figure	F_{mix}	typ.	6,5 dB
I.F. suppression	α_{if}	typ.	40 dB
Oscillator suppression at the input	α_{osc}	typ.	46 dB
Supply voltage range (pins 12 and 13)	V_P		4 to 25 V
Operating ambient temperature range	T_{amb}		−30 to +80 °C

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO-16; SOT-109A).

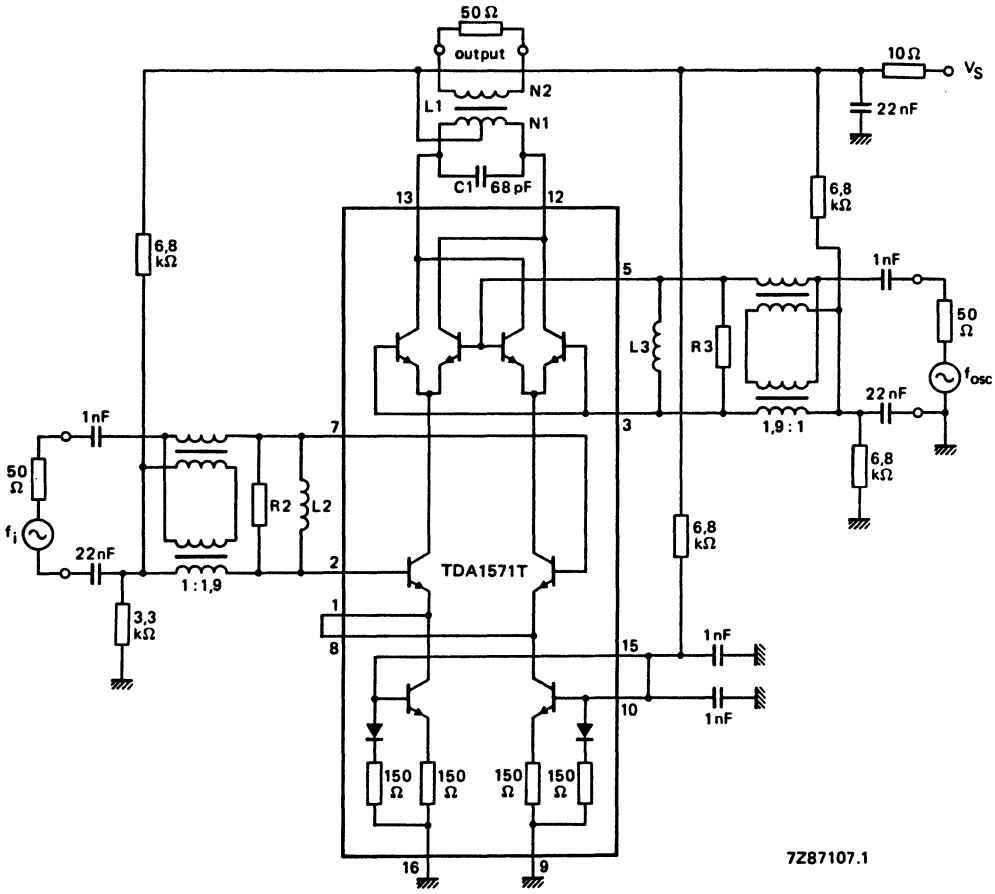


Fig. 1 Application circuit diagram of the TDA1571T used as a FM mixer; also used as test circuit for the characteristics.

Data for coil L1: N1 = 2 x 7 turns CuL (0,18 mm) on coil former
N2 = 1 turn Cul (0,18 mm) on coil former
$Q_o = 78$

L2, R2, L3 and R3 are selected for minimum reflection
$r < 0.03$; R2 = R3 = 1 kΩ

N.B.: Unused pins should be grounded.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages (pins 12 and 13)	$V_P = V_{12-9} = V_{13-16}$	max.	40 V
Voltage at pins 2 and 7	$V_{2-9} = V_{7-16}$	max.	18 V
Voltage at pins 3 and 5	$V_{3-2} = V_{5-7}$	max.	18 V
Voltage at pins 3 and 5	$V_{3-9} = V_{5-16}$	max.	23 V
Voltage at pins 12 and 13	$V_{12-3} = V_{13-5}$	max.	18 V
Voltage between pins 3 and 5	$\pm V_{3-5}$	max.	6 V
Voltage at pins 2 and 7	$-V_{2-1} = -V_{7-8}$	max.	6 V
Current on all pins	I_n	max.	10 mA
Total power dissipation	P_{tot}	max.	700 mW
Storage temperature range	T_{stg}	−55 to	+150 °C
Operating ambient temperature range	T_{amb}	−30 to	+80 °C

CHARACTERISTICS

f_i = 98 MHz; f_{osc} = 108,7 MHz with $R_S = R_L$ = 50 Ω; oscillator amplitude P_{osc} = −14 dBm; T_{amb} = 25 °C; measured in test circuit in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_S	–	15	–	V
Total supply current	I_S	–	6,5	–	mA
D.C. supply current output stage (pins 12 and 13)	I_P	–	2	–	mA
Input admittance					
at pins 2 and 7 for f = 98 MHz	y_{11}	–	3,8 + j5	–	mS
at pins 3 and 5 for f = 108,7 MHz	y_{11}	–	2,3 + j8	–	mS
Output admittance at pins 12 and 13 for f = 108,7 MHz	y_{22}	–	0,001 + j0,24	–	mS
Conversion transconductance of mixer	$\lvert y_{21} \rvert$	–	11	–	mS
Mixer gain	G_{mix}	–	19,5	–	dB
Mixer noise figure at R_S' = 200 Ω	F_{mix}	–	6,5	–	dB
I.F. suppression at an input signal amplitude P_i = −60 dBm	α_{if}	–	40	–	dB
Oscillator suppression					
at the input	$\alpha_{osc\ i}$	–	46	–	dB
at the i.f. output	$\alpha_{osc\ if}$	–	38	–	dB

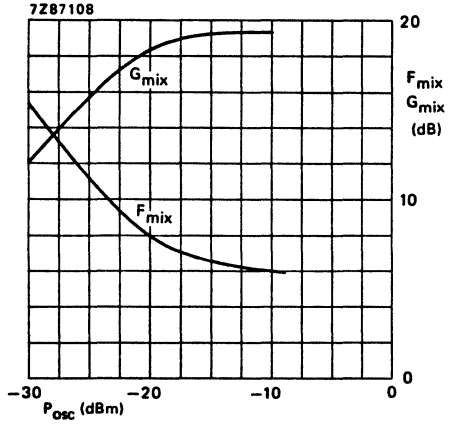


Fig. 2 Mixer gain (G_{mix}) and mixer noise figure (F_{mix}) at R_S' = 200 Ω as a function of the oscillator amplitude (P_{osc}).

GENERAL DESCRIPTION

The TDA1574 is a monolithic integrated FM tuner circuit designed for use in the r.f./i.f. section of car radios and home-receivers. The circuit comprises a mixer, oscillator and a linear i.f. amplifier for signal processing, plus the following additional features.

Features

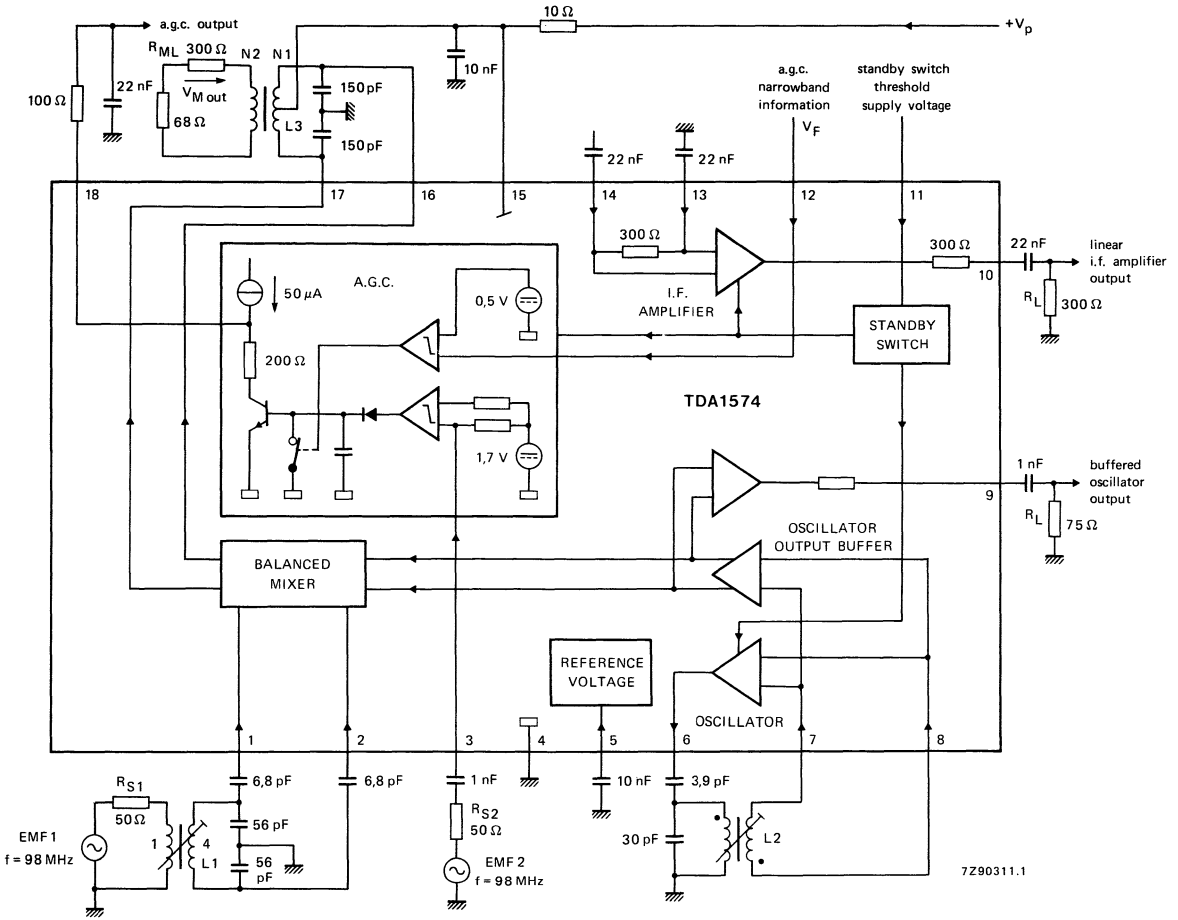
- Keyed automatic gain control (a.g.c.)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

Supply voltage range (pin 15)	V_P	7 to 16	V
Mixer input bias voltage (pins 1 and 2)	$V_{1,2-4}$	typ. 1	V
noise figure	NF	typ. 9	dB
Oscillator output voltage (pin 6)	V_{6-4}	typ. 2	V
output admittance at pin 6 for f = 108,7 MHz	Y22	typ. 1,5 + j2	mS
Oscillator output buffer			
D.C. output voltage (pin 9)	V_{9-4}	typ. 6	V
Total harmonic distortion	THD	typ. −15	dBC
Linear i.f. amplifier output voltage (pin 10)	V_{10-4}	typ. 3,5	V
noise figure at R_S = 300 Ω	NF	typ. 6,5	dB
Keyed a.g.c. output voltage range (pin 18)	V_{18-4}	0,5 to V_P−0,3	V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).



Coil data

L1: TOKO MC-108, 514HNE-150023S14; L = 0,078 μH
L2: TOKO MC-111, E516HNS-200057; L = 0,08 μH
L3: TOKO coil set 7P, N1 = 5,5 + 5,5 turns, N2 = 4 turns

Fig. 1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit is a double balanced multiplier with a preamplifier (common base input) to obtain a large signal handling range and a low oscillator radiation.

Oscillator

The oscillator circuit is an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tanh-transfer-function to obtain low order 2nd harmonics.

Linear i.f. amplifier

The i.f. amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed a.g.c.

The a.g.c. processor combines narrow- and wideband information via an r.f. level detector, a comparator and an ANDing stage. The level dependent, current sinking output has an active load which sets the a.g.c. threshold.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15-4}$	max.	18	V
Mixer output voltage (pins 16 and 17)	$V_{16,17-4}$	max.	35	V
Standby switch input voltage (pin 11)	V_{11-4}	max.	23	V
Reference voltage (pin 5)	V_{5-4}	max.	7	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to + 150		°C
Operating ambient temperature range	T_{amb}	−40 to + 85		°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}amb}$	=	80	K/W

Note

All pins are short-circuit protected to ground.

CHARACTERISTICS

$V_P = V_{15-4} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15-4}$	7	–	16	V
Supply current (except mixer)	$I_P = I_{15}$	16	23	30	mA
Reference voltage (pin 5)	V_{5-4}	4,0	4,2	4,4	V
Mixer					
D.C. characteristics					
Input bias voltage (pins 1 and 2)	$V_{1,2-4}$	–	1	–	V
Output voltage (pins 16 and 17)	$V_{16,17-4}$	4	–	35	V
Output current (pin 16 + pin 17)	$I_{16} + I_{17}$	–	4,5	–	mA
A.C. characteristics (f_i = 98 MHz)					
Noise figure	NF	–	9	–	dB
Noise figure including transforming network	NF	–	11	–	dB
3rd order intercept point	$EMF1_{IP3}$	–	115	–	dBμV
Conversion power gain					
$10 \log \frac{4\ (V_{M(out)}\ 10{,}7\ MHz)^2}{(EMF1\ 98\ MHz)^2} \times \frac{R_{S1}}{R_{ML}}$	G_P	–	14	–	dB
Input resistance (pins 1 and 2)	$R_{1,2-4}$	–	12	–	Ω
Output capacitance (pins 16 and 17)	$C_{16,17}$	–	13	–	pF
Oscillator					
D.C. characteristics					
Input voltage (pins 7 and 8)	$V_{7,8-4}$	–	1,3	–	V
Output voltage (pin 6)	V_{6-4}	–	2	–	V
A.C. characteristics (f_{osc} = 108,7 MHz)					
Residual FM (Bandwidth 300 Hz to 15 kHz); de-emphasis = 50 μs	Δf	–	2,2	–	Hz

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parameter	symbol	min.	typ.	max.	unit
Linear i.f. amplifier					
D.C. characteristics					
Input bias voltage (pin 13)	V_{13-4}	–	1,2	–	V
Output voltage (pin 10)	V_{10-4}	–	3,5	–	V
A.C. characteristics (f_i = 10,7 MHz)					
Input impedance					
	R_{14-13}	240	300	360	Ω
	C_{14-13}	–	13	–	pF
Output impedance					
	R_{10-4}	240	300	360	Ω
	C_{10-4}	–	3	–	pF
Voltage gain					
$20 \log \frac{V_{10-4}}{V_{14-13}}$	G_{VIF}	27	30	–	dB
T_{amb} = −40 to + 85 °C	ΔG_{VIF}	–	0	–	dB
1 dB compression point (r.m.s. value)					
at V_P = 8,5 V	$V_{10-4rms}$	–	900	–	mV
at V_P = 7,5 V	$V_{10-4rms}$	–	500	–	mV
Noise figure					
at R_S = 300 Ω	NF	–	6,5	–	dB
Keyed a.g.c.					
D.C. characteristics					
Output voltage range (pin 18)	V_{18-4}	0,5	–	V_P−0,3	V
A.G.C. output current					
at I_3 = ϕ or V_{12-4} = 450 mV; V_{18-4} = $V_P/2$	$-I_{18}$	25	50	100	μA
at V_{3-4} = 2 V and V_{12-4} = 1 V; V_{18-4} = V_{15-4}	I_{18}	2	–	5	mA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Narrowband threshold					
at V_{3-4} = 2 V; V_{12-4} = 550 mV	V_{18-4}	–	–	1	V
at V_{3-4} = 2 V; V_{12-4} = 450 mV	V_{18-4}	V_P–0,3	–	–	V
A.C. characteristics (f_i = 98 MHz)					
Input impedance					
	R_{3-4}	–	4	–	kΩ
	C_{3-4}	–	3	–	pF
Wideband threshold (r.m.s. value) (see figures 2, 3, 4 and 5)					
at V_{12-4} = 0,7 V; $V_{18-4} = V_P/2$; I_{18} = 0	$EMF2_{rms}$	–	19	–	mV
Oscillator output buffer (pin 9)					
D.C. output voltage	V_{9-4}	–	6,0	–	V
Oscillator output voltage (r.m.s. value)					
at $R_L = \infty$	V_{9-4rms}	–	110	–	mV
at R_L = 75 Ω	V_{9-4rms}	25	–	–	mV
D.C. output impedance	R_{9-15}	–	2,5	–	kΩ
Signal purity					
Total harmonic distortion	THD	–	–15	–	dBC
Spurious frequencies					
at EMF1 = 1 V; R_{S1} = 50 Ω	f_S	–	–35	–	dBC
Electronic standby switch (pin 11)					
Oscillator; linear i.f. amplifier; a.g.c.					
at T_{amb} = –40 to + 85 °C					
Input switching voltage					
for threshold ON; $V_{18-4} = \geqslant V_P$–3 V	V_{11-4}	0	–	2,3	V
for threshold OFF; $V_{18-4} = \leqslant$ 0,5 V	V_{11-4}	3,3	–	23	V
Input current					
at ON condition; V_{11-4} = 0 V	$-I_{11}$	–	–	150	μA
at OFF condition; V_{11-4} = 23 V	I_{11}	–	–	10	μA
Input voltage					
at $I_{11} = \phi$	V_{11-4}	–	–	4,4	V

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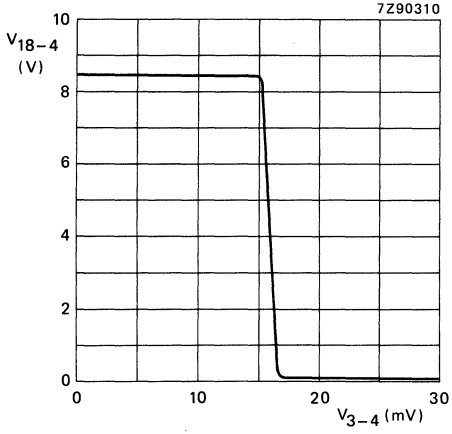


Fig. 2 Keyed a.g.c. output voltage V_{18-4} as a function of r.m.s. input voltage V_{3-4}. Measured in test circuit Fig. 1 at V_{12-4} = 0,7 V; $I_{18} = \phi$.

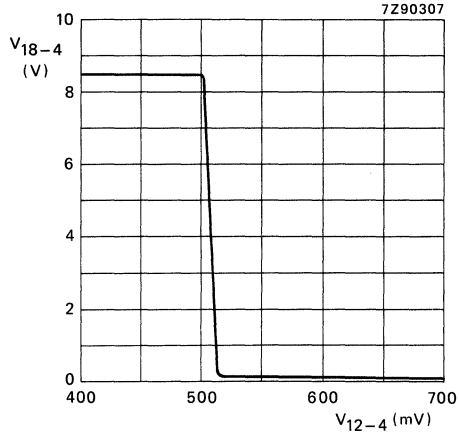


Fig. 3 Keyed a.g.c. output voltage V_{18-4} as a function of input voltage V_{12-4}. Measured in test circuit Fig. 1 at V_{3-4} = 2 V; $I_{18} = \phi$.

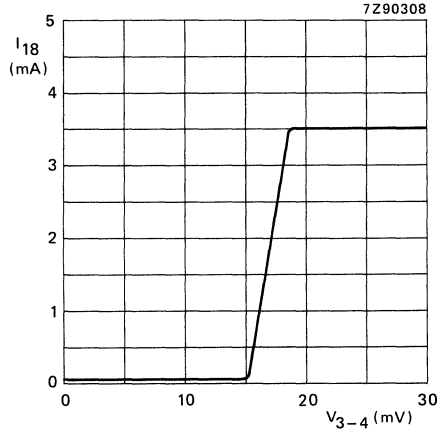


Fig. 4 Keyed a.g.c. output current I_{18} as a function of r.m.s. input voltage V_{3-4}. Measured in test circuit Fig. 1 at V_{12-4} = 0,7 V; V_{18-4} = 8,5 V.

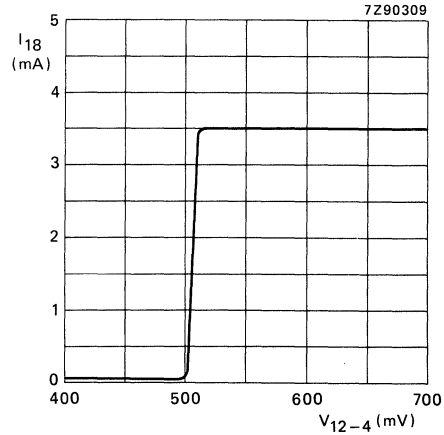
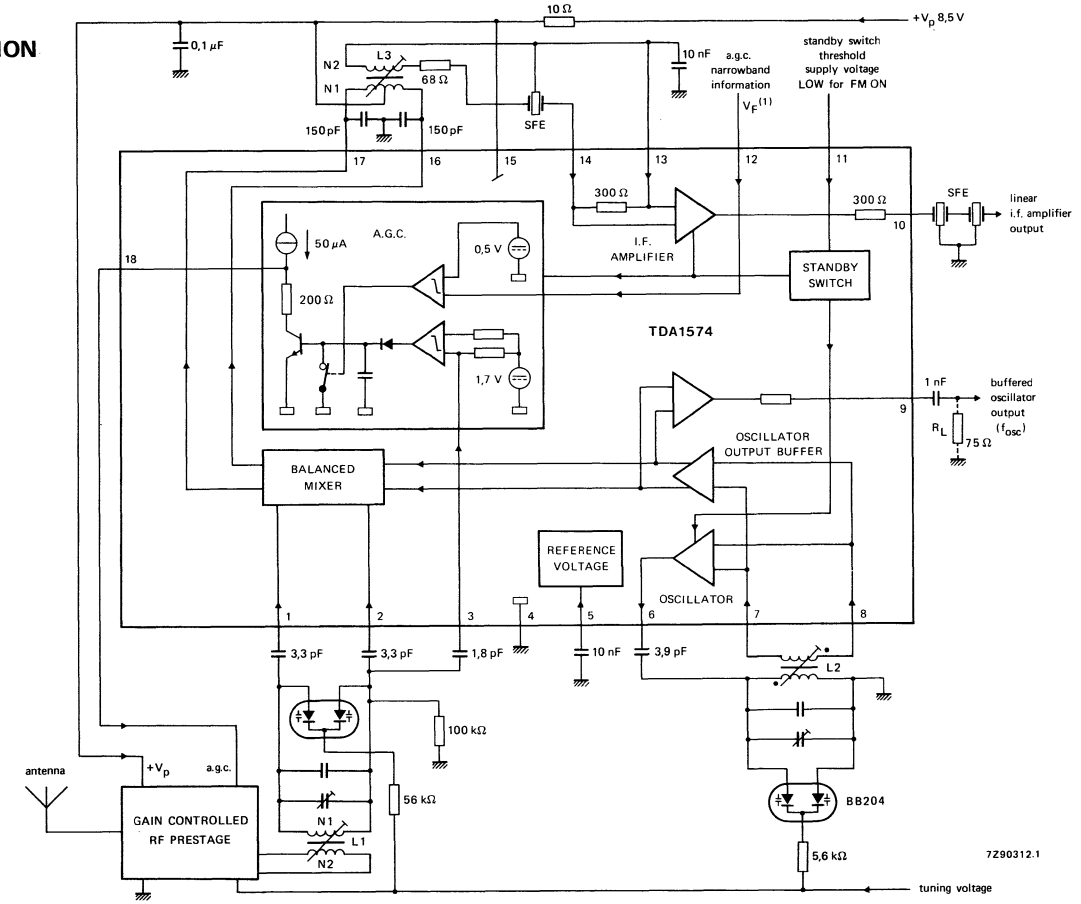


Fig. 5 Keyed a.g.c. output current I_{18} as a function of input voltage V_{12-4}. Measured in test circuit Fig. 1 at V_{3-4} = 2 V; V_{18-4} = 8,5 V.

APPLICATION INFORMATION



Coil data:

L1: TOKO MC-108, N1 = 5,5 turns, N2 = 1 turn
L2: } see Fig. 1
L3: }

(1) Field strength indication of main i.f. amplifier.

Fig. 6 TDA1574 application diagram.

FM I.F. (Quadrature Detector) TDA1576

The TDA1576 is a monolithic integrated f.m./i.f. amplifier circuit provided with the following functions:

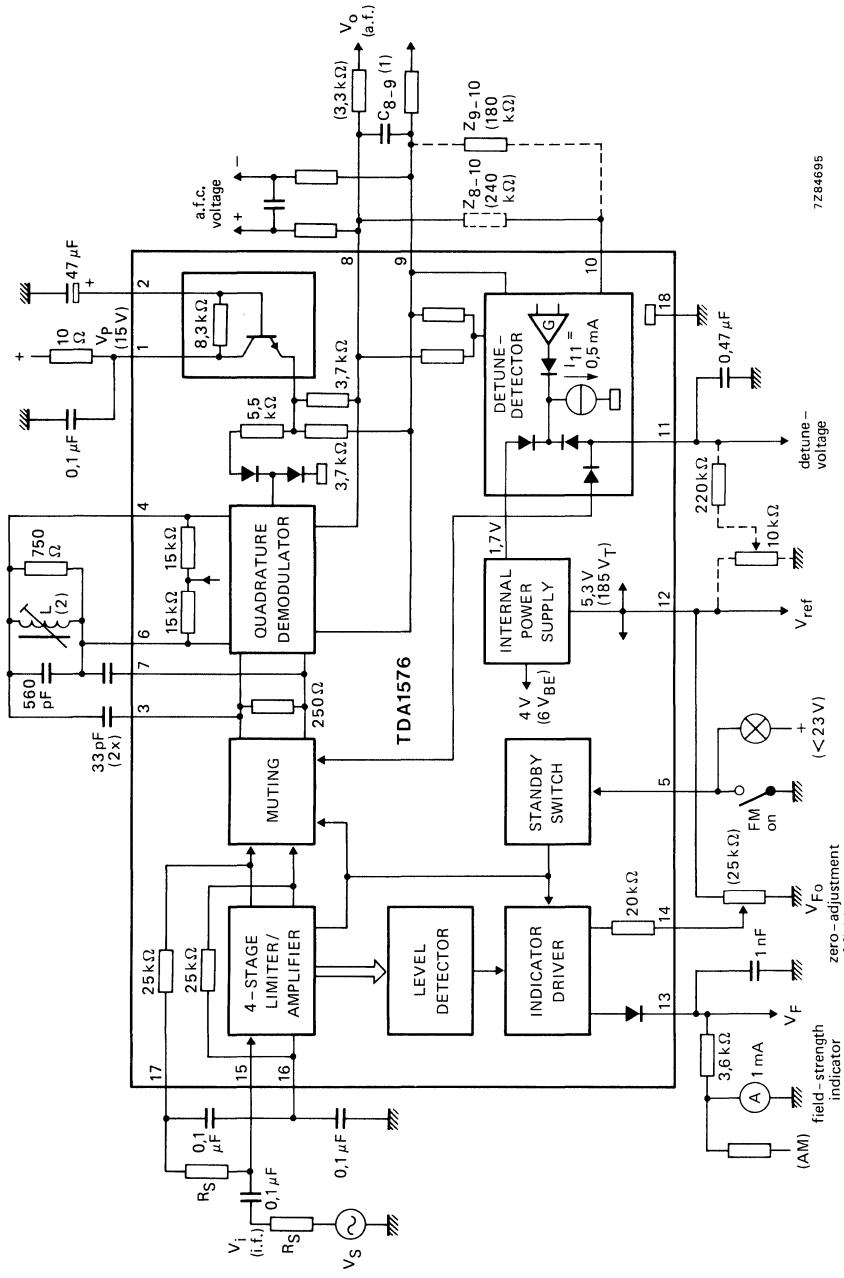
- symmetrical limiting i.f. amplifier
- symmetrical quadrature demodulator
- internal muting circuit
- symmetrical a.f.c. output
- field-strength indication output
- detune-detector
- reference voltage output
- electronic smoothing of the supply voltage
- standby on/off switching circuit.

QUICK REFERENCE DATA

f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 400 Hz; Q_L = 20; de-emphasis τ = 50 μs					
Supply voltages (pin 1)	V_P		8,5	15	V
Supply current	I_P	typ.	16	18	mA
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
A.F. output voltage	V_o	typ.	67	135	mV
Total distortion					
single tuned circuit	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio; $V_i > 1$ mV	S + N/N	typ.	76	80	dB
A.M. rejection	α	typ.	50		dB
A.F.C. offset drift	± Δf	typ.	3		kHz
		<	6		kHz
Field-strength indication range	ΔV_i	typ.	90		dB
Permissible indicator (load) current	I_L	<	2		mA
Supply voltage range (pin 1)	V_P		7,5 to 20		V
Ambient temperature range	T_{amb}		−30 to +80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102C).



(1) For de-emphasis τ = 50 μs: $C_{8\text{-}9}$ = 6,8 nF.
For stereo operation: $C_{8\text{-}9}$ = 56 pF.

(2) L = 0,38 μH; Q_o = 70; Q_L = 20; adjusted to minimum 2nd harmonic distortion (d_2); at V_i = 1 mV; coil: 6 turns CuL (0,25 mm) on coil former KAN (C).

Fig. 1 Block diagram and test circuit.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-18}$	max.	23 V
Voltages			
at pin 2	V_{2-18}	max.	V_P V
	$-V_{2-18}$	max.	0 V
at pin 5	V_{5-18}	max.	23 V
	$-V_{5-18}$	max.	0 V
at pin 12	V_{12-18}	max.	7 V
	$-V_{12-18}$	max.	0 V
at pin 13	V_{13-18}	max.	6 V
at pin 14	V_{14-18}	max.	23 V
	$-V_{14-18}$	max.	0 V
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80 K/W

CHARACTERISTICS

f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 400 Hz; R_S = 60 Ω; de-emphasis τ = 50 μs (C_{8-9} = 6,8 nF); T_{amb} = 25 °C; measured in Fig. 1, unless otherwise specified. The demodulator circuit is adjusted at minimum 2nd harmonic (d_2) distortion: V_i = 1 mV; Δf = ± 75 kHz.

Supply voltage range (pin 1)	V_P		7,5 to 20		V
		V_P = 8,5 V		V_P = 15 V	
Supply current; without load ($I_{12} = I_{13} = 0$)	I_P	typ.	16	18	mA
			10 to 23	12 to 25	mA
I.F. amplifier/detector					
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
		<	30		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
I.F. output voltage (peak-to-peak value) V_i = 1 mV; $Z_{3-18} = Z_{7-18}$ = 1 MΩ in parallel with 10 pF	$V_{3-7(p-p)}$	typ.	680		mV
I.F. output resistance	R_{3-7}	typ.	250		Ω
Detector input impedance	R_{4-6}	typ.	30		kΩ
	C_{4-6}	typ.	1		pF
Output resistance	R_8; R_9	typ.	3,7		kΩ
D.C. output voltage	$V_{8-18} = V_{9-18}$	typ.	5,5	9,8	V
A.F. output voltage; Q_L = 20	V_o	typ.	67	135	mV
			60 to 75	120 to 150	mV
Total distortion					
single tuned circuit; Q_L = 20	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio B = 250 Hz to 15 kHz; V_i > 1 mV	S + N/N	typ.	76	80	dB
A.M. rejection; V_i = 10 mV					
f.m.: f_m = 70 Hz; Δf = ± 22,5 kHz					
a.m.: f_m = 1 kHz; m = 0,3	α	typ.	54		dB*
I.F. input voltage range; α > 40 dB	V_i		0,5 to 500		mV
Hum suppression at f = 100 Hz					
$V_P = V_{1-18}$ = 100 mV r.m.s.; C_{2-18} = 47 μF	α_{100}	>	43		dB
		typ.	48		dB
A.F.C. tuning slope at Q_L = 20	$\frac{\Delta V_{8-9}}{\Delta f_o}$	typ.	8,5	17	mV/kHz
A.F.C. offset voltages; Q_L = 20					
at V_i = 1 mV	$\pm \Delta V_{8-9}$	<	100	200	mV
at V_i = 30 μV to 500 mV		typ.	25	50	mV
(reference at 1 mV and muting)	$\pm \Delta V_{8-9}$	<	50	100	mV

* Simultaneously measured.

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		V_P = 8,5 V | V_P = 15 V		
		20 μV to 600 mV		
Field-strength indication				
Indicator sensitivity; $I_{14} = 0$	V_i			
Field-strength indicator voltage				
R_{13-18} = 3,6 kΩ; $I_{14} = 0$				
$V_i = 0$	$V_F = V_{13-18}$	typ.	0	mV
		<	200	mV
V_i = 250 mV	$V_F = V_{13-18}$	typ.	3,6	V
			3,2 to 4,1	V
Available output current	$-I_{13}$	>	2	mA
Reverse voltage at the output for FM 'off'; $V_{5-18} > 3,5$ V	V_{13-18}	>	5	V
Detune-detector				
Quiescent input current; $V_{10-9} = 0$	I_{10}	typ.	20	nA
		<	100	nA
Output voltage range	V_{11-18}		1,8 to 5,0	V
Available output current	I_{11}	typ.	0,5	mA
			0,35 to 0,65	mA
Voltage gain: $\Delta V_{11}/\Delta(\pm V_{10-9})$ at I_{11} = 0,25 mA	G_v	typ.	– | 3,3	
Input offset voltage (pin 10) at V_{11-18} = 2,5 V	V_{10-9}	typ.	20	mV
Reference voltage				
Output voltage; $-I_{12}$ = 1 mA	$V_{ref} = V_{12-18}$	typ.	5,1 | 5,3	V
Available output current	$-I_{12}$	typ.	2,5	mA
Standby switch				
Required control voltage within the rated ambient temperature and supply voltage ranges				
for FM 'on'	$V_{5\ on}$	<	2	V
for FM 'off'	$V_{5\ off}$	>	3,5	V
Input switching current for FM 'on'	$-I_5$	<	100	μA

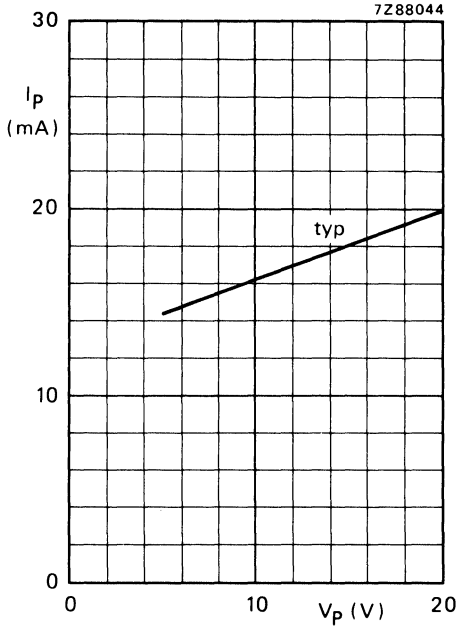


Fig. 2 Supply current consumption; without load.

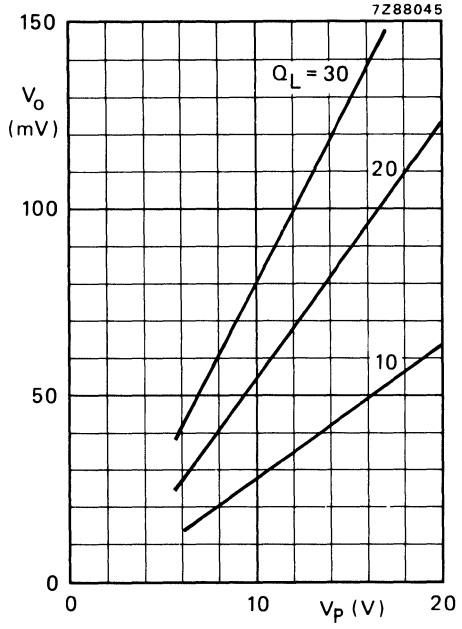


Fig. 3 A.F. output voltage; V_i = 1 mV (i.f.); $\Delta f = \pm 15$ kHz; f_m = 400 Hz; typical values.

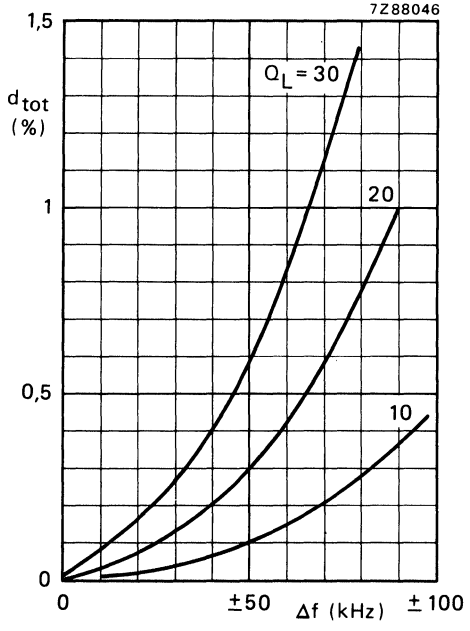


Fig. 4 Total distortion for single tuned circuit; V_i = 1 mV (i.f.); f_m = 400 Hz; adjusted at minimum 2nd harmonic distortion; typical values.

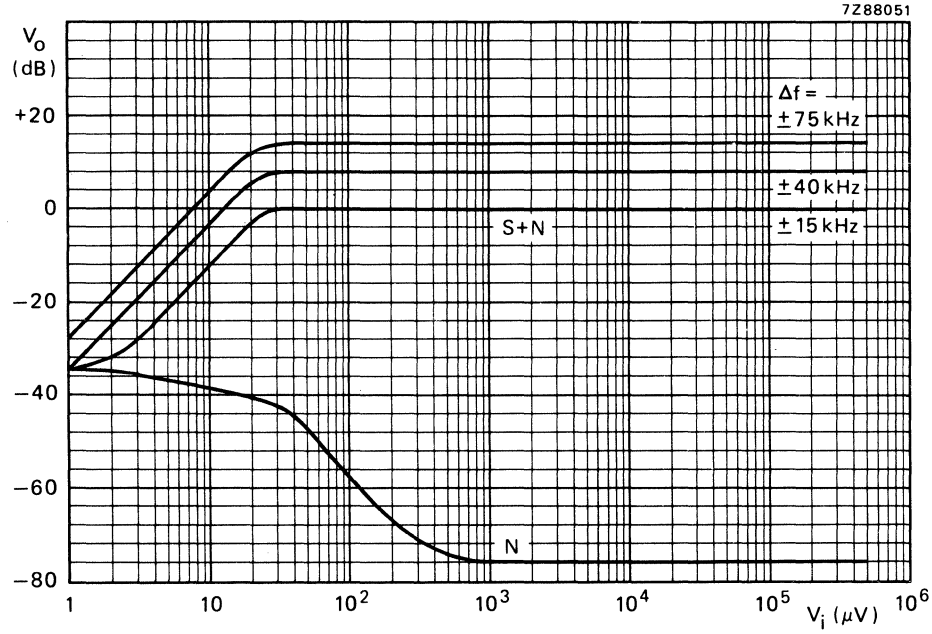


Fig. 5 A.F. output voltage level as a function of i.f. input voltage; S = signal voltage; N = noise voltage; V_P = 15 V; f_m = 400 Hz; B = 250 Hz to 16 kHz; Q_L = 20; C_{8-9} = 6,8 nF; typical values.

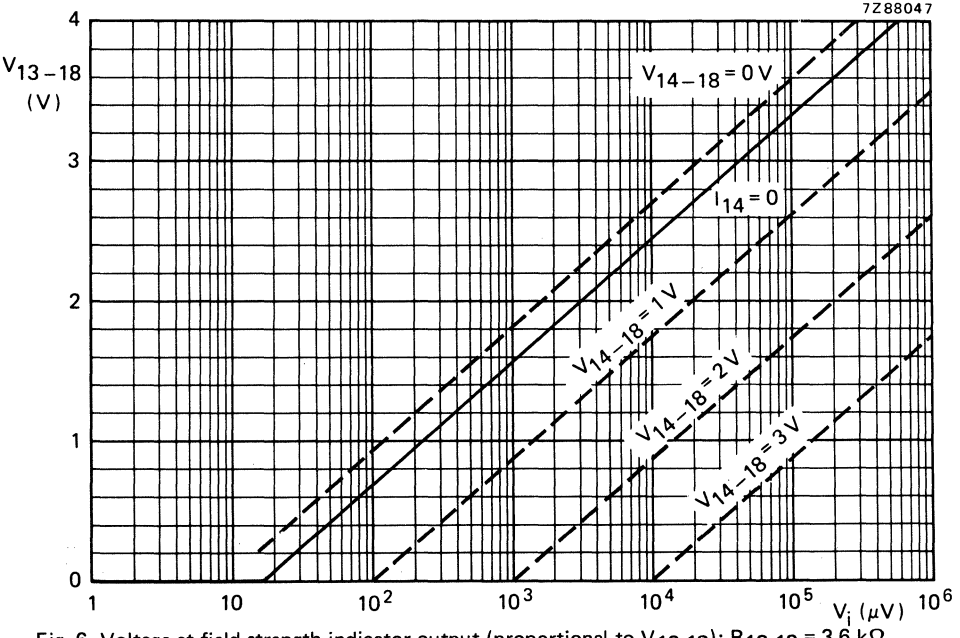


Fig. 6 Voltage at field-strength indicator output (proportional to V_{12-18}); R_{13-18} = 3,6 kΩ.

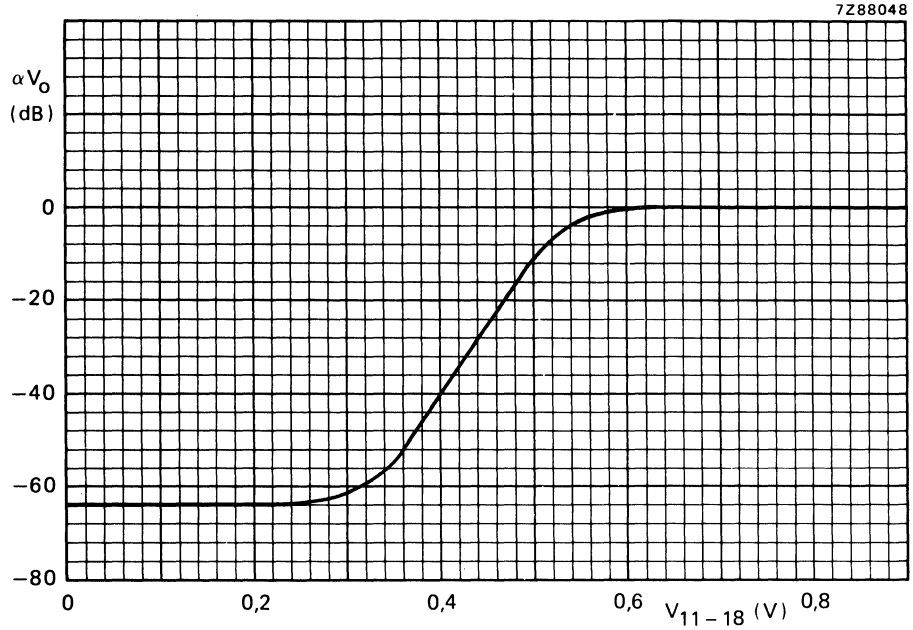


Fig. 7 Attenuation of output voltage (αV_o) as a function of the muting control voltage $V_{11\text{-}18}$.

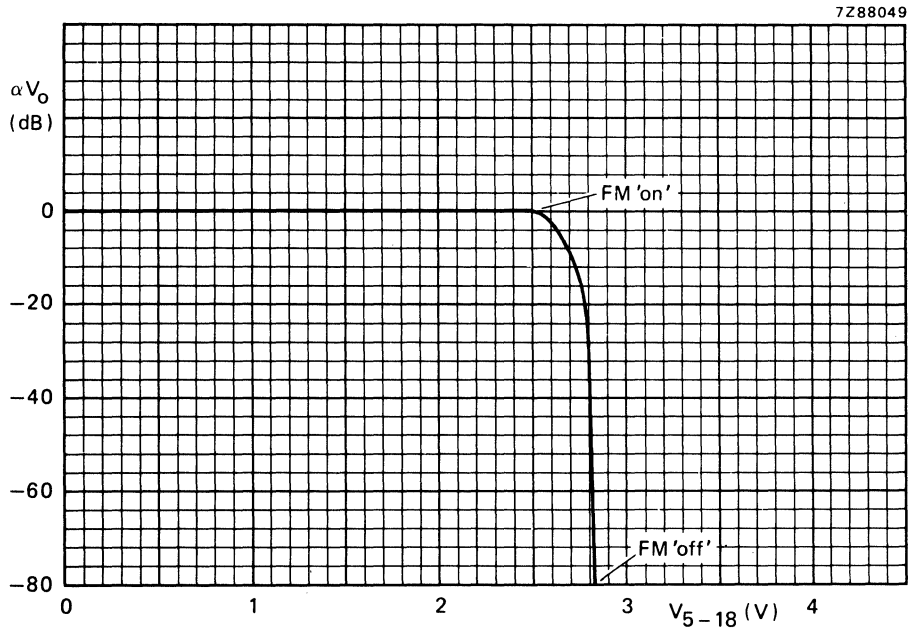
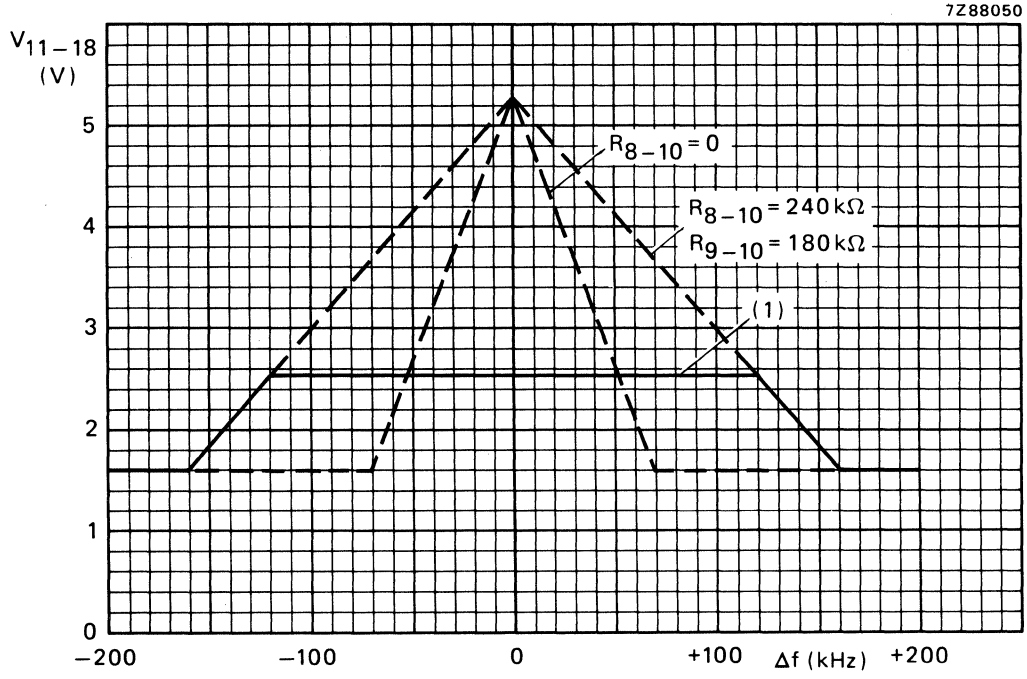


Fig. 8 FM 'on'/FM 'off' stand-by switch; attenuation of output voltage (αV_o) as a function of control voltage $V_{5\text{-}18}$.



(1) Limited by external preset ($\alpha \cdot V_{12\text{-}18}$).

Fig. 9 Detune-detector output voltage; V_P = 7,5 to 20 V; Q_L = 20.

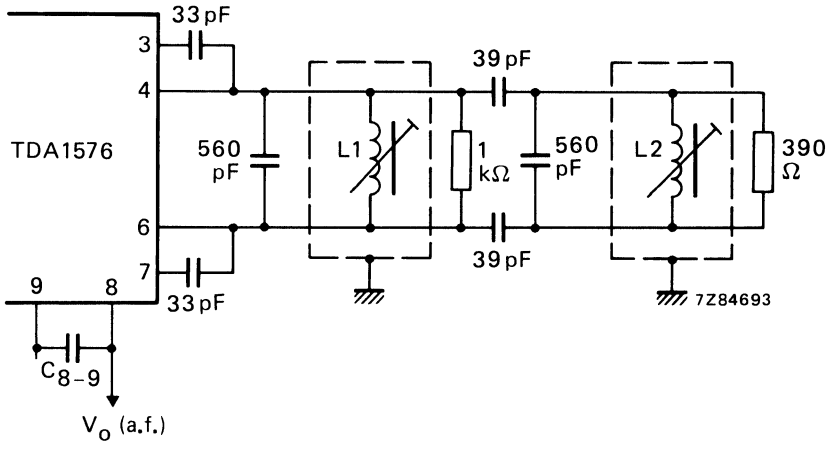


Fig. 10 Example of the TDA1576 when using a demodulator with two tuned circuits. Adjustment of the demodulator circuit is obtained with an i.f. signal which is higher than the 3 dB limiting level, L2 should be short-circuited or detuned, L1 should be adjusted to min. d_2 distortion, and then L2 to min. d_2 distortion. Coil data: L1 = L2 = 0,38 μH; Q_o = 70; coil former KAN (C).

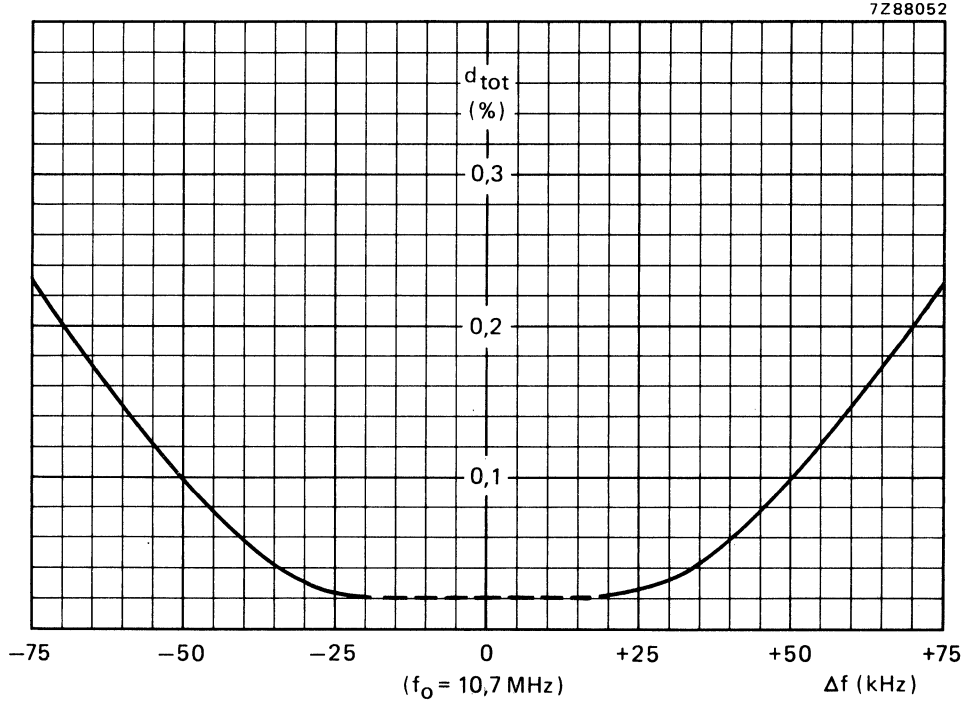
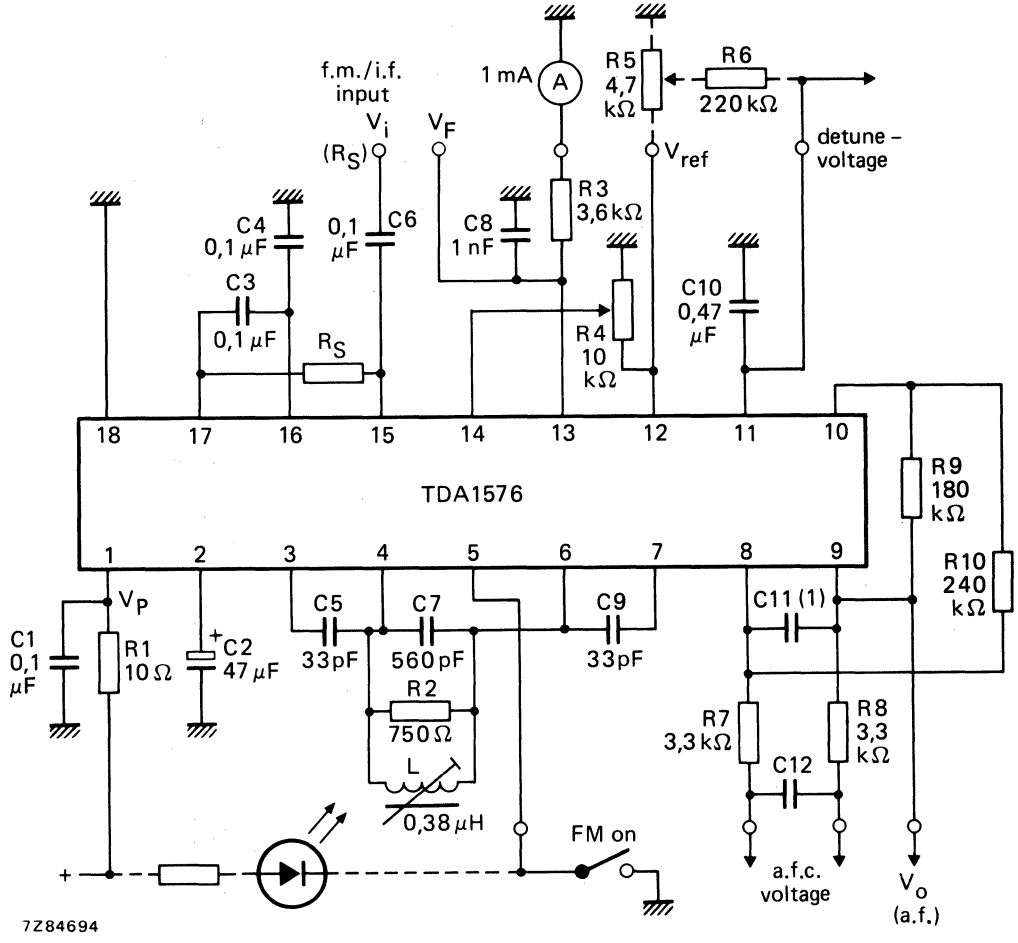


Fig. 11 Total distortion as a function of detuning; f_m = 400 Hz; C_{8-9} = 6,8 nF; $\Delta f = \pm$ 75 kHz; V_o = 330 mV for a frequency deviation $\Delta f = \pm$ 75 kHz.



(1) For mono: C11 = 6,8 nF; for stereo: C11 = 56 pF.

Fig. 12 Application example of using TDA1576.

FM I.F. Amplifier TDA1596

DESCRIPTION

The TDA provides 1596 i.f. amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for both mono and stereo reception. It may also be applied to common frontends, stereo decoders and AM receiver circuits.

FEATURES

- **Simulated ratio detection (internal, field strength + detuning – dependent voltage for dynamic AF signal muting)**
- **Mono/stereo blending and field strength indication control**
- **Three-state mode switch giving FM/FM + mute-off/FM-off**
- **Compensation of AF signal total harmonic distortion (THD)**
- **Two tuning-stop outputs for micro-computer tuning control**
- **Internal reference voltage source**
- **Built-in hum and ripple rejection circuits**

APPLICATIONS

- **FM IF systems**

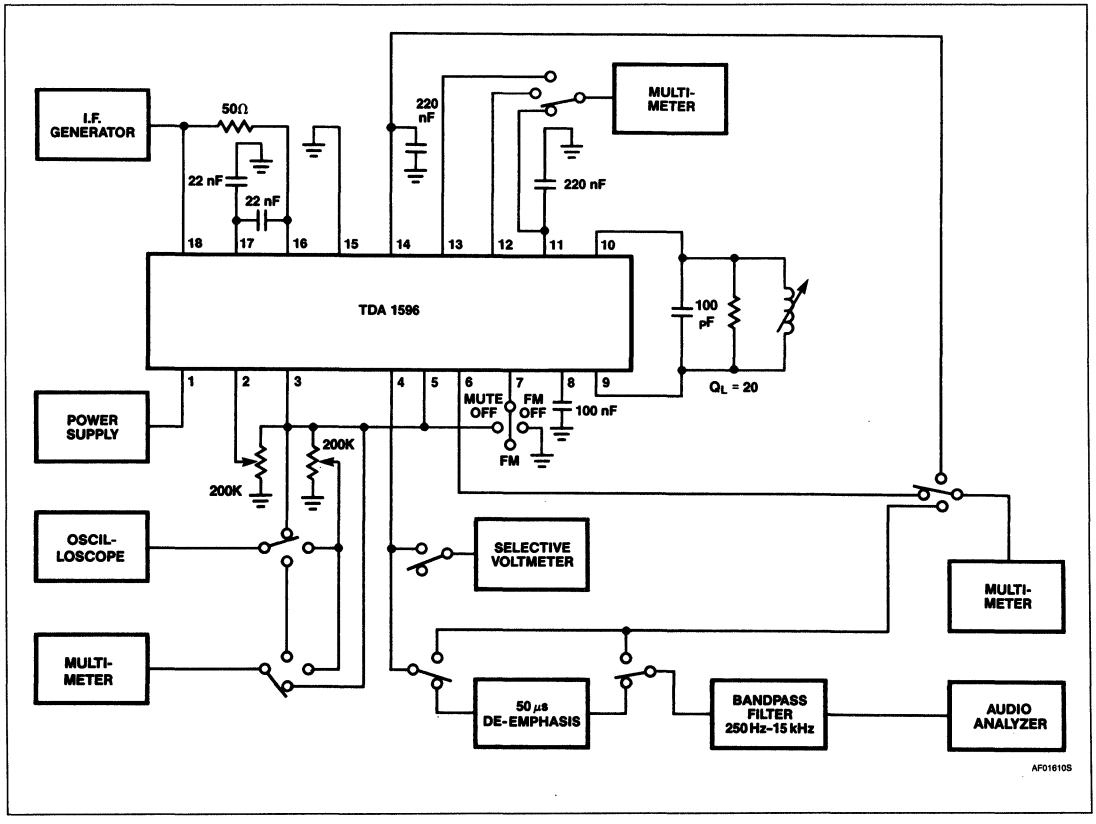
5

FM I.F. Amplifier | TDA1596

REFERENCE DATA

PARAMETER	SYMBOL	LIMITS			UNIT
		Min	Typ	Max	
Positive supply voltage range, V_{1-15}	V_p	7.5		12.0	V
Supply current at V_p = 8.5V; $I_2 = I_7$ = 0mA, I_1			18		mA
AF output voltage (r.m.s. value) for input signal $V_{18\ (rms)}$ = 10mV, V_{4-15}	(rms)		180		mV
Signal-to-noise ratio with input signal $V_{18(rms)}$ = 10mV; modulation frequency = 400Hz; deviation = 75kHz	S/N		82		dB
THD with input signal $V_{18(rms)}$ = 10mV; modulation frequency = 1kHz; deviation = 75kHz; detuning 40kHz without deemphasis; I_7 = 0mA; internal muting on	THD		0.1		%

TYPICAL TEST CIRCUIT/APPLICATION DIAGRAM



FM Radio Circuit TDA7000

DESCRIPTION

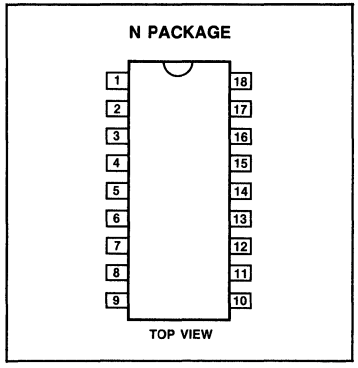
The TDA7000 is a monolithic integrated circuit for mono FM portable radios where a minimum of peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The I.F. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too-noisy input signals. Special precautions are taken to meet the radiation requirements.

FEATURES

- **R.F. input stage**
- **Mixer**
- **Local oscillator**
- **I.F. amplifier/limiter**
- **Phase demodulator**
- **Mute detector**
- **Mute switch**

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Supply voltage (pin 5)	12	V
$V_{6\text{-}5}$	Oscillator voltage (pin 6)	V_{CC}−0.5 to V_{CC}+0.5	V
	Total power dissipation	See derating curve Figure 2	
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	0 to +60	°C

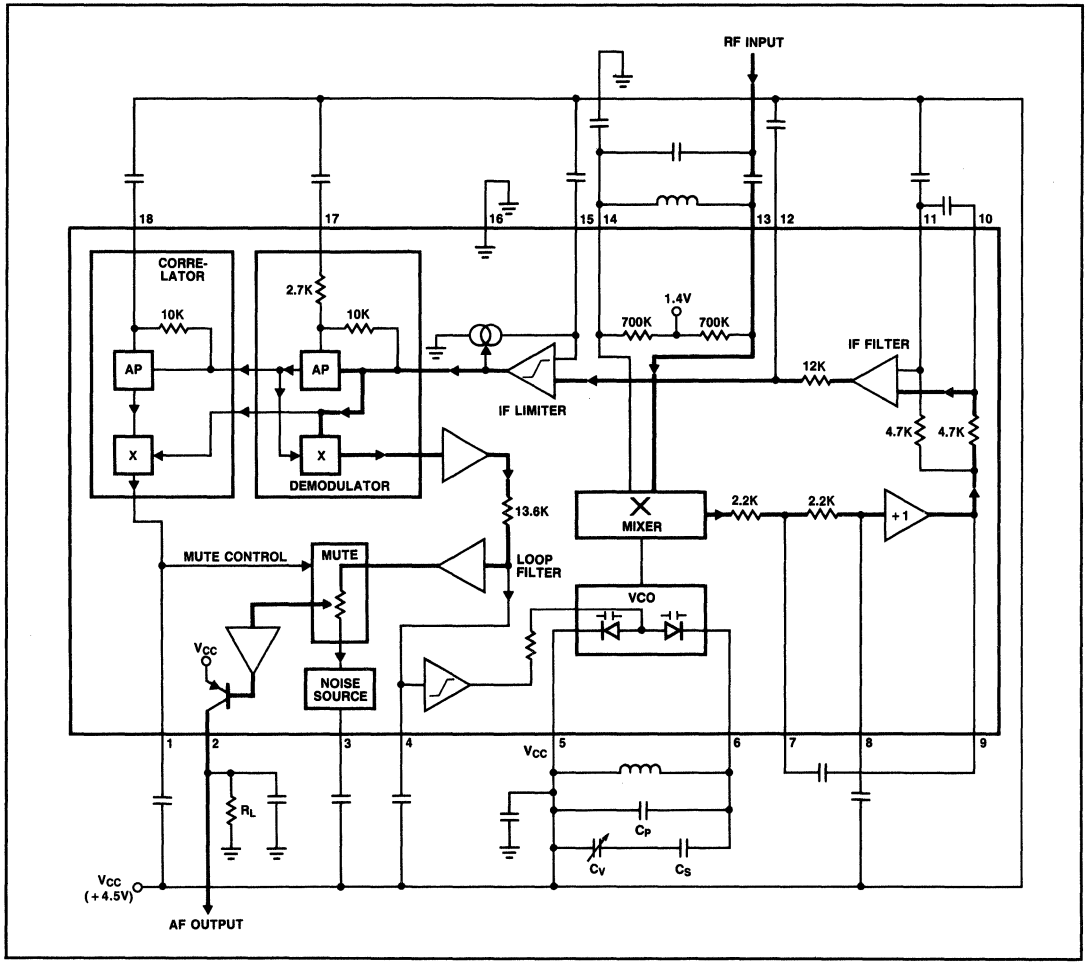
FUNCTIONAL PIN DESCRIPTION

PIN NO.	NAME AND FUNCTION
1	Muting capacitor
2	Audio frequency output
3	Noise source
4	Loop filter capacitor
5	Supply voltage
6	VCO
7	1st integrator capacitor (to pin 9)
8	2nd integrator capacitor
9	1st integrator capacitor (to pin 7)
10	IF filter capacitor (to pin 11)
11	IF filter capacitor
12	IF limiter capacitor
13	RF input
14	Mixer
15	Current source capacitor
16	Ground
17	Demodulator capacitor
18	Correlator capacitor

5

FM Radio Circuit TDA7000

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V; T_A = 25°C: measured in Figure 3; unless otherwise specified

SYMBOL AND PARAMETER		TEST CONDITION	TDA7000			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage	(Pin 5)	2.7	4.5	10	V
I_{CC}	Supply current	V_{CC} = 4.5V		8		mA
I_6	Oscillator current	(Pin 6)		280		μA
V_{14-16}	Voltage	(Pin 14)		1.35		V
I_2	Output current	(Pin 2)		60		μA
V_{2-16}	Output voltage	(Pin 2) R_L = 22 kΩ		1.3		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V; T_A = 25°C; measured in Figure 3 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ±22.5 kHz; f_m = 1 kHz; EMF = 0.2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

5

SYMBOL AND PARAMETER		TEST CONDITION	TDA7000			UNIT
			Min	Typ	Max	
EMF	Sensitivity (see Figure 2) (e.m.f. voltage)	−3 dB limiting; muting disabled		1.5		μV
		−3 dB muting		6		
		S/N = 26 dB		5.5		
EMF	Signal handling (e.m.f. voltage)	THD < 10%; Δf = ± 75 kHz		200		mV
S/N	Signal-to-noise ratio			60		dB
THD	Total harmonic distortion	Δf = ±22.5 kHz		0.7		%
		Δf = ±75 kHz		2.3		
AMS	AM suppression of output voltage	(ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ±75 kHz AM signal: f_m = 1 kHz; m = 80%		50		dB
RR	Ripple rejection	(ΔV_{CC} = 100 mV; f = 1 kHz)		10		dB
$V_{6-5(rms)}$	Oscillator voltage (r.m.s. value)	(Pin 6)		250		mV
Δf_{osc}	Variation of oscillator frequency	Supply voltage (ΔV_{CC} = 1V)		60		kHz/V
S_{+300}	Selectivity			45		dB
S_{-300}				35		
Δf_{rf}	A.F.C. range			±300		kHz
B	Audio bandwidth	ΔV_O = 3 dB measured with pre-emphasis (t = 50 μs)		10		kHz
$V_{O(rms)}$	A.F. output voltage (r.m.s. value)	R_L = 22 kΩ		75		mV
R_L	Load resistance	V_{CC} = 4.5V			22	kΩ
		V_{CC} = 9.0V			47	

NOTES:

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

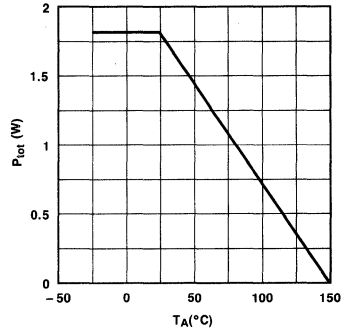


Figure 1. Power Derating Curve.

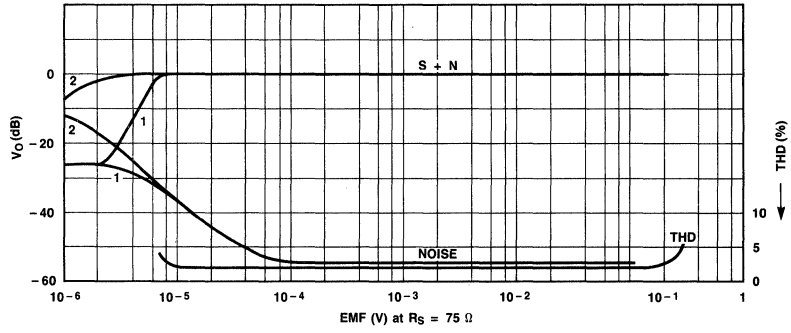


Figure 2. AF output voltage (V_O) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0dB = 75mV; f_{rf} = 96 MHz
for S + N curve: $\Delta f = \pm$ 22.5 kHz f_m = 1 kHz
for THD curve: $\Delta f = \pm$ 75 kHz f_m = 1 kHz

NOTES:
1. The muting system can be disabled by feeding a current of about 20μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

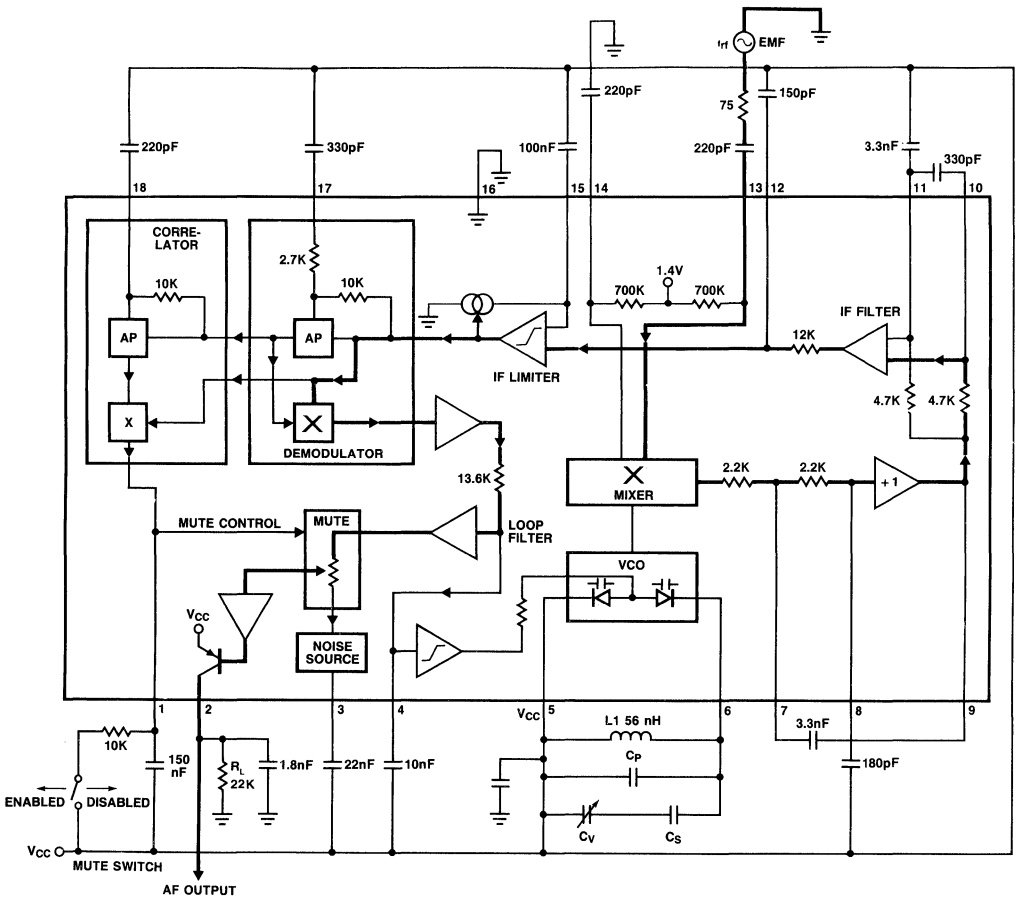


Figure 3. Test Circuit

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FM Radio Circuit (SO Package) TDA7010T

DESCRIPTION

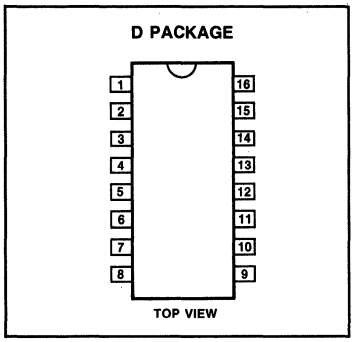
The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum of peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The I.F. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

FEATURES

- **R.F. input stage**
- **Mixer**
- **Local oscillator**
- **I.F. amplifier/limiter**
- **Phase demodulator**
- **Mute detector**
- **Mute switch**

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

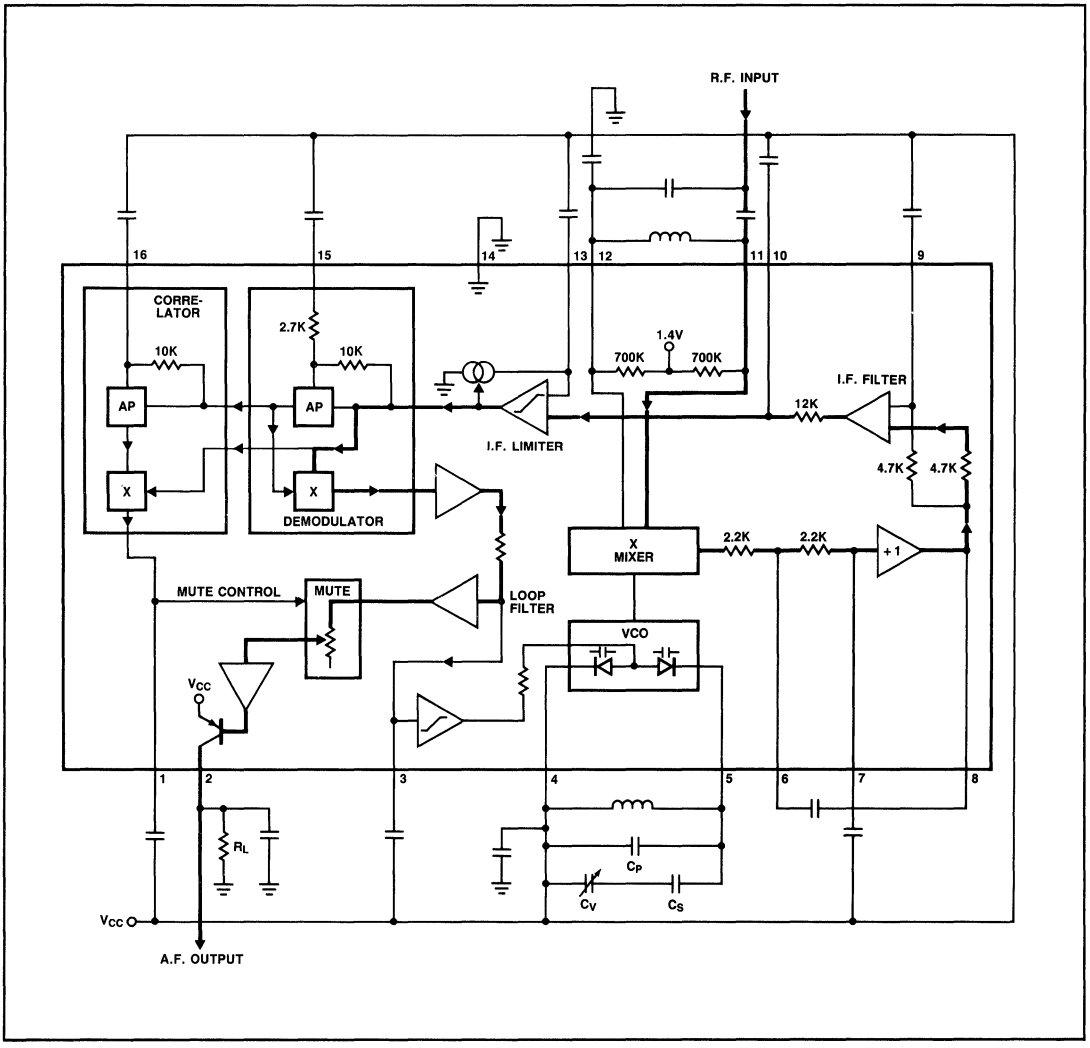
SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Supply voltage (pin 4)	12	V
$V_{6\text{-}5}$	Oscillator voltage (pin 5)	V_{CC}−0.5 to V_{CC}+0.5	V
	Total power dissipation	See derating curve Figure 2	
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	0 to +60	°C

FUNCTIONAL PIN DESCRIPTION

PIN NO.	NAME AND FUNCTION
1	Muting capacitor
2	Audio frequency output
3	Loop filter capacitor
4	Supply voltage
5	VCO
6	1st integrator capacitor (to pin 8)
7	2nd integrator capacitor
8	1st integrator capacitor (to pin 6)
9	IF filter capacitor
10	IF limiter capacitor
11	RF input
12	Mixer
13	Current source capacitor
14	Ground
15	Demodulator capacitor
16	Correlator capacitor

FM Radio Circuit (SO Package) TDA7010T

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V; T_A = 25°C: measured in Figure 3; unless otherwise specified.

SYMBOL AND PARAMETER		TEST CONDITION	TDA7010T			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage	(Pin 4)	2.7	4.5	10	V
I_{CC}	Supply current	V_{CC} = 4.5V		8		mA
I_5	Oscillator Current	(Pin 5)		280		μA
V_{12-14}	Voltage	(Pin 12)		1.35		V
I_2	Output current	(Pin 2)		60		μA
V_{2-14}	Output voltage	(Pin 2) R_L = 22 kΩ		1.3		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V; T_A =25°C; measured in Figure 3 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ±22.5 kHz; f_m = 1 kHz; EMF = 0.2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

SYMBOL AND PARAMETER		TEST CONDITION	TDA7010T			UNIT
			Min	Typ	Max	
EMF	Sensitivity (see Figure 2) (e.m.f. voltage)	−3 dB limiting; muting disabled		1.5		μV
		−3 dB muting		6		
		S/N = 26 dB		5.5		
EMF	Signal handling (e.m.f. voltage)	THD < 10%; Δf = ± 75 kHz		200		mV
S/N	Signal-to-noise ratio			60		dB
THD	Total harmonic distortion	Δf = ±22.5 kHz Δf = ±75 kHz		0.7 2.3		% %
AMS	AM suppression of output voltage	(ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ±75 kHz AM signal: f_m = 1 kHz; m = 80%		50		dB
RR	Ripple rejection	(ΔV_{CC} = 100 mV; f = 1 kHz)		10		dB
$V_{5-4(rms)}$	Oscillator voltage (r.m.s. value)	(Pin 5)		250		mV
Δf_{osc}	Variation of oscillator frequency	Supply voltage (ΔV_{CC} = 1V)		60		kHz/V
S_{+300}	Selectivity			43		dB
S_{-300}				28		
Δf_{rf}	A.F.C. range			±300		kHz
B	Audio bandwidth	ΔV_O = 3 dB measured with pre-emphasis (t = 50 μs)		10		kHz
$V_{O(rms)}$	A.F. output voltage (r.m.s. value)	R_L = 22 kΩ		75		mV
R_L	Load resistance	V_{CC} = 4.5V			22	kΩ
		V_{CC} = 9.0V			47	

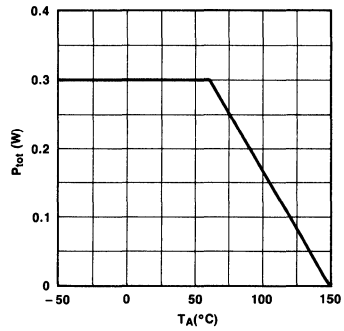


Figure 1. Power Derating Curve

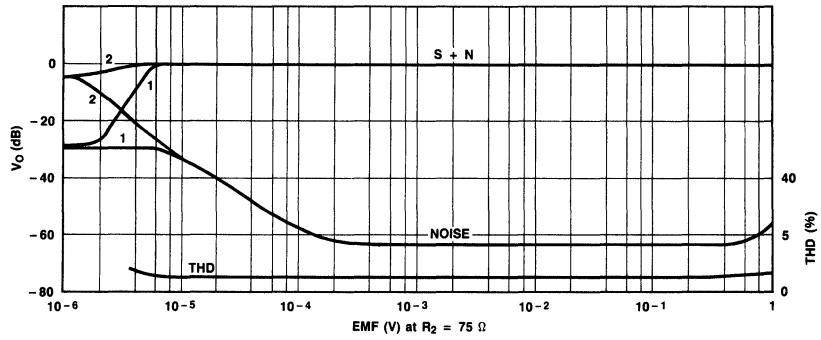


Figure 2. AF output voltage (V_O) and total harmonic distortion (THD) as a function of the E.M.F. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75mV; f_{rf} = 96 MHz
for S + N curve: $\Delta f = \pm$ 22.5 kHz: f_m = 1 kHz
for THD curve: $\Delta f = \pm$ 75 kHz: f_m = 1 kHz

NOTE:
1. The multing system can be disabled by feeding a current of about 20 μA into pin 1.

FM Radio Circuit (SO Package) TDA7010T

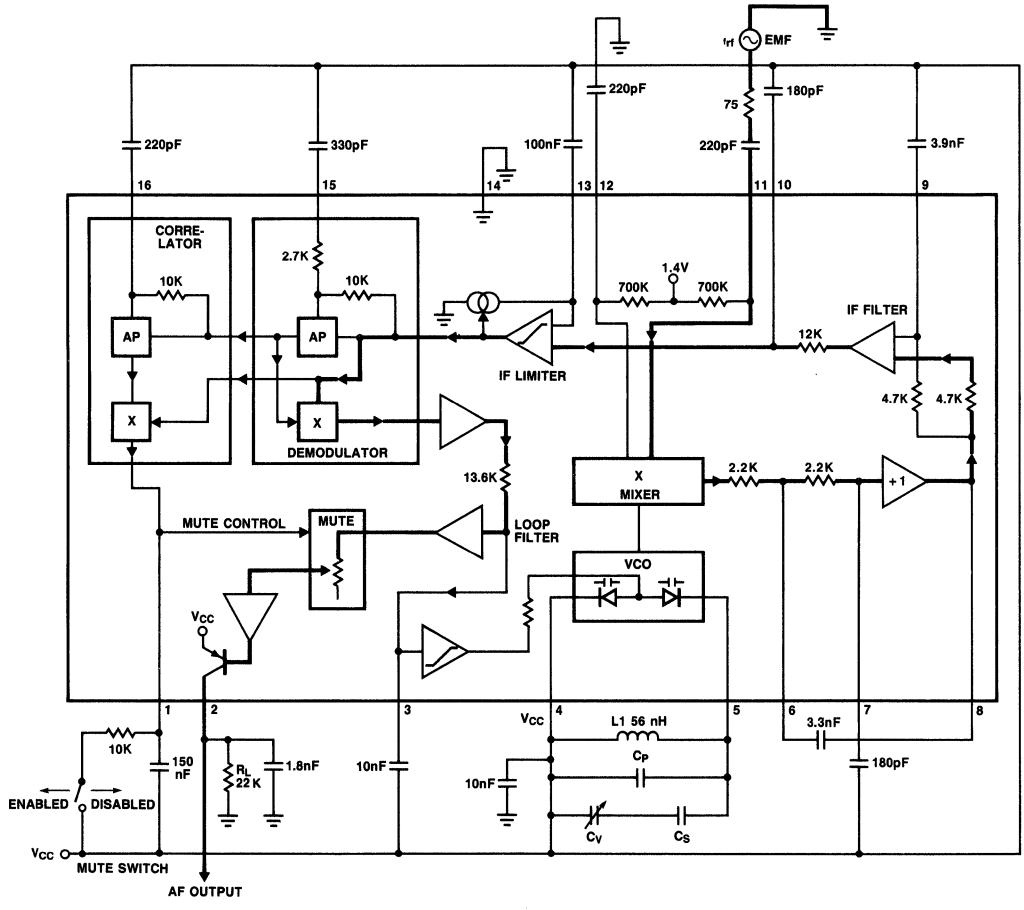


Figure 3. Test Circuit

FM Radio Circuit | TDA7020T

GENERAL DESCRIPTION

The TDA7020T integrated circuit is for FM portable radios, stereo as well as mono, where a minimum periphery is important in terms of small dimensions and low cost. The IC has a FLL (Frequency Locked Loop) system with an intermediate frequency of 76 kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant circuit of the oscillator. Interstation-noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MPX signal is required to avoid noise when receiving stereo. 50 kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field-strength detector enables field-strength dependent channel separation control.

The TDA7020T includes the following functions:

- RF input stage
- Mixer
- Local oscillator
- IF amplifier/limiter
- Frequency detector
- Mute circuit
- Loop amplifier
- Internal reference circuit
- LF amplifier for:
  - mono earphone amplifier or
  - MPX filter
- field-strength dependent channel separation control facility

5

QUICK REFERENCE DATA

Supply voltage range (pin 4)	V_P		1,8 to 6 V
Supply current at V_P = 3 V	I_P	typ.	6,3 mA
RF input frequency range	f_{rf}		1,5 to 110 MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ.	3 μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ.	200 mV
AF output voltage	V_o	typ.	90 mV

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO-16; SOT-109A).

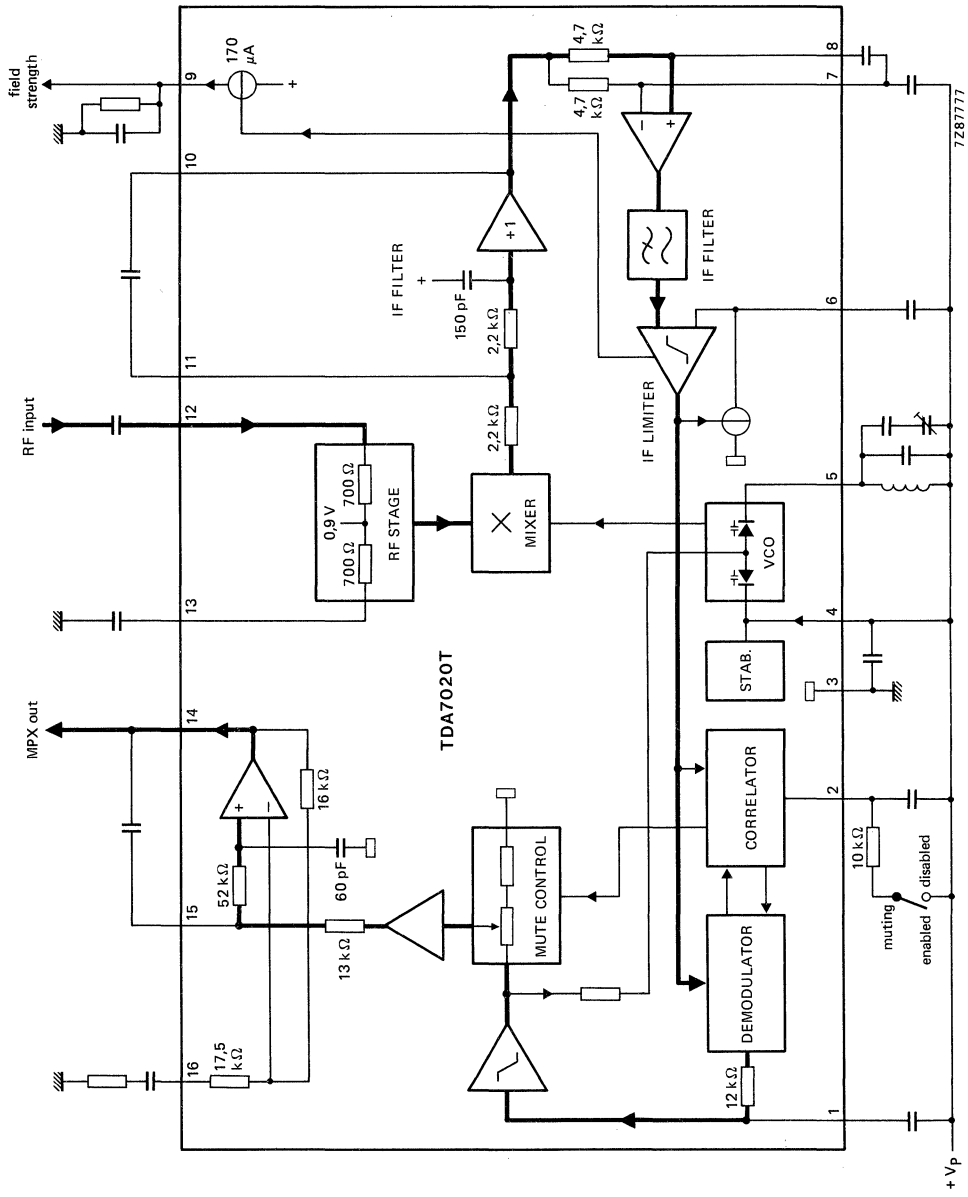


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 4)	V_P	max. 7	V
Oscillator voltage (pin 5)	V_{6-5}	$V_P - 0{,}5$ to $V_P + 0{,}5$	V
Total power dissipation	see derating curve (Fig. 2)		
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−10 to + 70	°C

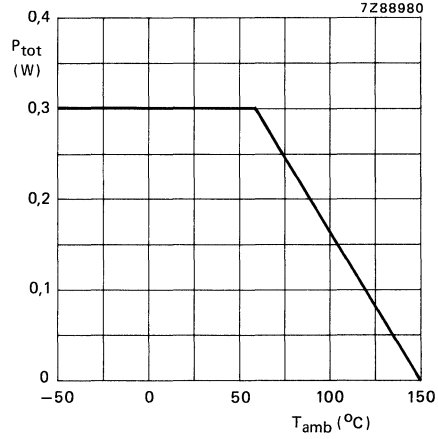


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)	V_{4-3}	1,8	3,0	6	V
Supply current at V_P = 3 V	$-I_3$	–	6,3	–	mA
Oscillator current (pin 5)	I_5	–	250	–	μA
Voltage at pin 13	V_{13-3}	–	0,9	–	V
Output voltage (pin 14)	V_{14-3}	–	1,3	–	V

A.C. CHARACTERISTICS MONO

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 4; f_{rf} = 96 MHz modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 300 μV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	4,0	–	μV
for −3 dB muting	EMF	–	5,0	–	μV
for S/N = 26 dB	EMF	–	6,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion					
at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of AM signal: f_m = 1 kHz; m = 80% to FM signal: f_m = 1 kHz; Δf = ± 75 kHz)	AMS	–	45	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	30	–	dB
Oscillator voltage (pin 5) r.m.s. value	$V_{5\text{-}3(rms)}$	–	250	–	mV
Variation of oscillator frequency					
with supply voltage (ΔV_P = 1 V)	$\Delta f_{osc}/\Delta V_P$	–	5	–	kHz/V
with temperature	$\Delta f_{osc}/\Delta T$	–	0,2	–	kHz/K
Selectivity	S_{+300}	–	30	–	dB
	S_{-300}	–	46	–	dB
AFC range	$\pm\Delta f_{rf}$	–	160	–	kHz
Mute range	$\pm\Delta f_{rf}$	–	120	–	kHz
Audio bandwidth at ΔV_o = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
AF output voltage (r.m.s. value) at $R_{L(pin\ 14)}$ = 100 Ω; pin 16 open	$V_{o(rms)}$	–	90	–	mV
AF output current					
max. d.c. load	$I_{o(dc)}$	−100	–	+100	μA
max. a.c. load for THD = 10%	$I_{o(ac)}$	−3	–	+3	mA

parameter	symbol	min.	typ.	max.	unit
Field strength signal					
EMF = 5 μV	$-I_9$	–	160	–	μA
EMF = 50 μV	$-I_9$	–	100	–	μA
EMF = 500 μV	$-I_9$	–	30	–	μA

A.C. CHARACTERISTICS

For STEREO operation (only the difference to MONO is given)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 5; f_{rf} = 96 MHz modulated with pilot Δf = ± 6,75 kHz and AF signal Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 1 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (Fig. 3) (e.m.f. voltage) for S/N = 46 dB	EMF	–	300	–	μV
Signal-to-noise ratio	S/N	–	53	–	dB
Channel separation	α	–	20	–	dB
Pilot voltage level at pin 14	V_{pilot}	–	12	–	mV
Selectivity	S_{+300}	–	22	–	dB
	S_{-300}	–	40	–	dB

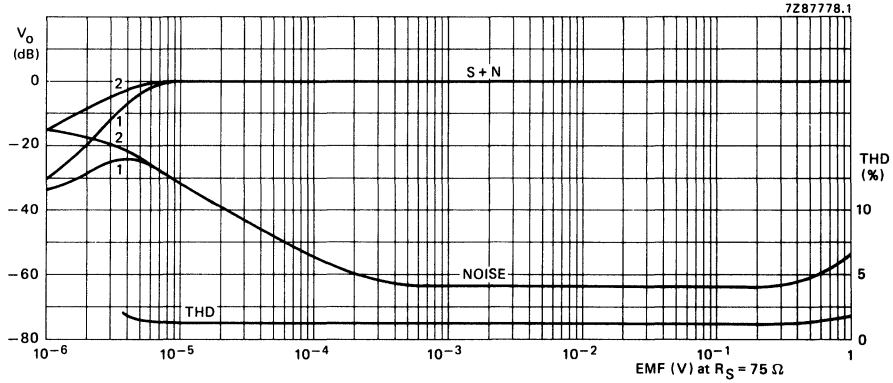
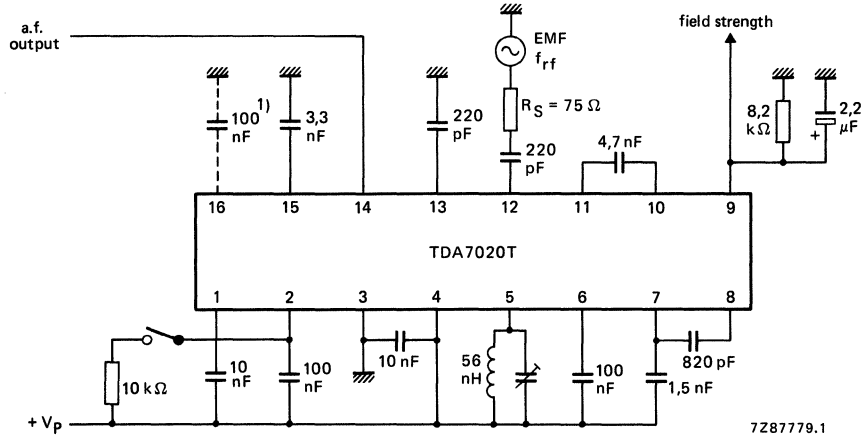


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 100 mV; f_{rf} = 96 MHz.
for S + N curve: Δf = ± 22,5 kHz; f_m = 1 kHz.
for THD curve: Δf = ± 75 kHz; f_m = 1 kHz.

Note
The muting system can be disabled by feeding a current of about 20 μA into pin 2.



1) To facilitate the use of high-impedance earphones the AF output can be increased by 5 dB by connection of the 100 nF capacitor to pin 16.

Fig. 4 Test circuit for MONO operation.

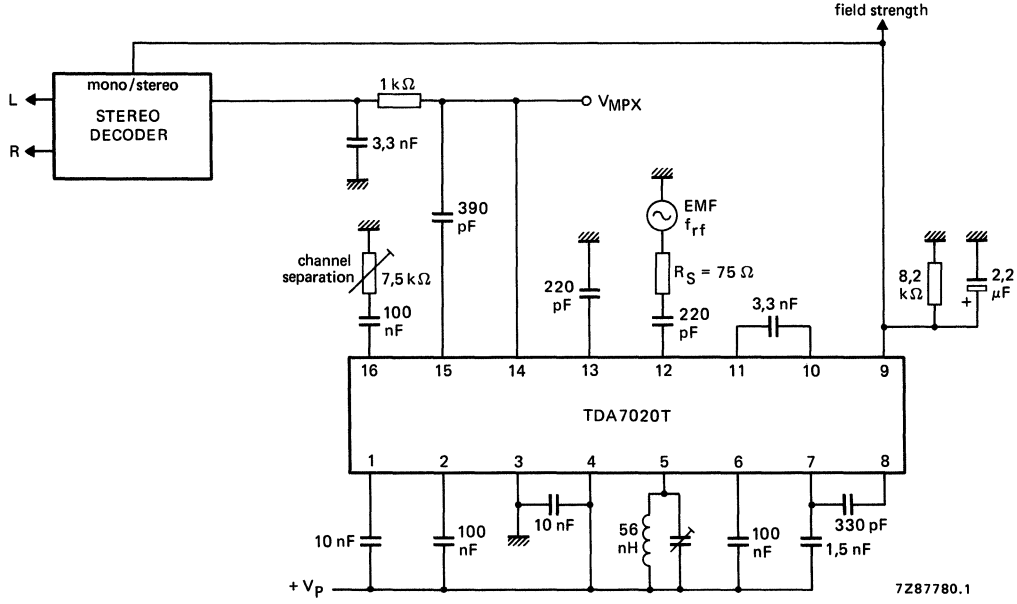


Fig. 5 Test circuit for STEREO operation.

FM Radio Circuit TEA5560

GENERAL DESCRIPTION

The TEA5560 is a monolithic integrated FM/IF system circuit, intended for car radios and home-receivers equipped with a ratio detector.
The system incorporates the following functions:

- a three-stage i.f. limiting amplifier
- a 15 dB field-strength dependent muting circuit
- a field-strength dependent d.c. voltage for e.g.:
  mono/stereo switching
  channel separation control of a stereo decoder
  an indicator ($I_{max} \leqslant 1$ mA)
- standby ON/OFF switching circuit
- a voltage stabilizer, for the internal circuit current and an external current up to 15 mA
- adjustable gain (ΔG = 15 dB)

QUICK REFERENCE DATA

Supply voltage range (pin 6)	V_P	10,2 to 18	V
Ambient temperature	T_{amb}	typ. 25	°C
Supply voltage (pin 6)	V_P	typ. 14,4	V
Frequency	f_o	10,7	MHz
Sensitivity (3 dB limiting)	V_i	typ. 150	μV
Signal-to-noise ratio for V_i = 10 mV	S/N	typ. 80	dB
A.F. output voltage at $\Delta f = \pm 22{,}5$ kHz	V_o	typ. 200	mV
Total harmonic distortion; $\Delta f = \pm 22{,}5$ kHz	THD	typ. 0,3	%
A.M. suppression AM signal: m = 0,3; f_m = 1 kHz FM signal: $\Delta f = \pm 22{,}5$ kHz; f_m = 70 Hz for V_i = 1 mV	AMS	typ. 50	dB

5

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142). The tab (on top of the package) is connected to pin 9.

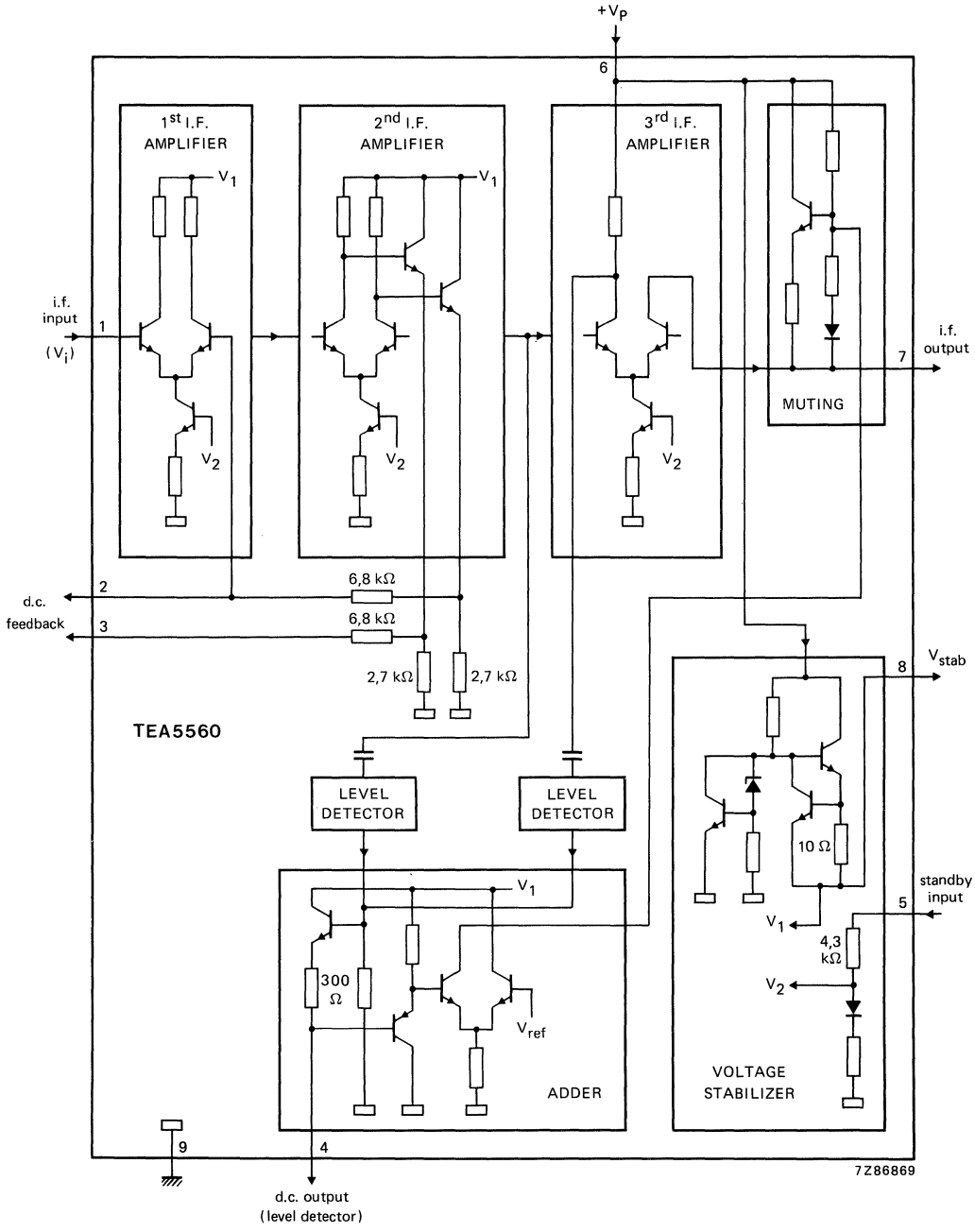


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages				
pin 6	$V_P = V_{6-9}$	max.	24	V
pin 7	V_{7-9}	max.	24	V
Voltage at pin 4	V_{4-9}	max.	6	V
Voltage at pin 5	V_{5-9}	max.	9	V
Non-repetitive peak output current (pin 8)	$-I_{8SM}$	max.	100	mA
Total power dissipation	P_{tot}	max.	1000	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−30 to	+85	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}amb}$	=	75	K/W

5

D.C. CHARACTERISTICS

V_P = 14,4 V; T_{amb} = 25 °C; measured in Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 6)					
Supply voltage *	$V_P = V_{6-9}$	10,2	14,4	18,0	V
Voltages					
at pin 8; $-I_8 = 0$ **	V_{8-9}	7,5	8,0	8,5	V
at pin 8 when $-I_8$ increases from 0 to 15 mA	ΔV_{8-9}	–	200	300	mV
at pin 8 when V_P reduces from 14,4 V to 10,2 V	ΔV_{8-9}	–	–	1,0	V
at pin 8 when V_P increases from 14,4 V to 18,0 V	ΔV_{8-9}	–	–	200	mV
at pin 4 (level detector)	V_{4-9}	–	–	100	mV
at pins 1, 2 and 3	$V_{1,2,3-9}$	–	2,4	–	V
Currents					
Total supply current; $-I_8 = 0$	I_{tot}	15	20	30	mA
Current supplied from pin 8	$-I_8$	–	–	15	mA
Stand-by current; $V_{5-9} = 0$	I_{sb}	8	11	14	mA
Current into pin 5	I_5	1,0	1,5	2,0	mA
Current into pin 7	I_7	–	3,0	–	mA
Power consumption					
at $-I_8 = 0$	P	–	300	–	mW

* A stabilized supply voltage of 7 to 9 V can also be applied at pin 5 and 6 (linked); for this application pin 8 must not be connected.

** The temperature coefficient of the stabilized voltage at pin 8 is typical −2,3 mV/K.

A.C. CHARACTERISTICS

V_P = 14,4 V; T_{amb} = 25 °C; V_i = 1 mV; f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 1 kHz; measured in Fig. 2; unless otherwise specified

parameter	symbpl	min.	typ.	max.	unit
I.F. part and ratio detector					
Sensitivity at −3 dB before limiting (pin 1); (without muting) *	V_i	105	150	210	μV
Signal-to-noise S + N/S measured in a bandwidth of 60 Hz to 15 kHz					
at V_i = 20 μV	S/N	40	45	–	dB
at V_i = 150 μV	S/N	–	65	–	dB
at V_i = 1 mV	S/N	–	78	–	dB
at V_i = 10 mV	S/N	–	80	–	dB
A.F. output voltage					
Δf = ± 22,5 kHz	V_o	–	200	–	mV
Δf = ± 75 kHz	V_o	–	600	–	mV
Total harmonic distortion					
Δf = ± 22,5 kHz	THD	–	0,3	–	%
Δf = ± 75 kHz	THD	–	2,0	–	%
AM suppression f_m = 1 kHz; m = 0,3 (for AM) f_m = 70 kHz; Δf = ± 22,5 kHz (for FM)					
at V_i = 150 μV	AMS	–	40	–	dB
at V_i = 1 mV	AMS	–	50	–	dB
at V_i = 10 mV	AMS	–	55	–	dB
Level detector circuit					
D.C. output voltage (pin 4)					
at V_i = 200 μV	V_{4-9}	–	1,9	–	V
at V_i = 500 μV	V_{4-9}	–	2,8	–	V
at V_i = 1 mV	V_{4-9}	–	3,5	–	V
at V_i = 3 mV	V_{4-9}	–	5,0	–	V
at V_i = 10 mV	V_{4-9}	–	5,7	–	V
Muting circuit (see also Fig. 5)					
Change in output voltage at V_i = 3 μV (with and without muting) *	α_{vo}	10	15	–	dB
Input voltage at a change in output voltage of ⩽ 1 dB* (V_i at α_{vo} ⩽ 1 dB)	V_i	–	–	250	μV

* With muting $V_{4-9} < 0,3$ V; without muting V_{4-9} = 1,2 to 6 V.

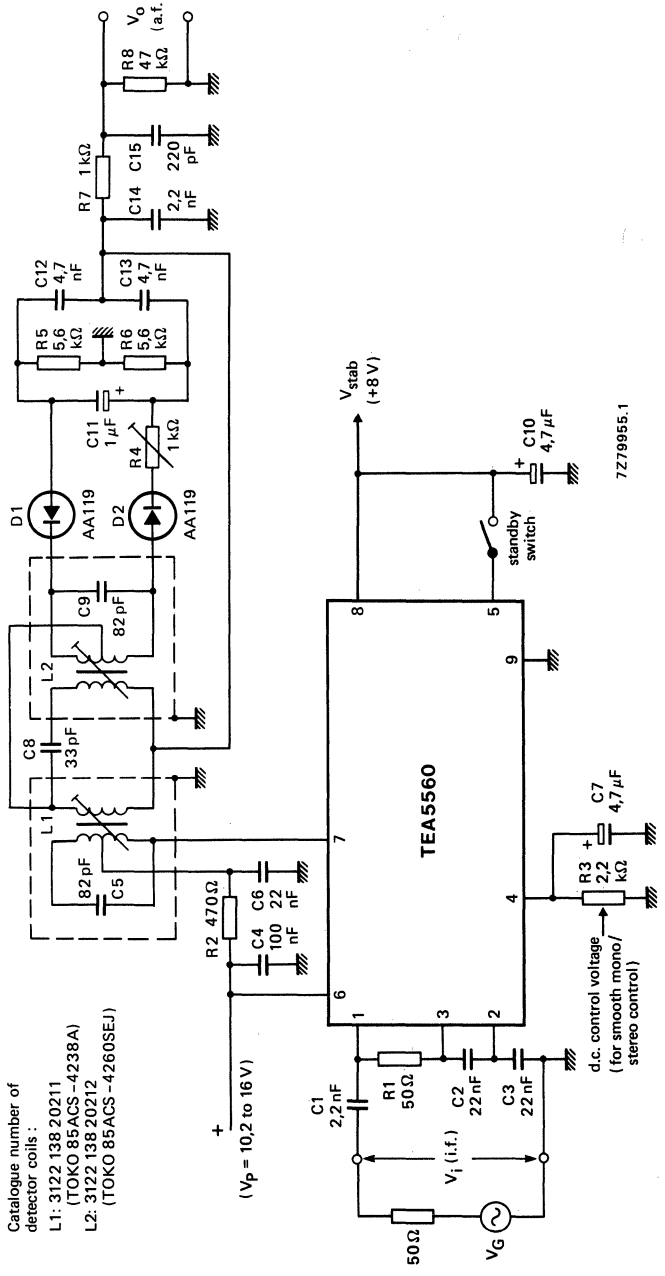


Fig. 2 FM test circuit.

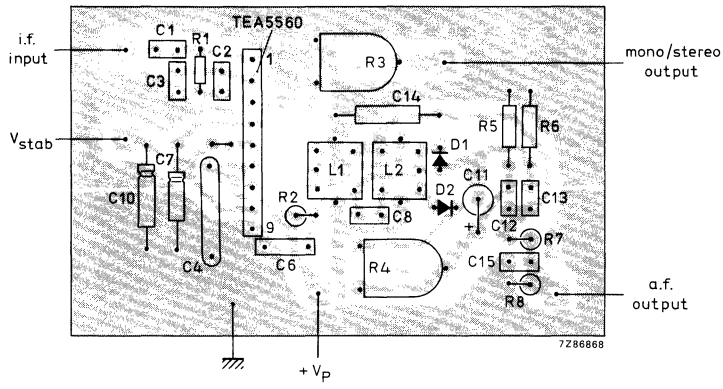
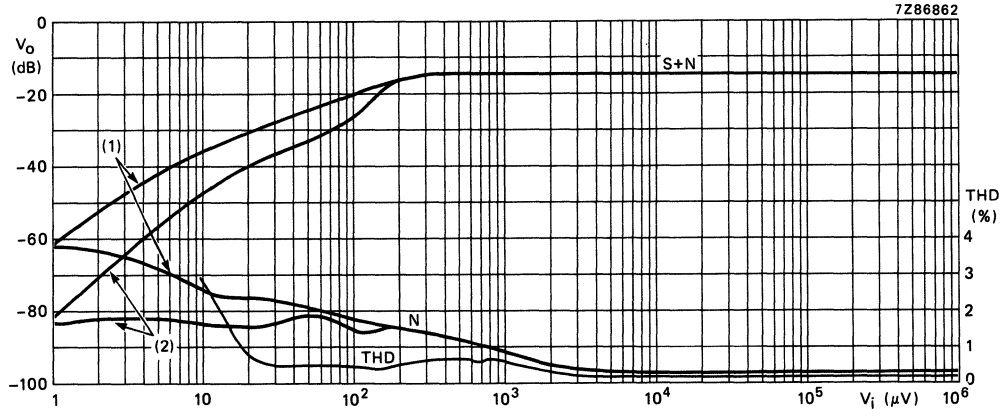


Fig. 3 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 2.

Fig. 4 Printed-circuit board showing track side.



(1) Without muting.
(2) With muting.

Fig. 5 A.F. output voltage (V_o); reference level 0 dB = 1 V, and the total harmonic distortion (THD) as a function of the i.f. input voltage (V_i). Measured in the test circuit Fig. 2 at $\Delta f = \pm 22{,}5$ kHz; $f_m = 1$ kHz.

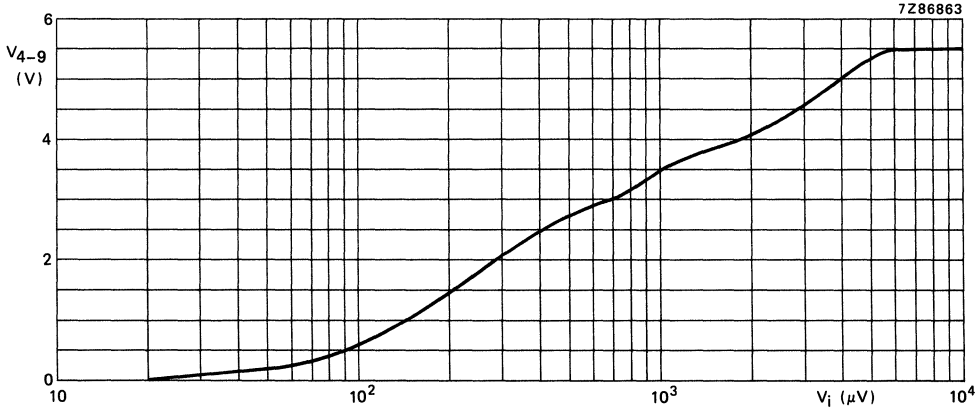
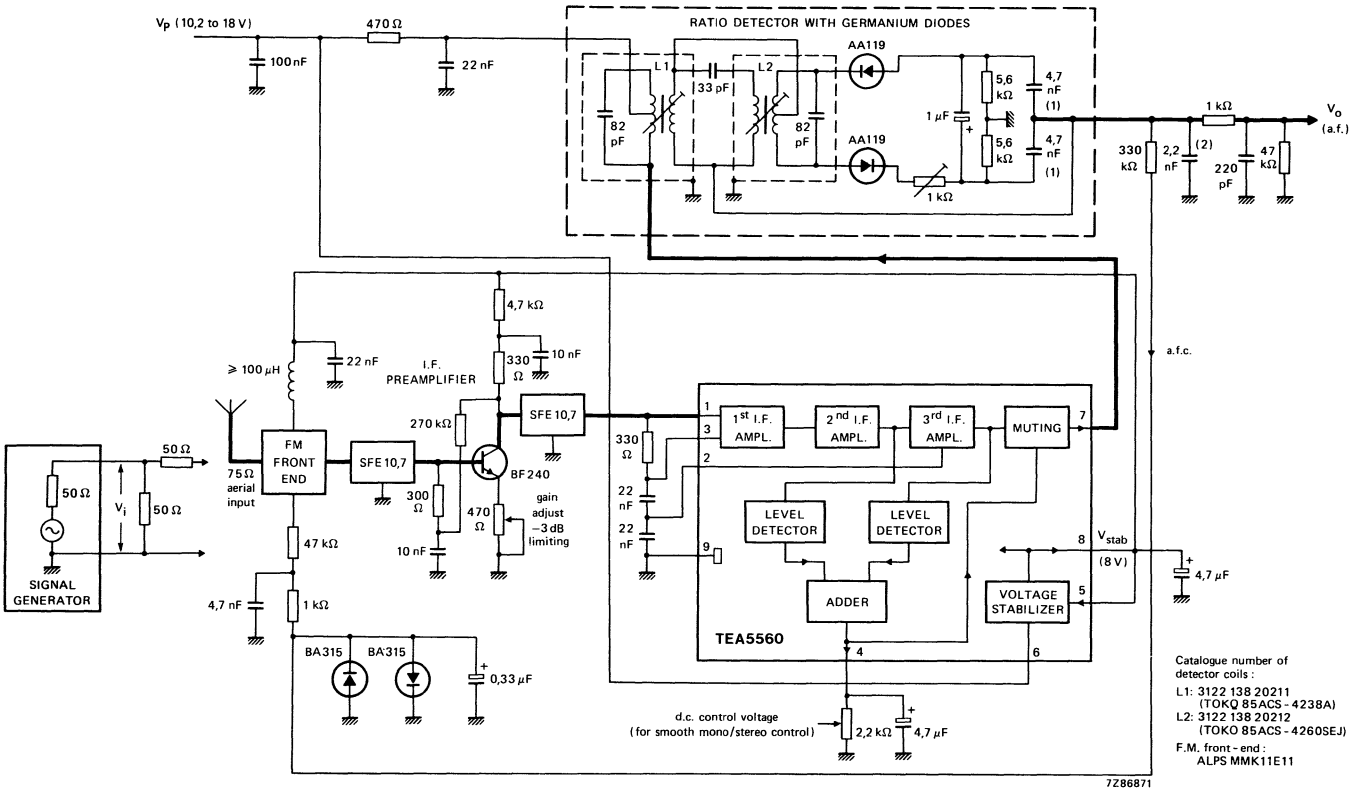


Fig. 6 Level detector d.c. output voltage (pin 4) as a function of the i.f. input voltage. Measured in test circuit Fig. 2.

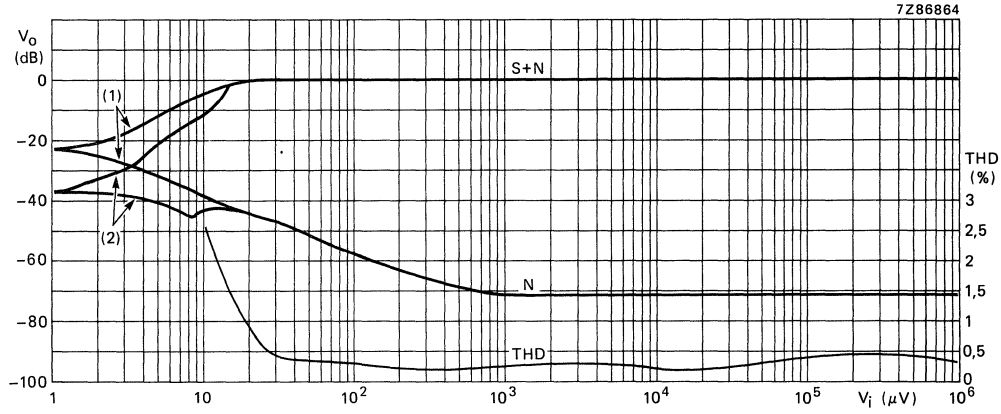
APPLICATION INFORMATION



(1) Stereo application 220 pF.
(2) Stereo application 390 pF.

Fig. 7 FM channel for (car) radios using the TEA5560 and a ratio detector with AA119 germanium diodes.

APPLICATION INFORMATION (continued)



(1) Without muting.
(2) With muting.

Fig. 8 Signal and noise (S + N) and noise (N); reference level 0 dB = 200 mV, and the total harmonic distortion (THD) as a function of the aerial input voltage (V_i). Measured in application circuit Fig. 7 at $\Delta f = \pm 22{,}5$ kHz; $f_m = 1$ kHz.

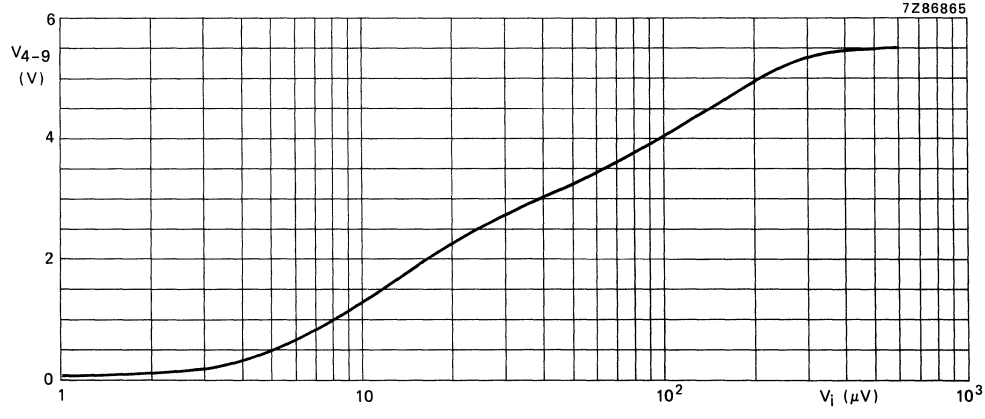
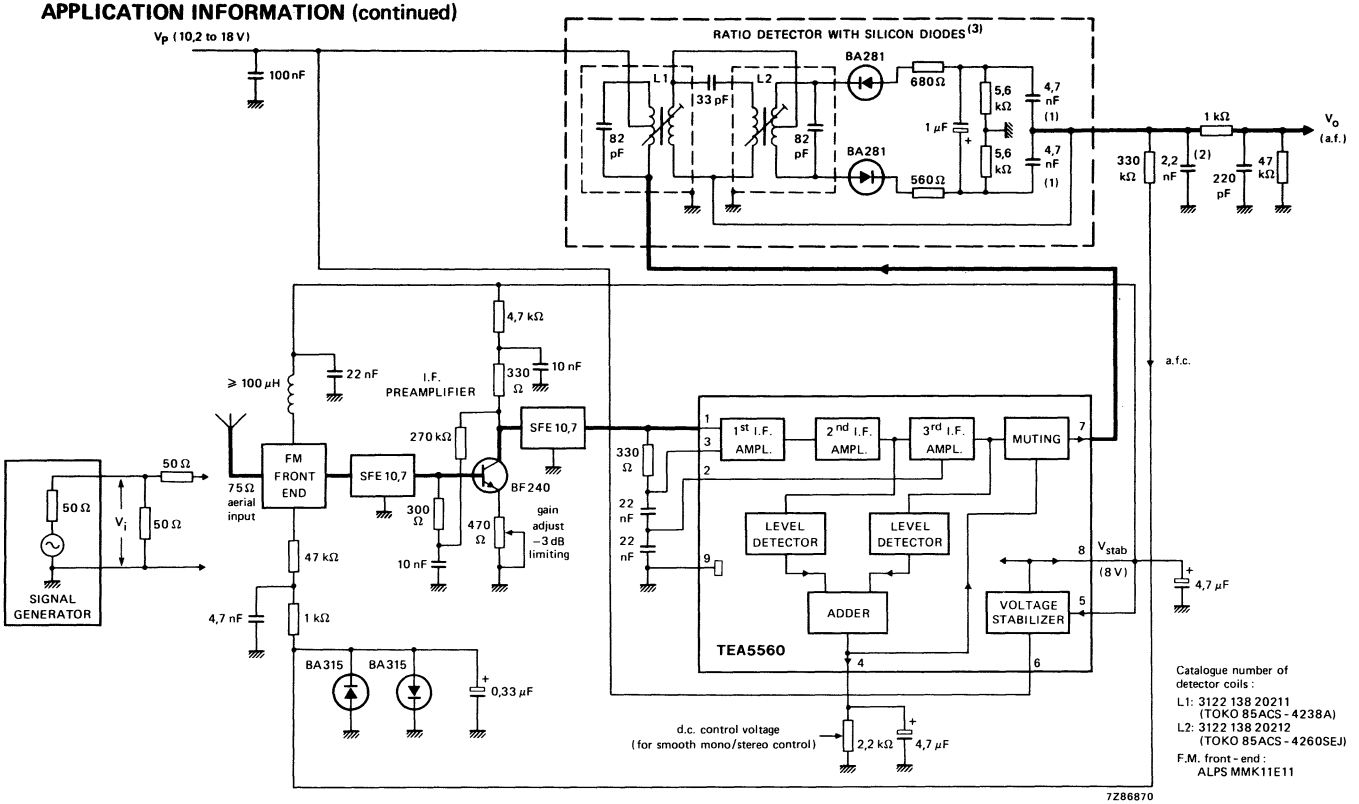


Fig. 9 Level detector d.c. output voltage (pin 4) as a function of the aerial input voltage. Measured in application circuit Fig. 7.

APPLICATION INFORMATION (continued)



Catalogue number of detector coils :

L1: 3122 138 20211 (TOKO 85ACS - 4238A)

L2: 3122 138 20212 (TOKO 85ACS - 4260SEJ)

F.M. front - end : ALPS MMK11E11

(1) Stereo application 220 pF.

(2) Stereo application 390 pF.

(3) Further detailed information of using silicon diodes is available on request.

Fig. 10 FM channel for (car) radios using the TEA5560 and a ratio detector with BA281 silicon diodes.

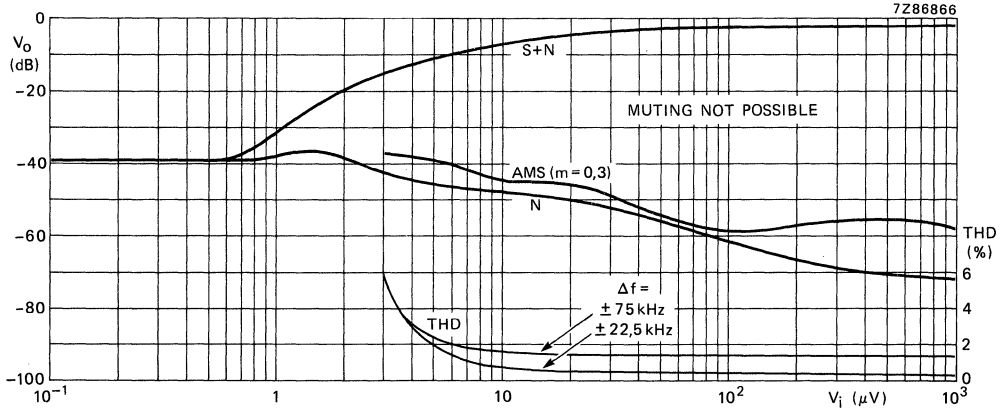


Fig. 11 Signal and noise (S + N) and noise (N); reference level 0 dB = 245 mV, AM suppression (AMS) and total harmonic distortion (THD) as a function of the aerial input voltage (V_i). Measured in application circuit Fig. 10 at $\Delta f = \pm 22{,}5$ kHz; $f_m = 1$ kHz; for AM suppression m = 0,3; $\Delta f = \pm 22{,}5$ kHz.

FM I.F. System and Computer Interface (MUSTI) Circuit

TEA6000

GENERAL DESCRIPTION

The TEA6000 is an FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes an AM/FM-IF counter and an analogue-to-digital interface. The i.f. counter generates AM/FM precision tuning and accurate stop information.

Features

- 3-stage IF limiter for driving a ratio detector
- 2-stage level detector with current output
- operational amplifier for active filtering (e.g. multipath detector)
- high resolution frequency counter for FM and AM IF-signals
- time base reference from crystal oscillator or external source (SAA1057)
- serial two wire bidirectional computer interface (I^2C-bus)
- multiplexed 3 bit A/D converter for two input signals
- software controlled sensitivity for both ADC inputs

5

QUICK REFERENCE DATA

Supply voltages (V_{P1} and V_{P2})	V_P	typ.	8,4 V
Supply current; ($I_{P1} + I_{P2}$)	I_P	typ.	36 mA
FM/IF sensitivity			
at −3 dB before limiting	V_i	typ.	150 μV
Signal to noise ratio for V_i = 10 mV	S/N	typ.	80 dB
Audio output voltage			
Δf = 22,5 kHz; V_i = 1 mV	V_O	typ.	170 mV
Δf = 75 kHz; V_i = 1 mV	V_O	typ.	520 mV
AM suppression at V_i = 10 mV	AMS	typ.	58 dB
Frequency counter sensitivity			
AM (pin 18)	$V_{i(am)}$	typ.	60 μV
FM (pin 16)	$V_{i(fm)}$	typ.	80 μV
Resolution frequency counter			
AM	$f_{s(am)}$	typ.	·250 Hz
FM	$f_{s(fm)}$	typ.	6,4 kHz
Power dissipation	P_{tot}	max.	1300 mW
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−30 to + 85	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

FM I.F. System and Computer Interface (MUSTI) Circuit

TEA6000

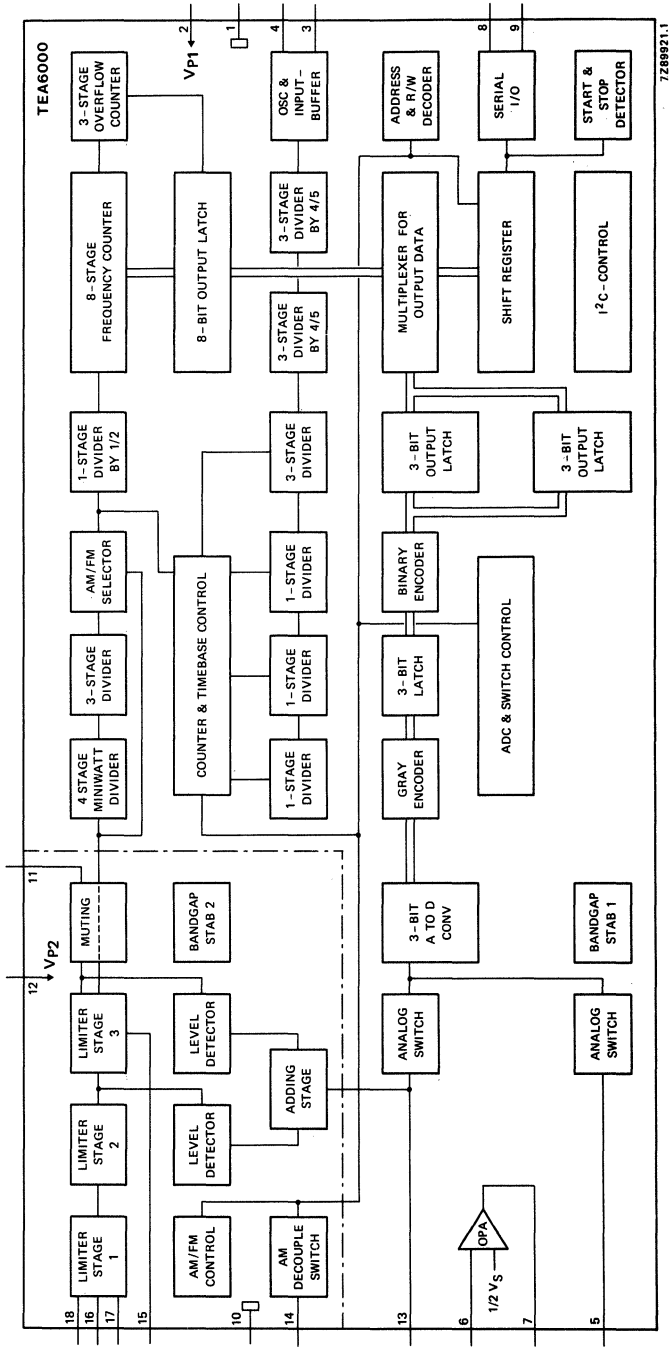


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The IF SECTION consists of three balanced differential stages with separated FM and AM inputs, directly coupled by emitter followers. The last stage also has separated outputs, which are intended for driving a ratio detector and the frequency measuring system respectively.

The last two stages are coupled via low-value capacitors to two LEVEL DETECTORS which generate a signal-dependent d.c. current for controlling channel separation and frequency response of a stereo decoder, multipath detector circuitry, AGC and the internal ADC.

The IF MUTING circuit has been incorporated to decrease the interstation noise by about 15 dB.

The 3-bit A/D CONVERTER has two inputs, which are selected via two multiplexed analogue switches. One of these switches is internally connected to the level detector output but can also serve as an external input, as the level detector output can be switched off. The outputs of the ADC are converted to a Gray code, latched and reconverted to a binary code to obtain glitch-free output data. The sensitivity of both inputs can be selected independently via software on two levels.

The reference for the ADC is derived from a BAND-GAP STABILIZER circuit. Multipath distortion on FM will generate an AM modulation on the d.c. voltage from the level detectors. This AM modulation can be filtered and rectified to obtain a multipath-dependent d.c. voltage. This voltage can be applied to the other input of the ADC.

To facilitate filtering an OPERATIONAL AMPLIFIER (OPA) is incorporated on the chip. The typical circuit diagram for a multipath filter is given in Fig. 4.

The FREQUENCY COUNTER is preceded by a 7-stage prescaler for FM, and FM/AM selector stage and a divider by 1 or 2. The actual counter is a presetable and resetable 8-stage counter with a 3-stage data disable overflow counter, which can be switched off. The eight significant output bits are situated symmetrically around 10,7 MHz and 460 kHz, when the external timebase source is used (e.g. SAA1057). See Table 1.

The reference for the TIMEBASE is primarily thought to be the SAA1057. This circuit generates from its 4 MHz crystal oscillator a 32 or 40 kHz signal. This signal is buffered and applied to the timebase circuitry (mode I). The circuit diagram for this mode I is given in Fig. 5a.
In the timebase, the selection is made for reference frequency (32 to 40 kHz), FM or AM mode and the width of the measuring window, all under software control. Accuracy ± ½ bit when the window is set to wide (see Fig. 2) and ± 1 bit when set to narrow. A special feature is the synchronization of the measuring cycle with the input DATA of the I^2C-bus, meaning the measuring cycle starts immediately after a "WRITE" instruction via the I^2C-bus.

For those who do not use the SAA1057 as reference, a 2^{15} Hz crystal (32 768 Hz) can be connected to the reference inputs directly, obtaining a quartz-oscillator reference. See Fig. 5b for the circuit diagram for this mode II.

When the circuit is used in mode II a correction has to be made to the values of window width and resolution as the cheap watch crystals differ by about 2,4% from the frequency generated by the SAA1057 (32 768 and 32 000 kHz respectively) See Table 2.

Communication between MUSTI and the microcomputer is accomplished via the two-wire bidirectional I^2C-bus (slave transceiver version); the SDA (serial data) and SCL (serial clock).

To prevent crosstalk between the digital and analogue parts of the circuit the power supply lines are fully isolated.

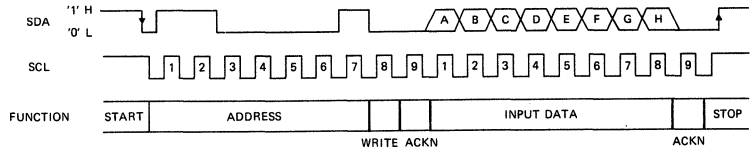


Fig. 2 Input data format waveforms.

Input bits

bit	function	"0"	"1"	reference to Fig. 2
1	reference frequency	32 kHz	40 kHz	A
2	sensitivity ADC2	LOW	HIGH	B
3	sensitivity ADC1	LOW	HIGH	C
4	level detector output	off	on	D
5	AM/FM	AM	FM	E
6	overflow counter	off	on	F
7	measuring window	narrow	wide	G
8	test mode	off	on	H

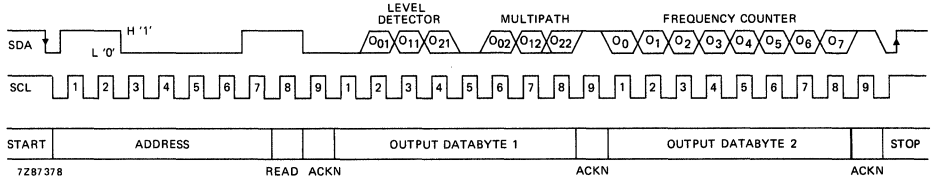


Fig. 3 Output data format waveforms.

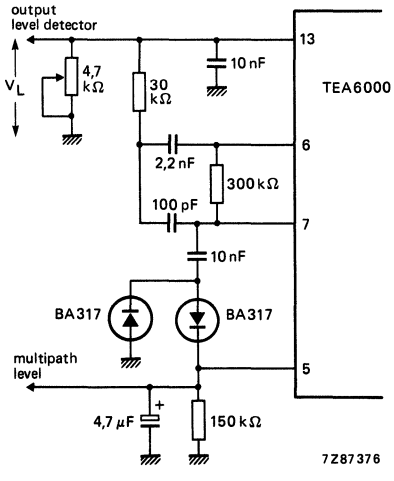


Fig. 4 Multipath detector circuit.

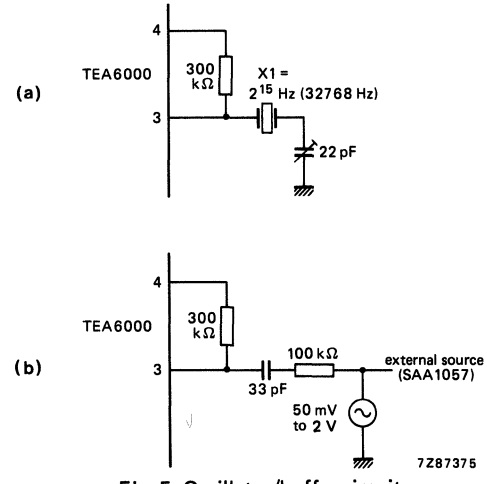


Fig. 5 Oscillator/buffer circuits. X1 = 2^{15} Hz (32 768 Hz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
pin 2	V_{P1}	max.	13,2 V
pin 12	V_{P2}	max.	13,2 V
Power dissipation	P_{tot}	max.	1300 mW
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−30 to + 85 °C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c\text{-}a}$	=	50 K/W

D.C. CHARACTERISTICS

$V_{P1} = V_{P2} = 8{,}4$ V; $T_{amb} = 25$ °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
(pin 2)	V_{P1}	7,6	8,4	9,2	V
(pin 12)	V_{P2}	7,6	8,4	9,2	V
Supply current AM mode					
pin 2	I_{P1}	–	18,5	–	mA
pin 12	I_{P2}	–	17,4	–	mA
Supply current FM mode					
pin 2	I_{P1}	–	19,2	–	mA
pin 12	I_{P2}	–	16,4	–	mA
Power dissipation	P_{tot}	–	350	–	mW

A.C. CHARACTERISTICS (see Fig. 6)

$V_{P1} = V_{P2} = 8{,}4$ V; $V_{16\text{-}10} = 1$ mV; f = 10,7 MHz; $\Delta f = 22{,}5$ kHz; $f_m = 1$ kHz; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity					
at −3 dB before limiting	$V_{I(FM)}$	–	150	–	μV
Signal-to-noise ratio, FM input					
V_i = 20 μV	S/N	40	46	–	dB
V_i = 150 μV	S/N	–	64	–	dB
V_i = 1 mV	S/N	–	76	–	dB
V_i = 10 mV	S/N	–	80	–	dB
Noise output voltage					
V_i = 0 V; with muting, switch S1 on	V_{no}	–	55	–	μV
V_i = 0 V; without muting, S1 off	V_{no}	–	420	–	μV
Audio output voltage					
Δf = 22,5 kHz	V_O	–	170	–	mV
Δf = 75 kHz	V_O	–	520	–	mV

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
AM suppression					
ratio of the AM output signal referred to the FM signal (m = 0,3)					
V_i = 150 μV	AMS	–	46	–	dB
V_i = 1 mV	AMS	–	62	–	dB
V_i = 10 mV	AMS	–	58	–	dB
V_i = 100 mV	AMS	–	60	–	dB
Level detector output voltage (Fig. 4)					
$R_{13\text{-}10}$ = 4,7 kΩ; V_i = 10 mV, FM mode	V_L	–	6,2	–	V
Level detector output voltage slope					
$R_{13\text{-}10}$ adjusted in FM mode for V_L = 5,5 V at V_i = 10 mV; f = 10,7 MHz					
V_i = 0 V (pin 16)	$V_{L(FM)}$	–	130	–	mV
V_i = 140 μV	$V_{L(FM)}$	–	1,3	–	V
V_i = 1 mV	$V_{L(FM)}$	–	2,7	–	V
V_i = 3 mV	$V_{L(FM)}$	–	4,4	–	V
$R_{13\text{-}10}$ adjusted in FM mode (see above)					
V_i = 0 V, f = 460 kHz (pin 18)	$V_{L(AM)}$	–	200	–	mV
V_i = 1 mV, f = 460 kHz (pin 18)	$V_{L(AM)}$	–	1,4	–	V
V_i = 10 mV, f = 460 kHz (pin 18)	$V_{L(AM)}$	–	2,7	–	V
Frequency counter sensitivity					
AM input voltage (pin 18)	$V_{I(AM)}$	–	60	–	μV
FM input voltage (pin 16)	$V_{I(FM)}$	–	80	–	μV
AM input impedance	R_i	–	30	–	kΩ
BUS inputs					
SDA and SCL (pins 9 and 8)					
input voltage HIGH	V_{IH}	3,0	–	V_{P1}	V
input voltage LOW	V_{IL}	−0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	10	μA
input current LOW	I_{IL}	–	–	10	μA
acknowledge sink current	I_{ack}	–	–	2	mA
maximum input frequency	$f_{i\ max}$	100	–	–	kHz
Output voltage SDA					
HIGH; 4 kΩ to 8,4 V	V_{OH}	8,0	–	–	V
LOW; I = 2 mA	V_{OL}	–	–	0,4	V

parameter	symbol	min.	typ.	max.	unit
A/D converter (pin 5 and 13)					
input resistance	R_i		t.b.f.		kΩ
input capacitance	C_i		t.b.f.		pF
Trip levels, sensitivity bit HIGH					
level 1	V_T	–	0,6	–	V
level 2	V_T	–	1,06	–	V
level 3	V_T	–	1,38	–	V
level 4	V_T	–	1,84	–	V
level 5	V_T	–	2,14	–	V
level 6	V_T	–	2,55	–	V
level 7	V_T	–	2,97	–	V
Trip levels, sensitivity bit LOW					
level 1	V_T	–	0,96	–	V
level 2	V_T	–	1,78	–	V
level 3	V_T	–	2,44	–	V
level 4	V_T	–	3,26	–	V
level 5	V_T	–	3,92	–	V
level 6	V_T	–	4,63	–	V
level 7	V_T	–	5,38	–	V
Crystal oscillator (see Fig. 5)					
reference frequency	f_{ref}	32	32,768	40	kHz
temperature coefficient	TC		t.b.f.		10^{-6}
input resistance	R_i		t.b.f.		kΩ
input capacitance	C_i		t.b.f.		pF
Operational amplifier (pins 6 and 7)					
voltage gain	G_V	–	10^4	–	
input bias current	I_{bias}	–	30	100	nA
output sink current at V_O = 1 V	I_O	–	0,2	–	mA
output source current at V_O = 7,4 V	I_O	5,5	10	–	mA
output voltage swing	$V_{7(p-p)}$	–	5,5	–	V
Frequency measuring system (see pages 8 and 9)					
measuring windows; f_{ref} = 32 or 40 kHz					
AM					
window "0" (LOW)	t_{gate}	–	4	–	ms
window "1" (HIGH)	t_{gate}	–	8	–	ms
FM					
window "0" (LOW)	t_{gate}	–	20	–	ms
window "1" (HIGH)	t_{gate}	–	40	–	ms
resolution frequency counter					
AM	$f_{s(am)}$	–	250	–	Hz
FM	$f_{s(fm)}$	–	6,4	–	kHz

t_{gate} has to be multiplied by 32 000/32 768 for a f_{ref} of 2^{15} Hz.
f_s has to be multiplied by 32 768/32 000 for a f_{ref} of 2^{15} Hz.

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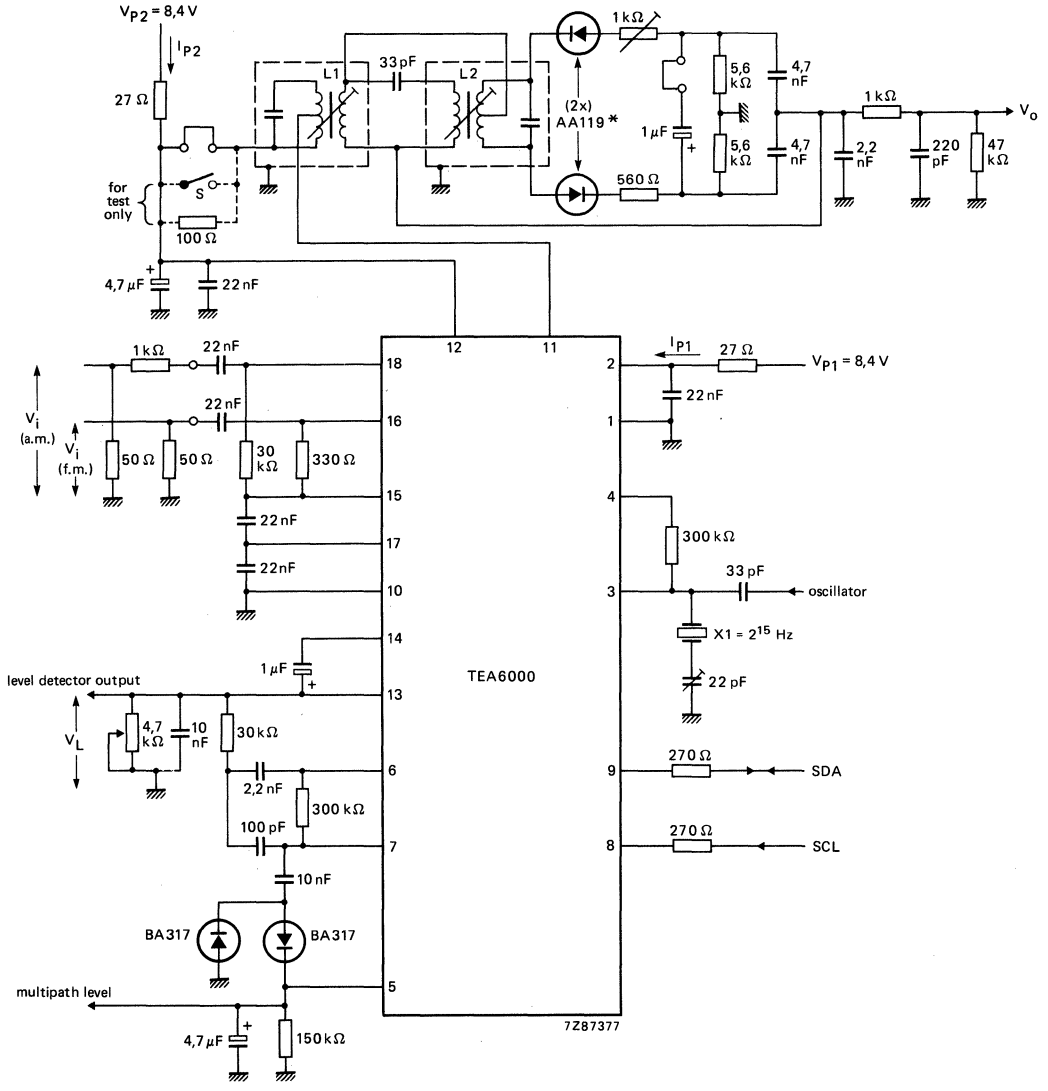
TABLE 1 REFERENCE FREQUENCY 32 000 Hz (SAA1057)

AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)
428.25	'00'	9.888	441.00	'33'	10.214	453.75	'66'	10.541	466.50	'99'	10.867	479.25	'CC'	11.194
428.50	'01'	9.894	441.25	'34'	10.221	454.00	'67'	10.547	466.75	'9A'	10.874	479.50	'CD'	11.200
428.75	'02'	9.901	441.50	'35'	10.227	454.25	'68'	10.554	467.00	'9B'	10.880	479.75	'CE'	11.206
429.00	'03'	9.907	441.75	'36'	10.234	454.50	'69'	10.560	467.25	'9C'	10.886	480.00	'CF'	11.213
429.25	'04'	9.914	442.00	'37'	10.240	454.75	'6A'	10.566	467.50	'9D'	10.893	480.25	'D0'	11.219
429.50	'05'	9.920	442.25	'38'	10.246	455.00	'6B'	10.573	467.75	'9E'	10.899	480.50	'D1'	11.226
429.75	'06'	9.926	442.50	'39'	10.253	455.25	'6C'	10.579	468.00	'9F'	10.906	480.75	'D2'	11.232
430.00	'07'	9.933	442.75	'3A'	10.259	455.50	'6D'	10.586	468.25	'A0'	10.912	481.00	'D3'	11.238
430.25	'08'	9.939	443.00	'3B'	10.266	455.75	'6E'	10.592	468.50	'A1'	10.918	481.25	'D4'	11.245
430.50	'09'	9.946	443.25	'3C'	10.272	456.00	'6F'	10.598	468.75	'A2'	10.925	481.50	'D5'	11.251
430.75	'0A'	9.952	443.50	'3D'	10.278	456.25	'70'	10.605	469.00	'A3'	10.931	481.75	'D6'	11.258
431.00	'0B'	9.958	443.75	'3E'	10.285	456.50	'71'	10.611	469.25	'A4'	10.938	482.00	'D7'	11.264
431.25	'0C'	9.965	444.00	'3F'	10.291	456.75	'72'	10.618	469.50	'A5'	10.944	482.25	'D8'	11.270
431.50	'0D'	9.971	444.25	'40'	10.298	457.00	'73'	10.624	469.75	'A6'	10.950	482.50	'D9'	11.277
431.75	'0E'	9.978	444.50	'41'	10.304	457.25	'74'	10.630	470.00	'A7'	10.957	482.75	'DA'	11.283
432.00	'0F'	9.984	444.75	'42'	10.310	457.50	'75'	10.637	470.25	'A8'	10.963	483.00	'DB'	11.290
432.25	'10'	9.990	445.00	'43'	10.317	457.75	'76'	10.643	470.50	'A9'	10.970	483.25	'DC'	11.296
432.50	'11'	9.997	445.25	'44'	10.323	458.00	'77'	10.650	470.75	'AA'	10.976	483.50	'DD'	11.302
432.75	'12'	10.003	445.50	'45'	10.330	458.25	'78'	10.656	471.00	'AB'	10.982	483.75	'DE'	11.309
433.00	'13'	10.010	445.75	'46'	10.336	458.50	'79'	10.662	471.25	'AC'	10.989	484.00	'DF'	11.315
433.25	'14'	10.016	446.00	'47'	10.342	458.75	'7A'	10.669	471.50	'AD'	10.995	484.25	'E0'	11.322
433.50	'15'	10.022	446.25	'48'	10.349	459.00	'7B'	10.675	471.75	'AE'	11.002	484.50	'E1'	11.328
433.75	'16'	10.029	446.50	'49'	10.355	459.25	'7C'	10.682	472.00	'AF'	11.008	484.75	'E2'	11.334
434.00	'17'	10.035	446.75	'4A'	10.362	459.50	'7D'	10.688	472.25	'B0'	11.014	485.00	'E3'	11.341
434.25	'18'	10.042	447.00	'4B'	10.368	459.75	'7E'	10.694	472.50	'B1'	11.021	485.25	'E4'	11.347
434.50	'19'	10.048	447.25	'4C'	10.374	460.00	'7F'	10.701	472.75	'B2'	11.027	485.50	'E5'	11.354
434.75	'1A'	10.054	447.50	'4D'	10.381	460.25	'80'	10.707	473.00	'B3'	11.034	485.75	'E6'	11.360
435.00	'1B'	10.061	447.75	'4E'	10.387	460.50	'81'	10.714	473.25	'B4'	11.040	486.00	'E7'	11.366
435.25	'1C'	10.067	448.00	'4F'	10.394	460.75	'82'	10.720	473.50	'B5'	11.046	486.25	'E8'	11.373
435.50	'1D'	10.074	448.25	'50'	10.400	461.00	'83'	10.726	473.75	'B6'	11.053	486.50	'E9'	11.379
435.75	'1E'	10.080	448.50	'51'	10.406	461.25	'84'	10.733	474.00	'B7'	11.059	486.75	'EA'	11.386
436.00	'1F'	10.086	448.75	'52'	10.413	461.50	'85'	10.739	474.25	'B8'	11.066	487.00	'EB'	11.392
436.25	'20'	10.093	449.00	'53'	10.419	461.75	'86'	10.746	474.50	'B9'	11.072	487.25	'EC'	11.398
436.50	'21'	10.099	449.25	'54'	10.426	462.00	'87'	10.752	474.75	'BA'	11.078	487.50	'ED'	11.405
436.75	'22'	10.106	449.50	'55'	10.432	462.25	'88'	10.758	475.00	'BB'	11.085	487.75	'EE'	11.411
437.00	'23'	10.112	449.75	'56'	10.438	462.50	'89'	10.765	475.25	'BC'	11.091	488.00	'EF'	11.418
437.25	'24'	10.118	450.00	'57'	10.445	462.75	'8A'	10.771	475.50	'BD'	11.098	488.25	'F0'	11.424
437.50	'25'	10.125	450.25	'58'	10.451	463.00	'8B'	10.778	475.75	'BE'	11.104	488.50	'F1'	11.430
437.75	'26'	10.131	450.50	'59'	10.458	463.25	'8C'	10.784	476.00	'BF'	11.110	488.75	'F2'	11.437
438.00	'27'	10.138	450.75	'5A'	10.464	463.50	'8D'	10.790	476.25	'C0'	11.117	489.00	'F3'	11.443
438.25	'28'	10.144	451.00	'5B'	10.470	463.75	'8E'	10.797	476.50	'C1'	11.123	489.25	'F4'	11.450
438.50	'29'	10.150	451.25	'5C'	10.477	464.00	'8F'	10.803	476.75	'C2'	11.130	489.50	'F5'	11.456
438.75	'2A'	10.157	451.50	'5D'	10.483	464.25	'90'	10.810	477.00	'C3'	11.136	489.75	'F6'	11.462
439.00	'2B'	10.163	451.75	'5E'	10.490	464.50	'91'	10.816	477.25	'C4'	11.142	490.00	'F7'	11.469
439.25	'2C'	10.170	452.00	'5F'	10.496	464.75	'92'	10.822	477.50	'C5'	11.149	490.25	'F8'	11.475
439.50	'2D'	10.176	452.25	'60'	10.502	465.00	'93'	10.829	477.75	'C6'	11.155	490.50	'F9'	11.482
439.75	'2E'	10.182	452.50	'61'	10.509	465.25	'94'	10.835	478.00	'C7'	11.162	490.75	'FA'	11.488
440.00	'2F'	10.189	452.75	'62'	10.515	465.50	'95'	10.842	478.25	'C8'	11.168	491.00	'FB'	11.494
440.25	'30'	10.195	453.00	'63'	10.522	465.75	'96'	10.848	478.50	'C9'	11.174	491.25	'FC'	11.501
440.50	'31'	10.202	453.25	'64'	10.528	466.00	'97'	10.854	478.75	'CA'	11.181	491.50	'FD'	11.507
440.75	'32'	10.208	453.50	'65'	10.534	466.25	'98'	10.861	479.00	'CB'	11.187	491.75	'FE'	11.514

TABLE 2 REFERENCE FREQUENCY 32 768 Hz (2^{15} Hz)

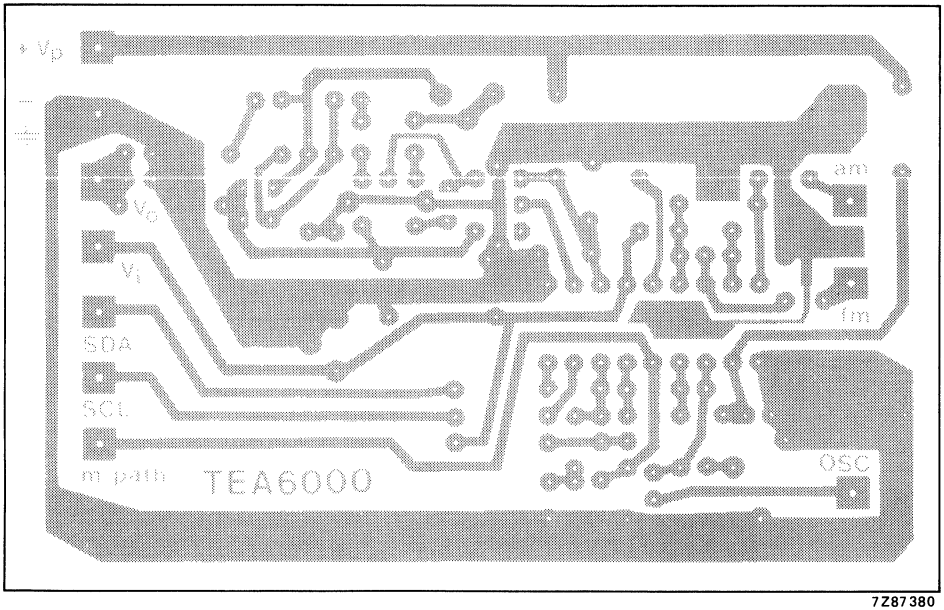
AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (MHz)	AM (kHz)	READ OUT	FM (HMz)	AM (kHz)	READ OUT	FM (MHz)
438.53	'00'	10.125	451.53	'33'	10.460	464.64	'66'	10.794	477.70	'99'	11.128	490.75	'CC'	11.462
438.78	'01'	10.132	451.84	'34'	10.466	464.90	'67'	10.800	477.95	'9A'	11.135	491.01	'CD'	11.469
439.04	'02'	10.138	452.10	'35'	10.473	465.15	'68'	10.807	478.21	'9B'	11.141	491.26	'CE'	11.475
439.30	'03'	10.145	452.35	'36'	10.479	465.41	'69'	10.813	478.46	'9C'	11.148	491.52	'CF'	11.482
439.55	'04'	10.152	452.61	'37'	10.486	465.66	'6A'	10.820	478.72	'9D'	11.154	491.78	'D0'	11.488
439.81	'05'	10.158	452.86	'38'	10.492	465.92	'6B'	10.827	478.98	'9E'	11.161	492.03	'D1'	11.495
440.06	'06'	10.165	453.12	'39'	10.499	466.18	'6C'	10.833	479.23	'9F'	11.167	492.29	'D2'	11.502
440.32	'07'	10.171	453.38	'3A'	10.505	466.43	'6D'	10.840	479.49	'A0'	11.174	492.54	'D3'	11.508
440.58	'08'	10.178	453.63	'3B'	10.512	466.69	'6E'	10.846	479.74	'A1'	11.180	492.80	'D4'	11.515
440.83	'09'	10.184	453.89	'3C'	10.519	466.94	'6F'	10.853	480.00	'A2'	11.187	493.06	'D5'	11.521
441.09	'0A'	10.191	454.14	'3D'	10.525	467.20	'70'	10.859	480.26	'A3'	11.194	493.31	'D6'	11.528
441.34	'0B'	10.197	454.40	'3E'	10.532	467.46	'71'	10.866	480.51	'A4'	11.200	493.57	'D7'	11.534
441.60	'0C'	10.204	454.66	'3F'	10.538	467.71	'72'	10.872	480.77	'A5'	11.207	493.82	'D8'	11.541
441.86	'0D'	10.211	454.91	'40'	10.545	467.97	'73'	10.879	481.02	'A6'	11.213	494.08	'D9'	11.547
442.11	'0E'	10.217	455.17	'41'	10.551	468.22	'74'	10.886	481.28	'A7'	11.220	494.34	'DA'	11.554
442.37	'0F'	10.224	455.42	'42'	10.558	468.48	'75'	10.892	481.54	'A8'	11.226	494.59	'DB'	11.561
442.62	'10'	10.230	455.68	'43'	10.564	468.74	'76'	10.899	481.79	'A9'	11.233	494.85	'DC'	11.567
442.88	'11'	10.237	455.94	'44'	10.571	468.99	'77'	10.905	482.05	'AA'	11.239	495.10	'DD'	11.574
443.14	'12'	10.243	456.19	'45'	10.578	469.25	'78'	10.912	482.30	'AB'	11.246	495.36	'DE'	11.580
443.39	'13'	10.250	456.45	'46'	10.584	469.50	'79'	10.918	482.56	'AC'	11.253	495.62	'DF'	11.587
443.65	'14'	10.256	456.70	'47'	10.591	469.76	'7A'	10.925	482.82	'AD'	11.259	495.87	'E0'	11.593
443.90	'15'	10.263	456.96	'48'	10.597	470.02	'7B'	10.931	483.07	'AE'	11.266	496.13	'E1'	11.600
444.16	'16'	10.269	457.22	'49'	10.604	470.27	'7C'	10.938	483.33	'AF'	11.272	496.38	'E2'	11.606
444.42	'17'	10.276	457.47	'4A'	10.610	470.53	'7D'	10.945	483.58	'B0'	11.279	496.64	'E3'	11.613
444.67	'18'	10.283	457.73	'4B'	10.617	470.78	'7E'	10.951	483.84	'B1'	11.285	496.90	'E4'	11.620
444.93	'19'	10.289	457.98	'4C'	10.623	471.04	'7F'	10.958	484.10	'B2'	11.292	497.15	'E5'	11.626
445.18	'1A'	10.296	458.24	'4D'	10.630	471.30	'80'	10.964	484.35	'B3'	11.298	497.41	'E6'	11.633
445.44	'1B'	10.302	458.50	'4E'	10.636	471.55	'81'	10.971	484.61	'B4'	11.305	497.66	'E7'	11.639
445.70	'1C'	10.309	458.75	'4F'	10.643	471.81	'82'	10.977	484.86	'B5'	11.312	497.92	'E8'	11.646
445.95	'1D'	10.315	459.01	'50'	10.650	472.06	'83'	10.984	485.12	'B6'	11.318	498.18	'E9'	11.652
446.21	'1E'	10.322	459.26	'51'	10.656	472.32	'84'	10.990	485.38	'B7'	11.325	498.43	'EA'	11.659
446.46	'1F'	10.328	459.52	'52'	10.663	472.58	'85'	10.997	485.63	'B8'	11.331	498.69	'EB'	11.665
446.72	'20'	10.335	459.78	'53'	10.669	472.83	'86'	11.003	485.89	'B9'	11.338	498.94	'EC'	11.672
446.98	'21'	10.342	460.03	'54'	10.676	473.09	'87'	11.010	486.14	'BA'	11.344	499.20	'ED'	11.679
447.23	'22'	10.348	460.29	'55'	10.682	473.34	'88'	11.017	486.40	'BB'	11.351	499.46	'EE'	11.685
447.49	'23'	10.355	460.54	'56'	10.689	473.60	'89'	11.023	486.66	'BC'	11.357	499.71	'EF'	11.692
447.74	'24'	10.361	460.80	'57'	10.695	473.86	'8A'	11.030	486.91	'BD'	11.364	499.97	'F0'	11.698
448.00	'25'	10.368	461.06	'58'	10.702	474.11	'8B'	11.036	487.17	'BE'	11.370	500.22	'F1'	11.705
448.26	'26'	10.374	461.31	'59'	10.709	474.37	'8C'	11.043	487.42	'BF'	11.377	500.48	'F2'	11.711
448.51	'27'	10.381	461.57	'5A'	10.715	474.62	'8D'	11.049	487.68	'C0'	11.384	500.74	'F3'	11.718
448.77	'28'	10.387	461.82	'5B'	10.722	474.88	'8E'	11.056	487.94	'C1'	11.390	500.99	'F4'	11.724
449.02	'29'	10.394	462.08	'5C'	10.728	475.14	'8F'	11.062	488.19	'C2'	11.397	501.25	'F5'	11.731
449.28	'2A'	10.401	462.34	'5D'	10.735	475.39	'90'	11.069	488.45	'C3'	11.403	501.50	'F6'	11.737
449.54	'2B'	10.407	462.59	'5E'	10.741	475.65	'91'	11.076	488.70	'C4'	11.410	501.76	'F7'	11.744
449.79	'2C'	10.414	462.85	'5F'	10.748	475.90	'92'	11.082	488.96	'C5'	11.416	502.02	'F8'	11.751
450.05	'2D'	10.420	463.10	'60'	10.754	476.16	'93'	11.089	489.22	'C6'	11.423	502.27	'F9'	11.757
450.30	'2E'	10.427	463.36	'61'	10.761	476.42	'94'	11.095	489.47	'C7'	11.429	502.53	'FA'	11.764
450.56	'2F'	10.433	463.62	'62'	10.768	476.67	'95'	11.102	489.73	'C8'	11.436	502.78	'FB'	11.770
450.82	'30'	10.440	463.87	'63'	10.774	476.93	'96'	11.108	489.98	'C9'	11.443	503.04	'FC'	11.777
451.07	'31'	10.446	464.13	'64'	10.781	477.18	'97'	11.115	490.24	'CA'	11.449	503.30	'FD'	11.783
451.33	'32'	10.453	464.38	'65'	10.787	477.44	'98'	11.121	490.50	'CB'	11.456	503.55	'FE'	11.790



L1 = 3122 138 2021/TOKO 85 ACS-4238 A
L2 = 3122 138 2022/TOKO 85 ACS-4260 SEJ

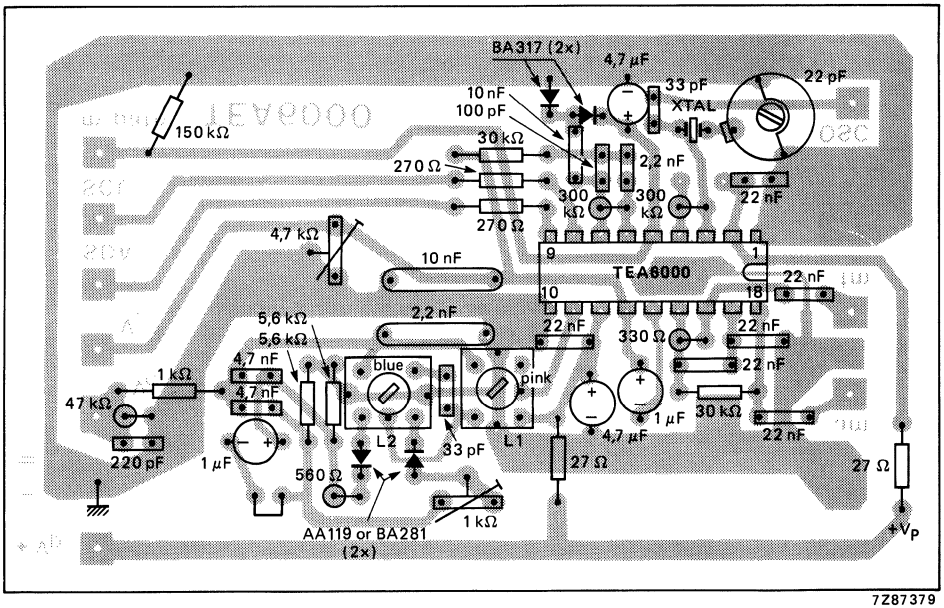
Fig. 6 MUSTI test and application circuit.
Germanium diodes AA119 are required in the test circuit only.
In a complete FM channel (inclusive FM front end) the silicon diodes BA281 are recommended.

S open = without muting
S closed = with muting
} for measuring purpose only.



7Z87380

Fig. 7 Track side of printed-circuit board.



7Z87379

Fig. 8 Component side of printed-circuit board.

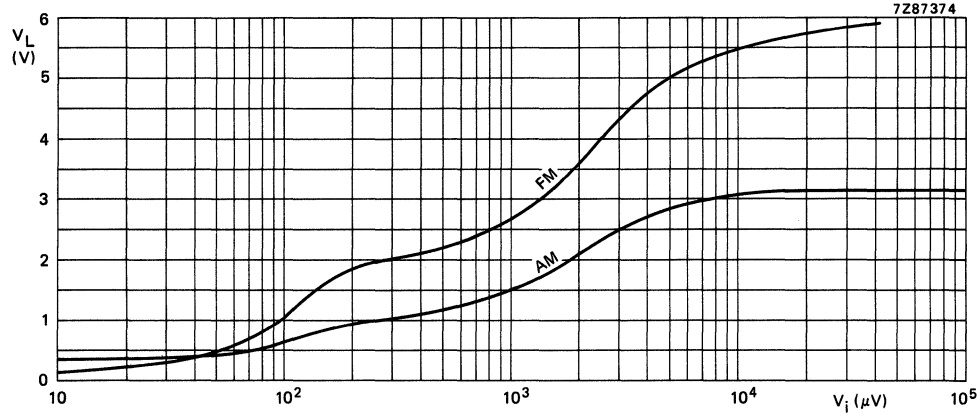


Fig. 9 Level detector output as a function of input voltage.

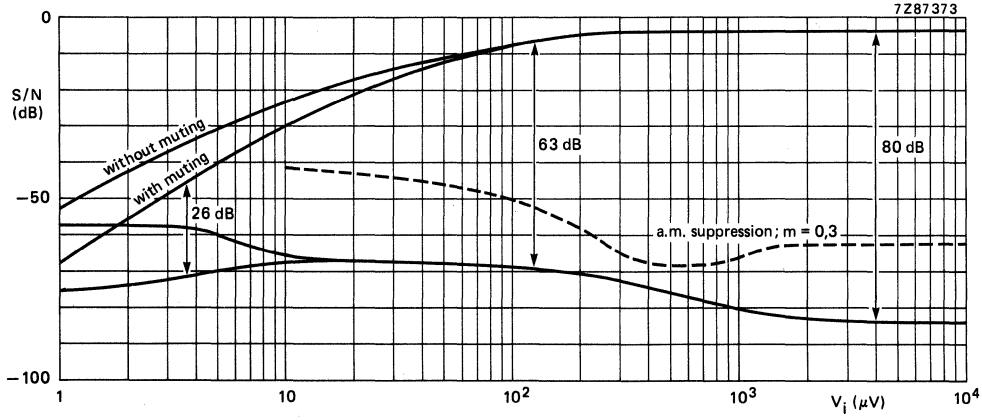


Fig. 10 Signal-to-noise ratio as a function of FM input voltage.
f_i = 10,7 MHz; Δf = 22,5 kHz; f_{mod} = 1 kHz; 0 dB = 245 mV.

GENERAL DESCRIPTION

The SAA3004 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The SAA3004 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

The SAA3004 has the following features:

- Flashed or modulated transmission
- 7 sub-system addresses
- Up to 64 commands per sub-system address
- High-current remote output at V_{DD} = 6 V ($-I_{OH}$ = 40 mA)
- Low number of additional components
- Key release detection by toggle bits
- Very low stand-by current ($< 2\ \mu A$)
- Operational current < 2 mA at 6 V supply
- Wide supply voltage range (4 to 11 V)
- Ceramic resonator controlled frequency (typ. 450 kHz)
- Encapsulation: 20-lead plastic DIL or 20-lead plastic mini-pack (SO-20)

PACKAGE OUTLINES

20-lead DIL; plastic (SOT-146C1).
20-lead mini-pack; plastic (SO-20; SOT-163AC3).

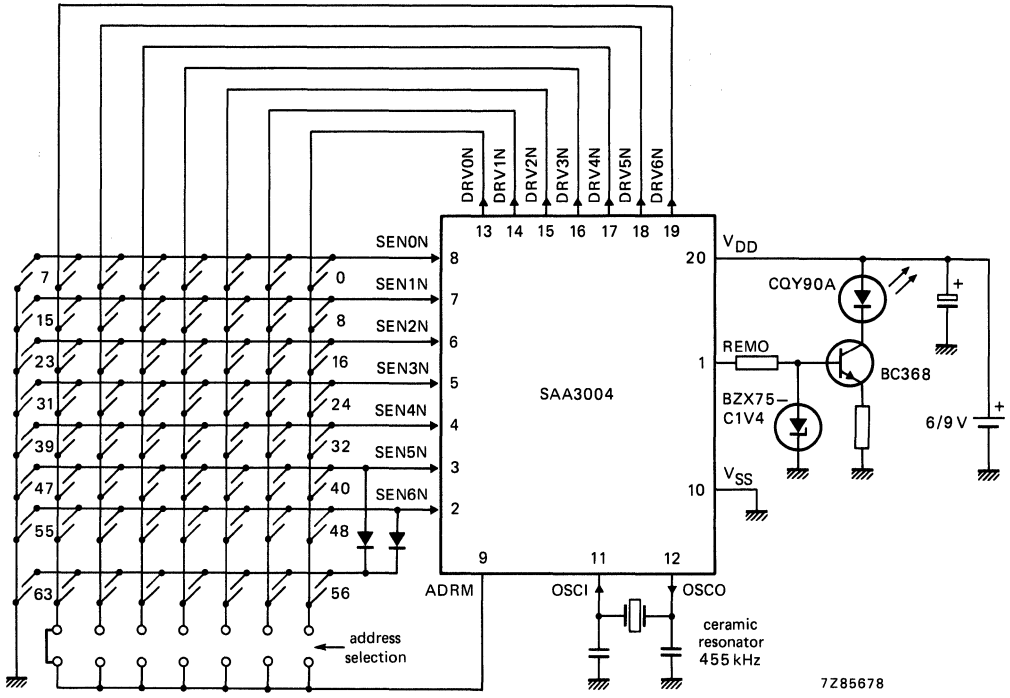


Fig. 1 Transmitter with SAA3004.

INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in Fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable.The sense inputs have P-channel pull-up transistors, so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

Address mode input (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode. This allows the definition of seven sub-system addresses as shown in Table 3. If driver DRV6N is connected to ADRM the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by presssing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if driver DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in transmitters for more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4.

A change of the sub-system address will not start a transmission.

Remote control signal output (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in Tables 1 and 2.

The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see Fig. 3).

The format of the output data is given in Figs 2 and 3. In the flashed transmission mode the data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A, which are defined by the selected key.

In the modulated transmission mode the first toggle bit T1 is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence.

The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command.

The codes for the sub-system address and the selected key are given in Tables 3 and 4.

Oscillator input/output (OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 400 kHz and 500 kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on. Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see Fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch. In contradiction to the command code the sub-system address is sensed only within the *first* scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key-stroke sequence (see Fig. 5) the command code is always altered in accordance with the sensed key.

Multiple key-stroke protection

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see Fig. 5). In case of a multiple key-stroke the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix:

FUNCTIONAL DESCRIPTION (continued)

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored.
- SEN5N and SEN6N are not protected against multiple key-stroke on the same driver line, because this condition has been used for the definition of additional codes (code numbers 56 to 63).

Output sequence (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in Figs 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see Fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

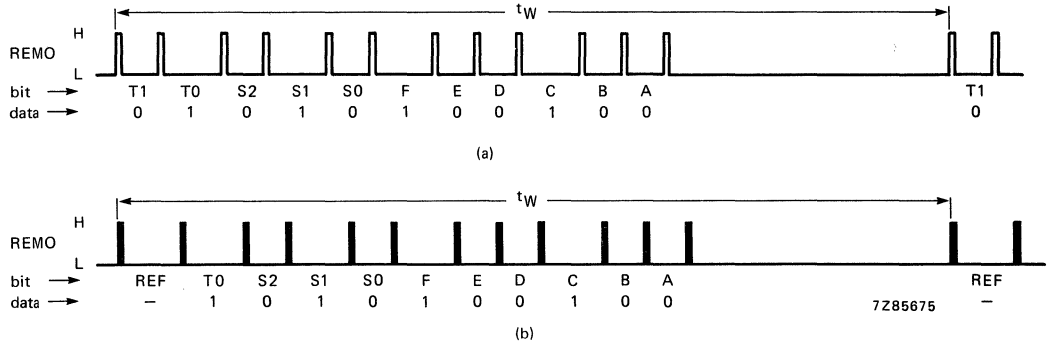
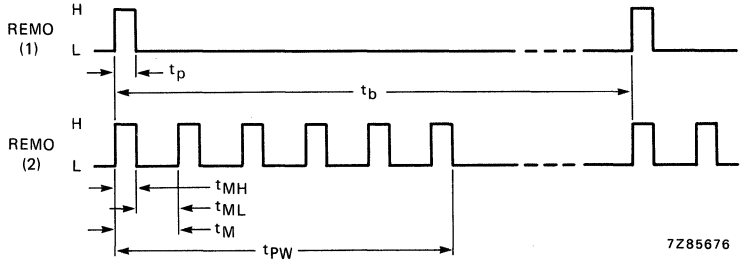


Fig. 2 Data format of REMO output; REF = reference time; T0 and T1 = toggle bits; S0, S1 and S2 = system address; A, B, C, D, E and F = command bits.
(a) flashed mode: transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).
(b) modulated mode: transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).



(1) Flashed pulse.
(2) Modulated pulse ($t_{PW} = (5 \times t_M) + t_{MH}$.

Fig. 3 REMO output waveform.

DEVELOPMENT SAMPLE DATA

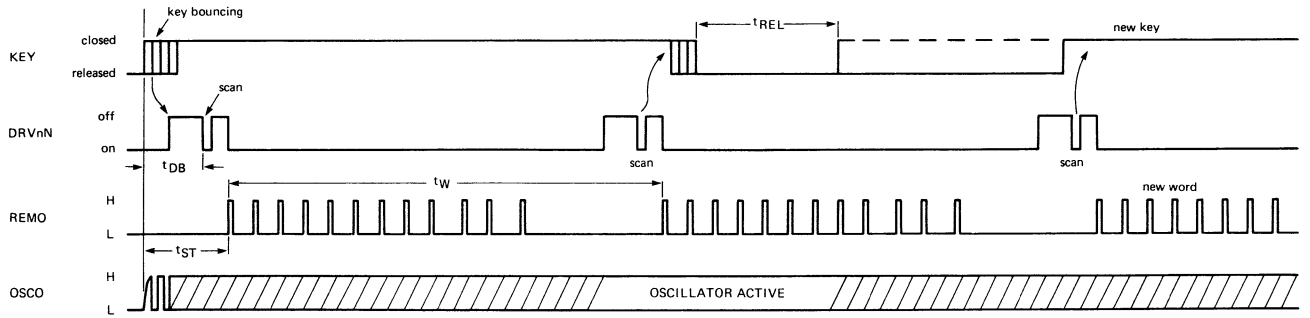


Fig. 4 Single key-stroke sequence.
Debounce time: $t_{DB} = 4$ to $9 \times T_o$.
Start time: $t_{ST} = 5$ to $10 \times T_o$.
Minimum release time: $t_{REL} = T_o$.
Word distance: t_W.

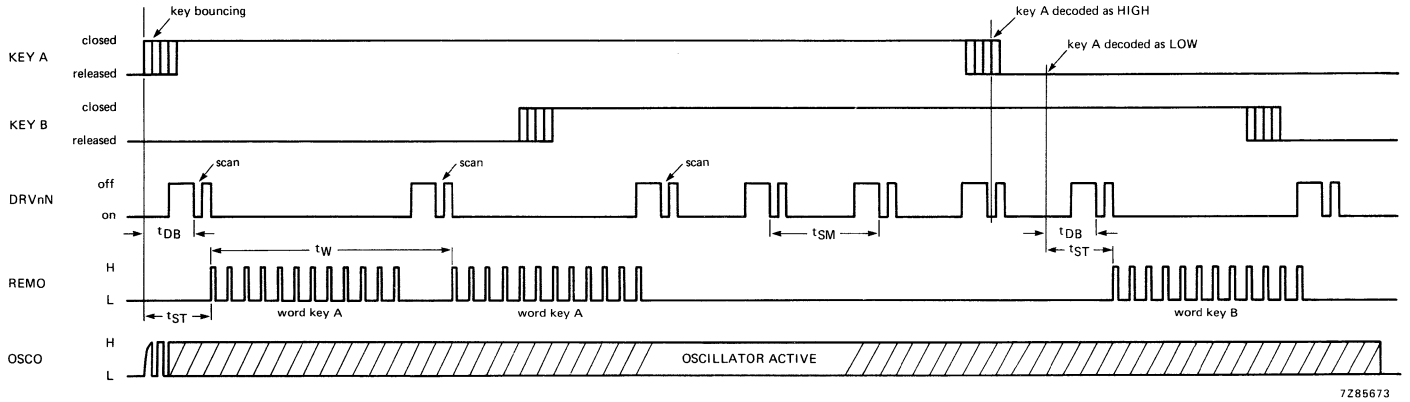


Fig. 5 Multiple key-stroke sequence.
Scan rate multiple key-stroke: $t_{SM} = 6$ to $10 \times T_o$.
For t_{DB}, t_{ST} and t_W see Fig. 4.

Table 1 Pulse train timing

mode	T_o ms	t_p µs	t_M µs	t_{ML} µs	t_{MH} µs	t_W ms
flashed	2,53	8,8	–	–	–	121
modulated	2,53	–	26,4	17,6	8,8	121

f_{osc}	455 kHz	$t_{osc} = 2{,}2\ \mu s$
t_p	$4 \times t_{osc}$	flashed pulse width
t_M	$12 \times t_{osc}$	modulation period
t_{ML}	$8 \times t_{osc}$	modulation period LOW
t_{MH}	$4 \times t_{osc}$	modulation period HIGH
T_o	$1152 \times t_{osc}$	basic unit of pulse distance
t_W	$55\,296 \times t_{osc}$	word distance

Table 2 Pulse train separation (t_b)

code	t_b
logic "0"	$2 \times T_o$
logic "1"	$3 \times T_o$
reference time	$3 \times T_o$
toggle bit time	$2 \times T_o$ or $3 \times T_o$

Table 3 Transmission mode and sub-system address selection

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by a diode.

mode	sub-system address				driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	o						
A	2	0	0	1	X	o					
S	3	0	1	0	X	X	o				
H	4	0	1	1	X	X	X	o			
E	5	1	0	0	X	X	X	X	o		
D	6	1	0	1	X	X	X	X	X	o	
M											
O	0	1	1	1							o
D	1	0	0	0	o						o
U	2	0	0	1	X	o					o
L	3	0	1	0	X	X	o				o
A	4	0	1	1	X	X	X	o			o
T	5	1	0	0	X	X	X	X	o		o
E	6	1	0	1	X	X	X	X	X	o	o
D											

o = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 Key codes

matrix drive	matrix sense	code F	E	D	C	B	A	matrix position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1	**			8 to 15
*	SEN2N	0	1	0	**			16 to 23
*	SEN3N	0	1	1	**			24 to 31
*	SEN4N	1	0	0	**			32 to 39
*	SEN5N	1	0	1	**			40 to 47
*	SEN6N	1	1	0	**			48 to 55
*	SEN5N and SEN6N	1	1	1	**			56 to 63

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5N/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

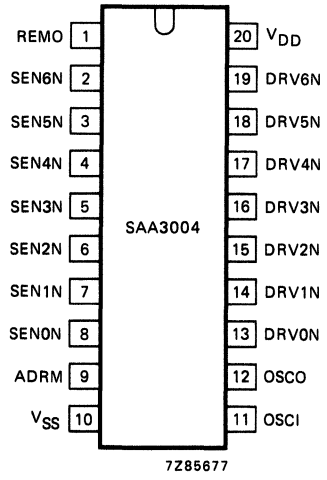


Fig. 6 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	key matrix sense inputs
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address mode control input
10	V_{SS}	ground
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	key matrix drive outputs
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to +15		V
Input voltage range	V_I	−0,5 to V_{DD} +0,5		V
Output voltage range	V_O	−0,5 to V_{DD} +0,5		V
D.C. current into any input or output	±I	max.	10	mA
Peak REMO output current during 10 μs; duty factor = 1%	$-I_{(REMO)M}$	max.	300	mA
Power dissipation per package for T_{amb} = −20 to +70 °C	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−55 to +150		°C
Operating ambient temperature range	T_{amb}	−20 to +70		°C

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage T_{amb} = 0 to +70 °C	–	V_{DD}	4	–	11	V
Supply current; active f_{osc} = 455 kHz; REMO output unloaded	6 9	I_{DD} I_{DD}	– –	1 3	– –	mA mA
Supply current; inactive (stand-by mode) T_{amb} = 25 °C	6 9	I_{DD} I_{DD}	– –	– –	2 2	µA µA
Oscillator frequency (ceramic resonator)	4 to 11	f_{osc}	400	–	500	kHz
Keyboard matrix						
Inputs SEN0N to SEN6N						
Input voltage LOW	4 to 11	V_{IL}	–	–	0,2 x V_{DD}	V
Input voltage HIGH	4 to 11	V_{IH}	0,8 x V_{DD}	–	–	V
Input current V_I = 0 V	4 11	$-I_I$ $-I_I$	10 30	– –	100 300	µA µA
Input leakage current V_I = V_{DD}	11	I_I	–	–	1	µA
Outputs DRV0N to DRV6N						
Output voltage "ON" I_O = 0,1 mA I_O = 1,0 mA	4 11	V_{OL} V_{OL}	– –	– –	0,3 0,5	V V
Output current "OFF" V_O = 11 V	11	I_O	–	–	10	µA
Control input ADRM						
Input voltage LOW	–	V_{IL}	–	–	0,8 x V_{DD}	V
Input voltage HIGH	–	V_{IH}	0,2 x V_{DD}	–	–	V
Input current (switched P- and N-channel pull-up/ pull-down)						
Pull-up active stand-by voltage: 0 V	4 11	I_{IL} I_{IL}	10 30	– –	100 300	µA µA
Pull-down active stand-by voltage: V_{DD}	4 11	I_{IH} I_{IH}	10 30	– –	100 300	µA µA

5

CHARACTERISTICS (continued)

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Data output REMO						
Output voltage HIGH	6	V_{OH}	3	–	–	V
$-I_{OH}$ = 40 mA	9	V_{OH}	6	–	–	V
Output voltage LOW	6	V_{OL}	–	–	0,2	V
I_{OL} = 0,3 mA	9	V_{OL}	–	–	0,1	V
Oscillator						
Input current OSCI at V_{DD}	6	I_I	0,8	–	2,7	μA
Output voltage HIGH $-I_{OL}$ = 0,1 mA	6	V_{OH}	–	–	$V_{DD}-0,6$	V
Output voltage LOW I_{OH} = 0,1 mA	6	V_{OL}	–	–	0,6	V

GENERAL DESCRIPTION

The SAA3006 is intended as a general purpose (RC-5) infrared remote control system for use where only low supply voltages are available. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

Features

- Low supply voltage requirements
- Very low current consumption
- For infrared transmission link
- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Transmission biphase technique
- Short transmission times; speed-up of system reaction time
- Single-pin oscillator input
- Input protection
- Test mode facility

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	2 to 7	V
Input voltage range	V_I	0,5 to (V_{DD} + 0,5)	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)	V*
Output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	−25 to +85	°C

* V_{DD} + 0,5 V not to exceed 9 V.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

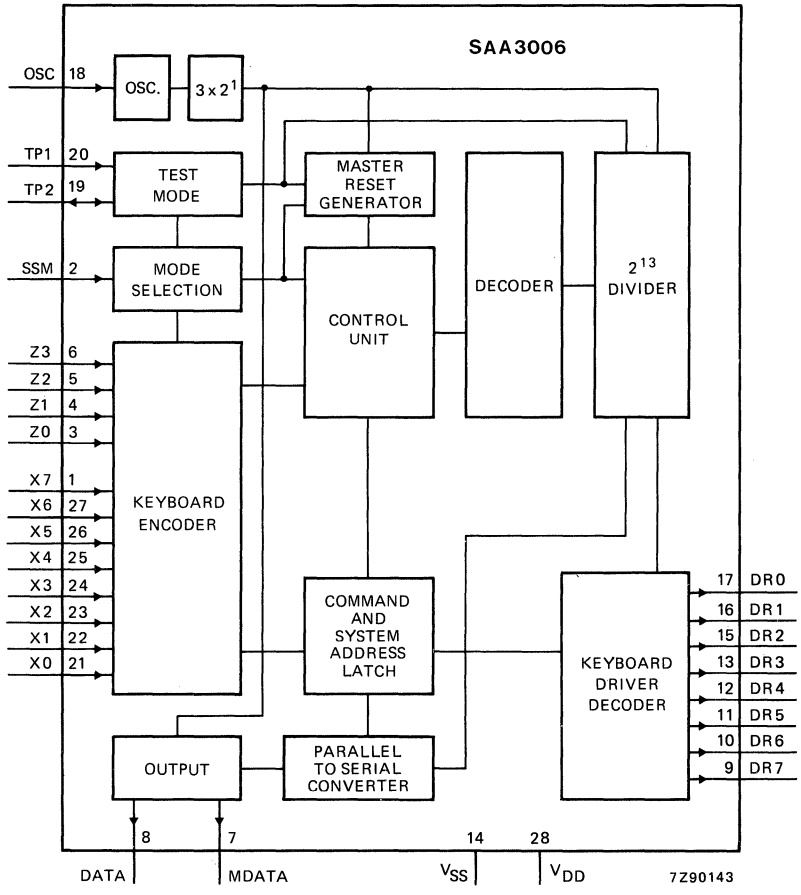


Fig. 1 Block diagram.

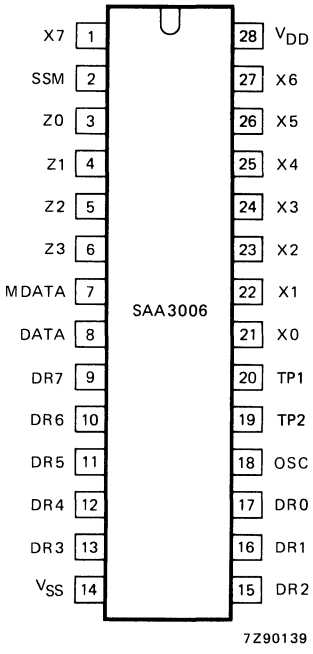
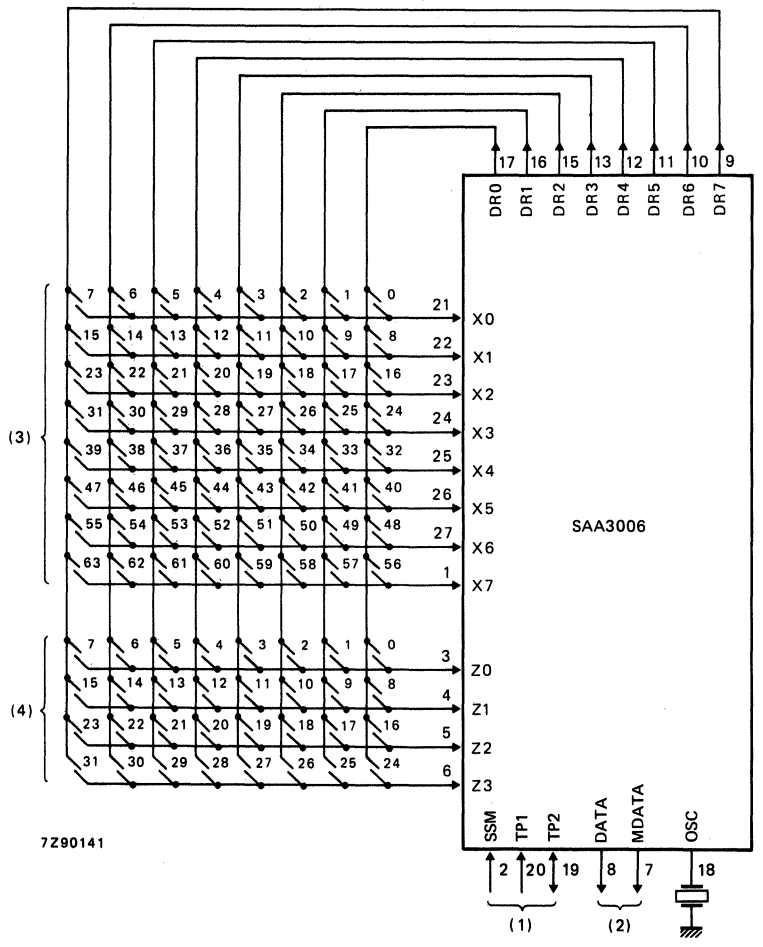


Fig. 2 Pinning diagram.

PINNING

14	V_{SS}	negative supply (ground)
28	V_{DD}	positive supply
21	X0	keyboard command inputs with P-channel pull-up transistors
22	X1	
23	X2	
24	X3	
25	X4	
26	X5	
27	X6	
1	X7	
3	Z0	keyboard system inputs with P-channel pull-up transistors
4	Z1	
5	Z2	
6	Z3	
2	SSM	system mode selection input
20	TP1	test input
19	TP2	test input/output
18	OSC	oscillator input
17	DR0	scan driver output with open drain N-channel transistors
16	DR1	
15	DR2	
13	DR3	
12	DR4	
11	DR5	
10	DR6	
9	DR7	
7	MDATA	remote signal outputs (3-state outputs)
8	DATA	

5



(1) Control inputs for operating modes, test modes and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 x 8.
(4) Keyboard system code matrix 4 x 8.

Fig. 3 Keyboard interconnection.

FUNCTIONAL DESCRIPTION

Combined system mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z- or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches, depending on whether sensing was found in the Z- or X-input matrix. After latching a system address number, the device will generate the last command (i.e. all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single system mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off, those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

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Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

The oscillator is formed by a ceramic resonator (catalogue number 2422 540 98021 or equivalent) feeding the single-pin input OSC. Direct connection is made for supply voltages in the range 2 to 5,25 V but it is necessary to fit a 10 kΩ resistor in series with the resonator when using supply voltages in the range 2,6 to 7 V.

Key-release detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

FUNCTIONAL DESCRIPTION (continued)

Outputs

The output DATA carries the generated information according to the format given in Fig. 4 and Tables 2 and 3. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Fig. 5.

The code consists of four parts:

- Start part formed by 2 bits (two times a logical '1');
- Control part formed by 1 bit;
- System part formed by 5 bits;
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of 1/12 of the oscillator frequency, so that each bit is presented as a burst of 32 pulses. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation all the driver outputs go into the high ohmic state; a scanning procedure is then started so that the outputs are switched into the conducting state one after the other.

Reset action

The circuit will be reset immediately when a key release occurs during:

- debounce time;
- between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:

- the key is released while one of the driver outputs is in the low-ohmic '0' state;
- the key is released before detection of that key;
- there is no wired connection in the Z-DR matrix while SSM is HIGH.

Test pin

The test pins TP1 and TP2 are used for testing in conjunction with inputs Z2 and Z3 as shown in Table 1.

Table 1 Test functions

TP1	TP2	Z2	Z3	function
LOW	LOW	matrix input	matrix input	normal
LOW	HIGH	matrix input	matrix input	scan + output frequency six times faster than normal
HIGH	output $f_{OSC}{}^{6}$	LOW	LOW	reset
HIGH	output $f_{OSC}{}^{6}$	HIGH	HIGH	output frequency 3×2^{7} faster than normal

KEY ACTIVITIES

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 7 kΩ.

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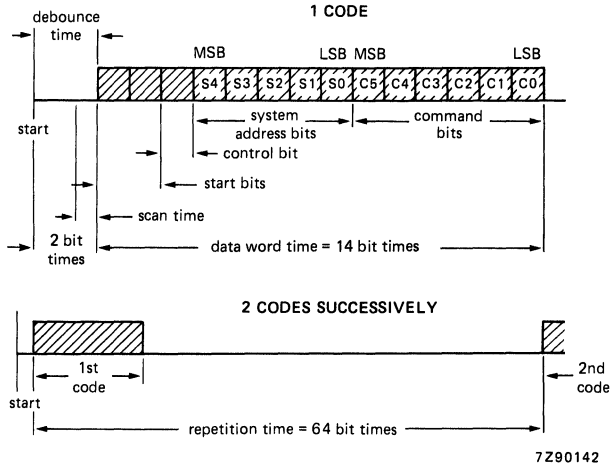

Fig. 4 DATA output format (RC-5).

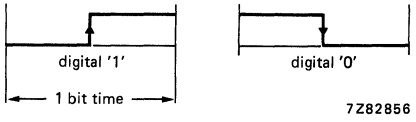

Fig. 5 Biphase transmission code; 1 bit time = $3 \times 2^8 \times T_{OSC}$ (typically 1,778 ms) where T_{OSC} is the oscillator period time.

Table 2 Command matrix X-DR

code no.	X-lines X.. 0	1	2	3	4	5	6	7	DR-lines DR.. 0	1	2	3	4	5	6	7	command bits C.. 5	4	3	2	1	0
0	●								●								0	0	0	0	0	0
1	●									●							0	0	0	0	0	1
2	●										●						0	0	0	0	1	0
3	●											●					0	0	0	0	1	1
4	●												●				0	0	0	1	0	0
5	●													●			0	0	0	1	0	1
6	●														●		0	0	0	1	1	0
7	●															●	0	0	0	1	1	1
8		●							●								0	0	1	0	0	0
9		●								●							0	0	1	0	0	1
10		●									●						0	0	1	0	1	0
11		●										●					0	0	1	0	1	1
12		●											●				0	0	1	1	0	0
13		●												●			0	0	1	1	0	1
14		●													●		0	0	1	1	1	0
15		●														●	0	0	1	1	1	1
16			●						●								0	1	0	0	0	0
17			●							●							0	1	0	0	0	1
18			●								●						0	1	0	0	1	0
19			●									●					0	1	0	0	1	1
20			●										●				0	1	0	1	0	0
21			●											●			0	1	0	1	0	1
22			●												●		0	1	0	1	1	0
23			●													●	0	1	0	1	1	1
24				●					●								0	1	1	0	0	0
25				●						●							0	1	1	0	0	1
26				●							●						0	1	1	0	1	0
27				●								●					0	1	1	0	1	1
28				●									●				0	1	1	1	0	0
29				●										●			0	1	1	1	0	1
30				●											●		0	1	1	1	1	0
31				●												●	0	1	1	1	1	1

code no.	X-lines X.. 0	1	2	3	4	5	6	7	DR-lines DR.. 0	1	2	3	4	5	6	7	command bits C.. 5	4	3	2	1	0
32					●				●								1	0	0	0	0	0
33					●					●							1	0	0	0	0	1
34					●						●						1	0	0	0	1	0
35					●							●					1	0	0	0	1	1
36					●								●				1	0	0	1	0	0
37					●									●			1	0	0	1	0	1
38					●										●		1	0	0	1	1	0
39					●											●	1	0	0	1	1	1
40						●			●								1	0	1	0	0	0
41						●				●							1	0	1	0	0	1
42						●					●						1	0	1	0	1	0
43						●						●					1	0	1	0	1	1
44						●							●				1	0	1	1	0	0
45						●								●			1	0	1	1	0	1
46						●									●		1	0	1	1	1	0
47						●										●	1	0	1	1	1	1
48							●		●								1	1	0	0	0	0
49							●			●							1	1	0	0	0	1
50							●				●						1	1	0	0	1	0
51							●					●					1	1	0	0	1	1
52							●						●				1	1	0	1	0	0
53							●							●			1	1	0	1	0	1
54							●								●		1	1	0	1	1	0
55							●									●	1	1	0	1	1	1
56								●	●								1	1	1	0	0	0
57								●		●							1	1	1	0	0	1
58								●			●						1	1	1	0	1	0
59								●				●					1	1	1	0	1	1
60								●					●				1	1	1	1	0	0
61								●						●			1	1	1	1	0	1
62								●							●		1	1	1	1	1	0
63								●								●	1	1	1	1	1	1

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Table 3 System matrix Z-DR

system no.	Z-lines Z..				DR-lines DR..								system bits S..				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	●				●								0	0	0	0	0
1	●					●							0	0	0	0	1
2	●						●						0	0	0	1	0
3	●							●					0	0	0	1	1
4	●								●				0	0	1	0	0
5	●									●			0	0	1	0	1
6	●										●		0	0	1	1	0
7	●											●	0	0	1	1	1
8		●			●								0	1	0	0	0
9		●				●							0	1	0	0	1
10		●					●						0	1	0	1	0
11		●						●					0	1	0	1	1
12		●							●				0	1	1	0	0
13		●								●			0	1	1	0	1
14		●									●		0	1	1	1	0
15		●										●	0	1	1	1	1
16			●		●								1	0	0	0	0
17			●			●							1	0	0	0	1
18			●				●						1	0	0	1	0
19			●					●					1	0	0	1	1
20			●						●				1	0	1	0	0
21			●							●			1	0	1	0	1
22			●								●		1	0	1	1	0
23			●									●	1	0	1	1	1
24				●	●								1	1	0	0	0
25				●		●							1	1	0	0	1
26				●			●						1	1	0	1	0
27				●				●					1	1	0	1	1
28				●					●				1	1	1	0	0
29				●						●			1	1	1	0	1
30				●							●		1	1	1	1	0
31				●								●	1	1	1	1	1

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5	to	8,5	V
Input voltage range	V_I	−0,5	to	$(V_{DD}+0,5)$	V*
Input current	$+I_I$	max.		10	mA
Output voltage range	V_O	−0,5	to	$(V_{DD}+0,5)$	V*
Output current	$+I_O$	max.		10	mA
Power dissipation output OSC	P_O	max.		50	mW
Power dissipation per output (all other outputs)	P_O	max.		100	mW
Total power dissipation per package	P_{tot}	max.		200	mW
Operating ambient temperature range	T_{amb}	−25	to	+85	°C
Storage temperature range	T_{stg}	−55	to	+150	°C

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HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

* V_{DD} + 0,5 V not to exceed 9 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	2	–	7	V
Supply current at I_O = 0 mA for all outputs; X0 to X7 and Z3 at V_{DD}; all other inputs at V_{DD} or V_{SS}; excluding leakage current from open drain N-channel outputs; T_{amb} = 25 °C	7	I_{DD}	–	–	10	μA
Inputs						
Keyboard inputs X and Z with P-channel pull-up transistors						
Input current (each input) at V_I = 0 V; TP = SSM = LOW	2 to 7	$-I_I$	10	–	600	μA
Input voltage HIGH	2 to 7	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	2 to 7	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; TP = HIGH; V_I = 7 V		I_{IR}	–	–	1	μA
V_I = 0 V		$-I_{IR}$	–	–	1	μA
SSM, TP1 and TP2						
Input voltage HIGH	2 to 7	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	2 to 7	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at T_{amb} = 25 °C; V_I = 7 V		I_{IR}	–	–	1	μA
V_I = 0 V		$-I_{IR}$	–	–	1	μA
OSC						
Input leakage current at T_{amb} = 25 °C; V_I = 0 V; TP1 = HIGH; Z2 = Z3 = LOW	2 to 7	$-I_I$	–	–	2	μA

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Outputs						
DATA and MDATA						
Output voltage HIGH at $-I_{OH}$ = 0,4 mA	2 to 7	V_{OH}	V_{DD} −0,3	–	–	V
Output voltage LOW at I_{OL} = 0,6 mA	2 to 7	V_{OL}	–	–	0,3	V
Output leakage current at:						
V_O = 7 V		I_{OR}	–	–	10	μA
V_O = 0 V		$-I_{OR}$	–	–	20	μA
T_{amb} = 25 °C;						
V_O = 7 V		I_{OR}	–	–	1	μA
V_O = 0 V		$-I_{OR}$	–	–	2	μA
DR0 to DR7, TP2						
Output voltage LOW at I_{OL} = 0,3 mA	2 to 7	V_{OL}	–	–	0,3	V
Output leakage current at V_O = 7 V	7	I_{OR}	–	–	10	μA
at V_O = 7 V						
T_{amb} = 25 °C		I_{OR}	–	–	1	μA
OSC						
Oscillator current at OSC = V_{DD}	7	I_{OSC}	4,5	–	30	μA
Oscillator						
Maximum oscillator frequency at C_L = 40 pF (Figs 6 and 7)	2	f_{OSC}	–	–	450	kHz
Free-running oscillator frequency at T_{amb} = 25 °C	2	f_{OSC}	10	–	120	kHz

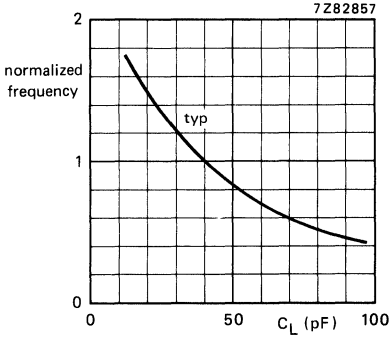


Fig. 6 Typical normalized input frequency as a function of the load (keyboard) capacitance.

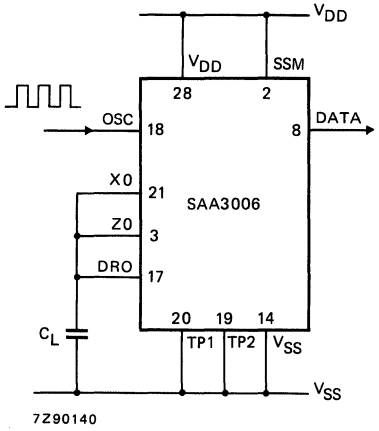


Fig. 7 Test circuit for measurement of maximum oscillator frequency.

GENERAL DESCRIPTION

The SAA3028 is intended for use in general purpose (RC-5) remote control systems. The main function of this integrated circuit is to convert RC-5 biphase coded signals into equivalent binary values. Two input circuits are available: one for RC-5 coded signals only; the other is selectable to accept (1) RC-5 coded signals only, or (2) RC-5 (extended) coded signals only. The input used is that at which an active code is first detected. Coded signals not in RC-5/RC-5(ext) format are rejected. Data input and output is by serial transfer, the output interface being compatible for I^2C bus operation.

Features

- Converts RC-5 or RC-5(ext) biphase coded signals into binary equivalents
- Two data inputs, one fixed (RC-5), one selectable (RC-5/RC-5(ext))
- Rejects all codes not in RC-5/RC-5(ext) format
- I^2C output interface capability
- Power-off facility
- Master/slave addressable for multi-transmitter/receiver applications in RC-5(ext) mode
- Power-on-reset for defined start-up

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,5 to	5,5 V
Supply current (quiescent) at V_{DD} = 5,5 V; T_{amb} = 25 °C	I_{DD}	max.	200 μA
Operating ambient temperature range	T_{amb}	−25 to	+85 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38Z).

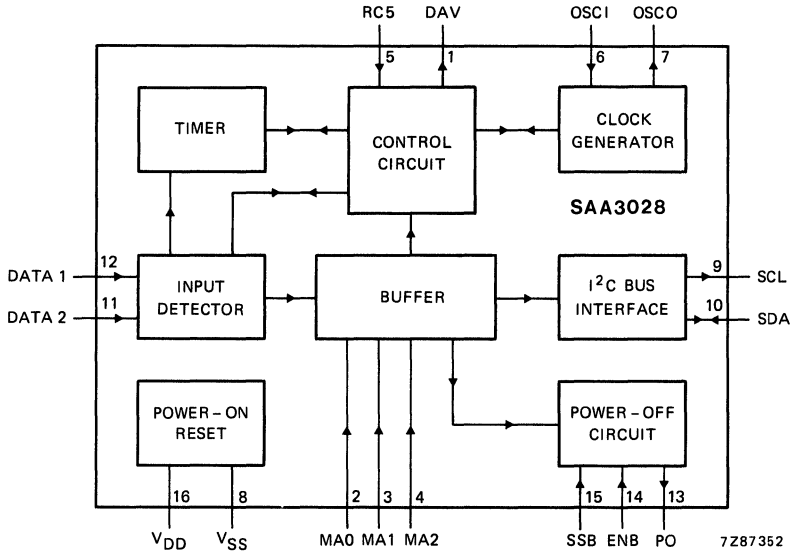


Fig. 1 Block diagram.

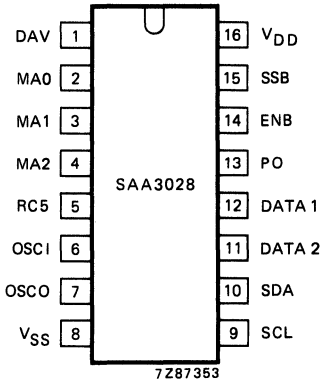


Fig. 2 Pinning diagram.

PINNING

1	DAV	data valid output with open drain N-channel transistor
2	MA0	master address inputs
3	MA1	master address inputs
4	MA2	master address inputs
5	RC5	data 2 input select
6	OSCI	oscillator input
7	OSCO	oscillator output
8	V_{SS}	negative supply (ground)
9	SCL	serial clock line (I^2C bus)
10	SDA	serial data line (I^2C bus)
11	DATA 2	data 2 input
12	DATA 1	data 1 input
13	PO	power-off signal output with open drain N-channel transistor
14	ENB	enable input
15	SSB	set standby input
16	V_{DD}	positive supply (+5 V)

FUNCTIONAL DESCRIPTION

Input function

The two data inputs are accepted into the buffer as follows:

- DATA 1. Only biphase coded signals which conform to the RC-5 format are accepted at this input.
- DATA 2. This input performs according to the logic state of the select input RC5. When RC5 = HIGH, DATA 2 input will accept only RC-5 coded signals. When RC5 = LOW, DATA 2 input will accept only RC-5(ext) coded signals.

The input detector selects the input, DATA 1 or DATA 2, in which a HIGH to LOW transition is first detected. The selected input is then accepted by the buffer for code conversion. All signals received that are not in the RC-5 or RC-5(ext) format are rejected.

Formats of RC-5 and RC-5(ext) biphase coded signals are shown in Figs 3 and 4 respectively; the codes commence from the left of the formats shown. The bit-times of the biphase codes are defined in Fig. 5.

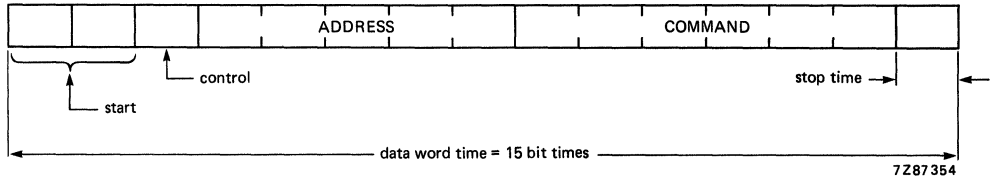


Fig. 3 RC-5 code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

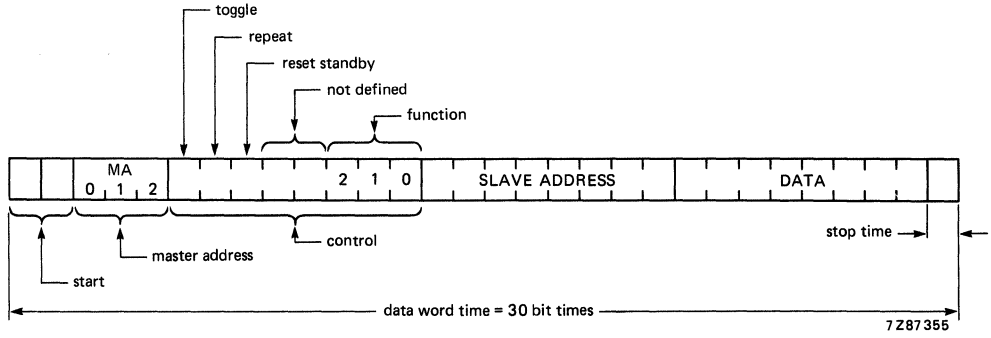


Fig. 4 RC-5(extended) code format: the first start bit is used only for detection and input gain-setting; stop time = 1,5 bit-times (nominal).

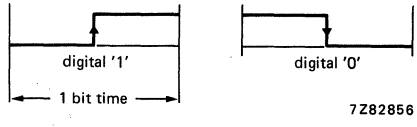


Fig. 5 Biphase code definition: RC-5 bit-time = $2^7 \times T_{OSC}$ = 1,778 ms (typical); RC-5(ext) bit-time = $2^6 \times T_{OSC}$ = 0,89 ms (typical), where T_{OSC} = the oscillator period time.

FUNCTIONAL DESCRIPTION (continued)

More information is added to the input data held in the buffer in order to make it suitable for transmission via the I^2C interface. The information now held in the buffer is as follows:

RC-5 buffer contents		RC-5(ext) buffer contents	
• data valid indicator	1 bit	• data valid indicator	1 bit
• format indicator	1 bit	• format indicator	1 bit
• input indicator	1 bit	• input indicator	1 bit
• control	1 bit	• master address	3 bits
• address data	5 bits	• control	8 bits
• command data	6 bits	• slave address	8 bits
		• data	8 bits

The information assembled in the buffer is subjected to the following controls before being made available at the I^2C interface:

ENB = HIGH — Enables the set standby input SSB.

SSB = LOW — Causes power-off output PO to go HIGH.

PO = HIGH — This occurs when the set standby input SSB = LOW and allows the existing values in the buffer to be overwritten by the new binary equivalent values. After ENB = LOW, SSB is don't care.

PO = LOW — This occurs according to the type of code being processed, as follows:

RC-5. When the binary equivalent value is transferred to the buffer.

RC-5(ext). When the reset standby bit is active and the master address bits are equal in value to the MA0, MA1, MA2 inputs.

At power-on, PO is reset to LOW.

DAV = HIGH — This occurs when the buffer contents are valid. If the buffer is not empty, or an output transfer is taking place, then the new binary values are discarded.

Output function

The data is assembled in the buffer in the format shown in Fig. 6 for RC-5 binary equivalent values, or in the format shown in Fig. 7 for RC-5(ext) binary equivalent values. The data is output serially, starting from the left of the formats shown in Figs 6 and 7.

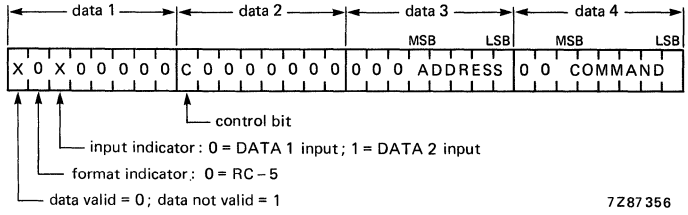


Fig. 6 RC-5 binary equivalent value format.

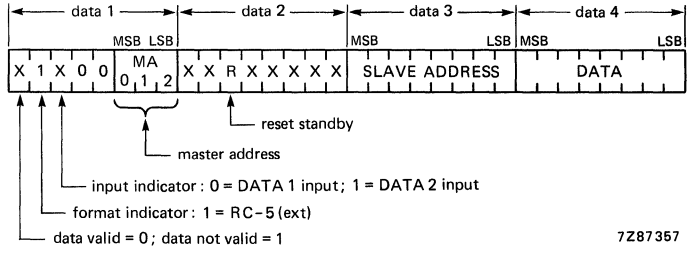


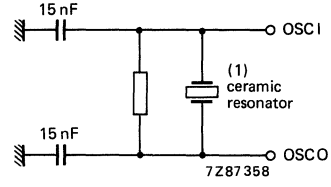
Fig. 7 RC-5(ext) binary equivalent value format.

The output signal DAV, derived in the buffer from the data valid bit, is provided to facilitate use of the transcoder on an interrupt basis. This output is reset to LOW during power-on.

The I^2C interface allows transmission on a bidirectional, two-wire I^2C bus. The interface is a slave transmitter with a built-in slave address, having a fixed 7-bit binary value of 0100110. Serial output of the slave address onto the I^2C bus starts from the left-hand bit.

Oscillator

The oscillator can comprise a ceramic resonator circuit as shown in Fig. 8. The typical frequency of oscillation is 455 kHz.



(1) Catalogue number of ceramic resonator: 2422 540 98008.

Fig. 8 Oscillator circuit.

FUNCTIONAL DESCRIPTION (continued)

I^2C bus transmission

Formats for I^2C transmission in low and high speed modes are shown respectively in Figs 9 and 10.

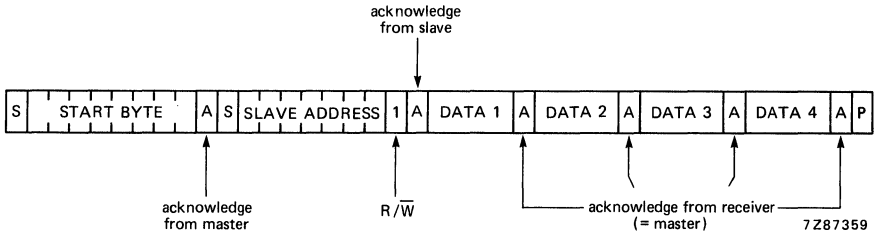


Fig. 9 Format for transmission in I^2C low speed mode.

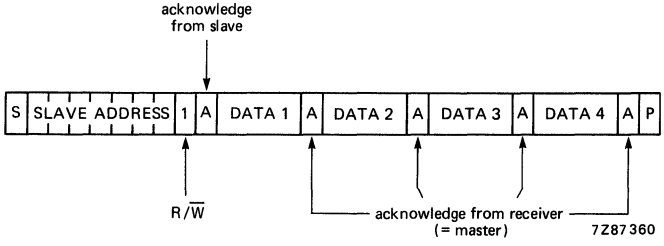


Fig. 10 Format for transmission in I^2C high speed mode.

Note to Figures 9 and 10

When R/$\overline{W}$ bit = 0; the slave generates a NACK (negative acknowledge), leaves the data line HIGH and waits for a stop (P) condition.

When the receiver generates a NACK; the slave leaves the data line HIGH and waits for P (the slave acting as if all data has been transmitted).

When all data has been transmitted, the data line remains HIGH and the slave waits for P.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to	+15	V
Input voltage range	V_I	−0,5 to	(V_{DD}+0,5)	V*
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O	−0,5 to	(V_{DD}+0,5)	V*
Output current	$\pm I_O$	max.	10	mA
Power dissipation output OSCO	P_O	max.	50	mW
Power dissipation per output (all other outputs)	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}	−25 to	+85	°C
Storage temperature range	T_{stg}	−55 to	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −25 to 85 °C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,5	–	5,5	V
Supply current; quiescent at T_{amb} = 25 °C	5,5	I_{DD}	–	–	200	μA
Inputs						
MA0, MA1, MA2, DATA 1, DATA 2, RC5, SCL, ENB, SSB, OSCI						
Input voltage HIGH	4,5 to 5,5	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	4,5 to 5,5	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 5,5 V; T_{amb} = 25 °C	5,5	I_I	–	–	1	μA
Input leakage current at V_I = 0 V; T_{amb} = 25 °C;	5,5	$-I_I$	–	–	1	μA
Outputs						
DAV, PO						
Output voltage LOW at I_{OL} = 1,6 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
OSCO						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	4,5 to 5,5	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,3 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at T_{amb} = 25 °C; V_O = 5,5 V	5,5	I_{OR}	–	–	1	μA
V_O = 0 V	5,5	I_{OR}	–	–	1	μA
SDO						
Output voltage LOW at I_{OL} = 2 mA	4,5 to 5,5	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 5,5 V; T_{amb} = 25 °C	5,5	I_{OR}	–	–	1	μA
Oscillator						
Max. oscillator frequency (Fig. 8)	4,75	f_{OSCI}	500	–	–	kHz

R/C Receiver; R/C Transmitter — SAF1032P/39P

The SAF1032P (receiver/decoder) and the SAF1039P (transmitter) form the basic parts of a sophisticated remote control system (pcm: pulse code modulation) for infrared operation. The ICs can be used, for example, in TV, audio, industrial equipment, etc.
Features:

SAF1032P receiver/decoder:
- 16 programme selection codes
- automatic preset to stand-by at power 'ON', including automatic analogue base settings to 50% and automatic preset of programme selection '1' code
- 3 analogue function controls, each with 63 steps
- single supply voltage
- protection against corrupt codes.

SAF1039P transmitter:
- 32 different control commands
- static keyboard matrix
- current drains from battery only during key closure time
- two transmission modes selectable.

The devices are implemented in LOCMOS (Local Oxidation Complementary MOS) technology to achieve an extremely low power consumption.
Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

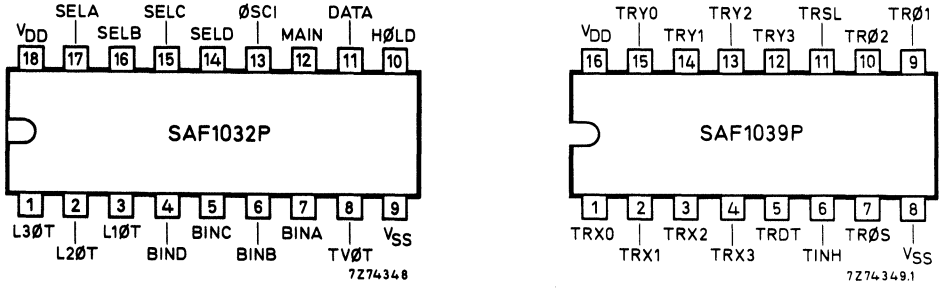


Fig. 1 Pin designations.

PACKAGE OUTLINES

SAF1032P: 18-lead DIL; plastic (SOT-102A).
SAF1039P: 16-lead DIL; plastic (SOT-38Z).

PINNING

To facilitate easy function recognition, each integrated circuit pin has been allocated a code as shown below.

SAF1032P

1	L3ØT	linear output	10	HØLD	control input
2	L2ØT	linear output	11	DATA	data input
3	L1ØT	linear output	12	MAIN	reset input
4	BIND	binary 8 output	13	ØSCI	clock input
5	BINC	binary 4 output	14	SELD	binary 8 output
6	BINB	binary 2 output	15	SELC	binary 4 output
7	BINA	binary 1 output	16	SELB	binary 2 output
8	TVØT	on/off input/output	17	SELA	binary 1 output
9	V_{SS}		18	V_{DD}	

SAF1039P

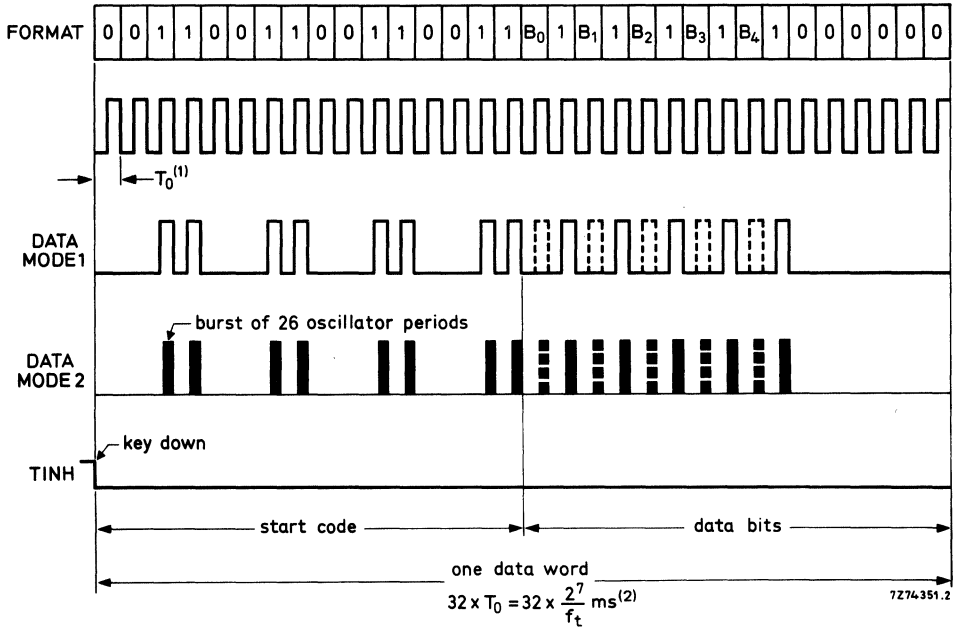
1	TRX0	keyboard input	9	TRØ1	oscillator control input
2	TRX1	keyboard input	10	TRØ2	oscillator control input
3	TRX2	keyboard input	11	TRSL	keyboard select line
4	TRX3	keyboard input	12	TRY3	keyboard input
5	TRDT	data output	13	TRY2	keyboard input
6	TINH	inhibit output/mode select input	14	TRY1	keyboard input
7	TRØS	oscillator output	15	TRY0	keyboard input
8	V_{SS}		16	V_{DD}	

BASIC OPERATING PRINCIPLES

The data to be transmitted are arranged as serial information with a fixed pattern (see Fig. 2), in which the data bit-locations B_0 to B_4 represent the generated key-command code. To cope with IR (infrared) interferences of other sources a selective data transmission is present. Each transmitted bit has a burst of 26 oscillator periods.

Before any operation will be executed in the receiver/decoder chip, the transmitted data must be accepted twice in sequence. This means the start code must be recognized each time a data word is applied and comparison must be true between the data bits of two successively received data words. If both requirements are met, one group of binary output buffers will be loaded with a code defined by the stored data bits, and an internal operation can also take place. See operating code table.

The contents of the 3 analogue function registers are available on the three outputs in a pulse code versus time modulation format after D (digital) to A (analogue) conversion. The proper analogue levels can be obtained by using simple integrated networks. For local control a second transmitter chip (SAF1039P) is used (see Fig. 7).



(1) T_0 = 1 clock period = 128 oscillator periods. (2) f_t in kHz.

Fig. 2 Pattern for data to be transmitted.

TIMING CONSIDERATIONS

The transmitter and receiver operate at different oscillator frequencies. Due to the design neither frequency is very critical, but correlation between them must exist. Calculation of these timing requirements shows the following.

With a tolerance of ±10% on the oscillator frequency (f_t) of the transmitter, the receiver oscillator frequency ($f_r = 3 \times f_t$) must be kept constant with a tolerance of ±20%.
On the other hand, the data pulse generated by the pulse stretcher circuit (at the receiver side) may vary ±25% in duration.

GENERAL DESCRIPTION OF THE SAF1039P TRANSMITTER

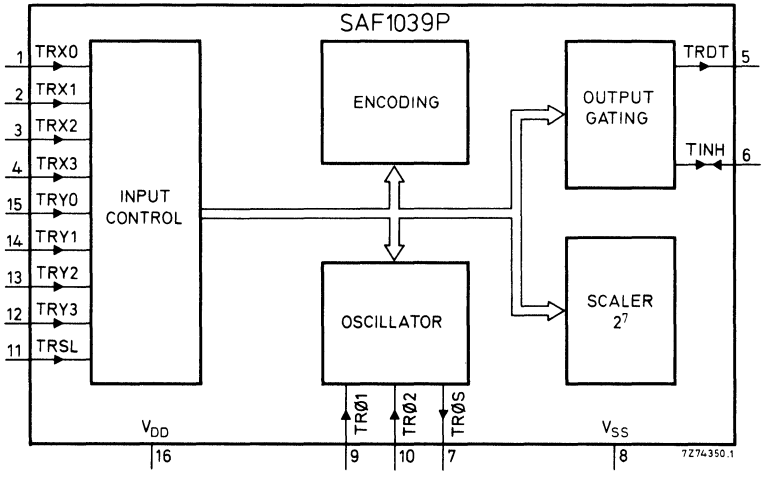


Fig. 3 Block diagram of SAF1039P transmitter.

Any keyboard activity on the inputs TRX0 to TRX3, TRY0 to TRY3 and TRSL will be detected. For a legal key depression, one key down at a time (one TRX and TRY input activated), the oscillator starts running and a data word, as shown on the previous page, is generated and supplied to the output TRDT. If none, or more than 2 inputs are activated at the same time, the input detection logic of the chip will generate an overall reset and the oscillator stops running (no legal key operation).

This means that for each key-bounce the logic will be reset, and by releasing a key the transmitted data are stopped at once.

The minimum key contact time required is the duration of two data words. The on-chip oscillator is frequency controlled with the external components R1 and C1 (see circuit Fig. 6); the addition of resistor R2 means that the oscillator frequency is practically independent of supply voltage variations. A complete data word is arranged as shown in Fig. 2, and has a length of 32 x T_0 ms, where $T_0 = 2^7/f_t$.

Operation mode

	DATA	FUNCTION OF TINH
1	unmodulated: LOCAL operation	output, external pull-up resistor to V_{DD}
2	modulated: REMOTE control	input, connected to V_{SS}

GENERAL DESCRIPTION OF THE SAF1032P RECEIVER/DECODER

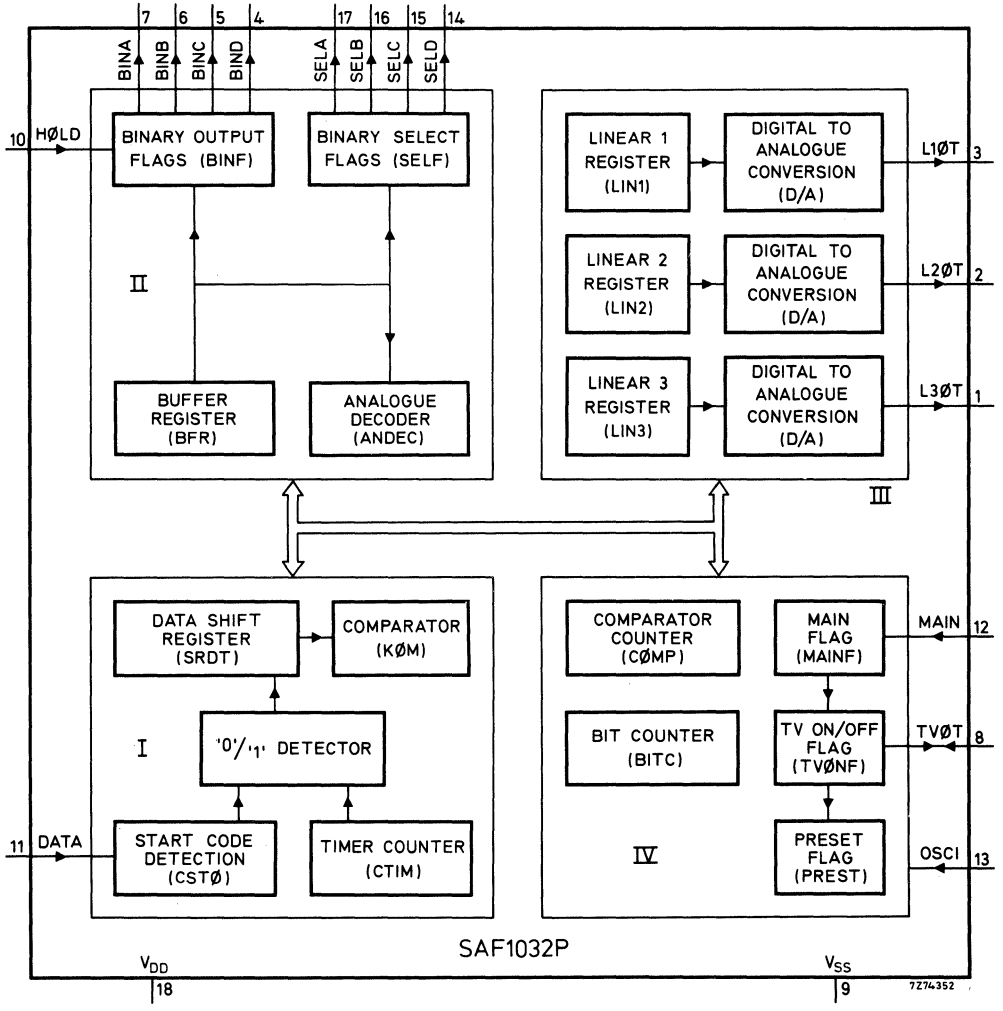


Fig. 4 Block diagram of SAF1032P receiver/decoder.

The logic circuitry of the receiver/decoder chip is divided into four main parts as shown in the block diagram above.

Part I

This part decodes the applied DATA information into logic '1' and '0'.
It also recognizes the start code and compares the stored data-bits with the new data-bits accepted.

Part II

This part stores the programme selection code in the output group (BINF) and memorizes it for condition HØLD = LOW.

It puts the functional code to output group (SELF) during data accept time, and decodes the internally used analogue commands (ANDEC).

Part III

This part controls the analogue function registers (each 6-bits long), and connects the contents of the three registers to the analogue outputs by means of D/A conversion. During sound mute, output L1ØT will be forced to HIGH level.

Part IV

This part keeps track for correct power 'ON' operation, and puts chip in 'stand-by' condition at supply voltage interruptions.

The logic design is dynamic and synchronous with the clock frequency (ØSCI), while the required control timing signals are derived from the bit counter (BITC).

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Operation

Serial information applied to the DATA input will be translated into logic '1' and '0' by means of a time ratio detector.

After recognizing the start code (CSTØ) of the data word, the data bits will be loaded into the data shift register (SRDT). At the first trailing edge of the following data word a comparison (KØM) takes place between the contents of SRDT and the buffer register (BFR). If SRDT equals BFR, the required operation will be executed under control of the comparator counter (CØMP).

As shown in the operating code table on the next page, the 4-bit wide binary output buffer (BINF) will be loaded for BFR0 = '0', while for BFR0 = '1' the binary output buffer (SELF), also 4-bit wide will be activated during the data accept time.

At the same time operations involving the internal commands are executed. The contents of the analogue function registers (each 6-bits long) are controlled over 63 steps, with minimum and maximum detection, while the D/A conversion results in a pulsed output signal with a conversion period of 384 clock periods (see Fig. 5).

First power 'ON' will always put the chip in the 'stand-by' position. This results in an internal clearing of all logic circuitry and a 50% presetting of the contents of the analogue registers (analogue base value). The programme selection '1' code will also be prepared and all the outputs will be non-active (see operating output code table).

From 'stand-by' the chip can be made operational via a programme selection command, generated LOCAL or via REMOTE, or directly by forcing the TV ON/OFF output (TVØT) to zero for at least 2 clock periods of the oscillator frequency.

For POWER ON RESET a negative-going pulse should be applied to input MAIN, when V_{DD} is stabilized; pulse width LOW $\geqslant$ 100 μs.

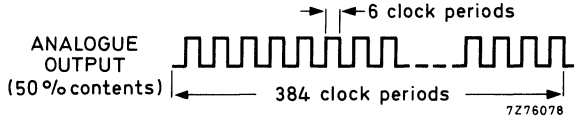

Fig. 5 Analogue output pulses.

OPERATING CODE TABLE

key-matrix position			buffer BFR					BINF (BIN.)				SELF (SEL.)				function
TRX.	TRY.	TRSL	0	1	2	3	4	A	B	C	D	A	B	C	D	
0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	programme select + ON
0	1	0	0	0	0	1	0	1	0	0	0	1	1	1	1	
0	2	0	0	0	1	0	0	0	1	0	0	1	1	1	1	
0	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	
1	0	0	0	1	1	1	0	0	0	1	0	1	1	1	1	
1	1	0	0	1	0	1	0	1	0	1	0	1	1	1	1	
1	2	0	0	1	1	0	0	0	1	1	0	1	1	1	1	
1	3	0	0	1	0	0	0	1	1	1	0	1	1	1	1	
2	0	0	0	0	1	1	1	0	0	0	1	1	1	1	1	programme select + ON
2	1	0	0	0	0	1	1	1	0	0	1	1	1	1	1	
2	2	0	0	0	1	0	1	0	1	0	1	1	1	1	1	
2	3	0	0	0	0	0	1	1	1	0	1	1	1	1	1	
3	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1	
3	1	0	0	1	0	1	1	1	0	1	1	1	1	1	1	
3	2	0	0	1	1	0	1	0	1	1	1	1	1	1	1	
3	3	0	0	1	0	0	1	1	1	1	1	1	1	1	1	
0	0	1	1	0	1	1	0	X	X	X	X	0	1	1	1	analogue base
0	1	1	1	0	0	1	0	X	X	X	X	0	0	1	1	reg. (LIN3) + 1
0	2	1	1	0	1	0	0	X	X	X	X	0	1	0	1	reg. (LIN2) + 1
0	3	1	1	0	0	0	0	X	X	X	X	0	0	0	1	reg. (LIN1) + 1
1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	OFF
1	1	1	1	1	0	1	0	X	X	X	X	1	0	1	1	reg. (LIN3) – 1
1	2	1	1	1	1	0	0	X	X	X	X	1	1	0	1	reg. (LIN2) – 1
1	3	1	1	1	0	0	0	X	X	X	X	1	0	0	1	reg. (LIN1) – 1
2	0	1	1	0	1	1	1	X	X	X	X	0	1	1	0	mute (set/reset)
2	1	1	1	0	0	1	1	X	X	X	X	0	0	1	0	spare functions
2	2	1	1	0	1	0	1	X	X	X	X	0	1	0	0	
2	3	1	1	0	0	0	1	X	X	X	X	0	0	0	0	
3	0	1	1	1	1	1	1	X	X	X	X	1	1	1	0	
3	1	1	1	1	0	1	1	X	X	X	X	1	0	1	0	
3	2	1	1	1	1	0	1	X	X	X	X	1	1	0	0	
3	3	1	1	1	0	0	1	X	X	X	X	1	0	0	0	

Note

Reset mute also on programme select codes, (LIN1) ± 1, and analogue base.

OPERATING OUTPUT CODE

	(BIN.)				(SEL.)				(L.ØT)			TVØT
	A	B	C	D	A	B	C	D	1	2	3	
'stand-by' OFF via remote	0	0	0	0	0	0	0	0	1	0	0	1
ON – 'not hold' condition non-operating	1	1	1	1	1	1	1	1	X	X	X	0
ON – 'hold' condition non-operating	X	X	X	X	1	1	1	1	X	X	X	0

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}-V_{SS}		−0.5 to 11	V
Input voltage	V_I	max.	11	V
Current into any terminal	$\pm I_I$	max.	10	mA
Power dissipation (per output)	P_o	max.	50	mW
Power dissipation (per package)	P_{tot}	max.	200	mW
Operating ambient temperature	T_{amb}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

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CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1039P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	7	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	10	μA	10	25
		–	1	50	μA	7	65
operating; TRØ1 at V_{SS}; outputs unloaded; one keyboard switch closed	I_{DD}	–	–	1.7	mA	10	all
		–	0.8	–	mA	10	25
Inputs (note 1)							
TRØ2; TINH (note 2)							
input voltage HIGH	V_{IH}	$0.8V_{DD}$	–	V_{DD}	V	7 to 10	all
input voltage LOW	V_{IL}	0	–	$0.2V_{DD}$	V	7 to 10	all
input current	I_I	–	10^{-5}	1	μA	10	25
Outputs							
TRDT; TRØS; TRØ1							
output current HIGH at $V_{OH} = V_{DD} - 0.5$ V	$-I_{OH}$	0.4	–	–	mA	7	all
output current LOW at V_{OL} = 0.4 V	I_{OL}	0.4	–	–	mA	7	all
TRDT output leakage current when disabled $V_O = V_{SS}$ to V_{DD}	I_{OL}	–	–	1	μA	10	25
TINH							
output current LOW V_{OL} = 0.4 V	I_{OL}	0.4	–	–	mA	7	all
Oscillator							
maximum oscillator frequency	f_{osc}	120	–	–	kHz		
frequency variation with supply voltage, temperature and spread of IC properties at f_{nom} = 36 kHz (note 3)	Δf	–	–	$0.15f_{nom}$		7 to 10	all
oscillator current drain at f_{nom} = 36 kHz	I_{osc}	–	1.3	2.5	mA	10	25

Notes follow characteristics.

CHARACTERISTICS

T_{amb} = 0 to +85 °C (unless otherwise specified)

SAF1032P only

	symbol	min.	typ.	max.		V_{DD} V	T_{amb} °C
Recommended supply voltage	V_{DD}	8	–	10	V		
Supply current							
quiescent	I_{DD}	–	–	50	μA	10	25
		–	1	300	μA	10	85
operating; I_O = 0; at ØSCI frequency of 100 kHz	I_{DD}	–	–	1	mA	10	all
Inputs							
DATA; ØSCI; HØLD; TVØT (see note 4)							
input voltage HIGH	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V	8 to 10	all
input voltage LOW	V_{IL}	0	–	$0.2V_{DD}$	V	8 to 10	all
MAIN; tripping levels							
input voltage increasing	V_{ti}	$0.4V_{DD}$	–	$0.9V_{DD}$	V	5 to 10	all
input voltage decreasing	V_{td}	$0.1V_{DD}$	–	$0.6V_{DD}$	V	5 to 10	all
input current; all inputs except TVØT	I_I	–	10^{-5}	1	μA	10	25
input signal rise and fall times (10% and 90% V_{DD}) all inputs except MAIN	t_r, t_f	–	–	5	μs	8 to 10	all
Outputs							
programme selection: BINA/B/C/D							
auxiliary: SELA/B/C/D							
analogue: L3ØT; L2ØT; L1ØT TVØT (note 4)							
all open drain n-channel							
output current LOW at V_{OL} = 0.4 V	I_{OL}	1.6	–	–	mA	8	all
output leakage current at $V_O = V_{SS}$ to V_{DD}	I_{OL}	–	–	10	μA	10	all

For note 4 see next page.

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Notes to characteristics

1. The keyboard inputs (TRX.; TRY.; TRSL) are not voltage driven (see application information diagram Fig. 6).

   If one key is depressed, the circuit generates the corresponding code. The number of keys depressed at a time, and this being recognized by the circuit as an illegal operation, depends on the supply voltage (V_{DD}) and the leakage current (between device and printed-circuit board) externally applied to the keyboard inputs.

   If no leakage is assumed, the circuit recognizes an operation as illegal for any number of keys > 1 depressed at the same time with $V_{DD} = 7$ V. At a leakage due to a 1 MΩ resistor connected to each keyboard input and returned to either V_{DD} or V_{SS}, the circuit recognizes at least 2 keys depressed at a time with $V_{DD} = 7$ V.

   The highest permissible values of the contact series resistance of the keyboard switches is 500 Ω.

2. Inhibit output transistor disabled.

3. Δf is the width of the distribution curve at 2 σ points (σ = standard deviation).

4. Terminal TVØT is input for manual 'ON'. When applying a LOW level TVØT becomes an output carrying a LOW level.

APPLICATION INFORMATION

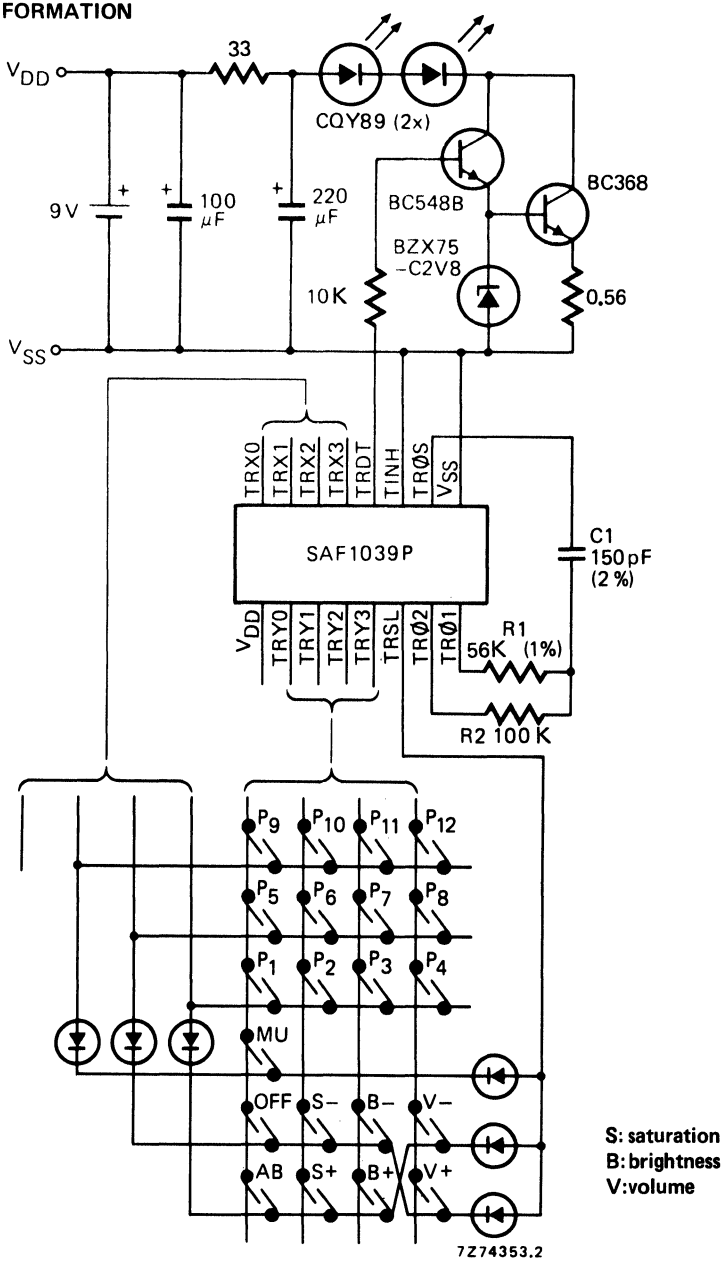


Fig. 6 Interconnection diagram of transmitter circuit SAF1039P in a remote control system, for a television receiver with 12 programmes.

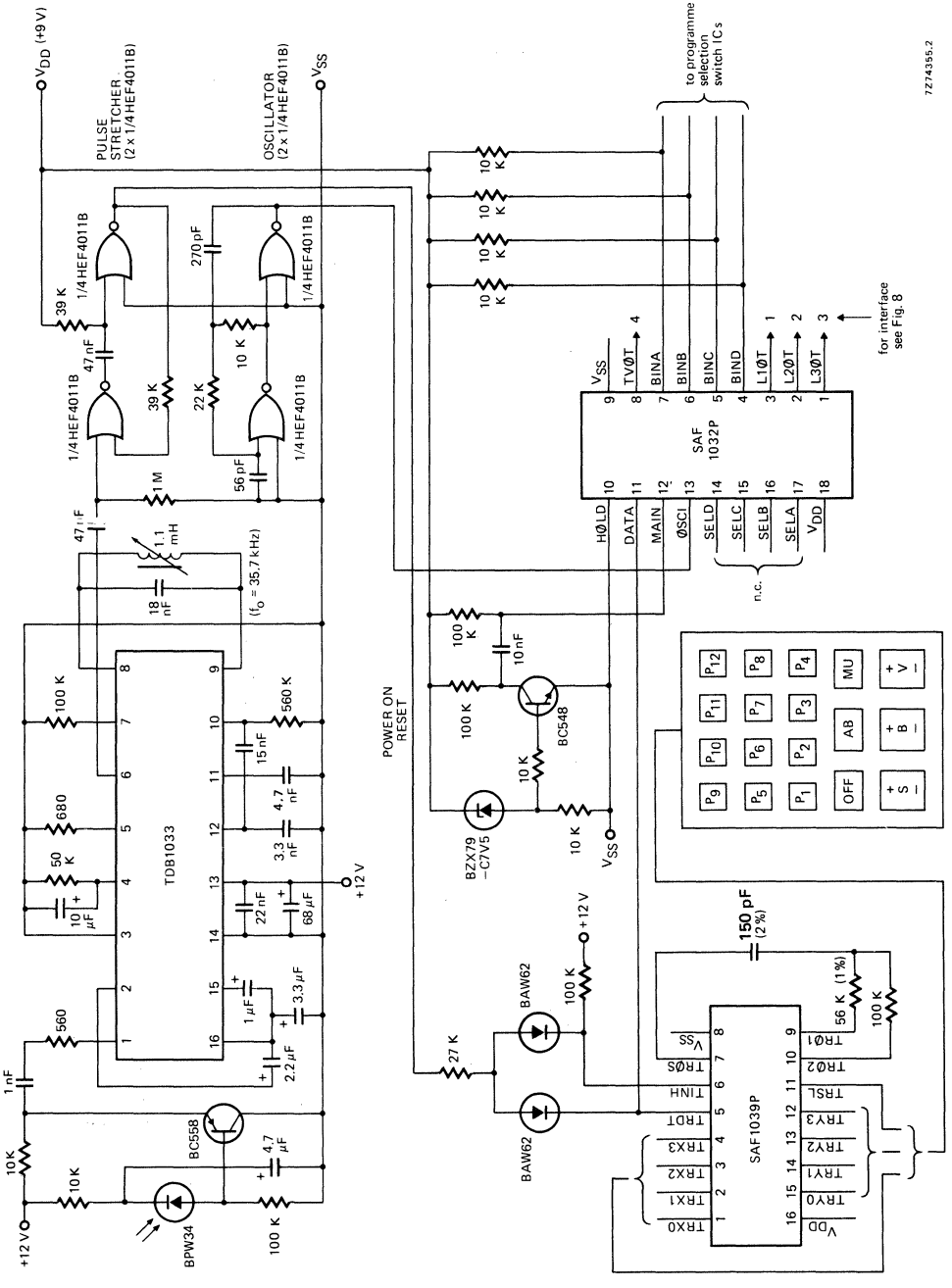


Fig. 7 Interconnection diagram showing the SAF1032P and SAF1039P used in a TV control system.

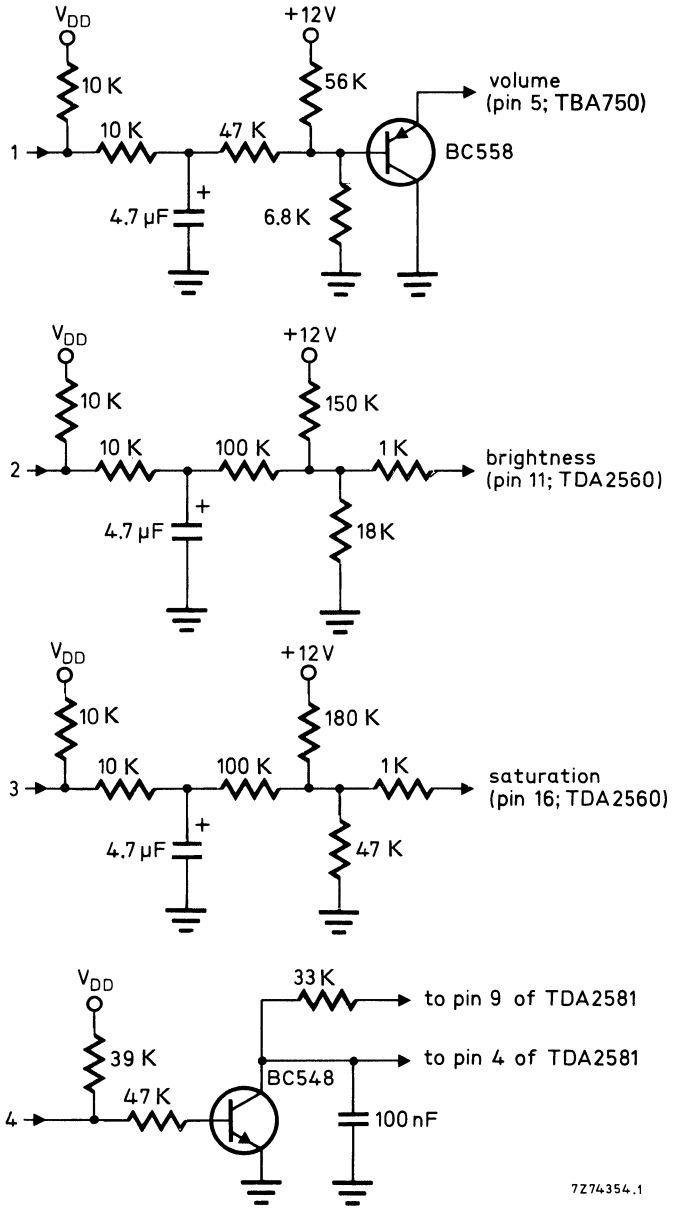


Fig. 8 Additional circuits from outputs L1ØT (1), L2ØT (2), L3ØT (3) and TVØT (4) of the SAF1032P in circuit of Fig. 7.

I/R Preamplifier — TDA3047

The TDA3047 is for infrared reception with low power consumption.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2.1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2\text{-}15(p\text{-}p)}$		0.02 to 200 mV
Output signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	4.5 V

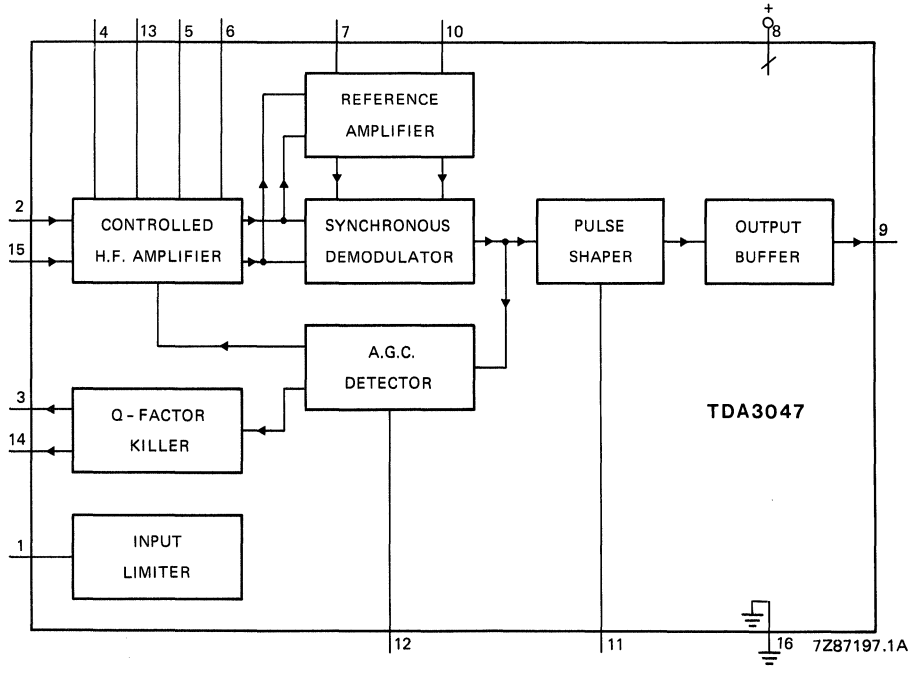


Fig. 1 Block diagram of TDA3047.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of > 75 μA with a voltage swing of 4.5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *high.*

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0.7 V. Limiting is 0.9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13.2 V
Output current pulse shaper (pin 11)	I_{11}	max.	10 mA
Voltages between pins*			
pins 2 and 15	V_{2-15}	max.	4.5 V
pins 4 and 13	V_{4-13}	max.	4.5 V
pins 5 and 6	V_{5-6}	max.	4.5 V
pins 7 and 10	V_{7-10}	max.	4.5 V
pins 9 and 11	V_{9-11}	max.	4.5 V
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 125 °C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4.65	5.0	5.35	V
Supply current	$I_P = I_8$	1.2	2.1	3.0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0.02	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0.5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range			see Fig. 2		
Inputs					
Input voltage (pin 2)	V_{2-16}	2.25	2.45	2.65	V
Input voltage (pin 15)	V_{15-16}	2.25	2.45	2.65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0.8	0.9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0.1	0.5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0.1	0.5	V
Output current; output voltage *high*					
at $V_{9-16} = 4.5$ V	$-I_9$	75	120	–	μA
at $V_{9-16} = 3.0$ V	$-I_9$	75	130	–	μA
at $V_{9-16} = 1.0$ V	$-I_9$	75	140	–	μA
Output current; output voltage *low* at $V_{9-16} = 0.5$ V	I_9	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3.1	4.7	6.2	kΩ

Notes

1. Voltage pin 9 is *high*; $-I_9 = 75$ μA.
2. Voltage pin 9 remains *low*.
3. Undistorted output pulse with 100% AM input.

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*)	V_{11-16}	3.75	3.9	4.05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*)	V_{11-16}	3.4	3.55	3.7	V
Hysteresis of trigger levels	ΔV_{11-16}	0.25	0.35	0.45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3.3	4.7	6.1	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at $V_{12-16} = 2$ V	$-I_3$	2.5	7.5	15	μA
Output current (pin 14) at $V_{12-16} = 2$ V	$-I_{14}$	2.5	7.5	15	μA

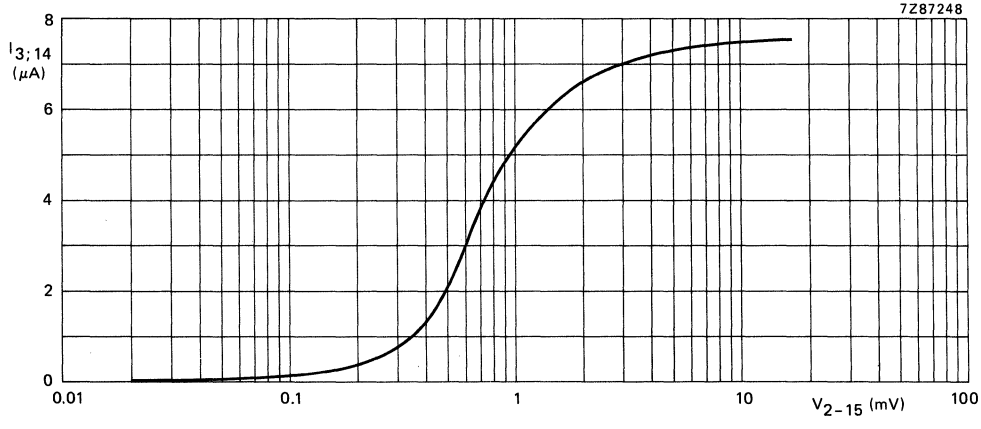
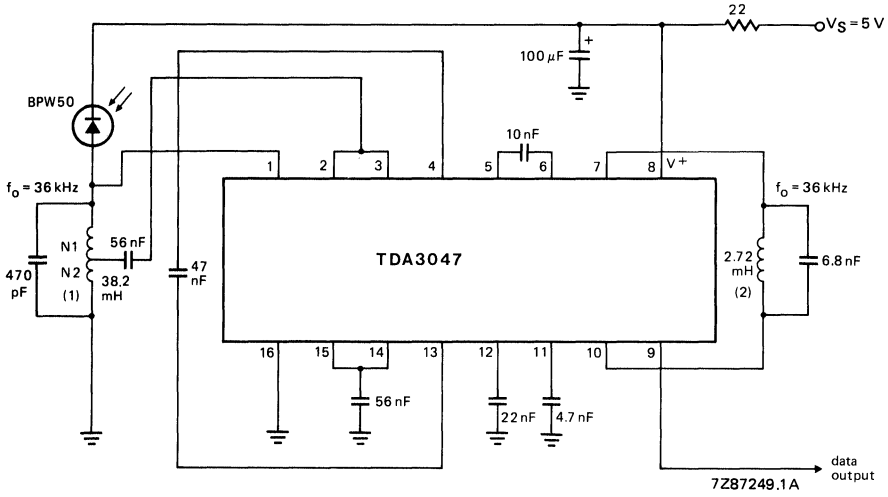


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; $V_P = 5$ V.



(1) N1 = 3.21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3047.

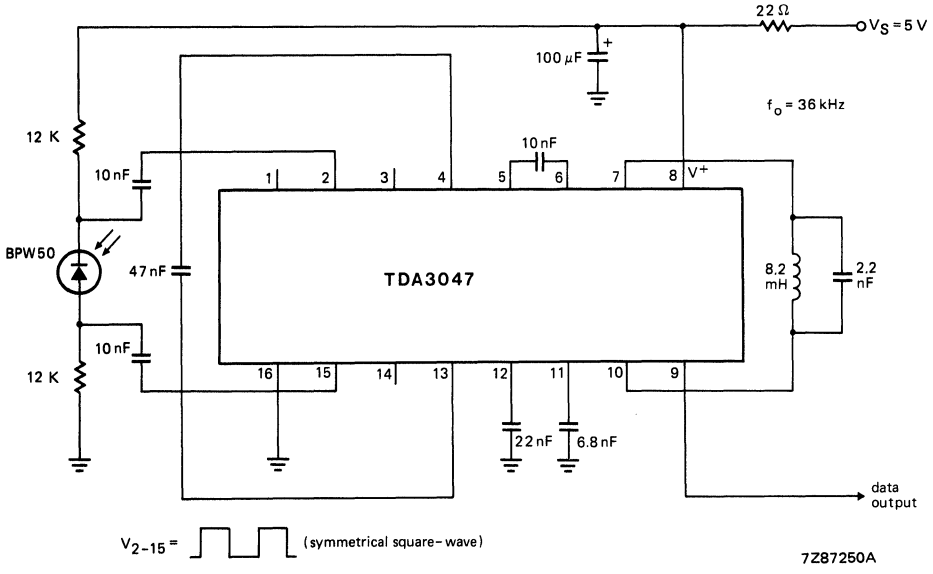


Fig. 4 Wide-band receiver with TDA3047.

For better sensitivity both 12 kΩ resistors may have a higher value.

5

I/R Preamplifier — TDA3048

The TDA3048 is for infrared reception with low power consumption.

Features

- H.F. amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

QUICK REFERENCE DATA

Supply voltage (pin 8)	$V_P = V_{8\text{-}16}$	typ.	5 V
Supply current (pin 8)	$I_P = I_8$	typ.	2.1 mA
Input signal (peak-to-peak value) (100% AM; f = 36 kHz)	$V_{2\text{-}15(p\text{-}p)}$		0,02 to 200 mV
Output signal (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$	typ.	4.5 V

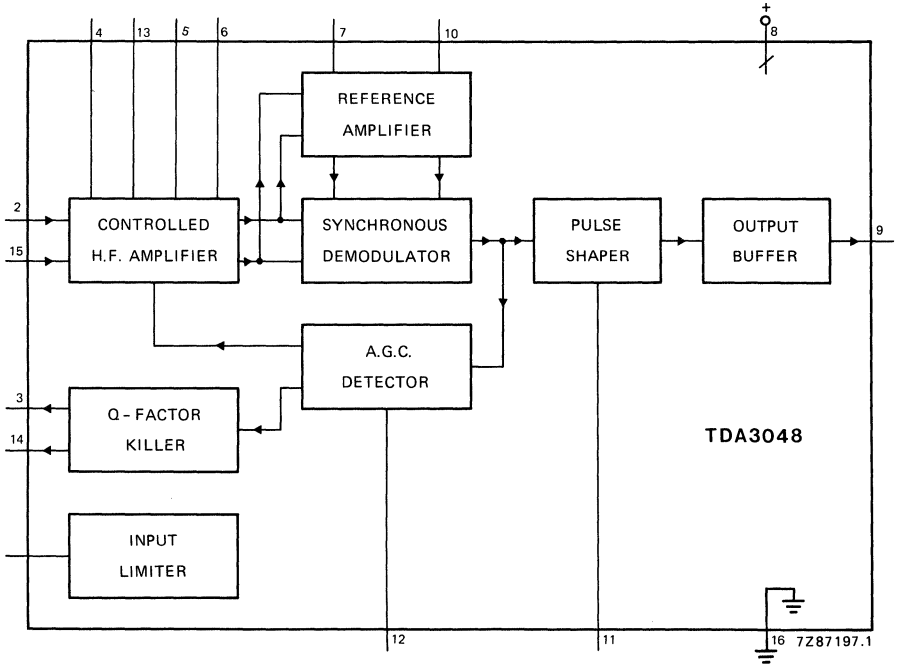


Fig. 1 Block diagram of TDA3048.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

FUNCTIONAL DESCRIPTION

General

The circuit operates from a 5 V supply and has a current consumption of 2 mA. The output is a current source which can drive or suppress a current of > 75 μA with a voltage swing of 4,5 V. The Q-killer circuit eliminates distortion of the output pulses due to the decay of the tuned input circuit at high input voltages. The input circuit is protected against signals of > 600 mV by an input limiter. The typical input is an AM signal at a frequency of 36 kHz. Figures 3 and 4 show the circuit diagrams for the application of narrow-band and wide-band receivers respectively. Circuit description of the eight sections shown in Fig. 1 are given below.

Controlled h.f. amplifier

The input signal is amplified by the gain-controlled amplifier. This circuit comprises three d.c. amplifier stages connected in cascade. The overall gain of the circuit is approximately 83 dB and the gain control range is in the order of 66 dB. Gain control is initially active in the second amplifier stage and is transferred to the first stage as limiting in the second stage occurs, thus maintaining optimum signal-to-noise ratio. Offset voltages in the d.c. coupled amplifier are minimized by two negative feedback loops; these also allow the circuit to have some series resistance of the decoupling capacitor. The output signal of the amplifier is applied to the reference amplifier and to the synchronous demodulator inputs.

Reference amplifier

The reference amplifier amplifies and limits the input signal. The voltage gain is approximately 0 dB. The output signal of this amplifier is applied to the synchronous demodulator.

Synchronous demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The demodulator output current is 25 μA peak-to-peak. The output signal of the demodulator is fed to the input of the a.g.c. detector and to the input of the pulse-shaper circuit.

A.G.C. detector

The a.g.c. detector comprises two n-p-n transistors operating as a differential pair. The top level of the output signal from the synchronous demodulator is detected by the a.g.c. circuit. Noise pulses are integrated by an internal capacitor. The output signal is amplified and applied to the first and second stages of the amplifier and to the Q-factor killer circuit.

Pulse-shaper

The pulse-shaper comprises two n-p-n transistors operating as a differential pair connected in parallel with the a.g.c. differential pair. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse-shaper is determined by the voltage of the capacitor connected to pin 11, which is applied directly to the output buffer.

Output buffer

The voltage of the pulse-shaper capacitor is fed to the base of the first transistor of a differential pair. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes. The output at pin 9 is active *low.*

Q-factor killer

Figure 3 shows the Q-factor killer in the narrow-band application. In this application it is necessary to decrease the Q-factor of the input selectivity particularly when large input signals occur at pins 2 and 15. In the narrow-band application the output of the Q-factor killer can be directly coupled to the input; pin 3 to pin 2 and pin 14 to pin 15.

Input limiter

In the narrow-band application high voltage peaks can occur on the input of the selectivity circuit. The input limiter limits these voltage peaks to approximately 0.7 V. Limiting is 0.9 V max. at I_1 = 3 mA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8-16}$	max.	13.2	V
Output current pulse shaper (pin 11)	I_{11}	max.	10	mA
Voltages between pins*				
pins 2 and 15	V_{2-15}	max.	4.5	V
pins 4 and 13	V_{4-13}	max.	4.5	V
pins 5 and 6	V_{5-6}	max.	4.5	V
pins 7 and 10	V_{7-10}	max.	4.5	V
pins 9 and 11	V_{9-11}	max.	4.5	V
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 125	°C

* All pins except pin 11 are short-circuit protected.

CHARACTERISTICS

$V_P = V_{8-16} = 5$ V; $T_{amb} = 25$ °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage	$V_P = V_{8-16}$	4.65	5.0	5.35	V
Supply current	$I_P = I_8$	1.2	2.1	3.0	mA
Controlled h.f. amplifier (pins 2 and 15)					
Minimum input signal (peak-to-peak value)					
at f = 36 kHz (note 1)	$V_{2-15(p-p)}$	–	15	25	μV
at f = 36 kHz (note 2)	$V_{2-15(p-p)}$	–	–	5	μV
A.G.C. control range (without Q-killing)		60	66	–	dB
Input signal for correct operation (peak-to-peak value; note 3)	$V_{2-15(p-p)}$	0.02	–	200	mV
Q-killing inactive ($I_3 = I_{14} < 0.5$ μA) (peak-to-peak value)	$V_{2-15(p-p)}$	–	–	140	μV
Q-killing active ($I_{14} = I_3$ = max.) (peak-to-peak value)	$V_{2-15(p-p)}$	28	–	–	mV
Q-killing range		see Fig. 2			
Inputs					
Input voltage (pin 2)	V_{2-16}	2.25	2.45	2.65	V
Input voltage (pin 15)	V_{15-16}	2.25	2.45	2.65	V
Input resistance (pin 2)	R_{2-15}	10	15	20	kΩ
Input capacitance (pin 2)	C_{2-15}	–	3	–	pF
Input limiting (pin 1) at I_1 = 3 mA	V_{1-16}	–	0.8	0.9	V
Outputs					
Output voltage *high* (pin 9) at $-I_9 = 75$ μA	$-V_{9-8}$	–	0.1	0.5	V
Output voltage *low* (pin 9) at $I_9 = 75$ μA	V_{9-16}	–	0.1	0.5	V
Output current; output voltage *low*					
$-V_{9-8} = 4.5$ V	I_9	75	120	–	μA
$-V_{9-8} = 3.0$ V	I_9	75	130	–	μA
$-V_{9-8} = 1.0$ V	I_9	75	140	–	μA
Output current; output voltage *high*					
$-V_{9-8} = 0.5$ V	$-I_9$	75	120	–	μA
Output resistance between pins 7 and 10	R_{7-10}	3.1	4.7	6.2	kΩ

Notes

1. Voltage pin 9 is *low*; $I_9 = 75$ μA.
2. Voltage pin 9 remains *high*.
3. Undistorted output pulse with 100% AM input.

5

parameter	symbol	min.	typ.	max.	unit
Pulse shaper (pin 11)					
Trigger level in positive direction (voltage pin 9 changes from *high* to *low*	V_{11-16}	3.75	3.9	4.05	V
Trigger level in negative direction (voltage pin 9 changes from *low* to *high*	V_{11-16}	3.4	3.55	3.7	V
Hysteresis of trigger levels	ΔV_{11-16}	0.25	0.35	0.45	V
A.G.C. detector (pin 12)					
A.G.C. capacitor charge current	$-I_{12}$	3.3	4.7	6.1	μA
A.G.C. capacitor discharge current	I_{12}	67	100	133	μA
Q-factor killer (pins 3 and 14)					
Output current (pin 3) at V_{12-16} = 2 V	$-I_3$	2.5	7.5	15	μA
Output current (pin 14) at V_{12-16} = 2 V	$-I_{14}$	2.5	7.5	15	μA

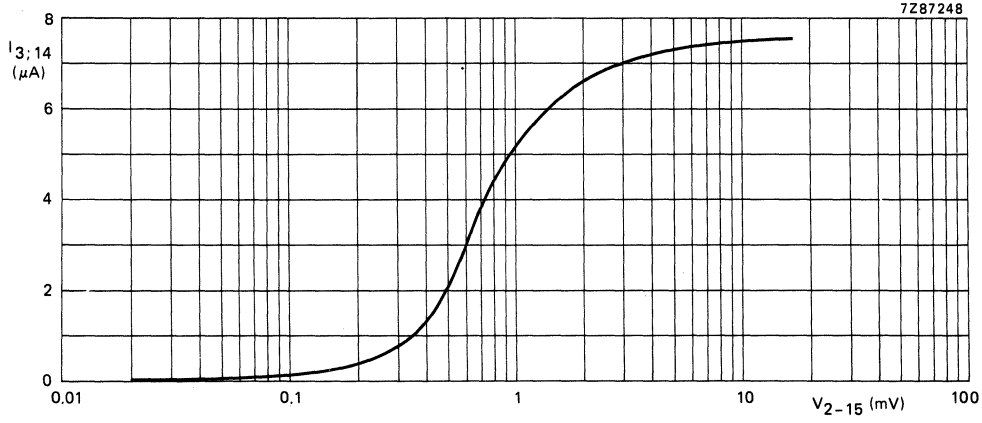
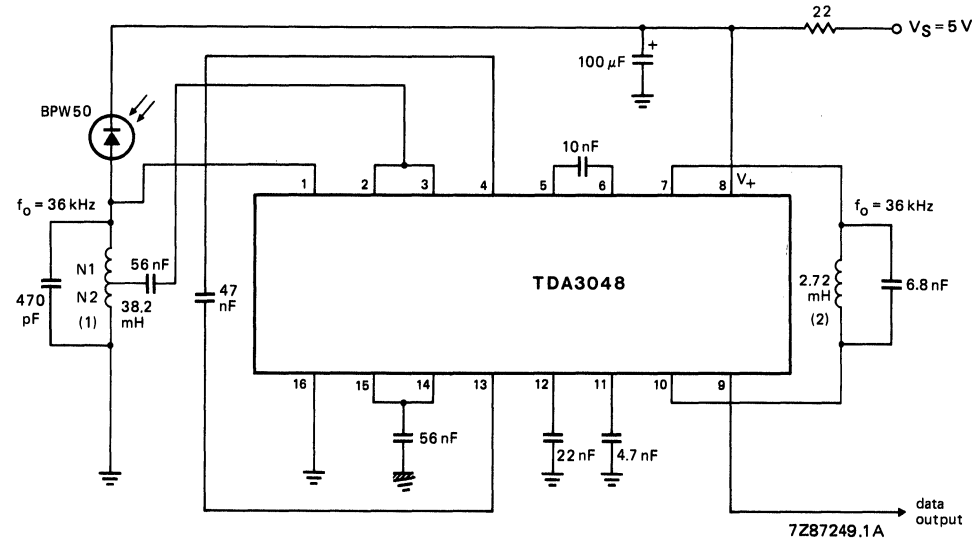


Fig. 2 Typical Q-factor killer current (pins 3 and 14) as a function of the peak-to-peak input voltage (V_{2-15}); $I_{3,14}$ is measured to ground, $V_{2-15(p-p)}$ is a symmetrical square wave. Measured in Fig. 4; V_P = 5 V.

APPLICATION INFORMATION



(1) N1 = 3.21
N2 = 1
Q = 16

(2) Q = 6

Fig. 3 Narrow-band receiver using TDA3048.

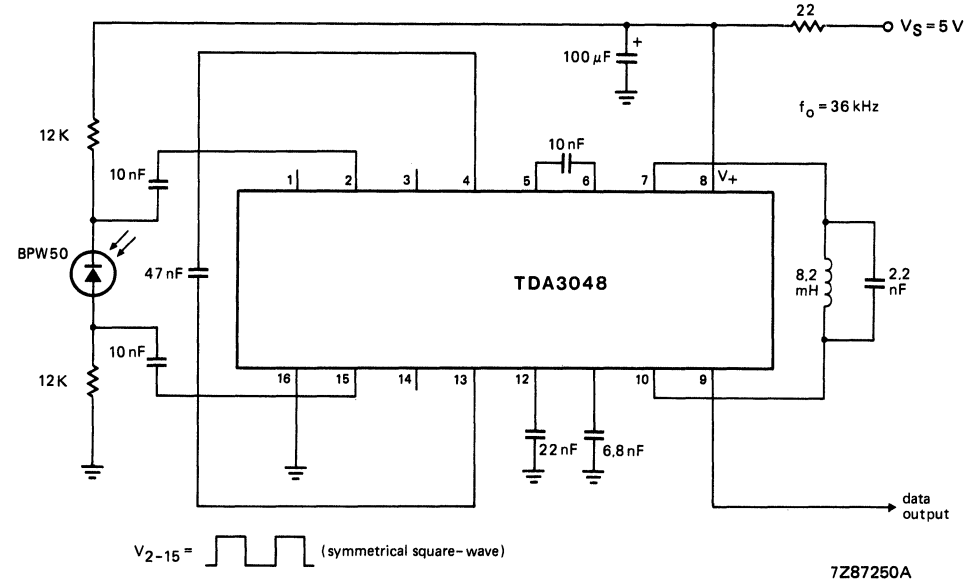


Fig. 4 Wide-band receiver with TDA3048.

For better sensitivity both 12 kΩ resistors may have a higher value.

Introduction

The I²C Concept

The Inter-IC bus (I^2C) is a 2-wire serial bus designed to provide the facilities of a local area network, not only between the circuits of one system, but also between different systems; e.g., teletext and tuning (see figures).

Philips/Signetics manufactures many devices with built-in I^2C interface capability, any of which can be connected in a system by simply "clipping" it to the I^2C bus. Hence, any collection of these devices around the I^2C bus is known as "clips."

The I^2C bus consists of two bidirectional lines, the Serial Data (SDA) line and the Serial Clock (SCL) line. The output stages of devices connected to the bus (these devices could be NMOS, CMOS, I^2C, TTL, ...) must have an open drain or open collector in order to perform the wired-AND function. Data on the I^2C bus can be transferred at a rate up to 100K bits/sec. The physical bus length is limited to 13 feet and the number of devices connected to the bus is solely dependent on the limiting bus capacitance of 400pF.

The inherent synchronization process, built into the I^2C bus structure, using the wired-AND technique does not only allow fast devices to communicate with slower ones, but also eliminates the "Carrier Sense Multiple Access/Collision Detect" (CSMA/CD) effect found in some local area networks, such as Ethernet.

Master-slave relationships exist on the I^2C bus; however, there is no central master. Therefore, a device addressed as a slave during one data transfer could possibly be the master for the next data transfer. Devices are also free to transmit or receive data during a transfer.

To summarize, the I^2C bus eliminates interfacing problems. Since any peripheral device can be added or taken away without affecting any other devices connected to the bus, the I^2C bus enables the system designer to build various configurations using the same basic architecture.

Application areas for the I^2C bus include:

Video Equipment

Audio Equipment

Home Appliances

Telephony

Automotive

Instrumentation

Industrial Control

Single-Chip 8-Bit Microcontroller — MAB84XX Family

DESCRIPTION

The MAB84XX family of microcontrollers is fabricated in NMOS. The instruction set is based on that of the 8048. The family consists of 8 devices:

- MAB/F 8400 – 128 RAM bytes, external program memory
- MAB/F 8401 – like 8400 but with 8-bit LED-driver (10mA), emulation of MAB/F 8422/42* possible
- MAB/F 8420 – 2K ROM/ 64 RAM bytes
- MAB/F 8440 – 4K ROM/128 RAM bytes
- MAB/F 8421 – 2K ROM/ 64 RAM bytes plus 8-bit LED-driver
- MAB/F 8441 – 4K ROM/128 RAM bytes plus 8-bit LED-driver
- MAB/F 8461 – 6K ROM/128 RAM bytes plus 8-bit LED-driver

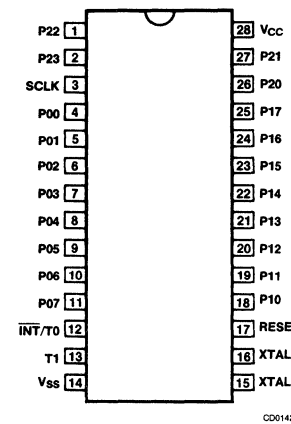
Each version has 20 quasi-bidirectional I/O port lines, one serial I/O line, one single-level vectored interrupt, an 8-bit timer event counter and on-board clock oscillator and clock circuits. Two 20-pin versions, MAB/F 8422 and MAB/F 8442 are also available.

This microcontroller family is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048. The microcontrollers have extensive bit handling abilities and facilities for both binary and BCD arithmetic.

FEATURES

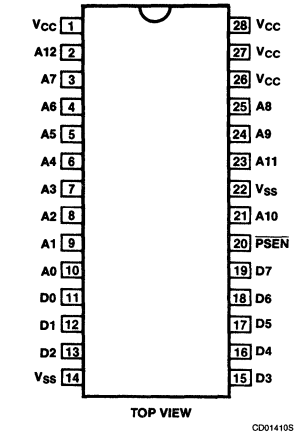
- **I^2C Compatible Serial I/O that can be used in single or multi-master systems (serial I/O data and clock via P23 and SCLK respectively)**
- **8-bit: CPU, ROM, RAM and I/O in a single 28-lead DIL package**
- **2K, 4K or 6K ROM bytes plus a ROM-less version**
- **64 or 128 RAM bytes**
- **20 quasi-bidirectional I/O port lines**
- **Two testable inputs: one of which can be used to detect zero cross-over; the other is also the external interrupt input**
- **Single level vectored interrupts: external, timer/event counter, serial I/O**
- **8-bit programmable timer/event counter**
- **Internal oscillator, generated with inductor, crystal, ceramic resonator or external source**
- **Over 80 instructions (based on SCN8048) all of 1 or 2 cycles**
- **Single 5V power supply (± 10%)**
- **Operating temperature range:**
  0 to +70°C MAB84XX family
  –40 to +85°C MAF84XX family
  –40 to +110°C MAF84AXX family

PIN CONFIGURATION



CD01420S

NOTE:
Pinning diagram for mask-programmable devices MAB8420, MAB8421, MAB8440, MAB8441, MAB8461 and for MAB8400 and MAB8401 'Piggy-back' version bottom pinning.



TOP VIEW

CD01410S

NOTE:
Pinning diagram for MAB8400/01B 'piggy-back' version top pinning to access a 2732 or 2764 EPROM. Access times for ROMS/EPROMS to be below 1 μs.

5

ORDERING CODE

See SCN8400 series in Microprocessor Data Manual

PIN DESCRIPTION for Bottom Pinning

DESCRIPTION	PIN NUMBER	FUNCTION
V_{SS}	14	**Ground**
V_{CC}	28	**Power supply,** +5V
P00 – P07	4 – 11	**Port 0,** 8-bit quasi-bidirectional I/O port
P10 – P17	18 – 25	**Port 1,** 8-bit quasi-bidirectional I/O port
P20 – P23	26, 27, 1, 2	**Port 2,** 4-bit quasi-bidirectional I/O port; P23 is the serial data I/O in serial I/O mode
SCLK	3	Bidirectional clock for serial I/O
$\overline{INT}$/TO	12	External interrupt input (sensitive to a negative-going edge min LOW> > 7 clock pulse, min HIGH < 4 clock pulses), testable using the JTO or JNTO instructions.
T1	13	Input pin, testable using the JT1 or JNT1 instructions. It can be designated as event counter input using the STRT CNT instruction. It can also be used to detect zero cross-over of slowly moving A.C. inputs.
RESET	17	Input to initialize the processor (active HIGH).
XTAL1	15	Connection to timing component (crystal) that determines the frequency of the internal oscillator. It is also the input for an external clock source.
XTAL2	16	Connection to other side of the timing component.

PIN DESCRIPTION for Top Pinning

DESCRIPTION	PIN NUMBER	FUNCTION
V_{SS}	14, 22	**Ground**
V_{CC}	1, 26 – 28	**Power supply,** +5V
A0 – A12	10 – 3, 25, 24, 21, 23, 2	Address outputs
D0 – D7	11 – 13, 15 – 19	Data inputs
$\overline{PSEN}$	20	Program store enable

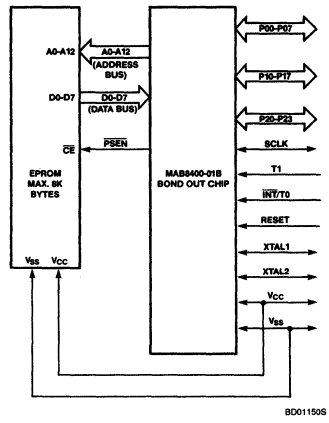
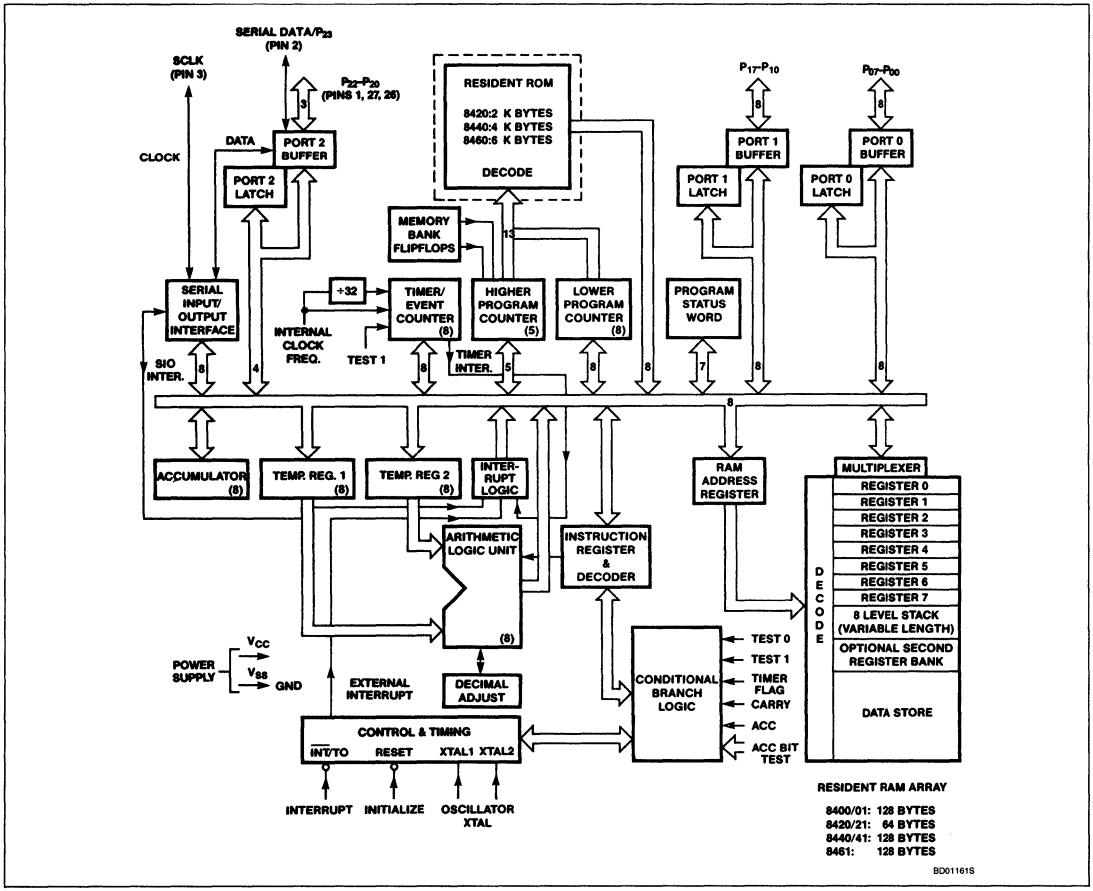


Figure 1. Connection of EPROM to 'Piggy-back' Package MAB8400/01B

BLOCK DIAGRAM



For additional information, consult the Applications Section and Signetics Microprocessor Data Manual

5

Speech Synthesizer MEA8000

DESCRIPTION

The MEA8000 is a 24-pin N MOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately in a Read-Only Memory. An efficient, easy-to-use speech editing and encoding system with EPROM programming capability, has been specially developed.

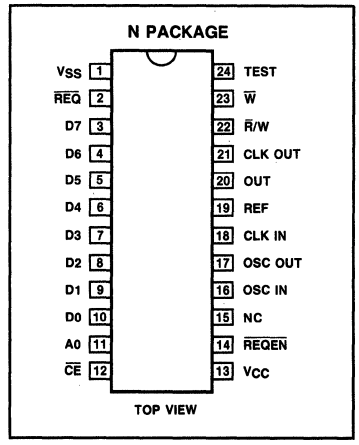
APPLICATIONS

- Telephony
- Automotive
- Computer response/prompt.
- Video games.
- General industrial.

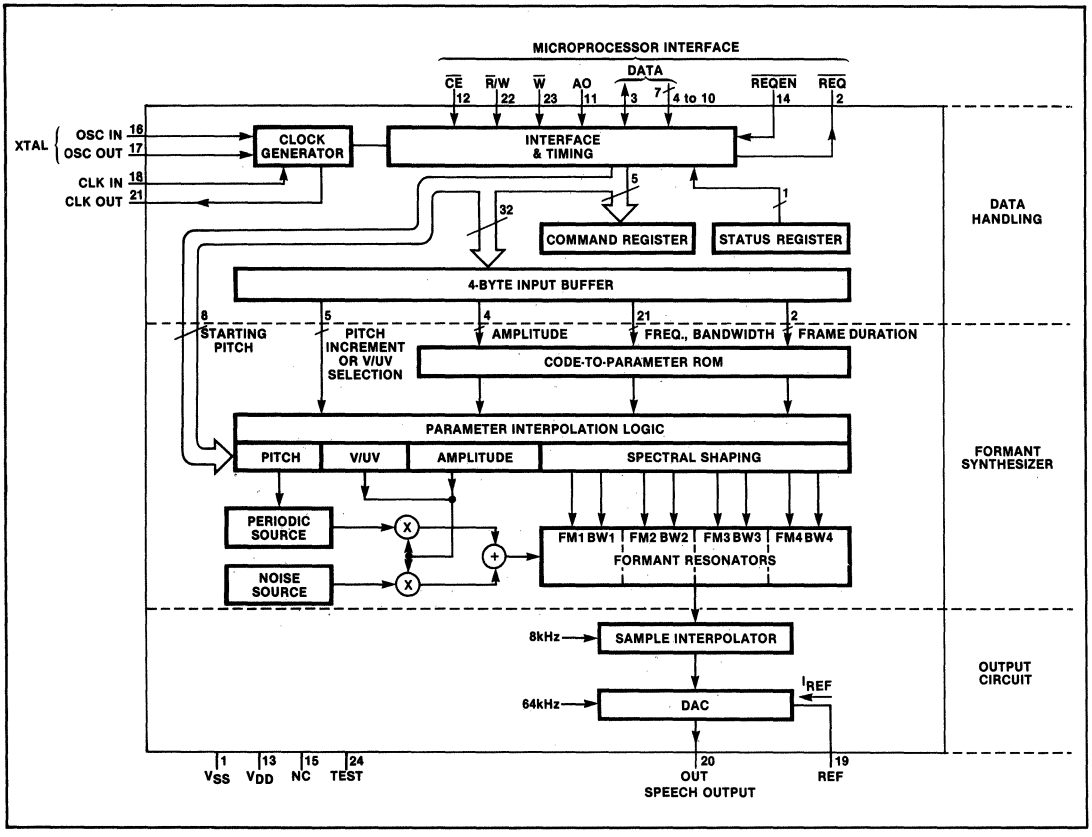
FEATURES

- **Microprocessor interface cability including an 8-bit data bus, an enable and a read/write input control signals.**
- **32-bit data buffer holding speech frame codes.**
- **Digital filter of 8th order with 3 programmable formant frequencies, one fixed formant frequency, and 4 programmable formant bandwidths. 4 KH bandwidth.**
- **Programmable amplitudes.**
- **Programmable duration of each frame: 8, 16, 32, or 64 milliseconds.**
- **Low data rate: average 1000 bits/sec.**
- **Operates from standard EPROMs/ROMs.**
- **Minimal external audio filter requirement.**
- **Crystal controlled oscillator or external (TTL) clock.**
- **Single +5V power supply.**

PIN CONFIGURATION

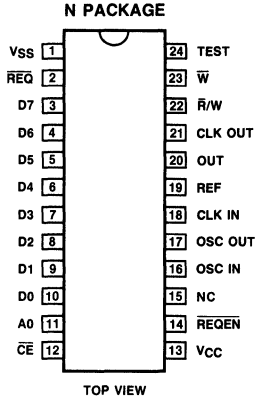


BLOCK DIAGRAM



Speech Synthesizer MEA8000

FUNCTIONAL PIN DESCRIPTION



PIN NO.	SYMBOL	NAME AND FUNCTION
		CONTROL
2	$\overline{REQ}$	**DATA REQUEST** output signal (open drain) which follows the inverse of the status REQ bit, but only if enabled by either the ROE bit in the command register or the external $\overline{REQEN}$ input pin.
3 to 10	D7 to D0	**Data bus** to which command or encoded speech parameters can be written. D7 is a bidirectional line through which the status bit can be read.
11	A0	**Data/control** input. Discriminates between speech code input buffer (A0 = '0') and command register (A0 = '1') during a 'write' operation.
12 22 23	$\overline{CE}$ R/$\overline{W}$ $\overline{W}$	**Chip enable, Read/Write, Write** These control signals provides an easy interface to most microprocessors or microcomputers (see timing diagrams).
14	$\overline{REQEN}$	**Request enable** input. $\overline{REQEN}$ = '0' enables the status REQ bit to appear inverted on the $\overline{REQ}$ output, independent of the command register.
		TIMING
16 17	OSC IN OSC OUT	Connections for internal clock oscillator. Nominal crystal frequency is 3.84 MHz. OSC IN must be tied to ground if CLK IN is used.
18 21	CLK IN CLK OUT	**Clock input** for external clock, TTL compatible, 3.84 MHz. Must be tied to ground when not used. A buffered output of the internal clock cycle (= CLK IN divided by 3).
		OUTPUT
19	REF	**Reference Current** Input pin for biasing the audio output level. This reference current can be derived from a resistor to the positive supply.
20	OUT	**Speech output.** This output is a 64 kHz pulse, modulated in both width and amplitude. It is configured as a current sink with a saturating voltage of about 3V.
		SUPPLY
1	V_{SS}	**Ground.**
13	V_{CC}	**Single supply voltage.** Nominally 5V, but battery operation is also possible.
15	NC	No connection.
24	TEST	Used for testing purposes. Changes other pin functions. Must be tied to ground for user operation.

5

ABSOLUTE MAXIMUM RATING

SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_I	Voltage on any pin with respect to V_{SS}	−0.5 to +7	V
$V_{\overline{REQ}}$, V_{OUT}	Output voltage on pins 2 and 20	15	V
T_{STG}	Storage temperature range	−20 to +125	°C
T_A	Operating ambient temperature range	0 to +70	°C

DC ELECTRICAL CHARACTERISTICS T_A = 25°C: V_{CC} = 5V, unless otherwise stated. All voltages referenced to V_{SS}

SYMBOL AND PARAMETER		TEST CONDITION	MEA8000			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage (note 1)		4.5	5.0	5.5	V
I_{CC}	Supply current	(No audio load)		30	50	mA
	D0 to D7, A0, $\overline{CE}$, $\overline{W}$, $\overline{R}$/W, $\overline{REQEN}$, CLK IN:					
V_{IH}	Input HIGH voltage		2.0		V_{CC}	V
V_{IL}	Input LOW voltage		−0.5		0.8	V
I_{IR}	Input Leakage current (note 2)				10	μA
C_I	Input Capacitance				7	pF
	D7 (I/O) , CLK OUT:					
V_{OH}	Output HIGH voltage	I_{OH} = −100 μA	2.4			V
V_{OL}	Output LOW voltage	I_{OL} = 1.6 mA			0.4	V
C_L	Output Load capacitance				50	pF
	$\overline{REQ}$:					
V_{OH}	Output HIGH voltage	Open drain			13.2	V
V_{OL}	Output LOW voltage	I_{OL} = 1.6 mA			0.4	V
C_L	Output Load capacitance				50	pF
	Audio output					
I_{REF}	Reference current (note 8) - Pin 19				0.3	mA
I_{OUT}	Output current (peak) - Pin 20					
		I_{REF} = 0 mA		100		μA
		I_{REF} = 0.1 mA		1.7		mA
		I_{REF} = 0.3 mA		5		mA
V_{OUT}	V_{OUT} (pin 20) for linear operation (note 3)	I_{REF} = 0.1 mA	2.5		13.2	V
	Oscillator					
f_{XTAL}	Crystal frequency	Internal		3.84	4.00	MHz
f_{CLK}	Clock frequency	External		3.84	4.00	MHz

NOTES
1. The circuit will continue to operate from a supply of up to 6.5V, but without necessarily meeting the specification.
2. This is also valid for V_{CC} = 0V.
3. This permits connection of the output load to a supply higher than that supplying the synthesizer.

AC ELECTRICAL CHARACTERISTICS (note 4) (Figure 4 and 5)

SYMBOL AND PARAMETER	TEST CONDITION	MEA8000			UNIT
		Min	Typ	Max	
t_{WR} Write enable pulse width.		200			ns
t_{AS} Address set-up time.		30			ns
t_{AH} Address hold time.		30			ns
t_{DS} Data set-up time for write operation.		150			ns
t_{DH} Data hold time for write operation.		30			ns
t_{RH} Request hold time (note 5)				350	ns
t_{RN} Request next (note 6)	Clock frequency = 3.84 MHz			3	μs
t_{RD} Read enable time.		200			ns
t_{DD} Data delay for read operation (note 7)				150	ns
t_{DF} Data floating for read operation (note 7)				150	ns
t_{RV} Request valid before a write operation.		0			ns
t_{ROE} Request output enable response.				750	ns
t_{CS} Control set-up time.				20	ns
t_{CH} Control hold time.				20	ns

NOTES

4. Timing reference level is 1.5V.
5. An external pull up resistor is required, as this is an open drain output. The time (t_{RH}) to reach 2.0V is specified at a load to 5V of 3.3 kΩ and 50 pF.
6. Between two data write operations of one speech frame.
7. Levels greater than 2.0V for a '1' or less than 0.8V for a '0' are reached with a load of one TTL input and 50 pF.
8. Typical voltage level at the REF pin is 2.5V.

5

Speech Synthesizer MEA8000

PRINCIPLE OF OPERATION

The MEA8000 voice synthesizer implements the vocal tract modeling technique of voice synthesis (also known as formant synthesis). This technique results in producing good quality speech with the lowest possible bit rates; this will in turn mean small memory size requirements.

Figure 1 shows an electronic model of the human vocal tract. A mixture of a periodic signal, representing the pitch of the original speech, and an aperiodic signal, representing the unvoiced sound in the speech, is fed via an amplifier stage to a variable filter comprising of four resonators. The amplifier controls the amplitude of the synthesized sound while the resonators model the sound in accordance with the formants in the original speech. Each resonator is controlled by two parameters, one for the resonant frequency and one for the bandwidth. The information required to control such a synthesizer system is defined by the pitch frequency, the amplitude values, the voiced/unvoiced source selection and the resonator settings. By periodic updating of this control information one can obtain a good replica of the original speech.

Operation

The MEA8000 generates speech output by suitable filtering of a relatively low frequency sawtooth waveform for voiced sounds or for random noise for unvoiced sounds.

Speech encoded parameters, controlling the on-chip periodic source and digital filter, are transmitted on the 8-bit data bus from external memory to the MEA8000 under the control of an external microprocessor or microcomputer.

At first, a byte containing the starting pitch code must be transmitted to the MEA8000. This byte goes directly to the pitch generating circuitry via the input interface logic. Subsequent pitch frequencies are then specified using the pitch increment parameter; this method of encoding pitch contributes to the low bit rate requirements.

After receiving the starting pitch code, the codes of each speech frame (32 bits), when received, are shifted into a four-byte input buffer before being translated into control parameters by the code-to-parameter ROM (See Block Diagram). The parameter interpolation logic calculates the difference, and interpolates linearly between consecutive parameters to smooth the parameter transients. The interpolation interval is decoded using the two Frame Duration (FD) bits in each speech frame. Because the FD bits specify a frame duration of 8, 16, 32 or 64ms, the resulting average bit rate is about 1000 bits/sec.

Since the on-chip output sampling rate is 64KHz, the need for an external analog output filter is greatly reduced.

Modes of Operation

1. STOP mode: characterized by a silent output and the status REQ bit set to '1'. This mode is entered from power up or by STOP command. The mode is entered automatically if at the end of an active speech frame the next four parameter bytes are not yet received while the CONT bit in the command register is a '0'. In the latter case the final speech frame will be repeated once but with a decaying amplitude and the same pitch.

2. ACTIVE mode: a speech sample is being produced.

3. CONTINUOUS mode: entered if an active speech frame is finished and new data is not supplied in time while the CONT bit in the command register is a '1'. The synthesizer will repeat the last speech frame indefinitely until all four new data bytes are received, a STOP command has been issued or the CONT command bit has been reset.

Control Signals

With the three control signals $\overline{CE}$, $\overline{W}$ and $\overline{R}/W$, provided on 3 external pins, the MEA8000 voice synthesizer chip is made compatible with most popular microprocessors and microcomputers. Please refer to the timing diagrams for timing requirements.

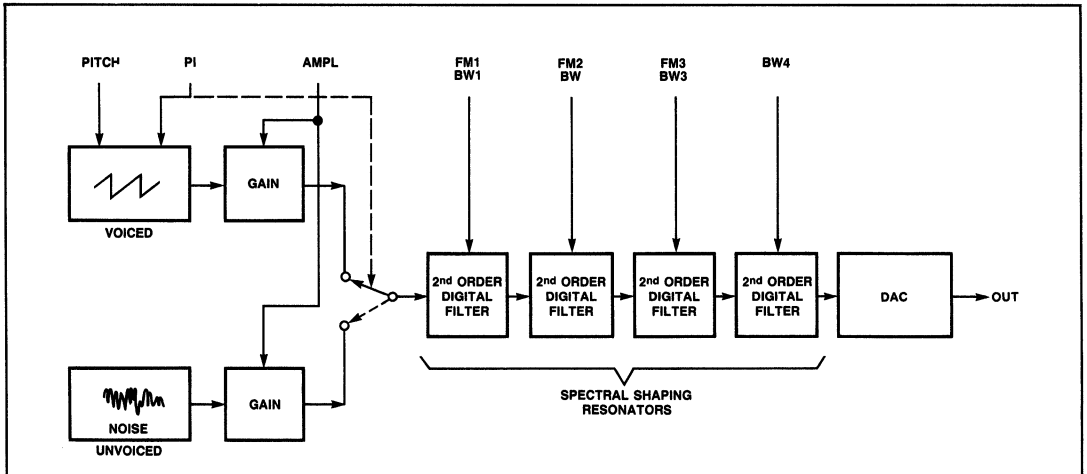


Figure 1. Electronic Model of Human Vocal Tract.

Addressing the MEA8000

The MEA8000 voice synthesizer chip is addressed as a peripheral device to the host microprocessor or microcomputer. The three control signals, $\overline{CE}$, $\overline{W}$, and $\overline{R}/W$ along with the A0 address input, allow the MEA8000 to be addressed as an I/O device or as a memory device in a memory-mapped I/O system.

The input buffer and the command register are write-only while the status register is a read-only, as depicted in the following table:

$\overline{CE}$	$\overline{W}$	$\overline{R}/W$	A0	OPERATION
0	0	1	0	Write Data
0	0	1	1	Write Command Register
0	X	0	X	Read Status Register
0	1	1	X	Three-State Data Bus
1	X	X	X	Three-State Data Bus

Status Register

The MEA8000 status register consists of a single bit: REQ. The status REQ bit appears on bit 7 of the data bus, D7, when reading the status register. The $\overline{REQ}$ output carries the inverse polarity of the status REQ bit. When the status REQ bit is a "0", the MEA8000 is busy and cannot accept any write data. The MEA8000 requests more data by setting its status REQ bit to a "1"; in this case the $\overline{REQ}$ output pin is active "0" only if this output is enabled. The $\overline{REQ}$ output is enabled either by hardware by connecting $\overline{REQEN}$ pin to ground, or by software by setting the ROE bit in the command register to a "1" while holding $\overline{REQEN}$ pin high. The MEA8000 voice synthesizer chip can then be used in an interrupt driven environment or in a polled type structure.

Speech Code Input Buffer

The MEA8000 has a 32-bit (4-byte) input buffer. This buffer holds the speech encoded parameters for one speech frame.

Starting from the STOP mode — see Modes of Operation — the first data byte received by the MEA8000 will be interpreted as a starting value for the pitch. Every four successive data bytes received thereafter are treated as a group of speech code. The coded speech frame format is shown in Figure 2.

Writing a data byte into the MEA8000 will, automatically, clear the status REQ bit to "0". Within a group of 4 bytes (i.e. one speech frame), the $\overline{REQ}$ output (if enabled) will be activated within 3µs, measured from the trailing edge of $\overline{CE}$ or $\overline{W}$ (depending on which is used as the write strobe — see Timing), indicating a request for the next byte within the same group. Note that this time is extended to a multiple of 8ms (8, 16, 32 or 64) after writing the fourth, or last, byte of a group. This allows the host microprocessor enough time to use polling, instead of interrupts, since the minimium time of a speech frame is 8ms.

When in the STOP mode, the MEA8000 voice synthesizer will commence producing sound after receipt of 5 bytes (Figure 2).

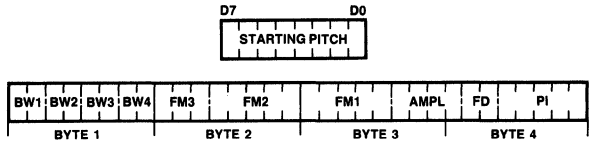


Figure 2. Format of Coded Speech Frame

SYMBOL AND PARAMETER		BITS
Starting Pitch	Initial value for pitch	8
FD	Speech frame duration	2
PI	Pitch increment (rate of pitch change) or noise selection	5
AMPL	Amplitude	4
FM1	Frequency of 1st formant	5
FM2	Frequency of 2nd formant	5
FM3	Frequency of 3rd formant	3
FM4	Frequency of 4th formant (fixed at 3500 Hz)	0
BW1	Bandwidth is 1st formant	2
BW2	Bandwidth of 2nd formant	2
BW3	Bandwidth of 3rd formant	2
BW4	Bandwidth of 4th formant	2

Command Register

The MEA8000 has a 5-bit command register. A command word is written into the command register by performaing a write operation with A0 input being set to "1".

The following explains the various command bits in the command register:

STOP results in an immediate reset of the synthesizer to the STOP mode. The ROE and CONT are not affected by this command.

CONT Continuous mode. This bit can be set or cleared only if the corresponding CONT enable bit is programmed as a '1'. In the continuous mode the synthesizer will not revert to the STOP mode if all four parameters are not received before the end of the current speech frame, but will repeat it indefinitely.

If CONT = '0', the last frame will be repeated once with decaying amplitude and the same pitch before the stop mode is entered.

ROE Request Output Enable. This bit can be set or cleared only if the corresponding ROE enable bit is a '1'. ROE determines whether the request in the status bit appears on the REQ pin. Note: the same can be achieved by connecting the REQEN pin (request enable) to a '0'.

After power on, the command register bits CONT and ROE will both be zero. Thus power on equals the command 00011010 = 1 A (hexadecimal).

D7	D6	D5	D4	D3	D2	D1	D0
			STOP	CONT enable	CONT	ROE enable	ROE
Not used			'0' = No action '1' = Stop	00 = No action 01 = No action 10 = Slow stop 11 = Continue		00 = No action 01 = No action 10 = Disable $\overline{REQ}$ output 11 = Enable $\overline{REQ}$ output	

ROM Mapping

The external ROM that stores the speech codes of an utterance or a word (called a speech file) also stores the starting pitch byte and the file header. The header comprises three bytes, two that indicate the number of bytes in the file and one that allows additional data to be encoded for each file.

Usually, more than one speech file will be stored in a ROM. An index is made by listing the 2-byte starting addresses of each file at the beginning of the ROM. The end of the index is indicated by the bytes FF FF. Figure 3 shows examples of ROM mapping.

Power Supply

During (slow) power-up or power-down, the MEA8000 voice synthesizer will not produce any spurious sound. When powering-up the device, the MEA8000 will be in the STOP mode with command bits ROE and CONT being set to "0".

Speech Editing and Encoding System

A specially designed speech editing and encoding system, targeted for use with the MEA80000, has been developed. The system consists of a Speech Adapter Box (SAB), a customized software package, and a general purpose personal computer.

The system is capable of programming the PROM's with the most efficient speech parameters. These parameters, when read by the MEA8000 voice synthesizer chip, will produce the best quality speech possible that this chip is capable of delivering.

Timing Diagrams

Read and write timing diagrams are depicted in Figures 4, 5, and 6. Note that for a read operation, either $\overline{CE}$ or R/$\overline{W}$ can be used as the read strobe whereas for a write operation, either $\overline{CE}$ or $\overline{W}$ can be used as the write strobe. This allows great flexibility in system design.

Figure 7 shows the timing sequence encountered when writing speech code data into the MEA8000. In the figure, data is written on the rising edge of $\overline{CE}$. Starting in the STOP mode, the first byte to be written is the starting pitch. This is followed by 4 consecutive bytes, representing the first speech frame to be written into the MEA8000. Note that within the same frame, $\overline{REQ}$ output pin (if enabled) is activated within 3µs indicating, to the host microprocessor, its readiness to accept the next byte. After receiving the fourth byte of a speech frame, the $\overline{REQ}$ output pin will not be activated until the frame duration period (specified by the two FD bits) has elapsed. This time is equivalent to 8, 16, 32 or 64ms.

System Configurations

Figure 8 shows a minimal system configuration for a voice application system using a general purpose microprocessor or a single chip microcomputer. In the latter case, speech code parameters are stored in the on-chip microcomputer ROM.

Figure 9 depicts a speech synthesis system using the SCN8051, 8-bit single chip microcomputer. Separate external program memory and speech parameters memory is shown, using 64K ROM chips. Note that external buffers might be needed on P0 (0-7) depending on loading conditions.

Figure 10 shows a typical audio output stage configuration using the TDA1011 audio power amplifier chip while Figure 11 depicts an audio output stage for 8 ohm speaker using discrete components.

The oscillator/clock configurations are depicted in Figure 12.

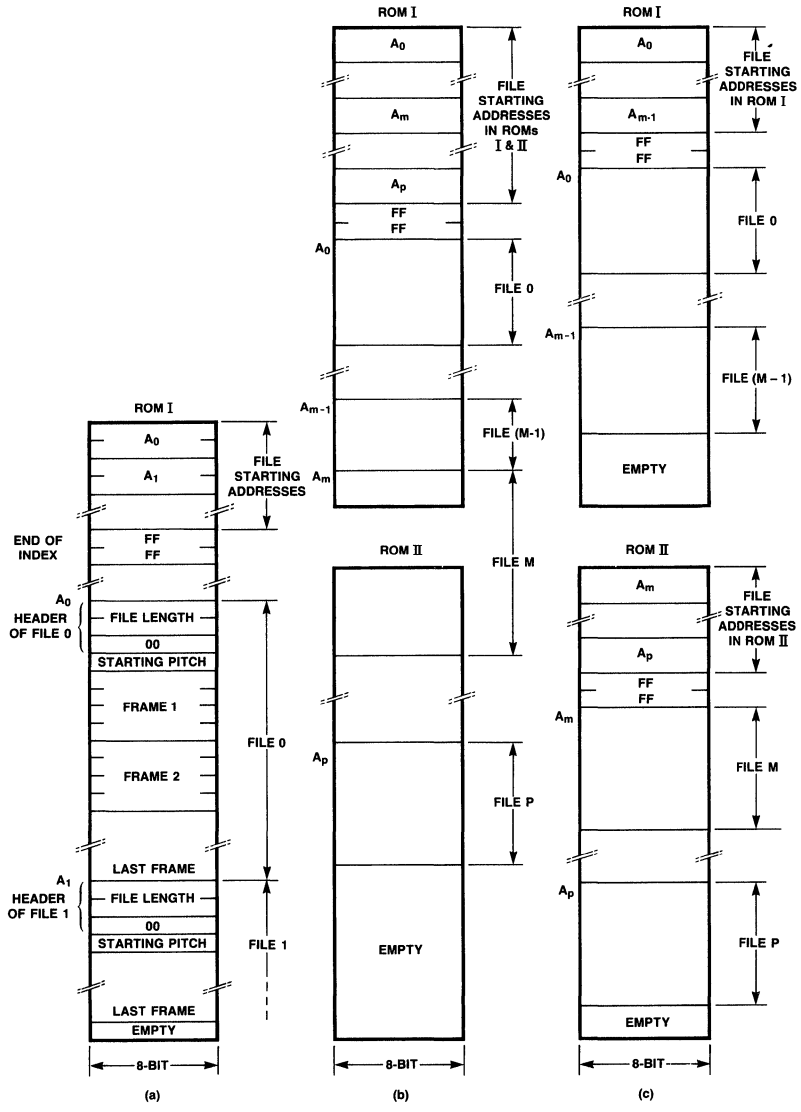


Figure 3. Examples of ROM Memory Mapping; (a) Vocabulary in One ROM, (b) and (c) Vocabulary in Two ROMs.

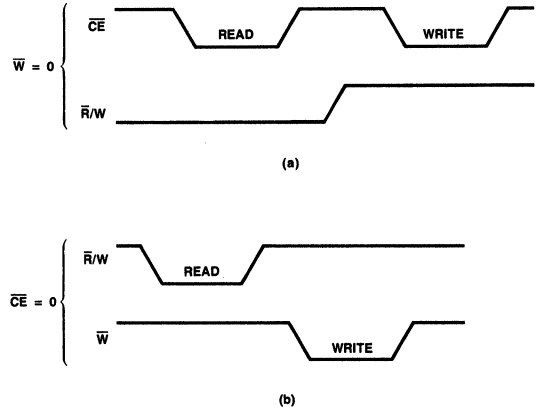


Figure 4. (a) Chip Enable (CE) Used as a Read or Write Strobe; (b) Separate Read and Write Strobes.

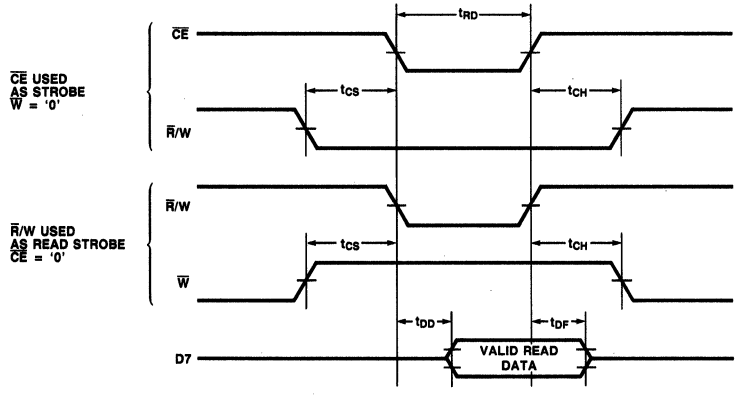


Figure 5. Read Timing

NOTES
Address input A0 is a don't care. Data bits D0 to D6 remain floating.

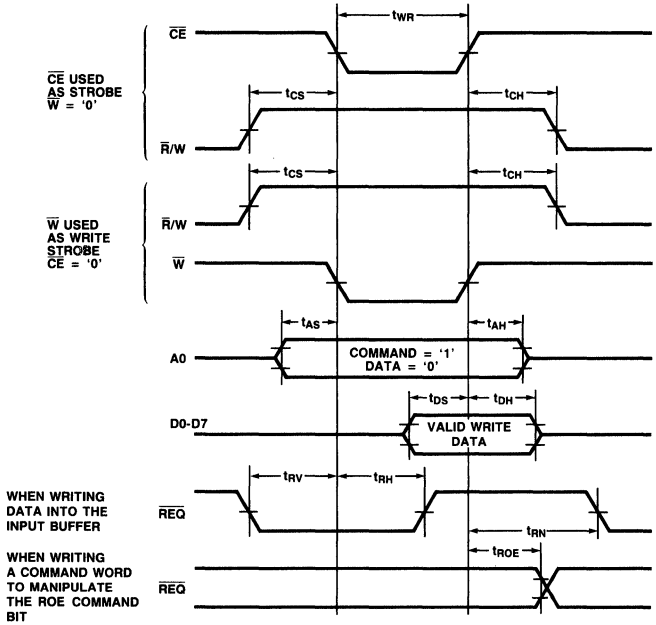


Figure 6. Write Timing

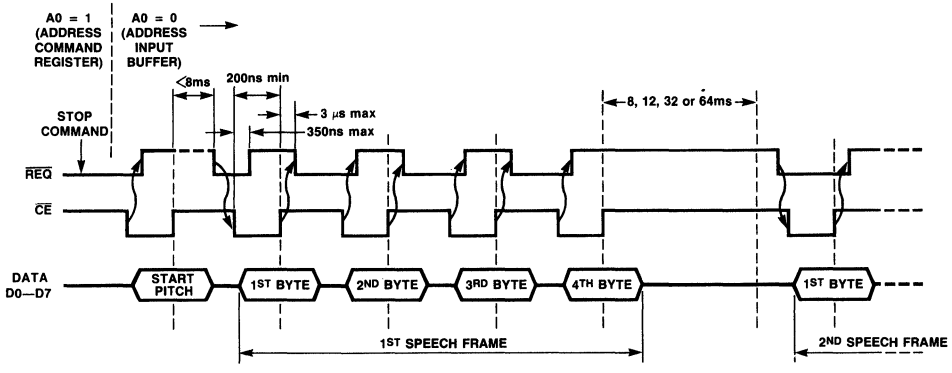
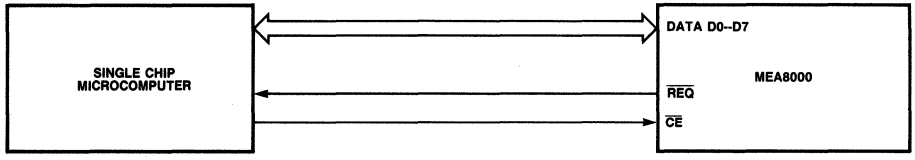
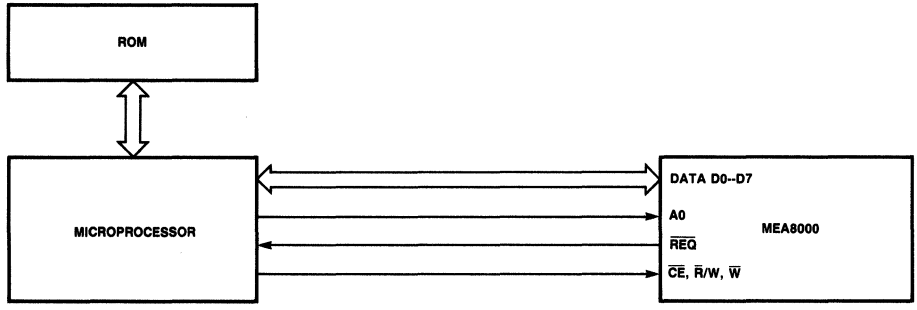


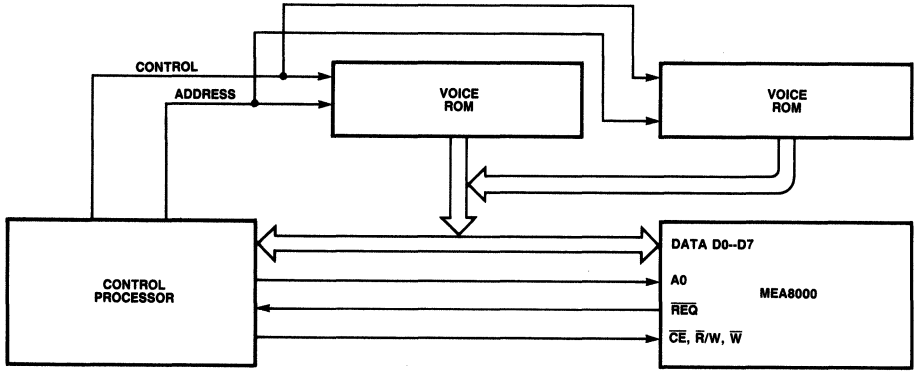
Figure 7. Speech Code Data Write Timing Sequence



a. Minimal System: Single Chip Microcomputer With On-chip Voice ROM.



b. MEA8000 as a Microprocessor Peripheral



c. Applications Using Separate Voice ROMs.

Figure 8. Typical Application Configurations.

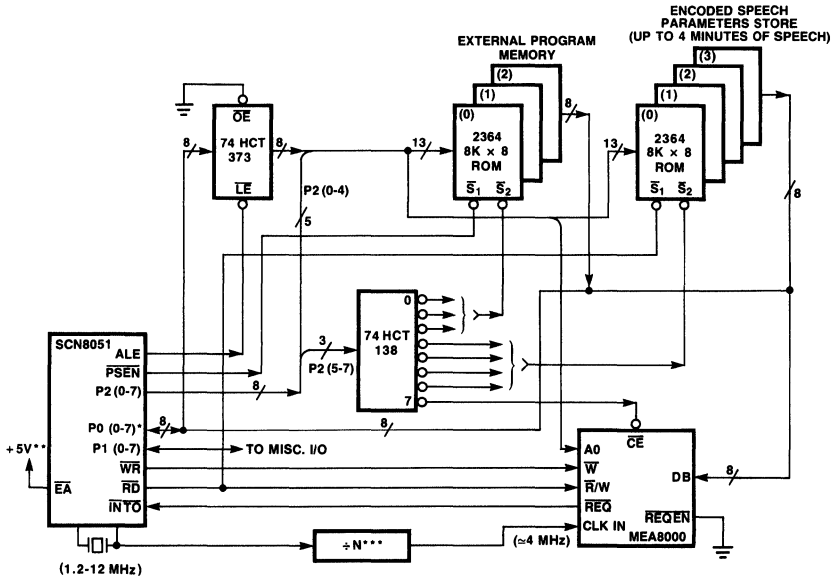


Figure 9. Speech Synthesis System Using the 8051 8-Bit Microcomputer

*External buffers might be needed.

**Connect EA to ground for the ROM less version (SCN 8031).

*** ÷ N is a single F/F when XTAL frequency is around 8 MHz

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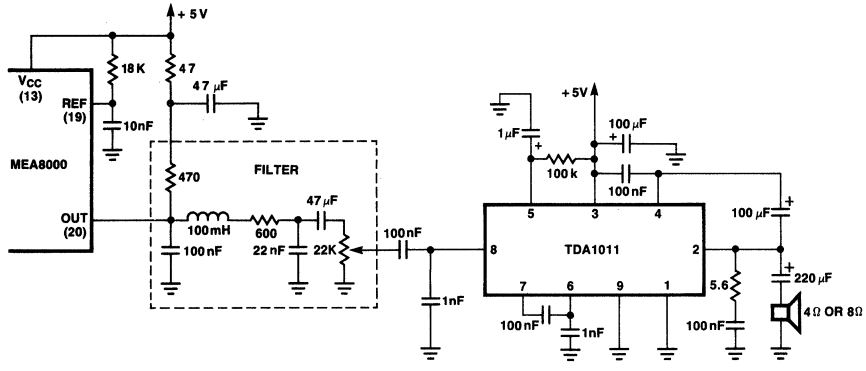


Figure 10. Audio Output Stage—Typical Configuration

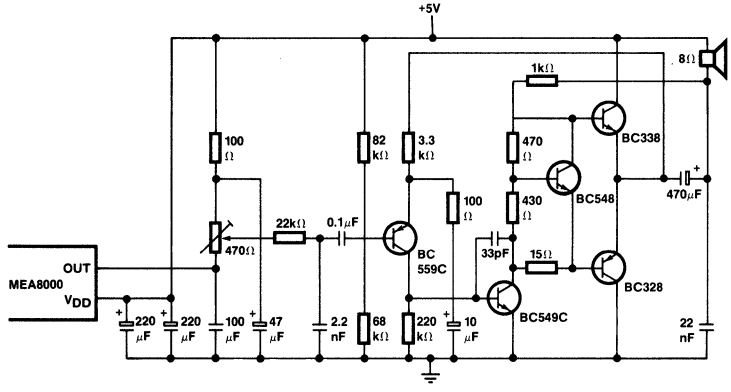


Figure 11. Audio Output Stage Using Discrete Components (8Ω Speaker)

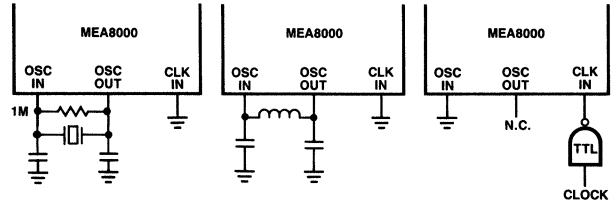


Figure 12. Oscillator/Clock Configurations

Speech Evaluation Board/Demonstrator OM8000/8001

DESCRIPTION

The OM8001 is an MEA8000-based speech demonstration box. It contains all the necessary circuitry and software to reproduce over 100 seconds of speech. The OM8001 may be used for evaluation purposes.

FEATURES

- **Based on the MEA8000 speech synthesizer**
- **Complete stand-alone speech system**
- **Built-in amplifier and loudspeaker**
- **Output selection via thumbwheel switches**
- **Automatic power-down mode**
- **Easily exchangeable speech EPROMS**

5

Speech Encoding System OM8010/8011

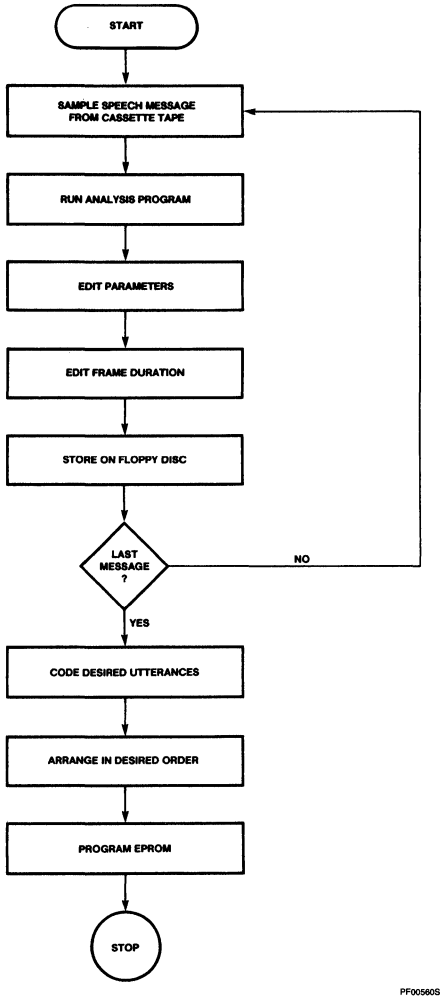
DESCRIPTION

The OM8010/8011 are stand-alone speech editing and encoding systems for creating synthetic digitized speech for use with the MEA8000 speech synthesizer. Both systems are based on popular personal computers: the OM8010 on the Hewlett Packard 9816S, and the OM8011 on the IBM PC. Along with the Speech Adaptor Box, these systems allow users to quickly create their own speech vocabulary.

The system functions include instant access to original, synthesized, edited and unedited speech. This creates a user-friendly environment where all phases of editing can be accessed and compared with each other. In addition, the system allows for independent editing of each speech parameter, a high-resolution graphical display of all speech parameters, and a wheel-controlled cursor (HP system) allowing for frame-by-frame sounding of each speech sample. An on-board PROM programmer makes the OM8010/8011 a complete stand-alone system for creating unlimited speech vocabulary.

FEATURES

- **IBM PC or HP 9816S compatible**
- **Sampling of analog speech signals**
- **Marking of begin and end of utterance**
- **Formants/pitch analysis program**
- **Graphical parameter representation**
- **Parameter editing capability: formants, pitch, voiced/unvoiced, amplitude, frame duration**
- **Conversion of parameters to synthesizer codes**
- **EPROM programmer on-board**
- **Parameter and code storage on floppy disc**



Speech Coding Process Flowchart

CMOS Male/Female Speech Synthesizer PCF8200

GENERAL DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.
Applications include automotive, telephony, personal computers, annunciators, aids for the handicapped, and general industrial devices.

Features

- Male and female speech with good quality
- Speech-band from 0 to 5 kHz
- Bit-rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range –40 to + 85 °C
- Single 5 V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8 bit parallel bus or I^2C bus
- Software readable status word (parallel bus or I^2C bus)
- BUSY-signal and REQN-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	–	5	–	V
Supply current	I_{DD}	–	10	t.b.f.	mA
Supply current (stand-by)	$I_{DD(SB)}$	–	200	–	μA
Inputs					
Input voltage	V_{IH}	2,0	–	V_{DD}	V
Input voltage	V_{IL}	0	–	0,8	V
Input capacitance	C_I	–	7	–	pF
Outputs (D5 to D7)					
Output voltage high	V_{OH}	3,5	–	V_{DD}	V
Output voltage low	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Operating ambient temperature range	T_{amb}	–40	–	+ 85	°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

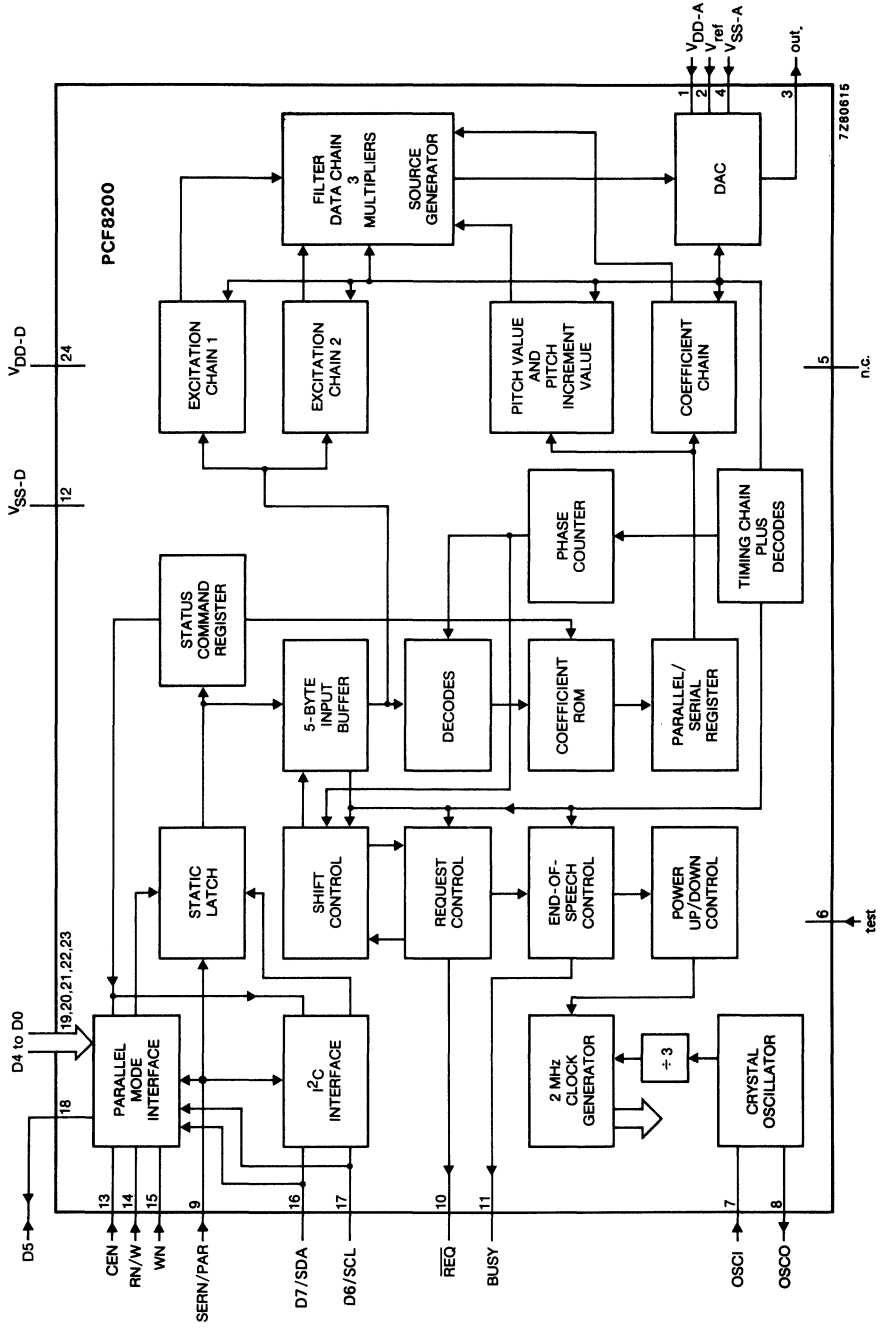


Fig. 1 Block diagram.

PINNING

1	V_{DD-A}	supply
2	V_{REF}	supply
3	OUT	output
4	V_{SS-A}	supply
5	NC	not connected
6	TEST	input
7	OSCI	input
8	OSCO	output
9	SERN/PAR	input
10	REQN	output
11	BUSY	output
12	V_{SS-D}	supply
13	CEN	input
14	RN/W	input
15	WN	input
16	SDA/D7	input/output
17	SCL/D6	input/output
18	D5	input/output
19	D4	input
20	D3	input
21	D2	input
22	D1	input
23	D0	input
24	V_{DD-D}	supply

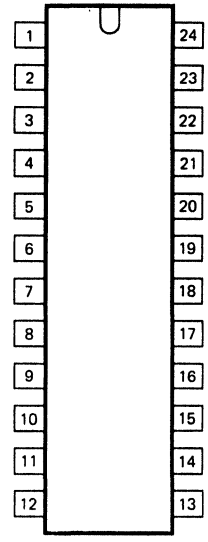


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage*	V_{DD}	min.	−0,3	max.	7,5 V
Input voltage*	V_I	min.	−0,3	max.	7,5 V
Output voltage*	V_O	min.	−0,3	max.	7,5 V
Operating ambient temperature range	T_{amb}				−40 to + 85 °C
Storage temperature range	T_{stg}				−55 to + 125 °C

* Any pin with respect to V_{SS}.

FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

OPERATION

Speech characteristics change quite slowly, therefore the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8,8 , 10,4, 12,8 or 17,6 milliseconds with the speed-option, speaking speed, in the command-register.
The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard-frame duration.

Table 1. Frame duration as a function of speed-option (FS1, FS0) and frame-duration (FD1, FD0).

FD1, FD0	10	01	00	11	FS1, FS0
00	8,8	10,4	12,8	17,6	ms
01	17,6	20,8	25,6	35,2	ms
10	26,4	31,2	38,4	52,8	ms
11	44,0	52,0	64,0	88,0	ms

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation.
A block diagram of the formant synthesizer is shown in Fig. 3.

The filter output is upsampled to 80 kHz and filtered with a digital low-pass filter. Before the signal is digital to analogue converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

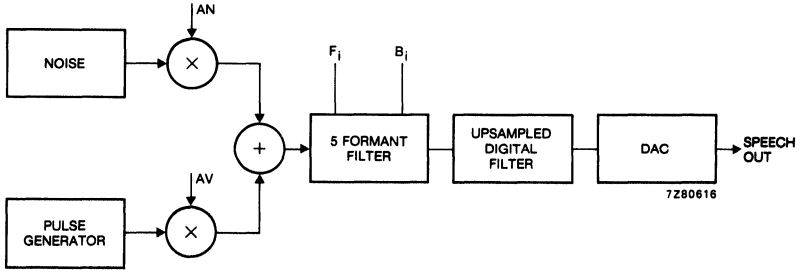


Fig. 3 Block diagram of formant synthesizer.

DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

DAC-amplitude factor

The DAC-amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or V_{DD} on. Table 2 indicates the amplitude factor.

Table 2 DAC amplitude factor.

byte	factor	dB
01110000	3,5	10,88
10110000	3,25	10,24
00110000	3,0	9,54
11010000	2,75	8,97
01010000	2,5	7,96
10010000	2,25	7,04
00010000	2,0	6,02
11100000	1,75	4,86
01100000	1,5	3,52
10100000	1,25	1,94
00100000	1,0	0,00
11000000	0,75	−2,50
01000000	0,5	−6,02
10000000	0,25	−12,04
00000000	0,0	
11110000	HEX code F0 and is not allowed as a DAC amplitude	

Start pitch

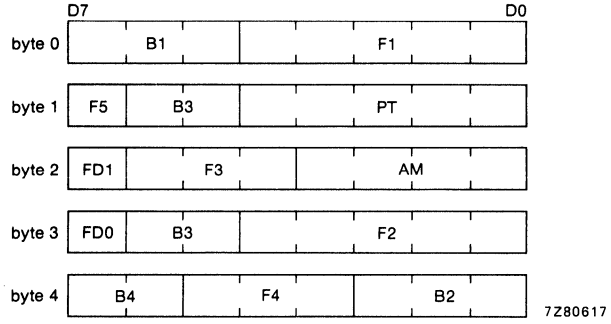
The second byte after a STOP or BADSTOP, or V_{DD} on is the start pitch. It is a one byte start value for the on-chip pitch-period generator.

Frame Data

The frame data is a five byte block which contains the filter and source information:

pitch increment/decrement value	5 bits
amplitude	4 bits
frame duration	2 bits
frequency of 1st formant	5 bits
frequency of 2nd formant	5 bits
frequency of 3rd formant	3 bits
frequency of 4th formant	3 bits
frequency of 5th formant	1 bit
bandwidth of 1st formant	3 bits
bandwidth of 2nd formant	3 bits
bandwidth of 3rd formant	2 bits
bandwidth of 4th formant	2 bits
bandwidth of 5th formant	2 bits
	40 bits = 5 bytes

The frame-data bits are organized as shown in Fig. 4.



It is not allowed to set byte 0 to the hexadecimal value E0.

Fig. 4 Format of frame-date.

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CONTROL FORMAT

Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Fig. 5.

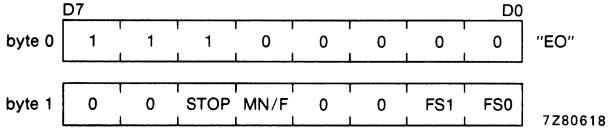

Fig. 5 Control write: first byte fixed, second byte control.

FS0, FS1 speed option

FS1	FS0	speech speed	standard-frame duration
0	0	100%	12,8 ms
0	1	123%	10,4 ms
1	0	145%	8,8 ms
1	1	73%	17,6 ms

MN/F, male/female option

MN/F = 0 male quantization table
= 1 female quantization table

STOP

STOP = 1 stop; repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP:

1. REQN = 1 STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

Status Read

Three status bits can be read out at any time without a preceding byte (E0).
This is shown in Fig. 6.

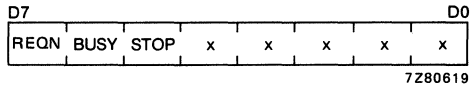

Fig. 6 Status read.

REQN	= 1	No data required
	= 0	Synthesizer requesting for new data
BUSY	= 1	Busy (an utterance is pronounced)
	= 0	Idle, REQN will set to 1; the synthesizer is in STOP or BADSTOP mode
STOP		The STOP bit is the same as the stop bit written to the synthesizer during a command write. STOP = 1, BUSY = 0 stopped by the user. STOP = 0, BUSY = 0 BADSTOP because the data was not sent in time.

After initial power-up the status/command register is set to the following status:

FS0, FS1	= 0	Standard-frame duration of 12,8 ms
MN/F	= 0	Male quantization table
STOP	= 1	
BUSY	= 0	Idle
REQN	= 1	No data required

INTERFACE PROTOCOL

Data can be written to the synthesizer when REQN = 0 or, when REQN = 1 and BUSY = 0. Figure 7 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor. In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up.

The I^2C transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs the byte must be provided within the duration of a half standard frame. If the byte is not provided in time a BADSTOP will be generated.

During each data write operation, the status bit REQN will be set to '1'.
Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

I^2C ADDRESS

On chip there is a I^2C slave receiver/transmitter with the address:

7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	R/W

POWER UP

The synthesizer will be set to power-up on a parallel-write sequence.

PAR-mode: The input-latches are active so they can receive the first byte

SER-mode: The I^2C transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer a parallel write sequence (Fig. 9) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, CEN, while WN = 0 and RN/W = 1.
The synthesizer can be set to permanent power-up by hard-wired control pins (CEN = 0, RN/W = 1, WN = 0).

POWER DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down. In the power-down mode the status/command register will be retained.
In power-down mode the clock-oscillator is switched off. After initial V_{DD} the synthesizer is in power-down mode.

SERN/PAR

SERN/PAR is hard-wired to V_{DD} or V_{SS}.

HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

CHARACTERISTICS

T_{amb} = −45 to + 85 °C; supply voltage (V_{DD} to V_{SS}) = 4,5 V to 5,5 V with respect to V_{SS}, otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	t.b.f.	V
Supply current	I_{DD}	–	10	–	mA
Standby current	$I_{DD(SB)}$	–	200	–	μA
Inputs					
CEN, RN/W, WN, OSCI					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
PARALLEL MODE					
Input Characteristics (D0 to D7)					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output Characteristics (D5 to D7 only)					
Output voltage HIGH (I_{OH} = −100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
SERIAL MODE					
Input Characteristics (SDA and SDL)					
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	10	pF
Output Characteristics (SDA only, open drain)					
Output voltage LOW (I_{OL} = 3 mA)	V_{OL}	0	–	0,4	V

parameter	symbol	min.	typ.	max.	unit
OSCILLATOR					
Crystal frequency	f_{XTAL}	t.b.f.	6	t.b.f.	MHz
V_{REF}					
Reference voltage	V_{REF}	1,9	–	$\frac{V_{DD}-1,5}{1,25}$	V
Input leakage current	I_{IR}	–	t.b.f.		
Outputs					
REQN, BUSY					
Output voltage HIGH (I_{OH} = 100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{QL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
OUT					
Output voltage	V_{OUT}	0,66 x V_{REF}		1,34 x V_{REF}	V
Minimum external load		600	–	–	Ω
Timing characteristics (note 1) (Figs 8 and 9)					
Write enable	t_{WR}	200	–	–	ns
Data set-up for write	t_{DS}	150	–	–	ns
Data hold for write	t_{DH}	30	–	–	ns
Read enable	t_{RD}	200	–	–	ns
Data delay for read (note 2)	t_{DD}	–	–	150	ns
Data floating for read (note 2)	t_{DF}	–	–	150	ns
Control set-up	t_{CS}	0	–	–	ns
Control hold	t_{CH}	0	–	–	ns
REQ new (new byte of the same speech frame)	t_{RN}	–	t.b.f. (≈ 3)		us
REQ Valid	t_{RV}	0	–	–	ns
REQ Hold	t_{RH}	–	250	t.b.f.	ns

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NOTES TO THE CHARACTERISTICS

1. Timing reference level is 1,5 V; supply 5 V ± 10%; temperature range of –40 °C to 85 °C.
2. Levels greater than 2 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
3. Rise and fall times between 0,6 V and 2,2 V levels.

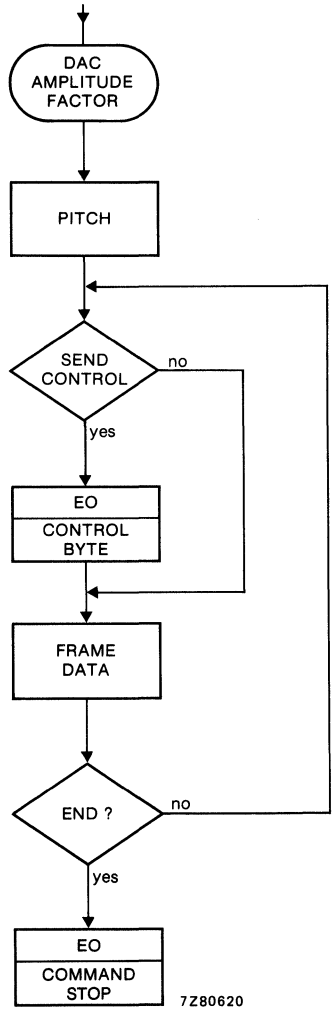
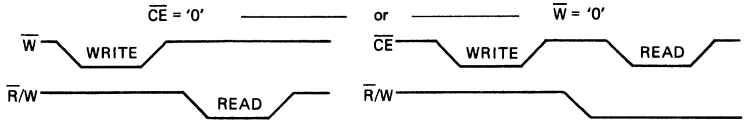


Fig. 7 Interface protocol.

Timing diagrams

The control signals CE, R/W and W have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the R/W and W inputs can be used as the RD and WR strobe inputs.



Typical connection of control signals.

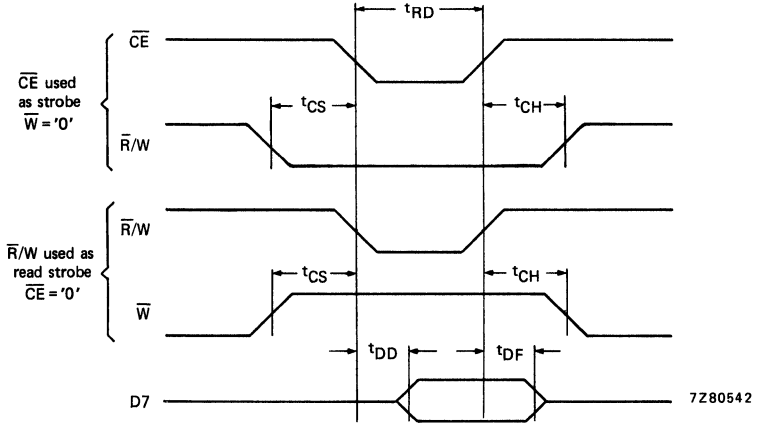


Fig. 8 Read timing.

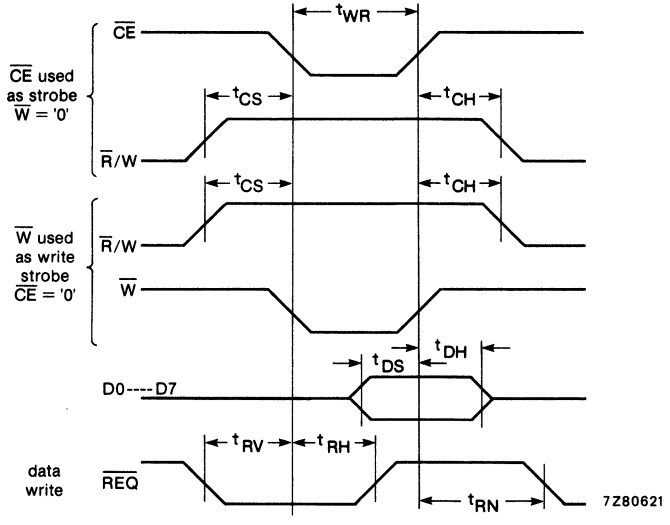


Fig. 9 Write timing.

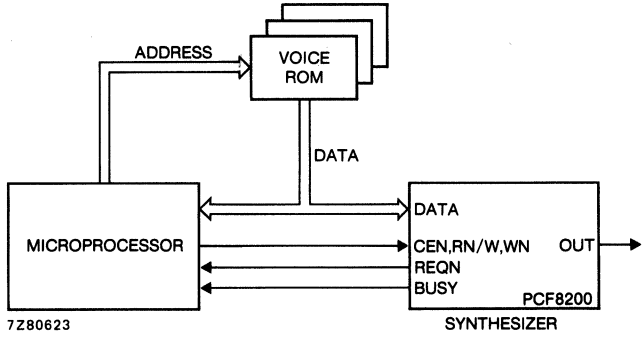


Fig. 10 Typical application configuration with parallel interface.

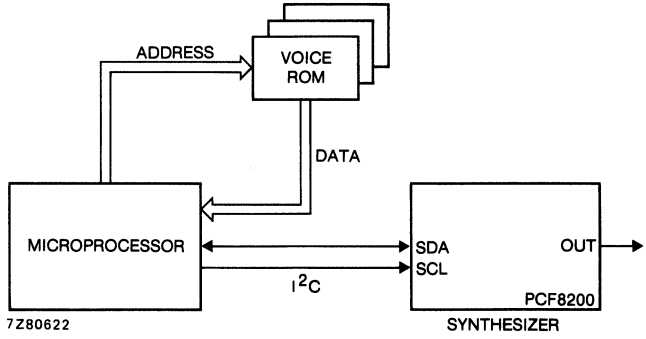


Fig. 11 Typical application configuration with series interface.

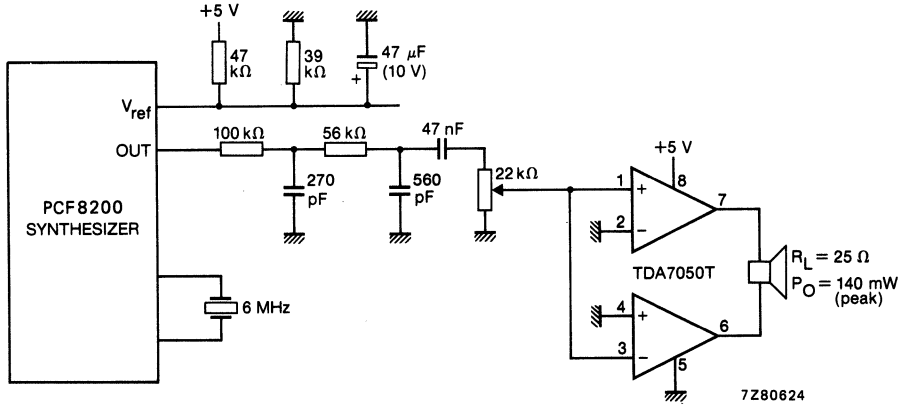


Fig. 12 An example of an output configuration.

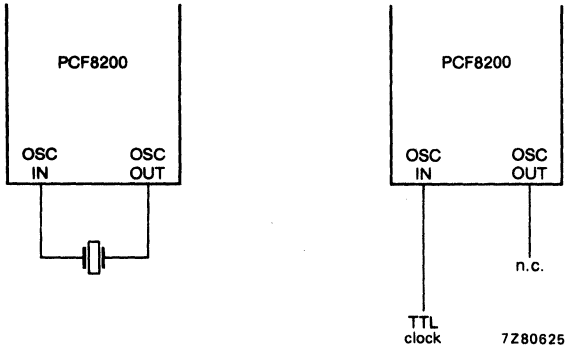


Fig. 13 Oscillator clock configurations.

5

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

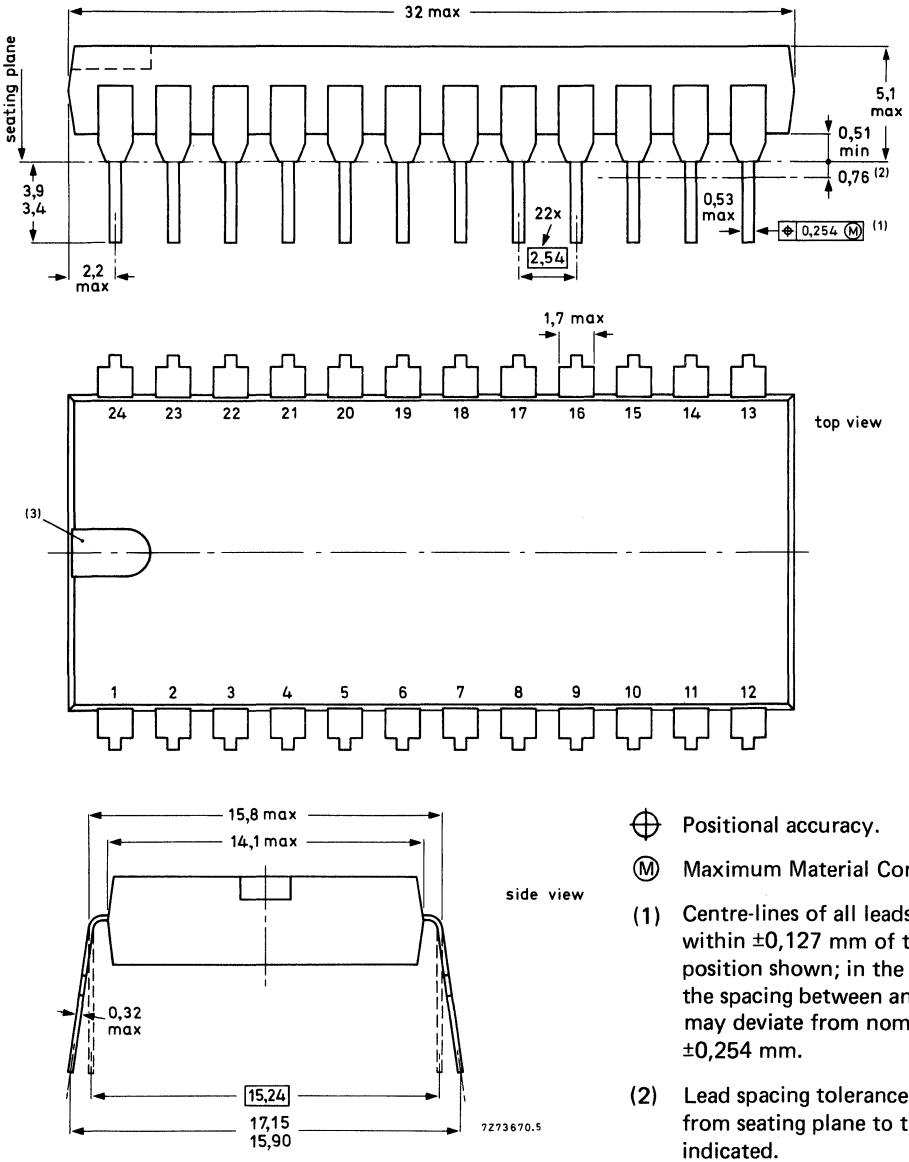
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

Pulse and DTMF Dialer with Redial | PCD3310

DESCRIPTION

The PCD3310 is a single-chip silicon-gate CMOS integrated circuit with an on-chip oscillator for a 3.58MHz crystal. It is a dual-standard dialing circuit for either pulse dialing (PD) or dual tone multi-frequency (DTMF) dialing.

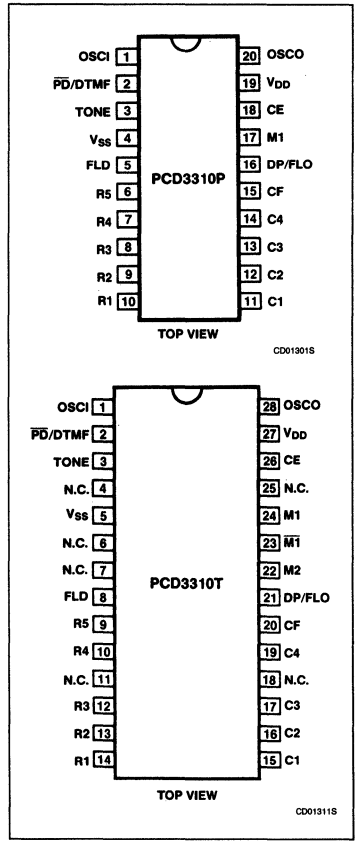
Input data is derived from any standard matrix keypad for dialing in either DP or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode, bursts as well as pauses are timed to a minimum in manual dialing, the maximum depending on the key depression time.

FEATURES

- **PD and DTMF dialing.**
- **23-digit capacity for redial operation (cursor method)**
- **Memory clear and electronic notepad**
- **Mixed mode dialing (start with DP and end with DTMF dialing**
- **Dual redial buffers for PABX and public calls**
- **Four extra function keys: program, flash, redial and PD to DTMF (mixed dialing)**
- **DTMF timing:**
  - **manual dialing-minimum duration for bursts and pauses**
  - **redialing-calibrated timing**
- **On-chip voltage reference for supply and temperature independent tone output**
- **On-chip filtering for low output distortion (CEPT CS 203 compatible)**
- **On-chip oscillator with low cost 3.58MHz TV color-burst crystal**
- **Uses standard single-contact or double-contact (common left open) keypad**
- **Keyboard entries fully debounced at both edges**
- **Flash (register recall) output**

PIN CONFIGURATION



Pulse and DTMF Dialer with Redial | PCD3310

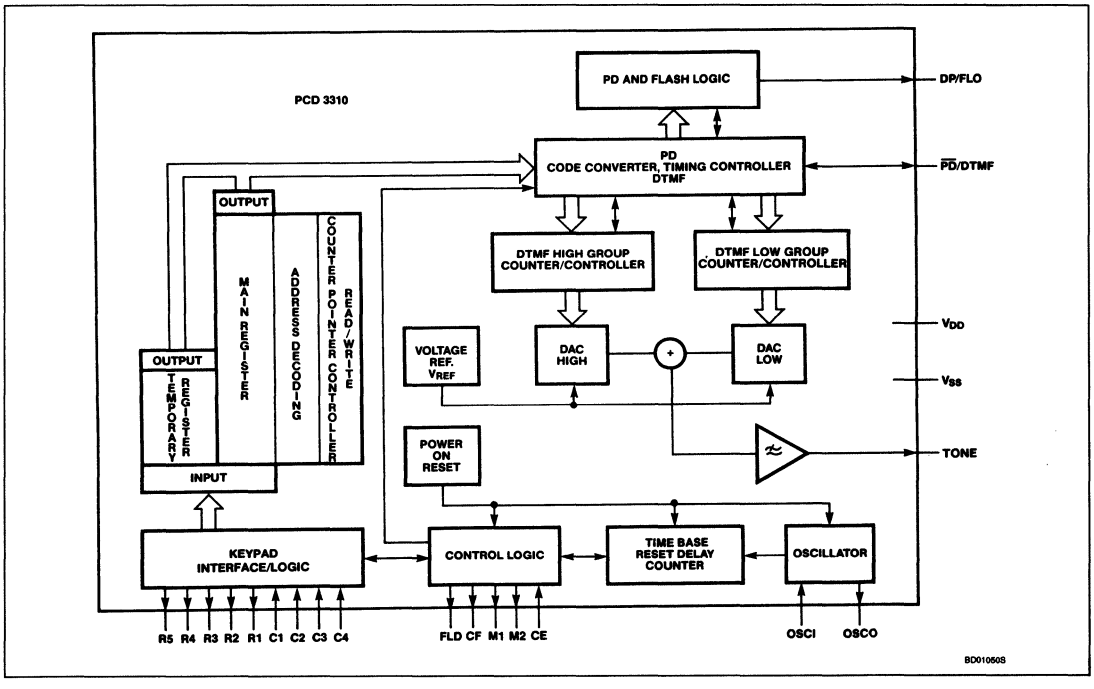
ORDERING CODE

	V_{DD} = 3.0V ± 5%; T_A = −25°C to +70°C		
	Pins	**Package**	**Notes**
PCD3310P	20	Plastic DIP	SOT146
PCD3310T	28	Plastic mini-Pack	SO28; SOT136

REFERENCE DATA

PARAMETER	SYMBOL	LIMITS			UNIT
		Min	Typ	Max	
Operating supply voltage	V_{DD}	2.5		6.0	V
Standby supply voltage	V_{DDO}	1.8		6.0	V
Low standby current (on-hook) at V_{DDO} = 1.8V	I_{DDO}			5	=mμA
Operating currents at V_{DD} = 3.0V Conversation mode Pulse dialing mode DTMF dialing mode	 I_{DDC} I_{DDP} I_{DDF}			 60 200 1.2	 =mμA =mμA mA
DTMF voltage levels (r.m.s. values)					mV_{rms}
High Group	V_{TONE}		192		mV_{rms}
Low Group	V_{TONE}		150		mV_{rms}
Pre-emphasis	ΔV		2.1		dB
Total harmonic distortion	d_{tot}		−25		dB
Operating ambient temperature range	T_A	−25		+70	°C

BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The PCD3311 and PCD3312 are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With their on-chip voltage reference the PCD3311 and PCD3312 provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	1,2	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	–25	–	dB
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINES

PCD3311P: 14-lead DIL; plastic (SOT-27K, M, T).
PCD3311T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).
PCD3312P: 8-lead DIL; plastic (SOT-97A).
PCD3312T: 8-lead mini-pack; plastic (VSO-8; SOT-176).

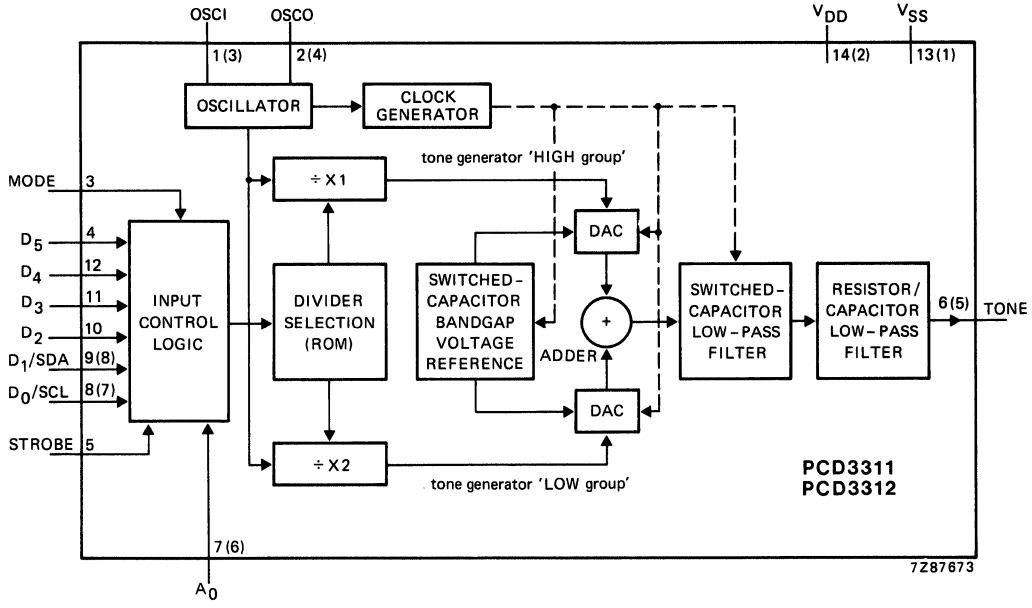


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312.

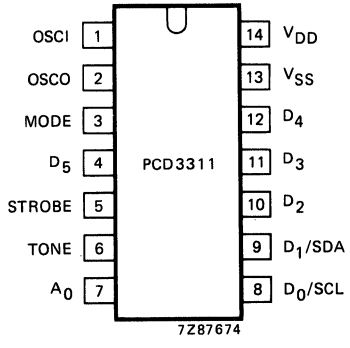


Fig. 2 Pinning diagram for the PCD3311.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C bus)
9	D_0/SDA	parallel data input* or serial data line (I^2C) bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

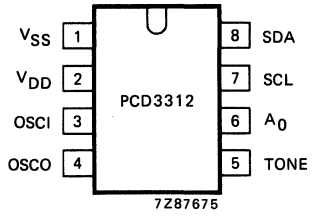


Fig. 3 Pinning diagram for the PCD3312.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311 and PCD3312 is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311), or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus (for both PCD3311 and PCD3312).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

FUNCTIONAL DESCRIPTION (continued)

Strobe input (STROBE, only for the PCD3311)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311 by setting MODE input LOW.

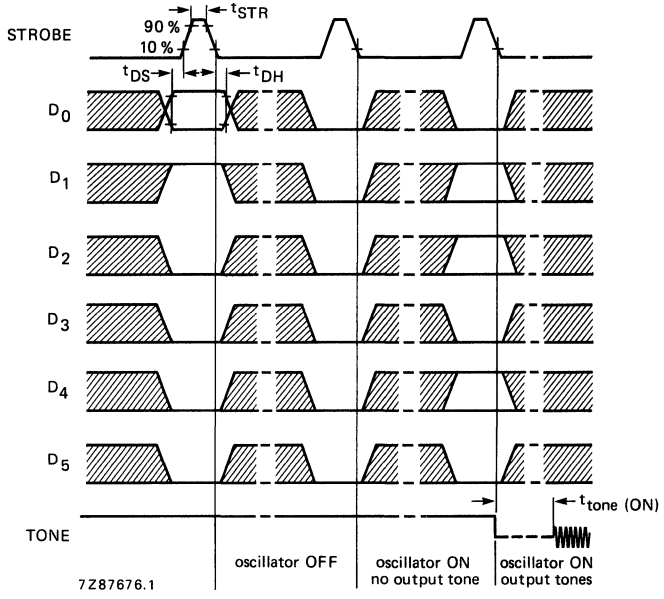


Fig. 4 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311 the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see "CHARACTERISTICS OF THE I^2C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311 or PCD3312 devices are connected to the same I^2C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see Fig. 5)

The PCD3311 and PCD3312 are always slave receivers in the I²C bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311 as well as for the PCD3312, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

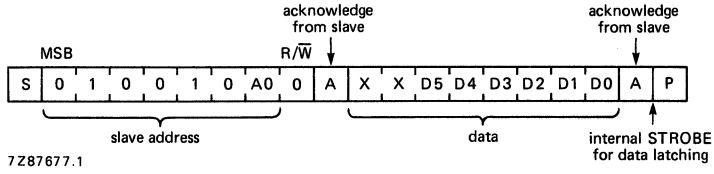


Fig. 5 I²C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 2 Input data for control (no output tone; TONE at V_{DD})

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X= don't care

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz	remarks
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz**
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level

0 = L = LOW voltage level

CHARACTERISTICS OF THE I²C BUS (continued)

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

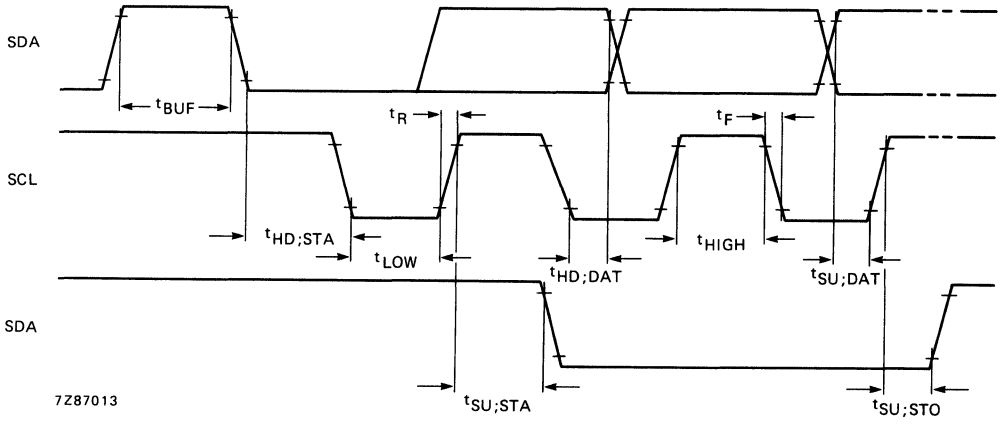


Fig. 10 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

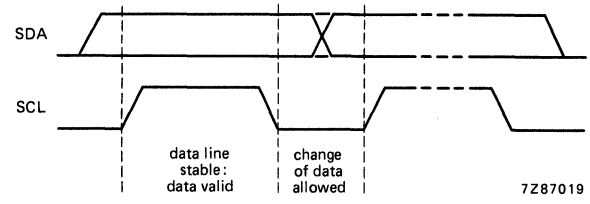


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

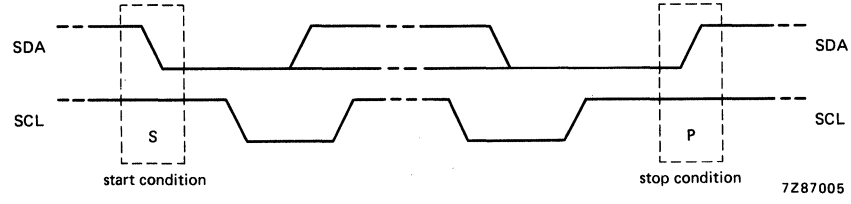


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

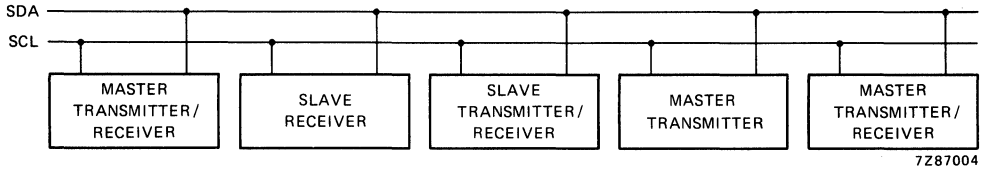


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

5

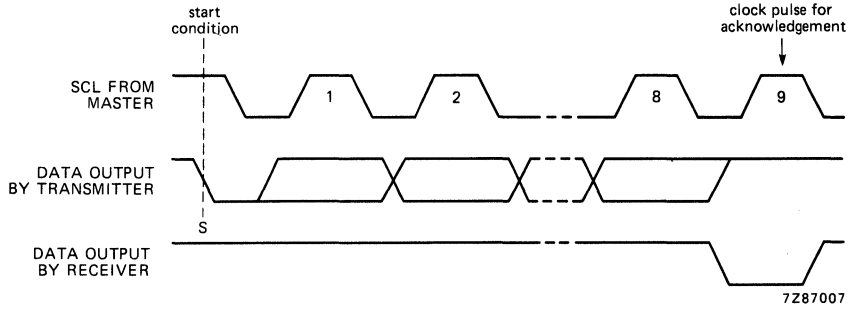


Fig. 9 Acknowledgement on the I^2C bus.

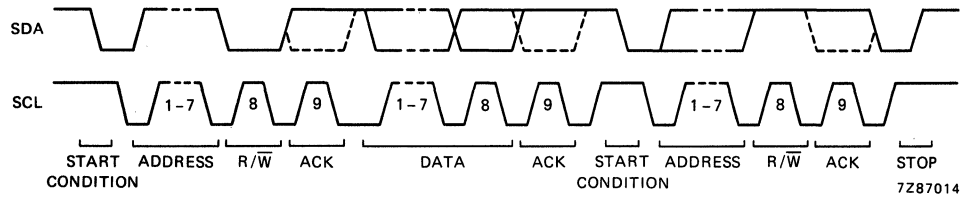


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

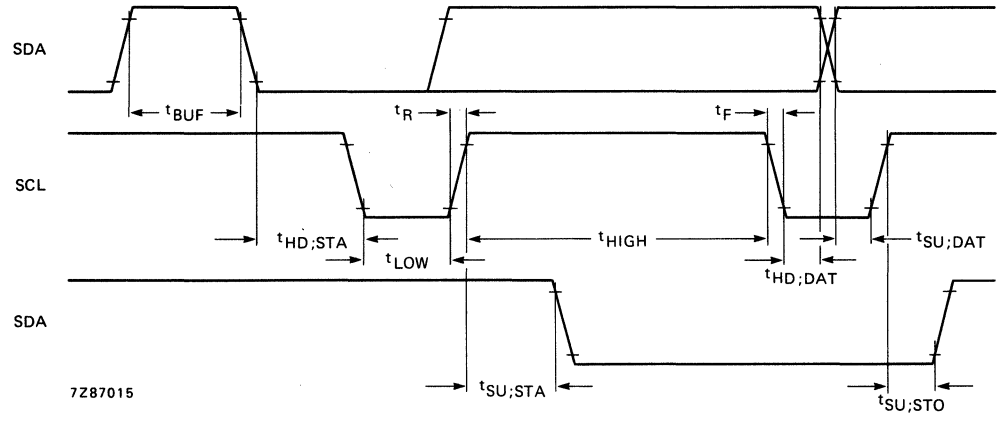


Fig. 12 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

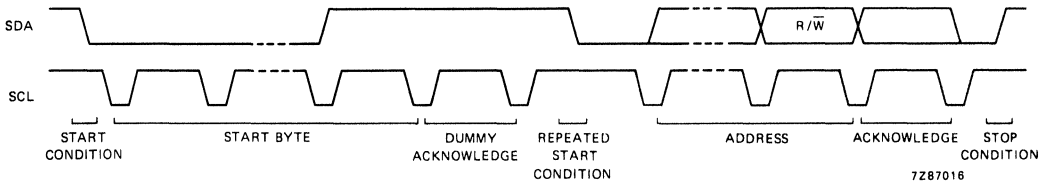


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
D.C. input current (any input)	$\pm I_I$	−	10	mA
D.C. output current (any output)	$\pm I_O$	−	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	−	50	mA
Power dissipation per output	P_O	−	50	mW
Total power dissipation per package	P_{tot}	−	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	−	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	−	50	100	μA
single output tone	I_{DD}	−	0,5	1,0	mA
dual output tone	I_{DD}	−	0,6	1,2	mA
Static standby current oscillator OFF; note 1	I_{DDO}	−	−	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	−	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	−	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current $V_I = V_{DD}$	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	−	−	mA
Clock frequency (see Fig. 10)	f_{SCL}	−	−	100	kHz
Input capacitance; $V_I = V_{SS}$	C_I	−	−	7	pF
Allowable input spike pulse width	t_I	−	−	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 14)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
D.C. voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	−25	–	dB
modem tone, note 3	THD	–	−29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

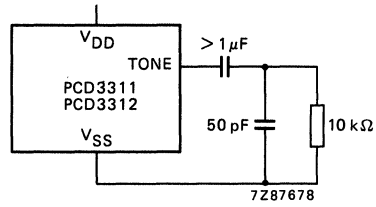


Fig. 14 TONE output test circuit.

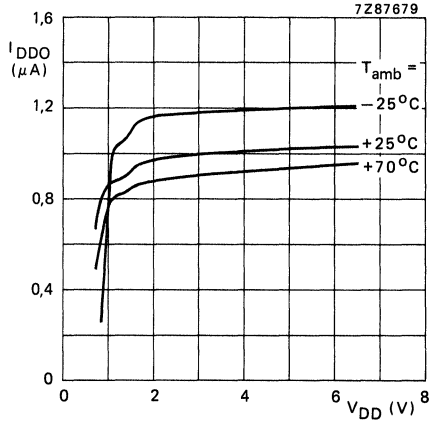


Fig. 15 Standby supply current as a function of supply voltage; oscillator OFF.

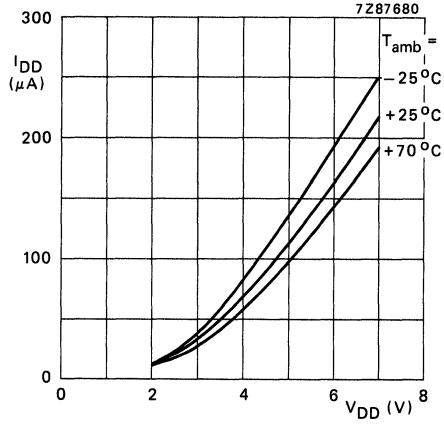


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

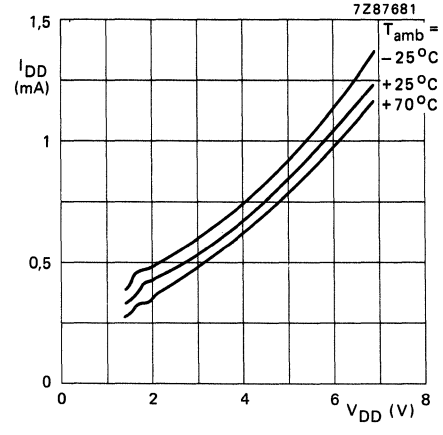


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

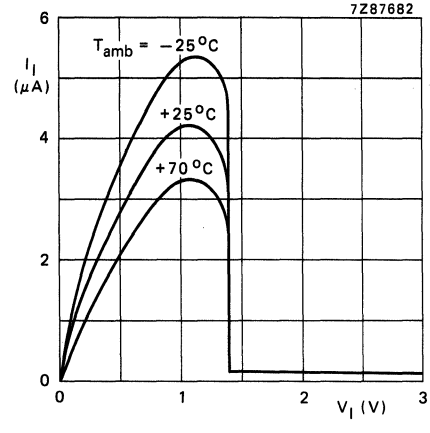


Fig. 18 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

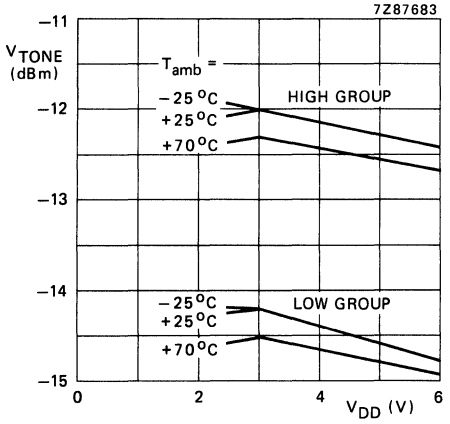


Fig. 19 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

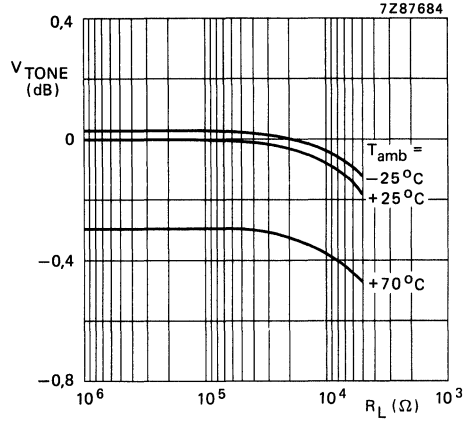


Fig. 20 Dual tone output voltage level as a function of output load resistance.

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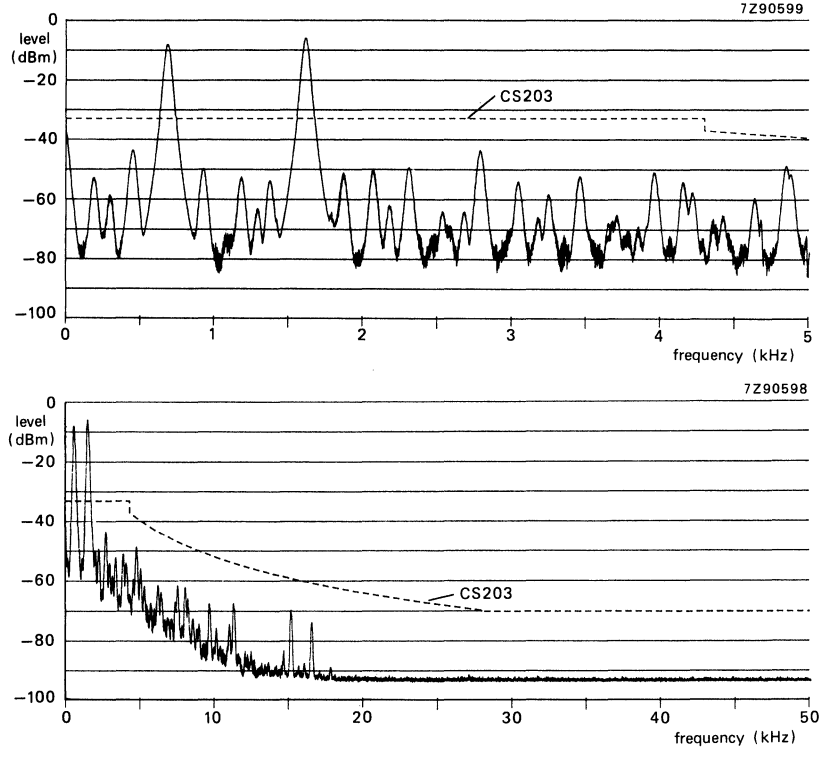


Fig. 21 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

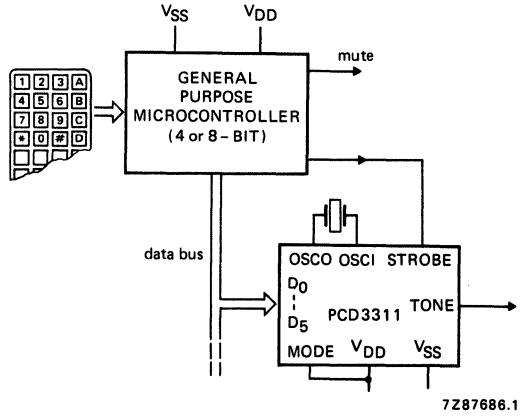


Fig. 22 PCD3311 driven by a microcontroller with parallel data-bus.

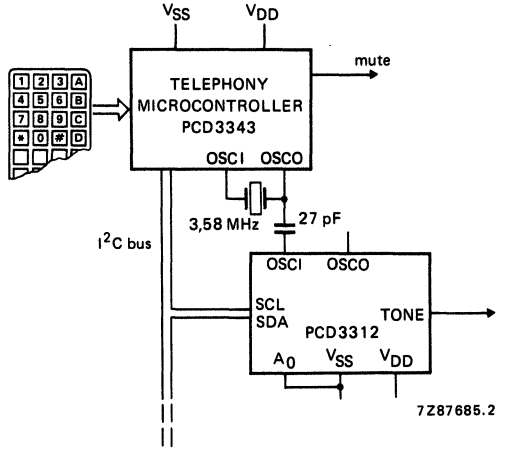


Fig. 23 PCD3312 driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311 with MODE = V_{SS}.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CMOS Redial and Repertory Dialer PCD3315

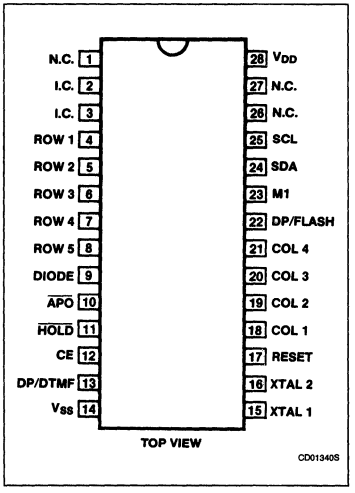
DESCRIPTION

The PCD3315 is a single chip CMOS dialer IC for telephone sets. It has two dialing modes: pulse dialing (PD), and dual tone multi-frequency (DTMF) when used in conjunction with tone generator PCD3312. As well as manual dialing it also features several automatic functions, e.g. redial, extended redial, notepad and repertory dial.

FEATURES

- **Pulse dialing**
- **DTMF dial control of tone generator PCD3312**
- **Redial**
- **Extended redial**
- **Electronic notepad**
- **Ten repertory dial numbers**
- **18-digit capacity for each autodial memory**
- **Maximum of 36 digits per call**
- **Flash or register recall**
- **Uses standard 4 x 4 keyboard (single or double contact)**
- **Four extra function keys: program/autodial, flash, redial, access pause**
- **Access pause generation and termination**
- **Automatic PABX-digit recognition resulting in an access pause insertion**
- **Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognizers**
- **Four diode or strap functions: general/German, access pause time, reset delay time, general: mark-space ratio/German: prepulse**
- **Manual reset of autodial RAM**
- **On-chip power-on reset**
- **Programmed for improved noise immunity.**

PIN CONFIGURATION



5

CMOS Redial And Repertory Dialer PCD3315

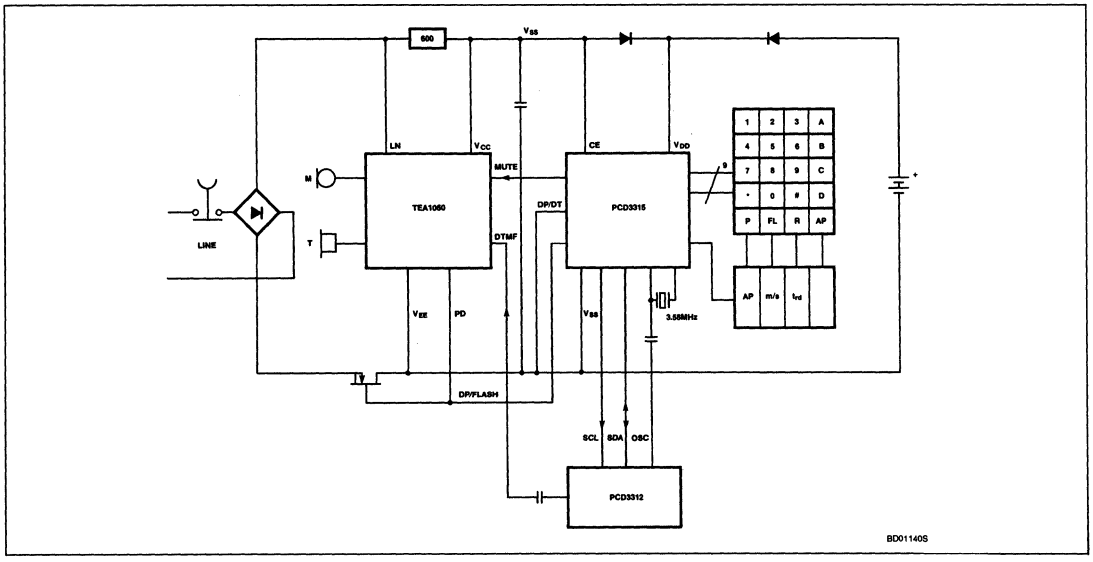
ORDERING CODE

	V_{DD} = 3.0V ± 5% T_A = −25°C to +70°C		
	Pins	**Packages**	**Notes**
PCD3315 P	28	Plastic DIP	SOT-117
PCD3315 T	28	Plastic mini-pack	SO-28; SOT-136A

REFERENCE DATA

PARAMETER	**SYMBOL**	**LIMIT**			**UNIT**
		Min	**Typ**	**Max**	
Operating supply voltage	V_{DD}	2.75		6.0	V
Standby supply voltage	V_{DD}	1			V
Operating currents at V_{DD} = 3.0V conversation mode	I_{DD}		300		=mμA
Standby supply at V_{DD} = 1.8V; T_A = 25°C	I_{DD}		1.2		=mμA
Crystal frequency	f		3.58		MHz
Operating ambient temperature range	T_A	−25		+70	°C

BLOCK DIAGRAM



CMOS Microcontroller for Telephone Sets PCD3343

GENERAL DESCRIPTION

The PCD3343 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCF8500 family. It has special on-chip features for application in telephone sets.
The device is mask programmable, designed to provide telephone dialling facilities such as redial, repertory dial, emergency call, keyboard scan and control for liquid crystal display, pulse dial and/or DTMF dial via dedicated peripheral.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 3 K ROM bytes
- 224 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O which can be used in bus systems with more than one master (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, MAB8400 and PCF8500)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312 DTMF generator)
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

5

PACKAGE OUTLINES

PCD3343P: 28-lead DIL; plastic (SOT-117D).
PCD3343D: 28-lead DIL; ceramic (CERDIP) (SOT-135A).
PCD3343T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

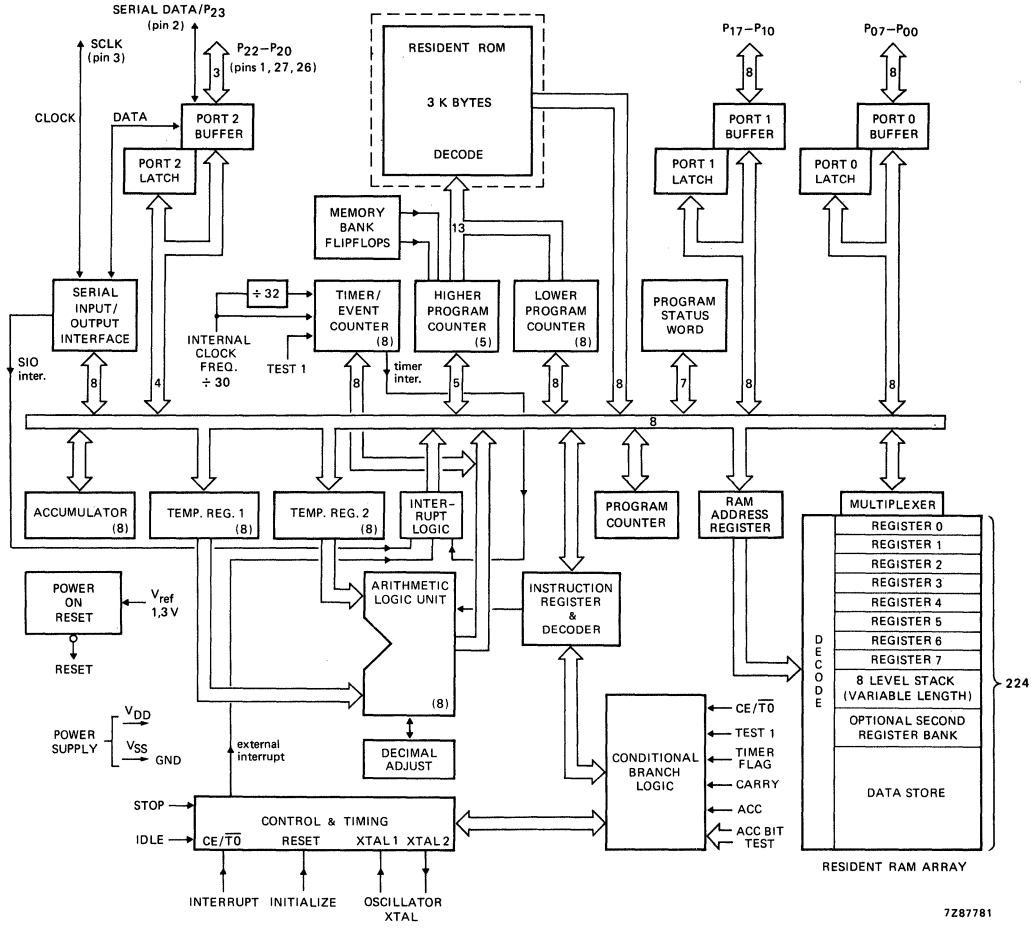
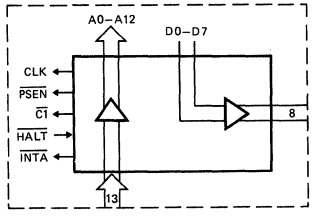
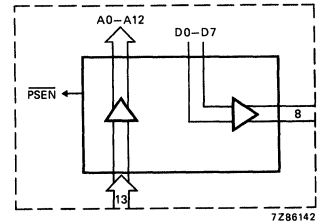


Fig. 1 Block diagram; PCD3343.



(a)

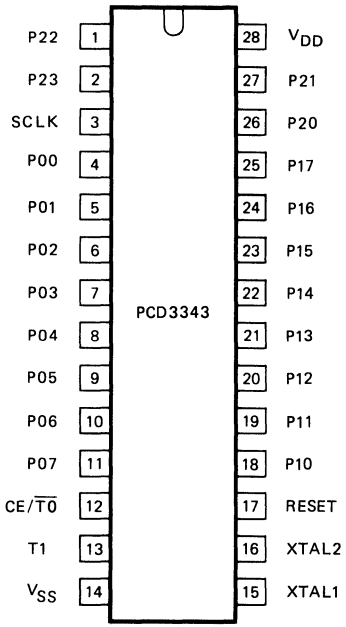
Fig. 1a Replacement of dotted part in Fig. 1, for the PCF8500F bond-out version.



(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF8500B 'Piggy-back' version.

PINNING



Note CE/$\overline{T0}$ is labelled $\overline{INT}$/T0 on the PCF8500B and has inverted polarity. 7Z87783

Fig. 2 Pinning diagram: PCD3343 and bottom pinning PCF8500B.

PIN DESIGNATION

3	SCLK	**Clock**: bidirectional clock for serial I/O.
4-11	P00-P07	**Port 0**: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	**Interrupt/Test 0**: external interrupt input (sensitive to positive-going edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	**Ground**: circuit earth potential.
15	XTAL 1	**Crystal input**: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	**Reset input**: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	**Port 1**: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	**Port 2**: 4-bit quasi-bidirectional I/O port. P23 is the serial data input/output in serial I/O mode.
28	V_{DD}	**Power supply**: 1,8 V to 6 V.

PINNING (continued)

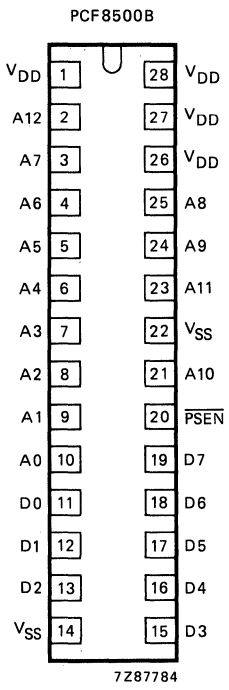


Fig. 3 Pinning diagram: PCF8500B 'Piggy-back' version top pinning; to access a 2732 or 2764 EPROM.

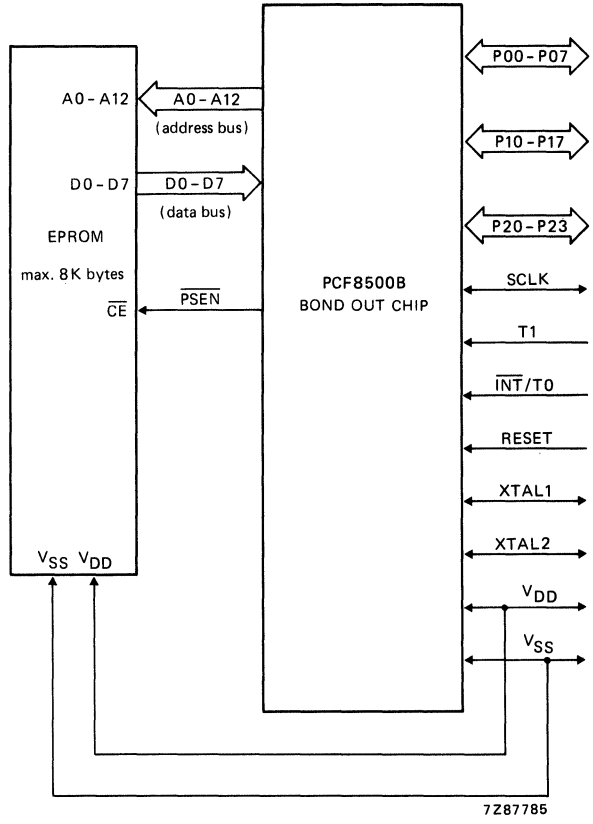


Fig. 3a Connection of EPROM to 'Piggy-back' package PCF8500B.

PIN DESIGNATION

14, 22	V_{SS}	**Ground**
1, 26-28	V_{DD}	**Power supply**
10-3, 25, 24, 21, 23, 2	A0-A12	**Address outputs**
11-13, 15-19	D0-D7	**Data**
20	$\overline{PSEN}$	**Program store enable**

Notes

1. RAM capacity of PCF8500B is 256 bytes.
2. Access time for ROMS/EPROMS to be below 7 x $1/f_{XTAL}$.
3. Pin 12 CE/$\overline{T0}$ is on the PCF8500B, inverted and labelled $\overline{INT}$/T0.

FUNCTIONAL DESCRIPTION

Bond-out version PCF8500F

The PCF8500F is a microcontroller that contains no on-board ROM, but has all address and data lines brought-out to access an external ROM or EPROM. This version has more pins than the PCD3343 with on-board ROM (see Fig. 1a). The RAM has 256 bytes. It can address 8 K bytes of ROM.

'Piggy-back' version PCF8500B

The PCF8500B is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the standard DIL package. The RAM has 256 bytes and can also address 8 K bytes of program memory.

Program memory PCD3343

The program memory consists of 3072 bytes (8-bit words), in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 4 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 5; contains the first byte of a serial I/O interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory PCD3343

Data memory consists of 224 bytes (8-bit words), random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 5 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

FUNCTIONAL DESCRIPTION (continued)

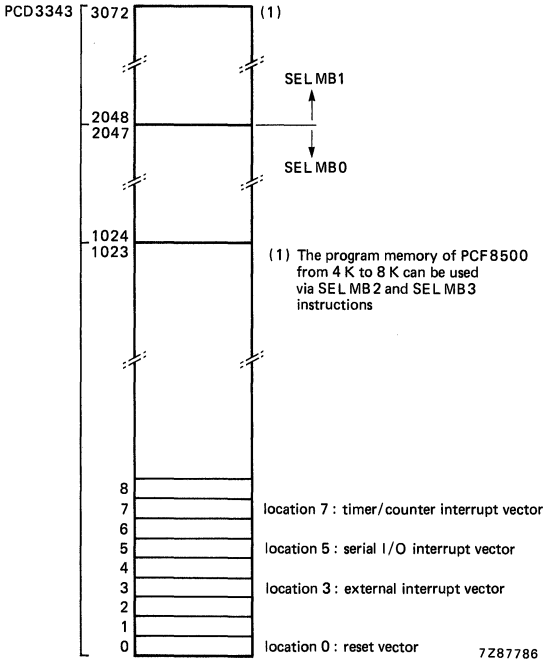


Fig. 4 Program memory map.

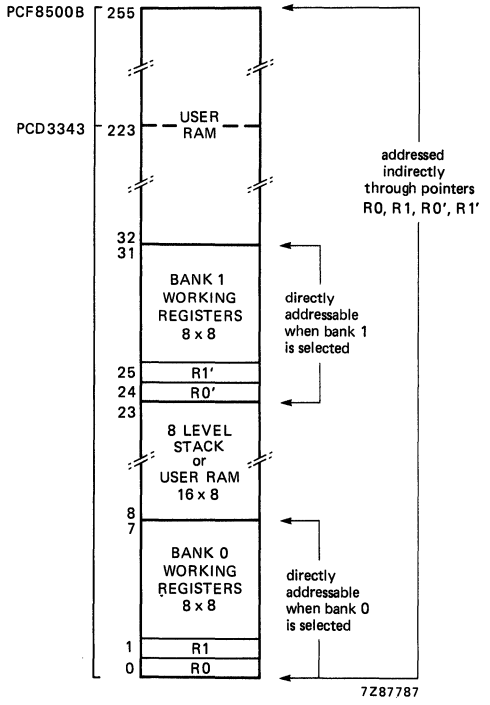


Fig. 5 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 6) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 223 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

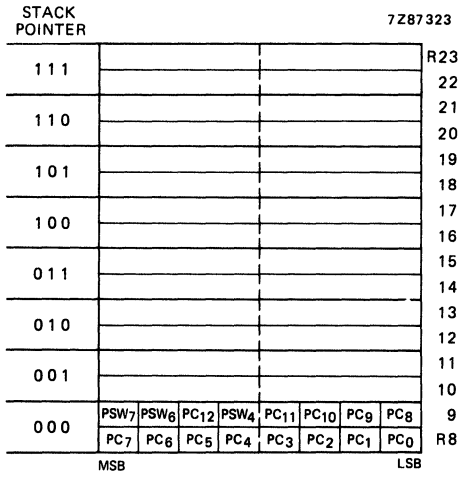


Fig. 6 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01') the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 7).

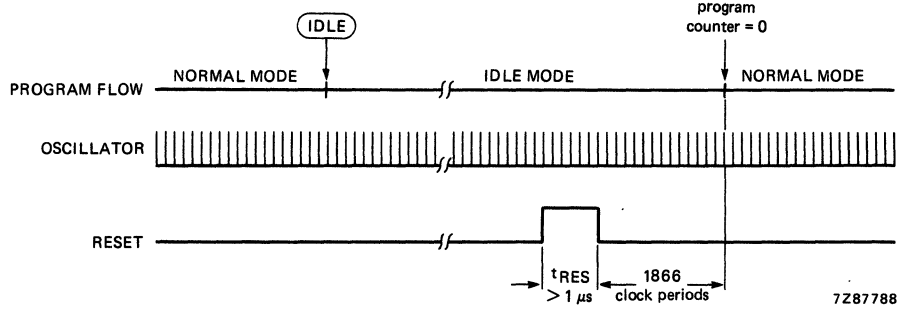


Fig. 7 Exit from IDLE mode via a RESET.

FUNCTIONAL DESCRIPTION (continued)

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{T0}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig. 8).

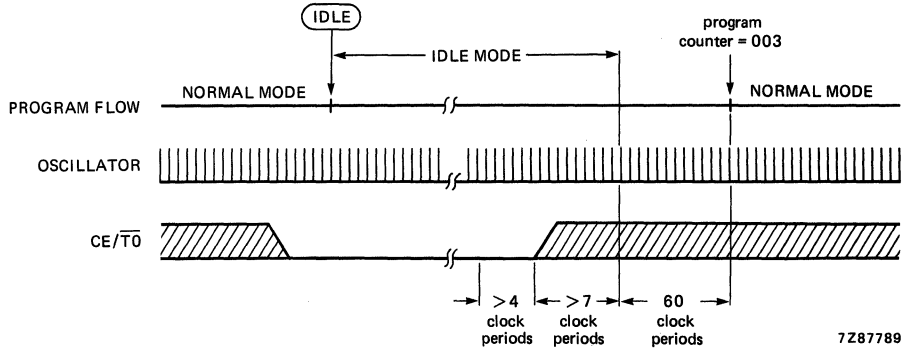


Fig. 8 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for 4 CP (clock periods) followed by a HIGH for 7 CP. After the initial forced CALL H'003' operation (60 CP) the program continues with the external interrupt service routine.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 9).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

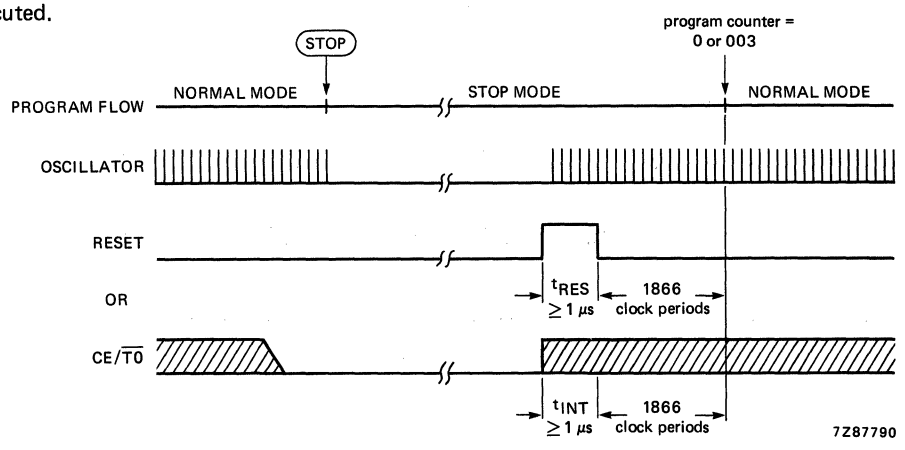


Fig. 9 Entering and exiting the STOP mode.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism.

When the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

I/O facilities

The PCD3343 family has 23 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P00 to P07)
- Port 1 parallel port of 8 lines (P10 to P17)
- Port 2 parallel port of 4 lines (P20 to P23)
- SCLK serial I/O consisting of a data line shared with a parallel port line (P23) and a separate clock line SCLK
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

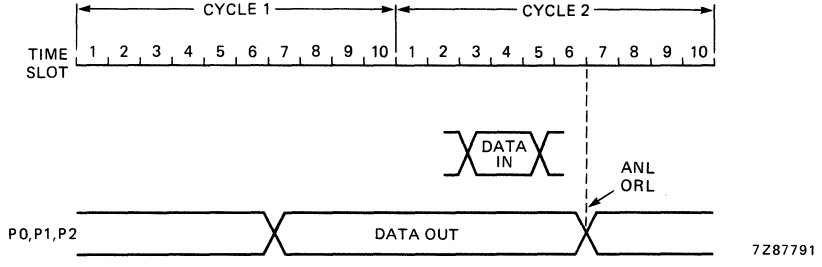


Fig. 10 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

Fig. 11 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.

Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current provides sufficient source current for a

FUNCTIONAL DESCRIPTION (continued)

TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3343 offers the possibility to select individually 19 of the 20 parallel port pins (not P23), by the following mask options:

Option 1- STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2 (1,5 mA). TR2 is only active during 1 clock cycle (0,28 μs at 3,58 MHz).

Option 2- OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 12).

Option 3- PUSH-PULL OUTPUT; drive capability of the output will be 1,5 mA (typ.) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig. 13).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S-SET; after RESET this pin will be initialized to HIGH.

Option R-RESET; after RESET this pin will be initialized to LOW.

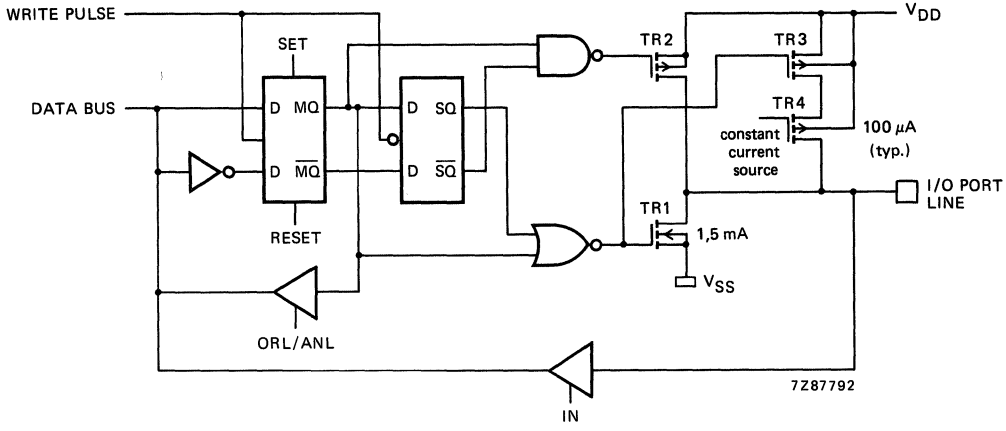


Fig. 11 Standard output with switched pull-up current source.

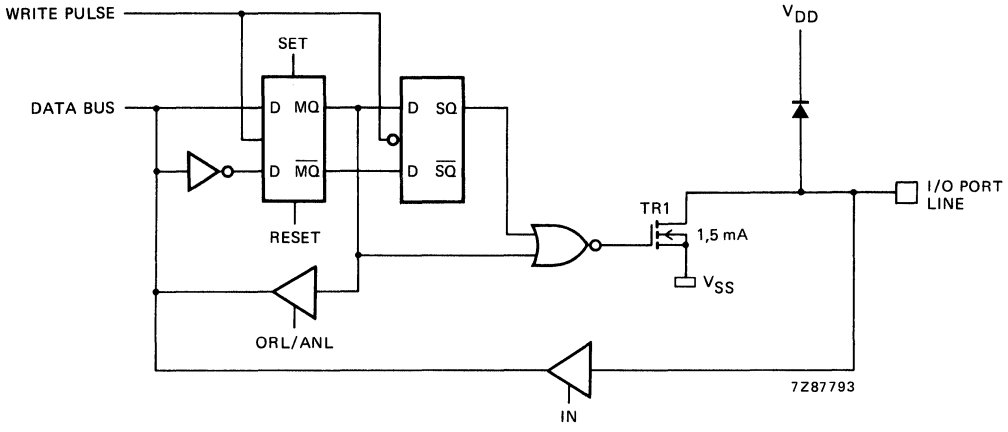


Fig. 12 Open drain output.

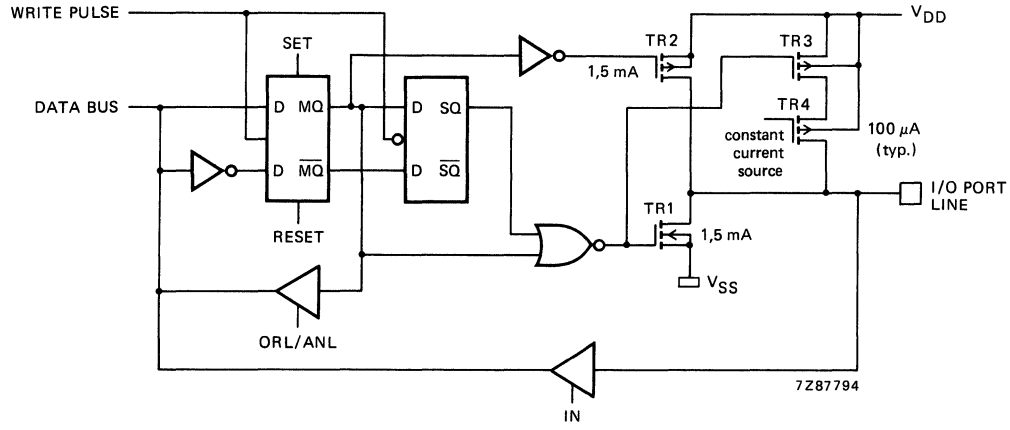


Fig. 13 Push-pull output.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (SIO)

The PCD3343 has an on-chip serial I/O interface. This SIO interface is a versatile feature in an intelligent telephone set, as shown in application diagram Fig. 32.

In this application the SIO is used to communicate with the different peripherals, such as:

- DTMF generator (PCD3312)
- LCD drivers (PCF8577)
- External RAM (PCD8571)
- Clock calendar (PCB8573)

No extra hardware is required for decoding, addressing and data processing.

Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCD3343 only when a complete byte is received. It then reads the data byte in one instruction. Likewise during transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCD3343 serial I/O system allows any number of devices from PCF8500 family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCD3343 is switched off. This means that the serial I/O logic will remain in the state it was at the occurance of the STOP instruction. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCD3343 has finished a serial data transfer.

Serial I/O interface

Figure 14 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK) while the data line shares pin 2 (serial data) with the I/O line P23 of port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line; (P23 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and TRX (see Table 1)

These bits determine the operating mode of the serial I/O interface.

Table 1 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

FUNCTIONAL DESCRIPTION (continued)

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

Serial clock control word (S2)

Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 3,58 MHz crystal is used, the frequency of the serial clock can be varied between 92 kHz and 580 Hz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ES0 = '0'.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

Table 2 SIO clock pulse frequency control when using a 3,58 MHz crystal

hexadecimal S20-S24 code	divisor	f_{SCLK} (kHz) (approximate)
0	not allowed	
1	39	92
2	45	80
3	51	70
4	63	57
5	75	48
6	87	41
7	99	36
8	123	29
9	147	24
A	171	21
B	195	18
C	243	15
D	291	12
E	339	11
F	387	9,2
10	483	7,4
11	579	6,2
12	675	5,3
13	771	4,6
14	963	3,7
15	1155	3,1
16	1347	2,7
17	1539	2,3
18	1923	1,9
19	2307	1,6
1A	2691	1,3
1B	3075	1,2
1C	3843	0,93
1D	4611	0,78
1E	5379	0,67
1F	6147	0,58

FUNCTIONAL DESCRIPTION (continued)

Table 3 Serial I/O addresses for telephony peripherals

type	address 7	6	5	4	3	2	1	0	description
PCF8570A	1	0	1	0	A2	A1	X	R/$\overline{W}$	2 K RAM
PCF8570	1	0	1	0	A2	A1	A0	R/$\overline{W}$	2 K RAM
PCD8571	1	0	1	0	A2	A1	A0	R/$\overline{W}$	1 K RAM
PCD3311	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCD3312	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCE2111	0	0	0	0	0	0	1	0	LCD driver *
PCD8573	1	1	0	1	0	A1	A0	R/$\overline{W}$	clock calendar
PCF8574	0	0	1	1	A2	A1	A0	R/$\overline{W}$	8-bit I/O expander
PCF8576	0	1	1	1	0	0	SA0	R/$\overline{W}$	1 : 4 LCD driver
PCF8577	0	1	1	1	0	1	0	R/$\overline{W}$	1 : 2 LCD driver

* LCD driver requires an additional enable line.

CMOS Microcontroller for Telephone Sets PCD3343

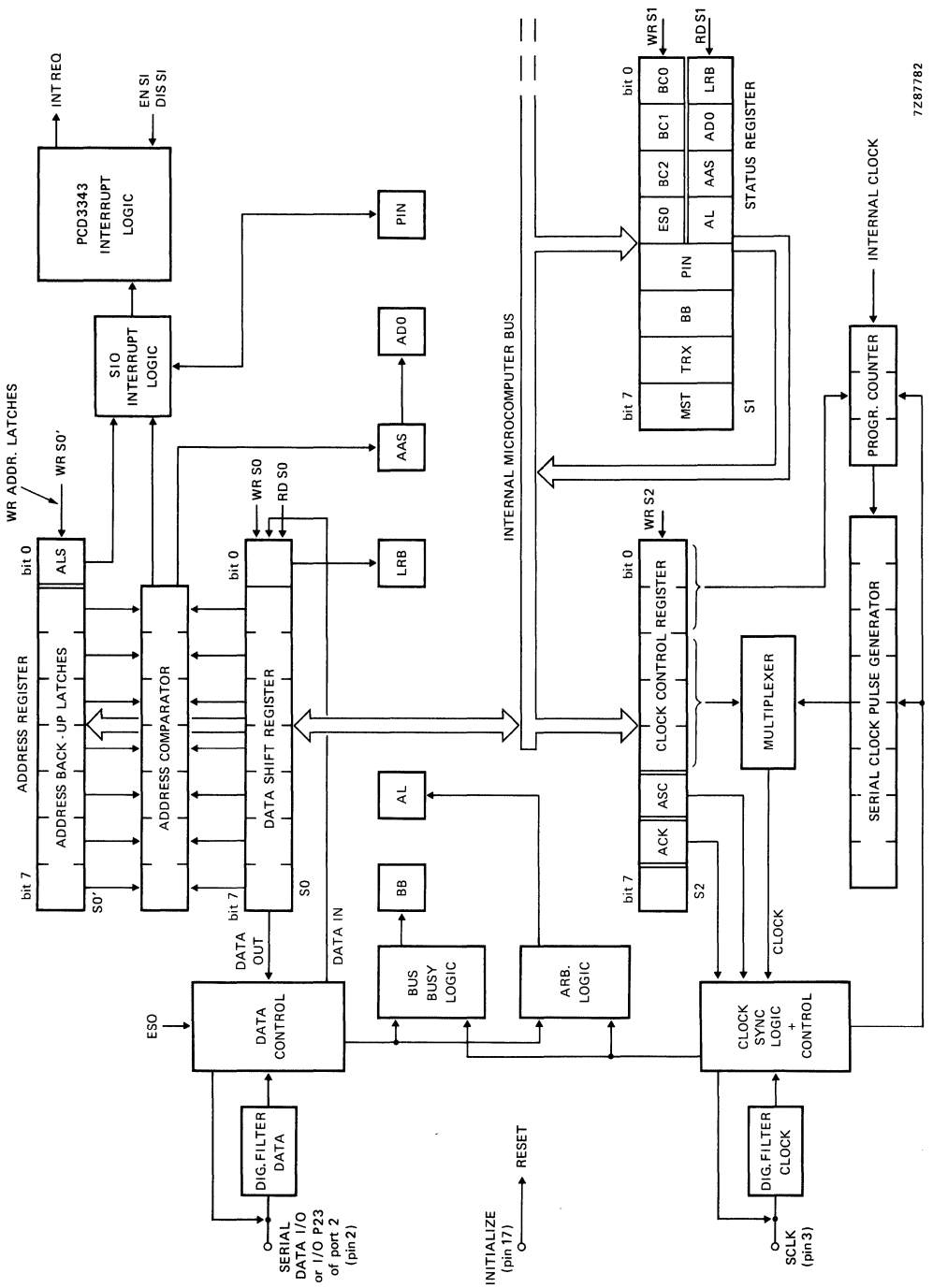


Fig. 14 Serial I/O interface.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (see Fig. 15)

When the external interrupt is enabled, a LOW-to-HIGH transition on the CE/$\overline{T0}$ input initiates an external interrupt subroutine which causes a CALL to program memory location 3 following completion of the current instruction.
The interrupt must remain enabled until the interrupt instruction is completed, otherwise the next instruction of the main program will be executed. Serial I/O interrupt, when enabled, causes a CALL to location 5, and a timer/event counter overflow forces a CALL to location 7 when the timer interrupt is enabled.

When an interrupt subroutine starts, the contents of the program counter and bits 4, 6 and 7 of the PSW have been saved in the program counter stack. Accumulator contents have to be saved by software. Interrupt acknowledgement can be carried out by software via port pins. All interrupt subroutines must reside in memory bank 0.

Since the interrupt system is single level, once an interrupt is detected, all further interrupt requests are latched, but ignored, pending a RETR instruction to re-enable the interrupt input logic. After executing RETR, the program continues in the main part; this is independent of the occurance of a second interrupt during the running of the first routine. If 2 or 3 interrupts occur simultaneously, their priority is:

- (1) external
- (2) serial I/O
- (3) timer/event counter

An external interrupt can be generated by using the timer/counter in the event counter mode. The counter is first preset to (H'FF'), then EN TCNTI instruction is executed. A LOW-to-HIGH transition of the T1 input will then initiate an interrupt subroutine and cause a CALL to location 7.

On execution of a DIS I instruction, the PCD3343 always clears the digital filter/latch and the External Interrupt Flag.

The Timer Flag (TF) is reset only when the JTF or JNTF instruction is executed or after RESET.

The Timer Interrupt Flag is set when timer overflow occurs, only if the timer interrupt is enabled.

The microcontroller will exit the IDLE mode when any one of the following three interrupts is enabled:

- External
- Serial I/O
- Timer/event counter

There is no internal pull-up or pull-down device connected to the external interrupt input (pin 12). If required pin 12 must be externally connected to a resistor ($R \leqslant 100\ k\Omega$). When the external interrupt is not used pin 12 must be connected to V_{SS}.

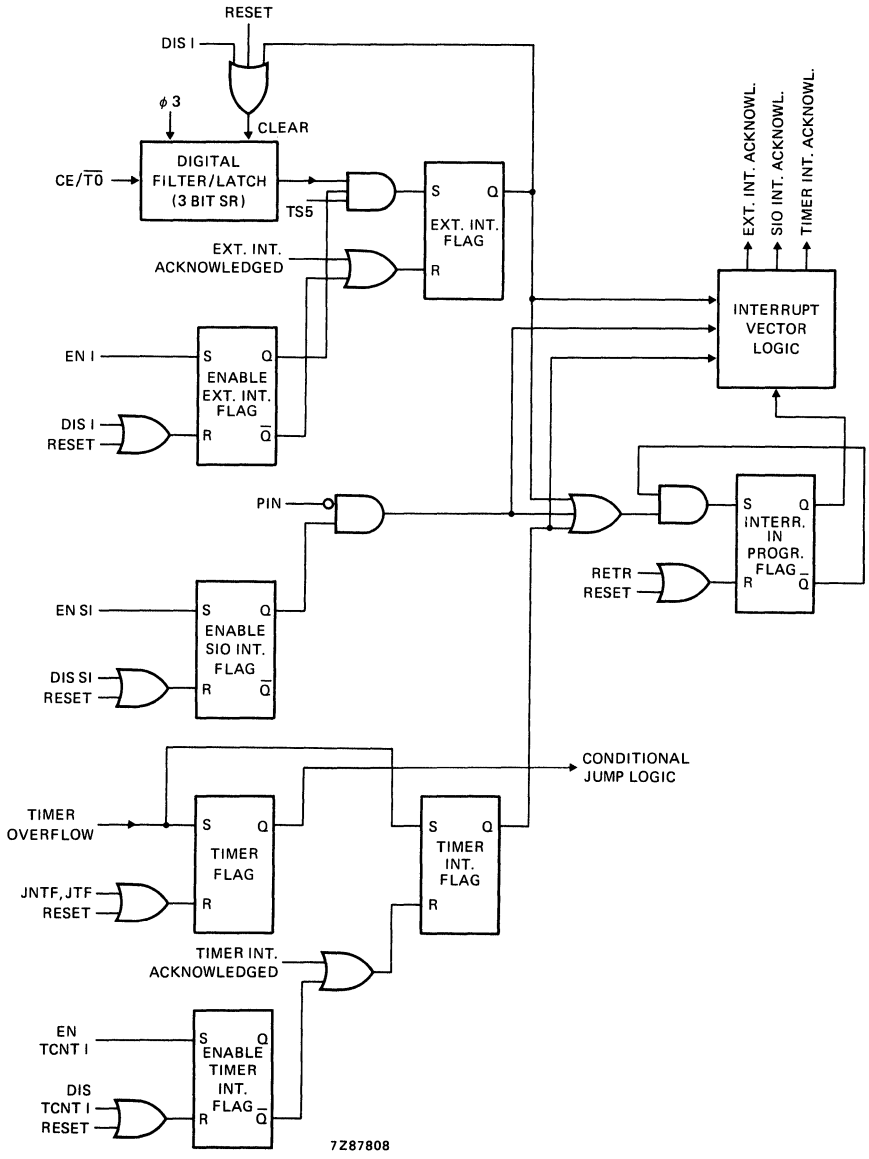


Fig. 15 Interrupt logic.

Notes to figure 15

1. CE/$\overline{T0}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing in ensured when CE/$\overline{T0}$ is LOW for > 4 CP followed by a HIGH for > 7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 16)

The 3,58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{T0}$ or RESET pin.

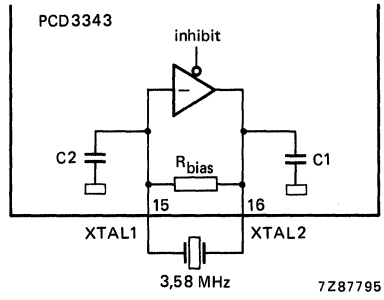


Fig. 16 Oscillator with integrated elements.

The oscillator has the output drive capability for the DTMF generator (PCD3311/3312) via pin 16 (XTAL 2). An external clock can be applied to pin 15 (XTAL 1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3,58 MHz crystal provides a 8,4 μs machine cycle. The range of the clock frequency is from 100 kHz up to a maximum which is a function of the supply voltage (see Fig. 23).

Timer/event counter (see Fig. 17)

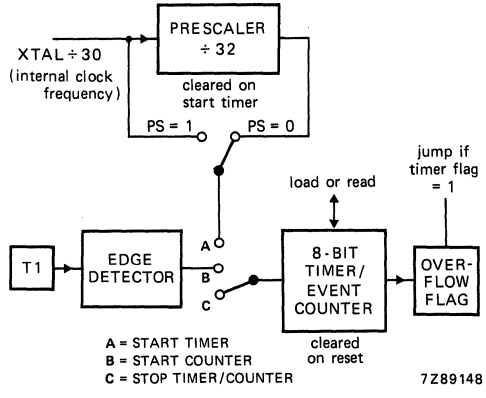


Fig. 17 Timer/event counter.

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 4 gives the instructions that control the counter and the prescaler, and the functions performed.

Table 4 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 13 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182,6 kHz for a 8,4 μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrpt Flag when the timer/event counter interrupt is enabled.

Program status word (see Fig. 18)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS); 0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS); 0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

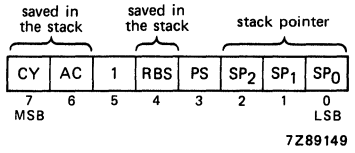


Fig. 18 Program status word.

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.
** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (continued)

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 19)

A 13-bit program counter is used to facilitate 8 K bytes of ROM being addressed. The arrangement of the bits is shown in figure 19. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

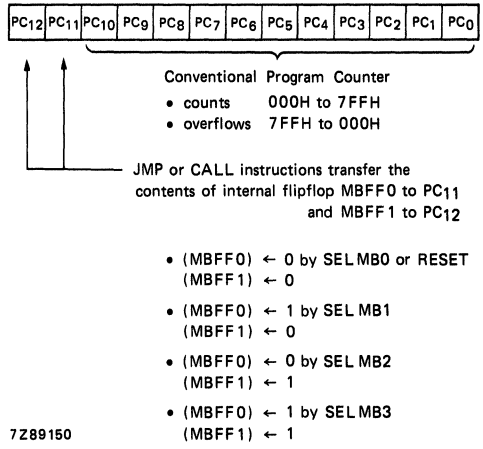


Fig. 19 Program counter.

Central processing unit

The PCD3343 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 5 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 5 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0*
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 13)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for $>$ 4 CP, followed by a HIGH for $>$ 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor (R = $\leqslant$ 100 kΩ). When T1 is not used pin 13 must be connected to V_{DD} or V_{SS}.

Reset (pin 17)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory band 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode

After the voltage is applied to RESET an internal delay of 1866 CP is introduced before the microcontroller commences operation.

* Because of the inverted interrupt input CE/$\overline{T0}$ the conditional jump JT0 is also inverted.

FUNCTIONAL DESCRIPTION (continued)

Power-on-reset and low-voltage detection (see Fig. 20)

In telephony applications, correct operation of the PCD3343 during moments of slowly changing supply voltages and low-voltage conditions is essential. This is achieved by the addition of an internal power-on-reset and low-voltage detection circuit.
To allow an external RESET signal being fed into the PCD3343, the reset pin (pin 17) has been configured as an input/output.

While a reset condition exists in the detection circuit, pin 17 is pulled HIGH by TR1 controlled by the reset circuit.
When the reset condition is not present a pull-down current source (TR2) will be activated. TR2 forces pin 17 LOW thus removing the RESET signal from the microcontroller.

Since the level at pin 17 is recognized by the microcontroller, the reset time constant can be stretched by connecting an external capacitor between V_{DD} and pin 17 (see Fig. 22).

The signal at pin 17 can also be used as an output to reset other devices in the system.

The internal reset circuit monitors the PCD3343 supply voltage. If the voltage drops below the switching level (typ. 1,3 V), a reset (HIGH) is applied to pin 17. This reset is removed (pin 17 goes LOW), after a fixed delay (t_d), when the supply voltage rises above the switching level again. The delay ensures a complete reset even when the supply voltage quickly rises above switching level after initial switch-on.

During a low-voltage condition the oscillator is inhibited to prevent complete discharge of a weak battery. The timing of the power-on-reset and low-voltage detection circuit is shown in figure 21.

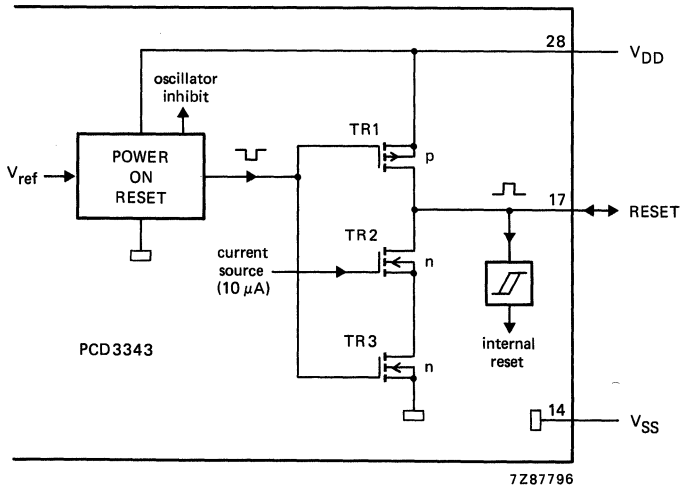
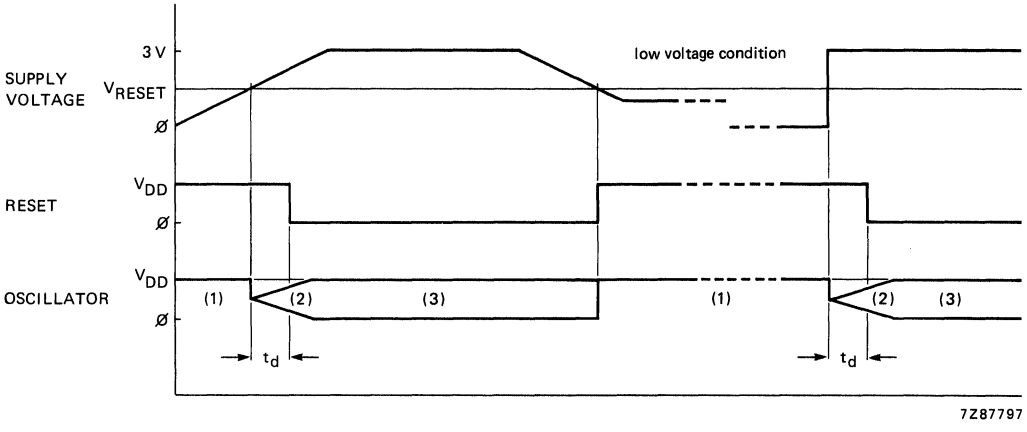


Fig. 20 Power-on-reset configuration.



Where: (1) Oscillator inhibited
(2) Oscillator starting
(3) Oscillator running, but may be stopped with a STOP condition

Fig. 21 Timing of power-on-reset and low-voltage detection.

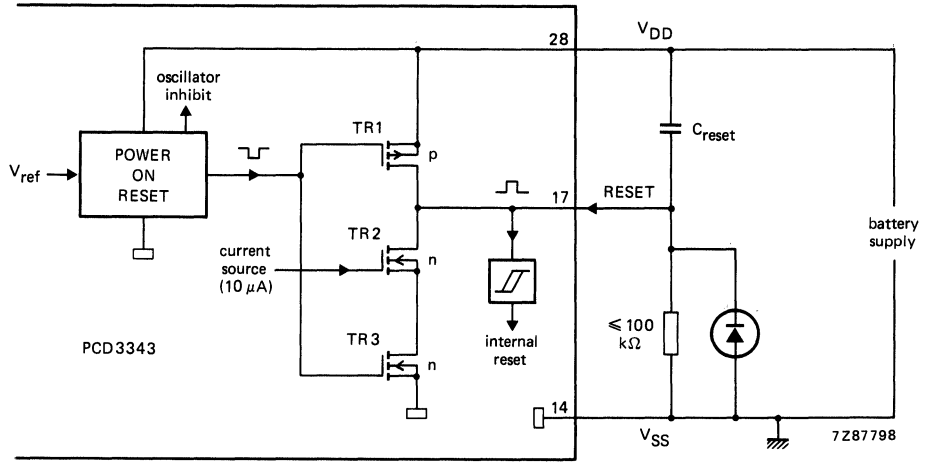


Fig. 22 Stretched power-on-reset with external capacitor.

INSTRUCTION SET

The PCD3343 instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 8 gives the instruction set of the PCD3343. Table 7 shows the instruction map and Table 6 details the symbols and definition descriptions that are used.

Table 6 Symbols and definitions used in Table 8

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

Table 7 PCD3343 instruction map

first hexadecimal character of opcode ↓

second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A,#data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp				MOV A,Sn			
1	INC @Rr		JBO addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr							
2	XCH A,@Rr		STOP	MOV A,#data	JMP page 1	EN TCNTI	JNTO addr	CLR A	XCH A,Rr							
3	XCHD A,@Rr		JB1 addr		CALL page 1	DIS TCNTI	JTO addr	CPL A	OUTL Pp,A				MOV Sn,A			
4	ORL A,@Rr		MOV A,T	ORL A,#data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr							
5	ANL A,@Rr		JB2 addr	ANL A,#data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr							
6	ADD A,@Rr		MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr							
7	ADDC A,@Rr		JB3 addr		CALL page 3			RR A	ADDC A,Rr							
8				RET	JMP page 4	EN SI			ORL Pp,#data							
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data				MOV Sn,#data			
A	MOV @Rr,A			MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A							
B	MOV @Rr,#data		JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data							
C	DEC @Rr				JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr							
D	XRL A,@Rr		JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr							
E	DJNZ @Rr,addr				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr							
F	MOV A,@Rr		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr							

INSTRUCTION SET (continued)

Table 8 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, (A)←((PC))		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	• 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) 6 (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	 7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 99 9A	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 89 8A	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	 8
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	 9
	MOV S_n, #data	9C 9D 9E	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P23, P22, P21, P20.
8. (S1) has a different meaning for read and write operation, see serial I/O interface.
9. (S2) is a write only register. Reading S2 will give value FFH.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 28)	V_{DD}		−0,8 to + 8	V
All input voltages	V_I		0,8 to V_{DD} + 0,8	V
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
Total power dissipation (see note)	P_{tot}	max.	500	mW
Power dissipation per output				
except P23, SCLK	P_O	max.	50	mW
P23, SCLK	P_O	max.	180	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Operating junction temperature	T_j	max.	125	°C

Note

Thermal resistance (junction to ambient)				
for SOT-117D	$R_{th\ j\text{-}a}$	max.	120	K/W
for SOT-135A	$R_{th\ j\text{-}a}$	max.	60	K/W
for SOT-136A	$R_{th\ j\text{-}a}$	max.	150	K/W

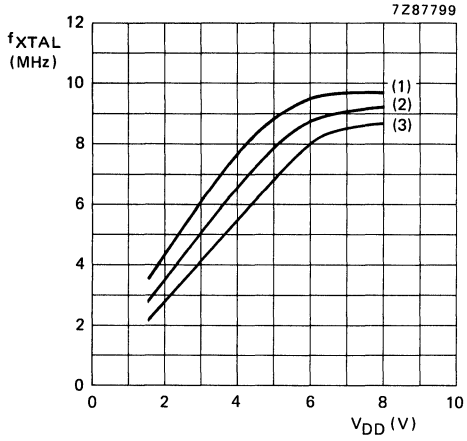
5

D.C. CHARACTERISTICS

V_{DD} = 2,75 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified.

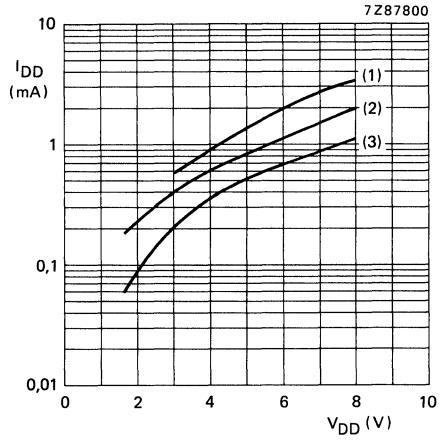
parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 23)	V_{DD}	1,8	–	6	V
STOP mode for RAM retention	V_{DD}	1,0	–	6	V
Supply current					
operating					
at V_{DD} = 3 V (see Fig. 24)	I_{DD}	–	600	–	μA
IDLE mode					
at V_{DD} = 3 V (see Fig. 25)	I_{DD}	–	300	–	μA
STOP mode (see Fig. 26 and note 1)					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,3	–	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V					
except P23/SDA, SCLK (see Fig. 27)	I_{OL}	0,75	1,5	–	mA
P23/SDA, SCLK (see Fig. 28)	I_{OL}	1,5	–	–	mA
Pull-up output source current HIGH (see Fig. 29)					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	25	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA
Push-pull output source current HIGH					
at V_{DD} = 3 V; $V_O = V_{DD}$−0,4 V	$-I_{OH}$	0,75	1,5	–	mA

Note 1
Crystal connected between XTAL 1 and XTAL 2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; CE and T1 at V_{SS}.



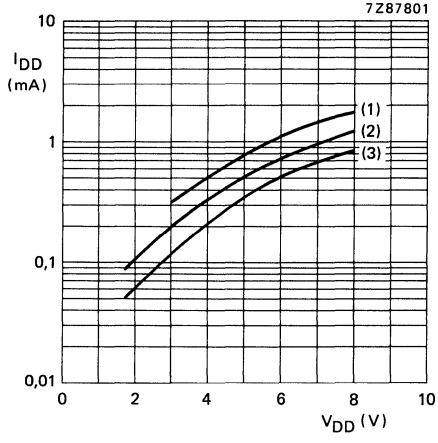
(1) T_{amb} = −25 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 70 °C

Fig. 23 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



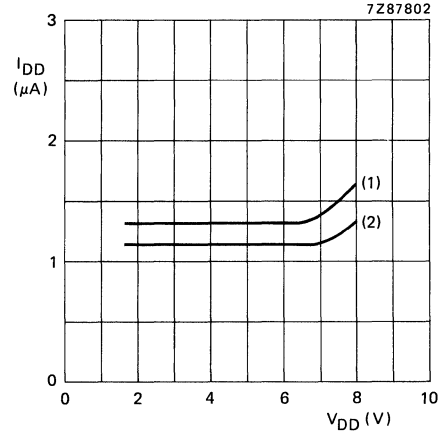
(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

Fig. 24 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C.



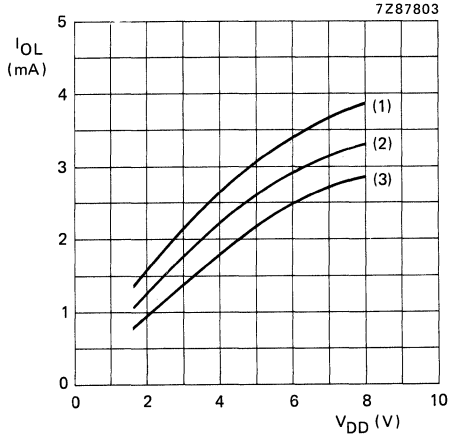
(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

Fig. 25 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); T_{amb} = 25 °C.



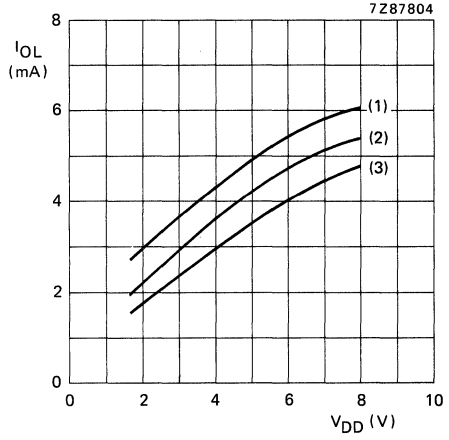
(1) T_{amb} = 70 °C
(2) T_{amb} = 25 °C

Fig. 26 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).



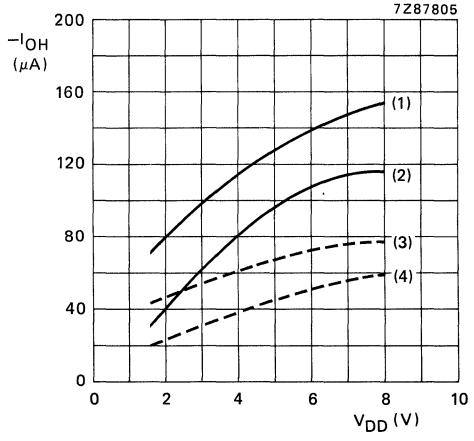
(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$
(3) $T_{amb} = 70\ ^{o}C$

Fig. 27 Output sink current LOW (I_{OL}), except outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); $V_O = 0,4$ V.



(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +70\ ^{o}C$

Fig. 28 Output current LOW (I_{OL}), outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); $V_O = 0,4$ V.



(1) $T_{amb} = 25\ ^{o}C$; $V_O = V_{SS}$
(2) $T_{amb} = 25\ ^{o}C$; $V_O = 0,9V_{DD}$
(3) $T_{amb} = 70\ ^{o}C$; $V_O = V_{SS}$
(4) $T_{amb} = 70\ ^{o}C$; $V_O = 0,9V_{DD}$

Fig. 29 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).

A.C. CHARACTERISTICS

Rise and fall times between 10 and 90% levels; C_L = 50 pF

parameter	symbol	at 70 °C max. value			unit
	V_{DD}	1,8	3,0	6,0	V
Fall time	t_f	200	100	70	ns
Rise time	t_r	200	100	80	ns

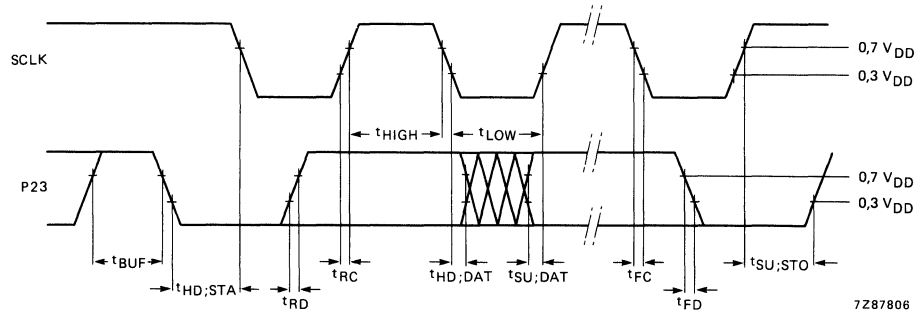


Fig. 30 PCD3343 timing requirements for the P23 and SCLK *input* signals.

Table 9 Input timing shown in figure 30

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SY;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1\ \mu s$
t_{RC}	$\leqslant 1\ \mu s$
t_{FD}	$\leqslant 1\ \mu s$
t_{FC}	$\leqslant 0{,}3\ \mu s$

Notes to Table 9

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
These figures apply to all modes.

A.C. CHARACTERISTICS (continued)

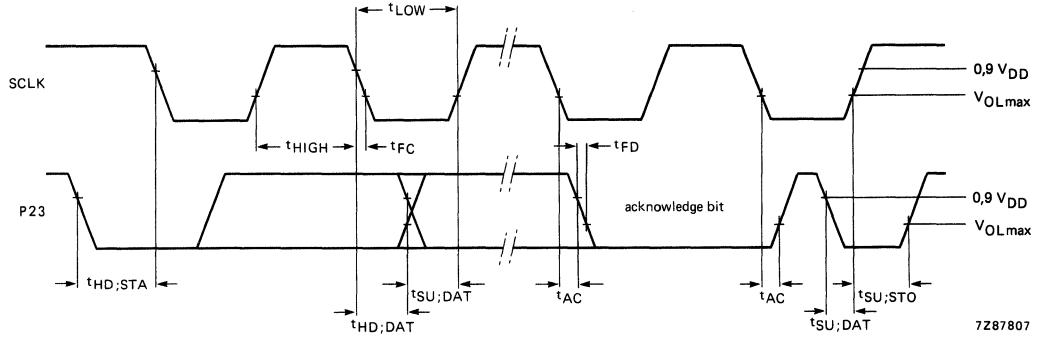


Fig. 31 PCD3343 timing requirements for the P23 and SCLK *output* signals.

Table 10 Output timing shown in figure 31

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	½ (DF + 9) t_{XTAL}	¾ (DF + 9) t_{XTAL}
t_{HIGH}	½ (DF) t_{XTAL}	¾ (DF) t_{XTAL}
t_{LOW}	½ (DF) t_{XTAL}	¼ (DF) t_{XTAL}
$t_{SU;STO}$	½ (DF − 3) t_{XTAL}	¼ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	– –
for DF $\leqslant$ 99	– –	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	– –
for DF > 99	–	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$	$\geqslant 9t_{XTAL}$
for DF $\leqslant$ 99	–	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$ $\leqslant$ 100 ns at C_b = 400 pF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$ $\leqslant$ 100 ns at C_b = 400 pF
t_{FD}, t_{FC}		

Notes to Table 10

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3343 is shown in figure 32. It comprises the following dedicated telephony IC's:

- TEA1060/1061 transmission circuit for telephony
- PCD3312 DTMF generator with Serial I/O
- PCE2111 or PCF8577 2 LCD drivers in LCD module MB7020160
- PCD8571 1 K RAM's with Serial I/O; the number of RAM's depends on the required amount of stored telephone numbers
- PCD3360/3361 programmable multi-tone ringer

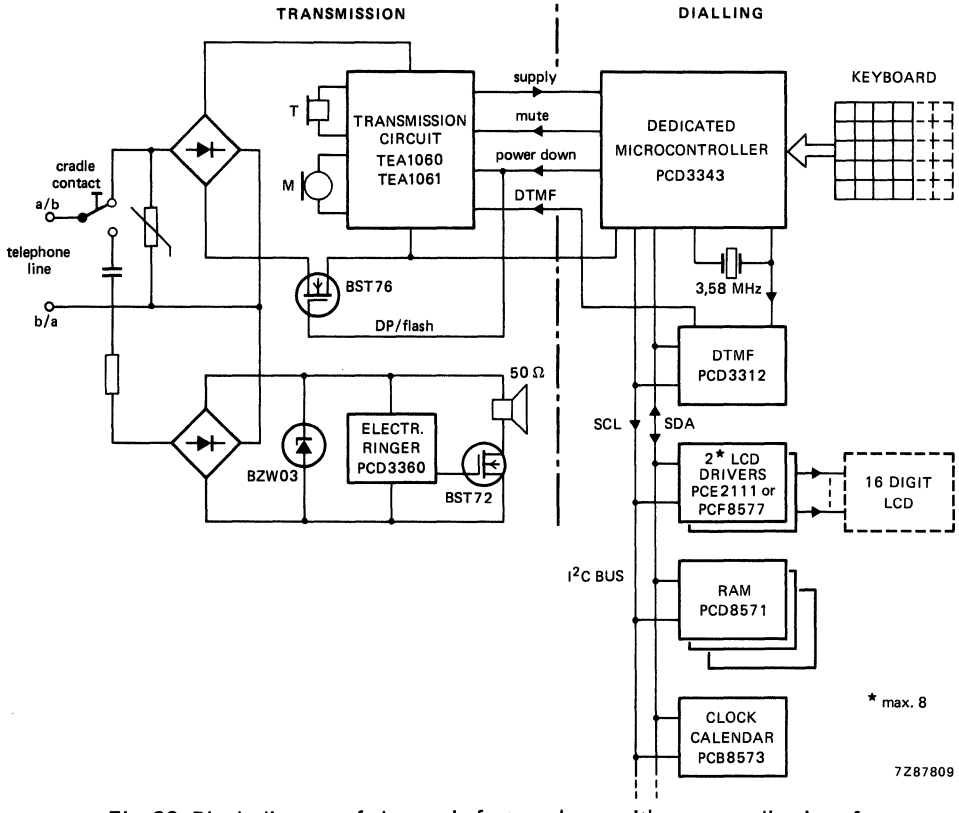


Fig. 32 Block diagram of electronic featurephone with common line interface.

A detailed application diagram of the PCD3343 with PCD3312 (DTMF), two PCD8571 (RAM) and two PCE2111 (LCD display drivers) is shown in figure 33.

Row 5 of the keyboard contains the following special keys:

- P program and autodial
- FL flash or register recall
- R redial or extended redial
- AP access pause

Row 6 contains the different diode options.

Columns 5 and 6 contain the button keys M0 to M9; single name keys for repertory telephone numbers.

APPLICATION INFORMATION (continued)

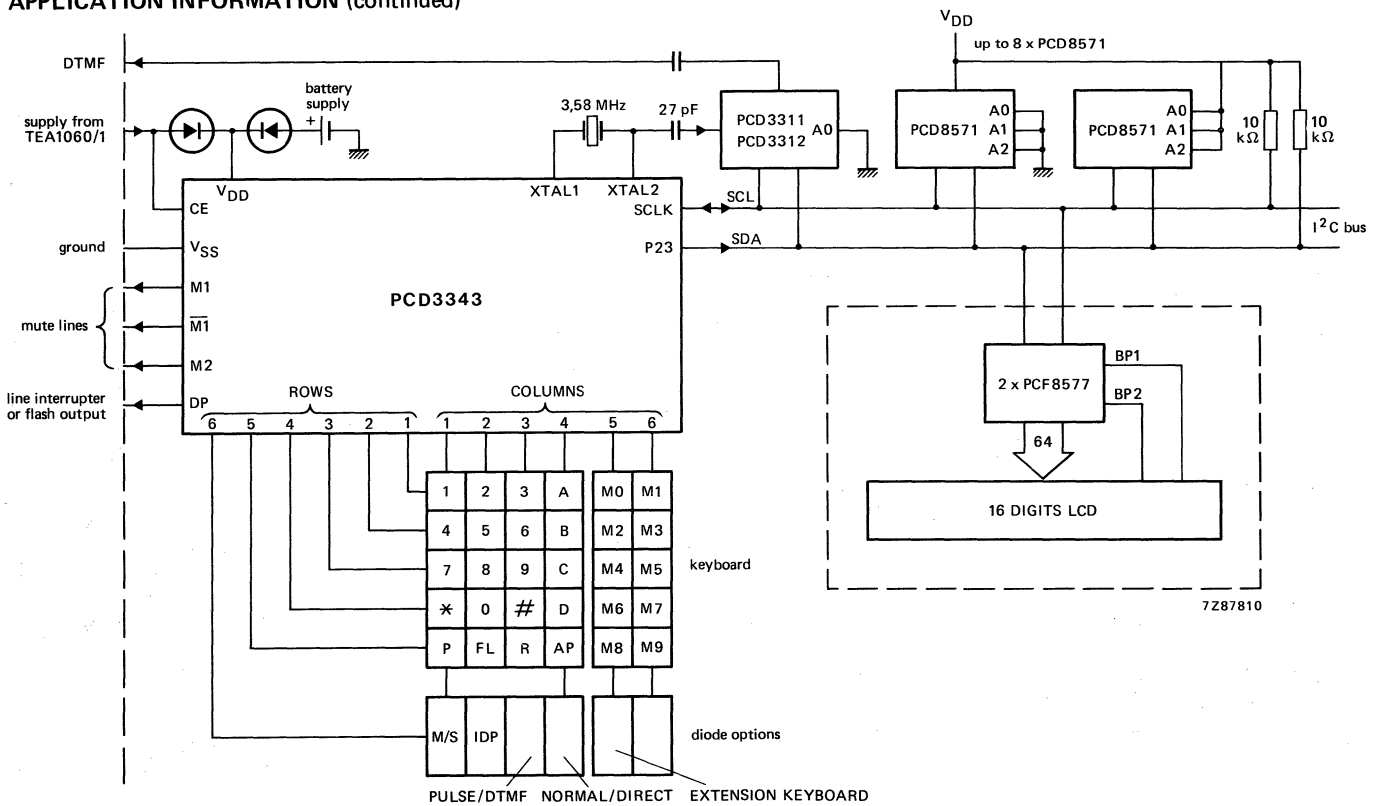


Fig. 33 Application diagram of PCD3343 for electronic featurephone with associated keyboard.

Additional information is available on request for the following:

- Serial I/O
- I^2C bus specification
- Interrupt logic
- Instruction set descriptions
- Software routines for an intelligent telephone set

Programmable Multi-Tone Telephone Ringer | PCD3360/61

GENERAL DESCRIPTION

The PCD3360/61 are CMOS integrated circuits, designed to replace the electro-mechanical bell in telephone sets. They meet most postal requirements, particularly with tone sequence possibilities and input frequency selectivity. Output signals for a loudspeaker or for a piezo-electric (PXE) transducer are provided. In the former application, no audio transformer is required since the loudspeaker is driven in class D.

Features

- Output signals for electro-dynamic transducer (loudspeaker) or for piezo-electric transducer (PXE)
- 7 basic frequencies (tones) and a pause
- 4 selectable tone sequences
- 4 selectable repetition rates
- 3 selectable impedance settings
- 3-step automatic swell } loudspeaker only
- Delta-modulated output signal that approximates a sinewave } loudspeaker only
- Input frequency discriminator with selectable upper and lower frequency limits
- Output for optical signal

5

Note

Tone sequences (up to 16 tones long), impedance settings and automatic swell levels are mask programmable for customized versions.

QUICK REFERENCE DATA

Available frequencies (tones)		533/600/667/800/ 1000/1067 and 1333 Hz
Number of intervals per tone sequence		15 or 16
Lower limits of frequency discriminator		13,33 or 20 Hz
Upper limits of frequency discriminator		30 or 60 Hz
Impedance settings (with 50 Ω loudspeaker)	approx.	7 or 10,5 or 17,5 kΩ
Switch-on delay at 25 Hz	max.	60 ms

PACKAGE OUTLINES

PCD3360P: 16-lead DIL; plastic (SOT-38).
PCD3361P: 8-lead DIL; plastic (SOT-97EE).
PCD3360T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).
PCD3361T: 8-lead mini-pack; plastic (SO-8L; SOT-176).

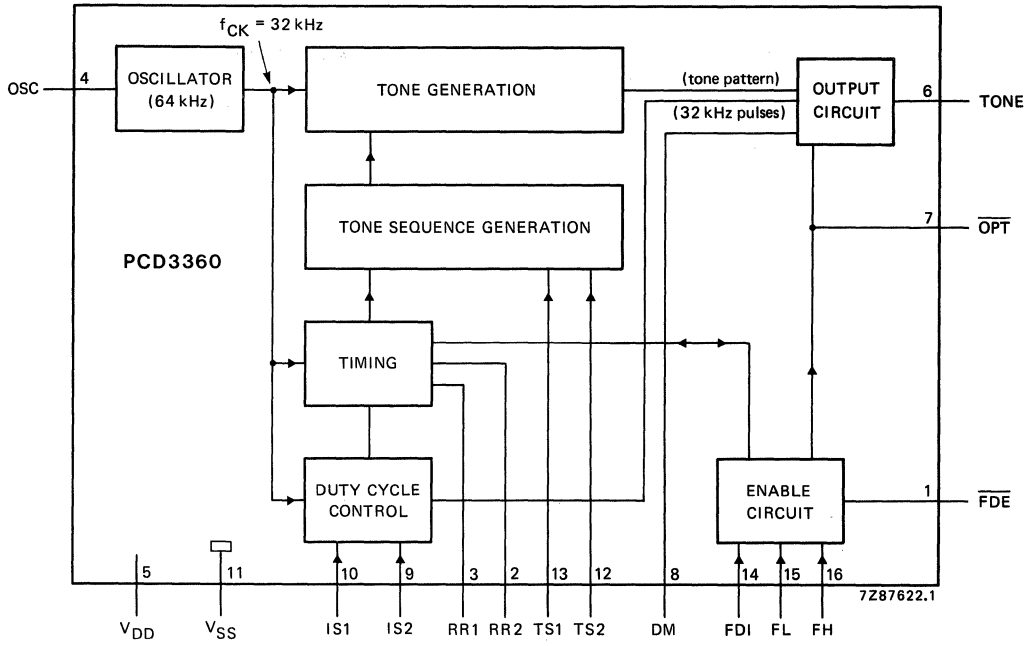


Fig. 1 Block diagram.

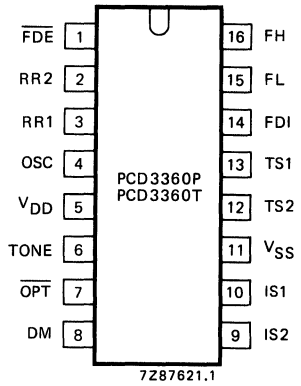


Fig. 2 Pinning diagram for PCD3360P and PCD3360T.

PINNING

1	$\overline{PDE}$	frequency descriminator enable
2	RR2	repetition rate selection
3	RR1	
4	OSC	oscillator
5	V_{DD}	positive supply
6	TONE	tone output
7	$\overline{OPT}$	optical signal output
8	DM	drive mode selection
9	IS2	impedance setting and automatic swell
10	IS1	
11	V_{SS}	negative supply
12	TS2	tone sequence selection
13	TS1	
14	FDI	frequency discriminator input
15	FL	lower frequency limit selection
16	FH	upper frequency limit selection

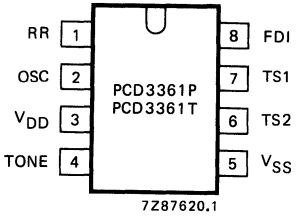


Fig. 3 Pinning diagram for PCD3361P and PCD3361T.

PINNING

1	RR	repetition rate selection
2	OSC	oscillator
3	V_{DD}	positive supply
4	TONE	tone output
5	V_{SS}	negative supply
6	TS2	tone sequence selection
7	TS1	
8	FDI	frequency discriminator input

Note

PCD3360 pins not available in the PCD3361 are at V_{SS}.

5

FUNCTIONAL DESCRIPTION (see Fig. 1)

Supply pins (V_{DD} and V_{SS})

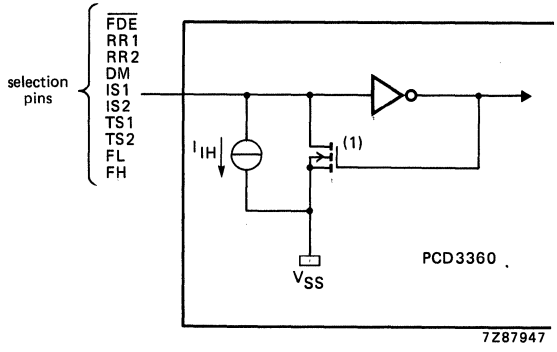
If the supply voltage (V_{DD}) drops below the standby voltage (V_{SB}), the oscillator and most other functions are switched off and the supply current is reduced to the standby current (I_{SB}). The automatic swell register retains its information until V_{DD} drops further to a value V_{AS} at which reset occurs.

Oscillator (OSC)

The 64 kHz oscillator is operated via an external resistor and capacitor connected to pin OSC. The oscillator signal is divided by two to provide the 32 kHz internal system clock.

Selection pins ($\overline{FDE}$, RR2, RR1, DM, IS2, IS1, TS2, TS1, FL and FH)

These pins are pulled down internally by a pull-down current I_{IH} when they are connected to V_{DD}, and by a pull-down resistance R_{IL} when they are connected to V_{SS} (see Fig. 4). Thus when the pins are open-circuit they are defined LOW. Therefore only a single-contact switch is required to connect the pins to V_{DD}; yet the supply current is only marginally increased as I_{IH} is very small.



(1) Transistor resistance = R_{IL} when switched on.

Fig. 4 Input circuit of selection pins.

Frequency discriminator circuit (pins $\overline{FDE}$ and FDI)

The frequency discriminator circuit prevents the ringer being activated by dial pulses, speech or other unqualified signals.

The circuit is enabled or disabled by input $\overline{FDE}$.

When $\overline{FDE}$ is HIGH, FDI acts as a logic enable input.
The circuit will produce tone sequences provided FDI is HIGH and V_{DD} exceeds V_{SB}.
When $\overline{FDE}$ is LOW, FDI acts as the frequency discriminator input.
The circuit will produce tone sequences provided V_{DD} exceeds V_{SB} and the signal at FDI fulfils the conditions set by FL and FH.

When the frequency discriminator is enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the circuit will start to produce tone sequences after two rising or two falling edges have occurred at FDI. The time between these edges must be within the limits set by FL and FH.

The circuit will continue to produce tone sequences provided the time between subsequent falling edges or between subsequent rising edges remains within the limits set by FL and FH, otherwise it will stop. Because two edges are required for detection, either positive or negative, the switch-on delay will vary between 1 and 1,5 cycles of the incoming ringing frequency.

FDI has a Schmitt-trigger action; the levels are set by an external resistor R2 (see Fig. 9) and an internal sink current that is switched from 20 μA (typ.) for FDI = LOW to $< 0{,}1$ μA for FDI = HIGH. Excess current entering FDI via R2 is absorbed by internal diodes clamped to V_{DD} and V_{SS}.

Selection of frequency discriminator limits (FL and FH)

With the frequency discriminator enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the lower and upper limits of the input frequency are set by inputs FL and FH as shown by Table 1 and Table 2 respectively.

Table 1 Selection of lower frequency discriminator limits (f_{osc} = 64 kHz)

FL input state	lower discriminator limit (Hz)
LOW	20
HIGH	13,33

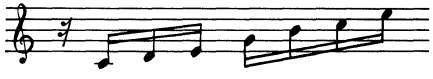
Table 2 Selection of upper frequency discriminator limits (f_{osc} = 64 kHz)

FH input state	upper discriminator limit (Hz)
LOW	60
HIGH	30

5

Selection of tone sequences (TS1 and TS2)

A tone sequence is composed of 15 or 16 equal time intervals. Each time interval may be filled with one of seven available tones or with a pause; these are shown together with their corresponding internal ROM tone code in Fig. 5.



tone key	–	c	d	e	g	b	c	e
frequency (Hz)	0	533	600	667	800	1000	1067	1333
frequency ratio		8	9	10	12	15	16	20
tone code	0	1	2	3	4	5	6	7

7Z87948

Fig. 5 Available tones and their corresponding internal ROM tone code.

FUNCTIONAL DESCRIPTION (continued)

Four tone sequences are programmed in the internal ROM (see Fig. 6). Inputs TS1 and TS2 determine which tone sequence is selected and output at pin TONE. The sequences are mask programmable with any length up to 16 time intervals.

The tone sequences are repeated continuously provided the enable conditions at inputs $\overline{FDE}$ and FDI are valid and $V_{DD} > V_{SB}$; the first sequence always starts with the first tone shown in Fig. 6.

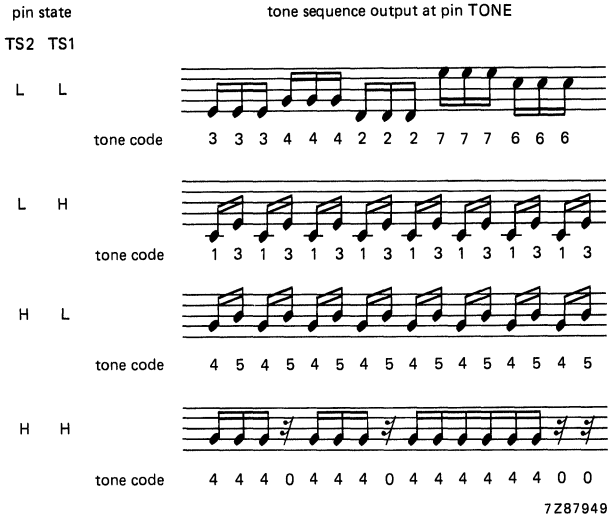


Fig. 6 Tone sequences mask-programmed in the PCD3360/61.

Selection of repetition rates (RR1 and RR2)

The duration of a time interval within a tone sequence is determined by the state of inputs RR1 and RR2 as shown in Table 3. The resultant variation of repetition rate acts as a distinguishing feature between adjacent telephones.

Table 3 Duration of time intervals (f_{osc} = 64 kHz)

input state		time interval
RR1	RR2	ms
L	L	15
L	H	30
H	L	45
H	H	60

The repetition rate variation can be extended by mask programming (for customer defined versions) the same tone combination for all 4 tone sequences, but with a different number of time intervals per tone. Thus the repetition rate can be selected from 16 values by inputs RR1, RR2, TS1 and TS2.

Drive mode selection (DM)

The output signal at pin TONE can be selected for application with electro-dynamic or piezo-electric transducers. An example of both signals, for a tone frequency of 667 Hz, is shown in Fig. 7.

Loudspeaker mode

In the loudspeaker mode (DM = LOW), pin TONE outputs a delta-modulated signal that approximates a sinewave sampled at a rate of 32 kHz. The output pulse duration is determined by pins IS1 and IS2. The resultant acoustic spectrum is aurally more acceptable and has greater penetration than a square wave spectrum because more power is concentrated at the fundamental frequency.

PXE mode

In the PXE mode (DM = HIGH), pin TONE outputs a square wave. In this mode the ringer impedance and sound pressure level are determined by the characteristics (e.g. the size) of the PXE transducer; inputs IS1 and IS2 are inactive.

Setting of impedance, sound pressure level and automatic swell (IS1 and IS2)

With DM = LOW (loudspeaker mode), inputs IS1 and IS2 determine the pulse duration of the output signal and thereby the d.c. resistance R_{xy} (seen at points x and y in Fig. 9) and also the Sound Pressure Level (SPL). The selection of 3 impedance settings and automatic swell is shown in Table 4.

Table 4 Setting of pulse duration and automatic swell (DM = LOW)

input state		function	ringing burst number (N)	pulse duration (μs)		R_{xy} (kΩ)	Z_I (kΩ)	SPL (dBr)
IS1	IS2			fund.	harm.			
			1	1,8	–	40	tbf	tbf
L	L	automatic	2	2,6	–	20	17,5	–4
		swell	> 2	3,9	1,6	5	7	0
L	H		–	2,6	–	20	17,5	–4
H	L	constant	–	3,6	–	10	10,5	tbf
H	H	level	–	5,0	–	5	7	0

Where:

1. Typical pulse duration values of the fundamental and harmonic frequencies are for f_{osc} = 64 kHz and f_{CK} = 32 kHz.
2. SPL is the relative Sound Pressure Level, and 0 dBr is defined as the SPL for IS1 = IS2 = HIGH.
3. Values of the d.c. resistance R_{xy}, bell impedance (Z_I) and SPL are valid for a value of input voltage V_I = 40 V_{rms} in Fig. 9.

FUNCTIONAL DESCRIPTION (continued)

Setting of impedance, sound pressure level and automatic swell

When pins IS1 and IS2 are both LOW, the circuit operates in the automatic swell mode. The SPL then increases in three steps so that the maximum level is reached for the third ringing burst.
Each time V_{DD} drops below V_{AS} the automatic swell register is reset and the next ringing burst is considered as N = 1 (see Table 4).
A buffer capacitor C3 (see Fig. 9) must hold $V_{DD} > V_{AS}$ during the time between two consecutive ringing bursts of a series.

For each of the other three combinations of pins IS1 and IS2 the pulse duration has a constant value. Thus the ringer can be designed so that the impedance represented at the telephone line will comply with postal requirements that vary in relation to parallel or series connections of more than one ringer.

To satisfy some applications, a harmonic signal is added to the fundamental frequency in the last step of the automatic swell mode. The pulses representing this harmonic signal are interleaved with the pulses of the fundamental signal (see Fig. 8). The difference in pulse duration shown in Table 4, is chosen so that the harmonic level is 10 dB below the fundamental level.
The harmonic frequency range is from 2 kHz to 3,2 kHz. The individual harmonic frequencies for the seven tone codes and the relative fundamental frequencies are shown in Table 5.

Table 5 Harmonic frequency in relation to tone code and fundamental frequency

tone code	frequency (Hz)	
	fundamental	harmonic
1	533	3200
2	600	2400
3	667	2667
4	800	3200
5	1000	2000
6	1067	2133
7	1333	2667

Using a single mask it is possible to program the following:–

- Addition of harmonics in all the other input states of IS1 and IS2
- All pulse duration values
- Other even harmonic frequencies.

Optical output ($\overline{OPT}$)

The $\overline{OPT}$ output is designed to drive an optical signal transducer or lamp. It is LOW when the ringer circuit is enabled and HIGH when the ringer circuit is disabled. This output can also be used to switch the transmitter ON and OFF in the base of a cordless telephone set.

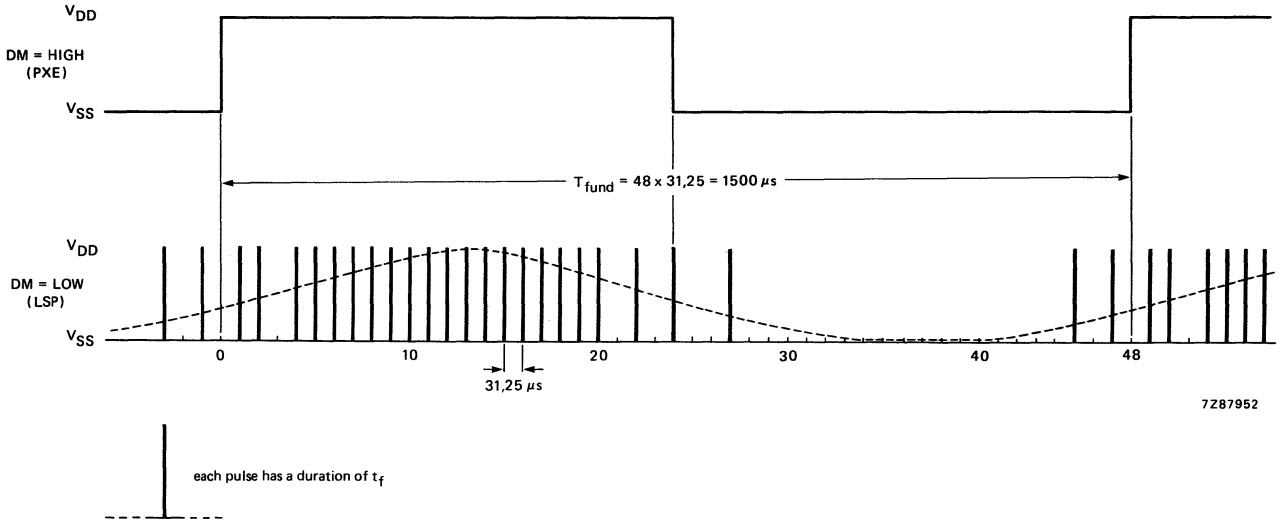


Fig. 7 Fundamental signal (667 Hz) at pin TONE
(for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

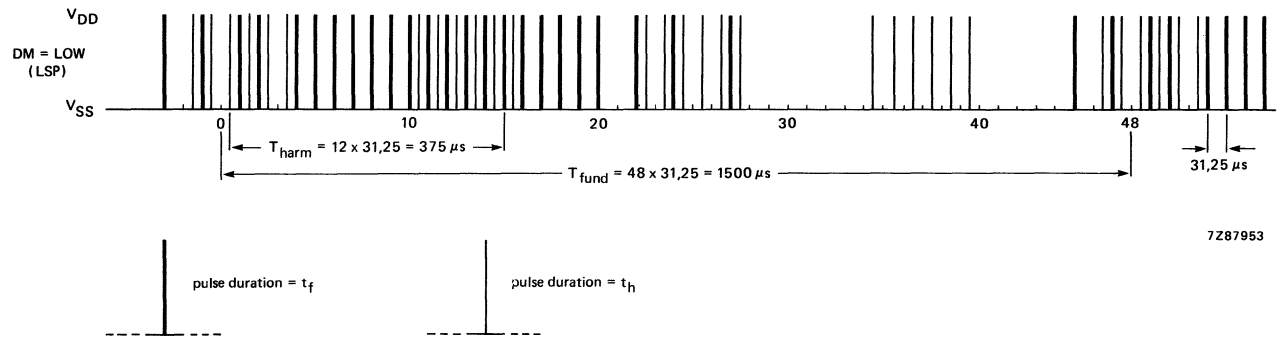


Fig. 8 Fundamental signal (667 Hz) + harmonic signal (2667 Hz) at pin TONE
(for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to + 9	V
Supply current	I_{DD}	max.	50	mA
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Total dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

D.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	V_{SB}+0,1	–	8,0	V
Standby supply voltage (note 1)	V_{SB}	tbf	4,8	5,7	V
Supply voltage for automatic swell reset (note 2)	V_{AS}	–	0,5V_{SB}	–	V
Operating supply current	I_{DD}	–	100	120	μA
Standby supply current at $V_{DD} < V_{SB}$ (note 3)	I_{SB}	–	4	8	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	0,3V_{DD}	V
Input voltage HIGH (any pin)	V_{IH}	0,7V_{DD}	–	V_{DD}	V
Pull-down circuits of inputs					
$\overline{FDE}$, RR1, RR2, DM, IS1, IS2, TS1, TS2, FL, FH					
pull-down resistance with input at V_{SS}	R_{IL}	–	20	–	kΩ
pull-down current with input at V_{DD}	I_{IH}	–	0,1	–	μA
Pull-down circuit of FDI					
pull-down current with V_{FDI} = 0,3V_{DD}	I_{SL}	tbf	20	tbf	μA
pull-down current with V_{FDI} = 0,7V_{DD}	I_{SH}	–	0,1	–	μA
pull-down current with $V_{DD} < V_{SB}$	I_{SX}	–	0,1	–	μA
Current into input FDI (note 4)	± I_{IS}	–	–	0,2	mA
Outputs					
TONE, $\overline{OPT}$					
Output sink current at V_{OL} = 0,5 V	I_{OL}	1	2	–	mA
Output source current at $V_{OH} = V_{DD}$−0,5 V	$-I_{OH}$	1	2	–	mA

Notes see next page.

A.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Switch-on delay (with $\overline{FDE}$ = LOW and ringing frequency within limits set by FL and FH)	$t_{d(on)}$	1	–	1,5	note 5
Switch-off delay (with $\overline{FDE}$ = LOW)					
at FL = LOW	$t_{d(off)}$	–	–	75	ms
at FL = HIGH	$t_{d(off)}$	–	–	112,5	ms
Oscillator frequency at R_{osc} = 365 kΩ; C_{osc} = 56 pF (note 6)	f_{osc}	tbf	64	tbf	kHz
Frequency variation at V_{DD} = 5,7 to 8,0 V	Δf_{osc}	–	–	1	%

Notes to the characteristics

1. For $V_{DD} < V_{SB}$ the circuit is in standby.
2. At $V_{DD} = V_{AS}$ the automatic swell register is reset.
3. The standby supply current is measured with all inputs and outputs open-circuit with the exception of OSC.
4. The current I_{IS} is clamped to V_{DD} and to V_{SS} by two internal diodes. Correct operation is ensured with $V_{FDI} > V_{DD}$ or $V_{FDI} < V_{SS}$, provided the maximum value of I_{IS} is not exceeded. (The input FDI has an extended HIGH and LOW input voltage range.)
5. The switch-on delay is measured in cycles of incoming ringing frequency.
6. Lead lengths of R_{osc} and C_{osc} to be kept to a minimum.

APPLICATION INFORMATION

Application of the PCD3360 in a telephone ringer circuit together with a loudspeaker is shown in Fig. 9.

The threshold levels V_H and V_L of the frequency discriminator circuit are determined by:

- The logic threshold of input FDI ($0{,}5V_{DD}$ typ. 3,4 V for V_{DD} = 6,8 V)
- The pull-down current of input FDI (20 μA typ. for FDI < 3,4 V)
- The value of R2 (680 kΩ in Fig. 9)

For a positive slope, the voltage at R2 must exceed the value V_H before FDI will become HIGH; V_H is the sum of the input threshold and the voltage drop across R2 thus:

$V_H = 3{,}4 + (680 \times 10^3) \times (20 \times 10^{-6}) = 17$ V.

For a negative slope, the voltage at R2 must decrease below the value V_L before FDI will become LOW. Because the current into FDI is negligible with FDI = HIGH the voltage drop across R2 can be discounted, thus V_L = 3,4 V.

The minimum operating voltage across C3 is 17,7 V which is determined by:

- The minimum operating voltage of the PCD3360 (5,7 V)
- The supply current of the PCD3360 (120 μA max.)
- The value of R2 (100 kΩ in Fig. 9)

The total switch-on delay equals approximately the time required to charge the supply capacitor C3 to the minimum operating value, plus the specified switch-on delay of the PCD3360.

The high operating voltage combined with the class D output stage ensures optimal energy conversion and thereby a high sound level. The design can easily be optimized for parallel or series connection of more than one ringer. The diode bridge, zener diode (D1) and resistor R1 protect the ringer against transients up to 5 kV. During these surges the voltage on the 68 V zener diode (BZW03) can rise to 100 V; the DMOS transistor BST72 (TR1) has a maximum drain-source voltage of 100 V. Up to 220 V, 50 Hz can be applied to the a/b terminals without damaging the ringer.
The choke (L1) in series with the 50 Ω loudspeaker increases the sound pressure level by approximately 3 dB by suppression of the 32 kHz carrier frequency and its sidebands.
The flyback diode BAX18A (D2) is a fast type with low forward voltage to obtain high efficiency.

Application of the PCD3360 together with a PXE transducer is shown in Fig. 10. The only significant difference between Fig. 9 and Fig. 10 is the output stage. Two BST72 transistors provide an output voltage swing almost equal to the voltage at C3. Pins IS1 and IS2 are inoperative because DM = HIGH. Volume control is possible using resistor R_V.

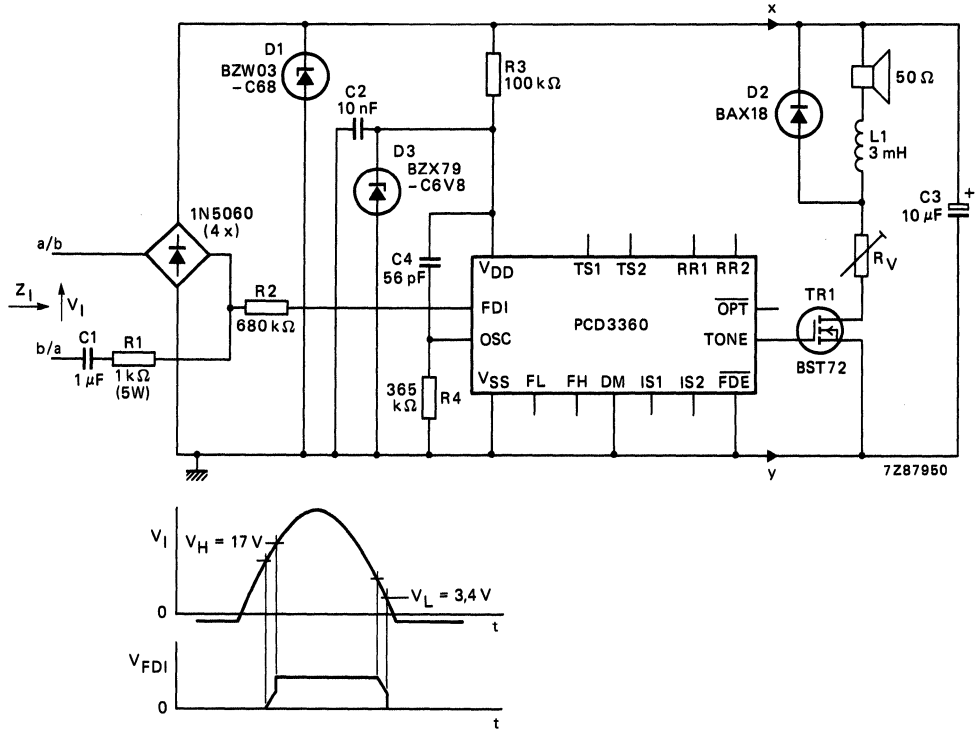


Fig. 9 Transformerless electronic ringer with PCD3360 and a loudspeaker.

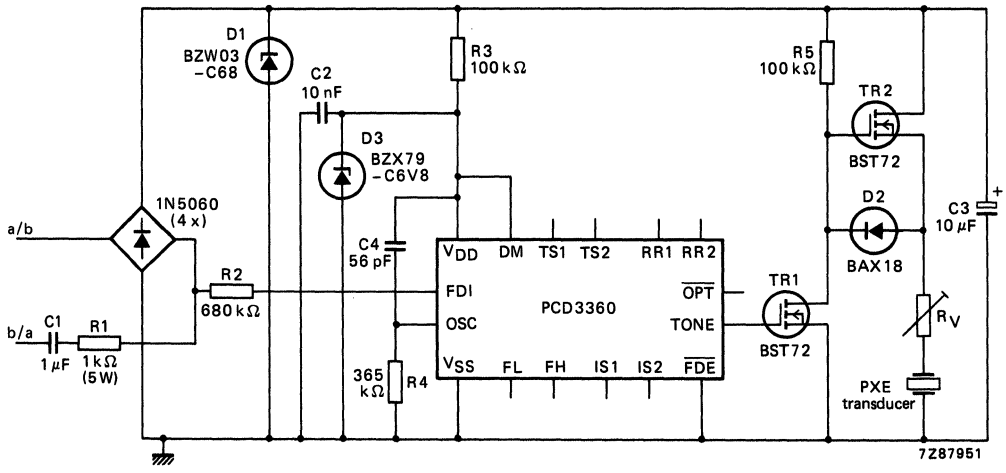


Fig. 10 PCD3360 ringer with PXE transducer.

Microcomputer Development System for MAB8400 PM4300/4337

DESCRIPTION

The PM4300 Microcomputer Instructor is a powerful tool for designing, prototyping, and debugging MAB8400 family-based, microcomputer systems. Such systems are built around the two-wire serial Inter-Integrated Circuit (I^2C) bus. Along with the PM4337 personality module, the Instructor can be used for writing and debugging programs in a target I^2C system. Features include hardware breakpoint, single-step with disassembly, automatic single-step, event timer, interrupt generation, and memory examination/editing capability. Complete access to all registers, flags, and I/O status information on each instruction can be viewed through the PM4300's LED display, or on a CRT display via the built-in RS232 interface.

The PM4300 Microcomputer Instructor is a completely self-contained system providing powerful emulation support for the I^2C bus system. Because the MAB8400 family instruction set is based on that of the 8048, MAB8400 programs can be developed and downloaded from a host with an 8048 assembler. Programs may also be entered via cassette or through the 'HEX' keyboard. Once entered, the operator can use commands to examine, change memory or registers, set breakpoints and single step. When program degubbing is finished, the built-in EPROM programmer transfer the program to a 2716 or 2732 EPROM. A piggyback MAB8400 may then be used to run the protype.

FEATURES

- **Complete low cost emulation support for the MAB8400 microcomputer.**
- **Manual or automatic single-stepping with disassembly.**
- **Direct communication link (RS232) to a host system (for editing and assembling).**
- **Complete access to ROM, RAM, registers and status bits.**
- **Interrupt handling.**
- **I/O exercising.**
- **LED or CRT display of HEX code, source code, memory, registers and status.**
- **Execution time measurements.**
- **Built-in test strip for hardware development.**
- **Built-in EPROM programmer.**
- **Personality modules available for most popular micro-processors.**

APPLICATIONS

The PM4300/4337 allows system designers to efficiently create and debug I^2C system hardware and software. The I^2C protocol allows for multiple masters to co-exist on a two-wire serial bus creating an efficient, cost-effective means for completely asynchronous serial communication between all controllers and peripherals on a single two-wire bus. The PM4300/4337 can be used to develop I^2C system in such application as:

- **Feature phones**
- **Television controllers**
- **Automative consoles**
- **Self-Aligning circuitry**
- **Control systems**
- **Any system which can benefit from the hardware simplicity of the I^2C bus.**

5

Transmission Interface with Loudspeaking Facility

TEA1042

GENERAL DESCRIPTION

The TEA1042 is a bipolar integrated circuit performing all speech and line interface functions in electronic telephone sets. It is especially designed for handsfree loudspeaking equipment.

Its features are:

- Supplied from telephone line current
- Voltage regulator with adjustable d.c. voltage drop and d.c. resistance
- High and low-impedance handset microphone inputs
- High-impedance base microphone input
- Handset/base selection input
- Muting input for pulse or DTMF dialling
- Gain setting facility on all amplifiers
- Line current dependent gain control facility with corrections for the exchange supply voltage and its feeding bridge resistance
- Supply output for additional circuits.

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{line}	typ.	4,2 V
Line current operating range	I_{line}		10 to 140 mA
Telephone line impedance	$\|Z_{line}\|$	nom.	600 Ω
Supply current	I_{CC}	typ.	1 mA
Voltage gain, transmitting amplifier			
MIC1 input	A_{vd}	typ.	44,1 dB
MIC2 input	A_{vd}	typ.	20 dB
MIC3 input	A_{vd}	typ.	20 dB
DTMF input	A_{vd}	typ.	25,6 dB
Voltage gain, receiving amplifier	A_{vd}	typ.	27 dB
Gain adjustment range			
transmitting amplifier	ΔA_{vd}	typ.	± 6 dB
receiving amplifier	ΔA_{vd}	typ.	± 8 dB
Range of gain control with line current, all amplifiers	ΔA_{vd}	typ.	6 dB
Exchange supply voltage range	V_{exch}		24 to 60 V
Exchange feeding bridge resistance	R_{exch}		400 or 800 Ω
Operating ambient temperature range	T_{amb}		−25 to + 70 °C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

Transmission Interface with Loudspeaking Facility

TEA1042

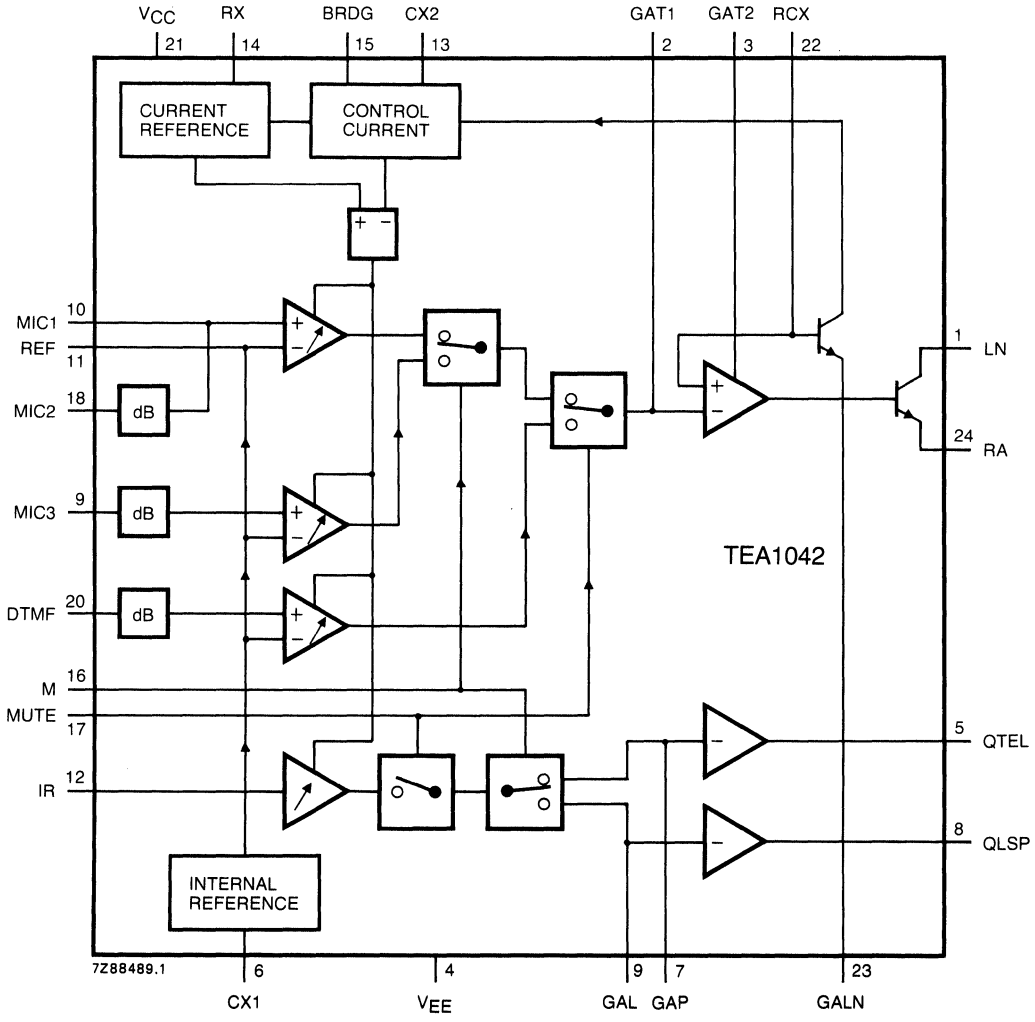


Fig. 1 Block diagram. The blocks marked dB are attenuators. The M and MUTE inputs operate analogue switches that activate or inhibit the inputs and outputs as required by their function.

Transmission Interface with Loudspeaking Facility

TEA1042

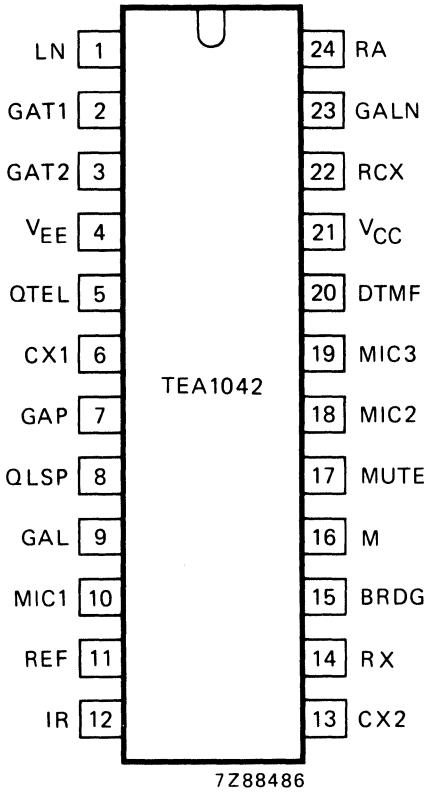


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAT1	gain adjustment; transmitting amplifier
3	GAT2	gain adjustment; transmitting amplifier
4	V_{EE}	negative line terminal
5	QTEL	handset telephone output
6	CX1	reference decoupling
7	GAP	gain adjustment; telephone amplifier
8	QLSP	loudspeaker preamplifier output
9	GAL	gain adjustment; loudspeaker preamplifier
10	MIC1	low-impedance handset microphone input
11	REF	reference voltage
12	IR	receiving amplifier input
13	CX2	external stabilizing capacitor
14	RX	external resistor
15	BRDG	selection input for gain control adaptation to feeding bridge impedance
16	M	mode (handset/base selection) input
17	MUTE	mute input
18	MIC2	high-impedance handset microphone input
19	MIC3	base microphone input
20	DTMF	dual-tone multi-frequency input
21	V_{CC}	positive supply
22	RCX	line voltage adjustment and voltage regulator decoupling
23	GALN	gain control with line current; all amplifiers
24	RA	d.c. resistance adjustment

FUNCTIONAL DESCRIPTION

The TEA1042 contains two receiving amplifiers, a transmitting amplifier, means to switch the inputs and the outputs, means to adjust the gain of all amplifiers individually, means to vary the gain with the line current and means to adjust the d.c. voltage drop and d.c. resistance. See the block diagram, Fig. 1.

Supply: LN, V_{CC}, V_{EE}, RA, CX1 and CX2 (pins 1, 21, 4, 24, 6 and 13)

The circuit is supplied from the line current, the arrangement is shown in Fig. 3. The circuit develops its own supply voltage at V_{CC} (pin 21). This supply voltage may also be used to supply an external circuit, e.g. a CMOS pulse or DTMF dialler or an electret microphone amplifier stage. The current available for this circuit depends on external components, see Fig. 4.

All line current has to flow through the circuit. If the line current exceeds the current required by the circuit itself via V_{CC} (pin 21), i.e. about 1 mA, plus the current required by the peripheral circuits connected to this pin, then the excess current is diverted via LN, the positive line terminal (pin 1), to RA (d.c. resistance adjustment; pin 24).

The minimum line voltage may be chosen by external resistor R5 and the variation with line current by external resistor R10. The circuit regulates the line voltage at T_{amb} = 25 °C to:

$$V_{line} = V_{LN} = \frac{R5 + R9}{R9} \times 0{,}62 + I_{LN} \times R10,$$

I_{LN} being the current diverted via LN.

A regulator decoupling capacitor has to be connected between RCX (pin 22) and V_{EE}, the negative line terminal (pin 4), a smoothing capacitor has to be connected between V_{CC} (pin 21) and V_{EE}, and a stabilizing capacitor between CX2 (pin 13) and V_{EE}. Further a decoupling capacitor has to be connected between CX1 (reference decoupling; pin 6) and V_{EE} (pin 4).

The dynamic impedance that the circuit presents to the line in the speech band is determined primarily by resistor R1 connected between LN (pin 1) and V_{CC} (pin 21).

Mode (handset/base selection) input M (pin 16)

The mode input permits selection of operation via the handset or via the base. A HIGH level on the M input or an open circuit selects handset operation, i.e. it activates the microphone inputs MIC1 and MIC2 and the handset telephone output QTEL. A LOW level on M selects the base microphone input MIC3 and the loudspeaker preamplifier output QLSP.

Microphone inputs MIC1, MIC2 and MIC3 (pins 10, 18 and 19)

Handset and base may be equipped with a sensitive microphone, e.g. an electret microphone with pre-amplifier. This has to be connected to the MIC2 or MIC3 input respectively. The available gain from these inputs is typ. 20 dB.

The handset may also be equipped with an insensitive low-impedance microphone, e.g. a dynamic or magnetic microphone. This has to be connected between MIC1 (pin 10) and (REF (pin 11). The available gain from this input is typ. 44,1 dB.

Dual-tone multi-frequency input DTMF and mute input MUTE (pins 20 and 17)

A HIGH level on the MUTE input inhibits all microphone inputs and the telephone and loudspeaker outputs QTEL and QLSP and enables the DTMF input, a LOW level does the reverse. Switching the MUTE input will not produce any clicks on the line or in the telephone or loudspeaker. The available gain from the DTMF input is typ. 25,6 dB.

Telephone output QTEL and loudspeaker preamplifier output QLSP (pins 5 and 8)

As described before, the M input determines which of the outputs QTEL and QLSP will be activated. The receiving amplifier input IR (pin 12) is the input for both outputs. For both outputs the available gain is typ. 27 dB. The output QTEL is intended for telephone capsules with an impedance of 150 Ω or more. The QLSP output is intended to drive a power amplifier. Its output impedance is less than 1 kΩ.

Gain adjustment: GAT1, GAT2, GAP and GAL (pins 2, 3, 7 and 9)

The gain of the transmitting amplifier may be adjusted by an external resistor R2 connected between GAT1 and GAT2 (pins 2 and 3; see Fig. 9). This adjustment influences the sensitivity of the inputs MIC1, MIC2, MIC3 and DTMF to the same amount. The gain is proportional to R2 and inversely proportional to R10 and R12.

The gain of the telephone amplifier may be adjusted by an external resistor R14 between GAP (pin 7) and CX1 (pin 6). The gain is proportional to R14 and inversely proportional to R12.

The gain of the loudspeaker preamplifier may be adjusted by an external resistor R13 between GAL (pin 9) and CX1 (pin 6). The gain is proportional to R13 and inversely proportional to R12.

Gain control with line current: GALN (pin 23)

The circuit offers a facility to automatically vary the gain of all its amplifiers with the line current. In this way the circuit compensates for differences in line attenuation. The variation is accomplished by connecting an external resistor R11 between GALN (pin 23) and V_{EE} (pin 4). The value of this resistor should be chosen in accordance with the supply voltage of the exchange (see Figs 5 and 6).

If no gain variation with line current is required the GALN connection may be left open. All amplifiers have their maximum gain then.

Selection input for gain control adaptation to feeding bridge impedance: BRDG (pin 15)

A LOW level at the BRDG input optimizes the gain control characteristics of the circuit for a 400 Ω feeding bridge in the exchange, a HIGH level for 800 Ω.

Side tone suppression

In the circuit diagram shown in Fig. 9 side tone suppression is obtained with components C2, R3, R4, R7 and R8. Their component values have to be chosen to suit the cable type used. This network attenuates the signal from the telephone line to the IR input of the receiving amplifier. This attenuation may be adjusted by choosing the value of R7 without affecting the side tone suppression.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current			
d.c.	I_{line}	max.	140 mA
non-repetitive ($t < 100$ h)	I_{line}	max.	250 mA
Storage temperature range	T_{stg}	−40 to +125	°C
Operating ambient temperature range	T_{amb}	−25 to +70	°C
Junction temperature	T_j	max.	150 °C

CHARACTERISTICS

I_{line} = 10 to 140 mA; f = 1000 Hz; T_{amb} = 25 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 21)					
Line voltage					
I_{line} = 15 mA	V_{line}	4	4,2	4,4	V
I_{line} = 50 mA	V_{line}	–	–	5,8	V
I_{line} = 100 mA	V_{line}	–	–	7,3	V
Variation with temperature	$-\Delta V_{line}/\Delta T$	8	10	12	mV/K
Line current operating rage	I_{line}	10	–	140	mA
Supply current at V_{CC} = 2 V	I_{CC}	–	–	1	mA
Mode (handset/base selection) input M (pin 16)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{16}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Low-impedance handset microphone input MIC1 and reference voltage pin REF (pins 10 and 11)					
Input impedance	$\lvert Z_{10\text{-}11}\rvert$	–	3	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	43,1	44,1	45,1	dB
High-impedance handset microphone input MIC2 (pin 18)					
Input impedance	$\lvert Z_{18\text{-}4}\rvert$	40	48	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	19	20	21	dB
Base microphone input MIC3 (pin 19)					
Input impedance	$\lvert Z_{19\text{-}4}\rvert$	40	48	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	19	20	21	dB
DTMF input (pin 20)					
Input impedance	$\lvert Z_{20\text{-}4}\rvert$	10	15	–	kΩ
Voltage gain, see Fig. 7	A_{vd}	24,6	25,6	26,6	dB
Gain adjustment pins; transmitting amplifier: GAT1 and GAT2 (pins 2 and 3)					
Gain adjustment range	ΔA_{vd}	–	±6	–	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	±0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	±0,5	–	dB

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CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Transmitting amplifier output LN (pin 1)					
Output voltage at I_{line} = 15 mA; R_{line} = 600 Ω; d = 2%	$v_{LN(rms)}$	1,4	–	–	V
Psophometrically weighted* noise output voltage at I_{line} = 15 mA; R_{line} = 600 Ω	$v_{LN(rms)}$	–	245	–	μV
MUTE input (pin 17)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{17}$	–	8	20	μA
Attenuation of non-selected signals	$-\Delta A_{vd}$	45	–	–	dB
Receiving amplifier input IR (pin 12)					
Input impedance	$\lvert Z_{12\text{-}4}\rvert$	–	10	–	kΩ
Telephone output QTEL (pin 5)					
Voltage gain at I_{line} = 15 mA; R_{load} = 150 Ω; R13 = 15 kΩ; see Fig. 8	A_{vd}	26	27	28	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	±0,5	–	dB
Gain variation with temperature at I_{line} = 50 mA; T_{amb} = −5 to +45 °C	ΔA_{vd}	–	±0,5	–	dB
Maximum output voltage at I_{line} = 15 mA; R_{load} = 150 Ω; d = 2%	$v_{O(rms)}$	350	–	–	mV
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Gain adjustment pin; telephone amplifier: GAP (pin 7)					
Gain adjustment range	ΔA_{vd}	–	±8	–	dB
Loudspeaker preamplifier output QLSP (pin 8)					
Voltage gain at I_{line} = 15 mA; R_{load} = 10 kΩ; R14 = 15 kΩ; see Fig. 8	A_{vd}	–	27	–	dB
Gain variation with frequency, f = 300 to 4000 Hz	ΔA_{vd}	–	±0,5	–	dB
Gain variation with temperature	ΔA_{vd}	–	±0,5	–	dB
Psophometrically weighted* noise output voltage at I_{line} = 15 mA	$v_{O(rms)}$	–	40	–	μV
Output impedance	$\lvert Z_{8\text{-}4}\rvert$	–	–	1	kΩ
Gain adjustment pin; loudspeaker preamplifier: GAL (pin 9)					
Gain adjustment range	ΔA_{vd}	–	±8	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Selection input for gain control adaptation to feeding bridge impedance BRDG (pin 15)					
Input voltage					
HIGH level	V_{IH}	1	–	V_{CC}	V
LOW level	V_{IL}	0	–	0,2	V
Input current	$-I_{15}$	–	8	20	μA
Gain control with line current pin GALN (pin 23)					
Gain control range	ΔA_{vd}	–	6	–	dB
Highest line current for maximum gain, R11 = 105 kΩ;					
BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	22,5	25	27,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	31,5	35	38,5	mA
Lowest line current for minimum gain, R11 = 105 kΩ;					
BRDG = HIGH (R_{exch} = 800 Ω)	I_{line}	49,5	55	60,5	mA
BRDG = LOW (R_{exch} = 400 Ω)	I_{line}	81	90	99	mA

* P53 curve.

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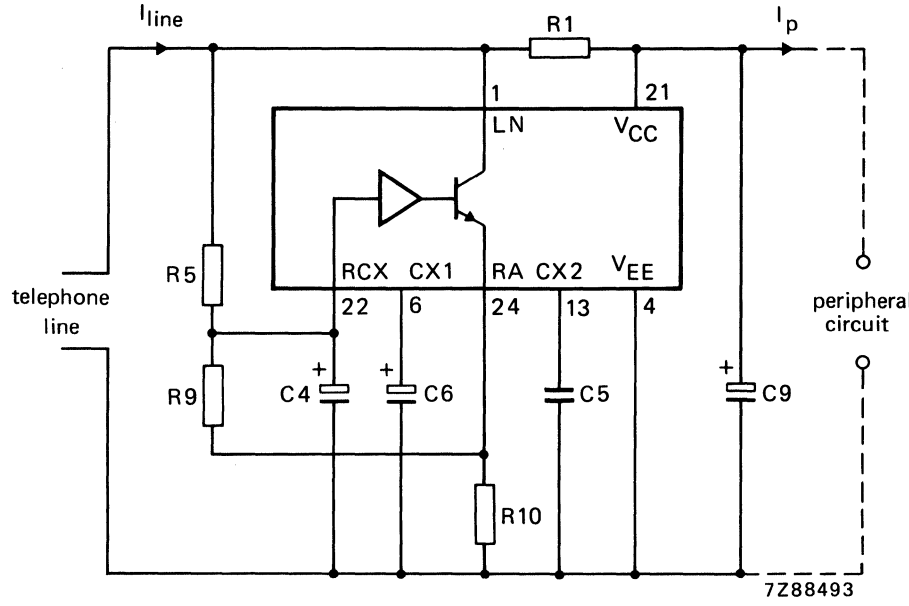

Fig. 3 Supply arrangement.

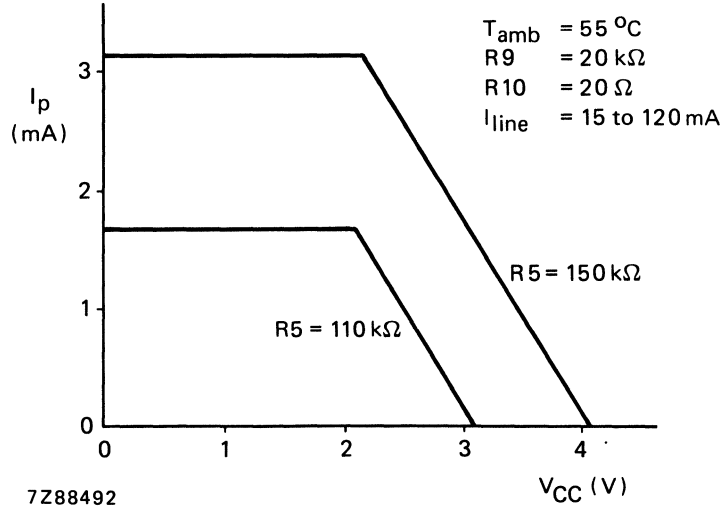

Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuits.

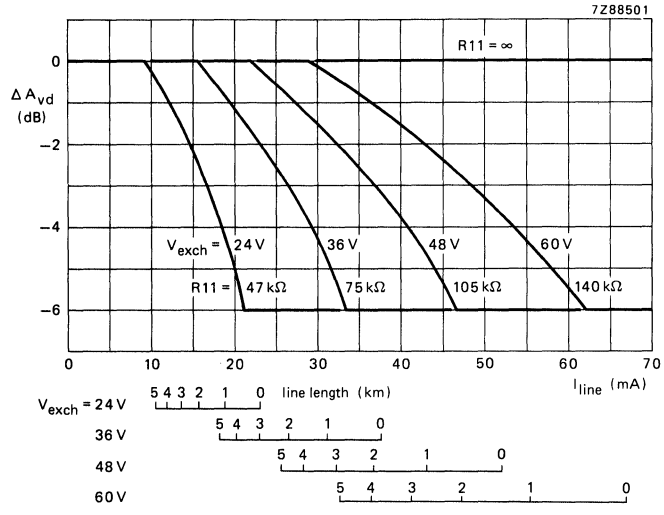

Fig. 5 Gain variation with line current, with R11 as a parameter, and with the BRDG input HIGH, i.e. the circuit optimized for 800 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

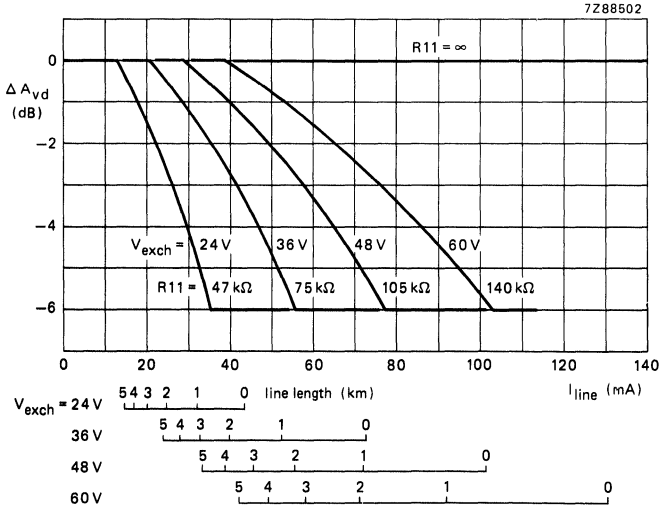

Fig. 6 Gain variation with line current, with R11 as a parameter, and with the BRDG input LOW, i.e. the circuit optimized for 400 Ω. The values chosen for R11 suit the usual values for the supply voltage of the exchange. The curves are valid for 0,5 mm twisted-pair cables with an attenuation of 1,2 dB/km and a d.c. resistance of 176 Ω/km.

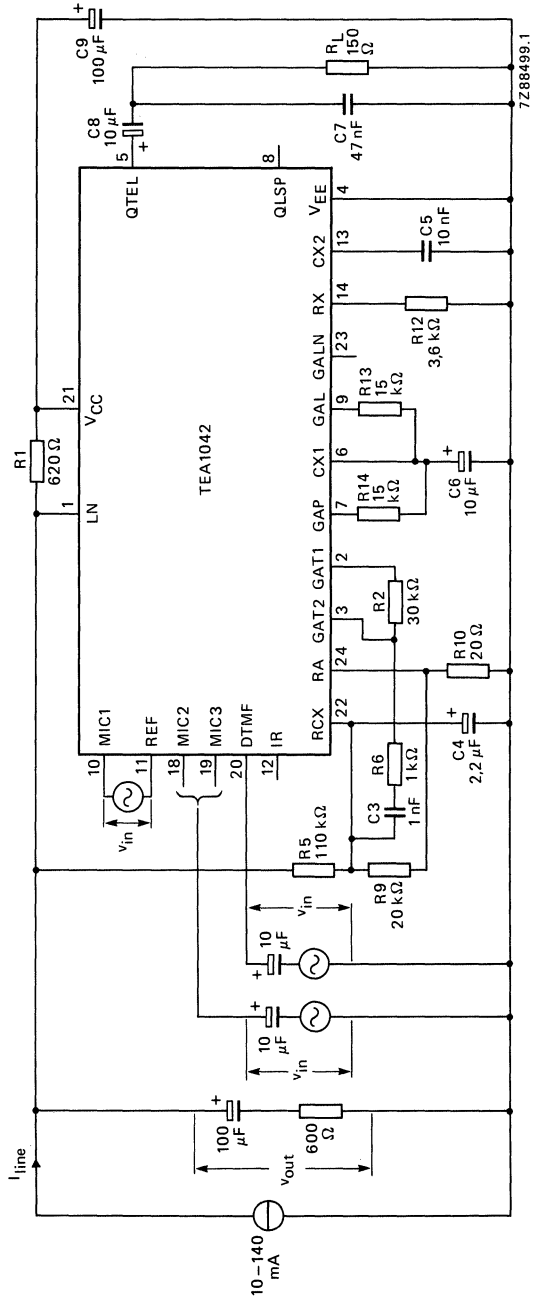

Fig. 7 Test circuit for defining voltage gain of MIC1, MIC2, MIC3 and DTMF inputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the MIC1 or MIC2 input the M input should be HIGH and the MUTE input LOW, for measuring the MIC3 input M and MUTE should both be LOW and for measuring the DTMF input M and MUTE should be HIGH. Inputs not under test should be open.

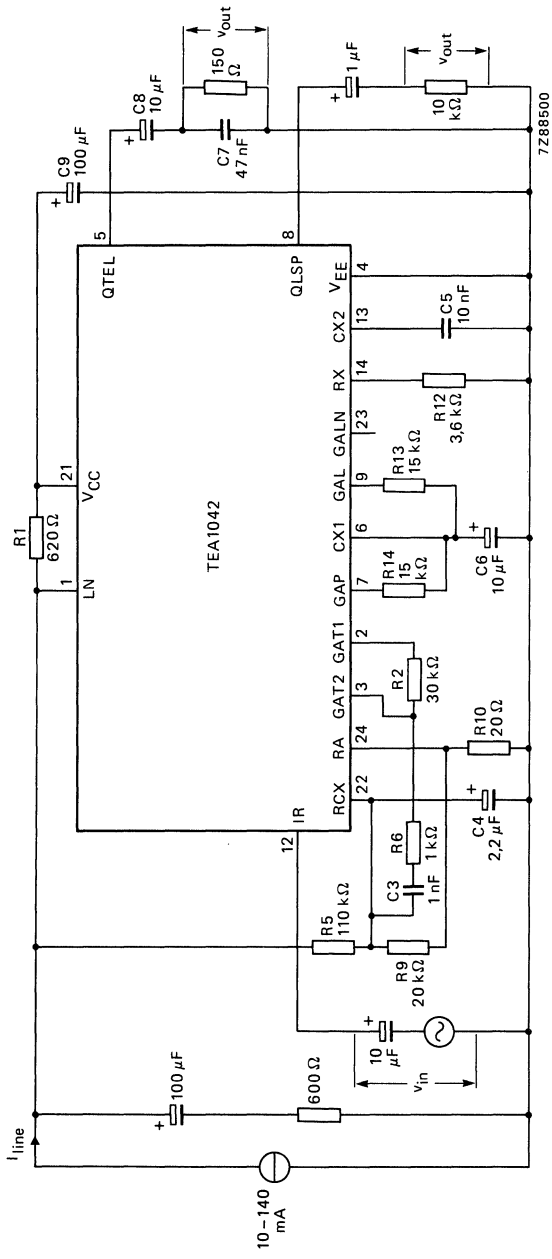

Fig. 8 Test circuit for defining voltage gain of QTEL and QLSP outputs. Gain is defined as: $A_{vd} = 20 \log |v_{out}/v_{in}|$. For measuring the QTEL output the M input should be HIGH and the MUTE input LOW, for measuring the QLSP output M and MUTE should both be LOW.

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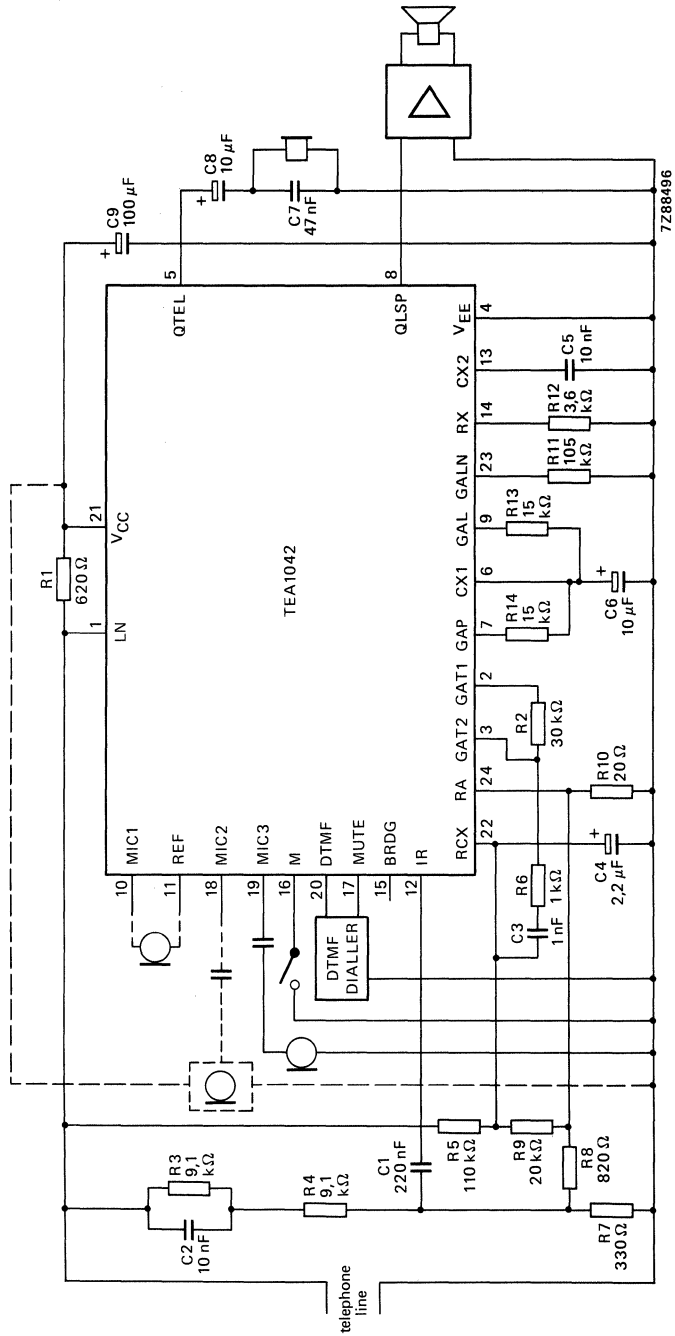


Fig. 9 Typical application of the TEA1042 in an electronic handsfree telephone set. The connections to the MIC1 and MIC2 inputs are alternatives. The connection to the BRDG input is not shown, see the Functional Description. The diagram does not show voice switches and associated control circuits required in a practical circuit for stable loudspeaking operation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

Transmission Interface with DTMF TEA1046

This integrated circuit is a dual-tone multi-frequency (DTMF) generator and a speech transmission circuit on a single chip. It supplies frequency combinations in accordance with CCITT recommendations for use in push-button telephones. It can be operated with a single contact keyboard or via a direct interface with a microcomputer. I^2L technology allows digital and analogue functions to be implemented on the same chip.

The speech-transmission part incorporates microphone and telephone amplifiers, anti-sidetone and line adaption. The microphone inputs, suitable for different types of transducers, are symmetrical to allow long cable connections with good immunity against radio-frequency interferences.

The logic inputs contain an interface circuit to guarantee well defined states and on and off resistance of the keyboard contacts.

The circuit features:
- stabilized DTMF levels to be set externally
- wide operating range of line current and temperature
- no individual DTMF level adjustments required
- microcomputer compatible logic inputs
- gain setting for microphone and receiver amplifiers
- internally generated electronic muting
- low spreads on amplifier gains
- low number of external components

5

QUICK REFERENCE DATA

Line voltage	V_L	typ. 4.8	V
Line current	I_L	10 to 120	mA
Adjustable dynamic resistance	R_i	600 to 900	Ω
Microphone signal amplification	A_M	typ. 50	dB
Telephone signal amplification	A_T	typ. 20	dB
DTMF tone levels (adjustable)			
lower frequency	V_{LG}	max. −6	dBm
higher frequency	V_{HG}	max. −4	dBm
Operating temperature range	T_{amb}	−25 to + 85	°C

PACKAGE OUTLINES

TEA1046P : 24-lead DIL, plastic (SOT-101).
TEA1046D: 24-lead DIL, ceramic (SOT-149).

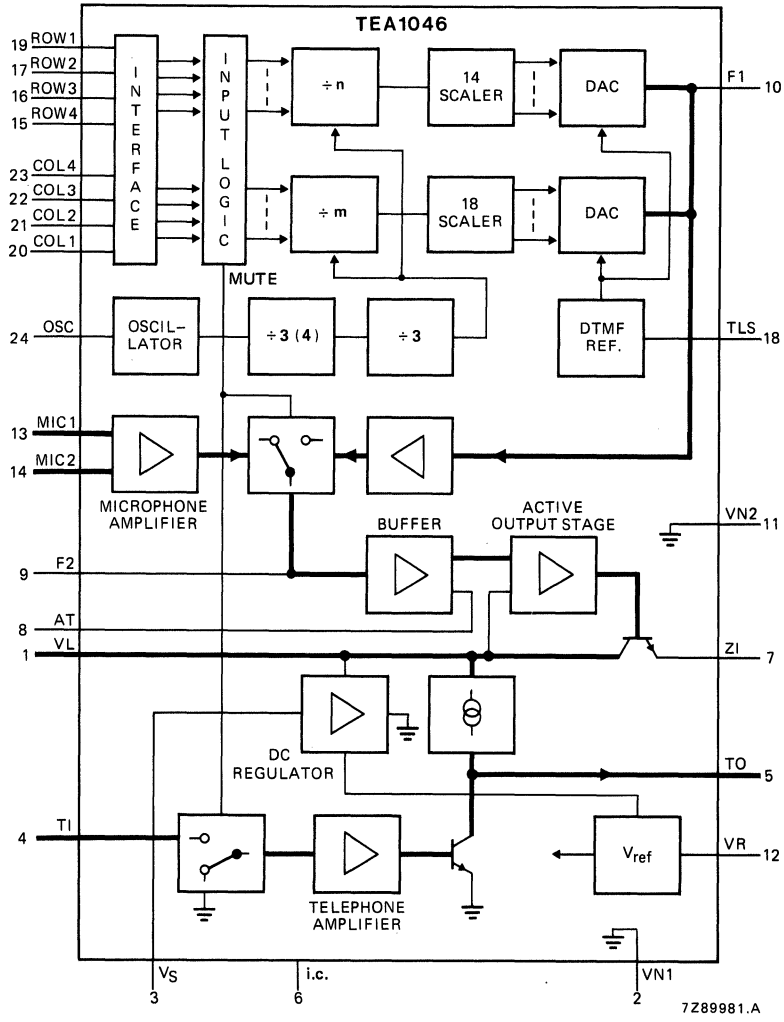


Fig. 1 Functional block diagram.

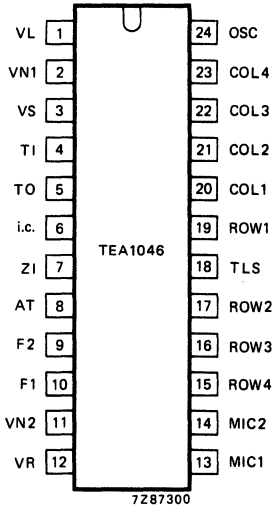


Fig. 2 Pinning diagram.

PINNING

1	VL	positive line-voltage
2	VN1	negative line-voltage
3	VS	voltage stabilizer filter
4	TI	telephone amplifier input
5	TO	telephone amplifier output
6	i.c.	internally connected
7	ZI	impedance setting input
8	AT	anti-sidetone output
9	F2	second filter
10	F1	first filter
11	VN2	negative line voltage
12	VR	reference voltage output
13	MIC1	microphone input (pos.)
14	MIC2	microphone input (neg.)
15	ROW4	row input 941 Hz/BCD input
16	ROW3	row input 852 Hz/BCD input
17	ROW2	row input 770 Hz/BCD input
18	TLS	DTMF level setting
19	ROW1	row input 697 Hz/BCD input
20	COL1	column input 1209 Hz/mute input
21	COL2	column input 1336 Hz/mute input
22	COL3	column input 1477 Hz/enable input
23	COL4	column input 1633 Hz/mute input
24	OSC	oscillator input

5

FUNCTIONAL DESCRIPTION

Voltage regulator (Fig. 3)

Different line lengths and feeding bridge resistances of the exchange cause a large line current range to supply this circuit. As all functions on this chip are working within a total current of 10 mA, the rest of the line current is shunted by the voltage regulator circuit. It regulates the voltage drop over the circuit on a nominal level of 4.8 V.

The capacitor connected to input VS provides a low-pass filter function to avoid influence of the audio signals on the line.

The static behaviour of the voltage regulator is expressed by:

$$V_L = V_o + (I_L - I_i)\ R13$$

where V_o = 4.8 V at T_a = 25 °C and R13 = 5 Ω, I_i = 10 mA.

The dynamic impedance of the regulator is equivalent to a resistor in series with a simulated inductor:

$$Zr\ (\omega) = R_{eq} + j\omega L_{eq}$$

where R_{eq} = R13 = 5 Ω
$L_{eq} \approx 5$ H (C_{VS} = 68 μF).

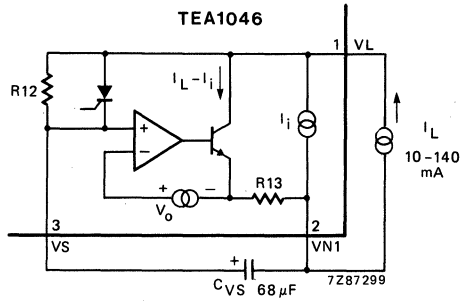


Fig. 3 Voltage regulator principle.

By connecting a resistor parallel to R12 the d.c. level (V_L) can be decreased. A resistor parallel C_{VS} increases the level (see Fig. 3). All this with respect to limited values. The shunt regulator contains a thyristor which short-circuits R12 for a short period during the switch-on time. This reduces the overshoot voltage to only 1 V above the level set by the regulator.

Active output stage

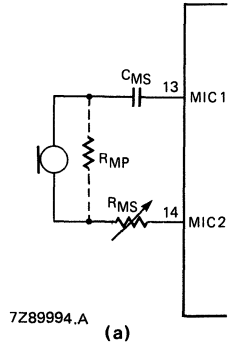
The amplifier consists of a voltage to current converter with a class-A output stage. Because of the feedback from the line to the input the circuit acts as a dynamic resistance (R_a). This resistance can be adjusted by the external resistor R_{ZI} and the value can be found by:

$$R_a = 8.93 \times R_{ZI}\ (\Omega)$$

The total dynamic resistance R_i equals R_a parallel with the resistance R_P of all other circuits parts, which value is approximately 7 kΩ.
With R_{ZI} = 75 Ω, R_a = 670 Ω and R_i = 610 Ω.
For R_{ZI} = 120 Ω, R_a = 1070 Ω and R_i = 900 Ω.

Microphone amplifier

Pins 13 and 14 respectively are the non-inverting and inverting inputs for the microphone. The purely symmetrical inputs are suitable for low ohmic dynamic or magnetic capsules. The input impedance equals 4 kΩ. The voltage amplification from microphone input to pin 1 (VL) is 50 dB and if a lower gain is required the attenuation for a series resistor R_{MS} will be:

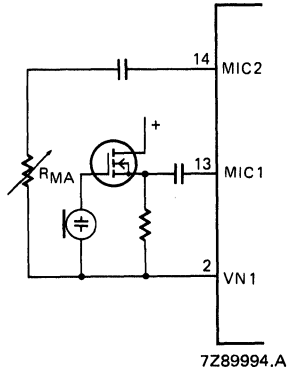


$$\frac{A_M(R_{MS} \neq 0)}{A_M(R_{MS} = 0)} = \frac{4}{4 + R_{MS}} \qquad (R_{MS} \text{ in k}\Omega)$$

$$A_M = \left|\frac{V_L}{V_M}\right|$$

Fig. 4 Symmetrical microphone connection. Resistor R_{MP} may be used to lower the microphone termination resistance.

The microphone amplifier also has an excellent behaviour for connection of an electret microphone with built in FET-source follower. In this condition pin 14 is decoupled for a.c. and the amplifier is driven at pin 13. The input impedance in this asymmetrical mode is 22 kΩ. If attenuation of the amplification is required the value of R_{MA} is given by:



(b)

$$\frac{A_M(R_{MA} \neq 0)}{A_M(R_{MA} = 0)} = \frac{22 + R_{MA}}{22 + 11R_{MA}} \quad (R_{MA} \text{ in k}\Omega)$$

$$A_M = \left| \frac{V_L}{V_{MIC1}} \right|$$

Fig. 5 Electret microphone circuit.

Telephone amplifier and anti-sidetone network

This amplifier is a non-inverting fixed feedback amplifier with a class-A output stage. The gain is fixed and measures 20 dB from pin 4 (TI) to pin 5 (TO). The output is intended to drive capsules Z_T of nom. 350 Ω. For Z_T smaller than 350 Ω the maximum output voltage swing is determined by the bias current of 3.5 mA and Z_T. For Z_T greater than 350 Ω the maximum voltage swing is determined internally. The received line signal is attenuated by the anti-sidetone network and can be adjusted by R_{AT}. The amplification from the line to the telephone output is given by:

$$A_T = 10 \frac{R_{AT}}{R_{AT} + Z_S} \times \frac{Z_T}{Z_T + R_O} \qquad \text{(see Fig. 14)}$$

Z_S is the impedance of the anti-sidetone network
Z_T is the capsule impedance
R_O is the amplifier output resistance

Optimum side-tone suppression is obtained as Z_S (R_{A1}, R_{A2} and C_A) equals

$$Z_S = K \frac{Z_L \times R_i}{Z_L + R_i}$$

Z_L = line terminating impedance
R_i = output stage impedance // passive circuit impedance
K = 237

In the application of Fig. 14 the network is optimized for 5 km of twisted copper wire (ϕ0.5 mm) cable with a d.c. resistance of 176 Ω/km. The side-tone suppression in the range from 0 – 10 km is at least 10 dB compared with the case when no compensation is applied.

5

Keyboard inputs

Inputs for the logic control are compatible with different types of keyboard. Using a keyboard, tone combinations are generated:

- by connecting one of row inputs to one of the column inputs by means of a single switch of the matrix.
- or by applying a dual contact keyboard having its common row contact tied to ground and the common column contact tied to VR.

An anti-bounce circuit eliminates the switch bounce for up to 2 ms. Two key roll-over is provided by blocking other inputs as soon as one key is pressed. Single tones can be generated if the column input is connected to VR or the row input to ground. The inputs for the keyboard connections can be used for direct connection to a microcomputer. If the column inputs are interconnected and made HIGH (= VR) the row inputs are changed to another mode, allowing the circuit to be driven by 4-bit data plus an enable signal. In this mode, it is also possible to connect a separate mute enable signal on inputs COL1, 2 and 4 and a tone enable input on COL3.

Truth table microcomputer mode

row				column		tones Hz	symbol	mute
1	2	3	4	1, 2, 4	3			
H	H	H	H	L	L	–	–	off
X	X	X	X	H	L	–	–	on
H	H	H	H	H	H	697/1209	1	on
H	H	H	L	H	H	697/1336	2	on
H	H	L	H	H	H	697/1477	3	on
H	H	L	L	H	H	697/1633	A	on
H	L	H	H	H	H	770/1209	4	on
H	L	H	L	H	H	770/1336	5	on
H	L	L	H	H	H	770/1477	6	on
H	L	L	L	H	H	770/1633	B	on
L	H	H	H	H	H	852/1209	7	on
L	H	H	L	H	H	852/1336	8	on
L	H	L	H	H	H	852/1477	9	on
L	H	L	L	H	H	852/1633	C	on
L	L	H	H	H	H	941/1209	*	on
L	L	H	L	H	H	941/1336	0	on
L	L	L	H	H	H	941/1477	#	on
L	L	L	L	H	H	941/1633	D	on

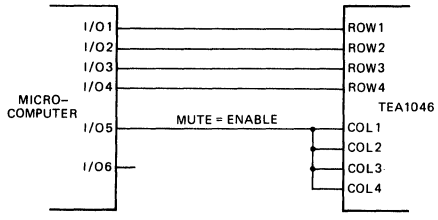
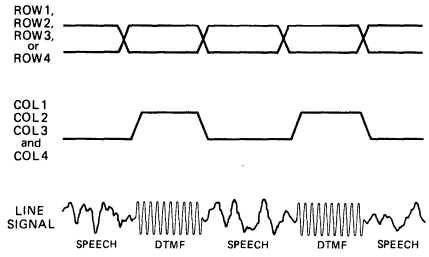


Fig. 6 Microcomputer mode.
All column inputs interconnected.



(a)

Fig. 7 Tone/speech waveform in circuit diagram Fig. 6.

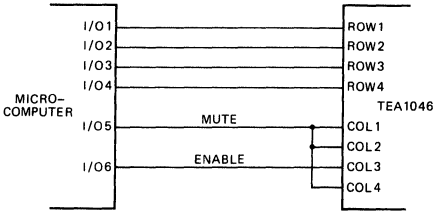
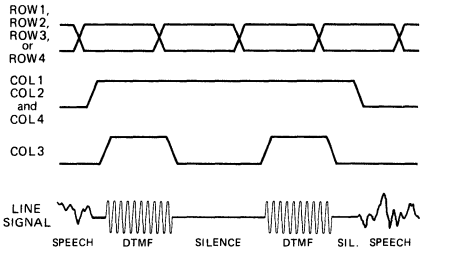


Fig. 8 Microcomputer mode.
Column inputs COL1, 2 and 3 interconnected.



(b)

Fig. 9 Tone/speech waveform in circuit diagram Fig. 8.

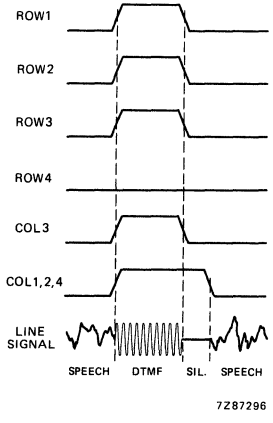


Fig. 10 Waveform tones 697/1336 Hz (dialing number 2).

Dial tone generator

The crystal oscillator frequency is twelve or nine times the clock frequency i.e. 4.782720 MHz or 3.579 545MHz (mask option). The CCITT recommends that the tones should be within 1.5% of the specified frequencies. Many authorities however require a closer tolerance. The application using a crystal of 4.78 MHz gives a maximum dividing error of 0.11% whilst for an application with a 3.58 MHz crystal the error is 0.25% maximum.

The output from the dividers for the higher and the lower frequency tones are symmetrical square-wave pulses which contain considerable odd-numbered harmonics. The lower order odd numbered harmonics (11th and less) are eliminated by synthesising the tone frequencies as crude stepped sinewave approximations. Each half cycle of the tone waveform comprises seven discrete amplitudes for the higher frequency tone. Each amplitude increment is generated by switching on and off an individual current source for the duration of each step of the sinewave. The frequency of the tones is varied by changing the duration of each step. This circuit allows the connecting of two low-pass first order filters to pins 9 and 10 if CEPT 203 recommendations have to be achieved.

The second filter is also used for filtering the microphone signal. If lower requirements for the distortion can be applied the filter at pin 10 can be deleted. In that case the filter at pin 9 must have a lower cut-off frequency (1800 Hz) to achieve a correct pre-emphasis since the roll-off of the filters is compensated internally.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150	mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	850	mA
Operating ambient temperature range	T_{amb}	−25 to	+85	°C
Storage temperature range	T_{stg}	−55 to	+125	°C
Junction temperature	T_j	max.	150	°C

CHARACTERISTICS

T_{amb} = 25 °C; I_L = 15 mA, unless otherwise specified. See also Fig. 11.

description	symbol	min.	typ.	max.	unit
Supply					
Line voltage d.c.					
I_L = 15 mA	V_L	4.5	4.8	5.1	V
I_L = 50 mA	V_L	4.7	5.0	5.3	V
I_L = 100 mA	V_L	5.0	5.4	6.5	V
Temperature coefficient	TC	–	−8	–	mV/K
Line current range	I_L	10	–	120	mA
Stabilized voltage (pin 3)					
I_L = 15 mA	V_S	–	3.3	–	V
I_L = 100 mA	V_S	–	3.8	–	V
Reference voltage (pin 12)	V_R	–	1.0	–	V

description	symbol	min.	typ.	max.	unit
Microphone					
Input resistance (symmetrical)	R_i 13-14	–	4	–	kΩ
Input resistance (asymmetrical)	R_i 13	–	22	–	kΩ
Voltage amplification f = 800 Hz; R_L = 600 Ω	A_M	48	50	52	dB
Temperature coefficient I_L = 50 mA; T_{amb} = −5 to +45 °C	TC		t.b.f.		dB
Common mode rejection ratio	CMRR	60	–	–	dB
Distortion at V_L = 3 dBm	dt	–	2	–	%
Noise output voltage Z_L = 600 Ω; psophometrically weighted (P53 curve)	V_{NO}	–	−70	–	dBmp
Amplification reduction during dialling	ΔA_M	–	70	–	dB
Anti-sidetone					
Voltage amplification, microphone to anti-sidetone output (R_{AT} = 3.9 kΩ)	A_{AT}	–	25.8	–	dB
Transmitter output stage					
Dynamic resistance setting range	R_i	600	–	900	Ω
Variation over line current R_i = 600 Ω	ΔZ_o	–	100	–	Ω
Balance return loss from 300 up to 3400 Hz at 600 Ω (R_{ZI} = 75 Ω, C_L = 10 nF)	BRL	20	–	–	dB
at 900 Ω (R_{ZI} = 120 Ω, C_L = 30 nF)	BRL	20	–	–	dB
Telephone amplifier					
Voltage amplification R_T = 350 Ω	A_T	18	20	22	dB
Amplification variation f = 300 to 3400 Hz	$\Delta A_T/f$	–	0	–	dB
Amplification variation T = −5 to +45 °C	$\Delta A_T/T$	–	0	–	dB
Output voltage swing (d_t = 10%)	$V_{o(p-p)}$	–	1300	–	mV
Output impedance	Z_o	–	5	10	Ω
Input impedance	Z_i	–	100	–	kΩ
Output distortion level < −7 dBV	d_o	–	2	–	%
Output noise voltage psophometrically weighted (P53 curve)	$V_{no\ (rms)}$	–	–	500	μV
Bias current	I_M	3	3.5	4	mA

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CHARACTERISTICS (continued)

description	symbol	min.	typ.	max.	unit
DTMF generator					
Tone frequencies					
low tones (row inputs)			697, 770, 852, 941		Hz
high tones (column inputs)			1209, 1336, 1477, 1633		Hz
Dividing error					
crystal frequency = 4.78 MHz	Δf_d	−0.04	–	+0.11	%
crystal frequency = 3.58 MHz	Δf_d	−0.25	–	−0.05	%
Tone output level					
$I_L > 10$ mA					
lower tones	V_{LG}	–	−11	–	dBm
higher tones	V_{HG}	–	−9	–	dBm
Tone output level					
$I_L > 12$ mA					
lower tones	V_{LG}	−11	–	−6	dBm
higher tones	V_{HG}	−9	–	−4	dBm
Tolerance on output level					
over temp. and current range	ΔV_o	−2	–	2	dB
Pre-emphasis higher tones					
over temp. and current range	ΔV_{HG}	1.3	2	2.7	dB
Tone delay					
after key actuation	t_d	–	10	–	μs
Switch delay time speech/mute					
after key release	t_d	–	10	–	μs
Switch bounce elimination	t_{sb}	–	2	–	ms
Keyboard inputs					
Contact off resistance	R_{Koff}	250	–	–	kΩ
Contact on resistance	R_{Kon}	–	–	10	kΩ
Lower frequency inputs (ROW1, 2, 3, 4)					
voltage LOW	V_{IL}	–	0.7	t.b.f.	V
voltage HIGH	V_{IH}	t.b.f.	1.7	–	V
current (d.c.) at V_{IL}	I_{IL}	–	20	1000	μA
current (d.c.) at V_{IH}	I_{IH}	–	–	–	μA
Higher frequency inputs (COL1, 2, 3, 4)					
voltage LOW	V_{IL}	–	0.3	t.b.f.	V
voltage HIGH	V_{IH}	t.b.f.	1.0	–	V
current (d.c.) at V_{IL}	I_{IL}	–	–	–	μA
current (d.c.) at V_{IH}	I_{IH}	–	20	1000	μA

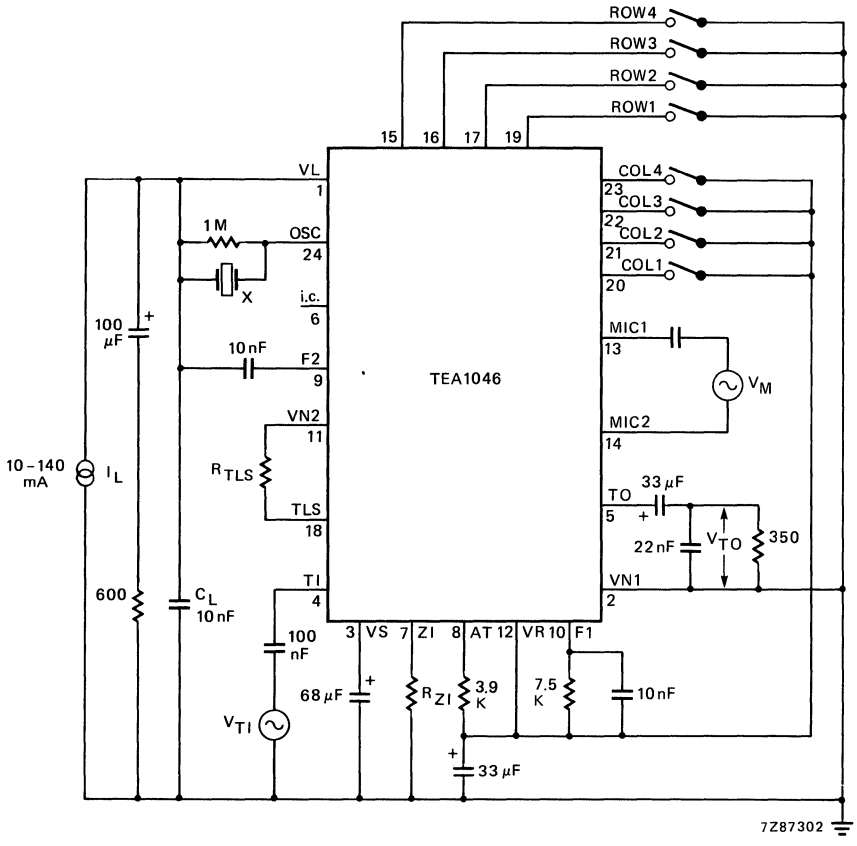


Fig. 11 Test circuit for measuring amplifier voltage gains and frequencies and levels of DTMF generator. X = 3.58 or 4.78 MHz.

$$A_M = \left| \frac{V_L}{V_M} \right| \quad (V_{TI} = 0) \qquad A_T = \left| \frac{V_{TO}}{V_{TI}} \right| \quad (V_M = 0) \qquad A_{AT} = \left| \frac{V_{AT}}{V_M} \right| \quad (V_{TI} = 0)$$

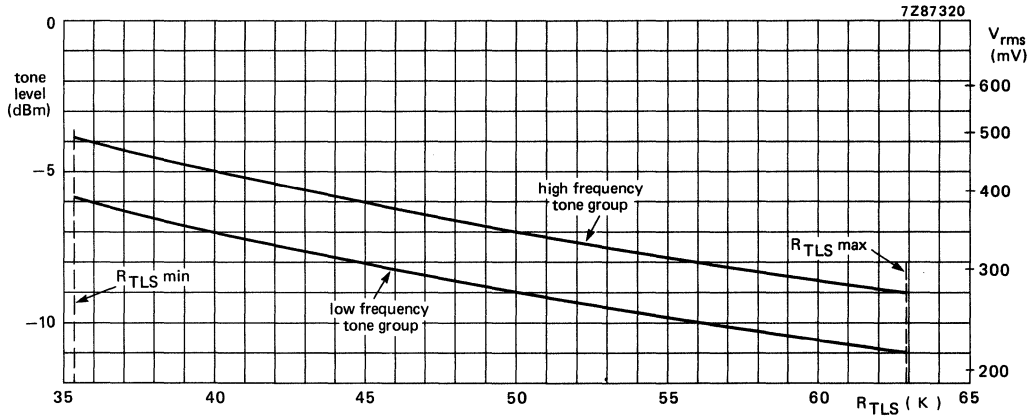


Fig. 12 DTMF level selection. The curve is valid for a dynamic impedance of 600 Ω (R_{ZI} = 75 Ω).

Some values:

LOW dBm	HIGH dBm	R_{TLS} kΩ
−6	−4	35.2
−8	−6	44.8
−11	−9	62.6

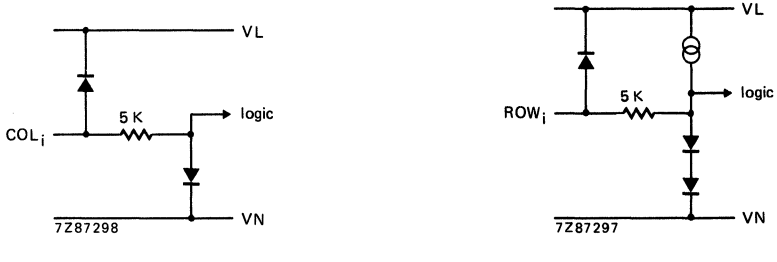


Fig. 13 Configuration inputs. (a) ROW1, 2, 3 and 4. (b) COL1, 2, 3 and 4.

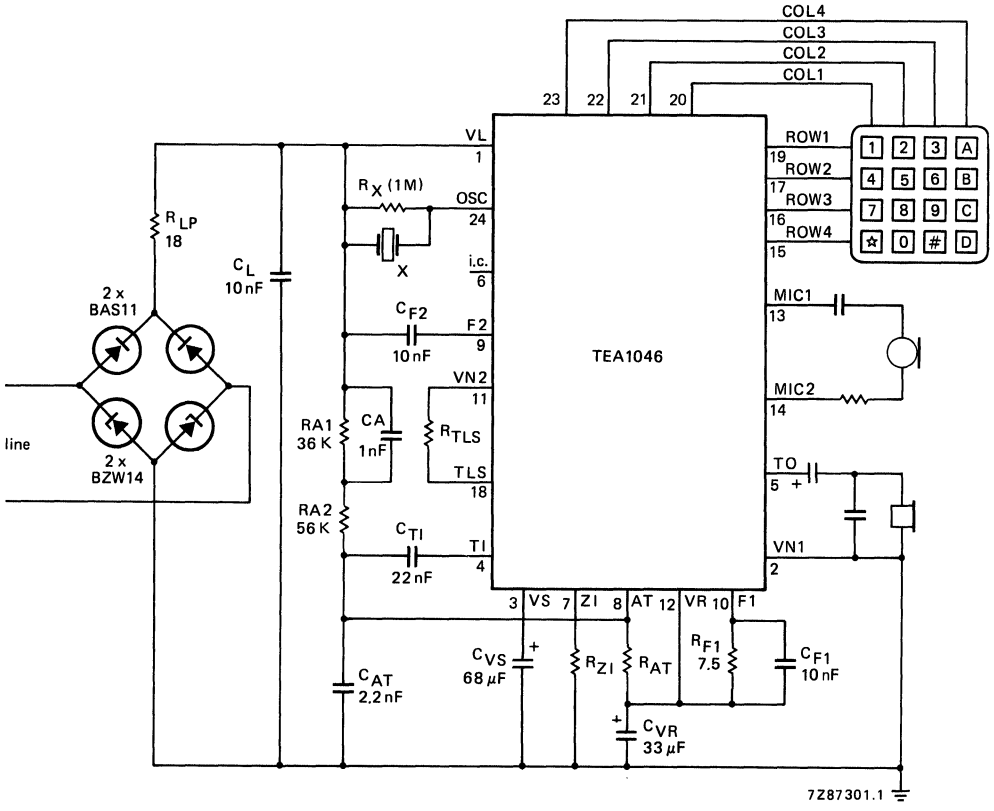


Fig. 14 Application diagram TEA1046 using dynamic transducers, R_{MS}, R_{AT}, R_{ZI} and R_{TLS} determined by transducers and system requirements.

Telephone Transmission Circuit with Dialer Interface — TEA1060/61

GENERAL DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech and line interface functions required in fully electronic telephone sets. The circuits internally perform electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)
- Asymmetrical high-impedance input for electret microphone (TEA1061)
- DTMF signal input
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on all amplifiers
- Line loss compensation facility, line current dependent
- Gain control adaptable to exchange supply

QUICK REFERENCE DATA

Line voltage at I_{line} = 15 mA	V_{LN}	typ.	4,35	V
Line current operating range	I_{line}	10 to	140	mA
Supply current				
power down input LOW	I_{CC}	typ.	1	mA
power down input HIGH	I_{CC}	typ.	50	μA
Voltage amplification range microphone amplifier				
TEA1060	A_{vd}	44 to	60	dB
TEA1061	A_{vd}	30 to	46	dB
receiving amplifier	A_{vd}	17 to	39	dB
Amplification control range	ΔA_{vd}	typ.	6	dB
Exchange supply voltage range	V_{exch}	24 to	60	V
Exchange feeding bridge resistance range	R_{exch}	400 to	1000	Ω
Operating ambient temperature range	T_{amb}	−25 to	+75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

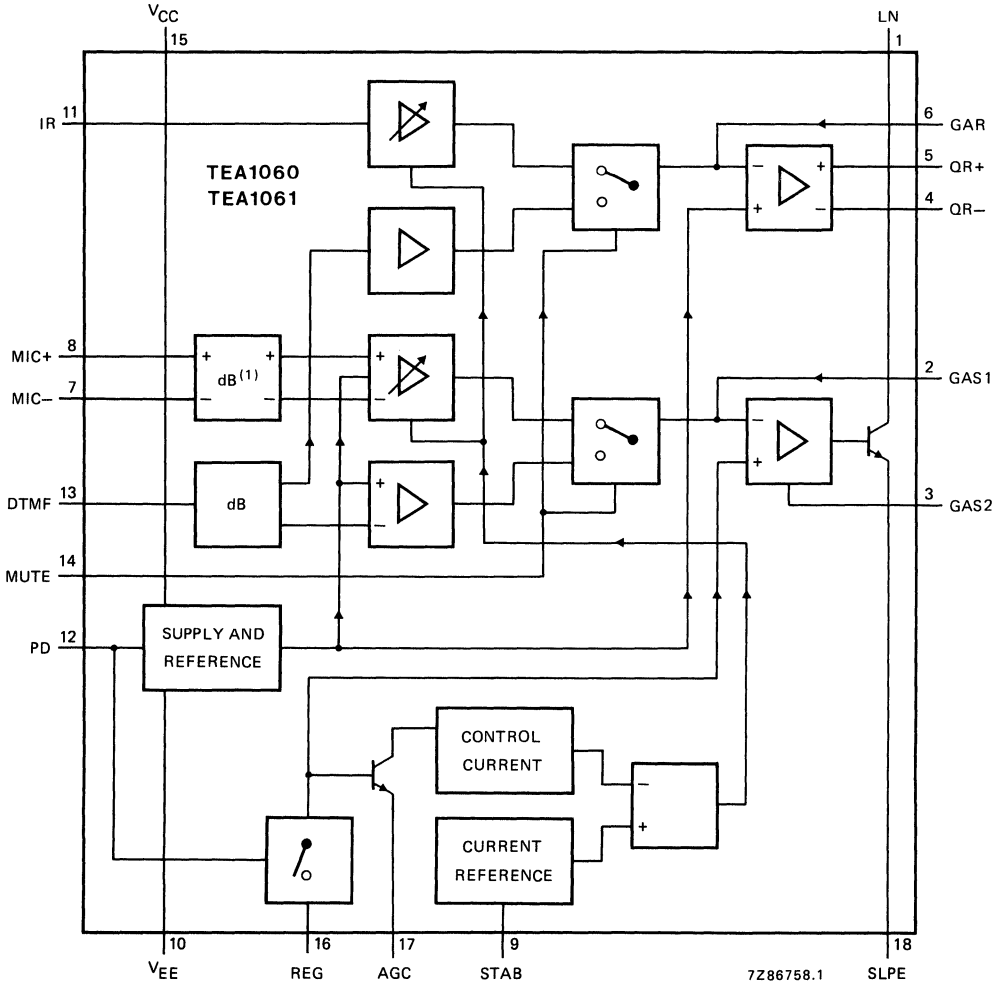


Fig. 1 Block diagram. The blocks marked "dB" are attenuators. The block marked (1) is only present in the TEA1061.

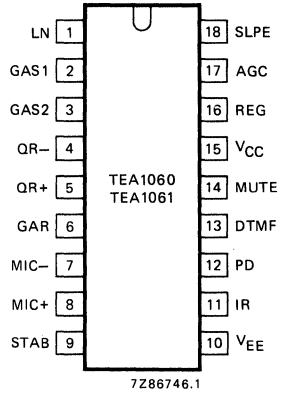


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (d.c. resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits usually are supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3,6 kΩ between STAB and V_{EE}.

The d.c. current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the d.c. resistance of the subscriber line R_{line} and the d.c. voltage on the subscriber set (see Fig. 3).

If the line current I_{line} exceeds the current I_{CC} + 0,5 mA required by the circuit itself ($I_{CC} \approx 1$ mA), plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0{,}5.10^{-3} - I_p) \times R9.$$

V_{ref} being an internally generated temperature compensated reference voltage of 4,1 V and R9 being an external resistor connected between SLPE and V_{EE}. Under normal conditions $I_{SLPE} \gg I_{CC} + 0{,}5\,mA + I_p$. The static behaviour of the circuit then equals a 4,1 V voltage regulator diode with an internal resistance R9. In the audio-frequency range the dynamic impedance equals R1.

FUNCTIONAL DESCRIPTION (continued)

The current I_p available from V_{CC} for supplying peripheral circuits depends on external components, and on the line current. Figure 4 shows this current for V_{CC} = 3 V min., this being the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC– and gain adjustment pins GAS1 and GAS2

The TEA1060 and TEA1061 have symmetrical microphone inputs.

The TEA1060 is intended for low-sensitivity, low-impedance dynamic or magnetic microphones. Its input impedance is 2 x 4 kΩ and its voltage amplification is typ. 52 dB.

The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 2 x 20 kΩ and its voltage amplification is typ. 38 dB.

The arrangements with the microphone types mentioned are shown in Fig. 5.

The amplification of the microphone amplifier in both types can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R7 connected between GAS1 and GAS2.

5

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage amplification from DTMF to LN is typ. 26 dB and varies with R7 in the same way as the amplification of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, OR– and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR–. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 6). Amplification from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the amplification is increased by 6 dB. This makes differential drive possible, which is required for high-impedance dynamic, magnetic and piezoelectric earpieces with load impedances exceeding 450 Ω.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and r.m.s. value is higher.

The amplification of the receiving amplifier can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The amplification is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C7 = 10 x C4 = 1 nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the amplification of the microphone amplifier and the receiving amplifier in accordance with the d.c. line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0,5 mm diameter copper twisted-pair cable with a d.c. resistance of 176 Ω/km and an average attenuation of 1,2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 7 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum amplification as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input, which reduces the supply current from typ. 1 mA to typ. 50 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the circuit's impedance equals a 4,1 V voltage regulator diode with an internal resistance equal to R9. This results in rectangular current waveforms in pulse dialling and register recall.

When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of R2, R3, R8 and Z_{bal} (see Fig. 10). Maximum compensation is obtained when Z_{bal}/k equals the line impedance Z_{line} as seen by the set (scale factor $k = R_8/R_1$).

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

The anti-side-tone network attenuates the signal from the line. With R8 = 390 Ω and R9 = 20 Ω the attenuation is 32 dB. The attenuation is nearly flat over the audio-frequency range.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive line voltage	V_{LN}	max.	13,2	V
Line current				
average	$I_{line(AV)}$	max.	140	mA
non-repetitive (t_{max} = 100 hours)	$I_{line(S)}$	max.	250	mA
non-repetitive peak (t_{max} = 1 ms)	$I_{line(SM)}$	max.	1	A
Voltage on all other pins	V	max.	V_{CC} + 0,7	V
	−V	max.	0,7	V
Total power dissipation	P_{tot}	max.	640	mW
Storage temperature range	T_{stg}	−40 to	+125	°C
Operating ambient temperature range	T_{amb}	−25 to	+75	°C

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)					
Voltage drop over circuit					
at I_{line} = 5 mA	V_{LN}	–	4,15	–	V
at I_{line} = 15 mA	V_{LN}	4,15	4,35	4,55	V
at I_{line} = 100 mA	V_{LN}	–	6,0	7	V
Variation with temperature at I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Supply current					
at V_{CC} = 2,8 V; PD = LOW	I_{CC}	–	0,96	1,25	mA
at V_{CC} = 2,8 V; PD = HIGH	I_{CC}	–	50	–	μA
Microphone inputs MIC+ and MIC−					
Input impedance					
TEA1060	$\lvert z_{is} \rvert$	–	4	–	kΩ
TEA1061	$\lvert z_{is} \rvert$	–	20	–	kΩ
Standard deviation on input impedance	σ	–	12	–	%
Common-mode rejection ratio; TEA1060	k_{CMR}	–	80	–	dB
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ					
TEA1060	A_{vd}	51	52	53	dB
TEA1061	A_{vd}	37	38	39	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB

5

parameter	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF					
Input impedance	$\|z_{is}\|$	–	20	–	kΩ
Standard deviation on input impedance	σ	–	12	–	%
Voltage amplification at I_{line} = 15 mA; R7 = 68 kΩ	A_{vd}	25	26	27	dB
Variation with frequency at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB
Gain adjustment pins GAS1 and GAS2					
Amplification variation with R7, transmitting amplifier	ΔA_{vd}	−8	–	+8	dB
Transmitting amplifier output LN					
Output voltage at I_{line} = 15 mA; d_{tot} = 2%	$V_{LN(rms)}$	1,4	2,3	–	V
d_{tot} = 10%	$V_{LN(rms)}$	–	2,6	–	V
Noise output voltage at I_{line} = 15 mA; R7 = 68 kΩ; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR					
Input impedance	$\|z_{is}\|$	–	20	–	kΩ
Receiving amplifier outputs QR+ and QR−					
Output impedance; single-ended	$\|z_{os}\|$	–	4	–	Ω
Voltage amplification at I_{line} = 15 mA; R4 = 100 kΩ; single-ended; R_L = 300 Ω	A_{vd}	24	25	26	dB
differential; R_L = 600 Ω	A_{vd}	30	31	32	dB
Variation with frequency, at f = 300 to 3400 Hz	$\Delta A_{vd}/\Delta f$	–	±0,2	–	dB
Variation with temperature at I_{line} = 50 mA; T_{amb} = −25 to +75 °C	$\Delta A_{vd}/\Delta T$	–	±0,5	–	dB
Output voltage at I_p = 0; d_{tot} = 2%; sine-wave drive single-ended; R_L = 150 Ω	$V_{o(rms)}$	0,3	0,38	–	V
single-ended; R_L = 450 Ω	$V_{o(rms)}$	0,4	0,52	–	V
differential; C_L = 47 nF + R_L = 100 Ω; f = 3400 Hz	$V_{o(rms)}$	0,8	1,0	–	V
Noise output voltage at I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve) single-ended; R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential; R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Gain adjustment pin GAR					
Amplification variation with R4, receiving amplifier	ΔA_{vd}	−8	–	+8	dB
MUTE input					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{MUTE}	–	8	15	μA
Reduction of voltage amplification from MIC+ and MIC− to LN at MUTE = HIGH	$-\Delta A_{vd}$	–	70	–	dB
Voltage amplification from DTMF to QR+ or QR− at MUTE = HIGH; single-ended load; R_L = 300 Ω	A_{vd}	–	−18	–	dB
Power-down input PD					
Input voltage					
HIGH	V_{IH}	1,5	–	V_{CC}	V
LOW	V_{IL}	–	–	0,3	V
Input current	I_{PD}	–	5	10	μA
Automatic gain control input AGC					
Amplification control range	$-\Delta A_{vd}$	–	6	–	dB
Highest line current for maximum amplification at R6 = 110 kΩ	I_{line}	–	22	–	mA
Lowest line current for minimum amplification at R6 = 110 kΩ	I_{line}	–	60	–	mA

5

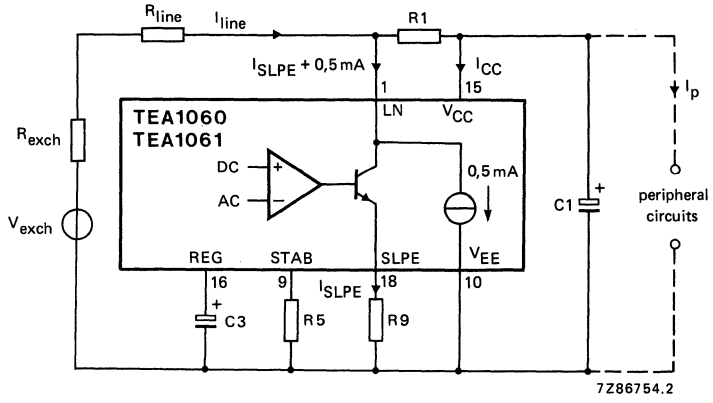


Fig. 3 Supply arrangement.

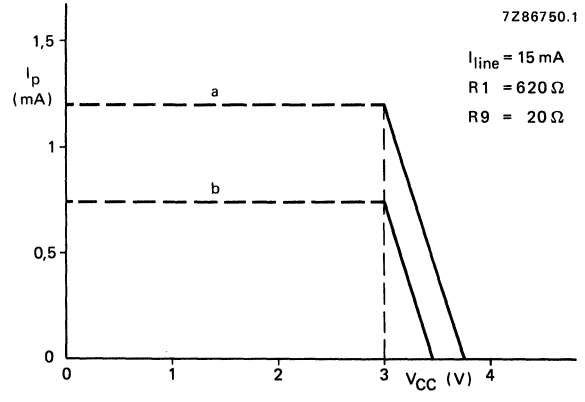


Fig. 4 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with $V_{CC} \geqslant 3$ V. Curve "a" is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve "b" is valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$.

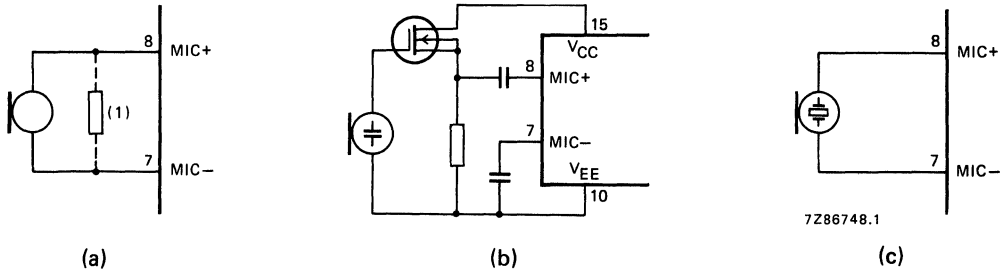


Fig. 5 Alternative microphone arrangements. (a) magnetic or dynamic microphone, TEA1060. The resistor marked (1) may be connected to lower the terminating impedance. (b) electret microphone, TEA1061. (c) piezoelectric microphone, TEA1061.

5

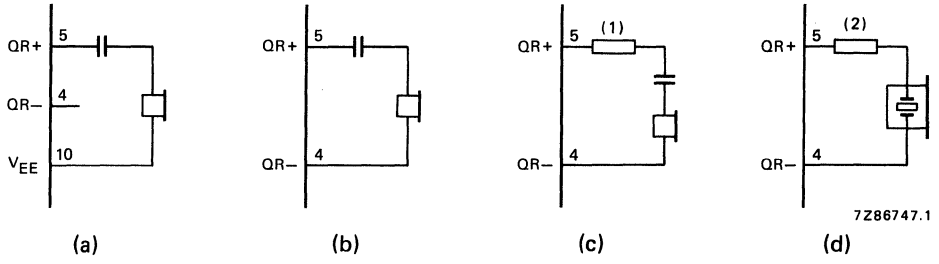


Fig. 6 Alternative receiver arrangements. (a) dynamic telephone with less than 450 Ω impedance. (b) dynamic telephone with more than 450 Ω impedance. (c) magnetic telephone with more than 450 Ω impedance. The resistor marked (1) may be connected to obtain an appropriate acoustic frequency characteristic. (d) piezoelectric telephone. The resistor marked (2) is required to increase the phase margin.

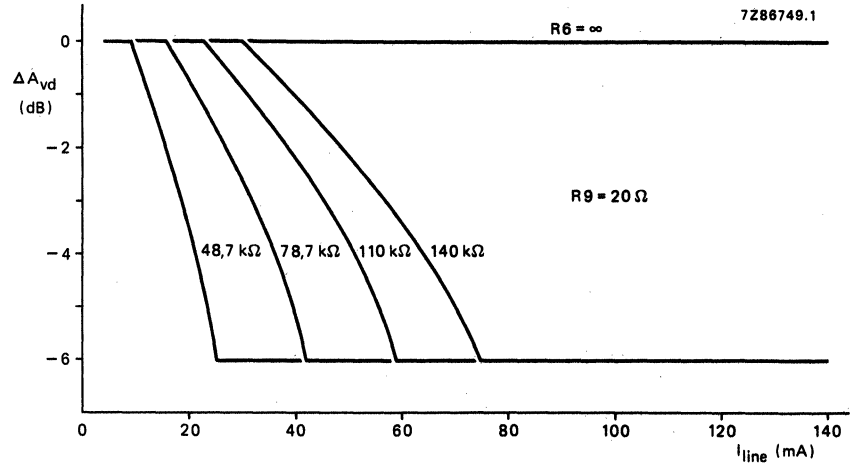


Fig. 7 Variation of amplification with line current, with R6 as a parameter.

Table 1. Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61,9	48,7	X	X
	36	100	78,7	68	60,4
	48	140	110	93,1	82
	60	X	X	120	102

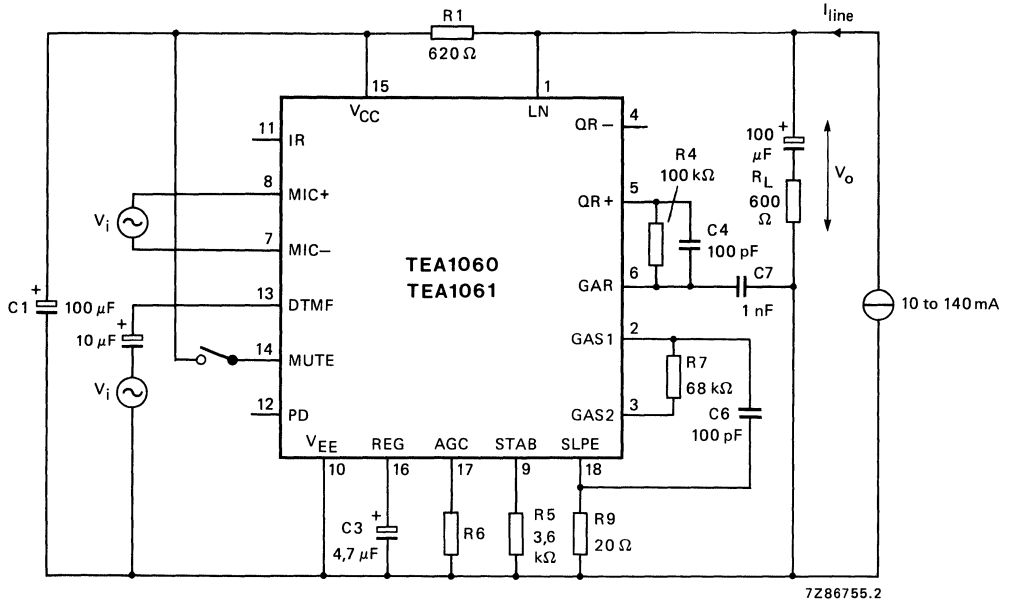


Fig. 8 Test circuit for defining voltage amplification of MIC+, MIC– and DTMF inputs. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$. For measuring the amplification from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

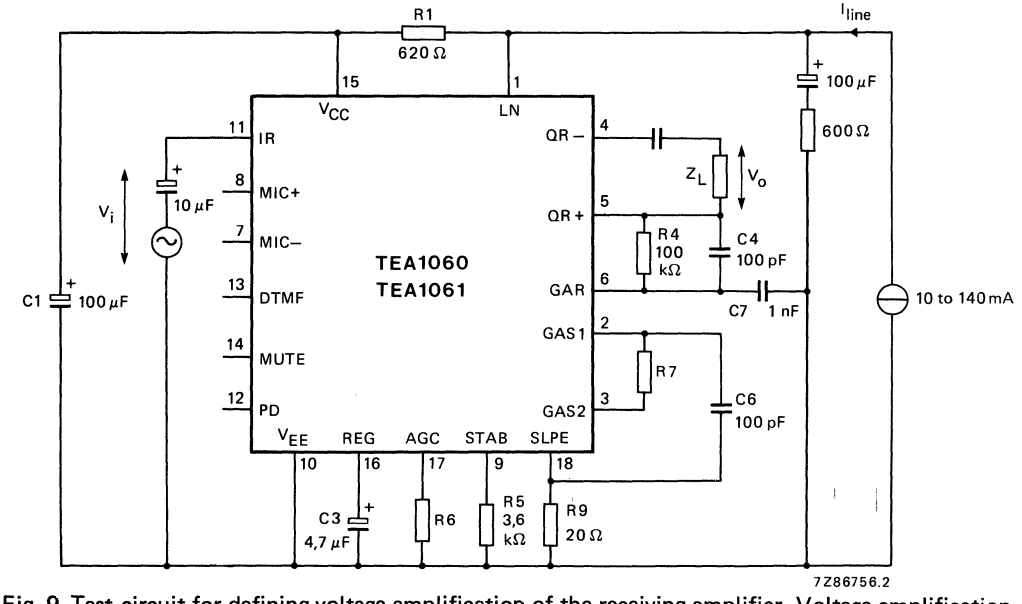


Fig. 9 Test circuit for defining voltage amplification of the receiving amplifier. Voltage amplification is defined as: $A_{vd} = 20 \log |V_o/V_i|$.

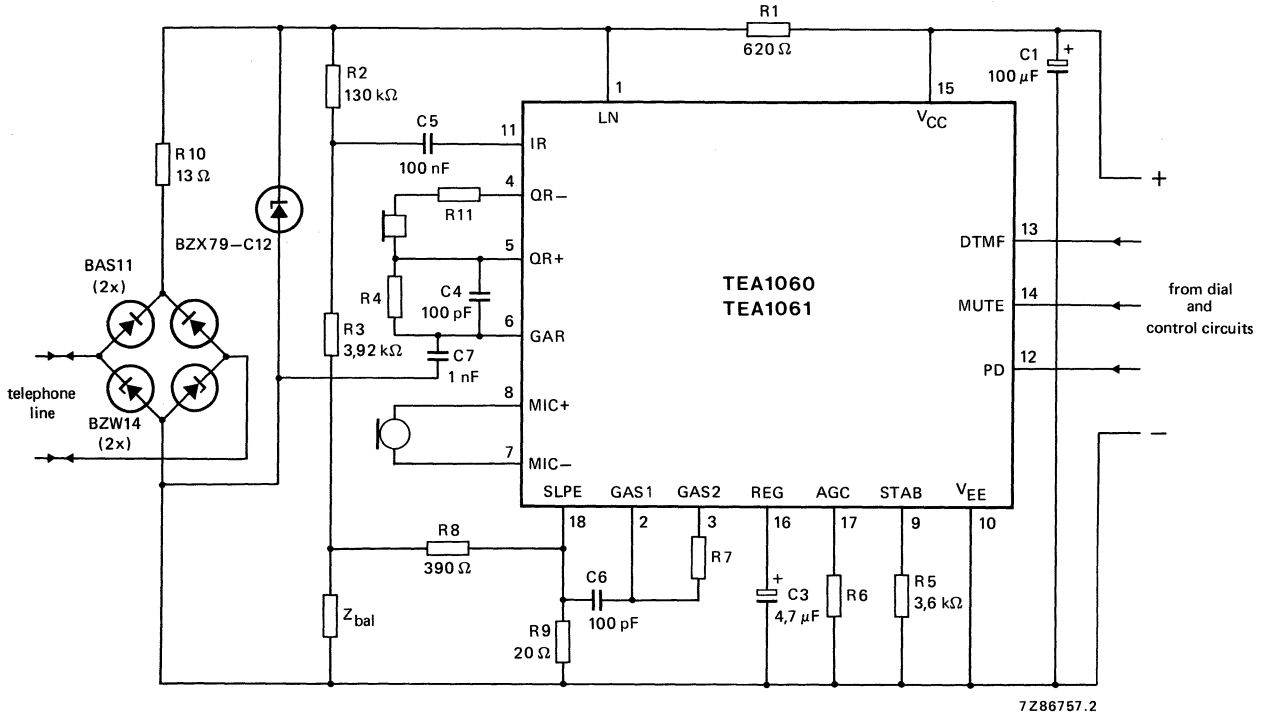


Fig. 10 Typical application of the TEA1060 or TEA1061, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

APPLICATION INFORMATION SUPPLIED ON REQUEST

APPLICATION INFORMATION (continued)

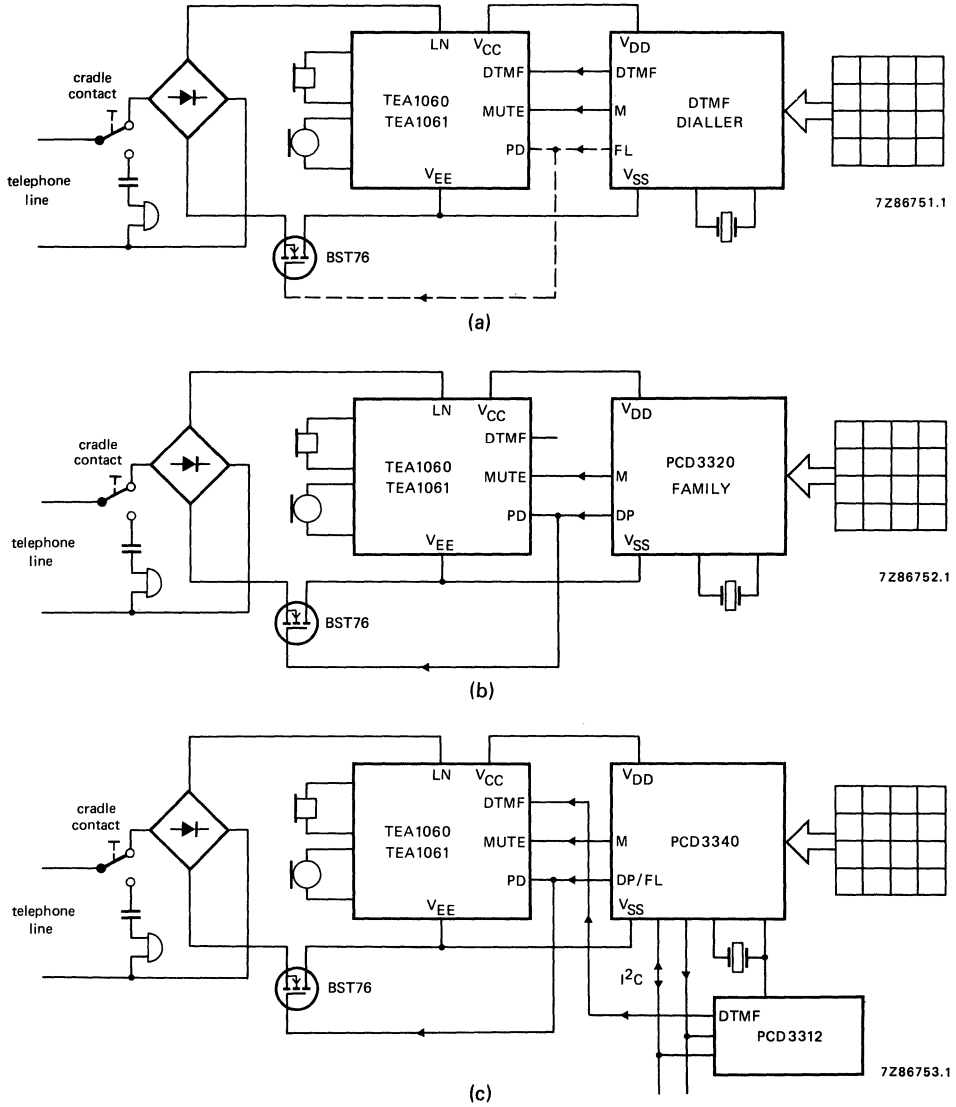


Fig. 11 Typical applications of the TEA1060 or TEA1061 (simplified).

(a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by timed loop break).
(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.
(c) Dual-standard (pulse and DTMF) feature phone with the PCD3340 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C bus.

Low Voltage Transmission IC with Dialer Interface TEA1067

DESCRIPTION

The TEA1067 is a low-voltage bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. The TEA1067 operates down to 2.0V which facilitates the use of telephone sets in parallel operation. Electronic switching between dialing and speech is performed by internal circuitry. Other specifications similar to TEA1060/61.

FEATURES

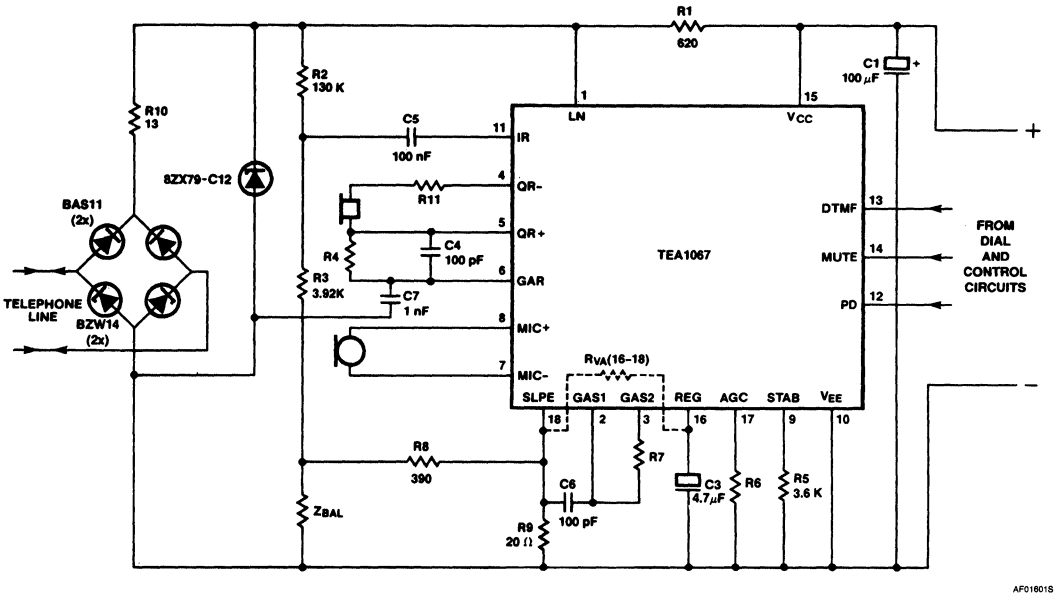
- **Low DC line voltage; operates down to 2V excluding polarity guard.**
- **Minimum instantaneous line voltage 0.9V excluding polarity guard.**
- **Voltage regular with adjustable static resistance.**
- **Provides supply with limited current for external circuitry.**
- **Symmetrical high-impedance inputs (64kohm) for dynamic, magnetic or piezoelectric microphones.**
- **Asymmetrical high-impedance input (32kohm) for electret microphone.**
- **DTMF signal input.**
- **Mute input for pulse or DTMF dialing.**
- **Power down input for pulse dial or register recall.**
- **Receiving amplifier for magnetic, dynamic or piezoelectric earpieces.**
- **Large amplification setting range on microphone and earpiece amplifiers.**
- **Line loss compensation facility, line current dependent.**
- **Gain control adaptable to exchange supply.**
- **Possibility to adjust the DC line voltage.**

APPLICATIONS

- **Telephone handsets requiring low operating voltage.**

Low Voltage Transmission IC with Dialer Interface | TEA1067

APPLICATIONS DIAGRAM



Typical application of the TEA1067, shown here with a piezoelectric earpiece and DTMF dialing. The bridge to the left, the zener diode, and R10 limit the current into and the voltage across the circuit during line transients. Pulse dialing, or register recall, require a different protection arrangement.

By means of resistor R_{VA} (16 – 18) the DC line voltage can be set to a higher value.

5

DTMF Generator for Telephone Dialing TEA1075

This integrated circuit is a dual tone multi-frequency (DTMF) generator with line interface for use in push button telephone sets containing an electronic speech circuit or a conventional hybrid transformer. The IC contains a mute switch handling the full line current, which allows two-wire connection between dial and speech parts. The logic inputs can be operated with a single contact keyboard or via a direct interface with a microcomputer. I^2L technology allows digital and analogue functions to be implemented on the same chip. The line interface incorporates a filter amplifier, an output stage and a voltage stabilizer all of which are switched off when the speech circuit is connected to the line. The tone generator is supplied by a temperature compensated current stabilizer and is be driven by a 3,58 MHz crystal.

The logic inputs contain an interface circuit to guarantee well-defined states of the keyboard.

Features:

- two wire connection between dial and speech parts allowed
- wide operating line current and temperature range
- operating voltage down to 1,7 V
- no individual tone level adjustment required
- few external components required
- all mute functions on chip
- common inputs for keyboard and microcomputer
- temperature and line current independent signal levels
- all pins protected against electrostatic discharges
- on-chip output stage and line regulator
- single tone generation possibility

QUICK REFERENCE DATA

Operating voltage	V_L	typ. 3,3	V
Line current range	I_L	10 to 120	mA
DTMF levels (adjustable)			
low frequency	V_{LG}	−11 to −6	dBm
high frequency	V_{HG}	−9 to −4	dBm
Pre-emphasis	$V_{HG}-V_{LG}$	max. 2	dB
Operating temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINE

TEA1075P: 18-lead DIL, plastic (SOT-102HE).

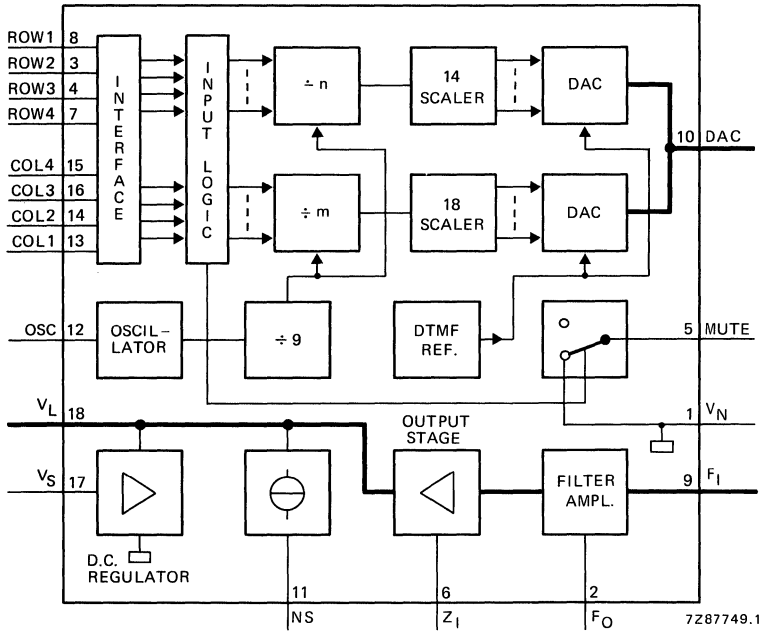


Fig. 1 Functional block diagram.

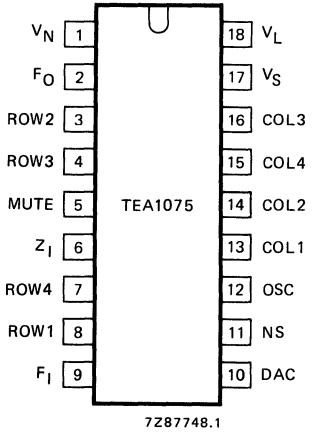


Fig. 2 Pin designation.

PINNING

1	V_N	negative line voltage
2	F_O	filter output
3	ROW2	row input 770 Hz/BCD input
4	ROW3	row input 852 Hz/BCD input
5	MUTE	mute switch
6	Z_I	impedance setting terminal
7	ROW4	row input 941 Hz/BCD input
8	ROW1	row input 697 Hz/BCD input
9	F_I	filter input
10	DAC	DTMF level setting
11	NS	noise suppression input
12	OSC	oscillator input
13	COL1	column input 1209 Hz/mute input
14	COL2	column input 1336 Hz/mute input
15	COL4	column input 1633 Hz/mute input
16	COL3	column input 1477 Hz/enable input
17	V_S	voltage stabilizer filter
18	V_L	positive line voltage

FUNCTIONAL DESCRIPTION

Voltage regulator

The voltage regulator switches on as a keyboard button is pressed. It regulates the voltage drop across the IC to a nominal level of 3,3 V, shunting excess line current to maintain a working current of 8 mA within the chip. The voltage regulator is switching to a higher voltage level when the keyboard switch is released.

The capacitor connected to input V_S provides a low-pass filter function to avoid influence of audio signals on the line. For a short period during switch-on time the capacitor is directly connected to the line to reduce overshoot voltages to only 1 V above the voltage set by the regulator.

In order to adapt the nominal d.c. level to the level as set by the speech circuit, a resistor can be connected either between V_L and V_S or between V_N and V_S. This will decrease or increase the level respectively. During the time the device is in the stand-by mode the voltage stabilizer circuit will conduct again as the d.c. line voltage set by the speech part achieves 6,0 V. Part of the line current then will flow through this stabilizer.

Active output stage

The transmitter amplifier consists of a voltage to current convertor with a class-A output stage. The circuit acts as a dynamic resistance (R_a) because of the feedback from the line to the input. This impedance can be set by output Z_I at pin 6:
R_a = 900 Ω if pin 6 is left open
R_a = 600 Ω if pin 6 is connected to V_N (pin 1).
The impedance is extremely high as long as no key is depressed (stand-by mode).

Speech muting

Figure 3 shows the connection of the dial circuit with a speech circuit TEA1060/61. All mute functions are performed by internal switches. Pressing any keyboard push button switches the TEA1075 to operating mode and isolates the speech circuit from the line.

The line adaption then is taken over by the dial circuit which causes:

- line voltage to be set by the voltage regulator TEA1075
- impedance to be set by the active output stage TEA1075
- audio output stage to be connected to the line for DTMF tone transmission.

During the stand-by mode (no key pressed) the voltage on the line is set by the speech circuit. The minimum d.c. operating voltage of the dial circuit for guaranteed detection of push button operation on the keyboard is 2,5 V. The impedance is approximately 10 kΩ and the current consumption 2 mA. The stand-by current is used for the logic part as well as driving current for the internal mute switch which can switch the full line current available.

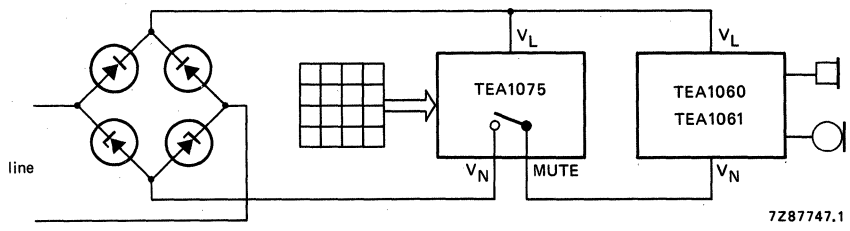


Fig. 3 Muting system.

FUNCTIONAL DESCRIPTION (continued)

OSC and DTMF generator

The crystal oscillator frequency (3,579 545 MHz) is divided by a factor of nine to give the clock frequency. A maximum division error of 0,31% is achieved in the TEA1075; CCITT recommendations are that tones should be within 1,5% of the specified frequencies.
A bias resistor of 1 to 4,7 MΩ must be connected between the oscillator input and V_P. An external frequency generator can be connected instead of a crystal (see Fig. 5).

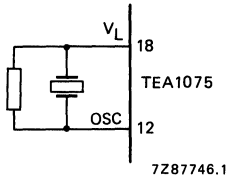


Fig. 4 Quartz crystal oscillator.

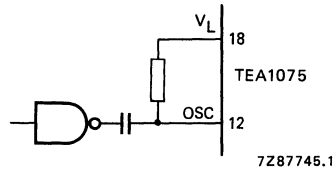


Fig. 5 External frequency generator.

5

The output from the dividers for the higher and the lower frequency tones are symmetrical square-wave pulses which contain considerable odd-numbered harmonics. The lower order odd-numbered harmonics (11th and less) are eliminated by synthesising the tone frequencies as crude stepped sinewave approximations. Each half cycle of the tone waveform comprises seven discrete amplitudes for the lower frequency tone and nine for the higher frequency tone. Each amplitude increment is generated by switching on and off an individual current source for the duration of each step of the sine wave.
The frequency of the tones is varied by changing the duration of each step. This circuit allows the connection of a first or second order filter, depending on the distortion requirements (see filter and DTFM level).

Deviation of ROW and COLUMN frequencies

	freq. Hz	deviation %	real Hz
ROW1	697	−0,24	695,33
ROW2	770	−0,28	767,81
ROW3	852	−0,25	849,84
ROW4	941	−0,31	938,04

	freq. Hz	deviation %	real Hz
COL1	1209	−0,31	1205,23
COL2	1337	−0,10	1334,66
COL3	1477	−0,27	1473,06
COL4	1633	−0,18	1630,03

Filter and DTMF level

The output current from the DAC causes a voltage drop across R_{TLS} at pin 10. At this point the signal path is broken to allow insertion of filter components in series with the amplifier input at pin 9. The output of this amplifier is brought out to pin 2 to allow connection of filter components in the feedback path to provide additional attenuation of the higher-order odd harmonics of the tone frequencies.

The output amplitude of the tones is directly proportional to the value of R_{TLS} and can therefore be adjusted to meet specific requirements. Fig. 6 shows the output level as function of R_{TLS} and R_a = 600 Ω. If R_a = 900 Ω R_{TLS} must be devided by 1,25.

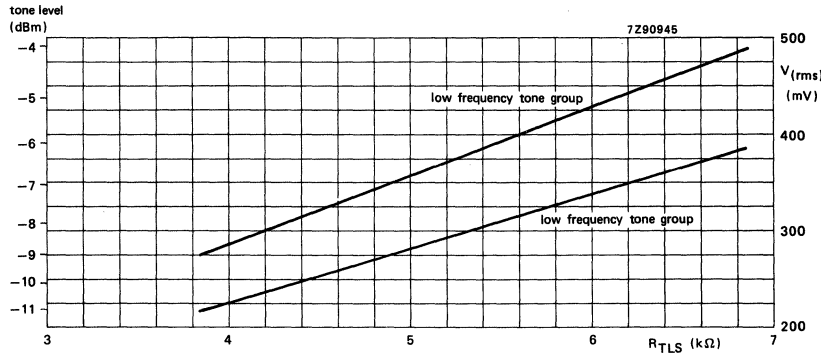


Fig. 6 DTMF level selection.

When R_{TLS} is selected for the required tone level, C_{FI} can be calculated to avoid too much influence of the filter characteristic on the pre-emphasis parameter, the time constant for a single pole filter is:

$R_{TLS} \cdot C_{FI} = 26\ \mu s$ (see Fig. 16).

If higher attenuation is required a second-order filter can be applied. The time constant for such is:

$R_{TLS} \cdot C_{FO} = R_{FS} \cdot C_{FI} = 46\ \mu s$ (see Fig. 15).

Keyboard inputs

Inputs for the logic control are compatible with different types of keyboards. Using a keyboard, tone combinations are generated:

- by connecting one of row inputs to one of the column inputs by means of a single switch of the matrix
- or by applying a dual contact keyboard having its common row contact tied to V_N and the common column contact via 68 kΩ to V_L.

Single tones can be generated by connecting a row input to V_N (pin 1) or one of the column inputs a 68 kΩ resistor to V_L (pin 18).

An anti-bounce circuit eliminates switch bounce.

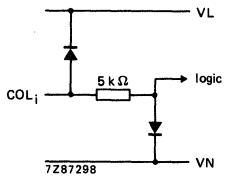


Fig. 7 Configuration of column inputs.

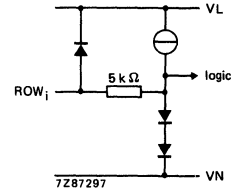


Fig. 8 Configuration of row inputs.

Microcomputer mode

The inputs for the keyboard connections can be used for direct connection to a microcomputer. If the column inputs are interconnected and made 'HIGH' (> 1 V or $I_{cd} = 30\ \mu A$) the row inputs are changed to another mode, allowing the circuit to be driven by 4-bit data plus an enable signal. In this mode, it is possible to connect a separate mute enable signal on inputs COL1, 2 and 4 and a tone enable input on COL3.

FUNCTIONAL DESCRIPTION (continued)

Truth table microcomputer mode

row				column		tones	symbol	mute *
1	2	3	4	1, 2, 4	3	Hz		
H	H	H	H	L	L	–	–	off
X	X	X	X	H	L	–	–	on
H	H	H	H	H	H	697/1209	1	on
H	H	H	L	H	H	697/1336	2	on
H	H	L	H	H	H	697/1477	3	on
H	H	L	L	H	H	697/1633	A	on
H	L	H	H	H	H	770/1209	4	on
H	L	H	L	H	H	770/1336	5	on
H	L	L	H	H	H	770/1477	6	on
H	L	L	L	H	H	770/1633	B	on
L	H	H	H	H	H	852/1209	7	on
L	H	H	L	H	H	852/1336	8	on
L	H	L	H	H	H	852/1477	9	on
L	H	L	L	H	H	852/1633	C	on
L	L	H	H	H	H	941/1209	*	on
L	L	H	L	H	H	941/1336	0	on
L	L	L	H	H	H	941/1477	#	on
L	L	L	L	H	H	941/1633	D	on

* Mute "on" = switch open.

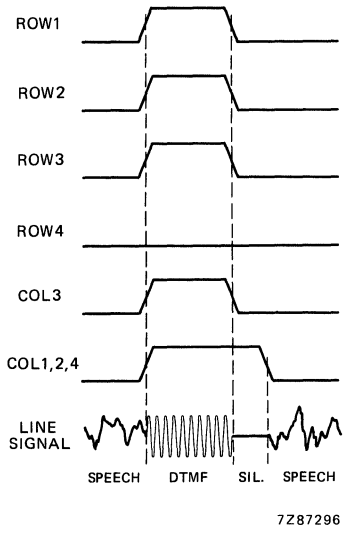


Fig. 9 Waveform tones 697/1336 Hz (dialling number 2).

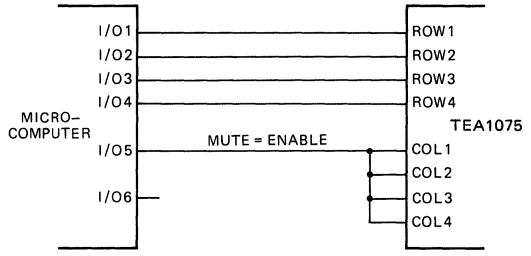


Fig. 10 Microcomputer mode.
All column inputs interconnected.

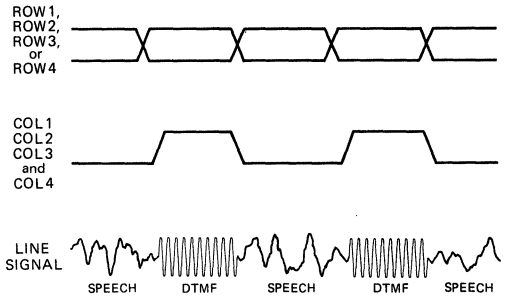


Fig. 11 Tone/speech waveform
in circuit diagram Fig. 10.

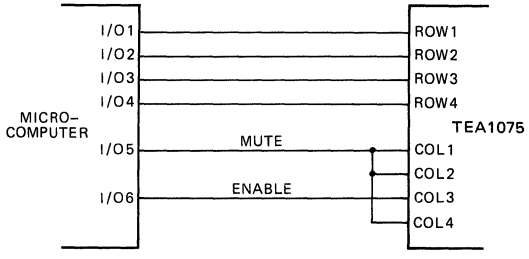
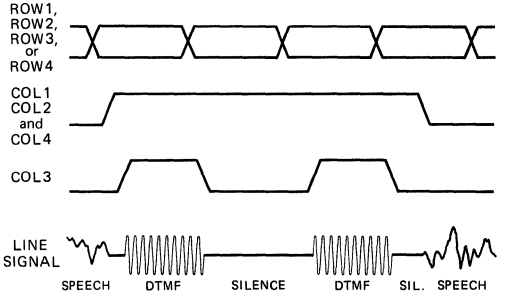


Fig. 12 Microcomputer mode.
Column inputs COL1, 2 and 4
interconnected.



7Z91000A

Fig. 13 Tone/speech waveform
in circuit diagram Fig. 12.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current	I_P	max.	150	mA
Surge current ($t_p < 250\ \mu s$)	I_S	max.	1000	mA
Operating ambient temperature range	T_{amb}		−25 to +70	°C
Storage temperature range	T_{stg}		−55 to +125	°C
Voltage on any pin	V_I		$(V_N-0,3)$ to $(V_L+0,3)$	V
Line voltage	V_{L-N}	max.	10	V
Power dissipation	P_{tot}	max.	750	mW

CHARACTERISTICS

T_{amb} = 25 °C; I_L = 15 mA; f = 1 kHz; unless otherwise specified. See also Fig. 14.

description	symbol	min.	typ.	max.	unit
Supply					
Line voltage d.c. (operating mode)					
I_L = 15 mA	V_L	–	3,3	–	V
I_L = 50 mA	V_L	–	3,7	–	V
I_L = 120 mA	V_L	–	4,5	–	V
Line voltage d.c. (stand-by mode)	V_L	–	–	6,5	V
Temperature coefficient	TC	–	–8	–	mV/K
Line current range	I_L	10	–	120	mA
Transmitter output stage					
Dynamic resistance setting range					
pin 6 open	R_i	–	900	–	Ω
pin 6 connected to V_N	R_i	–	600	–	Ω
Variation over line current					
R_i = 600 Ω	ΔZ_o	–	100	–	Ω
Gain	A_{TL}	–	t.b.f.	–	dB
Balance return loss from 300 up to 3400 Hz					
at 600 Ω	BRL	20	–	–	dB
at 900 Ω (C_L = 30 nF)	BRL	20	–	–	dB
Total harmonic distortion with respect to total output level (second-order filter)	d_{tot}	–	–40	–25	dB
DTMF generator					
Tone frequencies					
low tones (row inputs)		697, 770, 852, 941			Hz
high tones (column inputs)		1209, 1336, 1477, 1633			Hz
Dividing error					
crystal frequency = 3,579545 MHz	Δf_d	–0,31	–	–0,1	%
Tone output level (adjustable)					
$I_L > 10$ mA					
lower tones	V_{LG}	–11	–	–8	dBm
higher tones	V_{HG}	–9	–	–6	dBm
$I_L > 12$ mA					
lower tones	V_{LG}	–11	–	–6	dBm
higher tones	V_{HG}	–9	–	–4	dBm
Tolerance on output level					
over temp. and current range	ΔV_o	–2	–	2	dB
Pre-emphasis higher tones/lower tones					
over temp. and current range	ΔV_{HG}	1	2	3	dB
Tone delay					
after key actuation	t_d	–	–	5	ms
Switch bounce elimination	t_{sb}	–	2	–	ms

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description	symbol	min.	typ.	max.	unit
Mute					
Mute output sink current (no key pressed)	I_{MSS}	–	–	120	mA
Saturation voltage (I_{MS} = 75 mA)	$V_{MT(sat)}$	–	150	500	mV
Maximum voltage (voltage set by speech part)	V_{MT}	–	–	10	V
Stand-by current (V_L = 4,5 V)	I_{STB}	–	2	2,5	mA
Switch delay after key release	t_d	–	–	10	μs
Resistance	R_M	–	10	–	kΩ
Keyboard inputs (microcomputer inputs)					
Contact off resistance	R_{Koff}	300	–	–	kΩ
Contact on resistance	R_{Kon}	–	–	10	kΩ
Lower frequency inputs (ROW1, 2, 3, 4)					
voltage LOW	V_{IL}	–	–	1,1	V
voltage HIGH	V_{IH}	1,5	–	–	V
current (d.c.) at V_{IL} dial mode	I_{ILD}	–	30	–	μA
Higher frequency inputs (COL1, 2, 3, 4)					
voltage LOW	V_{IL}	–	–	0,5	V
voltage HIGH	V_{IH}	0,9	–	–	V
current (d.c.) at V_{IH} dial mode	I_{IHD}	–	30	–	μA

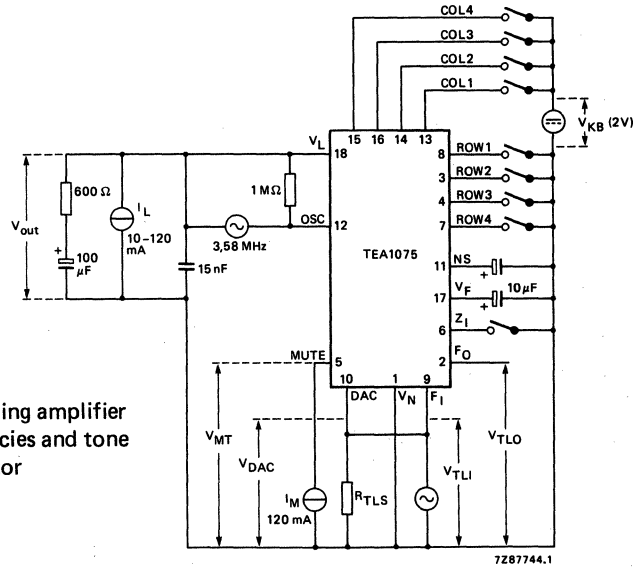

Fig. 14 Test circuit measuring amplifier voltage gain (A_{TL}) frequencies and tone output levels of the generator

$$A_{TL} = \left| \frac{V_{TLO}}{V_{TLI}} \right|$$

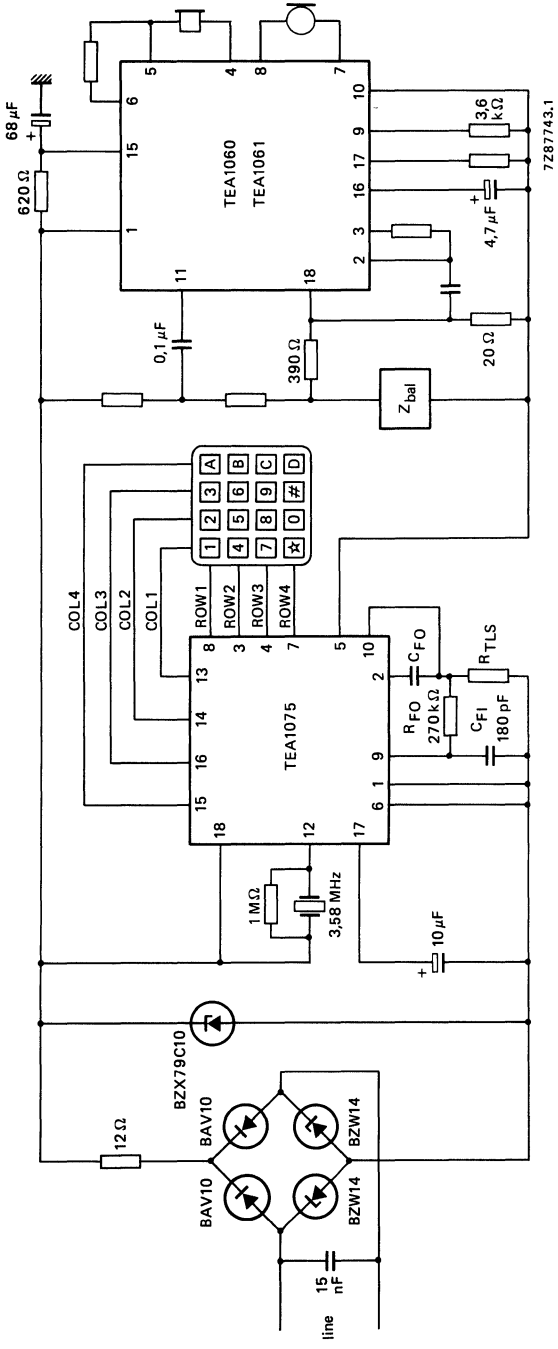

Fig. 15 Application diagram TEA1075 using a second-order filter for low harmonic distortion (CEPT T/CS 34-08). Dial and speech functions are complete separated, so line adaption is done either by TEA1075 or TEA1060. The diagram shows a complete DTMF telephone set including protection. Both circuits are set to an impedance of 600 Ω.

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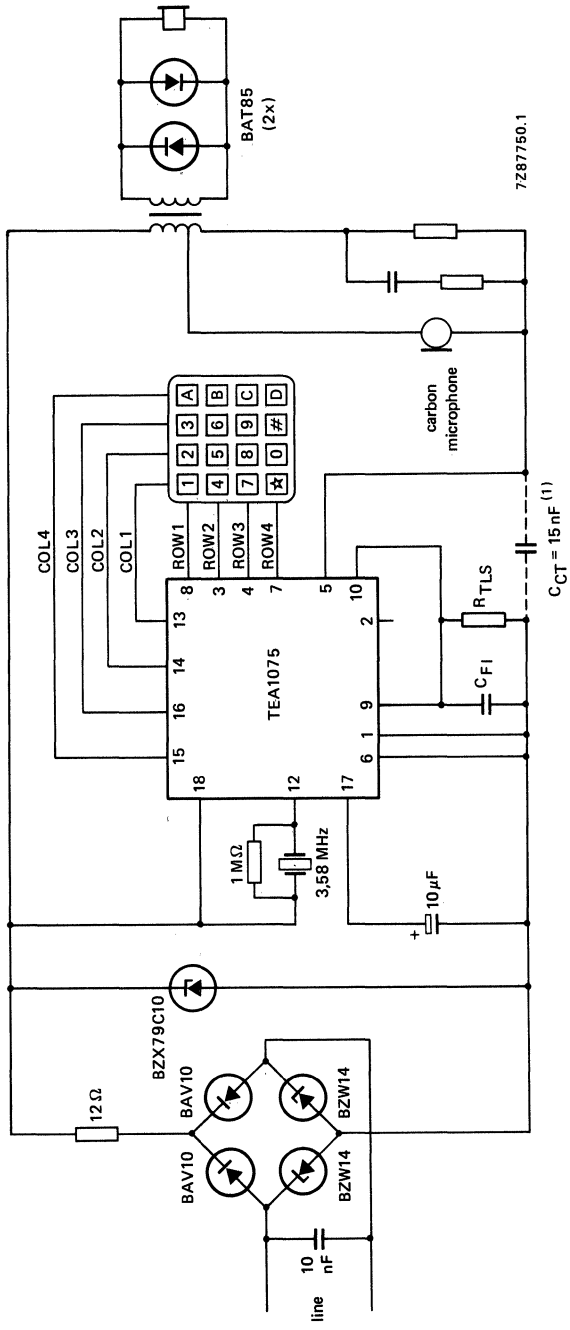


Fig. 16 Application diagram TEA1075 using a single pole filter.

The diagram shows a complete DTMF set including protection.

* C_{CT} connected only if confidence tone is desired.

Supply IC for Telephone Set Peripherals — TEA1080

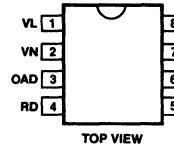
DESCRIPTION

The TEA1080 is a bipolar integrated circuit intended for use in line powered telephone sets to supply peripheral circuits for extended dialing and or loudspeaking facilities. The IC uses a part of the surplus of the line current sinked normally in the voltage regulator of the applied speech/transmission circuit.

FEATURES

- **High input impedance for audio signals**
- **High output current**
- **Large audio signal handling**
- **Low distortion**
- **Two modes of operation:**
  - **Regulated output voltage**
  - **Constant DC voltage drop in series with a resistor between line and output terminal**
- **Low number of external components**

PIN CONFIGURATION

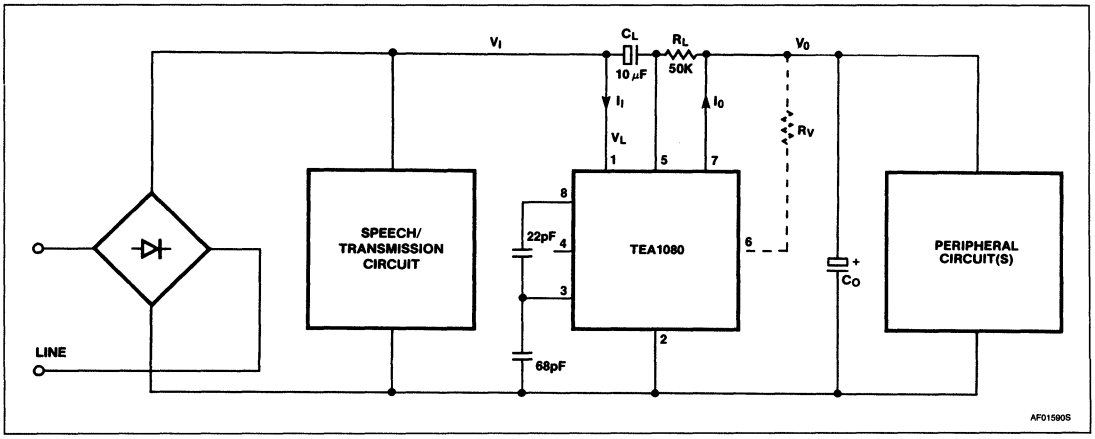


TOP VIEW

CD01370S

PIN	SYMBOL	FUNCTION
1	VL	Positive line terminal
2	VN	Negative line terminal
3	OAD	Output amplifier decoupling
4	RD	Regulator decoupling
5	IF	Low pass filter input
6	OVA	Output voltage adjustment
7	SO	Supply output terminal
8	ER	Terminal for external series resistance

APPLICATIONS DIAGRAM



ORDERING CODE

	PINS	PACKAGE	NOTE
TDA1080	8-lead DIL	Plastic	(SOT-97A)

REFERENCE DATA

PARAMETER	SYMBOL	LIMITS			UNIT
		Min	Typ	Max	
Line voltage, V_1		2.5		10	V
DC output voltage, V_O		2		9.5	V
DC voltage drop, $V_1 - V_O$		.5			V
Series resistance, R_1			20		ohm
Output current ($V_1 > = 4V$)	I_O			30	mA
AC line level ($V_1 > = 4.5V$, $I_O < 15mA$, $d < 2\%$), V_1	(rms)	1.5			V
Internal supply current	I_{int}			1	mA
Operating ambient temperature	T_A	−25		+70	°C

Explanation of Terms

Data Slicing: The process of extracting digital data from an incoming, non-TTL signal.

Full Field Teletext: In this mode, teletext information is transmitted over, virtually, all available TV lines.

Gearing: Since only 32 data characters can be transmitted during one TV line period and 40 characters need to be displayed, a gearing function needs to be implemented.

Ghost Rows: These are the rows that are specified by the "row address field" of the "page header" but do not get displayed. These are rows 24 to 31. Sometimes referred to as "extension packets," these rows carry miscellaneous control information (page extension for telesoftware, linked pages, higher display level,.... etc.)

NABTS: North American Broadcast Teletext Specifications. Note that this is **not** a standard. This document specifies both the acquisition protocol and the display format. The display format is NAPLPS.

NAPLPS: North American Presentation Level Protocol Syntax. Again this is **not** a display standard. It applies to both teletext and videotex services.

Page Header: This is equivalent to row 0. Carry control information about this page.

SRM: Service Reference Model of NAPLPS. It is a skeleton NAPLPS, specifying a low level type display in order to allow for easy implementation (256H x 200H pixels).

Teletext: One way broadcast of digital information. The digital information is injected in the broadcast TV signal: VBI, or full field. The transmission medium could be satellite, cable, ... etc.

The display medium is a regular TV receiver.

VBI: Vertical Blanking Interval – the time it takes the beam to flyback to the top of the screen in order to retrace the opposite field (odd or even). VBI is in the order of 20 TV lines. Teletext information is transmitted over 4 of these lines (lines 14-17).

Videotex: A two-way interactive system through which the user can communicate with a large, organized and secure, data base through a telephone line using the TV as the display medium.

WST: World System Teletext. WST is based on the U.K. teletext standard in which a one-to-one correspondence exists between transmitted characters, page memory, word addresses, and the display screen character locations. The block diagram depicts the 5-chip set WST decoder. Over 98% of the world's teletext decoders are WST compatible.

Teletext Timing Chain for USA 525 Line System — SAA5025D

GENERAL DESCRIPTION

The SAA5025D is a MOS N-channel integrated circuit which performs the timing functions for a Teletext system. It provides the necessary timing signals to extract data from a memory and produce a display according to the USA 525 line television standard (system M).
The SAA5025D may be used in conjunction with the SAA5030 (Teletext video processor; VIP) the SAA5050 (Teletext character generator; TROM), the SAA5040B (Teletext acquisition control; TAC) and the SAA5045 (Gearing and Address Logic Array; GALA).

Features

- Designed to operate with USA 525 line television standard (system M)
- For 24 row (8 TV lines per row) x 40 character display
- Big character select input for double height characters
- Composite sync signal output for display time-base synchronization

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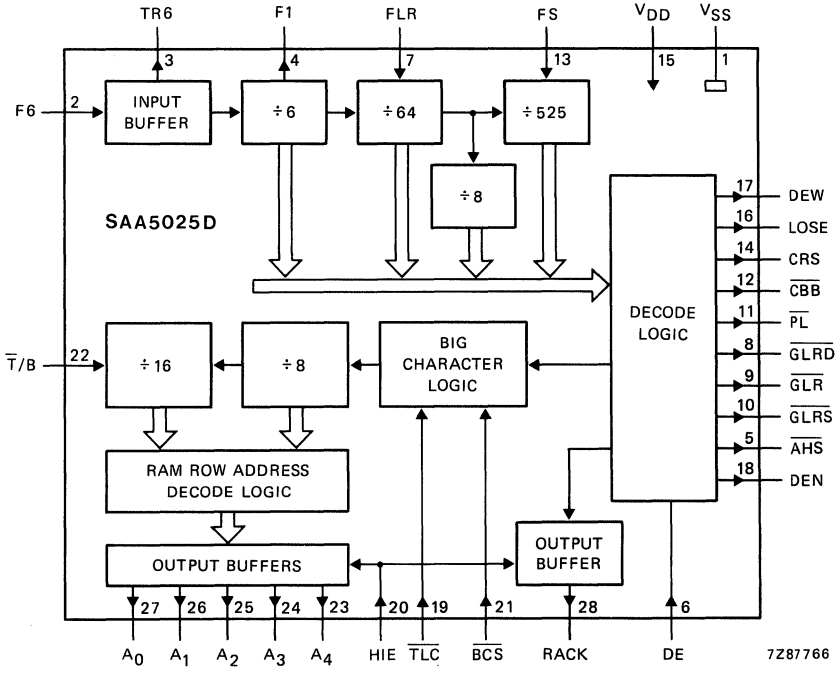

Fig. 1 Block diagram.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117D).

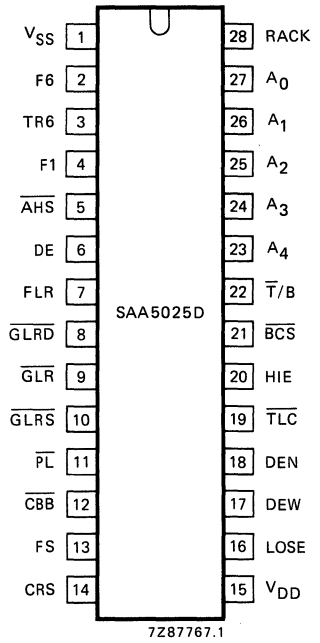

Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground
2	F6	6,0419 MHz clock input
3	TR6	6,0419 MHz clock output
4	F1	1,007 MHz clock output
5	$\overline{AHS}$	after hours sync output
6	DE	display enable input
7	FLR	fast line reset input
8	$\overline{GLRD}$	general line reset delay output
9	$\overline{GLR}$	general line reset output
10	$\overline{GLRS}$	general line reset starting output
11	$\overline{PL}$	phase lock open drain output
12	$\overline{CBB}$	colour burst blanking output
13	FS	field (picture) sync input
14	CRS	character rounding select output
15	V_{DD}	positive supply (+ 5 V)
16	LOSE	load output shift register enable output
17	DEW	data entry window output
18	DEN	display enable output (negative-going)
19	$\overline{TLC}$	transmitted large characters input
20	HIE	high impedance enable input
21	$\overline{BCS}$	big character select input
22	$\overline{T}$/B	top/bottom select input
23	A_4	memory row address outputs (3-state)
24	A_3	
25	A_2	
26	A_1	
27	A_0	
28	RACK	read address clock output

FUNCTIONAL DESCRIPTION

The basic input to the SAB5025D is a 6,0419 MHz clock signal (e.g. from SAA5030). The clock input (F6) is buffered and also available as an output at TR6 to provide a dot rate clock. The signal at F6 is divided by 6 to produce the 1,007 MHz character rate clock at output F1, which is in turn divided by 64 to produce the line period of 63,556 μs. A divide-by-262 or 263 counter, clocked at line rate, produces a field (picture) period of 16,683 ms (average) i.e. 33,366 ms for divide-by-525. The display format is 40 characters per row for 24 rows (1 row is 8 TV lines).

A big character select ($\overline{BSC}$) input is provided and it enables double-height characters (16 TV lines per row) to be displayed. The top or bottom select ($\overline{T}$/B) input must be used in conjunction with $\overline{BCS}$ to select either the top half or bottom half of the page to be displayed on the television screen.

A composite sync ($\overline{AHS}$) output is available for synchronizing the display timebase. A high-impedance enable (HIE) input is included to switch the read address clock (RACK) and the memory row address (A_0 to A_4) outputs into their high-impedance states.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,3	+ 7,5	V
Input voltage range (note 1)	V_I	−0,3	+ 7,5	V
High-impedance state output voltage	V_{OHZ}	−0,3	+ 7,5	V
Open drain output voltage	V_{ODD}	−0,3	+ 13,2	V
Electrostatic charge protection on all inputs and outputs (notes 2 and 3)		1000	—	V
Total power dissipation per package	P_{tot}	—	275	mW
Operating ambient temperature range	T_{amb}	−20	+ 70	°C
Storage temperature range	T_{stg}	−20	+ 125	°C

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Notes to ratings

1. See also characteristics on F6 input and Fig. 10.
2. Equivalent to discharging a 250 pF capacitor through a 1 kΩ series resistor.
3. N.B.: the SAA5025D is not protected against TV tube flash-over.
4. All outputs are TTL compatible.

CHARACTERISTICS

T_{amb} = 25 °C; F6 input frequency = 6,041957 MHz; unless otherwise specified

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4,5	5,0	5,5	V
Supply current	5	I_{DD}	5	–	50	mA
Inputs						
Input leakage currents						
F6	5,5	I_I	0,2	–	10	μA
	0	$-I_I$	–	–	10	μA
FLR, $\overline{TLC}$, FS, HIE, $\overline{BCS}$, $\overline{T}$/B, DE	0 to 5,5	$\pm I_I$	–	–	10	μA
Input capacitance; all inputs	5	C_I	–	–	7	pF
HIGH level input voltages						
F6; see Fig. 10	5	V_{IH}	2,7	–	6,5	V
FLR, $\overline{TLC}$, FS, HIE, $\overline{BCS}$, $\overline{T}$/B, DE	5	V_{IH}	2,0*	–	5,5	V
LOW level input voltage all inputs; see Fig. 10	5	V_{IL}	–	–	0,8*	V
Input rise and fall time F6; see Fig. 6	0 and 2,7	t_r; t_f	–	–	30	ns
Input F6 duty factor (see Fig. 10)	5	δ	40	50	56	%

* These values give no noise immunity.

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Outputs						
Output node capacitance all outputs	5	C_O	–	–	7	pF
Output leakage current high-impedance state; A_0 to A_4, RACK	0 to 5,5	$\pm I_O$	–	–	10	μA
Output leakage current open drain; $\overline{PL}$, $\overline{CBB}$	6	I_O	–	–	10	μA
Output TR6 6,041957 MHz clock						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,75	–	V_{DD}	V
LOW level output voltage I_{OL} = 100 μA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	15	pF
Output rise and fall times see Fig. 7	5	t_r; t_f	–	–	30	ns
Duty factor at 1,5 V level depends on input F6 see F6 data and Fig. 10	5	δ	40	–	60	%
Output F1 1,007 MHz clock						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,75	–	V_{DD}	V
LOW level output voltage I_{OL} = 400 μA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	40	pF
Output rise and fall times see Fig. 7	5	t_r; t_r	–	–	50	ns
Propagation delays from rising edge of TR6; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	7	–	60	ns
Duty factor at 1,5 V level	5	δ	45	50	52	%

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CHARACTERISTICS (continued)

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Output $\overline{AHS}$ see Fig. 6						
HIGH level output voltage $-I_{OH}$ = 200 μA	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage I_{OL} = 1,6 mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times see Fig. 7	5	t_r; t_f	–	–	100	ns
Propagation delay from rising edge of F1; see Fig. 8; LOW-to-HIGH	5	t_{PLH}	0	–	350	ns
Outputs $\overline{GLR}$, $\overline{GLRD}$, $\overline{GLRS}$ see Fig. 3						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage I_{OL} = 0,8 mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	40	pF
Output rise and fall times see Fig. 7	5	t_r t_f	– –	– –	70 50	ns ns
Propagation delay from rising edge of F1; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	0	–	300	ns
Output $\overline{PL}$ see Fig. 3						
LOW level output voltage I_{OL} = 2 mA	5	V_{OL}	0	–	1,0	V
Output load capacitance	5	C_L	–	–	30	pF
Output fall time; see Fig. 7	5	t_f	–	–	100	ns
Propagation delay from rising edge of F1; see Fig. 8; LOW-to-HIGH	5	t_{PLH}	0	–	250	ns

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Output $\overline{CBB}$ see Fig. 3						
LOW level output voltage I_{OL} = 2 mA	5	V_{OL}	0	–	1,0	V
Output load capacitance	5	C_L	–	–	30	pF
Output fall time; see Fig. 7	5	t_f	–	–	200	ns
Propagation delay from rising edge of F1; see Fig. 8; LOW-to-HIGH	5	t_{PLH}	0	–	250	ns
Output CRS						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage I_{OL} = 100 μA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times see Fig. 7	5	t_r; t_f	–	–	1	μs
Output LOSE see Fig. 3						
HIGH level output voltage $-I_{OH}$ = 100 μA	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage I_{OL} = 100 μA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times; see Fig. 7	5	t_r; t_f	–	–	50	ns
Propagation delay from rising edge of F1; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	0	–	1	μs

CHARACTERISTICS (continued)

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Output DEN						
HIGH level output voltage $-I_{OH}$ = 200 μA	5	V_{OH}	2,4	–	–	V
LOW level output voltage I_{OL} = 100 μA	5	V_{OL}	–	–	0,4	V
Output load capacitance	5	C_L	–	–	30	pF
Output rise and fall times	5	t_r; t_f	–	–	50	ns
Propagation delay from rising edge of F1; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	–	–	250	ns
Output DEW see Fig. 4						
HIGH level output voltage $-I_{OH}$ = 200 μA	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage I_{OL} = 1,6 mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	50	pF
Output rise and fall times	5	t_r; t_f	–	–	200	ns
Propagation delay from rising edge of $\overline{CBB}$; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	6,5	6,96	7,5	μs

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Outputs A_0 to A_4 see Fig. 4						
HIGH level output voltage $-I_{OH} = 100\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 1,6$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	85	pF
Output rise and fall times	5	t_r; t_f	–	–	1	μs
Propagation delay from falling edge of $\overline{CBB}$; see Fig. 8; HIGH-to-LOW and LOW-to-HIGH	5	t_{PHL}; t_{PLH}	6,5	–	9,0	μs
Propagation delay from rising edge of HIE to high-impedance state; see Fig. 9	5	t_{PHZ}; t_{PLZ}	0	–	0,9	μs
Propagation delay from falling edge of HIE to normal active state; see Fig. 9	5	t_{PZH}; t_{PZL}	1	–	2,9	μs
Output RACK see Figs 3 and 4						
HIGH level output voltage $-I_{OH} = 100\ \mu A$	5	V_{OH}	2,4	–	V_{DD}	V
LOW level output voltage $I_{OL} = 1,6$ mA	5	V_{OL}	0	–	0,4	V
Output load capacitance	5	C_L	–	–	40	pF
Output rise and fall times see Fig. 7	5	t_r t_f	– –	– –	60 300	ns ns
Propagation delay from falling edge of F1; see Fig. 8; HIGH-to-LOW	5	t_{PHL}	150	–	280	ns
Propagation delay from rising edge of HIE to high-impedance state; see Fig. 9	5	t_{PHZ}; t_{PLZ}	1	–	2,9	μs
Propagation delay from falling edge of HIE to normal active state; see Fig. 9	5	t_{PZH}; t_{PZL}	0	–	0,9	μs

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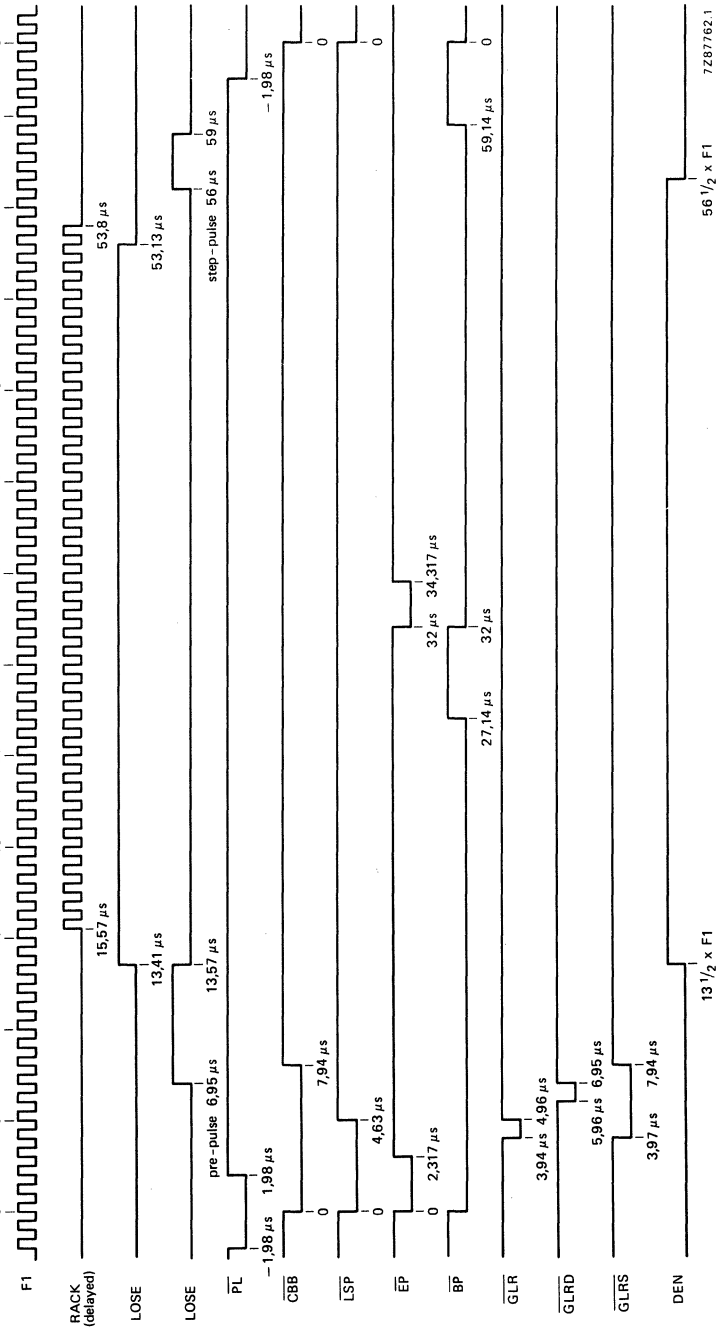


Fig. 3 Timing diagram showing the line-rate signals.

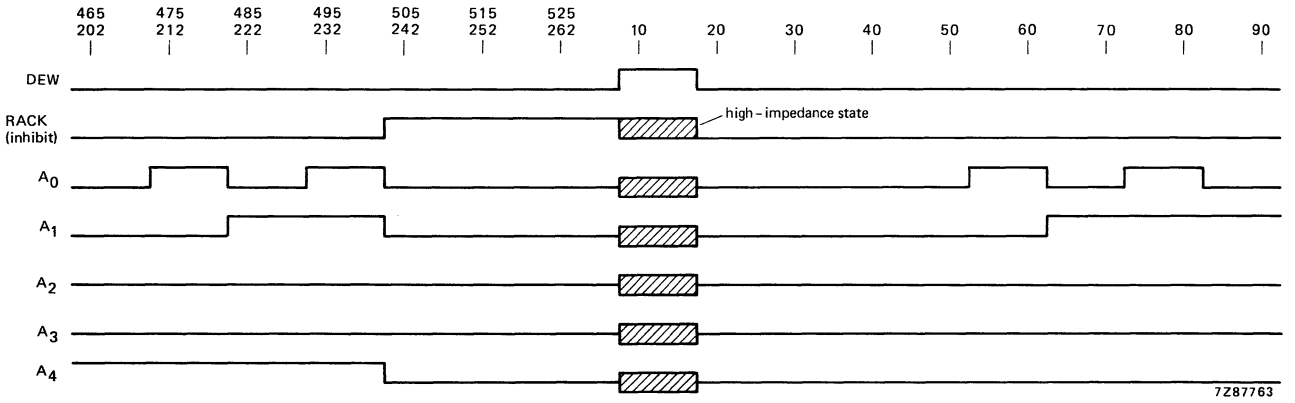


Fig. 4 Timing diagram showing the decoded signals from the field (picture) counters.

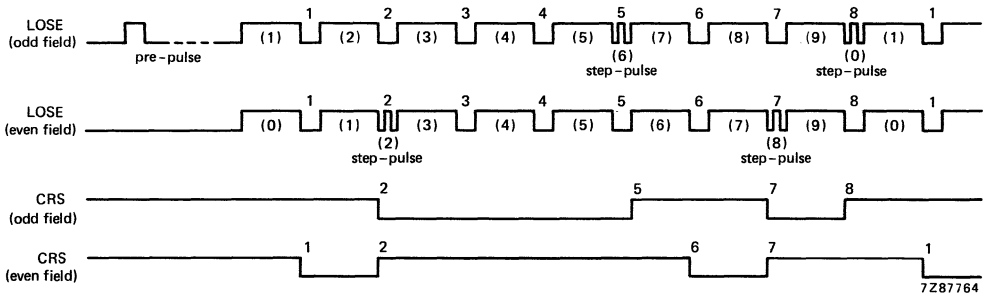


Fig. 5 Timing diagram showing the field-rate signals.

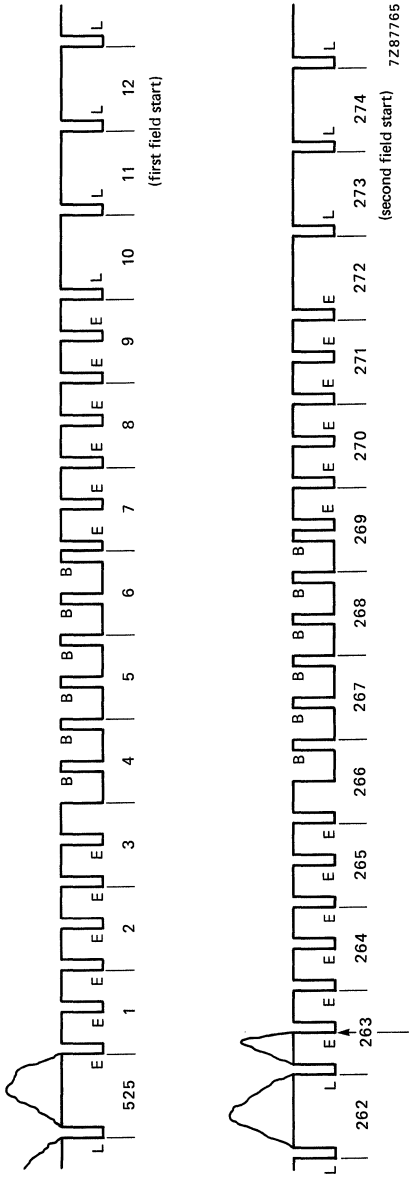
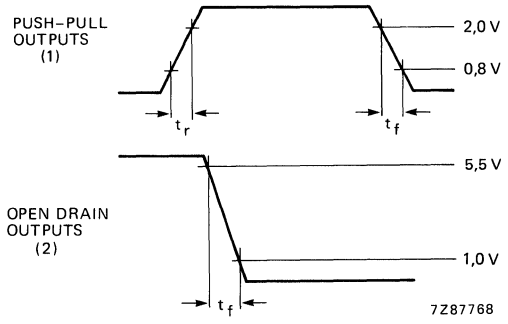


Fig. 6 After hours sync waveforms.

L = line sync pulses (4,2 to 5,1 μs)

E = equalizing pulses (2,29 μs $\pm$ 10%)

B = broad pulses (26,4 to 28 μs)



(1) These outputs will be tested with simulated TTL loads and with the load resistors adjusted such that the correct current conditions are obtained.

(2) These outputs will be tested with 3 kΩ resistors to the +6 V line for outputs $\overline{PL}$ and $\overline{CBB}$.

Fig. 7 Definition of the rise and fall times for the output stages.

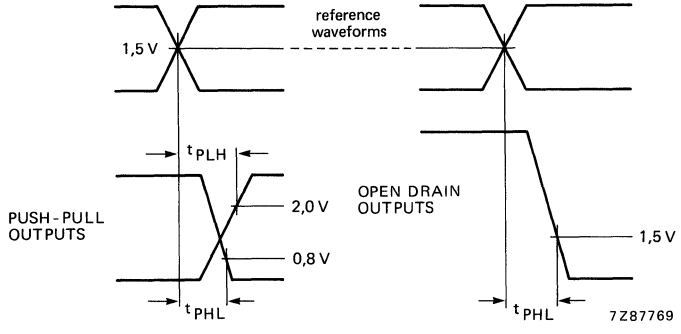


Fig. 8 Definition of the propagation delays for the output stages.

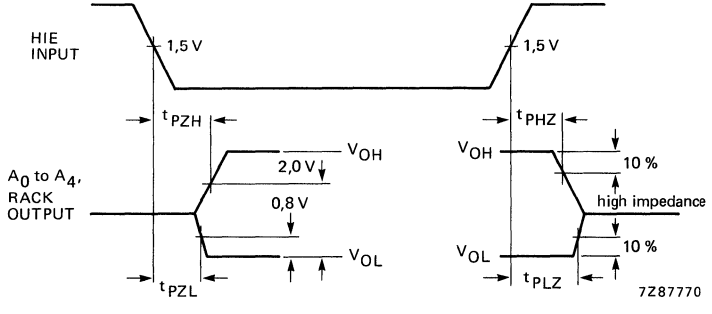


Fig. 9 Definitions of the high-impedance state propagation delay times.

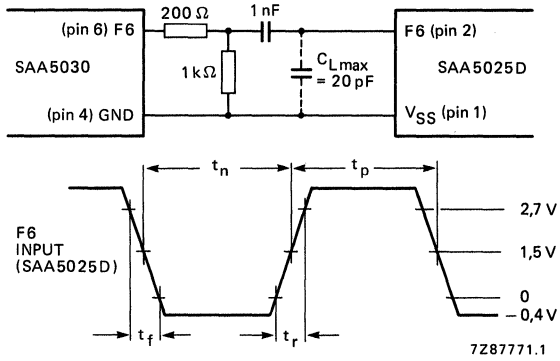


Fig. 10 Recommended 6 MHz interface circuitry between the SAA5025D and the SAA5030 (input F6). With this circuitry the F6 input will be set to a level of approximately −0,4 V in the LOW state. This is acceptable as the internal clamping diode in the F6 input of the SAA5025D provides an adequate current clamp; also shown is the F6 input waveform with the appropriate definitions.

The duty factor is defined as: $\frac{t_p}{t_p + t_n} \times 100\%$

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. **V_{SS} – ground (0 V)**

2. **F6 – 6,041957 MHz clock input**

   Obtained from video processor (SAA5030) or other source. The permissible mark/space ratio is in the range from 56:44 to 40:60 (see also Fig. 10).

3. **TR6 – 6,041957 MHz clock output**

   Dot-rate clock for Teletext character generator SAA5050 series.

4. **F1 – 1,007 MHz clock output**

   Character-rate clock for Teletext character generator SAA5050 series.

5. **$\overline{AHS}$ – after hours sync output**

   A composite sync waveform consisting of a successive sequence of line sync pulses ($\overline{LSP}$) followed by six equalizing pulses ($\overline{EP}$), six broad pulses ($\overline{BP}$) and six equalizing pulses ($\overline{EP}$), and is followed by another sequence of $\overline{LSP}$. This composite sync waveform occurs at the end and beginning of each field/picture (see also Fig. 6).

6. **DE – display enable input**

   A LOW level signal from the Teletext acquisition and control circuit (SAA5040 series) to this input switches output DEN to the LOW state.

7. **FLR – fast line reset input**

   This is the input for a positive-going pulse with a duration of 0,5 μs to 63 μs which resets the line rate counter ($\div$ 64).
   After accepting an FLR pulse, further resets are inhibited for one line period of approximately 63,5 μs.

8. **$\overline{GLRD}$ – general line reset delay output**

   A negative-going pulse with a duration of 993 ns which commences 5,96 μs from the start of each line (see also Fig. 3).

9. **$\overline{GLR}$ – general line reset output**

   A negative-going pulse with a duration of 993 ns which commences 3,97 μs from the start of each line (see also Fig. 3).

10. **$\overline{GLRS}$ – general line reset starting output**

    A negative-going pulse with starting 3,97 μs and ending 7,94 μs from the start of each line (see also Fig. 3).

APPLICATION INFORMATION (continued)

11. $\overline{PL}$ -- phase lock open drain output

This open drain output is used to lock the oscillator in the SAA5030 to the line rate. It is a negative-going pulse with a duration of 3,96 μs which starts at 61,58 μs on one line and it ends at 1,98 μs after the start of the following line (see also Fig. 3).

12. $\overline{CBB}$ – colour burst blanking output

This open-drain output blanks the colour burst in the SAA5030. It is a 7,94 μs negative-going pulse which starts at the beginning of each line (t = 0; see also Fig. 3).

13. FS – field (picture) sync input

This input accepts a positive-going pulse of approximately 160 μs duration. Its leading edge occurs during the second half of line one on even fields (half picture) and correspondingly in odd fields (other half picture). It is ignored during the odd field.

14. CRS – character rounding select output

The output signal starts HIGH during the even field (lines 1 to 263), goes LOW after the 1st LOSE pulse, again HIGH after the 2nd LOSE pulse, then LOW after the 6th LOSE pulse and finally HIGH at the end of the 7th LOSE pulse. This sequence repeats every 8 lines (every row) for the entire display period (see also Fig. 5). For the odd field (lines 264 to 525) CRS starts HIGH, goes LOW after the 2nd LOSE pulse, again HIGH after the 5th LOSE pulse, then LOW after the 7th LOSE pulse and finally HIGH at the end of the 8th LOSE pulse. This sequence repeats every 8 lines (every row) for the entire display period (see also Fig. 5).

15. V_{DD} – positive supply (+ 5 V)

16. LOSE – load output shift register enable output

This is a positive-going output pulse of 39,72 μs duration commencing 13,41 μs from start of line valid during line 47 to 238 inclusive, for the even field. A step-pulse starting at the count of 3 characterrate clock pulses (F1) after the 2nd and 7th LOSE pulses and of the count of 3 character-rate clock pulses repeated every row is included. For the odd field, the LOSE pulse is preceded by a pre-pulse of 7 μs duration commencing 7,41 μs in line 20 and has a step-pulse after the 5th and 8th pulse, repeated every row (see also Fig. 5).

17. DEW – data entry window output

This output defines the period during which data may be extracted from the incoming television signal. It is HIGH during line 7 to 18 inclusive for the even fields and line 270 to 281 inclusive for the odd fields. The positive-going pulse has a duration of 762,67 μs and commences at 6,95 μs from the start of the line (see also Fig. 4).

18. DEN – display enable output

The output pulse is positive-going at 13,5 μs from the start of a line to 56,5 μs and is active during line 47 to 238 inclusive if the DE input is HIGH. If the DE input is LOW, the DEN is held in the LOW state.

19. $\overline{TLC}$ – transmitted large characters input

When this input is LOW, it enables rows of double-height characters to be displayed as required. Large characters descend into the next memory row address location. $\overline{TLC}$ is always HIGH (i.e. small) for the first line of a row, even if it contains large characters.

20. HIE – high impedance enable input

When this input is in the HIGH state it will force the RACK and memory row address output into the high-impedance state. For normal Teletext operation this input should be connected to the DEW output (pin 17).

21. $\overline{BCS}$ – big character select input

For normal size character display this input signal must be HIGH while a LOW gives double-height characters.

22. $\overline{T}$/B – top/bottom select input

When both $\overline{BCS}$ and $\overline{T}$/B are LOW the top half of a page is displayed with double-height characters. If $\overline{T}$/B is HIGH and $\overline{BCS}$ is LOW the bottom half of the page is displayed also with double-height characters.

23 to 27. A_0 to A_4 – memory row address outputs (3-state)

These binary count outputs sequencing from 00000 (count 0) to address 10111 (count 23) for the 40 x 24 format.
The binary count changes every 8 TV lines per row in the display period of line 47 to 238 inclusive for the 24 row display. The count changes between 6,5 μs and 9,0 μs during the line period.

28. RACK – read address clock output

This is the read address clock output to the SAA5045 (GALA) column address counter during the display period. It consists of 39 positive pulses at the 1,007 MHz rate starting at 13,57 μs from the start of the line period with the last negative edge occuring at 51,8 μs. This sequence is active on line 45 to 238 inclusive. RACK is delayed by two F1 clock periods for the whole of the field when input DE is LOW for the whole of line 39. On line 19 to 44 inclusive output RACK is permanently delayed by two F1 clock periods, unaffected by DE.

Note

In the big character top mode the memory row address count is 0 to 11 and in the big character bottom mode the count is 12 to 23.
Each big character row is equal to 16 television lines.

The memory row addresses are held LOW for one line period starting 6,5 μs to 9 μs from the beginning of line 36 which is only valid in the big character bottom mode.

For additional information
consult the Applications Section.

Teletext Video Processor | SAA5030

The SAA5030 is a monolithic bipolar integrated circuit used for teletext video processing. It is one of a package of four circuits to be used in teletext tv data systems. The SAA5030 extracts data and data clock information from the television composite video signal and feeds this to the Acquisition and Control circuit SAA5040. A 6 MHz crystal controlled phase locked oscillator is incorporated which drives the Timing Chain circuit SAA5020. An adaptive sync separator is also provided which derives line and field sync pulses from the input video in order to synchronise the timing chain.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	12	V
Supply current (V_{CC} = 12 V)	I_{CC}	typ.	110	mA
Video input amplitude (sync-white)	$V_{16video(p-p)}$	nom.	2.4	V
Teletext data input amplitude	$V_{16teletext(p-p)}$	nom.	1.1	V
Sync amplitude	$V_{16sync(p-p)}$	nom.	0.7	V
Operating ambient temperature range	T_{amb}		−20 to +70	°C

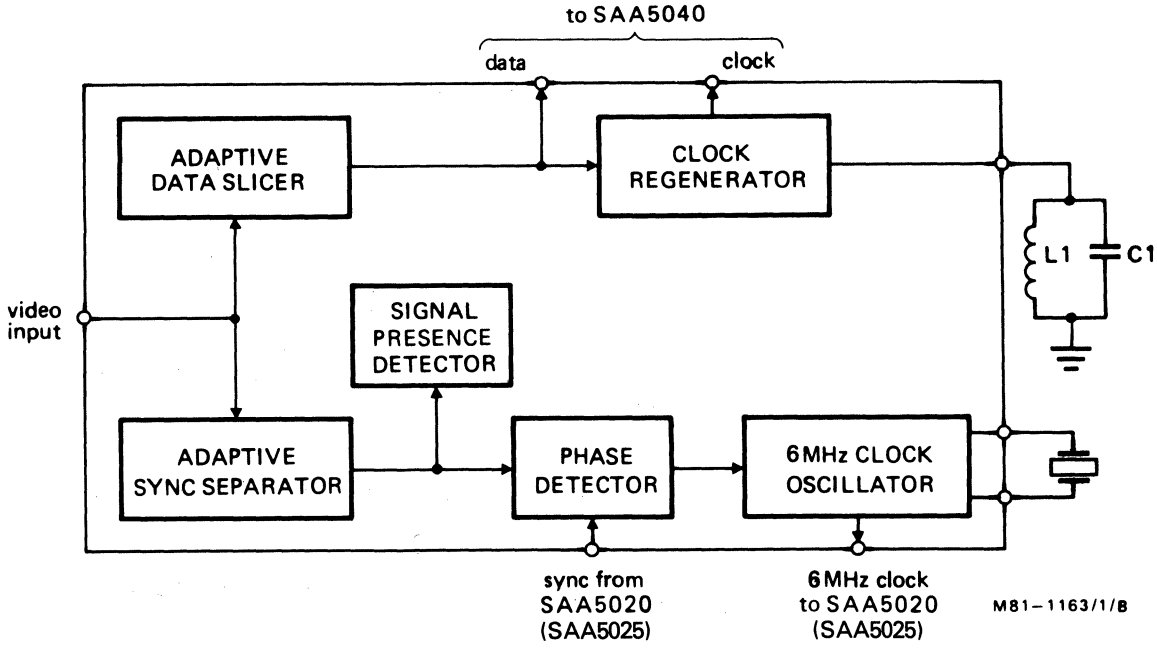


Fig.1 Block diagram

PACKAGE OUTLINE

24-lead DIL; plastic (SOT−101A with internal heat spreader).

PINNING

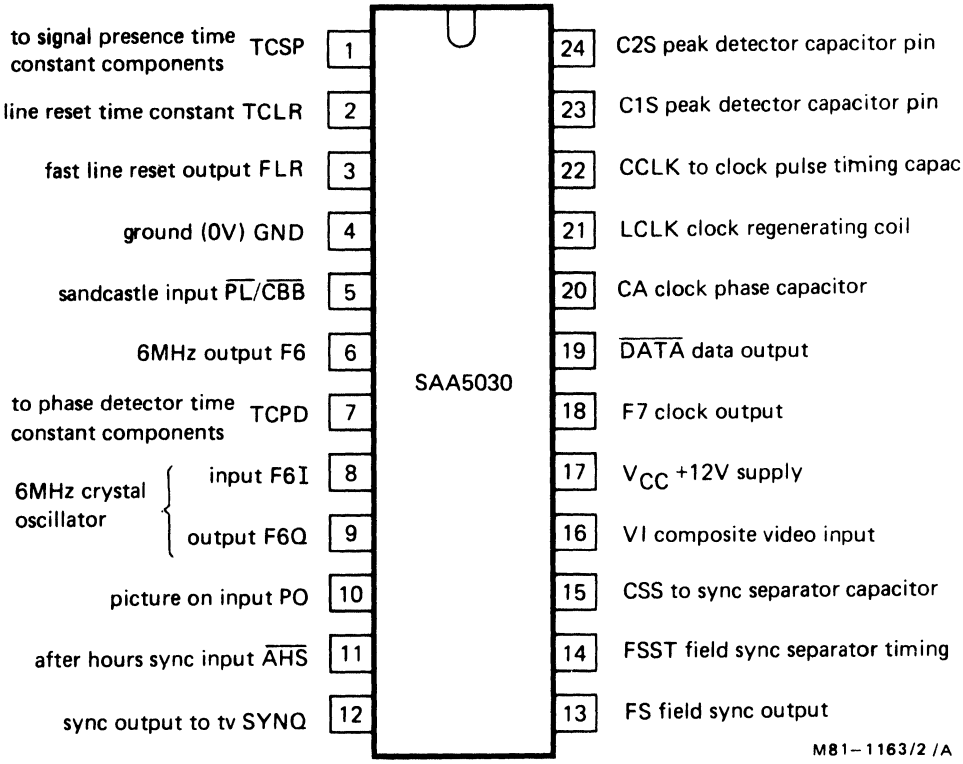


Fig.2 Pinning diagram

5

RATINGS Limiting values in accordance with the Absolute Maximum System. (IEC134)

Voltages

Supply voltage	V_{17-4}	V_{CC}	max.	13.2	V
Input voltages	V_{5-4}	V_I	max.	9.0	V
	V_{10-4}	V_I	max.	V_{CC}	V
	V_{11-4}	V_I	max.	7.5	V

Temperatures

Storage temperature range	T_{stg}	−20 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

CHARACTERISTICS (At T_{amb} = 25 °C, V_{CC} = 12 V and with external components as shown in Fig.3 unless otherwise stated).

		min.	typ.	max.	
Supply voltage	V_{CC}	10.8	12.0	13.2	V
Supply current (V_{CC} = 12.0 V)	I_{CC}	–	110	–	mA
Video input and sync separator					
Video input amplitude (sync to white) Fig.4	$V_{16video(p-p)}$	2.0	1.4	3.0	V
Source impedance, f = 100 kHz	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude	$V_{16sync(p-p)}$	0.07	0.7	1.0	V
Delay through sync separator	t_d	–	0.5	–	μs
Delay between field sync datum at pin 12 and the leading edge of separated field sync at pin 13 (Note 1, Fig.4)	t_d	32	48	62	μs
Field sync output					
V_O (LOW) (I_{13} = 20 μA)	V_{OL}	–	–	0.5	V
V_O (HIGH) ($-I_{13}$ = 100 μA)	V_{OH}	2.4	–	–	V

Crystal controlled phase-locked oscillator

Measured using a crystal with the following specification e.g. catalogue number 4322 143 03241

C_1 = 27.5 fF (typ.)

C_0 = 6.8 pF (typ.)

C_L = 20 pF

Trimability (C_L increased to 30 pF) > 750 Hz

Fundamental ESR < 50 Ω

		min.	typ.	max.	
Frequency	$^fF6$	–	6.0	–	MHz
Holding range		1.5	3.0	–	kHz
Catching range		1.5	3.0	–	kHz
Control sensitivity of phase detector measured as voltage at pin 7 with respect to phase difference between separated syncs and phase lock pulse $\overline{PL}$		–	0.3	–	mV/ns
Control sensitivity of oscillator measured as change in 6 MHz phase shift from pin 8 to pin 9 with respect to voltage at pin 7		–	2	–	deg/mV
Gain of sustaining amplifier, V_{9-8} measured with input voltage of 100 mV_{p-p} and phase detector immobilised		2.5	–	–	V/V
Output voltage of 6 MHz signal at pin 6, measured into 20 pF load capacitance; peak-to-peak value		–	5.5	–	V
Output rise and fall times at pin 6 into 20 pF load	t_r; t_f	–	–	30	ns
Data slicer and clock regenerator					
Teletext data input amplitude, pin 16 (Note 2, Fig.4); peak-to-peak value		–	1.1	–	V
Data input amplitude at pin 16 required to enable amplitude gate flip-flop; peak-to-peak value		–	0.46	–	V
Attack rate, measured at pins 23 and 24 with a step to pin 16 (positive)		–	15	–	V/μs
(negative)		–	9	–	V/μs

5

Data slicer and clock regenerator (continued)		min.	typ.	max.	
Decay rate, measured at pins 23 and 24 with a step input to pin 16		48	100	144	mV/μs
Width of clock coil drive pulses from pin 21 when clock amplitude is not being controlled (Note 3)		–	40	–	ns
Clock hangover measured at pin 18 as the time the clock coil continues ringing after the end of data (Note 4)		20	–	–	Clock Periods
Clock and data output voltages at pins 18 and 19 measured with 20 pF load capacitance; peak-to-peak value		–	5.5	–	V
Output rise and fall times at pins 18 and 19 into 20 pF loads	t_r; t_f	–	–	30	ns
Sandcastle input					
Sandcastle detector thresholds, pin 5					
Phase lock pulse (PL) on		2	–	–	V
Phase lock pulse off		–	–	3	V
Blanking pulse ($\overline{CBB}$) on		4.5	–	–	V
Blanking pulse off		–	–	5.5	V
Dual polarity sync buffer					
After hours sync ($\overline{AHS}$) pulse input pin 11					
Threshold for $\overline{AHS}$ active		1.0	–	–	V
Threshold for $\overline{AHS}$ off		–	–	2.0	V
Picture On (PO) input, pin 10					
Threshold for PO active		–	–	2.0	V
Threshold for PO off		1.0	–	–	V
Sync output, pin 12					
$\overline{AHS}$ output with pin 10 < 1 V (Note 5) peak-to-peak value		–	0.7	–	V
Composite sync output with pin 10 > 2 V (Notes 5 and 6); peak-to-peak value		–	0.7	1.0	V
Output current		–	–	3	mA
Line reset and signal presence detectors					
Schmitt trigger threshold on pin 2 to inhibit line reset output at pin 3 (syncs coincident)		–	6.2	–	V
Schmitt trigger threshold on pin 2 to permit line reset output at pin 3 (syncs non-coincident)		–	7.8	–	V
Line reset output V_{OL} (I_3 = 20 μA)		–	–	0.5	V
Line reset output V_{OH} ($-I_3$ = 100 μA)		2.4	–	–	V
Signal presence Schmitt trigger threshold on pin 2 below which the circuit accepts the input signal		–	6.0	–	V
Signal presence Schmitt trigger threshold on pin 2 above which the input signal is rejected.		–	6.3	–	V

Notes

1. This is measured with the dual polarity buffer external resistor connected to give negative-going syncs. The measurement is made after adjustment of the potential divider at pin 14 for optimum delay.
2. The teletext data input contains binary elements as a two level NRZ signal shaped by a raised cosine filter. The bit rate is 6.9375 M bit/s. The use of odd parity for the 8-bit bytes ensures that there are never more than 14-bit periods between each data transition.
3. This is measured by replacing the clock coil with a small value resistor.
4. This must be measured with the clock coil tuned and using a clock-cracker signal into pin 16. The clock-cracker is a teletext waveform consisting of only one data transition in each byte.
5. With the external resistor connected to the ground rail, syncs are positive-going centred on +2.3 V. With the resistor connected to the supply rail, syncs are negative-going centred on +9.7 V.
6. When the composite sync is being delivered, the level is substantially the same as that at the video input.

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. **Signal presence time constant**

   A capacitor and a resistor connected in parallel between this pin and supply determine the delay in operation of the signal presence detector.

2. **Line reset time constant**

   A capacitor between this pin and supply integrates current pulses from the coincidence detector; the resultant level is used to determine whether to allow FLR pulses (see pin 3).

3. **Fast line reset output (FLR)**

   Positive-going sync pulses are produced at this output if the coincidence detector shows no coincidence between the syncs separated from the incoming video and the $\overline{CBB}$ waveform from the timing chain circuit SAA5020. These pulses are sent to the timing chain circuit and are used to reset its counters, so as to effect rapid lock-up of the phase locked loop.

4. **Ground** (0 V)

5. **Sandcastle input ($\overline{PL}$ and $\overline{CBB}$)**

   This input accepts a sandcastle waveform which is formed from $\overline{PL}$ and $\overline{CBB}$ from the timing chain SAA5020. $\overline{PL}$ is obtained by slicing the waveform at 2.5 V, and this, together with separated sync, are inputs to the phase detector which forms part of the phase locked loop. When the loop has locked up, the edges of $\overline{PL}$ are nominally 2 μs before and 2 μs after the leading edge of separated line syncs.
   CBB is obtained by slicing the waveform at 5 V, and is used to prevent the data slicer being offset by the colour burst.

6. **6 MHz output (F6)**

   This is the output of the crystal oscillator (see pins 8 and 9), and is taken to the timing chain circuit SAA5020 via a series capacitor.

7. **Phase detector time constant**

   The integrating components for the phase detector of the phase locked loop are connected between this pin and supply.

APPLICATION DATA (continued)

8, 9. **6 MHz crystal**

A 6 MHz crystal in series with a trimmer capacitor is connected between these pins. It forms part of an oscillator whose frequency is controlled by the voltage on pin 7, which forms part of the phase locked loop.

10. **Picture On input (PO)**

The PO signal from the acquisition and control circuits SAA5040 Series is fed to this input and is used to determine whether the input video (pin 16) or the $\overline{\text{AHS}}$ waveform (pin 11) appears at pin 12.

11. **After hours sync ($\overline{\text{AHS}}$)**

A composite sync waveform $\overline{\text{AHS}}$ is generated in the timing chain circuit SAA5020 and is used to synchronise the tv (see pin 10).

12. **Sync output to tv**

Either the input video of $\overline{\text{AHS}}$ is available at this output dependent on whether the PO signal is HIGH or LOW. In addition either signal may be positive-going or negative-going, dependent on whether the load resistor at this output is connected to ground or supply.

13. **Field sync output (FS)**

A pulse, derived from the input video by the field sync separator, which is used to reset the line counter in the timing chain circuit SAA5020.

14. **Field sync separator timing**

A capacitor and adjusting network is connected to this pin and forms the integrator of the field sync separator.

15. **Sync separator capacitor**

A capacitor connected to this pin forms part of the adaptive sync separator.

16. **Composite video input (VI)**

The composite video is fed to this input via a coupling capacitor.

17. **Supply voltage (+12 V)**

18. **Clock output**

The regenerated clock, after extraction from the teletext data, is fed out to the acquisition and control circuits SAA5040 Series via a series capacitor.

19. **Data output**

The teletext data is sliced off the video waveform, squared up and latched within the SAA5030. The latched output is fed to the acquisition and control circuits SAA5040 Series via a series capacitor.

20. **Clock decoupling**

A 1 nF capacitor between pin 20 and ground is required for clock decoupling.

21. **Clock regenerator coil**

A high-Q parallel tuned circuit is connected between this pin and an external potential divider. The coil is part of the clock regeneration circuit (see pin 22).

APPLICATION DATA (continued)

22. **Clock pulse timing capacitor**

Short pulses are derived from both edges of data with the aid of a capacitor connected to this pin. The resulting pulses are fed, as a current, into the clock coil connected to pin 21. Resulting oscillations are limited and taken to the acquisition and control circuits SAA5040 Series via pin 18.

23, 24 **Peak detector capacitors**

The teletext data is sliced with an automatic data slicer whose slicing level is the mid-point of two peak detectors working on the video signal. Storage capacitors are connected to these pins for the negative and positive peak detectors.

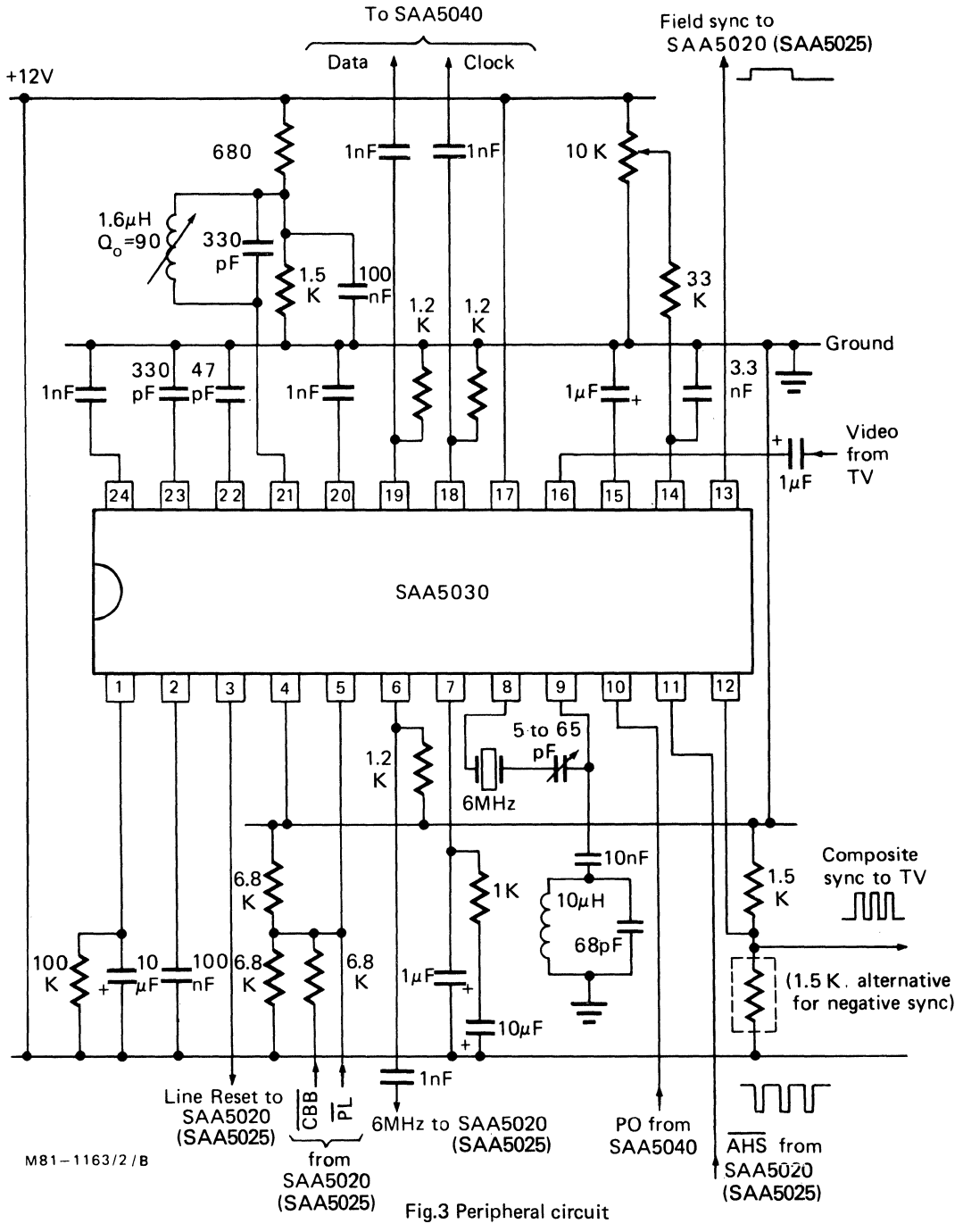


Fig.3 Peripheral circuit

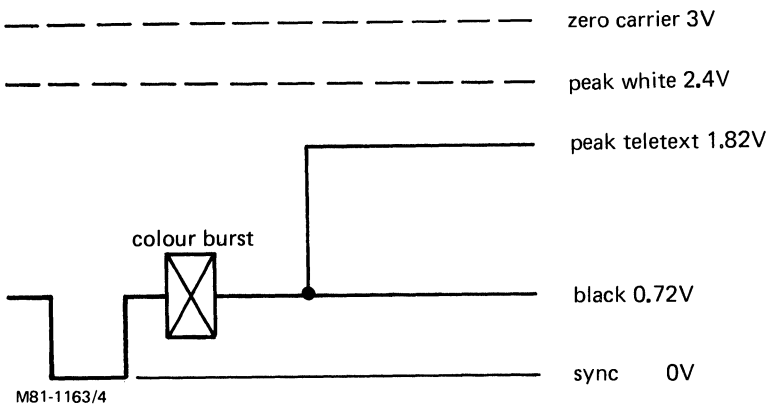


Fig.4 Part of teletext line, with burst showing nominal levels.

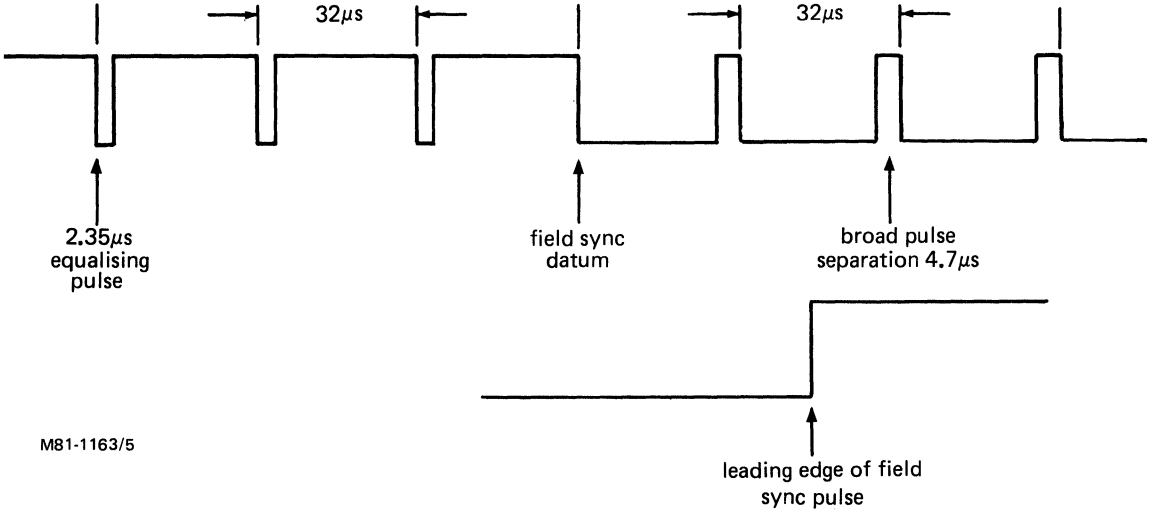


Fig.5 Detail of idealised composite sync waveform.

GENERAL

The SAA5040A, SAA5040B, SAA5040C, SAA5041, SAA5042 and SAA5043 form the SAA5040 series of MOS N-channel integrated circuits. They perform the control, data acquisition and data routing functions of the teletext system. The circuits differ in the on-screen display that is provided and in the decoding of the remote control commands. The functions of the circuits are detailed in Tables 1, 2 and 3; throughout the remainder of the data the SAA5040 is referred to when the complete series of the circuits is being described.

The SAA5040 is a 28-lead device which receives serial teletext data and clock signals from the remote control systems incorporating the SAA5012 or SAB3022, SAB3023 decoder circuits. The SAA5040 selects the required page information and feeds it in parallel form to the teletext page memory.

The SAA5040 works in conjunction with the SAA5020 timing chain and the SAA5050 series of character generators.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	80	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

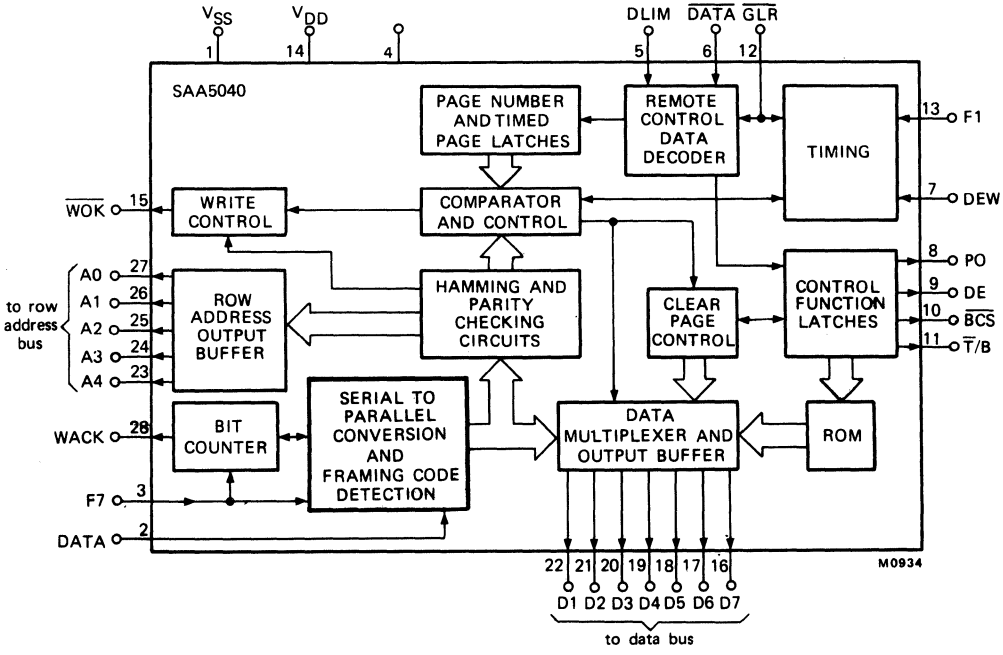


Fig.1 Block diagram.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117)

PINNING

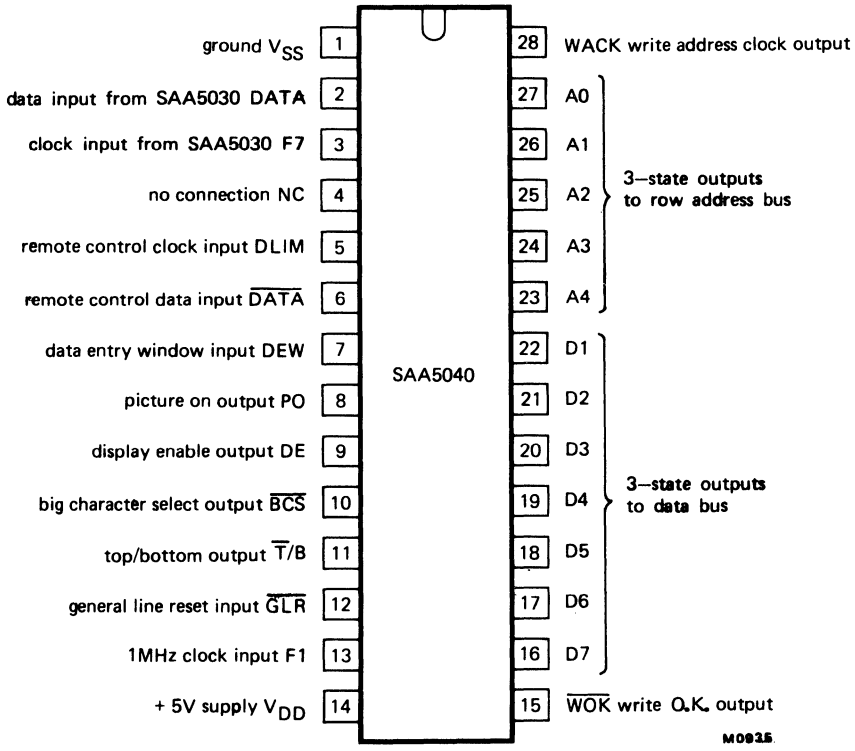


Fig.2 Pinning diagram.

DESCRIPTION

The circuit consists of two main sections.

a) Data acquisition section

The basic input to this section is the serial teletext data stream DATA from the SAA5030 video processor circuit. This data stream is clocked at a 6.9375 MHz clock rate (F7) from the SAA5030. The incoming data stream is processed and sorted so that the page of data selected by the user is written as 7-bit parallel words into the system memory. Hamming and parity checks are performed on the incoming data to reduce errors. Provision is also made to process the control bits in the page header.

b) Control section

The basic input to this section is the 7-bit serial data ($\overline{\text{DATA}}$) from the remote control decoder circuit such as the SAA5012 or SAB3012. This is clocked by the DLIM signal.
The remote control commands are decoded and the control functions are stored.
Full details of the remote control commands used in the various SAA5040 series options are given in Tables 1, 2 and 3 below. The control section also writes data into the page memory independently of the data acquisition section. This gives an on-screen display of certain user-selected functions such as page number and programme name.
The 3-state data and address outputs to the system memory are set to high impedance state if certain remote control commands are received (e.g. viewdata mode). This is to allow another circuit to access the memory using the same address and data lines. The address lines are also high impedance while the acquisition and control circuit is not writing into the memory.
Further information on the control of the complete teletext system is available.
The circuit is designed in accordance with the September 1976 Broadcast Teletext specification published by BBC/IBA/BREMA.
A typical circuit diagram of a teletext decoder is shown in Fig.7.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS devices").

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Voltages (with respect to pin 1)

		min.	max.	
Supply voltage (pin 14)	V_{DD}	−0.3	7.5	V
Input voltage (all inputs)	V_I	−0.3	7.5	V
Output voltage (pin 8)	V_{O8}	−0.3	13.2	V
Output voltage (all other outputs)	V_O	−0.3	7.5	V
Temperatures				
Storage temperature range	T_{stg}		−20 to +125	°C
Operating ambient temperature range	T_{amb}		−20 to +70	°C

CHARACTERISTICS

		min.	typ.	max.	
Supply voltage (pin 14)	V_{DD}	4.5	–	5.5	V
The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.					
Supply current	I_{DD}	–	80	120	mA
Inputs					
F7 DATA (pin 2), **F7 CLOCK** (pin 3)					
Input voltage; HIGH	V_{IH}	3.5	–	5.5	V
Input voltage; LOW Note 1	V_{IL}	–	–	0.5	V
Rise time	t_r	–	–	30	ns
Fall time	t_f	–	–	30	ns
Input resistance (measured at 4 V)	R_I	2	–	18	MΩ
Input capacitance	C_I	–	–	7	pF
F1 (pin 13)					
Input voltage; HIGH	V_{IH}	2.4	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Rise time	t_r	–	–	50	ns
Fall time	t_f	–	–	30	ns
Input capacitance	C_I	–	–	7	pF
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
All other inputs					
DLIM (pin 5), **$\overline{\text{DATA}}$** (pin 6), **DEW** (pin 7), **$\overline{\text{GLR}}$** (pin 12)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input capacitance	C_I	–	–	7	pF
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Outputs					
DE (pin 9), **$\overline{\text{BCS}}$** (pin 10), **$\overline{\text{T}}$/B** (pin 11) (with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 400 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH $-I_{OH}$ = 50 μA for pin 9 $-I_{OH}$ = 30 μA for pin 10 $-I_{OH}$ = 20 μA for pin 11	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time	t_r	–	–	10	
Output voltage fall time	t_f	–	–	1	μs
Output capacitance	C_O	–	–	7	pF
Output current with output in HIGH state (V_O = 0.5 V)	$-I_O$	50	–	500	μA

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CHARACTERISTICS Continued

		min.	typ.	max.	
PO (pin 8) (with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 140 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 50 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	10	μs
Output capacitance	C_O	–	–	7	pF
Output current with output in HIGH state (V_O = 0.5 V)	$-I_O$	50	–	500	μA
D1 to D7 (pins 16 to 22) (3-state)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH (I_{OH} = −100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	100	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$\pm I_{ORoff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF
$\overline{\text{WOK}}$ (pin 15) (3-state with internal pull-up to V_{DD})					
Output voltage; LOW (I_{OL} = 400 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time (C_L = 80 pF) (Note 3)	t_r	–	–	50	ns
Output voltage fall time (C_L = 80 pF) (Note 3)	t_f	–	–	100	ns
Output current with 3-state 'OFF' (V_O = 0.5 V)	$-I_{ORoff}$	80	–	500	μA
Output capacitance	C_O	–	–	7	pF
WACK (pin 28) (3-state)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output voltage rise time (C_L = 40 pF) (Note 3)	t_r	–	–	50	ns
Output voltage fall time (C_L = 40 pF) (Note 3)	t_f	–	–	300	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$\pm I_{ORoff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF
A0 to A2 (pins 25 to 27) (3-state)					
Output voltage; LOW (I_{OL} = 200 μA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 90 pF) (Note 3)	t_r, t_f	–	–	300	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$\pm I_{ORoff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF

CHARACTERISTICS (Continued)

Outputs

		min.	typ.	max.	
A3 and A4 (pins 23 and 24) (3-state)					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall time (C_L = 40 pF) (Note 3)	t_r, t_f	–	–	300	ns
Output leakage current in 'OFF' state (V_O = 0 to 5.5 V)	$+I_{ORoff}$	–	–	10	μA
Output capacitance	C_O	–	–	7	pF
TIMING CHARACTERISTICS					
Teletext Data and Clock (F7 DATA + F7 CLOCK) (Note 2 and Fig.3)					
F7 Clock cycle time	TF_7	144	–	–	ns
F7 Clock duty cycle (HIGH to LOW)		30	–	70	%
F7 Clock to data set-up time	t_{SU}	–	60	–	ns
F7 Clock to data hold time	t_{HOLD}	–	40	–	ns
Control $\overline{\text{DATA}}$ and Clock ($\overline{\text{DATA}}$ + DLIM) (Note 3 and Fig.4)					
DLIM Clock HIGH time	t_{CH}	6.5	8	Note 4	μs
DLIM Clock LOW time	t_{CL}	3.5	8	60	μs
DLIM to DATA set-up time	t_{SU}	0	14	–	μs
DLIM to DATA hold time	t_{HOLD}	8	14	–	μs
Writing Teletext data into memory during DEW (Fig.5)					
WACK cycle time	T_{WACK}	1150	–	–	ns
WACK rising edge to $\overline{\text{WOK}}$ falling edge	t_{AWW}	250	–	450	ns
WACK rising edge to $\overline{\text{WOK}}$ rising edge	t_{WRW}	150	–	310	ns
$\overline{\text{WOK}}$ pulse width	t_{WPD}	300	–	–	ns
Data output set-up time	t_{DW}	330	–	–	ns
Data output hold time	t_{DH}	0	–	–	ns
Row address set-up time before first $\overline{\text{WOK}}$	t_{RAW}	190	–	–	ns
Row address valid time after last $\overline{\text{WOK}}$	t_{RWR}	0	–	–	ns

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TIMING CHARACTERISTICS

		min.	typ.	max.	
Writing Header information into memory during tv line 40 (Fig.6)					
This arrangement is a combined phasing of the SAA5040 and the SAA5020 and is therefore referred to F1 input. The first $\overline{WOK}$ is related to F1 No 14½ from the SAA5020					
F1 Clock cycle time		1000	–	–	ns
Time from F1 to $\overline{WOK}$ falling edge	t_{WF}	300	–	500	ns
Time from F1 to $\overline{WOK}$ rising edge	t_{FW}	0	–	120	ns
Data output set-up time	t_{DW}	330	–	–	ns
Data output hold time	t_{DH}	0	–	–	ns

Notes

1. These inputs may be a.c. coupled. Minimum rating is −0.3 V but the input may be taken more negative if a.c. coupled.
2. Transition times measured between 0.5 and 3.5 volt levels. Delay times are measured from 1.5 V level.
3. Transition times measured between 0.8 and 2.0 volt levels. Delay times are measured from 1.5 V level.
4. There is no maximum DLIM cyle time provided the DLIM duty cycle is such that $t_{CLmax.}$ requirement is not exceeded.

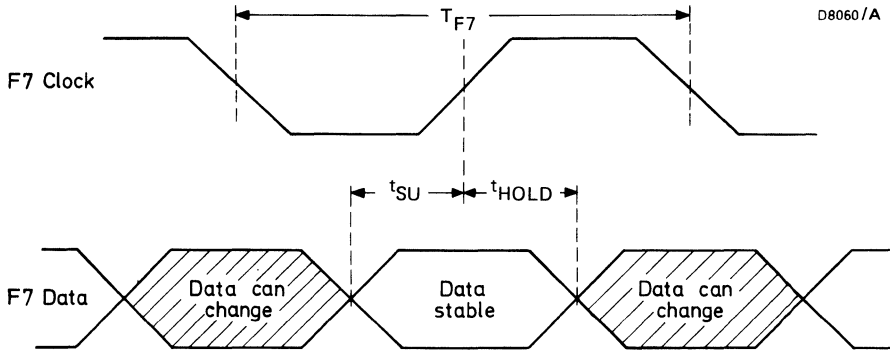


Fig.3 Teletext data timing

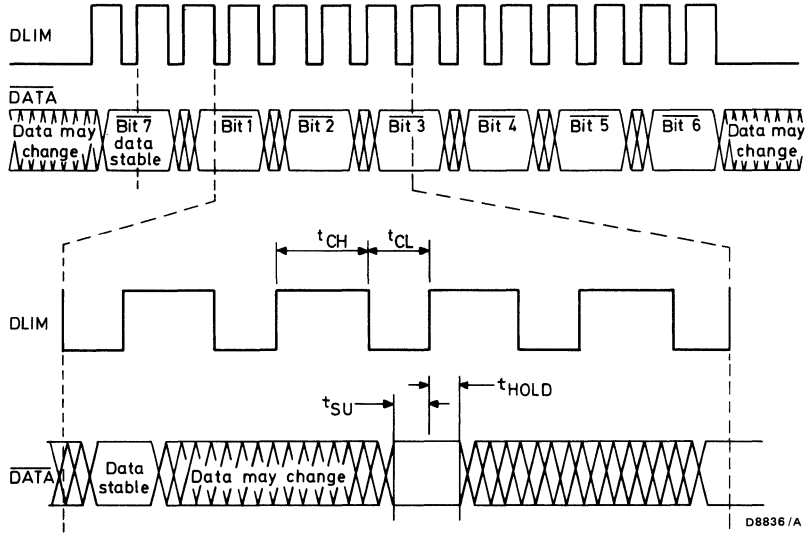


Fig.4 Remote control data input timing

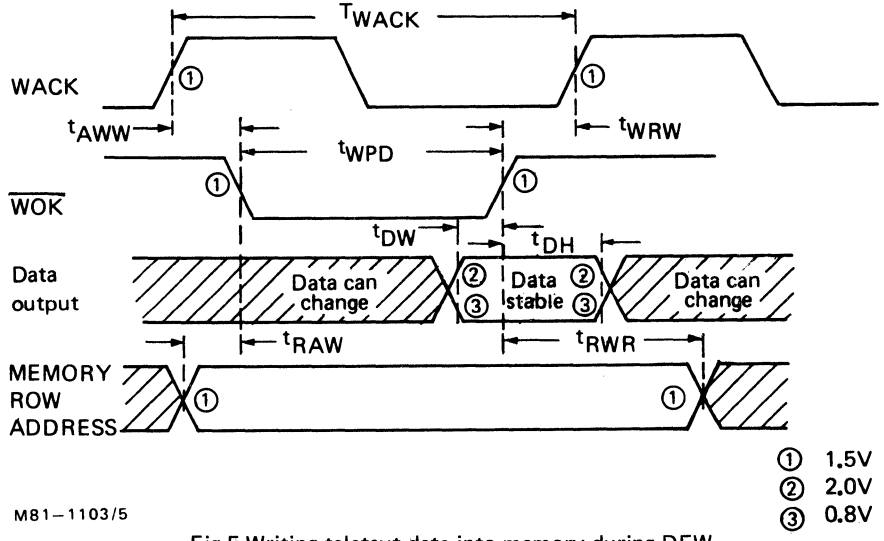


Fig.5 Writing teletext data into memory during DEW

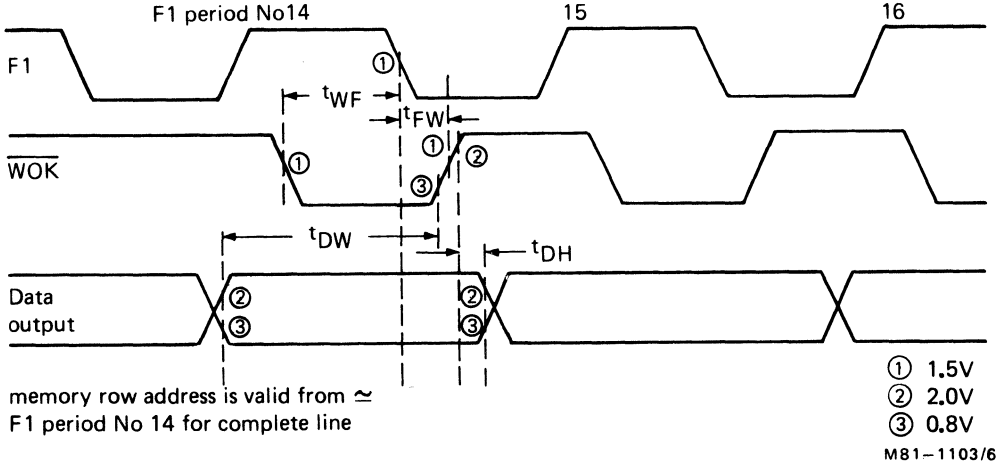


Fig.6 Writing data into memory during tv line 40

APPLICATION DATA

The function is quoted against the corresponding pin number

Pin No.

1. V_{SS} Ground - 0 V
2. **DATA Data input from SAA5030**

   This input is a serial data stream of broadcast teletext data from the SAA5030 video processor, the data being at a rate of 6.9375 MHz.
   This input from the SAA5030 is a.c. coupled with internal d.c. restoration of the signal levels.
3. **F7 Clock input from SAA5030**

   This input is a 6.9375 MHz clock from the SAA5030 video processor which is used to clock the teletext data acquisition circuitry. The positive edge of this clock is nominally at the centre of each teletext data bit.
   This input from the SAA5030 is a.c. coupled with internal d.c. restoration of the signal levels.
5. **DLIM Remote control clock input**

   This input from the remote control receiver decoder is used to clock remote control data into the SAA5040. The positive-going edge of every second clock pulse is nominally in the centre of each remote control data bit.
6. **$\overline{\text{DATA}}$ Remote control data**

   This input is a 7-bit serial data stream from the remote control receiver decoder.
   This data contains the teletext and viewdata remote control user functions. The nominal data rate is 32 μs/bit. The remote control commands used in the SAA5040 series are shown in Tables 1, 2 and 3.
7. **DEW Data entry window**

   This input from the SAA5020 Timing Chain defines the period during which received teletext data may be accepted by the SAA5040. This signal is also used to enable the 5 memory address outputs (pins 23 to 27) and the 7-bit parallel data outputs (pins 16 to 22).
8. **PO Picture On**

   This output to the SAA5012, SAA5030 and SAA5050 circuits is a static level used for the selection of tv picture video 'on' or 'off'. The output is HIGH for tv picture 'ON', LOW for tv picture 'OFF'. The output has an internal pull-up to V_{DD}.
9. **DE Display enable**

   This output to the SAA5050 teletext character generator is used to enable the teletext display. The output is HIGH for display enabled, LOW for display disabled.
   The output is also forced to the LOW state during the DEW and tv line 40 periods and when a teletext page is cleared.
   The output has an internal pull-up to V_{DD}.
10. **$\overline{\text{BCS}}$ Big character select**

    This output to the SAA5020 timing chain and to the SAA5050 character generator is used to select double height character format under user control. The output is HIGH for normal height characters, LOW for double height characters. It is also forced to the HIGH state on page clear. The output has an internal pull-up to V_{DD}.
11. **$\overline{\text{T}}$/B Top/bottom**

    This output to the SAA5020 timing chain is used to select whether top or bottom half page is being viewed. The output is HIGH for bottom half page and LOW for top half page. It is also forced to the LOW state on page clear.
    The output has an internal pull-up to V_{DD}.

APPLICATION DATA

12. **$\overline{\text{GLR}}$ General line reset**

This input from the SAA5020 timing chain is used as a reset signal for internal control and display counter.

13. **F1**

This input is a 1 MHz clock signal from the SAA5020 timing chain used to clock internal remote control processing and encoding circuits.

14. **V_{DD} +5 V Supply**

This is the power supply input to the circuit.

15. **$\overline{\text{WOK}}$ Write O.K.**

This 3-state output signal to the system memory is used to control the writing of valid data into the system memory. The signal is LOW to write, and is in the high impedance state when viewdata is selected. The three-state buffer is enabled at the same time as the data outputs (see below). An internal pull-up device prevents the output from floating into the LOW state when the 3-state buffer is OFF.

16, 17, 18, 19, 20, 21, 22 **D7 to D1, Data outputs**

These 3-state outputs are the seven bit parallel data outputs to the system memory. The outputs are enabled at the following times:—

a) During the data entry window (DEW) to write teletext data into the memory. The data rate is 867 kbytes per second and is derived from the teletext data clock.

b) During tv line 40 for encoded status information about user commands (e.g. programme number), to be written into the memory. This period is known as EDIL (encoded data insertion line). The data rate is 1 Mbyte per second and is derived from the 1 MHz display clock F1.

c) When the page is cleared. In this case the data output is forced to the space code (0100000) during the display period for one field. This data is held at the space code from either tv line 40 (if page clear is caused by user command), or the received teletext data line causing the clear function, until the start of the data entry window (DEW) of the next field.

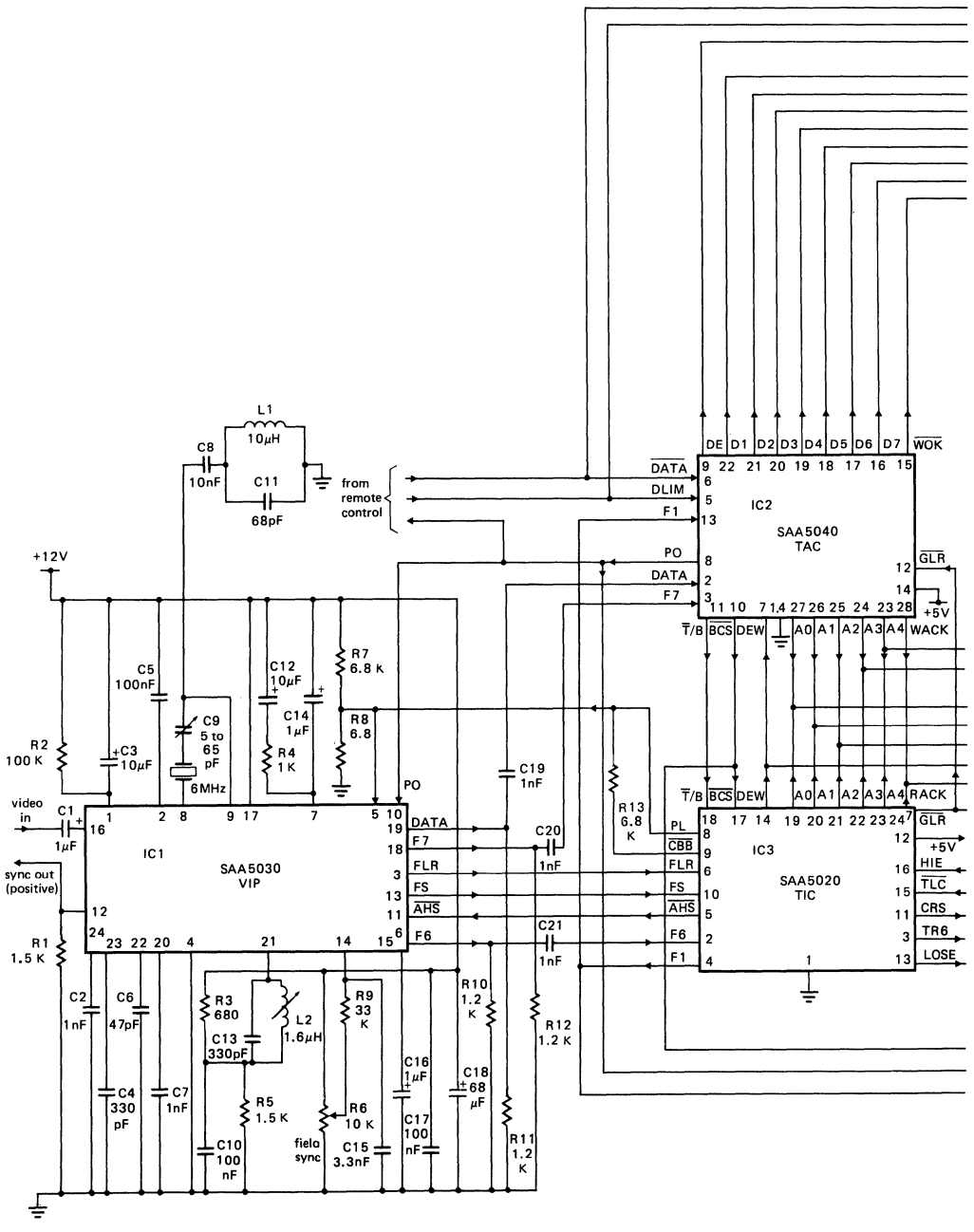
23, 24, 25, 26, 27 **A4 to A0 Memory addresses**

These 3-state outputs are the 5-bit row address to the page memory. This address specifies in which of 24 rows the teletext data is to be written. The outputs are enabled during the data entry period (DEW).

28. **WACK Write address clock**

This 3-state output is used to clock the memory address counter during the data entry period (DEW). The output is enabled only during this period. The positive-going edge of WACK is used to clock the address counter.

Teletext Acquisition and Control Circuit SAA5040



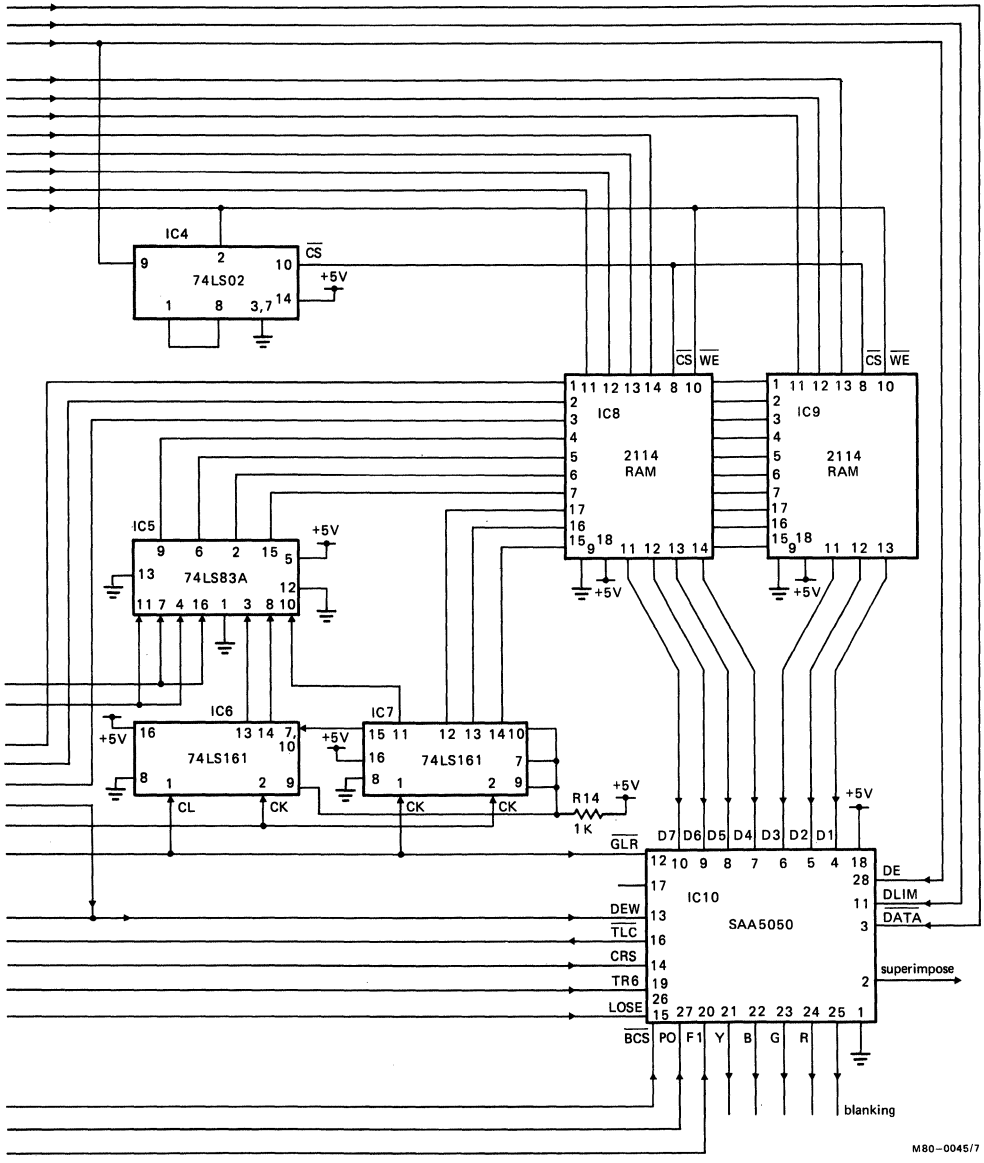


Fig.7 Typical circuit diagram of a teletext decoder.

TABLE 1 (Note 8)

Remote control commands used in the SAA5040A/SAA5040B/SAA5040C/SAA5043

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$) (Note 7)	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$) (Note 7)
0	0	0	0	0	RESET (Note 1)	
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1	TV/ON Gives programme display.	
0	0	1	0	0	STATUS Gives programme display.	STATUS Programme/header display (Note 6)
0	0	1	0	1		HOLD Stops reception of teletext. (Note 9)
0	0	1	1	0		
0	0	1	1	1	TIME Gives time display.	DISPLAY CANCEL (Note 3)
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		
0	1	0	1	1		
0	1	1	0	0		TAPE Resets to small characters.
0	1	1	0	1		
0	1	1	1	0		TIMED PAGE OFF
0	1	1	1	1		TIMED PAGE ON
1	0	0	0	0	PROGRAMMES (Note 2)	NUMBERS (Notes 4 and 6) 1
1	0	0	0	1		2
1	0	0	1	0		3
1	0	0	1	1		4
1	0	1	0	0		5
1	0	1	0	1		6
1	0	1	1	0		7
1	0	1	1	1		8
1	1	0	0	0		9
1	1	0	0	1		0
1	1	0	1	0		SMALL CHARACTERS
1	1	0	1	1		LARGE CHARACTERS TOP HALF PAGE
1	1	1	0	0		LARGE CHARACTERS BOTTOM HALF PAGE
1	1	1	0	1		
1	1	1	1	0		SUPERIMPOSE (Note 6)
1	1	1	1	1		TELETEXT/ON (Note 5)

5

Notes for Table 1

1. Reset clears the page memory, sets page number to 100 and time code to 00.00 and resets timed page and display cancel modes.
2. Programme names are displayed for 5 s in a box at the top left of the screen in large characters. Programme commands clear the page memory except in timed page mode.

The following boxed information is displayed.

REMOTE CONTROL COMMAND b_5 b_4 b_3 b_2 b_1	SAA5040A	SAA5040B	SAA5040C	SAA5043
1 0 0 0 0	BBC1	Gives no status box	BBC1	Ch 1
1 0 0 0 1	BBC2		ITV	Ch 2
1 0 0 1 0	ITV		BBC2	Ch 3
1 0 0 1 1	4		BBC1	Ch 4
1 0 1 0 0	5		ITV	Ch 5
1 0 1 0 1	6		VTR	Ch 6
1 0 1 1 0	7		BBC1	Ch 7
1 0 1 1 1	VCR		ITV	Ch 8
1 1 0 0 0	9		BBC2	Ch 9
1 1 0 0 1	10		BBC1	Ch 0
1 1 0 1 0	11		ITV	Ch 10
1 1 0 1 1	12		VTR	Ch 11

3. Display cancel removes the text and restores the television picture. The device then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The full page of text can then be displayed when required using the teletext/on command.
4. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested the page header turns green and the page numbers roll until the new page is captured.
5. The teletext/on command resets display cancel, hold and superimpose modes.
6. Status, timed page on, timed page off, numbers, superimpose and teletext/on commands all reset to top half page and produce a box round the header for 5 s. This allows the header to be seen if the television picture is on (e.g. newsflash or display cancel modes).
7. In viewdata mode ($b_7 = b_6 = 1$) the device is disabled and teletext cannot be received. All 3-state outputs are high impedance.
8. Table 1 shows code required for functions specified. The device requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.
9. When hold node is selected 'HOLD' is displayed in green at the top right of the screen.
10. A 'P' is displayed before the page number at the top left of the screen (e.g. P123).

TABLE 2 (Note 9)

Remote control commands used in the SAA5041

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$) (Note 8)	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$) (Note 8)
0	0	0	0	0		
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1		
0	0	1	0	0	TIME Gives time display.	STATUS Gives header and time display. (Note 6)
0	0	1	0	1		TIMED PAGE On/off toggle function.
0	0	1	1	0		
0	0	1	1	1		
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		
0	1	0	1	1		
0	1	1	0	0		
0	1	1	0	1		
0	1	1	1	0		
0	1	1	1	1		TELETEXT RESET (Note 1)
1	0	0	0	0		0
1	0	0	0	1		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
1	0	1	0	1	PROGRAMMES (Note 10)	NUMBERS 5
1	0	1	1	0		(Notes 2 and 7) 6
1	0	1	1	1		7
1	1	0	0	0		8
1	1	0	0	1		9
1	1	0	1	0		SMALL CHARACTERS
1	1	0	1	1		LARGE CHARACTERS Top/bottom toggle function
1	1	1	0	0		HOLD Stops reception of teletext - toggle function (Note 3)
1	1	1	0	1		DISPLAY CANCEL (Note 4)
1	1	1	1	0		SUPERIMPOSE
1	1	1	1	1		NORMAL DISPLAY (Note 5)

5

Notes for Table 2

1. The teletext reset command clears the page memory, selects Page 100, goes to small characters and resets hold, timed page and display cancel modes.

2. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested the page header turns green and the page numbers roll until the new page is captured.

3. When hold mode is selected 'HALT' is displayed in green at the top right of the screen.

4. Display cancel removes the text and restores the television picture. The SAA5041 then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The full page of text can then be displayed when required using the normal display command.

5. The normal display command resets display cancel, hold and superimpose modes.

6. Status, timed page, numbers, hold, superimpose and normal display commands all reset to top half page and produce a box round the header for five seconds. This allows the header to be seen even if the television picture is on (e.g. newsflash or display cancel modes).

7. An 'S' is displayed before the page number at the top left of the screen (e.g. S123).

8. In viewdata mode ($b_7 = b_6 = 1$) the SAA5041 is disabled and teletext cannot be received. All 3-state outputs are high impedance.

9. Table 2 shows code required for functions specified. The SAA5041 requires the inverse of these codes i.e. b_7 to b_1. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.

10. Clear Memory occurs except in Timed Page Mode.

TABLE 3 (Note 9)

Remote control commands used in the SAA5042

CODE b_5	b_4	b_3	b_2	b_1	TELEVISION MODE ($b_7 = b_6 = 0$) (Note 8)	TELETEXT MODE ($b_7 = 1$, $b_6 = 0$) (Note 8)
0	0	0	0	0	RESET (Note 1)	
0	0	0	0	1		
0	0	0	1	0		
0	0	0	1	1		
0	0	1	0	0		STATUS Gives header and time display. (Note 6)
0	0	1	0	1		HOLD Stops reception of teletext - toggle function (Note 3)
0	0	1	1	0		
0	0	1	1	1	TIME Gives time display	
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		SMALL CHARACTERS
0	1	0	1	1		
0	1	1	0	0		LARGE CHARACTERS TOP HALF PAGE
0	1	1	0	1		LARGE CHARACTERS BOTTOM HALF PAGE
0	1	1	1	0		DISPLAY CANCEL/RECALL (Note 4)
0	1	1	1	1		DISPLAY RECALL
1	0	0	0	0	PROGRAMMES (Note 10)	NUMBERS (Notes 2 and 7) 0
1	0	0	0	1		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
1	0	1	0	1		5
1	0	1	1	0		6
1	0	1	1	1		7
1	1	0	0	0		8
1	1	0	0	1		9
1	1	0	1	0		TIMED PAGE On/Off toggle function
1	1	0	1	1		CLEAR MEMORY
1	1	1	0	0		LONG TERM STORE/SMALL CHARACTERS
1	1	1	0	1		
1	1	1	1	0		SUPERIMPOSE
1	1	1	1	1		TELETEXT/ON (Note 5)

5

Notes for Table 3

1. Reset clears the page memory, sets page number to 100 and time code to 00.00 and resets timed page and display cancel modes.

2. Three number commands in sequence request a new page, and four number commands select a new time code in timed page mode. When a new page has been requested the page header turns green and the page numbers roll until the new page is captured.

3. When hold mode is selected 'STOP' is displayed in green at the top right of the screen.

4. Display cancel/recall removes the text and restores the television picture. The SAA5042 then reacts to any update indicator on the selected page. An updated newsflash or subtitle is displayed immediately. When an updated normal page arrives the page number only is displayed in a box at the top left of the screen. The same command will then cause a normal page to be displayed, but will cancel a newsflash or subtitle page. Alternatively, text can be recalled by using the teletext/on command.

5. The teletext/on command resets display cancel, hold and superimpose modes.

6. Status, timed page, numbers, superimpose and teletext/on commands all reset to top half page and produce a box round the header for five seconds. This allows the header to be seen even if the television picture is on (e.g. newsflash or display cancel modes).

7. A 'P' is displayed before the page number at the top left of the screen (e.g. P123).

8. In viewdata mode ($b_7 = b_6 = 1$) the SAA5042 is disabled and teletext cannot be received. All 3-state outputs are high impedance.

9. Table 3 shows code required for functions specified. The SAA5042 requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$, $\overline{b_1}$, $\overline{b_2}$, $\overline{b_3}$, $\overline{b_4}$, $\overline{b_5}$, $\overline{b_6}$.

10. Clear Memory occurs except in Timed Page Mode.

Gearing and Address Logic Array for USA Teletext (GALA)

SAA5045

GENERAL DESCRIPTION

The SAA5045 is a PCF0700 CMOS process gate array designed to interface the SAA5040B Teletext Acquisition Control (TAC) IC to the SAA5030 Video Processor (VIP) data output for modified U.K. standard 525-line Teletext. It also provides an address interface between SAA5040B, SAA5025D Teletext Timing Chain for USA 525 line system (USTIC) and the page memory RAM. The memory interface includes read/write control compatible with the geared 32 + 8 transmission system at 5,727272 MHz data rate employed in the modified U.K. system.

For RATINGS and CHARACTERISTICS see data sheet: CMOS GATE ARRAYS (PCF0700).

SYSTEM CONTENT

Functionally the chip contains two main sections which operate during the acquisition and display periods.

5

Gearing control section

The data from the SAA5030 (VIP) and data clock, are processed to detect the presence of the gearing bit and convert the data for correct operation of the SAA5040B (TAC). Data and clock outputs to the TAC are internally compensated for processing delays, so that correct clocking-in of data is ensured.

Addressing section

Column counters are included, which operate from the WACK (TAC) and RACK (USTIC) column clock signals during acquisition and display respectively.

Five row-address input circuits (pins A0 to A4) are provided for (TAC) and (USTIC) address outputs. These are multiplexed with the column address from the internal counters for correct mapping of the RAM via ten output address pins (AA0 to AA9). During acquisition, the multiplexer is controlled by the gearing bit detection to give correct assembly of the 40 character per row page structure.

The address output buffers are 3-state devices controlled by the line reset signal (pin 8; $\overline{\text{GLRS}}$). During the horizontal flyback period the address pins are 3-state to allow alternative addressing for customized applications.

Read/write control to RAM

An internal counter prevents overwriting if more than 32 character WOK pulses are received from TAC due to poor transmission conditions. Two control outputs, one for read/write ($\overline{\text{WE}}$) and the other for chip select ($\overline{\text{CS}}$), are provided to eliminate conflicts on the input/output RAM bus.

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117D).

SYSTEM CURRENT (continued)

Framing code detection

When a valid data line is received and the framing code is detected in the gearing section, then flag pulses (pair of pulses) are available at output $\overline{WE}$, before the $\overline{CS}$ output is driven LOW for normal writting into the RAM. If a framing-code-present signal is required, it can be obtained by gating $\overline{WE}$ and $\overline{CS}$ outputs such, that an output from the $\overline{WE}$, when output $\overline{CS}$ is HIGH, indicates the detection of a framing code; N.B., each framing code produces a pair of pulses.

RAM ADDRESS CONTROL

Figure 2 shows that the ten RAM address outputs are controlled by a multiplexer (MUX3), which interchanges the two groups of five address lines, when a gearing bit equal to logic "1" is received during data input. During display, MUX3 is switched by bit number 6 of the column counter. MUX1, which is switched by the gearing bit, controls stepping of the row address when fill-in rows are received. MUX2 is switched by either the gearing bit or bit 6 of the column counter to access the part of RAM storing the last eight bytes of each row of data.

The mapping of the 1024-byte RAM is shown in Fig. 1. Area "A" stores data corresponding to the left-hand side (32 bytes wide) of the display whilst area "B" stores the remainder for the right-hand side.

Access to the RAM for custom operations can be made during the time that $\overline{GLRS}$ (pin 8) is LOW, which causes all ten address buffers to be in the open state. It should be noted that $\overline{GLRS}$ LOW also resets the column counters and the gearing-bit detection system to logic "0". This normally occurs during the horizontal interval (between 5 and 8 μs) after the horizontal sync pulse falling edge.

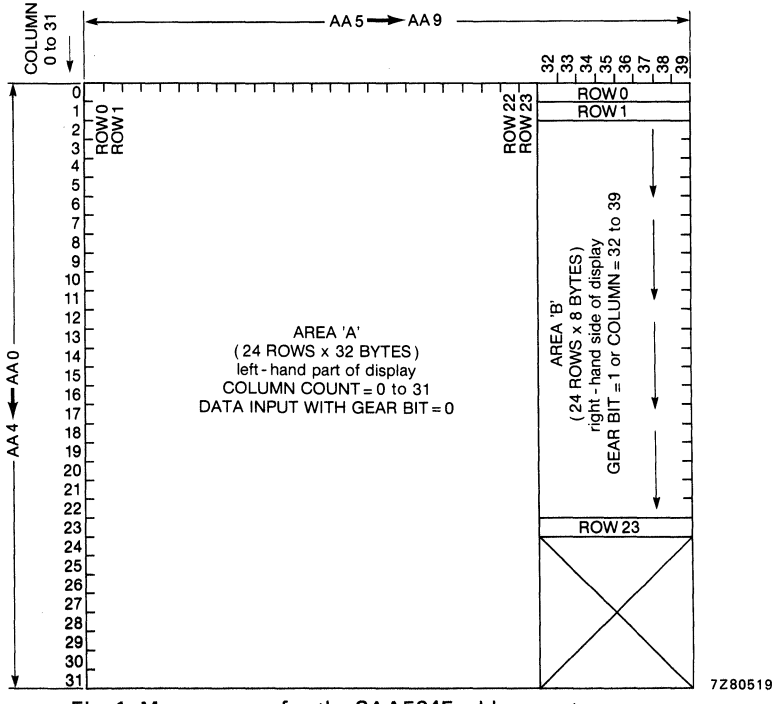


Fig. 1 Memory map for the SAA5045 address system.

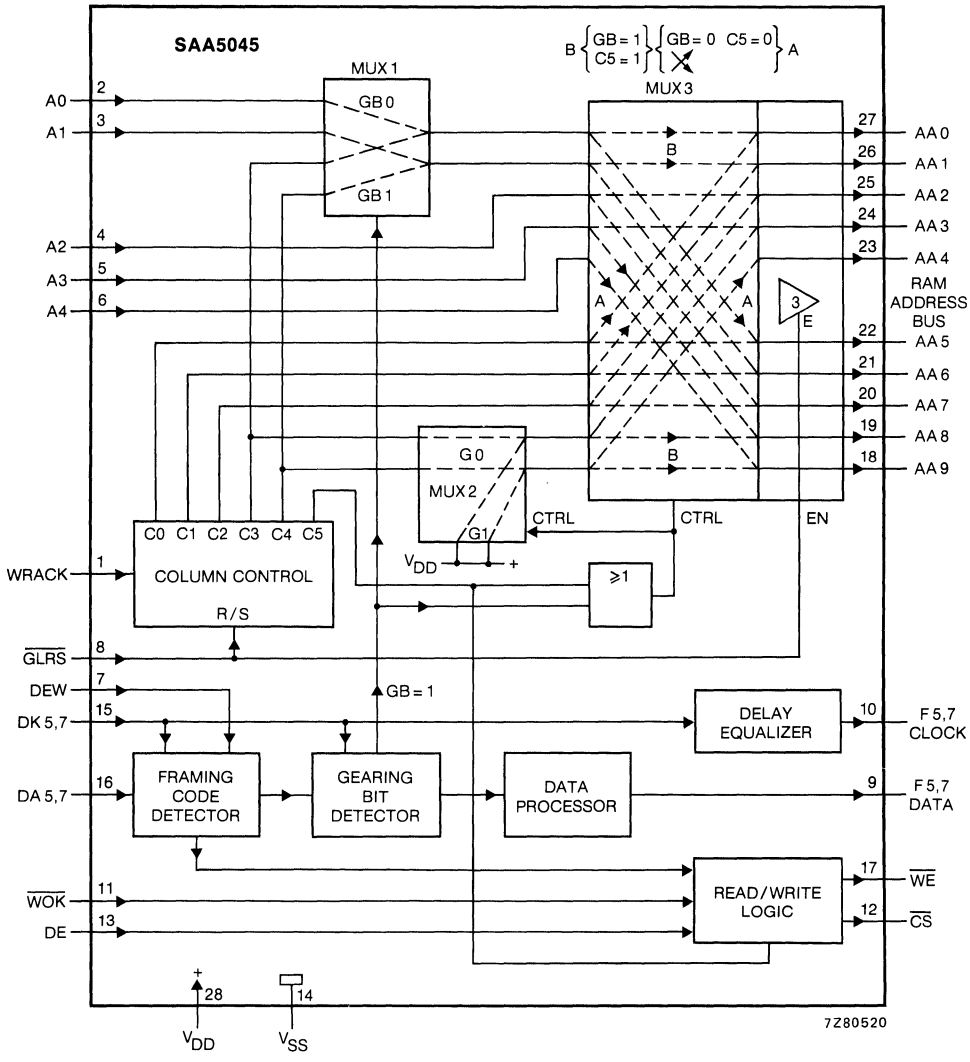


Fig. 2 Block diagram.

PIN DESCRIPTION

pin no.	symbol	name and function
1	WRACK	input clock to column counter
2	A0	row address system inputs
3	A1	
4	A2	
5	A3	
6	A4	
7	DEW	data entry window input
8	$\overline{\text{GLRS}}$	general line reset starting output
9	F5,7 DATA	5,7 MHz data output
10	F5,7 CLOCK	5,7 MHz clock output
11	$\overline{\text{WOK}}$	write enable input
12	$\overline{\text{CS}}$	chip select output
13	DE	display enable input
14	V_{SS}	ground
15	DK5,7	5,7 MHz data clock input
16	DA5,7	5,7 MHz data input
17	$\overline{\text{WE}}$	write enable output
18	AA9	memory address outputs
19	AA8	
20	AA7	
21	AA6	
22	AA5	
23	AA4	
24	AA3	
25	AA2	
26	AA1	
27	AA0	
28	V_{DD}	positive supply (+ 4,5 V to + 5,5 V)

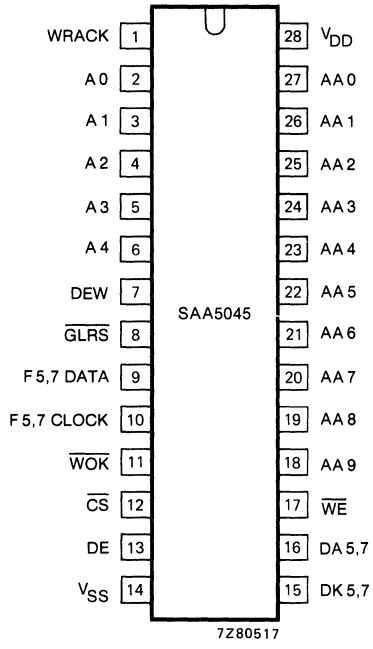


Fig. 3 Pin configuration.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. WRACK – input clock to column counter

Input clock to column counter during data input or display; WACK from SAA5040B (TAC) or RACK from SAA5025D (USTIC).

2 to 6. A0 to A4 – row address system inputs

Inputs to row address system during data input or display. Row address numbers greater than 0 to 23 disable writing to the RAM during input.

7. DEW – data entry window input

Data entry window input enables gearing bit detection and data processing part of system.

8. $\overline{\text{GLRS}}$ – general line reset starting output

Input from the SAA5025D is a negative reset pulse at line rate for column counters and gearing system. When this input is LOW, it opens 3-state address buffers.

9. F5,7 DATA – 5,7 MHz data output

Data output at 5,7 MHz rate to SAA5040B (TAC) during the data acquisition period when DEW is HIGH.

10. F5,7 CLOCK – 5,7 MHz clock output

Data clock output at 5,7 MHz rate to SAA5040B (TAC), synchronized to data at pin 9 (F5,7 DATA).

11. $\overline{\text{WOK}}$ – write enable input

Write enable input from SAA5040B (TAC) during data acquisition, when correct data is received, for RAM write/read control (via output $\overline{\text{WE}}$; pin 17).

12. $\overline{\text{CS}}$ – chip select output

Output to drive the RAM chip enable during data input and display periods controlled by the display enable output (DE) and write O.K. ($\overline{\text{WOK}}$) output of the SAA5040B (TAC), avoiding input/output bus conflict.

13. DE – display enable input

Display enable input from SAA5040B (TAC) to control $\overline{\text{CS}}$.

14. V_{SS} – ground

15. DK5,7 – 5,7 MHz data clock input

Data clock input at 5,7 MHz rate from the SAA5030 (VIP); this pin is capacitively coupled with a d.c. restoring diode and is externally connected to V_{SS}.

16. DA5,7 – 5,7 MHz data input

Data input at 5,7 MHz rate from SAA5030 (VIP); this pin is capacitively coupled with a d.c. restoring diode and is externally connected to V_{SS}.

APPLICATION INFORMATION (continued)

17. $\overline{WE}$ – write enable output

$\overline{Write}$ enable output to control RAM write/read. This output is the gated and delay version of the $\overline{WOK}$ from the SAA5040B, but limited to 32 pulses which are possible before the WACK count is equal to 32.

A pair of pulses on this output precedes the $\overline{WOK}$ pulses, whilst $\overline{CS}$ is HIGH whenever a framing code is detected.

18 to 27. AA9 to AA0 – memory address outputs

Memory address outputs; 3-state buffered outputs, open when $\overline{GLRS}$ is LOW for auxiliary access to the RAM address bus if required.

N.B.: AA9 and AA8 are simultaneously HIGH whenever a gear bit with logic "1" is received during DEW is HIGH. This enables detection of gearing bit reception, following $\overline{GLRS}$ reset on each line, which always resets AA0 to AA9 to logic "0".

28. V_{DD} – positive supply (4,5 V to 5,5 V)

Note

Input pins other than 15 and 16 have internal 15 kΩ pull-up resistors for compatibility with SAA5025D and SAA5040B output signal ranges. Pins 15 and 16 are CMOS inputs for d.c. restored drive from the SAA5030 (VIP) clock and data output signals.

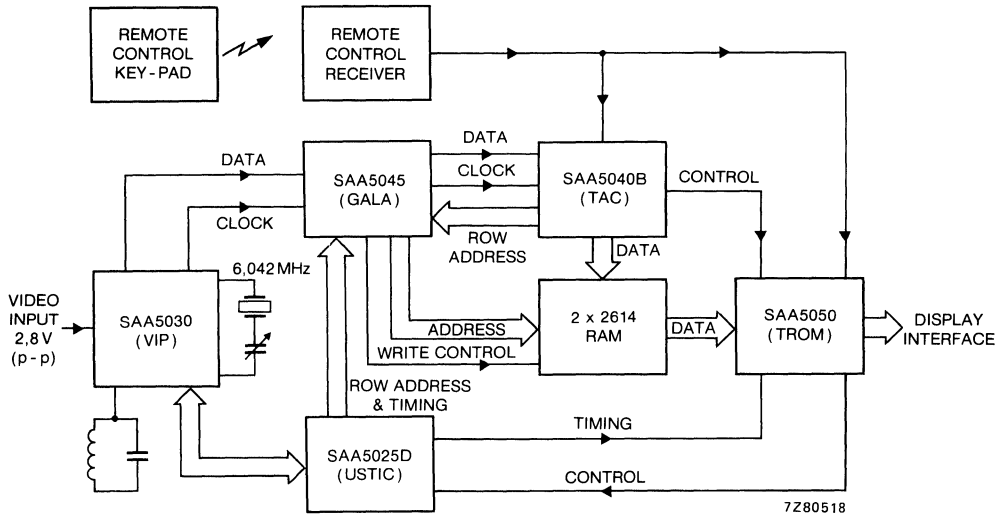


Fig. 4 Schematic diagram of the 5-chip decoder.

5

For additional information
consult the Applications Section.

Teletext Character Generator | SAA5050/55

The SAA5050 series of MOS N-channel integrated circuits provides the video drive signals to the television receiver necessary to produce the teletext/viewdata display. The variants are described in the Quick Reference Data and full details of the characters sets are given in Figs. 11 to 18.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	85	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

Variant	Character set	Variant	Character set
5050	English	5054	Belgian
5051	German	5055	US ASCII
5052	Swedish	5056	Hebrew
5053	Italian	5057	Cyrillic

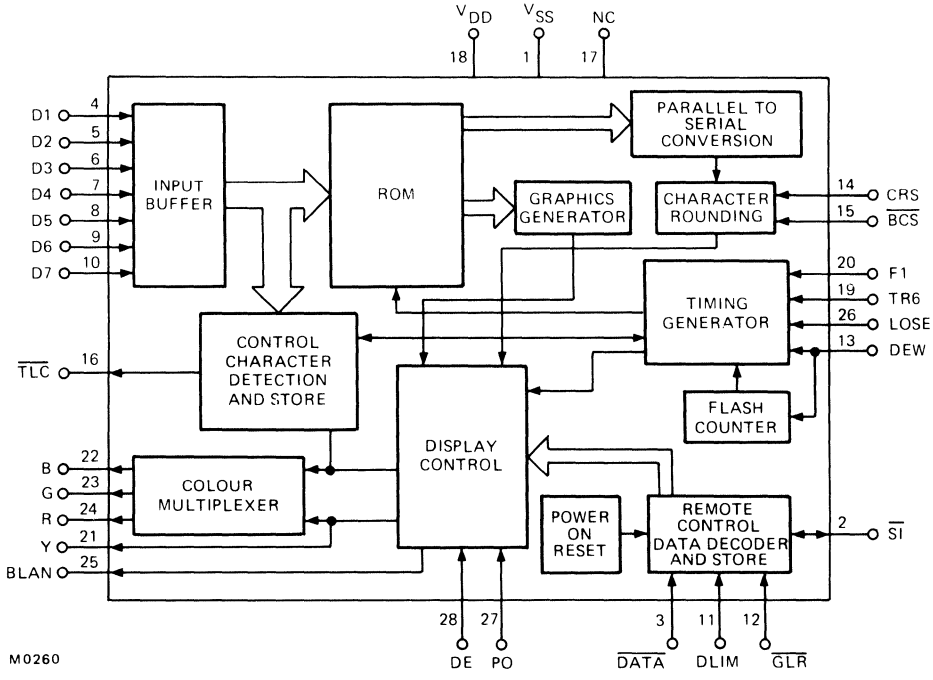


Fig.1 Block diagram

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

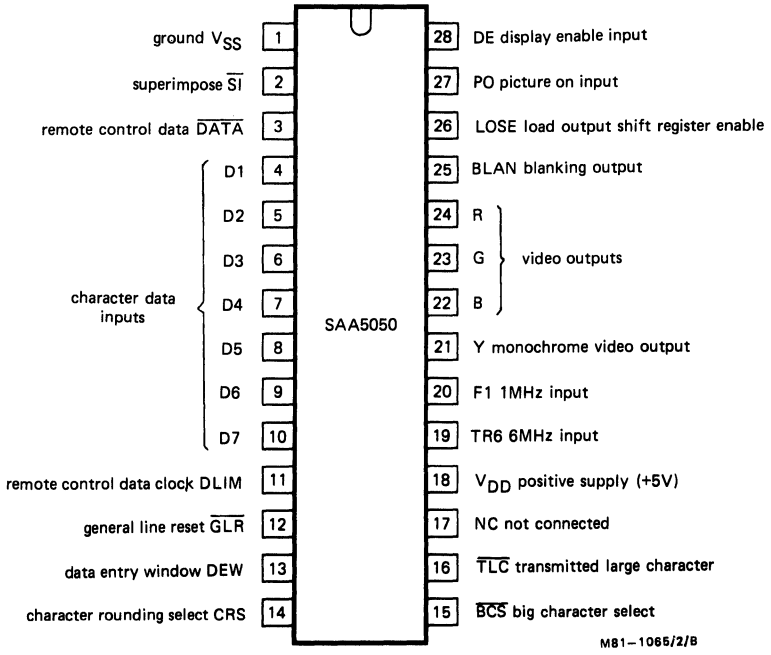


Fig.2 Pinning diagram

DESCRIPTION

The SAA5050 is a 28 pin device which incorporates a fast access character generator ROM (4.3 k bits), the logic decoding for all the teletext control characters and decoding for some of the remote control functions. The circuit generates 96 alphanumeric and 64 graphic characters. In addition there are 32 control characters which determine the nature of the display.

The SAA5050 is suitable for direct connection to the SAA5010, SAA5012, SAA5020 and SAA5040 Series integrated circuits.

The basic input to the SAA5050 is the character data from the teletext page memory. This is a 7 bit code. Each character code defines a dot matrix pattern. The character period is 1 μs and the character dot rate is 6 MHz. The timings are derived from the two external input clocks F1 (1 MHz) and TR6 (6 MHz) which are amplified and re-synchronised internally. Each character rectangle is 6 dots wide by 10 TV lines high. One dot space is left between adjacent characters, and there is one line space left between rows. Alphanumeric characters are generated on a 5 x 9 matrix, allowing space for descending characters. Each of the 64 graphic characters is decoded to form a 2 x 3 block arrangement which occupies the complete 6 x 10 dot matrix (Fig.9). Graphics characters may be either contiguous or separated (Fig.10). The alphanumeric characters are character rounded, i.e. a half dot is inserted before or after a whole dot in the presence of a diagonal in a character matrix.

The character video output signals comprise a monochrome signal and RGB signals for a colour receiver. A blanking output signal is provided to blank out the television video signal under the control of the PO and DE inputs and the box control characters (see Table 3).

The monochrome data signal can be used to inlay characters into the television video. The use of the 32 control characters provides information on the nature of the display, e.g. colour. These are also used to provide other facilities such as 'concealed display' and flashing words etc. The full character set is given in Table 1.

5

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (See 'Handling MOS Devices').

RATINGS Limiting values in accordance with the Absolute Maximum System, (IEC134)

		min.	typ.	max.	
Voltages (with respect to pin 1)					
Supply voltage (pin 18)	V_{DD}	−0.3	–	7.5	V
Input voltages (all inputs + input/output)	V_I	−0.3	–	7.5	V
Output voltage (pin 16)	V_{O16}	−0.3	–	7.5	V
(all other outputs)	V_O	−0.3	–	14.0	V
Temperature					
Storage temperature range	T_{stg}		−20 to +125		°C
Operating ambient temperature range	T_{amb}		−20 to +70		°C

CHARACTERISTICS

		min.	typ.	max.	
Supply voltage (pin 18)	V_{DD}	4.5	–	5.5	V
The following parameters apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.					
Supply current	I_{DD}	–	85	160	mA
Inputs					
Character data D1 to D7 (pins 4 to 10)					
Input voltage; HIGH	V_{IH}	2.65	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Clock inputs F1 (pin 20) **TR6** (pin 19)					
Input voltage; HIGH	V_{IH}	2.65	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.6	V
Logic inputs					
$\overline{\text{DATA}}$ (pin 3) DEW (pin 13) LOSE (pin 26) DLIM (pin 11) $\overline{\text{CRS}}$ (pin 14) PO (pin 27) $\overline{\text{GLR}}$ (pin 12) $\overline{\text{BCS}}$ (pin 15) DE (pin 28)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
All inputs					
Input leakage current (V_I = 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

			min.	typ.	max.	
Outputs						
Character video outputs + Blanking output (open drain) (note 3)						
B – (pin 22), G – (pin 23), R – (pin 24), Y – (pin 21), Blanking (pin 25)						
Output voltage; LOW (I_{OL} = 2 mA)		V_{OL}	–	–	0.5	V
Output voltage; LOW (I_{OL} = 4 mA)		V_{OL}	–	–	1.0	V
Output voltage; LOW (I_{OL} = 6 mA)		V_{OL}	–	–	2.0	V
Output voltage; HIGH (note 5)		V_{OH}	V_{DD}	–	13.2	V
Output load capacitance		C_L	–	–	15	pF
Output fall time	note 1	t_f	–	–	30	ns
Variation of fall time between any outputs	note 1	Δt_f	0	–	20	ns
$\overline{\text{TLC}}$ (pin 16)						
Output voltage; LOW (I_{OL} = 100 μA)		V_{OL}	0	–	0.5	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)		V_{OH}	2.4	–	V_{DD}	V
Output load capacitance		C_L	–	–	30	pF
Output rise time	Measured between 0.8 V and 2.0 V levels	t_r	–	–	1.0	μs
Output fall time	Measured between 0.8 V and 2.0 V levels	t_f	–	–	1.0	μs
Input/output						
$\overline{\text{SI}}$ (pin 2) (open drain)						
Input voltage; HIGH		V_{IH}	2.0	–	6.5	V
Input voltage; LOW		V_{IL}	0	–	0.8	V
Input leakage current (V_I = 5.5 V)		I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 0.4 mA)		V_{OL}	0	–	0.5	V
Output voltage; LOW (I_{OL} = 1.3 mA)		V_{OL}	0	–	1.0	V
Output load capacitance		C_L	–	–	45	pF
Output voltage; HIGH state (note 2)		V_{OH}	–	–	6.5	V

5

Timing characteristics

For typical display of 40 characters per line. Line rate = 64 μs. Field rate = 20 ms.

Character data timing (Fig.4)

			min.	typ.	max.	
TR6 rising edge to F1 falling edge		t_D	6	–	60	ns
TR6 frequency		f_{TR6}	–	6	–	MHz
TR6 mark/space ratio			40:60	–	60:40	
F1 frequency		f_{F1}	–	1	–	MHz
F1 mark/space ratio			40:60	–	60:40	
Data set-up time		t_{CDS}	80	–	–	ns
Data hold time		t_{CDH}	100	–	–	ns
Delay time – character in/ character data at outputs	Graphics	t_{CDG}	–	2.6	–	μs
	Alphanumerics	t_{CDA}	–	2.767	–	μs

Display period timing (Fig.5)

F1 falling edge to LOSE rising edge	t_{LDH}	0	–	250	ns
F1 falling edge to LOSE falling edge	t_{LDL}	0	–	250	ns
LOSE rising edge to 'Display on'	t_{DON}	–	2.6	–	μs
LOSE falling edge to 'Display off'	t_{DOFF}	–	2.6	–	μs
'Display period'	t_{DP}	–	40	–	μs

Line rate timing (Fig.6)

F1 rising edge to GLR falling edge	t_{DGL}	0	–	200	ns
F1 rising edge to GLR rising edge	t_{DGH}	0	–	200	ns
GLR LOW time	t_{GLP}	–	1	–	μs
Line start* to GLR falling edge	t_{GLR}	–	5	–	μs
Line start* to LOSE rising edge	t_{LSL}	–	14.5	–	μs
LOSE falling edge to Line start*	t_{LLS}	–	9.5	–	μs
Line period	t_{LNP}	–	64	–	μs
LOSE HIGH time	t_{LHP}	–	40	–	μs

Remote data input timing (Fig.8)

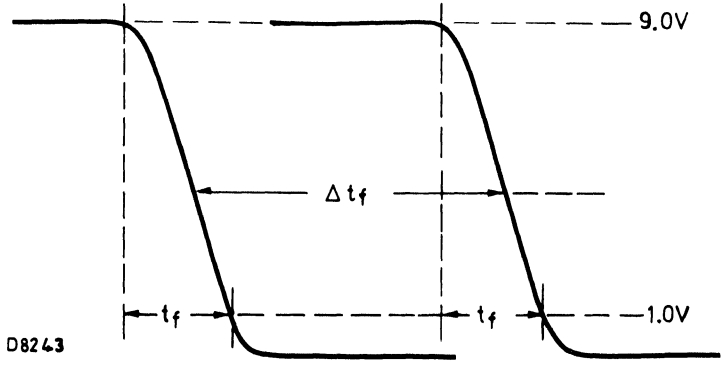
Assuming F1 period = 1 μs and GLR period = 64 μs

DLIM clock HIGH time	t_{CH}	6.5	8	(note 4)	μs
DLIM clock LOW time	t_{CL}	3.5	8	60	μs
DATA to DLIM set-up time	t_{DS}	0	14	–	μs
DLIM to DATA hold time	t_{DH}	8	14	–	μs

*Taken as falling edge of 'line sync' pulse.

Notes to characteristics

1. Fall time, t_f and Δt_f, are defined as shown and are measured using the circuit shown below:
   t_f is measured between the 9 V and 1 V levels.
   Δt_f is the maximum time difference between outputs.



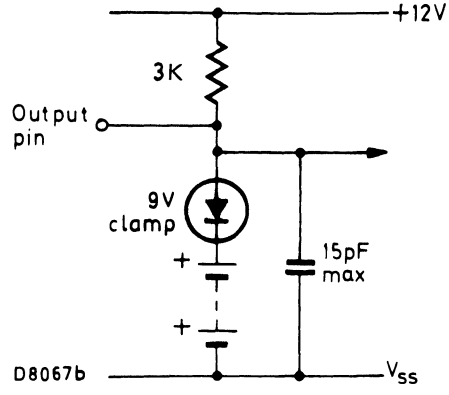


Fig.3

2. Recommended pull-up resistor for $\overline{SI}$ is 18 kΩ.
3. The R, G, B, Y and blanking outputs are protected against short circuit to supply rails.
4. There is no maximum DLIM cycle time, provided the DLIM duty cycle is such that the $t_{CL\ max}$ requirement is not exceeded.
5. With maximum pull-up voltage applied to R, G, B and BLAN outputs the leakage current will not exceed 20 μA with the outputs in the OFF state.

SPECIAL FEATURES

Flash oscillator

The circuit generates a 0.75 Hz signal with a 3:1 ON/OFF ratio to provide the flashing character facility.

Power-on-reset

When the supply voltage is switched on, the character generator will reset to tv, conceal, and not superimpose modes.

Character rounding

The character rounding function is different for the small and double height characters. In both cases the ROM is accessed twice during the character period of 1 μs. The dot information of two rows is then compared to detect the presence of any diagonal in the character matrix and to determine the positioning of the character rounding half dots.
For small characters rounding is always referenced in the same direction (i.e. row before in even fields and row after in odd fields as determined by the CRS signal).
For double height characters rounding is always referenced alternately up and down changing every line using an internally generated signal. (The CRS signal is '0' for the odd field and '1' for the even field of an interlaced tv picture).

Graphics decoder

The 64 graphics characters are decoded directly from the character data inputs and they appear on a 2 x 3 matrix. Figure 9 gives details of the graphics decoding.

APPLICATION DATA

The function is quoted against the corresponding pin numbers

Pin No.

1. **V_{SS} Ground** - 0 V

2. **$\overline{SI}$ Superimpose**

   This is a dual purpose input/output pin. The output is an open drain transistor (capable of sinking current to V_{SS}), which is in the conducting state when superimpose mode is selected. This allows contrast reduction of the tv picture in superimpose mode if required. If the pin is held LOW, the internal 'tv mode' flip-flop is held in the 'text' state. This is for VDU applications when the remote control is not used.

3. **$\overline{DATA}$ Remote control data**

   This input accepts a 7-bit serial data stream from the remote control decoder. This data contains the teletext and viewdata remote control functions. The nominal data rate is 32 μs/bit. The command codes used in the SAA5050 are shown in Table 2.

4,5,6 7,8,9, 10 **D1 to D7 Character data**

These inputs accept a 7-bit parallel data code from the page memory. This data selects the alphanumeric characters, the graphics characters and the control characters. The alphanumeric addresses are ROM column addresses, the graphics and control data are decoded internally.

11. **DLIM**

    This input receives a clock signal from the remote control decoder and this signal is used to clock remote control data into the SAA5050. The positive-going edge of every second clock pulse is nominally in the centre of each remote control data bit (Fig.8).

12 **GLR General line reset**

This input signal from the SAA5020 Timing Chain is required for internal synchronisation of remote control data signals.

13. **DEW Data entry window**

    This input signal from the SAA5020 Timing Chain is required to reset the internal ROM row address counter prior to the display period. It is also used internally to derive the 'flash' period.

APPLICATION DATA (continued)

14. **CRS Character rounding select**

This input signal from the SAA5020 Timing Chain is required for correct character rounding of displayed characters. (Normal height characters only).

15. **$\overline{BCS}$ Big character select**

This input from the SAA5040 Teletext Acquisition and Control device allows selection of large characters by remote control.

16. **$\overline{TLC}$ Transmitted large characters**

This output to the SAA5020 Timing Chain enables double height characters to be displayed as a result of control characters stored in the page memory.

18. **V_{DD} + 5 V supply**

This is the power supply input to the circuit.

19. **TR6**

This input is a 6 MHz signal from the SAA5020 Timing Chain used as a character dot rate clock.

20. **F1**

This input is a 1 MHz equal mark/space ratio signal from the SAA5020 Timing Chain. It is used to latch the 7-bit parallel character data into the input latches. It is also used to synchronise an internal divide-by 6 counter. The F1 signal is internally synchronised with TR6.

21. **Y Output**

This is a video output signal which is active in the HIGH state containing character dot information for tv display.
The output is an open drain transistor capable of sinking current to V_{SS}

22,23, 24. **B,G,R outputs**

These are the Blue, Green and Red Character video outputs to the tv display circuits. They are active HIGH and contain both character and background colour information.
The outputs are open drain transistors capable of sinking current to V_{SS}.

25. **BLAN Blanking**

This active HIGH output signal provides tv picture video blanking. It is active for the duration of a box when Picture On and Display Enable are HIGH. It is also activated permanently for normal teletext display when no tv picture is required (PO LOW). The output is an open drain transistor capable of sinking current to V_{SS}. Full details given in Table 3.

26. **LOSE Load output shift register enable**

This input signal from the SAA5020 Timing Chain resets the internal control character flip-flops prior to the start of each display line.
This signal also defines the character display period.

27. **PO Picture On**

This input signal from the SAA5040 Teletext Acquisition and Control device is used to control the character video and blanking outputs. When PO is HIGH, only text in boxes is displayed unless in superimpose mode. The input is HIGH for tv picture video on, LOW for picture off. See Table 3.

28. **DE Display enable**

This input signal from the SAA5040 Teletext Acquisition and Control device is used to enable the teletext display. The input is HIGH for teletext display enabled. LOW for display cancelled. See Table 3.

5

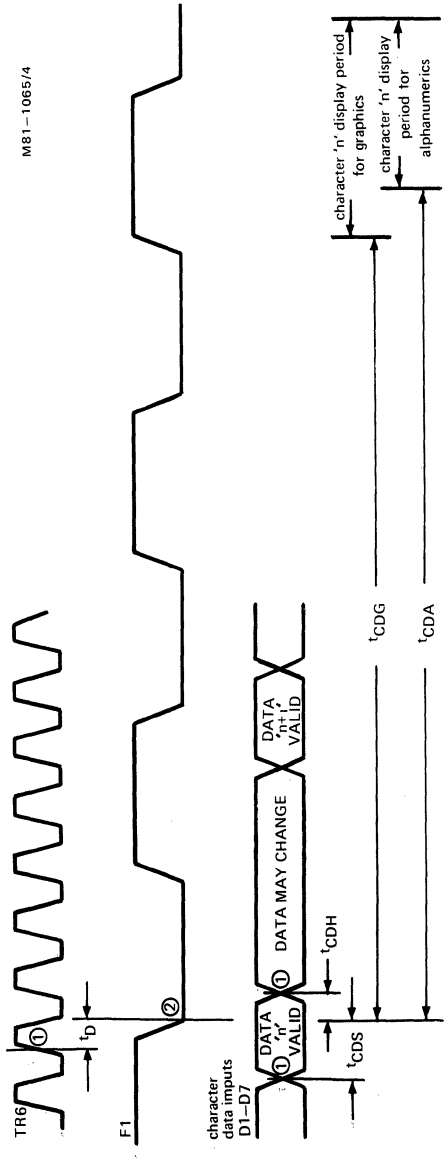


Fig.4 Character data timing (for typical 40 character display)

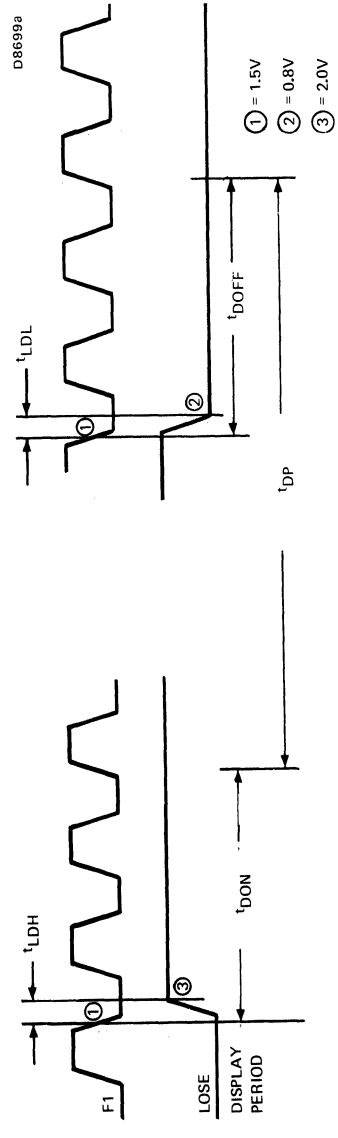


Fig.5 Display period timing (for typical 40 character display)

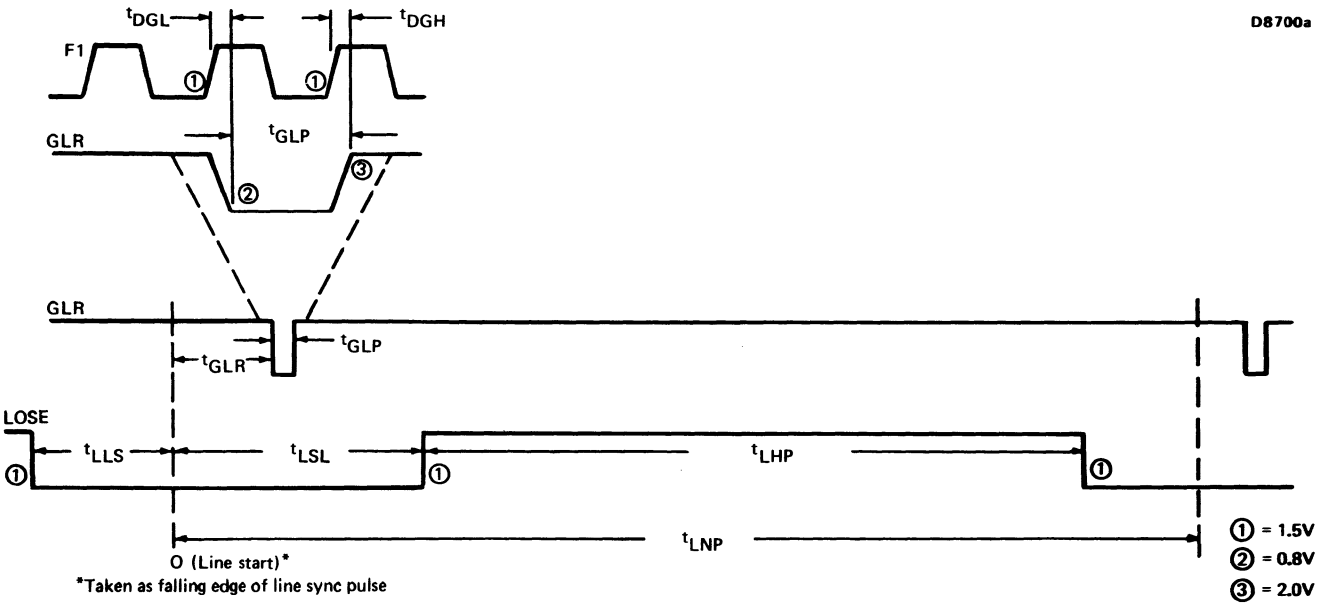


Fig.6 Line rate clocks (for line period of 64 μs)

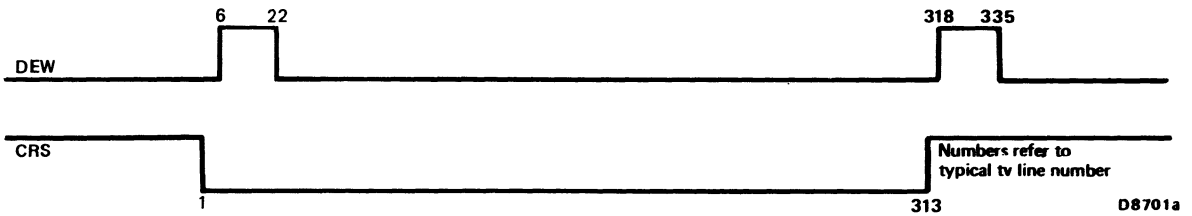


Fig.7 Field rate clocks (for field period of 20 ms, 312½ lines per field)

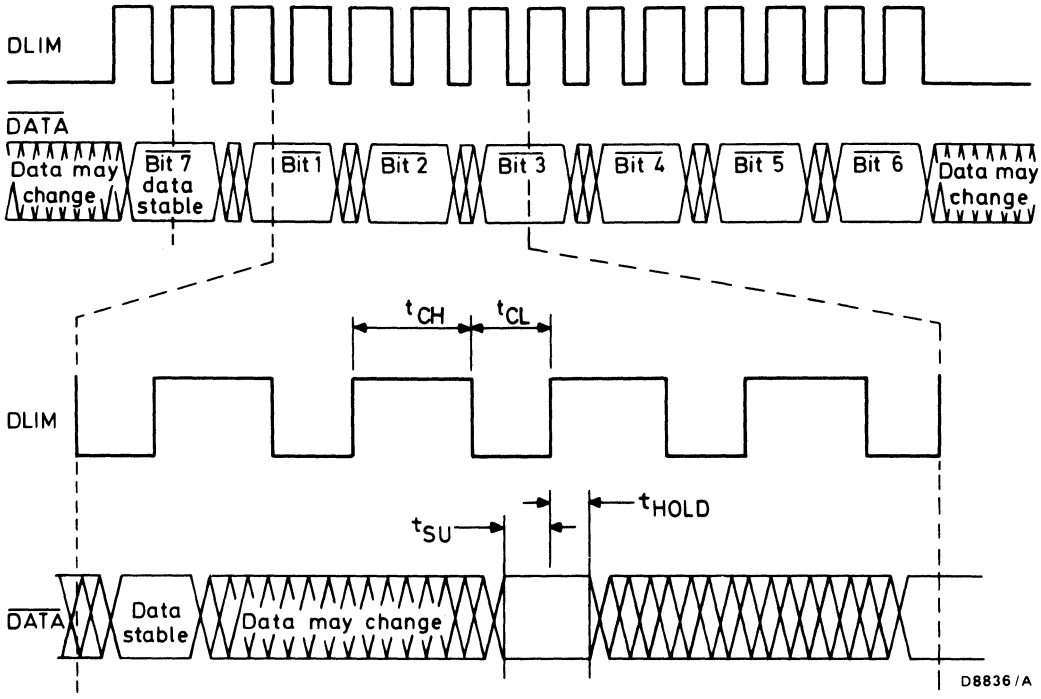
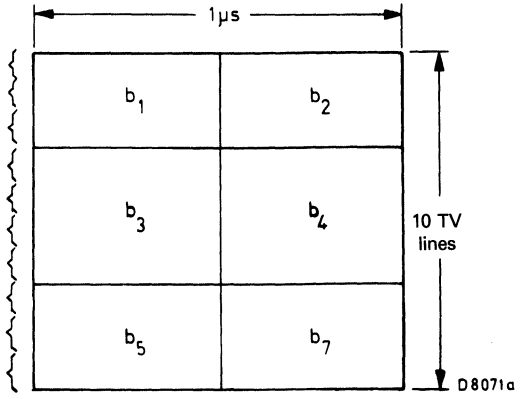


Fig.8 Remote control input timing



Each cell is illuminated if particular 'bit' (b_1, b_2, b_3, b_4, b_5, or b_7) is a '1'.
For graphics characters b_6 is always a '1' – See Table 1.

Fig.9 Graphics Character

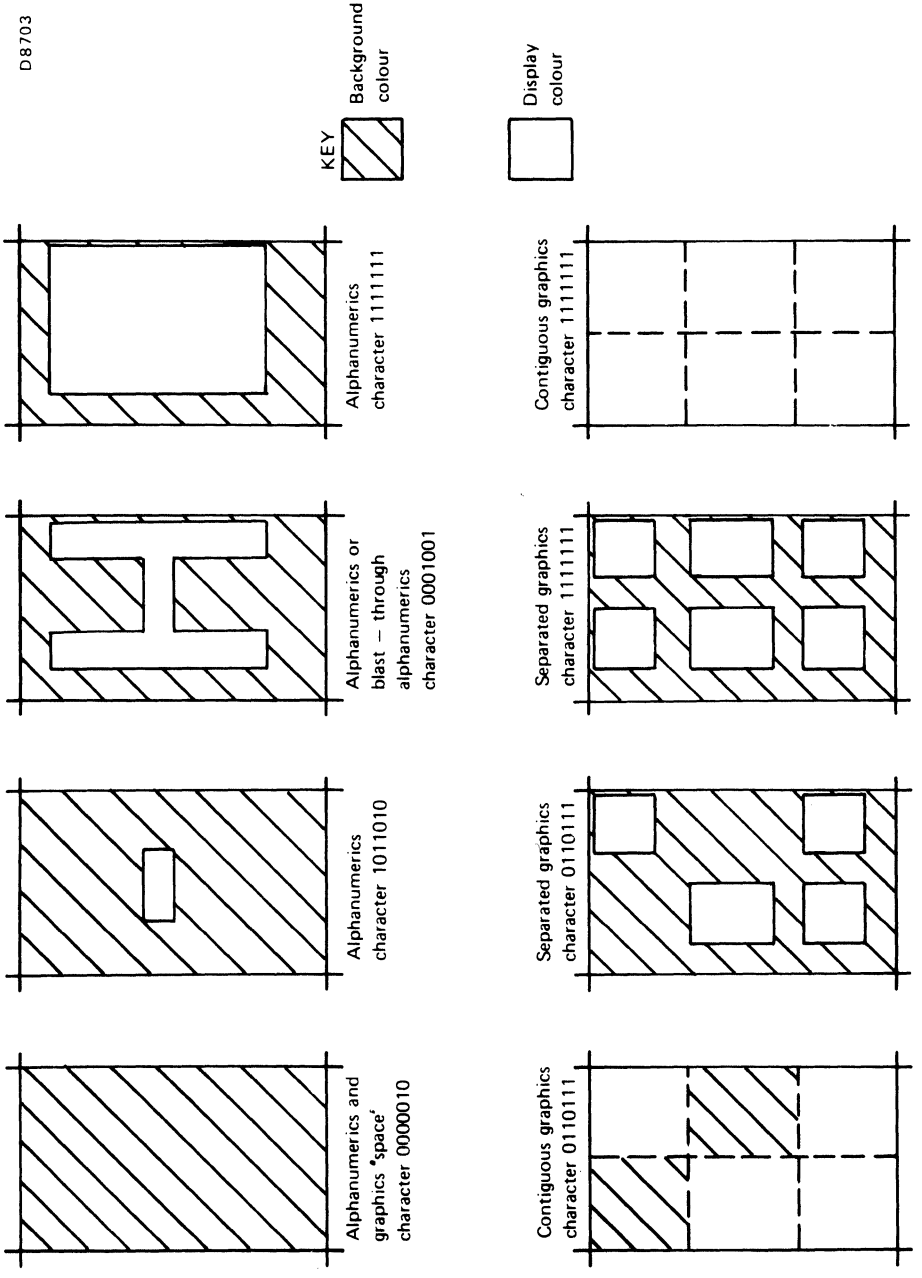


Fig.10 Character format

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TABLE 1

Character data input decoding

D8068a

Bits b_4 b_3 b_2 b_1	Row	b_7 b_6 b_5 = 0 0 0 Col 0	0 0 1 Col 1	0 1 0 Col 2	2a	0 1 1 Col 3	3a	1 0 0 Col 4	1 0 1 Col 5	1 1 0 Col 6	6a	1 1 1 Col 7	7a
0 0 0 0	0	NUL*	DLE*			0		@	P	–		p	
0 0 0 1	1	Alpha Red	Graphics Red	!		1		A	Q	a		q	
0 0 1 0	2	Alpha Green	Graphics Green	"		2		B	R	b		r	
0 0 1 1	3	Alpha Yellow	Graphics Yellow	£		3		C	S	c		s	
0 1 0 0	4	Alpha Blue	Graphics Blue	$		4		D	T	d		t	
0 1 0 1	5	Alpha Magenta	Graphics Magenta	%		5		E	U	e		u	
0 1 1 0	6	Alpha Cyan	Graphics Cyan	&		6		F	V	f		v	
0 1 1 1	7	Alpha White**	Graphics White	'		7		G	W	g		w	
1 0 0 0	8	Flash	Conceal Display	(		8		H	X	h		x	
1 0 0 1	9	Steady**	Contiguous Graphics**	)		9		I	Y	i		y	
1 0 1 0	10	End Box**	Separated Graphics	*		:		J	Z	j		z	
1 0 1 1	11	Start Box	ESC*	+		;		K	←	k		¼	
1 1 0 0	12	Normal Height**	Black Background**	,		<		L	½	l		‖	
1 1 0 1	13	Double Height	New Background	–		=		M	→	m		¾	
1 1 1 0	14	SO*	Hold Graphics	.		>		N	↑	n		÷	
1 1 1 1	15	SI*	Release Graphics**	/		?		O	#	o		■	

Control characters shown in columns 0 and 1 are normally displayed as spaces.
The SAA5050 character set is shown as example. Details of character sets are given in Figs. 11 and 12.

* These control characters are reserved for compatability with other data codes.

** These control characters are presumed before each row begins.

Codes may be refered to by their column and row e.g. 2/5 refers to %

Character rectangle

Black represents display colour.

White represents background.

TABLE 2

Remote control command codes used in the SAA5050

CODE b_7	b_6	b_5	b_4	b_3	b_2	b_1	COMMAND	FUNCTION
0	X	X	X	X	X	X	'tv' mode	Allows text on top row of display only.
1	X	X	X	X	X	X	'Text' mode	Allows text throughout display period.
1	0	1	1	1	1	0	Superimpose	Sets Superimpose mode.
1	0	1	1	1	1	1	teletext	Resets Superimpose mode.
0	X	X	X	X	X	X	'tv' mode	Resets Superimpose mode.
1	1	X	X	X	X	X	viewdata mode	Resets Superimpose mode;
1	X	0	0	1	1	0	Reveal	Reveals for time-out (notes 3, 4).
1	X	0	1	0	1	1	Reveal set	Sets Reveal mode (note 3).
Any command apart from reveal set.								Resets Reveal mode (note 3)

X = Don't care.

Notes

1. When the power is applied the SAA5050 is set into the 'tv' mode and reset out of Superimpose and Reveal modes.
2. 'Text' mode is selected when $\overline{SI}$ (pin 2) is held LOW
3. Reveal mode allows display of text previously concealed by 'conceal display' control characters.
4. This code is sent from the SAA5010 or the SAA5012 Series as a repeated command. Thus Reveal mode is set for as long as the Reveal key is depressed. The SAA5050 reverts to normal 'not Reveal' mode 160 ms after the last Reveal command.
5. The Superimpose output is LOW only if Superimpose mode is set and the DE (display enable) input is HIGH.
6. The above table shows code required for functions specified.
   The SAA5010 or the SAA5012 Series transmits and the SAA5050 requires the inverse of these codes i.e. $\overline{b_7}$ to $\overline{b_1}$. The code is transmitted serially in the following order: $\overline{b_7}$ $\overline{b_1}$ $\overline{b_2}$ $\overline{b_3}$ $\overline{b_4}$ $\overline{b_5}$ $\overline{b_6}$.
   For full details of remote control data coding see the SAA5010 or the SAA5012 data sheets.

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TABLE 3

Conditions affecting display (see note 3)

	Inputs		Control data		Outputs	
	Picture On (PO)	Display Enable (DE)	Superimpose Mode	Box	Text Display Enabled (i.e. R,G,B,Y outputs)	Blanking
(a)	1	0	1 or 0	1 or 0	0	0
(b)	0	1	1 or 0	1 or 0	1	1
(c)	0	0	1 or 0	1 or 0	0 (note 2)	1
(d)	1	1	0	0	0	0
(e)	1	1	1	0	1	0
(f)	1	1	1	1	1	1
(g)	1	1	0	1	1	1

Notes

1. For tv mode (Picture On = '1', Superimpose mode not allowed) rows (a), (d) and (g) of Table 3 refer to display row 0 only. For all other rows text display is disabled and Blanking = '0'.
2. The R, G, B outputs may contain character and background colour information. The only exception is that background colours are inhibited when Blanking = '0'.
3. Valid during display period only (see Fig.5) otherwise no character or background information is displayed as blanking is determined by the Picture On. (No blanking if PO = '1').

Fig. 11 SAA5050 character set (English).

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Fig. 12 SAA5055 character set (US ASCII).

Microcomputer/Microprocessor Peripheral for Viewdata (LUCY)

SAA5070

The SAA5070 is a complex microcomputer/microprocessor peripheral integrated circuit in N-channel MOS technology intended for use in wired data communication systems, notably viewdata.

Features

- Microcomputer/microprocessor interface. • Modem – both 1200/75 and 1200/1200 baud.
- Line "UART" and tape recorder "UART", both with software parity control (or 8-bit without parity).
- Tape recorder modem (modified 'Kansas City' standard 1300 baud).
- Autodialler for British Post Office and Continental requirements.
- IBUS receivers and transmitters. • Timer circuits (60 s and 1.5 s time-outs).
- General input/output ports.
- Provision for connection of any external modem through V24 interface.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	75	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

5

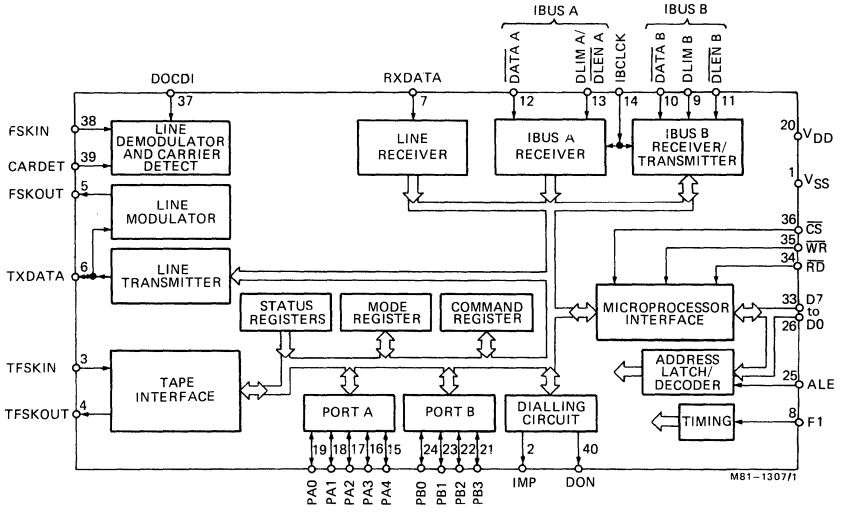


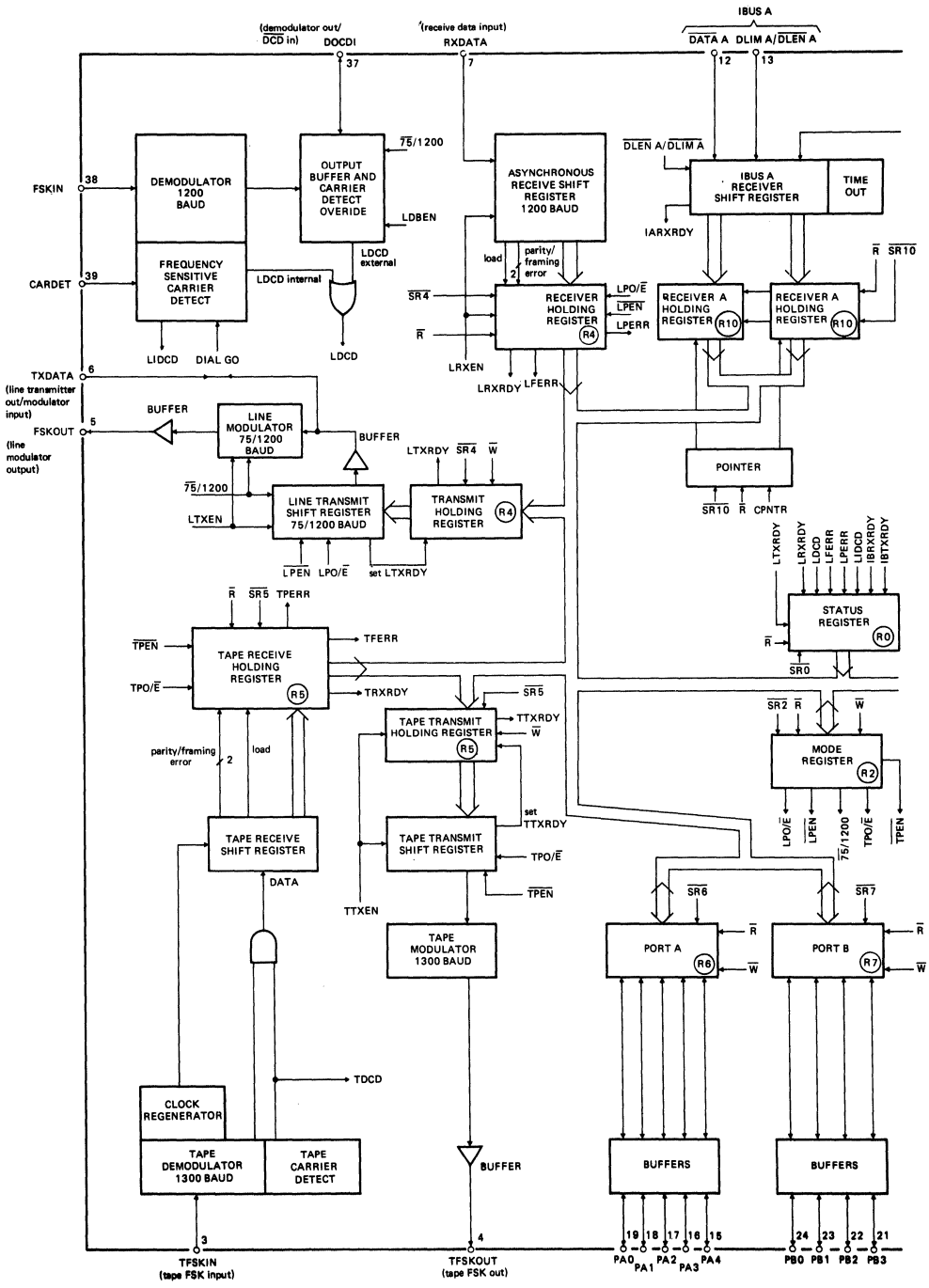
Fig.1a Simplified block diagram

PACKAGE OUTLINE

40-lead DIL; plastic (SOT–129).

Microcomputer/Microprocessor Peripheral for Viewdata (LUCY)

SAA5070



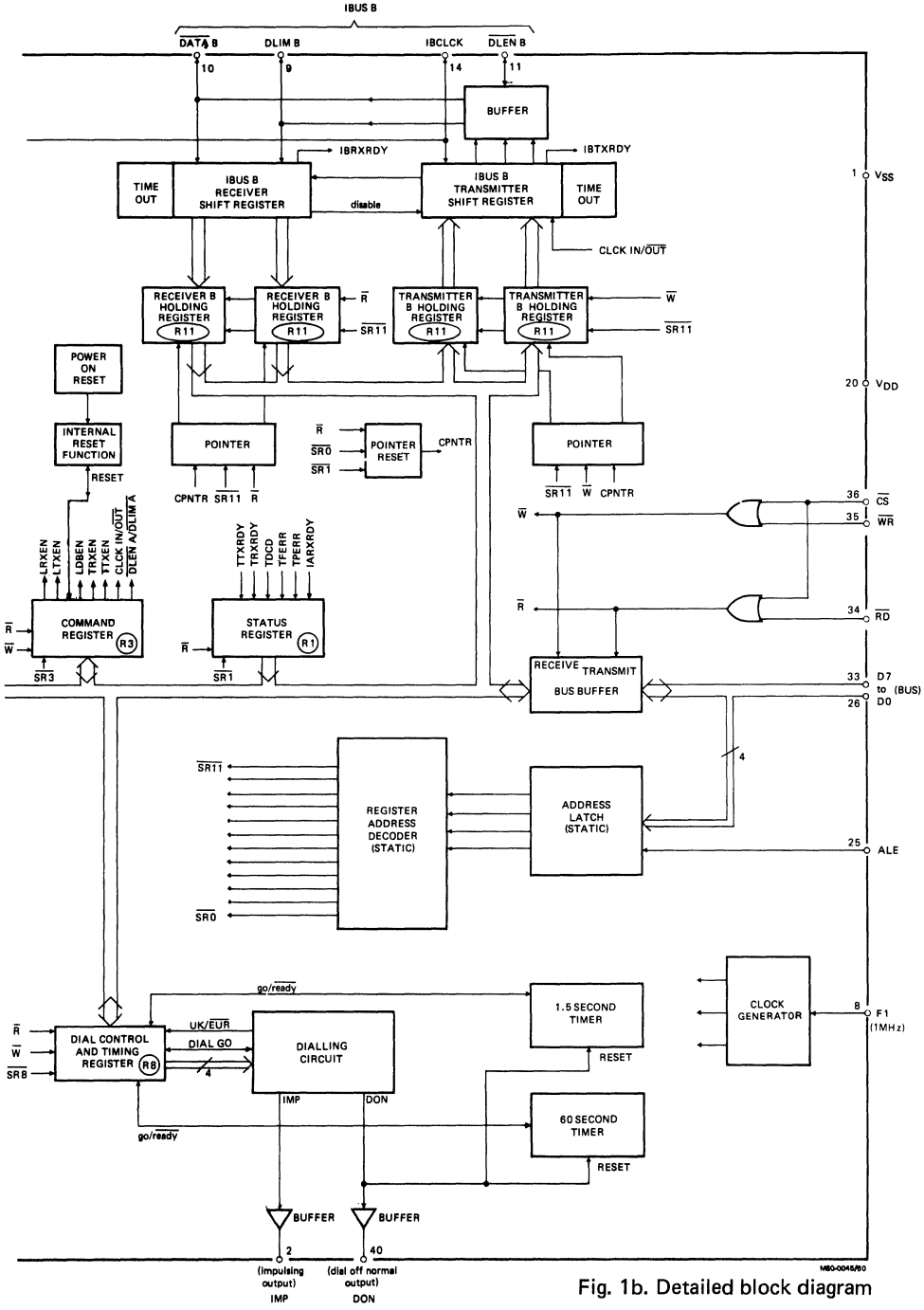


Fig. 1b. Detailed block diagram

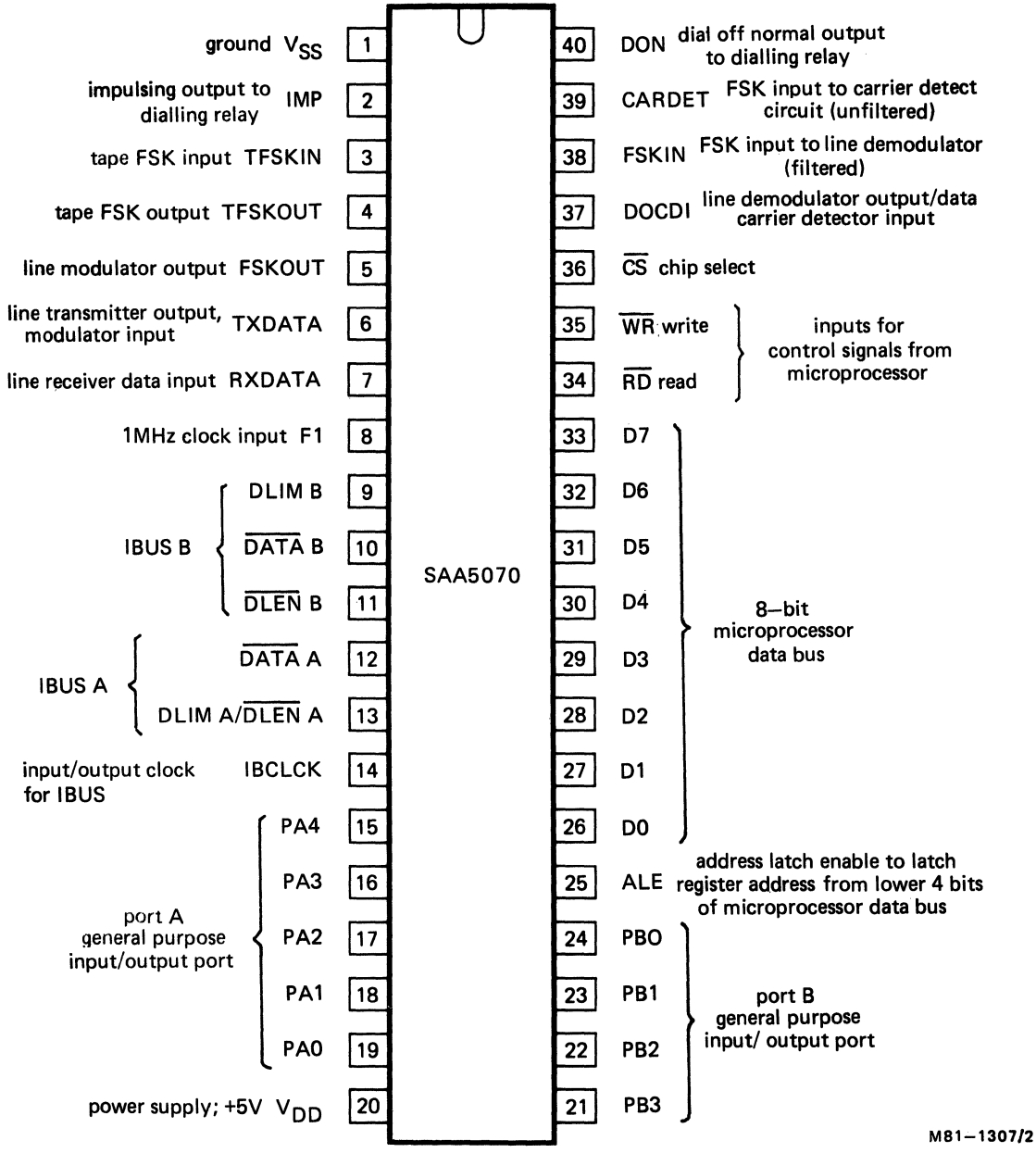


Fig.2 Pinning diagram

Microcomputer/Microprocessor Peripheral for Viewdata (LUCY) — SAA5070

DESCRIPTION

The SAA5070 is a 40 pin integrated circuit in N-channel MOS with a 1 MHz clock supplying all the operating frequencies. It performs most of the hardware functions of a viewdata terminal including an autodialling circuit, a 1200 baud demodulator and asynchronous receiver, and a 75/1200 baud modulator and asynchronous transmitter.

The device also includes a tape interface circuit suitable for the recording of character codes of pages of text on a standard audio cassette recorder, and an IBUS receiver and receiver/transmitter on separate ports enabling the software recoding of IBUS transmissions. The 75 baud modulator and asynchronous transmitter can be switched to operate at 1200 baud for private telecommunications systems.

There are also two general purpose input/output ports. Port A could, for example, be used as an interface to a non volatile RAM which can store telephone numbers for autodialling and user passwords and Port B could be used for display control.

The SAA5070 has been partitioned for flexibility of use, e.g. an external modem can be used, if required, in conjunction with the internal asynchronous receiver and transmitter, or the internal modem can be used independently of the internal receiver and transmitter. Also the tape interface can work independently of, and simultaneously with, the line receiver.

5

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See 'HANDLING MOS DEVICES').

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

		min.	typ.	max.	
Voltages (with respect to pin 1)					
Supply voltage (pin 20)	V_{DD}	−0.3	–	7.5	V
Input voltage:					
PORT A (pins 15 to 10) and PB0 (pin 24)	V_I	−0.3	–	14.0	V
Input voltage (all other pins)	V_I	−0.3	–	7.5	V
Temperatures					
Storage temperature range	T_{stg}		−20 to +125		°C
Operating ambient temperature range	T_{amb}		−20 to +70		°C

CHARACTERISTICS

Supply voltage (pin 20)	V_{DD}	4.5	–	5.5	V

The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.

Supply current	I_{DD}	–	75	150	mA
Inputs					
All inputs (except F1 clock)					
Input voltage; LOW	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

Data specific to certain inputs

		min.	typ.	max.	
F1 (1 MHz) Clock					
Input voltage; LOW	V_{IL}	−0.3	–	0.6	V
Input voltage; HIGH	V_{IH}	2.2	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Mark/space ratio (measured at 1.5 V level)		40:60	–	60:40	
$\overline{\text{DATA}}$ A, DLIM A/$\overline{\text{DLEN}}$ A (IBUS A)					
Data set up time	t_{DS}	3	–	–	μs
Data hold time	t_{DH}	3	–	–	μs
DLIM clock; HIGH	t_{CH}	4	–	–	μs
DLIM clock; LOW	t_{CL}	4	–	62	μs
Time between commands	t_{BC}	140	–	∞	μs
DLIM frequency	f_{DLIM}	16	–	160	kHz
ALE (Address Latch Enable) (Figs. 3 and 4)					
Pulse width (HIGH)	t_{ALEH}	400	–	–	ns
Cycle time	T_{ALE}	–	2500	–	ns
$\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{CS}}$ (Figs. 3 and 4)					
Control pulse width	t_{WL}	–	700	–	ns
Address hold time	t_{LA}	80	–	–	ns
Address set-up time	t_{AL}	120	–	–	ns
Read cycle timings (Fig.3) ALE to read pulse delay time	t_{ALR}	80	–	–	ns
Read pulse (falling edge) to data bus delay time	t_{RD}	–	–	500	ns
Data hold time	t_{DR}	0	–	200	ns
Write cycle timings (Fig.4) ALE to write pulse delay time	t_{ALW}	80	–	–	ns
Address set-up time to $\overline{\text{WR}}$	t_{AW}	230	–	–	ns
Data set up time before $\overline{\text{WR}}$	t_{DW}	500	–	–	ns
Data hold time after $\overline{\text{WR}}$	t_{WD}	120	–	–	ns

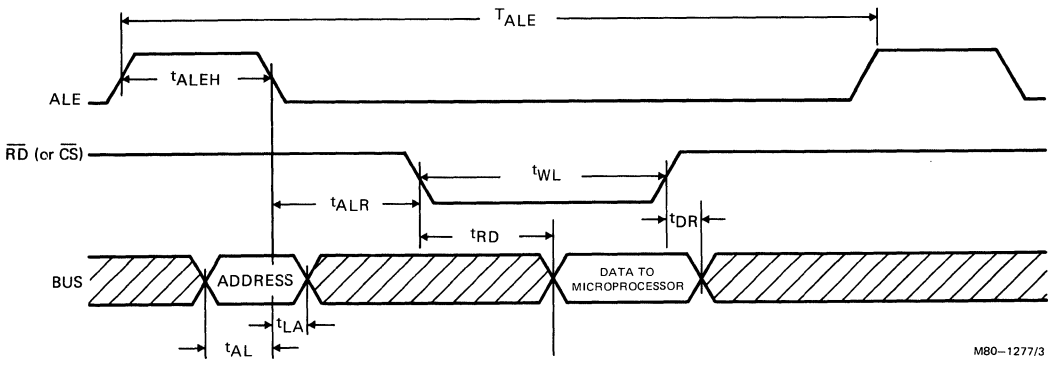


Fig.3 Read cycle timing

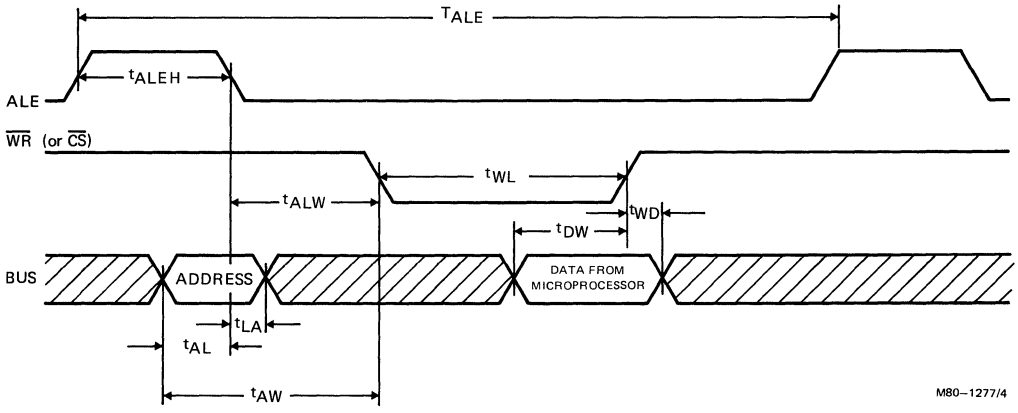


Fig.4 Write cycle timing

Inputs/Outputs

These are protected against connection to V_{SS} or V_{DD}

			min.	typ.	max.	
$\overline{DATA}$ B, DLIM B, $\overline{DLEN}$ B, IBCLCK (IBUS B)						
Input voltage; LOW	Fig.14	V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input leakage current (V_I = 0 to 5.5 V) (3 state buffers off)		I_{IR}	–	–	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Output voltage; HIGH (−I_{OH} = 200 μA)		V_{OH}	2.4	–	–	V
Output rise and fall times (C_L = 300 pF)		t_r, t_f	–	–	1	μs
other timings as IBUS A						
DOCDI (open drain output)						
Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input leakage current; (V_I = 0 to 5.5 V) (output transistor off)		I_{IR}	–	0.4	10	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	0.4	–	V
TXDATA						
(Internal resistive pull-up, permitting wired - AND connection)						
Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	5.5	V
Input current; LOW (V_I = 0.4 V)		$-I_{IL}$	–	–	500	μA
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Output voltage; HIGH (−I_{OH} = 50 μA)		V_{OH}	2.4	–	–	V
Load capacitance		C_L	–	–	40	pF
Output rise time (C_L = 40 pF)		t_r	–	3	–	μs
PA0 to PA4 (PORT A) (open drain output)						
Input voltage; LOW		V_{IL}	−0.3	–	0.8	V
Input voltage; HIGH		V_{IH}	2.0	–	13.2	V
Input capacitance		C_I	–	–	7	pF
Output voltage; LOW (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 13.2 V)		I_{OR}	–	–	10	μA
Load capacitance		C_L	–	–	40	pF
Fall time		t_f	–	–	1	μs

Inputs/Outputs (continued)		min.	typ.	max.	
PBO (PORT B) (open drain output) as PORT A except					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH	V_{OH}	–	–	13.2	V
Load capacitance	C_L	–	–	100	pF
PB1 to PB3 (PORT B)					
Input voltage; LOW	V_{IL}	–0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Input capacitance	C_I	–	–	7	pF
Load capacitance	C_L	–	–	100	pF
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Off state leakage current (V_I = 0 to 5.5 V)	I_{OR}	–	–	10	μA
D0 to D7 (8-bit Data bus)					
Input voltage; LOW	V_{IL}	–0.3	–	0.8	V
Input voltage; HIGH	V_{IH}	2.0	–	5.5	V
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Input leakage current (V_I = 0 to 5.5 V) (3-state buffers off)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output rise and fall times (C_L = 150 pF)	t_r, t_f	–	–	150	ns
Outputs					
These are protected against connection to V_{SS} or V_{DD}.					
FSKOUT and TFSKOUT					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Rise and fall times (C_L = 100 pF)	t_r, t_f	–	–	500	ns
DON and IMP					
Output voltage; LOW (I_{OL} = 50 μA)	V_{OL}	–	–	0.2	V
Output current; HIGH (V_{OH} = 0.8 V clamped)*	I_{OH}	200	–	2000	μA
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	–	V
Autodialling timings are given in Fig.6					

*These outputs are normally intended to drive the base-emitter junction of a bipolar transistor and so in normal use the V_{OH} may be clamped to V_{be}.

RESET FUNCTION

It is possible to reset the SAA5070 to its nominal state either automatically on power-on by means of an internal power-on reset circuit, or by setting D5 in command register (R3) to '1', which returns to '0' on completion of the reset sequence. The device resets to viewdata mode, i.e. 75 baud transmit rate, even parity, etc, as shown by the all zero's state in registers R0 to R3, R6, R7 and R8 except for LTXRDY, IBTXRDY, and TTXRDY (in the status registers R0 and R1) which will come up as '1' after the transmitters have been reset, showing that they are ready to accept new data.

APPLICATION DATA

Chip organisation

Each section of the SAA5070 may be accessed by the microprocessor via a register (of up to 8-bits) connected to an internal data bus. There are 15 registers on chip accessed by 11 addresses. Some of the registers are two-level, i.e. two bytes of data are transferred by two successive read (or write) sequences to the same address, also some read only registers have the same address as a write only register.
An appendix lists the registers, their contents, and their use.

Section descriptions

The description of each section includes associated registers, flags, and pins, as well as the method of operation. On the following block diagrams external pins are shown boxed and internal flags are shown underlined.

Microprocessor Interface

D0 to D7 — I/O — 8-bit input/output port

Associated pins:	ALE	input	address latch enable from microprocessor
	$\overline{WR}$	input	write pulse from microprocessor
	$\overline{RD}$	input	read pulse from microprocessor
	$\overline{CS}$	input	chip select

Operation

The control microprocessor communicates with the SAA5070 via an 8-bit data I/O port D0 to D7. An internal read or write pulse is produced by gating $\overline{RD}$ and $\overline{WR}$ with $\overline{CS}$. A single register is enabled onto the internal bus by gating the read or write lines with the address decoder outputs. The register address is taken from the 4 least significant data bits latched on the falling edge of ALE. (See timing diagrams Figs. 3, 4). The address (D3 most significant, D0 least significant) relates directly to the register numbers shown in the register map, detailed in the appendix, and referred to in other section descriptions.

Four registers not specifically related to any one section are included. These are the status registers R0 and R1, the mode register R2, and the command register R3. These registers are used to determine the current status of the device, to dictate the mode of operation or to initiate a specific operation. The status registers are read only, the mode and command registers are read/write. When writing to these registers, it is recommended that the unallocated bits are set to '0'. On reading the registers the state of the unallocated bits should be assumed to be random. The exact functions of the flags contained in these registers are described in the section description to which they relate.

Autodial section (see Fig.5)

Associated Register: — R8 — D0 to D3 write only
D4 to D7 read/write

Associated flags in other registers: None

Associated pins: DON output, IMP output } to drive dialling relays

Operation

The autodial section includes a clock divider, a digit impulse counter, a sequence controller and an impulse generator (see block diagram Fig.5). A sequence to generate the impulses for one digit is initiated by setting D5 (DIAL GO) to '1', D3 to D0 to the binary code of the required digit, and D7 to the required mode. This initiates the sequence controller which loads the binary code into the digit impulse counter. The counter then generates the correct number of impulses at the rate of 10 per second, together with a DON pulse which overlaps the impulses by about 7 ms at the start and end (see Figs.6, 7); the interdigit pause period is also added by the sequence controller. D5 is reset to '0' at the end of a dialling sequence and may be read by the microprocessor to determine when the dial circuit is free to accept the next digit.

D7 (UK/$\overline{\text{EUR}}$) determines the mark/space ratio of the IMP pulses

UK = 2 off to 1 on
$\overline{\text{EUR}}$ = 1.5 off to 1 on
} both one pulse per 100 ms

There is a timer in the dial circuit which can be used to time out 1.5 seconds or 60 seconds by setting D4 or D6 respectively. These bits are read/write and are reset after the relevant time out period. In addition the 60 second timer can be reset by writing a '0' to D6. The 60 second timer may be used typically by the microprocessor to release the telephone line if connection has not been made within 60 seconds. The DON pulse resets the counter so that the time out is taken from the end of the last digit dialled. Once a dialling sequence for one digit has been initiated, R8 should be used only in read mode until D5 has been reset internally to '0' indicating the end of the dial sequence for that digit.

When D5 (DIAL GO) is set to '1' the carrier detect circuit (see the next section and Fig.8) is disabled.

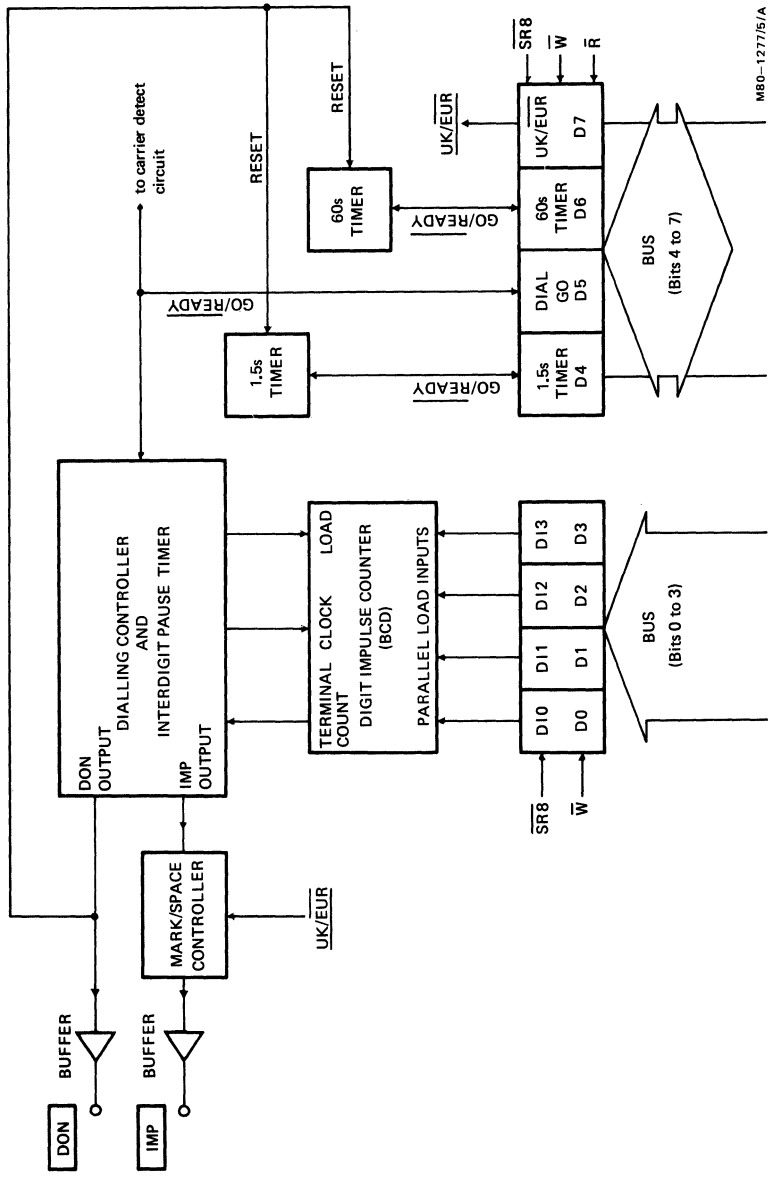


Fig.5 Autodial block diagram

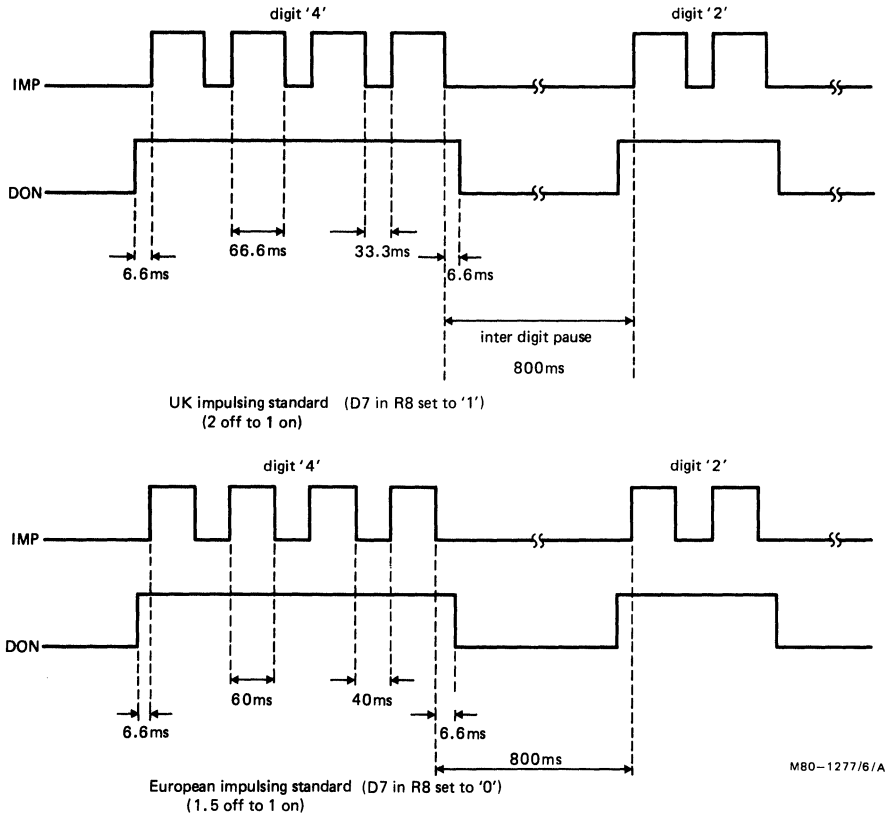


Fig.6 Autodialling timing

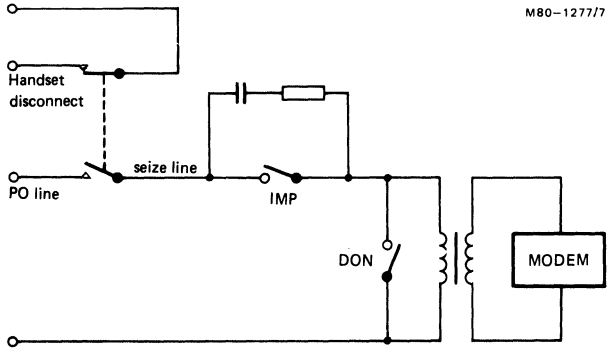


Fig.7 Simplified relay diagram

Line Demodulator and Carrier Detect (see Fig.8)

Associated Register:– None

Associated flags in other registers:

LIDCD	–	D2	–	R0 (Status)	–	instantaneous carrier detect flag
LDCD	–	D5	–	R0 (Status)	–	carrier detect flag
$\overline{75}$/1200	–	D5	–	R2 (Mode)	–	transmit frequency baud rate (used in demodulator carrier detect circuit)
LDBEN	–	D4	–	R3 (Command)	–	line demodulator output buffer and carrier detect enable
DIAL GO	–	D5	–	R8 (Dial control)	–	used to disable carrier detect circuit during dialling sequence

Associated pins:	FSKIN	– input	–	filtered, squared F.S.K. signal
	CARDET	– input	–	unfiltered (squared) F.S.K. signal.
	DOCDI	– input/output	–	demodulator output, external LDCD in

Operation

The input to the demodulator is the previously filtered and squared up F.S.K. signal from the telephone line. Its output is a pseudo analogue signal which must be externally filtered and squared to produce the demodulated data. The carrier detect circuit functions in the following modes:

a) Viewdata mode (1200 baud receive, 75 baud transmit). Initially, a narrow frequency band 'window' around 1300 Hz is accepted as carrier, this must be applied to the CARDET input. If a frequency in this range is present, the 'instantaneous carrier detected' flag will be HIGH (LIDCD), after about 2 seconds the 'line carrier detected' flag will be set HIGH (LDCD). When this occurs, the frequency window is widened to include 2100 Hz and the circuit no longer takes its input from the CARDET pin, but from the FSKIN pin.
If carrier is then removed LIDCD immediately goes LOW, and after about 1 second LDCD is reset, the frequency window again becomes narrow and around 1300 Hz and the CARDET input again becomes active. Reappearance of carrier in the 1300 Hz range will cause a repeat of the above.

b) 1200 baud each way mode
Only the instantaneous carrier detect is active in this mode. LDCD is forced LOW and the CARDET input inhibited (only FSKIN should be used in this mode).

c) External carrier detect input
If an external modem is used its (active LOW) carrier detect output is connected to DOCDI. Provided that the demodulator is not enabled, LDCD will be set if DOCDI is LOW and reset if it is HIGH.

Demodulator enable

LDCD is produced by the carrier detect circuit, which is enabled by LDBEN and disabled by DIAL GO, In the viewdata mode the demodulator is enabled by LDCD.
In the 1200 baud each way mode the demodulator is enabled directly by LDBEN.

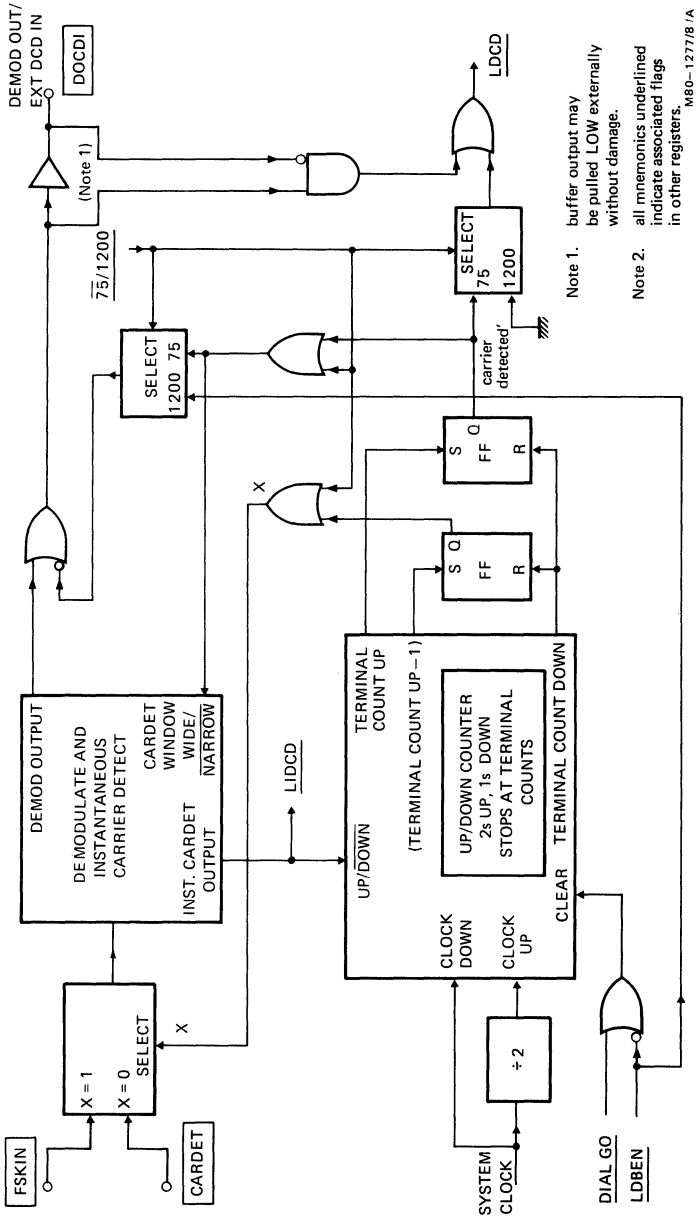


Fig.8 Line demodulator and carrier detect block diagram

5

Line Receiver (see Fig.9)

Associated Register: — R4 read only

Associated flags in other registers:

LRXRDY	—	D6	—	R0 (status)	—	valid data available in receive holding register
LFERR	—	D4	—	R0 (status)	—	line framing error (derived from STOP bit of message).
LPERR	—	D3	—	R0 (status)	—	line parity error.
LPO/$\overline{E}$	—	D7	—	R2 (mode)	—	odd or even parity detection mode select
$\overline{LPEN}$	—	D6	—	R2 (mode)	—	8 bit data or 7 bit plus parity mode select
LRXEN	—	D7	—	R3 (command)	—	line receiver enable.

Associated pins: RXDATA — input — received data input

Operation

The receiver may be configured to work with either 7 data bits and 1 parity, or with 8 data bits and no parity. Odd or even parity can be detected on chip, the LPERR flag being set when an error is detected. The required mode of operation should be selected by setting $\overline{LPEN}$ and LPO/$\overline{E}$ to the required states by writing to mode register (R2) before enabling the receiver by setting LRXEN to '1' in command register (R3). The data format is 10 bits per data word. The data word is made up of a start bit (LOW), 8 data bits, the 8th being an optional parity bit, and a stop bit (HIGH). The receive data will remain HIGH after the stop bit until the next data word. When the receiver has been enabled a negative transition is looked for on the RXDATA input indicating a possible start bit. After half a bit rate period the data is sampled again and if it is still LOW it is interpreted as a start bit, initiating a sequence which clocks the data into a shift register. When the full ten bit message has been received, the 8 data bits are parallel loaded into the receiver holding register (R4), the LRXRDY flag is set to '1'. The complement of the stop bit is loaded into the LFERR latch and the result of the parity check is loaded into LPERR latch. If line parity is not enabled i.e. $\overline{LPEN}$ = '1', then LPERR is held at '0'. The LRXRDY flag is reset to '0' after the microprocessor has read the receiver holding register (R4). The receiver has a 52 times baud rate factor to allow for maximum isochronous distortion.

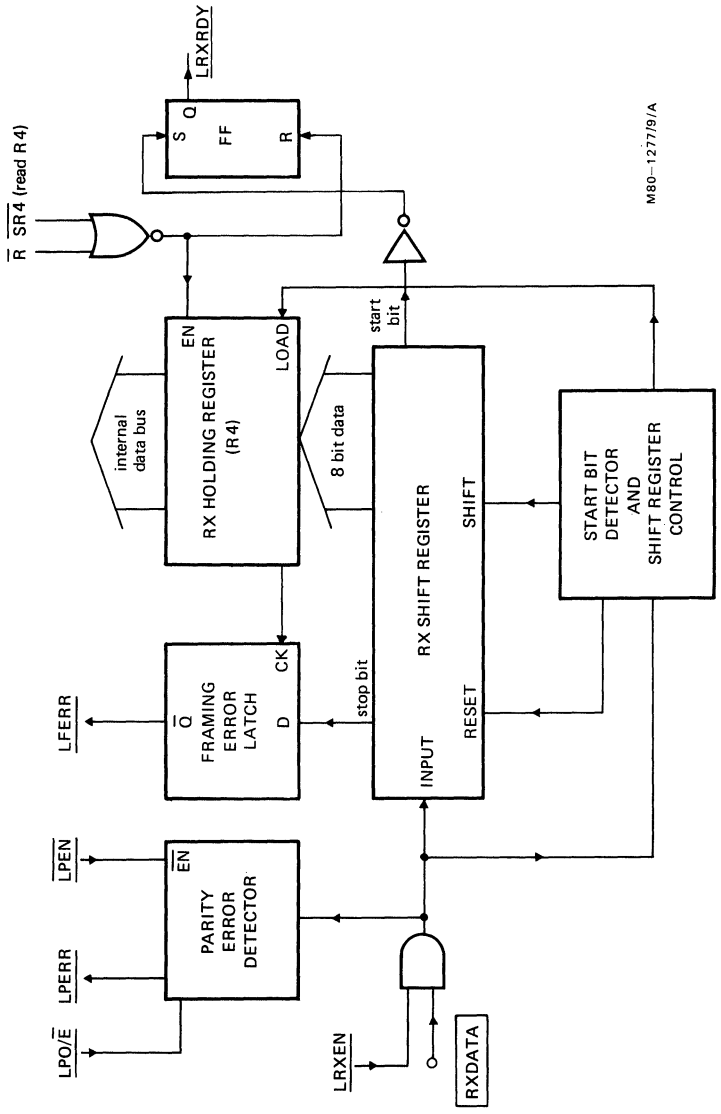


Fig.9 Line receiver block diagram

5

Line Transmitter (see Fig.10)

Associated Register: – R4 write only

Associated flags in other registers:

LTXRDY	–	D7	–	R0 (status)	–	transmit holding register ready to accept new data
LPO/$\overline{E}$	–	D7	–	R2 (mode)	–	odd or even parity mode select
$\overline{\text{LPEN}}$	–	D6	–	R2 (mode)	–	8 bit data or 7 bit data with parity mode select
$\overline{75}$/1200	–	D5	–	R2 (mode)	–	select transmit baud rate
LTXEN	–	D6	–	R3 (command)	–	line transmitter/modulator output enable

Associated pins: TXDATA – I/O – transmitter output (and also modulator input)

Operation

The data format of the transmitter is the same as that of the line receiver i.e. 10-bits, a start bit (LOW) followed by 8-data bits, the 8th bit being an optional parity (selected by LPEN), odd or even parity being selectable (by LPO/$\overline{E}$) ending with a STOP bit (HIGH) the output remaining HIGH until the next data word is written.

The transmitter and modulator may be used together or separately. The transmitter output is brought to the TXDATA pin (if LTXEN = 1) which is connected internally to the modulator input. The TXDATA pin has an internal resistive pull up permitting wire - AND connection. If the modulator is used with an off chip data source (e.g. UART) then data should not be written to the internal transmit holding register (R4). The STOP bit (HIGH) will then be continuously output when LTXEN = 1 (required to enable modulator output) allowing the external UART to control the TXDATA (pin 6).

To operate the transmitter the required mode should be set-up initially by writing to the mode register (R2) the required states of $\overline{75}$/1200, $\overline{\text{LPEN}}$, LPO/$\overline{E}$. The transmitter can then be enabled by setting LTXEN to '1' in the command register (R3). The 8-bit data word can then be written to the transmit holding register (R4). If parity is enabled then the 8th bit is ignored and the value of the parity bit calculated from the first 7-data bits and LPO/$\overline{E}$. The LTXRDY flag is set to zero when the holding register is written into. If the transmit output shift register is not currently in use the contents of the holding register are transferred to the output shift register and LTXRDY returns to '1'. This means that new data may now be written to the holding register but will not be transferred to the output shift register until the 10-bits of the current message have been clocked out. The start, stop, and parity bit (if selected) are written into the output shift register with the data word automatically.

Two transmit baud rates are selectable, 75 baud for viewdata transmissions or 1200 baud for private data communication systems.

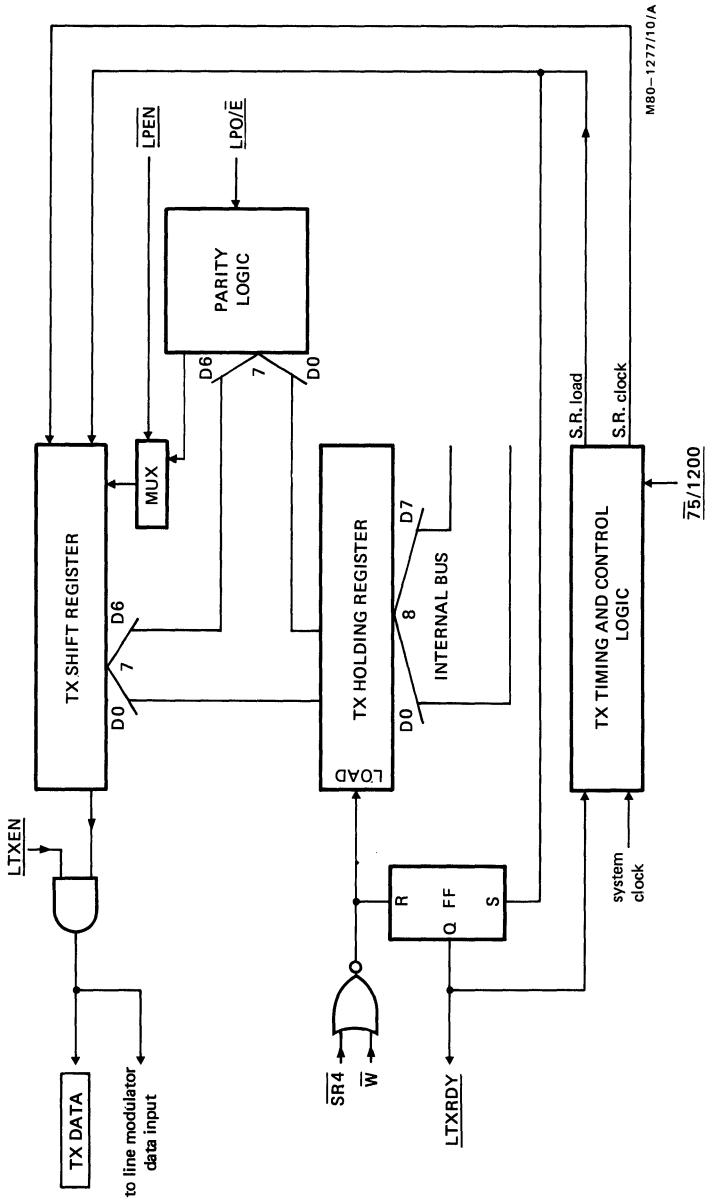


Fig.10 Line transmitter block diagram

Line Modulator (see Fig.11)

Associated Register: — None

Associated flags in other registers:

$\overline{75}$/1200	—	D5	—	R2 (mode)	—	transmit baud rate select.
LTXEN	—	D6	—	R3 (command)	—	line transmitter/modulator output enable.

Associated Pins:	TXDATA	—	I/O	—	modulator input (also (on chip) transmitter output).
	FSKOUT	—	output	—	line modulator output

Operation

The modulator generates a pseudo analogue signal from a serial shift register which is parallel loaded with patterns from an internal ROM. The frequency of the sine wave is determined by the selected baud rate $\overline{75}$/1200, and the value of the data on TXDATA (pin 6).

data	'1'	'0'
1200 baud	1300 Hz	2100 Hz
75 baud	390 Hz	450 Hz

One sine wave cycle is comprised of a 92-bit pattern which after minimal external low pass filtering provides a suitable F.S.K. signal out (see Fig.11)

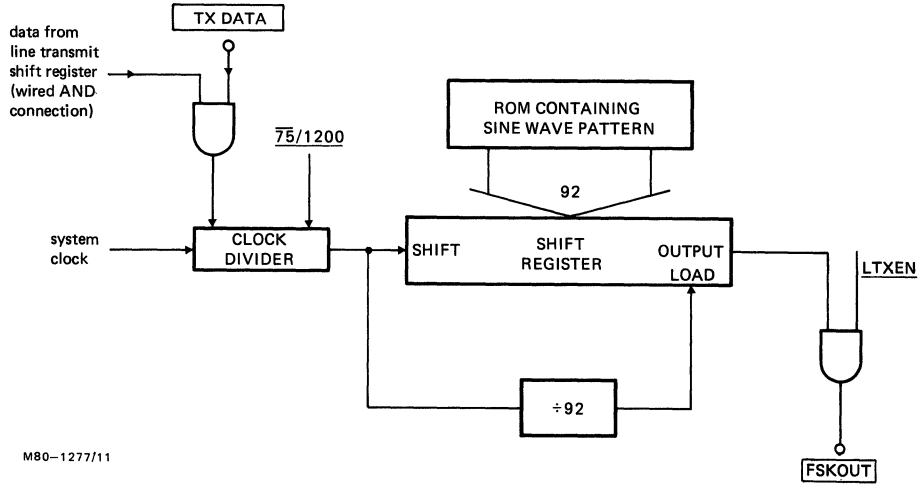


Fig.11 Line modulator block diagram

Tape section (see Fig.12)

Associated registers: — R5 — Consists of two registers with the same address:
transmit holding register write only
receive holding register read only

Associated flags in other registers:

TTXRDY	—	D7	—	R1 (status)	—	transmit holding register ready to accept new data
TRXRDY	—	D6	—	R1 (status)	—	valid data available in receive holding register
TDCD	—	D5	—	R1 (status)	—	tape data carrier detect flag
TFERR	—	D4	—	R1 (status)	—	tape framing error (derived from STOP bit of message)
TPERR	—	D3	—	R1 (status)	—	tape parity error
TPO/$\overline{E}$	—	D3	—	R2 (mode)	—	odd or even parity mode select.
$\overline{TPEN}$	—	D2	—	R2 (mode)	—	8-bit data or 7-bit plus parity mode select
TRXEN	—	D3	—	R3 (command)	—	tape receiver enable
TTXEN	—	D2	—	R3 (command)	—	tape transmitter enable

Associated pins:	TFSKIN	— input	—	F.S.K. input to tape sections
	TFSKOUT	— output	—	F.S.K. modulated data out

5

Operation of tape section (see Fig.12)

The tape data modulation system is a modified form of the 'Kansas City' standard. A logic '1' is represented by one cycle of 1300 Hz, and a logic '0' by two cycles of 2600 Hz, the data rate being 1300 baud. The data format is the same as that for viewdata, i.e. 10-bit words consisting of a START bit (LOW), followed by 8-data bits, the 8th being an optional parity bit, ending with a STOP bit (HIGH) which is continuous until the next data word.

To operate the tape section the required parity mode should first be set up by writing the required states of TPEN and TPO/$\overline{E}$ to the mode register (R2). The TTXEN command enables the output of the transmit shift register into the modulator, and should be set before data is written to the transmit holding register. (With TTXEN = '0' the modulator outputs a continuous 1300 Hz signal '1'). When a data word is written to the transmit holding register the TTXRDY flag is reset to '0'. If the transmit shift register is not currently active the contents of the holding register, along with valid parity bit (if enabled) and the START and STOP bits are transferred to the transmit shift register, at the same time TTXRDY is set to '1'. The holding register is then free to accept new data but this will not be transferred to the shift register until the current data has been clocked out. Data should be written to the tape transmit holding register, therefore, only when TTXRDY = '1'.

The modulator produces 1300 Hz and 2600 Hz signals which occur synchronously with the data from the transmitter. Hence a '1' is one complete 1300 Hz cycle, and a '0' two complete 2600 Hz cycles. The modulator output, TFSKOUT, requires minimal external low pass filtering to produce data suitable for audio cassette tape recorders.

To overcome the tendency of cassette recorders to attenuate high frequencies, the 1300 Hz signal contains 2 μs wide attenuating pulses every 12 μs. This reduces the 1300 Hz signal by approximately 3 dB relative to the 2600 Hz signal after external filtering.

The data rate of 1300 baud is slightly faster than the 1200 baud line receive rate, allowing incoming data from the line to be transferred simultaneously (via the microprocessor) to tape.

The TFSKIN input accepts the previously filtered and squared data from the tape recorder. The demodulator uses the fact that the modulated data is in phase with clock to regenerate the clock from the data. This permits a wide tolerance on replay speeds. A carrier detect circuit is included which sets the TDCD flag to '1' if carrier (1300 Hz or 2600 Hz) is valid for 100 ms. If carrier is lost for 100 ms the TDCD flag is reset to '0'. This flag may be read by the microprocessor to determine when to enable the tape receiver by setting TRXEN to '1'.

If TRXEN is set, then on detection of a start bit (LOW) data is shifted into the tape receive shift register by the clock which has been extracted from the data. After ten clocks, the contents of the shift register are transferred to the receive holding register. At the same time the complement of the STOP bit is loaded into the TFERR latch, the results of the parity calculation loaded into the TPERR latch, and TRXRDY is set to '1'. The TRXRDY flag is read by the microprocessor to identify when valid data is in the holding register and is reset to '0' when the holding register (R5) is read.

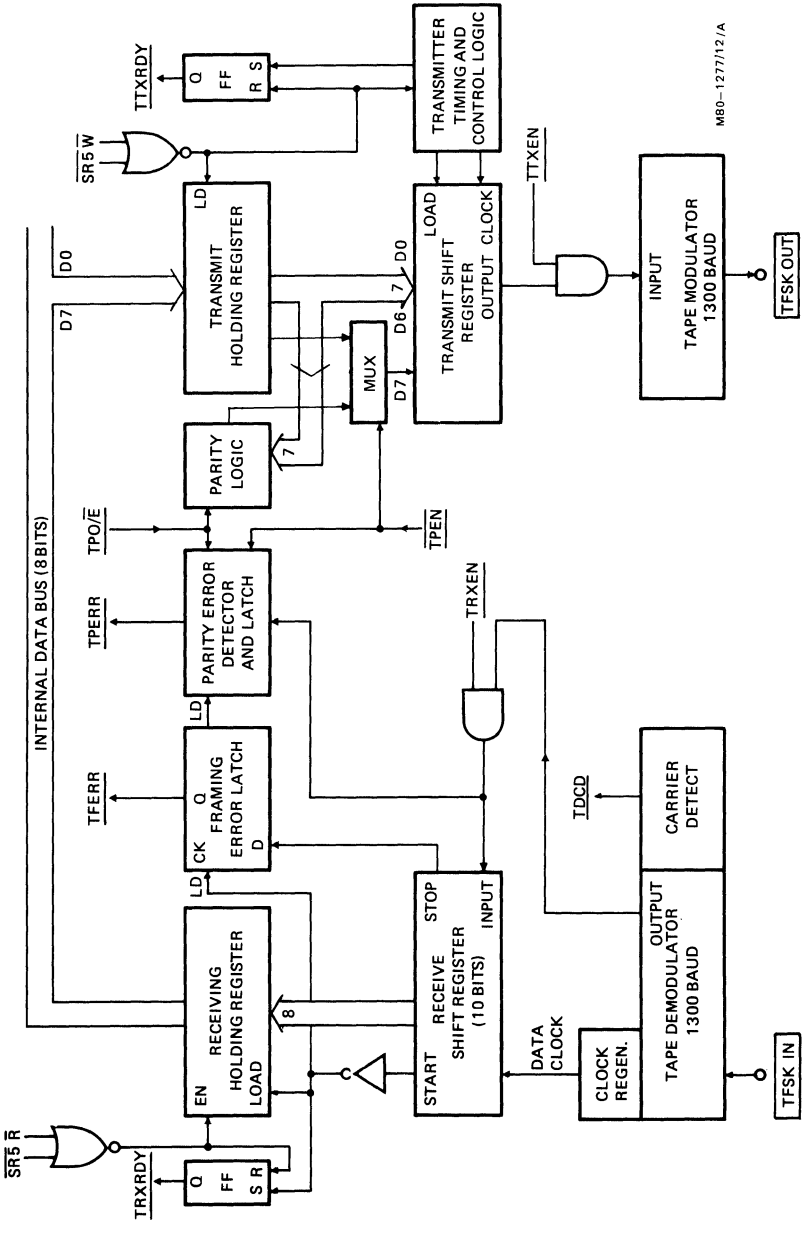


Fig.12 Tape section block diagram

5

IBUS A receiver and IBUS B receiver/transmitter (see Fig.13)

Associated registers:

Receiver A (2 bytes) – R10 – read only
Receiver B (2 bytes) – R11 – read only
Transmitter B (2 bytes) – R11 – write only

Associated flags in other registers:

IBRXRDY	–	D1	– R0 (status)	–	valid data available in receiver B holding register
IBTXRDY	–	D0	– R0 (status)	–	transmitter B holding register ready to accept new data
IARXRDY	–	D1	– R1 (status)	–	valid data available in receiver A holding register
CLCK IN/$\overline{\text{OUT}}$	–	D1	– R3 (command)	–	input/output control for 62.5 kHz pin
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	–	D0	– R3 (command)	–	3-line/2-line control for IBUS A receiver.

Associated pins:

$\overline{\text{DATA}}$ A	– input	–	receiver A data input
DLIM A/$\overline{\text{DLEN}}$ A	– input	–	receiver A data clock or bus enable signal
$\overline{\text{DATA}}$ B	– I/O	–	receiver B data input/transmitter B data output
DLIM B	– I/O	–	receiver B data clock input/transmitter B data clock output
$\overline{\text{DLEN}}$ B	– I/O	–	receiver B bus enable input/transmitter B bus enable output
IBCLCK	– I/O	–	62.5 kHz clock input/output

Operation

All three IBUS circuits (receiver A, receiver B, and transmitter B) are capable of handling variable length codes from 1 to 12 bits. (In fact 15 bits can be transmitted 12 being data the rest being trailing zero's, and 15 bits may be received but only the last 12 being retained). Each of the three circuits have two 8-bit registers which are accessed by two successive read or write operations to the same address. There is a pointer for each pair of registers which selects the first or second byte. The pointers act in a bistable fashion with each access and are reset to point to the first byte with power on, D5 set in R3, or by reading either of the status registers R0 and R1. The two bytes of data in each holding register contain 12 bits of message, and 4-bits which specify the word length of message. For the transmitter the word length is used to generate the correct number of data clocks, for the receivers it may be used to identify the source of the message, or to establish that the message was a valid length.

The contents of each receiver register pair is organised as:

1st byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10A RXB – R11A	L – 4	L – 5	L – 6	L – 7	L – 8	L – 9	L – 10	L – 11

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10B RXB – R11B	Word length MSB	Word length	Word length	Word length LSB	L	L – 1	L – 2	L – 3

Where L, L – 1 etc. means last data bit received, last minus one etc.

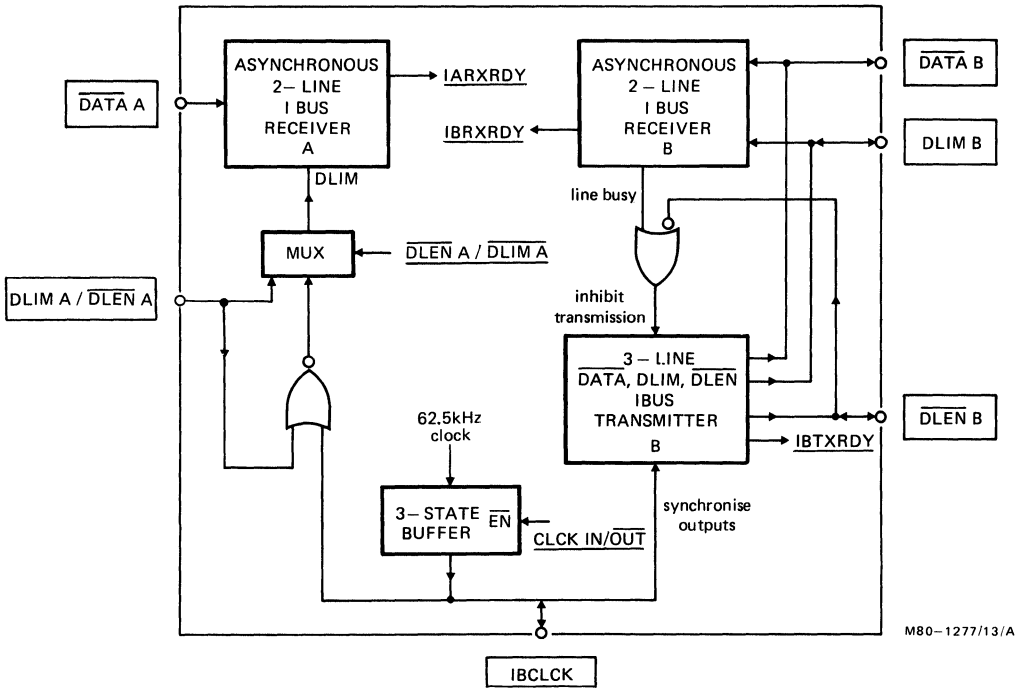


Fig. 13 IBUS block diagram

For the transmitter the register pair is organised as:

1st byte	D7	D6	D5	D4	D3	D2	D1	D0
TXB – R11A	8	7	6	5	4	3	2	1

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
TXB – R11B	Word length MSB	Word length	Word length	Word length LSB	12	11	10	9

Where 1, 2, etc. means first data bit transmitted, second data bit transmitted, etc.

IARXRDY or IBRXRDY (D1 in status registers R1 and R0) are set when a message has been received by RXA or RXB respectively. These flags also inhibit the receive holding registers from being overwritten by subsequent messages until the holding registers have been read. Reading a holding register pair will reset the relevant IARXRDY or IBRXRDY flags.

Transmitter B is initiated by writing two bytes to the transmit holding register (R11). This sets IBTXRDY to '0'. The DLIM line is sampled to detect the line busy state, and when the line is free a time out starts. If further DLIM's are detected before the end of the time out period the time out is reset and the sequence will begin again. When the time out has been completed the contents of the holding register are transferred to the output shift register and word length counter. The data and correct number of data clocks are then transmitted, at the completion of which IBTXRDY is returned to a '1'. New data should not be written to the transmit holding register (R11) while IBTXRDY = '0'. If the line is busy when a transmission is requested, the transmission will not start until 300 – 330 μs after the line becomes free (last DLIM). Receiver B is inhibited from receiving data transmitted by transmitter B.
Receiver A may operated either as a two line receiver with $\overline{\text{DATA}}$ and DLIM, or as a three line $\overline{\text{DATA}}$, $\overline{\text{DLEN}}$ and $\overline{\text{CLK}}$ receiver. DLIM A/$\overline{\text{DLEN}}$ A use the same pin, the function of which is selected by the $\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A command D0, register R3 (command).
The 62.5 kHz clock (pin IBCLCK) may be used either as an input for receiver A (as described above), or to synchronise transmitter B outputs, or as an output synchronous with transmitter B. The function is selected by CLCK IN/$\overline{\text{OUT}}$ command D1 in R3

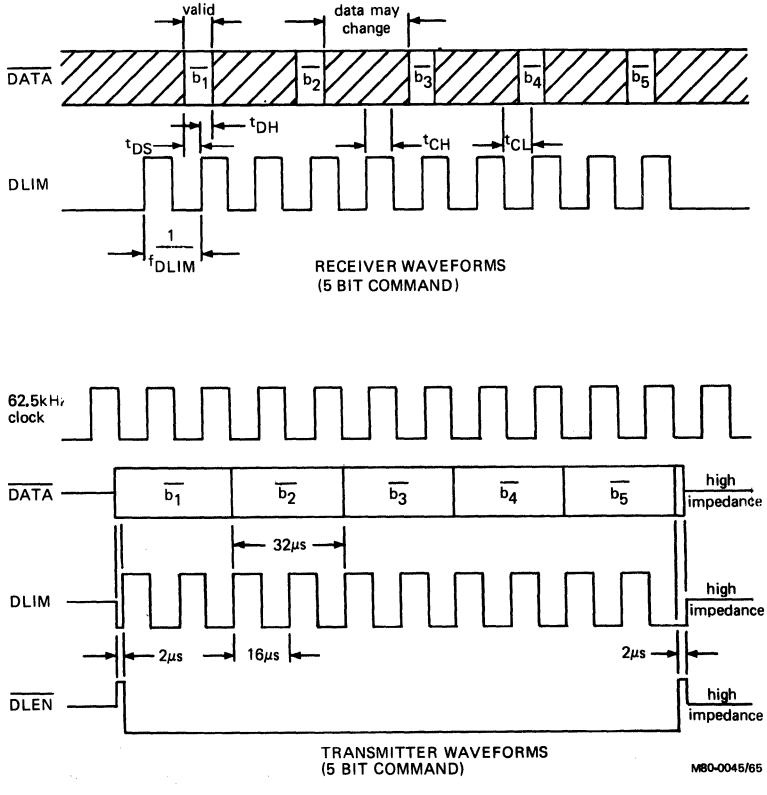


Fig. 14 IBUS waveforms

PORT A

Associated register: R6 – bits 0 to 4 – read/write

Associated pins: PA0 to PA4

Operation

This is a 5-bit general purpose input/output port. The outputs are latched and are open drain up to nominal 12 V.

The latches may be accessed by the microprocessor via BUS D0 to D7 by a read or write sequence to register R6. If any pin of the port is used as an input then its output latch must first be written with a '1'. This allows the external circuit to control the pin. The state of the pins may be read by the microprocessor by reading R6. If the supply to the open drain outputs is turned on before the V_{DD} supply to the IC, then the PORT must first be cleared by writing 1's to the output latch before operation.

PORT A might typically be used in viewdata mode as an interface to a non-volatile memory in which telephone and password numbers may be stored.

5

PORT B

Associated register: R7 – bits 0 to 3 – read/write

Associated pins: PB0 to PB3

Operation

This is a 4-bit general purpose input/output port. It behaves in exactly the same way as PORT A except that access is by addressing R7, and that outputs PB1 to PB3 are open drain to nominal 5 V. PB0 is open drain to nominal 12 V, and might typically be used in combined teletext/viewdata applications to control the Picture On function.

APPENDIX
Register map

	D7	D6	D5	D4	D3	D2	D1	D0	
R0	LTXRDY R	LRXRDY R	LDCD R	LFERR R	LPERR R	LIDCD R	IBRXRDY R	IBTXRDY R	STATUS REGISTER 0
R1	TTXRDY R	TRXRDY R	TDCD R	TFERR R	TPERR R		IARXRDY R		STATUS REGISTER 1
R2	LPO/$\overline{E}$ R/W	$\overline{\text{LPEN}}$ R/W	$\overline{75/1200}$ R/W		TPO/$\overline{E}$ R/W	$\overline{\text{TPEN}}$ R/W			MODE REGISTER
R3	LRXEN R/W	LTXEN R/W	RESET R/W	LDBEN R/W	TRXEN R/W	TTXEN R/W	CLCK IN/$\overline{\text{OUT}}$ R/W	$\overline{\text{DLEN A}}$/$\overline{\text{DLIM A}}$ R/W	COMMAND REGISTER
R4 R	PARITY OR B8 (R) R	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	LINE RECEIVE HOLDING REGISTER
R4 W	PARITY OR B8 (W) W	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	LINE TRANSMIT HOLDING REGISTER
R5 R	PARITY OR B8 (R) R	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	TAPE RECEIVE HOLDING REGISTER
R5 W	PARITY OR B8 (W) W	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	TAPE TRANSMIT HOLDING REGISTER
R6				PA4 R/W	PA3 R/W	PA2 R/W	PA1 R/W	PA0 R/W	PORT A
R7					PB3 R/W	PB2 R/W	PB1 R/W	PB0 R/W	PORT B
R8	UK/$\overline{\text{EUR}}$ R/W	60s TIMER R/W	DIAL GO R/W	1.5s TIMER R/W	DI 3 W	DI 2 W	DI 1 W	DI 0 W	DIAL CONTROL AND TIMING REGISTER
R10 A R10 B	B8 R – WL3 R	B7 R – WL2 R	B6 R – WL1 R	B5 R – WL0 R	B4 R – B12 R	B3 R – B11 R	B2 R – B10 R	B1 R – B9 R	IBUS A REGISTERS

APPENDIX

Register map (continued)

	D7	D6	D5	D4	D3	D2	D1	D0	
R11 A	B8 R/W	B7 R/W	B6 R/W	B5 R/W	B4 R/W	B3 R/W	B2 R/W	B1 R/W	IBUS B REGISTERS
R11 B	– WL3 R/W	– WL2 R/W	– WL1 R/W	– WL0 R/W	– B12 R/W	– B11 R/W	– B10 R/W	– B9 R/W	

NOTE R9 is unused.

For details of bit movement in R10 and R11 see discussion of IBUS operation. A mnemonic list for use with this register map and Fig.1b is given on the next page.

MNEMONIC LIST

ALE	address latch enable from microprocessor
CLCK IN/$\overline{\text{OUT}}$	input/output control for 62.5 kHz clock pin
CPNTR	pointer signal for two byte registers
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	three line/two line control for IBUS A receiver
DON	dial off normal relay control for dialling
IMP	impulsing relay control for dialling
IARXRDY	IBUS A receiver ready — data available
IBRXRDY	IBUS B receiver ready — data available
IBTXRDY	IBUS B transmitter ready — previous transmission complete
LDBEN	line demodulator output buffer enable
LDCD	line data carrier detected
LFERR	line receiver framing error — received stop bit not HIGH
LIDCD	line instantaneous data carrier detect
$\overline{\text{LPEN}}$	line parity enable command
LPERR	line receiver parity error flag
LPO/$\overline{\text{E}}$	line parity odd/even command
LRXEN	line receiver enable
LRXRDY	line receiver ready — data available
LTXEN	line transmitter and modulator enable
LTXRDY	line transmitter ready — transmit holding register empty
$\overline{\text{SR}}$n	select register 'n'
TDCD	tape data carrier detected
TFERR	tape receiver framing error — received stop bit not HIGH
$\overline{\text{TPEN}}$	tape parity enable command
TPERR	tape receiver parity error flag
TPO/$\overline{\text{E}}$	tape parity odd/even command
TRXEN	tape receiver enable
TRXRDY	tape receiver ready — data available
TTXEN	tape transmitter enable
TTXRDY	tape transmitter ready — transmit holding register empty
UK/$\overline{\text{EUR}}$	impulsing ratio control for UK and European standards
$\overline{75}$/1200	baud rate selection command for line modulator and line transmit shift register

Teletext Video Processor SAA5230

The SAA5230 is bipolar integrated circuit intended as a successor to SAA5030. It extracts teletext data from the video signal, regenerates teletext clock and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (Computer Controlled Teletext), EUROM or other compatible devices.

Its main functions are:

- Adaptive data slicer
- Data clock regenerator
- Sync separator, line phase detector and 6 MHz VCO forming display phase locked loop (PLL)

QUICK REFERENCE DATA

Supply voltage	V_{CC}	typ.	12	V
Supply current	I_{CC}	typ.	70	mA
Video input amplitude (pin 2 LOW)	$V_{27(p-p)}$	typ.	1	V
Video input amplitude (pin 2 HIGH)	$V_{27(p-p)}$	typ.	2,5	V
Storage temperature	T_{stg}	−55 to	+150	°C
Operating ambient temperature	T_{amb}	−25 to	+70	°C

5

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

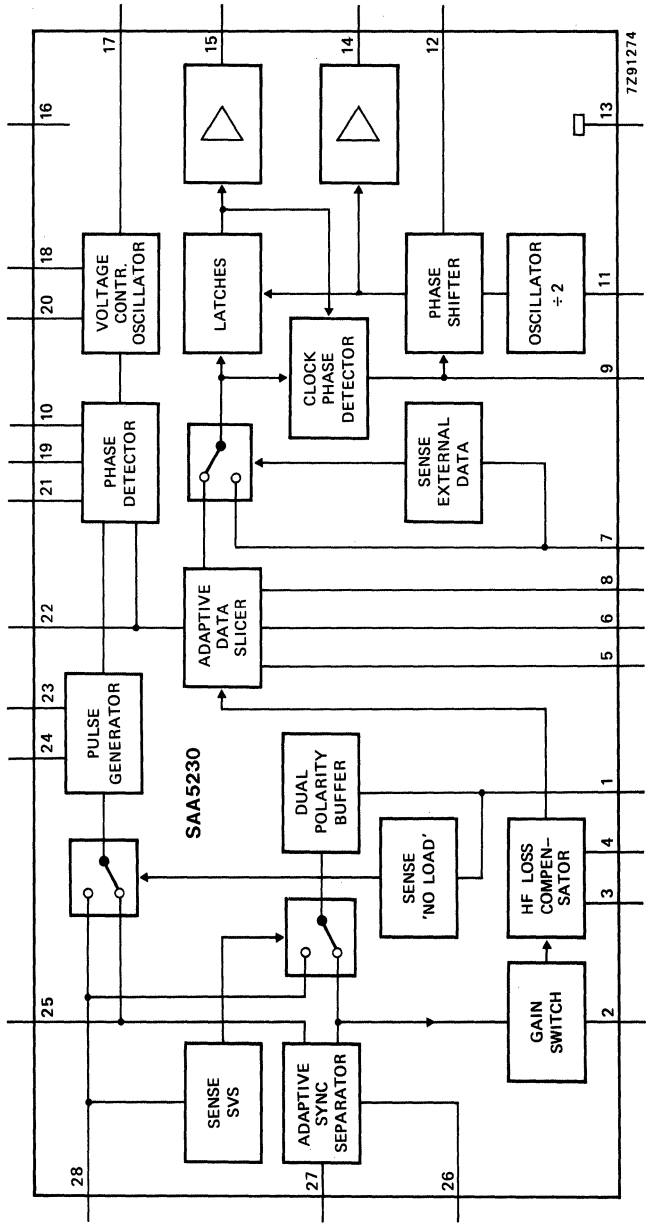


Fig. 1 Block diagram.

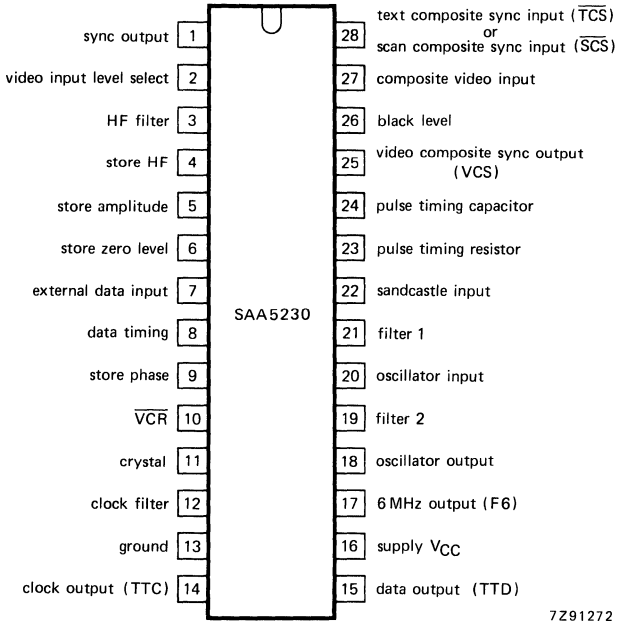


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 16)	V_{CC}	max.	13,2 V
Storage temperature range	T_{stg}	−55 to	+150 °C
Operating ambient temperature	T_{amb}	−25 to	+70 °C

5

CHARACTERISTICS

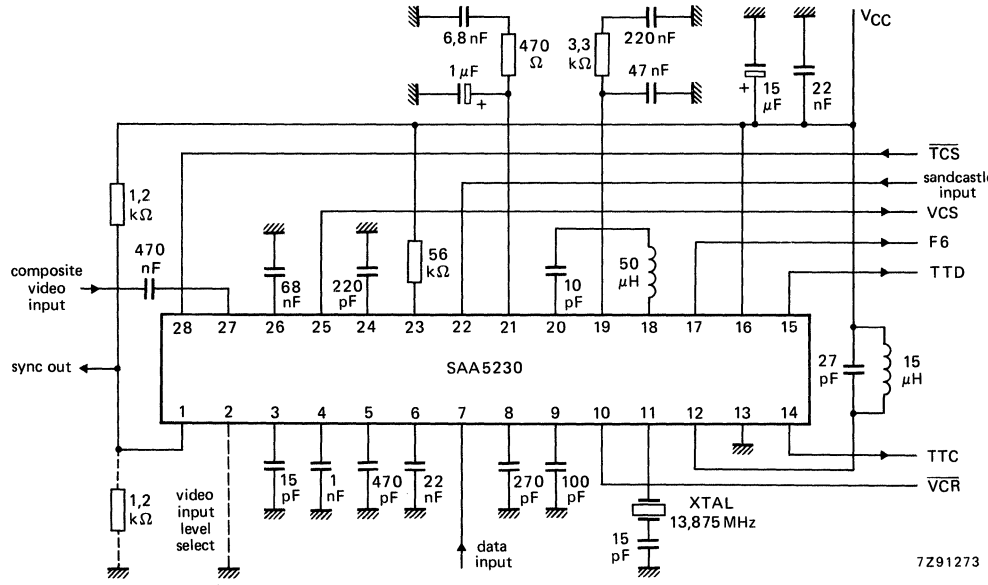
V_{CC} = 12 V; T_{amb} = 25 °C with external components as shown in Fig. 3 unless otherwise stated.

		min.	typ.	max.	unit
Supply voltage	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	–	70	–	mA
Video input and sync separator					
Video input amplitude (sync to white)					
pin 2 LOW	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
pin 2 HIGH	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\lvert Z_s \rvert$	–	–	250	Ω
Sync amplitude	$V_{27\text{-}13(p\text{-}p)}$	–	–	1	V
Video level select input					
Input voltage LOW	$V_{2\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current LOW	I_2	0	–	−150	μA
Input current HIGH	I_2	0	–	1	mA
Text composite sync input ($\overline{TCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{28\text{-}13}$	2,0	–	7,0	V
Scan composite sync input ($\overline{SCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	1,5	V
Input voltage HIGH	$V_{28\text{-}13}$	3,5	–	7,0	V
Select video sync from pin 1					
Input current					
V_i = 0 to 7 V	I_{28}	−40	−70	−100	μA
V_i = 10 V to V_{CC}	I_{28}	−5	–	+5	μA
Video composite sync output (VCS)					
Output voltage LOW	$V_{25\text{-}13}$	0	–	0,4	V
Output voltage HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
Output d.c. current LOW	I_{25}	–	–	0,5	mA
Output d.c. current HIGH	I_{25}	–	–	−1,5	mA
Sync separator delay time	t_d	–	0,5	–	μs

		min.	typ.	max.	unit
Dual polarity buffer output					
$\overline{TCS}$ sync amplitude	$V_{1(p-p)}$	–	0,45	–	V
Video sync amplitude	$V_{1(p-p)}$	–	–	1	V
Output current	I_1	–3	–	+3	mA
D.C. output voltage					
R_L to ground (0 V)	V_1	–	1,4	–	V
R_L to V_{CC} (12 V)	V_1	–	10,1	–	V
Sandcastle input					
Phase lock pulse					
PL on (LOW)	V_{22}	0	–	3	V
PL off (HIGH)	V_{22}	3,9	–	5,5	V
Blanking pulse					
CBB on (LOW)	V_{22}	0	–	0,5	V
CBB off (HIGH)	V_{22}	1,0	–	5,5	V
Input current	I_{22}	–10	–	+10	μA
PLL					
Line sync timing					
pulse width (using composite video)	t_p	–	2	–	μs
pulse width (using scan composite sync)	t_p	–	3	–	μs
Pulse duration					
period PL must be LOW to make VCO free-run	t_p	100	–	–	μs
6 MHz - VCO (F6)					
A.C. output voltage	$V_{17(p-p)}$	1	2	3	V
D.C. output voltage	V_{17-13}	4	–	8	V
Rise and fall time	t_r, t_f	20	–	40	ns
Load capacitance	C_{17-13}	–	–	40	pF
$\overline{VCR}$					
VCR-mode on (LOW)	V_{10-13}	0	–	0,8	V
VCR-mode off (HIGH)	V_{10-13}	2,0	–	V_{CC}	V
Input current	I_{10}	–10	–	+10	μA
Data slicer					
Data amplitude of video input					
pin 2 LOW	V_{27}	0,30	0,46	0,70	V
pin 2 HIGH	V_{27}	0,75	1,15	1,75	V

5

		min.	max.	typ.	unit
Teletext clock output					
A.C. output voltage	$V_{14(p-p)}$	2	3	4	V
D.C. output voltage	V_{14-13}	4	–	8	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns
Delay of falling edge relative to other edges of TTD	t_d	–20	0	+20	ns
Teletext data output					
A.C. output voltage	$V_{15(p-p)}$	2,0	3,0	4,0	V
D.C. output voltage	V_{15-13}	4	–	8	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	$t_r = t_f$	20	30	45	ns



X = 13,875 MHz

Fig. 3 Test and application circuit.

APPLICATION DATA

The function is quoted against the corresponding pin number

1. **Sync output to TV**
   Output with dual polarity buffer, a load resistor to 0 V or + 12 V selects positive-going or negative-going syncs.
2. **Video input level select**
   LOW level selects 1 volt input video level. With no connection level floats HIGH, selecting 2,5 volt level.
3. **H.F. filter**
   A capacitor connected to this pin filters the video signal for the h.f.-loss compensator.
4. **Store h.f.**
   The h.f. amplitude is stored by a capacitor connected to this pin.
5. **Store amplitude**
   Store capacitor stores the amplitude for the adaptive data slicer.
6. **Store zero level**
   Store capacitor stores the zero level for the adaptive data slicer.
7. **External data input**
   Current input for sliced teletext data from external device. Active HIGH level (current), low impedance input.
8. **Data timing**
   A capacitor is connected to this pin for timing of the adaptive data slicer.
9. **Store phase**
   A capacitor connected to this pin stores the output signal from the clock phase detector.
10. **Video tape recorder mode ($\overline{VCR}$)**
    Signal input to command PLL into (short time constant mode), to enable text to synchronize to a video tape recorder. Active is LOW. If not connected, the level is HIGH.
11. **Crystal**
    A 13,875 MHz crystal (2x data rate) in series with a capacitor is connected to this pin.
12. **Clock filter**
    A filter for the clock signal is connected to this pin (6,938 MHz).
13. **Ground (0 V)**
14. **Teletext clock output**
    TTC for CCT (Computer Controlled Teletext).
15. **Teletext data output**
    TTD for CCT.
16. **Supply voltage V_{CC}**
    Typical value + 12 V.
17. **F6**
    6 MHz output clock for timing and sandcastle generation in CCT.
18. **Oscillator output (6 MHz)**
    A series resonant circuit is connected between this pin and pin 20 to control the nominal frequency of the VCO.

5

APPLICATION DATA (continued)

19. **Filter 2**
A filter for the line phase detector is connected to this pin. The filter has a short time constant and is used in video recorder mode and while the loop is locking up.

20. **Oscillator input (6 MHz)**
See pin 18.

21. **Filter 1**
A long time constant filter for the line phase detector is connected to this pin.

22. **Sandcastle input**
This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. Signal timing see Fig. 4.

23. **Pulse timing resistor**
A connected resistor defines the current for the pulse generator.

24. **Pulse timing capacitor**
A connected capacitor is used for timing of the pulse generator.

25. **VCS output**
Video composite sync output signal for CCT.

26. **Black level**
A capacitor connected to this pin stores the black level for the adaptive sync separator.

27. **Composite video input**
The composite video is fed to this input via a clamp capacitor.

28. **Sync input**
Input for text composite sync ($\overline{TCS}$) from CCT or $\overline{SCS}$ from external sync circuit. $\overline{SCS}$ is expected if there is no load resistor at pin 1.

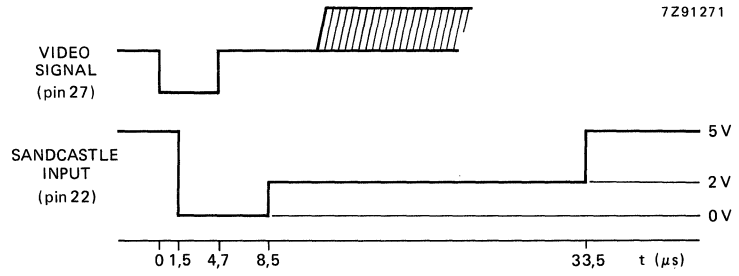


Fig. 4 Sandcastle waveform and timing.

For additional information
consult the Applications Section.

European Computer Controlled Teletext Circuit (EURO CCT) SAA5240

GENERAL DESCRIPTION

The SAA5240 is a MOS N-channel integrated circuit which performs all the digital logic functions of a 625-line World System Teletext decoder. It operates in conjunction with the teletext video processor SAA5230, standard static RAM's and is controlled via the 2-wire I^2C bus. The device can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 6 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language selection of up to three different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Ghost row reception option (extension packets)
- Standard I^2C bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets: SAA5240A; English, German, Swedish SAA5240B; Italian , German, French

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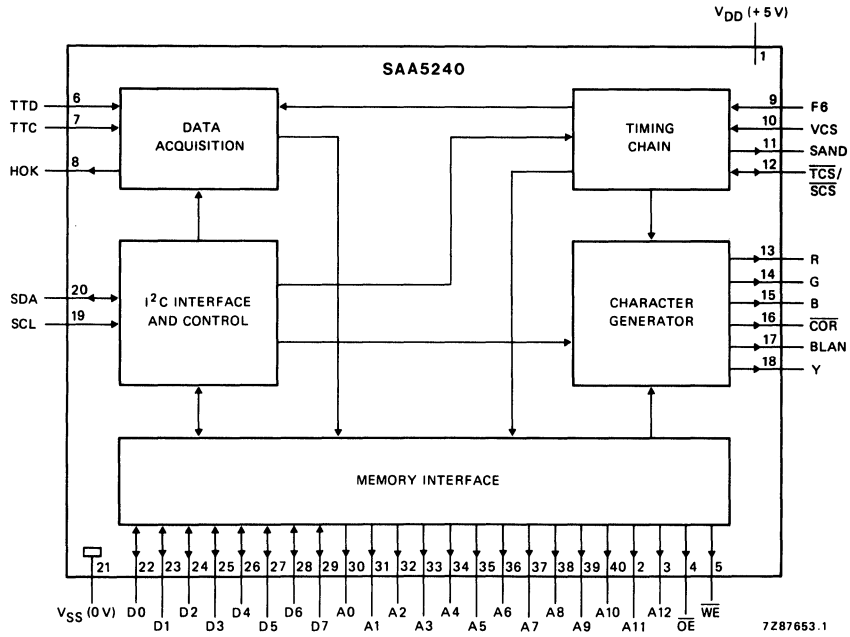


Fig. 1 Block diagram.

PACKAGE OUTLINES

40-lead DIL; plastic (SOT-129).

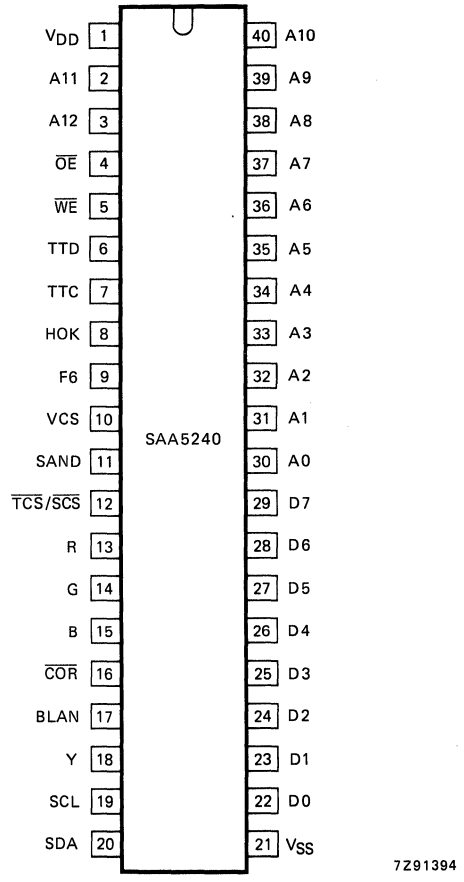


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	**Power supply**: + 5 V power supply pin.
2, 3, 40	A11, A12, A10	**Chapter Address**: three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
4	$\overline{OE}$	**Output Enable**: active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.
5	$\overline{WE}$	**Write Enable**: active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data**: input from the SAA5230 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct d.c. level following the external a.c. coupling.

7	TTC	**Teletext Clock**: 6,9375 MHz clock input from the SAA5230. It is internally a.c. coupled to an active clamp input buffer.
8	HOK	**Hamming O.K.**: an active high output signal indicating reception of a valid teletext data line with no Hamming errors in the magazine or row bytes. It is reset at line rate.
9	F6	**Character display clock**: 6 MHz clock input from the SAA5230. It is internally a.c. coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync**: input from the SAA5230 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle**: 3-level sandcastle output to the SAA5230 containing the phase locking and colour burst blanking information.
12	$\overline{TCS}/\overline{SCS}$	**Text Composite Sync/Scan Composite Sync**: as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig. 6) which is fed to the SAA5230 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Blue, Green**: these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{COR}$	**Contrast Reduction**: open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking**: open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground**: open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock**: input signal which is the I^2C bus clock from the microcontroller.
20	SDA	**Serial Data**: is the I^2C bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground**: 0 volts.
22-29	D0-D7	**8 RAM data lines**: 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address**: 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 1)	V_{DD}	−0,3 to +7,5 V
Input voltage range		
VCS, SDA, SCL, D0-D7	V_I	−0,3 to +7,5 V
TTC, TTD, F6, $\overline{TCS}/\overline{SCS}$	V_I	−0,3 to +13,2 V
Output voltage range		
SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, HOK	V_O	−0,3 to +7,5 V
R, G, B, BLAN, $\overline{COR}$, Y, $\overline{TCS}/\overline{SCS}$	V_O	−0,3 to +13,2 V
Storage temperature range	T_{stg}	−20 to +125 °C
Operating ambient temperature range	T_{amb}	−20 to +70 °C

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 1)	I_{DD}	–	160	–	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2,0	–	7,0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
D.C. input voltage range	V_I	–0,3	–	+ 10,0	V
A.C. input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	–	7,0	V
Input peaks relative to 50% duty cycle	± V_P	0,2	–	3,5	V
TTC clock frequency	f_{TTC}	–	6,9375	–	MHz
F6 clock frequency	f_{F6}	–	6,0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5,5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

5

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5,5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,5	–	10,0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 0 to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
at I_{OH} = 0,1 mA	V_{OH}	2,4	–	6,0	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1,5	V
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at V_I = 5,5 V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	0	–	0,5	V
Output fall time between 3,0 V and 1,0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5,5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
HOK (note 9)					
Output voltage LOW at I_{OL} = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Output rise and fall times between 0,6 V and 2,2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0,2 mA	V_{OL}	0	–	0,2	V
Output voltage INTERMEDIATE at I_{OL} = ± 30 μA	V_{OI}	1,3	–	2,7	V

5

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −30 μA	V_{OH}	4,2	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0,4 V and 1,1 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 2,9 V and 4,0 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 4,0 V and 0,4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{\text{COR}}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0,4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1,0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6,0	V
Output fall time with a load resistor of 1,2 kΩ to 6 V and measured between 5,5 V and 1,5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1,2 kΩ to 6 V and measured on the falling edges at 3,5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I²C bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low to high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

5

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig. 3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2,0 V; data stable 0 $\leqslant$ 0,8 V (see Fig. 4).
5. The TTC and F6 inputs have internal clamping diodes and are a.c. coupled (see Fig. 3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^2C bus timing see Fig. 8.
8. For details of RAM timing see Fig. 9.
9. For details of synchronization and HOK timing see Fig. 5.
10. For details of display output timing see Fig. 7.
11. The I^2C bus timings are referred to V_{IH} = 3 V and V_{IL} = 1,5 V. For waveforms see Fig. 8.
12. The memory interface timings are referred to V_{IL} = 1,5 V. For waveforms see Fig. 9.

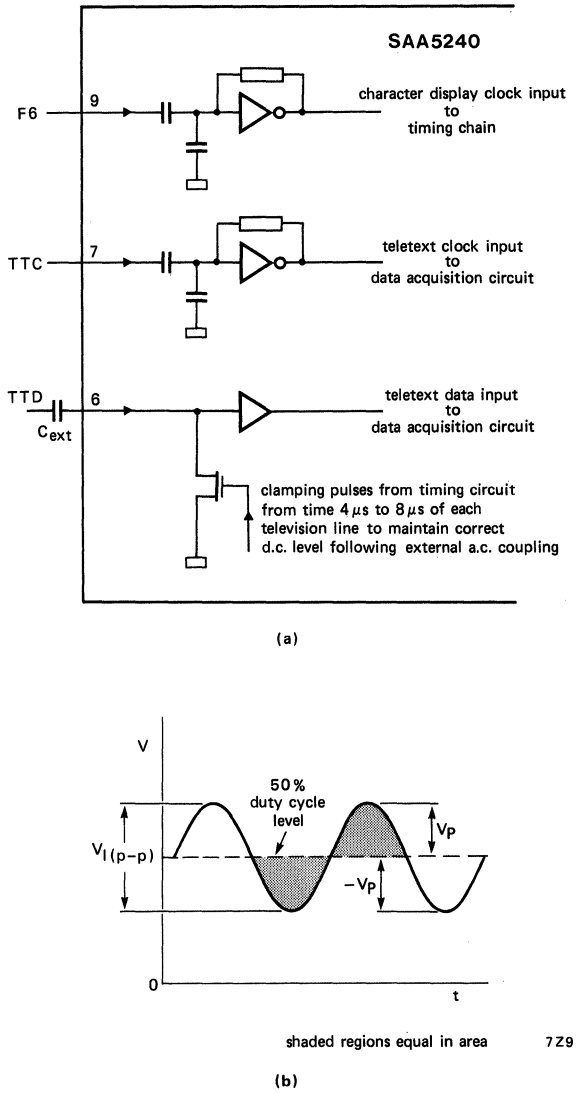
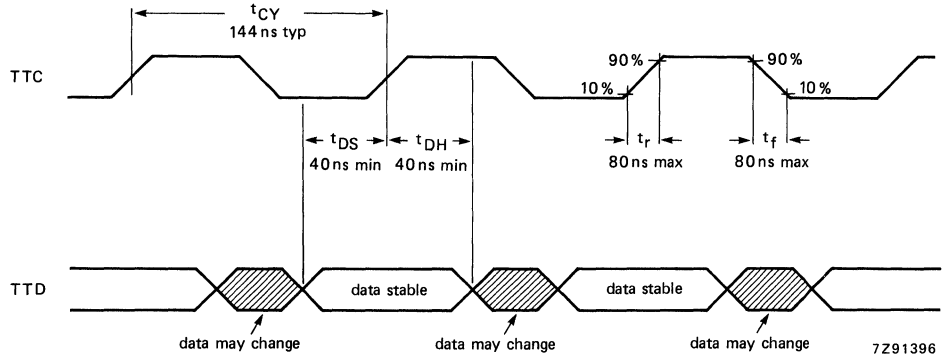


Fig. 3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is $\geqslant$ 2,0 V; 0 is $\leqslant$ 0,8 V.

Fig. 4 Teletext data input timing.

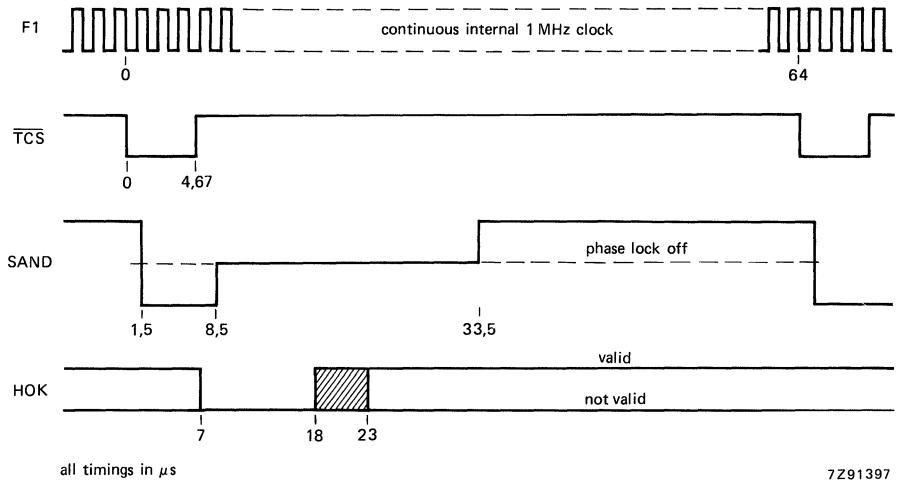
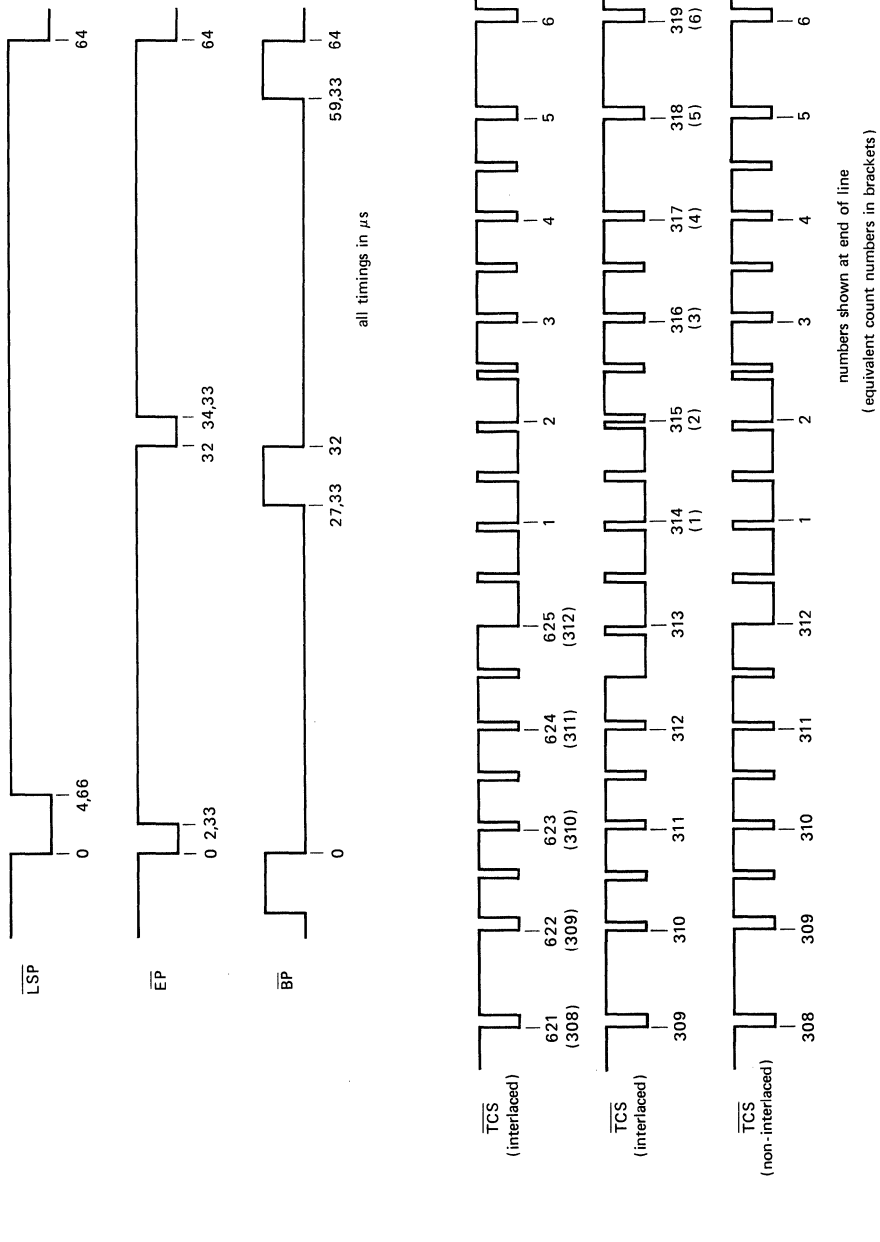


Fig. 5 Synchronization and HOK timing.



Line sync pulses ($\overline{LSP}$), equalizing pulses ($\overline{EP}$) and broad pulses ($\overline{BP}$) are combined to provide the text composite sync waveform ($\overline{TCS}$) as shown.

All timings measured from falling edge of $\overline{LSP}$ with a tolerance of ± 100 ns.

Fig. 6 Composite sync waveforms.

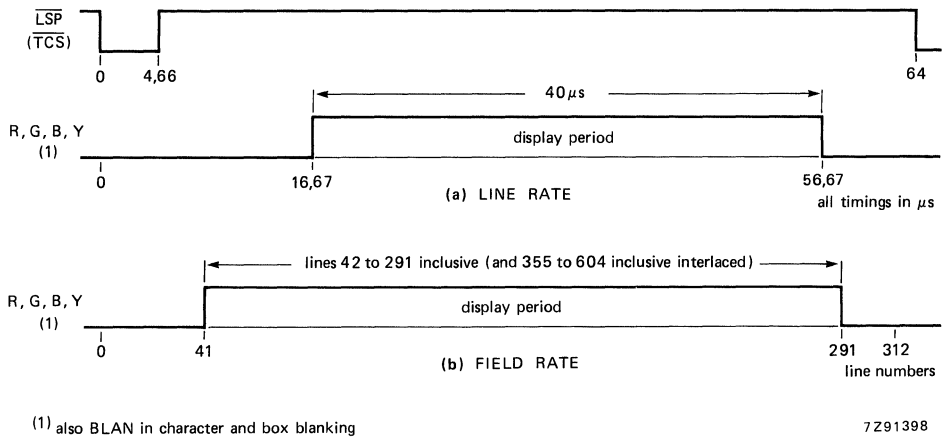


Fig. 7 Display output timing (a) line rate (b) field rate.

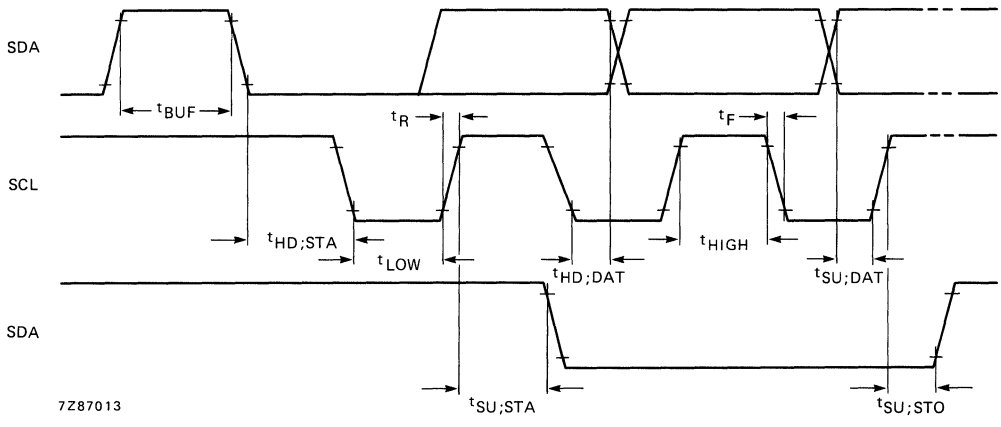


Fig. 8 I^2C bus timing.

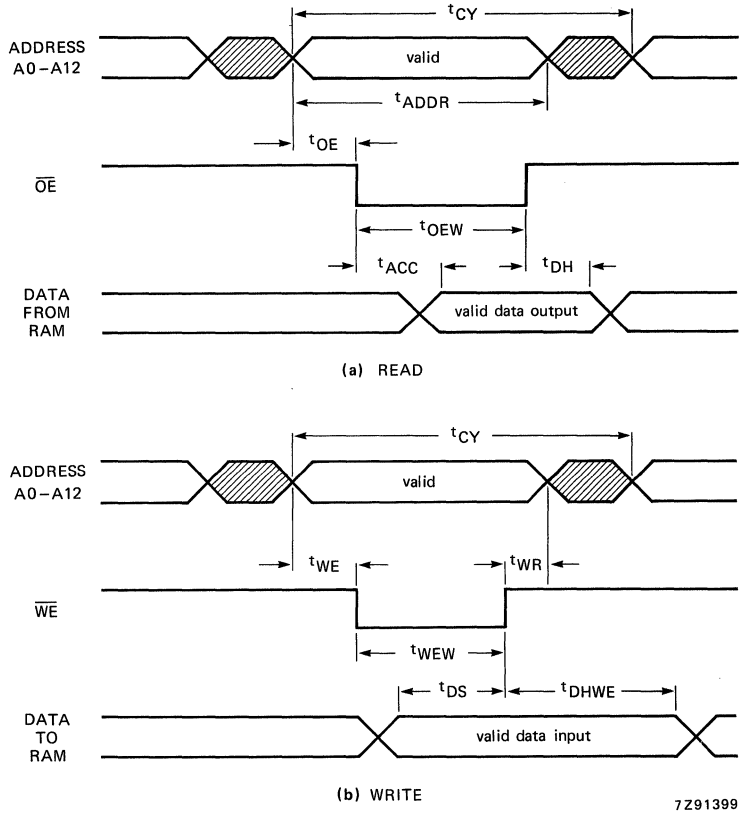


Fig. 9 Memory interface timing (a) read (b) write.

APPLICATION INFORMATION

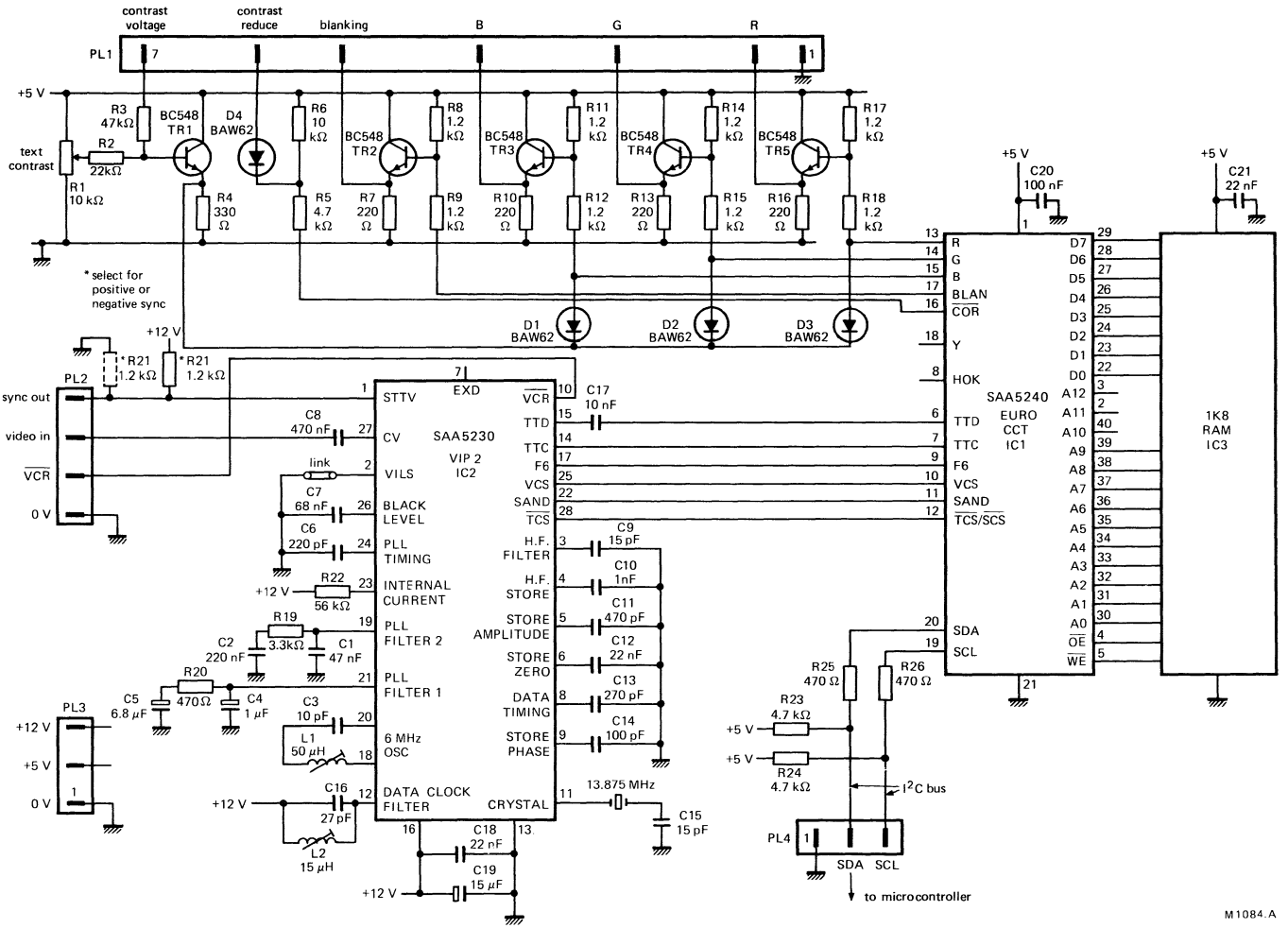


Fig. 10 EURO CCT based single-page decoder circuit diagram.

APPLICATION INFORMATION (continued)

EURO CCT page memory organization

The organization of a page memory is shown in Fig. 11. The EURO CCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF CCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

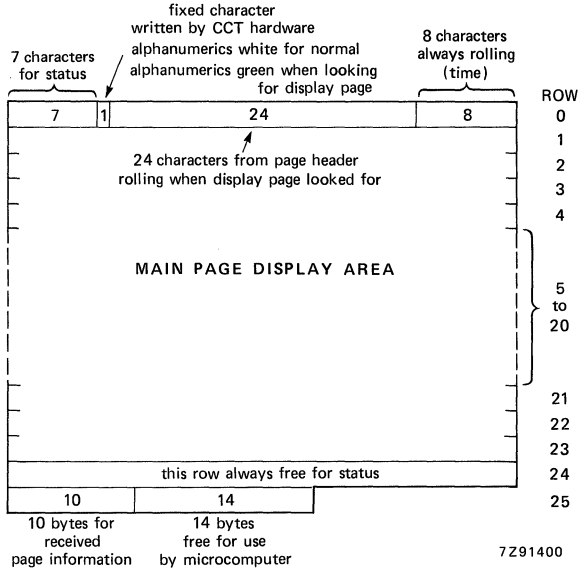


Fig. 11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	FOUND	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
PBLF	page being looked for		HT	hours tens	
FOUND	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by EURO CCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

EURO CCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 EURO CCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	GHOST ROW ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
–	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
–	–	–	–	–	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
–	–	–	–	CLEAR MEM.	A2	A1	A0	R8	Active chapter
–	–	–	R4	R3	R2	R1	R0	R9	Active row
–	–	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

– bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^2C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

APPLICATION INFORMATION (continued)

Table 2 (continued)

Where:

R1 Mode	
T0, T1	interlace/non interlace 312/313 line control
TCS ON	text composite sync or direct sync select
$\overline{\text{DEW}}$/FULL FIELD	field-flyback or full channel mode
7 + P/8 BIT	7 bits with parity checking or 8-bit mode
TA, TB	test bits; 0 for normal operation
R2 Page request address	
START COLUMN	start column for page request data
ACQ CCT	selects one of four acquisition circuits
BANK SELECT	selects bank of four pages being addressed for acquisition
R3 Page request data	see Table 3
R4 Display chapter	determines which of the 8 pages is displayed
R5, R6 Display control	for normal and newsflash/subtitle
PON	picture on
TEXT	text on
COR	contrast reduction on
BKGND	background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode	
BOX ON 0 (1-23, 24)	boxing function allowed on row 0 (row 1-23, 24)
STATUS ROW $\overline{\text{BTM}}$/TOP	row 25 displayed above or below the main text
R8 to R11	active chapter, row, column and data information written to or read from page memory via the I^2C bus.

Table 3 Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

Abbreviations are as for Table 1 except for D0 CARE bits.
When the D0 CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the D0 CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).
Columns auto-increment on successive I^2C transmission bytes.

APPLICATION INFORMATION (continued)

CHARACTER SETS

The UK teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14 as shown in Table 4. The basic 96 character sets differ only in the 13 national option characters as indicated in Tables 8 and 9 with reference to their table position in the basic character matrix shown in Table 7. EURO CCT automatically decodes control bits C12 to C14. Other combinations of C12 to C14 are defaulted to SAA5240A (English); SAA5240B (German). With 8-bit decoding the character matrices are shown in Tables 5 and 6.

Table 4 Selection of national character sets

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH
C12	0	0	0	0	1
C13	0	0	1	1	0
C14	0	1	0	1	0

Where:

PHCB page header control bits.

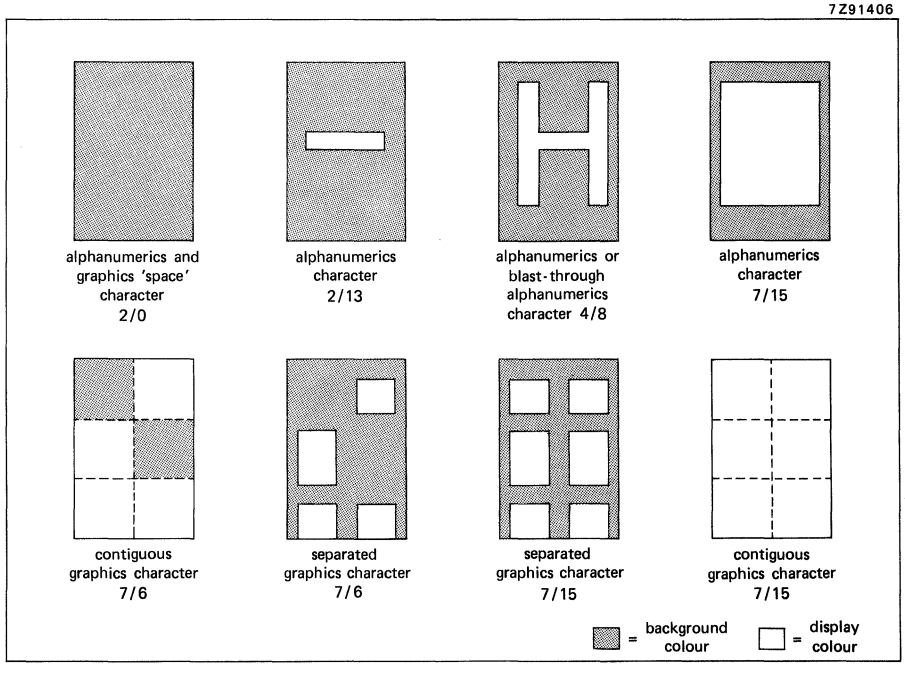


Fig. 12 Character format.

Table 5 Character data input decoding (SAA5240A)

BITS b_8	0	0	0 or 1		0 or 1		0 or 1	0 or 1	0 or 1		0 or 1		1	1
b_7	0	0	1		1		1	0	1		1		0	0
b_6	0	0	1		1		0	0	0		1		0	0
b_5	0	1	0		1		0	1	0		1		0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9
0 0 0 0	0	alpha-numerics black	graphics black											
0 0 0 1	1	alpha-numerics red	graphics red											
0 0 1 0	2	alpha-numerics green	graphics green											
0 0 1 1	3	alpha-numerics yellow	graphics yellow											
0 1 0 0	4	alpha-numerics blue	graphics blue											
0 1 0 1	5	alpha-numerics magenta	graphics magenta											
0 1 1 0	6	alpha-numerics cyan	graphics cyan											
0 1 1 1	7	alpha-numerics white **	graphics white											
1 0 0 0	8	flash	conceal display											
1 0 0 1	9	steady **	contiguous graphics **											
1 0 1 0	10	end box **	separated graphics											
1 0 1 1	11	start box	ESC *											
1 1 0 0	12	normal height **	black background **											
1 1 0 1	13	double height	new background											
1 1 1 0	14	SO *	hold graphics											
1 1 1 1	15	SI *	release graphics **											

7Z91402

* These control characters are reserved for compatibility with other data codes.

** These control characters are presumed before each row begins.

APPLICATION INFORMATION (continued)

Table 6 Character data input decoding (SAA5240B)

BITS b_8	0	0	0 or 1		0 or 1		0 or 1	0 or 1	0 or 1		0 or 1		1	1
b_7	0	0	0		0		1	1	1		1		0	0
b_6	0	0	1		1		0	0	0		1		0	0
b_5	0	1	0		1		0	1	0		1		0	1
b_4 b_3 b_2 b_1 ↓ ↓ ↓ ↓	column 0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9
0 0 0 0	0	alpha–numerics black	graphics black											
0 0 0 1	1	alpha–numerics red	graphics red											
0 0 1 0	2	alpha–numerics green	graphics green											
0 0 1 1	3	alpha–numerics yellow	graphics yellow											
0 1 0 0	4	alpha–numerics blue	graphics blue											
0 1 0 1	5	alpha–numerics magenta	graphics magenta											
0 1 1 0	6	alpha–numerics cyan	graphics cyan											
0 1 1 1	7	alpha–numerics white **	graphics white											
1 0 0 0	8	flash	conceal display											
1 0 0 1	9	steady **	contiguous graphics **											
1 0 1 0	10	end box **	separated graphics											
1 0 1 1	11	start box	ESC *											
1 1 0 0	12	normal height **	black background **											
1 1 0 1	13	double height	new background											
1 1 1 0	14	SO *	hold graphics											
1 1 1 1	15	SI *	release graphics **											

7Z91484

* These control characters are reserved for compatibity with other data codes.

** These control characters are presumed before each row begins.

Notes to Tables 5 and 6

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. The SAA5240A national option characters are shown in Table 8.
6. The SAA5240B national option characters are shown in Table 9.
7. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters to combine with character 8/5.
8. With bit 8 = 0 national option characters will be decoded according to the setting of control bits C12 to C14 (see Table 4).

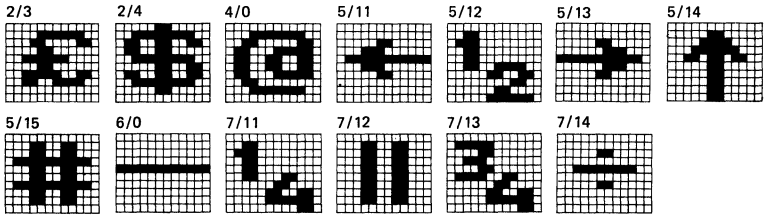
APPLICATION INFORMATION (continued)

Table 7 SAA5240 basic character matrix

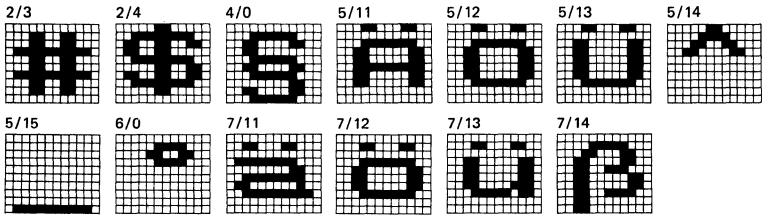
Where: NC national option character position.

Table 8 SAA5240A character set (national option characters)

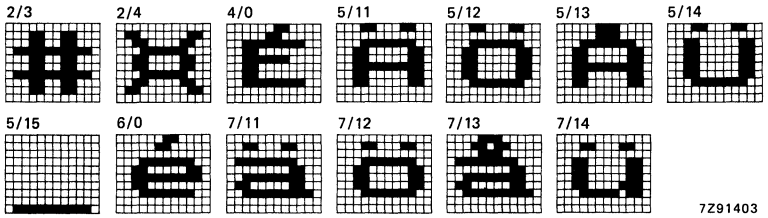
ENGLISH



GERMAN



SWEDISH



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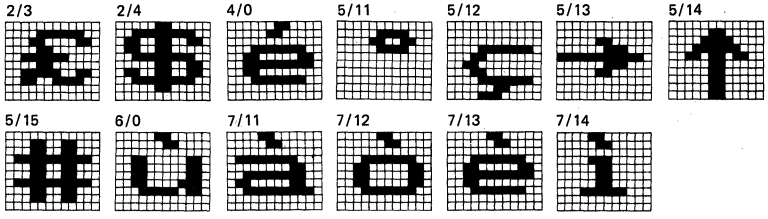
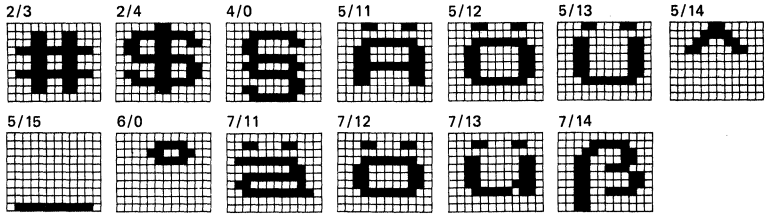
APPLICATION INFORMATION (continued)

Table 9 SAA5240B character set (national option characters)

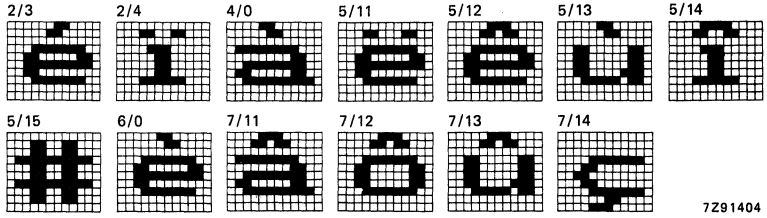
ITALIAN



GERMAN



FRENCH



7Z91404

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

For additional information
consult the Applications Section.

Single-Chip Color CRT Controller (EUROM) SAA5350

GENERAL DESCRIPTION

The SAA5350 EUROM is a single-chip VLSI NMOS crt controller capable of handling all display functions required by the CEPT videotex terminal, model A4. Only minimal hardware is required to produce a videotex terminal using EUROM – the simplest configuration needs just a microcontroller and 4 Kbytes of display memory.

Features

- Minimal additional hardware required
- Screen formats of 40/80 character by 1-to-25 row display
- 512 alphanumeric or graphical characters on-chip or extendable off-chip
- Serial attribute storage (STACK) and parallel attribute storage
- Dynamically redefinable character (DRCS) capability over full field
- Interfaces with 8/16-bit microprocessors with optional direct memory access
- On-chip scroll map minimizes data to be transferred when scrolling
- On-chip colour map RAM followed by three non-linear digital-to-analogue converters which compensate for crt non-linearity
- Memory interface capable of supporting multi-page terminals. EUROM can access up to 128 Kbytes of display memory
- Programmable cursor
- Programmable local status row
- Three synchronization modes:

stand-alone	built-in oscillator operating with an external 6 MHz crystal
simple slave	directly synchronized from the source of text composite sync
phase-locked slave	indirect synchronization allows picture-in-text displays (e.g. VCR/VLP video with text overlay)

- On-chip timing composite sync output
- Zoom feature which allows the height of any group of rows to be increased to enhance legibility

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PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

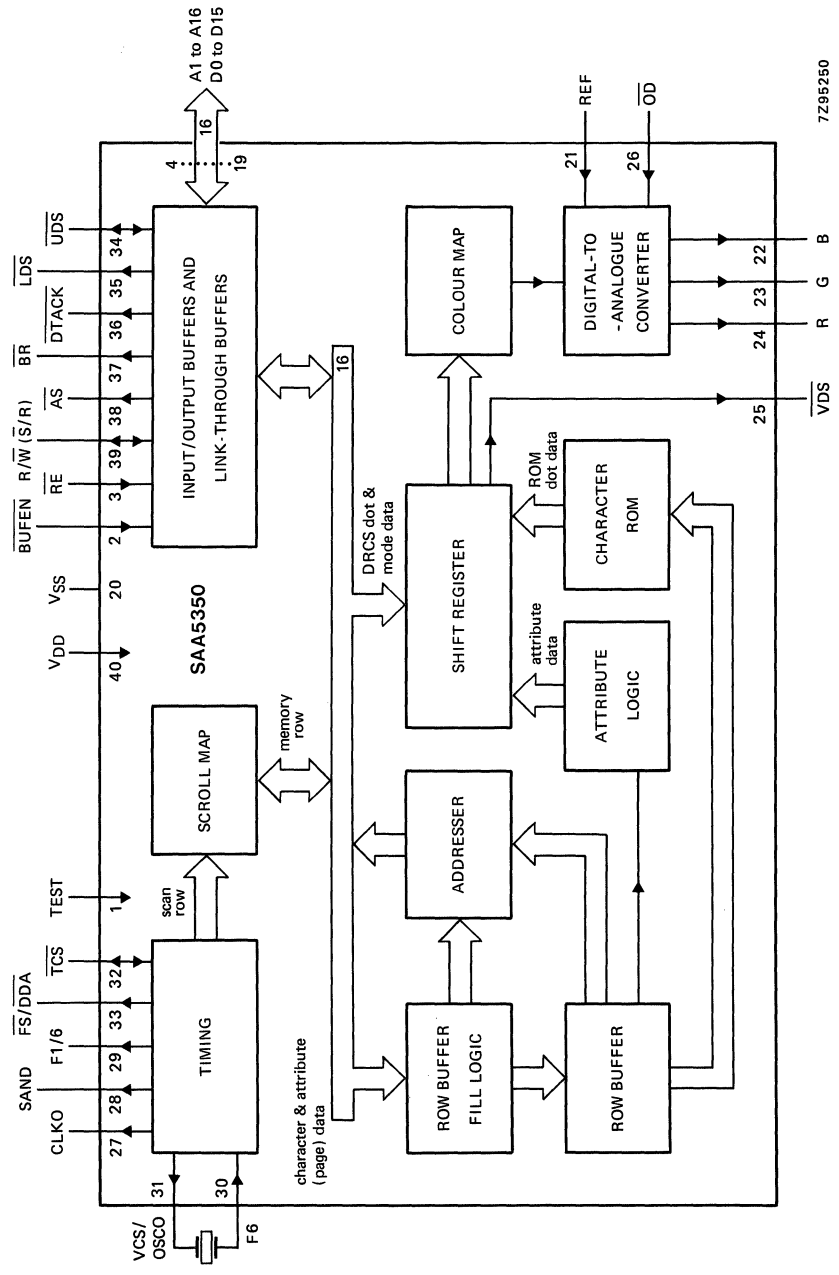

Fig. 1 Block diagram.

PINNING

1	TEST	Input to be connected to V_{SS}.
2	$\overline{BUFEN}$	Buffer enable input to the 8-bit link-through buffer.
3	$\overline{RE}$	Register enable input. This enables A1 to A6 and $\overline{UDS}$ as inputs, and D8 to D15 as input/outputs.
4 to 19	A16 to A1/ D15 to D0	Multiplexed address and data bus input/outputs. These pins also function as the 8-bit link-through buffer.
20	V_{SS}	Ground (0 V).
21	REF	Analogue reference input.
22	B	Analogue outputs (signals are gamma-corrected).
23	G	
24	R	
25	$\overline{VDS}$	Switching output for dot, screen (row), box and window video data; for use when video signal is present (e.g. from tv, VLP, alpha + photographic layer). This output is LOW for tv display and HIGH for text and will interface directly with a number of colour decoder ICs (e.g. TDA3560, TDA3505).
26	$\overline{OD}$	Output disable causing R, G, B and $\overline{VDS}$ outputs to go to high-impedance state. Can be used at dot-rate.
27	CLKO	12 MHz clock output for hard-copy dot synchronization (referenced to output dots).
28	SAND	Sandcastle feedback output for SAA5230 teletext video processor or other circuit. Used when the display must be locked to the video source (e.g. VLP). The phase-lock part of the sandcastle waveform can be disabled to allow free-running of the SAA5230 phase-locked loop.
29	F1/6	1 MHz or 6 MHz output.
30	F6	6 MHz clock input (e.g. from SAA5230). Internal a.c. coupling is provided.
31	VCS/OSCO	Video composite sync input (e.g. from SAA5230) for phase reference of vertical display timing when locking to a video source (e.g. VLP) or, in stand-alone sync mode, output from internal oscillator circuit (fixed frequency).
32	$\overline{TCS}$	Text composite sync input/output depending on master/slave status.
33	$\overline{FS}$/$\overline{DDA}$	Field sync pulse output or defined-display-area flag output (both referenced to output dots).
34	$\overline{UDS}$	Upper data strobe input/output.
35	$\overline{LDS}$	Lower data strobe output.
36	DTACK	Data transfer acknowledge (open drain output).
37	$\overline{BR}$	Bus request to microprocessor (open drain output).
38	$\overline{AS}$	Address strobe output to external address latches.
39	R/$\overline{W}$ ($\overline{S}$/R)	Read/write input/output. Also serves as send/receive for the link-through buffer.
40	V_{DD}	Positive supply voltage (+ 5 V).

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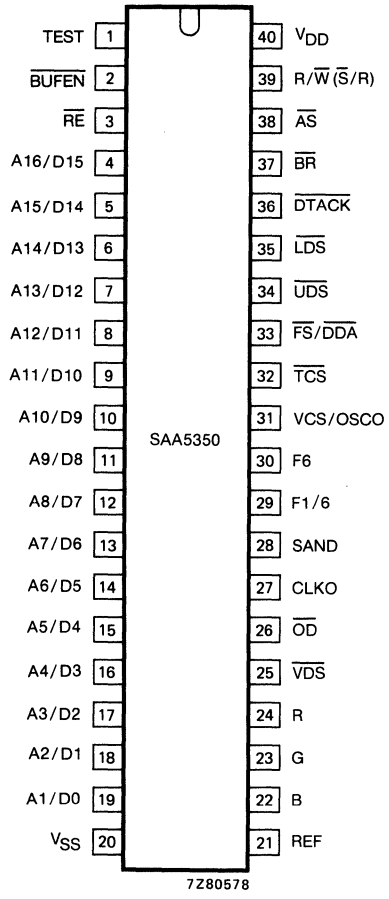

Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}	−0.3 to + 7.5 V
Maximum input voltage (except F6, $\overline{TCS}$, REF)	V_{Imax}	−0.3 to + 7.5 V
Maximum input voltage (F6, $\overline{TCS}$)	V_{Imax}	−0.3 to + 10.0 V
Maximum input voltage (REF)	V_{REF}	−0.3 to + 3.0 V
Maximum output voltage	V_{Omax}	−0.3 to + 7.5 V
Maximum output current	I_{Omax}	10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

Outputs other than CLKO, OSCO, R, G, B, and $\overline{VDS}$ are short-circuit protected.

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 40)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 40)	I_{DD}	–	–	350	mA
INPUTS					
F6 (note 1)					
Slave modes (Fig. 3)					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1.0	–	7.0	V
Input peaks relative to 50% duty factor	$\pm V_P$	0.2	–	3.5	V
Input leakage current at V_I = 0 to 10 V; T_{amb} = 25 °C	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	12	pF
Stand-alone mode (Fig. 4)					
Series capacitance of crystal	C_1	–	28	–	fF
Parallel capacitance of crystal	C_0	–	7.1	–	pF
Resonance resistance of crystal	R_r	–	–	60	Ω
Gain of circuit	G	–	–	tbf	V/V
$\overline{\text{BUFEN}}$, $\overline{\text{RE}}$, $\overline{\text{OD}}$					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	6.5	V
Input current at V_I = 0 to V_{DD}+0.3 V; T_{amb} = 25 °C	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
REF (Fig. 5)					
Input voltage	V_{REF}	0	1 to 2	2.7	V
Resistance (pin 21 to pin 20) with REF supply and R, G, B outputs OFF	R_{REF}	–	125	–	Ω

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parameter	symbol	min.	typ.	max.	unit
OUTPUTS					
SAND					
Output voltage high level at I_O = 0 to −30 μA	V_{OH}	4.2	–	V_{DD}	V
Output voltage intermediate level at I_O = −30 to + 30 μA	V_{OI}	1.3	2.0	2.7	V
Output voltage low level at I_O = 0.2 mA	V_{OL}	0	–	0.2	V
Load capacitance	C_L	–	–	30	pF
F1/6, CLKO, $\overline{\text{DDA}}$/$\overline{\text{FS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.4	V
Load capacitance	C_L	–	–	50	pF
$\overline{\text{LDS}}$, $\overline{\text{AS}}$					
Output voltage HIGH at I_{OH} = −200 μA	V_{OH}	2.4	–	V_{DD}	V
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.4	V
Load capacitance	C_L	–	–	200	pF
$\overline{\text{DTACK}}$, $\overline{\text{BR}}$ (open drain outputs)					
Output voltage LOW at I_{OL} = 3.2 mA	V_{OL}	0	–	0.4	V
Load capacitance	C_L	–	–	150	pF
Capacitance (OFF state)	C_{OFF}	–	–	7	pF
R, G, B (note 2)					
Output voltage HIGH (note 3) at I_{OH} = −100 μA; V_{REF} = 2.7 V	V_{OH}	2.4	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Output resistance during line blanking	R_{OBL}	–	–	150	Ω
Output capacitance (OFF state)	C_{OFF}	–	–	12	pF
Output leakage current (OFF state) at V_I = 0 to V_{DD}+ 0.3 V; T_{amb} = 25 °C	I_{OFF}	−10	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
$\overline{VDS}$					
Output voltage HIGH at $I_{OH} = -250\ \mu A$	V_{OH}	2.4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 2$ mA	V_{OL}	0	–	0.4	V
Output voltage LOW at $I_{OL} = 1$ mA	V_{OL}	0	–	0.2	V
Output leakage current (OFF state) at $V_I = 0$ to $V_{DD}+0.3$ V; $T_{amb} = 25\ ^oC$	I_{OFF}	−10	–	+ 10	μA
INPUT/OUTPUTS					
VCS/OSCO					
Input voltage HIGH	V_{IH}	2.0	–	6.0	V
Input voltage LOW	V_{IL}	0	–	0.8	V
Input current (output OFF) at $V_I = 0$ to $V_{DD}+0.3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
$\overline{TCS}$					
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input voltage LOW	V_{IL}	0	–	1.5	V
Input current at $V_I = 0$ to $V_{DD}+0.3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200$ to $100\ \mu A$	V_{OH}	2.4	–	6.0	V
Output voltage LOW at $V_{OL} = 3.2$ mA	V_{OL}	0	–	0.4	V
Load capacitance	C_L	–	–	50	pF
A1/D0 to A16/D15, $\overline{UDS}$, R/$\overline{W}$					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	6.0	V
Input current at $V_I = 0$ to $V_{DD}+0.3$ V; $T_{amb} = 25\ ^oC$	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage HIGH at $I_{OH} = -200\ \mu A$	V_{OH}	2.4	–	V_{DD}	V
Output voltage LOW at $I_{OL} = 3.2$ mA	V_{OL}	0	–	0.4	V
Load capacitance	C_L	–	–	200	pF

parameter	symbol	min.	typ.	max.	unit
TIMING					
F6 (Fig. 3)					
Rise and fall times	t_r, t_f	10	–	80	ns
Frequency	f_{F6}	5.9	–	6.1	MHz
CLKO, F1/6, R, G, B, $\overline{VDS}$, $\overline{FS}$/$\overline{DDA}$, $\overline{OD}$ (notes 4, 5 and Fig. 6)					
CLKO HIGH time	t_{CLKH}	30	–	–	ns
CLKO LOW time	t_{CLKL}	20	–	–	ns
CLKO rise and fall times	t_{CLKr} t_{CLKf}	–	–	10	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ change	t_{VCH}	10	–	–	ns
R, G, B, $\overline{VDS}$ valid to CLKO rise	t_{VOC}	10	–	–	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ valid	t_{COV}	–	–	60	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ floating after $\overline{OD}$ fall	t_{FOD}	–	–	30	ns
Skew between outputs R, G, B, $\overline{VDS}$	t_{VS}	–	–	20	ns
R, G, B, $\overline{VDS}$ rise and fall times	t_{Vr}, t_{Vf}	–	–	30	ns
CLKO HIGH to R, G, B, $\overline{VDS}$ active after $\overline{OD}$ rise	t_{AOD}	0	–	–	ns
CLKO HIGH to $\overline{FS}$/$\overline{DDA}$ change	t_{COD}	–	–	55	ns
$\overline{FS}$/$\overline{DDA}$ valid to CLKO rise	t_{DOC}	5	–	–	ns
F1 HIGH time (note 6)	t_{F1H}	–	500	–	ns
F1 LOW time (note 6)	t_{F1L}	–	500	–	ns
F6 HIGH time	t_{F6H}	–	83	–	ns
F6 LOW time	t_{F6L}	–	83	–	ns
$\overline{OD}$ to CLKO rise set-up	t_{ODS}	–	–	45	ns
$\overline{OD}$ to CLKO HIGH hold	t_{ODH}	–	–	0	ns
MEMORY ACCESS TIMING (notes 7, 8, 9 and Fig. 7)					
$\overline{UDS}$, $\overline{LDS}$, $\overline{AS}$					
Cycle time	t_{cyc}	–	500	–	ns
$\overline{UDS}$ HIGH to bus-active for address output	t_{SAA}	75	–	–	ns
Address valid set-up to $\overline{AS}$ fall	t_{ASU}	20	–	–	ns
Address valid hold from $\overline{AS}$ LOW	t_{ASH}	20	–	–	ns
Address float to $\overline{UDS}$ fall	t_{AFS}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
$\overline{AS}$ LOW to $\overline{UDS}$ fall delay	t_{ATD}	50	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ HIGH time	t_{HDS}	220	–	–	ns
$\overline{UDS}$, $\overline{LDS}$ LOW time	t_{LDS}	200	–	–	ns
$\overline{AS}$ HIGH time	t_{HAS}	125	–	–	ns
$\overline{AS}$ LOW time	t_{LAS}	320	–	–	ns
$\overline{AS}$ LOW to $\overline{UDS}$ HIGH	t_{AUH}	305	–	–	ns
Data valid set-up to $\overline{UDS}$ rise	t_{DSU}	30	–	–	ns
Data valid hold from $\overline{UDS}$ HIGH	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{AS}$ rise delay	t_{UAS}	0	–	–	ns
$\overline{AS}$ LOW to data valid	t_{AFA}	–	–	270	ns
Link-through buffers (notes 7, 8 and Fig. 8)					
$\overline{BUFEN}$ LOW to output valid	t_{BEA}	–	–	100	ns
Link-through delay time	t_{LTD}	–	–	85	ns
Input data float prior to direction change	t_{IFR}	0	–	–	ns
Output float after direction change	t_{OFR}	–	–	60	ns
Output float after $\overline{BUFEN}$ HIGH	t_{BED}	–	–	60	ns
Microprocessor READ from EUROM (Fig. 9)					
R/$\overline{W}$ HIGH set-up to $\overline{UDS}$ fall	t_{RUD}	0	–	–	ns
$\overline{UDS}$ LOW to returned-data access time	t_{UDA}	–	–	210	ns
$\overline{RE}$ LOW to returned data access time	t_{REA}	–	–	210	ns
Data valid to $\overline{DTACK}$ LOW delay	t_{DTL}	–20	–	–	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	50	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	0	–	–	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	10	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ fall	t_{UDR}	0	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DSD}	190	–	260	ns
Address valid to $\overline{UDS}$ fall	t_{AUL}	0	–	–	ns

parameter	symbol	min.	typ.	max.	unit
MEMORY ACCESS TIMING (continued)					
Microprocessor WRITE to EUROM (Fig. 10)					
Write cycle time (note 10)	t_{WCY}	500	–	–	ns
R/$\overline{W}$ LOW set-up to $\overline{UDS}$ fall	t_{WUD}	0	–	–	ns
$\overline{RE}$ LOW to $\overline{UDS}$ fall	t_{RES}	30	–	–	ns
Address valid to $\overline{UDS}$ fall	t_{ASS}	30	–	–	ns
$\overline{UDS}$ LOW time	t_{LUS}	100	–	–	ns
Data valid to $\overline{UDS}$ rise	t_{DSS}	80	–	–	ns
$\overline{UDS}$ LOW to $\overline{DTACK}$ LOW	t_{DTA}	0	–	60	ns
$\overline{DTACK}$ LOW to $\overline{UDS}$ rise	t_{DLU}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{DTACK}$ rise	t_{DTR}	0	–	50	ns
$\overline{UDS}$ HIGH to data hold	t_{DSH}	0	–	–	ns
$\overline{UDS}$ HIGH to address hold	t_{DSA}	0	–	–	ns
$\overline{UDS}$ HIGH to $\overline{RE}$ rise	t_{SRE}	10	–	–	ns
$\overline{UDS}$ HIGH to R/$\overline{W}$ rise	t_{UDW}	0	–	–	ns
F1/6 to memory access cycle (Fig. 11)					
$\overline{UDS}$ HIGH to F6 (component of F1/6) rise	t_{UF6}	20	–	–	ns
F6 (component of F1/6) HIGH to $\overline{UDS}$ rise	t_{F6U}	40	–	–	ns
SYNCHRONIZATION and BLANKING					
$\overline{TCS}$, SAND, $\overline{FS/DDA}$					
See Fig. 12 for timing relationships and Fig. 13 for vertical sync and blanking waveforms.					

Notes to the characteristics

1. Pin 30 must be biased externally as it is internally a.c. coupled.
2. 16-level analogue voltage outputs.
3. Output voltage guaranteed when programmed for top level.
4. CLKO, R, G, B, F1/6, $\overline{VDS}$: C_L = 25 pF
   $\overline{FS/DDA}$: C_L = 50 pF
5. CLKO, F1/6, $\overline{VDS}$, $\overline{FS/DDA}$: reference levels = 0.8 to 2.0 V
   R, G, B: reference levels = 0,8 to 2,0 V with V_{REF} = 2.7 V
6. These times may momentarily be reduced to a nominal 83 ns in slave-sync mode at the moment of re-synchronization.
7. C_L = 150 pF.
8. Reference levels = 0.8 to 2.0 V.
9. F6 input at 6 MHz.
10. Microprocessor write cycle times of less than 500 ns are permitted but often result in Wait States being generated, the precise timing of $\overline{DTACK}$ will then depend on the internal synchronization time.

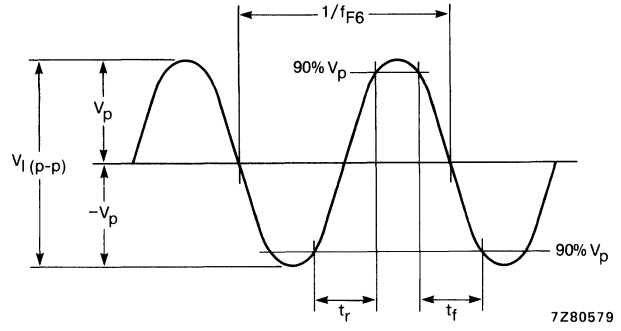
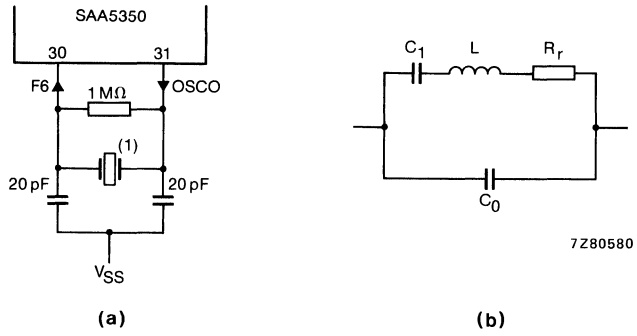


Fig. 3 F6 input waveform.



(1) Catalogue number of crystal: 4322 143 04101

Fig. 4(a) Oscillator circuit for SAA5350 stand-alone sync mode and (b) equivalent circuit of crystal at resonance (see **characteristics** for values).

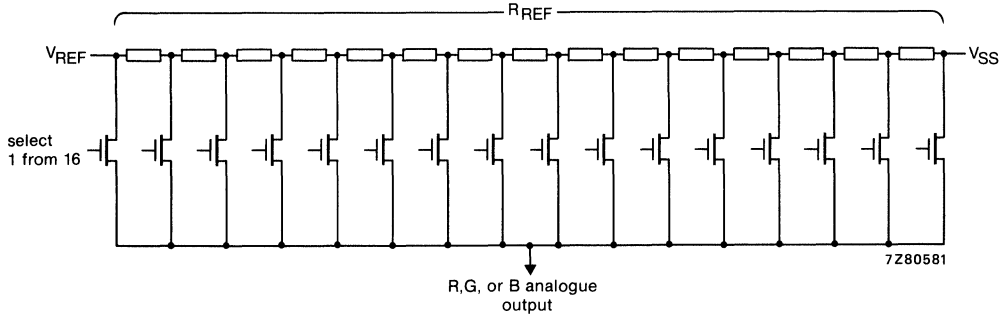


Fig. 5 Circuit arrangement giving one-of-sixteen reference voltage levels for the R, G or B analogue outputs.

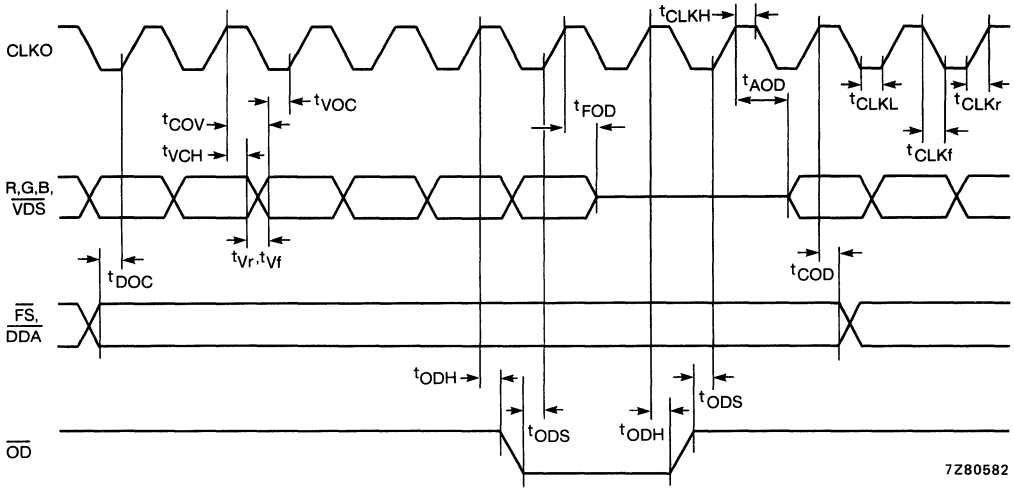


Fig. 6 Video timing.

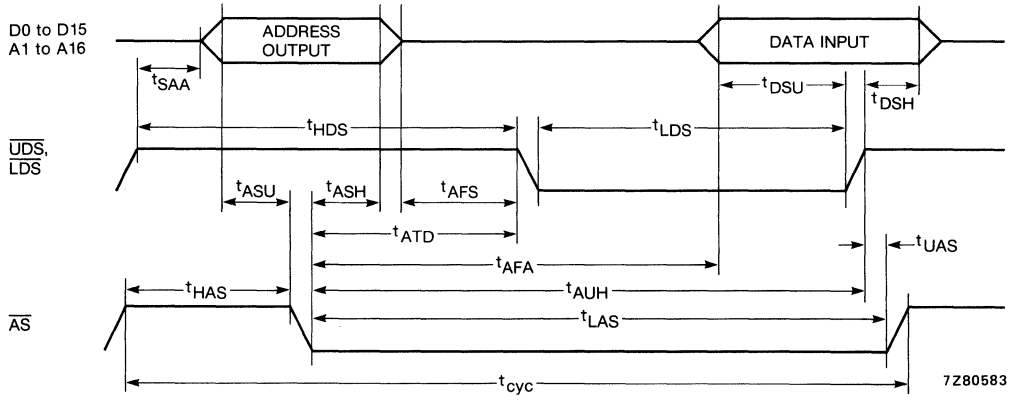


Fig. 7 Memory access timing.

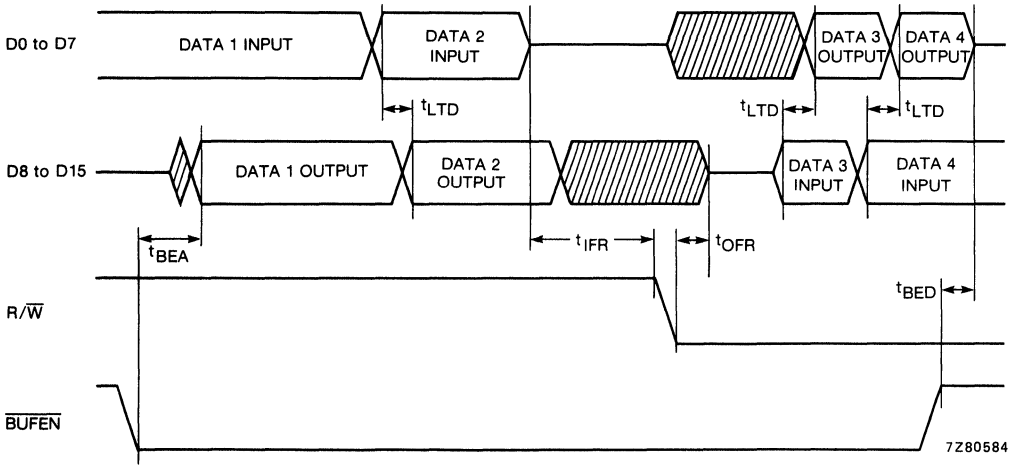


Fig. 8 Timing of link-through buffers.

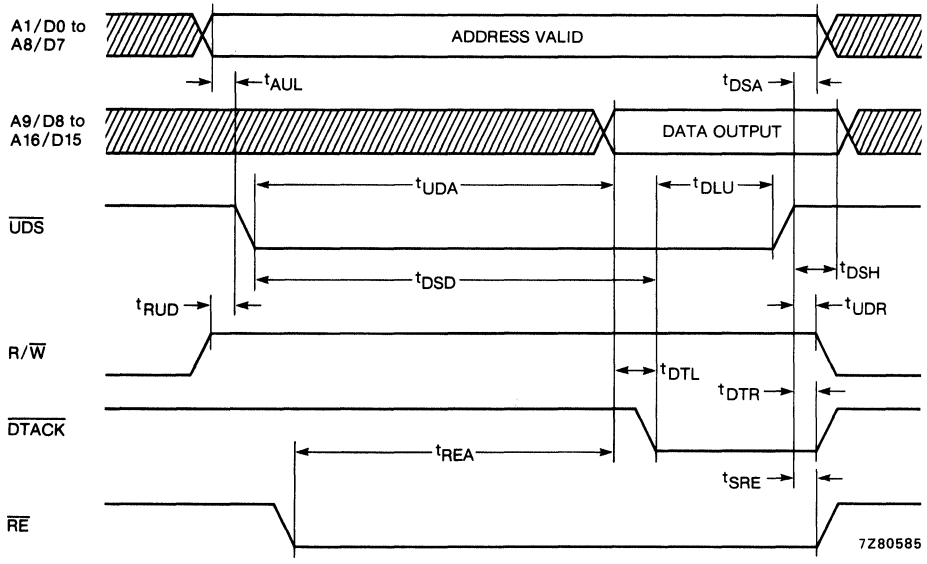


Fig. 9 Timing of microprocessor read from EUROM.

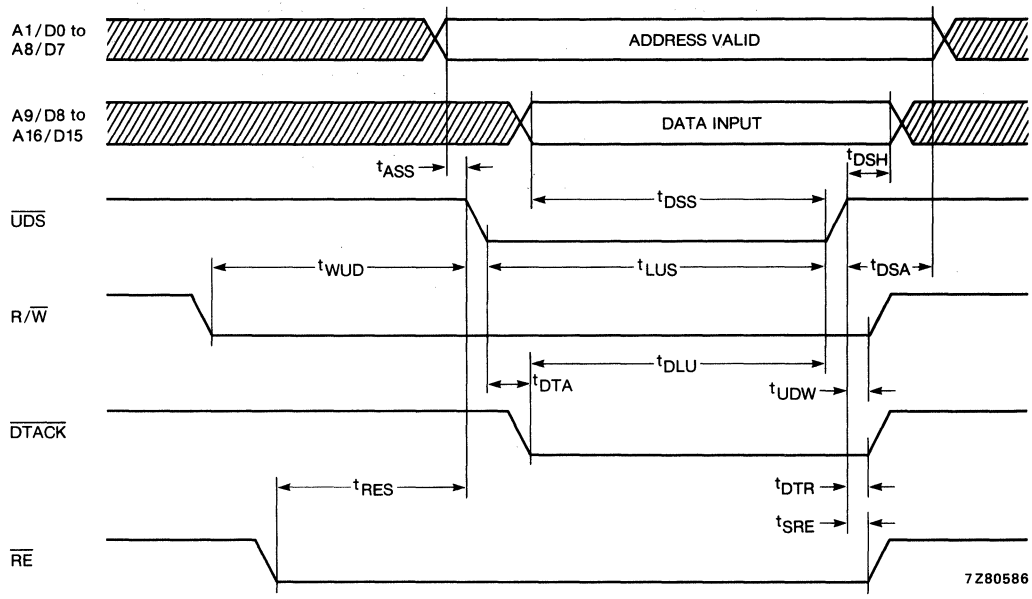


Fig. 10 Timing of microprocessor write to EUROM.

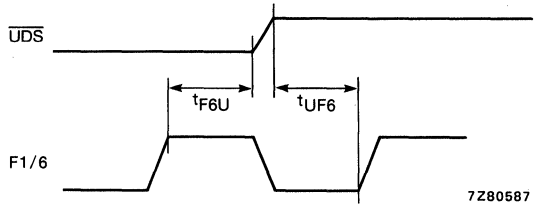


Fig. 11 Timing of F1/6 to memory access cycle.

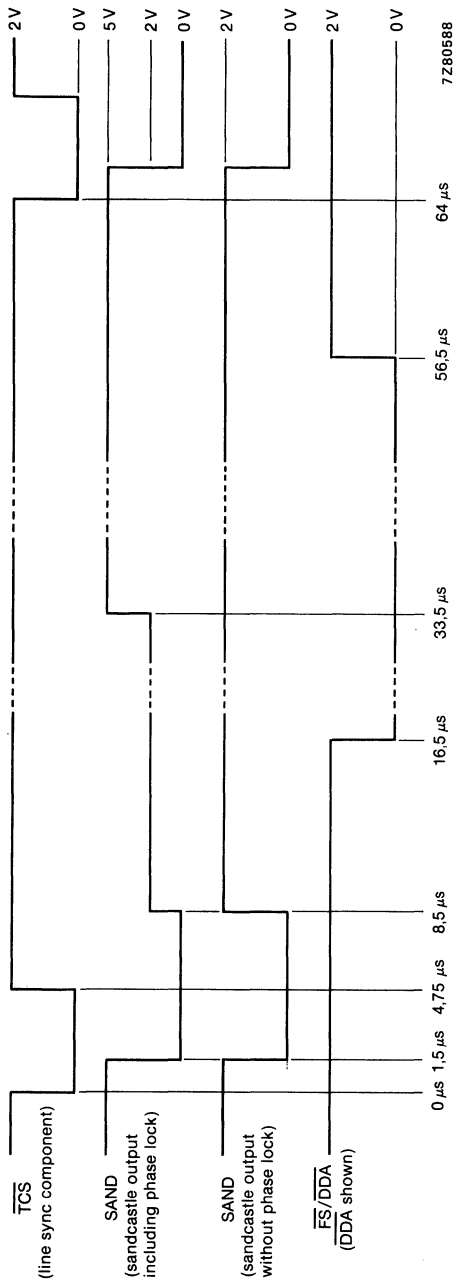


Fig. 12 Timing of synchronization and blanking outputs; all timings are nominal and assume f_{F6} = 6 MHz.

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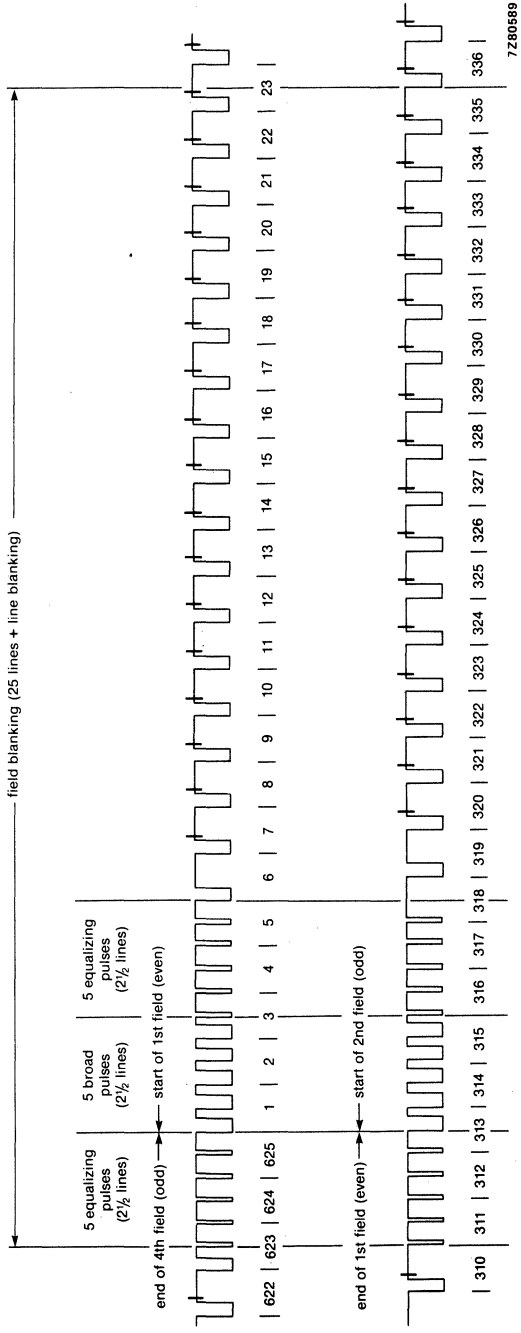


Fig. 13 Vertical synchronization and blanking waveforms; separation of broad pulses = 4.75 μs; equalizing pulse widths = 2.25 μs.

APPLICATION INFORMATION

More detailed application information is available on request

BASIC VIDEOTEX DECODER CONFIGURATION

A basic, practical decoder configuration is shown in Fig. 14, reference should also be made to the block diagram Fig. 1.

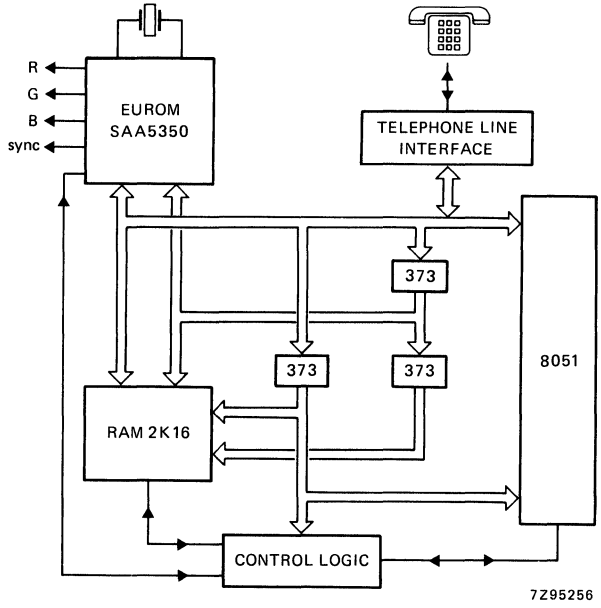


Fig. 14 Basic videotex decoder configuration.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (in stack mode) and then fed into one half of the dual display row buffer. The data fetch process takes place during one line-flyback period (per row) and, since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows — each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colours, and during the display time it is also used for addressing DRCS characters.

Timing

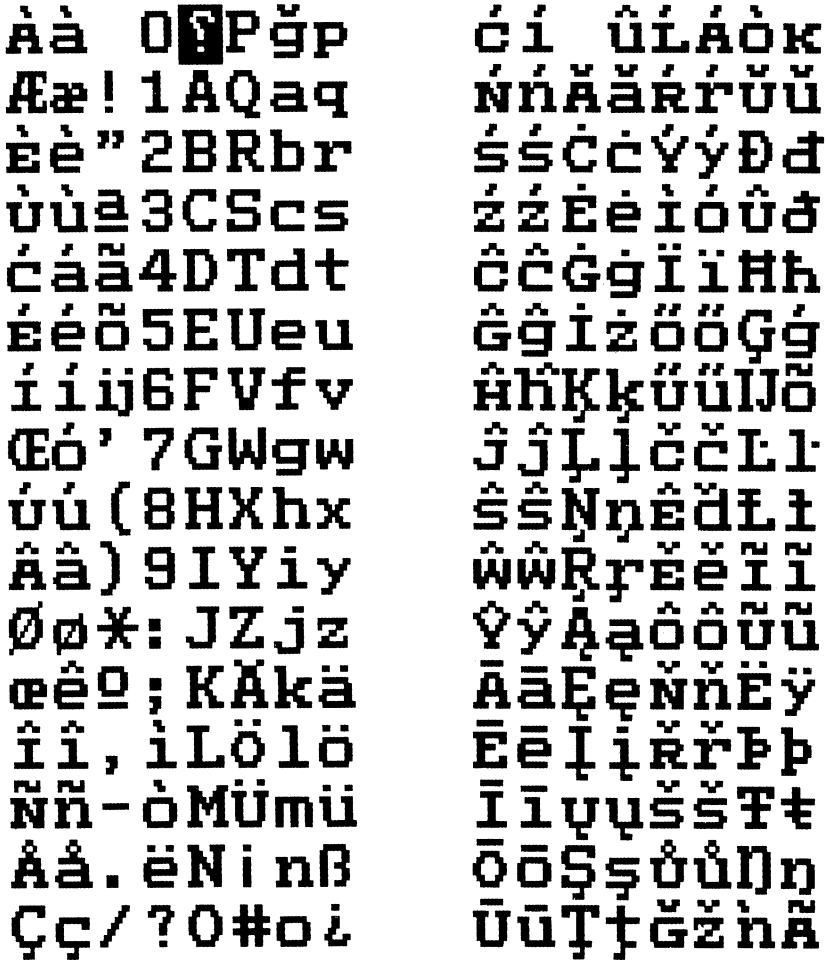
The timing chain operates from an external 6 MHz clock or an on-chip fixed-frequency crystal oscillator. The basic video format is 40 characters per row, 24/25 rows per page and 10 video lines per row. EUROM will also operate with 20/21 rows per page and 12 video lines per row. The two extra lines per row are added symmetrically and contain background colour only for ROM-based alpha-numeric characters. DRCS characters, block and smooth mosaics and line drawing characters occupy all 12 lines.

The display is generated to the normal 625-line/50 Hz scanning standard (interlaced or non-interlaced). In addition to composite sync (pin 32) for conventional timebases, a clock output at 1 MHz or 6 MHz

(pin 29) is available for driving other videotex devices, and a 12 MHz clock (pin 27) is available for hard-copy dot synchronization. A defined-display-area timing signal (pin 33) simplifies the application of external peripherals such as a light pen; this signal is nominally coincident with the character dot information.

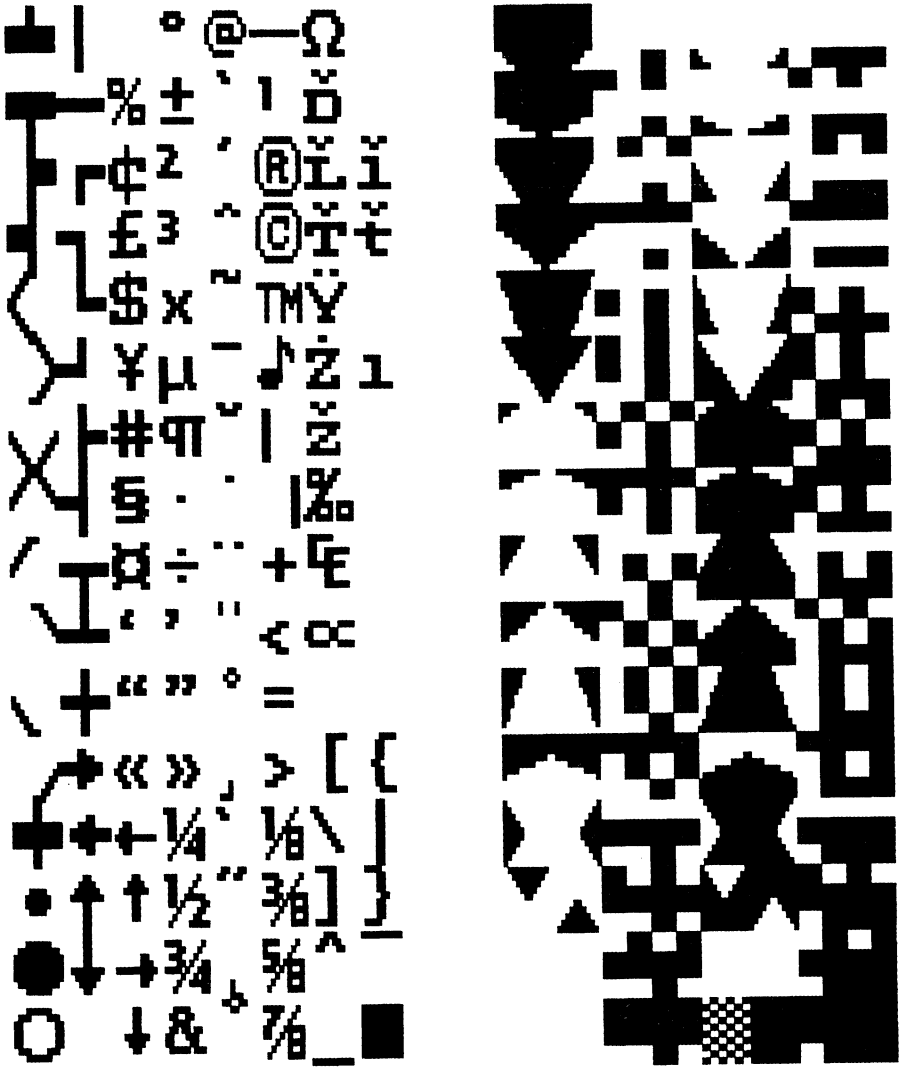
Character generation

EUROM supports eight character tables, each of (nominally) 128 characters. Four tables are in on-chip ROM and contain fixed characters and four are stored in an external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figs 15 and 16.



(a) (b)

Fig. 15 On-chip characters: (a) Table 0; (b) Table 1.



(a) (b)

Fig. 16 On-chip characters: (a) Table 2; (b) Table 3.

The 128 most commonly used characters are contained in Table 0, these are the standard upper and lower-case letters of the Roman alphabet, numerals, punctuation and the more common accented characters. In normal text transmission, Table 0 is used most of the time. Table 1 contains other accented characters. Miscellaneous characters, mathematical symbols, the line drawing character set and accents without associated symbols are contained in Table 2. Table 3 contains the block mosaics for the basic alpha-mosaic service and also the new smooth mosaics.

The four tables stored in the external RAM (Tables 4 to 7) are used for DRCS.

Scroll map

The scroll map uses a 26-byte area of on-chip RAM and functions in association with the timing chain. It maps the scan row on to the fetched memory row so allowing the stored page to be displayed in any row order. For each row, a 1-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to, or from, side storage.
Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Colour map and digital-to-analogue converters

The colour map RAM contains thirty-two 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D-A converter. The resulting R, G and B outputs are low-impedance with peak-to-peak amplitudes controlled by the reference voltage applied at pin 21.

Cursor

The cursor is available in the stack mode. Its position, character code, character table, foreground colour, background colour, lining and flash attributes are all software programmable via internal register bits.

NON-VIDEOTEX APPLICATIONS

For non-Videotex applications, the device will also support the following operating modes:

Explicit fill mode. An alternative 40 character/rows mode which does not use the memory compression technique of stack coding. More display memory is required but there are no limitations on the number of display attribute changes per row.

80 characters/rows mode. When operating with 80 characters per row, the available display attributes are eight foreground colours, eight (potentially different) background colours (including transparent) as well as underline and blink.

Full field DRCS mode. This mode is not mutually exclusive to the explicit fill and 80 characters/rows modes but rather the available DRCS memory is expanded so that the whole screen can be covered, thus enabling a 'bit map'. All ROM-based characters and all display attributes remain available.

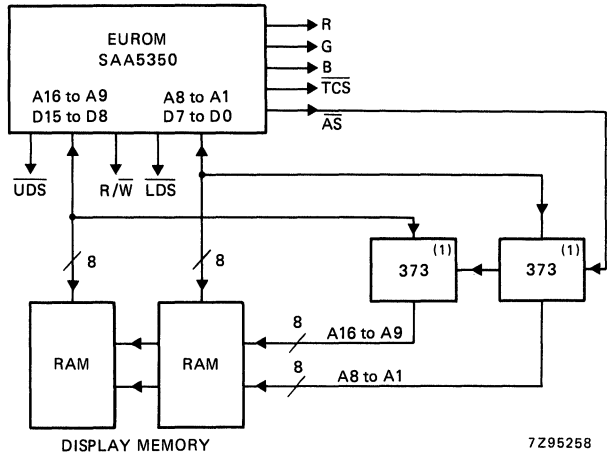
MICROPROCESSOR and RAM BUS INTERFACE

Three types of data transfer take place at the bus interface:

- EUROM fetches data from the display memory
- The microprocessor reads from, or writes to, EUROM's internal register map
- The microprocessor accesses the display memory

EUROM access to display memory (Figs 17 and 18)

EUROM accesses the external display memory via a 16-bit multiplexed address and data bus with a cycle time of 500 ns. The address strobe ($\overline{AS}$) signal from EUROM flags the bus cycle and writes the address into octal latches (74LS373). The display data is stored in bytes of upper (most-significant) and lower (least-significant) display information and is always fetched in pairs of bytes (upper + lower = 16 bits). The upper and lower display RAM sections are enabled simultaneously by the upper and lower data strobes (respectively $\overline{UDS}$ and $\overline{LDS}$) which are always asserted together to fetch a 16-bit word. The read/write control R/$\overline{W}$ is included although EUROM only reads from the display memory.



(1) 74LS373 octal transparent latch (3-state)

Fig. 17 Simple RAM interface circuit for display memory access.

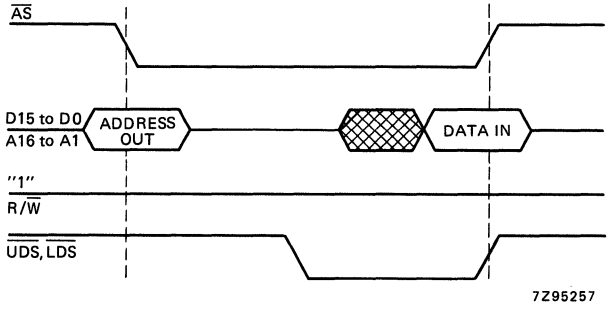


Fig. 18 Bus timing for display memory access.

The display memory organization uses the word/byte addressing convention adopted for the SCN68000 microprocessor series. Data fetched on the 16-bit bus is considered in terms of bytes where the even numbered bytes use the upper (most-significant) part of the bus as shown in Fig. 19. The word addresses are numerically the same as the upper byte that they contain – there are no odd-numbered word addresses.

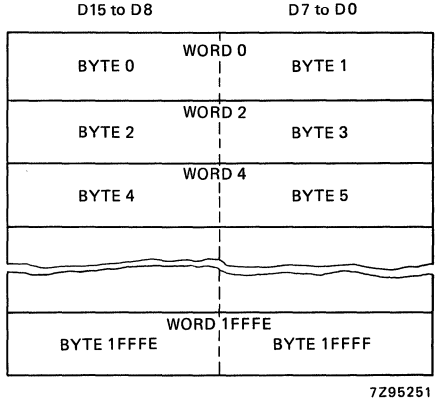


Fig. 19 Display memory word/byte organization.

Warning time

As EUROM is a real-time display device, it must have direct access to the display memory with priority over the microprocessor and other peripheral devices. This is achieved by EUROM issuing a bus request ($\overline{BR}$) signal for the duration of the memory access plus a programmable advance warning time which allows the microprocessor to complete its current bus cycle.

In systems where the buses of the microprocessor and EUROM are intimately connected (connected systems), $\overline{BR}$ may be used to suspend all microprocessor activity so that EUROM can act as a dedicated DMA controller. In systems where the two buses are separated by buffers (disconnected systems), $\overline{BR}$ may be used either to generate an interrupt or as a direct signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of EUROM's bus activity is programmable to be between 0 and 23 μs.

Microprocessor access to register map

EUROM has a set of internal registers which, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of the data bus (Fig. 20). The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled by the signal $\overline{RE}$. Addresses are input via the lower part of the bus. A data transfer acknowledge signal ($\overline{DTACK}$) indicates to the microprocessor that the data transfer is complete.

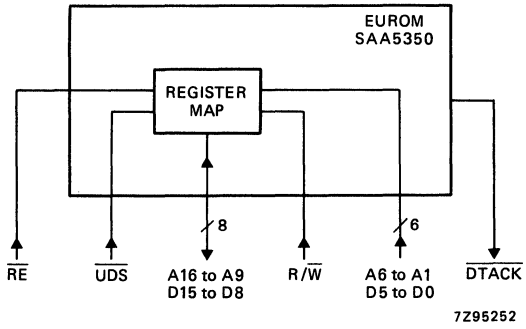


Fig. 20 Microprocessor access to register map.

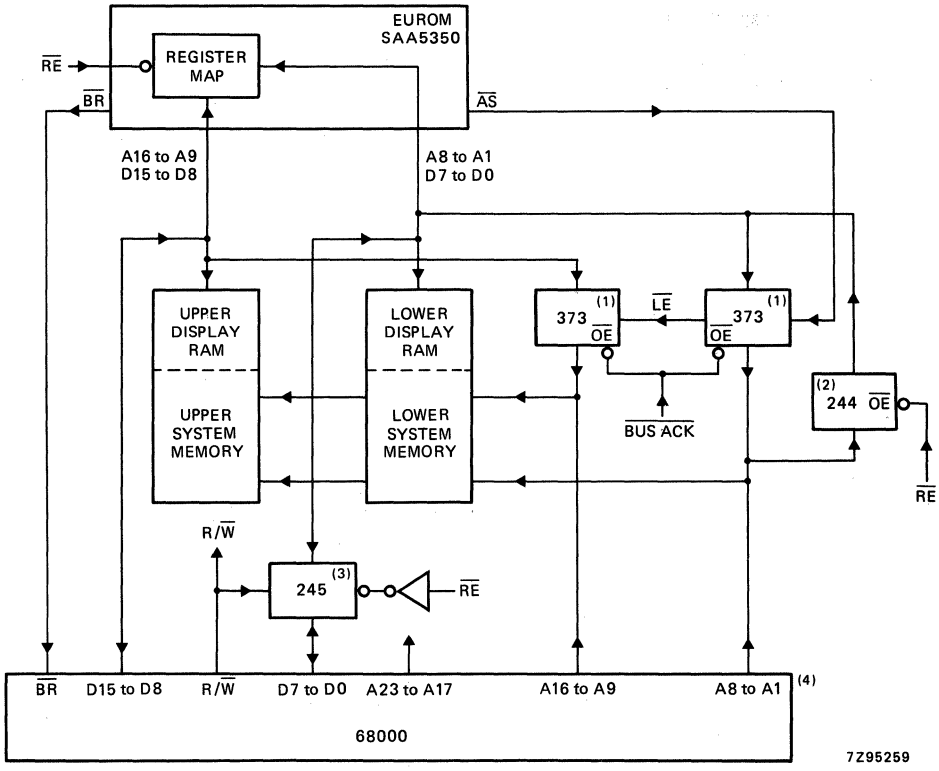
The main data and address paths used in a connected 68000 interface are shown in Fig. 21. The outputs from the octal latches (74LS373) are enabled only when the 68000 has made the bus available in response to a bus request ($\overline{BR}$). When the register map is accessed data is transferred via the upper part of the bus and the microprocessor's low-order address is passed to EUROM via the octal buffers (74LS244). At the same time the bidirectional buffers (74LS245) disable the signals from the low order data bus of the 68000.

The buffers '244 and '245 may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by EUROM as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of EUROM's scroll map contents at a location in its main memory.

8-bit microprocessors

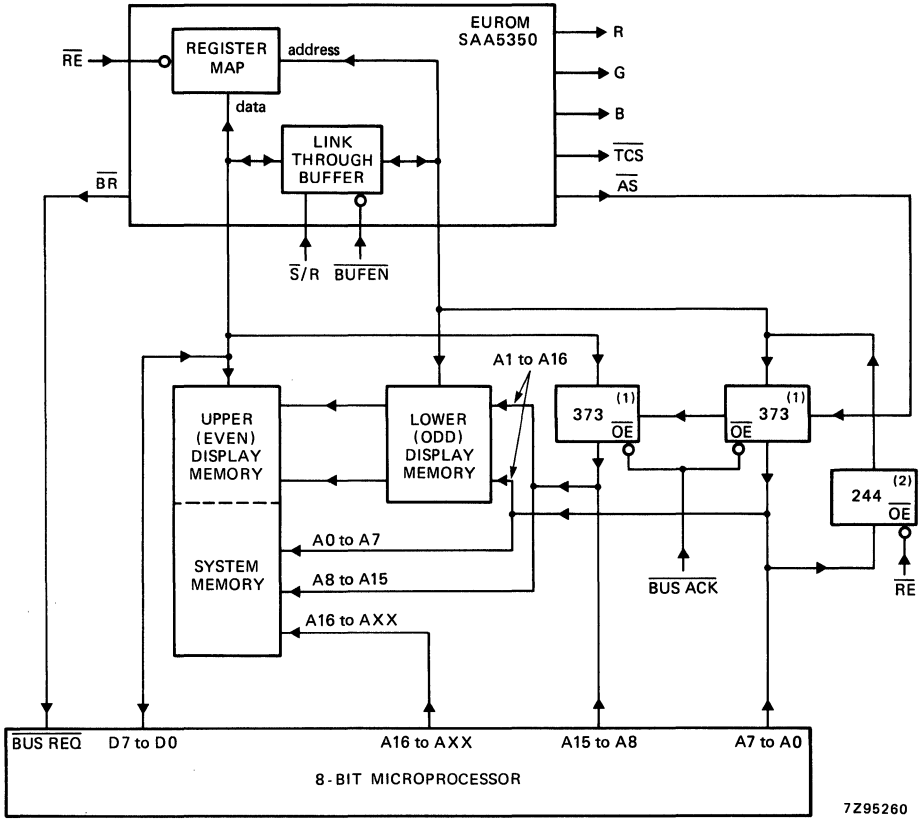
Although the control bus is optimised for the SCN68000 16-bit microprocessor unit, EUROM will operate with a number of widely differing industry-standard 8, 16 or more-bit microprocessors or microcontrollers (e.g. SCN68008, MAB8051). The interfacing of 8-bit microprocessors to the 16-bit wide display memory is made simple by EUROM's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd) half of the memory. The link-through buffer is enabled by the buffer-enable signal $\overline{BUFEN}$, and the send/receive direction is controlled by the signal $\overline{S}$/R.

The main data and address paths used in a connected 8-bit microprocessor system are shown in Fig. 22. The interface is similar to that of the 16-bit system but here the display memory does not receive A0 as an address, rather A0 is used as the major enabling signal for $\overline{BUFEN}$ (enables when HIGH).



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 74LS245 octal bus transceiver (3-state)
(4) SCN68000 microprocessor unit

Fig. 21 Connected 16-bit microprocessor system.

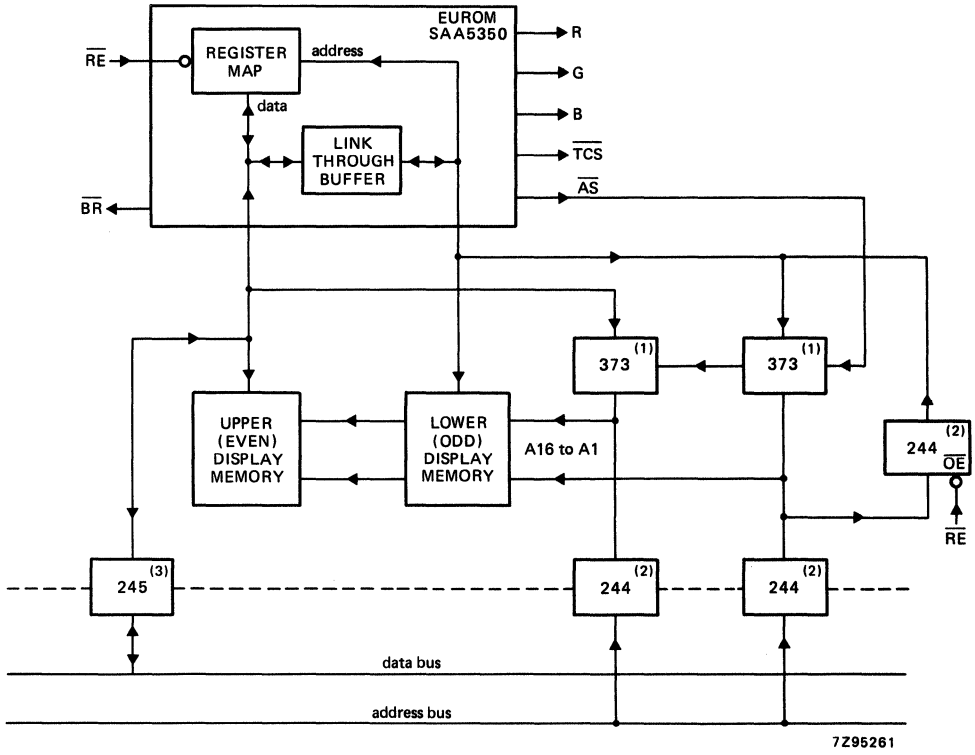


(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)

Fig. 22 Connected 8-bit microprocessor system.

Disconnected systems

For many applications it may be desirable to disconnect EUROM and the display memory from the microprocessor and its ROM, RAM and other peripherals by using isolating buffers as shown in Fig. 23. The two parts of the system then operate independently and communicate only when the microprocessor accesses EUROM's register map or the display memory.



(1) 74LS373 octal transparent latch (3-state)
(2) 74LS244 octal buffer (3-state)
(3) 75LS245 octal bus transceiver (3-state)

Fig. 23 Disconnected 8-bit system.

Synchronization

Stand-alone mode

As a stand-alone device (e.g. in terminal applications) EUROM can output a composite sync signal ($\overline{TCS}$) to the display timebase IC or to a monitor. Timing is obtained from a 6 MHz on-chip oscillator using an external crystal as shown in Fig. 24.

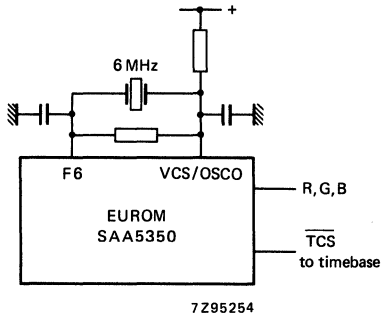


Fig. 24 Stand-alone synchronization mode.

Simple-slave

In the simple-slave mode EUROM synchronizes directly to another device, such as to the $\overline{TCS}$ signal from the SAA5240 European computer-controlled teletext circuit (CCT) or from another EUROM as shown in Fig. 25. EUROM's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built in to avoid resetting the counter at every tv line and so prevents screen jitter.
Field synchronization is made using EUROM's internal field sync separator.

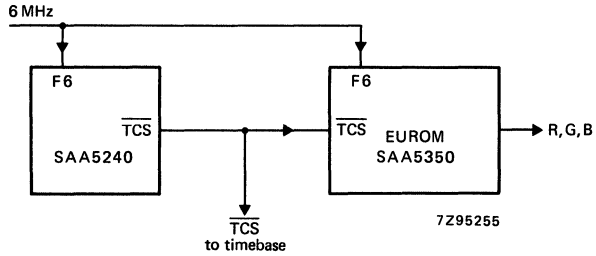


Fig. 25 Simple-slave (direct sync) mode.

Phase-locked slave

The phase-locked slave (indirect sync) mode is shown in Fig. 26. A phase-locked VCO in the SAA5230 teletext video processor provides sync to the timebases. When EUROM is active, its horizontal counter forms part of the phase control loop – a horizontal reference is fed back to the SAA5230 from the SAND output and a vertical reference is generated by feeding separated composite sync to EUROM's field sync separator via the VCS input. In the phase-locked slave mode, the display derived from EUROM can sync with that from a tv source or a local VLP player, thus giving picture-in-text display possiblities.

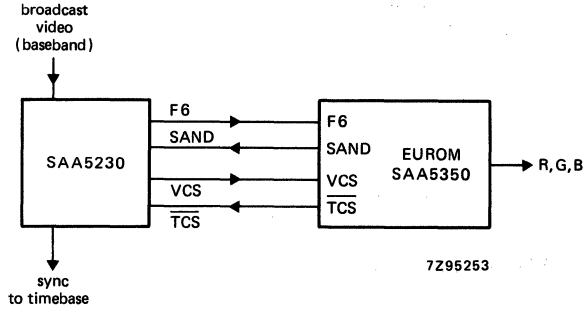
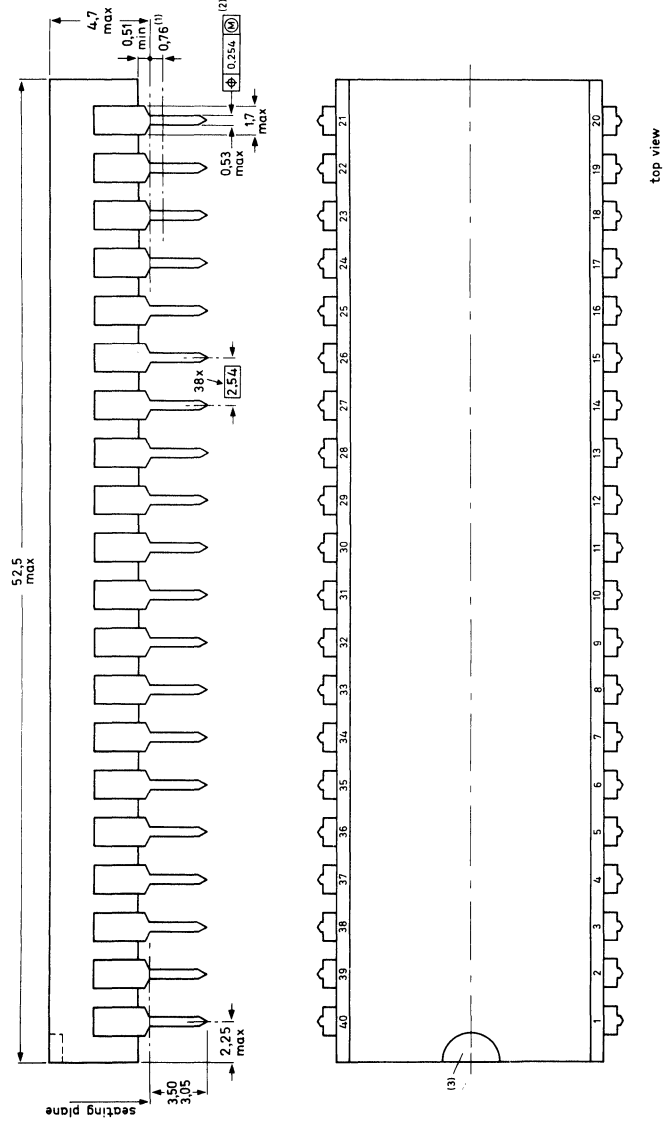
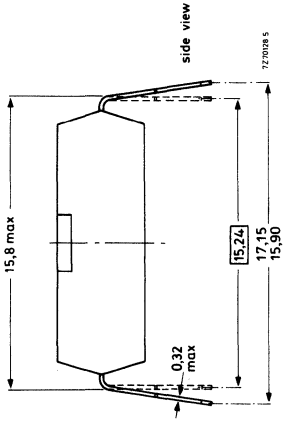


Fig. 26 Phase-locked slave (indirect sync) mode.

40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See next page.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

Clock/Calendar with Serial I/O PCF8573

GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS circuit that functions as a real time clock/calendar in the Inter IC (I^2C) bus-oriented microcomputer systems. The device includes an addressable time counter and an addressable alarm register, both for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred serially via a two line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1,2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal-controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

5

QUICK REFERENCE DATA

Supply voltage range (clock)	$V_{DD}-V_{SS1}$		1,1 to 6,0 V
Supply voltage range (I^2C interface)	$V_{DD}-V_{SS2}$		2,5 to 6,0 V
Crystal oscillator frequency	f_{osc}	typ.	32,768 kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT-38).
PCF8573T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

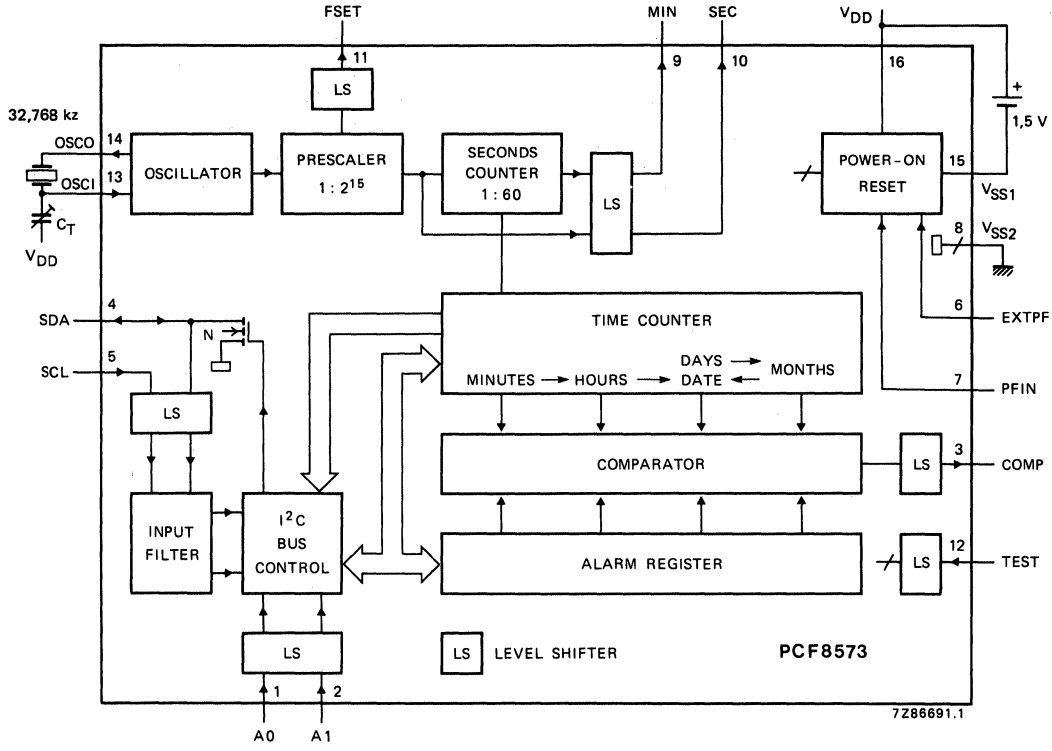


Fig. 1 Block diagram.

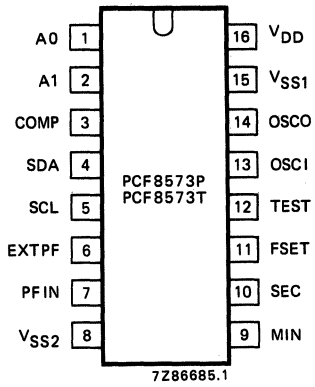


Fig. 2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C bus
5	SCL	serial clock line	I^2C bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (see note)
			or 29 → 01	
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note: Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

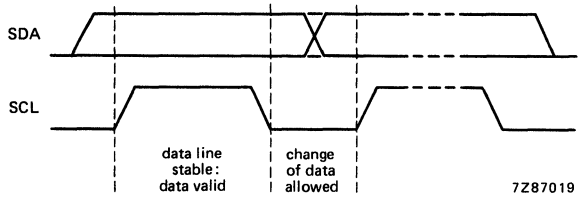


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

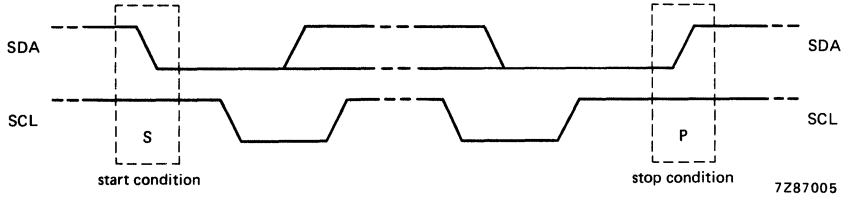


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

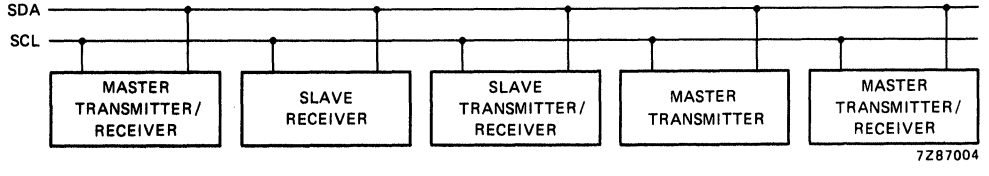


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 13 and Fig. 14.)

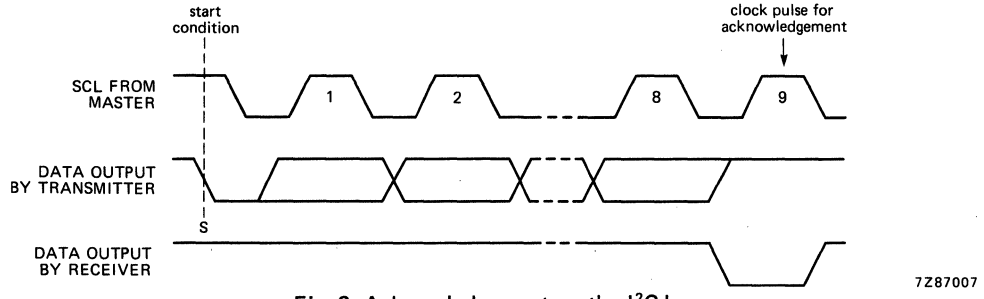


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8573 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

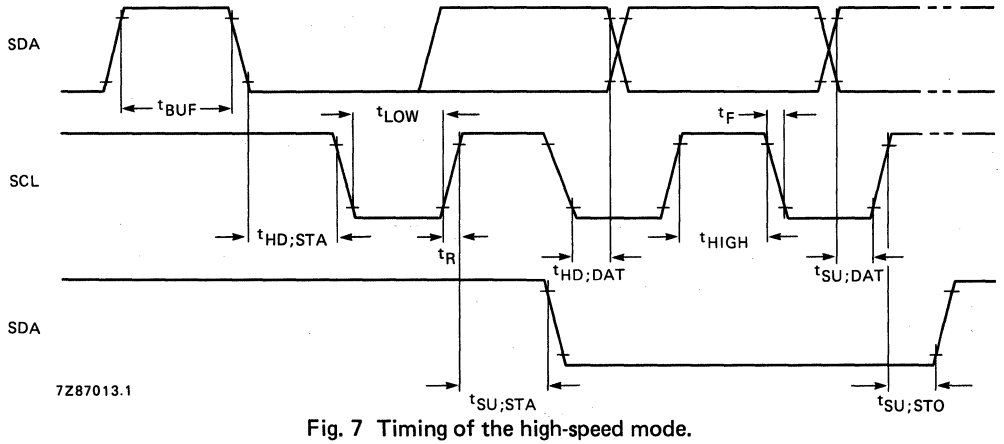


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

5

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

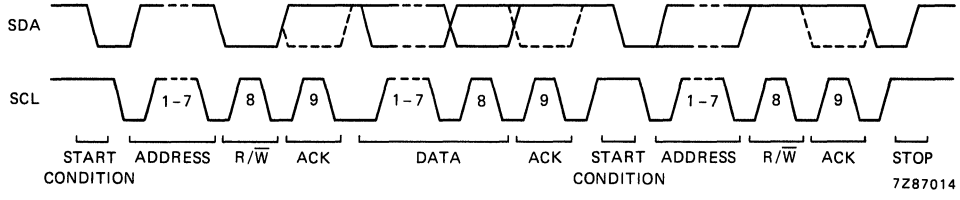


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

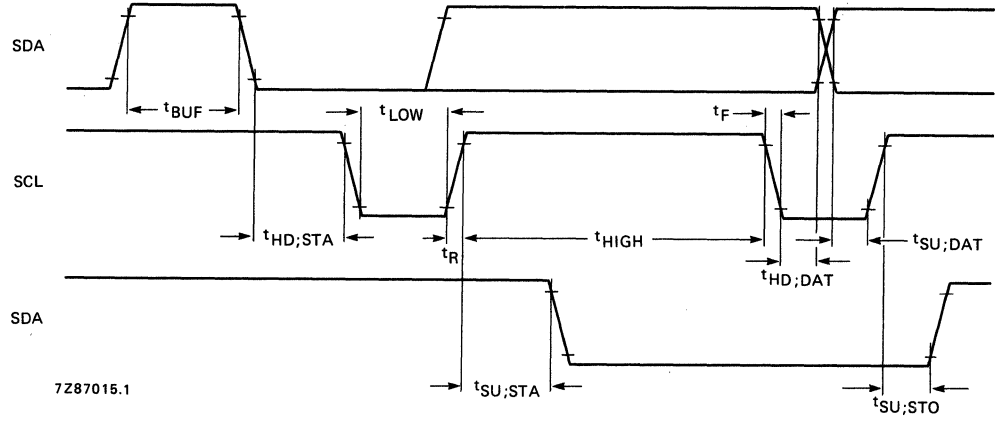


Fig. 9 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}, for definitions see high-speed mode.

* Only valid for repeated start code.

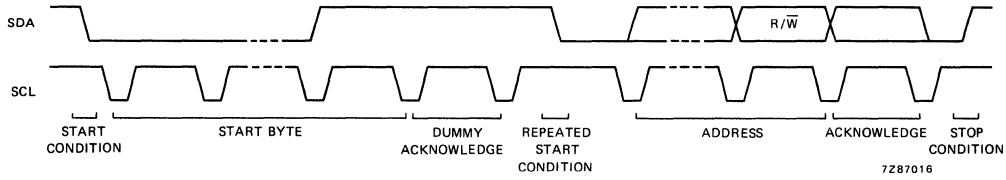


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

5

ADDRESSING

Before any data is transmitted on the I^2C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 11.

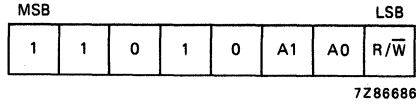


Fig. 11 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I^2C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 12 and Fig. 13.

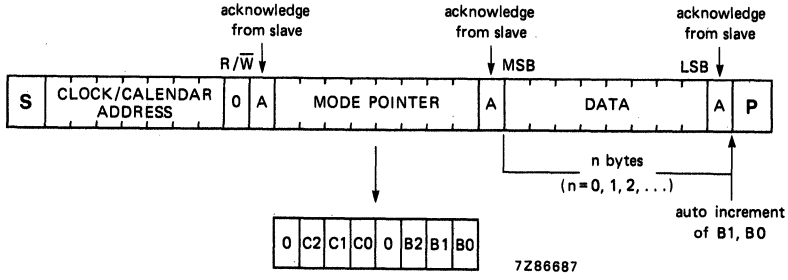


Fig. 12 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

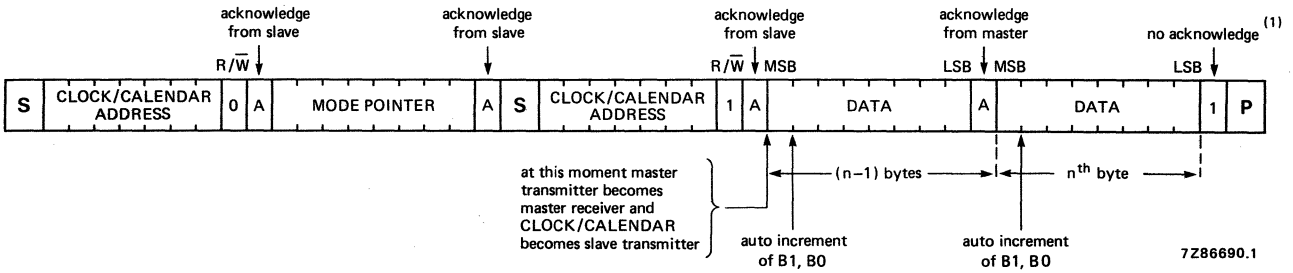
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where "X" is the don't care bit and "D" is the data bit.

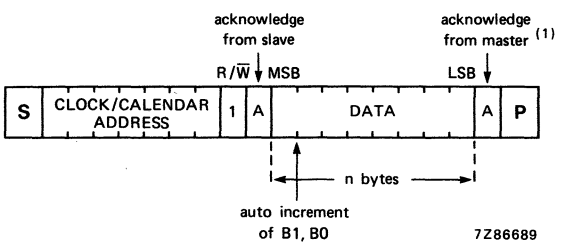
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 13 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 14 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where "X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where: "D" is the data bit.
* = minutes.
** = seconds.

5

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges	$V_{DD}-V_{SS1}$		−0,3 to +8	V
	$V_{DD}-V_{SS2}$		−0,3 to +8	V
Voltage on pins 4 and 5			V_{SS2}−0,8 to V_{DD} +0,8	V*
Voltage on pins 6, 7, 13 and 14			V_{SS1}−0,6 to V_{DD} +0,6	V
Voltage on any other pin			V_{SS2}−0,6 to V_{DD} +0,6	V
Input current	I_I	max.	10	mA
Output current	I_O	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−40 to +85	°C
Storage temperature range	T_{stg}		−55 to +125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* Impedance min. 500 Ω.

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = + 25 °C

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (I^2C interface)	$V_{DD}-V_{SS2}$	2,5	5	6,0	V
Supply voltage (clock[1])	$V_{DD}-V_{SS1}$	1,1	1,5	$(V_{DD}-V_{SS2})$	V
Supply current V_{SS1}					
at $V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	3	10	μA
at $V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
Supply current V_{SS2}					
at $V_{DD}-V_{SS2}$ = 5 V (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs SCL, SDA, A0, A1, TEST					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW	V_{IL}	–	–	0,3 x V_{DD}	V
Input leakage current					
at V_I = V_{SS2} to V_{DD}	$\pm I_I$	–	–	1	μA
Inputs EXTPF, PFIN					
Input voltage HIGH	$V_{IH}-V_{SS1}$	0,7 x $(V_{DD}-V_{SS1})$	–	–	V
Input voltage LOW	$V_{IL}-V_{SS1}$	0	–	0,3 x $(V_{DD}-V_{SS1})$	V
Input leakage current					
at V_I = V_{SS1} to V_{DD}	$\pm I_I$	–	–	1	μA
at T_{amb} = 25 °C; V_I = V_{SS1} to V_{DD}	$\pm I_I$	–	–	0,1	μA
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)					
Output voltage HIGH					
at $V_{DD}-V_{SS2}$ = 2,5 V; $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output voltage LOW					
at $V_{DD}-V_{SS2}$ = 2,5 V; I_O = 0,3 mA	V_{OL}	–	–	0,4	V
at $V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1,6 mA	V_{OL}	–	–	0,4	V

5

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Output SDA (N-channel open drain)					
Output "ON": I_O = 3 mA at $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current) at $V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	I_O	–	–	1	μA
Internal threshold voltage					
Power failure detection	V_{TH1}	1	1,2	1,4	V
Power "ON" reset at $V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals					
Input EXTPF	t_r, t_f	–	–	1	μs
Input PFIN	t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels					
rise time	t_r	–	–	1	μs
fall time	t_f	–	–	0,3	μs
Frequency at SCL at $V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (see Figs 7 and 9)	t_{LOW}	4,7	–	–	μs
Pulse width HIGH (see Figs 7 and 9)	t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA input	T_I	0,25	1	2,5	μs
Input capacitance (SCL, SDA)	C_I	–	–	7	pF
Oscillator					
Integrated oscillator capacitance	C_{out}	–	40	–	pF
Oscillator feedback resistance	R_f	–	3	–	MΩ
Oscillator stability for: $\Delta(V_{DD}-V_{SS1})$ = 100 mV at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	kΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

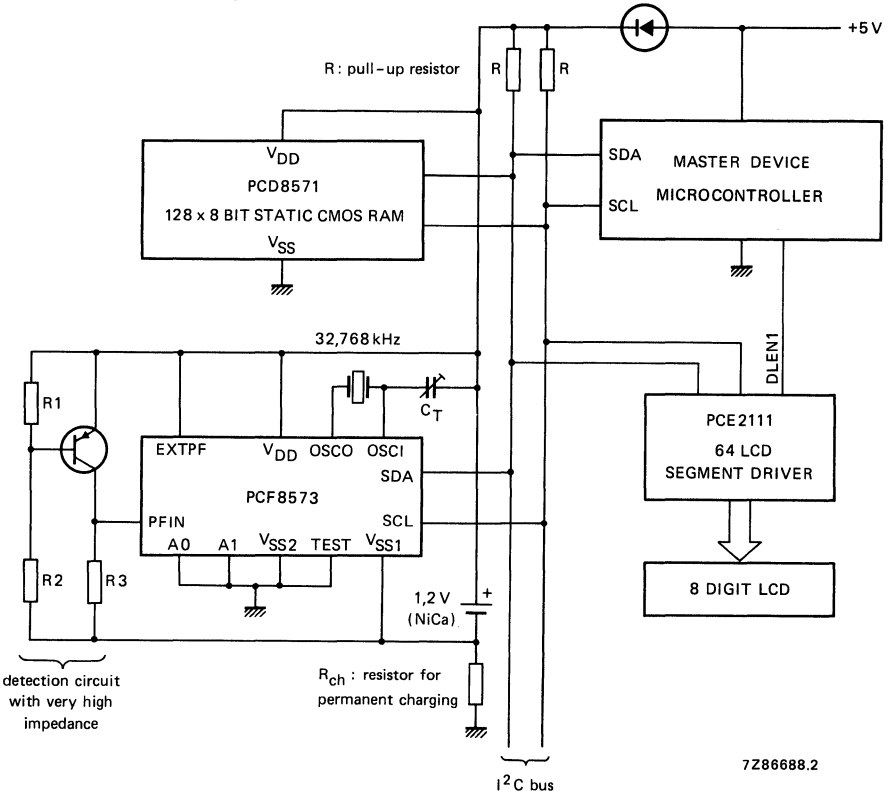


Fig. 15 Application example of the PCF8573 clock/calendar.

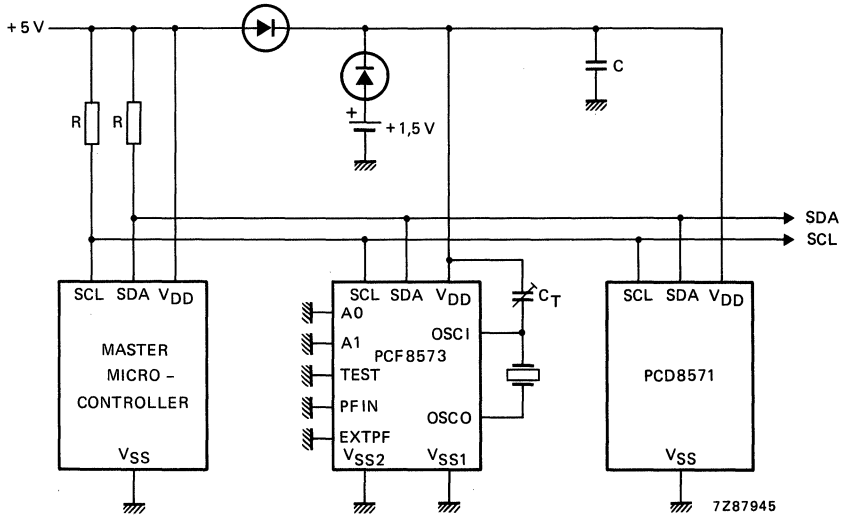


Fig. 16 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

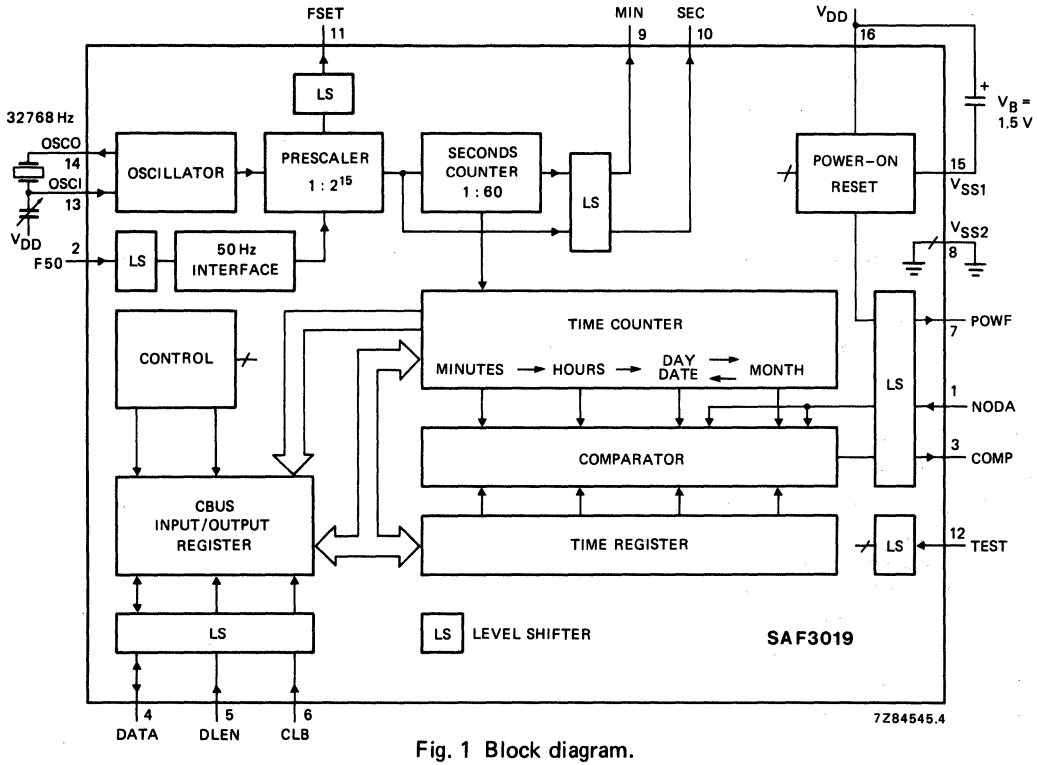


Fig. 1 Block diagram.

5

Features

- serial bidirectional CBUS interface for input/output of minutes, hours, day and month
- additional pulse outputs for seconds and minutes
- time register for presetting a time for alarm or remote switching functions
- battery back-up for clock function during supply interruption
- controlled either by the 50 Hz mains frequency or a crystal oscillator (automatic switch)

QUICK REFERENCE DATA

Supply voltage		V_{DD}	typ.	5 V
Battery supply voltage range	T_{amb} = −40 to + 85 °C	V_B		1.5 to 2.6 V
	T_{amb} = 0 to + 70 °C	V_B		1.3 to 2.6 V
Crystal oscillator frequency		f_{osc}	typ.	32.768 Hz
Alternative input frequency (pin 2)		f_{F50}	typ.	50 Hz
Operating ambient temperature range		T_{amb}		−40 to + 85 °C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38D, DE).

GENERAL DESCRIPTION

The SAF3019 is a C-MOS integrated circuit comprising a digital clock for minutes, hours, day and month, as well as an additional register for resetting minutes, hours, day and month. The time counter provides cycles of 28, 30 or 31 days automatically, depending on the length of the month.

The time reference is the 50 Hz mains frequency or a 32.768 Hz on-chip reference oscillator with an external crystal. If the 50 Hz mains frequency is interrupted, the circuit is automatically switched to crystal oscillator operation.

The circuit can be controlled by a microcomputer. The data transmission (e.g. TIME SET and TIME READ of the time counter and time register) is achieved via the CBUS. A microcomputer then controls the data processing and the display unit drive.

The circuit uses a 5 V supply for data transmission. If this 5 V supply is interrupted, the clock function is maintained by a 1.5 V battery. The clock can then continue to function for an extended period, because the battery load current is only a few μA.

OPERATION DESCRIPTION

Oscillator and prescaler (outputs OSCO, FSET; inputs OSCI, F50)

The 32.768 Hz reference oscillator is achieved by connecting a quartz crystal between the output OSCO and the input OSCI (see also Fig. 7). The oscillator frequency of 32.768 Hz is divided by 256, and again by 128, in a prescaler. This results in a pulse once every second which controls the time counter. The divided-by-256 oscillator frequency (128 Hz) is available at FSET, which is used for fine-adjustment of the oscillator without loading it.

The circuit can also be operated by applying the 50 Hz mains frequency to input F50. This signal is divided-by-50 to obtain a pulse every second to drive the time counter. Input F50 has a Schmitt trigger characteristic which allows slowly rising pulses at this input.

If the mains frequency is interrupted, automatic quartz crystal operation is obtained (see Fig. 8). When the 50 Hz operation is not used, input F50 should be connected to ground (V_{SS2}).

Time counter (outputs SEC, MIN)

The one-second pulses are counted by a (no direct TIME READ) seconds counter and, after 60 seconds, they are transferred to successive counters for minutes, hours, day and month. This counter can be TIME SET and TIME READ by a microcomputer via the CBUS interface. The cycle length for the time counter is given in Table 1.

The seconds and minutes pulses are avilable at output SEC and MIN respectively, with a pulse ratio of 0.5.

The input/output DATA is set LOW at each transfer of seconds to the minutes counter (i.e. each minute), as long as the CBUS is not occupied by a DLEN = HIGH transmission.

DATA will be set HIGH again by a TIME ADDRESS/TIME READ or TIME SET instruction.

Table 1 Cycle lengths of time counter

unit	counting cycle	carry for following unit	content of month counter
minutes	00 59	59 → 00	1 12
hours	00 23	23 → 00	1 12
days	01 28	28 → 01	2
		or 29 → 01*	2
	01 30	30 → 01	4, 6, 9, 11
	01 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	01 12	12 → 01	

* The day counter may be set to 29.2. by a TIME SET instruction (for a leap year), then the month transfer occurs at 1.3.

5

Comparator (output COMP; input NODA)

The time register for a preset switching time (alarm or remote switching) is a 24-bit memory, which can also be set and read-out via the CBUS interface. If both the times of the time counter and the time register are equal, the output COMP becomes HIGH for one minute.

It is possible to choose a comparison between time counter and the time register either based upon minutes, hours, day and month (i.e. clock time *and* date) or minutes and hours (i.e. daily). It is controlled by bit 'UC' and input NODA (see also Table 3) during setting of the month register;

comparison with date: UC = 0 *and* NODA = LOW

comparison daily: UC = 1 *or* NODA = HIGH.

CBUS interface

The data transmission of the SAF3019 to the microcomputer (TIME READ) and vice versa (TIME SET) is possible via the CBUS; DATA (input/output), DLEN (input) and CLB (input).

Data and addresses are transmitted serially via the DATA line, which are synchronized with the clock burst (CLB) pulses from the microcomputer. The duration of the data transmission is determined by the number of CLB pulses when DLEN = HIGH.

The IC includes a word format checking function, which allows the CBUS to be used for controlling other circuits as well. The following word lengths are recognized as valid transmissions:

- TIME ADDRESS (3-bits and 1 start bit);
- TIME SET (10-bits and 1 start bit).

A TIME ADDRESS instruction always has to be followed by a TIME READ (7-bits) sequence. A TIME SET instruction combines address and data. With each instruction (each TIME ADDRESS and TIME READ instruction cycle) two digits of the time counter and time register can be set. The result is, that for a complete TIME READ and TIME SET transmission, 4 cycles TIME ADDRESS/TIME READ or 4 TIME SET instructions are needed.

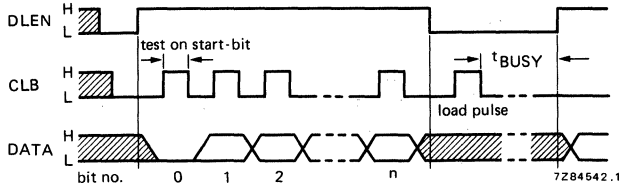


Fig. 2 CBUS data transmission.

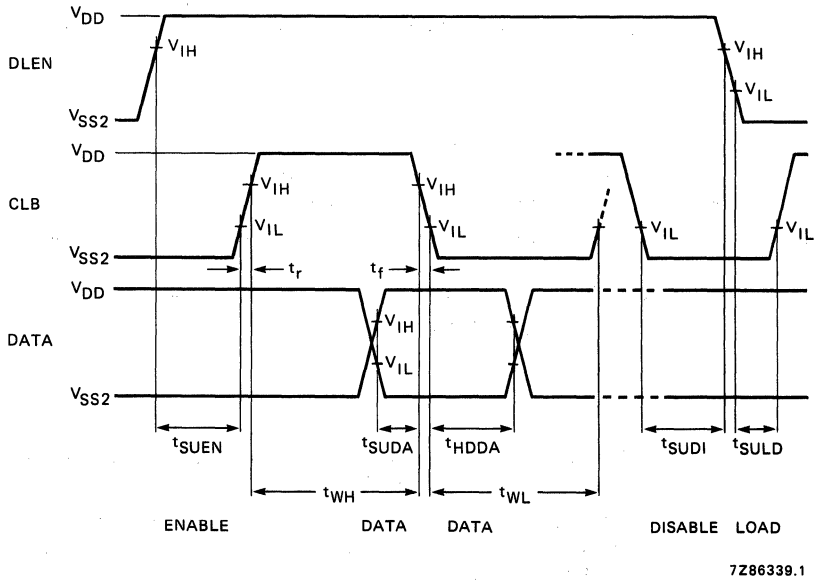


Fig. 3 CBUS timing.

TIME READ

First the bits S, A0 and A1 are transferred from the microcomputer to the SAF3019 with the TIME ADDRESS instruction. With the next instruction (TIME READ), the contents of the selected digits are transferred from the SAF3019 to the microcomputer.

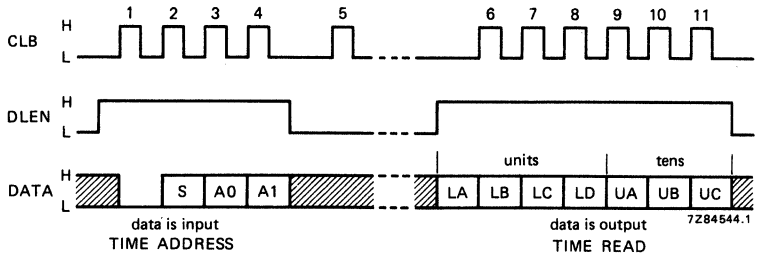


Fig. 4 TIME ADDRESS/TIME READ cycle.

Table 2 Selected digits with respect to the address bits and the TIME READ instruction function.

S	A0	A1	LA	LB	LC	LD	UA	UB	UC	instruction	
0	1	1	D	D	D	D	D	D	D	minutes	time read counter
0	0	1	D	D	D	D	D	D	0	hours	
0	1	0	D	D	D	D	D	D	0	date	
0	0	0	D	D	D	D	D	0	0	month	
1	1	1	D	D	D	D	D	D	D	minutes	time read register
1	0	1	D	D	D	D	D	D	0	hours	
1	1	0	D	D	D	D	D	D	0	date	
1	0	0	D	D	D	D	D	0	0	month	

D = data bit.

TIME SET

The TIME SET instruction transfers the address bits S, A0 and A1 as well as the selected digits of the BCD-coded incoming data from the microcomputer to the SAF3019. The last bit (UC) can control special functions. A TIME SET instruction will not stop the time counter, and also will not generate a non-selected digit for transmission.

The prescaler and seconds counter are reset with the TIME SET instruction when S = 0, A0 = 0, A1 = 0 (addressed for month) and UC = 0. If the seconds counter is between 30 and 59, this instruction generates a transfer for the minutes counter. Therefore, this instruction may be used for a very simple correction of the time counter if the deviation is within ±30 seconds.

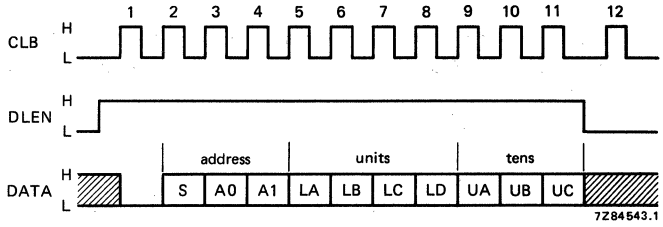


Fig. 5 Data format for TIME SET instruction.

Table 3 Selected digits with respect to the address bits and the possible TIME SET instruction function.

S	A0	A1	LA	LB	LC	LD	UA	UB	UC	instruction	
0	1	1	D	D	D	D	D	D	D	minutes	time set counter
0	0	1	D	D	D	D	D	D	X	hours	
0	1	0	D	D	D	D	D	D	X	date	
0	0	0	D	D	D	D	D	X	1	month	
0	0	0	X	X	X	X	X	X	0	seconds	reset counter
1	1	1	D	D	D	D	D	D	D	minutes	time set register
1	0	1	D	D	D	D	D	D	X	hours	
1	1	0	D	D	D	D	D	D	X	date	
1	0	0	D	D	D	D	D	X	0	month*	
1	0	0	D	D	D	D	D	X	1	month**	

D = data bit; X = 1 or 0.

* Compare *with* date. ** Compare *without* date.

Level shifters

The circuit has been designed for low-voltage operation. However, to interface with the microcomputer, most inputs and outputs have level shifters to operate with the 5 V supply voltage of the microcomputer. These level shifters only function when the 5 V supply (V_{DD}) is available. The internal clock function is independent of this supply.

Power failure (output POWF)

If the supply voltage V_{DD}-V_{SS1} is below a certain internal value (V_{POWF}), the power-failure output (POWF) is set HIGH. The threshold voltage V_{POWF} is lower than the minimum battery voltage V_{DD}-V_{SS1}. This battery is required as back-up for the logic circuitry. It is impossible to have data transmission via the CBUS when V_{DD}-$V_{SS1} < V_{POWF}$, however, the clock will continue running as long as V_{DD}-V_{SS1} does not drop to a lower value. The CBUS is released directly when V_{DD}-V_{SS1} becomes larger than V_{POWF}, but POWF stays HIGH until the next TIME SET instruction, which sets POWF LOW again.

N.B. The 5 V supply voltage (V_{DD}-V_{SS2}) must be switched off when exchanging the battery.

TEST input

The TEST input is used for testing purposes and it is connected to ground (V_{SS2}) for normal operation.

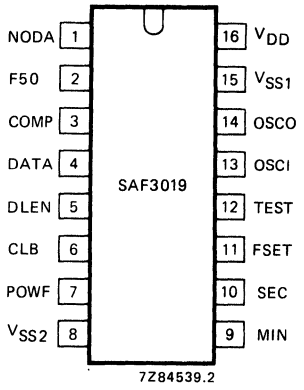


Fig. 6 Pinning diagram.

PINNING

16	V_{DD}	common positive supply (5 V; V_B = 1.5 V)
15	V_{SS1}	negative battery supply (V_B)
8	V_{SS2}	ground (V_{DD})
4	DATA	data input/output } CBUS (bidirectional)
5	DLEN	data line enable input } CBUS (bidirectional)
6	CLB	clock burst input } CBUS (bidirectional)
1	NODA	comparator mode select input
12	TEST	test mode input (normally ground)
2	F50	50 Hz mains frequency input
13	OSCI	input and output of the on-chip oscillator
14	OSCO	input and output of the on-chip oscillator
10	SEC	1 pulse per second output
9	MIN	1 pulse per minute output
3	COMP	comparator output
7	POWF	power failure output
11	FSET	frequency setting signal output (128 Hz)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges	$V_{DD} - V_{SS1}$		−0.5 to + 8 V
	$V_{DD} - V_{SS2}$		−0.5 to + 8 V
Voltage on any pin (except OSCI, OSCO)	V_I	V_{SS2}	−0.6 to V_{DD} + 0.6 V
Voltage on pins OSCI, OSCO	V_I	V_{SS1}	−0.6 to V_{DD} + 0.6 V
Input currents	$\|I_I\|$	max.	10 mA
Output currents	$\|I_O\|$	max.	10 mA
Power dissipation per output	P_O	max.	100 mW
Total power dissipation per package	P_{tot}	max.	200 mW
Operating ambient temperature range	T_{amb}		−40 to + 85 °C
Storage temperature range	T_{stg}		−65 to + 150 °C

D.C. CHARACTERISTICS

V_{SS2} = 0 V; V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	with respect to V_{SS2}*	V_{DD}	4.5	5	5.5	V
Battery voltage	between V_{DD} and V_{SS1}	V_B	1.5	–	2.6	V
	at T_{AMB} = 0 to 70 °C	V_B	1.3	–	2.6	V
Time keeping battery voltage		V_{BO}	1.3	–	2.6	V
Supply current	I_O = 0 mA**	$-I_{SS2}$	–	–	50	μA
Battery current	V_B = 1.5 V	$-I_{SS1}$	–	–	10	μA
Inputs DLEN, DATA, CLB, F50, NODA						
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input current at $V_I = V_{SS2}$ or V_{DD}	V_{DD} = 5.5 V	$\|I_I\|$	–	–	1	μA
Input F50 hysteresis	$\Delta V = V_{IH} - V_{IL}$	ΔV	0.2	–	–	V
Outputs SEC, MIN, COMP, POWF (buffer outputs)						
Output voltage HIGH	$-I_O$ = 0.5 mA	V_{OH}	V_{DD} − 0.4	–	–	V
Output voltage LOW	I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Output DATA (N-channel open drain)						
Output voltage LOW	I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Output leakage current	V_O = 5.5 V (HIGH)	I_{OR}	–	–	1	μA

* All outputs are available down to $V_{SS2} = V_B$ at reduced current capability.

** $V_I = V_{SS2}$ or $V_I = V_{DD}$ at all inputs; quartz crystal oscillator operation:
f = 32 768 Hz, series resistance of crystal $R_{s\,max}$ = 25 kΩ (40 kΩ for 0 to + 70 °C), C_L = 10 pF.

A.C. CHARACTERISTICS

V_{SS2} = 0 V; V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

See Figs 2 and 3 for all timing.

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs DLEN, DATA, CLB, NODA						
Rise and fall times	note 1	t_r, t_f	–	–	1	μs
CLB pulse width HIGH		t_{WH}	4	–	∞	μs
CLB pulse width LOW		t_{WL}	4	–	∞	μs
Data set-up time DATA → CLB		t_{SUDA}	1	–	–	μs
Data hold time DATA → CLB		t_{HDDA}	2	–	–	μs
Enable set-up time DLEN → CLB		t_{SUEN}	2	–	–	μs
Disable set-up time CLB → DLEN		t_{SUDI}	2	–	–	μs
Set-up time DLEN → CLB (load pulse)		t_{SULD}	1	–	–	μs
Busy-time from load pulse to next start of transmission		t_{BUSY}	2	–	–	μs
CLB frequency		f_{CLB}	0	–	100	kHz
Input F50						
Rise and fall times	notes 1 and 2	t_r, t_f	–	–	10	ms
Pulse width HIGH		t_{WH}	30	–	–	μs
Pulse width LOW		t_{WL}	30	–	–	μs
Oscillator (OSCI, OSCO)						
Series resistance of crystal	f = 32.768 Hz at T_{amb} =	R_s	–	–	25	kΩ
	0 to 70 °C	R_s	–	–	40	kΩ
Load capacitance		C_L	–	10	–	pF

Notes

1. All timing values are referred to V_{IH} and V_{IL} within a voltage swing of minimum V_{SS2} to V_{DD}.
2. The supply current I_{SS2} increases at slow rise/fall times.

5

APPLICATION INFORMATION

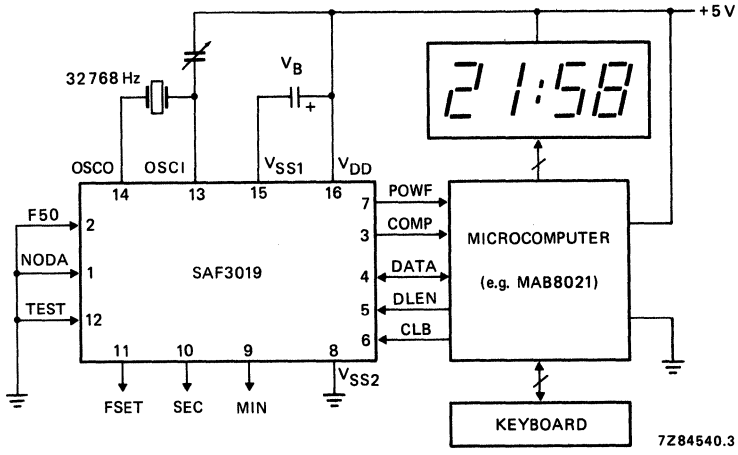


Fig. 7 Typical application of the SAF3019 in a microcomputer controlled system.

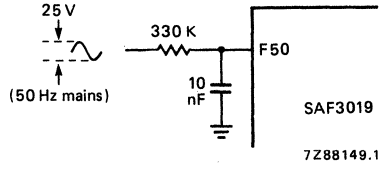


Fig. 8 Circuitry for applying the 50 Hz mains to input F50.

GENERAL DESCRIPTION

The SAA7000 interpolation and muting circuit descrambles and separates data into left and right channels and minimizes the effects of erroneous data on the performance of the Compact Disc Digital Audio System. Minor errors (those present in one data sample only) are replaced with audio data obtained by interpolation; more persistent errors are removed by muting.

Features

- Descrambles data from error corrector SAA7020 and formats into left and right channels
- Minimizes the effect of erroneous data samples
- 16-bit serial data input (two's complement)
- Smoothed transitions before and after muting
- Interpolated data replaces single erroneous data samples
- Serial output for digital-to-analogue converters (DACs) or filter circuits
- Generates crystal-derived timing signals for system master data clock (4,2336 MHz), serving error corrector SAA7020 and digital filter SAA7030
- Selectable output format: offset binary or two's complement; 14 or 16-bit word

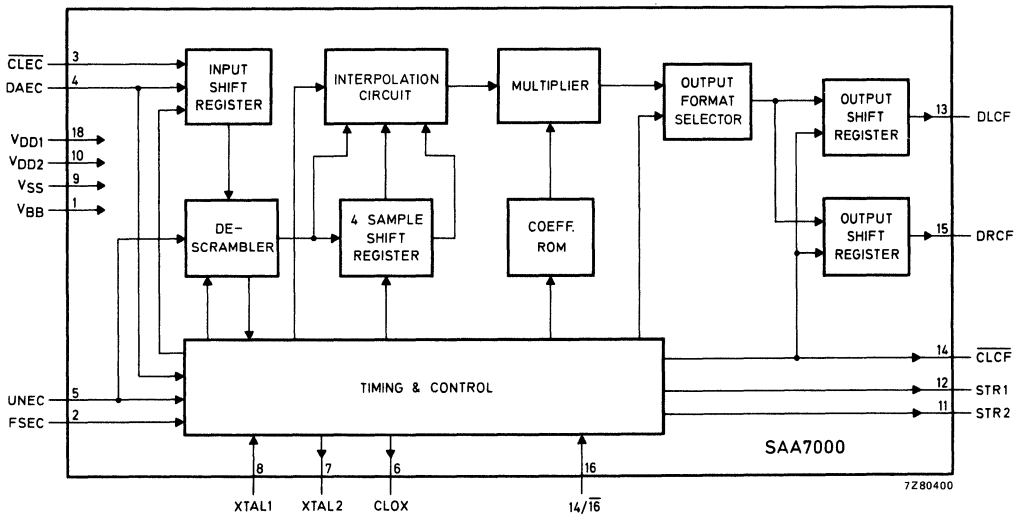


Fig. 1 Block diagram.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

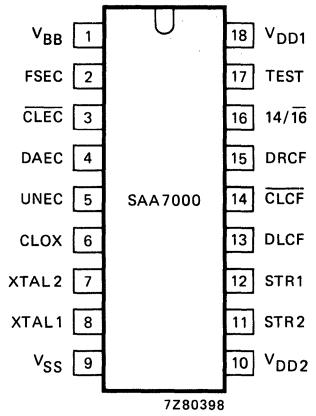


Fig. 2 Pinning diagram.

PINNING

1	V_{BB}	back bias supply
2	FSEC	frame sync pulse input
3	$\overline{CLEC}$	input data clock
4	DAEC	data input (two's complement) and output format selector
5	UNEC	error flag input
6	CLOX	buffered clock output (XTAL1)
7	XTAL2	drive output to clock crystal
8	XTAL1	external clock input
9	V_{SS}	ground
10	V_{DD2}	+ 12 V supply
11	STR2	strobe 2 output
12	STR1	strobe 1 output
13	DLCF	left channel data output (format selected by DAEC)
14	$\overline{CLCF}$	14/16-bit clock burst output
15	DRCF	right channel data output (format selected by DAEC)
16	14/$\overline{16}$	selects bit length of clock burst output from $\overline{CLCF}$
17	TEST	test input
18	V_{DD1}	+ 5 V supply

FUNCTIONAL DESCRIPTION

The SAA7000 is used in the Compact Disc system to reconstruct audio data by interpolation if the error corrector SAA7020 is unable to correct a data sample, or mutes the data when it passes consecutive erroneous data samples. Errors are indicated by an error flag (UNEC) from the SAA7020; when no error flag occurs, the data value through SAA7000 is unaffected.

Data samples (at DAEC, clocked in by $\overline{CLEC}$) are first descrambled and then separated into left and right channels. A similar descramble and separation is performed on the error flag (UNEC).

If, for either left or right channels, a single 'error' is flagged between two 'good' data samples then linear interpolation is used to replace the erroneous value. If two or more adjacent samples are flagged, then the samples in error are muted. Beginning thirty samples before the first of the consecutive errors, the data value of the samples is attenuated smoothly to zero following a (0 to π) cosine curve. After the error burst, the next thirty samples are smoothly returned to full level following a (π to 2π) cosine curve. The muting is applied simultaneously to data in both left and right channels regardless of the source of the error.

The data (good or processed) is formatted into two's complement or offset binary to match the DACs in use. This selection is made with a special function of the data input (DAEC, see Fig. 6). The data is then fed to the left and right outputs (DLCF and DRCF) and is clocked out by the output clock ($\overline{CLCF}$). Strobes (STR1 and STR2) are generated for the DACs and the digital filter (SAA7030). Fourteen or sixteen-bit DACs can be accommodated by the use of the select input (14/$\overline{16}$).

The SAA7000 automatically synchronizes to the error detector SAA7020 output using the frame sync pulse (FSEC) for internal timing reset and feeds a 2 x bit-rate clock (CLOX) to the system.

Pin functions

pin no.	mnemonic	description
1	V_{BB}	Back bias supply voltage: −2,5 V ± 20%.
2	FSEC	Frame sync pulse (active HIGH) received from SAA7020 at the start of a data frame (12 data samples). FSEC is used to synchronize the descrambler to the data frames. For re-synchronization to occur, two consecutive FSEC pulses must be received each having a pulse width of approximately 6 CLOX cycles and the leading edge of the second pulse must be one data frame later than that of the first. FSEC is also used to synchronize the internal clock to the $\overline{\text{CLEC}}$ clock input, so aligning the gap in the internal clock to the FSEC pulse (see Fig. 4).
3	$\overline{\text{CLEC}}$	Input data clock used to load serial data at DAEC into the input shift register. After a data sample has been loaded $\overline{\text{CLEC}}$ is held LOW to give a gap of 16 CLOX cycles (see Fig. 4). The period of the $\overline{\text{CLEC}}$ clock is 2 x the period of a CLOX cycle.
4	DAEC	Serial data samples are received at DAEC in two's complement form. The data is in 16-bit words separated by gaps; each word comprising two 8-bit symbols. The DAEC input is also used to select the output format; during the $\overline{\text{CLEC}}$ gap, a HIGH level at DAEC selects two's complement and a LOW level selects offset binary format (see Fig. 4).
5	UNEC	Error flag indicating unreliable data from SAA7020. During the period when data is clocked in at DAEC, UNEC is LOW only if the present 8-bit symbol is valid. During the period of the $\overline{\text{CLEC}}$ gap, UNEC is LOW only if the whole of the data word due to arrive 5 frames later is valid.
6	CLOX	Buffered XTAL1 clock output.
7	XTAL2	Main clock crystal drive output. This pin should remain disconnected if a crystal is not used.
8	XTAL1	Clock input from crystal circuit or for externally derived clock.
9	V_{SS}	Ground (0 V).
10	V_{DD2}	Positive supply voltage: + 12 V ± 10%.
11	STR2	Active HIGH strobe pulse of 2 CLOX cycles duration occurring every 24 CLOX cycles and used to strobe data to the DACs. This pin should be left disconnected if SAA7030 is not used.
12	STR1	Active HIGH strobe pulse of 2 CLOX cycles duration occurring every 96 CLOX cycles – after each pair of data words have been clocked out. It is used to strobe data to SAA7030, or to the DACs if SAA7030 is not used. Both STR1 and STR2 are re-synchronized to XTAL1 to minimize jitter.
13	DLCF	Left channel data output; format in two's complement or offset binary, as selected at DAEC.
14	$\overline{\text{CLCF}}$	Clock burst output of either 14 or 16 bits, as selected at pin 16. It is used to clock data from DLCF and DRCF (data is valid on $\overline{\text{CLCF}}$ falling edge, see Fig. 5).
15	DRCF	Right channel data output; format is two's complement or offset binary, as selected at DAEC.
16	14/$\overline{16}$	Selects 14 or 16-bit bursts of output clock $\overline{\text{CLCF}}$.

5

17	TEST	This pin should be held LOW to ensure normal operation.
18	V_{DD1}	Positive supply voltage: + 5 V ± 10%.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134); V_{SS} = 0 V

Supply voltage 1 range (pin 18)	V_{DD1}	−0,3 to + 7,5	V
Supply voltage 2 range (pin 10)	V_{DD2}	−0,3 to + 15	V
Back bias supply voltage range (pin 1)	V_{BB}	−4 to + 0,3	V
Input voltage range	V_I	−0,3 to + 7,5	V
Output voltage range at V_I = −0,3 to + 6,5 V; T_{amb} = 25 °C	V_O	−0,3 to + 7,5	V
Output current	I_O	max. 10	mA
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 125	°C

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage 1 (pin 18)	V_{DD1}	4,5	5,0	5,5	V
Supply voltage 2 (pin 10)	V_{DD2}	10,8	12,0	13,2	V
Back bias supply voltage (pin 1)	$-V_{BB}$	2,0	2,5	3,0	V
Supply current 1 (pin 18)	I_{DD1}	30	70	140	mA
Supply current 2 (pin 10)	I_{DD2}	2	5	10	mA
Back bias supply current (pin 1)	$-I_{BB}$	–	–	500	μA
Inputs (except V_{BB})					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,4	–	6,5	V
Input current (note 1)	I_I	−1	–	+ 1	μA
Input capacitance (not XTAL1)	C_I	–	–	7	pF
Outputs DLCF, DRCF, $\overline{\text{CLCF}}$, CLOX, STR1, STR2 (note 2)					
Output voltage LOW at $-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at I_{OH} = 0,2 mA	V_{OH}	3,0	–	V_{DD1} + 0,5	V
Load capacitance	C_L	–	–	150	pF
Output XTAL2					
Operating frequency using crystal oscillator (Fig. 3)	f_{XTAL}	3,0	4,2336	4,5	MHz
Operating frequency using driven input applied to XTAL1	f_{IN}	3,0	4,2336	4,5	MHz
Input XTAL1					
Input clock LOW	t_{IXL}	40	–	–	% of period
Input clock HIGH	t_{IXH}	40	–	–	% of period
Crystal amplifier (pins 7 and 8)					
Mutual conductance at 5 MHz	gm	1,5	–	–	mA/V
Bandwidth of mutual conductance at minimum 3 dB	B_{gm}	10	–	–	MHz
Input capacitance	C_I	–	–	10	pF
Output capacitance	C_O	–	–	7	pF
Feedback capacitance	C_{FB}	–	–	5	pF
Input leakage current	I_I	−1	–	+ 1	μA
Output current at 5 MHz	I_o	−1	–	+ 1	mA
Small signal gain at 5 MHz	A_V	−4	–	–	

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parameter	symbol	min.	typ.	max.	unit
Inputs DAEC, UNEC, $\overline{\text{CLEC}}$, FSEC					
Input rise time (FSEC only)	t_{IR}	–	–	100	ns
Input fall time (FSEC only)	t_{IF}	–	–	100	ns
$\overline{\text{CLEC}}$ HIGH	t_{ICH}	100	–	–	ns
$\overline{\text{CLEC}}$ LOW	t_{ICL}	100	–	–	ns
DAEC to $\overline{\text{CLEC}}$ set-up time	t_{IDS}	40	–	–	ns
$\overline{\text{CLEC}}$ to DAEC hold time	t_{IDH}	40	–	–	ns
FSEC HIGH (note 3)	t_{FSH}	4 CLOX periods −400	–	8 CLOX periods + 190	ns
DAEC/UNEC to FSEC set-up time	t_{UFS}	0	–	–	ns
FSEC to DAEC/UNEC hold time (note 3)	t_{UFH}	8 CLOX periods + 325	–	–	ns
Output CLOX (notes 4 and 5)					
Output clock LOW	t_{OXL}	30	–	–	% of period
Output clock HIGH	t_{OXH}	30	–	–	% of period
output clock rise time	t_{OXR}	–	–	50	ns
Output clock fall time	t_{OXF}	–	–	40	ns
Outputs STR1, STR2 (note 6)					
Output strobe rise time	t_{OSR}	–	10	20	ns
Output strobe fall time	t_{OSF}	–	6	20	ns
Output strobe HIGH	t_{OSH}	1 CLOX period + 50	2 CLOX periods −20	4 CLOX periods	ns
Output strobe LOW	t_{OSL}	10	–	–	CLOX periods
CLOX to STR1, STR2 delay time	t_{XSL}	0	–	–	ns
	t_{XSH}	–	–	45	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs $\overline{CLCF}$, DLCF, DRCF (note 4)					
Output rise time	t_{OR}	–	–	50	ns
Output fall time	t_{OF}	–	–	40	ns
Output data clock HIGH	t_{OCH}	120	–	–	ns
Output data clock LOW	t_{OCL}	120	–	–	ns
DLCF, DRCF to $\overline{CLCF}$ set-up time	t_{ODS}	50	–	–	ns
$\overline{CLCF}$ to DLCF, DRCF hold time	t_{ODH}	100	–	–	ns
$\overline{CLCF}$ LOW prior to STR1 (note 3)	t_{CSL}	52	60	–	CLOX periods

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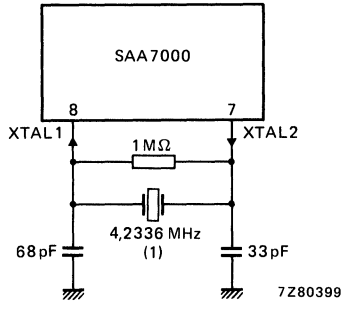
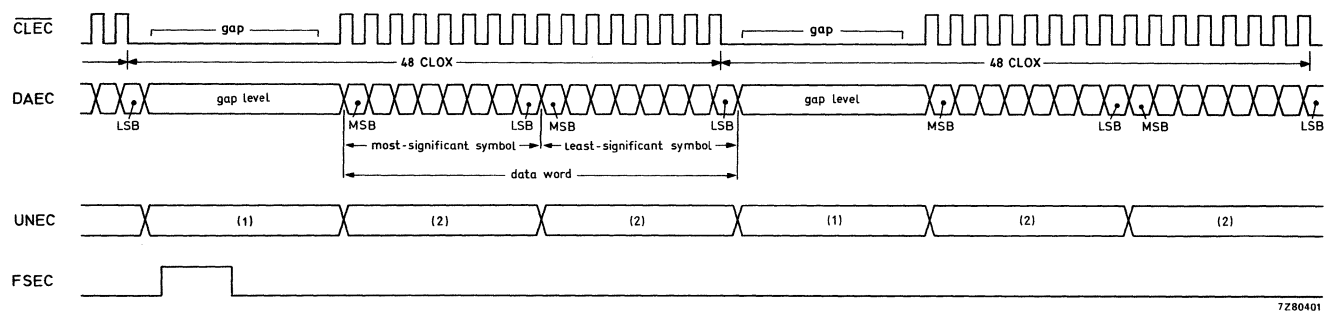
NOTES TO THE CHARACTERISTICS

1. $V_I = -0,3$ to $+ 6,5$ V; $T_{amb} = 25\ ^oC$.
2. All outputs, except XTAL2, are short-circuit protected to V_{DD1} and V_{SS}. Output XTAL2 is protected to V_{SS} only.
3. Input timings assume that CLOX output (pin 6) is used to drive SAA7020 CLOX input. $\overline{CLEC}$ period is twice the CLOX period.
4. Output load capacitance is 50 pF.
5. XTAL1 (pin 8) is driven by an external clock.
6. Output load capacitance is 30 pF on STR1, STR2 outputs.



(1) Catalogue number of crystal is 6416 009 00111.

Fig. 3 Crystal oscillator circuit.



(1) When HIGH indicates unreliability of data word that will follow five frames later.
(2) When HIGH indicates unreliability of current symbol.

Fig. 4 Typical input waveforms.

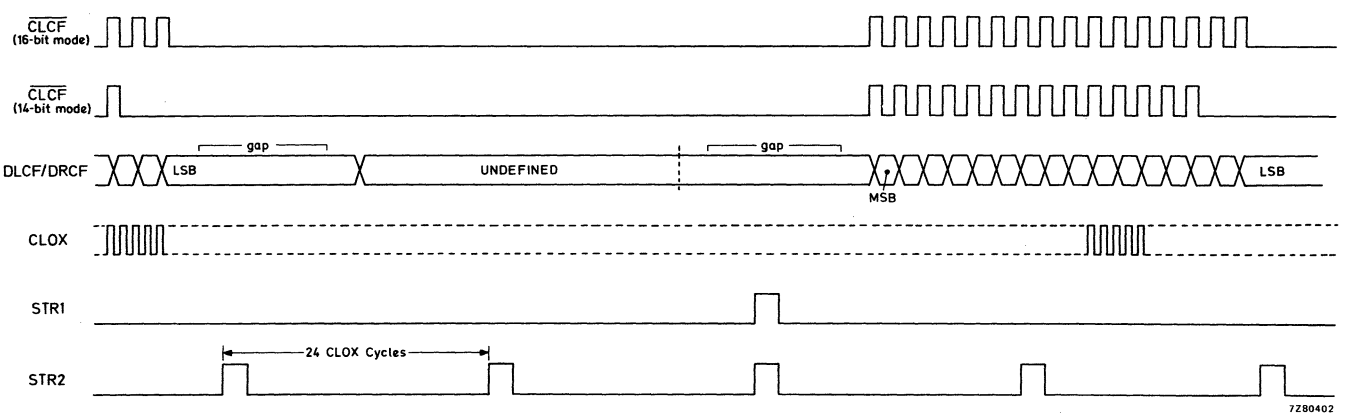
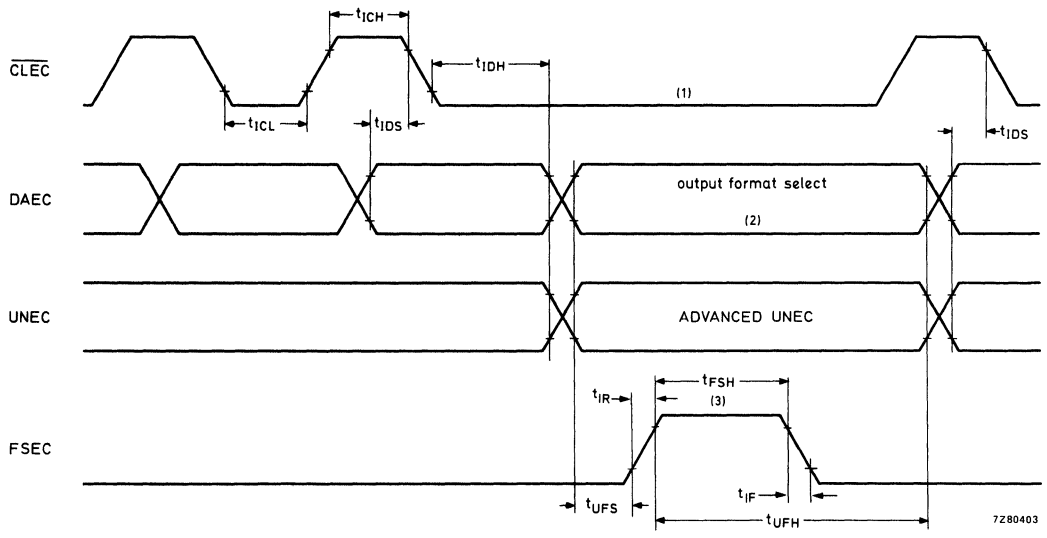


Fig. 5 Typical output waveforms.



(1) $\overline{CLEC}$ remains LOW for a minimum period of approximately 16 CLOX periods.

(2) Data during this time is used to determine the format of the output from SAA7000; when DAEC is HIGH a two's complement format is selected, when LOW an offset binary format is selected.

(3) Input timings assume that CLOX output (pin 6) is used to drive SAA7020 CLOX input. $\overline{CLEC}$ period is twice the CLOX period.

Fig. 6 Input waveforms. Reference levels are 0,8 V and 2,4 V; t_{IR} and t_{IF} apply to FSEC waveform only.

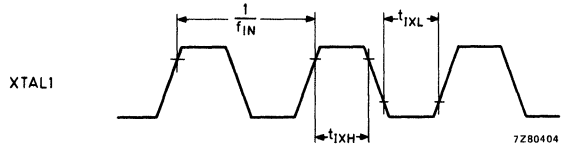


Fig. 7 Optional clock input waveform at XTAL1 (pin 8).

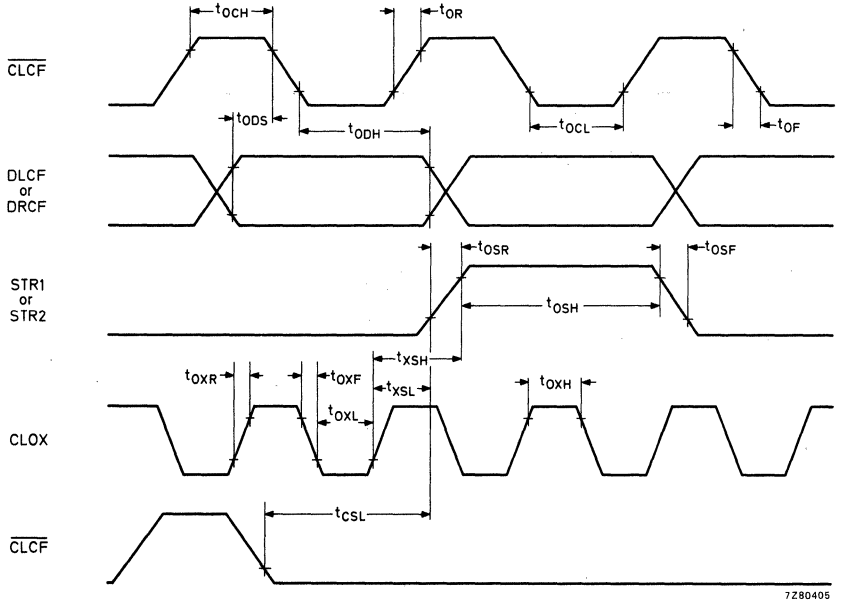


Fig. 8 Output waveforms. Reference levels are 0,8 V and 2,4 V. Output loadings on STR1 and STR2 are 30 pF; output loadings on CLOX, $\overline{CLCF}$, DLCF and DRCF are 50 pF.

Demodulator for Compact Disc SAA7010

GENERAL DESCRIPTION

The SAA7010 demodulates and decodes the pulse code modulated input signal into digital data for the Compact Disc Digital Audio system. A 4,3 MHz (typical) clock locked to the disc rate is also produced.

Features

- Phase-locked loop clock regenerator with frequency detector for locking
- High-frequency level detector with adaptive slicer for input data
- Built-in drop-out detector to prevent error propagation in adaptive slicer
- Outputs to subcoding microprocessor
- Fully protected timing synchronization to incoming data

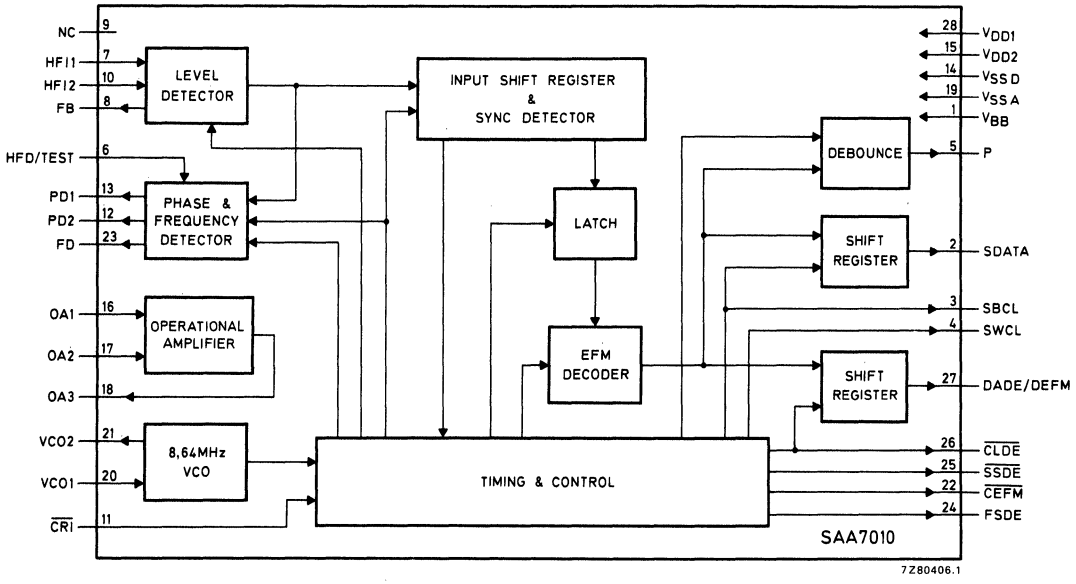


Fig. 1 Block diagram.

PACKAGE OUTLINE

28-lead DIL; package (SOT-117).

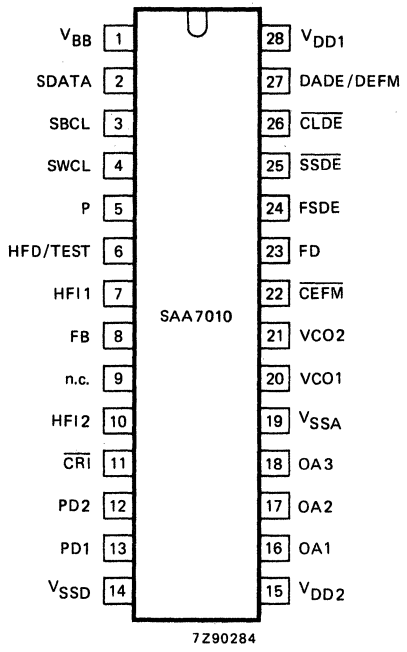


Fig. 2 Pinning diagram.

PINNING

1	V_{BB}	back bias supply
2	SDATA	subcoding data output
3	SBCL	subcoding bit clock output
4	SWCL	subcoding word clock output
5	P	subcoding pause bit output
6	HFD/TEST	high-frequency detector input in normal operation. Selects test mode when at V_{DD2}
7	HFI1	level detector input
8	FB	current feedback from level detector
9	n.c.	not connected
10	HFI2	alternative input to level detector
11	$\overline{CRI}$	counter reset inhibit input
12	PD2	phase detector reference output
13	PD1	phase detector signal output
14	V_{SSD}	digital ground
15	V_{DD2}	+ 12 V supply
16	OA1	operational amplifier non-inverting input
17	OA2	operational amplifier inverting input
18	OA3	operational amplifier source-follower output
19	V_{SSA}	analogue ground
20	VCO1	voltage-controlled oscillator amplifier input
21	VCO2	voltage-controlled oscillator amplifier output
22	$\overline{CEFM}$	4,3218 MHz clock output
23	FD	frequency detector output
24	FSDE	frame sync signal output
25	$\overline{SSDE}$	symbol sync signal output
26	$\overline{CLDE}$	data bit clock output
27	DADE/DEFM	serial data output/EFM digital output: selection determined by level at pin 11
28	V_{DD1}	+ 5 V supply

FUNCTIONAL DESCRIPTION

The SAA7010 demodulator forms the front-end of the Compact Disc Digital Audio system, supplying demodulated data and timing signals to the error corrector (SAA7020) and to the subcoding microprocessor.

The detected signal from the disc is amplified and filtered externally and then converted to a digital signal via the level detector. The level detector is an adaptive data slicer which relies on the nature of the modulation system to determine the optimum slicing level.

A frequency detector and a phase detector provide the coarse and fine control signals for the phase-locked loop (PLL) system. The loop gain is supplied by an internal operational amplifier which drives a voltage-controlled oscillator (VCO) running at twice the input data rate (typically 8,6436 MHz). The VCO output is divided by two by a clock generator in the timing and control circuits and the resulting output is used to clock the input shift register and the timing chain. This clock signal completes the PLL loop when it is compared with the incoming data in the phase detector.

After phase detection the data is clocked into the 23-bit input shift register which then detects the frame sync pattern. Within the timing and control circuits are minimum and maximum data length detectors which provide frequency limit signals for the frequency detector.

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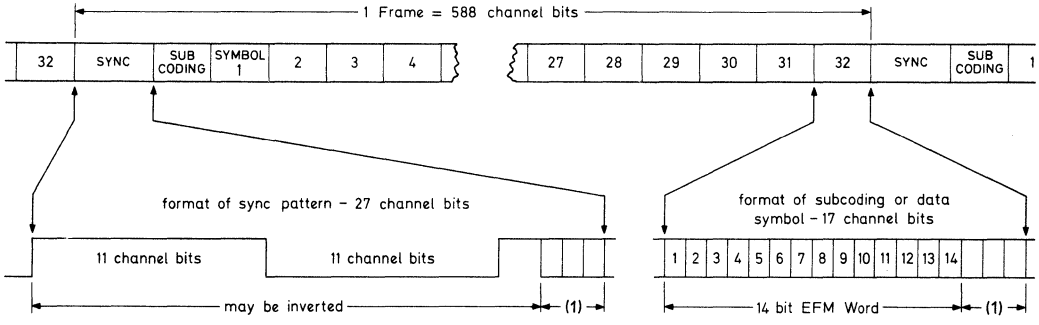
Also within the timing and control circuits are two divide-by-588 counters, one master and one slave, two divide-by-17 symbol rate counters and a lock indication counter. The frame sync signal is used to reset the divide-by-588 slave counter. This counter and one divide-by-17 symbol rate counter supply timing signals for clocking the EFM (eight-to-fourteen modulation) decoder and the subcoding output circuits. The data is read from the input shift register in 14-bit symbols which are first latched and then decoded into 8-bit data words. The subcoding part of the data consists of one word per frame (Fig. 3), so the output SDATA comprises a burst of 8 data bits accompanied by a 2,1906 MHz clock burst signal SBCL (Fig. 4). One bit of this subcoding output data is replaced by a subcoding frame sync bit which is decoded from one of two special EFM codes. The displaced bit (the pause (P) bit) is latched to its own output via a debounce circuit to remove erroneous changes.

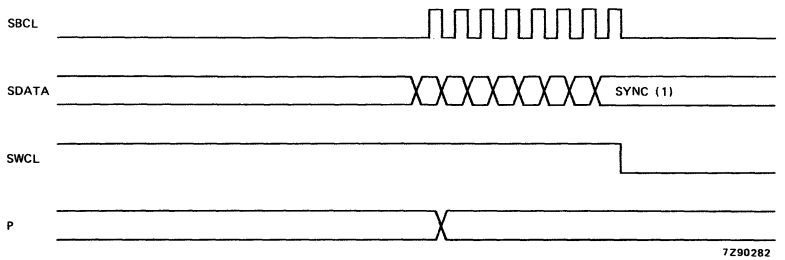
The divide-by-588 slave counter also provides a sync coincidence pulse which occurs when two detected sync pulses are precisely one frame apart (588 clock cycles). The sync coincidence pulse is used to reset the lock indication counter and disable the FD output from the frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.



(1) Merging and low frequency suppression bits.

Fig. 3 Data input signal.

FUNCTIONAL DESCRIPTION (continued)



(1) The sync bit is LOW when a subcoding sync word is detected.

Fig. 4 Typical subcoding waveform outputs.

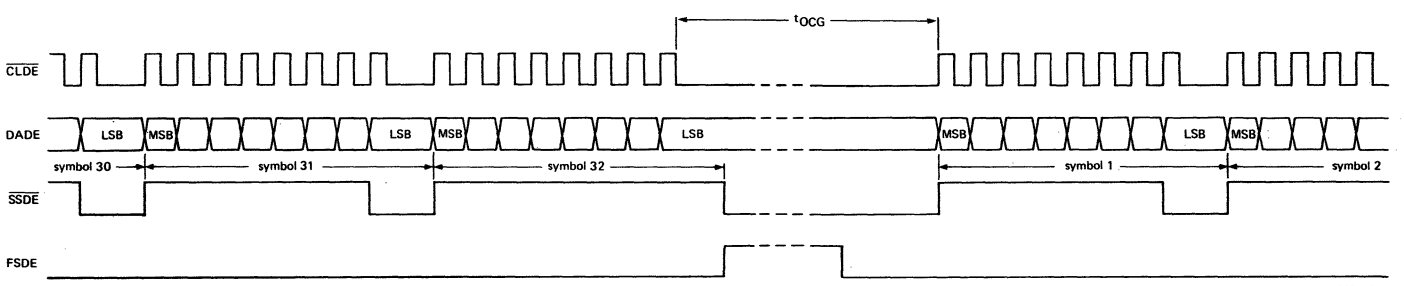


Fig. 5 Typical waveform outputs to SAA7020.

FUNCTIONAL DESCRIPTION (continued)

A delayed version of the sync coincidence pulse resets the divide-by-588 master counter. This counter is reset only by coincident sync pulses or sync pulses which occur during a predetermined 'window' at the start of each frame and is therefore protected from accidental reset by erroneous sync patterns. The window is wide enough to allow PLL bit-slips but narrow enough to avoid false sync signals generated by corrupt data. The divide-by-588 master counter may be allowed to free-run by taking $\overline{CRI}$ input (pin 11) LOW to inhibit the reset signal.

The divide-by-588 master counter and the second divide-by-17 symbol rate counter are used to time the data and clock outputs to the error corrector SAA7020 (Fig. 5). In this way, even if the data has been corrupted, the timing signals will be correct and are only re-synchronized after a complete frame has been sent to SAA7020.

The data output to SAA7020 comprises thirty-two 8-bit symbols per frame, with half-bit gaps between each symbol and a much longer gap during the frame sync period. It is this longer gap that changes in length when corrupt data upsets the timing system.

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Pin functions

pin no.	mnemonic	description
1	V_{BB}	Back bias supply voltage: −2,5 V ± 20%.
2	SDATA	Subcoding data push-pull output. An 8-bit burst of data (including a 1-bit subcoding frame sync) is output serially once per frame coincident with SBCL.
3	SBCL	Subcoding bit clock push-pull output. An 8-bit burst clock, typically at 2,1609 MHz, is used to synchronize the subcoding data.
4	SWCL	Subcoding word clock push-pull output. A square-wave signal at data frame rate (7,35 kHz) used to synchronize the subcoding words and the pause (P) bit.
5	P	Subcoding pause bit push-pull output. This signal is derived from the encoded subcoding word and is used to indicate a music pause. A debounce circuit is incorporated to eliminate erroneous data.
6	HFD/TEST	External high-frequency detector input. When this signal is HIGH the frequency detector output (FD) and phase detector are enabled. When pin 6 is connected to V_{DD2}, the device enters TEST mode.
7	HFI1	Level detector input. A signal of between 0,25 and 2,5 V (peak-to-peak value) is required to drive the level detector correctly.
8	FB	Current feedback from the level detector.
9	n.c.	Not connected.
10	HFI2	Alternative input to the level detector.
11	$\overline{CRI}$	Counter reset inhibit signal input. When LOW, this signal allows the divide-by-588 master counter to free-run and causes pin 27 output to be converted to DEFM. During power-up, pin 11 should be held HIGH for 10 ms.
12	PD2	Phase detector reference signal, maximum impedance 10 kΩ.
13	PD1	Phase detector output signal, maximum impedance 10 kΩ. The differential d.c. content of PD1 and PD2 signals is a measure of the phase difference between the data and the internal 4,3218 MHz clock.

pin no.	mnemonic	description
14	V_{SSD}	Digital ground. Main ground terminal.
15	V_{DD2}	Positive supply voltage: + 12 V ± 10%.
16	OA1	Operational amplifier non-inverting input.
17	OA2	Operational amplifier inverting input.
18	OA3	Operational amplifier source follower output.
19	V_{SSA}	Analogue ground. Ground terminal for operational amplifier and VCO only. Connected internally to V_{SSD} via a 25 Ω (nominal) resistor.
20	VCO1	Voltage-controlled oscillator amplifier input. The amplifier is a simple inverter operating up to 10 MHz. Frequency control is achieved via an external tuned circuit using variable capacitance diodes.
21	VCO2	Voltage-controlled oscillator amplifier output. The load for the inverting transistor may be turned off for test purposes by reducing V_{DD2} to 0 V.
22	$\overline{\text{CEFM}}$	Internal 4,3218 MHz clock generator push-pull output.
23	FD	Frequency detector three-state push-pull output. This output has a 1 kΩ (typical) impedance when active but assumes a high impedance state once the system is in lock.
24	FSDE	Frame sync signal push-pull output (to SAA7020). It provides a positive-going pulse at the end of each data frame. Typical frequency = 7,35 kHz.
25	$\overline{\text{SSDE}}$	Symbol sync signal push-pull output for each data symbol. Typical frequency = 254 kHz.
26	$\overline{\text{CLDE}}$	Data bit clock push-pull output (to SAA7020). An 8-bit clock burst at 2,1609 MHz (typical) which is used to synchronize the data to SAA7020 (see Fig. 5).
27	DADE/DEFM	Data push-pull output (to SAA7020). Serial data comprising 32 x 8-bit symbols per frame, synchronized to $\overline{\text{CLDE}}$ (see Fig. 5). This output is converted to DEFM when $\overline{\text{CRI}}$ (pin 11) is LOW. DEFM is the digital signal appearing at the output of the level detector.
28	V_{DD1}	Positive supply voltage: + 5 V ± 10%.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134);
$V_{SSA} = V_{SSD} = 0$ V.

Supply voltage 1 range (pin 28)	V_{DD1}	−0,3 to + 7,5 V
Supply voltage 2 range (pin 15)	V_{DD2}	−0,3 to + 15 V
Back bias supply voltage range (pin 1)	V_{BB}	−4 to + 0,3 V
Input voltage range	V_I	−0,3 to + 7,5 V
Output voltage range (except FD, OA3)	V_O	−0,3 to + 7,5 V
Output voltage range (FD, OA3 only)	V_O	−0,3 to + 15 V
Output current (each output)	I_O	max. 10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

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CHARACTERISTICS

$V_{SSA} = V_{SSD} = 0$ V; $T_{amb} = -20$ to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLIES					
Supply voltage 1 (pin 28)	V_{DD1}	4,5	5,0	5,5	V
Supply voltage 2 (pin 15)	V_{DD2}	10,8	12,0	13,2	V
Back bias supply voltage (pin 1)	$-V_{BB}$	2,0	2,5	3,0	V
Supply current 1 (pin 28)	I_{DD1}	30	60	150	mA
Supply current 2 (pin 15)	I_{DD2}	4	8	21	mA
Back bias supply current (pin 1)	$-I_{BB}$	–	–	500	μA
DIGITAL CIRCUITS					
Input HFD, $\overline{CRI}$					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,4	–	6,5	V
Input current (note 1)	I_I	−1	–	+ 1	μA
Input capacitance	C_I	–	–	7	pF
Outputs DADE/DEFM, $\overline{CLDE}$, FSDE, $\overline{SSDE}$, SBCL, SDATA, P, SWCL, $\overline{CEFM}$ (note 2)					
Output voltage LOW at $-I_{OL} = 1,6$ mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $I_{OH} = 0,2$ mA	V_{OH}	3,0	–	V_{DD1} + 0,5	V
Load capacitance	C_L	–	–	150	pF

parameter	symbol	min.	typ.	max.	unit
DIGITAL CIRCUITS (continued)					
Output FD					
Output voltage LOW at $-I_{OL}$ = 100 μA	V_{OL}	0	–	0,5	V
Output voltage HIGH at I_{OH} = 100 μA	V_{OH}	8,0	–	V_{DD2} + 0,5	V
Output leakage current at V_O = 0 to 6 V (note 3)	$\pm I_L$	–	–	1	μA
Output impedance	Z_O	–	1	–	kΩ
Outputs PD1, PD2					
Output impedance	Z_O	–	5	10	kΩ
LEVEL DETECTOR					
Inputs HFI1, HFI2					
A.C. input voltage range (peak-to-peak value)	$V_{I(p-p)}$	0,25	–	2,5	V
Input capacitance	C_I	–	–	7	pF
Output FB					
Output current at V_{FB} = 2 V	I_{FB}	–	150	–	μA
OPERATIONAL AMPLIFIER (note 4)					
Inputs OA1, OA2					
Common-mode voltage range	V_{CIM}	1,5	–	6,0	V
Input offset voltage	$\pm V_{IOF}$	–	20	–	mV
Input current (note 1)	$\pm I_I$	–	–	1	μA
Input offset current (note 5)	$\pm I_{IOF}$	–	–	0,1	μA
Input capacitance	C_I	–	–	7	pF
Common-mode rejection ratio	CMRR	40	–	–	dB
Open loop gain (d.c.)	A	40	–	–	dB
Gain bandwidth product (20 dB/decade roll-off)		1	5	–	MHz
Output OA3					
Output voltage LOW at $-I_{OL}$ = 1 mA	V_{OL}	0	–	1	V
Output voltage HIGH at I_{OH} = 1 mA	V_{OH}	8,0	–	V_{DD2} + 0,5	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
VCO					
Input VCO1, output VCO2					
Mutual conductance at 100 kHz	g_m	1,5	–	–	mA/V
Bandwidth (–3 dB cut-off)	B_{gm}	20	–	–	MHz
Input capacitance	C_I	–	–	7	pF
Output capacitance	C_O	–	–	7	pF
Feedback capacitance	C_{FB}	–	–	5	pF
Input leakage current (note 1)	$\pm I_I$	–	–	1	μA
Output current at 10 MHz	$\pm I_O$	–	1	–	mA
Small-signal voltage gain at 100 kHz	A_V	4	–	–	V/V
TIMING					
Operating frequency (except VCO)	F_{CEFM}	0,1	–	5	MHz
Operating frequency (VCO only)	F_{VCO}	0,2	–	10	MHz
Outputs $\overline{\text{CLDE}}$, DADE, $\overline{\text{SSDE}}$, FSDE, $\overline{\text{CEFM}}$ (Fig. 6 and note 6)					
Output rise time	t_{OR}	–	–	50	ns
Output fall time	t_{OF}	–	–	40	ns
$\overline{\text{CLDE}}$ period	t_{OCP}	400	–	–	ns
$\overline{\text{CLDE}}$ HIGH time	t_{OCH}	150	–	–	ns
$\overline{\text{CLDE}}$ LOW time	t_{OCL}	150	–	–	ns
DADE/$\overline{\text{SSDE}}$/FSDE to $\overline{\text{CLDE}}$ set-up time	t_{ODS}	100	–	–	ns
$\overline{\text{CLDE}}$ to DADE/$\overline{\text{SSDE}}$/FSDE hold time	t_{ODH}	100	–	–	ns
$\overline{\text{SSDE}}$ LOW time (note 7)	t_{SSL}	–	3	–	$\overline{\text{CEFM}}$ period
$\overline{\text{CLDE}}$ LOW time during FSDE (Fig. 5 and note 8)	t_{OCG}	16	46	–	$\overline{\text{CEFM}}$ period
Outputs SBCL, SDATA, P, SWCL (Fig. 7)					
Output rise time (SBCL, SDATA) (note 6)	t_{OR}	–	–	50	ns
Output fall time (SBCL, SDATA) (note 6)	t_{OF}	–	–	40	ns
Output rise time (P, SWCL) (note 9)	t_{OSR}	–	–	200	ns
Output fall time (P, SWCL) (note 9)	t_{OSF}	–	–	200	ns
SBCL HIGH time	t_{OCH}	150	–	–	ns
SBCL LOW time	t_{OCL}	150	–	–	ns
SDATA to SBCL set-up time	t_{ODS}	100	–	–	ns
P to SWCL set-up time	t_{ODSP}	1	–	–	ns
SBCL to SDATA hold time	t_{ODH}	100	–	500	ns
SBCL to SWCL hold time	t_{SWH}	0	–	–	μs
SWCL duty cycle (t_{HIGH}/t_{period})		40	50	60	%

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parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Output FD					
Output rise time (note 6)	t_{FDR}	–	–	1	μs
Output fall time (note 6)	t_{FDF}	–	–	1	μs
Outputs DEFM, $\overline{\text{CEFM}}$ (Fig. 8)					
Output rise time (note 6)	t_{OR}	–	–	50	ns
Output fall time (note 6)	t_{OF}	–	–	40	ns
DEFM to $\overline{\text{CEFM}}$ set-up time (note 10)	t_{ODS}	50	–	–	ns
$\overline{\text{CEFM}}$ to DEFM hold time (note 10)	t_{ODH}	70	–	–	ns
$\overline{\text{CEFM}}$ HIGH time	t_{OCH}	50	–	–	ns
$\overline{\text{CEFM}}$ LOW time	t_{OCL}	50	–	–	ns

NOTES TO THE CHARACTERISTICS

1. At T_{amb} = 25 °C; V_{IN} = −0,3 to + 6,5 V; V_{DD1} = 6,5 V.
2. Short-circuit protected to V_{DD1} and V_{SS}. The maximum load capacitance that can be applied before short-circuit protection becomes operative is 150 pF.
3. At T_{amb} = 25 °C; output in high impedance state.
4. All tests performed within common-mode voltage range.
5. At T_{amb} = 25 °C.
6. Output loading = 50 pF.
7. $\overline{\text{SSDE}}$ remains LOW for only one negative edge of $\overline{\text{CLDE}}$.
8. Excessive bit-slip may cause gap to disappear. $\overline{\text{CLDE}}$ remains LOW when FSDE is HIGH.
9. Output loading = 150 pF.
10. Free running VCO frequency tuned to nominal and PLL in lock with a typical application circuit.

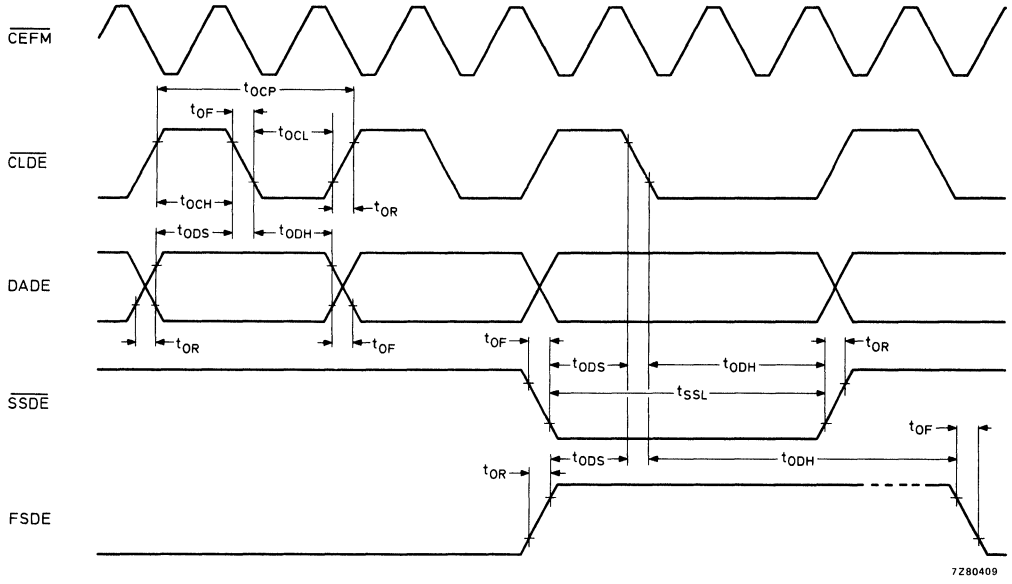

Fig. 6 Timing of waveform outputs to SAA7020.

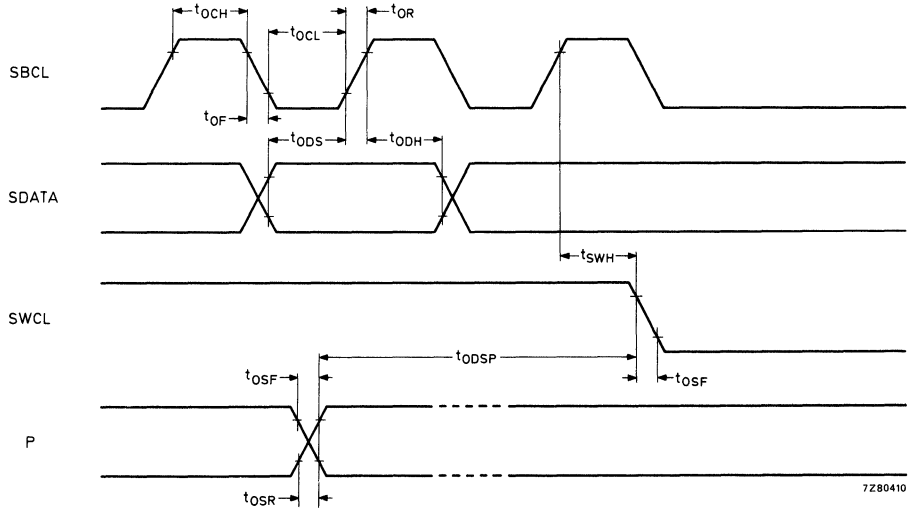

Fig. 7 Timing of waveform outputs for subcoding: reference levels are 0,8 and 2,4 V; SBCL and SDATA output loading = 50 pF; SWCL and P output loading = 150 pF; SWCL has a 50% duty cycle.

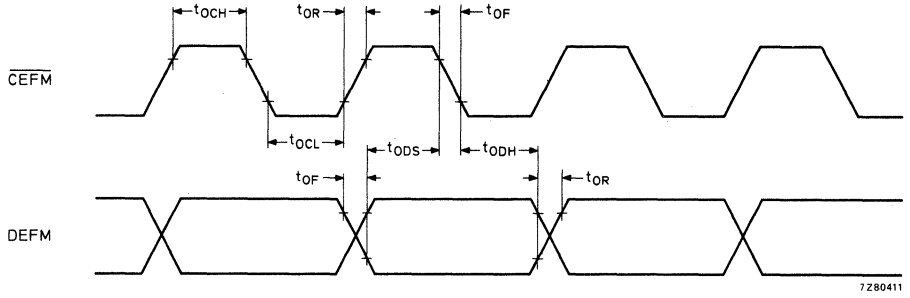

Fig. 8 Timing of EFM output waveforms: output loading = 50 pF; reference levels are 0,8 and 2,4 V.

Error Corrector for Compact Disc — SAA7020

GENERAL DESCRIPTION

The SAA7020 detects and corrects errors in digital data received from the demodulator (SAA7010). The data is received serially in frames of 32 x 8-bit symbols and, after processing, is transmitted in a 16-bit serial format to the interpolating and muting circuit (SAA7000). An error flag is generated to warn of data in which errors have not been corrected.

Features

- Internal timing and control circuits
- Serial data input and output
- 8-bit bidirectional data bus to external RAM (2K x 8 bits)
- Corrects up to seven erroneous frames of data
- Generates error flag to identify unreliable data
- Provides a motor speed control output which stabilizes the input data rate and eliminates wow and flutter.

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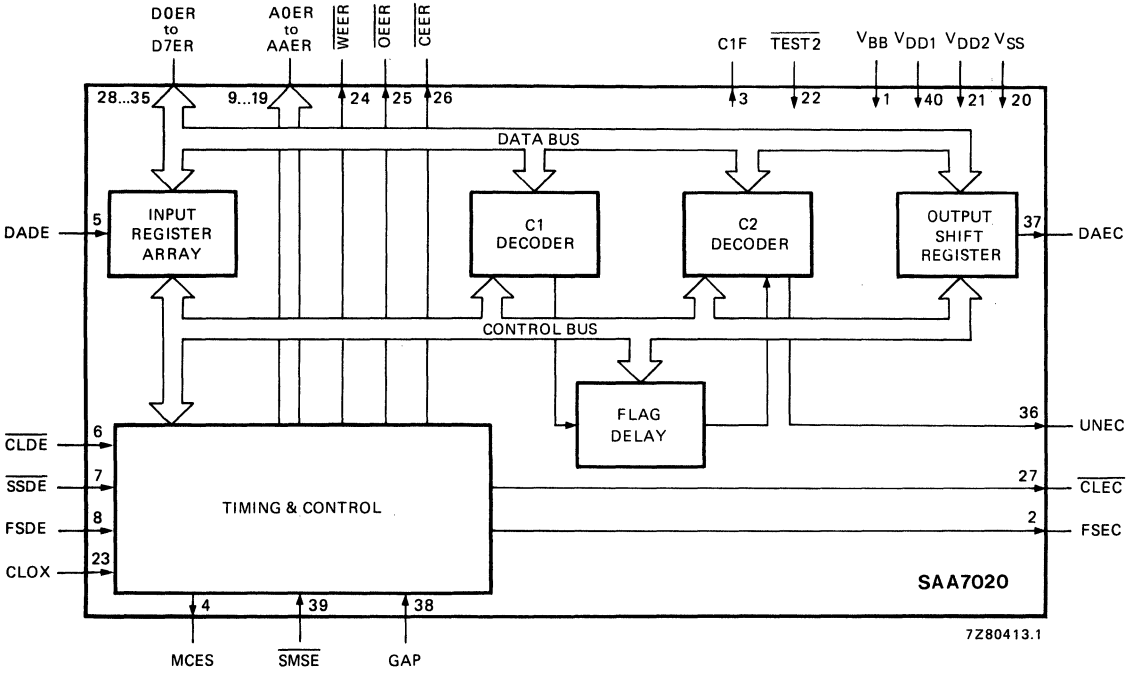

Fig. 1 Block diagram.

PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

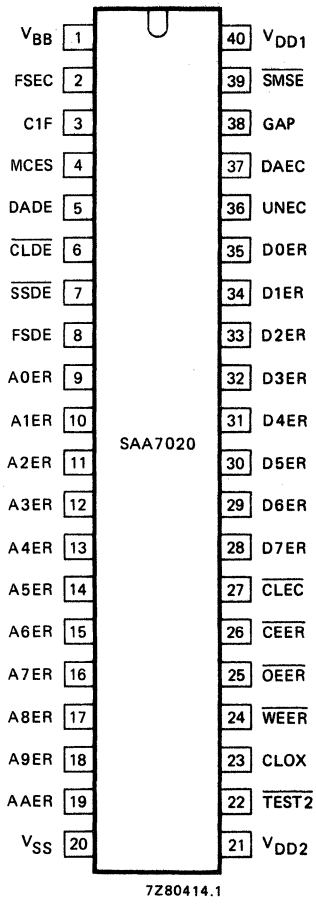

Fig. 2 Pinning diagram.

PINNING

1	V_{BB}	back bias supply
2	FSEC	frame sync pulse output
3	C1F	C1 decoder error flag
4	MCES	motor speed control output
5	DADE	serial data input
6	$\overline{CLDE}$	data bit clock input
7	$\overline{SSDE}$	symbol sync signal input
8	FSDE	frame sync signal input
9-19	A0ER-AAER	address outputs to external RAM
20	V_{SS}	ground
21	V_{DD2}	+ 12 V supply
22	$\overline{TEST2}$	test input
23	CLOX	basic clock input
24	$\overline{WEER}$	write enable output to external RAM
25	$\overline{OEER}$	output enable signal to external RAM
26	$\overline{CEER}$	chip enable output to external RAM
27	$\overline{CLEC}$	output data clock
28-35	D0ER-D7ER	data bus to/from external RAM
36	UNEC	error flag output
37	DAEC	data output (two's complement) and SAA7000 output format control
38	GAP	input to determine DAEC control output to SAA7000
39	$\overline{SMSE}$	mute signal from servo
40	V_{DD1}	+ 5 V supply

FUNCTIONAL DESCRIPTION

The SAA7020 error corrector receives data samples from the Compact Disc Digital Audio demodulating system (SAA7010), processes the data samples and then passes them to the interpolating and muting circuit (SAA7000). The processing detects erroneous data and then, if possible, corrects the errors. If error correction is not possible, a flag (UNEC) is generated to warn of unreliable data output. The SAA7020 also controls the motor speed of the disc drive servo.

Serial data received from the demodulator (SAA7010) is arranged in frames of 32 x 8-bit symbols; 24 of the symbols contain audio samples, the remaining eight symbols contain parity information for error detection/correction. The data (DADE) is clocked into the input register array at the demodulator rate by $\overline{\text{CLDE}}$. The input register array comprises a register which accumulates symbols ready for parallel output to an external RAM and a FIFO register which acts as a jitter reduction circuit.

The jitter reduction circuit uses the difference between the input data rate ($\overline{\text{CLDE}}$) and the system data rate (derived from CLOX) to generate the motor speed control signal $\overline{\text{MCES}}$ (Fig. 3). This forms a feedback loop with the disc drive motor to control the disc speed and hence the input data rate. In this way unwanted effects such as wow and flutter are eliminated from the Compact Disc system, the FIFO being capable of handling deviations from the system data rate of up to ± 2 frames.

An 8-bit bidirectional bus is used for transferring data to and from the external RAM (2K x 8 bits) and an 11-bit bus for addressing. Three bits control the RAM; write enable $\overline{\text{WEER}}$, output enable $\overline{\text{OEER}}$ and chip enable $\overline{\text{CEER}}$ (the latter is for operation with dynamic RAMs).

The error correction process makes use of data interleaving and two Reed-Solomon codes, C1 and C2. The C1 decoder can correct one erroneous symbol in a 32-symbol frame after de-interleaving; the C2 decoder can correct two erroneous symbols in a group of 28 symbols. Input data is de-interleaved and read from the RAM by the C1 decoder where syndromes are formed to check for erroneous symbols. If one error is detected it is corrected and the data is written back to the RAM with some parity symbols being discarded. If more than one error is detected the data is written back to the RAM unchanged but internal C1 flags are set to mark these symbols as unreliable. The data in the RAM is then further de-interleaved and read back to the C2 decoder. The symbols are then checked for errors as previously, if one error is detected it is corrected and the symbols are again written back to the RAM. If two error flags are detected erasure correction is attempted when the flags are received from C1. The corrected data is then written back to the RAM. If more than two symbols are in error the data is written back to the RAM unchanged but a flag is set to mark these symbols as unreliable. At this stage the remaining parity bits are discarded.

After processing, the data is held in the RAM to give a 5-frame delay so that the error warning flag UNEC can be sent to the interpolation and muting circuit (SAA7000). The UNEC flag is also output when $\overline{\text{SMSE}}$ is active, this warns of data to be immediately muted. At the end of the 5-frame delay, the data is read back to the output shift register to be serially shifted out at DAEC.

Pin functions

pin no.	mnemonic	description
1	V_{BB}	Back bias supply voltage: −2,5 V ± 20%.
2	FSEC	Frame sync pulse output, data is valid on the falling edge (Figs 5 and 9).
3	C1F	This output pin flags uncorrectable C1 errors.
4	MCES	Motor control error signal; this open drain output provides a pulse width modulated signal to control the rate of data entry. If the data rate has been correct for a period, MCES duty cycle = 50%; if low, the duty cycle < 50%; if high, the duty cycle > 50% (Fig. 3).
5	DADE	Serial data input. The data is clocked in by $\overline{\text{CLDE}}$ in 8-bit symbols, the most-significant bit first (Figs 4 and 6).
6	$\overline{\text{CLDE}}$	Data clock input, data is accepted into DADE on the negative transition of $\overline{\text{CLDE}}$ (Figs 4 and 6).
7	$\overline{\text{SSDE}}$	Input indicating the last bit of a symbol. A symbol is counted and clocked in when $\overline{\text{SSDE}}$ is LOW during the negative transition of $\overline{\text{CLDE}}$; for correct operation, $\overline{\text{SSDE}}$ must remain LOW for only one negative transition in eight (Figs 4 and 6).
8	FSDE	Input indicating the end of a data frame. Indication is given when FSDE is HIGH during a negative transition of $\overline{\text{CLDE}}$.
9-19	A0ER-AAER	Eleven address outputs to the external RAM. When data is being received at DADE, $\overline{\text{CLDE}}$, etc. then addresses A0ER to AAER are completely exercised every four frames allowing refresh to be automatic for dynamic RAMs (Figs 7 and 8).
20	V_{SS}	Ground.
21	V_{DD2}	Positive supply voltage: + 12 V ± 10%.
22	$\overline{\text{TEST2}}$	Test input. Connect to V_{DD1} or V_{DD2} for normal operation.
23	CLOX	System clock input, typical frequency = 4,2336 MHz (Fig. 6).
24	$\overline{\text{WEER}}$	Write enable output to external RAM; when LOW, SAA7020 is writing to the RAM (Fig. 7).
25	$\overline{\text{OEER}}$	Output enable to external RAM; when HIGH, memory output buffers must be in the high impedance state (Figs 7 and 8).
26	$\overline{\text{CEER}}$	Chip enable output for use with dynamic memories (Figs 7 and 8).
27	$\overline{\text{CLEC}}$	Output data clock; data is valid on the falling edge (Figs 5 and 9).
28-35	D0ER-D7ER	Input/output ports for 8-bit bidirectional bus from/to external RAM. The outputs are in the high impedance state when $\overline{\text{OEER}}$ is LOW (Figs 7 and 8).
36	UNEC	Error flag output; when HIGH, indicates that output data is unreliable. During active data output (i.e. when $\overline{\text{CLEC}}$ is operating) UNEC applies to each symbol of 8 bits of data output at that time. Before each data word of two symbols is output, UNEC applies to the whole data word that will follow in five frames time.

FUNCTIONAL DESCRIPTION (continued)

pin no.	mnemonic	description
37	DAEC	Serial data output. Data is clocked out by $\overline{CLEC}$ and is in 16-bit words separated by gaps. Each word is in two's complement format with the most-significant bit first and comprises two 8-bit symbols. Data is valid on the falling edge of $\overline{CLEC}$. During the gap between the data words, the state of pin 38 (GAP) acts as an output from DAEC (Figs 5 and 9).
38	GAP	The input level at this pin is reflected in the state of the output from DAEC between data words and is used to control the output format of the SAA7000. When GAP is HIGH, DAEC gap level is HIGH, and vice versa (Fig. 5).
39	$\overline{SMSE}$	Select muting input. If $\overline{SMSE}$ is held LOW, the UNEC output will be held HIGH causing the interpolation and muting circuit (SAA7000) to mute the data.
40	V_{DD1}	Positive supply voltage: + 5 V ± 10%.

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HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134); V_{SS} = 0 V

Supply voltage 1 range (pin 40)	V_{DD1}	−0,3 to + 7,5 V
Supply voltage 2 range (pin 21)	V_{DD2}	−0,3 to + 15 V
Back bias supply voltage range (pin 1)	V_{BB}	−4 to + 0,3 V
Input voltage range (except TEST)	V_I	−0,3 to + 7,5 V
Input voltage range (TEST only)	V_I	−0,3 to + 15 V
Output voltage range (except MCES)	V_O	−0,3 to + 7,5 V
Output voltage range (MCES only) applied through a 10 kΩ resistor	V_O	−0,35 to + 15 V
Output current	I_O	max. 10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage 1 (pin 40)	V_{DD1}	4,5	5,0	5,5	V
Supply voltage 2 (pin 21)	V_{DD2}	10,8	12,0	13,2	V
Back bias supply voltage (pin 1)	$-V_{BB}$	2,0	2,5	3,0	V
Supply current 1 (pin 40)	I_{DD1}	–	145	280	mA
Supply current 2 (pin 21)	I_{DD2}	–	14	26	mA
Back bias supply current (pin 1)	$-I_{BB}$	–	–	500	μA
Inputs (except D0ER-D7ER)					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH (except $\overline{SMSE}$)	V_{IH}	2,4	–	6,5	V
Input voltage HIGH ($\overline{SMSE}$ only)	V_{IH}	2,0	–	6,5	V
Input current (note 1)	I_I	−1	–	+ 1	μA
Input capacitance	C_I	–	–	7	pF
Input/output D0ER-D7ER					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current (notes 1 and 2)	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage LOW at $-I_{OL}$ = 1,6 mA (notes 3 and 4)	V_{OL}	0	–	0,4	V
Output voltage HIGH at I_{OH} = 0,2 mA (notes 3 and 4)	V_{OH}	3,0	–	V_{DD1} + 0,5	V
Load capacitance (notes 3 and 4)	C_L	–	–	150	pF
Outputs A0ER-AAER, $\overline{WEER}$, $\overline{OEER}$, $\overline{CEER}$, DAEC, UNEC, FSEC, $\overline{CLEC}$ (notes 3 and 4)					
Output voltage LOW at $-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at I_{OH} = 0,2 mA	V_{OH}	3,0	–	V_{DD1} + 0,5	V
Load capacitance	C_L	–	–	150	pF
Output MCES (open drain) (note 5)					
Output voltage LOW with pin 4 connected to V_{DD2} via a 10 kΩ resistor	V_{OL}	0	–	0,4	V
Output current with output OFF and pin 4 connected to V_{DD2} via a 10 kΩ resistor; T_{amb} = 25 °C	I_{OH}	–	–	20	μA

parameter	symbol	min.	typ.	max.	unit
Input CLOX (note 6)					
Operating frequency	f_{IN}	3,0	4,2336	4,5	MHz
Input clock LOW	t_{IXL}	40	–	–	ns
Input clock HIGH	t_{IXH}	40	–	–	ns
Inputs DADE, $\overline{\text{CLDE}}$, $\overline{\text{SSDE}}$, FSDE (note 7)					
Input rise time	t_{IR}	–	–	50	ns
Input fall time	t_{IF}	–	–	50	ns
$\overline{\text{CLDE}}$ period	t_{ICP}	1 CLOX period	–	20	µs
$\overline{\text{CLDE}}$ HIGH	t_{ICH}	100	–	–	ns
$\overline{\text{CLDE}}$ LOW	t_{ICL}	100	–	–	ns
DADE/$\overline{\text{SSDE}}$/FSDE to $\overline{\text{CLDE}}$ set-up time	t_{IDS}	50	–	–	ns
$\overline{\text{CLDE}}$ to DADE/$\overline{\text{SSDE}}$/FSDE hold time	t_{IDH}	80	–	–	ns
$\overline{\text{SSDE}}$ LOW time	t_{SSL}	–	1	–	$\overline{\text{CLDE}}$ period
$\overline{\text{CLDE}}$ gap after FSDE	t_{FCG}	6	–	–	CLOX periods
Input $\overline{\text{SMSE}}$ (note 7)					
Input rise time	t_{IR}	–	1	100	µs
Input fall time	t_{IF}	–	1	100	µs
SMSE to UNEC output delay time	t_{SMD}	–	–	20	CLOX periods
Outputs $\overline{\text{CLEC}}$, DAEC, UNEC, FSEC (notes 3, 4, 7 and 8)					
Output rise time	t_{OR}	–	–	50	ns
Output fall time	t_{OF}	–	–	40	ns
$\overline{\text{CLEC}}$ HIGH	t_{OCH}	130	–	350	ns
$\overline{\text{CLEC}}$ LOW	t_{OCL}	130	–	–	ns
FSEC HIGH	t_{FSH}	6 CLOX periods −180	–	6 CLOX periods + 180	ns
$\overline{\text{CLEC}}$ to FSEC delay time	t_{CFD}	3 CLOX periods −300	–	3 CLOX periods + 300	ns
DAEC/UNEC to FSEC set-up time	t_{UFS}	100	–	–	ns
FSEC to DAEC/UNEC hold time	t_{UFH}	12	–	–	CLOX periods

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parameter	symbol	min.	typ.	max.	unit
RAM interfaces A0ER-AAER, D0ER-D7ER, $\overline{OEER}$, $\overline{CEER}$, $\overline{WEER}$ (notes 3, 4 and 7)					
Output rise time	t_{OR}	–	–	30	ns
Output fall time	t_{OF}	–	–	25	ns
Cycle time	t_C	390	–	670	ns
Read cycle timing					
$\overline{CEER}$ HIGH time	t_{CEH}	65	–	–	ns
$\overline{CEER}$ LOW time	t_{CEL}	265	–	–	ns
A0ER-AAER to $\overline{CEER}$ set-up time	t_{ACS}	0	–	–	ns
$\overline{CEER}$ to A0ER-AAER hold time	t_{ACH}	300	–	–	ns
D0ER-D7ER to $\overline{OEER}$ set-up time	t_{DOS}	85	–	–	ns
$\overline{OEER}$ to D0ER-D7ER hold time	t_{DOH}	0	–	–	ns
D0ER-D7ER to A0ER-AAER set-up time	t_{DAS}	85	–	–	ns
A0ER-AAER to D0ER-D7ER hold time	t_{DAH}	0	–	–	ns
$\overline{OEER}$ to D0ER-D7ER from RAM active	t_{OLZ}	0	–	–	ns
$\overline{OEER}$ to D0ER-D7ER from RAM high impedance state	t_{OHZ}	0	–	100	ns
$\overline{OEER}$ LOW to A0ER-AAER valid	t_{OAD}	−25	–	+ 25	ns
Write cycle timing					
$\overline{CEER}$ HIGH time	t_{CEH}	196	–	–	ns
$\overline{CEER}$ LOW time	t_{CEL}	196	–	–	ns
A0ER-AAER to $\overline{CEER}$ set-up time	t_{ACS}	100	–	–	ns
A0ER-AAER to $\overline{WEER}$ set-up time	t_{AWS}	50	–	–	ns
$\overline{WEER}$ to A0ER-AAER hold time	t_{AWH}	50	–	–	ns
$\overline{WEER}$ to $\overline{CEER}$ set-up time	t_{WCS}	50	–	–	ns
$\overline{CEER}$ to $\overline{WEER}$ hold time	t_{WCH}	65	–	–	ns
D0ER-D7ER to $\overline{CEER}$ set-up time	t_{DCS}	50	–	–	ns
$\overline{CEER}$ to D0ER-D7ER hold time	t_{DCH}	150	–	–	ns
$\overline{WEER}$ to $\overline{CEER}$ recovery time	t_{WR}	65	–	–	ns
D0ER-D7ER to $\overline{WEER}$ set-up time	t_{DWS}	150	–	–	ns
$\overline{WEER}$ to D0ER-D7ER hold time	t_{DWH}	100	–	–	ns
$\overline{OEER}$ to D0ER-D7ER output active	t_{DOZ}	100	–	–	ns
$\overline{OEER}$ to D0ER-D7ER output in high impedance state	t_{ODZ}	20	–	–	ns

NOTES TO THE CHARACTERISTICS

1. Measured from −0,3 to + 6,5 V at T_{amb} = 25 °C; V_{DD1} = 6,5 V.
2. Input/output port in high impedance state (OFF); measured from 0 to 6 V at T_{amb} = 25 °C.
3. Output loading: 1 TTL gate + C_L = 50 pF.
4. All outputs are protected against short-circuit to V_{SS} and V_{DD1}. The maximum load capacitance that can be applied before the short-circuit protection becomes active is 150 pF.
5. Phase detector gain for average MCES output voltage = 1,1 V per frame. Phase detector control range = ± 2 frames.
6. All maximum or minimum values assume respective frequency where appropriate.
7. Reference levels = 0,8 V and 2,4 V.
8. The DAEC level during the advanced UNEC period is defined by the state at pin 38 (GAP). If this state changes during $\overline{CLEC}$ LOW, the timings are applicable. If the state at pin 38 changes at other times, DAEC follows with a delay of between 20 and 500 ns.

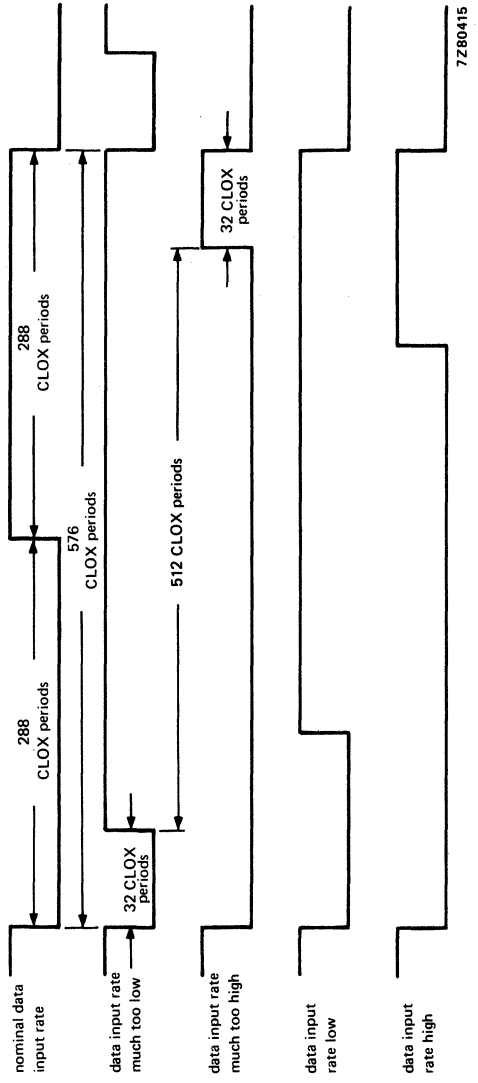


Fig. 3 MCES output waveforms: waveforms are updated each frame (576 CLOX periods); open drain output, rise times depend on external pull-up circuit. This output has an internal clamp to prevent the voltage at pin 4 (MCES) rising above V_{DD2} + 1,8 V maximum.

DEVELOPMENT SAMPLE DATA

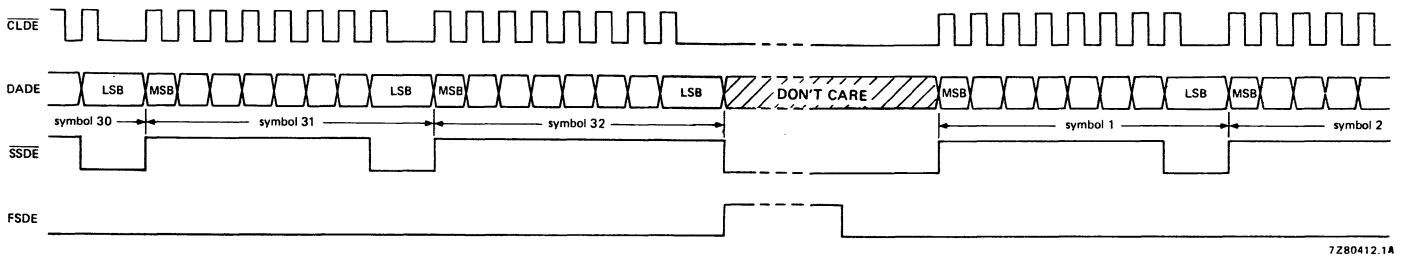
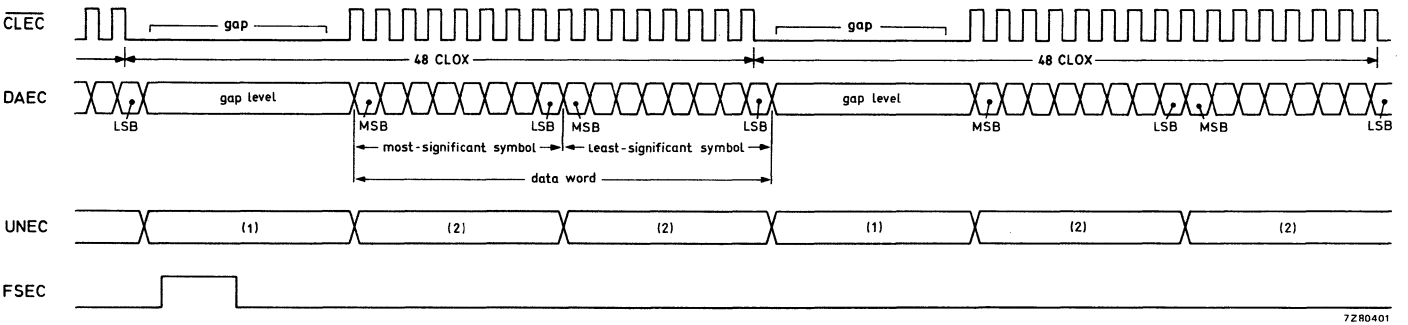


Fig. 4 Typical input waveforms from SAA7010/SAA7011.



(1) When HIGH indicates unreliability of data word that will follow five frames later.
(2) When HIGH indicates unreliability of current symbol.

Fig. 5 Typical output waveforms to SAA7000.

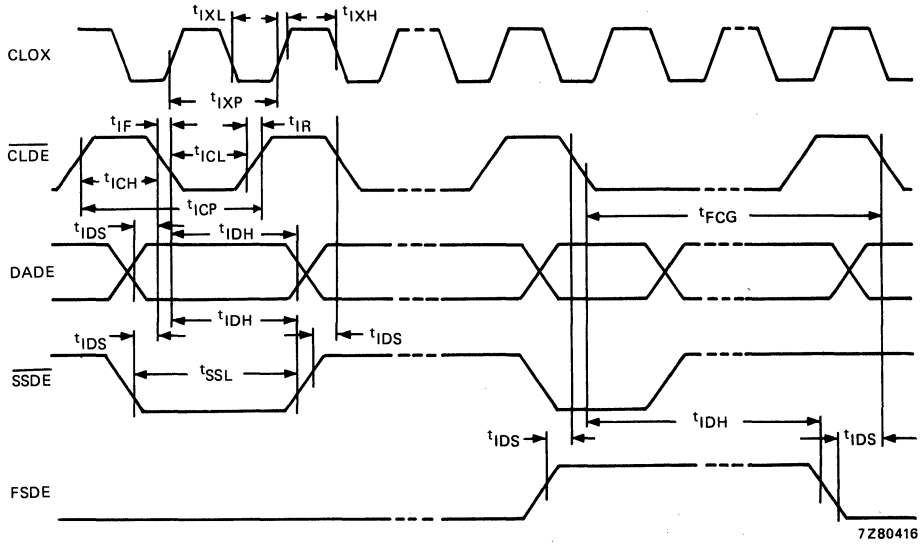


Fig. 6 Input waveform timing; reference levels = 0,8 V and 2,4 V.

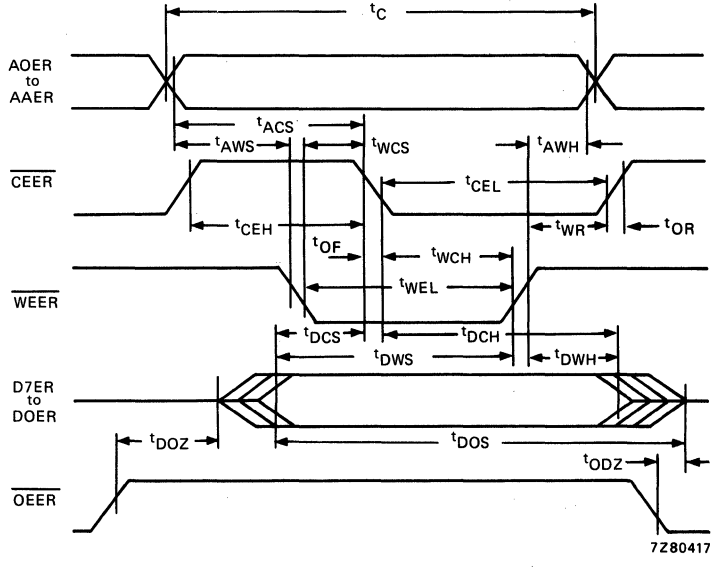


Fig. 7 RAM interface write cycle timing; reference levels = 0,8 V and 2,4 V, output loading = 1 TTL gate and C_L = 50 pF.

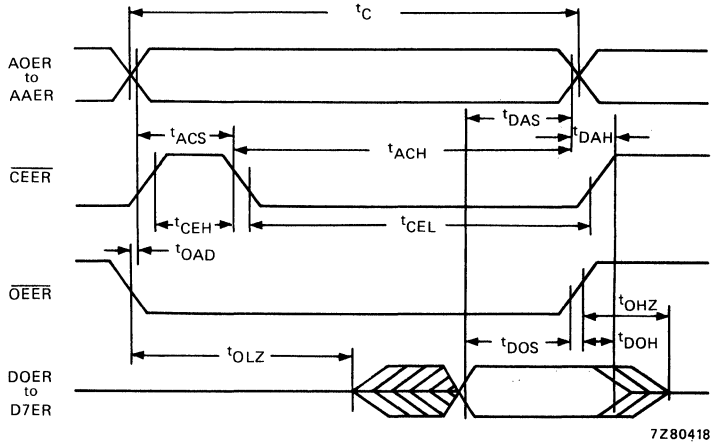
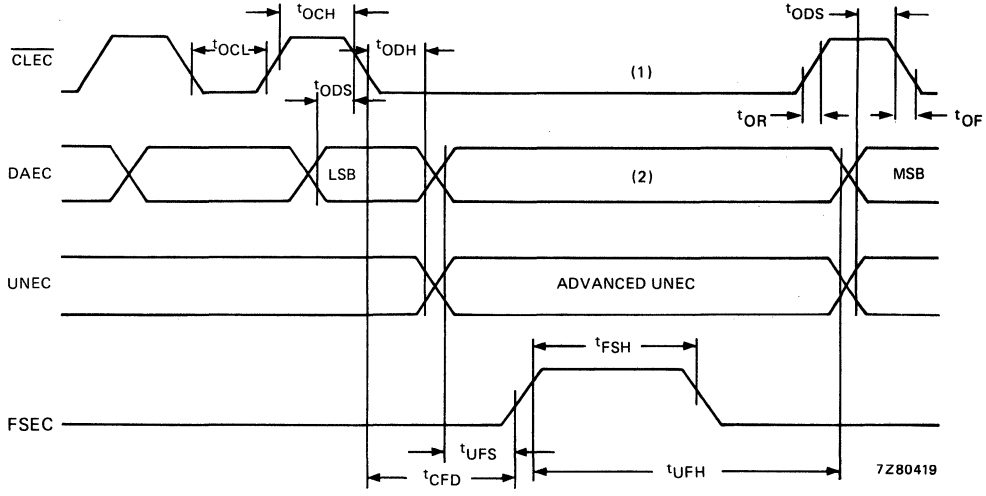


Fig. 8 RAM interface read cycle timing; reference levels = 0,8 V and 2,4 V; output loading = 1 TTL gate and C_L = 50 pF; $\overline{WEER}$ is HIGH during read cycle.



(1) $\overline{CLEC}$ remains LOW for 8 $\overline{CLEC}$ cycle periods.
(2) DAEC level during this period is defined by the level on pin 38 (GAP). If GAP changes during $\overline{CLEC}$ active, the above timings apply. If GAP changes at other times, DAEC follows with a delay of 20 to 500 ns.

Fig. 9 Output waveform timing; reference levels = 0,8 V and 2,4 V, output loading = 1 TTL gate and C_L = 50 pF.

Filter Circuit for Compact Disc SAA7030

GENERAL DESCRIPTION

The SAA7030 is a stereo interpolating digital filter designed for the Compact Disc Digital Audio system. The circuit incorporates two identical filters, each with a sampling rate of four times that of the normal digital audio sampling.

Features

- Suppresses spurious lobes in the audio spectrum
- Improves the signal quality for digital-to-analogue conversion
- Allows a low-order analogue post filter to be used after the digital-to-analogue convertor (DAC)
- Option of offset binary or two's complement data output format
- Electrically-selectable d.c. offset/no offset on data output
- Overflow detection and protection
- Directly compatible with the interpolation and muting circuit (SAA7000)
- Generates a latch output strobe to the DAC

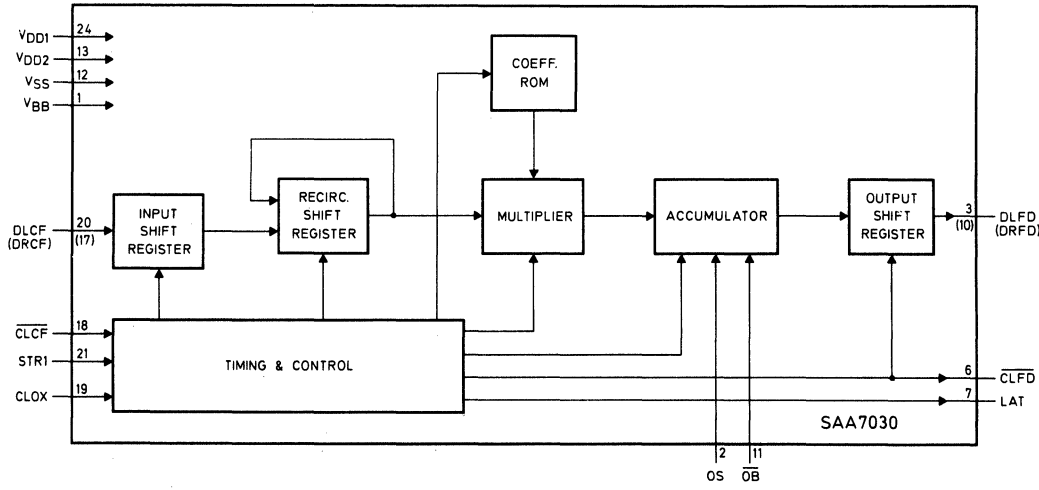


Fig. 1 Block diagram.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

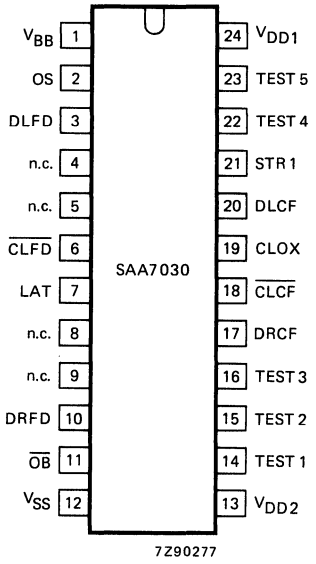


Fig. 2 Pinning diagram.

PINNING

1	V_{BB}	back bias supply
2	OS	offset/no offset select input
3	DLFD	left channel data output
4	n.c.	not connected
5	n.c.	not connected
6	$\overline{CLFD}$	data clock output
7	LAT	strobe output
8	n.c.	not connected
9	n.c.	not connected
10	DRFD	right channel data output
11	$\overline{OB}$	offset binary/two's complement select input
12	V_{SS}	ground
13	V_{DD2}	+ 12 V supply
14	TEST1	test output
15	TEST2	test input
16	TEST3	test input
17	DRCF	right channel data input
18	$\overline{CLCF}$	data clock input
19	CLOX	master clock input
20	DLCF	left channel data input
21	STR1	strobe input
22	TEST4	test input
23	TEST5	test input
24	V_{DD1}	+ 5 V supply

5

FUNCTIONAL DESCRIPTION

The SAA7030 is a stereo interpolating filter which quadruples the data sample rate from 44,1 to 176,4 kHz and thus achieves the following:

1. It suppresses spurious spectrum lobes in the output data that occur between the baseband frequency and 176,4 ± 20 kHz. This allows the DAC to be followed by a low-cost filter of the linear phase, low order, analogue post filter type (a very high order, low-pass filter would otherwise be required to suppress the 44,1 ± 20 kHz lobe).
2. It performs noise-shaping so that a 14-bit DAC yields the same in-band quantizing signal-to-noise ratio as from a 16-bit DAC supplied with unprocessed 44,1 kHz samples.

The circuit incorporates two identical filters (one per channel). Each is a finite impulse response, linear phase transversal filter. The filter length is 96 bits with 16-bit data words and 12-bit coefficients. The composition of each filter is as follows:

serial-to-parallel input shift register;
sixteen 24-bit shift registers for data storage;
96 x 12-bit coefficient ROM;
12 x 16-bit array multiplier;
28-bit accumulator;
parallel-to-serial output shift register.

Overflow protection is incorporated in the filters so that, in the unlikely event of accumulator overflow, the output limits cleanly. Overflow only occurs if the input samples continuously reverse sign coincidently with the coefficients, so that the products of the two entered into the accumulator are continually of the same sign.

The data inputs may run asynchronously with the master clock (CLOX) provided that the data inputs are always complete before the rising edge of the 44,1 kHz input strobe (STR1). A 176,4 kHz output strobe (LAT) is provided, the rising edge of which follows the completion of the serial output data stream. This strobe pulse is timed to be used to gate the master clock (CLOX) if required.

The input OS provides selection of −3% d.c. offset or no offset of the data output voltage level. The format of the output data is selected via the input $\overline{OB}$ to be in offset binary or two's complement form.

Pin functions

pin no.	mnemonic	description
1	V_{BB}	Back bias supply voltage: −2,5 V ± 20%.
2	OS	Offset select input. When connected to V_{DD1}, the data output has a fixed d.c. offset of −3%. When connected to V_{SS}, the data output has no offset.
3	DLFD	Left channel data output. The data is 14-bit serial with most-significant bit first and is valid on the falling edge of the output clock ($\overline{CLFD}$).
6	$\overline{CLFD}$	Data clock output. Typical frequency = 4,2336 MHz (= CLOX). The falling edge of this clock defines output data valid.
7	LAT	Strobe output at 176,4 kHz. The rising edge of this pulse indicates that the output of a 14-bit data word is complete.
10	DRFD	Right channel data output (see DLFD).
11	$\overline{OB}$	Offset binary/two's complement select input. When connected to V_{SS}, the output data is coded in offset binary. When connected to V_{DD1}, the output data is coded in two's complement.
12	V_{SS}	Ground (0 V).
13	V_{DD2}	Positive supply voltage: + 12 V ± 10%.
14	TEST1	Test output; not used in normal operation.
15	TEST2	Test input; in normal operation this pin should be connected to V_{SS} or V_{DD1}.
16	TEST3	Test input; in normal operation this pin should be connected to V_{SS} or V_{DD1}.
17	DRCF	Right channel data input. Data should be 16-bit serial with most-significant-bit first and in offset binary code. It is valid on the falling edge of the input data clock ($\overline{CLCF}$).
18	$\overline{CLCF}$	Input data clock. The falling edge of this clock defines input data valid.
19	CLOX	Master clock input. Runs continuously at a typical frequency of 4,2336 MHz.
20	DLCF	Left channel data input (see DRCF).

FUNCTIONAL DESCRIPTION (continued)

pin no.	mnemonic	description
21	STR1	Strobe input at 44,1 kHz. The internal timing chain of the SAA7030 is synchronized by the rising edge of STR1 which must be synchronous with CLOX within the tolerance specified in CHARACTERISTICS. The rising edge should follow the completion of the input data stream.
22	TEST4	Test input; in normal operation this pin should be connected to V_{DD1}.
23	TEST5	Test input; in normal operation this pin should be connected to V_{DD1}.
24	V_{DD1}	Positive supply voltage: + 5 V ± 10%.

Pins 4, 5, 8 and 9 have no internal connection.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134); V_{SS} = 0 V

Supply voltage 1 range (pin 24)	V_{DD1}	−0,3 to + 7,5	V
Supply voltage 2 range (pin 13)	V_{DD2}	−0,3 to + 15	V
Back bias supply voltage range (pin 1)	V_{BB}	−4 to + 0,3	V
Input voltage range	V_I	−0,3 to + 7,5	V
Output voltage range	V_O	−0,3 to + 7,5	V
Output current	I_O	max. 10	mA
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 125	°C

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage 1 (pin 24)	V_{DD1}	4,5	5,0	5,5	V
Supply voltage 2 (pin 13)	V_{DD2}	10,8	12,0	13,2	V
Back bias supply voltage (pin 1)	$-V_{BB}$	2,0	2,5	3,0	V
Supply current 1 (pin 24)	I_{DD1}	50	120	240	mA
Supply current 2 (pin 13)	I_{DD2}	3,5	8,0	15,0	mA
Back bias supply current (pin 1) at $V_{DD1} \leqslant 5{,}5$ V; $V_{DD2} \leqslant 13{,}2$ V	$-I_{BB}$	–	–	500	μA
Inputs					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current at T_{amb} = 25 °C; V_I = −0,3 to + 6,5 V	$\pm I_I$	–	–	1	μA
Input capacitance	C_I	–	–	7	pF
Outputs (note 1)					
Output voltage LOW at $-I_{OL}$ = 1,6 mA	V_{OL}	−0,3	–	+ 0,4	V
Output voltage HIGH at I_{OH} = 0,2 mA	V_{OH}	3,0	–	V_{DD1} + 0,5	V
Load capacitance	C_L	–	50	150	pF
Input CLOX					
Operating frequency	f_{IX}	1,0	4,23	4,5	MHz
Input clock LOW	t_{IXL}	25	–	–	% of t_{IXP}
Input clock HIGH	t_{IXH}	25	–	–	% of t_{IXP}

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Inputs $\overline{\text{CLCF}}$, DLCF, DRCF, STR1					
$\overline{\text{CLCF}}$ frequency	f_{IC}	0,1	2,12	4,50	MHz
$\overline{\text{CLCF}}$ LOW time	t_{ICL}	75	–	–	ns
$\overline{\text{CLCF}}$ HIGH time	t_{ICH}	75	–	–	ns
DLCF/DRCF to $\overline{\text{CLCF}}$ set-up time	t_{IDS}	25	–	–	ns
$\overline{\text{CLCF}}$ to DLCF/DRCF hold time	t_{IDH}	75	–	–	ns
$\overline{\text{CLCF}}$ LOW to STR1 time	t_{CSL}	0	–	–	ns
STR1 LOW time	t_{ISL}	4	–	–	CLOX cycles
STR1 HIGH time	t_{ISH}	1	–	–	CLOX cycles
CLOX to STR1 rising	t_{XSL}	–5	–	–	ns
CLOX to STR1 HIGH	t_{XSH}	–	–	55	ns
Outputs $\overline{\text{CLFD}}$, DRFD, DLFD, LAT (notes 2 and 3)					
Output rise time (except LAT)	t_{OR}	–	10	30	ns
Output fall time (except LAT)	t_{OF}	–	8	15	ns
Output rise time (LAT only)	t_{LR}	–	7	15	ns
Output fall time (LAT only)	t_{LF}	–	6	10	ns
$\overline{\text{CLFD}}$ HIGH time	t_{OCH}	40	75	–	ns
$\overline{\text{CLFD}}$ LOW time	t_{OCL}	40	105	–	ns
DRFD/DLFD to $\overline{\text{CLFD}}$ set-up time	t_{ODS}	20	70	–	ns
$\overline{\text{CLFD}}$ to DRFD/DLFD hold time	t_{ODH}	50	120	–	ns
$\overline{\text{CLFD}}$ LOW prior to LAT rising	t_{CLD}	100	350	–	ns
CLOX to LAT starting to change (note 4)	t_{XLS}	0	30	–	ns
CLOX to LAT reaching final value	t_{XLF}	0	80	–	ns
$\overline{\text{CLFD}}$ LOW to rising edge of CLOX with rising edge to STR1	t_{XCL}	50	400	–	ns
LAT HIGH time	t_{LH}	–	1	–	CLOX cycle

NOTES TO THE CHARACTERISTICS

1. All outputs are protected against short-circuit to V_{SS} and V_{DD1}. The maximum load capacitance that can be applied before the short-circuit protection becomes active is 150 pF.
2. Output loading C_L = 50 pF.
3. Reference levels are 0,8 and 2 V.
4. Rising edge of LAT occurs in the first CLOX LOW period following the rising edge to STR1 and then recurs at every 24th CLOX cycle.

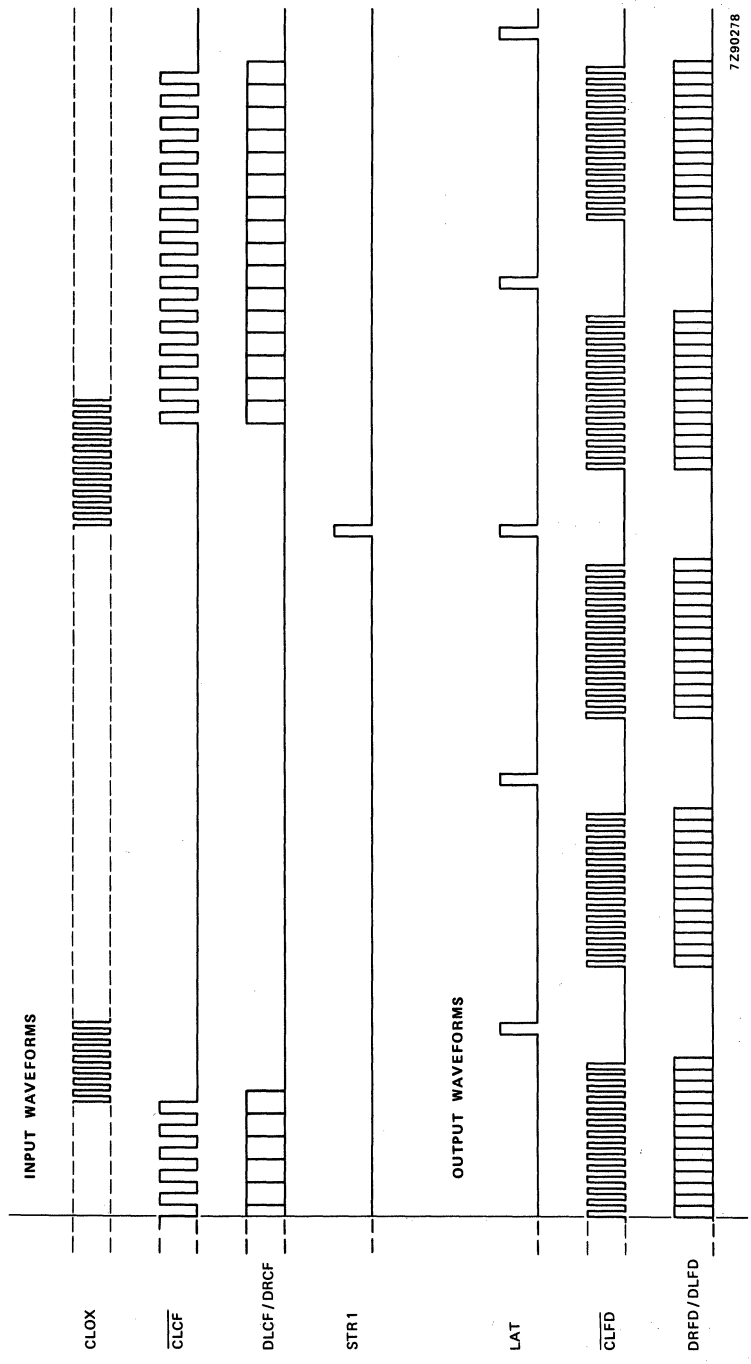
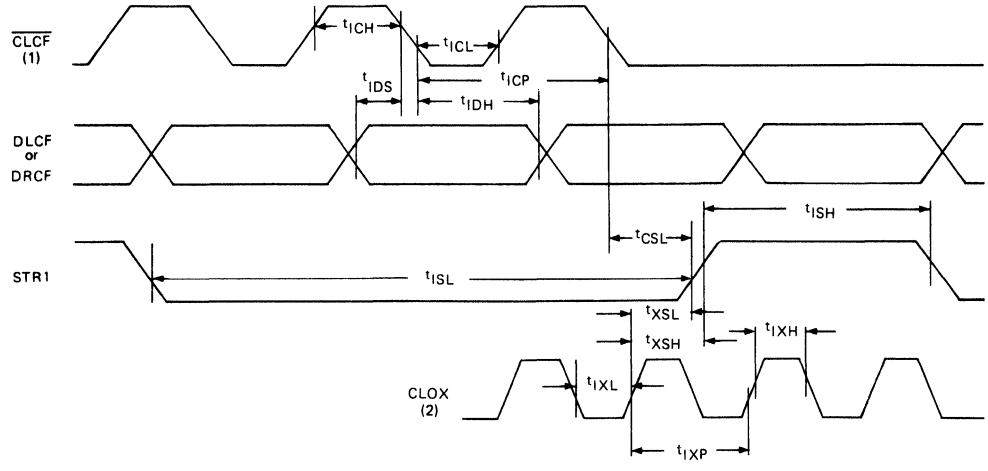


Fig. 3 Typical input and output waveforms (for illustration only).



(1) $\overline{CLCF}$ frequency (f_{IC}) = $1/t_{ICP}$. The trailing edge of $\overline{CLCF}$ must occur 16 times between consecutive rising edges of STR1.

(2) CLOX frequency (f_{IX}) = $1/t_{IXP}$.

Fig. 4 Input waveform timing; reference levels are 0,8 and 2 V.

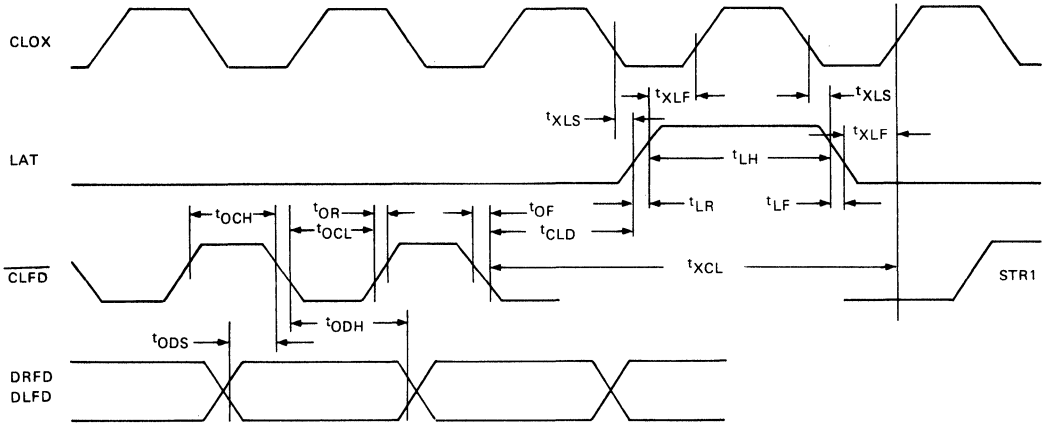


Fig. 5 Output waveform timing: reference levels are 0,8 and 2 V; output loading = 50 pF.

Microprocessor Controlled Stereo Sound Generator for Sound Effects and Music Synthesis

SAA1099

GENERAL DESCRIPTION

The SAA1099 is a monolithic integrated circuit designed for generation of stereo sound effects and music synthesis.

Features

- Six frequency generators
  - eight octaves per generator
  - 256 tones per octave
- Two noise generators
- Six noise/frequency mixers
- Twelve amplitude controllers
- Two envelope controllers
- Two 6-channel mixers/current sink analogue output stages
- TTL input compatible
- Readily interfaces to 8-bit microcontroller
- Minimal peripheral components
- Simple output filtering

Applications

- Consumer games systems
- Home computers
- Electronic organs
- Arcade games
- Toys
- Chimes/alarm clocks

QUICK REFERENCE DATA

Supply voltage (pin 18)	V_{DD}	typ.	5 V
Supply current (pin 18)	I_{DD}	typ.	55 mA
Reference current (pin 6)	I_{ref}	typ.	250 μA
Total power dissipation	P_{tot}		450 mW
Operating ambient temperature range	T_{amb}		0 to + 70 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

Microprocessor Controlled Stereo Sound Generator for Sound Effects and Music Synthesis

SAA1099

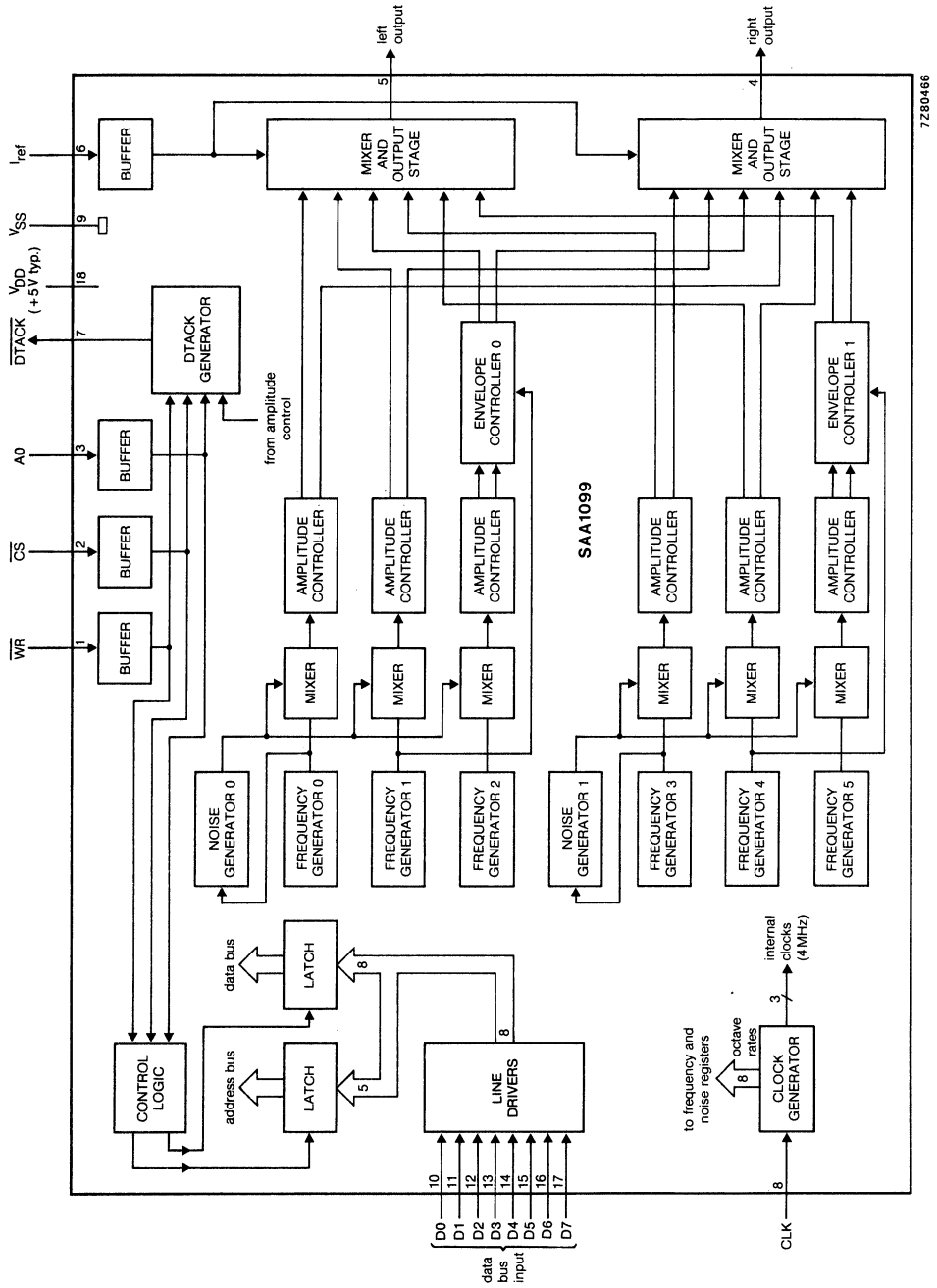


Fig. 1 Block diagram.

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PINNING

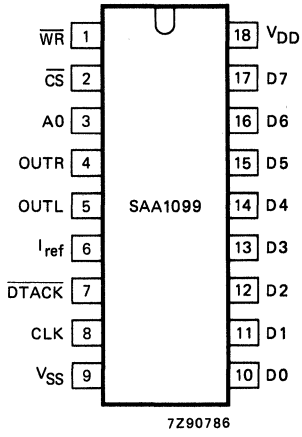

Fig. 2 Pinning diagram.

PIN DESIGNATION

1	$\overline{WR}$	**Write Enable**: active LOW input which operates in conjunction with $\overline{CS}$ and A0 to allow writing to the internal registers.
2	$\overline{CS}$	**Chip Select**: active LOW input to identify valid $\overline{WR}$ inputs to the chip. This input also operates in conjunction with $\overline{WR}$ and A0 to allow writing to the internal registers.
3	A0	**Control/Address select**: input used in conjunction with $\overline{WR}$ and $\overline{CS}$ to load data to the control register (A0 = 0) or the address buffer (A0 = 1).
4	OUTR	**Right channel output**: a 7-level current sink analogue output for the 'right' component. This pin requires an external load resistor.
5	OUTL	**Left channel output**: a 7-level current sink analogue output for the 'left' component. This pin requires an external load resistor.
6	I_{ref}	**Reference current supply**: used to bias the current sink outputs.
7	$\overline{DTACK}$	**Data Transfer Acknowledge**: open drain output, active LOW to acknowledge successful data transfer. On completion of the cycle $\overline{DTACK}$ is set to inactive.
8	CLK	**Clock**: input for an externally generated clock at a nominal frequency of 8 MHz.
9	V_{SS}	**Ground**: 0 V.
10-17	D0-D7	**Data**: Data bus input.
18	V_{DD}	**Power supply**: + 5 V typical.

FUNCTIONAL DESCRIPTION

The following sections provide a detailed functional description of the SAA1099 as shown in the block diagram, Fig. 1.

Frequency generators

Six frequency generators can each select one of 8 octaves and one of 256 tones within an octave. A total frequency range of 30 Hz to 7,74 kHz is available. The outputs may also control noise or envelope generators. All frequency generators have an enable bit which switches them on and off, making it possible to preselect a tone tone and to make it inaudible when required.

The frequency ranges per octave are:

Octave	Frequency range
0	30 Hz to 60 Hz
1	60 Hz to 122 Hz
2	122 Hz to 244 Hz
3	244 Hz to 488 Hz
4	489 Hz to 976 Hz
5	978 Hz to 1,95 kHz
6	1,95 kHz to 3,90 kHz
7	3,91 kHz to 7,81 kHz

Noise generators

The two noise generators both have a programmable output. This may be a software controlled noise via one of the frequency controlled generators or one of three pre-defined noises. There is no tone produced by the frequency generator when it is controlling the noise generator. The noise produced is based on double the frequency generator output, i.e. a range of 61 Hz to 15,6 kHz.
In the event of a pre-defined noise being chosen, the output of noise generator 0 can be mixed with frequency generator 0, 1 and 2; and the output of noise generator 1 can be mixed with frequency generator 3, 4 and 5. In order to produce an equal level of noise and tone outputs (when both are mixed) the amplitude of the tone is increased. The three pre-defined noises are based on a clock frequency of 7,8 kHz, 15,6 kHz or 31,25 kHz.

Noise/frequency mixers

Six noise/frequency mixers each with four selections

- Channel off
- Frequency only
- Noise only
- Noise and frequency

Each mixer channel has one of the frequency generator outputs fed to it, three channels use noise generator 0 and the other three use noise generator 1.

Amplitude controllers

Each of the six channel outputs from the mixer is split up into a right and left component giving effectively twelve amplitude controllers. An amplitude of 16 possible levels is assigned to each of the twelve signals. With this configuration a stereo effect can be achieved by varying only the amplitude component. The moving of a sound from one channel to the other requires, per tone, only one update of the amplitude register contents.

When an envelope generator is used, the amplitude levels are restricted. The number of levels available is then reduced to eight. This is achieved by disabling the least significant bit (LSB) of the amplitude control.

Envelope controllers

Two of the six tone generators are under envelope control. This applies to both the left and right outputs from the tone generator.
The envelope has the following eight possible modes:

- Amplitude is zero
- Single attack
- Single decay
- Single attack-decay (triangular)
- Maximum amplitude
- Continuous attack
- Continuous decay
- Continuous attack-decay

The timing of the envelope controllers is programmable using one of the frequency generators (see Fig. 1). When the envelope mode is selected for a channel its control resolution is halved for that channel from 16 levels to 8 levels by rounding down to the nearest even level.
There is also the capability of controlling the 'right' component of the channel with inverse of the 'left' component, which remains as programmed.

A direct enable permits the start of an envelope to be defined, and also allows termination of an envelope at any time. The envelope rate may be controlled by a frequency channel (see Fig. 1), or by the microprocessor writing to the address buffer register. If the frequency channel controlled is OFF (NE = FE = 0) the envelope will appear at the output, which provides an alternative 'non-square' tone capability. In this event the frequency will be the envelope rate, which provided the rate is from the frequency channel, will be a maximum of 1 kHz. Higher frequencies of up to 2 kHz can be obtained by the envelope resolution being halved from 16 levels to 8 levels. Rates quoted are based on the input of a 8 MHz clock.

Six-channel mixers/current sink analogue output stages

Six channels are mixed together by the two mixers allowing each one to control one of six equally weighted current sinks, to provide a seven level analogue output.

Command/control select

In order to simplify the microprocessor interface the command and control information is multiplexed. To select a register in order to control frequencies, amplitudes, etc. the command-register has to be loaded. The contents of this register determines to which register the data is written in the next control-cycle. If a continuous update of the control-register is necessary, only the control-information has to be written (the command-information does not change).
If the command/control select (A0) is logic 0, the byte transfer is control; if A0 is logic 1, the byte transfer is command.

Interface to microprocessor

The SAA1099 is a data bus based I/O peripheral. Depending on the value of the command/control signal (A0) the $\overline{CS}$ and $\overline{WR}$ signals control the data transfer from the microprocessor to the SAA1099. The data-transfer-acknowledge ($\overline{DTACK}$) indicates that the data transfer is completed. When, during the write cycle, the microprocessor recognizes the $\overline{DTACK}$, the bus cycle will be completed by the processor.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)	V_{DD}	−0,3 to + 7,5	V
Maximum input voltage	V_I	−0,3 to + 7,5	V
at V_{DD} = 4,5 to 5,5 V	V_I	−0,5 to + 7,5	V
Maximum output current	I_O	max. 10	mA
Total power dissipation	P_{tot}	450	mW
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Electrostatic handling*	V_{es}	−1000 to + 1000	V

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* Equivalent to discharging a 250 μF capacitor through a 1 kΩ series resistor.

D.C. CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 0 to 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	55	90	mA
Reference current (note 1)	I_{ref}	100	250	400	μA
INPUTS					
Input voltage HIGH	V_{IH}	2,0	–	6,0	V
Input voltage LOW	V_{IL}	−0,5	–	0,8	V
Input leakage current	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	10	pF
OUTPUTS					
$\overline{DTACK}$ (open drain; note 2)					
Output voltage LOW at I_{OL} = 3,2 mA	V_{OL}	0	–	0,4	V
Voltage on pin 7 (OFF state)	V_{7-9}	−0,3	–	6,0	V
Output capacitance (OFF state)	C_O	–	–	10	pF
Load capacitance	C_L	–	–	150	pF
Output leakage current (OFF state)	$-I_{LO}$	–	–	10	μA
Audio outputs (pins 4 and 5)					
With fixed I_{ref} (note 3)					
One channel on	I_{01}/I_{ref}	90	–	125	%
Six channels on	$I_{06}/6xI_{ref}$	85	–	120	%
With I_{ref} = 250 μA; R_L = 1,1 kΩ (± 5%)					
One channel on	I_{01}/I_{ref}	95	–	115	%
Six channels on	$I_{06}/6xI_{ref}$	90	–	110	%
Output current one channel on	I_{01}	238	–	288	μA
Output current six channels on	I_{06}	1,38	–	1,65	mA
With resistor supplying I_{ref} (note 4)					
Output current one channel on	I_{01}	155	–	270	μA
Output current six channels on	I_{06}	0,94	–	1,65	mA
Load resistance	R_L	600	–	–	Ω
D.C. leakage current all channels off	$-I_{LO}$	–	–	10	μA
Maximum current difference between left and right current sinks (note 5)	$\pm I_{Omax}$	–	–	15	%
Signal-to-noise ratio (note 6)	S/N	–	tbf	–	dB

A.C. CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 0 to 70 °C; timing measurements taken at 2,0 V for a logic 1 and 0,8 V for a logic 0 unless otherwise specified (see waveforms Figs 3 and 4)

parameter	symbol	min.	typ.	max.	unit
Bus interface timing (see Fig. 3)					
A0 set-up time to $\overline{CS}$ fall	t_{ASC}	0	–	–	ns
$\overline{CS}$ LOW to $\overline{WR}$ fall	t_{CSW}	30	–	–	ns
A0 set-up time to $\overline{WR}$ fall	t_{ASW}	50	–	–	ns
$\overline{WR}$ LOW time	t_{WL}	100	–	–	ns
Data bus valid to $\overline{WR}$ rise	t_{BSW}	100	–	–	ns
$\overline{DTACK}$ fall delay from $\overline{WR}$ fall (note 7)	t_{DFW}	0	–	85	ns
A0 hold time from $\overline{WR}$ HIGH	t_{AHW}	0	–	–	ns
$\overline{CS}$ hold time from $\overline{WR}$ HIGH	t_{CHW}	0	–	–	ns
Data bus hold time from $\overline{WR}$ HIGH	t_{DHW}	0	–	–	ns
$\overline{DTACK}$ rise delay from $\overline{WR}$ HIGH	t_{DRW}	0	–	100	ns
Bus cycle time (note 8)	t_{CY}	2CP	–	–	
Bus cycle time (note 9)	t_{CY}	8CP	–	–	
Clock input timing (see Fig. 4)					
Clock period	t_{CLK}	120	125	255	ns
Clock LOW time	t_{HIGH}	55	–	–	ns
Clock HIGH time	t_{LOW}	55	–	–	ns

5

Notes to the characteristics

1. Using an external constant current generator to provide a nominal I_{ref} or external resistor connected to V_{DD}.
2. This output is short-circuit protected to V_{DD} and V_{SS}.
3. Measured with I_{ref} a constant value between 100 and 400 μA; load resistance (R_L) allowed to match E24 (5%) in all applications via:

$$R_L = \frac{0{,}27775 \pm 0{,}03611}{I_{ref}}.$$

4. Measured with R_{ref} = 10 kΩ (± 5%) connected between I_{ref} and V_{DD}; R_L = 820 Ω (± 5%); OUTR and OUTL short-circuit protected to V_{SS}.
5. Left and right outputs must be driven with identical configuration.
6. Sample tested value only.
7. This timing parameter only applies when no wait states are required; otherwise parameter is invalid.
8. The minimum bus cycle time of two clock periods is for loading all registers except the amplitude registers.
9. The minimum bus cycle time of eight clock periods is for loading the amplitude registers. In a system using $\overline{DTACK}$ it is possible to achieve minimum times of 500 ns. Without $\overline{DTACK}$ the parameter given must be used.

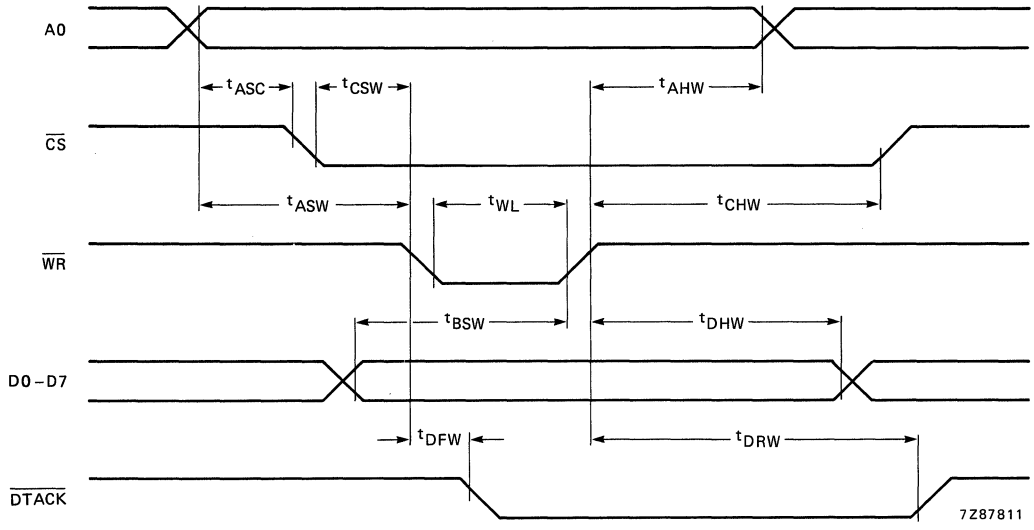


Fig. 3 Bus interface waveforms.

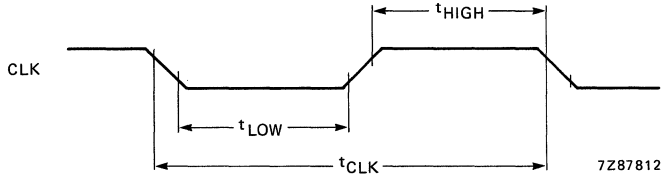


Fig. 4 Clock input waveform.

APPLICATION INFORMATION

Device operation

The SAA1099 uses pulse width modulation to achieve amplitude and envelope levels. The twelve signals are mixed in an analogue format (6 'left' and 6 'right') before leaving the chip. The amplitude and envelope signals chop the output at a minimum rate of 62,5 kHz, compared with the highest tone output of 7,74 kHz. Simple external low-pass filtering is used to remove the high frequency components.

Rates quoted are based on the input of a 8 MHz clock.

A data bus based write only structure is used to load the on-board registers. The data bus is used to load the address for a register, and subsequently the data to that register. Once the address is loaded multiple data loads to that register can be performed.

The selection of address or data is made by the single address bit A0, as shown in register maps Table 1 and Table 2.

The bus control signals $\overline{WR}$ and $\overline{CS}$ are designed to be compatible with a wide range of microprocessors, a $\overline{DTACK}$ output is included to optimise the interface with an S68000 series microprocessor. In most bus cycles $\overline{DTACK}$ will be returned immediately, this applies to all register address load cycles and all except amplitude data load cycles. With respect to amplitude data, a number of wait cycles may need to be performed, depending on the time since the previous amplitude load. $\overline{DTACK}$ will indicate the number of required waits.

5

Register description (see Tables 2 and 3)

The amplitudes are assigned with 'left' and 'right' components in the same byte, on a channel by channel basis. The spare locations that are left between blocks of registers is to allow for future expansion, and should be written as zero's. The tone within an octave is defined by eight bits and the octave by three bits. Note that octaves are paired (0/1, 2/3 etc.). The frequency and noise enables are grouped together for ease of programming. The controls for noise 'colour' (clock rate) are grouped in one byte.

The envelope registers are positioned in adjacent locations. There are two types of envelope controls, direct acting controls and buffered controls. The direct acting controls always take immediate effect, and are:

- Envelope enable (reset)
- Envelope resolution (16/8 level)

The buffered controls are acted upon only at the times shown in Fig. 5 and control selection of:

- Envelope clock source
- Waveform type
- Inverted/non-inverted 'right' component

Table 1 External memory map

select	data bus inputs								operations
A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	D7	D6	D5	D4	D3	D2	D1	D0	data for internal registers
1	X	X	X	A4	A3	A2	A1	A0	internal register address

Where X = don't care state.

Table 2 Internal register map.

register address	data bus inputs D7	D6	D5	D4	D3	D2	D1	D0	operations
00	AR03	AR02	AR01	AR00	AL03	AL02	AL01	AL00	amplitude 0 right channel; left channel
01	1	1	1	1	1	1	1	1	amplitude 1 right/left
02	2	2	2	2	2	2	2	2	amplitude 2 right/left
03	3	3	3	3	3	3	3	3	amplitude 3 right/left
04	4	4	4	4	4	4	4	4	amplitude 4 right/left
05	5	5	5	5	5	5	5	5	amplitude 5 right/left
06	X	X	X	X	X	X	X	X	
07	X	X	X	X	X	X	X	X	
08	F07	F06	F05	F04	F03	F02	F01	F00	frequency of tone 0
09	1	1	1	1	1	1	1	1	frequency of tone 1
0A	2	2	2	2	2	2	2	2	frequency of tone 2
0B	3	3	3	3	3	3	3	3	frequency of tone 3
0C	4	4	4	4	4	4	4	4	frequency of tone 4
0D	F57	F56	F55	F54	F53	F52	F51	F50	frequency of tone 5
0E	X	X	X	X	X	X	X	X	
0F	X	X	X	X	X	X	X	X	
10	X	012	011	010	X	002	001	000	octave 1; octave 0
11	X	032	031	030	X	022	021	020	octave 3; octave 2
12	X	052	051	050	X	042	041	040	octave 5; octave 4
13	X	X	X	X	X	X	X	X	
14	X	X	FE5	FE4	FE3	FE2	FE1	FE0	frequency enable
15	X	X	NE5	NE4	NE3	NE2	NE1	NE0	noise enable
16	X	X	N11	N10	X	X	N01	N00	noise generator 1; noise generator 0
17	X	X	X	X	X	X	X	X	
18	E07	X	E05	E04	E03	E02	E01	E00	envelope generator 0
19	E17	X	E15	E14	E13	E12	E11	E10	envelope generator 1
1A	X	X	X	X	X	X	X	X	
1B	X	X	X	X	X	X	X	X	
1C	X	X	X	X	X	X	X	SE	sound enable (all channels)
1D	X	X	X	X	X	X	X	X	
1E	X	X	X	X	X	X	X	X	
1F	X	X	X	X	X	X	X	X	

Where:
All don't cares (X) should be written as zero's.
00 to 1F block of registers repeats eight times in the block between addresses 00 to FF (full internal memory map).

APPLICATION INFORMATION (continued)

Table 3 Register description

bit	description
ARn3; ARn2; ARn1; ARn0 (n = 0,5)	4 bits for amplitude control of right channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
ALn3; ALn2; ALn1; ALn0 (n = 0,5)	4 bits for amplitude control of left channel 0 0 0 0 minimum amplitude (off) 1 1 1 1 maximum amplitude
Fn7 to Fn0 (n = 0,5)	8 bits for frequency control of the six frequency generators 0 0 0 0 0 0 0 0 lowest frequency 1 1 1 1 1 1 1 1 highest frequency
On2; On1; On0 (n = 0,5)	3 bits for octave control 0 0 0 lowest octave (30 Hz to 60 Hz) 0 0 1 (60 Hz to 122 Hz) 0 1 0 (122 Hz to 244 Hz) 0 1 1 (244 Hz to 488 Hz) 1 0 0 (489 Hz to 976 Hz) 1 0 1 (978 Hz to 1,95 kHz) 1 1 0 (1,95 kHz to 3,90 kHz) 1 1 1 highest octave (3,91 kHz to 7,81 kHz)
FEn (n = 0,5)	frequency enable bit (one tone per generator) FEn = 0 indicates that frequency 'n' is off
NEn (n = 0,5)	noise enable bit (one tone per generator) NEn = 0 indicates that noise 'n' is off
Nn1; Nn0 (n = 0,1)	2 bits for noise generator control. These bits select the noise generator rate (noise 'colour') Nn1 Nn0 clock frequency (kHz) 0 0 31,3 0 1 15,6 1 0 7,6 1 1 61 to 15,6 (frequency generator 0/2)

5

bit	description
En7; En5 to En0 (n = 0,1)	7 bits for envelope control En0 0 left and right component have the same envelope 1 right component has inverse of envelope that is applied to left component En3 En2 En1 0 0 0 zero amplitude 0 0 1 maximum amplitude 0 1 0 single decay 0 1 1 repetitive decay 1 0 0 single triangular 1 0 1 repetitive triangular 1 1 0 single attack 1 1 1 repetitive attack En4 0 4 bits for envelope control (maximum frequency = 976 Hz) 1 3 bits for envelope control (maximum frequency = 1,95 kHz) En5 0 internal envelope clock (frequency generator 1 or 4) 1 external envelope clock (address write pulse) En7 0 reset (no envelope control) 1 envelope control enabled
SE	SE sound enable for all channels (reset on power-up to 0) 0 all channels disabled 1 all channels enabled

Note

All rates given are based on the input of a 8 MHz clock.

APPLICATION INFORMATION (continued)

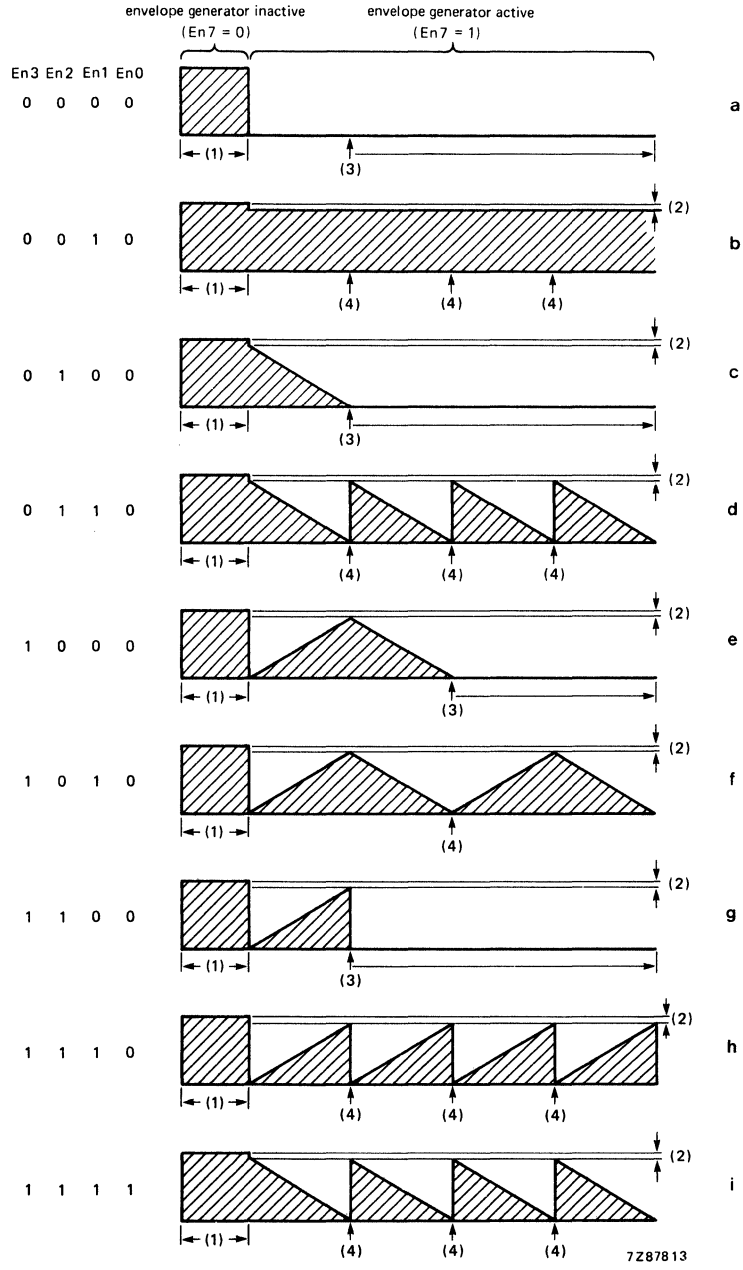


Fig. 5 Envelope waveforms.

Notes to Fig. 5

(1) The level at this time is under amplitude control only (En7 = 0; no envelope).

(2) When the generator is active (En7 = 1) the maximum level possible is 15/16ths of the amplitude level, rounded down to the nearest eight. When the generator is inactive (En7 = 0) the level will be 16/16ths of the amplitude level.

(3) After position (3) the buffered controls will be acted upon when loaded.

(4) At positions (4) the buffered controls will be acted upon if already loaded.

(5) Waveforms 'a' to 'h' show the left channel (En0 = 0; left and right components have the same envelope).
Waveform 'i' shows the right channel (En0 = 1; right component inverse of envelope applied to left).

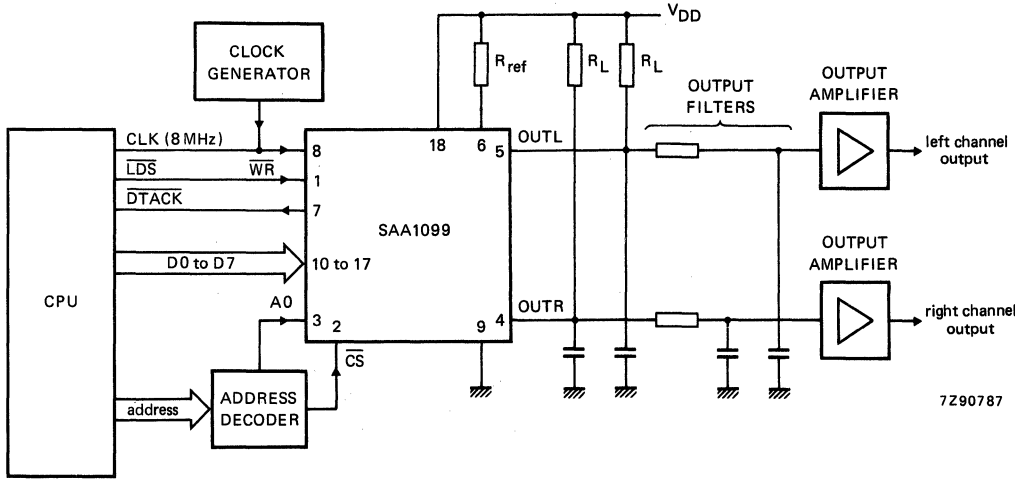


Fig. 6 Typical application circuit diagram.

Sound Generator IC for Organs — UAA2183

DESCRIPTION

ORIC is a monolithic bipolar integrated circuit which generates tones and envelopes for use in electronic keyboards.

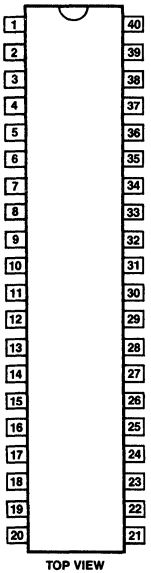
FEATURES

- 10-tone polyphonic tone generator
- 5-octave pitch capability
- 6-octave tone capability
- 3-tone output waveforms (squarewave 50% and 12.5% duty cycle and 8 steps staircase)
- 10 analog envelope generators offering a variety of possibilities (piano, percussion, sustain, percussion/sustain)
- Serial/parallel interface

APPLICATIONS

- Electronic pianos/organs
- Melody generators

PIN CONFIGURATION



TOP VIEW

CD01290S

PIN	FUNCTION
1	CENV10 (envelope capacitor)
2	CENV9
3	CENV8
4	CENV7
5	CENV6
6	DWB (drawbar)
7	SUL (sustain level)
8	T_{out} 2 (tone output)
9	T_{out} 4
10	T_{out} 6
11	T_{out} 1
12	T_{out} 3
13	T_{out} 5
14	DAN (decay time pin)
15	+12 Volt
16	CENV5
17	CENV4
18	CENV3
19	CENV2
20	CENV1
21	IREF (current reference + I^2L supply)
22	TIN8 (TOS I/O pin)
23	TIN7
24	TIN6
25	TIN5
26	TIN9 (TOS input pin)
27	DATA 0 (bus pin)
28	DATA 1
29	DATA 2
30	DATA 3
31	CLOCK (bus)
32	PR (pointer reset bus)
33	TIN12
34	TIN11
35	TIN10
36	TIN1 (TOS I/O highest frequency)
37	TIN2
38	TIN3
39	TIN4
40	COMMON

5

Signetics

Amplifiers
Section 6

Linear Products

Hearing Aid Amplifier — 0M200/S2

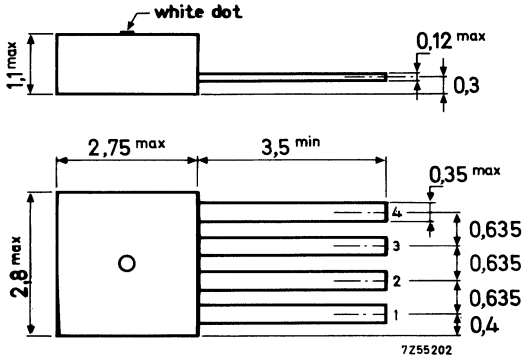
Monolithic integrated circuit amplifier in a plastic envelope, primarily intended for use in ear hearing aids.

QUICK REFERENCE DATA				
For meaning of symbols see test circuit on page 3				
Supply voltage	V_{1-3}	max.	5	V
Supply current	I_2	max.	5	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	25	mW
The following data are measured in test circuit on page 3				
Total supply current	I_{tot}	typ.	1	mA
Transducer gain	G_{tr}	>	77	dB
		typ.	85	dB
Output power at d_{tot} = 10%	P_o	>	0,2	mW
Cut-off frequency (−3 dB)	f_c	>	20	kHz

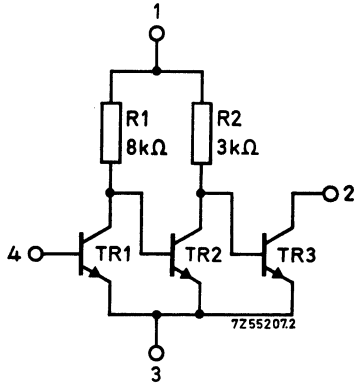
6

PACKAGE OUTLINE (Dimensions in mm)

SOT-20



CIRCUIT DIAGRAM



The sealing of the plastic envelope withstands the accelerated damp heat test of IEC recommendation 68-2 (test D, severity IV, 6 cycles).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

For meaning of symbols test circuit on page 3.

Voltages

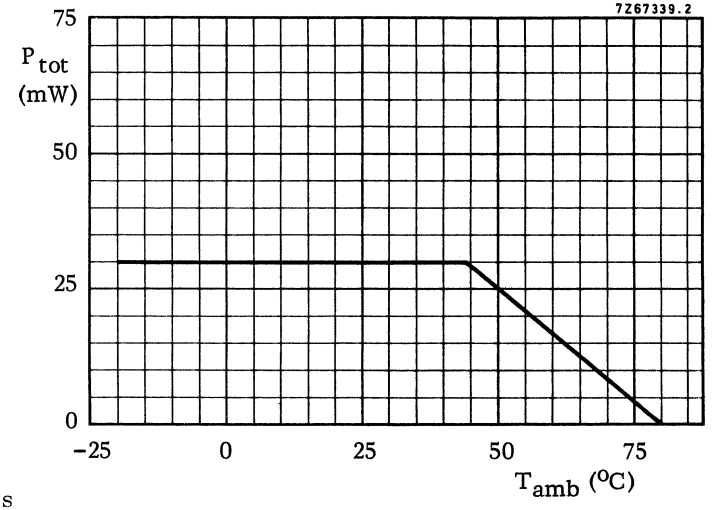
Supply voltage	V_{1-3}	max.	5	V
Output voltage	V_{2-3}	max.	5	V [1]
Input voltage	$-V_{4-3}$	max.	5	V

Currents

Output current	I_2	max.	5	mA
Input current	I_4	max.	5	mA

Power dissipation

Power derating curve



Temperatures

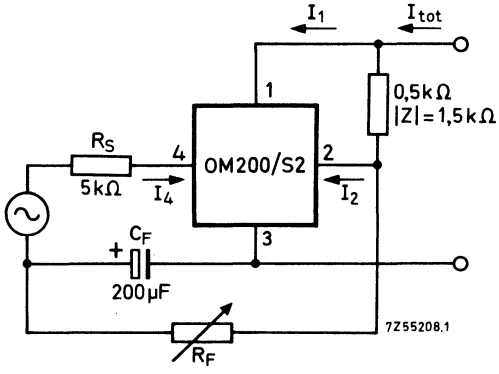
Storage temperature	T_{stg}	−20 to +80	°C
Ambient temperature (see derating curve above)	T_{amb}	−20 to +80	°C

1) This value may be exceeded during inductive switch-off for transient energies < 10 µWs.

CHARACTERISTICS at $V_{1-3} = 1,3\,V; I_2 = 0,7\,mA$ and $T_{amb} = 25\,^{o}C$ unless otherwise specified

Supply currents (no signal)	I_{tot}	<	1,1	mA	
	I_1	typ.	0,30	mA	
Transducer gain at f = 1 kHz	G_{tr}	>	77	dB	1)
		typ.	85	dB	
Total distortion at f = 1 kHz					
P_o = 100 µW	d_{tot}	typ.	4	%	
		<	6	%	
P_o = 200 µW	d_{tot}	<	10	%	
Noise figure at R_S = 5 kΩ					
B = 400 to 3200 Hz	F	typ.	2,5	dB	
		<	6	dB	2)
Cut-off frequency (−3 dB)	f_c	>	20	kHz	
Value of R_F to adjust I_2 at 0,7 mA	R_F		170 to 1000	kΩ	
		typ.	400	kΩ	

Test circuit



Note

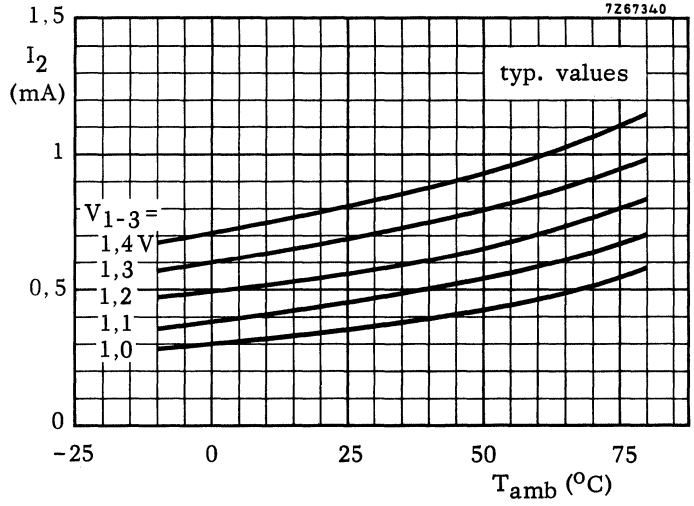
I_2 = 0,7 mA; adjusted by means of R_F
V_{1-3} = 1,3 V; T_{amb} = 25 °C

1) The transducer gain is defined as the ratio of the output power in the load |Z| = 1,5 kΩ and the available input power of the source with R_S = 5 kΩ.

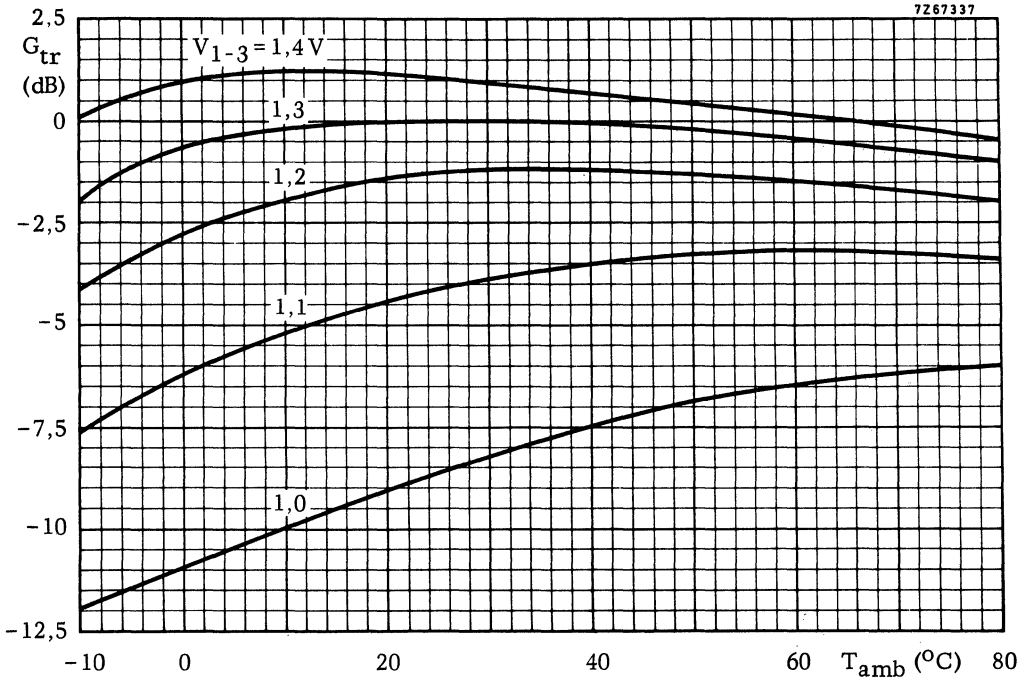
$$G_{tr} = \frac{P_o}{V_i^2/4\,R_S}$$

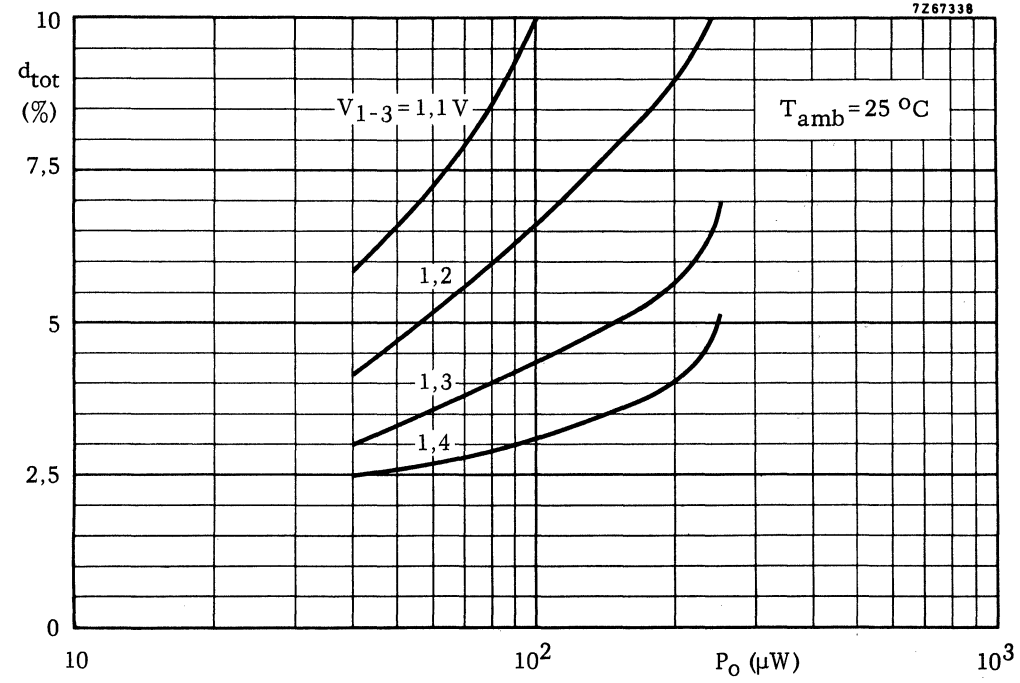
2) Due to special processing and pre-measuring, the flutter-noise level is extremely low.

CHARACTERISTICS



The graph applies to test circuit on page 3


7Z67337
2,5
G_{tr}
(dB)
0
-2,5
-5
-7,5
-10
-12,5
V_{1-3} = 1,4 V
1,3
1,2
1,1
1,0
-10
0
20
40
60
T_{amb} (°C)
80


7Z67338
10
d_{tot}
(%)
7,5
5
2,5
0
V_{1-3} = 1,1 V
1,2
1,3
1,4
T_{amb} = 25 °C
10
10^2
P_o (µW)
10^3

6W Audio Amplifier — TDA1010A

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24 V
Repetitive peak output current	I_{ORM}	max.	3 A
Output power at pin 2; d_{tot} = 10%			
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	6,4 W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6,2 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,4 W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9 W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2 %
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	30 kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20 kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31 mA
Sensitivity for P_o = 5,8 W; R_L = 4 Ω	V_i	typ.	10 mV
Operating ambient temperature	T_{amb}		−25 to + 150 °C
Storage temperature	T_{stg}		−55 to + 150 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

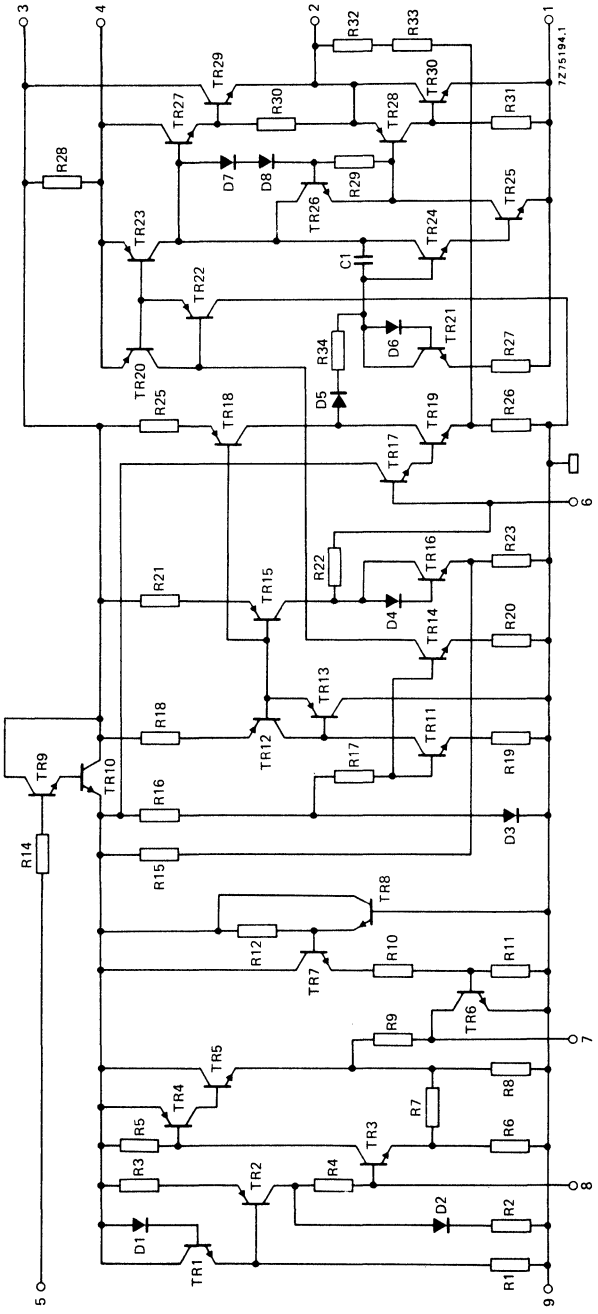


Fig. 1 Circuit diagram.

6

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	5 A
Repetitive peak output current	I_{ORM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; without heatsink at V_P = 14,4 V	t_{sc}	max.	100 hours

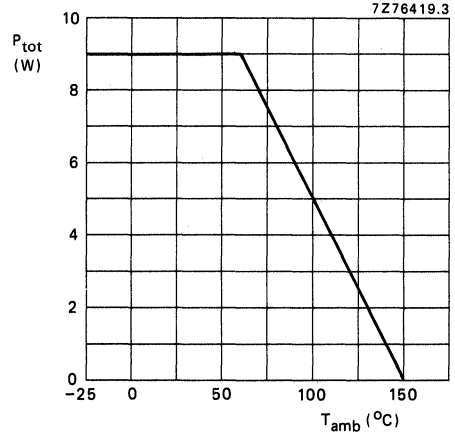


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 14,4 V; R_L = 2 Ω; T_{amb} = 60 °C maximum; thermal shut-down starts at T_j = 150 °C. The maximum sine-wave dissipation in a 2 Ω load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{3,9} = 23\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W,

$R_{th\ h\text{-}a}$ = 23 − (10 + 1) = 12 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P	6 to 24	V
Repetitive peak output current	I_{ORM}	< 3	A
Total quiescent current at V_P = 14,4 V	I_{tot}	typ. 31	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power (see Fig. 4) at d_{tot} = 10%; measured at pin 2; with bootstrap			
V_P = 14,4 V; R_L = 2 Ω (note 1)	P_o	typ. 6,4	W
V_P = 14,4 V; R_L = 4 Ω (note 1 and 2)	P_o	> 5,9 typ. 6,2	W W
V_P = 14,4 V; R_L = 8 Ω (note 1)	P_o	typ. 3,4	W
V_P = 14,4 V; R_L = 4 Ω; without bootstrap	P_o	typ. 5,7	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ. 9	W
Voltage gain			
preamplifier (note 3)	G_{v1}	typ. 24 21 to 27	dB dB
power amplifier	G_{v2}	typ. 30 27 to 33	dB dB
total amplifier	$G_{v\,tot}$	typ. 54 51 to 57	dB dB
Total harmonic distortion at P_o = 1 W	d_{tot}	typ. 0,2	%
Efficiency at P_o = 6 W	η	typ. 75	%
Frequency response (−3 dB)	B	80 Hz to 15	kHz
Input impedance			
preamplifier (note 4)	$\lvert Z_i \rvert$	typ. 30 20 to 40	kΩ kΩ
power amplifier (note 5)	$\lvert Z_i \rvert$	typ. 20 14 to 26	kΩ kΩ
Output impedance of preamplifier; pin 7 (note 5)	$\lvert Z_o \rvert$	typ. 20 14 to 26	kΩ kΩ
Output voltage preamplifier (r.m.s. value) d_{tot} < 1% (pin 7) (note 3)	$V_{o(rms)}$	> 0,7	V
Noise output voltage (r.m.s. value; note 6)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,3	mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ. 0,7 < 1,4	mV mV
Ripple rejection at f = 1 kHz to 10 kHz (note 7)	RR	> 42	dB
at f = 100 Hz; C2 = 1 μF	RR	> 37	dB
Sensitivity for P_o = 5,8 W	V_i	typ. 10	mV
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ. 30	mA

6

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_o \leqslant 3$ W : $d_{tot} \leqslant 1\%$.
3. Measured with a load impedance of 20 kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The tab must be electrically floating or connected to the substrate (pin 9).

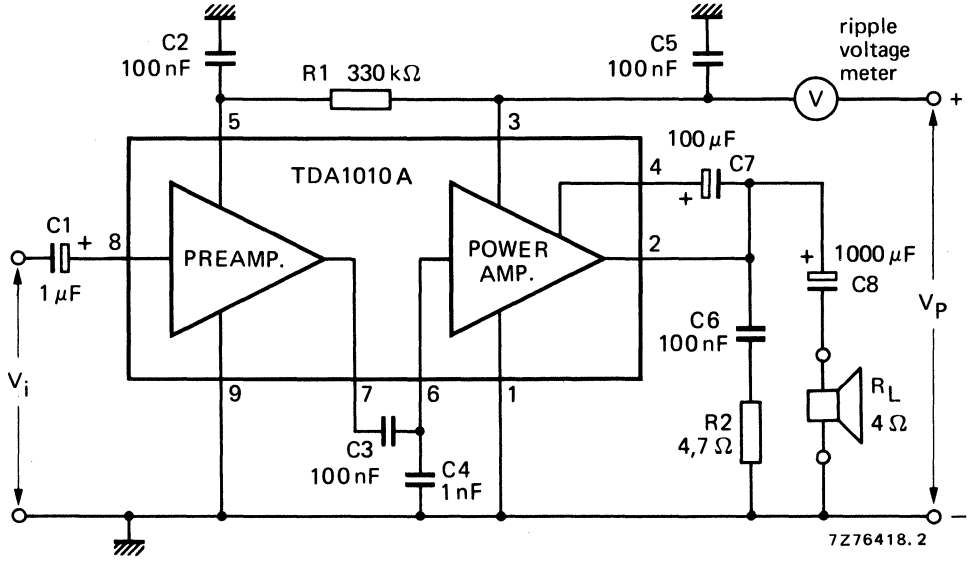


Fig. 3 Test circuit.

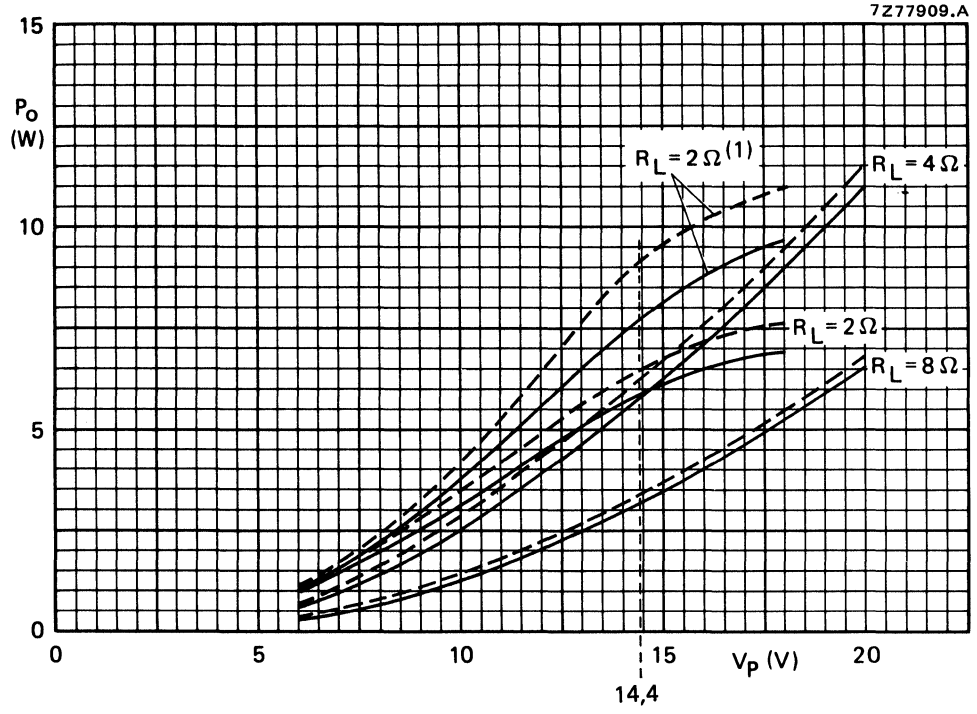


Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, d_{tot} = 10%, T_{amb} = 25 °C.

Fig. 5 See next page.
Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, V_P = 14,4 V.

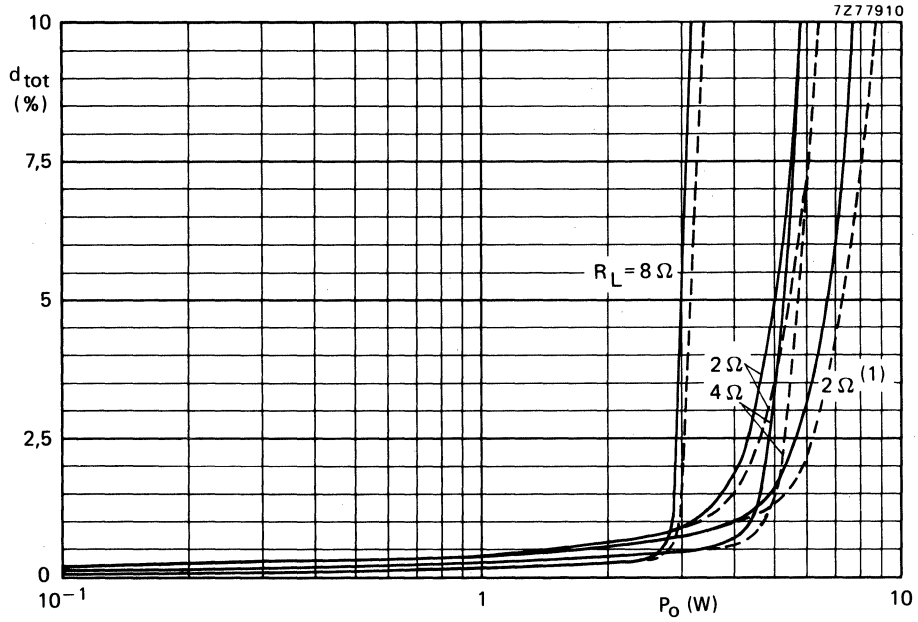


Fig. 5 For caption see page 6.

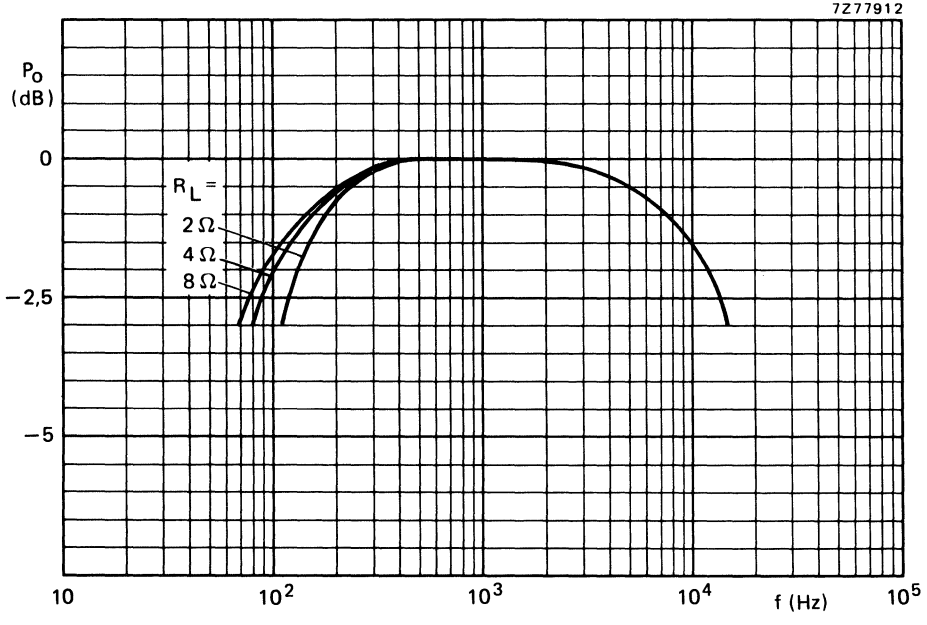


Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values. P_O relative to 0 dB = 1 W; V_P = 14,4 V.

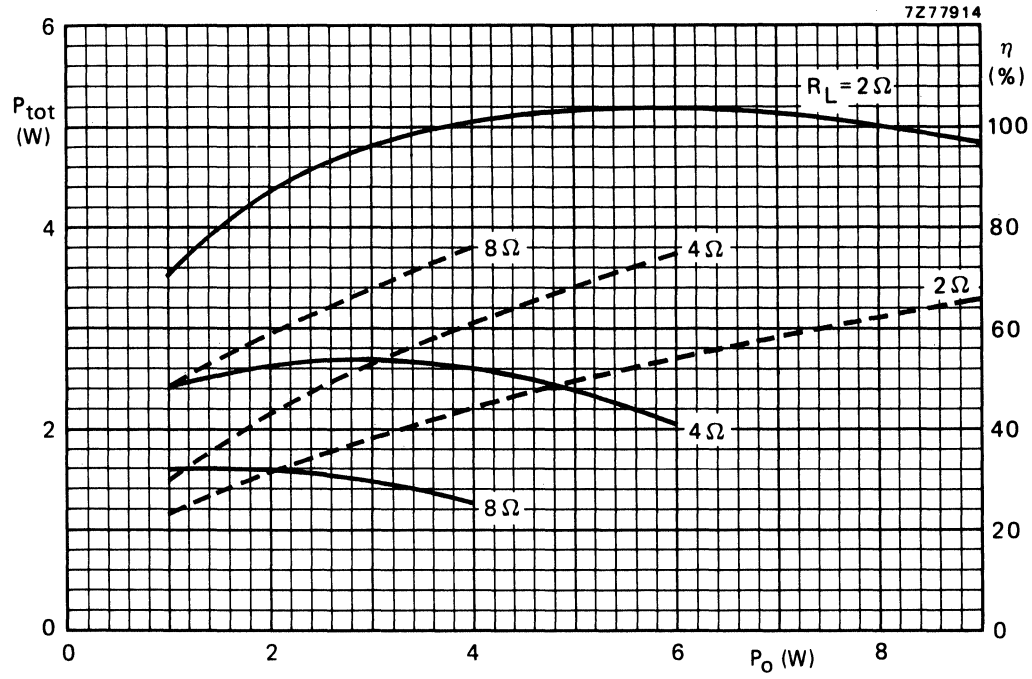


Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for R_L = 2 Ω an external bootstrap resistor of 220 Ω has been used); typical values. V_P = 14,4 V; f = 1 kHz.

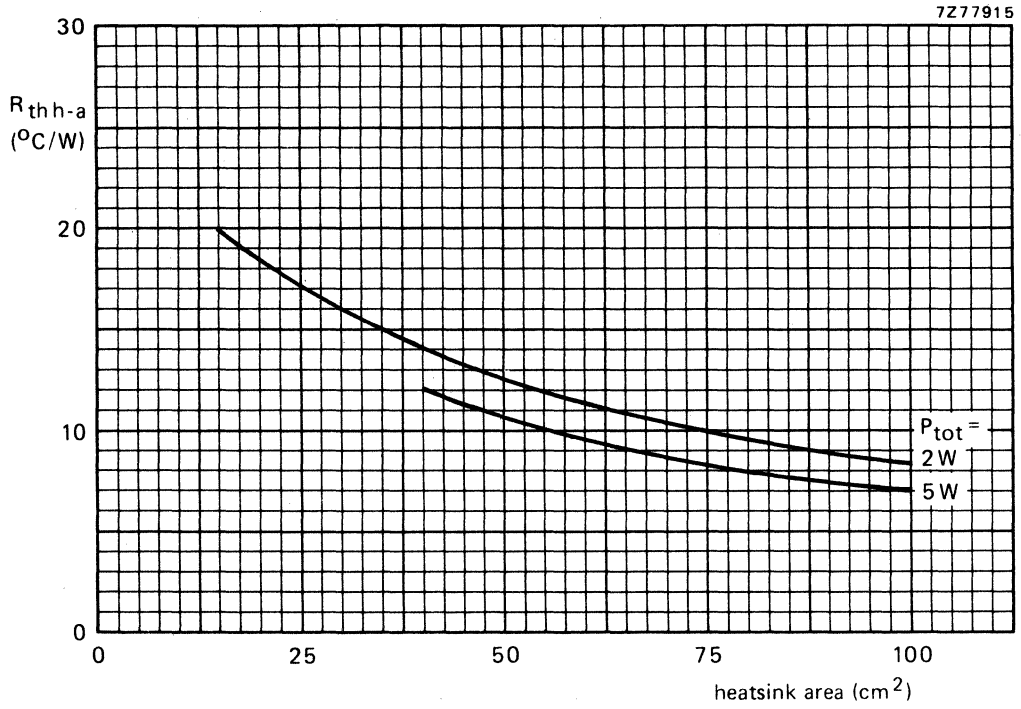


Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.

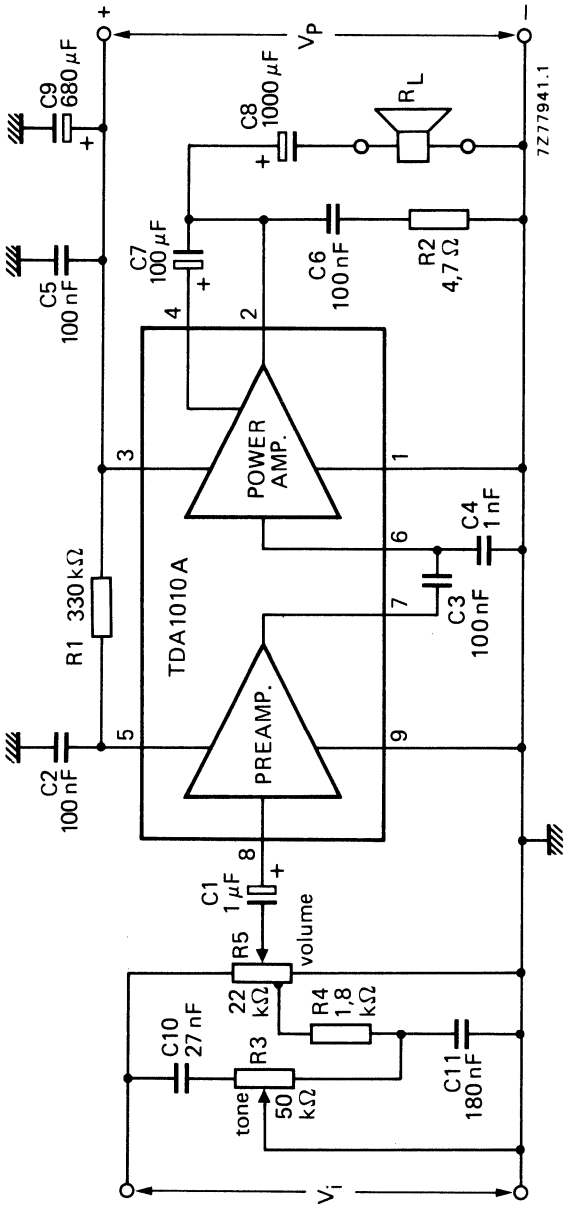


Fig. 9 Complete mono audio amplifier of a car radio.

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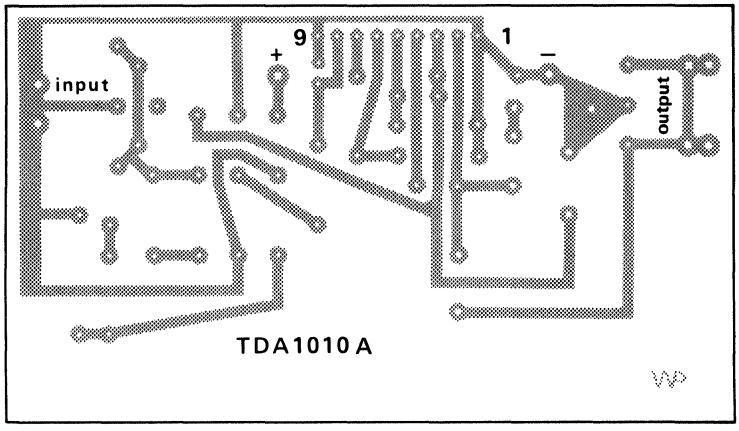


Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

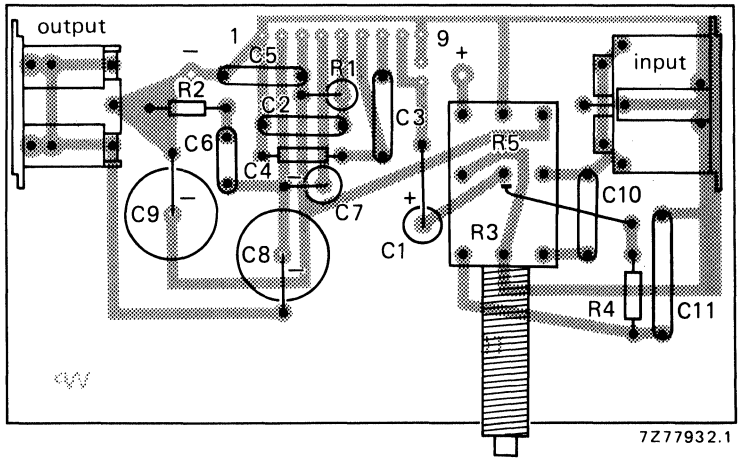


Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

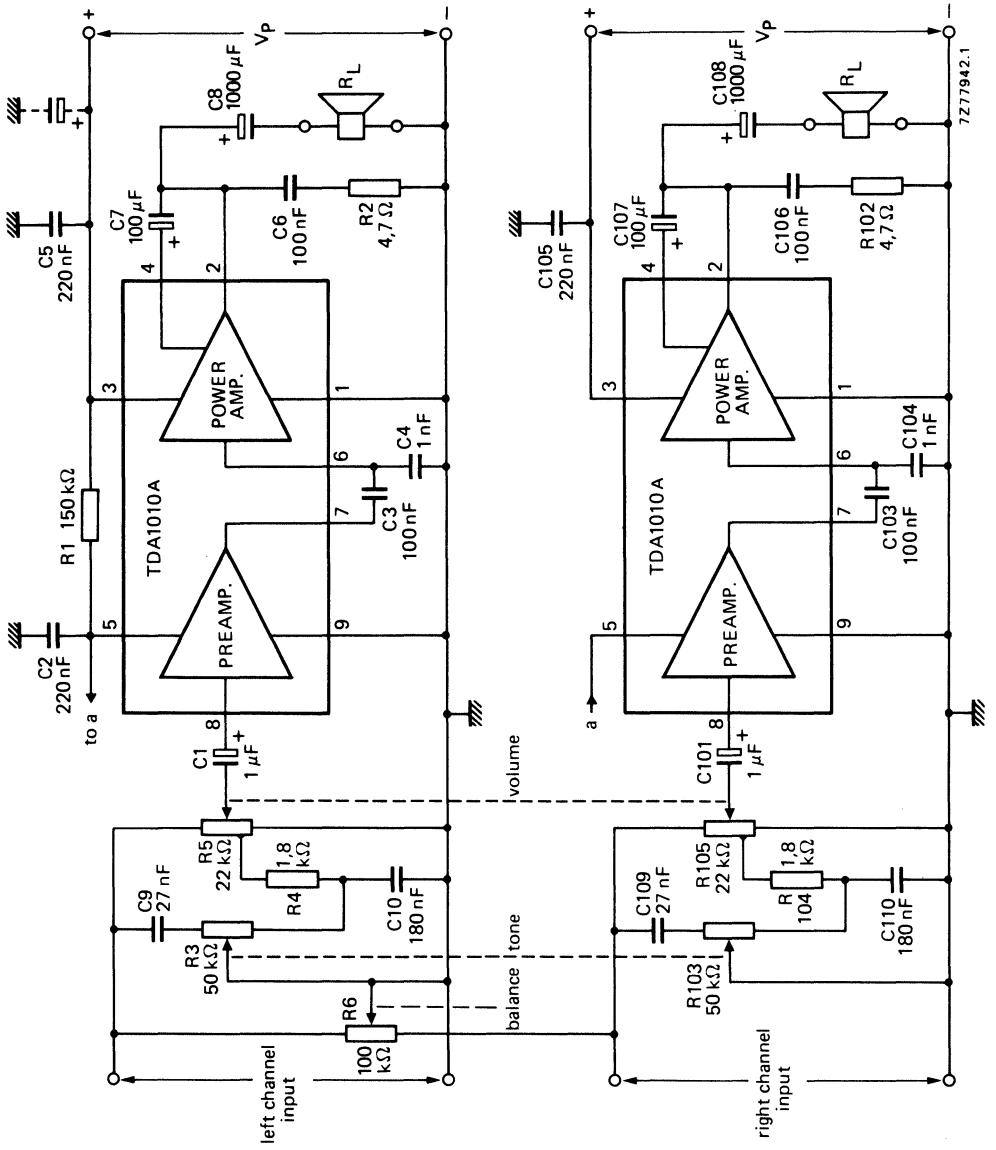


Fig. 12 Complete stereo car radio amplifier.

6

4W Audio Amplifier with DC Volume Control — TDA1013A

The TDA1013A is a monolithic integrated audio amplifier circuit with d.c. volume control in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit very suitable for applications in mains-fed apparatus such as television receivers and record players.

The d.c. volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control can be obtained by means of a variable d.c. voltage between 3.5 and 8 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop gain. This offers an optimum in number of external components, performance and stability.

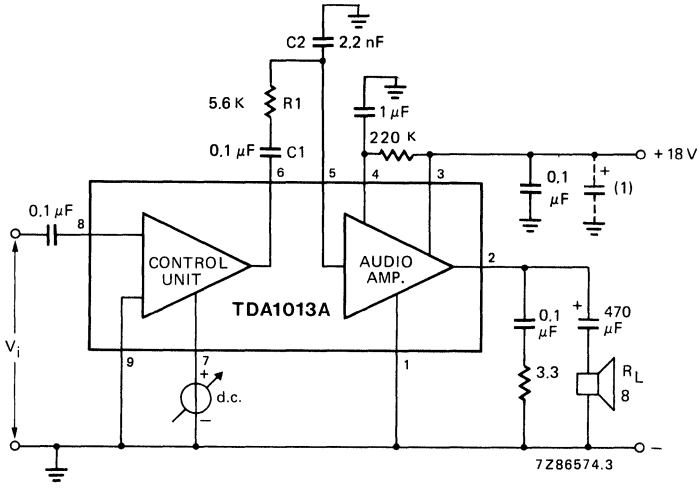
The SIL package (SOT-110B) offers a simple and low-cost heatsink connection.

QUICK REFERENCE DATA

Supply voltage range	V_P	15 to 35	V
Repetitive peak output current	I_{ORM}	max. 1.5	A
Total sensitivity (d.c. control at max. gain) for P_o = 2.5 W	V_i	typ. 55	mV
Audio amplifier			
Output power at d_{tot} = 10% V_P = 18 V; R_L = 8 Ω	P_o	typ. 4.5	W
Total harmonic distortion at P_o = 2.5 W; R_L = 8 Ω	d_{tot}	typ. 0.5	%
Sensitivity for P_o = 2.5 W	V_i	typ. 125	mV
D.C. volume control unit			
Gain control range	ϕ	> 80	dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	V_i	> 1.2	V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ. 55	mV
Input impedance (pin 8)	$\|Z_i\|$	typ. 250	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).



(1) Belongs to power supply.

Fig. 1 Basic application diagram also used as test circuit with R1 = 5.1 kΩ and C1 = 22 nF.

6

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1.5 A
Storage temperature	T_{stg}		−55 to + 150 °C
Crystal temperature	T_j		−25 to + 150 °C
Total power dissipation	see derating curve Fig. 2		

HEATSINK DESIGN

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C (max.); T_j = 150 °C (max); for a 4 W application into an 8 Ω load, the maximum dissipation is about 2.5 W.
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2.5} = 36\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 − (9 + 1) = 26 K/W.

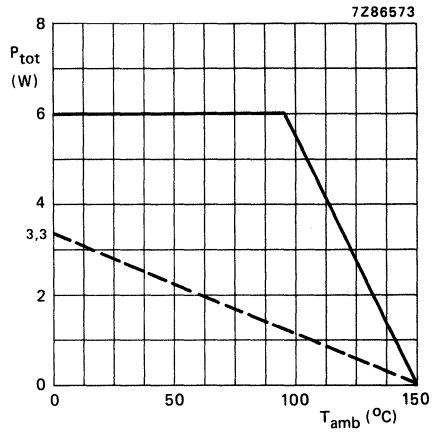


Fig. 2 Power derating curve.
——— infinite heatsink;
– – – without heatsink.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

Supply voltage	V_P	typ.	18	V
			15 to 35	V
Total quiescent current	I_{tot}	typ.	35	mA
Noise output voltage (see also note)	V_n	<	1.4	mV
Total sensitivity (d.c. control at maximum gain) for P_o = 2.5 W	V_i		38 to 69	mV
		typ.	55	mV
Frequency response (–3 dB)	f		35 Hz to 20	kHz
Audio amplifier				
Repetitive peak output current	I_{ORM}	<	1.5	A
Output power at d_{tot} = 10%	P_o	>	4	W
		typ.	4.5	W
Total harmonic distortion at P_o = 2.5 W	d_{tot}	typ.	0.5	%
		<	1	%
Voltage gain	G_v	typ.	30	dB
Sensitivity for P_o = 2.5 W	V_i	typ.	125	mV
Input impedance (pin 5)	$\|Z_i\|$	>	100	kΩ
		typ.	250	kΩ

Note

Measured in a bandwidth according to IEC 179-curve 'A'; R_S = 5 kΩ and d.c. control at minimum gain.

CHARACTERISTICS (continued)

D.C. volume control unit

Gain control range (see also Fig. 3)	ϕ	>	80 dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	V_i	>	1.2 V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ.	55 mV
Input impedance (pin 8)	$\|Z_i\|$	>	100 kΩ
		typ.	250 kΩ
Output impedance (pin 6)	$\|Z_o\|$	100 to	400 Ω
		typ.	200 Ω

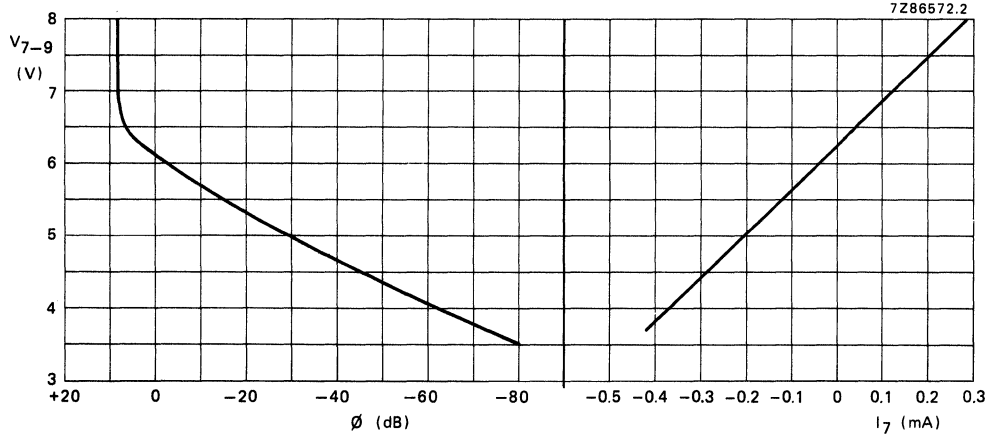


Fig. 3 Typical values gain control; V_i at pin 7.

6

1 to 4W Audio Amplifier TDA1015

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications. Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 18	V
Peak output current	I_{OM}	max.	2,5	A
Output power at d_{tot} = 10%				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,3	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

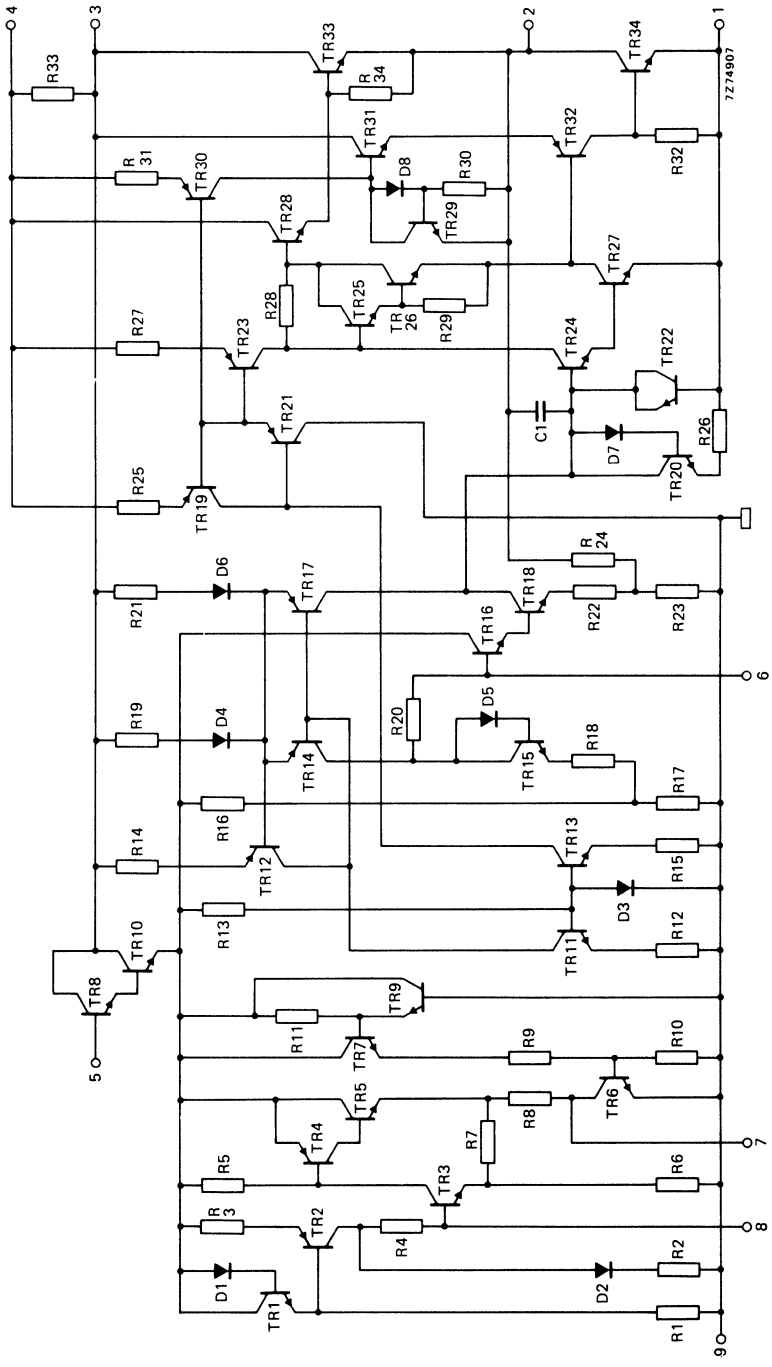


Fig. 1 Circuit diagram.

6

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Peak output current	I_{OM}	max.	2,5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

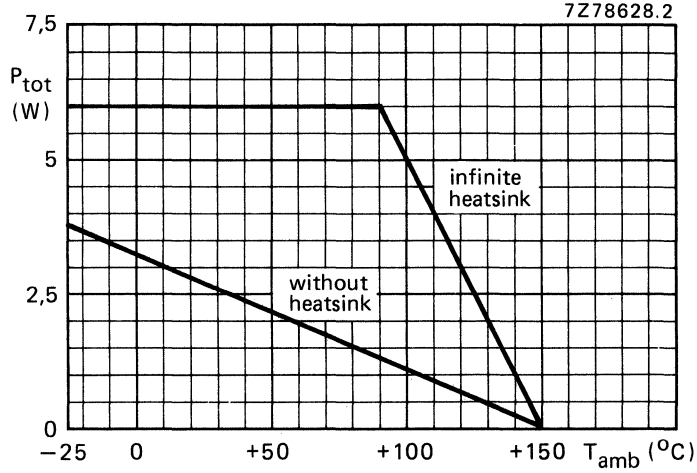


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 45}{1,8} = 58\ K/W.$$

Where $R_{th\ j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P	3,6 to 18	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 25	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,0	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23	dB
power amplifier	G_{v2}	typ. 29	dB
total amplifier	$G_{v\,tot}$	typ. 52 49 to 55	dB dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1,0	% %
Frequency response; −3 dB (note 3)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ. 20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	typ. 0,8	V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 100 Hz	RR	typ. 38	dB

6

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

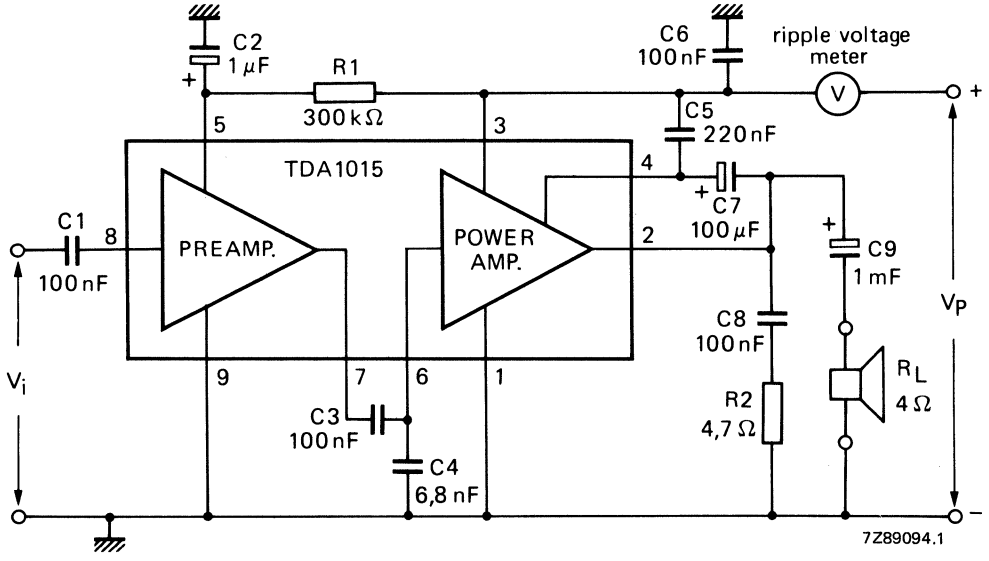


Fig. 3 Test circuit.

APPLICATION INFORMATION

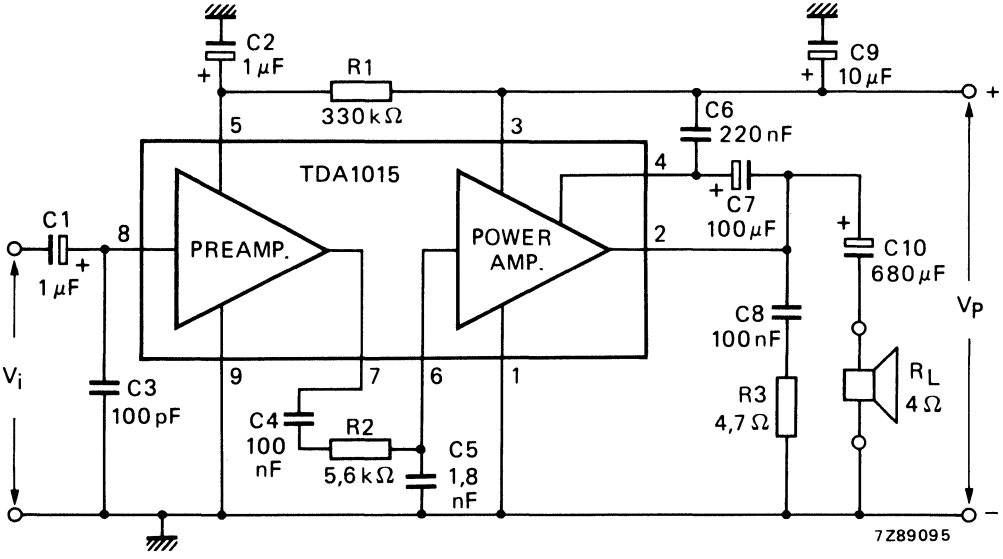


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

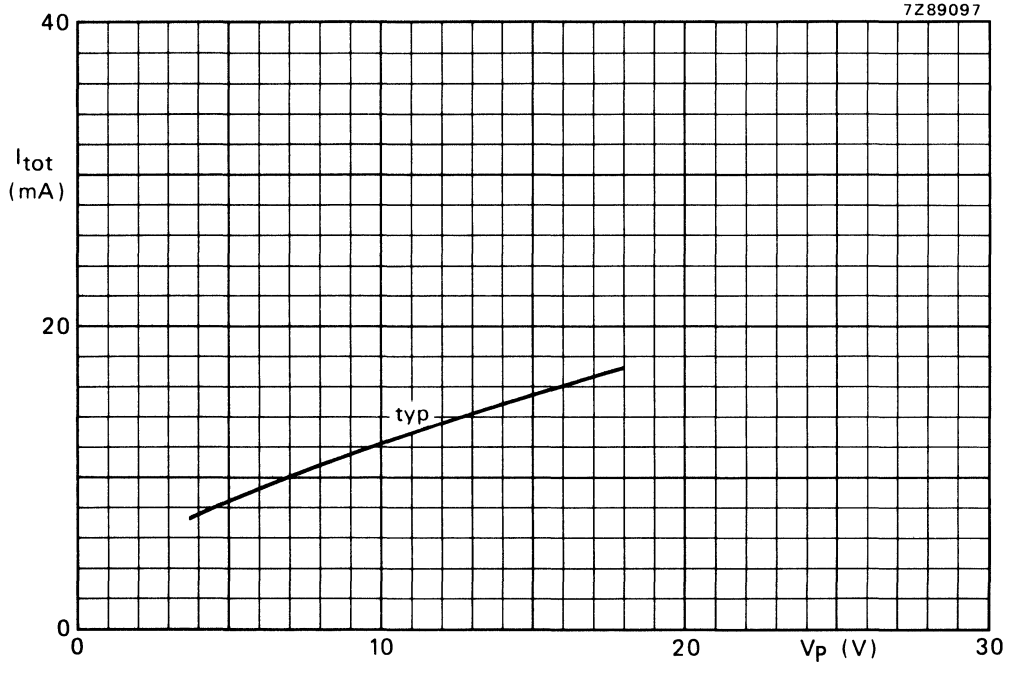


Fig. 5 Total quiescent current as a function of supply voltage.

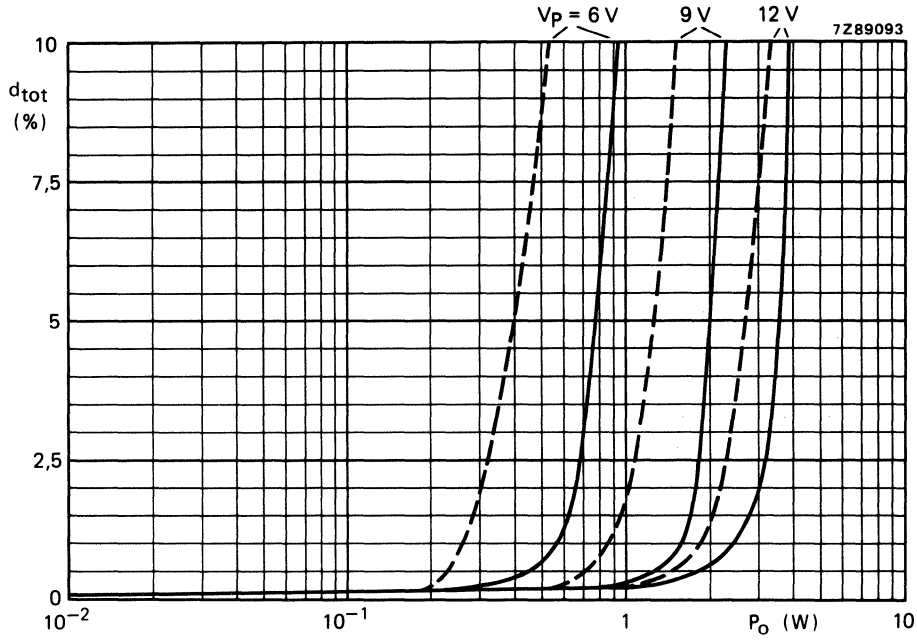


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

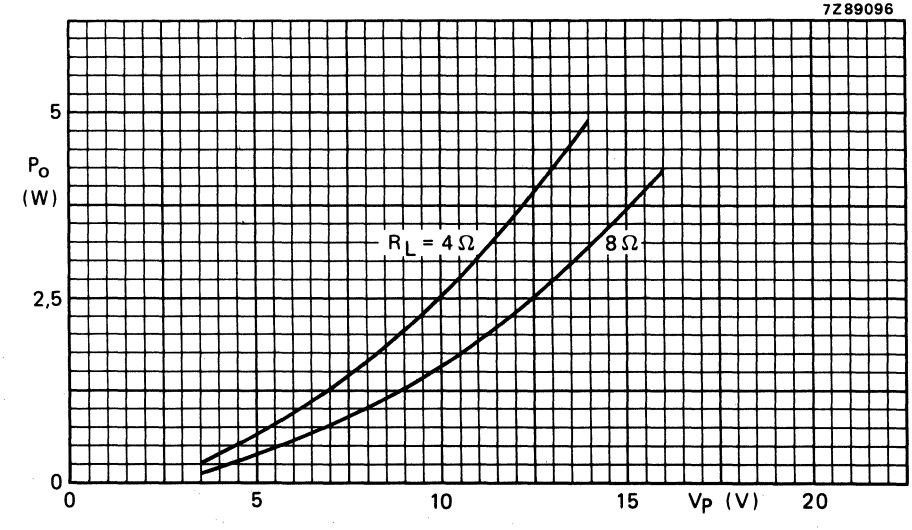


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

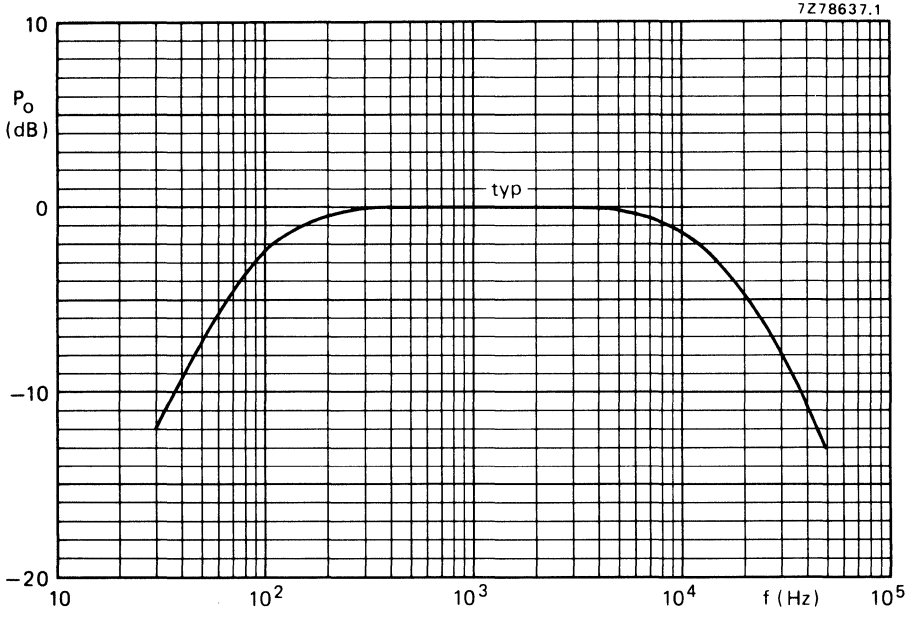


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

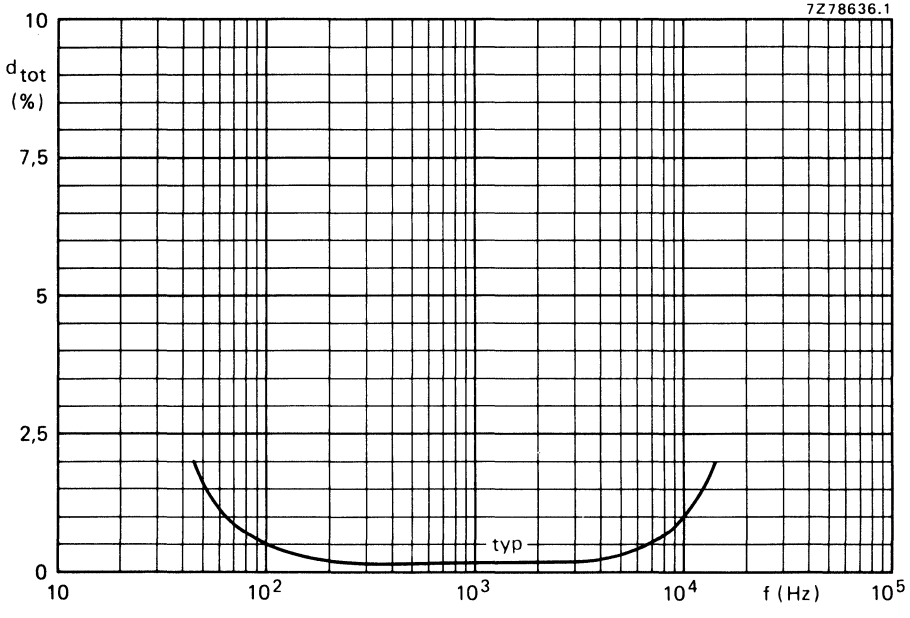


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

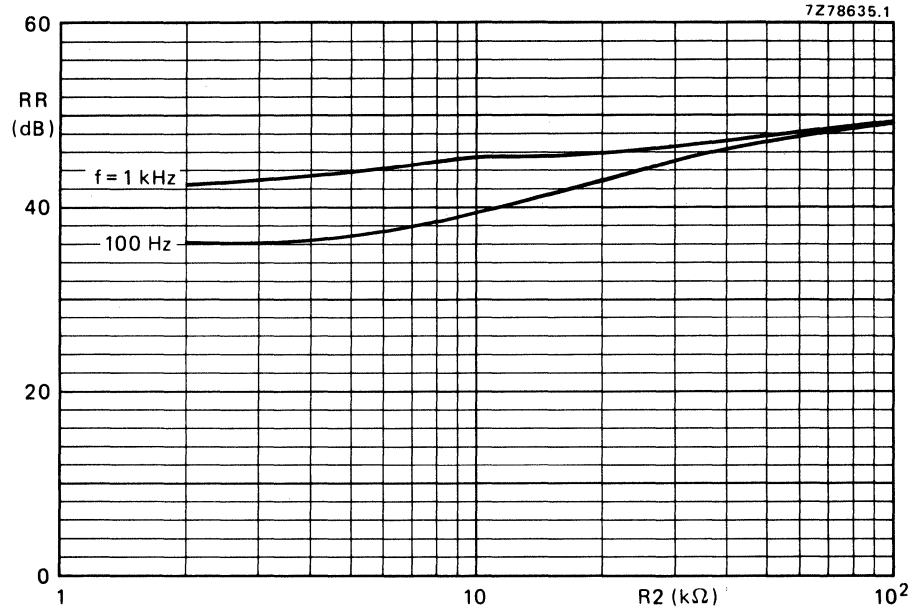


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); R_S = 0; typical values.

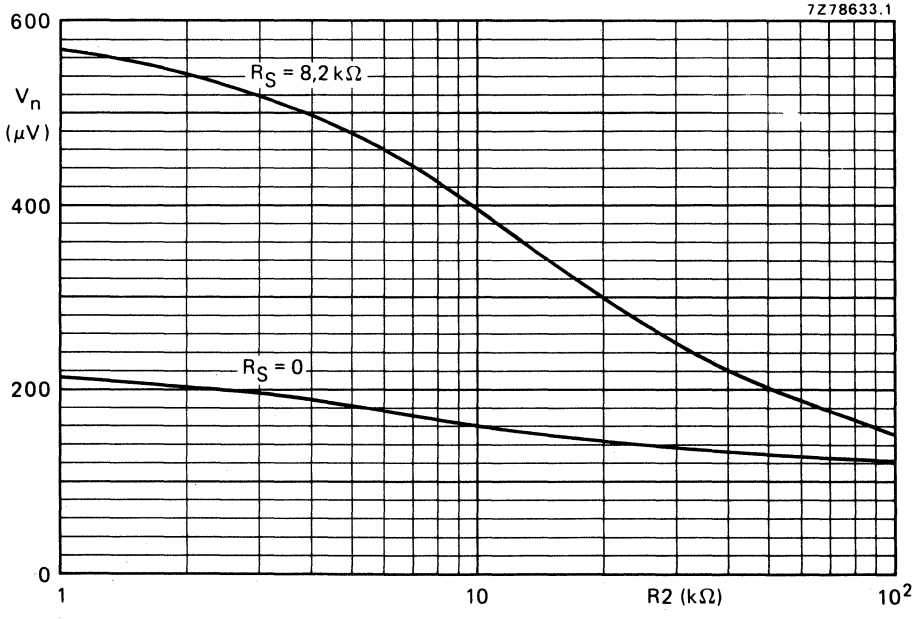


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

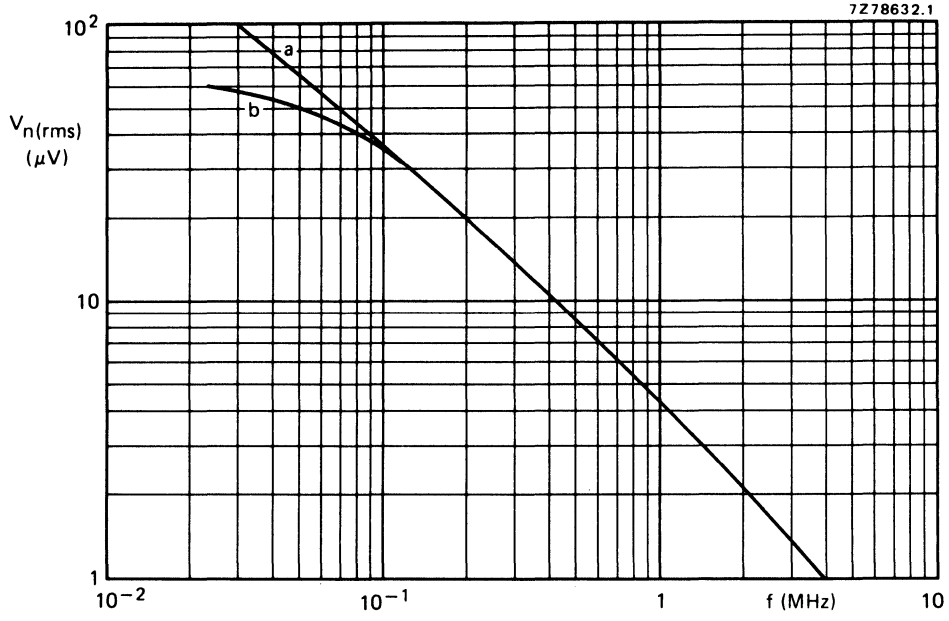


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

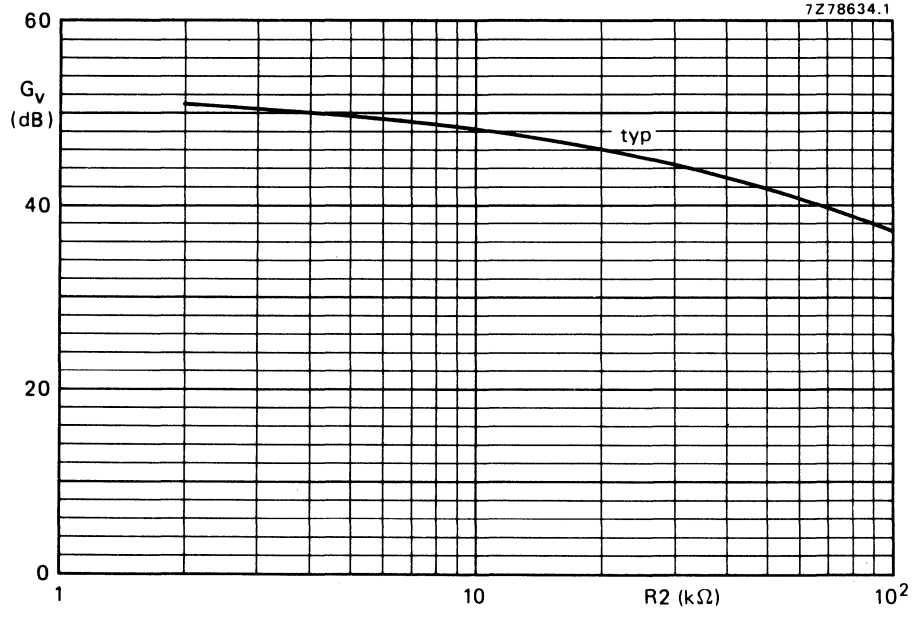


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

12W Audio Amplifier | TDA1020

The TDA1020 is a monolithic integrated 12 W audio amplifier in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a car radio amplifier. At a supply voltage of V_P = 14,4 V, an output power of 7 W can be delivered into a 4 Ω load and 12 W into 2 Ω.

To avoid interferences and car ignition signals coming from the supply lines into the IC, frequency limiting is used beyond the audio spectrum in the preamplifier and the power amplifier.

The maximum supply voltage of 18 V makes the IC also suitable for mains-fed radio receivers, tape recorders or record players. However, if the supply voltage is increased above 18 V (< 45 V), the device will not be damaged (load dump protected). Also a short-circuiting of the output to ground (a.c.) will not destroy the device. Thermal protection is built-in. As a special feature, the circuit has a low stand-by current possibility.

The TDA1020 is pin-to-pin compatible with the TDA1010.

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Output power at d_{tot} = 10% (with bootstrap)			
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	12 W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	7 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,5 W
Output power at d_{tot} = 10% (without bootstrap)			
V_P = 14,4 V; R_L = 4 Ω	P_o	>	4,5 W
Input impedance			
preamplifier (pin 8)	$\|Z_i\|$	typ.	40 kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ.	40 kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	30 mA
Stand-by current	I_{sb}	<	1 mA
Storage temperature range	T_{stg}		−55 to + 150 °C
Crystal temperature	T_c	max.	150 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

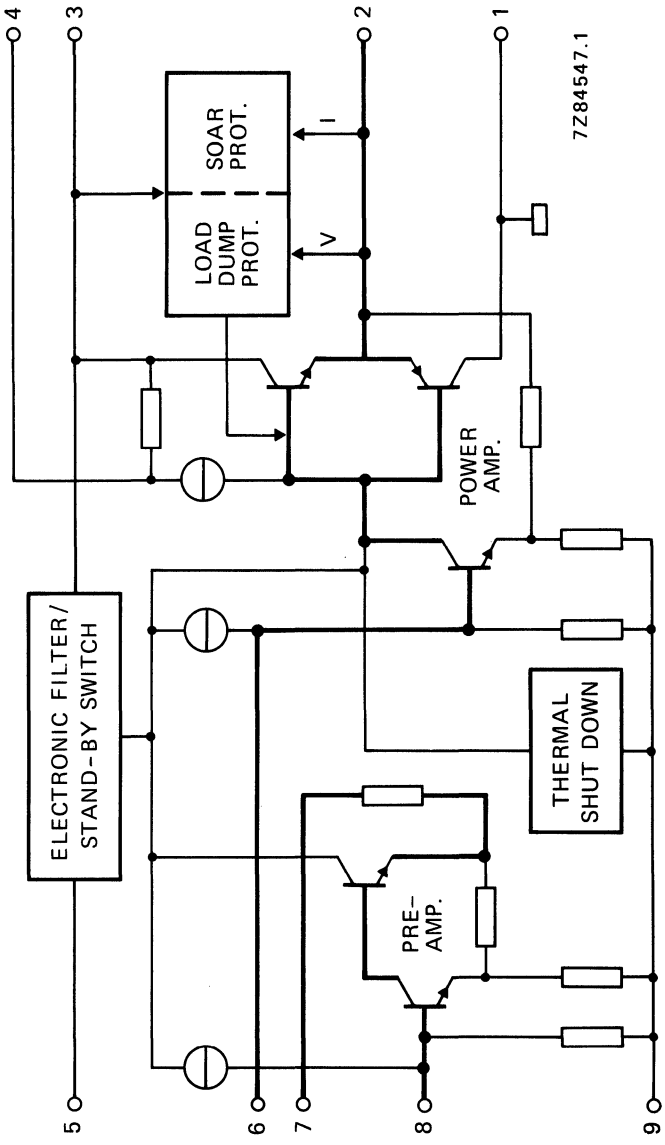


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

PINNING

1. Negative supply (substrate)
2. Output power stage
3. Positive supply (V_P)
4. Bootstrap
5. Ripple rejection filter
6. Input power stage
7. Output preamplifier
8. Input preamplifier
9. Negative supply

6

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 3)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; load dump	V_P	max.	45 V
Non-repetitive peak output current	I_{OSM}	max.	6 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C
Short-circuit duration of load behind output electrolytic capacitor at 1 kHz sine-wave overdrive (10 dB); V_P = 14,4 V	t_{sc}	max.	100 hours

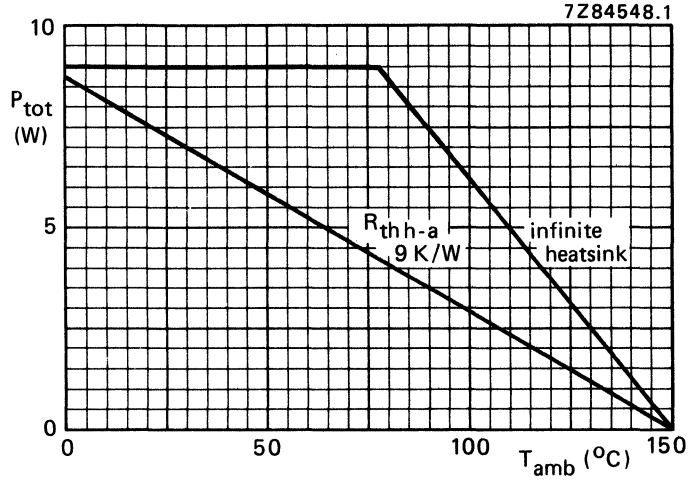


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 8 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

10 W in 2 Ω at V_P = 14,4 V
maximum sine-wave dissipation: 5,2 W
T_{amb} = 60 °C maximum

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{5,2} = 17,3\ K/W$$

Since $R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} = 8$ K/W, $R_{th\ h\text{-}a} = 17,3 - 8 \approx 9$ K/W.

D.C. CHARACTERISTICS

Supply voltage range (pin 3)	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Total quiescent current			
at V_P = 14,4 V	I_{tot}	typ.	30 mA
at V_P = 18 V	I_{tot}	typ.	40 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; unless otherwise specified; see also Fig. 3

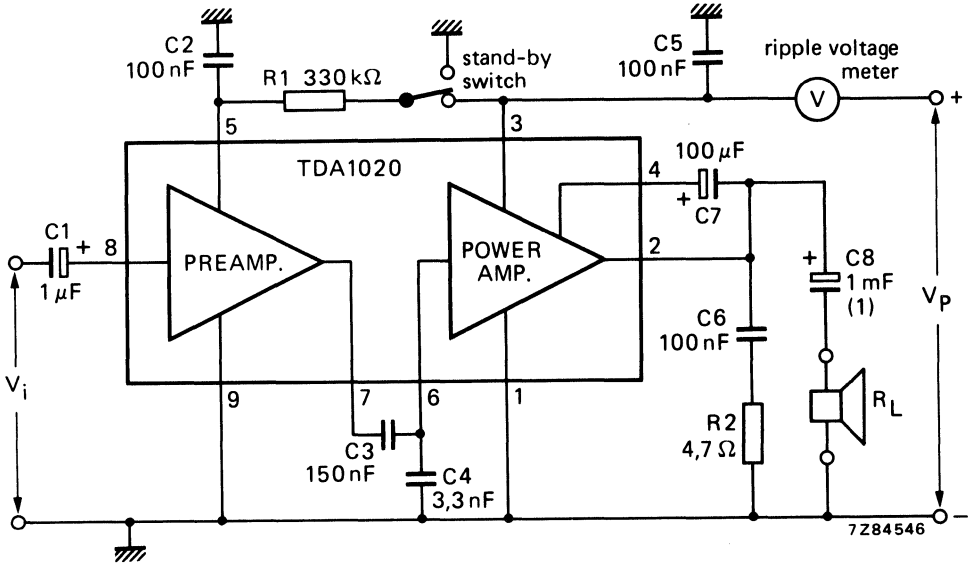
Output power at d_{tot} = 10%; with bootstrap (note 1)			
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	12 W
V_P = 14,4 V; R_L = 4 Ω	P_o	>	6 W
		typ.	7 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,5 W
Output power at d_{tot} = 1%; with bootstrap (note 1)			
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9,5 W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3 W
Output voltage (r.m.s. value)			
R_L = 1 kΩ; d_{tot} = 0,5%	$V_{o(rms)}$	typ.	5 V
Output power at d_{tot} = 10%; without bootstrap	P_o	>	4,5 W
Voltage gain			
preamplifier (note 2)	G_{v1}	typ.	17,7 dB
			16,7 to 18,7 dB
power amplifier	G_{v2}	typ.	29,5 dB
			28,5 to 30,5 dB
total amplifier	$G_{v\,tot}$	typ.	47 dB
			46,2 to 48,2 dB
Input impedance			
preamplifier	$\|Z_i\|$	typ.	40 kΩ
			28 to 52 kΩ
power amplifier	$\|Z_i\|$	typ.	40 kΩ
			28 to 52 kΩ
Output impedance			
preamplifier	$\|Z_o\|$	typ.	2,0 kΩ
			1,4 to 2,6 kΩ
power amplifier	$\|Z_o\|$	typ.	50 mΩ
Output voltage (r.m.s. value) at d_{tot} = 1%			
preamplifier (note 2)	$V_{o(rms)}$	>	1 V
		typ.	1,5 V
Frequency response	B		50 Hz to 25 kHz
Noise output voltage (r.m.s. value; note 3)			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,3 mV
		<	0,5 mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ.	0,5 mV
		<	1,0 mV

6

Ripple rejection (note 4)			
at f = 100 Hz; C2 = 1 μF	RR	typ.	44 dB
at f = 1 kHz to 10 kHz	RR	>	48 dB
		typ.	54 dB
Bootstrap current at onset of clipping (pin 4)			
R_L = 4 Ω and 2 Ω	I_4	typ.	40 mA
Stand-by current (note 5)	I_{sb}	<	1 mA
Crystal temperature for −3 dB gain	T_c	>	150 °C

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 40 kΩ.
3. Measured according to IEC curve-A.
4. Maximum ripple amplitude is 2 V; input is short-circuited.
5. Total current when disconnecting pin 5 or short-circuited to ground (pin 9).
6. The tab must be electrically floating or connected to the substrate (pin 9).



(1) With R_L = 2 Ω, preferred value of C8 = 2200 μF.

Fig. 3 Test circuit.

2 x 12W Audio Amplifier — TDA1510

The TDA1510 is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6 Ω). At a supply voltage V_P = 14,4 V, an output power of 24 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Special features are:

- flexibility in use – stereo as well as mono BTL
- high output power
- low offset voltage at the output (important for BTL)
- large useable gain variation
- very good ripple rejection
- load dump protection
- a.c. short-circuit safe to ground
- thermal protection
- internal limited bandwidth for high frequencies
- low stand-by current possibility, to simplify required switches
- low number and small sized external components
- high reliability

QUICK REFERENCE DATA

Supply voltage range (operating)	V_P		6 to 18	V
Supply voltage (non-operating)	V_P	max.	28	V
Supply voltage (non-operating; load dump protection)	V_P	max.	45	V
Repetitive peak output current	I_{ORM}	max.	4	A
Total quiescent current	I_{tot}	typ.	75	mA
Stand-by current	I_{sb}	<	2	mA
Switch-on current	I_{so}	typ.	0,35	mA
Input impedance	$\lvert Z_i \rvert$	>	1	MΩ
Storage temperature range	T_{stg}		−55 to + 150	°C
Crystal temperature	T_c	max.	150	°C
Bridge tied load application (BTL)	V_P	= 14,4	13,2	V
Output power at R_L = 4 Ω (with bootstrap)				
d_{tot} = 0,5%	P_o	typ. 18	15	W
d_{tot} = 10%	P_o	typ. 24	20	W
Supply voltage ripple rejection; R_S = 0; f = 1 kHz	RR	typ. 50	50	dB
D.C. output offset voltage between the outputs	$\lvert \Delta V_{5\text{-}9} \rvert$	< 50	50	mV
Stereo application				
Output power at d_{tot} = 10% (with bootstrap)				
R_L = 4 Ω	P_o	typ. 7	6	W
R_L = 2 Ω	P_o	typ. 12	10	W
Output power at **d_{tot} = 0,5%** (with bootstrap)				
R_L = 4 Ω	P_o	typ. 5,5	4,5	W
R_L = 2 Ω	P_o	typ. 9,0	7,5	W
Channel separation	α	> 40	40	dB
Noise output voltage; R_S = 10 kΩ; according to IEC curve-A	V_n	typ. 0,2	0,2	mV

PACKAGE OUTLINE

13-lead SIL; plastic power (SOT-141B).

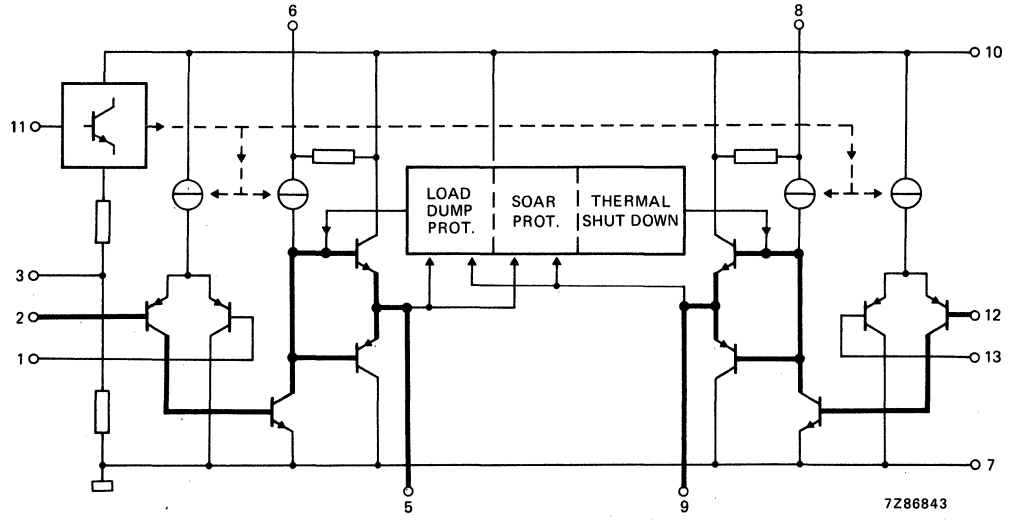


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths. Pin 4 is internally connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; during 50 ms (load dump protection)	V_P	max.	45 V
Peak output current	I_{OM}	max.	6 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C

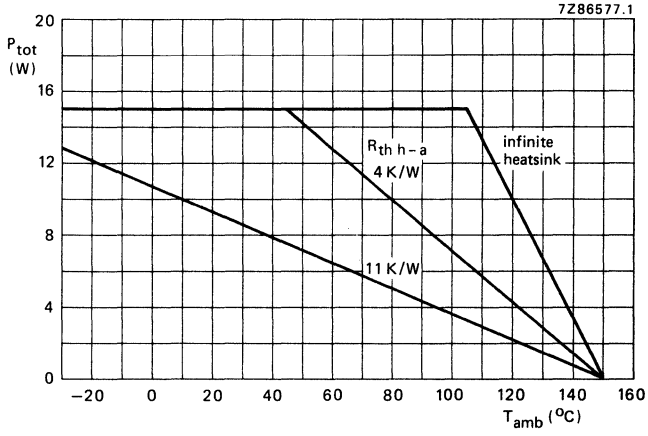


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)
maximum sine-wave dissipation: 12 W
T_{amb} = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150 - 65}{12} - 3 = 4\ \text{K/W}.$$

2 x 7 W stereo (4 Ω)
maximum sine-wave dissipation: 6 W
T_{amb} = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150 - 65}{6} - 3 = 11\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range (pin 10)	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Total quiescent current	I_{tot}	typ. <	75 mA 150 mA
Stand-by current	I_{sb}	<	2 mA
Switch-on current (pin 11) at $V_{11} \leqslant V_{10}$ (note 1)	I_{so}	typ. <	0,35 mA 0,8 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

Bridge tied load application (BTL); see Fig. 3

Output power at R_L = 4 Ω (with bootstrap)

V_P = 14,4 V; **d_{tot} = 0,5%**	P_o	> typ.	15,5 W 18,0 W
V_P = 14,4 V; d_{tot} = 10%	P_o	> typ.	20 W 24 W
V_P = 13,2 V; **d_{tot} = 0,5%**	P_o	typ.	15 W
V_P = 13,2 V; d_{tot} = 10%	P_o	typ.	20 W
Open loop voltage gain	G_o	typ.	75 dB
Closed loop voltage gain (note 2)	G_c	typ.	40 (± 0,5) dB
Frequency response at −3 dB (note 3)	B	20 Hz to	min. 20 kHz
Input impedance (note 4)	$\|Z_i\|$	>	1 MΩ
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. <	0,35 mV 0,8 mV
R_S = 10 kΩ; according to IEC 179 curve A	V_n	typ.	0,25 mV
Supply voltage ripple rejection (note 5)			
f = 100 Hz	RR	> typ.	42 dB 50 dB
D.C. output offset voltage between the outputs	$\|\Delta_{5\text{-}9}\|$	< typ.	50 mV 2 mV
Loudspeaker protection (if one of the 2 outputs is short-circuited to ground) maximum d.c. voltage (across the load)	$\|\Delta V_{5\text{-}9}\|$	<	1 V
Power bandwidth; −1 dB; **d_{tot} = 0,5%**	B	30 Hz to	40 kHz

Stereo application; see Fig. 4

Output power at d_{tot} = 10%; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	>	6 W
		typ.	7 W
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	12 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	6 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	10 W
Output power at d_{tot} = **0,5%**; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	5,5 W
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9,0 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	4,5 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	7,5 W
Output power at d_{tot} = 10%; without bootstrap			
V_P = 14,4 V; R_L = 4 Ω (notes 6, 8 and 9)	P_o	typ.	6 W
Frequency response; −3 dB (note 3)	B	40 Hz to	min. 20 kHz
Supply voltage ripple rejection (note 5)			
f = 1 kHz	RR	typ.	50 dB
Channel separation; R_S = 10 kΩ; f = 1 kHz	α	>	40 dB
		typ.	50 dB
Closed loop voltage gain (note 7)	G_c	typ.	40 dB
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,15 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,25 mV
R_S = 10 kΩ; according to IEC curve A	V_n	typ.	0,2 mV

6

Notes

1. If $V_{11} > V_{10}$, then I_{11} must be ⩽ 10 mA.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 (or 8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

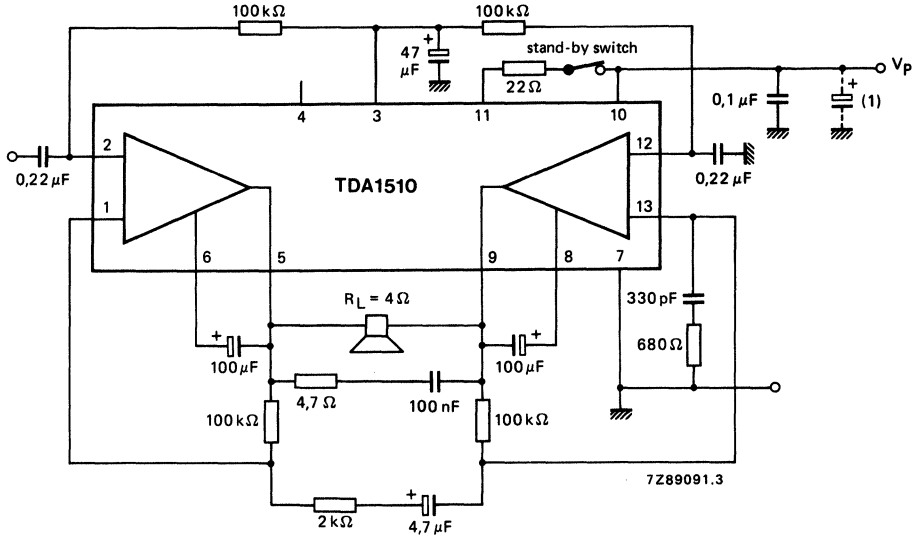


Fig. 3 Test and application circuit bridge tied load (BTL).

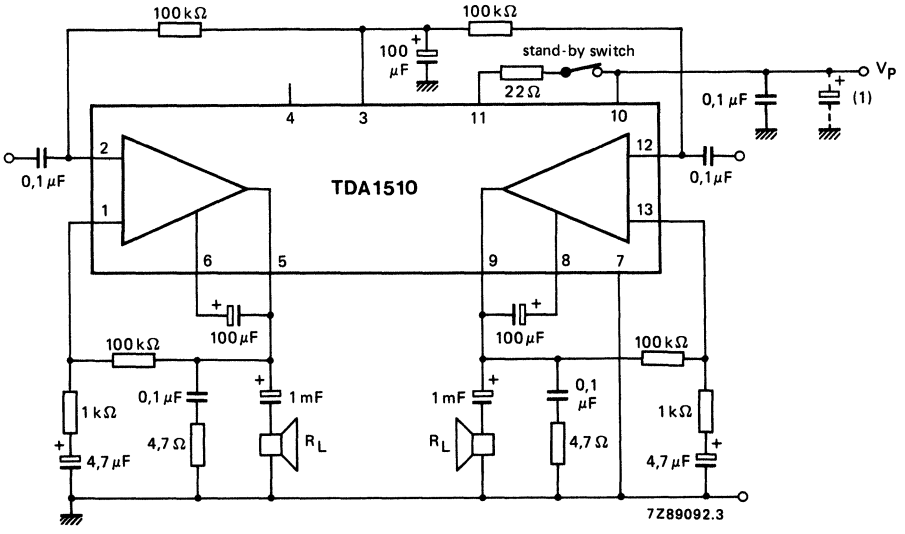


Fig. 4 Test and application circuit stereo mode.

(1) Belongs to power supply.

12 x 20W Audio Amplifier — TDA1512

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA
Output power at d_{tot} = 0,7%			
sine-wave power			
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13 W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7 W
music power			
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21 W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12 W
Closed-loop voltage gain (externally determined)	G_c	typ.	30 dB
Input resistance (externally determined)	R_i	typ.	20 kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72 dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50 dB

6

PACKAGE OUTLINES

TDA1512: 9-lead SIL; plastic power (SOT-131B).
TDA1512Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157B).

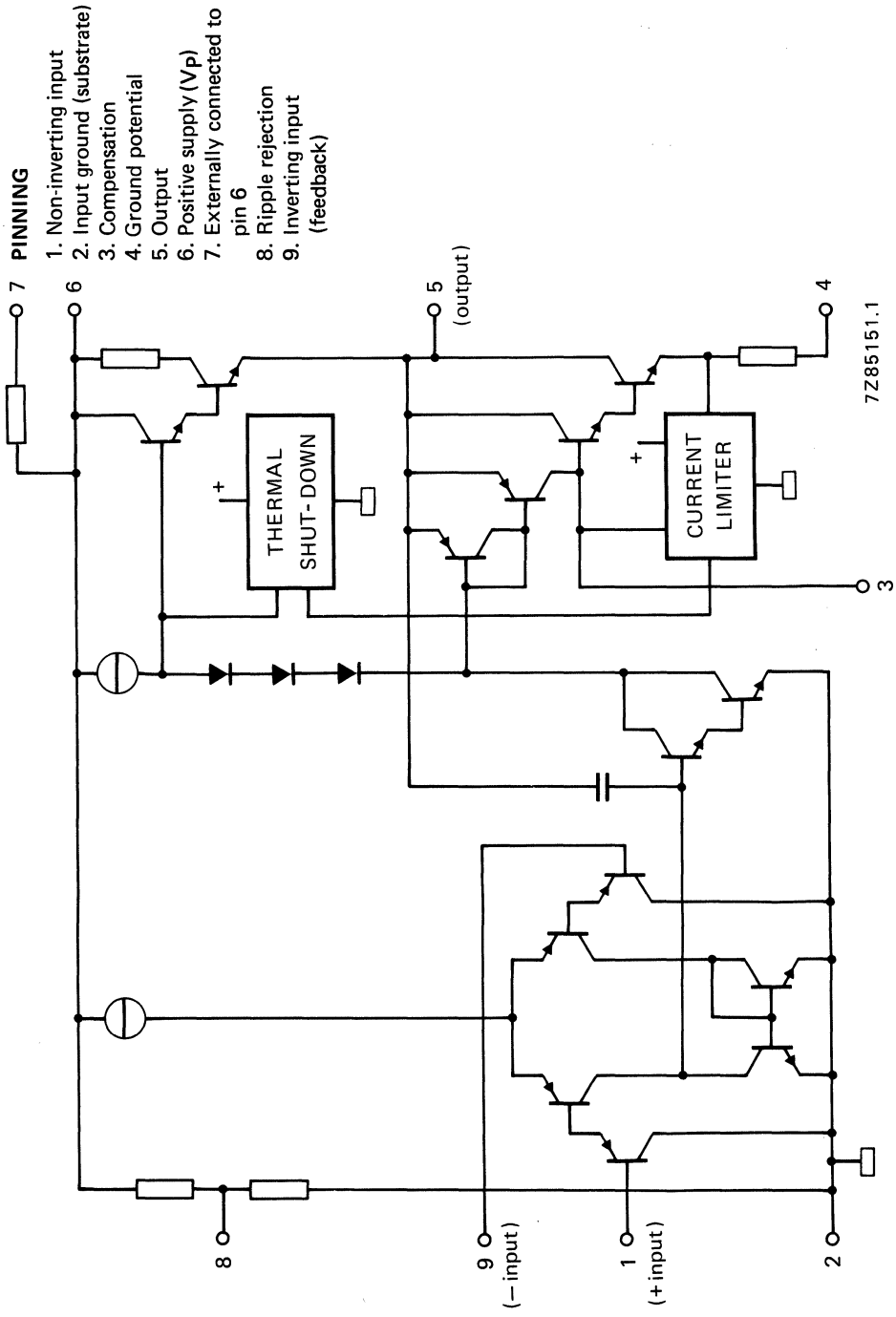
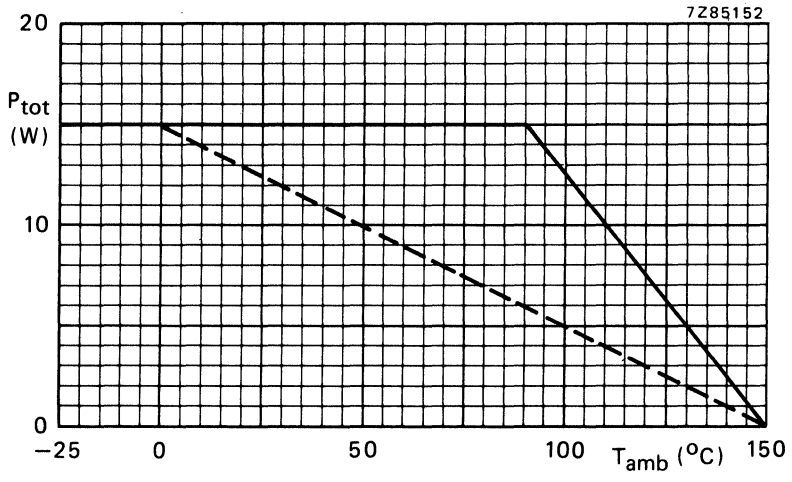


Fig. 1 Simplified internal circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Repetitive peak output current	I_{ORM}	max.	3,2 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100 hours



——— mounted on infinite heatsink.

– – – – mounted on heatsink of 6 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	typ.	3 K/W
		⩽	4 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA

A.C. CHARACTERISTICS

V_P = 25 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,7 %			
R_L = 4 Ω	P_o	typ.	13 W
R_L = 8 Ω	P_o	typ.	7 W
music power at V_P = 32 V			
R_L = 4 Ω; d_{tot} = 0,7 %	P_o	typ.	21 W
R_L = 4 Ω; d_{tot} = 10 %	P_o	typ.	25 W
R_L = 8 Ω; d_{tot} = 0,7 %	P_o	typ.	12 W
R_L = 8 Ω; d_{tot} = 10 %	P_o	typ.	15 W
Power bandwidth; −1,5 dB; d_{tot} = 0,7%	B		40 Hz to 16 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	100 kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ.	16 mV
for P_o = 10 W	V_i	typ.	210 mV
Signal-to-noise ratio			
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	>	68 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76 dB
Ripple rejection at f = 100 Hz	RR	typ.	50 dB
Total harmonic distortion at P_o = 10 W	d_{tot}	typ. <	0,1 % 0,3 %
Output resistance (pin 5)	R_o	typ.	0,1 Ω

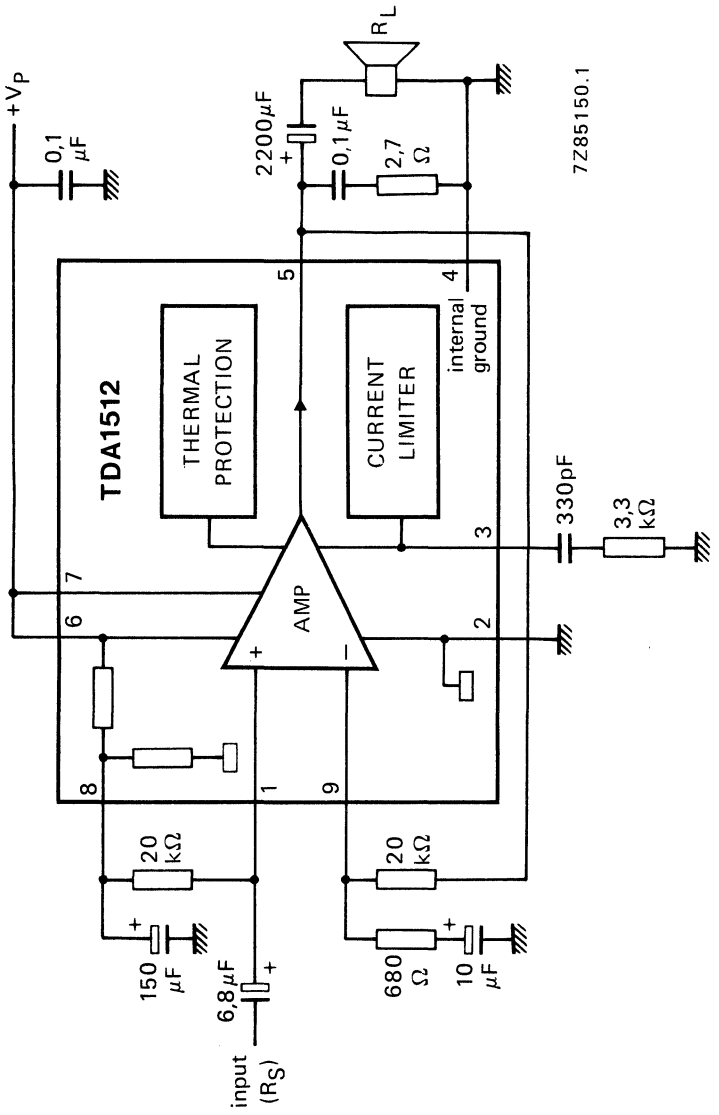


Fig. 3 Test circuit.

6

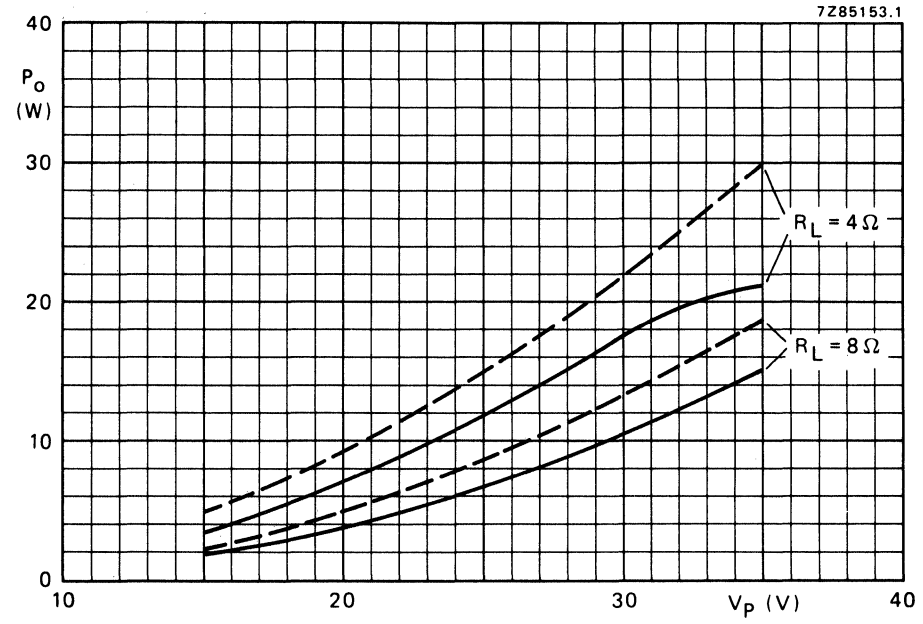


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz;
——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

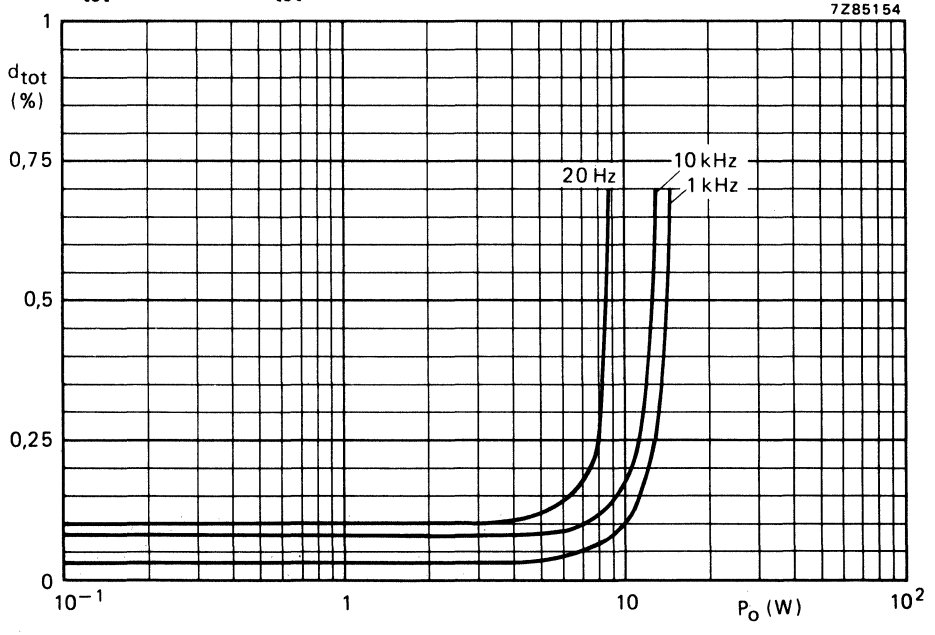


Fig. 5 Total harmonic distortion as a function of the output power.

24W BTL Audio Amplifier — TDA1515

The TDA1515 is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1.6 Ω). At a supply voltage V_P = 14.4 V, an output power of 21 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 11 W into 2 Ω or 2 x 6.5 W into 4 Ω.

Special features are:

- flexibility in use – mono BTL as well as stereo
- high output power
- low offset voltage at the output (important for BTL)
- large usable gain variation
- very good ripple rejection
- internal limited bandwidth for high frequencies
- low stand-by current possibility (typ. 1 μA), to simplify required switches; TTL drive possible
- low number and small sized external components
- high reliability

The following currently required protections are incorporated in the circuit. These protections also have positive influence on reliability in the applications.

- load dump protection
- **a.c. and d.c. short-circuit safe to ground up to V_P = 18 V**
- thermal protection
- speaker protection in bridge configuration
- SOAR protection
- outputs short-circuit safe to ground in BTL
- reverse polarity safe

6

QUICK REFERENCE DATA

Supply voltage range (operating)	V_P		6 to 18	V
Supply voltage (non-operating)	V_P	max.	28	V
Supply voltage (non-operating; load dump protection)	V_P	max.	45	V
Repetitive peak output current	I_{ORM}	max.	4	A
Total quiescent current	I_{tot}	typ.	75	mA
Stand-by current	I_{sb}	typ.	0	μA
Switch-on current	I_{so}	<	100	μA
Input impedance	$\|Z_i\|$	>	1	MΩ
Bridge tied load application (BTL)	V_P	= 14.4	13.2	V
Output power at R_L = 4 Ω (with bootstrap)				
d_{tot} = 0.5%	P_o	typ. 16	14	W
d_{tot} = 10%	P_o	typ. 21	18	W
Supply voltage ripple rejection; R_S = 0 Ω; f = 100 Hz	RR	typ. 50	50	dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5\text{-}9}\|$	< 50	50	mV
Stereo application				
Output power at d_{tot} = 10% (with bootstrap)				
R_L = 4 Ω	P_o	typ. 6.5	6	W
R_L = 2 Ω	P_o	typ. 11	10	W
Output power at **d_{tot} = 0.5%** (with bootstrap)				
R_L = 4 Ω	P_o	typ. 5	4.5	W
R_L = 2 Ω	P_o	typ. 8	7.5	W
Channel separation	α	> 40	40	dB
Noise output voltage; R_S = 10 kΩ; according to IEC curve-A	V_n	typ. 0.2	0.2	mV

PACKAGE OUTLINE 13-lead SIL; plastic power (SOT-141B).

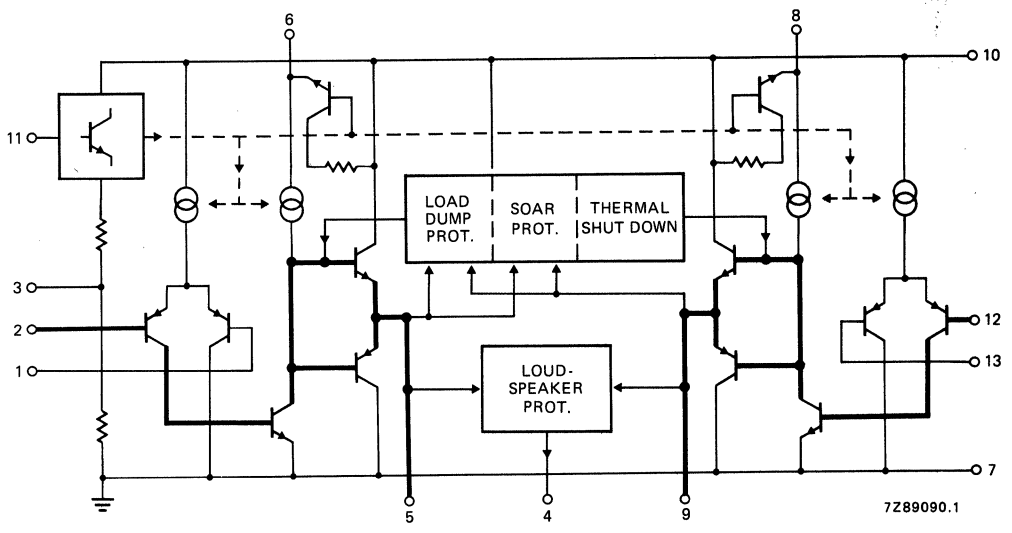


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; during 50 ms (load dump protection)	V_P	max.	45 V
Peak output current	I_{OM}	max.	6 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C
A.C. and d.c. short-circuit safe voltage		max.	18 V
Reverse polarity		max.	10 V

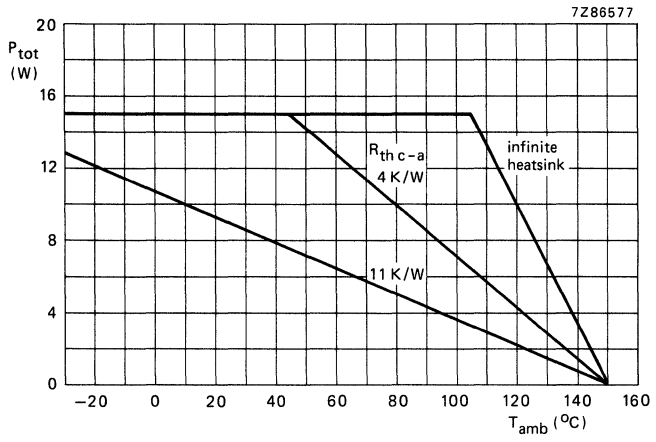


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

21 W BTL (4 Ω) or 2 x 11 W stereo (2 Ω)
maximum sine-wave dissipation: 12 W
T_{amb} = 65 °C maximum

$$R_{th\ h-a} = \frac{150-65}{12} - 3 = 4\ \text{K/W}.$$

2 x 6.5 W stereo (4 Ω)
maximum sine-wave dissipation: 6 W
T_{amb} = 65 °C maximum

$$R_{th\ h-a} = \frac{150-65}{6} - 3 = 11\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range (pin 10)	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Total quiescent current	I_{tot}	typ.	75 mA
Switching level 11 : OFF	V_{11}	<	1.8 V
ON	V_{11}	>	3 V
Impedance between pins 10 and 6; 10 and 8 (stand-by position $V_{11} < 1.8$ V)	$\|Z_{OFF}\|$	>	100 kΩ
Stand-by current at V_{11} = 0 to 0.8 V	I_{sb}	typ. <	1 μA 200 μA
Switch-on current (pin 11) at $V_{11} \leqslant V_{10}$ (note 1)	I_{so}	typ. <	10 μA 100 μA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14.4 V; f = 1 kHz; unless otherwise specified

Bridge tied load application (BTL); see Fig. 3

Output power at R_L = 4 Ω (with bootstrap)			
V_P = 14.4 V; $\mathbf{d_{tot}}$ = **0.5%**	P_o	>	15.5 W
		typ.	16 W
V_P = 14.4 V; d_{tot} = 10%	P_o	>	20 W
		typ.	21 W
V_P = 13.2 V; $\mathbf{d_{tot}}$ = **0.5%**	P_o	typ.	14 W
V_P = 13.2 V; d_{tot} = 10%	P_o	typ.	18 W
Open loop voltage gain	G_o	typ.	75 dB
Closed loop voltage gain (note 2)	G_c	typ.	40 (± 0.5) dB
Frequency response at −3 dB (note 3)	B		20 Hz to min. 20 kHz
Input impedance (note 4)	$\|Z_i\|$	>	1 MΩ
Noise input voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0.2 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0.35 mV
		<	0.8 mV
R_S = 10 kΩ; according to IEC 179 curve A	V_n	typ.	0.25 mV
Supply voltage ripple rejection (note 5)			
f = 100 Hz	RR	>	42 dB
		typ.	50 dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5\text{-}9}\|$	<	50 mV
Loudspeaker protection (all conditions)		typ.	2 mV
maximum d.c. voltage (across the load)	$\|\Delta V_{5\text{-}9}\|$	<	1 V
Power bandwidth; −1 dB; $\mathbf{d_{tot}}$ = **0.5%**	B		30 Hz to 30 kHz

Stereo application; see Fig. 4

Output power at d_{tot} = 10%; with bootstrap (note 6)			
V_P = 14.4 V; R_L = 4 Ω	P_o	>	6 W
		typ.	6.5 W
V_P = 14.4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	11 W
V_P = 13.2 V; R_L = 4 Ω	P_o	typ.	6 W
V_P = 13.2 V; R_L = 2 Ω	P_o	typ.	10 W
Output power at d_{tot} = 0.5%; with bootstrap (note 6)			
V_P = 14.4 V; R_L = 4 Ω	P_o	typ.	5 W
V_P = 14.4 V; R_L = 2 Ω	P_o	typ.	8 W
V_P = 13.2 V; R_L = 4 Ω	P_o	typ.	4.5 W
V_P = 13.2 V; R_L = 2 Ω	P_o	typ.	7.5 W
Output power at d_{tot} = 10%; without bootstrap			
V_P = 14.4 V; R_L = 4 Ω (notes 6, 8 and 9)	P_o	typ.	5.5 W
Frequency response at −3 dB (note 3)	B	40 Hz to min.	20 kHz
Supply voltage ripple rejection (note 5)	RR	typ.	50 dB
Channel separation; R_S = 10 kΩ; f = 1 kHz	α	>	40 dB
		typ.	50 dB
Closed loop voltage gain (note 7)	G_c	typ.	40 dB
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0.15 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0.25 mV
R_S = 10 kΩ; according to IEC curve A	V_n	typ.	0.2 mV

Notes

1. The internal circuit impedance at pin 11 is > 5 kΩ if $V_{11} > V_{10}$.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 (8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

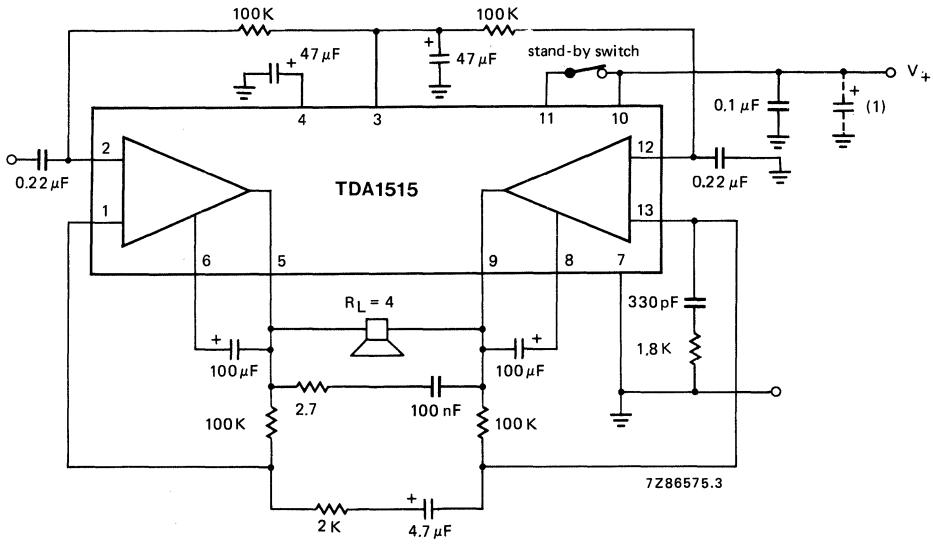


Fig. 3 Test/application circuit bridge tied load (BTL).

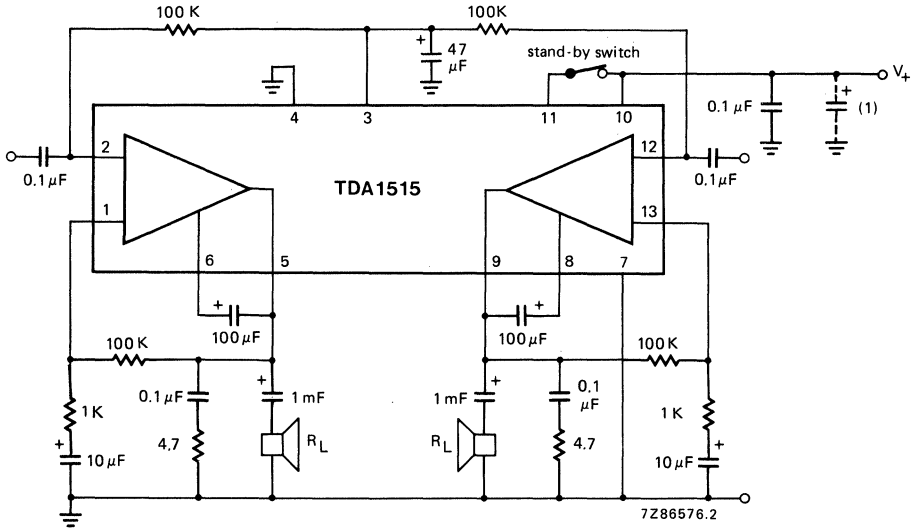


Fig. 4 Test/application circuit stereo.

1. Belongs to power supply.

20W Hi-Fi Audio Amplifier — TDA1520A

GENERAL DESCRIPTION

The TDA1520A is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.

Features

- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected
- Very low internal thermal resistance
- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Complete SOAR protection

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 50	V
Total quiescent current at V_P = 33 V	I_{tot}	typ.	70	mA
Output power at d_{tot} = 0.5% sine-wave power				
V_P = 33 V; R_L = 4 Ω	P_O	typ.	22	W
V_P = 33 V; R_L = 4 Ω	P_O	>	20	W
V_P = 42 V; R_L = 8 Ω	P_O	typ.	20	W
Closed-loop voltage gain (externally determined)	G_c	typ.	30	dB
Input resistance (externally determined by R_{8-1})	R_i	typ.	20	kΩ
Signal-to-noise ratio at P_O = 50 mW	S/N	typ.	76	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	60	dB

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PACKAGE OUTLINE

TDA1520A : 9-lead SIL; plastic power (SOT-131A).
TDA1520AQ: 9-lead SIL-bent-to-DIL; plastic power (SOT-157A).

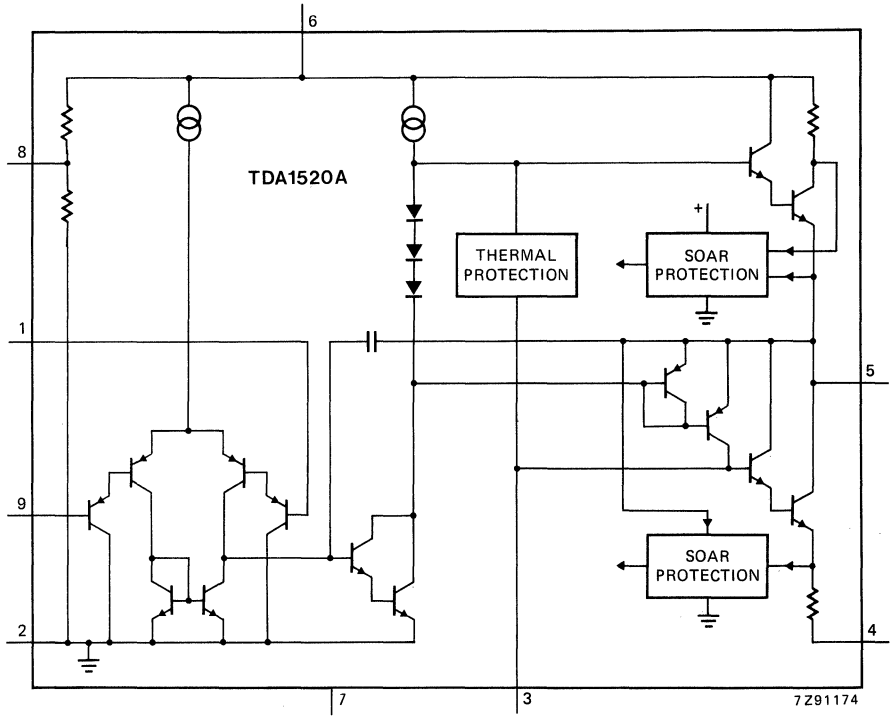


Fig. 1 Simplified internal circuit diagram.

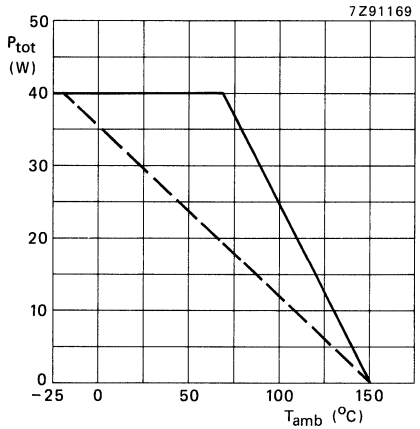
PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (V_P)
7. Not connected
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	50 V
Repetitive peak output current	I_{ORM}	max.	4 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Duration of a.c. short-circuit of load (R_L = 0 Ω) during full-load sine-wave drive at: V_S = ± 20 V (symmetrical) and R_{supply} = 0 Ω; or V_S = 35 V (asymmetrical) and $R_{supply} \geqslant 4$ Ω	t_{sc}	max.	100 hours



——— mounted on infinite heatsink.
– – – mounted on heatsink of 2.3 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	2 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 50	V
Total quiescent current at V_P = 33 V	I_{tot}	typ.	70	mA
		⩽	105	mA
Minimum guaranteed output current (peak value)	I_{ORM}	⩾	3.2	A

A.C. CHARACTERISTICS

V_P = 33 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power				
sine-wave power at d_{tot} = 0.5%				
R_L = 4 Ω	P_o	typ.	22	W
R_L = 4 Ω (Fig. 4)	P_o	>	20	W
R_L = 8 Ω; V_P = 42 V	P_o	typ.	20	W
Power bandwidth at d_{tot} = 0.5% from P_o = 50 mW to 10 W	B	20 Hz to	20	kHz
Voltage gain				
open-loop	G_o	typ.	74	dB
closed-loop	G_c	typ.	30	dB
Internal resistance of pin 1 (at R_{1-8} = ∞)	R_i	>	1	MΩ
Input resistance of test circuit at pin 1 (Fig. 3)	R_i	typ.	20	kΩ
Input sensitivity				
for P_o = 16 W	V_i	typ.	260	mV
Signal-to-noise ratio				
at P_o = 50 mW; R_{source} = 2 kΩ				
f = 20 Hz to 20 kHz; unweighted	S/N	typ.	76	dB
weighted; measured according to IEC 179 (A-curve)	S/N	typ.	80	dB
Ripple rejection at f = 100 Hz; R_S = 0 Ω	RR	typ.	60	dB
Total harmonic distortion at P_o = 16 W	d_{tot}	typ.	0.01	%
Output resistance (pin 5)	R_o	typ.	0.01	Ω
Input offset voltage	V_{5-8}	typ.	1	mV
		<	100	mV
Transient intermodulation distortion				
at P_o = 10 W	d_{TIM}	typ.	0.01	%
Intermodulation distortion at P_o = 10 W	d_{IM}	typ.	0.01	%
Slew rate	SR	typ.	9	V/μs

APPLICATION INFORMATION

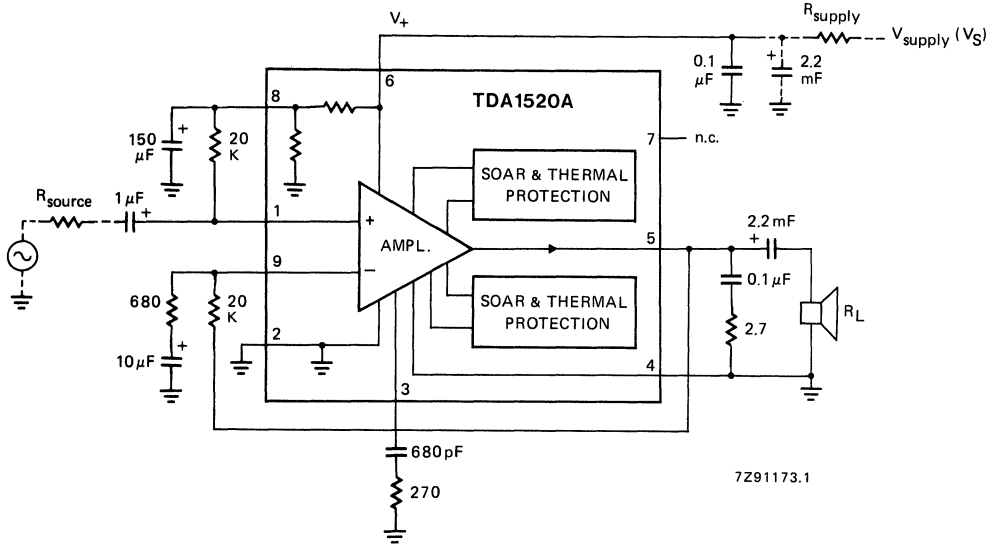


Fig. 3 Test and application circuit.

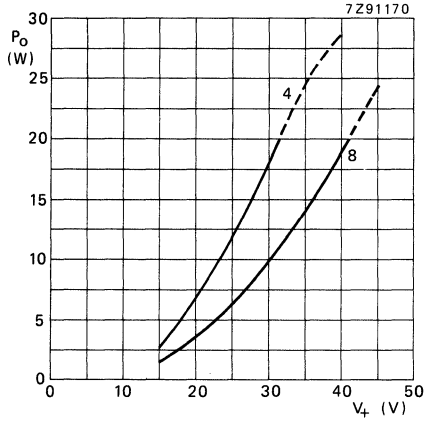


Fig. 4 Output power (P_o) versus supply voltage (V_p) at f = 1 kHz, d_{tot} = 0.5%, G_v = 30 dB.

APPLICATION INFORMATION (continued)

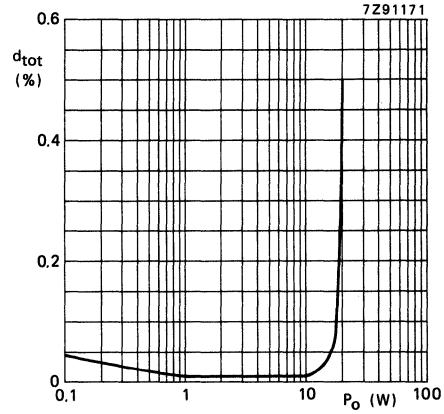


Fig. 5 Total harmonic distortion (d_{tot}) versus output power (P_o) at V_p = 33 V, R_L = 4 Ω, f = 1 kHz.

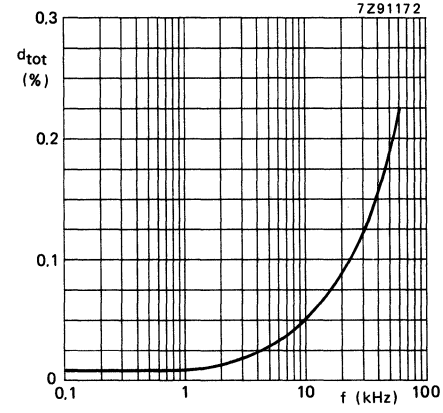


Fig. 6 Total harmonic distortion (d_{tot}) versus operating frequency (f) at V_p = 33 V, R_L = 4 Ω, P_o = 10 W (constant).

5W Audio Output for TV — TDA2611A

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P	6 to 35	V
Repetitive peak output current	I_{ORM}	< 1,5	A
Output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	typ. 4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ. 5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ. 0,3	%
Input impedance	$\lvert Z_i \rvert$	typ. 45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ. 25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ. 55	mV
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

6

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

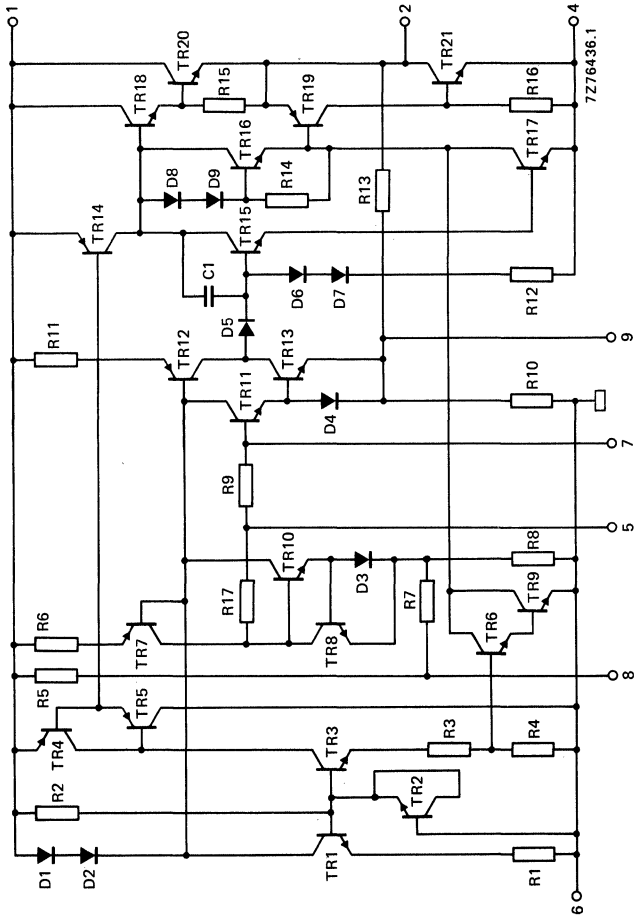


Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C

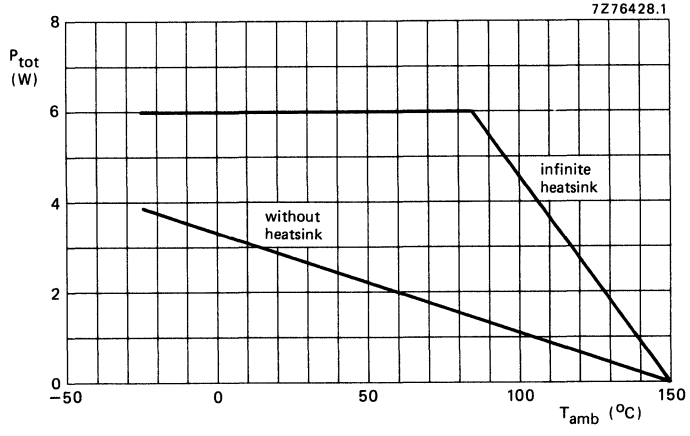


Fig. 2 Power derating curves.

HEATSINK EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C maximum; T_j = 150 °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{2,2} = 41\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 11 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 41 − (11 + 1) = 29 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 18 V; R_L = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	>	4 W
		typ.	4,5 W
V_P = 12 V; R_L = 8 Ω	P_o	typ.	1,7 W
V_P = 8,3 V; R_L = 8 Ω	P_o	typ.	0,65 W
V_P = 20 V; R_L = 8 Ω	P_o	typ.	6 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
Total harmonic distortion at P_o = 2 W	d_{tot}	typ.	0,3 %
		<	1 %
Frequency response		>	15 kHz
Input impedance	$\|Z_i\|$	typ.	45 kΩ *
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2 mV
		<	0,5 mV
Sensitivity for P_o = 2,5 W	V_i	typ.	55 mV
			44 to 66 mV

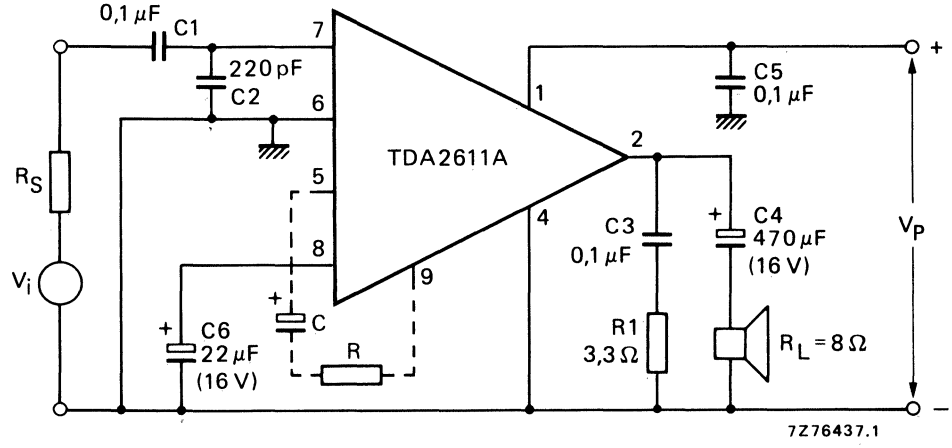


Fig. 3 Test circuit; pin 3 not connected.

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

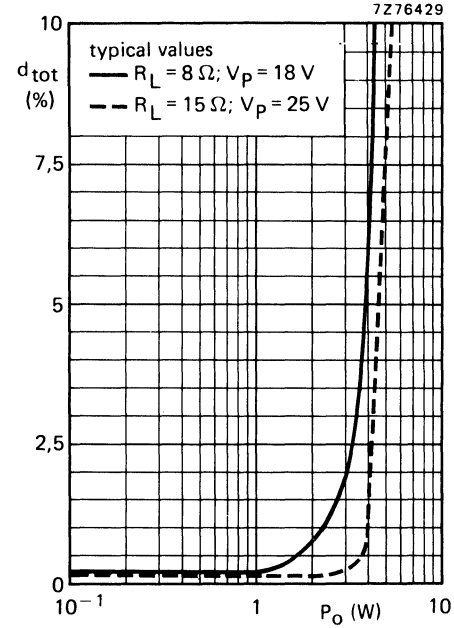


Fig. 4 Total harmonic distortion as a function of output power.

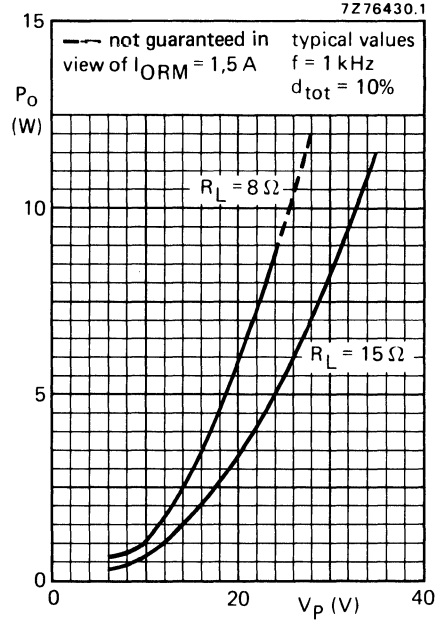


Fig. 5 Output power as a function of supply voltage.

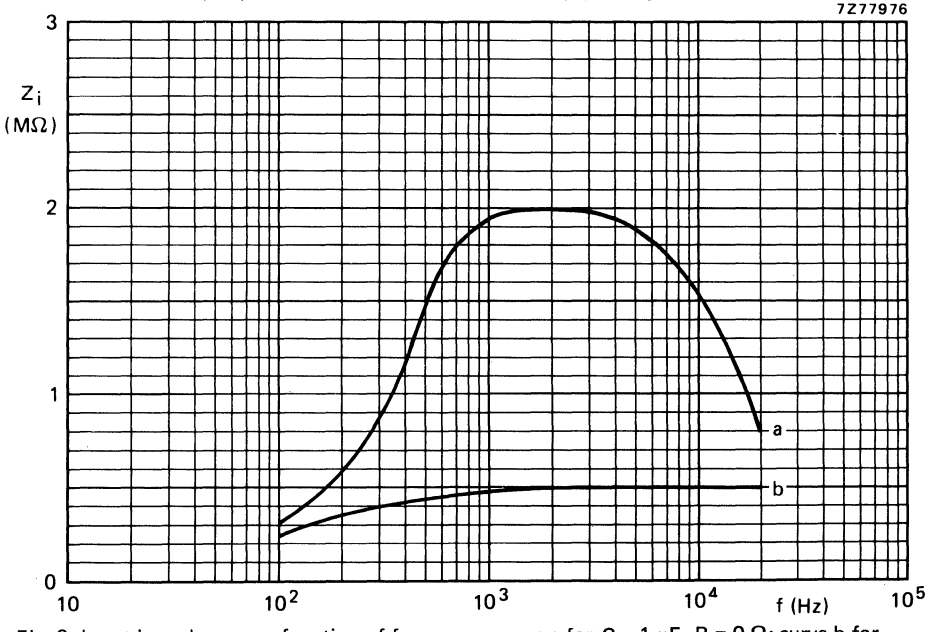


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

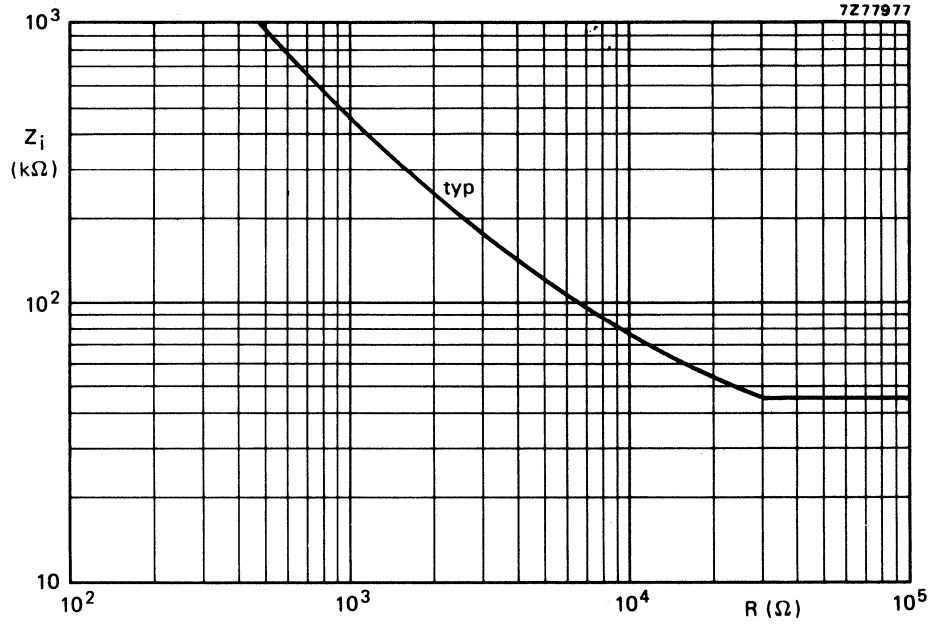


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

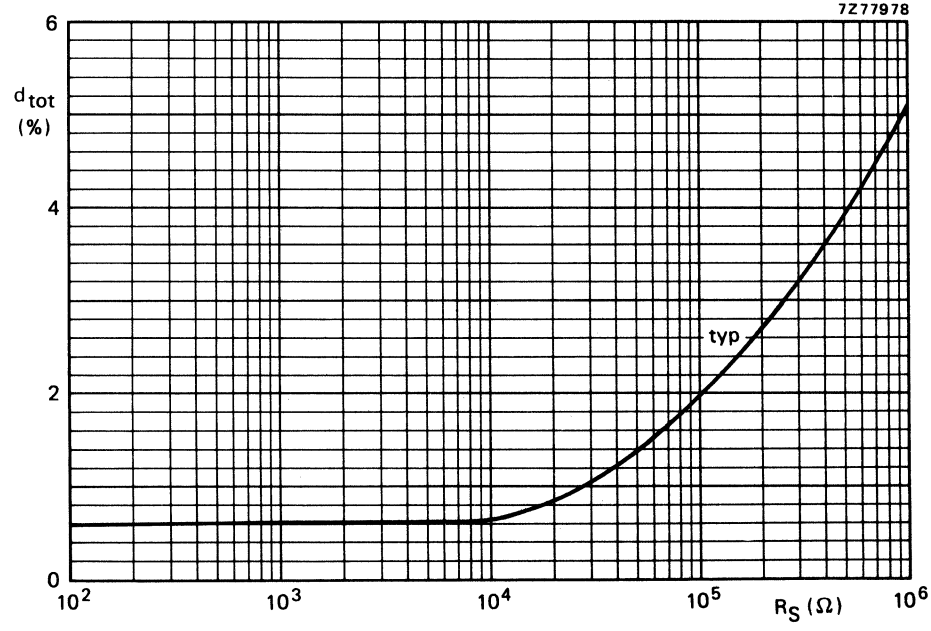
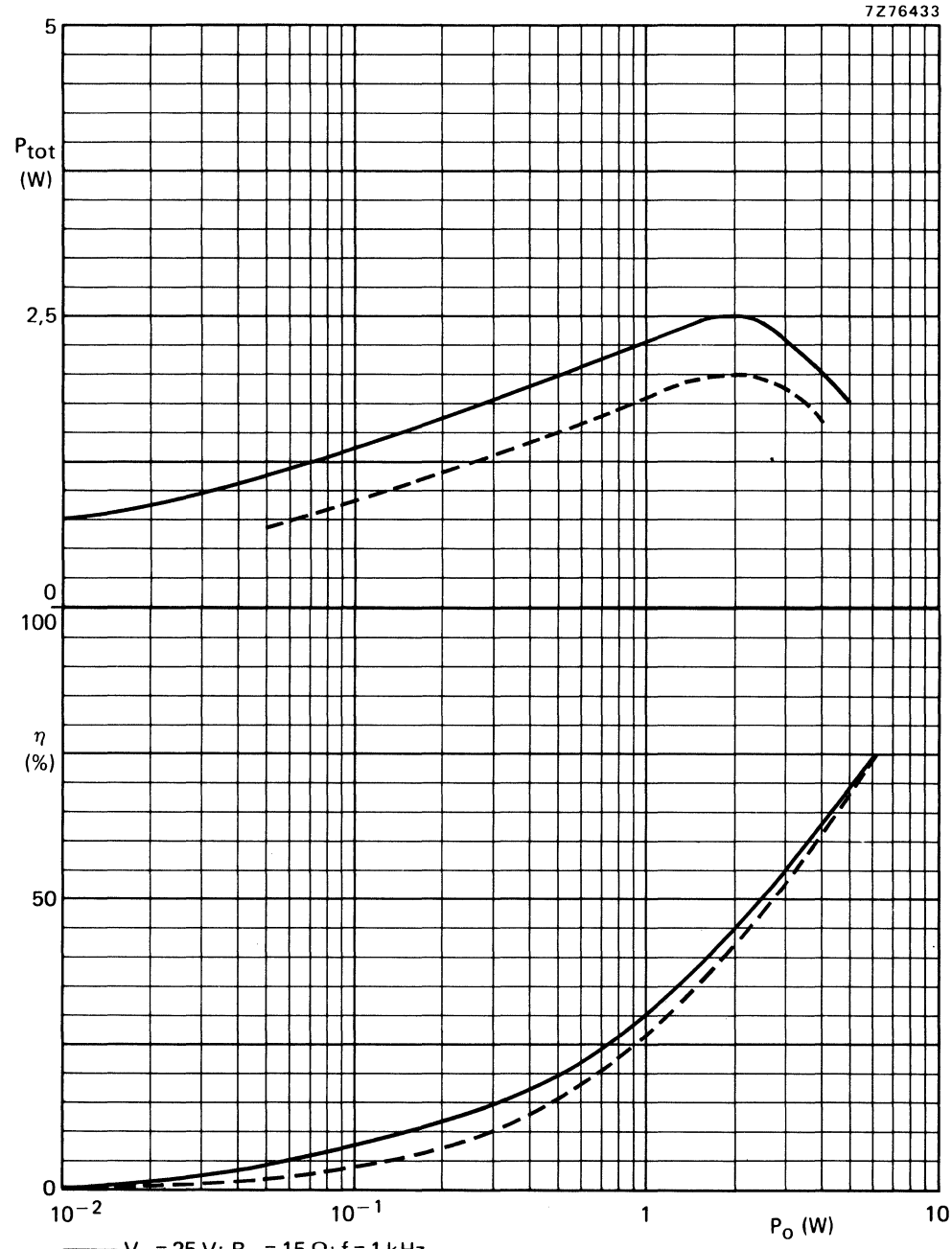


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.



—— V_P = 25 V; R_L = 15 Ω; f = 1 kHz

— — V_P = 18 V; R_L = 8 Ω; f = 1 kHz

Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

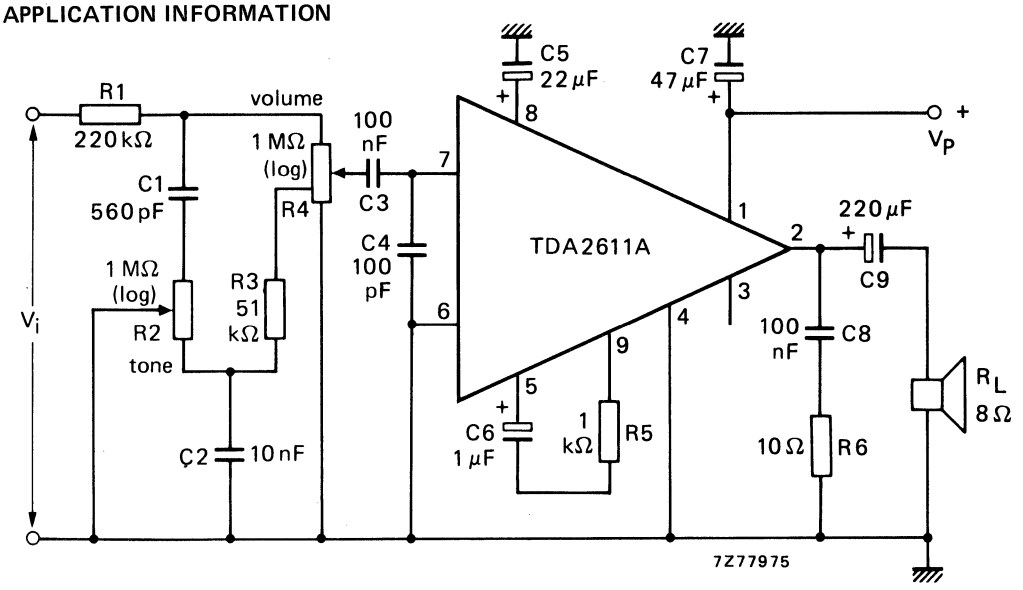


Fig. 10 Ceramic pickup amplifier circuit.

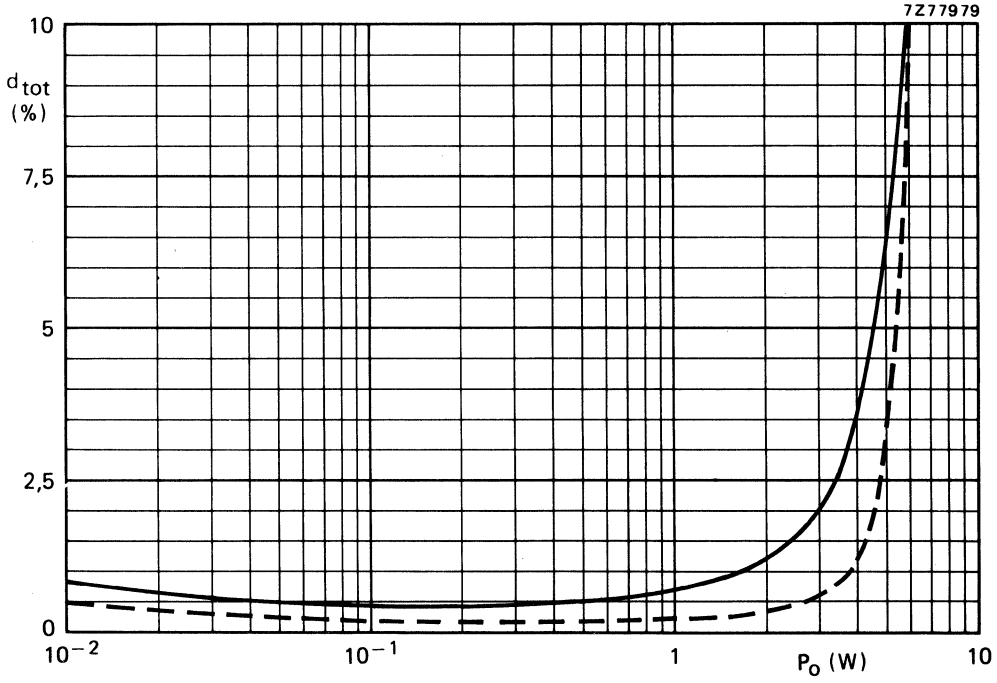


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

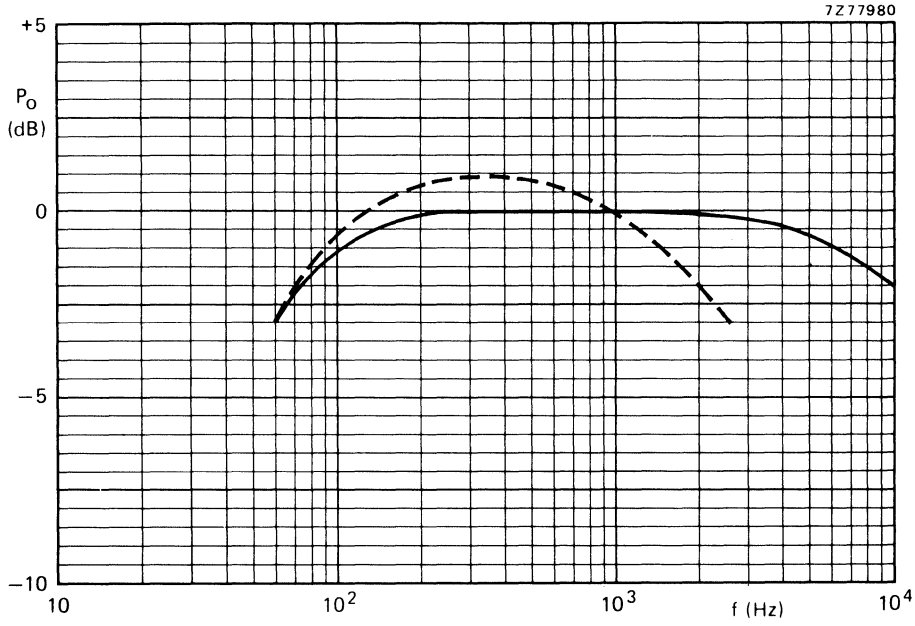


Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; – – – tone control min. high; P_O relative to 0 dB = 3 W; typical values.

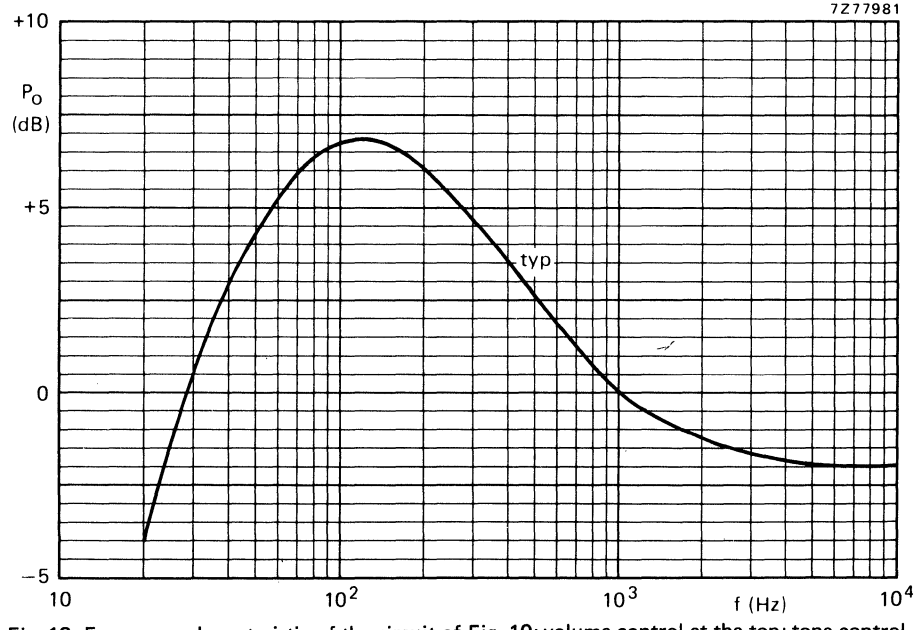


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

Low Voltage Mono/Stereo Power Amplifier — TDA7050T

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1.6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use—mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1.6 to 6.0	V
Total quiescent current (at V_P=3 V)	I_{tot}	typ. 3.2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\lvert\Delta V\rvert$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32Ω			
d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4.5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO-8; SOT-96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6	V
Peak output current	I_{OM}	max.	150	mA
Total power dissipation	see derating curve, Figure 1			
Storage temperature range	T_{stg}	−55 to +150		°C
Crystal temperature	T_c	max.	100	°C
A.C. and d.c. short-circuit duration at V_P = 3.0 V (during mishandling)	t_{sc}	max.	5	s

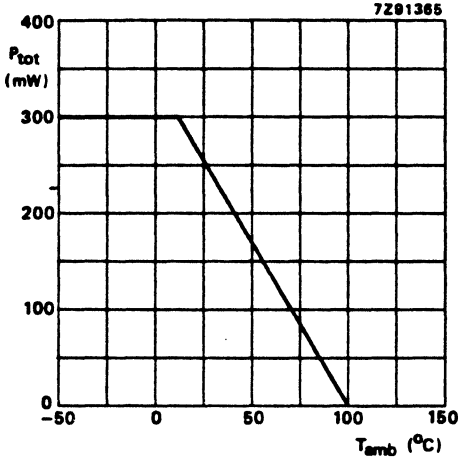


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100-60}{300} = 0.1\ W.$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1.6	–	6.0	V
Total quiescent current	I_{tot}	–	3.2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3.0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4.5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3.0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4.5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	–	26	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

*Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

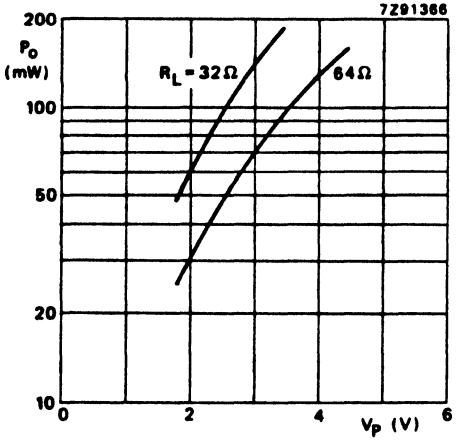


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

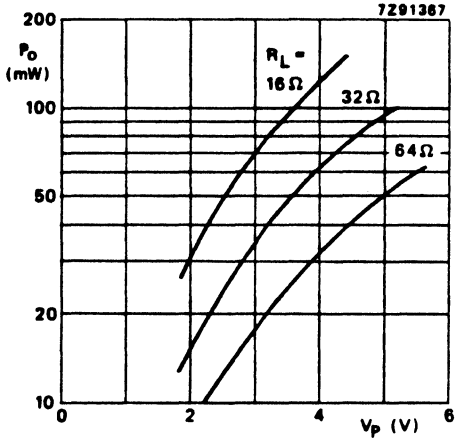


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

6

APPLICATION INFORMATION

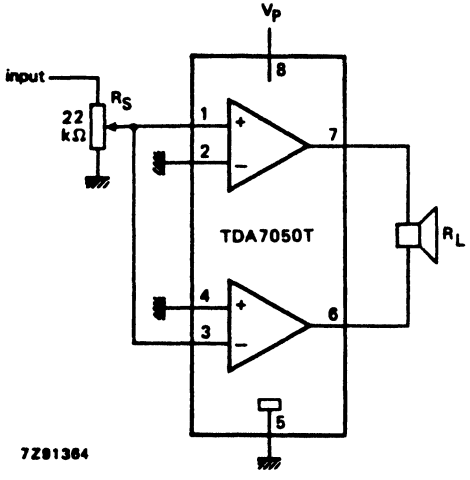


Fig. 4 Application diagram (BTL); also used as test circuit.

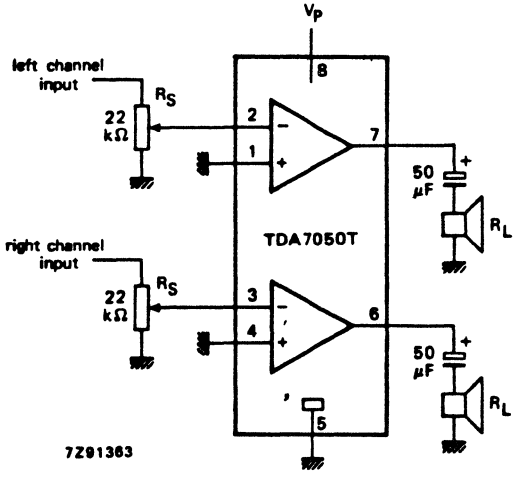


Fig. 5 Application diagram (stereo); also used as test circuit.

Wideband High Frequency Amplifier | NE5205

DESCRIPTION

The NE5205 is a High Frequency Amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz. This performance makes the amplifier ideal for cable TV applications. The NE5205 operates with a single supply of 6 volts, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75 ohm system and 6dB in a 50 ohm system.

Until now, most RF or high frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE5205 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75 ohm input and output impedances. The Standing Wave Ratios in 50 and 75 ohm systems do not exceed 1.5 on either the input or output over the entire DC to 600MHz operating range.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 650MHz. The metal can is hermetically sealed, and can operate over the full −55 to +125°C range.

No external components are needed other than AC coupling capacitors because the NE5205 is internally compensated and matched to 50 and 75 ohms. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75 ohm cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50 ohm test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50 ohms include mobile radio, CB radio and data/video transmission in fiber optics, as well as broadband LAN's and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE5205's in series as required, without any degradation in amplifier stability.

FEATURES:

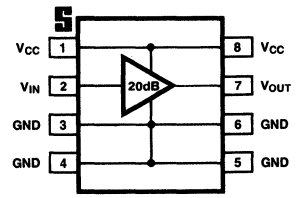
- **650MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O = 75\Omega$ ($Z_O = 50\Omega$)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface-Mount package available**
- **Excellent performance in cable TV 75Ω systems**

APPLICATIONS

- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broadband LAN's**
- **Fiber optics**
- **Modems**
- **Mobile radio**
- **CB radio**
- **Telecommunications**

PIN CONFIGURATION

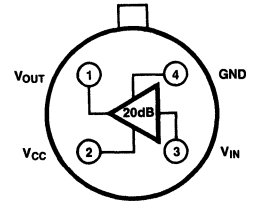
D PACKAGE



TOP VIEW
Order Number
NE5205D

NOTE: Signetics designates Pin 1.

EC PACKAGE



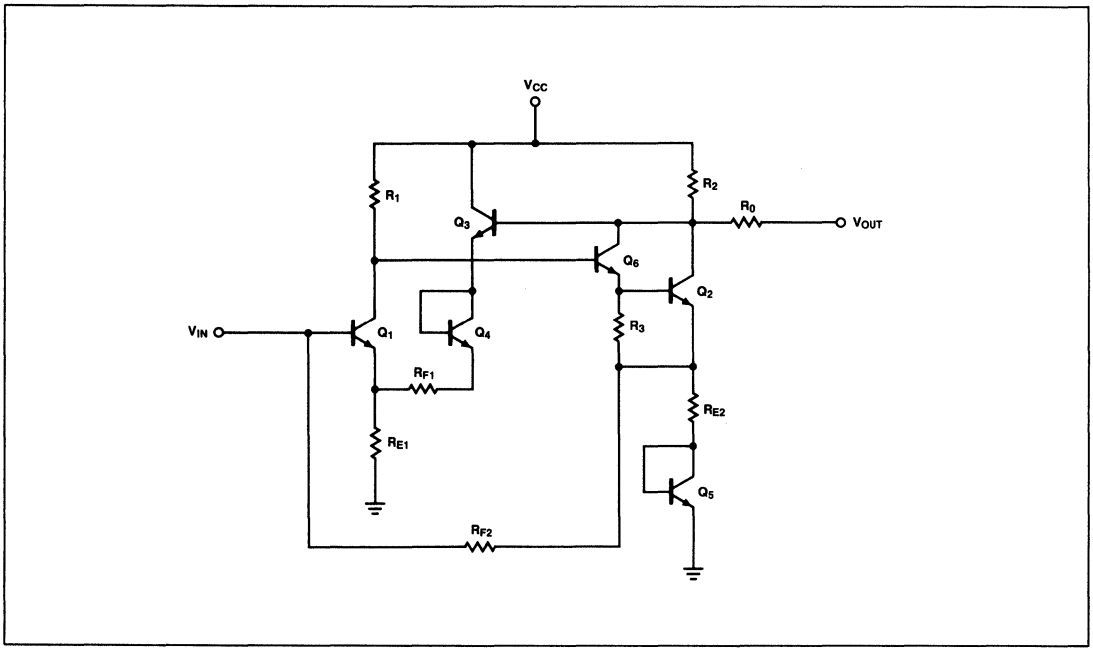
TOP VIEW
Order Number
NE5205EC

NOTE: Tab denotes Pin 1.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Supply Voltage	9	V
AC Input Voltage	5	V-PP
Operating Temperature		
SO package air-mount	– 55 to + 85	°C
TO package air-mount	– 55 to + 125	°C
(Derate SO package above 6V)		

EQUIVALENT SCHEMATIC



Wideband High Frequency Amplifier — NE5205

DC ELECTRICAL CHARACTERISTICS at $V_{CC} = 6V$, $Z_S = Z_L = Z_0 = 50\Omega$ and $T_A = 25\ °C$, in SO package unless otherwise specified.

PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
Operating supply voltage range		5		8	V
Supply current		20	24	30	mA
Insertion gain – S21	f = 100MHz	17	19	21	dB
Input return loss – S11	f = 100MHz SO pkg		25		dB
	DC – 550MHz	12			dB
Input return loss – S11	f = 100MHz TO pkg		23		dB
	DC – 600MHz	10			dB
Output return loss – S22	f = 100MHz SO pkg		27		dB
	DC – 550MHz	12			dB
Output return loss – S22	f = 100MHz TO pkg		26		dB
	DC – 600MHz	10			dB
Isolation – S12 (SO, TO)	f = 100MHz		– 25		dB
	DC – 550MHz	– 18			dB
Bandwidth-SO	± 0.5dB		450		MHz
Bandwidth-SO	– 3dB	550	600		MHz
Bandwidth-TO	– 3dB	600	650		MHz
Noise figure (75Ω)	f = 100MHz		4.8		dB
Noise figure (50Ω)	f = 100MHz		6.0		dB
Saturated output power	f = 100MHz		+ 7.0		dBm
1dB gain compression	f = 100MHz		+ 4.0		dBm
Third-order intermodulation intercept (output)	f-100MHz		+ 17		dBm
Second-order intermodulation intercept (output)	f = 100MHz		+ 24		dBm

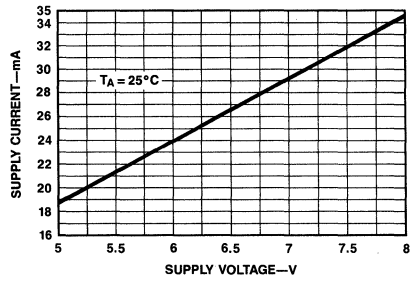


Figure 1. Supply Current vs Supply Voltage

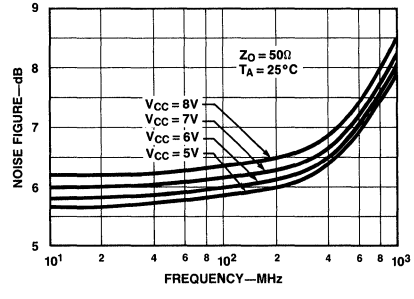


Figure 2. Noise Figure vs. Frequency

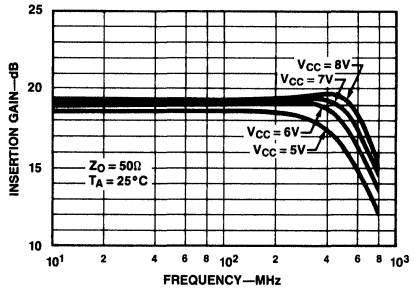


Figure 3. Insertion Gain vs Frequency (S_{21})

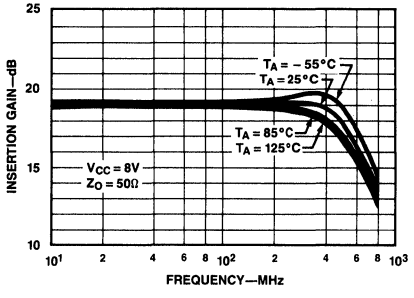


Figure 4. Insertion Gain vs Frequency (S_{21})

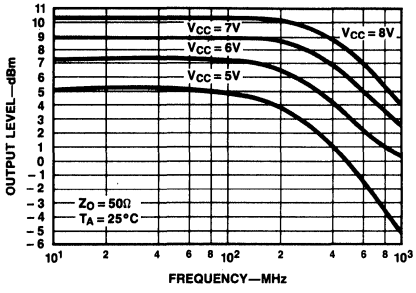


Figure 5. Saturated Output Power vs Frequency

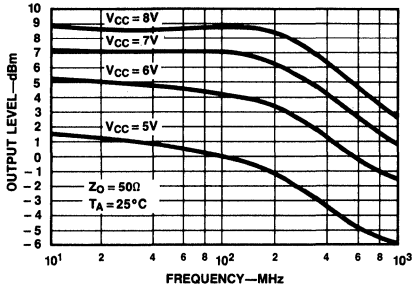


Figure 6. 1dB Gain Compression vs Frequency

6

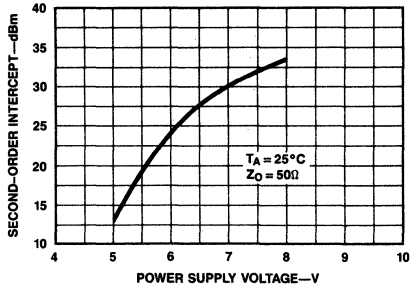


Figure 7. Second-Order Output Intercept vs Supply Voltage

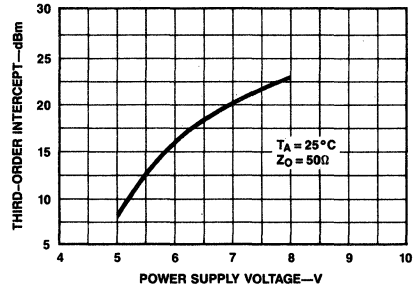


Figure 8. Third-Order Intercept vs Supply Voltage

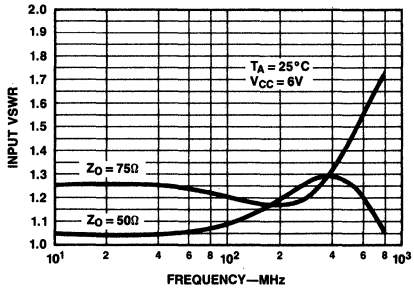


Figure 9. Input VSWR vs Frequency

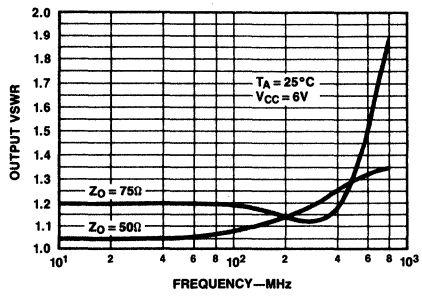


Figure 10. Output VSWR vs Frequency

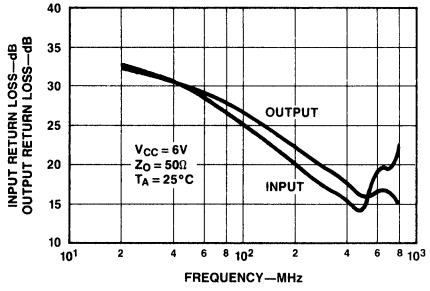


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

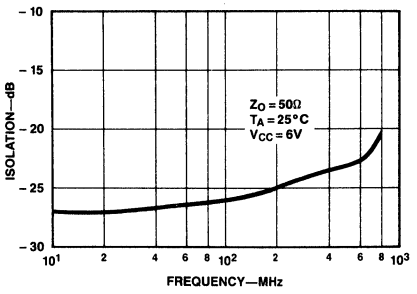


Figure 12. Isolation vs Frequency (S_{12})

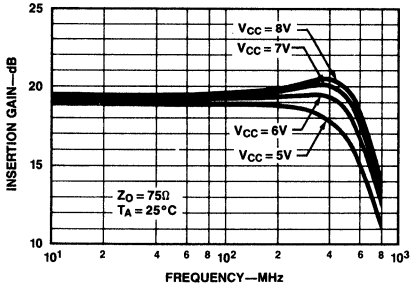


Figure 13. Insertion Gain vs Frequency (S_{21})

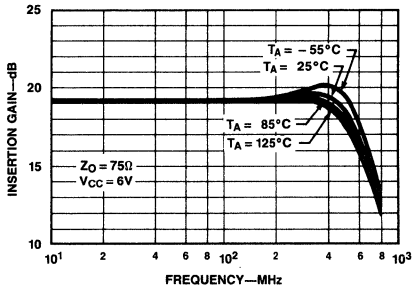


Figure 14. Insertion Gain vs Frequency (S_{21})

6

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wideband gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure for 50 and 75 ohm systems is given by the following equation:

$$NF = 10 \text{ Log} \left\{ 1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}} \right]}{R_0} \right\} dB \quad (2)$$

where $I_{C1} = 5.5mA$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26mV$ at 25°C and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3})R_{E1} \quad (3)$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8V$, $I_{C1} = 5mA$ and $I_{C3} = 7mA$ (currents rated at $V_{CC} = 6V$).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of $R_{F1} = 140$ ohms is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R_2 , \quad (4)$$

where $V_{CC} = 6V$, $R_2 = 225\Omega$, $I_{C2} = 7mA$ and $I_{C6} = 5mA$.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package. Signetics does not recommend operation at die temperatures above 110°C in the SO package. With this in mind, the following equation can be used to estimate the die temperature:

$$T_j = T_A + (P_d \times \theta_{jA})$$

where T_A = Ambient Temperature, T_j = Die Temperature, P_d = Power Dissipation = $I_{CC} \times V_{CC}$, θ_{jA} = Package Thermal Resistance, and $\theta_{jA} = 270°C/watt$ for SO-8, $\theta_{jA} = 100°C/watt$ for TO-46.

At the nominal supply voltage of 6 volts, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6 volts, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either tempera-

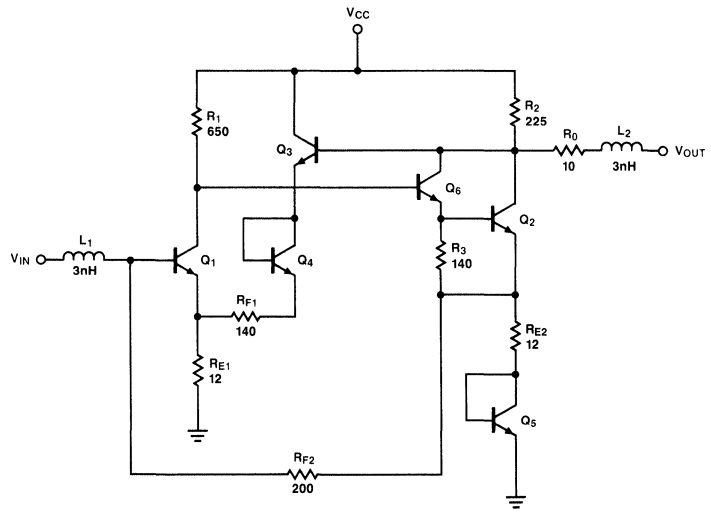


Figure 15. Schematic Diagram

ture extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the SO and TO-46 package body against the PC board plane. Operation at higher temperatures is possible but may result in lower MTBF (Mean Time Between Failures). This lower MTBF should be considered before operating beyond 110°C die temperature because of the overall reliability degradation.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). In addition, if the TO-46 package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at V_{CC} = 6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

Both of the evaluation boards that will be discussed next do not have input an output capacitors because it is assumed the user will use AC coupled test systems. Chip or foil capacitors can easily be inserted between the part and connector if the board trace is removed.

50 OHM EVALUATION BOARD

The evaluation board layout shown in Figure 17 produces excellent results. The board is to scale and is for the SO package but can be

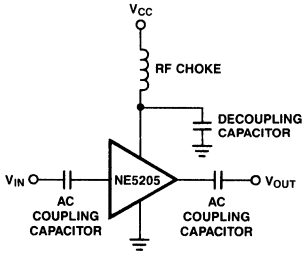
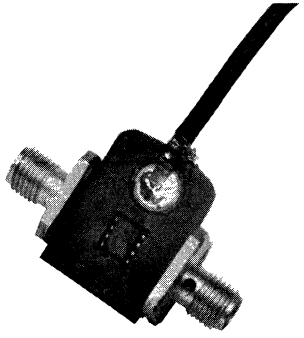


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling



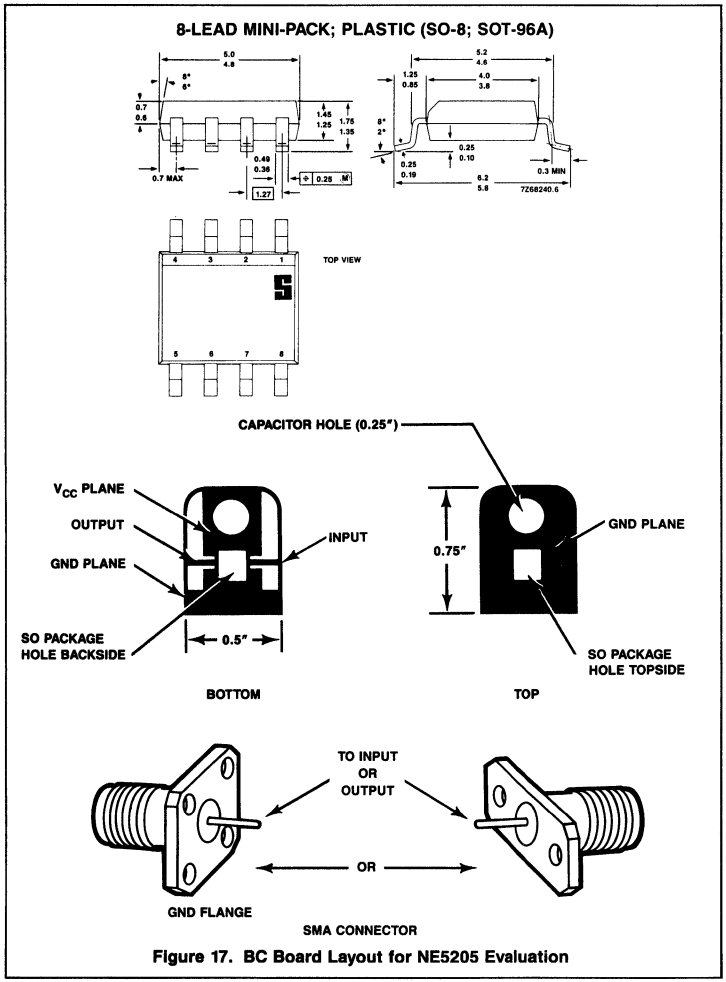


Figure 17. BC Board Layout for NE5205 Evaluation

used for the TO-46 package as well. Both top and bottom are copper clad and the ground planes are bonded together through 50 ohm SMA cable connectors. These are solder mounted on the sides of the board so that the signal traces line up straight to the connector signal pins.

Solid copper tubing is soldered through the flange holes between the two connectors for increased strength and grounding characteristics. Two or four hole flanges can be used. A flat round decoupling capacitor is placed in the board's round hole and soldered between the bottom V_{CC} plane and the top side ground. The capacitor is as thin or thinner than the PC board thickness and has insulation around its side to isolate V_{CC} and ground. The square hole is for the SO package which is put in upside down through the bottom of the board so that the leads are kept in position for soldering. Both holes are just slightly larger than the capacitor and IC to provide for a tight fit.

This board should be tested in a system with 50 ohm input and output impedance for correct operation.

75 OHM EVALUATION BOARD

Another evaluation board is shown in Figure 18. This system uses the same PC board as presented in Figure 17, but makes use of 75 ohm female N-type connectors. The board is mounted in a nickel plated box* that is used to support the N-type connectors. This is an excellent way to test the part for cable TV applications. Again, the board should be tested in a system with 75 ohm input and output impedance for correct operation.

*The box and connectors are available as a "MODPACK SYSTEM" from the ANZAC division of ADAMS-RUSSELL CO., INC., 80 Cambridge Street, Burlington, MA 01803.

SCATTERING PARAMETERS

The primary specifications for the NE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 19.

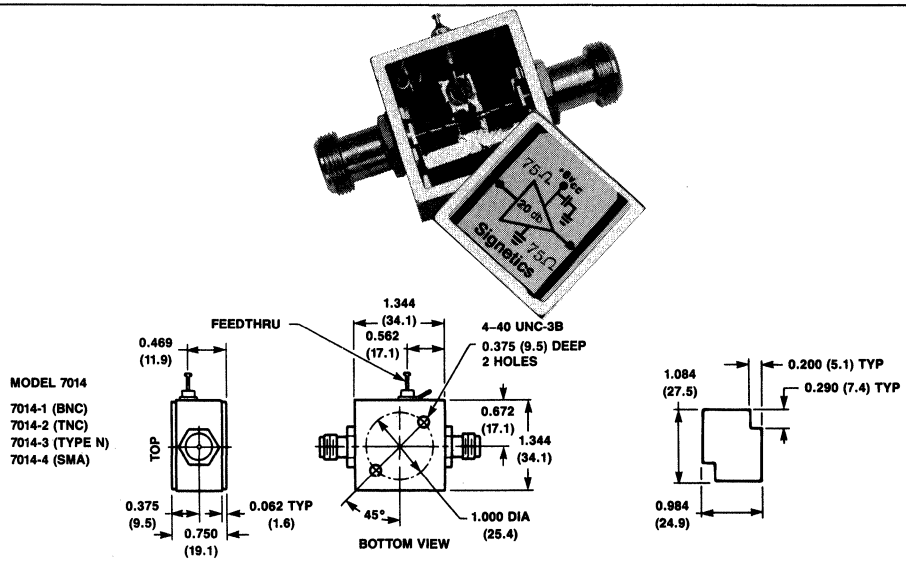


Figure 18. 75-Ohm N-Type Connector System

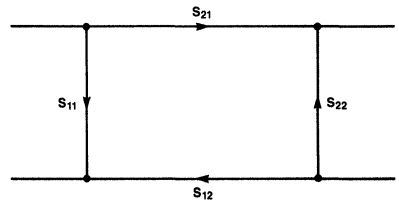


Figure 19a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

Figure 19b

Actual S-parameter measurements using an H.P. network analyzer (model 8505A) and an H.P. S-parameter tester (models 8503A/B) are shown in Figure 20. These were obtained with the device mounted in a PC board as described in Figures 17 and 18.

For 50 ohm system measurements, SMA connectors were used. The 75 ohm data was obtained using N-connectors.

Values for the figures below are measured and specified in the data sheet to ease adap-

50Ω System

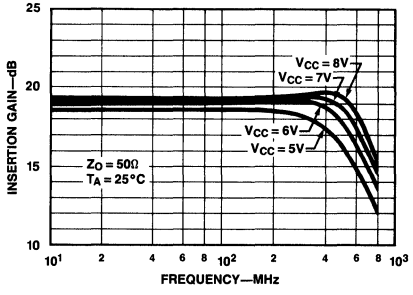


Figure A. Insertion Gain vs Frequency (S_{21})

75Ω System

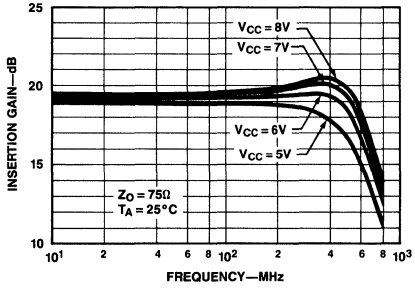


Figure B. Insertion Gain vs Frequency (S_{21})

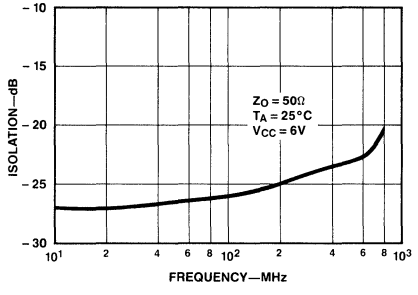


Figure C. Isolation vs Frequency (S_{12})

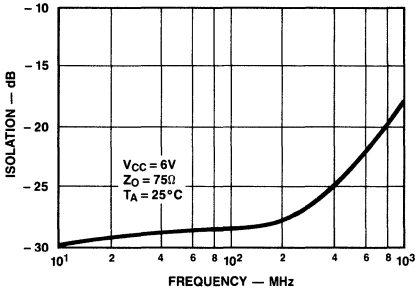


Figure D. S_{12} Isolation vs Frequency

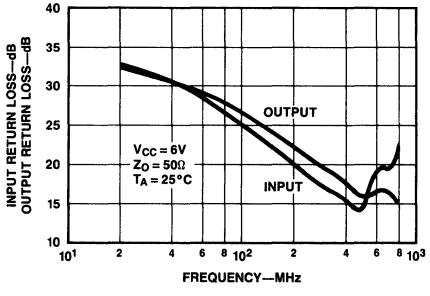


Figure E. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

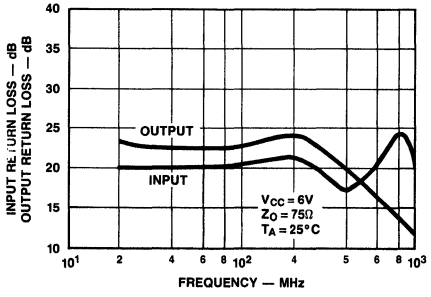


Figure F. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 20

6

tation and comparison of the NE5205 to other high frequency amplifiers. The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE5205

$$P_{IN} = \frac{V_{IN}^2}{Z_D} \quad \boxed{\text{NE5205}\ Z_D} \quad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain

V_I = Insertion Voltage Gain

Measured value for the NE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$$

$$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$$

$$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 21. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = $S_{11}dB$

$S_{11}dB = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = $S_{22}dB$

$S_{22}dB = 20 \text{ Log } |S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leq 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{22}|}{|1 - S_{22}|} \leq 1.5$$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 22, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$$IP_2 = P_{OUT} + IMR_2$$

$$IP_3 = P_{OUT} + IMR_3/2$$

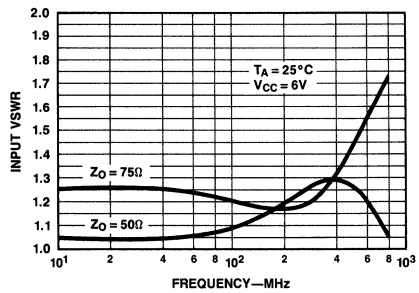


Figure A. Input VSWR vs Frequency

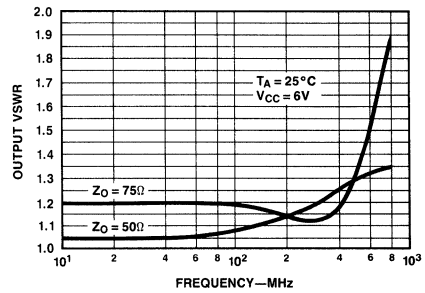


Figure B. Output VSWR vs Frequency

Figure 21. Input/Output VSWR Versus Frequency

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE5205 we have chosen an output level of −10.5dBm with fundamental frequencies of 100.000 and 100.01 MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

S-Parameter Techniques for Faster, More Accurate Network Design, H.P. App Note 95-1, Richard W. Anderson, 1967, HP Journal.

S-Parameter Design, H.P. App Note 154, 1972.

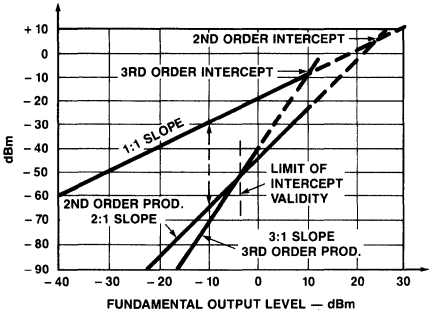


Figure 22

6

Signetics

Power Conversion and Control
Section 7

Linear Products

AC Motor Control Circuit — HEF4752V

The HEF4752V is a circuit for a.c. motor speed control utilizing LOCMOS technology. The circuit synthesizes three 120° out of phase signals, of which the average voltage varies sinusoidally with time in the frequency range 0 to 200 Hz. The method employed is based upon the pulse width modulation principle, in order to achieve a sufficient accuracy of the output voltages over the whole frequency range. A pure digital waveform generation is used.

All outputs are of the push-pull type. Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

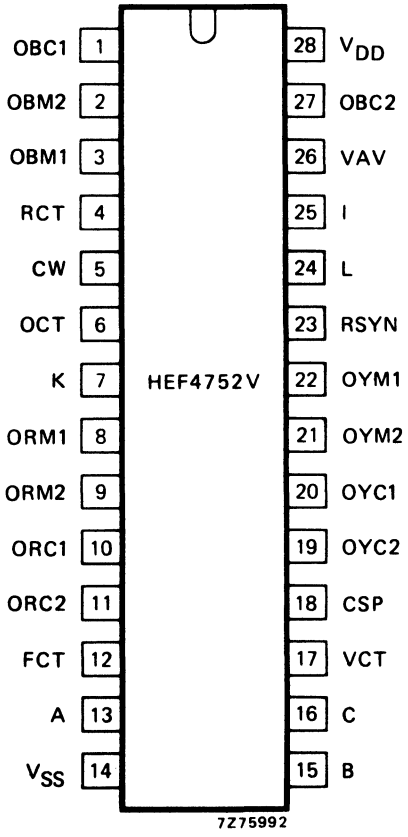


Fig. 1 Pinning diagram.

PINNING

Inputs; group I		Inputs; group II	
24 = L	data	12 = FCT	frequency clock
25 = I	data	17 = VCT	voltage clock
7 = K	data	4 = RCT	reference clock
5 = CW	data	6 = OCT	output delay clock
13 = A	data		
15 = B	data		
16 = C	data		

Outputs; group I

23 = RSYN	R-phase synchronization
26 = VAV	average voltage
18 = CSP	current sampling pulses

Outputs; group II

8 = ORM1	R-phase main
9 = ORM2	R-phase main
10 = ORC1	R-phase commutation
11 = ORC2	R-phase commutation
22 = OYM1	Y-phase main
21 = OYM2	Y-phase main
20 = OYC1	Y-phase commutation
19 = OYC2	Y-phase commutation
3 = OBM1	B-phase main
2 = OBM2	B-phase main
1 = OBC1	B-phase commutation
27 = OBC2	B-phase commutation

SUPPLY VOLTAGE

	rating	recommended operating
HEF4752V	−0,5 to 18	4,5 to 12,5 V

HEF4752VP : 28-lead DIL; plastic (SOT-117).
HEF4752VD : 28-lead DIL; ceramic (cerdip) (SOT-135A).
HEF4752VT : 28-lead mini-pack; plastic (SO-28; SOT-136A).

FAMILY DATA see Family Specifications

7

D.C. CHARACTERISTICS V_{SS} = 0 V

parameter	V_{DD} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	unit	conditions
Quiescent device current	5	I_{DD}	–	50	–	50	–	375	μA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}
	10		–	100	–	100	–	750	μA	
Input leakage current	10	$\pm I_{IN}$	–	–	–	0,3	–	1	μA	V_I = 0 or 10 V
Input voltage HIGH	5	V_{IH}	3,5	–	3,5	–	3,5	–	V	inputs: group I
	10		7,0	–	7,0	–	7,0	–	V	
Input voltage LOW	5	V_{IL}	–	1,5	–	1,5	–	1,5	V	inputs: group I
	10		–	3,0	–	3,0	–	3,0	V	
Output voltage HIGH	5	V_{OH}	4,95	–	4,95	–	4,95	–	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1\ \mu A$
	10		9,95	–	9,95	–	9,95	–	V	
Output voltage LOW	5	V_{OL}	–	0,05	–	0,05	–	0,05	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1\ \mu A$
	10		–	0,05	–	0,05	–	0,05	V	
Input tripping level; input voltage increasing	5	V_{ti}	1,5	4,0	1,5	4,0	1,5	4,0	V	inputs: group II
	10		3,0	8,0	3,0	8,0	3,0	8,0	V	
Input tripping level; input voltage decreasing	5	V_{td}	1,0	3,5	1,0	3,5	1,0	3,5	V	inputs: group II
	10		2,0	7,0	2,0	7,0	2,0	7,0	V	
Output current LOW	5	I_{OL}	0,45	–	0,38	–	0,3	–	mA	V_{OL} = 0,4 V; outputs: groups I and II
	10		1,4	–	1,17	–	0,9	–	mA	V_{OL} = 0,5 V; outputs: groups I and II
Output current HIGH	5	$-I_{OH}$	0,3	–	0,25	–	0,2	–	mA	V_{OH} = 4,6 V; outputs: group I
	10		0,9	–	0,75	–	0,6	–	mA	V_{OH} = 9,5 V; outputs: group I
Output current HIGH	5	$-I_{OH}$	0,9	–	0,75	–	0,6	–	mA	V_{OH} = 2,5 V; outputs: group I
Output current HIGH	5	$-I_{OH}$	0,6	–	0,5	–	0,4	–	mA	V_{OH} = 4,6 V; outputs: group II
	10		1,8	–	1,5	–	1,2	–	mA	V_{OH} = 9,5 V; outputs: group II
Output current HIGH	5	$-I_{OH}$	1,8	–	1,5	–	1,2	–	mA	V_{OH} = 2,5 V; outputs: group II
Total supply current	10	I_{tot}	–	–	typ. 2		–	–	mA	$I_{OL} = I_{OH} = 0$; frequency applied to inputs; FCT = 700 kHz; VCT = 400 kHz; RCT = 400 kHz

APPLICATION INFORMATION

Figure 2 shows the functional block diagram of a 3-phase a.c. motor speed control system using a thyristorized inverter with variable frequency output. The inverter control signals are generated by the HEF4752V (PWM-IC). A special feature of the PWM (Pulse-Width Modulation) - IC is here, that the motor is supplied by sinnoidally modulated pulses, hence the resulting motor current will approach a sine-wave with a minimum on higher harmonics. In this way, an optimum speed drive with high performance is obtained.

Furthermore, the HEF4752V contains all logic circuitry required for this special waveform generation, so that the amount of control circuit components is reduced considerable. The speed drive system in Fig. 2 is controlled by the analogue control section.

The FCT and VCT clock pulse oscillators are driven in such a way, that a fast response speed control of the a.c. motor is obtained, depending on: the reference values for speed; motor voltage; motor current (Limited by the measured motor current via DCCT - d.c. current transformer -); the increasing value of V_{Cb} during braking action.

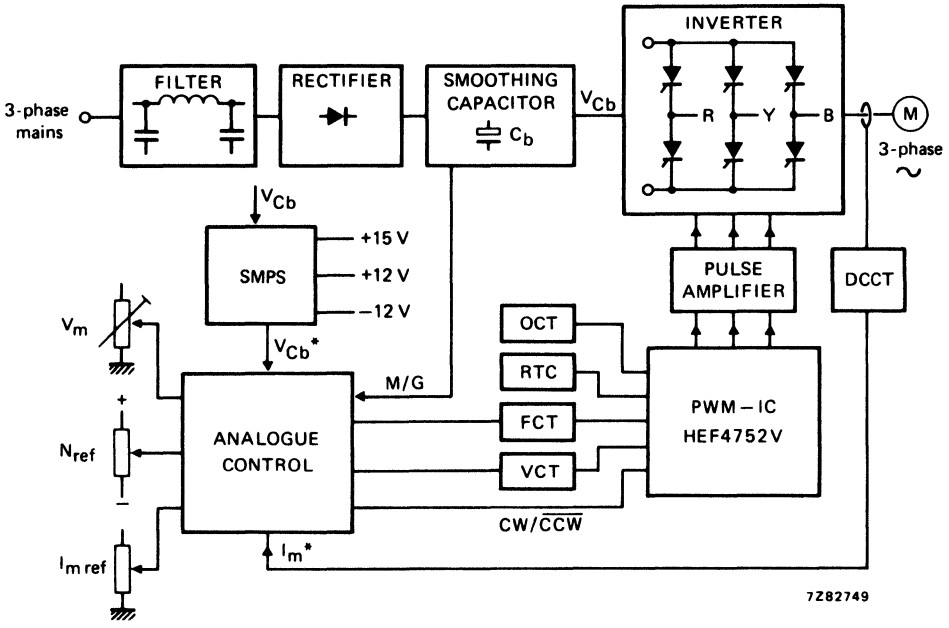


Fig. 2 PWM motor speed control system using HEF4752V.

MORE APPLICATION INFORMATION SUPPLIED ON REQUEST

7

Motor Regulator and Function Controller — TDA1506

The TDA1506 is for car radio/casette players. It incorporates the following functions:

- a motor speed regulator with a multiplication coefficient of k = 20,5.
- an electronic motor stop, controlled by commutator pulses;
- protection circuitry to avoid restarting of the motor after the set is switched to radio reception;
- playback indication;
- tape-end indication with intermittent light;
- fast-wind/rewind circuitry;
- two separately stabilized voltage regulators for the playback amplifier stages;
- a stabilized output voltage for the radio part;
- an automatic switch for switching the preamplifier supply outputs to zero and the radio supply output to a high level at tape-end;
- an output signal for auto-reverse;
- short-circuit protection for all pins to ground at T_{amb} = 30 °C maximum and between output and power supply pin;
- load dump protection.

During fast wind (or rewind) the voltage regulator for the second playback preamplifier is switched off. This feature allows application in an A.P.S.S. (Automatic Program Search System) set. At tape-end and at an externally chosen fixed time before motor stop, the automatic replay output gives a d.c. information signal. This signal may, e.g., be used to control the plunger in an automatic-reverse set. Automatic switching, with all switches to ground.

QUICK REFERENCE DATA

Supply voltage range		V_P	10 to 16	V
Operating ambient temperature range				
at V_P = 14,4 V		T_{amb}	−20 to +80	°C
at V_P = 16 V		T_{amb}	−20 to +60	°C
Motor regulator				
Regulator supply voltage range		V_{6-3}	3,2 to 12	V
Internal reference voltage	V_{ref} =	V_{6-5} typ.	1,38	V
Drop-out voltage		V_{4-3} <	1,8	V
Multiplication coefficient ($\Delta I_4/\Delta I_6$)		k typ.	20,5	
Stabilization radio				
Output voltage		V_{11-8} >	8,5	V
Limited output current		$I_{11\ lim}$ >	45	mA
Stabilization preamplifier I				
Output voltage		V_{10-8} >	7,7	V
Limited output current		$I_{10\ lim}$ >	2	mA
Stabilization preamplifier II				
Output voltage		V_{9-8} >	8,7	V
Limited output current		$I_{9\ lim}$ >	20	mA
Lamp driver				
Output voltage		V_{2-8} >	13	V
Limited output current		$I_{2\ lim}$ >	20	mA

PACKAGE OUTLINE 16-lead DIL; plastic power (SOT-38).

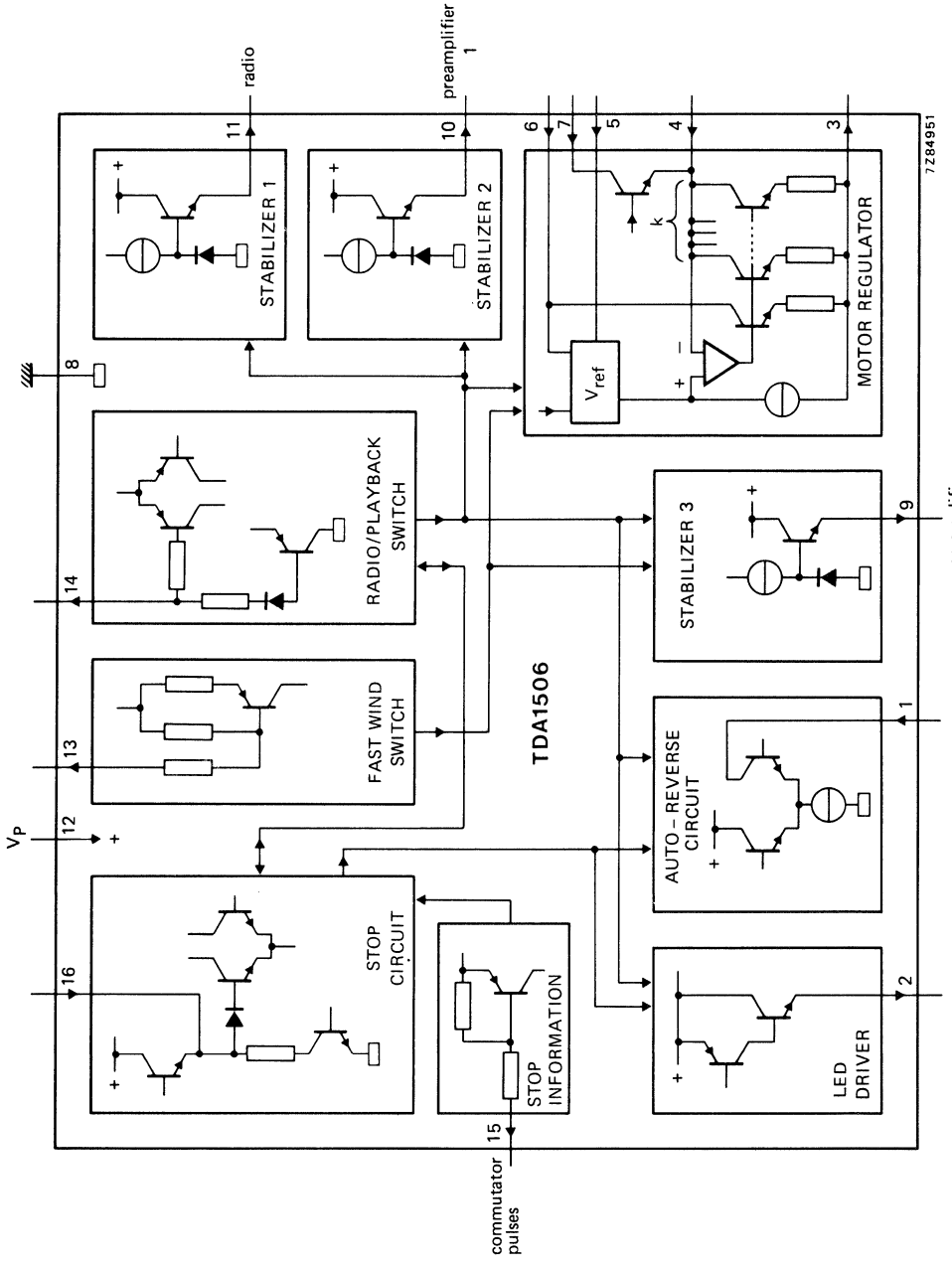


Fig. 1 Block diagram.

7

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Limited output current	$I_{4\ lim}$	max.	1 A
Power dissipation	see Fig. 2		
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	55 K/W

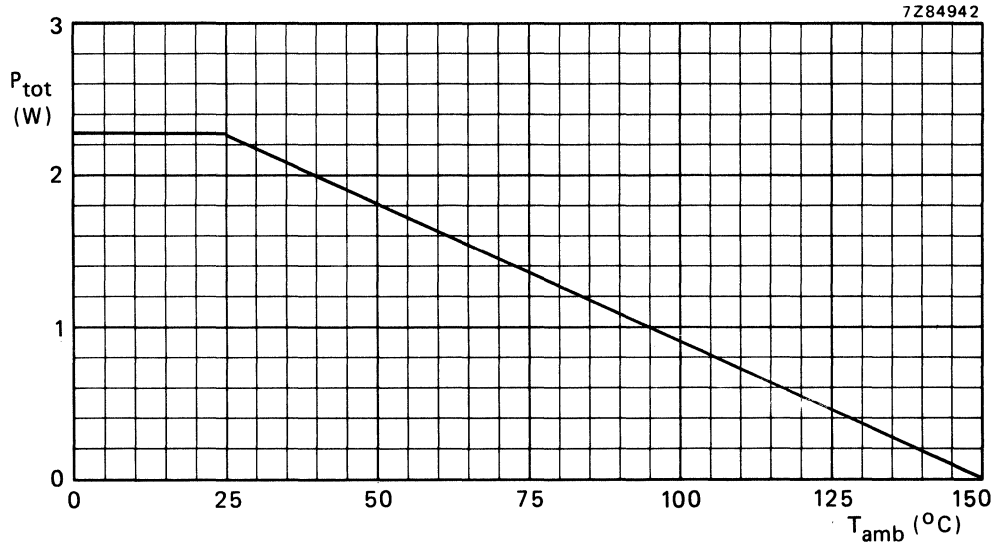


Fig. 2 Power derating curve.

Note to Fig. 2

$$P_{tot} = \frac{T_{j\ max} - T_{amb}}{R_{th\ j\text{-}a}}$$

P_{tot} in playback position (see Figure 3):

$$P_{tot} \approx I_{12} \times V_P + V_{4\text{-}3}\left(I_m + \frac{V_{ref}}{R_2}\right) + \left(V_{4\text{-}3} + V_{ref}\right)\left(\frac{I_4}{k} + I_q\right) - I_2 \times V_{2\text{-}8} - I_9 \times V_{9\text{-}8} - I_{10} \times V_{10\text{-}8}$$

P_{tot} in radio reception is much lower than P_{tot} in playback.

CHARACTERISTICS

V_P = 14,4 V; T_{amb} = 25 °C; I_4 = 70 mA; I_{11} = 45 mA; I_{10} = 0,3 mA; I_2 = 18 mA; I_9 = 2 mA; unless otherwise specified; see test circuit Fig. 3.

	symbol	min.	typ.	max.	unit	conditions
General						
Supply voltage	V_P	10 *	–	16	V	
Current consumption						
at playback	I_{12}	–	–	38	mA	I_4 = 0
at radio	I_{12}	–	–	64	mA	
Motor regulator						
Supply voltage	V_{6-3}	3,2	–	12	V	
Drop-out voltage	V_{4-3}	–	–	1,8	V	ΔV_{ref} = ± 2%
Internal reference voltage	$V_{ref} = V_{6-5}$	1,32	1,38	1,44	V	V_{6-3} = 8,7 V
Quiescent current	I_q	–	1,5	2,5	mA	I_4 = 0; V_{6-3} = 8,7 V
Limited output current	$I_{4\ lim}$	0,5	–	–	A	V_{6-3} = 8,7 V
Multiplication coefficient	$k = \Delta I_4/\Delta I_6$	18,5	20,5	22,5		V_{6-3} = 8,7 V; $\lvert\Delta I_4\rvert$ = ± 10 mA
Line regulation variation						
V_{ref} versus V_P	$\frac{\Delta V_{ref}}{\Delta V_P} \times \frac{100\%}{V_{ref}}$	0	0,05	0,09	%/V	V_P = 3,2 to 12 V
k versus V_P	$\frac{\Delta k}{\Delta V_P} \times \frac{100\%}{k}$	0	0,3	0,6	%/V	V_P = 3,2 to 12 V; $\lvert\Delta I_4\rvert$ = ± 10 mA
I_q versus V_P	$\frac{\Delta I_q}{\Delta V_P} \times \frac{100\%}{I_q}$	–	1,25	–	%/V	V_P = 3,2 to 12 V; I_4 = 0
Load regulation variation						
V_{ref} versus I_4	$\frac{\Delta V_{ref}}{\Delta I_4} \times \frac{100\%}{V_{ref}}$	–0,037	–0,018	–	%/mA	I_4 = 20 to 150 mA
k versus I_4	$\frac{\Delta k}{\Delta I_4} \times \frac{100\%}{k}$	–0,02	0	+0,02	%/mA	I_4 = 20 to 150 mA; $\lvert\Delta I_4\rvert$ = ± 10 mA
Temperature coefficient variation						
V_{ref} versus T_{amb}	$\frac{\Delta V_{ref}}{\Delta T_{amb}} \times \frac{100\%}{V_{ref}}$	0	0,025	0,045	%/K	T_{amb} = –20 to +80 °C; V_{6-3} = 8,7 V
k versus T_{amb}	$\frac{\Delta k}{\Delta T_{amb}} \times \frac{100\%}{k}$	–0,016	0,008	0,032	%/K	T_{amb} = –20 to +80 °C; V_{6-3} = 8,7; ΔI_4 = ±10 mA
I_q versus T_{amb}	$\frac{\Delta I_q}{\Delta T_{amb}} \times \frac{100\%}{I_q}$	–	0,13	–	%/K	T_{amb} = –20 to +80 °C; V_{6-3} = 8,7 V; I_4 = 0
Saturation voltage fast winding	$V_{7-4\ sat}$	–	0,18	–	V	I_7 = 10 mA (max. 50 mA)
Input current (pin 5)	I_5	–	19	–	μA	V_{6-3} = 8,7 V

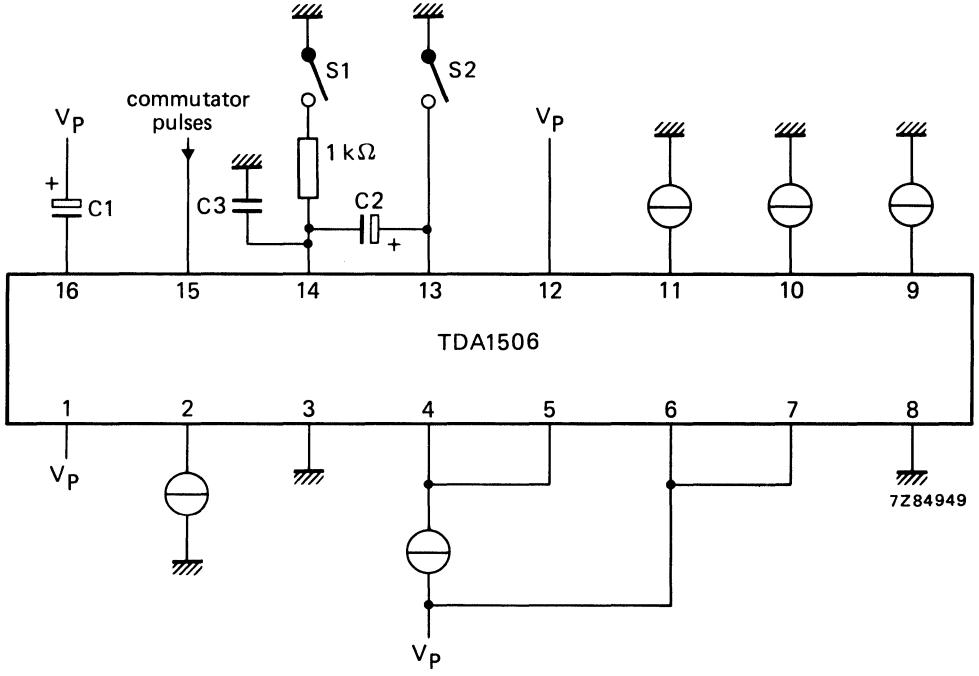
* For starting conditions: min. 6 V.

7

	symbol	min.	typ.	max.	unit	conditions
Automatic motor stop						
Output current (pin 15)	I_{15}	0,4	–	0,9	mA	
Time constant	t_{st}	–	700	–	ms	C1 = 47 μF ± 1%; Fig. 4
Switching level	V_{16-8}	–	9	–	V	
Stabilization radio						
Output voltage	V_{11-8}	8,5	8,9	9,3	V	
Limited output current	$I_{11\ lim}$	45	–	–	mA	
Variation of V_{11-8}	ΔV_{11-8}	–	–	200	mV	V_P = 10,5 to 16 V
		–	100	–	mV/V	V_P = 10 to 10,5 V
Leakage current	I_{11}	–	–	0,5	μA	R_{11-8} = 100 kΩ
	I_{11}	–	–	4	μA	R_{11-8} = 100 kΩ; T_{amb} = 80 °C
Temperature coefficient	$\Delta V_{11-8}/\Delta T_{amb}$	–2	0	+2	mV/K	T_{amb} = –20 to +80 °C
Stabilization preamp. I						
Output voltage	V_{10-8}	7,7	8,1	–	V	
Limited output current	$I_{10\ lim}$	2	–	–	mA	
Variation V_{10-8} versus V_P	$\Delta V_{10-8}/\Delta V_P$	–	–	12	mV/V	V_P = 10,5 to 16 V
	$\Delta V_{10-8}/\Delta V_P$	–	5	–	mV/V	V_P = 10 to 10,5 V
Stabilization preamp. II						
Output voltage	V_{9-8}	8,5	9,1	–	V	
Output voltage	V_{9-8}	–	0	0,5	V	fast rewind
Limited output current	$I_{9\ lim}$	20	–	–	mA	
Variation V_{9-8} versus V_P	$\Delta V_{9-8}/\Delta V_P$	–	–	12	mV/V	V_P = 10,5 to 16 V
	$\Delta V_{9-8}/\Delta V_P$	–	10	–	mV/V	V_P = 10 to 10,5 V
Lamp driver						
Output voltage	V_{2-8}	13	13,4	–	V	
Limited output current	$I_{2\ lim}$	20	–	–	mA	
Blinking time	t_b	–	0,5	–	s	C1 = 47 μF; Fig. 4
Rejection voltage supply	ΔV_P	–	0,3	–	V	
Automatic replay output						
Output current; playback	I_1	–	–	10	μA	$V_{1-8} = V_P$
Output current; radio	I_1	300	500	–	μA	$V_{1-8} \geqslant 5$ V
Delay time	t_d	–	380	–	ms	C1 = 47 μF; Fig. 4

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	unit	conditions
Radio playback switch						
Switching levels						
to playback	V_{14-8}	–	–	2	V	V_P = 10 to 16 V
to radio	V_{14-8}	3,5	–	–	V	T_{amb} = –20 to +80 °C
Input impedance	$\lvert Z_{14-8}\rvert$	–	20	–	kΩ	
Output current	I_{14}	–	200	–	μA	V_{14-8} = 0
Fast wind switch						
Switching levels						
normal to fast	V_{13-8}	–	–	2	V	V_P = 10 to 16 V
fast to normal	V_{13-8}	6	–	–	V	T_{amb} = –20 to +80 °C
Output voltage; playback	V_{13-8}	–	6,8	–	V	
Output current; fast wind	I_{13}	–	500	–	μA	V_{13-8} = 0
Output impedance	$\lvert Z_{13-8}\rvert$	–	13	–	kΩ	



S1 closed: playback
S1 open: radio reception
S2 closed: fast speed
S2 open: normal speed

C2 is only used with sets on which a fast rewind key is available (C2 = 2,2 μF).
C1 is 200 μF maximum (typ. 47 μF).
C3 = 100 nF.

Fig. 3 Test circuit.

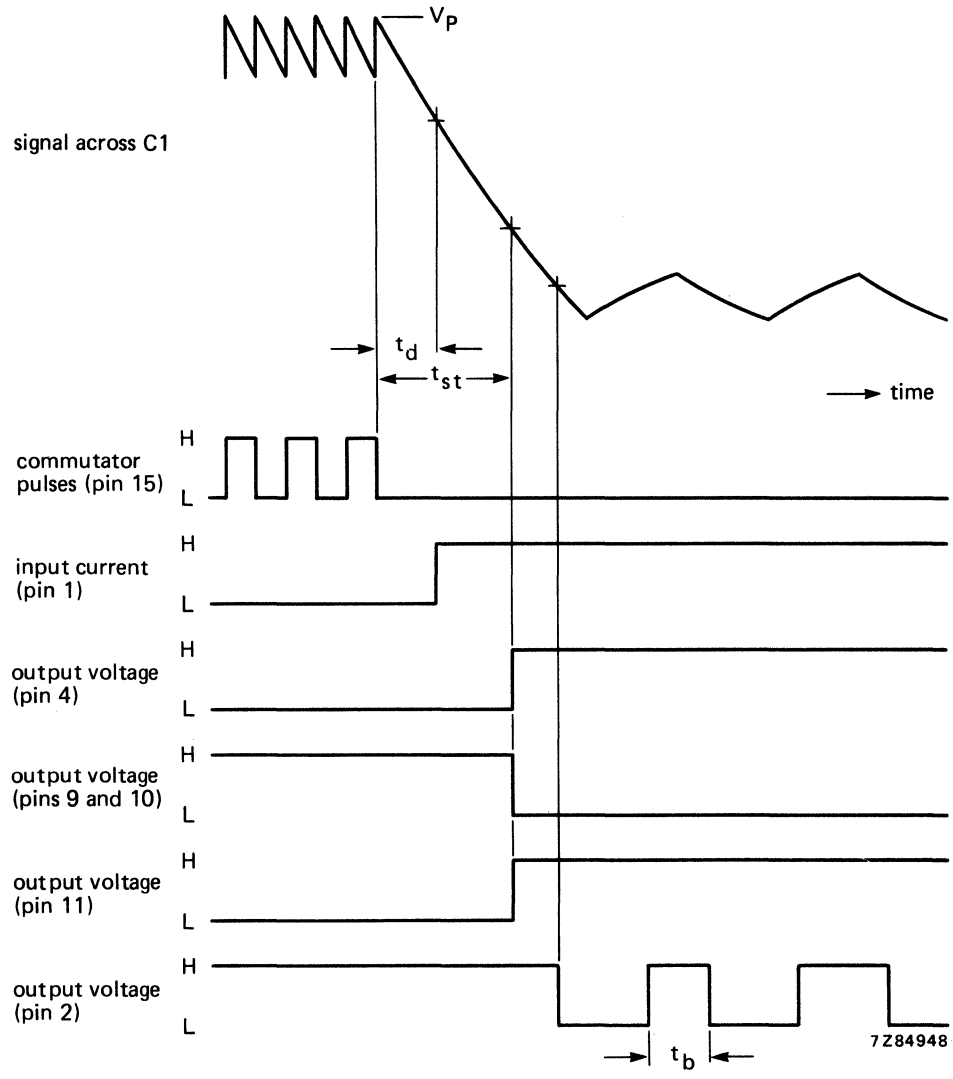


Fig. 4 Waveforms showing signal levels and time constants.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

APPLICATION INFORMATION

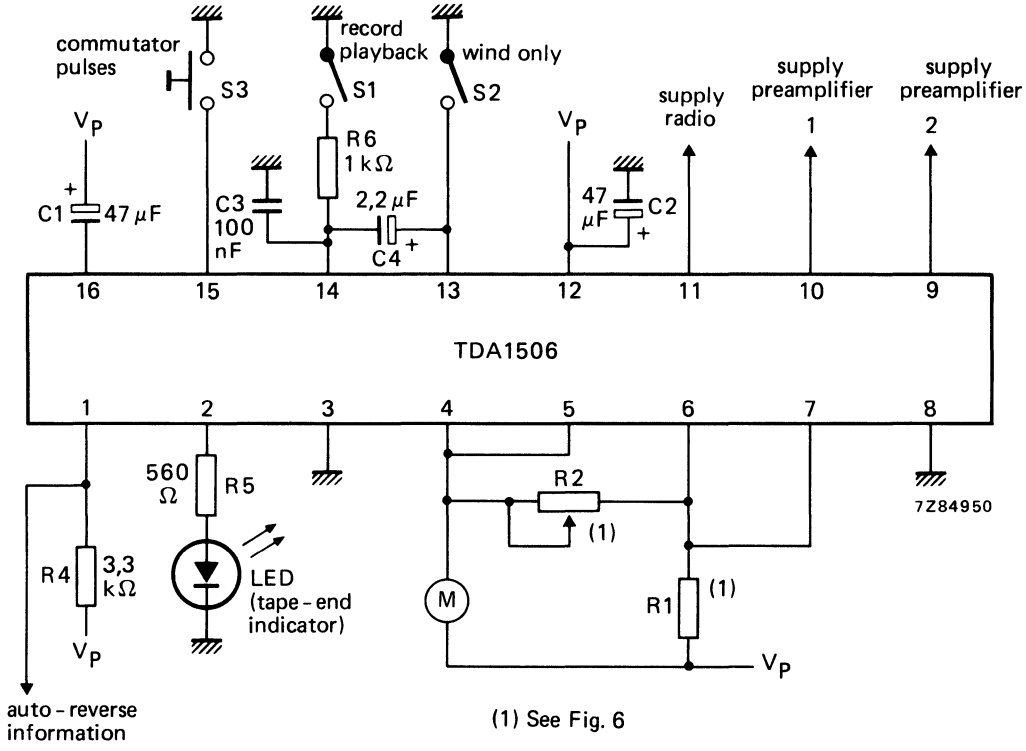
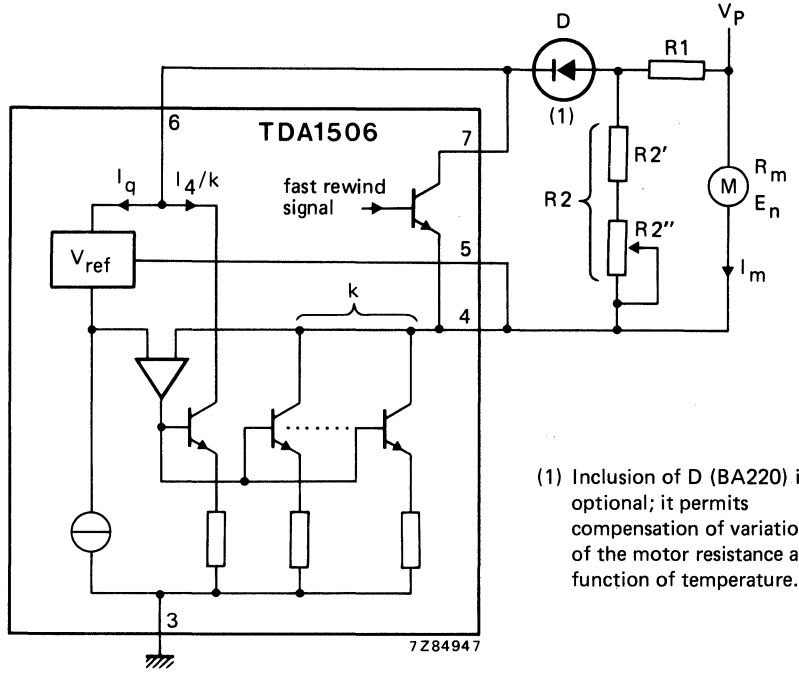


Fig. 5 Typical simplified application circuit diagram.



(1) Inclusion of D (BA220) is optional; it permits compensation of variation of the motor resistance as function of temperature.

Fig. 6 Example of using the TDA1506 (only the motor regulation part is shown) in a d.c. motor speed regulation circuit.

Notes to Fig. 6

$R2 = R2' + R2''$

$E_n = n \times C \times \phi$

$I_m = T \times \frac{2\pi}{60} \times \frac{1}{C.\phi}$

where: n = speed in revolutions per minute
C = motor constant
ϕ = magnetic flux
E_n = electromotive force
T = motor torque
R_m = motor resistance

E_n can be expressed (excluding diode D) as:

$$E_n = I_m \left(\frac{R1}{k} - R_m\right) + V_{ref} \left\{1 + \frac{R1}{R2}\left(1 + \frac{1}{k}\right)\right\} + R1 \times I_q$$

For optimal regulation (dn/dT = 0), $\left(\frac{R1}{k} - R_m\right)$ should be zero.

However, if $R1 = k \times R_m$, the regulator will be oscillating, so for stability always $R1 < k \times R_m$.

R2 is determined by:

$$R2 = \frac{V_{ref} \times R1 \times \left(1 + \frac{1}{k}\right)}{E_n - (R1 \times I_q) - V_{ref} - I_m \left(\frac{R1}{k} - R_m\right)}$$

Example:

$E_n = E_{2400} = 5{,}24$ V(±12,2%)

$R_m = 25{,}6\ \Omega$(±10%)

n = 2400 rev/min

T = 1,3 mNm
R1 = 430 Ω
R2' = 110 Ω
R2'' = 220 Ω

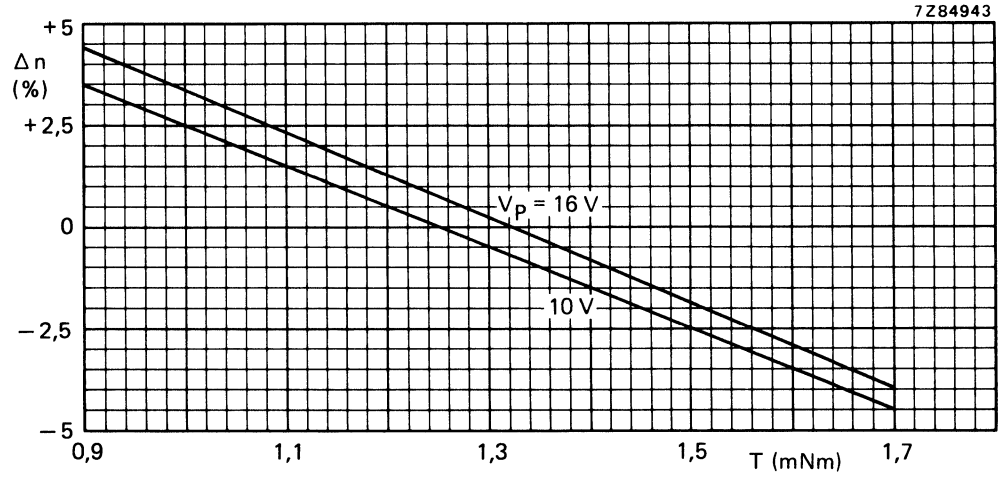


Fig. 7 Variation in motor speed (n is revolutions per minute) as a function of the applied motor torque at T_{amb} = 25 °C.

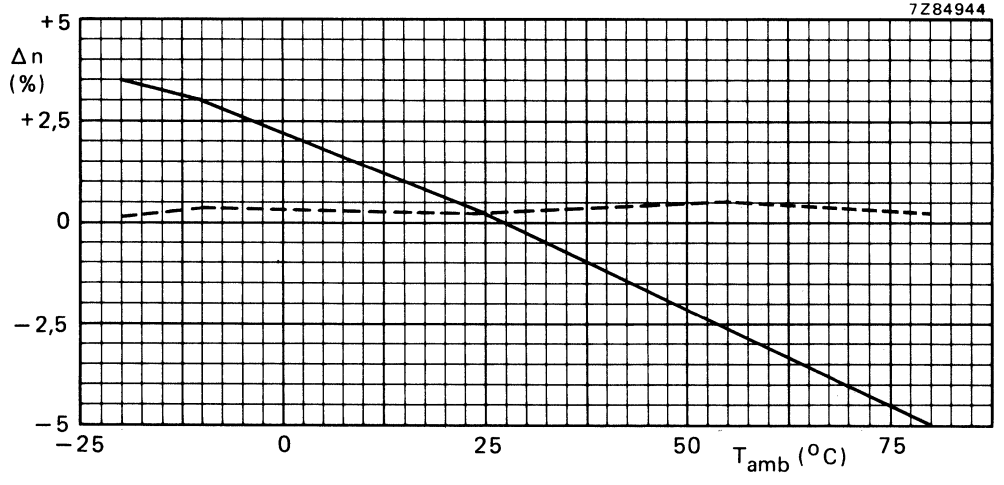


Fig. 8 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature at T = 1,3 mNm nominal and V_P = 16 V.
————————: with diode D (see Fig. 6).
— — — — — — —: without diode.

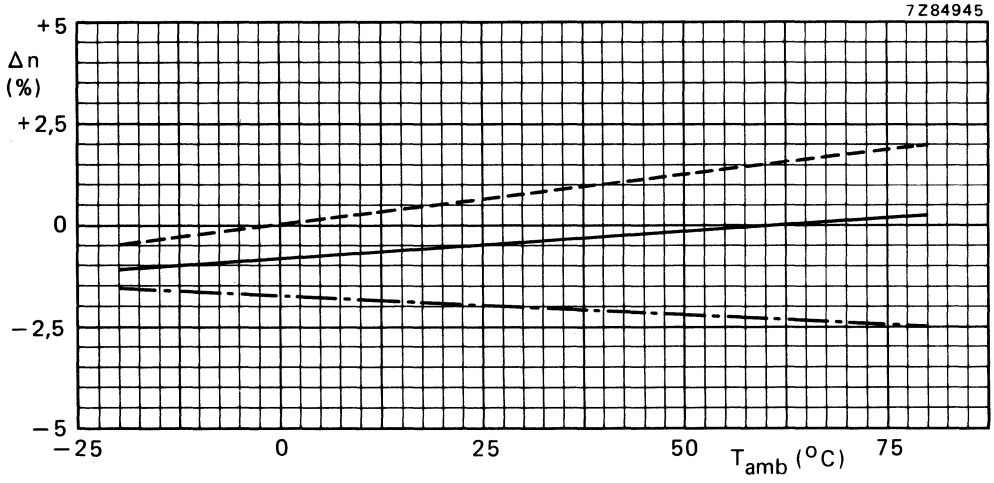


Fig. 9a V_P = 10 V.

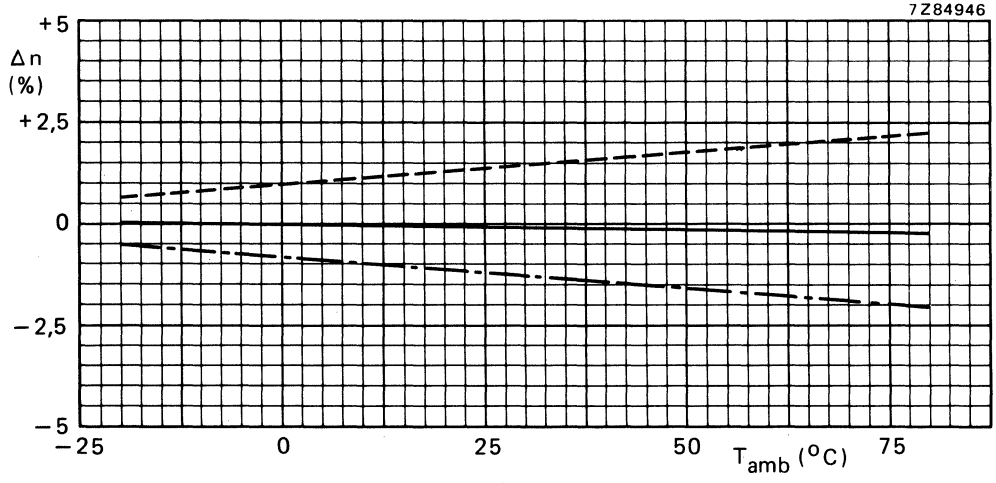


Fig. 9b V_P = 16 V.

Fig. 9 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature without diode (see Fig. 6).
— — — — —: T = 1,17 mNm
————: T = 1,30 mNm
—· — · —·—: T = 1,43 mNm

Motor Speed Regulator — TDA1559

The TDA1559 is a 3 pins speed regulator circuit for d.c. motors. It is especially intended for low-voltage motors in battery operated cassette recorder systems and record players. The IC features a high multiplication coefficient (k = 21,5) and a low drop-out voltage (0,5 V). It also contains a current limiter and thermal shut-down.

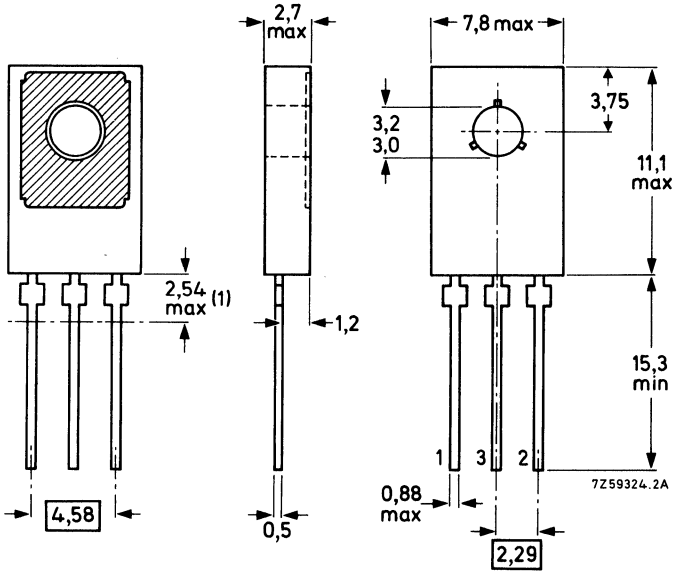
QUICK REFERENCE DATA

Supply voltage	V_P	max.	16 V
Internal reference voltage	V_{ref}	typ.	1,26 V
Drop-out voltage	V_{2-3}	typ.	0,5 V
Limited output current	$I_{2\ lim}$	typ.	0,7 A
Multiplication coefficient	k	typ.	21,5
Thermal limitation	$T_{j\ lim}$	typ.	145 °C
Operating ambient temperature range	T_{amb}		−25 to +70 °C

PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).
Pin 1 connected to metal part of mounting surface.



(1) Within this region the cross-section of the leads is uncontrolled.

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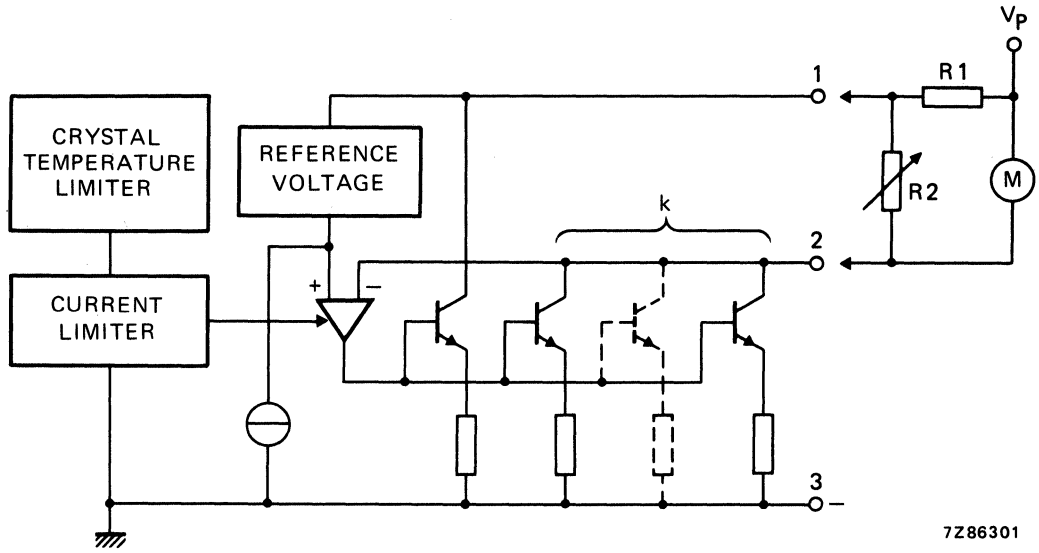


Fig. 2 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{1-3}$	max.	16	V
Output current	I_2	max.	1,2	A
Storage temperature	T_{stg}		−25 to +125	°C
Junction temperature (limited by thermal limitation)	T_j	max.	130	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=	10 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	100 K/W

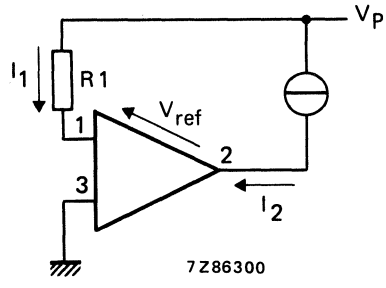


Fig. 3 Test circuit.

CHARACTERISTICS

V_P = 9 V; I_2 = 70 mA; T_{amb} = 25 °C; R1 = 0; heatsink with R_{th} = 100 K/W and after thermal stabilization; unless otherwise specified; see test circuit Fig. 3.

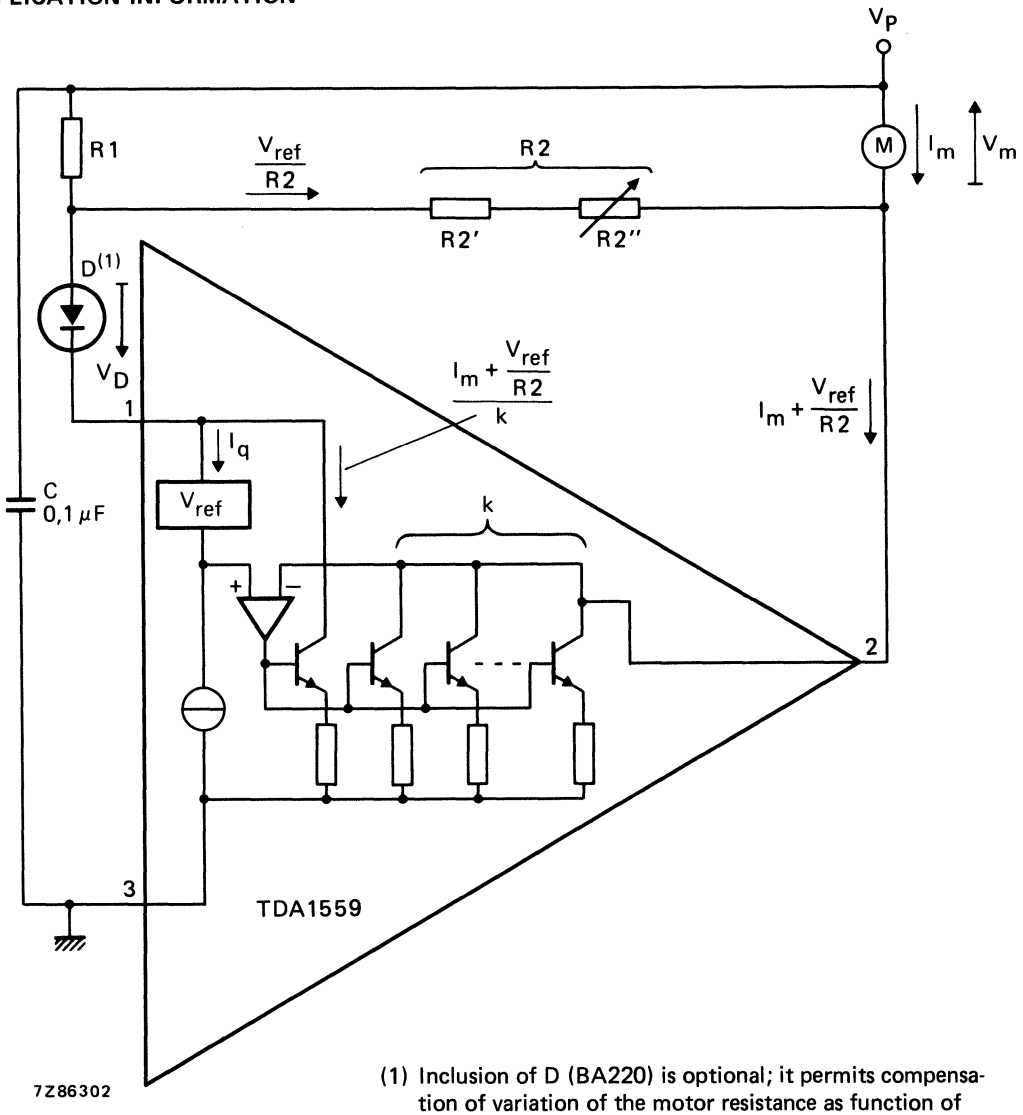
	symbol	min.	typ.	max.	unit	conditions
Internal reference voltage	$V_{ref} = V_{1-2}$	1,20	1,26	1,32	V	V_P = 2,1 V
Drop-out voltage	V_{2-3}	–	0,5	0,7	V	
	V_{2-3}	–	0,85	1,1	V	I_2 = 400 mA
Quiescent current	I_q	0,8	1,3	1,8	mA	
Limiting output current	$I_{2\,lim}$	0,45	0,7	1	A	
Multiplication coefficient*	$k = \frac{\Delta I_2}{\Delta I_1}$	19,3	21,5	24,3		ΔI_2 = ±10 mA
Thermal limitation	$T_{j\,lim}$	130	–	160	°C	V_{ref} = 1,2 V
Line regulation variation						
V_{ref} versus V_P	$\frac{\Delta V_{ref}}{\Delta V_P}$	0 0	0,9 0,07	2,0 0,16	mV/V %/V	V_P = 2,1 to 15 V
k-spread versus V_P	$\frac{\Delta k}{\Delta V_P}$	–0,3	+0,2	+1	%/V	ΔI_2 = ± 10 mA V_P = 2,1 to 15 V
I_q versus V_P	$\frac{\Delta I_q}{\Delta V_P}$	– –	11 0,95	– –	µA/V %/V	I_2 = 0 V_P = 2,1 to 15 V
Load regulation variation						
V_{ref} versus I_2	$\frac{\Delta V_{ref}}{\Delta I_2}$	–0,4 –0,03	0 0	+0,4 +0,03	V/A %/mA	I_2 = 50 to 100 mA
k-spread versus I_2	$\frac{\Delta k}{\Delta I_2}$	–0,05	0	+0,05	%/mA	I_2 = 50 to 100 mA ΔI_2 = ± 10 mA
Temperature coefficient variation						
V_{ref} versus T_{amb}	$\frac{\Delta V_{ref}}{\Delta T_{amb}}$	–0,2 –0,02	0,1 0,01	+0,4 +0,04	mV/K %/K	T_{amb} = –5 to +55 °C
k-spread versus T_{amb}	$\frac{\Delta k}{\Delta T_{amb}}$	–0,03	0	+0,03	%/K	T_{amb} = –5 to +55 °C ΔI_2 = ± 10 mA
I_q versus T_{amb}	$\frac{\Delta I_q}{\Delta T_{amb}}$	– –	–1,1 –0,08	– –	µA/K %/K	T_{amb} = –5 to +55 °C I_2 = 0

* There are 4 ranges of k-factors, indicated by either '1', '2', '3', or '4' on the package. Ordering a specific range is not possible.

1 = 19,3 to 20,5
2 = 20,3 to 21,5
3 = 21,3 to 22,7
4 = 22,5 to 24,3

7

APPLICATION INFORMATION



(1) Inclusion of D (BA220) is optional; it permits compensation of variation of the motor resistance as function of temperature.

Fig. 4 Example of using the TDA1559 in a d.c. motor speed regulation circuit.

Notes to Fig. 4

$R2 = R2' + R2''$

$E_n = n \times C \times \phi$ where: n = speed in revolutions per minute

$I_m = T \times \frac{2\pi}{60} = \frac{1}{C.\phi}$ C = motor constant

ϕ = magnetic flux

E_n = electromotive force (e.m.f.)

T = motor torque

R_m = motor resistance

E_n can be expressed as:

$$E_n = I_m\left(\frac{R1}{k} - R_m\right) + V_{ref}\left\{1 + \frac{R1}{R2}\left(1 + \frac{1}{k}\right)\right\} + R2 \times I_q$$

For optimal regulation (dn/dT = 0), $\left(\frac{R1}{k} - R_m\right)$ should be zero.

However, if $R1 = k \times R_m$, the regulator will be oscillating, so for stability always $R1 < k \times R_m$.

R2 is determined by:

$$R2 = \frac{V_{ref} \times R1 \times \left(1 + \frac{1}{k}\right)}{E_n - (R1 \times I_q) - V_{ref} - I_m\left(\frac{R1}{k} - R_m\right)}$$

Example:

$E_n = E_{2000} = 3{,}58\ V \pm 11{,}6\%$
$R_m = 13\ \Omega \pm 10\%$
n = 2000 rev/min
T = 1 mNm
$R1 = 220\ \Omega$
$R2' = 82\ \Omega$
$R2'' = 220\ \Omega$

When a diode (D = BA220) is connected is series with pin 1, then the expressions for R2 and E_n are:

$$R2 = \frac{(V_{ref} + V_D) \times R1 \times \left(1 + \frac{1}{k}\right)}{E_n - (R1 \times I_q) - (V_{ref} + V_D) - I_m\left(\frac{R1}{k} - R_m\right)}$$

$$E_n = I_m\left(\frac{R1}{k} - R_m\right) + (V_{ref} + V_D)\left\{1 + \frac{R1}{R2}\left(1 + \frac{1}{k}\right)\right\} + R2 + I_q$$

Example:

$E_n = E_{2000} = 3{,}58\ V \pm 11{,}6\%$
$R_m = 13\ \Omega \pm 10\%$
n = 2000 rev/min
T = 1 mNm
$R1 = 220\ \Omega$
$R2' = 160\ \Omega$
$R2'' = 470\ \Omega$
D = BA220

7

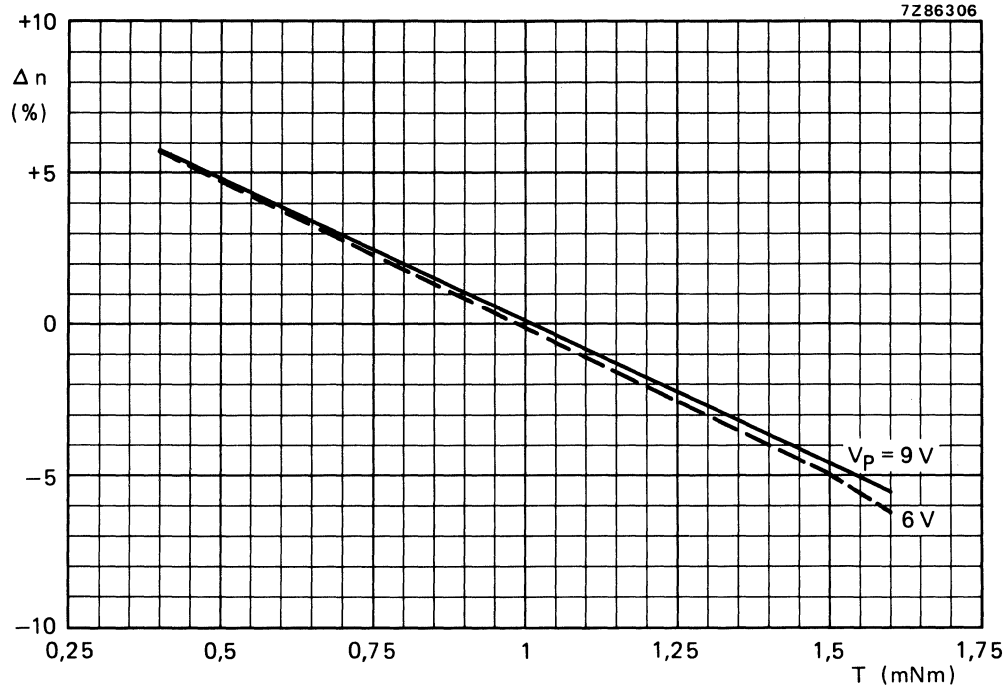


Fig. 5 Variation in motor speed (n is revolutions per minute) as a function of the applied motor torque at T_{amb} = 25 °C.

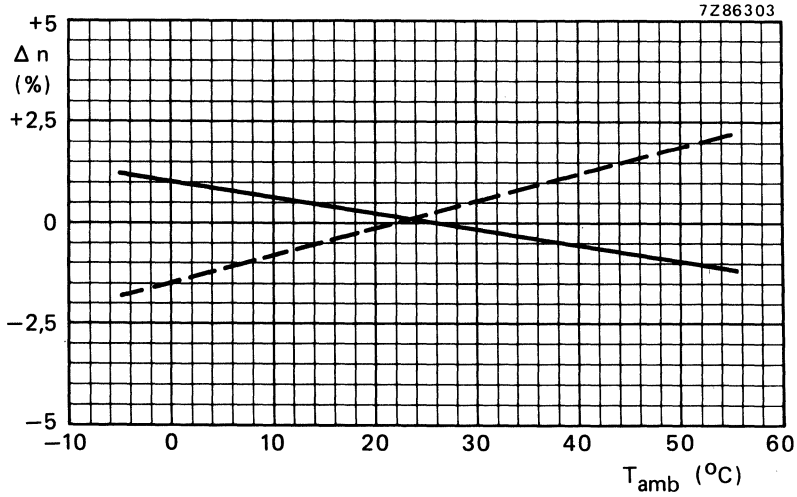


Fig. 6 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature at T = 1 mNm nominal and V_P = 9 V.

————————: with diode (D = BA220; see Fig. 4).

— — — — —: without diode.

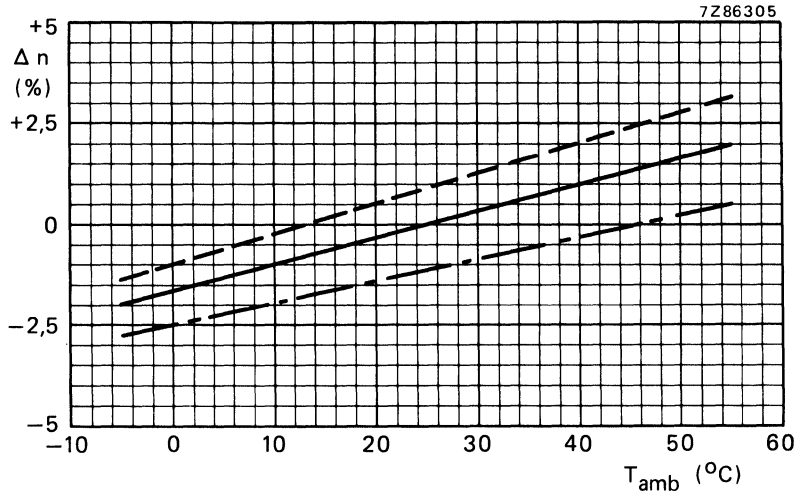


Fig. 7a V_P = 6 V.

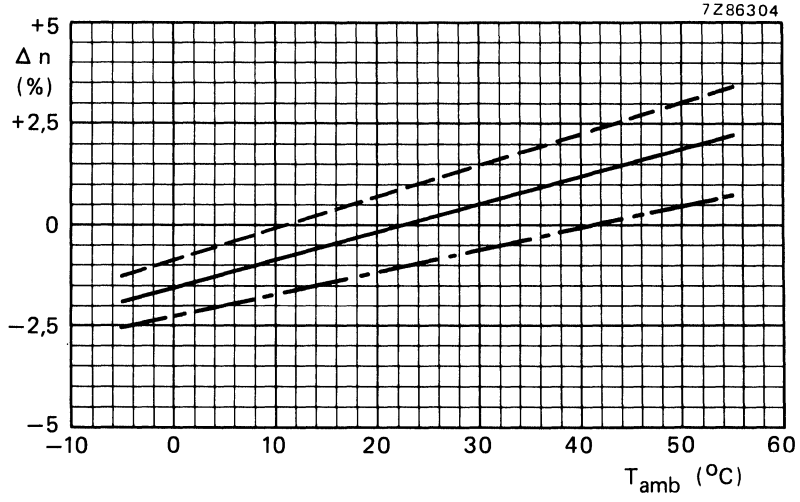


Fig. 7b V_P = 9 V.

Fig. 7 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature without diode (D = BA220; see Fig. 4).

– – – – – – – : T = 0,9 mNm
——————— : T = 1,0 mNm
– · – · – · – : T = 1,1 mNm

Stepping Motor Control Circuit TEA1012

GENERAL DESCRIPTION

The circuit is intended to drive two phase stepping motors in full step as well in half step mode. The logic part is driven by four input stages:

CL — a clock signal input stage
F/$\overline{H}$ — to select the full step or half step mode
$\overline{CW}$/CCW — to select clockwise or counter clockwise direction
$\overline{STOP}$ — to stop the motor after the last step is completed

The input stages are TTL compatible. The circuit contains also a bi-level switch for bi-level voltage drive of the motorcoils.
Moreover the circuit offers a constant current motordrive capability, independent of the i.c. supply and motordrive voltage.

Features

- TTL inputs, all logic included
- Full/half step mode
- Bi-level output control
- Optimum system by external drivers
- Closed loop current control
- Free choice of motor supply voltage
- Wide i.c. supply voltage range
- One i.c. per motor
- Simple system design

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	4,5 to 16	V
Supply current (without load)	I_{CC}	typ. 6,5	mA
Output current (per output)	I_O	> 50	mA
Operating ambient temperature range	T_{amb}	−20 to + 80	°C

PACKAGE OUTLINE

TEA1012P: 16-lead dual in-line; plastic (SOT-38).

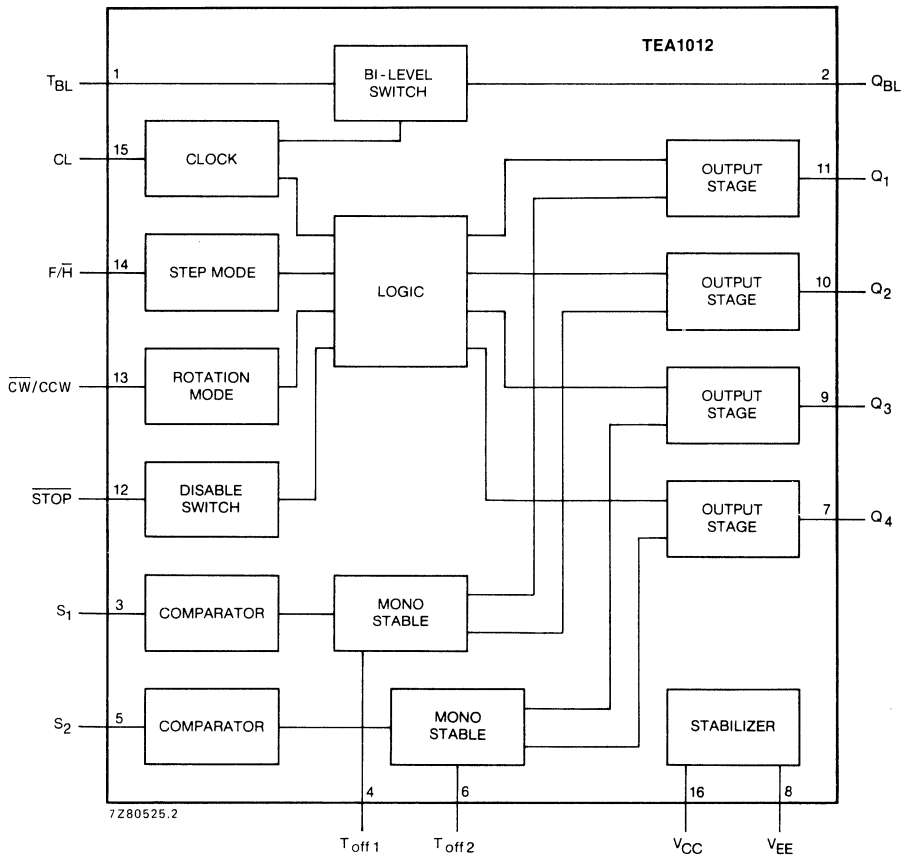


Fig. 1 Block diagram.

Pin designation

1	T_{BL}	bi-level time adjustment
2	Q_{BL}	bi-level switch output
3	S_1	current sense input 1
4	T_{off1}	monostable period setting 1
5	S_2	current sense input 2
6	T_{off2}	monostable period setting 2
7	Q_4	output 4
8	V_{EE}	negative supply (ground)
9	Q_3	output 3
10	Q_2	output 2
11	Q_1	output 1
12	$\overline{STOP}$	stop input (last step)
13	$\overline{CW}$/CCW	direction control
14	F/$\overline{H}$	full/half step mode control
15	CL	clock input (step freq.)
16	V_{CC}	positive supply

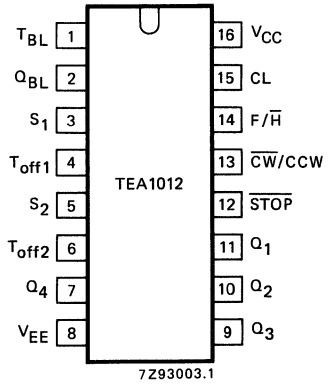


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

function	pin	description
CL	15	Clock input The leading edge of the clock input triggers the circuit.
F/$\overline{H}$	14	Full/half step mode Determines full step or half step mode of operation. Full step active HIGH; Half step mode active LOW.
$\overline{CW}$/CCW	13	Clock wise/Counter clock wise Input to determine the direction of rotation. CW active LOW; CCW mode active HIGH.
$\overline{STOP}$	12	Stop At LOW level the last output current combination is fixed and the other inputs are disabled. A step in progress will be finished.
Q_1 Q_2 Q_3 Q_4	11 10 9 7	Drive outputs to the motor current switches.
$S_{1,2}$	3, 5	Current sense inputs 1 and 2 If the voltage-drop across the sense-resistor in the motor current loop exceeds 0,4 V the internal comparator will be activated.
$T_{off1,2}$	4, 6	Monostable period settings 1 and 2 After activation of the current sense comparator circuit a one-shot is triggered. The timing of this one-shot is determined by the R/C network connected to this pin.
Q_{BL}	2	Bi-level switch output Output terminal to activate the external bi-level drive transistor (active is LOW).
T_{BL}	1	Bi-level time adjustment. The R/C network connected to this pin determines the on-time of the bi-level drive transistor.
V_{CC}	16	Positive supply to the circuit.
V_{EE}	8	Negative supply to the circuit (ground).

TRUTH TABLE

Sequential logical states of the outputs in full step and half step mode.

INPUTS				OUTPUTS			
CL	F/$\overline{H}$	$\overline{CW}$/CCW	$\overline{STOP}$	Q_1	Q_2	Q_3	Q_4
half step mode		ccw					
∫	0	1	1	0	0	0	1
∫	0	1	1	0	1	0	1
∫	0	1	1	0	1	0	0
∫	0	1	1	0	1	1	0
∫	0	1	1	0	0	1	0
∫	0	1	1	1	0	1	0
∫	0	1	1	1	0	0	0
∫	0	1	1	1	0	0	1
half step mode		cw					
∫	0	0	1	1	0	0	1
∫	0	0	1	1	0	0	0
∫	0	0	1	1	0	1	0
∫	0	0	1	0	0	1	0
∫	0	0	1	0	1	1	0
∫	0	0	1	0	1	0	0
∫	0	0	1	0	1	0	1
∫	0	0	1	0	0	0	1
full step mode		cw					
∫	1	0	1	1	0	0	1
∫	1	0	1	1	0	1	0
∫	1	0	1	0	1	1	0
∫	1	0	1	0	1	0	1
full step mode		ccw					
∫	1	1	1	0	1	0	1
∫	1	1	1	0	1	1	0
∫	1	1	1	1	0	1	0
∫	1	1	1	1	0	0	1

Positive logic:
1 = H = HIGH state
= the more positive voltage
0 = L = LOW state
= the less positive voltage
∫ = LOW to HIGH transition

7

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	18 V
Output voltage $Q_{1, 2, 2, 4}$, Q_{BL}, $T_{off1,2}$	V_O	max.	18 V
Input voltages	V_I	max.	V_{CC} + 0,4 V
Total power dissipation	P_{tot}	max.	500 mW
Storage temperature range	T_{stg}		−40 to + 150 °C
Operating ambient temperature range	T_{amb}		−20 to + 80 °C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c\text{-}a}$	=	75 K/W

CHARACTERISTICS

V_{CC} = 7,5 V, T_{amb} = 25 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{CC}	4,5	5	16	V
Supply current	I_{CC}	4,5	6,5	18	mA
Output current; V_{CC} = 7,5 V	I_Q	75	–	–	mA
Output current; V_{CC} = 5 V	I_Q	50	–	–	mA
Saturation output voltage					
I_Q = 30 mA	V_{Qsat}	–	–	0,3	V
I_Q = 50 mA; $V_{CC} > 7,5$ V	V_{Qsat}	–	–	0,5	V
Pulse width factor (k x R x C)					
of chopper drive $T_{off1, 2}$	k	0,74	–	0,92	
of monostable T_{BL}	k	0,74	–	0,92	
Output current Q_{BL}	I_{QBL}	20	–	–	mA
Switching level of input stages	V_I	0,8	1,4	2,0	V
Input current of input stages					
V_I HIGH	I_I	–	–	2	μA
V_I LOW	$-I_I$	–	–	10	μA

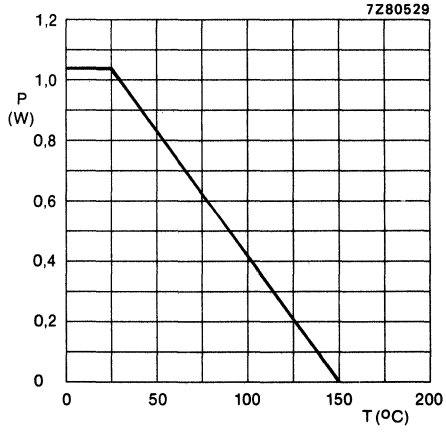


Fig. 3 Power derating curve.

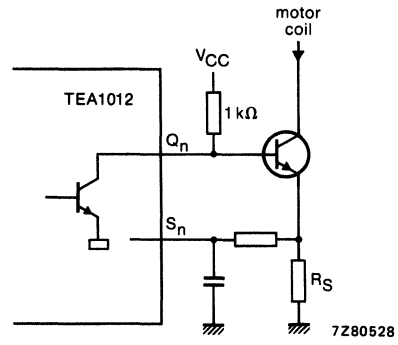


Fig. 4 IC output; motor drive stage.

In case of driving the motor by a bi-level switch, resistor R_S and the low-pass filter can be omitted; inputs S_1 and S_2 should be connected to ground.

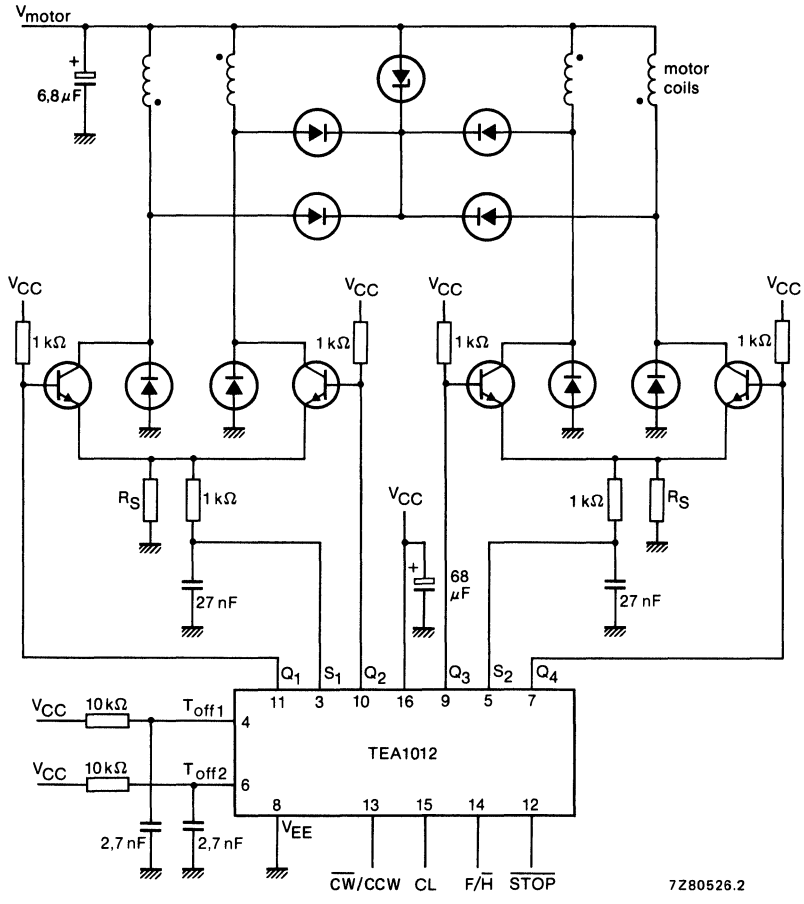


Fig. 5 Application circuit diagram constant current mode.

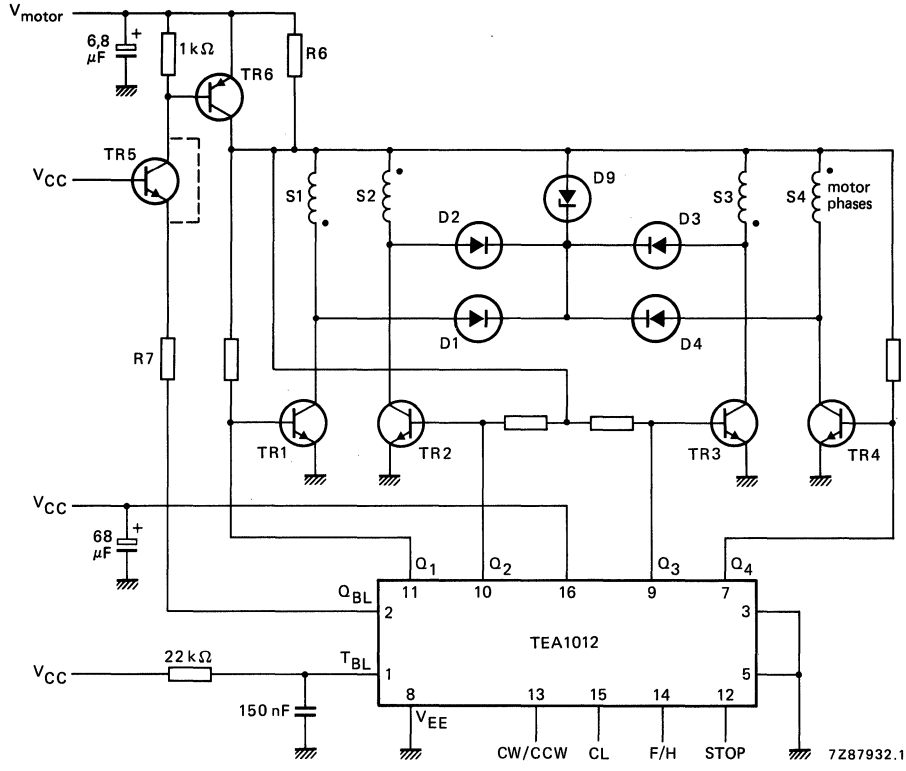
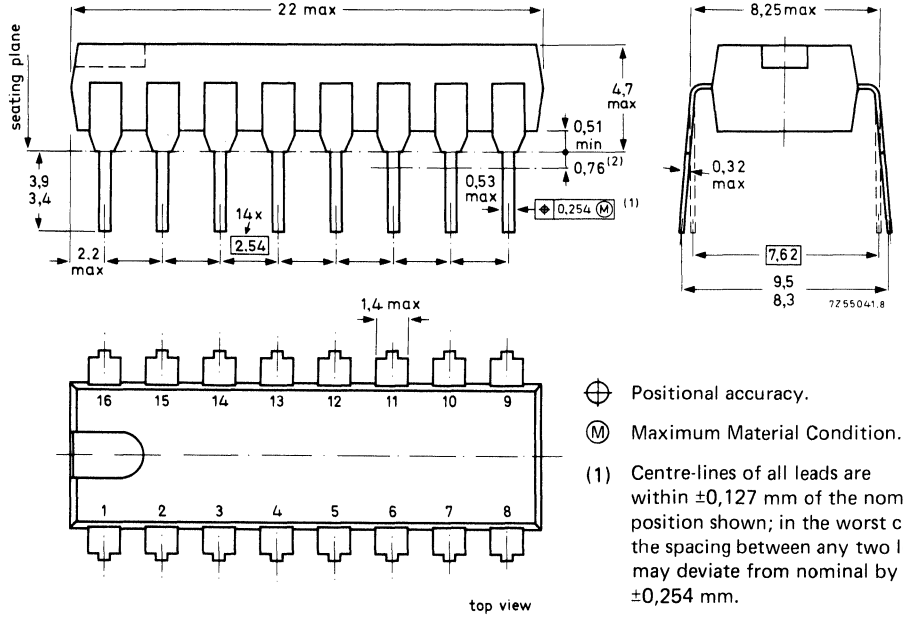


Fig. 6 Application circuit diagram bi-level mode.

In case $V_m < 18$ V it is possible that $V_m = V_{CC}$. Then TR1 can be omitted and output Q_{BL} can be connected directly to the base of TR2 (dotted line).

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

7

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

Time Proportional Triac Trigger TDA1023

GENERAL DESCRIPTION

The TDA1023 is a bipolar integrated circuit for controlling triacs in the time proportional or burst firing mode. It permits very precise temperature control of heating equipment and is especially suited for the control of panel heaters. The circuit generates positive-going trigger pulses and complies with the regulations on radio interference and mains distortion.

Special features are:

- adjustable proportional range width
- adjustable hysteresis
- adjustable trigger pulse width
- adjustable firing burst repetition time
- control range translation facility
- failsafe operation
- supplied from the mains
- provides supply for external temperature bridge

QUICK REFERENCE DATA

Supply voltage (derived from mains voltage)	V_{CC}	typ.	13.7 V
Stabilized supply voltage for temperature bridge	V_Z	typ.	8 V
Supply current (average value)	$I_{16(AV)}$	typ.	10 mA
Trigger pulse width	t_w	typ.	200 μs
Firing burst repetition time at C_T = 68 μF	T_b	typ.	41 s
Output current	$-I_{OH}$*	max.	150 mA
Operating ambient temperature range	T_{amb}		−20 to + 75 °C

* Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

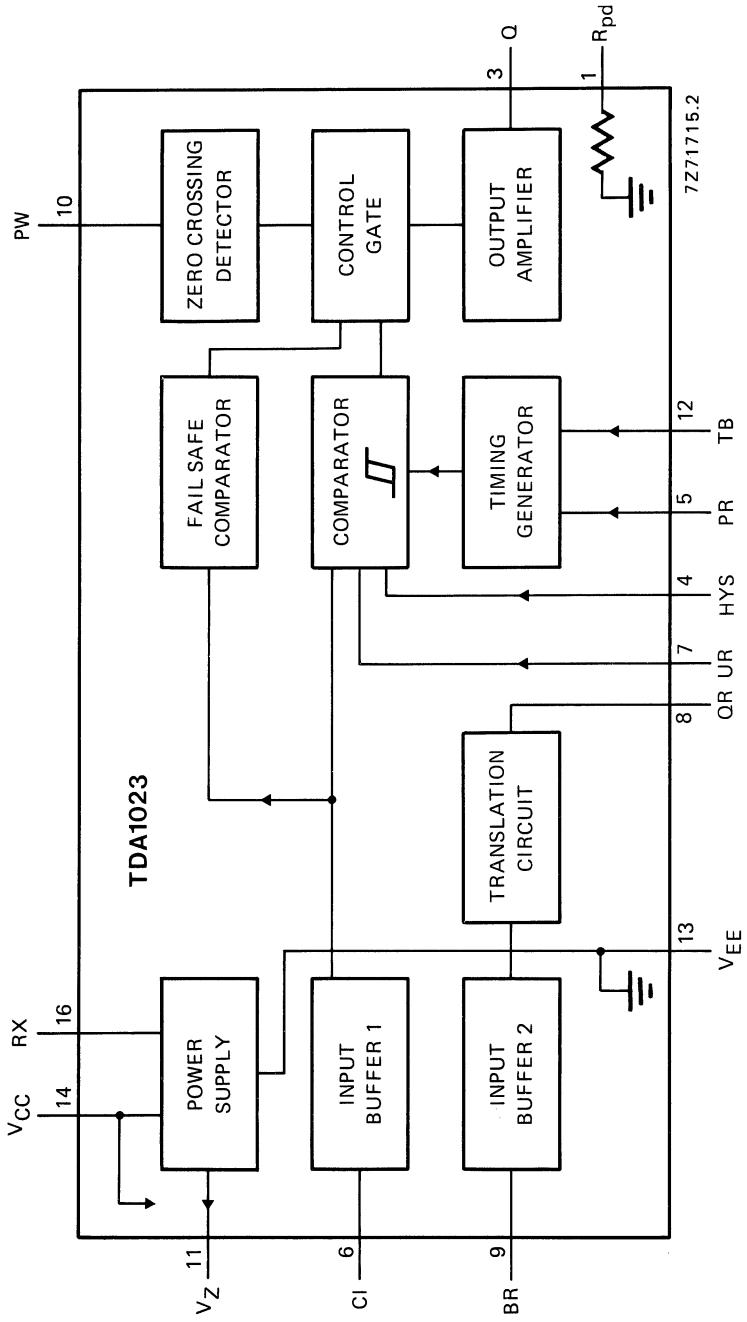


Fig. 1 Block diagram.

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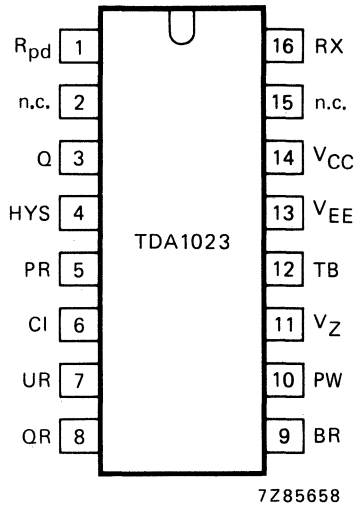

Fig. 2 Pinning diagram.

PINNING

1	R_{pd}	internal pull-down resistor connection
2	n.c.	not connected
3	Q	output
4	HYS	hysteresis control input
5	PR	proportional range control input
6	CI	Control input
7	UR	unbuffered reference input
8	QR	output of reference buffer
9	BR	buffered reference input
10	PW	pulse width control input
11	V_Z	reference supply output
12	TB	firing burst repetition time control input
13	V_{EE}	ground connection
14	V_{CC}	positive supply connection
15	n.c.	not connected
16	RX	external resistor connection

FUNCTIONAL DESCRIPTION

The TDA1023 generates pulses to trigger a triac. These trigger pulses coincide with the zero crossings of the mains voltage. This minimizes r.f. interference and transients on the mains supply. The trigger pulses come in bursts, with the net effect that the load is periodically switched on and off. This further minimizes mains pollution. The average power in the load is varied by varying the duration of the trigger pulse burst, in accordance with the voltage difference between the control input CI and the reference input, either UR or BR.

Power supply: V_{CC}, RX and V_Z (pins 14, 16 and 11)

The TDA1023 is supplied from the a.c. mains via a resistor R_D to the RX connection (pin 16); the V_{EE} connection (pin 13) is connected to the neutral line (see Fig. 4a). A smoothing capacitor C_S has to be connected between the V_{CC} and V_{EE} connections.

The circuit contains a string of stabilizer diodes between the RX and V_{EE} connections that limit the d.c. supply voltage, and a rectifier diode between the RX and V_{CC} connections (see Fig. 3).

At pin 11 the device provides a stabilized reference voltage V_Z for an external temperature sensing bridge.

The operation of the supply arrangement is as follows. During the positive half of the mains cycles the current through external voltage dropping resistor R_D charges the external smoothing capacitor C_S until RX reaches the stabilizing voltage of the internal stabilizer diodes. R_D should be chosen such that it can supply the current I_{CC} for the TDA1023 itself plus the average output current $I_{3(AV)}$ plus the current required from the V_Z connection for an external temperature bridge, and recharge the smoothing capacitor C_S (see Figs 9 to 12). Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S has to supply the sum of the currents mentioned above. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit.

FUNCTIONAL DESCRIPTION (continued)

Dissipation in resistor R_D is halved by connecting a diode in series (see Fig. 4b and 9 to 12).

A further reduction of dissipation is possible by using a high-quality voltage dropping capacitor C_D in series with a resistor R_{SD} (see Figs 4c and 14). Asuitable VDR connected across the mains provides protection of the TDA1023 and of the triac against mains-borne transients.

Control and reference inputs CI, BR and UR (pins 6, 9 and 7)

For room temperature control (5 °C to 30 °C) the best performance is obtained by using the translation circuit. The buffered reference input BR (pin 9) is used as a reference input, and the output of the reference buffer QR (pin 8) is connected to the unbuffered reference input UR (pin 7). In this arrangement the translation circuit ensures that most of the potentiometer rotation can be used to cover the room temperature range. This provides an accurate temperature setting and a linear temperature scale.

If the translation circuit is not required, the unbuffered reference input UR (pin 7) is used as a reference input. The buffered reference input BR (pin 9) must be connected to the reference supply output V_Z (pin 11).

For proportional power control the unbuffered reference input UR (pin 7) must be connected to the firing burst repetition time control input TB (pin 12) and the buffered reference input BR (pin 9), which is inactive now, must be connected to the reference supply output V_Z (pin 11).

In all arrangements the train of output pulses becomes longer when the voltage at the control input CI (pin 6) becomes lower.

Proportional range control input PR (pin 5)

With the proportional range control input PR open the output duty factor changes from 0% to 100% by a variation of 80 mV at the control input CI (pin 6). For temperature control this corresponds with a temperature difference of only 1 K.

This range may be increased to 400 mV, i.e. 5 K, by connecting the proportional range control input PR (pin 5) to ground. Intermediate values are obtained by connecting the PR input to ground via a resistor R5, see Table 1.

Hysteresis control input HYS (pin 4)

With the hysteresis control input HYS (pin 4) open the device has a built-in hysteresis of 20 mV. For temperature control this corresponds with 0.25 K.

Hysteresis is increased to 320 mV, corresponding with 4 K, by grounding HYS (pin 4). Intermediate values are obtained by connecting pin 4 to ground via a resistor R4. See Table 1 for a set of values for R4 and R5 giving a fixed ratio between hysteresis and proportional range.

Trigger pulse width control input PW (pin 10)

The trigger pulse width may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor R_S between the trigger pulse width control input PW (pin 10) and the a.c. mains. The pulse width is inversely proportional to the input current (see Fig. 13).

Output Q (pin 3)

Since the circuit has an open-emitter output, it is capable of sourcing current, i.e. supplying a current out of the output. Therefore it is especially suited for generating positive-going trigger pulses. The output is current-limited and protected against short-circuits. The maximum output current is 150 mA and the output pulses are stabilized at 10 V for output currents up to that value.

FUNCTIONAL DESCRIPTION (continued)

A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figs 5 to 8). This minimizes the total supply current and the power dissipation.

Pull-down resistor R_{pd} (pin 1)

The TDA1023 includes a 1.5 kΩ pull-down resistor R_{pd} between pins 1 and 13 (V_{EE}, ground connection), intended for use with sensitive triacs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	16	V
Supply current				
average	$I_{16(AV)}$	max.	30	mA
repetitive peak	$I_{16(RM)}$	max.	100	mA
non-repetitive peak	$I_{16(SM)}$	max.	2	A
Input voltage, all inputs	V_I	max.	16	V
Input current, CI, UR, BR, PW input	$I_{6;7;9;10}$	max.	10	mA
Voltage on R_{pd} connection	V_1	max.	16	V
Output voltage, Q, QR, V_Z output	$V_{3;8;11}$	max.	16	V
Output current				
average	$-I_{OH(AV)}$	max.	30	mA
peak, max. 300 μs	$-I_{OH(M)}$	max.	700	mA
Total power dissipation	P_{tot}	max.	500	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−20 to +	75	°C

CHARACTERISTICS

V_{CC} = 11 to 16 V; T_{amb} = −20 to + 75 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply: V_{CC} and RX (pins 14 and 16)					
Internally stabilized supply voltage at I_{16} = 10 mA	V_{CC}	12	13.7	15	V
Variation with I_{16}	$\Delta V_{CC}/\Delta I_{16}$	–	30	–	mV/mA
Supply current at V_{16-13} = 11 to 16 V; I_{10} = 1 mA; f = 50 Hz; pin 11 open; $V_{6-13} > V_{7-13}$; pins 4 and 5 open	I_{16}	–	–	6	mA
pins 4 and 5 grounded	I_{16}	–	–	7.1	mA
Reference supply output V_Z (pin 11) for external temperature bridge					
Output voltage	V_{11-13}	–	8	–	V
Output current	$-I_{11}$	–	–	1	mA
Control and reference inputs CI, BR and UR (pins 6, 9 and 7)					
Input voltage to inhibit the output	V_{6-13}	–	7.6	–	V
Input current at V_I = 4 V	$I_{6;7;9}$	–	–	2	μA
Hysteresis control input HYS (pin 4)					
Hysteresis, pin 4 open	ΔV_6	9	20	40	mV
pin 4 grounded	ΔV_6	–	320	–	mV
Proportional range control input PR (pin 5)					
Proportional range, pin 5 open	ΔV_6	50	80	130	mV
pin 5 grounded	ΔV_6	–	400	–	mV
Pulse width control input PW (pin 10)					
Pulse width at $I_{10(RMS)}$ = 1 mA; f = 50 Hz	t_w	100	200	300	μs
Firing burst repetition time control input TB (pin 12)					
Firing burst repetition time, ratio to capacitor C_T	T_b/C_T	320	600	960	ms/μF
Output of reference buffer QR (pin 8)					
Output voltage at input voltage V_{9-13} = 1.6 V	V_{8-13}	–	3.2	–	V
V_{9-13} = 4.8 V	V_{8-13}	–	4.8	–	V
V_{9-13} = 8 V	V_{8-13}	–	6.4	–	V

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	symbol	min.	typ.	max.	unit
Output Q (pin 3)					
Output voltage HIGH at $-I_{OH}$ = 150 mA	V_{OH}	10	–	–	V
Output current HIGH	$-I_{OH}$	–	–	150	mA
Internal pull-down resistor R_{pd} (pin 1)					
Resistance to V_{EE}	R_{pd}	1	1.5	3	kΩ

Table 1. Adjustment of proportional range and hysteresis.
Combinations of resistor values giving hysteresis > ¼ proportional range.

proportional range mV	proportional range resistor R5 kΩ	minimum hysteresis mV	maximum hysteresis resistor R4 kΩ
80	open	20	open
160	3.3	40	9.1
240	1.1	60	4.3
320	0.43	80	2.7
400	0	100	1.8

Table 2. Timing capacitor C_T values.

effective d.c. value	marked a.c. specification		catalogue number*
μF	μF	V	
68	47	25	2222 016 90129
47	33	40	– – 90131
33	22	25	– 015 90102
22	15	40	– – 90101
15	10	25	– – 90099
10	6.8	40	– – 90098

* Special electrolytic capacitors recommended for use with TDA1023.

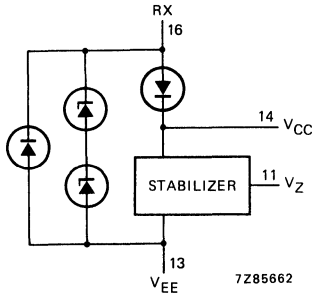

Fig. 3 Internal supply connections.

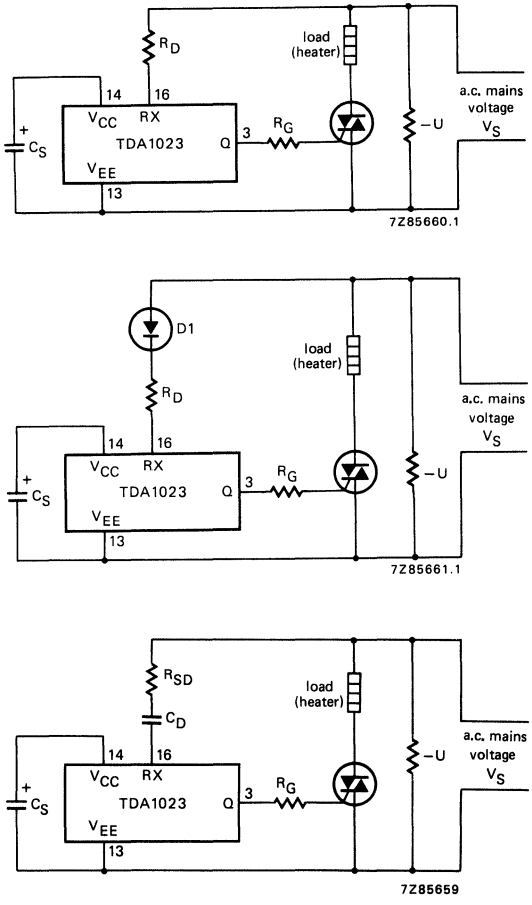

Fig. 4 Alternative supply arrangements.

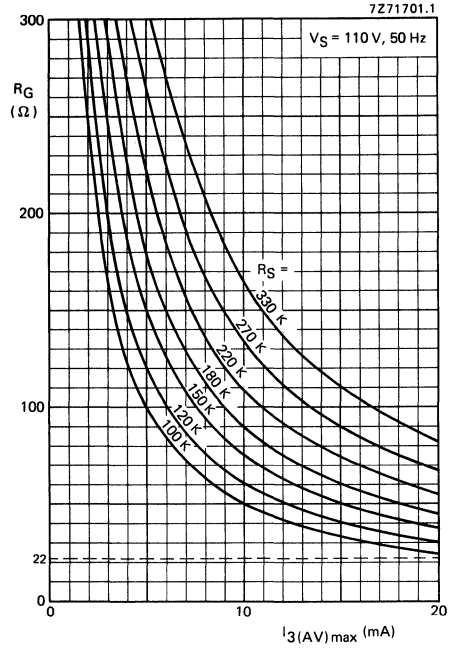

Fig. 5.

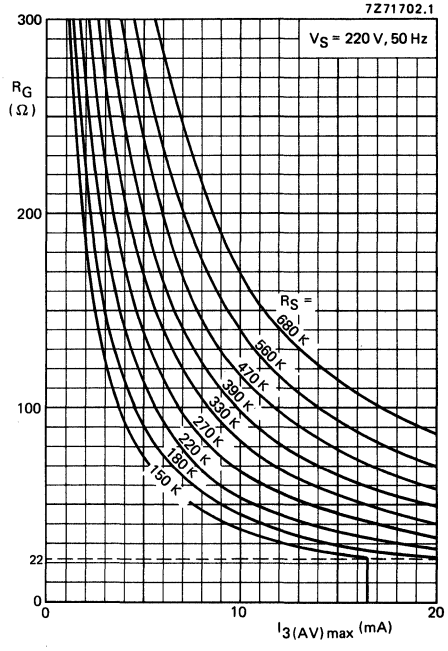

Fig. 6.

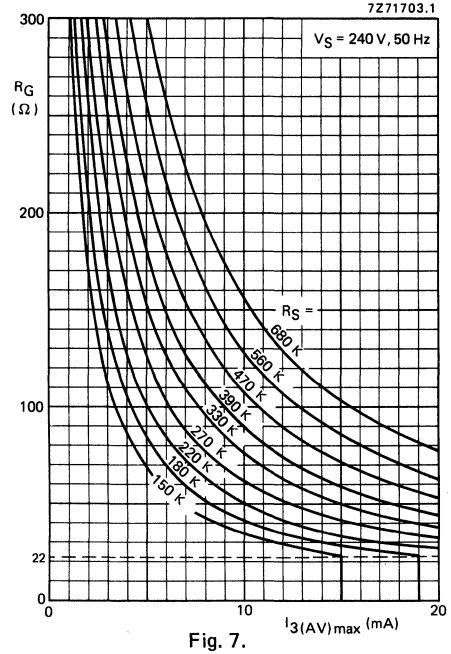

Fig. 7.

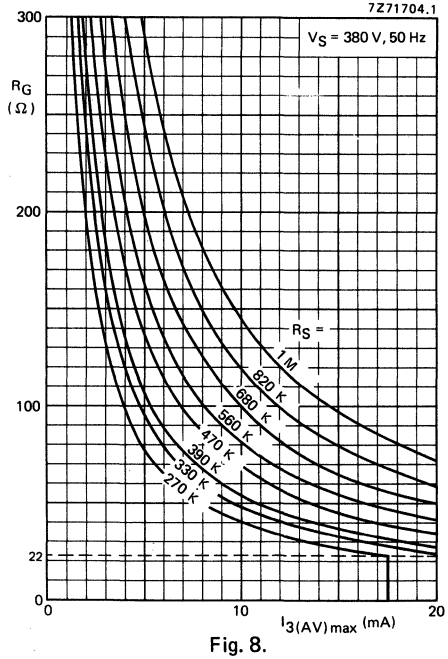

Fig. 8.

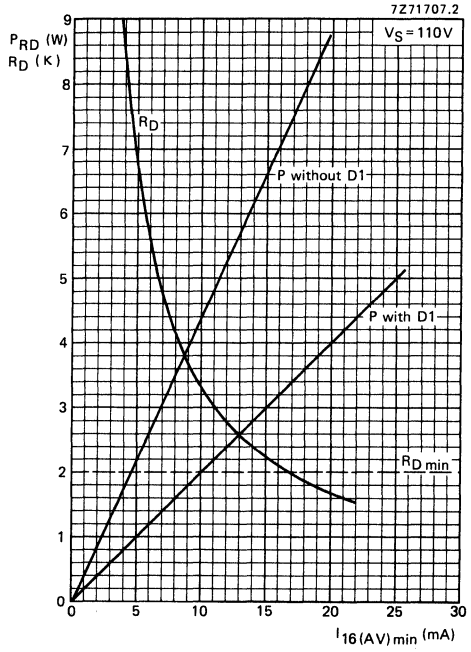

Fig. 9.

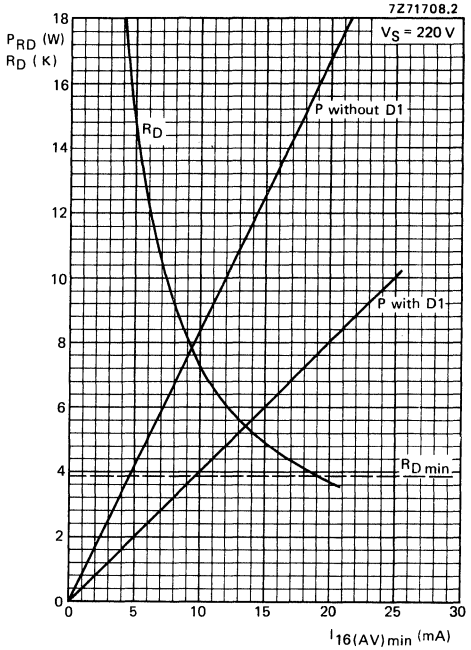

Fig. 10.

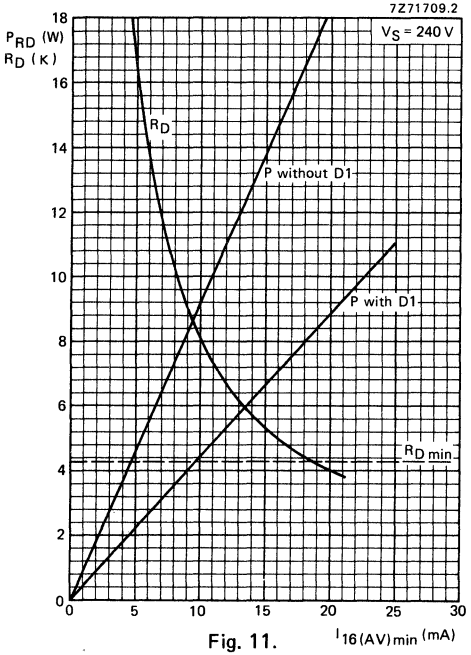

Fig. 11.

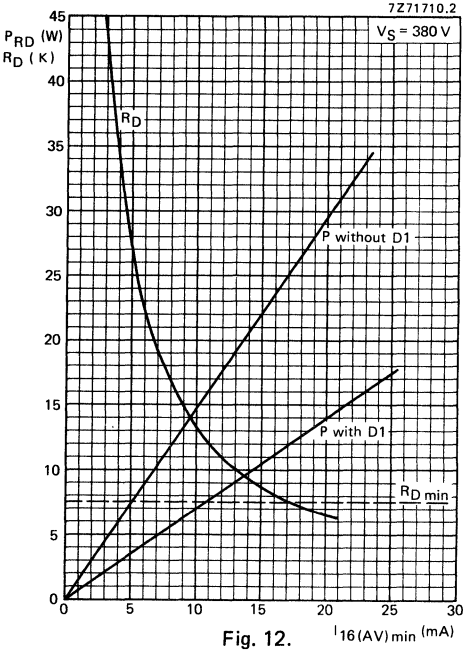

Fig. 12.

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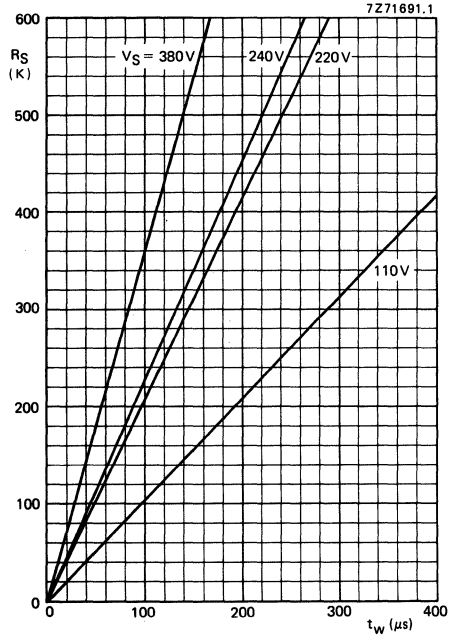

Fig. 13 Synchronization resistor R_S as a function of required trigger pulse width t_W with mains voltage V_S as a parameter.

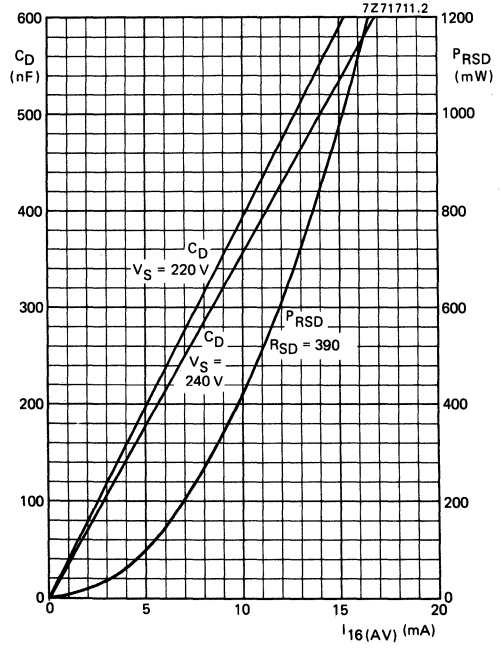

Fig. 14 Nominal value of voltage dropping capacitor C_D and power P_{RSD} dissipated in voltage dropping resistor R_{SD} as a function of the average supply current $I_{16(AV)}$ with the mains supply voltage V_S as a parameter.

APPLICATION INFORMATION

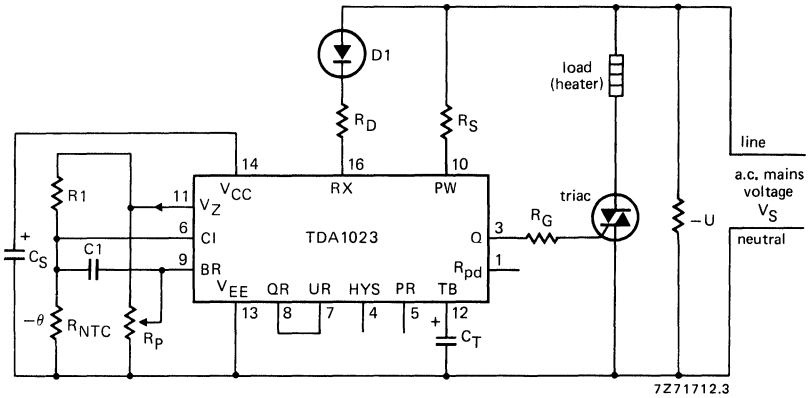

Fig. 15 The TDA1023 used in a 1200 to 2000 W heater with triac BT139. For component values see Table 3.

Conditions

Mains supply: V_S = 220 V

Temperature range = 5 to 30 °C

BT139 data: $V_{GT} < 1.5$ V; $I_{GT} > 70$ mA; $I_L < 60$ mA } at T_j = 25 °C

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Table 3. Temperature controller component values (see Fig. 15).

parameter	symbol	value	remarks
Trigger pulse width	t_W	75 μs	see BT139 data sheet
Synchronization resistor	R_S	180 kΩ	see Fig. 13
Gate resistor	R_G	110 Ω	see Fig. 6
Max. average gate current	$I_{3(AV)}$	4.1 mA	see Fig. 8
Hysteresis resistor	R4	n.c.	see Table 1
Proportional band resistor	R5	n.c.	see Table 1
Min. required supply current	$I_{16(AV)}$	11.1 mA	
Mains dropping resistor	R_D	6.2 kΩ	see Fig. 10
Power dissipated in R_D	P_{RD}	4.6 W	see Fig. 10
Timing capacitor (eff. value)	C_T	68 μF	see Table 2
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 593 62512
Rectifier diode	D1	BYW56	
Resistor to pin 11	R1	18.7 kΩ	1% tolerance
NTC thermistor (at 25 °C)	R_{NTC}	22 kΩ	B = 4200 K cat. no. 2322 642 12223
Potentiometer	R_P	22 kΩ	
Capacitor between pins 6 and 9	C1	47 nF	
Smoothing capacitor	C_S	220 μF; 16 V	
If R_D and D1 are replaced by C_D and R_{SD}			
Mains dropping capacitor	C_D	470 nF	see Fig. 14
Series dropping resistor	R_{SD}	390 Ω	
Power dissipated in R_{SD}	P_{RSD}	0.6 W	
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 594 62512

Notes

1. ON/OFF control: pin 12 connected to pin 13.
2. If translation circuit is not required: slider of R_P to pin 7; pin 8 open; pin 9 connected to pin 11.

APPLICATION INFORMATION SUPPLIED ON REQUEST

Zero Crossing Triac Trigger TDA1024

GENERAL DESCRIPTION

The TDA1024 is a bipolar integrated circuit delivering positive pulses for triggering a triac or a thyristor. It is primarily intended for use as a static switch to replace mechanical thermostats that switch resistive loads, such as:

- central heating installations
- washing machine heaters
- water heaters
- smoothing irons

The TDA1024 provides its own d.c. supply and will supply an external circuit, e.g. a temperature sensing bridge. The circuit complies with the regulations on radio interference and mains distortion.

Its main features are:

- adjustable trigger pulse width
- adjustable hysteresis
- supplied from the mains
- provides supply for external temperature bridge
- protected inputs and output
- low supply current, low dissipation

QUICK REFERENCE DATA

Supply voltage (d.c.) (internally derived from mains voltage)	V_{CC}	typ.	6.5	V
Supply current (average value, unloaded)	$I_{RX(AV)}$	max.	1.8	mA
Output current HIGH	$-I_{OH}$*	max.	100	mA
Output pulse width	t_w	typ.	195	μs
Power dissipation (unloaded)	P	typ.	12	mW
Operating ambient temperature range	T_{amb}		−20 to +80	°C

* Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

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PACKAGE OUTLINE

8-lead DIL; plastic (SOT-97A).

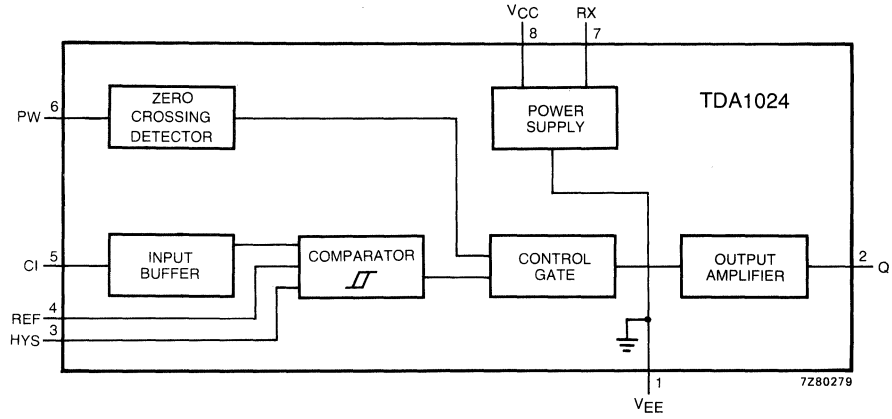

Fig. 1 Block diagram.

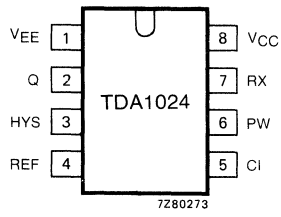

Fig. 2 Pinning diagram.

PINNING

1	V_{EE}	ground
2	Q	output
3	HYS	hysteresis control input
4	REF	reference input
5	CI	control input
6	PW	pulse width control input
7	RX	external resistor
8	V_{CC}	positive supply

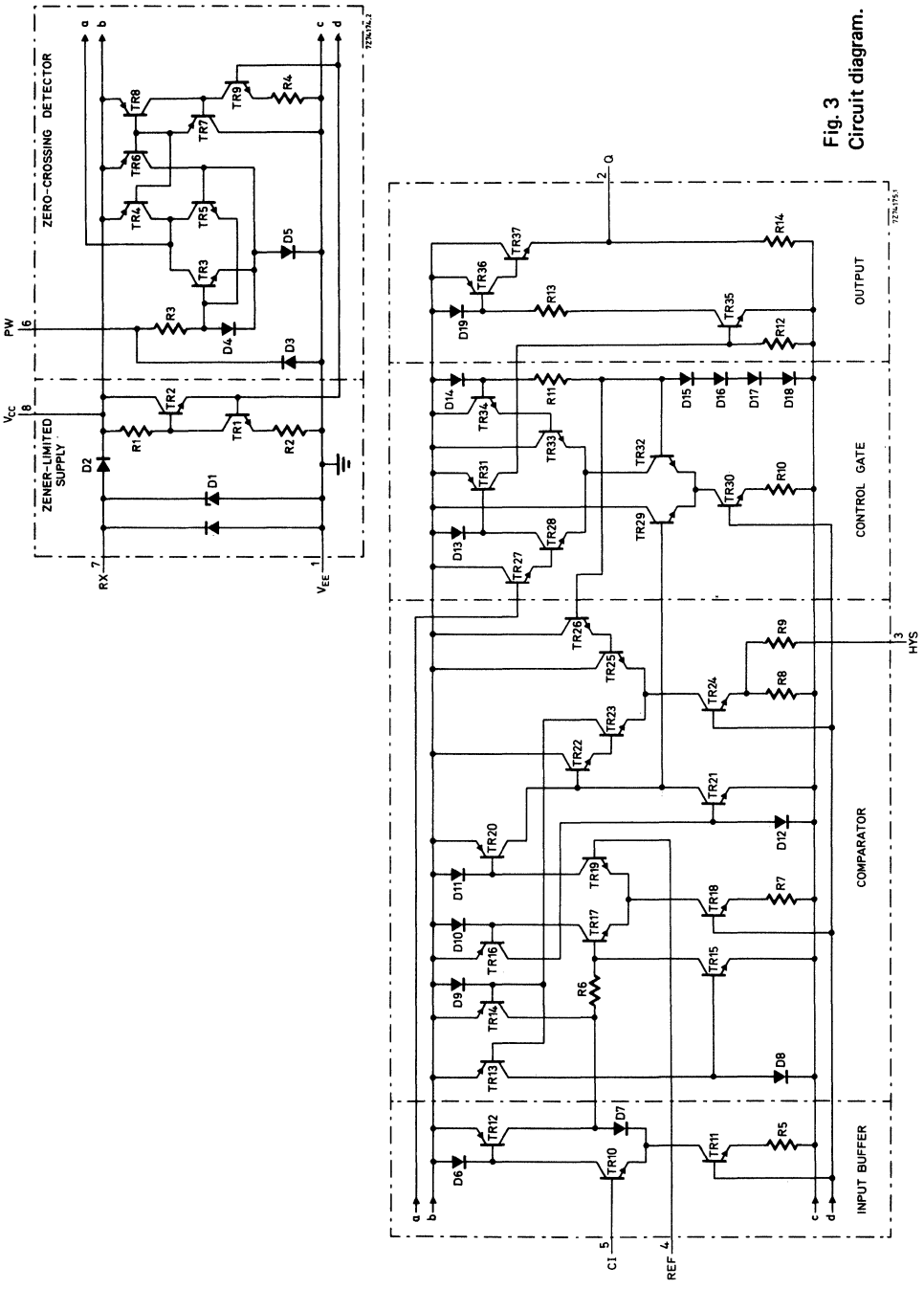

Fig. 3 Circuit diagram.

FUNCTIONAL DESCRIPTION

The TDA1024 generates positive-going output pulses to trigger a triac. These trigger pulses coincide with the zero crossings of the mains voltage. This minimizes r.f. interference and transients on the mains supply.

Supply: V_{CC} and RX (pins 8 and 7)

The TDA1024 may be supplied by an external d.c. power supply connected to V_{CC} (pin 8), but usually it is supplied directly from the mains voltage. For this purpose the circuit contains a stabilizer diode between RX and V_{EE} that limits the d.c. supply voltage (see Fig. 4). An external resistor R_D has to be connected from the mains to RX (pin 7); V_{EE} is connected to the neutral line (see Fig. 5a). A smoothing capacitor C_S has to be connected between V_{CC} and V_{EE}.

During the positive half of the mains cycles the current through external voltage-dropping resistor R_D charges the external smoothing capacitor C_S up to the stabilizing voltage of the internal stabilizer diodes. R_D should be chosen such that it can supply the current I_{CC} for the TDA1024 itself plus the average output current $-I_{Q(AV)}$, and recharge the smoothing capacitor C_S. Any excess current is bypassed by the internal stabilizer diode. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S supplies the circuit. Its capacitance must be high enough to maintain the supply voltage above 5 V, the minimum specified limit (see Fig. 10).

Dissipation in resistor R_D is halved by connecting a diode in series (see Figs 5b and 11).

A further reduction of dissipation is possible by using a high-quality voltage-dropping capacitor C_D in series with a resistor R_{SD} (see Figs 5c and 12).

A suitable VDR connected across the mains provides protection of the TDA1024 and of the triac against mains-borne transients.

Control and reference inputs CI and REF (pins 5 and 4)

The TDA1024 produces output pulses when the CI input is at a higher potential than the REF input. For power control as a function of temperature the inputs may be connected as shown in Fig. 14.

An input buffer circuit at the CI input gives a high input impedance and a low output impedance. This makes the hysteresis of the circuit independent of the input voltage.

Hysteresis control input HYS (pin 3)

With the hysteresis control input HYS open the device has a built-in hysteresis of 20 mV. For temperature control this corresponds with a temperature difference of 0.25 K.

Hysteresis is increased to 300 mV, corresponding with a temperature difference of 4 K, by grounding HYS. Intermediate values are obtained by connecting HYS to ground via a resistor.

Pulse width control input PW (pin 6)

The output pulse width may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor R_S between the pulse width control input PW and the a.c. mains. The pulse width is inversely proportional to the input current (see Fig. 13).

Output Q (pin 2)

Since the circuit has an open-emitter output, it is capable of sourcing current, i.e. supplying a current out of the output. Therefore it is especially suited for generating positive-going trigger pulses. The output is current-limited and protected against short-circuits. The maximum output current is 100 mA and the output pulses are stabilized at 4 V for output currents up to that value.

FUNCTIONAL DESCRIPTION (continued)

Output Q (pin 2) (continued)

A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figs 6 to 9). This minimizes the total supply current and the power dissipation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	8 V
Supply current			
average	$I_{RX(AV)}$	max.	30 mA
repetitive peak	$I_{RX(RM)}$	max.	80 mA
non-repetitive peak ($t < 50\ \mu s$)	$I_{RX(SM)}$	max.	2 A
Input voltage (all inputs)	V_I	max.	8 V
Input current (CI, REF, PW)	I_{CI}; I_{REF}; $\pm I_{PW}$	max.	10 mA
Output voltage HIGH	V_Q	max.	8 V
Output current			
average	$-I_{OH(AV)}$	max.	30 mA
peak, max. 300 μs	$-I_{OH(M)}$	max.	400 mA
Total power dissipation	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}		−55 to +125 °C
Operating ambient temperature range	T_{amb}		−20 to +80 °C

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CHARACTERISTICS

V_{CC} = 5 to 8 V; T_{amb} = −20 to +80 °C unless otherwise specified.

	symbol	min.	typ.	max.	unit
Supply: V_{CC} and RX (pins 8 and 7)					
Internally stabilized supply voltage at $I_{RX(AV)}$ = 10 mA	V_{CC}	5.5	6.5	7.5	V
variation with I_{RX}	$\Delta V_{CC}/\Delta I_{RX}$	–	15	–	mV/mA
Supply current at V_{CC} = 5.5 V; unloaded; f = 50 Hz; $V_{CI} > V_{REF}$ pin 3 open (minimum hysteresis)	$I_{RX(AV)}$	–	–	1.8	mA
Supply current increase pin 3 grounded (maximum hysteresis)	$\Delta I_{RX(AV)}$	–	1.4	–	mA
Control and reference inputs CI and REF (pins 5 and 4)					
Input current, CI input, at $V_{CI} > V_{REF}$	I_{CI}	–	–	5	μA
Input current, REF input, at $V_{REF} > V_{CI}$	I_{REF}	–	–	5	μA
Hysteresis control input HYS (pin 3)					
Hysteresis, pin 3 open (minimum hysteresis)	$\Delta V_{CI\text{-}REF}$	10	20	30	mV
pin 3 grounded (maximum hysteresis)	$\Delta V_{CI\text{-}REF}$	150	300	500	mV
Pulse width control input PW (pin 6)					
Pulse width at $I_{PW(RMS)}$ = 1 mA; V_{CC} = 5.5 V; f = 50 Hz	t_w	130	195	265	μs
Output Q (pin 2)					
Output voltage HIGH at $-I_{OH}$ = 100 mA	V_{OH}	4	–	–	V
at $-I_{OH}$ = 1 mA	V_{OH}	1	–	–	V
Output current HIGH	$-I_{OH}$	–	–	100	mA

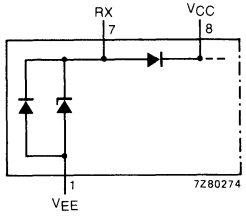
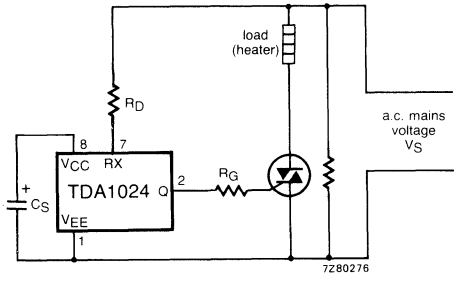
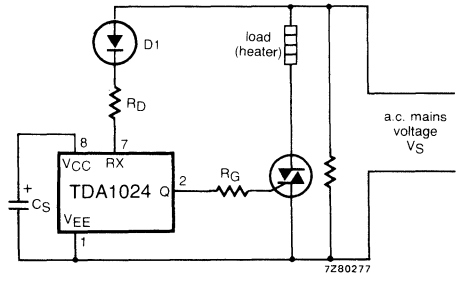


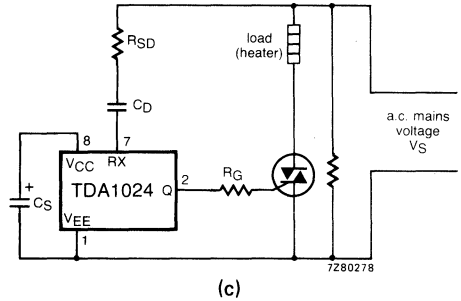
Fig. 4 Internal supply connections.



(a)



(b)



(c)

Fig. 5 Alternative supply arrangements.

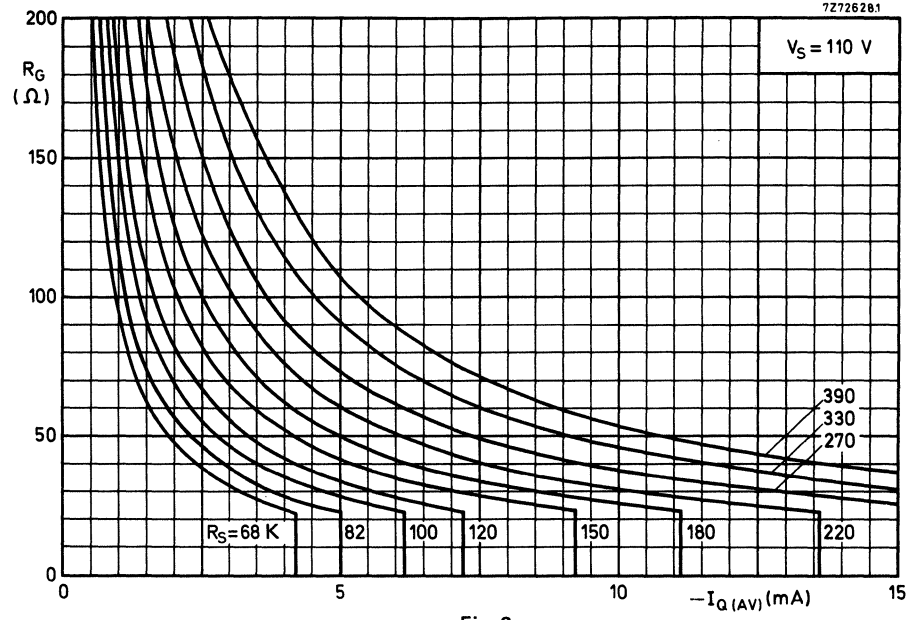

7Z72628.1
V_S = 110 V
R_G (Ω)
200
150
100
50
0
0
5
10
15
$-I_{Q(AV)}$ (mA)
R_S=68 K
82
100
120
150
180
220
390
330
270

Fig. 6.

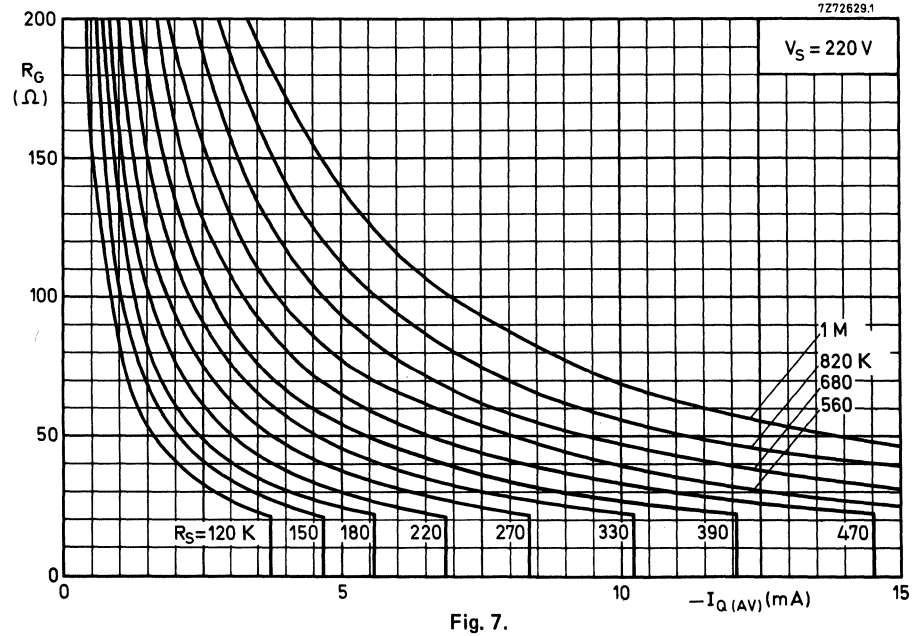

7Z72629.1
V_S = 220 V
R_G (Ω)
200
150
100
50
0
0
5
10
15
$-I_{Q(AV)}$ (mA)
R_S=120 K
150
180
220
270
330
390
470
1 M
820 K
680
560

Fig. 7.

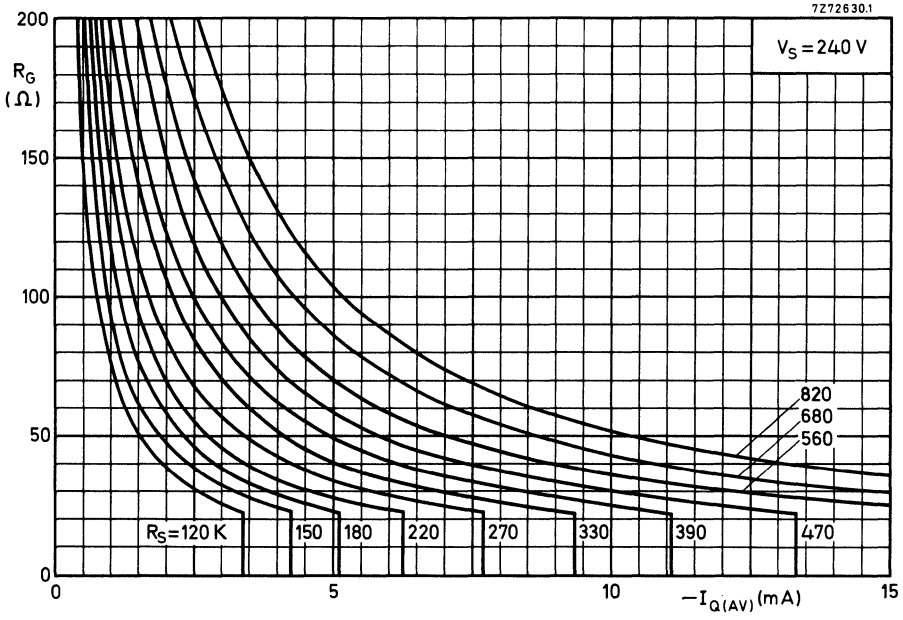

7Z72630.1
V_S = 240 V
R_G (Ω)
200
150
100
50
0
820
680
560
R_S = 120 K
150
180
220
270
330
390
470
0
5
10
15
$-I_{Q(AV)}$ (mA)

Fig. 8.

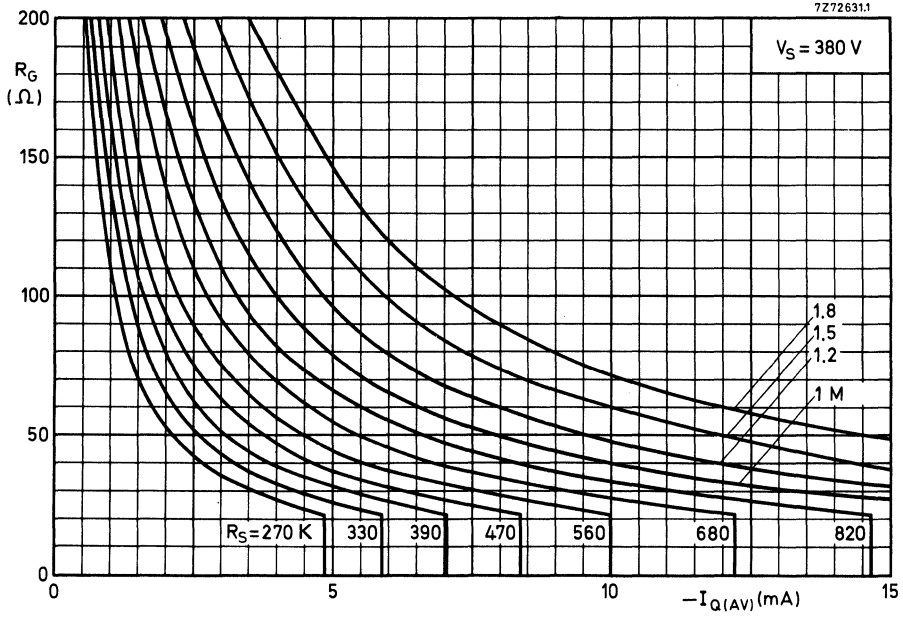

7Z72631.1
V_S = 380 V
R_G (Ω)
200
150
100
50
0
1.8
1.5
1.2
1 M
R_S = 270 K
330
390
470
560
680
820
0
5
10
15
$-I_{Q(AV)}$ (mA)

Fig. 9.

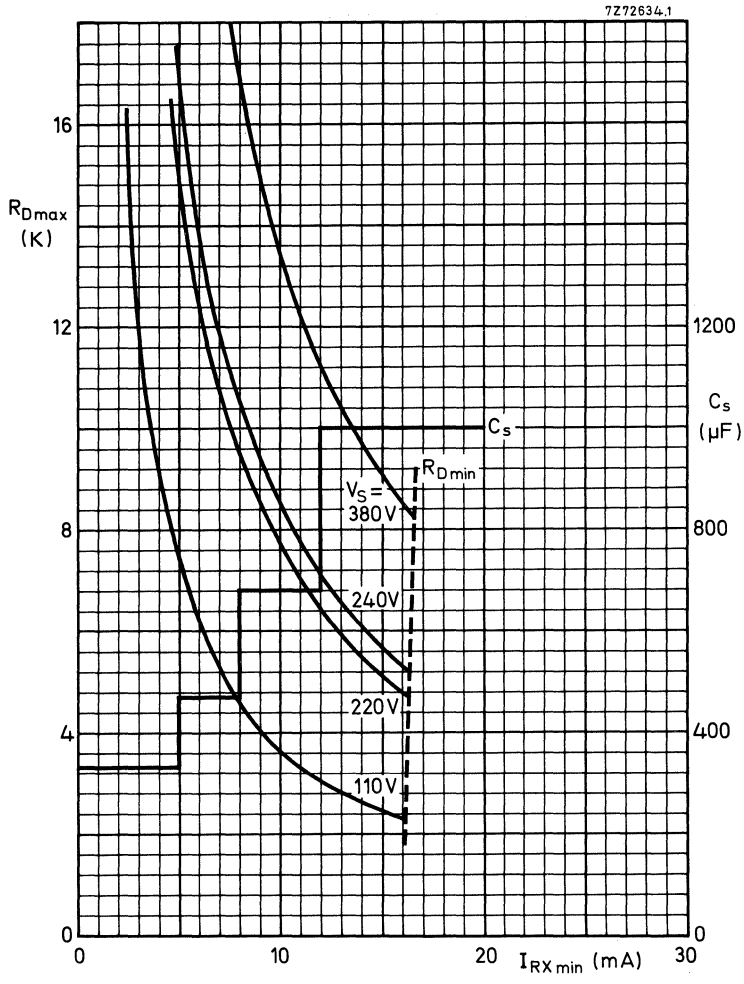


Fig. 10 Maximum value of voltage-dropping resistor R_D as a function of minimum value of the current into RX with the mains supply voltage V_S as a parameter for the supply arrangements of Figs 5a and 5b, and recommended value of smoothing capacitor C_S as a function of the current into RX for all three supply arrangements of Fig. 5. When V_{CC} is used to supply external circuitry such as a temperature-sensing bridge, the current required by that external circuitry should be added to I_{RXmin}.

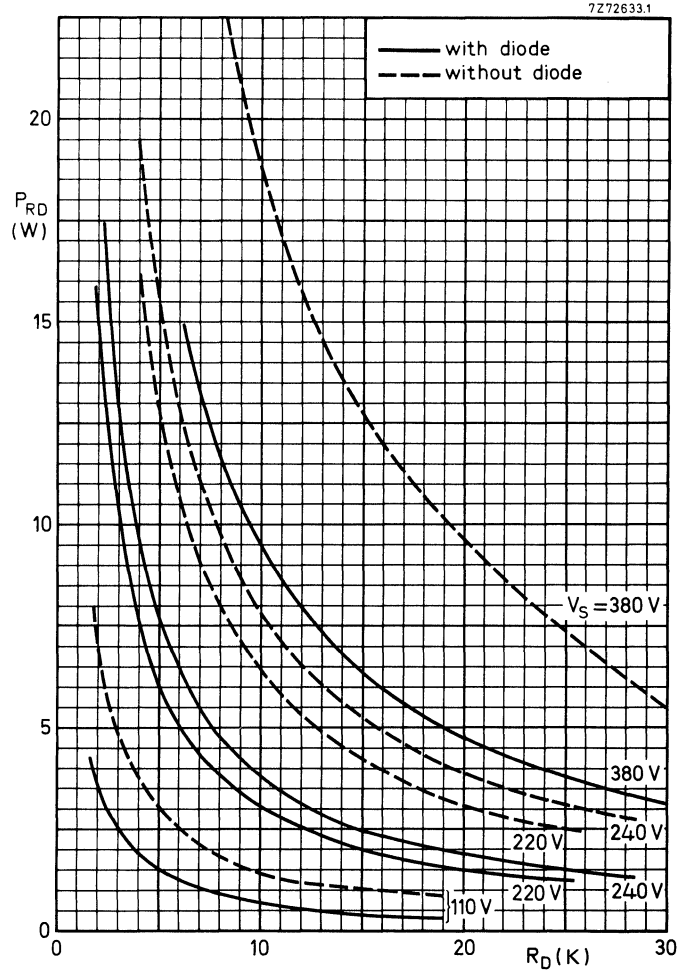


Fig. 11 Power dissipated in voltage-dropping resistor R_D as a function of its value with the mains supply voltage V_S as a parameter, for the supply arrangements of Figs 5a and 5b.

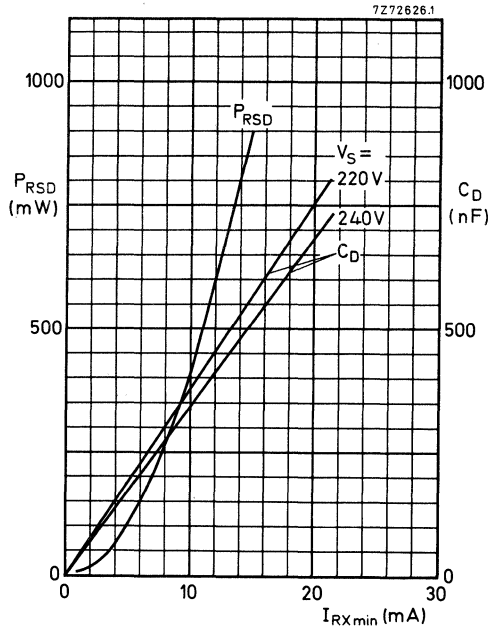


Fig. 12 Power dissipated in voltage-dropping resistor R_{SD} and dropping capacitor C_D as a function of the minimum current into RX with the mains supply voltage V_S as a parameter, for the supply arrangement of Fig. 5c. When V_{CC} is used to supply external circuitry such as a temperature-sensing bridge, the current required by that external circuitry should be added to I_{RXmin}.

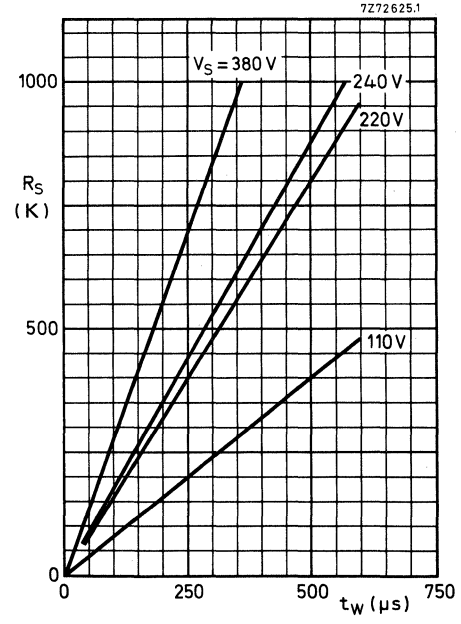


Fig. 13 Synchronization resistor R_S as a function of required trigger pulse width t_W with mains supply voltage V_S as a parameter.

APPLICATION INFORMATION

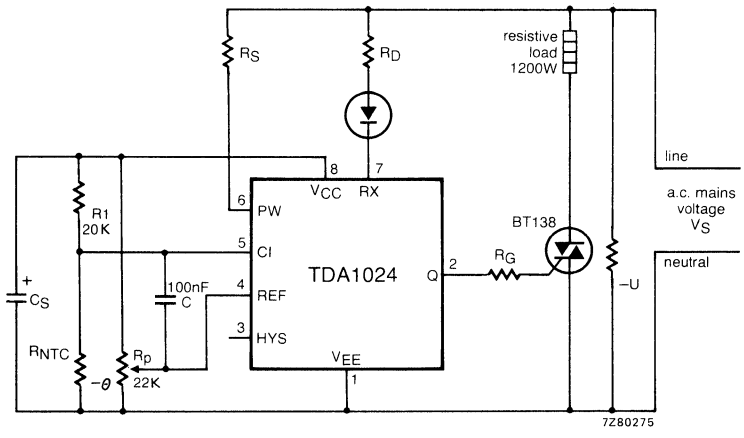


Fig. 14 Typical application of the TDA1024 in a 1200 W thermostat covering the temperature range 5 to 30 °C. For component values see Table 1.

Conditions

Mains supply voltage $V_{S(RMS)}$ = 220 V

Temperature range: 5 to 30 °C

BT138 data: $V_{GT} < 1.5$ V, $I_{GT} > 70$ mA, $I_L < 60$ mA } at T_j = 25 °C

7

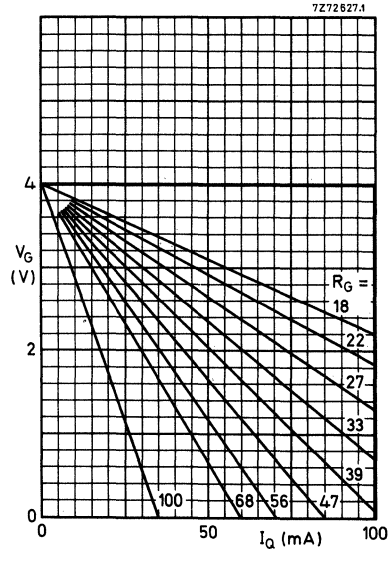
Table 1

Temperature controller component values (see Fig. 14)

parameter	symbol	value	remarks
Trigger pulse width	t_W	105 μs	see BT138 data sheet
Synchronization resistor	R_S	180 kΩ	see Fig. 13
Gate resistor	R_G	33 Ω	see Fig. 7
Average output current	$I_{Q(AV)}$	3.7 mA	
Min. required supply current	$I_{RX(AV)}$	6.5 mA	
Voltage-dropping resistor	R_D	10 kΩ	see Fig. 10
Power dissipated in R_D	P_{RD}	3.2 W	see Fig. 11
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 593 62512
Rectifier diode	D1	BYW56	
NTC thermistor (at 25 °C)	R_{NTC}	22 kΩ	B = 4200 K cat. no. 2322 642 12223
Smoothing capacitor	C_S	220 μF; 16 V	

If R_D and D1 are replaced by C_D and R_{SD}

Voltage-dropping capacitor	C_D	270 nF	
Series dropping resistor	R_{SD}	390 Ω	
Power dissipated in R_{SD}	P_{RSD}	190 mW	
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 594 62512



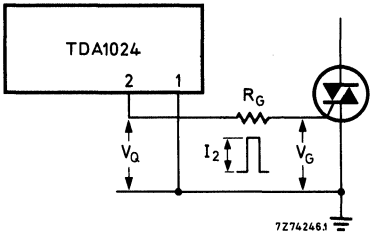


Fig. 15 Gate voltage (V_G) as a function of trigger current (I_Q) with gate resistor (R_G) load lines.

Touch Dimmer Circuit | TEA1010, T

GENERAL DESCRIPTION

The TEA1010 is a bipolar integrated circuit for switching and regulating lamps and other loads with a minimum of external components. It provides ON/OFF switching and a physiological power regulation (equal brightness steps). It is suited for touch plates and for switches, and may combine local and remote control. It produces negative pulses to drive a triac. The circuit is suited for resistive and for inductive loads, i.e. it is not only suited for dimming lamps but also for regulating motors in fans, vacuum cleaners, etc.

The TEA 1010 and TEA1010T switch on at the maximum brightness level upon a brief touch of the contacts.

The circuits feature:
- Alternative ON/OFF switching by a brief touch of one or both contacts.
- ON switching at minimum brightness by a long touch of one or both contacts.
- Gradual change to maximum brightness during a long touch of the UP contact.
- Gradual change to minimum brightness during a long touch of the DOWN contact.
- No action during a long touch of both contacts in the ON state.

QUICK REFERENCE DATA

Supply voltage, d.c. (derived from mains voltage)	V_{CC}	typ.	15 V
Supply current	I_{CC}	typ.	1 mA
Output current	I_O	max.	100 mA
Firing phase range	φ	typ.	30° to 140°
Time to change from minimum to maximum brightness, or vice versa	t_v	typ.	3,8 s
Power dissipation in the ON state	P	typ.	19 mW
Operating ambient temperature range	T_{amb}		0 to + 85 °C

7

PACKAGE OUTLINE

TEA1010 : 8-lead DIL; plastic (SOT-97C2).
TEA1010T: 8-lead mini-pack; plastic (SO-8; SOT-96AC1).

FUNCTIONAL DESCRIPTION

The TEA1010 generates negative output pulses to trigger a triac. These output pulses are phase shifted with respect to the mains voltage. The amount of phase shift is determined by the difference between the initial states of two 7-bit counters. Both counters are driven by the same clock pulse generator. One of the counters is preset to a number determined by the required phase angle. The higher the required brightness, the smaller the required phase angle, the lower the number to which the counter is preset. The relation between brightness and preset number has been chosen so that almost equal brightness steps are obtained (physiological control). The minimum phase shift corresponds with 32 clock pulses and the maximum with 160.

Upwards and downwards regulation inputs UP and DN (pins 7 and 6)

At 50 Hz mains frequency the device ignores signals with a duration of less than 80 ms and signals with a duration of 80 to 320 ms are accepted as brief commands, these cause the circuit to switch on and off alternatively. Signals that last longer than 320 ms are interpreted as long commands. A long command via the UP input causes the output phase angle to decrease, i.e. the brightness to increase gradually; a long command via the DN input has the opposite effect. A long signal on both inputs will switch on the lamp at minimum brightness. If the lamp is already on, a long signal on both inputs will have no effect.

The UP and DN inputs may be activated by touch plates or by switches. For the input arrangements see Fig. 2.

Slave input SLV (pin 2)

The SLV input operates in the same manner as the UP and DN inputs, but with a two-wire connection, ideal for remote control. The SLV input is only suited for switches. For the arrangement see Fig. 3. If the SLV input is not used it must be connected to the load via a 1,5 MΩ resistor (see Fig. 4).

Oscillator RC pin OSC (pin 1)

The frequency of the clock pulse generator is determined by an external resistor and capacitor, both connected to the OSC terminal (see Fig. 4). The generator switches at levels equal to 1/6 and 1/2 of the difference between the injector voltage V_{inj} and the supply voltage V_{CC}. The clock pulse period is about 50 μs.

Output Q (pin 3)

Since the circuit has an open-collector output, it is capable of sinking current, i.e. drawing a current into the output. Therefore it is especially suitable for delivering negative trigger pulses.

The maximum output current is 100 mA. A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Fig. 4). This minimizes the total supply current and the power dissipation.

A negative-going trigger pulse is generated at the output after every zero crossing of the mains voltage. The output pulse has a maximum duration of one clock pulse period, i.e. 50 μs. To reduce the power dissipation the output pulse is terminated as soon as the triac has switched on.

Supply V_{CC} and V_{EE} (pins 8 and 4)

The TEA1010 is supplied from the a.c. mains via a capacitor C_D and a diode to V_{EE}; V_{CC} is connected to the line (see Fig. 4). A smoothing capacitor C_S has to be connected between V_{CC} and V_{EE}. The circuit contains a string of stabilizer diodes between V_{CC} and V_{EE} that limit the d.c. supply voltage.

During the positive half of the mains cycles the current through external voltage dropping capacitor C_D charges the external smoothing capacitor C_S up to the stabilizing voltage of the internal stabilizer diodes. C_D should be chosen such that it can supply the current I_{CC} for the TEA1010 itself plus the average output current $I_{3(AV)}$, and recharge the smoothing capacitor C_S.

Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S supplies the circuit. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit.

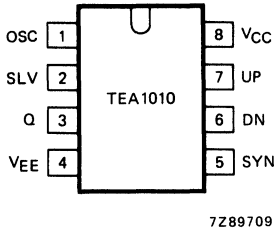
A supply voltage at V_{EE} that is negative with respect to V_{CC} and the line is developed at the V_{EE} pin. Note that in the characteristics the voltages are mainly measured with respect to V_{EE} and not with respect to V_{CC} and the line.

The circuit has an internal power-on reset, which forces the circuit into the OFF state.

Synchronization input SYN (pin 5)

The connection to the SYN input should be short and must be decoupled via a capacitor to V_{CC} (pin 8).

PINNING



1	OSC	oscillator (RC)
2	SLV	slave input
3	Q	output
4	V_{EE}	common
5	SYN	synchronization input
6	DN	downward regulation input
7	UP	upward regulation input
8	V_{CC}	positive supply

Fig. 1 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, d.c.	V_{CC}	−0,5 to + 18	V
Supply current, d.c.	I_{CC}	max. 20	mA
peak, max. 10 μs	I_{CCM}	max. 0,5	A
Input voltage range, all inputs	V_I	−0,5 to + 18	V
Input current, all inputs	$\pm I_I$	max. 20	mA
Output voltage range	V_O	−0,5 to + 18	V
Output current range	I_O	−20 to + 150	mA
Power dissipation	P_{tot}	max. 250	mW
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 85	°C

CHARACTERISTICS

V_{CC} = 5 to 18 V; T_{amb} = 0 to + 85 °C

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 8)					
Internally stabilized supply voltage, at I_{CC} = 1,5 to 20 mA	V_{CC}	13,3	15	16,8	V
Supply current at V_{CC} = 15 V, unloaded, OFF state	I_{CC}	–	1	1,2	mA
ON state	I_{CC}	–	1,25	1,5	mA
Power dissipation, unloaded, OFF state	P	–	15	–	mW
ON state	P	–	19	25	mW
Thermal resistance TEA1010	$R_{th\ j\text{-}a}$	–	162	–	K/W
TEA1010T (note 1)	$R_{th\ j\text{-}a}$	–	140	–	K/W
TEA1010T (note 2)	$R_{th\ j\text{-}a}$	–	220	–	K/W
Power-on reset threshold voltage	V_{CCpor}	–	–	4,8	V
Oscillator RC pin OSC (pin 1)					
Injector voltage	V_{inj}	550	–	700	mV
Synchronization input SYN (pin 5)					
Input current (r.m.s. value)	$I_{5(rms)}$	3	–	–	μA
Upwards and downwards regulation inputs UP and DN (pins 7 and 6)					
Input voltage	$V_{6\text{-}4}$; $V_{7\text{-}4}$	1	–	–	V
Input current	$-I_6$; $-I_7$	–	3 $I_{5(rms)}$	–	μA
Slave input SLV (pin 2)					
Input current	$\pm I_2$	10	–	–	μA
Output Q (pin 3)					
Output current	I_3	–	–	100	mA

Notes

1. TEA1010T mounted on a ceramic substrate of 50 x 50 x 0,7 mm.
2. TEA1010T mounted on a printed-circuit board of 50 x 50 x 1,5 mm.

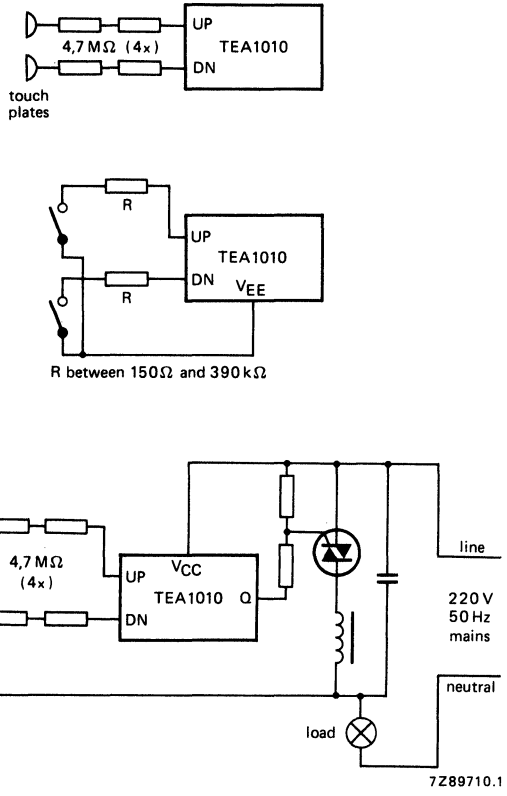


Fig. 2 Alternative arrangements for the UP and DN inputs.

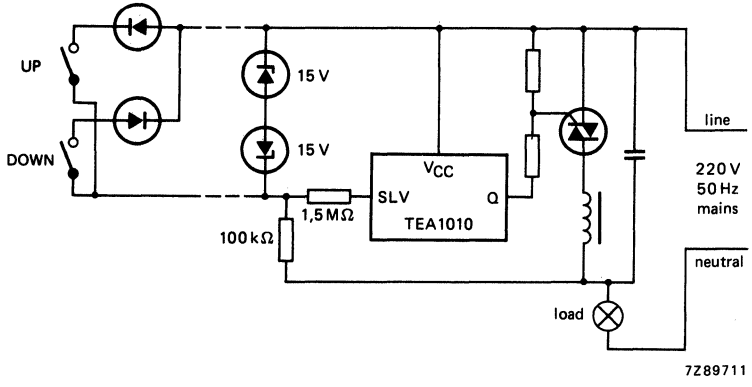


Fig. 3 SLV input arrangement.

Touch Controlled Lamp Dimmer with Memory TEA1058, T

GENERAL DESCRIPTION

The TEA1058 is a bipolar integrated circuit for switching and regulating lamps and other loads with a minimum of external components. It provides ON/OFF switching and a physiological power regulation (equal brightness steps). It is suited for touch plates and for switches, and may combine local and remote control. It produces negative pulses to drive a triac. The circuit is suited for resistive and for inductive loads, i.e. it is not only suited for dimming lamps but also for regulating motors in fans, vacuum cleaners, etc.

The TEA1058 and TEA1058T switch on at the level at which they were switched off.

The circuits feature:
- Alternative ON/OFF switching by a brief touch of one or both contacts.
- ON switching at previous brightness by a long touch of one or both contacts.
- Gradual change to maximum brightness during a long touch of the UP contact.
- Gradual change to minimum brightness during a long touch of the DOWN contact.
- No action during a long touch of both contacts in the ON state.

QUICK REFERENCE DATA

Supply voltage, d.c. (derived from mains voltage)	V_{CC}	typ.	15 V
Supply current	I_{CC}	typ.	1 mA
Output current	I_O	max.	100 mA
Firing phase range	φ	typ.	30° to 140°
Time to change from minimum to maximum brightness, or vice versa	t_v	typ.	3,8 s
Power dissipation in the ON state	P	typ.	19 mW
Operating ambient temperature range	T_{amb}		0 to + 85 °C

PACKAGE OUTLINE

TEA1058 : 8-lead DIL; plastic (SOT-97C2).
TEA1058T: 8-lead mini-pack; plastic (SO-8; SOT-96AC1).

FUNCTIONAL DESCRIPTION

The TEA1058 generates negative output pulses to trigger a triac. These output pulses are phase shifted with respect to the mains voltage. The amount of phase shift is determined by the difference between the initial states of two 7-bit counters. Both counters are driven by the same clock pulse generator. One of the counters is preset to a number determined by the required phase angle. The higher the required brightness, the smaller the required phase angle, the lower the number to which the counter is preset. The relation between brightness and preset number has been chosen so that almost equal brightness steps are obtained (physiological control). The minimum phase shift corresponds with 32 clock pulses and the maximum with 160.

Upwards and downwards regulation inputs UP and DN (pins 7 and 6)

At 50 Hz mains frequency the device ignores signals with a duration of less than 80 ms and signals with a duration of 80 to 320 ms are accepted as brief commands, these cause the circuit to switch on and off alternatively. Signals that last longer than 320 ms are interpreted as long commands. A long command via the UP input causes the output phase angle to decrease, i.e. the brightness to increase gradually; a long command via the DN input has the opposite effect. A long signal on both inputs will switch on the lamp at previous brightness. If the lamp is already on, a long signal on both inputs will have no effect.

The UP and DN inputs may be activated by touch plates or by switches. For the input arrangements see Fig. 2.

Slave input SLV (pin 2)

The SLV input operates in the same manner as the UP and DN inputs, but with a two-wire connection, ideal for remote control. The SLV input is only suited for switches. For the arrangement see Fig. 3. If the SLV input is not used it must be connected to the load via a 1,5 MΩ resistor (see Fig. 4).

Oscillator RC pin OSC (pin 1)

The frequency of the clock pulse generator is determined by an external resistor and capacitor, both connected to the OSC terminal (see Fig. 4). The generator switches at levels equal to 1/6 and 1/2 of the difference between the injector voltage V_{inj} and the supply voltage V_{CC}. The clock pulse period is about 50 μs.

Output Q (pin 3)

Since the circuit has an open-collector output, it is capable of sinking current, i.e. drawing a current into the output. Therefore it is especially suitable for delivering negative trigger pulses.

The maximum output current is 100 mA. A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Fig. 4). This minimizes the total supply current and the power dissipation.

A negative-going trigger pulse is generated at the output after every zero crossing of the mains voltage. The output pulse has a maximum duration of one clock pulse period, i.e. 50 μs. To reduce the power dissipation the output pulse is terminated as soon as the triac has switched on.

Supply V_{CC} and V_{EE} (pins 8 and 4)

The TEA1058 is supplied from the a.c. mains via a capacitor C_D and a diode to V_{EE}; V_{CC} is connected to the line (see Fig. 4). A smoothing capacitor C_S has to be connected between V_{CC} and V_{EE}. The circuit contains a string of stabilizer diodes between V_{CC} and V_{EE} that limit the d.c. supply voltage. During the positive half of the mains cycles the current through external voltage dropping capacitor C_D charges the external smoothing capacitor C_S up to the stabilizing voltage of the internal stabilizer diodes. C_D should be chosen such that it can supply the current I_{CC} for the TEA1058 itself plus the average output current $I_{3(AV)}$, and recharge the smoothing capacitor C_S.

Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S supplies the circuit. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit.

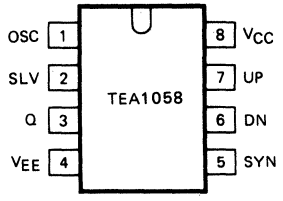
A supply voltage at V_{EE} that is negative with respect to V_{CC} and the line is developed at the V_{EE} pin. Note that in the characteristics the voltages are mainly measured with respect to V_{EE} and not with respect to V_{CC} and the line.

The circuit has an internal power-on reset, which resets the brightness to minimum and forces the circuit into the OFF state.

Synchronization input SYN (pin 5)

The connection to the SYN input should be short and must be decoupled via a capacitor to V_{CC} (pin 8).

PINNING



1	OSC	oscillator (RC)
2	SLV	slave input
3	Q	output
4	V_{EE}	common
5	SYN	synchronization input
6	DN	downward regulation input
7	UP	upward regulation input
8	V_{CC}	positive supply

Fig. 1 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, d.c.	V_{CC}	−0,5 to + 18	V
Supply current, d.c.	I_{CC}	max. 20	mA
peak, max. 10 μs	I_{CCM}	max. 0,5	A
Input voltage range, all inputs	V_I	−0,5 to + 18	V
Input current, all inputs	$\pm I_I$	max. 20	mA
Output voltage range	V_O	−0,5 to + 18	V
Output current range	I_O	−20 to + 150	mA
Power dissipation	P_{tot}	max. 250	mW
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	0 to + 85	°C

CHARACTERISTICS

V_{CC} = 5 to 18 V; T_{amb} = 0 to + 85 °C

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 8)					
Internally stabilized supply voltage, at I_{CC} = 1,5 to 20 mA	V_{CC}	13,3	15	16,8	V
Supply current at V_{CC} = 15 V, unloaded,					
OFF state	I_{CC}	–	1	1,2	mA
ON state	I_{CC}	–	1,25	1,5	mA
Power dissipation, unloaded,					
OFF state	P	–	15	–	mW
ON state	P	–	19	25	mW
Thermal resistance					
TEA1058	$R_{th\ j\text{-}a}$	–	162	–	K/W
TEA1058T (note 1)	$R_{th\ j\text{-}a}$	–	140	–	K/W
TEA1058T (note 2)	$R_{th\ j\text{-}a}$	–	220	–	K/W
Power-on reset threshold voltage	V_{CCpor}	–	–	4,8	V
Oscillator RC pin OSC (pin 1)					
Injector voltage	V_{inj}	550	–	700	mV
Synchronization input SYN (pin 5)					
Input current (r.m.s. value)	$I_{5(rms)}$	3	–	–	μA
Upwards and downwards regulation inputs UP and DN (pins 7 and 6)					
Input voltage	$V_{6\text{-}4}$; $V_{7\text{-}4}$	1	–	–	V
Input current	$-I_6$; $-I_7$	–	3 $I_{5(rms)}$	–	μA
Slave input SLV (pin 2)					
Input current	$\pm I_2$	10	–	–	μA
Output Q (pin 3)					
Output current	I_3	–	–	100	mA

Notes

1. TEA1058T mounted on a ceramic substrate of 50 x 50 x 0,7 mm.
2. TEA1058T mounted on a printed-circuit board of 50 x 50 x 1,5 mm.

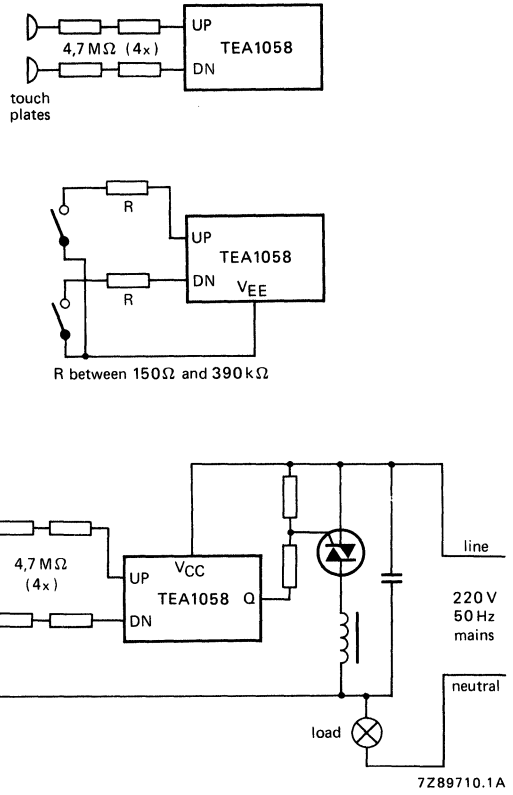


Fig. 2 Alternative arrangements for the UP and DN inputs.

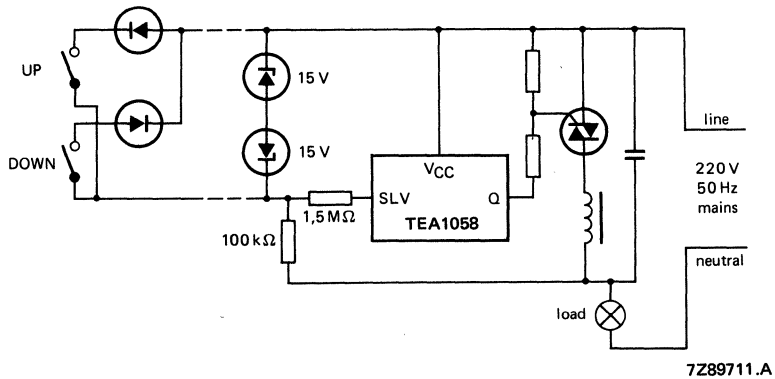
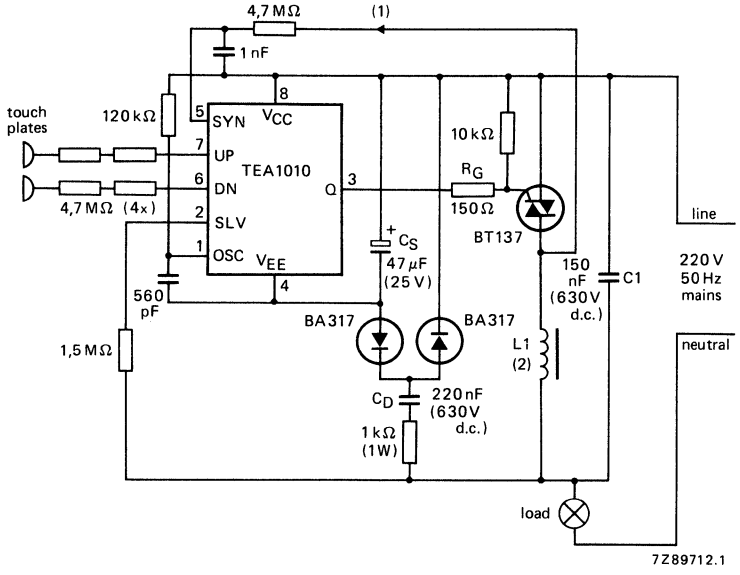


Fig. 3 SLV input arrangement.

APPLICATION INFORMATION



(1) The connection to the SYN input should be short and must be decoupled near to pins 5 and 8.
(2) For example, Vakuumschmelze FD 2.5 1N1 KN.

Fig. 4 Touch-controlled lamp dimmer circuit for max. 450 W. L1 and C1 form a radio-frequency interference filter with a quality factor Q of less than 1. This filter is necessary to satisfy the regulations of C.I.S.P.R. and V.D.E.

7

Signetics

Video
Section 8

Linear Products

Section 8 Video

Explanation Of Terms

Anti-Top Flutter Pulse: Disables the phase detector during equalization and framing times.

Black Current Stabilizer: Is an adjustment on each gun (R,G,B) for setting the leakage current when the gun is in the off condition. If this is not adjusted, you will get background discoloring. The leakage is measured via sensing resistors.

Black Level Noise: Is very similar to a white spot noise spike except it is in the opposite, or black level, direction.

Breakthroughs: Are unwanted signals present at the output.

CVS: Composite Video Signal. The signal carrying information for brightness (black & white), color, and synchronization of scan.

Hue: Tint, or color-yellow, blue, violet, orange.

NTSC: National Television Standards Committee. This group defines T.V. technical standards of broadcasting. (U.S.A. system).

PAL: Phase Alternate Line. The primary T.V. system used in Europe.

Peaking: Is a technique whereby a little overshoot is induced on a waveform (usually a pulsed wave) for the purpose of realizing better definition, or sharpness, in a picture.

Pulling: Is caused by part of the signal from the R.F. input affecting the horizontal oscillator. The top of the picture "pulls" to one side.

RGB: Three signals, Red, Green, and Blue (with luminance information), that are sent to a color CRT to produce the color image.

R-Y, B-Y, G-Y Red (R), blue (B), or green (G) color saturation signal without the luminance (-Y) signal.

Sandcastle Pulse: Is used to synchronize the burst keying signal, the horizontal flyback pulse, and the vertical flyback pulse. This is a waveform generated internally by the sync processor and then output to the color decoder.

Y Signal Luminance signal or brightness signal that determines the brightness of each spot on the face of the picture tube of monochrome receivers. It is a D.C. level.

256 x 8 Static RAM | PCF8570/70A

GENERAL DESCRIPTION

The PCF8570 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.
In the PCF8570A the hardware address pin A0 is don't care.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder
- General purpose — RAM expansion for the microcomputer families MAB8400 and PCF84C00

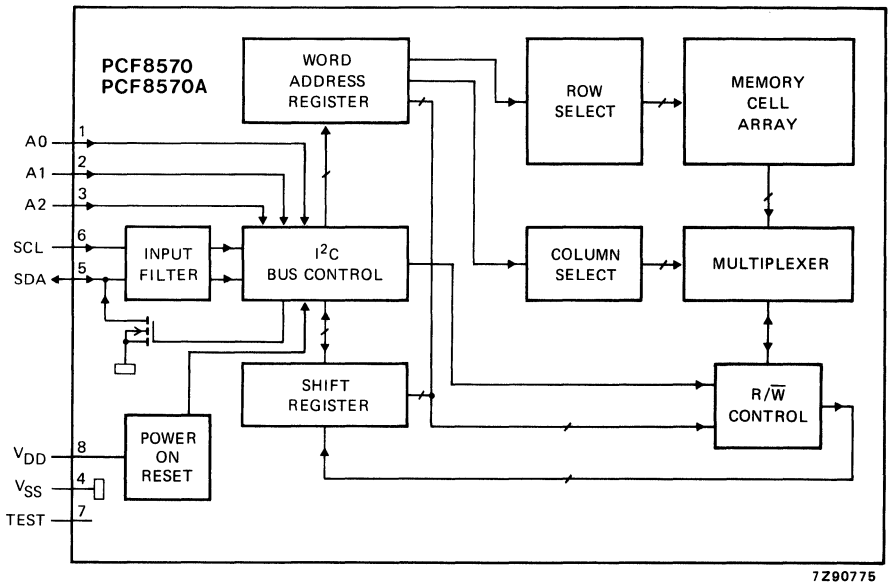


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF8570P: 8-lead DIL; plastic (SOT-97A).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line } I^2C bus
6	SCL	serial clock line } I^2C bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 14 and 15)
8	V_{DD}	positive supply

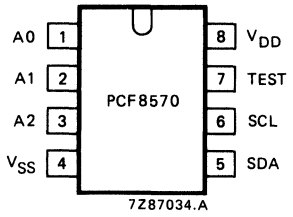


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}	−0,8 to + 8,0	V
Voltage range on any input	V_I	−0,8 to V_{DD} + 0,8	V
D.C. input current (any input)	$\pm I_I$	max. 10	mA
D.C. output current (any output)	$\pm I_O$	max. 10	mA
Supply current (pin 4 or pin 8)	$\pm I_{DD}; I_{SS}$	max. 50	mA
Power dissipation per package	P_{tot}	max. 300	mW
Power dissipation per output	P	max. 50	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at f_{SCL} = 100 kHz; $V_I = V_{SS}$ or V_{DD}					
operating	I_{DD}	–	–	200	μA
standby	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Input SCL; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current (A0, A1, A2) at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Figs 14 and 15)					
Supply current at T_{amb} = 25 °C; TEST = V_{DDR}	I_{DDR}	–	50	400	nA

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.

8

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

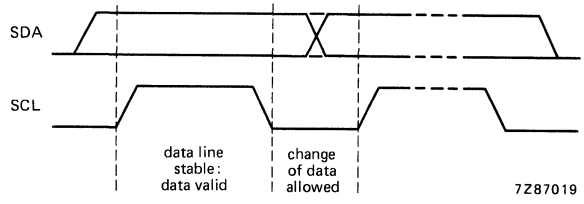


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

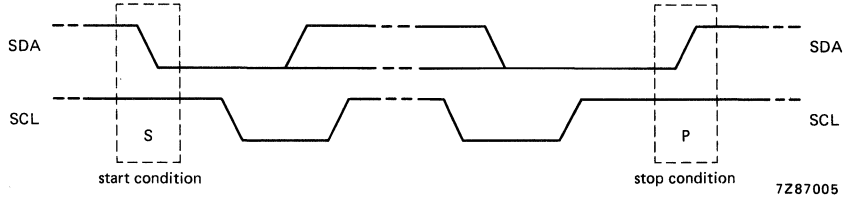


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

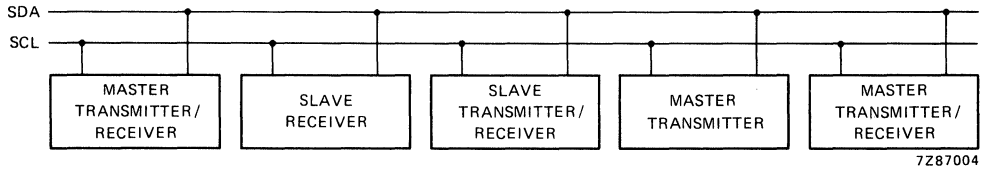


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

8

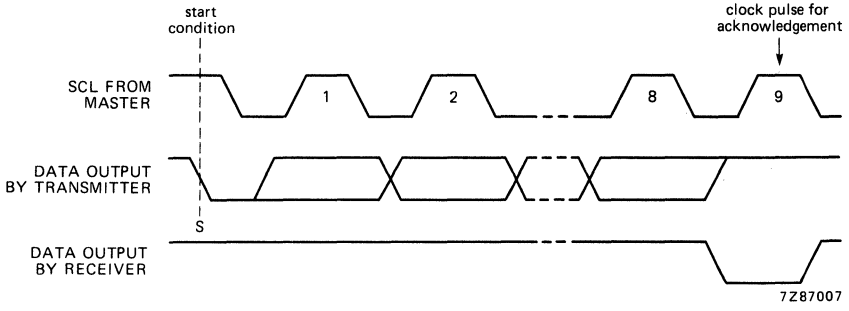


Fig. 6 Acknowledgement on the I^2C bus.

Timing specifications

Within the I^2C bus specifications a high-speed mode and a low-speed mode are defined. The device operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

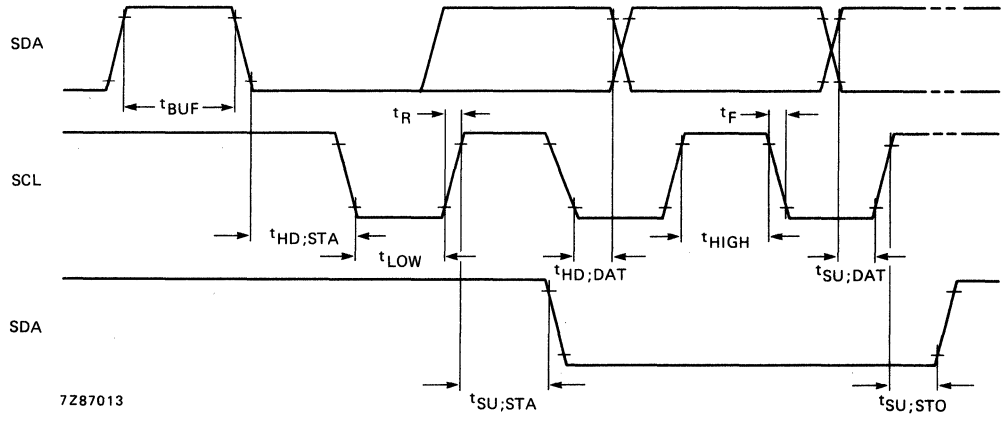


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

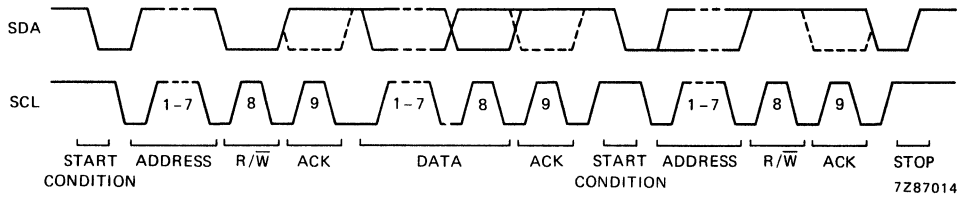


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

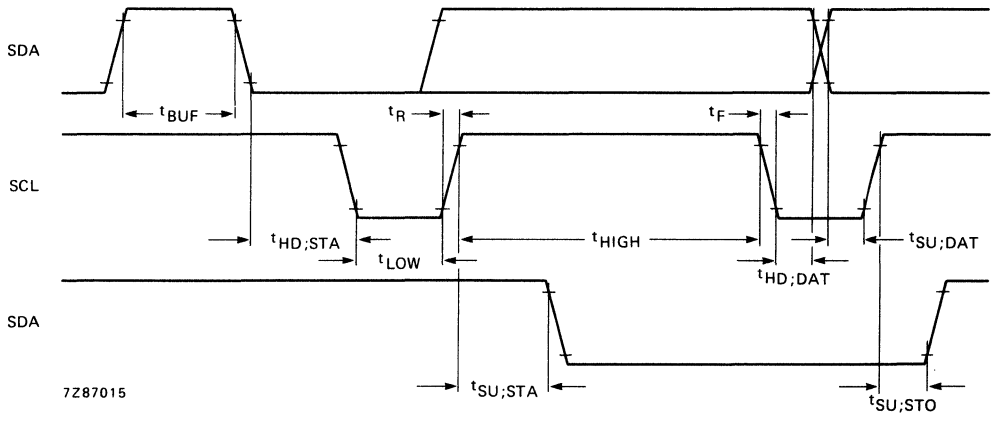


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

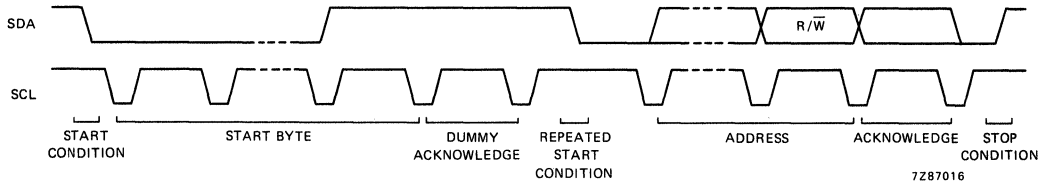


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570 READ and WRITE cycles is shown in Fig. 11.

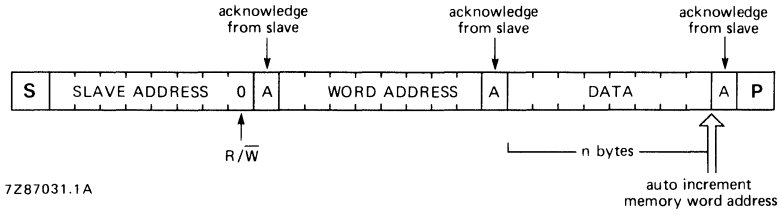


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

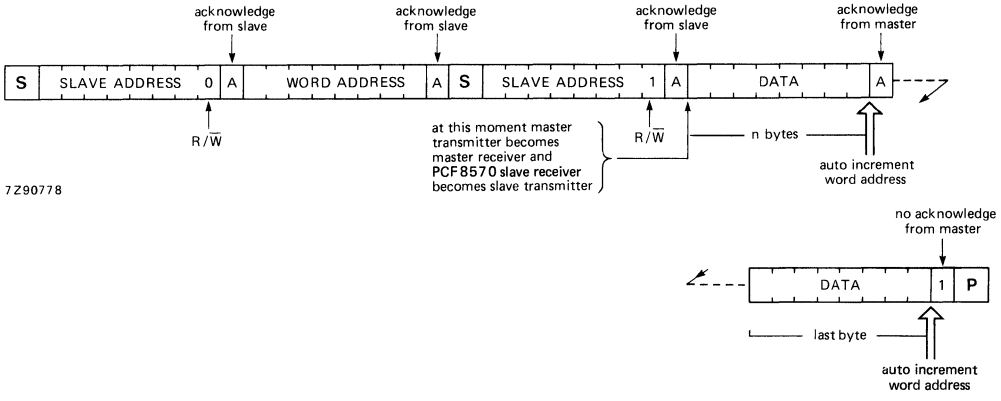


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

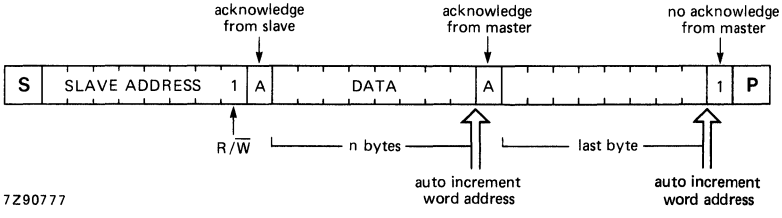


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

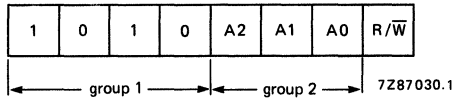


Fig. 12 PCF8570 address.

Note

PCF8570A version: the slave address A0 state is X (don't care), however, the hardware address A0 input must still be connected to V_{SS} or V_{DD}.

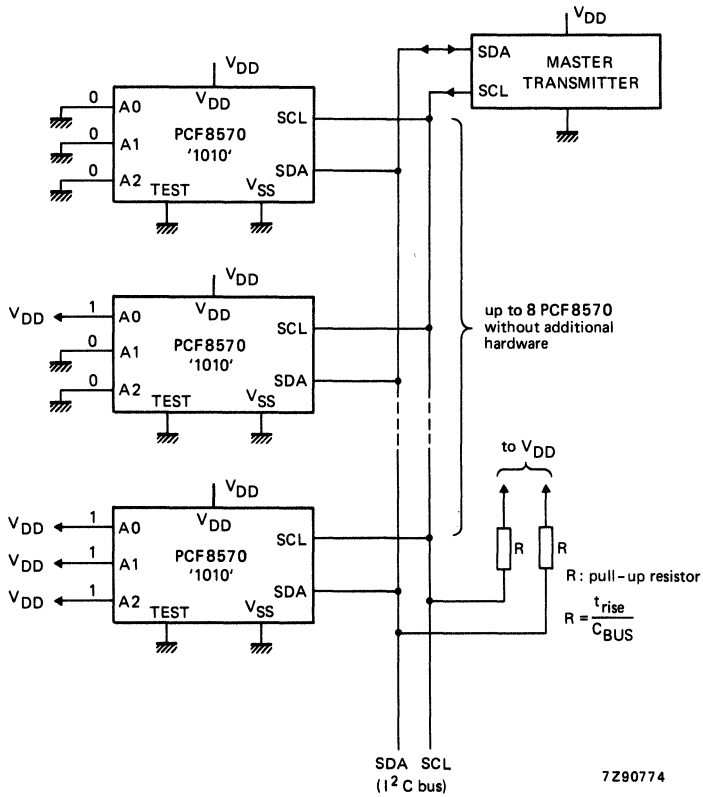


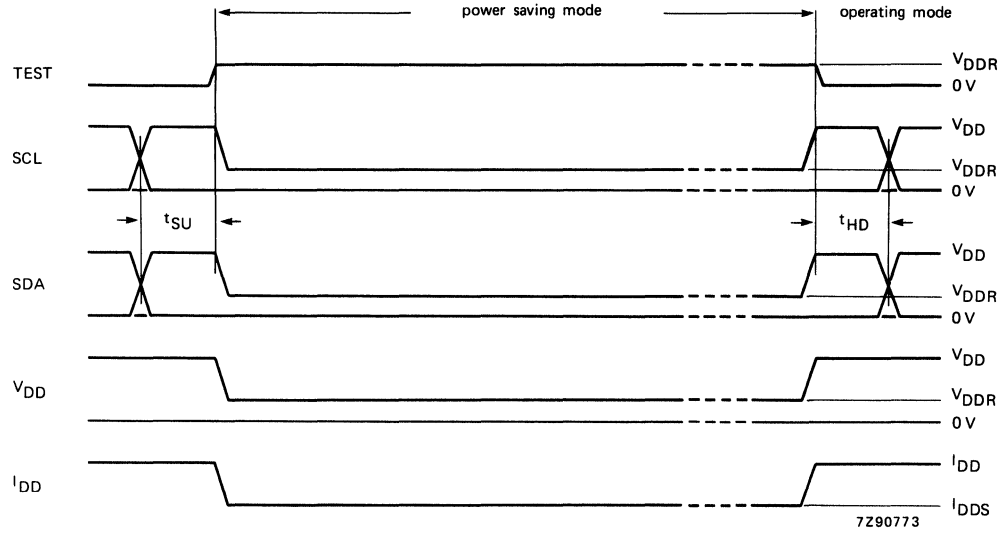
Fig. 13 PCF8570 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition TEST = V_{DDR}, the PCF8570 goes into the power saving mode.



Where:
$t_{SU} \geqslant 4\ \mu s$
$t_{HD} \geqslant 4\ \mu s$

Fig. 14 Timing for power saving mode.

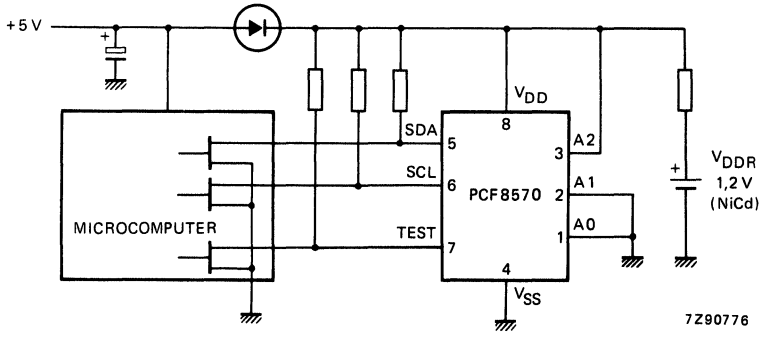


Fig. 15 Application example for power saving mode.

Note to Fig. 15

1. In the operating mode, TEST = 0.
2. In the power saving mode, TEST = V_{DDR}.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specification defined by Philips.

GENERAL DESCRIPTION

The PCD8571 is a low power 1024-bit static CMOS RAM organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1, A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 5 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony
- Radio and television
- Video cassette recorder

RAM expansion for stored numbers in repertory dialling (e.g. PCD3340 applications) channel presets

- General purpose

RAM expansion for the microcomputer families MAB8400 and PCF84C00

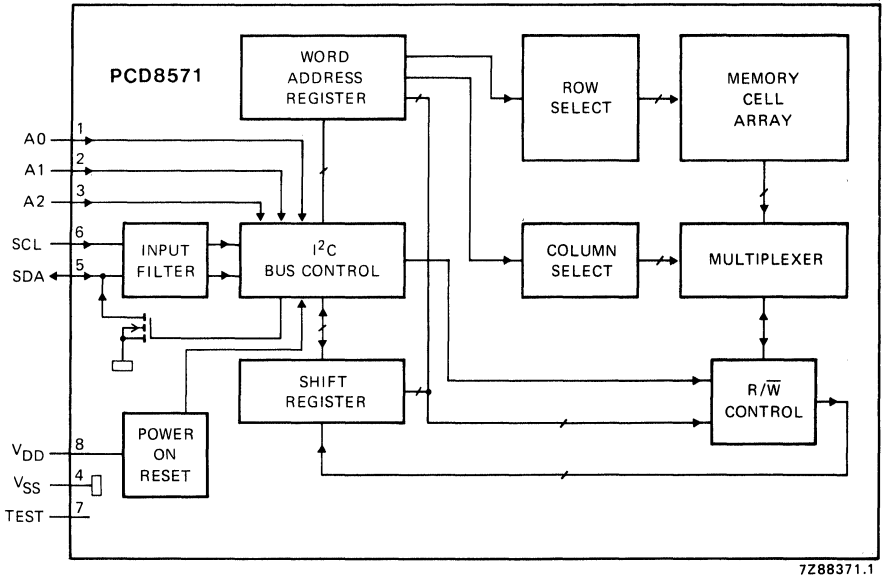


Fig. 1 Block diagram.

PACKAGES OUTLINES

PCD8571P: 8-lead DIL; plastic (SOT-97A).
PCD8571D: 8-lead DIL; ceramic (cerdip) (SOT-151A).
PCD8571T: 8-lead mini-pack (VSO-8; SOT-176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line } I^2C bus
6	SCL	serial clock line } I^2C bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Fig. 14 and 15)
8	V_{DD}	positive supply

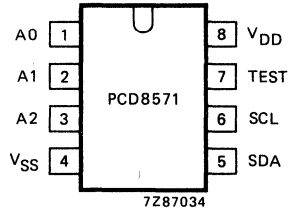


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}		−0,8 to + 8,0	V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8	V
D.C. input current (any input)	$\pm I_I$	max.	10	mA
D.C. output current (any output)	$\pm I_O$	max.	10	mA
Supply current (pin 4 or pin 8)	$\pm I_{DD}; I_{SS}$	max.	50	mA
Power dissipation per package	P_{tot}	max.	300	mW
Power dissipation per output	P	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating temperature range	T_{amb}		−25 to + 70	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at f_{SCL} = 100 kHz; $V_I = V_{SS}$ or V_{DD}					
operating	I_{DD}	–	–	200	μA
standby	I_{DDO}	–	–	5	μA
Power-on reset voltage level* at $V_{SCL} = V_{SDA} = V_{DD}$	V_{POR}	1,5	1,9	2,3	V
Input SCL; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	100	nA
Input leakage current (A0, A1, A2) at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	100	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	–	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	2	μA
Power saving mode (Fig. 14)					
Supply current at T_{amb} = 25 °C; TEST = A0 = A1 = A2 = V_{DDR}	I_{DDS}	–	50	200	nA

* The power-on reset circuit resets the I²C bus logic when $V_{DD} < V_{POR}$.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

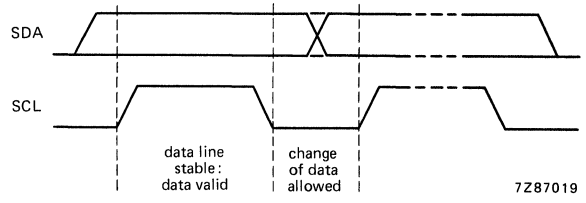


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

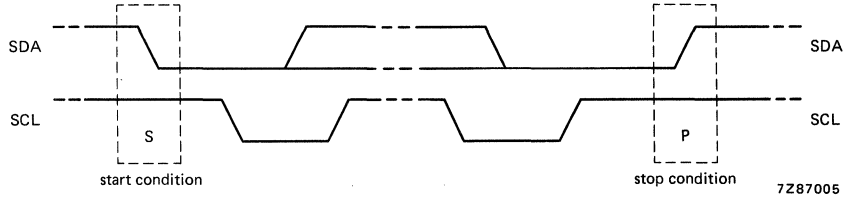


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

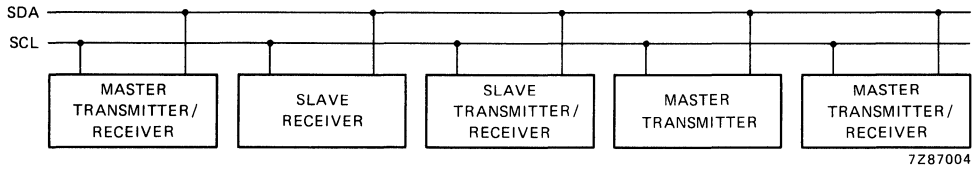


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

8

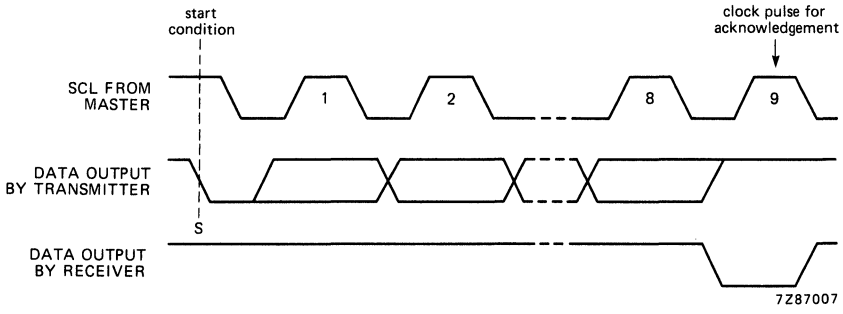


Fig. 6 Acknowledgement on the I^2C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCD8571 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

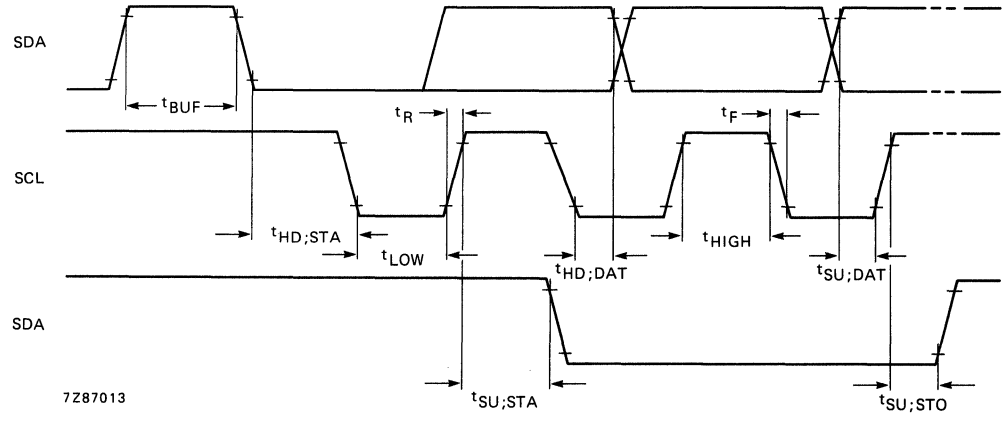


Fig. 7 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

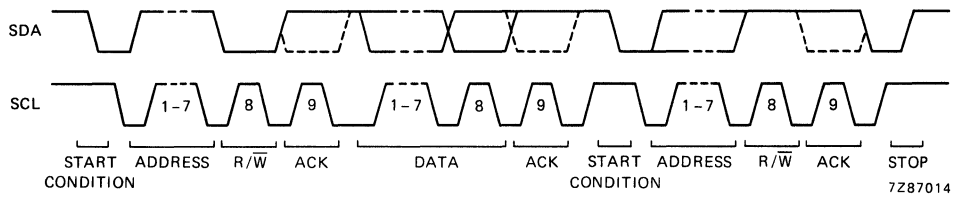


Fig. 8 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 9.

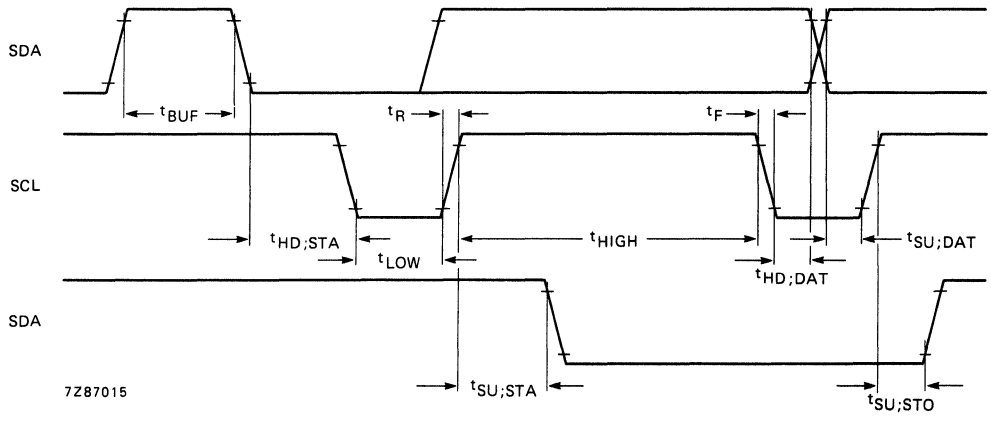


Fig. 9 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

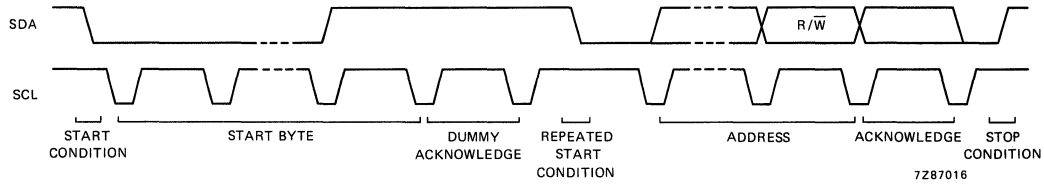


Fig. 10 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCD8571 READ and WRITE cycles is shown in Fig. 11.

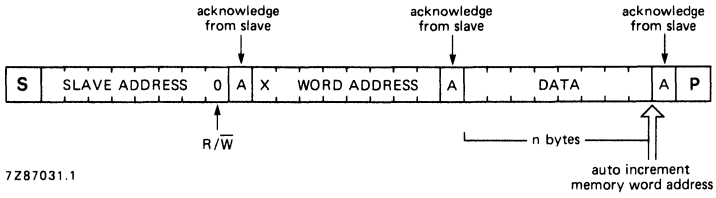


Fig. 11(a) Master transmits to slave receiver (WRITE mode).

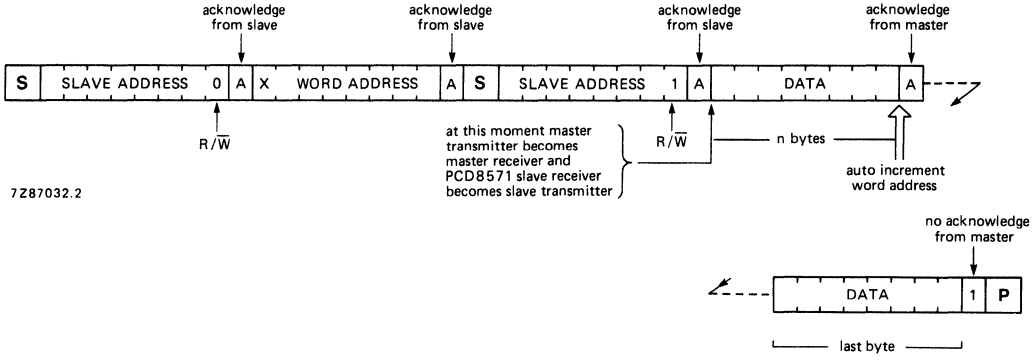


Fig. 11(b) Master reads after setting word address (WRITE word address; READ data).

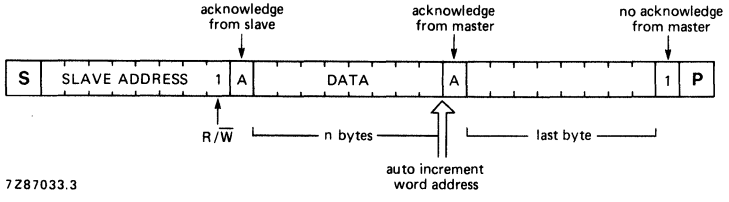


Fig. 11(c) Master reads slave immediately after first byte (READ mode).

Note

X = don't care bit.

APPLICATION INFORMATION

The PCD8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

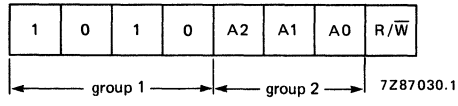


Fig. 12 PCD8571 address.

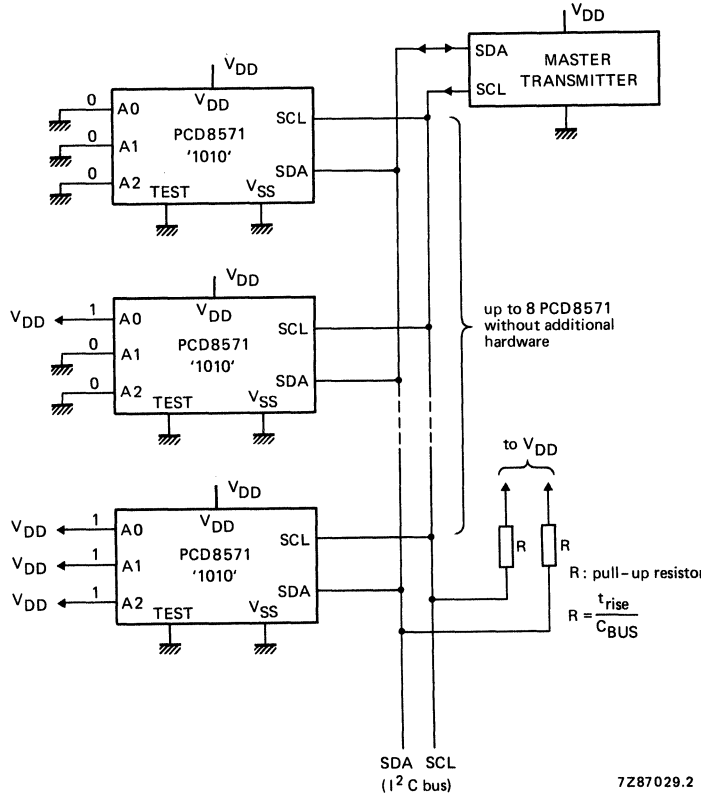


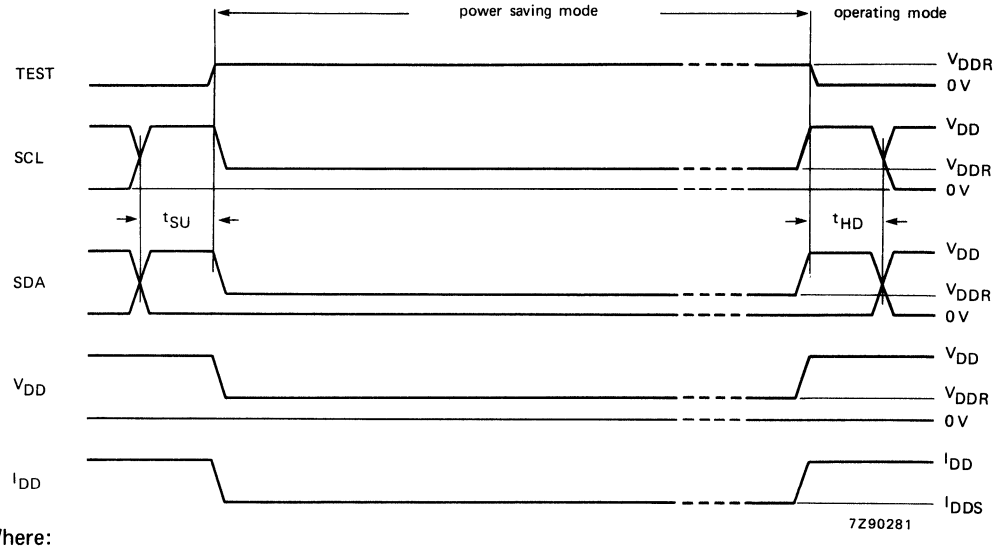
Fig. 13 PCD8571 application diagram.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open.

POWER SAVING MODE

With the condition TEST = A2 = A1 = A0 = V_{DDR}, the PCD8571 goes into the power saving mode.



Where:
$t_{SU} \geqslant 4\ \mu s$
$t_{HD} \geqslant 4\ \mu s$

Fig. 14 Timing for power saving mode.

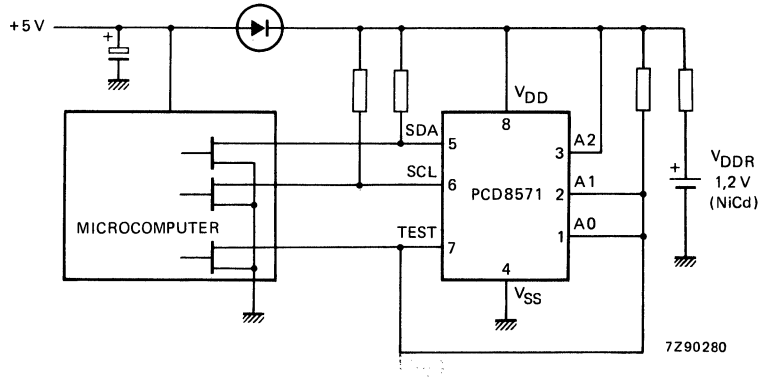


Fig. 15 Application example for power saving mode.

Note

1. In the operating mode, TEST = 0 (A0, A1 = 0; A2 = 1).
2. In the power saving mode, TEST = A0 = A1 = A2 = V_{DDR}.

8-Bit Remote I/O Expander | PCF8574

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF8500 microcomputer families via the two-line serial bidirectional bus (I^2C).
It can also interface microcomputers without a serial interface to the I^2C bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C bus. This means that the PCF8574 can remain a simple slave device.

Features

- Operating supply voltage 2,5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I^2C bus
- Peripheral for the MAB8400 and PCF8500 microcomputer families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 possible with mask option)

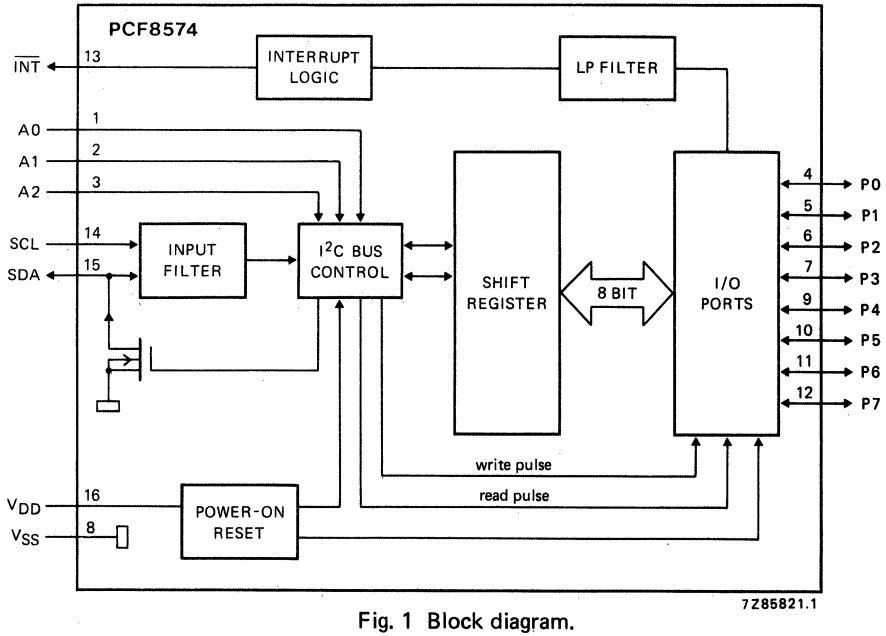


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8574P: 16-lead DIL; plastic (SOT-38).
PCF8574T: 16-lead mini-pack; plastic (SO-16L; SOT-162A).

PINNING

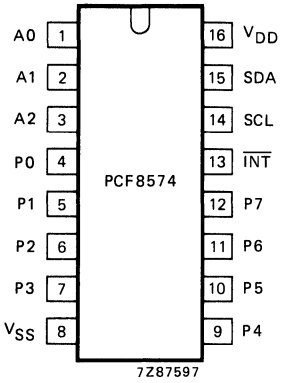


Fig. 2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

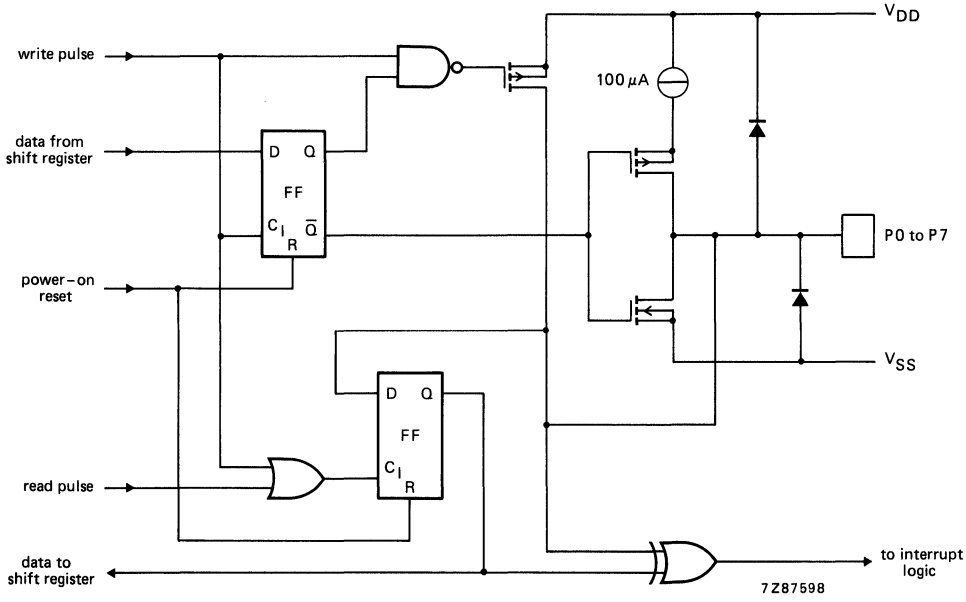


Fig. 3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

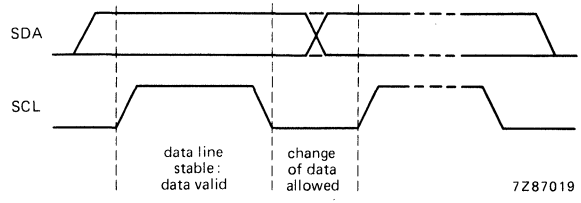


Fig. 4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

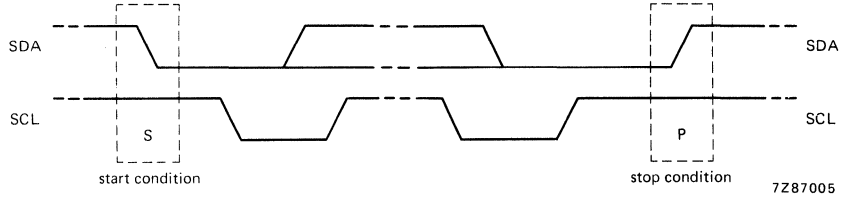


Fig. 5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

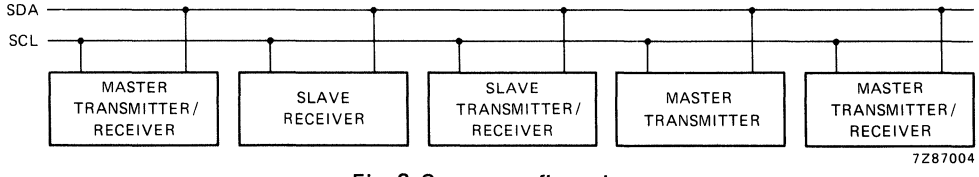


Fig. 6 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

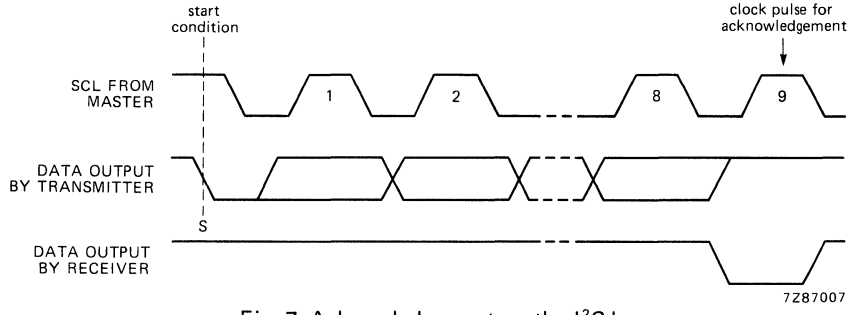


Fig. 7 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8574 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 8.

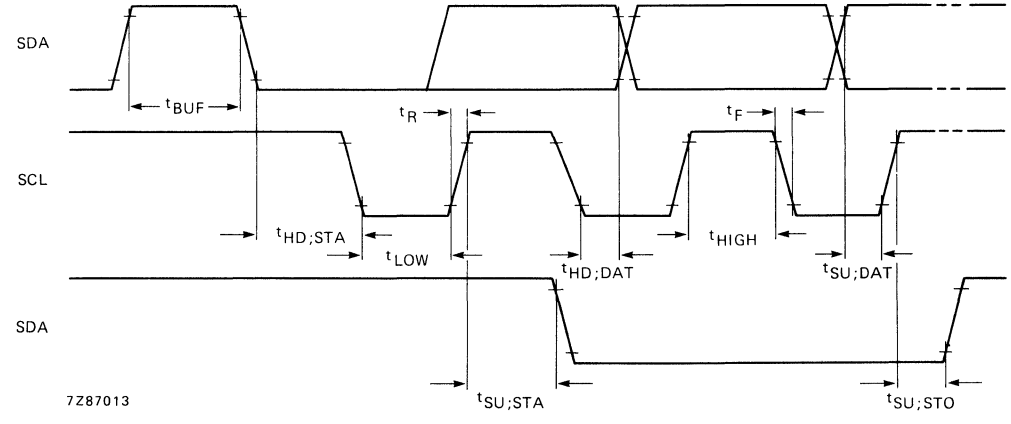


Fig. 8 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

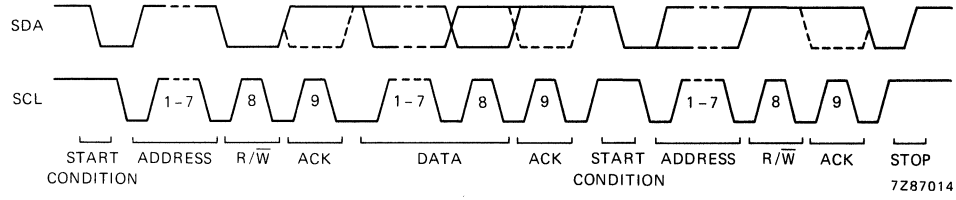


Fig. 9 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

CHARACTERISTICS OF THE I²C BUS (continued)

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 10.

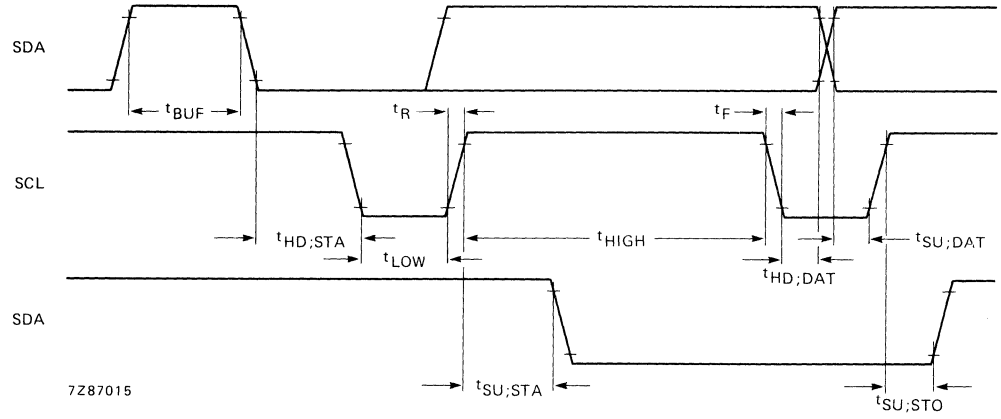


Fig. 10 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

8

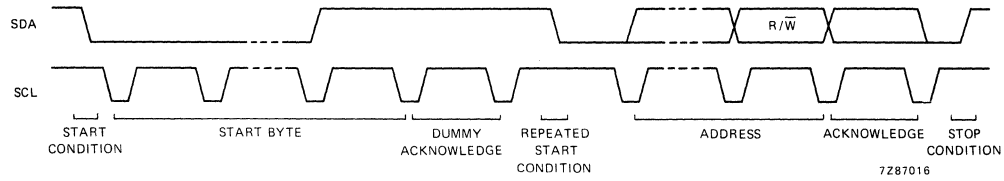


Fig. 11 Complete data transfer in the low-speed mode.

Where:	
Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 12 and 13)

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

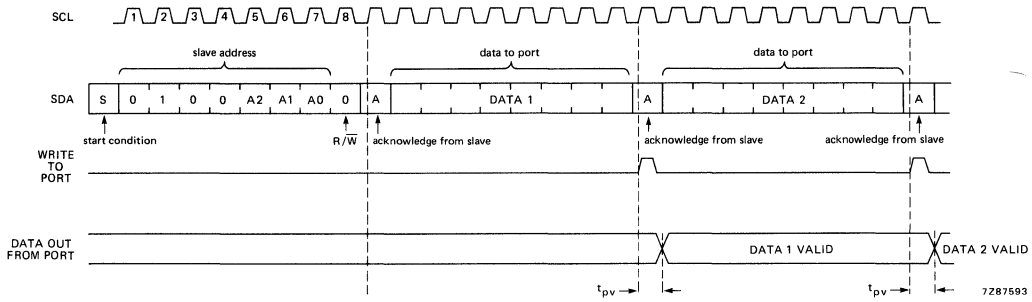


Fig. 12 WRITE mode (output port).

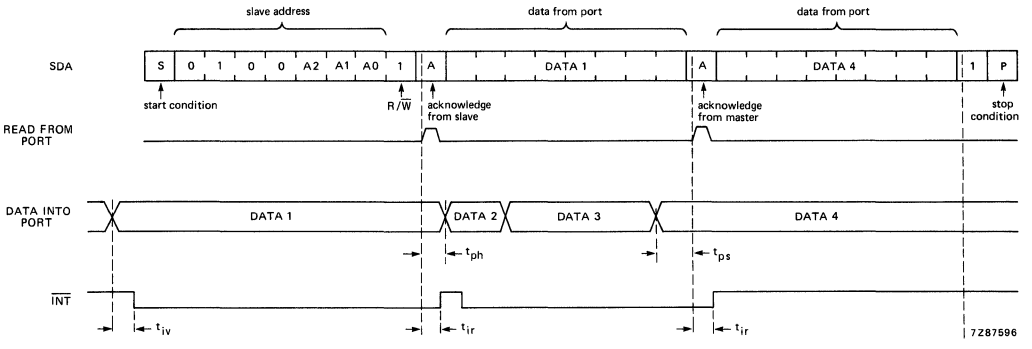


Fig. 13 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 14 and 15)

The PCF8574 provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

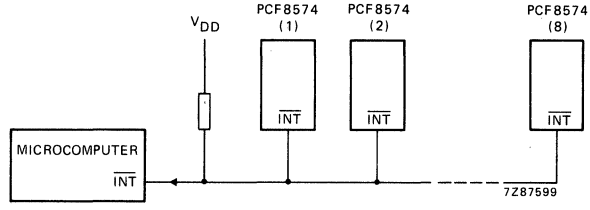


Fig. 14 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH to LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

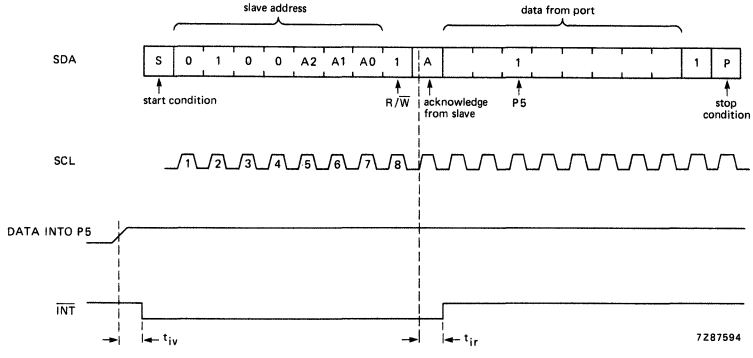


Fig. 15 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig. 16)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW to HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

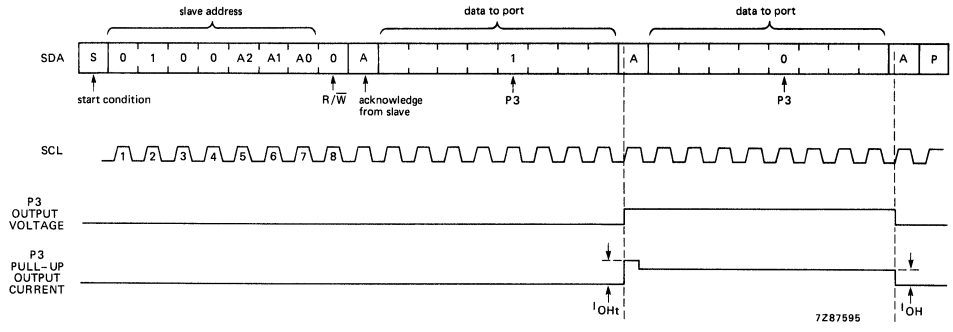


Fig. 16 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

8

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 7	V
Input voltage range (any pin)	V_I	V_{SS}−0,5 to V_{DD} + 0,5	V
D.C. current into any input	$\pm I_I$	max. 20	mA
D.C. current into any output	$\pm I_O$	max. 25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; I_{SS}	max. 100	mA
Total power dissipation	P_{tot}	max. 400	mW
Power dissipation per output	P_o	max. 100	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
at V_{DD} = 6 V; no load, inputs at V_{DD}, V_{SS}					
operating	I_{DD}	–	–	100	μA
standby	I_{DDO}	–	–	10	μA
Power-on reset voltage level (note 1)	V_{REF}	–	1,3	2,4	V
Input SCL; input/output SDA (pins 14; 15)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Input/Output leakage current	$\|I_L\|$	–	–	100	nA
Clock frequency (see Fig. 8)	f_{SCL}	–	–	100	kHz
Tolerable spike width					
at SCL and SDA input	t_s	–	–	100	ns
Input capacitance (SCL, SDA)					
at $V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports (pins 4 to 7; 9 to 12)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Maximum allowed input current through protection diode					
at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW					
at V_{OL} = 1 V; V_{DD} = 2,5 V	I_{OL}	5	–	–	mA
Output current HIGH					
at $V_{OH} = V_{SS}$ (current source only)	$-I_{OH}$	30	100	300	μA
Transient pull-up current HIGH during acknowledge (see Fig. 16)					
at $V_{OH} = V_{SS}$	$-I_{OHt}$	–	0,5	–	mA
Input/Output capacitance	$C_{I/O}$	–	–	10	pF
Port timing; $C_L \leqslant 100$ pF (see Figs 12 and 13)					
Output data valid	t_{pv}	–	–	4	μs
Input data set-up	t_{ps}	0	–	–	μs
Input data hold	t_{ph}	4	–	–	μs

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$ (pin 13)					
Output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA
Output current HIGH at $V_{OH} = V_{DD}$	$\|I_{OH}\|$	–	–	100	nA
$\overline{INT}$ timing; $C_L \leqslant 100$ pF (see Fig. 13)					
Input data valid	t_{iv}	–	–	4	μs
Reset delay	t_{ir}	–	–	4	μs
Select inputs A0, A1, A2 (pins 1 to 3)					
Input voltage LOW	V_{IH}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	100	nA

Note 1

The power-on reset circuit resets the I^2C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

8

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 100 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

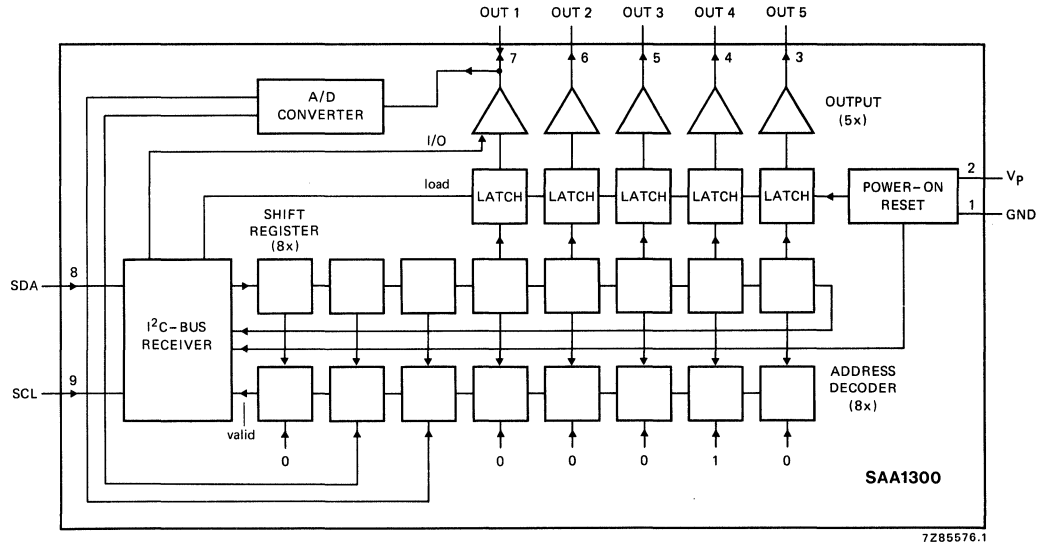


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142B).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION*

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

8

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max. 13,2	V
Input voltage range at SDA, SCL	V_I	−0,5 to + 13,7	V
Input voltage range at OUT 1	V_I	−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O	−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max. 20	mA
Input current at OUT 1	I_I	max. 20	mA
Total power dissipation	P_{tot}	max. 650	mW
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 80	°C

* Detailed information is given in a separate data sheet.

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	–	12	V
Supply current	I_P	–	10	–	mA
Power-on reset level output stage in "OFF" condition	V_{PR}	–	–	3,5	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	2,8	–	V_P + 0,5	V
Input voltage LOW	V_{IL}	0	–	1,8	V
Input current HIGH	$-I_{IH}$	–	–	50	μA
Input current LOW	I_{IH}	–	–	0,1	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source : "ON"	I_{Oso}	+ 100	–	+ 150	mA
Maximum output current; source : "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso}	V_{OH}	–	–	V_P –2	V
Output current; sink: "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi}	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 12,5 mA	V_{OM}	–	–	V_P –0,5	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V

* Outputs must not be driven simultaneously at maximum source current.

1GHz Divide by 64 — SAB1164/65

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C. It features a high sensitivity and low harmonic contents of the output signal.

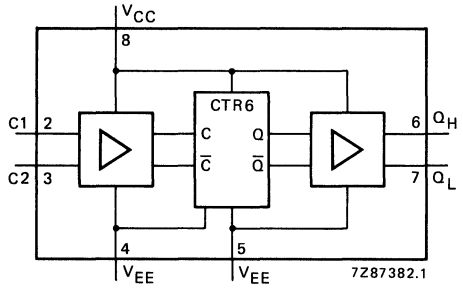


Fig. 1 Block diagram. CTR6 = 6 binary dividers = (÷ 64).

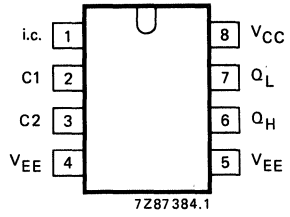
QUICK REFERENCE DATA

Supply voltage (pin 8)	V_{CC}	5 ± 10%	V
Input frequency range (pins 2 and 3)	f_i	70 to 1000	MHz
Output voltage swing (pins 6 and 7)	$V_{o(p-p)}$	typ. 1	V
Supply current; unloaded (pin 8)	I_{CC}	typ. 42	mA
Operating ambient temperature	T_{amb}	0 to + 70	°C

8

PACKAGE OUTLINE

SAB1164P: 8-lead DIL; plastic (SOT-97A).



PINNING

V_{CC}	positive supply
V_{EE}	0 V; ground
C_1, C_2	differential inputs
Q_H, Q_L	complementary outputs
i.c.	internally connected

Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-64 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7 V
Input voltage	V_i	0 to V_{CC}	V
Storage temperature	T_{stg}	−55 to + 125	°C
Junction temperature	T_j	max. 125	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c\text{-}a}$	= 120	K/W

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Output voltage				
HIGH level	V_{OH}	max.	V_{CC}	V
LOW level	V_{OL}	max.	V_{CC}−0,8	V
Supply current	I_{CC}	typ.	42	mA
		max.	50	mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 70 °C.

		min.	typ.	max.	unit
Input voltage r.m.s. value (see Fig. 4)					
input frequency 70 MHz	$V_{i(rms)}$	–	9	17,5	mV
150 MHz		–	4	10	mV
300 MHz		–	3	10	mV
500 MHz		–	3	10	mV
900 MHz		–	2	10	mV
1 GHz		–	3	17,5	mV
Input overload voltage r.m.s. value					
input frequency range 70 MHz up to 1 GHz	$V_{i(rms)}$	–	–	200	mV
Output voltage swing	$V_{o(p-p)}$	0,8	1	–	V
Output resistance					
SAB1164	R_o	–	1	–	kΩ
SAB1165	R_o	–	0,5	–	kΩ
Output unbalance	ΔV_o	–	–	0,1	V
Output rise time*					
f_i = 1 GHz	t_{TLH}	–	25	–	ns
Output fall time*					
f_i = 1 GHz	t_{THL}	–	25	–	ns

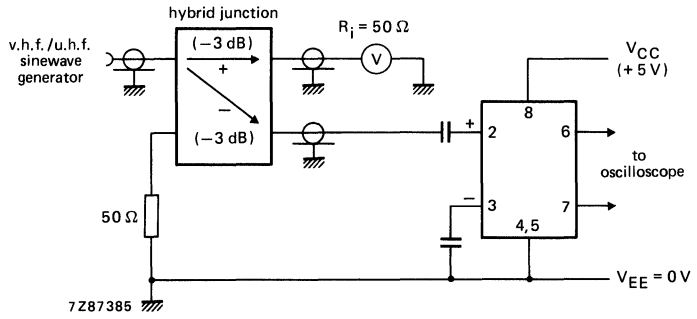


Fig. 3 Test circuit for defining input voltage.

– Cables must be 50 Ω coaxial.
– The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
– All connections to the device and to the meter must be kept short and of approximately equal lengths.
– Hybrid junction is ANZAC H-183-4 or similar.

* Between 10% and 90% of observed waveform.

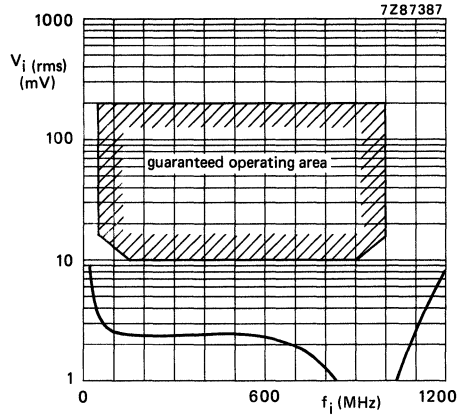


Fig. 4 Typical sensitivity curve under nominal conditions.

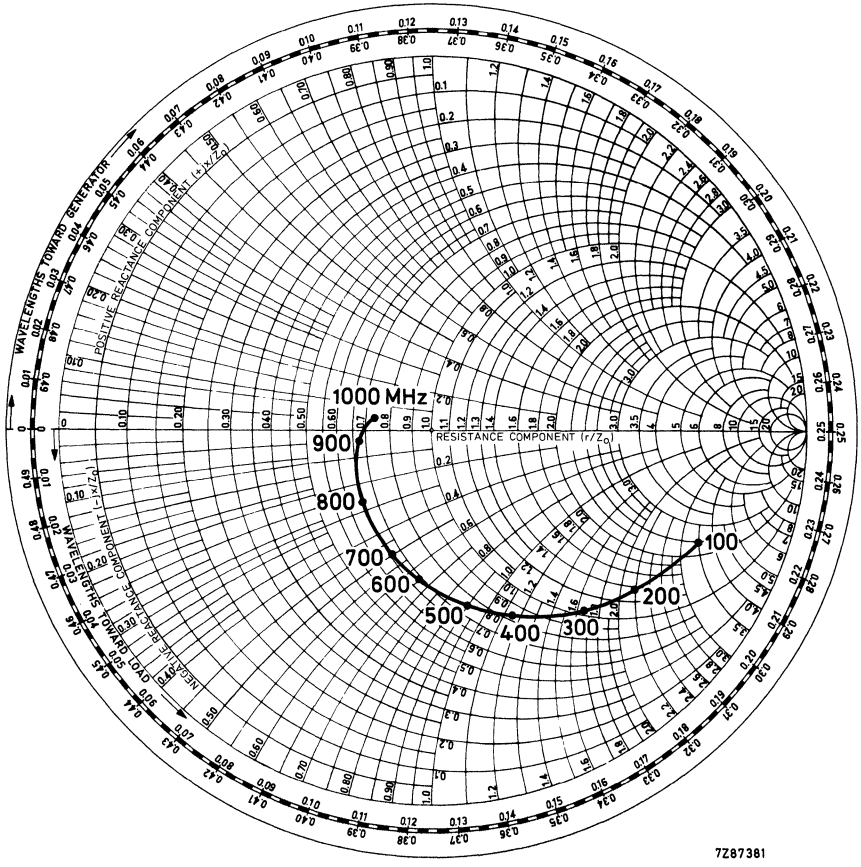


Fig. 5 Smith chart of typical input impedance.
$V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 50 Ω.

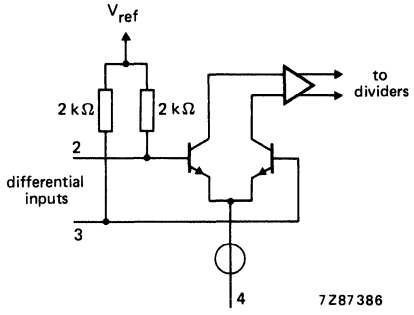


Fig. 6 Input stage.

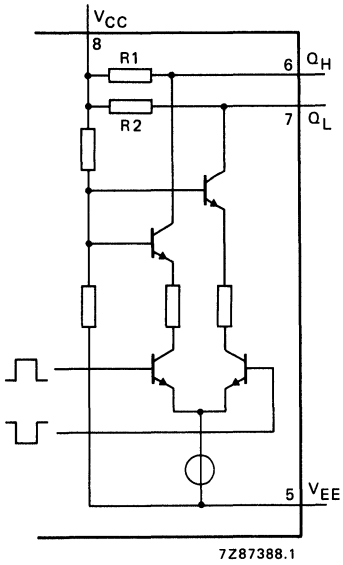


Fig. 7 Output stage. V_{CC} = 5 V.
SAB1164: R1 = R2 = 1 kΩ; I = 1 mA
SAB1165: R1 = R2 = 0,5 kΩ; I = 2 mA.

APPLICATION INFORMATION

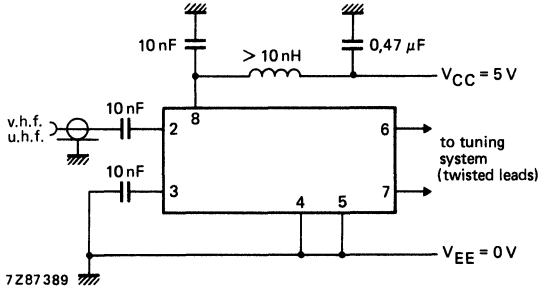


Fig. 8 Circuit diagram. Application in a television tuning system.
The output peak-to-peak voltage is about 1 V.

1GHz Divide by 256 SAB1256

This silicon monolithic integrated circuit is a prescaler in current-mode logic. It contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a television tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C. It features a high sensitivity and low harmonic contents of the output signal.

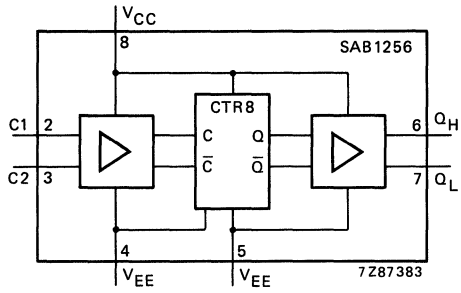


Fig. 1 Block diagram. CTR8 = 8 binary dividers = (÷ 256).

QUICK REFERENCE DATA

Supply voltage (pin 8)	V_{CC}	5 ± 10%	V
Input frequency range (pins 2 and 3)	f_i	70 to 1000	MHz
Output voltage swing (pins 6 and 7)	$V_{o(p-p)}$	typ. 1	V
Supply current, unloaded (pin 8)	I_{CC}	typ. 47	mA
Operating ambient temperature	T_{amb}	0 to + 70	°C

PACKAGE OUTLINE

SAB1256P: 8-lead DIL; plastic (SOT-97).

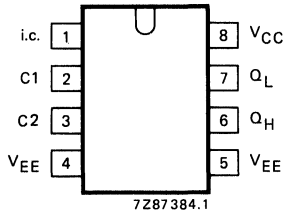


Fig. 2 Pinning diagram.

PINNING

V_{CC}	positive supply
V_{EE}	0 V; ground
C_1, C_2	differential inputs
Q_H, Q_L	complementary outputs
i.c.	internally connected

FUNCTIONAL DESCRIPTION

The circuit contains an amplifier, a divide-by-256 scaler and an output stage. It has been designed to be driven by a sinusoidal signal from the local oscillator of a TV tuner, with frequencies from 70 MHz up to 1 GHz, for a supply voltage of 5 V ± 10% and an ambient temperature of 0 to 70 °C.

The inputs are differential and are internally biased to permit capacitive coupling. For asymmetrical drive the unused input should be connected to ground via a capacitor.

The first divider stage will oscillate in the absence of an input signal; an input signal within the specified range will suppress this oscillation.

The output differential stage has two complementary outputs. The output voltage edges are slowed down internally to reduce the harmonic contents of the signal.

Wide, low-impedance ground connections and a short capacitive bypass from the V_{CC} pin to ground are recommended.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (d.c.)	V_{CC}	max.	7 V
Input voltage	V_i	0 to V_{CC}	V
Storage temperature	T_{stg}	−55 to + 125	°C
Junction temperature	T_j	max. 125	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ c\text{-}a}$	=	120 K/W

8

D.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified.

The circuit has been designed to meet the d.c. specifications as shown below, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board.

Output voltage				
HIGH level	V_{OH}	max.	V_{CC}	V
LOW level	V_{OL}	max.	V_{CC}–0,8	V
Supply current	I_{CC}	typ.	47	mA
		max.	55	mA

A.C. CHARACTERISTICS

V_{EE} = 0 V (ground); V_{CC} = 5 V ± 10%; T_{amb} = 0 to + 70 °C.

		min.	typ.	max.	unit
Input voltage r.m.s. value (see Fig. 4)					
input frequency 70 MHz	$V_{i(rms)}$	–	9	17,5	mV
150 MHz		–	4	10	mV
300 MHz		–	3	10	mV
500 MHz		–	3	10	mV
900 MHz		–	2	10	mV
1 GHz		–	3	17,5	mV
Input overload voltage r.m.s. value					
input frequency range 70 MHz to 1 GHz	$V_{i(rms)}$	–	–	200	mV
Output voltage swing	$V_{o(p-p)}$	0,8	1	–	V
Output resistance	R_o	–	1	–	kΩ
Output unbalance	ΔV_o	–	–	0,1	V
Output rise time*					
f_i = 1 GHz	t_{TLH}	–	40	–	ns
Output fall time					
f_i = 1 GHz	t_{THL}	–	40	–	ns

* Between 10% and 90% of observed waveform.

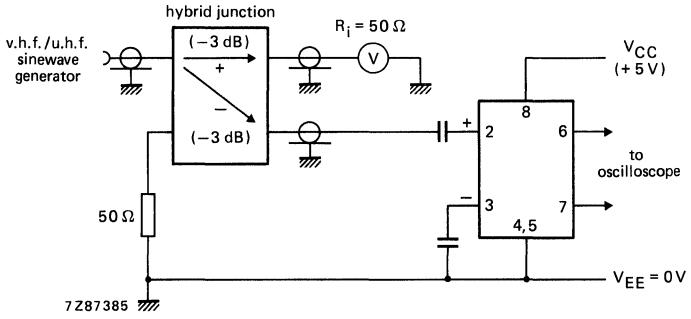


Fig. 3 Test circuit for defining input voltage.

- Cables must be 50 Ω coaxial.
- The capacitors are leadless ceramic (multilayer capacitors) of 10 nF.
- All connections to the device and to the meter must be kept short and of approximately equal lengths.
- Hybrid junction is ANZAC H-183-4 or similar.

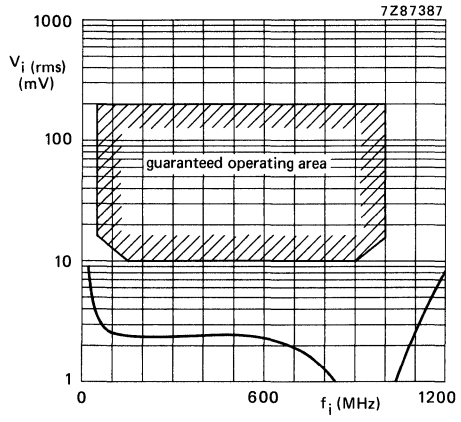


Fig. 4 Typical sensitivity curve under nominal conditions.

8

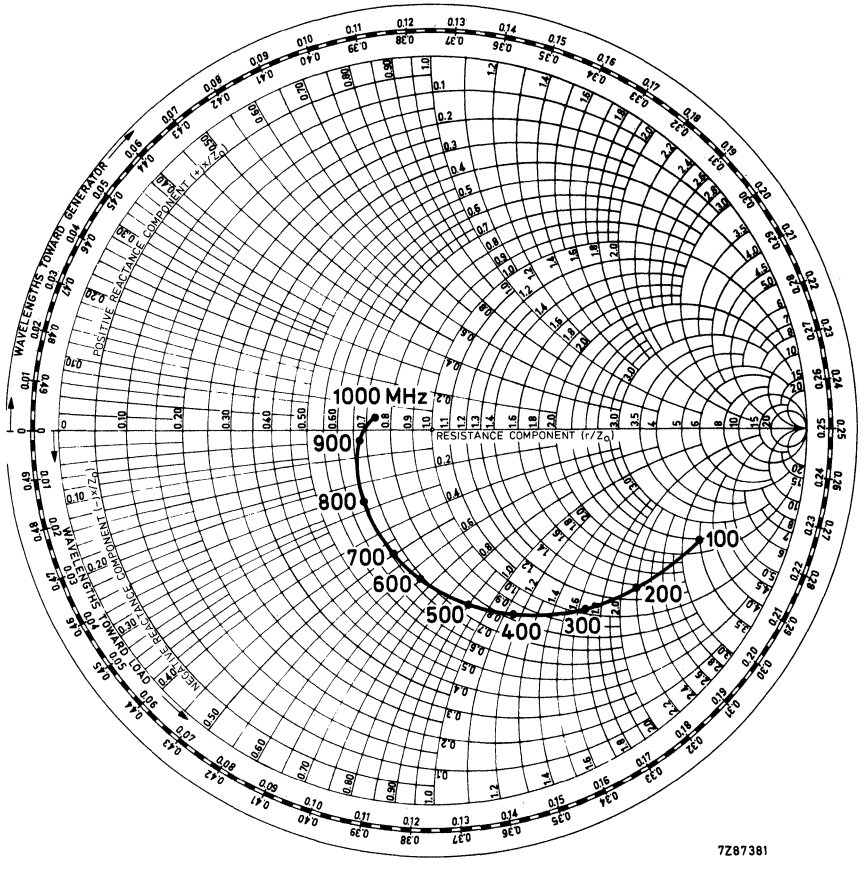


Fig. 5 Smith chart of typical input impedance.
$V_{i(rms)}$ = 25 mV; V_{CC} = 5 V; reference value = 50 Ω.

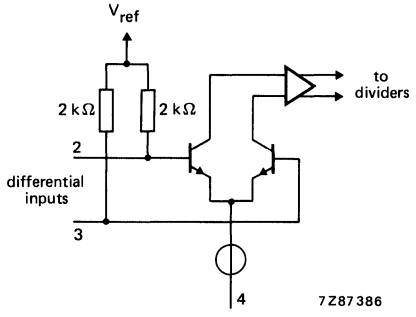


Fig. 6 Input stage.

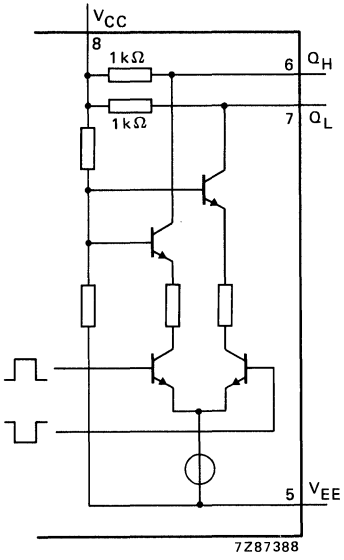


Fig. 7 Output stage.
V_{CC} = 5 V; I = 1 mA.

APPLICATION INFORMATION

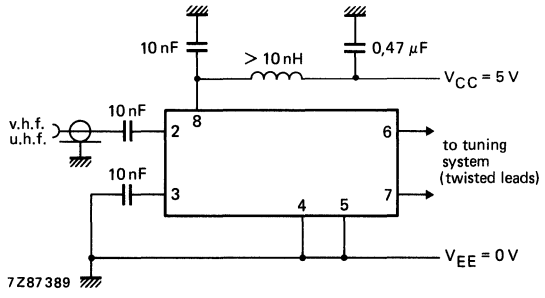


Fig. 8 Circuit diagram.
Application in a television tuning system. The output peak-to-peak voltage is about 1 V.

FLL TV Tuning Circuit | SAB3035

GENERAL DESCRIPTION

The SAB3035 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 8 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 8 static digital to analogue convertors (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages				
(pin 16)	V_{P1}	typ.	12	V
(pin 22)	V_{P2}	typ.	13	V
(pin 17)	V_{P3}	typ.	32	V
Supply currents (no outputs loaded)				
(pin 16)	I_{P1}	typ.	32	mA
(pin 22)	I_{P2}	typ.	0.1	mA
(pin 17)	I_{P3}	typ.	0.6	mA
Total power dissipation	P_{tot}	typ.	400	mW
Operating ambient temperature range	T_{amb}	−20 to +70		°C

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

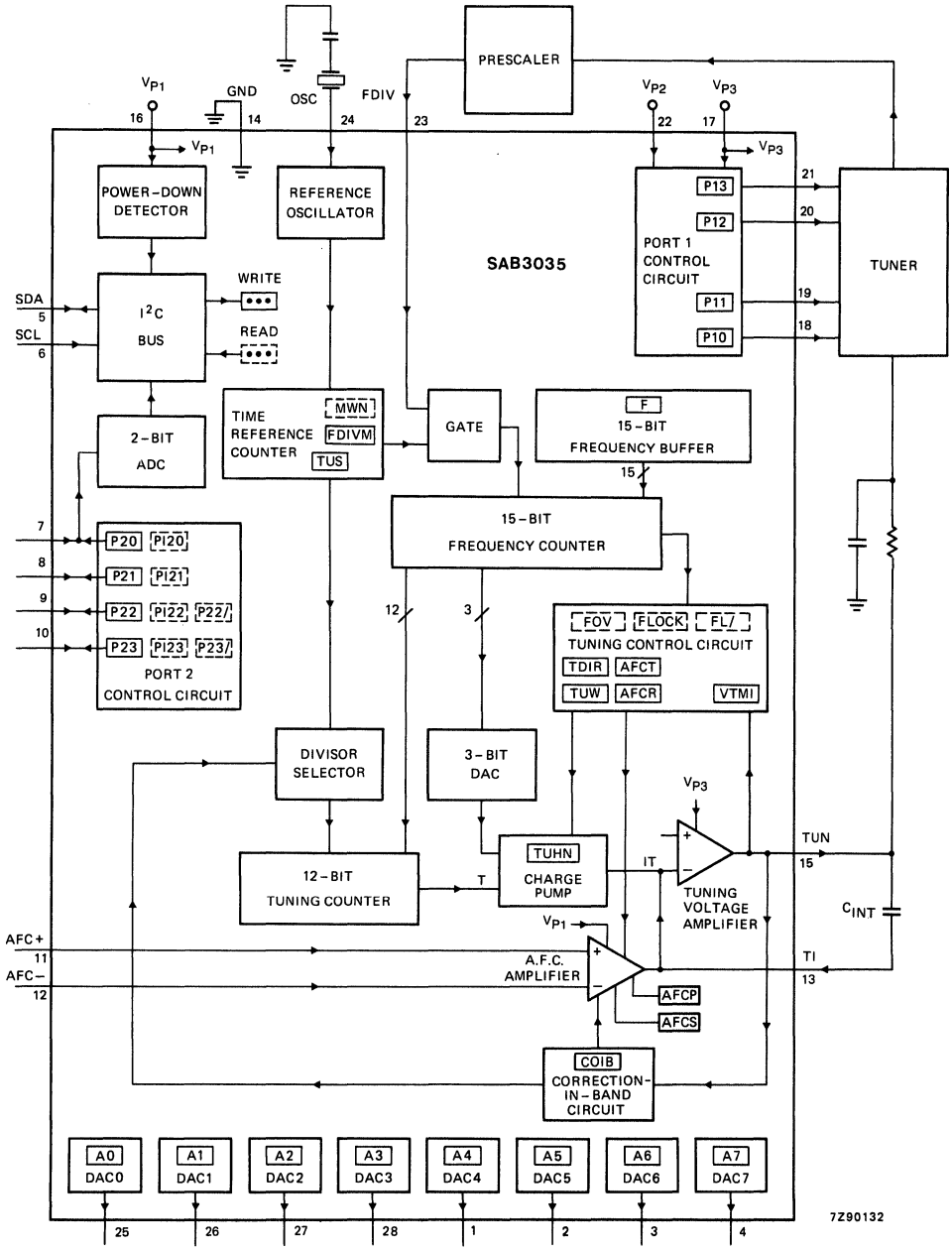


Fig. 1 Block diagram.

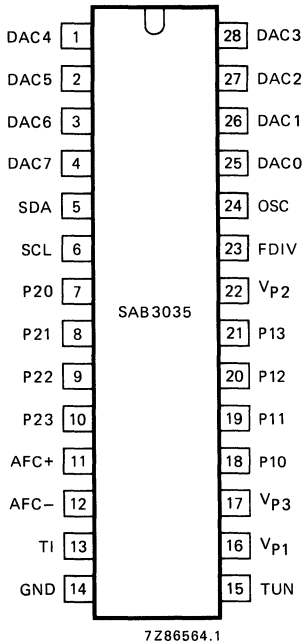


Fig. 2 Pinning diagram.

PINNING

1	DAC4	outputs of static DACs
2	DAC5	
3	DAC6	
4	DAC7	
5	SDA	serial data line (I^2C bus)
6	SCL	serial clock line (I^2C bus)
7	P20	general purpose input/output ports
8	P21	
9	P22	
10	P23	
11	AFC+	a.f.c. inputs
12	AFC–	
13	TI	tuning voltage amplifier inverting input
14	GND	ground
15	TUN	tuning voltage amplifier output
16	V_{P1}	+12 V supply voltage
17	V_{P3}	+32 V supply for tuning voltage amplifier
18	P10	High-current band-selection output ports
19	P11	
20	P12	
21	P13	
22	V_{P2}	positive supply for high-current band-selection output circuits
23	FDIV	input from prescaler
24	OSC	crystal oscillator input
25	DAC0	outputs of static DACs
26	DAC1	
27	DAC2	
28	DAC3	

FUNCTIONAL DESCRIPTION

The SAB3035 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6.4 ms (or 2.56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 $\mu A\ \mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250\ \mu A\ \mu s$ (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Eight 6-bit digital-to-analogue converters DAC0 to DAC7 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8.5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

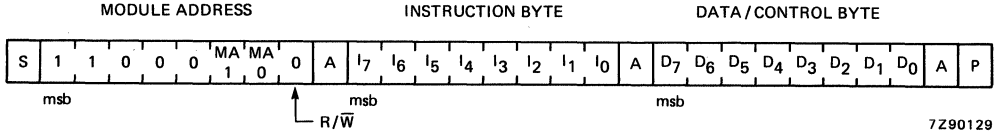


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8.5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3.5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0.25*	0.25*
0	0	1	0.5	0.5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0.25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

8

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6.4*	5.12*
1	64	2.56	1.28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X2, X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

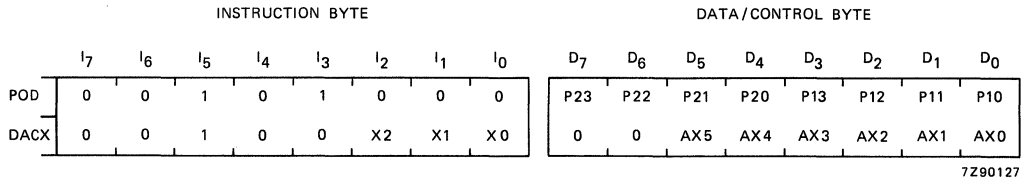


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

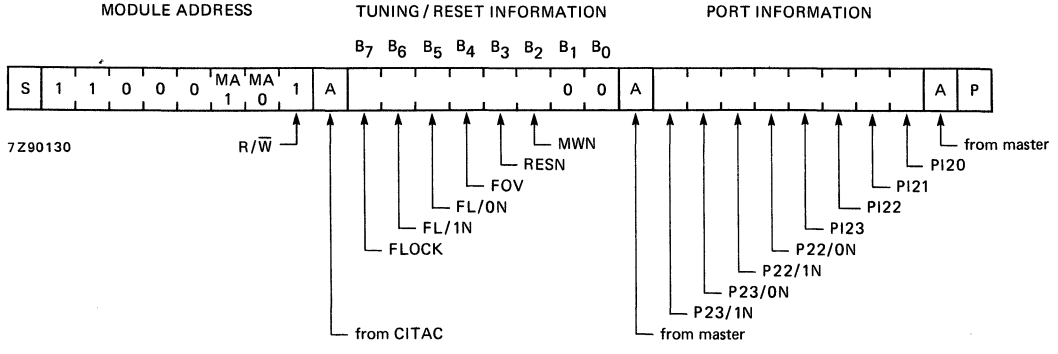


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1.28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

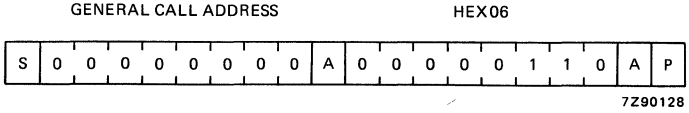


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 16)	V_{P1}	−0.3 to +18	V
(pin 22)	V_{P2}	−0.3 to +18	V
(pin 17)	V_{P3}	−0.3 to +36	V
Input/output voltage ranges:			
(pin 5)	V_{SDA}	−0.3 to +18	V
(pin 6)	V_{SCL}	−0.3 to +18	V
(pins 7 to 10)	V_{P2X}	−0.3 to +18	V
(pins 11 and 12)	$V_{AFC+,AFC-}$	−0.3 to V_{P1}*	V
(pin 13)	V_{TI}	−0.3 to V_{P1}*	V
(pin 15)	V_{TUN}	−0.3 to V_{P3}*	V
(pins 18 to 21)	V_{P1X}	−0.3 to V_{P2}**	V
(pin 23)	V_{FDIV}	−0.3 to V_{P1}*	V
(pin 24)	V_{OSC}	−0.3 to +5	V
(pins 1 to 4 and 25 to 28)	V_{DACX}	−0.3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.

** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10.5	12	13.5	V
	V_{P2}	4.7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	20	32	50	mA
	I_{P2}	0	–	0.1	mA
	I_{P3}	0.2	0.6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0.2	–	2	mA
Total power dissipation	P_{tot}	–	400	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I^2C bus inputs/outputs					
SDA input (pin 5); SCL input (pin 6)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0.3	–	1.5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 5, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0.4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 7 to 10, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	–0.3	–	0.8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current	I_{OL}	–	4	–	mA

8

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 11, 12)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2.5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 13, 15)					
Maximum output voltage at $I_{load} = \pm 2.5$ mA	V_{TUN}	$V_{P3}-1.6$	–	$V_{P3}-0.4$	V
Minimum output voltage at $I_{load} = \pm 2.5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2.5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0.4	1	1.7	µA µs
0 1	CH_{01}	4	8	14	µA µs
1 0	CH_{10}	15	30	48	µA µs
1 1	CH_{11}	130	250	370	µA µs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1.7	3.5	5.1	µA
0 1	I_{T01}	15	29	41	µA
1 0	I_{T10}	65	110	160	µA
1 1	I_{T11}	530	875	1220	µA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 18 to 21)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0.6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 23)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0.1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14.5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

8

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 7 (pins 25 to 28 and 1 to 4)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11.5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0.1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0.5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7.5	–	9.5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 7) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0.3	–	16	V
0 1	V_{VA01}	−0.3	–	0.8	V
1 0	V_{VA10}	2.5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0.3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0.3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification.
After reset has been activated, transmission may only be started after a 50 μs delay.

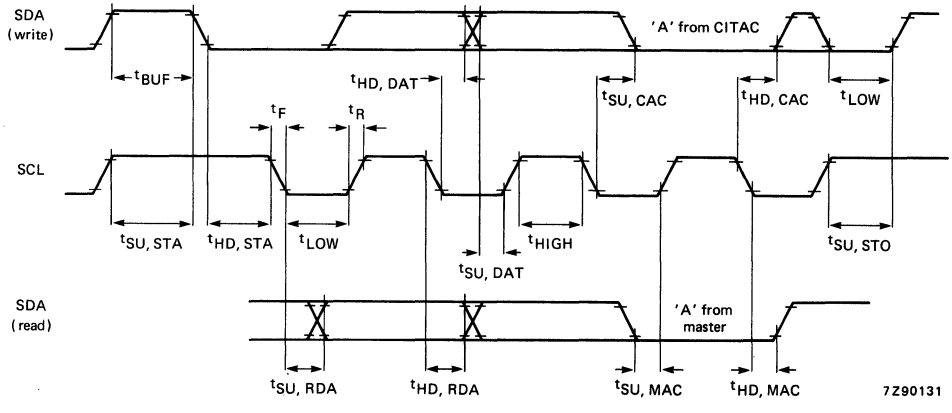


Fig. 8 I²C bus timing SAB3035.

FLL TV Tuning Circuit — SAB3036

GENERAL DESCRIPTION

The SAB3036 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages			
(pin 5)	V_{P1}	typ.	12 V
(pin 14)	V_{P2}	typ.	13 V
(pin 9)	V_{P3}	typ.	32 V
Supply currents (no outputs loaded)			
(pin 5)	I_{P1}	typ.	23 mA
(pin 14)	I_{P2}	typ.	0.1 mA
(pin 9)	I_{P3}	typ.	0.6 mA
Total power dissipation	P_{tot}	typ.	300 mW
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

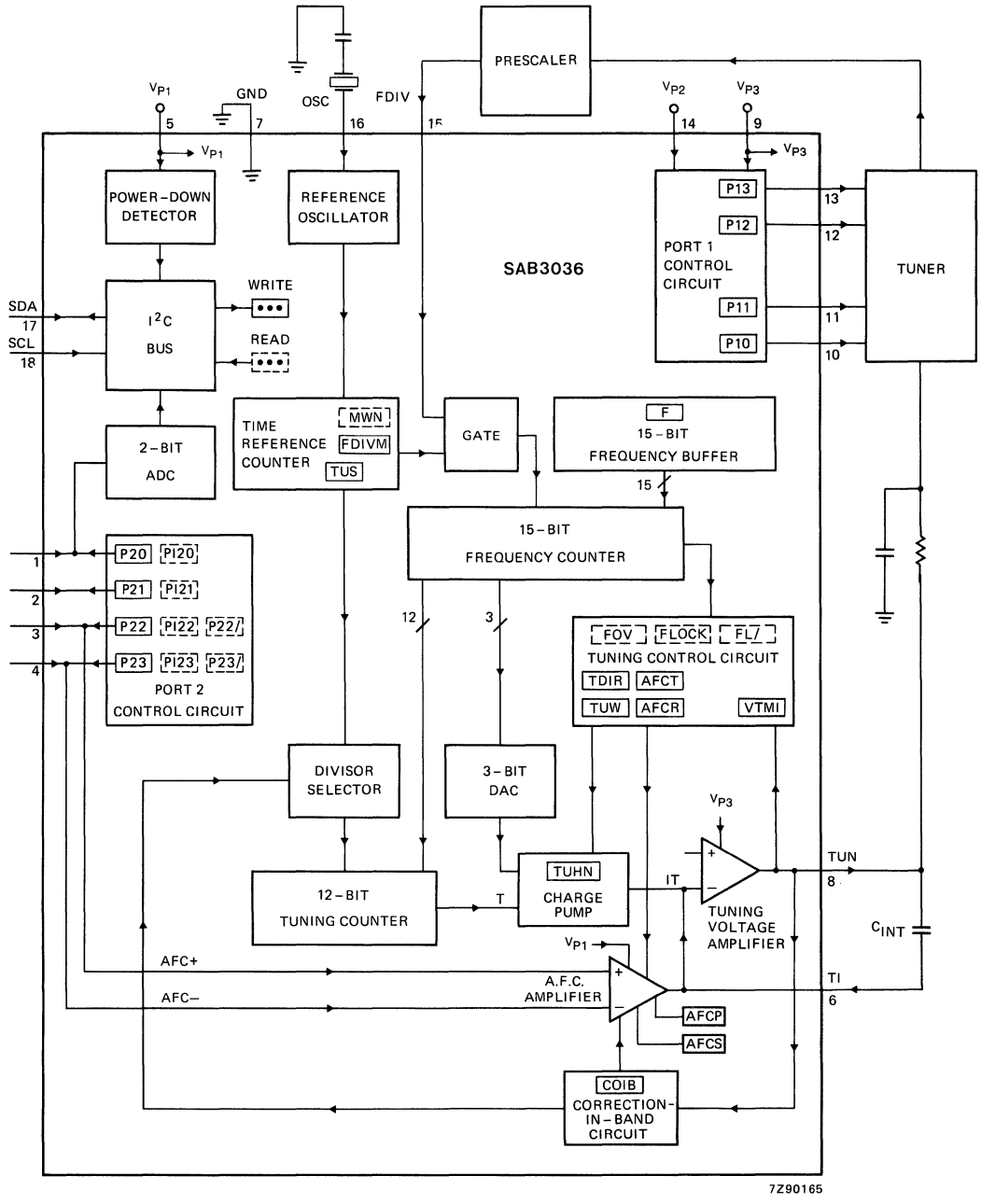


Fig. 1 Block diagram.

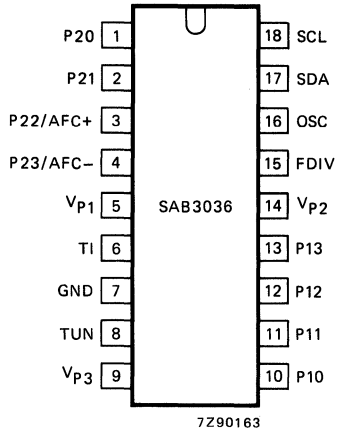


Fig. 2 Pinning diagram.

PINNING

1	P20	general purpose input/output ports
2	P21	
3	P22/AFC+	general purpose input/output ports and a.f.c. inputs
4	P23/AFC–	
5	V_{P1}	+ 12 V supply voltage
6	TI	tuning voltage amplifier inverting input
7	GND	ground
8	TUN	tuning voltage amplifier output
9	V_{P3}	+ 32 V supply for tuning voltage amplifier
10	P10	high-current band-selection output ports
11	P11	
12	P12	
13	P13	
14	V_{P2}	positive supply for high-current band-selection output circuits
15	FDIV	input from prescaler
16	OSC	crystal oscillator input
17	SDA	serial data line, I^2C bus
18	SCL	serial clock line, I^2C bus

FUNCTIONAL DESCRIPTION

The SAB3036 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6.4 ms (or 2.56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 $\mu A\ \mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250\ \mu A\ \mu s$ (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals and are connected with the AFC+ and AFC– inputs respectively. The a.f.c. amplifier must be switched off when P22 and/or P23 are used. When a.f.c. is used, P22 and P23 must be programmed HIGH (high impedance state). With the aid of port P20, up to three independent module addresses can be programmed.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8.5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

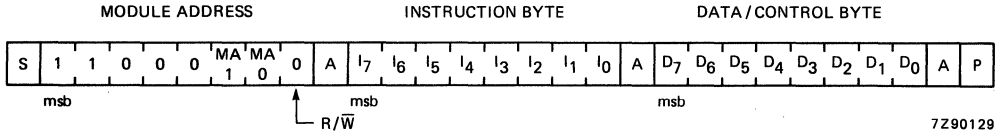


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8.5$ V (typical)).

OPERATION (continued)

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

INSTRUCTION BYTE

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
freq.	1	F14	F13	F12	F11	F10	F9	F8
TCD0	0	0	1	0	1	0	0	1
TCD1	0	0	1	0	1	0	1	0
TCD2	0	0	1	0	1	0	1	1

DATA/CONTROL BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
F7	F6	F5	F4	F3	F2	F1	F0
AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3,5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

8

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0.25*	0.25*
0	0	1	0.5	0.5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

OPERATION (continued)

Table 5 Tuning window programming

TUW1	TUW0	|Δf| (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as |Δf| is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	|Δf| (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0.25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6.4*	5.12*
1	64	2.56	1.28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction byte POD (port output data) is shown in Fig. 5, together with the corresponding data/control byte. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

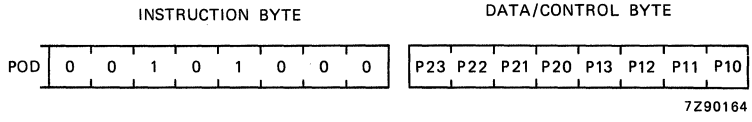


Fig. 5 Control programming.

OPERATION (continued)

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

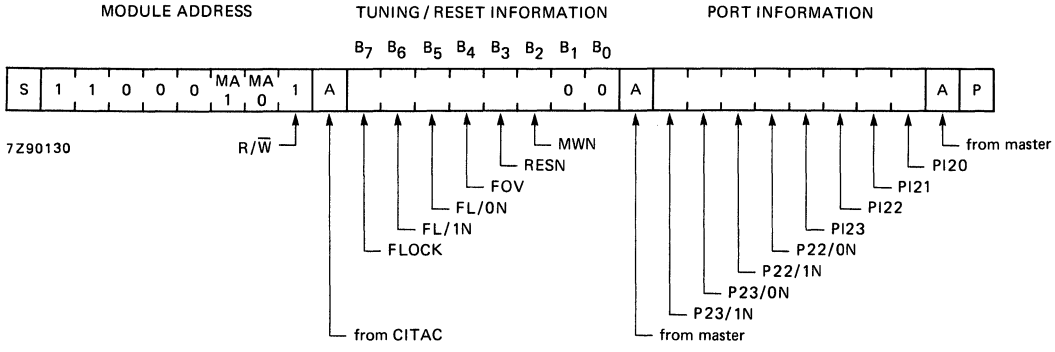


Fig. 6 Information byte format.

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1.28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

8

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

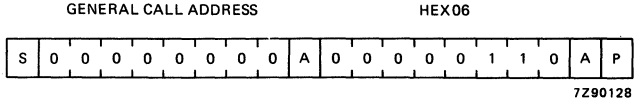


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:		
(pin 5)	V_{P1}	−0.3 to + 18 V
(pin 14)	V_{P2}	−0.3 to + 18 V
(pin 9)	V_{P3}	−0.3 to + 36 V
Input/output voltage ranges:		
(pin 17)	V_{SDA}	−0.3 to + 18 V
(pin 18)	V_{SCL}	−0.3 to + 18 V
(pins 1 and 2)	$V_{P20, P21}$	−0.3 to + 18 V
(pins 3 and 4)	$V_{P22, P23, AFC}$	−0.3 to V_{P1}* V
(pin 6)	V_{TI}	−0.3 to V_{P1}* V
(pin 8)	V_{TUN}	−0.3 to V_{P3}* V
(pins 10 to 13)	V_{P1X}	−0.3 to V_{P2}** V
(pin 15)	V_{FDIV}	−0.3 to V_{P1}* V
(pin 16)	V_{OSC}	−0.3 to + 5 V
Total power dissipation	P_{tot}	max. 1000 mW
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature	T_{amb}	−20 to + 70 °C

* Pin voltage may exceed supply voltage if current is limited to 10 mA.
** Pin voltage must not exceed 18 V but may exceed V_{P2} if current is limited to 200 mA.

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10.5	12	13.5	V
	V_{P2}	4.7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	14	23	40	mA
	I_{P2}	0	–	0.1	mA
	I_{P3}	0.2	0.6	2	mA
Additional supply currents (A)	I_{P2A}	–2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0.2	–	2	mA
Total power dissipation	P_{tot}	–	300	–	mW
Operating ambient temperature	T_{amb}	–20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 17); SCL input (pin 18)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	–0.3	–	1.5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 17, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0.4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 1 to 4, open collector)					
Input voltage HIGH (P20, P21)	V_{IH}	2	–	16	V
Input voltage HIGH (P22, P23) AFC switched off	V_{IH}	2	–	$V_{P1}-2$	V
Input voltage LOW	V_{IL}	–0.3	–	0.8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current	I_{OL}	–	4	–	mA

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 3, 4)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2.5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current (P22 and P23 programmed HIGH)	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 6, 8)					
Maximum output voltage at $I_{load} = \pm 2.5$ mA	V_{TUN}	$V_{P3}-1.6$	–	$V_{P3}-0.4$	V
Minimum output voltage at $I_{load} = \pm 2.5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2.5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0.4	1	1.7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1.7	3.5	5.1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 10 to 13)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0.6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 15)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0.1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	16	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

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parameter	symbol	min.	typ.	max.	unit
OSC input (pin 24)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7.5	–	9.5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 1) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0.3	–	16	V
0 1	V_{VA01}	−0.3	–	0.8	V
1 0	V_{VA10}	2.5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0.3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0.3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification.
After reset has been activated, transmission may only be started after a 50 μs delay.

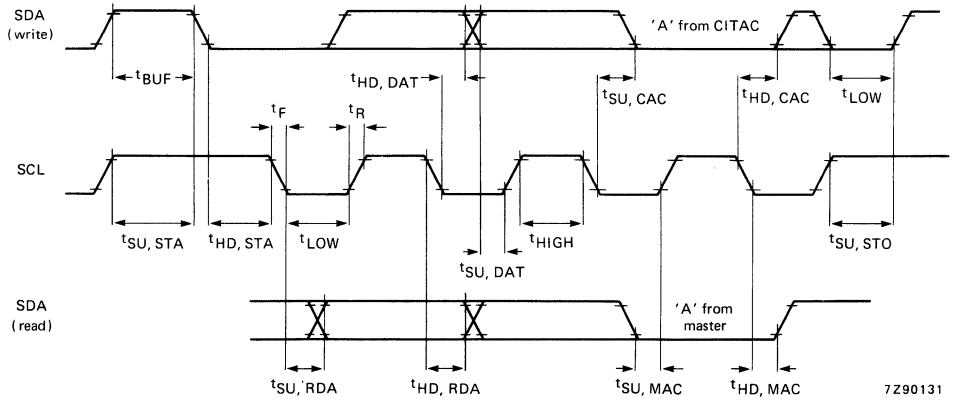


Fig. 8 I²C bus timing SAB3036.

FLL TV Tuning Circuit SAB3037

GENERAL DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without a.f.c., as required. It also controls up to 4 analogue functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bidirectional I^2C bus.

Features

- Combined analogue and digital circuitry minimizes the number of additional interfacing components required
- Frequency measurement with resolution of 50 kHz
- Selectable prescaler divisor of 64 or 256
- 32 V tuning voltage amplifier
- 4 high-current outputs for direct band selection
- 4 static digital to analogue convertors (DACs) for control of analogue functions
- Four general purpose input/output (I/O) ports
- Tuning with control of speed and direction
- Tuning with or without a.f.c.
- Single-pin, 4 MHz on-chip oscillator
- I^2C bus slave transceiver

QUICK REFERENCE DATA

Supply voltages				
(pin 13)	V_{P1}	typ.	12	V
(pin 19)	V_{P2}	typ.	13	V
(pin 14)	V_{P3}	typ.	32	V
Supply currents (no outputs loaded)				
(pin 13)	I_{P1}	typ.	30	mA
(pin 19)	I_{P2}	typ.	0.1	mA
(pin 14)	I_{P3}	typ.	0.6	mA
Total power dissipation	P_{tot}	typ.	380	mW
Operating ambient temperature range	T_{amb}	−20 to +70		°C

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

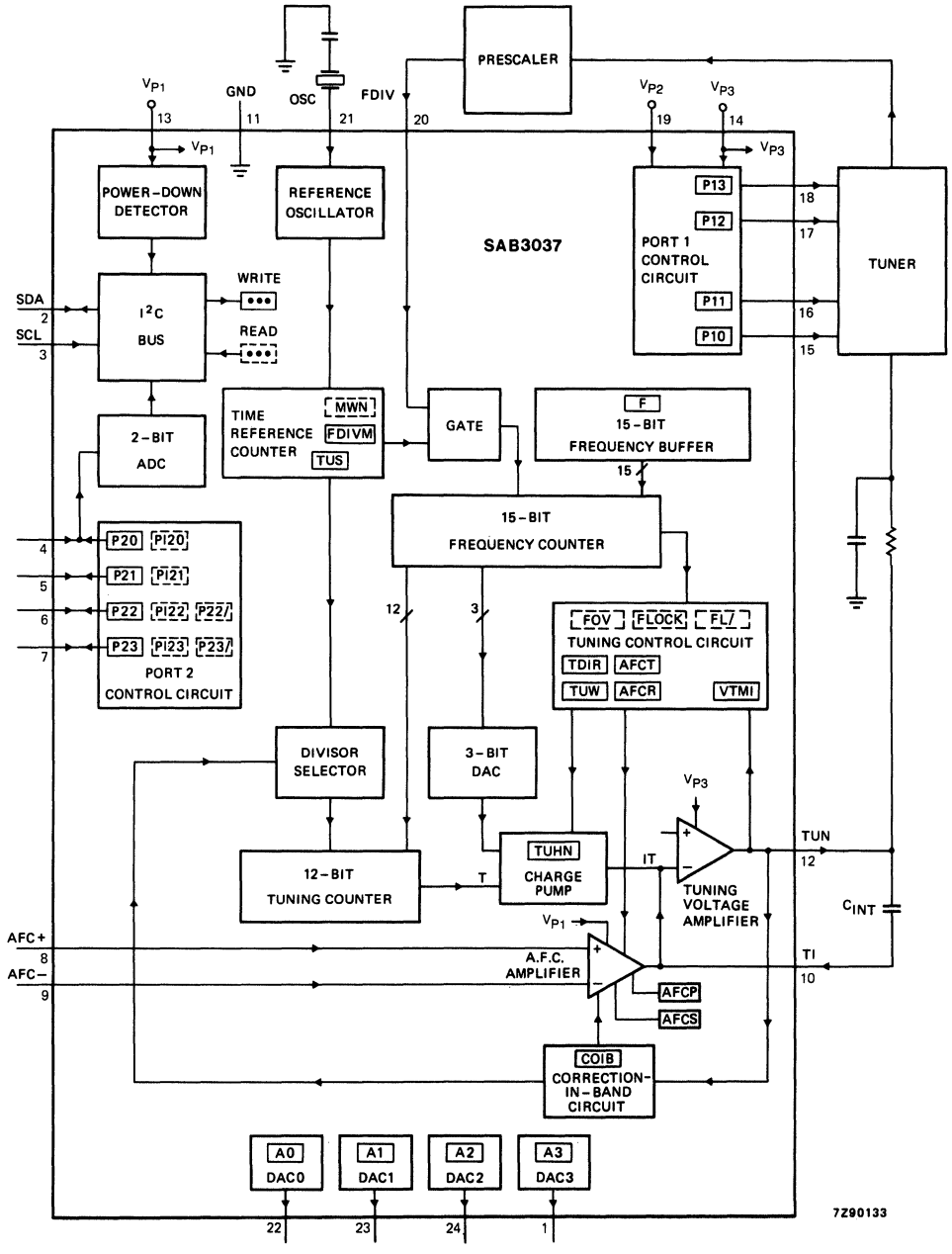


Fig. 1 Block diagram.

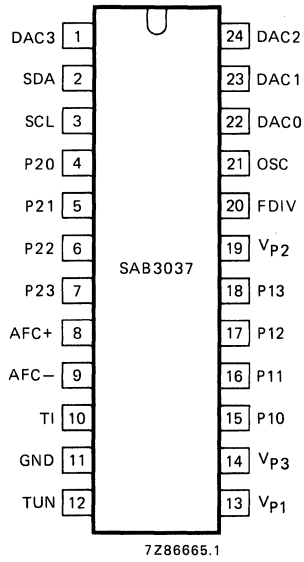


Fig. 2 Pinning diagram.

PINNING

1	DAC3	output of static DAC
2	SDA	serial data line (I²C bus)
3	SCL	serial clock line (I²C bus)
4	P20	general purpose input/output ports
5	P21	general purpose input/output ports
6	P22	general purpose input/output ports
7	P23	general purpose input/output ports
8	AFC+	a.f.c. inputs
9	AFC−	a.f.c. inputs
10	TI	tuning voltage amplifier inverting input
11	GND	ground
12	TUN	tuning voltage amplifier output
13	V_{P1}	+ 12 V supply voltage
14	V_{P3}	+ 32 V supply for tuning voltage amplifier
15	P10	high-current band-selection output ports
16	P11	high-current band-selection output ports
17	P12	high-current band-selection output ports
18	P13	high-current band-selection output ports
19	V_{P2}	positive supply for high-current band-selection output circuits
20	FDIV	input from prescaler
21	OSC	crystal oscillator input
22	DAC0	outputs of static DACs
23	DAC1	outputs of static DACs
24	DAC2	outputs of static DACs

FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50 kHz within a programmable tuning window (TUW).

The system cycles over a period of 6.4 ms (or 2.56 ms), controlled by the time reference counter which is clocked by an on-chip 4 MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50 kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1, see OPERATION), the minimum charge IT at Δf = 50 kHz equals 250 $\mu A\ \mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at Δf = 50 kHz equals $2^6 \times 2^3 \times 250\ \mu A\ \mu s$ (typical).

The maximum tuning current I is 875 μA (typical). In the tuning-hold (TUHN) mode (TUHN is active LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable a.f.c. hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, a.f.c. will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The a.f.c. has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and a.f.c. to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs P10 to P13 which are capable of sourcing up to 50 mA at a voltage drop of less than 600 mV with respect to the separate power supply input V_{P2}.

For additional digital control, four open collector I/O ports P20 to P23 are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analogue converters DAC0 to DAC3 are provided for analogue control.

Reset

CITAC goes into the power-down-reset mode when V_{P1} is below 8.5 V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus; the I^2C bus is specified in our data handbook "ICs for digital systems in radio, audio, and video equipment". For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Fig. 3.

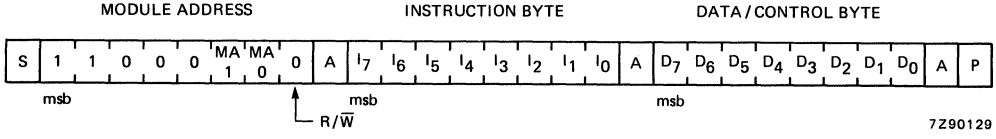


Fig. 3 I^2C bus write format.

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down-reset mode ($V_{P1} > 8.5$ V (typical)).

Table 1 Valid module addresses

MA1	MA0	P20
0	0	don't care
0	1	GND
1	0	$\frac{1}{2}V_{P1}$
1	1	V_{P1}

OPERATION (continued)

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Fig. 4.

	INSTRUCTION BYTE								DATA/CONTROL BYTE							
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
freq.	1	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
TCD0	0	0	1	0	1	0	0	1	AFCT	VTMI0	AFCR1	AFCR0	TUHN1	TUHN0	TUW1	TUW0
TCD1	0	0	1	0	1	0	1	0	VTMI1	COIB1	COIB0	AFCS1	AFCS0	TUS2	TUS1	TUS0
TCD2	0	0	1	0	1	0	1	1	0	0	0	0	AFCP	FDIVM	TDIRD	TDIRU

7Z90125

Fig. 4 Tuning control format.

Frequency

Frequency is set when bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50 kHz. All frequency bits are set to logic 1 at reset.

Tuning hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50 kHz) into the tuning amplifier.

Table 2 Tuning current control

TUHN1	TUHN0	typ. I_{max} μA	typ. IT_{min} $\mu A\ \mu s$	typ. ΔV_{TUNmin} at C_{INT} = 1 μF μV
0	0	3.5*	1*	1*
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

* Values after reset.

During tuning but before lock-in, the highest current value should be selected.
After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (max. 5 nA). However it is good practice to program the lowest current value during tuner band switching.

Tuning sensitivity

To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50 kHz; TUHN0 and TUHN1 = logic 1.

8

Table 3 Minimum charge IT as a function of TUS

Δf = 50 kHz; TUHN0 = logic 1; TUHN1 = logic 1

TUS2	TUS1	TUS0	typ. IT_{min} mA μs	typ. ΔV_{TUNmin} at C_{INT} = 1 μF mV
0	0	0	0.25*	0.25*
0	0	1	0.5	0.5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

* Values after reset.

Correction-in-band

This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

Table 4 Programming correction-in-band

COIB1	COIB0	charge multiplying factors at typical values of V_{TUN} at:			
		< 12 V	12 to 18 V	18 to 24 V	> 24 V
0	0	1*	1*	1*	1*
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

* Values after reset.

The transconductance multiplying factor of the a.f.c. amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning window

Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation $|\Delta f|$ between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If $|\Delta f|$ is up to 50 kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

Table 5 Tuning window programming

TUW1	TUW0	$\|\Delta f\|$ (kHz)	tuning window (kHz)
0	0	0*	0*
0	1	50	100
1	0	150	300

* Values after reset.

OPERATION (continued)

A.F.C.

When AFCT is set to logic 1 it will not be cleared and the a.f.c. will remain on as long as $|\Delta f|$ is less than the value programmed for the a.f.c. hold range AFCR (see Table 6). It is possible for the a.f.c. to remain on for values of up to 50 kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Table 6 A.F.C. hold range programming

AFCR1	AFCR0	$\|\Delta f\|$ (kHz)	a.f.c. hold range (kHz)
0	0	0*	0*
0	1	350	700
1	0	750	1500

* Values after reset.

Transconductance

The transconductance (g) of the a.f.c. amplifier is programmed via the a.f.c. sensitivity bits AFCS as shown in Table 7.

Table 7 Transconductance programming

AFCS1	AFCS0	typ. transconductance (μA/V)
0	0	0.25*
0	1	25
1	0	50
1	1	100

* Value after reset.

A.F.C. polarity

If a positive differential input voltage is applied to the (switched on) a.f.c. amplifier, the tuning voltage V_{TUN} falls when the a.f.c. polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum tuning voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in CHARACTERISTICS.

Frequency measuring window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Table 8 Frequency measuring window programming

FDIVM	prescaler division factor	cycle period (ms)	measuring window (ms)
0	256	6.4*	5.12*
1	64	2.56	1.28

* Values after reset.

Tuning direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analogue converter control) are shown in Fig. 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes HIGH. All outputs are LOW after reset.

P23, P22, P21, P20 — Open collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analogue converters. The digital-to-analogue converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

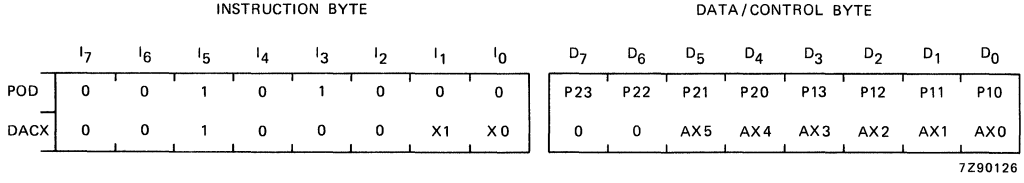


Fig. 5 Control programming.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master the slave (CITAC) stops transmitting. The format of the information bytes is shown in Fig. 6.

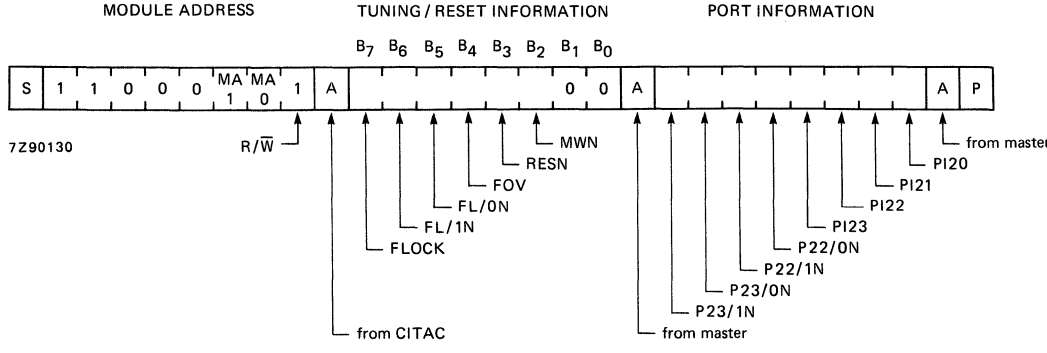


Fig. 6 Information byte format.

OPERATION (continued)

Tuning/reset information bits

FLOCK	Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.
FL/1N	Set to logic 0 (active LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.
FL/0N	As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.
FOV	Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.
RESN	Set to logic 0 (active LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.
MWN	MWN (frequency measuring window, active LOW) is at logic 1 for a period of 1.28 ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured. When slightly different frequencies are programmed repeatedly and a.f.c. is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port information bits

P23/1N, P22/1N	Set to logic 0 (active LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22 respectively. Both are reset to logic 1 after the port information has been read.
P23/0N, P22/0N	As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.
PI23, PI22, PI21, PI20	Indicate input voltage levels at P23, P22, P21 and P20 respectively. A logic 1 indicates a HIGH input level.

8

Reset

The programming to reset all registers is shown in Fig. 7. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down-reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

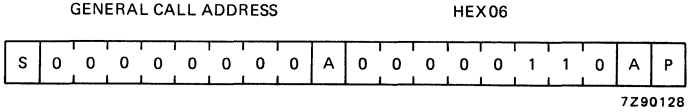


Fig. 7 Reset programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges:			
(pin 13)	V_{P1}	−0.3 to +18	V
(pin 19)	V_{P2}	−0.3 to +18	V
(pin 14)	V_{P3}	−0.3 to +36	V
Input/output voltage ranges:			
(pin 2)	V_{SDA}	−0.3 to +18	V
(pin 3)	V_{SCL}	−0.3 to +18	V
(pins 4 to 7)	V_{P2X}	−0.3 to +18	V
(pins 8 and 9)	$V_{AFC+,AFC-}$	−0.3 to V_{P1}*	V
(pin 10)	V_{TI}	−0.3 to V_{P1}*	V
(pin 12)	V_{TUN}	−0.3 to V_{P3}*	V
(pins 15 to 18)	V_{P1X}	−0.3 to V_{P2}**	V
(pin 20)	V_{FDIV}	−0.3 to V_{P1}*	V
(pin 21)	V_{OSC}	−0.3 to +5	V
(pins 1 and 22 to 24)	V_{DACX}	−0.3 to V_{P1}*	V
Total power dissipation	P_{tot}	max. 1000	mW
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−20 to +70	°C

CHARACTERISTICS

T_{amb} = 25 °C; V_{P1}, V_{P2}, V_{P3} at typical voltages, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages	V_{P1}	10.5	12	13.5	V
	V_{P2}	4.7	13	16	V
	V_{P3}	30	32	35	V
Supply currents (no outputs loaded)	I_{P1}	18	30	45	mA
	I_{P2}	0	–	0.1	mA
	I_{P3}	0.2	0.6	2	mA
Additional supply currents (A)	I_{P2A}	−2	–	I_{OHP1X}	mA
(note 1)	I_{P3A}	0.2	–	2	mA
Total power dissipation	P_{tot}	–	380	–	mW
Operating ambient temperature	T_{amb}	−20	–	+70	°C
I²C bus inputs/outputs					
SDA input (pin 2); SCL input (pin 3)					
Input voltage HIGH (note 2)	V_{IH}	3	–	$V_{P1}-1$	V
Input voltage LOW	V_{IL}	−0.3	–	1.5	V
Input current HIGH (note 2)	I_{IH}	–	–	10	μA
Input current LOW (note 2)	I_{IL}	–	–	10	μA
SDA output (pin 2, open collector)					
Output voltage LOW at I_{OL} = 3 mA	V_{OL}	–	–	0.4	V
Maximum output sink current	I_{OL}	–	5	–	mA
Open collector I/O ports					
P20, P21, P22, P23 (pins 4 to 7, open collector)					
Input voltage HIGH	V_{IH}	2	–	16	V
Input voltage LOW	V_{IL}	−0.3	–	0.8	V
Input current HIGH	I_{IH}	–	–	25	μA
Input current LOW	$-I_{IL}$	–	–	25	μA
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output sink current	I_{OL}	–	4	–	mA

8

parameter	symbol	min.	typ.	max.	unit
A.F.C. amplifier					
Inputs AFC+, AFC– (pins 8, 9)					
Transconductance for input voltages up to 1 V differential:					
AFCS1 AFCS2					
0 0	g_{00}	100	250	800	nA/V
0 1	g_{01}	15	25	35	μA/V
1 0	g_{10}	30	50	70	μA/V
1 1	g_{11}	60	100	140	μA/V
Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	ΔM_g	–20	–	+20	%
Input offset voltage	V_{Ioff}	–75	–	+75	mV
Common mode input voltage	V_{com}	3	–	$V_{P1}-2.5$	V
Common mode rejection ratio	CMRR	–	50	–	dB
Power supply (V_{P1}) rejection ratio	PSRR	–	50	–	dB
Input current	I_I	–	–	500	nA
Tuning voltage amplifier					
Input TI, output TUN (pins 10, 12)					
Maximum output voltage at $I_{load} = \pm 2.5$ mA	V_{TUN}	$V_{P3}-1.6$	–	$V_{P3}-0.4$	V
Minimum output voltage at $I_{load} = \pm 2.5$ mA:					
VTMI1 VTMI0					
0 0	V_{TM00}	300	–	500	mV
1 0	V_{TM10}	450	–	650	mV
1 1	V_{TM11}	650	–	900	mV
Maximum output source current	$-I_{TUNH}$	2.5	–	8	mA
Maximum output sink current	I_{TUNL}	–	40	–	mA
Input bias current	I_{TI}	–5	–	+5	nA
Power supply (V_{P3}) rejection ratio	PSRR	–	60	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuning voltage amplifier (continued)					
Minimum charge IT to tuning voltage amplifier					
TUHN1 TUHN0					
0 0	CH_{00}	0.4	1	1.7	μA μs
0 1	CH_{01}	4	8	14	μA μs
1 0	CH_{10}	15	30	48	μA μs
1 1	CH_{11}	130	250	370	μA μs
Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	ΔCH	−20	–	+20	%
Maximum current I into tuning amplifier					
TUHN1 TUHN0					
0 0	I_{T00}	1.7	3.5	5.1	μA
0 1	I_{T01}	15	29	41	μA
1 0	I_{T10}	65	110	160	μA
1 1	I_{T11}	530	875	1220	μA
Correction-in-band					
Tolerance of correction-in-band levels 12 V, 18 V and 24 V	ΔV_{CIB}	−15	–	+15	%
Band-select output ports					
P10, P11, P12, P13 (pins 15 to 18)					
Output voltage HIGH at $-I_{OH}$ = 50 mA (note 3)	V_{OH}	V_{P2}−0.6	–	–	V
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
Maximum output source current (note 3)	$-I_{OH}$	–	130	200	mA
Maximum output sink current	I_{OL}	–	5	–	mA
FDIV input (pin 20)					
Input voltage (peak-to-peak value) (t_{rise} and $t_{fall} \leqslant 40$ ns)	$V_{FDIV(p-p)}$	0.1	–	2	V
Duty cycle	–	40	–	60	%
Maximum input frequency	f_{max}	14.5	–	–	MHz
Input impedance	Z_i	–	8	–	kΩ
Input capacitance	C_i	–	5	–	pF

8

parameter	symbol	min.	typ.	max.	unit
OSC input (pin 21)					
Crystal resistance at resonance (4 MHz)	R_X	–	–	150	Ω
DAC outputs 0 to 3 (pins 22 to 24 and pin 1)					
Maximum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DH}	10	–	11.5	V
Minimum output voltage (no load) at V_{P1} = 12 V (note 4)	V_{DL}	0.1	–	1	V
Positive value of smallest step (1 least-significant bit)	ΔV_D	0	–	350	mV
Deviation from linearity	–	–	–	0.5	V
Output impedance at $I_{load} = \pm 2$ mA	Z_o	–	–	70	Ω
Maximum output source current	$-I_{DH}$	–	–	6	mA
Maximum output sink current	I_{DL}	–	8	–	mA
Power-down-reset					
Maximum supply voltage V_{P1} at which power-down-reset is active	V_{PD}	7.5	–	9.5	V
V_{P1} rise-time during power-up (up to V_{PD})	t_r	5	–	–	μs
Voltage level for valid module address					
Voltage level at P20 (pin 4) for valid module address as a function of MA1, MA0					
MA1 MA0					
0 0	V_{VA00}	−0.3	–	16	V
0 1	V_{VA01}	−0.3	–	0.8	V
1 0	V_{VA10}	2.5	–	$V_{P1}-2$	V
1 1	V_{VA11}	$V_{P1}-0.3$	–	V_{P1}	V

Notes to the characteristics

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{P2} and I_{P3} respectively.
2. If $V_{P1} < 1$ V, the input current is limited to 10 μA at input voltages up to 16 V.
3. At continuous operation the output current should not exceed 50 mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{P1}.

I²C BUS TIMING (Fig. 8)

I²C bus load conditions are as follows:
4 kΩ pull-up resistor to +5 V; 200 pF capacitor to GND.

All values are referred to V_{IH} = 3 V and V_{IL} = 1.5 V.

parameter	symbol	min.	typ.	max.	unit
Bus free before start	t_{BUF}	4	–	–	μs
Start condition set-up time	$t_{SU,STA}$	4	–	–	μs
Start condition hold time	$t_{HD,STA}$	4	–	–	μs
SCL, SDA LOW period	t_{LOW}	4	–	–	μs
SCL HIGH period	t_{HIGH}	4	–	–	μs
SCL, SDA rise time	t_R	–	–	1	μs
SCL, SDA fall time	t_F	–	–	0.3	μs
Data set-up time (write)	$t_{SU,DAT}$	1	–	–	μs
Data hold time (write)	$t_{HD,DAT}$	1	–	–	μs
Acknowledge (from CITAC) set-up time	$t_{SU,CAC}$	–	–	2	μs
Acknowledge (from CITAC) hold time	$t_{HD,CAC}$	0	–	–	μs
Stop condition set-up time	$t_{SU,STO}$	4	–	–	μs
Data set-up time (read)	$t_{SU,RDA}$	–	–	2	μs
Data hold time (read)	$t_{HD,RDA}$	0	–	–	μs
Acknowledge (from master) set-up time	$t_{SU,MAC}$	1	–	–	μs
Acknowledge (from master) hold time	$t_{HD,MAC}$	2	–	–	μs

Note

Timings $t_{SU,DAT}$ and $t_{HD,DAT}$ deviate from the I²C bus specification .
After reset has been activated, transmission may only be started after a 50 μs delay.

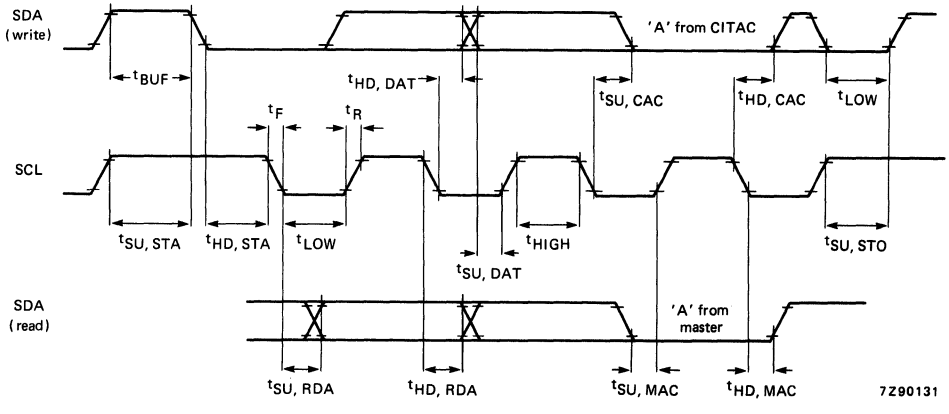


Fig. 8 I²C bus timing SAB3037.

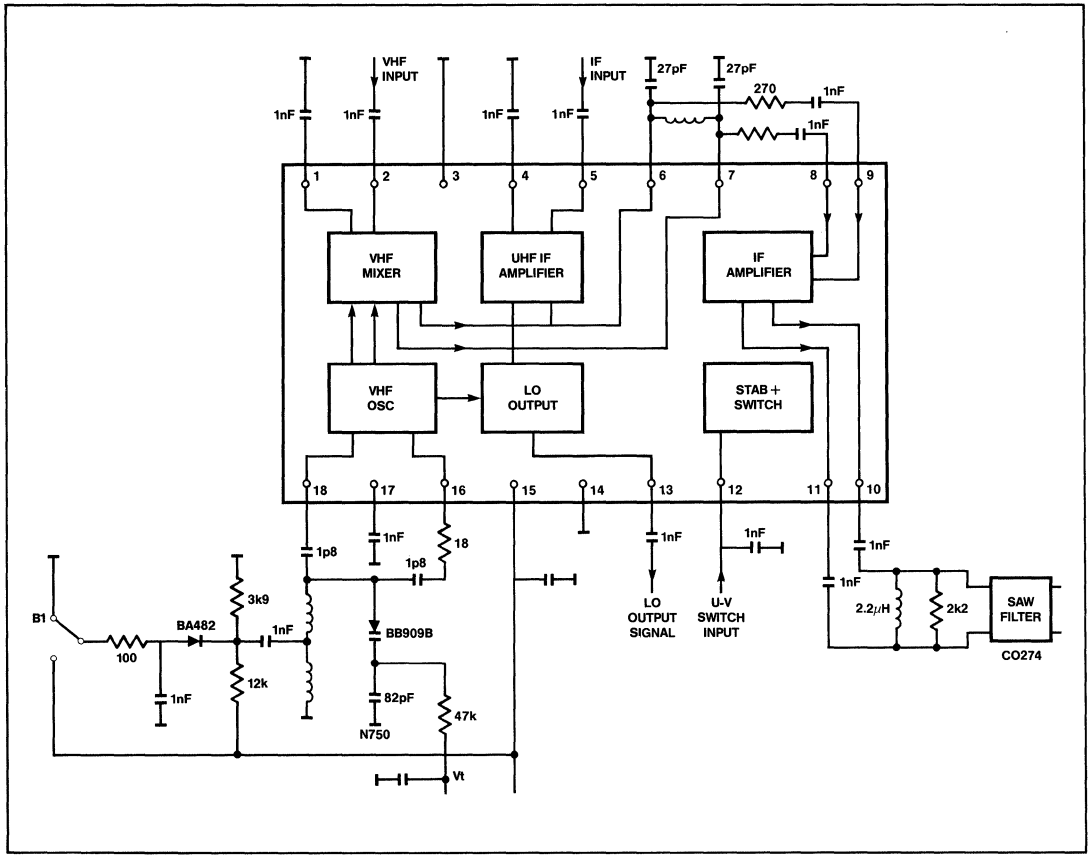
VHF Mixer-Oscillator TDA5030

DESCRIPTION
The TDA5030T is a monolithic IC for the VHF mixer/oscillator function in TV tuners.

FEATURES
- Balanced mixer
- Amplitude controlled oscillator
- SAW filter preamplifier
- UHF IF preamplifier
- Buffered stage for drive of a prescaler with the oscillator signal
- Voltage stabilizer
- U-V switching circuit

APPLICATIONS
- Mixer/oscillator
- RF receiver
- Tuners
- CATV

BLOCK DIAGRAM



CMOS Frequency Synthesizer (LOPSY) — TDD1742T

DESCRIPTION

The TDD1742T is an oxide-isolated CMOS (LOCMOS) circuit designed specifically for Low Power Frequency Synthesizer applications, especially for VHF and UHF portables.

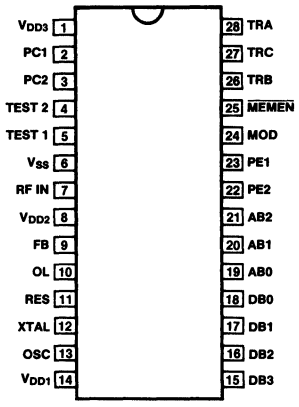
FEATURES

- **Single chip with on-board sample and hold capacitor**
- **Low power requirements**
- **High performance phase comparator with low phase noise and spurious response**
- **Auxiliary digital phase comparator for fast locking**
- **On-board phase modulator**
- **Simple interface to memory**
- **Microprocessor controllable**
- **Power-on reset circuitry**

APPLICATIONS

- **Frequency synthesizers**
- **Radio/TV LO circuit**

PIN CONFIGURATION



TOP VIEW

CD01350S

PIN	SYMBOL	FUNCTION
1	V_{DD3}	Main power supply; +7 to +10V
2	PC1	High-gain phase comparator (analogue)
3	PC2	Low-gain phase comparator (digital)
4	Test 2	Not connected
5	Test 1	Not connected
6	V_{SS}	Positive power supply
7	RF IN	RF input
8	V_{DD2}	Power supply for TTL-compatible stages; +5V ± 10%
9	FB	Feedback to pre-scaler
10	OL	Out-of-lock indication
11	RES	Power-on-reset
12	XTAL	Reference oscillator/buffer output
13	OSC	Reference oscillator/buffer input
14	V_{DD1}	Main power supply; +7 to +10V
15	DB3	Data bus inputs
16	DB2	Data bus inputs
17	DB1	Data bus inputs
18	DB0	Data bus inputs
19	AB0	Address bus
20	AB1	Address bus
21	AB2	Address bus
22	PE2	Program enable 2
23	PE1	Program enable 1
24	MOD	Phase modulation input
25	$\overline{\text{MEMEN}}$	Memory enable
26	TRB	Bias resistor R_B
27	TRC	Bias resistor R_C
28	TRA	Bias resistor R_A

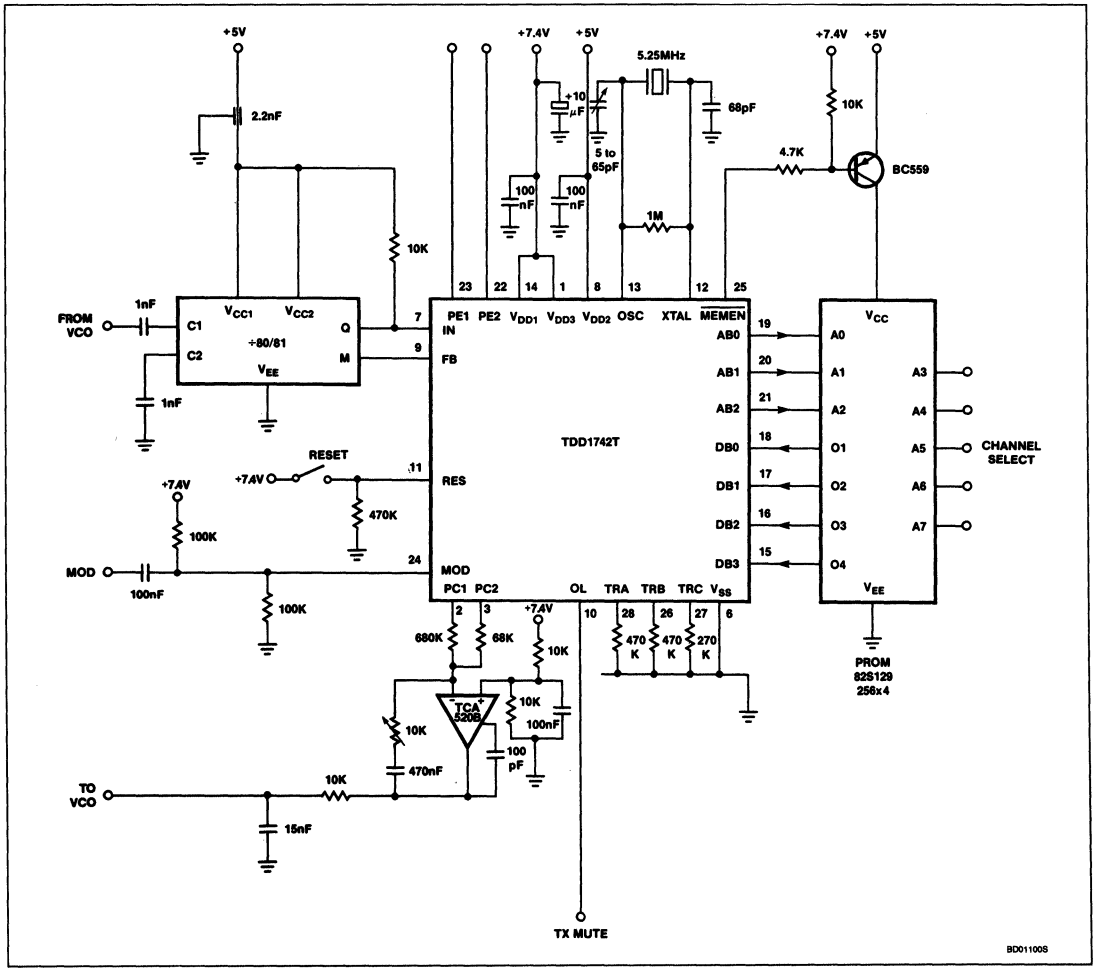
8

CMOS Frequency Synthesizer (Lopsy) TDD1742T

REFERENCE DATA

PARAMETER Operating supply voltages (referenced to V_{SS} = 0V, GND)	LIMITS		UNIT
	Min	Max	
V_{DD1}	7.0	10.0	V
V_{DD2}	4.5	5.0	V
V_{DD3}	7.0	10.0	V
I_{DD1} (modulator off)		3.0	mA
I_{DD2}		100.0	=mμA

BLOCK DIAGRAM



Video I.F./AFT TDA2540

The TDA2540 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using n-p-n tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit with noise gating
- tuner a.g.c. output (n-p-n tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal

QUICK REFERENCE DATA

Supply voltage	V_{11-13}	typ.	12 V
Supply current	I_{11}	typ.	50 mA
I.F. input voltage at f = 38.9 MHz (r.m.s. value)	$V_{1-16\ (rms)}$	typ.	100 μV
Video output voltage (white at 10% of top sync)	$V_{12(p-p)}$	typ.	2.7 V
I.F. voltage gain control range	G_v	typ.	64 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58 dB
A.F.C. output voltage swing for Δf = 100 kHz	ΔV_{5-13}	typ.	10 V

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PACKAGE OUTLINES

TDA2540 : 16-lead DIL; plastic (SOT-38).
TDA2540Q: 16-lead QIL; plastic (SOT-58).

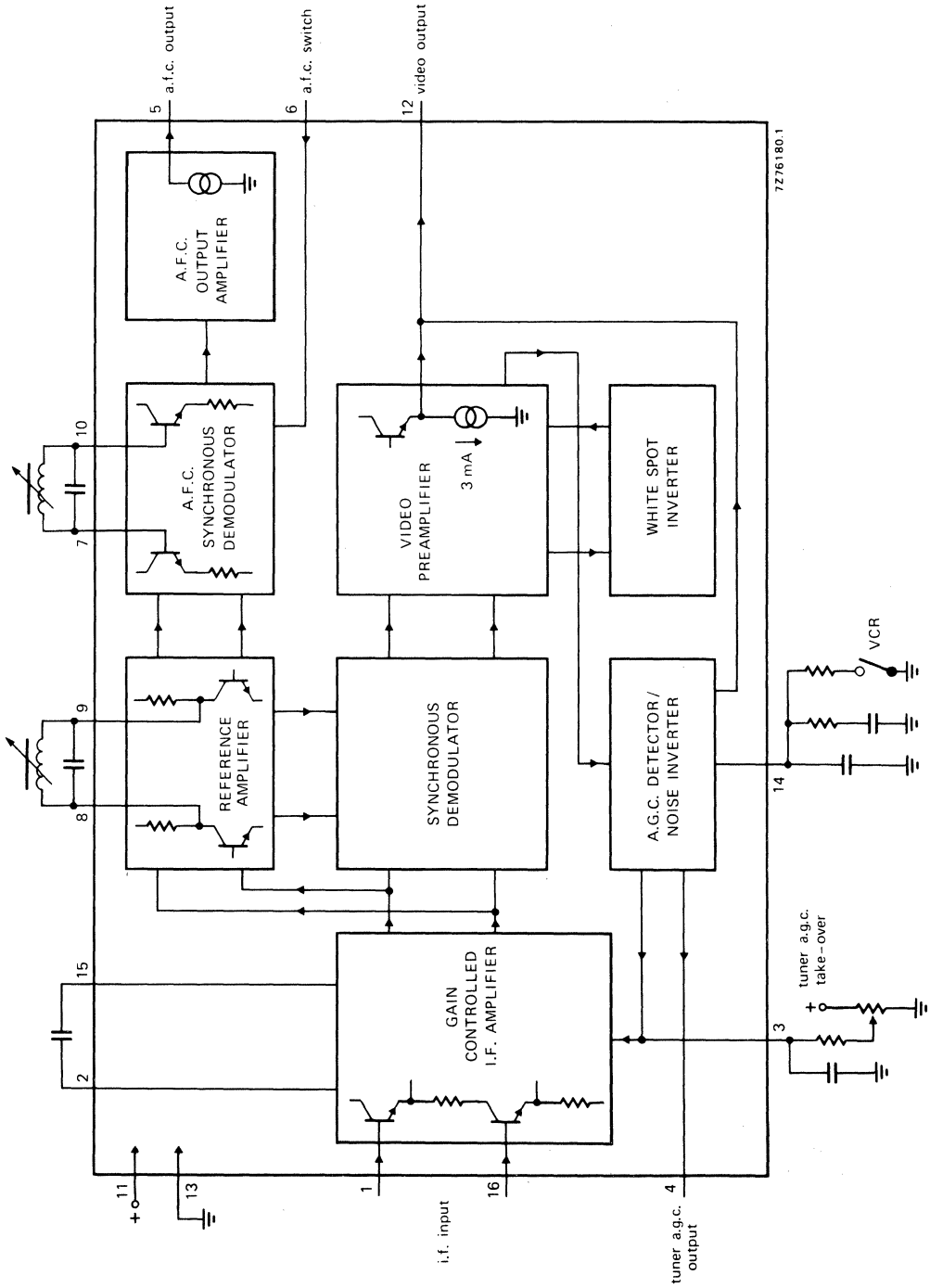


Fig. 1 Block diagram.

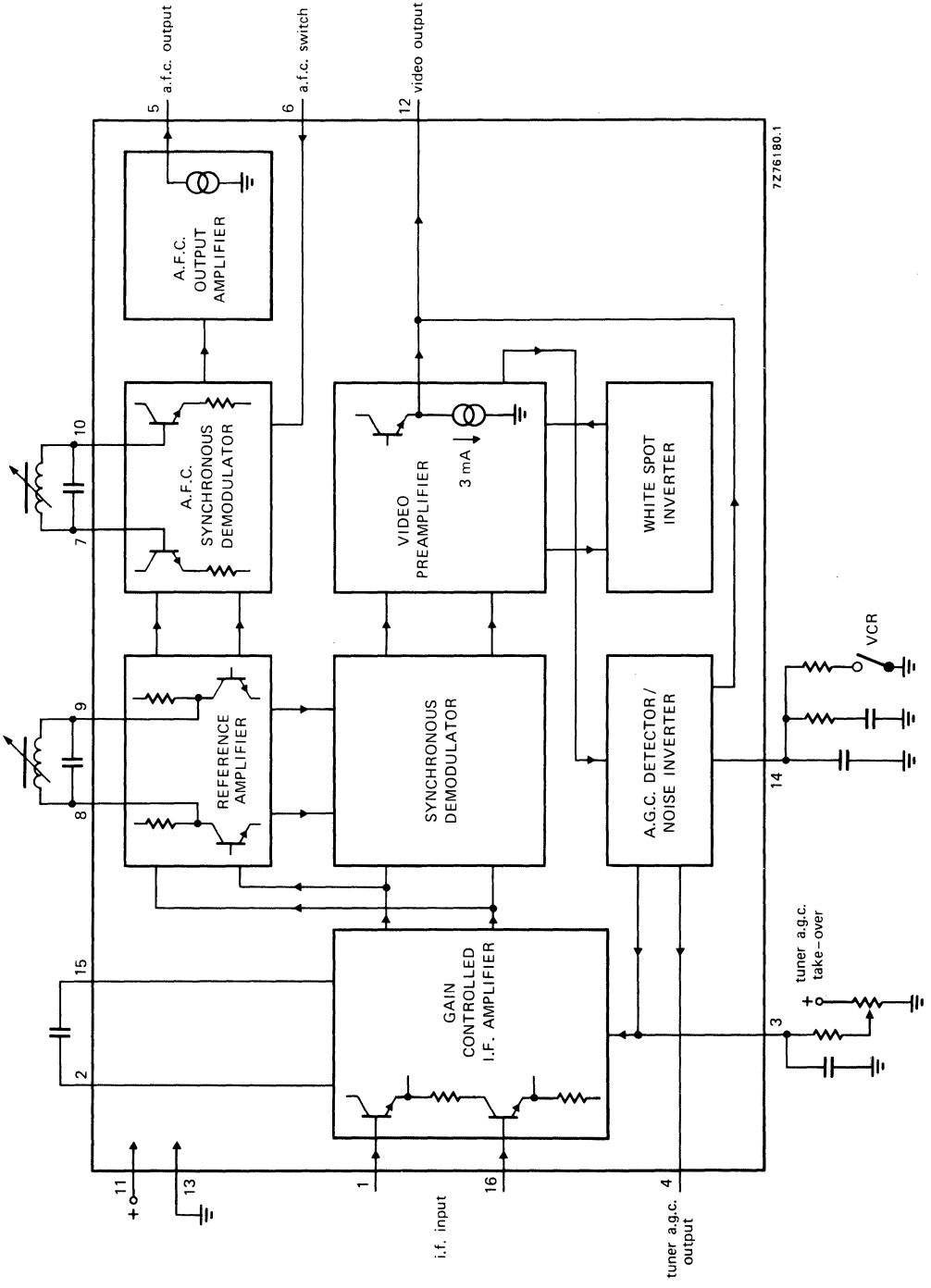


Fig. 1 Block diagram.

8

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{11-13}	max.	13.2	V
Tuner a.g.c. voltage	V_{4-13}	max.	12	V
Total power dissipation	P_{tot}	max.	900	mW
Storage temperature	T_{stg}		−55 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 60	°C

CHARACTERISTICS (measured in Fig. 5)

Supply voltage range	V_{11-13}	typ.	12	V
			10.2 to 13.2	V

The following characteristics are measured at T_{amb} = 25 °C; V_{11-13} = 12 V; f = 38.9 MHz

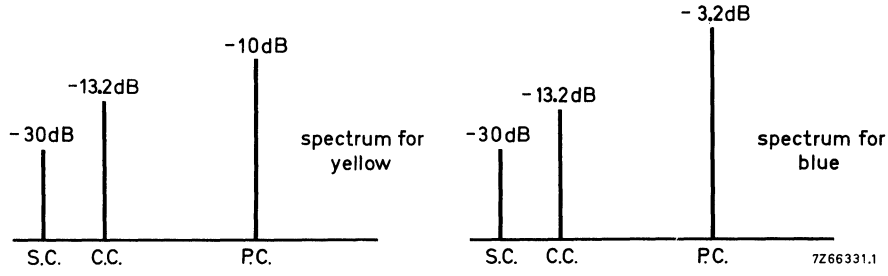
I.F. input voltage for onset of a.g.c. (r.m.s. value)	$V_{1-16(rms)}$	typ.	100	μV
		<	150	μV
Differential input impedance	$\lvert Z_{1-16} \rvert$	typ.	2 kΩ in parallel with 2 pF	
Zero-signal output level	V_{12-13}	typ.	6 ± 0.3	V*
Top sync output level	V_{12-13}	typ.	3.07	V
			2.9 to 3.2	V
I.F. voltage gain control range	G_V	typ.	64	dB
Bandwidth of video amplifier (3 dB)	B	typ.	6	MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB**
Differential gain	dG	typ.	4	%
		<	10	%
Differential phase	$d\varphi$	typ.	2°	
		<	10°	

* So-called 'projected zero point', e.g. with switched demodulator.

** $S/N = \dfrac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.

CHARACTERISTICS (continued)

Intermodulation at 1.1 MHz: blue*	>	46 dB
	typ.	60 dB
yellow*	>	46 dB
	typ.	50 dB
at 3.3 MHz**	>	46 dB
	typ.	54 dB



S.C.: sound carrier level
C.C.: chrominance carrier level
P.C.: picture carrier level
} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

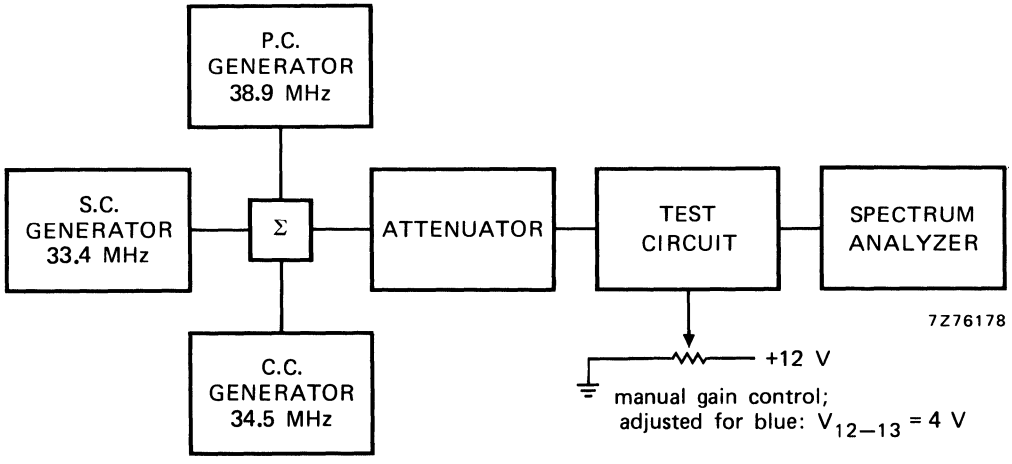


Fig. 3 Test set-up for intermodulation.

* $20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6$ dB. ** $20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$.

Carrier signal at video output		typ. <	4 mV 30 mV
2nd harmonic of carrier at video output		typ. <	20 mV 30 mV
White spot inverter threshold level (Fig. 4)		typ.	6.6 V
White spot insertion level (Fig. 4)		typ.	4.7 V
Noise inverter threshold level (Fig. 4)		typ.	1.8 V
Noise insertion level (Fig. 4)		typ.	3.8 V
External video switch (VCR) switches off the output at:	V_{14-13}	<	1.1 V

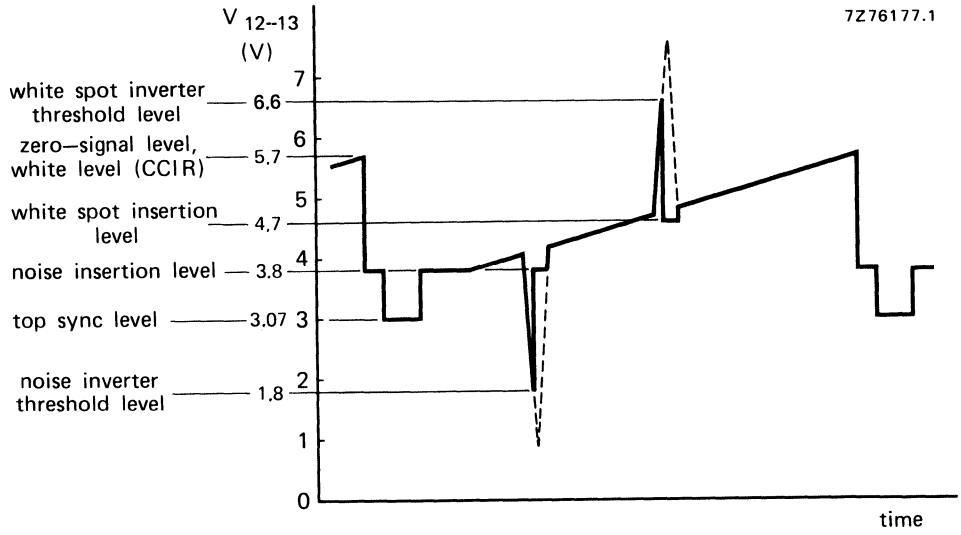


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		10 to 0 mA
Tuner a.g.c. output voltage at I_4 = 10 mA	V_{4-13}	<	0.3 V
Tuner a.g.c. output leakage current V_{14-13} = 5 V; V_{4-13} = 12 V	I_4	<	15 µA
Maximum a.f.c. output voltage swing	ΔV_{5-13}	> typ.	10 V 11 V
Detuning for a.f.c. output voltage swing of 10 V	Δf	tvp. <	100 kHz 200 kHz
A.F.C. zero-signal output voltage (minimum gain)	V_{5-13}	typ.	6 V 4 to 8 V
A.F.C. switches on at:	V_{6-13}	>	3.2 V
A.F.C. switches off at:	V_{6-13}	<	1.5 V

APPLICATION INFORMATION

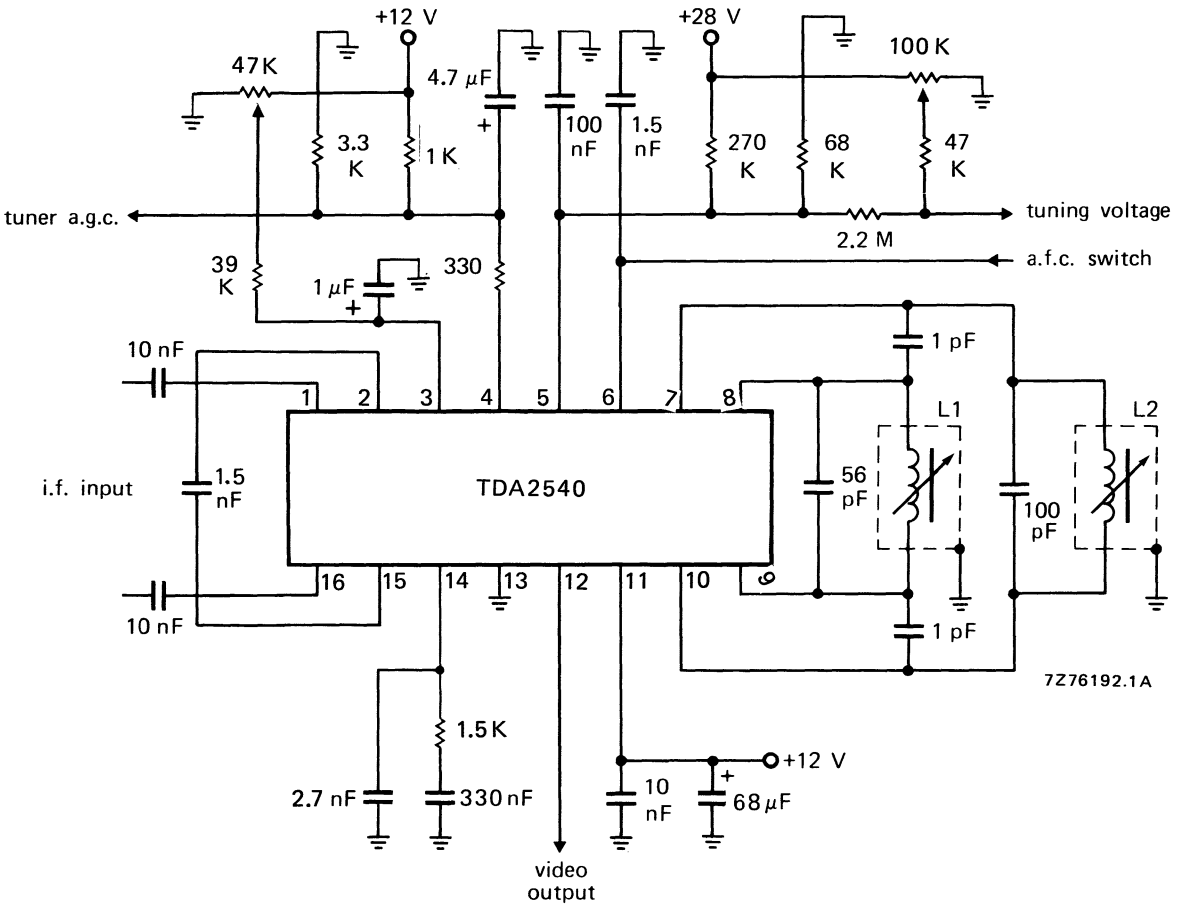


Fig. 5 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f = 38,9 MHz.

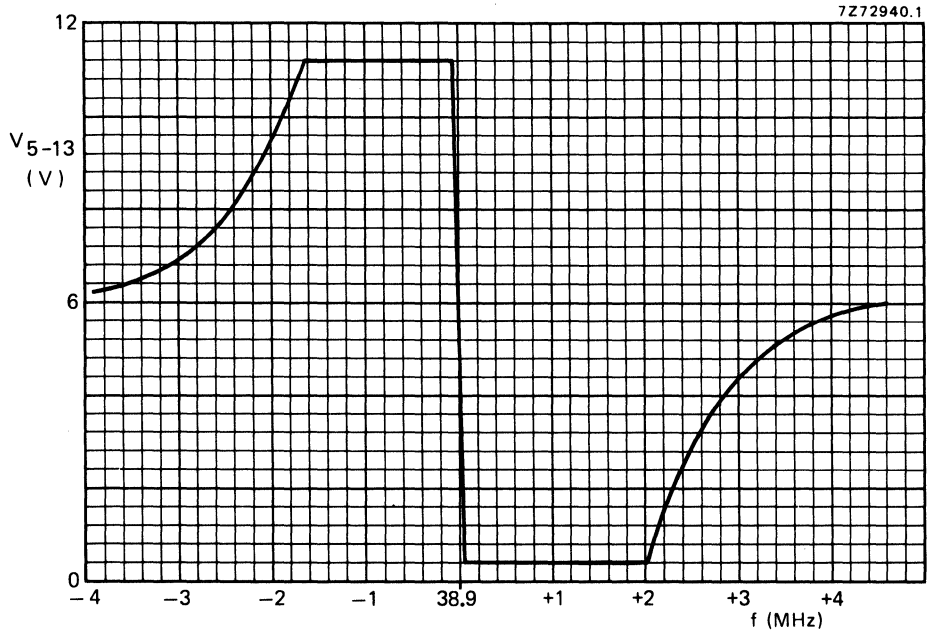


Fig. 6 A.F.C. output voltage (V_{5-13}) as a function of the frequency.

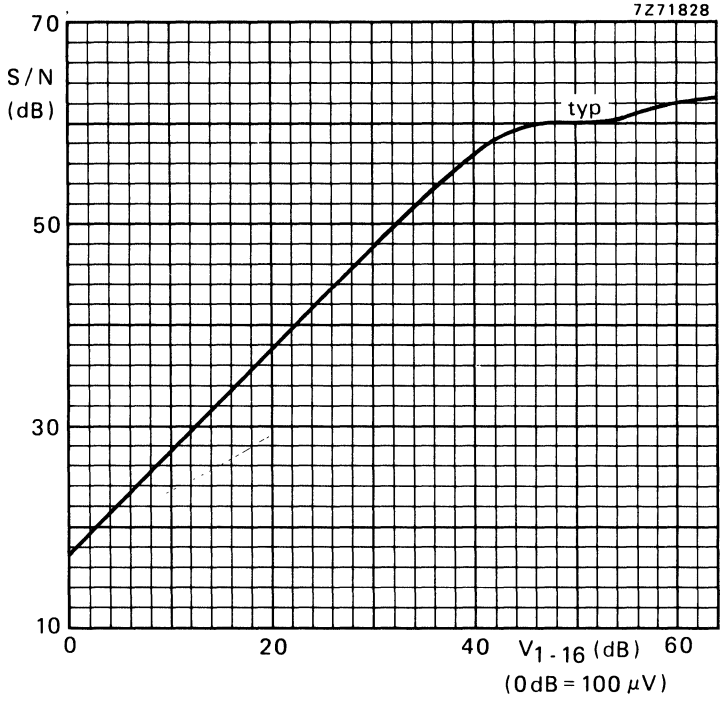


Fig. 7 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

The TDA2541 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using p-n-p tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit with noise gating
- tuner a.g.c. output (p-n-p tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal.

QUICK REFERENCE DATA

Supply voltage	$V_{11\text{-}13}$	typ.	12 V
Supply current	I_{11}	typ.	50 mA
I.F. input voltage at f = 38.9 MHz (r.m.s. value)	$V_{1\text{-}16(rms)}$	typ.	100 μV
Video output voltage (white at 10% of top sync)	$V_{12(p\text{-}p)}$	typ.	2.7 V
I.F. voltage gain control range	G_v	typ.	64 dB
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58 dB
A.F.C. output voltage swing for Δf = 100 kHz	$\Delta V_{5\text{-}13}$	typ.	10 V

PACKAGE OUTLINES

TDA2541 : 16-lead DIL; plastic (SOT-38).
TDA2541Q: 16-lead QIL; plastic (SOT-58).

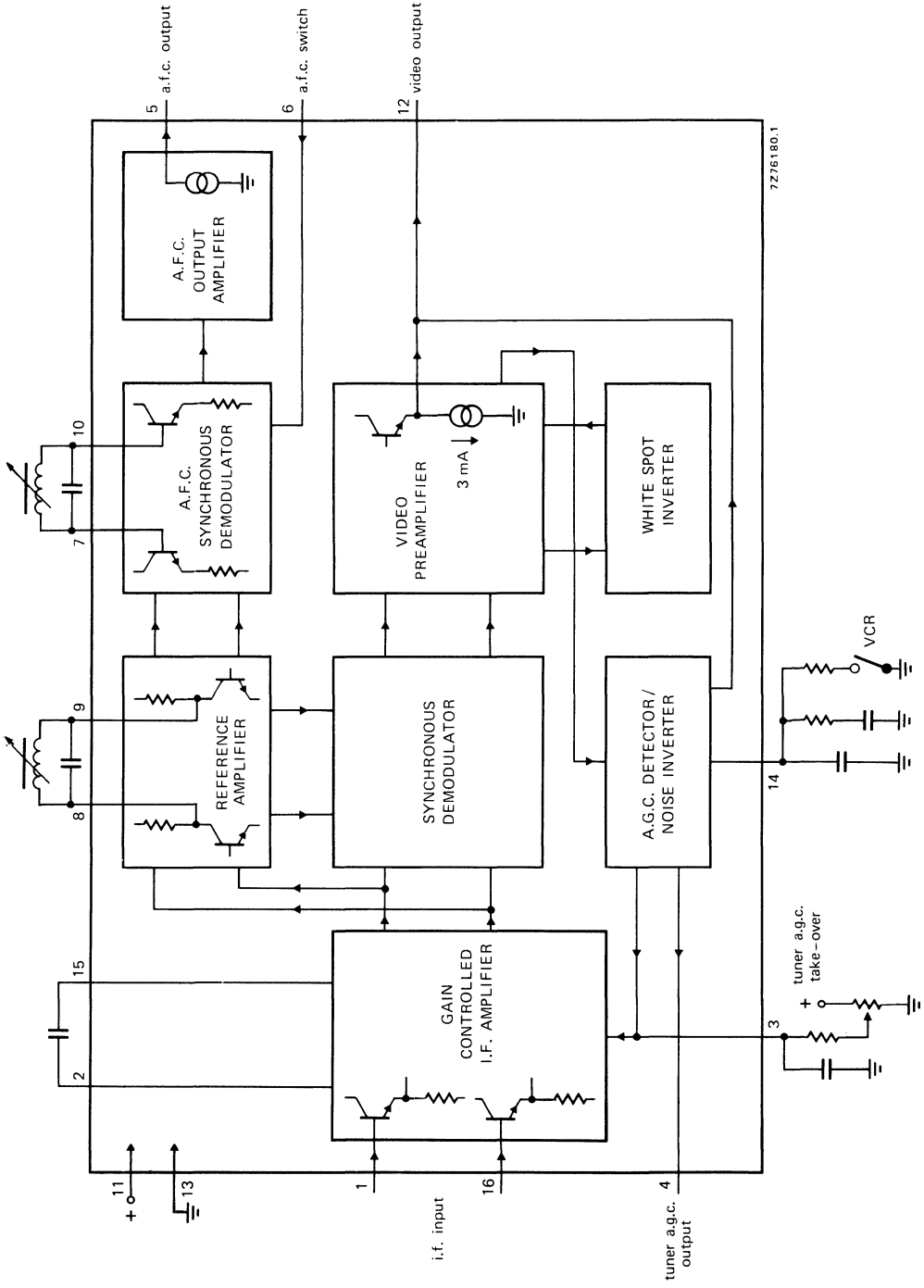


Fig. 1 Block diagram.

8

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{11-13}	max.	13.2	V
Tuner a.g.c. voltage	V_{4-13}	max.	12	V
Total power dissipation	P_{tot}	max.	900	mW
Storage temperature	T_{stg}		−55 to + 125	°C
Operating ambient temperature	T_{amb}		−25 to + 60	°C

CHARACTERISTICS (measured in Fig. 5)

Supply voltage range	V_{11-13}	typ.	12	V
			10.2 to 13.2	V

The following characteristics are measured at T_{amb} = 25 °C; V_{11-13} = 12 V; f = 38.9 MHz

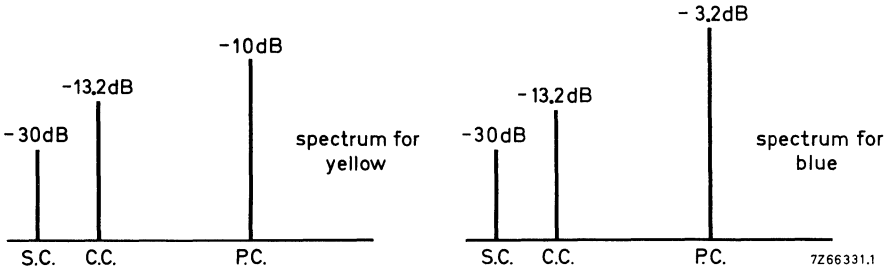
I.F. input voltage for onset of a.g.c. (r.m.s. value)	$V_{1-16(rms)}$	typ.	100	μV
		<	150	μV
Differential input impedance	$\lvert Z_{1-16} \rvert$	typ.	2 kΩ in parallel with 2 pF	
Zero-signal output level	V_{12-13}	typ.	6 ± 0.3	V*
Top sync output level	V_{12-13}	typ.	3.07	V
			2.9 to 3.2	V
I.F. voltage gain control range	G_v	typ.	64	dB
Bandwidth of video amplifier (3 dB)	B	typ.	6	MHz
Signal-to-noise ratio at V_i = 10 mV	S/N	typ.	58	dB**
Differential gain	dG	typ.	4	%
		<	10	%
Differential phase	dφ	typ.	2°	
		<	10°	

* So-called 'projected zero point', e.g. with switched demodulator.

** $$S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$

CHARACTERISTICS (continued)

Intermodulation at 1.1 MHz: blue*	>	46 dB
	typ.	60 dB
yellow*	>	46 dB
	typ.	50 dB
at 3.3 MHz**	>	46 dB
	typ.	54 dB



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level

} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

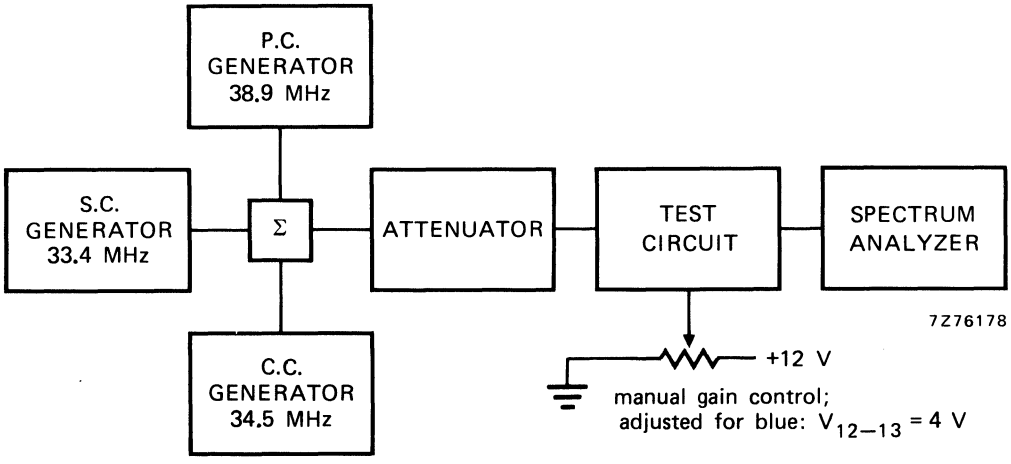


Fig. 3 Test set-up for intermodulation.

* $20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6$ dB.

** $20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$

8

Carrier signal at video output		typ. <	4 mV 30 mV
2nd harmonic of carrier at video output		typ. <	20 mV 30 mV
White spot inverter threshold level (Fig. 4)		typ.	6.6 V
White spot insertion level (Fig. 4)		typ.	4.7 V
Noise inverter threshold level (Fig. 4)		typ.	1.8 V
Noise insertion level (Fig. 4)		typ.	3.8 V
External video switch (VCR) switches off the output at:	V_{14-13}	<	1.1 V

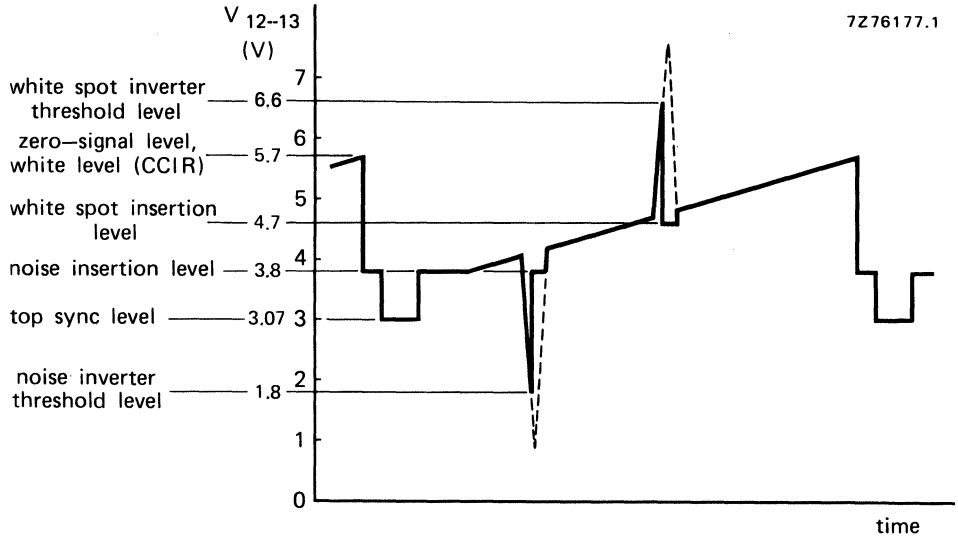


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

Tuner a.g.c. output current range	I_4		0 to 10 mA
Tuner a.g.c. output voltage at I_4 = 10 mA	V_{4-13}	<	0.3 V
Tuner a.g.c. output leakage current V_{14-13} = 11 V; V_{4-13} = 12 V	I_4	<	15 μA
Maximum a.f.c. output voltage swing	ΔV_{5-13}	> typ.	10 V 11 V
Detuning for a.f.c. output voltage swing of 10 V	Δf	typ. <	100 kHz 200 kHz
A.F.C. zero-signal output voltage (minimum gain)	V_{5-13}	typ.	6 V 4 to 8 V
A.F.C. switches on at:	V_{6-13}	>	3.2 V
A.F.C. switches off at:	V_{6-13}	<	1.5 V

APPLICATION INFORMATION

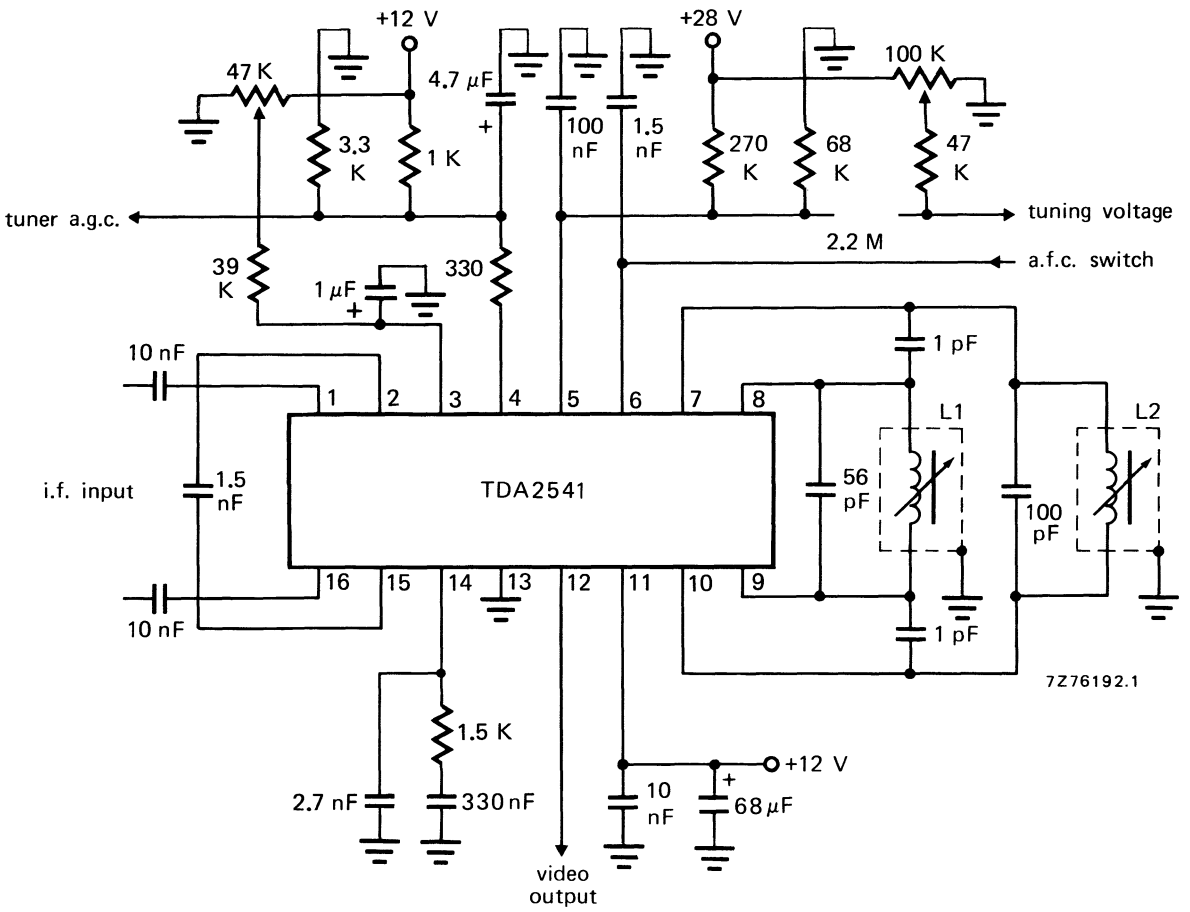
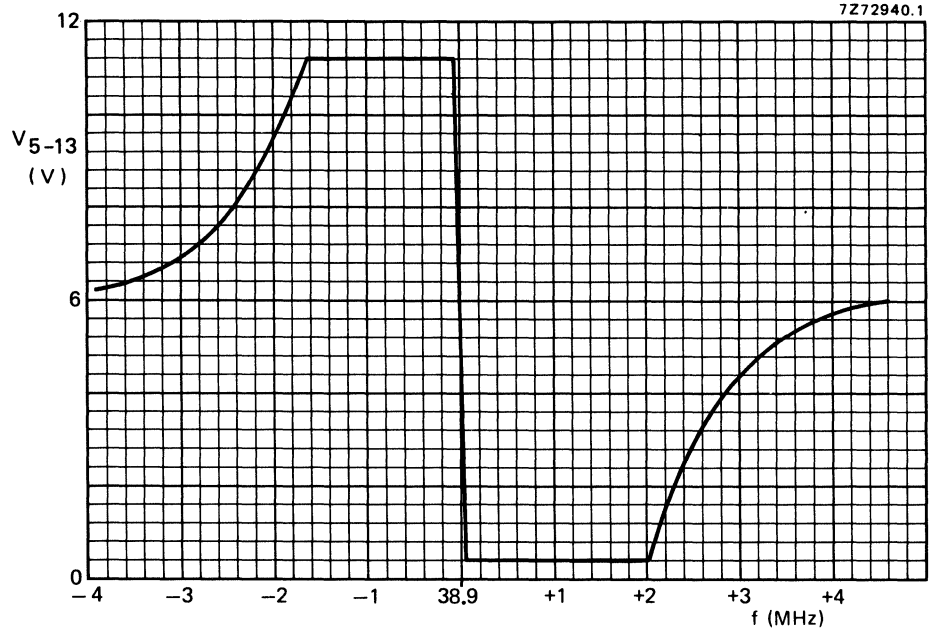


Fig. 5 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f_o = 38.9 MHz.



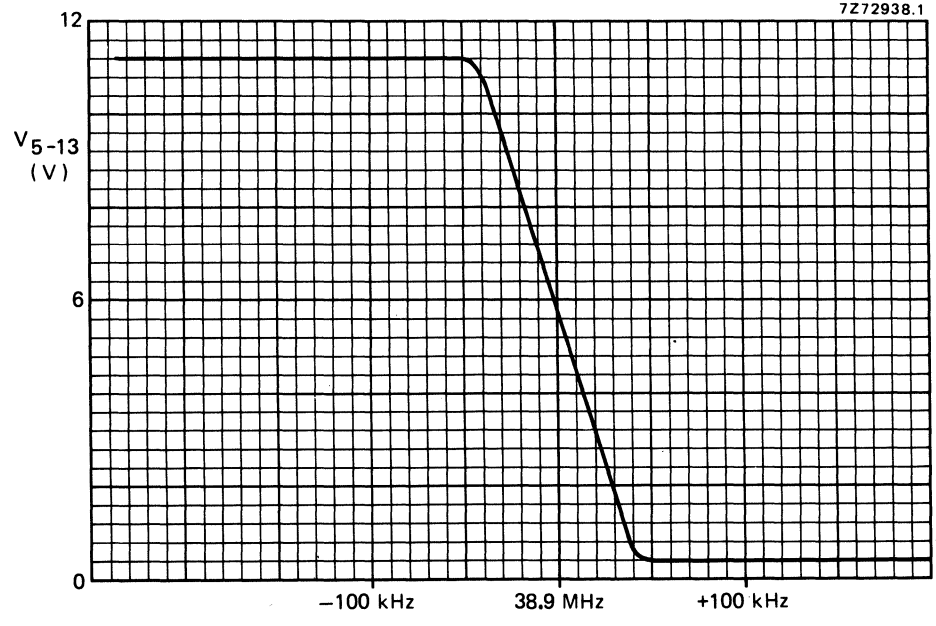


Fig. 6 A.F.C. output voltage (V_{5-13}) as a function of the frequency.

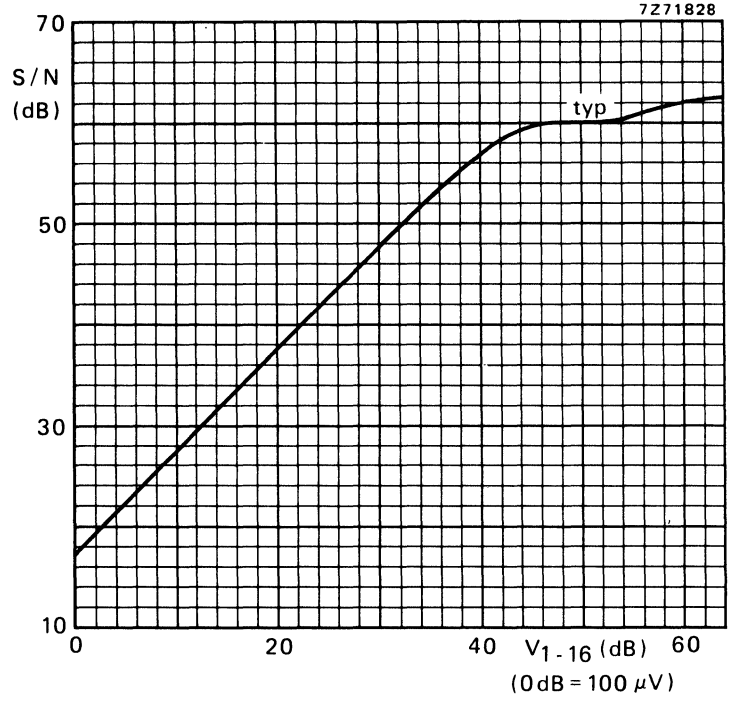


Fig. 7 Signal-to-noise ratio as a function of the input voltage (V_{1-16}).

Small Signal Combination IC for Color TV TDA4501

GENERAL DESCRIPTION

The integration into a single package of all small-signal functions required for colour tv reception is achieved in the TDA4501. The only additional circuits needed to complete the receiver are a tuner, the deflection output stages and a colour decoder.
The IC includes a vision IF amplifier with synchronous demodulator and AFC circuit; an AGC detector with tuner output; an integral three-level sandcastle pulse generator; and fully synchronized vertical and horizontal drive outputs. A triggered vertical divider automatically adapts to 50 or 60 Hz working and eliminates the need for an external vertical frequency control.
Signal-strength dependent time-constant switches in the horizontal phase detector make external VCR switching unnecessary.
Sound signals are demodulated and amplified within the IC in a circuit which includes volume control and muting.

Features

- Vision IF amplifier with synchronous demodulator
- AGC detector for negative modulation
- AGC output to tuner
- AFC circuit
- Video and audio preamplifiers
- Sound IF amplifier and demodulator
- Choice of sound volume control or horizontal oscillator starting function
- Horizontal synchronization circuit with two control loops
- Triggered divider system for vertical synchronization and sawtooth generation giving automatic amplitude adjustment for 50 or 60 Hz working
- Transmitter identification circuit with mute output
- Sandcastle pulse generator

QUICK REFERENCE DATA

Supply voltage	V_{7-6}	typ.	10,5 V
Supply voltage	V_{11-6}	typ.	10,5 V
Operating ambient temperature range	T_{amb}	−25 to	+ 65 °C
Storage temperature	T_{stg}	−25 to	+ 150 °C
Power dissipation	P_{tot}	max.	1,7 W

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT-117).

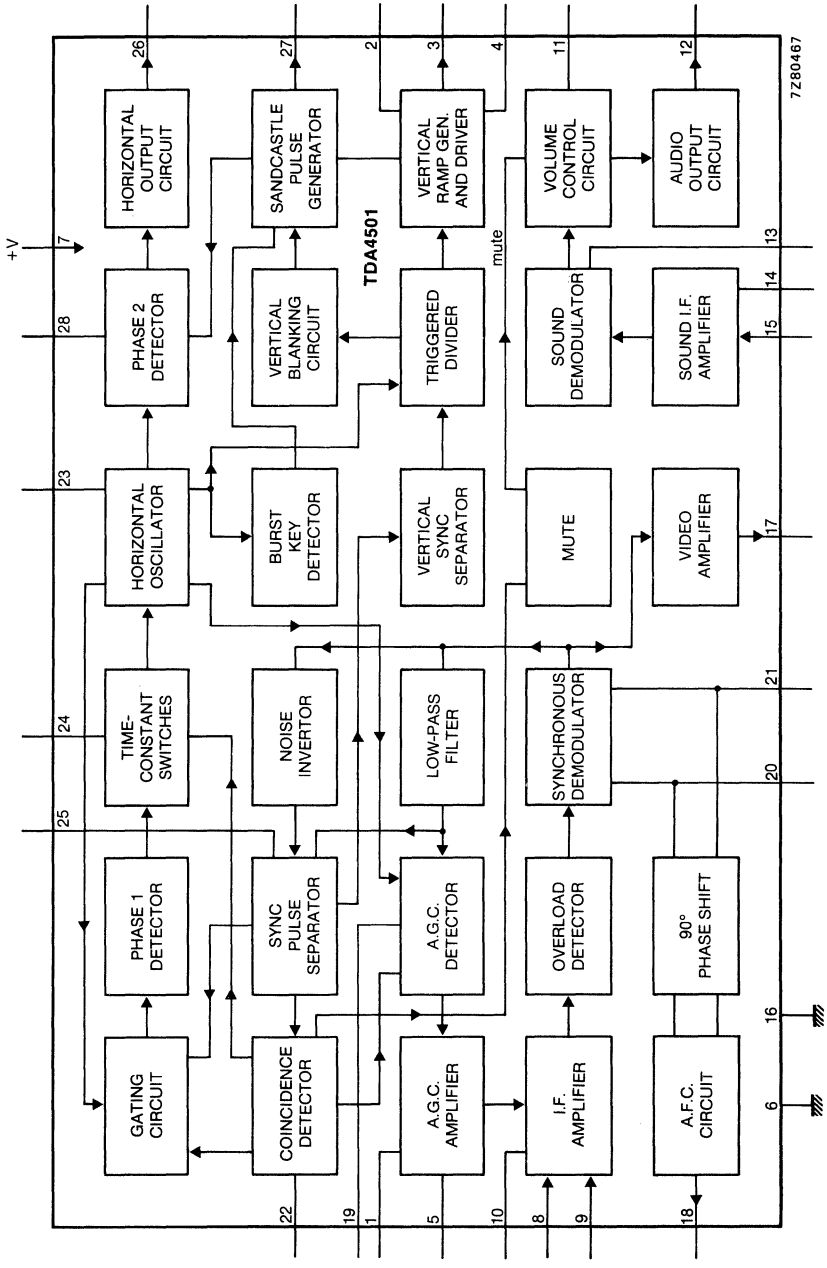


Fig. 1 Block diagram.

8

PINNING

1. AGC take over
2. Ramp generator
3. Vertical drive
4. Vertical feedback
5. Tuner AGC
6. Ground
7. Supply
8. IF input
9. IF input
10. Decoupling capacitor
11. Volume control/start Hor. osc.
12. Audio output
13. Sound demodulator
14. Sound IF decoupling
15. Sound IF input
16. Ground
17. Video output
18. AFC
19. AGC detection
20. Sync demodulator
21. Sync demodulator
22. Coincidence detector decoupling
23. Horizontal oscillator
24. Frequency control
25. Sync separator
26. Horizontal drive
27. Sandcastle out/flyback in
28. Phase detection

FUNCTIONAL DESCRIPTION

IF amplifier, demodulator and AFC

The IF amplifier has a symmetrical input (pins 8 and 9), the input impedance of which is suitable for SAW-filtering to be used. The synchronous demodulator and the AFC circuit share an external reference tuned circuit (pins 20 and 21). An internal RC-network provides the necessary phase-shifting for AFC operation. The AFC circuit provides a control voltage output with a swing greater than 9 V from pin 18.

AGC circuit

Gating of the AGC detector is performed to reduce sensitivity of the IF amplifier to external electrical noise. The AGC time constant is provided by an RC-circuit connected to pin 19. Tuner AGC voltage is supplied from pin 5 and is suitable for tuners with p-n-p or n-p-n RF stages. The sense of the AGC (to increase in a positive or negative direction) and the point of tuner take-over are preset by the voltage level at pin 1.

Video amplifier

The signal through the video amplifier comprises video and sound information, therefore no gating of the video amplifier is performed during flyback periods.

Sound circuit and horizontal oscillator starting function

The input to the sound IF amplifier is obtained by a bandpass filter coupling from the video output (pin 17). The sound is demodulated and passed via a dual-function volume control stage to the audio output amplifier. The volume control function is obtained by connecting a variable resistor (10 kΩ) between pin 11 and ground, or by supplying pin 11 with a variable voltage. Sound output is suppressed by an internal mute signal when no input signal is present.

The horizontal oscillator starting function is obtained by supplying pin 11 with a current of 6 mA during the switching-on period. The IC then uses this current to generate drive pulses for the horizontal deflection. For this application, the main supply voltage for the IC can be obtained from the horizontal deflection circuit.

FUNCTIONAL DESCRIPTION (continued)

Vertical divider system

A triggered divider system is used to synchronize the vertical drive waveforms, adjusting automatically to 50 or 60 Hz working. A large window (search window) is opened between counts of 488 and 722; when a separated vertical sync pulse occurs before count 576, the system works in the 60 Hz mode, otherwise 50 Hz working is chosen.
A narrow window is opened when 15 approved sync pulses have been detected. Divider ratio between 522 and 528 switches to 60 Hz mode; between 622 and 628 switches to 50 Hz mode.
The vertical blanking pulse is also generated via the divider system by adding the anti-topflutter pulse and the blanking pulse.

Line phase detector

The circuit has three operating conditions:
a. Strong input signal and synchronized.
b. Weak signal and synchronized.
c. Non synchronized (weak and strong) signal.
The input signal condition is obtained from the AGC circuit.

D.C. volume control/horizontal oscillator start

The operation depends on the application. When during switch-on no current is supplied pin 11 will act as volume control. When a current of 6 mA is applied the volume control is set to maximum and the circuit will generate drive pulses for the horizontal deflection.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7-6}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Operating ambient temperature range	T_{amb}		−25 to + 65	°C
Storage temperature range	T_{stg}		−25 to + 150	°C

8

CHARACTERISTICS

$V_P = V_{7-6} = 10{,}5$ V; $T_{amb} = 25\ ^oC$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 7)	V_{7-6}	9,5	10,5	13,2	V
Supply current (pin 7)	I_7	–	120	–	mA
Supply voltage (pin 11)	V_{11-6}	–	10,5	–	V
Supply current (pin 11) for horizontal oscillator start	I_{11}	–	6	–	mA
Vision IF amplifier (pins 8 and 9)					
Input sensitivity at 38,9 MHz (note 1)	V_{8-9}	40	70	120	μV
Input sensitivity at 45,75 MHz (note 1)	V_{8-9}	–	90	–	μV
Differential input resistance (pin 8 to 9)	R_{8-9}	–	1,3	–	kΩ
Differential input capacitance (pin 8 to 9)	C_{8-9}	–	5	–	pF
AGC range		–	60	–	dB
Maximum input signal	V_{8-9}	50	70	–	mV
Expansion of output signal for 50 dB variation of input signal with V_{8-9} at 150 μV (0 dB)	ΔV_{17-6}	–	1	–	dB
Video amplifier					
Output level for zero signal input (zero point of switched demodulator)	V_{17-6}	–	4,5	–	V
Output signal top sync level (note 2)	V_{17-6}	–	1,4	–	V
Amplitude of video output signal (peak-to-peak value)	$V_{17-6(p-p)}$	–	2,8	–	V
Internal bias current of output transistor (n-p-n emitter follower)	$I_{17(int)}$	1,4	2,0	–	mA
Bandwidth of demodulated output signal	B	–	6	–	MHz
Differential gain (Fig. 4)	G_{17}	–	6	–	%
Differential phase (Fig. 4)		–	4	–	%
Video non-linearity complete video signal amplitude		–	–	10	%
Intermodulation (Fig. 5) at gain control = 45 dB					
f = 1,1 MHz; blue;		55	60	–	dB
f = 1,1 MHz; yellow;		50	54	–	dB
f = 3,3 MHz; blue;		60	66	–	dB
f = 3,3 MHz; yellow		55	59	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Video amplifier (continued)					
Signal to noise ratio (note 3)					
Z_S = 75 Ω					
V_i = 10 mV	S/N	50	54	–	dB
end of gain control range	S/N	50	56	–	dB
Residual carrier signal		–	7	30	mV
Residual 2nd harmonic of carrier signal		–	3	30	mV
Tuner AGC *					
Take-over voltage (pin 1 for positive-going tuner AGC (NPN tuner)	$V_{1\text{-}6}$	–	3,5	–	V
Starting point take over; V = 5 V	$V_{1\text{-}6(rms)}$	–	0,4	2	mV
Starting point take over; V = 1,2 V	$V_{1\text{-}6(rms)}$	50	70	–	mV
Take-over voltage (pin 1) for negative-going tuner AGC (PNP tuner)	$V_{1\text{-}6}$	–	8	–	V
Starting point take over; V = 9,5 V	$V_{1\text{-}6(rms)}$	–	0,3	2	mV
Starting point take over; V = 5,6 V	$V_{1\text{-}6(rms)}$	50	70	–	mV
Maximum output swing	$I_{5\,max}$	2	3	–	mA
Output saturation voltage I = 2 mA	$V_{5\text{-}6(sat)}$	–	–	300	mV
Leakage current	I_5	–	–	1	μA
Input signal variation complete tuner control	ΔV_i	0,5	2	4	dB
AFC circuit (pin 18; note 4)					
AFC output voltage swing	$V_{18\text{-}6(p\text{-}p)}$	9	–	10	V
Available output current	$\pm I_{18}$	–	1	–	mA
Control steepness					
–100% picture carrier		20	40	80	mV/kHz
–10% picture carrier		–	15	–	mV/kHz
Output voltage at nom. tuning of the reference tuned circuit	$V_{18\text{-}6}$	–	5,25	–	V
Output voltage without input signal	$V_{18\text{-}6}$	2,7	5,25	8,5	V

* Starting point tuner take-over NPN current 1,8 mA; PNP tuner I = 0,2 mA.

parameter	symbol	min.	typ.	max.	unit
Sound circuit					
Input limiting voltage $V_o = V_o$ max. −3 dB; $Q_L = 16$ $f_{AF} = 1$ kHz; $f_c = 5{,}5$ MHz	V_{15lim}	–	400	–	μV
Input resistance $V_{i(rms)} = 1$ mV	$R_{15\text{-}6}$	–	2,6	–	kΩ
Input capacitance $V_{i(rms)} = 1$ mV	$C_{15\text{-}6}$	–	6	–	pF
AM rejection (Figs 8 and 9) $V_i = 10$ mV $V_i = 50$ mV	 AMR AMR	 – –	 35 43	 – –	 dB dB
AF output signal Δf = 7,5 kHz; min. distortion	$V_{12\text{-}6(rms)}$	220	320	–	mV
AF output impedance	$Z_{12\text{-}6}$	–	150	–	Ω
Total harmonic distortion Δf = 27,5 kHz	THD	–	1	–	%
Ripple rejection $f_k = 100$ Hz, volume control 20 dB when muted	 RR RR	 – –	 22 26	 – –	 dB dB
Output voltage mute condition	$V_{12\text{-}6}$	–	2,6	–	V
Signal to noise ratio weighted noise (CCIR 468)	S/N	–	47	–	dB
Volume control					
Voltage (pin 11 disconnected)	$V_{11\text{-}6}$	–	4,8	–	V
Current (pin 11 short circuited)	I_{11}	–	1	–	mA
External control resistor	$R_{11\text{-}6}$	–	10	–	kΩ
Suppression output signal during mute condition		–	66	–	dB
Horizontal synchronization					
Slicing level sync separator		–	30	–	%
Holding range PLL		800	1100	1500	Hz
Catching range PLL		600	1000	–	Hz
Control sensitivity video to oscillator; at weak signal at strong signal during scan during vert. retrace and during catching	 	 – – –	 2 3 6	 – – –	 kHz/μs kHz/μs kHz/μs

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Second control loop (positive edge)					
Control sensitivity	$\Delta t_d/\Delta t_o$	–	300	–	µs
Control range	t_d	–	25	–	µs
Phase adjustment via second control loop; control sensitivity		–	25	–	µA/µs
Maximum allowed phase shift		–	± 2	–	µs
Horizontal oscillator (pin 23)					
Free running frequency R = 35 kΩ; C = 2,7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		–	–	4	%
Frequency variation due to change of supply voltage from 8 to 12 V	Δf_{fr}	–	0	0,5	%
Frequency variation with temperature	Δf_{fr}	–	–	1×10^{-4}	K^{-1}
Maximum frequency shift	Δf_{fr}	–	–	10	%
Maximum frequency deviation (V_{7-6} = 8 V)	Δf_{fr}	–	–	10	%
Horizontal output (pin 26)					
Output voltage high	V_{26-6}	–	–	13,2	V
Output voltage at which protection commences	V_{26-6}	–	–	15,8	V
Output voltage low at I_{26} = 10 mA	V_{26-6}	–	0,3	0,5	V
Duty cycle of horizontal output signal	δ_0	–	45	–	%
Rise and fall times of output pulse	t_r, t_f	–	150	–	ns
Flyback input and sandcastle output					
Input current required during flyback pulse	I_{27}	0,1	–	2	mA
Output voltage during burst key pulse	V_{27-6}	7,5	–	–	V
Output voltage during horizontal blanking	V_{27-6}	3,5	4,0	4,5	V
Output voltage during vertical blanking	V_{27-6}	1,8	2,2	2,6	V
Width of burst key pulse		3,1	3,5	3,9	µs
Width of horizontal blanking pulse		flyback pulse width			
Width of vertical blanking pulse					
50 Hz working		–	21	–	lines
60 Hz working		–	17	–	lines
Delay between start of sync pulse at video output and rising edge of burst key pulse		–	5,2	–	µs

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parameter	symbol	min.	typ.	max.	unit
Coincidence detector mute output (pin 22)					
Voltage for in-sync condition	V_{22-6}	–	9,5	–	V
Voltage for no-sync condition no signal	V_{22-6}	–	1,0	1,5	V
Switching level to switch phase detector from slow to fast	V_{22-6}	4,9	5,3	5,8	V
Fast-to-slow hysteresis		–	1	–	V
Switching level to activate mute function (transmitter identification)	V_{22-6}	2,25	2,5	2,75	V
Output current for in-sync condition (peak-to-peak value)	$I_{22(p-p)}$	0,7	1,0	–	mA
Vertical ramp generator (pin 2)					
Input current during scan	I_2	–	12	–	μA
Discharge current during retrace	I_2	–	0,5	–	mA
Minimum voltage	V_{2-6}	–	1,5	–	V
Vertical output (pin 3)					
Output current	I_3	–	–	10	mA
Output impedance	R_{3-6}	–	400	–	Ω
Feedback input (pin 4)					
Input voltage					
d.c. component	V_{4-6}	–	3	–	V
a.c. component (peak-to-peak value)	$V_{4-6(p-p)}$	–	1,2	–	V
Input current	I_4	–	–	12	μA
Internal precorrection to sawtooth		–	6	–	%
Deviation amplitude 50/60 Hz		–	–	5	%

Notes

1. Typical value taken at starting level of AGC.
2. Signal with negative going sync, maximum white level 10% of the maximum sync amplitude (see Fig. 3).
3. Signal-to-noise ratio equals $20 \log \frac{V_{o(\text{black to white})}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.
4. $V_{i(rms)} = 10$ mV; see Fig. 2; Q-factor = 36.

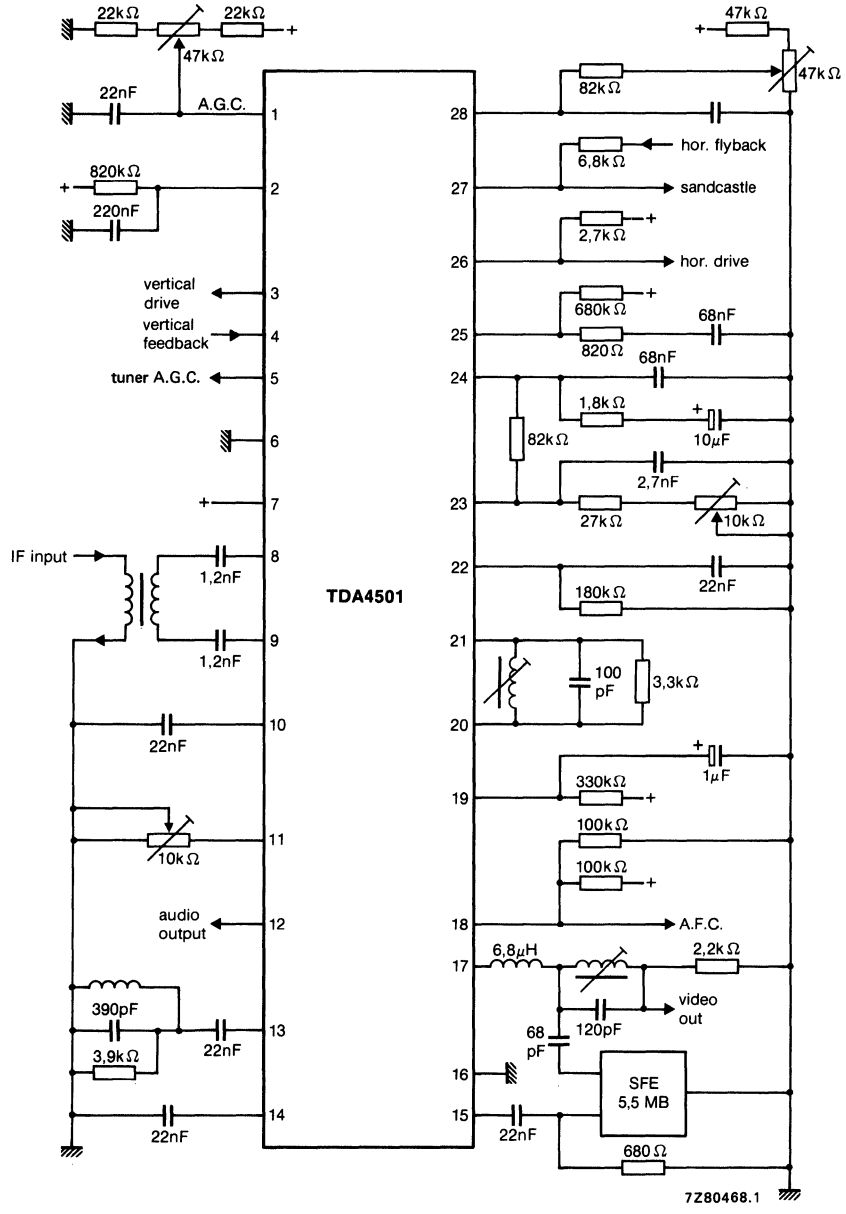


Fig. 2 Application diagram.

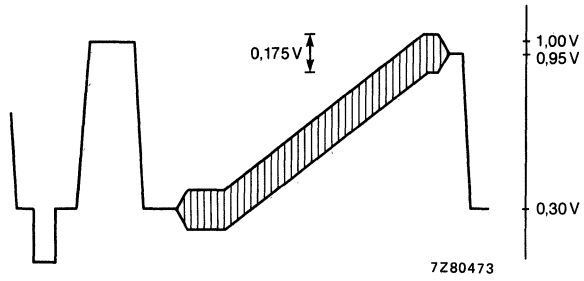


Fig. 3 Video output signal.

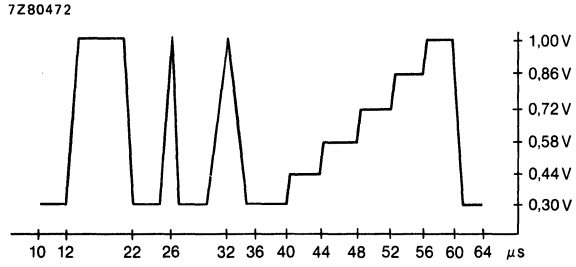
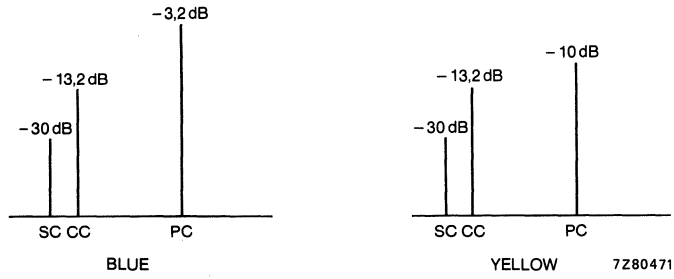
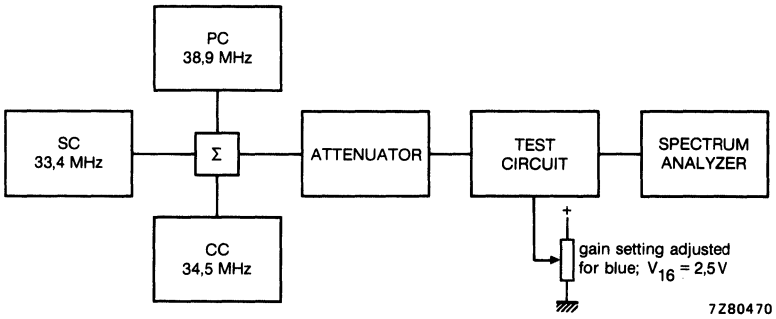


Fig. 4 E.B.U. test signal waveform (line 330).



SC = sound carrier
CC = chrominance carrier
PC = picture carrier
all with respect to top sync level.

Fig. 5 Input signal conditions.



Value at 1,1 MHz: $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6 \text{ dB}$

Value at 3,3 MHz: $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$.

Fig. 6 Test set-up intermodulation.

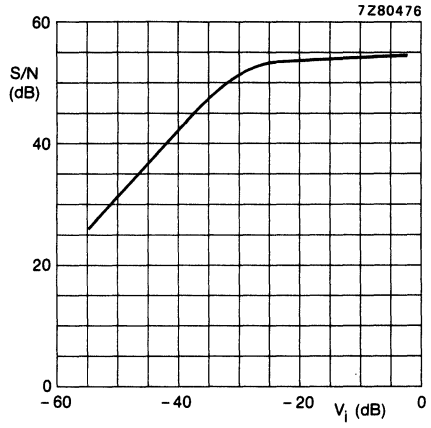


Fig. 7 S/N ratio as a function of the input voltage.

8

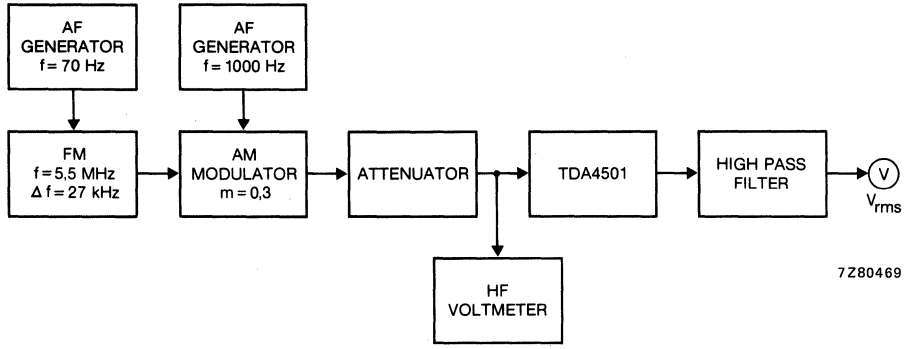


Fig. 8 Test set-up AM suppression.

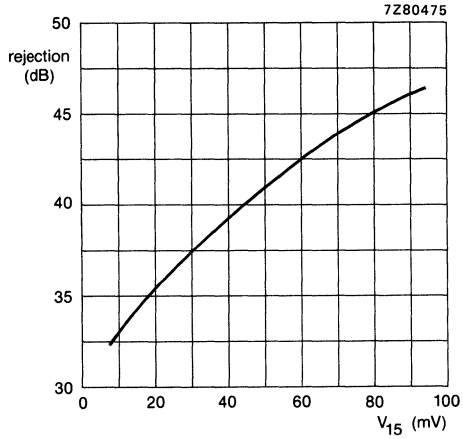


Fig. 9 AM rejection.

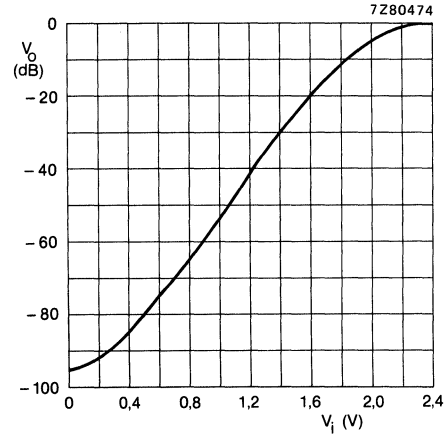


Fig. 10 Volume control characteristics.

Complete Video I.F. IC with Vertical and Horizontal Sync TDA4502

DESCRIPTION

The TDA4502 is a monolithic integrated small signal combination for television receivers.

FEATURES

- **Vision IF-amplifier with synchronous demodulator.**
- **A.G.C. detector suited for negative modulation.**
- **Tuner A.G.C.**
- **A.F.C. circuit with on/off switch.**
- **Video pre-amplifier.**
- **Video-switch to select the internal video signal or an external video signal.**
- **Horizontal synchronization circuit with two control loops.**
- **Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 and 60Hz.**
- **Transmitter identification (mute)**
- **Sandcastle pulse generation.**
- **The vision IF-amplifier and synchronization circuit is identical to that of the TDA4501. The differences of TDA4502 compared to the TDA4501 are the following:**
  - **The TDA4502 has no sound circuit but contains instead a video switching circuit.**

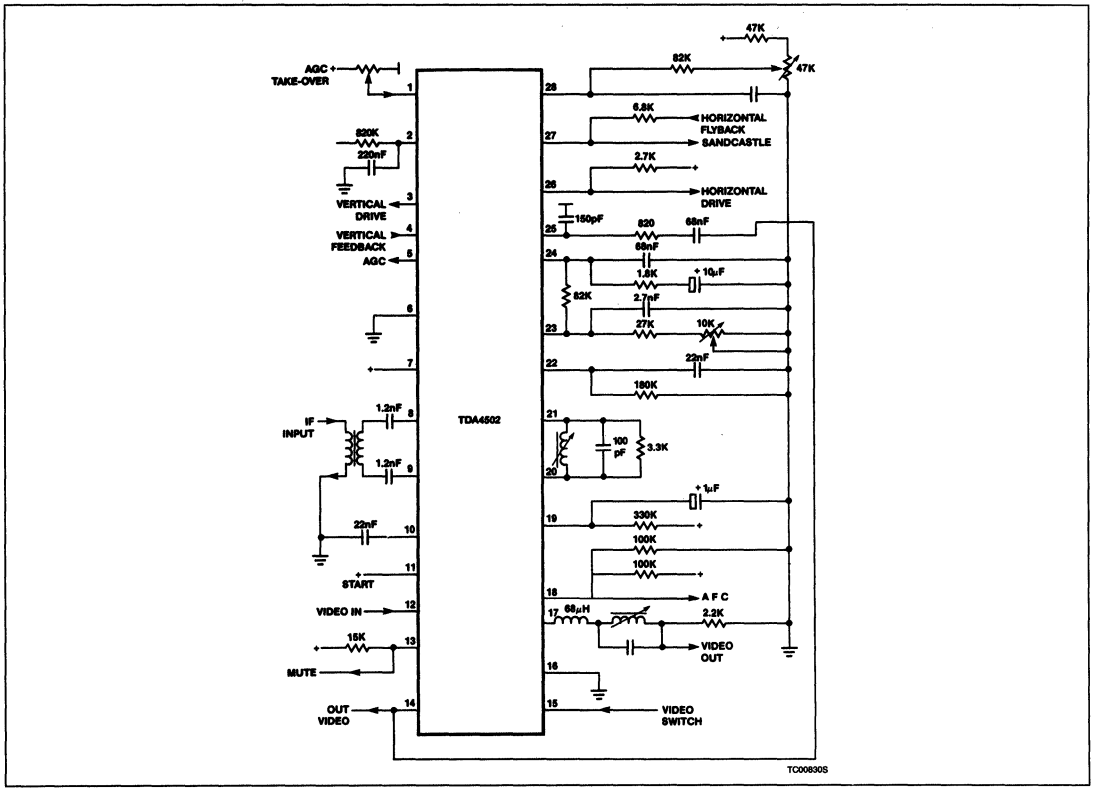
APPLICATIONS

- **Color TV receivers**

8

Complete Video I.F. IC with Vertical and Horizontal Sync TDA4502

APPLICATIONS DIAGRAM



Small Signal Combination for Monochrome TV TDA4503

GENERAL DESCRIPTION

The TDA4503 combines all small signal functions (except the tuner) which are required for a monochrome television receiver.

For a complete monochrome television receiver only output stages are required to be added for horizontal and vertical deflection, video and sound. The TDA4503 can also be used in simple colour television receivers. In this application an external sandcastle pulse generator is required.

It incorporates the following functions:

- vertical sync separator/oscillator
- vertical output
- coincidence detector (sound mute)
- phase detector/frequency control
- a.g.c. detector
- sync separator
- horizontal oscillator
- synchronous demodulator
- vision i.f. amplifier
- tuner a.g.c.
- d.c. volume control
- a.f.c. detector
- video output
- sound demodulator
- audio output
- gate pulse generator
- sound limiter/feedback
- 90° phase shift
- overload detector
- horizontal output

QUICK REFERENCE DATA

Supply voltage	V_{7-10}, V_{22-10}	typ.	10.5	V
Supply current	I_7	typ.	75	mA
Supply current	I_{22}	typ.	4.5	mA
Operating ambient temperature range	T_{amb}		−25 to +65	°C
Storage temperature range	T_{stg}		−25 to +150	°C
Power dissipation	P_{tot}	max.	1.7	W

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT-117).

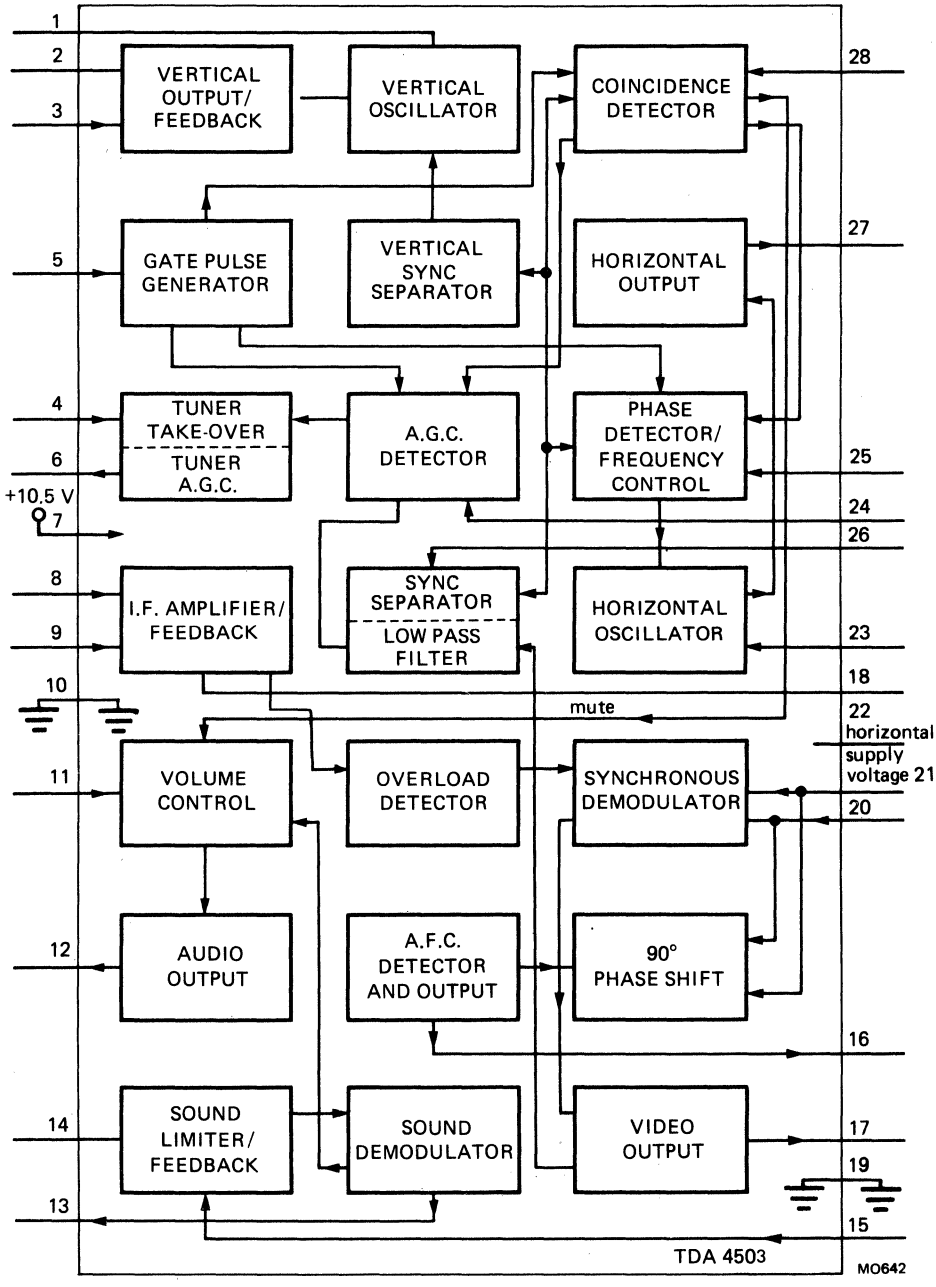


Fig. 1 Block diagram.

PINNING

Pin number	function	Pin number	function
1.	vertical oscillator	15.	sound i.f.
2.	vertical output	16.	a.f.c. output
3.	vertical feedback	17.	video output
4.	top linearity	18.	decoupling capacitor
5.	flyback pulse	19.	ground
6.	tuner a.g.c.	20.	38,5 MHz reference
7.	+10.5 V supply	21.	(38,9 MHz reference)
8.	i.f. input	22.	horizontal supply voltage
9.		23.	horizontal oscillator
10.	ground	24.	top sync detector
11.	volume control	25.	phase detector
12.	sound output	26.	sync separator
13.	6 MHz tuning (5,5 MHz tuning)	27.	horizontal output
14.	decoupling	28.	mute/coincidence detector

FUNCTIONAL DESCRIPTION (Fig. 1)

A complete black-and-white receiver can be built around this circuit by adding only the output stages for horizontal and vertical deflection with the video and sound output stages. The TDA4503 can also be used in simple colour television receivers using an external circuit to generate the sandcastle.

The block diagram (Fig. 1) depicts the various functions which are described briefly below.

The sensitivity of the i.f. amplifier is 70 μV for a peak-to-peak output voltage of 3 V (compare the TDA3541). This amplifier has a symmetrical input (pins 8 and 9) and is followed by a synchronous demodulator. The external tuned circuit is connected to pins 20 and 21. This circuit provides the information for the a.f.c. circuit, the 90° phase shift being supplied by internal RC-networks. An a.f.c. output with a voltage swing of about 9 V is obtained from pin 17 (V_{7-10} = 10.5 V).

The a.g.c. detector is gated to reduce sensitivity to external electrical noise and the a.g.c. time constant network is connected to pin 24. Gain control range of the i.f. amplifier is greater than 60 dB. Adjustments of the tuner take-over point is made at pin 4. When the voltage at pin 4 is approximately 3.5 V the direction of the tuner control voltage is positive-going. When the voltage at pin 4 is approximately 8 V the direction of the tuner control voltage is negative-going.

An output signal of 3 V (p-p) is obtained from the video amplifier (top sync level 1.5 V) with negative-going sync. Since the sound signal is derived from pin 16 (see Fig. 4) the video output is not blanked during the flyback period. As shown in the application circuit (Fig. 4) the band-pass filter for the sound must be connected between video output (pin 16) and sound i.f. input (pin 15). Sound information passes through a sound limiter network and a sound demodulator circuit with an external tuned circuit for this stage connected to pin 13. The demodulator is followed by a volume control stage with a control range of 80 dB and an output amplifier with an audio output signal of 170 mV (r.m.s.) for a Δf of 7.5 kHz and at maximum volume setting.

The slicing level of the sync separator is referred to the top sync and is determined by the values of external resistors, the recommended slicing level being 30%. Noise protection is provided for the sync separator stage. Separated sync pulses are supplied to the gated phase detector which compare the sync pulses with the sawtooth voltage obtained from the horizontal flyback pulse (pin 5). During catching the gating of the phase detector is switched off and the phase detector output current is increased.

The in-sync or out-of-sync condition is detected with the coincidence detector which is also used for transmitter identification. Sound output is suppressed when no input signal is available. Clamping the voltage on pin 28 to a level of 3.5 V sets the phase detector to a high output current, short time constant mode. This is appropriate for the reception of VCR signals.

Phase detector output voltage levels maintain the horizontal oscillator at its correct operating frequency. The push-pull output (pin 27) has a typical duty cycle of 40%.

Vertical sync pulses are obtained from an internal integrating network with the vertical sawtooth being generated in the vertical oscillator. This sawtooth voltage is compared with the feedback voltage from the deflection coil via pin 3. The comparator generates the drive voltage for the vertical deflection output stage.

The TDA4503 has four supply pins. Pin 7 and pin 10 are for the main positive supply and circuit ground respectively.

Critical circuits are grounded by pin 19. Pin 22 is the supply for the horizontal oscillator. A low current supply (5 mA minimum) can be used to start the oscillator from an external high voltage supply rail.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_{7-10}, V_{22-10}	max.	13.2	V
Total power dissipation	P_{tot}	max.	1.7	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		−25 to +65	°C

CHARACTERISTICS

V_{7-10} = 10.5 V, V_{22-10} = 10.5 V and T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{7-10}	9.5	10.5	13.2	V
Supply current	I_7	–	75	–	mA
Supply voltage (horizontal oscillator)	V_{22-10}	9.5	10.5	13.2	V
Supply current (horizontal oscillator, note 1)	I_{22}	–	4.5	–	mA
Power dissipation	P_{tot}	–	850	–	mW
Vision i.f. amplifier (pin 8)					
Input sensitivity (onset of a.g.c.) at 39.5 MHz (note 2)	$V_{i(rms)}$	–	70	–	μV
Differential input resistance (note 3)	R_i	–	800	–	Ω
Differential input capacitance (note 3)	C_i	–	6	–	pF
Gain control range	ΔG	–	56	–	dB
Output signal expansion for 50 dB input signal variation (note 4)	ΔV_o	–	1	–	dB
Maximum input signal	$V_{i\ max}$	–	50	–	mV
Video amplifier (note 5)					
Zero signal output level (note 6)	V_{16-10}	–	5	–	V
Top sync output level (note 7)	V_{16-10}	1.2	1.4	1.6	V
Video output signal amplitude (peak-to-peak value)	$V_{16-10(p-p)}$	2.75	3.0	3.25	V
Internal bias current of n-p-n emitter follower output transistor	I_B	1.4	2.0	–	mA
Bandwidth of demodulated output signal	B	5	6	–	MHz
Video non-linearity (note 8)		–	–	10	%

8

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Tuner a.g.c.					
Take-over voltage (pin 4) for positive-going tuner a.g.c. (n-p-n tuner)	V_{4-10}	–	3.5	–	V
Take-over voltage (pin 4) for negative-going tuner a.g.c. (p-n-p tuner)	V_{4-10}	–	8	–	V
Maximum tuner a.g.c. output swing	$I_{6\ max}$	2	3	–	mA
Output saturation voltage at I_6 = 2 mA	$V_{6-10(sat)}$	–	–	300	mV
Leakage current	I_6	–	–	1	μA
A.F.C. circuit (note 9)					
A.F.C. output voltage swing	V_{17-19}	9	–	10	V
Available output current	$\pm I_{17}$	–	1	–	mA
Output voltage at nominal tuning of the reference tuned circuit	V_{17-19}	–	5.25	–	V
Sound circuit					
Input limiting voltage when $V_O = V_{Omax} - 3$ dB (note 10)	$V_{14\ lim}$	–	400	–	μV
Input resistance at pin 15 (note 11)	R_i	–	3	–	kΩ
A.F. output signal at pin 12 (note 12) (r.m.s. value)	$V_{12-10(rms)}$	170	–	240	mV
Volume control (pin 11) (Fig. 3)					
Voltage with pin 11 disconnected	V_{11-10}	–	6.5	–	V
Current pin 11 short-circuited to ground	I_{11}	–	1	–	mA
Volume control characteristic (note 13)			See Fig. 3		
Value of external control resistor	R_{11-10}	–	5	–	kΩ

parameter	symbol	min.	typ.	max.	unit
Horizontal synchronization circuit					
Slicing level sync separator (note 14)		–	30	–	%
Holding range PLL		–	±1000	–	Hz
Catching range PLL		–	±600	–	Hz
Control sensitivity video to flyback (note 15)		–	2	–	kHz/μs
Horizontal oscillator					
Free running frequency	f_{osc}	–	15625	–	Hz
Spread with fixed external components	Δf_{osc}	–	–	4	%
Frequency variations due to supply voltage changes (note 16)	$\Delta f_{osc}/\Delta V$	–	0	–	%
Frequency variation with temperature	$\Delta f_{osc}/\Delta T$	–	–	1×10^{-4}	K^{-1}
Maximum frequency shift	Δf_{osc}	–	–	10	%
Maximum frequency deviation between starting point output and nominal condition	Δf_{osc}	–	–	10	%
Horizontal (push-pull) output					
Output current	I_{27}	10	–	–	mA
Output impedance	R_{27-10}	–	200	–	Ω
Voltage when I_{27} = 10 mA	V_{27-10}	–	2	–	V
	V_{27-22}	–	3	–	V
Duty cycle of output pulse (note 17)	δ	0.35	0.40	0.45	
Flyback input (note 18)					
Minimum required input amplitude (peak-to-peak value)	$V_{5-10(p-p)}$	–	4	–	V
Phase detector switching voltage		–	0	–	V

8

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Coincidence detector (mute) (note 19)					
Voltage in synchronized condition	V_{28-19}	–	9.5	–	V
Voltage in non-synchronized condition (no-signal)	V_{28-19}	–	1.0	1.5	V
Switching level to switch phase detector from slow to fast	V_{28-19}	4 5	5.0	5.5	V
Switching level to activate the 'mute' function (transmitter identification)	V_{28-19}	2.25	2.5	2.75	V
Output current; in-sync (peak-to-peak value)	$I_{28(p-p)}$	–	1	–	mA
Vertical oscillator					
Free running frequency	f_{osc}	–	47.5	–	Hz
Spread with fixed external components	Δf_{osc}	–	–	4	%
Holding range at nominal frequency		52.5	–	–	Hz
Temperature coefficient	TC	–	1×10^{-4}	–	K^{-1}
Frequency shift due to a supply voltage change from 9.5 to 12 V	$\Delta f_{osc}/\Delta V$	–	5	–	%
Vertical output (pin 2)					
Output current	I_2	1	1.3	–	mA
Output resistance	R_{2-10}	–	2	–	kΩ
Feedback input (pin 3)					
D.C. input voltage	V_{3-10}	4.75	5	5.25	V
A.C. input voltage (peak-to-peak value)	$V_{3-10(p-p)}$	–	1.2	–	V
Input current	I_3	–	–	10	μA
Non-linearity of deflection current at V_P = 10.5 V		–	–	2.5	%

Notes to characteristics

1. It is possible to start the horizontal oscillator by supplying a current of 5 mA which can be taken from the mains rectifier, to pin 22. The main supply (pin 7) can then be derived from the horizontal output stage.
2. I.F. input voltage (r.m.s.) – value at top sync level at which the video amplitude has dropped 0.5 dB compared with the amplitude at an input signal of 10 mV.
3. The input impedance has been chosen such that a SAW-filter can be applied. 800 Ω is an acceptable compromise between the requirements for triple transient suppression and power loss.
4. Measured with 0 dB = 150 μV.
5. Measured at 10 mV(r.m.s.) top sync input signal.
6. With switched demodulator.
7. Signal with negative-going sync with top white being 10% of the top sync amplitude (Fig. 2).
8. This figure is valid for the complete video signal amplitude (peak-white to top sync).
9. Measured with an input signal (V_{8-9}) of 10 mV(r.m.s.); the a.f.c. output (pin 7) loaded with 2 x 100 kΩ between the supply and ground. The Q factor of the reference tuned circuit is 50.
10. Voltage at pin 15 is the r.m.s. value. Q_L of the demodulator tuned circuit is 20. Audio frequency is 1 kHz and the carrier frequency is 5.5 MHz.
11. Measured with an input signal of 1 mV(r.m.s.)
12. The tuned demodulator circuit must give an output level equal to that given in the "mute" condition.
13. Volume can be controlled using a variable resistor connected to ground (nominal 5 kΩ) or by means of a variable d.c. voltage. In this latter case the rather low impedance at pin 11 must be taken into account.

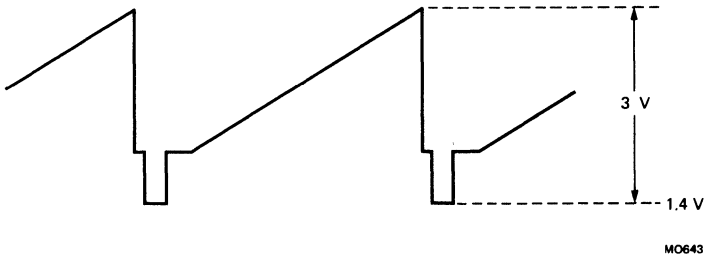


Fig. 2 Video output signal.

Notes to characteristics (continued)

14. The sync separator is noise gated. The slicing level is referred to top sync level and is independent of the video information. The value given is a percentage of the sync pulse amplitude. The slicing depends on the values of external resistors connected to pin 26.
15. Phase detector current increases by a factor of 7 during "catching" and when phase detector operates in the 'FAST' mode (pin 28). This ensures a high catching range and a higher dynamic loop gain.
16. Supply voltage variation in the range 8 to 12 V.
17. The negative-going edge of this pulse initiates the switch-off of the horizontal output transistor (simultaneous driver).
18. The circuit requires an integrated flyback pulse. The gate pulses for a.g.c. and the coincidence detector are obtained from the sawtooth.
19. The functions of in-sync/out-of-sync and transmitter identification have been combined on pin 28. For reception of VCR-signals the voltage on this pin must be fixed between 3 V and 4.5 V so that the time constant is fast and the sound is still available.

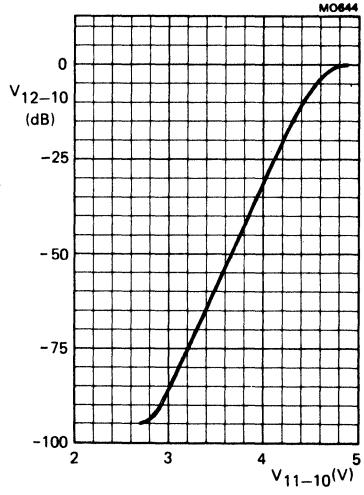


Fig. 3 Volume control characteristic at f = 1 kHz.

APPLICATION INFORMATION

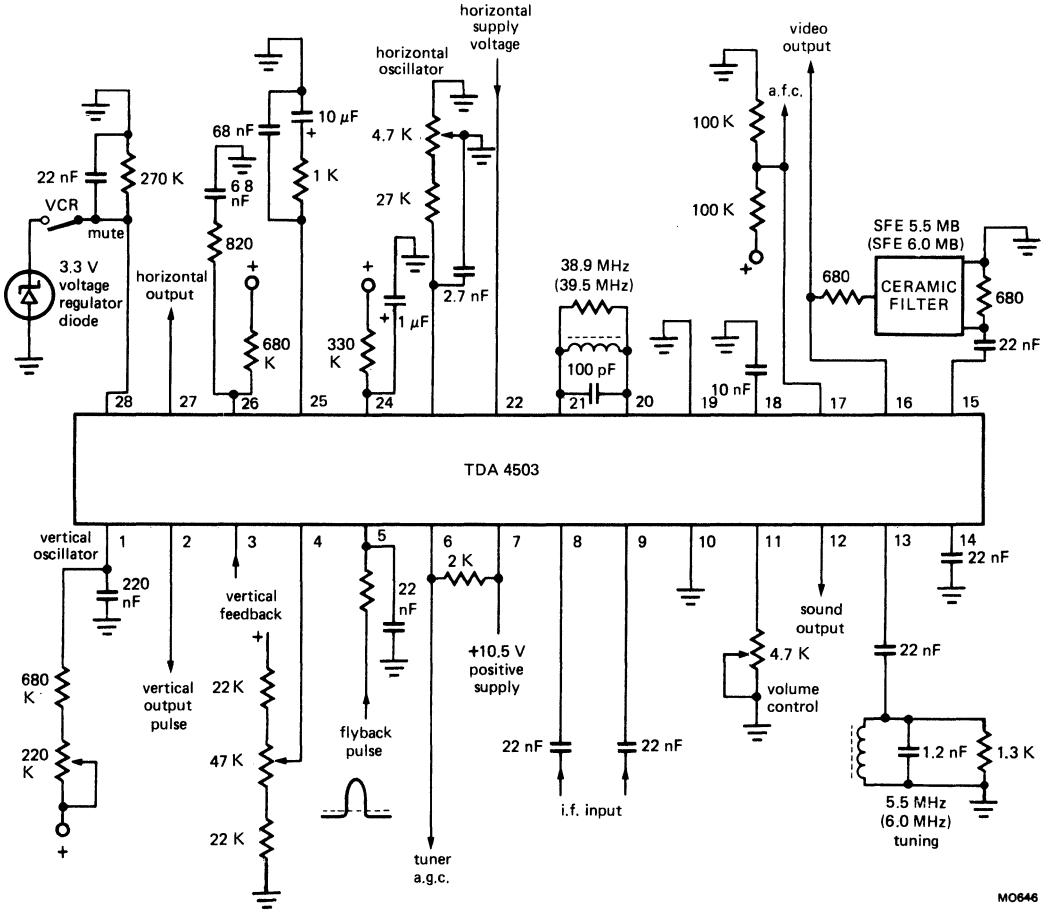


Fig. 4 Typical application circuit.

Sound I.F. Amplifier/Demodulator For TV — TBA120U

The TBA120U is an i.f. amplifier with a symmetrical FM demodulator and an a.f. amplifier with adjustable output voltage. The a.f. amplifier is also provided with an output for volume control and an input for VCR operation.

The input and output of the TBA120U are especially designed for LC-circuits, but the input can also be used with a ceramic filter.

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	12 V
Supply current	I_P	typ.	13,5 mA
I.F. voltage gain at f = 5,5 MHz	$G_{v\ if}$	typ.	68 dB
Input voltage starting limiting	V_i	typ.	30 μV
AM suppression at $\Delta f = \pm 50$ kHz	α	typ.	60 dB
A.F. output voltage adjustment range (pin 8)	$\Delta V_{o\ af}$	typ.	85 dB
A.F. output voltage at $\Delta f = \pm 50$ kHz (r.m.s. value)			
at pin 8	$V_{o\ af(rms)}$	typ.	1,2 V
at pin 12	$V_{o\ af(rms)}$	typ.	1,0 V

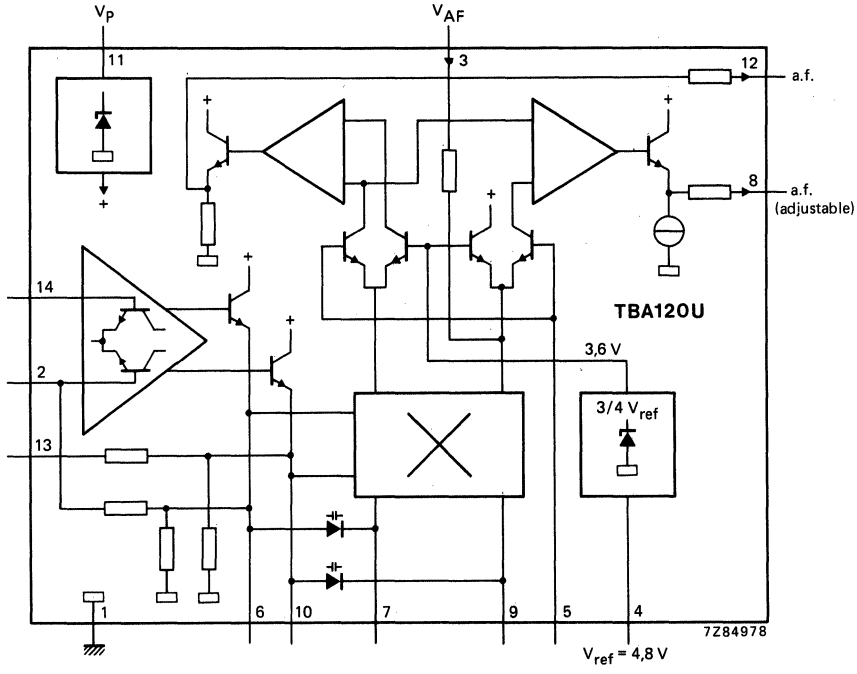


Fig. 1 Block diagram.

PACKAGE OUTLINE

14-lead DIL; plastic (SOT-27K, M, T).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11-1}$	max.	18	V*
Adjustment voltage (pin 5)	V_{5-1}	max.	6	V
Total power dissipation	P_{tot}	max.	400	mW
By-pass resistance	R_{13-14}	max.	1	kΩ
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−15 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; f = 5,5 MHz

I.F. voltage gain	$G_{v\ if\ 6-14}$	typ.	68	dB
Input voltage starting limiting at Δf = ± 50 kHz; f_m = 1 kHz	V_i	typ. <	30 60	μV μV
I.F. output voltage at limiting (peak-to-peak value)	$V_{o\ if\ (p-p)}$	typ.	250	mV
AM suppression at Δf = ± 50 kHz; V_i = 500 μV; f_m = 1 kHz; m = 30%	α	> typ.	50 60	dB dB
I.F. residual voltage without de-emphasis at pin 12	$V_{if\ 12}$	typ.	30	mV
at pin 8	$V_{if\ 8}$	typ.	20	mV
A.F. voltage gain	$G_{v\ af\ 8-3}$	typ.	7,5	
A.F. adjustment at R_{4-5} = 5 kΩ; R_{5-1} = 13 kΩ	$\Delta V_{o\ af}$	 typ.	20 to 36 28	dB dB
A.F. output voltage control range	$\Delta V_{o\ af}$	> typ.	70 85	dB dB
Adjustment resistor**	R_{4-5}		1 to 10	kΩ
D.C. voltage portion at the a.f. outputs pin 12	V_{12-1}	typ.	5,6	V
pin 8	V_{8-1}	typ.	4,0	V
Output resistance of the a.f. outputs pin 12	$R_{o\ 12-1}$	typ.	1,1	kΩ
pin 8	$R_{o\ 8-1}$	typ.	1,1	kΩ
Input resistance of the a.f. input	$R_{i\ 3-1}$	typ.	2	kΩ
Stabilized reference voltage	$V_{4-1} = V_{ref}$	 typ.	4,2 to 5,3 4,8	V V
Source resistance of reference voltage source	R_{4-1}	typ.	12	Ω

* Supply voltage operating range is 10 to 18 V.

** Pin 5 must be connected to pin 4, when volume control adjustment is not applicable.

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Hum suppression			
at pin 12	V_{12}/V_{11}	typ.	30 dB
at pin 8	V_8/V_{11}	typ.	35 dB
Supply current (pin 11)	$I_P = I_{11}$		9,5 to 17,5 mA
		typ.	13,5 mA
I.F. input impedance	$\|Z_i\|$	typ.	40 kΩ/4,5 pF
		>	15 kΩ/< 6 pF
A.F. output voltage at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 45$; r.m.s. value			
at pin 12	$V_{o\ af\ (rms)}$	typ.	1,0 V
at pin 8	$V_{o\ af\ (rms)}$	typ.	1,2 V
Distortion at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 20$	d_{tot}	typ.	1 %

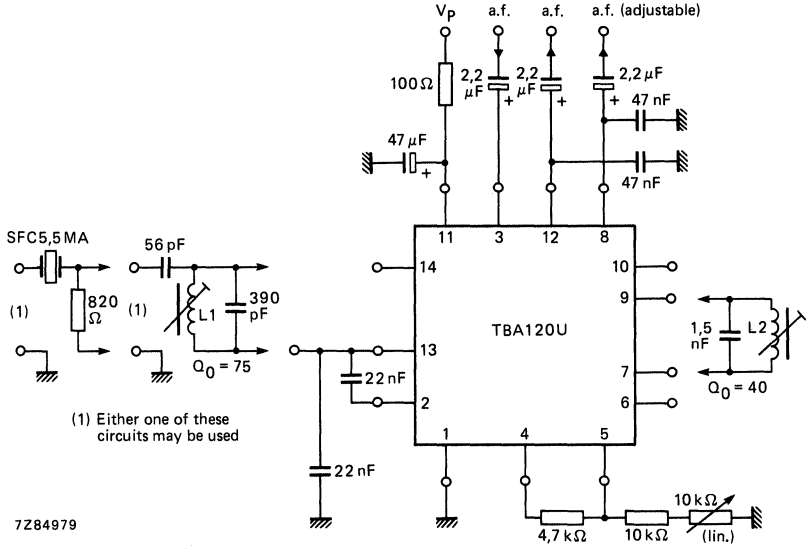


Fig. 2 Application example using TBA120U.

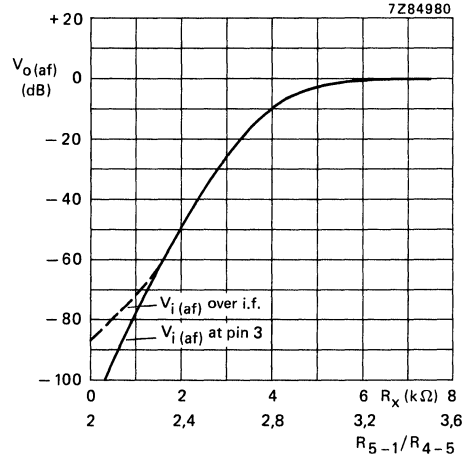


Fig. 3 The a.f. output voltage at pin 8 as a function of the resistance values as shown in Fig. 4.

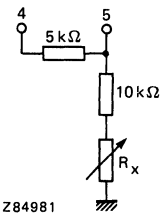
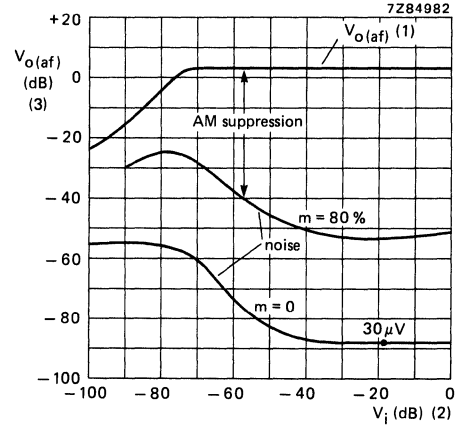


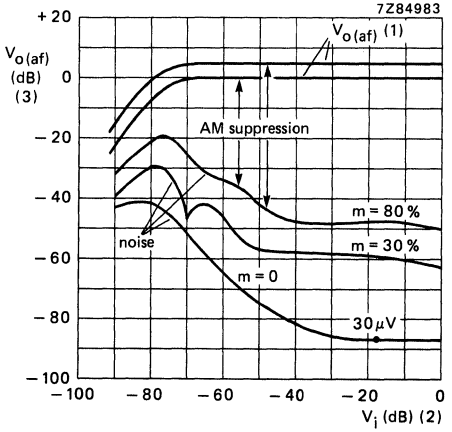
Fig. 4 Resistor conditions for curves in Fig. 3.



(1) $V_{o\,af}$ with de-emphasis at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $d_{tot} = 1{,}5\%$; 0 dB ≙ 770 mV.

(2) V_i: 0 dB ≙ 200 mV at 60 Ω.

Fig. 5 The a.f. output voltage at pin 8 as a function of the input voltage with SFC 5,5 MA at the input (see Fig. 2).



(1) $V_{o\,af}$ with de-emphasis at $f_m = 1$ kHz; 0 dB ≙ 770 mV;
curve a: $\Delta f = \pm 50$ kHz; $d_{tot} = 3\%$;
curve b: $\Delta f = \pm 25$ kHz; $d_{tot} = 1\%$.

(2) V_i: 0 dB ≙ 200 mV at pin 14.

Fig. 6 The a.f. output voltage at pin 8 as a function of the input voltage with broadband input (60 Ω).

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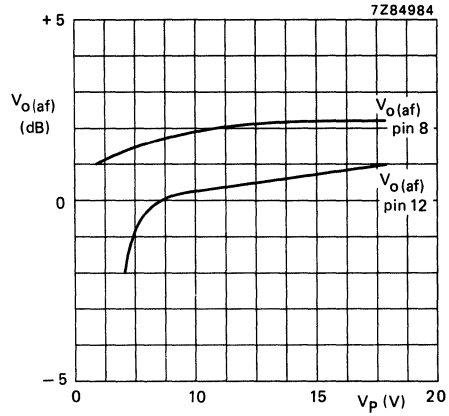


Fig. 7 The a.f. output voltages at pins 8 and 1 as a function of the supply voltage; 0 dB ≙ 770 mV.

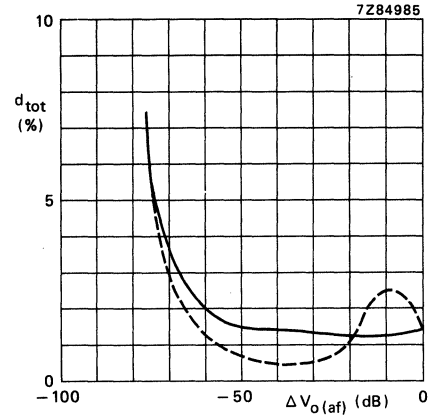


Fig. 8 Total distortion as a function of the a.f. output voltage change.
——— 0 dB ≙ 900 mV over i.f. (pin 8)
– – – – 0 dB ≙ 1,15 V (pin 8)

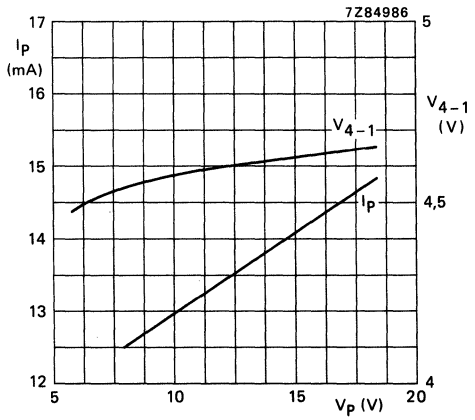
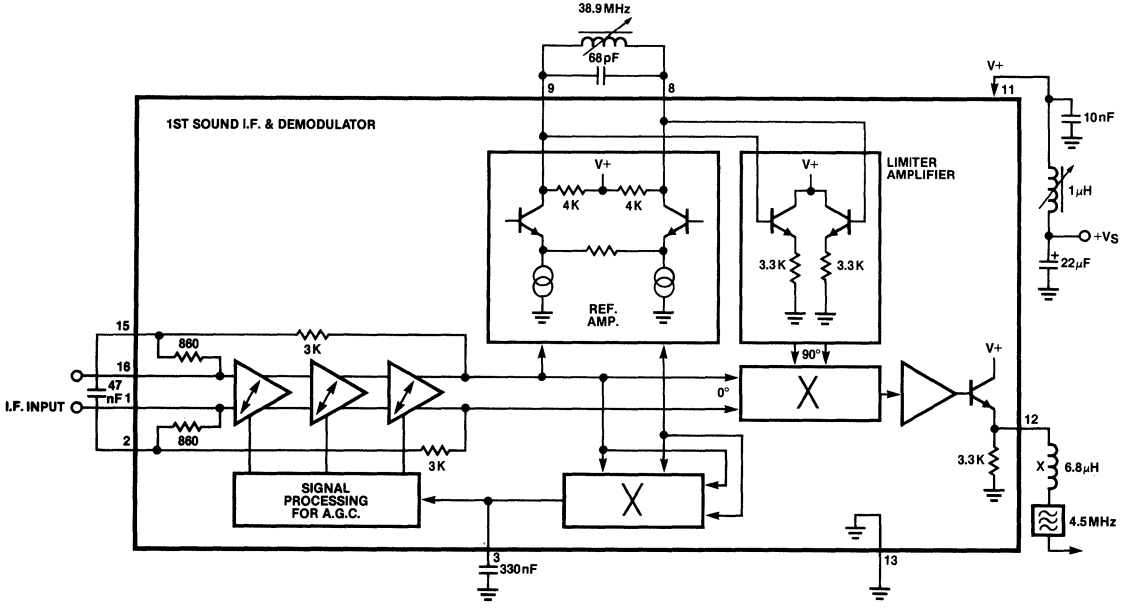


Fig. 9 Supply current and the reference voltage at pin 4 as a function of supply voltage.

Quasi-Split Sound Circuit TDA2545A

The TDA2545A is a monolithic integrated circuit for quasi-split-sound processing in television receivers.

- **3-stage gain controlled IF amplifier**
- **A.G.C. circuit**
- **Reference amplifier with limiter amplifier for vision carrier (V.C.) processing**
- **Linear multiplier for quadrature demodulator**



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Quasi-Split Sound I.F. with Sound Demodulator TDA2546A

GENERAL DESCRIPTION

The TDA2546A is a monolithic integrated circuit for quasi-split-sound processing, including 5.5 MHz demodulation, in television receivers.

Features

1st i.f. (V.C.: vision carrier plus S.C.: sound carrier)

- 3-stage gain controlled i.f. amplifier
- A.G.C. circuit
- Reference amplifier and limiter amplifier for vision carrier (V.C.) processing
- Linear multiplier for quadrature demodulation

2nd i.f. (5.5 MHz signal)

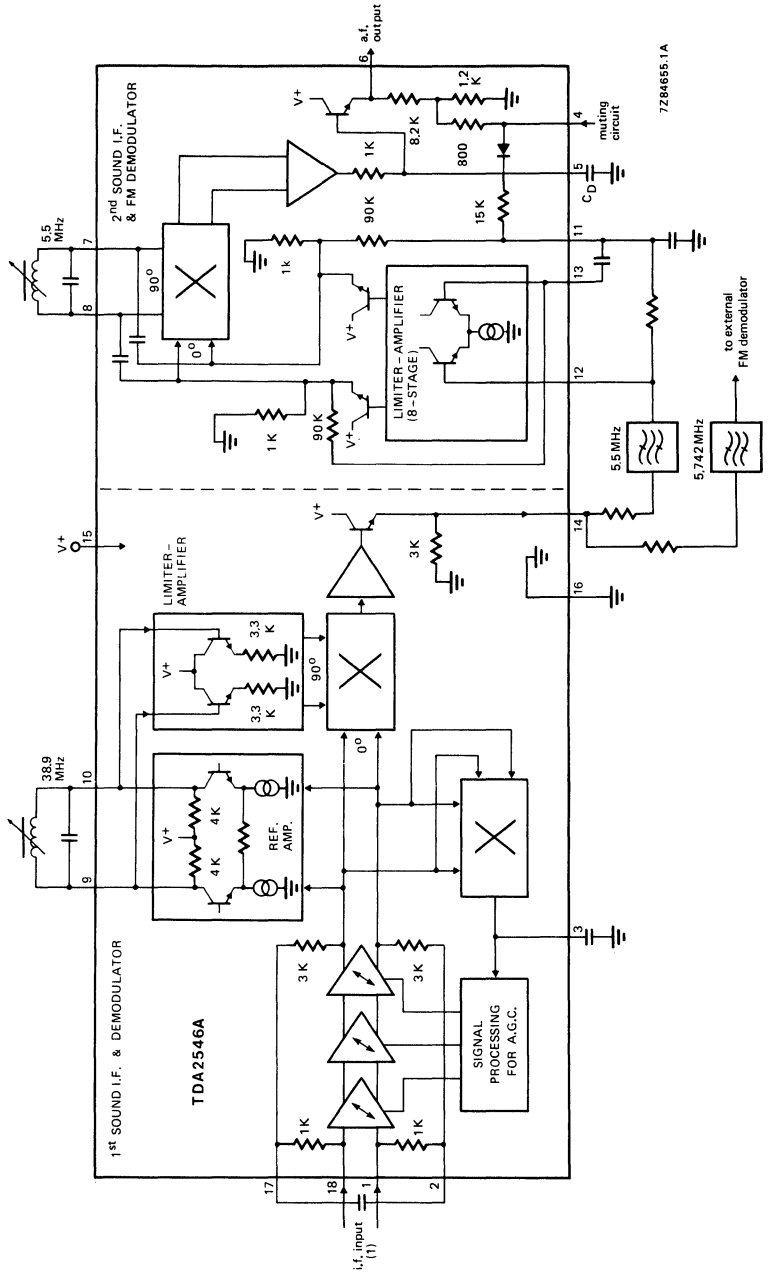
- 8-stage limiter amplifier
- Quadrature demodulator
- A.F. amplifier with de-emphasis
- AV switch

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_P = V_{15-16}$	typ.	12 V
Supply current (pin 15)	$I_P = I_{15}$	typ.	54 mA
Minimum i.f. vision carrier input voltage (r.m.s. value)	$V_{VC1-18(rms)}$	typ.	50 μV
Output voltage; 5.5 MHz (r.m.s. value)	$V_{14-16(rms)}$	typ.	100 mV
Output voltage; 5.742 MHz (r.m.s. value)	$V_{14-16(rms)}$	typ.	45 mV
I.F. control range	ΔG_V	min.	66 dB
Signal-to-weighted-noise ratio			
at 5.5 MHz	S + W/W	min.	53 dB
at 5.742 MHz	S + W/W	min.	51 dB
A.F. output voltage (r.m.s. value)	$V_{o6-16(rms)}$	typ.	0.6 V

PACKAGE OUTLINES

18-lead DIL; plastic (SOT-102CS).



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

Fig. 1 Block diagram.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15-16}$	max.	13.2	V
Input current (pin 4)	I_4	max.	5	mA
Storage temperature range	T_{stg}	−25 to	+150	°C
Operating ambient temperature range	T_{amb}	0 to	+70	°C

CHARACTERISTICS

$V_P = V_{15-16} = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38.9$ MHz, $f_{SC1} = 33.4$ MHz, $f_{SC2} = 33.158$ MHz:

Vision carrier (V.C.) modulated with 2 T/20 T pulses, line-for-line alternating with white bars; modulation depth 100% (proportional to 10% residual carrier).

Sound carriers (S.C.1, S.C.2) modulated with f = 1 kHz and $\Delta f = \pm 30$ kHz.

Vision-to-sound carrier ratios are V.C./S.C.1 = 13 dB and V.C./S.C.2 = 20 dB.
Vision carrier amplitude (r.m.s. value) is $V_{VC} = 10$ mV.
For measuring circuit see Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15-16}$	10.8	12	13.2	V
Supply current	$I_P = I_{15}$	–	54	–	mA
I.F. amplifier					
Minimum input voltage (r.m.s. value) (intercarrier signals –3 dB)	$V_{VC1-18(rms)}$	–	50	–	μV
Maximum input voltage (r.m.s. value) (intercarrier signals + 1 dB)	$V_{VC1-18(rms)}$	–	100	–	mV
I.F. control range	ΔG_v	66	–	–	dB
Control voltage range	V_{3-16}	4	–	9	V
Input resistance	R_{1-18}	–	2	–	kΩ
Input capacitance	C_{1-18}	–	2	–	pF
Intercarrier generation					
Output voltage; 5.5 MHz (r.m.s. value)	$V_{14-16(rms)}$	–	100	–	mV
Output voltage; 5.742 MHz (r.m.s. value)	$V_{14-16(rms)}$	–	45	–	mV
D.C. output voltage	V_{14-16}	–	5.9	–	V
Allowable load resistance at the output	R_{14-16}	7	–	–	kΩ
Allowable output current	$-I_{14}$	–	–	1	mA
Frequency demodulator (measured at f = 5.5 MHz)					
Input voltage for start of limiting (r.m.s. value)	$V_{12-16(rms)}$	–	–	100	μV
Maximum input voltage (r.m.s. value)	$V_{12-16(rms)}$	–	200	–	mV
D.C. output voltage	$V_{11,12,13-16}$	–	2.2	–	V

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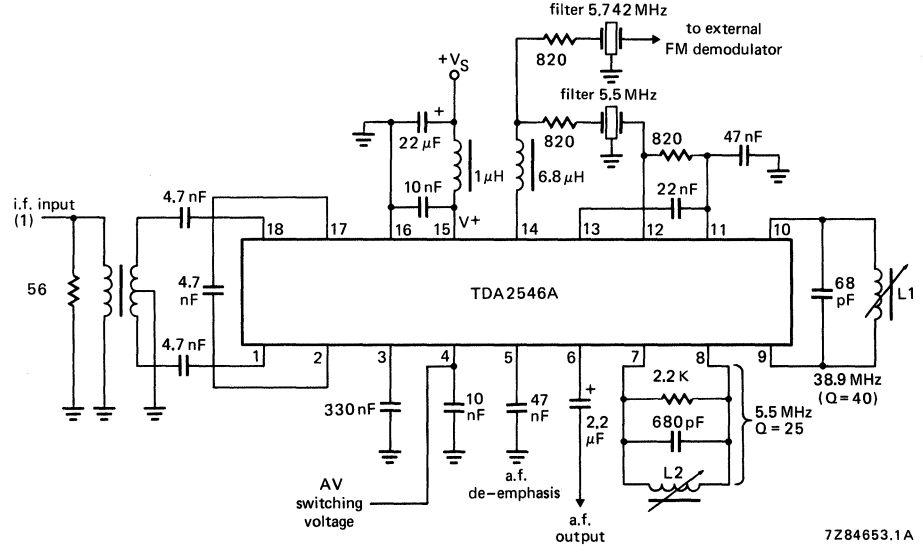
parameter	symbol	min.	typ.	max.	unit
A.F. output voltage (r.m.s. value)	$V_{6\text{-}16(rms)}$	–	600	–	mV
D.C. output voltage	$V_{6\text{-}16}$	–	4	–	V
Allowable load resistance at the output	$R_{6\text{-}16}$	27	–	–	kΩ
Total harmonic distortion	THD	–	–	1	%
Internal de-emphasis resistance	$R_{i5\text{-}16}$	–	1	–	kΩ
Switching voltage (pin 4)					
for mute	$V_{4\text{-}16}$	9	–	–	V
for a.f. on	$V_{4\text{-}16}$	–	–	2.5	V
Intercarrier signal-to-noise (measured behind the FM demodulators)					
Signal-to-weighted-noise ratio according to CCIR 468-2, quasi-peak					
at 5.5 MHz	S + W/W	53	–	–	dB
at 5.742 MHz	S + W/W	51	–	–	dB
with black level (vision carrier modulated with sync pulses only)					
at 5.5 MHz	S + W/W	60	–	–	dB
at 5.742 MHz	S + W/W	58	–	–	dB



(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 2 Measuring circuit for TDA2546A.

Dual TV Sound Demodulator Circuit TDA2555

GENERAL DESCRIPTION

The TDA2555 incorporates two FM demodulator systems to perform the demodulator functions required in a dual sound carrier TV system for demodulating the sound carriers.

- Eight stage limiting amplifier
- Quadrature demodulator for FM detection
- De-emphasis stage
- Output amplifier

QUICK REFERENCE DATA

Supply voltage (pins 13 and 15)	V_P	typ.	12 V
Supply current (pins 13 and 15)	I_P	typ.	24,5 mA
AF output voltage (pins 2 and 8), rms value	$V_{o(rms)}$	typ.	350 mV
Total harmonic distortion	THD	<	0,1 %

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

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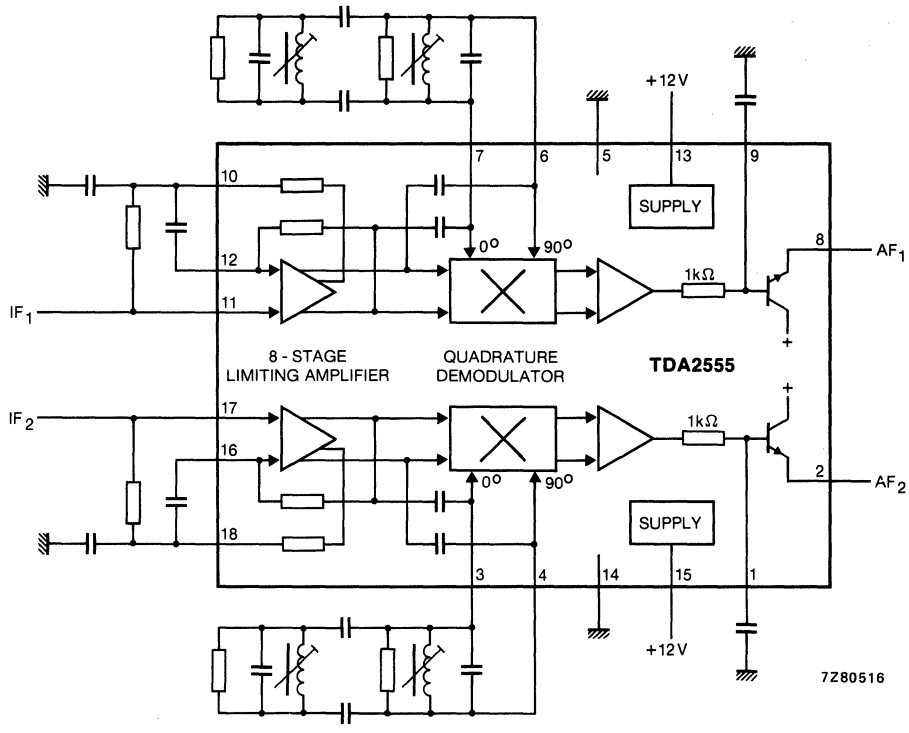

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pins 13 and 15)	V_P	max.	13,2 V
Total power dissipation	P_{tot}	max.	400 mW
Storage temperature range	T_{stg}	−25 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

CHARACTERISTICS

$V_P = V_{13,15-14} = 12$ V; $T_{amb} = 25$ °C; f = 5,5 MHz; $f_{m1} = 1$ kHz; $\Delta f = \pm 30$ kHz; $V_{i\,(rms)} = 5$ mV, see test circuit Fig. 2, voltages with respect to ground (pin 14), unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pins 13 and 15)	V_P	10,8	12,0	13,2	V
Supply current	$I_{13,\,15}$	–	24,5	–	mA
Input voltage (rms value) for start of limiting	$V_{12,\,17(rms)}$	–	–	100	μV
Maximum input voltage	$V_{12,17-14}$	–	200	–	mV
D.C. voltage at inputs pins 10, 11, 12, 16, 17 and 18 to 14	V_i	–	2,0	–	V
A.M. suppression $f_{m(fm)} = 70$ Hz; $\Delta f = \pm 30$ kHz $f_{m(am)} = 1$ kHz; m = 30%	AMS	50	–	–	dB
A.F. output voltage r.m.s. value	$V_{2,8-14}$	350	–	–	mV
D.C. voltage at outputs pins 2 and 8	$V_{2,8-14}$	–	3,7	–	V
Output lead resistance pins 2 and 8	R_L	10	–	–	kΩ
Total harmonic distortion	THD	–	–	0,1	%
Internal de-emphasis resistance pins 1 and 9	R_i	–	1,0	–	kΩ
Channel separation	α	60	–	–	dB

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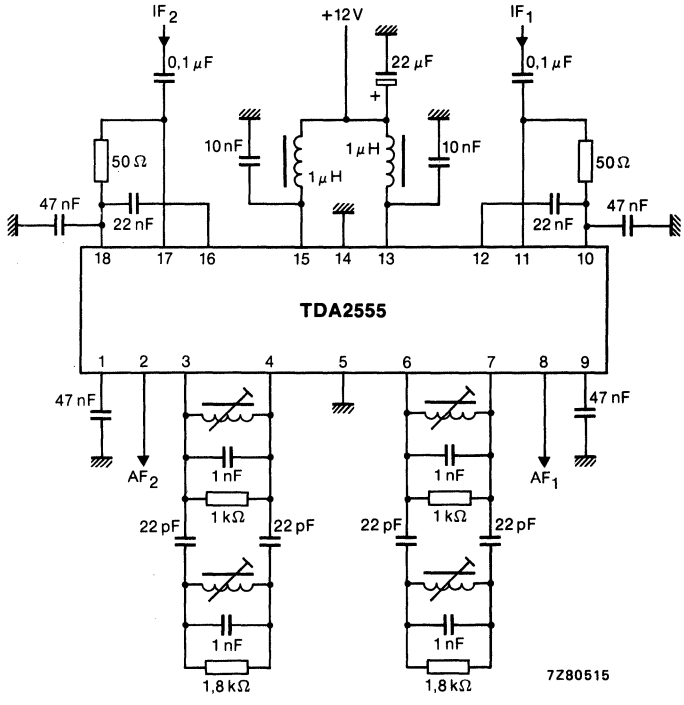

Fig. 2 Test circuit.

Sync Circuit with Vertical Oscillator and Driver — TDA2577A

GENERAL DESCRIPTION

The TDA2577A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector ($\varphi 2$) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6.5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 3% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical comparator with internal 3% pre-correction circuit for vertical oscillator/sawtooth generator
- Vertical driver stage
- Vertical blanking pulse generator with external adjustment of pulse duration (50 Hz: 21 lines; 60Hz: 17 lines)
- Vertical guard circuit

8

QUICK REFERENCE DATA

Supply			
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4 mA
Main supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
Supply current	$I_P = I_{10}$	typ.	55 mA
Input signals			
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5-9(p-p)}$	0.15 to 1	V
Output signals			
Horizontal output pulse (open collector) at I_{11} = 40 mA	V_{11-9}	<	0.5 V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	V_{1-9}	>	4 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

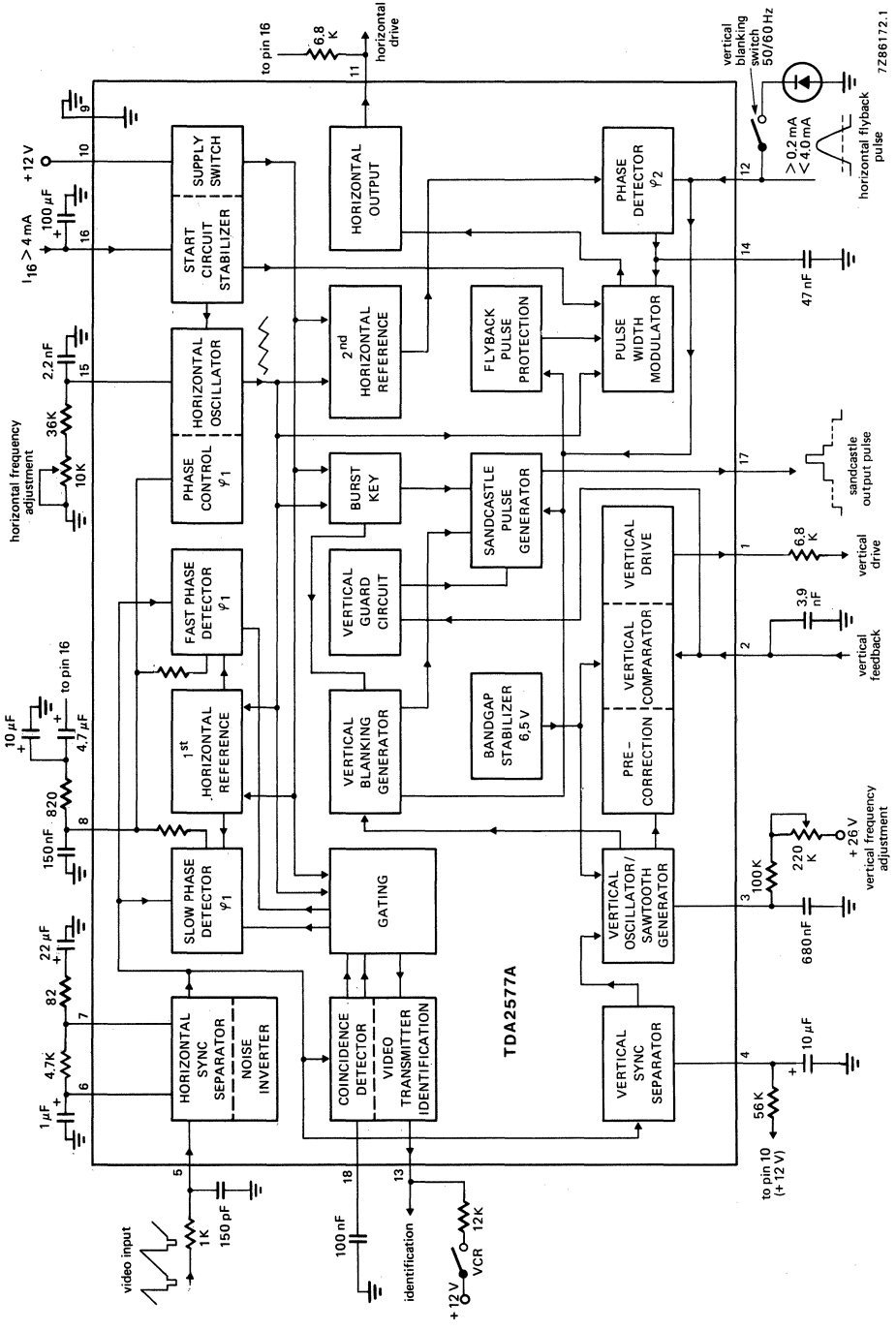

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8 mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	max.	13.2 V
Total power dissipation	P_{tot}	max.	1.1 W
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−25 to + 65 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	typ.	50 K/W

CHARACTERISTICS

I_{16} = 5 mA; V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}		4 to 8 mA
Stabilized supply voltage (pin 16)	V_{16-9}	typ.	8.7 V
			8.0 to 9.5 V
Supply current (pin 10)	I_{10}	typ.	55 mA
		<	70 mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
			10 to 13.2 V

Video input (pin 5)

Top-sync level	V_{5-9}	typ.	3.1 V
			1.5 to 3.75 V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5-9(p-p)}$	typ.	0.6 V
			0.15 to 1 V
Slicing level		typ.	50 %
			35 to 65 %
Delay between video input and detector output	t_1	typ.	0.35 µs

Noise gate (pin 5)

Switching level	V_{5-9}	typ.	0.7 V
		<	1 V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ.	± 800 Hz
Catching range	Δf	typ.	± 800 Hz
			± 600 to 1100 Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse			
for slow time constant		typ.	1 kHz/µs
for fast time constant		typ.	2 75 kHz/µs

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Sync Circuit with Vertical Oscillator and Driver | TDA2577A

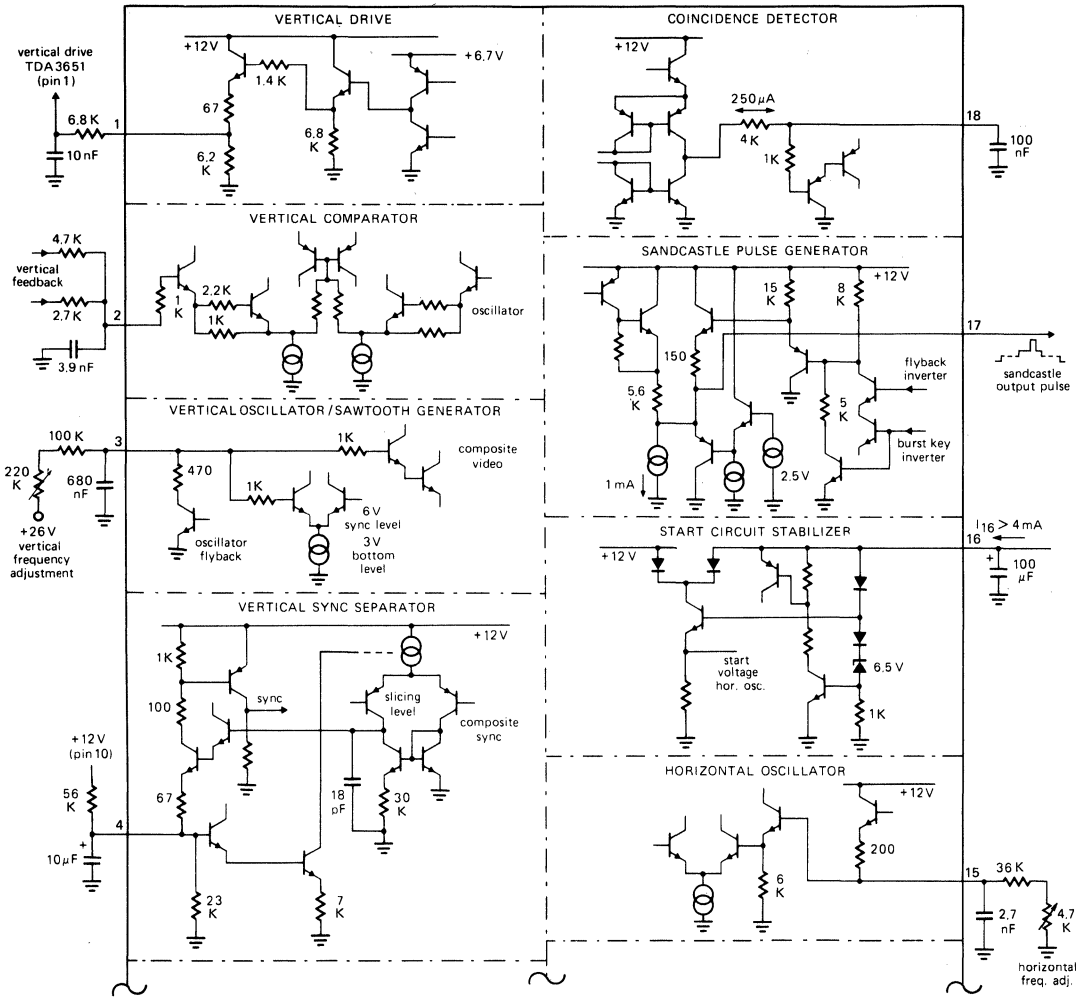

Fig. 2 TDA2577A Circuit Diagram.

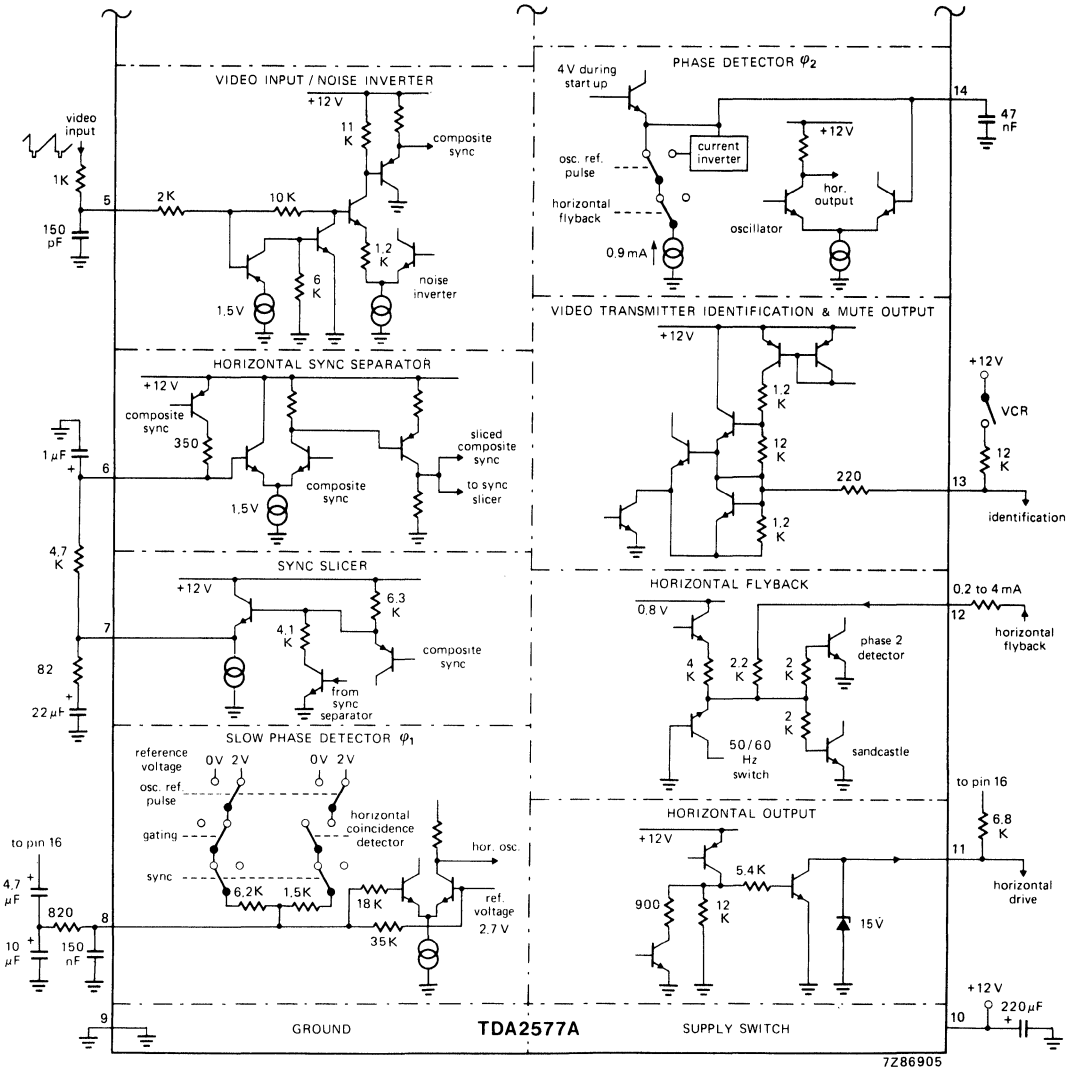

Fig. 2 TDA2577A Circuit Diagram. (Continued)

Second control loop (horizontal output to flyback; pin 14)				
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400	$\mu s/\mu s$
Control range	t_d		1 to 50	μs
Controlled edge	negative			
Phase adjustment (via 2nd control loop; pin 14)				
Control sensitivity		typ.	25	$\mu A/\mu s$
Maximum permissible control current	$\pm I_{14}$	<	50	μA
Horizontal oscillator (pin 15)				
Frequency (no sync)	f_{osc}	typ.	15 625	Hz
Frequency spread (C_{osc} = 2.2 nF; R_{osc} = 40 kΩ)	Δf_{osc}	<	4	%
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. <	6 8	% %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}
Horizontal output (pin 11)				
Output voltage; high level	$V_{11\text{-}9}$	<	13.2	V
Voltage at which protection starts	$V_{11\text{-}9}$		13 to 15.8	V
Output voltage; low level start condition at I_{11} = 10 mA	$V_{11\text{-}9}$	typ. <	0.3 0.5	V V
normal condition at I_{11} = 40 mA	$V_{11\text{-}9}$	typ. <	0.3 0.5	V V
Duty factor of output signal during starting (no phase shift; voltage at pin 11 low)	δ	typ.	65	%
Duty factor of output signal without flyback pulse	δ	typ. 	50 45 to 55	% %
Controlled edge	negative			
Duration of output pulse (see Fig. 3)			$t_d + t_o + 2.5$	μs
Sandcastle output pulse (pin 17)				
Output voltage during: burst key	$V_{17\text{-}9}$	>	10	V
horizontal blanking	$V_{17\text{-}9}$	typ. 	4.6 4.2 to 5	V V
vertical blanking	$V_{17\text{-}9}$	typ. 	2.5 2 to 3	V V
Pulse duration				
burst key	t_p	typ. 	4 3.6 to 4.4	μs μs
horizontal blanking	flyback pulse (see note 3)			
vertical blanking for 50 Hz application ($-I_{12}$: 0 to 0.1 mA) for 60 Hz application ($-I_{12}$: typ. 0.2 mA)			21 17	lines lines

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ.	4.9 μs
			4.5 to 5.3 μs
Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 2			
Detector output current	$\pm I_{18}$	typ.	300 μA
Voltage during noise (note 4)	$V_{18\text{-}9}$	typ.	0.3 V
Voltage level for in-sync condition	$V_{18\text{-}9}$	typ.	7.5 V
Switching level slow to fast	$V_{18\text{-}9}$	typ.	3.5 V
			3.2 to 3.8 V
Switching level mute function active; φ_1 fast to slow	$V_{18\text{-}9}$	typ.	1.2 V
			1.0 to 1.4 V
vertical period counter 3 periods fast	$V_{18\text{-}9}$	typ.	0.12 V
			0.08 to 0.16 V
Switching level slow to fast (locking) mute function inactive	$V_{18\text{-}9}$	typ.	1.7 V
			1.5 to 1.9 V
Switching level fast to slow (locking)	$V_{18\text{-}9}$	typ.	5.0 V
			4.7 to 5.3 V
Switching level for VCR (fast time constant) without mute function	$V_{18\text{-}9}$	typ.	8.6 V
			8.2 to 9.0 V
Video transmitter identification output (pin 13)			
Output voltage active (no sync) at I_{13} = 1 mA	$V_{13\text{-}9}$	>	10 V
		typ.	11 V
Output voltage active (no sync) at I_{13} = 5 mA	$V_{13\text{-}9}$	>	7 V
		typ.	10 V
Output voltage inactive	$V_{13\text{-}9}$	<	0.5 V
		typ.	0.1 V
VCR switching (pin 13)			
Input current for fast time constant phase detector φ_1, with mute function active	I_{13}	typ.	0.6 mA
			0.4 to 0.8 mA
Flyback input pulse (pin 12)			
Switching level	$V_{12\text{-}9}$	typ.	1 V
Input current	I_{12}		0.2 to 4 mA
Input pulse amplitude (peak-to-peak value)	$V_{12\text{-}9(p\text{-}p)}$	<	12 V
Input resistance	$R_{12\text{-}9}$	typ.	2.7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; t_{fl} = 12 μs (see also note 2 and Fig. 4)	t_o	typ.	1.3 μs

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Duration of vertical blanking pulse (pin 12)			
Required input current (negative)			
for 50 Hz application; 21 lines blanking	$-I_{12}$	typ.	0.2 mA
		>0.15 to <0.3	mA
for 60 Hz application; 17 lines blanking	$-I_{12}$	$<$	0.1 mA
Maximum allowed input current	$-I_{12}$	$<$	0.4 mA
Vertical sawtooth generator (pin 3)			
Vertical frequency (no sync)	f_s	typ.	46 Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 180 kΩ; at + 26 V)	Δf_s	$<$	4 %
Synchronization range		typ.	22 %
Input current at V_{3-9} = 6 V	I_3	$<$	2 μA
Frequency shift for V_P = 10 to 13 V	Δf_s	$<$	0.2 %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$ K^{-1}
Comparator (pin 2)			
Input voltage; d.c. level	V_{2-9}	typ.	4.4 V
			4.0 to 4.8 V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	1.6 V
Input current at V_{2-9} = 6 V	I_2	$<$	2 μA
Sawtooth internal pre-correction (parabolic convex)		typ.	3 %
Vertical output stage; emitter follower (pin 1)			
Output voltage at I_1 = 10 mA	V_{1-9}	typ.	3.6 V
			3.2 to 5 V
Output current	I_1	$<$	20 mA
Vertical guard circuit			
Activating voltage levels (vertical blanking level is 2.5 V)			
switching level low	V_{2-9}	typ.	3 V
			2.7 to 3.3 V
switching level high	V_{2-9}	typ.	5.7 V
			5.3 to 6.1 V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between negative transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.

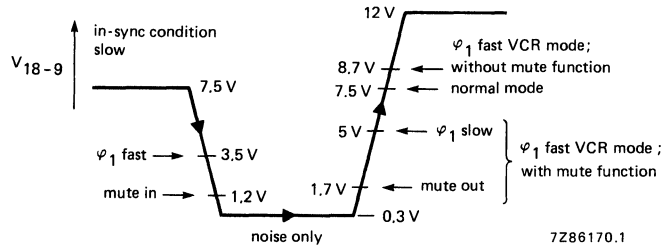

Fig. 3 Voltage levels at pin 18 (V_{18-9}).

APPLICATION INFORMATION

The TDA2577A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the negative-going edge of the horizontal output signal.

A bandgap reference voltage (6.5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4.7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3.1 V. The amplitude selective noise inverter is activated at a level of 0.7 V.

8

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking interval of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

APPLICATION INFORMATION (continued)

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector $\varphi 1$				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7.5 V	X		X			X	video signal detected
7.5 to 3.5 V	X		X			X	video signal detected
3.5 to 1.2 V		X		X		X	video signal detected
1.2 to 0.1 V	X		X		X		noise only
0.1 to 1.7 V	X	*	X	*	X		new video signal detected
1.7 to 5.0 V		X		X		X	horizontal oscillator locked VCR playback with mute function
5.0 to 7.5 V	X		X			X	horizontal oscillator locked
8.7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5.5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0.1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1.2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground. Also a current of 0.6 mA into pin 13 sets the first phase detector to fast without affecting the mute output function (active HIGH with no video signal detected). For VCR playback without mute function, the first phase detector can be set to fast by connecting a resistor of 1 kΩ to the supply (pin 10).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 3.5 mA, which will result in a supply voltage of about 5.5 V (for guaranteed operation of all devices $I_{16} > 4$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5.5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8.8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8.7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays

in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally precorrected by 3% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6.5 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4.6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2.5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration is set by the negative voltage value of the horizontal flyback pulse at pin 12.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3 V or higher than 5.8 V, the guard circuit will insert a continuous level of 2.5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

APPLICATION INFORMATION (continued)

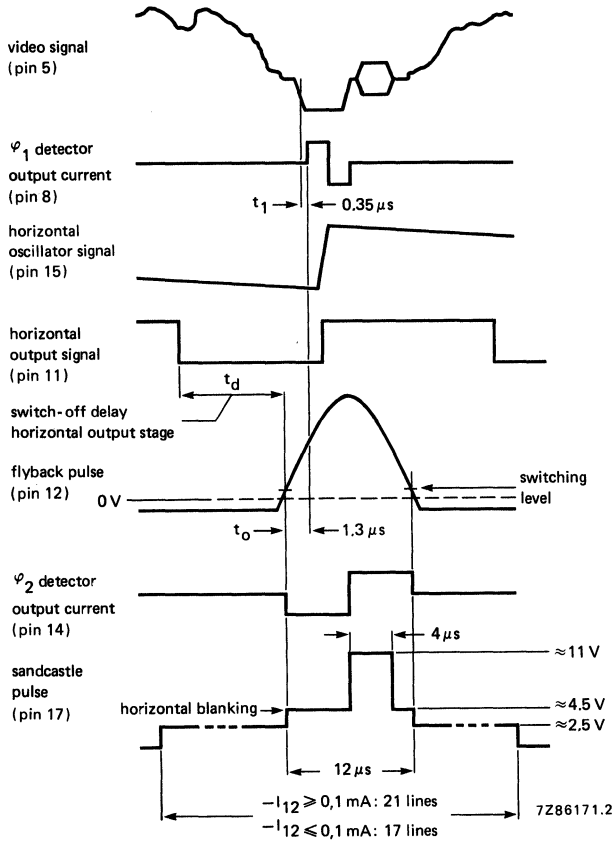

Fig. 4 Timing diagram of the TDA2577A.

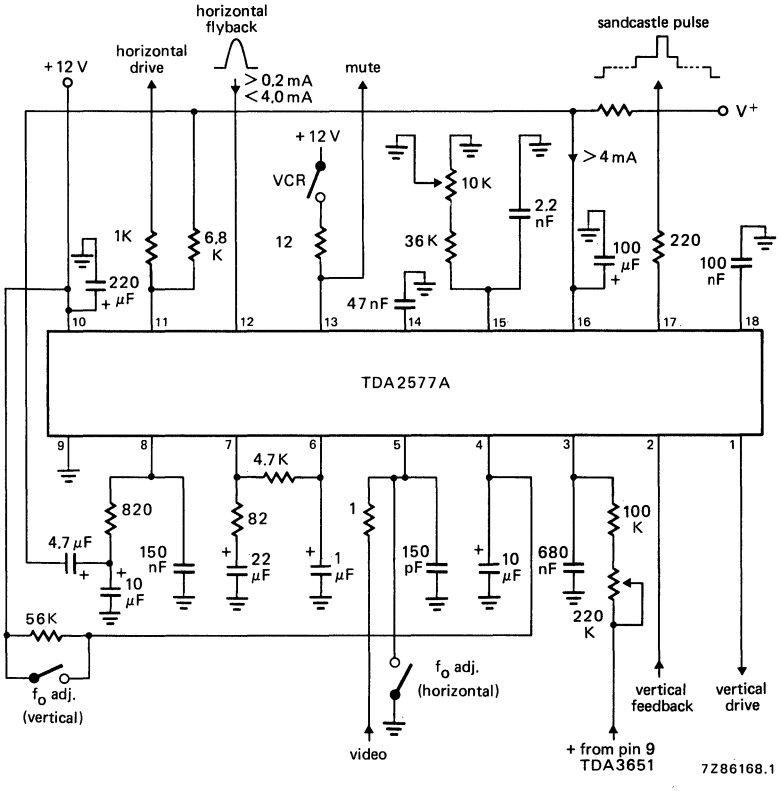

Fig. 5 Typical application circuit diagram; for combination of the TDA2577A with the TDA3651 see Fig. 7.

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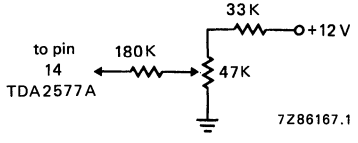

Fig. 6 Circuit configuration at pin 14 for phase adjustment.

APPLICATION INFORMATION (continued)

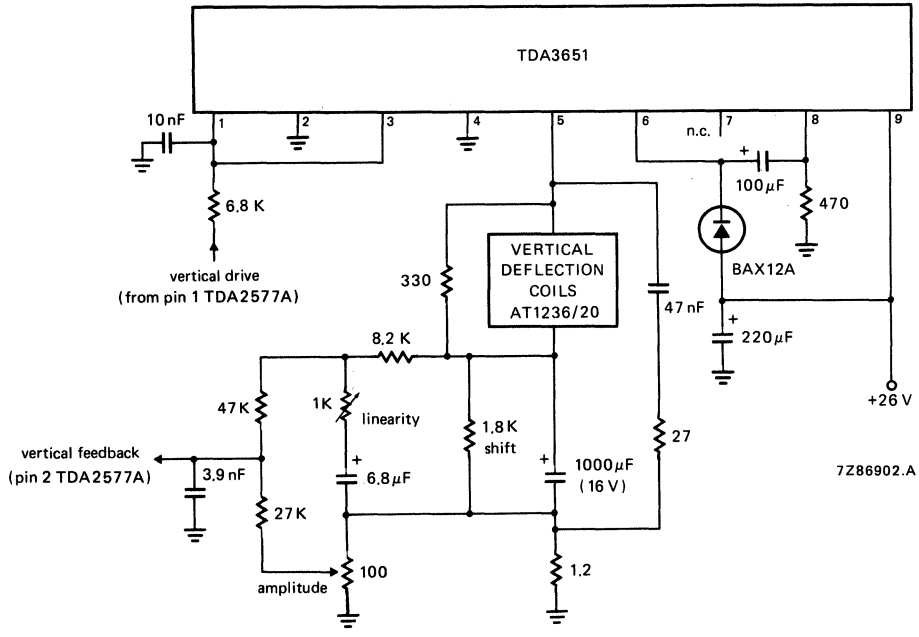

Fig. 7 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2577A (90° application).

Sync Circuit with Vertical Oscillator and Driver — TDA2578A

GENERAL DESCRIPTION

The TDA2578A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector (φ_2) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6.5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 6% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical driver stage
- Vertical blanking pulse generator
- 50/60 Hz detector
- 50/60 Hz identification output
- Automatic amplitude adjustment for 60 Hz
- Automatic adjustment of blanking pulse duration (50 Hz: 21 lines; 60 Hz: 17 lines)
- Vertical guard curcuit

8

QUICK REFERENCE DATA

Supply			
Minimum current required to start horizontal oscillator and output stage (pin 16)	I_{16}	>	4 mA
Main supply voltage (pin 10)	$V_P = V_{10-9}$	typ.	12 V
Supply current	$I_P = I_{10}$	typ.	55 mA
Input signals			
Sync pulse input voltage (peak-to-peak value; negative-going)	$V_{5-9(p-p)}$		0.15 to 1 V
Output signals			
Horizontal output pulse (open collector) at I_{11} = 40 mA	V_{11-9}	<	0.5 V
Vertical output pulse (emitter-follower) at I_1 = 10 mA	V_{1-9}	>	4 V

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

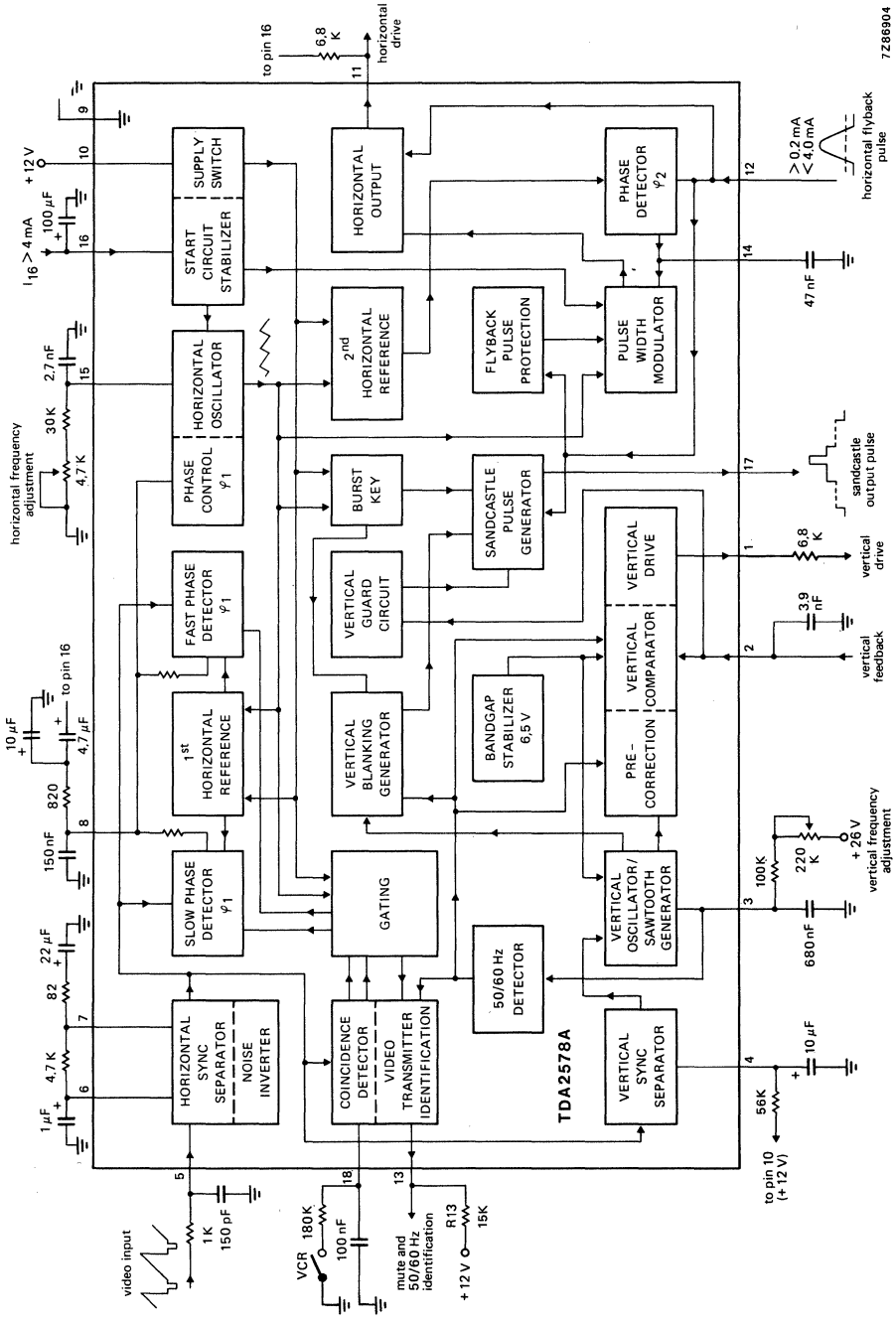

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Start current (pin 16)	I_{16}	max.	8 mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	max.	13.2 V
Total power dissipation	P_{tot}	max.	1.1 W
Storage temperature range	T_{stg}	−55 to +	150 °C
Operating ambient temperature range	T_{amb}	−25 to +	65 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	typ.	50 K/W

CHARACTERISTICS

I_{16} = 5 mA; V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

Supply

Supply current at pin 16	I_{16}	4 to 8	mA
Stabilized supply voltage (pin 16)	V_{16-9}	typ. 8.7 8.0 to 9.5	V V
Supply current (pin 10)	I_{10}	typ. 55 < 70	mA mA
Supply voltage (pin 10)	$V_P = V_{10-9}$	typ. 12 10 to 13.2	V V

Video input (pin 5)

Top-sync level	V_{5-9}	typ. 3.1 1.5 to 3.75	V V
Sync pulse amplitude (peak-to-peak value) (note 1)	$V_{5-9(p-p)}$	typ. 0.6 0.15 to 1	V V
Slicing level		typ. 50 35 to 65	% %
Delay between video input and detector output	t_1	typ. 0.35	µs

Noise gate (pin 5)

Switching level	V_{5-9}	typ. 0.7 < 1	V V

First control loop (sync to oscillator; pin 8)

Holding range	Δf	typ. ± 800	Hz
Catching range	Δf	typ. ± 800 ± 600 to 1100	Hz Hz
Control sensitivity video with respect to oscillator, burst key and flyback pulse			
for slow time constant		typ. 1	kHz/µs
for fast time constant		typ. 2.75	kHz/µs

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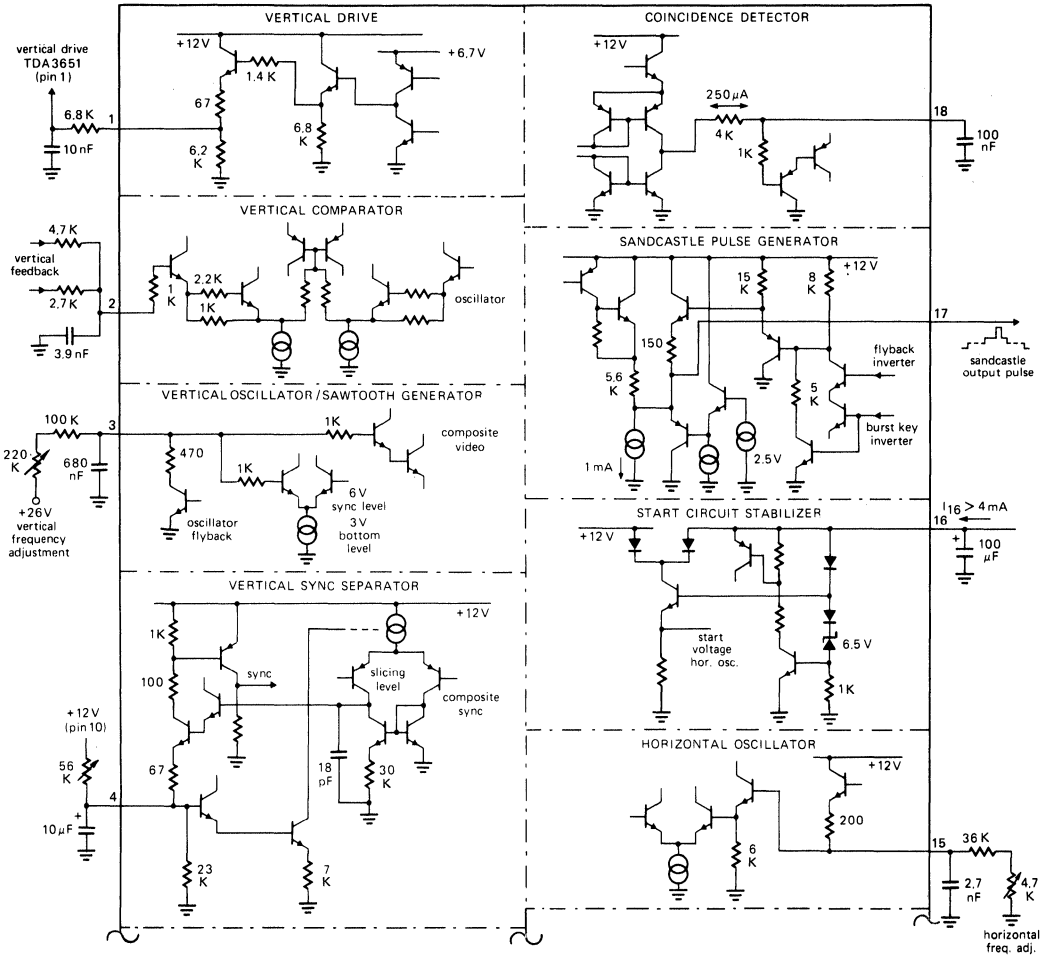

Fig. 2 TDA2578A Circuit diagram.

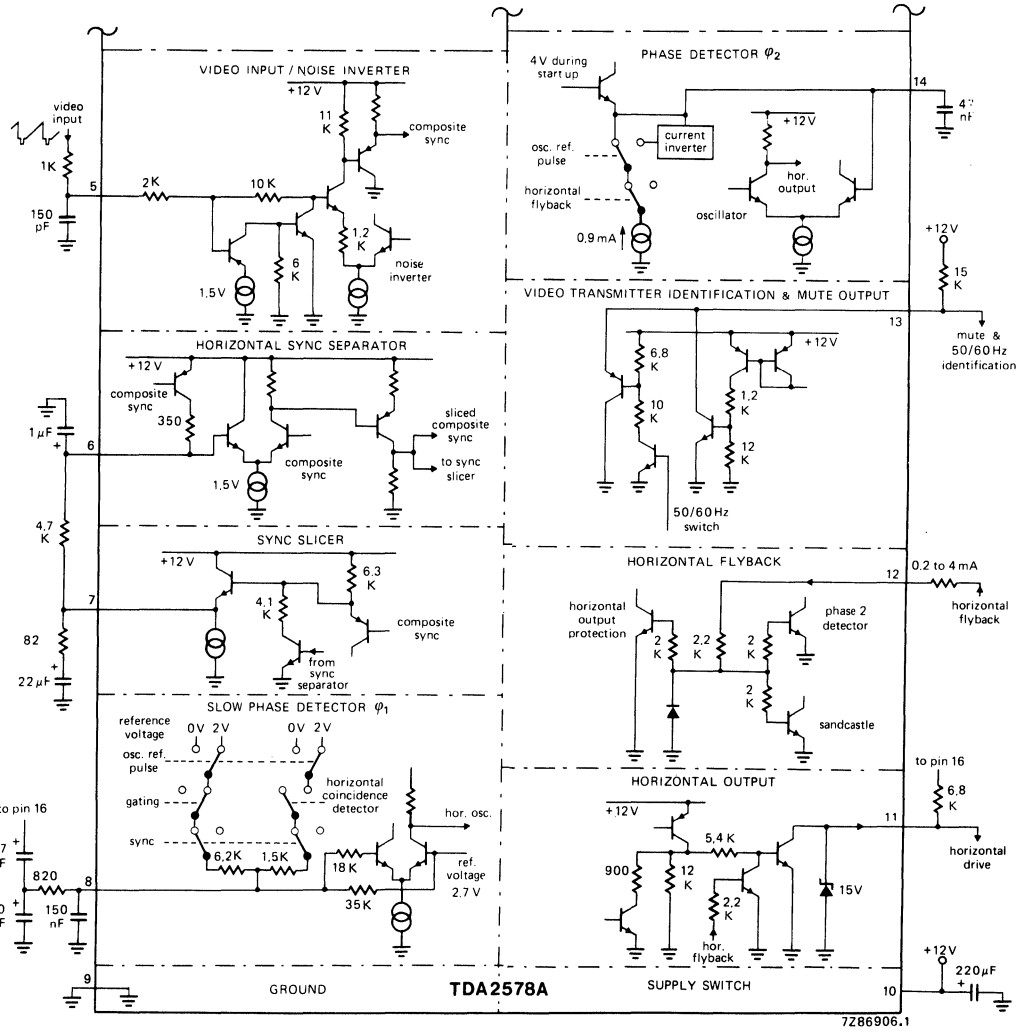

Fig. 2 TDA2578A Circuit diagram. (Continued)

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Second control loop (horizontal output to flyback; pin 14)				
Control sensitivity; static (see note 2)	$\Delta t_d/\Delta t_o$	typ.	400	$\mu s/\mu s$
Control range	t_d		1 to 45	μs
Controlled edge	positive			
Phase adjustment (via 2nd control loop; pin 14)				
Control sensitivity		typ.	25	$\mu A/\mu s$
Maximum permissible control current	$\pm I_{14}$	<	50	μA
Horizontal oscillator (pin 15)				
Frequency (no sync)	f_{osc}	typ.	15 625	Hz
Frequency spread (C_{osc} = 2,7 nF; R_{osc} = 33 kΩ; no sync)	Δf_{osc}	<	4	%
Frequency deviation between starting point of output signal and stabilized condition	Δf_{osc}	typ. <	6 8	% %
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}
Horizontal output (pin 11)				
Output voltage; high level	V_{11-9}	<	13.2	V
Voltage at which protection starts	V_{11-9}		13 to 15.8	V
Output voltage; low level start condition at I_{11} = 10 mA	V_{11-9}	typ. <	0.3 0.5	V V
normal condition at I_{11} = 40 mA	V_{11-9}	typ. <	0.3 0.5	V V
Duty factor of output signal during starting (no phase shift) I_{16} = 4 mA (voltage at pin 11 low)	δ	typ.	65	%
Duty factor of output signal without flyback pulse	δ	typ.	50 45 to 55	% %
Controlled edge	positive			
Duration of output pulse (see Fig. 4)	t_d + horizontal flyback pulse			
Sandcastle output pulse (pin 17)				
Output voltage during: burst key	V_{17-9}	>	10	V
horizontal blanking	V_{17-9}	typ.	4.6 4.2 to 5	V V
vertical blanking	V_{17-9}	typ.	2.5 2 to 3	V V
Pulse duration burst key	t_p	typ.	4 3.6 to 4.4	μs μs
horizontal blanking	flyback pulse (see note 3)			
vertical blanking at 50 Hz at 60 Hz	 21 lines 17 lines			

CHARACTERISTICS (continued)

Delay between the start of the sync at the video input and the rising edge of the burst key pulse	t_2	typ.	4.9 μs 4.5 to 5.3 μs
Coincidence detector; video transmitter identification circuit; time constant switches (pin 18); see also Fig. 3			
Detector output current	$\pm I_{18}$	typ.	300 μA
Voltage during noise (note 4)	V_{18-9}	typ.	0.3 V
Voltage level for in-sync condition	V_{18-9}	typ.	7.5 V
Switching level slow to fast	V_{18-9}	typ.	3.5 V 3.2 to 3.8 V
Switching level mute function active; φ_1 fast to slow	V_{18-9}	typ.	1.2 V 1 0 to 1.4 V
vertical period counter 3 periods fast	V_{18-9}	typ.	0.12 V 0.08 to 0.16 V
Switching level slow to fast (locking) mute function inactive	V_{18-9}	typ.	1.7 V 1.5 to 1.9 V
Switching level fast to slow (locking)	V_{18-9}	typ.	5.0 V 4.7 to 5.3 V
Switching level for VCR (fast time constant) without mute function	V_{18-9}	typ.	8.6 V 8.2 to 9 0 V
Video transmitter identification output (pin 13)			
Output voltage active (no sync) at I_{13} = 1 mA	V_{13-9}	<	0.5 V
		typ.	0.3 V
Sink current active (no sync)	I_{13}	⩽	5 mA
Output current inactive (sync: 50 Hz)	I_{13}	<	1 μA
50/60 Hz identification (pin 13)			
R13 = 15 kΩ to + 12 V (note 5) at f = 50 Hz (in sync condition)	V_{13-9}	typ.	V_{10-9} V
at f = 60 Hz (in sync condition)	V_{13-9}	typ.	7.6 V 7.2 to 8 V
Flyback input pulse (pin 12)			
Switching level	V_{12-9}	typ.	1 V
Input current	I_{12}		0.2 to 4 mA
Input pulse amplitude (peak-to-peak value)	$V_{12-9(p-p)}$	<	12 V
Input resistance	R_{12-9}	typ.	2.7 kΩ
Delay time of sync pulse (measured in φ_1) to flyback at switching level; t_{fl} = 12 μs (see also note 2 and Fig. 4)	t_o	typ.	1.3 μs

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Vertical sawtooth generator (pin 3)				
Vertical frequency (no sync)	f_s	typ.	46	Hz
Frequency spread (C_{osc} = 680 nF; R_{osc} = 180 kΩ; at + 26 V)	Δf_s	<	4	%
Synchronization range (note 6)		typ.	33	%
Input current at V_{3-9} = 6 V	I_3	<	3	μA
Frequency shift for V_P = 10 to 13 V	Δf_s	<	0.2	%
Temperature coefficient	TC	typ.	$1 \cdot 10^{-4}$	K^{-1}
Comparator (pin 2)				
Input voltage; d.c. level	V_{2-9}	typ. 4.0 to 4.8	4.4	V V
a.c. level (peak-to-peak value)	$V_{2-9(p-p)}$	typ.	0.8	V
Input current at V_{2-9} = 6 V	I_2	<	2	μA
Sawtooth internal pre-correction (parabolic convex)		typ.	6	%
Vertical output stage; emitter follower (pin 1)				
Output voltage at I_1 = 10 mA	V_{1-9}	typ. 3.2 to 5		V V
Output current	I_1	<	20	mA
Vertical guard circuit				
Activating voltage levels (vertical blanking level is 2.5 V) switching level low	V_{2-9}	typ. 3.0 to 3.7	3.35	V V
switching level high	V_{2-9}	typ. 4.75 to 5.55	5.15	V V

Notes to characteristics

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. t_d = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
   t_o = delay between the rising edge of the flyback pulse and the start of the current in φ_1 (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V (t_{fl}).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5-9} \approx 5$ V.
5. For 60 Hz a p-n-p emitter clamp is activated.
6. When f_o = 46 Hz the 50/60 Hz detector switches over to 60 Hz; video input signal at pin 5 ≈ 55 Hz.

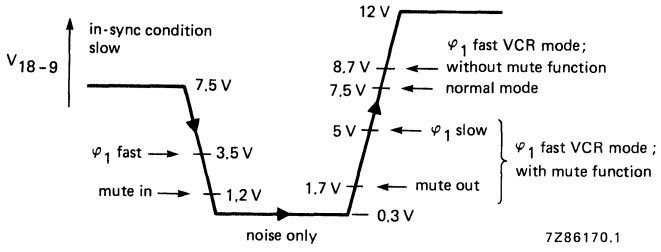

Fig. 3 Voltage levels at pin 18 (V_{18-9}).

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APPLICATION INFORMATION

The TDA2578A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector (φ_2) is activated to control the timing of the positive-going edge of the horizontal output signal.

A bandgap reference voltage (6.5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4.7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3.1 V. The amplitude selective noise inverter is activated at a level of 0.7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking internal of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

Table 1 Switching levels at pin 18.

voltage at pin 18	first phase detector φ_1				mute output at pin 13		receiving conditions
	time constant		gating				
	slow	fast	on	off	on	off	
7.5 V	X		X			X	video signal detected
7.5 to 3.5 V	X		X			X	video signal detected
3.5 to 1.2 V		X		X		X	video signal detected
1.2 to 0.1 V	X		X		X		noise only
0.1 to 1.7 V	X	*	X	*	X		new video signal detected
1.7 to 5.0 V		X		X		X	horizontal oscillator locked VCR playback with mute function
5.0 to 7.5 V	X		X			X	horizontal oscillator locked
8.7 V		X		X		X	VCR playback without mute function

Where: * = 3 vertical periods.

APPLICATION INFORMATION (continued)

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5.5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0.1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1.2 V is reached within 5 ms (C_{18} = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground (see Fig. 7).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 3.6 mA, which will result in a supply voltage of about 5.5 V (for guaranteed operation of all devices $I_{16} > 4$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5.5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8.8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8.7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally pre-corrected by 6% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6.7 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4.6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2.5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration and sawtooth amplitude is automatically adjusted via the 50/60 Hz detector.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3.35 V or higher than 5.15 V, the guard circuit will insert a continuous level of 2.5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

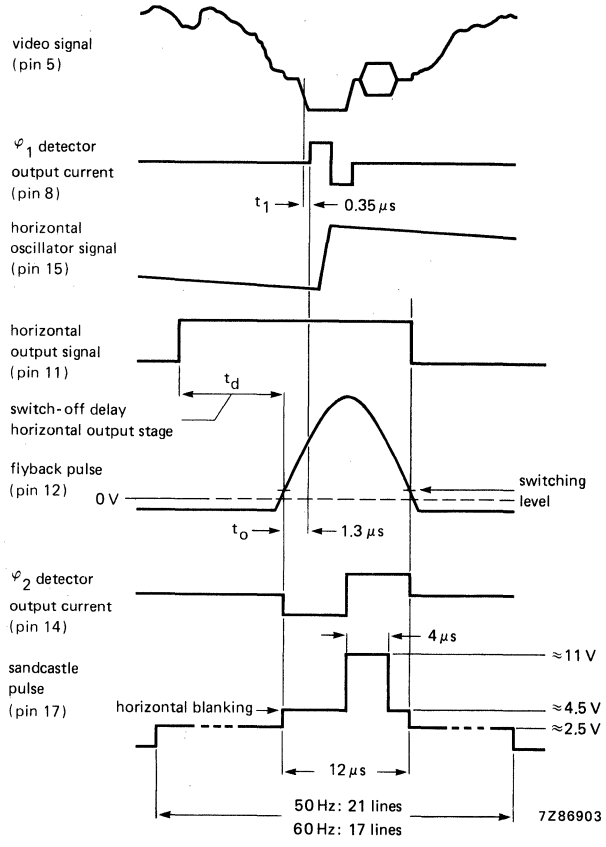
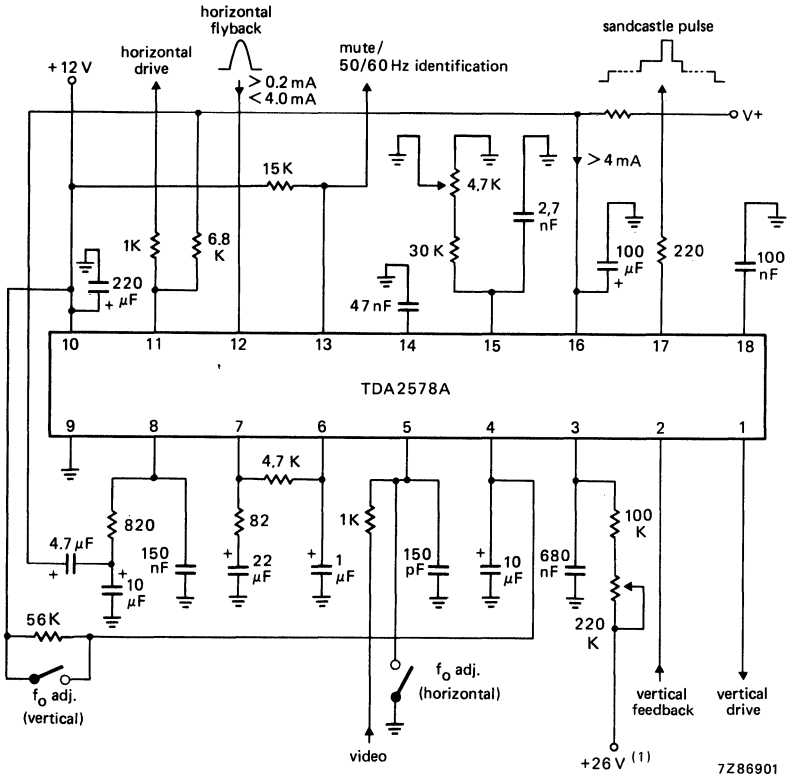


Fig. 4 Timing diagram of the TDA2578A.

APPLICATION INFORMATION (continued)



(1) ⩾ 26 V for linear scan.

Fig. 5 Typical application circuit diagram; for application of the TDA2578A with the TDA3651 see Fig. 8.

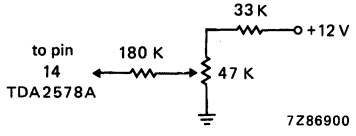


Fig. 6 Circuit configuration at pin 14 for phase adjustment.

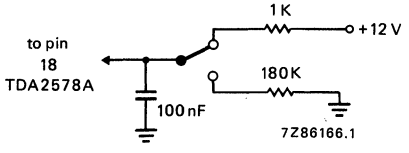


Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
180 kΩ between pin 18 and ground: with mute function.

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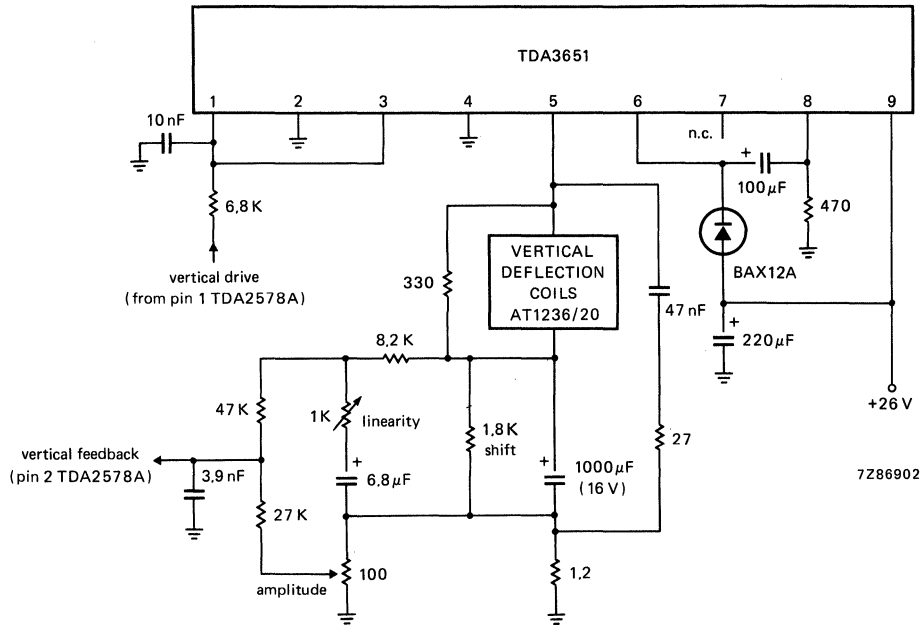


Fig. 8 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2578A, (90° application).

Sync Circuit with Vertical Oscillator and Driver (with Horizontal Output)

TDA2579

DESCRIPTION

The TDA2579 is a synchronization circuit with synchronized vertical divider system and horizontal and vertical output stages.

FEATURES

- **Horizontal sync. separator and noise inverter**
- **Horizontal oscillator**
- **Horizontal output stage**
- **Horizontal phase detector (sync. to oscillator)**
- **Slow phase detector time constant and gated sync. pulse operation are automatically switched on by an internal sync. pulse noise level detection circuit**
- **Slow time constant for noise only conditions**
- **Time constant externally switchable**
- **Sandcastle pulse generator (3 levels)**
- **Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the main's rectifier.**
- **The duty cycle of the horizontal output pulse is 50% when the horizontal flyback pulse is absent.**
- **Vertical synchronization pulse separator without external components and 2 integration times.**
- **Zener diode reference voltage source for the vertical sawtooth-generator and vertical comparator.**
- **50/60 Hz detection system**
- **50/60 Hz identification output combined with mute function.**
- **Automatic amplitude adjustment for 50Hz and 60Hz**
- **Automatic adjustment of blanking pulse duration in 50Hz: 42 clockpulses; 60Hz: 34 clockpulses**
- **Guard circuit which generates the frame blanking level on the sandcastle output pin 17 when the feedback level at pin 2 is not within the specified limits**

APPLICATIONS

- **Video monitors**
- **Graphics**
- **Color printers**
- **TV receivers**

8

Sync Circuit with Vertical Oscillator and Driver (with Horizontal Output)

TDA2579

ORDERING CODE

	PINS	PACKAGE	NOTE
TDA2579	18	Plastic DIP	SOT-102HE

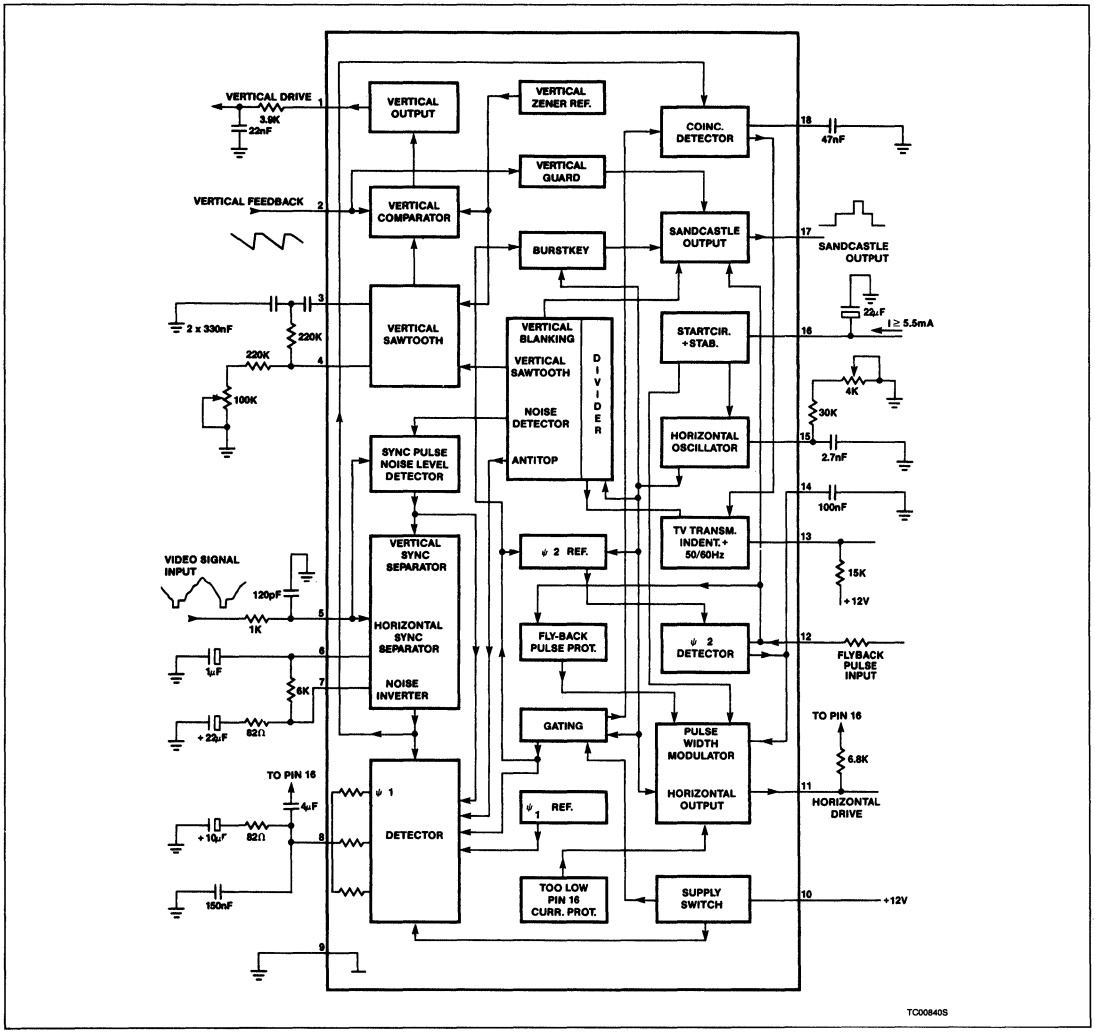
REFERENCE DATA

PARAMETER	TYPICAL	UNIT
Min. required current for starting horizontal oscillator + output stage, $I_{pin\ 16}$	0.5	mA
Main supply voltage, $V_{pin\ 10}$ Supply current, $I_{pin\ 10}$	12 typ 65	V mA
Sync. pulse input amplitude, $V_{pin\ 5-9pp}$	0.1-1	V
Horizontal output (open collector) I_{pin} 11–40mA, $V_{pin\ 11}$	0.5	V
Vertical output stage driver (emitter follower) I_{pin} 1–1.5mA, $V_{pin\ 11}$	5	V

Sync Circuit with Vertical Oscillator and Driver (with Horizontal Output)

TDA2579

BLOCK DIAGRAM



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Horizontal Combination — TDA2593

The TDA2593 is a monolithic integrated circuit intended for use in colour television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3500, TDA3510 and TDA3520. The circuit incorporates the following functions:

- horizontal oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage (φ_1)
- internal key pulse for phase detector (φ_1) (additional noise limiting)
- phase comparison between line flyback pulse and oscillator voltage (φ_2)
- larger catching range obtained by coincidence detector (φ_3; between sync and key pulse)
- switch for changing the filter characteristic and the gate circuit (VCR-operation)
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage with separate supply voltage for direct drive of thyristor deflection circuits
- low supply voltage protection

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}16}$	typ.	12 V
Supply current	I_1	typ.	30 mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{9\text{-}16(p\text{-}p)}$		3 to 4 V
Noise separator input voltage (peak-to-peak value)	$V_{10\text{-}16(p\text{-}p)}$		3 to 4 V
Pulse duration switch input voltage			
at t = 7 μs (thyristor driving)	$V_{4\text{-}16}$		9.4 to $V_{1\text{-}16}$ V
at t = 14 μs + t_d (transistor driving)	$V_{4\text{-}16}$		0 to 3.5 V
at t = 0 (input 4 open or $V_{3\text{-}16} = 0$)	$V_{4\text{-}16}$		5.4 to 6.6 V
Output signals			
Vertical sync output pulse (peak-to peak value)	$V_{8\text{-}16(p\text{-}p)}$	typ.	11 V
Burst gating output pulse (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	typ.	11 V
Line drive pulse (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10.5 V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

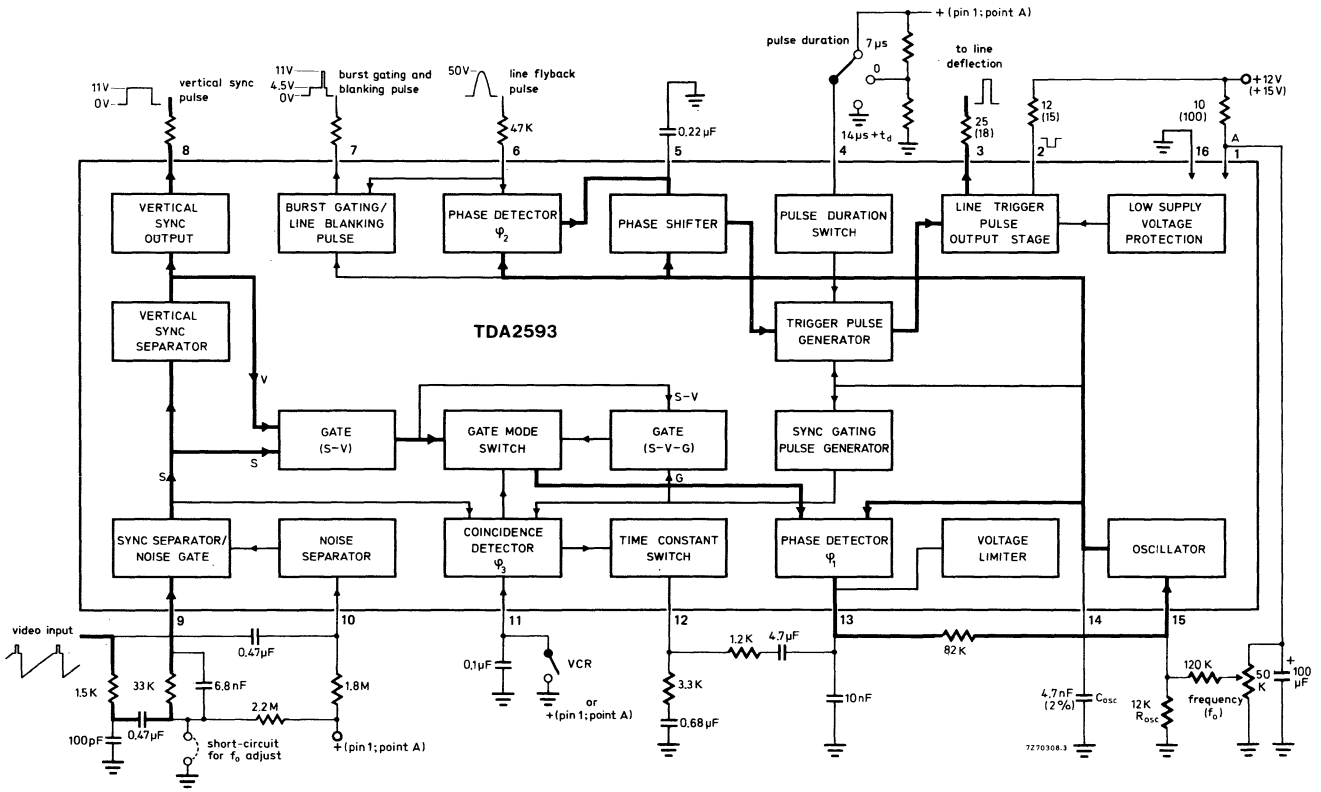

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage				
at pin 1 (voltage source)	V_{1-16}	max.	13.2	V
at pin 2	V_{2-16}	max.	18	V
Voltages				
Pin 4	V_{4-16}	max.	13.2	V
Pin 9	$\pm V_{9-16}$	max.	6	V
Pin 10	$\pm V_{10-16}$	max.	6	V
Pin 11	V_{11-16}	max.	13.2	V
Currents				
Pins 2 and 3 (thyristor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	650	mA
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400	mA
Pin 4	I_4	max.	1	mA
Pin 6	$\pm I_6$	max.	10	mA
Pin 7	$-I_7$	max.	10	mA
Pin 11	I_{11}	max.	2	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−25 to + 125	°C
Operating ambient temperature	T_{amb}		−20 to + 70	°C

CHARACTERISTICS at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

Sync separator

Input switching voltage	V_{9-16}	typ.	0.8	V
Input keying current	I_9		5 to 100	μA
Input leakage current at $V_{9-16} = -5$ V	I_9	<	1	μA
Input switching current	I_9	⩽	5	μA
Switch off current	I_9	>	100	μA
		typ.	150	μA
Input signal (peak-to-peak value)	$V_{9-16(p-p)}$		3 to 4	V*

* Permissible range 1 to 7 V.

Noise separator				
Input switching voltage	V_{10-16}	typ.	1.4	V
Input keying current	I_{10}		5 to 100	μA
Input switching current	I_{10}	>	100	μA
		typ.	150	μA
Input leakage current at $V_{10-16} = -5$ V	I_{10}	<	1	μA
Input signal (peak-to-peak value)	$V_{10-16(p-p)}$		3 to 4	V *
Permissible superimposed noise signal (peak-to-peak value)	$V_{10-16(p-p)}$	<	7	V
Line flyback pulse				
Input current	I_6	typ.	1	mA
			0.02 to 2	mA
Input switching voltage	V_{6-16}	typ.	1.4	V
Input limiting voltage	V_{6-16}		−0.7 to + 1.4	V
Switching on VCR				
Input voltage	V_{11-16}		0 to 2.5	V
	V_{11-16}		9 to V_{1-16}	V
Input current	$-I_{11}$	<	200	μA
	I_{11}	<	2	mA
Pulse duration switch				
For t = 7 μs (thyristor driving)				
Input voltage	V_{4-16}		9.4 to V_{1-16}	V
Input current	I_4	>	200	μA
For t = 14 μs + t_d (transistor driving)				
Input voltage	V_{4-16}		0 to 3.5	V
Input current	$-I_4$	>	200	μA
For t = 0; $V_{3-16} = 0$ or input pin 4 open				
Input voltage	V_{4-16}		5.4 to 6.6	V
Input current	I_4	typ.	0	μA

* Permissible range 1 to 7 V.

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Vertical sync pulse (positive-going)			
Output voltage (peak-to-peak value)	$V_{8\text{-}16(p\text{-}p)}$	>	10 V
		typ.	11 V
Output resistance	R_8	typ.	2 kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15 μs
Delay between trailing edge of input and output signal	t_{off}	typ.	t_{on} μs
Burst gating pulse (positive-going)			
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$	>	10 V
		typ.	11 V
Output resistance	R_7	typ.	70 Ω
Pulse duration; $V_{7\text{-}16}$ = 7 V	t_p	typ.	4 μs
			3.7 to 4.3 μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; $V_{7\text{-}16}$ = 7 V	t	typ.	2.65 μs
			2.15 to 3.15 μs
Output trailing edge current	I_7	typ.	2 mA
Line flyback-blanking pulse (positive-going)			
Output voltage (peak-to-peak value)	$V_{7\text{-}16(p\text{-}p)}$		4 to 5 V
Output resistance	R_7	typ.	70 Ω
Output trailing edge current	I_7	typ.	2 mA
Line drive pulse (positive-going)			
Output voltage (peak-to-peak value)	$V_{3\text{-}16(p\text{-}p)}$	typ.	10.5 V
Output resistance			
for leading edge of line pulse	R_3	typ.	2.5 Ω
for trailing edge of line pulse	R_3	typ.	20 Ω
Pulse duration (thyristor driving)			
$V_{4\text{-}16}$ = 9.4 to $V_{1\text{-}16}$ V	t_p	typ.	7 μs
			5.5 to 8.5 μs
Pulse duration (transistor driving)			
$V_{4\text{-}16}$ = 0 to 4 V; t_{fp} = 12 μs	t_p		14 + t_d μs*
Supply voltage for switching off the output pulse	$V_{1\text{-}16}$	typ.	4 V
Overall phase relation			
Phase relation between middle of sync pulse and the middle of the flyback pulse	t	typ.	2.6 μs**
Tolerance of phase relation	$\lvert \Delta t \rvert$	<	0.7 μs

* t_d = switch-off delay of line output stage.
** Line flyback pulse duration t_{fp} = 12 μs.

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2. If additional adjustment is applied it can be arranged by current supply at pin 5 such that	$\Delta I_5/\Delta t$	typ.	30	$\mu A/\mu s$
Oscillator				
Threshold voltage low level	$V_{14\text{-}16}$	typ.	4.4	V
Threshold voltage high level	$V_{14\text{-}16}$	typ.	7.6	V
Discharge current	$\pm I_{14}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4.7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15.625	kHz
Spread of frequency	$\Delta f_o/f_o$	<	± 5	%*
Frequency control sensitivity	$\Delta f_o/\Delta I_{15}$	typ.	31	$Hz/\mu A$
Adjustment range of network in circuit (Fig. 1)	$\Delta f_o/f_o$	typ.	± 10	%
Influence of supply voltage on frequency	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	<	± 0.05	%*
Change of frequency when $V_{1\text{-}16}$ drops to 5 V	Δf_o	<	± 10	%*
Temperature coefficient of oscillator frequency		<	$\pm 10^{-4}$	Hz/K*
Phase comparison φ_1				
Control voltage range	$V_{13\text{-}16}$		3.8 to 8.2	V
Control current (peak value)	$\pm I_{13M}$		1.9 to 2.3	mA
Output leakage current at $V_{13\text{-}16}$ = 4 to 8 V	I_{13}	<	1	μA
Output resistance at $V_{13\text{-}16}$ = 4 to 8 V	R_{13}	high ohmic		**
at $V_{13\text{-}16}$ < 3.8 V or > 8.2 V	R_{13}	low ohmic		▲
Control sensitivity		typ.	2	$kHz/\mu s$
Catching and holding range (82 kΩ beteeen pins 13 and 15)	Δf	typ.	± 780	Hz
Spread of catching and holding range	$\Delta(\Delta f)$	typ.	± 10	%*

* Excluding external component tolerances.
** Current source.
▲ Emitter follower.

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Phase comparison φ_2 and phase shifter				
Control voltage range	$V_{5\text{-}16}$		5.4 to 7.6	V
Control current (peak value)	$\pm I_{5M}$	typ.	1	mA
Output resistance				
at $V_{5\text{-}16}$ = 5.4 to 7.6 V		high ohmic		*
at $V_{5\text{-}16} < 5.4$ V or > 7.6 V	R_5	typ.	8	kΩ
Input leakage current				
$V_{5\text{-}16}$ = 5.4 to 7.6 V	I_5	<	5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	<	15	μs
Static control error	$\Delta t/\Delta t_d$	<	0.2	%
Coincidence detector φ_3				
Output voltage	$V_{11\text{-}16}$		0.5 to 6	V
Output current (peak value)				
without coincidence	I_{11M}	typ.	0.1	mA
with coincidence	$-I_{11M}$	typ.	0.5	mA
Time constant switch				
Output voltage	$V_{12\text{-}16}$	typ.	6	V
Output current (limited)	$\pm I_{12}$	<	1	mA
Output resistance				
at $V_{11\text{-}16}$ = 2.5 to 7 V	R_{12}	typ.	0.1	kΩ
at $V_{11\text{-}16} < 1.5$ V or > 9 V	R_{12}	typ.	60	kΩ
Internal gating pulse				
Pulse duration	t_p	typ.	7.5	μs

* Current source.

Horizontal Combination | TDA2594

The TDA2594 is a monolithic integrated circuit intended for use in colour television receivers. The circuit incorporates the following functions:

- Horizontal oscillator based on the threshold switching principle.
- Phase comparison between sync pulse and oscillator voltage (φ_1).
- Internal key pulse for phase detector (φ_1) (additional noise limiting).
- Phase comparison between line flyback pulse and oscillator voltage (φ_2).
- Larger catching range obtained by coincidence detector (φ_3; between sync and key pulse).
- Switch for changing the filter characteristic and the gate circuit (VCR-operation).
- Sync separator.
- Noise separator.
- Vertical sync separator and output stage.
- Colour burst keying and line flyback blanking pulse generator and clamp circuit for vertical blanking.
- Phase shifter for the output pulse.
- Output pulse duration for transistor deflection systems.
- External switching off of the line trigger pulse.
- Output stage with separate supply voltage.
- Low supply voltage protection.
- Transmitter identification and muting circuit, and vertical sync switch-off.

QUICK REFERENCE DATA

Supply voltage	$V_{1-18} = V_S$	typ. 12	V
Supply current	I_1	typ. 30	mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{11-18(p-p)}$	typ. 3	V*
Noise separator input voltage (peak-to-peak value)	$V_{12-18(p-p)}$	typ. 3	V*
Pulse duration switch input voltage			
at t = 14 μs + t_d (transistor driving)	V_{4-18}	0 to 3.5	V
at t = 0 (V_{3-18} = 0); input 4 open (I_4 = 0)	V_{4-18}	5.4 to 6.6	V
Output signals			
Vertical sync output pulse (peak-to-peak value)	$V_{8-18(p-p)}$	typ. 11	V
Burst key output pulse (peak-to-peak value)	$V_{7-18(p-p)}$	typ. 11	V
Line drive-pulse (peak-to-peak value)	$V_{3-18(p-p)}$	typ. 10	V

* Permissible range: 1 to 7 V.

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PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102DS).

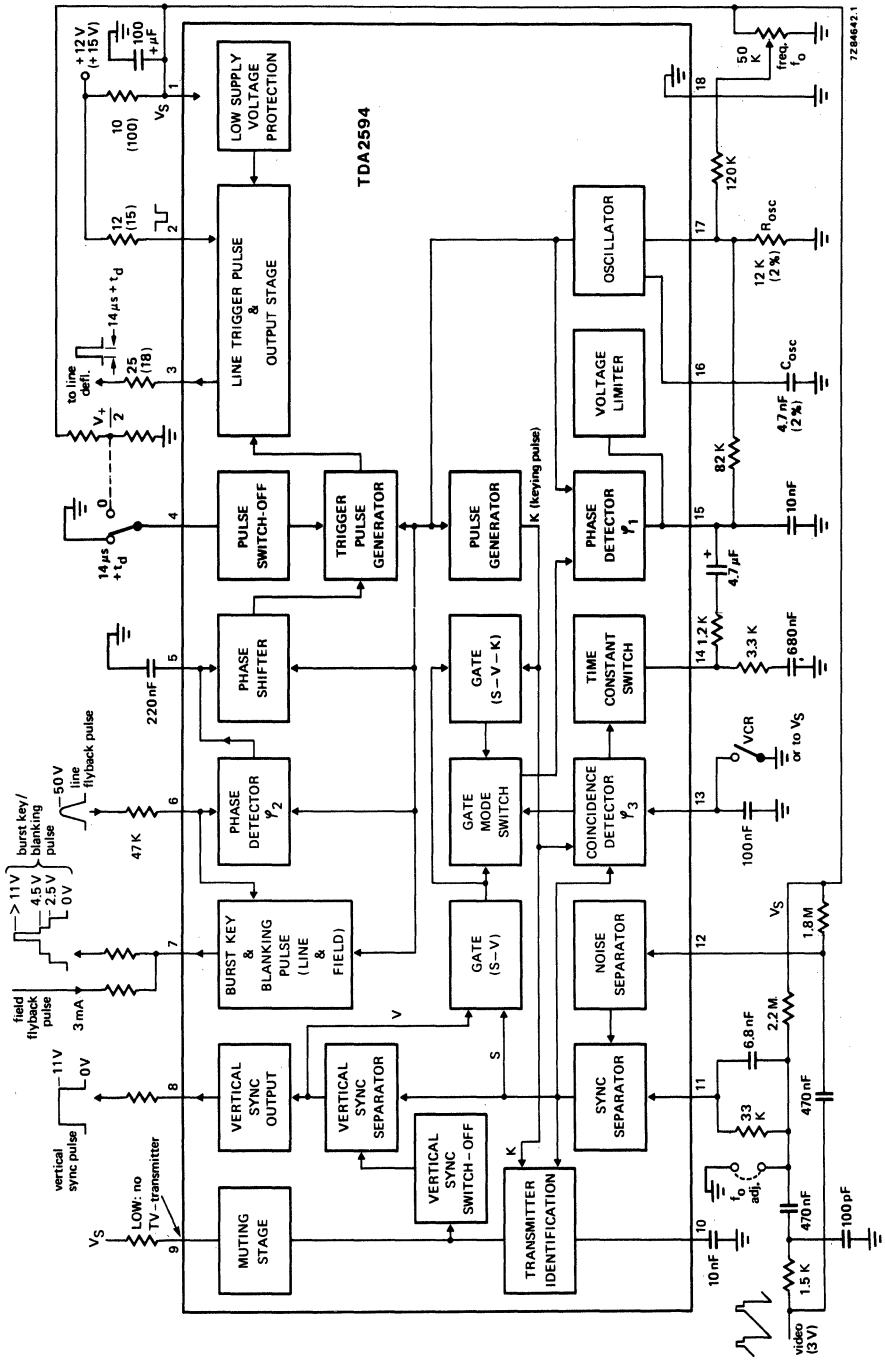

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
at pin 1 (voltage source)	$V_{1-18} = V_S$	max.	13.2 V
at pin 2	V_{2-18}	max.	18 V
Voltages			
Pin 4	V_{4-18}	max.	13.2 V
Pin 9	V_{9-18}	max.	18 V
	$-V_{9-18}$	max.	0.5 V
Pin 11	$\pm V_{11-18}$	max.	6 V
Pin 12	$\pm V_{12-18}$	max.	6 V
Pin 13	V_{13-18}	max.	13.2 V
Currents			
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400 mA
Pin 4	I_4	max.	1 mA
Pin 6	$\pm I_6$	max.	10 mA
Pin 7	$-I_7$	max.	5 mA
Pin 9	I_9	max.	10 mA
Pin 13	I_{13}	max.	2 mA
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature range	T_{stg}	−25 to	+125 °C
Operating ambient temperature range	T_{amb}	−20 to	+70 °C

CHARACTERISTICS at $V_{1-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

Sync separator (pin 11)

Input switching voltage	V_{11-18}	typ.	0.8 V
Input keying current	I_{11}		5 to 100 μA
Input leakage current at $V_{11-18} = -5$ V	I_{11}	⩽	1 μA
Input switching current	I_{11}	⩽	5 μA
Switch off current	I_{11}	⩾	100 μA
		typ.	150 μA
Input signal (peak-to-peak value)	$V_{11-18(p-p)}$		3 to 4 V*

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* Permissible range 1 to 7 V.

Noise separator (pin 12)			
Input switching voltage	$V_{12\text{-}18}$	typ.	1.4 V
Input keying current	I_{12}		5 to 100 μA
Input switching current	I_{12}	⩾	100 μA
		typ.	150 μA
Input leakage current at $V_{12\text{-}18} = -5$ V	I_{12}	⩽	1 μA
Input signal (peak-to-peak value)	$V_{12\text{-}18(p\text{-}p)}$		3 to 4 V*
Permissible superimposed noise signal (peak-to-peak value)	$V_{12\text{-}18(p\text{-}p)}$	⩽	7 V
Line flyback pulse (pin 6)			
Input current	I_6	⩾	0.02 mA
		typ.	1 mA
Input switching voltage	$V_{6\text{-}18}$	typ.	1.4 V
Input limiting voltage	$V_{6\text{-}18}$		−0.7 to +1.4 V
Switching on VCR (pin 13)			
Input voltage	$V_{13\text{-}18}$		0 to 2.5 V
	or: $V_{13\text{-}18}$		9 to V_S V
Input current	$-I_{13}$	⩽	200 μA
	or: I_{13}	⩽	2 mA
Pulse switching off (pin 4)			
For t = 0; input pin 4 open or $V_{3\text{-}18} = 0$			
Input voltage	$V_{4\text{-}18}$		5.4 to 6.6 V
Input current	I_4	typ.	0 μA
Vertical sync pulse (positive-going) (pin 8)			
Output voltage (peak-to-peak value)	$V_{8\text{-}18\,(p\text{-}p)}$	⩾	10 V
		typ.	11 V
Output resistance	R_8	typ.	2 kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15 μs
Delay between trailing edge of input and output signal	t_{off}	⩾	t_{on} μs
Switching off the vertical sync pulse	$V_{10\text{-}18}$	⩽	3 V
Burst key pulse (positive-going) (pin 7)			
Output voltage	$V_{7\text{-}18}$	⩾	10 V
		typ.	11 V
Output resistance	R_7	typ.	70 Ω
Pulse duration; $V_{7\text{-}18} = 7$ V	t_p	typ.	4 μs
			3.7 to 4.3 μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst key pulse; $V_{7\text{-}18} = 7$ V	t	typ.	2.65 μs
			2.15 to 3.15 μs
Output trailing edge current	I_7	typ.	2 mA
Saturation voltage during line scan	$V_{7\text{-}18}$	⩽	1 V

* Permissible range 1 to 7 V.

Line flyback-blanking pulse (positive-going) (pin 7)			
Output voltage	V_{7-18}		4.1 to 4.9 V
Output resistance	R_7	typ.	70 Ω
Output trailing edge current	I_7	typ.	2 mA
Field flyback/blanking pulse (pin 7)			
Output voltage with externally forced in current I_7 = 2.4 to 3.6 mA	V_{7-18}		2 to 3 V
Output resistance at I_7 = 3 mA	R_7	typ.	70 Ω
TV-transmitter identification output (pin 9; open collector)			
Output voltage at I_9 = 3 mA; no TV-transmitter	V_{9-18}	≤	0.5 V
Output resistance at I_9 = 3 mA; no TV-transmitter	R_9	≤	100 Ω
Output current at $V_{10-18} \geq 3$ V; TV-transmitter identified	I_9	≤	5 μA
TV-transmitter identification (pin 10)			
When receiving a TV signal the voltage V_{10-18} will change from ≤ 1 V to ≥ 7 V.			
Line drive pulse (positive-going)			
Output voltage (peak-to-peak value)	$V_{3-18(p-p)}$	typ.	10 V
Output resistance			
for leading edge of line pulse	R_3	typ.	2.5 Ω
for trailing edge of line pulse	R_3	typ.	20 Ω
Pulse duration (transistor driving)			
V_{4-18} = 0 to 3.5 V; $-I_4 \geq 200$ μA; t_{fp} = 12 μs	t_p		14 + t_d μs*
Supply voltage for switching off the output pulse	V_{1-18}	typ.	4 V
Overall phase relation			
Phase relation between middle of sync pulse and the middle of the flyback pulse	Δt	typ.	2.6 ± 0.7 μs**

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2.

If additional adjustment is applied it can be arranged by current supply at pin 5, such that:

Supplying current	$\Delta I/\Delta t$	typ.	30 μA/μs

* t_d = switch-off delay of line output stage.
** Line flyback pulse duration t_{fp} = 12 μs.

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Oscillator (pins 16 and 17)				
Threshold voltage low level	$V_{16\text{-}18}$	typ.	4.4	V
Threshold voltage high level	$V_{16\text{-}18}$	typ.	7.6	V
Charging current	$\pm I_{16}$	typ.	0.47	mA
Frequency; free running (C_{osc} = 4.7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15.625	kHz
Spread of frequency	Δf_o	⩽	± 5	%▲
Frequency control sensitivity	$\Delta f_o/\Delta_{17}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	Δf_o	typ.	± 10	%
Influence of supply voltage on frequency; reference at V_S = 12 V	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	⩽	± 0.05	%▲
Change of frequency when V_S drops to 5 V; reference at V_S = 12 V	Δf_o	⩽	± 10	%▲
Temperature coefficient of oscillator frequency	TC	⩽	$\pm 10^{-4}$	K^{-1}▲
Phase comparison φ_1 (pin 15)				
Control voltage range	$V_{15\text{-}18}$		4.1 to 7.9	V
Control current (peak value)	$\pm I_{15M}$		1.8 to 2.2	mA
Output leakage current at $V_{15\text{-}18}$ = 4.3 to 7.7 V	I_{15}	⩽	1	μA
Output resistance				
at $V_{15\text{-}18}$ = 4.3 to 7.7 V	R_{13}	high ohmic		*
at $V_{15\text{-}18} \leqslant 4.1$ V or $\geqslant 7.9$ V	R_{13}	low ohmic		**
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ between pins 15 and 17)	Δf	typ.	± 680	Hz
Spread of catching and holding range	Δ(Δf)	typ.	± 12	%▲
Phase comparison φ_2 **and phase shifter** (pin 5)				
Control voltage range	$V_{5\text{-}18}$		5.4 to 7.6	V
Control current (peak value)	$\pm I_{5M}$	typ.	1	mA
Output resistance at $V_{5\text{-}18}$ = 5.4 to 7.6 V	R_5	high ohmic		*
Input leakage current at $V_{5\text{-}18}$ = 5.4 to 7.6 V	I_5	⩽	5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	⩽	15.5	μs
Static control error	$\Delta t/\Delta t_d$	⩽	0.2	%
Coincidence detector φ_3 (pin 13)				
Output voltage	$V_{13\text{-}18}$		0.5 to 6	V
Output current (peak value)				
without coincidence	I_{13M}	typ.	0.1	mA
with coincidence	$-I_{13M}$	typ.	0.5	mA

* Current source.
** Emitter follower.
▲ Excluding external component tolerances.

Time constant switch (pin 14)			
Output voltage	$V_{14\text{-}18}$	typ.	6 V
Output current (limited)	$\pm I_{14}$	typ.	1 mA
Output resistance			
at $V_{13\text{-}18}$ = 3.5 to 7 V	R_{14}	typ.	0.1 kΩ
at $V_{13\text{-}18} \leqslant 2.5$ V or $\geqslant 9$ V	R_{14}	typ.	60 kΩ
Internal keying pulse			
Pulse duration	t_p	typ.	7.5 μs

Horizontal Combination | TDA2595

GENERAL DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in colour television receivers. The circuit incorporates the following functions:

- Positive video input; capacitively coupled (source impedance $< 200\ \Omega$)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- φ_1 phase control between horizontal sync and oscillator
- Coincidence detector φ_3 for automatic time-constant switching; overruled by the VCR switch
- Time-constant switch between two external time-constants or loop-gain; both controlled by the coincidence detector φ_3
- φ_1 gating pulse controlled by coincidence detector φ_3
- Mute circuit depending on TV transmitter identification
- φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4 V or higher than 8 V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot-suppressor controlled by the line flyback control

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_{15\text{-}5} = V_P$	typ.	12 V
Sync pulse amplitude (positive video)	$V_{i(p\text{-}p)}$	min.	50 mV
Horizontal output current	I_4	max.	30 mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

Horizontal Combination

TDA2595

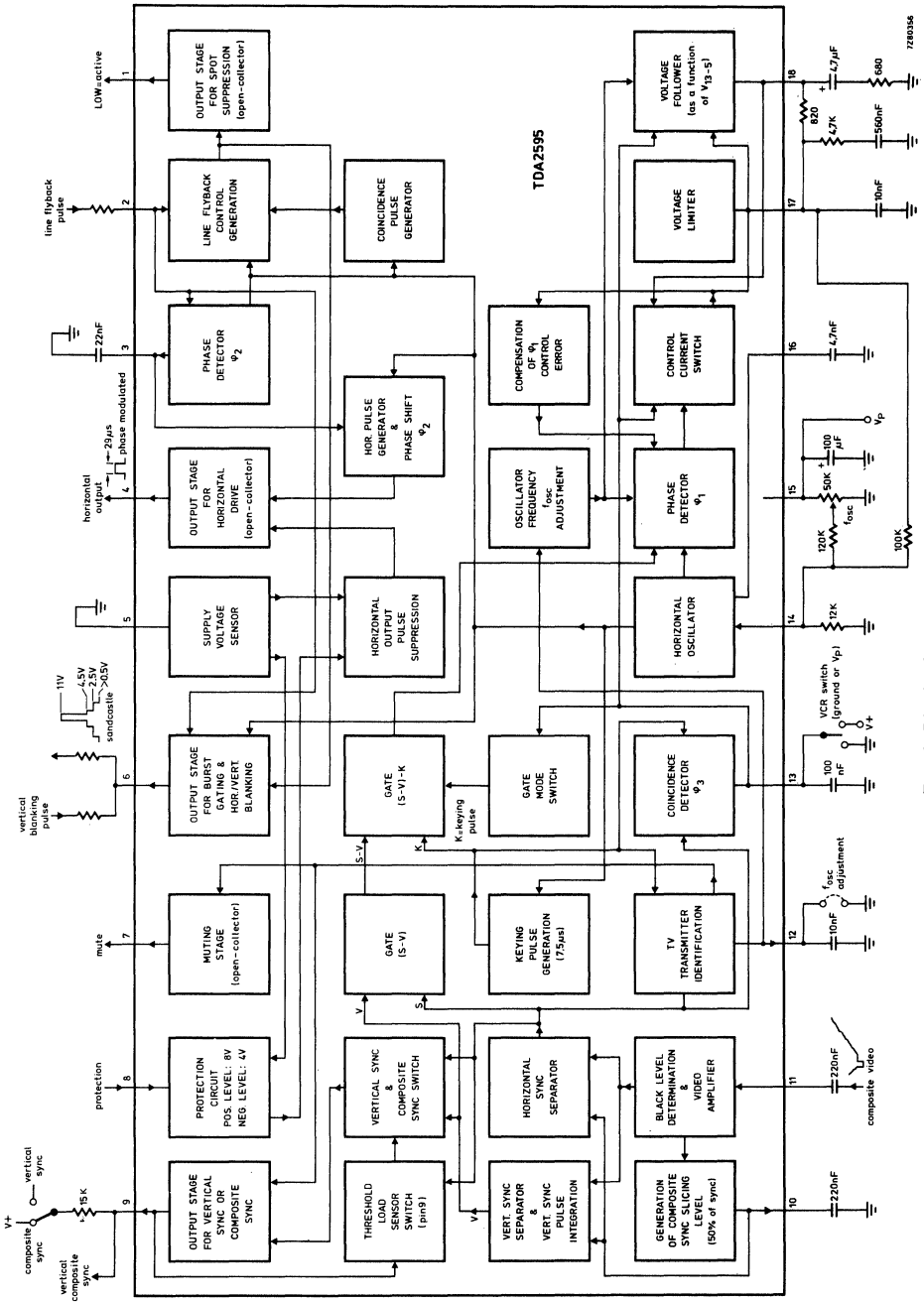

Fig. 1 Block diagram.

8

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_{15-5} = V_P$	max.	13.2	V
Voltages at:				
pins 1, 4 and 7	$V_{1;4;7-5}$	max.	18	V
pins 8, 13 and 18	$V_{8;13;18-5}$	max.	V_P	V
pin 11 (range)	V_{11-5}		−0.5 to + 6	V
Currents at:				
pin 1	I_1	max.	10	mA
pin 2 (peak value)	$\pm I_{2M}$	max.	10	mA
pin 4	I_4	max.	100	mA
pin 6 (peak value)	$\pm I_{6M}$	max.	6	mA
pin 7	I_7	max.	10	mA
pin 8 (range)	I_8		−5 to + 1	mA
pin 9 (range)	I_9		−10 to + 3	mA
pin 18	$\pm I_{18}$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−25 to + 125	°C
Operating ambient temperature range	T_{amb}		−20 to + 70	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Composite video input and sync separator (pin 11) (internal black level determination)					
Input signal (positive video; standard signal; peak-to-peak value)	$V_{11\text{-}5(p\text{-}p)}$	0.2	1	3	V
Sync pulse amplitude (independent of video content)	$V_{11\text{-}5(p\text{-}p)}$	50	–	–	mV
Generator resistance	R_G	–	–	200	Ω
Input current during:					
video	I_{11}	–	5	–	μA
sync pulse	$-I_{11}$	–	40	–	μA
black level	$-I_{11}$	–	30	–	μA
Composite sync generation (pin 10) horizontal slicing level at 50% of the sync pulse amplitude					
Capacitor current during:					
video	I_{10}	–	12	–	μA
sync pulse	$-I_{10}$	–	170	–	μA
Vertical sync pulse generation slicing level at 25% (50% between black level and horizontal slicing level); pin 9					
Output voltage	$V_{9\text{-}5}$	10	–	–	V
Pulse duration	t_p	–	190	–	μs
Delay with respect to the vertical sync pulse (leading edge)	t_d	–	45	–	μs
Pulse-mode control					
output current for vertical sync pulse (dual integrated)		no current applied at pin 9			
output current for horizontal and vertical sync pulse (non-integrated separated signal)		current applied via a resistor of 15 kΩ from V_P to pin 9			

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parameter	symbol	min.	typ.	max.	unit
Horizontal oscillator (pins 14 and 16)					
Frequency; free running	f_{osc}	–	15 625	–	Hz
Reference voltage for f_{osc}	V_{14-5}	–	6	–	V
Frequency control sensitivity	$\Delta f_{osc}/\Delta I_{14}$	–	31	–	Hz/μA
Adjustment range of circuit Fig. 1	Δf_{osc}	–	± 10	–	%
Spread of frequency	Δf_{osc}	–	–	5	%
Frequency dependency (excluding tolerance of external components)					
with supply voltage (V_P = 12 V)	$\frac{\Delta f_{osc}/f_{osc}}{\Delta V_{15-5}/V_{15-5}}$	–	± 0.05	–	
with supply voltage drop of 5 V	Δf_{osc}	–	–	10	%
with temperature	TC	–	–	$\pm 10^{-4}$	K^{-1}
Capacitor current during:					
charging	$-I_{16}$	–	1024	–	μA
discharging	I_{16}	–	313	–	μA
Sawtooth voltage timing (pin 14)					
rise time	t_r	–	49	–	μs
fall time	t_f	–	15	–	μs
Horizontal output pulse (pin 4)					
Output voltage LOW at I_4 = 30 mA	V_{4-5}	–	–	0.5	V
Pulse duration (HIGH)	t_p	–	29 ± 1.5	–	μs
Supply voltage for switching off the output pulse (pin 15)	V_P	–	4	–	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_1 (pin 17)					
Control voltage range	$V_{17\text{-}5}$	3.55	–	8.3	V
Leakage current at $V_{17\text{-}5}$ = 3.55 to 8.3 V	I_{17}	–	–	1	μA
Control current for external time-constant switch	$\pm I_{17}$	1.8	2	2.2	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5} < 2$ V or $V_{13\text{-}5} > 9.5$ V	$\pm I_{17}$	–	8	–	mA
Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5}$ = 2 to 9.5 V	$\pm I_{17}$	1.8	2	2.2	mA
Horizontal oscillator control					
control sensitivity	S_φ	6	–	–	kHz/μs
catching and holding range	Δf_{osc}	–	± 680	–	Hz
spread of catching and holding range	Δf_{osc}	–	± 10	–	%
Internal keying pulse at $V_{13\text{-}5}$ = 2.9 to 9.5 V	t_p	–	7.5	–	μs
Time-constant switch					
slow time-constant at	$V_{13\text{-}5}$	9.5	–	2	V
fast time-constant at	$V_{13\text{-}5}$	2	–	9.5	V
Impedance converter offset voltage (slow time-constant)	$\pm V_{17\text{-}18}$	–	–	3	mV
Output resistance					
slow time-constant	$R_{18\text{-}5}$	–	–	10	Ω
fast time-constant	$R_{18\text{-}5}$	high impedance			
Leakage current	I_{18}	–	–	1	μA

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parameter	symbol	min.	typ.	max.	unit
Coincidence detector φ_3 (pin 13)					
Output voltage					
without coincidence with composite video signal	V_{13-5}	–	–	1	V
without coincidence without composite video signal (noise)	V_{13-5}	–	–	2	V
with coincidence with composite video signal	V_{13-5}	–	6	–	V
Output current					
without coincidence with composite video signal	I_{13}	–	50	–	μA
with coincidence with composite video signal	$-I_{13}$	–	300	–	μA
Switching current					
at $V_{13-5} = V_P - 0.5$ V	I_{13}	–	–	100	μA
at $V_{13-5} = 0.5$ V (average value)	$I_{13(av)}$	–	–	100	μA
Phase comparison φ_2 (pins 2 and 3) (see note 1)					
Input for line flyback pulse (pin 2)					
Switching level for φ_2 comparison	V_{2-5}	–	3	–	V
Switching level for horizontal blanking and flyback control	V_{2-5}	–	3	–	V
Input voltage limiting	V_{2-5}	–	–0.7	–	V
	or:	–	+4.5	–	V
Switching current					
at horizontal flyback	I_2	0.01	1	–	mA
at horizontal scan	I_2	–	–	2	μA
Phase detector output (pin 3)					
Control current for φ_2	$\pm I_3$	–	1	–	mA
Control range	$\Delta t_{\varphi 2}$	–	19	–	μs
Static control error	$\Delta t/\Delta t_d$	–	–	0.2	%
Leakage current	I_3	–	–	5	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Phase comparison φ_2 (pins 2 and 3) (continued)					
Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at t_{fp} = 12 μs (note 2)	Δt	–	2.6 ± 0.7	–	μs
If additional adjustment is required, it can be arranged by applying a current at pin 3, such that for applied current:	$\Delta I/\Delta t$	–	30	–	μA/μs
Burst gating pulse (pin 6; note 3)					
Output voltage	V_{6-5}	10	11	–	V
Pulse duration	t_p	3.7	4	4.3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at V_{6-5} = 7 V	$t_{\varphi 6}$	2.15	2.65	3.15	μs
Output trailing edge current	I_6	–	2	–	mA
Horizontal blanking pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	4.2	4.5	4.9	V
Output trailing edge current	I_6	–	2	–	mA
Saturation voltage at horizontal scan	V_{6-5sat}	–	–	0.5	V
Clamping circuit for vertical blanking pulse (pin 6; note 3)					
Output voltage at I_6 = 2.8 mA	V_{6-5}	2.15	2.5	3	V
Minimum output current at $V_{6-5} > 2.15$ V	I_{6min}	–	2.3	–	mA
Maximum output current at $V_{6-5} < 3$ V	I_{6max}	–	3.3	–	mA
TV-transmitter identification (pin 12)					
Output voltage					
no TV transmitter	V_{12-5}	–	–	1	V
TV transmitter identified	V_{12-5}	7	–	–	V

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parameter	symbol	min.	typ.	max.	unit
Mute output (pin 7)					
Output voltage at I_7 = 3 mA no TV transmitter	V_{7-5}	–	–	0.5	V
Output resistance at I_7 = 3 mA no TV transmitter	R_{7-5}	–	–	100	Ω
Output leakage current at $V_{12-5} > 3$ V TV transmitter identified	I_7	–	–	5	μA
Protection circuit (beam-current/ EHT voltage protection) (pin 8)					
No-load voltage for $I_8 = 0$ (operative condition)	V_{8-5}	–	6	–	V
Threshold at positive-going voltage	V_{8-5}	–	8 ± 0.8	–	V
Threshold at negative-going voltage	V_{8-5}	–	4 ± 0.4	–	V
Current limiting for V_{8-5} = 1 to 8.5 V	$\pm I_8$	–	60	–	μA
Input resistance for $V_{8-5} > 8.5$ V	R_{8-5}	–	3	–	kΩ
Response delay of threshold switch	t_d	–	10	–	μs
Control output of line flyback pulse control (pin 1)					
Saturation voltage at standard operation; I_1 = 3 mA	V_{1-5sat}	–	–	0.5	V
Output leakage current in case of break in transmission	I_1	–	–	5	μA

Notes to the characteristics

1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase modulated (φ_2) horizontal output pulse with constant duration.
2. t_{fp} is the line flyback pulse duration.
3. Three-level sandcastle pulse.

Universal Sync Generator SAA1043

GENERAL DESCRIPTION

The SAA1043 generates the synchronizing waveforms required in all types of video source equipment (video cameras, film-scanners, video games, computer displays and similar applications). The device is programmable to suit standards SECAM 1, SECAM 2, PAL/CCIR, NTSC 1, NTSC2, and PAL-M; the video game 624 and 524-line standards; and can be synchronized to an external sync signal. Inputs and outputs are CMOS compatible.

Features

- Programmable to eight standards
- Horizontal frequency manipulation for application in non-standard systems
- Oscillator functions with LC or crystal elements
- Additional outputs to simplify camera signal processing
- Can be synchronized to an external sync signal
- Vertical reset for fast vertical lock
- Subcarrier lock in combination with subcarrier coupler SAA1044
- Very low power consumption

QUICK REFERENCE DATA

Supply voltage range (pin 28)	V_{DD}	5,7 to 7,5	V
Supply current (quiescent)	I_{DD}	max. 10	μA
Oscillator frequency	f_{OSCI}	max. 5,1	MHz

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PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

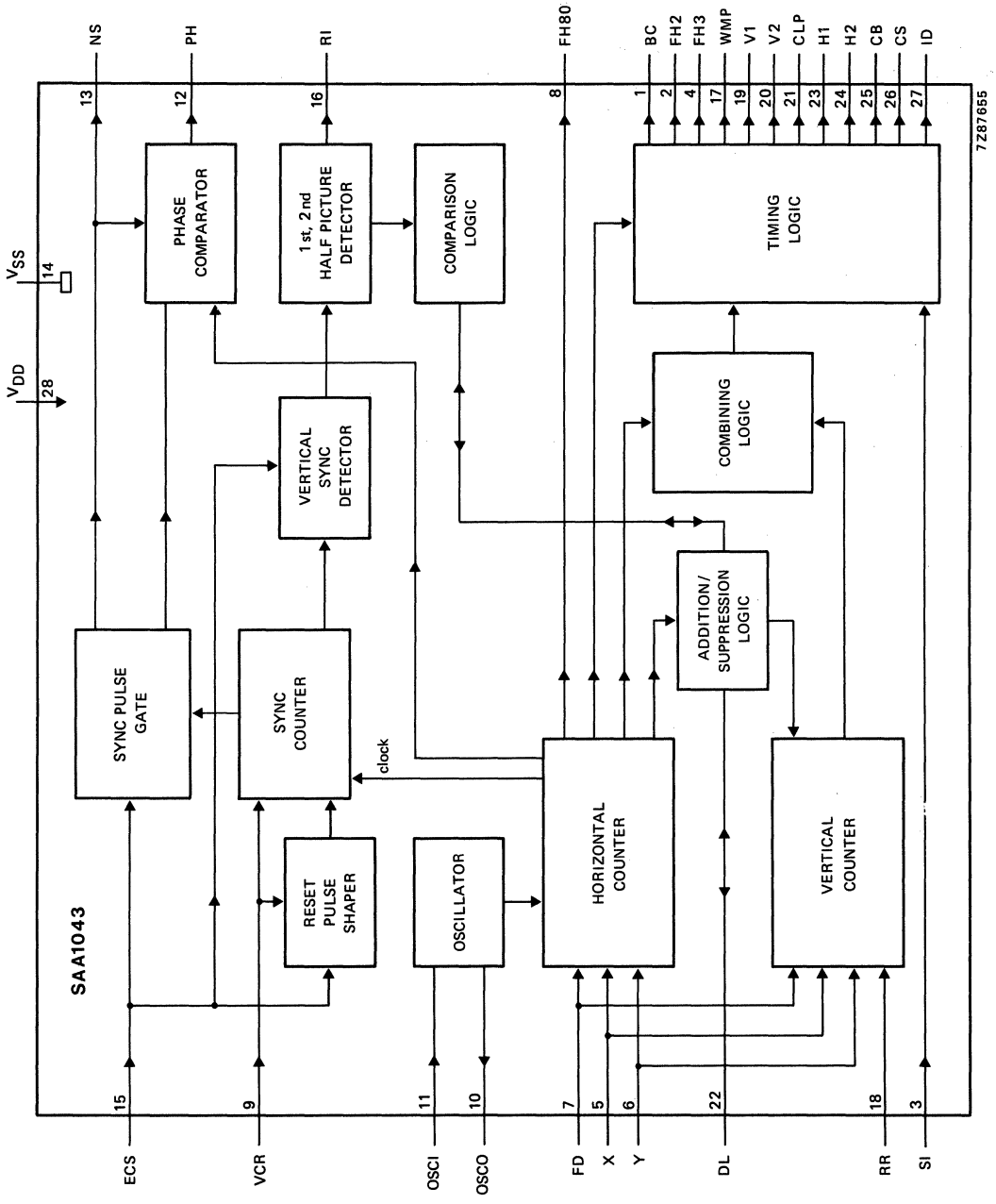


Fig. 1 Block diagram.

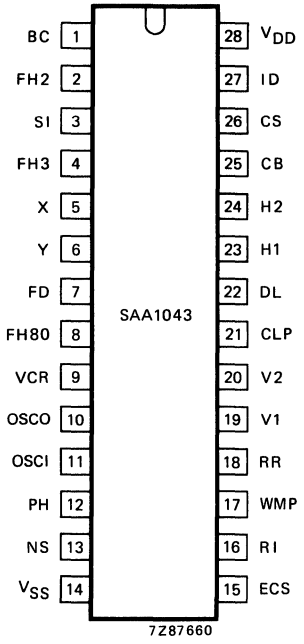


Fig. 2 Pinning diagram.

PINNING

1	BC	burst flag/chroma blanking (SECAM) output
2	FH2	PAL identification output
3	SI	set identification input (SECAM, PAL, PAL-M)
4	FH3	400 Hz (PAL); 360 HZ (NTSC, PAL-M) and $f_H/3$ (SECAM)
5	X	standard programming input
6	Y	standard programming input
7	FD	standard programming input
8	FH80	80 x f_H output (1,25 MHz)
9	VCR	VCR standard input
10	OSCO	oscillator output
11	OSCI	oscillator input
12	PH	phase detector output
13	NS	no-sync detector output
14	V_{SS}	negative supply voltage (ground)
15	ECS	external composite sync input
16	RI	vertical identification output
17	WMP	white measurement pulse output
18	RR	vertical reset input
19	V1	vertical drive output
20	V2	vertical drive output
21	CLP	clamp pulse output
22	DL	2 x f_H input/output
23	H1	horizontal drive output
24	H2	horizontal drive output
25	CB	composite blanking output
26	CS	composite sync output
27	ID	SECAM identification output
28	V_{DD}	positive supply voltage

8

FUNCTIONAL DESCRIPTION

Sync pulse generation

Programming of operating standard

The standard required for operation is programmed using the inputs X, Y and FD as shown in Table 1. The FD input selects 525 or 625-line working of the vertical counter (524 or 624-lines for video game standards) and also influences the choice of oscillator frequency as shown in Table 2.

Table 1 Programming of operating standard

standard	FD	X	Y
SECAM 1	0	0	0
SECAM 2	0	0	1
624	0	1	0
PAL/CCIR	0	1	1
NTSC 1	1	0	0
NTSC 2	1	0	1
524	1	1	0
PAL-M	1	1	1

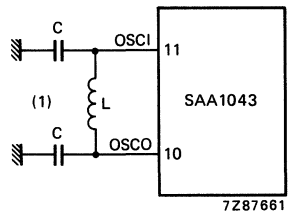
positive logic: 1 = HIGH; 0 = LOW

Oscillator

The built-in oscillator of the SAA1043 functions with an external LC-circuit (Fig. 3) or with a crystal of the parallel resonance type (Fig. 4). For operation in the VCR mode the LC oscillator circuit is recommended. The frequencies required for the operating standards are shown in Table 2.

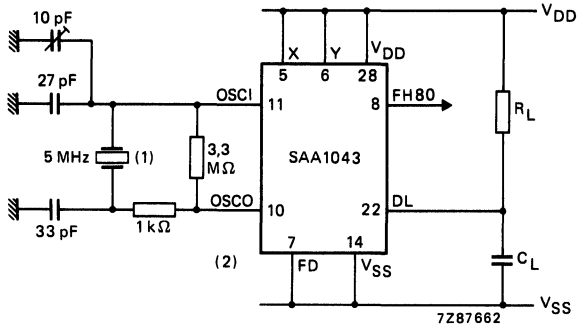
Table 2 Oscillator input frequencies

operating standard	osc. frequency (f_{OSCI}) MHz	vertical divider (FD)	vertical frequency (f_V) Hz	horizontal frequency (f_H) Hz
PAL, SECAM, 624	5,0	0	50	15625
NTSC, PAL-M, 524	5,034964	1	59,94	15734,26
PAL, SECAM, 624	2,5	H2 (pin 24)	50	15625
NTSC, PAL-M, 524	2,501748	H1 (pin 23)	59,94	15734,26



(1) Component values can be calculated from the formula $f_{OSCI} = 1/2\pi\sqrt{LC_V}$ where $C_V = C/2 + C_p$ and C_p = parasitic capacitance of typically 5 pF.

Fig. 3 LC oscillator circuit.



(1) Catalogue number of crystal: 8222 298 40760.

(2) All inputs not shown are at V_{SS}.

Fig. 4 Crystal oscillator circuit showing test set-up for oscillator frequency measurement.

Synchronization to an external sync signal

Use is made of the phase comparator output PH to lock the internally generated sync pulses to an external sync signal. Reset pulses derived at each falling edge of the external sync signal (ECS) reset the the sync counter which is clocked at the internal horizontal frequency by the horizontal counter. At each horizontal scan period the sync counter opens the sync pulse gate and allows the ECS to be applied to the phase comparator where it is compared with the phase of the internally generated horizontal sync pulse. When the two signals are in phase the output PH is in a high impedance state. When a phase difference exists PH is pulled towards V_{DD} or V_{SS} depending on the direction of the error (Fig. 5). The phase-analogue voltage on PH is used to correct the frequency at OSCI via a voltage-controlled oscillator and null the phase error between internal and external signals. Pulses occurring on the ECS outside of the sync pulse gating time (serration and equalization pulses) do not effect the phase comparator.

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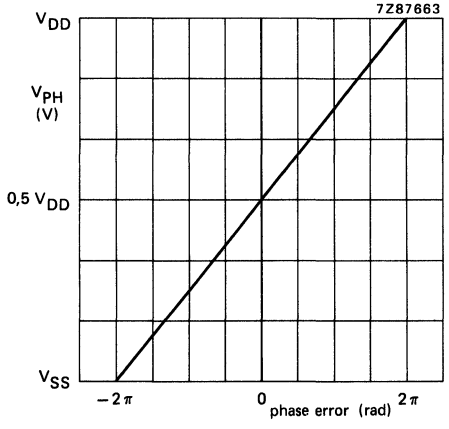


Fig. 5 Phase comparator characteristic.

FUNCTIONAL DESCRIPTION (continued)

Synchronization to an external sync signal (continued)

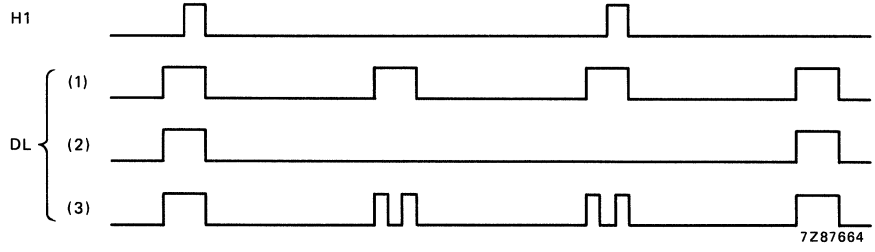
The circuit will lock to standard and non-standard sync signals. With standard signals the resetting of the sync counter is permitted after 3/4 of the horizontal scan period and if one reset pulse is missed the next pulse will reset the counter. With non-standard signals a narrow reset window is imposed to avoid disturbances which would otherwise be visible on the screen during vertical blanking time. The width of this window is $64 - 15{,}2 <$ reset time $< 64 + 15{,}2$ μs. If a reset pulse does not occur within this window the same window timing is specified for the next horizontal scan.

A no-sync signal is generated by the sync pulse gate if the sync counter is not reset from the ECS. The no-sync signal (NS) occurs 6,4 μs after the time of the missing reset pulse.

Detection of the vertical sync in the ECS is performed using a double sampling method which minimizes detection failures. Vertical lock is performed by comparing the internal vertical sync with a pulse derived from the ECS and using the result to modify the period of the vertical counter. This is achieved by manipulating the DL ($2 \times f_H$) input to the vertical counter via the addition/subtraction logic. The DL pulses are added or suppressed to bring the circuit into lock in the shortest possible time; the direction taken is determined by a logic decision based on the half picture in which the ECS derived pulse occurred.

Use in non-standard systems

For systems requiring a non-standard horizontal frequency the number of horizontal scans per picture can be manipulated using the open drain input/output DL. The addition or suppression of pulses during the high ohmic period of DL modifies the vertical counter value. The suppression of two DL pulses per half picture will give one extra horizontal scan and the addition of two DL pulses will remove one horizontal scan from the half picture (see Fig. 6).



(1) Normal waveform at DL; $f_{DL} = 2 \times f_H$.

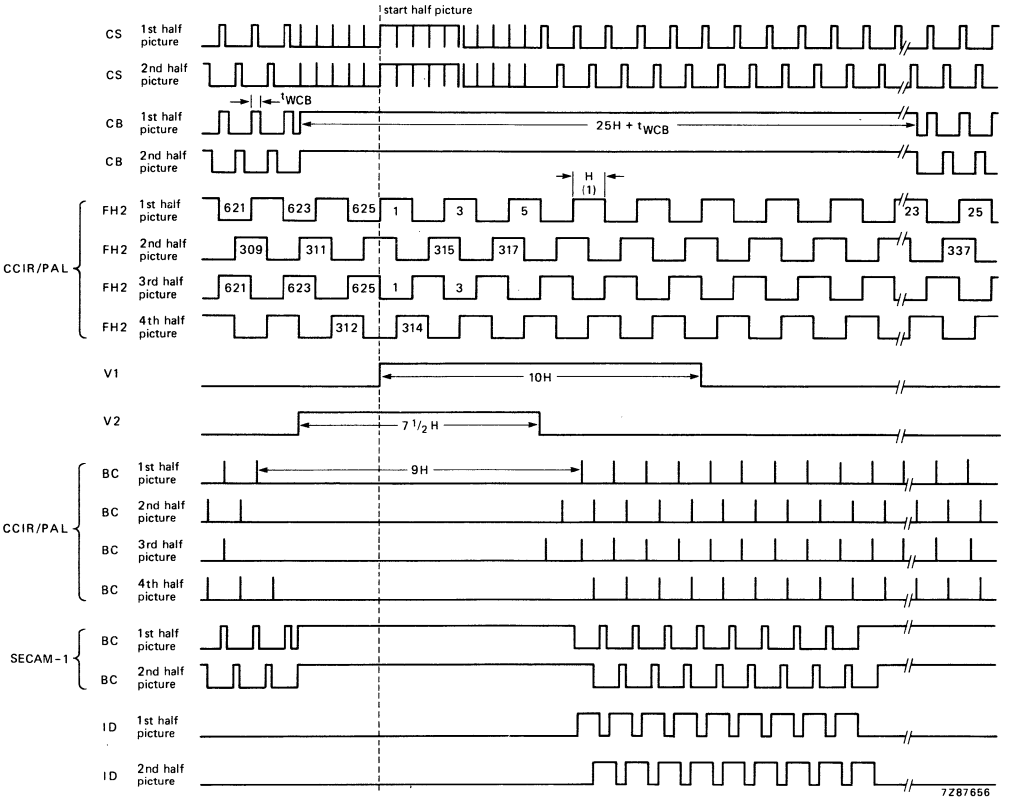
(2) Waveform at DL with two pulses suppressed increases the number of horizontal scans per half picture by 1.

(3) Waveform at DL with two additional pulses decreases the number of horizontal scans per half picture by 1.

Fig. 6 Manipulation of the horizontal frequency for non-standard systems.

Output waveforms

The output waveforms for the different modes of operation are shown in Figs 7 and 8.

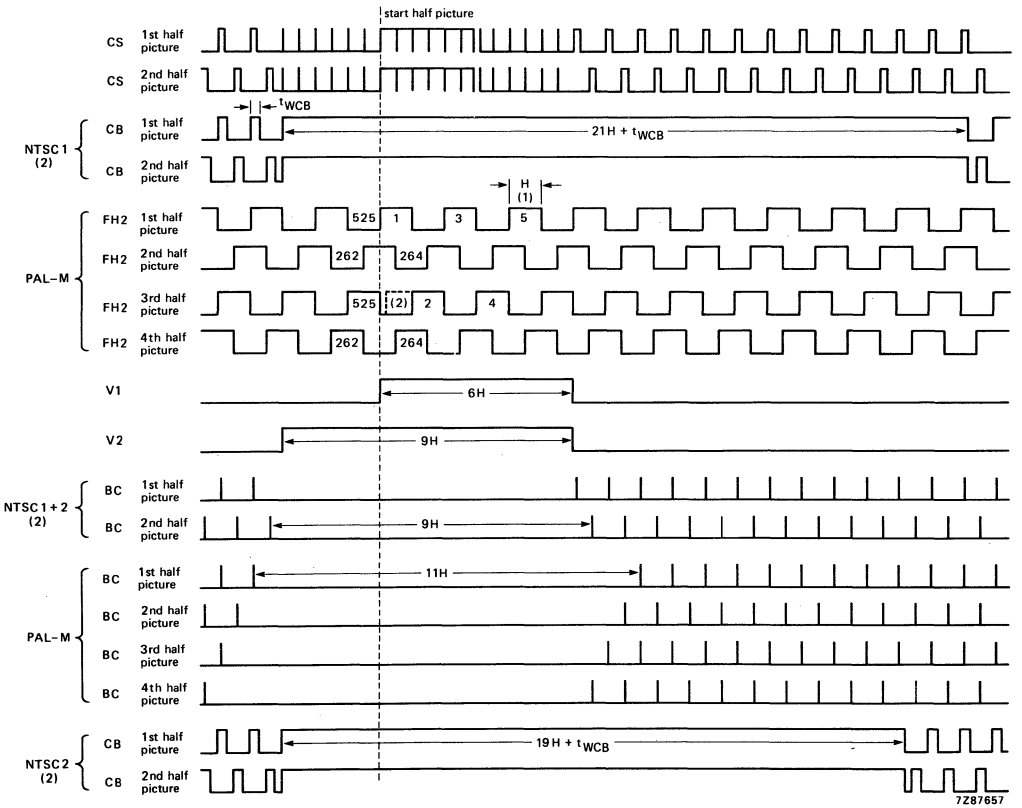


(1) H = 1 horizontal scan.

Fig. 7 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the 1st half picture of PAL/CCIR and are not interlaced (0,5H subtracted from the waveform timing).

FUNCTIONAL DESCRIPTION (continued)

Output waveforms (continued)



(1) H = 1 horizontal scan.

(2) NTSC mode reset; the 4th half picture is identical to the 2nd half picture for NTSC.

Fig. 8 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the 1st half picture of NTSC and are not interlaced (0,5H subtracted from the waveform timing).

WAVEFORM TIMING (Table 3, Figs 9 and 10)

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is shown in Table 3 as the number (n) of oscillations at OSCI. The timings given are derived from n x t_{OSCI} ± 100 ns. One horizontal scan (H) = 320 x t_{OSCI} = $1/f_H$. Note that the number of horizontal scans per half picture can be modified for non-standard systems using input/output DL as shown in Fig. 6.

Table 3 Waveform timing

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
CS							
Horizontal sync pulse width	t_{WSC1}	4,8	4,77	4,77	4,8	µs	24
Equalizing pulse width	t_{WSC2}	2,4	2,38	2,38	2,4	µs	8
Serration pulse width	t_{WSC3}	4,8	4,77	4,77	4,8	µs	24
Duration of pre-equalizing pulses	–	2,5	3	3	2,5	H	
Duration of post-equalizing pulses	–	2,5	3	3	2,5	H	
Duration of serration pulses	–	2,5	3	3,5	2,5	H	
CB							
Horizontal blanking pulse width							
PAL/SECAM/PAL-M	t_{WCB}	12	–	11,12	12	µs	60
NTSC 1	t_{WCB}	–	11,12	–	–	µs	56
NTSC 2	t_{WCB}	–	10,53*	–	–	µs	53
Front porch	t_{PCBCS}	1,6	1,59	1,59	1,6	µs	8
Duration of vertical blanking							
PAL/SECAM/PAL-M		25H+t_{WCB}	–	21H+t_{WCB}	25H+t_{WCB}		
NTSC 1		–	21H+t_{WCB}	–	–		
NTSC 2		–	19H+t_{WCB}	–	–		
BC (PAL)							
Burst key pulse width	t_{WBC}	2,4	2,38	2,38	–	µs	12
Sync to burst delay	t_{PCSBC}	5,6	5,56	5,76	–	µs	28
Burst suppression	–	9	9	11	–	H	
Position of burst suppression: 1st half picture	–	H623 to H6	H523 to H6	H523 to H8	–	–	
2nd half picture	–	H310 to H318	H261 to H269	H260 to H270	–	–	
3rd half picture	–	H622 to H5	H523 to H6	H522 to H7	–	–	
4th half picture	–	H311 to H319	H261 to H269	H259 to H269	–	–	

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WAVEFORM TIMING (continued)

Table 3 (continued)

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
BC (SECAM)							
Chroma pulse width	t_{WBC}	–	–	–	7,2	µs	36
Chroma to sync delay	t_{PBCCS}	–	–	–	1,6	µs	8
Duration of vertical blanking: SECAM 1	1st half picture: 25H + t_{WBC} except H320 to H328 2nd half picture: 24,5H + t_{WBC} except H7 to H15						
SECAM 2	1st half picture: 25H + t_{WBC} 2nd half picture: 24,5H + t_{WBC}						
CLP							
Clamp pulse width	t_{WCLP}	2,4	2,38	2,38	2,4	µs	12
Sync to clamp delay	t_{PCSCLP}	2,4	2,38	2,38	2,4	µs	12
DL							
Frequency	f_{DL}	2 x f_H	2 x f_H	2 x f_H	2 x f_H	–	
Pulse width	t_{WDL}	9,6	9,53	9,53	9,6	µs	48
DL to sync delay	t_{PCLCS}	5,6	5,56	5,56	5,6	µs	28
FH80							
Frequency	f_{FH80}	80 x f_H	80 x f_H	80 x f_H	80 x f_H	–	
Sync to FH80 delay	–	0,2	0,2	0,2	0,2	µs	1
H1, H2							
H1 pulse width	t_{WH1}	7,2	7,15	7,15	7,2	µs	36
H2 pulse width	t_{WH2}	7,2	7,15	7,15	7,2	µs	36
H1 to sync delay	t_{PH1CS}	0,8	0,79	0,79	0,8	µs	4
Sync to H2 delay	t_{PCSH2}	0,8	0,79	0,79	0,8	µs	4
Repetition period	–	64	63,56	63,56	64	µs	
V1, V2							
V1 duration	–	10	6	6	10	H	
V2 duration	–	7,5	9	9	7,5	H	
V1 to sync delay	t_{PV1CS}	1,6	1,59	1,59	1,6	µs	8
Sync to V2 delay	t_{PV2CS}	1,6	1,59	1,59	1,6	µs	8
FH2							
Frequency	f_{FH2}	$f_H/2$	$f_H/2$	$f_H/2$	$f_H/2$	–	
Sync to FH2 delay	–	0	0	0	0	µs	
FH3							
Frequency	f_{FH3}	400	360	360	$f_H/3$	–	
Sync to FH3 delay	–	–	–	–	0	µs	

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
WMP							
WMP pulse width	–	2,4	2,38	2,38	2,4	μs	12
Sync to WMP delay	–	34,4	34,16	34,16	34,4	μs	172
Duration of WMP	–	10	9	9	10	H	
Position of WMP							
1st half picture:	–	H163 to H173	H134 to H143	H134 to H143	H163 to H173	– –	
2nd half picture:	–	H475 to H485	H396 to H405	H396 to H405	H475 to H485	– –	
RI							
Frequency	–	$f_V/2$	$f_V/2$	$f_V/2$	$10f_H$	–	
Position of edges	–	H6 and H318	H7 and H269	H7 and H269	–	–	
ID							
ID pulse width	t_{WID}	12,0	11,12	11,12	12,0	μs	60
ID to sync delay	t_{PIDCS}	1,6	1,59	1,59	1,6	μs	8
Position of ID							
1st half picture:	–	H7 to H15	H8 to H22	H8 to H22	H7 to H15	–	
2nd half picture:	–	H320 to H328	H271 to H285	H271 to H285	H320 to H328	– –	

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* Horizontal blanking pulse width for NTSC 2 can be 11, 12 μs maximum.

WAVEFORM TIMING (continued)

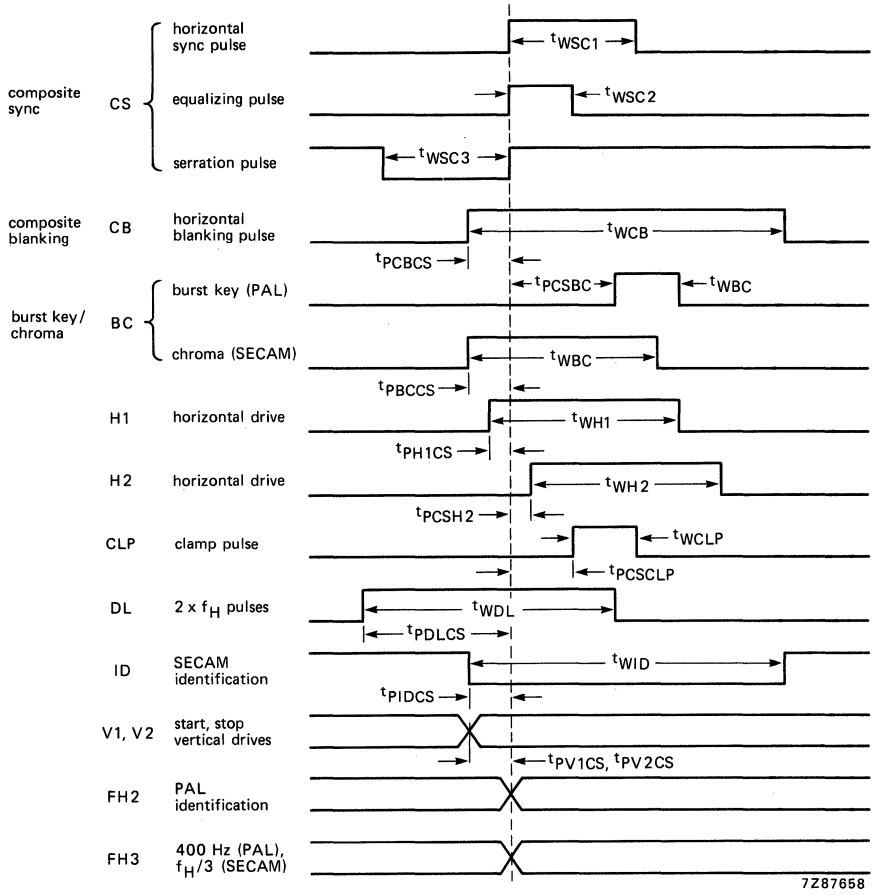

Fig. 9 Waveform timings: PAL/CCIR; SECAM; 624-line modes.

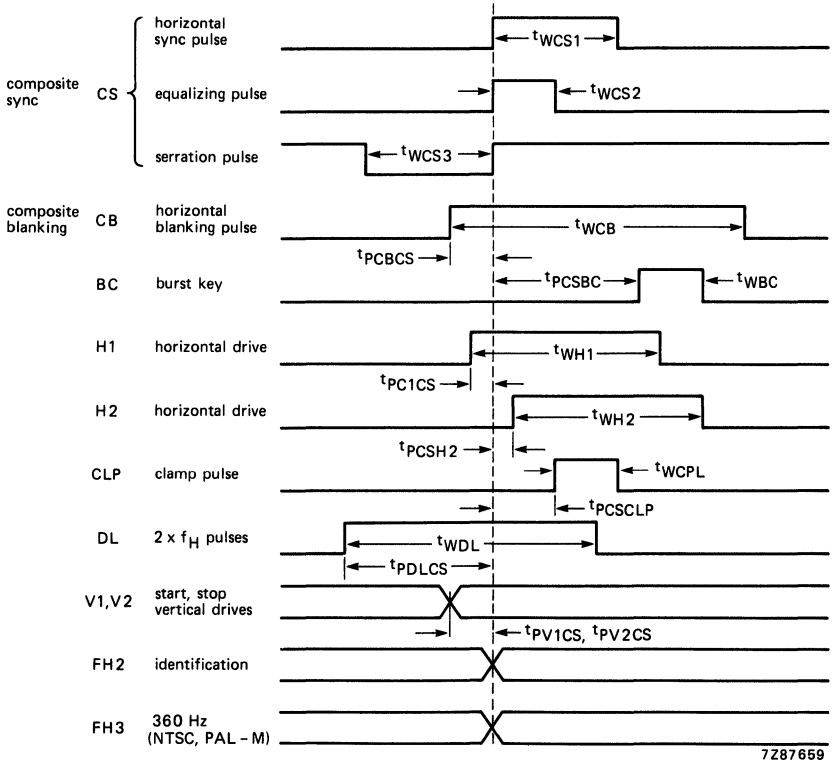

Fig. 10 Waveform timings: NTSC; PAL-M; 524-line modes.

8

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	−0,5 to + 15	V
Input voltage range	V_I	−0,5 to (V_{DD} + 0,5)*	V
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	−0,5 to (V_{DD} + 0,5)*	V
Output current	$\pm I_O$	max. 10	mA
Power dissipation per output	P_O	max. 100	mW
Total power dissipation per package	P_{tot}	max. 200	mW
Operating ambient temperature range	T_{amb}	−25 to + 70	°C
Storage temperature range	T_{stg}	−55 to + 150	°C

* V_{DD} + 0,5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5,7 to 7,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5,7	–	7,5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °V	I_{IR}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{IR}$	–	–	1	μA
Outputs (except PH and OSC0)					
Output voltage HIGH at $-I_{OH}$ = 0,5 mA	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 0,5 mA	V_{OL}	–	–	0,4	V
Output PH					
Output voltage HIGH at $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} − 0,5	–	–	V
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V	I_{OR}	–	–	5	μA
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{OR}	–	–	1	μA
Output leakage current at V_O = 0 V; V_{DD} = 7,5 V	$-I_{OR}$	–	–	5	μA
Output leakage current at V_O = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{OR}$	–	–	1	μA
Output OSCO					
Output voltage HIGH at V_{OSCI} = 0 V; $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} - 0,5	–	–	V
Output voltage LOW at V_{OSCI} = V_{DD}; I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V

parameter	symbol	min.	typ.	max.	unit
Input/output DL (open drain)*					
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V	I_{OR}	–	–	5	μA
Output leakage current at V_O = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{OR}	–	–	1	μA
Load resistance (Fig. 4)					
at V_{DD} = 5,7 V	R_L	1,4	–	–	kΩ
at V_{DD} = 7,5 V	R_L	0,82	–	–	kΩ
Time constant (Fig. 4)					
at V_{DD} = 5,7 V	R_LC_L	–	–	19	ns
at V_{DD} = 7,5 V	R_LC_L	–	–	13	ns
Oscillator frequency (Fig. 4)					
Maximum oscillator frequency at V_{DD} = 5,7 V	f_{OSCI}	5,1	–	–	MHz

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* **An external pull-up resistor (3,9 kΩ) must be connected between DL and V_{DD}. The time constant R_LC_L must not exceed the values given.**

APPLICATION INFORMATION

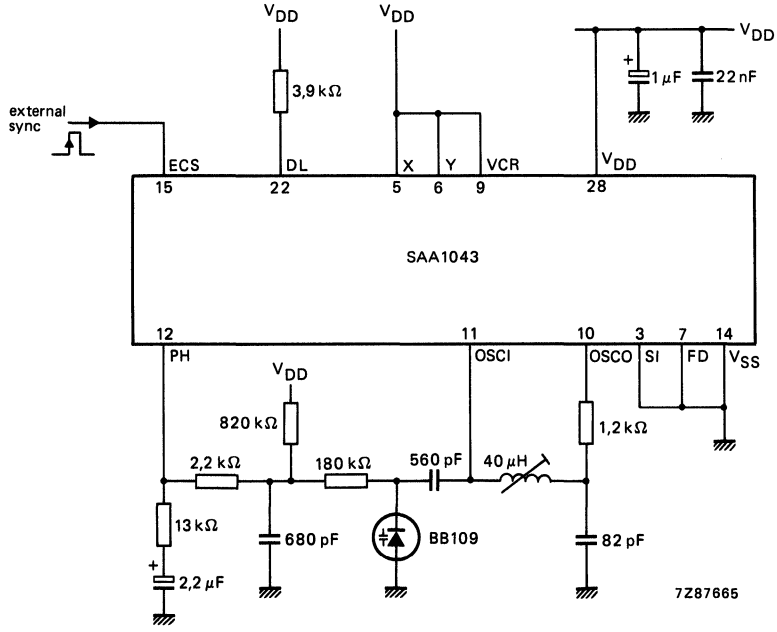

Fig. 11 Synchronizing circuit using passive filter network.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

Subcarrier Coupler | SAA1044

GENERAL DESCRIPTION

The SAA1044 maintains the correct relationship between subcarrier and horizontal scan frequencies when an exact coupling is required. It is for use in combination with sync generator SAA1043 for application in colour video sources (cameras, film-scanners and similar equipments).

Features

- Provides exact relationship between subcarrier and horizontal scan frequencies
- Accommodates all standard frequencies
- Facilitates GENLOCK (general locking) applications

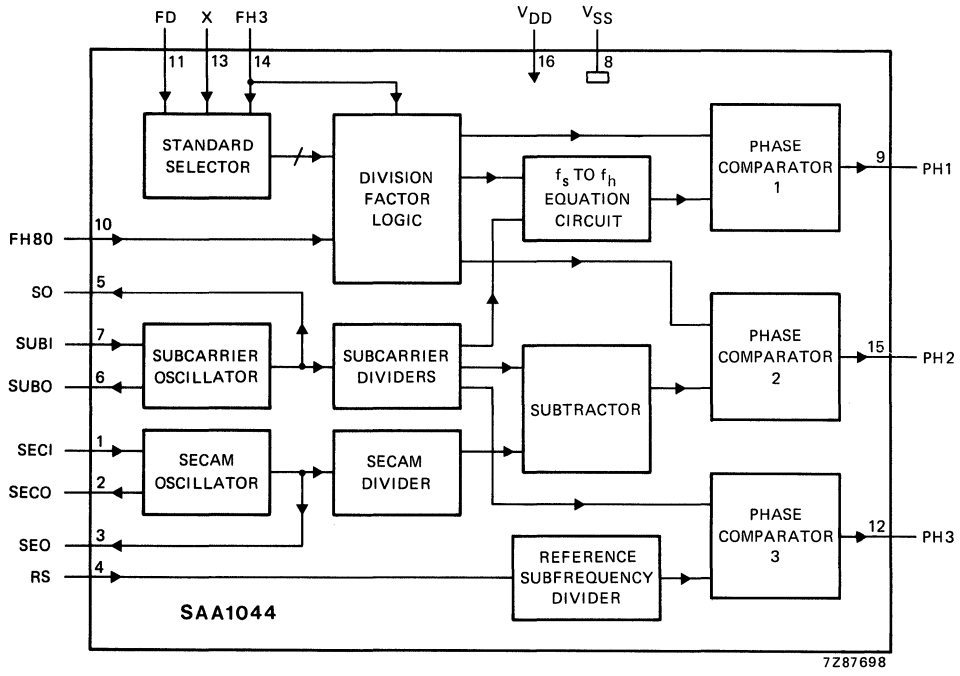

Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

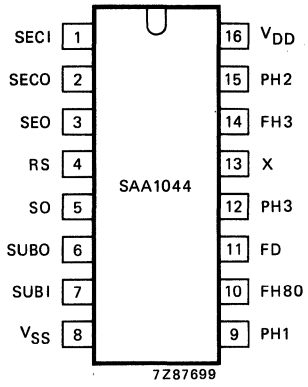

Fig. 2 Pinning diagram.

PINNING

1	SECI	SECAM oscillator input ($272f_H$)
2	SECO	SECAM oscillator output ($272f_H$)
3	SEO	inverted SECAM oscillator output
4	RS	reference subfrequency
5	SO	inverted subcarrier oscillator output
6	SUBO	subcarrier oscillator output
7	SUBI	subcarrier oscillator input
8	V_{SS}	negative supply voltage (ground)
9	PH1	phase comparator 1 output (FH80/SUBI)
10	FH80	1,25 MHz input (from SAA1043)
11	FD	standard programming input
12	PH3	phase comparator 3 output (RS/SUBI)
13	X	standard programming input
14	FH3	standard programming input (from SAA1043)
15	PH2	phase comparator 2 output (SECI/FH80)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Programming of operating standard

The standard required for operation is programmed using the inputs FD, X and FH3 as shown in Table 1.

Table 1 Programming of operating standard

standard	FD	X	FH3	relationship of subcarrier frequency (f_S) to horizontal scan frequency (f_H)
PAL	0	1	400 Hz	$f_S = 283{,}7516f_H$
SECAM	0	0	don't care	$f_S = 282f_H$
PAL-N	1	1	400 Hz	$f_S = 229{,}2516f_H$
PAL-M	1	0	1	$f_S = 227{,}25f_H$
NTSC	1	0	0	$f_S = 227{,}5f_H$

Positive logic: 1 = HIGH; 0 = LOW

Subcarrier/horizontal scan frequency relationship

The input FH80 from SAA1043 is the reference for horizontal scan frequency (f_H). This frequency is reduced by a factor determined by the selected operating standard to give a value of $8f_H$ (PAL, SECAM or $10f_H$ (PAL-N, PAL-M, NTSC) to phase comparator 1. The subcarrier frequency (f_S) is manipulated to provide a comparable value at the second input to the phase comparator. When the frequencies of the two inputs to phase comparator 1 are equal, the relationship between f_H and f_S is as shown in Table 1.

Phase comparator 1 functions with an exclusive-OR phase detector circuit and provides an output which may be used to control a voltage-controlled oscillator (VCO) via a low-pass filter. The VCO reference can be the subcarrier or the horizontal scan frequency and the filter can be active or passive, depending on application.

A second subcarrier oscillator circuit is provided for SECAM operation. The operating frequency of this is centred on $272f_H$ to give, when $f_S = 282f_H$, comparable values of $5f_H$ at the two inputs to phase comparator 2. A second VCO loop can be used to control the SECAM oscillator frequency.

The high degrees of accuracy and stability required for GENLOCK applications are met by phase comparator 3. This compares the internal subcarrier and external reference frequencies. To adjust the phase over 2π, this comparator has a linear characteristic over 4π. The output signal PH3 has a period time of $f_S/4$ and a duty cycle of between 12,5% and 62,5% giving a sensitivity of 240 mV/rad. Errors due to temperature variation are minimized by symmetrical circuit and chip design.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}		−0,5 to + 15	V
Input voltage range	V_I		−0,5 to (V_{DD} + 0,5)*	V
Input current	$\pm I_I$	max.	10	mA
Output voltage range	V_O		−0,5 to (V_{DD} + 0,5)*	V
Output current	$\pm I_O$	max.	10	mA
Power dissipation per output	P_O	max.	100	mW
Total power dissipation per package	P_{tot}	max.	200	mW
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Storage temperature range	T_{stg}		−55 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0,5 V not to exceed 15 V.

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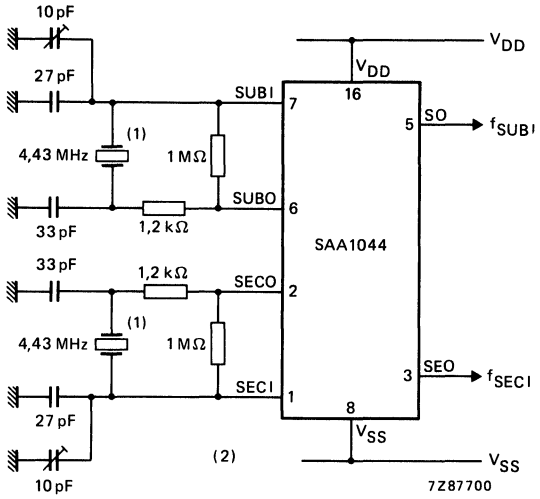
CHARACTERISTICS

V_{DD} = 5,7 to 7,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5,7	–	7,5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input leakage current at V_I = 7,5 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	I_{IR}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7,5 V; T_{amb} = 25 °C	$-I_{IR}$	–	–	1	μA
Outputs (except SECO and SUBO)					
Output voltage HIGH at $-I_{OH}$ = 0,5 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW at I_{OL} = 0,5 mA	V_{OL}	–	–	0,4	V
Outputs SECO and SUBO					
Output voltage HIGH at $-I_{OH}$ = 0,9 mA	V_{OH}	V_{DD} −0,5	–	–	V
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,4	V
Oscillator frequency (Fig. 3)					
Maximum oscillator frequency at V_{DD} = 5,7 V	f_{SUBI} } f_{SECI} }	5,1	–	–	MHz



(1) Catalogue number of crystal: 4322 143 04040.
(2) Inputs not shown are don't care.

Fig. 3 Test set-up for oscillator frequency measurement.

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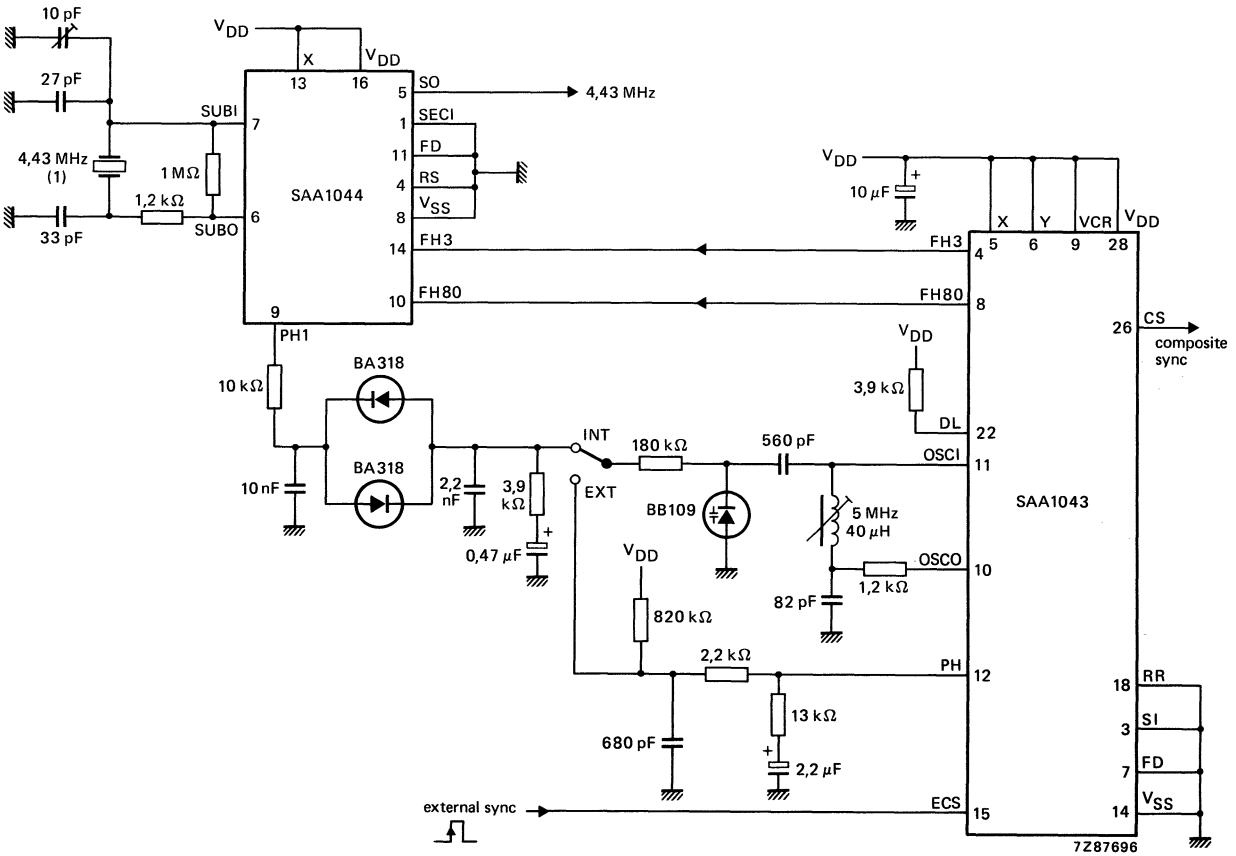
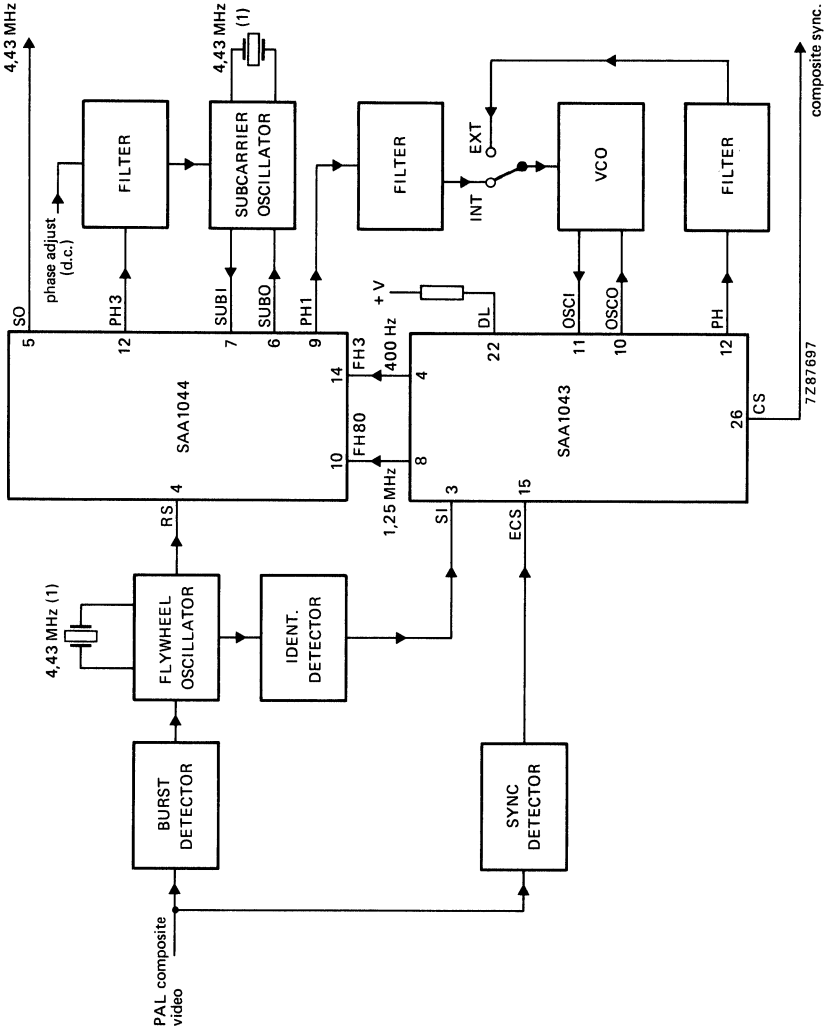
APPLICATION INFORMATION



(1) Catalogue number of crystal: 4322 143 04040.

Fig. 4 Subcarrier coupling for PAL application; external synchronization is selected with switch in EXT condition.



(1) Catalogue number of crystal: 4322 143 04040.

Fig. 5 Subcarrier coupling for PAL GENLOCK application.

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PAL/NTSC Encoder TDA2501

The TDA2501 encodes two colour-difference signals R-Y and B-Y onto one subcarrier. Quadrature modulation allows the coding to be in accordance with either the PAL or NTSC system.

Functions:

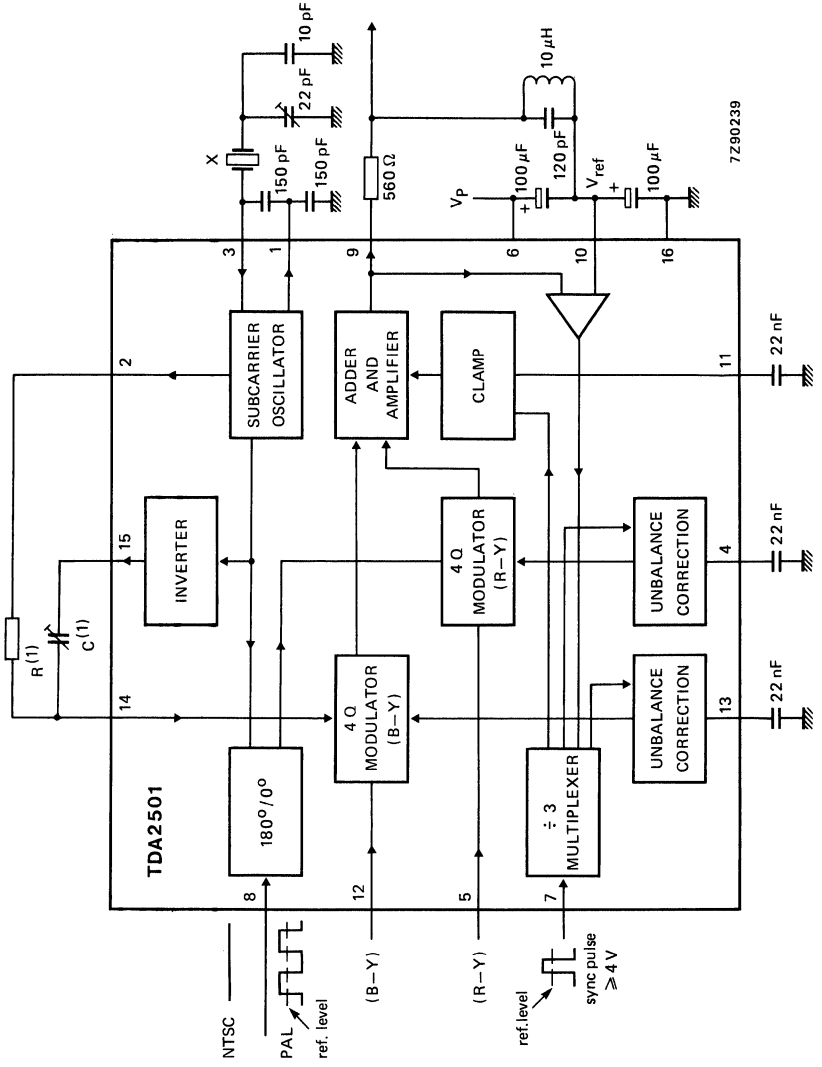
- Generates two sinusoidal subcarriers with a relative phase of 90° (also accepts external subcarriers)
- Modulates the two subcarriers with the colour difference signals
- Inverts the output from one modulator on command of an external signal (as in case of PAL)
- Sums the output from the modulators to obtain a quadrature modulated output signal
- Clamps the output d.c. level to a reference voltage
- Divides the frequency of horizontal sync pulses by three so that the output level can be clamped and the balance of the two modulators sequentially controlled during the line-blanking minus burst-key period

QUICK REFERENCE DATA

Supply voltage (pin 6)	V_P	typ.	6 V
Supply current	I_P	typ.	40 mA
Output chrominance voltage (pin 9)	$V_{9(p-p)}$	max.	1,4 V
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	−25 to +70	°C

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT-38WE-2).



(1) R = 0,885 (2 π fC); for PAL f = 4,433 619 MHz, R = 963 Ω and C = 33 pF.

Fig. 1 Block diagram. Also test and application diagram.

8

DESCRIPTION

The colour difference signals B-Y and R-Y with a maximum amplitude of 1,4 volt are to be applied at pin 12 and pin 5. D.C.-coupling of the input signals is allowed if their d.c. levels are within specified limits from the d.c. level at pin 10 (V_{ref}). The following table shows these limits as a function of supply voltage. The table also shows the limits of the reference voltage range as a function of the supply voltage.

supply voltage V_{6-16} (V)	input d.c. (R-Y) (B-Y) min. (V)*	V_{5-16} V_{12-16} (V) max. (V)*	reference voltage• V_{10-16} (V)		
			min	typ.	max.
5,5	2,4	3,3	2,3	3,0	3,5
6,0	$> V_{ref} - 1,4$ V	3,8	2,4	3,3	3,9
7,0	$> V_{ref} - 1,4$ V	4,8	2,6	4,0	4,7
8,0	$> V_{ref} - 1,4$ V	5,8	2,8	4,8	5,5
9,0	$> V_{ref} - 1,4$ V	6,8	3,0	5,5	6,3
10,0	$> V_{ref} - 1,4$ V	7,8	3,2	6,3	7,1

* Minimum 2,4 V.
** At $V_S - 2,2$ V.
• Minimum values at $0,2\ V_S + 1,2$ V.
Typical values without pull-up or pull-down resistor.
Maximum values at $0,8\ V_S - 0,9$ V.

The inputs (B-Y) and (R-Y) should be zero, independent of their (limited) d.c.-levels, during the line-blanking minus burst-key period (LB – BK). Clamping the output and correcting the out-of-balance of the modulators, is done by applying a HIGH level to pin 7 within the (LB – BK) period (e.g. line sync pulse).

Modulation at output:
V_8 = LOW; output = sc x (B-Y) + sc' x (R-Y)
V_8 = HIGH; output = sc x (B-Y) – sc' x (R-Y)
in which sc' = subcarrier
sc = 90° phase-shifted subcarrier to sc' (sc lags).

The bandpass filter at the output suppresses the d.c. components of the (R-Y) + (B-Y) signal. Luminance (Y) is not processed by this circuit.

Internal subcarrier

The internal subcarrier oscillator is crystal controlled. The oscillator generates a sinewave with low harmonic distortion and an amplitude of about 500 mV peak-to-peak. The amplitude can be changed if necessary with a current input at pin 1. The adjustment range is 0 to 800 mV, with a corresponding current range of +250 to –150 μA.

Phase shift

To obtain a 90° phase-shifted carrier, two low impedance subcarrier outputs are provided, pins 2 and 15, the last being the inverse of the first. Between pins 2 and 15 an external RC combination must be used to obtain the desired 90° shift. The capacitor value must be limited to 33 pF to minimize subcarrier distortion.

The resistor required between pins 2 and 14 is 0,885 (2π fC).

External subcarrier

The (B-Y) and (R-Y) signals can also be multiplied with an external subcarrier. In this case the external subcarrier is connected to pin 1. For maximum input impedance at pin 1 $V_3 = V_{16}$ ($Z_{mi} > 1400\,\Omega$). The same RC network generate the 90° phase-shifted subcarrier. For the use of an externally generated subcarrier, applied at pin 14, the d.c. level must be the same as in the case of an RC-network generated one.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage V_{6-16}	V_P	max. 13,2 V
Total power dissipation	see derating curve (Fig. 2)	
Storage temperature range	T_{stg}	−65 to +150 °C
Operating ambient temperature	T_{amb}	−25 to +70 °C

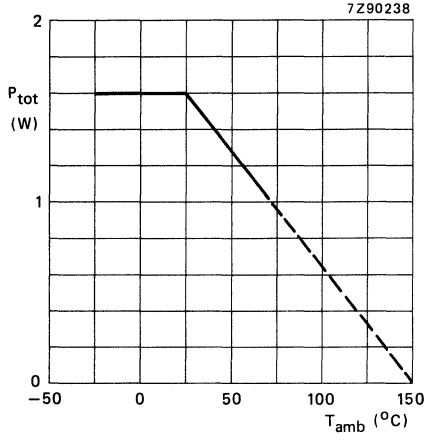


Fig. 2 Power derating curve.

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D.C. CHARACTERISTICS

$V_{6-10} = -V_{16-10} = 3$ V; $T_{amb} = 25$ °C; see Fig. 1

		min.	typ.	max.
Single power supply	V_{6-16}	5,5	6	10 V
Dual power supply				
positive	V_{6-10}	2	3	5 V
negative	$-V_{16-10}$	2,3	3	5 V
Supply current				
at pin 10	I_{10}	−1	0	3,5 mA
positive (pin 6)	I_6	28	40	64 mA
negative (pin 6)	$-I_{16}$	28	40	64 mA
Limitation d.c. level				
oscillator feedback	V_1	−30	0	+30 mV
Nominal amplitude input signal				
a.c. peak-to-peak	$V_{5(p-p)}$ $V_{12(p-p)}$	−	1	1,4 V
Input voltages (R-Y) and (B-Y)				
zero d.c. level	V_5, V_{12}	2,4	3,3	3,9 V
Required level sync input				
HIGH	V_7	4	−	V_P V
LOW	V_7	−	−	V_{10} V
Required level PAL pulse (H/2)				
HIGH	V_8	$V_{10} + 0{,}8$	−	V_P V
LOW	V_8	$-V_P$	−	0 V
Input current sync input				
$V_7 = V_P + 1$ V	I_7	−	4	15 µA
Input current PAL input (H/2)				
$V_8 = V_{10} + 0{,}8$ V	I_8	−	1,5	5 µA
Output chroma voltage swing				
(R-Y) = (B-Y) = 1,4 V				
subcarrier pulse = 0,5 V	$V_{9(p-p)}$	−	−	1,4 V
Amplitude of suppressed				
subcarrier	V_9	0	7	16 mV
Input currents				
$V_4 = V_{10}$	I_4	0	1,5	5 µA
$V_{11} = V_{10}$	I_{11}	0	1,5	5 µA
$V_{13} = V_{10}$	I_{13}	0	1,5	5 µA
$V_5 = V_{10}$	I_5	0	9	30 µA
$V_{12} = V_{10}$	I_{12}	0	9	30 µA
$V_{14} = V_{16} + 2{,}3$ V	I_{14}	−	6	− µA
Input impedance (R-Y)	Z_5	−	160	− kΩ
Input impedance (B-Y)	Z_{12}	−	160	− kΩ

Chroma Control Circuit TDA3505

The TDA3505 performs the control functions in a PAL/SECAM decoder, which also comprises the TDA3510 (PAL decoder) and/or TDA3530 (SECAM decoder).

The required input signals are: luminance and colour difference −(R-Y) and −(B-Y), while linear RGB signals can be inserted from external sources. RGB output signals are delivered for driving the video output stages. This circuit provides automatic cut-off control of the picture tube. The TDA3505 has the following features:

- capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- linear saturation control in the colour difference stages
- (G-Y) and RGB matrix
- linear transmission of inserted signals
- equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- peak beam current limiting input
- horizontal and vertical blanking and clamping of the three input signals obtained via a 3-level sandcastle pulse
- d.c. gain controls for each of the RGB output signals (white point adjustment)
- emitter-follower outputs for driving the RGB output stages
- input for automatic cut-off control of the picture tube
- compensation for leakage current of the picture tube

QUICK REFERENCE DATA

Supply voltage	$V_{6-24} = V_P$	typ.	12 V
Supply current	$I_6 = I_P$	typ.	85 mA
Composite video input signal (peak-to-peak value)	$V_{15-24(p-p)}$	typ.	0,45 V
Input resistance	R_{15-24}	>	100 kΩ
Colour difference input signals (peak-to-peak values)			
−(B-Y)	$V_{18-24(p-p)}$	typ.	1,33 V
−(R-Y)	$V_{17-24(p-p)}$	typ.	1,05 V
Inserted RGB signals (black-to-white values)	$V_{12,13,14-24(p-p)}$	typ.	1 V
Three-level sandcastle pulse (required input voltage)	V_{10-24}	typ.	2,5/4,5/8,0 V
Control voltage ranges			
brightness	V_{20-24}		1,0 to 3,0 V
contrast	V_{19-24}		2,0 to 4,3 V
saturation	V_{16-24}		2,0 to 4,3 V

PACKAGE OUTLINE 28-lead DIL; plastic (SOT-117).

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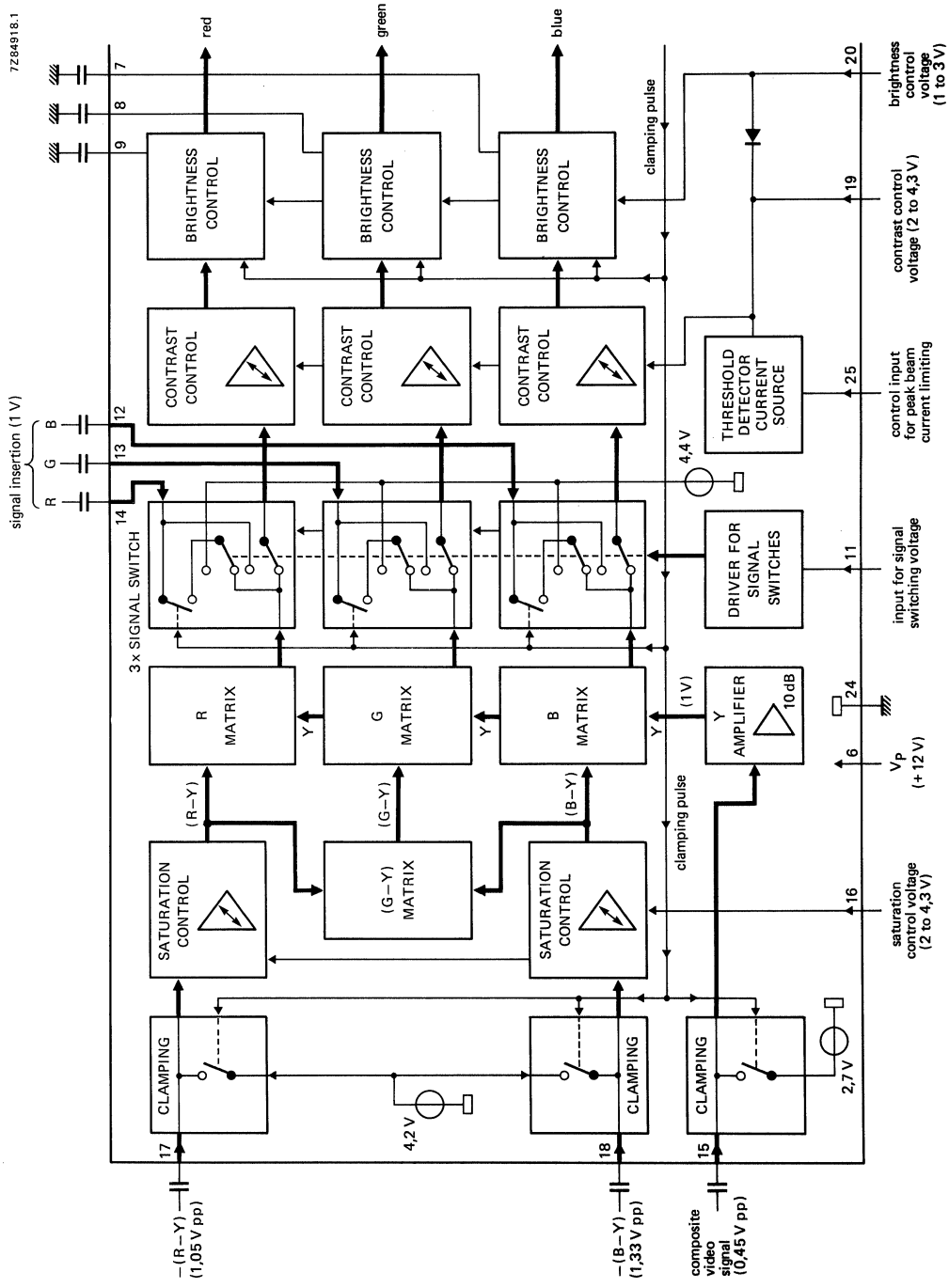

Fig. 1a Part of block diagram; continued in Fig. 1b.

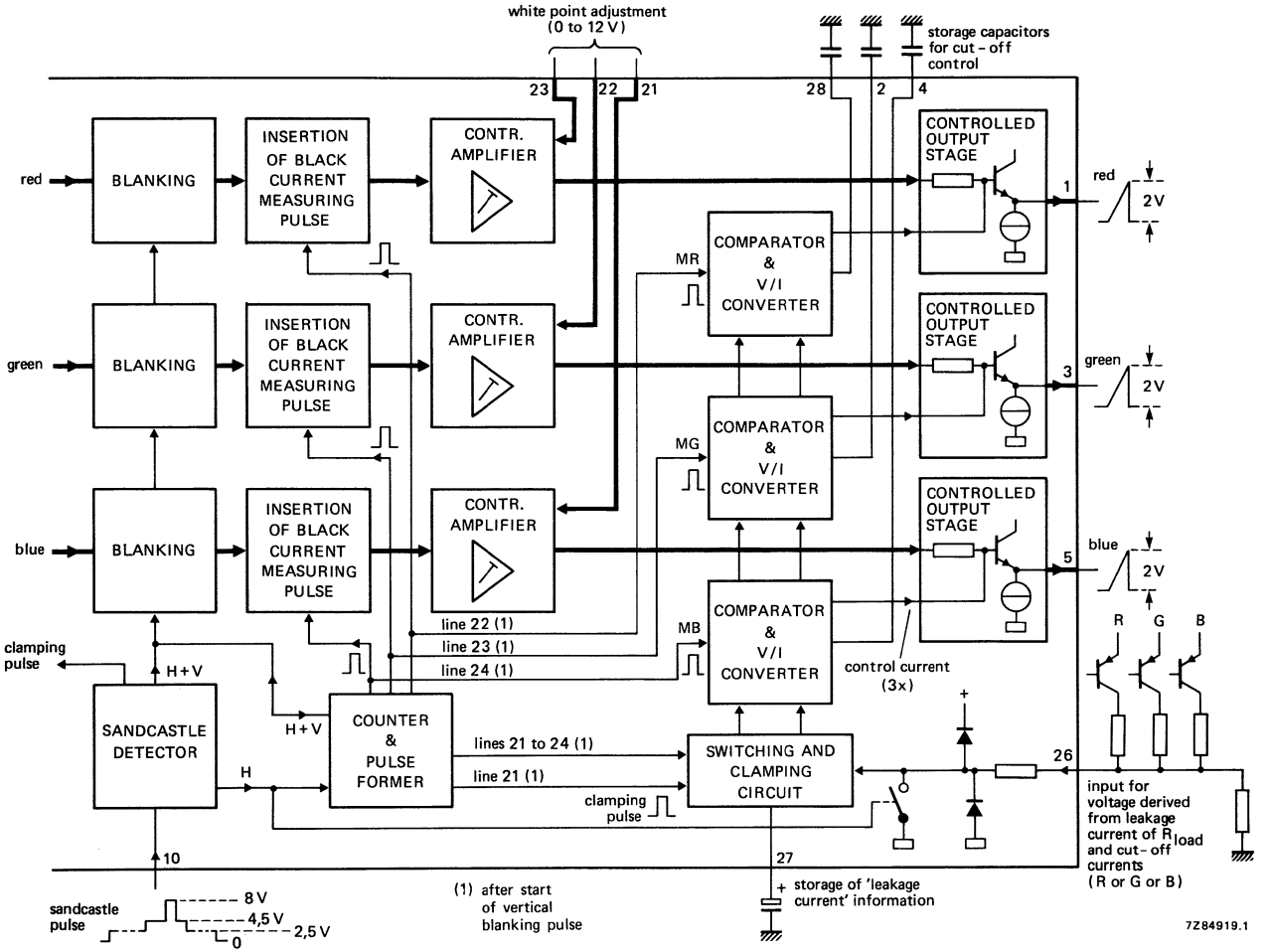

Fig. 1b Part of block diagram; continued from Fig. 1a.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		min.	max.	
Supply voltage	$V_P = V_{6-24}$	–	13,2	V
Voltages with respect to pin 24				
pin 26	V_{26-24}	0	V_P	V
pin 25	V_{25-24}	0	V_P	V
pin 10	V_{10-24}	0	V_P	V
pin 11	V_{11-24}	−0,5	3	V
pins 16, 19, 20	$V_{16,19,20-24}$	0	0,5 V_P	V
pins 21, 22, 23	$V_{21,22,23-24}$	0	V_P	V
pins 1, 3, 5; 2, 4, 28; 7, 8, 9; 12, 13, 14; 15, 17, 18; 27	no external d.c. voltage			
Currents				
pins 1, 3, 5	$-I_{1, 3, 5}$	max.	3	mA
pin 19	I_{19}	max.	10	mA
pin 20	I_{20}	max.	5	mA
pin 25	$-I_{25}$	max.	5	mA
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to +125	°C
Operating ambient temperature range	T_{amb}		−20 to +70	°C

CHARACTERISTICS

Supply voltage range	$V_P = V_{6-24}$		10,8 to 13,2	V
The following characteristics are measured in a circuit similar to Fig. 2; V_P = 12 V; T_{amb} = 25 °C; $V_{18-24(p-p)}$ = 1,33 V; $V_{17-24(p-p)}$ = 1,05 V; $V_{15-24(p-p)}$ = 0,45 V; $V_{12,13,14-24(p-p)}$ = 1 V; unless otherwise specified				
Supply current	$I_6 = I_P$	typ.	85	mA
Colour difference inputs				
−(B-Y) input signal at pin 18 (peak-to-peak value)*	$V_{18-24(p-p)}$	typ.	1,33	V
−(R-Y) input signal at pin 17 (peak-to-peak value)*	$V_{17-24(p-p)}$	typ.	1,05	V
Input current during scanning	$I_{17, 18}$	<	1	μA
Input resistance	$R_{17,18-24}$	>	100	kΩ
Internal d.c. voltage due to clamping	$V_{17,18-24}$	typ.	4,2	V
Saturation control at pin 16				
control voltage range for a change of saturation from −20 dB to +6 dB	V_{16-24}		2,1 to 4,3	V
control voltage for attenuation > 40 dB	V_{16-24}	<	1,8	V
nominal saturation (6 dB below max.)	V_{16-24}	typ.	3,1	V
input current	I_{16}	<	20	μA

* For saturated colour bar with 75% of maximum amplitude.

(G-Y) matrix

Matrixed according to the equation	$V_{(G-Y)} = -0,51\ V_{(R-Y)} - 0,19\ V_{(B-Y)}$			

Luminance amplifier (pin 15)

Composite video input signal (peak-to-peak value)	$V_{15-24(p-p)}$	typ.	0,45	V
Input resistance	R_{15-24}	>	100	kΩ
Internal d.c. voltage	V_{15-24}	typ.	2,7	V
Input current during scanning	I_{15}	<	1	μA

RGB channels

Signal switching input voltage for insertion (pin 11)				
on level	V_{11-24}		0,9 to 3	V
off level	V_{11-24}	<	0,4	V
Input current	I_{11}		−100 to + 200	μA
Signal insertion (pin 12: blue; pin 13: green; pin 14: red)				
external RGB input signal (black-to-white values)	$V_{12,13,14-24(p-p)}$	=	1	V
internal d.c. voltage due to clamping*	$V_{12,13,14-24}$	typ.	4,4	V
input current during scanning	$I_{12,13,14}$	<	1	μA
Contrast control (pin 19)				
control voltage range for a change of contrast from −18 dB to + 3 dB	V_{19-24}		2 to 4,3	V
nominal contrast (3 dB below max.)	V_{19-24}	typ.	3,6	V
control voltage for −6 dB	V_{19-24}	typ.	2,8	V
input current at $V_{25-24} \geqslant 6$ V	I_{19}	<	2	μA
Peak beam current limiting (pin 25)				
internal d.c. bias voltage	V_{25-24}	typ.	5,5	V
input resistance	R_{25-24}	typ.	10	kΩ
input current at contrast control input at V_{25-24} = 5,1 V	I_{19}	typ.	17	mA
Brightness control (pin 20)				
control voltage range	V_{20-24}		1 to 3	V
input current	$-I_{20}$	⩽	10	μA
control voltage for nominal black level which equals the inserted artificial black level	V_{20-24}	typ.	2	V
change of black level in the control range related to the nominal luminance signal (black-white) for ΔV_{20-24} = 1 V		typ.	50	%

* $V_{11-24} < 0,4$ V during clamping time: the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
$V_{11-24} > 0,9$ V during clamping time: the black levels of the inserted signals are clamped on an internal d.c. voltage.
Correct clamping of the external RGB signals is only possible when they are synchronous with the sandcastle pulse.

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CHARACTERISTICS (continued)

Internal signal limiting				
signal limiting for nominal luminance (black to white = 100%)				
black		typ.	−25	%
white		typ.	120	%
White point adjustment (pin 21: blue; pin 22: green; pin 23: red)				
A.C. voltage gain (note 1)				
at $V_{21,22,23-24}$ = 5,5 V		typ.	100	%
at $V_{21,22,23-24}$ = 0 V		=	60	%
at $V_{21,22,23-24}$ = 12 V		=	140	%
Input resistance	$R_{21,22,23-24}$	typ.	20	kΩ
Emitter-follower outputs (pin 1: red; pin 3: green; pin 5: blue)				
At nominal contrast, saturation and white point adjustment				
Output voltage (black-to-white signal, positive)	$V_{1,3,5-24(p-p)}$	typ.	2	V
Black level without automatic cut-off control ($V_{28,2,4-24}$ = 10 V)	$V_{1,3,5-24}$	typ.	6,7	V
Internal current source	I_{source}	typ.	3	mA
Cut-off current control range	$-\Delta V_{1,3,5-24}$	typ.	4,6	V
Automatic cut-off control (pin 26)				
The measurement occurs in the following lines after start of the vertical blanking pulse: line 21: measurement of leakage current; line 22: measurement of red cut-off current; line 23: measurement of green cut-off current; line 24: measurement of blue cut-off current				
Input voltage range	V_{26-24}		0 to + 6,5	V
Voltage difference between cut-off current measurement (note 2) and leakage current measurement (note 3)	ΔV_{26-24}	typ.	0,7	V
Input 26 switches to ground during horizontal flyback				

Notes

1. With input pins 21, 22 and 23 not connected an internal bias voltage of 5,5 V is supplied.
2. Black level of measured channel is nominal; the other two channels are blanked to ultra-black.
3. All three channels blanked to ultra-black.
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
   The internal signal blanking continues until the end of the last measurement line.
   The vertical blanking pulse is not allowed to contain more than 34 line pulses otherwise another control cycle begins.

Gain data

At nominal contrast, saturation and white point adjustment

Voltage gain with respect to Y-input (pin 15)	$G_{1,3,5\text{-}15}$	typ.	16 dB
Frequency response (0 to 5 MHz)	$d_{1,3,5\text{-}15}$	$\leqslant$	3 dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)	$G_{5\text{-}18} = G_{1\text{-}17}$	typ.	6 dB
Frequency response (0 to 2 MHz)	$d_{5\text{-}18} = d_{1\text{-}17}$	$\leqslant$	3 dB
Voltage gain of inserted signals	$G_{1\text{-}14} = G_{3\text{-}13} = G_{5\text{-}12}$	typ.	6 dB
Frequency response (0 to 6 MHz)	$d_{1\text{-}14} = d_{3\text{-}13} = d_{5\text{-}12}$	$\leqslant$	3 dB

Sandcastle detector (pin 10)

There are 3 internal thresholds (proportional to V_P); note 1. The following amplitudes are required for separating the various pulses:

horizontal and vertical blanking pulses (note 2)	$V_{10\text{-}24}$	$>$ $<$	2 V 3 V
horizontal pulse	$V_{10\text{-}24}$	$>$ $<$	4 V 5 V
clamping pulse (note 3)	$V_{10\text{-}24}$	$>$	7,5 V
d.c. voltage for artificial black level (scan and flyback)	$V_{10\text{-}24}$	$>$	7,5 V
no keying	$V_{10\text{-}24}$	$<$	1 V
input current	$-I_{10}$	$<$	110 μA

Notes

1. The thresholds are for
   horizontal and vertical blanking: $V_{10\text{-}24} = 1{,}5$ V
   horizontal pulse: $V_{10\text{-}24} = 3{,}5$ V
   clamping pulse: $V_{10\text{-}24} = 7{,}0$ V
2. Blanking to ultra-black (−25%).
3. Pulse duration $\geqslant 3{,}5\ \mu$s.

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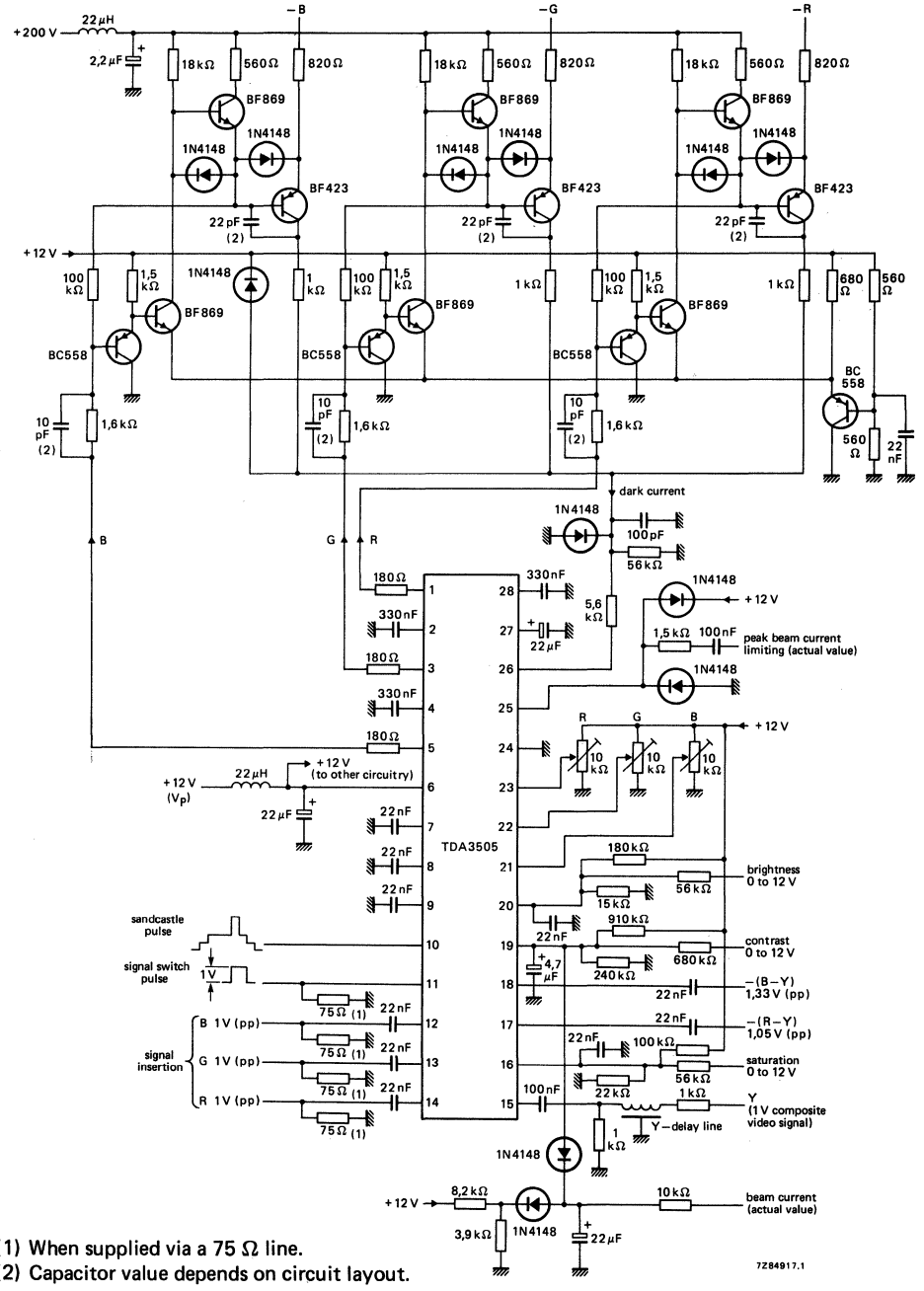

(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using the TDA3505.

GENERAL DESCRIPTION

The TDA3562A is a monolithic integrated decoder for the PAL and/or NTSC colour television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 4 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. Teletext/broadcast Antiope), channel number display, etc.

Features

- A black-current stabilizer which controls the black-currents of the three electron-guns to a level low enough to omit the black-level adjustment
- Contrast control of inserted RGB signals
- No black-level disturbance when non-synchronized external RGB signals are available on the inputs
- NTSC capability with hue control

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1-27}$	typ.	12 V
Supply current (pin 1)	$I_P = I_I$	typ.	80 mA
Luminance amplifier (pin 8)			
Input voltage (peak-to-peak value)	$V_{8-27(p-p)}$	typ.	450 mV
Contrast control range		typ.	20 dB
Chrominance amplifier (pin 4)			
Input voltage range (peak-to-peak value)	$V_{4-27(p-p)}$		40 to 1100 mV
Saturation control range		min.	50 dB
RGB matrix and amplifiers			
Output voltage at nominal luminance and contrast (peak-to-peak value)	$V_{13,15,17-27(p-p)}$	typ.	4 V
Data insertion			
Input signals (peak-to-peak value)	$V_{12,14,16-27(p-p)}$	typ.	1 V
Data blanking (pin 9)			
Input voltage for data insertion	V_{9-27}	min.	0.9 V
Sandcastle input (pin 7)			
Blanking input voltage	V_{7-27}	typ.	1.5 V
Burst gating and clamping input voltage	V_{7-27}	typ.	7 V

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PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT-117).

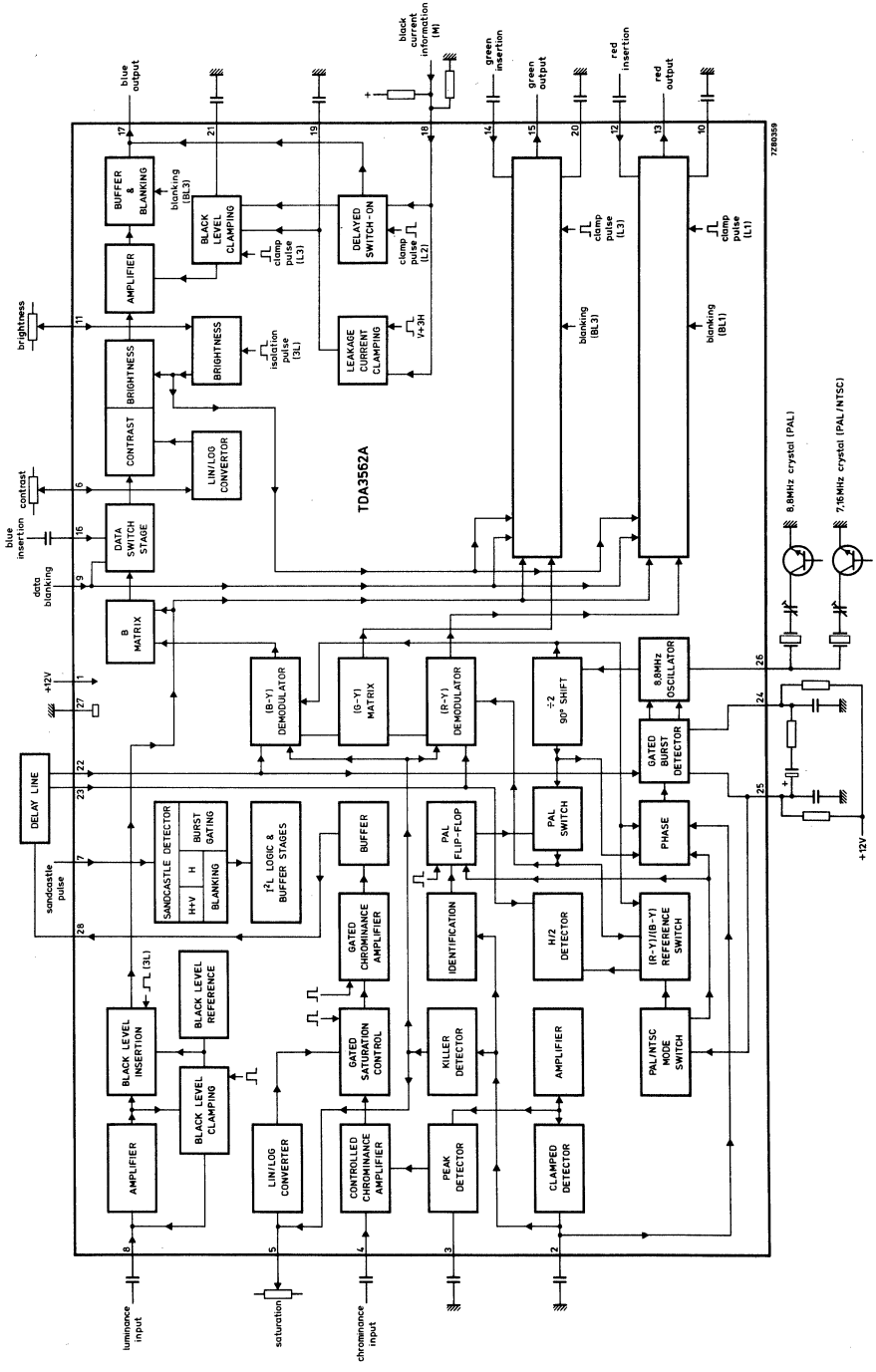

Fig. 1 Block diagram; for explanation of pulse mnemonics see Fig. 6.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal is a.c. coupled to the input (pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed d.c. level by the black level clamping circuit.

During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit. This black level reference voltage is controlled via pin 11 (brightness). At the same time the RGB signals are clamped. Noise and residual signals have no influence during clamping thus simple internal clamping circuitry is used.

Chrominance amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be a.c. coupled (pin 4) and have a minimum amplitude of 40 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1.1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation control stage. Saturation is linear controlled via pin 5. The control voltage range is 2 to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12 dB higher gain during the chrominance signal. As a result the signal at the output (pin 28) has a burst to chrominance ratio which is 6 dB lower than that of the input signal when the saturation control is set at −6 dB. The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (pins 22 and 23). These signals are fed to the burst phase detector.

Oscillator and identification circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (pin 7). In the detector the (R-Y) and (B-Y) signals are added to provide the composite burst signal again. This composite signal is compared with the oscillator signal divided-by-2 (R-Y) reference signal. The control voltage is available at pins 24 and 25, and is also applied to the 8.8 MHz oscillator. The 4.4 MHz signal is obtained via the divide-by-2 circuit, which generates both the (B-Y) and (R-Y) reference signals and provides a 90° phase shift between them.

The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R-Y) reference signal coming from the PAL switch, is compared to the vertical signal (R-Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst. When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the a.c.c. To avoid 'blooming-up' of the picture under weak input signal conditions the a.c.c. voltage is generated by peak detection of the H/2 detector output signal.

The killer and identification circuits get their information from a gated output signal of the H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression. The time constant of the saturation control (pin 5) provides a delayed switch-on after killing.

Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between pins 24 and 25 (see Fig. 7). With this application the trimmer capacitor in series with the 8.8 MHz crystal (pin 26) can be replaced by a fixed value capacitor to compensate for unbalance of the phase detector.

FUNCTIONAL DESCRIPTION (continued)

Demodulator

The (R-Y) and (B-Y) demodulators are driven by the colour difference signals from the delay-line matrix circuit and the reference signals from the 8.8 MHz divider circuit. The (R-Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G-matrix. The demodulation circuits are killed and blanked by by-passing the input signals.

NTSC mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (pins 24 and 25) is adjusted below 9 V. To ensure reliable application the phase detector load resistors are external. When the TDA3562A is used only for PAL these two 33 kΩ resistors must be connected to + 12 V (see Fig. 7). For PAL/NTSC application the value of each resistor must be reduced to 10 kΩ and connected to the slider of a potentiometer (see Fig. 8). The switching transistor brings the voltage at pins 24 and 25 below 9 V which switches the circuit to the NTSC mode. The position of the PAL flip-flop ensures that the correct phase of the (R-Y) reference signal is supplied to the (R-Y) demodulator. The drive to the H/2 detector is now provided by the (B-Y) reference signal. In the PAL mode it is driven by the (R-Y) reference signal.

Hue control is realized by changing the phase of the reference drive to the burst phase detector. This is achieved by varying the voltage at pins 24 and 25 between 7.5 and 8.5 V, nominal position 8.0 V. The hue control characteristic is shown in Fig. 5.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.

The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal, which is then fed to the contrast control stage. The contrast control voltage is supplied to pin 6 (high-input impedance). The control range is + 5 dB to −15 dB nominal. The relationship between the control voltage and the gain is linear (see Fig. 2).

During the 3-line period after blanking a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at pin 11. This applies a variable offset to the normal black level, thus providing brightness control. The brightness control range is 1 V to 3 V.

While this offset level is present, the 'black-current' input impedance (pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at pin 19 with the voltage developed across the external resistor network R_A and R_B (pin 18) which is provided by picture tube beam current. The output of the comparator is stored in capacitors connected from pins 10, 20 and 21 to ground which controls the black level at the output. The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.

The RGB output signals can never exceed a level of 10 V. When the signal tends to exceed this level the output signal is clipped. The black level at the outputs (pins 13, 15 and 17) will be about 3 V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (pin 18) via a resistor network.

Data insertion

Each colour amplifier has a separate input for data insertion. A 1 V peak-to-peak input signal provides a 4 V peak-to-peak output signal. To avoid the 'black-level' of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore a.c. coupling is required for the data inputs. To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150 Ω.

The data insertion circuit is activated by the data blanking input (pin 9). When the voltage at this pin exceeds a level of 0.9 V, the RGB matrix circuits are switched off and the data amplifiers are switched on. To avoid coloured edges, the data blanking switching time is short.

The amplitude of the data output signals is controlled by the contrast control at pin 6. The black level is equal to the video black level and can be varied between 2 and 4 V (nominal condition) by the brightness control voltage at pin 11.

Non-synchronized data signals do not disturb the black level of the internal signals.

Blanking of RGB and data signals

Both the RGB and data signals can be blanked via the sandcastle input (pin 7). A slicing level of 1.5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of + 1 V is available at the output.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-27}$	max.	13.2	V
Total power dissipation	P_{tot}	max.	1.7	W
Storage temperature range	T_{stg}		−25 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	40	K/W

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CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ V; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1-27}$	10.8	12	13.2	V
Supply current	$I_P = I_1$	–	80	110	mA
Total power dissipation	P_{tot}	–	0.95	1.3	W
Luminance amplifier (pin 8)					
Input voltage (note 1) (peak-to-peak value)	$V_{8-27(p-p)}$	–	0.45	–	V
Input level before clipping	V_{8-27}	–	–	1	V
Input current	I_8	–	0.1	1	μA
Contrast control range (see Fig. 2)		−15	–	+5	dB
Input current contrast control	I_7	–	–	15	μA
Chrominance amplifier (pin 4)					
Input voltage (note 2) (peak-to-peak value)	$V_{4-27(p-p)}$	40	390	1100	mV
Input impedance	$\lvert Z_{4-27}\rvert$	–	10	–	kΩ
Input capacitance	C_{4-27}	–	–	6.5	pF
A.C.C. control range		30	–	–	dB
Change of the burst signal at the output over the whole control range		–	–	1	dB
Gain at nominal contrast/saturation pin 4 to pin 28 (note 3)		34	–	–	dB
Chrominance to burst ratio at nominal saturation (notes 2 and 3) at pin 28		–	12	–	dB
Maximum output voltage (peak-to-peak value); $R_L = 2$ kΩ	$V_{28-27(p-p)}$	4	5	–	V
Distortion of chrominance amplifier at $V_{28-27(p-p)} = 2$ V (output) up to $V_{4-27(p-p)} = 1$ V (input)	d	–	–	5	%
Frequency response between 0 and 5 MHz	α_{28-4}	–	–	−2	dB
Saturation control range (see Fig. 3)		50	–	–	dB
Input current saturation control (pin 5)	I_5	–	–	20	μA
Cross-coupling between luminance and chrominance amplifier (note 4)		–	–	−46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\varphi$	–	–	± 5	deg
Output impedance of chrominance amplifier	$\lvert Z_{28-27}\rvert$	–	10	–	Ω
Output current	I_{28}	–	–	15	mA

parameter	symbol	min.	typ.	max.	unit
Reference part					
Phase-locked-loop catching range (note 6)	Δf	500	700	–	Hz
phase shift for ± 400 Hz deviation of f_{osc} (note 6)	$\Delta\varphi$	–	–	5	deg
Oscillator temperature coefficient of oscillator frequency (note 6)	TC_{osc}	–	–2	–	Hz/K
frequency variation when supply voltage increases from 10 V to 13.2 V (note 6)	Δf_{osc}	–	40	–	Hz
input resistance (pin 26)	$R_{26\text{-}27}$	–	400	–	Ω
input capacitance (pin 26)	$C_{26\text{-}27}$	–	–	10	pF
A.C.C. generation (pin 2) control voltage at nominal input signal	$V_{2\text{-}27}$	–	4.5	–	V
control voltage without chrominance input	$V_{2\text{-}27}$	–	2.0	–	V
colour-off voltage	$V_{2\text{-}27}$	–	2.8	–	V
colour-on voltage	$V_{2\text{-}27}$	–	3.0	–	V
identification-on voltage	$V_{2\text{-}27}$	–	1.7	–	V
change in burst amplitude with temperature		–	0.1	0,25	%/K
voltage at pin 3 at nominal input signal	$V_{3\text{-}27}$	–	5.1	–	V
Demodulator part					
Input burst signal amplitude (peak-to-peak value) between pins 23 and 27 (note 7)	$V_{23\text{-}27(p\text{-}p)}$	–	80	–	mV
Input impedance between pins 22 or 23 and 27	$\lvert Z_{22\text{-}27/23\text{-}27}\rvert$	–	1	–	kΩ
Ratio of demodulated signals (note 8) (B-Y)/(R-Y)	$\frac{V_{17\text{-}27}}{V_{13\text{-}27}}$	–	1.78 ± 10%	–	
(G-Y)/(R-Y); no (B-Y) signal	$\frac{V_{15\text{-}27}}{V_{13\text{-}27}}$	–	–0.51 ± 10%	–	
(G-Y)/(B-Y); no (R-Y) signal	$\frac{V_{15\text{-}27}}{V_{17\text{-}27}}$	–	–0.19 ± 25%	–	
Frequency response between 0 and 1 MHz		–	–	–3	dB
Cross-talk between colour difference signals		40	–	–	dB
Phase difference between (R-Y) signal and (R-Y) reference signal	$\Delta\varphi$	–	–	5	deg
Phase difference between (R-Y) and (B-Y) reference signals	$\Delta\varphi$	85	90	95	deg

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CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers					
Output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white) (note 3)	$V_{13,15,17\text{-}27(p\text{-}p)}$	3.5	4	4.5	V
Output voltage at pin 13 (peak-to-peak value) at nominal contrast/saturation and no luminance signal to (R-Y)	$V_{13\text{-}27(p\text{-}p)}$	–	4.2	–	V
Maximum peak-white level	$V_{13,15,17(m)}$	9.7	10	10.3	V
Available output current (pins 13,15,17)	$I_{13,15,17}$	10	–	–	mA
Difference between black level and measuring level at the output for a brightness control voltage at pin 11 of 2 V (note 9)	$\Delta V_{13,15,17\text{-}27}$	–	0	–	V
Difference in black level between the three channels without black current stabilization (note 10)		–	–	100	mV
Control range of black-current stabilization at V_{b1} = 3 V; $V_{11\text{-}27}$ = 2 V		–	–	±2	V
Black level shift with vision contents		–	–	40	mV
Brightness control voltage range			see Fig. 4		
Brightness control input current	I_{11}	–	–	5	μA
Variation of black level with temperature	$\Delta V/\Delta T$	–	0	–	mV/K
Variation of black level with contrast*	ΔV	–	–	100	mV
Relative spread between the R, G and B output signals		–	–	10	%
Relative black-level variation between the three channels during variation of contrast, brightness and supply voltage (± 10%)		–	0	20	mV
Differential black-level drift over a temperature range of 40 °C*		–	0	20	mV
Blanking level at the RGB outputs		–	0.95	1.1	V
Difference in blanking level of the three channels		–	0	–	mV
Differential drift of the blanking levels over a temperature range of 40 °C		–	0	–	mV
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	–	1	–	
Tracking of contrast control between the three channels over a control range at 10 dB		–	–	0.5	dB

* With respect to the measuring pulses.

parameter	symbol	min.	typ.	max.	unit
Output signal during the clamp pulse (3L) after switch-on		7.5	–	–	V
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 4,4 MHz signal at RGB outputs (peak-to-peak value)		–	–	50	mV
Residual 8.8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		–	–	150	mV
Output impedance of RGB outputs	$\lvert Z_{13,15,17-27}\rvert$	–	50	–	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		–	–1	–3	dB
Current source of output stage		2	3	–	mA
Difference of black level at the three outputs at nominal brightness *		–	–	10	mV
Tracking of brightness control		–	–	2	%
Data insertion (pins 12, 14 and 16)					
Input signals (peak-to-peak value) for an RGB output voltage of 4 V (peak-to-peak) at nominal contrast	$V_{12,14,16-27(p-p)}$	0.9	1	1.1	V
Difference between the black levels of the RGB signals and the inserted signals at the output (note 11)	ΔV	–	–	100	mV
Output rise time	t_r	–	–	80	ns
Differential delay time for the three channels	t_d	–	0	40	ns
Input current	$I_{12,14,16}$	–	–	10	μA
Data blanking (pin 9)					
Input voltage for no data insertion	V_{9-27}	–	–	0.4	V
Input voltage for data insertion	V_{9-27}	0.9	–	–	V
Maximum input voltage	$V_{9-27(m)}$	–	–	3	V
Delay of data blanking	t_d	–	–	20	ns
Input resistance	R_{9-27}	7	10	13	kΩ
Suppression of the internal RGB signals when $V_{9-27} > 0.9$ V		46	–	–	dB

* With respect to the measuring pulses.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Sandcastle input (pin 7)					
Level at which the RGB blanking is activated	V_{7-27}	1	1.5	2	V
Level at which the horizontal pulses are separated	V_{7-27}	3	3.5	4	V
Level at which burst gating and clamping pulse are separated	V_{7-27}	6.5	7.0	7.5	V
Delay between black level clamping and burst gating pulse	t_d	–	0.6	–	μs
Input current					
at V_{7-27} = 0 to 1 V	$-I_7$	–	–	1	mA
at V_{7-27} = 1 to 8.5 V	I_7	–	50	–	μA
at V_{7-27} = 8.5 to 12 V	I_7	–	–	2	mA
Black current stabilization (pin 18)					
D.C. bias voltage	V_{18-27}	3.5	5	7.0	V
Difference between input voltage for 'black' current and leakage current	ΔV	–	0.5	–	V
Input current during 'black' current	I_{18}	–	–	1	μA
Input current during scan	I_{18}	–	–	10	mA
Internal limiting at pin 10	V_{10-27}	–	9	–	V
Switching threshold for 'black' current control ON	V_{1-27}	–	8	–	V
Input resistance during scan	R_{1-27}	–	1.5	–	kΩ
D.C. input current during scan at pins 10, 20 and 21	$I_{10,20,21}$	–	–	50	nA
Maximum charge/discharge current during measuring time at pins 10,19,20 and 21	$I_{c/d}$	–	10	–	mA
NTSC					
Level at which the PAL/NTSC switch is activated (pins 24 and 25)	V_{24-25}	–	9	–	V
Average output current (note 12)	I_{24+25}	75	90	105	μA
Hue control			see Fig. 5		

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2.2 : 1.
3. Nominal contrast is specified as the maximum contrast −5 dB and nominal saturation as the maximum saturation −6 dB.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to r.m.s. noise.
6. All frequency variations are referred to 4.4 MHz carrier frequency.
7. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
8. The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal. This also applies to the (B-Y) signals.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5 V) but in that application the amplitude of the output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discolouration during adjustments of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. This difference occurs when the source impedance of the data signals is 150 Ω and the black level clamp pulse width is 4 μs (sandcastle pulse). For a lower impedance the difference will be lower.
12. The voltage at pins 24 and 25 can be changed by connecting the load resistors (10 kΩ in this application) to the slider bar of the hue control potentiometer (see Fig. 8). When the transistor is switched on, the voltage at pins 24 and 25 is reduced below 9 V, and the circuit is switched to NTSC mode.

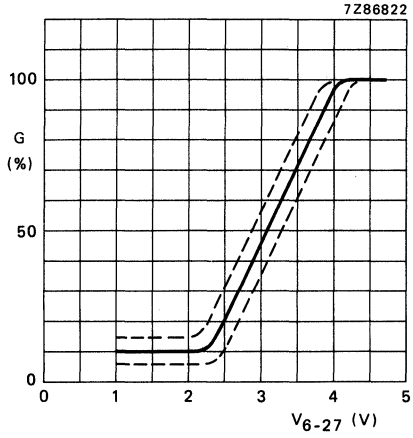

Fig. 2 Contrast control voltage range.

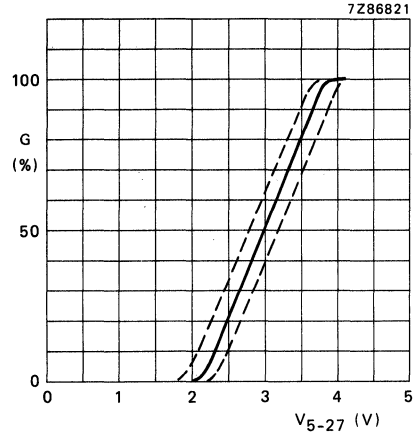

Fig. 3 Saturation control voltage range.

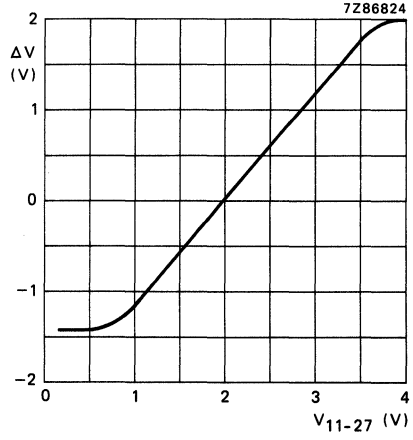

Fig. 4 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the brightness control input voltage (V_{11-27}).

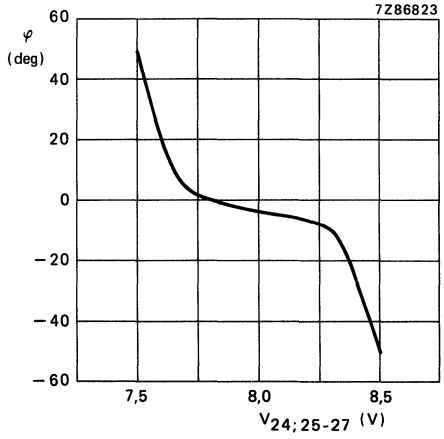

Fig. 5 Hue control voltage range.

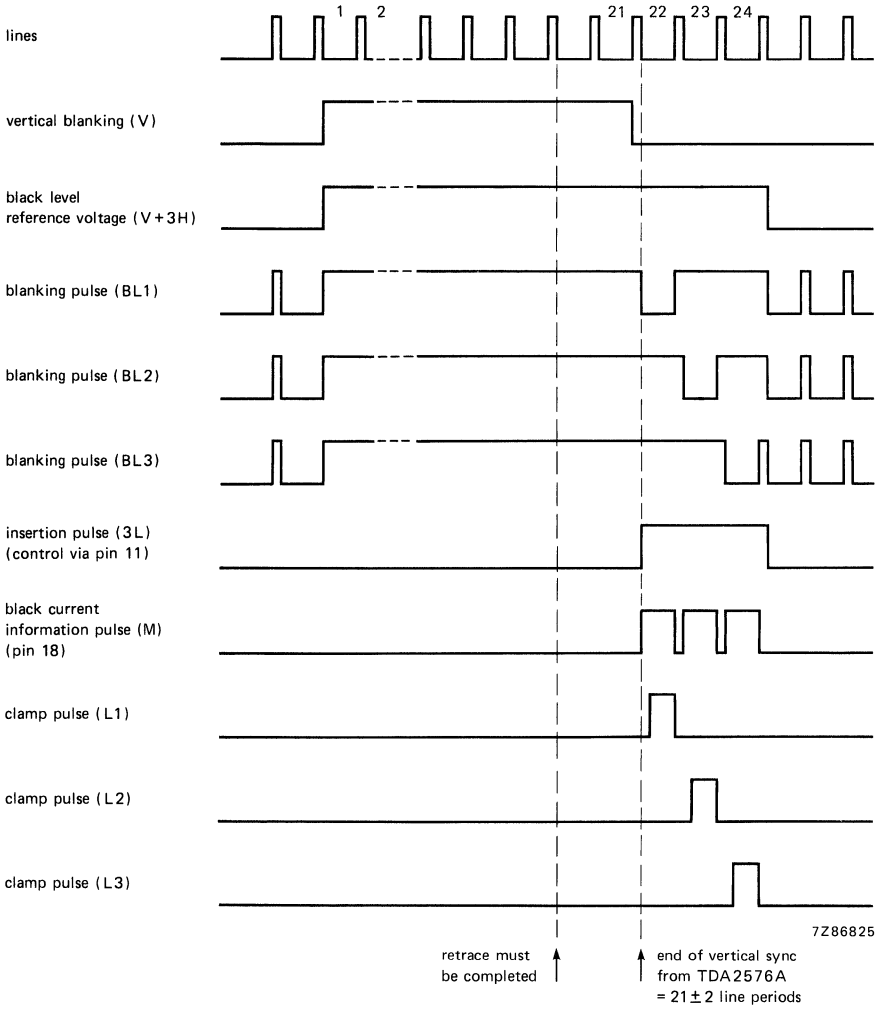

Fig. 6 Timing diagram for black-current stabilizing.

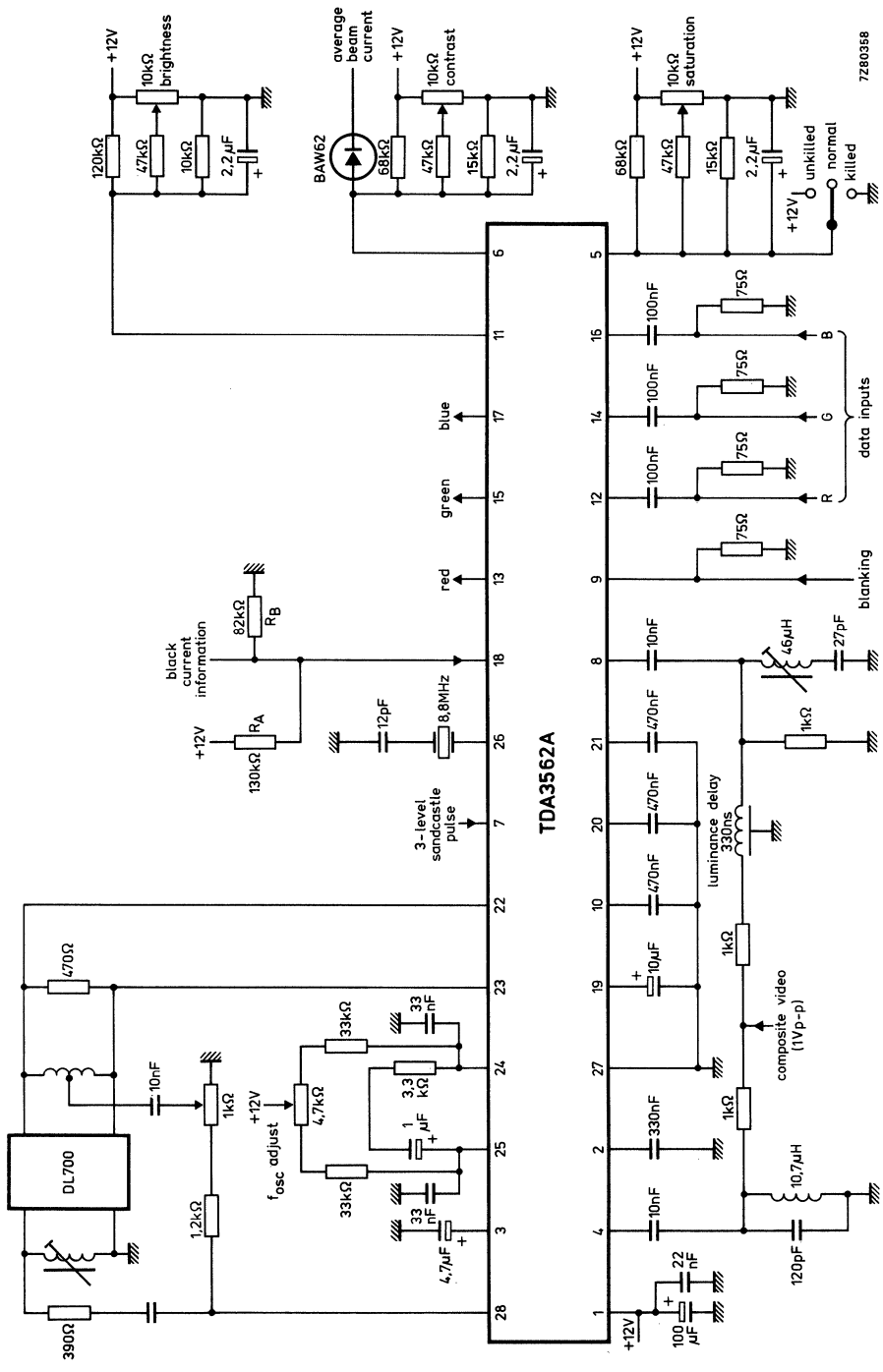

Fig. 7 Application diagram showing the TDA3562A for a PAL decoder.

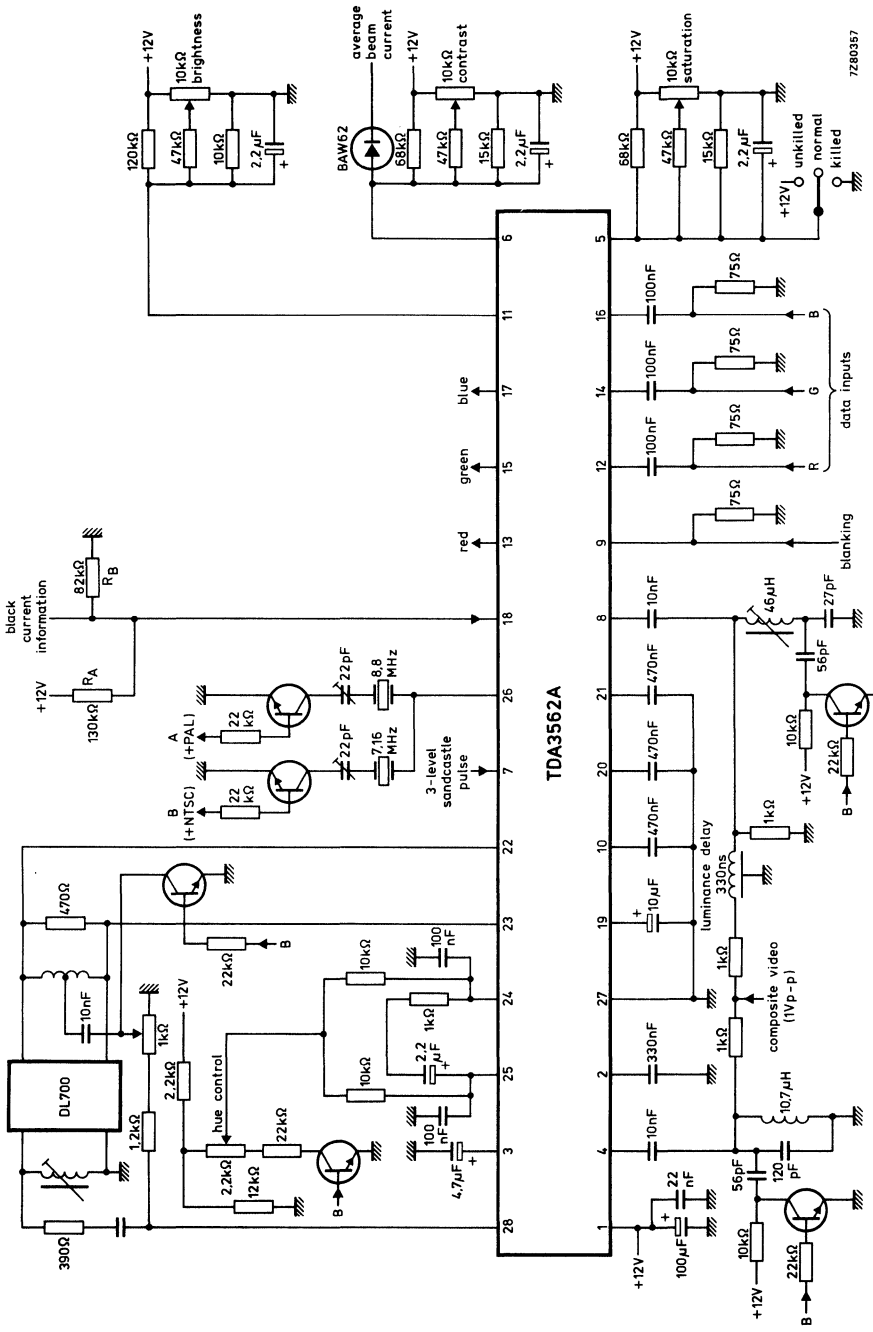

Fig. 8 Application diagram showing the TDA3562A for a PAL/NTSC decoder.

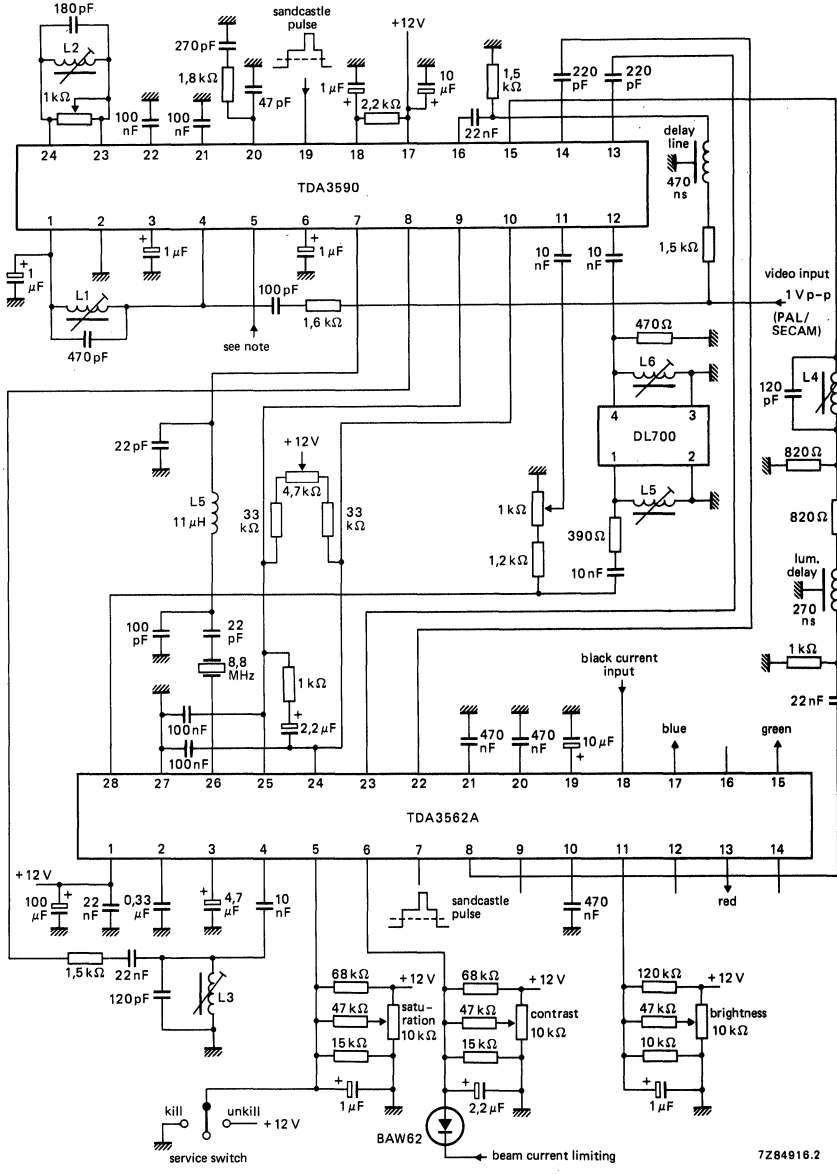

Fig. 9 PAL/SECAM application circuit diagram using the TDA3590 and TDA3562A.

Note to pin 5 TDA3590:

$V_{5\text{-}2} < 1$ V; horizontal identification and black level clamping.
$V_{5\text{-}2} > 11$ V; vertical identification and artificial black level.
$V_{5\text{-}2} = 5$ to 7 V; horizontal identification and artificial black level.

NTSC Decoder with RGB Inputs TDA3563

GENERAL DESCRIPTION

The TDA3563 is a monolithic integrated colour decoder for the NTSC standard. It combines all functions required for the identification and demodulation of NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply signals up to 5,3 V peak-to-peak (picture information) enabling direct drive of the output stages. The circuit also contains inputs for data insertion, analogue as well as digital, which can be used for Teletext information, channel number display, etc.

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1-27}$	typ.	12 V
Supply current (pin 1)	$I_P = I_1$	typ.	85 mA
Luminance input signal (peak-to-peak value)	$V_{10-27(p-p)}$	typ.	0,45 V
Chrominance input signal (peak-to-peak value)	$V_{3-27(p-p)}$		55 to 1100 mV
Data input signals (peak-to-peak value)	$V_{13;15;17-27(p-p)}$	typ.	1 V
RGB output signals at nominal contrast and saturation (peak-to-peak value)	$V_{12;14;16-27(p-p)}$	typ.	5,3 V
Contrast control range		typ.	20 dB
Saturation control range		min.	50 dB
Input voltage for fast video-data signal switching	V_{9-27}	min.	0,9 V
Blanking input voltage	V_{8-27}	typ.	1,5 V
Burst gating and black-level gating input voltage	V_{8-27}	typ.	7 V

8

PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT-117).

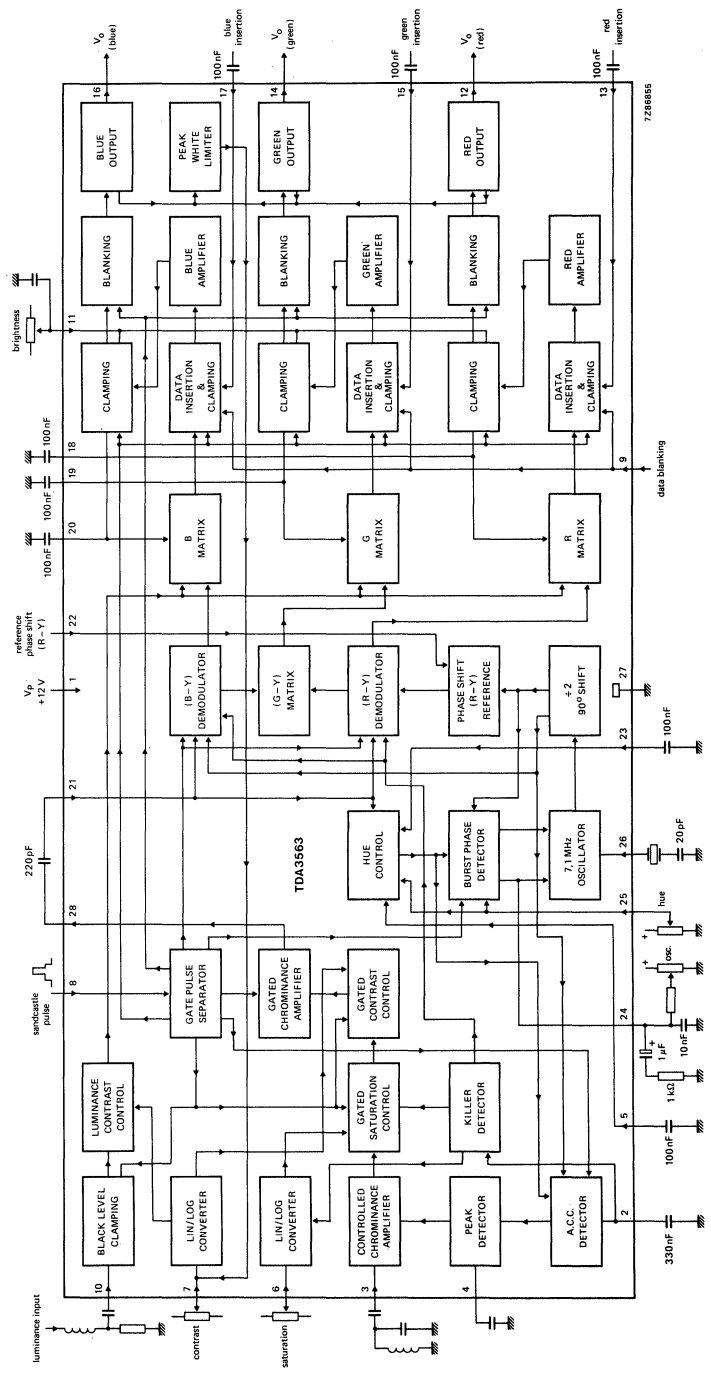

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-27}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1,7	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		−25 to +65	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	50	K/W

CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1-27}$	10	12	13,2	V
Supply current	$I_P = I_1$	–	85	115	mA
Total power dissipation	P_{tot}	–	1	1,4	W
Luminance amplifier					
Input voltage (note 1) (peak-to-peak value)	$V_{10-27(p-p)}$	–	0,45	–	V
Contrast control range (see Fig. 2)		–17	–	+3	dB
Control voltage for an attenuation of 40 dB		–	1,2	–	V
Contrast control input current	I_7	–	–	15	μA
Chrominance amplifier					
Input voltage (note 2) (peak-to-peak value)	$V_{3-27(p-p)}$	55	550	1100	mV
A.C.C. control range		30	–	–	dB
Change of the burst signal at the output over the whole control range		–	–	1	dB
Output voltage (note 3) (peak-to-peak value) at a burst signal of 0,3 V peak to peak	V_{28-27}	–	0,15	–	V
Maximum output voltage range (peak-to-peak value); $R_L = 2$ kΩ	V_{28-27}	–	4	–	V
Frequency response between 0 and 5 MHz	α_{28-3}	–	–	–2	dB
Saturation control range (see Fig. 3)		50	–	–	dB
Saturation control input current	I_6	–	–	20	μA
Output impedance of chrominance amplifier	$\lvert Z_{28-27} \rvert$	–	25	–	Ω
Output current	I_{28}	–	–	10	mA
Reference part					
Phase-locked loop					
Catching range (note 4)	Δf	500	700	–	Hz
Phase shift (notes 4 and 5)	$\Delta\varphi$	–	–	5	deg
Oscillator					
Temperature coefficient of oscillator frequency (note 4)	TC_{osc}	–	–1,5	–	Hz/K
Frequency variation when supply voltage increases from 10 V to 13,2 V (note 4)	Δf_{osc}	–	40	–	Hz

parameter	symbol	min.	typ.	max.	unit
Reference part (continued)					
Oscillator (continued)					
Input resistance (pin 26)	$R_{26\text{-}27}$	–	400	–	Ω
Input capacitance (pin 26)	$C_{26\text{-}27}$	–	–	10	pF
A.C.C. generation (pin 2)					
Control voltage at nominal input signal	$V_{2\text{-}27}$	–	5,0	–	V
Control voltage without chrominance input	$V_{2\text{-}27}$	–	2,7	–	V
Colour-off voltage	$V_{2\text{-}27}$	–	3,0	–	V
Colour-on voltage	$V_{2\text{-}27}$	–	3,3	–	V
Hue control					
Control range		±50	–	–	deg
Demodulator part					
Input burst signal amplitude (peak-to-peak value)	$V_{21\text{-}27(p\text{-}p)}$	–	300	–	mV
Ratio for demodulated signals for equal input signal amplitudes					
(B-Y)/(R-Y)	$\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$	–	1,06±10%	–	
(G-Y)/(R-Y); no (B-Y) signal	$\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$	–	−0,27±20%	–	
(G-Y)/(B-Y); no (R-Y) signal	$\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$	–	−0,2±20%	–	
Frequency response between 0 and 1 MHz		–	–	−3	dB
RGB matrix and amplifiers					
Output voltage (note 3) (peak-to-peak value) at nominal luminance/contrast (black-to-white)	$V_{12;14;16\text{-}27}$	4,5	5,3	6,3	V
Maximum peak-white level (note 6)	$V_{12;14;16\text{-}27}$	9,0	9,3	9,6	V
Maximum output current	$I_{12;14;16}$	–	–	10	mA
Output black level voltage for brightness control of 2 V		–	2,7	–	V
Brightness control voltage range			see Fig. 4		
Brightness control input current	I_{11}	–	–	50	μA
Relative spread between R, G and B output signals		–	–	10	%
Blanking level at RGB outputs		1,9	2,1	2,3	V
Tracking of output black level with supply voltage	$\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$	–	1,1	–	

8

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers (continued)					
Output impedance of RGB outputs	$\|Z_{12;14;16-27}\|$	–	50	–	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		–	–	–3	dB
Data insertion					
Input signals (peak-to-peak value) for an RGB output voltage of 5 V (peak-to-peak)	$V_{13;15;17-27(p-p)}$	0,9	1	1,1	V
Data blanking (pin 9)					
Input voltage for no data insertion	V_{9-27}	–	–	0,3	V
Input voltage for data insertion	V_{9-27}	0,9	–	–	V
Maximum input voltage	$V_{9-27(m)}$	–	–	2	V
Delay of data blanking	t_d	–	–	20	ns
Input current	I_9	–	–	35	μA
Sandcastle input (pin 8)					
Level at which RGB blanking is activated	V_{8-27}	1	1,5	2	V
Level at which burst gating and clamping pulse are separated	V_{8-27}	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse	t_d	–	0,4	–	μs
Input current					
at V_{8-27} = 0 to 1 V	$-I_8$	–	–	1	mA
at V_{8-27} = 1 to 8,5 V	I_8	–	20	–	μA
at V_{8-27} = 8,5 to 12 V	I_8	–	–	2	mA

Notes to the characteristics

1. Signal with negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. At nominal contrast and saturation. Nominal contrast is specified as the maximum contrast –3 dB and nominal saturation as the maximum saturation –6 dB.
4. All frequency variations are referred to 3,58 MHz carrier frequency.
5. For ± 400 Hz deviation of the oscillator frequency.
6. If the typical voltage for this white level is exceeded, the output voltage is reduced by discharging the capacitor at pin 7 (contrast control); discharge current is 1,5 mA.

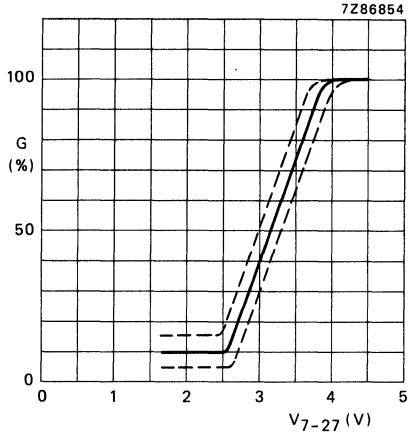

Fig. 2 Contrast control voltage range.

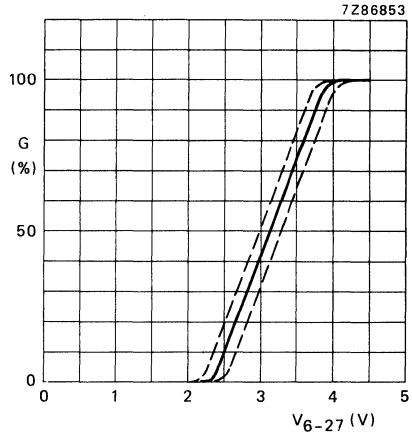

Fig. 3 Saturation control voltage range.

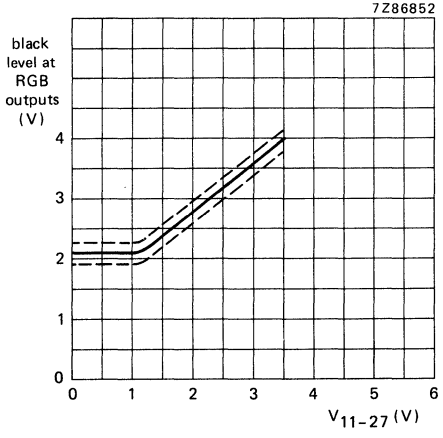

Fig. 4 Brightness control voltage range.

8

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage of the TDA3563. All signal and control levels have a linear dependency on the supply voltage. The current consumed by the IC at + 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

2. Control voltage for identification

The output pulses of the a.c.c. detector are detected with a sample-and-hold circuit to obtain information for the colour killer. The output is available at pin 2.

3. Chrominance input

The chrominance signal must be a.c.-coupled to the input. Its amplitude must be between 55 and 1100 mV peak-to-peak (25 to 500 mV peak-to-peak burst signal). All figures for the chrominance signals are based on a colour bar signal with 75% saturation, that is if the burst-to-chrominance ratio of the input is 1 : 2,2.

4. Control voltage a.c.c. detector

The shifted burst signal is synchronously demodulated in a separate a.c.c. detector to generate the a.c.c. voltage. The output pulses of this detector are peak detected to control the gain of the chrominance amplifier, thus preventing blooming-up of the colour during weak signal reception.

5. Decoupling of the 90° phase shift circuit

A control circuit is required in the 90° phase shift circuit to make the chrominance voltage independent of the hue setting. The control circuit is decoupled by a capacitor at this pin.

6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external control network is sufficiently high. Then the chrominance amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 24 and 26).

7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 V to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signals via the contrast control by discharging a 10 μF capacitor via an internal current sink.

8. Sandcastle and vertical blanking input

The output signals are blanked if the amplitude of the pulse is between 2 V and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V. The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of the video signal on the sync pulse. The duration should be about 4 μs for proper a.c.c. operation.

9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to ground (pin 27).

The switching times are very short (< 20 ns) to avoid coloured edges of the inserted signals on the screen.

10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak-white to sync) to obtain a black-white output signal of 5,3 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage. The 1 kΩ luminance delay line can be applied because the luminance impedance is very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 4). The minimum black level is identical to the blanking level. The black level can be set higher than 4 V, however, the available output signal amplitude is reduced (see also pin 7). Brightness control also operates on the black level of the inserted signals.

12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5,3 V (black-white) for nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2,1 V. The peak-white level is limited to 9 V. When this level is exceeded the output signal amplitude is reduced via the contrast control (see also pin 7).

13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak to peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to ground (pin 27).

18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

21, 22. Demodulator input and reference signal phase adjustment

The (R-Y) and (B-Y) demodulator inputs are internally connected (pin 21). The phase angle between the two reference carriers is 115°. At the nominal hue adjustment the (B-Y) signal is demodulated with a difference of 0°. The phase shift of 115° can be changing the voltage at pin 22. The gain at the two demodulators is identical. The (G-Y) is composed of −0,27(R-Y) −0,22(B-Y).

23, 25. Hue control

The hue control is obtained by changing the phase of the input signal of the burst phase detector with respect to the demodulator input signal. This phase shift is obtained by generating a 90° shifted sine-wave via a Miller integrator (biased via pin 23) which is mixed with the original burst signal.

APPLICATION INFORMATION (continued)

24, 26. Reference oscillator

As the burst phase detector has an asymmetrical output the oscillator can be adjusted by changing the voltage of the output (pin 24) via a high-ohmic resistor. The capacitor in series with the oscillator crystal must then have a fixed value. When pin 6 (saturation control) is connected to the positive supply line the burst phase detector is based in its nominal position and the colour killer is overruled. This position can therefore be used for the adjustment of the oscillator.

27. Ground

28. Output of the chrominance amplifier

The (R-Y) and (B-Y) demodulator input (pin 21) is a.c.-coupled to this output.

GENERAL DESCRIPTION

The TDA3564 is a monolithic integrated decoder for the NTSC colour television standards. It combines all functions required for the demodulation of NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages.

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_P = V_{1-23}$	typ.	12 V
Supply current (pin 1)	$I_P = I_1$	typ.	85 mA
Luminance input signal (pin 9)			
Input voltage (peak-to-peak value)	$V_{9-23(p-p)}$	typ.	450 mV
Contrast control range		typ.	−17 to + 3 dB
Chrominance amplifier (pin 3)			
Input voltage range (peak-to-peak value)	$V_{3-23(p-p)}$		55 to 1100 mV
Saturation control range		min.	50 dB
RGB matrix and amplifiers			
Output voltage at nominal luminance input signal and nominal contrast (peak-to-peak value)	$V_{13, 14, 15-23(p-p)}$	typ.	5 V
Sandcastle input (pin 8)			
Blanking input voltage	V_{8-23}	typ.	1,5 V
Burst gating and clamping input voltage	V_{8-23}	typ.	7 V

8

PACKAGE OUTLINE

24-lead DIL; plastic, with internal heat spreader (SOT-101A, B).

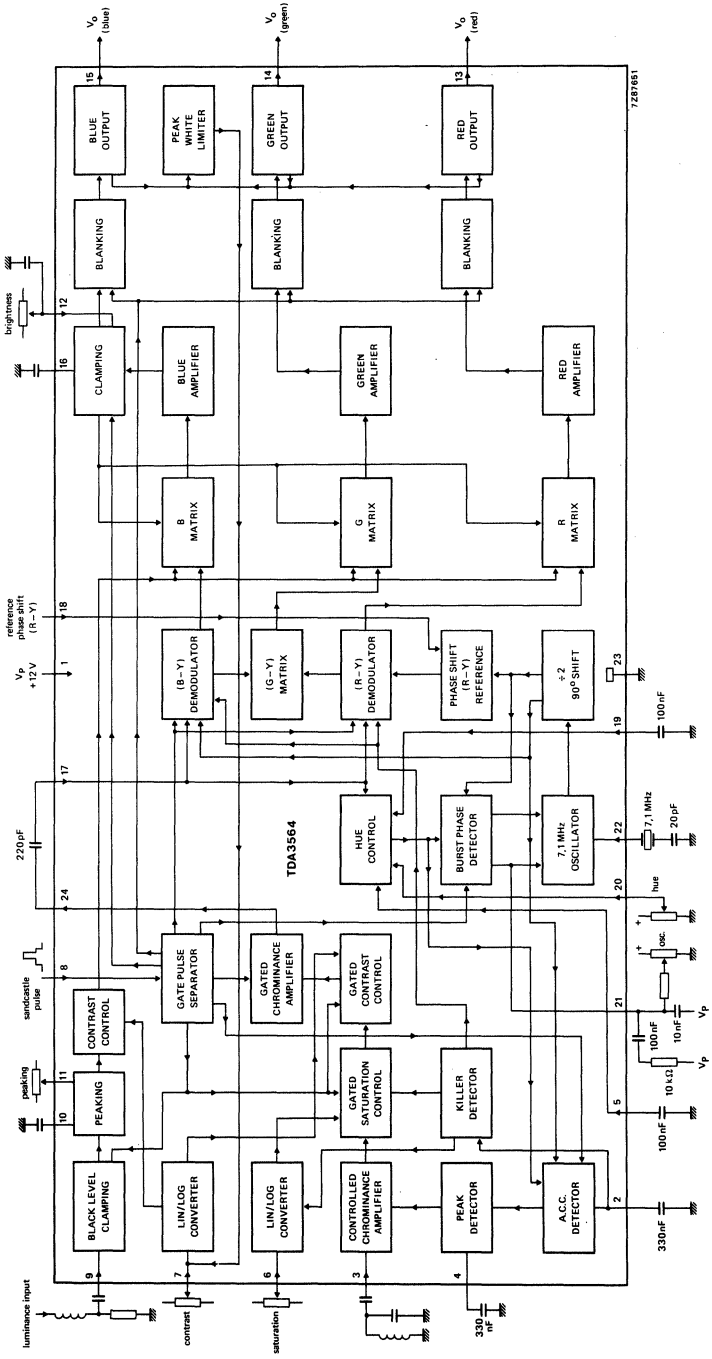

Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal is a.c. coupled to the input (pin 9).

The black level at the output of the preamplifier is clamped to a fixed d.c. level by the black level clamping circuit. The high input impedance of the luminance amplifier minimizes disturbance of the input signal black level by the source impedance (delay line matching resistors).

During clamping the low input impedance reduces noise and residual signals. After clamping the signal is fed to a peaking stage. The overshoot is defined by the capacitor connected to pin 10 and the peaking is adjusted by the control voltage at pin 11.

The peaking stage is followed by a contrast control stage. The contrast control voltage range (pin 7) is nominally −17 to + 3 dB. The linear relationship between the contrast control voltage and the gain is shown in Fig. 2.

Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal must be a.c. coupled (pin 3) and have a minimum amplitude of 55 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation and contrast control stages. Chrominance and luminance contrast control stages are directly coupled to obtain good tracking. Saturation is linearly controlled via pin 6 (see Fig. 3). The control voltage range is 2 V to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by saturation control. The output signal at pin 24 is a.c. coupled to the demodulators via pin 17.

Oscillator and a.c.c. detector

The 7,16 MHz reference oscillator operates at twice the subcarrier frequency. The reference signals for the (R-Y) and (B-Y) demodulators, burst phase detector and a.c.c. detector are obtained via the divide-by-2 circuit, which provides a 90° phase shift. The oscillator is controlled by the burst phase detector, which is gated with the narrow part of the sandcastle pulse (pin 8). As the burst phase detector has an asymmetrical output the oscillator can be adjusted by changing the voltage of the output (pin 21) via a high-ohmic resistor. The capacitor in series with the oscillator crystal must then have a fixed value. When pin 6 (saturation control) is connected to the positive supply line the burst signal is suppressed and the colour killer is overruled. This position can therefore be used for adjustment of the oscillator. The adjustment is visible on the screen.

The hue control is obtained by changing the phase of the input signal of the burst phase detector with respect to the chrominance signal applied to the demodulators. This phase shift is obtained by generating a 90° shifted sine-wave via a Miller integrator (biased via pin 19) which is mixed with the original burst signal. A control circuit is required in the 90° phase shift circuit to make the chrominance voltage independent of the hue setting. This control circuit is decoupled by a capacitor connected to pin 5.

Oscillator and a.c.c. detector

As the shifted burst signal is synchronously demodulated in a separate a.c.c. detector to generate the a.c.c. voltage, it is not affected by the hue control. The output pulses of this detector are peak detected (pin 4) to control the gain of the chrominance amplifier, thus preventing blooming-up of the colour during weak signal reception. This ensures reliable operation of the colour killer. During colour killing the colour channel is blocked by switching-off saturation control and the demodulators.

FUNCTIONAL DESCRIPTION (continued)

Demodulators

The (R-Y) and (B-Y) demodulators are driven by the chrominance signal (pin 24) and the reference signals from the 7,16 MHz divider circuit. The phase angle between the two reference carriers is 115°. This is achieved by the (R-Y) demodulator receiving an additional phase shift by mixing the two signals from the divider circuit. The phase shift of 115° can be varied between 90° and 140° by changing the bias voltage at pin 18. The demodulator output signals are fed to R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G matrix. The demodulator circuits are killed and blanked by by-passing the input signals.

RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.
The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal. Output signals are 5 $V_{(p-p)}$ (black-white) for the following nominal input signals and control settings.

- Luminance 450 $mV_{(p-p)}$
- Chrominance 550 $mV_{(p-p)}$ (burst-to-chrominance ratio of the input 1: 2,2)
- Contrast −3 dB max.
- Saturation −6 dB max.

The maximum output voltage is approximately 7 $V_{(p-p)}$.
The black level of the blue channel is compared with a variable external reference level (pin 12) which provides brightness control. The brightness control range is 1 V to 3,2 V (see Fig. 4). The control voltage is stored in a capacitor (connected to pin 16) and controls the black level at the output (pin 15) between 2 V and 4 V, via a change of the level of the luminance signal before matrixing.

Note

Black levels of up to approximately 6 V are possible, but amplitude of the output signal is reduced to 3 $V_{(p-p)}$.
If the output signal surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signal via the contrast control.

Blanking of RGB signals

The RGB signals can be blanked via the sandcastle input (pin 8). A slicing level of 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of + 2 V is available at the output.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-23}$	max.	13,2 V
Total power dissipation	P_{tot}	max.	1,7 W
Storage temperature range	T_{stg}	−25 to + 150	°C
Operating ambient temperature range	T_{amb}	−25 to + 65	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j-a}$	=	50 K/W

CHARACTERISTICS

$V_P = V_{1-23} = 12$ V; $T_{amb} = 25\ ^oC$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 1)					
Supply voltage	$V_P = V_{1-23}$	8	12	13,2	V
Supply current	$I_P = I_1$	–	85	–	mA
Total power dissipation	P_{tot}	–	1,0	–	W
Luminance amplifier (pin 9)					
Input voltage (note 1) (peak-to-peak value)	$V_{9-23(p-p)}$	–	450	–	mV
Input level before clipping	V_{9-23}	–	–	2	V
Input current	I_9	–	0,15	1	μA
Contrast control range (see Fig. 2)		–17	–	+ 3	dB
Control voltage for an attenuation of 40 dB		–	1,2	–	V
Input current contrast control	I_7	–	–	15	μA
Peaking of luminance signal					
Output impedance (pin 10)	$\lvert Z_{10-23}\rvert$	–	200	–	Ω
Ratio of internal/external current when pin 10 is short-circuited		–	3	–	
Control voltage for peaking adjustment (pin 11)	V_{11-23}	–	2-4	–	V
Input impedance (pin 11)	$\lvert Z_{11-23}$	–	10	–	kΩ
Chrominance amplifier (pin 3)					
Input voltage (note 2) (peak-to-peak value)	$V_{3-23(p-p)}$	55	550	1100	mV
Input impedance	$\lvert Z_{3-23}\rvert$	–	8	–	kΩ
Input capacitance	C_{3-23}	–	4	6	pF
A.C.C. control range		30	–	–	dB
Change of the burst signal at the output over the whole control range		–	–	1	dB
Gain at nominal contrast/saturation pin 3 to pin 24 (note 3)		13	–	–	dB
Output voltage (note 3) (peak-to-peak value) at a burst signal of 300 $mV_{(p-p)}$	$V_{24-23(p-p)}$	–	240	–	mV
Maximum output voltage range (pin 24) (peak-to-peak value)	$V_{24-23(p-p)}$	–	1-7	–	V
Distortion of chrominance amplifier at $V_{24-23(p-p)} = 0,5$ V (output) up to $V_{3-23(p-p)} = 1$ V (input)	d	–	3,0	5	%

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CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance amplifier (continued)					
Frequency response between 0 and 5 MHz	$\alpha_{24\text{-}3}$	–	–	–2	dB
Saturation control range (see Fig. 3)		50	–	–	dB
Input current saturation control (pin 6)	I_6	–	–	20	μA
Tracking between luminance and chrominance contrast control		–	–	2	dB
Cross-coupling between luminance and chrominance amplifier (note 4)		–	–	–46	dB
Signal-to-noise ratio at nominal input signal (note 5)	S/N	56	–	–	dB
Phase shift between burst and chrominance at nominal contrast/saturation	$\Delta\phi$	–	–	± 5	deg
Output impedance of chrominance amplifier	$\lvert Z_{24\text{-}23}\rvert$	–	25	–	Ω
Output current	I_{24}	–	–	10	mA
Reference part					
Phase-locked loop					
Catching range (note 6)	Δf	500	700	–	Hz
Phase shift for ± 400 Hz deviation of f_{osc} (note 6)	$\Delta\phi$	–	–	5	deg
Oscillator					
Temperature coefficient of oscillator frequency (note 6)	TC_{osc}	–	–1,5	–	Hz/K
Frequency variation when supply voltage increases from 10 to 13,2 V (note 6)	Δf_{osc}	–	40	–	Hz
Input resistance (pin 22)	$R_{22\text{-}23}$	–	300	–	Ω
Input capacitance (pin 22)	$C_{22\text{-}23}$	–	–	10	pF
A.C.C. generation (pin 2)					
Control voltage at nominal input signal	$V_{2\text{-}23}$	–	5,3	–	V
Control voltage without chrominance input	$V_{2\text{-}23}$	–	2,8	–	V
Colour-off voltage	$V_{2\text{-}23}$	–	3,4	–	V
Colour-on voltage	$V_{2\text{-}23}$	–	3,6	–	V
Change in burst amplitude with supply voltage		independent			
Voltage at pin 4 at nominal input signal	$V_{4\text{-}23}$	–	5,2	–	V
Hue control					
Control range		± 50	–	–	deg
Control voltage range		see Fig. 5			V

parameter	symbol	min.	typ.	max.	unit
Demodulator part					
Input burst signal amplitude (pin 17) (peak-to-peak value)	$V_{17\text{-}23(p\text{-}p)}$	–	320	–	mV
Input impedance (pin 17; note 7)	$\lvert Z_{17\text{-}23}\rvert$	–	2	–	kΩ
Ratio of demodulated signals (B-Y)/(R-Y)	$\frac{V_{15\text{-}23}}{V_{13\text{-}23}}$	–	1,1	–	
(G-Y)/(R-Y); no (B-Y) signal	$\frac{V_{14\text{-}23}}{V_{13\text{-}23}}$	–	0,26	–	
(G-Y)/(B-Y); no (R-Y) signal	$\frac{V_{14\text{-}23}}{V_{15\text{-}23}}$	–	0,22	–	
Frequency response between 0 and 1 MHz		–	–	–3	dB
Cross-talk between colour difference signals		40	–	–	dB
Control range reference signal (R-Y) demodulator (pin 18; note 8)	ϕ	see Fig. 6			deg
RGB matrix and amplifiers					
Output voltage (peak-to-peak value) at nominal input signal (black-to-white) (note 3)	$V_{13,14,15\text{-}23(p\text{-}p)}$	–	5	–	V
Output voltage at pin 13 (peak-to-peak value) at nominal contrast/saturation and no luminance signal to (R-Y)	$V_{13\text{-}23(p\text{-}p)}$	–	5,25	–	V
Maximum peak-white level (note 9)	$V_{13,14,15\text{-}23}$	9,0	9,3	9,6	V
Maximum output current (pins 13, 14, 15)	$I_{13,14,15}$	–	–	10	mA
Output black level voltage for a brightness control voltage at pin 12 of 2 V	$V_{13,14,15\text{-}23}$	–	2,7	–	V
Black level shift with vision contents		–	–	40	mV
Brightness control voltage range		see Fig. 4			V
Brightness control input current	I_{12}	–	–	5	μA
Variation of black level with temperature	$\Delta V/\Delta T$	–	0,35	1,0	mV/K
with contrast	ΔV	–	10	100	mV
Relative spread between the R, G and B output signals		–	–	10	%
Relative black-level variation between the three channels during variation of contrast, brightness and supply voltage		–	0	20	mV
Differential black-level drift over a temperature range of 40 °C		–	0	20	mV
Blanking level at the RGB outputs		1,9	2,1	2,3	V
Difference in blanking level of the three channels		–	0	–	mV

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
RGB matrix and amplifiers (continued)					
Differential drift of the blanking levels over a temperature range of 40 °C		–	0	–	mA
Tracking of output black level with supply voltage	$\frac{\Delta V_{b1}}{V_{b1}} \times \frac{V_P}{\Delta V_P}$	–	1,1	–	
Signal-to-noise ratio of output signals (note 5)	S/N	62	–	–	dB
Residual 7,1 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value)		–	75	150	mV
Output impedance of RGB outputs	$\lvert Z_{13,14,15-23} \rvert$	–	50	–	Ω
Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz		–	–	–3	dB
Sandcastle input (pin 8)					
Level at which the RGB blanking is activated	V_{8-23}	1	1,5	2	V
Level at which burst gating and clamping pulse are separated	V_{8-23}	6,5	7,0	7,5	V
Delay between black level clamping and burst gating pulse	t_d	–	0,4	–	μs
Input current					
at V_{8-23} = 0 to 1 V	$-I_8$	–	–	1	mA
at V_{8-23} = 1 to 8,5 V	I_8	–	20	–	μA
at V_{8-23} = 8,5 to 12 V	I_8	–	–	2	mA

Notes to the characteristics

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast –3 dB and nominal saturation as the maximum saturation –6 dB.
4. Cross coupling is measured under the following conditions:
   - Input signals nominal
   - Contrast and saturation such that nominal output signals are obtained
   - The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to r.m.s. noise.
6. All frequency variations are referred to 3,58 MHz carrier frequency.
7. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
8. When pin 18 is open circuit the phase shift between the (R-Y) and (B-Y) reference carrier is 115°. This phase shift can be varied by changing the voltage applied to pin 18.
9. If the typical voltage for this white level is exceeded, the output voltage is reduced by discharging the capacitor at pin 7 (contrast control); discharge current is 1,5 mA.

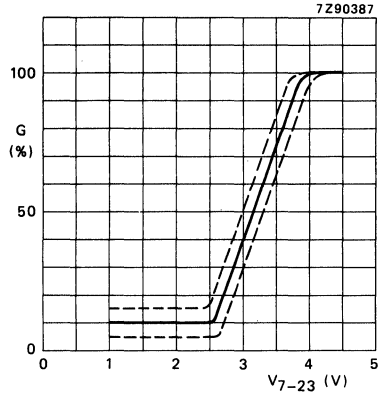


Fig. 2 Contrast control voltage range.

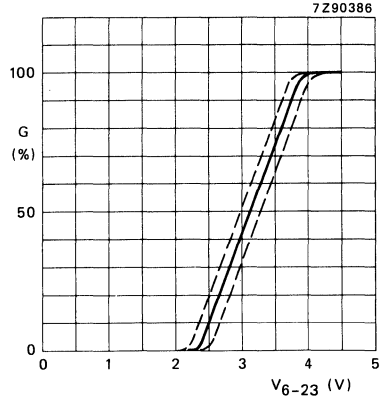


Fig. 3 Saturation control voltage range.

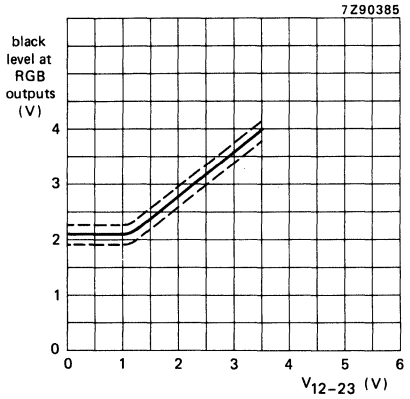


Fig. 4 Brightness control voltage range.

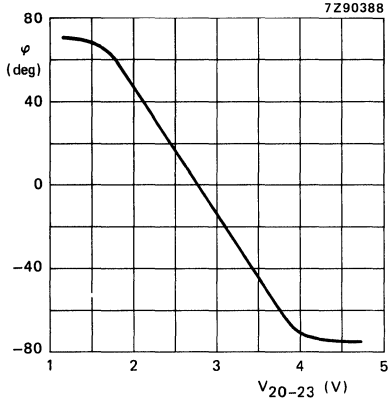


Fig. 5 Hue control voltage range.

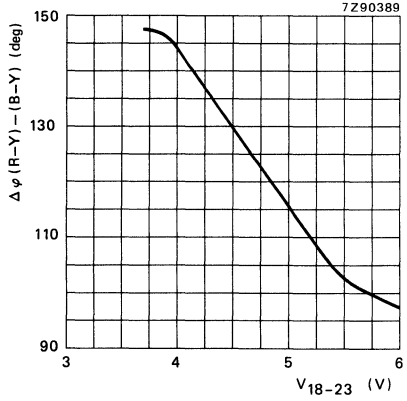


Fig. 6 Phase shift between (R-Y) and (B-Y) as a function of V_{18-23}.

Monolithic Integrated Delay Line and Filter Combination for NTSC Television Receivers

TDA3568

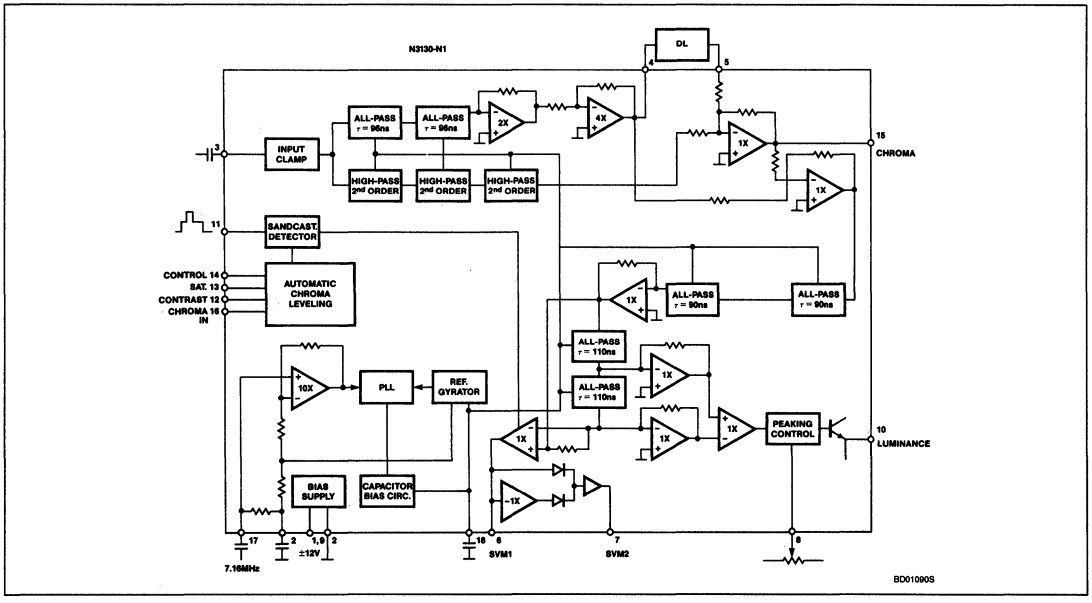
DESCRIPTION

Monolithic integrated delay line and filter combination for NTSC television receivers. It is intended to be used in combination with the NTSC-decoder TDA3563.

FEATURES

- **Combination filter interface for glass delay line**
- **Luminance delay line**
- **Peaking circuit for the luminance signal**
- **Differentiated luminance signal outputs which can be used for driving Scan Velocity Modulation circuits**
- **Automatic chroma leveling circuit to avoid heavy oversaturated pictures for non-standard signals**
- **Tuning circuit which compensates for spreads of gyrator cells which are used in the various functions.**

BLOCK DIAGRAM



Multistandard Decoder | TDA4555/56

GENERAL DESCRIPTION

The TDA4555 and TDA4556 are monolithic integrated multistandard colour decoders for the PAL, SECAM, NTSC 3,58 MHz and NTSC 4,43 MHz standards. The difference between the TDA4555 and the TDA4556 is the polarity of the colour difference output signals (B-Y) and (R-Y).

Features

Chrominance part

- Gain controlled chrominance amplifier for PAL, SECAM and NTSC
- ACC rectifier circuits (PAL/NTSC, SECAM)
- Burst blanking (PAL) in front of 64 μs glass delay line
- Chrominance output stage for driving the 64 μs glass delay line (PAL, SECAM)
- Limiter stages for direct and delayed SECAM signal
- SECAM permutator

Demodulator part

- Flyback blanking incorporated in the two synchronous demodulators (PAL, NTSC)
- PAL switch
- Internal PAL matrix
- Two quadrature demodulators with external reference tuned circuits (SECAM)
- Internal filtering of residual carrier
- De-emphasis (SECAM)
- Insertion of reference voltages as achromatic value (SECAM) in the (B-Y) and (R-Y) colour difference output stages (blanking)

Identification part

- Automatic standard recognition by sequential inquiry
- Delay for colour-on and scanning-on
- Reliable SECAM identification by PAL priority circuit
- Forced switch-on of a standard
- Four switching voltages for chrominance filters, traps and crystals
- Two identification circuits for PAL/SECAM (H/2) and NTSC
- PAL/SECAM flip-flop
- SECAM identification mode switch (horizontal, vertical or combined horizontal and vertical)
- Crystal oscillator with divider stages and PLL circuitry (PAL, NTSC) for double colour subcarrier frequency
- HUE control (NTSC)
- Service switch

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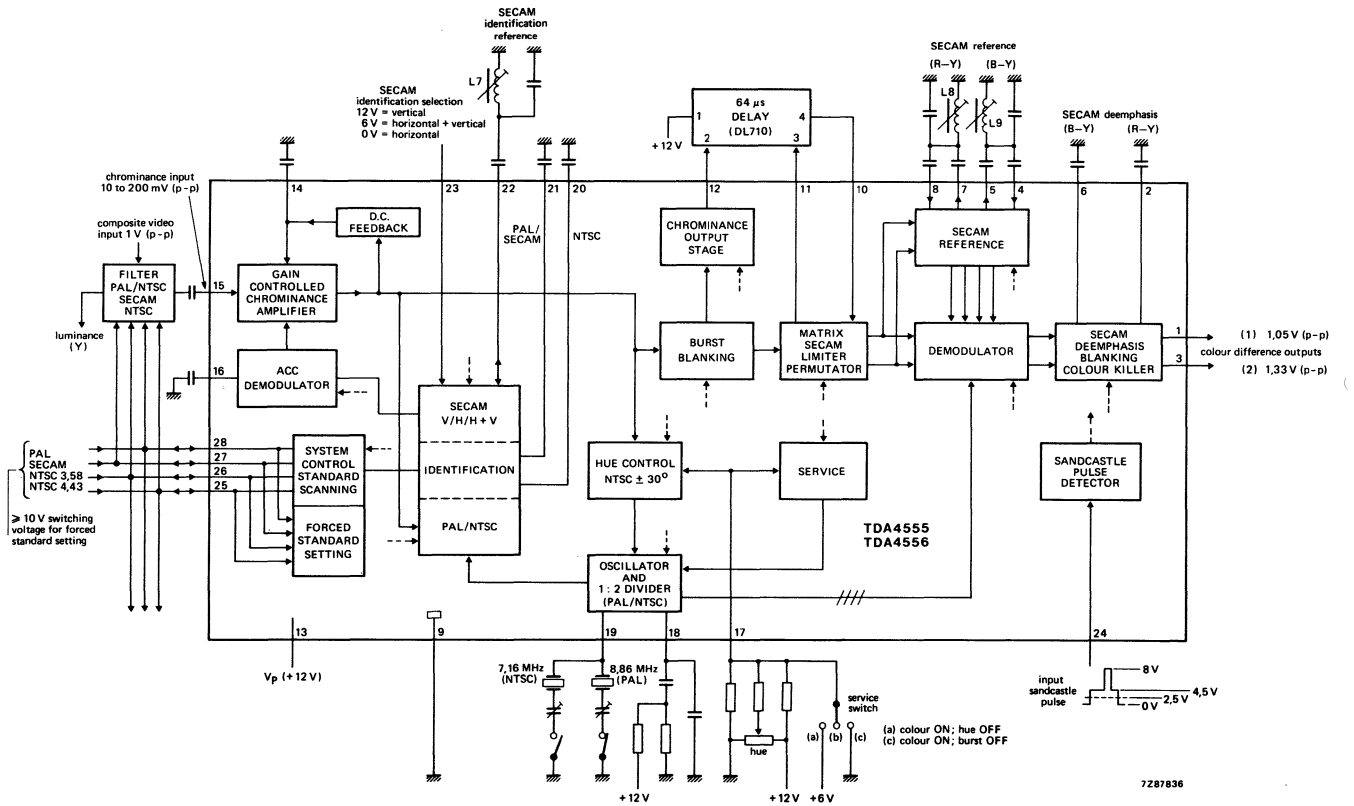
QUICK REFERENCE DATA

Supply voltage (pin 13)	$V_P = V_{13-9}$	typ.	12 V
Supply current (pin 13)	$I_P = I_{13}$	typ.	65 mA
Chrominance input signal (peak-to-peak)	$V_{15-9(p-p)}$		20 to 200 mV
Chrominance output signal (peak-to-peak)	$V_{12-9(p-p)}$	typ.	1,6 V
Colour difference output signals (peak-to-peak values)			
TDA4555: –(R-Y); **TDA4556:** + (R-Y)	$V_{1-9(p-p)}$	typ.	1,05 V ± 2 dB
TDA4555: –(B-Y); **TDA4556:** + (B-Y)	$V_{3-9(p-p)}$	typ.	1,33 V ± 2 dB
Sandcastle pulse; required amplitude for			
vertical and horizontal pulse separation	V_{24-9}	typ.	2,5 V
horizontal pulse separation	V_{24-9}	typ.	4,5 V
burst gating	V_{24-9}	typ.	7,7 V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).



(1) TDA4555: –(R-Y); TDA4556: + (R-Y)
(2) TDA4555: –(B-Y); TDA4556: + (B-Y)

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13-9}$	max.	13,2	V
Voltage range at pins 10, 11, 17, 23, 24, 25, 26, 27, 28 to pin 9 (ground)	V_{n-9}		0 to V_P	V
Current at pin 12	I_{12}	max.	8	mA
Peak value	I_{12M}	max.	15	mA
Total power dissipation	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}		−25 to +150	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

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CHARACTERISTICS

$V_P = V_{13-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 13)					
Supply voltage range	$V_P = V_{13-9}$	10,8	–	13,2	V
Supply current	$I_P = I_{13}$	–	65	–	mA
Chrominance part					
Chrominance input signal (pin 15)					
input voltage with 75% colour bar signal (peak-to-peak value)	$V_{15-9(p-p)}$	20	100	200	mV
input impedance	$\lvert Z_{15-9}\rvert$	2,3	3,3	–	kΩ
Chrominance output signal (pin 12)					
output voltage (peak-to-peak value)	$V_{12-9(p-p)}$	–	1,6	–	V
output impedance (n-p-n emitter follower)	$\lvert Z_{12-9}\rvert$	–	–	20	Ω
d.c. output voltage	V_{12-9}	–	8,2	–	V
Input for delayed signal (pin 10)					
d.c. input current	I_{10}	–	–	10	μA
input resistance	R_{10-9}	10	–	–	kΩ
Demodulator part (PAL/NTSC)					
Colour difference output signals					
output voltage (proportional to V_{13-9}) (peak-to-peak value)					
TDA4555					
– (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05 V ± 2 dB	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33 V ± 2 dB	–	V
TDA4556					
+ (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05 V ± 2 dB	–	V
+ (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33 V ± 2 dB	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0,79 ± 10%	–	
Residual carrier (subcarrier frequency) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	–	30	mV
Residual carrier (PAL only) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	10	–	mV
H/2 ripple at (R-Y) output (pin 1) (peak-to-peak value) without input signal	$V_{1-9(p-p)}$	–	–	10	mV
D.C. output voltage n-p-n emitter follower with internal current source of 0,3 mA	$V_{1,3-9}$	–	7,7	–	V
output impedance	$\lvert Z_{1,3-9}\rvert$	–	–	150	Ω

parameter	symbol	min.	typ.	max.	unit
Demodulator part (SECAM)					
Colour difference signals (see note 1) output voltage (proportional to V_{13-9}) (peak-to-peak value) TDA4555					
–(R-Y) signal (pin 1	$V_{1-9(p-p)}$	–	1,05	–	V
– (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
TDA4556					
+ (R-Y) signal (pin 1)	$V_{1-9(p-p)}$	–	1,05	–	V
+ (B-Y) signal (pin 3)	$V_{3-9(p-p)}$	–	1,33	–	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1/3-9}$	–	0,79* ± 10%	–	
Residual carrier (4 to 5 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	20	30	mV
Residual carrier (8 to 10 MHz) (peak-to-peak value)	$V_{1,3-9(p-p)}$	–	20	30	mV
H/2 ripple at (R-Y) (B-Y) outputs (pins 1 and 3) (peak-to-peak value) with f_o signals	$V_{1,3-9(p-p)}$	–	–	20	mV
D.C. output voltage	$V_{1,3-9}$	–	7,7	–	V
Shift of inserted levels relative to levels of demodulated f_o frequencies (IC only)	$\Delta V/\Delta T(R-Y)$	–	–0,55	–	mV/K
	$\Delta V/\Delta T(B-Y)$	–	+0,25	–	mV/K
HUE control (NTSC)/service switch					
Phase shift of reference carrier at V_{17-9} = 2 V	$-\phi$	–	30**	–	deg
at V_{17-9} = 3 V	ϕ	–	0	–	deg
at V_{17-9} = 4 V	$+\phi$	–	30**	–	deg
Input resistance	R_{17-9}	–	5	–	kΩ
Service position					
Switching voltage (pin 17) burst OFF; colour ON (for oscillator adjustment)	V_{17-9}	–	–	0,5	V
HUE control OFF; colour ON (for forced colour ON)	V_{17-9}	6	–	–	V
Crystal oscillator (pin 19)					
For double colour subcarrier frequency input resistance	R_{19-9}	–	350	–	Ω
lock-in-range referred to subcarrier frequency	Δf	± 400	–	–	Hz

* Value measured without influence of external circuitry.

** Relative to phase at V_{17-9} = 3 V.

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CHARACTERISTICS (continued)

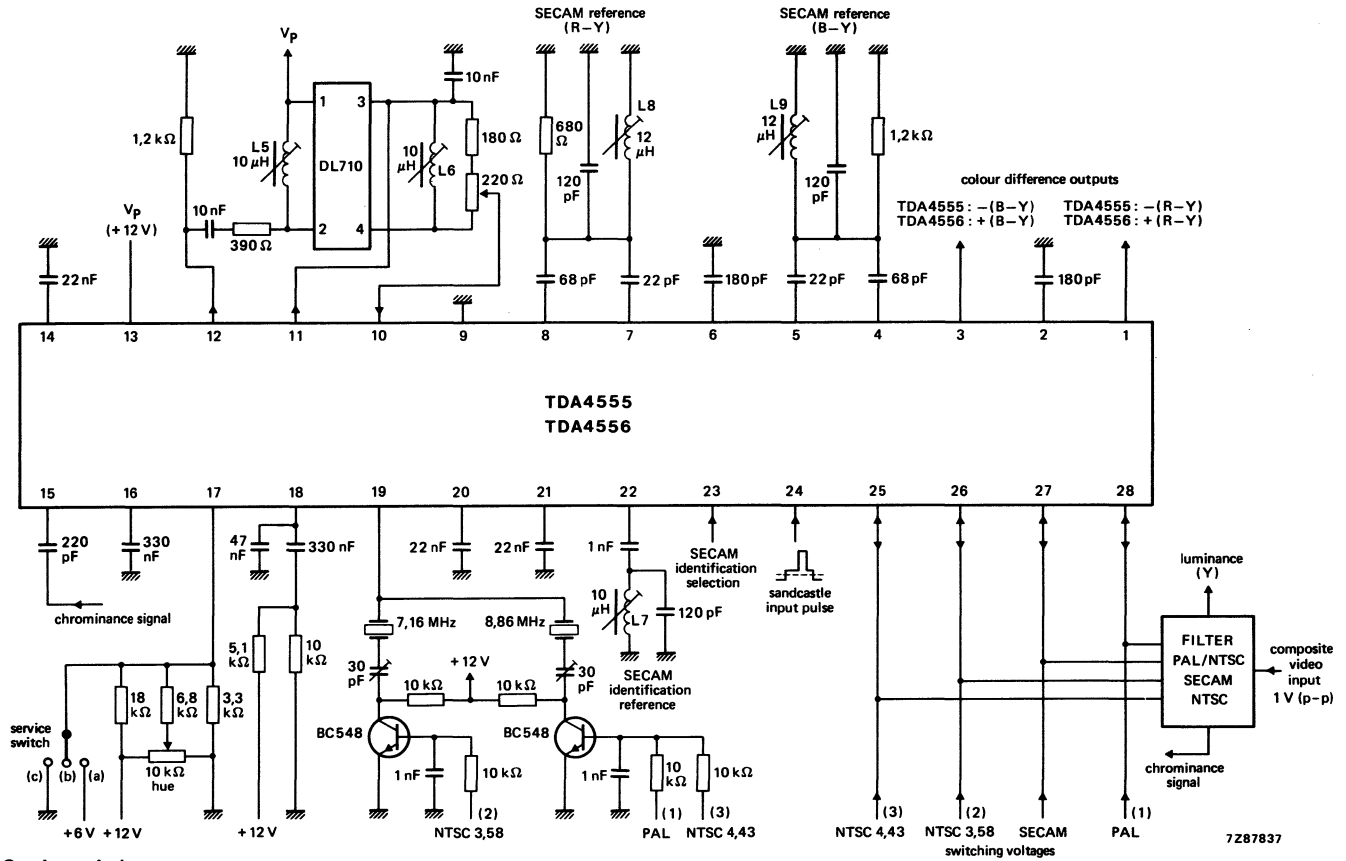
parameter	symbol	min.	typ.	max.	unit
Identification part					
Switching voltages for chrominance filters and crystals at pin 28 (PAL) at pin 27 (SECAM) at pin 26 (NTSC 3,58 MHz) at pin 25 (NTSC 4,43 MHz)					
Control voltage OFF state	$V_{25,26,27,28-9}$	–	–	0,5	V
Control voltage ON state during scanning; colour OFF	$V_{25,26,27,28-9}$	–	2,45	–	V
colour ON	$V_{25,26,27,28-9}$	–	5,8	–	V
Output current	$-I_{25,26,27,28-9}$	–	–	3	mA
Voltage for forced switching ON PAL	V_{28-9}	9	–	–	V
SECAM	V_{27-9}	9	–	–	V
NTSC 3,58 MHz	V_{26-9}	9	–	–	V
NTSC 4,43 MHz	V_{25-9}	9	–	–	V
Delay time for restart of scanning	t_{dS}	2 to 3 vertical periods			
colour ON	t_{dC1}	2 to 3 vertical periods			
colour OFF	t_{dC2}	0 to 1 vertical periods			
SECAM identification (pin 23)					
Input voltage for horizontal identification (H)	V_{23-9}	–	–	2	V
vertical identification (V)	V_{23-9}	10	–	–	V
combined (H) and (V) identification	V_{23-9}	–	6*	–	V
Sequence of standard inquiry PAL-SECAM-NTSC 3,58 MHz-NTSC 4,43 MHz					
Reliable SECAM identification by PAL priority circuit					
Scanning time for each standard	t_S	4 vertical periods			

parameter	symbol	min.	typ.	max.	unit
Sandcastle pulse detector (see note 2)					
Input voltage pulse levels (pin 24) to separate vertical and horizontal blanking pulses	V_{24-9}	1,2	–	2,0	V
required pulse amplitude	$V_{24-9(p-p)}$	2,0	–	3,0	V
to separate horizontal blanking pulse	V_{24-9}	3,2	–	4,0	V
required pulse amplitude	$V_{24-9(p-p)}$	4,0	–	5,0	V
to separate burst gating pulse	V_{24-9}	6,5	–	7,7	V
required pulse amplitude	$V_{24-9(p-p)}$	7,7	–	V_P	V
Input voltage during horizontal scanning	V_{24-9}	–	–	1,0	V
Input current	$-I_{24}$	–	–	100	μA

Notes to the characteristics

1. The signal amplitude of the colour difference signals (R-Y) and B-Y) is dependent on the characteristics of the external tuned circuits at pins 7, 8 and 4, 5 respectively. Adjustment of the amplitude is achieved by varying the Q-factor of these tuned circuits. The resonant frequency must be adjusted such that the demodulated output frequency (f_o) provides the same output level as the internally inserted reference voltage (achromatic value).
2. The sandcastle pulse is compared with three internal threshold levels, which are proportional to the supply voltage.

APPLICATION INFORMATION



Service switch

(a) colour ON; hue OFF
(c) colour ON; burst OFF

Fig. 2 Application diagram.

Color Transient Improvement Circuit TDA4560

GENERAL DESCRIPTION

The TDA4560 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 720 ns to 1035 ns in steps of 45 ns
- Output for the option of velocity modulation

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10\text{-}18}$	typ.	12	V
Supply current (pin 10)	$I_P = I_{10}$	typ.	35	mA
(R-Y) and (B-Y) attenuation	α_{cd}	typ.	0	dB
(R-Y) and (B-Y) output transient time	t_{tr}	typ.	150	ns
Adjustable Y-delay time	t_d	720 to	1035	ns
Y-attenuation	α_y	typ.	7	dB

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PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

Color Transient Improvement Circuit | TDA4560

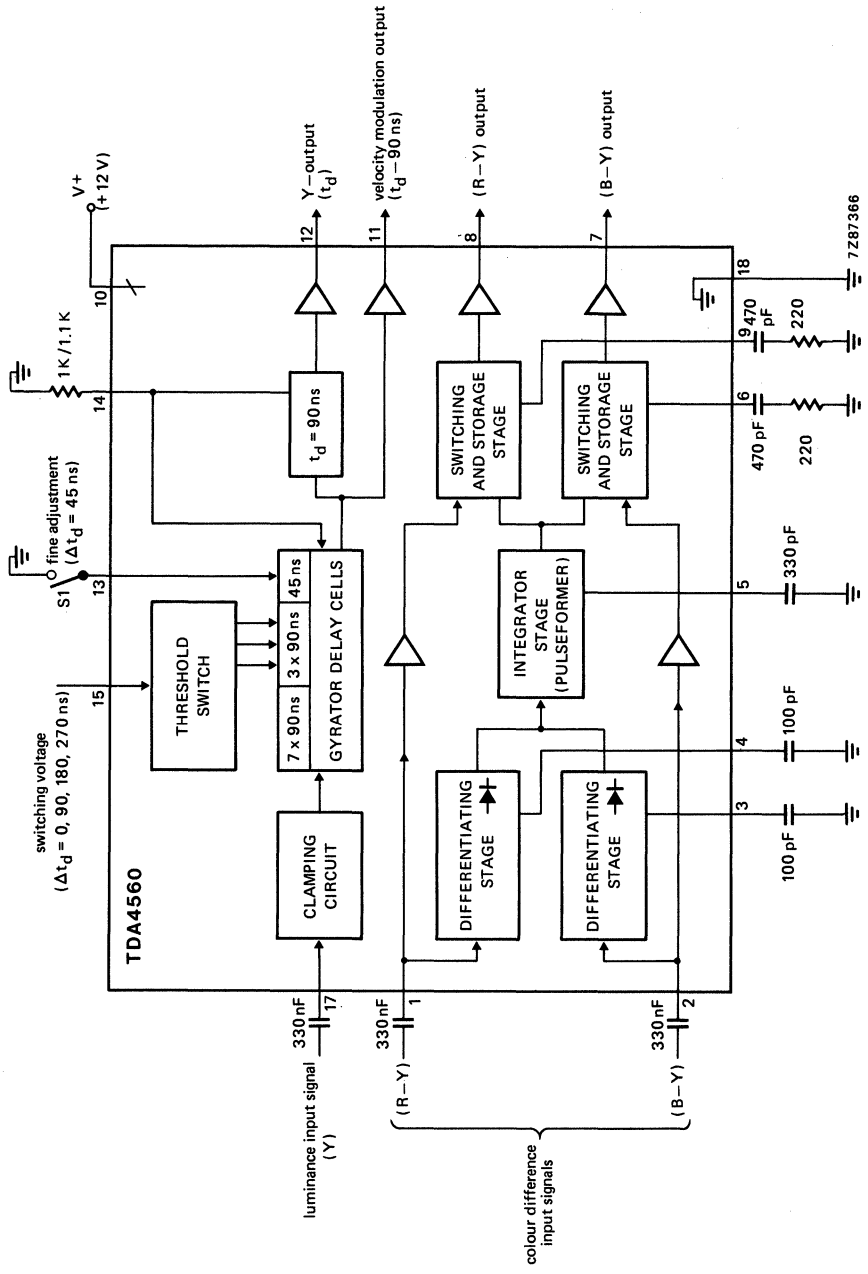

Fig. 1 Block diagram.

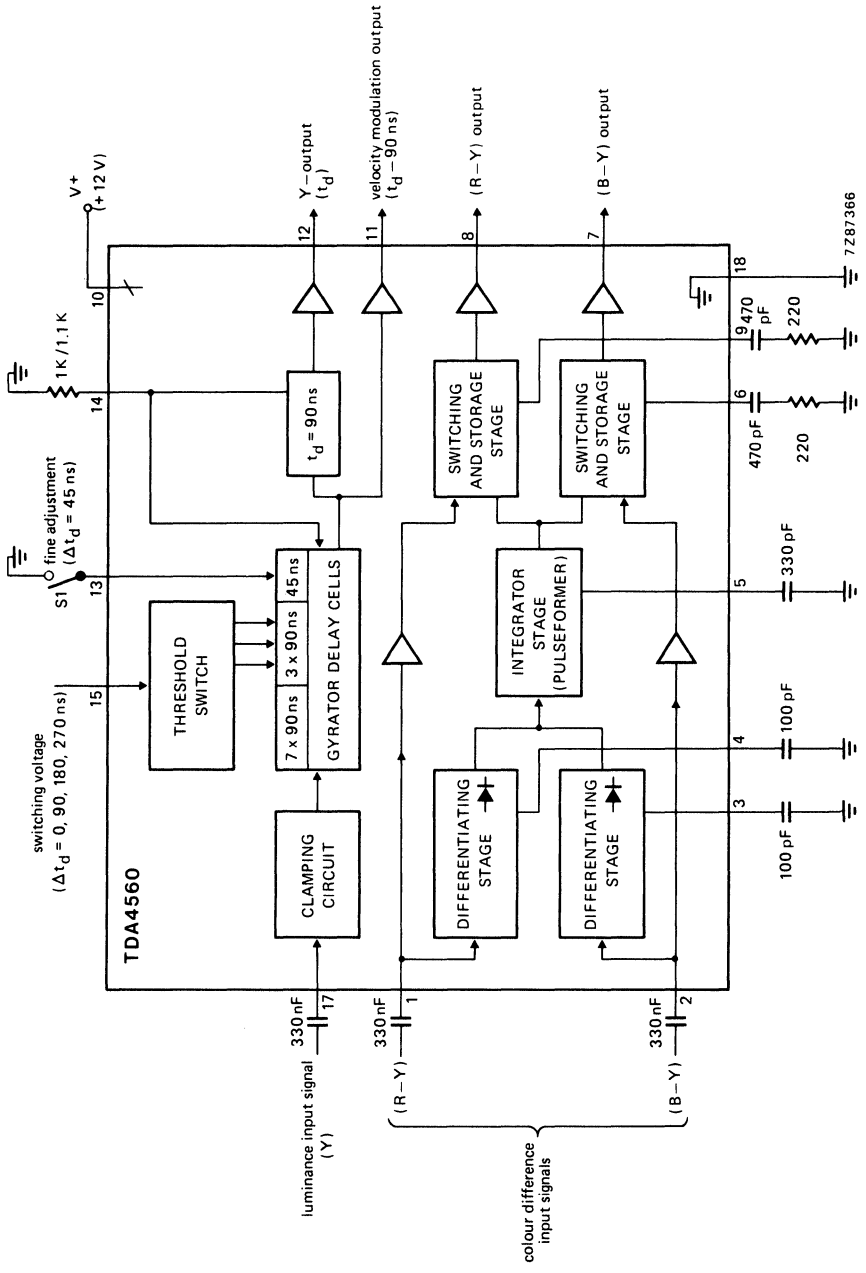

Fig. 1 Block diagram.

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FUNCTIONAL DESCRIPTION

The IC consists of two colour difference channels (B-Y) and (R-Y) and a luminance signal path (Y) as shown in Fig. 1.

Colour difference channels

The (B-Y) and (R-Y) colour difference channels consist of a buffer amplifier at the input, a switching stage and an output amplifier. The switching stages, which are controlled by transient detecting stages (differentiators), switch to a value that has been stored at the beginning of the transients. The differentiating stages get their signal direct from the colour difference detecting signal (pins 1 and 2). Two parallel storage stages are incorporated in which the colour difference signals are stored during the transient time of the signal. After a time of about 600 ns they are switched immediately (transient time of 150 ns) to the outputs. The colour difference channels are not attenuated.

Y-signal path

The Y-signal input (pin 17) is capacitively coupled to an input clamping circuit. Gyrator delay cells provide a maximum delay of 1035 ns including an additional delay of 45 ns via the fine adjustment switch (S1) at pin 13. Three delay cells are switched with two interstage switches dependent on the voltage at pin 15. Thus three switchable delay times of 90 ns, 180 ns or 270 ns less than the maximum delay time are available. A tuning compensation circuit ensures accuracy of delay time despite process tolerances. The Y-signal path has a 7 dB attenuation as a normal Y-delay coil and can replace this completely. The output is fed to pin 12 via a buffer amplifier. An additional output stage provides a signal of 90 ns less delay at pin 11 for the option of velocity modulation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 10)	$V_P = V_{10\text{-}18}$	max.	13.2	V
Voltage ranges to pin 18 (ground)				
at pins 1, 2, 12, 15	$V_{n\text{-}18}$	0 to	V_P	V
at pin 11	$V_{11\text{-}18}$	0 to	$V_P - 3$	V
at pin 17	$V_{17\text{-}18}$	0 to	7	V
Voltages ranges				
at pin 7 to pin 6	$V_{7\text{-}6}$	0 to	5	V
at pin 8 to pin 9	$V_{8\text{-}9}$	0 to	5	V
Currents				
at pins 6, 9	$\pm I_{6,9}$	max.	15	mA
Total power dissipation	P_{tot}	max.	1.1	W
Storage temperature range	T_{stg}	−25 to +	150	°C
Operating ambient temperature range	T_{amb}	0 to +	70	°C

Note

Pins 3, 4, 5, 6, 9, 13 and 14 d.c. potential not published.

CHARACTERISTICS

$V_P = V_{10-18} = 12$ V; $T_{amb} = 25$ °C; measured in application circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 10)					
Supply voltage	$V_P = V_{10-18}$	–	12	13.2	V
Supply current	$I_P = I_{10}$	–	35	–	mA
Colour difference channels (pins 1 and 2)					
(R-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{1-18}	–	1.05	–	V
(B-Y) input voltage (peak-to-peak value) 75% colour bar signal	V_{2-18}	–	1.33	–	V
Input resistance	$R_{1,\,2-18}$	–	12	–	kΩ
(B-Y), (R-Y) signal attenuation $\frac{V_8}{V_1}, \frac{V_7}{V_2}$	α_{cd}	–	0	–	dB
Output current (emitter follower with constant current source 0.5 mA)	$-I_{7,\,8}$	–	1.2	–	mA
(R-Y) and (B-Y) output signal transient time	t_{tr}	–	150	–	ns
Y-signal path (pin 17)					
Y-input voltage (composite signal) (peak-to-peak value)	$V_{17-18(p-p)}$	–	1	–	V
Input resistance	R_{17-18}	–	20	–	kΩ
Internal bias voltage	V_{17-18}	–	2.3	–	V
Input current during picture content	I_{17}	–	8	–	μA
during synchronizing pulse	$-I_{17}$	–	100	–	μA
Y-signal attenuation $\frac{V_{11}}{V_{17}}, \frac{V_{12}}{V_{17}}$	α_y	–	7	–	dB
Output current (emitter follower with constant current source 0.4 mA)	$-I_{11,\,12}$	–	1.2	–	mA
Frequency response ($V_{15-18} = 0$ V) at $R_{14-18} = 1$ kΩ	f_{12-17}	–	6	–	MHz
at $R_{14-18} = 1.1$ kΩ	f_{12-17}	–	4.5	–	MHz

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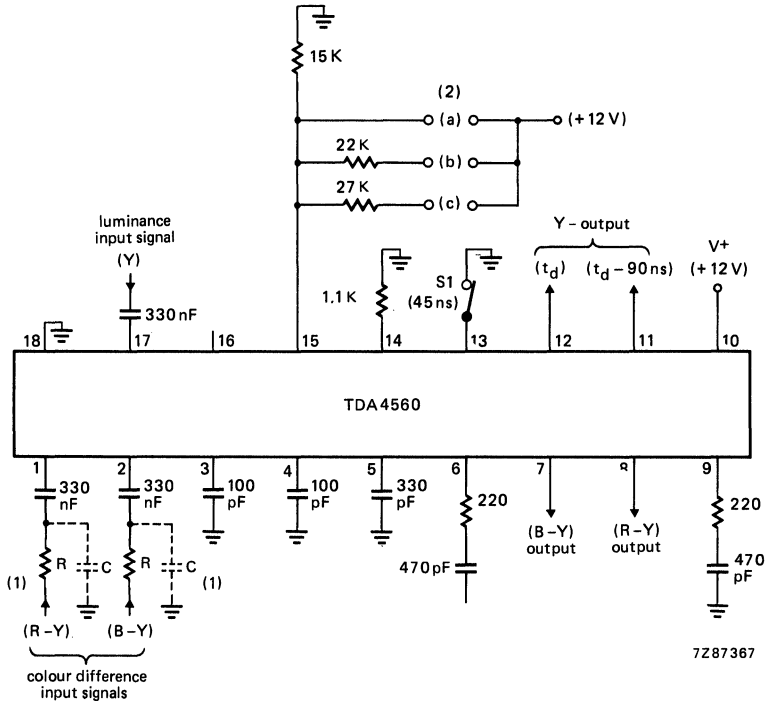
parameter	symbol	min.	typ.	max.	unit
Y-signal path (pin 17) (continued)					
Adjustable delay (switch S1 open)					
at V_{15-18} = 0 to 2.5 V; R_{14-18} = 1 kΩ	t_d	–	640	–	ns
at V_{15-18} = 0 to 2.5 V; R_{14-18} = 1.1 kΩ	t_d	–	720	–	ns
at V_{15-18} = 3.5 to 5.5 V; R_{14-18} = 1 kΩ	t_d	–	720	–	ns
at V_{15-18} = 3.5 to 5.5 V; R_{14-18} = 1.1 kΩ	t_d	–	810	–	ns
at V_{15-18} = 6.5 to 8.5 V; R_{14-18} = 1 kΩ	t_d	–	800	–	ns
at V_{15-18} = 6.5 to 8.5 V; R_{14-18} = 1.1 kΩ	t_d	–	900	–	ns
at V_{15-18} = 9.5 to 12 V; R_{14-18} = 1 kΩ	t_d	–	880	–	ns
at V_{15-18} = 9.5 to 12 V; R_{14-18} = 1.1 kΩ	t_d	–	990	–	ns
Fine adjustment delay (switch S1 closed)					
at V_{13-18} = 0 V	Δt_d	–	45	–	ns
Signal delay for velocity modulation (pin 11)					
with R_{14-18} = 1 kΩ	t		t_d – 80 ns		
with R_{14-18} = 1.1 kΩ	t		t_d – 90 ns		
Thermal resistance					
From junction to ambient (in free air)	$R_{th\ j-a}$	–	–	70	K/W

APPLICATION INFORMATION



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.

Fig. 2 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

connection			voltage at pin 15	delay time (ns)*
(a)	(b)	(c)		
X	X	X	0 to 2.5 V	720
X	X	O	3.5 to 5.5 V	810
X	O	O	6.5 to 8.5 V	900
O	O	O	9.5 to 12 V	990

Where: X = connection closed; O = connection open.

* When switch (S1) is closed the delay time is increased by 45 ns.

Video Control with Two RGB and Color Difference Inputs — TDA4580

DESCRIPTION

The TDA4580 is a monolithic integrated video control circuit with automatic cut-off stabilization for TV-receivers with color difference interface, e.g. in connection with the multistandard decoder TDA4555 linear RGB-signals can be inserted from two different external sources.

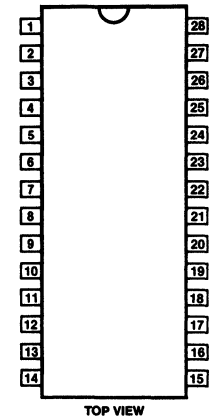
FEATURES

- **Clamped input stage for capacitive coupled R-, G- and B-signals followed by a high precision matrix to obtain the luminance- and color-difference-signals**
- **Fast switch 1 for Y-, CD, R-, G-, B-signals**
- **Switch for NTSC-matrix and vertical blanking time**
- **Fast switch 2 for insertion of Teletext-signals**
- **Emitter-follower outputs for driving the RGB output signals**

APPLICATIONS

- **Video monitors**
- **Graphics**
- **Color printers**
- **TV receivers**

PIN CONFIGURATION



TOP VIEW

CD01330S

PIN	FUNCTION
1	R- output
2	Storage capacity for cutoff central
3	G- output
4	Storage capacity for cutoff central
5	B- output
6	Supply V_{CC}
7	Storage capacity for cutoff central
8	NTSC- matrix and blanking time switch
9	Peak drive listing
10	Sandcastle- input
11	Signal switch for RGB inputs
12	B- input (ext. signal)
13	G- input (ext. signal)
14	R- input (ext. signal)
15	Y- input
16	Saturation control
17	(R - Y-)- input
18	(B - Y-)- input
19	Contrast control
20	Brightness control
21	TxT — B input
22	TxT — G input
23	TxT — R input
24	Ground
25	Average beam current listing
26	Beam info (cutoff central)
27	Storage capacity for leakage current information
28	Signal switch for TxT inputs

ORDERING CODE

	PINS	PACKAGE	NOTE
TDA4580	28	Plastic DIP	SOT117

REFERENCE DATA

PARAMETER	LIMITS			UNIT
	Min	Typ	Max	
Supply voltage range	10.8		13.2	V
Supply current, I_6		110		mA
Color difference inputs (pin 17, 18)				
(B – Y) input signal at pin 18 (peak to peak value), V_{18-24}		1.33		V
(R – Y) input signal at pin 17 (peak to peak value), V_{17-24}		1.05		V
Luminance input (pin 15)				
Composite video input signal (peak to peak value), V_{15-24}		0.45		V
R, G, B inputs (pin 12, 13, 14)				
R, G, B signals controlled by saturation, contrast and brightness Input signal (peak to peak value), $V_{12, 13, 14-24}$		0.7		V
TXT-inputs (pin 21, 22, 23)				
RGB inputs for teletext use. The signals are only controlled by the brightness control. Input signal for 100% output signals (peak to peak value), $V_{21, 22, 24-24}$		1.0		V
Outputs for positive RGB signals				
Emitter followers with current sources and emitter protection resistors Minimum output voltage, $V_{1, 3, 5-24}$		1.0		V

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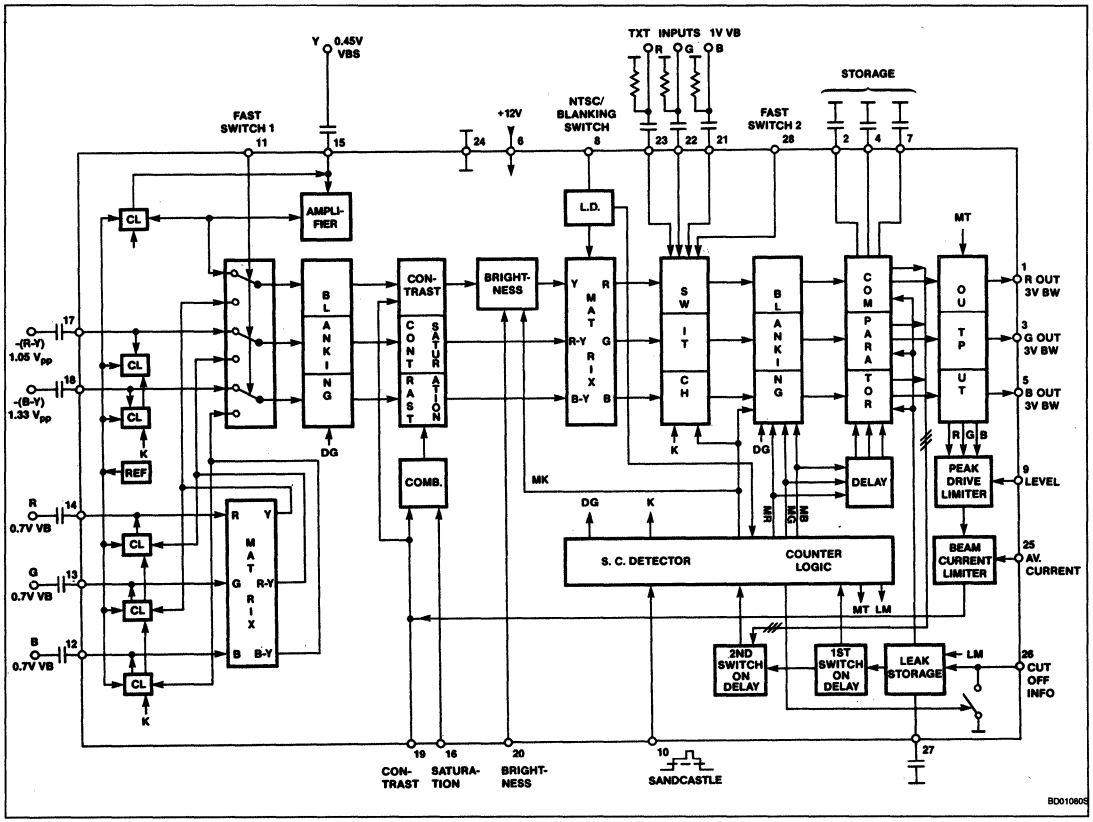
Video Control with Two RGB and Color Difference Inputs TDA4580

BLOCK DIAGRAM



For additional information, consult the Applications Section.

RGB to NTSC/PAL Encoder — TEA2000

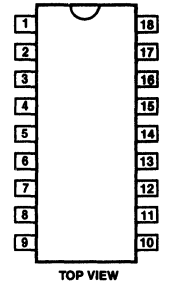
DESCRIPTION

The TEA2000 encodes color information and provides composite video output for driving a VHF or UHF modulator.

FEATURES

- **An internal oscillator from which the (R-Y) and (B-Y) waveforms are generated**
- **Accepts timing signals (composite sync, composite blanking)**
- **A 6-bit binary coded input giving color information**
- **Resulting output is a 64 color composite video signal (including black and white).**
- **Burst timing and PAL-switch-function is internally generated.**

PIN CONFIGURATION



TOP VIEW

CD01400S

PIN	FUNCTION
1	Red 1 binary input
2	Green 0 binary input
3	Green 1 binary input
4	Blue 0 binary input
5	Blue 1 binary input
6	Composite video output
7	Luminance output to delay line
8	Luminance input from delay line
9	Ground 0 volt
10	Chroma band limiting
11	Supply voltage
12	7.16MHz crystal for NTSC
13	8.86MHz crystal for PAL
14	PAL/$\overline{\text{NTSC}}$ switch
15	Ramp
16	Composite sync input ($\overline{\text{CSYNC}}$)
17	Composite blanking input (CBLNK)
18	Red 0 binary input

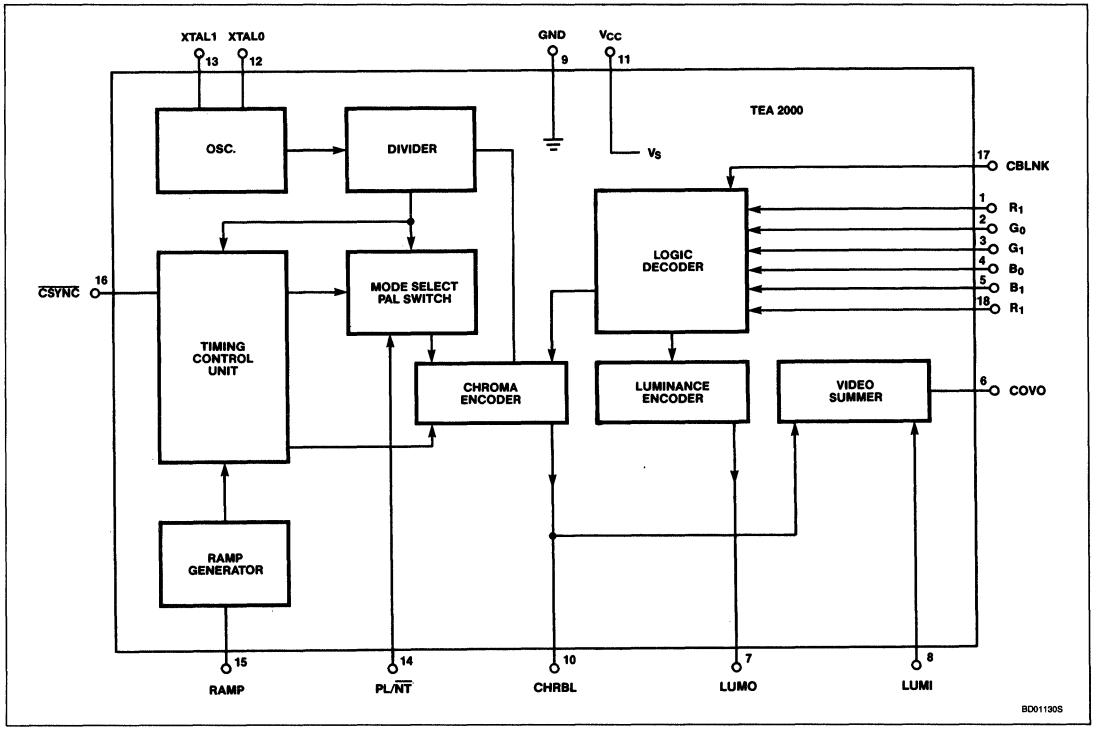
8

RGB to NTSC/PAL Encoder — TEA2000

REFERENCE DATA

PARAMETER	SYMBOL	LIMITS			UNIT
		Min	Typ	Max	
Supply voltage, V_{11-9}			12		V
Supply current at $V_{11-9} = 12V$, I_{11}			55		mA
Input voltage (pins 1, 2, 3, 4, 5, 14, 16, 17, 18)	V_{IL} V_{IH}	 2.0		0.8	V V
Composite video output (peak-to-peak), V_6			2		V

BLOCK DIAGRAM



Vertical Deflection TDA2653A

The TDA2653A is a monolithic integrated circuit for vertical deflection in large screen colour television receivers, e.g. 30AX and PIL-S4 systems.

The circuit incorporates the following functions:

- Oscillator; switch capability for 50 Hz/60 Hz operation.
- Synchronization circuit.
- Blanking pulse generator with guard circuit.
- Sawtooth generator with buffer stage.
- Preamplifier with fed-out inputs.
- Output stage with thermal and short-circuit protection.
- Flyback generator.
- Voltage stabilizer.

QUICK REFERENCE DATA

For 30AX system				
Supply voltage (pin 9)	$V_{9-8} = V_S$	typ.	26	V
Supply current (pin 5 + pin 9)	$I_5 + I_9 = I_S$	typ.	325	mA
Output current (peak-to-peak value)	$I_{6(p-p)}$	typ.	2.2	A
Picture frequency	f		50 Hz/60	Hz
Sync input pulse (peak-to-peak value)	$V_{2-8(p-p)}$	$\geqslant$	1	V
Thermal resistance from junction to mounting base	$R_{th\ j-mb}$	$\leqslant$	5	K/W

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PACKAGE OUTLINE

13-lead DIL; plastic power (SOT-141B).

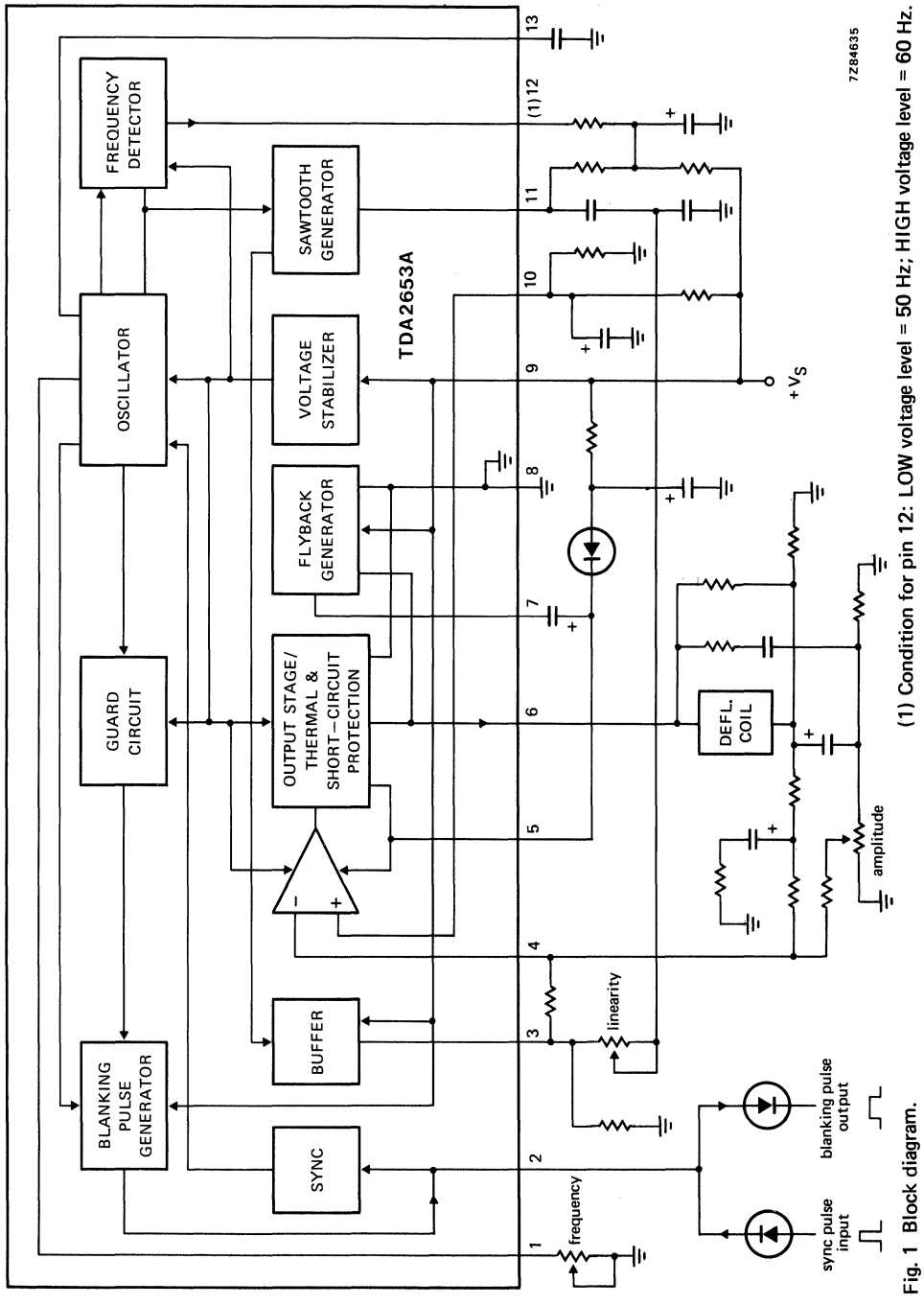

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	$V_{9-8} = V_S$	max.	40 V
Supply voltage output stage (pin 5)	V_{5-8}	max.	58 V
Voltages			
Pin 3	V_{3-11}	max.	7 V
Pin 13	V_{13-8}	max.	7 V
Pins 4 and 10	$V_{4;10-8}$	max.	24 V
Pin 6	V_{6-8}	max.	58 V
	$-V_{6-8}$	max.	0 V
Pins 7 and 11	$V_{7;11-8}$	max.	40 V
Currents			
Pin 1	I_1	max.	0 mA
	$-I_1$	max.	1 mA
Pin 2	$\pm I_2$	max.	10 mA
Pin 3	I_3	max.	0 mA
	$-I_3$	max.	5 mA
Pin 7	I_7	max.	1.2 A
	$-I_7$	max.	1.5 A
Pin 11	I_{11}	max.	50 mA
	$-I_{11}$	max.	1 mA
Pin 12	I_{12}	max.	3 mA
	$-I_{12}$	max.	0 mA

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

Storage temperature range	T_{stg}	−25 to + 150 °C
Operating ambient temperature range	T_{amb}	−20 °C to limiting value

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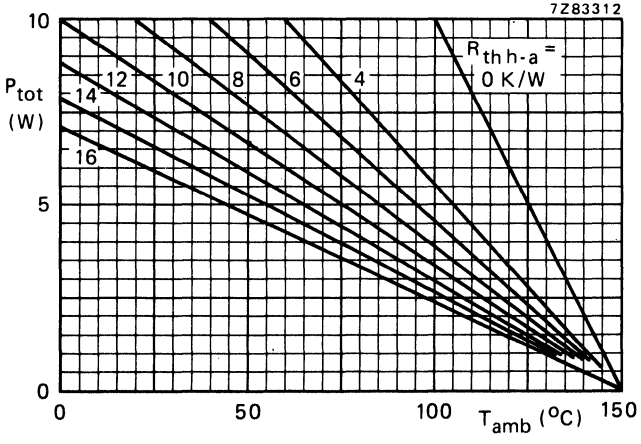


Fig. 2 Total power dissipation. $R_{th\ h-a}$ includes $R_{th\ mb-h}$ which is expected when heat-sink compound is used. $R_{th\ j-mb} \leqslant 5$ K/W.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

Supply voltage/output stage			
Supply voltage	$V_{9-8} = V_S$		9 to 30 V
Output voltage at $-I_6$ = 1.1 A	V_{6-8}	⩾ typ.	$V_{5-8} - 2.2$ V $V_{5-8} - 1.9$ V
at I_6 = 1.1 A	V_{6-8}	typ. ⩽	1.3 V 1.6 V
Flyback generator output voltage at $-I_6$ = 1.1 A	V_{7-8}	typ.	$V_S - 2.2$ V
Peak output current	$\pm I_6$	⩽	1.2 A
Flyback generator peak current	$\pm I_7$	⩽	1.2 A
Feedback			
Input quiescent current	$-I_{4;10}$	typ.	0.1 μA
Synchronization			
Sync input pulse	V_{2-8}		1 to 12 V
Tracking range		typ.	28 %
Oscillator/sawtooth generator			
Oscillator frequency control input voltage	V_{1-8}		6 to 9 V
Sawtooth generator output voltage	V_{3-8} V_{11-8}		0 to $V_S - 1$ V 0 to $V_S - 2$ V
Sawtooth generator output current	$-I_3$		0 to 4 mA
	I_{11}	⩾ ⩽	−2 μA +30 mA
Oscillator temperature dependency T_{case} = 20 to 100 °C	$(\Delta f/f)/\Delta T_{case}$	typ.	10^{-4} K^{-1}
Oscillator voltage dependency V_S = 10 to 30 V	$(\Delta f/f)/\Delta V_S$	typ.	4×10^{-4} V^{-1}
Blanking pulse generator			
Output voltage at V_S = 24 V; I_2 = 1 mA	V_{2-8}	typ.	18.5 V
Output current	$-I_2$	⩽	3 mA
Output resistance	R_{2-8}	typ.	410 Ω
Blanking pulse duration at 50 Hz sync	t_b	typ.	1.4 ± 0.07 ms
50 Hz/60 Hz switch capability			
Saturation voltage; LOW voltage level	V_{12-8}	typ.	1 V
Output leakage current	I_{12}	typ.	1 μA

Thermal resistance/junction temperature

From junction to mounting base	$R_{th\ j\text{-}mb}$	⩽	5 K/W
Junction temperature; switching point thermal protection	T_j	typ.	150 ± 8 °C

PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply (V_S)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

APPLICATION INFORMATION

The function is described against the corresponding pin number

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA.

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

APPLICATION INFORMATION (continued)

10. Reference voltage of preamplifier

    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

    This sawtooth capacitor has been split to realize linearity control.

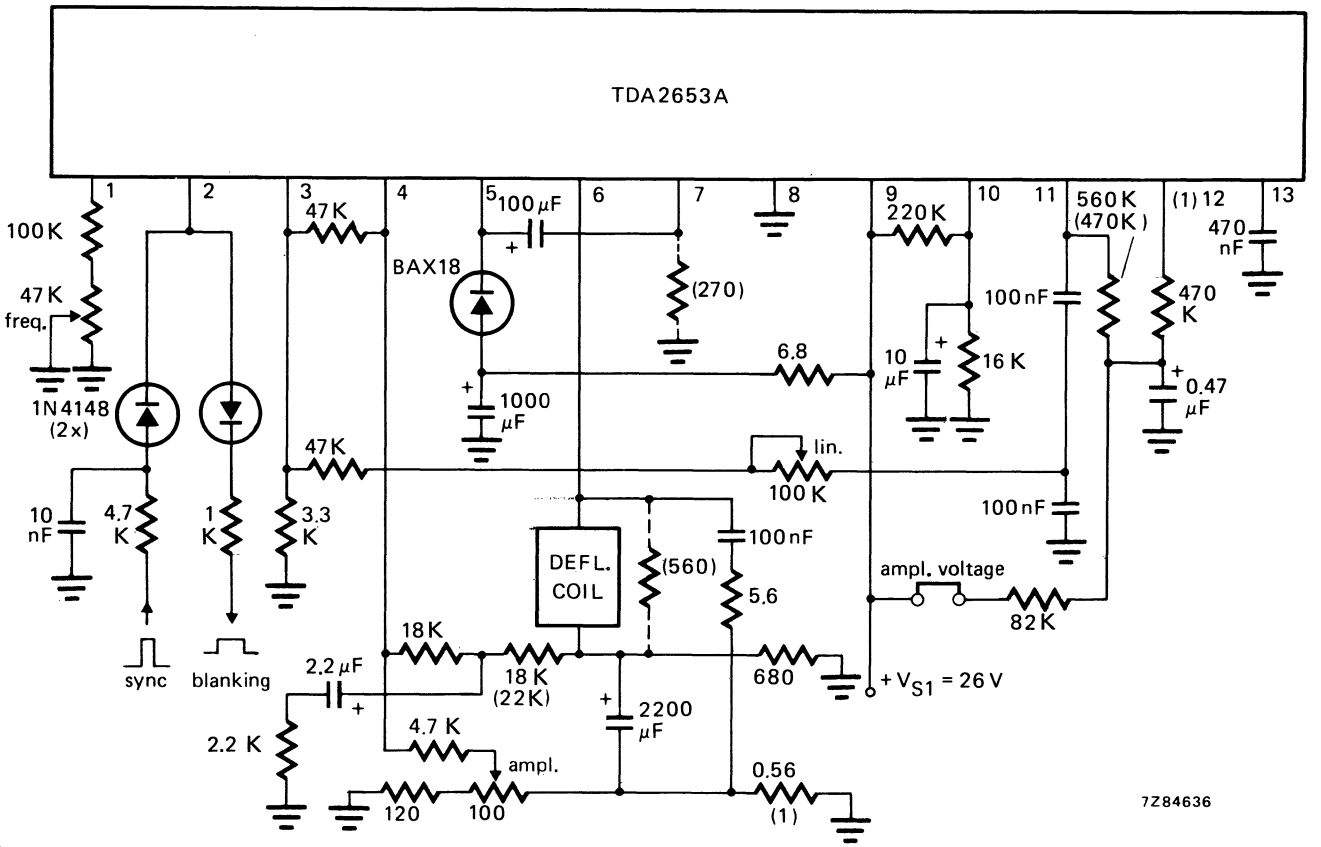
12. 50 Hz/60 Hz switching level

    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.

The following application data are measured in Figs 3 and 4.

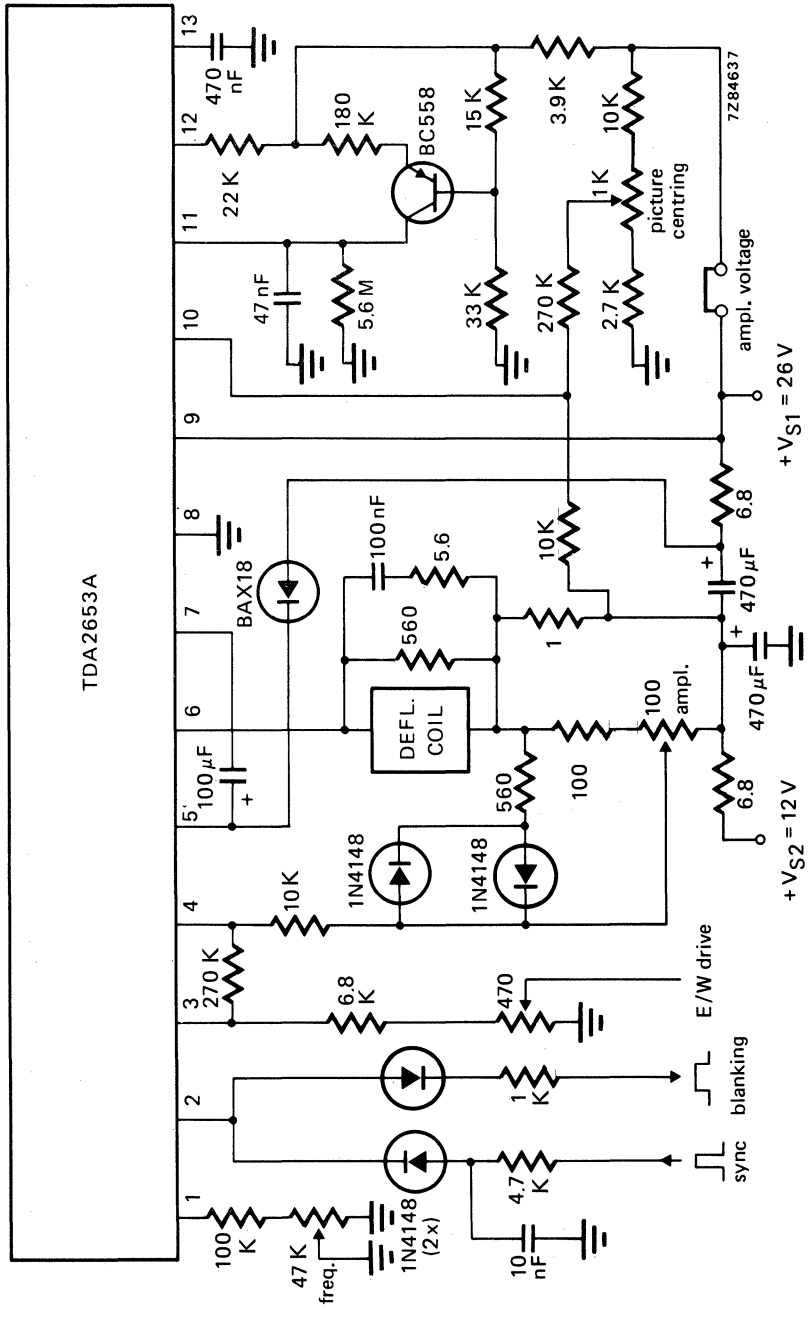
			30AX system (26 V) Fig. 3	30AX system (26 V/12 V) Fig. 4	PIL-S4 system Fig. 3
System supply voltages	V_{S1}	typ.	26	26	26 V
	V_{S2}	typ.	–	12	– V
System supply currents	I_{S1}	typ.	315	330	195 mA
	I_{S2}	typ.	–	–35	– mA
Output voltage	V_{6-8}	typ.	14	14.6	13.5 V
Output voltage (peak value)	V_{6-8}	typ.	42	42	49 V
Deflection current (peak-to-peak value)	$I_{6(p-p)}$	typ.	2.2	2.2	1.32 A
Flyback time	t_{fl}	typ.	1	0.9	1.1 ms
Total power dissipation per package	P_{tot}	typ.	4.1	4	3 W
		max.	4.8	4.8	3.4 W*
Oscillator frequency unsynchronized	f	typ.	46.5	46.5	46.5 Hz

* Calculated with $\Delta V_S = +5\%$ and $\Delta R_{yoke} = -7\%$.



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit for 30AX system (26 V). The values given in parentheses and the dotted components are valid for the PIL-S4 system.



(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 4 Typical vertical deflection circuit for 30AX system (V_{S1} = 26 V, V_{S2} = 12 V) in quasi-bridge connection.

The TDA3651A;AQ is a vertical deflection output circuit for drive of various deflection systems with deflection currents up to 2 A peak-to-peak.

The circuit incorporates the following functions:

- Driver
- Output stage
- Thermal protection and output stage protection
- Flyback generator
- Voltage stabilizer

QUICK REFERENCE DATA

			3651		3653		
Supply voltage (pin 9)	$V_{9-4} = V_P$		0 to 50	V		0 to 40	V
Peak output voltage during flyback (pin 5)	V_{5-4M}	<	55	V	max.	60	V
Output current (peak-to-peak value)	$I_{5(p-p)}$	<	1.5	A	max.	1.5	A
Operating junction temperature	T_j	max.	150	°C	max.	150	°C
Thermal resistance from junction to mounting base	$R_{th\ j-mb}$	typ.	3	K/W	typ.	10	K/W
					typ.	3.5	K/W

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PACKAGE OUTLINES

TDA3651A: 9-lead SIL; plastic power (SOT-131B).
TDA3651AQ: 9-lead SIL bent to DIL; plastic power (SOT-157B).
TDA3653: 9-lead SIL bent to DIL (SOT-110B).

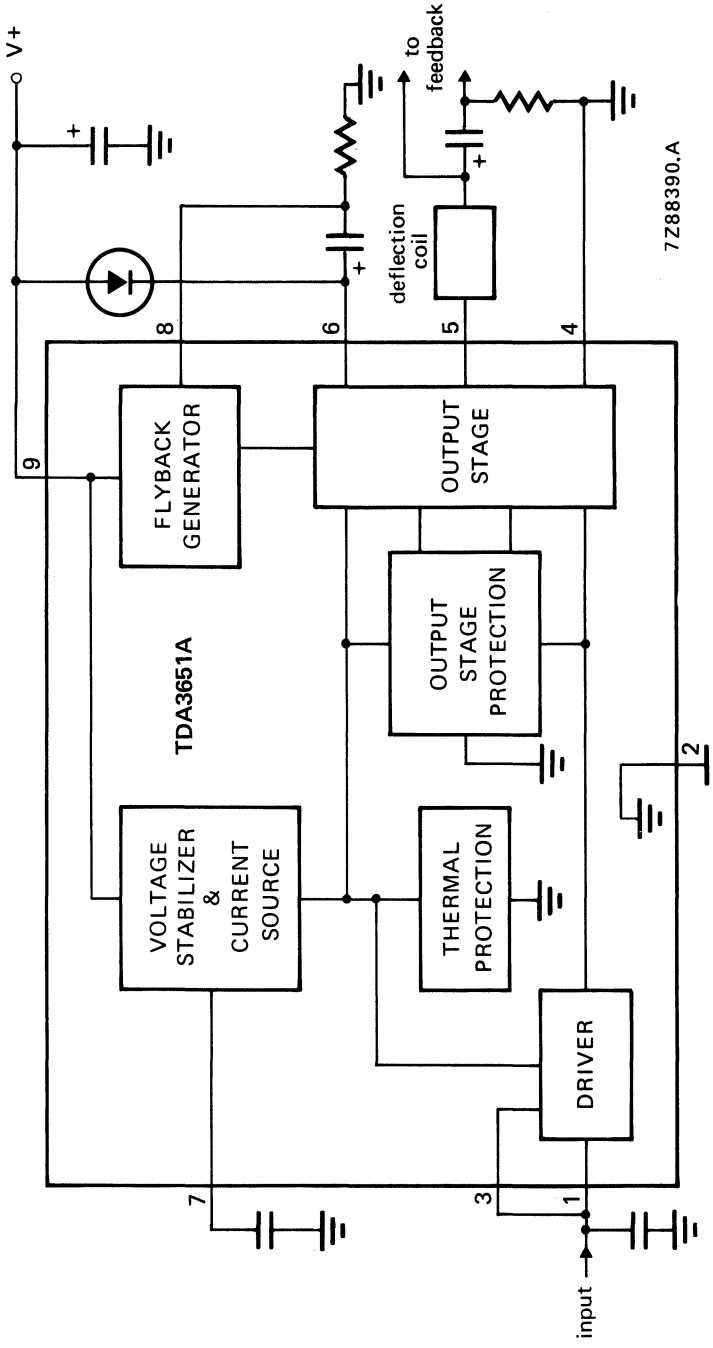

Fig. 1 Block diagram.

GENERAL DESCRIPTION

Output stage and protection circuit

Pin 5 is the output pin. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. The output transistors of the class-B output stage can each deliver 1 A maximum. The 'upper' power transistor is protected against short-circuit currents to ground, whereas, during flyback, the 'lower' power transistor is protected against too high voltages which may occur during adjustments.
Moreover, the output transistors have been given extra solidity by means of special measures in the internal circuit layout.
A thermal protection circuit is incorporated to protect the IC against too high dissipation. This circuit is 'active' at 175 ^{o}C and then reduces the deflection current to such a value that the dissipation cannot increase.

Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied to pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator. Pin 3 is connected externally to pin 1, in order to allow for different applications in which pin 3 is driven separate from pin 1.

Flyback generator

The capacitor at pin 6 is charged to a maximum voltage, which is equal to the supply voltage V_P (pin 9), during scan.
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage (pin 9), the flyback generator is activated. The V_P is connected in series (via pin 8) with the voltage across the capacitor.
The voltage at the supply pin (pin 6) of the output stage will then be maximum twice V_P. Lower voltages can be chosen by changing the value of the external resistor at pin 8.

Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V for drive of the output stage, so the drive current of the output stage is not affected by supply voltage variations. The stabilized voltage is available at pin 7.
A decoupling capacitor of 2,2 μF can be connected to this pin.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

		3651			3653		
Voltages (pins 4 and 2 externally connected to ground)							
Output voltage (pin 5)	V_{5-4}	max.	55	V	max.	60	V
Supply voltage (pin 9)	$V_{9-4} = V_P$	max.	50	V	max.	40	V
Supply voltage output stage (pin 6)	V_{6-4}	max.	55	V	max.	60	V
Input voltage (pins 1 and 3)	V_{1-2}; V_{3-2}	max.	V_P		max.	V_P	
External voltage (pin 7)	V_{7-2}		—		max.	5.6	V
Currents							
Repetitive peak output current (pin 5)	$\pm I_{5RM}$	max.	0.75	A	max.	0.75	A
Non-repetitive peak output current (pin 5)	$\pm I_{5SM}$	max.	1.5	A*	max.	1.5	A*
Repetitive peak flyback generator output current (pin 8)	I_{8SM}	max.	−0.75 +0.85	A A	max.	−0.75 +0.85	A A
Non-repetitive peak flyback generator output current (pin 8)	I_{8SM}	max.	−1.5 +1.6	A A*	max.	−1.5 +1.6	A A*
Temperatures							
Storage temperature range	T_{stg}	−65 to	+150	°C	−65 to	+150	
Operating ambient temperature range	T_{amb}	−25 to	+65	°C	−25 to	+65	
Operating junction temperature range	T_j	−25 to	+150	°C	−25 to	+150	

CHARACTERISTICS

T_{amb} = 25°C; V_P = 26V; pins 4 and 2 externally connected to ground; unless otherwise specified

		3651			3653		
Output current (peak-to-peak value)	$I_{5(p-p)}$	typ. <	1.2 1.5	A A	typ. <	1.2 1.5	A A
Flyback generator output current	$-I_8$	typ. <	0.7 0.85	A A	typ. <	0.7 0.85	A A
Flyback generator output current	I_8	typ. <	0.6 0.75	A A	typ. <	0.6 0.75	A A
Output voltages							
Peak voltage during flyback	V_{5-4M}	<	55	V	<	60	V
Saturation voltage to supply at $-I_5$ = 1A (3651); 0.6A (3653)	$-V_{5-6sat}$	typ. <	2.5 3.0	V V	typ. <	2.3 2.8	V V
Saturation voltage to ground at $-I_5$ = 1A (3651); 0.6A (3653)	V_{5-4sat}	typ. <	2.5 3.0	V V	typ. <	1.7 2.2	V V
Saturation voltage to supply at $-I_5$ = 0.75A	$-V_{5-6sat}$	typ. <	2.2 2.7	V V	typ. <	2.5 3.0	V V
Saturation voltage to ground at I_5 = 0.75A	V_{5-4sat}	typ. <	2.2 2.7	V V	typ. <	2.0 2.5	V V

*Non-repetitive duty factor maximum 3.3%.

		3651			3653		
Supply							
Supply voltage	$V_{9-2;\ 4}$		10 to 50	V*		10 to 40	V
Supply voltage output stage	V_{6-4}	<	55	V*	<	60	V
Supply current (no load and		typ.	9	mA	typ.	10	mA
no quiescent current)	I_9	<	12	mA	<	20	mA
		typ.	38	mA	typ.	25	mA
Quiescent Current (see Fig. 2)	I_4		25 to 52	mA		6 to 40	mA
Variation of quiescent current with temperature		typ.	-0.04	mA/K	typ.	-0.04	mA
Flyback generator							
Saturation voltage at $-I_8$ = 1.1A		typ.	1.6	V	typ.	1.6	V
(3651); 0.85A (3653)	V_{9-8sat}	<	2.1	V	<	2.1	V
Saturation voltage at I_8 = 1A		typ.	2.5	V	typ.	2.3	V
(3651); 0.75A (3653)	V_{8-9sat}	<	3.0	V	<	2.8	V
Saturation voltage at I_8 = 0.85A		typ.	1.4	V	typ.	1.4	V
(3651); 0.7A (3653)	V_{9-8sat}	<	1.9	V	<	1.9	V
Saturation voltage at I_8 = 0.75A		typ.	2.3	V	typ.	2.2	V
(3651); 0.6A (3653)	V_{8-9sat}	<	2.8	V	<	2.7	V
Flyback generator active if:	V_{5-9}	>	4	V	>	4	V
		typ.	250	μA	typ.	5	μA
Leakage current	$-I_8$	<	100	μA	<	100	μA
Input current for $\pm I_5$ = 1A		typ.	230	μA		—	
(3651); 1.5A (3653)	I_1		175 to 380	μA		1.3	mA
		typ.	1.9	V		—	
Input voltage during scan	V_{1-2}		0.9 to 2.7	V		3.2	V
Input current during scan	I_3		0.01 to 2.5	mA		.01 to .52	mA
Input voltage during scan	V_{3-2}		0.9 to V_P	V		0.9 to V_P	V
Input voltage during flyback	V_{3-2}		0 to 0.2	V		250	mV
		typ.	6.1	V	typ.	5.0	V
Voltage at pin 7	V_{7-2}		5.6 to 6.6	V		4.4 to 5.6	V
Load current of pin 7	I_7	<	15	V			
Unloaded voltage at pin 7 during flyback	V_{7-2}	typ.	15	V			
Junction temperature of switching		typ.	175	°C			
on the thermal protection	T_j		158 to 192	°C			
Thermal resistance from junction		typ.	3	K/W	typ.	10	K/W
to mounting base	$R_{th\ j\text{-}mb}$	<	4	K/W	<	12	K/W
Power dissipation	see Fig. 3						
Open loop gain at 1kHz; R_{load} = 1kΩ	G_o	typ.	36	dB	typ.	42	dB
Frequency response (-3dB); R_{load} = 1kΩ	f	typ.	60	kHz	typ.	40	kHz

*The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 55V.

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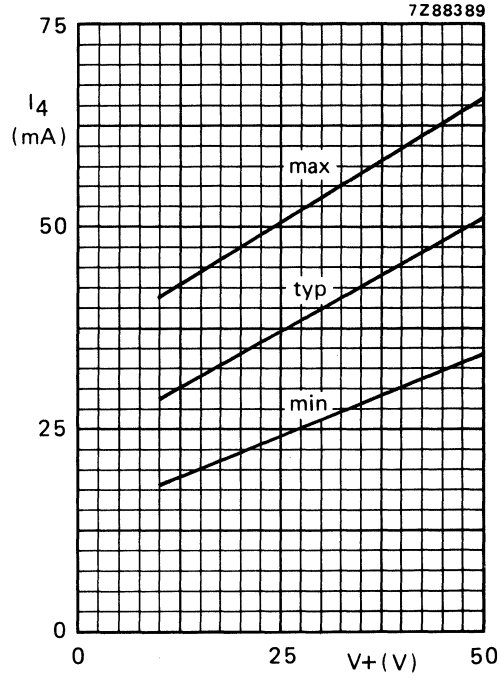

Fig. 2 Quiescent current I_4 as a function of supply voltage V_P.

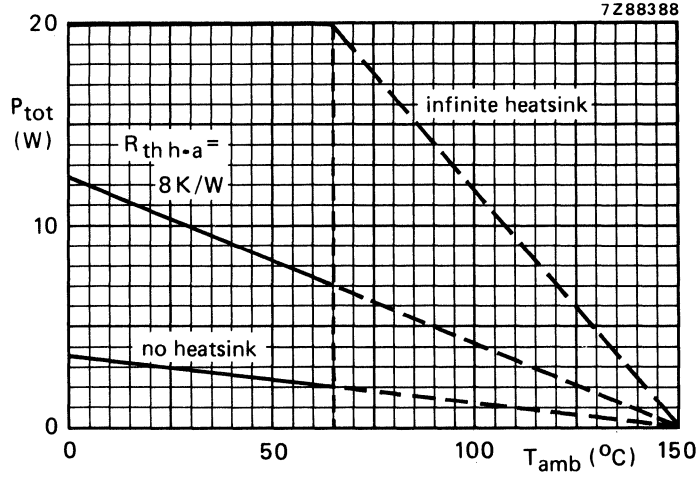

Fig. 3 Power derating curves.

APPLICATION INFORMATION

The following application data are measured in a typical application as shown in Figs 4 and 5.

Deflection current (including 6% overscan) peak-to-peak value	$I_{5(p-p)}$	typ.	0.87 A
Supply voltage	V_{9-4}	typ.	26 V
Total supply current	I_{tot}	typ.	148 mA
Peak output voltage during flyback	V_{5-4M}	<	50 V
Saturation voltage to supply	V_{5-6sat}	typ. <	2.0 V 2.5 V
Saturation voltage to ground	V_{5-4sat}	typ. <	2.0 V 2.5 V
Flyback time	t_{fl}	typ. <	0.95 ms 1.2 ms
Total power dissipation in IC	P_{tot}	typ.	2.5 W
Operating ambient temperature	T_{amb}	<	65 °C

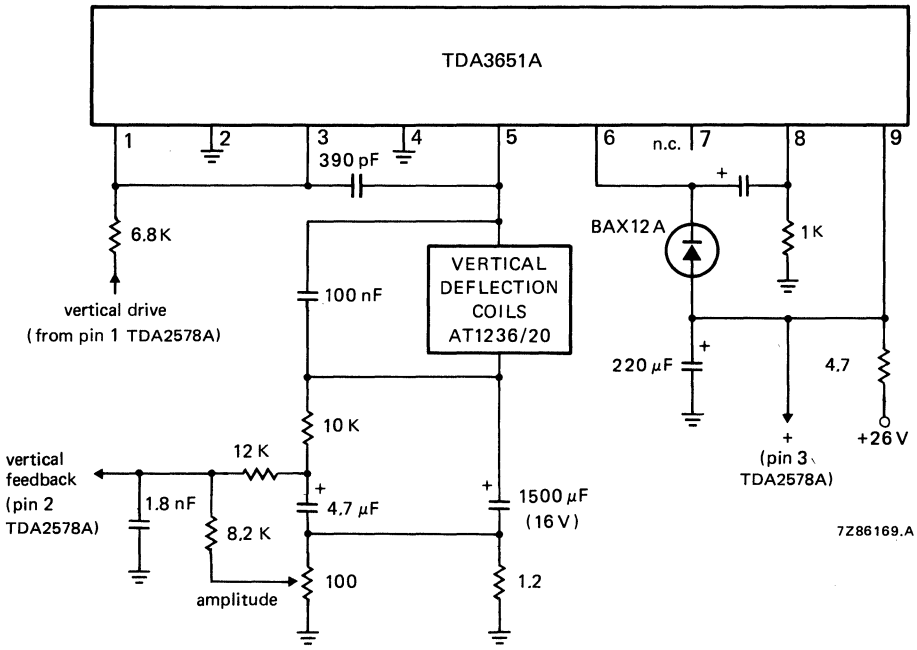

Fig. 4 Typical application circuit diagram of the TDA3651A (vertical output), when used in combination with the TDA2578A (see Fig. 5).

Note to deflection coils AT1236/20: L = 29 mH, R = 13.6 Ω; deflection current without overscan is 0.82 A peak-to-peak and EHT voltage is 25 kV.

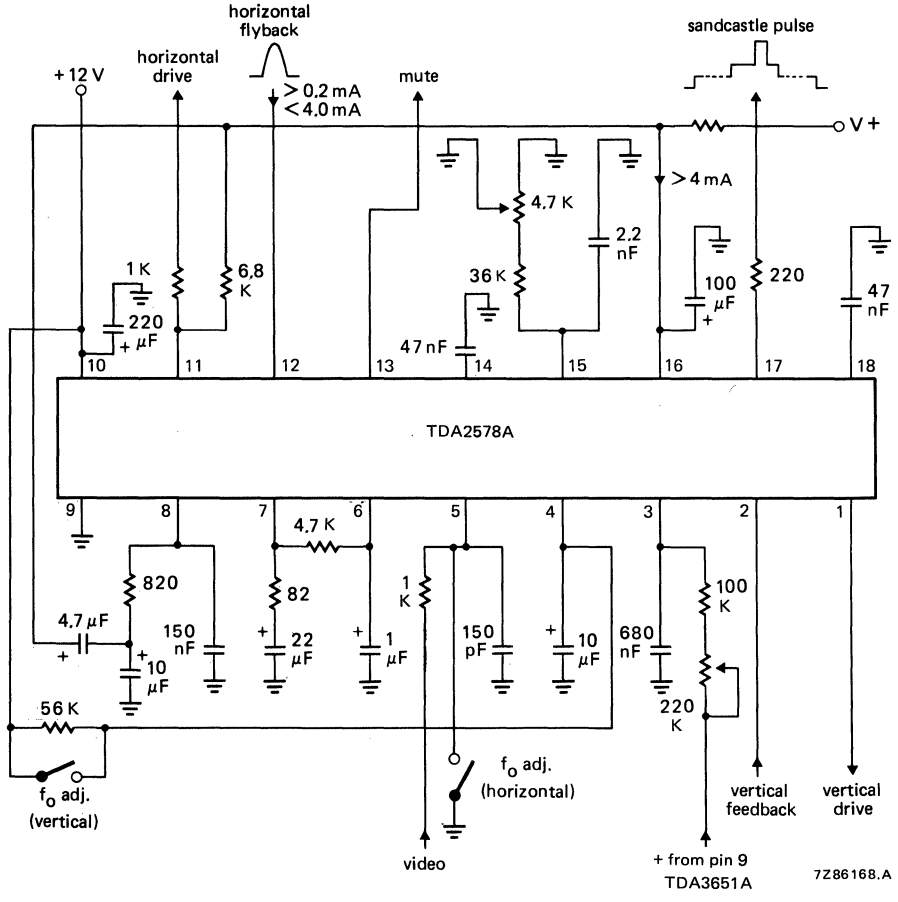

Fig. 5 Typical application circuit diagram; for combination of the TDA2578A with the TDA3651A see Fig. 4.

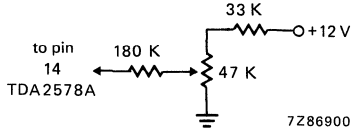

Fig. 6 Circuit configuration at pin 14 for phase adjustment.

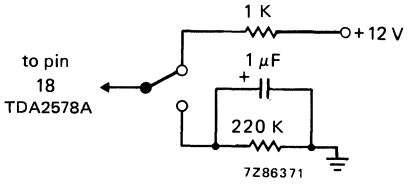

Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
220 kΩ between pin 18 and ground: with mute function.

Vertical Deflection — TDA3652

GENERAL DESCRIPTION

The TDA3652 is an integrated power output circuit for vertical deflection in systems with deflection currents up to 3 A peak to peak.

Features

- Driver
- Output stage and protection circuits
- Flyback generator
- Voltage stabilizer

QUICK REFERENCE DATA

Supply voltage (pin 9)	$V_{9-4} = V_P$		0 to 40 V
Peak output voltage during flyback (pin 5)	V_{5-4M}	<	55 V
Output current (peak-to-peak value)	$I_{5(p-p)}$	max.	3 A
Operating junction temperature	T_j	max.	150 °C
Thermal resistance from junction to mounting base	$R_{th\ j-mb}$	max.	4 K/W

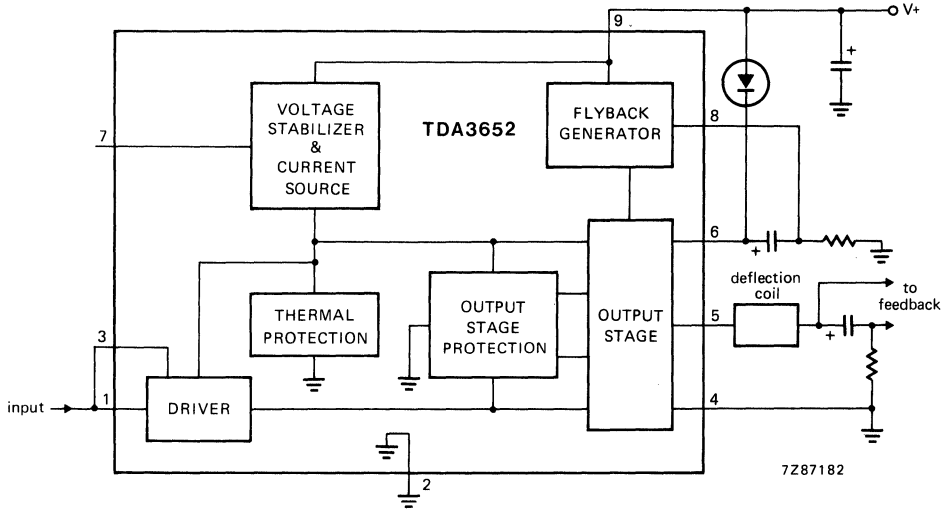

Fig. 1 Block diagram.

PACKAGE OUTLINES

TDA3652: 9-lead SIL; plastic (SOT-131B).
TDA3652Q: 9-lead SIL bent to DIL; plastic (SOT-157B).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages (pins 4 and 2 externally connected to ground)			
Output voltage (pin 5)	V_{5-4}		0 to 55 V
Supply voltage (pin 9)	$V_{9-4} = V_P$		0 to 40 V
Supply voltage output stage (pin 6)	V_{6-4}		0 to 55 V
Driver input voltage (pin 1)	V_{1-2}		0 to V_P V*
Switching circuit input voltage (pin 3)	V_{3-2}		0 to 5.6 V
Currents			
Repetitive peak output current (pin 5)	$\pm I_{5RM}$	max.	1.5 A
Non-repetitive peak output current (pin 5)	$\pm I_{5SM}$	max.	3 A**
Repetitive peak flyback generator output current (pin 8)	I_{8RM}	max.	−1.5 A +1.6 A
Non-repetitive peak flyback generator output current (pin 8)	$\pm I_{8SM}$	max.	3 A**
Temperatures			
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−25 to +65 °C
Operating junction temperature range	T_j		−25 to +150 °C

* The maximum input voltage should not exceed the supply voltage (V_P at pin 9). In most applications pin 1 is connected to pin 3; the maximum input voltage should then not exceed 5.6 V.

** Non-repetitive duty factor maximum 3.3%.

CHARACTERISTICS

V_P = 26 V; T_{amb} = 25 °C; pins 4 and 2 externally connected to ground; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage; pin 9	V_P	10	–	40	V*
Supply voltage output stage; pin 6	V_{6-4}	–	–	55	V*
Supply current (no load and no quiescent current); pin 9	I_P	–	9	12	mA
Quiescent current (see Fig. 2)	I_4	25	40	65	mA
Variation of quiescent current with temperature	ΔI_4	–	−0.04	–	mA/K
Output current					
Output current (pin 5) (peak-to-peak value)	$I_{5(p-p)}$	–	2.5	3.0	A
Output current flyback generator (pin 8)	$-I_8$	–	1.35	1.6	A
Output current flyback generator (pin 8)	I_8	–	1.25	1.5	A
Output voltage					
Peak voltage during flyback	V_{5-4M}	–	–	55	V
Saturation voltage to supply at $-I_5$ = 1.5 A	$-V_{5-6sat}$	–	2.5	3.0	V
Saturation voltage to ground at I_5 = 1.5 A	V_{5-4sat}	–	2.5	3.0	V
Saturation voltage to supply at $-I_5$ = 1 A	$-V_{5-6sat}$	–	2.2	2.7	V
Saturation voltage to ground at I_5 = 1 A	V_{5-4sat}	–	2.2	2.7	V
Flyback generator					
Saturation voltage at $-I_8$ = 1.6 A	V_{9-8sat}	–	1.6	2.1	V
Saturation voltage at I_8 = 1.5 A	V_{8-9sat}	–	2.5	3.0	V
Saturation voltage at $-I_8$ = 1.1 A	V_{9-8sat}	–	1.4	1.9	V
Saturation voltage at I_8 = 1 A	V_{8-9sat}	–	2.3	2.8	V
Flyback generator active if:	V_{5-9}	4	–	–	V
Leakage current at pin 8	$-I_8$	–	5	100	μA
Input current for I_5 = 4 A at pin 1 (peak-to-peak value)	$I_{1(p-p)}$	190	240	400	μA
Input voltage during scan (pin 1)	V_{1-2}	1.3	2.0	3.5	V
Input current during scan (pin 3)	I_3	0.01	–	2.5	mA

* The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 55 V.

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CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Flyback generator (continued)					
Input voltage during scan (pin 3)	V_{3-2}	0.9	–	5.6	V
Input voltage during flyback (pin 3)	V_{3-2}	0	–	0.2	V
General data					
Junction temperature of switching on the thermal protection	T_j	158	175	192	°C
Thermal resistance from junction to mounting base	$R_{th\ j\text{-}mb}$	–	–	4	K/W
Total power dissipation	P_{tot}		see Fig. 3		
Open-loop gain at 1 kHz	G_o	–	36	–	dB
Frequency response (–3 dB) at R_L = 1 kΩ	f	–	50	–	kHz

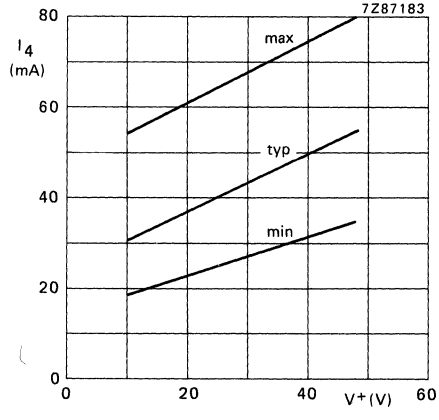


Fig. 2 Quiescent current (I_4) as a function of supply voltage (V_P).

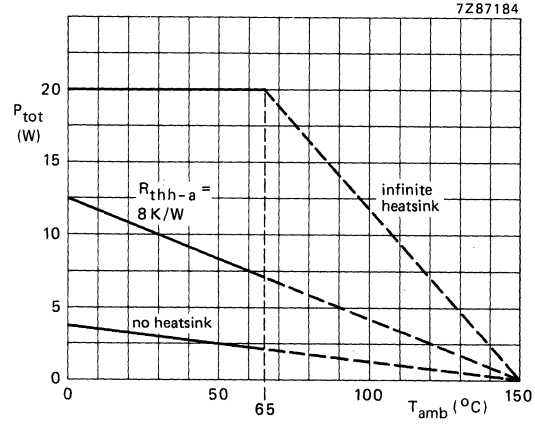


Fig. 3 Power derating curve.

APPLICATION INFORMATION

The function is described against the corresponding pin number.

1. Driver

This is the input for the driver of the output stage.

2. Negative supply (ground)

3. Switching circuit

This pin is normally connected externally to pin 1. It is also possible to use this pin to drive the switching circuit for different applications. This switching circuit rapidly turns off the lower output stage at the end of scan and also allows for a quick start of the flyback generator.

4. Output stage ground

5 and 6. Output stage and protection circuits

Pin 5 is the output pin and pin 6 is the output stage supply pin. The output stage is a class-B type with each transistor capable of delivering 1.5 A maximum. The "upper" output transistor is protected against short-circuit currents to ground. The base of the "lower" power transistor is connected to ground during flyback and so it is protected against too high flyback pulses which may occur during adjustments. In addition the output transistors are protected by a special layout of the internal circuit. The circuit is protected thermally against excessive dissipation by a circuit which operates at temperatures of 175 ^{o}C upwards causing the output current to drop to a value such that the dissipation cannot increase.

7. Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply voltage of 6 V for drive of the output stage, so the drive current is not influenced by the various voltages of different applications.

8 and 9. Flyback generator

Pin 8 is the output pin of the flyback generator. Depending on the value of the external resistor at pin 8, the capacitor at pin 6 will be charged to a fixed level during the scan period. The maximum height of this level is equal to the supply voltage at pin 9 (V_P). When the flyback starts and the flyback pulse at pin 5 exceeds the supply voltage, the flyback generator is activated and then the supply voltage is connected in series (via pin 8) with the voltage across the capacitor. The voltage at the supply pin (pin 6) of the output stage will then be not more than twice the supply voltage.

NTSC Decoder TDA3654

DESCRIPTION

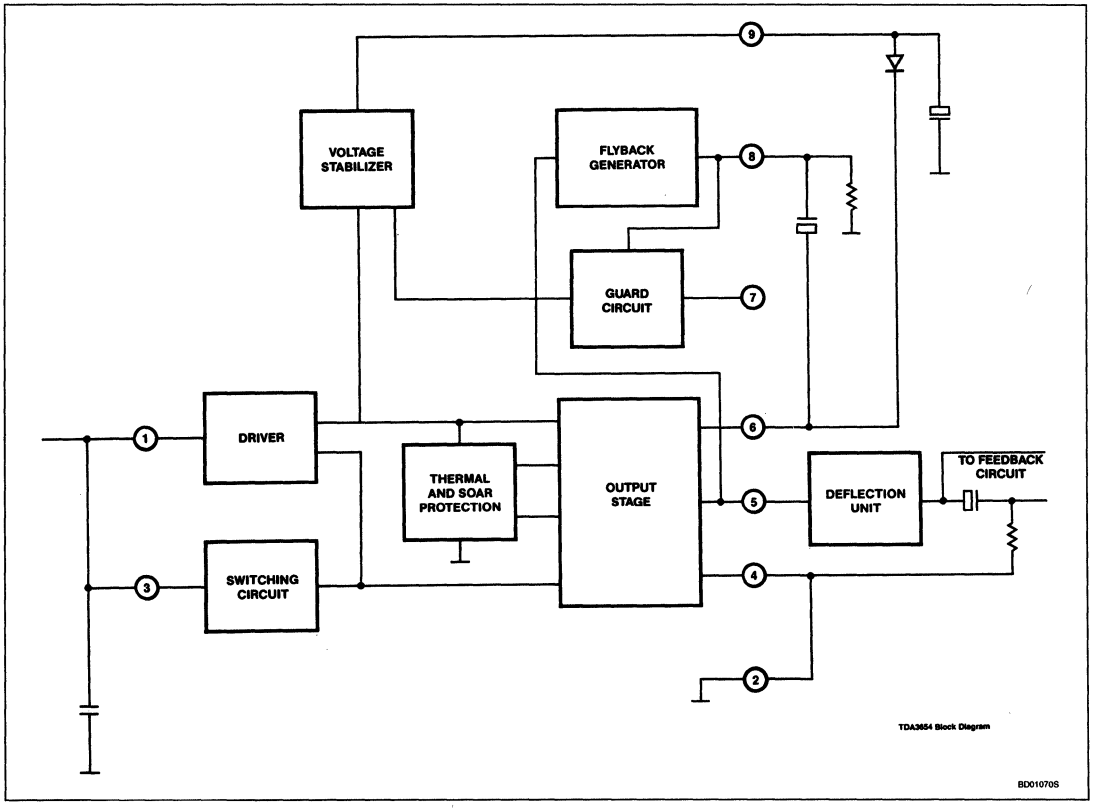
The TDA3654 is a full performance vertical deflection output circuit intended for direct drive of the deflection coils. It can be used for a wide range of 90° and 100° deflection systems.

The TDA3654 is provided with a guard circuit which blanks the picture tube screen in case of absence of the deflection current.

FEATURES

- **Output stage**
- **Thermal protection and SOAR protection circuits**
- **Driver and switching circuit**
- **Flyback generator**
- **Voltage stabilizer**
- **Guard circuit**

BLOCK DIAGRAM



NTSC Decoder TDA3654

ORDERING CODE

	PINS	PACKAGE	NOTE
TDA3654	9	Plastic SIL	SOT-131B
TDA3654	9	Plastic SIL bent to DIL	SOT-157B

REFERENCE DATA

PARAMETER	LIMITS			UNIT
	Min	Typ	Max	
Output voltage, V_5			60	V
Output current (peak to peak), I_5			3.0	A
Supply voltage, pin 9			40	V
Supply voltage output stage, V_{6-4}			60	V
Peak voltage during flyback, V_{5-4}			60	V
Input current of pin 1 for $I_5 = 1.5A$		0.33	0.55	mA
Input voltage during scan (pin 1), V_{1-2}		2.35	3.0	V

Signetics

Applications
Section 9

Linear Products

Monolithic 14-Bit DAC with 85dB S/N Ratio AN110

R. J. v. d. PLASSCHE

The introduction of digital signal processing in sound recording and reproduction systems imposes stringent requirements on the performance of digital-to-analogue converters (DACs). Many of these systems demand converters with up to 16-bit resolution to obtain sufficiently high signal-to-noise ratio and good linearity.

The TDA1540 is the first monolithic bipolar 14-bit DAC with a signal-to-noise ratio of 85 dB (typ) for audio signals, sampled at 44 kHz. It uses a new method of current division, called dynamic element matching, to achieve high-accuracy binary-weighted currents, with long-term stability. Dynamic element matching combines passive division with a time division concept which eliminates resistor trimming.

In addition, the TDA1540 features:

- on-chip serial-to-parallel shift register and data latches,
- on-chip current reference,
- inherent monotonicity from −25 to +70 °C,
- TTL compatible input,
- serial data input (offset binary) which reduces feed-through and correlated noise,
- improved bit switching – no deglitching circuit required.

Table 1 gives further data on the TDA1540.

STANDARD DIGITAL-TO-ANALOGUE CONVERSION TECHNIQUES

Monolithic DACs widely use an R-2R resistive ladder network with multiple-emitter terminating transistors to generate binary-weighted currents. These currents are switched by digitally-controlled switches (bit switches) to a summing point; thereby digital-to-analogue signal conversion is performed. Figure 1 shows a DAC of this type.

There are two problems in the design of an R-2R DAC: the weighting accuracy of the binary currents which is set by the tolerance of the resistors and transistors, and the switching of the accurately weighted binary currents without glitches which determines the dynamic performance. Regarding the problem of accuracy, Table 2 shows that it is straightforward to integrate DACs having up to 10 bits; a 10-bit converter requires a 512:1 current division, i.e. requires resistor tolerance better than 0.05%. Twelve-bit converters usually need laser trimming of thin-film resistors, or trimming of the binary-weighted currents using Zener zapping to achieve 12-bit accuracy.

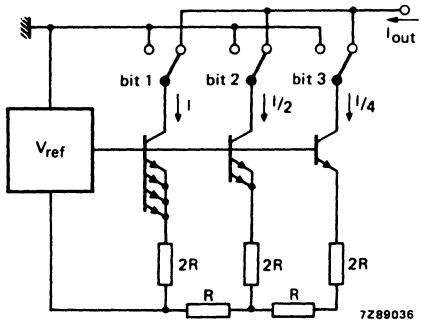


Fig.1 3-bit binary-weighted R-2R digital-to-analogue converter

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TABLE 1
TDA1540 data

Resolution	14 bits
Signal-to-noise ratio* (typ.)	85 dB
Linearity (typ.)	±¼LSB at T_{amb} = 25 °C
	±½LSB −20 °C < T_{amb} < +70 °C
Full-scale current (typ.)	4 mA
Settling time to ±½LSB (for a full-scale change)	typ. 1 μs
Maximum input bit rate	12 Mbit/s
Power dissipation	350 mW
Supply voltages	+5 V, −5 V and −17 V
Encapsulation	28-pin ceramic DIL

* measured between 31,5 Hz and 20 kHz at a sampling frequency of 44 kHz.

TABLE 2
Matching tolerance of different types of resistor

fabrication process	matching tolerance			
	σ(%)		mean (%)	
	10 μm	40 μm	10 μm	40 μm
Diffusion	0.44	0.23	−0.1	0.07
Thin-film	0.24	0.11	−0.1	−0.06
Ion implantation	0.34	0.12	−0.04	0.05

Resistor linewidth 10 μm and 40 μm.

It is questionable how successfully trimming can be applied to 14 or 16-bit converters. Mounting the chip after trimming can change the resistances; trimming after mounting can be expensive. Long-term stability may be a problem too. Furthermore, the cost of laser trimming in large-volume production can be significant.

In the TDA1540 trimming has been eliminated by dynamic element matching.

DYNAMIC ELEMENT MATCHING

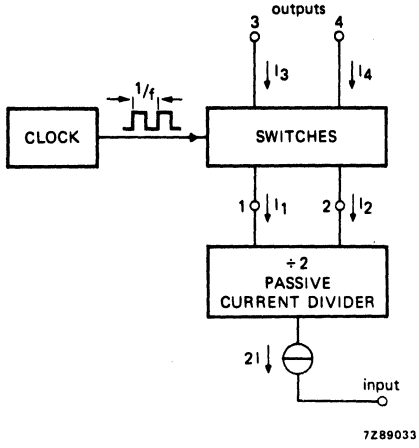
Basic current divider

Figure 2(a) shows the block diagram of the divider. It consists of a passive current divider and a set of switches driven at a frequency f by a clock pulse generator.

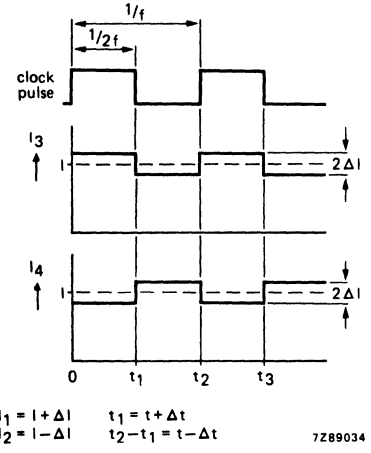
The input current 2I is divided into two nearly equal parts: $I_1 = I + \Delta I$ and $I_2 = I - \Delta I$. Then, I_1 and I_2 are interchanged with respect to the output terminals 3 and 4 *for equal times* by means of the switches. The average current at each output terminal is then exactly equal and has a value I, see Fig.2(b).

There is a small ripple current 2ΔI (p-to-p) of frequency f on the output currents. This ripple is proportional to the accuracy of current division by the passive divider. By using a simple low-pass filter to suppress the ripple an exact current ratio of 2:1 (input-to-output) is obtained.

If the time that I_1 and I_2 are switched to each output differs by Δt, see Fig.2(b), there will be an error in their 1:1 current ratio of $(\Delta t/t)(\Delta I/I)$. For $\Delta I/I \approx 1\%$ and $\Delta t/t \approx 0.1\%$, this error is ≈0.001%.



(a) Basic current divider using dynamic element matching



(b) Output currents I_3 and I_4

Fig.2

By cascading divider stages an accurate binary-weighted current network is formed. However, in a practical circuit, each stage requires a minimum supply voltage of ≈2 V. This leads to an impractically large supply voltage for a 14-bit current network. Therefore, an improved divider is used which gives more weighted currents in one current interchange.

Improved divider

In the improved divider, a current 4I is divided into four nearly equal parts: $I + \Delta_1 I$, $I + \Delta_2 I$, $I + \Delta_3 I$ and $I + \Delta_4 I$, see Fig.3(a). Note that $\Delta_1 + \Delta_2 + \Delta_3 + \Delta_4 = 0$.

These currents are fed into a switching network which interchanges all the currents with respect to the output terminals for equal times. The switches are controlled by signals from a 4-bit shift register.

At the output of the switching network, two currents are combined; thus, the output currents have average values of 2I, I and I, Fig.3(b). All currents have a ripple of frequency f/4 (the time for one complete interchange of the four currents being 4/f). Timing errors in the current switching have the same effect on accuracy as for the basic divider.

Figure 4 shows the circuit diagram of a practical current divider. Transistors TR1, TR2, TR3 and TR4, with the resistors R divide the current 4I into four nearly equal currents. These currents are fed into the switching network which consists of Darlington transistor switches to minimise base current loss. Two currents are summed directly giving an output current of 2I (av.). A 4-bit shift register controls the transistor switches which for accurate current division must have high current gain.

BINARY-WEIGHTED CURRENT NETWORK

By cascading divider stages, a binary-weighted current network is formed, see Fig.5. In the first stage the on-chip reference current source I_{ref} and a current amplifier form an accurate current mirror. The reference current is used as the most significant bit current, which eliminates filtering.

To obtain 14-bit accuracy, a choice can be made between the number of switched and unswitched current dividers. The minimum supply voltage decreases as the number of unswitched dividers increases. However, the number of unswitched dividers is limited by circuit yield. Five switched dividers followed by a 4-bit passive divider using emitter scaling represents the best compromise between supply voltage and circuit yield.

FILTERS AND BIT SWITCHES

Figure 6 shows how the output currents of a switched divider stage are filtered and switched to the output. R1C1 and R2C2 form first-order filters (the capacitors are connected externally). Darlington transistors TR3, TR4 and TR5, TR6 isolate the filters from the switching of the binary-weighted currents to the output (bit switching). Bit switching is performed with a diode-transistor configuration TR1, D1 and TR2, D2, enabling fast and accurate switching with no loss of base currents.

Individual filtering of bit currents minimises the noise of the TDA1540 output current, and makes the conversion time solely dependent upon the speed of the bit switches.

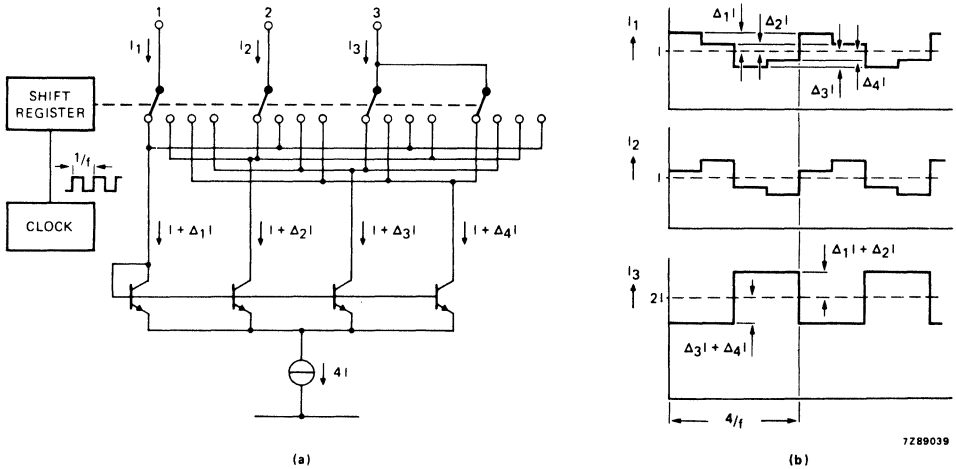


Fig.3
(a) Improved current divider. (b) Output currents I_1, I_2 and I_3

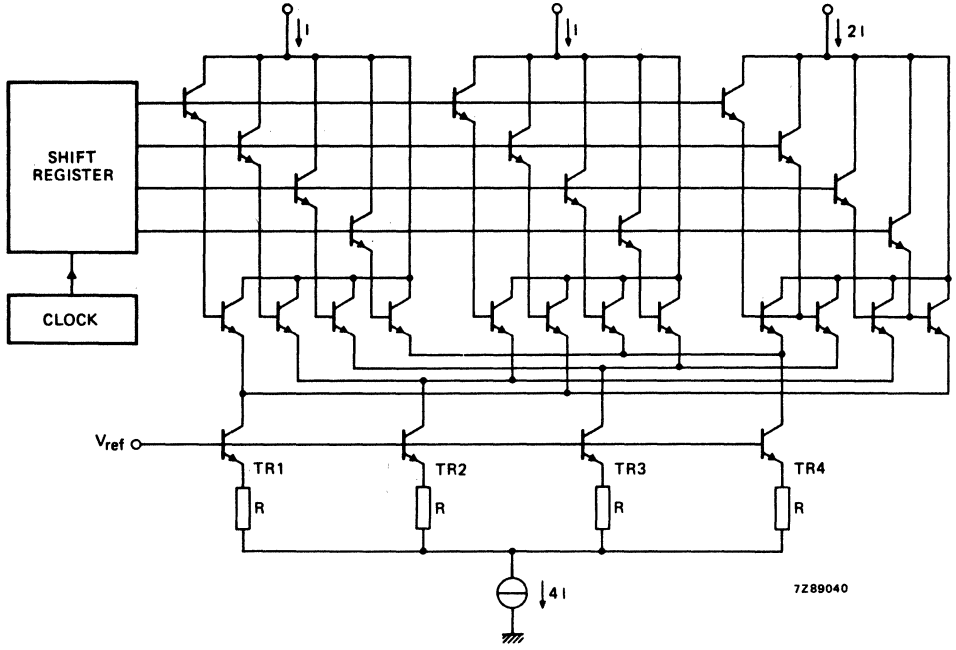


Fig.4 Circuit diagram of the practical current divider

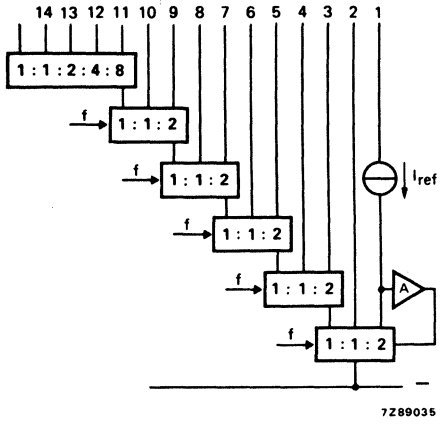


Fig.5 Binary-weighted current network

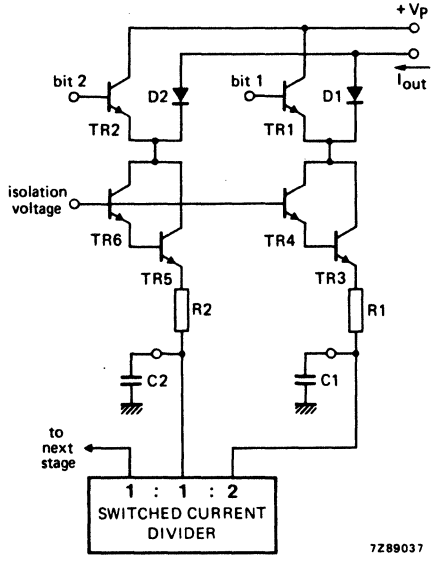


Fig.6 Filtering and switching the binary-weighted currents to the output

COMPLETE 14-BIT DAC

Figure 7 is the block diagram of the complete DAC. It shows the 14-bit binary-weighted current network, the reference current source, individual bit-current filters and the bit switches. The shift register that controls the Darlington transistor switches is at the bottom of the figure.

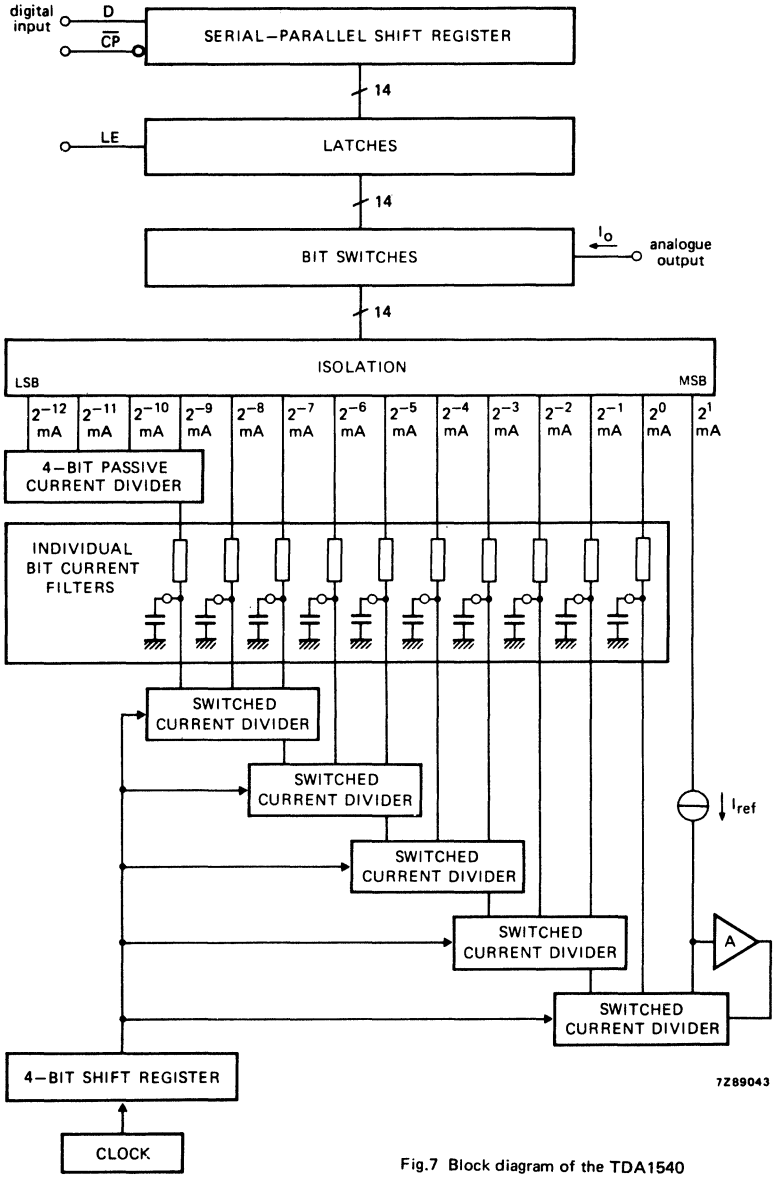


Fig.7 Block diagram of the TDA1540

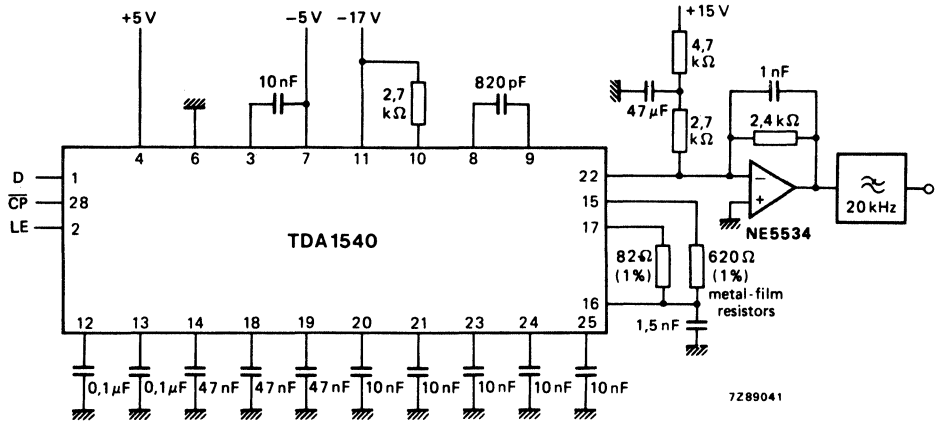


Fig.8 Circuit diagram of a voltage-output digital-to-analogue converter using the TDA1540

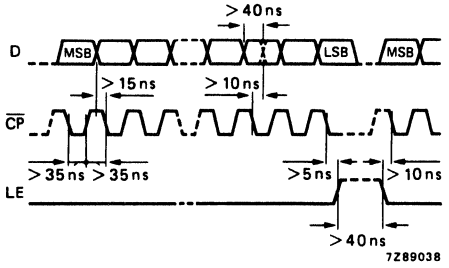


Fig.9 TDA1540 timing diagram

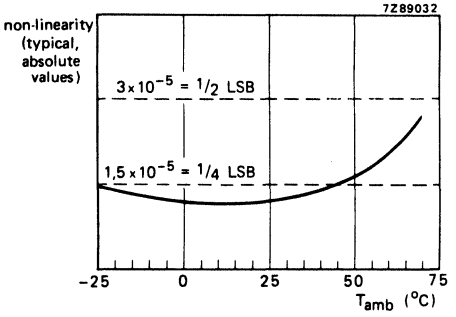


Fig.10 Non-linearity of the TDA1540 as a function of temperature

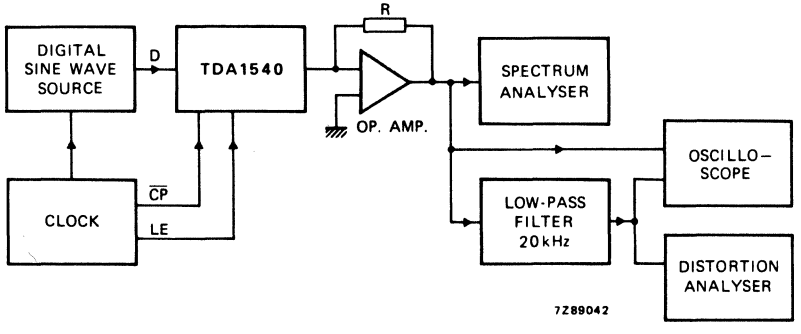


Fig.11 Arrangement for measuring dynamic performance

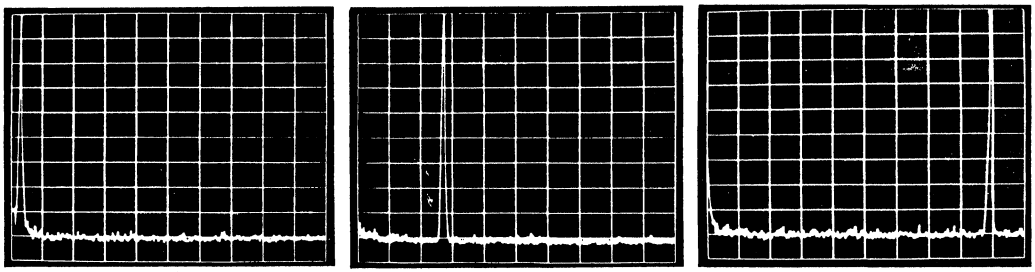


Fig.12 Distortion of an output sinewave of frequency 600 Hz, 5.5 kHz and 18 kHz, respectively. Vertical scale 10 dB/div., horizontal scale 2 kHz/div. Bandwidth 30 Hz

Figure 8 shows how to obtain a voltage output using the TDA1540 with an operational amplifier.
Figure 9 shows the input data format D, and the corresponding timing signals $\overline{CP}$ (clock input) and LE (latch enable).

PERFORMANCE

Linearity

A DAC is monotonic if the non-linearity is less than ±½ LSB. Figure 10 shows that the non-linearity of the TDA1540 is typically less than ½LSB (3×10^{-5}) over the temperature range −20 to +70 °C.

Dynamic performance

Figure 11 shows the arrangement used to measure dynamic performance. A digital sine wave source produces 14-bit words which are latched at 44 kHz. The outputs of the latches drive directly the bit switches of the converter. A high-speed operational amplifier with feedback resistor R converts the output current of the converter into a voltage suitable for examination by spectrum analyser and oscilloscope, or distortion analyser.

Figure 12 shows the results of spectrum analysis. For sine waves of 600 Hz, 5.5 kHz and 18 kHz, distortion is about −90 dB with respect to the maximum sine wave output. Note, −90 dB is the limit of resolution of the spectrum analyser.

Figure 13 shows oscillograms of the filtered and unfiltered output signals. The low-pass filter introduces a delay in the output signal.

APPLICATIONS

Dynamic element matching is a simple, accurate and reliable method of current division for high-accuracy monolithic DACs; the resulting dynamic performance of the TDA1540 makes it ideal for sound reproduction and recording systems.

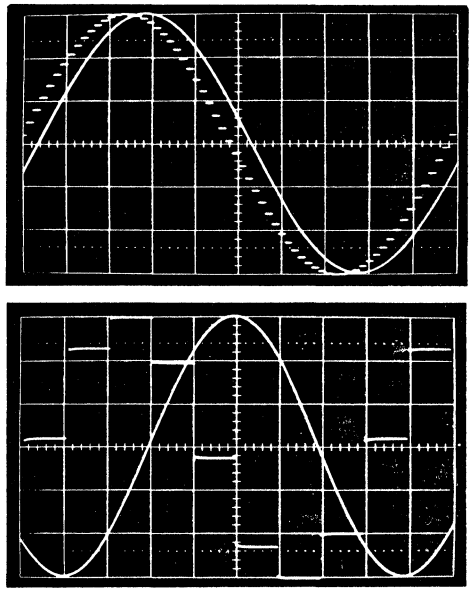


Fig.13 Filtered and unfiltered output signals: above, 1 kHz; below, 6.3 kHz. Vertical scale 0.33 volt/div.

Its 15-bit linearity also makes it suitable for applications that do not require 14-bit resolution, but demand high linearity to improve relative accuracy. Such applications include graphic display systems, electron-beam recording and nuclear instrumentation.

The TDA1540 easily fulfills the requirements of a 12-bit DAC for telephony. For instrument manufacturers, the TDA1540 can extend present limits of performance of distortion meters, spectrum analysers, sine wave and other signal generators.

The use of over-sampling techniques with the TDA1540 further improves the S/N ratio in audio applications and simplifies output analogue filters.

Designing With The SA/NE602

AN198

INTRODUCTION

The SA/NE602 represents a new industry standard for low power, double-balanced mixers. This device also includes an on-board local oscillator and voltage regulator. Typical power supply requirements are 2.5mA at 6 volts for a conversion gain of 20dB and a noise figure of 5dB with operation up to 200MHz. The SA/NE602 is available in either an eight pin DIP or a surface mount package. These specifications render this device an ideal choice for portable battery-operated applications.

CIRCUIT CONFIGURATIONS

Figure 1 shows a simplified block diagram of the SA/NE602. A multiplier "Gilbert Cell" is used as the mixer portion of the device with the input differential amplifier providing most of the conversion gain. This differential amplifier also serves as an input balun which helps reduce the second-order distortion products.

Figure 2 shows some possible balanced and unbalanced input and output circuits while Table 1 summarizes these configurations' relative advantages and disadvantages.

Figure 3 shows the internal circuitry adjacent to the device pins. The oscillator can be configured with a crystal, a tank, or as a buffer/driver for an external oscillator. When used as a buffer amplifier, optimum performance will be achieved when pin 6 is driven with a 200 to 300mV RMS signal. This LO amplitude tolerance becomes more critical as the LO frequency approaches the 200MHz maximum. Figure 4 shows a typical test circuit for the SA/NE602. For this circuit it is important to specify the *parallel mode* crystal frequency and use a crystal with a loading capacitance of 5pF.

DESIGN DATA

Figure 6 shows typical intermodulation and compression point performance of the SA/NE602. The compression point defines the upper limit of the effective mixer dynamic range at about −25dBm. This level is mainly a function of the circuit insertion loss prior to the 602 input. The input third order intercept point is shown here at the minimum value of −15dBm, and, as such, can be considered a worst case condition.

The remaining charts show various mixer parameters over temperature and supply voltage variation. The overall optimum supply voltage is 6 volts, and this value is thus recommended. Unless specifically indicated, Figure 4 was the test circuit used to produce the data. The frequency schemes used here are typical of those found in cellular radio applications employing a 455kHz 2nd IF. All of the major specifications are nearly constant over the 200MHz frequency range with the exception of the LO drive level tolerance and device impedances.

OSCILLATOR ALIGNMENT

The objective in measuring the crystal oscillator frequency in a production environment is to read the data without loading the circuit. This can be accomplished by using one of two methods. The first uses a small inductive loop placed near the oscillator circuit. The loop feeds a suitable amplifier which drives a counter. The second method takes advantage of LO leakage into the output. Again, with the oscillator running and no RF input signal present, the 602 output is connected to an amplifier and counter. The single-ended output configuration will provide more LO leakage and the mixer itself will act as a buffer.

Written by: Bob Zavrel

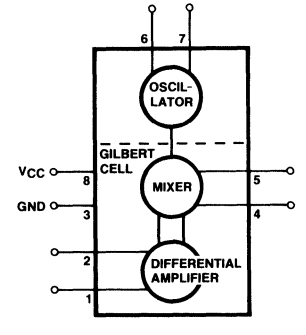


Figure 1. SA/NE602 Functional Diagram

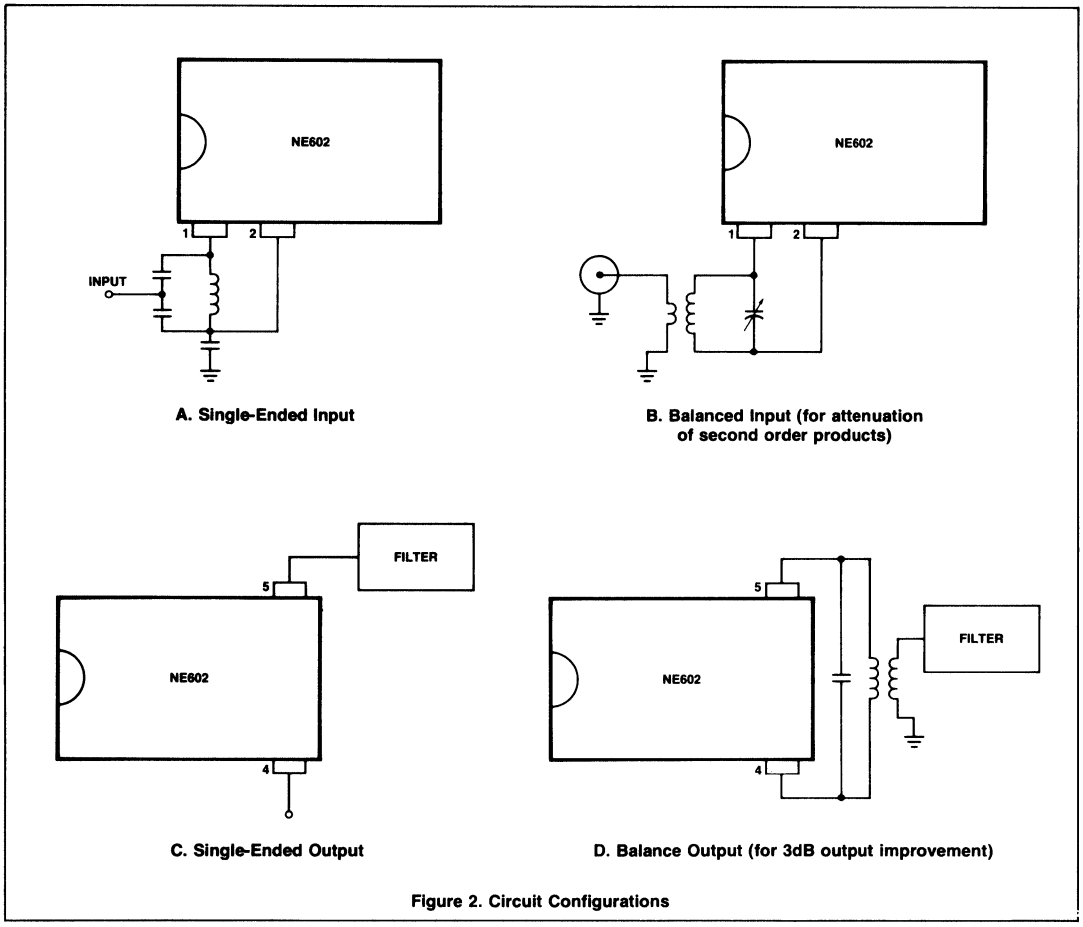


Figure 2. Circuit Configurations

TABLE 1

		ADVANTAGES	DISADVANTAGES
Input Pins 1 & 2	Single-ended	No sacrifice in 3rd order performance, simplified circuit	Increase in 2nd order products
	Balanced	Reduce 2nd order products	Impedance match more difficult to achieve
Output Pins 4 & 5	Single-ended	Simple interface to filters	3dB reduction in output, less RF and LO isolation
	Balanced	3dB improvement in output, better LO and RF isolation at the output	more complex circuitry required

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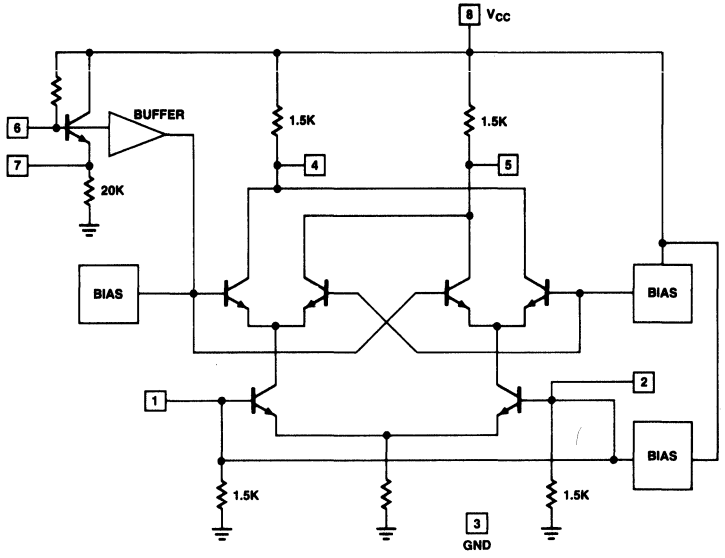


Figure 3. SA/NE602 Equiv Circuit

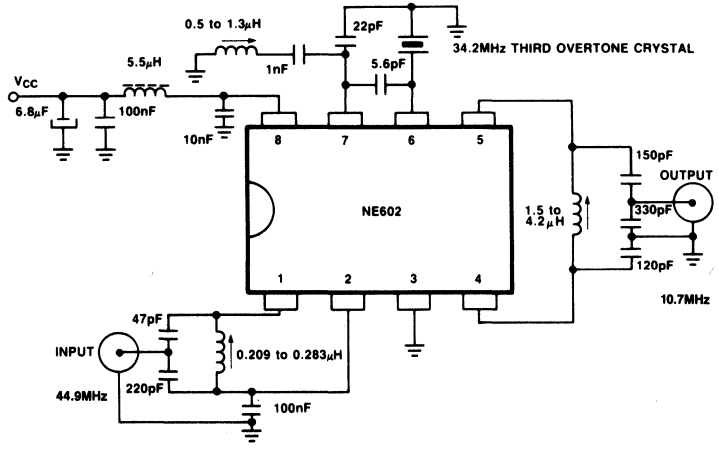


Figure 4. Typical Application

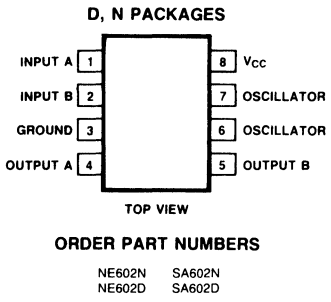


Figure 5. Pin Configuration

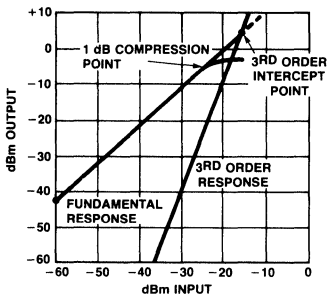


Figure 6. SA/NE602 3RD Order Intermod and 1dB Compression Point Performance

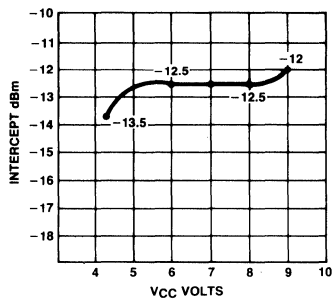


Figure 7. Input Third Order Intercept Point Vs V_{CC}

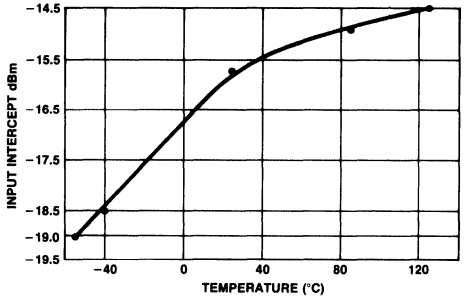


Figure 8. Third Order Intercept Point Vs Temperature

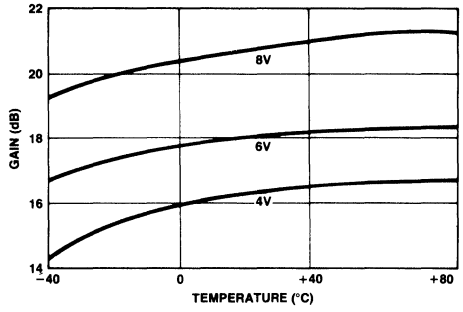


Figure 9.

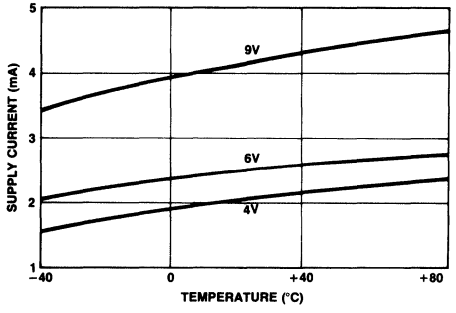


Figure 10.

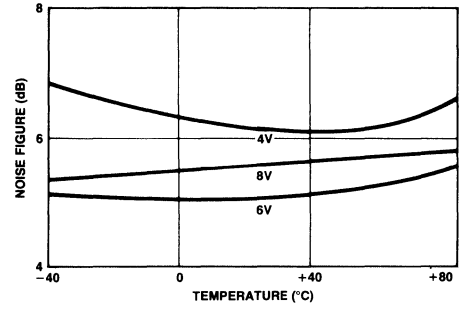


Figure 11.

Designing with the SA/NE604

AN199

INTRODUCTION

The SA/NE604 represents a new standard of performance in low power FM IF integrated circuits. Originally designed for cellular radio applications, the 604 is also well suited to other radio frequency circuits where good performance and low power consumption are the important design considerations. When used with its companion double-balanced mixer, the SA/NE602, a low power system solution for the cellular radio and other RF applications is realized. (Reference 1).

Figures 1 and 2 show the device pin-out and a functional diagram of the 604. The device provides an IF amplifier, quadrature detector, received signal strength indicator (RSSI), and mute circuit. Two detector outputs are provided for audio and data information with the audio output being controlled by the mute circuit.

CIRCUIT OVERVIEW

The IF amplifier consists of five differential stages with a total gain of about 90dB. Provision is made for an external inter-stage filter to reduce broadband noise and increase receiver selectivity. The differential input to the first IF section appears at pins 15 and 16. One pin is usually AC-coupled to ground (pin 15) with pin 16 used as the "high" input. The first IF section has a typical gain of 40dB with its output appearing on pin 14. Similar to the first IF section, the second section uses a differential input appearing at pins 12 and 11, with pin 11 usually AC-coupled to ground. The five stages are identical and any one may go into limiting, depending on the RF input level.

The interstage filter can be ceramic, crystal, or an LC circuit. RSSI tracking is optimized when the filter circuit loss is 6dB. The output impedance of both amplifier sections (pins 14 and 9) is about 1K ohms. For convenience, an "L" pad circuit showing 6dB loss is shown in Figure 3. This circuit allows observation of the RSSI response without using a filter.

The quadrature detector multiplies two IF signals to produce the audio output. One of the IF signals is differentially phase shifted by an external quadrature tank or discriminator circuit connected between pins 8 and 9 (Figure 4). The second IF signal is fed to the other detector input internally. Figure 5 shows the desired phase/frequency response of the quadrature-tuned circuit. A detailed mathematical explanation of detector operation can be found in Reference 2. The detected audio appears at the data terminal (pin 7) and, via the mute circuit, at the audio (pin 6) terminal.

The cellular radio specifications call for a logarithmic signal strength indicator accurate within 3dB over an 80dB dynamic range. The 604 meets this requirement with an effective technique. A sample current corresponding to the output of each IF stage is fed to a summing amplifier. The output of this amplifier provides a current source which is reflected by a current mirror. The current mirror output that appears on pin 5 provides the logarithmic RSSI information. It is usable over a 90dB dynamic range with 1.5dB accuracy. Typically, a 100K ohm resistor is used to convert the RSSI current to a voltage which is logarithmically proportional to the received signal strength.

PACKAGING

Both the SA/NE604 and its companion double balanced mixer, the SA/NE602, are available in either the plastic dual-in-line "DIP" or surface mounted "SO" packages. The NE prefix specifies a 0 to+70°C operating temperature range while SA specifies−40 to+85°C operation. The extensive temperature data presented in this application note pertain to both the SA and NE devices.

TYPICAL APPLICATIONS

Figure 6 is a simplified schematic diagram of the 604 which details the internal circuitry adjacent to the device's pins. This should help the designer match impedances to external circuitry. Figure 7 shows the schematic diagram of a typical test circuit using the 604 and 602.

The quadrature tuned circuit (F3) shifts the phase of the IF signal as shown in Figure 5. Low distortion demodulation is obtained if the IF signal deviation is restricted to the linear portion of the S-curve. There are three variables affecting quadrature linearity: circuit Q, deviation, and IF frequency. If the deviation is increased, the Q must be decreased for a given degree of linearity. The circuit Q will also affect the demodulated signal level. A higher Q will yield a higher audio output from the quadrature detector since the phase shift will be greater for a given deviation. The quadrature Q must be optimized for a given frequency deviation, IF frequency, and desired linearity. A loaded Q of about 20 is typical for narrow band FM applications using a 455kHz IF.

The supply voltage for the 602/604 pair can range from 4.5 to 8 volts. Optimum overall performance is realized at 6.0 volts for the device pair. Several operation parameters are plotted for supply voltage as well as temperature.

Quadrature detector linearity can be affected by temperature variations. LC circuit resonances will drift as the coil and capacitor values change with temperature. This effect becomes more critical with increased circuit Q. If wide temperature variations are expected, careful choice of circuit components can minimize this effect. Most inductors have positive temperature coefficients (increase of inductance with increase of temperature). If a negative coefficient capacitor is chosen to compensate the inductor, the resonant frequency will track over temperature.

Since a bipolar current source is used to provide the RSSI function, the current will change with temperature. An increase in temperature will result in an increase in RSSI indication (Figure 8, uncorrected response). The circuit shown in Figure 9 will "smooth" the response over temperature by dropping the load impedance presented to pin 5 as temperature increases (Figure 8, corrected response).

All the major performance parameters of the 604 are shown in Figure 10. Figure 11 illustrates a typical test set-up for measuring many of the discussed parameters. Figures 12 to 25 provide a comprehensive guide to 604 performance over temperature and other variables.

USE AS A FIELD STRENGTH/ RF VOLTMETER

As stated earlier the RSSI function is usable over a 90dB dynamic range. This function taken alone can provide a useful RF voltmeter function. The circuit in Figure 26 can be used as a field strength or RF voltmeter application. A linear readout device can be calibrated directly in decibels or logarithmically for power, current, or volts.

USE AS AN AM SYNCHRONOUS DETECTOR

The 604 can also be used as an AM envelope detector. The IF signal is fed to both the 604,

as in the FM application, and to an additional linear IF amplifier (Figure 27). The linear amplifier then feeds the quadrature detector which mixes with the AM limited carrier and demodulates the envelope. 1% THD is obtainable with this technique with a 90% AM modulated signal.

USE AS A PRODUCT DETECTOR

Figure 28 shows how the 604 can be used as a product detector for SSB or DSB. In this case the LO is applied to the 604 IF amplifier and an external linear IF amplifier is used for the SSB or DSB signal. The 604 quadrature detector then acts as the product detector. With the addition of a simple switching array, a single 604 can be used for FM, AM, or SSB detection in a communications receiver!

REFERENCES

1. Zavrel, R.: Signetics AN198 *Designing With the SA/NE 602*, December, 1984.

2. Hayward, W.: *Introduction to Radio Frequency Design*, 1982, Prentice-Hall.

Written by Bob Zavrel

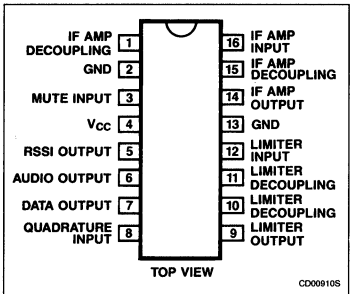


Figure 1. Pin Configuration

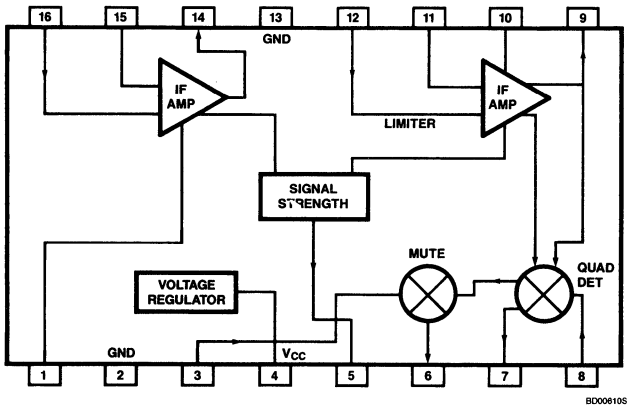


Figure 2. Block Diagram

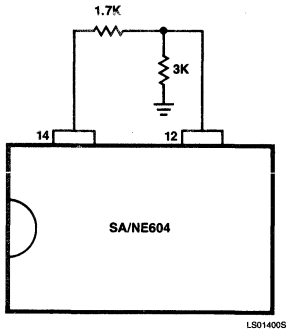


Figure 3. 6dB "L" Pad

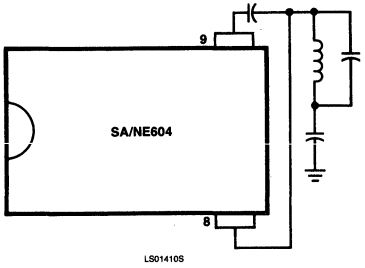


Figure 4. Quadrature Network

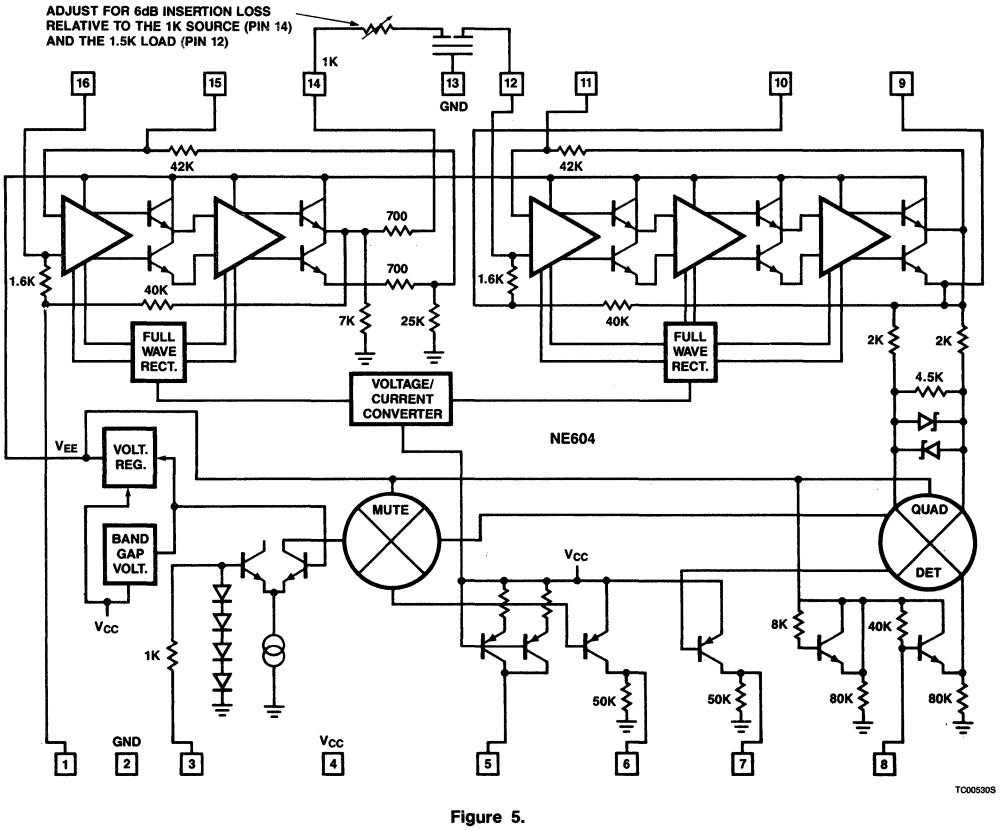


Figure 5.

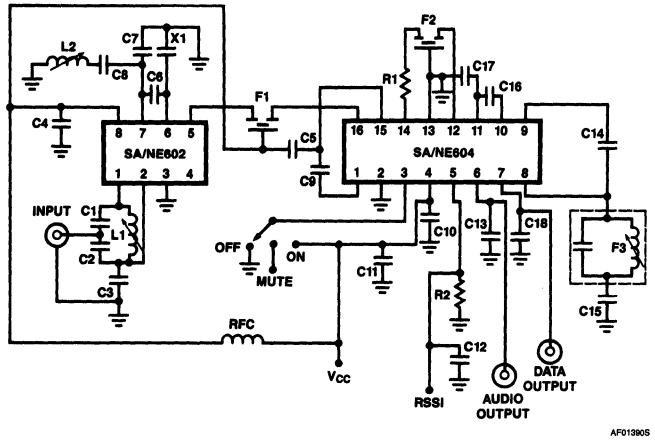
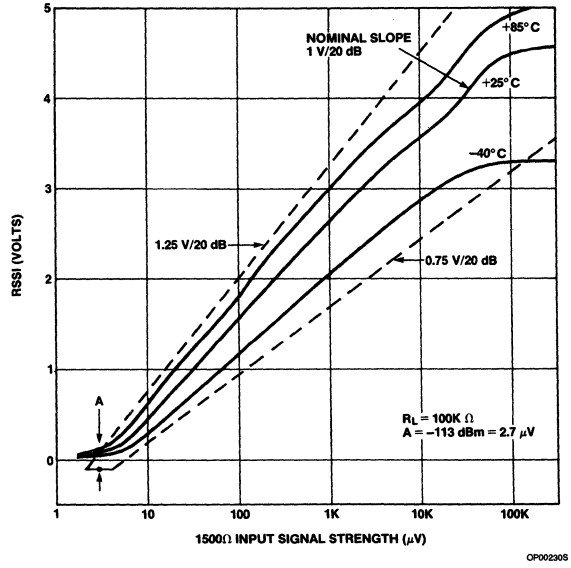


Figure 6. Application Demonstration Board

C1	47 pF ± 2%	100 V	N750 Ceramic
C2	220 pF ± 2%	100 V	N750 Ceramic
C3	0.1 μF ± 10%	50 V	Polyester
C4	10 nF ± 80% 20%	63 V	K10000 — 25X Ceramic
C5	0.1 μF ± 10%	50 V	Polyester
C6	5.6 pF ± 25%	100 V	NPO Ceramic
C7	22 pF ± 2%	100 V	N150 Ceramic
C8	1 nF ± 10%	100 V	K2000 — Y5P Ceramic
C9	0.1 μF ± 10%	50 V	Polyester
C10	0.1 μF ± 10%	50 V	Polyester
C11	6.8 μF ± 20%	25 V	Tantalum
C12	1 nF ± 10%	100 V	K2000 — Y5P Ceramic
C13	15 nF ± 10%	50 V	Polyester
C14	10 pF ± 2%	100 V	NPO Ceramic
C15	0.1 μF ± 10%	50 V	Polyester
C16	0.1 μF ± 10%	50 V	Polyester
C17	0.1 μF ± 10%	50 V	Polyester
C18	150 pF ± 2%	100 V	N1500 Ceramic
R1	1.5 K ± 5%	1/8 W	Carbon Composition
R2	100 K ± 1%	1/4 W	Metal Film
RFC	5.5 μH		RF Chocke J.W. Miller 542 — 4609
L1	0.209 — 0.283 μH		Adjustable VHF Coil Miller 48A257MPC
L2	0.5 — 1.3 μH		Adjustable Coil 1811 — 0036TW
F1	455 kHz		Ceramic Filter Murata SFG 455A3
F2			
F3	455 kHz		IF Filter Toko A2549
X1	44.545 MHz		Third Overtone Crystal

TB00440S

Figure 7. Application Test Board Parts



OP00230S

Figure 8. RSSI vs. Signal Strength

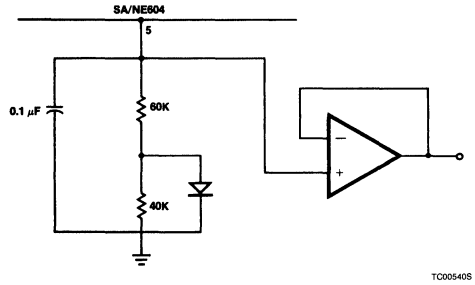


Figure 9. Temperature Compensated RSSI Circuit

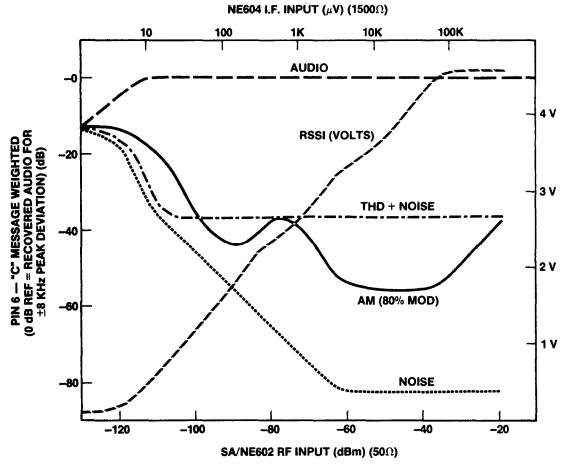


Figure 10. NE602/604 System Performance

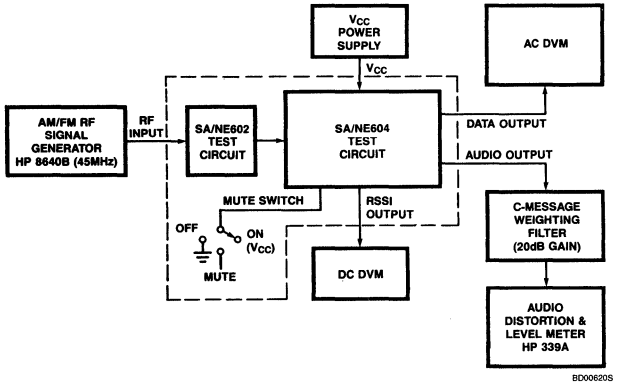


Figure 11. SA/NE602/SA/NE604 Applications Board

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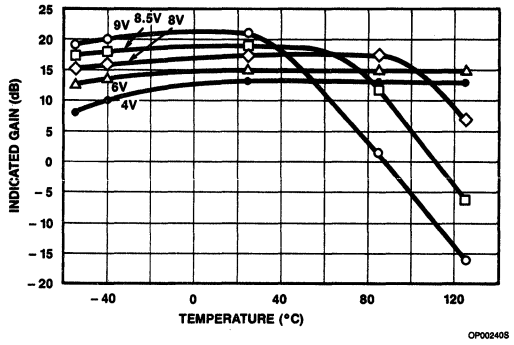

Figure 12. SA/NE604 Indicated Gain vs Temperature and Voltage

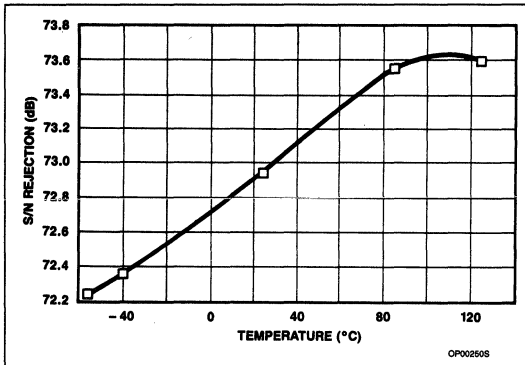

Figure 13. SA/NE604 Signal-To-Noise Ratio vs Temperature

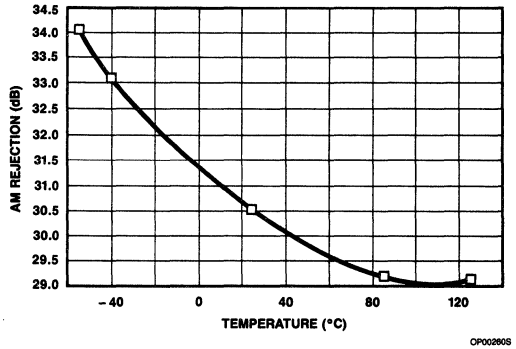

Figure 14. SA/NE604 AM Rejection vs Temperature

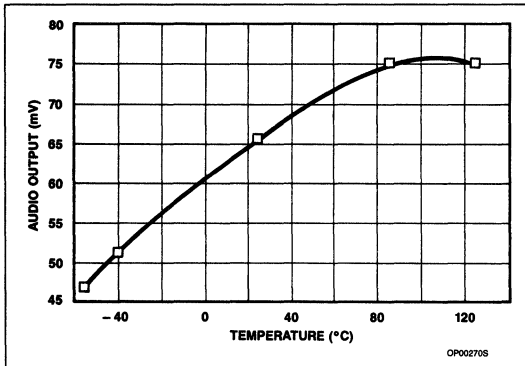

Figure 15. SA/NE604 Audio Output vs Temperature

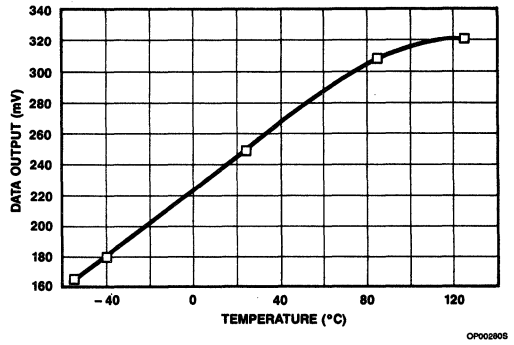

Figure 16. SA/NE604 Data Output vs Temperature

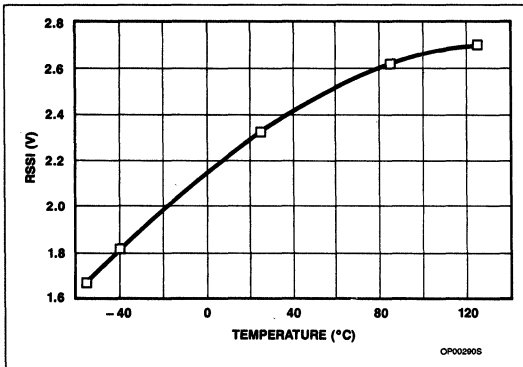

Figure 17. RSSI vs Temperature

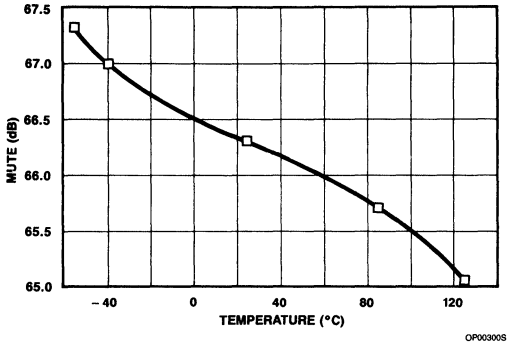

Figure 18. SA/NE604 Muting vs Temperature

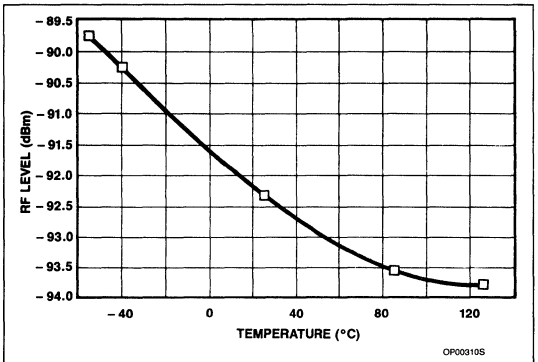

Figure 19. SA/NE604 Limiting RF Level vs Temperature

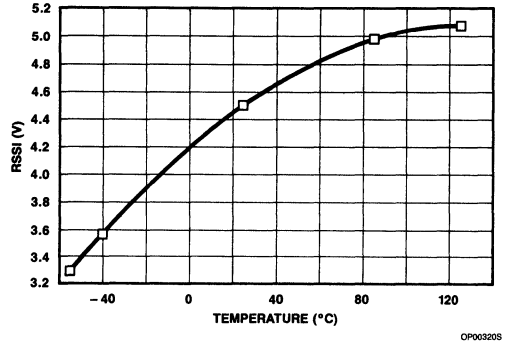

Figure 20. SA/NE604 Large Signal Uncompensated RSSI Voltage vs Temperature

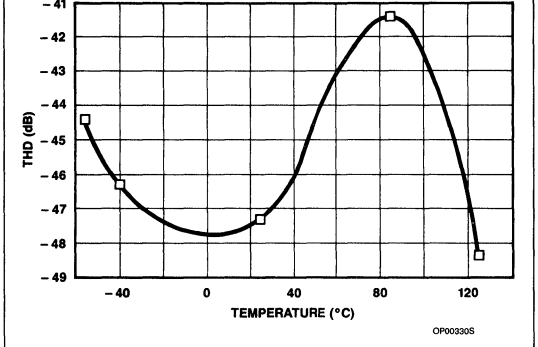

Figure 21. SA/NE604 Total Harmonic Distortion vs Temperature

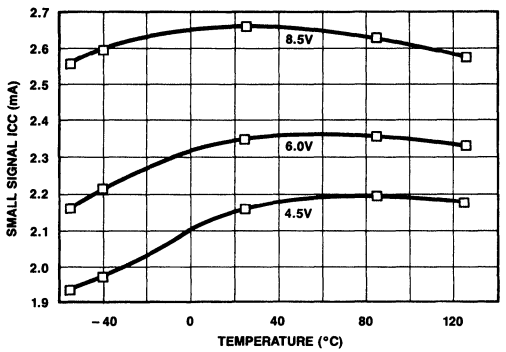

Figure 22. SA/NE604 Supply Current vs Temperature and Voltage

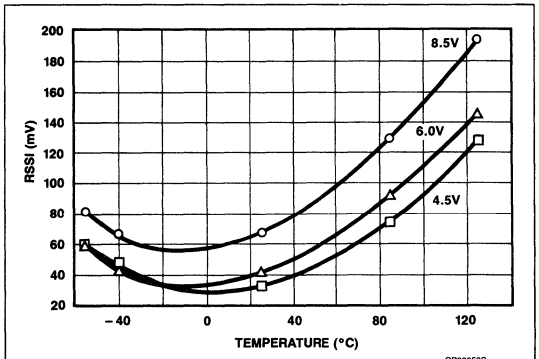

Figure 23. Small Signal RSSI vs Temperature and Voltage

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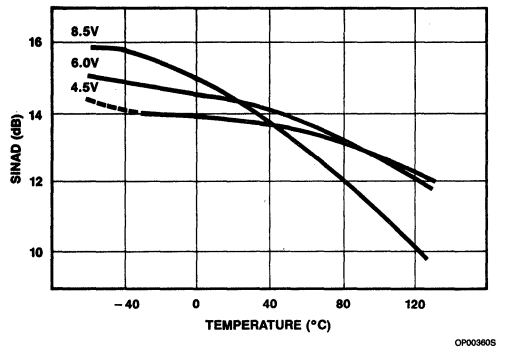


Figure 24. SA/NE604 SINAD vs Temperature and V_{CC}

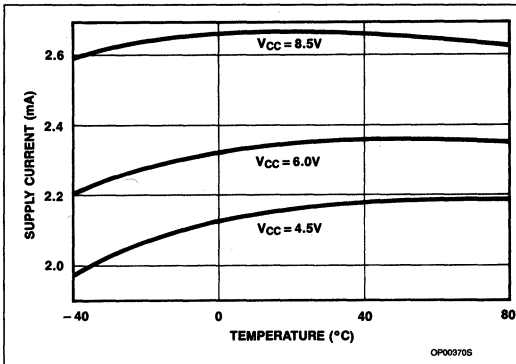


Figure 25. SA604 Supply Current vs Temperature

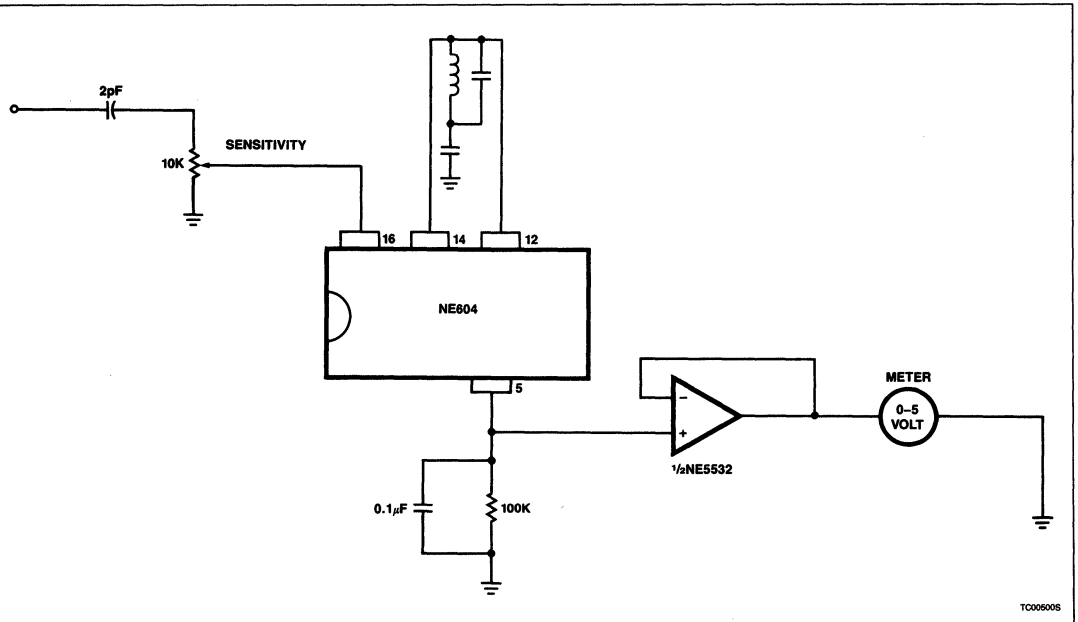


Figure 26. Field Strength Meter

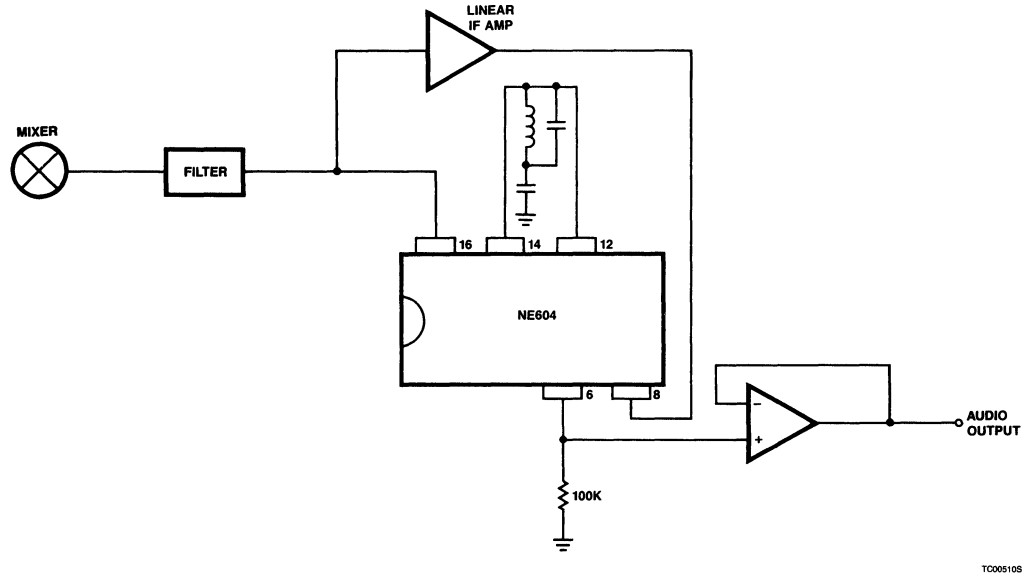


Figure 27. AM Synchronous Detector

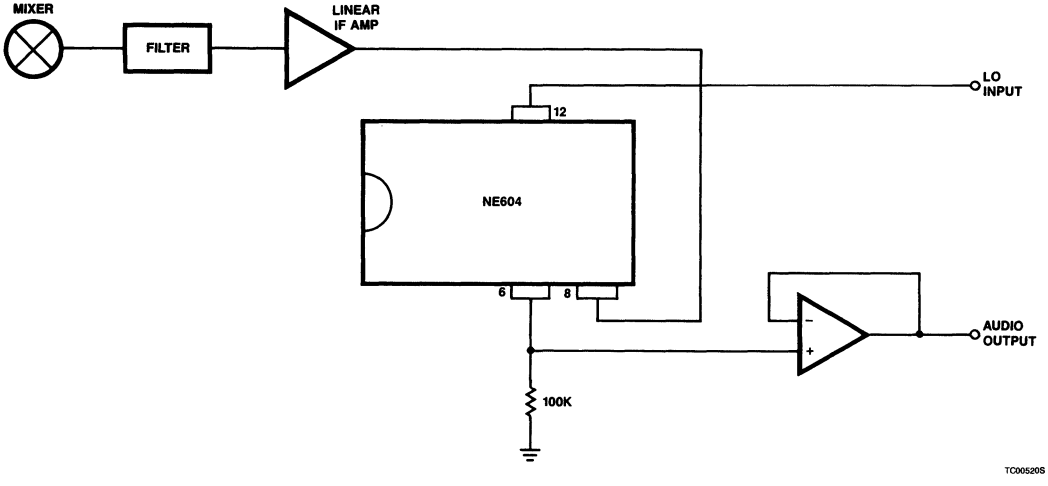


Figure 28. Product Detector

ICs for Compact Audio Disc Decoders AN200

J. MATULL

One side of a 12 cm Compact Disc stores an hour of stereo music in the form of a helical track of tiny pits and flats representing more than five billion data bits. During playback, the pits scatter the light from a small semiconductor laser, the flats reflect it onto a photodetector. The data bits are recovered at a rate of 4.3 million bits/s and converted into a PCM signal from which the original audio waveform is accurately reconstructed without the degradation associated with analogue reproduction systems.

The change to digital signal processing leaves all analogue problems such as wow and flutter and crosstalk behind. Owners of a Compact Disc player will therefore be able to enjoy music of a quality unequalled by that available from disc or tape. Compact Disc players can be programmed to access individual pieces of music and reproduce them in any order desired by the listener. Some other possible features, not easily implemented in a conventional LP disc system, are the display of elapsed/remaining playing time, automatic switching of de-emphasis circuits and search and repeat functions.

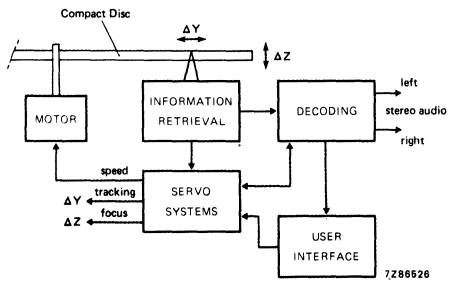
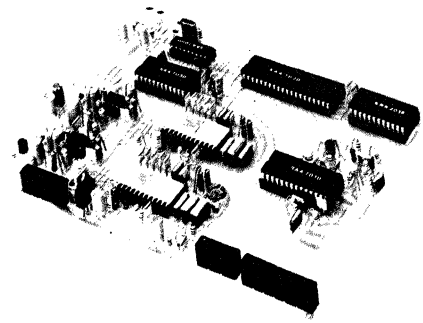


Fig.1 Functional schematic of a Compact Disc player.



Development decoder board which performs more than 4 million decoding, control and error-correction operations every second of playback of a Compact Disc. The four new NMOS LSI circuits at the heart of this mammoth processing task enable a complete decoder controlled by one master clock to be assembled on one small single-sided board (≈220 cm²)

Figure 1 shows the main components of a Compact Disc player. This article describes the decoding section for which four new NMOS LSI circuits have been developed:

- SAA7010, demodulator IC (28-pin DIL).
- SAA7020, error correction IC (40-pin DIL).
- SAA7000, interpolation and muting IC (18-pin DIL).
- SAA7030, digital oversampling filter IC (24-pin DIL) used with the TDA1540 DAC (28-pin DIL) in a unique 16-bit digital-to-analogue conversion system.

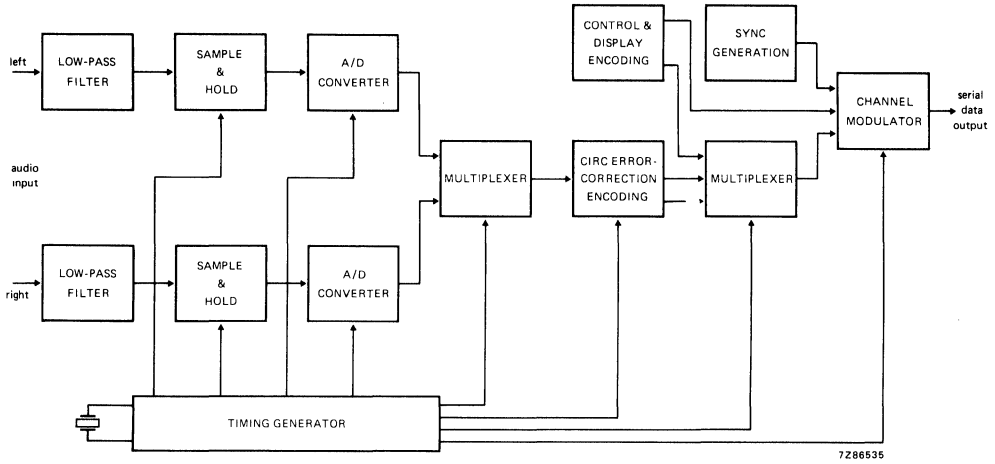


Fig.2 Compact Disc encoding system

These circuits are in standard DIL packages, require only a few peripheral components and are controlled by one master clock. Because of a high degree of integration, a complete decoder from h.f. input to audio output can be built on one small (≈220 cm²) single-sided printed circuit board.

The ICs are key components determining the performance of a Compact Disc player. Before describing them and the decoding process, it will be helpful to describe briefly the digitising and encoding of audio signals onto a Compact Disc. Figure 2 shows the encoding process.

ENCODING THE DIGITAL AUDIO

The first step is to sample the analogue audio and convert the samples to 16-bit PCM signals. Since the frequency spectrum of impulse-sampled audio signals is simply double sidebands of the audio signal spectrum repeated at multiples of the sampling frequency, the analogue input signals are first passed through a low-pass filter with sharp cut-off which limits their bandwidth to less than half the sampling frequency. This prevents intermodulation distortion due to aliasing. If required, the filtered analogue signals can be passed through a pre-emphasis network to improve signal-to-noise ratio (SNR).

The analogue signals are sampled at 44.1 kHz. The output of the sample and hold circuit is a flat-top PAM signal, whose pulse heights correspond to the audio signal amplitudes at the sampling instants.

Each sample is held long enough for the previous one to be converted to a 16-bit 2's complement number by an analogue-to-digital converter (ADC). Sixteen-bit quantisation gives extremely high resolution, the maximum SNR of a 16-bit PCM signal being ≈98 dB (6n + 1.8 dB, where n is the number of bits used to express each quantisation level).

Channel separation in Compact Disc digital audio is almost total, because the data of the left channel are completely independent of those of the right.

The 16-bit binary words from the ADC go to a multiplexer which sends a serial data stream of alternately 16 left channel bits and 16 right channel bits to an error-correction encoder.

Sixteen-bit quantisation solves one problem associated with any digital audio system – quantisation noise. Another – drop-out (the loss of single or several data bits in the recovered data) – is overcome in the Compact Disc system by the method used for encoding the digital data prior to recording the Disc. This enables any errors in the signal read from a Compact Disc, which could cause distortion, to be detected and corrected during playback. A powerful multiple-error-correcting code called the Cross Interleave Reed-Solomon Code (CIRC) is used. This code is based on parity bits and an interleaving (rearranging) of the digital audio samples in time.

This code can correct a drop-out in which up to about 3500 successive bits are lost (equivalent to a track length on the disc of about 2.4 mm). Beyond this, it enables the loss of up to about 12 000 bits, occupying a track length of 8.5 mm, to be compensated by interpolation. This, plus the track being beneath a protective layer, is why a Compact Disc is insensitive to scratches and dirt on its surface.

Figure 3 shows the principle of interleaving. In Fig.3(a), a sequence of signal processing events is shown without interleaving. An audio signal is sampled at instants 1, 2, 3 etc., digitised and the data representing the samples recorded onto disc. If there is a drop-out while reading the disc, some words will be missing in the received data. In Fig.3(a), three

words are missing. If the length of the drop-out region is greater than the error correction ability of the decoder, the missing values cannot be reconstructed and the audio output has to be muted in order to avoid audible clicks in the reproduced sound.

In Fig.3(b), the same sequence of events is shown, this time with interleaving of data. The original audio signal is sampled, but the sequence of the samples is then rearranged prior to recording on disc. For the same drop-out as before, three words are again missing. After the original sequence of the data words is restored, the drop-out region is spread out in time, but now there are only single errors (dashed lines) which can be easily corrected.

The Compact Disc system enables many features, not possible with the microgroove record system, to be incorporated in the new players. For example, signals can be added to mark the pause between two successive pieces of music and used to implement search and repeat functions, or to indicate remaining/elapsed playing time, titles and composers. This control and display information (known as subcoding information) must be inaudible and so is encoded separately by the control and display encoder. The 8-bit output of this encoder means eight information channels can be recorded. Since the subcoding information is generated and recorded bit-serially, there must be provision for recognising the beginning of a block of subcoding data. There are two outputs from the encoder, one carrying the data, the other synchronising the data blocks.

The subcoding data and the 8-bit serial words from the error correction and encoding unit, which are either data or parity words, pass through a multiplexer to the channel modulator. The sync generator creates a unique pattern, not contained in the normal data, which identifies the beginning of each frame of data.

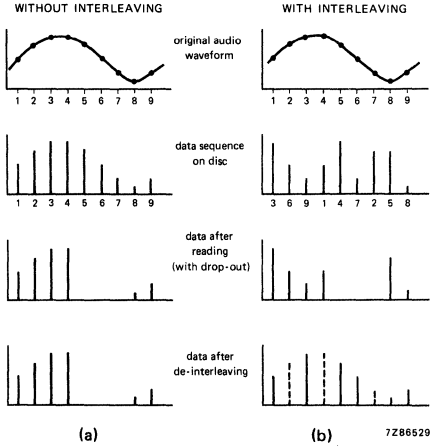


Fig.3 Principle of interleaving

The output data of both the error correction encoding unit and the control and display encoding unit are in non-return-to-zero (NRZ) format. Data in NRZ format are not suitable for recording onto disc, because the bit clock cannot be recovered from the data stream during playback. In addition, the data stream may contain low-frequency components which could interfere with the servo systems in the player, controlling the disc rotation and the tracking/focusing of the laser pick-up. The NRZ data is converted to another code in the channel modulator, whose output is then recorded on disc.

The requirements of a code for an optical audio disc system are:

- bit clock can be regenerated from the data
- low spectral power at low frequencies
- permits read-out at high information density
- small error propagation.

The encoding procedure used is called Eight-to-Fourteen Modulation (EFM). As the name implies, each group of 8 data bits (called a symbol) from the error correction encoder, or from the control and display encoding unit, is encoded into a group of 14 bits. To ensure that the bit clock can be regenerated from the data, and to permit the reading of high-density information, there are always at least two 0s between successive 1s and no more than ten consecutive 0s in a 14-bit EFM word. The transmitted information is contained in the transitions which are indicated by the 1s. There are 277 combinations of 14 bits which satisfy the constraint of at least two 0s. Deleting the 21 patterns with ten or more 0s in a row leaves 256 combinations, which gives a one-to-one correspondence between 8-bit NRZ data and 14-bit EFM data. Code conversion can therefore be done easily, via a T flip-flop, using a look-up table stored in a ROM.

The 14-bit blocks generated cannot, however, be concatenated without violating the constraint of the two to ten 0s at the block boundaries. Therefore, three merging bits are inserted between successive 14-bit blocks. These bits do not contain audio or control/display information and are skipped by the decoder. The d.c. content of the bit stream can be controlled by inserting a transition in the merging bits, if the constraints are not violated. The decision to insert is made using advance knowledge of symbols.

Because of the requirement for regenerating the bit clock, synchronisation is necessary. This is achieved by dividing the bit stream into frames and adding a unique pattern to each. Each frame contains:

- a synchronisation pattern
- twelve 16-bit data words representing 6 stereo samples
- four 16-bit error correction parity words
- one 8-bit control and display word.

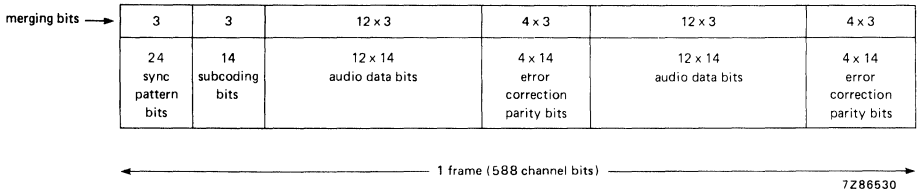


Fig.4 Data stream after Eight-to-Fourteen Modulation (EFM)

The 16-bit data and parity words are split into 8-bit words before EFM encoding.

The total number of channel bits per frame after encoding is 588, comprising:

- 24 sync pattern bits
- 336 (12 x 2 x 14) data bits
- 112 (4 x 2 x 14) error correction bits
- 14 control and display bits
- 102 (34 x 3) merging and d.c. control bits.

Figure 4 shows the arrangement of the bit stream after EFM.

Since EFM is based upon a block structure of 8-bit input data, it is well suited for the CIRC error correction system, also based on blocks of eight consecutive data bits. Propagation of errors is limited to the eight bits in a symbol.

DECODER

The function of the decoding system of a Compact Disc player is to regenerate both analogue audio channels from the h.f. data stream retrieved from the disc by the laser pick-up. Figure 5 shows the block diagram of a decoder and the ICs used:

- SAA7010, for the signal processing tasks of demodulation. Converts the data stream from the laser pick-up back to its original format, regenerates the bit clock from the data stream, and separates the data representing the recorded sound from control and display data.
- SAA7020 and an SBB2016 RAM.
  De-interleave the demodulated data from the SAA7010, and detect and correct errors in the data stream. The SAA7020 generates an unreliable data signal if it is unable to correct an error. The SAA7020 also removes jitter in the data by resynchronising the data to a clock derived from a crystal oscillator.
- SAA7000, for interpolation and muting.
  Reconstructs audio data by interpolation should the SAA7020 be unable to correct any single samples in error; mutes consecutive erroneous samples.
- SAA7030 and two TDA1540s for digital-to-analogue conversion. SAA7030 increases the SNR of the 16-bit data stream containing the audio information by 13 dB so that 14-bit DACs can be used with no loss of quality in the reproduced audio.

Figure 6 shows the demodulation, error correction and muting section of the decoder in more detail. Figure 8 shows the 16-bit digital-to-analogue conversion section.

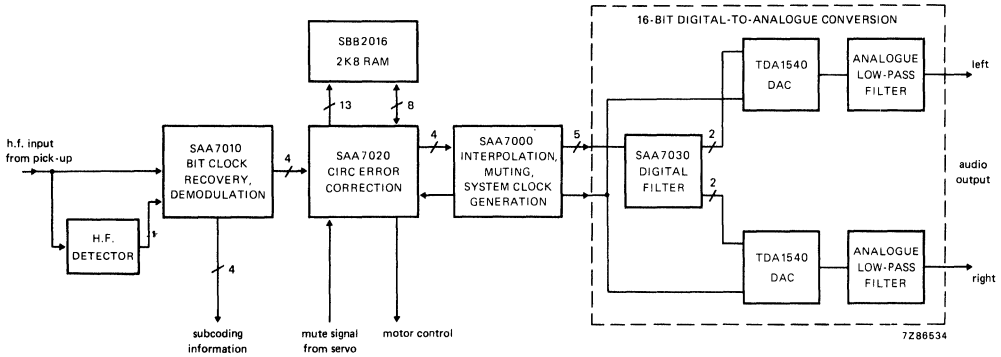


Fig.5 Block diagram of a Compact Disc decoder

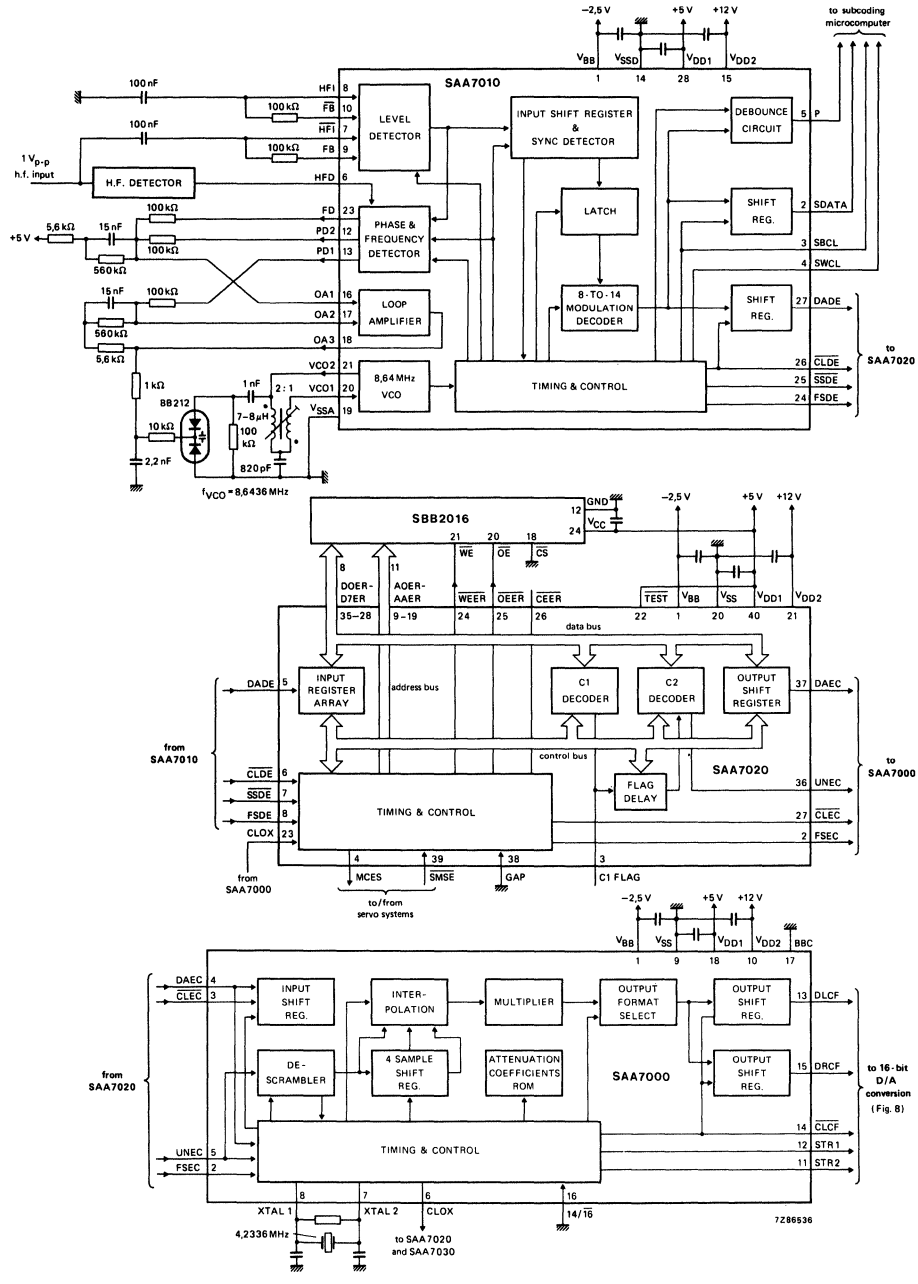


Fig.6 Demodulation, error correction and muting section of a Compact Disc decoder

SAA7010: demodulator IC

The SAA7010 forms the front-end of the decoding system and supplies demodulated data and timing signals to the error correction IC (SAA7020) and to the subcoding microcomputer.

The h.f. signal read from the Compact Disc by the laser pick-up is first amplified and filtered, then supplied to the input of the SAA7010 and to an optional h.f. threshold detector. The analogue h.f. signal is first digitised by a level detector and then passed to a phase-locked loop (PLL) which regenerates the bit clock from the incoming data.

There are six complete stereo audio samples in one frame (588 EFM channel bits) of the disc data. Therefore, one stereo sample comprises 98 channel bits. For a sampling frequency of 44.1 kHz, the data rate of the h.f. signal is 4.3218 Mbits/s. The voltage-controlled oscillator (VCO) of the PLL operates at twice the incoming data rate from which a 4.3218 MHz master clock signal used in all internal timing is derived. Frequency-sensitive and phase-sensitive detectors provide the coarse and fine tuning signals for the VCO. Both detectors are enabled/disabled using the HFD input.

The incoming data is clocked into a shift register and the sync pattern detected, which enables the start of each frame of data to be identified. Sync information is passed to the timing and control logic in order to synchronise the demodulation with the incoming data. The level detector has feedback which automatically adjusts to the optimum switching level. However, if the frequency of the incoming data falls below a set level, e.g. owing to a drop-out, the level detector switches to a nominal feedback level of half the supply voltage V_{DD1}. This prevents the switching level drifting away from its optimum.

Provided the timing generator is locked to the h.f. signal, each 14-bit word received is stored in a latch, then converted into an 8-bit word by the EFM decoder.

In the SAA7010, a logic array is used for code conversion, not a ROM look-up table as mentioned earlier. This saves chip area and reduces power dissipation.

Demodulated audio data are shifted out of the SAA7010 to the error correction IC SAA7020 on DADE, with the clock signal $\overline{\text{CLDE}}$ and the symbol and frame sync signals $\overline{\text{SSDE}}$ and FSDE respectively.

The seven bits Q to W of the subcoding data plus a sync bit are shifted out serially at the SDATA output with clock SBCL and sync signal SWCL, while channel P (pause bit) is output at P after passing through a debounce circuit.

Note, use of an h.f. threshold detector at the input HFD of the SAA7010 is optional. If one is not used, the HFD input is connected to V_{DD1} for normal operation of the demodulator. Using an h.f. detector can improve the performance of a Compact Disc player because it disables the phase and frequency detectors in the demodulator when the amplitude of the h.f. input is small. Thus, the PLL cannot lock onto noise in the absence of an h.f. signal and so clock jitter is prevented.

SAA7020: error correction IC

The SAA7020 detects, and where possible corrects, errors in the demodulated data stream and supplies these data together with a flag, indicating whether the data are correct or unreliable, to the SAA7000.

Data from the SAA7010 are arranged in frames of thirty-two 8-bit symbols. Twenty-four of these symbols contain 12 audio samples (i.e. 6 stereo samples), the remaining eight are parity symbols added for error detection and correction.

Data enter serially into a register array at DADE. This array comprises a shift register which accumulates symbols for parallel processing and a FIFO register which acts as a jitter reduction circuit. The FIFO register can compensate for deviation of up to ±2.25 frames from the nominal data rate. It is this register that eliminates wow and flutter in the Compact Disc system. The output data rate from the SAA7020 depends only on the clock signal CLOX derived from a crystal oscillator. Any discrepancy between the clock derived in the demodulator and that from the crystal oscillator generates an error signal MCES which controls the speed of the motor spinning the disc. MCES is a PWM signal with a range of 142 linear steps.

The CIRC makes use of interleaving and two Reed-Solomon codes C1 and C2. The data from the demodulator are de-interleaved by temporarily storing the thirty-two 8-bit symbols forming the input word of the C1 decoder and the output word of this decoder in a 2K8 RAM.

An 8-bit bidirectional bus is used for transferring data to and from the RAM, an 11-bit bus for addressing. Three bits control the RAM: write enable $\overline{\text{WEER}}$, output enable $\overline{\text{OEER}}$, and chip enable $\overline{\text{CEER}}$. The last is for operation with pseudo-static RAMs.

The C1 decoder of the SAA7020 is designed to correct one erroneous symbol in a 32-symbol frame. The C2 decoder is designed to correct one erroneous symbol, or two erasures in a group of 28 symbols.

The input word to the C1 decoder is checked for errors by multiplying this word with the C1 parity check matrix. This produces four syndromes. If there are no errors in the input word, all four syndromes are equal to zero and the 28 data symbols at the output of the C1 decoder (4 parity symbols being discarded) are written back into the RAM unchanged. In case of one erroneous symbol, this is corrected and the 28 corrected output symbols are written into the RAM. In case of two or more erroneous symbols, the 28 output symbols are written into the RAM unchanged and a flag is set which marks these 28 symbols as unreliable.

Since each symbol in a C1 output word is delayed by a different amount before reaching the C2 decoder, the C1 flag of each unreliable symbol is delayed by the same amount as the symbol to ensure that symbol and flag arrive at the input of the C2 decoder together.

The output symbols of the C1 decoder are de-interleaved further by means of the RAM. Then, the 28 symbols

forming the input word of the C2 decoder are also checked for errors by examining the four syndromes resulting from multiplication of this word with the C2 decoder parity check matrix.

If there are no errors, all four syndromes are equal to zero, and the 24 data symbols at the output of the C2 decoder are written back into the RAM unchanged and the remaining four parity symbols discarded.

In case of one erroneous symbol, this symbol is corrected in the same way as for the C1 decoder. Then, the corrected 24 output symbols are written into the RAM. In case of two erroneous symbols, the sum of the error values is given by one of the syndromes. Information about the position of erasure symbols is given by the flags. With this additional information, both symbols can be corrected and the 24 corrected output symbols are written back into the RAM. In case of more than two erroneous symbols in a C2 word, all 24 symbols are rewritten into the RAM unchanged and a C2 flag is set which marks these 24 symbols as unreliable.

Data from the SAA7020 are output on DAEC in 16-bit bursts separated by 8-bit intervals. If the unreliable data signal UNEC is output simultaneously with a data symbol, it marks that symbol as unreliable. If UNEC is output during the interval between data bursts, it indicates that the sample arriving 30 sampling periods later is unreliable. This advance information of the reliability of symbols is used in the SAA7000 in a muting procedure.

The unreliable data signal is generated when:

- both C1 and C2 decoders detect an uncorrectable error pattern. In this case, UNEC marks one or more symbols of the C2 output data as unreliable.
- C1 fails to detect an error, but C2 detects it without being able to correct all erroneous symbols. In this case, the whole C2 output frame is marked unreliable.
- a mute signal $\overline{\text{SMSE}}$ is received from the servo system. UNEC is immediately activated and marks symbols as unreliable as long as $\overline{\text{SMSE}}$ is present.

The output data are shifted out serially with the data clock $\overline{\text{CLEC}}$ and the frame sync signal FSEC. The logic state of DAEC in the gaps between successive clock bursts, which is determined by the input GAP, is used to select 2's complement or offset binary format for the SAA7000.

The 8-bit input and output data format of the SAA7020 makes it also suitable for error correction in other applications.

CIRC decoding

Use of error correction is one of the fundamental reasons why digital audio is vastly superior to analogue audio. And from a practical point of view, the ability to correct errors means that the requirements for disc manufacture are not pushed to impossible limits.

A very powerful error-correcting code called the Cross Interleave Reed-Solomon Code is used in the Compact Disc system. This code, which is based on the use of parity bits and an interleaving of the digital audio samples, enables an error burst of up to about 3500 bits to be corrected. Beyond this, it enables a loss of up to about 12 000 bits to be compensated by interpolation. In systems not using interleaving, a drop-out means that several adjacent samples are lost, leaving no chance of reconstructing them.

Two Reed-Solomon Codes termed C1 and C2 are used for correcting erroneous audio samples. C1 is characterised by thirty-two 8-bit symbols, comprising 28 data symbols and 4 parity symbols. C2 is characterised by twenty-eight 8-bit symbols, comprising 24 data symbols and 4 parity symbols. The minimum distance of each code, i.e. the Hamming distance at symbol level, is five. Thus, in theory, 2 symbols in error, or four erasures (symbols whose position is known but whose value is not) can be corrected.

Figure 7 shows the principle of a CIRC decoder. Delays are used to rearrange (de-interleave) the digital samples back to their original sequence and are organised for efficient error correction.

Delays at the input of the C1 decoder are all of equal length and separate the even and odd numbered symbols. This enables the C1 decoder to correct small errors in adjoining symbols. Delays between the two decoders are of unequal length and longer than those at the input of the C1 decoder which enables the C2 decoder to correct burst errors.

The input to the C1 decoder is a frame of 32 symbols which is multiplied by the C1 parity check matrix to produce four syndromes. From the syndromes, errors can be detected and corrected. The C1 decoder of the SAA7020 is designed to fully correct one erroneous symbol out of a 32-symbol frame. If there is more than one error, each of the 28 output symbols (the four C1 parity symbols having been dropped) is marked with a flag, indicating that each may contain an error. If there is no flag associated with a symbol arriving at the C2 decoder, that symbol is correct.

The C2 decoder is designed to correct one erroneous symbol, or two erasures. When even the C2 decoder cannot correct all errors, it outputs the 24 data symbols (the four C2 parity symbols having been dropped) uncorrected, but marked with flags. Most of these output symbols are usually error-free and can be reconstructed by linear interpolation, because the combination of the C1 and C2 flags is used as an unreliable data signal for interpolation, or if necessary, muting of symbols in the SAA7000.

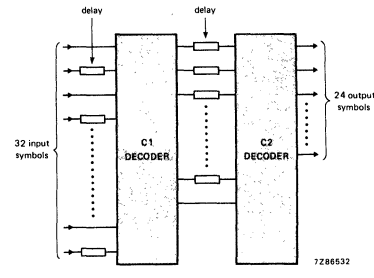


Fig.7 Principle of a CIRC decoder

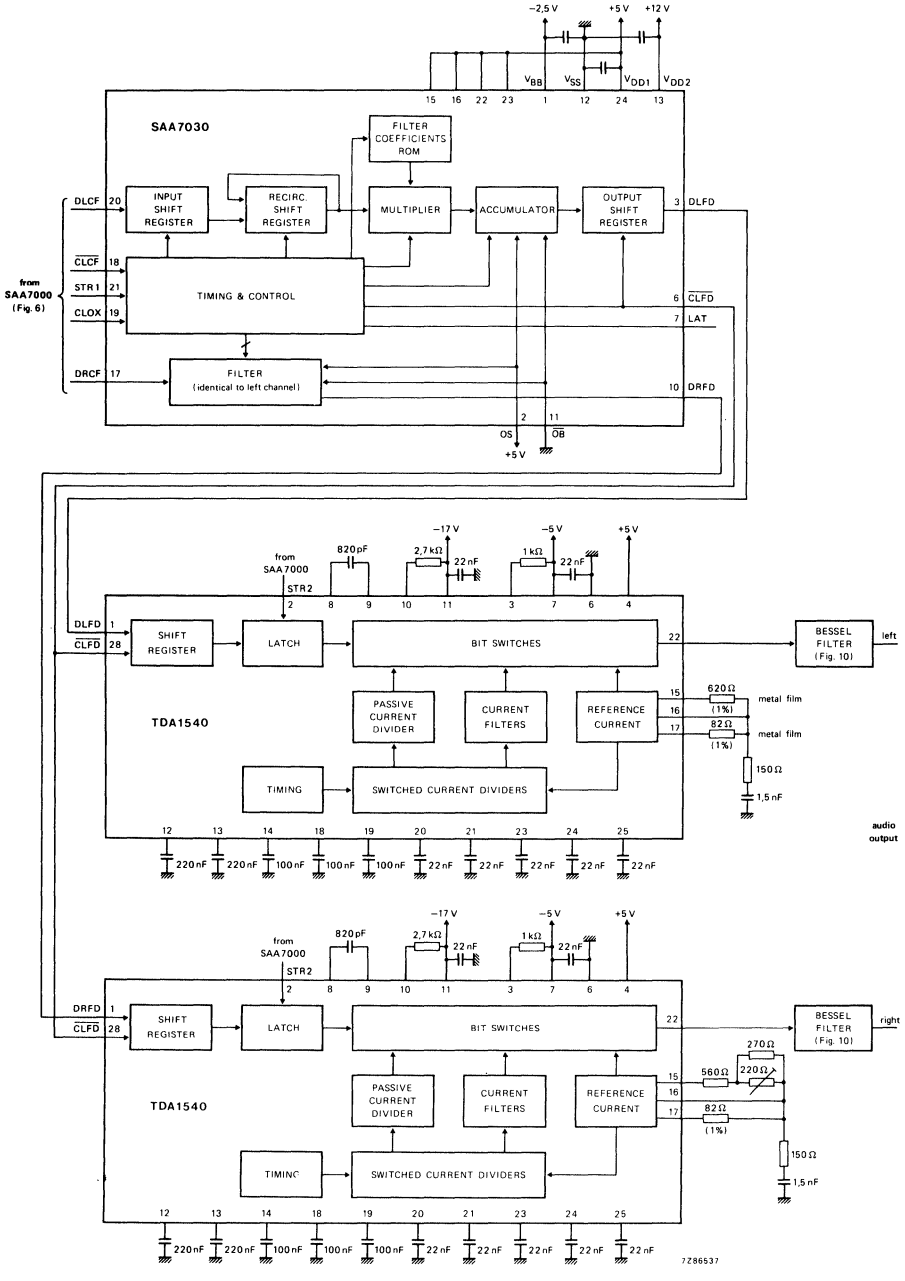


Fig.8 16-bit digital-to-analogue conversion section of a Compact Disc decoder

SAA7000: interpolation and muting IC

The SAA7000 eliminates the audible annoyance that could result if an erroneous symbol which managed to get through the error correction circuitry was processed further. The SAA7000 also generates the clock used for internal timing of the SAA7020 and SAA7030.

Serial data from the SAA7020 on DAEC are entered into a shift register using the clock $\overline{\text{CLEC}}$. Data are then descrambled and separated into left and right channel samples. A similar descrambling and separation is performed on the unreliable data flag UNEC. When there are no unreliable data flags, the data values of the audio samples are unaffected by the SAA7000.

When, for either left or right channel, a single unreliable sample is flagged between two correct samples, linear interpolation is used to replace the erroneous sample. If two or more adjacent samples are flagged as unreliable, they are muted. Starting thirty samples before muting (by making use of the advance information of UNEC), the correct samples are attenuated smoothly to zero according to a cosine curve. The levels of the first thirty samples following muting are then increased back to the normal level, again according to a cosine curve. The thirty-sample (5-frame) delay necessary in muting is obtained using the 2K8 RAM.

The data which are now either correct or processed are converted into 2's complement or offset binary depending on the digital-to-analogue converters used. Selection is made by the status of DAEC during the intervals between input samples which is controlled by the GAP input of the SAA7020. Left and right channel output data on DLCF and DRCF are clocked out by the shift clock $\overline{\text{CLCF}}$. Strobe signals STR1 and STR2 are generated for the digital-to-analogue conversion unit. A 14-bit or 16-bit output data format can be selected using the input $14/\overline{16}$. A full-performance 16-bit conversion system is described in the next section.

A crystal oscillator is used to generate internal timing signals and the clock signal CLOX for the SAA7020 and the SAA7030. By using the frame sync signal FSEC to reset the internal timing, the SAA7000 is automatically synchronised with the output of the SAA7020.

16-bit digital-to-analogue conversion

The digital-to-analogue conversion section (Fig.8) converts the digital output data from the interpolation and muting IC to analogue voltages and removes all unwanted frequency components above the audio band.

This conversion system is an outstanding feature of the Compact Disc decoder. It is based on a digital oversampling filter (SAA7030) followed by two (one for each channel) 14-bit DACs (TDA1540) and low-order analogue filters. This arrangement has the SNR of a system using 16-bit DACs and high-order filters, plus the following advantages over that approach:

- linear phase response in the audio band (0–20 kHz)
- reduced slew rate distortion
- requires only a 14-bit DAC
- less intermodulation distortion, because the oversampling frequency moves any intermodulation products well outside the audio band
- only a simple low-cost analogue filter is needed after the DAC to suppress any residual frequency components not removed by the digital filter.

SAA7030: digital oversampling filter IC

The SAA7030 consists of three main parts: oversampling section, transversal filter, and noise shaper. Circuitry in the SAA7030 is duplicated, one for each channel.

The two 16-bit data streams, at DLCF and DRCF are fed into shift registers which quadruple the sampling frequency from 44.1 kHz up to 176.4 kHz. Quadrupling the sampling frequency also quadruples the effective audio bandwidth, which is thus increased from 22 kHz to 88 kHz. The quantisation noise power, previously distributed uniformly across a 22 kHz bandwidth, is now distributed uniformly up to 88 kHz. Since 75% of the noise is now above the audio band, it can be suppressed by filtering.

The SAA7030 incorporates two identical filters, one for each stereo channel. Each filter is a finite impulse response transversal filter of length 24 with ninety-six 12-bit coefficients and using 16-bit input data words entering at 44.1 kHz. A recirculating shift register is used to store data required during the multiplication of input data with the filter coefficients which are stored in ROM. Each multiplication produces a 28-bit word which is stored in an accumulator, the 14 most significant bits of the words are then shifted out at DLFD for the left channel, DRFD for the right channel, with the clock $\overline{\text{CLFD}}$. Overflow protection is incorporated so that the output always limits cleanly in the unlikely event of accumulator overflow.

Oversampling and filtering add 6 dB to the SNR of the digital audio signal, bringing it to 90 dB for the 14-bit output words. A further improvement of 7 dB is obtained in the SAA7030 by means of a noise shaper. This circuit redistributes the quantisation noise, now uniformly spread across 0-88 kHz because of oversampling, reducing the noise in the audible region still further and increasing it above 22 kHz, see Fig.9.

A choice of offset binary or 2's complement output data can be made using $\overline{\text{OB}}$. The OS input enables a 3% d.c. offset to be added. This can be useful to reduce the effects of glitches at low output voltages with certain DACs. A 176.4 kHz strobe (LAT) is provided which can be used to latch data into the DAC in applications where a SAA7000 is not used.

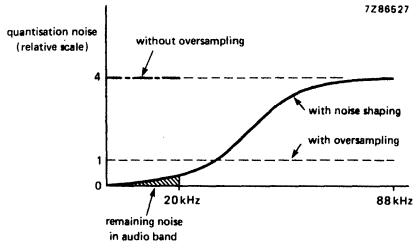


Fig.9 How 16-bit SNR is obtained from a system using 14-bit DACs. Oversampling reduces the in-band quantisation noise by spreading the total noise over a wide bandwidth. Only a quarter of the original quantisation noise remains in the audio band after oversampling. This increases the SNR of the words applied to the 14-bit DACs from 84 dB to 90 dB. Noise shaping adds another 7 dB, making the maximum SNR of the conversion system 97 dB, the same as that of a conventional 16-bit system

TDA1540: 14-bit DAC

Each TDA1540 converts 14-bit digital audio samples arriving at 176.4 kHz to an analogue output current. The output current is held between conversions by latching a flip-flop in the output circuitry of the DAC.

Data DLFD (left channel), or DRFD (right channel) are entered serially with the clock $\overline{\text{CLFD}}$. STR2 strobes the input data into a latch.

The TDA1540 uses a method of current division called dynamic element matching to achieve high-accuracy, binary-weighted currents with long-term stability. The input data are used to activate fourteen bit switches which determine the output current. Conversion to an output voltage is done in the analogue filters following the DAC.

The hold function of the DAC results in a (sin x)/x response with a first zero point at 176.4 kHz which suppresses the signal around that frequency.

If desired, one of the reference current sources in the TDA1540s can be adjusted, see Fig.8. This will compensate for slight differences in the DAC output currents for identical input data due to tolerances in the external components.

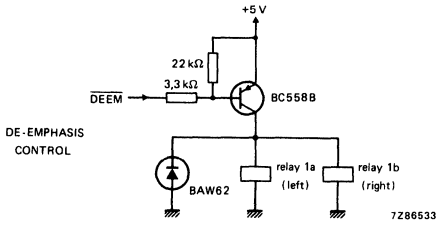
Analogue filters

The analogue filters suppress any remaining frequencies above the audio band. Since the first spectral lobe is at 176.4 kHz ± 20 kHz and has already been largely suppressed by the hold function of the DAC, third order low-pass filters provide sufficient attenuation. A Bessel filter with a cut-off frequency of 30 kHz is used because it has a linear phase characteristic. Figure 10 shows a suitable filter designed around the NE5532 dual opamp. The output of the filter is 1 V r.m.s. max. The filter components don't have to be adjusted and the de-emphasis circuit can be automatically controlled by information on the discs.

Both the Bessel filter response and the (sin x)/x response of the DAC have been taken into account when calculating and scaling the filter coefficients in the SAA7030 to give the digital-to-analogue conversion unit a flat frequency response in the audio band.

Note: the conversion system can be used at other sampling frequencies since the digital filter retains its cut-off frequency at 0.45 times the input sampling frequency. In addition, the (sin x)/x compensation is unchanged for different sampling frequencies, the first zero always occurring at the oversampling frequency. For a large frequency variation, only the analogue filter has to be changed to maintain an optimally flat amplitude characteristic.

Figure 11 shows how the original audio spectrum is recovered from the digital audio by oversampling and digital filtering followed by analogue filtering.



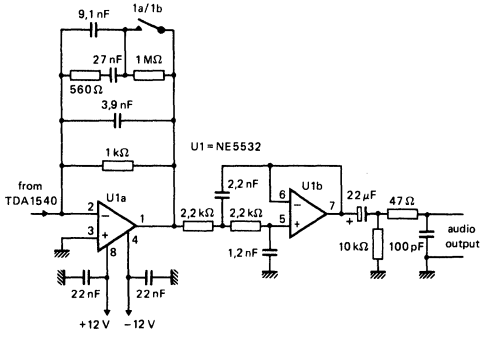


Fig.10 Third-order Bessel filter shown in Fig.8

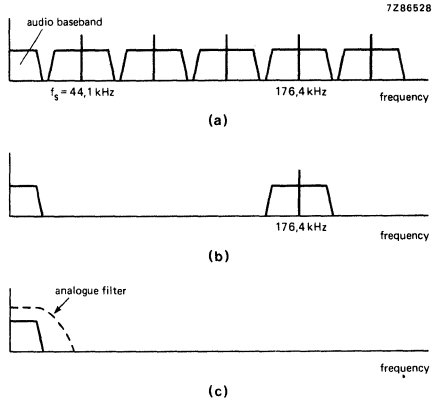


Fig.11 Oversampling and digital filtering remove the spectral lobes between the baseband and 176.4 ± 20 kHz, so that cheap low-order low-pass analogue filters can be used after the DACs instead of very-high-order ones necessary to suppress the 44.1 ± 20 kHz lobe in systems not using oversampling techniques. (a) Spectrum of an impulse-sampled audio signal sampled at 44.1 kHz. (b) Spectrum after oversampling at 176.4 kHz and digital filtering which suppress the lobes between the audio baseband and 176.4 ± 20 kHz. (c) Audio output spectrum. The lobe around 176.4 kHz is suppressed by the hold function of the DAC, which has a sin x/x characteristic with a first zero at 176.4 kHz, and by the analogue low-pass output filter with a cut-off frequency between 30 and 40 kHz

Power supply

Supplies for the decoder shown in Figs.6 and 8 are easily derived. Figure 12 shows an example.

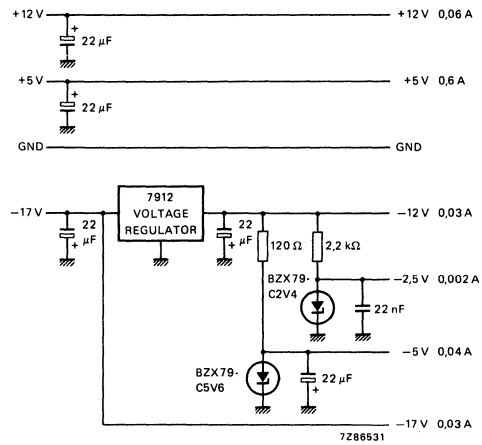


Fig.12 Power supply of decoder

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2. VAN DE PLASSCHE, R. J., 'Monolithic 14-bit DAC with 85 dB S/N ratio', Electronic Components and Applications, Vol. 2, No. 4, August 1980, pp. 234-241.

Small Area Networks Using Serial Data Transfer AN163

THE I²C AND CLIPS

The attraction of serial data transfer is that it requires fewer lines — and, equally important, fewer line drivers, receivers and signal processing circuits — than parallel transfer. Microprocessors and microcomputers work with data in parallel form, so parallel transfer is still the method of choice where distances are short and the number of devices sharing a communication channel is small.

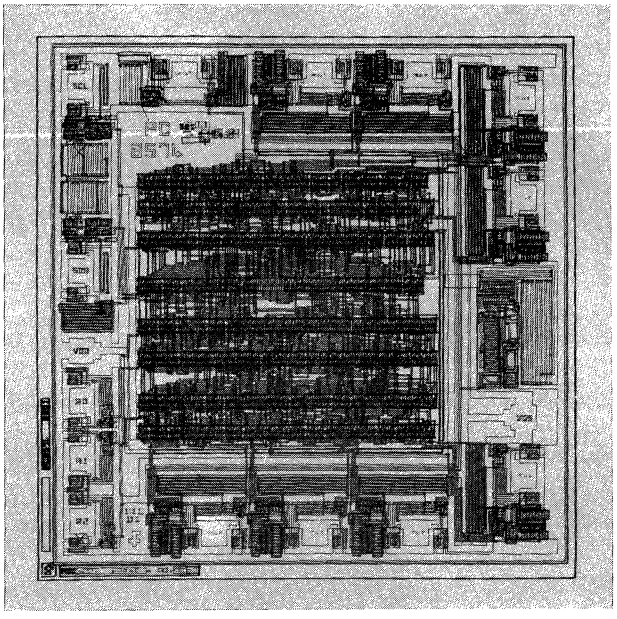
It is straightforward and fast, and in the disciplined environment of most computing and data processing equipment the multiplicity of conductors required is unobjectionable. But in many other applications of digital data transfer that is not so.

The answer is then to sacrifice speed for simplicity and flexibility, and to opt for serial instead of parallel transfer. Two conductors are usually sufficient, and the additional requirement it imposes for parallel-to-serial and serial-to-parallel converters can be easily met by today's LSI.

Serial data can be transferred asynchronously (unclocked) or synchronously (clocked). Asynchronous data typically originates from low speed terminals with rates of less than 1200 bits per second. When idle, the transmission line is at mark (binary 1); a start bit, or transmission from mark to space (binary 0), signals the beginning of each character, and one or more stop bits its end. This sequence is repeated character by character until the whole message has been sent; the start and stop bits enable the receiver to synchronize itself character by character with the transmitter.

In synchronous transmission, the clock signal that synchronizes transmitter and receiver may be carried on a separate wire or incorporated in the data stream by one of several codes (NRZI, Manchester, FM, etc). Once the receiver senses a synchronization character, data proceeds character by character with no intervening start or stop bits. A special ending character or a specified character count tells the receiver when the message is over.

Asynchronous transmission is advantageous when the data flow is irregular, as from a keyboard operator's typing speed. Because of the simplicity of the interface logic and circuitry, it is also cheap. Synchronous transmission, on the other hand, makes far better use of the communication channel capacity by eliminating start and stop bits between characters. Furthermore, when using modems, it proves suitable for multi-level modulation schemes which combine two or four bits in one signal element.



One of the CLIPS System IC's — the PCF8574 8-bit I/O Circuit.

One of the major drawbacks of a serial data link is that it is autocratic; it relies on a master or primary station to control all communication on the link. Even if the data from one secondary station is meant not for the primary but for another secondary, the primary must first store the data, poll the intended secondary to determine whether it is ready to accept the data, and then retransmit the data.

It does not adapt easily to changing conditions. If some stations have periods of peak activity, elaborate software algorithms must be written to take that into account. Moreover, if the system characteristics are ever changed, those algorithms have to be updated.

Also, it does not adapt easily to changing requirements. As all activity is centrally controlled, adding or removing secondary stations necessitates changing the software that controls the primary. This is so even if the secondaries affected need only to communicate with each other and not with the primary.

The reliability of the entire system depends on that of the primary; if for any reason it fails, the entire system fails.

If the system is one that relays control information to a decision-making center, its data-gathering and status monitoring secondaries have to be polled continually. Often, however, the polling indicates no change and so returns little real information; thus, the overhead due to the polling protocol is high in relation to the data acquired. (This problem is dealt with dif-

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ferently in a computer. There, a peripheral unit takes the initiative and interrupts the computer when it requires attention. As serial data links lack that facility, they must often be designed with much more capacity than their actual data rate requires, merely to accommodate the polling protocol).

These limitations of serial data links derive primarily from the fact that they are based on old electromechanical principles and do not take advantage of the opportunities now offered by VLSI.

Local area networks, by contrast, do not rely on a central controller; they are democratic, not autocratic. Any unit can take control of the network whenever it needs to and can transmit directly to any other. When two units require control simultaneously, they arbitrate to determine which gets it.

Local area networks are self-adapting to conditions since the attached units request to use it only when they need to; if necessary, some can be assigned higher priorities than others.

Like a telephone exchange, networks can easily be adapted to changing requirements. Any unit can call any other or group of others (conferencing). New units can be added without disturbing existing ones, provided that the total data rate never exceeds the network capacity.

Since control is not central, communication does not depend on any single unit, and since any unit can take control and address any other, the network in effect allows one unit to interrupt another. In a monitoring and control system, therefore, the network capacity need be scarcely larger than the required data capacity.

Small area networks such as Ethernet, intended for data rates of 10^6 to 10^7 bits per second over distances of 400 to 2000 metres, are well suited to transferring data between two large computers with their own files or to carrying digitized voice communication as well as data. However, they are overqualified for tasks such as transferring data between a terminal and a slow printer, or between a floppy-disc file server and a terminal.

Small area networks (SANs) can be regarded as less expensive, lower-performance counterparts of LANs. Their application areas include: the home, where they can be used to transfer control, information, and security signals; business, where they can deal with traffic insufficient to justify a LAN or can serve as feeder networks to a LAN; and certain self-contained units, such as motor cars, where sensors, actuators, and services are necessarily remote from the operator's displays and controls.

Apart from size and performance, SANs differ from LANs in another important respect: LANs are big enough to justify professional managers to configure and administer them; SANs are not. A SAN should require no adaptation when units are added to the network or removed from it.

Two SANs that provide the facilities of a LAN but on a smaller scale and have appeared in the past two years are the Inter-IC bus (I^2C) and the digital data bus (D^2B). Both are designed to cover only limited distances.

The procedure for a unit attempting to use the bus is as follows:

- Wait until no activity is detected on the bus.
- Then issue a start bit which is unique and recognizable as such. (If a unit detects another's start bit just as it is about to issue one of its own, it retires and synchronizes its internal clock on the edge of the detected start bit).
- After the start bit, issue message bits serially, most significant bit first.

I^2C and D^2B are both wire-AND buses, which is essential to their method of resolving conflicts. Consider the situation when two units, A and B, happen to transmit simultaneously. Say A attempts to issue the signal 1101, and B the signal 1110. Both issue the first bit, a 1, and monitor the bus; both see a 1, so both proceed. The same occurs again on the second bit. But on the third bit, A issues and sees a 0, while B issues a 1 and sees a 0 because of the wired-AND. This is a signal to B to retire immediately, as it has lost the arbitration. (The retirement must be immediate, otherwise a similar situation would occur again on the fourth bit, but in that case with A losing). This method of arbitration works because the shortness of the bus sets a limit to the propagation time between any two units on it.

Besides using the same principle for arbitration, I^2C and D^2B are also similar in other respects. They both distinguish between master and slave and transmitter and receiver. The master is the unit that initiates an exchange with a slave. If it requests a slave to supply data, it is the receiver and the slave is the transmitter. If it supplies data to a slave, it is the transmitter and the slave is the receiver. Not every unit on the bus has to be able to function as a master; slave-only units are also permissible and are of course cheaper.

Another similarity is in the method of acknowledging correct receipt, whether of data or address. The line is an open collector one, and while the transmitter awaits acknowledgement it lets the line stay high. If the receiver does not pull it low within a prescribed time, the transmitter interprets that as a NACK (negative acknowledge) indicating that what was sent was not correctly received. If a non-existent unit is addressed, the addresser will automatically see a NACK.

Apart from these similarities, I^2C and D^2B differ significantly in function, application area, and throughput characteristics.

The I^2C bus is designed to provide the facilities of a local area network within a single system or equipment. It enables the system designer to distribute the system functions where they are most needed or convenient, without having to pay more than cursory attention to interconnection problems.

The bus consists of two lines, serial clock (SCL) and serial data (SDA), and, unlike other buses, permits more than one unit to drive the clock. This is possible because their own internal clocks can operate together and synchronize with each other (figure 1).

Normally the SDA line changes only when SCL is low, so that the receiver can sample data on the rising edge of the next clock pulse. To generate a start condition, however, SDA goes from high to low while SCL is high (figure 2); this is a unique occurrence which enables all units to recognize the start of a message. The stop is similarly unique: SDA goes from low to high while SCL is high.

A complete message on the I^2C bus consists of the following fields:

START BYTE	SADD	R/W ACK	ACK	DATA STOP

START — Start condition (also called start bit).

SADD — Slave address, a 7-bit identifying the slave to be addressed and the priority of the message.

R/W — Read/write, a single bit indicating whether the addressed slave is to be read from or written to.

ACK — Acknowledge bit for the preceding field.

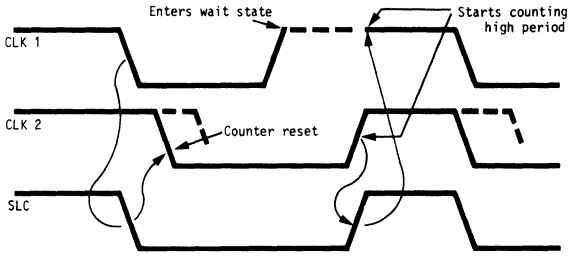

Figure 1. Clock Synchronization on the I²C Bus.

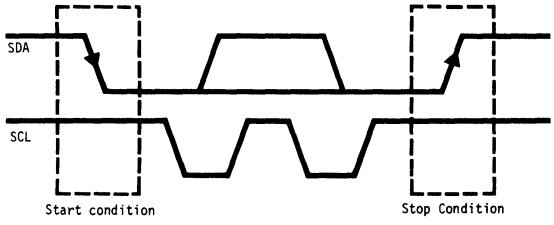

Figure 2. Start and Stop Conditions.

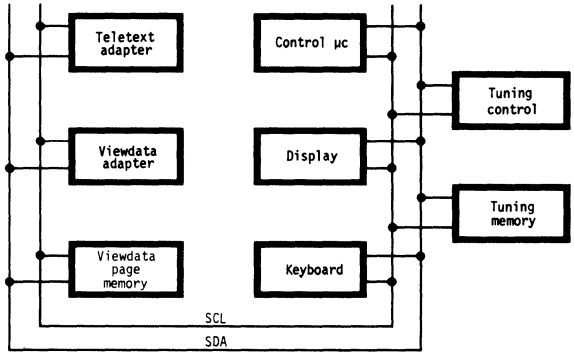

Figure 3. Application of the I²C Bus in a TV Set.

DATA — A series of 8-bit characters, each followed by an ACK. There is no set limit to the number of characters in this field, although one may be imposed in certain implementations.

STOP — Stop condition (also called stop bit).

There are no hard and fast limits to the length of the bus or the number of units that can be attached to it; there are implicit limits, however, due to the 400pF maximum capacitance that can be connected to either the SCL or the SDA line.

The I²C bus can be monitored and driven either by specialized hardware or, more slowly, by software in a microcomputer. In the latter case, the start bit is followed by a start byte of the form 00000001 to give slaves which have the system algorithm implemented in software rather than hardware time to poll the data line. Once such a slave detects a low value on the SDA line, it switches to scanning the line more frequently.

The maximum bus throughput rate is 100K bits per second, corresponding to about 11K characters per second; lower rates can be achieved with slower devices making use of the clock synchronization principle.

Typical applications of the I²C bus take advantage of the ease with which units can be added to or removed from it. As an example, consider the TV set illustrated in figure 3. The 'standard' set includes the blocks on the right of the diagram. The control microprocessor has master capabilities and communicates with slave-only units in the keyboard, tuning control, tuning memory, and tuning display. The optional units on the left can be added or removed at any time; the ACK/NACK facility of the bus automatically tells the control microprocessor whether they are there or not.

The optional page memory for viewdata is an example of the ability to communicate on the bus without the controller even having to be aware of the unit's existence. Only the viewdata unit needs to communicate with the page memory, and, provided it has bus-master capability, it can do so directly.

The bus gives the set designer freedom to place the various units wherever is functionally best — the display and keyboard on the front panel, the tuning control away from heat sources, and the others where they can most easily be installed later as

extras. It also gives him the freedom to redesign units to reduce cost, improve operation, or take advantage of new technology without worrying about the impact on other units in the system; only the two-wire interface and the command set need remain the same.

The D²B is designed primarily as a device-to-device interconnection, although it could also be used in certain self-contained equipment where some of its characteristics, such as low radiation and greater length, might make it preferable to the I²C. It is currently being considered by CENELEC as a possible European standard for the interconnection of electronic apparatus in the home.

The CLIPS concept: To exploit the 'building block' design possibilities using the I²C, Philips now offers a range of devices under the collective designation CLIPS (consumer and industrial peripheral set). The aim of CLIPS is to create a design environment in which devices can be 'clipped' on to a bus. Incorporating the hardware capable of supporting the I²C bus directly on-chip enables the designer to concentrate on the functional aspects of a system without having to worry about the communication link between the different system parts.

Hardware for I²C is already being marketed by Philips and includes the MAB8400 series of single-chip microcomputers. Peripherals incorporating the bus interface are also available and more are being developed. They include display drivers, memories, timers, tuning systems, A/D and D/A converters, and a CMOS gate array for specialized functions.

A licensing agreement between Philips, Signetics and Intel (*Electronic Engineering*, March 1983, page 108) has resulted in the availability of PCF80C48 and PCF80C51-based microcomputers incorporating the I²C and D²B buses, as well as development support products such as assemblers and in-circuit emulators.

Devices: To give examples of the types of circuit available addressing schemes and read/write actions, some of the CLIPS ICs are described below.

The PCD8571 static CMOS RAM incorporates an interface for direct connection to the I²C bus. Its low data retention voltage (min 1V) and low standby current (typically 50nA) make this memory suitable for numerous CLIPS applications.

In addition to acting as a general-purpose RAM expansion for CLIPS microcomputers, the PCD8571 can also find service as a more dedicated device. In the telephone application described below, for example, it can provide the extra RAM to store telephone numbers for repertory dialing. In radio or tv, it can be used to store channel presets.

Three hardware address pins are included on the PCD8571 to extend the specific device address. Up to eight of these RAMs can be connected to the I²C bus, allowing the amount of memory used and its eventual purpose to rest with the designer.

Auto-increment for memory word addresses also facilitates efficient write/read of blocks of data; for example, channel preset information in a tv application would usually require two consecutive data bytes.

The PCF8577 is a CMOS silicon gate LCD driver for driving either 64 segments duplex or up to 32 segments directly. For systems with several PCF8577s, hardware subaddressing and automatic address incrementing keeps wiring and bus traffic to a minimum.

CLIPS circuits such as LCD drivers require control information from the microcomputer in the form of pointers or control bytes before they can carry out a requested function. This information is provided within the I²C bus addressing procedure. The first byte of the slave address is used to address all LCD drivers connected to the I²C bus. All PCF8577 devices connected to the bus will therefore respond to this address. Each device then loads the second byte into its control register.

The six least significant bits of this byte constitute the segment byte vector (SBV); they select the device and the segment byte register which is to be loaded next. The upper three bits of the SBV are compared with the preset hardware address of the device. If the address is the same, the device is enabled for loading.

After each segment byte is loaded, the SBV is incremented automatically. In this way, sequential loading occurs when more than one segment byte is received in a data transfer. The control register also includes two display control bits, MODE and BANK. The MODE bit selects either direct drive or duplex; the BANK bit allows switching between two alternative control stores when the device is in the direct drive mode.

The programmable addressing of the PCF8577 allows the number of LCD drivers connected to a CLIPS system to be increased to a maximum of eight directly driven units (four duplex), giving 256 display segments. Therefore, the type of display output can be tailored to suit each member of a product range.

As shown in the industrial control example, (figure 8), remote I/Os within a CLIPS system can act as an interface between the I²C bus and a digital source. The PCF8574 is an 8-bit I/O circuit. It consists of an 8-bit quasi-bidirectional port and an I²C interface. This device can also interface microcomputers without a serial interface to the I²C bus (as a slave function only). The PCF8574 has low current consump-

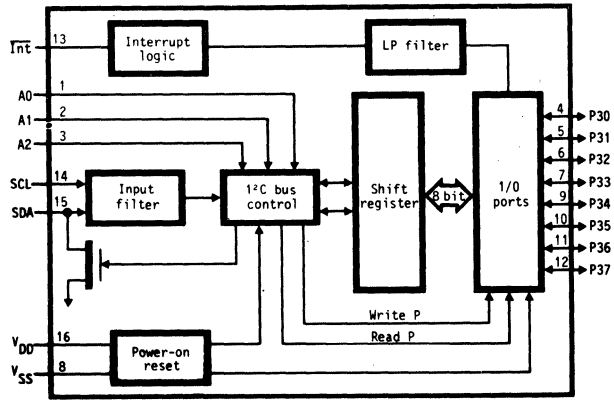

Figure 4. Block diagram of the PCF8574. The interrupt latch informs the microcomputer of data on the I/O ports which can then access the expander in the READ mode via the I²C bus.

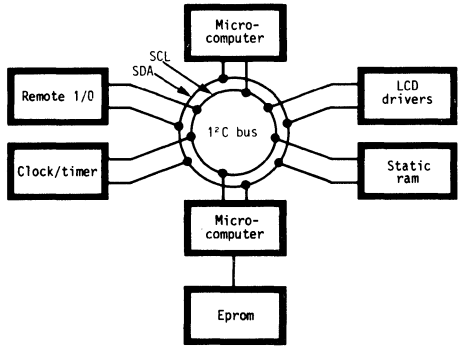

Figure 5. Typical CLIPS Application Showing the General Purpose Circuits Used in Most 8-bit Designs.

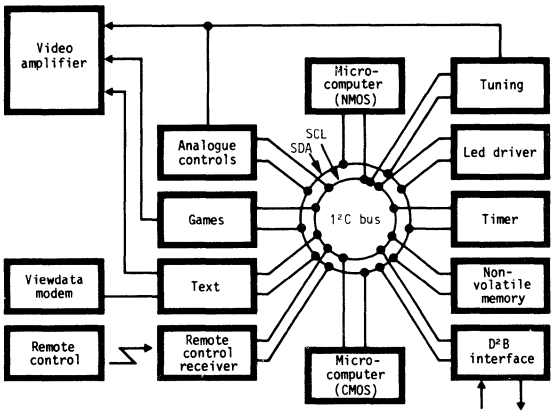

Figure 6. Modern TV Using the I²C Bus.

tion and includes latched outputs with high current drive capability for directly driving LEDs.

The PCF8574 differs from the other CLIPS circuits described above in that it possesses an interrupt line (INT). This line is connected to the interrupt logic of the microcomputer on the I²C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C bus. This means that the PCF8574 can remain a simple slave device (figure 4).

To cover a broad range of applications, including battery-powered operation, most CLIPS circuits will be CMOS devices; because of its high noise immunity CMOS is ideal for noisy industrial and automotive applications. The specification of the I²C bus, however, permits devices using any type of technology (CMOS, NMOS or I²L) to be connected together in one CLIPS system. Besides standard DIL, all CLIPS circuits are also available in SO packages.

CLIPS circuits are also adaptable to further integration. A typical system can be considered as various general purpose devices — microcomputers, LCD drivers, I/O expanders, extra memory (figure 5), with specific application-oriented devices tagged on. If a particular CLIPS system has been successfully used in large numbers, the specific combination of devices can be integrated with the existing general-purpose devices. Separate microcomputer and A/D converter ICs, for example, can easily become one unit, with circuit functions and system performance remaining the same.

Standardization within CLIPS systems leads to more economical use of any software developed. Modular application software can be used again and again in a variety of applications, carrying out the general-purpose functions within a CLIPS system. Subroutines associated with implementing a particular CLIPS IC will also be included in the support material for that circuit as an aid to designers.

Applications: To illustrate how CLIPS can be used, a few implementations in widely differing applications will be discussed.

Video games, teletext and home computers are transforming TV sets from mere receivers of broadcast programes to complete entertainment and information terminals. As extra features are introduced, the TV receiver must be able both to accept them and integrate them.

Let us consider a top-of-the-range TV set including at least a remote control, a games interface, and viewdata capability. Figure 6 shows how these, as well as other functions, might be served by a CLIPS system. Using CLIPS, it is possible to relate each block to an equivalent IC.

A point worth noting is the use of the remote control receiver within the system. Since the microcontroller associated with this device has to be active all the time, it is best implemented in CMOS. The I²C bus supports devices in any of the major manufacturing technologies and, therefore, allows each IC in the CLIPS system to be realized in the technology best suited to its function.

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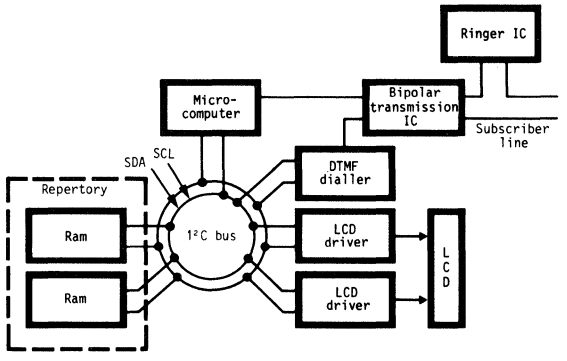


Figure 7. Telephone Using the Bus.

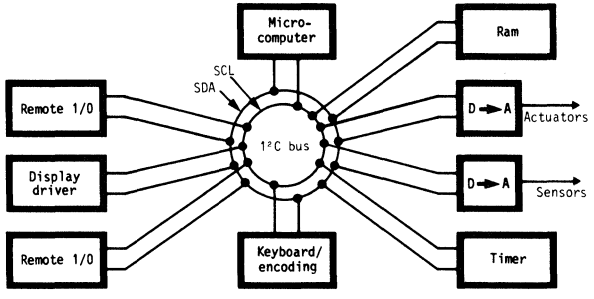


Figure 8. An I²C Bus Based System for Industrial Control.

The D²B interface enables the TV to be linked to other 'intelligent' appliances, such as a VCR or video camera, which themselves benefit from CLIPS implementation.

The CLIPS implementation of a subscriber telephone set includes all the functional units usually found in top-of-the-range models (figure 7). The RAM is in addition to that found on the microcomputer and can be used for such functions as repeated call or repertory dialing. The DTMF dialer can be added whenever the local exchange converts to a tone-dialing system. The LCD and its drivers are also optional.

By providing the general-purpose devices within a telephone set, the CLIPS system gives the designer a great deal of freedom. Although the application demands that the interfacing ringer and bipolar transmission ICs are not connected directly to the I²C bus, the other devices which can be configured to match a wide range of specifications and demands from both telephone authorities and subscribers.

Philips has already built up a library of telephony-related software modules to help designers meet the various requirements they are likely to encounter.

Each telephone authority has its own requirements; each consumer has his own preference. To design a 'cover-all' telephone set is almost impossible. CLIPS offers a framework within which a designer can work effectively.

In industrial environments, CLIPS systems (figure 8) can perform a variety of functions. For intelligent machine control, level sensing or pressure monitoring, the implementation of CLIPS systems can provide distributed processing and microcomputer control on-site, where it is needed.

For analogue applications, a range of sensors can be used. These can then be connected to an A/D converter to provide data for devices connected to the I²C bus. Keyboard encoding circuitry provides user-access to the system, with user-output sent via the display driver.

For control purposes, evaluated data can be fed back to actuators such as temperature controls or electromechanical switches via another D/A converter.

For digital applications, data can be sent or received via remote I/O circuits.

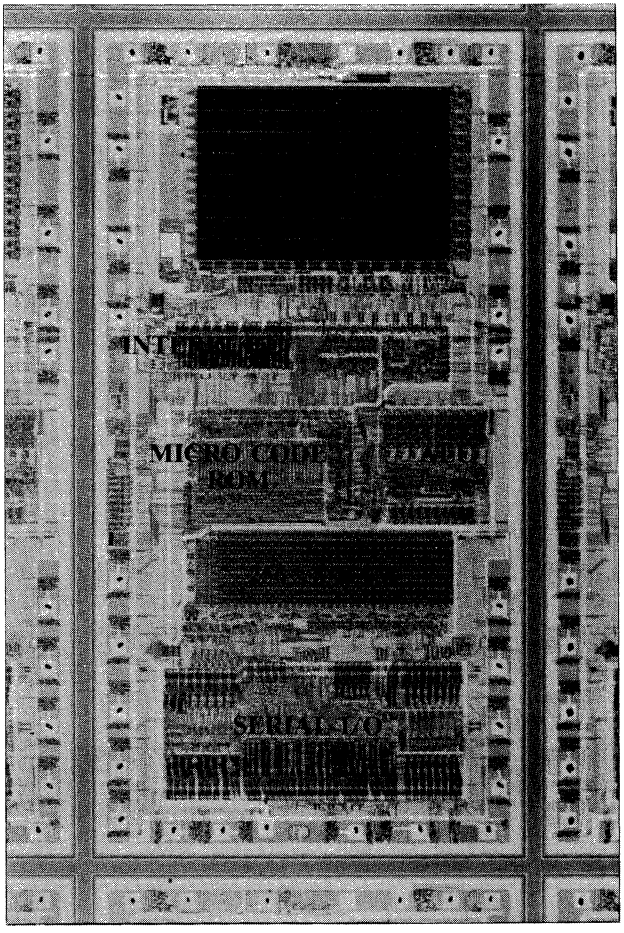
Due to the nature of the I²C bus, remote I/Os can be situated anywhere within the control environment; other CLIPS circuits can likewise be placed exactly where they will best perform their alotted task. Within a cabinet, wiring can therefore be greatly reduced. Instead of trailing parallel wires between devices, remote I/Os can be used to convert the parallel device output into serial bus input almost immediately — saving space and wire and making life much easier for the service engineer.

The remote I/O, for example, would be connected near simple on/off devices: to drive valves or relays, activate emergency sirens, or read keys and drive LEDs.

When used in an industrial environment, CLIPS systems can also be connected to higher levels of control, using parallel ports of the microcontroller, for example.

A CLIPS system can therefore cover the complete range of industrial applications from hand held, battery powered measuring instruments to the first stage of a large scale process control system.

For low volume industrial designs, piggyback versions of both the NMOS MAB8400 and CMOS PCF84COO single chip microcomputers can be used. By connecting industry standard EPROMs to these devices, designers can still build systems using CLIPS ICS.



SLAVE DEVICES

In the preceding section the salient features of the Inter IC (I^2C) bus and its protocol were described. The bus is key to a structured approach to system design based on a combination of microcontrollers, general purpose peripheral IC's (LCD drivers, memory) and/or application-dedicated peripheral IC's. Such circuits are known collectively as CLIPS since they can simply be 'clipped' onto the bus.

While multi-master control and two-way information transfer are fundamental elements in any flexible design concept, there are many applications in which the peripheral circuits need only accept commands and/or data and thus, apart from the need to acknowledge receipt of data, information transfer is one way only. Now we will describe how the bus may be used in such applications. For simplicity, it is assumed that only one master controller is used.

The I^2C bus has been described in some detail and the main features are as follows:

There are two lines — for serial data (SDA) and for serial clock (SCL).

A START condition occurs when the SDA level changes from high to low when SCL is high.

DATA on SDA is changed when SCL is low and is clocked on the rising edge of SCL.

The byte immediately following the START condition consists of the seven bit address of the intended addressee and, in the LSB position, a READ/NOT-WRITE bit for the ensuing communication.

At the end of each 8-bit byte, including the first, a ninth clock pulse is supplied on SCL and an addressed receiver may pull SDA low to signal an acknowledgement of a received byte.

A STOP condition is defined by a low to high of SDA when SCL is high. Figure 9 illustrates the SDA and SCL for START, address with R/W, two data bytes and STOP.

In multimaster configurations of the I^2C bus, a contending master must be able to detect that the bus is busy and that arbitration after bus contention has been achieved.

A slave must be able to:

- recognize a START condition,
- recognize its own address when sent immediately after a START,
- respond to the READ/NOT-WRITE bit,
- when receiving, provide an ACKNOWLEDGE on each ninth clock,
- recognize a STOP and, if a transmitter, release the bus.

I^2C bus hardware: There are several bus configurations to be considered:

- single master and one or more passive slaves that do not put data on the bus e.g., display drivers;
- single master and slaves that can transmit e.g., RAMs; and
- multiple masters.

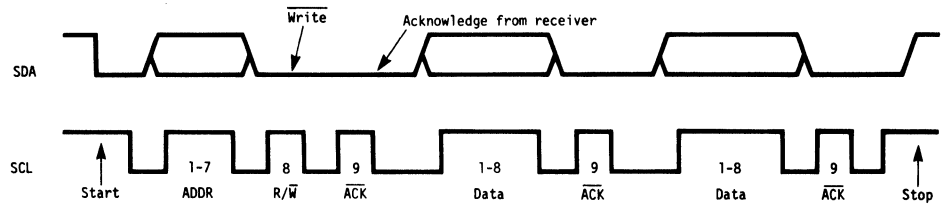


Figure 9. The SDA and SCL for START, Address with R/W, Two Data Bytes and STOP.

All devices are connected to the I²C bus in the WIRED-AND mode and the two lines, SDA and SCL, each have a pull-up resistor. The 'quasi-bidirectional' I/O on many MOS LSI circuits, with open drain, is suitable provided the device can sink 3mA.

A single master transmitter, apart from being able to provide the proper timing, in particular for the START and STOP conditions, has a data register which can send out data serially, MSB first, onto the SDA line and which can be loaded in parallel from the rest of the IC.

It must also leave SDA high for the ninth clock pulse and be able to test for receipt of ACKNOWLEDGE.

As a master receiver, it must accept serial data and read the I/O register in parallel.

For the other bus configurations this serial data register should rotate such that data sent out serially is also clocked back into the same register. However, the hardware requirements of these other configurations will be described in a future issue.

The requirements of a master transmitter can be met by a single chip microcontroller 'bit bashing' two I/O pins under software control, but to transmit data at the maximum serial clock rate of 100 kHz specified in the I²C bus specification would occupy most of the microcontroller's real time capacity.

The first devices developed with I/O specifically for controlling the I²C bus are the MAB8400 range of microcontrollers. These are based on the widely used 8048 8-bit controllers. Other microcontrollers with I²C bus interface and based on the 80C49 and the 80C51 will come onto the market this year.

The MAB8400 is based on the 8048 but, instead of being housed in a 40 pin package, it uses a 28 pin package. Unlike the 8048 it does not have an external data bus and, therefore, cannot access external program memory. However, it is available with 4K ROM, which is the maximum program memory size addressable by the 8048 family. It has most of the 8048 instructions set, but those instructions for operating external memory are omitted and the two one-bit flags for setting and testing are not available.

An addition to the 8048 circuit within the MAB8400 is an area dedicated to controlling the serial I/O bus. At the time the MAB8400 was developed, there were few I²C peripheral devices available so the I/O circuitry was designed so that it can be programmed to drive other serial buses for which peripherals are available — the 'C'

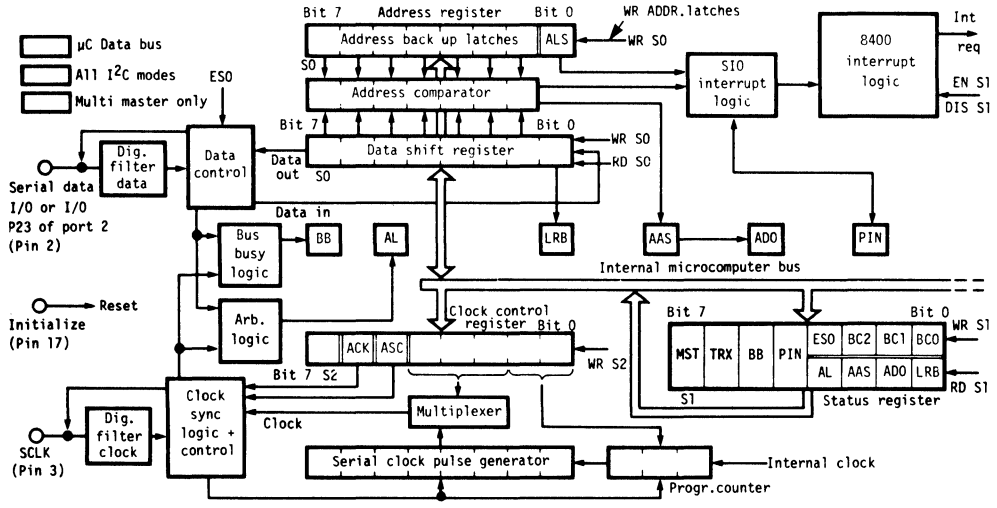


Figure 10. Serial I/O Interface of the MAB8400.

bus and the 'I' bus. A simpler I/O control can be made if I²C bus only is considered and controllers with simplified serial I/O will be available soon (MAB8422 and MAB8442 in 20-pin).

A block diagram of the serial section of the MAB8400 is shown in Figure 10. The serial I/O circuit lies on the main data bus of the microcontroller and is controlled by instructions for moving data between the accumulator and registers S0, S1 and S2. These registers can also be loaded by immediate instructions.

Register S0 is the I/O register with a serial connection to the I²C bus.

Register S1 is the main control and status register.

The MSB bit (MST) contains the Master/slave bit which is set to '1' when the microcontroller is commanding the bus conversation.

Bit 6 (TRX) is the transmitter/receiver set to '1' when transmitting.

Bit 5 (BB) is the bus busy bit and is set to '1' whenever a START appears on the I²C bus and is reset by a STOP, whether initiated by this or another master.

Bit 4, the pending interrupt not (PIN), is set to '0' whenever a complete word is transmitted or received over the I²C bus. It also reflects the serial interrupt state if that is enabled.

PIN is reset to '1' either by moving data to or from the I/O register S0 or by direct loading of S1.

There are two lower nibbles to S1:

a) can be written only by the controller, bit 3 (ESO) is set to enable the serial I/O, and bits 0-2 are for bit counting;

b) is set by the hardware and is read only by the controller to determine the status of the serial I/O: bits 3, 2, and 1 are arbitration lost (AL), addressed as slave (AAS), and all zeros addressed (ADO) respectively, and will be dealt with in more detail when multi-master systems are discussed.

Bit 0 (LRB) contains the last received bit and reflects the last data bit to appear on SDA after the rising edge of the last serial clock pulse on SCL.

Register S2 is used for setting up the I/O clock speed, whether the acknowledge feature will be used, and whether a symmetrical clock for I²C standard is selected. For I²C bus acknowledge is mandatory. This is summarized in Table 1.

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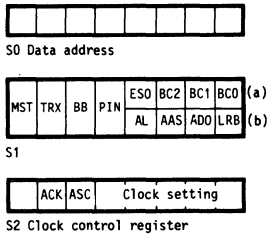

The simplest configuration of the I²C bus is one master controlling the bus and one or more 'dumb' peripherals that are not required to respond with any data. The following procedures must be implemented within the software that the user must write for the microcontroller:

- initialization of the serial I/O,
- sending the slave address,
- data transfer, and
- signing off.

Initialization: First the serial clock frequency is selected and, if working to I²C, rules, 'acknowledge', and normal symmetric clock are selected.

These are set by immediate addressing of the control register S2 e.g., MOV S2, #H'43'

will set the clock at 87kHz, assuming the MAB8400 is using a 4.43 MHz crystal. It also sets 'with Ack', (ACK = 1), and 'Symmetric', (ASC = 0).

By setting the status register S1, the controller is put into slave receiver mode, the serial I/O is enabled, and the word length is set to 8 bits:
MOV S1, #H'18'

MST = 0, TRX = 0, BB = 0, PIN = 1, SIO = 1, BC2, BC1, BC0 = 0.

To operate in an Interrupt mode then:
ENSI

Enable serial interrupt

But if it is prefered to work in a polling mode, the pending interrupt-not PIN bit in S1 (bit 4) may be examined. For this single master — dumb slave mode this completes the initialization.

Sending slave address: The slave address is seven bits which are sent out onto the I²C but MSB first. The LSB is set at 0 or 1 depending on the direction of flow of the data to follow. If 0, then the master will WRITE data to the slave.

If the address of the slave device, plus the WRITE bit, is in, say, register 7 the address must first be moved to the accumulator and then to the Serial I/O register S0:
MOV A,R7

Get slave address.

MOV S0,A

Put address in S0.

Alternatively, S0 could be immediately addressed:
MOV S0,#H'xx'

Address 'xx' with LSB = 0 to S0.

A 'START' condition must be created and the slave address transmitted.

This is done by setting the MASTER, TRANSMIT and BUS BUSY bits in the control register S1:
MOV S1,#H'f8'

Mst, Trx, BB, PIN = 1, ES0 = 1, BC2—BC0 = 0 (8-bits)

Transmission now starts.

Address sent: After eight clock pulses the address will have been sent onto the I²C bus. On the ninth clock pulse the serial data (SDA) line will be left high by the transmitting master and, if a slave recognizes the address, the slave will pull SDA line low to signal 'Acknowledge'.

The PIN bit in S1 of the MAB8400 will now go to 0 and the serial clock line, SCL, will be held low. If enabled, the serial interrupt will call the appropriate service routine.

Bit 0 (last received bit) is now examined to check that acknowledge was received. The programmer may jump to an 'error' routine if an acknowledge is not received:
MOV A,S1

Get status into accum. for testing.

JBO Error

Acknowledge failed so go to 'Error'

Send data: Having established a connection with the addressed slave, data can now be sent. A record of the communication will be kept in some register for checking that all the data has been sent.
MOV A,Rx

Will fetch data from Rx into accumulator

MOV S0,A

Puts the data in the I/O register.

This last instruction also releases the clock line, restarts the transmission and resets the PIN bit to 1.

Again, after nine clock pulses a serial interrupt will occur. As before the LRB will be tested to check if Acknowledge has been received.

Signing off: Once all the data has been sent, the bus may be cleared by creating a STOP condition. Another device may not be addressed until the bus has been cleared. To STOP all that is needed is to force the BUS BUSY bit in S1 to zero when in Master Transmitter mode:
MOV S1,#H'D8'

MST = 1, TRX = 1, BB = 0, PIN = 1, ES0 = 1.

The MAB8400 reverts to Slave Receiver mode automatically once the STOP has been transmitted.

To address the same or a further device, the procedure is repeated but with a fresh slave address.

The most obvious requirement for a straightforward single-master writing to slave peripherals is remote switching and specific applications include LED or LCD driving. As the number of segments in a display increases, the advantages of the I²C bus become more apparent since the use of serial data transmission still requires only the two data lines. The limitation on the number of segments is then determined by the drive capability of the drivers themselves or in some cases by the number of sub-addressed devices allowed.

There are several I²C bus peripherals suitable for remote driving extending from the SAA1300 which has five output stages capable of supplying up to 100 mA to LCD drivers capable of driving 160 LCD segments each. The DTMF (dual tone multifrequency) and modem tone generator, the PCD3312, also falls into the class of remote switching applications. A fuller list is given in the appendix, but for the purposes of this article a more detailed account will be given of the PCF8577 LCD-driver.

THE PCF8577 is designed to drive LCD displays. Each device is individually capable of driving either 32 segments in the static mode or 64 segments in the duplex mode, and several devices may be cascaded to permit system expansion to up to 256 display segments. In such multiple IC applications, I²C bus traffic is minimized by additional design features, including automatic address incrementing, hardware sub-addressing, and display memory switching.

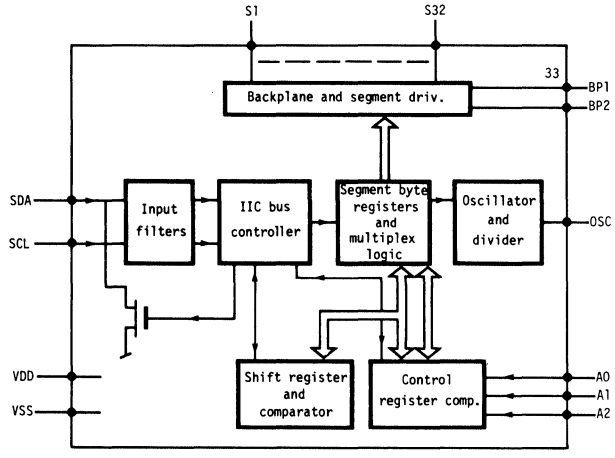

Figure 11. Block Diagram of the PCF8577 LCD Driver.

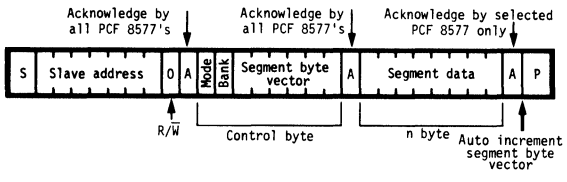

Figure 12. The Data Format of the PCF8577.

The salient features of the circuit are shown in the block diagram, Figure 11. The inputs include the I²C bus, clock (SCL) and data (SDA), and three hardware sub-address address inputs A0, A1, and A2 which are used to program the sub-addressed uniquely for each PCF8577 on the bus. The outputs include two back plane drivers, BP1 and BP2, and thirty-two segment drivers, S1 to S32. The second back plane signal (BP2) is only required during duplex mode driving of 64 segments. In passing it should be noted that, to reduce pin-out requirements, A0 and A2 are shared with the oscillator and BP2 signals respectively, but this may be disregarded for the moment.

The data format of the PCF8577 differs slightly from that of other I²C peripheral circuits and is shown in Figure 12. It comprises a slave address and a control byte followed by N segment data bytes.

The seven-bit 'software' slave address (0111010) is identical for all 8577's and all 8577's on the same bus acknowledge the slave address in parallel. Note that the eighth bit of the first byte is always set to zero, i.e. WRITE mode. The second byte is always a control byte and is loaded into the control register of all the PCF8577's on the bus and again all the services acknowledge its receipt in parallel. Subsequent data bytes are loaded into the segment data registers of the selected device (see below) but only the selected device acknowledges receipt of its data. If a STOP condition is generated after the control byte acknowledge, the segment data remains unchanged.

There are nine user controlled byte wide registers in the PCF8577. The first is the control register which is used to control the loading of data into the other eight segment byte registers and to select the display options. All PCF8577 devices on the bus load the control byte into the control register from the I²C-bus and thus at any one time each device has an identical copy of the control byte in the control register.

The register is shown in more detail in Figure 13. The six least significant bits select which device and which segment byte registers are to be loaded next and ac-cordingly this part of the register is known as the segment byte vector (SBV). The upper three bits of the SBV (V5 to V3) are compared with the hardware address input signals (A2 to A0) and if they are identical then the device is enabled for loading, otherwise the device ignores the incoming data. The three least significant bits (V2 to V0) define the address of the segment byte registers into which the segment data has to be loaded.

After each segment byte is loaded, the SBV is automatically incremented so that more than one segment byte can be sent in a data transfer. Furthermore, since the SBV refers to both the device and the segment byte registers, then auto-incremented loading may proceed across device address boundaries provided that the hardware-sub-addresses are arranged contiguously. In an expanded system, roll-over of the SBV form 111 111 to 000 000 is also possible.

All PCF8577 devices on the bus auto-increment the SBV even though they may not be loading segment data, but only the selected device transmits the acknowledge.

The control register also has two display control bits, MODE and BANK.

The MODE bit selects whether the device is to operate in the direct or duplex drive mode and the BANK bit allows the user to select which of the two groups of segment byte registers are to be displayed when operating in the direct mode.

If the MODE control bit is set to zero, then the PCF8577 is set to the direct drive mode. In this mode only four bytes are needed to store the data for the 32 segment drivers; accordingly, the eight seg-ment byte registers have been divided into two separate banks, even and odd respectively, which may be separately selected by the BANK bit. Setting the BANK bit to zero selects even bytes (bank A), whereas setting the BANK bit to one selects the odd bytes (bank B). Thus, in the direct drive mode, two independent display memory maps may be stored and the BANK mode bit may be used to display either one or toggle between them.

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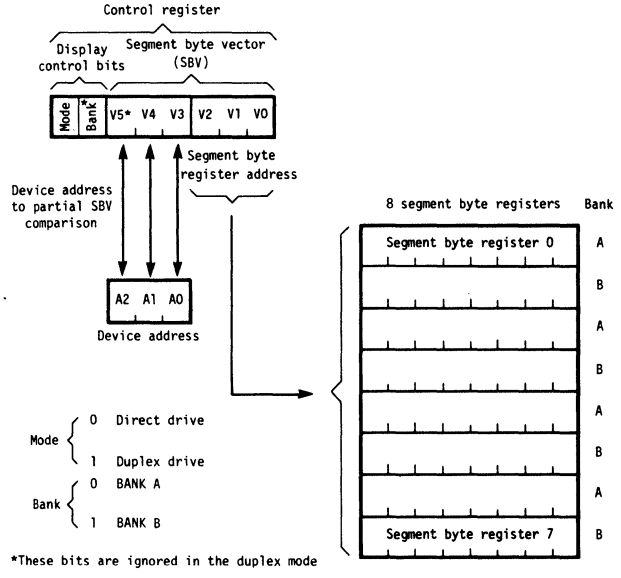

Figure 13. The Nine User Controlled Byte Wide Registers in the PCF8577.

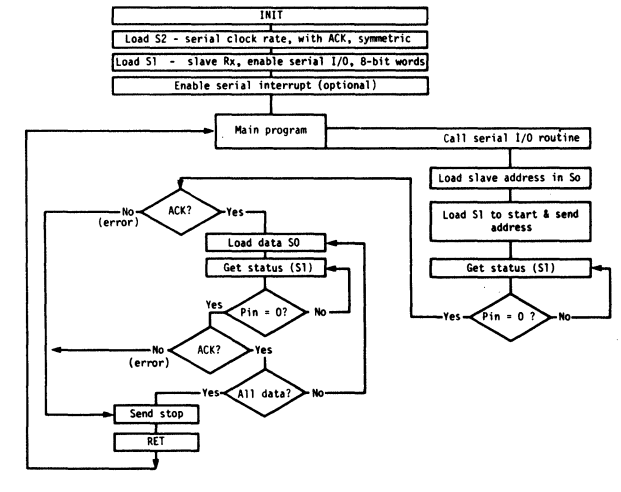

Figure 14. A General Flow Chart for Addressing and Sending Data to a Slave CLIPS Device.

When operating in the direct drive mode, the SBV is auto incremented by two after each segment byte vector is loaded. Thus, independent auto-incremented loading of bank A or bank B is possible, and either bank may be completely or partially loaded irrespective of which bank is being displayed.

With eight display drivers on the bus, two memory maps of up to 256 segments each may be stored, and, once loaded, it is only necessary to generate the relevant control bytes to switch between the two.

The duplex mode is established by setting the MODE bit to 'one'. In this mode the second back plane signal BP2 is required to drive the display, and consequently, since this pin is shared with A2, the value of the address pin A2 thus becomes undefined.

Duplex Mode

Accordingly, A2 (V5 in the SBV) and the BANK bit are ignored in the duplex mode, and the device hardware address is defined only by A1 and A0. Naturally, the SBV auto-increments by one between loaded bytes and device sub-address boundaries may still be crossed.

Inevitably, a maximum of four devices are permitted on the bus, but this still allows 256 LCD segments to be driven.

A flow chart for addressing and sending data to a slave CLIPS device is shown in Figure 14. It is assumed that the 'main program' calls the serial I/O routine when it is necessary to update the display.

After each byte has been put into S0 and transmission has started, S1 is repeatedly checked for PIN = 0 indicating that all eight bits of data have been sent and that the ninth clock pulse has also been generated. The LRB bit in S1 can then be tested to see if the data has been acknowledged. When all the data has been sent, a STOP is generated.

Figure 15 is a complete software listing of program that could be used for driving the PCF8577.

While in the above example a single display driver was used, the expansion to two or more devices involves no new I^2C bus principles and the application circuit Figure 16 shows how straightforwardly it may be implemented.

There are other LCD drivers in the CLIPS family designed specifically for higher levels of multiplexing and for dot matrix displays; namely, the PCF8576 and

```
*************************************************************************
*       Routine for driving PCF8577 LCD driver and liquid crystal display
*       via the IIC bus from MAB8400 master.
*************************************************************************

* In this example of single master 'dumb' slave system the program first goes
* through a short SIO initialisation.  The display routing DISP is called as
* a subroutine.
* The PCF8577 is used in the direct drive mode to drive 32 segments of LCD.
* The data to be displayed is assumed to be in the lower nibble only of
* RAM addresses 30-33Hex.
* Conversion of the numbers into data for driving the segments of the LCD
* is via a look-up table.
* In this example all 32 segments are loaded or updated using the
* auto-incrementing of the PCF8577 register addresses.  (If you need to
* change one digit only then just the appropriate register need be updated.)
* In this example the Pending Interrupt Not bit will be polled, as an
* alternative to using the serial interrupt.  The latter would give a more
* complex program but leave the CPU more time for other activities.
*
LCDD    asect   rom,inpage
        page    256
        entry   strt
        org     00
*
strt    JMP     init            reset vector
        org     09              clear of interrupt vectors
init    MOV     S2,#H'43'       with ACK, SCLK=67KHz with 4.43MHz Xtal.
        MOV     S1,#H'18'       slave, receiver, enable serial I/O
main    NOP                     main program!
        CALL    DISP            call display subroutine
        JMP     main
*
DISP    MOV     R0,#H'30'       pointer for display data
        MOV     R7,#04          counter for digits
        MOV     S0,#H'74'       address of PCF8577-write
        MOV     S1,#H'f8'       send out address
bytA    MOV     A,S1            get SIO status
        JB4     bytA            wait for PIN=0
*
* address sent so now check for acknowledge:
        JB0     ERROR           no acknowledge so go ERROR
*
* now send Control Byte to PCF8577
* select direct drive, bank A, 010 device address, 000 segment byte address.
        MOV     S0,#H'10'       this send control byte out and resets PIN=1
bytC    MOV     S1,A            get SIO status
        JB4     bytC            wait for control byte finished, PIN=0
        JB0     ERROR           check for acknowledge.
*
* Now get numbers from RAM, converting to segment data with look-up table SEGT
num     MOV     A,@R0           get number
        ADD     A,#H'50'        start address of look-up table
        MOVP    A,@A            get segment data
        MOV     S0,A            send out data
        INC     R0              set pointer for next number
bytD    MOV     A,S1            SIO status
        JB4     bytD            wait for PIN=0
        JB0     ERROR           ACK?
        DJNZ    R7,num          finished?
*
* message is finished so STOP must be sent.
Stop    MOV     S1,#H'd8'       send Stop.
*               MAB8400 automatically reverts to Slave Receiver after STOP.
*
        RET                     return to main program
*
ERROR   JMP     Stop            clear bus and try again!
*
*
SEGT    org     H'50'           Segment look-up table
        data    H'7E'           Segment data for '0'
        data    H'06'                            1
        data    H'DA'                            2
        data    H'8E'                            3
        data    H'A6'                            4
        data    H'AC'                            5
        data    H'FC'                            6
        data    H'0E'                            7
        data    H'EE'                            8
        data    H'BE'                            9
*
        END
```

Figure 15.

PCF8578. Naturally these devices need more control information to be sent in order to select between various modes of operation, but apart from the need to increase the number of control bytes between the slave address and the segment data, the data format remains the same and hence the driving routines are very similar.

In contrast with general purpose CLIPS such as the LCD drivers mentioned above, a dedicated peripheral, which may be used for the generation of DTMF, modem and musical tones, will be briefly described. The device, in contrast with the general purpose 14 pin tone generator (PCD3311), the PCD3312 requires only eight pins, two of which are required for the I²C-bus, one for the tone output and a hardware address pin A0. This latter pin identifies the particular device when two PCD3312's are connected to the same bus. Because all the filtering is done on-chip, no external components are required.

The simple data format is shown in Figure 17. The first byte, slave address, is followed by a single data byte. The lowest six bits in this byte are used to switch the oscillator on and off and to select various tone or tone combinations. These include:

- single-and-dual DTMF frequencies in accordance with CEPT CS203
- 300 and 1200 baud modem frequencies in accordance with V21, V23, Bell 103 and Bell 202, and
- two octaves of musical semitones in the frequency range 622 to 2489 Hz.

Modular Approach

Accordingly, with this single dedicated circuit a range of advanced DTMF/DECADIC 'feature telephones' with repertory, display, calendar-timing facilities may be constructed from what may be regarded as general purpose components. Such a modular approach, centered on the I²C-bus, leads to a high degree of flexibility: increased memory size or use of non-volatile RAMs instead of volatile ones, display options, etc, which are typical of I²C-bus applications.

The SAA1300 remote switch was designed to enable the I²C bus to be used to control the power supply lines of integrated circuits or other parts of a system. Consequently, the five-output stages were designed to supply 100mA in the on-state, or sinking — 100μA in the off stage. Naturally current limiting and short-circuit protection are included on chip and there are limitations on the total power dissipa-

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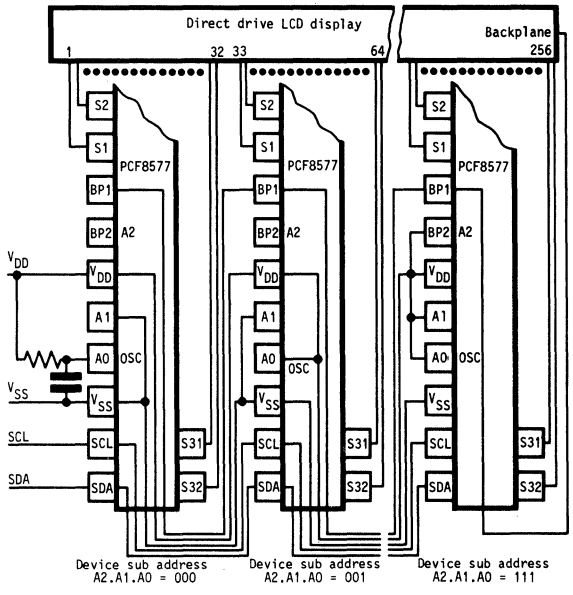


Figure 16. PCF8577 Direct Drive Display Application Diagram with Expansion to 256 Segments with 8 PCF8577 Units.

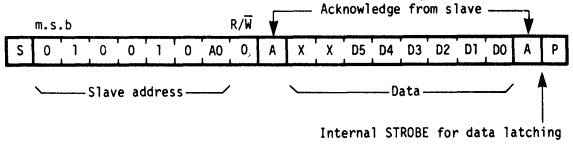


Figure 17. The Data Format of the PCD3312.

tion which prevents the supply of the maximum current at all the output stages simultaneously.

One of the output stages can be alternatively used as a sub-address input, and up to three circuits may be attached to the same I²C-bus. The 2-byte data format is similar to that of the previously described PCD3312, a slave address byte followed by a data byte. The only unconventional features of the circuit are the use of bipolar technology to obtain the high current capability and the use of a single sub-address which recognizes three separate voltage levels to select one of a maximum of three devices on the bus.

LED Drivers

Naturally, LED display applications fall between the very low current drive requirements of LCD's and the applications for which the SAA1300 was designed, and a specific LED driver is planned to fill this gap. Meanwhile the PCD8574 I/O port expander, to be described next, may be used as a LED driver.

An A/D and D/A integrated circuit, the PCF8591, is in development and, while it should be classified as a slave transceiver which will be featured more fully in a subsequent article, the D to A part is an example of another category of simple receive-only-peripheral I²C-bus applications. The complete device possesses a four-input multiplexed analogue to digital converter and a single I²C-bus to analogue output converter; the device is designed to function simultaneously as an ADC and DAC.

The data format is similar to that of the PCF8577 which in the DAC mode comprises a slave address (including three hardware sub-address kits), a control byte, and a data byte.

I²C MASTER CONTROLLER OPERATION

I²C bus applications have been considered in which a single master controller was programmed to write to one or more receive-only slaves. A liquid crystal display driver was used as the example, controlled by the MAB8400 microcontroller.

A larger range of CLIPS peripherals do not just receive data but respond with data; e.g., RAMs, I/O expanders, analogue to digital converters, etc.

The purpose of this section is to describe what is currently the most common configuration of the I²C bus, namely a single master microcontroller in the WRITE and READ modes. The particular case to be considered will be the use of the bus to store and retrieve data from the Mullard PDC8571 128 x 8 CMOS RAM with I²C interface.

As before it will be assumed that there is but one 'master' using the I²C bus. Arbitration between competing masters will be covered next month.

However, before this specific application is studied, the general format of the data is described.

The data format for sending data is shown in Figure 18a. The START condition is a falling edge of the serial data line (SDA) when the serial clock line (SCL) is still high. Then follows a seven bit address, to select the slave, together with the WRITE bit (0). This is followed by the acknowledge bit when the transmitter leaves SDA high and checks for the receiver dragging SDA low. In the case of the RAM the next byte is a pointer or word address but this could well be a command with other peripherals. This byte is acknowledged. The subsequent bytes are the data flow, each acknowledged, and the communication terminated with a STOP condition (rising edge of SDA with SCL high).

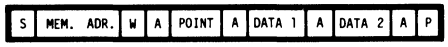
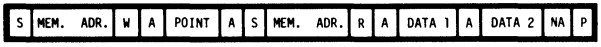


Figure 18a. Format to Write Pointer Value and Two Data Bytes.



S is the START condition
MEM ADR is the slave address of the CMOS memory PCD8571
POINT is the pointer address (internal RAM location address)
W is the read/write bit in write status (= 0)
R is the read/write bit in read state (= 1)
A is the acknowledge bit; this has to be '0'
NA is the not acknowledge bit, this has to be '1'
P is the STOP condition

Figure 18b. Format to Write Pointer Value and Read Two Data Bytes.

Though some peripherals may just send data as slave transmitters when addressed, many peripherals need a command or, in the case of a RAM, an address pointer, sent after the device address and before the actual data can be returned. This means that at the start of the conversation the master is a transmitter and then, having sent the slave address and the appropriate command(s) or pointer, the master must turn the conversation round and receive data from the slave transmitter. At the end of the conversation a STOP condition has to be created to clear the I²C bus.

The format for sending a pointer and receiving data is shown in Figure 18b. The READ/WRITE bit only occurs as the least significant bit of the slave address which follows the start condition; therefore a second start condition is generated followed by the slave address with the READ bit set (1). When all the required data has been received, the master receiver instructs the slave transmitter to release the bus by sending a 'not acknowledge' of the last data byte; the master can then generate the stop to clear the bus.

In the CLIPS family of I²C peripherals the four most significant bits of the device address are commonly fixed within the IC leaving the three LSBs for selection by wiring. This means normally up to eight CLIPS of the same type can be used on a single I²C.

Some CLIPS devices, such as the PCD8571 RAM, receive or send several bytes of data in each transfer and these devices usually auto-increment their internal word address pointer after each byte, so such block transfers use the bus efficiently.

In the previous article the high speed, or normal mode of the I²C bus, has been discussed. The I²C bus specification also allows for a slow speed mode. This mode is to facilitate the driving of CLIPS devices by controllers not specifically designed to interface and control this bus.

In the low speed mode the serial clock is limited to 2kHz and the data format includes a START byte (01Hex) immediately after the start condition, and before the slave address, to indicate that the low speed mode is being used.

When using the MAB8400 range of microcontrollers for controlling the I²C bus, the following software functions should be included in the user's program.

First, a reminder of the special serial I/O registers being used: 'S0' is the data register connected to the bus, and data/address is clocked in or out of S0 on the rising edge of SCL.

'S1' is the status and control register:

ESO	BC2	BC1	BC0

Mst	Trx	BB	PIN

AL	AAS	ADO	LRB

'S2' is used to set up clock speeds, etc:

—	ACK	ASC	5 Clock speed bits

Within the normal initialization routines in the user's program, the initialization of the serial I/O is carried out, e.g.:

MOV S2,#h'43'

Clock at 87 kHz, with ACK.

MOV S1,#h'18'

Enable Serial I/O, slave Rx.

ENSI

(Enable Serial Interrupt if used)

When the main program calls the Serial I/O routine to read data from a slave, the address of the slave is sent out following the START condition, e.g.:

MOV S0,#h'A0'

Slave address — write mode.

MOV S1,#h'F8'

Send START and device address.

Wait for 'address sent' by polling PIN or serial interrupt as shown last month:

MOV S1,A

Check status

JB0 ERROR

Check for acknowledge (LRB = 0)

Now the 'command' or address pointer is sent:

MOV SO,#h'xx'

Send command 'xx'

and tests for PIN = 0 and LRB = 0 (ACK) etc. performed.

Having sent the command or pointer, it is now necessary to reverse the direction of the communication on the I²C bus.

Multiple starts are permitted within the I²C protocol so the slave address is transmitted again but this time with the LSB = 1 (READ).

Loading or reading S0 clears PIN and allows the SCL to restart so, if S0 is just loaded with 'slave address+read', transmission will start immediately as if this were data and it would be received by the slave as data. The START condition distinguishes 'address + R/W' from data bytes.

First the serial data, SDA, and serial clock SCL lines are released by:

MOV S1,#h'18'

Slave, Rx, BB =0, ESO = 1

This is not a STOP condition as the master is no longer a transmitter. First the SDA will go high. Then the SCL goes high and this action clocks the data into the last received bit of S1 so both SDA and SCL can be checked to see if they are high by testing S1 for LRB = 1, and it is then clear to create a fresh START condition: (see Figure 19).

9

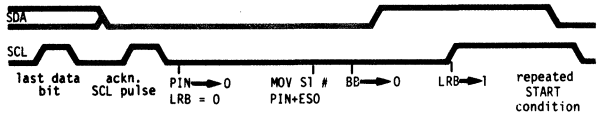


Figure 19. Testing Status Bits BB and LRB to See Whether the SCL Line has Been Released.

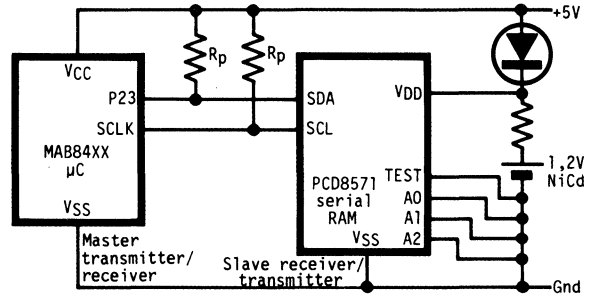


Figure 20. Block Diagram MAB84XX — PCD8571 Serial RAM Configuration.

Test
MOV A,S1 *Get status,*
JBO Restrt *LRB =1 so go to repeat start.*
JMP Test *Still waiting — try again.*
Now to turn bus round:
Restart
MOV S0,#h'A1' *Slave address + read*
MOV S1,#h'F8' *START — Master, Tx, BB = 1, PIN = 1, ESO =1.*

Though the MAB8400 sends this repeated start plus slave address in master transmit mode because the LSB = 1 (Not Write), the MAB8400 changes to master receive mode at the end of the byte. The addressed slave generates the ACK on the ninth clock and becomes a transmitter. The master checks for receipt of the acknowledge and then, to reset the PIN and allow clocking to continue, S0 is read, even though it just contains the slave address and read.

To read bytes of data from the slave the master receiver continues providing the serial clock, and on its ninth clock the master holds SDA low to acknowledge the receipt of the data. To clear the bus after each byte then:

MOV A,S0

reads the data, clears the PIN bit and allows the clocking to continue.

When the required number of bytes has been read by the master receiver, the master has to indicate this to the slave transmitter.

This is where the acknowledge bit comes in. The master is generating nine clock pulses for each byte and is pulling SDA low on the ninth. If the master receiver does not acknowledge but leaves SDA high on the ninth SCL, then the slave transmitter will cease sending data and will leave the SDA and SCL high also. This is a requirement of an I²C peripheral. Now a STOP condition can be generated by the master.

The MAB8400 is the first of a range of I²C bus controllers and the generation of the STOP condition in master receiver mode is fairly complex. Later controllers, already in development, have simpler solutions.

First, a 'not acknowledge' must be created. Before clocking the last data byte from the slave transmitter, the MAB8400 is set in the not acknowledge mode by clearing the ACK bit (bit 6) in S2:

MOV S2,#h'03'

(was 43 when initialized)

This is done before reading the penultimate byte from S0 in the master receiver. The MAB8400 will now provide eight clock pulses only to receive the final data byte. The slave transmitter is now waiting for the ninth clock pulse with SDA held low as an acknowledge. As the MAB8400 is in the 'not Ack' mode, after eight clock pulses PIN = 0 (and serial interrupt, if enabled) and the SCL stays low. The last received byte is now in S0.

One more clock pulse is needed with SDA left high so the bit counter in S1 is set for a word length of one:

MOV S1,#h'A9' *Mst, Rx, BB, PIN = 0, ESO = 0 & BC = 1.*

The clock is released as the received byte is read from S0:

MOV A, S0 *last byte to accumulator*

and the slave transmitter sees the 'ninth' clock with 'no Ack', as this READ will leave SDA high, so releases the bus.

The master checks that the single bit has gone out by checking for PIN = 0 (completion of transmission of the one-bit word);

GON MOV A,S1 *Get status*
JB4 GON *wait until PIN = 0.*

The 'with Ack' mode can now be restored and the STOP condition sent:

MOV S2,#h'43'
MOV S1,#h'D8'

This clears the bus so a new conversation can be started.

A practical example. Figure 20 shows the PCD8571 RAM connected to the MAB8400 microcontroller.

The PCD8571 is a 128 x 8 CMOS RAM and as it uses the I²C bus for both data and address, it is housed in an eight pin package. Three address pins are supplied to allow up to eight PCD8571s to be on the same I²C bus.

Access time is determined by the 100kHz maximum clock rate of the I²C bus specification. In power-down mode data may be maintained by a 1 volt battery from which it draws typically only 50nA.

A program for reading four bytes of data from the RAM is shown. This program was modified to read just two bytes and oscilloscope pictures of the serial data and clock lines taken. The composite picture is shown in Figure 21.

The serial clock frequency used is 87kHz and at this speed the time between each acknowledge and the restarting of the clock is significant. It is then that the check is made for Ack and the I/O register S0 is read. Faster I²C bus microcontrollers are in development which will reduce the time interval between successive bytes on the bus.

After the pointer has been sent and acknowledged, both SDA and SCL are low. The bus is cleared (both high) by the

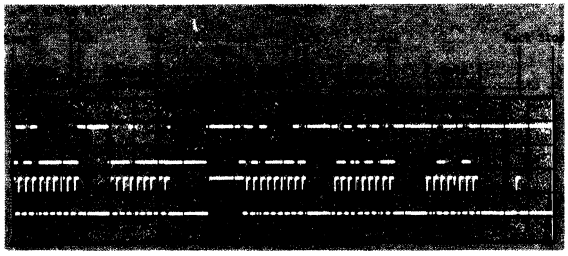


Figure 21. SDA (top) and SCL MAB8400 Reading Two Bytes from PCD8571.

MOV S1,#h'18' instruction (line 42 of listing) so the second start condition can be generated (line 48).

The eight clock pulse for the last data byte can be seen clearly; the rising edge of the delayed ninth clock pulse clocks the NACK into the PCD8571 to indicate the end of transmission. The SDA is left high and is then taken low by the MOV S1,#h'D8' instruction (line 77) when the STOP condition is generated (SDA low to high with SCL high).

A non-volatile memory (EEPROM) equivalent of the PCD8571 is being developed. This circuit, the PCF8572, has the same pinning and hardware address as PCD8571; it can be used as a plug-in replacement for the RAM. Naturally there are some differences for which allowances have to be made.

In the first place the single 5V power supply voltage has a more restricted range of ±10% and secondly the write cycle (ie, erase/rewrite) time is now significantly longer (10 ms/byte). As a consequence, the circuit will not accept more than two consecutive data bytes in the write mode, but otherwise the data format is the same as has been described above. Furthermore, the device is block-erasable. Finally, allowance has to be made for the inclusion of an RC-time constant at pin 7 which is not required in the RAM application.

Clock/calendar/timer: The PCB8573 is a real time clock/calendar circuit using a 32kHz crystal controlled oscillator and an auxiliary 1.2V battery to protect against power supply interruptions. The device has both addressable time counter and addressable alarm register for minutes, hours, days, and months. Access to the counter and the alarm register is via the I²C bus. Consequently, the circuit not only functions as a clock/calendar but also can be used for presetting a time and/or a date for alarm or remote switching function.

Figure 22 shows a block diagram of the circuit. In essence the timer function is provided by comparing the time-counter and alarm registers. When the contents are equal, a flag COMP is set. This flag is accessible either via the I²C bus or via an external pin. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set.

The data format of this slave transceiver follows the general format described above. Specifically, the control byte or mode pointer is divided equally into an upper control-nibble and a lower address-nibble.

The former is used to read or set the control and status flags as well as for seconds adjustment, whereas the latter is used to set or read the time counter or alarm register, i.e. selects hours, minutes, days or months. Each of the two registers is 24 bits long but four data bytes are necessary for complete data transfer to or from each register.

Remote 8-bit I/O Expander PCF8574.

The block diagram of this circuit is shown in Figure 4. The device was designed as a remote I/O expander for the 8400 and 84C00 families of 8-bit microcomputers but naturally it can be used to interface microcomputers without a serial interface. When used as an input device an interrupt line, INT is used to interrupt a master device on the I²C bus so that the PCF8574 remains a slave transceiver.

The I/O ports are quasi-bidirectional and thus can be used as inputs or outputs without the use of a control signal for data direction. Any bit designated as an input must be first loaded with a logic 1, although all ports are set to logic 1 automatically by the power-on-reset circuit.

Reading from and writing to the I/O ports follows the principles already outlined and, in doing so, it is only necessary to recognize that in a read cycle the inputs are latched in the same clock period as the acknowledge signal after the state address, and in the write cycle the outputs are latched in the acknowledge signal clock period after receipt of the data byte.

It has already been mentioned that the PCF8574 is a slave transceiver so, in the event of an input change, the device does not take control of the I²C bus to transmit the relevant information to the microcontroller but uses a separate interrupt request line. The microcontroller then takes action to read the port expander concerned. An interrupt is generated by any rising or falling edge at a pin which has been designated as an input. The interrupt signal (INT) is reset either when the data on the input in question returns to its original value or when data is read from or written to the port which has generated the interrupt.

```
1  ********************************************************************************
2  *               Routine for reading from PCD8571 CMOS RAM
3  *        via the I2C bus with MAB8400 microcontroller as Master
4  ********************************************************************************
5  * In this example of a single Master conversing with a responsive CLIPS device
6  * the Master sets up a pointer for the word address in the RAM, then becomes a
7  * Master Receiver to read from the RAM.  The Master indicates the end of the
8  * conversation by Not Acknowledge and, having become a Master Transmitter again
9  * puts out a Stop condition to clear the bus.
10 * For this example the data to be read is in addresses 10-13Hex in the RAM and
11 * will be stored in R30-33 in the MAB8400.
12 *
13 RAMR    asect   rom,inpage
14         page    256
15         entry   strt
16         org     0
17 strt    JMP     init            reset vector
18         org     09              clear of interrupt vectors
19 init    MOV     S2,8H'43'       with ACK, SCLK=87KHz.
20         MOV     S1,8H'18'       slave Rx,Enable Serial I/O
21 main    NOP                     Main program!
22         CALL    DAR             Call read data routine.
23         JMP     main            continue main program.
24 *
25 DAR     MOV     R0,8H'30'       pointer for read data to be stored.
26         MOV     R7,8D2          Counter for number of bytes to be read -2.
27         MOV     S0,8H'A0'       Address of PCD8571 (1010000) + Write (0).
28         MOV     S1,8H'F8'       START and send address
29 *                               -Mst,Trx,BB,PIN,ESO,8Bits.
30 bytA    MOV     A,S1            get SIO status
31         JB4     bytA            wait for PIN=0 ,(address sent)
32         JB0     ERROR           exit if no ACK.
33 * Address sent so now send word address pointer
34         MOV     S0,8H'10'       address of first word to be read.
35 bytW    MOV     A,S1            Get status                    ,
36         JB4     bytW            wait for PIN=0 (word address sent)
37         JB0     ERROR           Check ACK.
38 * PCD8571 now set up with pointer so change Master from Write to READ.
39 * SCL and SDA currently LOW as PIN=0 not yet reset.
40         MOV     S1,8H'18'       Clear Bus Busy bit to clear bus, PIN=1, ESO=1.
41 TestB   MOV     A,S1            get status
42         JB0     Clear           LRB=1 so clear to continue.
43         JMP     TestB           Still waiting for bus to clear - try again.
44 *
45 Clear   MOV     S0,8H'A1'       Address of PCD8571 + READ
46         MOV     S1,8H'F8'       START - Mst,Trx,BB,PIN,ESO,8Bits.
47 bytR    MOV     A,S1            Get status
48         JB4     bytR            wait for PIN=0
49         JB0     ERROR
50 * MAB8400 now a Master Receiver. To release the Bus clear PIN by reading S0.
51         MOV     A,S0            SCL can now run to fetch data from RAM
52 bytD    MOV     A,S1            Get status
53         JB4     bytD            Wait for PIN=0 (Data received.)
54         MOV     A,S0            Read data received and clear PIN.
55         MOV     @R0,A           store data away.
56         INC     R0              increment data store pointer.
57         DJNZ    R7,bytD         data byte counter>0, get more.
58 * Penultimate byte on its way.
59 bytP    MOV     A,S1            Get Status
60         JB4     bytP            wait for PIN=0
61 * Now change to No Ack mode to signal PCD8571 'end of conversation'
62 * Penultimate byte still in S0 and but is not moved until No Ack mode is set up.
63         MOV     S2,8H'03'       NO ACK, 87KHz.
64         MOV     A,S0            read data. PIN=1, SCL restarts.
65         MOV     @R0,A           store away byte just read.
66         INC     R0              increment data store pointer for final byte.
67 bytF    MOV     A,S1            get status
68         JB4     bytF            wait PIN=0 (final byte in S0)
69 * Final byte so a "No Ack" must be sent to RAM - a one bit word =1.
70         MOV     S1,8H'A9'       Mst,Rx,BB,PIN=0,ESO,BC=1
71         MOV     A,S0            read final byte and release bus for
72 *                               one bit word.
73         MOV     @R0,A           Store away final byte.
74 * Now check for one bit word transmission complete.
75 GON     MOV     A,S1            get status
76         JB4     GON             wait PIN=0
77         MOV     S2,8H'43'       restore "with ACK" mode
78 STOP    MOV     S1,8H'D8'       STOP
79 *               MAB8400 automatically reverts to Slave Receiver after STOP.
80 *
81         RET                     return to main program.
82 *
83 ERROR   JMP     STOP            IF ERROR - STOP
84 *
85         END
```

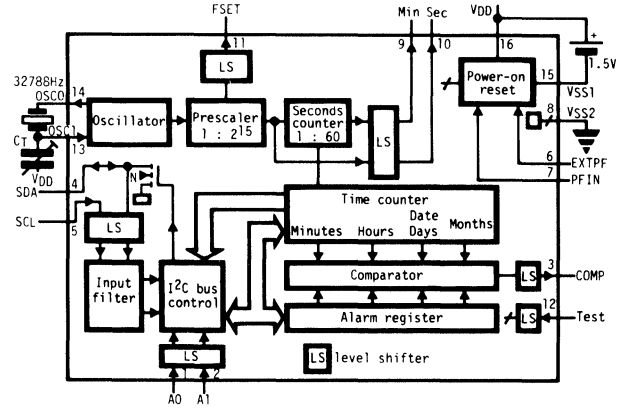


Figure 22. Block Diagram of the PCB8573.

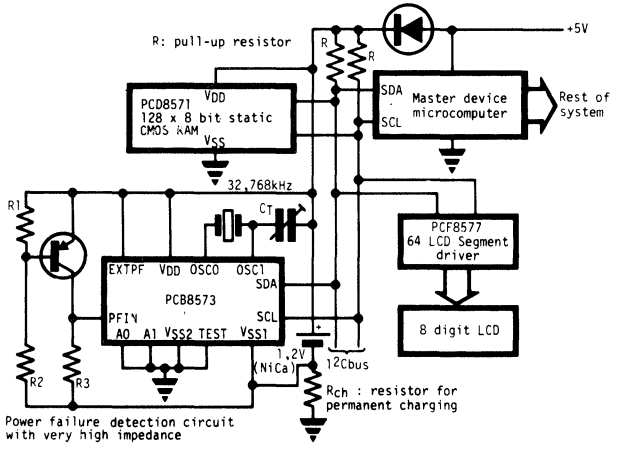


Figure 23. Application Example of the PCB8573.

In Figure 23 a typical application of the clock/calendar circuit the PCB8573 is shown. The most obvious point about this application is that this is neither the simplest nor the cheapest way of making a clock/calendar with an LCD display since there are several ICs capable of performing that function alone. However, in a system in which a microcontroller is performing a large number of other tasks, using its 8-bit wide ports, it will be simpler and cheaper to use a serial port to provide additional features and facilities, which do not require high data transfer rates, such as the clock/calendar function. This is because the costs of interfacing between the microcomputer and a separate dedicated clock circuit may be high. Thus the first application area is one of incremental facilities which in themselves may not be particularly expensive to provide in isolation, but might be to add to a more complex system.

A second related aspect of I^2C bus designs is that it allows for 'optional' facilities i.e. some equipments may require a clock, others not. A particularly good example of this is a facility phone shown in Figure 24, where a DTMF option can be readily added or the repertory dialing memory can be easily extended, simply by plugging in extra integrated circuits, e.g., PCD3312 and PCD8571.

The circuit shows the PCD3340 repertory dialer controller. This is a special adaptation in CMOS of the general purpose MAB8420 microcontroller to make it more suitable for telephone applications. It has sufficient RAM on board to store 10 repertory numbers and possesses redial and extended redial features. The microcontroller interfaces directly with a suitable transmission circuit such as one of the TEA1060 family and provides decadic dialing and register recall outputs.

This circuit, together with two LCD drivers, forms the starting point of a facility telephone with repertory and display features. To extend the repertory store, it is only necessary to add PCD8571 RAMs to the I^2C bus and, to add DTMF signaling, the PCD3312 tone-generator, described earlier, is 'clipped-on' the bus as well. Naturally there would be advantages in using EEPROMs instead of the RAMs.

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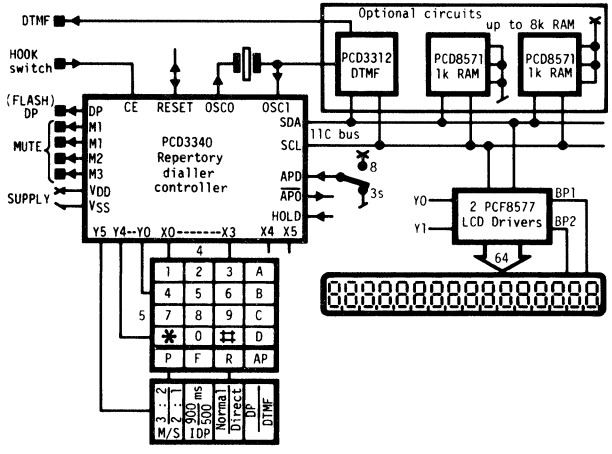

Figure 24. Repertory Dialing Facility Phone.

I²C Bus with Multiple Masters

Previously bus configurations with only one master have been discussed. An increasing number of applications use more than one master, either initially to divide the total system tasks or as extensions added to provide customer options.

In the latter case, as long as the original single master was programmed to accommodate the possibility of having to compete for the I²C bus, the additional masters can be added without modifying the program of the original master. This assumes that the added master is not required to communicate with the original master.

In a system designed with several masters the possibility arises that masters, competing for the bus, may be addressing each other so this must be allowed for.

Two or more masters may use the same bus just to drive their 'own' sets of peripherals or they may even share peripherals. The MAB8400 microcontroller, commonly used as a master, may also be

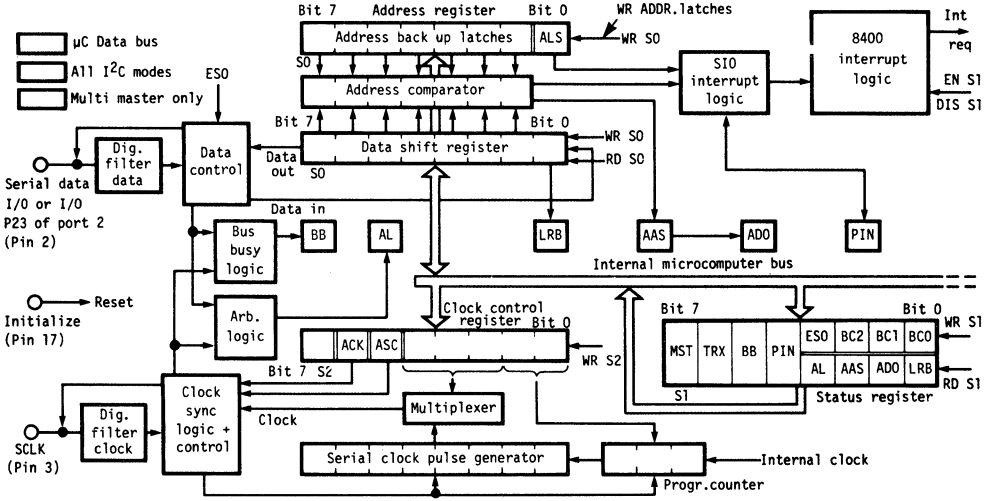

Figure 25. Block Diagram of the MAB8400 SIO Interface.

used as an 'intelligent' slave and can have its address loaded by software.

For the I²C bus to function with multiple masters, an arbitration system is required, and this section describes both the arbitration and the software control of a multi-master system.

The first section described how master controllers competing for the bus can recognize competition. As the connection to the bus is by open-drain MOS, with a common pull-up resistor, a LOW always overrules a HIGH and as the serial I/O pins are quasi-bidirectional, a device failing to get a HIGH bit onto the bus will be able to recognize that fact.

The second section showed the serial I/O section of the MAB8400, but, as this will be referred to in some detail, it is shown again in Figure 25.

Register S0' is used for the address of this device so it may be addressed as a slave. If a START condition appears on the I²C bus, then the address following it is fed into S0 and then compared with S0'. If the comparison is true, then PIN bit in S1 is set to '0' and, if enabled, the serial interrupt is asserted.

If the LSB in S1' is set to '1', this indicates the always selected (ALS) mode in which case the comparison of address is assumed true.

S2 operates as previously described and is used to set up the serial clock frequency and operating modes in the initialization routine.

The significance of each bit in the serial status register S1 requires more detailed explanation:

The master bit (MST) is set to '1', by software, when the interface is in the master mode, in which case this device provides the serial clock SCL. It may be reset by software, but will be reset to '0' if the device loses the bus in an arbitration contest.

MST	TRX	Operating code
0	0	'Slave receiver'
1	0	'Master receiver'
0	1	'Slave transmitter'
1	1	'Master transmitter'

Figure 26. Operating Modes Set by Bits MST and TRX.

The transmitter bit (TRX) is set to '1', by software in master mode, when transmitting. It can also be set to '1', in slave mode, when another master demands that data be transmitted by this device. It will be reset to '0' if arbitration is lost. Both MST and TRX are reset to '0' by a STOP condition.

The operating modes of MST and TRX are summarized in Figure 26.

The busy bit (BB) is set by hardware whenever a START condition appears on the I²C bus and it is reset by a STOP condition. When in master transmitter mode, it is set to '1' by software to create a START condition and reset to '0' to create a STOP.

Setting the pending interrupt not bit (PIN) to '0' initiates a serial interrupt, if enabled. As long as PIN = 0 the serial clock is held LOW. It is taken LOW by several conditions — a complete word has been transmitted, this device has been addressed or a complete word has been received. It is reset to '1' by reading from or writing to serial data register S0 or by direct operation on S1.

The enable serial output bit (ESO) enables the serial I/O. If ESO = 0 then the SCL pin is at high impedance and the SDA pin reverts to an ordinary port pin. Also, with ESO = 0, any data loaded by software into S0 is also latched into S0' thus enabling this device to load its 'slave' address.

The arbitration lost bit (AL) is set to '1' whenever this device transmits a 'high' onto the serial data line and this is overruled by a 'low' written by some other device, or noise. Setting of AL also resets MST and TRX. It is cleared by a MOV to or from S0 or S1.

The addressed as slave bit (AAS) is set to '1' when the comparison between the data received after a START and S0' is true, or anyway if the ALS bit in S0' is set.

The addressed by 0s bit (ADO) is set if an all zeros byte is received following a START condition, this being the 'general call' address.

The last received bit (LRB) reflects the state of SDA and is latched in by the rising edge of each SCL. It is normally used to check for acknowledge, as described earlier.

In the simpleset case of multi-masters the controllers only communicate with slave peripherals and not with each other.

After initialization, the user's program should include the following actions for controlling the bus.

When a potential master requires the bus, it must first check that it is free. As any other master currently using the bus must have put a START condition onto it, this will have set the bus busy bit within all potential master MAB8400 controllers. This can be checked by examining the status register S1:

```
MSTX MOV A,S1          Get status
     JB5 MSTX          Bus busy so try again.
```

BB can be checked indefinitely or, if the system involves lengthy bus useage, for a finite time before withdrawing to try later.

Having established the bus is available, the slave address is loaded into S0 ready for transmission. S1 is then loaded to create a START and send out the slave address.

```
MOV S0,#SLAD  Load slave address into S0
MOV S1,#H'F8'  Mst, Trx, BN, PIN, ESO.
                — START.
```

In the interval between checking BB and sending out a START, another master may have put a START onto the bus. The serial I/O hardware of the MAB8400 will recognize this START and automatically prevent a further transmission of a START. In this case the MST and TRX bits will be reset to '0' and the AL bit set to '1'.

If a competing master sends out a coincident START, then both potential masters will send out the slave addresses. The clock arbitration circuit on the MAB8400 ensures that an effective SCL results from competing masters. As the bus ensures that LOWs overrule HIGHs, the lower, numerical value address will succeed at some stage. At this moment the device sending out the higher address will immediately cease putting data out. The MST and TRX bits in the loser will be reset to '0' and its AL set to '1'.

At the end of this first byte the status register is examined just as in the single master configurations described earlier. Examination of the MST bit will show if the transmission was successful and the LRB bit will show if the addressed slave has acknowledged.

```
MOV A, S1              Get status
JB7 MSTR               Still master?
RETR                   Return
                       (If serial interrupt used)
MSTR JBO ERROR         Check for
                       acknowledge . . . (0 = O.K.)
```

Communication now continues as with single master and the final STOP condition will clear the BB bit in ALL the I²C bus controllers.

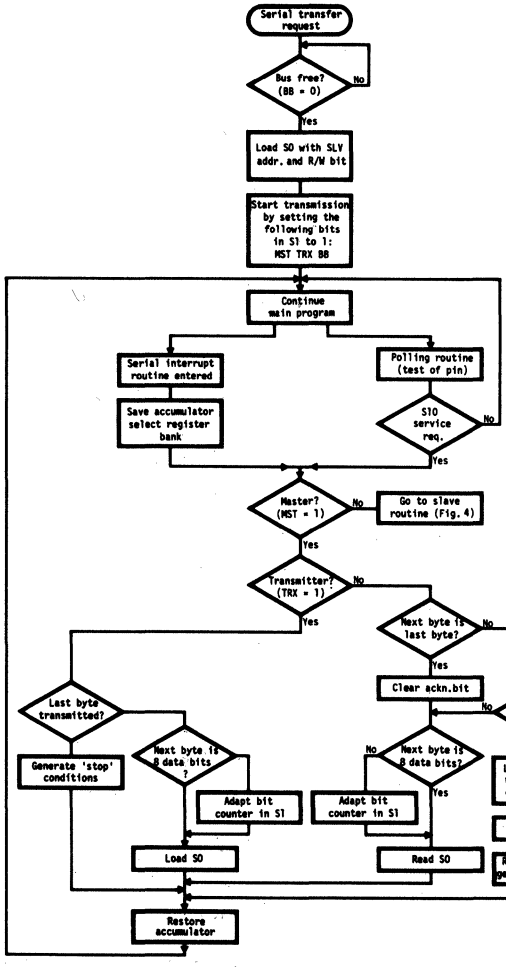

Figure 27. Flow Chart of the 'Master' Mode After Initialization.

If the system uses two or more MAB8400 communicating with each other, as well as the CLIPS peripherals, then different procedures are necessary.

First, before the serial I/O is enabled, the MAB8400 loads its own address into S0':

```
MOV S0,#OWNAD      Load own address
MOV S1,#H'18'      PIN + ESO
```

Now, just as before, when this master requires the bus, it checks BB and then sends out a START and slave address.

However, when checking S1 after transmission there are more possibilities.

Just as before check to see if this device is still a master:

```
MOV A,S1           Get status
JB7 MSTR           Still master so continue from MSTR.
```

If this device is no longer the master, the reason is determined and a jump is made to the appropriate subroutine. Bit 3 will indicate that arbitration has been lost:

```
JB3 MSTAL          Master lost arbitration
```

At MSTAL S1 is further examined to see if this device was addressed as a slave; if not, the program returns to its main activity ready to try for the bus again.

```
JB2 ADDSL          Addressed as slave
JMP CLEAR          CLEAR reads S0 to clear the bus and PIN before returning to main program.
```

It is possible for a losing master to recognize its own address, despite trying to transmit another, as before the address bit where arbitration is lost the transmitted bits are returned into the LSB of S0. Subsequent address bits on the bus follow into S0 so the 'winning' address always appears complete.

At ADDSL a further test of S1 will indicate whether, as a slave, this device is now a receiver or a transmitter.

```
JBC SLVTR          Slave transmitter routine
```

If the test fails, then this device must be a slave receiver and should behave just as any CLIPS peripheral described previously.

There is just the possibility that the general call address (all zeros) was used and this can be checked by examining bit 1 of S1. If true, then successive bytes will indicate to receivers what to do. This facility is available for controlling hardware masters in a multi-master configuration with a mixture of software controlled and hardware masters.

Once all the checks described above have been completed, the current configuration of the bus, one master and one slave, is clear and procedures continue as for a single master situation described previously. Figure 27 illustrates the decision tree for a master and Figure 28 for a slave, but not including general call.

In some applications the I^2C bus may be subject to occasional interference, e.g., flash-over of a TV tube. The MAB8400

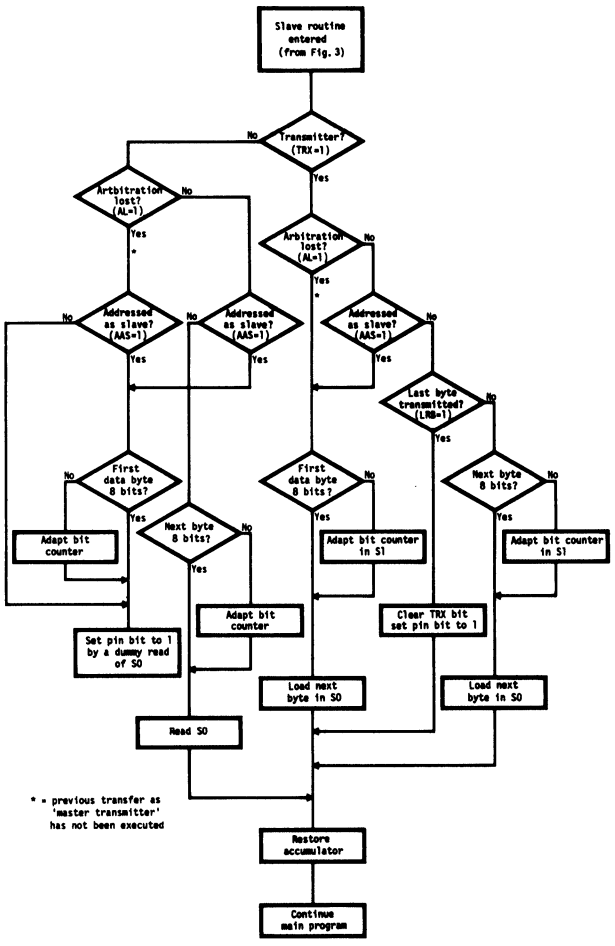

Figure 28. Flow Chart of the 'Slave' Mode After Initialization.

provides some resistance to interference by means of a digital filter on the SDA and SCL inputs. This prevents spikes less than about 1/2 microsecond getting through. However, the consequences of bus disturbances should be considered and, when possible, recovery procedures included in the program.

Disturbances can, of course, occur on either or both SCL and SDA, but as the effect is similar it will be assumed SCL is undisturbed and SDA is corrupted.

If SDA should be high and is transiently forced low, the significance depends on the state of SCL.

If SCL is low, then SDA being forced low is the same as losing arbitration. In a single master configuration it is therefore advisable to check for this despite not having to compete for the bus. The master must then clear the bus and start again.

If SCL is HIGH, then the HIGH to LOW transition of SDA is a repeated start condition and 'new address' will be on the bus. The normal S1 checks should reveal this and the master will create a STOP and try again.

If SDA is properly LOW and forced HIGH when SCL is HIGH, then a STOP condition has been created so the bus will be cleared.

An effective way of handling these situations is to check on the time that PIN = 0 before it is reset. If excessively long then the bus should be cleared by a STOP. In really extreme cases, possible where the I²C bus is not most suitable, all masters could create a STOP and clear the bus at regular intervals. In such a case messages would be repeated and the data rate on the bus would be low; however it has been shown that this bus can be used effectively in hostile environments with recovery routines operating.

Two classes of multimaster applications will now be considered. At one extreme is the category where full use is made, at the outset, of the bus protocol for distribution of control amongst several microcontrollers. These master-transmitter devices communicate with each other and with a set of shared peripherals. One such application which will be considered is a local area network (LAN) terminal.

At the other extreme is the case where a new feature is added to an existing system which may not have been contemplated at the outset of the design and accordingly the new devices added to the bus may or may not communicate with devices already on the bus; two examples of this type of application will be considered first.

One of the most powerful features of the I²C-bus protocol is that it allows the addition (or subtraction) of components to (from) the bus without the need for major redesign of the system; i.e., a clock or a display may or may not be present. Usually, of course, all the relevant software will have been written in the master controller. It is perhaps natural to assume that all the required functions have been accommodated in the original design and the various production options merely require the inclusion or omission of the different peripheral types.

Furthermore, it has probably been assumed that there is only one master controller and that, therefore, the bus is always available to it. In such a situation the bus-busy bit is probably not interrogated in the original software and bus crashes could be anticipated if another master device is added to the bus. It is

therefore prudent, if possible, to check the availability of the bus, even in single-master applications, since this does allow increased flexibility should a new feature have to be added.

Additional Controllers

If as an afterthought it becomes necessary, for example, to display particular data which are available in a slave receiver such as a memory or I/O port, it is a straightforward task, assuming that the relevant data locations are known, to write the appropriate software for a separate master controller and associated display driver.

Care must be taken to ensure that the memory device pointers are returned to their initial addresses to ensure that the original microcontroller is unaware of the system additions. It is conceivable that in some situations the nature of the addition does require the modification of the data base, but, naturally, the interaction with the original controller is indirect and very limited in scope.

A second application concerns the modification of a system function, for example, continuing the display theme, the case of changing from an LED to an LCD driver or or modifying the data displayed on the same display. In this application the commands and data from the original microcontroller are intercepted by replacing the original slave peripheral with a microcontroller having the same address. The data is added to, and/or manipulated by, the second controller and retransmitted to a new peripheral or to the same peripheral with a new externally programmed address. Again the original controller is unaware of the system changes.

These examples, while they may be very useful in accommodating real-life changes, are in fact pseudo-multi-master applications and do not take into account the full capabilities of the I²C-bus. An example of a genuine multi-master application now follows:

Local area networks (LANs) are designed to provide for efficient data communications for a local environment such as a single building or office. Several standards have been proposed and, although it is outside the scope of the current article to provide any justification, it is possible to demonstrate that emphasis on efficient data transfer has led to proposals which are not especially suitable for applications in which efficient transfer of 64kbits/s digitized speech is as important as efficient data transfer.

Accordingly, with this and the development of integrated services digital networks (ISDN) in mind, a new integrated services terminal bus (IST-bus) suitable for the local transmission of digital voice, text, image and data on a single twisted-pair cable has been proposed. The bus may be used to provide a completely distributed switching system for up to 30 terminals.

A generalized application of the IST bus is shown in Figure 29, and various types of terminal are depicted, each of which contains three parts:

- a microcontroller
- an IST-bus interface circuit
- a service module (voice, text, image, etc.)

All three sub-systems are interconnected, for control purposes, by the I²C-bus. (Incidentally the other bus shown is a terminal highway (THW) over which 64K bits/s circuit switched channels are transmitted to and from the IST-bus and the service modules). In the event that connection to an external network is required an additional interface circuit, as shown in Figure 30, is required. Once again control data is transmitted via the I²C-bus.

For the purpose of this article, the first significant point is that the use of the I²C-bus for control purposes permits the construction of a complete range of stations from a limited number of dedicated IC's, together with the general purpose microcontrollers, RAMs, LCD drivers, etc., which have been described in previous sections (see Figure 31).

Secondly, because the I²C-bus carries the control information necessary to establish an inter-terminal connection on the IST-bus, and, in the case of a gateway station, the signaling and control data for another networks, a single master-microcontroller would be unable to cope.

Furthermore, when using a multi-master approach, it is important to recognize that there is a limit to the amount of control

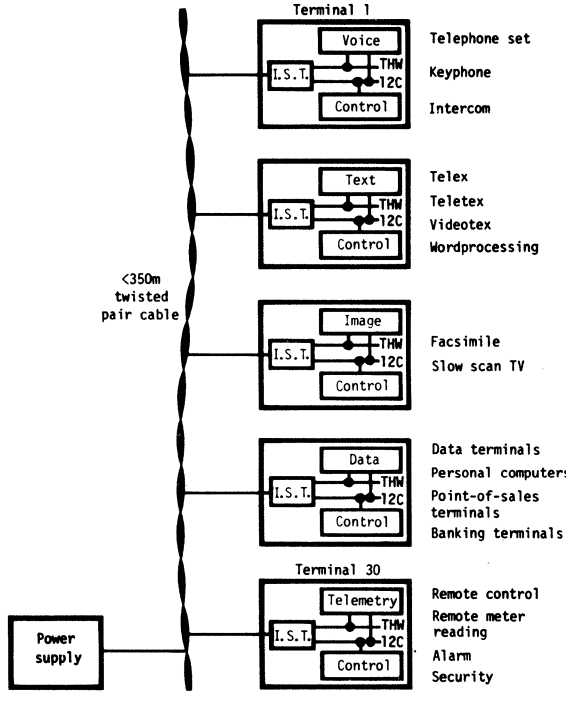

Figure 29. The IST Bus Concept.

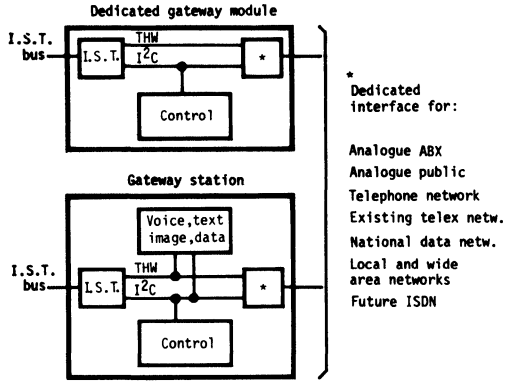

Figure 30. Interfacing to External Network.

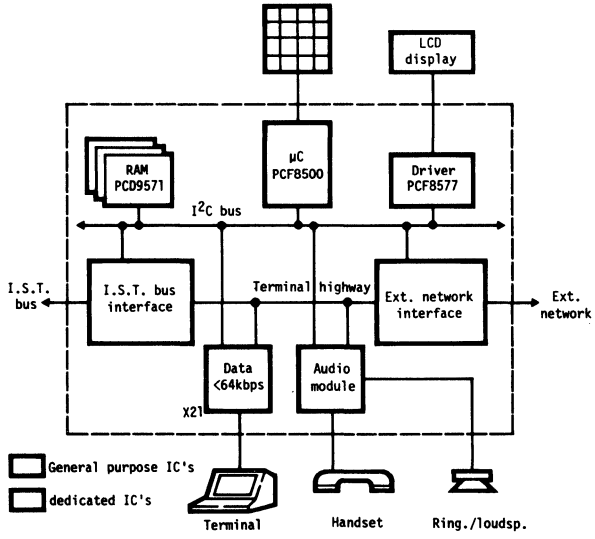

Figure 31. Complete Range of Stations from a Limited Number of Dedicated IC's.

information that can be handled by the serial bus.

Extreme Case

Accordingly, in this example, which is indeed an extreme case, the dedicated sub-master circuits poses a high degree of autonomy and intelligence. For example the IST-bus interface circuit performs all the functions needed to establish a link between terminals, including the retransmission of control messages if necessary (i.e., it performs all the relevant OSI layer 1 and 2 functions). This allows the station controller to contend with overall terminal control functions.

This has attempted to show that a well specified serial data bus for Inter-IC (I^2C) communication is capable of leading to a range of flexible but structured designs based upon a growing family of 8-bit microcontrollers, general purpose peripherals, and/or application dedicated circuits. Furthermore, the availability of a range of CMOS gate arrays with an I^2C-interface permits customer-specific circuits to be designed as well.

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Twisted-Pair Bus Carries Speech, Data, Text, and Images

AN167

If any one characteristic can be said to dominate currently available local-area networks, it is efficient data transfer. That is all well and good, except for integrated communications networks, where traffic consists mainly of digitized speech. In the foreseeable future, in fact, speech traffic will become increasingly important, so that communications networks will have to be as efficient in transferring digitized speech as in transferring data.

In addition, a digital network for general-purpose communication must be able to transmit other types of information as well; interface easily with telephone sets and existing networks; use a low-cost transmission medium; and of course connect to almost all types of equipment commonly found in factories, offices and so on.

All these requirements are met by the Integrated Services Terminal (IST) bus, which forms a low-cost local network for transmitting digitized speech, data, text, and facsimile copies. A serial bus, it conforms to the seven-layer Open Systems Interconnection reference model of the ISO and uses twisted-pair cable to carry 64-kbit channels synchronized to the 8-kHz speech sampling frequency.

The IST bus provides distributed switching and control and offers several major benefits over current telephone, intercom, and small PBX systems. It can be interfaced with larger networks such as digital or analog PBX, public telephone, Telex, and data networks, and higher-performance (local and wide-area) networks.

The first applications will be for small, internal communication systems that primarily handle speech. Here, subscribers require very few lines (often only one) to the public network, and the IST bus will form an economical and versatile communications medium. In addition, the bus's data, text, and telemetry facilities will allow factories, offices, retailers — and even consumers — to connect telephone sets, personal computers, intercoms, word processors, and viewdata and point-of-sales terminals, as well as lighting, heating, and security equipment.

Twisted-pair Cables

The twisted-pair cable of the bus gives high speech and data transfer rates at low cost for the wire, installation, connectors and coupling transformers. The transmission speed is 1.024 Mbits/s, the maximum bus length 350 meters. Depending on the type of cable used, the characteristic impedance of the line can be between 100 and 150 Ω.

Each station is connected to the bus by an interface circuit and has a microcontroller, called the station controller (Figure 1.). The only other circuits needed are those which provide the services at each station.

As many as 30 stations may be connected either in a cluster or spread along the cable, and a dc power supply can be connected directly to the bus to provide up to about 0.5 W to each station. A small transistor splits the dc supply and the digital bus signals. Alternate mark inversion (AMI) line code, which reverses the polarity of each successive 1 to ensure no dc component, prevents the coupling transformer from distorting the signals.

Both circuit-switched and packet-switched data can be transmitted across the bus. In a circuit-switched channel, a connection between the calling and called stations is established for exclusive use of the circuit until the connection is released (as for a telephone call), whereas in a packet-switched channel the connection between stations exists only while each individual packet is being transmitted.

The data on the IST bus is time-multiplexed into frames that are synchronized to the standard 8-kHz speech sampling frequency, making for easy and inexpensive connection to public and private digital networks. Each frame is 125 μs long and is divided into 10 channels, one for 8-kHz frame synchronization; one 64-kbit/s half-duplex channel for control, signaling, and packet-switched data; and eight 64-kbit/s half-duplex channels (or four simultaneous duplex) for speech and circuit-switched data. In one frame, each occupied channel begins with a 1 (the start bit), followed by a single word comprising four bits for the frame synchronization channel and eight bits for each of the other channels.

The 32-kbit/s frame synchronization channel (f) carries a four-bit frame word (0011), which is transmitted by one of the stations on the bus every 125 μs to synchronize all stations to the 8-kHz speech sampling frequency. During power-on, a synchronization procedure selects the station that will transmit the frame word. Each station has a unique five-bit address, and each begins to count up from that address; the first to reach 00000 takes over as the master station (that is, begins to transmit the frame word). If this station later fails or is removed from the bus for any reason, another station will take over as master.

If any station needs to make an external call, the bus must be synchronized to the PBX or public network. Stations with links to exchanges have higher addresses (a sixth address bit is hard-wired on the station) and consequently take priority in becoming masters over other stations.

Besides overall synchronization, the synchronization procedure also ensures that there is no corruption of the data when equipment is plugged onto the bus, because a station can only begin to transmit data once it has been synchronized.

The Circuit-Switched Channels

The eight 64-kbit/s channels that carry digitized speech and circuit-switched data to and from the stations are designated b_1-b_8. Stations take control of vacant circuit-switched channels as needed. Two halves of a duplex phone call between two stations may, for example, be carried on channels b_3 and b_8, while those for a call between two other stations may be located on channels b_4 and b_6. Routing for the calls is performed by the relevant station controller using the station's IST bus interface circuit.

The packet-switched channel (bd) has three main uses: to arbitrate between stations wishing to make a connection to the circuit-switched channels, to set up the physical links that will transfer the circuit- and packet-switched data between stations, and to transfer packet-switched data and telemetry information between stations. It uses a protocol similar to the ISO's High-level Data Link control.

The channel's access method keeps retransmissions and access delays to a minimum for efficient packet transport. It is based on CSMA/CD (carrier-sense multiple access with collision detection), which allows network control to be fully distributed. CSMA/CD uses the principle "listen before and during transmission" to access the bus. All stations monitor the signals on

The Rules for Control and Message Packets

The IST bus uses a protocol for its packet-switched channel that closely resembles HDLC (High-level Data Link Control). One important difference is that each byte of data transferred over an IST bus channel is preceded by a 1 (the start bit), as long as information is transferred in a channel, whereas HDLC uses flag bytes to indicate the start and end of a data packet. Another is that the first bit of the first byte indicates whether the message being transferred consists of information (1) or control (C) characters (see the figure).

Control characters are transmitted by a station in the form of a seven-bit frame control message (FCM), the main uses of which are to arbitrate between stations wishing to make a connection to the eight circuit-switched channels and to set up the physical link (layer 1 of the ISO's seven-layer reference model) between the stations.

Before connecting to one of the circuit-switched channels, a station must first take control of the packet-switched channel by transmitting a frame control message (to prevent circuit-switched messages from colliding). Once a station has transmitted this message, it occupies over one or two vacant circuit-switched channels, depending on wheter the connection is half-or full-duplex.

A station will also place a frame control message on the bus when it wishes to make an external call. The master station decodes this message, "wakes up" the link to the exchange, and synchronizes the IST bus to it. Once the transmitting station has finished the call, it sends another frame control message to the master, which disconnects from the exchange.

If the first bit of the first byte indicates an information message, the following five bits form a destination address and the last two bits are unused. The second byte contains a message service indicator for the controller of the receiving station, of which the first bit specifies whether a signaling or data message follows; the remaining seven bits indicate further message type identifications, for example, call setup messages or response messages. On this byte, the controller can also decide to take the message or route it to another I^2C bus member.

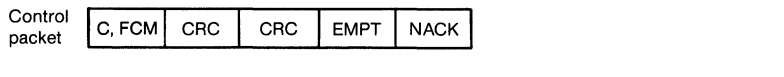
The subsequent data bytes carry the actual information in the message being transmitted (signaling information, display information, packet data, and so on). The number of data bytes in a message is limited only by the buffer space in the stations' IST bus interface circuit.

For signaling messages, the data bytes give the information used to establish and cancel circuit-switched connections. A telephone call or circuit-switched data transmission on the circuit-switched channels is therefore preceded by one or more signaling messages on the packet-switched channel to establish the connection; after the call or transmisison is finished, signaling messages are sent to release the connection.

All packet-switched data and telemetry transfers between stations use data messages. Such messages would establish a packet-switched connection between terminals, serve as a "wake-up call," or signal the start or end of a packet transport. The data bytes in this message would consist, for example, of packets between Telex terminals, between V.24 (RS-232) or X.25 stations (personal computers or word processors), between remote control equipment, or between telemetry equipment.

After each control of information packet, two CRC (cyclic-redundancy-check) bytes are transmitted for error detection. The end of a transmission is indicated by an "empty" byte, which is simply the absence of start and information bits. After this byte, any station that was unable to receive the message can transmit a "not acknowledged" (NACK) byte (11111111). It will do so if an error was detected, if the station's buffer was full, or if there was a collision between two or more transmissions that destroyed the information. The negative acknowledgment allows broadcast calls to be made (one station transmitting to all others, using the destination address 00000).

If a not-acknowledge signal is detected, the IST bus interface circuit retransmits the message, relieving the terminal from the software burden of retransmissions.



C = "control" bit
FCM = 7-bit frame control message
s/d = signaling or data bit
Data = data being transmitted
EMPT = empty byte

I = information bit
DEA = 5-bit destination address
MSI = 7-bit message service indicator
CRC = cyclic-redundancy-check byte
NACK = not acknowledged byte

Twisted-Pair Bus Carries Speech, Data, Text, and Images

the bus, and any unit can begin transmission as soon as the bus is free (CSMA). If two or more units begin to transmit simultaneously, they detect that fact (CD) and retire from the bus.

During message transmission, signaling and frame control messages have a higher priority than data messages. If, for example, two signaling messages and three data messages were to try to simultaneously access the bus (an improbably high number, even with 30 stations), the signaling messages would be transmitted first, followed by the data messages.

Message errors and collisions are resolved by an access protocol that prevents continued collisions from occurring. This protocol — unlike that of Ethernet and many other CSMA/CD networks — guarantees that a station will gain access within a certain time; if the message suffers three successive retransmissions (because the destination station was unable to receive the message), the bus interface warns the station controller, which takes the appropriate action.

Access delay to the packet-switched channel is low — less than 250 μs — if the channel is idle. If the channel is occcupied and no collision occurs, the worst-case access delay is the maximum packet length of the station currently occupying the bus plus 2 ms.

Gateways can connect the bus to analog and digital PBXs, public Telex and data networks, and other local networks. The interface is particularly easy to implement if the larger network is an integrated services digital network (ISDN), because the bus has been designed with such networks in mind. Furthermore, the bus can be connected to a PBX to particular advantage.

The traditional star configuration of a PBX is reliable but rather costly (each station requires an interface and twisted-pair cable to the exchange). In addition, it cannot be extended easily. Large bus systems, on the other hand, are easy to extend and, because of today's VLSI technology, can use low-cost interfaces. A bus network, however, is very sensitive to bus failures, which can moreover be difficult to locate.

An Island Cabin

Small, local IST buses connected to a PBX give the advantages of both bus and star networks with none of the attendant disadvantages. The IST bus can simply be connected in place of an existing PBX telephone set; the resulting network has the

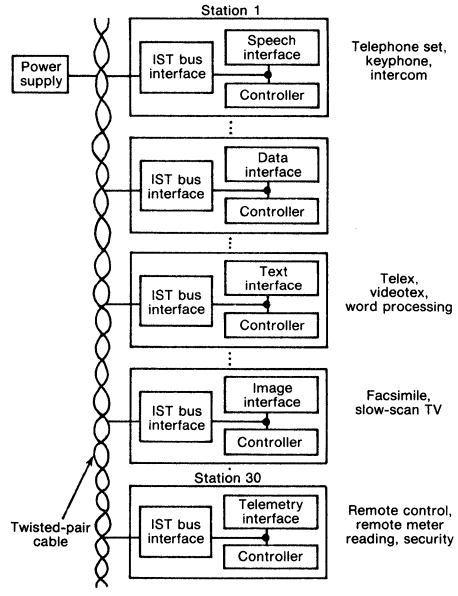


Figure 1. The IST bus serves speech and data transfer, carries up to 30 stations and can easily be interfaced to larger networks. The twisted-pair cable can supply dc power to the stations on the bus.

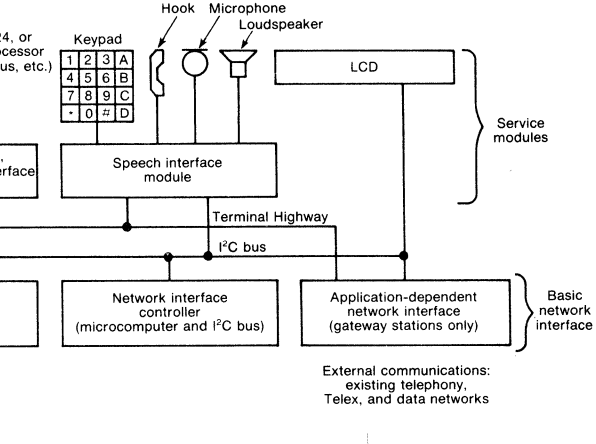


Figure 2. In this modular setup for telephones and data terminals, the interfaces between the various ICs are standardized by means of the I²C bus and the terminal highway. The lower part services the network interface, the upper part the speech and data services.

reliability of a PBX and is also inexpensive to implement (much of the existing PBX wiring can be used).

The networks connected by the bus function as speech and data "islands" passing information between telephone sets, data terminals, building energy-control equipment (lighting, heating, and ventilation), and security equipment. This island configuration is very flexible and can be easily extended.

A station connected to one node of the bus can range from a single digital telephone up to a computer with peripherals. In addition, the station can incorporate network interfaces to connect to other computers, local networks, and the exchange. The modular architecture (Figure 2) will allow a complete range of stations to be built up from a few dedicated ICs, together with general-purpose microcomputers, RAMs, LCD drivers, and so on.

The two major interfaces in this architecture are the inter-IC (I^2C) bus and the Terminal Highway (THW). Together, they guarantee a well-structured station architecture with easy, smooth expansion from simple systems up to intelligent data terminals with integral speech services.

The I^2C bus is a two-wire multiple-master bus for transferring data and control information between integrated circuits (*Electronic Design*, March 31, 1981, p. 69A). Its maximum specified transfer speed is 100 kbit/s (for synchronization reasons, the maximum transfer rate for interfacing with the 8-kHz synchronous IST bus is 64 kbit/s). The multimaster feature of this bus makes distributed system control possible and is therefore very powerful for use in ISDN telephone sets and ISDN interfaces for personal computers and data terminals. The bus carriers the information transfer to be received or transmitted across the packet-switched channel. This information includes signaling, telemetry, and packet-switched data, as well as control information between the station controller (which has an on-chip I^2C bus interface) and other ICs in the station. In a gateway station, the information is similar.

The Terminal Highway is a standard 2.048-Mbit/s 32-channel PCM highway that is compatible with those used in digital telephone switching equipment. In an IST bus station, it provides connections between the various circuits in the station, such as the station controller; the IST bus interface circuit; and the ICs in the speech, text, image, and/or data interface modules and network interface(s). Access to the THW is assigned via the I^2C bus by the station controller, which switches the 64-kbit/s channels of the various circuits to the required THW channels.

The IST bus interface circuit performs all functions needed to establish a link between stations and to transfer information and control messages over the packet-switched channel between two or more stations, including retransmissions. It therefore relieves the station controller from OSI layer 1 and 2 functions. The circuit is controlled, and data entered, via the I^2C bus, which can function as an interface medium to layer 3. This layer is actually located in the software of the station controller, or it can be part of the service modules.

A station will be connected to the bus using this IC and a small coupling transformer (Figure 3). The transformer provides a convenient means of supplying dc to the stations and also affords a high resistance to induced common-mode signals, important in industrial environments. Some additional components are required when the station is supplied dc via the bus — for example, a polarity guard bridge to prevent incorrect installation and a dc-dc converter to convert the varying dc bus voltage (approximately 20 to 50 V) to a stable 5-V station supply.

To reduce the implementation costs of an IST bus system, the interface circuit will be integrated onto a single chip. (Samples are planned for mid-1985). It will incorporate a dedicated microcontroller, a 256-by-8-bit RAM, and a PLA (programmable logic array). On-chip layer 1 circuitry will interface the IST bus with the THW and the I^2C bus and layer 2 functions will be implemented in the control section's PLA.

To keep system costs low, the interface chip will integrate several additional circuits. These include a 8.192-MHz crystal-controlled oscillator, a choice of a 4.096- or 8.192-MHz clock output (to provide the clock for other station ICs), a 2.048-MHz Terminal Highway synchronization output, and the control section of the station's dc-dc converter. For synchronization with other digital networks, the IC will also have an 8-kHz external synchronization input.

The timing section of the interface chip will also take care of any cable delays. Once a station gains access to the packet-switched circuit-switched channels and begins transmitting, the receiving station must be synchronized to it. Although each station is synchronized to the 8-kHz frame word at the beginning of each frame, there will be a cable delay between transmitting and receiving stations. The bus interface IC therefore allows for a 4-μs reception window, which accounts for the maximum cable length (5 ns/m x 2[400 m]); as soon as it receives the start bit, the chip syn-

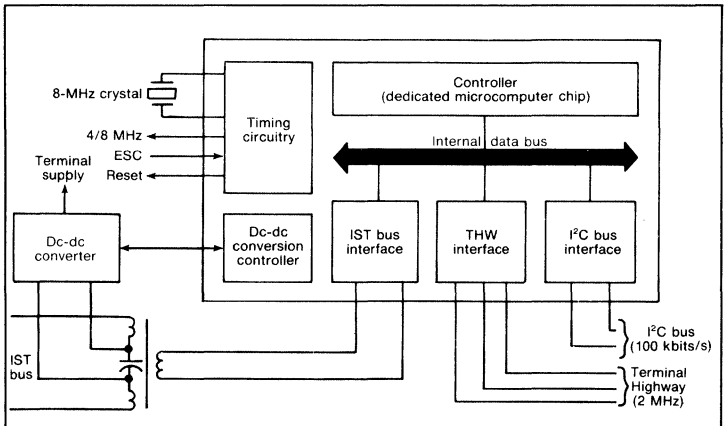


Figure 3. In the one-chip IST bus interface, layer 1 functions — such as for the I^2C bus, THW, and IST bus — are performed by dedicated hardware. Layer 2 funtions are programmed into the memory of the special on-chip microcontroller. The chip includes a 256-by-8-bit RAM for message storage and housekeeping.

chronizes to it to permit reception of the attendant byte.

A 1-Mbyte/s data bus in the IC will connect the layer 1 circuitry to the chip's controller. Packet-switched data and control signals will be routed via this bus to the various sections of the circuit.

Thirty-two RAM locations will be used for internal housekeeping, the remainder providing four bd channel buffers. The size of each of these buffers will be programmable by messages across the I^2C bus interface during system initialization. Two buffers are used to transmit and receive the signaling messages to and from the bd channel, and two to transmit and receive data packets.

The station controller can route information into two additional header buffers, allowing the interface chip to route incoming signaling or data messages to other ICs in the station independently of the station controller.

Putting It All Together

The IST bus interface circuit simplifies the designer's job of connecting the terminals of an internal communications system to an integrated services digital network. As stated earlier, it takes care of all layer 1 and 2 protocols, and the designer needs to know only the protocol used on the I^2C bus, which serves as an interface between layers 2 and 3. The network controller, which can be one or more standard microprocessors, will incorporate the software for layer 3 and higher layers.

The microprocessor adds the routing addresses to calls and routes incoming signaling messages and data packets to other terminal circuits such as the terminal's display, the data modules, or in case of a gateway, to the interface circuit of another network.

The terminal controller's software modules include call setup and breakdown routines and initialization routines that cause the terminal circuits to initialize at power-on.

The initialization procedure for the IST bus interface circuit will be performed mostly by the chip itself; it resets all internal registers and RAM locations after power-on. During this process, which takes about 4 ms, the Reset output is kept high. If this output is connected to the Reset input of the terminal controller, the program counter of the controller will be kept at zero.

After the reset process is finished, the terminal controller starts the initialization program to load the IST bus address of the terminal; set the sizes of the on-chip signaling, message, data-packet transmission or reception and routing header buffers; and initialize the IST bus. The IC then does the rest automatically. If another terminal begins to transmit the frame word, the chip will lock its synchronization circuitry to the IST bus; otherwise it will itself start to transmit the frame word and then become available to set up connections on the bus.

The use of an interface circuit implementing layers 1 and 2 makes terminal design more of a software than a hardware job. Like the terminal architecture around the I^2C bus and the THW and the architecture of the IST bus interface IC, the software of the network or terminal controller will be modular. When the software modules become available for standardized call setup procedures and routing routines, life will be even easier for the terminal designer.

Single-Chip Synthesizer for Radio Tuning AN196

J. MATULL and J. VAN STRAATEN

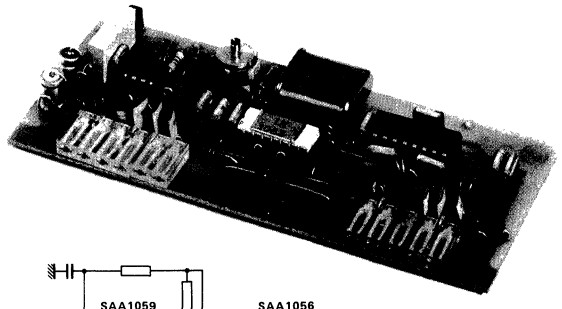
To remain competitive, manufacturers of domestic radios must not only produce a comprehensive range of reliable equipment with the required performance at the right price, but must also meet the needs of the market with regard to styling, ease of operation and available functions. Although the widespread use of integrated circuits has allowed vast improvements of performance and reliability and has increased the range of available facilities, the integrated circuits are not always optimally matched, resulting in partial redundancy and a large number of peripheral components. We foresaw this problem and were able to avoid it by using a total systems approach to manufacture our comprehensive range of ideally matched integrated circuits for signal processing and digital control of tuning, displays and analogue functions in all classes of radio. We can now therefore devote our design resources and considerable knowledge of integration technologies and techniques to reducing radio manufacturers' development and assembly costs by minimising the number of integrated circuits needed to implement the wide range of features and facilities required in today's radios.

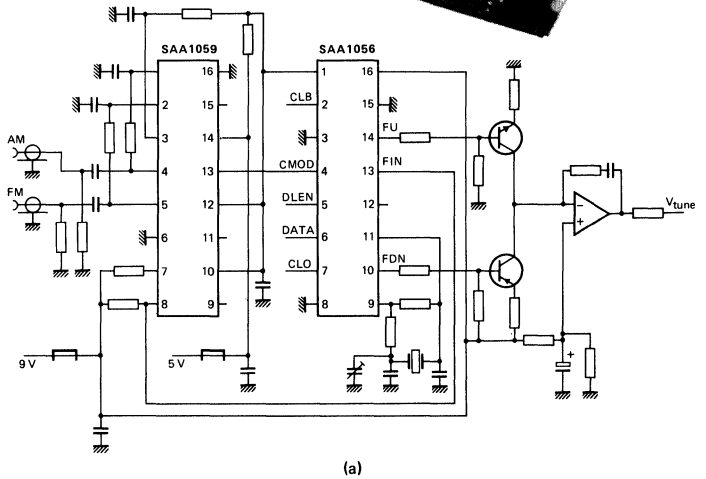
If a radio must incorporate facilities such as search tuning and/or tuning by direct entry of frequency at a keyboard, variable-capacitance diode tuning must be used and a stable local-oscillator signal can be generated by indirect frequency synthesis with a phase-locked loop (PLL) controlled by a microcomputer. This system was fully described in Ref.1 which showed how integrated circuits SAA1059 (h.f. prescaler), SAA1056 (PLL frequency synthesiser) and an op-amp integrator (PLL loop filter and amplifier) were used in our radio tuning system (RTS). We have now used bipolar technology to combine analogue circuits with several types of logic (I^2L, ECL and miniwatt) so that all the functions previously performed by three integrated circuits can be performed by a single 18-pin LSI integrated circuit called synthesiser module SAA1057. The component economy afforded by the SAA1057 is amply illustrated by Fig.1 which shows that tuning synthesiser functions which previously required the use of three integrated circuits and a large number of peripheral components can now be performed by the SAA1057 and only 16 peripheral components.

The SAA1057 is not only economical with regard to the required number of components. It also consumes very little current (<20 mA) and is able to meet the varied performance requirements of all classes of radio from battery-powerd portables to mains-powered hi-fi tuners. For example, a novel twin phase detector system in the PLL achieves the fast tuning often required for car radios and also ensures that, when the PLL is locked, the VCO signal has high spectral purity to ensure low distortion in hi-fi tuners. The wide frequency range (a.m. 512 kHz to 32 MHz, f.m. 70 MHz to 120 MHz) and high maximum tuning voltage (30 V) make the SAA1057 suitable for multi-waveband mains sets. The low current consumption combined with the wide supply voltage range (3.6 V to 12 V) due to internal stabilisation allow it to be used in battery-powered portables.

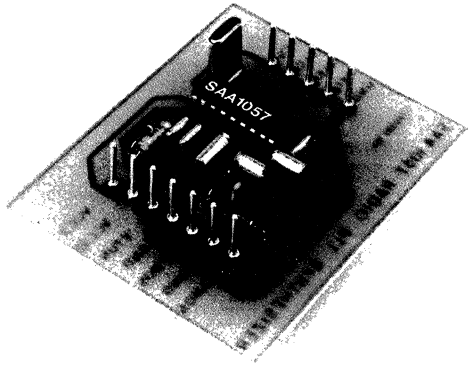
In addition to the basic function of tuning by direct entry of frequency, the SAA1057 can also provide the following software-controlled facilities:

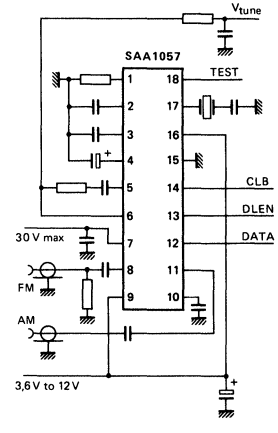
- search tuning with muted interstation noise
- continuous up/down step tuning (manual tuning)
- accurate storage and automatic tuning to preset frequencies





(a)





(b)

Fig.1 Basic radio tuning synthesisers. Circuit (a) uses three integrated circuits and 36 peripheral components. Circuit (b) performs the same functions using synthesiser module SAA1057 and 16 peripheral components

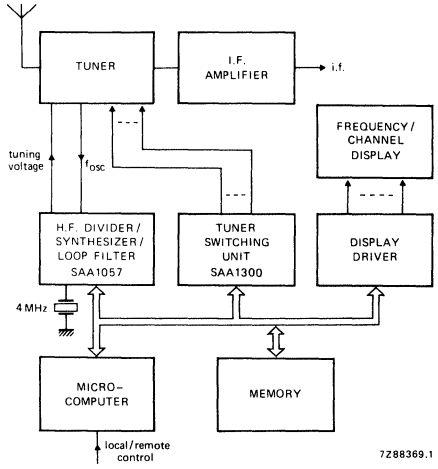


Fig. 2 Integrated circuits for tuning systems using SAA1057.

BIPOLAR CIRCUITS

Remote control

TDB2033 gain-controlled remote IR receiver amplifier

Frequency synthesiser

SAA1057 radio tuning PLL frequency synthesiser

Display drivers

SAA1060 32 segment LED
SAA1062/T 20 static outputs for LCD
SAA1063 32 segment FTD

Tuner switching

SAA1300 5-line switching circuit

MOS CIRCUITS

Display drivers

PCE2100 40 segment LCD
PCE2110 60 segment LCD + 2 LEDs } in duplex mode
PCE2111 64 segment LCD
PCE2112 32 segment LCD static
SAA1061 16 static outputs for LED drive and switching functions
SAB3044 2 digit LED

Single-chip 8-bit microcomputers

MAB8021 with 1K byte ROM and 28-pin package
MAB8048 with 1K byte ROM and 40-pin package
MAB84XX NMOS family with 1 to 4 Kbyte ROM and I^2C bus
MAB85XX CMOS family with 0.5 to 4K byte ROM and I^2C bus

Memories

PCD8571 128 x 8-bit CMOS memory with serial I/O
PCB1400 100 x 16-bit EEPROM with serial I/O

Infrared remote-control receivers

SAB3023 receiver and analogue memory
SAB3033 receiver and analogue memory
SAB3042 receiver and decoder with C-bus
SAB3028 receiver and decoder with I^2C bus

Infrared remote-control transmitters

SAB3004 7 x 64 commands
SAB3021 2 x 64 commands
SAB3027 32 x 64 commands

- loading of frequency data in synchronism with the sampling frequency to prevent disturbance of the tuning lock
- feed out of a number of internal signals for alignment purposes
- adjustment of PLL current gain over 40 dB range (0.023 to 2.3) to eliminate switching of external loop filter components during waveband selection.

As the word 'module' in the name of the SAA1057 indicates, this new IC is part of a modular, data-bus compatible, digitally-controlled tuning system in accordance with the systems design philosophy followed for other circuits in our range of ICs for digital systems in radios. The modular approach minimises radiation and reduces wiring and screening costs because:

- all the sensitive signal processing circuits for the tuning systems are now in the SAA1057 which can be mounted in the ideal position close to the tuner
- internal h.f. dividers eliminate the need for an external prescaler
- two sensitive, internally switched VCO inputs to the SAA1057 allow direct connection of the f.m. and a.m. local-oscillator signals without additional impedance matching, amplification or switching
- the crystal-controlled reference oscillator for the PLL operates at the same frequency for the a.m. and f.m. waveband and causes little radiation because it generates a low-level sinewave
- the separate microcomputer and memory can be mounted close to the keyboard and their capacity can be tailored to meet the demands of specific radios
- the frequency display driver can be mounted close to its display.

As shown in Fig.2, the data-bus compatibility of tuning systems using the SAA1057 also allows the simple addition of circuits as required for waveband-switching and for driving LED, LCD or fluorescent displays of preset station number, waveband and channel number. Other facilities which can be simply and economically accommodated are analogue signal control, extra display functions, and remote control via an infrared data link.

OPERATING PRINCIPLES OF FREQUENCY SYNTHESIS

A basic digitally-controlled PLL for radio tuning is shown in Fig.3. The output from the voltage-controlled local-oscillator in the radio is converted into a pulse train, and frequency divided by a programmable divider, before being applied to one of the inputs of the phase detector. The output from the crystal-controlled reference oscillator is converted into a pulse train, and frequency divided by one of two ratios, before being applied to the other input of the phase detector. The phase detector output, which is proportional to the relative phase (and therefore the frequency) of the two input signals, is passed through the low-pass loop filter to remove the high-frequency components and fed back to the VCO as the tuning control voltage. The loop is locked, and the radio correctly tuned, when $f_{osc}=Nf_{ref}$ where N is the programmable division ratio determined by selecting the frequency of the required broadcast.

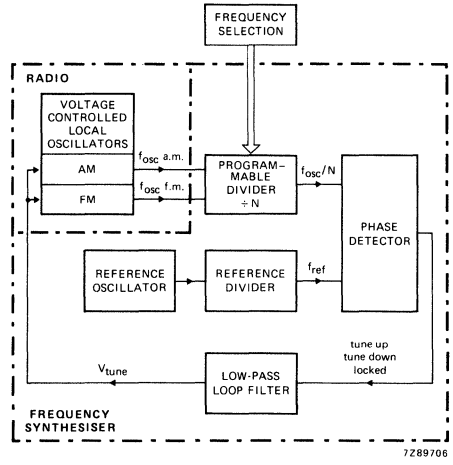


Fig.3 A basic digitally-controlled PLL for radio tuning

BRIEF DESCRIPTION OF THE FUNCTIONS OF THE SAA1057 (Fig.4)

Local-oscillator inputs

The local-oscillator signals from the radio are applied to inputs FFM for f.m. and FAM for a.m. Since these inputs have a sensitivity of 30 mV to 500 mV (a.m.) and 10 mV to 500 mV (f.m.), the local-oscillator signals can be directly applied without preamplification or buffering. A separate pin (DCA) allows the bias circuitry of the internal input amplifiers to be decoupled by an external capacitor. The input frequency range is 512 kHz to 32 MHz for a.m. and 70 MHz to 120 MHz for f.m., the f.m. signals being passed through an internal divide-by-ten h.f. prescaler which is switched off by software to minimise current consumption whilst tuning the a.m. band. Since the a.m. and f.m. local-oscillator signals are automatically selected by software, they need not be externally switched during waveband selection.

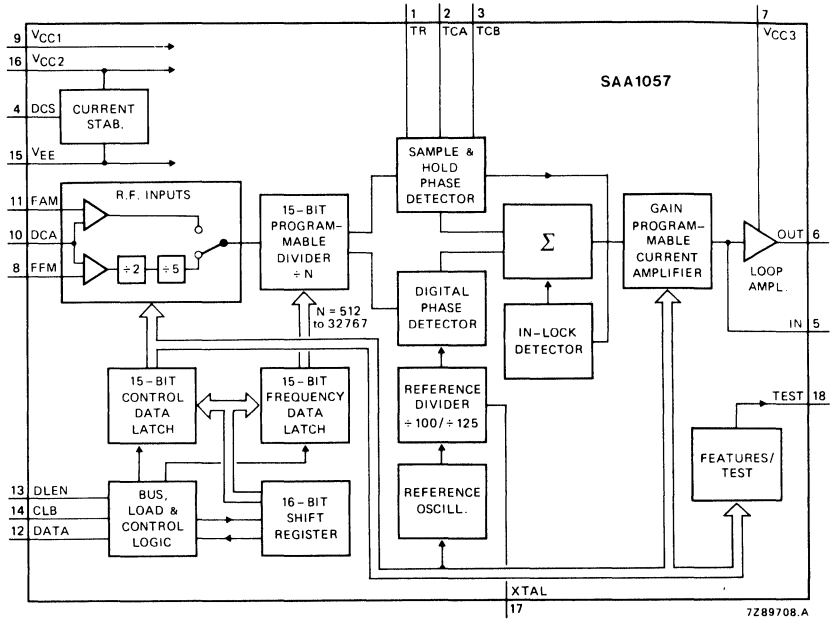


Fig.4 Block diagram of the SAA1057

Programmable divider

This 15-bit frequency divider, which is designed in a special manner to minimise current consumption, is programmed with a binary-coded divisor (N) to synthesise the required frequency for the voltage-controlled local-oscillator in the radio. The local-oscillator frequency (f_{osc}) is usually the i.f. above the tuned frequency. The dividing number is $(32f_{osc})/f_{ref}$ for a.m. and $(3.2f_{osc})/f_{ref}$ for f.m., where f_{ref} is the output frequency from the reference frequency divider (40 kHz or 32 kHz). The minimum divisor is 512 and the maximum divisor is 32 767. The frequency-divided local-oscillator signal is applied as one of the inputs to a dual phase detector system.

Reference frequency oscillator

This stable, temperature-compensated oscillator is controlled by an inexpensive 4 MHz crystal (series resistance <150Ω) connected in series with a capacitor between pin 17 of the SAA1057 and the common return line. The reference frequency may alternatively be derived from a stable external source. In this case, a 4 MHz squarewave of 5 V peak to peak may be connected to pin 17 via a series-connected 10 nF capacitor and 22 kΩ resistors.

Reference frequency divider

This circuit divides the frequency of the signal from the reference oscillator by 125 or 100 to obtain a reference frequency of 32 kHz or 40 kHz for the dual phase detector system under the control of software. If the selected reference frequency is 32 kHz, the minimum tuning step is 1 kHz on a.m. and, due to the divide-by-ten h.f. divider, 10 kHz on f.m. If the selected reference frequency is 40 kHz, the minimum tuning steps for a.m. and f.m. are 1.25 kHz and 12.5 kHz respectively. If larger tuning steps are required, integer multiples of these tuning steps can be selected by software.

Phase detector system

To simplify the design of the PLL loop filter, the SAA1057 incorporates a novel dual phase detector system that uses the same reference frequency for a.m. and f.m. One of the phase detectors is a high speed digital memory (flip-flop) type, the other is a high gain analogue memory (sample and hold) type. The digital phase detector operates at the reference frequency, generates about 100 times as much tuning current as the analogue phase detector and provides high speed tuning over a wide frequency range. The analogue

phase detector operates at 1/32 of the reference frequency, has no region of uncertainty in its transfer characteristic and provides increased spectral purity of the local-oscillator signal when the PLL is locked. The 'hold' voltage from the analogue phase detector is converted into a d.c. current and summed with the output pulses from the digital phase detector to provide a current proportional to tuning error. This current drives a gain-programmable amplifier to generate the tuning voltage output.

The analogue phase detector is always operating, but the digital phase detector can be switched on/off by setting/resetting the in-lock detector with features/test bits in the software (e.g. to minimise noise during step tuning). If the software does not include any features/test bits, the digital phase detector is automatically switched on if the tuning error exceeds the phase range of the analogue phase detector. This could occur, for example, as the result of executing a large frequency change. When the in-lock detector determines that the tuning error has been reduced to within the operating range of the analogue phase detector for three consecutive sampling periods, the digital phase detector is automatically switched off again.

Gain-programmable current amplifier

The sum of the output currents from the two phase detectors drives a gain-programmable bidirectional current source which replaces the normally-used resistor between the charge pump and loop amplifier of a PLL. This allows the loop gain of the PLL to be software programmed over a 40 dB range within the limits 0.023 to 2.3, thereby eliminating the need to switch loop filter components during waveband selection.

Loop amplifier

The loop amplifier is capable of providing a tuning voltage output of up to 30 V and only requires a series-connected RC network between its input and output to form an active low-pass loop filter. The supply voltage for the loop amplifier (V_{CC3}) need not be stabilised but it should be adequately filtered.

Reception of frequency and control data

Data for the SAA1057 consists of serially-transmitted 17-bit frequency setting and control words from a microcomputer. Both types of word incorporate a zero start bit which is tested to identify a correct transmission. Each word also contains a latch selection bit which is 0 for a frequency setting word and 1 for a control word. The incoming data is transmitted via an asynchronous data highway with separate data (DATA), clock (CLB) and enable (DLEN) lines. The logic levels on the lines are TTL compatible and are independent of supply voltage.

Sixteen bits of each incoming data word are loaded into a shift register. The bus, load and control logic then checks that the transmission is valid by checking that the first bit is zero and that the word length is correct during the HIGH period of the DLEN line. If valid, the data word is then transferred to the appropriate latch by the next pulse on the clock line.

A frequency-setting word includes fifteen bits which define the required frequency expressed as a 15-bit binary-coded divisor (512 to 32 767) for the programmable divider.

A control word includes fifteen bits for the following purposes:

- one bit (FM) to control the switch to select the required input from the a.m. or f.m. local-oscillator. If the a.m. input is selected, the divide-by-ten prescaler is switched off to conserve power
- one bit (REFH) to program the divisor for the reference frequency divider
- four bits (CP0 to CP3) to set the gain of the gain-programmable current amplifier
- one bit (SB2) to determine whether the remaining eight features/test bits should be used or not
- one feature bit (SLA) which determines whether frequency setting data is loaded into the programmable divider immediately after reception (asynchronous loading) or synchronised with the sampling frequency (synchronous loading). Synchronous loading is for minimising noise during manual tuning without muting
- two features bits (PDM0 and PDM1) which set the operating mode of the digital phase detector as previously described
- one feature bit (BRM) which sets the bus receiver into an automatic mode so that it is switched off to conserve power after a data transmission
- four test bits (T0 to T3) which can route the reference signal, the output from the programmable divider or the output level from the in-lock detector to the TEST pin for alignment purposes.

TECHNIQUES USED TO OBTAIN THE HIGH PERFORMANCE OF THE SAA1057

Many new circuit techniques have been used in the SAA1057 to achieve the high performance, application flexibility and low power consumption. A description of the techniques listed here is beyond the scope of this article but further information can be found in the references:

- travelling-wave dividers in the divide-by-ten prescaler ensure low current consumption and high sensitivity for the r.f. inputs

- a tail-end divider is used to increase the speed of the digital phase detector
- a rate-select technique in the programmable divider minimises phase jump in the digital phase detector
- current consumption is minimised by using stacked logic for the three different types of digital circuits (I^2L, ECL and miniwatt). In this way, many of the logic circuits act as current sources for other logic circuits
- use of a bandgap current reference ensures that the current consumption remains constant over a wide range of supply voltage and operating temperature
- the op-amps at the r.f. inputs have an input bias current of less than 10 nA and also have a very high slew rate
- the tuning voltage is derived from a 30 V op-amp with a low bias current and a high slew rate.

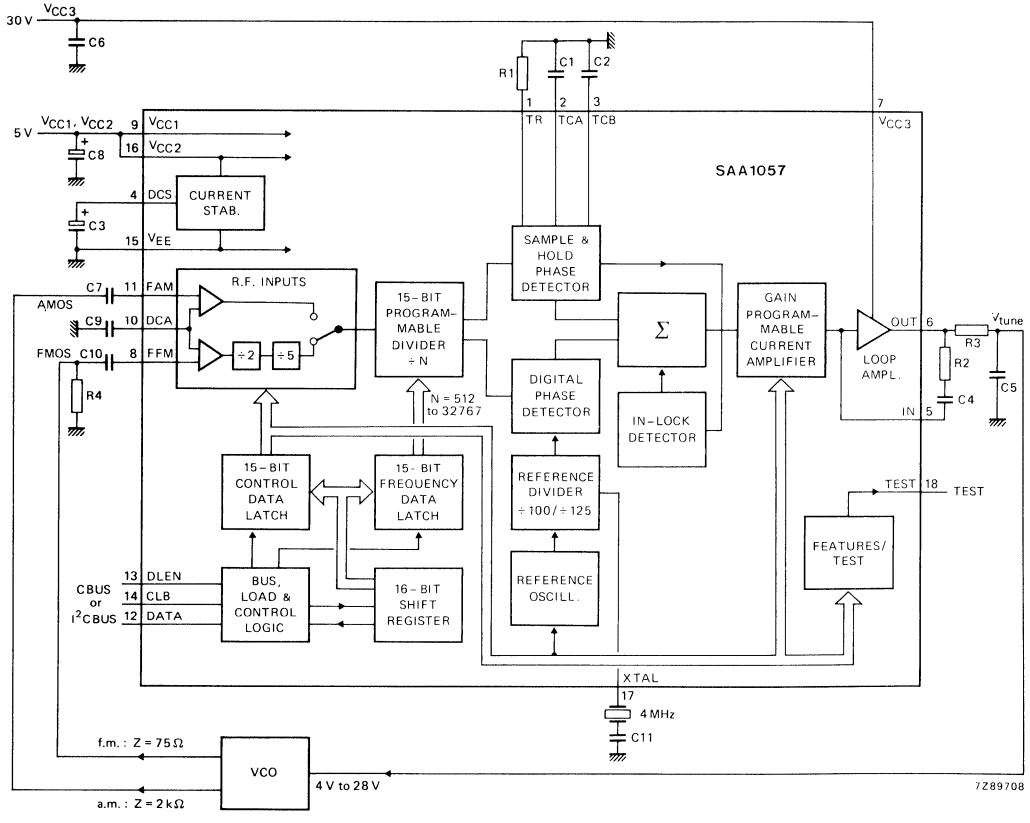


Fig.5 An a.m./f.m. frequency synthesiser using the SAA1057

BASIC APPLICATION OF THE SAA1057

Figure 5 is the circuit diagram of a complete frequency synthesiser using the SAA1057. The functions and values for each component in the diagram are as follows:

ref.	function	value
R_1	defines the current in the analogue phase detector	180 Ω
R_2	loop filter resistor (value depends on VCO)	18 kΩ
R_3	low-pass filter resistor (value depends on VCO)	100 Ω min.
		10 kΩ typ.
R_4	matching resistor for 75 Ω f.m. input	180 Ω
C_1	sample capacitor (low leakage type)	2.2 nF typ.
C_2	hold capacitor (low leakage type)	10 nF typ.
C_3	decoupling of internal reference voltage	47 μF
C_4	loop filter capacitor (value depends on VCO)	330 nF typ.
C_5	low-pass filter capacitor, normally located in the tuner (value depends on loop frequency)	100 nF typ.
C_6	power supply filtering	100 nF
C_7	d.c. blocking	1 nF
C_8	power supply filtering	100 μF
C_9	decoupling of r.f. input stages	10 nF
C_{10}	d.c. blocking	11 nF
C11	series capacitor for crystal (value depends on crystal)	33 pF

PERFORMANCE OF THE CIRCUIT FOR F.M.

tuning range	87.5 (88) to 108 MHz
tuning steps	10 kHz or 12.5 kHz
intermediate frequency	10.7 MHz (variable in steps of 10 kHz or 12.5 kHz)
tuning voltage of the VCO	4 to 28 V
VCO gain	0.3 to 3 MHz/V
ref. frequency	32 kHz
prog. divider ratios	9820 (9870) to 11870
time to tune across band	<400 ms
gain of current amplifier	0.3
loop filter time constant	1 ms
r.m.s. ripple on tuning voltage	
noise (20 Hz to 20 kHz)	5 μV
1 kHz	<1 μV (0.3 μV)

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ACKNOWLEDGEMENT

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Analysis and Basic Application of the SAA1057 AN197

Author: J. Matull

INTRODUCTION

Early digital tuning systems for AM/FM radio receivers were constructed from ICs out of standard logic families (ECL, TTL etc.).

Later, first dedicated ICs for PLL frequency synthesizers have appeared on the market, but there were still several packages required for the complete tuning system. The partitioning of functions depends on the semiconductor technologies used. The tuning part of a digital tuning system typically requires three packages: a prescaler in ECL or Schottky TTL (speed), a programmable divider and other digital functions in either LOCMOS, NMOS or I^2L (packing density, current consumption) and a loop amplifier with FET inputs (low bias current) and a bipolar output stage (current, slew rate).

Now, more sophisticated ICs for digital tuning of radio receivers are showing. The SAA 1057, being described in this report, belongs to this new generation of radio PLL frequency synthesizers. It comprises all of the functions of a digital PLL frequency synthesizer and all active components from the inputs for the local oscillators to the output for the varactor tuning voltage on one monolithic chip, requiring only a minimum of external passive components.

SYSTEM DESCRIPTION

A functional block diagram of the SAA 1057 is shown in Figure 1. This system is designed to handle both AM and FM local oscillator frequencies in a microcomputer-controlled radio receiver. Attention has been paid to the power consumption of the IC in order to permit its use in portable as well as in mains operated radios.

An important property of the SAA 1057 is its very low radiation. This is due to the compact one-chip design which does not require an external prescaler and its control line and due to the crystal controlled reference oscillator which operates with a low sine-wave voltage swing.

R.F. Inputs

Separate inputs are provided for the AM and FM local oscillators. Amplifiers at the inputs offer high sensitivity for easy interfacing to the radio's VCOs. No external buffers are required. A built-in divide-by-10 prescaler for FM permits a maximum input frequency of 120MHz while the AM input can directly handle up to 32MHz.

An input multiplexer permits both oscillators to be operating at the same time, thus saving cost for switching the oscillators in the radio. On AM, the prescaler is switched off in order to reduce the current drain of the chip.

There is one pin, DCA, for the decoupling of the input amplifiers' bias circuitry.

Programmable Divider

This 15 bit divider is programmed with a binary coded dividing number, N, in order to synthesize a desired frequency f_{VCO}. In view of the current consumption, this divider was designed according to the rate select technique. This implies a minimum permissible dividing number, N_{min}, which is equal to 512 in the SAA 1057. The maximum dividing number, N_{max}, is given by the 15 bit length as 32767.

Two outputs of the programmable divider are fed to the phase detectors. They differ in frequency by a factor of 32.

Reference Oscillator

This oscillator is designed to operate with a low-cost 4MHz crystal. Only one pin is required for this stable, temperature-compensated oscillator.

In case of an externally available 4MHz signal of sufficient stability, the pin XTAL can be supplied with a resistor from that source.

Reference Divider

This divider generates the reference frequency for the digital phase detector from the 4MHz crystal frequency. This reference frequency is either 32kHz or 40kHz. It can be changed under software control and outputted at the pin TEST in case that is desired, e.g. for aligning the frequency of the reference oscillator.

With these two reference frequencies, the minimum step size for changing the VCO's frequency is 1kHz and 1.25kHz on AM. On FM, the step size is 10kHz and 12.5kHz due to the divide-by-10 prescaler. Larger steps in VCO frequency (integer multiples of the values given above) can be achieved under software control.

Phase Detectors

A novel phase detector concept is used in the SAA1057, permitting the use of the same reference frequency on AM and FM, thereby facilitating the design of the loop filter.

Two phase and frequency sensitive detectors are used in this concept, a high-speed digital flip-flop type detector and a high-gain analog sample and hold type detector. The digital phase detector (PD) operates at the reference frequency and provides for high tuning speed. The analog PD operates at 1/32 of the reference frequency and provides for improved spectral purity of the radio's VCO after lock has been achieved. There is no region of uncertainty in the analog PD's transfer characteristic.

The analog PD is always operating. The digital PD can be switched on/off either under software control (see also 2.9) or automatically. If no features/test bits are selected, the digital PD is automatically switched on if the operating range of the analog PD is exceeded, e.g. when a jump in frequency is executed. It is automatically switched off again if the operating range of the analog PD has not been exceeded during three consecutive sampling periods. That is accomplished by the in-lock detector. This detector can be set and reset under software control to establish the different modes of PD operation.

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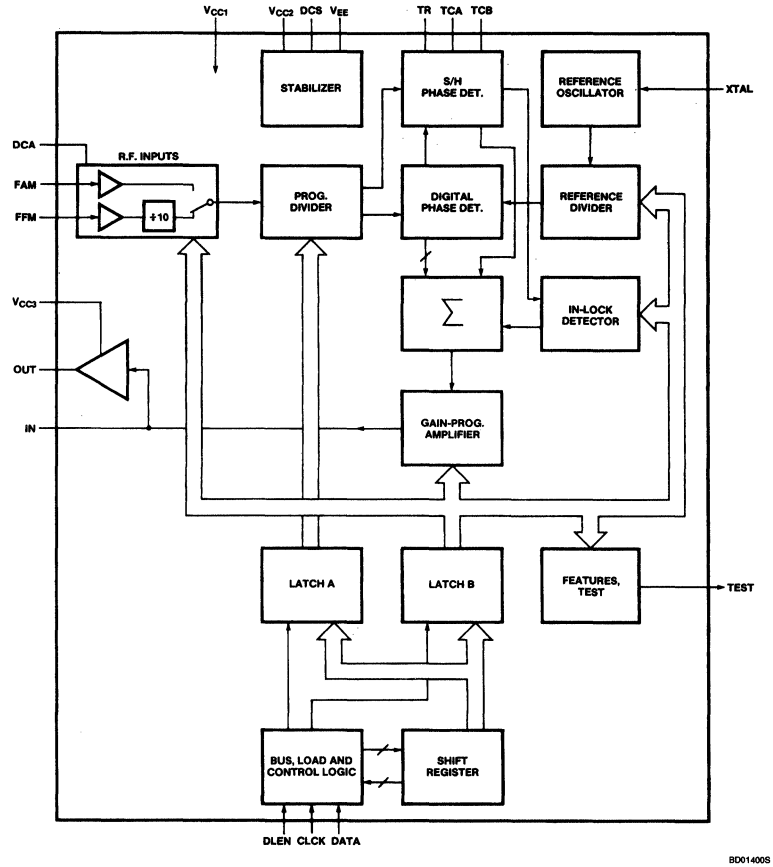

Figure 1. Functional Block Diagram

The "hold" voltage of the analog PD is converted to a DC current and summed with the output pulses of the digital PD.

Gain-Programmable Current Amplifier

The output current of the phase detector configuration is passed through a gain-programmable amplifier. This is an equivalent for the normally used series resistor from the charge pump to the loop amplifier. The advantage of this solution is that the loop gain can be programmed under software control without any changes in hardware.

Loop Amplifier

The on-chip loop amplifier requires only a CR series connection between its input and output pins to build a basic loop filter. Tuning voltages of up to 30 volts can be generated. The supply voltage for this amplifier, V_{CC3}, need not be stabilized; however, it should be sufficiently filtered.

Data Reception

The SAA1057 requires both frequency and control information from an external microcomputer. This information is received via an asynchronous serial data link with separate data (DATA), shift clock (CLCK) and enable (DLEN) lines. This structure with the associated timing requirements used to be called CBUS. The logic levels on these CBUS lines are TTL compatible, independent of the supply voltage.

Incoming data is received in a shift register. A bus, load and control logic performs a format check on received data and a decision on whether the transmission was valid or not. Only correctly received data are transferred to one of the two latches. Frequency information is stored in latch A and control information in latch B.

Features / Test

In addition to the basic PLL operation of the SAA1057 there are a few features and test functions which can be enabled by certain bits in the control information.

Examples are synchronous loading of frequency data to prevent an out-of-lock condition due to that transmission, disabling of the digital phase detector to avoid tuning noise in case of step tuning, and outputting of the reference frequency, e.g. for the alignment of the crystal oscillator frequency. Details are described in the application section of this report.

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Table 1. Description of Components

R1	Defines current in S/H detector	e.g. R1 = 390	Ω
R2	Loop filter resistor, depends on VCO	e.g. R2 = 18	kΩ
R3	Low-pass filter resistor	min. R3 = 100	Ω
R4	Matching resistor for FM input	e.g. R4 = 180	Ω
C1	Sample capacitor, low leakage type	typ. C1 = 2.2	nF
C2	Hold capacitor, low leakage type	typ. C2 = 10	nF
C3	Decoupling of internal reference voltage	typ. C3 = 10	nF
C4	Loop filter capacitor, depends on VCO	e.g. C4 = 330	nF
C5	LOW-pass filter capacitor, mostly located in tuner, depends on loop frequency	e.g. C5 = 100	nF
C6	Power supply filter capacitor	e.g. C6 = 100	nF
C7	DC blocking capacitor	typ. C7 = 1	nF
C8	Power supply filter capacitor	e.g. C8 = 100	nF
C9	Decoupling of RF input stages	typ. C9 = 10	nF
C10	DC blocking capacitor	typ. C10 = 22	nF
C11	Series capacitor for crystal	e.g. C11 = 33	pF
Y1	Crystal for reference oscillator, f = 4.000MHz		

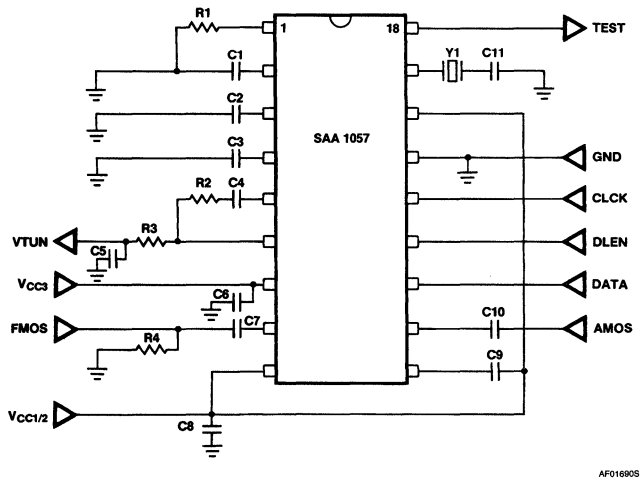

Figure 2. Basic Application

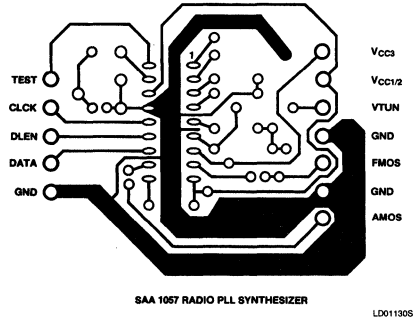

Figure 3. Bottom View of P.C. Board

Power Supply

Besides the already mentioned supply voltage for the loop amplifier there are two pins for the supply of the whole circuit: V_{CC1} and V_{CC2}. The supply voltage may be chosen in the range from 3.6 to 12 volts without significant influence on the supply current due to the internal stabilizer, which is decoupled at pin DCS. The supply voltage should be well filtered.

APPLICATION

The circuit diagram for the basic application of the SAA1057 in an AM/FM radio receiver is shown in Figure 2; a short description of the components is given in Table 1.

As there are many ways in which radio receivers can be different from each other,

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e.g. number of wave bands, supply voltages, tuning voltage range, V/F characteristic of the VCO, the synthesizer circuitry has to be designed for a specific application.

In this chapter information is given on all of the components in the circuit diagram and on the software requirements of the SAA1057 for a number of receiver tuning procedures.

A typical lay-out of a printed circuit board for the application of the SAA1057 is given in Figure 3. There are two connectors; one for the supply voltages and the connection of the radio receiver and one for the CBUS from the microcomputer or a synthesizer controller, like the SYCO II.

Interfacing of the Tuner's Oscillators

The oscillator frequency lines are either realized on a p.c. board or as a screened cable, depending on their length, among others. The output at the AM VCO is not critical; it can be an inductive or capacitive tap at the resonant circuit, provided the output voltage is at least 30 millivolts rms into a load of 2 kΩ. The minimum required FM oscillator voltage is 10 millivolts rms, the input resistance of the SAA 1057 is 135 ohms. In order to minimize the voltage standing wave ratio, VSWR, a resistor, R4, is used to match the input resistance, R_{iFM}, to that of the connecting cable, Z_o. Ignoring the capacitances, R4 can be calculated according to

$$R4 = \frac{R_{iFM} \cdot Z_o}{R_{iFM} - Z_o} \quad (1)$$

Let $Z_o = 75$ ohms, then

$$R4 = \frac{135 \cdot 75}{135 - 75} = 169\Omega$$

The closest standard resistor is R4 = 180 ohms.

The DC blocking capacitors, C7 and C10, should be chosen so that their series reactance at the lowest VCO frequency is small compared to the input impedance. Thus,

$$C7 > > \frac{1}{2 \cdot \pi \cdot f_{FM,min} \cdot R_{iFM}} \quad (2)$$

and

$$C10 > > \frac{1}{2 \cdot \pi \cdot f_{AM,min} \cdot R_{iAM}} \quad (3)$$

Interfacing of the Tuning Voltage

The output of the loop amplifier is connected to the varicap tuning diodes via a CR low-pass filter, R3 and C5.

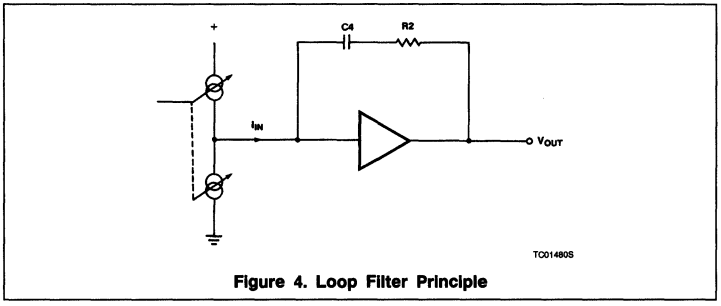

Figure 4. Loop Filter Principle

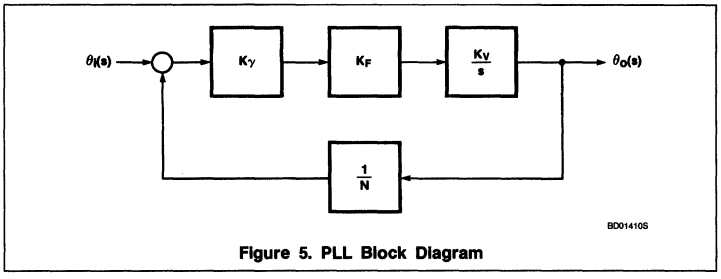

Figure 5. PLL Block Diagram

Although there is no lower limit of R3, a minimum of about 100Ω should be used to avoid capacitive loading of the loop amplifier output. For C5, there is normally a lower limit given by the design of the varactor tuned resonant circuits in the radio.

The cut-off frequency of the low-pass filter, f_{1p}, should be less than the sampling frequency, f_s, of the phase detector in order to attenuate potential ripple at this frequency. On the other hand, the cut-off frequency should be high compared to the loop's natural frequency, f_n, to keep the decrease of the phase margin as small as possible. f_n depends on the F/V characteristic of the VCO, the dividing number, N, and the loop filter design.

Thus, the choice of the low-pass filter's cut-off frequency is a compromise between ripple rejection at the sampling frequency and loss of phase margin.

$$f_n < f_{1p} < f_s \quad (4)$$

or

$$\frac{1}{\omega_n} > R3 \cdot C5 > \frac{1}{2\pi \cdot f_s} \quad (5)$$

with $\omega_n = 2 \cdot \pi \cdot f_n$

f_s = 1kHz or 1.25kHz

Designing the Loop Filter

Due to the on-chip loop amplifier and gain-programmable current amplifier, the loop filter consists of only two external components, R2 and C4. The loop filter principle is shown in Figure 4.

As outlined earlier, the commonly used series resistor between charge pump and loop amplifier input is replaced by a gain-programmable current amplifier in the SAA1057. Therefore, the loop filter transfer function evaluates to

$$K_F = \frac{V_{OUT}\ (s)}{i_{IN}\ (s)} = \frac{1 + sT}{sC4} \quad (6)$$

with T = R2 • C4.

The basic block diagram of a PLL in terms of gain is shown in Figure 5.

The output to input ratio reflects a second order system:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_\varphi \cdot K_F \cdot K_V}{s + \frac{K_\varphi \cdot K_F \cdot K_V}{N}} \quad (7)$$

with K_φ = gain of digital phase detector including current amplifier
K_F = gain of loop filter as given in Equation (6)
K_V = gain of VCO
N = integer divisor

Substituting K_F yields (8)

Table 2. Loop Filter Input Current vs. Gain Programming

CP3	CP2	CP1	CP0	I_{dig}
0	0	0	0	0.01mA
0	0	0	1	0.03mA
0	0	1	0	0.1mA
0	1	1	0	0.3mA
1	1	1	0	1.0mA

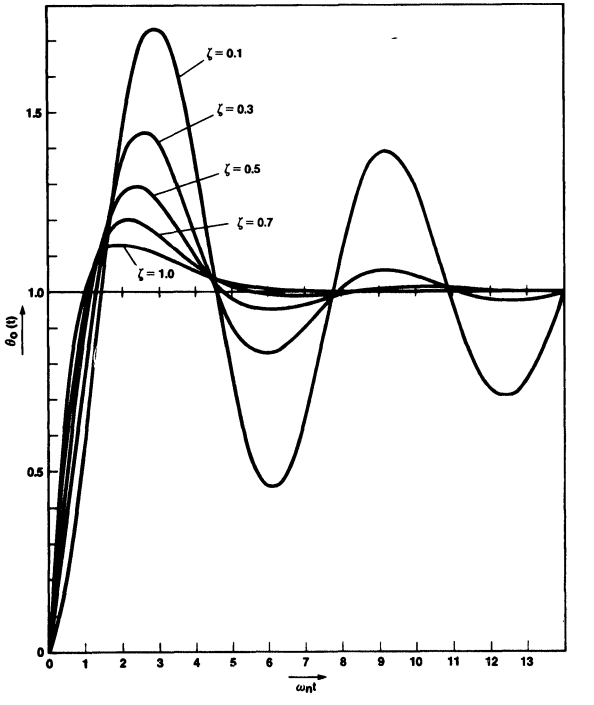

Figure 6. Type 2. Second Order Step Response

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{K_\varphi \cdot K_V}{C} \cdot (1 + sT)}{s^2 + s \cdot \frac{K_\varphi \cdot K_V \cdot R2}{N} + \frac{K_\varphi \cdot K_V}{C4 \cdot N}}$$

clearly showing the Characteristic Equation of a second order polynomial:

$$C.E. = s^2 + s \cdot 2\zeta \cdot \omega_n + \omega_n^2 \quad (9)$$

By comparison of coefficients one obtains

$$\omega_n = \sqrt{\frac{K\varphi \cdot K_V}{C4 \cdot N}} \quad (10)$$

$$\zeta = \omega_n \cdot \frac{R2 \cdot C4}{2} \quad (11)$$

with ω_n = loop bandwidth or natural frequency

ζ = damping factor

The gain of the phase detector, $K\mu$, is the output current of the P.D. times the gain of the programmable current amplifier. In order to simplify the calculation, we re-write Equation (10) as follows:

$$\omega_n = \sqrt{\frac{I_{dig} \cdot S_{vco}}{C4 \cdot N}} \quad (12)$$

with I_{dig} = current programmed according to Table 2

and

$$S_{vco} = \frac{df_{vco}}{dV_{tune}} \quad (13)$$

being the slope of the VCO's F/V characteristic.

Since neither S_{VCO} nor N remain constant over a larger frequency band, ω_n and ζ should be calculated for several points in the wave band considered, in order to find the appropriate constants for best loop performance. See the Appendix for a design example.

The lock-up time not only depends on the loop filter components but also on the current gain setting. The longest time which can occur is that for a jump from one end of a wave band to the other. It consists of two parts:

$$t_{band} \approx t_{slew} + t_{settle} \quad (14)$$

The output pulses of the digital phase detector can be assumed to have an average duty cycle of 50 o/o during most of the slew time. Therefore, t_{slew} can be approximated as

$$t_{slew} \approx 2 \cdot \frac{C4 \cdot \Delta V_{tune}}{I_{dig}} \quad (15)$$

The settling time, t_{settle}, depends on ω_n and can be estimated from

$$t_{settle} \approx \frac{\omega_n t}{\omega_n} \quad (16)$$

with $\omega_n t$ taken from Figure 6 for a certain overshoot and ω_n as given by Equation (12).

The output phase response of a type 2 second order system (Figure 5) to a phase step input is shown in Figure 6. The curves can also be used for frequency inputs and outputs. The required damping factor, ζ, for a given overshoot can be taken from the plot. Also, the natural frequency, ω_n, can be calculated if ζ and the lock-up time, t_{settle}, are known.

The Analog Phase Detector

In the analog PD a comparison of the relative phase of two digital signals is performed. In principle, a voltage ramp is started by the crystal controlled reference frequency and stopped by the high-speed output of the programmable divider. As only every 32nd output pulse is sampled, the phase jitter of that rate-multiplier type divider is eliminated. The ramp voltage is transferred to the hold capacitor, C2. Any deviation from the ramp's center voltage is converted to a current, amplified in the gain-programmable current amplifier, and fed into the loop amplifier.

The voltage ramp is generated by first charging the capacitor, C1, with internal circuitry and then discharging it with a constant current, which is defined by an external resistor,

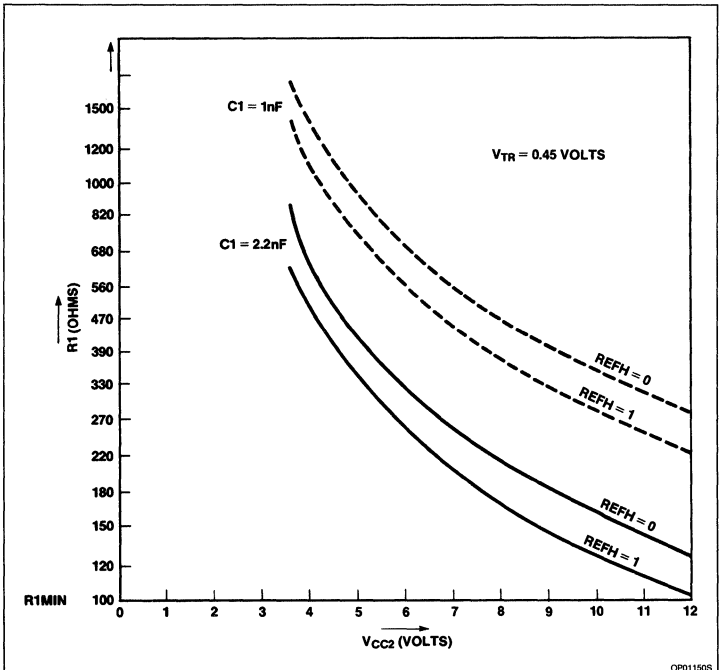

Figure 7. Maximum R1 As A Function Of V_{CC2}

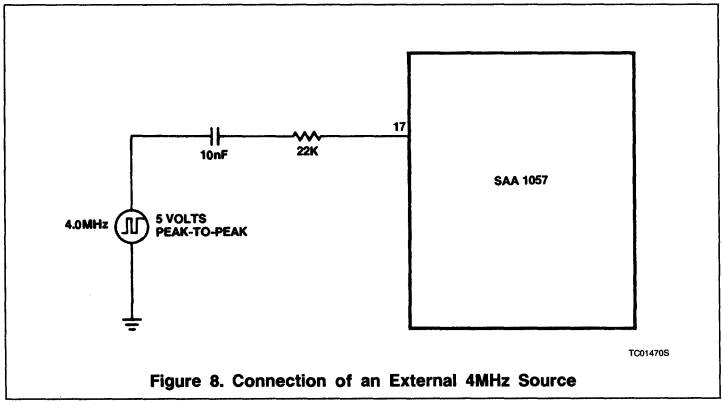

Figure 8. Connection of an External 4MHz Source

Table 3. Loop Filter Input Current Per Volt Change of the Hold Capacitor Voltage

CP3	CP2	CP1	CP0	I_{analog} PER VOLT
0	0	0	0	0.03=mμA
0	0	0	1	0.1=mμA
0	0	1	0	0.3=mμA
0	1	1	0	1.0=mμA
1	1	1	0	3.5=mμA

R1. Thus, the slope of the ramp, i.e. the gain of the analog PD, can be changed by changing the component values of C1 and R1. There are two limitations. For R1, there exists a minimum value of 100 ohms in order to limit the discharge current to a safe value and for C2, there is a maximum value given for both reference frequencies to permit complete pre-charging of that capacitor.

The maximum ramp amplitude depends on the supply voltage, V_{CC2}, and is typically

$$V_{ramp} = V_{CC2} - 2 \text{ volts} \quad (17)$$

The time required for a discharge of C1 from $V_{TCA,max}$ to $V_{TCA,min}$ depends on the value of C1 and the discharge current, which is defined by R1. The maximum time is

$$t_{ramp} = \frac{C1 \cdot V_{ramp}}{I_{dis}} \quad (18)$$

With

$$I_{dis} = \frac{V_{TR}}{R1} \quad (19)$$

and the maximum permitted time, t_{dis}, we can calculate the maximum value of resistor R1 to be

$$R1_{max} = \frac{t_{dis} \cdot V_{TR}}{C1 \cdot (V_{CC2} - 2)} \quad (20)$$

V_{TR} is the voltage at pin 1 of the SAA1057 during the discharging of capacitor, C1. The dependency of the upper limit of R1 on V_{CC2} is shown in Figure 7 for two different values of C1.

The center voltage is typically

$$V_{r,o} = \frac{V_{CC2}}{2} + 0.3 \text{ volts} \quad (21)$$

giving an operating range of the analog PD of

$$V_{SH} = V_{r,o} \pm \frac{V_{ramp}}{2} \quad (22)$$

As the maximum output current of the analog PD depends on V_{CC2}, only a "gain" constant of 1.5=mμA/V is specified, i.e. a deviation of 1 volt from the center voltage, $V_{r,o}$, produces an output current of 1.5=mμA. This current is amplified in the gain-programmable amplifier and then fed into the loop amplifier. In Table 3 there are given some loop filter input current values for different gain settings of the gain-programmable amplifier.

To obtain the maximum currents obtainable from the analog PD, the values in Table 3 have to be multiplied by $1/2 \cdot V_{ramp}$.

Generating the Reference Frequency

The simplest way of completing the reference frequency oscillator is to connect a 4MHz quartz crystal from pin 17 (XTAL) to ground.

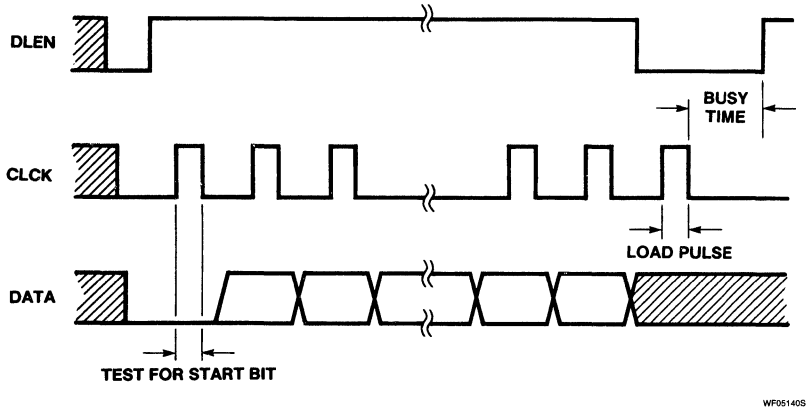

Figure 9. CBUS Timing

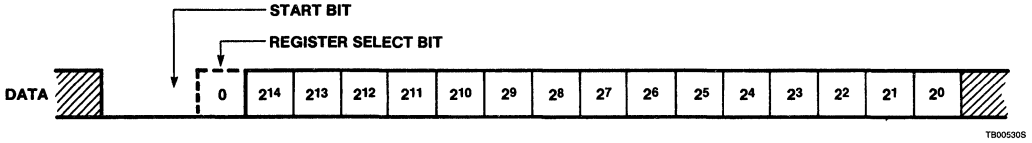

Figure 10. Data Word for Frequency

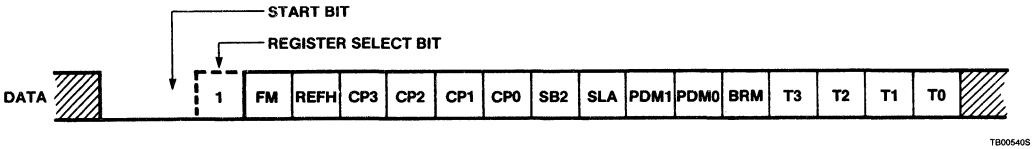

Figure 11. Data Word for Control Information

Table 4. Frequency Programming Range

INPUT		$\frac{f_{ref}}{32}$ = 1kHz	$\frac{f_{ref}}{32}$ = 1.25kHz
AM	f_{min} =	512kHz	640kHz
	f_{max} =	32767kHz	40958.75kHz
FM	f_{min} =	5.12MHz	6.40MHz
	f_{max} =	327.67MHz	409.5875MHz

Any crystal with a series resistance of not more than 150 ohms will do. As crystal frequencies are normally specified for a certain external capacitance, a series capacitor, C11, should be connected in series with the crystal, Y1. If the crystal spec is properly chosen, a fixed capacitor will normally do. If we assume a mis-alignment of 50 ppm the resulting VCO frequency of e.g. 100MHz would be offset by 5kHz, i.e. half the step size. That is normally unimportant. In special applications, however, it might be necessary to tune the crystal. There is room for a series trimmer capacitor on the p.c. board.

Another way of generating the reference frequency is the use of an external 4MHz source of satisfactory stability. In Figure 8 it is shown how to connect such an external source.

Please note that the stray capacitance at pin 17 should not exceed 8pF.

Transmitting Data to the SAA1057

All information is entered serially into the SAA 1057. The timing of the CBUS data transmission is shown in Figure 9.

There are two checks performed on data received in the SAA1057

- a test for the start bit
- a test for correct word length.

The start bit is tested during the high time of the first clock pulse. It has to be '0' to indicate the beginning of a proper transmission.

The word length is defined as the number of clock pulses during the time interval DLEN = '1', i.e. the number of data bits plus 1

Table 5. Phase Detector Mode

PDM1	PDM0	DIGITAL PD
0	0	Automatic on/off
0	1	Automatic on/off
1	0	On
1	1	Off

Table 6. TEST Signals

T3	T2	T1	T0	OUTPUT AT TEST (PIN 18)
0	0	0	0	Reference frequency
0	1	0	0	Output of prog. divider
0	0	0	1	Output of in-lock detector low = out-of-lock high = in-lock
0	1	0	1	

Table 7. Control Information

TRANSMISSION	SB2	SLA	PDM1	PDM0
Control 1	1	0	0	X
Control 2	1	1	0	X
Control 3	1	1	1	1

X = don't care

(start bit). The word length for the SAA1057 is 17.

Correctly received data are transferred to their latch by another pulse on the CLCK line, the so-called load pulse. Clock pulses need not be symmetric; however, minimum high and low times should be observed.

Due to internal data shifting there is a time after the reception of the load pulse during which the SAA1057 does not react to information on the CBUS lines. This time is called busy time. Under worst case conditions this busy time is as long as 1.3 milliseconds, i.e. a following data transmission to the SAA1057 must not start before 1.3 milliseconds have passed since the trailing edge of the load pulse. If the following transmission is, however, intended for a different device, e.g. a display driver, it may start as early as 5μs after the load pulse for the SAA1057.

Frequency Information

The organization of the data word for the setting of frequency is shown in Figure 10.

Frequency is expressed as a dividing number, N, for the programmable divider according to the following formulae:

$$N_{AM} = \frac{32 \cdot f_{OSC,AM}}{f_{ref}} \quad (23)$$

$$N_{FM} = \frac{32 \cdot f_{OSC,FM}}{10 \cdot f_{ref}} \quad (24)$$

with f_{OSC} being the VCO frequency (normally the sum of tuning frequency and i.f.) and

f_{ref} being the reference frequency at the digital PD of either 32kHz or 40kHz.

The dividing number has then to be converted to binary notation in a 15 bit format as shown in Figure 10 and a '0' added for the register select bit, thereby defining latch A as the destination of the data word.

Due to the applied divider principle, the minimum dividing number is $N_{min} = 512$. In case a smaller value is transmitted, N = 512 will be programmed. The maximum dividing number of $N_{max} = 32767$ results from the 15 bit length. The total programming range of the SAA1057 is given in Table 4.

Concerning the usability of the given programming range the frequency limits of the SAA1057 (AM: 0.512 to 32MHz, FM: 60 to 120MHz) as well as any relevant licensing regulations (e.g. FCC, GPO etc.) have to be observed.

Control Information

The organization of the data word for the transmission of control information is shown in Figure 11.

By setting the control bits either low or high the mode of operation of the SAA1057 is programmed. The register select bit is always '1' to define latch B as the destination of control information.

Control bit FM — With the control bit FM either the frequency at the AM input (FM = '0') or one tenth of the frequency at the FM input (FM = '1') is switched to the input of the programmable divider. In AM mode (FM = '0') a part of the FM signal path is switched off in order to reduce the current drain of the chip.

Control bit REFH — With the control bit REFH the reference divider can be programmed for two different dividing numbers, $N_{r0} = 125$ and $N_{r1} = 100$. In connection with the 4MHz reference oscillator this results in the reference frequencies $f_{r0} = 32$kHz and $f_{r1} = 40$kHz and the sampling frequencies $f_{s0} = 1$kHz (REFH = '0') and $f_{s1} = 1.25$kHz (REFH = '1'), respectively.

Control bits CP3 to CP0 — With the control bits CP3 through CP0 the gain of the gain-programmable current amplifier is influenced. In addition to a minimum gain there are 4 steps available which may be combined at will. In Table 2 there are given some programming examples and the resulting loop filter input currents under control of the digital PD. With a given loop filter the PLL gain can be changed under software control in a range of 1 to 100 with intermediate values resulting from programming of bit combinations. The current from the analog PD depends on the amount of phase error and the supply voltage, V_{CC2}, as outlined in section 3.4. See also Table 3 for some current values.

Control bit SB2 — With the control bit SB2 it can be chosen whether the features/test bits (lower half of control word) shall be used (SB2 = '1') or not (SB2 = '0'). In case of SB2 = '0' the lower 8 bits of the control word are interpreted as all "zeros" independent of the actual transmitted bit pattern. Please note, that the length of the control word must not be shortened in view of the format requirements of the SAA1057. In case of SB2 = '1' the actual value of the lower 8 bits is used.

Control bit SLA — With this control bit it can be chosen whether transmitted frequency information is loaded into the programmable divider immediately after reception (SLA = '0') or synchronized to the sampling frequency (SLA = '1').

Asynchronous loading is mandatory for frequency changes of more than 31 tuning steps, e.g. when recalling a pre-programmed station from memory. Synchronous loading (SLA = '1') is recommended for manual tuning without muting in order to minimize tuning noise.

Control bits PDM1, PDM0 — With these control bits the operating mode of the phase detectors is selected according to Table 5.

The meaning of automatic on/off is that in case of a phase error exceeding the operating range of the analog PD the digital PD is automatically switched on. It is switched off again as described in section 2.5, i.e. if the analog PD's operating range has not been

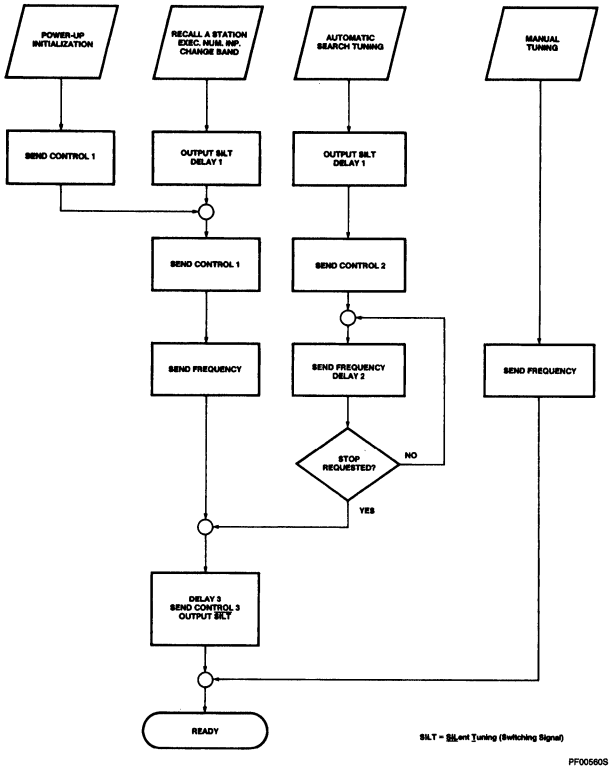

Figure 12. Data Sequences for the Synthesizer

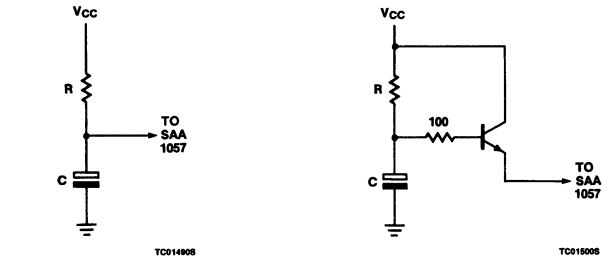

Figure 13. Power Supply Filtering

exceeded during three consecutive sampling periods. For the in-lock condition it is recommended to switch the digital PD permanently off in order to improve the digital PD permanently off in order to improve the VCO's spectral purity. Otherwise, induced disturbances could cause a temporary out-of-lock condition and, thus, an audible noise.

Control bit BRM — With this control bit the bus receiver mode is selected, i.e. whether the bus receiver is permanently switched on (BRM = '0') or automatically switched off after each data transmission (BRM = '1') in order to reduce the current drain.

Control bits T3 to T0 — These bits are test bits. T3 and T1 must always be programmed low. With T2 and T0 a few internal signals can be put out at pin 18 (TEST) as shown in Table 6.

Software Considerations

After power has been applied to the SAA 1057, an initialization must be performed before any meaningful data transmission takes place. This initialization can either consist of a train of at least 10 clock pulses on the CLCK line and afterwards a transmission of control information (word B) or by transmitting that control information twice, as it contains a sufficient number of clock pulses.

A number of radio tuning operations is executed with the audio part being mute in order to suppress any tuning noise. This applies to recalling of stored stations, executing numerical frequency inputs, changing of wave bands and to automatic search tuning. During manual tuning undistorted listening should be possible. From the above there result a few different sequences of data transmissions from a μC to the SAA1057, as shown in Figure 12.

It is assumed that at power-up the receiver is silent. Therefore, no SILT signal need be output to operate switching or squelch circuitry.

In Table 7 a proposal is made for a few control bits which are not dictated by tuner characteristics or test signals.

FM and REFH depend on the current waveband and the desired VCO step size. CP3 to CP0 depend on the tuner characteristics and tuning time specification, their programming need not be the same for each control word. The word "control 3" sets the synthesizer to synchronous loading of frequency data, i.e. no extra control information is required in case of manual tuning, and switches the digital phase detector off for best spectral purity of the tuner's VCO.

The different delays shown in Figure 12 serve for the following purposes. 'Delay 1' is intended to permit the audio squelch circuitry to reach a certain muting depth before tuning changes. The time is typically in the range between 0 and 50 milliseconds. 'Delay 2' is to adjust search tuning sweep speed to a specified value. The time depends largely on the frequency step size and on receiver time constants. In case of the minimum step size there might be no delay allowed at all. Time is typically between 0 and 50 milliseconds. Dur-

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ing 'delay 3' the actual tuning process takes place. In order to permit any frequency to be tuned to, this time is normally between 200 and 500 milliseconds.

The path for manual tuning in Figure 12 depends on the type of actuator, e.g. tuning knob or plus/minus buttons. In case of a tuning knob the tuning speed depends on the user's action. In case of plus/minus buttons and one step per operation it is nearly the same. But in case of an auto-repeat function some time delay is required to adjust the speed, as shown for the path of automatic search tuning.

Please note, that between consecutive transmissions to the SAA1057 there has to be a minimum time delay of 1.3 milliseconds (SLA = '1'). This need not necessarily be a restriction, as processing of data in the microcomputer, e.g. BCD to binary conversion or operating a display driver, also takes time.

Power Supply Requirements

As shown in Figure 2, two different supply voltages are required for the SAA1057. $V_{CC1/2}$ is between 3.6 and 12 volts and V_{CC3} between V_{CC2} and 31 volts, depending on the varactor diodes used in the tuner. If the full programming range of the gain-programmable current amplifier is to be used, $V_{CC1/2}$ should, however, not be less than 5 volts.

Power supply ripple cannot be neglected because of the limited ripple rejection of the SAA1057. For the calculation of permissible power supply ripple let us assume the following:

- we use an FM tuner
- the maximum slope is S_{VCO} = 3MHz/V
- the desired signal-to-noise ratio is SNR = 75dB
- SNR is based on a deviation of $\Delta f = \pm$ 40kHz
- SNR depends on supply ripple only

From the data sheet it can be seen that the rejection of V_{CC2} and V_{CC3} ripple is dominating. If we assume both voltages to be of equal influence each of them has to give an SNR which is 3dB better than specified. The permissible supply ripple voltage (peak-to-peak) can be calculated from

$$V_{r,\,VCCi} = \frac{2 \cdot \Delta f}{S_{VCO}} \cdot 10^{\frac{(r_{VCCi} - SNR - 3dB)}{20}} \qquad (25)$$

with i = 2 or 3, indicating V_{CC2}, V_{CC3}
r_{VCCi} = ripple rejection of V_{CCi} in dB

For the data assumed above we will get
$V_{r,VCC2}$ = 0.6mV peak-to-peak
$V_{r,VCC3}$ = 6mV peak-to-peak

In other words, if the power supply ripple in the basic application of Figure 2 is not greater than indicated above, an overall signal-to-noise ratio of 75dB can be achieved with a VCO slope of 3MHz/V and no other noise sources being present.

If, however, the actual power supply ripple is larger than the limit calculated for a desired SNR, additional filtering has to be used. The design of a filter circuit depends on the permitted voltage drop. If a drop of several volts is acceptable, a circuit as given in Figure 13a can be used. If the drop should be less than 1 volt, Figure 13b could be used.

Let us assume that a stabilized supply voltage of 8 volts with a maximum ripple of 5 millivolts peak-to-peak is available. We choose the filter circuit of Figure 13a to generate the supply voltage $V_{CC1/2}$. The attenuation is given by

$$a = 20 \cdot \log\sqrt{1 + (\omega RC)^2} \qquad (26)$$

The required attenuation is 20 · log (5/0.6) = 18.5dB. In order not to operate the SAA1057 below 5 volts, the drop across R should be less than 3 volts. Thus,

$$R_{max} = \frac{3 \text{ volts}}{18mA} = 167\Omega$$

We select
R = 150Ω
C = 100µF

and obtain an attenuation of
a = 21dB @ f_r = 120Hz

Now let us calculate component values for Figure 13b as a filter for V_{CC3}. Let us assume a supply voltage of 30 volts with a ripple of 1 volt peak-to-peak and a maximum tuning voltage of 27 volts. The allowed voltage drop should be less than 1 volt. The required filter attenuation is 20 log (1/0.006) = 44.4dB. Again the attenuation is given by Equation (26). The voltage drop is

$$\Delta V = V_{BE} + \frac{I_E \cdot R}{B} \qquad (27)$$

with

I_E = load current = I_{CC3}

B = DC gain of transistor

We select
R = 10kΩ
C = 22µF

and obtain
a = 44.4dB @ fr = 120Hz
ΔV = 0.7 volts @V_{BE} = 0.6 volts
B = 100
I_E = 1mA

In case of higher attenuation, i.e. a larger time constant R · C, a speed-up path for a quick charging of C at power-on should be provided. Otherwise, V_{CC3} could reach its nominal value too late and tuning to the desired frequency can be delayed.

SUMMARY

This report has described a new microcomputer-controlled AM/FM radio PLL frequency synthesizer IC, the SAA1057, and its basic application.

There are several unique design ideas realized in the IC. The most important is the combination of a digital and an analog phase detector, giving improvements in tuning speed as well as in spectral purity of the VCO. The use of the same reference frequency for both AM and FM tuning simplifies the design of the loop filter. The PLL gain can be programmed in a range of 1 to 100 under software control, thereby eliminating the need for switching of external loop filter components.

For the basic application to AM/FM radios there is information given on hardware, software, power supply and a design example for the calculation of the loop filter.

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APPENDIX

Design Example

Based on the Circuit Diagram of Figure 2 a PLL frequency synthesizer for an FM radio shall be designed. The following tuner data are given:

tuning range	$f_{r.f.}$ = 88 to 108MHz
tuning steps	$\Delta f_{r.f.}$ = 10kHz
intermediate frequency	$f_{i.f.}$ = 10.70MHz
tuning voltage	V_{tune} = 4 to 28 volts
VCO gain	S_{VCO} = 3.0 to 0.3MHz/V

S_{VCO} is assumed to decrease linearly from the low end of the tuning range to the high end.

From the tuning step size it is obvious to use REFH = 0, i.e. 32kHz reference frequency. Using Equation (24) we can calculate the min and max values of the dividing number, N, for the programmable divider:

$N_{min} = 9870$
$N_{max} = 11870$

The tuning time from one end of the band to the other is assumed to be not longer than 0.4 seconds. If we split this time into equal parts for the slew and settle times, we can calculate capacitor C4 by rewriting equation (15) as

$$C4 \approx \frac{t_{slew} \cdot I_{dig}}{2 \cdot \Delta V_{tune}} \qquad (15a)$$

For the first trial a medium value is taken for the loop filter current, e.g.

$I_{dig} = 0.1mA$ (CP = 0010)

We then get from Equation (15a)

$C4 \approx 0.4\mu F$

We choose the closest standard capacitor value of

$C4 = 0.33\mu F$

and calculate an approximate slew time of

$t_{slew} \approx 0.16$ seconds

Now we have to determine the lower limit of the loop's natural frequency and see if the actual frequency is larger. From Figure 6 we read $\omega_n t = 7$ for a maximum overshoot of 1 o/o at an optimum damping factor of 0.7. We re-write Equation (16) as

$$\omega_n = \frac{\omega_n \cdot t}{t_{settle}} \qquad (16a)$$

and calculate

$\omega_{n,min} \geq 35 s^{-1}$

with $t_{settle} = 0.2$ seconds being our initial assumption. Using Equation (12) we calculate the loop's natural frequency for the low and high ends of the tuning range.

$\omega_{n,low} = 304\ s^{-1}$
$\omega_{n,high} = 88\ s^{-1}$

As both values are well above the minimum, the settling time will not be larger than assumed and we will not have to change the assumptions made so far.

Now, we have to solve for resistor, R2. Looking at Equation (11) we quickly realize that the damping factor, ζ, will change with ω_n, thereby influencing the overshoot. Let us try to solve this dilemma by calculating R2 for the mid of the tuning range. We take

$N = 10870$
$S_{VCO} = 1.7MHz/V$
$I_{dig} = 0.1mA$
$\zeta = 0.7$
$C4 = 0.33\mu F$

and get

$\omega_n = 218\ s^{-1}$
$R2 = 19500$ ohms

We choose a standard resistor value of

$R2 = 18k\Omega$

and check the damping factor with the aid of Equation (11) at the ends of the tuning range end get

$\zeta_{low} = 0.87$
$\zeta_{high} = 0.25$

The low end value is still good. At the high end the response is highly under-damped, resulting in $\omega_n t = 18$ for a maximum overshoot of 1 o/o. That would mean a settling time of

$t_{settle} = 0.2$ seconds

which is equal to our assumption. In reality, the digital phase detector will be switched off earlier due to the action of the analog PD. Thus, tuning from one end of the band to the other is achieved in less than 0.4 seconds. If the calculated damping factor ζ_{high} is regarded too small, a new calculation can be started with a higher current gain, e.g. $I_{dig} = 0.3mA$ (CP = 0110). This would result in $\zeta_{high} = 0.45$ and $\zeta_{low} = 1.56$ which is now too large.

For normal applications it seems to be satisfactory to use only one value for the gain-programmable amplifier. Using more than one value within one wave-band requires additional software in the μC because the tuning frequency has to be checked against some cross-over frequency.

For the low-pass filter, R3 and C5, we get from Equation (5) by using $\omega_n = \omega_{n,low}$

$4.6ms > R3 \cdot C5 > 0.32ms$

We choose the filter time constant to be 1 millisecond, resulting in component values of e.g.

$R3 = 10k\Omega$
$C5 = 0.1\mu F$

As the filter capacitor might be designed in view of r.f. reasons, a modification may be necessary which, however, should include R3 to maintain the time-constant of the low-pass filter.

ADDENDUM

The currently available samples of the SAA1057 are stamped as N 1653. These samples require an extra current of approximately 10 microamps at room temperature into pin 4. This extra current can most easily be realized by connecting a resistor between pins 4 and 16. In this case, the supply voltage $V_{CC1/2}$ shall not be changed, once a resistor value has been fixed. For a nominal supply voltage of $V_{CC1/2} = 5$ volts, a resistor value of 270k ohms is an adequate solution at room temperature. At ambient temperatures above approx. 40 to 45°C it may be necessary to increase the resistor value.

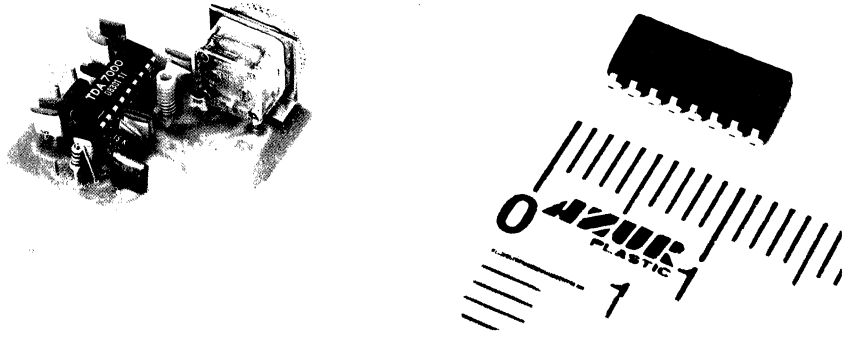
A Complete FM Radio on a Chip

AN192

W. H. A. VAN DOOREMOLEN and M. HUFSCHMIDT

Until now, the almost total integration of an f.m. radio has been prevented by the need for LC tuned circuits in the r.f., i.f., local-oscillator and demodulator stages. An obvious way to eliminate the coils in the i.f. and demodulator stages is to reduce the normally used intermediate frequency of 10.7 MHz to a frequency that can be tuned by active RC filters, the op-amps and resistors of which can be integrated. An i.f. of zero seems to be ideal because it eliminates spurious signals such as repeat spots and image response, but it would not allow the i.f. signal to be limited prior to demodulation, resulting in poor S/N ratio and no a.m. suppression. With an i.f. of 70 kHz, these problems are overcome and the image frequency occurs about halfway between the desired signal and the centre of the adjacent channel. However, the i.f. image signal must be suppressed and, in common with conventional f.m. radios, there is also a need to suppress interstation noise and noise when tuned to a weak signal. Spurious responses above and below the centre frequency of the desired station (side tunings), and harmonic distortion in the event of very inaccurate tuning must also be eliminated.

We have now developed a mono f.m. reception system which is suitable for almost total integration. It uses an active 70 kHz i.f. filter and a unique correlation muting circuit for suppressing spurious signals such as side responses caused by the flanks of the demodulator S-curve. With such a low



A laboratory model of the TDA7000 in a complete f.m. radio. Also shown is the TDA7010T in the SO package against a cm scale.

A Complete FM Radio on a Chip AN192

i.f., distortion would occur with the ±75 kHz i.f. swing due to received signals with maximum modulation. The maximum i.f. swing is therefore compressed to ±15 kHz by controlling the local-oscillator in a frequency locked loop (FLL). The combined action of the muting circuit and the FLL also suppresses image response.

The new circuit is the TDA7000 which integrates a mono f.m. radio all the way from the aerial input to the audio output. External to the IC are only one tunable LC circuit for the local-oscillator, a few inexpensive ceramic plate capacitors and one resistor. The TDA7000 dramatically reduces assembly and post-production alignment costs because only the oscillator circuit needs adjustment during manufacture to set the limits of the tuned frequency band. The complete f.m. radio can be made small enough to fit inside a calculator, cigarette lighter, key-ring fob or even a slim watch. The TDA7000 can also be used as a receiver in equipment such as cordless telephones, CB radios, radio-controlled models, paging systems, the sound channel of a tv set or other f.m. demodulating systems.

Using the TDA7000 results in significant improvements for all classes of f.m. radio. For simpler portables, the small size, lack of i.f. coils, easy assembly and low power consumption are not the only attractive features. The unique correlation muting system and the FLL make it very easy to tune, even when using a tiny tuning knob. For higher-performance portables and clock radios, variable-capacitance diode tuning and station presetting facilities are often required. These are easily provided with the TDA7000 because there are no variable tuned circuits in the r.f. signal

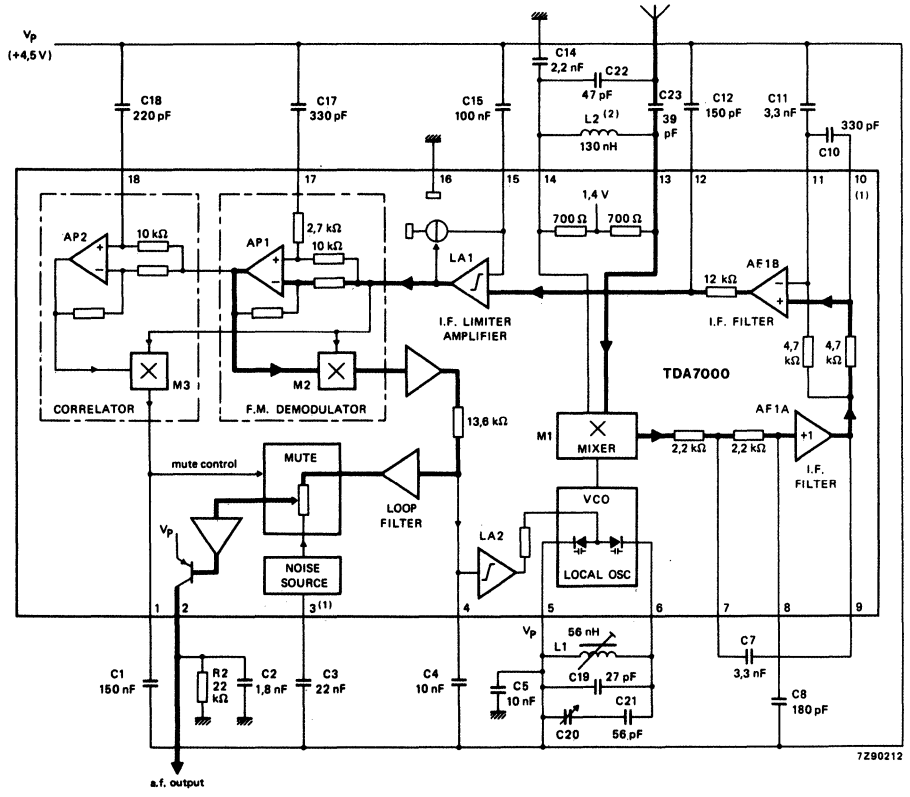


Fig.1 The TDA7000 as a variable capacitor tuned f.m. broadcast receiver

1) These pins are not used in the SO package version (TDA7010T)
AP = All-Pass filter.

2) L_2 is printed on the experimental PCB (Fig.12).
L_1 = Toko MC108 No.514 HNE 150013S13.
C_{20} = Toko No. 2A-15BT-R01.

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path. Only the local-oscillator needs to be tuned, so tracking and distortion problems are eliminated.

The TDA7000 is available in either an 18-lead plastic DIL package (TDA7000), or in a 16-pin SO package (TDA7010T). Future developments will include reducing the present supply voltage (4.5 V typ.), and the introduction of f.m. stereo and a.m./f.m. versions.

BRIEF DATA

typical supply voltage	V_p	4.5 V
typical supply current	I_p	8 mA
r.f. input frequency range	f_{rf}	1.5 to 110 MHz
sensitivity for −3 dB limiting e.m.f. with $Z_S = 75\Omega$, mute disabled	$V_{rf\text{-}3\,dB}$	1.5 μV
maximum signal input for THD < 10%, $\Delta f = \pm 75$ kHz e.m.f. with $Z_S = 75\Omega$	V_{rf}	200 mV
audio output (r.m.s.) with $R_L = 22\,k\Omega$, $\Delta f = \pm 22.5$ kHz	V_o	75 mV

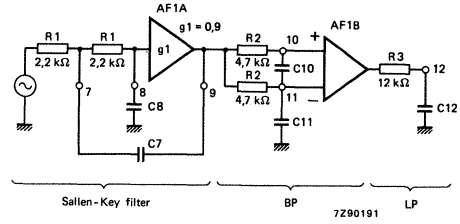
CIRCUIT DESCRIPTION

As shown in Fig.1, the TDA7000 consists of a local-oscillator and a mixer, a two-stage active i.f. filter followed by an i.f. limiter/amplifier, a quadrature f.m. demodulator, and an audio muting circuit controlled by an i.f. waveform correlator. The conversion gain of the mixer, together with the high gain of the i.f. limiter/amplifier, provides a.v.c. action and effective suppression of a.m. signals. The r.f. input to the TDA7000 for −3 dB limiting is 1.5 μV. In a conventional portable radio, limiting at such a low r.f. input level would cause instability because higher harmonics of the clipped i.f. signal would be radiated to the aerial. With the low i.f. used with the TDA7000, the radiation is negligible.

To prevent distortion with the low i.f. used with the TDA7000, it is necessary to restrict the i.f. deviation due to heavily modulated r.f. signals to ±15 kHz. This is achieved with a frequency-locked loop (FLL) in which the output from the f.m. demodulator shifts the local-oscillator frequency in inverse proportion to the i.f. deviation due to modulation.

Active i.f. filter

The first section of the i.f. filter (AF1A) is a second-order low-pass Sallen-Key circuit with its cut-off frequency determined by internal 2.2 kΩ resistors and external capacitors C_7 and C_8. The second section (AF1B) consists of a first-order bandpass filter with the lower limit of the passband determined by an internal 4.7 kΩ resistor and external capacitor C_{11}. The upper limit of the passband is determined by an internal 4.7 kΩ resistor and external capacitor C_{10}. The final section of the i.f. filter consists of a first-order low-pass network comprising an internal 12 kΩ resistor and external capacitor C_{12}. The overall i.f. filter therefore consists of a fourth-order low-pass section and a first-order high-pass section. Design equations for the filter are given in Fig.2. Figure 3 shows the measured response for the filter.



Sallen-Key circuit

$$A_{SK} = \frac{g}{1 + j\omega a - \omega^2 b} \qquad \text{with } a = 2R_1C_8,\ b = R_1^2C_7C_8$$

$$\text{With } f_0 = \frac{1}{2\pi R_1\sqrt{(C_7C_8)}} \text{ and } Q = \frac{\sqrt{b}}{a} = 0.5\sqrt{\frac{C_7}{C_8}}$$

$$A_{SK} = \frac{g}{1 + \left(j\,\frac{\omega}{\omega_o} \times \frac{1}{Q}\right) - \frac{\omega^2}{\omega_o^2}}$$

For $C_7 = 3.3$ nF, $C_8 = 180$ pF; $Q = 2.1$ and $f_o = 94$ kHz

Bandpass circuit

$$A_{BP} = \frac{1}{1 + j\omega C_{10}R_2} \times \frac{j\omega C_{11}R_2}{1 + j\omega C_{11}R_2 + \frac{j\omega C_{10}R_2}{1 + j\omega C_{10}R_2}}$$

$$\text{for } f_{LP} = \frac{1}{2\pi R_2 C_{10}} \text{ and } f_{HP} = \frac{1}{2\pi R_2 C_{11}}$$

$$A_{BP} = \frac{f_{LP}}{f_{HP}} \times \frac{1}{\left(1 + j\,\frac{f}{f_{HP}}\right)\left(1 - j\,\frac{f_{LP}}{f}\right) + 1}$$

For $C_{10} = 330$ pF, $C_{11} = 3.3$ nF; $f_{LP} = 103$ kHz, $f_{HP} = 10.3$ kHz

Low-pass circuit

$$A_{LP} = \frac{1}{1 + j\omega C_{12}R_3}$$

$$\text{for } f_{LP} = \frac{1}{2\pi C_{12}R_3}$$

$$A_{LP} = \frac{1}{1 + j\,\frac{\omega}{\omega_{LP}}}$$

For $C_{12} = 150$ pF; $f_{LP} = 88.4$ kHz.

Fig.2 I.F. filter of the TDA7000

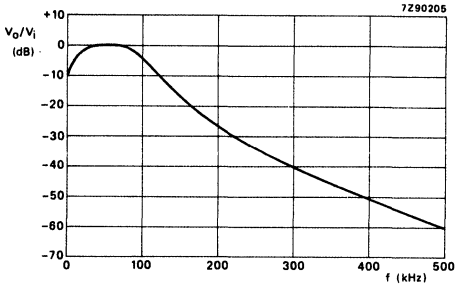
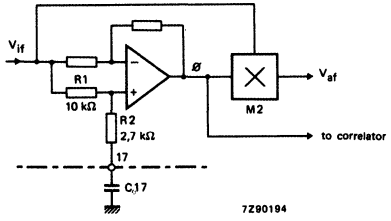


Fig.3 Measured response of the i.f. filter

F.M. demodulator

The quadrature f.m. demodulator M2 converts the i.f. variations due to modulation into an audio frequency voltage. It has a conversion gain of −3.6 V/MHz and requires phase quadrature inputs from the i.f. limiter/amplifier. As shown in Fig.4, the 90° phase shift is provided by an active all-pass filter which has about unity gain at all frequencies but can provide a variable phase shift, dependent on the value of external capacitor C_{17}.



With $R_2 = 0$,

$\phi = -2 \tan^{-1} \omega R_1 C_{17}$

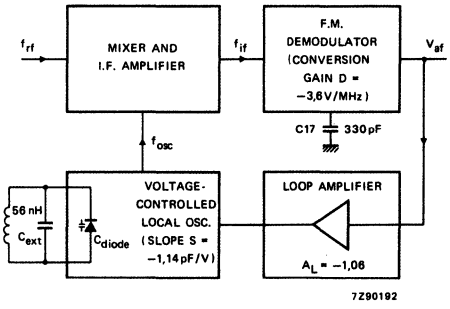
for $\phi = -90°$, $C_{17} = \frac{1}{\omega R_1}$, = 227 pF for f_{if} = 70 kHz.

To improve the performance of the all-pass filter with the amplitude limited i.f. waveform, R_2 has been added. Since this influences the phase angle, the value of C_{17} must be increased by 45% i.e. to 330 pF for f_{if} = 70 kHz.

Fig.4 F.M. demodulator phase shift circuit (all-pass filter)

I.F. swing compression with the FLL

With a nominal i.f. as low as 70 kHz, severe harmonic distortion of the audio output would occur with an i.f. deviation of ±75 kHz due to full modulation of a received f.m. broadcast signal. The FLL of the TDA7000 is therefore used to compress the i.f. swing by using the audio output from the f.m. demodulator to shift the local-oscillator frequency in opposition to the i.f. deviation. The principle is illustrated in Fig.5, which shows that an i.f. deviation of 75 kHz is compressed to about 15 kHz. The THD is thus limited to 0.7% with ±22.5 kHz modulation, and to 2.3% with ±75 kHz modulation.



$C_o = C_{ext} + C_{stray} + C_{diode}$ with open loop = 49 pF at f_o = 96 MHz

feedback factor $\beta = \frac{A_L S f_o}{2C_o}$

open loop conversion gain = D = −3.6 V/MHz

closed loop conversion gain = $\frac{D}{1 + D\beta}$ = 0.68 V/MHz for f_o = 96 MHz

modulation compression factor $K = \frac{\text{open loop gain}}{\text{closed loop gain}} = \frac{3.6 \text{ V/MHz}}{0.684 \text{ V/MHz}} \approx 5$

$\Delta f_{osc} = \Delta f_{rf} \left(1 - \frac{1}{K}\right)$

$\Delta f_{if} = \frac{\Delta f_{rf}}{K}$

for Δf_{rf} = 75 kHz, $\Delta f_{osc} \approx$ 60 kHz, $\Delta f_{if} \approx$ 15 kHz

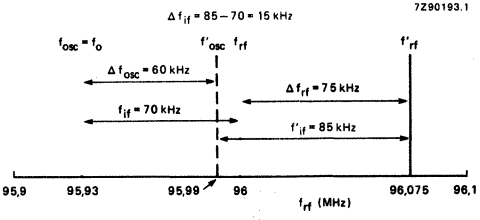


Fig.5 I.F. swing compression with the FLL

Correlation muting system with open FLL

A well-known difference between f.m. and a.m. is that, for f.m., each station is received in at least three tuning positions. Fig.6 shows the frequency spectrum of the output from the demodulator of a typical portable f.m. radio receiving an r.f. carrier frequency-modulated with a tone of constant frequency and amplitude. In addition to the audio response at the correct tuning point in the centre of Fig.6, there are two side responses due to the flanks of the demodulator S-curve. Because the flanks of the S-curve are non-linear the side responses have increased harmonic distortion. In Fig.6, the frequency and intensity of the side responses are functions of the signal strength, and they are

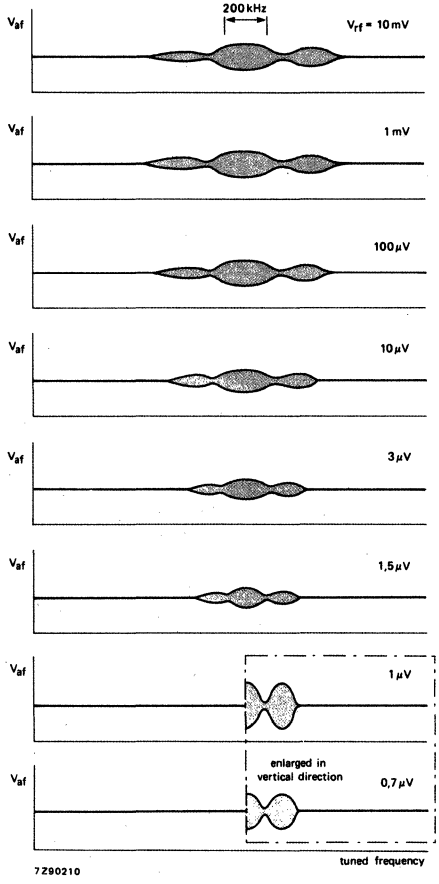


Fig.6 Audio signal of a typical portable radio as a function of tuned frequency with r.f. input as a parameter. The modulation frequency and amplitude are both constant

separated from the correct tuning point by amplitude minima. However, in practice, the amplitude minima are not well defined because the modulation frequency and index are not constant and moreover, the side responses of adjacent channels often overlap.

High performance f.m. radios incorporate squelch systems such as signal-strength-dependent muting and tuning-deviation-dependent muting (Ref.1) to suppress side responses. They also have a tuning meter to facilitate correct tuning. Although the TDA7000 is mainly intended for use in portables and clock radios, it incorporates a very effective new correlation muting system which suppresses interstation noise and spurious responses due to detuning to the flanks of the demodulator S-curve. The muting system is controlled by a circuit which determines the correlation between the waveform of the i.f. signal and an inverted version of it which is delayed (phase shifted) by half the period of the nominal i.f. (180°). A noise generator works in conjunction with the muting system to give an audible indication of incorrect tuning.

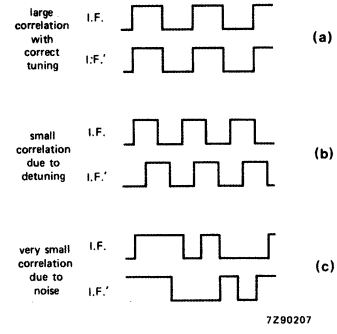
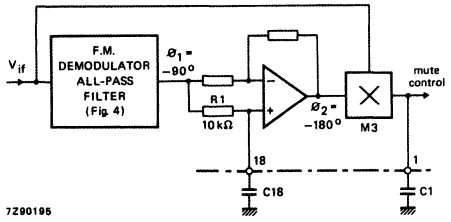


Fig.7 Function of the correlation muting system

Figure 7 illustrates the function of the muting system. Signal IF′ is derived by delaying the i.f. signal by half the period of the nominal i.f. and inverting it. With correct tuning as shown in Fig.7(a), the waveform of the two signals are identical resulting in large correlation. In this situation, the audio signal is not muted. With detuning as shown in Fig.7(b), signal IF′ is phase-shifted with respect to the i.f. signal. The correlation between the two waveforms is therefore small and the audio output is muted. Figure 7(c) shows that, because of the low Q of the i.f. filter, noise causes considerable fluctuations of the period of the i.f. signal waveform. There is then small correlation between the two waveforms and the audio is muted. The correlation muting system thus suppresses noise and side responses due

to detuning to the flanks of the demodulator S-curve. Since the mute threshold is much lower than that obtained with most other currently used muting systems, this muting system is ideal for portable radios which must often receive signals with a level only slightly above the input noise.



$$\phi_2 = -2 \tan^{-1} \omega R_1 C_{18} - \phi_1$$

$$\text{for } \phi_2 = -180°\ C_{18} = \frac{1}{\omega R_1}$$

$$\text{for } f_{if} = 70\ \text{kHz}, C_{18} = 227\ \text{pF}.$$

Fig.8 Correlator of the TDA7000

As shown in Fig.8, the correlation muting circuit consists of all-pass filter AP2 connected in series with f.m. demodulator all-pass filter AP1 and adjusted by an external capacitor to provide a total phase shift of 180°. The output from AP2 is applied to mixer M3 which determines the correlation between the undelayed limited i.f. signal at one of its inputs and the delayed and inverted version of it at its other input. The output from mixer M3 controls a muting circuit which feeds the demodulated audio signal to the output when the correlation is high, or feeds the output from a noise source to the output to give an audible indication of incorrect tuning when the correlation is low. The switching of the muting circuit is progressive (soft muting) to prevent the generation of annoying audio transients. The output from mixer M3 is available externally at pin 1 and can also be used to drive a detuning indicator.

Figure 9 shows that there are two regions where the demodulated audio signal is fed to the output because the muting is inactive. One region is centred on the correct tuning point f_L. The other is centred on the image frequency $-f_L$. The image response is therefore not suppressed by the muting system when the frequency-locked loop is open. When the loop is closed, the time-constant of the muting system, which is determined by external capacitor C_1, prevents the image response being passed to the audio output. This is described under the next heading.

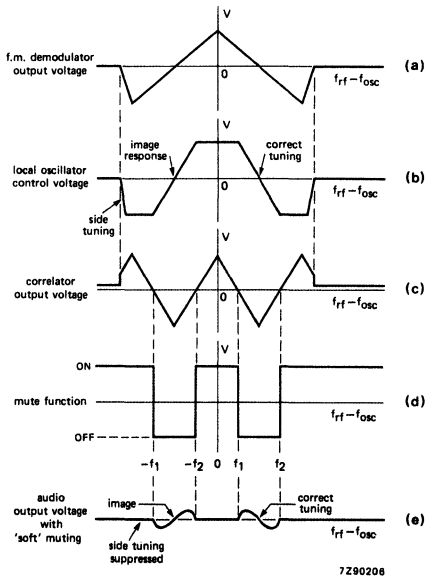


Fig.9 Operation of the correlation muting system with open-loop FLL

Correlation muting system with closed FLL

The closed-loop response of the FLL is shown in Fig.10, in which the point of origin is the nominal i.f. ($f_{rf} - f_{osc} = f_L$). With correct tuning, the muting is inactive and the audio

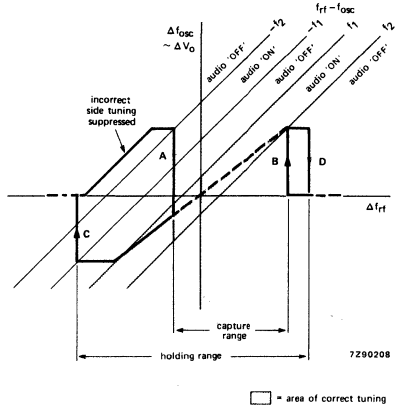


Fig.10 Closed-loop response of the FLL. The slope of the correct tuning line is such that a 75 kHz deviation of f_{rf} causes a 15 kHz deviation of $f_{rf} - f_{osc}$

signal is fed to the output. Spurious responses due to the flanks of the demodulator S-curve which occur outside the i.f. band $-f_2$ to f_2 are suppressed because the muting is active. Fast transients of the audio signal due to locking of the loop (A and B), and to loss of lock (C and D) are suppressed in two ways.

Lock and loss of lock transients B and D occur when the i.f. is greater than f_2 and are therefore suppressed because the muting is active. The situation is different during loss of lock transient C because the muting is only active for the last part of the transient. To completely suppress this transient, capacitor C_1 in Fig.1 holds the muting control line positive (muting active) during the short interval whilst the i.f. traverses from $-f_1$ to $-f_2$. The same applies for lock transient A during the short interval whilst the i.f. traverses from $-f_2$ to $-f_1$. Since the image response occurs halfway between $-f_1$ and $-f_2$, it is also suppressed.

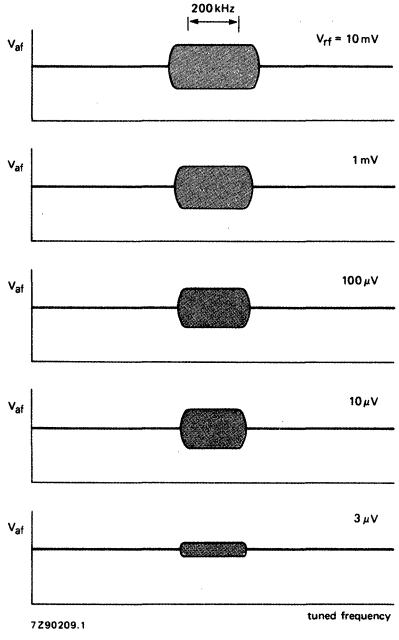


Fig.11 Audio signal of the TDA7000 as a function of the tuned frequency with r.f. input as a parameter. The modulation frequency and amplitude are both constant

Figure 11 shows the audio output from the TDA7000 radio as a function of tuned frequency with aerial signal level as a parameter. Compared with the similar diagram for a typical conventional portable radio (Fig.6), there are three important improvements:

- There are no side responses due to the flanks of the demodulator S-curve. This is due to the action of the correlation muting system (soft mute) which combines the function of a detuning-dependent muting system with that of a signal-strength-dependent muting system
- The correct tuning frequency band is wide, even with weak aerial signals. This is due to the a.f.c. action of the FLL which reduces a large variation of aerial input frequency (equivalent to detuning) to a small variation of the i.f. There is no audio distortion when the radio is slightly detuned
- Although the soft muting system remains operative with low-level aerial signals, there is no degradation of the audio signal under these conditions. This is due to the high gain of the i.f. limiter/amplifier which provides -3 dB limiting of the i.f. signal with an aerial input level of 1.5 μV. However, the soft muting action does reduce the audio output level with low level aerial signals.

RECEIVER CIRCUITS

Circuits with variable capacitor tuning

The circuit diagram of the complete mono f.m. radio shown in the frontispiece is given in Fig.1. An experimental printed-wiring board layout is given in Fig.12. Special attention has been paid to supply lines and the positioning of large-signal decoupling capacitors.

The functions of the peripheral components of Fig.1 not already described are as follows:

C_1:

Determines the time constant required to ensure muting of audio transients due to the operation of the FLL.

C_2:

Together with R_2 determines the time-constant for audio de-emphasis (e.g. $R_2C_2 = 40\,\mu s$).

C_3:

The output level from the noise generator during muting increases with increasing value of C_3. If silent mute is required, C_3 can be omitted.

C_4:

Capacitor for the FLL filter. It eliminates i.f. harmonics at the output of the f.m. demodulator. It also determines the time-constant for locking the FLL and influences the frequency response.

C_5:

Supply decoupling capacitor which must be connected as close as possible to pin 5 of the TDA7000.

C_7 to C_{12}, C_{17} and C_{18}:
Filter and demodulator capacitors. The values shown are for an i.f. of 70 kHz. For other intermediate frequencies, the values of these capacitors must be changed in inverse proportion to the i.f. change.

C_{14}:
Decouples the reverse r.f. input. It must be connected to the common return via a good quality short connection to ensure a low-impedance path. Inductive or capacitive coupling between C_{14} and the local-oscillator circuit or i.f. output components must be avoided.

C_{15}:
Decouples the d.c. feedback for i.f. limiter/amplifier LA1.

C_{19} and C_{21}:
Local-oscillator tuning capacitors. Their values depend on the required tuning range and on the value of tuning capacitor C_{20}.

C_{22}, C_{23}, L_1, L_2:
The values given are for an r.f. bandpass filter with Q = 4 for the European and U.S.A. domestic f.m. broadcast band (87.5 MHz to 108 MHz). For reception of the Japanese f.m. broadcast band (76 MHz to 91 MHz), L_1 must be increased to 78 nH and L_2 must be increased to 150 nH. If stopband attenuation for high level a.m. or tv signals is not required, L_2 and C_{22} can be omitted and C_{23} changed to 220 pF.

R_2:
The load for the audio output current source. It determines the audio output level, but its value must not exceed 22 kΩ for V_p = 4.5 V, or 47 kΩ for V_p = 9 V.

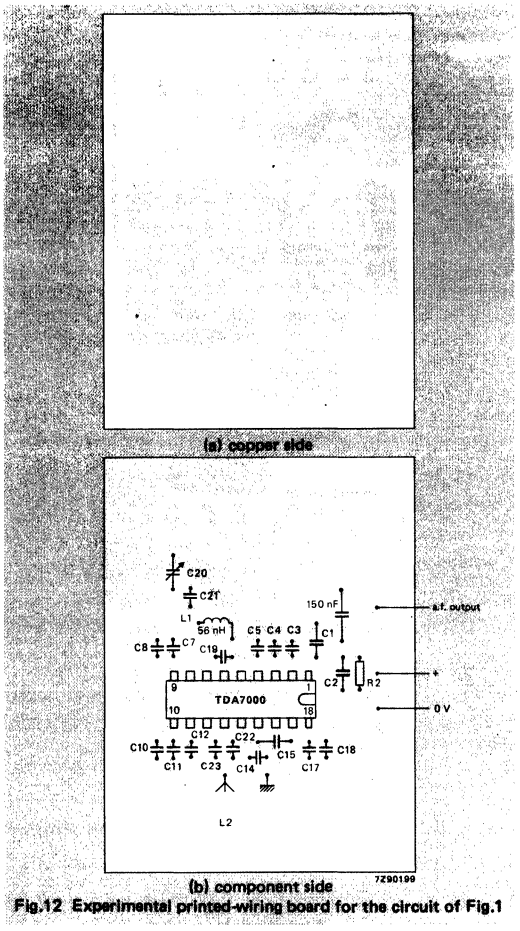
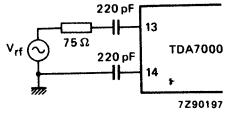


Fig.12 Experimental printed-wiring board for the circuit of Fig.1



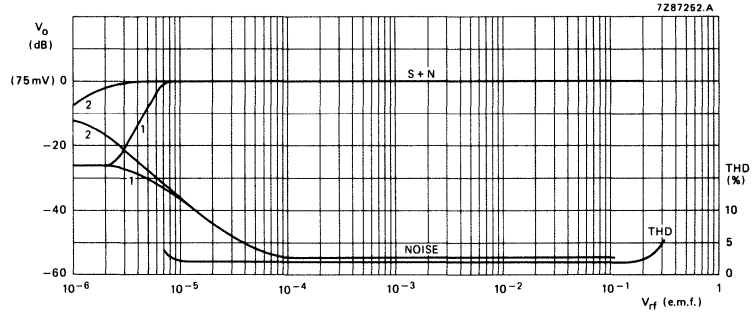


Fig.13 Audio output as a function of input e.m.f. The curves numbered 1 were measured with the muting system active. The curves numbered 2 were measured with the muting system disabled by injecting about 20 μA into pin 1 of the TDA7000. The input frequency was 96 MHz modulated with 1 kHz with a deviation of ±22.5 kHz for the output level curves, and ±75 kHz for the distortion curve

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Performance of the circuit

unless otherwise specified, V_p = 4.5 V, T_{amb} = 25 °C, f_{rf} = 96 MHz, V_{rf} = 0.2 mV e.m.f. from a 75 Ω source, modulated with Δf = ±22.5 kHz, f_m = 1 kHz. Noise voltage measured unweighted over the bandwidth 300 Hz to 20 kHz

parameter	symbol	typ.	max.	unit
sensitivity				
(e.m.f. voltage)				
for −3 dB limiting:				
muting disabled	EMF	1.5	–	μV
for −3 dB muting	EMF	6	–	μV
for (S+N)/N = 26 dB	EMF	5.5	–	μV
signal handling (e.m.f. voltage)				
for THD < 10%; Δf = ±75 kHz	EMF	200	–	mV
signal-to-noise ratio (see Fig.13)	(S+N)/N	60	–	dB
total harmonic distortion (see Fig.13)				
at Δf = ±22.5 kHz	THD	0.7	–	%
at Δf = ±75 kHz	THD	2.3	–	%
a.m. suppression				
(ratio of the a.m. output signal				
referred to the f.m. output signal)				
f.m. signal: f_m = 1 kHz; Δf = ±75 kHz				
a.m. signal: f_m = 1 kHz; m = 80%	AMS	50	–	dB
ripple rejection (ΔV_p = 100 mV;				
f = 1 kHz)	RR	10	–	dB
oscillator voltage (r.m.s. value)				
at pin 6	$V_{6\text{-}5(rms)}$	250	–	mV
variation of oscillator frequency				
with supply voltage (ΔV_p = 1 V)	Δf_{osc}	60	–	kHz/V
selectivity	S_{+300}	45	–	dB
	S_{-300}	35	–	dB
a.f.c. range	Δf_{rf}	±300	–	kHz
audio bandwidth at ΔV_o = 3 dB				
measured with pre-emphasis (t = 50 μs)	B	10	–	kHz
a.f. output voltage (r.m.s. value)				
at R_L = 22 kΩ	$V_{o(rms)}$	75	–	mV
load resistance for audio output current source				
at V_p = 4.5 V	R_L	–	22	kΩ
at V_p = 9.0 V	R_L	–	47	kΩ

Circuit with variable-capacitance diode tuning

Since it is only necessary to tune the local-oscillator coil, it is very simple to modify the circuit of Fig.1 for variable-capacitance diode tuning. The modifications are shown in Fig.14. A circuit board layout for the modified receiver and a photograph of a complete laboratory model are shown in Fig.15.

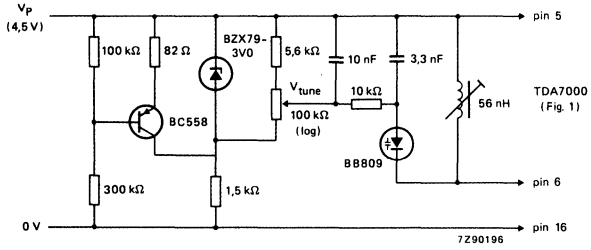

Fig.14 Variable-capacitance diode tuning for the local-oscillator. Additonal measures must be taken to ensure temperature stability

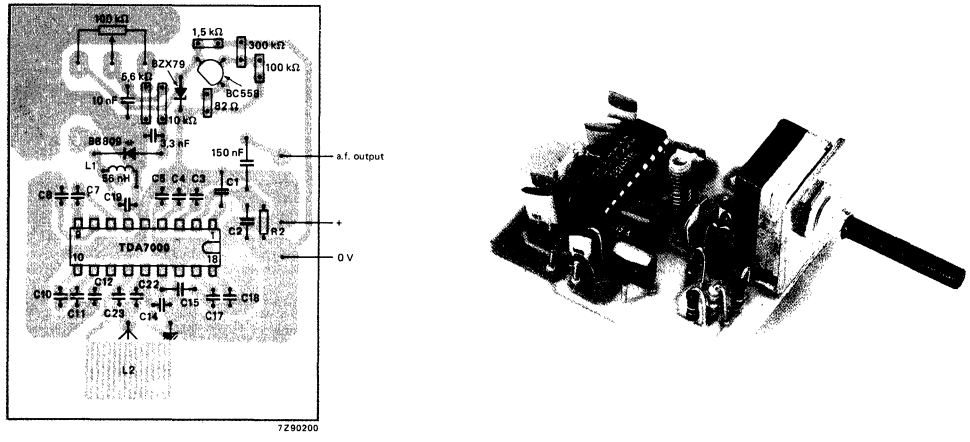

Fig.15 Circuit board layout and complete model of a TDA7000 radio with variable-capacitance diode tuning. This is the same pcb as shown in Fig.12

Narrow-band f.m. receiver

The TDA7000 can also be used for reception of narrow-band f.m. signals. In this case, the local-oscillator is crystal-controlled as shown in Fig.16 and there is therefore hardly any compression of the i.f. swing by the FLL. The deviation of the transmitted carrier frequency due to modulation must therefore be limited to prevent severe distortion of the demodulated audio signal.

The component values in Fig.16 result in an i.f. of 4.5 kHz and an i.f. bandwidth of 5 kHz (Fig.17). If the i.f. is multiplied by N, the values of capacitors C_{17} and C_{18} in the all-pass filters and the values of filter capacitors C_7, C_8, C_{10}, C_{11}, and C_{12} must be multiplied by 1/N. For improved i.f. selectivity to achieve greater adjacent channel attenuation, second-order networks can be used in place of C_{10} and C_{11}.

In this circuit the detuning noise generator is not used. Since the circuit is mainly for reception of audio signals, the audio output must be passed through a low-pass Chebyshev filter to suppress i.f. harmonics.

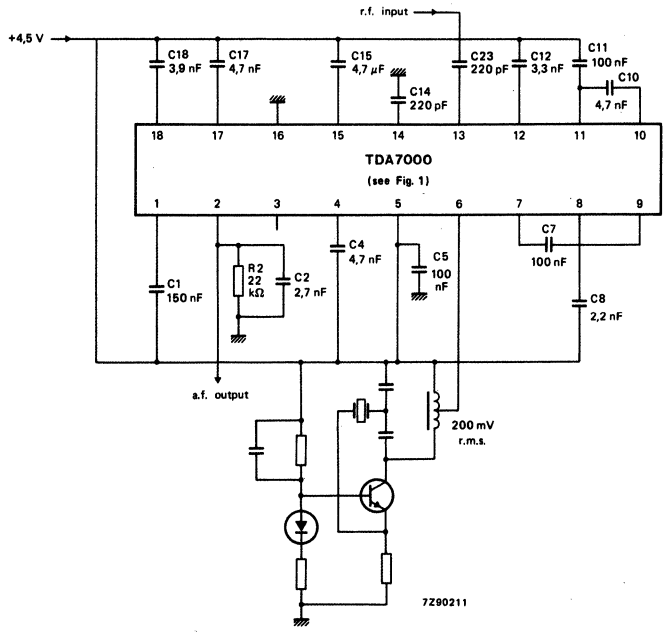

Fig.16 A narrow-band f.m. receiver with a crystal-controlled local-oscillator

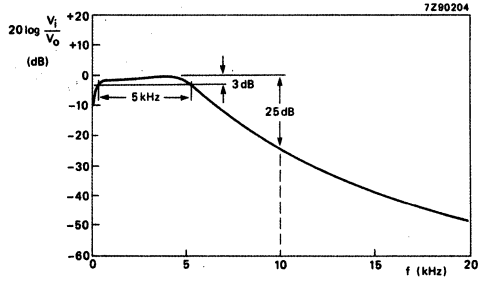

Fig.17 I.F. selectivity for the narrow-band f.m. receiver

AUDIO AMPLIFIER AND DETUNING INDICATOR CIRCUITS

Audio output stages suitable for use with the TDA7000 are shown in Fig.18 and 19. Figure 20 shows how the muting signal can be used to operate a LED to give an indication of detuning.

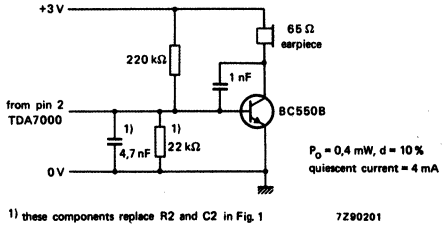

Fig.18 A 0.4 mW transistor audio output stage without volume control for driving an earpiece

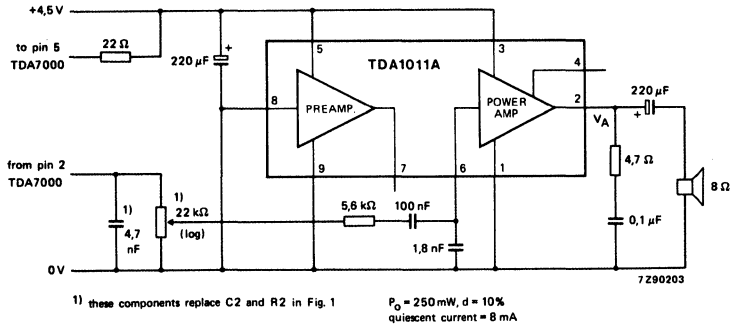

Fig.19 An integrated 250 mW audio output stage

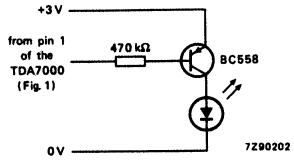

Fig.20 A detuning indicator driven by the mute signal from the TDA7000

ACKNOWLEDGEMENTS

The authors wish to acknowledge the information provided by D. Kasperkovitz and H. v. Rumpt for incorporation in this article.

REFERENCE

KANOW, W. and SIEWERT, I., 'Integrated circuits for hi-fi radios and tuners', Electronic Components and Applications, Vol. 4, No. 1, November 1981, pp. 11 to 27.

9

TDA7000 for Narrow-Band FM Reception AN193

Author: W. V. Dooremolen

INTRODUCTION

Today's cordless telephone sets make use of duplex communication with carrier frequencies of about 1.7MHz and 49MHz.

- In the base unit incoming telephone information is frequency-modulated on a 1.7MHz carrier.
- This 1.7MHz signal is radiated via the AC-mains line of the base unit.
- The remote unit receives this signal via a ferrite bar antenna.
- The remote unit transmits at 49MHz via a telescopic antenna the call-signals and speech-information from the user.
- The base unit receives this 49MHz FM-modulated signal via a telescopic aerial.

A Today's Remote Unit Receiver

In cordless telephone sets which are used today, a normal superheterodyne receiver is used for the 1.7MHz handset. The suppression of the adjacent channel at e.g. 30kHz must be 50db and the bandwidth of the channel must be 6-10kHz for good reception. Therefore an i.f.-frequency of 455kHz is chosen. Since at this frequency there are ceramic filters with a bandwidth of 9kHz (AM-filters), the 1.7MHz is mixed down to 455kHz with an oscillator frequency of 2.155MHz. Now there is an image reception at 2.61MHz. To suppress this image sufficiently, there must be at least two RF filter-sections at the input of the receiver.

The ceramic IF-filter with its subharmonics is bad for far-off-selectivity, so there must be an extra LC-filter added between mixer output and the ceramic filter.

After the selectivity there is a hard-limiter for agc-function and suppression of AM.

Then there is an FM-detector which must be accurate, because it must detect a swing of ±2.5kHz at 455kHz; hence it must be tuned.

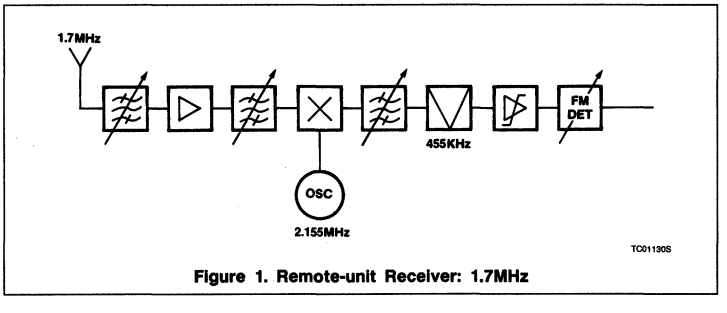

Figure 1. Remote-unit Receiver: 1.7MHz

Figure 1 shows the block diagram which fulfills this principal. The total numbers of alignment points of this receiver is then 5:

2 RF-filter
1 Oscillator
1 IF-filter
1 FM-detector

5 Alignments

A Remote Unit Receiver With TDA7000

The remote unit receiver, see Figure 2, has as main component the IC TDA7000, which contains mixer, oscillator, i.f. amplifiers and demodulator (and squelch functions).

To avoid expensive filtering (and expensive filter-adjustments) in RF, IF and demodulator stages, the TDA7000 mixes the incoming signal to such a low IF-frequency, that filtering can be realized by active RC-filters, of which the active part and the R's are integrated.

To select the incoming frequency, only one tuned circuit is necessary: the oscillator tank circuit. The frequency of this circuit can be set by a crystal.

IMAGE RECEPTION

For today's concept there are a lot of expensive components necessary to suppress the image sufficiently. The suppression of the image is very important because the signal at the image can be much larger than the wanted signal and there is no correlation between the image and the wanted signal.

In a concept with 455kHz i.f. frequency, the 1.7MHz receiver has image reception at 2.155MHz. In the TDA7000 receiver the i.f. frequency is chosen to be at 5kHz. Then the 1.7MHz receiver (with 1.695MHz oscillator frequency) has image reception at 1.69MHz, which is at 10kHz from the required frequency, see Figure 3.

An IF-frequency of 5kHz has been chosen as:

- this frequency is so low, there will be no neighboring-channel reception at the image frequency.
- this frequency is not that low that at maximum deviation (maximum modulation) distortion could occur (folding distortion, caused by the higher order bessel functions)
- this frequency gives the opportunity to obtain the required neighboring-channel-suppression with minimum components in the IF-selectivity.

CIRCUIT DESCRIPTION (see Figure 2)

When a remote unit is at "Power on" in the "Stand-by"-position, it is ready to receive a "Bell-signal". A bell-signal-coming through the telephone line will

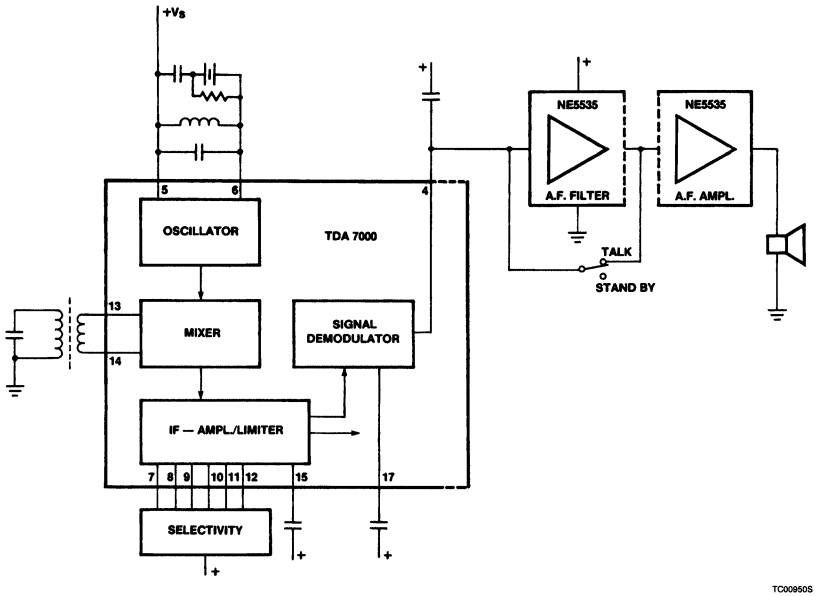

Figure 2

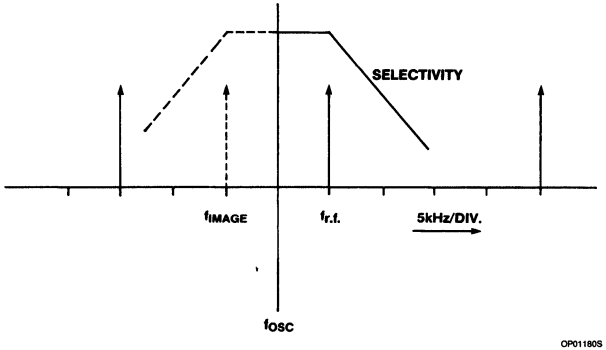

Figure 3

set the base unit in the mode of transmitting a 1.7MHz signal, modulated with e.g. 0.75kHz with ±3kHz deviation.

The ferrite-antenna of the remote unit receives this signal and feeds it to the mixer, where it is converted into a 5kHz IF signal.

Before the RF signal enters the mixer (at pins 13 and 14) it passes RF-selectivity, taking care of good suppression of unwanted signals from e.g. tv- or radiobroadcast frequencies. The IF signal from the mixer output passes IF selectivity (pins 7 to 12) and the IF amplifier/limiter (pin 15), from which the output is supplied to a quadrature demodulator (pin 17). Due to the low IF frequency, cheap capacitors can be used for both IF-selectivity and the phase-shift for the quadrature demodulator.

The A.F.-output of the demodulator (pin 4) is fed to the A.F. filter and A.F. amplifier NE 5535.

The RF Input Circuit

As the image reception is an in-channel problem, solved by the choice of IF-frequency and IF-selectivity, the RF input filter is only required for stopband selectivity (a far-off selectivity to suppress unwanted large signals from e.g. Radio-Broadcast transmitters).

In a remote unit receiver at 1.7MHz, this filter is at the ferrite-rod. Figure 4 shows the bandpass behavior of such a filter at 1.7MHz.

RF-filter at 46MHz: see Appendix

Pre-stage at 46MHz: see Appendix

The Mixer

The mixer conversion gain depends on the level of the oscillator voltage as shown in Figure 5; so the required oscillator voltage at pin 6 is 200mV rms.

The Oscillator

To obtain the required frequency stability in a cordless telephone set, where adjacent channels are at 20 or 30kHz, crystal oscillators are common used.

The crystal oscillator circuits usable for this kind of application always need an LC-tuned resonant circuit to suppress the other modes of the crystal. In this type of oscillator (see as an example Figure 6) the crystal is in the feedback line of the oscillator-amplifier. Integration of such an amplifier should give a 2-pin oscillator.

The TDA 7000 contains a one-pin oscillator. An amplifier with current output develops a voltage across the load impedance.

TDA7000 for Narrow-Band FM Reception

AN193

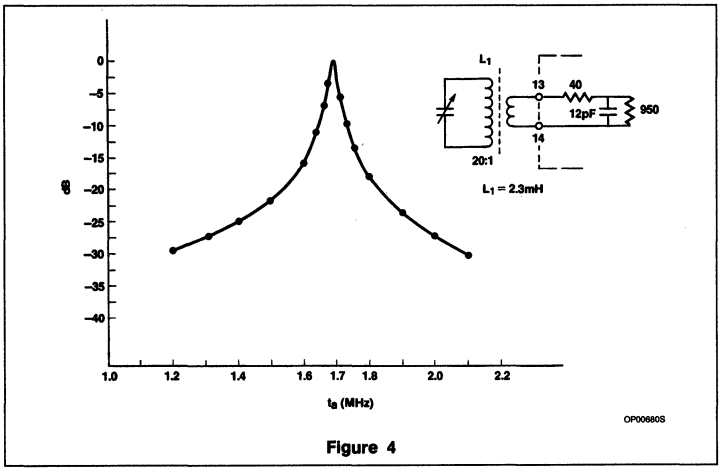

Figure 4

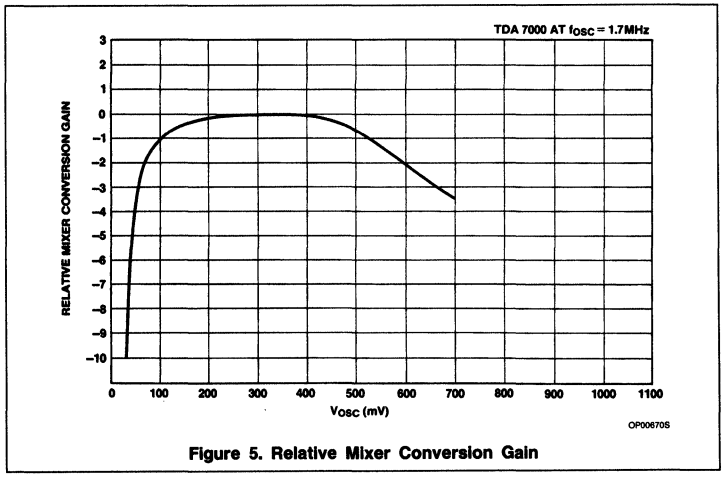

Figure 5. Relative Mixer Conversion Gain

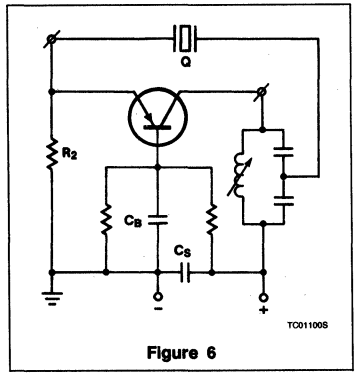

Figure 6

Voltage feedback is internal to the IC.

To obtain a crystal oscillator with the TDA 7000 one-pin concept, a parallel circuit configuration as shown in Figure 7 has to be used.

Explanation of this circuit:

a. Without the parallel resistor Rp.
Figure 8 shows the relevant part of the equivalent circuit. There are three frequencies where the circuit is in resonance (see Figure 9, and the frequency response for "impedance" and "phase", shown in Figure 10). The real part of the highest possible oscillation frequency dominates; and, as there is also a zero crossing of the imaginary part, this highest frequency will be the oscillator frequency. However this frequency $f_{par.}$, is not crystal controlled; it is the LC-oscillation, in which the parasitic capacitance of the crystal contributes.

b. With parallel resistor Rp.
The frequency response (in "amplitude" and "phase") of the oscillator circuit of Figure 7 *with Rp*is given in Figure 11. As the resistor value of Rp is large related to the value of the X-tal series resistance R1 or R3 the influence of Rp at x-tal resonances is negligible. So, at x-tal resonance (see Figure 9b), R3 causes a circuit damping R = 1/w **2. R3. C1**2 + R3 (1 + C2/C1)**2

However at the higher LC-oscillation frequency f_{par} (see Figure 9c), Rp reduces the circuit impedance Ro to (Ro*R damping)/Ro + R damping) = Rc, where Rdamping = 1/w**2. Rp.C1**2 + Rp (1 + C2/C1)**2.

Thus a damping resistor parallel to the crystal (Fig. 7), damps the parasitic LC-oscillation at the highest frequency. (Moreover the imaginary part of the impedance at this frequency shows incorrect zero-crossing).

Taking care that Rp ≫ Rseries, the resistor is too large to have influence on the crystal-resonances. Then with the impedance Rc at the parasitic resonance lower than R at x-tal-resonance, oscillation will only take place at the required x-tal-frequency, where impedance is maximum and phase is correct (In this example at third-overtone resonance).

Remarks:

a. For application in cheap sets, operating at 1.7MHz, the application of an LC-tuned oscillator circuit has been described in appendix 5.3.

b. It is advised to avoid inductive or capacitive coupling of the oscillator tank circuit with the RF-input circuit by careful positioning of the components for these circuits and by avoiding common supply or ground connections.

The IF-amplifier

The Selectivity

Normal selectivity in the TDA7000 is a 4th order low-pass and a 1st order high-pass filter. This selectivity can be split up in a Sallen and Key section (pins 7, 8, 9), a bandpass filter (pins 10, 11) and a 1st order lowpass filter (pin 12).

Some possibilities for obtaining required selectivity are given:

a. In the basic application circuit, Figure 12a, the total filter has a bandwidth of 7kHz and gives a selectivity at 25kHz IF-frequency of 42dB.
In this filter the lower limit of the passband is determined by the value of C4 at pin 11, where C3 at pin 10 determines the upper limit of the bandpass filter section (see Ref. 1).

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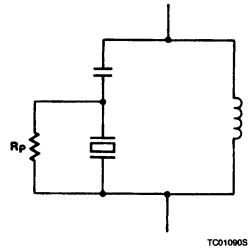

Figure 7

b. To obtain a higher selectivity, there is the possibility to add a coil in series with the capacitor between pins 11 and ground. The so obtained 5th order filter has a selectivity at 25kHz of 57dB, (see Figure 12b).
c. If this selectivity is still too small, there is a possibility to increase the 25kHz selectivity to 65dB by adding a coil in series with the capacitor at pin 11 to ground. In this application, where at 5kHz IF-frequency an adjacent channel at −30kHz will cause a (30−5) = 25kHz interfering IF-frequency, the pole of the last mentioned LC-filter (trap-function) is at 25kHz, (see Figure 12c).

For cordless telephone sets with channels at 15kHz distance, the filter characteristics are optimum as shown in the curves in Figure 13 in which case the filters are dimensioned for 5kHz IF-bandwidth (instead of 7kHz). So for this small channel-distance application the required selectivity is obtained a.o. by reducing the IF-bandwidth; this at the cost of up to 2dB loss in sensitivity. (Note: At 5kHz IF-frequency adjacent channels at ±15kHz give undesired IF-frequencies of 20kHz and 10kHz resp.).

The Limiter/Amplifier

The high gain of the limiter/amplifier provides a.v.c. action and effective suppression of a.m.-modulation. D.C.-feedback of the limiter is decoupled at pin 15.

The Signal-demodulator

The signal-demodulator is a quadrature-demodulator driven by the IF-signal from the limiter and by a phase-shifted IF-signal derived from an all-pass-filter, (see Figure 14).

This filter has a capacitor connected at pin 17, which fixes the IF-frequency, being that frequency where 90 degrees phase shift takes care for the center position in the demodulator output characteristics (see Figure 15, showing the demodulator output (at pin 4) as a function of the frequency, at 1mV input signal).

The A.F. Output Stage

The signal demodulator output is available at pin 4, where a capacitor C serves for elimination of IF-harmonics. This capacitor also influences the audio-frequency response. Appendix 5.4 gives more information about the use of an extra a.f.-output stage. The output from this stage, available at pin 2, has an audio-frequency response as shown in Figure 16, curve a. The output at pin 2 can be muted (see Appendix 5.5).

Output Signal Filtering

Output signal filtering is required to suppress the IF harmonics and interference products of these harmonics with the higher order bessel components of the modulation. Active filtering with operational amplifiers have been used (see Figure 17). The frequency response of such a filter is given in Figure 16, curve b, for an active second order filter with an additional passive RC-filter.

Output Amplification

The dimensioning of the operational amplifier of Fig. 17-a results in no amplification of the a.f. signal. In case amplification of this opamp is required, a feedback resistor and an RC-filter at the reverse input can be added (see Figure 17b, for about 30dB amplification).

MEASUREMENTS

For sensitivity, signal-handling and noise behavior information in a standard application as shown in Figure 18, the signal and noise output as a function of input signal has been measured at 1.7MHz, at 400Hz modulation where the deviation is ±2.5kHz (see Figure 19). As a result the S+N/N ratio is as given in Figure 19, curve 3.

APPENDIX

RF-tuned Input Circuit at 46MHz

In Figure 20 a filter is given which matches at 46MHz a 75 ohm aerial to the input of the TDA7000. Extra suppression of RF-frequencies outside the passband has been obtained by a trapfunction.

RF-Pre-Stage at 46MHz

For better quality receivers at 46MHz an RF-pre-stage can be added, see Figure 21, such to improve the noise figure. Without this transistor a noise figure F = 11dB was found. With a transistor (BFY 90) with RC-coupling at 3mA F = 7dB or at 6mA F = 6dB.

With a transistor stage having an LC-tuned circuit one can obtain F = 7dB at I = 0.3mA. (Note: The noise figure includes image-noise).

An LC-oscillator at 1.7MHz

An LC-oscillator can be designed with or without AFC. If for better stability external AFC is required, one can make use of the d.c.-output of the signal demodulator, which delivers 80mV/kHz at a d.c.-level of 0.65V to +supply. An LC-oscillator as shown in Figure 22a, using a capacitor with a temperature coefficient of −150ppm, gives an oscillator signal of 190mV, with a temperature stability of 1kHz/50 degrees.

With the use of AFC, as shown in Figure 22b, one can further improve the stability, as such AFC reduces the influence of frequency-changes in the transmitter (due to temp. influence or aging). The given circuit gives a factor 2 reduction. Note that the temperature behavior of the AFC-diode has to be compensated. In Figure 22b, with BB405B having a capacitance of 18pF at the reverse voltage V4 = 0.7 Volt, the temp. coefficient of the capacitor C has to be −200ppm.

A.F.-output Possibilities

The a.f.-output from the signal demodulator, available at pin 4, depends on the slope of the demodulator as shown in Figure 15. The TDA7000 A.F. output is also available at pin 2 (see Figure 23). The important difference between the output at pin 2 and the output at pin 4 is that the pin 4 output is amplified and limited before it is led to pin 2 (see Figure 24). Moreover the pin 2 output is controlled by the mute function; a mute which operates in case the received signal is bad as far as noise and distortion is concerned (see chapter 5.5).

The pin 2 output delivers a higher a.f. signal; however the a.f. output spectrum shows more mixing products between i.f.-harmonics and modulation-frequency-harmonics. This is due to the "limited output situation" at pin 2. In narrow band application with relative large deviation these products are so high, that extra a.f. output filtering is required and moreover the if-center frequency has to be higher compared with the concept, using a.f. output at pin 4.

So for those sets where the mute/squelch function of the TDA7000 is not used, and the higher a.f. output is not required, the use of the a.f. output at pin 4 is advised, giving less

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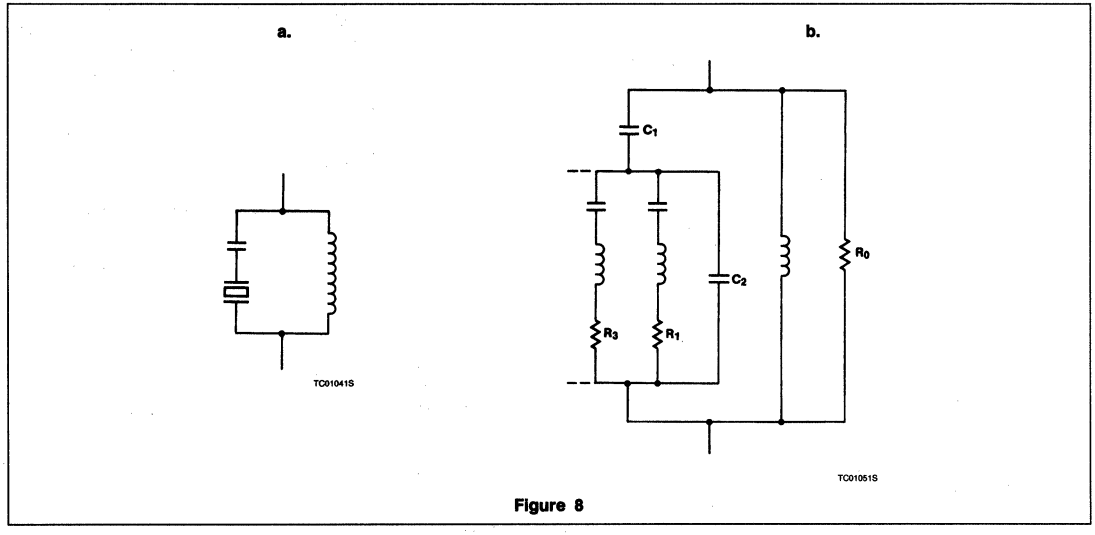


Figure 8

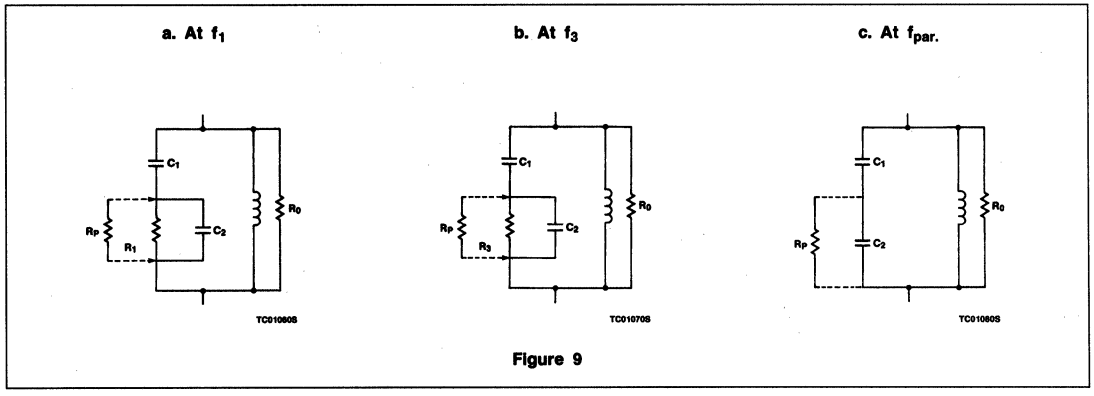


Figure 9

interfering products and simplified a.f.-output filtering.

Squelch And Squelch Indication

The TDA7000 contains a mute function, controlled by a "waveform correlator", based on the exactness of the IF-frequency.

The correlation circuit uses the i.f. frequency and an inverted version of it, which is delayed (phase shifted) by half the period of nominal i.f. The phase shift depends on the value of the capacitor at pin 18 (see Figure 23).

This mute also operates at low field strength-levels, where the noise in the IF-signal means: bad-signal definition. (The correlation between i.f. signal and the inverted phase shifted version is small due to fluctuations caused by noise; see Figure 25). This field strength-dependent mute behavior is shown in Fig. 26, curve 2, measured at full-mute operation. The a.f.-output is not "fast-switched" by the mute function, but there is a "progressive-(soft-muting-) switch". This soft-muting reduces the audio-output signal at low field strength levels, without degradation of the audio output signal under these conditions.

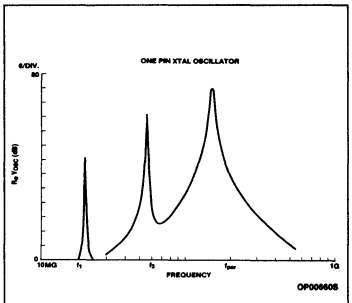
The capacitor C1 at pin 1 (see Figure 23) determines the time constant for the mute action.

Part-operation of the mute is also a possibility (as shown by curve 3, Figure 26) by circuiting a resistor in parallel with the mute capacitor at pin 1.

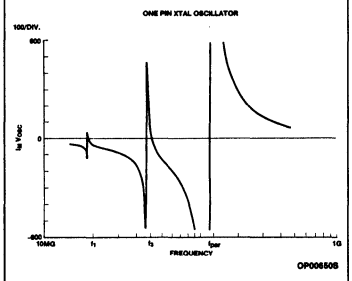
In Figure 26 the small signal behavior with the mute disabled has been given, too (see curve 1).

One can make use of the mute output signal, available at pin 1, to indicate squelch situation by a LED (see Figure 27). Operation of the mute by means of an external d.c.-voltage (see Figure 28) is also possible.

TDA7000 for Narrow-Band FM Reception AN193



a. One Pin XTAL Oscillator



b. One Pin XTAL Oscillator

Figure 10

Bell-signal Operation

To avoid tone decoder filters and tone decoder rectifiers for Bell-signal transmission, use can be made of the mute information in the TDA7000 to obtain a bell-signal without the transmission of a bell-pilot-signal.

With a handset receiver as shown in Figure 23 in the "Stand-by" position, the high mute output level keeps via transistor T1 amplifier 1 out of operation. This situation remains until a correct IF-frequency is obtained. This situation appears at the moment that a Bell-signal switches the base-unit in transmission mode.

If the transmitted field strength is high enough to be received above a certain noise level, the mute level output goes down; T1 will be closed and the amplifier 1 starts operating. However due to feedback this amplifier starts oscillating at a low frequency (a frequency, dependent on the filter concept). This low-frequent signal serves for bell-signal information at the loudspeaker.

Switching the handset to "Talk"-position will stop the oscillation. Then the amplifier 1 serves to amplify normal speech information.

Mute at Dialing

During dial-operation the key-pulser IC delivers a mute voltage. This voltage can be used to mute the A.F.-amplifier e.g. via T1 of the bell-signal circuit/amplifier (see Figure 23).

CONCLUSIONS

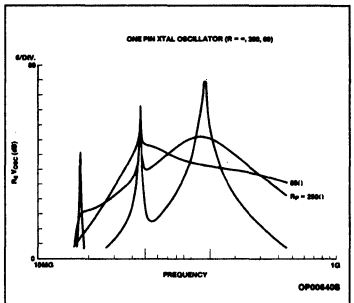
The application of the TDA7000 in the remote unit (hand set) as narrow band FM-receiver is very attractive, as the TDA7000 reduces assembly and post-production alignment costs. The only tunable circuit is the oscillator circuit, which can be a simple x-tal controlled tank circuit.

A TDA7000 with:
- 5th order i.f. filter
- 3rd order a.f. output filter
- matched input circuit
- crystal-oscillator tank circuit
- disabled mute circuit

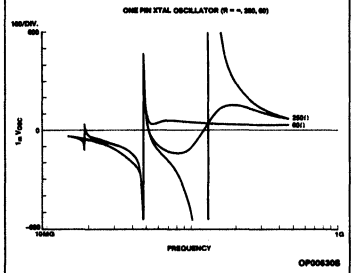
gives in cordless telephone application at 1.7MHz a sensitivity of 2.5μV for 20dB signal to noise ratio, at adjacent channel selectivity of 40dB (at 15kHz).

The TDA7000 circuit is:
- without an R.F. pre-stage
- without R.F. tuned circuits
- without oscillator transistor (and its components)
- without LC or ceramic filters in I.F. and demodulator.

For improved performance the TDA7000 circuit can be expanded



a. One Pin XTAL Oscillator (R = ∞, 250, 60)



b. One Pin XTAL Oscillator (R = ∞, 250, 60)

Figure 11

- with an R.F. pre-stage and R.F. selectivity
- with higher order I.F. filtering
- with mute/squelch function

For reduced performance the TDA7000 circuit can be simplified
- to LC tuned oscillator
- to lower-order I.F. filter
- to Bell-signal operation without pilot transmission.

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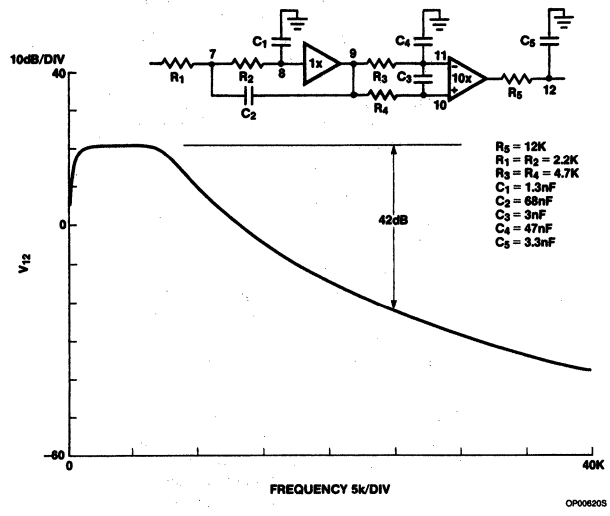
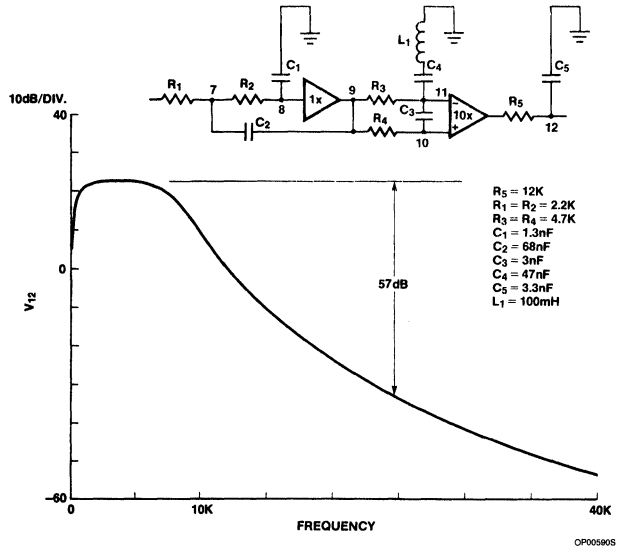

10dB/DIV
40
0
-60
0
40K
FREQUENCY 5k/DIV
V_{12}
C_1
C_2
C_3
C_4
C_5
R_1
R_2
R_3
R_4
R_5
1x
10x
7
8
9
10
11
12
42dB
R_5 = 12K
R_1 = R_2 = 2.2K
R_3 = R_4 = 4.7K
C_1 = 1.3nF
C_2 = 68nF
C_3 = 3nF
C_4 = 47nF
C_5 = 3.3nF
OP00620S

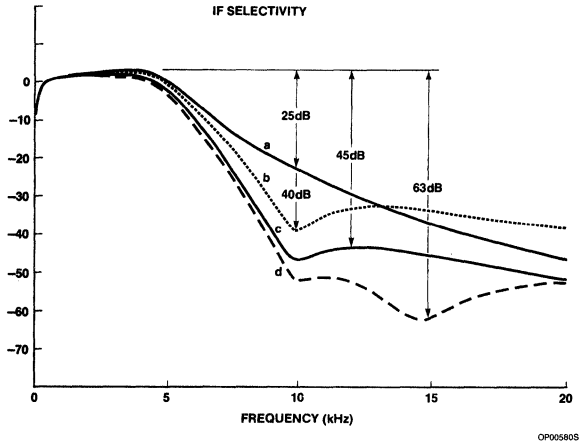
a.

Figure 12



b.

Figure 12



c.

Figure 12

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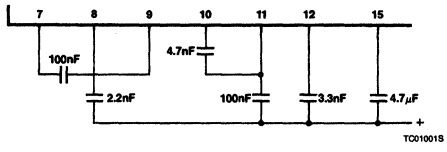
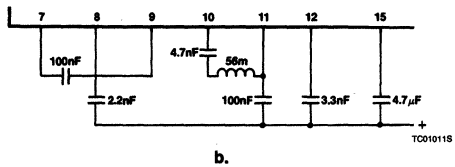
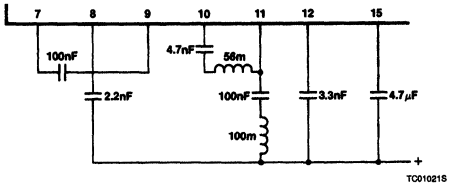
TDA7000 for Narrow-Band FM Reception AN193



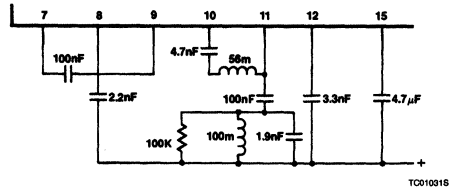
a.



b.

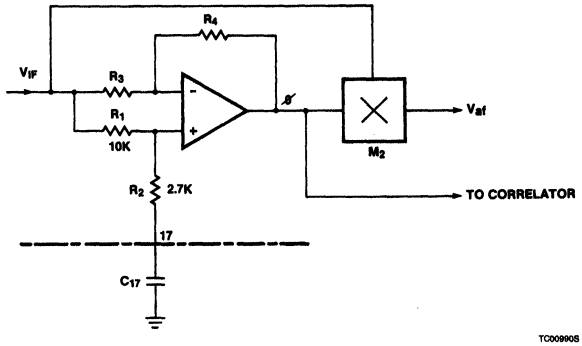


c.



d.

Figure 13



With $R_2 = 0$.

$\phi = -2 \tan_1 wR_1C_{17}$

for $\phi = -90°C$, $C_{17} = \frac{1}{wR1\sqrt{\frac{R_4}{R_3}}} = 4.1nF$ for $f_{if} = 5kHz$.

To improve the performance of the all-pass filter with the amplitude limited i.f. waveform, R_2 has been added. Since this influences the phase angle, the value of C_{17} must be increased by 13% i.e. to 4.7nF.

Figure 14. F.M. Demodulator Phase Shift Circuit (All-pass Filter)

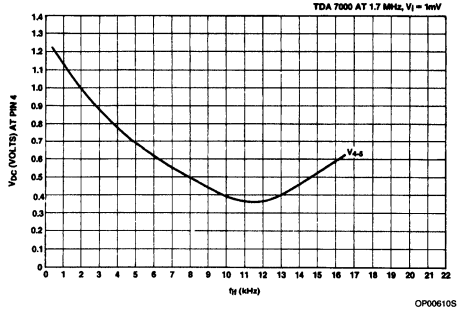


Figure 15

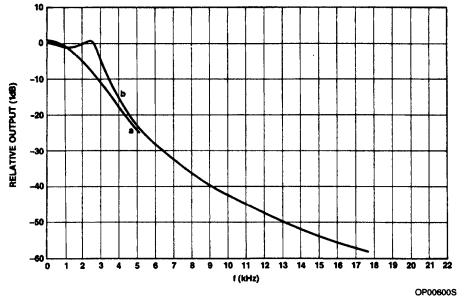


Figure 16

9

TDA7000 for Narrow-Band FM Reception AN193

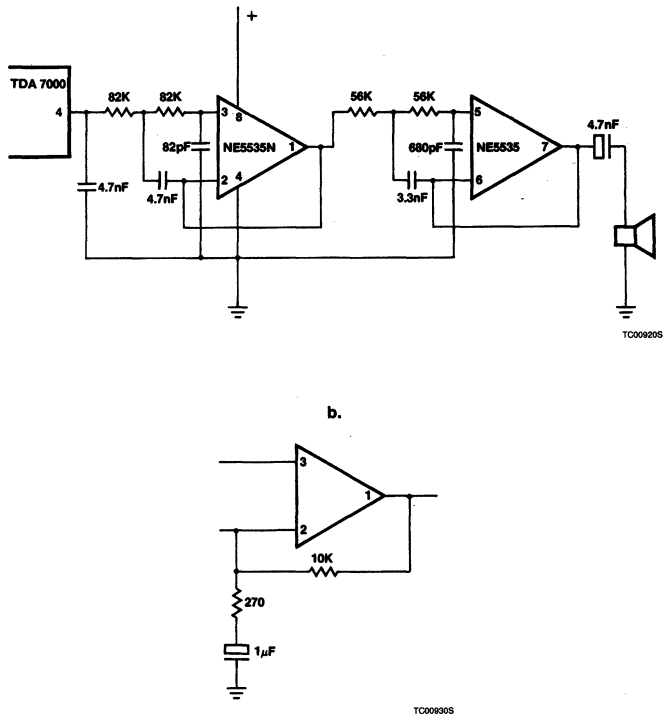


Figure 17

TDA7000 for Narrow-Band FM Reception AN193

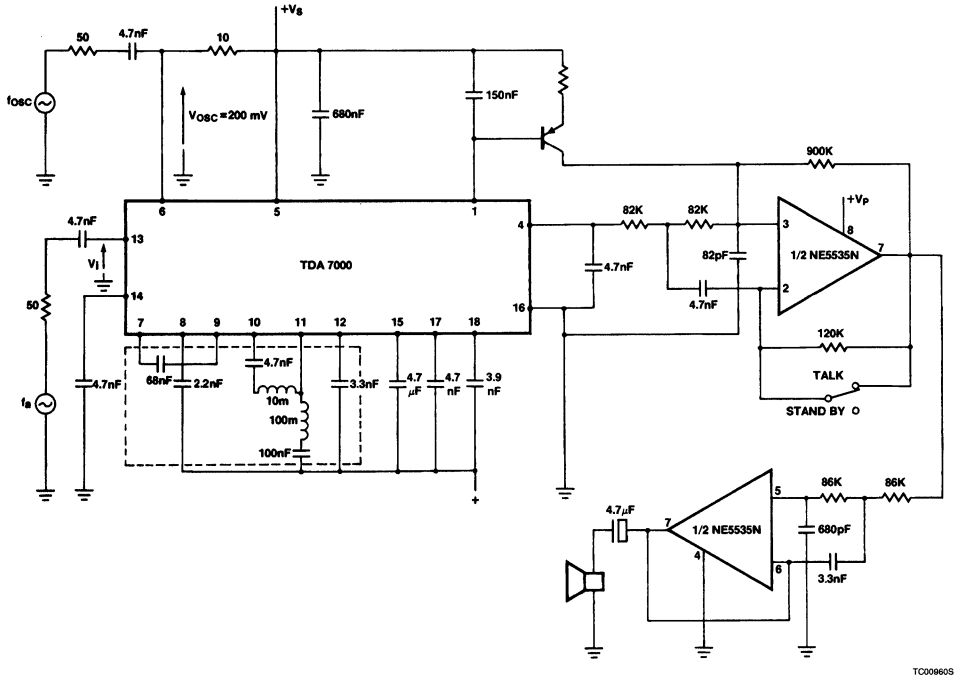


Figure 18

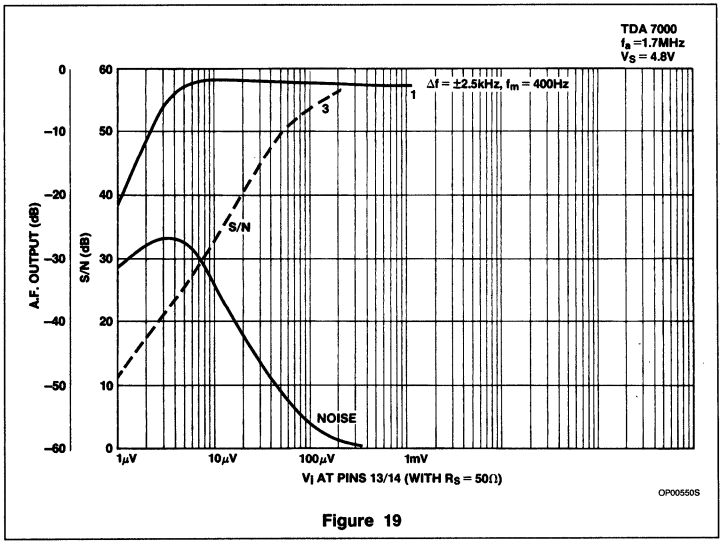


Figure 19

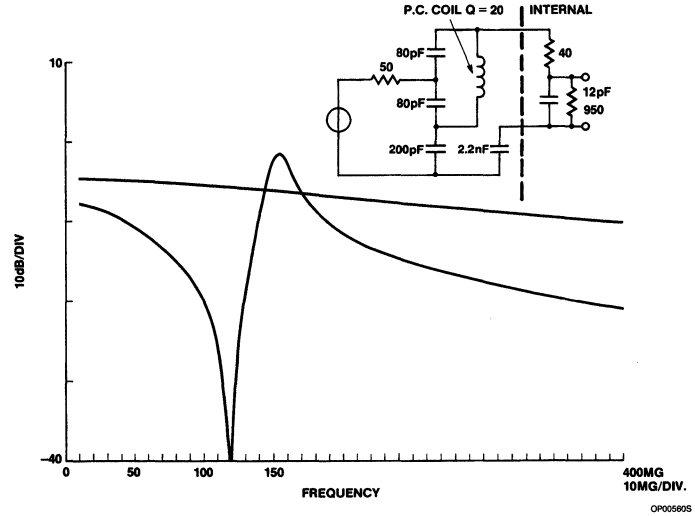


Figure 20

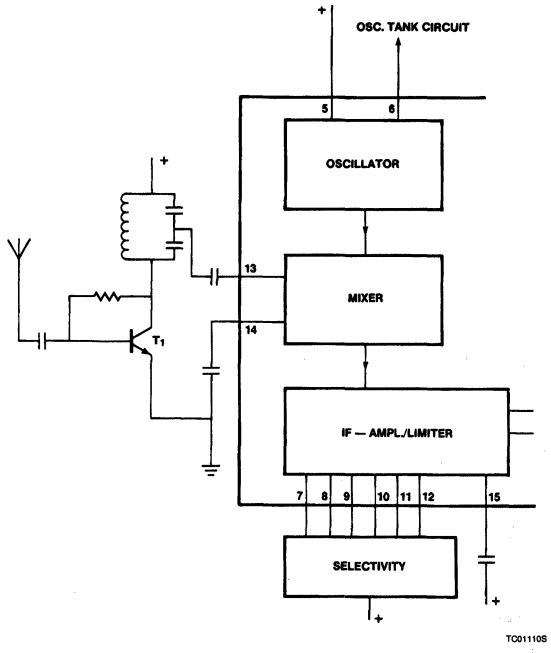
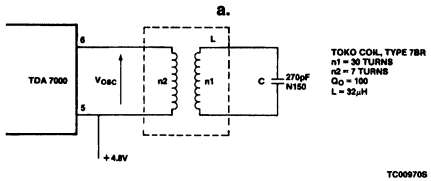


Figure 21

TDA7000 for Narrow-Band FM Reception AN193



Toko coil, type 7BR
n1 = 30 turns
n2 = 7 turns
Q_O = 100
L = 32μH

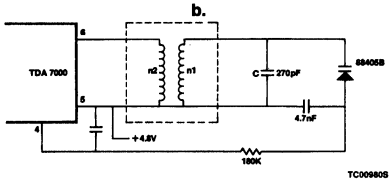


Figure 22

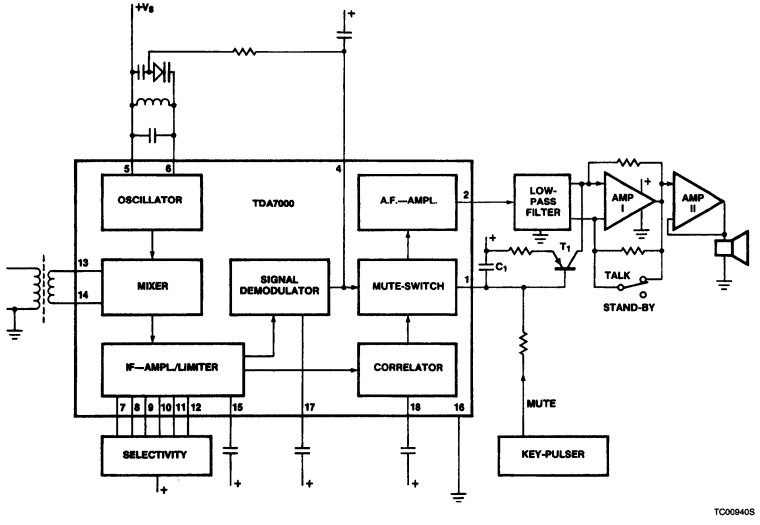


Figure 23. Remote-unit Receiver: 1.7MHz

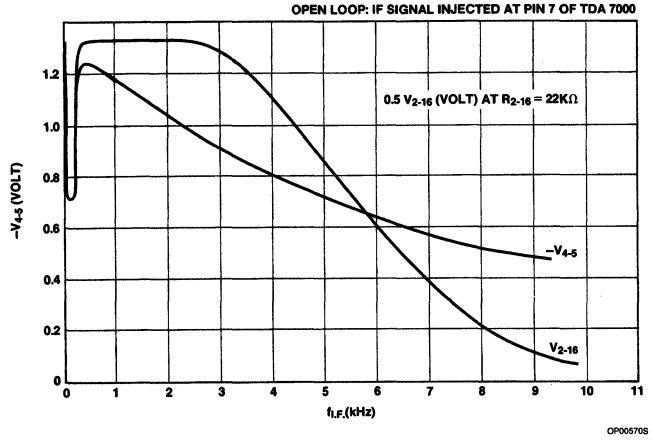


Figure 24. Demodulator Characteristics

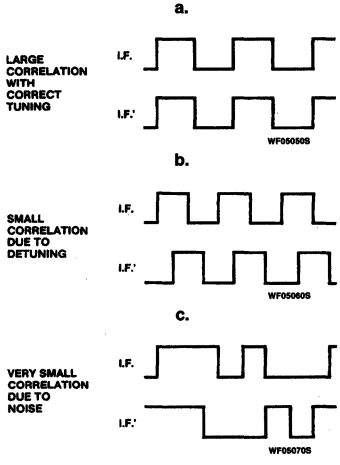


Figure 25. Function Of The Correlation Muting System

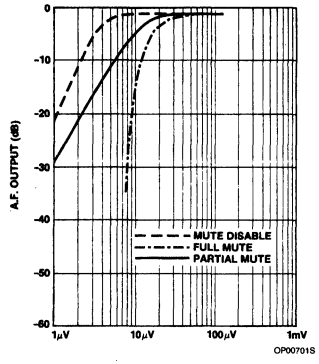


Figure 26

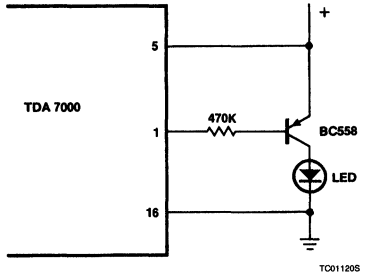


Figure 27

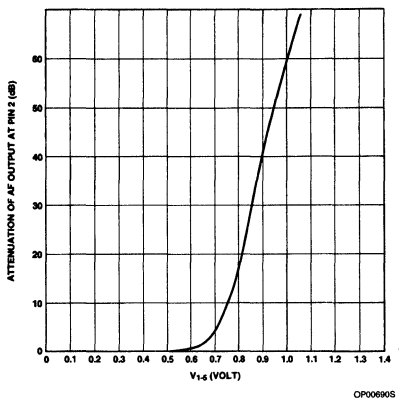


Figure 28

9

Circuit Description of the Infra Red Receiver TDA3047/TDA3048 AN172

Author: A.J.E. Bretveld

INTRODUCTION

As a successor of the current integrated circuits TCA440 and NE555 for receiving infra red remote controlled signals a new integrated circuit has been developed.

In comparison with the TCA440-NE555 combination this IC is aimed to have a higher replacement value and improved performance. The TDA3048 is equal to the TDA3047 except for the polarity of the output signal.

GENERAL DESIGN CONSIDERATIONS

The target of this development is to make a receiver integrated circuit for infra red remote controlled signals which functions optimally in a narrow band application.

This integrated circuit shall have the following advantages in comparison with the present TCA440-NE555 combination:

- A higher replacement value
- A considerable saving of the current consumption
- An improvement of the specification (less spread)
- Less periphery and no adjustment points
- Total spread on pulse widening < 10% by a standard RC-5 signal.

Besides the IC is also suitable to be used in a RC-5 extended receiver and in a wide band receiver.

A standard bipolar process with single layer interconnect and without collector wall has been used.

Due to the low currents a collector wall is not necessary.

FUNCTIONAL DESCRIPTION OF THE BLOCK PARTS

Block diagram.

Figure 1 shows the block diagram of the TDA3047 and TDA3048.

Amplifier

The input signal is amplified by the gain-controlled amplifier. The output signal of the amplifier is fed to the synchronous demodulator inputs and to the reference amplifier.

Reference Amplifier

The reference amplifier amplifies and limits the input signal. The output signal of this amplifier is fed to the synchronous demodulator.

Synchronous Demodulator

In the synchronous demodulator the input signal and reference signal are multiplied. The output signal of the demodulator is fed to the input of a pulse-shaper circuit and to the input of the AGC circuit.

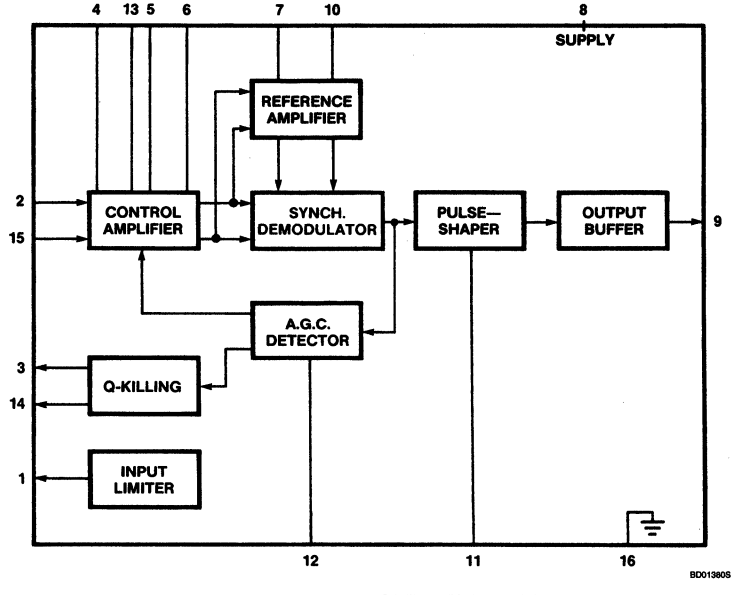


Figure 1. Block Diagram Of The TDA 3047/3048

Circuit Description of the Infra Red Receiver TDA3047/TDA3048 AN172

FUNCTIONAL DESCRIPTION (Continued)

AGC Circuit

The output signal of the synchronous demodulator is fed to the AGC circuit. The top level of the signal is detected by the AGC detector. Noise pulses are integrated by an internal capacitor. The output signal from the AGC detector is amplified and supplied to the first and second stage of the amplifier and to the Q killing circuit.

Pulse-shaper Circuit

The output of the synchronous demodulator is also fed to the pulse-shaper circuit. The slicing level of the pulse-shaper is lower than the slicing level of the AGC detector.

The output of the pulse-shaper is fed to the output buffer.

Output Buffer

The output buffer gives for the TDA3047 an active high level and for the TDA3048 an active low level on the output pin. To obtain a correct RC-5 code a hysteresis circuit protects the output against spikes.

Q Killing Circuit

In the narrow band application it is necessary to degenerate the Q of the input selectivity particularly when large signals occur at the input.

The output of the Q killing circuit can be directly coupled to the input.

Input Voltage Limiter

In the narrow band application high voltage peaks can occur on the input selectivity. The input limiter limits these voltage peaks to about 0.7 Volts.

APPLICATION

The narrow band application diagram has been given in Figure 2 and a lower performance wide band application diagram in Figure 3.

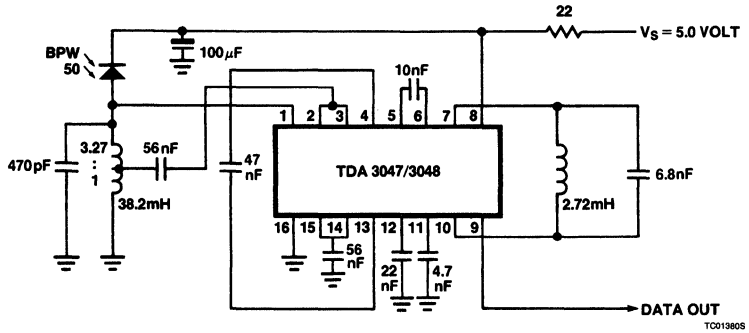


Figure 2. Narrow Band Application Diagram Of The TDA 3047/3048

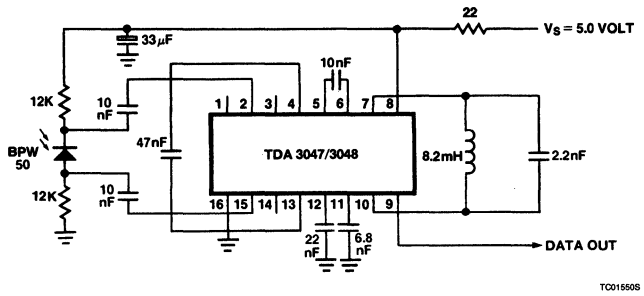


Figure 3. Wide Band Application Diagram Of The TDA 3047/3048

Low Power Pre-Amplifiers for IR Remote Control Systems AN173

INTRODUCTION

The monolithic integrated bipolar circuits TDA3047 and TDA3048 are amplifiers intended for use in infra-red remote control systems. Both circuits are excellent and applicable as narrow band amplifiers, especially for those types of remote control concepts which use the modulated transmission technique. Under certain conditions both IC's are also applicable as broadband amplifiers. The only difference between the IC's is polarity of the output signal. This type of IR amplifier offers the following advantages:

- Low power consumption, typically 10.5mV
- Gain controlled amplification, control range 66dB
- High amplification factor, > 80dB, ensures a long range
- Great stability in signal handling
- Demodulation via a synchronous demodulator
- Automatic limitation of large input signals, 600mV
- Independent of large input amplitude variations with a Q-killer
- Applicable as narrow or broadband amplifier

This circuit proves to be a reliable device with regard to interference from other IR sources such as light bulbs, etc.

The automatic gain control (A.G.C.) ensures very good stability in amplification of large or low input signals, which correspond to short or long distances from transmitter to receiver.

FUNCTIONAL DESCRIPTION

The functional block diagram is shown in Figure 1. The input signal is applied to the gain controlled multi-stage differential pre-amplifier, capacitively coupled via C_2 and C_3. The capacitors C_4 and C_5 stabilize the differential pre-amplifier. Hereafter the signal is fed to a synchronous demodulator and the reference amplifier, which limits the input signal. After multiplication of the input and reference signal by the demodulator, the signal is applied to a pulse shaper, whose time constant is controlled by C_8. The same signal is also used for the feed back loop, resulting in an automatic gain control defined by the amplitude of the input signal. The A.G.C. acquisition time is set by C_7. The Q-killer limits the amplification of the tuned input circuit in conjunction with input amplitude. In this way the behavior of this device on large amplitude variations ensures a great stability in the signal handling. A maximum input limitation is achieved via the amplitude limiter, typically activated by a 600mV input signal.

The differential pre-amplifier has in principle two stages, as shown in Figure 2. Each stage is stabilized via an external feedback capacitor. Both define the lower boundary of the frequency, with the greatest influence from C_4 because stage 1 has the highest gain. Both capacitors should be specified so that interference from low frequencies is suppressed. For instance, bulbs radiate infra-red frequencies at (n)(100Hz).

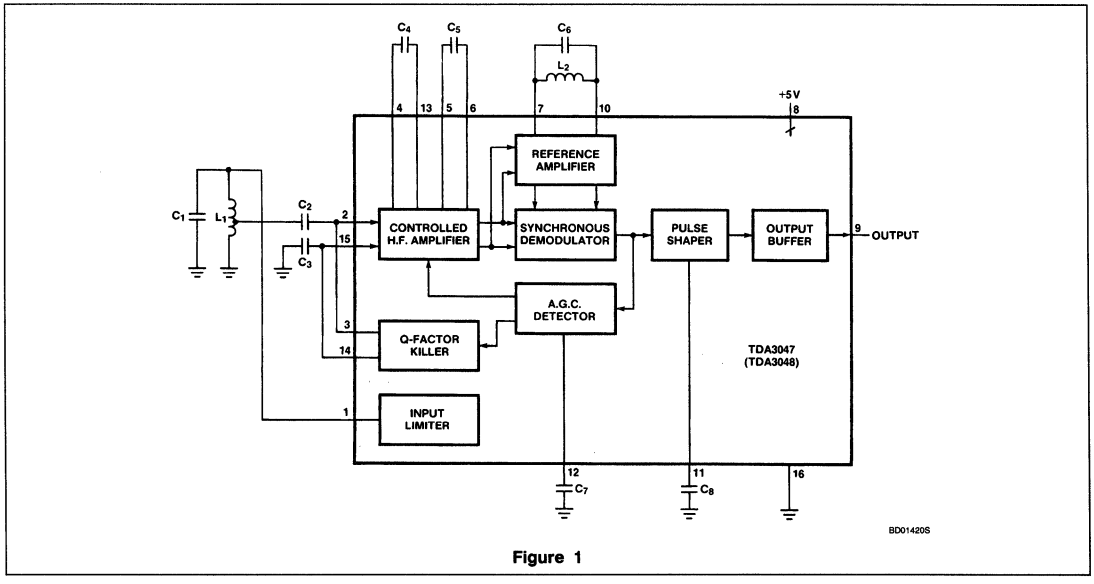


Figure 1

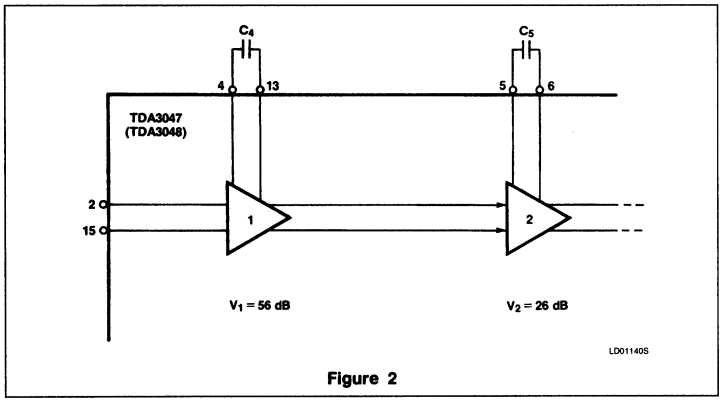


Figure 2

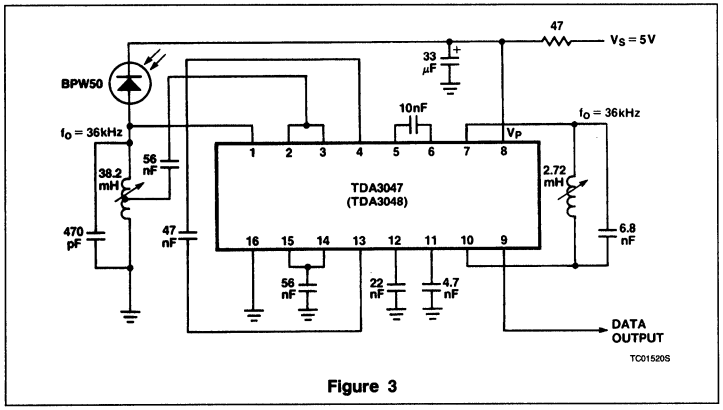


Figure 3

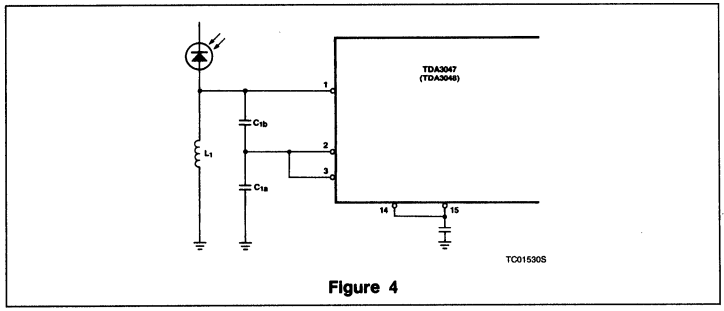


Figure 4

The highest boundary in frequency of this amplifier is greater than 1MHz and is given by the internal capacitance of this device.

IR AMPLIFIER

For remote control systems two different types of amplifiers are available. Both are described in the following sections.

Narrow Band Amplifier

The diagram of Figure 3 shows the TDA3047/48 in such an application. Pin 15, one of the differential inputs, is grounded for AC, while the second input, pin 2, is connected to the tuned input circuit via a capacitor of 0.056µF. The input voltage is taken with a transformer ratio N = 1:3. Direct coupling to the top will only lower the quality Q factor of the tuned input circuit, due to the relatively low input resistor R_{IN} of the IC.

The selectivity is obtained with the tuned input circuit and strongly reduces IR interferences. The effect of direct IR radiation is also avoided. Due to the low-ohmic resistance of the coil, the IR-receiving diode will never become saturated. The center frequency of the input tank must be equal to the modulation frequency of the transmitter used.

For this frequency (f_o) the input tank has a high impedance. Small variations of the current of the IR receiving diode at (f_o) result directly in large input signals.

This frequency (f_o) is equal to 37.5kHZ for the SAA3004 transmitting chip. The R.C. combination of 47 ohms and .33µF suppresses the unwanted current variations caused by the supply line.

The Q of the tuned input circuit is practically defined by the transformer ratio and the input resistor R_{IN} of the IC. The effect of R_{IN} to the quality Q_1 of the coil is negligible, because R_{IN} is relatively low (typically 16K ohms).

The transformer ratio must be adjusted for small signals, so that the range is hardly influenced by component spread and/or tolerances in frequency at both sides in the system. The Q can be calculated from

$$Q = \frac{1}{R_{L1}\sqrt{\frac{C_1}{L_1}} + \frac{1}{R_P}\sqrt{\frac{L_1}{C_1}}}$$

where R_{L1} is the ohmic resistance of the coil and the parallel resistor $R_p = n^2 R_{IN1}$.

With the component values shown in Figure 4 and a given R_{L1} = 125 ohms, R_{IN} = 16K ohms, the factor Q is calculated as Q = 13. The bandwidth is now known from

$$\Delta f = \frac{f_o}{Q} = 2.9\text{kHz}$$

The transformer ratio can also be realized with two capacitors in series, as shown in Figure 4, where the total capacity is equal to the required one.

The ratio is $n = \frac{C_{1a} + C_{1b}}{C_{1b}}$

With values of: C_{1a} = 2.2nF, C_{1b} = 560pF and L_1 = 40mH, about the same input quality will be obtained.

The A.G.C. acquisition time and the time constant of the pulse shaper are defined by the capacitors C_7 and C_8 respectively. The time constant at pin 12 equals the length of a received data bit and C_8 delays the pulse shaper output to the output stage.

The Q_s of the tuned circuit of the synchronous demodulator is practically given by the

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Low Power Pre-amplifiers for IR Remote Control Systems AN173

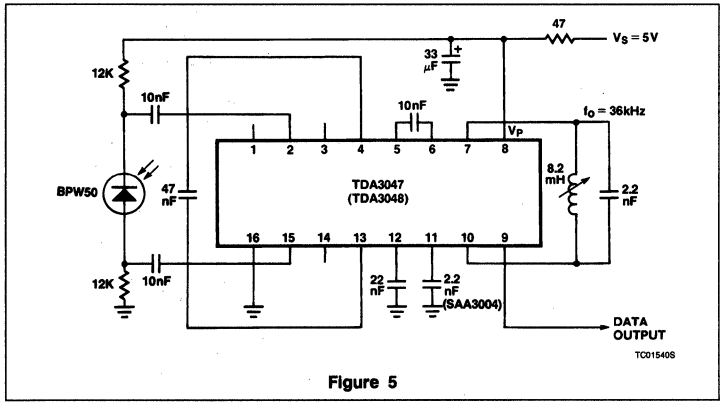

Figure 5

internal resistance R_{IN2} between the pins 7 and 10 and is calculated from

$$Q_s = \frac{1}{R_{L2}\sqrt{\frac{C_6}{L_2}} + \frac{1}{R_{In2}}\sqrt{\frac{L_2}{C_6}}}$$

with 12 ohms for RL_2 and 5K ohms for R_{IN}, $Q_s \simeq 7$. The quality Q_s is continuously limited. With a relatively high value for Q_s, the acquisition time will be increased and this will delay the pulse edges. By amplification of "biphase" modulated signals, disturbances could occur in the decoding. For correct decoding of "biphase" coded data, a nearly exact position of the pulse edges is required.

Broadband Amplifier

The application as broadband amplifier is shown in Figure 5. The IR-receiving diode is now positioned between both differential inputs, while the series resistors of 12K ohms are the work resistors. The Q-killer and Amplitude Limiter do not have any function here and are not used. Also the resonance frequency (f_o) of the tuned demodulator circuit equals the modulation frequency of the remote transmitter.

The charge current to capacitor C_8 equals to

$$I_{C8} = (C_8)\frac{\Delta V_{C8}}{\Delta t}$$

where Δt is the charge time and ΔVC_8 is the voltage increment. IC_8 is generated by an internal current source.

The voltage increment at C_8 is proportional to Δt, with IC_8 constant and expressed as

$$\Delta V_{C8} = \frac{(I_{C8})(\Delta t)}{C_8}$$

The pulse width Δt of the demodulated signal must be large enough that VC_8 exceeds the threshold voltage of the pulse shaper.

Given the format of the received data, C_8 will have different values

	Pulse Width	C_8
SAA3004	8.8µsec	2.2nF

A 2.2nF capacitor in the SAA3004 remote control system is an optimum one.

The SAA3004 used in unmodulated mode has a pulse width of 8.8µsec. C_8 must have a low value so that the threshold voltage of the pulse shaper is exceeded. On the other hand, if C_8 becomes too small, interference pulses will easily trigger the pulse shaper. The selection of C_8 is a compromise between the sensitivity of the amplifier and the immunity against interference. Such a compromise is a 2.2nF capacitor for the unmodulated mode of the SAA3004, including the tolerances of the internal current sources. Given the technology, small tolerances are not possible.

Correct operation can not be guaranteed for the combination of a small pulse width (8.8µsec.) and a low source current. However, practical tests did show that correct operation of the SAA3004, in the unmodulated mode in combination with this type of preamplifier, can be realized.

CONSIDERATIONS FOR AMPLIFIER SELECTION

The narrow or broadband application is defined by the following points:

- Modulation mode of the transmitter
- Requirements for the reach in distance
- Reliability (insensitivity to interference)
- Price-attractive total remote control system

Either modulated or unmodulated data transmission is possible with the SAA3004.

In the unmodulated mode of the SAA3004, the logic representation of the data word is defined by the time intervals between the generated output pulses, each of 8.8µsec width. In the modulated output mode each active output stage has a burst of 6 clock periods.

The ground wave of this output, with a frequency of 38kHZ, contains the IR power generated.

The greatest sensitivity is realized with a narrow band amplifier, whose tuned input circuit is selected for this ground wave frequency.

In the unmodulated transmission mode, the single output pulse represents a continuous frequency spectrum, in which the generated IR power is divided. A broadband amplifier is then required.

The greatest range, with constant current through the IR transmission diode(s), will be obtained with a narrow band amplifier, because the signal-to-noise ratio is the largest value.

When IR interference is absent, the combination of modulated transmission mode and the narrow band amplifier is the most preferable. With lower requirements for the reliability, less range etc., the broadband amplifier is the most effective solution for both types of modulation modes.

RANGE

To give some idea what range can be expected, a number of measurements are made with the remote transmitters SAA3004.

With Various IR Output Powers

Transmitter SAA3004 drives 1 IR-transmitting diode with a peak current IC≅2A. In the modulated mode, the power product per bit equals

(m) (I_F) (n) (t_p)

where m = number of diodes, n = number of pulses per bit, and t_p = pulse width.

The power product for each bit is:

- Modulated mode (m) (I_F) (n) (t_p) = (1) (2) (6) (8.8) = 106=mµA sec
- Unmodulated mode (m) (I_F) (n) (t_p) = (1) (2) (1) (8.8) = 18=mµA sec

This power product is proportional to the generated IR power. Table 1 indicates the results of the measurements. Optic lenses will increase the distances about 10%.

With Equal Output Power

These measurements are done with one transmitting diode for each transmitter type and the power product/bit constant at 18=mµA sec. Table 2 is comprised of the results from these measurements.

Table 1. Distance Reach with Various Power Products

	SAA3004	
	Modulated	**Unmodulated**
Power product	106μA sec.	18μA sec.
Narrow band C_8 = 4.7nF	25mt	11mt
Broad band C_8 = 2.2nF	16mt	12mt

Table 2. Distance Reach with Constant Power Product of 18μA sec.

	SAA3004	
	Modulated	**Unmodulated**
Narrow band C_8 = 4.7nF	11mt	11mt
Broad band C_8 = 2.2nF	8mt	12mt

Table 3. Application Possibilities

	SAA3004	
	Unmodulated	**Modulated**
Narrow band	No sense; no selectivity	Great distance reach, high selectivity, reliable
Broad band	Function only possible with small width output pulse; less reliable	Low reach, low selectivity; interference.

Results of the Measurements

The results of the measurements can be summarized as follows:

a. Only the combinations "modulated and narrowband amplifier" are reasonable.

b. With the peak current I_F through one IR-transmitting diode, the range with one IR diode is limited.

c. A maximum range is obtained using the modulated mode of data transmitting, but the loss of power in the transmitter is of subordinate importance.

POWER DISSIPATION

In comparison with older types of pre-amplifiers, the power consumption is enormously reduced. For instance, the TDB2033 consumed 204mW at 12 volt supply, while the TDA3047/48 only takes 10mW at 5 volt supply, which is very useful for "stand by" mode. A second advantage is the 5 volt supply which can also be used by the decoding microcomputer.

POSSIBLE APPLICATION COMBINATIONS

In Table 3 the different combinations are given for remote control systems operating in the modulated or unmodulated mode.

OUTPUT SIGNAL

As indicated in the introduction, the TDA3047 has an active "high" output signal, while an active "low" output is generated by the TDA3048. This choice in polarity is made available for maximum cooperation with the decoding part. If, for example, an 8048 microcomputer is used on interrupt level, with active "low" at input $\overline{INT}$, the TDA3048 is then the correct amplifier. If the $\overline{INT}$ input is active "High", the TDA3047 outputs the proper "High" level.

PC-BOARD DESIGN

Special attention must be given to the placement of C_5. The greatest distance must be realized between the position of this capacitor and the inputs 2 and/or 15. Ground connections and screening must also be done with great accuracy.

TEA1042: Use in Loudspeaking Phone AN194

Author: J.A.C.M. van Tiggelen

SUMMARY

The TEA1042 is a dedicated transmission circuit designed for use in loudspeaking telephone sets. Besides the normal lowspeaking functions (transducers in the handset) it also contains amplifiers for a microphone and a loudspeaker in the base. A logical input is provided to select between lowspeaking and loudspeaking. However to make full handsfree operation possible some additional circuitry has to be applied, i.e. two voice-switches and a duplex controller in order to avoid howling of the telephone set, a microphone preamplifier and a power amplifier for the loudspeaker. This report gives a design example for this additional circuitry using off-the-shelf components. It has been designed for a low supply voltage and a low supply current consumption. Therefore the circuitry can be powered from the telephone line. This has been realized using an electronic inductor which fulfills all balance-return-loss demands.

INTRODUCTION

The TEA1042 is a transmission circuit designed for use in loudspeaking telephone sets. Besides the normal functions (supplied from telephone line current, adjustable voltage regulator, high and low-impedance handset microphone inputs, muting input, gain setting facility and a line current dependent gain control facility) it contains amplifiers for the base microphone and the base loudspeaker and switches to select between lowspeaking and loudspeaking. However, to make full handsfree operation possible, some additional equipment has to be used.

Because of the much greater distance the sound of the talker has to bridge (typ. 50cm between mouth/ears of the user and the microphone/loudspeaker of the telephone set instead of typ. 2.5cm when a handset is used) a microphone preamplifier and a loudspeaker power amplifier are necessary.

FUNCTIONAL DESCRIPTION

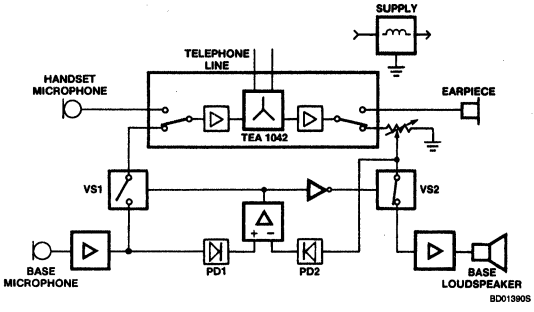

Figure 1. Block Diagram Of The Loudspeaking Telephone Set

As a result of introducing this extra gain, stable operation of the telephone set cannot be ensured under all circumstances. The gain of the loop consisting of microphone amplifiers, hybrid network, receiving amplifiers and the acoustic coupling between loudspeaker and microphone then can exceed unity which will cause 'howling' of the telephone set. Therefore it is necessary to insert a loss in this loop to ensure the loop gain not to exceed unity. Since this loss will attenuate voice signals, too, it is necessary to insert it at any moment in the channel in which no voice signals (or in practice: less voice signals) are present. Therefore a duplex controller has to be inserted with the task to control in which channel the loss has to be inserted.

This report gives a design example for this additional circuitry using standard components.

In Figure 1 a block diagram of the loudspeaking telephone set is shown. As a base microphone an electret type is preferable because of its small dimensions and its high sensitivity. The signals of this microphone are amplified and then go to the transmission circuit TEA1042 via voice-switch VS1. The preamplified signals are also fed to the duplex controller.

The signals received from the transmission circuit TEA1042 go to the loudspeaker amplifier and the loudspeaker via voice-switch VS2 and a volume regulator. The signals are also input for the duplex controller.

The duplex controller consists of two peak value detectors, PD1 and PD2, which rectify the microphone and telephone signals respectively. The peak values are compared in a comparator. The voice-switch in the channel with the stronger signals is closed by the comparator.

The duplex controller and the microphone amplifier have been built using an LM324 quadruple operational amplifier. For the loudspeaker amplifier a TDA7050 has been used. The voice-switches have been made using BC547 transistors. The circuit is powered from the telephone line using an operational amplifier of the type TCA520 as an electronic inductor.

MICROPHONE PREAMPLIFIER

The transmission circuit TEA1042 provides a gain for base microphone signals of typ. 20dB. In practice a much higher value is needed. Therefore a microphone preamplifier is necessary. This has to be a low-noise amplifier which must have a constant gain over the full supply voltage range of 3 to 6V. Therefore it has been realized using a BC549 as a low-noise preamplifier and one of

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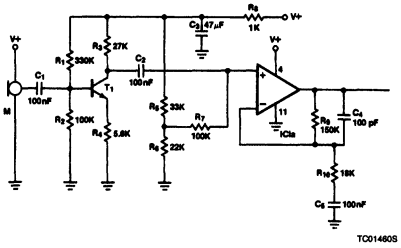

Figure 2. Circuit Diagram Of The Microphone Preamplifier

the four op amps of the LM324. The schematic diagram is shown in Figure 2.

The gain of this amplifier is 30dB (11dB in the preamplifier; 19dB in the LM324 amplifier). The capacitors C_4 and C_5 have been included in order to reject out-of-band signals.

The low pass filter consisting of R_8 and C_3 is necessary to avoid unwanted amplification of supply voltage variations.

LOUDSPEAKER AMPLIFIER

The transmission circuit TEA1042 contains a loudspeaker preamplifier which drives in this design a TDA7050 dual power amplifier. This results in a very simple circuit requiring few external components (see Figure 3). The TDA7050 provides a fixed gain of 26dB in this single-ended configuration which is preferred to the bridge-tied-load configuration from the view of supply current consumption in this application. The second amplifier in the TDA7050 might be used as a preamplifier in case the 26dB gain turns out to be too low. A volume regulator has been included making it possible for the user to adjust the volume to the required acoustic level.

The filter in the supply line (R_{11} and C_7) has been included in order to protect the rest of the circuitry for excessive supply voltage drops caused by the TDA7050 when it is driven to full power.

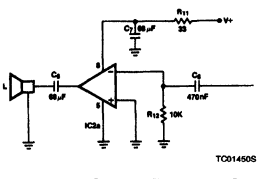

Figure 3. Circuit Diagram Of The Loudspeaker Amplifier

VOICE SWITCHES

The extra gain of about 30dB of the microphone signals and of the received signals is too much to ensure stable operation of the telephone set under all circumstances.

Therefore it is necessary to insert a loss to ensure the loop gain not to exceed unity. Since this loss will attenuate the voice signals, too, it is necessary to insert it in the channel in which no voice signals (or in practice: fewer voice signals) are present at a moment.

The amount of loss necessary can easily be calculated using Figure 4. As can be seen in this Figure the loop gain is max. 22dB in our design. The contributions of the amplifiers and the volume adjustment are quite obvious. The contributions of the acoustic coupling and the hybrid coupling are less clear.

The contribution of the acoustic coupling depends mainly on the acoustic properties of the cabinet used, the optimization of which is of paramount importance for the ultimate performance of the loudspeaking telephone set. There are three mechanisms of sound propagation from the loudspeaker to the microphone.

First, the sound can propagate via the air outside the cabinet. This contribution can be minimized by maximizing the distance between loudspeaker and microphone, i.e. placing them in opposite sides of the cabinet.

Second, the sound can travel via vibration of the cabinet which can be prevented by using a 'stiff' cabinet and a rather loose mounting of the loudspeaker and the microphone in the cabinet.

A third mechanism is the propagation via the air inside the cabinet. This contribution can be diminished by means of shielding the loudspeaker and the microphone with respect to each other and by means of filling the appropriate holes (acoustic resonators!) with material (e.g. foam, but even a printed circuit board with electronics can have a positive effect) in order to prevent the occasion of standing waves in the speech frequency spectrum.

In our design an existing cabinet has been used giving with some small modifications an acoustic coupling between loudspeaker and microphone of max. −34dB (electrically measured).

The contribution of the hybrid coupling depends on the side tone suppression which has been optimized for an average telephone line length (about 3km) and an average frequency (about 1kHz). For shortest (0km) and longest (10km) line lengths and lowest (300Hz) and highest (3400Hz) frequencies this suppression reaches a minimum. In our design the maximum hybrid coupling was measured to be 0dB at a frequency of 3400Hz. At higher frequencies the hybrid coupling was even higher and therefore it turned out to be necessary to introduce a low-pass filter into the circuit. This has been realized in the receiving amplifier of the TEA1042 (see Figure 13, capacitor C_{80}).

The amount of loss to be introduced in the loop in our design therefore is 22dB (the sum of all contributions of Figure 4) plus a singing margin of 15dB.

The loss elements have been built using resistor networks with transistor-switches of the type BC547C to select between the loss and no-loss position (see Figure 5).

If the input of the switches is high, transistor T_{20} switches off the loss in the microphone channel by means of T_{21}, while the signals in the receiver channel are attenuated by transistor T_{22} which will have a resistance of about 60 Ohm (divider $(R_{28} + R_{29})/(R_{30} + T_{22})$). If the input of the switches is low, then transistor T_{21} is in conduction and the microphone signals are attenuated (divider $(R_{20} + R_{21})$) while the receiver channel signals pass unattenuated. T_{21} and T_{22} are applied inversely in order to minimize switching 'clicks'. As the on-resistance of transistors depends on their beta, C-types have to be used. The values of the resistors R_{20}, R_{21}, R_{28} and R_{29} depend on the type of cabinet and the type of telephone lines used. Therefore no values are given in Figure 5. See Appendix II for more details.

The voice-switch in the receiving channel is followed by an emitter-follower (T_{23}) in order to convert down the high output impedance.

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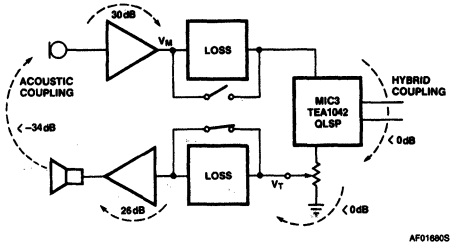

Figure 4. Calculation Of The Loss Required To Achieve Stable Operations

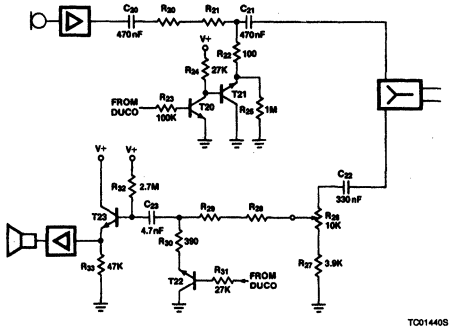

Figure 5. The Voice-Switches Used In The Microphone And Receiver Channel

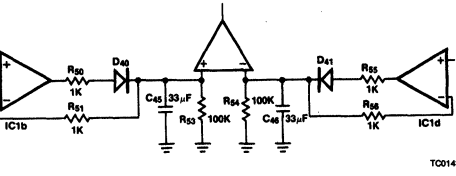

Figure 6. Simplified Circuit Diagram Of The Duplex Controller

DUPLEX CONTROLLER (DUCO)

Introduction

The voice switches are controlled by the DUCO. The task of this DUCO is to determine in which channel the stronger signals are present in order to switch off the attenuation in this channel and to insert it in the channel with the weaker voice signals. Therefore its switching behavior is of crucial importance for the ultimate performance of the loudspeaking telephone set.

A simplified circuit diagram is shown in Figure 6. The circuit has been built using three op amps of the LM324. Two of them are used as peak-value rectifiers, one for the signals coming from the microphone preamplifier and one for the received signals coming from the TEA1042 (pin QLSP).

During the positive parts of the (AC) input signals the capacitors C_{45} and C_{46} will be charged to the peak value of their respective input voltages. During the negative parts, however, the diodes D_{40} and D_{41} are blocked and the capacitors can discharge only via the resistors R_{53} and R_{54} respectively. The time constants R_{53}*C_{45} and R_{54}*C_{46} are chosen rather high in order to diminish the influence of echo signals; if after a signal is received from the telephone line, capacitor C_{46} is discharged before the echos in the room have ebbed away, the voltage on C_{45} could be the higher voltage resulting in an unwanted switching action. The resistors R_{50} and R_{55} have been included in order to diminish the influence of spike voltages at the inputs.

The rectified signals are then compared in the third op amp which is used as a comparator. If the microphone signals are the stronger signals its output will be high and vice versa.

Attenuators

It is not possible to include this DUCO in Figure 5 without additional measures. To understand this it is necessary to look carefully at the Figures 7 and 8.

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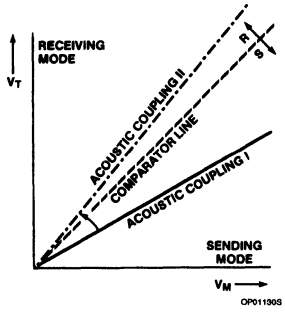

Figure 7. Influence Of Acoustic Coupling

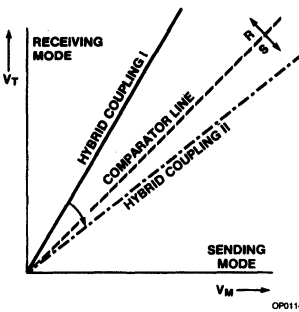

Figure 8. Influence Of Hybrid Coupling

When the telephone set is in the receiving mode, its microphone receives rather strong signals from its loudspeaker. This is called the acoustic coupling. As can be seen in Figure 4 the signals after the microphone preamplifier, v_m, are in our design up to 22dB stronger than the original signals v_t.

The (linear) relation of this acoustic feedback signals with the original signals v_t is shown in Figure 7 by the line 'acoustic coupling I'. As the comparator selects the stronger signals as is shown by the dashed line in Figure 7 the loudspeaking telephone set would immediately switch into the sending mode as a result of its own acoustic feedback.

In order to prevent such unwanted switching action, it is necessary to attenuate the microphone signals which are fed to the DUCO to such an amount that the acoustic feedback signals never can become greater than the original signals v_t. As a result the acoustic coupling line (Figure 7) will turn off until it falls completely in the receiving mode part of the figure ('acoustic coupling II').

Note that the acoustic coupling in practice is extremely frequency-dependent. Therefore it is necessary for stable operation of the DUCO that the acoustic coupling line for every frequency is in the receiving mode part of Figure 7.

There is a similar problem in the sending mode of the loudspeaking telephone set. Dependent on the hybrid coupling and the position of the volume regulator, the signals v_t received via the hybrid might be slightly greater than the original microphone signals v_m. This also will cause unstable operation of the DUCO as is shown in Figure 8 by the line 'hybrid coupling I'. As the comparator still selects the stronger signal (dashed line), the loudspeaking telephone set would select the receiving mode as a result of its own hybrid coupling.

To prevent unwanted switching actions it is necessary to introduce a loss in the receiver input of the DUCO in this sending mode in order to ensure the hybrid coupled signals always to be smaller than the original signals v_m. The hybrid coupling line in Figure 8 will then turn off until it falls completely in the sending mode area of the figure ('hybrid coupling II').

Note again that this demand must be fulfilled under all circumstances, especially for the maximum volume position of the volume regulator together with maximum hybrid coupled signals (i.e. maximum line impedance mismatching).

The input-attenuators have been realized as a tap on the respective speech attenuators. This is shown in Figure 9 ($R_{20} - R_{21}$ in the sending channel; $R_{28} - R_{29}$ in the receiving channel).

In the sending position (output of the comparator high) transistor T_{21} is blocked, switching off the attenuator in the microphone input of the DUCO. Transistor T_{22} is conducting inserting a loss determined by divider $R_{28}/(R_{29} + R_{30} + T_{22})$ in the receiving channel in order to turn off the hybrid coupling line into the sending mode part of Figure 8.

In the receiving position (output of the comparator low) transistor T_{22} is blocked, switching off the attenuator in the receiving channel; T_{21} is conducting inserting the attenuator $R_{20}/(R_{21} + R_{22} + T_{21})$ in the microphone channel in order to turn off the acoustic coupling line into the receiving mode part of Figure 7. See Appendix II for more details.

In principle the DUCO only has to be supplied with signals of the part of the frequency spectrum from about 500 to 2000Hz. In this part of the spectrum the strongest voice signals are present, therefore allowing for a reliable decision of the DUCO.

In the acoustic coupling of the cabinet used in our design there are some resonances at frequencies of about 3kHz. As the acoustic coupling line for every frequency has to be in the receiving mode part of Figure 7, the loss in the DUCO microphone input has to be adjusted at the acoustic coupling at these frequencies. Therefore it is advantageous in our design to introduce a lowpass filter in this input (R_{40}/C_{41}; cut-off frequency: 2000Hz) giving an additional loss for this frequency and thus allowing for a reduction of the required loss of the attenuator. This measure turns out to be advantageous for the interruption behavior of the loudspeaking telephone set.

In order to counteract this filter at frequencies above about 5kHz (which is necessary due to the increased hybrid coupling at this and higher frequencies) a second lowpass filter has been included in the receiver input of the DUCO (R_{60}/C_{49}) with a cut-off frequency of 5kHz. Two emitter-followers (T_{40} and T_{41}) convert down the high output impedance of the filters.

DC-Adjustments And Hysteresis

For the DC-adjustment of the DUCO it is not sufficient to supply R_{43} and R_{57} with a suitable common DC voltage. Referring to Figures 7 and 8 this would result in an undefined position of the comparator in the absence of input signals ($v_t = v_m = 0$, zero crossing point) due to offset voltages of the op amps and due to always present noise signals on the inputs.

Offset voltage compensation has been realized with R_{49} in Figure 10. With this resistor the DC voltage at the receiver input (via R_{57}) of the DUCO can be made slightly different from the DC voltage at the microphone input (via R_{43}) of the DUCO. See Appendix II for more details.

In order to make the DUCO bistable, even in the absence of input signals, a small positive feedback has been made. This has been realized with R_{52} in Figure 10. The capacitors C_{43} and C_{47} increase the positive feedback of the circuit during switching actions resulting in a firm switch-over.

In Figure 10 the circuit diagram of the part of the duplex controller considered here is given.

POWER SUPPLY OF THE CIRCUIT

The circuit described in the preceding chapters consumes a supply current of about 5mA in quiescent state while the loudspeaker amplifier will need another 5mA to power the loudspeaker in the receiving state. This is far above the supply capacity of the supply point of the TEA1042 which is about 1mA.

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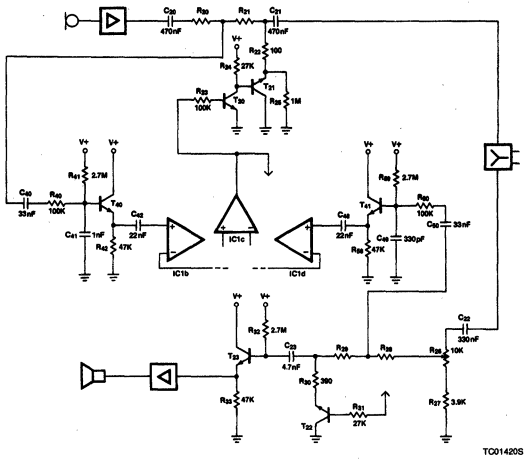

Figure 9. Simplified Circuit Diagram Of DUCO Including Attenuators

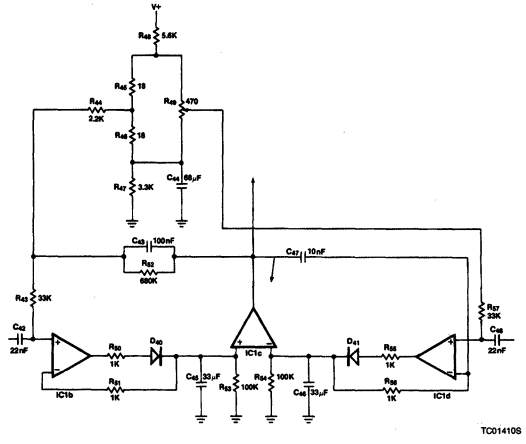

Figure 10. Circuit Diagram Of The DC-adjustment And Hysteresis Measurements Of The Duplex-controller.

Therefore it is necessary to bridge the 620 Ohm supply resistor R_{71} of the TEA1042 (see Figure 11) with an inductor resulting in a low supply voltage drop at high supply currents for DC and in a high impedance for speech frequencies thus keeping the good balance return loss figures of the TEA1042 itself.

A coil with these properties is rather bulky. Therefore we have chosen an electronic solution. This is shown in Figure 11. For DC this circuit acts as a resistance of 15 Ohm (R_{63}) in series with a diode (0.7V voltage drop across the base-emitter transition of T_{60}). For AC it acts as an inductance of about 10H (R_{63}*R_{61}*C_{60}).

This supply circuit itself consumes about 1mA supply current resulting in a total (quiescent) current of the loudspeaking circuitry of 6mA.

APPLICATION DIAGRAM AND PRINTED CIRCUIT BOARD

In Figures 12 and 13 a complete application diagram of the loudspeaking circuit with the TEA1042 transmission circuit has been given. In Appendix I a parts list is given.

C.A.B. have developed a p.c. board (C.A.B. Elcoma nr. 3206) which contains all the circuitry. The print lay-out is shown in Figure 14.

In Appendix II a summary of required adjustments is given.

CONCLUSIONS

Using the TEA1042 transmission circuit it is possible with the rather simple circuitry presented in this report to make a loudspeaking telephone with good performance. The circuit is powered from the telephone line.

To obtain optimal performance it is very important to adjust the duplex controller carefully to its cabinet (acoustic coupling) and to the types of telephone lines used (hybrid coupling). Appendix II might help you in the adjustment procedure.

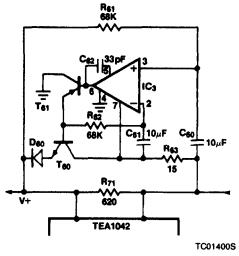

Figure 11. Circuit Diagram Of The Supply Circuit For The Loudspeaking Equipment

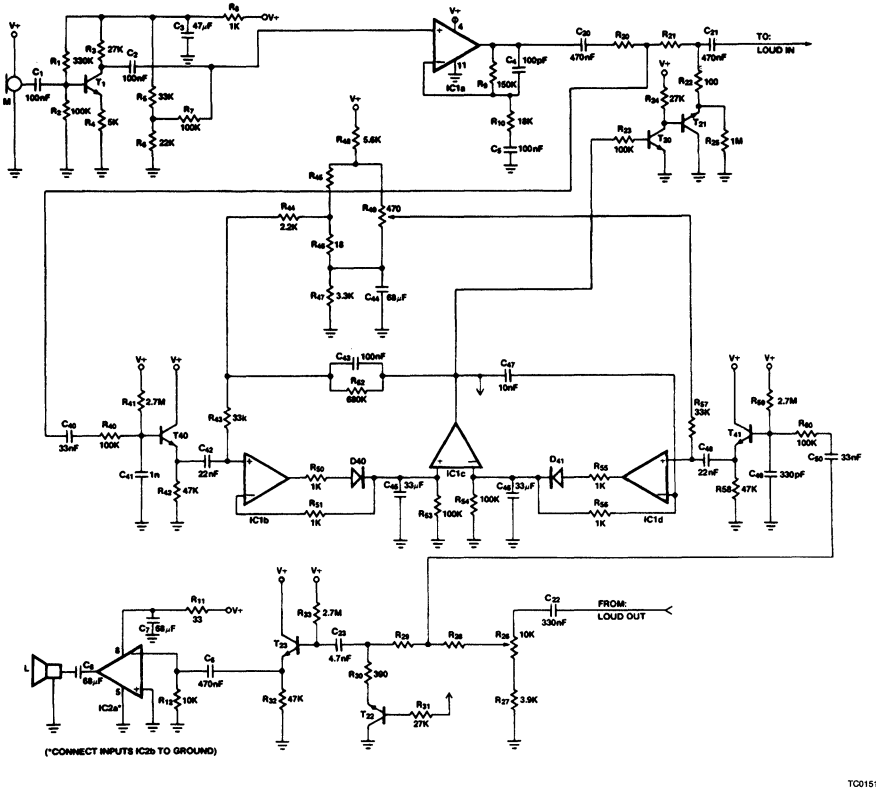

Figure 12. Application Diagram Of The Loudspeaking Circuitry With The TEA1042 Circuit (Loudspeaking Part).

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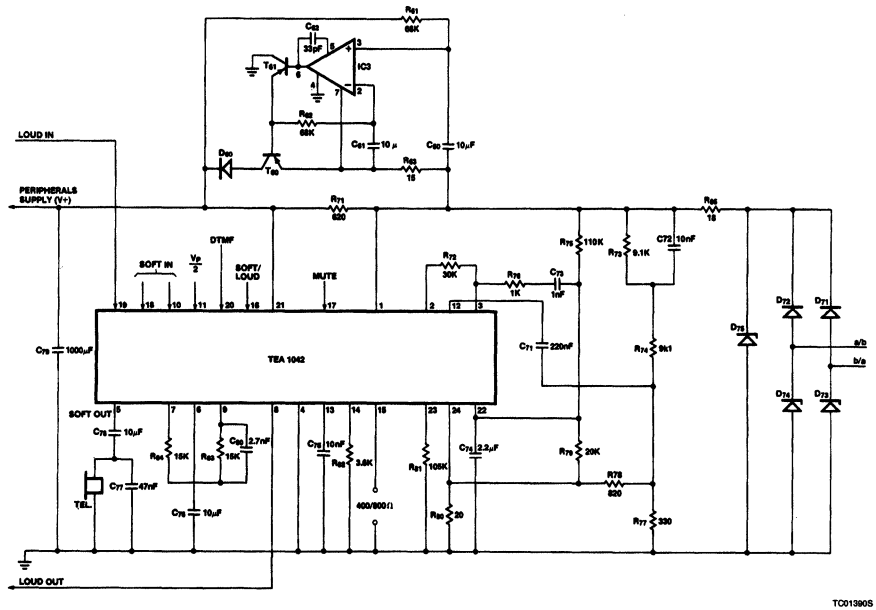


Figure 13. Application Diagram Of The Loudspeaking Circuitry With The TEA1042 Circuit (Transmission Circuit And Supply).

APPENDIX I: PARTS LIST

ITEM	DESCRIPTION
R1	330K
R2, 7, 23, 40, 53, 54, 60	100K
R3, 24, 31	27K
R4, 48	5.6K
R5, 43, 57	33K
R6	22K
R8, 50, 51, 55, 56, 76	1K
R9	150K
R10	18K
R11	33
R12	10K
R20, 21, 28, 29	*
R22	100
R25	1M
R26	10K log potm.
R27	3.9K
R30	390
R32, 41, 59	2.7M
R33, 42, 58	47K
R44	2.2K
R45, 46	18
R47	3.3K
R49	470 10t-potm.
R52	680K

ITEM	DESCRIPTION
R61, 62	68K
R63	15
R71	620
R72	30K
R73, 74	9.1K
R75	110K
R77	330
R78	820
R79	20K
R80	20
R81	105K
R82	3.6K
R83, 84	15K
R85	18
C1, 2, 5, 43	100nF
C3	47μF
C4	100pF
C6, 20, 21	470nF
C7, 8, 44	68μF
C22	330nF
C23	4.7nF
C40, 50	33nF
C41, 73	1nF
C42, 48	22nF
C45, 46	33μF

ITEM	DESCRIPTION
C47, 72, 75	10nF
C49	330pF
C60, 61, 76, 78	10μF
C62	33pF
C71	220nF
C74	2.2μF
C77	47nF
C79	1000μF
C80	2.7nF
D40, 41	BAW62
D60	BAT85
D71, 72	BAS11
D73, 74	BZW14
D75	BZX79C12
T1	BC549
T20	BC547
T21, 22	BC547C
T23, 40, 41	BC547A
T60, 61	BC557
IC1	LM324N
IC2	TDA7050
IC3	TCA520B
IC4	TEA1042
L	AD3071/Y50

* t.b.f.; see Appendix II

APPENDIX II: SUMMARY OF REQUIRED ADJUSTMENTS

N.B. apply and measure all voltages with respect to ground.

Dimension the Voice-switches in the Sending and Receiving Channel ($R_{20} + R_{21}$, $R_{28} + R_{29}$)

A suitable method is the following:
Remove R_{20}, R_{21}, R_{28}, R_{29}. Make the output of the comparator ICIc LOW (receiving position) by means of R_{49} (extreme position of 10 turn potmeter; measure on R_{52} (solder tag 1)). Apply an AC voltage (10..30mV) of variable frequency to C_{23}/R_{30} (solder tag 2). Measure the transfer function between this point and C_{20} (solder tag 3) for frequencies of 100Hz to 10kHz. This measurement gives you the transfer function of the loudspeaker amplifier plus microphone amplifier plus the cabinet (acoustic coupling).

Keep in mind that the acoustic coupling is influenced by persons (or things) in the surroundings of the cabinet. It might be necessary to include this influence in the measurements.

Now apply the AC voltage to C_{21}/R_{22} (solder tag 4). Make the output of the comparator HIGH (sending position) by means of R_{49} (other extreme position). Adjust maximum volume with the volume regulator. Measure the transfer function between this point and the wiper of R_{26} (solder tag 5) for frequencies of 100Hz to 10kHz. This measurement gives you the transfer function of the sending and receiving amplifiers of the TEA1042 plus the sidetone network (hybrid coupling). Note that the hybrid coupling component is dependent on the type and length of telephone line used and on its termination. Do this measurement for several telephone line lengths, types and terminations in order to find the worst-case transfer function.

The sum of these two worst-case transfer functions gives you, at a certain frequency, the maximum loop gain of the telephone set. Since this loop gain must always remain lower than −15dB the loss required for the voice-switches is 15dB plus the measured maximum loop gain. This loss must be realized by a suitable choice of ($R_{20} + R_{21}$) for the microphone loss element and by ($R_{28} + R_{29}$) for the receiving loss element.

In order to prepare the circuit for the adjustments 2 and 3, choose R_{21} and R_{28} zero (shortcircuit) and make R_{20} and R_{29} equal to the sum resistances calculated above, ($R_{20} + R_{21}$) respectively ($R_{28} + R_{29}$).

Dimension the Loss Element in the Sending Input of the Duplex Controller (R_{20}, R_{21})

A suitable method is:
Make the output of the comparator ICIc LOW (receiving position). Apply an AC voltage of 10 − 30mV to R_{28}/R_{26} (solder tag 5). Measure the transfer functions from this point to R_{57}/C_{48} and to R_{43}/C_{42}. As the signals on R_{43}/C_{42} always have to be smaller than the signals on R_{57}/C_{48} for proper operation of the DUCO, the difference (in dB) of the two transfer functions (R_{43}/C_{42} minus R_{57}/C_{48}) has to be less than 0dB for every frequency in the band of 100Hz to 10kHz. Strong negative values, which you are likely to find now, will negatively influence the switching sensitivity. You have achieved the optimal loss if the difference is less than or equal to −5dB for every frequency which gives you a reasonable switching sensitivity and a good overall stability (even if something or someone is near to the cabinet (increased acoustic coupling) or in the presence of echo signals).

The resistance which is now in R_{20} alone must be divided over R_{20} and R_{21} (without altering the sum of the resistances!) to such an amount that the −5dB demand sketched above is fulfilled.

Calculate the Required Loss in the Receiving Input of the Duplex Controller

A suitable method is:
Make the output of the comparator ICIc HIGH (sending position). Apply an AC voltage of 10 − 30mV to C_{20}/R_{20} (solder tag 3). Measure the transfer functions from this point to R_{43}/C_{42} and to R_{57}/C_{48}. As the signals on R_{57}/C_{48} always have to be smaller than the signals on R_{43}/C_{42} for proper operation of the DUCO, the difference (in dB) of the two transfer functions (R_{57}/C_{48} minus R_{43}/C_{42}) has to be less than 0dB for every frequency in the band of 100Hz to 10kHz. You are likely to find a slightly positive value for the worst case telephone line types, lengths and terminations. The optimal value for the difference is now about −2dB.

The resistance which is now in R_{29} alone must be divided over R_{28} and R_{29} (without altering the sum resistance) to such an amount that the −2dB demand sketched above is fulfilled.

Now the optimal values for the resistors R_{20}, R_{21}, R_{28} and R_{29} have been found. You might wish to check points 2 and 3 once again. Be sure the difference between the two transfer functions in point 2 is −5dB and more and in point 3 is −2dB and more for every frequency.

DC-adjustment

a − Adjust maximum voltage on R_{57}/R_{49} with R_{49}. the duplex controller is monostable now; if no signals are applied to it it will switch to the receiving position.

b − Turn R_{49} until the duplex controller tends to become bistable: if only a microphone signal has been applied to it it remains in the sending position. Mark the position of the potentiometer.

c − Continue turning R_{49} until the duplex controller tends to become monostable again; if no signals are applied to it, it switches to the sending position. Mark this position of the potentiometer, too.

d − Adjust R_{49} between the two marks until the DUCO operates stable, i.e. there are no unwanted switching actions anymore.

The adjustment procedure has been finished now. The circuit now must operate quite well. In case you still have problems with the circuit the list given below might help you. This list assumes that you have done the adjustments 1 to 4 as described above.

TROUBLESHOOTING LIST

- Unwanted switching actions to sending position while the DUCO has to remain in the receiving position.

This might be caused by echo signals. Some remedies are possible:

1) Enlarge C_{45} and C_{46}. Disadvantage: the DUCO will switch slower.
2) Decrease R_{52}. This increases the hysteresis of the DUCO. Disadvantage: switching sensitivity will decrease.
3) Increase R_{20} and/or decrease R_{21}. Disadvantage: the sensitivity for switching to sending position will decrease.

- DUCO switches too slow to the other position.

This is caused by a too large time constant in the peak value rectifiers. Decrease C_{45} and C_{46}. Disadvantage: sensitivity for echo signals will increase.

- DUCO sensitivity for switching to sending position is not enough.

This might be caused by a strong acoustic coupling between loudspeaker and microphone which demands for a high loss in the microphone input of the DUCO. Try to decrease the acoustic coupling. Don't forget to readjust the circuit according to the points 1 to 4 in this Appendix after changes in the acoustic coupling have been made.

SAA5350 A Single-Chip CRT Controller AN152

The SAA5350 is a VLSI Advanced Peripheral Display Controller (APDC) containing approximately 120,000 transistors in advanced NMOS technology.

The APDC may be used for many display terminal applications such as color video monitors, personal computers, medical/industrial equipment, picture-telephones, videotex terminals, dot color printers, workstations and more.

Video systems design is made simple when using the APDC. The APDC can easily interface to a general purpose 8 or 16-bit microprocessor and act as a DMA device when accessing the display memory. Due to stack coding technique and the on-chip character ROM, external display memory requirements are minimal; 4K bytes is sufficient to create a high resolution, full color, animated display. Figure 1 depicts a typical Videotex terminal implementation using the SAA5350. The 4K bytes include a 2K bytes user defined Dynamically Redefinable Character Set (DRCS). The DRCS Concept is a powerful technique which allows each pixel of a character cell to be individually set permitting almost unlimited expansion of the character repertoire and the display of more complex alphabets (Cyrillic, Arabic, Katakana, etc.) simple pictures, company logos, and other symbols (Figure 2).

The main features of the APDC are:

- 40/80 column by 20/24 row display
- On-chip ROM containing 512 alphanumeric characters
- Dynamically Redefinable Character Set (DRCS) capability
- On-chip scroll map
- On-chip color look-up table RAM and three D/A converters with gamma corrected outputs (32 colors/row-total color palette of 4,096 colors)
- Various flashing modes
- Many display attributes: double height, double width, double size, invert, conceal, window, . . . etc.
- Easy interface to 8 or 16-bit microprocessors
- DMA capability to system display memory (this IC has a 16-bit multiplexed address and data bus.)
- Three synchronization modes; standalone, simple slave or phase locked slave, allowing easy implementation of text-in-picture or picture-in-text type displays.

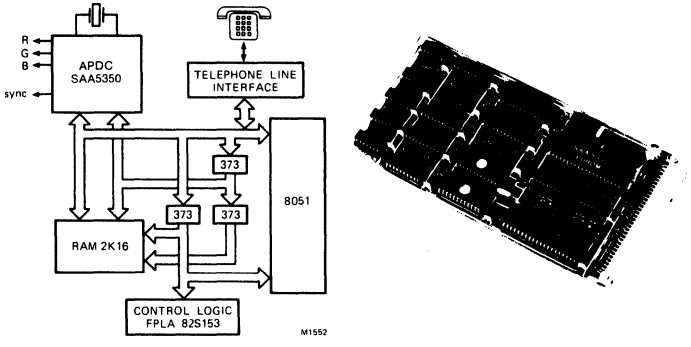


Figure 1. Videotex Decoder Using the SAA5350

- Composite sync output
- Support both interlaced and non-interlaced type displays
- Designed for 625 line systems
- Single 5V supply, 40-pin DIP

This application note outlines how the APDC operates, summarizes its attributes and gives examples of how it interfaces with microprocessors and display memory. The concepts of stack coding and DRCS are also briefly described.

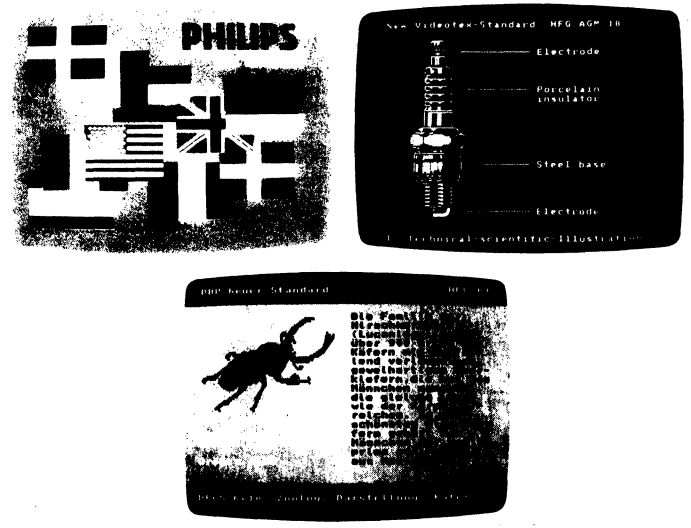


Figure 2. Examples of Displays Using DRCS

SAA5350 A Single-Chip CRT Controller AN152

SAA5350 CRT Controller IC APDC

A block diagram of APDC is shown in Figure 3. The APDC contains the following general functions: timing chain, character generator, attribute logic, scroll map, screen color logic, DRCS logic, and microprocessor interface.

To optimize system cost, APDC also incorporates a color map RAM and D/A converters providing RGB outputs corrected for CRT non-linearity. The on-chip scroll map eliminates the need for massive data transfer when scrolling.

Character and attribute data is fetched from the external memory, processed by the row buffer fill logic according to the stack coding scheme (when in Stack Mode), and then fed into one half of the

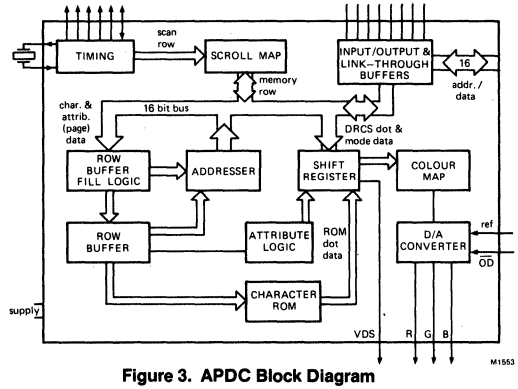


Figure 3. APDC Block Diagram

DYNAMICALLY REDEFINABLE CHARACTER SETS (DRCS)

In a basic alphamosaic system, the shape of each character is stored as a dot (pixel) pattern within a defined matrix. Since the repertoire of possible characters within the matrix is finite, simple and inexpensive decoders can be designed. The use of DRCS, however, enormously extends the display repertoire. Using DRCS, additional characters can be defined by the information provider, and then used as part of the character set for a specific page or group of pages. The additional characters can be used singly, or as alphanumerics in a different alphabet, or as symbols in timetables, etc. They can also be used in groups to create simple designs such as company logos.

In essence DRCS requires the transmission of the dot pattern for each character matrix and the allocation of a code to that matrix. When transmitting a page containing DRCS, the DRCS data can be transmitted independently of the page information and stored in DRCS RAM. For display, both the fixed and the DRCS character tables are used, depending on the character code stored in the page memory.

The DRCS character cell is based on a 12 pixel horizontal resolution. When operating with 10 lines/row, the following modes, each representing different combinations of horizontal, vertical, and color resolutions, are available.

10 lines/row

Mode	Pixel Configuration (h x v)	Bits/Pixel	Maximum Number of Characters/Chapter*
1	12 x 10	1	102
2	12 x 10	2	51
3	6 x 10	1	2 x 102
4	6 x 10	2	102
5	6 x 10	4	51
6	6 x 5	2	2 x 102
7	6 x 5	4	102

*one chapter contains 1024 16-bit words

12 lines/row

Mode	Pixel Configuration	Bits/Pixel	Maximum Number of Characters/Chapter*
8	12 x 12	1	85
9	12 x 12	2	42
10	6 x 12	1	2 x 85
11	6 x 12	2	85
12	6 x 12	4	42
13	6 x 6	2	2 x 85
14	6 x 6	4	85

APDC can also operate in a 6 x 10, 4 bits/pixel mode with a memory organization more suited to bit-map implementation.

When operating with 12 lines/row, fewer characters are available per chapter.

All attributes apply to DRCS in the same manner as to normal characters, but for multi-color DRCS (that is, the modes with more than one data bit per pixel) the following rules apply:

- The whole character cell is treated as foreground color
- When the Conceal (or Flash, Invert) attribute is used, the background color that would otherwise be pertaining is displayed
- The Underline attribute has no effect (the one bit/pixel DRCS modes are underlined as normal alphanumeric characters).

When operating with 2 bits/pixel color DRCS, the DCLUT (DRCS Color Look-up Table) is used. This behaves as a small RAM that maps the four combinations of two bits onto any four fo the 32 locations in the color map.

When operating with 4 bits/pixel color DRCS, the 16 combinations can be taken either from locations 0 to 15 or from locations 16 to 31 of the color map depending on the value of a register bit.

The physical organization of APDC's DRCS memory is 1K16 (1024 16-bit words) for Tables 4 and 5, and a further 1K16 for Tables 6 and 7. In addition to the page memory pointer, two independent memory pointers in APDC indicate the beginning of each 1K16 'chapter' of DRCS memory.

dual display row buffer. The data fetch process takes place during one line flyback period (per row), and since time is required to complete the fill, the other half of the dual row buffer is used for display. The row buffers exchange functions on alternate rows; each holds the 40 columns of 32 bits required to define explicitly every character in a row.

The addresser is used for row buffer filling and for fetching screen colors; during the display time it is also used for addressing DRCS characters.

Timing

The timing chain operates from an external 6MHz clock or the on-chip fixed-frequency crystal oscillator. The basic format is 40 characters per row, 24/25 rows per page, 10 video lines per row.

APDC will also operate with 20/21 rows per page, 12 video lines per row. (This meets the requirements of Ref. 2 which embodies the DIN standard on terminal ergonomics, reducing operator fatigue by improving the readability of displayed text.)

The two extra lines per row are added symmetrically, and contain background color only for ROM-based alphanumeric characters. DRCS characters, block and smooth mosaics, and line drawing characters, however, occupy all 12 lines.

The display is generated to the normal 625-line/50Hz scanning standard, interlaced or non-interlaced. In addition to composite sync for conventional timebases, a clock output at 1 MHz or 6 MHz is available for driving other videotex devices, and a 12MHz clock is available for hardcopy dot synchronization. A Defined Display Area timing signal simplifies the application of external peripherals such as a light pen. This signal is nominally coincident with the character dot information.

Character Generation

APDC supports eight character tables, each of nominally 128 characters. Four are in on-chip ROM and contain fixed characters, and four for DRCS are stored in external RAM. The contents of the fixed character tables (Tables 0 to 3) are shown in Figures 4 and 5.

Table 0 contains the 128 most commonly used characters: standard upper- and lower-case Roman alphabet, numerals, punctuation, and the more common accented characters. In normal text transmission, Table 0 is used most of the time.

Table 1 contains further accented characters.

Table 2 contains a number of miscellaneous characters, mathematical symbols, the line drawing character set, and accents without associated characters.

Table 3 contains the block mosaics for the basic alphamosaic service, together with the new smooth mosaics. The two sets are complementary and can readily be combined to create pleasing graphic displays such as maps, some examples of which are shown in Figure 6. Although the editorial need for these characters has decreased somewhat with the availability of DRCS, being pre-defined and resident on-chip, their use makes for savings in transmission time and avoids the waiting times associated with the downloading of DRCS characters.

Tables 4, 5, 6 and 7 are stored in external memory and are used for DRCS.

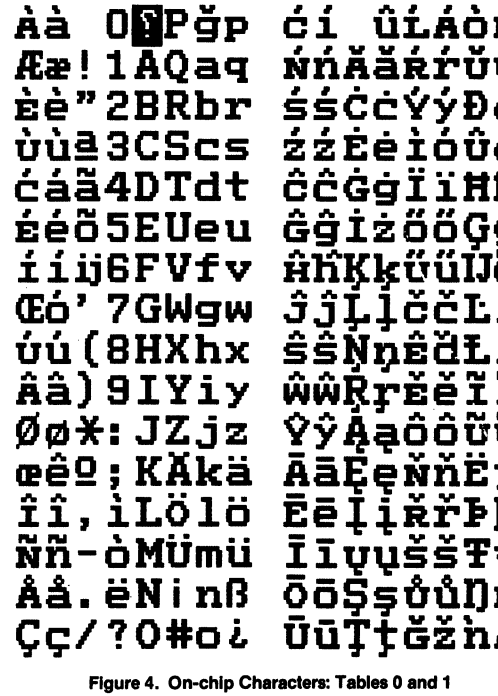


Figure 4. On-chip Characters: Tables 0 and 1

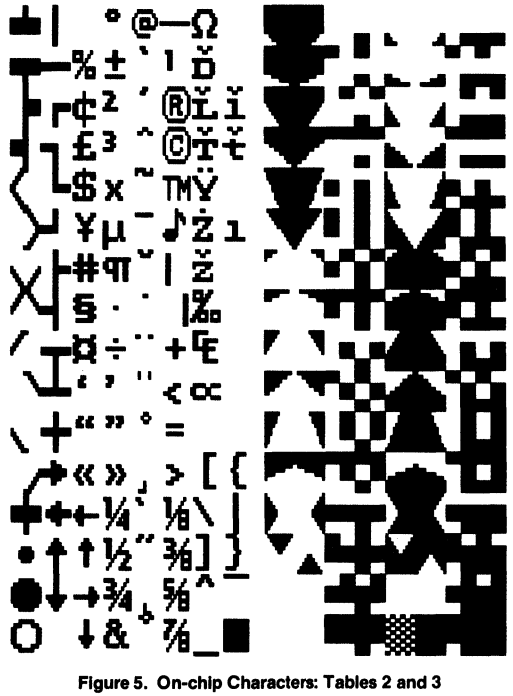


Figure 5. On-chip Characters: Tables 2 and 3

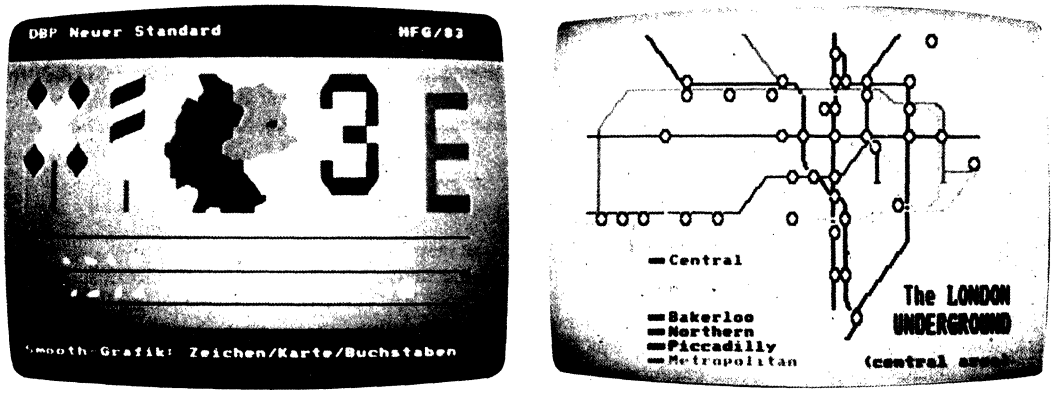


Figure 6. Examples of Displays Using Smooth and Mosaic Line Drawing Characters

Scroll Map

Associated with the timing chain is the scroll map, an area of on-chip RAM of 26 bytes. It maps the scan row on to the fetched memory row, allowing the stored page to be displayed in any row order. For each row, a one-byte pointer to the display memory row is stored in the scroll map. This allows scrolling without the need for data transfer to or from side storage. Additional control bits are stored, allowing 1 to 25 rows to be displayed at any location on the screen.

Color Map and D/A Converters

The on-chip color map and D/A converters considerably simplify the external circuitry. The color map RAM contains 32 12-bit words that are loaded by the microprocessor and read out in three 4-bit groups at pixel rate. Each group is fed to a non-linear (gamma-corrected) D/A converter. The resulting R, G, and B outputs are low impedance with peak-to-peak amplitudes controlled by the voltage applied to the Reference Pin.

Cursor

A cursor is available in Stack Mode. Its position, character code, character table, foreground color, background color, lining and flash attributes are all software programmable via internal register bits.

DISPLAY ATTRIBUTES

APDC provides the following attributes for any character displayed.

Foreground Color

Foreground color is coded in five bits, implying a total of 32 colors. Of these, 31 represent specific locations in the color map; the last is interpreted as transparent.

When a pixel is set to transparent, the display color pointer is set to the value of the screen color at this location. If the screen color attribute is also transparent, the underlying tv picture, if any, is unblanked (i.e. displayed).

The 32nd location is also used during line or field flyback to output blanking level (black).

Background Color

Background color operates in exactly the same way as foreground color, with five bits defining 31 colors plus transparent.

Screen Color

The color of the screen may also be set to any one of the 31 color map locations, or transparent. The screen is notionally divided into 27 areas corresponding to the 25 rows and the upper and lower border areas. Each of these 27 areas can refer to a different location in the color map.

Flash

Ref. 2 defines three states and six rates of flash. Other combinations such as 3-phase flash at 1Hz are not required but nonetheless are available with APDC.

Three flash states defined by Ref. 2 are:

- normal flash (active pixels alternating between foreground and background colors)
- inverted flash (in antiphase with normal flash)
- color table flash, where the active pixels alternate between two colors in the color map

The six flash rates are:

- 2-phase 1Hz flash (even flashing at 1Hz)
- each phase of 3-phase 2 Hz flash
- ICF (increment flash)
- DCF (decrement flash)

If the image of an object is given sequential phases in adjacent character cells, three-phase flash gives the impression of movement along a row. Three-phase flash can also be used with DRCS to produce dynamic displays without the need for continuous transmission.
The ICF and DCF attributes cause objects to appear to move right or left respectively, in the same way as with 3-phase flash. It avoids the need to specify flash phase explicitly on a per-character basis. In Stack Mode, APDC automatically supplies the correct phase. This method of specifying object motion reduces transmission time and serial attribute memory utilization.

STACK CODING

For full implementation of all the required functions in APDC, 32 bits per character location are necessary. This means that to display a full screen of 25 rows of 40 characters, 4 Kbytes of external memory are required — four times the capacity of a basic alphamosaic decoder memory, excluding any DRCS requirements.

7 Bits Character Code
3 Bits Character Table
5 Bits Foreground Color
5 Bits Background Color
5 Bits Flash
3 Bits Size (D.HT., Top/Bot., D.Width)
1 Bit Lining (Underline or Mosaic Separation)
1 Bit Conceal
1 Bit Invert
1 Bit Window/Box

32 Bits per character position

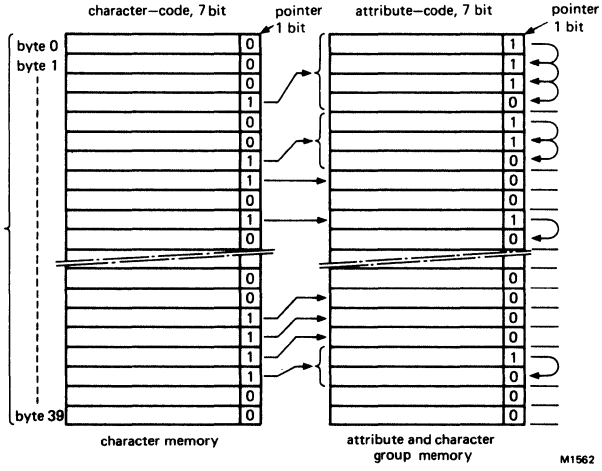
To reduce the amount of memory required, attributes in APDC are coded using a Stack architecture. Such a system exploits the natural redundancy of normal text by allocating memory dynamically. It allows the external memory to be reduced to 2 Kbytes per screen. This has beneficial side effects; for example, it reduces the memory bandwidth for a given display, reducing the memory speed required or increasing the time available for microprocessor operations.

In the stack coding system used in APDC, the page memory is divided into character and attribute sections, each organized as 40-byte groups. The 40 character bytes and 40 attribute bytes together make up one displayed row.

Each 8-bit byte includes a pointer bit. When the pointer bit of a character byte is set, it indicates the presence of one or more attributes set at the same character position. When the pointer bit of an attribute byte is set, it indicates that there are further attributes in that group. At the beginning of a row, default attributes are set, which are then updated by the attribute bytes fetched from the stack.

An example of stack coding is given in the Figure. The first three characters of the row have clear pointer bits. These characters will be taken from the default group of 128 (on-chip) characters, and will be displayed white on black, normal size, not underlined, etc. The fourth character in the row has its pointer bit set, and so the first (or, generally, the next) attribute byte is fetched from memory. This byte also has its pointer bit set, and so the next attribute byte is also fetched, and so on.

The fourth attribute byte has a clear pointer bit indicating that it is the last in the group. The next character byte is now fetched. The pointer being clear, this character is displayed with the same attributes as those set for the previous one.



Example of Dynamic Allocation of Memory Using Coding Stack

The stack system records only the position in a row where attribute-changes occur, with no restriction upon how many attribute-changes apply to any one character. The restriction to 40 attribute-changes in a row has been carefully studied, and not found in practice to be an editorial limitation; it is built in to Ref. 2 as a transmission requirement.

The actual coding of attributes, a form of Huffman coding, is shown below.

Stack coding used in APDC

B7	B6	B5	B4	B3	B2	B1	B0	Comments
P	0	0	F4	F3	F2	F1	F0	Foreground color (PIBGR) Transparent = 00000
P	0	1	B4	B3	B2	B1	B0	Background color (PIBGR) Transparent = 00000
P	1	0	H4	H3	H2	H1	H0	Flash
P	1	1	0	L	T2	T1	T0	Character Table and Lock bit
P	1	1	1	0	0	G	D	Size. Double Height and Width
P	1	1	1	0	1	0	U	Underline (Lining)
P	1	1	1	0	1	1	I	Invert
P	1	1	1	1	0	0	C	Conceal
P	1	1	1	1	0	1	W	Window/Box
P	1	1	1	1	1	0	H	Marked area (not a display attribute)
P	1	1	1	1	1	1	P	Protected area (not a display attribute)

9

Character Size
Double height is available in the basic alphamosaic service, with certain restrictions. For example, a single row can contain only top or bottom halves of characters, not both, and so double-height characters cannot be interleaved. In accordance with Ref. 1 APDC provides double-width and double-size in addition to double-height, with no restrictions on horizontal or vertical interleaving.

In Stack Mode, APDC applies 'size rules' to determine the displayed output when conflicts occur; for example, if the bottom half of a double-height character would occupy the same position as the right-hand half of a double-width character. Part characters are never displayed.

Lining
For alphanumeric characters, the Lining attribute underlines the character. For mosaics and line drawing characters, it separates the character into six blocks or sub-squares (mosaic separation).

Conceal
The Conceal attribute makes the foreground and background colors the same until a local reveal function is activated. The local reveal function can be applied either to the whole field or on a row-by-row basis, allowing progressive reveal in response to user interaction.

Invert
This attribute exchanges the foreground and background colors and is included for compatibility with Teletel transmission codes. It also applies to Flash, giving anti-phase instead of normal flash.

Box/Window
If the basic frame begins in tv mode, this attribute superimposes a box containing text (Foreground and Background or Screen colors) on the tv picture. It is compatible with the Box function used in the basic alphamosaic teletext service.

If the basic frame begins in text mode, the attribute provides a Window. That is, it sets the screen color to transparent at the character positions where it applies, so that the underlying tv picture is visible at pixels that are not obscured by foreground or background colors.

White Button
Various attributes and combinations of attributes can cause on-screen data to be obscured — double height/double width, conceal, foreground and background colors the same, etc. It is a requirement of Ref. 2 that this effect can be negated by a user function, colloquially known as the 'white button', which sets all the attributes to their default values without affecting the display memory contents. This function is implemented in APDC by a microprocessor-defined register bit which is active in Stack, Explicit Fill, and 80 Characters/Row modes (see later).

ADDITIONAL FEATURES
As well as exceeding the Ref. 1 specification in several respects — supplementary flash modes for example — APDC offers a number of features which are outside the specification, giving the IC a wider range of application.

Explicit Fill
In Explicit Fill mode, the page memory is not stack coded, and no processing is carried out during the Row Buffer Fill operation. Data from the memory is transferred directly to the row buffer.

Since there is then an explicit representation of all the attributes at every character location, there is no limit to the number of attribute changes on a given row. However, this mode requires a larger amount of external RAM (6 Kbytes/page including DRCS memory). Also, enlarged characters are not checked, so the rules concerning the size attributes must be implemented in software.

80-Characters/Row
The 80-character mode is also an explicit fill mode without stack coding. No additional circuitry is required; the row buffer is effectively rearranged as 80 16-bit words, each containing:

- 8 character bits
- 3 foreground color bits
- 3 background color bits
- 1 underline bit
- 1 flash bit

Dot data is fetched from external memory in the same way that DRCS data is retrieved. All characters are displayed as a 6 x 10 dot matrix, with both one and two bits/dot modes available. In the one bit/dot mode, the external dot memory need only be eight bits wide. When using 10 lines/row, 204 different character matrices may be stored in a 2K8 memory.

The flash mode incorporates color table flash. For maximum flexibility of display the foreground and background colors are applied to different areas of the color map.

Full-Field DRCS
For alphageometric and similar applications, a bit-map display is desirable, where each pixel on the screen corresponds to a location in the memory. APDC implements this indirectly by expanding the DRCS character repertoire so that the entire defined display area can be covered with fully random data.

One chapter (1K16) of DRCS memory can contain data for 51 6x10x4 (6 pixels wide, 10 pixels high, 4 bits per pixel) characters, sufficient for two complete character columns. If after these two columns have been scanned, the DRCS chapter is incremented to a new area of memory, a further two columns can be covered with different random data.

This method of using 20 contiguous chapters of display memory and incrementing the DRCS chapter latch in synchronism with the horizontal scan forms the basis of the full-field DRCS mode. All DRCS modes, on-chip ROM-based characters, and attributes are still available.

If, for example, a less memory-intensive DRCS mode, such as 12x10x1, is desired, then the necessary 10 chapters can be addressed by omitting the least significant chapter bit (A11) from the memory address.

MICROPROCESSOR AND RAM INTERFACE
Three types of data transfer take place at the bus interface:

- APDC fetches data from the display memory
- The microprocessor reads from, or writes to, APDC internal register map
- The microprocessor accesses the display memory

APDC Access to Display Memory
APDC accesses the external display memory via a 16-bit multiplexed address and data bus with a 500 ns cycle time. Figure 7 shows a rudimentary RAM interface circuit and bus timing diagram. When APDC accesses the display memory, its Address Strobe signal $\overline{AS}$ flags the bus cycle and writes the address into the '373 latches. The display RAMs, shown in Fig. 10 as two 8-bit blocks, are enabled with

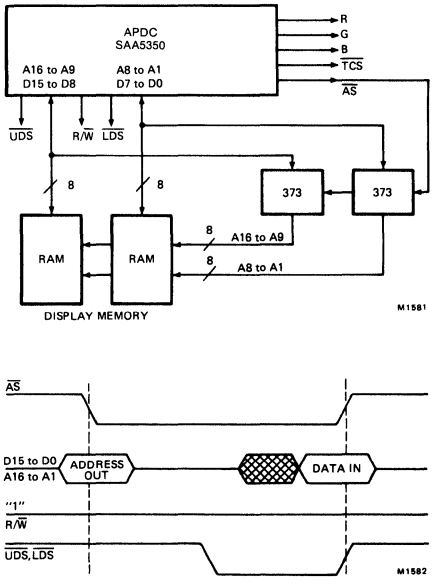


Figure 7. APDC Access to Display Memory

Upper Data Strobe, $\overline{UDS}$, and Lower Data Strobe, $\overline{LDS}$, respectively. (APDC never actually fetches a single byte from memory; $\overline{UDS}$ and $\overline{LDS}$ are alway asserted together to fetch a 16-bit word.) The Read/Write control signal, R/$\overline{W}$ is included for completeness although APDC only reads the display memory.

Although the APDC data bus is 16 bits wide, the data fetched is often considered to exist in terms of bytes and so the byte addressing convention is important. The standard adopted is that of the 68000 microprocessor where the even-numbered bytes exist on the left or upper (most significant) part of the bus, as shown in Fig. 8. The word addresses are numerically the same as the upper byte they contain — there are no odd-numbered word addresses.

Warning Time

Because APDC is a real-time display device, it must have direct access to the display memory with priority over the controlling microprocessor or other peripheral devices. To achieve this, APDC issues a Bus Request $\overline{BR}$ signal for the duration of the memory access plus a programmable advance warning time to allow the microprocessor to complete its current bus cycle.

In systems where the microprocessor's bus and APDC's bus are intimately connected, (a 'connected' system), $\overline{BR}$ may be used to suspend all microprocessor activity so that APDC acts as a dedicated DMA controller. In systems where the two buses are separated by buffers ('disconnected' systems), the $\overline{BR}$ signal may be used either to generate an interrupt or as a directly testable signal. To these ends, the warning time between the assertion of $\overline{BR}$ and the beginning of APDC's bus activity is programmable from 0 to 23 μs.

Microprocessor Access to APDC's Register Map

The set of internal registers, when memory-mapped, behave as an 8-bit wide RAM connected to the upper part of APDC's bus; see Fig. 9. The control signals $\overline{UDS}$ and R/$\overline{W}$ are reversed to become inputs and the register map is enabled with Register Enable, $\overline{RE}$. Addresses are input via the lower portion of the bus. A Data Transfer Acknowledge signal $\overline{DTACK}$, is also generated to indicate to the microprocessor that data transfer is complete.

Fig. 10 shows the main data and address paths used in a 'connected' 68000 interface. The outputs of the '373 latches are only enabled when the 68000 has yielded the bus in response to Bus Request, $\overline{BR}$. When the register map is accessed, data is transfered via the upper part of the bus, and the microprocessor's low-order address is passed to APDC via the '244 buffer. Simultaneously, the '245 bidirectional buffer disables the signals from the low-order data bus of the 68000.

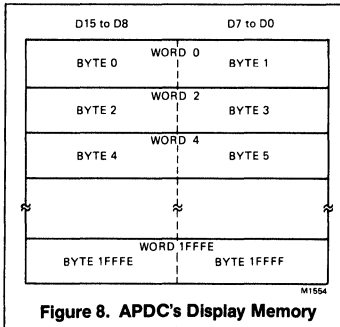


Figure 8. APDC's Display Memory Word/Byte Organization

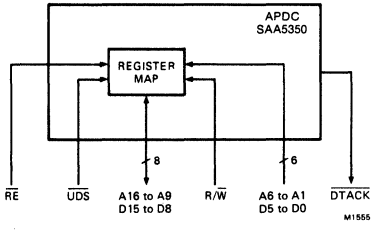


Figure 9. Processor Access to APDC's Internal Register Map

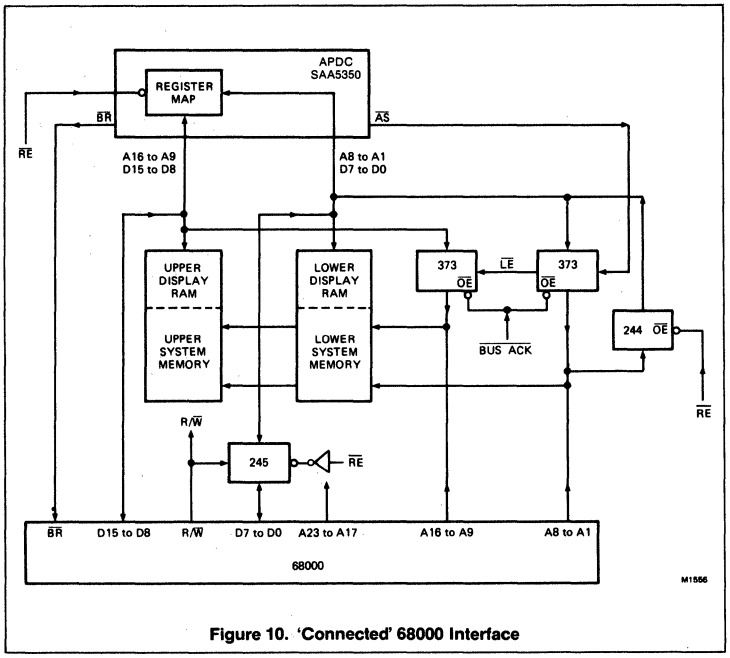


Figure 10. 'Connected' 68000 Interface

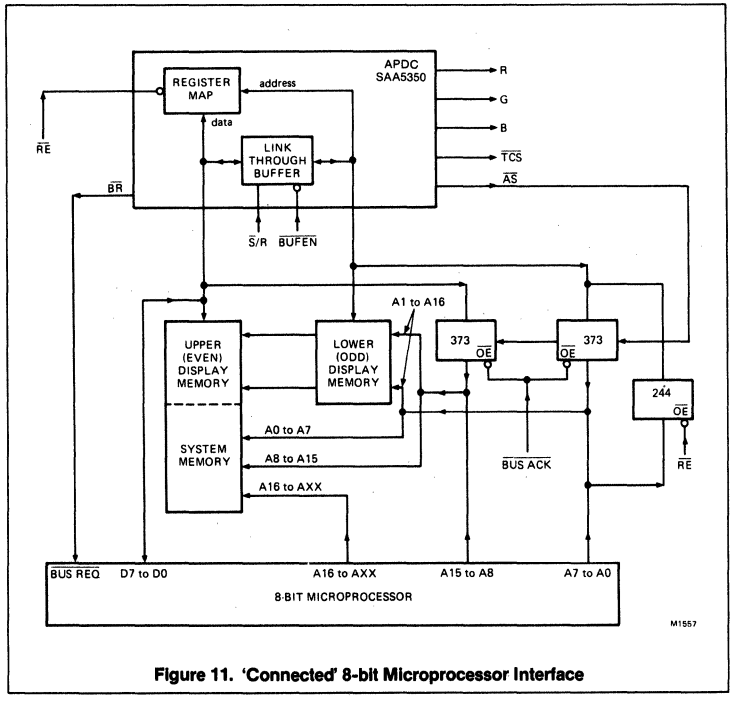


Figure 11. 'Connected' 8-bit Microprocessor Interface

The '244 and '245 buffers may be omitted in a 16-bit write-only configuration where the least-significant data byte is interpreted by APDC as an address. Here it will generally be necessary for the microprocessor to hold a (readable) 'master copy' of APDC's scroll map contents at some location in main memory.

8-bit Microprocessors

Although the control bus is optimized for the 68000, APDC will operate with a number of widely different industry-standard 8- and 16- (or more) bit microprocessors such as 80(1)88, 68008, 8051, etc. The interfacing of 8-bit microprocessors to the 16-bit wide display memory is simplified by APDC's on-chip link-through buffer which provides the microprocessor with bidirectional access to the lower (odd byte) half of the display RAM. The link-through buffer is enabled with Buffer Enable, $\overline{\text{BUFEN}}$, and its Send/Receive direction is controlled by $\overline{\text{S}}$/R which is physically the same APDC pin as R/$\overline{\text{W}}$.

Fig. 11 shows the main data and address paths used in a 'connected' 8-bit microprocessor interface. This is very similar to the 68000 interface but it should be noted that the display memory does not receive A0 as an address, rather A0 (when high) is used as the major enabling signal for $\overline{\text{BUFEN}}$.

Disconnected Systems

For many applications it may be desirable to 'disconnect' APDC and the display RAM from the microprocessor and its ROM, RAM, and peripherals. The two parts of the system then operate independently and communicate only when the microprocessor accesses APDC's register map or the display memory. Fig. 12 shows the rudiments of such an 8-bit system; it can be seen that the main data and address paths are essentially the same as those described above, the only difference being the addition of a set of isolating buffers.

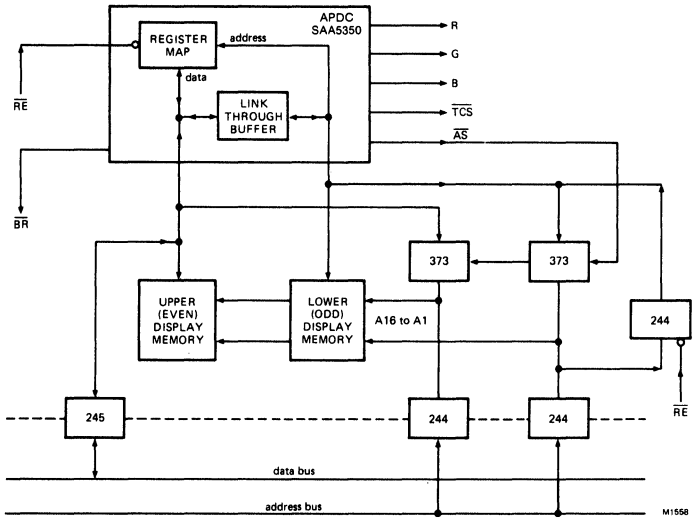


Figure 12. 'Disconnected' 8-bit System

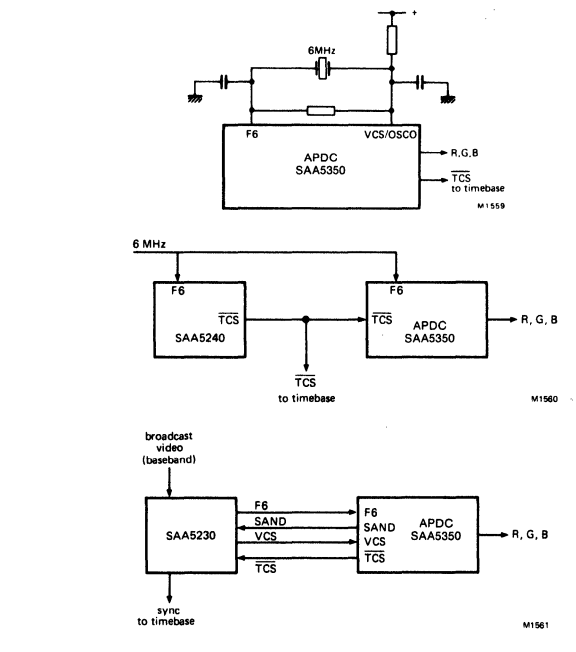


Figure 13. Synchronization Modes
a. Stand-alone
b. Simple Slave (Direct Sync)
c. Phase-locked Slave (Indirect Sync)

Synchronization

APDC has three synchronization modes. As a stand-alone device (in terminal applications for example, it can output a composite sync signal $\overline{TCS}$ to the display timebase IC or to a monitor. Timing is derived from a 6 MHz on-chip oscillator with an external crystal as shown in Fig. 13a.

APDC can also sync directly to another device, such as the $\overline{TCS}$ signal from the SAA5240 teletext IC or another APDC, as shown in Fig. 13b. APDC's horizontal counter is reset by the falling edge of $\overline{TCS}$. A dead time of 250 ns is built-in to avoid resetting the counter on every tv line, so that screen jitter does not occur. Field synchronization is achieved with APDC's internal field sync separator.

The third mode is phase-locked slave operation, as in Fig. 13c. In the SAA5230 video input processor IC, an internal phase-locked VCO provides a 6 MHz clock. When APDC is active, its horizontal counter is part of the phase control loop; a horizontal reference is fed back to the SAA5230 via the SAND pin and the vertical reference is generated by feeding separated composite sync via the VCS pin into APDC's field sync separator. In this mode, the display derived from APDC can sync with that from a tv source or a local VLP (laser disc) player, to allow picture-in-text displays, as might be used, for example, in the travel industry.

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The 5 Chip Set Teletext Decoder AN153

Author: D. S. Hobbs

SYSTEM REQUIREMENTS

The current 525 line (modified U.K.) Teletext system differs in a few respects from the 625 line system for which the U.K. chip set was designed. These are:

(a) Data Rate 5.727272Mb/s.
(b) Data bytes per data line 32.
(c) Gearing bit system for routing data to RAM.
(d) Approximately 200 display lines available for text with normal raster geometry.

These are catered for in the decoder described below so that the 625 line chip set is presented with signals which it can interpret correctly and provide a suitable display for general use.

Data Rate (a) and (b)

(a) To accomodate the lower data rate the clock coil and tuning capacitor in the SAA5020 video input processor circuit are redesigned.
(b) The write enable (WOK) signal from TAC (SAA5040) to the RAM is limited to 32 data bytes in GALA.

Gearing Bit System (c)

This is accomodated in the Gearing and Address Logic chip (GALA). Since 40 characters per row are displayed, whereas only 32 are transmitted per data line, a routing system is used to position character data in RAM as it is received.

The left hand part of the display is built up by 32 byte rows of data positioned in RAM by transmitted ROW addresses. The right hand side of the display is 'filled-in' by 4 sequential groups of 8 characters sent as one data line but stored in RAM as the last 8 bytes of 4 sequential rows. A gearing bit in the magazine number/row address group (see Table 1) is set to '1' if fill-in information is being transmitted and to '0' if left hand rows are sent. The ROW address of the data line containing the gearing bit set to '1' determines the starting ROW number for the fill-in operation. For ROW zero start, a ROW address for ROW number 1 is employed since ROW zero can only be used for header information. The presence of the gearing bit set = 1 together with ROW address number 1 is detected in GALA.

From Table 1 it will be seen that the gearing bit occupies the position occupied by the most significant bit of the magazine number in the 625 system. In order to allow the Teletext Acquisition Chip (TAC, SAA5040B) to acquire data from such lines the gearing bit is detected by GALA and converted always to zero. This preserves the magazine number as that set by the two least significant bits. The number of magazines available using the present decoder is 4. (Subsequent development of new chip sets will allow expansion of these by using header coding at present designated as time coded page information and detected as such by the 625 line TAC).

Display Compression (d)

In order to allow the display of 40 characters per row and 24 rows on a 525 line raster, a compression technique has been developed which only requires 192 active t.v. line pairs (interlaced). The character shape is essentially unchanged from the 625 line set but the row timing is now only every 8 t.v. lines instead of every 10. This is achieved using a special 525 line standard timing chip (SAA5025D), to drive the same TROM (SAA5050) as is used in the 625 line decoder.

DECODER BLOCK SCHEMATIC

Diagram 1 shows the basic decoder elements in block form, made up of dedicated chips SAA5025D, SAA5030, SAA5040B, SAA5045 (GALA) and SAA5050 together with RAM. These are divided into functional areas to simplify the decoder description. Only the most important inter-connections are shown in order to reduce complexity.

Inputs to the system are the video input to the Video Input Processor (VIP) and remote control signals (see Appendix 'A'), to (TAC) and (TROM).

Outputs consist of R, G and B, blanking, Y and superimpose control. These allow flexible interfacing with the t.v. set video drive system. (See Appendix B).

Video Input Processor (SAA5030)

This chip (VIP) performs mainly analogue functions concerned with extracting the data signal from the t.v. set video and presenting it in a suitable form to the Teletext Acquisition Chip (TAC, SAA5040B).

VIP also provides a phase locked crystal oscillator at 384MHz horizontal line rate, i.e. 6.041957MHz. This frequency is divided down in the Timing Chip (TIC, SAA5025D) to produce all the line and field related timing waveform locked to the input video sync pulses. As ancillary to this function VIP includes a sync separator to provide field rate sync to TIC.

Data is sliced in VIP by an adaptive slicer referenced to peak detectors. This is followed by Data Clock regeneration in an DC circuit. A data latch driven internally supplies latched data, correctly phased with the Data Clock, to TAC.

Gearing And Address Logic Array (GALA) SAA5045

Due to the system differences between 525 and 625 line Teletext the data from VIP must be modified before it is presented to the Teletext Acquisition Chip (TAC, SAA5040B). The presence of a gearing bit set to '1' or '0' is detected in GALA and the data is delayed for one byte period in a shift register. This allows the inversion of the gearing bit, if required, to avoid confusion in the decoding of the magazine number (see paragraph on Gearing Bit System).

GALA includes a bistable which is set or not set, according to the state of the gearing bit. This is held for the duration of each data line and reset before the next. Also included in GALA are RAM address and read/write control functions.

Table 1. Data Line Coding for 525 Line Teletext (U.K. Modified) System Characteristics Current for Operating Systems 1982

CLOCK RUN IN	CLOCK RUN IN	FRAMING CODE	MAGAZINE AND ROW ADDRESS																							DATA	DATA
1 0 1 0 1 0 1 0	1 0 1 0 1 0 1 0	1 1 1 0 0 1 0 0																									
DATA RATE 5.727272Mb/s (364 H = 8/5 COLOR SC) DATA PERIOD = 174.6ns H PERIOD = 63.55μs 32 BYTES DATA/LINE 32/8 SYSTEM 24 ROWS 40 CHARACTERS			P	2^0	P	2^1	P	2^2	P	2^0	P	2^1	P	2^2	P	2^3	P	2^4	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	
			Hamming	Magazine 1	Hamming	Magazine 2	Hamming	Gearing Bit	Hamming	Row Address 1	Hamming	Row Address 2	Hamming	Row Address 3	Hamming	Row Address 4	Hamming	Row Address 5	Data 0	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7	Data 0	Etc.
			Invert Bit 1			Invert Bit 2	Invert Bit 3	Invert Bit 4																				
← Start CRI 9.5 Microsec. From Sync 0 (Operation Normal As For 625)			Conversion Coding When Gearing Bit = 1								Operation Normal As For 625 Except Write RAM ENABLE (DATA) Limited To 32 Bytes →															

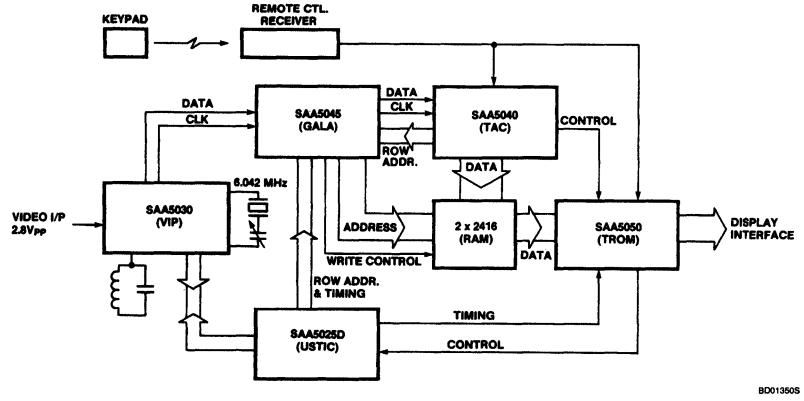

Figure 1. 5-Chip Decoder Block Schematic

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The 5 Chip Set Teletext Decoder AN153

Teletext Acquisition and Control (TAC, SAA5040B)

Data from GALA is clocked into TAC, by the data clock (5.727272MHz), where it is decoded byte by byte to provide character and control data for the storage in RAM. Row addresses are decoded after Hamming checks and issued to the RAM address system. A column address clock for writing into RAM during data lines (WACK) is also generated at byte (character) rate. Parity checking is carried out to produce write enable pulses ($\overline{WOK}$) for each correctly received character to be written into RAM.

Header (row zero) information is also decoded and Hamming checked in TAC so that only the data relating to the page called up by the remote control system (Key Pad input of required page number) is written into RAM. Clearing functions are also controlled by Header and Remote Control input data, to clear the RAM.

Selected page number information is written into RAM by TAC during an unused t.v. line between the end of data entry (DEW) and the start of the text display period. When double height characters are requested (via remote control) TAC issues commands to the timing chain (TIC) and display device (TROM). Similarly the system controls for TEXT or TV or MIXED (Text + t.v.), are issued by TAC as picture ON (PO) and display enable (DE) to VIP and TROM.

Timing Chain (TIC, SAA5025D)

The timing of line and field rate functions together with display dot clock are derived from the VIP crystal oscillator (6.041957MHz) signal fed to TIC. This signal is counted down to line rate (÷384) and field rate, phase locked to the incoming t.v. syncs. A composite sync waveform ($\overline{AHS}$) is also generated which free runs (under crystal control) to allow display of text to continue after the t.v. signal has ended. This is known as 'after hours sync'.

Row addresses for the display period are generated in TIC (A_0 through A_4) together with a column count (character rate) clock (RACK). The row addresses are stepped from zero to twenty three at one eighth of t.v. line rate giving 24 rows at 8 lines/row in each field (60 fields/sec.). This address information for reading RAM is multiplexed with the writing address information under control of a field rate signal generated by TIC, called (DEW) or data entry window. This is timed to occur on t.v. lines 10 through 19 inclusive which are the lines in the vertical interval during which data is accepted. The DEW signal controls data entry in (TAC) and also the address tristate switches.

Signals fed back from TIC to VIP are used to reset the data slicer system and to enable rapid phase locking of the crystal oscillator. A buffered dot rate clock at crystal frequency is issued by TIC to drive the display generators in TROM. The display area on the t.v. raster is controlled by the (LOSE) signal from TIC (load output shift register enable) which occurs on all active text lines.

When double height characters are called up by control signals from (TAC), originated at the Key Pad, the row addresses are stepped at half rate and the top or bottom of the display is selected by the (T/B) signal. This resets the row address counter in TIC to start at row zero or twelve of the text display.

Address Logic (GALA)

The address logic in GALA contains column address counters for the character rate address generation, a multiplexer for address combining and an address latch/step function for the gearing system. Since the teletext address structure for transmission and display contains five row address bits and six column address bits these must be reduced to a total of ten bits to suit conventional RAM structures. This is achieved in GALA by multiplexing the Row and column addresses.

During the input of data lines, containing a gearing bit set to '1', a multiplexer causes the row address to be indexed every 8 bytes. The multiplexer is transparent to addresses during data lines containing a gearing bit set to zero. The row addresses from TAC go to the GALA and are multiplexed with the display row addresses under control of (DEW), by tristates in Tlc and TAC.

Random Access Memory (RAM)

Character data from TAC is stored in a page display memory with a capacity of 1024 eight bit bytes. Of these only 960 bytes of seven bit length are actually used. Data is written in during acquisition from (TAC) and read out during display to TROM, under control of write enable and chip select signals, generated from the $\overline{WOK}$ and DE signals from TAC via GALA. A common input/output bus structure is used in the devices employed in this decoder. Conflict of signal direction is avoided in the $\overline{WOK}$/DE gating arrangement in GALA.

Display Compression (5025D)

The drive signals from TIC (5025D) to TROM during the display period are organized so that suitably shaped characters are generated by TROM on an 8 t.v. line pair per row basis. Since TROM is primarily intended for 10 line pairs per row operation, it is necessary to provide effectively 10 drive pulses per row per field although output dot data is only required on eight of these in each field. The compression logic in TIC (5025D) inserts additional step pulses during the horizontal sync interval to keep the internal counters in TROM in the correct sequence. A further operation included is the blanking of the display during the same period to avoid spurious 'dots' on the t.v. tube. Character rounding normally employed in the TROM character generator is also controlled to obtain the best shaped 'compressed' characters.

Teletext Read Only Memory (TROM, SAA5050)

This device contains the read only memory and character generating system which produces the text display (and graphics) characters. It is controlled by direct input remote control signals (Key Pad originated) and by transmitted controls via TAC. Timing of the display system is controlled by signals from TIC and the actual display data is read in from the page memory RAM.

Output signals for R, G, B, Y, Blanking and superimpose are available by open collector transistor output buffers. These are interfaced to the regular t.v. video drive system via 75Ω emitter followers in this decoder. However, it is simple to obtain outputs at different impedance levels by changing the emitter follower input/output components or by substituting TTL buffers with input pull-up resistors. Interfacing will differ for different setmakers but the 75Ω 1V p-p system is flexible in allowing long connections between the decoder and the video circuits of the t.v.

FUNCTIONAL LOGIC INTERCONNECTION SCHEMATIC

The complete decoder is built on a double side P.C.B. with Molex 0.1″ pitch plug connectors. Supplies required are 150mA at 12V and 250mA at 5V ± 5%. The supply rails are decoupled by distributed discrete 100n capacitors not shown on the circuit diagram. P.C.B. layout is only critical in the analogue area surrounding VIP where connections must be kept short and ground paths sensibly routed. Good video frequency practice is followed in this area to ensure minimum radiation of interference and suppression of local oscillatory effects.

VIP Circuit

IC4 the SAA5030 device has a number of discrete resistors and capacitors connected to it to define operating levels and frequencies. Tuning capacitors C_{17}, C_{18}, C_{15}, C_{12}, C_{13} should all be of high grade r.f. tuning types. The crystal XT1 is of similar grade to a color sub-carrier crystal in that it needs good setting stability with the possibility of being 'pulled' by about ± 750Hz for phase locked operation.

The center frequency is 6.041957MHz when series connected with a load capacitance of 30pF. Capacitor C_{17} and coil L_2 form a

rejector circuit to avoid oscillation outside the correct frequency range of the crystal.

Inductor L_1 and capacitor C_{15} form the data clock recovery tuned circuit. A coil Q-factor of greater than 50 is essential for good clock recovery. A component with an unloaded Q of 90 is commonly employed. The clock coil is tuned on test by applying a video signal at pin 3 of PL3 containing data lines with pseudo random data at 5.727272MHz preferably throughout the normal display period for ease of observation on an oscilloscope. This should be connected to pin 18 of VIP.

The coil is adjusted for minimum jitter of the clock falling edge which should occur approximately at the center of the 'eye' pattern formed by syncing the source data on another trace of the oscilloscope. For best results it is preferable to trigger the oscilloscope from the data clock of the generator used to form the test data.

Phase Locking Adjustments For Sync

The series tuning capacitor C_{19} is used to adjust the center frequency of the crystal oscillator which determines horizontal (line) frequency phase lock, whereas R_{10} is adjusted for field sync lock.

The crystal circuit is adjusted first whilst observing an input video signal at pin 3 of PL3 together with a line frequency signal such as that on VIP pin 5 ('sandcastle waveform'). Connect pin 1 of VIP direct to the 12V rail, which allows the oscillator to free run, and shunt the filter capacitor C_1 with a 5.6MΩ resistor (this gives a preferred initial offset). C_{19} is then adjusted to obtain a stationary relationship between the two signals. Remove the test connections from pin 1 of VIP and C_1 when the two waveforms should remain solidly locked in phase.

Field sync adjustment can then be carried out by adjusting R_{10} whilst observing the output of (FS) at pin 13 of VIP together with the field sync of the incoming video. When correctly adjusted, the rising edge of (FS) should be half way along the second broad pulse of the field sync pattern of the input video. This adjustment is important to ensure the correct selection of data lines in the vertical interval by the (DEW) signal. Field lock in the wrong position may cause the loss of one or more data lines.

The adjustments of the decoder are now complete, all subsequent areas of operation are controlled by digital systems.

Input And Output Requirements Of VIP

The video input from the t.v. should be 2.8V p-p at pin 3 of PL3 and its DC level not greater than 7 volts. If higher, the electrolytic capacitor C_5 (1μ) may be reverse biased and cause maloperation of the DC restoration circuit in VIP.

Sync Output Signals

The t.v. set may be synchronized via VIP if a synchronized display is required from ($\overline{AHS}$) when the t.v. signal disappears. This is obtained from pin 2 of PL3. The polarity can be set by connecting resistor R_1 (1k5) via link (LPI) to +12 volts or zero volts for negative or positive going syncs respectively.

TAC (SAA5040B)

Data from GALA is clocked into TAC pin 2 by the data clock at pin 3, also from GALA. When correct data is received write enable pulses are issued from pin 15 ($\overline{WOK}$). This is an indication that Hamming codes and parity are correct. Data is output in parallel from pins 16 through 22 to RAM, whilst row address A_0 through A_4 are supplied by pins 23 – 27.

Internal Data Writing To RAM

Selected page numbers, called up by the remote control Key Pad input, are written into the row zero position in RAM together with indications such as 'HOLD' and timed page 'time'. This function occurs during t.v. line number 37 only. At this time the display enable (DE) output pin 9 is held low and $\overline{WOK}$ pulses are emitted at pin 15 in two groups of 8, corresponding to the first and last eight character spaces in row zero. Since this function occurs outside of the (DEW) period the column counters are driven by read address pulses (RACK) from TIC.

Character Generator, TROM (SAA5050)

The character generator i.c. (SAA5050) receives data from RAM during the display period (t.v. lines 48 to 239 inclusive) and internally decodes the data to generate characters or control functions. TROM receives direct remote control information on pins 3 (DATA) and 11 (DLIM) which control such functions as MIX (T.V. + text), conceal/reveal.

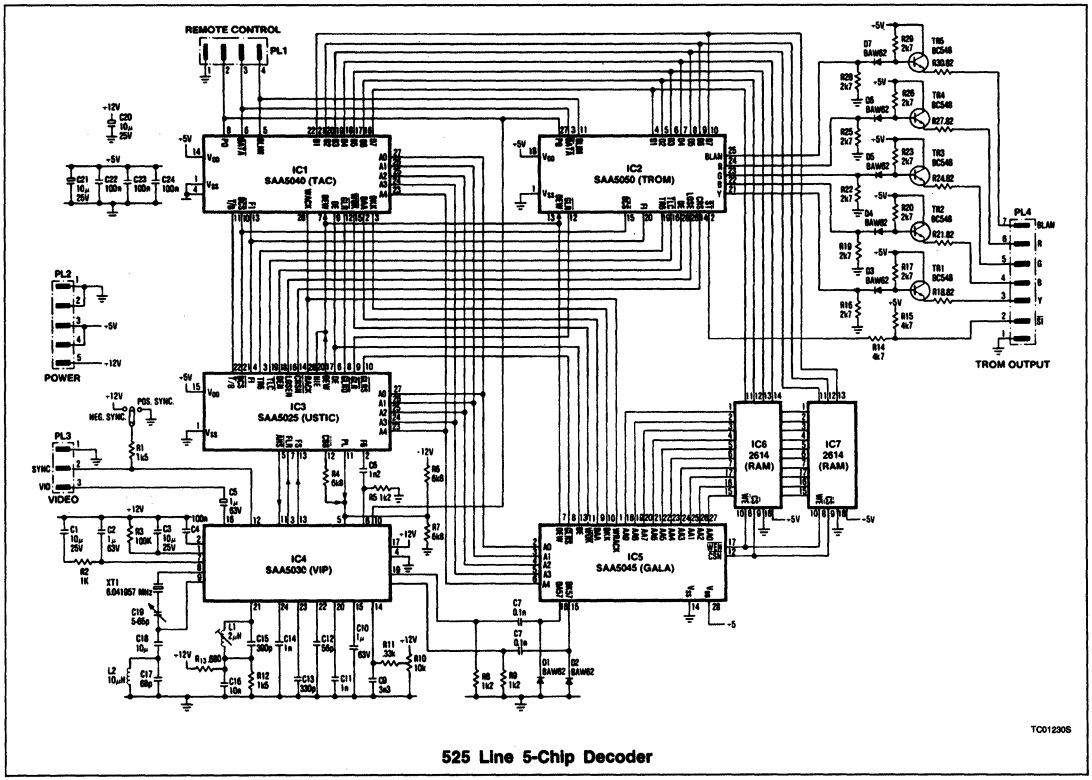
Control of display on/off (DE) and double height are received from TAC on pins 28 and 15 together with picture on (PON) pin 27. TROM outputs control signals to TIC from pin 16 when 'Transmitted Large Characters' ($\overline{TLC}$) are called up by transmitted data codes.

The video output of TROM consists of R, G and B signals at pins 24, 23 and 22 (open collector) and a Y signal pin 21 (open collector). Blanking is obtained at pin 25 (open collector) to switch the t.v. video on and off under control of signals decoded in TROM.

Superimpose signals from pin 2 are used to modify the contrast setting of the t.v. video when MIX mode is called up (by remote control or News Flash). This output pin must be connected via a pull-up resistor of 10kohm to the +5V rail whether its output is used or not.

The R, G, B, Y and Blanking output buffers will drive interface circuits directly if required provided that the open circuit output voltage does not exceed 13.2 volts maximum.

The 5 Chip Set Teletext Decoder AN153



525 Line 5-Chip Decoder

Teletext Decoders: Keeping up with the Latest Technology Advances AN154

Author: Nabil G. Damouny

ABSTRACT

The new generation teletext decoder, unlike its predecessor introduced in 1976, is user programmable under the control of a general purpose microcomputer or microprocessor. The new decoder is programmable to operate in the Vertical Blanking Interval (VBI) or full field teletext mode of operation. It can, simultaneously, acquire multi-pages resulting in a much faster system response time.

The new teletext decoder is I^2C bus controlled; therefore it is easy to integrate into any digitally controlled I^2C bus system. The modular nature of the I^2C bus architecture allows the system designer to add to or delete from his or her system various function blocks. The teletext decoder can be treated as one of these blocks.

INTRODUCTION

Integrated Circuit (IC) technology has marched a long way since the advent of the first generation teletext decoder in 1976. Some improvements and new features can now be economically incorporated in the second generation decoder while keeping the chip count even lower than its first generation counterpart.

The new generation teletext decoder is microcomputer (or microprocessor) controlled. It is user programmable and therefore more flexible and friendlier to use. Today, virtually every system is microprocessor controlled. The microprocessor controls various special purpose peripheral chips, each controlling one or more functions of the overall system. One of these peripheral chips can control the television tuning function while another chip can control the teletext acquisition and display function. The system can be designed in a modular fashion so that modules performing different functions can be added to or deleted from the system with minimal effort.

The Inter-IC (I^2C) bus has been designed to achieve modularity. Bus interfacing problems are eliminated by integrating all the necessary bus handshake logic in the on-chip silicon. The I^2C bus is a serial bus consisting of two bidirectional lines: the Serial Data (SDA) line and the Serial Clock (SCL) line.

THE NEW GENERATION TELETEXT DECODER

The new generation teletext decoder consists of a super data slicer (the Video Input Processer - VIP), the teletext controller chip, multi-page memory, and a general purpose microcomputer. (See Figure 1.)

The microcomputer communicates with the teletext controller via the I^2C. The microcomputer can be either a master or a slave; the teletext controller chip is a slave-only device.

The new teletext controller is an I^2C peripheral and belongs to the large "CLIPS" family. The new I^2C teletext decoder can be integrated in a system where a single microcomputer is used. The microcomputer is the only master and controls other system functions in addition to the teletext decoder, simultaneously. (See Figure 2.) On the other hand, since I^2C bus concept allows modularity, a multi-master system can be easily implemented. (See Figure 3.)

In the single master system, the system designer should allow for possible future software (and, consequently, memory) expansion. This is necessary to allow future system expansion. In the multi-master case, only one microcomputer is shown to receive and decode remote control commands. This microcomputer will then communicate the different commands to other microcomputers via the I^2C bus.

Microcomputers with built-in I^2C bus interface are available today. The instruction set is based on that of the industry standard 8048 microcomputer family.

The New Teletext Decoder Acquisition Circuitry

The teletext decoder accepts as input a composite video baseband signal. This signal is readily available in a TV set (to be discussed later). Digital data is inserted in the Vertical Blanking Interval (VBI) or into, virtually, all available TV lines (full field). The acquisition circuitry can be programmed to operate in the VBI or in a full field mode. Full field teletext is a useful feature contributing to a very fast system response time but, obviously, does not permit any video information to be transmitted.

Since high speed teletext digital data (data rate is 6.93MHz in Europe and only 5.72MHz in North America due to bandwidth limitation) is transmitted via broadcast information, a high performance data slicer is essential to have at the receiving end.

The video input processor should have good data slicing capability in the presence of echoes, noise, and co-channel interference. The device should provide compensation for high frequency losses and be able to regenerate the clock from the digital data. The digital data can have different rates, as mentioned above. Other desirable features that the video input processor might have include: providing a mechanism by which it is easy to lock to a VCR; having a minimal number of external components/adjustments required; being able to accept many levels of peak-to-peak amplitudes of the composite video input; and last, but not least, consuming low power.

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Teletext Decoders: Keeping Up With the Latest Technology Advances

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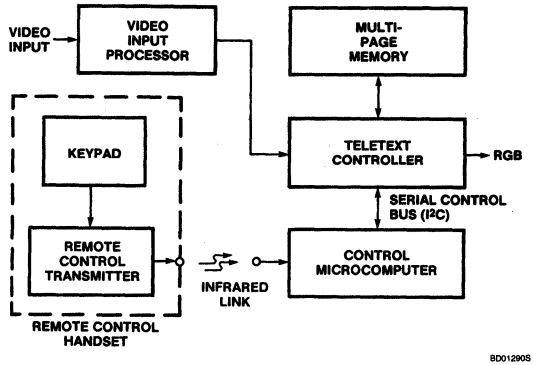

Figure 1. Computer Controlled Teletext (CCT) Decoder Block Diagram

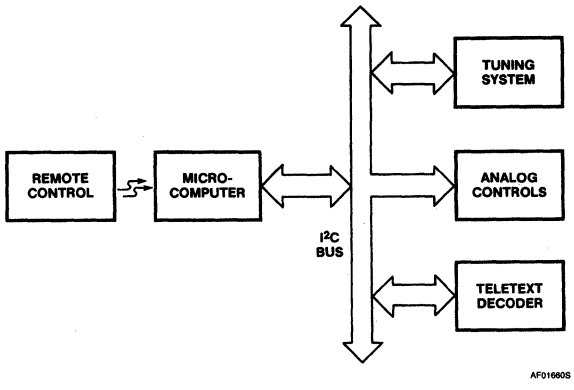

Figure 2. Centralized Control Structure

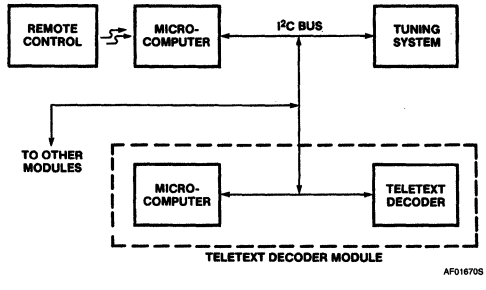

Figure 3. Distributed Control Architecture

Digital data and its associated clock (Figure 4) can now be presented by the video input processor in a nice clean form to the teletext controller chip.

The teletext controller is looking for the page addressing information, imbedded in the page header - row number 0 - to find a match with the pre-specified page number requested by the user via the remote control keypad. When a page address match is found, this page is captured and stored in page memory. In order to speed up the system response time and to make it friendlier to use, the acquisition circuitry is designed to capture four teletext pages simultaneously. Four independent acquisition circuits co-exist on the teletext controller and are able to capture four pages simultaneously. The four acquired pages can be specified, by the user program, to be the requested page plus the next three sequential pages or the requested page plus the next three linked pages as specified by the linking information received in ghost row number 27.

The teletext controller can then support up to 8K bytes of memory. If ghost rows are to be received and decoded for, 2K bytes of memory will be needed per teletext page.

The new acquisition circuitry can be programmed to receive the normal 7-bit plus one parity bit or 8-bit byte data. This is useful when a more sophisticated error correction scheme (such as CRC) needs to be implemented. The 8-bit mode is also instrumental in implementing the "telesoftware" concept. Through telesoftware, computer programs can be down-loaded and acquired as teletext information.

It is worth noting that the fixed format, World System Teletext, is virtually error free. This is due to the simple fact that a one-to-one correspondence exists between transmission codes, acquisition memory, display memory, and the actual display position on the screen. Due to the fact that teletext information is being constantly cycled through the system, an error received during one cycle can be automatically corrected during a subsequent cycle.

The New Teletext Decoder Display Circuitry

Since four pages can be acquired and stored in the acquisition memory simultaneously, but only one page can be displayed at a time, a display chapter register, residing on the teletext controller chip, is user programmable to select which acquired page is to be displayed. The display memory is, physically, the same as the acquisition memory. Ghost rows are not displayable and the display consists of 25 rows, (the 25th row contains locally generated status information), 40 characters each. The character cell occupies a 12 x 10 dot matrix, giving nicely shaped characters at 12MHz dot rate. The display could be interlaced or non-interlaced.

There are four control functions that can be individually turned on or off under user software control. These are: TV picture, text, background, and contrast reduction. Boxed text information in a TV picture can be displayed by specifying the "Start box", "End box" control characters.

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The teletext controller provides RGB outputs as well as a blanking output and a contrast reduction output. These outputs can be used as they are or a video buffer stage can be added. (See Figure 4.) This stage consists of emitter followers and clamping diodes. The diodes clamp the upper voltage values to a potential suitable for the particular TV receiver's contrast control. The blanking output is a combined box and dot blanking (full screen). The contrast reduction output is used for implementing more readable mixed (text over video) displays or to implement subtitles in reduced contrast boxes.

If a composite video display is desirable, a single chip multi-standard color encoder is available to produce PAL or NTSC compatible displays.

It is important to note that the new teletext decoder provides a secure means to synchronize the incoming video with the resulting text/video display. In addition, the decoder generates a composite sync signal that is suitable for driving the display time base.

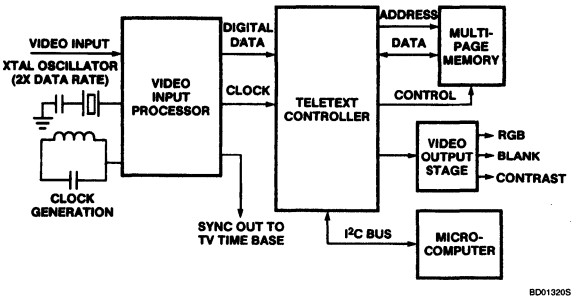

Figure 4. Teletext Decoder – Detailed Block Diagram

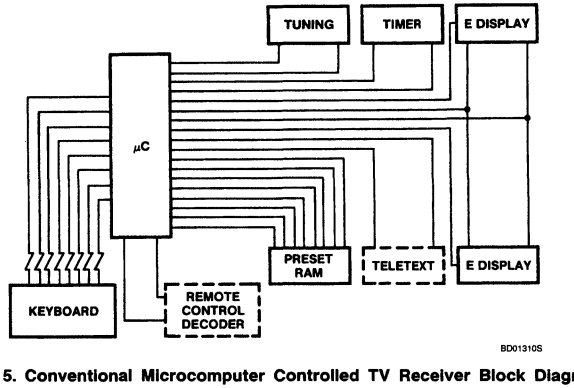

Figure 5. Conventional Microcomputer Controlled TV Receiver Block Diagram

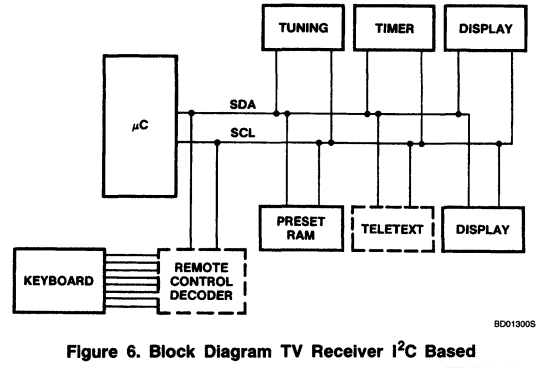

Figure 6. Block Diagram TV Receiver I²C Based

THE I²C BUS – GENERAL CONCEPT

Many system applications do not require very fast data transfer offered by the traditional parallel schemes.

As shown in Figure 5, a typical microcomputer controlled television receiver using a parallel bus type architecture implies a large number of interconnects, devices with a large number of pinouts and a bigger layout area. Since many applications do not necessarily need the speed offered by parallel bus type architecture, an economical, easy to implement solution can be used. Figure 6 depicts the television receiver block diagram designed around the 2-wire I²C serial bus.

Many devices have been implemented with on-chip I²C bus interface logic. These devices communicate through the 2-wire serial bus. The system designer will no longer worry about the communication interface between the different blocks in his or her system and can now concentrate on the more important issues: the function/system requirements. Devices with built-in I²C bus interface can be added to or deleted from the system by simply "clipping" them to the common 2-wire bus. The only limitation is the bus capacitance of 400pF. Hence a collection of these devices is known as "CLIPS".

The I²C bus consists of 2 bidirectional lines, the Serial Data (SDA) line and the Serial Clock (SCL) line. Devices with built-in I²C bus interface can be implemented in any technology, i.e. NMOS, CMOS, I²L, TTL, etc. These devices are connected together (wired-AND) to form an I²C bus-based system, provided that they all exhibit an open collector output at each of their respective SDA and SCL lines.

The I²C bus concept allows a flexible master/slave relationship to exist. A device master during the present bus cycle can be a device slave during the following bus cycle.

An I²C bus cycle starts with a START condition. (See Figures 7 and 8.) A 7-bit device (slave) address is then sent followed by a single bit to determine the direction of the data transfer. A ninth clock pulse is then

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generated by the master device to allow the addressed receiver to acknowledge reception of this byte. Now any number of 8-bit data transfers can take place with the receiver acknowledging each byte after it has been received. At the end of the data transfer, the device master generates a STOP condition.

The I^2C bus uses the wired-AND concept to achieve clock synchronization and proper arbitration between different device masters in the system. If two device masters start bidding for the bus simultaneously by generating the start condition, they will both be driving the SDA and the SCL lines. Clock synchronization is easily achieved through the wired-AND connection. The resulting clock will have a LOW period determined by the device master with the longest clock LOW period. The HIGH period of the resulting clock is determined by the device master with the shortest clock HIGH period.

Arbitration procedure in an I^2C bus system is also easy to implement. Keep in mind that all devices are wire-ANDed and that a master device driving the SDA line will sample that line during the same clock period. In Figure 9 master device 1 is driving the data line HIGH but the resulting SDA line is LOW (due to master device 2) and so transmitter 1 loses arbitration, after detecting that condition, and prepares itself as a slave that could be addressed during this very same cycle. Note that no time is wasted for the arbitration procedure since both address and data information is used to determine the winning bus master.

It is very comforting to know that all of the functions above have been implemented on all of the "CLIPS" peripherals. This allows system designers to implement modular architectures and build systems around the various available function blocks. Each function block, in its simplest form, can be one of the "CLIPS" peripherals.

TELETEXT DECODER - SYSTEM INTEGRATION

Tv Receiver With Built-in Teletext Decoder

Teletext decoders, in general, can be easily integrated into TV receivers. In reality, TV receivers can be considered a natural home to house teletext decoders. The input to the teletext decoder is composite video, baseband signal which is already available at the output of the demodulator stage in a typical TV receiver. (See Figure 10.) The output of the teletext decoder consists of RGB signals, blanking and contrast reduction/control signals. The signals are of open collector type and can be easily manipulated. A simple video output circuit might be needed at the output of the teletext decoder, the purpose of which is to provide the buffer/drive capability and the appropriate voltage level control suitable for the TV receiver under consideration. These signals can then be combined with the existing RGB and contrast control signals available at the output of the TV video amplifier stage.

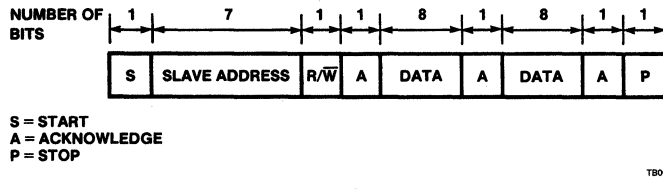

Figure 7. Typical I^2C Data Transfer

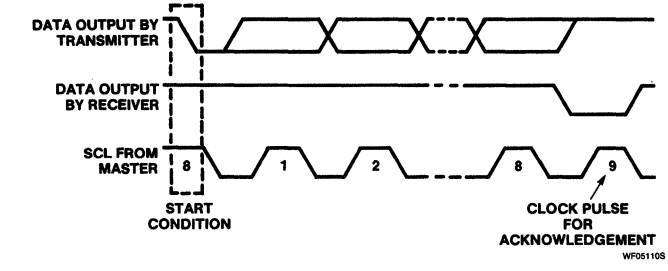

Figure 8. Acknowledgement On The I^2C Bus

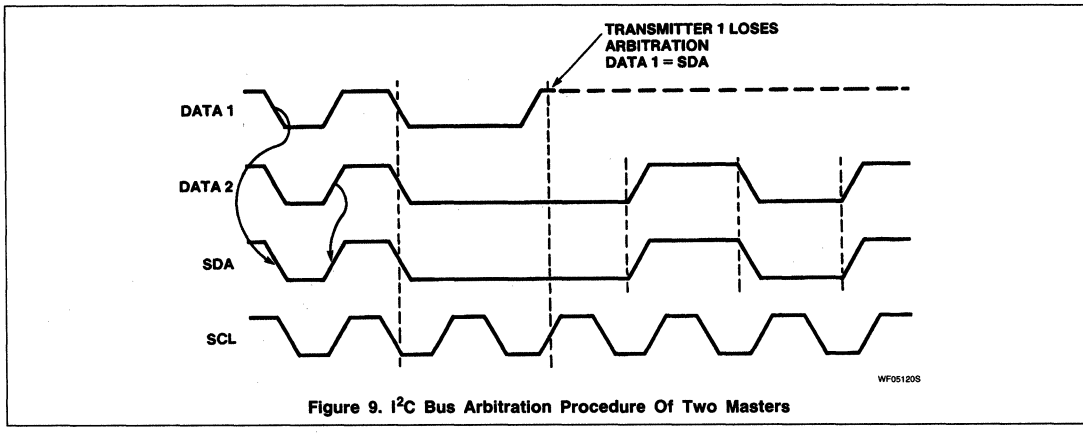

Figure 9. I^2C Bus Arbitration Procedure Of Two Masters

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In Figure 10, the digital portion of the TV chassis is depicted to be I^2C controlled. Some of the function blocks can be implemented with a single chip belonging to the "CLIPS" peripheral set. For example, the tuning function, as well as controlling the various analog signals, is implemented using one of the "CLIPS" peripherals. Non-volatile serial memory devices (I^2C bus compatible) as well as LCD display drivers are readily available and can be, as explained earlier, clipped to the I^2C bus.

Teletext Decoder As A Set-top Adapter

Teletext service can be incorporated in existing TV receivers through the addition of a set-top adapter. The set-top adapter concept is familiar through the use of the CATV cable converter boxes. The set-top adapter concept will offer the average consumer teletext and cable TV service as well as a remote control feature. This is true even though his or her existing TV is, at present, not remotely controlled.

Figure 11 depicts a set-top adapter block diagram. The switch can be used to inhibit the teletext feature, if necessary. On the other hand when switching at high speed, this

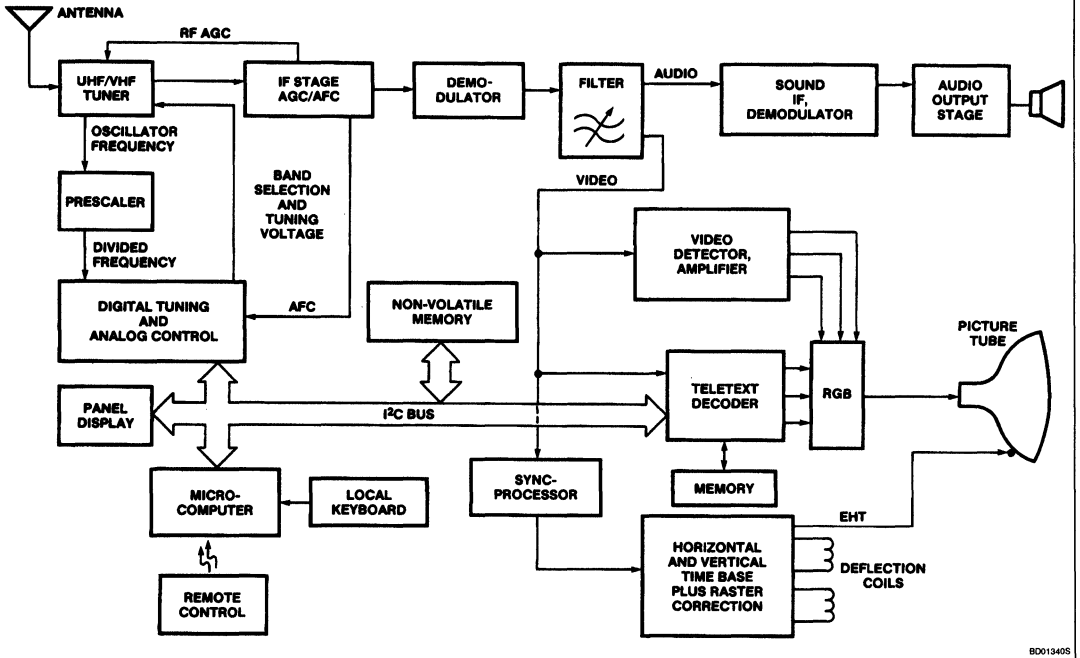

Figure 10. TV Receiver Block Diagram

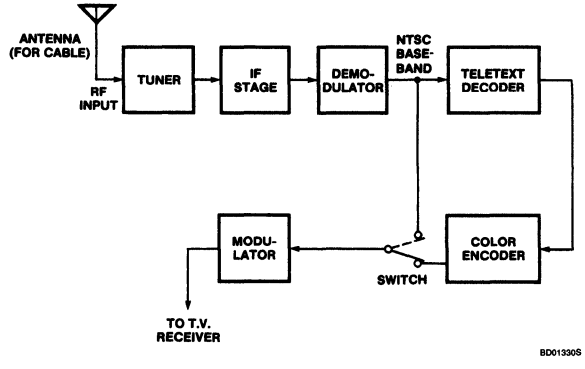

Figure 11. Teletext Set-Top Adapter

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switch can be used to implement a superimposed text over video feature.

SUMMARY

The newly introduced teletext decoder is discussed. The decoder is microcomputer controlled so it is user programmable. The teletext controller chip belongs to the diversified number of I^2C bus peripherals, known as "CLIPS", and therefore can be easily integrated in an I^2C bus controlled digital system. The new decoder performs well under poor signal conditions, it can work in either VBI or full field mode, it offers an easy, effective way to implement the "telesoftware" concept, it can acquire multi-teletext pages simultaneously resulting in a fast system response time and is capable of displaying interlaced or non-interlaced type displays. In addition to all of the above, the new teletext decoder is easy to integrate into a TV receiver or as a set-top adapter.

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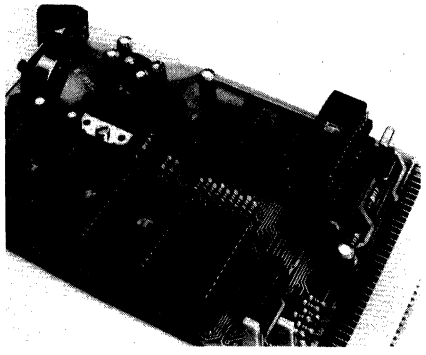
MEA8000 Voice Synthesizer: Principles and Interfacing AN119

Until now, communication between machine and man has mainly been in sign language from visual displays, audible communication being restricted to cries of alarm emitted by beepers, hooters, bells and buzzers. Voice communication has been impractical because analogue storage of speech required the use of moving parts, e.g. tape drives, which unduly prolonged the retrieval time, and digital storage of speech required handling an enormous number of bits. The development of speech synthesis techniques (Fig.1) has dramatically reduced the bit rate and the memory required for digital speech synthesis so that it is now economically feasible to open a wideband voice channel between machine and man. Such a channel is provided by our totally-digital integrated voice synthesizer MEA8000.

FEATURES OF THE MEA8000

- interfaces easily with most 8-bit microprocessors and microcomputers
- 4 kHz speech bandwidth
- can generate melodies
- bit rate from 500 to 4000 bit/s thanks to a variable speech frame duration
- synthesis occupies a very small percentage of the control processor's time
- 8th-order digital filter with three programmable formant frequencies, one fixed formant frequency and four programmable formant bandwidths
- operates with standard PROMS
- requires minimal external audio filtering
- timing: crystal-controlled internal oscillator or external TTL clock
- dynamic NMOS technology
- 30 mA current consumption (typ.) from one +5 V supply
- 24-pin plastic DIL package.



Part of a demonstration board incorporating the MEA8000 voice synthesizer and an integrated audio output stage TDA1011. The MEA8000 uses the technique of vocal tract modelling to generate quality speech from digital code. Formant synthesis, a variation of linear predictive coding (LPC), is used to control the electronic model representing the human speech production mechanism. Formant synthesis has all the advantages of LPC plus a lower bit rate than straight LPC for the same speech quality.

MEA8000 Voice Synthesizer: Principles and Interfacing AN119

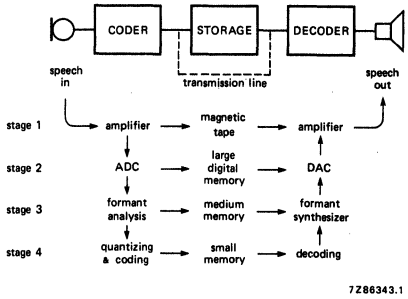


Fig.1 The development of speech storage methods. In stages 1 and 2 (waveform coding), the actual speech waveform is stored, the digital approach (stage 2) requiring a very large memory. In stages 3 and 4, a much smaller memory is required, because redundant speech information is eliminated and only the essential characteristics of the speech sounds are stored. This voice 'score' is then used to control a voice generating instrument (speech synthesizer). In stage 4, the method used in the MEA8000, formant coding allows further reduction of the required bit rate.

PRINCIPLES OF FORMANT SPEECH SYNTHESIS

Figure 2 shows the human speech mechanism. To produce speech, the lungs build up air pressure like a pump. This increasing pressure causes the initially-closed vocal cords to open. As a result, pressure drops, the vocal cords close and pressure builds up again. This mechanism excites the vocal tract with a periodic train of sawtooth pressure pulses. Sounds generated in this way, e.g. the vowels A and E, are called voiced sounds. Voiced sounds contain a lot of harmonics which fall off at about 12 dB/octave. The frequency of this periodic signal is commonly referred to as pitch.

The vocal tract can also be excited with the vocal cords always slightly open, so that air passes continuously through them, causing turbulence in the vocal tract. Sounds generated in this way, for instance the sibilants, are called unvoiced sounds.

All speech is derived from either a periodic or a noise source, i.e. a voiced or an unvoiced source. During speech, the source and its amplitude are always varying, sometimes quite rapidly.

Situated above the vocal cords are the pharyngeal, oral and nasal cavities which shape the spectrum of the generated sounds. The nasal cavity is accessed via the velum. Like all other synthesizers, the MEA8000 does not simulate the velum and the nasal cavity, so their functions are not separately represented. Consequently, for speech synthesis, the vocal tract can be analysed as if it were a tube of constant diameter, Fig.3.

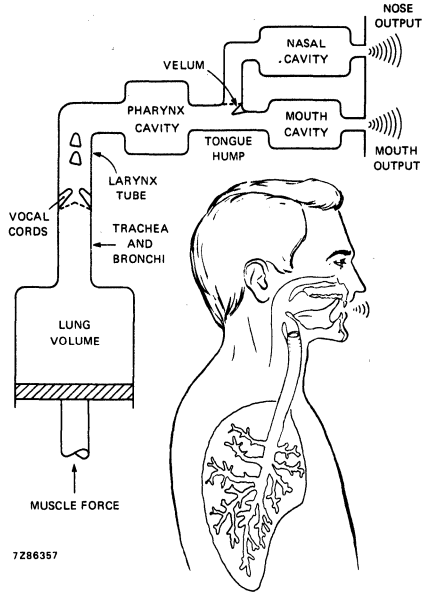


Fig.2 The human speech production mechanism.

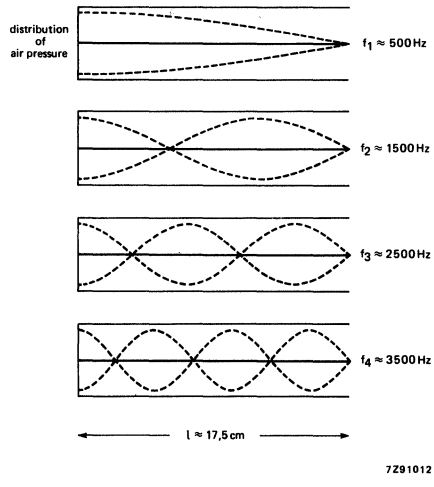


Fig.3 Resonance of a cylindrical tube.

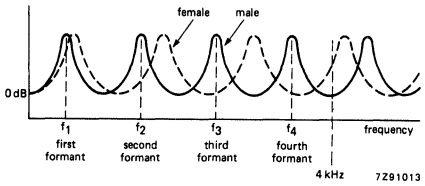


Fig.4 Frequency response of a cylindrical tube.

This tube is almost closed by the vocal cords at one end and is open at the other where mouth radiation takes place. The frequency response of the tube is characterized by a number of equally-spaced resonances at frequencies given by:

$$f(n) = \frac{340\,(2n-1)}{41} \qquad \text{for } n = 1, 2, 3, 4 \ldots$$

where 1 is the tube length in metres.

These resonant frequencies are called the formants of the vocal tract. Within a 4 kHz bandwidth, as used in the MEA8000, four formants are present for a male voice ($1 \approx 0{,}175$) and three for a female voice due to a woman's shorter vocal tract, see Figs.3 and 4.

During speech, the shape of the vocal tract is constantly changing. When an E is pronounced, for example, the pharyngeal cavity is large while the oral cavity is small. This increases the frequency of the second formant. When an A is pronounced, the situation is reversed, reducing the separation between the first and second formant, see Fig.5.

Each formant is further characterized by its bandwidth. The first two or three formants are the most important for intelligible speech; the MEA8000 generates and shapes four. The first three have adjustable frequency and adjustable bandwidth; the fourth has a fixed frequency of 3500 Hz and adjustable bandwidth.

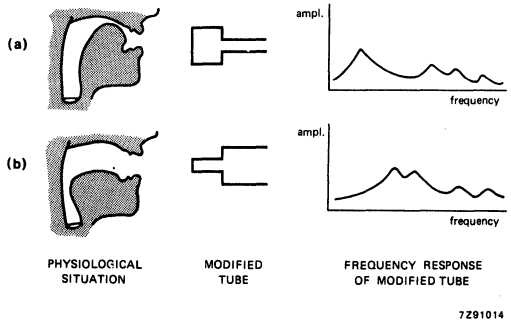


Fig.5 (a) Pronouncing E; (b) Pronouncing A.

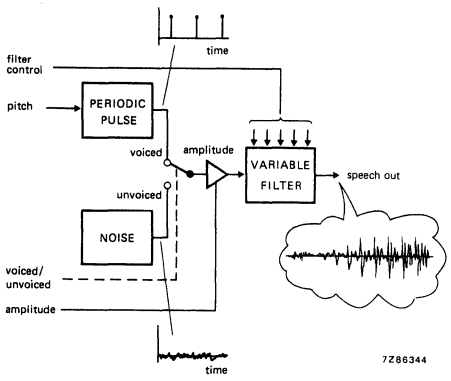


Fig.6 Simple electronic model of the human speech production mechanism.

Figure 6 shows a simplified electronic model of the human speech production mechanism (i.e. a formant synthesizer). A combination of a periodic signal, representing the pitch of the original speech, and an aperiodic signal, representing the unvoiced sound in the speech, is fed to a variable filter comprising four resonators, via an amplifier which controls the amplitude of the synthesized sound. The resonators model the sound in accordance with the formants in the original speech. Each resonator is controlled by two parameters, one for the resonant frequency and one for the bandwidth. The information required to control the synthesizer is:

– pitch	excitation source (vocal cords)
– amplitude	
– voiced/unvoiced source selector	
– filter settings	spectrum shaping (vocal tract)

A good replica of the original speech is obtained by periodic updating of this control information.

In the MEA8000, each formant is simulated by a second-order digital filter, comprising three multipliers, an adder and two delays (Fig.7). The resonant frequency and bandwidth are set by assigning different values to the multipliers A, B and C where:

$A = 1 - B - C$	for unity gain
$B = 2\sqrt{-C}\cos 2\pi f_O/f_S$	sets the formant frequency (f_O is the resonant frequency, f_S is the sampling frequency)
$C = -\exp(-2\pi b/f_S)$	sets the 3 dB bandwith b.

The filter of Fig.7 can be modified slightly to give explicit expressions for bandwidth and resonant frequency, see Fig.8. To simulate four formants, four such filters are cascaded, see Fig.9.

Figure 10 shows the complete formant synthesizer. As mentioned earlier, the jaws, tongue and lips are constantly moving during speech. In addition, the pitch and amplitude are constantly changing and the type of source can change too. This is why all input parameters controlling the synthesizer need regular updating. In the MEA8000, the standard updating period is 8 ms.

Speech parameters are determined using the LPC encoding algorithm on sampled speech data. This involves sampling the speech waveform and passing the samples through a digital analysing filter to obtain an 'inverse' voice spectrum. From this spectrum, it is possible to extract the centre frequencies and bandwidths of the four formants that represent the vocal tract resonances up to 4 kHz. From the formants, the coefficients of the digital filter in the MEA8000 which control the electronic vocal tract can be set to give faithful reproduction of the original recorded speech. The advantage of formant encoding over LPC encoding is a lower bit rate for equal speech quality.

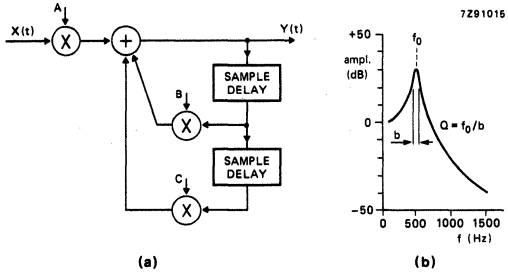


Fig.7 (a) Second-order digital filter and (b) its frequency response for: a formant centre frequency f_0 = 500 Hz (A = 0,15); a 3 dB bandwidth b = 100 Hz (B = 1,77); and a sampling frequency f_s = 8 kHz (C = −0,92).

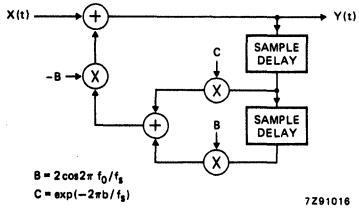


Fig.8 Modified digital filter.

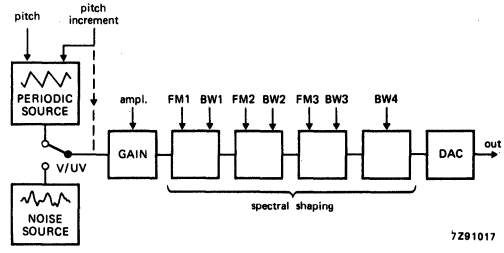


Fig.10 Formant synthesizer.

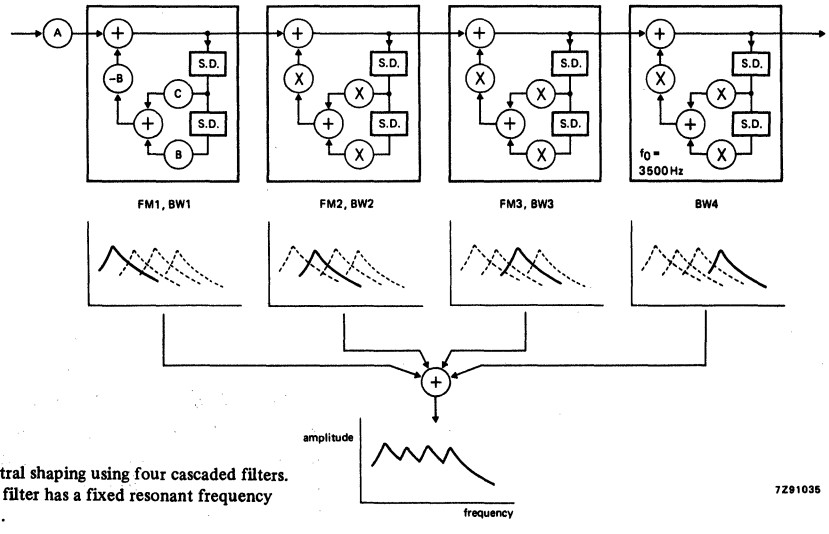


Fig.9 Spectral shaping using four cascaded filters. The fourth filter has a fixed resonant frequency of 3500 Hz.

MEA8000 BLOCK DIAGRAM

Figure 11 is a block diagram of the MEA8000. Speech codes from external ROM are sent to the synthesizer and converted to the parameters controlling the formant synthesizer. The output of the formant synthesizer is converted to an analogue signal, ready for amplification and filtering.

Formant synthesizer

The periodic and noise sources and the four formant resonators actually consist of a 16-bit multiplication and addition unit which calculates the voice samples at a rate of 8 kHz. The synthesizer is controlled by eleven parameters representing pitch, pitch increment (rate of pitch change) for voiced operation or noise selection for unvoiced operation, amplitude, four filter centre frequencies and four filter bandwidths.

A second-order digital filter is used to simulate each formant resonator. To simplify the ROM containing the filter coefficients, we have used three multipliers in the digital formant filters (see Fig.8) so that each bandwidth and each centre frequency are determined by only one filter coefficient.

Output circuit

The 16-bit samples from the formant filter bank are truncated to 11-bits before entering the interpolation and digital-to-analogue circuitry. This circuitry combines pulse-width and current modulation techniques to perform the dual functions of 8-bit DAC and linear interpolator, the latter generating seven additional samples between each 8 kHz sample from the formant filter bank. The sample rate of the DAC is therefore 64 kHz which is far above the audible frequency range, allowing the use of a simple external audio filter.

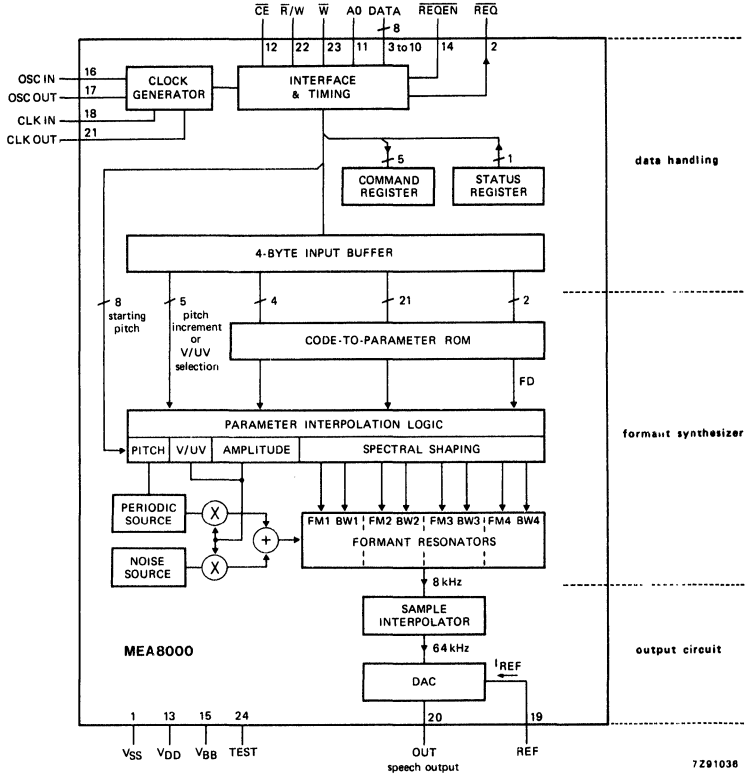


Fig.11 Block diagram of the MEA8000.

Input data handling, speech code format and parameter quantization

Since the human vocal tract is a mechanical system, its characteristics change quite slowly during the formation of voice sounds. It has been found that the speech synthesizer control parameters can be adequately represented if they are updated once every few tens of milliseconds with linear interpolation during the intervals to ensure a smooth changeover from one set of parameters to the next. In the MEA8000, the updating period (called a speech frame) can be set to 8, 16, 32 or 64 ms.

The duration of a speech frame must be long enough for it to contain sufficient speech samples to allow the speech parameters to be calculated, yet short enough to isolate changes of the parameters. Using a long speech frame when the utterance is either not changing, or changing linearly means that intelligible speech can be created using average bit rates of about 1000 bit/s.

During voice output, the speech codes from a microcomputer or external ROM are transmitted on an 8-bit data bus to the DATA port of the MEA8000 in blocks of four bytes, each block characterizing a speech frame, see Fig.12 and Table 1. Byte four contains a 5-bit pitch increment code which can be positive or negative. However, when the synthesizer starts to talk, a preliminary byte containing the full starting pitch code must be transmitted. This byte goes directly to the pitch generating circuitry via the input interface. This method of encoding pitch contributes to a lower bit rate.

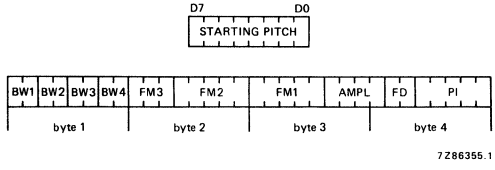


Fig.12 Format of a speech frame.

After the starting pitch code, the codes of each speech frame are shifted into a four-byte input buffer (when A0 = 0), before being translated into control parameters by the code-to-parameter ROM. The parameter interpolation logic calculates the difference between consecutive parameters and interpolates linearly between them to smooth the parameter transients. The interpolation interval is decoded using the two frame duration (FD) bits in each speech frame.

TABLE 1 Speech frame bit allocation.

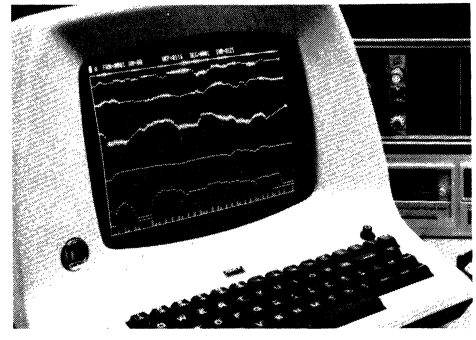
code	bits	parameter
PI	5	pitch increment or noise selection
FD	2	speech frame duration
AMPL	4	amplitude
FM1	5	frequency of 1st formant
FM2	5	frequency of 2nd formant
FM3	3	frequency of 3rd formant
BW1	2	bandwidth of 1st formant
BW2	2	bandwidth of 2nd formant
BW3	2	bandwidth of 3rd formant
BW4	2	bandwidth of 4th formant

FM4, the frequency of the fourth formant, is fixed.

MEA8000 EDITING SYSTEM

During speech encoding, digitized speech samples from a recorded voice are analysed by a computer to produce speech codes which, after manual editing, are stored in PROM. These codes are applied to the synthesizer which translates them into the pitch, amplitude, voiced/unvoiced source and filter control information required to reproduce the original speech.

In order to obtain the lowest possible bit rate and the highest possible speech quality, any voice synthesizer needs an editing system. Present editing systems for both waveform analysis and LPC synthesizers have the severe disadvantage that the speech to be edited is usually displayed on a screen in the form of complex tables of coded parameters. It is a specialized task to edit these parameters, because the editor must know what the codes mean before he can start. In our editing system, the synthesized speech is displayed on a screen as a waveform instead of as codes. Speech editing is so simplified by this method that the entire speech editing process be learnt in a day. At present, speech encoding and editing for the MEA8000 is a service that we provide. A stand-alone speech editing system will be included in a popular type of personal computer available in autumn 1983.



The pitch increment code goes directly from the buffer to the parameter interpolation logic. One of the pitch increment codes, 10000_2 (16_{10}), does not change the pitch, and is used to select the voiced or unvoiced source.

The outputs of the interpolation logic control the aforementioned synthesizer functions of pitch, amplitude, voiced/unvoiced source selection and filter formants.

The speech code parameters are shown in Table 2. Fig.13 shows the beginning of a stream of speech codes for the utterance 's'. The starting pitch is 98 Hz (represented by H31) and 104 ms of speech are represented by these codes, since the FD bits indicate speech frames of 32, 64 and 8 ms. The average bit rate of this utterance would therefore be about 1000 bit/s. Note, a common speech frame of 8 ms is used initially, this being changed if necessary during editing.

TABLE 2 Speech code parameters when using a clock frequency of 3,84 MHz.

decimal code	hex. code	FD (ms)	pitch (Hz)	PI (Hz/8 ms)	amplitude	FM1 (Hz)	FM2 (Hz)	FM3 (Hz)	BW (Hz)
0	00	8	0	0	0	150	440	1179	726
1	01	16	2	1	0,008	162	466	1337	309
2	02	32	4	2	0,011	174	494	1528	125
3	03	64	6	3	0,016	188	523	1761	50
4	04		8	4	0,022	202	554	2047	
5	05		10	5	0,031	217	587	2400	
6	06		12	6	0,044	233	622	2842	
7	07		14	7	0,062	250	659	3400	
8	08		16	8	0,088	267	698		
9	09		18	9	0,125	286	740		
10	0A		20	10	0,177	305	784		
11	0B		22	11	0,250	325	830		
12	0C		24	12	0,354	346	880		
13	0D		26	13	0,500	368	932		
14	0E		28	14	0,707	391	988		
15	0F		30	15	1,00	415	1047		
16	10		32	noise		440	1110		
17	11		34	−15		466	1179		
18	12		36	−14		494	1254		
19	13		38	−13		523	1337		
20	14		40	−12		554	1428		
21	15		42	−11		587	1528		
22	16		44	−10		622	1639		
23	17		46	−9		659	1761		
24	18		48	−8		698	1897		
25	19		50	−7		740	2047		
26	1A		52	−6		784	2214		
27	1B		54	−5		830	2400		
28	1C		56	−4		880	2609		
29	1D		58	−3		932	2842		
30	1E		60	−2		988	3105		
31	1F		62	−1		1047	3400		
⋮	⋮		⋮						
49	31		98						
⋮	⋮		⋮						
255	FF		510						

The frequency of FM4 is fixed at 3500 Hz. The BW (bandwidth) column applies to all four filters. For exact values of pitch and pitch increment, multiply the values given above by 1,024.

starting pitch	byte 1	byte 2	byte 3	byte 4	speech frame
31	05	D2	FE	50	1
	0A	D7	FE	70	2
	1A	D8	F5	90	3

(a)

Fig.13 (a) Beginning of a stream of speech codes in hexadecimal notation; (b) binary representation of the codes shown in (a); (c) parameter values of the speech codes in (a) and (b).

byte 1				byte 2		byte 3		byte 4			speech frame
BW1	BW2	BW3	BW4	FM3	FM2	FM1	AMPL.	FD	PI		
00	00	01	01	110	10010	11111	110	0	10	10000	1
00	00	10	10	110	10111	11111	110	0	11	10000	2
00	01	10	10	110	11000	11110	101	1	00	10000	3

(b)

	BW1	BW2	BW3	BW4	FM3	FM2	FM1	AMPL.	FD	PI	speech frame
	726	726	309	309	2842	1254	1047	0,354	32	noise	1
	726	726	125	125	2842	1761	1047	0,354	64	noise	2
	726	309	125	125	2842	1897	988	0,250	8	noise	3

(c)

CONTROL

Control inputs

The inputs $\overline{CE}$, $\overline{W}$, $\overline{R}/W$ and A0, together with the $\overline{REQ}$ output pin which signals a request for speech codes, are used to control the transmission of codes to the synthesizer and to set the synthesizer's operating mode.

The functions of the control inputs are:

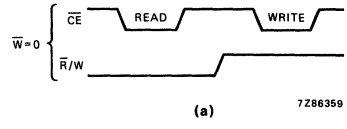
$\overline{CE}$ enables the circuit

$\overline{W}$ controls the writing of data

$\overline{R}/W$ controls the reading/writing of data

A0 when A0 = 0, the input buffer is addressed,
when A0 = 1, the command register is addressed.

Table 3 is the control input truth table. The control inputs can be used in many combinations to allow simple interfacing of the MEA8000 to a variety of host processors. Figure 14 shows two ways of interfacing the MEA8000 to most popular microcomputers. Read and write timing are shown in Figs.15 and 16 and Table 4.



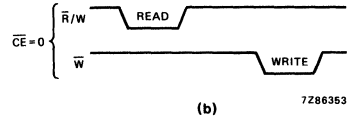


Fig.14 (a) Chip enable ($\overline{CE}$) used as a read or write strobe; (b) separate read and write strobes.

TABLE 3 Control input truth table.

$\overline{CE}$	$\overline{W}$	R/$\overline{W}$	A0	operation
0	0	1	0	write data
0	0	1	1	write command
0	X	0	X	read status
0	1	1	X	three-state data bus
1	X	X	X	

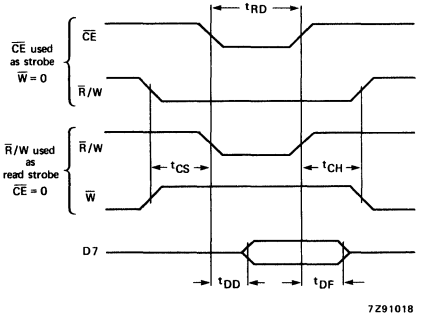


Fig.15 Read timing.

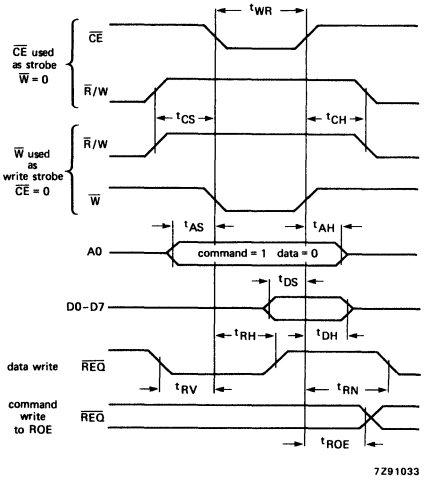


Fig.16 Write timing.

TABLE 4 Timing characteristics[1] (Figs.15 and 16).

		min.	*max.*	
write enable	t_{WR}	200	–	ns
address set-up	t_{AS}	30	–	ns
address hold	t_{AH}	30	–	ns
data set-up for write	t_{DS}	150	–	ns
data hold for write	t_{DH}	30	–	ns
request hold[2])	t_{RH}	–	350	ns
request next[3]) (3,84 MHz clock)	t_{RN}	–	3	μs
read enable	t_{RD}	200	–	ns
data delay for read[4])	t_{DD}	–	150	ns
data floating for read[4])	t_{DF}	–	150	ns
request valid before write	t_{RV}	0	–	ns
request output enable response	t_{ROE}	–	350	ns
control set-up	t_{CS}	–	20	ns
control hold	t_{CH}	–	20	ns

[1]) Timing reference level is 1,5 V.

[2]) $\overline{REQ}$ is an open drain output, requiring an external pull-up. The time stated is that to reach 2,0 V via a 3,3 kΩ and 50 pF pull-up connected to 5 V.

[3]) Between two data write operations of a speech frame.

[4]) Levels greater than 2,0 V for a 1, or less than 0,8 V for a 0 are reached with a load of one TTL input and 50 pF.

Command register and status register

The contents of the command register (command word) determines whether the synthesizer is silent or active (operating mode) and the procedure that will be followed when the supply of speech codes is intermittent. It also determines how the contents of the status register, i.e. the data request bit (REQ) used to request more data, will be broadcast. Table 5 gives the bit allocation of the command register. It is written into via data lines D4 to D0 when $\overline{CE} = \overline{W} = 0$ and A0 = R/$\overline{W}$ = 1.

The request bit REQ

REQ is stored in the status register and signals a request for the next byte of speech code, or the starting pitch byte if a STOP command has just been received. The request for data can be broadcast in two ways:

– on the $\overline{REQ}$ pin,

– on data port D7.

The $\overline{REQ}$ pin can be enabled in hardware or software. The hardware method is to connect $\overline{REQEN}$ (pin 14) to ground. The software method is to set ROE in the command register to a 1 (and to hold $\overline{REQEN}$ high). The $\overline{REQ}$ pin can be connected to the control processor's interrupt input or polled.

The status bit REQ can also be broadcast to the control processor via bidirectional port D7, D7 being read when $\overline{CE} = \overline{R/W} = 0$ (see Table 3).

TABLE 5 Command word bit allocation and truth table.

D4 STOP	D3 CONT enable	D2 CONT	D1 ROE enable	D0 ROE
0 = no action	0	0 = no action	0	0 = no action
1 = STOP	0	1 = no action	0	1 = no action
	1	0 = SLOW STOP procedure	1	0 = disable $\overline{REQ}$
	1	1 = CONTINUOUS procedure	1	1 = enable $\overline{REQ}$

D7, D6 and D5 are not used;
ROE = request output enable.

After power-on reset, the command register bits CONT and ROE will both be zero since power-on corresponds to the command word XXX11010. Therefore, the synthesizer will be in the SLOW STOP procedure.

OPERATING MODES AND PROCEDURE DURING INTERMITTENT CODE SUPPLY

The operating modes (Fig.17) are:

– the SILENT mode

– the ACTIVE mode.

The SILENT mode, characterized by a silent output and the status REQ bit high, is entered after a power-on reset or reception of a STOP command, or at the end of a SLOW STOP procedure. The STOP command mutes the synthesizer immediately. The active mode is re-entered after a starting pitch byte has been received.

In the ACTIVE mode, speech codes are synthesized. During the synthesis of one speech frame, all four bytes of the next frame must be received. If this is not the case, one of two procedures is followed depending on the CONT bit of the command word:

– the CONTINUOUS procedure (CONT = 1)

– the SLOW STOP procedure (CONT = 0).

The CONTINUOUS procedure causes the synthesizer to repeat the last speech frame indefinitely until all the codes of the next frame have been received or until a STOP command is received. When generating melodies, this procedure can be used to advantage.

The SLOW STOP procedure causes the synthesizer to enter the SILENT mode by repeating the last frame once, decreasing amplitude to zero and then going silent.

Figure 18 shows the audio output in the case of intermittent code supply for the CONTINUOUS and SLOW STOP procedure.

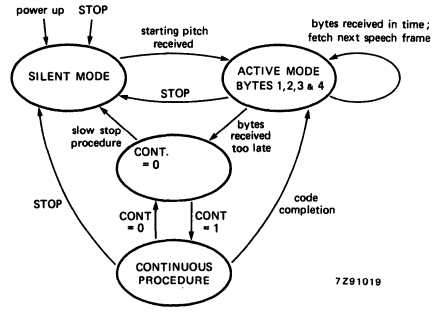


Fig.17 Operating modes and procedures.

Figure 19 shows the speech codes for the utterance 's' again, plus the audio output during the utterance. The timing for the first frame is shown in Fig.20. Subsequent frames have identical timing, with the exception of the starting pitch. The utterance starts from the SILENT mode, in this case after a STOP command has been written to the synthesizer, so $\overline{REQ}$ is low. After the starting pitch byte has been written, $\overline{REQ}$ remains high for up to 8 ms, then goes low indicating that the first byte of speech codes may be sent. To write data to the input buffer, $\overline{CE}$ is first brought low, data being written on the rising edge of $\overline{CE}$. After a byte has been received, $\overline{REQ}$ remains high for about 2 μs between the first and second, second and third, and third and fourth bytes. After the fourth byte has been written, $\overline{REQ}$ remains high for 8 to 64 ms during which time the synthesizer sets the speech parameters of the first frame according to the codes 05, D2, FE and 50.

Preparing the first frame is different to preparing those that follow, because, except for the amplitude which starts from zero and reaches its correct value at the end of the frame, the value of each parameter is set before the first frame is spoken. For subsequent frames, the values of all parameters are only reached at the end of the frame owing to the internal linear parameter interpolation.

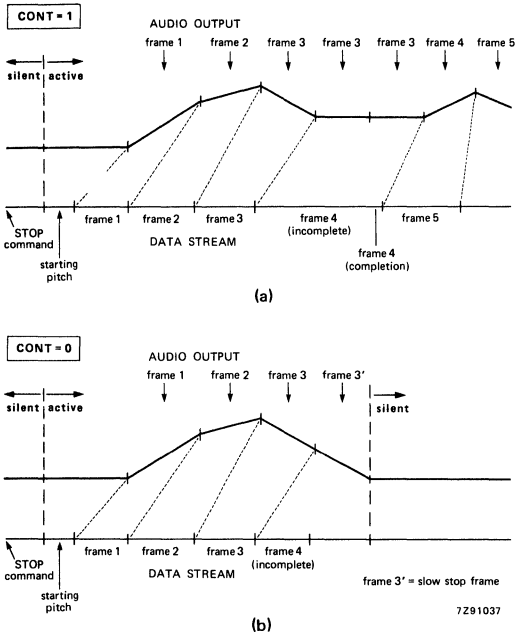


Fig.18 Audio output in the case of intermittent code supply
(a) for the CONTINUOUS procedure
(b) for the SLOW STOP procedure.

At t_2 (Fig.19), the synthesizer starts speaking, $\overline{REQ}$ going low at the same time, requesting the next speech codes. The duration of the first speech frame is 32 ms (the FD bits being 10_2) during which the four bytes of the second frame must be received.

At t_3, pronounciation of the first frame ends, the synthesizer starts pronouncing the second and, by means of $\overline{REQ}$, requests the codes of the third. In this example, 64 ms are available to receive the third frame, since that is the time taken to pronounce the second.

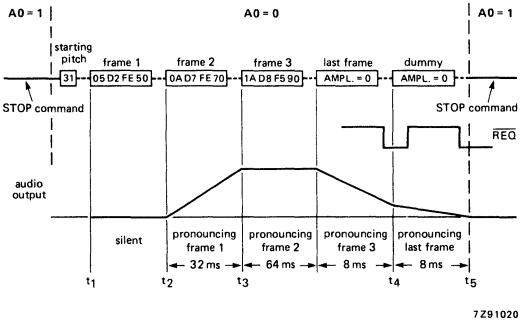


Fig.19 A four frame utterance in which a dummy frame is used to ensure that pronounciation of the last frame is not curtailed by the STOP command.

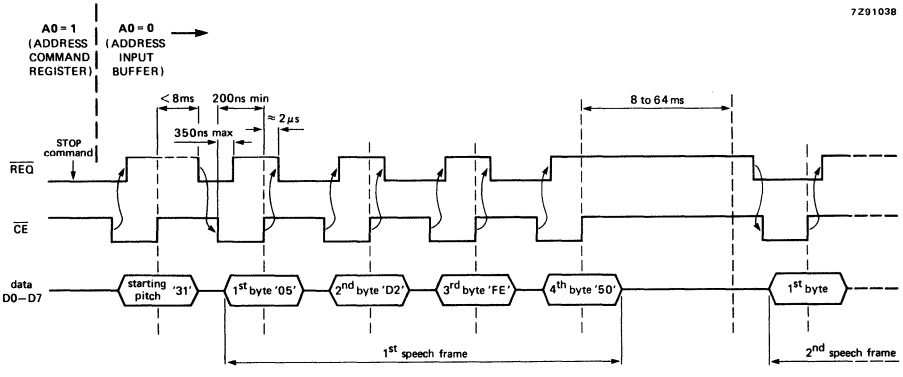


Fig.20 Timing of the first frame of Fig.19 in detail. Data is written on the rising edge of $\overline{CE}$. Polling of $\overline{REQ}$ is unnecessary since it returns to the high state within 3 µs of receiving each byte. The trailing edge of $\overline{REQ}$ is good timing reference, occurring at multiples of 8 ms.

At t_4, the synthesizer starts pronouncing the last frame. Since the utterance has to be terminated by a STOP command so that the new starting pitch of the next utterance can be received, the microprocessor has to determine when STOP may be written without shortening the last frame. A practical way of doing this is to provide a dummy frame when $\overline{REQ}$ goes low at t_4, the amplitude bits of the dummy frame being set to zero. After the dummy frame has been received, $\overline{REQ}$ goes low again at t_5 marking the end of speech output and STOP may be written.

INTERPOLATION, D/A CONVERSION AND SPECTRAL RESPONSE

The 8 kHz samples from the digital filters are fed to a linear interpolator which increases the effective sampling rate to 64 kHz, simplifying analogue post filtering.

The 8-bit digital samples are converted into a series of synthesized speech waveform increments by the D/A converter shown in Fig.21. The converter consists of two parallel-connected open-drain current sinks of amplitude I and 16I and an external capacitor. Current I equals the d.c. current injected into the REF pin of the MEA8000. When all eight bits of the digital sample are zero, both current sinks are off and capacitor C charges through resistor R. For other digital samples, one or both sinks are activated and three capacitor discharge currents can be defined (I, 16I and 17I). To ensure that the charge on the capacitor is well-defined before each digital sample is converted, both sinks are turned off for the last two clocks of each 20-clock sampling period and on the first three, leaving 15 clocks per sampling period to define each analogue increment.

The current sinks are switched on for the number of clocks indicated by the two nibbles of each 8-bit sample. The least significant nibble indicates the time for which the capacitor discharges into the I current sink, and the most significant nibble that for which it discharges into the 16I sink, see Fig.22. Each nibble can determine discharge durations from 0 clocks (both sinks off for whole sampling period) to 15 clocks. The sixteen possible discharge durations of the 16I sink combined with the sixteen of the I sink allow 256 average voltage levels (16 x 16) to be defined for each increment of the speech waveform.

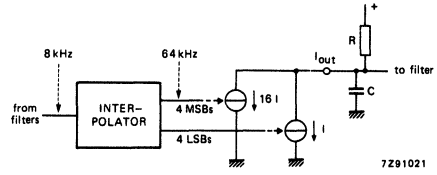


Fig.21 Output circuit.

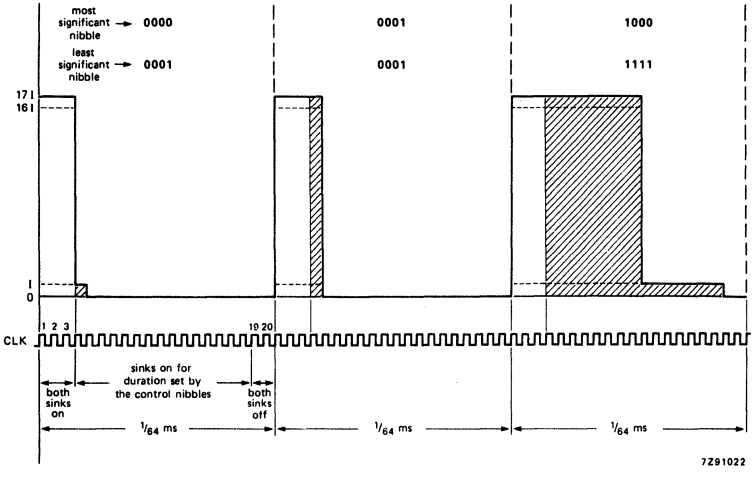


Fig.22 Output current pulses from the MEA8000 for three samples. Two 4-bit codes are used to produce a possible 256 average charge levels of which three are shown here shaded.

Note, to compensate for the fall-off in the frequency response due to the linear interpolation, an analogue post filter for the MEA8000 should have an $(x/\sin x)^2$ correction, Fig.23. The interpolation can be regarded as a convolution of the 8 kHz samples with a triangular non-causal impulse response, see Fig.24.

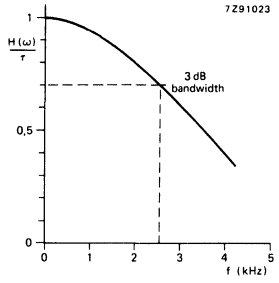


Fig.23 $H(\omega)/\tau$. Frequency response of the MEA8000. $1/\tau$ is the sampling frequency.

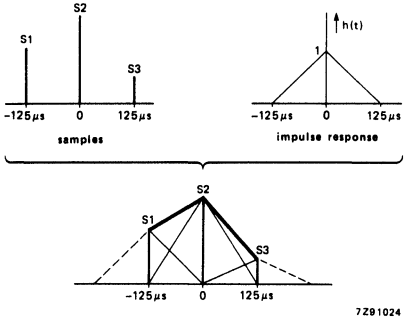


Fig.24 Convolution of 8 kHz samples with a triangular non-causal impulse response.

AUDIO OUTPUT STAGE

Figure 25 shows an integrated 6 W audio output stage for the MEA8000 and filter which performs $(x/\sin x)^2$ correction as well as bandlimiting. The best voice quality is obtained with an audio filter having the transfer characteristic shown in Fig.26 and Table 6. The characteristic of the actual filter is a good approximation of the optimum.

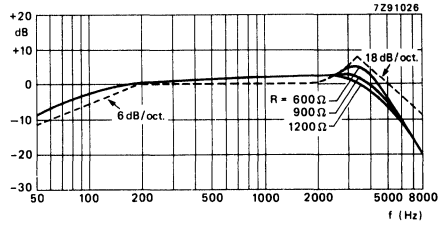


Fig.26 Output filter transfer characteristic.
--- for optimum voice quality;
—— characteristic of the filter shown in Fig.25.

The first section of the filter integrates the pulses from the output of the MEA8000 and cuts off at about 3400 Hz. The second section is an LCR circuit with resonant frequency 3400 Hz which compensates for the $(x/\sin x)^2$ distortion. If less high frequency compensation is required, the Q of the resonant circuit ($\omega L/R$) can be decreased by connecting a resistor in series with the inductor. The 600 Ω resistance R is the winding resistance of the 100 mH inductor. The third section is a first order low-pass section which removes any d.c. components.

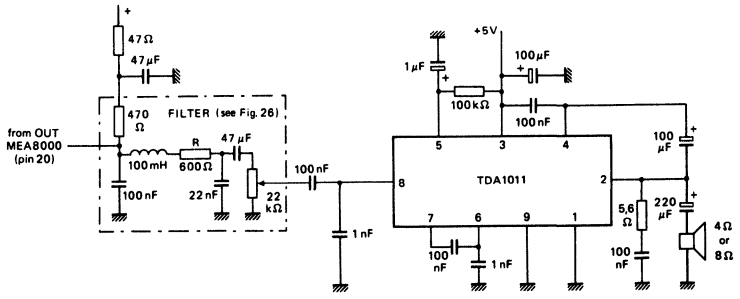


Fig.25 Audio output stage.

TABLE 6 $(x/\sin x)^2$ correction factors for the audio output filter.

freq. (Hz)	$\left(\frac{\sin x}{x}\right)^2$	$20 \log \left(\frac{x}{\sin x}\right)^2$ (dB)
0	1	0
400	0,99	0,09
800	0,97	0,26
1200	0,93	0,63
1600	0,88	1,11
2000	0,81	1,83
2400	0,74	2,62
2800	0,66	3,61
3200	0,57	4,88
3600	0,49	6,20
4000	0,41	7,74

Table 7 shows a header and a starting pitch byte followed by twenty-one four-byte speech frames for synthesizing the word 'stop'.

Usually, more than one speech file will be stored in a ROM. An index is made by listening the 2-byte starting addresses of each file at the beginning of the ROM. The end of the index is indicated by the bytes FF FF. Figure 27 shows examples of ROM mapping.

SOFTWARE

ROM mapping

The external ROM that stores the speech codes of an utterance or a word (called a speech file) also stores the starting pitch byte and the file header. The header comprises three bytes, two that indicate the number of bytes in the file and one that allows additional data to be encoded for each file.

Speech output routine

This routine controls the transmission of speech codes to the synthesizer. Figure 28 shows the flow chart.

Each utterance is terminated with the STOP command.

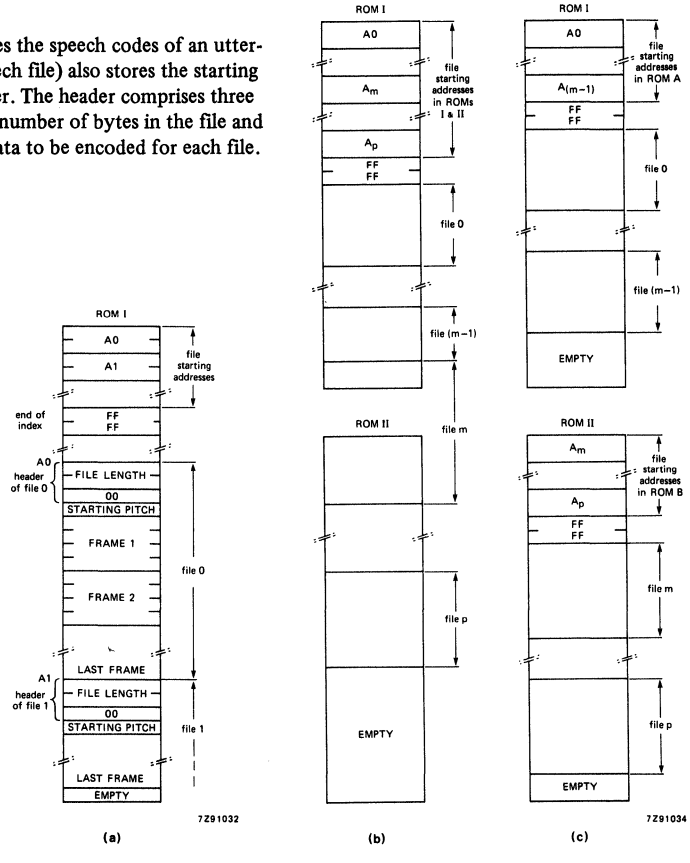


Fig.27 Examples of ROM memory mapping; (a) vocabulary in one ROM, (b) and (c) vocabulary in two ROMs.

TABLE 7 Hexadecimal speech codes for the word 'stop'.

												——(a)——			(b)	
												00	58	00	31	
05	D2	FE	50	0A	D7	FE	70	1A	D8	F5	90	1A	D8	F0	10	Speech codes
44	D9	F8	70	48	DA	FF	B0	08	DB	FF	90	46	DB	FF	02	
79	D1	67	0F	AA	CF	9F	7E	BB	AD	96	C1	96	CC	85	BE	
46	8F	B4	99	55	D7	24	12	45	B6	13	9E	05	B5	A3	1F	
05	B5	A0	00	2A	B3	B0	70	59	B3	E5	B0	2A	B2	DD	B0	
19	B2	ED	90													

(a) header containing byte count of word code file for microcomputer.
(b) starting pitch.

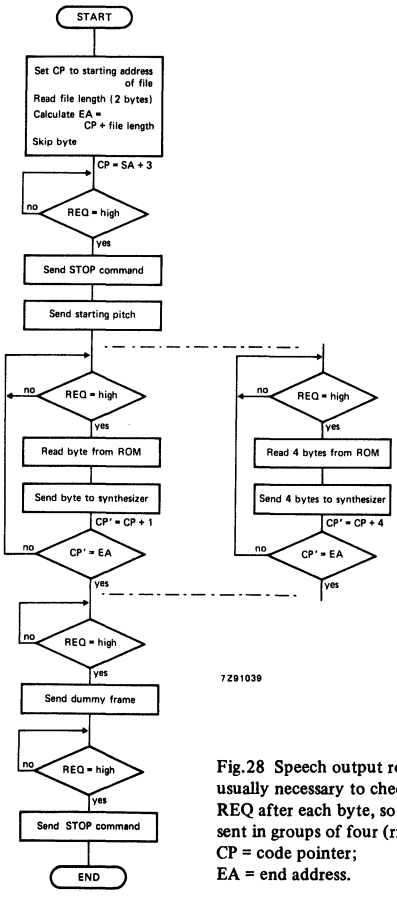


Fig.28 Speech output routine. It is not usually necessary to check the status of REQ after each byte, so bytes can be sent in groups of four (right).
CP = code pointer;
EA = end address.

A STOP command should be given when the status bit REQ is high. It can also be useful to send a STOP command at the beginning of an utterance, e.g. if a new frame is to override the present one.

INTERFACING

System timing is set using clock pulses from an internal oscillator controlled by a crystal connected between OSC-IN and OSC-OUT. The synthesizer can also be driven by an external clock via CLK IN. Pulses at one third of the clock frequency are available at CLK OUT. Figure 29 shows examples of oscillator/clock configurations.

Figure 30 shows how the MEA8000 can be interfaced to different control devices.

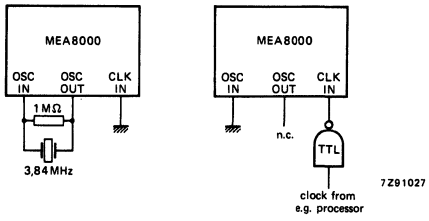
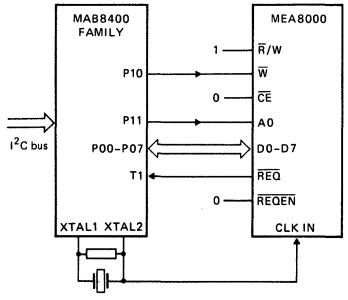


Fig.29 Oscillator/clock configurations.

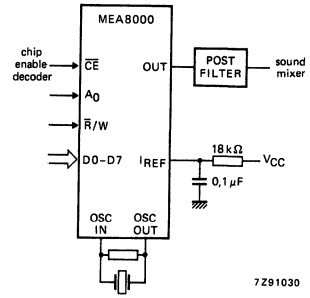
REFERENCE

1. 'Higher quality synthesised speech through fast and easy editing', Electronic Components and Applications, Vol.4 No.4, Aug. 1982, p. 241.

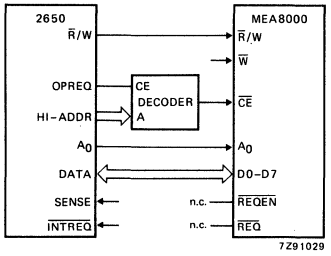
MEA8000 Voice Synthesizer: Principles and Interfacing AN119



(a)



(c)



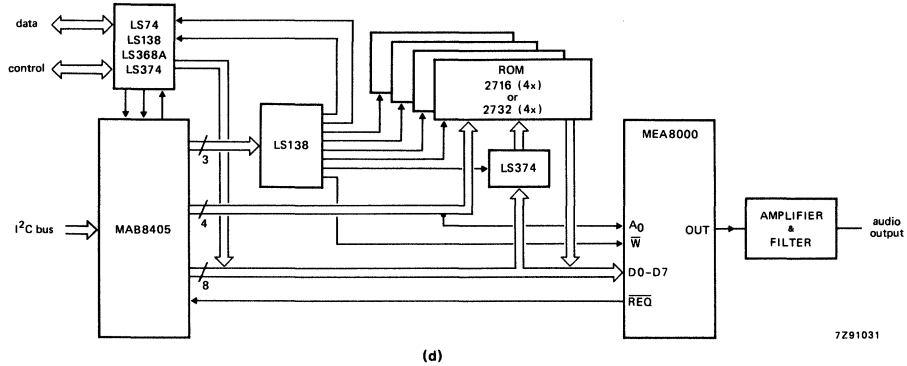
(b)

Fig.30 (a) Small vocabulary system. Status is tested on the T1 input via the $\overline{REQ}$ signal. $\overline{REQ}$ is enabled via $\overline{REQEN}$ = 0. The MAB8400 microcomputer holds both the program and the speech codes.

(b) Small vocabulary system. Status is tested via data port D7. $\overline{R}$/W pins are connected so that the REQ signal can be read on D7. The program and the speech codes are in external ROM.

(c) Adding a voice output to an existing video game. In addition to the hardware shown, the game cartridge ROM needs to be increased by about 125 bytes for the speech output routine. The speech codes can also be put in the same ROM. When used with an interrupt routine, only 1% of the processor's time is used.

(d) General system for applications in card systems, small-volume large-vocabularly systems. Serial or parallel input data. Status is read via $\overline{REQ}$.



(d)

Wideband FM Composite Video Fiber Optic Link AN146

INTRODUCTION

A low cost yet high performance, color, composite video fiber optic link for short-haul applications can easily be built using readily available off-the-shelf I.C.'s and optoelectronic devices. Also, all the necessary tools and hardware for interfacing the fiber to the electronics are available in kit form. This adds further simplicity and lower cost to the construction of the finished design and cancels the need to obtain factory installed terminations.

OPERATION

Starting at the transmitter end (Figure 1), the system begins with an NE592 differential video amplifier. The amplifier receives the composite video signal and then differentially drives the voltage controlled oscillator (VCO) of an NE564 phase locked loop (PLL). This is done through the output pins of the PLL phase comparator. The VCO is driven directly to avoid the input limiter and phase detector of the NE564. This method of operation opens up a number of applications for the NE564 that were previously impossible. The loop, in this case, is configured as a frequency modulator with a center of 30MHz and a deviation of ±10MHz. From here, the modulated signal is fed to an NE522 high speed comparator with an open collector output. The comparator boosts the signal in order to drive a high power aluminum gallium arsenide infrared (810μm) LED which has a typical rise time of 3ns.

The composite video is essentially sent at a 60 Mb/s data rate over the fiber and is received by an AlGaAs PIN photodiode. The light is converted to a current by the diode and is amplified and changed to a voltage by the NE5539 op amp in a transimpedance configuration. The very high speed response (600V/μs) and wide bandwidth (350MHz unity gain) makes this device ideally suited for high performance optical links. Compensation components and their values are also shown in Figure 1 to make the NE5539 unconditionally stable because it is not internally compensated. The second NE5539 is a voltage gain stage and is optional depending upon the attenuation in the fiber or its length. Immediately following is another NE564 PLL set up as an FM demodulator which is AC coupled to the last NE5539 op amp. This third NE5539 acts as an amplifier and buffer that drives 75 ohm cable to a video monitor.

TEST

Tests using 30 meters of 125μm glass fiber show the chrominance S/N ratio of an EIA color bar test signal to be approximately 40dB. This S/N ratio can be improved if an additional filter is added to the circuit. The primary noise source is the 30MHz modulation frequency. To attenuate this noise and other high frequencies effectively, a third order low pass Chebyshev filter with a cutoff of 3.58MHz is constructed around the last NE5539 (Figure 2). This increases the S/N ratio significantly. Comparison photos taken from a spectrum analyzer are shown in Figure 3.

Caution should be exercised so as not to roll off too much of the 3.58MHz chrominance signal. A tradeoff between noise and color signal should be considered. Higher order filters using the NE5539 will sharpen the roll off considerably so that the color amplitude will not be affected. A comparison of input and output using the EIA color bar test signal is shown in Figure 4. As can be seen, there is excellent reproduction of the original signal and little overall phase shift in the vector plot. Also, using a 5 step staircase signal, differential gain and phase error measurements of the entire system are 1% and 0.5° respectively.

SYNOPSIS

The main intent is to show how to build a color video transmission system. But it may be possible to transmit other analog or digital signals along with the video since the circuit shown only utilizes the 20 to 40MHz band. These signals can be sent using the lower frequencies (i.e., data via FSK, voice channels, etc.). Additional circuitry can be used to multiplex the signals electronically after the first PLL, and bandpass filters utilized before the second PLL, on the receiver side, to separate and then demodulate them.

The circuit in Figure 1 can be made very inexpensively. The tools and connectors as well as instructions for constructing a very reliable fiber link are from Amp Inc. kit number 227385. The fiber used is ITT number T-3000, and the IR LED and photodiode are Motorola part numbers MFOE1202 and MFOD1100 respectively.

The circuits should be laid out on a double sided copper clad PC board with all power supply pins decoupled as shown. Care should be exercised in shielding both the PIN photodiode and the first NE5539 in the receiver end to avoid pick up and amplification of unwanted noise. The RF chokes are Ferroxcube part number VK200-10-3B. The I.C.'s are all available from Signetics.

Written by: Thomas DeLurio

Wideband FM Composite Video Fiber Optic Link AN146

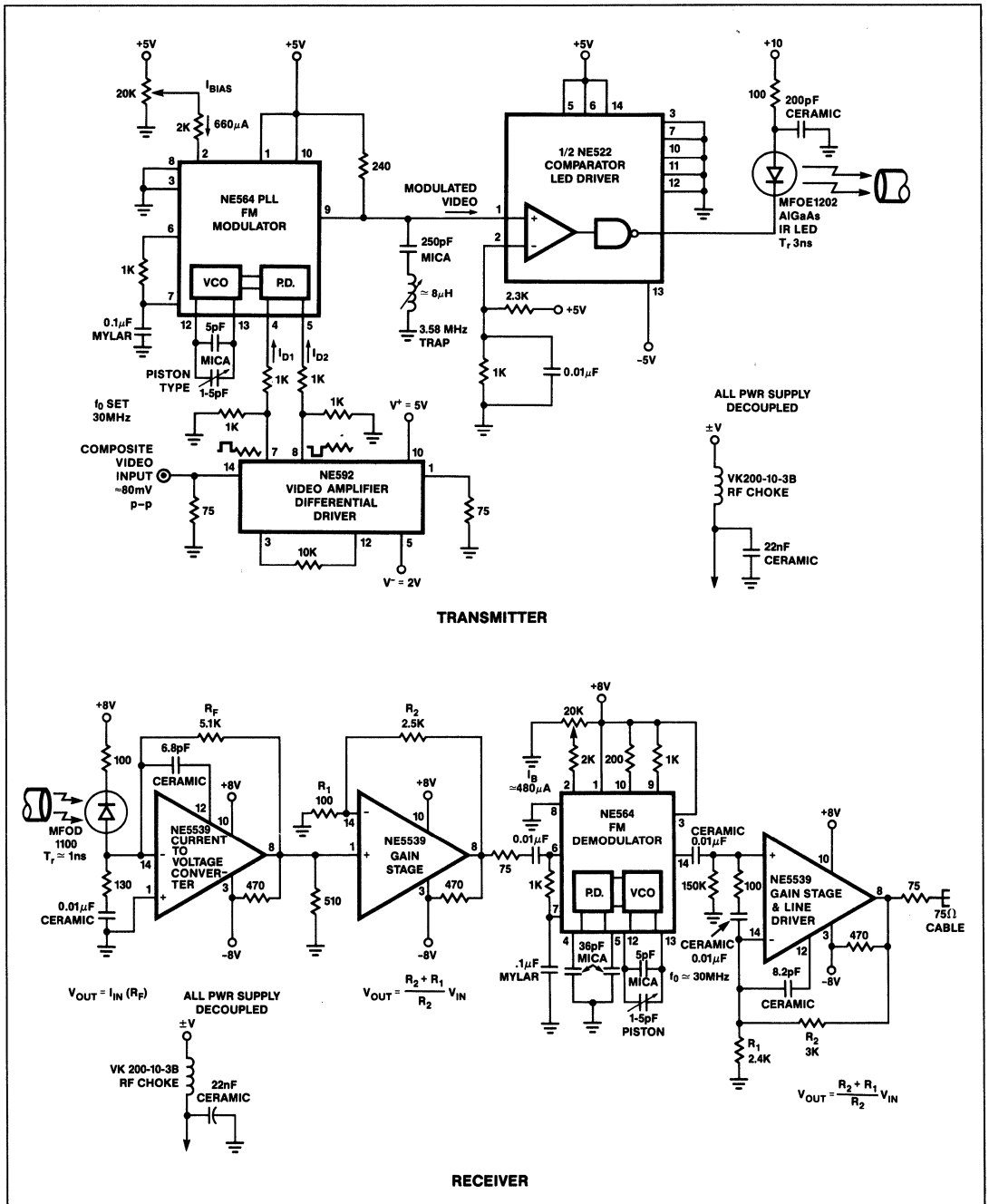


Figure 1. Fiber Optic Video System

Wideband FM Composite Video Fiber Optic Link AN146

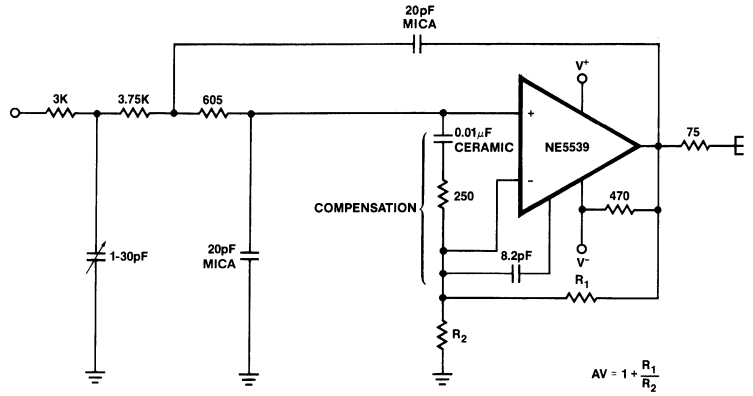
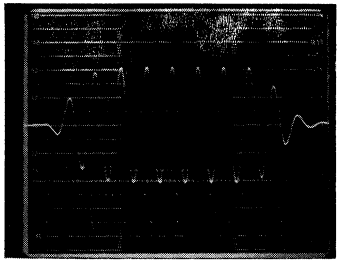
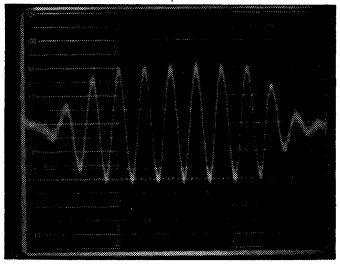


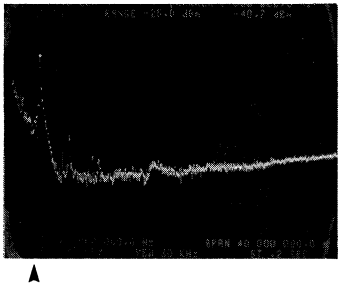
Figure 2. NE5539 CHEBYSHEV Low Pass Filter—3.58MHz Cutoff



INPUT 3.58MHz BURST

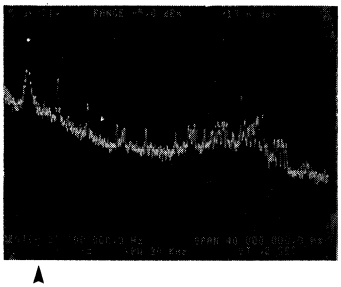


OUTPUT 3.58MHz BURST AFTER LOW PASS FILTER



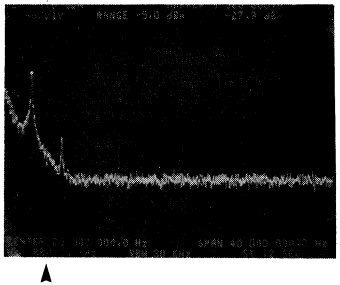
3.58MHz

INPUT SIGNAL SPECTRUM 0 TO 40MHz



3.58MHz

OUTPUT BEFORE FILTER

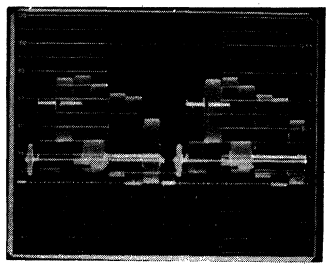


3.58MHz

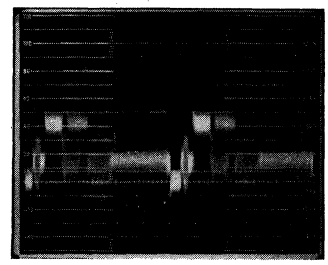
OUTPUT AFTER FILTER

Figure 3. Noise Tests

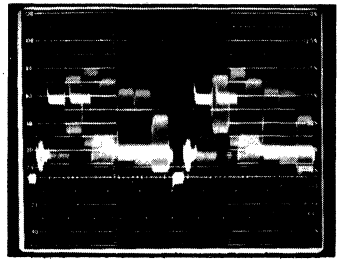
9



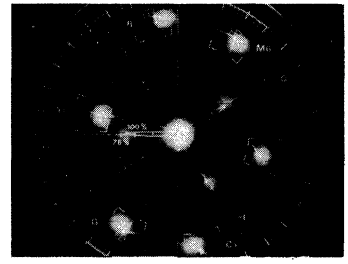
INPUT



OUTPUT



OUTPUT AFTER FILTER



INPUT/OUTPUT VECTORS AFTER FILTER

Figure 4. Input/Output Test Signals Not to Scale

Audio Amplifier with TDA1013A

AN148

Author: D. Udo

ABSTRACT

The 9 lead SOT 110 B encapsulated TDA1013A is an audio power amplifier that has a DC volume control on board. The device is designed for audio amplifier applications in TV sound channels.

At a supply voltage of 18V, the output power is about 4.4W into an 8Ω loudspeaker.

The gain control range is > 80dB with a DC control voltage from 8 to 3.5V.

Some basic information of the TDA 1013A is dealt with in this application note. Detailed performance properties are given for an 18V into 8Ω application.

INTRODUCTION

The TDA1013A has two functions: a DC volume control and audio power amplifier.

Some performance characterisitcs are:

- Supply voltage range 15 – 35V
- Max. repetitive peak current 1.5A
- Max. non-repetitive peak current 3A
- $R_{th\ j\text{-}tab}$ 9K/W
- $R_{th\ j\text{-}a}$ 45K/W
- Input imedance (pins 5 and 8) > 100kΩ
- Output impedance (pin 6) 200Ω (typ.)
- Voltage gain DC control part (pins 8 to 6) 7dB
- Voltage gain power amplifier (pins 5 to 2) 30dB

APPLICATION CIRCUIT

The complete application circuit is given in Fig. 1. With high input inpedance, C_9 is necessary to filter out RF input interferences. R_3 in combination with C_5 is used to limit the a.f. frequency bandwidth. The 470μF power supply decoupling capacitor is C_{10}.

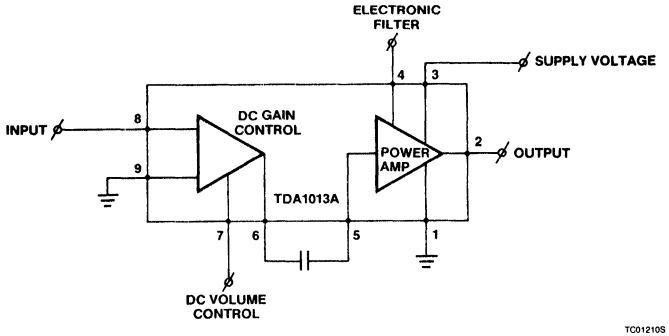


Figure 1

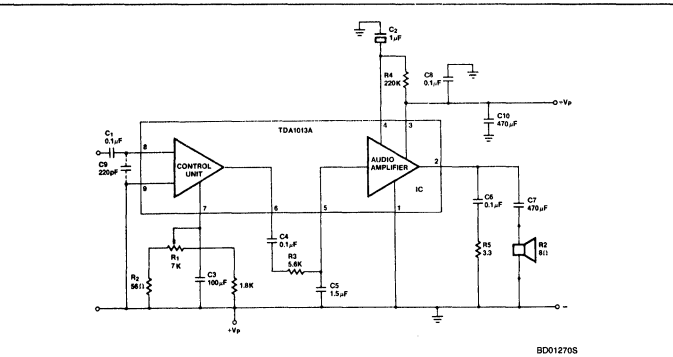


Figure 2. Block Diagram And External Components.

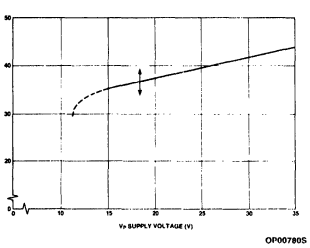


Figure 3. Quiescent Current Versus V_p

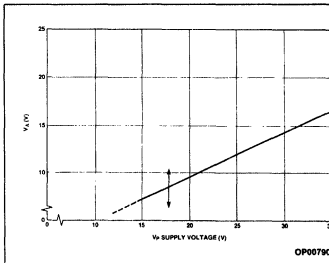


Figure 4. Midtap Voltage Versus V_p

MEASUREMENTS

Various measurements made in the circuit of Fig. 1 are given. If not otherwise stated, the measurements are done at V_p = 18V, R_L = 8Ω, f = 1kHz and T_a = 25°C.

Audio Amplifier With TDA1013A AN148

Quiescent Current Consumption

The quiescent current as a function of V_p is given in Fig. 3. At V_p = 18V the maximum spread on 20 samples is indicated by arrows.

Midtap Voltage

The midtap voltage V_A versus V_p at output pin 2 is shown in Fig. 4.

Output Power and Dissipation

The output power for d = 10% as a function of V_p at pin 2 and across the 8Ω loudspeaker load is given in Fig. 5. The upper curve gives the worst case sinewave dissipation. The dissipation versus output power for V_p = 18V is given in Fig. 6.

Distortion

The total harmonic distortion as a function of P_o is shown in Fig. 7 for signal frequencies of 1 and 10kHz (DC control voltage at pin 7 is constant 8V). In Fig. 8 the same curve is given for f = 1kHz but now the output power is reduced by the DC control voltage (at d = 10% V_{DC} pin 7 = 8V). The distortion for 2.5W output power versus frequency is given in Fig. 11. In Fig. 9 the distortion of the DC gain controlled pre-amplifier as a function of the signal excursion at pin 6 is shown for a DC control voltage (V_{DC} pin 7) of 8V.

Gain Control

The typical overall voltage gain (V_{DC} pin 7 = 8V) is 38dB. The gain control curve versus the DC control voltage on pin 7 is shown in Fig. 10.

Frequency Characteristic

The frequency characteristic is presented in Fig. 12. The -3dB bandwidth is from 32Hz to 20kHz.

Power Bandwidth

The power bandwidth (d = 10%) is given in Fig. 13. The low frequency behavior is determined by the value of the output electrolytic C_7.

Supply Voltage Ripple Rejection

The supply voltage ripple rejection versus frequency is shown in Fig. 14 for R_S = 0 and 10kΩ. Ripple voltage on pin 3 is 500m. V_{rms}.

Noise Behavior

The A-weighted, IEC 179 standard, signal-to-noise ratio at maximum gain (V_{DC} pin 7 = 8V) is 68dB at R_S = 0Ω and related to P_o = 2.5W. Increasing R_S has hardly any influence on this noise level. Typical S/N is 74dB.

CONCLUSIONS

The TDA1013A is a suitable IC as an audio amplifier in TV receivers. It delivers an output power of about 4.4W in R_L = 8Ω at V_P = 18V. An 80dB DC gain control is incorporated.

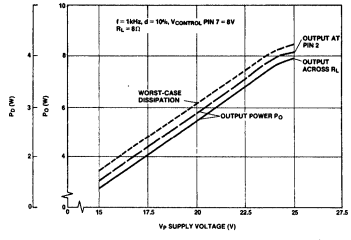


Figure 5. Output Power And Dissipation Versus V_p

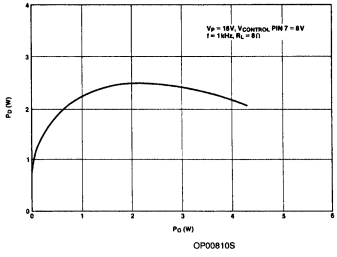


Figure 6. Dissipation Versus P_o

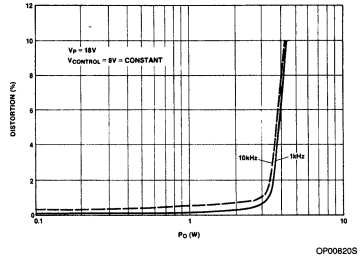


Figure 7. Distortion Versus P_o

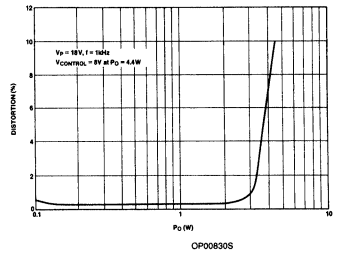


Figure 8

Audio Amplifier With TDA1013A

AN148

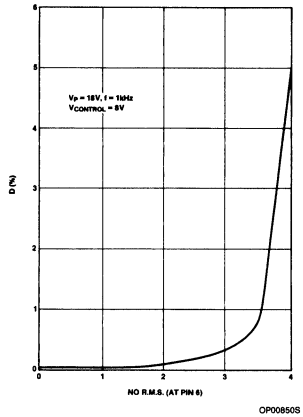


Figure 9. Distortion of Control Amplifier At Pin 6

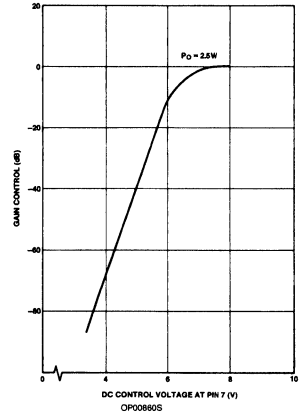


Figure 10. Typical Control Curve DC Control Voltage At Pin 7

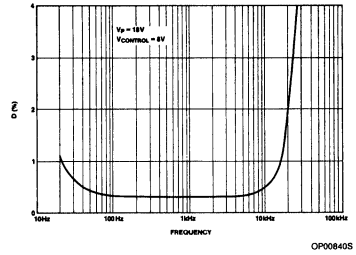


Figure 11. Distortion at P_O = 2.5W Versus Frequency (At Pin 2 of I.C.)

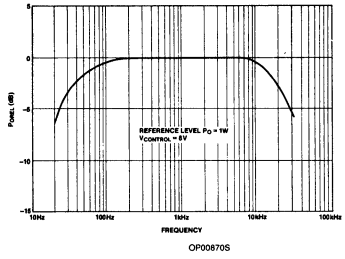


Figure 12. Frequency Characteristic

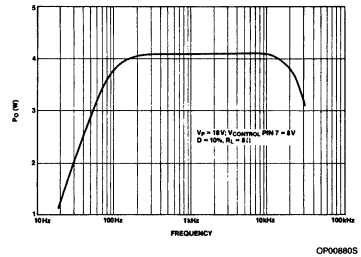


Figure 13. Power Bandwidth

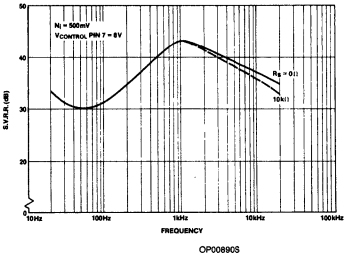


Figure 14. Ripple Rejection Versus Frequency

9

20W Hi-Fi Power Amplifier with the TDA1520A AN149

Author: D. Udo

ABSTRACT

The TDA1520A single operational hi-fi power amplifier is intended for audio and television applications.

The circuit can deliver output power up to 20W into 4 and 8 ohm loudspeakers operating either from symmetrical or asymmetrical power supplies.

The 9-lead SOT 131A power encapsulation combines good thermal behavior ($R_{thj\text{-}mb} \leqslant 2$ K/W) with a reliable simple mounting to external heatsinks (screw or clip mounting).

The IC has several internal protection circuits to allow misloading conditions.

INTRODUCTION

The TDA1520A integrated operational amplifier in the 9-lead single-in-line plastic power package SOT 131A, is intended for use as class-B hi-fi power amplifier.

Some performance specifications are shown below.

Supply voltage range	15 – 50V
Minimum guaranteed output current	3.2A
Minimum non-repetitive output peak current	5A
Maximum operating ambient temperature	150°C
Thermal resistance $R_{thj\text{-}mb}$	$\leqslant$ 2 K/W
Input impedance at pin 1	> 1 Mohm

The TDA1520A can be powered with symmetrical and asymmetrical power supplies. This APP note shows applications with asymmetrical power supplies.

INTERNAL CIRCUIT DESCRIPTION

The internal circuit block diagram of the TDA1520A is shown in Figure 1.

The input amplifier is a Darlington coupled PNP differential stage (T1 – T4) having a 800/=mμA current source S1. D.C. biasing for T1 can be derived from the internal voltage bleeder RA – RB.

In our application, with asymmetrical power supply, the D.C. biasing is made with an external resistor between pin 1 and pin 8. The external resistance between pin 1 and pin 8 must be limited to 100 kohm for offset voltage reasons. The current drive to the class-A driver stage (T7 – T8) is obtained from the current mirror circuit of T5 – T6.

The D.C. current source S2 (5mA), for the class-A stage T7 – T8 flows through the three series diodes D, to adjust and stabilize the quiescent current of the output stage.

Each branch of the quasi complementary output stage consists of two Darlington coupled NPN transistors (T9 – T10 and T13 – T14).

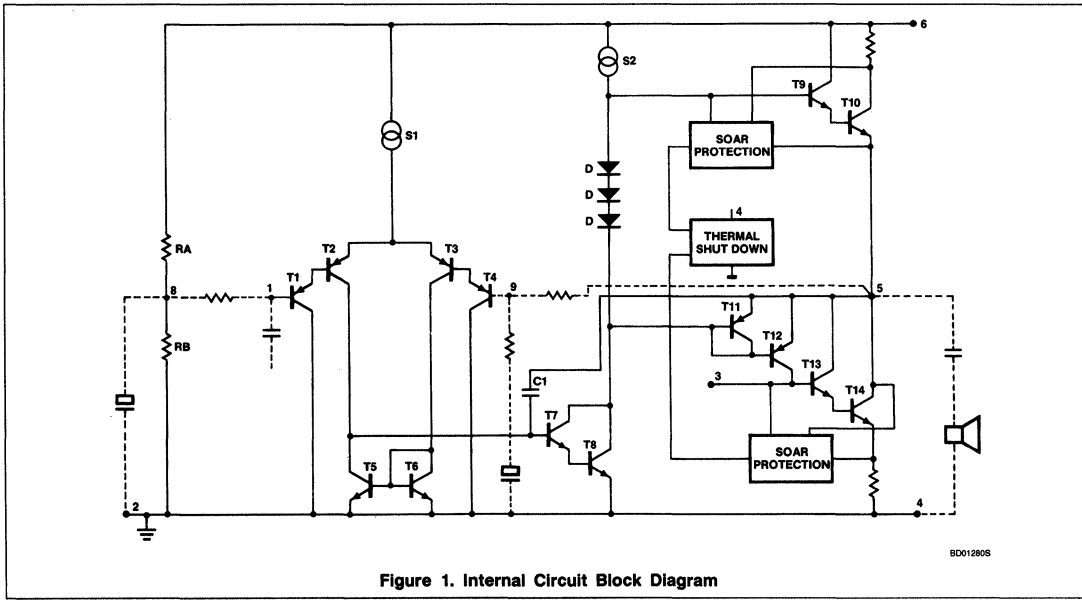


Figure 1. Internal Circuit Block Diagram

20W HI-FI Power Amplifier With The TDA1520A AN149

The unity gain PNP class-B driver (T11 – T12) offers the 180° phase-shift for the lower output stage.

The open loop frequency cut-off is determined by the integrated capacitor C1. Open loop gain is typical 74dB.

The amplifier has a number of internal circuit blocks to protect the device against short-circuiting of the loudspeaker, misloading conditions (SOAR and thermal protection).

The thermal shut-down circuit starts operating for chip temperatures *higher* than 150°C.

AMPLIFIER APPLICATION CIRCUIT

The circuit diagram of the TDA1520A amplifier operating from an asymmetrical power supply is shown in Figure 2.

The closed loop gain of 30dB is fixed by the resistors R1 and R3 while the input resistor R2 has the same value as R3 to keep the offset voltage as small as possible.

Also to keep the offset voltage low, it is advised to limit the value of R2 to about 100 Kohm.

To improve the turn-off behavior, some external components are added. These components, a resistor of 2.2 Kohm and two diodes, are dashed in Figure 2.

It is recommended to have the power supply electrolytic as close as possible to the amplifier p.c.board.

With the asymmetrical power supply of 33V, the worst-case power dissipation is 15.5W (see also Figure 18).

Calculation of the heatsink:

$$Rth(j\text{-}a) = \frac{Tjmax - Tamax}{Ptot}$$

$$= \frac{(150 - 45)°C}{15.5W} = 6.7\ K/W$$

The thermal resistance of the heatsink becomes:

Rth(h-a) = Rth(j-a) – Rth(j-mb) – Rth(mb-h) = (6.7 – 2 – 0.2) K/W = 4.5 K/W.

In the proposed appliance a 3.5cm extruded heatsink is used (type KL-134 of Seifert).

MEASUREMENTS

Several measurements are done on the application circuit of Figure 2.

Quiescent Current Consumption.

The quiescent current consumption versus supply voltage is given in Figure 3.

Midtap Voltage

The midtap voltage versus supply voltage is given in Figure 4.

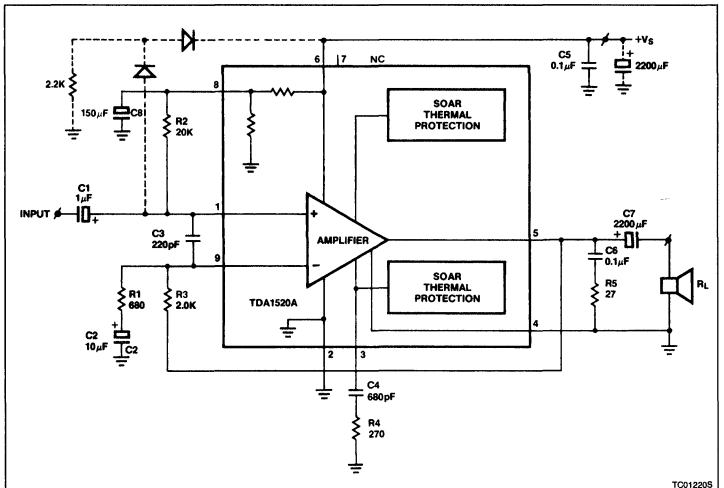


Figure 2. Circuit Diagram

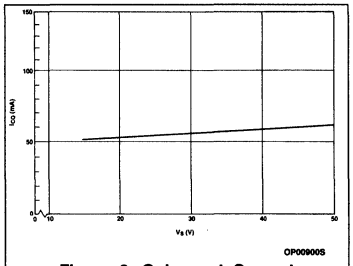


Figure 3. Quiescent Current Versus Supply Voltage

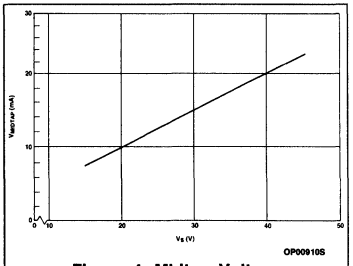


Figure 4. Midtap Voltage Versus Supply Voltage

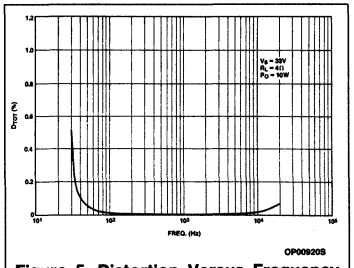


Figure 5. Distortion Versus Frequency

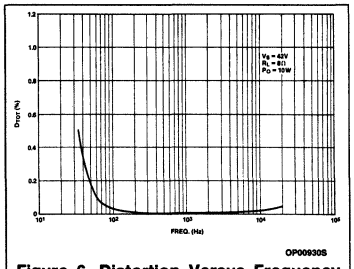


Figure 6. Distortion Versus Frequency

Harmonic Distortion

The harmonic distortion versus frequency at Po = 10W is given in Figure 5 for Vs = 33V and RL = 4 ohm and in Figure 6 for Vs = 42V and RL = 8 ohm.

The harmonic distortion versus output power at f = 1kHz is given in Figure 7 for Vs = 33V and RL = 4 ohm and in Figure 8 for Vs = 42V and RL = 8 ohm.

Power Bandwidth

The power bandwidth for d_{tot} = 0.5% is given in Figure 9 for Vs = 33V and RL = 4 ohm and in Figure 10 for Vs = 42V and RL = 8 ohm.

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20W HI-FI Power Amplifier With The TDA1520A

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Intermodulation Distortion

IM distortion versus output power is given in Figure 11 for Vs = 33V and RL = 4 ohm and in Figure 12 for Vs = 42V and RL = 8 ohm.

Frequency Response

In Figure 13 the frequency response is given for Vs = 33V and RL = 4 ohm and in Figure 14 for Vs = 42V and RL = 8 ohm.

The reference level (0dB) is at 10dB below Po max (= 2.2W) at f = 1kHz.

Output Power

The output power versus supply voltage is given in Figure 15 for RL = 4 ohm and 8 ohm, measured at d_{tot} = 0.5% and f = 1kHz.

Power Dissipation

The power dissipation of the TDA1520A as a function of the output power, measured at Vs = 33V, f = 1kHz and RL = 4 ohm is given in Figure 16 and with Vs = 42V, f = 1kHz and RL = 8 ohm in Figure 17.

The worst-case power dissipation versus supply voltage is shown in Figure 18.

Input And Output Impedance

The input impedance of the TDA1520A at pin 1 is > 1 Mohm. The input impedance of the application circuit of Figure 2 is 20 Kohm, determined by the external resistor R2.

The output impedance at pin 5 is 10 mohm at f = 1kHz.

Gain

The input sensitivity for Po = 10W is 210mV. The closed loop gain measured at f = 1kHz is 30dB. The closed loop gain can be varied by resistors R1 and R3.

Noise

The weighted signal to noise ratio at Po = 50mW and RS = 2 Kohm is 80dB measured according to IEC 179 (A-curve).

The unweighted noise (f = 20Hz – 20kHz) is 76dB.

Measured according to CCIR 468 peak value (also new DIN 45405 standard) this S/N ratio is 66dB.

Slew Rate

The slew rate of the amplifier is 6V/μsec.

Supply Voltage Ripple Rejection

The supply voltage ripple rejection at f = 100Hz, is 58dB (RS = 0).

Short Circuit Behavior

A.C. short circuiting is possible during 60 sec, measured with sine wave drive f $\geqslant$ 40Hz into clipping at a supply voltage of 30V and with a supply series resistance of 4 ohm.

Measuring under the same conditions but with pink noise drive, according to IEC 268-1C, A.C. short circuiting is allowed up to 15 minutes.

Turn-on and -off Behavior

With the extra network the turn-off behavior of the TDA1520A can be improved.

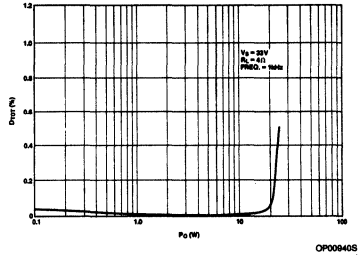

Figure 7. Distortion Versus Output Power

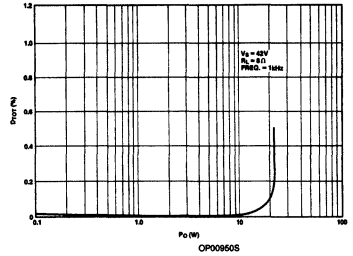

Figure 8. Distortion Versus Output Power

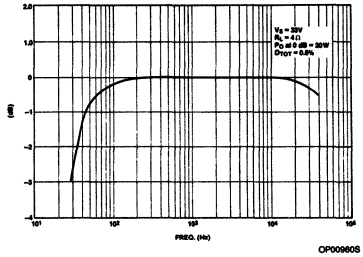

Figure 9. Power Bandwidth

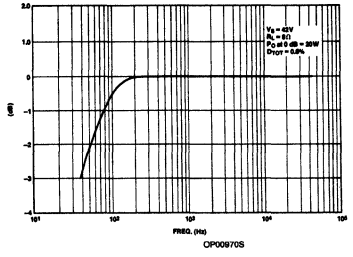

Figure 10. Power Bandwidth

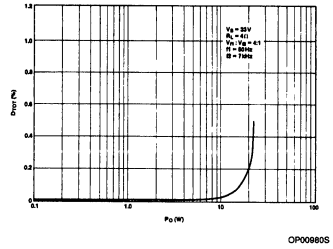

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Figure 11. IM Distortion Versus Output Power

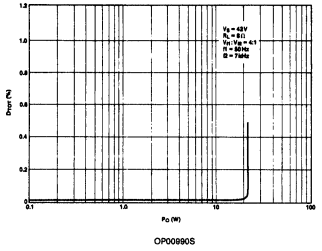

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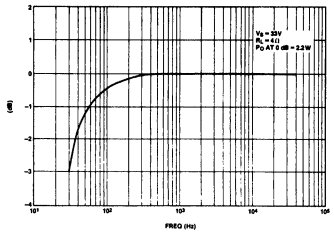
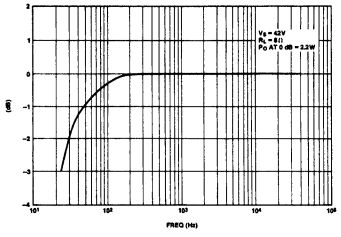
Figure 12. IM Distortion Versus Output Power



OP01000S

Figure 13. Frequency Response at P_O = 2.2W



OP01010S

Figure 14. Frequency Response at P_O = 2.2W

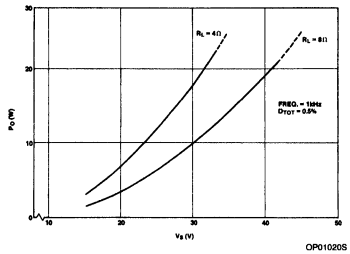


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Figure 15. Output Power Versus Supply Voltage

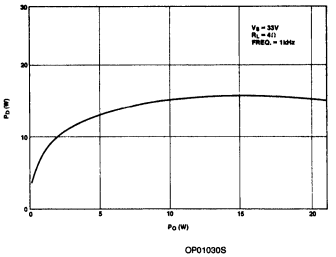

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Figure 16. Power Dissipation Versus Output Power

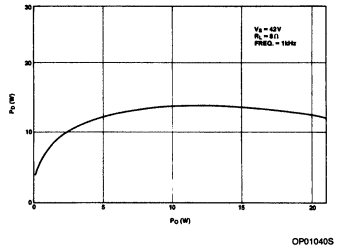

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Figure 17. Power Dissipation Versus Output Power

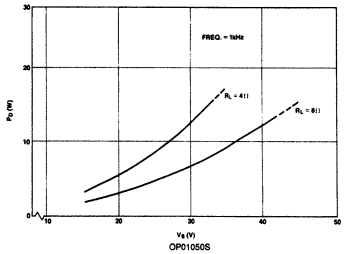

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Figure 18. Worst Case Power Dissipation Versus Supply Voltage

9

Progress in SMPS Magnetic Component Optimization AN125

L. P. M. BRACKE

The last ten years have seen considerable progress in the development of the switched-mode power supply. Both design methods and associated hardware have been refined by experience and intensive development. These improvements, especially in the understanding of the influence of magnetic material and winding-conductor properties on SMPS operation, are reflected in the more straightforward and complete design routines now available. The better understanding that made for the improved design routines has also resulted in improved core designs: the ETD range of ferrite cores. Furthermore, lessons learned from experience in wound-component production have been applied to the design of the associated hardware, especially the coil former. The improved core and coil former, together with specially-developed assembly hardware, form the ETD system.

IMPROVED DESIGN ROUTINES

References 1 to 4 form a series of publications that presents complete design routines for the magnetic components of all common versions of SMPS. Part 1 of the Series (Ref.1) covers most aspects of SMPS design, with emphasis on the interaction between the electronic and magnetic aspects. The basic electrical relationships are given for forward, push-pull and flyback converters. Practical formulae are given for inductance and effective-current values. Auxiliary outputs and other special features are included in the coverage, as are related control aspects. All treatments are related to the magnetic design.

The data derived from Ref.1 are used in Part 2 of the Series (Ref.2) to select a suitable ferrite core for the transformer. Here, the magnetic and thermal properties of ferrite cores are considered as they affect their suitability for a given application. Initial selection of a suitable core is by means of charts showing the limits of performance to be expected at various frequencies. The optimum working conditions for cores in various transformer types are discussed, and a further chart enables this optimum to be determined. Wound transformer thermal characteristics are discussed, and formulae given for the losses in the core itself. Together with expressions for the number of turns required, Ref.2 allows the design of an SMPS transformer to progress from the electrical requirements set forth in Ref.1 to the mechanical design of the windings themselves discussed in Ref.3.

SELECTING THE CORRECT CORE

Most SMPS requirements can be satisfied by the range of cores currently available (Ref.5). The preferred grade of material for such high-frequency power applications is Ferroxcube 3C8.

Core selection charts

Due to the wide variation in application conditions, the selection charts have been designed to indicate the range of operation of the cores. This is done by using areas of throughput power as a function of frequency as shown in Fig.1. These are effectively areas of good design, since both boundaries represent the performance of a well-designed transformer.

The upper boundary of each area corresponds to a transformer design operating at optimum flux density sweep, with maximum use of the winding window, and Litz-wire windings, for minimum a.c. resistance. The lower boundary corresponds to a transformer design that also operates at optimum flux density, but has optimised solid-wire windings

incorporating 8 mm creepage distance for IEC 435 mains isolation, and with a demagnetising winding occupying one third of the winding space.

Selection charts are given for push-pull, forward and flyback converter SMPS. However, the flyback converter charts are mainly intended as a cross-check on the design obtained by the method given in Ref.4 for chokes.

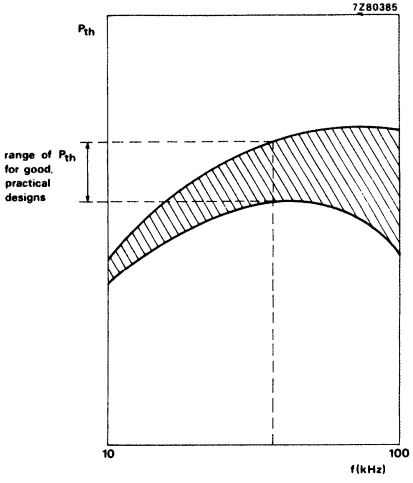


Fig.1 In the core selection charts given in Part 2 of the SMPS transformer design series (Ref.2), the power-handling capability of each core is plotted as a shaded area extending from 10 kHz to 100 kHz. The vertical boundaries of this area are the upper and lower limits of throughput power capacity achievable by good design but depending on conductor type and insulation requirements

Operating conditions

Converter type has the largest influence on throughput power obtainable, but other factors also influence performance, principally

- flux-density sweep
- winding configuration (simple or split, for example) and
- the presence of sensor or demagnetising windings
- the type of conductor used in the windings
- the number of output windings required
- mains insulation requirements.

Generally, the selection charts assume worst-case conditions. Operation at ambient temperatures lower than the 60 °C assumed, the use of feed-forward to ease the restriction on peak flux density (1/1.72 of saturation to allow for transient conditions), or heatsinking or potting to reduce thermal resistance, will all increase transformer power capacity.

Flyback transformers and chokes

Flyback converter transformers and output chokes are magnetically much the same: the main design requirement is stored energy, $\frac{1}{2}I^2L$. This is the basis of a separate design routine that includes winding design (Ref.4). This routine, using specially-developed design charts, leads directly to spacer thickness and number of turns.

OPERATING FLUX DENSITY

For chokes and flyback-converter transformers (which operate as chokes), stored energy is the basis of the design (subject to the core not being driven into saturation). With forward and push-pull converter transformers, the operating flux density (both a.c. and d.c. components) is set at the beginning of the design process.

Forward and push-pull converters

The operating flux density in forward and push-pull converter transformers strongly influences the overall volume of the transformer. Thus, it is set at the beginning of the design process to as high a level as practicable. For forward converter transformers, this level is determined by transient protection requirements or permissible core loss only. With push-pull converters, however, considerations of symmetry may dominate the choice.

Both forward and push-pull converter transformers must be designed to accommodate rapid changes of load. This is done by introducing a transient factor, usual symbol α, related to the range of input voltage for which the power supply is designed. A common value of α is 1.72. This is suitable for mains-fed supplies (215 V to 370 V or 200 V to 340 V), telephone supplies (40 V to 70 V), and mobile supplies (9 V to 15.5 V).

Considerations of symmetry usually result in the value of α being multiplied by a further factor ϵ for push-pull converter transformers. Asymmetry leads to core saturation, which in turn results in destruction of power switches. Principal causes of asymmetry are unbalanced flux linkage in windings (Ref.3) and unequal conduction times in switches. Where care has been taken to achieve balanced transformer windings, and protection circuitry is incorporated to ensure equal conduction times, the value of ϵ may be 1.15; that is, α is increased from 1.72 to 2 for a typical core. Where unbalance is accepted, however, the value of ϵ should be 2. (A list of the symbols used in this article, together with their definitions, is given as Table 1).

The use of feedforward (Ref.1) can considerably reduce the value of α required but at the expense of reduced transient response.

In forward-converter transformers core remanence should also be taken into consideration. However, the introduction of a small airgap in the core, and the use of a slow-rise capacitor (Ref.1) allows the whole first quadrant of the core hysteresis loop to be used.

TABLE 1
List of symbols

symbol	unit	definition
B_{ac}	T	flux-density sweep; half the peak-to-peak flux density excursion
B_{CF}	mm	coil former breadth
f	Hz	operating frequency
f_1	Hz	the frequency at which the number of turns on the lowest-voltage transformer winding becomes unity
f_L	Hz	the lowest frequency at which the coil former height is sufficient to accommodate ideal (minimum-loss) windings
f_T	Hz	the frequency above which no useful increase in the throughput-power capacity of a transformer can be obtained
H_{CF}	mm	coil former height
L	H	choke inductance
ℓ_{av}	mm	average turn length
P_c	W	total transformer core loss
$R_{th\,c}$	K/W	transformer or choke thermal resistance with winding creepage distance incorporated
$R_{th\,n}$	K/W	transformer or choke thermal resistance for a winding without creepage distance
V_e	m^3	effective volume of a core
α	–	ratio of core saturation flux to working flux allowed: for transient response without saturation
ΔT	K	temperature rise above ambient
ϵ	–	unbalance factor

subscripts

e	effective value
cp	pertains to centre pole

Figure 2 shows the maximum transformer flux-density sweeps for various converter types, and Table 2 gives the value of transient factors α and ϵ under various conditions.

Optimum flux-density sweeps

Manipulation of the expression (Ref.6) for the throughput power of an SMPS transformer shows that power reaches a maximum at a combination of operating frequency and flux density such that core loss is 44% of total loss. That is, when

$$0.44\ \frac{\Delta T}{R_{th}} = 16.7\ f^{1.3}\ B_{ac\,em}^{2.5}\ V_e$$

Here, the right-hand part of the expression is the typical hysteresis loss of Ferroxcube 3C8 ferrite. Since eddy-current loss is neglected, this expression applies only up to about 100kHz.

TABLE 2
Maximum values of flux-density sweep for various converter types and control circuits

boundary conditions	flux-density sweep $B_{ac\,cp}$ (T)	
	forward	push-pull
maximum sweep for FXC 3C8 (100 °C)	0.16	0.32
at transient factor α	$\frac{0.32}{2\alpha}$	$\frac{0.32}{\alpha}$
with unbalance factor ϵ*	–	$\frac{0.32}{\epsilon\alpha}$
with x% feedforward	$\frac{0.32}{2\,(1 + x/100)}$	$\frac{0.32}{(1 + x/100)}$
with unbalance factor ϵ and x% feedforward	–	$\frac{0.32}{\epsilon\,(1 + x/100)}$

* ϵ is the ratio of peak flux density in a balanced converter to the peak flux density in an unbalanced converter.

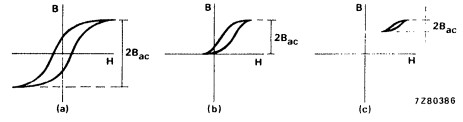


Fig.2 Flux-density excursions and corresponding flux-density sweeps for (a) push-pull, (b) forward converter transformers (with slow-rise capacitor) or ringing choke, and (c) flyback converter chokes

Using this expression, curves of $B_{ac\,em}$, the peak flux-density sweep, have been derived for all Philips' SMPS transformer cores (See Fig.3).

THERMAL RESISTANCE AND TEMPERATURE RISE

The maximum permissible dissipation of a transformer or choke is set by its maximum operating temperature; ambient temperature and thermal resistance depend on core size, mounting method and attitude, the type of conductor in the winding and the amount of insulation incorporated. Due to the insulating effect of the interleaving where 8 mm creepage distance is allowed for in the windings, two values are quoted for thermal resistance in Ref.2: with and without creepage allowance.

Measurement methods are discussed in Ref.2 and 7. Results given in Ref.7 confirm that transformer temperature rise can be accurately calculated from the product of total transformer dissipation and thermal resistance for any ratio of core to winding loss.

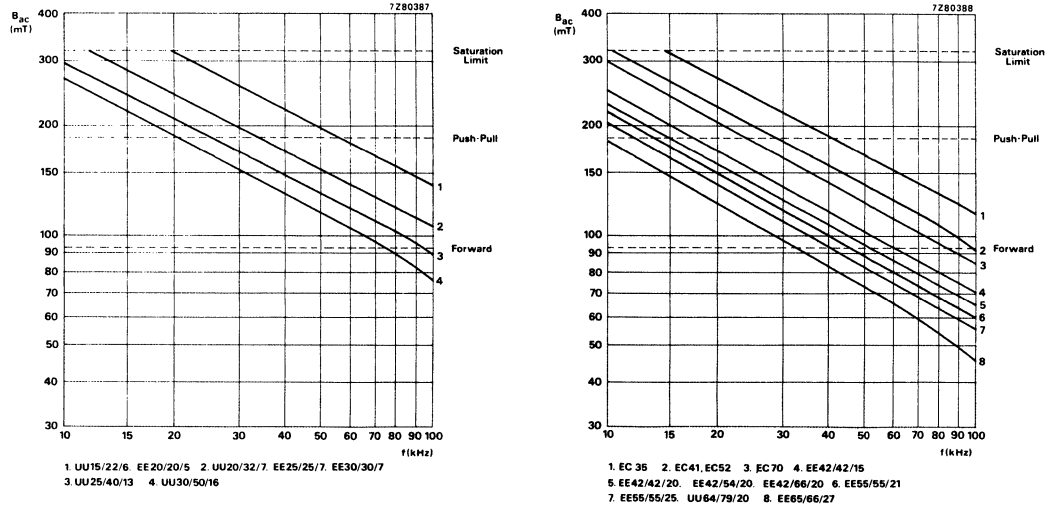


Fig.3 Optimum, peak, centre-pole flux-density sweeps $B_{ac\,cp}$ for a variety of cores for SMPS applications. Horizontal lines indicate the limits for various converter types ($\alpha = 1.72$). The curves were calculated for a peak temperature rise of 40 K

THE EFFECT OF OPERATING FREQUENCY

Winding properties

Depending on frequency, the windings of an SMPS transformer fall into one of three categories. At low frequencies, the available winding-window height will be insufficient to accommodate minimum-loss (ideal) windings. At some higher frequency, f_L, the height of minimum-loss windings becomes less than that of the winding window. Finally, at some higher frequency, f_1, the number of turns required for the lowest-voltage winding becomes unity.

It is shown in Ref.8 that, where the winding height is insufficient for minimum-loss windings, winding loss is inversely proportional to the squares of both flux-density sweep and operating frequency. At frequencies above f_L winding loss becomes inversely proportional to operating frequency.

Flux density sweep

From the considerations given earlier, it is apparent that at lower frequencies, operating flux density is limited by core saturation rather than loss. Above some frequency f_T, the optimum operating flux density (for maximum power) becomes less than the saturation-related maximum, and the flux-density sweep is limited by the requirement that (for Ferroxcube 3C8) core loss $P_c = 0.44\,P_{tot}$, where P_{tot} is the total permissible dissipation.

Throughput power

In Ref.8, these various effects of operating frequency are combined to explain the observed variation of SMPS transformer throughput power with operating frequency for Ferroxcube 3C8 cores. Figure 4(a) shows the division between core and winding loss for an SMPS transformer as a function of operating frequency. Frequencies f_L, f_T and f_1, are marked. (Note that f_L may, in fact, be higher than f_T for some cores. This does not alter the main argument.) In Region I, operating flux density is limited by saturation considerations only, so that throughput power is roughly proportional to frequency. Operation remains saturation limited into Region II, but here power increases roughly as the root of the frequency. (This relationship is complicated by the fact that average turn length decreases as ideal-winding height decreases.) Region III begins at f_T, where core operating flux density becomes limited by core loss to the optimum value for that frequency. The shape of the throughput power curve in the region depends on core material characteristics: the Steinmetz coefficient and its associated flux-density and frequency exponents. For Ferroxcube 3C8, flux density is inversely proportional to the root of frequency. Then, winding resistance decreases slightly with frequency so that, since winding loss is constant, throughput power is also about constant.

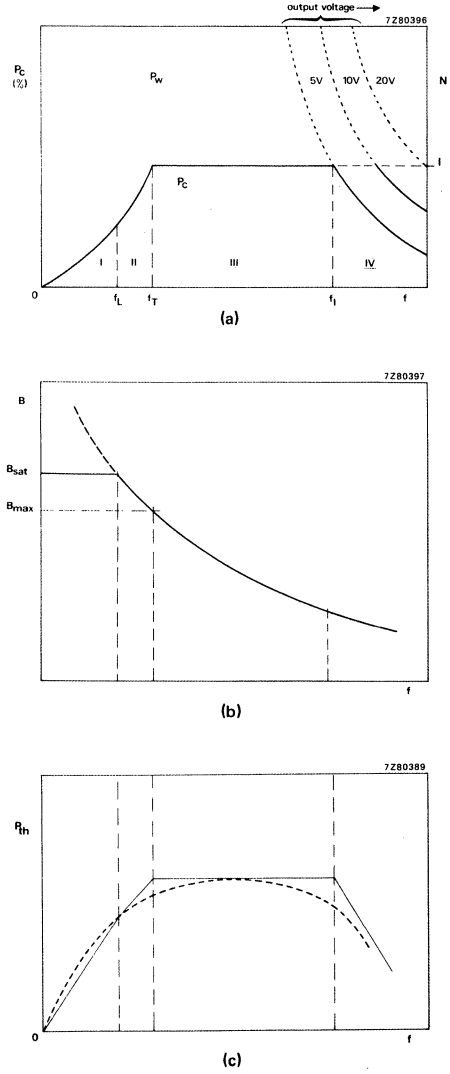


Fig.4 (a) Division of transformer loss between core loss and winding loss as a function of frequency, showing the various boundary frequencies. (b) Relation between flux density and frequency for maximum throughput power. (c) The corresponding throughput power characteristic

Region IV begins where frequency increases to the point where the number of turns required on the lowest-voltage winding falls to unity. (Contours of number of turns N as a function of frequency for various voltages are indicated in Fig.4(a)). When this happens, flux density must then decrease with frequency. The rate of this decrease is greater than that required for optimum core loss, so that throughput power decreases. The effect is accentuated by the increasing contribution of eddy-current losses at high frequencies.

In practice, other factors, such as eddy-currents, parasitic capacitance and rounding of numbers of turns, cause the transitions from one Region to another to become blurred so that, as Fig.4(c) shows, the thoughput power characteristic is more rounded. Calculated values for real cores, Fig.5, shows that the general characteristics remain, however: there is always a frequency, close to the core transition frequency, above which no useful increase in throughput power can be obtained.

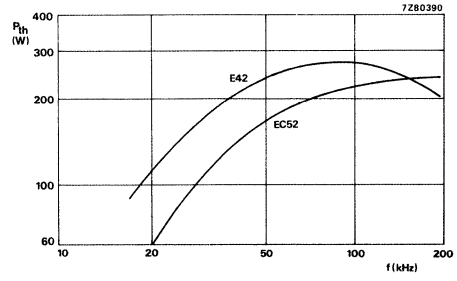


Fig.5 Calculated throughput powers (5 V forward converters) with frequency for EC52 and E42/21/20 core show the same general characteristics: there is a frequency (from Fig.3) above which no useful increase in throughput power can be obtained. For the EC52 core this is 100 kHz, for the E42 core it is 52 kHz

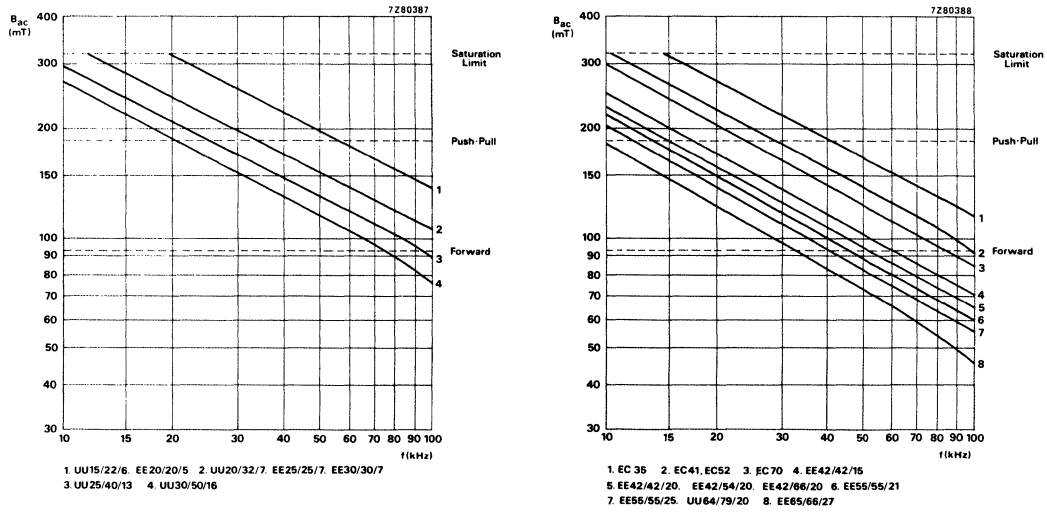
EFFECT OF CORE DESIGN

The more complete understanding of the factors that influence throughput power obtainable has made it possible to examine established core designs with a view to improving the designs available. Electrical, magnetic and mechanical considerations can now be combined so that the core can be made as effective as possible.

Existing core designs

Analysis of existing core designs (E, EC, PM, PQ and RM cores, Ref.8) shows that performance agrees well with values of f_T. The performance of the smaller cores is found to be relatively poor at 50 kHz due to lack of sufficient winding-window height for ideal windings.

The effectiveness of the use of core materials is another important consideration, since it directly affects the weight of an SMPS. Constant cross-section E cores generally have the best power-to-weight ratios.



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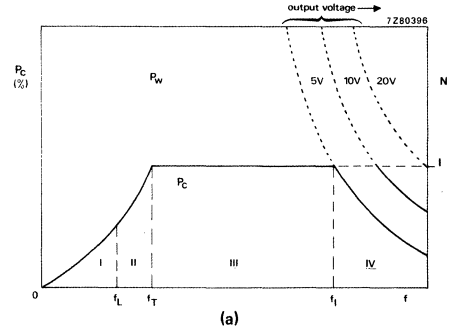

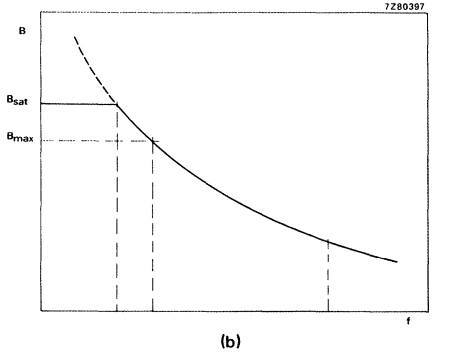

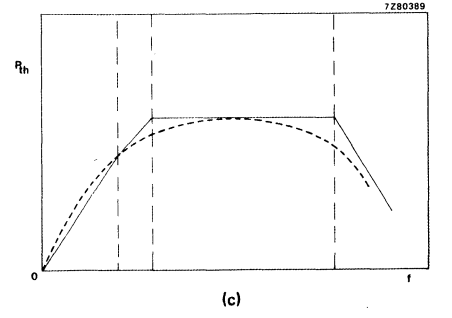

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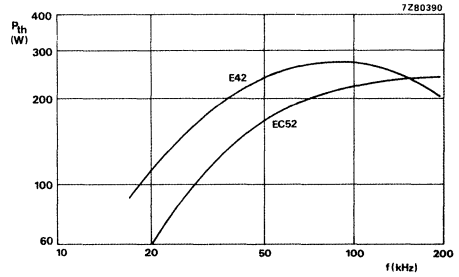

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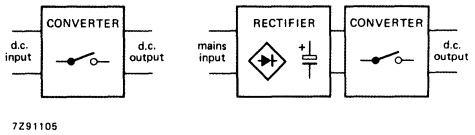
SWITCHED-MODE POWER SUPPLIES

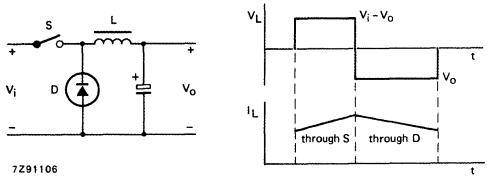
The essential difference between switched-mode and conventional (mains) power supplies is operating frequency. Whereas conventional power supplies operate at mains frequencies, 50 Hz or 60 Hz, switched-mode power supplies (SMPS) operate at frequencies of the order of 50 kHz. The complications associated with operation at these high frequencies are more than compensated for by the savings in weight and volume, especially of transformers and smoothing components.

Voltage conversion and control in SMPS is achieved by chopping the incoming supply voltage with a high-speed switch such as a transistor. The chopped voltage is applied to a transformer which performs voltage conversion and provides isolation. This transformer is generally wound on a ferrite core, and is much smaller and lighter than a 50 Hz unit of comparable power capacity. Fine control of output voltage is obtained by varying the duty cycle of the switch.

Most SMPS converters require a d.c. input and provide a d.c. output. For operation from the mains, therefore, a rectifier and smoothing circuit generally precedes the converter itself, Fig.A.



A



B

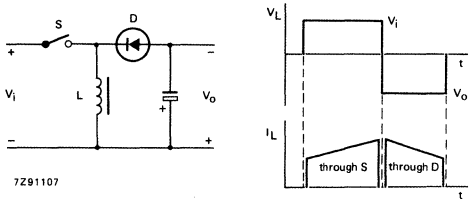
SMPS converters

There are three basic SMPS converter arrangements; they and their variants are discussed in detail in Ref.1.

In the forward converter, Fig.B, power is transferred directly to the load while the switch is closed; the energy stored in the inductor is transferred to the load while the switch is open. The switch may be transformer coupled to the inductor for input/output isolation.

In the flyback converter, Fig.C, power is stored in the inductor while the switch is closed and transferred to the load while the switch is open. The functions of transformer and inductor may be combined where voltage transformation is required.

The push-pull converter is, effectively, a forward converter in which the output choke is driven by any push-pull arrangement of power transistors, including a full bridge, Fig.D. Operation after the transformer is similar to that of a forward converter, but with twice the effective switching frequency.



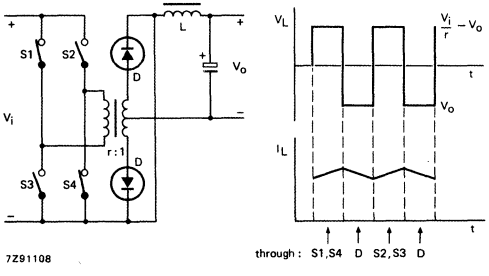
C

Transformer and choke requirements

There are two main boundary conditions for the power transformer: it must not saturate (otherwise the power transistors will be damaged) and it must not overheat. In addition to these boundary conditions, the output choke should be capable of storing sufficient energy to deliver one output cycle so that ripple will be low and regulation good.

Saturation is prevented by designing for worst probable combinations of load change and input voltage fluctuation. In forward converters, provision must be made for removing energy stored in the transformer at the end of the ON period of the switch. In push-pull converters, the degree of symmetry achievable in both power switches and transformer windings determines the unbalance allowance.

Overheating of the transformer and choke is prevented by calculation of total power dissipation: core hysteresis and eddy current losses, and winding losses.



D

Mechanical design is of great importance since this influences manufacturing cost and transformer production cost. The core should be cheap to manufacture. Enclosed cores, such as pot cores and their variants (RM, PQ, PM cores) are more expensive to make than E cores for a given power capacity. However, round centre legs make for easier winding, with less leakage inductance – especially for strip. For all but the smallest transformers, E cores result in more compact design than U cores. Finally, due to their symmetry, E cores require some 20% less core material for a given power capacity than U cores, with a consequent reduction in eddy-current losses. This last point is of especial importance at higher operating frequencies.

Core design requirements

From this theoretical and practical background the requirements for a new core design are clear. The range of cores should be optimised for frequencies appropriate to their power handling capacity: 50 kHz for 300 W, 100 kHz for 100 W, for example. This requires proper choice of f_L and f_T. Optimisation should be aimed at forward-converter applications (the cores will then also be suitable for unbalanced push-pull converters).

The design of the associated coil formers is also critically important. They should be suitable for automatic handling. A large number of pins is required, both for flexibility of layout and to accommodate multiple secondaries.

The core and wound coil former should be quick and easy to assemble. The combination should be designed for horizontal mounting on p.c. boards to minimise height and make termination of strip windings easier.

THE ETD SYSTEM

The cores

These criteria have been adopted in the design of the ETD cores (Ref.8). They are constant cross-section E cores in Ferroxcube 3C8 ferrite with round centre legs, photo and Fig.6, and are designed for

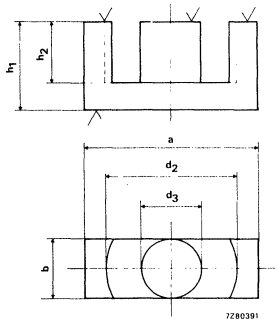
- minimum throughput powers in the range 100 W to 300 W
- economical manufacture
- minimum weight of ferrite
- operating frequencies in the range 50 kHz to 150 kHz
- high throughput power density
- mains isolation
- minimum transformer volume and p.c. board areas.

Magnetic properties are given in Table 3.

The ETD cores are compared with existing core designs for power per unit weight in Fig.7. Throughput power areas as a function of frequency for ETD cores are given in Fig.8, and the optimum flux density sweep in Fig.9.

TABLE 3
Magnetic dimensions of ETD system cores

core type	$A_{cp\ min}$ (mm^2)	A_e (mm^2)	V_e (mm^3)	ℓ_e (mm)
ETD 34	87	97.1	7 640	78.6
ETD 39	117	125	11 500	92.2
ETD 44	167	173	17 800	103
ETD 49	204	211	24 000	114



core type	mid-limit dimensions (mm)						mass (g)
	a	d_2	d_3	h_1	h_2	b	(core half)
ETD 34	34.2	26.3	10.8	17.3	12.1	10.8	20
ETD 39	39.1	30.1	12.5	19.8	14.6	12.5	30
ETD 44	44.0	33.3	14.9	22.3	16.5	14.9	47
ETD 49	48.7	37.0	16.4	24.7	18.1	16.4	62

Fig.6 Outline drawing and dimensions of the new ETD core range

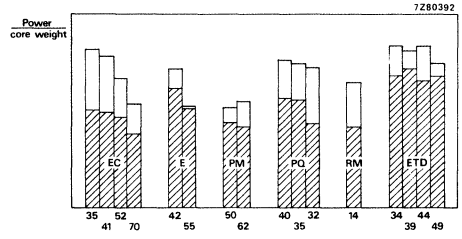


Fig.7 The throughput power per unit weight of core material for ETD cores compared with that of other popular core types at two operating frequencies: 50 kHz (shaded areas) and 100 kHz (open areas). Forward-converter operation is assumed

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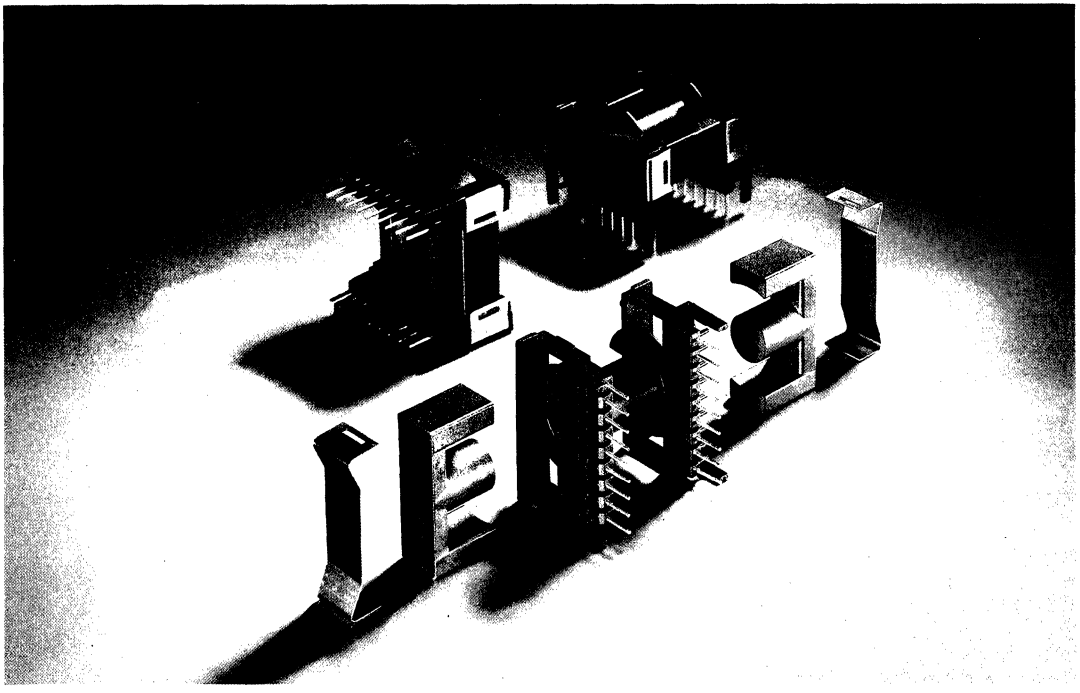


These ETD system components provide OEMs with the most efficient and economical route to SMPS transformers

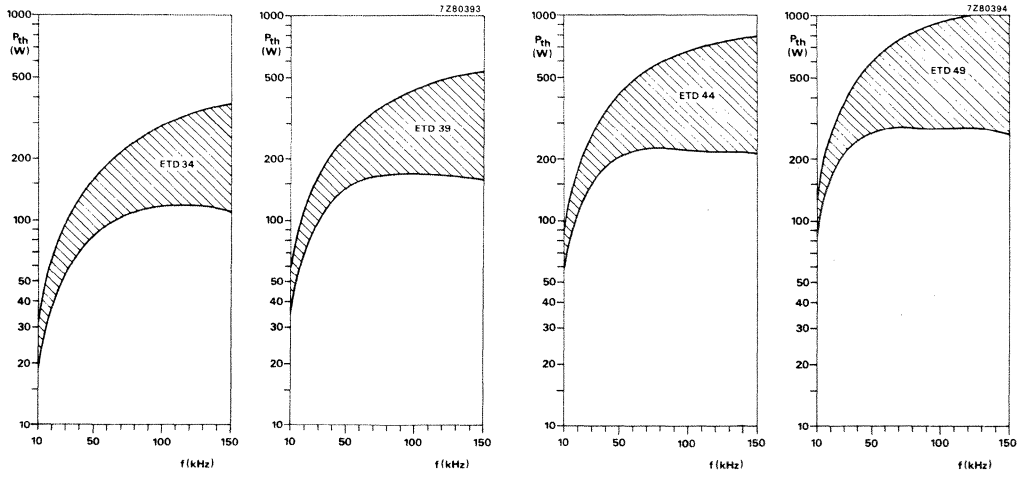


Fig.8 Throughput power as a function of frequency for ETD cores in forward-converter transformers

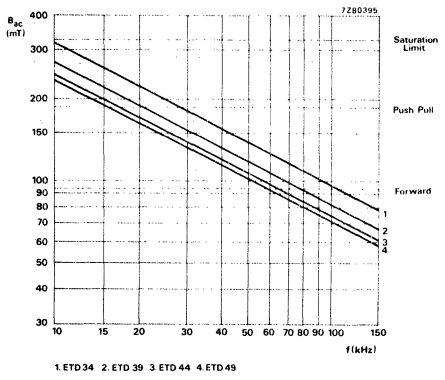


Fig.9 Optimum flux-density sweeps for ETD cores

The coil former and assembly hardware

Simple, rapid winding and assembly of ETD-system based transformers and chokes is made possible by the coil former of Fig.10, together with the associated snap-on stainless-steel assembly clips.

Principal features of the design are indicated in Fig.10:

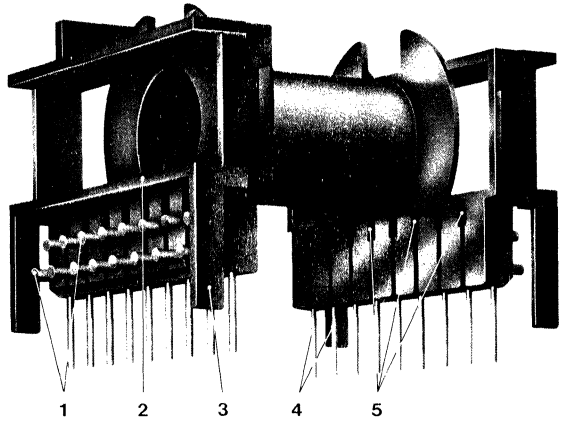
- the length and number of slots gives a wide choice of lead-out position
- there is at least 8 mm creepage distance from the pins to the ferrite core
- the pegs between the slots allow wire to be run from any one slot or pin to any other
- the four support legs provide 8 mm creepage distance between the windings and the p.c. board
- the hood over the pins provides 8 mm creepage distance between leadouts and assembly clips
- a separate earthing clip for the core is to be available.

The coil former itself is moulded in polybutylene terephthalate, a high-grade, flame retardant (UL 94-VO), thermoplastic. Windings dimensions are given in Table 4.

TABLE 4
Winding dimensions of ETD-system coil formers

type	B_{CF} (mm)	H_{CF} (mm)	ℓ_{av} (mm)
ETD 34	20.9	5.9	61
ETD 39	25.7	6.9	69
ETD 44	29.5	7.3	78
ETD 49	32.7	8.4	86

ETD system components provide OEMs with the most efficient electrical, magnetic and mechanical route to full, economical, automated production of SMPS transformers.



1 – pegs allow wires to be taken from most appropriate slot to chosen pin
2 – these plates give 8 mm creepage distance between wires and assembly clips
3 – legs give 8 mm creepage distance from windings and p.c. board.
4 – 8 mm creepage from pins to core
5 – multiple slots for maximum freedom of lead-out position

Fig.10 Coil former design for the ETD system, intended for automatic winding

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Using the SAA1027 with Airpax Four-Phase Stepper Motors AN127

INTRODUCTION

Airpax has introduced a range of five new 4-phase stepper motors which can be directly driven by an SAA1027 integrated circuit without the need for discrete power stages or compensating networks. Both the IC and the motors can operate from a single 12V supply. The high noise immunity design of the IC makes the system particularly suitable for use in electrically noisy environments. Use of the new motors and IC will drastically reduce the cost and complexity of stepper motor systems and thereby open up many new areas of application for digital motor control systems.

THE STEPPER MOTORS

The five new stepper motors are similar to our present industrial range with modified stator windings to match them to the output capability of the SAA1027 (350mA each phase). The maximum torque and pull-in rates obtained from the motors when they are driven by the SAA1027 are given in Table 1 for easy reference: the torque/speed characteristic curves and outline drawings of the motors are given in the *Technical Data* section of this publication.

THE INTEGRATED CIRCUIT

The SAA1027 integrated stepper motor drive circuit is contained in a 16-pin DIL plastic package and is shown in block diagram form in Fig. 1. The circuit comprises three input stages, a logic section, and an output stage for each of the four stator windings of the motor. The three input stages are compatible with high noise immunity logic to ensure correct operation in electrically noisy environments:

- The trigger stage accepts the incoming pulse train which initiates the logic section switching sequence, and thereby controls the speed of rotation and ultimate angular position of the motor drive shaft.
- The set stage accepts a logic level input which overrides the switching sequence of the logic section and sets the output stages to a predetermined logic state. This facility simplifies the programming of a system by allowing the motor drive shaft to be pre-positioned.
- The cw/ccw* stage accepts a logic level input which reverses the switching sequence of the logic section, thereby reversing the direction of rotation of the motor drive shaft.

The logic section contains a 4-bit bidirectional synchronous counter which switches the four output stages in the correct sequence to cause the motor drive shaft to rotate at the speed, and in the direction, dictated by the input stages.

The four output stages switch the supply current to the four phases of the motor stator. Each output stage is capable of switching a current of 350mA and incorporates an integrated diode for protection against transient spikes caused by switching the stator windings.

Brief data for the SAA1027 is given in Table 2. Further information is given in the *Technical Data* section of this publication.

Table 1. Quick Reference Data for the Motors

CATALOGUE NO.	STEP ANGLE	MAX. TORQUE (mNm)	MAX. PULL-IN RATE (STEPS/S)
9904 112 04002	7° 30'	12	240
9904 112 05001		65	140
9904 112 06001		45	120
9904 112 07005		5	350
9904 112 08001	15°	43	120

Table 2. Brief Data for the SAA1027

Supply voltage	V_P	9.5V to 18V
Load current (Each output)	I_Q	350mA max.
HIGH logic input level	V_{RH}, V_{SH}, V_{TH}	7.5V to V_P
LOW logic input level	V_{RL}, V_{SL}, V_{TL}	0V to 4.5V max.

THE SYSTEM

A practical stepper motor drive system and pulse diagram are given in Fig. 2.

Electrical Requirements

The system is powered from a single 12V supply with a current output compatible with the motor being driven. The current applied to pin 4 of the IC must be adjusted by selection of resistor R_B for each type of motor in accordance with Table 3.

Table 3. Selection Of Resistor R_B

MOTOR	R_B VALUE	I_{SYSTEM} (mA)
9904 112 04002	470 Ω, 0.33W	300
9904 112 05001	220 Ω, 0.67W	620
9904 112 06001	220 Ω, 0.67W	620
9904 112 07005	620 Ω, 0.33W	200
9904 112 08001	220 Ω, 0.67W	620

The relationship between the current at pin 4 of the IC and the output current is given in the *Technical Data* section of this publication.

Trigger Input *T*

The repetition rate and the number of pulses applied to pin 15 of the IC determine the stepping rate and ultimate angular position of the motor drive shaft. The steps are initiated by the positive-going edges of the pulses in the sequence shown in Table 4. The '0' state shown in the table is the logic state of

* Clockwise/counter-clockwise

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BLOCK DIAGRAM

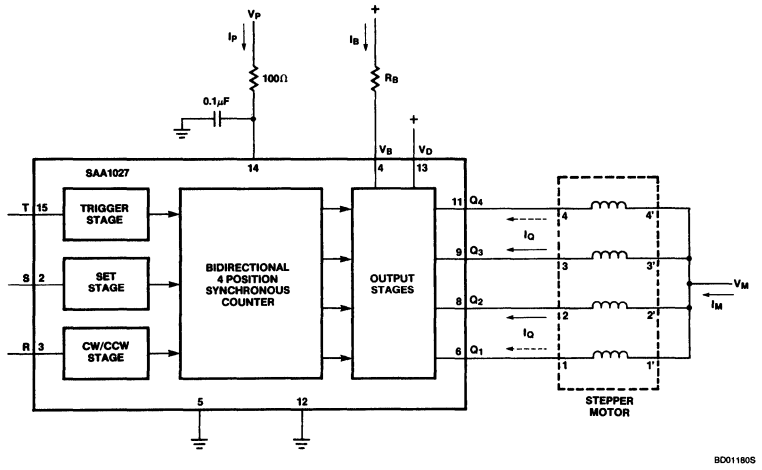

Figure 1. Block Diagram Of The SAA1027

the outputs when the 'set' input is operative.

Set Input *S*

The output switching sequence can be set to a predetermined logic state (Q_1 = L, Q_2 = H, Q_3 = L, Q_4 = H), by applying a LOW voltage level to pin 2 of the IC. This input is only effective if the voltage level at the trigger input is HIGH. To achieve maximum noise immunity, this input should be connected permanently to the HIGH voltage level if it is not required.

Direction Of Rotation Input *R*

The output switching sequence of the IC, and therefore the direction of rotation of the motor drive shaft, is determined by the level of the voltage applied to pin 3 of the IC. If the voltage level is HIGH, the drive shaft will rotate counter-clockwise: if the level is LOW, the drive shaft will rotate clockwise. The level of the voltage applied to pin 3 can be changed at any time regardless of the logic state of the other two inputs. To achieve maximum noise immunity, this input must not be left floating if not used, but should be connected to the voltage level appropriate to the required direction of rotation (to pin 14 for counter-clockwise; to pin 5 for clockwise).

Table 4. Output Switching Sequence

S = H										
R = L					R = H					
T	Q_1	Q_2	Q_3	Q_4	T	Q_1	Q_2	Q_3	Q_4
0	L	H	L	H	0	L	H	L	H
1	H	L	L	H	1	L	H	H	L
2	H	L	H	L	2	H	L	H	L
3	L	H	H	L	3	H	L	L	H
0	L	H	L	H	0	L	H	L	H

Precautions to Minimize the Effects of Switching Transients

If the IC and the motor are connected to the same supply source, a simple *RC*-network must be connected in the supply line to the logic part of the IC to prevent the switching sequence from being disturbed by transient spikes caused by switching of the motor windings. This network, which consists of a resistor of 100Ω and a capacitor of 0.1μF, is shown in Fig. 2 and Fig. 3. The capacitor must be located as close as possible to pins 14 and 5(12) of the IC. The connection between the common line of the four integrated clamping diodes (pin 13) and the common line of the four motor windings must be as short as possible.

Minimizing the Dissipation of the IC

The four integrated clamping diodes dissipate the energy which is stored in the motor windings when outputs *Q* are switched off. This dissipation (P_D) is different for each of the motors and adds to the normal dissipation of the IC. If it is necessary to reduce P_D to prevent overheating of the IC, the integrated clamping diodes must be disconnected, by removing the connection from pin 13, and four discrete clamping diodes must be connected to the motor windings as shown in Fig. 3.

TECHNICAL DATA

Electrical Requirements of the Drive System

The various parameters are shown in Fig. 1.

Supply Characteristics

Control circuit supply voltage	V_P	9.5 – 18V (12V typ.)
Control circuit supply current at V_P = 12V	I_P	4.5mA typ.
Output circuit current	I_B	see Fig. 4
Output circuit bias voltage at pin 4	V_B	see Fig. 5
Motor supply voltage	V_m	1.5 – 18V (12V typ.)
Total motor current	I_m	700mA max.
Motor current in one stator	I_Q	350mA max.
Saturation voltage of output transistors at I_Q = 350mA (pins 6, 8, 9 and 11)	V_{sat}	< 1V

Input Levels R, S and T

HIGH	V_{RH}, V_{SH}, V_{TH}	7.5V to V_P
	I_{RH}, I_{SH}, I_{TH}	1μA typ.
LOW	V_{RL}, V_{SL}, V_{TL}	0 – 4.5V max.
	I_{RL}, I_{SL}, I_{TL}	−30μA typ.

Ratings

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).

Voltages

Voltage to pins 6, 8, 9, 11, 13 and 14	18V max.
Input voltages *R* (pin 3), *S* (pin 2) and *T* (pin 15)	V_P max.

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Currents
Output currents I_{Q1} (pin 6), 500mA max.
I_{Q2} (pin 8), I_{Q3} (pin 9) and I_{Q4} (pin 11)
Bias current into pin 4 I_B 90mA max.

Thermal Resistance
From junction to ambient $R_{th\ j\text{-}a}$ 70°C/W

Junction Temperature T_j 125°C Max.

STEPPER MOTOR CHARACTERISTICS

Each of the five stepper motors will have its own typical performance when it is connected as shown in Fig. 2 with the value of resistor R_B correctly selected. The typical torque/speed characteristics for the motors under these conditions, together with a typical dimensioned mechanical outline drawing is given in Fig. 6.

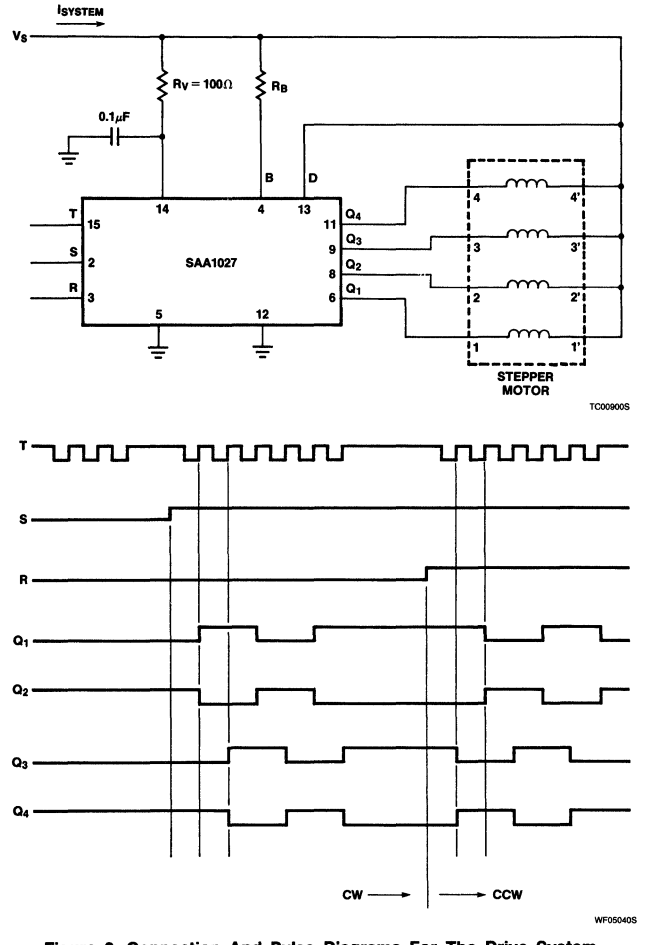

Figure 2. Connection And Pulse Diagrams For The Drive System.

Using the SAA1027 With Airpax Four-Phase Stepper Motors

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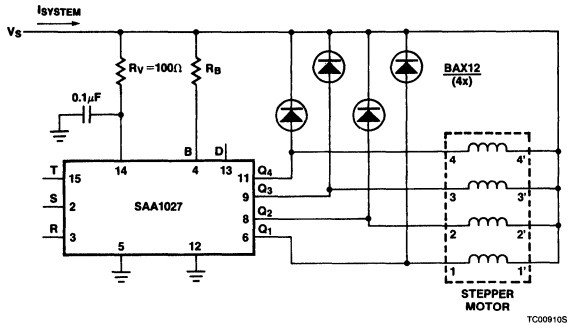

Figure 3. External Spike Suppression Diodes Being Used To Reduce The Dissipation Of The IC.

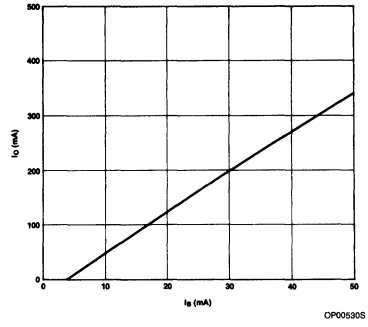

Figure 4. Relationship Between Output Current And Bias Current.

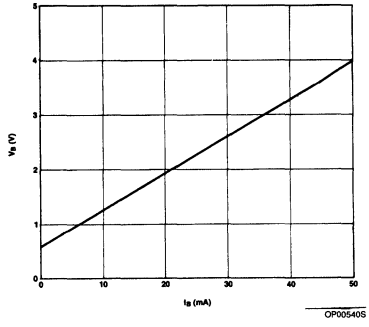

Figure 5. Relationship Between Bias Voltage At Pin 4 And Bias Current.

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Using the SAA1027 With Airpax Four-Phase Stepper Motors

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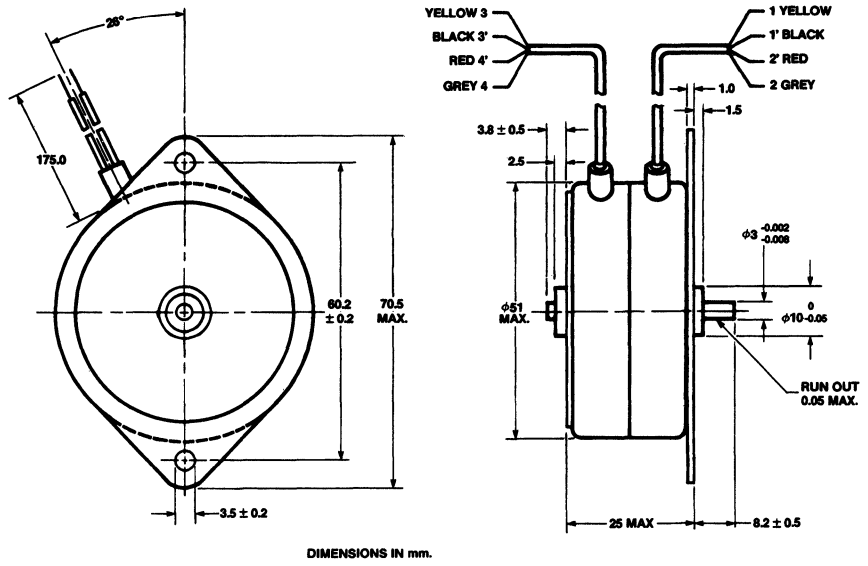

DIMENSIONS IN mm.

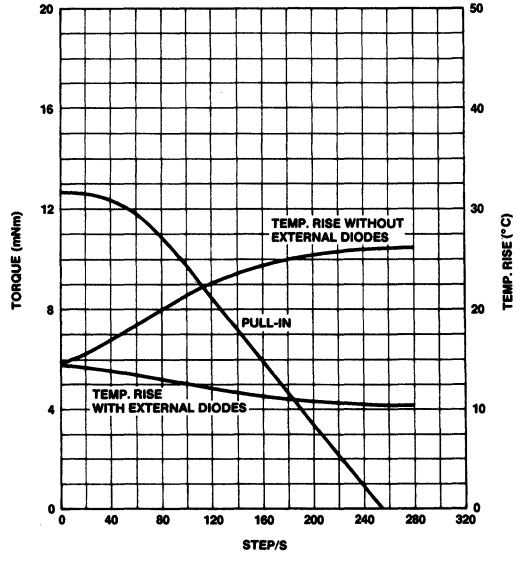

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Figure 6. Dimensions And Torque/Speed Characteristic For Stepper Motor 9904 112 04002, And The Temperature Rise Of The IC With And Without External Diodes.

Introduction to the Series-Resonant Power Supply AN128

E. B. G. NIJHOF and H. W. EVERS

There has long been a need for a smaller and more efficient alternative to the transformer/rectifier/series-stabiliser circuit for deriving a constant, easily-isolated d.c. supply from the mains. The development of high-voltage switching transistors, such as our BUX80 series, has allowed the construction of SMPS circuits which go a long way toward meeting this need but are still far from providing the ideal answer to the problem. The main drawbacks of the SMPS, when it is supplied from the 220 V/240 V mains, are limited efficiency due to switching losses and dissipation in dV/dt limiting RC networks, mains pollution and r.f.i. due to the generation of near-rectangular current waveforms, difficult transformer design, and the need for a complex control circuit to ensure continued operation with an open-circuit or short-circuit load. A circuit that overcomes these drawbacks is the series-resonant power supply (SRPS) which incorporates an inverter in which a semiconductor switch maintains sinusoidal oscillation in a series-resonant LC network. Although the high-frequency sinusoidal currents generated in an SRPS allow it to be made compact and efficient, with far less mains pollution and r.f.i. than the SMPS, its use has so far been restricted to low-voltage power supplies due to the lack of a suitable low-loss, high-voltage semiconductor switch.

Our recently introduced range of GTOs (gate turn-off Thyristors described in Ref. 1, 2 and 3) with their high VA ratings, fast switching and simple, transistor-like drive, now allow the construction of SRPS circuits which can operate from a rectified mains input and will undoubtedly replace the SMPS for controlled mains power conversion in applications such as television sets, industrial drives, fluorescent lighting systems, microwave and inductive cookers. The SRPS is also suitable for controlling the speed of d.c. series-wound motors in domestic appliances, and for reducing harmonic distortion in the mains supply by acting as a buffer between the mains and a d.c. power supply. The main advantages of the SRPS are:

- It is a more than 90% efficient power converter.
- It causes minimal mains pollution because the mains input current can be made sinusoidal 50 Hz in phase with the mains voltage.
- It can be built with a single, easily-designed, inductive element (transformer) which also provides mains isolation.
- It continues to operate with the output short-circuit. It also continues to supply a well-stabilised output when it is not connected to a load.
- It can be made self-starting and does not therefore need a small 50 Hz transformer to supply the control circuit for the GTO.

Survey of GTOs for SRPS

type number	V_{DRM} (V)	I_{TCRM} (A)	$I_{T(AV)}$ (A)	case
BT157	1500	10	2.2	TO-220
	1300	10	2.2	TO-220
BTW58	1500	25	6.5	TO-220
	1300	25	6.5	TO-220
	1000	25	6.5	TO-220
BTW59*	1500	50	12	TO-238
	1300	50	12	TO-238

* With isolated base.

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Introduction to the Series-Resonant Power Supply

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PRINCIPLES OF SRPS OPERATION

Figure 1 is the basic circuit of an SRPS, the operating principle of which depends on sinusoidal alternating current generation in the $L_1C_1C_O$ circuit. For guaranteed self-oscillation, there are two conditions regarding the values of the components. The inductance of L_S must be at least ten times that of L_1, and the value of C_O must be at least twice that of C_1. The operation of the circuit will first be described without a load connected to V_O and with a very brief conduction period for the GTO. This will be followed by a description of the circuit operation under similar conditions but with a longer conduction period for the GTO. Since the behaviour of the SRPS is complex (it sometimes functions as a fourth-order network), a complete analysis of the circuit is only possible with the aid of a computer; these theoretical descriptions are therefore only intended to give a basic understanding of the circuit operation and are followed by plots of the current and voltage waveforms derived by computer analysis of the basic circuit. The article concludes with a description of ten methods of connecting a load to the SRPS.

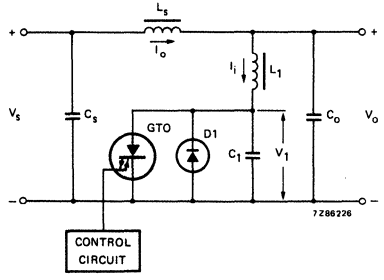

Fig.1 Basic SRPS circuit

Unloaded circuit with brief GTO conduction period

The waveforms for this mode of operation are given in Fig.2. Since $L_S \gg L_1$, and I_O is very small, the influence of L_S and I_O on the circuit behaviour can be disregarded for this simplified description.

In the steady state, with the GTO turned off, C_1 is charged to V_S. Assume that the GTO is turned on for the very short time necessary to just discharge C_1. Further assume that current I_1 is negligible during this brief on-time of the GTO. When the GTO is switched off, current I_1 oscillates sinusoidally about zero at the resonant frequency of

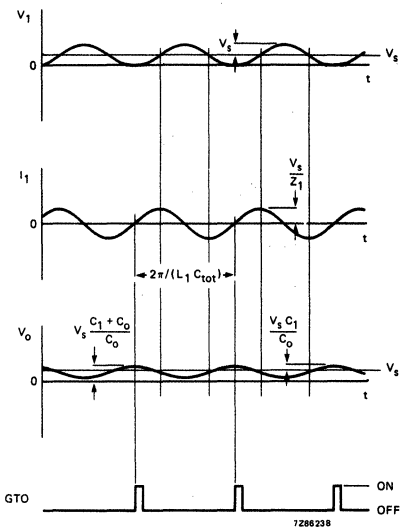

Fig.2 Waveforms of the basic SRPS for the shortest possible conduction time for the GTO

the circuit comprising L_1 together with C_O and C_1 in series:

$$\omega = \frac{1}{\sqrt{(L_1 C_{tot})}}$$

where

$$C_{tot} = \frac{C_1 C_O}{C_1 + C_O}$$

The peak oscillatory current is the supply voltage divided by the impedance of the resonant circuit (Z_1),

$$\hat{I}_1 = \frac{V_S}{Z_1} = V_S \sqrt{\frac{C_{tot}}{L_1}} \qquad (1)$$

which has an instantaneous value

$$I_1 = \frac{V_S}{Z_1} \sin \omega t$$

For stable self-oscillation of the circuit, the minimum level of V_1 must just reach zero during each cycle. The instantaneous value of V_1 is therefore given by

$$V_1 = V_S (1 - \cos \omega t)$$

$$\hat{V}_1 = 2V_S \qquad (2)$$

the a.c. component of which is

$$\hat{V}_{1\,a.c.} = \hat{V}_1 - V_S = V_S$$

This voltage therefore oscillates sinusoidally between 0 V

and $2V_S$ and has an average value equal to the supply voltage (V_S). Since the average value of the oscillatory current I_1 must therefore be zero, it is apparent that, as is to be expected, power is not drawn from the supply when the output from the circuit is unloaded.

The ratio V_O/V_1 is determined by the ratio of the values of C_1 and C_O. The peak value of V_O is

$$\hat{V}_O = V_S + \frac{\hat{V}_1 C_1}{2C_O} = V_S \frac{C_1 + C_O}{C_O}$$

the a.c. component of which is

$$\hat{V}_{O\,a.c.} = \hat{V}_O - V_S = V_S \frac{C_1}{C_O} \qquad (3)$$

Unloaded circuit with longer GTO conduction period

The waveforms for this mode of operation are given in Fig.3. If the conduction period of the GTO is made longer than that necessary to just discharge C_1, considerable current due to I_O and the discharge of C_O is flowing in L_1 at the turn-off instant. This value of I_1 will be denoted I_{off}. The peak oscillatory current V_S/Z_1 from equation (1) will now increase, in proportion to the ratio I_{off} to V_S/Z_1, by a factor

$$M = \sqrt{\left[\left(\frac{I_{off} Z_1}{V_S}\right)^2 + 1\right]}$$

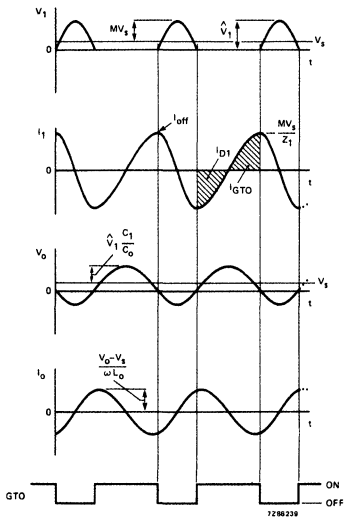

Fig.3 Waveforms for the longest possible conduction time for the GTO and V_1 = 1200 V max, V_S = 300 V, C_1 = 10 nF, C_O = 22 nF, L_O = 10 mH, L_1 = 1 mH, M = 3

The peak current through L_1 will therefore be

$$\hat{I}_1 = \frac{MV_S}{Z_1} \qquad (4)$$

The peak voltage across C_1 in Eq.(2) was V_S above its average value V_S. The rise of V_1 above V_S will now increase by the multiplying factor M, which gives

$$\hat{V}_1 = V_S + MV_S = V_S(M + 1) \qquad (5)$$

the a.c. component of which is

$$\hat{V}_{1\,a.c.} = MV_S$$

Solving Eq.(5) for the maximum multiplying factor in terms of the supply voltage and the maximum allowable peak voltage across the GTO gives

$$M_{max} = \frac{\hat{V}_1}{V_S} - 1 \qquad (6)$$

The a.c. component of the output voltage is $\hat{V}_{1\,a.c.}$ multiplied by the ratio C_1/C_O, which gives

$$\hat{V}_{O\,a.c.} = \frac{\hat{V}_{1\,a.c.}\, C_1}{C_O} = \frac{MV_S C_1}{C_O} \qquad (7)$$

Voltage control range of the basic SRPS

Assuming that V_S is the rectified mains voltage (300 V) and that the maximum peak voltage permitted across the GTO ($\hat{V}_1$) is 1200 V, then from Eq.(6) the maximum multiplying factor is 3 and, from Eq.(4), the maximum peak current through L_1 is

$$\hat{I}_1 = \frac{3V_S}{Z_1} \qquad (8)$$

Comparing Eq.(1) and (8) shows that the peak current through L_1 increases threefold when the conduction period of the GTO is increased to the maximum allowed by the permitted peak voltage across the GTO ($\hat{V}_1$). Comparing Eq.(2) and (5) shows that, with M = 3, the peak voltage across the GTO increases from $2V_S$ = 600 V to $4V_S$ = 1200 V when the conduction period of the GTO is changed from minimum to maximum. Comparing Eq.(3) and (7) shows that, with C_1/C_O = 0.5, the control range for the a.c. component of V_O is

$$V_{O\,a.c.}\ min = 0.5\,V_S = 150\ V$$

$$V_{O\,a.c.}\ max = 1.5\,V_S = 450\ V$$

The circuit can therefore be used as a power converter with its output voltage controllable over a 3:1 range by varying the conduction period of the GTO.

Alternatively, for a lower supply voltage such as V_S = 100 V, and the same maximum peak voltage $\hat{V}_1$ = 1200 V, the maximum multiplying factor from Eq.(6) is 11. Solving

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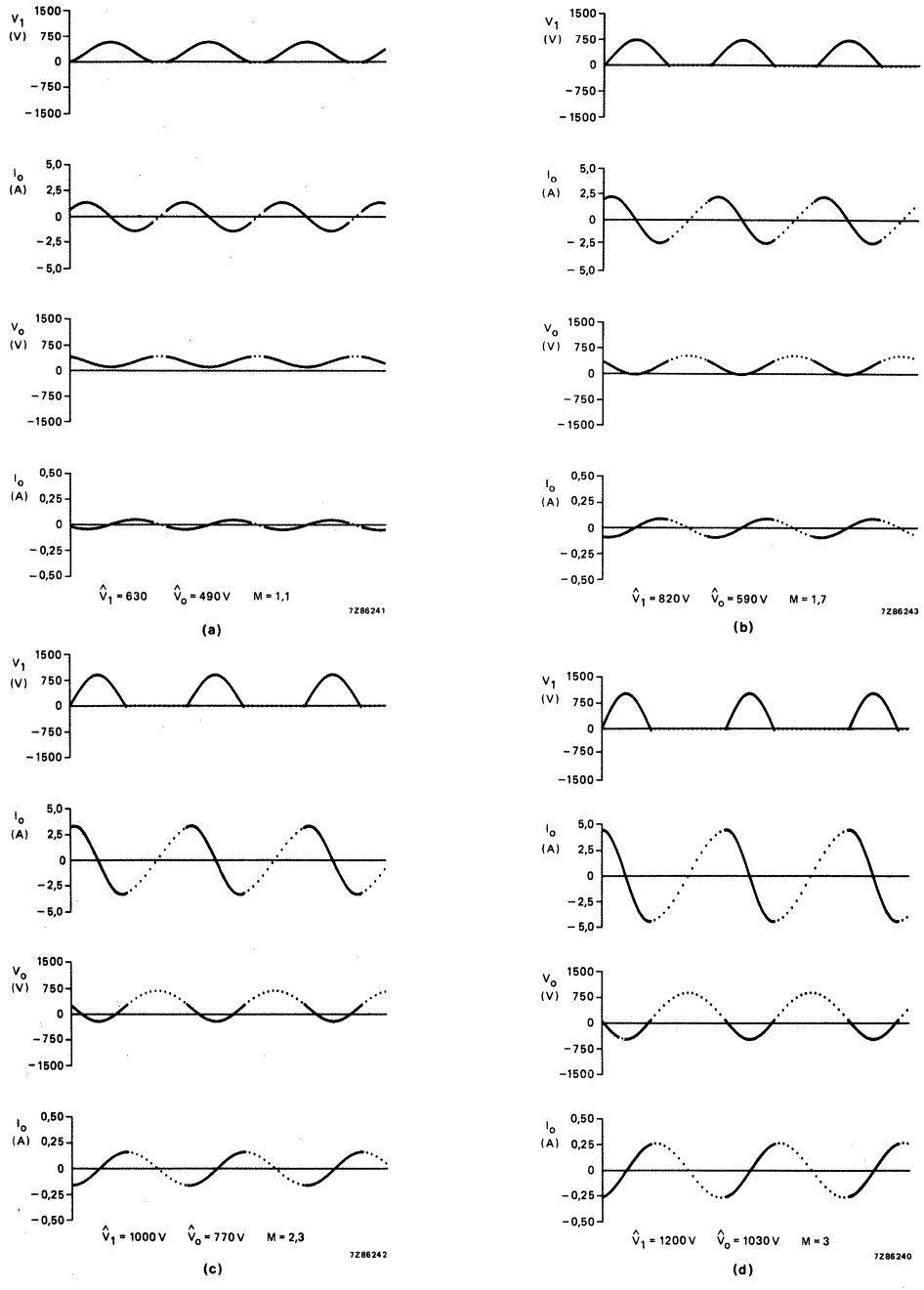


Fig.4 Computer plots of the waveforms in the circuit of Fig.1 with V_s = 300 V d.c., L_o = 10 mH, L_1 = 1 mH, C_o = 20 nF, C_1 = 10 nF. The dotted sections are the conduction period of the GTO, which is the maximum allowed by the V_1 specification

Eq.(2) and (5) for V_S shows that the variation of supply voltage (V_S) that can be compensated by variation of the conduction period of the GTO is:

$$V_{S\,min} = \frac{\hat{V}_1}{M+1} = 100\,V \qquad V_{S\,max} = \frac{\hat{V}_1}{2} = 600\,V$$

The SRPS output voltage can therefore be stabilised against a 6:1 d.c. supply voltage variation by varying the conduction period of the GTO.

Computer plot of the SRPS voltage and currents

As shown in Fig.4, a computer program has been used to plot the exact time functions for I_O, I_1, V_O and V_1 with V_S = 300 V d.c. and components values L_S = 10 mH, L_1 = 1 mH C_O = 20 nF and C_1 = 10 nF. The computer plots have been made for peak values of V_O of 490 V, 590 V, 770 V and 1030 V. Subtracting V_S = 300 V from these figures gives the a.c. component of V_O, which is about 190 V, 290 V, 470 V and 720 V respectively. This shows that the available output voltage control range for V_S = 300 V and V_1 max. = 1200 V is at least 3.8:1 instead of 3:1 as calculated in Eq.(3) and (7). This is due to the fact that the voltages across the capacitors in the oscillatory circuit are almost 180° out of phase so that the voltage division between them is not directly proportional to their values. The plots also indicate that the operating frequency decreases as the conducting time of the GTO is increased.

Extracting power from the SRPS

There are three basic methods of extracting power from the SRPS. They are:

- From capacitor C_O, via a diode, to an output electrolytic capacitor. Since the output voltage V_O a.c. is superimposed on the input d.c. level V_S, the voltage across the electrolytic capacitor will always exceed V_S. The circuit is therefore an up-converter and its main use is as a buffer between the mains and a d.c. power supply unit.
- From capacitor C_O via a capacitor which blocks the d.c. component of V_O so that pure a.c. is available at the output. This circuit is suitable for driving resistive loads and fluorescent lighting tubes. If the output from the blocking capacitor is rectified in a voltage doubler circuit, this type of SRPS is suitable for controlling the speed of a series-wound d.c. motor.
- By replacing inductor L_S with a transformer. This arrangement gives the best performance because it gives very good mains isolation and the load can be correctly matched to the SRPS by adjustment of the turns ratio of the transformer. This type of circuit can drive resistive or rectifier loads and can also be used as a supply for fluorescent tubes. For rectifier loads, however, the leakage inductance of the transformer must be made very low; for example, by using sandwiched windings. The final part of this article shows how inductor L_1 can be integrated with the transformer to overcome this problem and create an SRPS with a single inductive component.

PRACTICAL SRPS CIRCUITS WITHOUT MAINS-ISOLATION

Direct-coupled SRPS up-converter

The circuit of this type of SRPS is given in Fig.5. Diode D_O half-wave rectifies V_O and feeds the resultant half-sinewaves to output electrolytic C_O. Since the average value of V_O is V_S, the rectified half-sinewaves at the output are superimposed on the d.c. input voltage and the d.c. output voltage must necessarily exceed this level. The circuit is therefore an up-converter. The percentage of the total output power which has to be converted by the series-resonant circuit is $(V_O - V_S)/V_O$. For V_S = 200 V (average voltage of full-wave rectified 220 V mains) and $V_{O\,a.c.}$ = 500 V, this amounts to only 60 % of the total output power. This, together with the inherent high efficiency of the SRPS (about 95 % at V_S = 200 V d.c.), allows the circuit to feed some current to the load, even when the input voltage is as low as 10 % of the output voltage. For $V_{O\,a.c.}$ = 500 V to 600 V, the full-wave rectified mains input need not therefore be smoothed and can be obtained directly from a bridge rectifier followed by a low value decoupling capacitor (a few μF). This arrangement results in an SRPS up-converter with a well-stabilised d.c. output with a low level of superimposed 100 Hz ripple. Since the 50 Hz mains current flowing via the bridge rectifier without a high value smoothing capacitor is sinusoidal, the circuit can convert unlimited power without exceeding the limits of mains harmonic generation specified for domestic equipment in CENELEC specification EN 50 006.

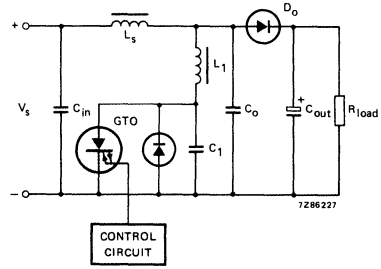


Fig.5 SRPS up-converter

The foregoing considerations indicate that the main use for this type of SRPS is for reducing mains distortion by acting as a buffer between the a.c. mains supply and a 500 V to 600 V d.c. power supply of more than 500 W.

Capacitively-coupled SRPS circuits

In capacitively-coupled SRPS circuits, the d.c. component of voltage V_O is blocked by a capacitor between C_O and the output rectifier. The circuit is given in Fig.6 which shows three methods of rectifying the a.c. component V_O.

Circuit 1. In circuit 1 of Fig.6, the a.c. component of V_O is rectified in a voltage doubler circuit that applies a positive d.c. voltage to the load. Like the previously described up-converter, this circuit works best with a d.c. output of more than 500 V, but has the added advantage that it is immune to output short-circuit. The main use of circuit 1 is speed control of a series d.c. motor connected as shown in Fig.7. Since inductor L_S has now been replaced by the series-connected armature and field windings of the motor, the SRPS has an effective input voltage of V_S minus the back e.m.f. Since the back e.m.f. is proportional to the current through the motor at a given speed, it is not necessary to use a high value capacitor to smooth the rectified mains input. The current flowing in the 50 Hz mains can therefore be made sinusoidal so that mains pollution is minimal. The range of back e.m.f. must not exceed about 75 % of supply voltage V_S so that the SRPS can still supply a reasonable amount of current when the motor is running at full speed.

Circuit 2. Circuit 2 of Fig.6 is similar to circuit 1 except that the output rectifier/voltage doubler is connected to provide a negative d.c. output voltage. The possible uses for this circuit are few.

Circuit 3. Circuit 3 of Fig.6 is again similar to circuits 1 and 2 except that the output is bridge-rectified. Since the bridge rectifier provides half the average output voltage of a voltage doubler rectifier, the minimum peak value for the d.c. output can be reduced to about 250 V. A disadvantage of the circuit however, is that the output is floating with respect to the return line of the input voltage.

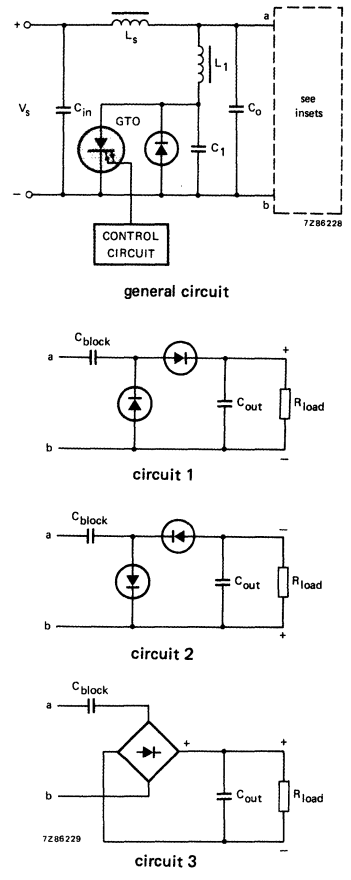


Fig.6 SRPS circuits with capacitively coupled output

SRPS CIRCUITS WITH MAINS ISOLATION

Since capacitor C_{in} has a much higher value than C_O, C_O is effectively in parallel with L_S so that V_O appears across this inductor. If mains isolation is required, L_S can therefore be replaced by a transformer with output rectifier connected to the secondary winding (Fig.8). The manner in which the rectifier and transformer are connected then determines the mode of operation, i.e. power transferred to the load

- when the current in the primary winding of the transformer is positive (forward mode, circuit 1)
- when the current in the primary is negative (flyback mode, circuit 2)
- when the current in the primary is positive and when it is negative (forward flyback mode, circuit 3).

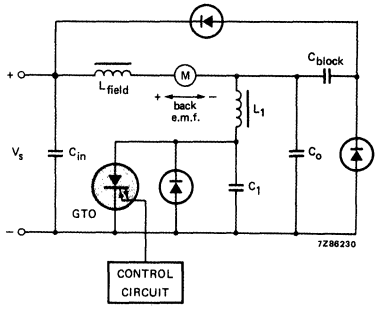
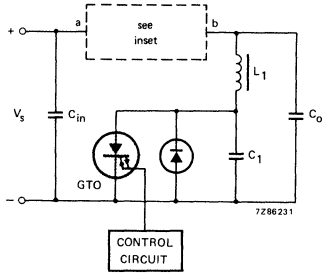
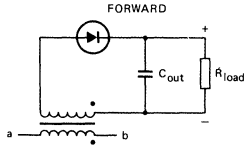


Fig.7 SRPS with capacitively coupled output controlling the speed of a d.c. series-wound motor

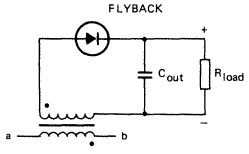
In circuit 3, a bridge rectifier can also be used with an untapped secondary winding.

In addition to driving rectifier loads via a transformer with low leakage inductance, these circuits with transformer-coupled output are also suitable for driving a resistive load or a load that behaves like a voltage source, for example, a fluorescent lamp or a magnetron in a microwave cooker. The best performance is obtained with a d.c. output of about 300 V.

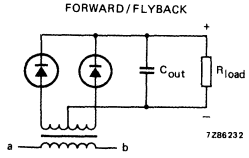




circuit 1



circuit 2



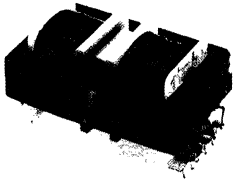
circuit 3

Fig.8 SRPS circuits with transformer coupled output

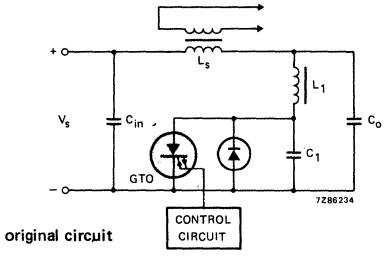
SRPS with a single inductive component (transformer)

In the circuits shown in Fig.8, inductor L_1 is rather bulky because, at operating frequencies of about 50 kHz, the flux swing in the core is quite large. It is therefore necessary to use a large core to prevent saturation and consequent overheating due to hysteresis losses. The core heating problem can be completely overcome by constructing the output transformer in such a manner that L_S is formed by the primary self-inductance and magnetising inductance of the transformer, and L_1 is formed by the primary and secondary leakage inductances. The flux swing of the transformer core is then quite small and the hysteresis losses are low.

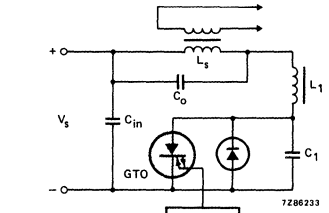
Figure 9 shows how inductor L_1 can be integrated with the output transformer. Firstly, since C_{in} is a much higher value than C_O, C_O is effectively in parallel with the primary winding of the transformer and can therefore be connected in this position. Secondly, if the value of C_O is multiplied by the square of the turns-ratio of the transformer, it can be connected in parallel with the secondary winding. Finally, since there is now no connection to the junction of L_S and L_1, L_1 can be integrated with the output transformer. This final step is clarified by the equivalent T-circuit of the transformer given in Fig.10. Since a requirement for guaranteed self-oscillation of the SRPS is that the value of L_S is at least ten times that of L_1, the minimum coefficient of coupling for the transformer is $\geqslant 0.8$. A transformer with sufficient leakage inductance can easily be constructed on a pair of ferroxcube U-cores with the primary wound round one pole and the secondary wound round the other. If the external magnetic field with this type of construction is too great (for example, in a television receiver), the primary and secondary windings can be stacked on the gapped centre pole of a pair of E-cores. Experiments have shown that when this type of transformer is installed in a working SRPS and positioned within 4 cm of the deflection coils of a 26-inch CTV set with a 30AX deflection system, there is no perceptible distortion of the raster. If the transformer is positioned within 4 cm of the most sensitive part of the tube (cathode, grid 1 and 2 area), the maximum distortion of the raster is 1 mm.



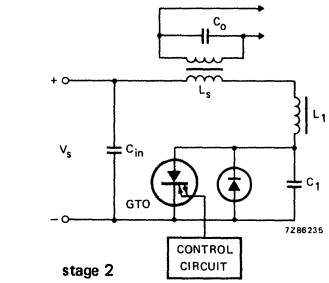
Typical construction of a mains-isolated SRPS output transformer in which the leakage inductance is used for L_S. This transformer is for a 150 W to 200 W power supply operating at a frequency of 30 – 40 kHz



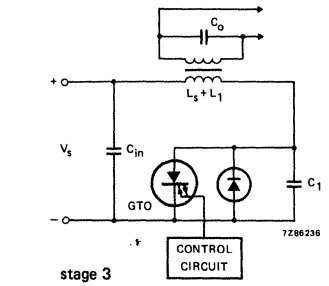
original circuit



stage 1

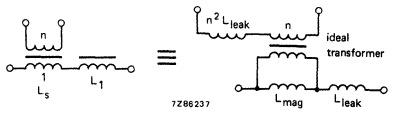


stage 2



stage 3

Fig.9 The three stages of integrating inductor L_1 with the output transformer of an SRPS



Approximate relations in the equivalent circuit ($L_s \geq 10L_1$)

$L_1 = 2L_{leak}$

$L_s = L_{mag}$

Fig.10 Transformer equivalent T-circuit with ideal transformation

An important advantage of the SRPS with a single inductive element is that it is inherently immune to a short-circuited output. It is therefore self-starting, even with zero volts across the output capacitor, so it is not necessary to use a separate 50 Hz transformer to provide a supply for the GTO control circuit.

The single-transformer SRPS can be used in any of the modes of operation illustrated in Fig.8 and can provide controlled power for all the previously mentioned types of load. Because the design of SRPS circuits is complex, we have calculated the time functions for the variables V_O, V_1, I_O and I_1 and used them in a closed-loop computer program to calculate the steady-state conditions for any set of input conditions. The computer program has also been used to construct a set of five universally-applicable graphs as a design aid for SRPS circuits.

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1. Burgum, F. J., Nijhof, E. B. G. and Woodworth, A., *Gate turn-off switch*, Electronic Components and Applications, Vol. 2, No. 4, August 1980.
2. Woodworth, A., *Understanding GTO data as an aid to circuit design*, Electronic Components and Applications, Vol. 3, No. 3, May 1981.
3. Burgum, F. J., *Basic GTO drive circuits*, Electronic Components and Applications, Vol. 3, No. 4, August 1981.

Design of Static Switching Circuits Using TDA1024 AN129

An a.c. static switch is an entirely electronic circuit which uses a controlled rectifier (triac or thyristor) as its switching element. It is considerably more reliable than a mechanical switch or contractor because it has no moving parts and is therefore not subject to wear or contact erosion due to arcing. Furthermore, it can be silently and safely operated by a very low power mains-isolated circuit such as a simple mechanical contact, a thermistor bridge, or the output from a logic element.

Static switches can be designed for either synchronous or asynchronous operation. Asynchronous switches are the less expensive of the two types but, since they can be operated at any instant during the a.c. voltage cycle, they can cause a rapid current rise in a switched resistive load and thereby generate considerable r.f. interference. This disadvantage can be overcome by using a switch that triggers the power switching element when the switched a.c. voltage passes through zero. Such a synchronous switch, however, tends to become expensive when constructed from discrete components because it must incorporate complex circuitry for detecting the a.c. voltage zero crossing instant and synchronizing the switching action.

The TDA1024 provides an economic solution to this problem.

DESCRIPTION OF THE TDA1024

The TDA1024 is an 8-pin dual-in-line integrated circuit which, together with a few peripheral components, can be used to construct on/off static switch circuits. It incorporates the following functions (see Figs 1 and 2):

- a comparator with Schmitt-trigger action. This circuit compares the control voltage at pin 5 with the reference voltage at pin 4 and switches on when the control voltage exceeds the reference voltage. The hysteresis of the circuit is adjustable between 20mV and 300mV by selection of the value of the resistor connected between pin 3 of the TDA1024 and the negative supply line.
- an input buffer circuit with high input impedance and low output impedance. This circuit presents a low impedance to the comparator input so that the hysteresis of the circuit is independent of variations of the input voltage.
- a d.c. supply circuit which provides a zener-limited nominal 6.5V supply, at a current of up to 30mA, for application to the input bridge.
- a zero-crossing detector which produces an output when the sinusoidal voltage applied to pin 6 passes through zero.
- a control gate which inhibits the output trigger pulse from the TDA1024 unless there are outputs from both the zero-crossing detector and the comparator.
- an output stage which delivers a positive-going, mains-synchronized triac trigger pulse whenever the control gate is activated. The output from this stage is current-limited and protected against short-circuit. Since, for zero voltage switching, the current and voltage in the load must be in phase, the applications of the TDA1024 described in this publication are restricted to the switching of resistive loads.

The TDA1024 is mainly intended for applications such as thermostatic control of:

- central heating installations;
- washing machine heaters;
- water heaters;
- smoothing irons;
- industrial heating equipment.

The circuit is also suitable for use in on/off lighting control systems. The input can be derived from a resistance bridge or from a logic element, either directly or via a photocoupler if mains isolation is essential.

PERIPHERAL COMPONENTS

This section will show how to select the values for the peripheral components so as to ensure correct operation of the TDA1024 under worst-case conditions with regard to operating conditions such as mains voltage, triac characteristics and load characteristics.

To aid the designer in selecting component values, larger versions of all the curves shown in this section are available on request.

TRIGGER PULSE WIDTH AS A FUNCTION OF TRIAC LOAD

The main advantage of triggering a triac at the instant when the applied voltage passes through zero is that this mode of operation renders the use of r.f. suppression components unnecessary. The trigger pulse (Fig. 3) must commence before the triac current (I_T) falls below the holding level and must continue until it rises above the latching level. Since, in general, the latching current (I_L) of a triac is 20% higher than its holding current (I_H), the minimum width for the trigger pulse is equal to twice

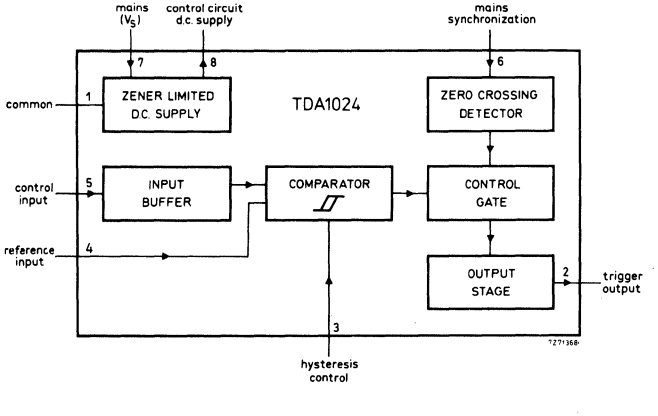


Figure 1. Block Diagram of the TDA1024.

Design of Static Switching Circuits Using TDA1024

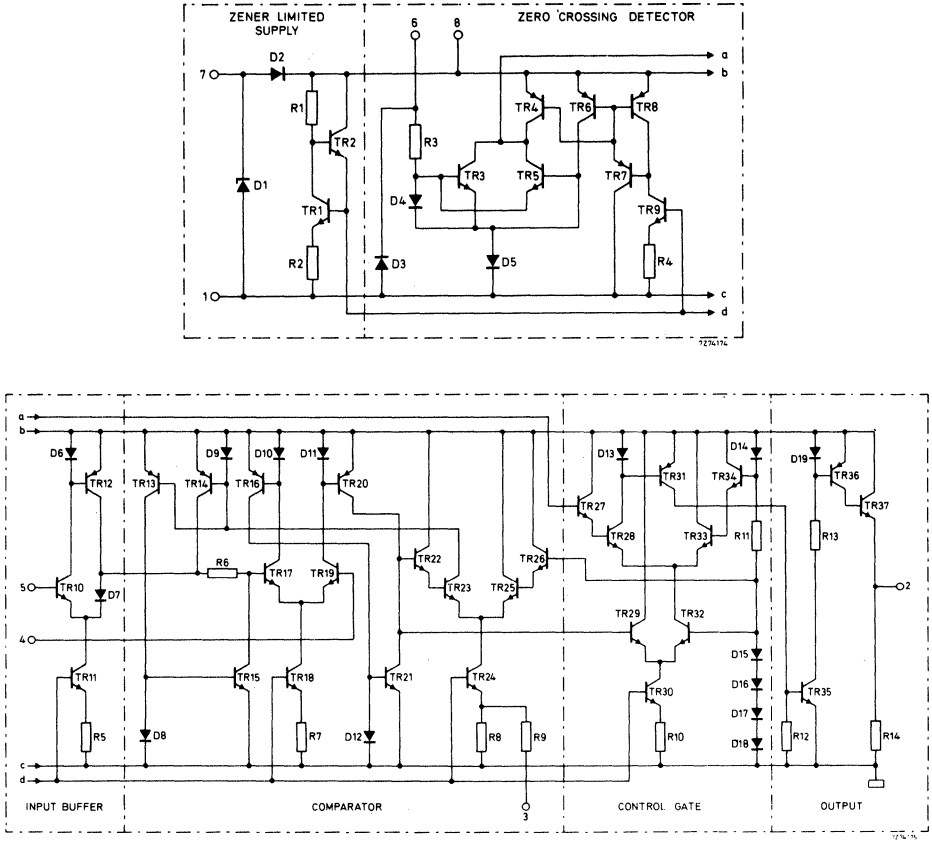


Figure 2. Circuit Diagram of the TDA1024.

the time taken for the triac current to rise from zero to the latching level.

The current passed by the triac is a function of its on-state voltage, the load resistance, and the applied a.c. voltage. The required trigger pulse width (t_p) is therefore a function of:

- the latching current of the triac (I_L);
- the applied a.c. voltage (V);
- the load resistance (R);
- the on-state voltage of the traic (V_T).

The following equation can be derived:

$$t_{p\ min} = \frac{2\,(I_L R + V_T)}{d\,(\hat{V} \sin \omega t)/dt} \qquad \text{at } t = 0.$$

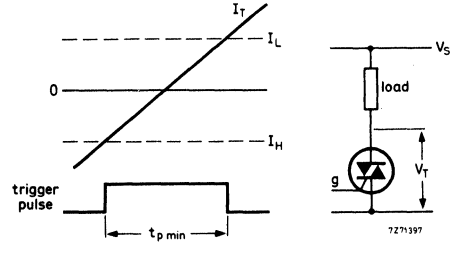


Figure 3. Definition of Minimum Trigger Pulse Width for Mains Zero-Point Triggering.

Assuming that the load resistance has a tolerance of ±5%, the a.c. voltage variation is ±10% and the on-state voltage of the triac is a maximum of 2V at I_L, the minimum width of the trigger pulse in the worst case is:

$$t_{p\ min} = \frac{2.1 I_L R + 4}{0.9 \hat{V}_\omega}$$

in which

$$R = \frac{V^2}{\text{power being controlled (P)}}$$

Figure 4 shows t_p as a function of P, with I_L as a parameter, at four a.c. voltages.

SYNCHRONIZATION RESISTOR VALUE AS A FUNCTION OF REQUIRED PULSE WIDTH

The minimum width of the trigger pulse available from pin 2 of the TDA1024 is specified in the published data as 130μs with a synchronization current into pin 6 (I_6) of 1mA at 50Hz, and a d.c. output voltage at pin 8 of 5.5V (a.c. input voltage to pin 7: 220V, 50Hz).

The general expression for the minimum width of the trigger pulse as a function of the current into pin 6 (see Fig. 5) is:

$$t_{p\ min} = \frac{t_{p\ min}\ \text{at}\ I_6 = 1mA}{I_{6\ max} \times 10^3}$$

$$= \frac{0.13 \times 10^{-6} \times R_{S\ min}}{V_{max}}$$

Assuming a tolerance of ±5% for R_S and ±10% for the supply voltage, it would appear that the worst-case (lowest) value for $t_{p\ min}$ is given by:

$$t_{p\ min} = \frac{0.13 \times 10^{-6} \times 0.95\ R_S}{1.1V}$$

This, however, is not realistic because the longest trigger pulse is required when the rate of change of the triac current is slowest, i.e. when the applied voltage is minimum (see Fig. 3). The true worst case therefore occurs when the applied voltage is minimum and the pulse length due to R_S is minimum (minimum R_S value). This is given by:

$$t_{p\ min} = \frac{0.13 \times 10^{-6} \times 0.95\ R_S}{0.9V}$$

$$= \frac{0.137\ R_S \times 10^{-6}}{V}$$

Figure 6 shows the value of R_S as a function of the required trigger pulse width with the applied a.c. voltage as a parameter.

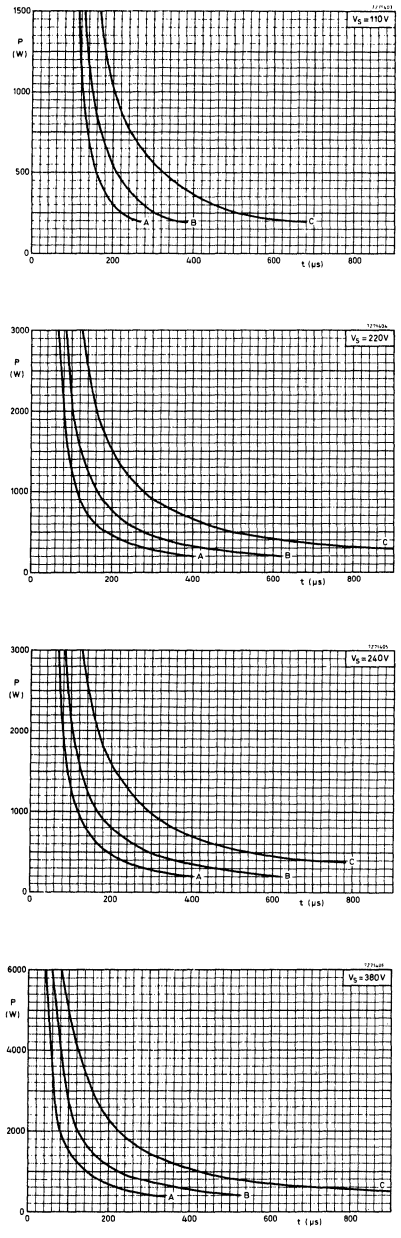


Figure 4. Minimum Pulse Width as a Function of Switched Power for Four Supply Voltages, with Latching Current as a Parameter: Curve A, I_L = 60mA; Curve B, I_L = 100mA; Curve C, I_L = 200mA.

Design of Static Switching Circuits Using TDA1024 AN129

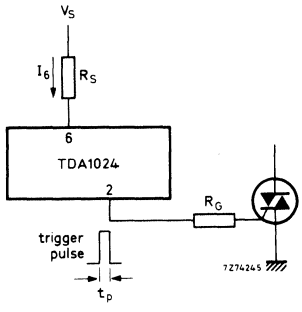


Figure 5. Definition of the Value of the Mains Synchronization Resistor as a Function of the Required Trigger Pulse Width.

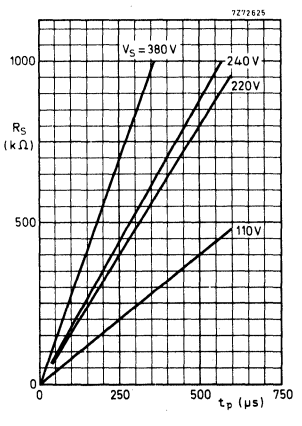


Figure 6. Synchronization Resistor Value as a Function of Required Trigger Pulse Width with Applied a.c. Voltage as a Parameter.

GATE RESISTOR VALUE AS A FUNCTION OF OUTPUT V/I CHARACTERISTIC AND TRIAC GATE CHARACTERISTICS

The maximum amplitude of the pulse at the output (pin 2) of the TDA1024 is specified in the published data as being not less than 4V at an output current of 100mA. Since the output stage is a voltage stabilizer, the output voltage remains at 4V minimum for all output currents below 100mA. If an attempt is made to draw a higher current at this output voltage, the output current is limited to 100mA. This limiting action does, in fact, render a gate current limiting resistor unnecessary.

Its use is, however, recommended to limit the gate current to its minimum value and thereby reduce the power dissipated by mains dropping resistor R_d by reducing the overall current consumption.

The rectangular output V/I characteristic of the TDA1024 is shown in Fig. 7. Load lines for various values of gate resistor have been plotted on this diagram so that the maximum value of gate resistor (minimum gate current) can be selected by plotting horizontal and vertical lines to represent the required minimum gate current and voltage that will reliably trigger all triacs of a particular type.

If gate resistor values are to be calculated, Fig. 8 shows that:

$$R_G = \frac{V_2 - V_G}{I_G}$$

therefore,

$$R_{G\ max} = \frac{4 - V_G}{I_G}$$

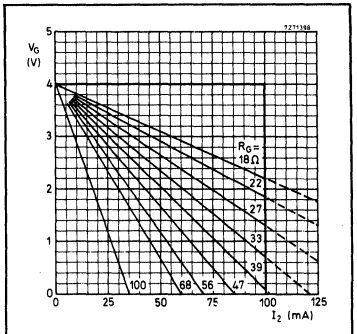


Figure 7. Gate Voltage as a Function of Output Current with Gate Resistor Load Lines. Example: for V_G = 1.5V and I_2 = 62mA, R_G = 39kΩ.

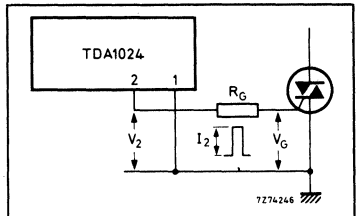


Figure 8. Definition of the Value of the Gate Resistor as a Function of the Output V/I Characteristic of the TDA1024 and the Characteristic of the Triac.

From the last equation, it is obvious that the plots of Fig. 7 will result in an indication of the maximum value for the gate resistor. If the plotted value falls between two load lines, the lower value must be selected for the gate resistor.

COMPARATOR HYSTERESIS AS A FUNCTION OF PERIPHERAL RESISTOR R_h

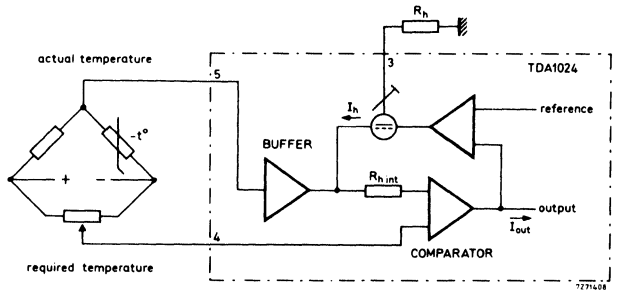
The comparator in the TDA1024 compares the input voltages at pins 4 and 5, and operates with Schmitt-trigger action and built-in hysteresis. The hysteresis increases the noise immunity of the circuit and prevents half-waving. It is adjustable between 20mV and 300mV by selection of the value of a resistor connected between pin 3 and the common return line. A diagram of the circuit is given Fig. 9 together with the transfer characteristic of the comparator.

The current delivered by the current source (I_h) can be set by selecting a value for peripheral resistor R_h. Current I_h defines the voltage across resistor $R_{h\ int}$ and therefore determines the voltage differential (the hysteresis) required between pins 4 and 5 of the TDA1024 to initiate output trigger pulses.

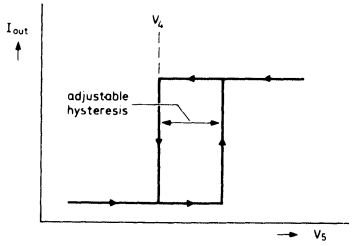
The typical hysteresis of the circuit is plotted as a function of the value of R_h in Fig. 10.

DETERMINATION OF MAXIMUM AVERAGE OUTPUT CURRENT AS A FUNCTION OF R_G WITH R_S AS A PARAMETER

In this section, the maximum average output current of the TDA1024 will be calculated so that the minimum required supply current can be determined in the next section. Since the *minimum* required supply current is to be calculated in the next section, this section will show how to calculate the maximum output current at *minimum* supply voltage, and will transform the result into the maximum average output current that can occur under conditions of maximum trigger pulse duty cycle. This procedure is feasible because all the parameters given in the published data are guaranteed at the minimum supply voltage (V_8 = 5.5V). Making the calculation at minimum supply voltage is also valid because making it at maximum supply voltage would result in subsequent selection of too high a value for the supply dropping resistor and consequent unnecessary power dissipation.



(a)



(b)

Figure 9. Hysteresis of the Comparator as a Function of R_h. The Comparator is Shown in (a) and the Transfer Characteristic in (b).

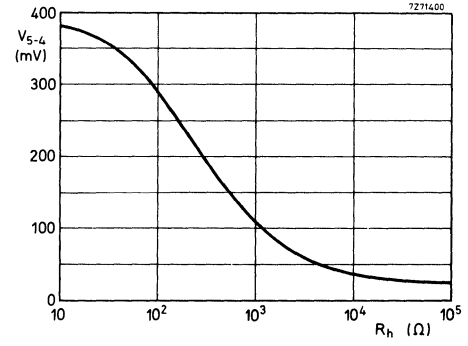


Figure 10. Comparator Hysteresis as a Function of the Value of Peripheral Resistor R_h.

Assuming a ±5% tolerance for gate resistor R_G, the worst-case peak output current from pin 2 is:

$$I_{2\,max} = \frac{V_{2\,max\ at\ V_{8\,min}}}{0.95R_G} = \frac{4.7}{0.95R_G} = \frac{4.947}{R_G}$$

Assuming a ±5% tolerance for R_S and a ±10% tolerance for the supply voltage, the maximum pulse width is:

$$t_{p\,max} = \frac{t_{p\,max\ at\ I_6\,=\,1\,mA}}{10^3} \times \frac{1.05R_S}{0.9V}$$

$$= \frac{0.265 \times 10^{-6} \times 1.167R_S}{V}$$

$$= \frac{0.309R_S \times 10^{-6}}{V}$$

The maximum trigger pulse duty cycle is:

$$\delta_{max} = \frac{t_{p\,max}}{\text{half 50Hz period}}$$

The worst-case maximum average current output from pin 2 is:

$$I_{2(av)\,max} = I_{2\,max} \times \delta_{max}$$

$$= \frac{4.947}{R_G} \times \frac{0.309R_S \times 10^{-4}}{V}$$

$$= \frac{1.53R_S \times 10^{-4}}{R_G V}$$

The value of $I_{2(av)\,max}$ is plotted as a function of the value of R_G, with the value of R_S as a parameter, for four 50Hz supply voltages in Figs 11 to 14.

MINIMUM REQUIRED SUPPLY CURRENT (I_7) AS A FUNCTION OF OUTPUT CURRENT (I_2) WITH HYSTERESIS SETTING AS A PARAMETER

The minimum supply current required at pin 7 of the TDA1024 is the sum of the following currents:

- the maximum average output current;
- the current drawn by the TDA1024 internal circuits;
- the current drawn by the input circuit components connected to pin 8 of the TDA1024.

The maximum average output current was defined in the previous section.

The current drawn by the internal circuits of the TDA1024 depends on the hysteresis control current drawn from pin 3. At $I_3 = 0$, I_{IC} = 1.8mA (minimum hysteresis), and at $V_3 = 0$, I_{IC} = 3mA (maximum hysteresis). Calculations and measurements have

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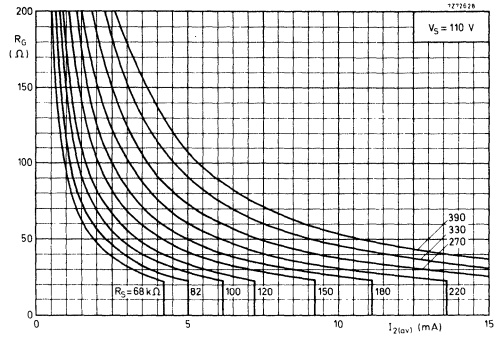

Figure 11. Maximum Average Trigger Current as a Function of the Value of R_G with the Value of R_S as a Parameter.

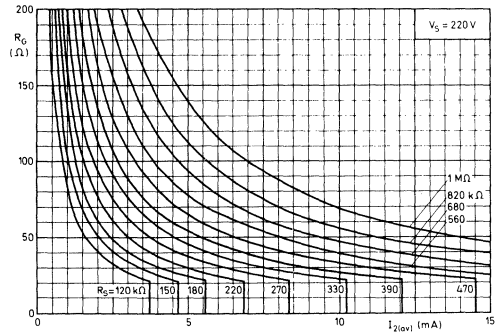

Figure 12. Maximum Average Trigger Current as a Function of the Value of R_G with the Value of R_S as a Parameter.

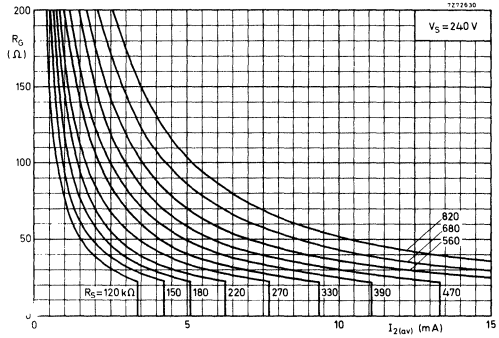

Figure 13. Maximum Average Trigger Current as a Function of the Value of R_G with the Value of R_S as a Parameter.

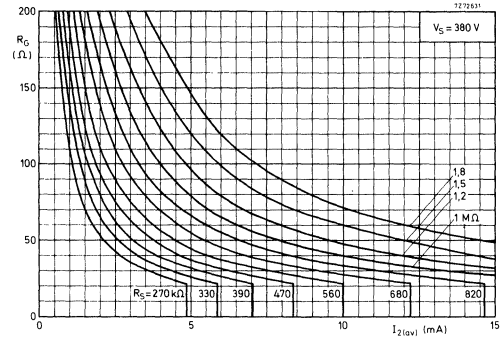

Figure 14. Maximum Average Trigger Current as a Function of the Value of R_G with the Value of R_S as a Parameter.

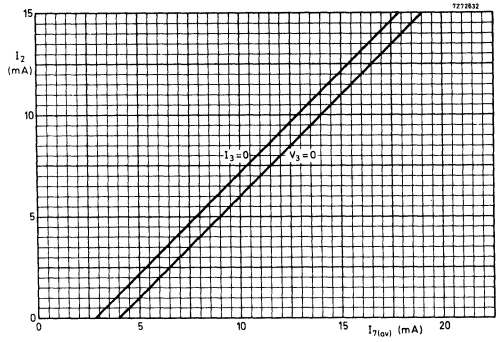

Figure 15. Minimum Required Supply Current as a Function of Maximum Average Trigger Current, with Hysteresis Setting as a Parameter.

shown that, with the hysteresis set to maximum, and input conditions such that $V_5 > V_4$ (maximum total current consumption), $I_{IC} = 3mA$.

With minimum hysteresis, the minimum required supply current is:

$I_{7\ min} = I_{2(av)\ max} + 0.0018 + I_{bridge}$.

With maximum hysteresis, the minimum required supply current is:

$I_{7\ min} = I_{2(av)\ max} + 0.003 + I_{bridge}$.

The minimum required supply current is shown as a function of the maximum average output current, with the hysteresis setting as a parameter in Fig. 15. The bridge current is assumed to be 1mA in this graph.

VALUE OF THE MAINS DROPPING RESISTOR AS A FUNCTION OF THE MINIMUM REQUIRED SUPPLY CURRENT WITH THE SUPPLY VOLTAGE AS A PARAMETER

The value of the mains dropping resistor (R_d) must be such that the average supply current to pin 7 of the TDA1024 is at least equal to the minimum required value defined in the previous section. Figure 16 shows the diagram of the supply circuit and gives the mains voltage waveform.

During the positive excursion of the mains voltage, the current supplied to the TDA1024 and the electrolytic capacitor via R_d is given by:

$$I_{7(av)} = \frac{1}{2\pi} \int_{a1}^{a2} \left(\frac{\hat{V} \sin a - V_7}{R_d} \right) da.$$

Assuming 10% mains voltage variation, 10% tolerance for R_d, and a maximum of 8.2V at pin 7, the worst-case condition (minimum current, maximum resistance) is given by:

$$I_{7\ min} = \frac{1}{2\pi} \int_{a1}^{a2} \left[\frac{(0.9 \times \hat{V} \sin a) - 8.2}{1.1 R_d} \right] da$$

in which $a_1 = \pi - a_2 = \arcsin 8.2/0.9V = \arcsin 9.1/V$.

This expression has been computed, and the results plotted graphically, for four values of r.m.s. mains voltage in Fig. 17.

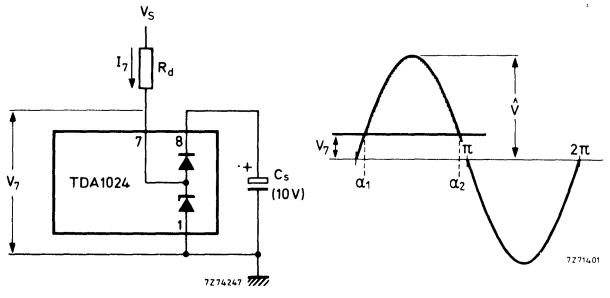

Figure 16. Mains Supply Circuit and Voltage Waveform.

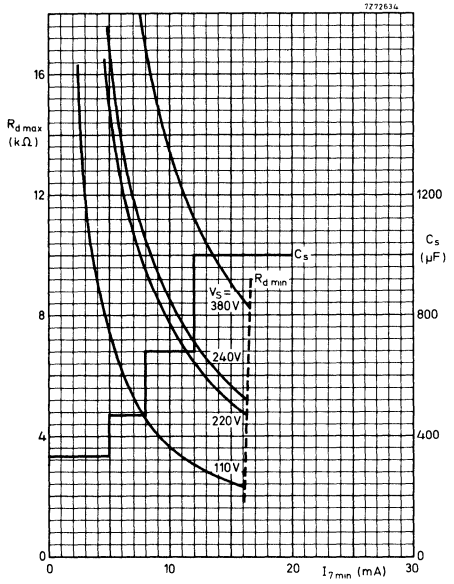

Figure 17. Value of R_d as a Function of I_7 with Supply Voltage (r.m.s.) as a Parameter. The Value of the Smoothing Capacitor as a Function of I_7 is also Shown.

Design of Static Switching Circuits Using TDA1024 AN129

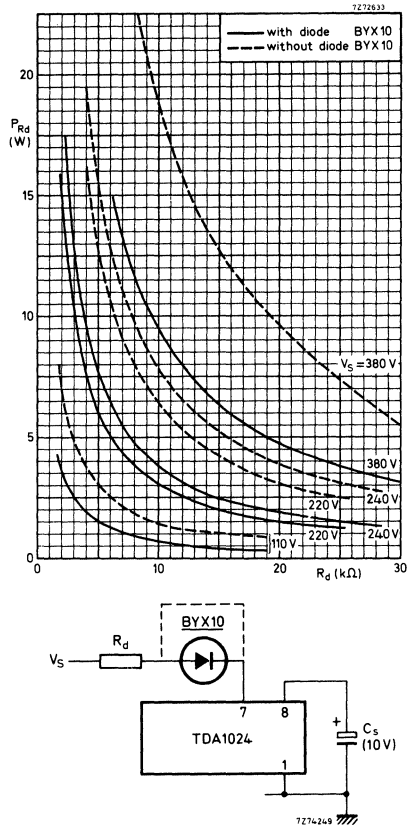

Figure 18. The Power Dissipated by Mains Dropping Resistor R_d as a Function of its Value with the Supply Voltage as a Parameter.

MINIMUM PERMISSIBLE VALUE FOR R_d AS A FUNCTION OF THE MAXIMUM PERMISSIBLE CURRENT TO PIN 7

The maximum current allowed at pin 7 of the TDA1024 is 80mA. This places the following restriction on the minimum value of R_d:

$$0.9R_{d\,min} = \frac{1.1\hat{V}}{0.08}$$

or, $R_{d\,min} = 15.28$. This lower limit for the value of mains dropping resistor has also been plotted in Fig. 17.

POWER DISSIPATED BY MAINS DROPPING RESISTOR R_d AS A FUNCTION OF ITS VALUE WITH THE SUPPLY VOLTAGE AS A PARAMETER

The following two methods can be used to reduce the supply voltage to the level required at pin 7 of the TDA1024:

- by connecting a series combination of a diode and a resistor between the supply voltage and pin 7 of the TDA1024. The diode half-wave rectifies the voltage applied to the resistor and thereby minimizes its dissipation.
- by connecting a resistor between the supply voltage and pin 7 of the TDA1024.

The general expression for the power dissipated by resistor R_d in Fig. 18 is:

$$P = V_{(rms)}^2/R_d$$

in which,

$$V_{(rms)}^2 = \frac{1}{2\pi}\int_{a_1}^{a_2} (\hat{V}\sin a - V_7)^2\,da + \frac{1}{2\pi}\int_{\pi}^{2\pi} (\hat{V}\sin a)^2\,da$$

(see Fig. 16).

Assuming a supply voltage variation of ±10%, a resistor tolerance of ±10%, and a minimum of 6.1V at pin 7 of the TDA1024, the worst-case dissipation by the resistor, if it is connected in series with a diode, is given by:

$$P_{max} = \left[\frac{1}{2\pi}\int_{a_1}^{a_2} (1.1\,\hat{V}\sin a - 6.1)^2\,da\right] \frac{1}{0.9R_d}$$

Assuming the same conditions, the worst-case dissipation by the resistor, if it is used without a diode, is given by:

$$P_{max} = \left[\frac{1}{2\pi}\int_{a_1}^{a_2} (1.1\,\hat{V}\sin a - 6.1)^2\,da + \frac{1}{2\pi}\int_{\pi}^{2\pi} (1.1\,\hat{V}\sin a)^2\,da\right] \frac{1}{0.9R_d}$$

These last two expressions have been computed for four values of supply voltage and have been plotted in Fig. 18.

USING A CAPACITOR FOR MAINS VOLTAGE REDUCTION

It is possible to replace the half-wave rectification diode and the supply dropping resistor with a capacitor (Fig.19), and thereby limit the power dissipated by the mains voltage reduction components yet further. However, for mains voltages below 220V, the power dissipated by the dropping resistor is comparatively small and the use of a capacitor is not considered to be necessary. For mains voltages above 240V, the additional cost of the required high-voltage capacitor is not justified. For these reasons, it is recommended that capacitive voltage reduction is only used with a mains input of 220V r.m.s. or 240V r.m.s.

Design of Static Switching Circuits Using TDA1024 — AN129

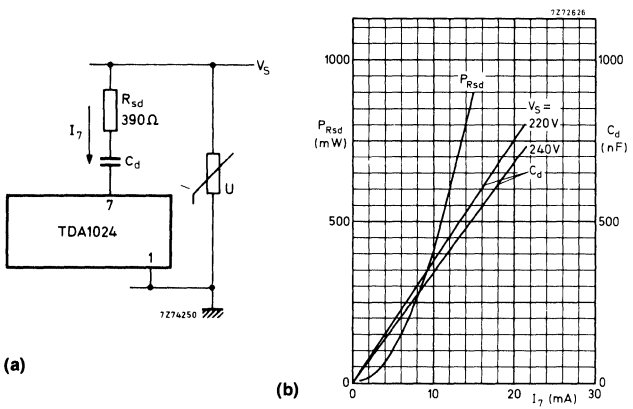

Figure 19. Using a Capacitor for Mains Voltage Dropping. The Circuit is Shown in (a) and the Power Dissipated by the Dropping Resistor and the Capacitor Value as Functions of the Current into Pin 7, with the Mains Supply Voltage as a Parameter, is Shown in (b).

When selecting a capacitor for mains voltage reduction, the following points must be considered:

- the specified maximum a.c. voltage for the capacitor must be compatible with the mains supply voltage.
- inrush current must be limited to less than 2A by a resistor connected in series with the capacitor.
- mains-borne transients must be suppressed to limit the maximum current applied to pin 7 of the TDA1024 to less than 2A.
- the value of the capacitor must be calculated as a function of the required average current at pin 7 of the TDA1024, using the mains voltage as a parameter. The maximum permissible value of the capacitor must also be calculated to ensure that the maximum permissible current at pin 7 of the TDA1024 is not exceeded under worst-case conditions.
- the power dissipated by the series resistor must be calculated as a function of the required average current at pin 7 of the TDA1024, using the mains voltage as a parameter.

Suppression of Mains-Borne Transients

A zinc-oxide voltage-dependent resistor must be connected across the mains input to limit mains-borne transients to:

$V_{trans} = I_{7SM} \times 0.9R_{sd}$

where I_{7SM} is the maximum permitted non-repetitive peak current at pin 7 (2 A).

For $R_{sd} = 390\Omega$, this yields a maximum transient voltage of about 700V. For 220V operation, a typical VDR type 2322 594 13512 will limit the supply voltage to the required level during current transients of up to about 200A. For 240V operation, a typical VDR type 2322 594 13912 will limit the supply voltage to the required level during current transients of up to about 80A.

Limitation of Inrush Current

Resistor R_{sd} must also limit the peak value of the inrush current to less than 2A under worst-case normal operating conditions. With a 240V r.m.s supply, the value of 390Ω will limit the worst-case peak value of the inrush current to:

$$\sqrt{2} \times \left(\frac{240 \times 1.1}{0.9 \times 390}\right) = 1.06A.$$

Value of the Capacitor as a Function of the Required Average Current at Pin 7 of the TDA1024

The average current supplied to pin 7 of the TDA1024 via capacitor C_d can be approximated by:

$$I_{(av)} = \frac{1}{\pi} \times \frac{\hat{V} - V_7}{\sqrt{|R_{sd}^2 + (1/\omega^2 C_d^2)|}}$$

Assuming tolerances of ±10% for the capacitor and the resistor, and variations of ±10% for the mains voltage, the worst-case average current can be approximated by:

$$I_{(av)} = \frac{1}{\pi} \times \frac{0.9\hat{V} - V_{7\,max}}{\sqrt{|(1.1R_{sd})^2 + (1/0.9\omega C_d)^2|}}$$

This relationship has been plotted for supply voltages of 220V and 240V in Fig. 19.

Maximum Permissible Value for the Capacitor

The maximum permissible value for the capacitor must be such that the maximum current into pin 7 of the TDA1024 does not exceed 80mA. Therefore, assuming ±10% tolerance for the components and for the mains voltage:

$$\frac{1.1\hat{V}}{\sqrt{|(0.9\,R_{sd})^2 + (1/1.1\omega C_d)^2|}} \leq 0.08.$$

Solving the expression for C_d gives:

$$C_{d\,max} = \frac{1}{1.1\omega\sqrt{|(1.1\hat{V}/0.08)^2 - (0.9\,R_{sd})^2|}}$$

For $V_{(rms)}$ = 220V, 50Hz, this yields $C_{d\,max}$ = 679nF (most suitable preferred value = 680nF). For $V_{(rms)}$ = 240V, 50Hz, the equation yields $C_{d\,max}$ = 622nF (most suitable preferred value = 560nF).

Power Dissipated by the Series Resistor

The power dissipated by the 390Ω series resistor R_{sd} can be approximated by:

$$P = I_{(rms)}^2\,R_{sd} = \left[\frac{1}{\sqrt{2}} \times \frac{\hat{V}}{\sqrt{|R_{sd}^2 + (1/\omega C_d)^2|}}\right]^2 R_{sd}.$$

Assuming tolerances of ±10% for the capacitor and the resistor, and variations of ±10% for the mains voltage, the worst-case dissipation can be approximated by:

$$P = \frac{1.1\,R_{sd}}{2} \times \frac{(1.1\hat{V})^2}{(1.1R_{sd})^2 + (1/1.1\omega C_d)^2}$$

The power dissipated by the resistor has been plotted as a function of I_7, with the mains voltage as a parameter, in Fig. 19.

TEMPERATURE SENSING BRIDGES FOR THERMOSTATIC SWITCHES

This section will show how to calculate nominal values for the components of a resistance bridge that incorporates an NTC thermistor as a temperature sensing element. The worst-case deviations of the indicated temperature due to component

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Design of Static Switching Circuits Using TDA1024

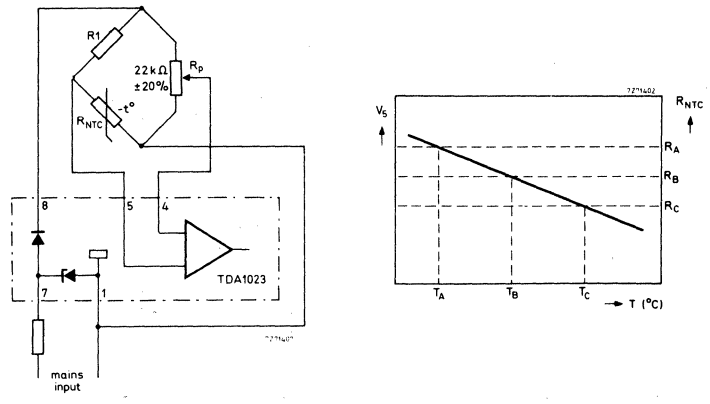

Figure 20. Typical Temperature Sensing Bridge, and the Relationship between R_{NTC}, V_5 and Temperature.

tolerances will also be calculated and represented graphically.

ACHIEVING A LINEAR TEMPERATURE SCALE

Figure 20 shows a temperature sensing bridge together with a graphical plot of the voltage at pin 5 of the TDA1024, and the resistance of the thermistor, as functions of the temperature of the thermistor. For the most linear relationship between the measured temperature and the voltage at pin 5, the following condition must apply:

$$T_A - T_B = T_B - T_C.$$

Therefore,

$$\frac{R_A}{R_1 + R_A} - \frac{R_B}{R_1 + R_B} = \frac{R_B}{R_1 + R_B} - \frac{R_C}{R_1 + R_C},$$

where R_A, R_B and R_C are the resistances of the thermistor at temperatures T_A, T_B and T_C respectively.

Solving for R_1 gives:

$$R_1 = \frac{R_B(R_A + R_C) - 2R_AR_C}{R_A + R_C - 2R_B} \quad (1)$$

Since the output voltage from the bridge is always less than the supply voltage and greater than zero, the full rotation of the adjustment potentiometer cannot be used because it is connected directly across the supply voltage. However, an advantage of this configuration is that the spreads of potentiometer values do not influence the accuracy of the bridge.

TEMPERATURE INDICATION ERROR DUE TO COMPONENT TOLERANCES

The component tolerances which affect the temperature indication are:

- the value of R_1 (±5%);
- the resistance of the NTC thermistor at 25°C (±10%);
- the B (β) value of the NTC thermistor (±5%).

The nominal resistance of the NTC thermistor at any given temperature is expressed by the well-known formula:

$$R_{NTC} = Ae^{B/T}, \quad (2)$$

where

$$A = \frac{R_{25}}{e^{B/298}}, \quad (3)$$

and T is the temperature in degrees kelvin (°C + 273).

Substituting Eq. (3) for A in Eq. (2) gives:

$$R_{NTC} = R_{25} \exp B \left(\frac{298 - T}{298T}\right). \quad (4)$$

Taking the tolerances of R_{25} and B into account for T > 25°C gives:

$$R_{NTC\,max} = 1.1R_{25} \exp 0.95B\left(\frac{298 - T}{298T}\right), \quad (5)$$

$$R_{NTC\,min} = 0.9R_{25} \exp 1.05B\left(\frac{298 - T}{298T}\right). \quad (6)$$

The equivalent equations for T < 25°C are:

$$R_{NTC\,max} = 1.1R_{25} \exp 1.05B\left(\frac{298 - T}{298T}\right), \quad (7)$$

$$R_{NTC\,min} = 0.9R_{25} \exp 0.95B\left(\frac{298 - T}{298T}\right). \quad (8)$$

The nominal voltage level at pin 5 of the TDA1024 (as a percentage of the voltage at pin 8), and therefore the percentage of the full travel of the adjustment potentiometer (270°), is given by:

$$\frac{V_5 \times 100}{V_8}\ \text{nom} = \frac{R_{NTC} \times 100}{R_1 + R_{NTC}}$$

$$= \frac{R_{25} \exp B\left(\frac{298 - T}{298T}\right)}{R_1 + \left[R_{25} \exp B\left(\frac{298 - T}{298T}\right)\right]} \times 100. \quad (9)$$

Taking the minimum value of R_1 into account and substituting Eq. (5) for R_{NTC} in Eq. (9) gives the worst-case upper limit at T > 25°C:

$$\frac{V_5 \times 100}{V_8}\ \text{max}$$

$$= \frac{1.1R_{25} \exp 0.95B\left(\frac{298 - T}{298T}\right)}{0.95R_1 + \left[1.1R_{25} \exp 0.95B\left(\frac{298 - T}{298T}\right)\right]} \times 100. \quad (10)$$

Taking the maximum value of R_1 into account and substituting Eq. (6) for R_{NTC} in Eq. (9) gives the worst-case lower limit at T > 25°C:

$$\frac{V_5 \times 100}{V_8}\ \text{min}$$

$$= \frac{0.9R_{25} \exp 1.05B\left(\frac{298 - T}{298T}\right)}{1.05R_1 + \left[0.9R_{25} \exp 1.05B\left(\frac{298 - T}{298T}\right)\right]} \times 100. \quad (11)$$

A TEMPERATURE SENSING BRIDGE FOR A WATER HEATER

For this application, the bridge must be capable of sensing temperatures within the range 60°C to 90°C. It uses an NTC thermistor type 2322 640 12473 (R_{25} = 47kΩ ± 10%, B = 3825 ±5%). The housing of an NTC thermistor type 2322 640 90007 can be used to mount the thermistor in a washing machine or a water heater; the

Table 1. Analysis of the Bridge Circuit

T (°C)	Plot	Reading on Nom. Scale	Error (°C)	Reading on Shifted Scale	Error (°C)
	Nominal (1)	60	0	—	—
60	Worst-case max. (3)	66.6	+6.6	56.3	−3.7
	Worst-case min. (2)	54	−6	62.3	+2.3
	Nominal (1)	75	0	—	—
75	Worst-case max. (3)	83.1	+8.1	73.6	−1.4
	Worst-case min. (2)	67.7	−7.3	75.9	+0.9
	Nominal (1)	90	0	—	—
90	Worst-case max. (3)	99.5	+9.5	90	0
	Worst-case min. (2)	81.2	−8.8	90	0

Potentiometer shaft rotation angle for temperature range 60°C to 90°C =

$$\frac{270\,(70.5 - 48.1)}{100} = 60.48°.$$

thermistor which is normally contained in the housing is not suitable for this application because its low resistance at the desired temperatures (60°C to 90°C) would cause the TDA1024 to draw additional current.

The three most important temperatures for the application are $T_A = 60°C$, $T_B = 75°C$ and $T_C = 90°C$. From Eq. (4), the nominal resistance of the thermistor ($R_{NTC\ nom}$) at each of these temperatures is:

$R_A = 12\,195\Omega$ at $T_A = 60°C$;

$R_B = 7433\Omega$ at $T_B = 75°C$;

$R_C = 4720\Omega$ at $T_C = 90°C$.

Substituting these values in Eq. (1) yields $R_1 = 5177\Omega$. The value selected for R_1 is therefore $5100\Omega \pm 5\%$. The worst-case current consumption for the bridge is:

$$\frac{V_{8\ min}}{R_{NTC\ min\ at\ T_C} + R_{1\ min}} + \frac{V_{8\ min}}{R_{p\ min}}$$

$$= \frac{5.5}{3788 + 4845} + \frac{5.5}{1760} = 0.95\ mA.$$

Equations (9), (10) and (11) have been computed for this bridge and have been plotted in Fig. 21 and analyzed in Table 1. The analysis shows that the worst-case maximum error is +9.5°C at 90°C. The worst-case minimum error is −9°C at 90°C. By rotating the scale around the shaft of the potentiometer until the readings are correct at 90°C in both cases, these errors are reduced to +2.3°C at 60°C and −3.7°C at 60°C.

For many thermostat applications, it is unwise to allow too high a temperature to be selected. For this reason, the potentiometer shaft should be prevented from rotating beyond the upper temperature limit by a stop affixed to the scale. This is also the reason for correcting the angular position of the scale at 90°C although the accuracy of the temperature adjustment would be improved if the correction were made at 75°C.

Figure 22 shows the same plots as Fig. 21 but, in this case, plot 2 has been moved upwards by the worst-case minimum error at 90°C. Plot 3 has been moved downwards by the worst-case maximum error at 90°C. Figure 22 therefore shows the accuracy of these thermostats if the angular position of every dial is correct at 90°C.

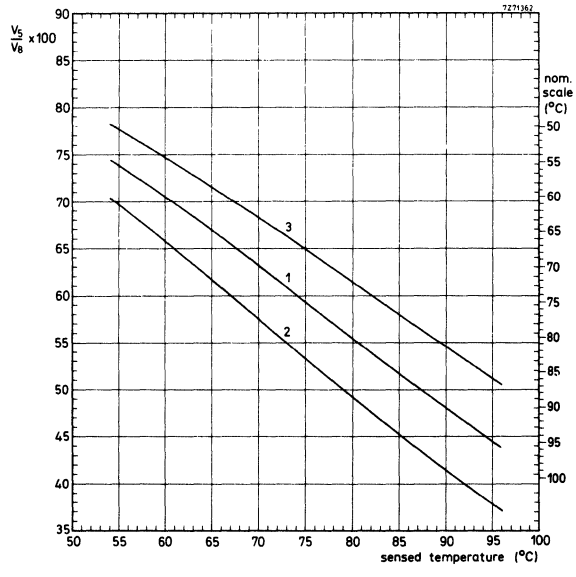

Figure 21. Nominal and Worst-Case Calculations of V_5 as a Percentage of V_8 Plotted as a Function of Temperature. Plot 1 is the Nominal Calculation; Plots 2 and 3 are the Minimum and Maximum Worst-Case Calculations Respectively.

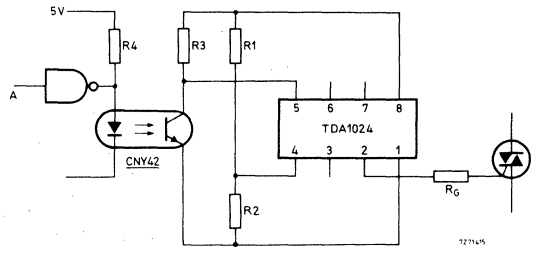

Figure 31. Interfacing the TDA1024 with a Shunt Photocoupler. When Input A is Logic 1, the Triac is On; when A is 0, the Triac is Off.

From Eq. (12):

$$V_4 = \frac{5.5 + 0.4}{2} = 2.95V.$$

From Eq. (13):

$$R_1 = \frac{70 \times 10^3 (6.5 - 2.95)}{6.5} = 38\,230\Omega.$$

The nearest preferred value is 39kΩ.

The nominal value for R_2 can be approximated by:

$R_2 = (70 \times 10^3) - (39 \times 10^3) = 31\,000\Omega$.

The nearest preferred value is 30kΩ.

The worst-case current drawn by the bridge at $V_8 = 5.5V$ is:

$$\frac{V_{8\ min}}{0.95\ (R_1 + R_2)} + I_{C\ max} + I_{5\ max}$$

$= 83.9 + 578.9 + 5 = 667.8\mu A$.

The circuit diagram of the TDA1024 interfaced with a photocoupler type CNY42 connected in parallel with the output from a logic element is given in Fig. 31. The component values are the same as those calculated for the previous circuit but the switching function is reversed.

Previously published as Technical Information 010, ELCOMA, April 1976.

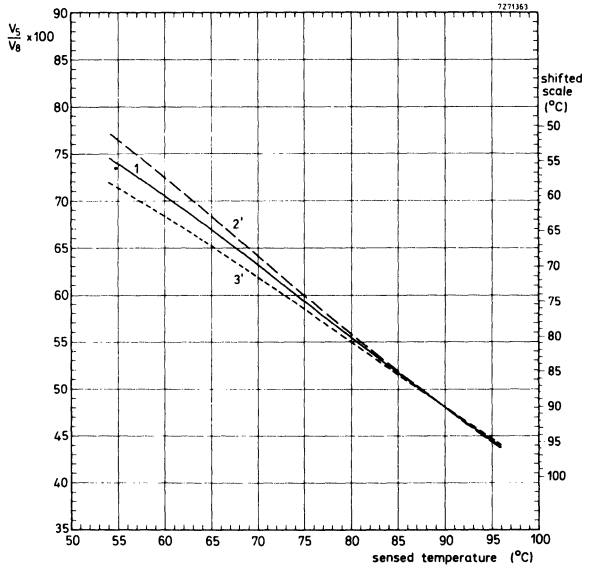

Figure 22. Nominal and Worst-Case Calculations of Dial Reading as a Function of Temperature, with the Angular Position of the Dial Corrected at 90° C. Plot 1 is the Nominal Calculation; Plots 2' and 3' are the Minimum and Maximum Worst-Case Calculations Respectively.

APPLICATION EXAMPLES

A COMPLETE DESIGN FOR A 1200 W WATER HEATER THERMOSTAT

For this application, three possible circuit configurations will be considered, namely:

- a circuit using the minimum number of peripheral components, i.e. a diode is not connected in series with mains dropping resistor R_d, and a gate resistor is not used.
- a circuit in which the power dissipated by the mains dropping resistor R_d is minimized by connecting a diode in series with R_d, and by using a gate resistor.
- a circuit that uses a capacitor for mains dropping.

The resistive water heating element is powered from a nominal 220V r.m.s. supply and is switched by a triac type BT138 (for BT138, P ≤ 1400W; for BT139, P ≤ 2000W). The essential design data are as follows:

- minimum gate voltage that will trigger all devices, V_{GT} = 1.6V at 0° C;
- minimum gate current that will trigger all devices, I_{GT} = 72mA at 0° C;
- maximum latching current, I_L = 60mA.

The three circuit diagrams are given in Figs 23, 24 and 25. The design of the bridge, which is common to all three circuits and is suitable for room temperature control, was discussed in the previous section. The bridge can be modified (e.g. operated via a photocoupler) as long as the current drawn from pin 8 of the TDA1024 does not exceed 1mA. If long leads are used between the temperature sensing bridge and the remainder of the circuit, it may be necessary to increase the noise immunity by connecting a 100nF capacitor in parallel with the bridge output (between pins 4 and 5 of the TDA1024).

In all three circuits, pin 3 of the TDA1024 is not connected; this causes minimum switching hysteresis (≈0.3° C). The reliability of the circuits is improved if a zinc-oxide VDR is used to protect the triac against mains-borne transients. The circuit with capacitor mains reduction (Fig. 25) must incorporate a Zn0 VDR in parallel with the mains supply to prevent high currents at pin 7 of the TDA1024 during mains transients.

Table 2. Component Values and Circuit Parameters for a 1200 W Water Heater Thermostat

Circuit Diagram	Fig. 23	Fig. 24	Fig. 25	Unit
Trigger pulse width t_p (Fig. 4)	105	105	105	μs
Synchronization resistor R_G (Fig. 6)	180	180	180	kΩ
Gate resistor R_G (Fig. 7)	—	33	33	Ω
Average gate current $I_{2(av)}$ (Fig. 12)	5.6	3.7	3.7	mA
Minimum required supply current I_7 (Fig. 15)	8.4	6.5	6.5	mA
Mains dropping resistor R_d (Fig. 17)	8.2	10	—	kΩ
Smoothing capacitor C_s (Fig. 17)	680	470	470	μF
Power dissipated by R_d (Fig. 18)	7.8	3.2	—	W
Mains dropping capacitor C_d (Fig. 19)	—	—	270	nF
Power dissipated by R_{sd} (Fig. 19)	—	—	190	mW

9

Design of Static Switching Circuits Using TDA1024 — AN129

The component values and operating characteristics for the three circuits are listed in Table 2. They have all been derived from the formulae and graphs given earlier in this publication.

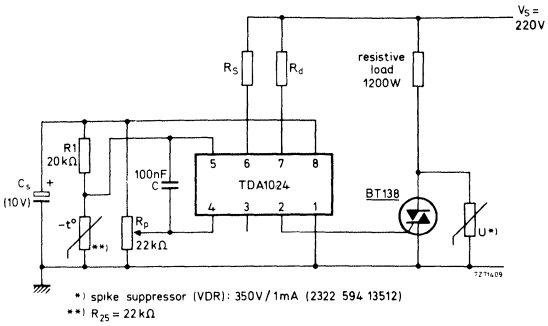

Figure 23. A 1200W Water Heater Thermostat Covering the Temperature Range 60° C to 90° C and Using the Minimum Number of Peripheral Components.

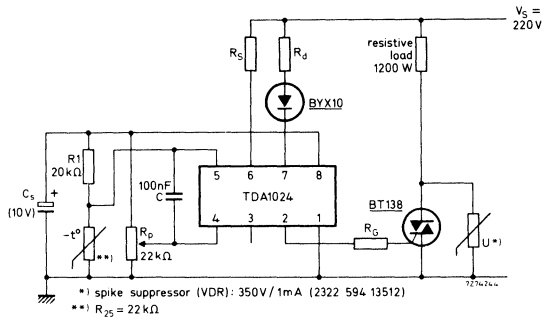

Figure 24. A 1200W Water Heater Thermostat Covering the Temperature Range 60° C to 90° C and Designed to Minimize the Power Dissipated by the Mains Dropping Resistor R_d.

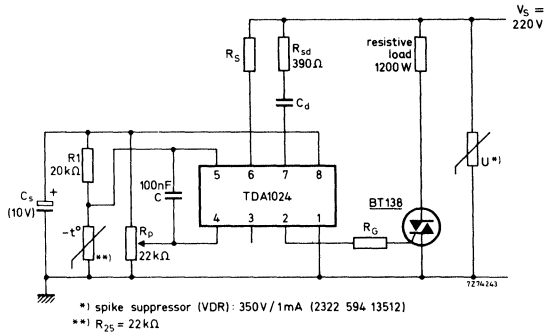

Figure 25. A 1200W Water Heater Thermostat Covering the Temperature Range 60° C to 90° C and Designed to Minimize the Dissipation in the Mains Voltage Reduction Circuit by Using Capacitor C_d.

SWITCHING HIGHER POWERED RESISTIVE LOADS

The thermal characteristics of triacs type BT138 and BT139 limit their use to the switching of resistive loads operating at powers up to 1400 W and 2000 W respectively. For switching higher powered loads, the TDA1024 can be used to drive a high current triac type BTW41.

The BTW41 is a glass-passivated 40A triac encapsulated in plastic. The essential design data for this component are:

- minimum gate voltage that will trigger all devices, V_{GT} = 2.1V at 0°C;
- minimum gate current that will trigger all devices, I_{GT} = 95mA at 0° C;
- maximum latching current, I_L = 60mA.

Note: A gate resistor will not reduce the overall current consumption in this case.

Although this triac is rated at 40A, its maximum power handling capability is limited by thermal considerations to about 5000W. A load that consumed more power than this would render forced cooling necessary and thereby make it unsuitable for application to domestic appliances.

THE TDA1024 AS A LIGHT-CONTROLLED SWITCH FOR A LAMP

The circuit given in Fig. 26 is similar to the previously described thermostat circuits except for the input bridge which incorporates a light-dependent resistor (LDR) instead of an NTC thermistor. In this application, the reference voltage at pin 4 of the TDA1024 is fixed at about 35% of the voltage at pin 8. The sensitivity of the switch is determined by the setting of the potentiometer connected in series with the LDR. The characteristics of the LDR are not critical for this application; types in the series 2322 600 93... or 2322 600 96... are all suitable.

INTERFACING THE TDA1024 WITH LOGIC ELEMENTS

The application range of the TDA1024 can be extended by driving it from the output of logic elements. This section describes the simple interface circuits that are required between the input of the TDA1024 (pin 5) and:

- 74S00 series TTL outputs;
- FZ/30 series HNIL interfacing gate type FZH161/4.LI31;
- LOCMOS logic outputs;
- photocoupler type CNY42.

Design of Static Switching Circuits Using TDA1024

AN129

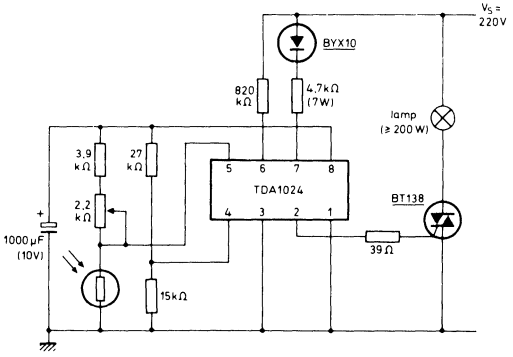

Figure 26. The TDA1024 as a Light-Controlled Switch for a Lamp.

Interfacing the TDA1024 with 74S00 Series TTL Outputs

The circuit diagram of the TDA1024 interfaced with a 74S00 series TTL gate with totem-pole output (e.g. SN74S00) is given in Fig. 27. The maximum output voltage specified for this logic series is 7V, and the specified logic levels are $V_{OH\ min}$ = 2.7V, $V_{OL\ max}$ = 0.5V. The series is therefore compatible with the TDA1024 and a direct interface can be made.

In the interests of minimum power consumption, the current drawn by the reference arms of the bridge (R_1 and R_2) should be restricted to about 100μA, a suitable value for the sum of the values of these two resistors is therefore about 70kΩ. For maximum noise immunity, the reference voltage at pin 4 of the TDA1024 should be at the middle of the logic level range, i.e.,

$$V_4 = \frac{V_{OH\ min} + V_{OL\ max}}{2} \qquad (12)$$

Inserting values in Eq. (12) gives:

$$V_4 = \frac{2.7 + 0.5}{2} = 1.6V.$$

The nominal value for R_1 can be approximated by:

$$R_1 = \frac{70 \times 10^3\ (V_8 - V_4)}{V_8} \qquad (13)$$

Inserting values in Eq. (13) gives:

$$R_1 = \frac{70 \times 10^3\ (6.5 - 1.6)}{6.5} = 52\,769\Omega.$$

The nearest preferred value is 51kΩ.

The nominal value for R_2 can be approximated by:

$R_2 = (70 \times 10^3) - (51 \times 10^3) = 19\,000\Omega$

The nearest preferred value is 18kΩ.

The worst-case current drawn by the bridge at V_8 = 5.5V is:

$$\frac{V_{8\ min}}{0.95(R_1 + R_2)} = 83.9\mu A.$$

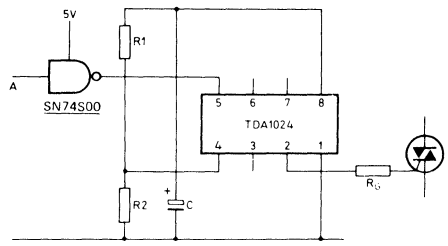

Figure 27. Interfacing the TDA1024 with TTL. When Input A is Logic 1, the Triac is Off; when A is 0, the Triac is On.

Interfacing the TDA1024 with FZ/30 Series HNIL Interface Gate Type FZH161/4.LI31

The circuit diagram of the TDA1024 interfaced with the FZH161/4.LI31 is given in Fig. 28. The output stage of the gate has an open collector. It can therefore be interfaced with the TDA1024 by connecting a collector load resistor (R_3) between the output of the gate and V_8.

When selecting a value for R_3, it is important to ensure the value is low enough to prevent the maximum current drawn by the gate in the HIGH state ($I_{QH\ max}$ = 80μA) from reducing the voltage at pin 5 of the TDA1024 to below V_8 — 0.5V. The maximum value for R_3 is therefore:

$$R_{3\ max} = \frac{0.5}{I_{QH\ max}} = \frac{0.5}{80 \times 10^{-6}}$$

$= 6250\Omega.$

The nearest preferred value is 6.8kΩ.

The maximum specified output level from the FZH161/4.LI31 in the LOW state is $V_{QL\ max}$ = 0.4V. The minimum output level when the gate is in the HIGH state will be approximately 5V.

From Eq. (12):

$$V_4 = \frac{5 + 0.4}{2} = 2.7V.$$

From Eq. (13):

$$R_1 = \frac{70 \times 10^3\ (6.5 - 2.7)}{6.5} = 40\,923\Omega.$$

The nearest preferred value is 39kΩ.

The nominal value for R_2 can be approximated by:

$R_2 = (70 \times 10^3) - (39 \times 10^3) = 31\,000\Omega.$

The nearest preferred value is 33kΩ.

The worst-case current drawn by the bridge at V_8 = 5.5V is:

$$\frac{V_{8\ min}}{0.95(R_1 + R_2)} + \frac{V_{8\ min} - V_{QL\ max}}{0.95R_3}$$

$= 80.4 + 789 = 869\mu A.$

Interfacing the TDA1024 with LOCMOS Logic Outputs

The circuit diagram of the TDA1024 interfaced with a LOCMOS inverting/non-inverting buffer type HEF4049 or HEF4050 is given in Fig. 29. The specified logic levels are $V_{OH\ min}$ = 5V, $V_{OL\ max}$ = 0.5V. The minimum available current in the HIGH state is $I_{OH\ min}$ = 700μA.

A direct interface with the TDA1024 can therefore be made.

9

Design of Static Switching Circuits Using TDA1024 — AN129

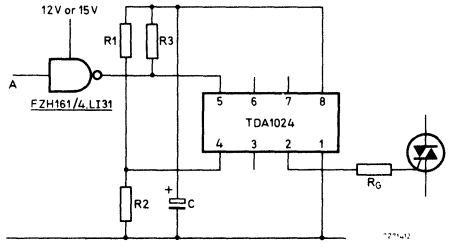

Figure 28. Interfacing the TDA1024 with FZ/30-Series. When Input A is Logic 1, the Triac is Off; when A is 0, the Triac is On.

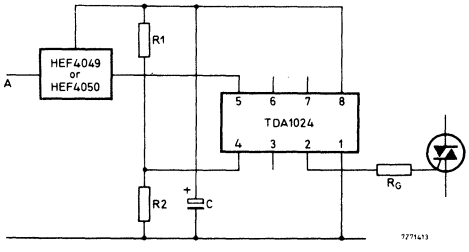

Figure 29. Interfacing the TDA1024 with LOCMOS. When the HEF4049 is used, a Logic 1 at A Means the Triac is Off; a 0 at A Means that the Triac is On: the Opposite is True when the HEF4050 is Used.

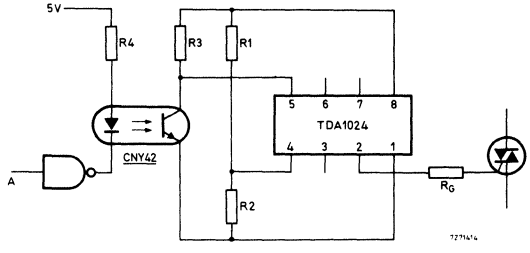

Figure 30. Interfacing the TDA1024 with a Series Photocoupler. When Input A is Logic 1, the Triac is Off; when A is 0, the Triac is On.

From Eq. (12):

$$V_4 = \frac{5 + 0.5}{2} = 2.75V.$$

From Eq. (13):

$$R_1 = \frac{70 \times 10^3 (6.5 - 2.75)}{6.5} = 40\,384\Omega.$$

The nearest preferred value is 39kΩ.

The nominal value for R_2 can be approximated by:

$R_2 = (70 \times 10^3) - (39 \times 10^3) = 31\,000\Omega$.

The nearest preferred value is 30kΩ.

The worst-case current drawn by the bridge at $V_8 = 5.5V$ is:

$$\frac{V_{8\,min}}{0.95\,(R_1 + R_2)} + I_{DD\,max} + I_{5\,max}$$

$= 83.9 + 45 + 5 = 133.9\mu A$

Interfacing the TDA1024 with Photocoupler CNY42

The circuit diagram of the TDA1024 interfaced with a CNY42 connected in series with the output from a logic element is given in Fig. 30. This is a useful circuit when safety regulations dictate that the logic circuitry must be mains isolated.

To obtain a diode current of about 10mA, the value of R_4 must be:

$$R_4 = \frac{5 - V_f}{10^{-2}} = \frac{5 - 1.2}{10^{-2}} = 380\Omega.$$

The nearest preferred value is 330Ω.

To ensure saturation of the transistor with a diode current of 10mA, the collector current of the transistor must be limited to 4mA. The minimum value for R_3 is therefore:

$$R_{3\,min} = \frac{V_{8\,max}}{4 \times 10^{-3}} = \frac{7.5}{4 \times 10^{-3}} = 1875\Omega.$$

To minimize the current consumption from pin 8 of the TDA1024, a value of 10kΩ has been chosen for R_3.

This results in a maximum collector current ($V_8 = 5.5V$) of:

$$I_{C\,max} = \frac{V_8}{0.95\,R_3} = \frac{5.5}{9500} = 578.9\mu A.$$

The minimum HIGH state level at pin 5 of the TDA1024 is:

$V_{OH\,min} \approx V_{8\,min} \approx 5.5V$.

The maximum LOW state voltage level at pin 5 of the TDA1024 is:

$V_{OL\,max} = V_{CE\,sat} = 0.4V$.

TDA1559 Motor Speed Regulator with Thermal Shut-Down AN130

INTRODUCTION

Trends of decreasing the supply voltage in portable apparatus sets was one of the reasons to develop the TDA1559. Another very important reason was to decrease the total current consumption.

The absolute value of the multiplication coefficient, called K-factor, determines the current consumption for a large portion. A higher K-factor results in a lower current consumption.

The TDA1559 has a K-factor of twenty-one.

Application in apparatus sets with a low supply voltage is only possible if the internal voltage loss, called drop-out voltage, is sufficiently low. The TDA1559 can be used in a voltage range of 2.1 up to and including 15V.

MOTOR REGULATORS

General

The function of the regulator is to supply the terminals of the applied DC-motor with a voltage capable of maintaining revolutions constant against supply voltage, applied torque and ambient temperature variations.

The discussed integrated regulator is a so called e.m.f. (ElectroMotive Force) regulator.

For calculations a DC-motor can be replaced by a voltage source E_i in series with a resistor R_m. The voltage source is the induced back e.m.f. of the DC-motor and defined as:

$$E_i = N.0.C \quad (1)$$

where

N = number of revolutions per minute
0 = magnetic flux in Weber
C = constant

The resistor R_m is the internal resistance of the DC-motor.

As soon as the motor is connected to a voltage source, a current I_m will be absorbed by the motor. The current is linear proportional to the applied torque T. The current can be expressed as:

$$I_m = T \cdot \frac{2\pi}{60} \cdot \frac{1}{C.0} \quad (2)$$

where: T = applied torque in Newton-meters.

$\frac{2\pi}{60} \times \frac{1}{C.0}$ is called the specific motor current (I specific).

An e.m.f. regulator is based on the expression

$$V_m = E_i + I_m \cdot R_m$$

where

V_m = voltage across the DC-motor
E_i = back electromotive force
I_m = current absorbed by the motor
R_m = internal resistance of the motor

Constant revolutions can be obtained by compensating the variations of voltage losses $I_m \cdot R_m$.

The solution is a voltage source with a negative output resistance equal to R_m.

Explanation:

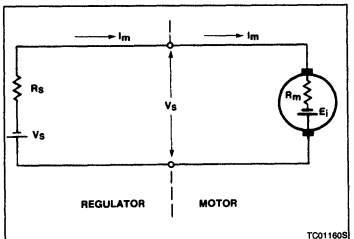

Figure 1

$$V_s - E_i = I_m (R_s + R_m) \quad (3)$$

The influence of I_m is zero if:

$$R_s = -R_m$$

Thus to any increase in current (caused by an increased torque) will correspond a proportional increasing of output voltage. In practice, however, R_s may never be equal to $-R_m$. This is because of low frequence oscillation.

Consequently the regulator will always show slight torque dependence.

Three Pins Regulator

The TDA1559 is a so-called three pins regulator like TDA1059 B/C.

Figure 2 shows a block-diagram of the integrated regulator.

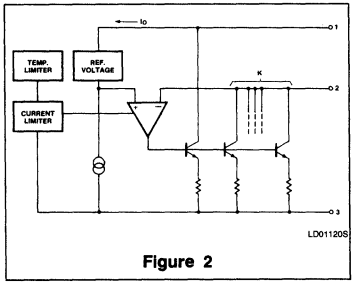

Figure 2

In contrast with TDA1059 B/C, the TDA1559 has a higher K-factor and a lower drop-out voltage. Also the nominal quiescent current is reduced. The principle of the discussed regulator can be expressed in a formula, namely:

$$\text{Input current} = \frac{\text{output current}}{\text{K-factor}}$$

The output current is given by the sum of the absorbed motor current I_m and a reference current I_{ref} (see Figure 3). The absolute value of the reference current depends on the speed of the motor.

This current should be, once adjusted, independent of supply voltage, temperature and torque variations. The reference current is being made by means of a voltage stabilizer, which is integrated in the TDA1559, and an externally adjustable resistor. The K-factor is fixed internally in the I.C.

CALCULATIONS

Figure 3 gives an application diagram of the TDA1559. All currents and voltages necessary for calculations are indicated too.

TDA1559 Motor Speed Regulator With Thermal Shut-Down AN130

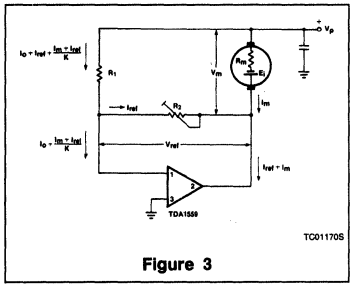

Figure 3

The regulator parameters are:
- V_{ref} (V_{2-3}) internal reference voltage.
- K-factor.
- I_o quiescent current

In such a network the voltage across the motor can be calculated as follows:

$$V_m = I_{ref} \cdot R_2 + R_1 (I_o + I_{ref} + \frac{I_m + I_{ref}}{K}) \quad (4)$$

I_{ref} is given by:

$$I_{ref} = \frac{V_{ref}}{R_2} \quad (5)$$

(4) and (5) gives:

(6)

$$V_m = R_1 \cdot I_o + I_m \cdot \frac{R_1}{K} + V_{ref} (1 + \frac{R_1}{R_2} (1 + \frac{1}{K}))$$

The voltage across the motor is also given by:

$$V_m = E_i + I_m \cdot R_m \quad (7)$$

So:

$$E_i + I_m \cdot R_m = R_1 \cdot I_o + I_m \cdot \frac{R_1}{K} + V_{ref} (1 + \frac{R_1}{R_2} (1 + \frac{1}{K}))$$

or:

(8)

$$E_i = R_1 \cdot I_o + I_m (\frac{R_1}{K} - R_m) + V_{ref} (1 + \frac{R_1}{R_2} (1 + \frac{1}{K}))$$

Formula (8) is very important and will be used for all other calculations. In equation (8) the resistance R_s is represented by the term R_1/K.

The Value of R_1

R_1 is very important since together with the K-factor it determines the quality of the regulator. I already noted that the motor current is linear to the applied torque. So the torque influence on the speed can be decreased by making the ΔR ($\Delta R = |\frac{R_1}{K} - R_m|$) as low as possible. Remember ΔR zero is not allowed.

Thus in practice from R_m, R_1 and K-factor we have to know:
- the absolute value
- the spread
- the temperature dependency
- the supply voltage dependency and
- the current dependency

So: R_1 should be
$R_{1(max)} < K_{min} \times R_{m(min)}$

R_2 Calculation

The speed of the applied DC motor can be adjusted by means of R_2. A simplification of formula (8) to R_2 gives:

(9)

$$R_2 = \frac{V_{ref} \times R_1 \times (1 + \frac{1}{K})}{E_i - R_1 \cdot I_o - I_m (\frac{R_1}{K} - R_m) - V_{ref}}$$

The spread, however, of each parameter will lead us to two values, namely:
- $R_{2\,(max)}$ and
- $R_{2\,(min)}$

$$R_{2(max)} = \frac{V_{ref(max)} \cdot R_{1(max)} \cdot (1 + \frac{1}{K_{(min)}})}{E_{i(min)} - R_{1(max)} \cdot I_{o(max)} - I_{m(max)} \cdot (\frac{R_{1(max)}}{K_{(min)}} - R_{m(min)}) - V_{ref(max)} \cdot}$$

$$R_{2(min)} = \frac{V_{ref(min)} \cdot R_{1(min)} \cdot (1 + \frac{1}{K_{(max)}})}{E_{i(max)} - R_{1(min)} \cdot I_{o(min)} - I_{m(min)} \cdot (\frac{R_{1(min)}}{K_{(min)}} - R_{m(max)}) - V_{ref(min)} \cdot}$$

In practice R_2 is realized by a fixed resistor $R_2{}^1$ in series with a potentiometer R_p used as an adjustable resistor. The components $R_2{}^1$ and R_p are determined as follows:

$R_2{}^1(max) > < R_{2(min)}$

$R_{p(max)} \geq R_{2(max)} - R_{x(min)}$
- R_x is the chosen value for $R_2{}^1$.

TEMPERATURE COMPENSATION

The temperature dependency of the regulator can be influenced by adding a diode in series with pin 1 (see Figure 4). The temperature behavior of the used mechanical parts (cassette deck) determines the necessity of applying a diode. Which type and the necessity of a diode should be determined by practical experiments. From our side we can only give the influence of the diode in a formula and a figure (see Figure 5) which shows the difference in motor speed between with and without a diode. Application diagram TDA1559 with temperature compensation diode is given in Figure 4.

Expression of R_1 and R_2 with Diode Compensation

The current I_{ref} through R_2 is now determined by:

(see Figure 4) $I_{ref} = \frac{V_{ref} + U_D}{R_2}$

Using formula (4) gives:

$$V_m = V_{ref}(1 + \frac{R_1}{R_2} (1 + \frac{1}{K})) + U_D(1 + \frac{R_1}{R_2} (1 + \frac{1}{K})) + R_1 \cdot I_o + I_m \cdot \frac{R_1}{K}$$

or

(10)

$$V_m = (V_{ref} + U_D) \cdot (1 + \frac{R_1}{R_2} (1 + \frac{1}{K})) + R_1 \cdot I_o + I_m \cdot \frac{R_1}{K}$$

Using (7) and (10) gives:

(11)

$$E_i = R_1 \cdot I_o + I_m (\frac{R_1}{K} - R_m) + (V_{ref} + U_D) \cdot (1 + \frac{R_1}{R_2} (1 + \frac{1}{K}))$$

Formula (11) shows that the application of D_1 has no influence on the calculation of R_1; ΔR is still $/ \frac{R_1}{K} - R_m /$. A simplification of formula (11) to R_2 gives:

$$R_2 = \frac{(V_{ref} + U_D) \times R_1 \times (1 + \frac{1}{K})}{E_i - R_1 \cdot I_o - I_m (\frac{R_1}{K} - R_m) - (V_{ref} + U_D)}$$

For measuring of Figure 5 the following components are being used:
- D_1 = BA220
- $R_1 = 220\Omega \pm 2\%$
- $R_2{}^1 = 180\Omega \pm 5\%$
- $R_p = 470\Omega$

TDA1559 Motor Speed Regulator With Thermal Shut-Down — AN130

TDA1559 APPLICATION

9V Application

-Accepted ambient temperature range: −5 to 55°C
-Accepted supply voltage range: 9 to 6V

Information about the used motor:
manufacture: Philips
type : 4322 010 71020

Nominal speed	2000 r.p.m.
Recommend torque to get optimal efficiency	1 mNm
e.m.f. at 2000 r.p.m.	3.58V ± 11.6%
R_m (static), $R_{m_{st}}$	13Ω ± 10%
R_m (dynamic), $R_{m_{dy}}$	$R_{m_{st}}$ x 1.16
I specific	59.25A/Nm ± 11.6%
Temperature dependency:	
−e.m.f.	−0.2%/°C
$-R_m$	+0.4%/°C

Remark: For the calculation of R_1 we have to use $R_{m_{dy}}$.

R_1 calculation:

Requirement: $R_{1\ max} < K_{min} \times R_{m\ min}$.

The minimum values will be found at $T_{amb} = -5°C$.

At worst-case condition we found:
$R_{min} \simeq 11.9\Omega$
$K_{min} \simeq 18$

So $K_{min} \times R_{m(min)} \simeq 214\Omega$

Practical value:
$R_1 = 220\Omega \pm 2\%$

R_2 calculation:

Using the formulas and the information given we found that R_2 is about:

$86 < R_2 < 203\Omega$

Remark: ambient temp. range*	15 to 35°C
voltage range*	9 ± 1.5V

We know that: $R_2 = R_2{}^1 + R_p$

$R_2{}^1(max) > < R_{2(min)}$

practical value for $R_2{}^1 = 82\Omega \pm 5\% = R_x$

$R_{p(max)} \geqslant R_{2(max)} - R_{x(min)}$

practical value $R_p = 220\Omega$

Measuring Results

N = f (Torque)
at: $T_{amb} = +25°C$
$V_p = 9V$ and
$V_p = 6V$
See Fig. 7.

N = f (T_{amb})
at: $V_p = 9V$ and
$V_p = 6V$
$T = 1$ mNm ± 10%
See Fig. 8 and Fig. 9.

Remark: For measuring set-up see Appendix 1.

6V Application

-Accepted ambient temperature range: −5 to 55°C
-Accepted supply voltage range: 6 to 4.2V

Information about the used motor:
manufacture: Philips
type : 4322 010 71000

Nominal speed	2000 r.p.m.
Recommend torque to get optimal efficiency	1 mNm
e.m.f. at 2000 r.p.m.	2.57V ± 9%
R_m (static), $R_{m_{st}}$	7.1Ω ± 8%
R_m (dynamic), $R_{m_{dy}}$	$R_{m_{st}}$ x 1.16
I specific	82.3A/Nm ± 9%
-temperature dependency:	
−e.m.f.	−0.2%/°C
$-R_m$	+0.4%/°C

Remark: For the calculation of R_1 we have to use $R_{m_{dy}}$.

R_1 calculation:

Requirement: $R_{1\ max} < K_{min} \times R_{m\ min}$.

Minimum value at $T_{amb} = -5°C$.

At worst-case condition we found:
$R_{min} \simeq 6.67\Omega$
$K_{min} \simeq 18$

So $K_{min} \times R_{m(min)} \simeq 120$

Practical value:
$R_1 = 120\Omega \pm 2\%$

R_2 calculation:

Using the formulas and the information given we found that R_2 is about:
$77 \leqslant R_2 \leqslant 192\Omega$.

Remark: ambient temp. range*	15 to 35°C.
voltage range*	6 ± 1.5V.

We know that: $R_2 = R_2{}^1 + R_p$
$R_2{}^1(max) > < R_{2(min)}$

Practical value for $R_2{}^1 = 75\Omega \pm 5\% = R_x$.
$R_{p(max)} \geqslant R_2{}^1(max) > - R_{x(min)}$.

Practical value
$R_p = 220\Omega$.

Measuring Results

N = f (Torque)
at: $T_{amb} = +25°C$
$V_p = 6V$ and 4.2V
See Fig. 11.

N = f (T_{amb})
at: $V_p = 6V$ and
$V_p = 4.2V$
$T = 1$ mNm ± 10%
See Fig. 12 and Fig. 13.

Remark: For measuring set-up see Appendix 1.

CONCLUSION

Specification and measuring results both show that the TDA1559 can be used in a lot of applications. The low drop-out voltage resulting in an input voltage at pin 2 as low as 2.1V offers the possibility to use the TDA1559 in applications with a low supply voltage.

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TDA1559 Motor Speed Regulator With Thermal Shut-Down AN130

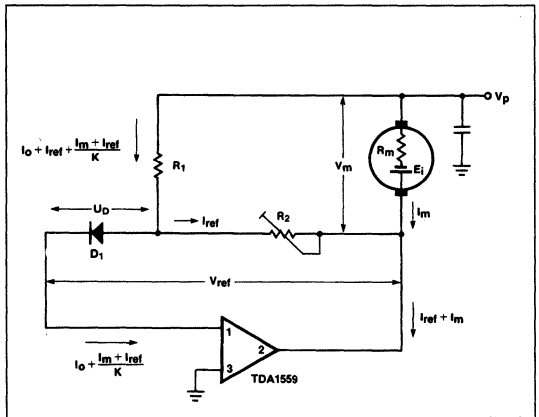

Figure 4

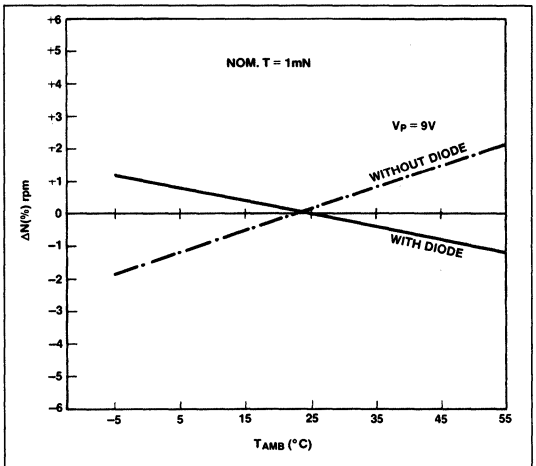

Figure 5

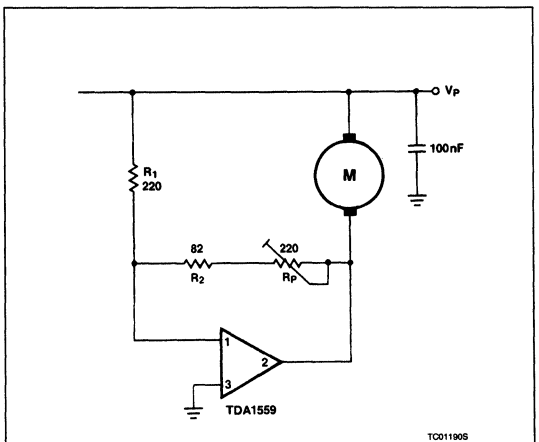

Figure 6. Application Circuit Diagram

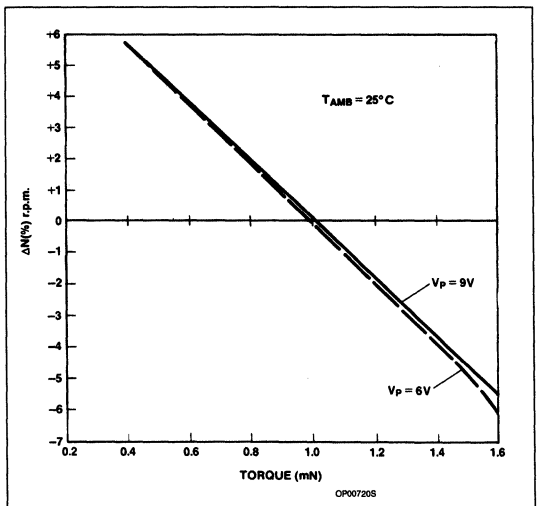

Figure 7

TDA1559 Motor Speed Regulator With Thermal Shut-Down AN130

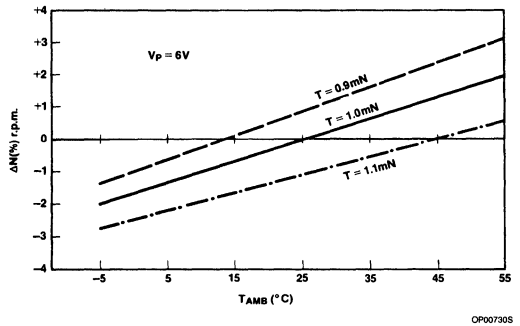

Figure 8

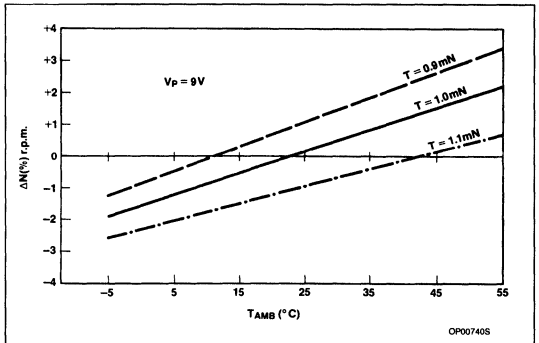

Figure 9

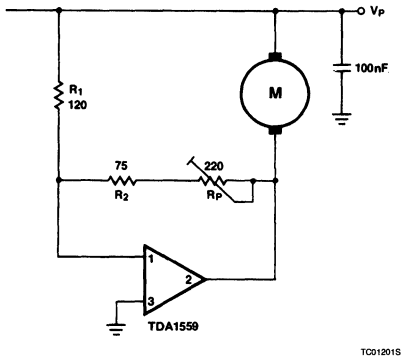

Figure 10. Application Circuit Diagram.

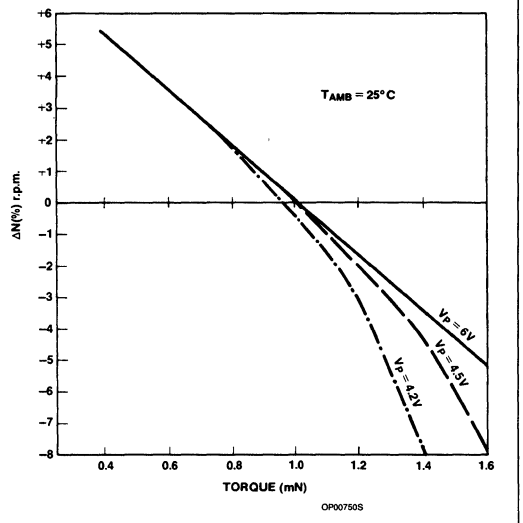

Figure 11

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TDA1559 Motor Speed Regulator With Thermal Shut-Down AN130

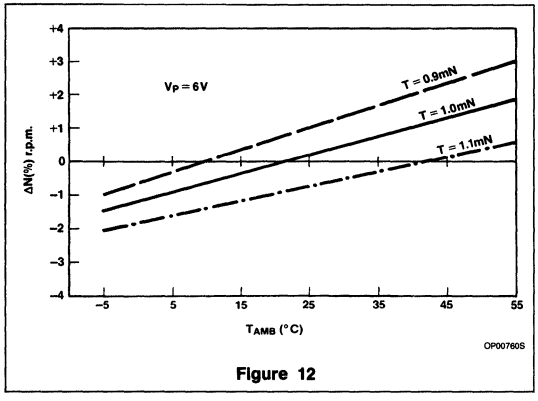


Figure 12

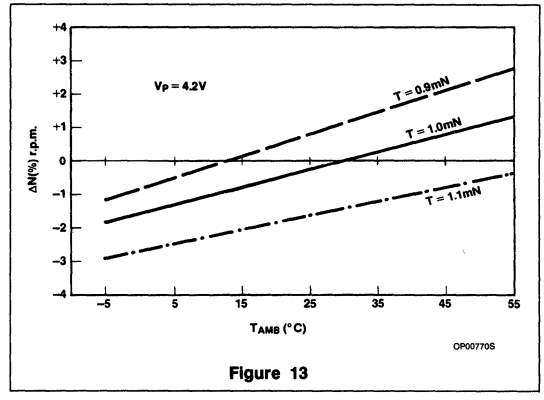
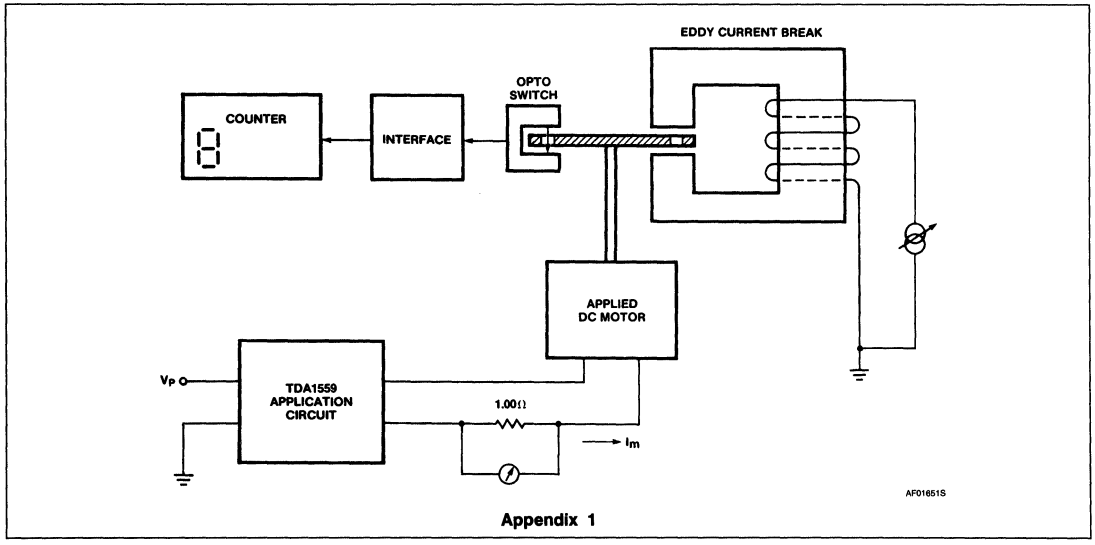


Figure 13



Appendix 1

Introduction to PWM Speed Control System for 3-Phase AC Motors AN135

J. A. HOULDSWORTH and W. B. ROSINK

The majority of industrial drives use electric motors, since they are controllable and readily available. In practice, most of these drives are based on a.c. induction motors because such motors are rugged, reliable, and relatively inexpensive.

To control the speed of a drive many methods have been developed, ranging from mechanical and hydraulic systems to electrical and electronic systems using, for example, d.c. shunt-wound motors whose speed can be controlled directly. However, it has been the desire of drive system manufacturers to vary the speed of the standard three-phase induction (asynchronous) motor by electrical means. This aim has been technically possible for some years, and with recent advances in power electronic components and integrated circuits it is now achievable with both cost and quality comparable to that of alternative systems.

This article begins by considering the development of the most common currently available electronic systems by examining two approaches to the control of d.c. motors: phase (or line) control, and chopper (switched mode) control. Then, the characteristics of the three-phase induction motor are discussed, establishing the dependence of motor speed on frequency, and the need to control both frequency and voltage for a proper method of control. This is achieved by using a three-phase inverter to convert the mains frequency to a variable frequency and voltage supply to the motor. The main features of the various types of inverter currently available are then considered. These systems have certain shortcomings, and in this article we describe a new improved system using Pulse-Width Modulation (PWM) techniques. We have developed a purpose-designed Large Scale Integrated (LSI) circuit specifically for this application.

GENERAL INTRODUCTION TO MOTOR SPEED CONTROL

Traditionally, d.c. motor control using Ward-Leonard sets required the use of three electrical machines: a three-phase induction motor, a d.c. generator, and a d.c. motor. This can now be replaced by a double six-thyristor bridge employing only one electric machine, the d.c. motor. Changing from electromechanical control systems to electronic control systems generally provides a reduction in complexity, savings in cost, space, and response time, and gains in efficiency.

Phase control of d.c. motors

Figure 1 shows a typical d.c. motor controller using a bridge circuit of six thyristors fed from the three-phase mains supply. Motor voltage control is achieved by varying the phase angle at which the thyristors are fired relative to the incoming mains voltage supply waveform. This provides an output voltage ranging from zero to a value equal to that provided by a full-wave diode rectifying bridge. Such a circuit is typically used in the control of d.c. shunt motors (d.c. motors with separate field excitation).

Phase controlled rectifier circuits, like that shown in Fig.1, are the simplest form of electronic motor control because the thyristors are naturally "mains-commutated" or "line-commutated" from the three-phase a.c. source. In this case, the commutation process consists of a cyclic transfer of current from one pair of conducting thyristors to the next. The three thyristors in the upper group (Th_1, Th_3, and Th_5) have a common cathode terminal, and conduction is via the thyristor with the most positive anode voltage. The other two thyristors are reverse-biased relative to the common cathode terminal. Similarly, the

Introduction to PWM Speed Control System for 3-Phase AC Motors AN135

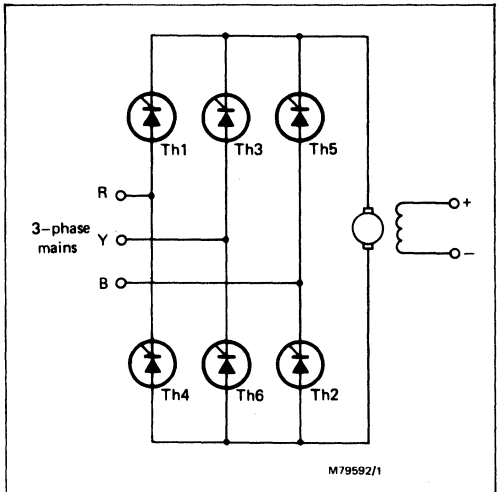


Fig.1 Basic 6-thyristor phase-control circuit for d.c. motor

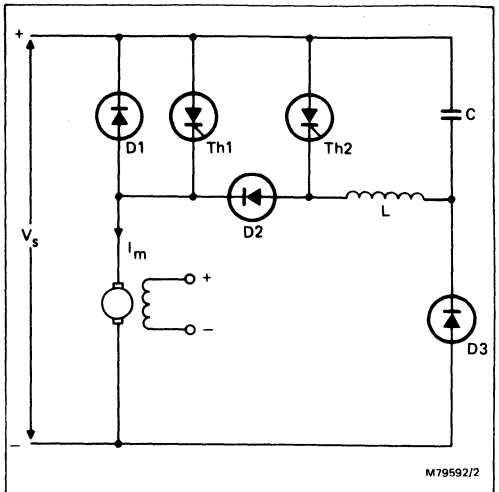


Fig.2 Basic chopper circuit for d.c. motor

thyristors in the lower group (Th_4, Th_6, and Th_2) have a common anode connection, and conduction is via the thyristor with the most negative cathode. For a phase sequence R, Y, B, the thyristors conduct in pairs: Th_1 and Th_2; Th_2 and Th_3; Th_3 and Th_4; Th_4 and Th_5; Th_5 and Th_6; they are consequently numbered in their correct firing sequence in Fig.1.

All phase control systems use line commutation which imposes a controller bandwidth limited by the mains supply frequency, and for improved performance other systems are required.

Chopper control of d.c. motor

The limitations of phase control may be overcome by using chopper control. The principle of chopper control can be illustrated by considering the speed control of a d.c. shunt motor from a rectified a.c. supply or d.c. supply source. The motor average voltage is controlled by varying the on-to-off time ratio for which the d.c. supply voltage is applied to the load, and thyristor turn-off is now achieved by forced commutation. Forced commutation, as the name implies, "forces" the thyristor to turn-off by using an auxiliary circuit (the commutation circuit) consisting for example of an auxiliary or commutation thyristor and a series resonant LC circuit.

The mechanism of varying the on-off time by "chopping" the input voltage into discrete pulses gives this type of control its name. Thus, by varying the width of the pulses, or the repetition frequency of the switching period, the average value of the d.c. output voltage can be varied from a very small value to almost the voltage of the supply source.

An example of a basic chopper circuit is shown in Fig.2. The motor current is labelled I_m. Thyristor Th_1 is the main thyristor and Th_2 the commutation thyristor which is used to turn off the main thyristor Th_1 with the aid of the series-resonant LC circuit. When Th_1 is switched off, the motor current I_m can flow via the diode D_3, the inductance L, and the diode D_2. The diode D_3 is therefore known as the 'flywheel diode'. The operation of the commutation circuit is described in detail later in this article.

The a.c. motor

The majority of industrial drives are powered by three-phase a.c. induction motors. The wide application of these motors is a direct consequence of their inherent advantages when compared with other types. These advantages include:

- High reliability with low maintenance costs.
- Low cost: for a given output power a d.c. motor can cost several times as much as its a.c. equivalent.
- High output power to volume and weight ratios.
- The speed is relatively independent of the load for a given supply frequency.
- Brushless construction: this makes it particularly suitable for use in hazardous environments such as mining and petrochemical industries.
- Standard versions are readily available from stock.

The standard three-phase induction motor is essentially a single-speed machine when supplied from mains of

Introduction to PWM Speed Control System for 3-Phase AC Motors AN135

fixed voltage and fixed frequency. If f is the frequency of the mains supply and p is the number of pole-pairs in the stator, then the speed of rotation of the stator field (the synchronous speed) is given by:

$$N_s = \frac{f}{p} \times 60 \text{ rev/min.}$$

By changing the number of pole-pairs of the motor, the motor can be made to operate at a number of fixed speeds. For continuously variable speed control, however, the supply frequency must be varied; the applied voltage must also be varied in linear proportion to the supply frequency to maintain constant motor flux. At low frequencies, where the motor inductive reactance is low, boosted voltage may be used to compensate for the stator 'IR' voltage drop. Thus control of both frequency and voltage is necessary for proper variable-speed operation. Under normal operating conditions, the rotor (motor shaft) speed is a few per cent less than the synchronous speed. The difference between the two speeds is called slip.

Figure 3 illustrates the induction motor torque-speed characteristics under nominal rated voltage V_1 and reduced voltage V_2 together with typical fan and industrial machine tool loads (superimposed). It can be shown that smooth speed control depends on the slope of both the motor torque curve and the speed torque curve. Thus constant-frequency variable-voltage operation is suitable only for "square law" loads such as fans or pumps to ensure proper starting and stable running conditions. Systems using speed control by variable voltage are not suitable for use with constant-torque loads, and, when used with fan or pump loads, efficiency

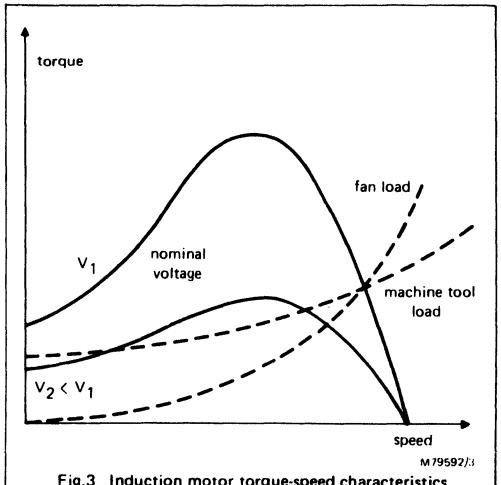


Fig.3 Induction motor torque-speed characteristics

is poor. To overcome these limitations it is necessary to provide a variable-frequency variable-voltage supply to the motor, and this requires the use of some type of inverter circuit.

INVERTERS FOR A.C. MOTORS

There are two basic types of inverter for use with variable-frequency and variable-voltage speed control systems for three-phase a.c. motors: the current-source type and the voltage-source type.

The current-source inverter

A block diagram of a current-source inverter is shown in Fig.4. It consists of either a phase-controlled rectifier circuit, or rectifier-chopper circuit, followed by a choke to provide a constant-current source for the inverter. The inverter thyristors are force-commutated to transfer the current between phases. Since the inverter is supplied from a current source, it is protected from transient current surges arising from rapid load variations.

In theory, the current-source inverter makes possible an economical inverter design in which the thyristors are fully utilised during normal operation. However, it cannot be used for the control of two or more motors in parallel, and motors exhibit pulsating torques at low frequencies. Because of these restrictions, current-source inverters are therefore only of limited application.

The voltage-source inverter

Because of the limitations of the current-source inverter, the voltage-source inverter is the most commonly used type. The simplest form of this is the quasi-square-wave inverter, or 'six-pulse inverter'.

Quasi-square-wave control of a.c. motors

In the quasi-square-wave inverter system, each of the three inverter outputs is switched every half-period between the plus and minus terminal of the fixed d.c. supply source as in Fig.5. This produces the output waveforms of Fig.6. The half-period average line output voltage is given by $V_{(R-Y)av} = V_s \times 2/3$, where V_s equals the d.c. supply voltage. However, the a.c. motor requires an average voltage proportional to frequency, and this variation of the output voltage with frequency requires the use of an additional chopper circuit.

Pulsed quasi-square-wave source inverter

The need for this extra circuitry can be overcome by the pulsed quasi-square-wave system. The output of this system is shown in Fig.7. Each of the three inverter outputs supply the motor with n output pulses, ampli-

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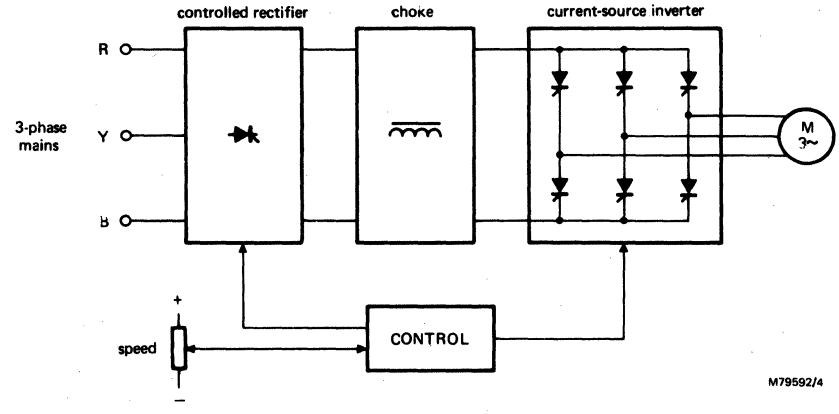

Fig.4 Variable-frequency current-source inverter system

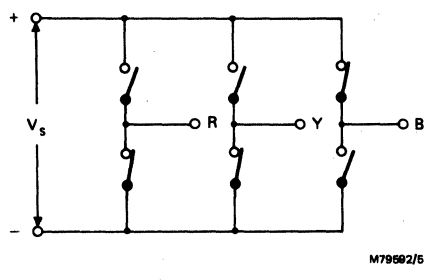

Fig.5 Voltage-source inverter

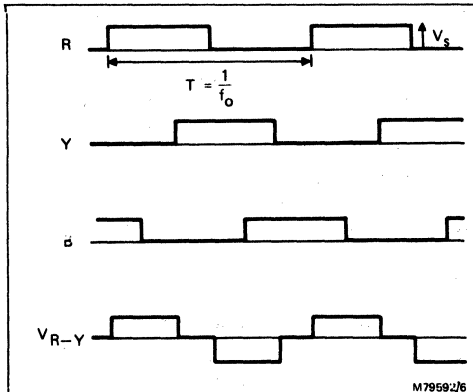

Fig.6 Quasi-square waveforms

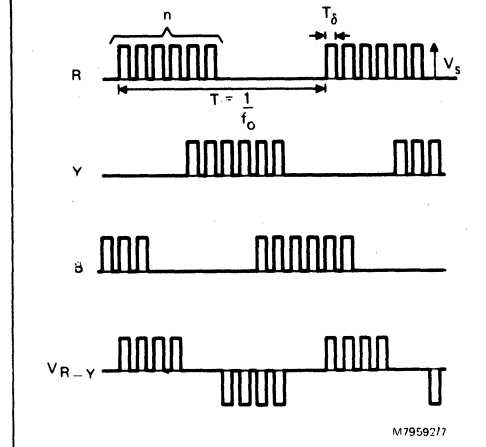

Fig.7 Pulsed quasi-square waveforms

tude V_s, pulse-width T_δ, during each half-period.

The average line output voltage for half a period is given by:

$$V_{(R-Y)av} = V_s \times n \times \frac{2}{3} \times T_\delta \times \frac{2}{T},$$

$$= V_s \times \frac{4n}{3} \times T_\delta \times f_o.$$

The output voltage $V_{(R-Y)av}$ is therefore proportional to the motor drive frequency f_o, assuming V_s, n, and T_δ are fixed, and so the induction over the whole speed range is constant. However, for a fixed number of pulses per cycle, system performance is limited at high speeds

by the high inverter switching frequency required, and at low speeds by the pulsating torques produced.

The performance of the pulsed quasi-square-wave system can be considerably improved by increasing the number of pulses per half-period as the motor speed decreases. The pulse-width T_δ has to be decreased at the same time so that the total half-period voltage-time product remains constant. This increase in pulse number reduces the level of the harmonics in the motor current to a level comparable with the simple quasi-square-waveforms. However, the harmonic spectra associated with the quasi-square-waveforms (Fig.8a) give rise to significant motor losses requiring derating of the motor.

PWM control of a.c. motors using an LSI circuit

The motor performance obtained using the quasi-square inverter system can be improved by using the technique of sinewave-modulated pulse-width modulation (PWM). Many types of sinusoidal PWM systems have been developed in the past, but each system has had its own shortcomings, such as circuit complexity, cost, and output variation with temperature, etc. Our approach overcomes all of these problems by using a purpose-designed LSI circuit type HEF4752V for signal generation. This IC uses a totally digital approach and is fabricated using the LOCMOS process. A block diagram of the system is shown in Fig.9, and the PWM section, the most important part of this diagram, is described below.

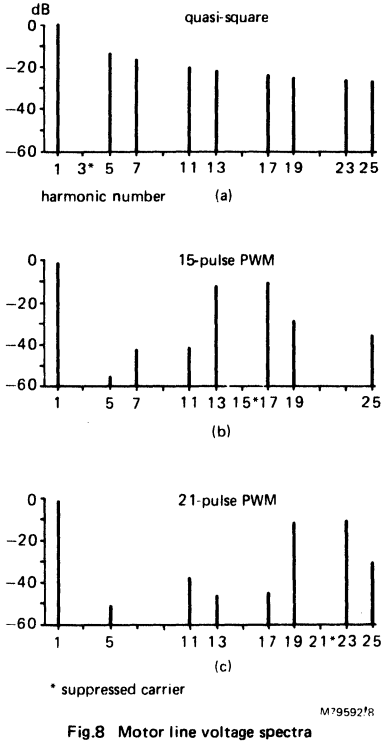

Fig.8 Motor line voltage spectra

The IC provides three complementary pairs of output drive waveforms which, when applied to a three-phase bridge inverter, produce a symmetrical three-phase (120°) output. Data inputs for reversing, start/stop, and interlock delay selection are provided. Twelve PWM outputs, together with monitoring and synchronising signals, are available for user control.

The output waveforms are pulse-width modulated using double-edged modulation such that the average voltage difference between any two of the three output phases varies sinusoidally, and this is illustrated in Fig.10 using a nine-pulse waveform for clarity. Figure 10a shows the unmodulated inverter output, 10b shows the double-edge modulated R-phase, 10c and 10d show the double-edge-modulated Y and B phases. The line-to-line voltage obtained by subtracting the R and Y phases is shown in Fig.10e. Double-edged modulation combined with odd multiple-of-three values for pulse number or frequency ratio n would give perfect line-to-line voltage waveform symmetry as illustrated in Fig.10e. The term n is defined as the ratio of switching frequency to motor drive frequency. In practice, the following eight pulse numbers (n) were chosen:

$$n = 15, 21, 30, 42, 60, 84, 120, 168.$$

Figure 8 compares the harmonic spectra of a quasi-square-waveform to the PWM waveforms with n = 15 and n = 21. The information in Fig.8 is also given in Table 1. These PWM harmonic patterns together with the variable pulse number operation produce low motor losses and smooth starting performance.

The relationship between the motor drive voltage and frequency is inherently linear, but separate control of voltage and frequency is possible if required. Double-edged modulation has the advantage of giving twice the number of line voltage pulses for any given switching frequency, resulting in substantially lower values for motor current ripple compared with single-edged modulation systems. The system has a built-in over-modulation capability which permits the PWM waveform to become a quasi-square waveform in the limit condition. This facility is useful in retro-fit applications where a standard induction motor is fitted to machinery and variable speed operation up to the same top speed is required.

The integrated circuit has four clock inputs which define motor frequency, motor Hz/volt, bridge switching

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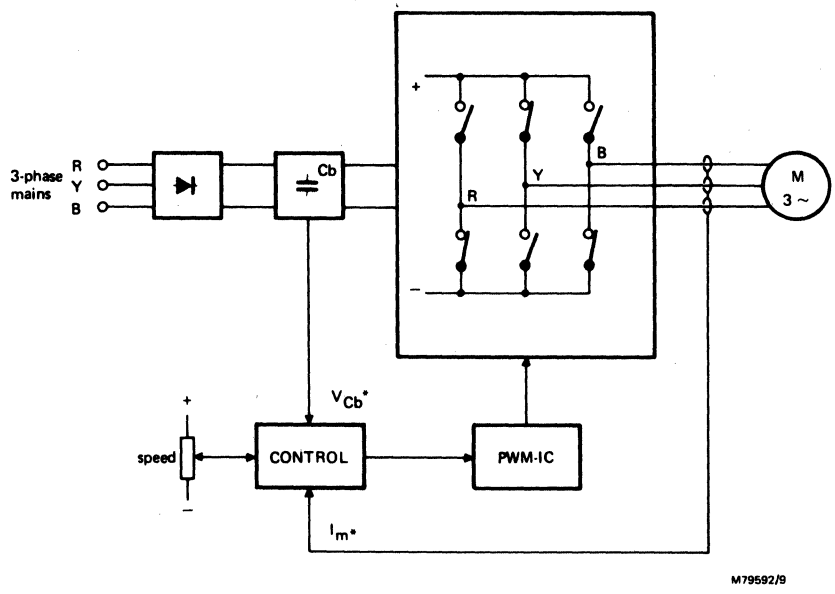


Fig.9 Voltage-source PWM inverter system

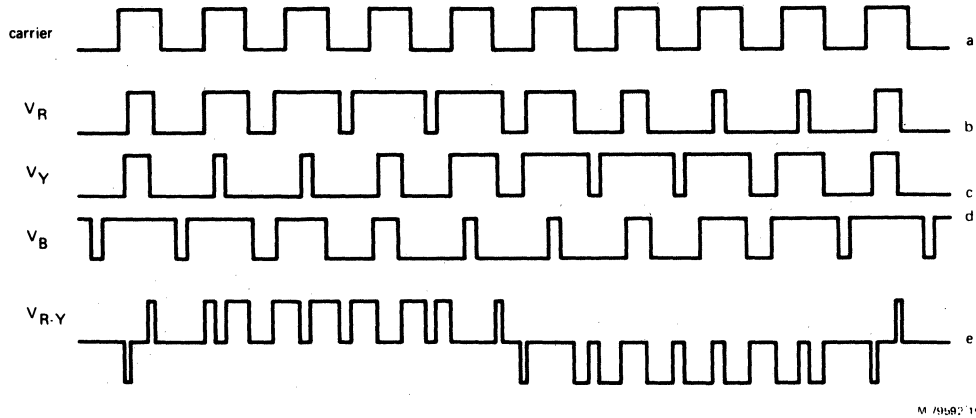


Fig.10 9-pulse sinusoidal PWM waveforms

TABLE 1

Harmonic contents for quasi-square, 15-pulse, and 21-pulse waveforms

Harmonic number	A_1	A_5	A_7	A_{11}	A_{13}	A_{17}	A_{19}	A_{23}	A_{25}
Quasi-square wave	1.103	0.221	0.157	0.100	0.085	0.065	0.058	0.048	0.044
15-pulse waveform*	0.881	0.002	0.007	0.009	0.248	0.305	0.038	0.001	0.016
21-pulse waveform*	0.881	0.003	0.001	0.014	0.005	0.006	0.257	0.295	0.031

*At 100% modulation

All tabulated values are referenced to the a.c. supply voltage source.

frequency, and minimum pulse width. The inverter switching frequency f_s is an integral multiple of the motor drive frequency f_o, that is:

$$f_s = nf_o.$$

Figure 11 shows typical operation with the maximum switching frequency set to 1 kHz. A small amount of hysteresis is included at the pulse number change points to ensure that jitter is avoided when operating in these regions. The minimum switching frequency is set internally by the LSI circuit to:

$$f_{s\,(min)} \simeq 0.6\, f_{s\,(max)}.$$

The frequency of the motor line-current ripple is held

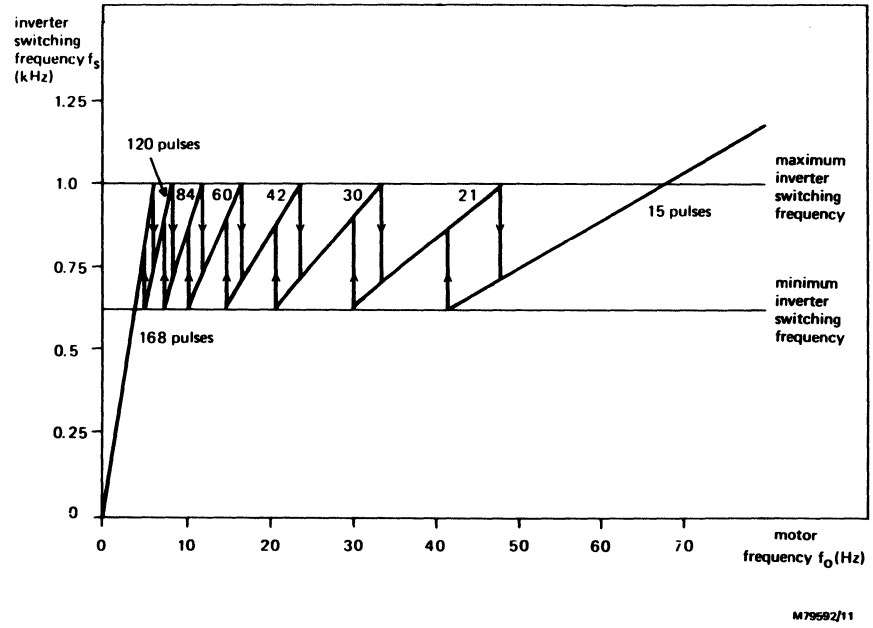
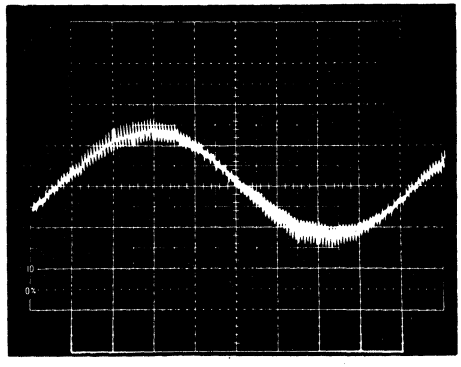
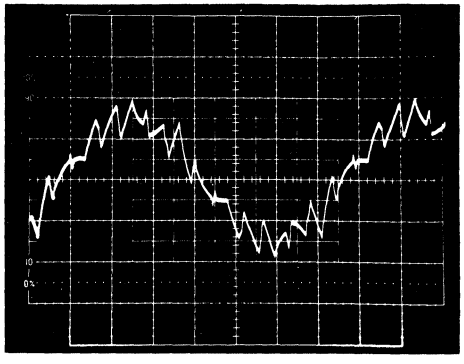


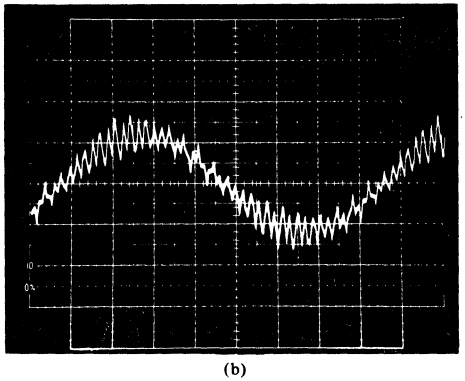
Fig.11 Inverter switching frequency versus motor drive frequency with pulse number as a parameter



(a)



(c)



(b)

Fig.12 Line current waveforms at various motor drive frequencies:
(a) motor drive frequency = 10 Hz
pulse number = 60
(b) motor drive frequency = 25 Hz
pulse number = 21
(c) motor drive frequency = 50 Hz
pulse number = 9

within a band of constant width over an operating motor drive frequency range of greater than 18.5:1.

Figure 12 shows the resultant line currents at various frequencies for a 2.2 kW motor system using a maximum switching frequency of 1 kHz.

Single section of three-phase inverter

The inverter circuit design required for PWM using the LSI circuit type HEF4752V is composed of three completely independent choppers, one for each of the phases R, Y, and B. A circuit diagram of a section of such an inverter is shown in Fig.13.

The circuit contains four thyristors: two main thyristors Th_1 and Th_2 which chop the rectified mains, and two commutation thyristors Th_3 and Th_4 which force-commutate Th_1 and Th_2. The trigger pulses for the thyristors are supplied via pulse amplifiers and trigger pulse transformers. The motor current I_m is conducted alternatively via Th_1 and the flywheel diode D_2, or via Th_2 and D_1. The commutation circuit for Th_1 is composed of the elements Th_3, D_3, L_2, and C_1, and flywheel diode D_1.

The anti-parallel connection of the main thyristor-diode combination (for example Th_1 and D_1) avoids the need to use reverse voltage commutation which is particularly important since it permits the use of modern high-speed asymmetric thyristor types having only a few volts reverse blocking capability.

The operating principle of the commutation circuit can be understood with reference to Fig.14 which shows only the basic elements of the commutation circuit associated with main thyristor Th_1. It is assumed that the capacitor C_1 is charged to the supply voltage with the polarity marked 'a' and Th_1 is conducting the load current I_m and is required to be turned off. Commutation is initiated by triggering the auxiliary thyristor Th_3. This action causes a sinusoidal resonant current to flow via Th_3, L_2, and C_1 in the direction indicated by the arrow marked 'A'. At the end of the half-cycle of sinusoidal

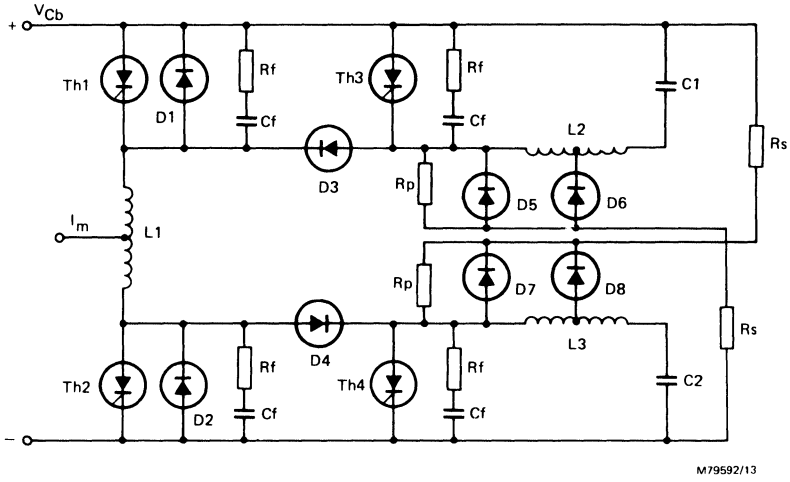


Fig.13 One phase of three-phase PWM inverter

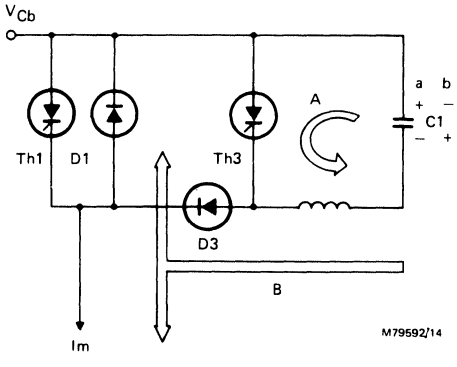


Fig.14 Principle of auxiliary commutation

current the voltage polarity of C_1 is now reversed (marked 'b'), the current through Th_3 is zero and Th_3 turns off. The direction of capacitor current now reverses, and the second half-cycle of sinusoidal resonant current begins to flow in the directions indicated by the arrow marked 'B'. As the current through D_3 increases during the resonant half-cycle, so the load current I_m is increasingly supplied from the resonant circuit. A point is reached when no current is supplied through Th_1 and the thyristor turns off. Any excess current flows through D_1, and the duration of conduction of D_1 provides the turn-off interval. During the fourth quarter-cycle when the current in D_3 is again reduced to the load current I_m, forward voltage is then reapplied to both thyristors Th_1 and Th_3, and the capacitor voltage polarity is now restored to the initial condition marked 'a' and commutation of Th_1 is complete.

The second half-sinewave of current which commutates-off Th_1 has an amplitude I_{cp} and a period T_{cp} given approximately by:

$$I_{cp} = V_{Cb}\sqrt{(C_1/L_1)},$$

$$T_{cp} = \pi\sqrt{(L_2C_1)},$$

where C_1 = commutation capacitance and L_2 = commutation inductance.

The values of C_1 and L_2 must be chosen so that the commutation current in L_2 exceeds the maximum peak load current I_m for the commutation turn-off, 't_q value' of the thyristor Th_1.

In the inverter section shown in Fig.13, the values of L_2 and C_1 required are determined by the maximum motor peak current, the minimum d.c. voltage $V_{Cb(min)}$, and the required turn-off time t_q of Th_1, as given in the following equations:

$$L_2 \triangleq \frac{0.4\, V_{Cb(min)} \times t_q}{I_{m(pk)}},$$

$$C_1 \geq \frac{t_q \times I_{m(pk)}}{V_{Cb(min)}}.$$

An RC filter is connected across each thyristor to ensure that, after commutation the rate of rise of reapplied voltage dV/dt does not exceed the thyristor rating. Diodes D_6 and D_8 with the resistors R_s provide critical

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damping of the L_2C_1 and L_3C_2 circuits at the end of a commutation cycle. Diodes D_5 and D_7 limit the maximum peak voltages across the thyristors to slightly more than the d.c. supply voltage.

For good performance, smooth operation at low speeds, and high electrical efficiency, it is necessary to operate the inverter at a relatively high PWM switching frequency. This requires the use of thyristors with short t_q times and high reapplied dV/dt ratings together with correspondingly fast diodes. Suitable thyristors and fast diodes are available from our range.

A.C. MOTOR SPEED CONTROL SYSTEM USING HEF4752V

An example of a practical drive system has been designed round our fast thyristors and the PWM IC type HEF4752V (see Fig.15). The type of thyristors, and the design of the power section, are determined by the power rating of the motor which is to be controlled.

System specification

The specification of the described system includes:

- Mains input: standard three-phase, 380 to 415 V, 50 Hz
- Fast dynamic speed response (accelerating and decelerating)
- Output frequency: 0 to 100 Hz (bidirectional speed control)
- Output voltage: up to 415 V r.m.s. (line-to-line) for 415 V r.m.s. line voltage input
- Fast dynamic braking

Control system

The control system provides the following facilities.

- Adjustment of motor speed, from zero up to twice nominal speed. Remote control is possible by an externally supplied control voltage.
- Adjustment of maximum motor current up to about 150% of the nominal value.
- Adjustment of the acceleration and deceleration time during motor speed variation.

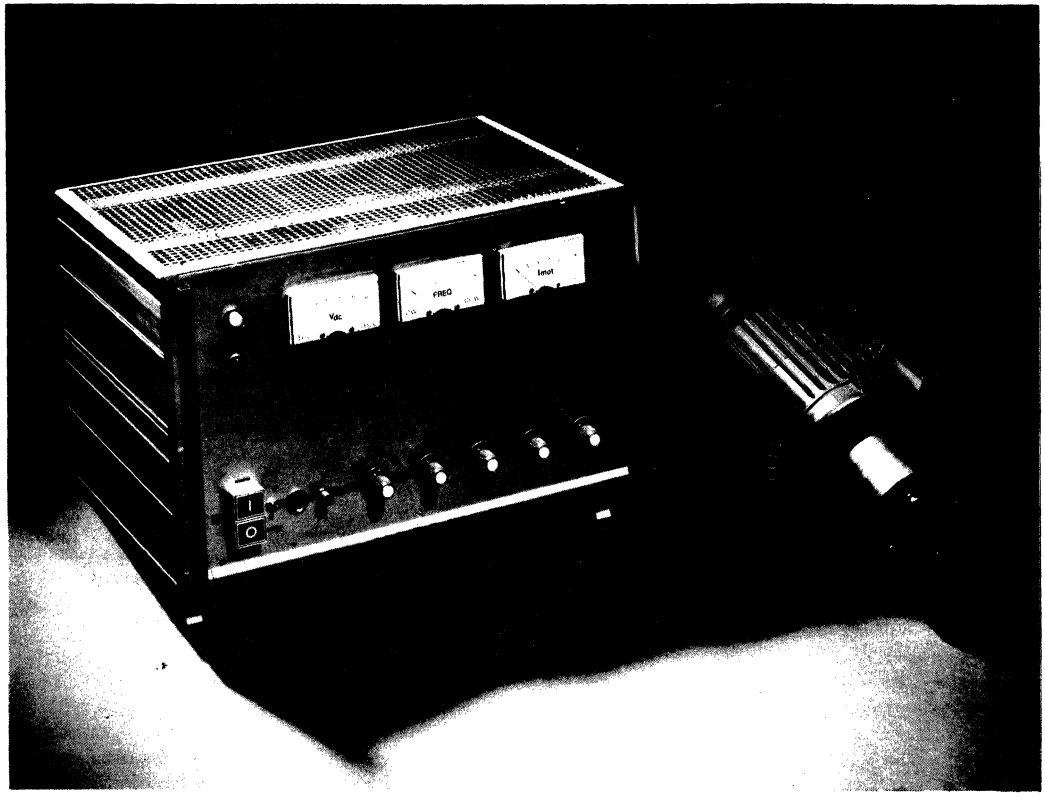

Fig.15 2,2 kW PWM a.c. motor control system

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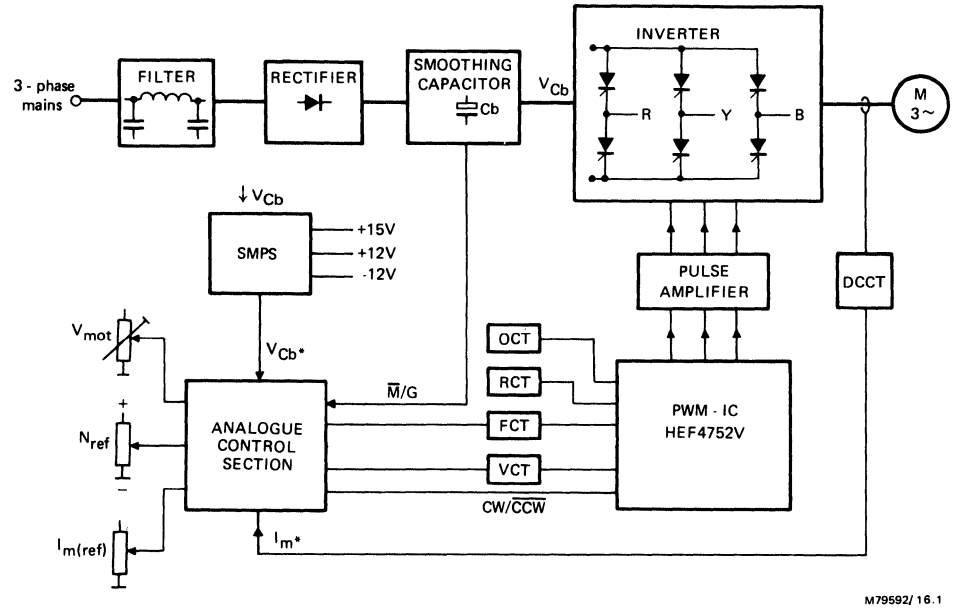

Fig.16 PWM motor control system using HEF4752V

- Limitation of power regenerated during speed deceleration to protect the inverter against overvoltage.
- Adjustable slip correction to improve speed regulation with load variation.
- Adjustable 'IR' compensation to increase the starting torque.

The basic speed control system is shown in Fig.16. The mains input is connected to the rectifier via an interference filter which ensures that mains pollution caused by the inverter remains below CISPR and VDE limits. The d.c. voltage V_{Cb} is smoothed by a smoothing capacitor and then applied to the inverter. The inverter delivers the three-phase output voltages for the a.c. motor. The d.c. supply voltage is also connected to an SMPS, which provides the low-voltage supply for the control section.

To limit motor current and V_{Cb} during overload or braking conditions, the following three feedback signals are supplied to the control section.

- A voltage V_{Cb}*, from the SMPS: this signal is proportional to the d.c. voltage across the smoothing capacitor. Without some form of voltage limitation, the d.c. voltage across the smoothing capacitor can become excessive under uncontrolled braking conditions. V_{Cb}* is also used to provide safe operating conditions during switch-on and switch-off.
- A signal M/G: this signal is also derived from the smoothing capacitor voltage, and indicates the direction of power flow in the drive system (motor mode or generator mode).
- The motor current signal I_m*: this is sensed by a D.C. Current Transformer (DCCT) in the motor current lines.

The twelve thyristors of the inverter section are triggered by the PWM IC, the HEF4752V, via pulse amplifiers and trigger transformers. The HEF4752V generates the sinusoidal pulse-width modulated signals. The following four clock inputs VCT, FCT, RCT, OCT define the operating conditions of the IC.

- VCT (Voltage Clock Trigger). This determines the output frequency/voltage ratio (Hz/V).
- FCT (Frequency Clock Trigger). This determines the motor supply frequency, thereby controlling the motor speed.
- RCT (Reference Clock Trigger). This sets the inverter maximum switching frequency.
- OCT (Output Clock Trigger): This sets the minimum pulse-width allowable.

The CW input to the HEF4752V determines the direction of motor rotation. The motor can only be reversed when the FCT clock is stopped. Both FCT and

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VCT are generated in the control section. Motor speed, maximum motor current, and motor voltage are adjustable by potentiometer settings N_{ref}, $I_{m(ref)}$, and V_{mot}. However, under overload and regenerative conditions, the motor speed is also controlled by the motor current and the d.c. voltage across the smoothing capacitor. The analogue control section provides the required start and stop signals to ensure safe switching on and off of the power section.

Speed reference circuit

The speed reference circuit provides the voltage control signal for the FCT clock pulse generator. The input speed reference signal can be adjusted by potentiometer, N_{ref} from −10 V to +10 V, varying the motor speed from maximum clockwise to maximum counter clockwise. A functional diagram of the circuit is given in Fig.17. The circuit rectifies the input signal. The output signal can be expressed as $V_N = -k|N_{ref}|$. The required direction of rotation is given by the digital CW/$\overline{\text{CCW}}$ output signal.

The output V_N is derived from the signal N_{ref} via a comparator (1) and an integrator (2). A stepwise variation of N_{ref} results in a linear increase or decrease of the output signal V_N. The rate of variation of V_N can be adjusted via the accelerate/decelerate limiting potentiometers A and D, as shown in the waveforms of Fig.18. This control of maximum speed variation protects the drive system, and is useful for achieving special speed change characteristics. Inverter protection against excessive motor currents and against excessive voltage across the smoothing capacitor during a regenerative mode is given by the I_{lim} signal, obtained from the current voltage control circuit (see next section). A motor current which exceeds the preset current limit under motoring conditions (such as a stalled motor), will result in a negative signal of I_{lim}. The negative value of V_N will be

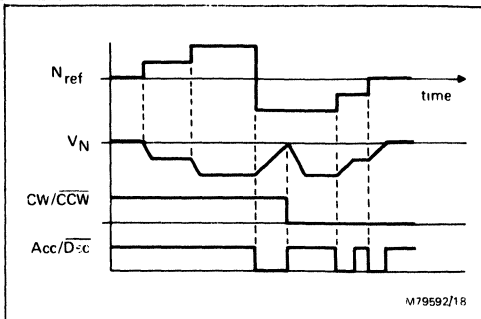

Fig.18 Performance of speed reference control system

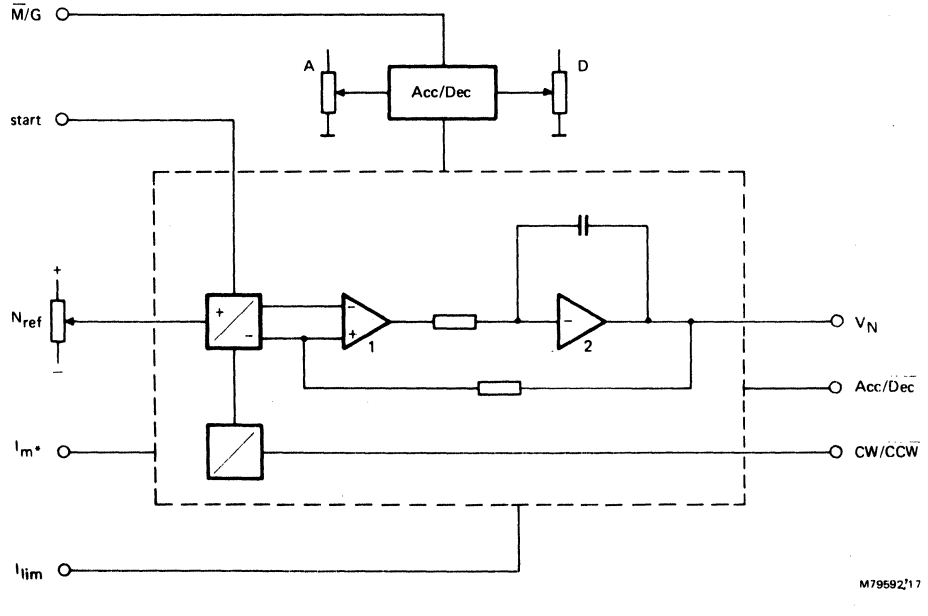

Fig.17 Speed reference control system

decreased, resulting in a lower output frequency of the inverter, thereby reducing the slip and the motor current.

Under regenerative conditions, I_{lim} will be positive if the preset limits for current or voltage across the smoothing capacitor are exceeded. This action increases the value of $-V_N$, and thus increases the output frequency. In this way the frequency difference between inverter and rotor (slip frequency) is decreased, thereby reducing the braking torque of the motor.

For correct current control, the $\overline{M}$/G signal is also supplied to the accelerate/decelerate limiting circuit. Motor acceleration is prevented as long as the $\overline{M}$/G signal indicates the generator mode. A second digital input is provided by the start signal which releases the output V_N after the start procedure. To improve the motor speed stability, a signal I_m* can be applied to the input of the first comparator (1). This signal increases the inverter output frequency when the motor torque is high (slip correction).

Current/voltage limitation

As mentioned in the previous section, the inverter should be protected against excessive current and voltage. The current and voltage control loops that provide this protection are shown in Fig.19.

The motor current is measured by three d.c. current transformers connected between the inverter output and motor. If the motor current exceeds the value set by the potentiometer $I_{m(ref)}$, I_{lim} becomes negative, resulting in reduction of the inverter output frequency and hence the motor torque.

During braking, when power is regenerated to the d.c. supply source, the voltage across the smoothing capacitor V_{Cb} rises above its normal value. This increase results in an activation of the $\overline{M}$/G signal from the mains supply section, and the lower control section of Fig.19 becomes operative. As soon as the braking current signal I_m* exceeds the value of $I_{G(ref)}$, a positive voltage is generated at the I_{lim} output. The inverter output frequency is therefore increased and the braking torque reduced. If the voltage across the smoothing capacitor exceeds the preset maximum level $V_{Cb(ref)}$, the comparator (3) reduces the reference value $I_{G(ref)}$ of the current comparator (4). The braking torque will then be reduced to a level where the regenerated power is just compensated by power losses of the inverter, the SMPS, and the motor. As a result of this control principle, the maximum braking action is always available.

Motor voltage control

To improve the low-speed torque of the motor, required for such load conditions as compressors and vehicle drive systems requiring a high starting torque, it is necessary

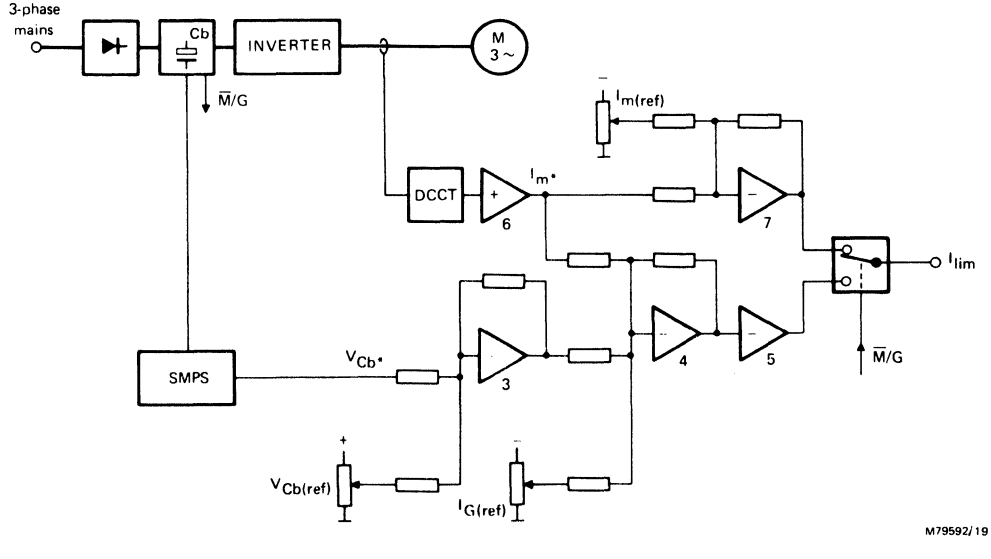

Fig.19 Current and voltage limit control system

to increase the motor voltage at low speed. This function, which compensates for the relatively high 'IR' losses at low speed, is obtained by decreasing the frequency of the VCT clock at the low end of the speed range. The circuit can be adjusted with three potentiometers giving control over the following conditions:

1) the motor voltage at nominal speed,
2) the speed range for 'IR' compensation,
3) the maximum 'IR' compensation at zero speed.

APPLICATIONS

The stage of technological evolution has now been reached where it is cost-effective to manufacture general-purpose high-quality industrial variable-speed drives using three-phase induction motors. This has been made possible by recent advances in power semiconductors and the introduction of a purpose-designed LSI circuit for signal generation.

The system described in this article illustrates one method of producing a high-performance variable-speed drive for a three-phase induction motor, using the most advanced power semiconductors and LSI technology now available. Typical applications of variable-frequency a.c. inverters include:

- textile manufacturing,
- chemical processing,
- glass manufacture,
- machine tools,
- polymer forming,
- food processing,
- material handling and packaging,
- printing and paper making,
- grinders,
- pumps.

In these and many other applications, the electronic motor control system described in this article provides improved efficiency, compactness, and control flexibility.

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LSI Circuit for AC Motor Speed Control

AN136

B.G. STARR and J.C.F. van LOON

In the past, sinusoidal Pulse-Width Modulation (PWM) speed control systems for three-phase a.c. motors have been produced in a number of different forms. However, no single system has been completely satisfactory. High costs, circuit complexity, output variation with temperature, etc. have all prevented the widespread application of this potentially attractive method of a.c. motor speed control. This article describes a purpose-designed LSI circuit, type HEF4752V, which has been developed specifically for signal generation in such systems, and overcomes all the previous disadvantages. The IC is manufactured using locally-oxidised complementary MOS technology (LOCMOS) and is mounted in a standard 28-pin dual-in-line package.

This is the third in a series of articles all devoted to our a.c. motor speed control system. A general introduction to this subject is given in Refs.1 and 2, and a description of an inverter circuit developed specifically for the system is given in Ref.3.

PWM CONTROL OF A.C. MOTORS

A block diagram of our PWM speed control system is shown in Fig.1. In this system, the output waveforms from the three phases Red (R), Yellow (Y), and Blue (B) of a six-element inverter consist of sinusoidally modulated trains of carrier pulses, both edges of each pulse being modulated to give an average voltage difference between any two of the output phases which varies sinusoidally. This is illustrated in Fig.2 for a carrier wave having 15 pulses for each cycle of the inverter output.

Figure 2a shows the 15-fold carrier, Fig.2b the double-edge modulated R-phase, and Figs.2c and 2d show the double-edge modulated Y and B phases. The line-to-line voltage obtained by subtracting the Y-phase from the R-phase is shown in Fig.2e.

A detail of the double-edge modulation of a carrier wave is shown in Fig.3. Each edge of the carrier wave is modulated by a variable time δ, where δ is proportional to $\sin\alpha$, and α is the angular displacement of the unmodulated edge. The modulation of a 15-fold carrier requires a total of 30 δ values.

The modulation of the output waveforms is achieved by opening and closing the upper and lower switching elements (transistors or thyristors) in each phase of the inverter. Closing the upper element gives a high output voltage, and closing the lower element gives a low output voltage. The basic function of the PWM IC is to provide three complementary pairs of output drive waveforms which, when applied to the six-element inverter, open and close the switching elements in the appropriate sequence to produce a symmetrical three-phase output. The drive waveforms are supplied to the inverter via buffer amplifiers with isolation where necessary. The integrated circuit is completely digital, so that the repetition frequency of the PWM signal (switching frequency) is always an exact multiple of the inverter output frequency. This results in excellent phase and voltage balance and consequent low motor losses.

A 15-fold carrier multiple is used only for the highest motor speed range. To improve the pulse distribution at lower motor speeds the switching frequency is derived from higher multiples of the inverter output frequency. A hysteresis between the switching points is included to avoid jitter when operating in these regions. Typical

LSI Circuit for AC Motor Speed Control AN136

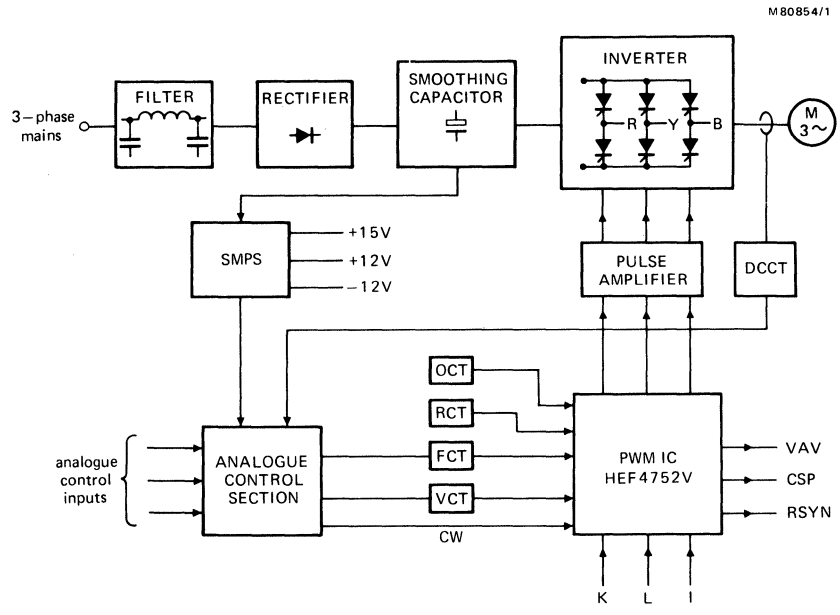


Fig.1 PWM motor control system using HEF4752V

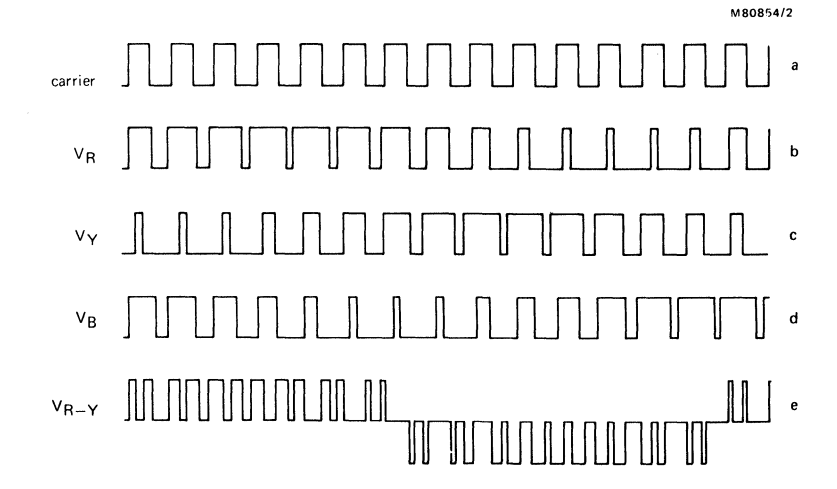


Fig.2 15-pulse sinusoidal PWM waveforms

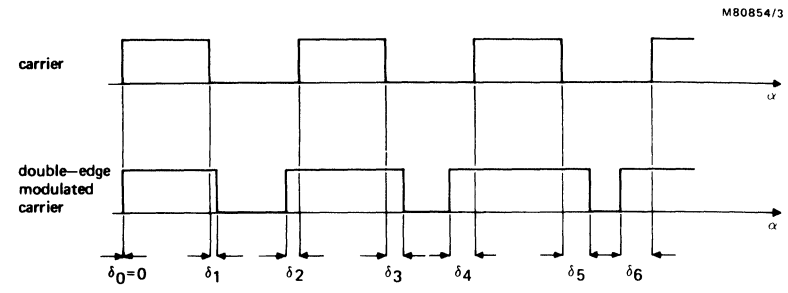


Fig.3 Detail of double-edge modulation

values of the carrier multiple and the output frequency are given in Table 1. It should be noted that this table applies only for a particular set of input conditions. The selection of input conditions is discussed later in this article.

For the values shown in Table 1, the IC has full control of the inverter switching frequency for output frequencies in the range 4.0 to 71.3 Hz. For output frequencies greater than 71.3 Hz, the switching frequency will increase beyond 1070 Hz until over-modulation is reached. Over-modulation implies a merging of adjacent pulses, with a corresponding reduction in switching frequency, until eventually a quasi-square output waveform is obtained. The point at which over-modulation occurs is determined by two of the clock inputs of the IC: VCT and FCT. This is covered in detail under the discussion of the VCT clock input. The practical upper limit on the output frequency is determined by the rating of the motor under control, the design of the inverter, and the performance of the IC. Detailed advice on the recommended maximum output frequency is also given under the discussion of the VCT clock input.

TABLE 1

Variation of carrier multiple with output frequency

Output frequency range Hz	Carrier multiple	Switching frequency Hz
0 to 4.0	168	0 to 675
4.0 to 6.4	168	675 to 1070
5.7 to 8.9	120	675 to 1070
8.1 to 12.8	84	675 to 1070
11.2 to 17.9	60	675 to 1070
16.3 to 25.5	42	675 to 1070
22.3 to 35.7	30	675 to 1070
32.5 to 51	21	675 to 1070
44.6 to 71.3	15	675 to 1070
71.3 +	15	See text

HEF4752V INTERNAL ORGANISATION

A block diagram indicating the internal organisation of the IC is shown in Fig.4. The circuit comprises three counters, one decoder, three output stages, and a test circuit. The test circuit is used primarily for testing the IC during manufacture, and is not discussed in this article. The operation of the IC is now considered in outline, and this is followed by a detailed discussion of the various input/output functions.

The three output stages (Fig.4) correspond to the R, Y, and B phases of the inverter. Each output stage has four outputs: two main outputs which control the upper and lower switching elements in each phase of the inverter, and two auxiliary outputs used to trigger commutation thyristors in 12-thyristor inverter systems. As explained above, the essential function of the IC is to provide the output waveforms which open and close the upper and lower inverter switching elements in the appropriate sequence. This is achieved by alternately switching between the upper and lower main outputs in each output stage. To ensure that the main outputs cannot be on simultaneously, an interlock delay period is used to separate the on condition of the upper and lower outputs. The interlock delay period is determined by inputs OCT and K, while the switch between the main outputs is controlled by an internally-generated control signal. A change in the level of this control signal causes the HIGH main drive output to switch off, and then after the interlock delay period, causes the LOW main drive output to switch on. With the interlock delay period fixed, variations in motor speed are produced by changes in the control signal, and a description of the production of this signal provides a basic understanding of the operation of the IC.

The control signal is derived from the carrier wave modulated by the appropriate δ values. Production of the control signal therefore requires the determination of the correct carrier frequency, and the corresponding δ modulations. The carrier frequency, which is equal to the product of the output frequency and the carrier multiple, is set by the FCT counter and the RCT counter. Dividing the clock input of the FCT counter by 3360 gives the output frequency, while the correct carrier multiple is determined by gating RCT clock pulses into the RCT counter, with a gating time equal to a fixed number of FCT clock pulses. For a given frequency of the RCT clock, the number of pulses counted in the gating time will fall as the frequency of the FCT clock increases, and this is used to derive a correspondingly lower value of the carrier multiple.

For each value of the carrier multiple, the decoder holds a corresponding set of δ values. Each δ value is

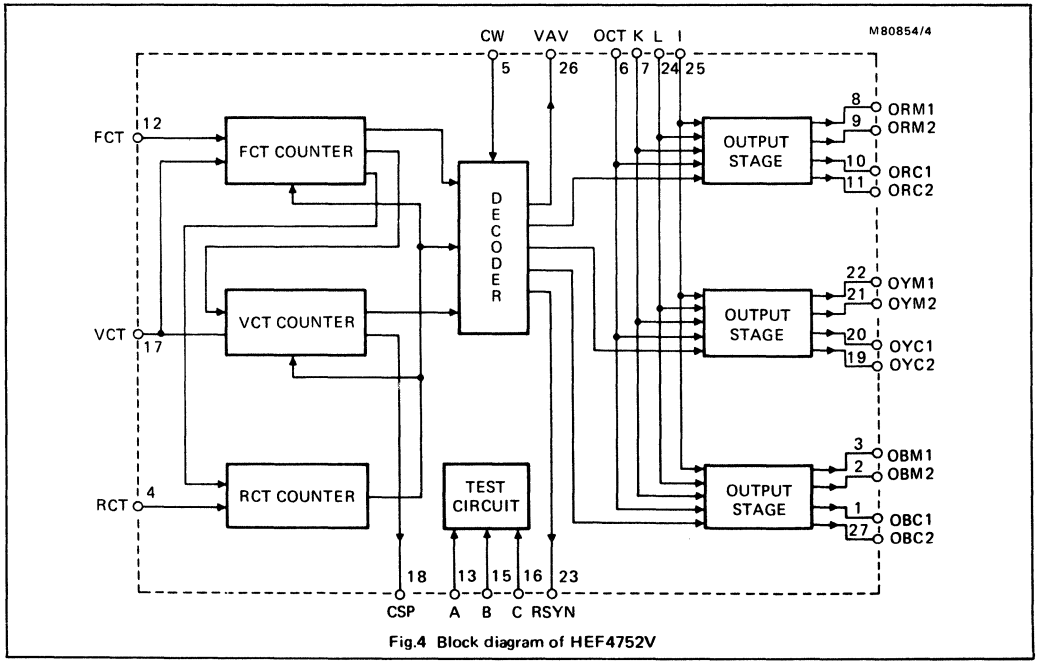


Fig.4 Block diagram of HEF4752V

stored as a number, and the width of the corresponding modulation is determined by the rate at which this number is counted. The counting frequency used is the VCT clock input, and the modulation depth is therefore inversely proportional to the frequency of the VCT clock input.

From the carrier frequency, and the δ modulations, the decoder finally assembles the control signal. A total of three control signals is produced by the decoder, one for each output stage, with a phase difference of 120° between each signal.

INPUT/OUTPUT FUNCTIONS OF THE HEF4752V

A pinning diagram of the HEF4752V IC is shown in Fig.5. The IC has 12 inverter drive outputs, three control outputs, four clock inputs, and seven data inputs.

Inverter drive signals

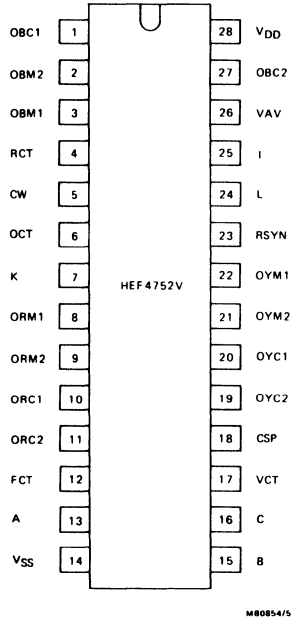
There are six main drive outputs which are arranged in complementary pairs. The pins are coded as follows.

First letter	O (output)
Second letter	R, Y, or B (phase indication)
Third letter	M (main)
Number	1 for output of upper switching element, or 2 for lower switching element

For example, ORM2 is the main drive waveform for the Red phase lower switching element.

Associated with each main output is the auxiliary output used to trigger the commutation thyristor in 12-thyristor inverter systems. These outputs are identified by a C as the third letter of the pin code, so that ORC2 is the commutation trigger pulse output associated with ORM2.

The inverter drive signals can be obtained in two



PINNING

Inverter drive signals		
8	ORM1	R-phase main
9	ORM2	R-phase main
10	ORC1	R-phase commutation
11	ORC2	R-phase commutation
22	OYM1	Y-phase main
21	OYM2	Y-phase main
20	OYC1	Y-phase commutation
19	OYC2	Y-phase commutation
3	OBM1	B-phase main
2	OBM2	B-phase main
1	OBC1	B-phase commutation
27	OBC2	B-phase commutation
Data inputs		
24	L	data
25	I	data
7	K	data
5	CW	data
13	A	data
15	B	data
16	C	data
Clock inputs		
12	FCT	frequency clock
17	VCT	voltage clock
4	RCT	reference clock
6	OCT	output delay clock
Control outputs		
23	RSYN	R-phase synchronisation
26	VAV	average voltage
18	CSP	current sampling pulses

Fig.5 Pinning diagram

forms, one mode for driving transistor inverters, the other for thyristor inverters. The form produced by the IC is determined by the logic level applied to the data input I.

Data inputs

Data inputs I, K, and L

As explained above, input I determines whether the inverter drive signals are in the thyristor or transistor mode. Input I LOW corresponds to the transistor mode; input I HIGH corresponds to the thyristor mode. In the transistor mode the main upper and lower switching elements in the inverter are switched HIGH alternately, with an interlock delay period (both switches LOW) at each changeover. During the delay period the commutation output associated with the off-going main output is set HIGH. The data input K, in association with the clock input OCT, is used to adjust the length of the interlock delay period. The details of this adjustment are described under the discussion of clock input OCT.

Input L provides a stop/start facility. In the transistor mode, with L LOW, all main and commutation signals are inhibited, and with L HIGH, the normal modulated block pulses continue. The action of L inhibits the actual output circuits only, so that while L is LOW the internal circuits generating the output signals continue to operate. Typical output waveforms for the transistor mode are shown in Fig.6. Figures 6a to 6d show the normal inverter drive outputs, and Fig.6e shows the internally-generated control signal which effects the transition between the upper and lower main drive outputs. Figures 6g to 6j illustrate the influence of changes in the level of input L (Fig.6f) on the inverter drive outputs.

With input I HIGH, thyristor mode, the main outputs become pulse trains with a mark-space ratio of 1:3, and the commutation outputs become a single pulse lasting for the first quarter of the interlock delay period. This is used to facilitiate the use of trigger transformers for isolation purposes. The interlock delay period is set in the same way as that used in the transistor mode, but in this case the logic level at input K and the frequency of OCT also control the frequency of the main output pulse trains, which in turn will affect the choice of trigger transformer. The delay period is selected to allow time for the commutation circuit to operate and reset in the 12-thyristor circuit, or to set the minimum pulse width for the six-thyristor self-commutated circuit. In this mode, with L LOW, the three lower switching elements in the inverter are triggered continuously, the upper elements being inhibited. Typical output waveforms for the thyristor mode are shown in Fig.7.

Data input CW

The phase sequence input CW is used to control the direction of rotation of the motor by altering the phase sequence. This is illustrated in Table 2. The phase sequences shown in Table 2 represent the order in which the phases pass through zero voltage in a positive direction.

TABLE 2

Phase sequence input CW

Input CW	Phase sequence
LOW	R, B, Y
HIGH	R, Y, B

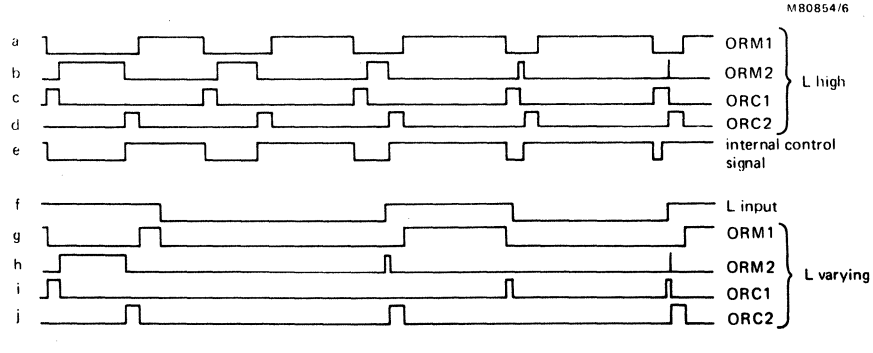


Fig.6 Typical output waveforms for transistor mode

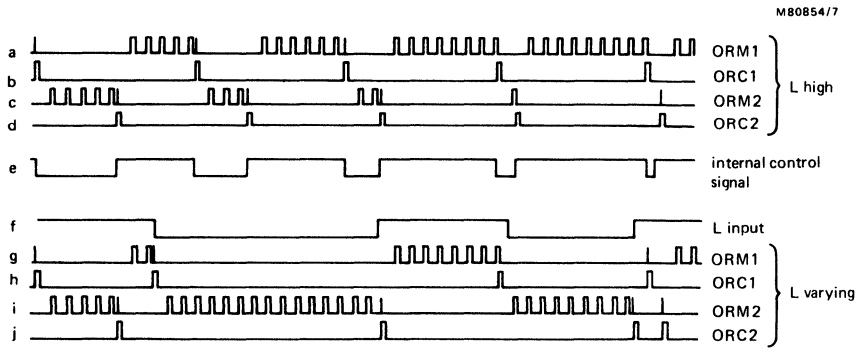


Fig.7 Typical output waveforms for thyristor mode

Data inputs A, B, and C

The three inputs A, B, and C are provided for use during production testing. They are not used during normal operation, when they must be connected to V_{ss} (0 V). Input A HIGH initiallises all the IC circuits, and can be used for reset. The use of input A is considered in detail below under the discussion of switch-on conditions.

Clock inputs

There are four clock inputs which are used to control the output waveforms. The following sections give a guide to selecting the frequency, or range of frequencies, for each clock.

Frequency control clock FCT

The clock input FCT controls the inverter output frequency f_{out}, and therefore the motor speed. The clock frequency f_{FCT} is related to f_{out} by the following equation:

$$f_{FCT} = 3360 \times f_{out}.$$

It is permissible to stop the FCT clock during system operation, the effect being to switch the outputs to either all M1 or all M2 outputs, and this occurs irrespective of the state of input I.

Voltage control clock VCT

An induction motor is governed by the general expression:

$$V = N\frac{d\Phi}{dt},$$

so that to maintain constant motor flux, the voltage-time product Vt must be kept constant. The IC automatically satisfies this requirement by making the output voltage directly proportional to the output frequency. The level of the average inverter output voltage, at a given output frequency, is controlled by the VCT clock input, changes in output voltage being achieved by varying the modulation depth of the carrier. Increasing f_{VCT} reduces the modulation depth, and hence the output voltage, while decreasing f_{VCT} has the opposite effect.

The maximum undistorted sinusoidal output voltage, which is obtainable in a given system, is determined by the voltage of the d.c. link, V_{link}; the maximum r.m.s. value of the fundamental component is given by $0.624 \times V_{link}$. This voltage occurs at 100% modulation of the carrier; that is, when some adjacent pulses are just about to merge. The output frequency at which this condition can apply in a given system is determined by the Vt product of the motor. The frequency at 100% modulation, $f_{out(m)}$, can be determined by relating the maximum r.m.s. inverter output voltage to the motor ratings as follows:

$$f_{out(m)} = f_N \times \frac{0.624 V_{link}}{V_N},$$

where f_N is the motor rated frequency and V_N the motor rated r.m.s. voltage.

Once $f_{out(m)}$ has been established, a value of f_{VCT} can be determined which will set the Vt product correctly throughout the frequency range of the motor to be controlled. This nominal value of f_{VCT} is denoted by $f_{VCT(nom)}$, and is related to $f_{out(m)}$ by:

$$f_{VCT(nom)} = 6720 \times f_{out(m)}.$$

With f_{VCT} fixed at $f_{VCT(nom)}$, the output voltage will be a linear function of the output frequency up to $f_{out(m)}$. Any required variation in this linear relation-

ship is obtained by changing f_{VCT}. For example, to double the output voltage at low frequencies, as a possible compensation for 'IR' losses, f_{VCT} is made equal to 0.5 $f_{VCT(nom)}$.

The frequency ratio f_{FCT}/f_{VCT} is important in system design. At 100% modulation it will have a value given by:

$$\frac{f_{FCT}}{f_{VCT(nom)}} = \frac{3360 \times f_{out(m)}}{6720 \times f_{out(m)}},$$

$$= 0.5.$$

Below 0.5 the modulation is sinusoidal, while above 0.5 the phase waveform approaches a squarewave, giving a quasi-squarewave line-to-line voltage. At approximately 2.5, the full squarewave is obtained. Above 3.0, the waveform becomes unstable as the internal synchronising circuits cannot function correctly, and 3.0 is therefore the recommended limit.

Reference clock RCT

RCT is a fixed clock which is used to set the maximum inverter switching frequency $f_{s(max)}$. The clock frequency, f_{RCT}, is related to $f_{s(max)}$ by the following equation:

$$f_{RCT} = 280 \times f_{s(max)}.$$

The absolute minimum value of the inverter switching frequency, $f_{s(min)}$, is set by the IC at 0.6 $f_{s(max)}$. These figures apply provided f_{FCT} is within the range 0.043 f_{RCT} to 0.8 f_{RCT}, and f_{FCT}/f_{VCT} is less than 0.5.

Figures 8 and 9 show the variation of inverter switching frequency plotted against output frequency with f_{RCT} = 280 kHz, and $f_{s(max)}$ = 1 kHz. To obtain the equivalent figures for different values of $f_{s(max)}$, both scales and f_{RCT} should be multiplied by the required value of $f_{s(max)}$ in kHz. For example, with $f_{s(max)}$ = 2 kHz, $f_{RCT} = 2 \times 280 = 560$ kHz, and referring to Fig.9, the value of f_s for f_{out} = 50 Hz (2 X 25) will be 1.5 kHz (2 X 0.75) at a pulse rate of 30 pulses per output cycle. Referring to Figs.8 and 9, it can be seen that the range of f_{out} that will keep f_s in the band 2 to 1.2 kHz will be 7.1 Hz (2 X 3.55) to 133 Hz (2 X 66.5), provided the ratio f_{FCT}/f_{VCT} is less than 0.5.

Output delay clock OCT

The OCT clock input, operating in conjunction with the data input K, is used to set the interlock delay period which is required at the changeover between the complementary outputs of each phase. For a thyristor inverter, where the output thyristors are triggered by a train of pulses (mark-space ratio 1:3), OCT and K have the additional function of determining the frequency of the pulse train.

The operation of OCT and K is shown in Table 3. Whenever possible input K should be HIGH as this keeps the jitter caused by lack of synchronisation between FCT and OCT to a minimum. In many cases a design economy can be obtained by using the same clock for both RCT and OCT.

Control outputs

Oscilloscope synchronisation RSYN

This is a pulse output of frequency f_{out} and pulse width identical to the VCT clock pulse. It is timed to occur just before the positive-going zero transition of the R-phase voltage. It therefore provides a stable reference for triggering an oscilloscope.

Output voltage simulation VAV

VAV is a digital waveform which simulates the average value of the expected line-to-line voltage of the inverter output; however, it excludes the effect of the interlock

TABLE 3

Operation of clock input OCT* and data input K

K	Interlock delay period ms	Trigger pulse frequency kHz	Trigger pulse width ms
LOW	$8/f_{OCT}$	$f_{OCT}/8$	$2/f_{OCT}$
HIGH	$16/f_{OCT}$	$f_{OCT}/16$	$4/f_{OCT}$

*f_{OCT} in kHz

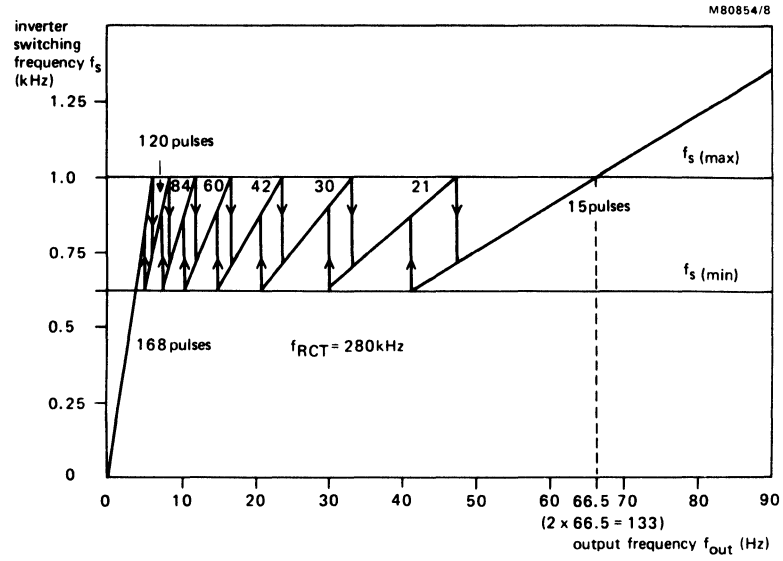


Fig.8 Inverter switching frequency against output frequency (full range)

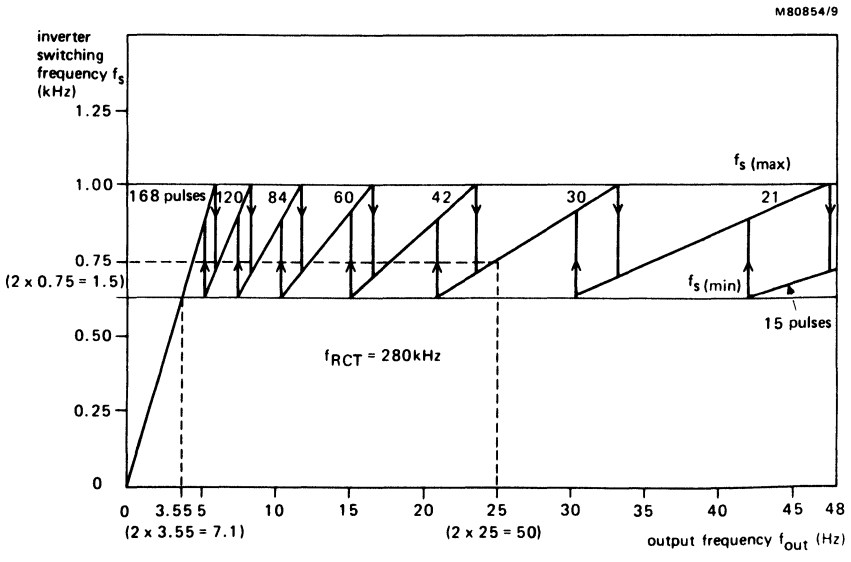


Fig.9 Inverter switching frequency against output frequency (expanded scale for low frequencies)

9

delay set by the K and OCT inputs, and is present irrespective of the L input state. The VAV signal has a frequency equal to the inverter switching frequency f_{out}, and a modulation given by $6f_{out}$.

VAV is useful for closed-loop control of f_{VCT} to obtain some improvement in the linearity of voltage with frequency when the frequency ratio $f_{I\,CT}/f_{VCT}$ is greater than 0.5. The variation of VAV with frequency ratio is shown in Fig.10.

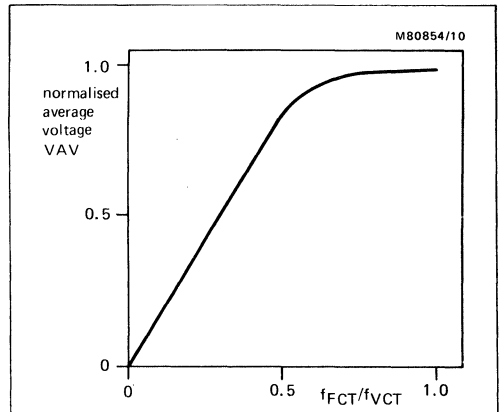


Fig.10 VAV against f_{FCT}/f_{VCT}

Inverter switching output CSP

The output CSP is a pulse train at twice the inverter switching frequency. The falling edge of each pulse occurs at the point of zero modulation of the main outputs. When $f_{I\,CT}/f_{VCT}$ exceeds 0.5, CSP represents the theoretical inverter frequency; however, because of the merging of pulses from over-modulation, the actual switching frequency will be less. As with the VAV output, CSP is unaffected by the state of input L.

APPLICATION ADVICE

Proper operation of the IC requires limitations on the frequency ratio $f_{I\,CT}/f_{VCT}$, and on the range of $f_{I\,CT}$. These limitations have already been described under the discussion of the clock inputs VCT and RCT. Three additional conditions for ensuring satisfactory performance are now considered.

Start/stop input L

If input L is used in the thyristor mode, care must be taken to ensure that the switching edges are clean. For example, if some switch bounce occurs when switching to the LOW condition, then this can result in one or more of the M1 outputs being on instead of all the M2 outputs. A simple circuit to overcome this problem, together with the corresponding output waveform, is shown in Fig.11.

Switch-on conditions

For safe operation an initial switch-on period is required, during which the thyristor trigger circuits or transistor drive circuits are inhibited, and the correct clock and input conditions are established. During the first half of the switch-on period, the internal IC circuit should be reset. This can be done by either applying a HIGH signal to input A, or running the FCT clock for at least 3360 FCT pulses.

The required input states on all inputs must be established during the second half of this period. If FCT is to

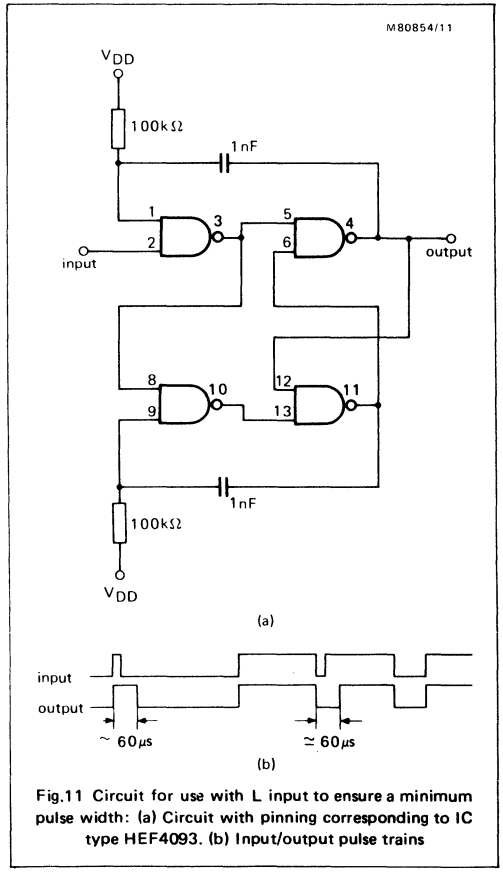


Fig.11 Circuit for use with L input to ensure a minimum pulse width: (a) Circuit with pinning corresponding to IC type HEF4093. (b) Input/output pulse trains

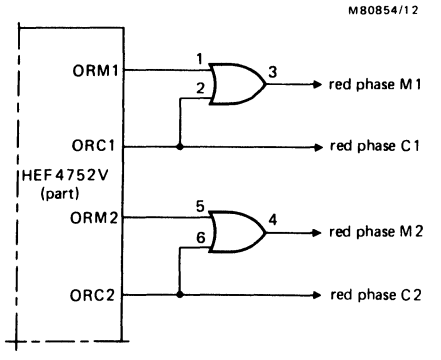


Fig.12 Circuit for producing a full length trigger pulse under minimum pulse width conditions. Pinning corresponds to IC type HEF4071

be started from zero during normal operation, it is advisable to run the FCT clock at about 0.04 f_{RCT} during the second half of the switch-on period for at least 3360 pulses, otherwise the output circuits will be set at 15 pulses per cycle for the first few pulses, instead of 168, which could result in damage to the inverter.

Minimum pulse width

From Figs.6 and 7 it can be seen that once the control signal (waveforms 6e and 7e) produces a pulse width equal to, or less than, the interlock delay, the appropriate main output is reduced to a narrow pulse. The width of this pulse is $1/f_{OCT}$ and it is always followed by a full-width commutation pulse. In the transistor mode, this narrow pulse will normally have little or no effect on the inverter. However, in the thyristor mode the correct triggering of the main thyristor may require the connection of the commutation pulse to the main pulse via an OR-function. A circuit to achieve this result is shown in Fig.12.

The next article in this series will describe the analogue control section.

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Analog Control System for AC Motor with PWM Variable Speed Drive

AN137

W.B. ROSINK

This article describes an analogue control system which has been developed for use with our Pulse-Width Modulation (PWM) variable speed drive for three-phase a.c. motors. The article is the fourth in a series, previous articles being listed in Refs.1, 2, and 3. Reference 1 gives a general introduction to our PWM drive system, Ref.2 describes a specially developed inverter circuit, and Ref.3 describes an LSI circuit, type HEF4752V, developed specifically for signal generation in PWM drive systems.

The three-phase a.c. motor is remarkable for its simplicity of construction. This simplicity is in contrast to the comparatively complex requirements of a control system for an a.c. motor operating under variable speed and load conditions. The features needed by such a system will be determined by three factors: the inherent operating characteristics common to all a.c. motors, the method of speed variation employed, and the particular control requirements needed by the motor user. The control system described in this article has been designed to meet the requirements of the majority of users, but without being excessively complex. Alternative system designs of greater or lesser refinement are of course possible. The detailed description of the design and operation of the analogue control system is preceded by a review of the operating characteristics of a.c. motors, and the relevant features of our PWM variable speed drive.

THE A.C. MOTOR

The three-phase a.c. induction (asynchronous) motor consists of a wound stator connected to a three-phase a.c. supply, and a squirrel-cage rotor with no external connections. The stator currents produce a rotating magnetic flux, with a speed of rotation (synchronous speed) n_s given by:

$$n_s = \frac{f_s}{p} \times 60 \text{ rev/min}, \qquad (1)$$

where f_s is the stator supply frequency, and p is the number of pole-pairs in the stator. The rotating stator field induces an e.m.f. in the rotor conductors, and since the conductors are short-circuited, this results in rotor currents. Motor torque is produced by the interaction of the stator flux and the rotor currents, the torque contribution T of each rotor conductor being proportional to the product of the in-phase component of the rotor current and the air-gap flux; that is:

$$T \propto I_r \cos\theta_r \phi, \qquad (2)$$

where I_r is the rotor current, $\cos\theta_r$ the rotor power factor, and ϕ the air-gap flux per pole.

In order that rotor currents may be induced, the rotor speed n_r must be different from the synchronous speed. This speed difference is called slip, and is usually expressed as a fraction of the synchronous speed; that is:

$$s = \frac{n_s - n_r}{n_s}. \qquad (3)$$

The speed of the rotor relative to the stator field is $(n_s - n_r)$, and the frequency of the rotor e.m.f., f_r, is therefore given by:

$$f_r = \left(\frac{n_s - n_r}{n_s}\right) f_s,$$

or:

$$f_r = sf_s. \qquad (4)$$

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For constant flux, the magnitude of the rotor e.m.f., and therefore I_r, is proportional to s, so that as load is added to an induction motor, additional torque is produced by an increase in fractional slip. Since the rotor impedance is low, a small increase in slip produces a large increase in rotor current, the full-load slip being typically 3 to 5%. When rotor current flows, there is a corresponding increase in stator current.

Provided that the fractional slip is small, torque will increase with increasing slip. However, as the slip increases, the frequency of the rotor e.m.f. will increase (see Eq.4) so that rotor reactance will rise, together with the phase angle θ_r. With increasing slip, the motor torque therefore reaches a maximum and then falls. This maximum value is called the pull-out torque, and the motor will stall if this peak value is exceeded. Controlled operation of the speed drive therefore requires that slip variations do not exceed the limit defined by the pull-out torque.

The variation of torque with fractional slip for a typical squirrel-cage motor of the standard type is shown in Fig.1. This curve has been extended into the generator mode, where the rotor speed is greater than the synchronous speed. In this region, the motor converts mechanical energy into electrical energy which is partially absorbed by the power converter system, or returned to the supply. The generator mode occurs when the load drives the motor at super-synchronous speeds, as in crane drives. It can also occur in a variable-frequency system when the supply frequency is rapidly reduced.

Under direct-on-line starting conditions, the fractional slip is unity, so that the rotor frequency and reactance are both high. This implies a high motor current at a low power factor so that the starting torque is low (see Eq.2). By increasing the rotor resistance, the power factor can be increased and starting torque improved (see Fig.1). However, under running conditions the motor will then operate at reduced efficiency due to high I^2R losses. In practice, rotor design is a compromise between the needs of starting performance and efficiency, and while there are ways of reducing this conflict, such as the double-squirrel-cage design, starting performance remains a potential weakness of the induction motor when operated under constant-frequency conditions.

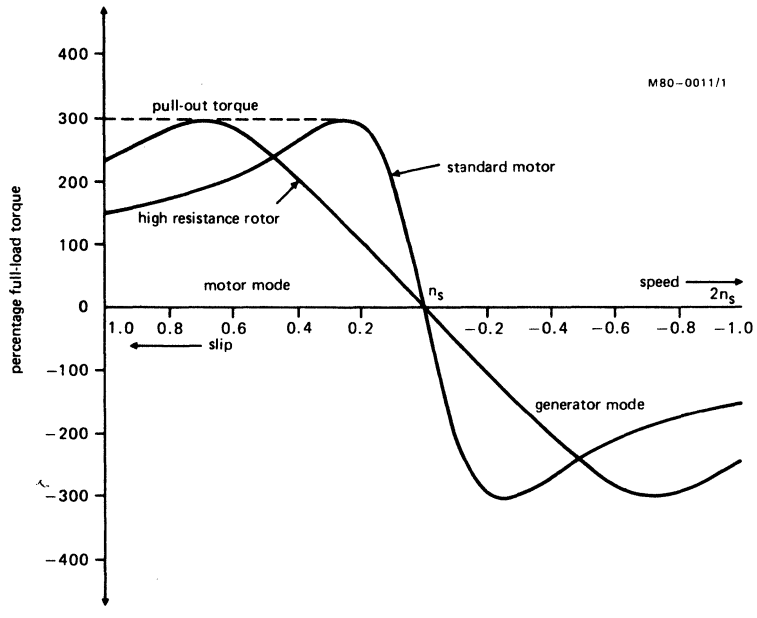

Fig.1 Variation of torque with slip for a standard squirrel-cage motor, and a motor with a high resistance rotor

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PWM DRIVE FOR A.C. MOTORS

From Eq.1 it can be seen that varying the input frequency to the stator will result in a corresponding change in the synchronous speed. Since under normal operating conditions the rotor speed is only a few percent less than the synchronous speed, this provides a method of continuously changing the motor speed. To maintain constant full-load torque, the air-gap flux must be held constant, and this requires an applied voltage which must be varied in linear proportion to the input frequency. The speed/torque characteristics for an induction motor operating under constant flux and variable frequency are shown in Fig.2.

Our PWM drive system (see Ref.1) is designed to provide this type of variable speed constant-torque operation. A block diagram of the system is shown in Fig.3. The three-phase mains input is connected to the bridge rectifier via an interference filter. The d.c. voltage V_{Cb} is smoothed by a capacitor input filter (a choke input filter may be used for higher powers), and then applied to the inverter. The outputs from the three phases of the inverter consist of sinewave-weighted pulse-width-modulated waveforms at the selected carrier frequency; this gives sinusoidal motor currents with low harmonic content. The form of the inverter output waveforms is determined by the timing of the trigger pulses, generated by the PWM IC, HEF4752V. This IC forms the central feature of the PWM drive system, and the analogue control section effects changes in the motor performance solely by varying the inputs to the IC.

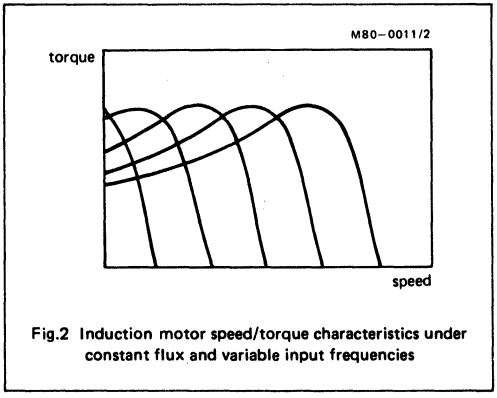

Fig.2 Induction motor speed/torque characteristics under constant flux and variable input frequencies

The operation of the IC is defined by a digital signal CW, which controls the direction of motor rotation, and four clock inputs FCT, VCT, RCT, and OCT. The four clock inputs have the following functions.

- FCT (Frequency Clock Trigger). This determines the stator frequency, thereby controlling the motor speed.
- VCT (Voltage Clock Trigger). This determines the stator frequency/voltage ratio.
- RCT (Reference Clock Trigger). This sets the inverter maximum switching frequency.
- OCT (Output Clock Trigger). This sets the minimum pulse-width allowable.

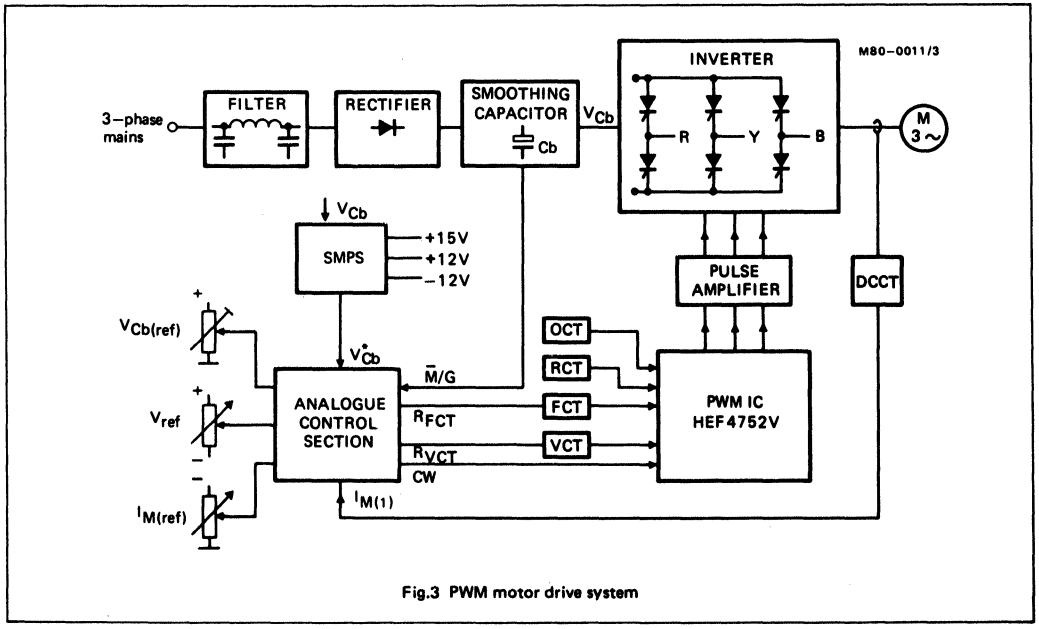

Fig.3 PWM motor drive system

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The clock inputs of FCT and VCT are determined by wide-frequency-range voltage-controlled oscillators (VCOs), while the clock inputs of RCT and OCT are fixed for a given application, and can be controlled by VCOs or fixed oscillators.

The analogue control section produces three outputs: the digital signal CW, and voltage reference signals R_{FCT} and R_{VCT} for the VCOs of FCT and VCT. There are six inputs to the analogue control section: three are feedback signals, and three are potentiometer settings. The three feedback signals are: a voltage V^*_{Cb} which is proportional to the voltage across the smoothing capacitor, the motor current signal $I_{M(1)}$, sensed by a D.C. Current Transformer (DCCT) in the motor current lines, and a digital signal $\overline{M}/G$, derived from the power rectifier/filter circuit, indicating whether the motor is in the motor mode or generator mode. The potentiometer settings V_{ref}, $I_{M(ref)}$, and $V_{Cb(ref)}$ respectively set the motor speed, limit motor current in the motor mode, and limit the d.c. voltage in the generator mode. A fuller explanation of the function of the various input/output signals, is given in the next section.

ANALOGUE CONTROL SECTION

The analogue control section is designed to ensure safe and effective speed control under variable load and variable speed conditions. It provides the following facilities.

- Bidirectional control of motor speed from zero up to twice nominal speed, with fast response.
- Adjustment of maximum motor current up to about 140% of the nominal value.
- Adjustment of acceleration and deceleration time during motor speed variation.
- Limitation of motor current and voltage to protect the inverter, and to keep the motor operating within the specified slip range.
- Adjustable slip correction to improve speed regulation with load variation.
- Adjustable IR compensation to increase the starting torque.
- Protection circuits to ensure safe switch-on/switch-off performance.

The control section can be subdivided into four separate, but interrelated, circuits: the start/stop circuit, the speed reference circuit, the current/voltage control circuit, and the IR-compensation circuit. Each of these four circuits will now be considered in turn.

Start/stop circuit

Strictly speaking, the start/stop circuit is peripheral to the analogue control section represented as a block in Fig.3. However, it provides a number of important functions essential to the safe operation of the drive system, and a brief description of its operation is therefore given. A block diagram showing the essential features of the start/stop circuit, and its position in the total drive system is shown in Fig.4.

The circuit protects the system against adverse start/stop conditions, and provides the reset signal for the PWM IC. After switch-on, the three-phase rectifier

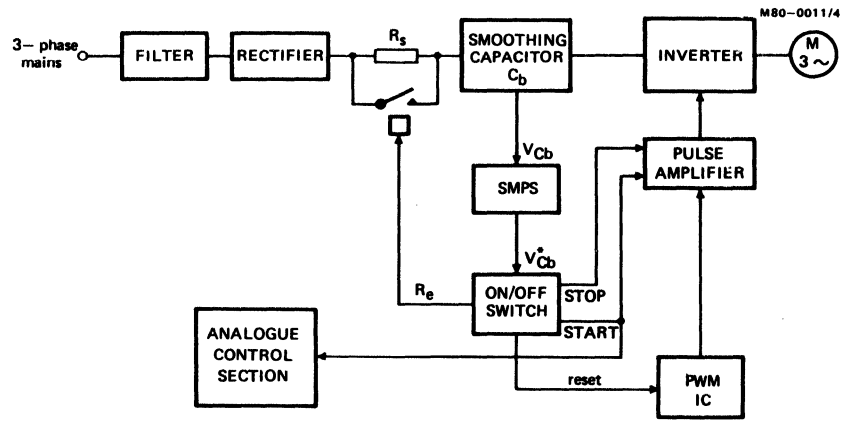

Fig.4 Start/stop circuit

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charges the smoothing capacitor C_b via a limiting resistor R_s, protecting the rectifier diodes against inrush currents. When V^*_{Cb} exceeds 80% of its nominal value, the signal R_e closes the relay which short-circuits R_s. After a delay, determined by the action of a ramp generator, the PWM IC is reset. With the IC reset, the START signal goes HIGH, and the start procedure is complete.

When the mains supplies are disconnected, the capacitor C_b starts to discharge. When V^*_{Cb} is at 80% of its nominal value, the STOP signal goes HIGH, inhibiting the inverter action. Below this level, the commutation currents of the inverter are too low for safe commutation of the motor currents. The STOP signal remains HIGH until C_b has discharged. Figure 5 shows the various signals associated with the start/stop procedure.

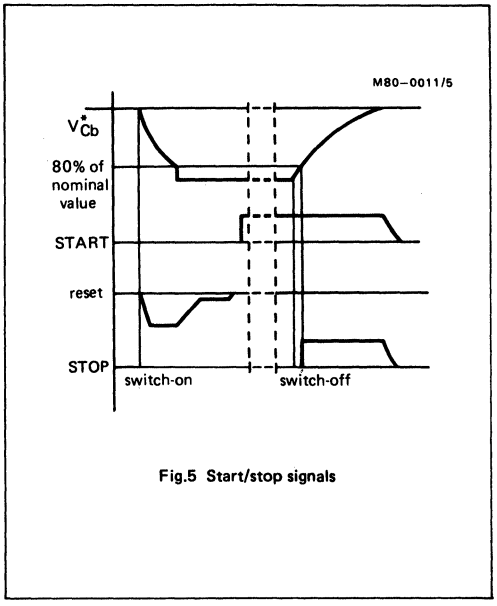

Fig.5 Start/stop signals

Speed reference circuit

The rate at which the speed of a motor can be changed is limited by the inertia of motor and load, and the available motor torque. As the stator frequency is altered, there is an inevitable lag in the response of the rotor, resulting in an increase in slip. Unless some limitation is placed on

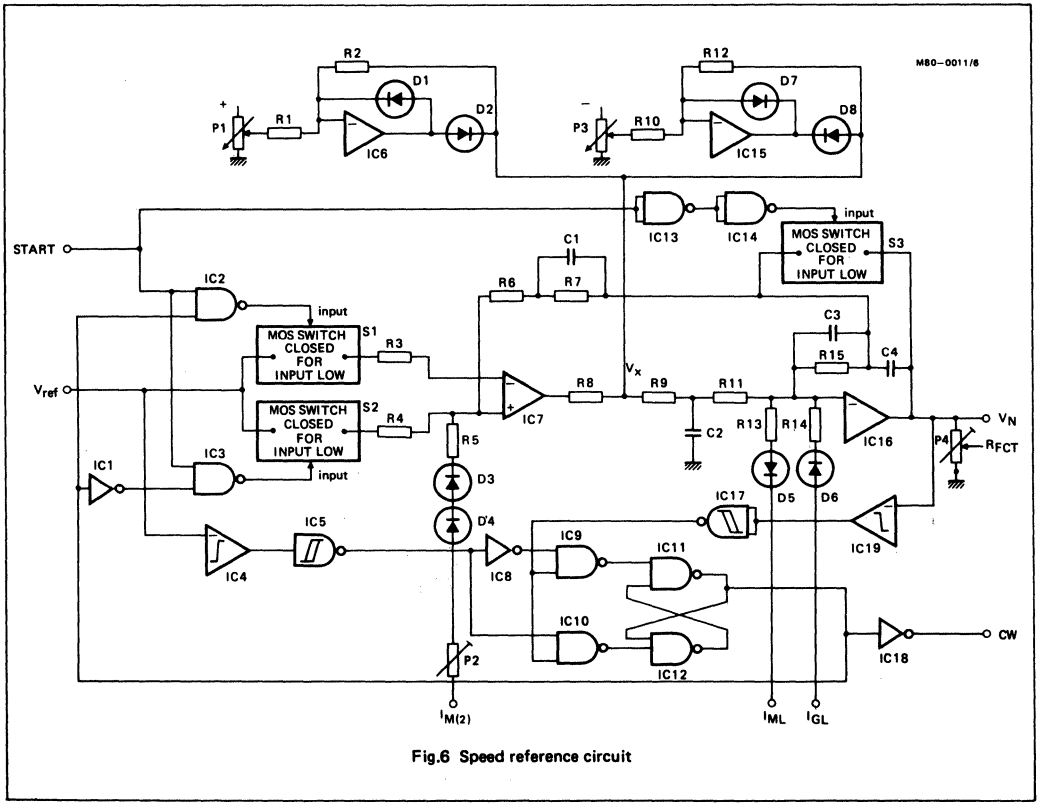

Fig.6 Speed reference circuit

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the rate at which the stator frequency can change, the increase in slip can result in the pull-out torque being exceeded and the motor stalling. The speed reference circuit gives bidirectional speed variation together with control over the maximum rates of increase (acceleration control), and decrease (braking control) in the stator frequency.

A simplified circuit diagram is shown at Fig.6. The motor speed is determined by the potentiometer setting V_{ref}. This can be changed from −10 V to +10 V, changing the motor speed from maximum clockwise to maximum counter-clockwise. The speed signal output V_N is derived from V_{ref} via a comparator IC_7, and an integrator IC_{16} to give $V_N = -k|V_{ref}|$. A stepwise variation of V_{ref} results in a linear increase or decrease of the output signal V_N. The rate of variation of V_N can be adjusted via the accelerate/decelerate limiting potentiometers P_1 and P_3. The output V_N is grounded as long as the START input is low. The voltage output R_{FCT}, proportional to V_N, controls the frequency of the FCT clock, which in turn sets the inverter output frequency and hence determines the motor speed. The third output CW, controls the direction of rotation of the motor. Inputs I_{ML} and I_{GL} protect the inverter against overload conditions, while input $I_{M(2)}$ gives improved speed regulation for large load variations. The action of these three inputs is considered in detail under the discussion of the current and voltage control circuit.

Circuit operation

The influence of changes in input signals V_{ref} and START, on the output signals V_N and CW is shown in Fig.7. The features of the circuit operation which give rise to the results of Fig.7 are now considered.

At t_0 START is LOW, V_{ref} is positive, and CW is HIGH. The outputs of IC_2 and IC_3 will therefore be HIGH, so that MOS switches S_1 and S_2 will be open and no reference signal is supplied to the comparator IC_7. The output of IC_{14} will be low, so that MOS switch S_3 is closed and capacitor C_4 short-circuited. The speed output signal V_N is then zero.

At t_1 START now goes HIGH, together with the output of IC_{14}, so that S_3 is opened. The output of IC_3 goes LOW, S_2 is closed, and V_{ref} is supplied to the non-inverting input of comparator IC_7. The output of IC_7 is positive and the integrator IC_{16} ramps to a negative value. The slope of the integrator output voltage is determined by voltage V_x, resistors R_9 and R_{11}, and capacitor C_4; that is:

$$\frac{dV}{dt} = -\frac{V_x}{C_4(R_9 + R_{11})} \qquad (5)$$

As described below, the value of V_x can be limited by potentiometers P_1 and P_3 to give maximum rates of deceleration and acceleration respectively.

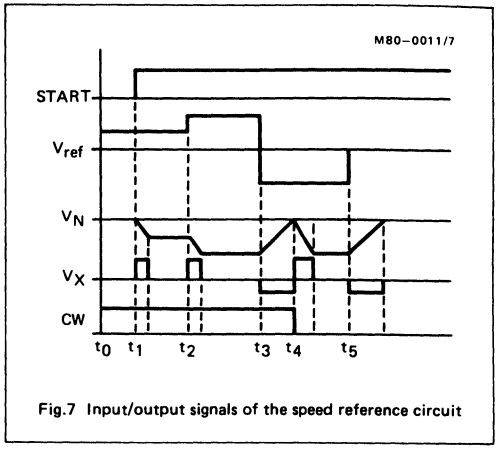

Fig.7 Input/output signals of the speed reference circuit

At t_2, V_{ref} is increased and V_N ramps to a more negative value.

At t_3 the input voltage V_{ref} is now reversed to a negative value, the output of IC_7 goes negative, voltage V_x is negative, and the integrator IC_{16} begins to ramp up. This implies a decelerating motor. The change in sign of V_{ref} causes the reference polarity detector IC_4 to switch the output of IC_5 from HIGH to LOW.

At t_4 the output of IC_{16} now reaches a slightly positive value, and the reference polarity detector IC_{19} switches the output of IC_{17} from LOW to HIGH. The flip-flop, IC_{11} and IC_{12}, now set via IC_9, and the output of IC_{11} goes HIGH so that CW goes LOW. With the CW signal LOW, the output of IC_3 goes HIGH and S_2 is opened, and the output of IC_2 goes LOW and S_1 is closed. This transfers the V_{ref} signal from the non-inverting to the inverting input of IC_7. This action ensures that the output of IC_7 is positive whenever the motor is accelerating, irrespective of the direction of rotation. The output V_N now ramps down to a value determined by the setting of V_{ref} at t_3.

At t_5, V_{ref} is set at zero, the output of IC_7 goes negative, and V_N ramps up to zero, bringing the motor to rest.

Limitation of the rate of speed variation

The maximum rate of speed variation is limited by controlling the maximum positive and negative values of V_x. The maximum positive value $V_{x(max)}$ is determined by the setting of potentiometer P_3 and the inverting operational amplifier IC_{15}; that is:

$$V_{x(max)} = -V_{p3}\,\frac{R_{12}}{R_{10}}, \qquad (6)$$

where V_{p3} is the voltage set by potentiometer P_3. Similarly, the maximum negative value of V_x is determined

by potentiometer P_1 and the inverting operational amplifier IC_6.

Suppose that the motor is accelerating; V_x will be positive. If V_x exceeds $V_{x(max)}$, then diode D_8 will conduct clamping V_x to $V_{x(max)}$. If V_x exceeds the preset maximum negative value while decelerating, then diode D_2 will conduct, clamping V_x to the maximum negative value. In this way independent control of acceleration and deceleration is obtained.

Current and voltage control circuit

The purpose of this circuit is to provide the I_{ML}, I_{GL}, and $I_{M(2)}$ signals for the speed reference circuit. As explained above, I_{ML} and I_{GL} limit the motor current and applied voltage to below the maximum capacity of the inverter, while $I_{M(2)}$ provides a degree of speed stabilisation under large loads. The protection of the inverter is considered first.

Inverter protection

In considering the problem of inverter protection, it is necessary to examine the requirements of the motor and generator modes separately.

In the *motor* mode, high motor currents will result if the required motor torque is too high, or the rate of acceleration is excessive. Both situations will give rise to high positive slip with correspondingly high currents. Motor current is controlled by *reducing* the synchronous speed so that the slip is also reduced.

In the *generator* mode, high motor currents can arise under braking conditions, or when the load drives the motor. In both cases, the motor speed can exceed the synchronous speed, giving negative slip. If this negative slip value is high, motor current will become excessive. By *increasing* the synchronous speed the slip is reduced and the motor current brought under control. There is a further complication in the generator mode, since the design of the control section does not allow for the return of energy to the supply; instead, any energy generated by the motor is initially stored in the smoothing capacitor. Without some limitation on the rate at which energy is fed to this capacitor the applied voltage could exceed the voltage rating of the inverter. To ensure that this voltage does not exceed a preset maximum value, the circuit reduces the synchronous speed at a slow enough rate so that power generation is just compensated by the power losses of the inverter and motor. In practice, limiting braking torque in this way still provides a fast braking action, even with large load inertia.

A circuit diagram is shown at Fig.8. The circuit has three input signals $I_{M(1)}$, $\overline{M}/G$ and V^*_{Cb}. The output signals are I_{ML}, I_{GL} and $I_{M(2)}$. Signal I_{ML} is the current limiting signal in the motor mode, while I_{GL} is the current limiting signal in the generator mode.

To reduce motor current in the motor mode, I_{ML} is driven negative. Diode D_5 of Fig.6 then conducts, so that the negative value of V_N is reduced, thus the synchronous speed falls and the slip is reduced. For excessive motor current conditions in the generator mode, I_{GL} is driven positive. Diode D_6 of Fig.6 then conducts, the negative value of V_N is increased, the synchronous speed rises, and the slip is again reduced.

The switch between I_{ML} and I_{GL} is controlled by the input $\overline{M}/G$. Signal $\overline{M}/G$ is LOW for the motor mode and HIGH for the generator mode. With $\overline{M}/G$ set LOW, the output of IC_3 (Fig.8) is HIGH. This clamps the output of IC_7 (Fig.8) negative, so that diode D_6 (Fig.6) inhibits the I_{GL} signal. With $\overline{M}/G$ HIGH, the output of IC_6 (Fig.8) is HIGH, keeping I_{ML} at a high level so that diode D_5 (Fig.6) inhibits the I_{ML} signal.

The measured motor current signal $I_{M(1)}$, sensed by the DCCT in the motor current lines, is amplified and filtered by IC_1 (Fig.8) and smoothed by capacitor C_2 to suppress the sampling ripple frequency of the measuring circuit. The output of IC_1, signal $I_{M(2)}$, is then supplied to the current limiting control amplifier IC_5, where it is compared with the current reference signal for the motor mode $I_{M(ref)}$. This circuit works as a 3-term error amplifier with proportional-integral-derivative control action. The proportional gain of the circuit is given by R_{18}/R_{11}. The crossover frequencies for the differential action are determined by the values of R_{11}, R_{12}, and C_7, while the crossover frequencies for the integral action are given by C_8, R_{17}, and R_{18}. The use of the differential network gives an optimal response for the current-limiting signal and prevents overshoot. By varying the setting of potentiometer $I_{M(ref)}$, the maximum motor current for the motor mode can be adjusted from 70% up to 140% of the nominal motor current. Current limiting below 70% can cause instabilities, because the motor current cannot be decreased below the magnetising current.

Control of motor current in the generator mode is achieved by supplying the $I_{M(2)}$ signal to the second error amplifier IC_2, where it is compared with the pre-adjusted reference signal $I_{G(ref)}$. As soon as $I_{M(2)}$ exceeds $I_{G(ref)}$, which sets the current limit level in the generating mode, the output of IC_2 goes negative. This signal is fed to a unity-gain inverting amplifier, IC_7, and then the resulting positive signal I_{GL}, is supplied to the speed reference circuit where it increases the synchronous speed, under current limit conditions in the generating mode.

To limit the applied voltage in the generator mode, the negative V^*_{Cb} signal, which is proportional to the voltage across the smoothing capacitor, is supplied to a third error amplifier IC_4, and compared with the adjustable maximum reference value $V_{Cb(ref)}$. For V^*_{Cb}

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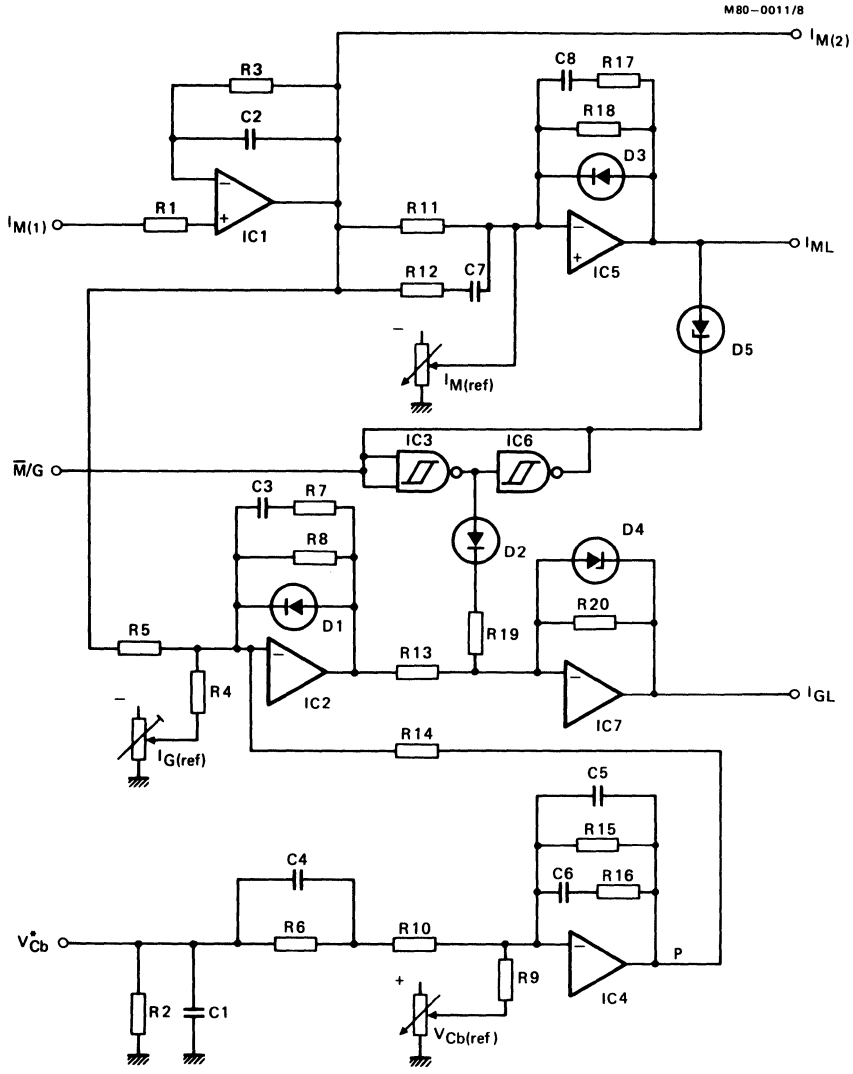

Fig.8 Current and voltage control circuit

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greater than $V_{Cb(ref)}$ the output signal P of IC_4 goes positive. This signal is supplied to the input of IC_2, where it effectively reduces the current reference level for the generator mode until the regenerative power is just equal to the power losses in the inverter and motor. The response of the current and voltage control circuit under variable speed conditions is shown in Fig.9. The lower trace of Fig.9b shows the change in synchronous speed following a stepwise variation in the V_{ref} input of the speed reference circuit. It shows a fast speed response, with an acceleration time of 0.8 seconds, and a braking time of one second. The motor current is limited to a peak value of 8 A on acceleration, and to a peak value of 7 A on braking (lower trace Fig.9a). The maximum voltage on braking is 700 V (upper trace Fig.9a).

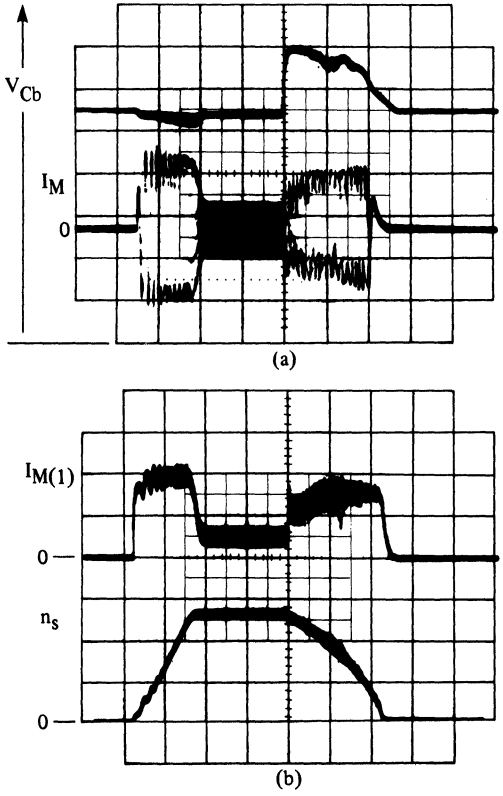

Fig.9 Current and voltage waveforms during speed change conditions
(a) upper trace – supply voltage V_{Cb} (100 V/division)
lower trace – motor current I_M (5 A/division)
(b) upper trace – DCCT output $I_{M(1)}$ (corresponds to I_m of approximately 3.5 A/division)
lower trace – synchronous speed (approximately 700 rev/min per division)
time scale: 0.5 s/division

Slip correction

Under increasing motor torque, the slip will increase, so that for a fixed synchronous speed the motor speed falls. The output of IC_1, signal $I_{M(2)}$, which is proportional to I_M, may be used to give improved speed regulation under variable load conditions.

The $I_{M(2)}$ signal is supplied to the non-inverting input of IC_7 (Fig.6) where its effect is to make V_N more negative, thus giving a higher synchronous speed and in turn a higher motor speed. The degree of slip correction can be varied with potentiometer P_2 (Fig.6).

The effectiveness of this technique of speed regulation is reduced for low-power standard asynchronous motors, where the magnetising current is a significant proportion of the load current. However, even with motors of this type, the speed deviation from the no-load to full-load condition can be reduced by 50 to 80%.

IR – compensation

With a variable frequency drive system, the motor is started at a low input frequency and then brought-up to the desired operating speed by a steady increase in frequency, and a motor voltage proportional to this frequency. In this way, the high motor currents, and low power factor associated with starting a fixed frequency system are avoided. However, the low input frequency will also result in a low applied motor voltage.

At low frequencies the voltage drop across the stator resistance is, therefore, relatively large when compared with the applied voltage. These high IR losses will result in a low air-gap flux, and consequently a low starting torque. If a high starting torque is required, it can be achieved by increasing the applied voltage at low frequencies.

The value of the applied voltage at a given input frequency is determined by the VCT clock input of the IC. Reducing the frequency of this clock will increase the applied voltage for a given input frequency, while increasing the clock frequency has the opposite effect. A full discussion of the relationship between the VCT clock and input frequency is given in Ref.3. The frequency of the VCT clock is determined by its voltage reference signal R_{VCT}, so that IR-compensation requires the modification of R_{VCT} for low input frequencies.

A circuit to obtain this modification is shown at Fig.10. The circuit has a single input, the negative speed signal V_N derived from the speed reference circuit, and a single output R_{VCT}. For values of V_N which are less negative than the value given by:

$$V_N = V_{p1} \frac{R_1}{R_3}, \qquad (7)$$

where V_{p1} is the voltage set by potentiometer P_1, the circuit decreases the negative value of R_{VCT}, while for

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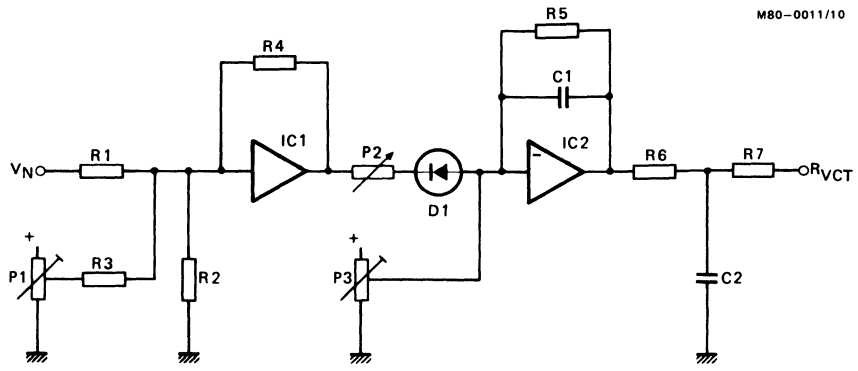

Fig.10 IR-compensation circuit

values of V_N which are more negative than the value defined by Eq.7, the output signal R_{VCT} is adjusted by potentiometer P_3 to obtain the nominal rated motor voltage. Equation 7 therefore defines the region of IR-compensation. For V_N as given by Eq.7, the output of IC_1 is zero, while for less negative values the output of IC_1 becomes increasingly negative, driving the output of IC_2 and thus R_{VCT} less negative. For more negative values, the output of IC_1 is blocked by diode D_1. Within the region of IR-compensation, the influence of V_N on R_{VCT} can be adjusted with potentiometer P_2. Figure 11 shows the effect of IR-compensation on the average applied voltage V_{AV}, and illustrates the roles of the three potentiometers P_1, P_2, and P_3.

The next article in this series will describe the D.C. Current Transformer (DCCT), which is used to sense the motor current.

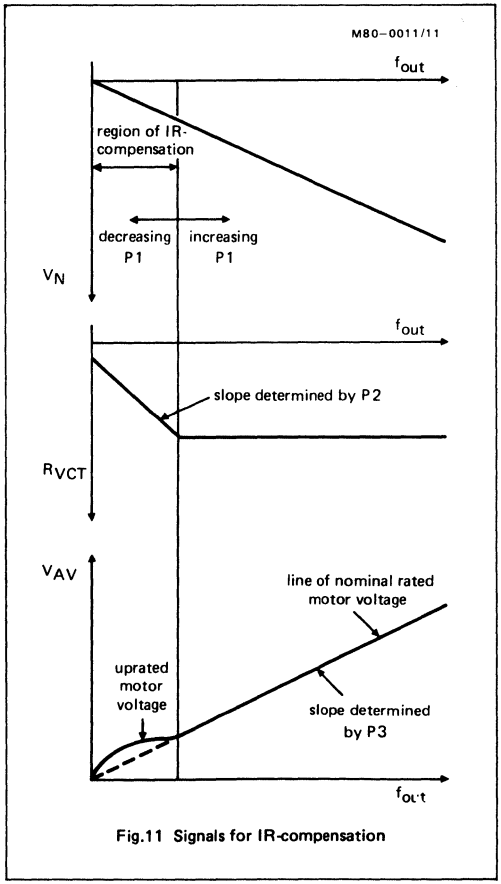

Fig.11 Signals for IR-compensation

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3. STARR, B.G. and van LOON, J.C.F., 'LSI circuit for AC motor speed control', Electronic Components and Applications Vol.2, No.4, August 1980, pp.219 to 229.

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Four Standard Color Decoder with Picture Improvement AN155

Author: Klaus Juhnke

The decoder concept presented here comprises a four standard decoder and a video combination. The concept can also be extended by means of a picture improvement circuit.

A brief overview will first be given to clarify this arrangement. Figure 1 shows the block diagram of a complete color decoder from the CVBS interface up to the picture tube. There are switchable filters for separation of the luminance and chrominance signals from one another. Only one IC is necessary for the demodulation of four color standards.

The output signals are the standard-independent color difference signals (B-Y) and (R-Y), i.e. U and V. The baseband signals (i.e. color difference signals and luminance signal Y) can either be directly supplied to the video combination or they can be supplied via a signal processor IC as shown here.

The video combination comprises all functions for advanced video signal processing. The RGB output signals of the IC can be fed to the video final stages directly.

The interface selected in this decoder concept, with the baseband signals as input signals of the video combination, also permits new circuit concepts to be introduced, e.g. the delay line which is required for PAL and SECAM can be realized with CCD lines. Picture improvement circuits with picture memories can also be added.

The CTI IC which is incorporated in Figure 1 was likewise developed for this interface. In this circuit two functions are integrated: a transient improvement for a better picture, and a Y delay line in gyrator technique to replace the previously required wound line.

In the past, multi-standard color decoders have been built up with a number of integrated circuits. Parallel working concepts are known, and also transcoder concepts specially for PAL and SECAM. The decoders of the various standards require circuit blocks of the same type; this applies in particular to the quadrature amplitude modulation standards (QAM standards) PAL and NTSC, but to a large extent also for the FM standard SECAM. An obvious approach for the integration of a multi-standard decoder on one chip is therefore to make use of as many circuit blocks as possible in common for the different standards, in order to minimize the components and thus also the crystal area required. Under the condition of automatic standard identification, as is already the state of the art for present MSD concepts, multiple utilization of the circuit blocks can only be realized if automatic standard identification is effected by *sequential standard scanning*. A system of this kind gives the great advantage that the entire decoder including the filters can be designed in the optimum way for the individual standards.

The MSD shown here as in the block diagram in Figure 2 works on this principle and is designed for 4 standards: PAL, SECAM, NTSC and a second (admittedly non-standard) NTSC with the PAL chrominance subcarrier frequency. This NTSC system has been introduced in the Near East due to American software and in Britain de facto.

The IC incorporates a digital control unit in I^2L technique, which switches the color decoder in the sequentially optimum way for the different standards. As long as there has been no identification of a color standard, the four possible standards are scanned sequentially in the order PAL, SECAM, NTSC M and NTSC 4.4MHz. The activation time for each of the standards is four vertical periods (80ms).

Investigations have shown that the time indicated in connection with suitable time constants for automatic chrominance control (ACC) and for standard identification gives a good compromise

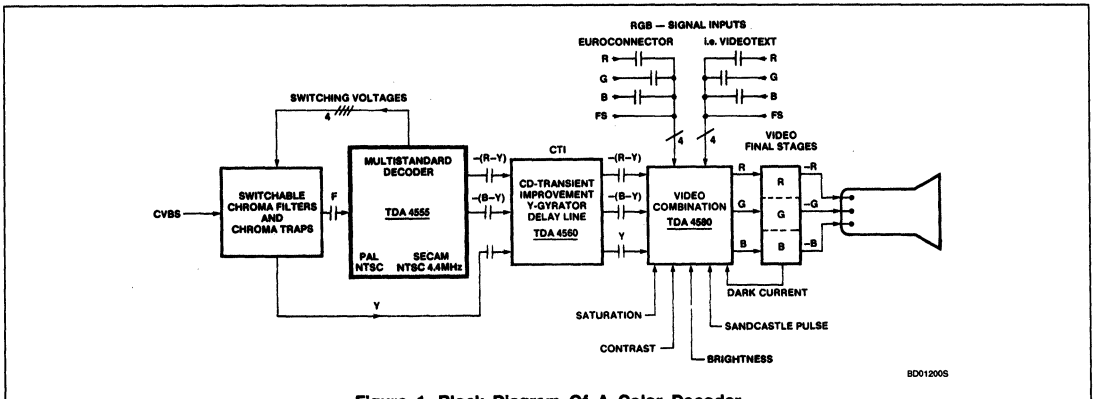

Figure 1. Block Diagram Of A Color Decoder

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between speed of "color on" switching and noise elimination.

Together with a "color on" switching delay circuit, which is likewise in digital technique and corresponds to the time of two vertical periods, "color on" switching is effected after 360ms in the worst case. The switching voltages output by the IC are also used for switching on/over the external chrominance signal filters and crystals.

The respective standard identification circuit checks whether the standard being scanned is present. If the standard is not identified in 80ms, the next standard is scanned. Thus the search is carried out continuously when there is a monochrome signal. If a color standard is detected by the identification circuit, the two color difference signals are supplied to the outputs after the "color on" switching delay. In addition, the switching voltage supplied (which is 2.5V for the search, and is used for switching on the chrominance signal filters and also the crystals) is increased to 6V, so that a chrominance subcarrier trap in the luminance channel can also be switched on with a suitable circuit.

A standard scanning start delay with a time of two vertical periods (40ms) is also incorporated, so that in the event of disturbances such as transient failure of the chrominance signal e.g. due to fading, there is no immediate start of a new search with corresponding lengthening of the color switch-off time.

The pulses for scanning control and all other necessary pulses are derived from the sandcastle pulse.

For extremely unfavorable signals there is also a manual "standard forced switch-on" provided. The MSD can be fixed to one of the four color standards by feeding in a switching voltage of $\geqslant 10V$, via the four switching voltage outputs. However the automatic color killer continues to operate.

The identification circuits make use of synchronous demodulators. For PAL and SECAM the H/2 components of the burst signals and of the f_0 frequencies on the back porch are evaluated, or also in the case of SECAM, evaluation is effected during the vertical blanking time.

In order to provide definite distinction between the NTSC color standard with PAL frequency and the PAL color standard, it is necessary to have two identification circuits working in parallel, one with and one without H/2 circuit. For this reason it is also necessary to have two pins for two identification capacitors. These identification signals are evaluated in a logic circuit in the standard control circuit.

The ACC works for all color standards. With QAM signals it controls for constant burst signal amplitude. With the FM signal SECAM, the entire signal is used for generation of the control voltage. Amplitude measurement is effected by in-phase synchronous demodulation. The controlled chrominance signal is supplied in the case of the PAL standard directly, and in the case of the NTSC standards, via a hue control circuit to the gated PLL circuit of the quartz oscillator.

The quartz oscillator oscillates at twice the frequency of the chrominance subcarrier, in order to obtain in the known manner the 90° out-of-phase reference carriers for the demodulators. The respective crystals for the standards oscillate in series resonance and are connected to the IC via external switching stages.

The hue control circuit is in operation for the NTSC standard. A phase shift of ±40° can be achieved with a DC control voltage. For the PAL and SECAM decoding it is necessary to have chrominance signals delayed by 64µs. The MSD is designed for a glass delay line, but can easily be adapted to color difference signal delay lines, e.g. in PCCD technique.

Demodulators with external LC reference circuits have been used for SECAM.

After the demodulators, the harmonics – especially the second – of the chrominance subcarrier frequencies in the demodulated color difference signals are filtered in each case with three integrated RC elements.

For the SECAM standard it is necessary to carry out color difference deemphasis and blanking for the two color difference signals after demodulation.

The color switch-off stages are directly before the outputs. The color difference outputs are low-resistance emitter followers with internal current sources. Apart from a chrominance input signal, the MSD with the TDA 4550 only requires the sandcastle pulse and of course the operating voltage in order to supply the negative baseband color difference signals.

The external circuitry required for the IC is minimal, and is included as periphery to the block diagram in Figure 3 with the exception of the standard-dependent filters.

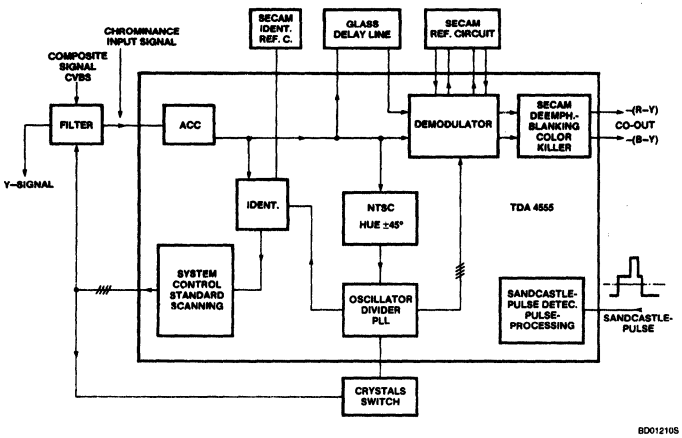

Figure 2. Block Diagram Of The Multistandard Color Decoder For PAL, SECAM, NTSC (3.5MHz) And NTSC (4.4MHz)

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The Multi-Standard Decoder IC has approximately 1500 components on an area of 14mm^2, and requires a 28-pin package.

The video combination IC incorporates all setting functions for color picture reproduction. A black current stabilizing circuit is provided. This saves three tuning operations and also automatically regulates operating point changes due to warming up after switch-on and to ageing.

RGB signal inputs are provided for signal supply from RGB sources via the peri-television plug, e.g. from cameras or from internal teletext decoders.

Figure 4 shows the block diagram of the input part of this IC. The two color difference signals −(R-Y) and −(B-Y) are fed in via capacitors and clamped in the input stages to reference values. After the saturation control stages, the −(G-Y) signal is generated with the (G-Y) matrix. These color difference signals together with the Y-signal which is likewise clamped in the input stage are converted to the R, G and B signals in the R, G and B matrix.

Switching stages, together with a switching matrix and a driver stage for the switching, permit the choice between the picture signals from the color difference and Y inputs or from the R, G, B inputs. When the R, G, B signals from the R, G, B inputs are selected, these are added to the black levels, which are simultaneously inserted. The switching times between blanking, insertion and changeover are about 50ns and are so small that there are no visible errors in the picture. If the RGB inputs are constantly connected, synchronization with the other signals is not necessary. The signals also pass through the contrast and brightness control stages. A peak beam current limitation can be effected via an input to a threshold level switching circuit. The threshold level circuit then reduces the contrast control voltage. Average beam current limitation is effected directly via the contrast control voltage, whereby under certain circumstances the brightness control is also reduced via an internal diode.

All the pulses required in the IC, and especially for the black current stabilization which will be explained below, are derived from the sandcastle pulse.

Signal processing is effected in parallel in three R, G, B channels and therefore the description and explanation will continue to be limited to the R channel.

Figure 5 shows the functional block diagram of the black current stabilizer. The R signal is blanked out and a measuring pulse is inserted for the black current measurement. A subsequent limiter stage prevents overdriving of the video final stages. A control stage is provided for white point adjustment, which can be effected by means of a DC setting voltage. There is an adding stage in which the voltage from the black current stabilization circuit is added to the R signal. The output stage of the IC can feed the video final stage directly. Its output voltage is supplied via a pnp measuring transistor to the cathode of the CRT. The collector circuit includes a measuring resistor at which voltage drops occur at the respective sequential measuring times; these are due on the one hand to any leakage currents which occur and on the other hand to dark current with leakage currents. These voltages are given to the IC. Following a buffer stage, the measurement voltage for the leakage currents is stored on the capacitor C_L. Switch S_L is only closed at the time when the signal is blanked and no signal current can flow. During the black level measurement time a reference voltage of 0.5V is subtracted from the voltage to be measured and then compared in a comparator circuit with the stored voltage for the leakage currents. Switch S_d is only closed during the black measurement time and closes the control loop. Capacitor C_d stores the control voltage.

A dark current of 10=mμA is not too small for reliable evaluation and not too big, so that if it is in the right time position no disturbing effects are visible on the screen.

Insertion of the measurement pulses and their evaluation is sequential; this means that from the measuring resistor through the measurement input and leakage current storage up to and including the comparator circuit these circuits only have to be realized once and are used for all three channels.

Figure 6 shows the time positions of the various measurement pulse insertions and evaluations. The measurement pulses are after the vertical flyback pulse and are thus above the upper picture edge in the overscan.

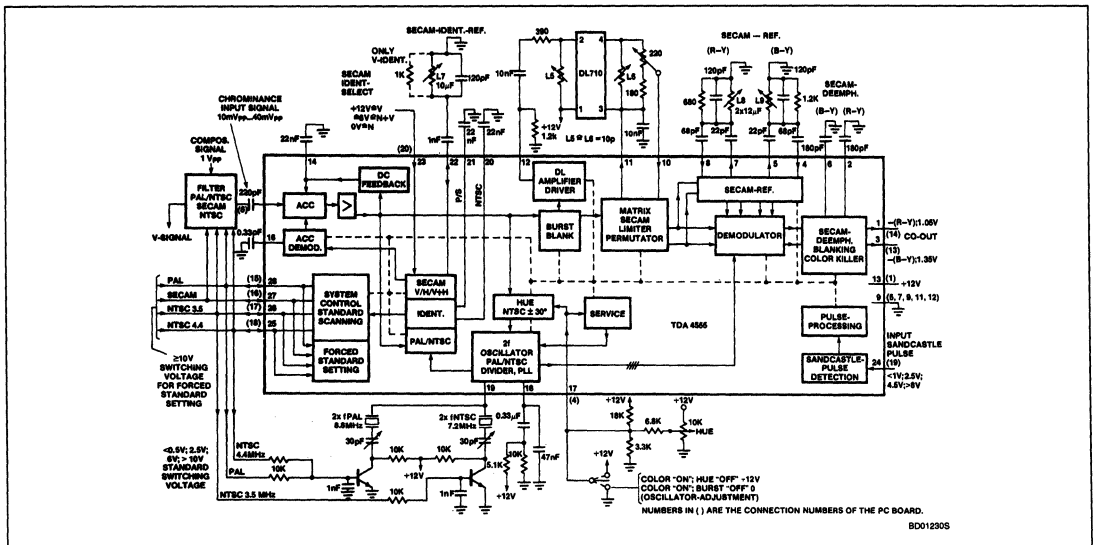

Figure 3. Multistandard Color Decoder For PAL, SECAM, NTSC (3.5MHz) And NTSC (4.4MHz)

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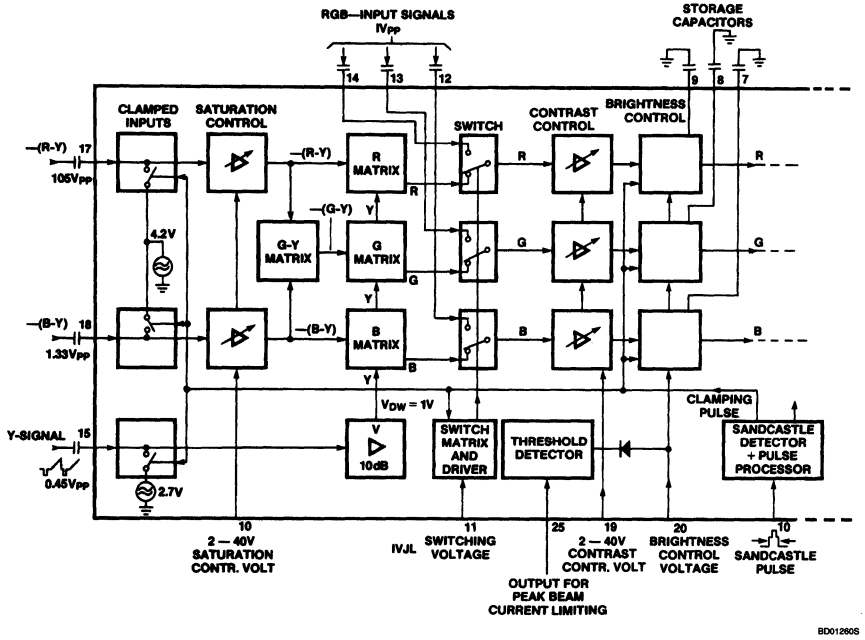

Figure 4. Front Part Of The Video Combination TDA3505

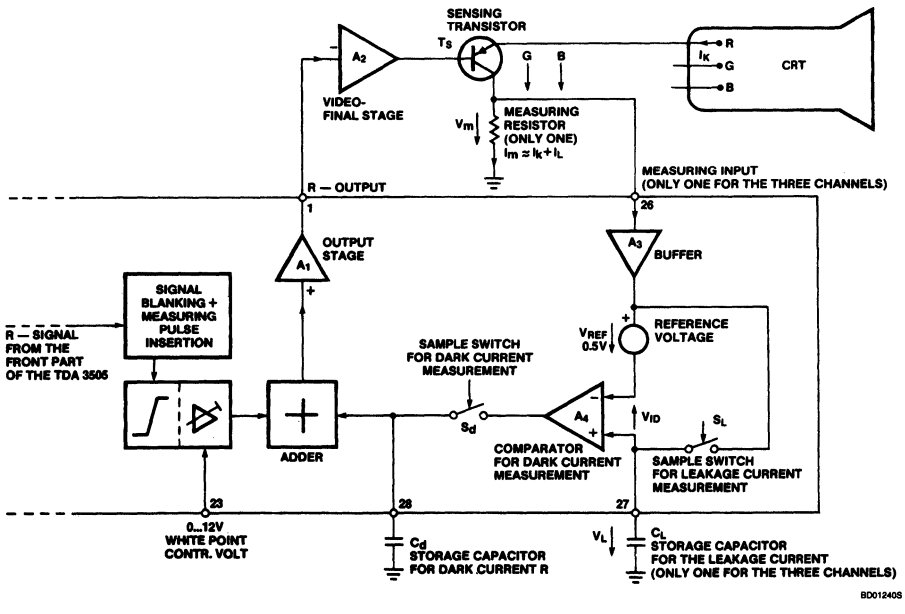

Figure 5. Function Block Diagram For The Dark Current Stabilization With The Video Comb. TDA3505 (R-channel)

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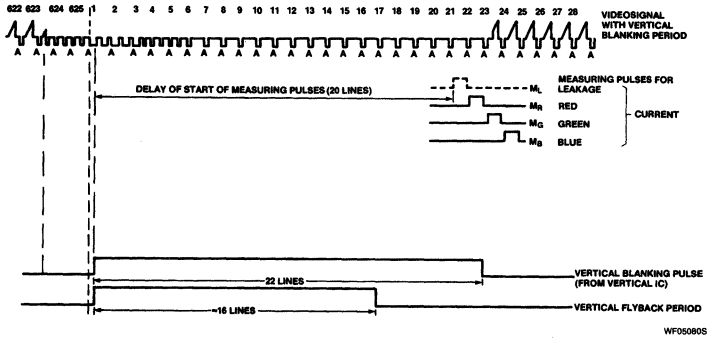

Figure 6. Position Of The Measuring Lines Of The Video Combination TDA3505

The R, G, B signals are blanked up to the inserted measurement pulses. The leakage current of all channels is measured in the line before the first measurement pulse. This is followed by the measurement pulses and their evaluation in the sequence red, green, blue.

A comprehensive application diagram with the video combination TDA 3505 and the video final stages is shown in Figure 7.

A complete Multi-Standard Decoder can be built up with the two IC's described above. A third IC, which can be interconnected in the color difference interface, can be used for color picture improvements by means of transient improvement of the color difference signals.

In Figure 8 the signal characteristics a) and b) show a transient in the Y and color difference signal. The rise time of the color difference signal is longer, corresponding to the smaller bandwidth. A delay line in the Y channel coordinates the centres of the transients as shown in Figure 8c.

In deviation from the previous signal processing, with the Color Transient Improvement IC the color difference transient does not occur until the input signal transient is finished, but then it occurs with a steepness corresponding to that of the Y signal. The characteristic of this color difference signal is shown in Figure 8d. It is now clear that – as shown in Figure 8e – a correspondingly longer delay is necessary for the Y signal in order to achieve coincidence of the transients.

Color signal transmissions, especially of test pictures coming via this CTI circuit, appear on the screen with the same color definition as RGB transmissions.

Figure 9 gives an explanation of the CTI function: the simplified circuits are shown on the left and the signals occuring at these are shown on the right. Part a shows a color difference input signal with a fast positive transient corresponding to the maximum bandwidth of the color difference signal.

The subsequent negative signal characteristics is slower. In this circuit the input signal is supplied after an impedance transformer via a switch and a further impedance transformer to the output. A storage capacitor is connected between the switch and the output impedance transformer, and is charged by the input impedance transformer in accordance with the signal characteristic.

Processing of the switching signal is effected by differentiation of the color difference signal, followed by full-wave rectification. Figure 9b shows the signals obtained in this way, which are supplied to a comparator via a high-pass filter. A diode at the high-pass filter reduces the charge reversal time and thus the dead time for generation of a switching signal for transients following in rapid succession. A comparator with threshold voltage generates a switching voltage as shown in Figure 9d from the signal of 9c when the threshold voltage is exceeded, and this triggers the switch. The switch is thus opened at the beginning of a transient and thus the voltage is maintained by the storage capacitor at the time before the transient. After completion of a fast transient the switch is closed and the capacitor's charge is changed in approx. 150ns to the voltage after the in approx. 150ns to the voltage after the

Figure 10 shows the entire block diagram with external circuitry of the CTI IC.

The lower CTI section effects signal processing for the two color difference signals in parallel circuits, as already described. Only one switching signal forming stage is incorporated, and this is triggered by the differentiating stage of the two channels. Thus the signal switches will always work in parallel, so that transient improvement is also parallel in the two channels.

The transient-improved color difference signals require a longer Y signal delay line with a delay time of up to 1000ns, and this is additionally realized in this IC in gyrator technique.

A selection capability has been incorporated for the delay time, by means of a switching voltage, since the total required delay time is dependent on the overall television receiver concept. The delay line comprises a total of 11 gyrator all-pass elements with a delay time of 90ns each, making a total of 990ns. The group delay and frequency behavior of the gyrator delay line is very good up to 5MHz.

A switching stage permits optional by-pass of one, two or three of these elements, so that a minimum of $8 \times 90ns = 720ns$ is effective. The transient improvement of the color difference signal makes coincidence errors with respect to the Y signal especially visible. A slight increase in delay time by 45ns has therefore been provided for fine tuning, working via an IC pin to be connected to ground.

A signal tapping is available before the last delay element for a further picture improvement capability by means of deflection modulation.

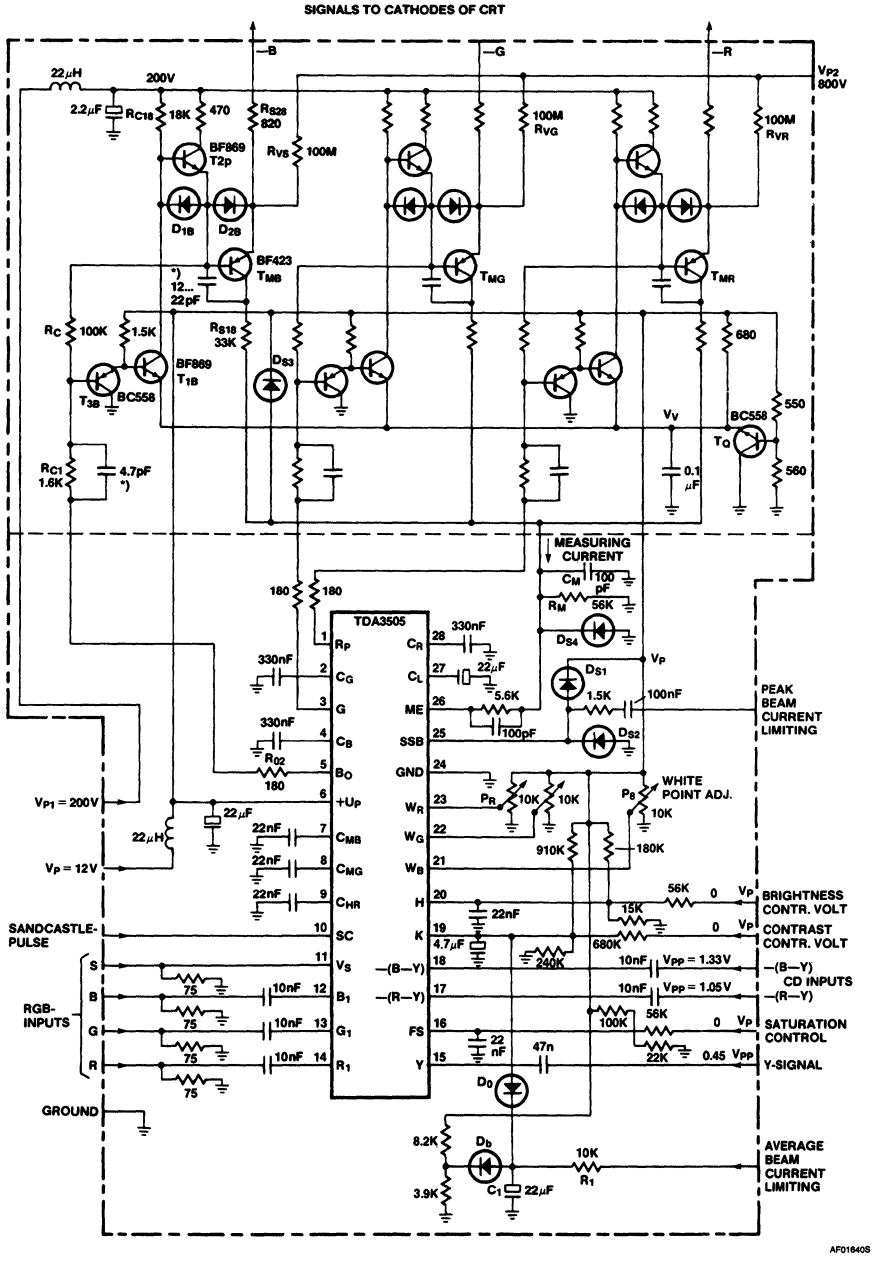

Figure 7. Application Diagram For The Video Combination TDA3505 And The Video Final Stages

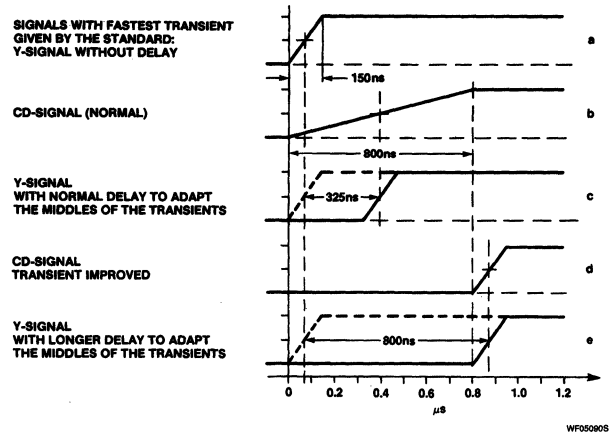

Figure 8. Y-delay Time For CD-signals Without And With Transient Improvement

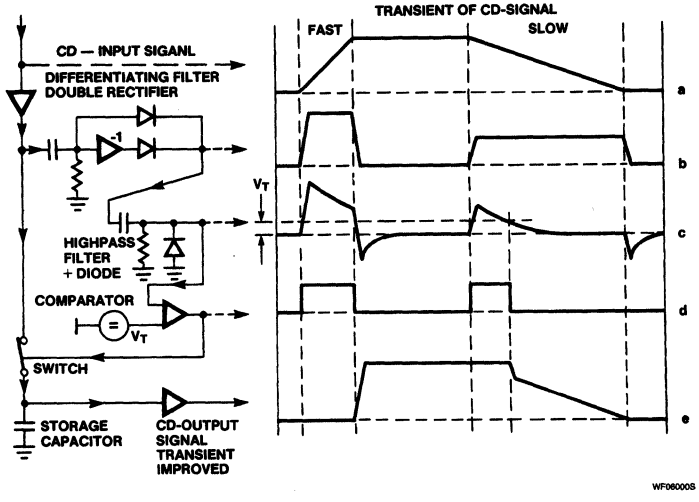

Figure 9. Function Of CTI

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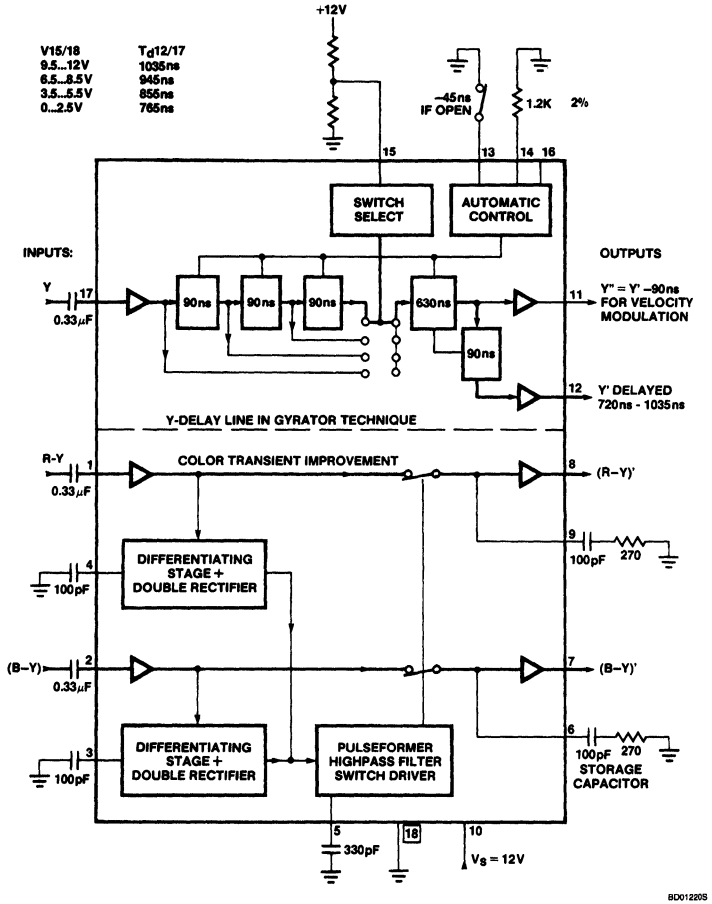

Figure 10. Block Diagram Of Picture Improvement IC TDA4560

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Four Standard Color Decoder With Picture Improvement — AN155

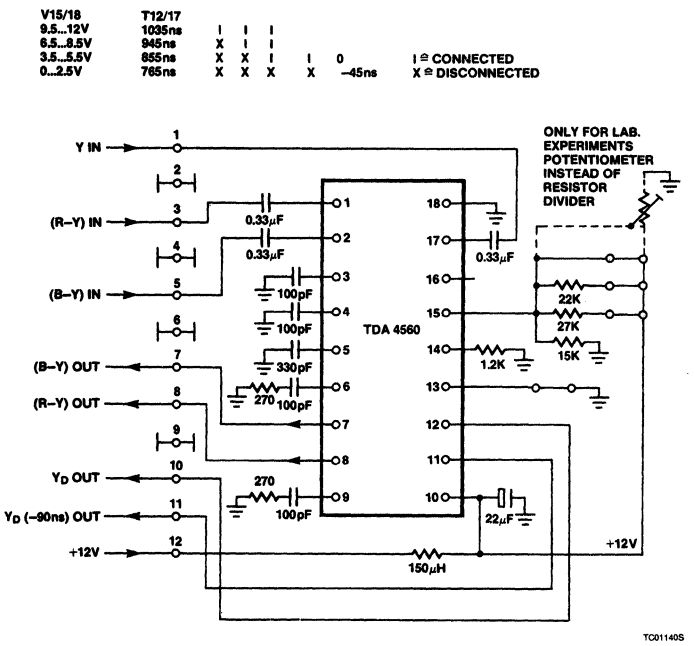


Figure 11. Circuit Diagram For CTI And Y-gyrator Delay Line With TDA4560

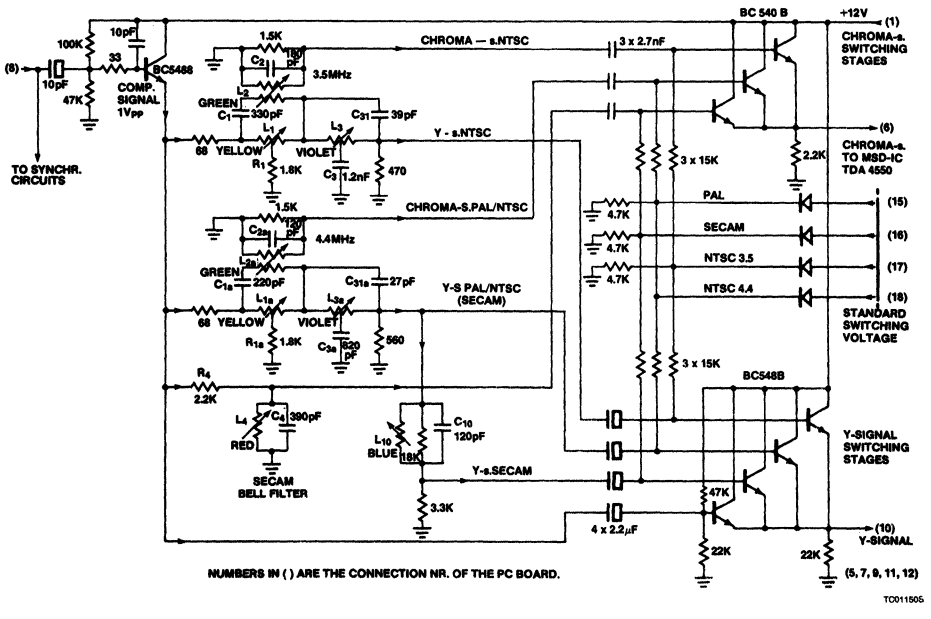
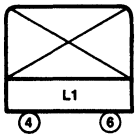
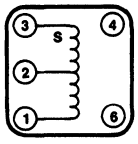


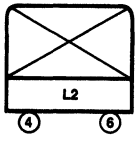
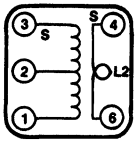
Figure 12. Chrominance And Luminance (Y) Signal Filters With Switching Stages For The MSD IC TDA4555

L1 YELLOW	DESIGN SPECIFICATIONS	TOKO'S SPECIFICATIONS
Center frequency	4.4MHz	4.4MHz
Tuning range (1 – 3)	240pF ± 10% at 4.4MHz	240pF ± 6% at 4.4MHz
Tuning capacitance	pF ± % (int)+ pF (ext)	pF ± % (int)+ pF (ext)
Inductance	5.5μH ± % at Hz	± % at Hz
Unloaded Q (Qu)	---- ± % at 4.4MHz	90 Min ± % at 4.4MHz

CONNECTION (BOTTOM VIEW)	STAMP & STAMPING SIDE	NUMBER OF TURNS			
		3 – 1	16		16
		3 – 2	8		8
		2 – 1			8
s: start of winding k: key of case x: cut of pin	Color YELLOW				

NOTES:
1. Qu & Ql measured without internal capacitor using Q-meter
2. Above sample modified from Toko Sample No.
3. (*) Indicates the data of customer's actual sample checked by Toko
   Chroma trap 2 x (4.4/3.5MHz)

L2 GREEN	DESIGN SPECIFICATIONS	TOKO'S SPECIFICATIONS
Center frequency	4.4MHz	4.4MHz
Tuning range (1 – 3)	105pF ± % at 4.4MHz	105pF ± 6% at 4.4MHz
Tuning capacitance	pF ± % (int)+ pF (ext)	pF ± % (int)+ pF (ext)
Inductance	12.5μH ± % at Hz	12.5μH ± % at Hz
Unloaded Q (Qu)	---- ± % at 4.4MHz	90 Min ± % at 4.4MHz

CONNECTION (BOTTOM VIEW)	STAMP & STAMPING SIDE	NUMBER OF TURNS			
		3 – 1	24		24
		4 – 6	1		1
s: start of winding k: key of case x: cut of pin	Color GREEN				

NOTES:
1. Qu & Ql measured without internal capacitor using Q-meter
2. Above sample modified from Toko Sample No.
3. (*) Indicates the data of customer's actual sample checked by Toko
   Chroma filter 2 x (PAL/NTSC)

Figure 13. Coil Specs For MSD Filter

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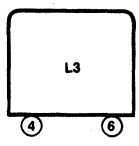
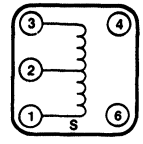
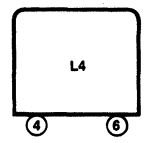
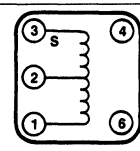
L3 VIOLET	DESIGN SPECIFICATIONS	TOKO'S SPECIFICATIONS
Center frequency	4.4MHz	4.4MHz
Tuning range (1 – 3)	66 μH ± 10% at 2.52MHz	66 μH ± 6% at 2.52MHz
Tuning capacitance	pF ± % (int)+ pF (ext)	pF ± % (int)+ pF (ext)
Inductance	H ± % at Hz	± % at Hz
Unloaded Q (Qu)	---- ± % at 4.4MHz	60 ±20% at 2.52MHz

CONNECTION (BOTTOM VIEW)	STAMP & STAMPING SIDE	NUMBER OF TURNS			
		1 – 3	65		65
		1 – 2	46		46
		2 – 3	19		19
s: start of winding k: key of case x: cut of pin	Color VIOLET				

NOTES:
1. Qu & Ql measured without internal capacitor using Q-meter
2. Above sample modified from Toko Sample No.
3. (*) Indicates the data of customer's actual sample checked by Toko
   Y-Aperture 2 x (PAL/NTSC)

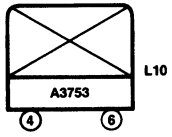
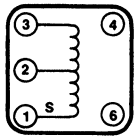
L4 RED	DESIGN SPECIFICATIONS	TOKO'S SPECIFICATIONS
Center frequency	4.4MHz	4.4MHz
Tuning range (1 – 3)	330pF ± 10% at 4.4MHz	330pF ± 6% at 4.4MHz
Tuning capacitance	pF ± % (int)+ pF (ext)	pF ± % (int)+ pF (ext)
Inductance	3·8μH ± % at Hz	3·8μH ± % at Hz
Unloaded Q (Qu)	---- ± % at 4.4MHz	60 ±20% at 4.4MHz

CONNECTION (BOTTOM VIEW)	STAMP & STAMPING SIDE	NUMBER OF TURNS			
		3 – 1	17		17
		3 – 2	14		14
		2 – 1	3		3
s: start of winding k: key of case x: cut of pin	Color RED				

NOTES:
1. Qu & Ql measured without internal capacitor using Q-meter
2. Above sample modified from Toko Sample No.
3. (*) Indicates the data of customer's actual sample checked by Toko
   Chromafilter SECAM bell 1 x

Figure 14. Coil Specs For MSD Filter

L10 BLUE	DESIGN SPECIFICATIONS	TOKO'S SPECIFICATIONS
Center frequency	4.4MHz	4.4MHz
Tuning range (1 – 3)	± % at MHz	120pF ± 6% at 4.4MHz
Tuning capacitance	pF ± % (int)+ pF (ext)	0 pF ± % (int)+ 120pF (ext)
Inductance	11μH ± % at Hz	± % at
Unloaded Q (Qu)	40 Min ± % at 4.4MHz	80 Min ± % at 4.4MHz

CONNECTION (BOTTOM VIEW)	STAMP & STAMPING SIDE	NUMBER OF TURNS			
		1 – 2			11
		2 – 3			11
		1 – 3			22
	Color BLUE				
s: start of winding k: key of case x: cut of pin					

NOTES:
1. Qu & Ql measured without internal capacitor using Q-meter
2. Above sample modified from Toko Sample No.
3. (*) Indicates the data of customer's actual sample checked by Toko

Glass delay line	2X
SECAM reference sig.	2X
SECAM reference ident	1X
Chroma trap SECAM	1X & 6X

Figure 15. Coil Specs For MSD Filter

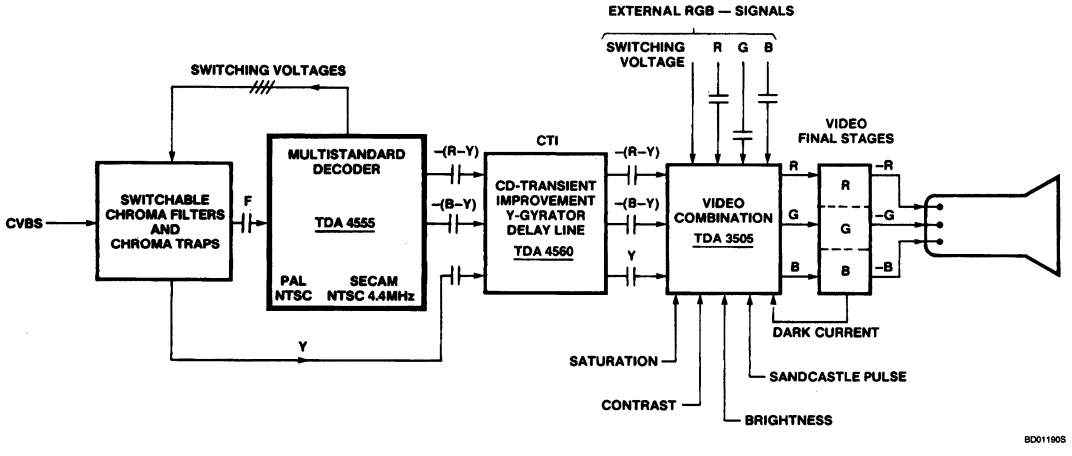


Figure 16. Block Diagram Of A Color Decoder With Baseband Signal Interface Using TDA4580

Four Standard Color Decoder With Picture Improvement AN155

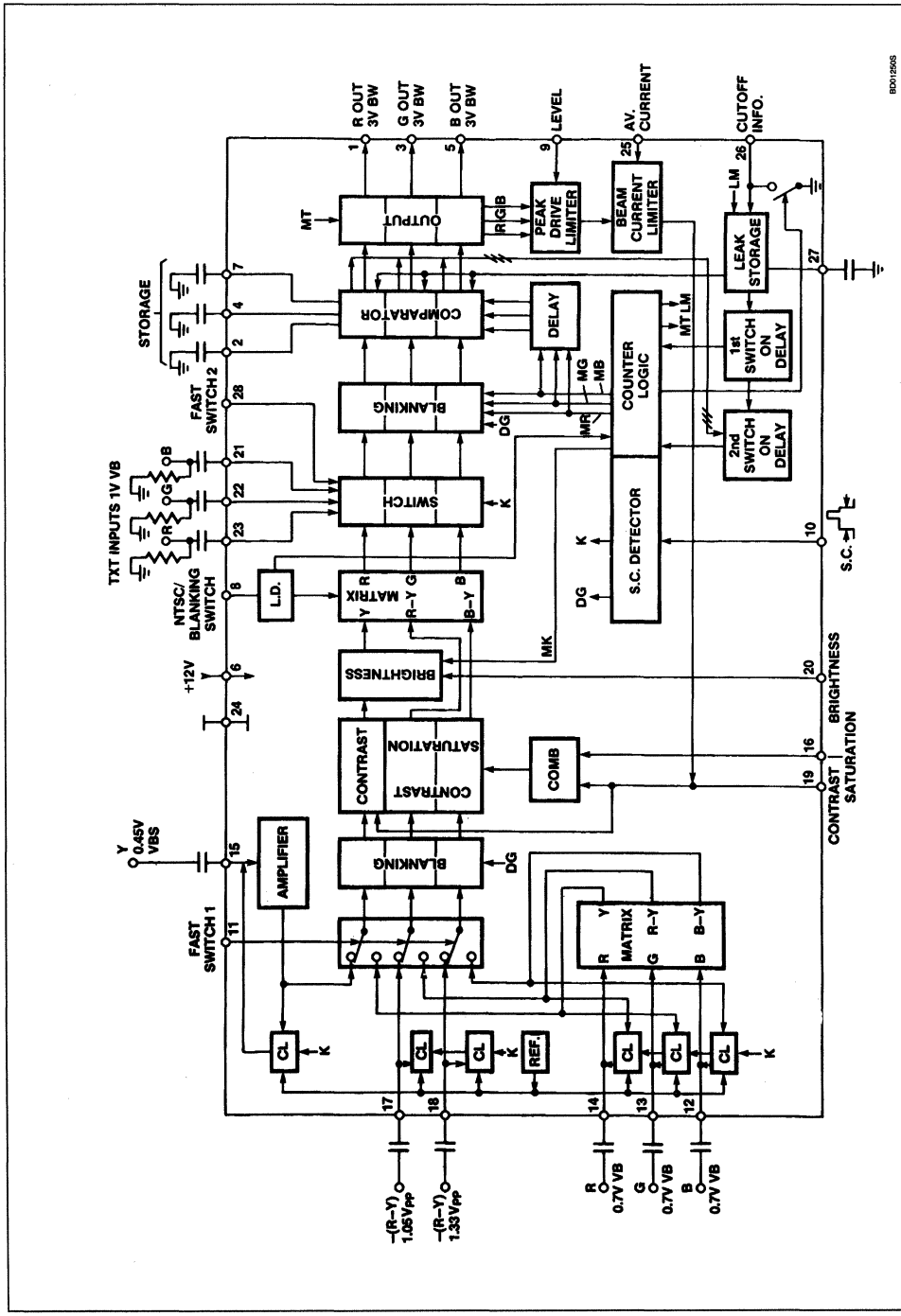


Figure 17. Video Control Circuit With Cut Off Control

Application of the N.T.S.C. Decoder: TDA3563 AN156

Author: H.J.S. Aben

INTRODUCTION

The 28-pin single chip decoder TDA3563 combines all the functions required for the identification and demodulation of NTSC signals.

Furthermore it contains a luminance amplifier, a R.G.B. matrix and R.G.B. amplifiers which provide nominal output signals of $5.3V_{pp}$.

It also contains analog inputs for external R.G.B. data signals. Switching over from video handling to data insertion occurs via fast video-data switching, which allows inlay of data into the running picture, without causing colored edges at the transients. So these inputs can be used for teletext, channel numbering, T.V. games, etc. The output signals are controlled by a peak white limiter, by means of an internal current sink on the contrast control voltage, which reduces the outputs when they tend to become too large. A description of the IC and its external circuitry is given in this report.

CIRCUIT DESCRIPTION

The block diagram of the TDA3563 is given in Figure 1. The internal circuitry connected directly to the pins will be discussed at the concerning subjects.

The Luminance Signal (see Figure 2)

The luminance channel is designed for luminance signals with negative-going sync pulses which should have a typical amplitude of $0.45V_{pp}$ (peak white to sync). So the decoder can also be easily designed to accept external video signals with an amplitude of $1V_{pp}$ (e.g. video recorder signals). The luminance signal is AC coupled to the luminance input (pin 10) where it is clamped to an internal reference voltage of about $2.5V_{DC}$.

The input impedance is very high (input current typ. 0.15=mμA) and the charging and discharging currents of the coupling capacitor are very small. Therefore a 1K delay line circuit can be placed in front of it, without influencing the black level of the input signal noticeably (also see Figure 3). Additionally the coupling capacitor can be small: 10nF. During clamping the input is very low-ohmic, which reduces noise and residual signals.

The clamping pulse is obtained from the upper part of the sandcastle pulse (pin 8) and it operates only during the back porch of the video signal. In the luminance contrast control stage the luminance is gain controlled by a DC voltage from the lin-log converter of the contrast control voltage at pin 7. For a control range of 2.0 to 4.0V there exists a linear relationship between a voltage change at pin 7 and the gain of the luminance contrast control stage (see Figure 4a).

The input impedance at this pin 7 is very high (maximum input current 15=mμA), so remote control circuitry can directly drive the contrast control without need for an impedance converter. (This also holds for the saturation and the brightness control inputs, resp. pins 6 and 11.)

The total contrast range is in excess of 20dB. At nominal contrast control voltage ($3.4V_{DC}$) and nominal input signal of $0.45V_{pp}$ (including sync pulse) the output signals at the R.G.B. output pins (resp. pins 12, 14 and 16) are $5.3V_{pp}$ (black to white). At maximum contrast control voltage ($4V_{DC}$) the output signals have an amplitude of +3dB, with respect to their nominal value. At minimum contrast control voltage ($2.0V_{DC}$) the output signals still have an amplitude of minus 17dB with regard to their nominal value (about 15% rest signal). This to avoid completely disappearing of the picture on the screen at mistuned front controls.

If the voltage at pin 7 is below $1.2V_{DC}$ (this is outside of the normal contrast control range) the output signals are completely suppressed (minus 40dB); also see Figure 4a. After contrast control, the luminance signal is fed to the three matrix circuits.

The External Luminance Input Circuit (also see Figure 3)

A composite video signal of $2.7V_{pp}$ is assumed with a low-ohmic source impedance:

The video signal is fed to an 3.58MHz trap (L1C1) and a delay equalization circuit (L2C2). Because of the latter the attenuation of the 3.58MHz chroma signal can be very high without causing group delay distortion into the luminance signal. Besides it has the additional advantage of contour correction, which generates very sharp transients; see Figure 6.

- the upper signal shows a 250kHz bar with a contour correction of about 10%
- the lower signal is the corresponding sweep signal up to 10MHz

The extension of contour correction depends on the source impedance of the video signal (the original source impedance plus the value of resistor R1) and on the adjustment of L2. (If a cheaper 3.58MHz trap or a comb filter is preferred, the filters L1C1 and L2C2 can be replaced by it.)

After trapping, the luminance signal is fed via a luminance delay line and a resistor network to a coupling capacitor of 10nF.

* NOTE: If a video input signal of $1V_{pp}$ is used R2 can be omitted and R3 should then have a value of 1 Kohm without changing the rest of the input circuit.

The Chrominance Signal (see Figures 3 And 7)

Via C3 the composite video signal is fed to the 3.58MHz bandpass filter, consisting of L4, C4 and R4. The chrominance information then is fed via a coupling capacitor of 10nF to the chroma input (pin 3). The chrominance channel has an asymmetrical input and must be AC coupled; its amplitude should be between 55 and $1100mV_{pp}$ (which corresponds to 25 and $500mV_{pp}$ burst information of a 75% saturated color bar). It

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Application of the N.T.S.C. Decoder: TDA3563 AN156

may not exceed $1.1V_{pp}$, otherwise clipping of the input signal will occur. The chrominance signal is first fed to the gain control stage, which has a control range in excess of 30dB, controlled by the A.C.C. (Automatic Color Control) detector. After this the signal is fed to the gated saturation and contrast control stages. The contrast stage is directly coupled to the luminance contrast control, so that there is a good tracking between the luminance and the chrominance contrast control. Typical tracking is within 1dB over a control range of 10dB, starting at maximum contrast.

The saturation control stage is driven by a DC voltage of the lin-log converter of the saturation control voltage at pin 6. The control range is in excess of 50dB, which corresponds to a saturation control voltage of 2.0 to $4.0V_{DC}$; also see Figure 4b.

To cancel the settings of saturation and contrast control during the burst information, the two control stages are set at maximum gain during flyback. Via an emitter follower the chrominance signal is fed to the chrominance output (pin 28).

* NOTE: If a video signal of $1V_{pp}$ is used C4 should have a value of xxpF and R4 can be omitted.

Via a capacitor of 220pF the chrominance output signal at pin 28 is fed to the demodulator input pin 21, where the chrominance signal is split up into two ways, the first going to the color demodulators and the second going to the chrominance reference circuit.

The Chrominance Reference Circuit (see Figure 8)

The chrominance signal at pin 21 is fed to a Miller integrator, which is biased via pin 23, where it is shifted over 90 degrees. Both the original incoming signal and the shifted signal are fed to a mixer circuit, which is controlled by the DC voltage of the hue control voltage at pin 25.

The voltage range of the hue control at pin 25 corresponds to a phase control; (see Figure 5a). In this way the chrominance signal of the reference circuit is phase-controlled. A gain control circuit is required in the 90° phase shift circuitry to make the chrominance voltage independent of the Hue setting. Its control voltage is decoupled by the capacitor connected at pin 5.

The Burst Phase Detector

The burst phase detector consists of a synchronous detector, in which the phase controlled chrominance signal is demodulated by the (R-Y) reference signal, obtained from the divider-by-2 circuit of the reference oscillator. Via the low pass filter R5, C5 and C6 at pin 24 the demodulated burst information is fed to the reference oscillator. In this way the reference oscillator is locked to the hue controlled chrominance signal.

The Reference Oscillator

The 7.16MHz reference oscillator operates at twice the subcarrier frequency and is controlled by the burst phase detector, which is gated with the narrow part of the sandcastle pulse. As the burst phase detector has an asymmetrical output the oscillator can be adjusted by changing the voltage of the output (pin 24) via a high-ohmic resistor (R6). The capacitor in series with the X-tal (pin 26) should then have a fixed value.

When pin 6 (saturation control) is connected to the positive supply line, the burst phase detector is biased in its nominal position and the color killer is overruled. In this position the reference oscillator can be adjusted (see chapter 3.1).

By dividing the oscillator signals by a factor 2, two reference signals, with a mutual phase difference of 90 degrees are obtained.

A.C.C. and Color Killing

For the generation of the A.C.C. control voltage, the phase controlled burst information is synchronously demodulated in a separate A.C.C. detector. Because the burst information as well as the reference signals are phase controlled, there will be no mutual phase difference. In this way the demodulated burst amplitude information will be independent of hue settings.

The output pulses of this detector are peak detected at pin 4 to control the gain of the chrominance amplifier, thus preventing blooming up of the color during weak signal reception, and fed to the A.C.C. gain control stage of the chrominance channel (also see Figure 7). To obtain information for the color killer, the output pulses of the A.C.C. detector are also detected by a sample and hold circuit, this output voltage is available at pin 2. For a decreasing burst information the control voltage also decreases until it reaches an internal fixed reference voltage of xxV_{DC}; then the killer becomes active. At that moment the demodulators are switched off and an internal current sink reduces the saturation control voltage to a low level (provided the source impedance of the external saturation control network is sufficiently high). Color switch-on can be delayed by proper choice of the time constant of the saturation setting circuit. Manual killing can be achieved by connecting pin 6 to ground.

Reference Signals for the Demodulators (see Figure 9)

The reference signal for the (B-Y) color demodulator is directly achieved from the divider-by-two circuit.

To obtain a flesh tone correction, the reference signal for the (R-Y) color demodulator is achieved by mixing the (R-Y) and (B-Y) reference signals to a new (R-Y)* reference signal. When pin 22 is left open there is a mutual phase relation of about 115 degrees between the (B-Y) and the (R-Y)* reference signal. If a DC voltage is connected to pin 22, this phase angle can be adjusted between 90° and 140° (see Figure 10).

The Color Demodulators

The incoming chrominance signal at pin 21 is also fed to the two demodulators. The reference signals for the demodulators are hue controlled, so the chrominance output signals of the demodulators will also be hue controlled.

Also for flesh tone correction the gain of the two demodulators is made identical. This means that the amount of (R-Y) information is increased by a factor 1.78.

The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix, where the (G-Y) signal is composed by:

$$(G\text{-}Y) = -0.27(R\text{-}Y) - 0.22(B\text{-}Y).$$

This means that only the red information is increased.

The Video Control Circuits (see Figure 11)

The R.G.B. Matrices

Because the three matrix and output circuits are identical, only the R-channel will be described.

The luminance signal from the luminance contrast control stage and the color-difference signal from the (R-Y) matrix are added in the matrix circuit. After this the signal is fed to the Video-Data switch.

The Video-Data Switch

This single chip NTSC decoder also has the facility for inserting analog external R.G.B. signals at resp. pins 13, 15 and 17. The black level of the inserted signals are equalized to the black level of the internal video signals. In this way there will be no mutual black level difference between the video and the inserted R.G.B. signals. For this purpose the external signals are AC coupled to the input pins and clamped during the upper part of the sandcastle pulse. The source impedance of the external signals should not exceed a value of 150 ohm to avoid any disturbance of black level during clamping.

Switching-over from video handling to external data insertion is activated by means of the input signal at pin 9. If the voltage level at this Switch input pin 9 exceeds a DC level of $0.9V_{DC}$ the internal R.G.B. signals, coming from the matrix circuits, are switched off and the external R.G.B. signals are inserted. Because switching times are very short (within 20nsec) also inlay of data into the running

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picture, e.g. teletext information, channel numbering, is possible without causing colored edges at the transients of the inserted signals. For an output signal amplitude of nominal $5.3V_{pp}$ the external input signal should have an amplitude of $1V_{pp}$.

Because the inserted signals are clamped by means of the sandcastle pulse, the external R.G.B. signals must be synchronous with the video input signal and the sandcastle pulse.

Even if they are not inserted by means of the video-data switching signal at pin 9, the external signals at the input pins 13, 15 and 17 must be synchronized. This is in order to avoid a disturbance of the control voltages at the storage capacitors at the pins 18, 19 and 20, by large current surges, introduced by voltage steps in the external signals during clamping time. This effect would disturb the black level of the output signals considerably and would be visible on the screen. If only video handling is wanted, the components at the switch and data inputs can be omitted.

The Brightness Control

After the Video-Data Switch the signal is amplified and fed to a black level clamp. The black level of the output signal is compared with an external reference voltage level (pin 11) which is used for brightness setting, and the control voltage is stored in a capacitor that is connected to pin 20 (pins 19 and 18 for resp. G and B). The clamping pulse is derived from the small upper part of the sandcastle pulse at pin 8.

The Peak White Limiter

The maximum white level of the output signals is $9.3V_{DC}$. If one (or more) of the output signals tends to surpass this level, the output signal will be clipped to this maximum voltage level and at the same time the peak white limiter becomes active. It reduces the output signals via the contrast control by discharging the smoothing capacitor C7 at pin 7 via an internal current sink of about 5mA. As long as the output signal is too high, the current sink will be active. The time constant of decreasing the contrast setting voltage is determined by the internal discharging current of 5mA and by the value of the smoothing capacitor C7. The recovery time is determined by the source impedance of the resistor network at pin 7. The complete time constant of loading and unloading should be chosen so that the peak white limiting action will not become visible on the screen within one field period. When this time constant is too small, the contrast setting voltage will decrease too rapidly (e.g. within some line periods) and will also recover too fast after the limiting action stops (depending on the picture contents). When this happens the complete action becomes visible on the screen; if there is a white object on the screen (with too high amplitude), the complete video signal amplitude will be reduced rapidly and when the object ends, the video signal amplitude also increases very fast. This would result into horizontal bars of different brightness on the screen; the length and the number of bars depends on the video contents.

Note: The peak white limiter will also be activated if the inserted R.G.B. signals become too large. However, these signals are not contrast-controlled and cannot be reduced by the limiter. If the inserted signals are inlaid into a running picture, and the peak white limiter is activated by them, the R.G.B. signals will be clipped at $9.3V_{DC}$, but the normal video signal will disappear because the limiter will reduce the contrast-setting voltage completely.

The Sandcastle Pulse Processor (see Figure 9)

In the sandcastle pulse processor, the sandcastle pulse at pin 8 is separated into two timing pulses. The first pulse is separated at a voltage level of $1.5V_{DC}$ and will be used for gating in the chrominance channel (for the gated saturation and contrast amplifiers) and for blanking the R.G.B. output signals. During blanking a level of $2V_{DC}$ is available at the outputs.

The second timing pulse is separated at a voltage level of $7V_{DC}$; this pulse is used for black level clamping and burst keying. Therefore, the upper part of the sandcastle pulse should start just after the horizontal synchronization pulse, to prevent black level clamping during the sync. pulse.

The Control Setting Circuits

Figure 3 also shows the resistor networks that are used to make the control voltage ranges, for the several controls, out of a control range of 0 to V_{supply}. This means that all the front controls of the color receiver are standard from zero up to the supply voltage. Using such networks it is also possible to transform control voltage ranges from remote control systems to the required voltage ranges in an easy way. Also see Appendix 1.

The contrast control voltage should also be controlled by the average beam current limiter, which should become active if the average beam current exceeds a certain value. At that moment the capacitor at pin 7 should be discharged via diode D1.

The contrast and saturation control voltages can be overruled by service switches used for adjustment procedures.

ALIGNMENT PROCEDURES

Only four adjustments are required by the whole decoder:

- the reference oscillator
- the 3.58MHz trap in the luminance channel
- the contour correction in the luminance channel
- the 3.58MHz band pass in the chrominance channel

The Reference Oscillator[1]

For adjusting the frequency of the reference oscillator, the color information on the screen can be used without using any extra measuring instruments:

1. apply a color bar signal.
2. connect pin 6 (sat.) to the supply voltage; the oscillator is free-running now and the killer is set at unkilling.
3. adjust R9 for minimum rolling of the colors on the screen.
4. remove connection of pin 6 to supply voltage.

The 3.58MHz Trap in the Luminance Channel

1. apply a color bar signal.
2. observe one of the output signals (pin 12, 14 or 16) and adjust L1 for minimum subcarrier information.

or

1. apply a plain color picture, e.g. red.
2. put the saturation control to minimum so that the screen becomes grey.
3. put contrast to maximum.
4. put brightness to normal position.
5. adjust L1 for minimum 3.58MHz interference on the screen.

Contour Correction

1. apply a 250kHz bar luminance signal, with rise and fall times of about 90nsec.
2. observe one of the output signals (pin 12, 14 or 16) and adjust L2 for equal pre- and overshoots. (also see Figure 5)

The 3.58MHz Band Pass in the Chrominance Channel

1. apply a color bar signal.
2. observe one of the output signals (pin 12, 14 or 16) and adjust L4 for optimum step response.

NOTE:
1. For alternative adjustment procedure, see Appendix II.

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AN156

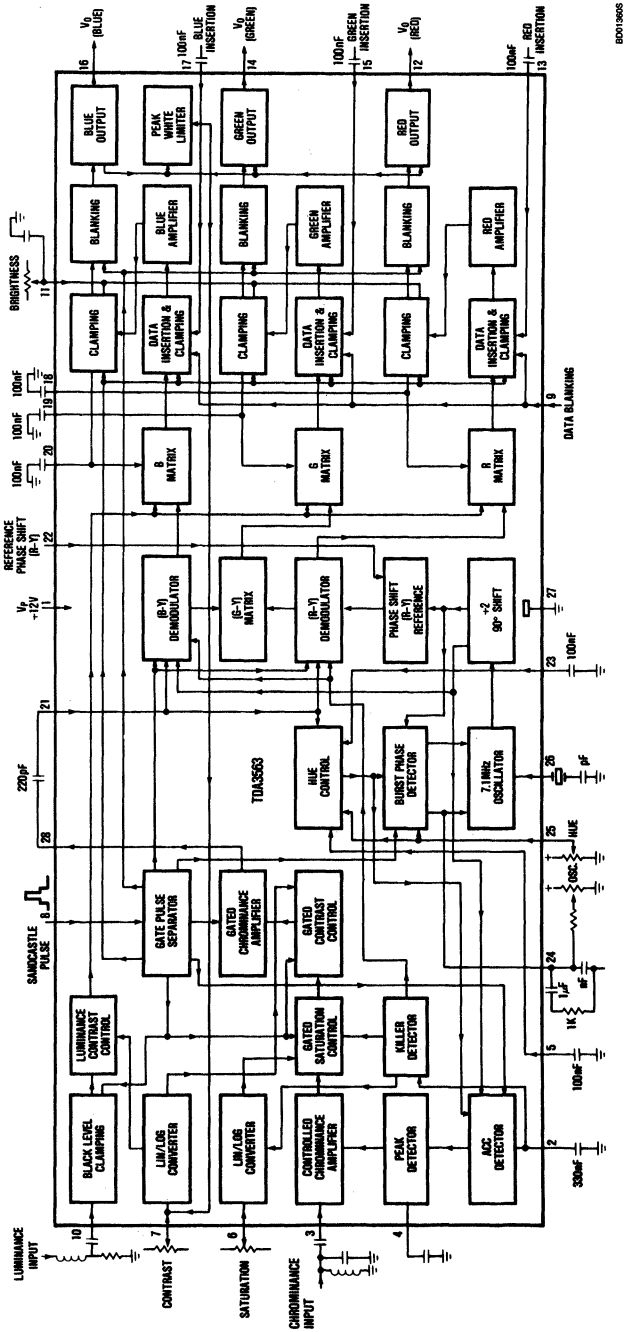


Figure 1. The Block Diagram of the N.T.S.C. Decoder: TDA3563.

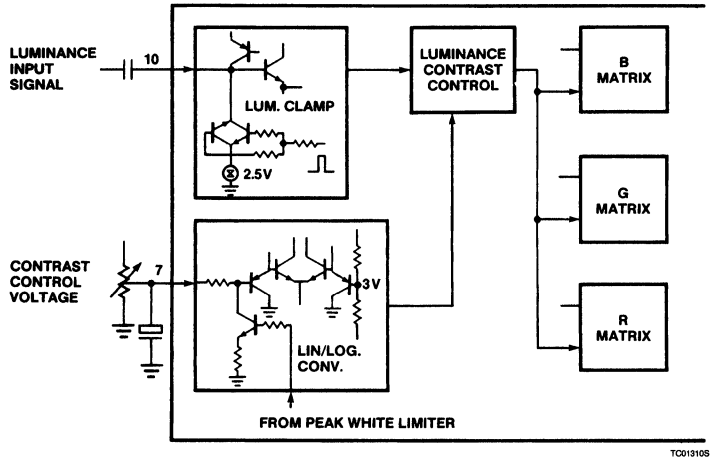


Figure 2. The Luminance Channel.

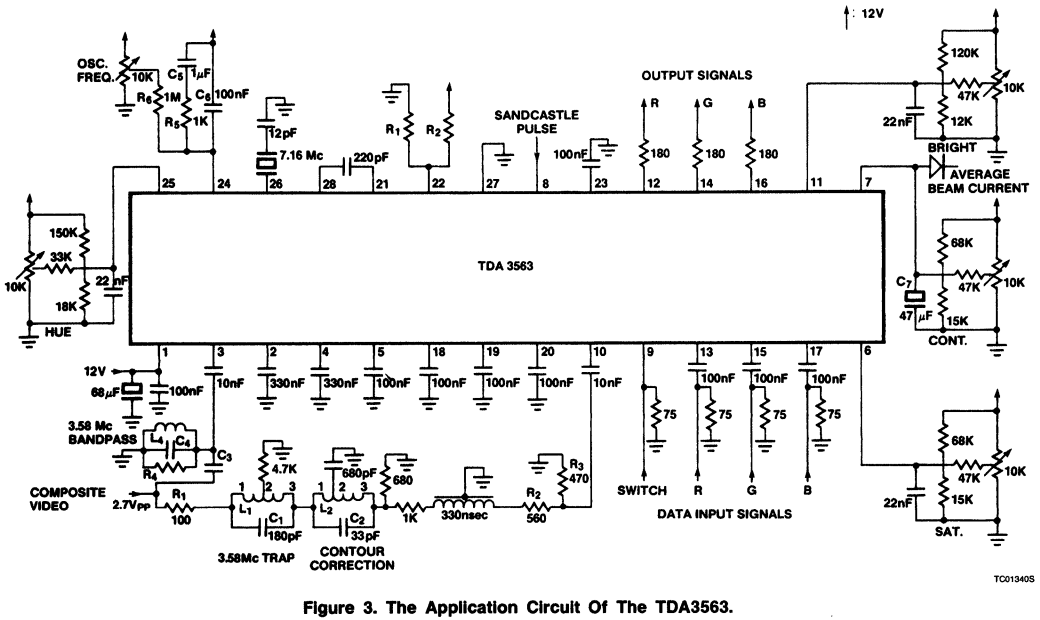
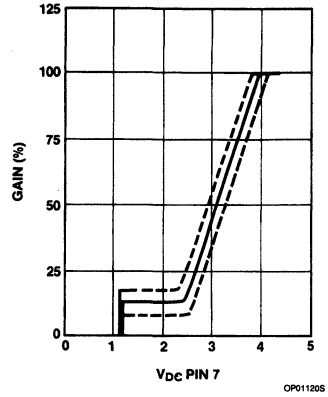
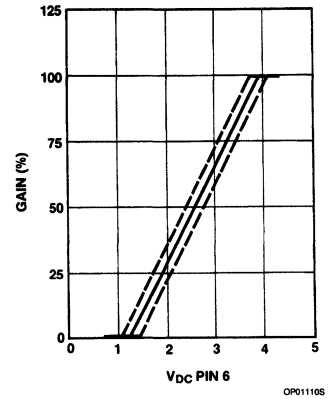


Figure 3. The Application Circuit Of The TDA3563.

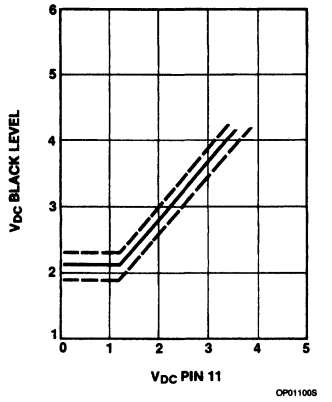


a. The Control Characteristic Of The Contrast Control.

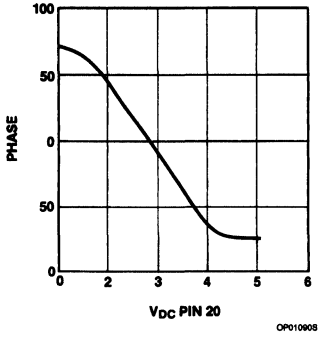


b. The Control Characteristic Of The Saturation Control.

Figure 4



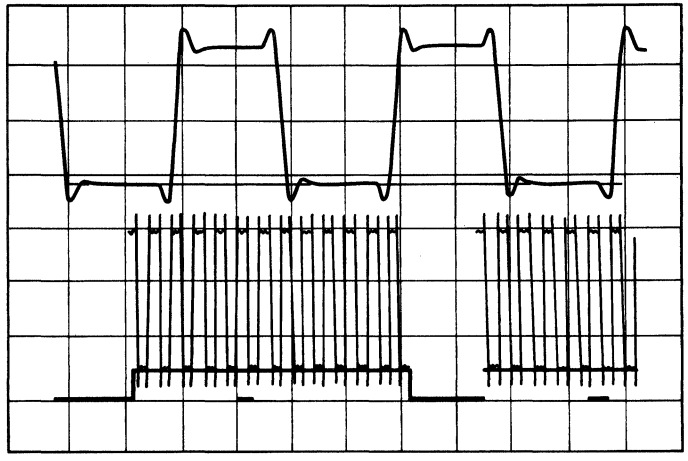
a. The Control Characteristic Of The Brightness Control.



b. The Control Characteristic Of The Hue Control.

Figure 5

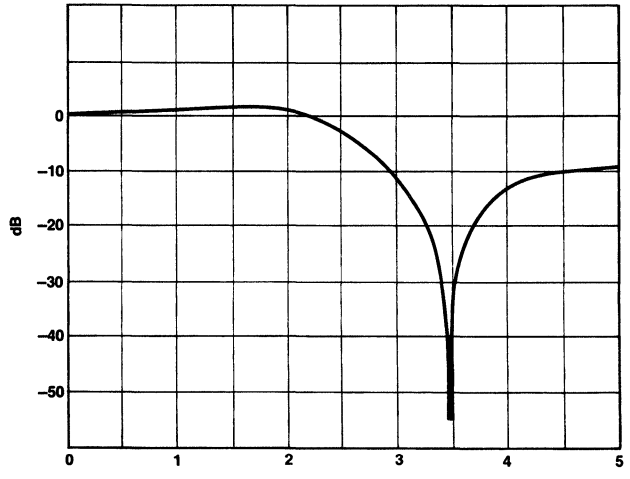
9



200kHz BAR SIGNAL

OP01080S

a



SWEEP SIGNAL 0 to 5MHz

OP01070S

b

Figure 6. The Contour Correction.

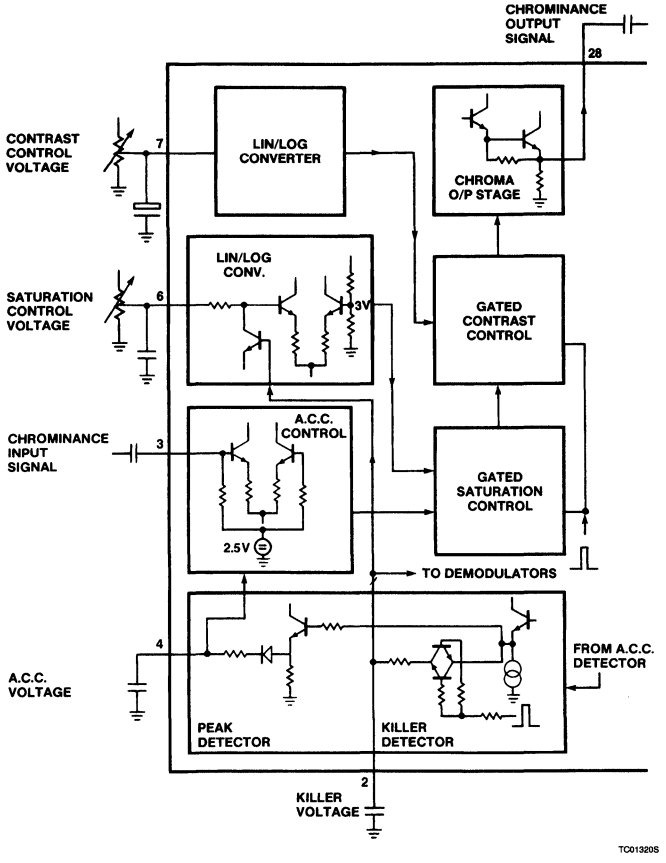


Figure 7. The Chrominance Channel.

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Application of the N.T.S.C. Decoder: TDA3563 AN156

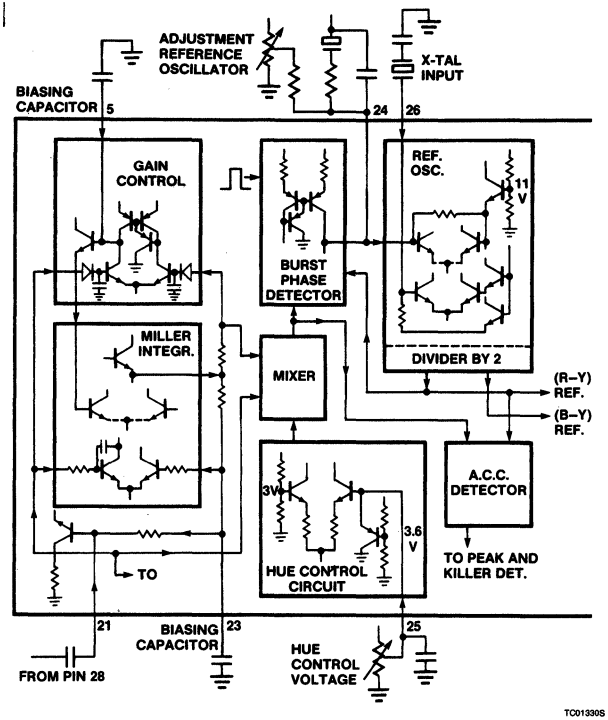


Figure 8. The Chrominance Reference Circuits.

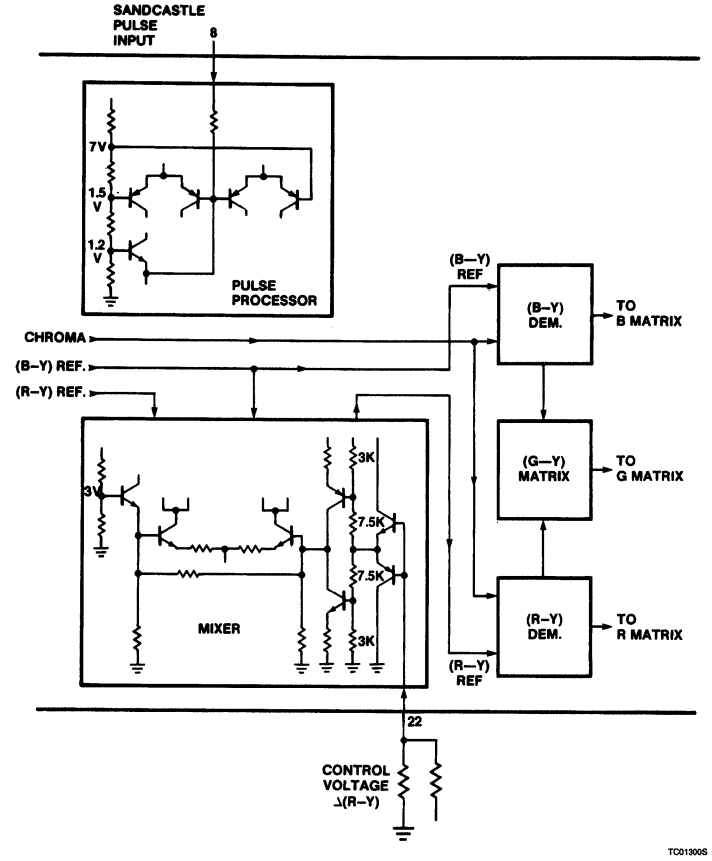


Figure 9. The Chrominance Reference Circuits (Continued).

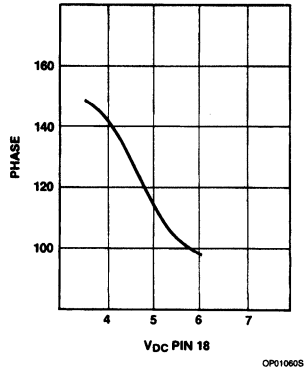


Figure 10. The Control Characteristic Of The Phase Of The (R-Y) Reference Signal, (B-Y) Phase Is Equal To Zero.

9

Application of the N.T.S.C. Decoder: TDA3563 AN156

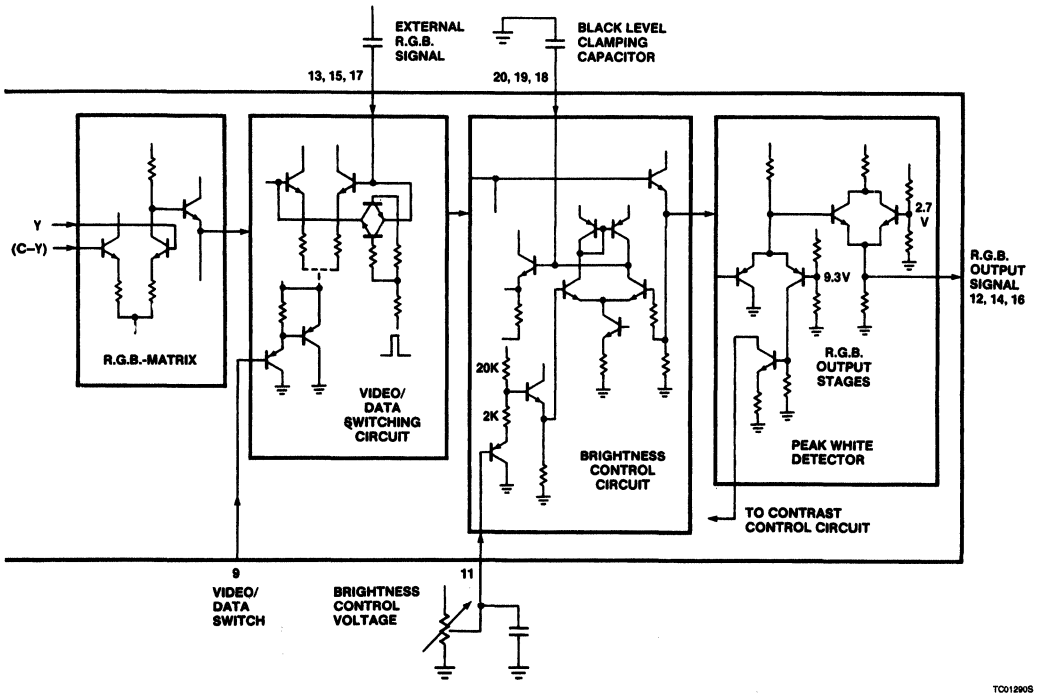
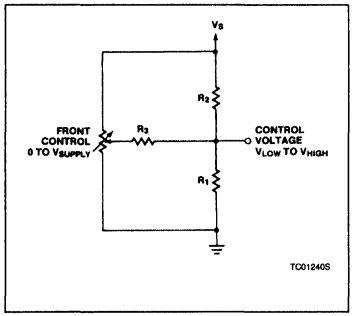


Figure 11. The Video Control Circuits.

Application of the N.T.S.C. Decoder: TDA3563 AN156

APPENDIX I:

Conversion of a full swing control voltage range (from zero up to V_{supply}) into a restricted control voltage range of V_{low} to V_{high}:



The resistors R_1, R_2 and R_3, as a function of the source impedance R_s of the network, are defined by the following formula:

* first define a source impedance R_s

* $R_1 = \frac{V_s}{V_s - V_H} \times R_s$

* $R_2 = \frac{V_s}{V_L} \times R_s$

* $R_3 = \frac{V_s}{V_H - V_L} \times R_s$

APPENDIX II

Temporary Information, Concerning TDA3563 Versions Up to N6

Alternative Adjustment Procedure for the Reference Oscillator of the TDA3563

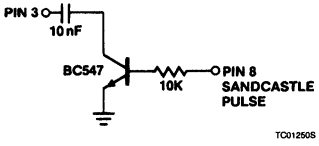
Using the normal frequency adjustment procedure for the reference oscillator of the TDA3563, i.e. setting the saturation control voltage (pin 6) to 12 volt (unkilling and unlocking of the reference oscillator), and adjusting the trimmer capacitor for minimum rolling of color bars on the TV screen, the adjustment is disturbed by an internal defect of the burst phase detector.

If the reference frequency is adjusted in this way, it results into a frequency deviation of about 1kHz when removing the 12 volt connection at the saturation control input. So this frequency adjustment of the oscillator of the TDA3563, N6 cannot be used.

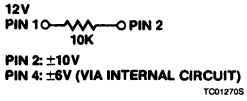
Therefore an alternative adjustment procedure is developed:
The X-tal has now a fixed capacitor of 12pF in series to ground, instead of the trimmer capacitor. The frequency adjustment is done via current injection into the burst phase detector (pin 24).

The reference oscillator is made free running by removing the burst information out of the chrominance signal.

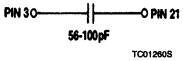
ADJUSTMENT PROCEDURE FOR THE REFERENCE OSCILLATOR OF THE TDA3565, N5.



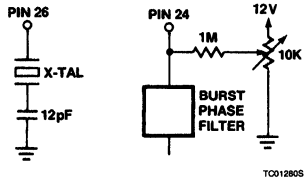
1. Connect An Electronic Switch To Pin 3. (Removing the burst information)



2. Connect A Resistor Of 10 Kohm Between Pin 2 And 12V Supply Line. (Color killer off and ACC control to minimum)



3. Connect A Capacitor of 56 to 100pF Between Pins 3 And 21. (Input signal at the demodulator input will be without any burst information)



4. Frequency Adjustment Of The Oscillator. (Adjust the potentiometer for minimum rolling of color bars at the TV screen)

9

Microcomputer Peripheral IC Tunes and Controls a TV Set AN157

The necessity for television set manufacturers to reduce costs, provide more features, simplify tuning and incorporate remote control has led to a need for all-electronic digital tuning and control circuits. Naturally enough, component manufacturers would prefer to meet the need with a dedicated integrated system which they can make in large quantities. This however is impractical because it would not allow the set manufacturers to satisfy the widely varying requirements of the tv market. The most suitable system is therefore one controlled by a standard microcomputer (e.g. one from the MAB8400 family), so that the variants can be accommodated by software. The only additional components than then need to be separately integrated are those required for interfacing and for performing functions that cannot be handled by the microcomputer because of speed, voltage or power consumption considerations. To minimise costs and maximise performance however, the partitioning of the remaining functions and their allocation to various integrated circuits peripheral to the microcomputer must be carefully considered.

Figure 1 illustrates the control and tuning functions in a basic tv set and shows how the circuitry is positioned within the cabinet. Some of the functions are concentrated around the microcomputer and mounted close to the front panel to reduce the cost of the wiring to the local keyboard and displays. The tuning and analogue controls are on the main chassis. The only link between the microcomputer and the main chassis is a 2-wire bidirectional I^2C bus which allows the microcomputer to read tuning status and other information from the main chassis, and to write data regarding required frequency and analogue control settings to the main chassis.

The foregoing considerations have led to the design of the SAB3035 integrated Computer Interface for Tuning

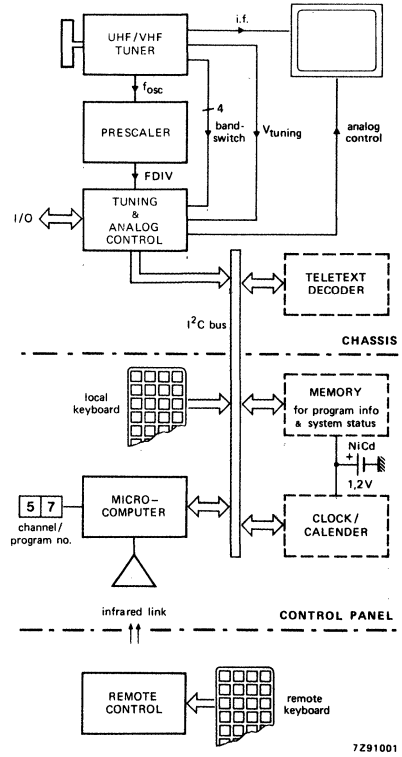


Fig.1 Basic tv control system

and Analogue Control (CITAC). The SAB3035 is an I²C bus-compatible microcomputer peripheral IC for digital frequency-locked loop (FLL) tuning and control of analogue functions associated with the tv picture and sound. As shown in block form in Fig.2, the IC incorporates a frequency synthesiser using the charge pump FLL principle and contains the following circuits:

- 15-bit frequency counter with a resolution of 50 kHz
- charge pump and 30 V tuning-voltage amplifier
- a.f.c. amplifier
- logic circuitry for programming the currents from the charge pump and a.f.c. amplifier
- four high-current band switches
- four general purpose I/O ports for additional control functions
- a one-pin crystal-controlled 4 MHz reference oscillator
- receiving/transmitting logic for the 2-wire I²C bus
- eight static DACs for control of analogue functions associated with the picture and sound.

FUNCTIONAL DESCRIPTION

I²C bus

The SAB3035 is microcomputer-controlled via an asynchronous, Inter-IC (I²C) bus. The bus is a two-wire, bi-directional serial interconnect which allows integrated circuits to communicate with each other and pass control and data from one IC to another. The communication commences after a start code incorporating an IC address and ceases on receipt of a stop code. Every byte of transmitted data must be acknowledged by the IC that receives it. Data to be read must be clocked out of the IC by the microcomputer. The address byte includes a control bit which defines the read/write mode.

Frequency synthesis tuning system

Figure 3 is the block diagram of the frequency synthesising system comprising a frequency-locked loop (FLL) and an external prescaler which divides the frequency of the voltage-controlled local-oscillator in the tv tuner by 64 or 256. The tuning section comprises a 15-bit programmable

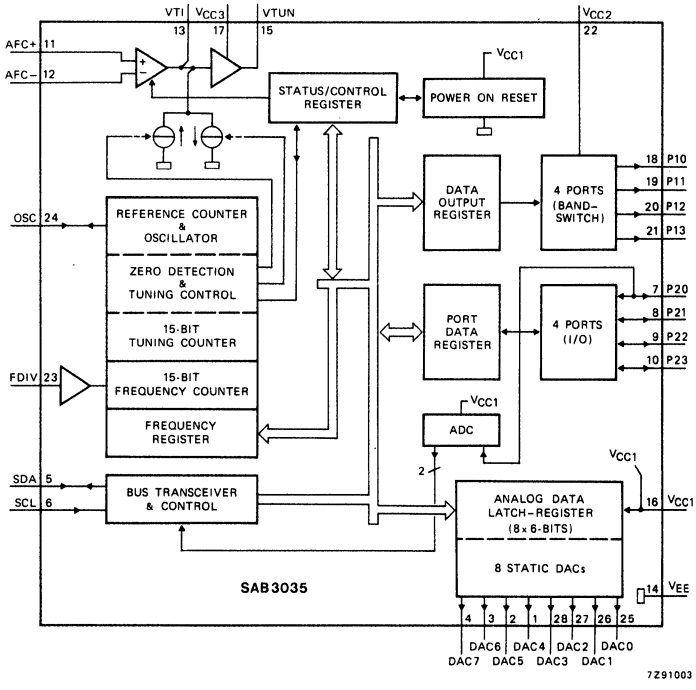


Fig.2 Block diagram of the SAB3035

Microcomputer Peripheral IC Tunes and Controls a TV Set AN157

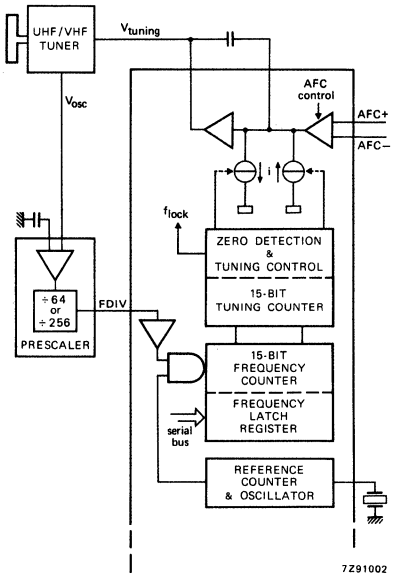


Fig.3 Block diagram of the SAB3035

frequency counter, a 15-bit tuning counter, tuning control and zero detection logic, a reference counter and a charge pump followed by a low-pass filter amplifier.

Input FDIV accepts frequency-divided local-oscillator signals with a level of more than 100 mV and a frequency of up to 16 MHz. The frequency measurement period is defined by passing the internally amplified signal from FDIV through a gate which is controlled by the reference counter. The reference counter is driven by a crystal-controlled oscillator, the low-level output of which is almost free from high-order harmonics. This oscillator also generates the internal clock for the IC. Before starting the frequency measurement cycle, the 15-bits of data in the latch register, which represent the required local-oscillator frequency, are loaded into the frequency counter. Pulses from the prescaler then decrement the frequency counter for the duration of the measurement period.

The contents of the frequency counter at the end of the measurement period indicate whether or not the frequency of the local-oscillator in the tuner is the same as the desired frequency which was preloaded into the frequency counter. If the frequency counter contents is zero after the measurement period, a flag (FLOCK), which can be read by the microcomputer serial bus, is set to indicate that the local-oscillator is correctly tuned.

A frequency counter contents of other than zero at the end of the measurement period indicates that the tuner local-oscillator frequency is either too high (contents below zero) or too low (contents above zero). If it is too high, an overflow flag which initiates the "tuning down" function is set. To generate the tuning voltage correction, the tuning counter is loaded with the remaining contents of the frequency counter at the end of the measurement period, and then decremented to zero by an internal clock. The duration of the pulse applied to the charge pump is proportional to the time taken to decrement the tuning counter to zero, and therefore also proportional to the tuning error. The frequency correction has a resolution of 50 kHz.

The frequency measurement method of tuning used in the SAB3035 can also be easily combined with anologue a.f.c. to allow tracking of a drifting transmitter frequency within a limited range. The required tuning mode (with or without a.f.c.) is selected and controlled by software. By not testing some of the LSBs of the contents of the frequency counter, tune-in "windows" of ±100 kHz or ±200 kHz can be defined. The corresponding a.f.c. "windows" are ±400 kHz or ±800 kHz. The SAB3035 also contains the a.f.c. control logic and amplifier. To allow matching to a wide variety of tuners, the tuning loop gain and tuning speed can be adjusted over a wide range. To minimise sound-on picture, a "tuning hold" mode is selectable in which the charge pump and a.f.c. currents can be reduced when correct tuning has been achieved.

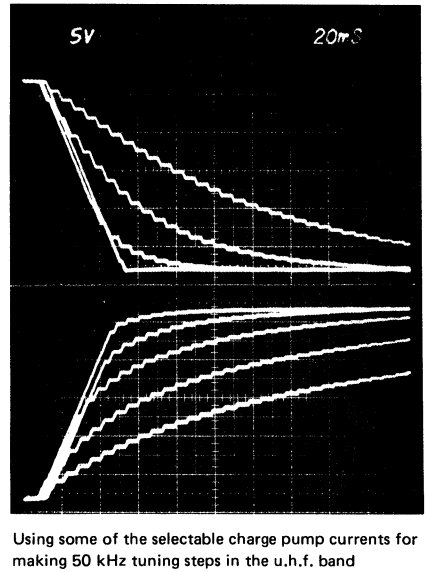


Fig.4 Using some of the selectable charge pump currents for making 50 kHz tuning steps in the u.h.f. band

decreasing frequency (top)
increasing frequency (bottom)

Bandswitching

The IC also incorporates four 50 mA current sources with outputs at ports P10 to P13 for executing band switching instructions from the microcomputer. Bandswitching data is stored in the data output register. The supply voltage for the current sources is derived from a separate input (V_{CC2}) and is therefore independent of the logic supply voltage (V_{CC1}).

I/O ports

There are four bidifectional ports P20 to P23 for additional control signals to or from the tv receiver. Typical examples of these additional controls are stereo/dual sound, search tuning and switching for external video sources. The output data for ports P20 to P23 is stored in the port data register. Input data must be present during the read cycle. Two of the inputs are edge-triggered. Each input signal transition is stored and can be read by the microcomputer via the serial data bus. The stored data is cleared after each read cycle.

Analogue controls

The SAB3035 includes eight static DACs for controlling analogue functions associated with the tv picture and sound (volume, tone, brightness, contrast, colour saturation etc,). External RC networks are not necessary to complete the D/A conversion. The control data for the DACs is derived from the serial data bus and stored in eight 6-bit latch registers. The output voltage range at DAC0 to DAC7 is 0.5 V to 10.5 V and can be adjusted in 64 increments.

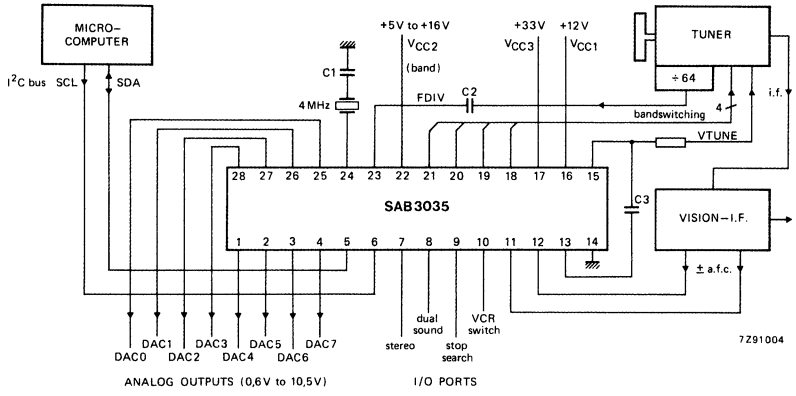


Fig.5 This typical example of the SAB3035 in a tv tuning and control system shows how the peripheral components have been reduced to three capacitors, a resistor and a 4 MHz crystal

9

ACKNOWLEDGEMENTS

Special thanks are due to F.A.v.d.Kerkhof and B.Strassenburg for their contributions, and to M.F.Geurts for the electrical design of the SAB3035.

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Features of the TDA2595 Synchronization Processor AN158

FEATURES

- Positive video input, capacitive coupled (source impedance $< 200\Omega$)
- Adaptive sync slicer at 50% of sync pulse amplitude
- Internal vertical pulse separator with double-slope integrator
- Outputstage for vertical sync pulse or composite sync depending on the load. Both are switched off by mute
- ϕ_1 phase control between H-sync and oscillator
- Coincidence detector ϕ_3 for automatic time-constant switching, overruled by the VCR-switch
- Time-constant switch between two external time-constants or loop-gain switch both controlled by coincidence detector ϕ_3
- ϕ_1 gating pulse controlled by coincidence detector ϕ_3
- Mute circuit depending on TV transmitter identification
- ϕ_2 phase control between line flyback and oscillator. The slicing levels for ϕ_2 control and line blanking can be set separately
- Burst keying and line blanking pulse generation, combined with clamping of field blanking pulse (triple-level sandcastle)
- H-drive output with constant duty cycle inhibited by the protection circuit or the supply voltage detector
- Detector for too low supply voltage
- Protection circuit switching off H-drive output continuously if input voltage is below 4V or higher than 8V
- Line flyback control causing line-blanking level at sandcastle output continuously in case of missing flyback pulse
- Spot-suppressor controlled by the line flyback control

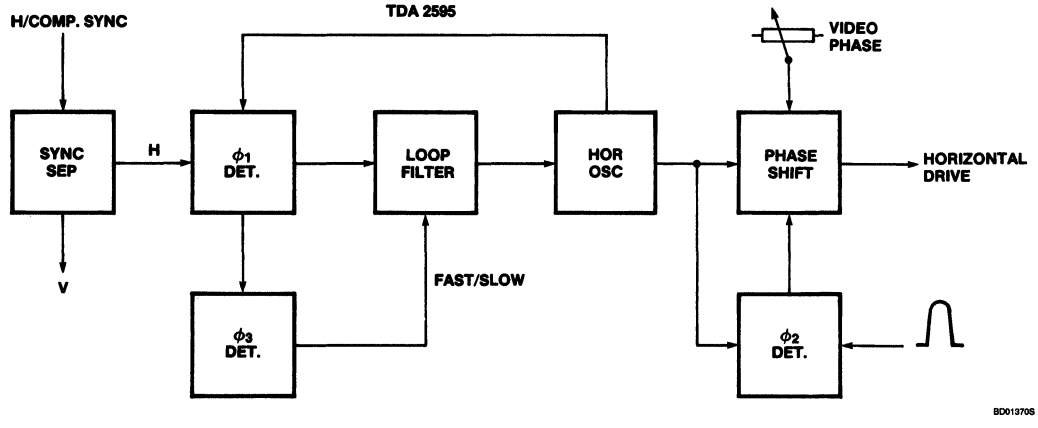

Figure 1

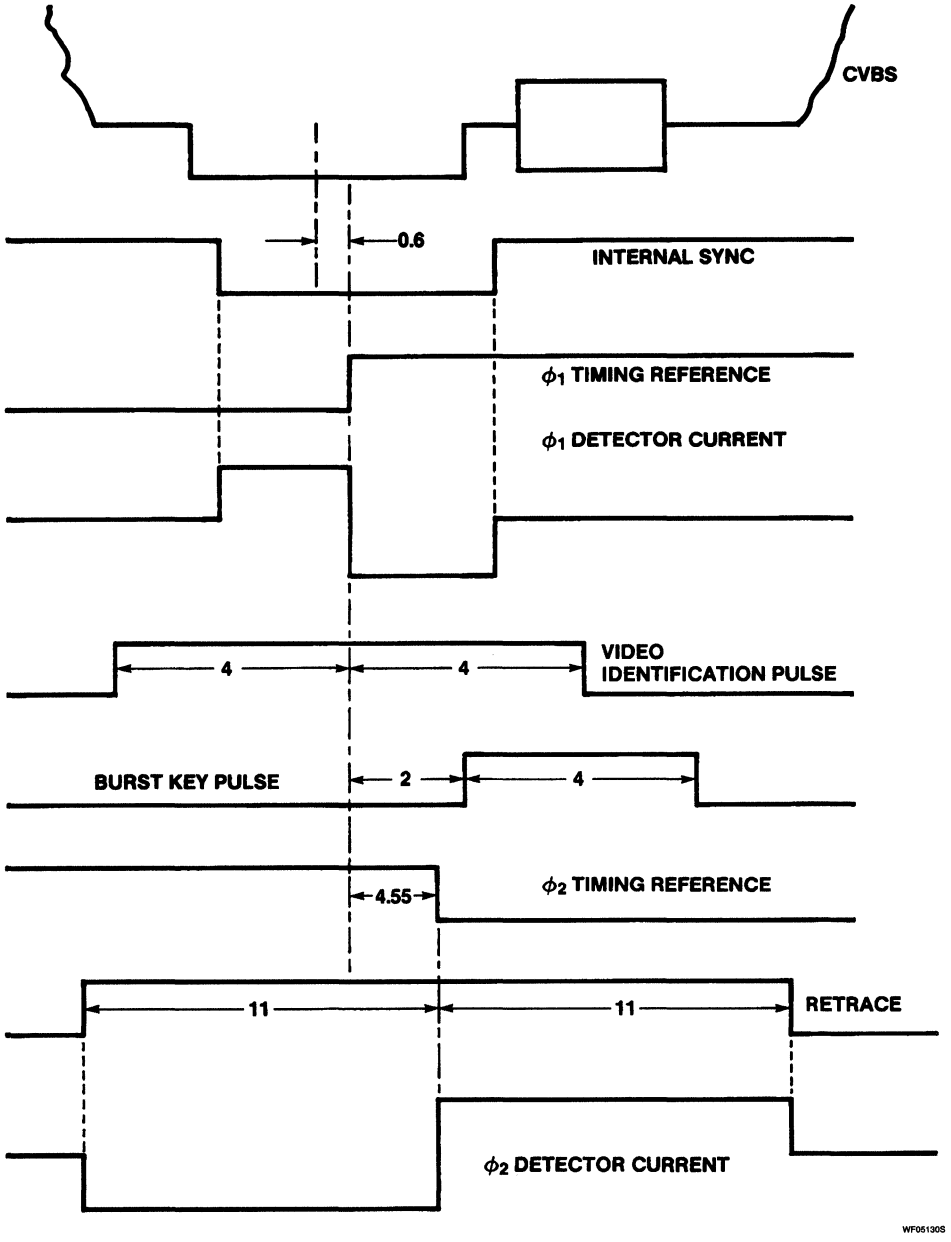

Figure 2. Timing Diagram

Features of the TDA2595 Synchronization Processor AN158

SYNC SEPARATOR

Adaptive sync separator to slice H-sync at 50% and V-sync at 25% independent on sync-amplitude. This is to insure immunity against deteriorated sync impulses. The black level is stored on a capacitor which is fed to the positive video-signal (source impedance 200Ω) into pin 11. The slicing level is detected internally and stored in a capacitor at pin 12.

The internal vertical integrator has a delay of 45μs and is of the double-slope type to avoid jitter and to improve noise immunity.

VERTICAL/COMPOSITE SYNC

The output stage at pin 9 delivers a positive vertical pulse or a positive composite sync signal if the current drain is higher than 3mA.

If no TV transmitter is detected, the output is switched to ground. The source impedance is low-ohmic.

15KHZ VCO

The VCO is a current controlled ramp oscillator with 49μs rise time and 15μs fall time. The timing capacitor is connected to pin 16; the control current has to be fed into pin 14.

While adjusting f_0, pin 12 should be connected to ground.

The oscillator generates the following signals (see timing diagram fig 2):

- timing reference for ϕ_1
- gating pulse for ϕ_1
- reference pulse for video identification circuit and coincidence detector ϕ_3
- burst keying pulse
- time reference for ϕ_2

ϕ_1 PHASE CONTROL

The phase control ϕ_1 compares the ϕ_1 timing reference of the VCO with the center of the H-sync signal and converts the time difference into a proportional current at pin 17.

The external low-pass filter at pin 17 determines the time constant and the catching and tracking range of the VCO.

If pin 18 is connected to the V+, the loop gain is increased 4 times as long as the oscillator is not locked in or pin 13 is connected to ground or V+ (VCR switch).

If pin 18 is connected as shown in the circuit diagram, pin 18 has the same voltage as pin 17 as long as the oscillator is not locked in or pin 13 is connected to ground. Due to this the "long" time constant connected from pin 18 to ground, ground is electrically disconnected from pin 17.

If the oscillator is locked in and pin 13 not connected to ground, pin 18 switches to high impedance and thus the loop filter to the "long" time-constant.

By switching loop gain or loop time-constant, the lock in condition of the oscillator is not disturbed. This enables a fast search tuning using the TV transmitter identification ($\overline{\text{mute}}$) as a search stop.

To increase noise immunity the phase detector is inhibited during horizontal retrace and vertical retrace if the oscillator is locked in and pin 13 not connected to ground or V+.

COINCIDENCE DETECTOR ϕ_3

The coincidence circuit detects whether there is coincidence between the H-sync pulse and a 8μs impulse generated by the VCO. The capacitor at pin 13 is discharged continuously by 8μs current pulses of 50=mμA. If there is coincidence, the capacitor is additionally charged by H-sync pulses of 350=mμA.

If the voltage at pin 13 exceeds 3V, the loop gain is reduced and the loop time constant is switched to the "long" value.

If the voltage exceeds 4.5V, the phase detector ϕ_1 is gated to improve noise immunity.

MUTE CIRCUIT

The mute circuit detects whether there is coincidence between the H-sync impulse and a 8μs impulse generated by the VCO. The capacitor at pin 12 is discharged during sync-pulses of 50=mμA and by 8μs current pulses of 50=mμA. If there is coincidence, the capacitor is additionally charged by H-sync pulses of 450=mμA.

If the voltage at pin 12 exceeds 4V, mute is released and the mute output at pin 7 is switched to high impedance. Although the coincidence detector ϕ_3 and the mute circuit act similarly, separate circuits have been chosen. This is to gain in design flexibility as far as the time constants are related and to keep the mute function alive independently on the VCR switch.

ϕ_2 PHASE CONTROL

The phase control ϕ_2 compares the center of the positive flyback pulse at pin 2 at a threshold of 3V with the ϕ_2 timing reference. The time difference is converted into a proportional current at pin 3. Loop gain and time-constant are influenced by the external components at pin 3. The voltage at pin 3 in turn controls the phase shift.

To achieve a small phase adjustment a small current may be injected into pin 3.

The aim of having two different thresholds at the flyback input is to determine the performance of the ϕ_2 loop, e.g. a straight vertical center line, by the amplitude of the applied flyback pulse without affecting the blanking time.

SUPER SANDCASTLE

For burst keying and vertical and horizontal blanking there is a 3 level pulse at pin 6.

The burst keying part is driven from the VCO and is 4μs wide. Due to its small tolerances in widths and phase it keys the burst very exactly and is suitable as black level clamping pulse.

The blanking part is derived from the line flyback pulse at pin 2 at a threshold of 0.2V. If no flyback is applied to pin 2, there will be continuous blanking level superimposed by the burst keying pulse.

The frame blanking part has to be fed in externally as a 2mA current.

HORIZONTAL DRIVE

The H-drive output is an open-collector output at pin 4. The output pulse has a constant aspect ratio of 45.3% off and 54.7% on dependent upon the line frequency. An internal guard logic insures that there will be high level during flyback. The output is inhibited by the protection circuit also if the supply voltage is below 4V. In both cases the line flyback vanishes and by this the spot suppressor is activated.

SPOT SUPPRESSOR

The spot suppressor is an open collector output at pin 1. If no flyback impulses are detected at pin 2, the output switches to high impedance and remains there as long as the flyback pulses are missing even if the supply voltage vanishes during that time.

PROTECTION CIRCUIT

The protection circuit is activated if the voltage at pin 8 exceeds 8V or decreases below 4V. One of both thresholds may be used (as indicated in Figures 4a and b) to have X-ray protection or over-current protection.

If activated, the H-drive is inhibited by this and the line flyback vanishes and in turn the spot suppressor is activated.

The protection circuit is reset if the supply voltage decreases below 4V e.g. the set is switched off.

Features of the TDA2595 Synchronization Processor AN158

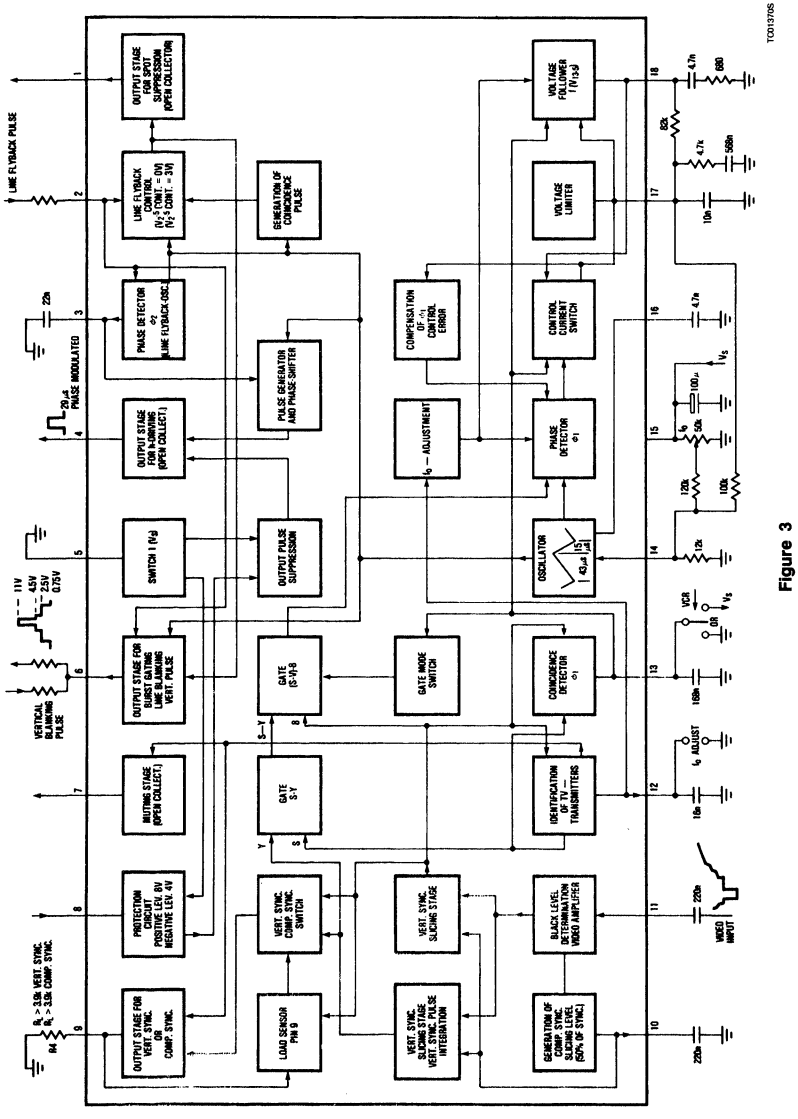

Figure 3

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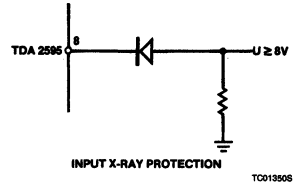


Figure 4a. Input X-ray Protection

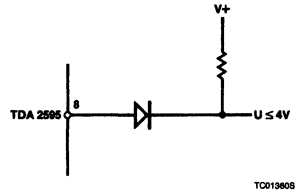


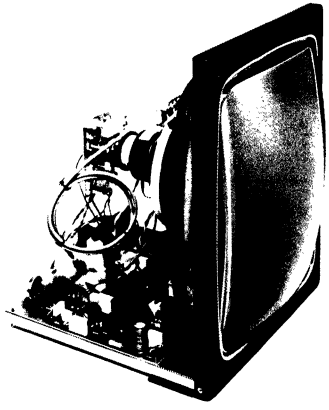
Figure 4b. Input Over Current Protection

Full-Page Display Using Television Components AN159

A full-page data-graphic display, with upwards of 5000 characters on an upright screen, puts severe demands on deflection, resolution, and raster geometry(Ref.). To meet those demands it has been usual to specify expensive monitor tubes and deflection components designed expressly for the purpose. Now, however, that is no longer necessary. The laboratory prototype shown in the photo more than satisfies the usual specifications for full-page display, and it does so with parts mainly derived from normal television practice.

The cathode-ray tube is a refinement of a black-and-white television tube, adapted to the requirements of data-graphic display. Its 38 cm diagonal screen is capable of displaying 10^6 pixels. The deflection assembly, though designed for the adapted tube, is constructed according to principles first developed for colour television. In addition, the line-driver, line-output, and picture-shift transformers are standard television parts, unaltered, as are the two integrated circuits used in the line and field timebase circuitry.

The use of television-derived technology benefits not only the cost and reliability of the display but also its size. Thanks to the 110° deflection angle, the 38 cm tube occupies no more depth than a 31 cm tube with 90° deflection. This and its television-style push-through mounting afford the designer more than ordinary latitude in the styling of an attractive, slim-line enclosure for a production version of the display.



Laboratory prototype full-page display. 110° deflection and push-through tube mounting afford generous styling latitude for a production version

PERFORMANCE SPECIFICATIONS

Table 1 lists the main specifications. The line and field deflection frequencies given there are for a non-interlaced raster of 1066 lines, just over 1000 of which are displayed. Non-interlacing precludes jitter, and at the 60 Hz field deflection frequency flicker is not a problem, even at the high brightness used with inverse video. Higher field frequencies may be used, as may an interlaced raster, but for thermal and other reasons the line deflection frequency should not exceed 64 kHz.

The prototype shown in the photo incorporates the elements to the right of the dashed line in the block diagram (Fig.1). The amplifier to the left of the line is required for video inputs at lower than TTL level. The power supply used with the prototype was a mains-isolated switched-mode supply operating at 30 kHz and stabilised against mains variations between 185 V and 225 V r.m.s.

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The excellent raster geometry of the display is due largely to the AT1039/00 deflection unit. Both the line and field deflection coils are saddle-type and are wound by the pin-indexed method in which each coil is divided into groups of turns that can be positioned to close tolerances. Since its introduction more than ten years ago to solve some of the electron-optical problems peculiar to 110° colour television, pin-indexed winding has gained wide acceptance and has opened the way to a number of improvements in deflection coil design. The AT1039/00 embodies one of the latest of these: 'flangeless' winding, in which the narrow end of each coil is not bent up into the usual flange but lies flat along the neck of the tube and is enclosed by the ferrite ring. The shape of the coils permits even closer control of their turns distribution, and their total enclosure by the ferrite ring prevents radiation of line and field frequencies. In a datagraphic display it also prevents ringing effects and the vertical bars that are often seen when a white page is displayed.

The electrical characteristics of the AT1039/00 coils are:
line deflection coil (parallel connected)

L = 0.23 mH R = 0.48 Ω

I = 6.18 A for edge-to-edge scan at 17 kV e.h.t.

field deflection coil (series connected)

L = 9.1 mH R = 10.1 Ω

I = 1.3 A for edge-to-edge scan at 17 kV e.h.t.

Built-in adjustable permanent magnets correct residual raster errors. No raster correction circuitry is required.

The AT1039/00 is for displays with upright page presentation. A unit with equivalent characteristics for horizontal page presentation is the AT1039/01; owing to the longer line scan, the line frequency with this unit is limited to about 32 kHz.

TABLE 1
Brief specification of the display

cathode-ray tube	M38-328
deflection unit	AT1039/00
line deflection frequency	64 kHz
line flyback time	3 μs
field deflection frequency	60 Hz
field flyback time	0.6 ms
e.h.t. voltage	17 kV
line linearity error	≤ 3%
field linearity error	≤ 3%
raster size variation ('breathing') for 0 to 100 μA beam current variation	1%
video bandwidth at 30 V input	60 MHz
sync inputs	positive-going composite sync or separate line and field sync at TTL level
supply	330 mA at 105 V 90 mA at 12 V

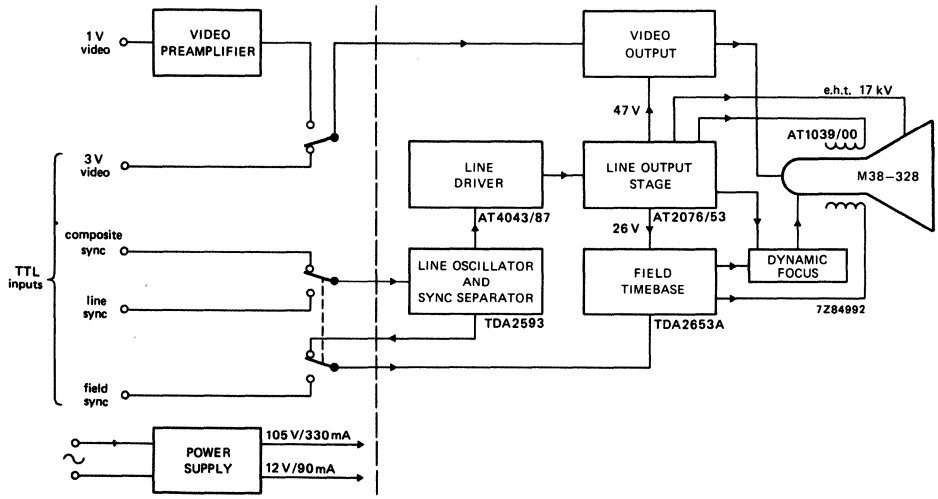

Fig.1 The photographed prototype includes the elements to the right of the dashed line

LINE OSCILLATOR AND LINE DRIVER

The TDA2593 in Fig.2 is a television IC that combines the functions of coincidence detector, sync separator, and line oscillator. Some functions provided for television are not used: for instance, a phase comparison loop for synchronising the oscillator voltage with the flyback pulse; the storage time of the line output transistor is sufficiently stable that there is no significant raster drift with respect to the video information during warm-up.

The AT4043/87 transformer that couples the line driver transistor to the line output stage is also a standard television part, chosen for the tight coupling between its windings. To minimise the effects of outside interference, particularly picture-tube flashover, the line driver is placed as close as possible to the line output transistor on the printed wiring board.

TABLE 2
Line driver stage operating conditions

supply voltage	105 V
supply current	40 mA
transformer voltage	63 V
transformer voltage ripple	3 V
peak collector voltage	150 V
peak collector current	120 mA

LINE OUTPUT STAGE

The line output stage (Fig.3) uses a parallel efficiency diode, as in television practice, with a 2.2 nF capacitor in parallel with the diode to give 3 μs flyback time. The small leakage inductance of the line driver transformer, aided by the speed-up capacitor and resistor in the base circuit, ensures suitable storage and zener times for correct turn-off of the transistor; the base-emitter resistor damps ringing of the base drive waveform.

The 220 nF capacitor in series with the AT1039/00 line deflection coil provides S correction. The AT4043/29 shift transformer and the potentiometer associated with it enable the raster to be centred laterally; the direction of shift can be reversed by reversing the connection of the flying lead shown dotted in the drawing. Since at the 64 kHz line fre-

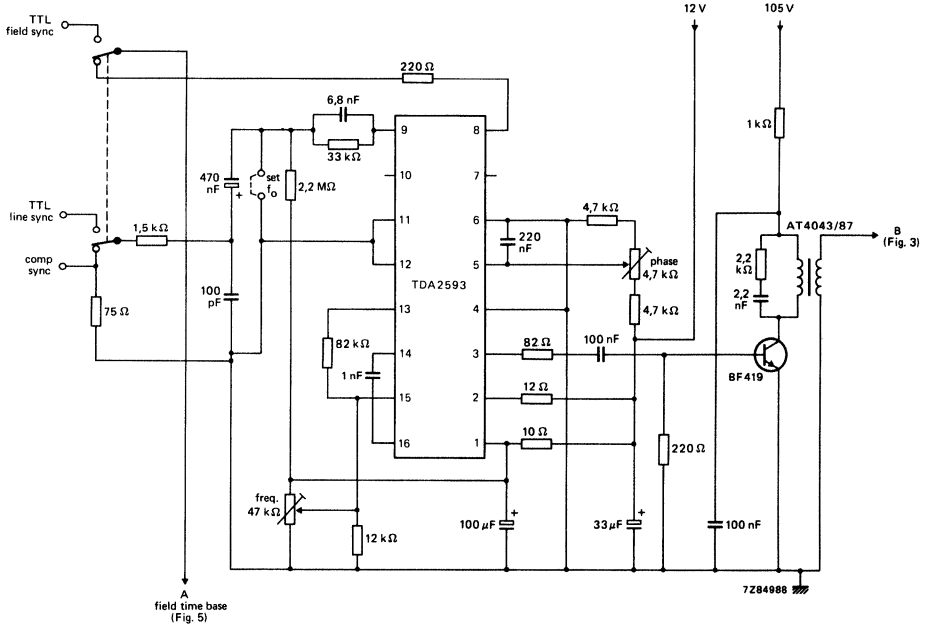

Fig.2 Line oscillator and line driver

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quency the resistance of the deflection coil is negligible compared with its impedance, no asymmetric linearity correction is required. Figure 4 shows the line-scan linearity.

Like a television receiver, the display obtains its e.h.t. and housekeeping voltages from a transformer driven by the line output stage. It is a type AT2076/53 'diode split' transformer intended for large-screen colour sets with 25 kV e.h.t. and 15.625 kHz line frequency. Although working here at slightly more than four times that frequency, it is quite capable of supplying 17 kV at the lower current required by the smaller, single-gun tube. Because of the very tight coupling between its primary and e.h.t. windings, the AT2076/53 can operate over a wide frequency range without distorting the line-scan waveforms. A harmonically tuned line output transformer, as used in some television receivers, would not be suitable.

The e.h.t. winding is in three layers connected by built-in diodes. The cable connecting it to the picture-tube anode incorporates a bleeder resistor to prevent raster width variation ('breathing') at low beam current.

Other windings supply 26 V for the field timebase, 47 V for the video amplifier, and −140 V for brightness (grid 1) and focus (grid 3) control potentiometers. Three turns of insulated wire on the core limb opposite the primary winding supply the heater.

The grid 2 potential is obtained by peak rectification of the line output transistor collector voltage. To ensure the best possible resolution, the maximum allowable grid 2 to grid 1 voltage is used: 700 V. The upper end of the voltage divider containing the focus control potentiometer is also connected to this voltage to provide for positive as well as negative control voltages.

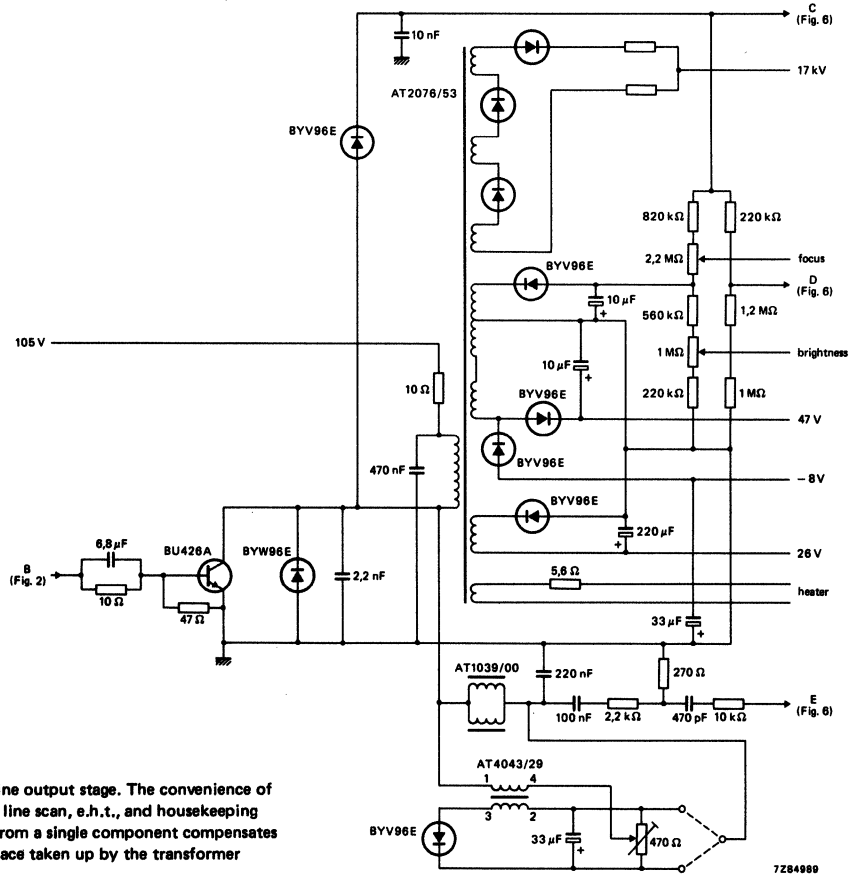

Fig.14 Line output stage. The convenience of obtaining line scan, e.h.t., and housekeeping voltages from a single component compensates for the space taken up by the transformer

TABLE 3
Line output stage operating conditions

supply voltage	105 V
supply current	290 mA
supply voltage ripple, 64 kHz	1 V
100 Hz	0.1 V
peak collector current	3.2 A
peak collector voltage	720 V
base current at end of scan	0.6 A
reverse base-emitter voltage	3 V
deflection coil current, peak-to-peak	6 A
scan-width/screen-width ratio	87 %

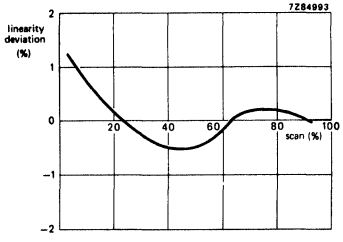

Fig.4 Line-scan linearity

FIELD TIMEBASE AND WAVE-SHAPING CIRCUIT

The TDA2653A field timebase circuit (Fig.5) is another television IC. It can accept separate sync pulses at TTL level or pulses obtained from a composite sync input by the sync separator of the TDA2593 in the line oscillator circuit. For interlaced operation, separate line and field sync pulses are recommended.

The TDA2653A has a class B output stage and thermal and short-circuit protection.

The wave-shaping circuit integrates the sawtooth voltage across the feedback resistor R to produce a positive-going field-frequency parabola for dynamic focus.

TABLE 4
Field timebase operating conditions

supply voltage	26 V
supply current	232 mA
deflection coil current, p-p	1.25 A
flyback time	0.6 ms
pin 5 voltage	25 V
pin 5 voltage ripple	2 V

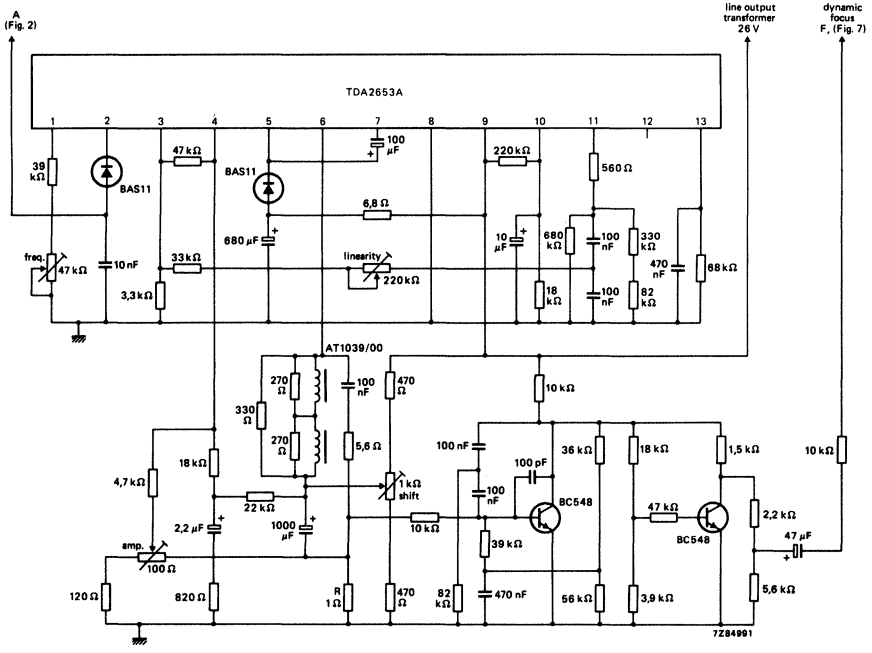

Fig.5 Field timebase and wave-shaping circuit

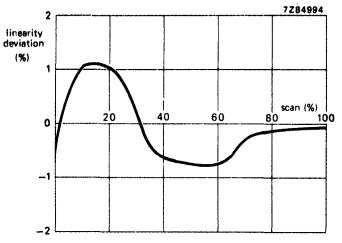

Fig.6 Field-scan linearity

VIDEO AMPLIFIER AND DYNAMIC FOCUS

The video amplifier (Fig.6) requires an input of about 4 V for a maximum output of 30 V. The small load resistance and peaking coil in the output transistor collector circuit, together with some compensation in the emitter circuit, ensure a bandwidth of 60 MHz. No provision is made for blanking; if it is required, it can be introduced in the logic circuits, as part of the video information.

Although the design of the deflection coils minimises deflection defocusing, there is some residual error. To correct it, line and field-frequency parabolas of about 250 V each are superimposed on the grid 4 focus voltage. The dynamic focus circuit uses two transistors in series to accommodate the 500 V excursion that occurs when the field-frequency parabola is maximum. Because the tube has a unipotential electron gun, the focus characteristic is fairly flat and it is unnecessary to provide for separate adjustment of the dynamic focus.

TABLE 5
Dynamic focus operating conditions

supply voltage	730 V
supply current	3.2 mA
input voltage, line frequency, p-p	5 V
input voltage, field frequency, p-p	5 V
output voltage, line frequency, p-p	250 V
output voltage, field frequency, p-p	250 V

CONSTRUCTION

Complete details of construction, setting up, and adjustment, together with a parts list and oscillograms of waveforms at all significant points, are available as a separate publication: Technical Publication M81-0084 from Mullard Ltd., Mitcham, England; or Technical Publication 026 from N.V. Philips', Electronic Components and Materials Division, Eindhoven, The Netherlands.

REFERENCE

'Cathode-ray tube requirements for data-graphic displays' Electronic Components and Applications, Vol. 4 No. 1, Nov. 1981.

ACKNOWLEDGEMENT

This article is based on the work of D. J. Gent of Mullard Application Laboratory, Mitcham, as more fully reported in the publication cited under 'Construction'.

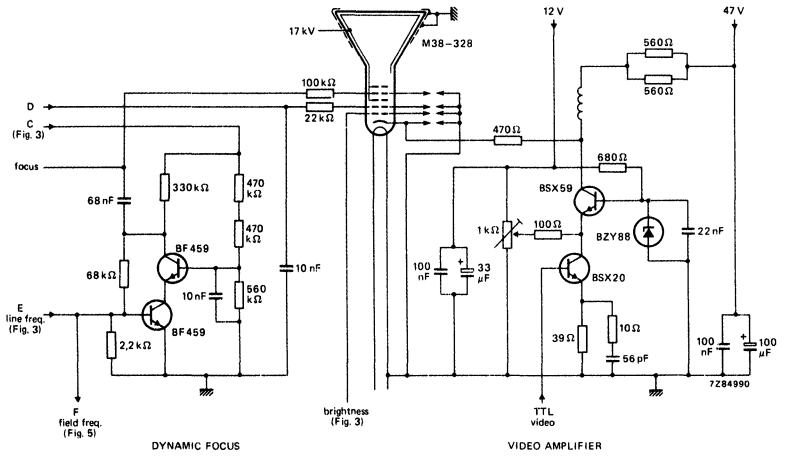

Fig.7 Video amplifier and dynamic focus

A Very-High-Resolution Monochrome Data and Graphics Display Unit

AN161

INTRODUCTION

The Data and Graphics Display (DGD) unit (also referred to as a VDU) is for specialist applications such as communications, medicine, and printing. Its uses include facsimile, phototypesetting, CAD graphics, and full-page word processor systems. It consists of a very-high-resolution CRT paired with precision deflection coils and all the associated display circuitry, as shown in Figure 1.

The picture tube/deflection coil combination, type M38-201, provides a high-quality display. Resolutions in excess of 3000 lines can be achieved with remarkably little deflection defocusing at the screen corners. The accurate geometry of the display is produced automatically without any need for external field shaping magnets. The small deflection angle (70°) requires modest scanning power. This allows operation at the high scanning frequencies necessary to fully utilize the resolution capabilities of the tube with a complete absence of flicker.

The monitor described is merely one example of the many possible applications of the M38-201 picture tube/deflection coil combination. It operates at a line frequency of 125 kHz, a field frequency of 100 Hz, a video dot rate of 288 Mbits, and a 100 MHz video bandwidth. Interlaced or non-interlaced operation is possible. When interlaced, it can display 1728 pixels per line and 2300 lines, thus meeting the CCITT Group III standard for digital facsimile. As such it offers a display capability of 4 million pixels or a minimum of 8000 complex characters (including Roman and subscripted) in full detail. Various display formats may be used. One example is a display of moderate character density with a large number of pixels per character. This allows the production of letter fonts as used in the printing industry and covers the requirements of various languages, special signs, and mathematical symbols.

Conventional techniques are used in the monitor design. Both line scan and e.h.t. are derived from a diode-split transformer, type AT2076/54. The line deflection coils are connected in parallel and directly driven.

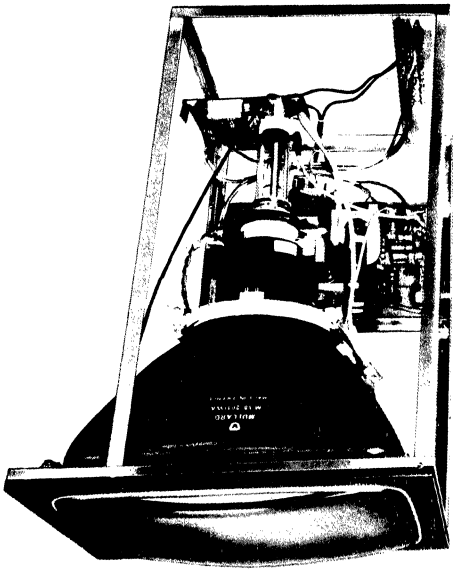

Figure 1. C52 DGD Unit

Dynamic focus, to provide optimum focus over the whole raster, is applied in both the line and field directions. E.H.T. regulation and minimum picture breathing (change in picture width with beam current) are ensured by modulating the flyback time with changes in picture tube beam current.

The unit will accept ECL level video input and separate positive-going line and field sync at TTL levels. It requires 5 V and 118 V stabilized d.c. supplies and has a total power consumption of 52 W.

Note: e.h.t stands for *extreme haûte-tension*, or extreme high voltage.

GENERAL DESCRIPTION

A block diagram of the DGD is shown in Figure 2. The circuit diagram is shown in Figure 3.

Picture Tube and Coils

The normal DGD requirements of good raster geometry with minimal loss of display quality between the screen center and corners are even more important in high-definition systems. To ensure a display offering the best possible presentation of information over the whole screen, the unit uses the very-high-quality, purpose-designed picture tube/deflection coil combination M38-201. This consists of the picture tube, type M38-200, and deflection coils, type AT1991.

The M38-200 picture tube has a 70° deflection angle and contains a bi-potential electron gun requiring a focus voltage of around 6 kV and an 800 V grid 2 potential; it is capable of resolving more than 3000 lines. It is available in a variety of phosphors including the WA type which gives a warmer white than the standard monochrome TV W phosphor and is considered more suitable for data display applications.

The AT1991 deflection coils give excellent deflection performance and raster geometry with no need for external raster correction. Terminations for each coil are brought out separately to allow for either series or parallel connections. The active dynamic focus circuit applies parabolic correction in both the line and field directions, and gives precise focus over the whole raster.

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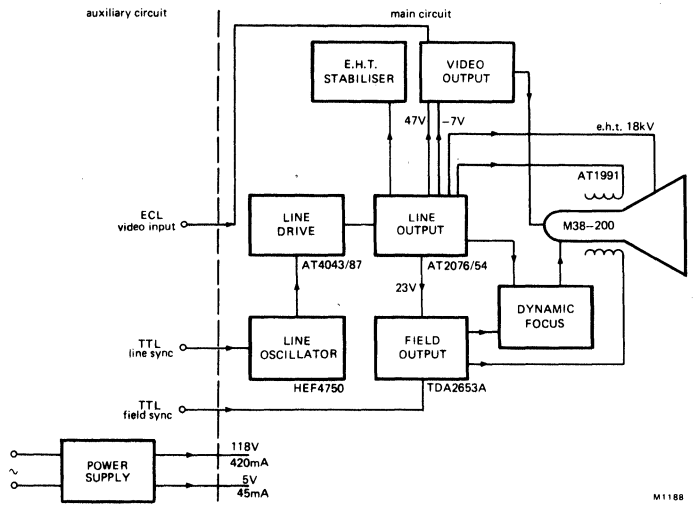

Figure 2. DGD Unit Block Diagram

Line Circuitry

The line output stage consists of transformer T1, type AT2076/54, transistor TR3 and parallel efficiency diode D2. The line drive is provided by transistor TR2 and driver transformer T4, type AT4043/87. Frequency synthesiser IC, type HEF4750, is used as line oscillator and coincidence detector.

Both line scanning and e.h.t. are provided by a diode-split line output transformer, T1. Although it has tight overwind-to-primary coupling it must be harmonically tuned. This is due to the very high operating frequency (and hence short flyback time) of the unit, and is accomplished by a small adjustable inductor, L1 in series with the h.t. supply. Transformer T1 also provides all the picture tube supply requirements and the h.t. for both the video and field output stages.

The line drive is supplied via transformer T4, which together with the speed-up capacitor C18 and its parallel resistor R23 provide the short storage and adequate zener times necessary to turn off the line output transistor TR3. Any ringing of the base drive waveforms, which might otherwise cause spurious turn-on, is damped by base-emitter resistor R23.

For systems operating at these very high line frequencies and data rates, the line phase jitter must be much less than 1 pixel duration. To meet this requirement, frequency synthesiser IC, type HEF4750 is used with an LC-tuned voltage-controlled oscillator. This IC contains a phase modulator, which is used for phase detection, with an adjustment for fine phase control. Phase comparison is made between the leading edges of the line flyback and line sync pulses. In the design shown, sync and blanking pulses are coincident but different phase positions can be accomodated by using a different value of integrating resistor R18.

Dynamic Focus

Parabolic dynamic focus is applied in both the line and field directions. The input for the line dynamic focus is taken directly from across S-correction capacitor, C29. For field frequencies, a parabolic waveform is obtained by integrating the sawtooth waveform across resistor R57. The same amplifier is used for both frequencies.

E.H.T. Stabilization

In displays containing large areas of both high and low beam currents, for example a white block in the center of a black raster, e.h.t. stabilization is particularly important. Any e.h.t. 'sagging' would produce a gradual change in the width of the displayed block.

To prevent this e.h.t. sagging and to obtain minimum picture breathing, an e.h.t. stabilization circuit is provided. The saturable transformer T2 is placed in parallel with the line deflection coil, its inductance being controlled by the picture-tube beam current. An increase in beam current produces a reduction in the inductance of T2 and a corresponding reduction in the flyback time. The increase in e.h.t., produced by the flyback time reduction, compensates for e.h.t. sagging due to the internal impedance of the e.h.t. generator. This provides an internal e.h.t. impedance of about 200 kΩ.

Field Timebase

All the field timebase functions are performed by the TDA2653A IC and its associated peripheral networks. This IC contains a class B output stage, incorporating thermal and short-circuit protection, which drives the AT1991 series-connected field coils. A field blanking pulse is available for screen-burn protection. The IC is contained in a 13-lead DIL plastic power encapsulation, SOT-141, which offers straightforward heatsinking.

Video Amplifier

The large number of displayed pixels and the high refresh rate needed to avoid picture flicker, mean that video dot rates in excess of 200 MHz are required. This is conveniently provided by an ECL logic unit "scanning" the contents of a semiconductor page memory. Thus, an ECL line receiver at the video amplifier input is used as an interface. The basic output stage consists of a long-tailed pair, using medium-power u.h.f. transistors TR11 and TR12, driven by the complementary outputs of the ECL device. To simplify the interface between the video amplifier output and the CRT cathode, the whole video amplifier is mounted directly on the tube base.

General Considerations

Picture-tube flashover protection for the circuitry is included. Spark gaps for all picture-tube pins are provided, and all are returned to a single point which is, in turn,

A Very-High-Resolution Monochrome Data and Graphics Display Unit

connected to the outside aguadag layer of the tube and the common earth point of the unit.

To achieve a satisfactory stable display with good linearity and no undesirable modulation, well recognized procedures should be adopted with regard to printed-circuit board layout. It is essential that each individual circuit block has its own grounding system connected to a central point on the main printed-circuit board which is, in turn, connected to the chassis. Circuit layout within the individual blocks may also be critical. For this reason printed-circuit cards and overlay diagrams are available for this design.

Table 1. DGD Unit Specifications

Picture tube		M38-200 15 in, 70°
Deflection coils		AT1991
Character display		4 X 10^6 pixels
Line frequency interlaced		125 kHz
Line flyback		1.6 μs
Field frequency		100 Hz
Field flyback		0.6 ms
E.H.T.		18 kV
Line linearity		better than 3%
Field linearity		better than 3%
Raster breathing	(0-100 μA)	better than 1%
Video rise time		<3.5 ns at 30 V pk-pk
Input signals		positive-going line sync at TTL level, positive-going field sync at TTL level, video at ECL level
Power input		52 W total 118 V d.c. at 400 mA 5 V d.c. at 40 mA

Originally published as "Technical Publication 136," EICOMA, The Netherlands, 1984.

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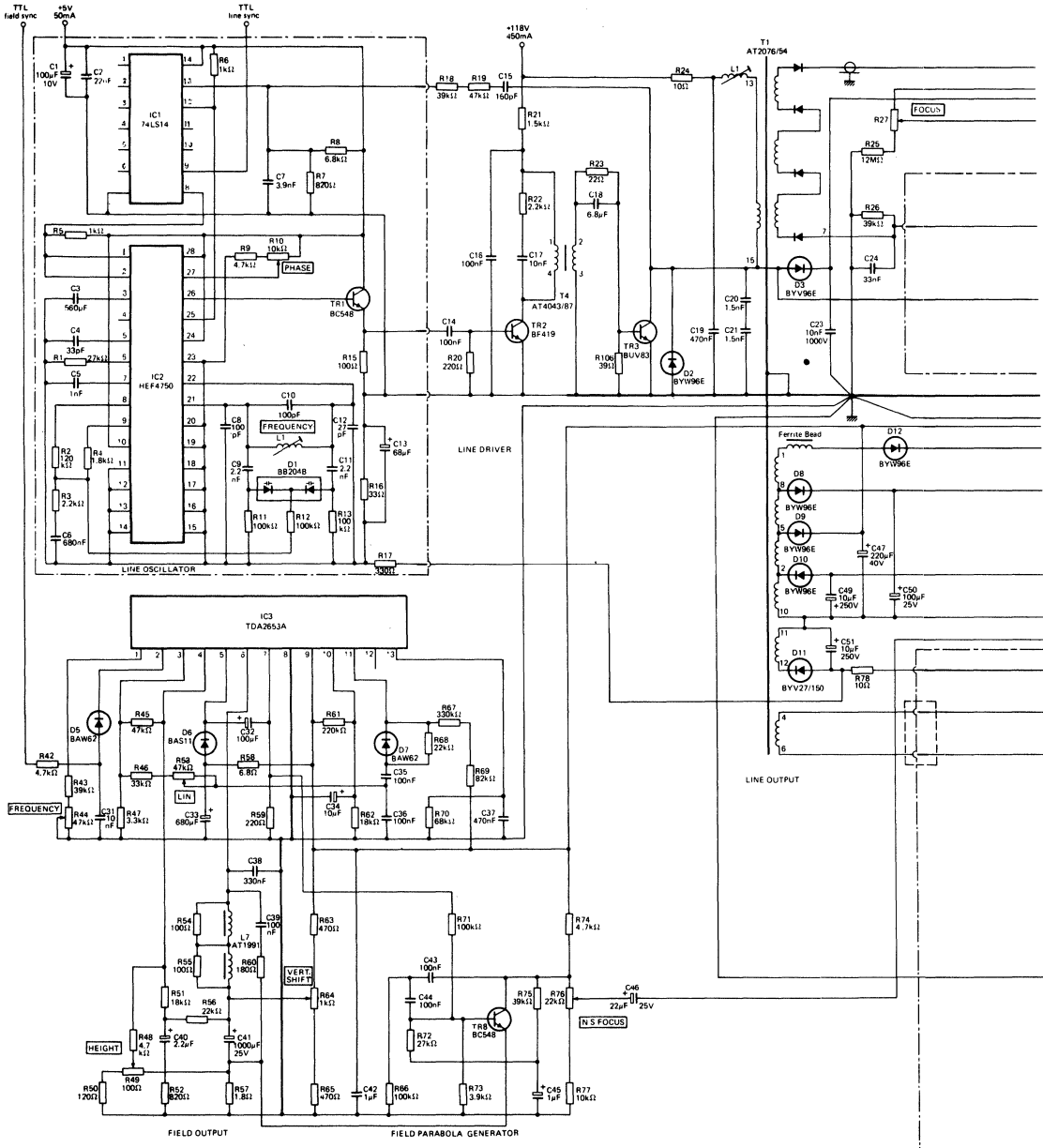

Figure 3. DGD Unit Circuit Diagram

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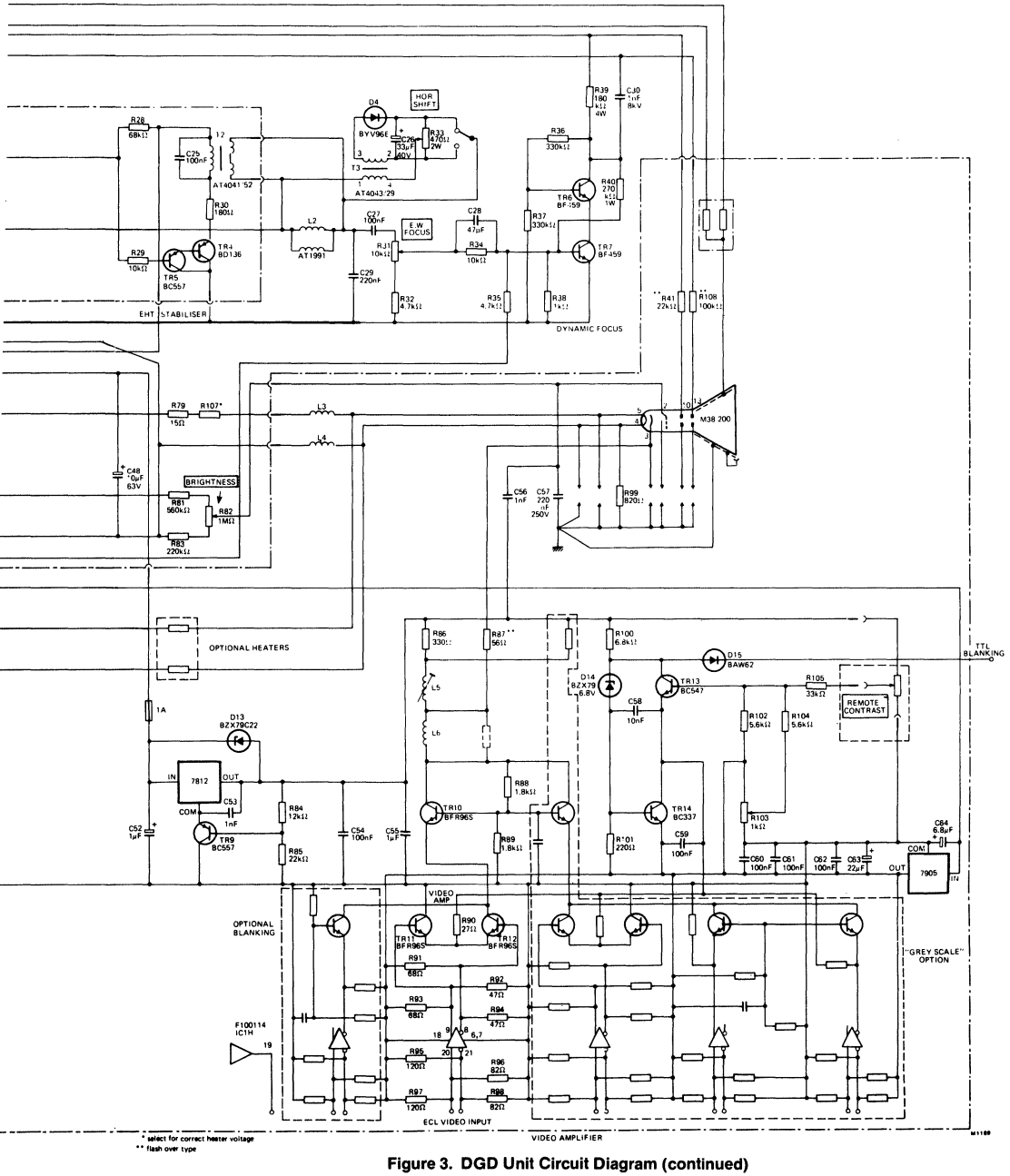

Figure 3. DGD Unit Circuit Diagram (continued)

A Versatile High-Resolution Monochrome Data and Graphics Display Unit

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INTRODUCTION

The Data and Graphics Display (DGD) unit (also referred to as a VDU) is built for wide ranging applications. It consists of a very high resolution c.r.t. paired with precision deflection coils and all the associated display circuitry, as shown in Figure 1. Using the same printed circuit board and components, it can easily be adapted to operate over a wide range of line and field frequencies with different flyback times in either horizontal (landscape) or vertical (portrait) format.

The possible applications of this unit range from video games to high-resolution displays. However, it is as a computer terminal display device that the DGD will be most useful. Normally, it is the logic design that determines all the parameters to be specified in a computer system, and it is only when the logic circuitry has been finalized that a suitable display is sought. Consequently, the display must be tailor-made for the application. There are no signs of any standardization in the future. For this reason the DGD has been designed to allow different dedicated display units to be built up very simply from one basic design.

The DGD is a straightforward and efficient design which will operate with line frequencies of between 15 and 70 kHz and field frequencies of 50 to 100 Hz, interlaced or non-interlaced. All the design features combine to provide the resolution required for very high density displays (up to 1.5 million picture elements per page). They also ensure a sharp picture right to the screen corners, and allow operation at high line frequencies without undue temperature rise. A diode-split transformer provides combined line scan and e.h.t., and it is this component which allows changes in line frequency and flyback time to be accomplished very easily.

Note: e.h.t stands for *extreme haute-tension*, or extreme high voltage.

GENERAL DESCRIPTION

Figure 2 shows a block diagram of the DGD unit and its auxiliary circuits. (The unit is to the right of the broken line, with the auxiliary circuits to the left.) The circuit diagram is shown in Figure 3.

The normal DGD requirements of good raster geometry and minimal loss of display quality between the screen center and corners are even more important in high-definition systems. To ensure a display offering the best possible resolution over the whole line frequency range, the unit uses high-quality purpose-designed deflection coils type AT1039. These are paired with either the 12 in (M31-326) or 15 in (M38-328) picture tubes. These coils have been designed using recently developed techniques to give good deflection performance and raster geometry suitable for correction by built-in magnets. For the 12 in tube, type AT1039/03 deflection coils are used. Two types of coil are available for the 15 in tube, the AT1039/00 which has been optimized for portrait (vertical) formats and the AT1039/01 for landscape (horizontal) displays. Terminations to each coil are brought out separately to allow for both series and parallel connections.

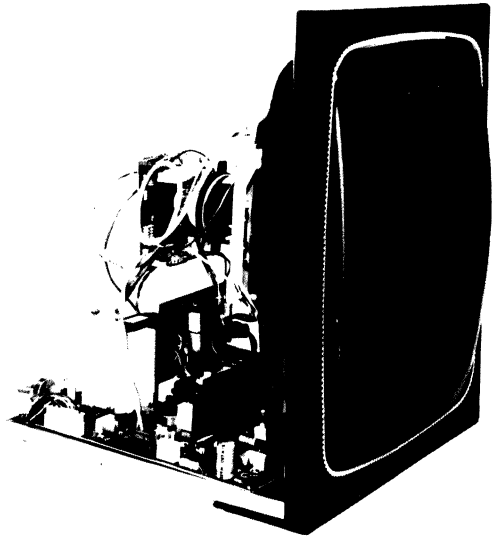

Figure 1. DGD Unit

Both line scanning and e.h.t. are provided by a purpose-built diode-split transformer. It is the flexibility of this device which produces the extreme versatility of the DGD unit as a whole and allows operation of the wide range of line frequencies and flyback times. In addition, all auxiliary power supply requirements are obtained from the same transformer. The primary is provided with several taps, each of which corresponds to a different peak voltage and hence flyback time. By careful positioning of these transformer primary taps, and by utilizing both parallel and series connection of the line deflection coils, a wide variety of flyback times can be accomodated in steps. Each step allows sensible values of flyback ratio for the different line frequencies. Apart from the selection of the correct transformer tap, the only other components that may need to be changed in order to use a different line frequency are the oscillator timing capacitor C6, S-correction capacitor C22, base drive resistor R52, linearity control L1, and heater resistor R84.

Although deflection defocusing has been minimized by careful design of the line deflection coils, there is still some focusing action in the deflection process. Also, there is a difference between the electron beam path lengths for axial beams and those deflected to the tube corners. These effects combine to produce a change in focus requirements from the center to the edges of the picture tube. To overcome this, dynamic focus is employed, The

A Versatile High-Resolution Monochrome Data and Graphics Display Unit

AN162

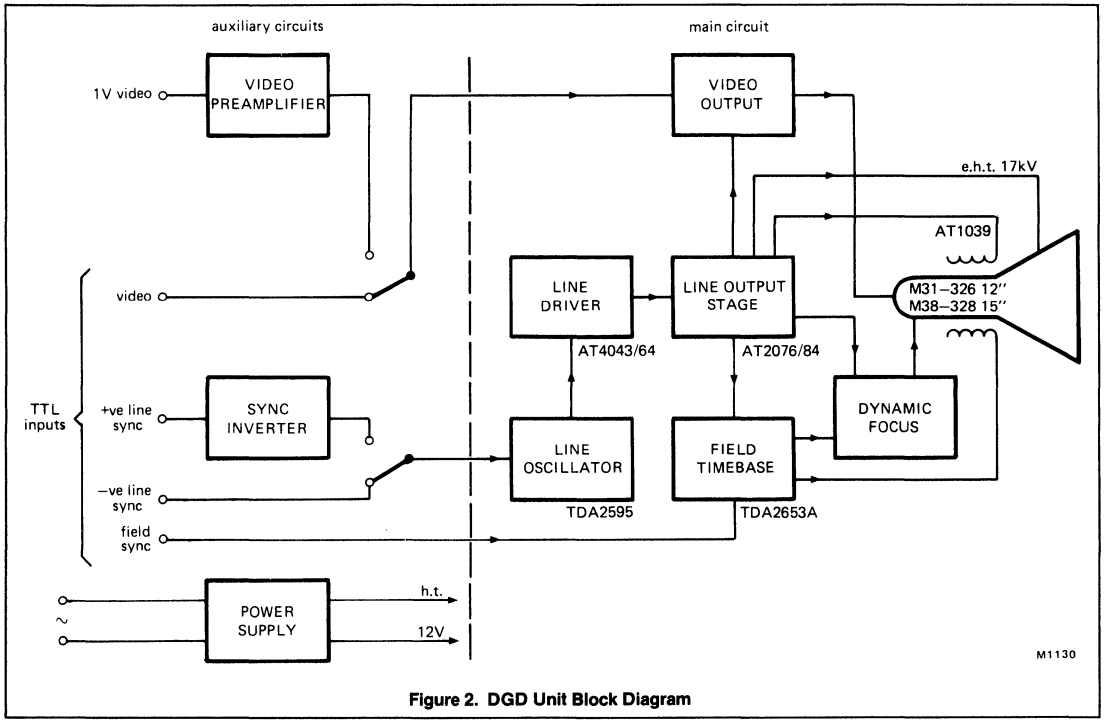

Figure 2. DGD Unit Block Diagram

active dynamic focus circuit applies parabolic correction in both the line and field directions to give precise focus over the whole raster. Because the electron gun is a unipotential type, the tube has a fairly flat focus characteristic. The amplitude of the dynamic focus can therefore be preset and adjustment is unnecessary.

Width control is accomplished with a series-parallel inductance arrangement which does not affect the flyback time or e.h.t. Adjustable picture shift is supplied in both the line and field directions by passing d.c. through the appropriate deflection coils.

The TDA2595 line oscillator combination IC provides the correct waveforms to drive the line output transistor via a transformer-coupled driver stage. This IC includes both the line oscillator and coincidence detector; a line flyback pulse, obtained from the collector of the line output transistor TR2, is required for phase detection. A protection circuit which turns off the output drive if the voltage at pin 8 is either below 4 or above 8 V is used to provide overvoltage protection for the line output stage.

All the field timebase functions are controlled by the TDA2653A IC. It takes a positive-going field sync input at TTL level and drives the impedance-matched AT-1039 deflection coils in series connection. A field blanking pulse, which may be used for screen burn protection, is available from pin 2. The IC is contained in a 13-lead DIL plastic power encapsulation type SOT-141, which offers straightforward heatsinking.

An emitter-driven video output stage is used with output transistor TR6 and driver TR7. The collector load resistors R87 and R88 with peaking coil L5 and some compensation in the emitter circuit ensure a bandwidth of 60 MHz at 35 V, measured at the cathode. In order to minimize stray capacitance, the video amplifier is placed on the tube-base printed circuit board close to the cathode pin of the tube. The 55 V h.t. line is provided from the line output stage.

The unit will accept video input at TTL level with positive-going field sync and negative-going line sync. However, inputs at other levels and polarities may be accepted by using the auxiliary circuits, as shown in Figure 2.

The main h.t. line input will depend upon the line frequency and varies from about 30 to 150 V. If lower values of h.t. are preferred, a floating tap will accomodate a series boosted circuit arrangement.

A 12 V supply is required at all frequencies. The total power consumption of the unit is about 40 W.

Standard measures are taken to protect the circuitry in the event of a picture tube flashover. Spark gaps for all picture tube pins are provided and all are returned to a single point which is, in turn, connected to the outside aquadag layer of the tube and the common earth point.

To achieve a satisfactory stable display with good linearity and one that is free from undesirable modulation, well recognized procedures should be adopted with regard to printed circuit board layout. It is essential that each individual circuit block has its own grounding system connected to a central point on the main printed circuit board which is, in turn, connected to the chassis. Circuit layout within the individual blocks may also be critical. For this reason printed circuit cards and overlay diagrams are available for this design.

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A Versatile High-Resolution Monochrome Data and Graphics Display Unit

AN162

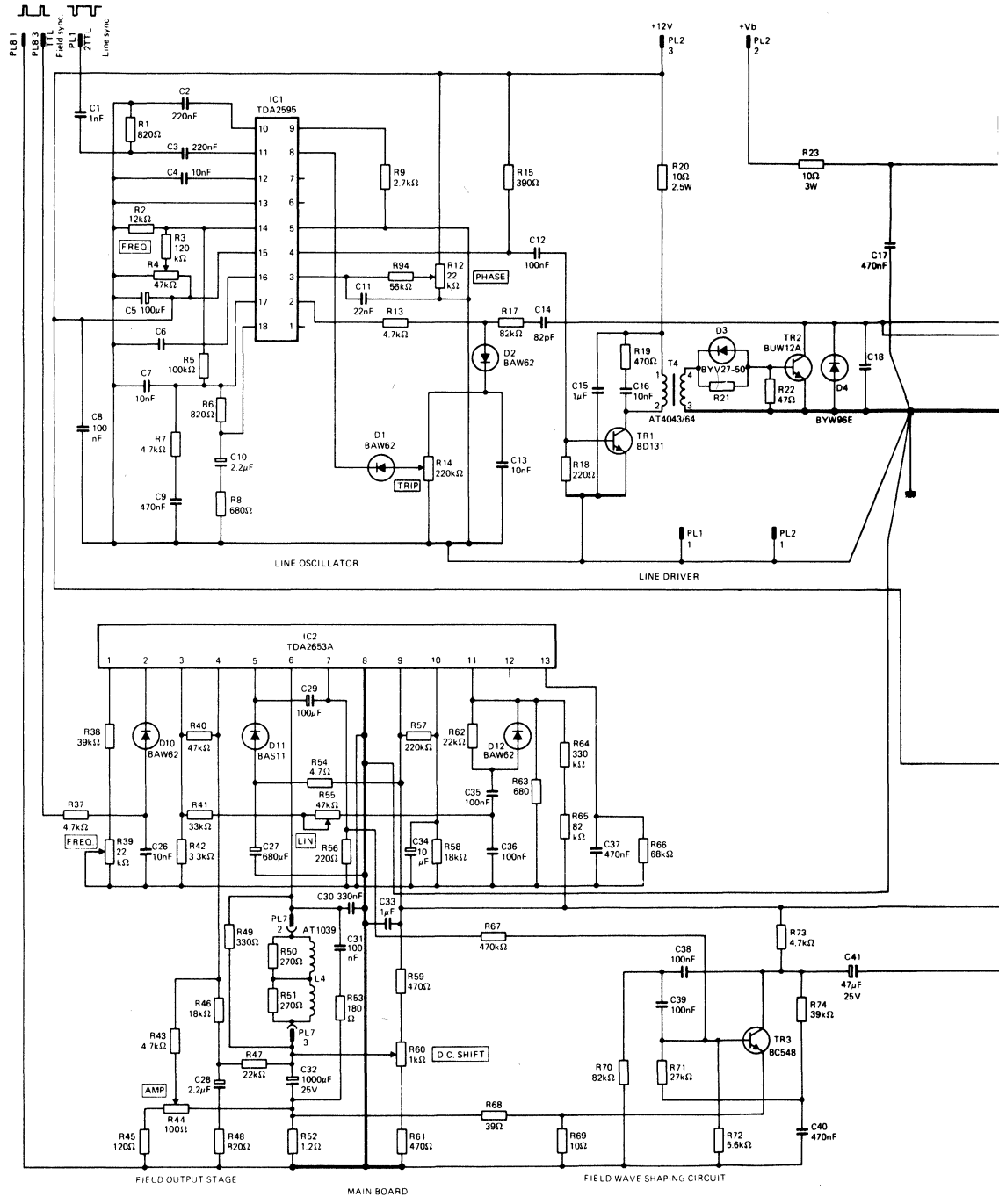

Figure 3. DGD Unit Circuit Diagram

A Versatile High-Resolution Monochrome Data and Graphics Display Unit

AN162

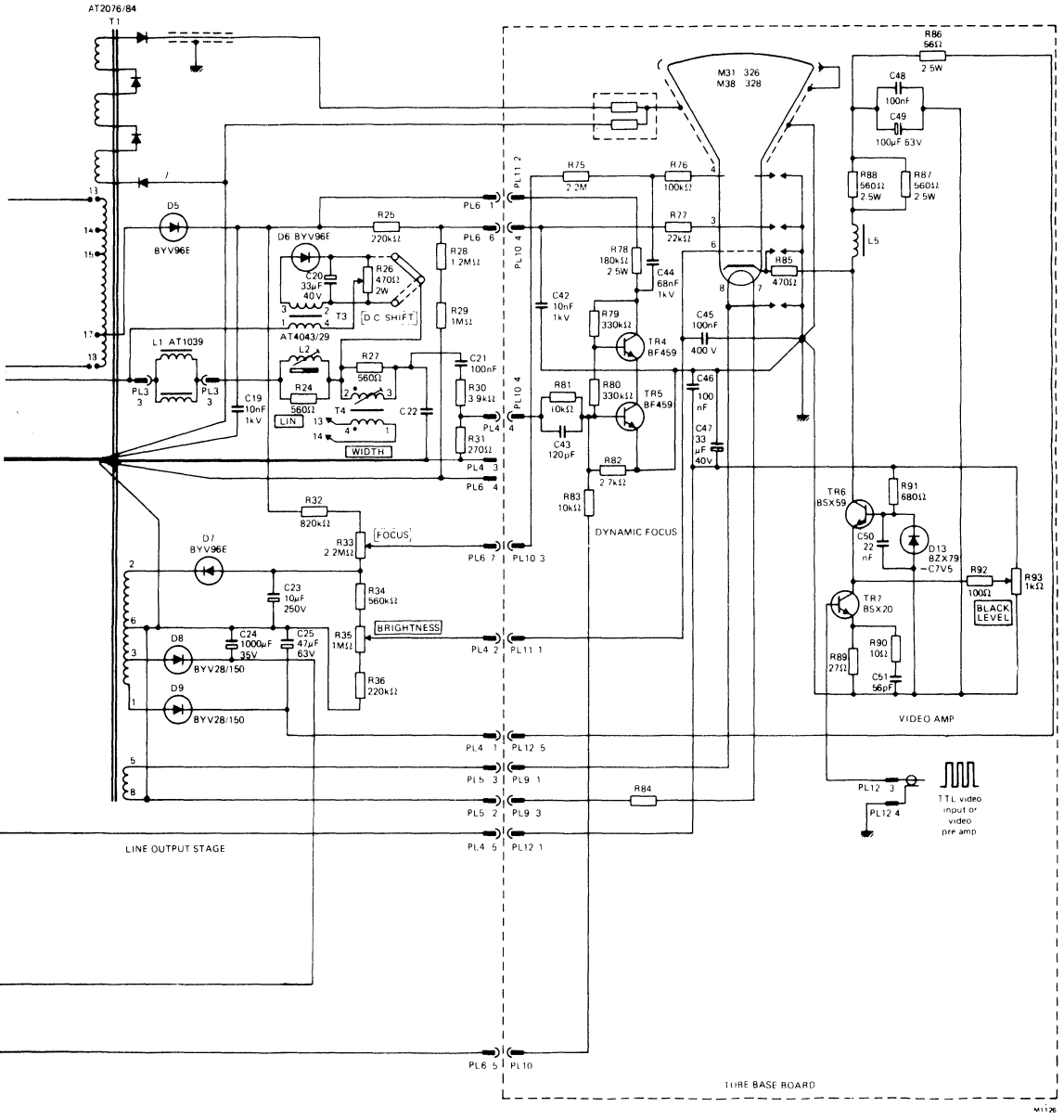

Figure 3. DGD Unit Circuit Diagram (continued)

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A Versatile High-Resolution Monochrome Data and Graphics Display Unit

Table 1. DGD Unit Specifications

Picture tube	12 in M31-326 series 15 in M38-328 series
Deflection coils	AT1039 series
Line output transformer	AT2076/84
Character display	up to 1.5 X 10^6 pixels
Line frequency landscape format portrait format	 15 to 50 kHz 15 to 70 kHz
Field frequency non-interlaced or interlaced	 50 to 100 Hz
E.H.T.	17 kV
Line linearity	better than 3%
Field linearity	better than 3%
Raster breathing (0 to 100 μA)	 better than 2%
Line flyback time	3 to 9 μs
Field flyback time	0.6 ms
Video bandwidth (at 35 V output measured at the cathode)	 60 MHz
Input signals	positive field sync at TTL level, negative line sync at TTL level, video input at TTL level
Power input	40 W total 30 to 150 V 36 W 12 V 4 W

Originally published as "Technical Publication 115," ELCOMA, The Netherlands, 1983.

SO Package Tape and Reel AN210

Integrated Circuits packaged and shipped in Tape and Reel will significantly alter the production methods of the US electronics industry. SO packages are now available in 12mm, 16mm, and 24mm tapes depending on the size of the package.

Tape and Reel will enable manufacturers to use very high speed automatic placement equipment. With reels containing 1000 or 2000 components each, this equipment can run at high speed for longer periods without stopping the machine to replace empty tubes. Further, the components packaged in Tape and Reel require much less storage space than those in the traditional tubes. For example, the SMD Technology Center in Milwaukee, WI saved over 90% in storage area for 5,000,000 SMDs in Tape and Reel vs. the space it would have required for the traditional axial leaded parts in tubes and/or reels.

SPECIFICATIONS

Tape and Reel specifications conform to Electronic Industries Association (EIA) Proposed Specification #RS-481 A, "Taping of Surface Mounted Components for Automated Placement".

The carrier tape material is PVC with a carbon filler and the cover tape is polyester. The reel material is cardboard.

Signetics' SO packages will be loaded onto reels in the quantities indicated in Table 1.

Components packaged in Tape and Reel are protected against damage due to electrostatic discharge. The carrier tape is conductive, as shown in Table 2. Resistivity measurements are in accordance with ASTM-D-991.

The cover tape is heat sealed to the carrier tape along the outer edges of the cover tape. The seal releases when pulled with a peelback force (Z) of 15 grams (min.) to 65 grams (max.). The peelback force must be exerted at an angle of 180–175° with respect to the carrier tape direction. Peel speed is 120 ± 5 mm/min.

Components are loaded with pin #1 on the side nearest the sprocket holes. The carrier tape, cover tape, and reels are designed to withstand normal conditions seen in the industrial environment without changes in dimensions or other physical properties. COMPONENTS ARE FULLY PROTECTED FROM LEAD DAMAGE ONCE THEY ARE LOADED INTO THE TAPE.

Table 1.

PACKAGE TYPE	TAPE		PARTS PER REEL	REEL	
	WIDTH	PITCH		DIAMETER	WIDTH
SO-8	12mm	8mm	2000	330mm	18.4mm
SO-14	16mm	8mm	2000	330mm	22.4mm
SO-16	16mm	8mm	2000	330mm	22.4mm
SO-16L	24mm	12mm	1000	330mm	22.4mm
SO-20	24mm	12mm	1000	330mm	30.4mm
SO-24	24mm	12mm	1000	330mm	30.4mm
SO-28	24mm	12mm	1000	330mm	30.4mm

Table 2. SURFACE RESISTIVITY

ITEM	RESISTIVITY RANGE	RESISTIVITY VALUES	SPECIFICATION
Carrier Tape	CONDUCTIVE	$<1 \times 10^5 \Omega$/sq	$<1 \times 10^5 \Omega$/sq
Cover Tape	ANTISTATIC	$>10^9$ to $>10^{14} \Omega$/sq	None
Reel	ANTISTATIC	$>10^9$ to $>10^{14} \Omega$/sq	None

BOXES

Taped components will be shipped in foil lined packing boxes approximately 16″ × 16″ × 11½″ which will in turn be placed in shipping boxes that are 16″ × 16″ × 10″. The shipping boxes can hold up to 5 packing boxes.

ORDERING

To order Tape and Reel, simply indicate with the letter 'R' after the part number (example: N74LS00DR). This SPC code identifies to the factory that this is a Tape and Reel order. Orders for Tape and Reel MUST BE FOR WHOLE REELS, i.e. 2000 units of SO-8, SO-14 and SO-16, and 1000 units of SO-16L, SO-20, SO-24 and SO-28. NO PARTIAL REELS WILL BE SHIPPED.

SAMPLES

Full reels of dummy parts will be available through Logic Division for purchase by customers who would like to use dummies to check out their automatic pick-and-place machines.

To Get...	Order...
DUMMY-SO-8	M1511DE R
DUMMY-SO-14	M1511DH R
DUMMY-SO-16	M1511DJ R
DUMMY-SO-16L	M1511DJA R
DUMMY-SO-20	M1511DLA R
DUMMY-SO-24	M1511DNA R
DUMMY-SO-28	M1511DQA R

Written by: Mark Kastner

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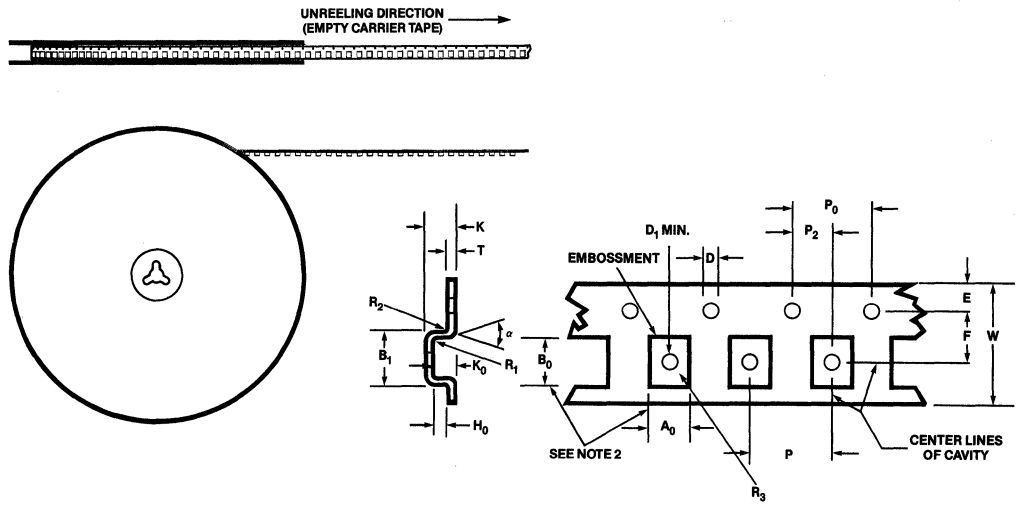
SO Package Tape and Reel

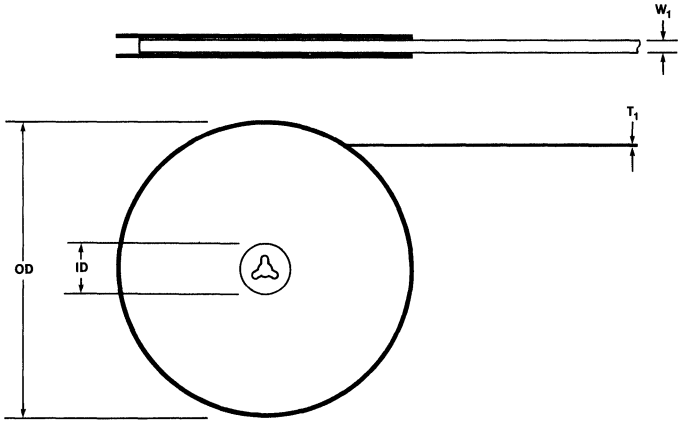
AN210



ITEM		SYMBOL	FOR ALL COMPONENTS SPECIFICATIONS		VALUE BY COMPONENT						
			Value	Tolerance	SO-8	SO-14	SO-16	SO-16L	SO-20L	SO-24L	SO-28L
Carrier Tape	Width	W		±0.30	12	16	16	16	24	24	24
	Film Thickness	t	0.40	Max.							
	Total Thickness	K		Max.	2.4	2.4	2.4	3.2	3.2	3.2	3.2
	Camber	δ	0.3	Max.							
Compartments	Length, Inside	A_0		±0.1	6.33	6.35	6.35	10.8	10.8	10.8	10.8
	Width, Inside	B_0		±0.1	5.15	8.90	10.15	10.65	13.15	15.75	18.25
	Depth, Inside	K_0		±0.1	1.9	1.9	1.9	2.80	2.80	2.80	2.80
	Width, Outside	B_1		Max.	8.2	12.1	12.1	12.1	20.1	20.1	20.1
	Length, Outside										
	Depth, Outside										
	Radius	R_1, R_2, R_3	0.3	Max.							
	Pitch	P		±0.1	8	8	8	12	12	12	12
	Wall Angle	α	6°	±1.0							
	Ref. Plane	H_0	0.3	+0.10 – 0.05							
	Center Line Distance, Width	P_2	2.0	±0.05	Compartment to Sprocket Hole						
	Center Line Distance, Length	F		±0.05	5.5	7.5	7.5	7.5	11.5	11.5	11.5
	Hole Diameter	D_1	1.5	Min. ⊕|ϕ0.2							
Sprocket Hole	Diameter	D	1.55	±0.05							
	Pitch	P_0	4.0	±0.1							
	10-Pitch	—	40.0	±0.2							
	Distance to Edge	E	1.75	±0.1							

NOTES:
1. All feature dimensions in millimeters.
2. A_0 and B_0 dimensions are measured at a plane defined as H_0 distance up from the inside compartment bottom and parallel to the bottom. K_0 is measured from the same plane to the top surface of the tape.
3. Camber to be no more than 1.0 mm per 250 mm length measure per semi specification #G10-83-(Camber).
4. Pin #1 to be nearest sprocket holes. Top side of the package will be up.

Figure 1. Embossed Carrier Tape Specifications



ITEM		SYMBOL	FOR ALL COMPONENTS SPECIFICATIONS		VALUE BY COMPONENT						
			Value	Tolerance	SO-8	SO-14	SO-16	SO-16	SO-20	SO-24	SO-28
Cover Tape	Width	W_1		−0.5	9.0	13.0	13.0	13.0	21.0	21.0	21.0
	Thickness	T_1	0.1	Max.							
	Break Force	—	1.0KG	Min.							

Figure 2. Cover Tape Specifications

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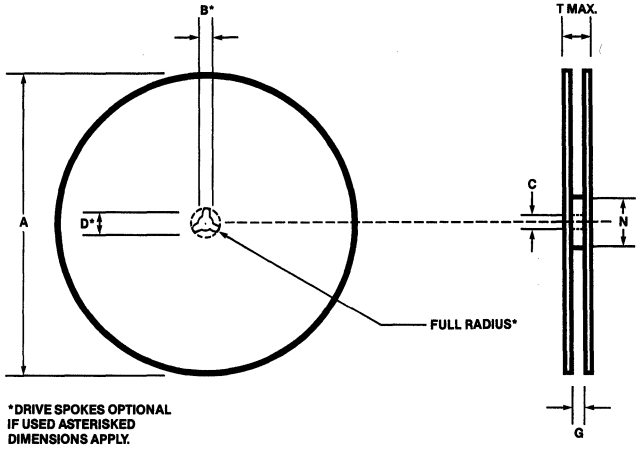
SO Package Tape and Reel AN210



ITEM			SYMBOL	FOR ALL COMPONENTS SPECIFICATIONS Value	Tolerance	VALUE BY COMPONENT SO-8	SO-14	SO-16	SO-16	SO-20	SO-24	SO-28
Reel Flange	Diameter, Outside		A	330	Max.							
	Thickness		t									
	Space Between Flanges		G		+2.0	12.4	16.4	16.4	16.4	24.4	24.4	24.4
Reel Hub	Diameter, Outside		N	55	±2.0							
	Diameter, Hole		C	13.0	±0.5							
	Key Slots	Width	B*	1.5	Min.							
		Diameter	D*	20.2	Min.							
		Location	o	120°								
Reel Assy.	Thickness		T		Max.	18.4	22.4	22.4	22.4	30.4	30.4	30.4

NOTES:
1. All feature dimensions in millimeters.
2. A clearance of 0.1mm to 2.2mm max. will be maintained between the carrier tape and the reel at the hub. This clearance will be measured at the hub O.D.
3. Dimension T and G will be measured at the hub O.D.

Figure 3. Reel Specifications

Signetics

Package Information
Section 10

Linear Products

Section 10 Package Information

Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

PLASTIC ONLY

5. Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO Packages-microminiature packages.
   a. Lead material: Alloy-42.
   b. Body material: Plastic (Epoxy).

HERMETIC ONLY

10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
    b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated or solder dipped.
    c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel or tin plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
    d. BeO Ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb .010 inches.
16. Maximum glass climb or lid skew is .010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

10

Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

PLASTIC PACKAGES			
	PACKAGE CODE	Θ_{ja}/Θ_{jc}(°C/W)	DESCRIPTION
Standard Dual-in-Line Packages			
8-Pin	N	99/50	
14-Pin	N	86/48	TO-116/MO-001
16-Pin	N	83/42	MO-001
18-Pin	N	63/29	
20-Pin	N	61/24	
22-Pin	N	51/23	
24-Pin	N	52/23	MO-015
28-Pin	N	52/23	MO-015
Metal Headers			
4-Pin	E	100/20	TO-46 Header
4-Pin	E	150/25	TO-72 Header
8-Pin	H	150/25	TO-5 Header
10-Pin	H	150/25	TO 5/TO-100 Header, Short Can
10-Pin	H	150/25	TO-5/TO-100 Header, Tall Can
Cerdip Family			
8-Pin	FE	110/30	Dual-in-Line Ceramic
14-Pin	F	110/30	Dual-in-Line Ceramic
16-Pin	F	100/30	Dual-in-Line Ceramic
18-Pin	F	93/27	Dual-in-Line Ceramic
20-Pin	F	90/25	Dual-in-Line Ceramic
22-Pin	F	75/27	Dual-in-Line Ceramic
24-Pin	F	60/26	Dual-in-Line Ceramic
28-Pin	F	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
16-Pin	I	90/25	Dip Laminate

SO Package Thermal Data

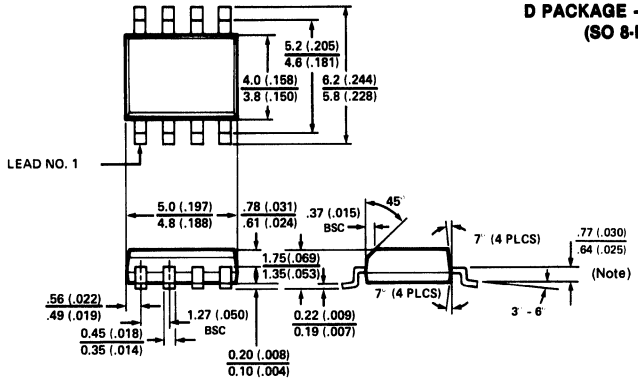
Package Type	Package Mounting Technique*	Max. Allowable Power Diss. (mW) at 25°C	Max. Allowable Power Diss. (mW) at 70°C	Thermal Resistance (θ_{JA}°C/Watt) Average	Maximum
SO-14	PCB	658	421	190	225
	Ceramic	962	615	130	165
	Ceramic w/H.S.	1471	941	85	110
SO-16	PCB	862	551	145	170
	Ceramic	1250	800	100	125
	Ceramic w/H.S.	1923	1231	65	85
SO-16L	PCB	1250	800	100	140
	Ceramic	1743	1143	70	100
	Ceramic w/H.S.	2500	1600	50	65
SO-20	PCB	1471	941	85	115
	Ceramic	2273	1454	55	85
	Ceramic w/H.S.	3572	2286	35	55
SO-24	PCB	1563	1000	80	110
	Ceramic	2000	1600	50	80
	Ceramic w/H.S.	4167	2667	30	50

PCB = Printed circuit board
Ceramic = Ceramic substrate
Ceramic w/H.S. = Ceramic substrate with heat sink and/or thermal compound
*Air gap is 0.006 inches unless thermal compound is used

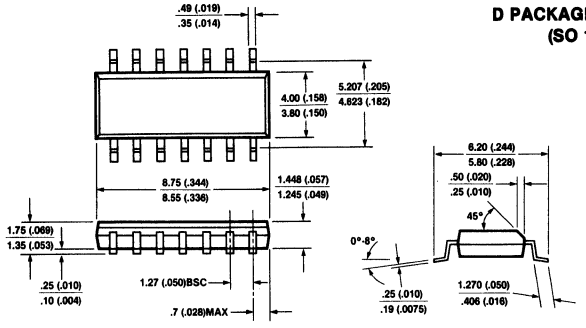
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

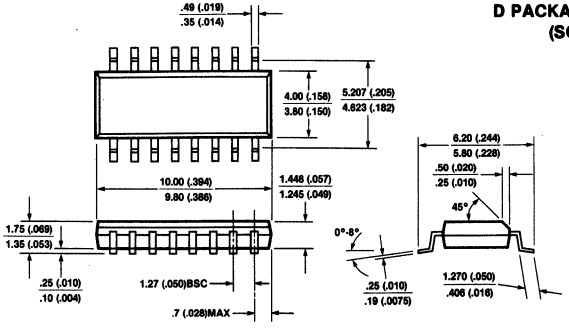
D PACKAGE — PLASTIC (SO 8-PIN)



D PACKAGE — PLASTIC (SO 14-PIN)



D PACKAGE — PLASTIC (SO 16-PIN)



Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

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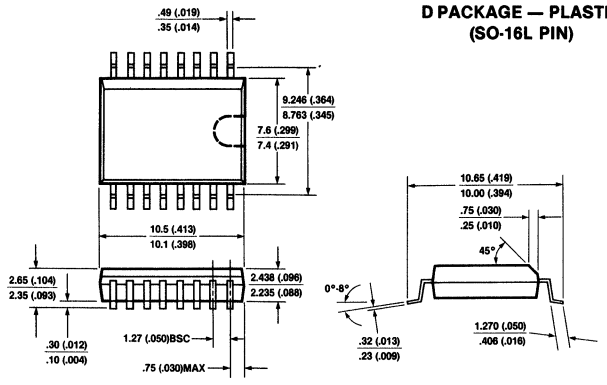
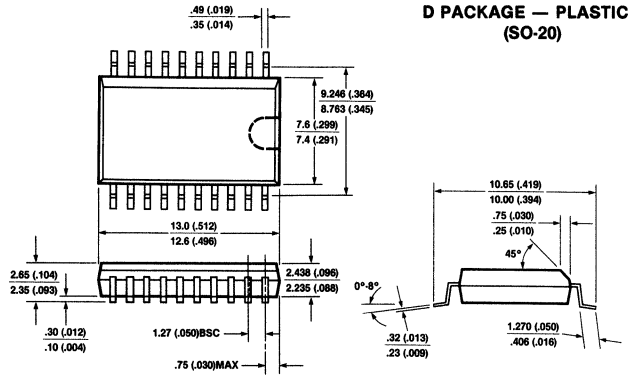
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

D PACKAGE — PLASTIC (SO-16L PIN)



D PACKAGE — PLASTIC (SO-20)

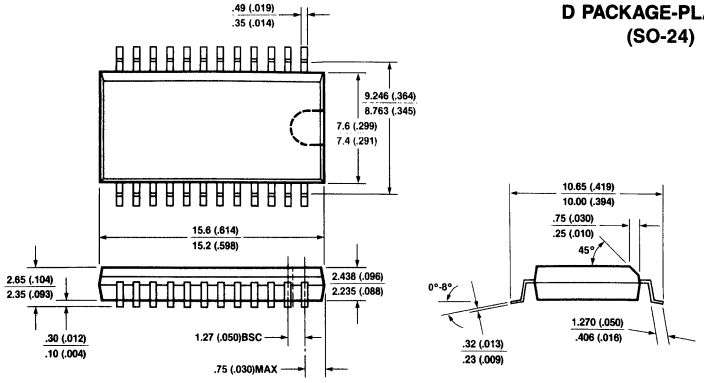


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

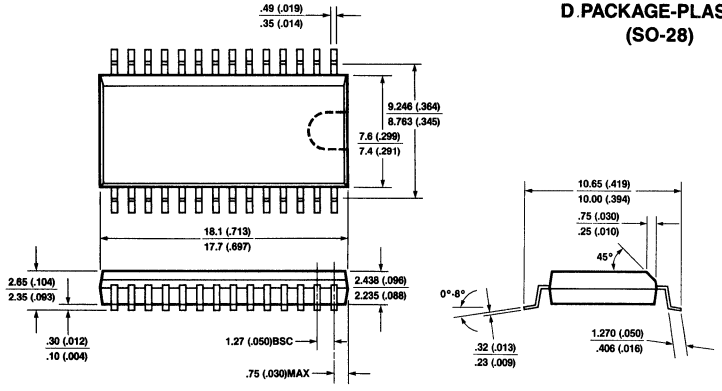
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

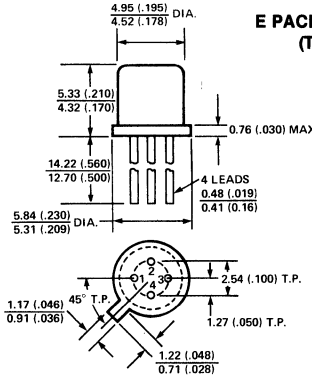
D PACKAGE-PLASTIC (SO-24)



D PACKAGE-PLASTIC (SO-28)



E PACKAGE — HERMETIC (TO-72 HEADER)



Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

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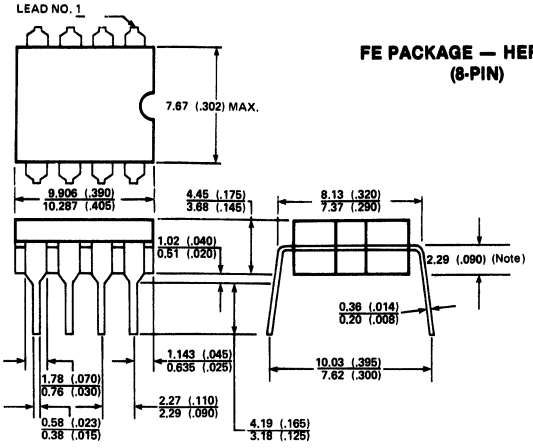
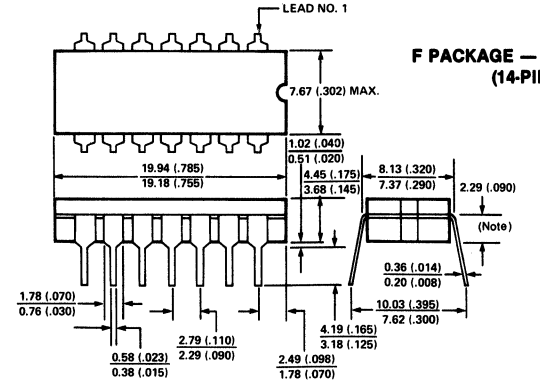
Package Outlines

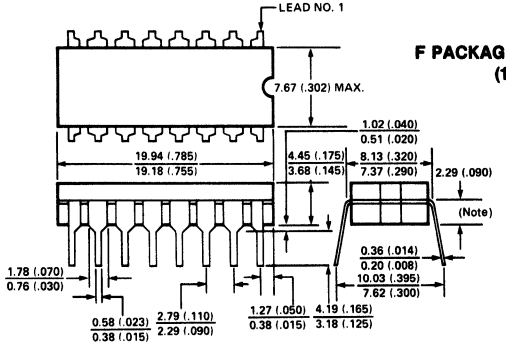
FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN



FE PACKAGE — HERMETIC (8-PIN)



F PACKAGE — HERMETIC (14-PIN)

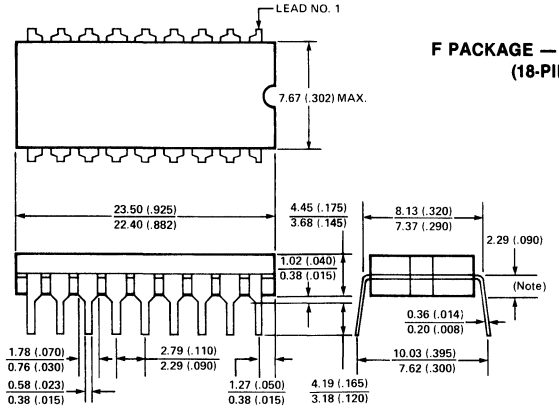


F PACKAGE — HERMETIC (16-PIN)

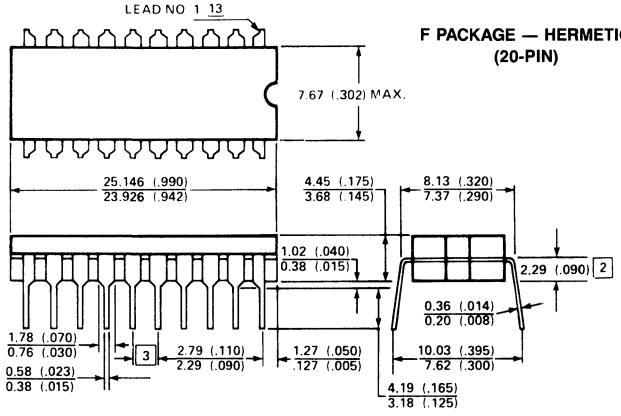
Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

Package Outlines

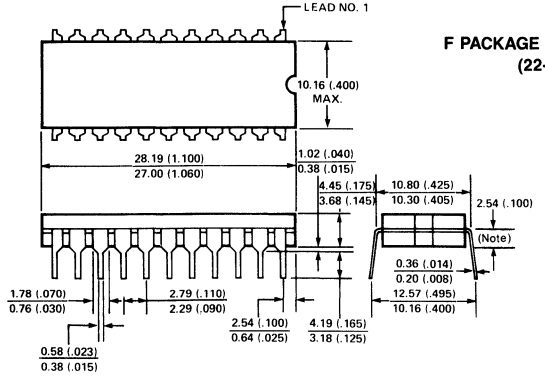
FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN



F PACKAGE — HERMETIC (18-PIN)



F PACKAGE — HERMETIC (20-PIN)



F PACKAGE — HERMETIC (22-PIN)

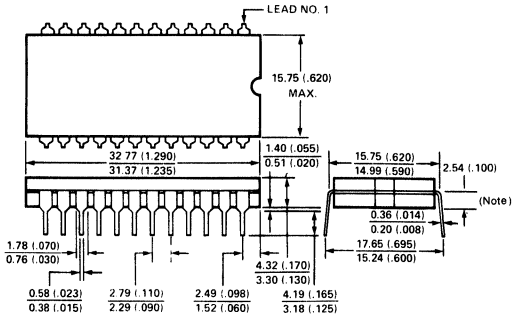
Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

10

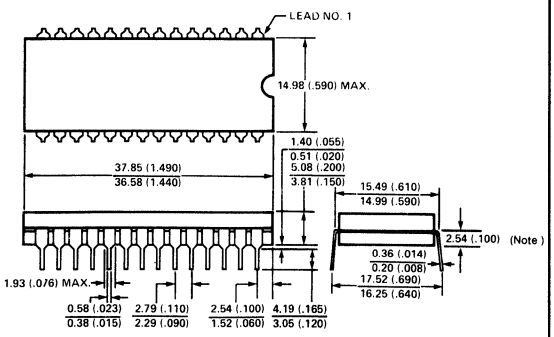
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

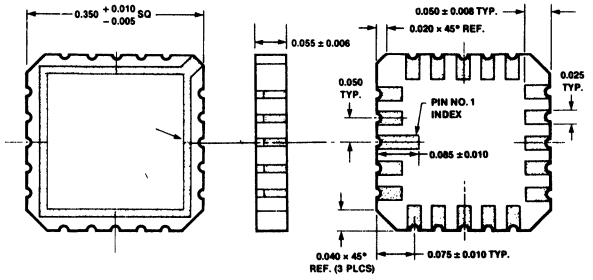
F PACKAGE — HERMETIC (24-PIN)



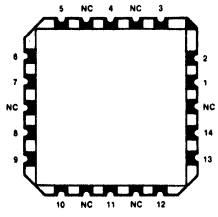
F PACKAGE — HERMETIC (28-PIN)



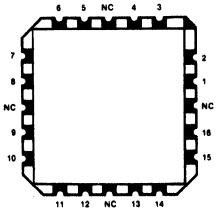
G PACKAGE



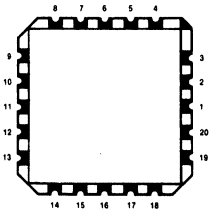
G PACKAGE (14-PIN)



G PACKAGE (16-PIN)



G PACKAGE (20-PIN)

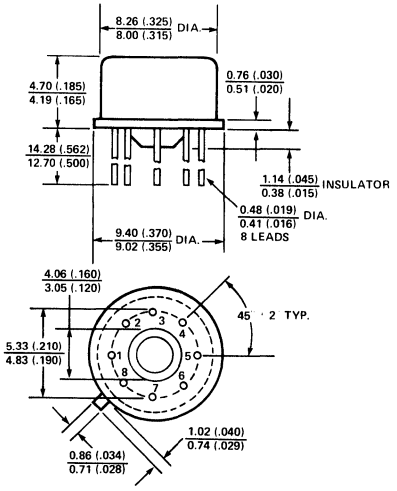


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

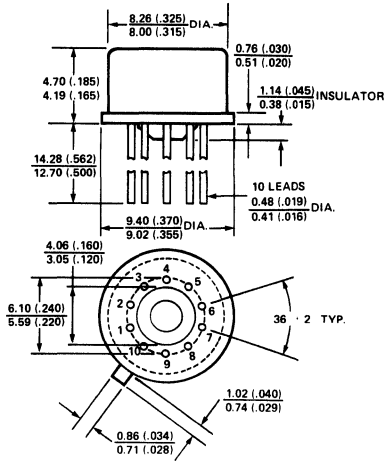
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

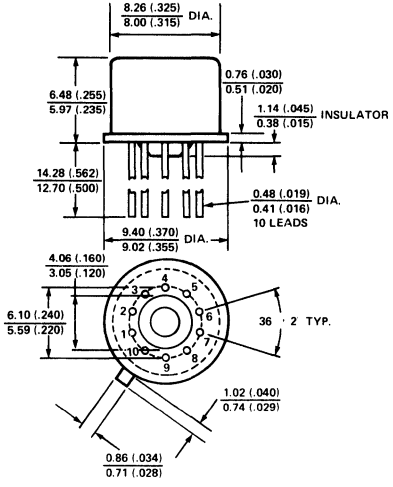
H PACKAGE — HERMETIC 8-PIN (TO-5 HEADER)



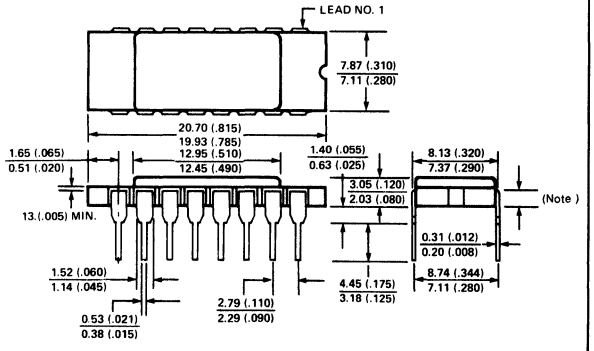
H PACKAGE — HERMETIC 10-PIN (TO-5/100 HEADER SHORT CAN)



H PACKAGE HERMETIC 10-PIN (TO-5/100 HEADER TALL CAN)



I PACKAGE — HERMETIC (16-PIN)

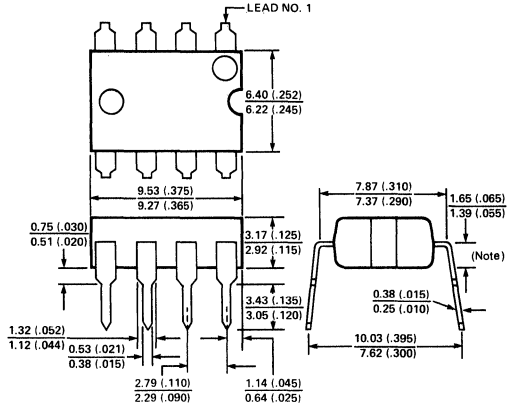


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

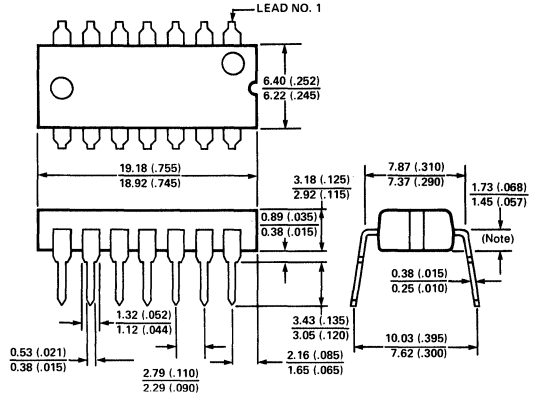
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC (8-PIN)



N PACKAGE — PLASTIC (14-PIN)

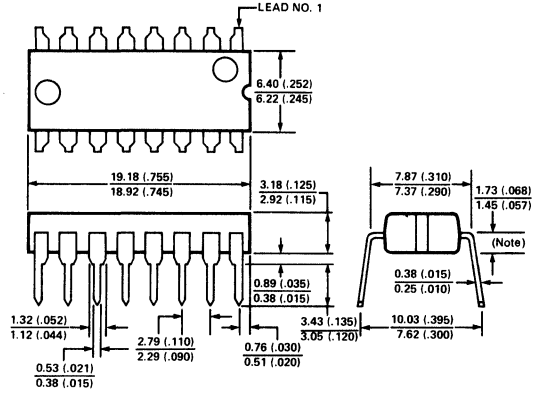


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

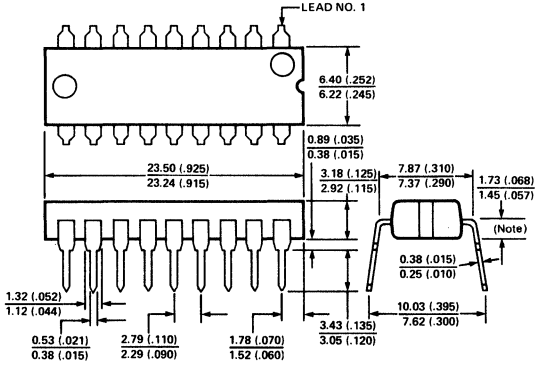
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC (16-PIN)



N PACKAGE — PLASTIC (18-PIN)



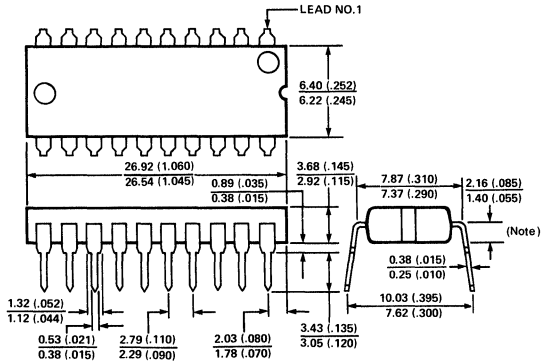
Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

10

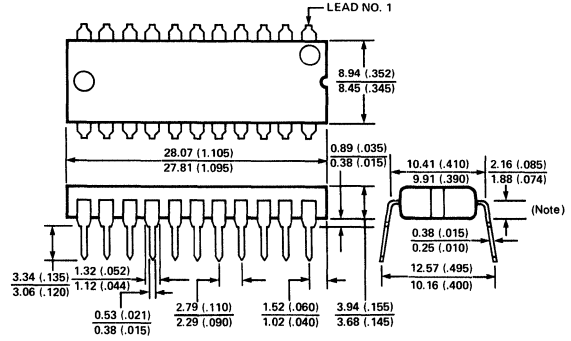
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC (20-PIN)



N PACKAGE — PLASTIC (22-PIN)

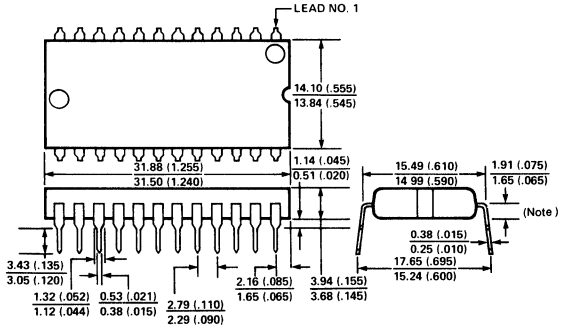


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

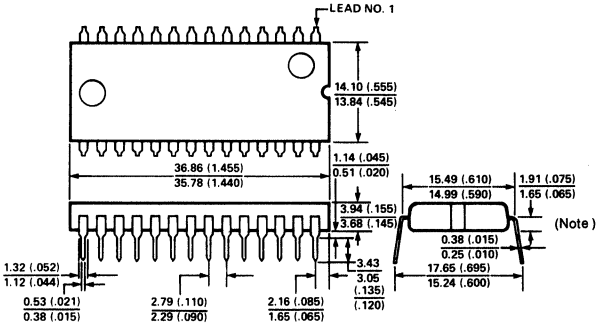
Package Outlines

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC (24-PIN)



N PACKAGE — PLASTIC (28-PIN)



Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

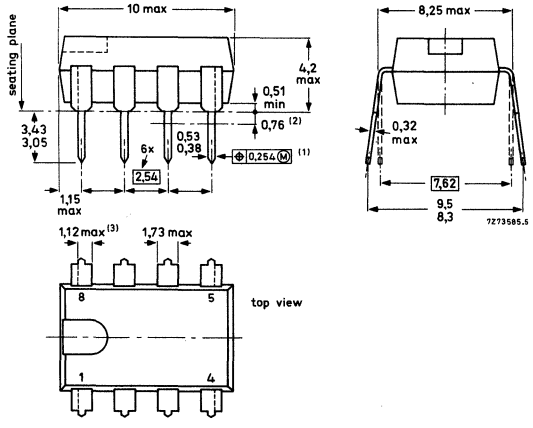
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

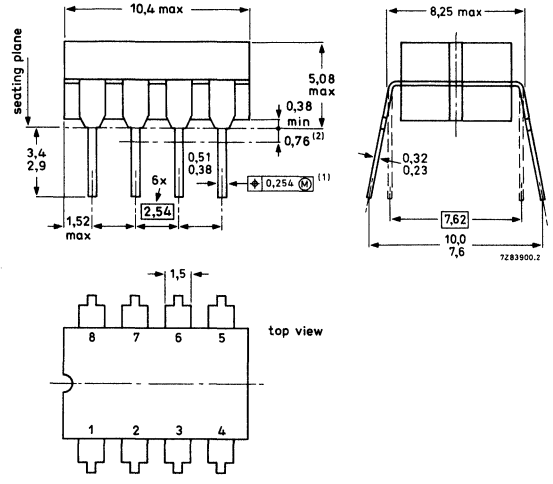
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97A)



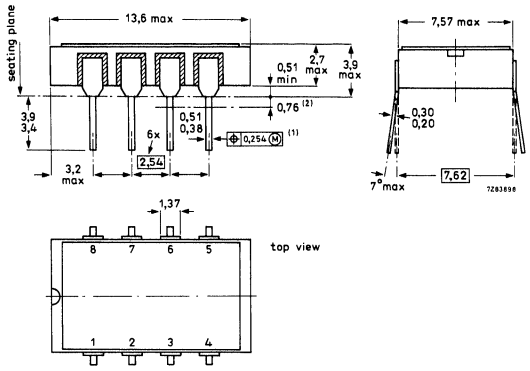
8-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-151A)



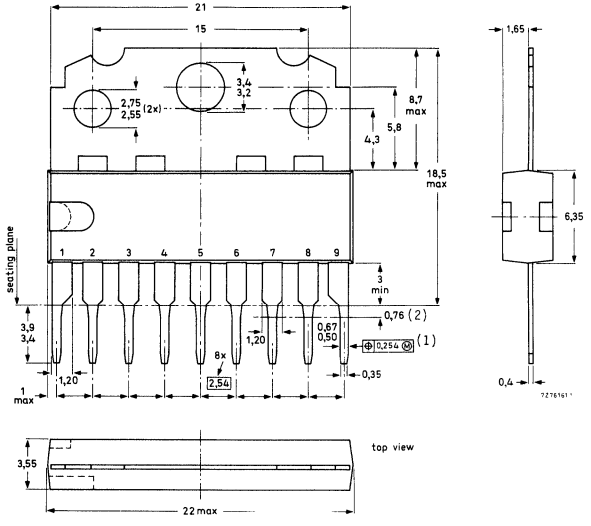
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

8-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-153B)



9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110B)

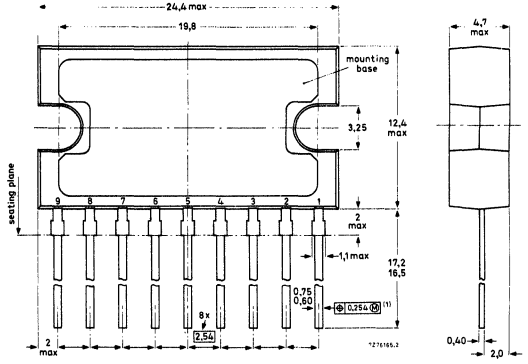


10

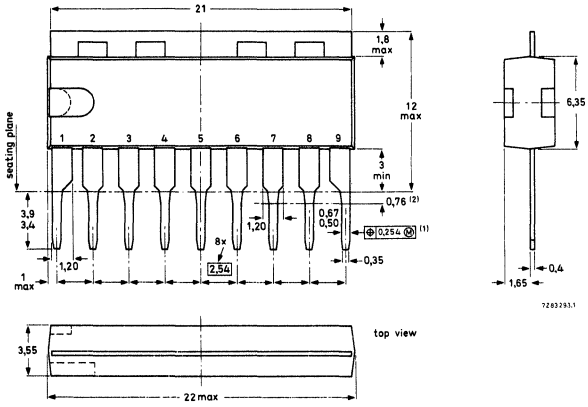
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT-131A, B)



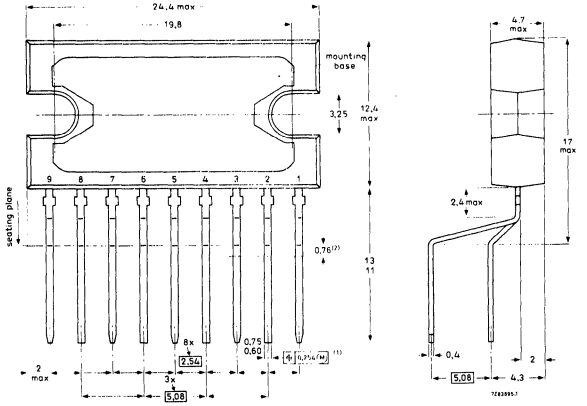
9-LEAD SINGLE IN-LINE; PLASTIC (SOT-142)



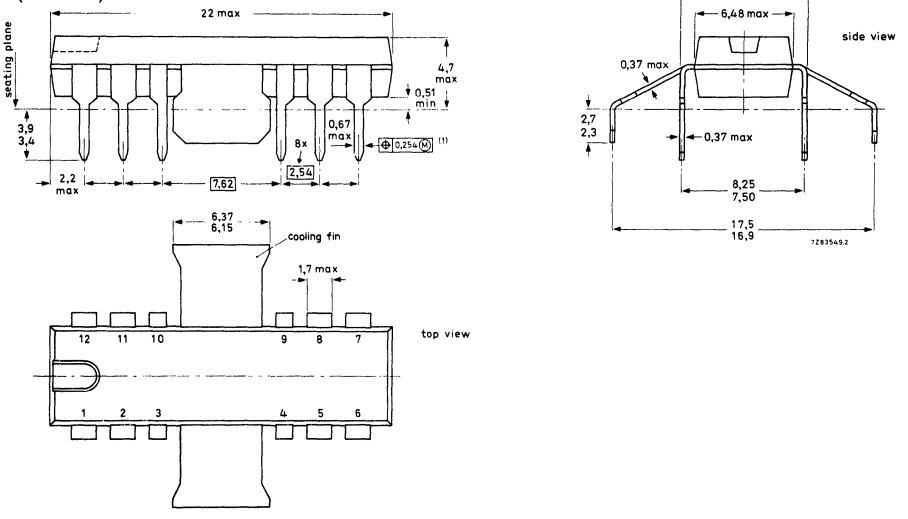
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-157B)



12-LEAD DUAL IN-LINE; PLASTIC WITH METAL COOLING FIN (SOT-150)

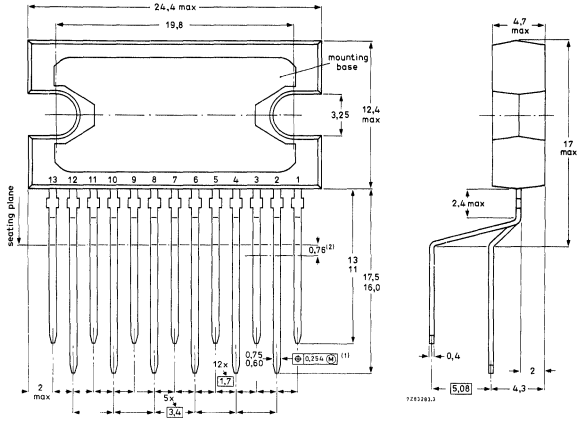


10

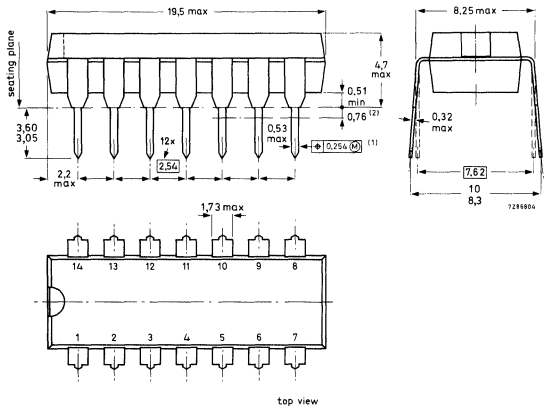
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-141B)



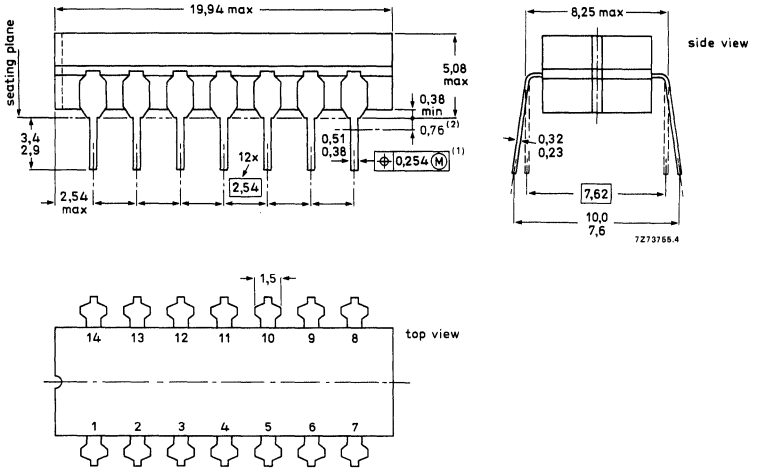
14-LEAD DUAL IN-LINE; PLASTIC (SOT-27K,M,T)



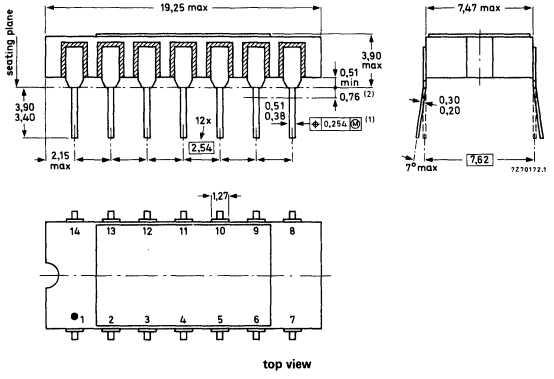
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

14-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-73A,B,C)



14-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-83B)



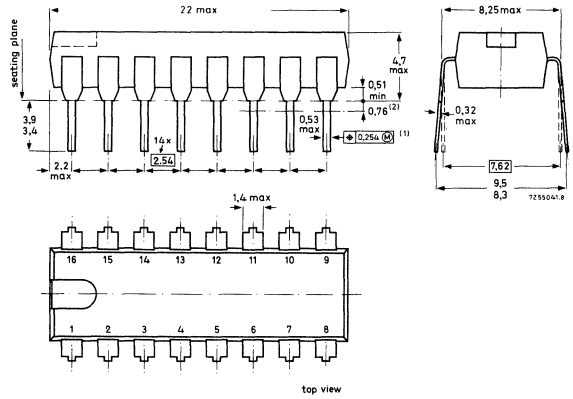
Dimensions in mm

10

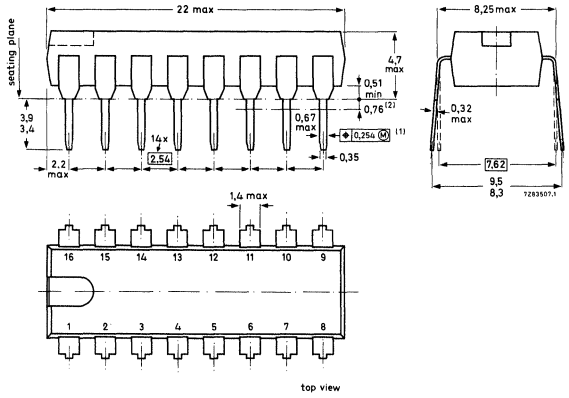
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



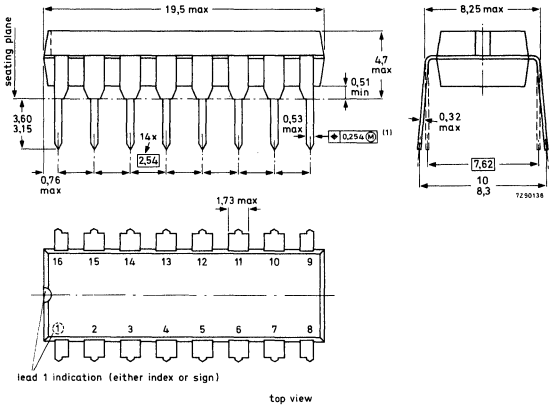
16-LEAD DUAL IN-LINE; PLASTIC (SOT-38A)



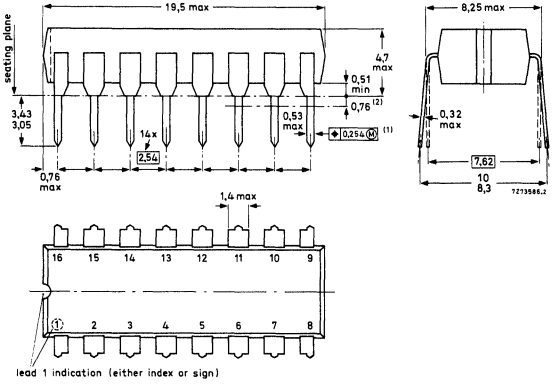
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38D, DE)



16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)

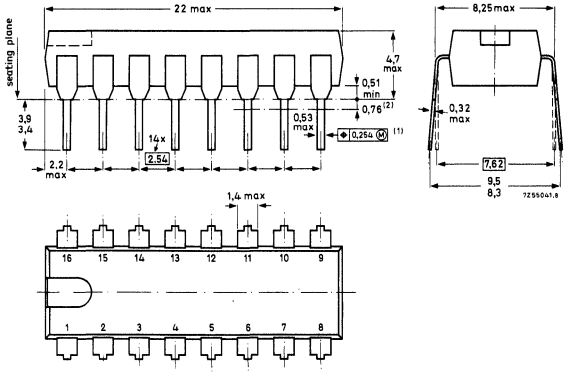


10

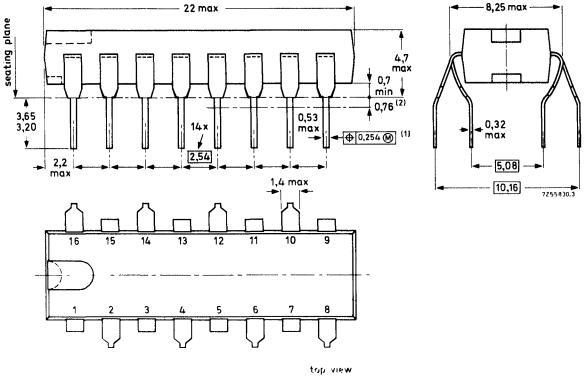
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER
(SOT-38WE-2)



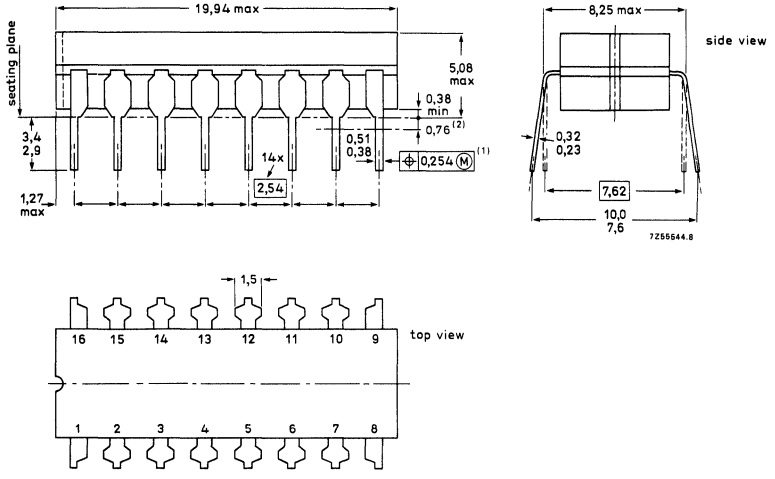
16-LEAD QUADRUPLE IN-LINE; PLASTIC (SOT-58)



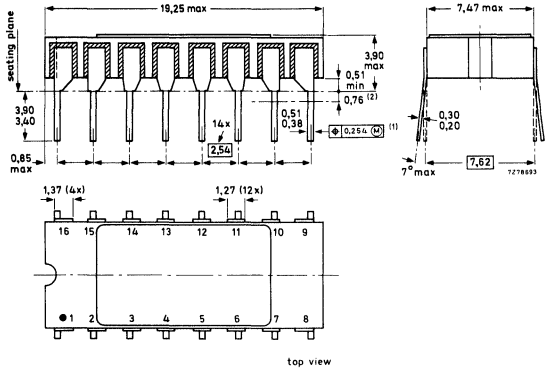
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-74A,B,C)



16-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-84B)



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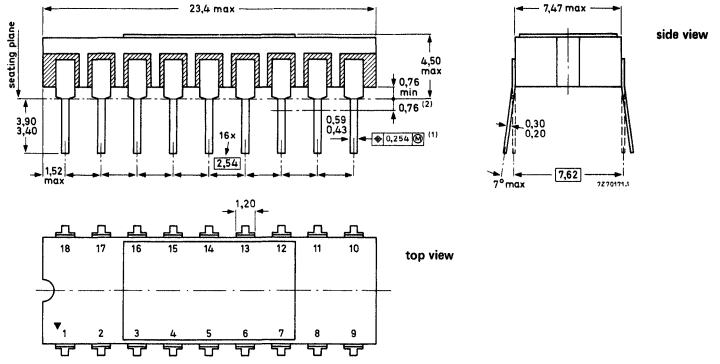
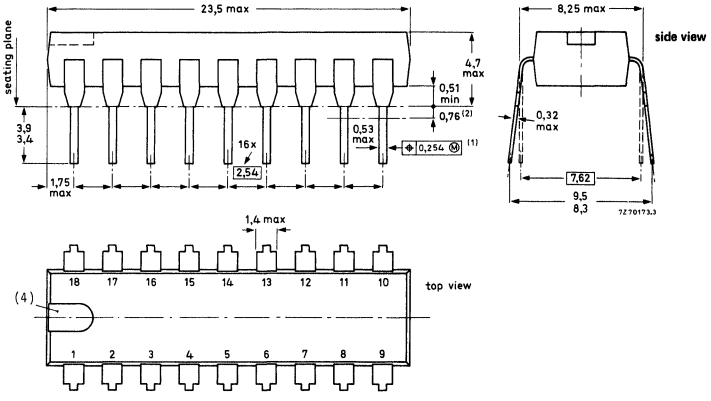
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

18-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-85B)



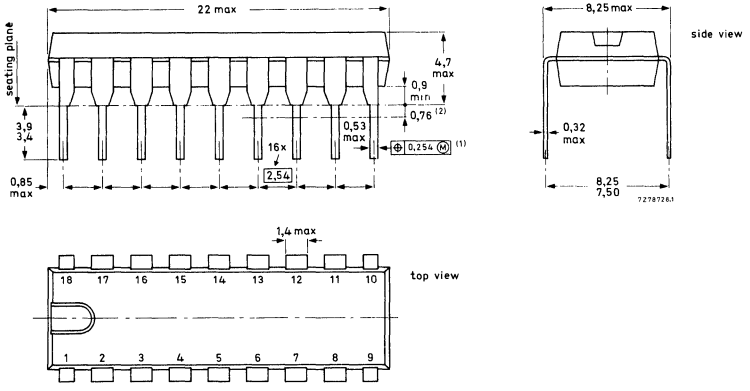
18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)



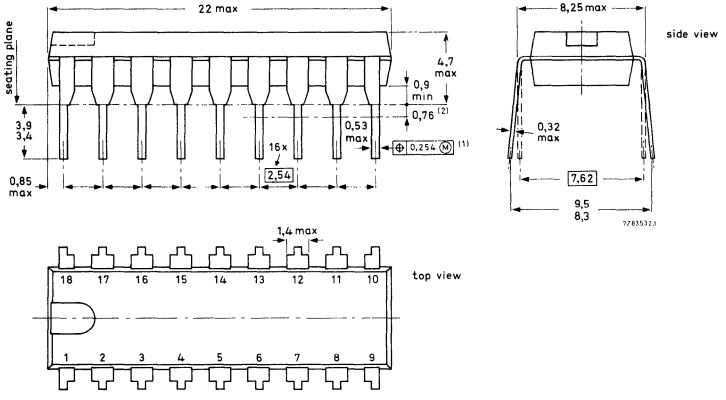
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102C)



18-LEAD DUAL IN-LINE; PLASTIC (SOT-102CS)



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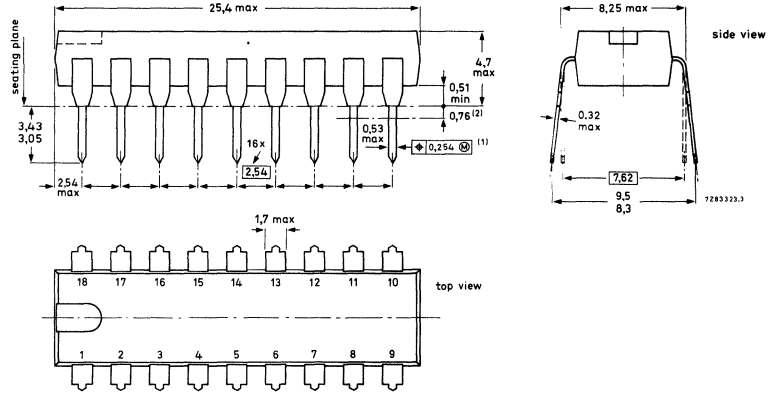
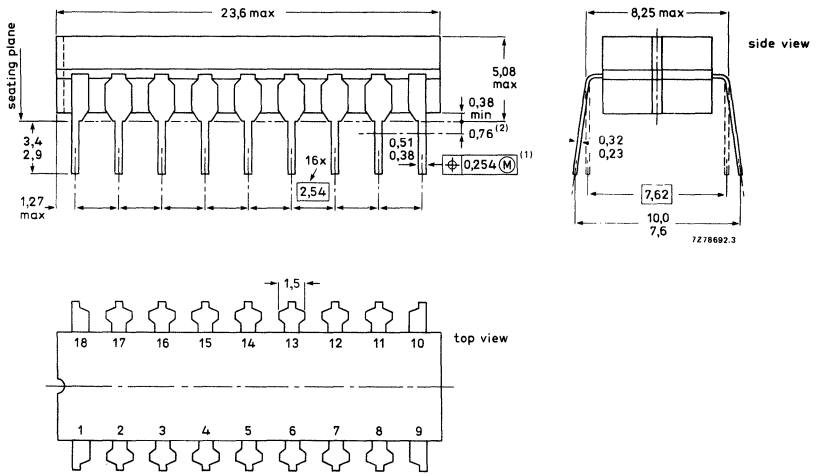
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102G)



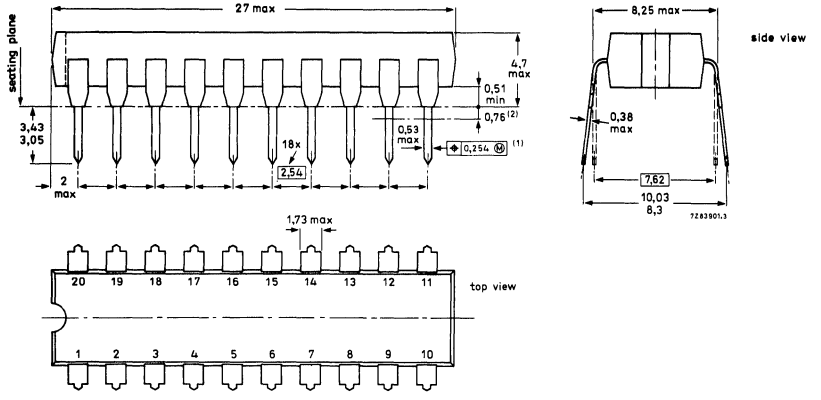
18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-133A,B)



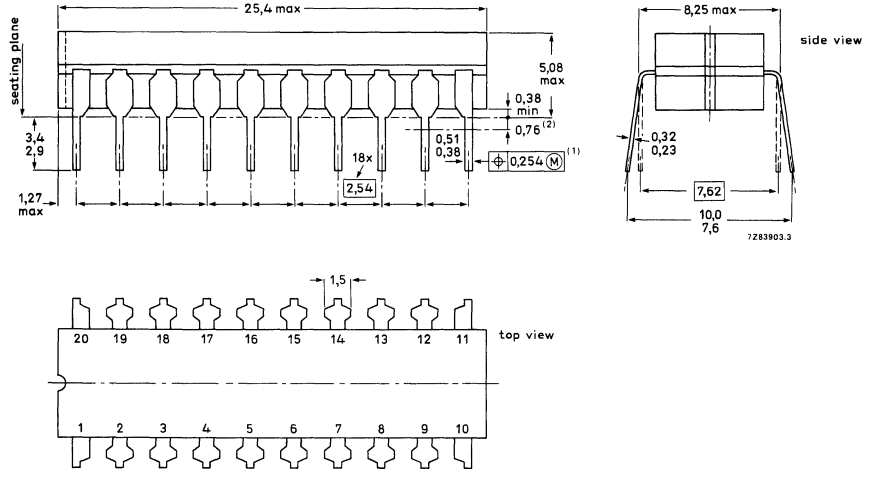
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

20-LEAD DUAL IN-LINE; PLASTIC (SOT-146)



20-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-152B, C)



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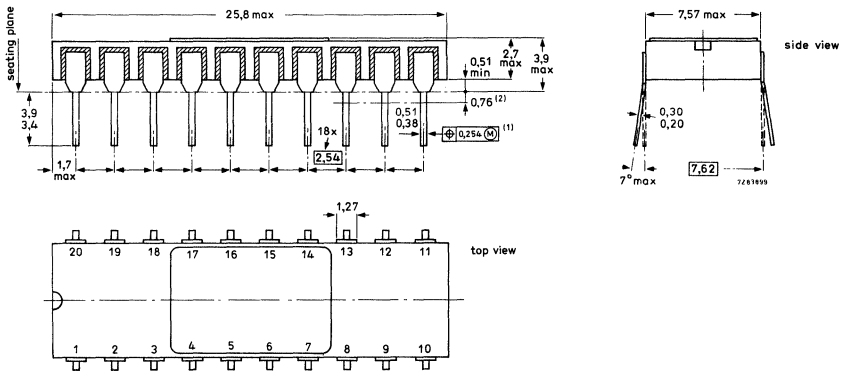
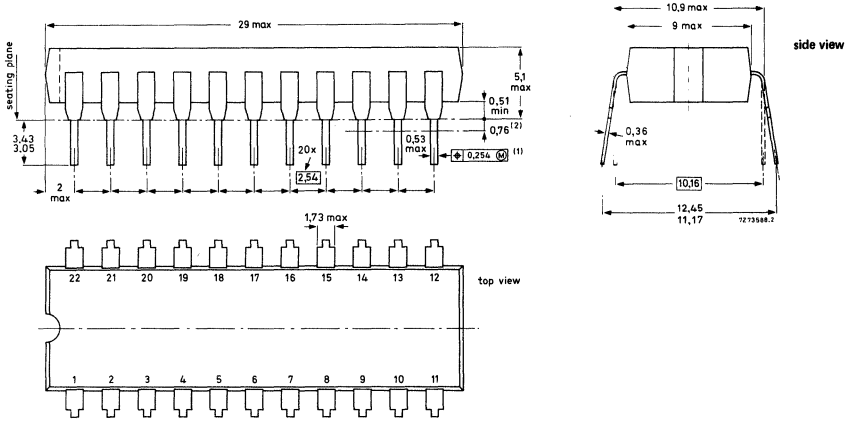
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

20-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-154B)



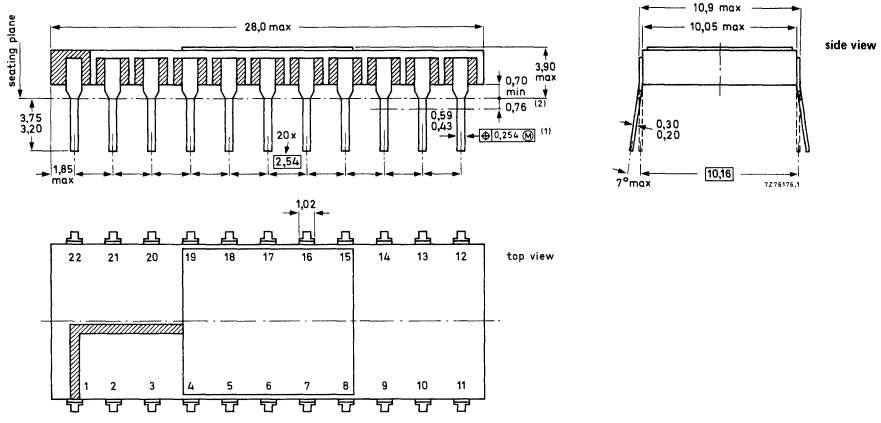
22-LEAD DUAL IN-LINE; PLASTIC (SOT-116)



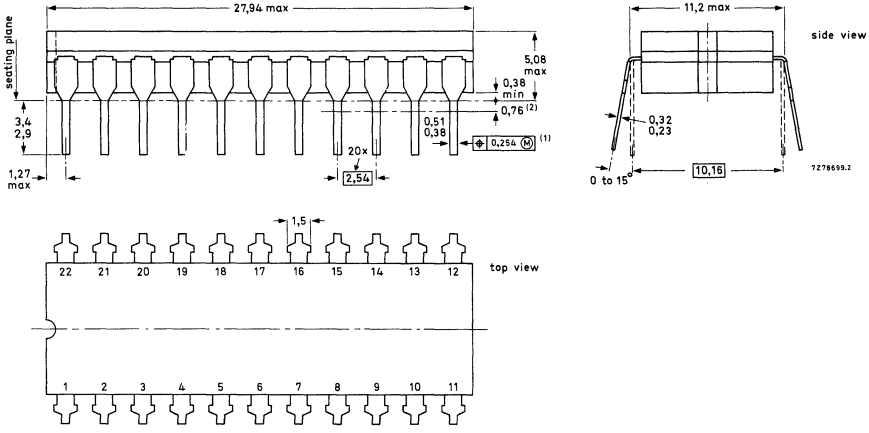
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

22-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-118B)



22-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-134A)



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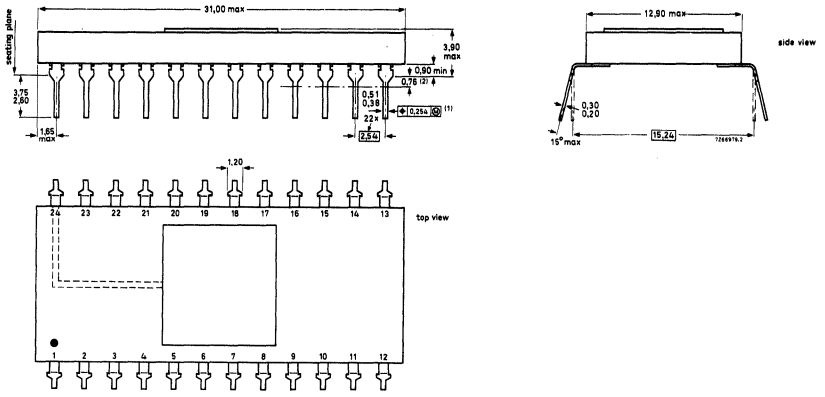
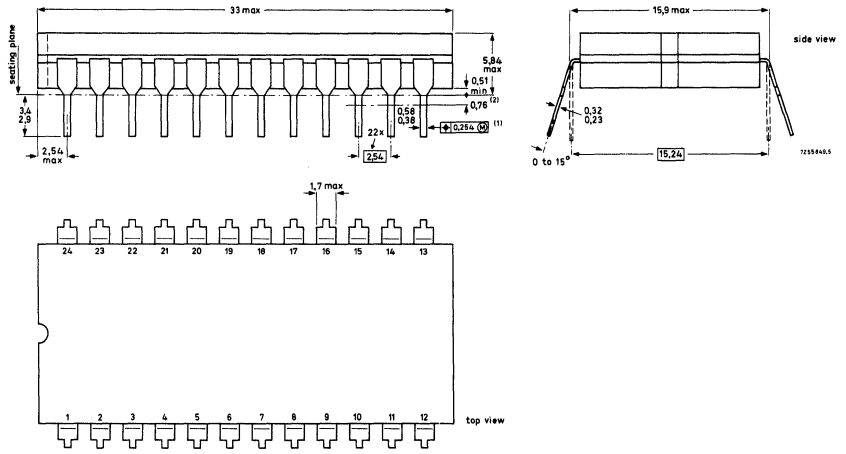
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

24-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-86A)



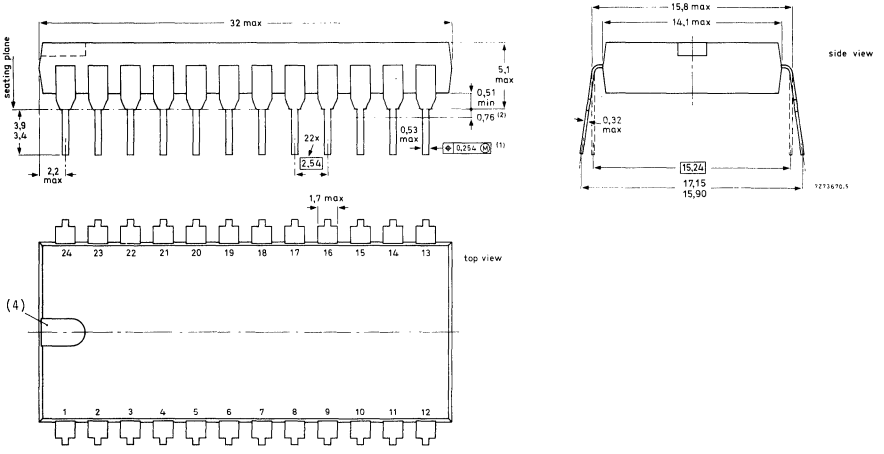
24-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-94)



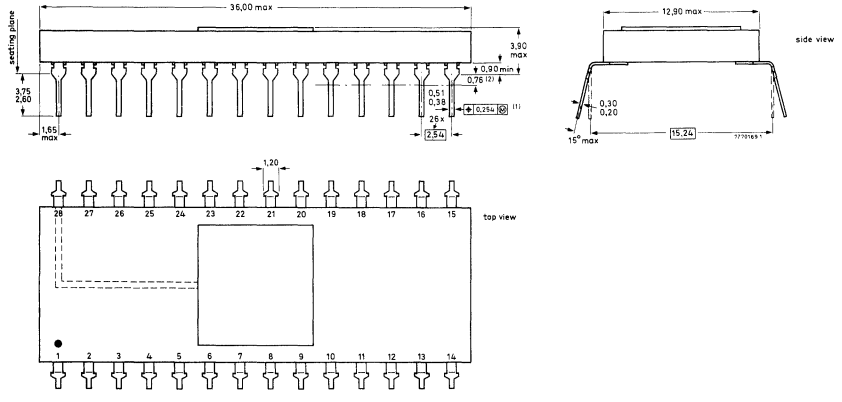
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

24-LEAD DUAL IN-LINE; PLASTIC (WITH INTERNAL HEAT SPREADER) (SOT-101A, B)



28-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-87A)



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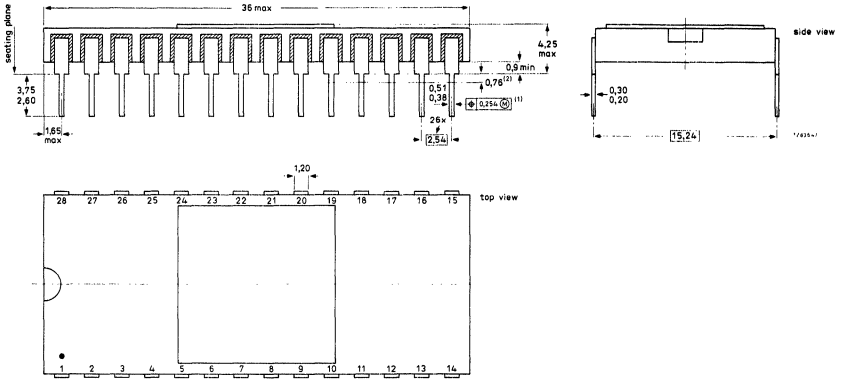
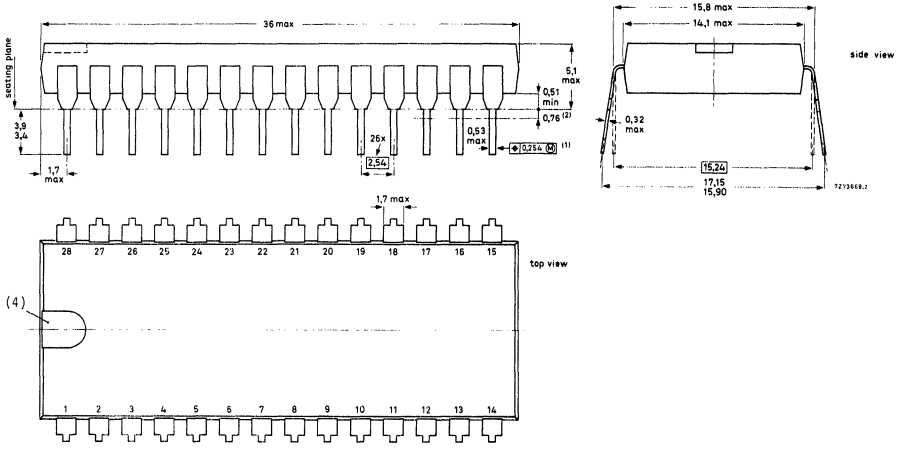
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

28-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-87B)



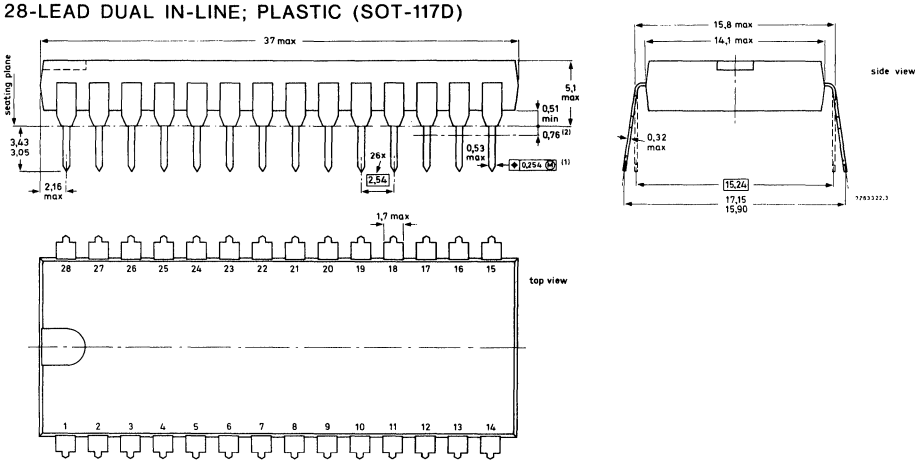
28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)



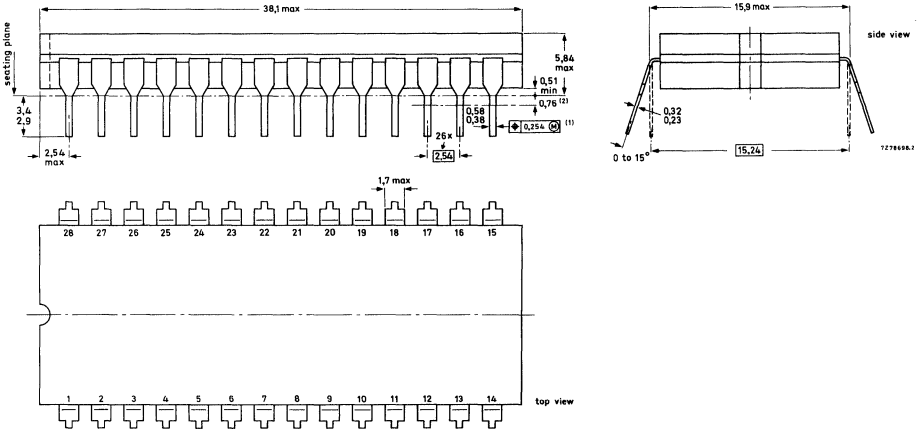
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117D)



28-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-135A)



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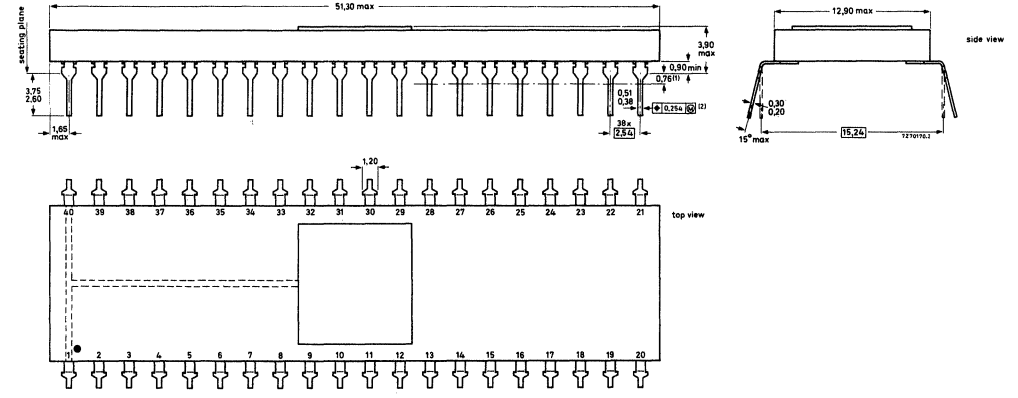
Package Outlines

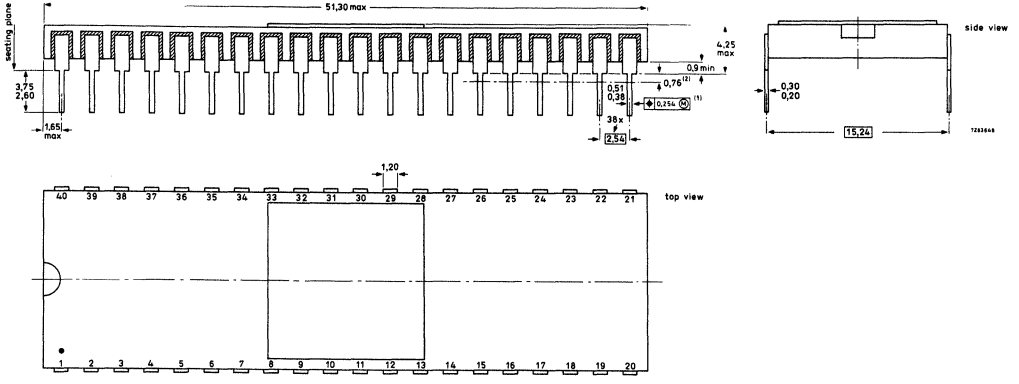
FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

40-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-88)

NO-102 SOT-88



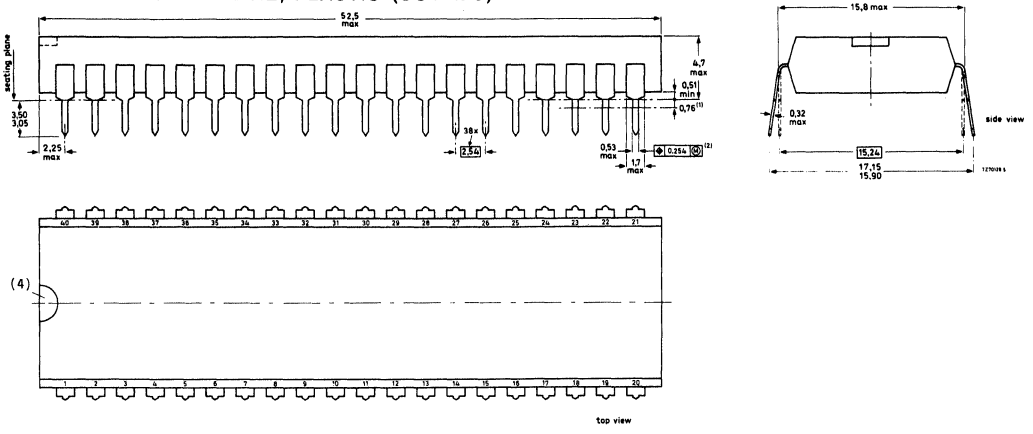
40-LEAD DUAL IN-LINE; METAL CERAMIC (CERDIL) (SOT-88B)



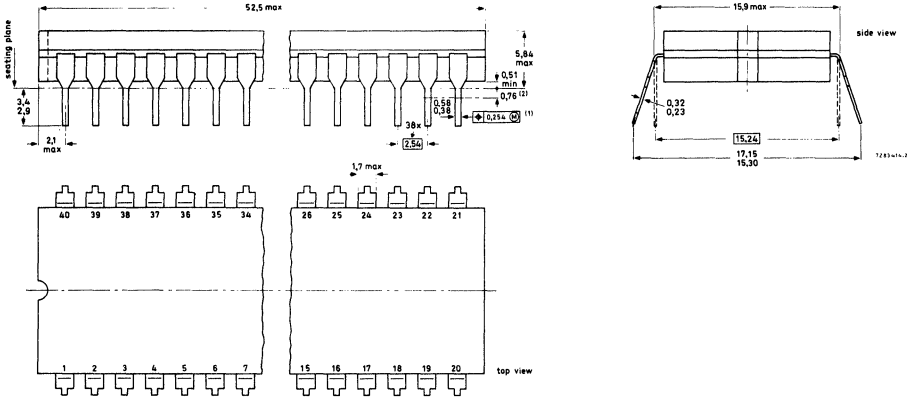
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)



40-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-145)



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Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

SOLDERING

The reflow solder technique

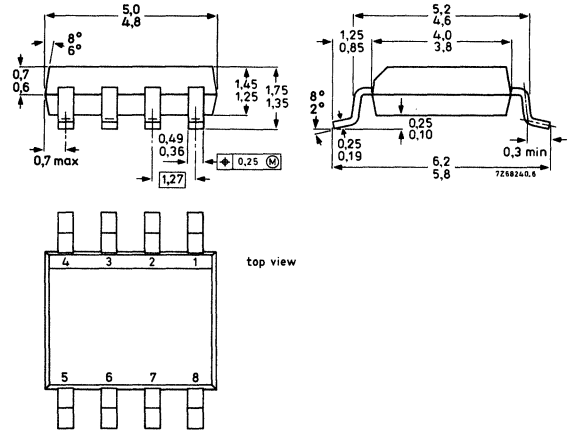
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

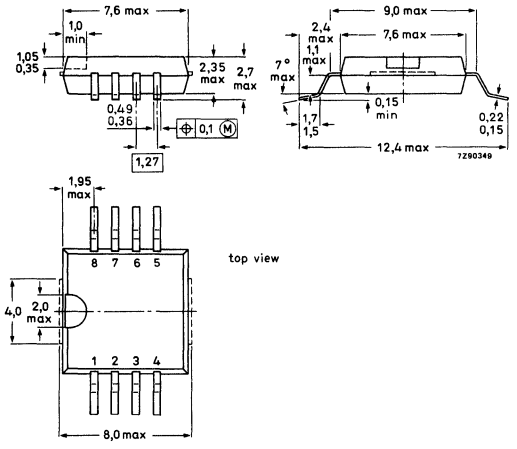
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

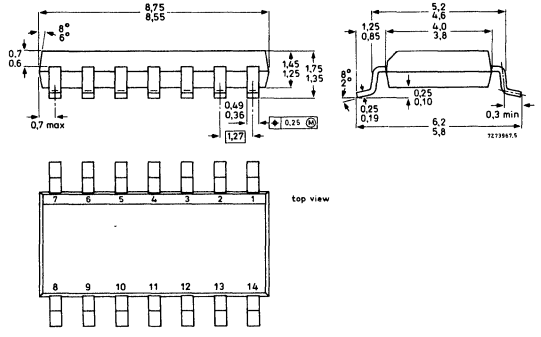
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

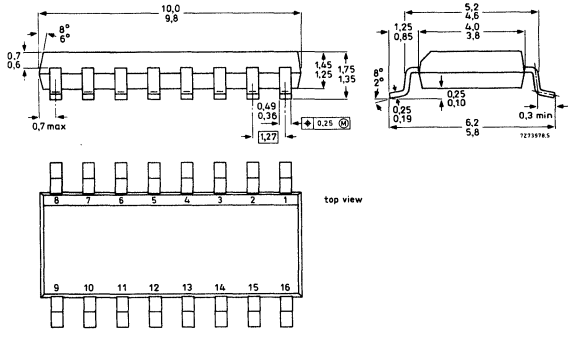
8-LEAD MINI-PACK; PLASTIC (VSO-8; SOT-176)



14-LEAD MINI-PACK; PLASTIC (SO-14; SOT-108A)



16-LEAD MINI-PACK; PLASTIC (SO-16; SOT-109A)

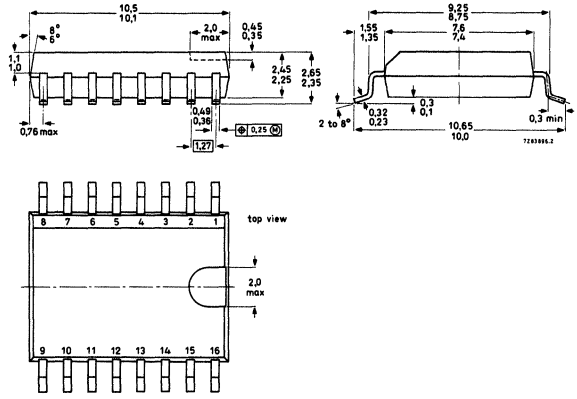


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

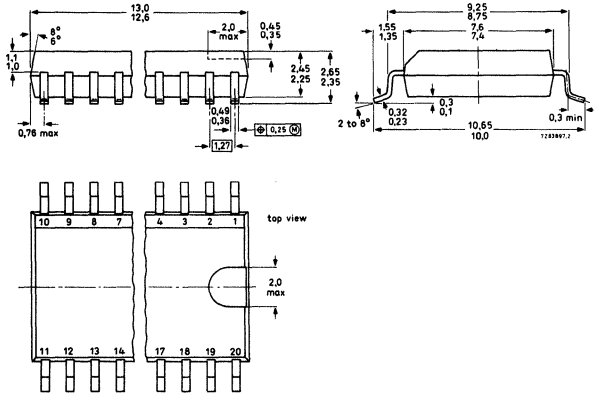
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

16-LEAD MINI-PACK; PLASTIC (SO-16L; SOT-162A)



20-LEAD MINI-PACK; PLASTIC (SO-20; SOT-163A)

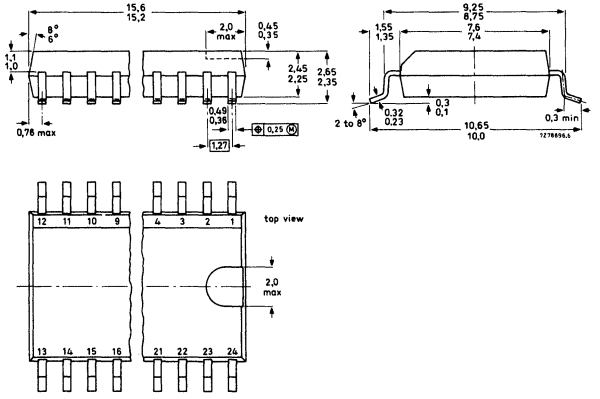


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

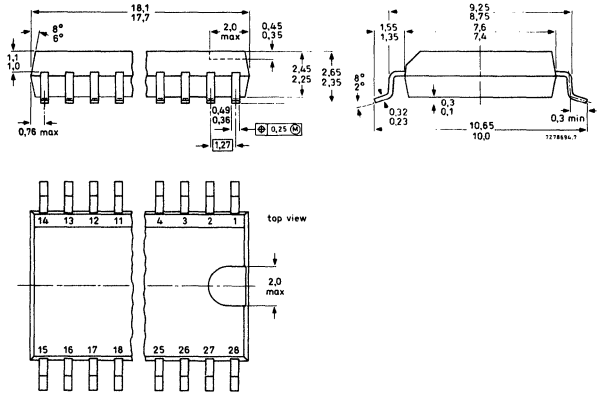
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

24-LEAD MINI-PACK; PLASTIC (SO-24; SOT-137A)



28-LEAD MINI-PACK; PLASTIC (SO-28; SOT-136A)

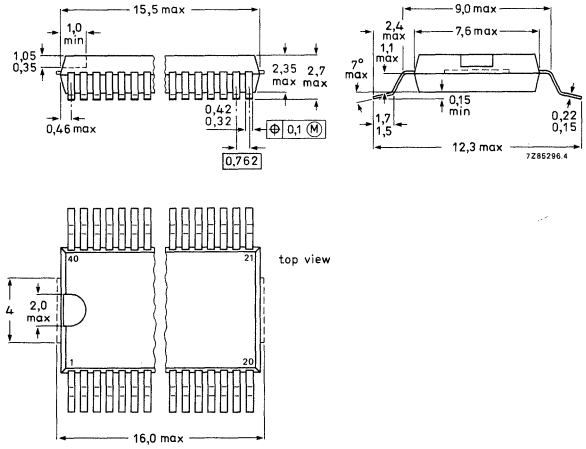


Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

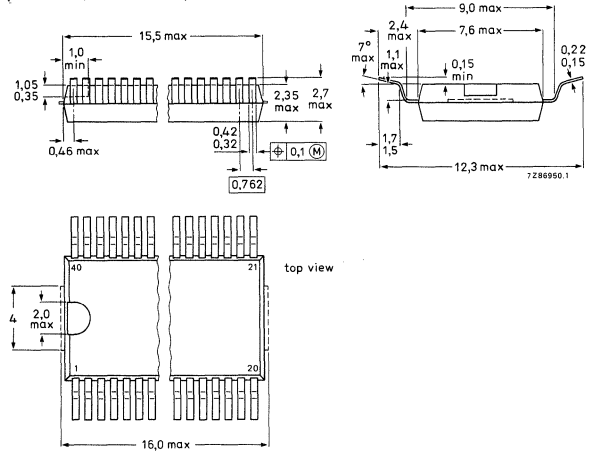
Package Outlines

FOR PREFIXES HEF, OM, MAB, MAF, MEA, PC, PN, SAA, SAB, SAF, TA, TB, TC, TD, TE, μAA

40-LEAD MINI-PACK; PLASTIC (VSO-40; SOT-158A)



40-LEAD MINI-PACK; PLASTIC (OPPOSITE BENT LEADS)
(VSO-40; SOT-158B)



Signetics

Sales Offices
Section 11

Linear Products

Sales Offices

SIGNETICS

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NE5212	Fiber Optic Preamplifier

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