CMOS

CMOS Integrated Circuit Data Book

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AUGUST 1990

SIERRA SEMICONDUCTOR

Sierra at a Glance

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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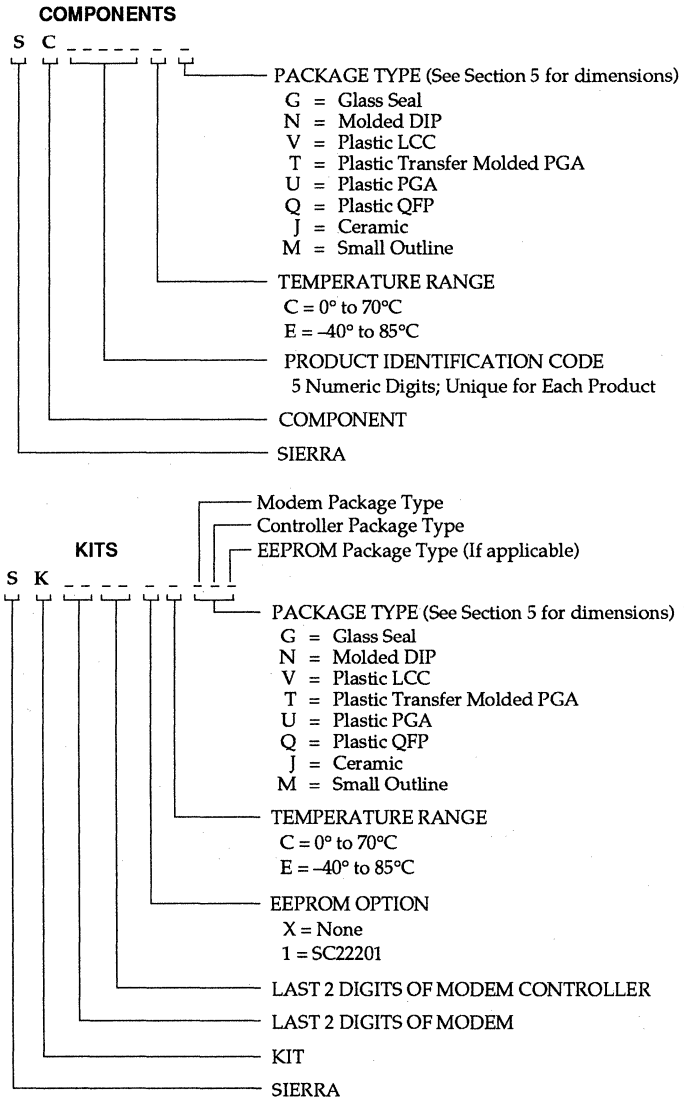
Introduction

The functional index beginning on the following page is arranged to facilitate the quick location of products of interest. Within the three product groupings (Data Communications, Telecommunications, and Graphics), the individual data sheets are in alphanumeric sequence. The numerical index on page xii is provided to quickly locate products where the product number is known.

Sierra Semiconductor uses 9-digit and 11-digit alphanumeric codes to uniquely identify the Company's products. The Company's product line consists of both individual components and kits, or chip sets. The components used in kits are often used in more than one kit. Hence, separate data sheets are provided for each component. The two charts below explain the significance of each digit in the code.



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® Sendfax is a registered trademark of Sierra Semiconductor Corporation.

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Data Communication Products 1

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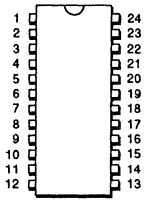
FEATURES

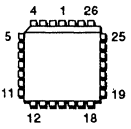
- ☐ Transmit and Receive filters with half-channel compromise equalizers
- ☐ Call Progress Mode Answer/ Originate mode switching
- ☐ Bell 212A, CCITT V.22 and V.22bis compatible with V.22 notch filters
- ☐ Analog Loopback capability

24-PIN DIP PACKAGE



SC11000CN
SC11001CN
SC11005CN

28-PIN PLCC PACKAGE



SC11001CV
SC11005CV

GENERAL DESCRIPTION

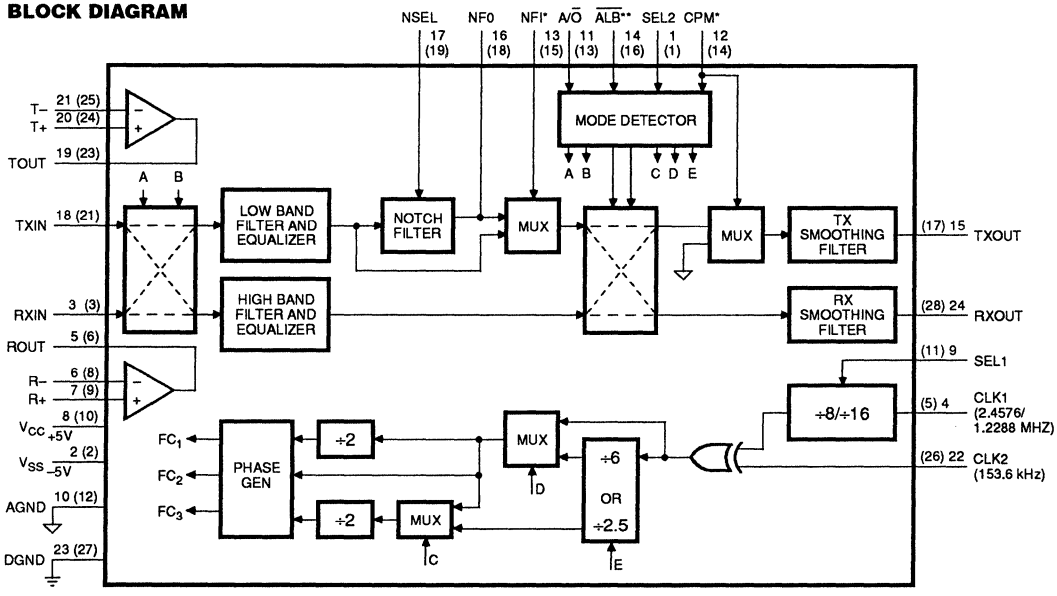
The SC11000, SC11001 and SC11005 modem filters are monolithic CMOS switched-capacitor filter circuits designed for use in full duplex 1200 and 2400 Bit Per Second modems. They meet the requirements of the Bell 212A, CCITT V.22 and V.22bis specifications and include high-band (2400 Hz) and low-band (1200 Hz) filters, half-channel compromise amplitude and group delay equalizers and smoothing filters for both bands. For CCITT V.22 and V.22bis applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. Also included in the filters are two uncommitted operational amplifiers that can be used for anti-aliasing filters or for gain control.

The SC11000 is pin and function compatible to the AMI S35212 and the Reticon R5632. Like the S35212, the high-band filter in the SC11000 can be scaled down by a factor of 6 so that it can be used to monitor call progress tones in an intelligent modem.

The SC11005 is pin and function compatible to the AMI S35212A. It contains all of the features of the SC11000, and like the S35212A, it contains an analog loopback mode—$\overline{\text{ALB}}$ (pin 14)—for testing the signal path.

The SC11001 is an enhanced version of the SC11005. In addition to all of the features of the SC11005, it contains two additional control pins, CPM (pin 12) and NFI (pin 13) that allow more accurate call progress monitoring and easier V.22 implementation without the need for external multiplexers or logic. Besides being able to scale the high-band filter by a factor of six, the low-band filter can be scaled by a factor of 2.5 for better centering over the call progress frequency range of 300 to 660 Hz. It also allows the unscaled high-band filter to be used for monitoring the modem answer tone, simplifying the design of full auto-dial/auto-answer modems.

BLOCK DIAGRAM



NOTES: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINS; NUMBERS IN ( ) ARE PLCC PINS. PLCC PINS (4), (7), (20), & (22) ARE NOT CONNECTED.

PINS 1, 4, 11, 12*, 13*, 17 AND 22 HAVE INTERNAL PULL-DOWN REGISTERS TO GROUND. PIN 14 HAS AN INTERNAL PULL-UP TO V_{CC}.

* FOR SC11001. PINS NOT CONNECTED ON SC11000 AND SC11005.

** FOR SC11001 AND SC11005. PINS NOT CONNECTED ON SC11000.

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1 (1)	SEL2	Call progress mode selection; SEL2 low for normal operation, SEL2 High scales down the high-band, filter by 6 for call progress monitoring
2 (2)	V_{SS}	Negative supply
3 (3)	RXin	Receive signal input
4 (5)	CLK1	Clock input 1; 2.4576 MHz with SEL1 high, or 1.2288 MHz with SEL1 low
5 (6)	Rout	Output of the R amplifier
6 (8)	R-	Inverting input to the R amplifier
7 (9)	R+	Noninverting input to the R amplifier
8 (10)	V_{CC}	Positive supply
9 (11)	SEL1	Selects clock frequency into pin 4; low for 1.2288 MHz, high for 2.4576 MHz
10 (12)	AGND	Analog ground
11 (13)	$A/\overline{O}$	Answer/originate mode selection; high for answer, low for originate
12 (14)	CPM	Enhanced call progress mode selection; CPM low for normal operation; CPM high scales down the low-band filter by 2.5 for enhanced call progress monitoring
13 (15)	NFI	Notch filter insert; low for notch filter bypass, high for inserting
14 (16)	$\overline{ALB}$	Analog loopback; high for normal operation, low to loopback TXin to RXout
15 (17)	TXout	Transmit signal output
16 (18)	NFO	Notch filter output
17 (19)	NSEL	Notch filter selection; low for 550 Hz, high for 1800 Hz
18 (21)	TXin	Transmit signal input
19 (23)	Tout	Output of the T amplifier
20 (24)	T+	Noninverting input to the T amplifier
21 (25)	T-	Inverting input to the T amplifier
22 (26)	CLK2	Clock input 2; 153.6 kHz
23 (27)	DGND	Digital ground
24 (28)	RXout	Receive signal output

Note: Pin numbers in ( ) refer to 28-lead PLCC pinout.

FUNCTIONAL DESCRIPTION

Low-Band Filter

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. See Figure 3 for the amplitude response of this filter. In the originate mode this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, will be in the test loop. In the Call Progress Monitoring mode with SEL2 (pin 1) high and CPM (pin 12) low, the center frequency of this filter is shifted down by a factor of 6 to 200 Hz. If pin 12 (CPM) is high, then the filter response will be scaled down by 2.5, moving the center frequency to 480 Hz.

Low-Band Delay Equalizer

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. See Figure 4 for the group delay response of the low-band filter cascaded with the low-band delay equalizer.

High-Band Filter

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. See Figure 5 for the amplitude response of this filter. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop. In the Call Progress Monitoring mode, with SEL2 (pin 1) high and CPM (pin 12) low, the center frequency will be shifted down by a factor of 6 to 400 Hz. If pin 1 is low or pin 12 is high, this filter operates in the normal data mode.

High-Band Delay Equalizer

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. See Figure 6 for the group delay response of the high-band filter cascaded with the high-band delay equalizer.

Transmit Smoothing Filter

The transmit smoothing filter is a first order low-pass switched-capacitor filter.

Receive Smoothing Filter

The Receive Smoothing Filter consists of a 2nd order low-pass switched-capacitor filter cascaded with a 2nd order, active RC, low-pass filter.

V.22 Notch Filter

The V.22 Notch Filter is a 2nd order switched-capacitor notch filter. The center frequency of the filter is at 550 Hz when NSEL (pin 17) is low and is shifted to 1800 Hz when NSEL is high. This filter is bypassed in the low-band if NFI (pin 13) is low. Its output, however, will always be available at pin 16 (NFO).

Uncommitted Operational Amplifiers

Two operational amplifiers—called the R amplifier and the T amplifier—are included as part of the SC11001 and SC11005. They are not used by the filter circuit and can be used, for example, as anti-aliasing filters or gain stages in a complete 212A modem circuit.

Analog Loop-Back

When $\overline{ALB}$ (pin 14) is low, the signal transmitted by the modem, TXin, is looped back to the modem through the RXout pin. If the low (high)-band filter/equalizer is to be tested, the A/$\overline{O}$ pin should be low (high). The receive smoothing filter is in this loop regardless of the A/$\overline{O}$ level. An internal pull up resistor keeps this pin high when it is not connected externally.

Answer/Originate Mode Selection

When A/$\overline{O}$ (pin 11) is low, the modem operates in the originate mode, transmitting in the low-band and receiving in the high-band. If A/$\overline{O}$ is high, the modem operates in the answer mode, transmitting in the high-band and receiving in the low-band. An internal pull down resistor keeps this pin low when it is not connected externally.

Clock Selection

SEL1 (pin 9) is used to select the correct internal divider, depending on the frequency of the external clock. SEL1 is set high for use with a 2.4576 MHz clock input on CLK1 (pin 4), and set low for a 1.2288 MHz input on CLK1 (pin 4). If a 153.6 kHz clock is used on CLK2 (pin 22), CLK1 (pin 4) and SEL1 (pin 9) should be left open.

Normal/Call Progress Mode

When SEL2 (pin 1) and CPM (pin 12) are low, the filter operates in the normal data mode—the modem mode. When either pin is high, the filter operates in the Call Progress Monitoring mode. When SEL2 is high and CPM is low, the center frequencies of both the low-band and the high-band filters are shifted down to one sixth of the frequencies used in the normal data mode. SEL2 is internally pulled down to keep it at a low level when it is not connected externally.

When CPM is high, the low-band filter is scaled down by a factor of 2.5 (Figure 7) and RXout is either the output of the scaled low-band filter, or the unscaled high-band filter, depending on the logic levels at $\overline{ALB}$ (pin 14) and A/$\overline{O}$ (pin 11) as shown in Table 1.

Transmit Squelch in Call Progress Mode

When CPM is high—Call Progress Mode—the input of the transmit smoothing filter is disconnected and shorted to ground, squelching the transmitter. In the handshake sequence of a 212A modem, this feature can be used to eliminate any transmit signal output. An internal pull down resistor keeps the CPM pin low when it is not connected externally.

SEL2 (pin 1), CPM (pin 12), $\overline{ALB}$ (pin 14), and A/$\overline{O}$ (pin 11) control the modes of operation of the filter as shown in Table 1. For each combination of these pins, the table shows to which filter each input or output is connected. "L" refers to the low-band filter with the response shown in Figure 2. "H" is used to denote the high-band filter as characterized in Figure 2. When L or H are divided by a factor (6 or 2.5), this is indicated as L/6, H/6, etc., meaning the frequency response is scaled down by 6.

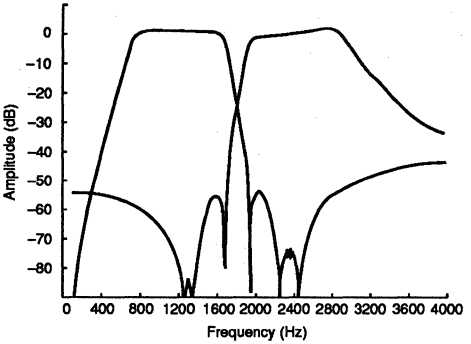


Figure 2. Low-Ban and High-Band Amplitude Responce—Normalized

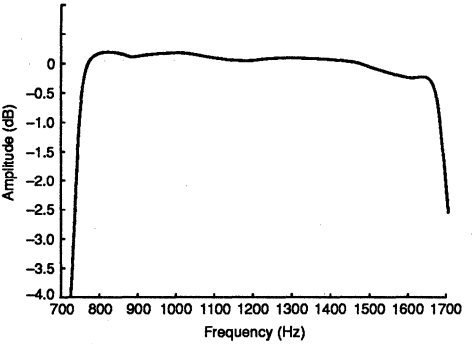


Figure 3. Low-Band Response—Normalized

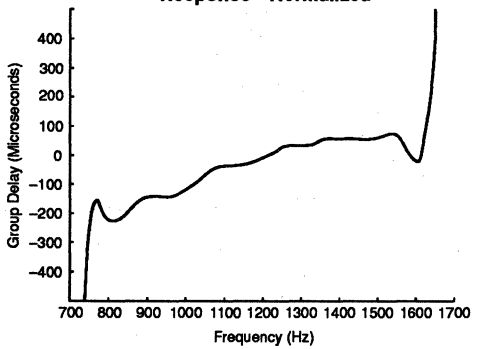


Figure 4. Low-Band Group Delay

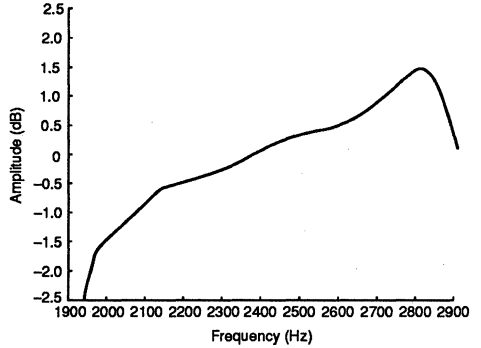


Figure 5. High-Band Response—Normalized

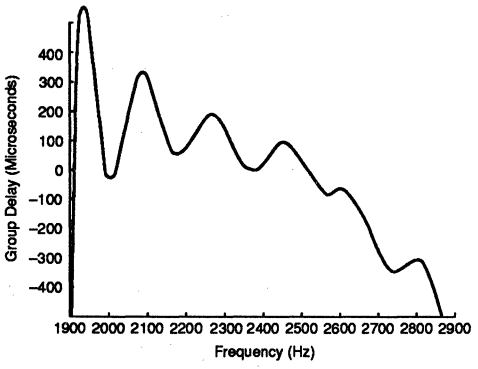


Figure 6. High-Band Group Delay (Hz)

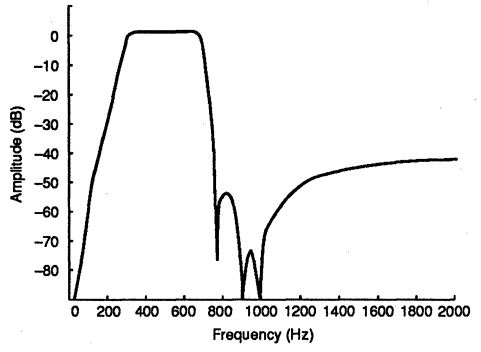


Figure 7. Low-Band Divided by 2.5 Amplitude Response—Normalized

Mode	CPM	SEL2	$\overline{ALB}$	A/$\overline{O}$	TXin	TXout	RXin	RXout
0	0	0	1	0	L	L	H	H
1	0	0	1	1	H	H	L	L
2	0	0	0	0	L	L	H	L
3	0	0	0	1	H	H	L	H
4	0	1	1	0	L/6	L/6	H/6	H/6
5	0	1	1	1	H/6	H/6	L/6	L/6
6	0	1	0	0	L/6	L/6	H/6	L/6
7	0	1	0	1	H/6	H/6	L/6	H/6
8	1	X	1	0	—	SQT	(L/2.5 + H)	H
9	1	X	1	1	H	SQT	L/2.5	L/2.5
10	1	X	0	0	—	SQT	(L/2.5 + H)	L/2.5
11	1	X	0	1	H	SQT	L/2.5	H

Note: SQT means the transmitter output is squelched.
"L" refers to center frequency of 1200 Hz.
"H" refers to center frequency of 2400 Hz.
— means no filter connection
+ means connection to both filters
X means "don't care"

By switching between modes 8 and 10, the filter can be used to detect reception of the call progress tones in the L/2.5 band as well as the answer tone in the H band.

Table 1. Operating Modes

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	7 V
Supply Voltage, V_{SS}	–7 V
Input Voltage-Analog Signals (Pins 3, 6, 7, 18, 20, 21)	V_{CC} +0.6 V V_{SS} -0.6 V
Input Voltage-Digital Signals (Pins 1, 4, 9, 11, 12, 13, 14, 17, 22)	V_{CC} +0.6 V V_{SS} -0.6 V
Storage Temperature Range	–65 to +150°C
Maximum Power Dissipation @ 25°C (Note 2)	500 mW
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range (Plastic)	0 to +70°C

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", the device should not be operated at these limits. The table of "Electrical Characteristics" provides actual operating limits.
2. Power dissipation temperature derating—plastic "N" package: –12 mW/°C from 65°C to 85°C.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ±10%, V_{SS} = –5 V ±10%

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	-5.0	–5.5	V
I_{CC}	Quiescent Current	No Load		7.5	15	mA
I_{SS}	Quiescent Current	No Load		7.5	15	mA
V_{IH}	High Level Input Voltage; Digital Signal Pins 1, 4, 9, 11, 12, 13, 14, 17, 22		2.0			V
V_{IL}	Low Level Input Voltage; Digital Signal Pins 1, 4, 9, 11, 12, 13, 14, 17, 22				0.8	V
V_{OMAX}	Output Signals, Pins 5, 15, 16, 19, 24	V_{CC} = +5 V, V_{SS} = -5 V R_L = 10 kΩ (Pins 5, 19) R_L = 20 kΩ (Pins 15, 16, 24)	±3			V

PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = +5 V, V_{SS} = –5 V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Noise RXout, TXout			30	33	dBrnCo
Crosstalk		55	60		dB
Total Harmonic Distortion			0.3		%
Dynamic Range			70		dB
Adjacent Channel Rejection Low band High band		 55 55	 65 75	 	 dB dB
Passband Gain at Center Frequency (1200 Hz, 2400 Hz)		–1		+1	dB
Relative Gain—Low Band Reference = 1200 Hz	@ 400 Hz @ 800 Hz @ 1600 Hz @ 1800 Hz @ 2000 Hz @ 2400 Hz @ 2800 Hz	 –1 –1.5 	 	–35 +1 +1 –18 –48 –55 –50	dB dB dB dB dB dB dB
Relative Gain—High Band Reference = 2400 Hz	@ 800 Hz @ 1200 Hz @ 1600 Hz @ 2000 Hz @ 2800 Hz @ 3200 Hz @ 3500 Hz	 –2.5 0 	 	–50 –53 –50 +0.5 +2.5 –10 –20	dB dB dB dB dB dB dB
Relative Gain—Low Band NFI = High	@ 550 Hz, NSEL = Low @ 1800 Hz, NSEL = High		–40 –40		dB dB

APPLICATIONS

Modes of Operation

The SC11000, SC11001 and SC11005 filters can be operated in three basic modes—a normal data mode, a test mode and a call progress monitor mode.

Normal Data Mode

Figures 8 through 11 illustrate the signal flow diagrams for the filter in the normal data mode for either a 212A or a V.22 modem. In the originate mode, the transmit signal goes through the low-band filter and the receive signal goes through the high-band filter. In the answer mode, the transmit signal goes through the high-band filter and the receive signal goes through the low-band filter.

Test Mode

The filter can be tested by entering the analog loopback mode as illustrated in Figures 12 and 13. In this mode, the transmit signal is looped back to the RXout pin after going through either the low-band filter or the high-band filter, depending on originate or answer mode selection. The analog loopback mode facilitates testing of the modem locally, without having to make a data call.

Call Progress Monitor Mode

The filter operates in one of two different call progress monitor modes, depending on whether the SEL2 or CPM pin is taken high. If SEL2 is taken high, the center frequency of both the low-band and high-band filters is shifted down by a factor of 6 and the bandwidth of the filters is also reduced by a factor of 6. Thus the high-band filter is shifted down to 400 Hz ±80 Hz while the low-band filter is shifted down to 200 Hz ±80 Hz. By selecting the originate mode, the receive signal will go through the modified high-band filter which now has a pass-band of approximately 300 Hz to 480 Hz. This allows precision dial tone of 350/440 Hz as well as audible ringing tone of 440/480 Hz to pass. However, only a portion of the busy or reorder tone of 480/620 Hz will pass through. An external energy detector circuit, combined with a method of cadence and timing determination, distinguishes between different conditions on the line during establishing a call.

The SC11001 features an additional mode for monitoring the call progress tones. This mode is initiated by taking the CPM pin high. Two deficiencies, inherent in the first mode described above, are overcome in this enhanced mode. First, the pass-band is more accurately centered over the call progress tone frequencies because the low-band filter is scaled down by a factor of 2.5. The low-band filter thus has a pass-band of 290 Hz to 670 Hz which allows the busy tone to pass through completely. Secondly, since the high-band filter is not scaled, answer tone can be easily monitored. The receive signal is connected to both the high-band filter and the scaled low-band filter. By toggling the $\overline{ALB}$ pin between high and low levels, either the answer tone or the call progress tone can be monitored on the RXout pin.

Figures 14 and 15 show the signal flow diagrams in the call progress monitor mode. A method for determining conditions on the line during establishing a call is described in the following section.

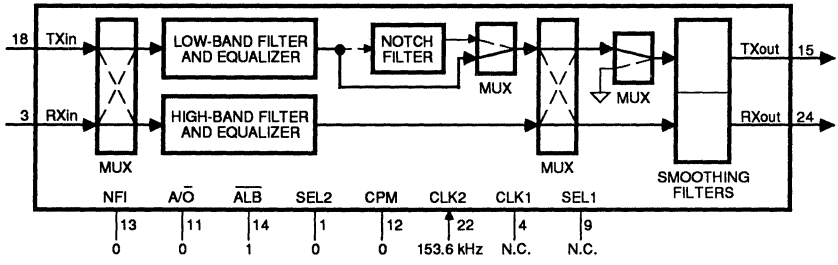


Figure 8. 212A Originate Mode

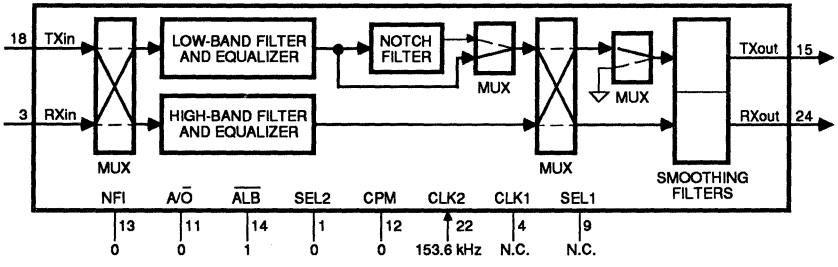


Figure 9. 212A Answer Mode

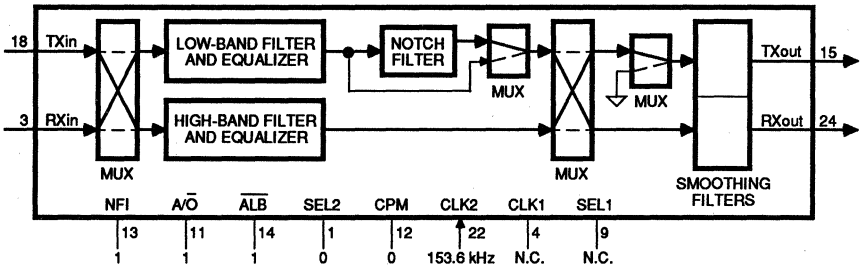


Figure 10. V.22 Answer Mode

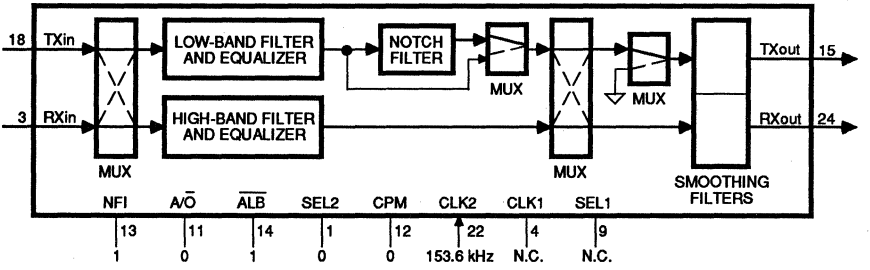


Figure 11. V.22 Originate Mode

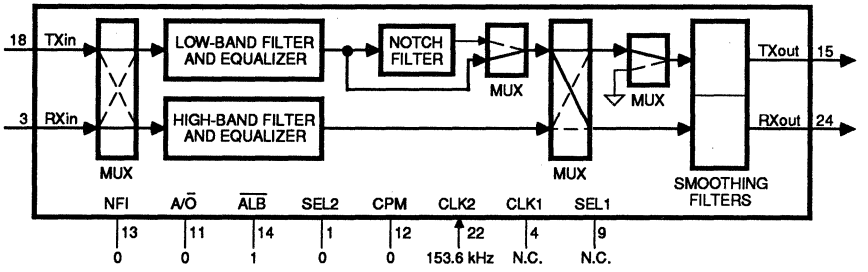


Figure 12. 212A Analog Loopback Mode Using Low-Band Filter (Originate Mode)

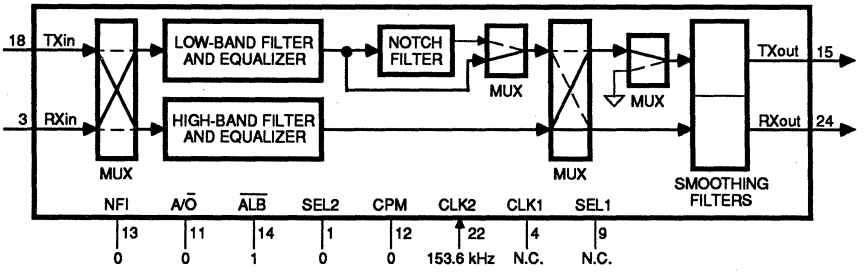


Figure 13. 212A Analog Loopback Mode Using High-Band Filter (Answer Mode)

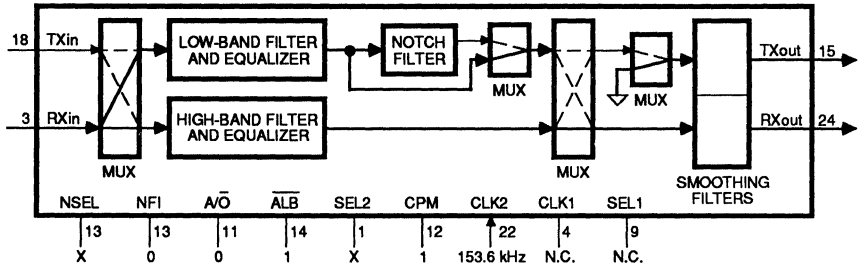


Figure 14. Call Progress Monitor Mode: Monitoring Answer Tone/Voice

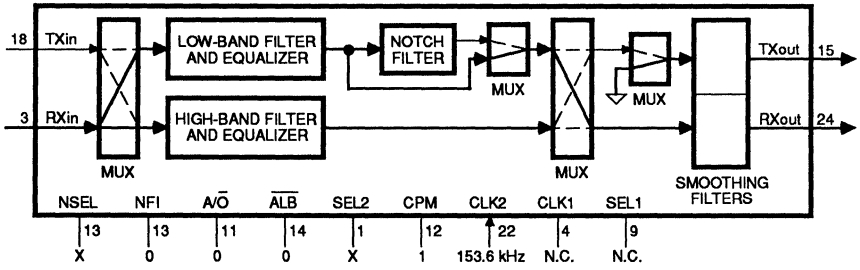


Figure 15. Call Progress Monitor Mode: Monitoring Call Progress Tones

Circuit Description

In the circuit of Figure 16, op amps U_1 and U_2 and resistors R_8 thru R_{13} form a 2 to 4 wire converter that seperates the line signal into the transmit and receive components. The receive signal is connected to the RXin input of the SC11001 filter. In the call originate mode, it goes through the high-band filter and comes out on the RXout pin. For call progress monitoring the low-band filter operates in the scaled mode, thus filtering the receive signal over the range of 290 Hz to 670 Hz. Op amps U_3 and U_4, comparator U_5 and associated discrete components form the energy detector. U_3 operates as a full wave rectifier. U_4 is a buffer that drives a low pass filter formed by R_{18} and C_4. The filtered signal is compared to a level set by R_{19} and R_{20}. The output of U_5 goes high if the signal level exceeds the level set by R_{19} and R_{20}. This output corresponds to the cadence information in the call progress tone signals and can be sampled by the controller according to the detection algorithm.

The rest of the circuitry in Figure 16 performs the functions of the DAA. Transformer T_1 provides isolation and sinks the line current in the off hook state. R_1, R_2, V_1, Z_3 and Z_4 provide surge protection. Relay KR_1 and transistor Q_1 control on hook/off hook condition. C_1, R_3, Z1, Z_2, D_1 and OC_1's internal diode limit and rectify the high voltage AC ringing signal. OC_1 provides isolation. R_4 and C_2 filter the rectified ring signal and Schmidt Trigger IC. U_6 converts it into a logic level for the controller.

A Call Progress Monitoring Application

Figure 16 shows a schematic for using the SC11001 filter in a call progress monitoring application. Specifically, this arrangement is well suited for implementing an intelligent 212A or V.22 modem. The modem can be designed to be either stand-alone with RS-232 interface to DTE or integrated in a computer with a parallel bus interface. It is assumed that a controller is available that can control the various operating modes of the filter, monitor the output of the energy detector and ring indicator, and control the switch-hook relay in the Data Access Arrangement (DAA). This application illustrates how the modem filter can be used with minimum of external circuitry to implement a fully automatic call establishment procedure.

Table 2 summarizes various call progress tone frequencies and their cadences. A call progress monitoring algorithm based on timing and cadence characteristics is described in the flow chart of Figure 17.

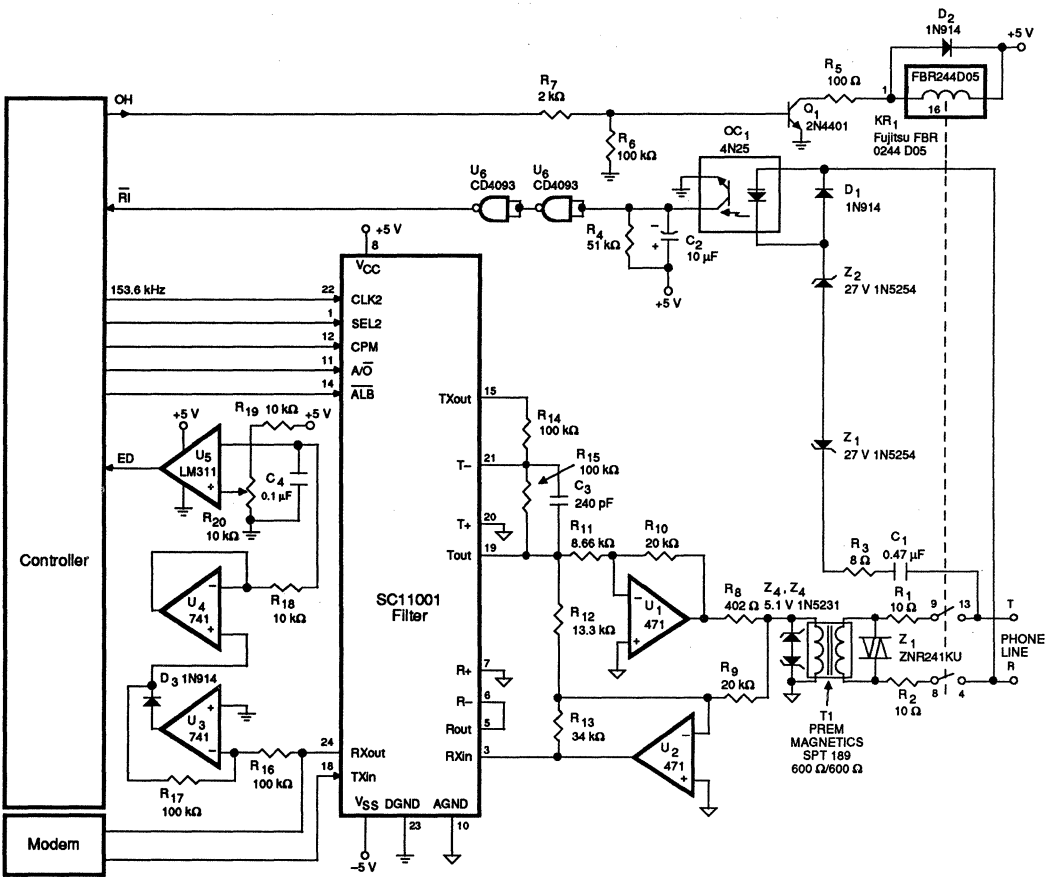


Figure 16. A Call Progress Monitoring Application

Call Progress Tone	Frequency (Hz)	Cadence
Dial tone	350 + 440* 400, 425 600 x 120 IPS**	Continuous steady tone
Audible ring	440 + 480* 400, 450 420 x 40 IPS 400 x 25 IPS	2 s on/4 s off 1 s on/3 s off
Busy (station)	480 + 620* 400, 425, 450 600 x 120 IPS	0.5 s on/0.5 s off
Busy (circuit)	Same as above	0.25 s on/0.25 s off
Off hook alert	Multifrequency	1 s on/1 s off

*Precision tone specified by AT&T
**IPS means interruptions per second

Table 2. Call Progress Tone Characteristics

Detection Algorithm

Figure 17 shows the flowchart of a detection algorithm that utilizes the features provided in the SC11001 filter and that uses the cadence information contained in the call progress tones to determine the status of the line. The main criterion in this algorithm was the high degree of reliability it provides, rather than the speed in which it executes. For instance, dial tone is detected only when the output of the energy detector is continuously high for at least one second. If dial tone is not detected within 5 seconds of going off hook, the call is aborted. Many dialers do not wait for the initial dial tone and begin dialing as soon as going off hook. This is termed blind dialing and is avoided by this algorithm.

Once dial-tone is detected, the first digit is dialed using the tone mode. Provision is made to check the absence of the dial-tone after the digit is dialed. If dial-tone remains on the line, the controller can either hang up the line or try to dial using rotary pulse dialing. If dial-tone is absent, the rest of the digits can be pulse dialed.

The algorithm waits for 1 second after dialing is done to monitor the energy detector. This insures that any clicks on the line will not cause a false detection. The $\overline{ALB}$ pin of the filter is then toggled at a 100 ms rate and the energy detector output is

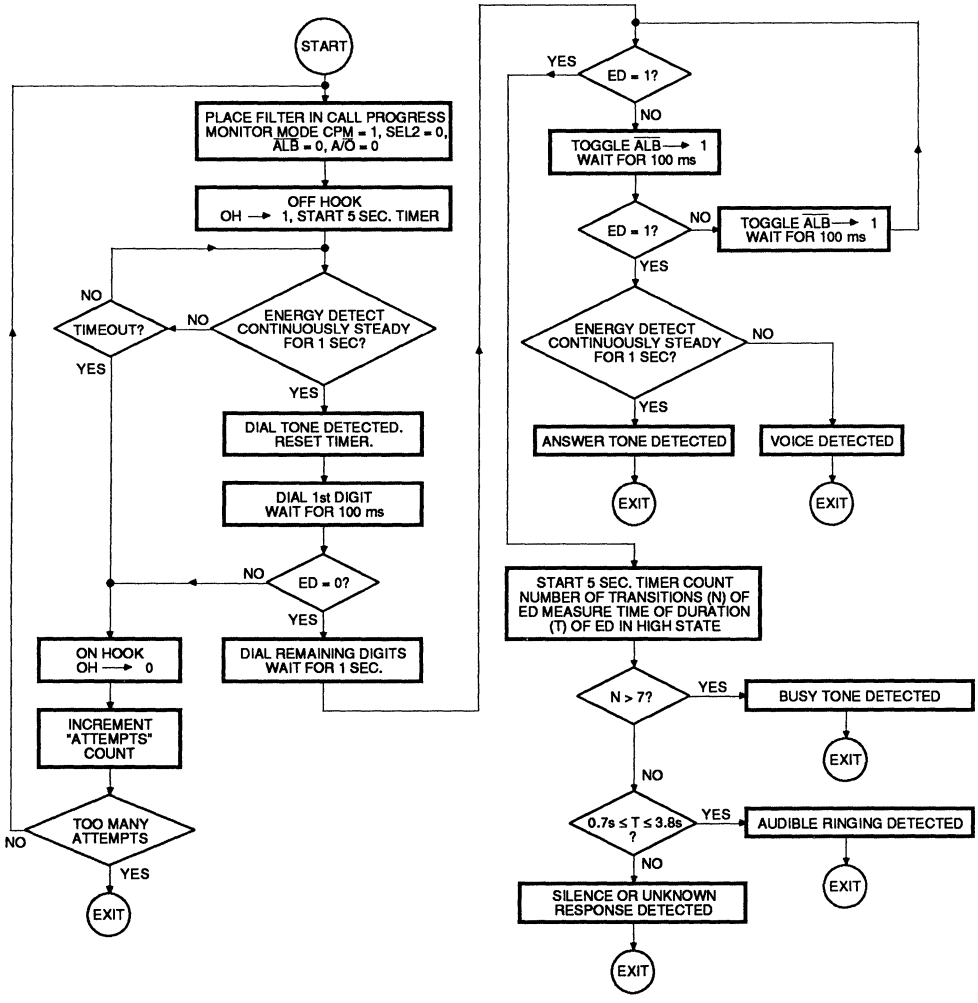


Figure 17. Call Progress Monitoring Algorithm

sampled to see if there is energy in the call progress band or in the voice band. If energy is detected in the call progress band, a 5 second timer is started and the number of transitions of the ED output are counted (N). The cumulative duration in which the ED output is in the high state is also measured (T).

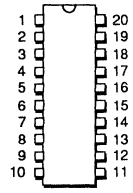
The algorithm makes a determination of various conditions based on N and T. The line is determined to be busy if N exceeds 7. If N is less than 7 and T is in the range of 0.7 seconds to 3.8 seconds, the signal is determined to be audible ringing. The controller can then count the ring cycles or start a timer. It can choose to hang up if the timer overflows or if the number of ring cycles exceeds a preset value. Any other value of N or T is classified as unknown response and it is left to the controller to take the next action.

If energy is detected in the high band, ED output is monitored to see if it is continuously high for at least one second. If so, this is interpreted as the distant modem answertone, indicating that the connection is made. If not, it indicates either silence or voice. In either case the controller can terminate the call and take the next step. Minor variations of this algorithm or fine tuning of the decision values can provide the designer with the flexibility he needs to deal with different situations. It should be emphasized that the algorithm does not stand alone and must be integrated in the application software for satisfactory performance.

FEATURES

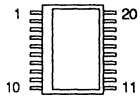
- ☐ Full duplex answer and originate operation
- ☐ All filters and Hybrid circuits on chip
- ☐ Analog loopback capacity
- ☐ Output drives 600 Ω at 0 dbm (–9 dbm for SC11003)
- ☐ Lower power CMOS design with power down mode

20-PIN DIP PACKAGE



SC11002CN
SC11003CN

20-PIN SOIC PACKAGE



SC11002CM
SC11003CM

GENERAL DESCRIPTION

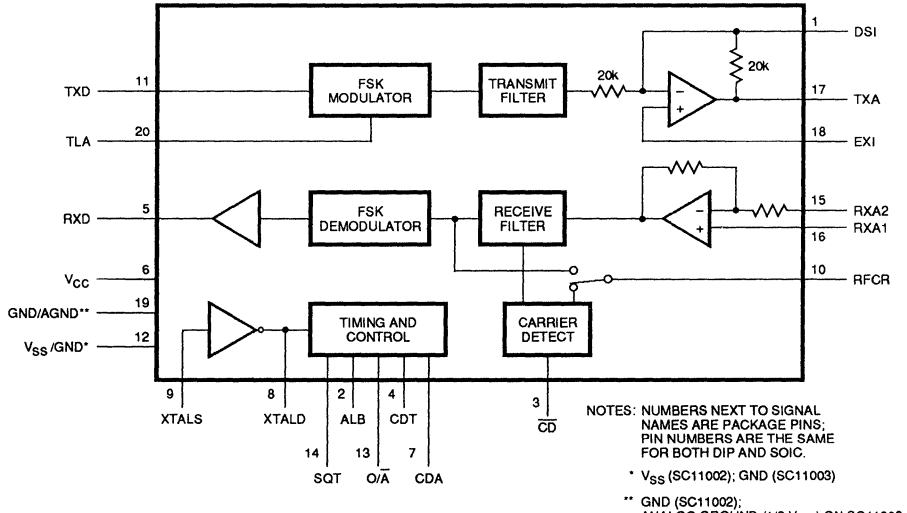
The SC11002 and SC 11003 are full duplex, 0 to 300 Bit Per Second single chip modems compatible with Bell 103 specifications. They are intended for data communications over the general switched telephone network and can also be used on other voice-band channels.

The SC11002 requires +5 volts and –5 volts; the SC11003 requires a single +5 volt supply. These 3-micron, CMOS, switched capacitor filter circuits are pin compatible with the National Semiconductor 74HC942 (SC11002) and the 74HC943 (11003) and are a functional replacement for Texas Instruments' TMS99532.

Included on chip are high-band and low-band filters, an FSK modulator and demodulator and a line driver and hybrid for directly driving a 600 Ω phone line.

Applications include integrated and stand-alone low speed modems for terminals, personal computers and small business computers and as built-in modems used for remote diagnostics in electronic test systems, computer installations, industrial control systems and business machines. Since they are CMOS, they are ideal as built-in modems for portable or lap-top computers.

BLOCK DIAGRAM



NOTES: NUMBERS NEXT TO SIGNAL NAMES ARE PACKAGE PINS; PIN NUMBERS ARE THE SAME FOR BOTH DIP AND SOIC.

* V_{SS} (SC11002); GND (SC11003)

** GND (SC11002); ANALOG GROUND (1/2 V_{CC}) ON SC11003

PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	DSI	Driver summing Input; used to transmit externally generated tones such as DTMF dialing signals. When not used, this pin should be left open. See functional description for details on how to use this input.
2	ALB	Analog loopback; low for normal operation, high for looping back the modulator output to the demodulator input. If ALB and SQT are simultaneously held high, the chip powers down.
3	$\overline{CD}$	Carrier detect output; goes low when carrier is detected.
4	CDT	Carrier detect timing input; a capacitor on this pin sets the time interval that the carrier must be present before CD goes low. For testing purposes, if this pin is connected to Pin 12, then RFCR will be connected to the output of the receive filter.
5	RXD	Received data—the data output.
6	V_{CC}	Positive supply.
7	CDA	Carrier detect adjust input; this is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB. For testing purposes, if this pin is connected to pin 12, the Transmit filter can be tested by using TLA as an input drive from a low output resistance signal source and TXA as the output.
8	XTALD	Crystal oscillator output; should be connected to a 3.579545 MHz crystal. It can also be driven by an external clock.
9	XTALS	Crystal oscillator input; should be connected to a 3.579545 MHz crystal. If external clock is used; this pin must be left open.
10	RFCR	Receive Filter/Carrier Rectifier; this is normally connected to the output of the carrier rectifier. If CDT is connected to Pin 12, then this pin is disconnected from the rectifier and instead it will be connected to a high impedance output of the receive filter. It may thus be used to evaluate filter performance. For normal modem operation, RFCR is AC grounded (Pin 19) via a 0.1 µF bypass capacitor.
11	TXD	Transmit data—the data input.
12	V_{SS}/GND	Negative supply: -5 V for SC11002, ground for SC11003.
13	O/$\overline{A}$	Originate/Answer mode select; when high (low), this pin selects the originate (answer) mode of operation.
14	SQT	Squelch Transmitter; this disconnects the modulator output from the line driver input when held high. The EXI input, however, remains active. If SQT and ALB are held high simultaneously, the chip will power down.
15	RXA2	Receive analog (2); RXA2 and RXA1 are analog inputs. When connected as recommended, they produce a balanced hybrid.
16	RXA1	Receive analog (1); see RXA2 for details. If not used it MUST be tied to Pin 19.
17	TXA	Transmit analog output; line driver output.
18	EXI	External input; this is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose, it should be connected to Pin 19. See functional description for further details on how to use this input.
19	GND/ GNDA	Ground (0 V) for SC11002. Analog ground (1/2 V_{CC}) for SC11003.
20	TLA	Transmit level adjust; a resistor from this pin to V_{CC} sets the transmit level.

Note: Pin Numbers are identical for both DIP and SOIC packages.

FUNCTIONAL DESCRIPTION

SC11002/SC11003 can be used to transmit and receive serial digital data over general switched telephone networks, leased lines, or other equivalent narrow band channels. Up to 300 bits per second can be transmitted and received simultaneously.

Transmitter

As shown in the block diagram, the digital input data (TXD) is first modulated by the frequency shift keying (FSK) modulator. FSK modulation is performed according to Bell 103 specifications as listed in Table 1.

Table 1. Bell 103 Transmit and Receive Tones

	High Band	Low Band
Mark	2225 Hz	1270 Hz
Space	2025 Hz	1070 Hz

To separate the transmit and receive signals, the originating modem transmits in the low band while the answering modem transmits in the high band. The transmit filter smooths and band limits the modulator output. The nominal center frequency of this filter is placed at 2125 Hz or 1170 Hz depending on whether the modem is in the answer mode or in the originate mode, respectively.

The output of the transmit filter goes through the line driver and appears at TXA (Pin 17). The signal level at TXA can be controlled by connecting a resistor between TLA (Pin 20) and V_{CC} (Pin 6). The open circuit voltage on Pin 20 is 0.1 V_{CC}. The transmitted power levels shown in Table 2 refer to the power delivered to a 600 Ω load from the external 600 Ω source impedance. The voltage on the load is half the TXA voltage.

Table 2. Resistor Values for Adjustment of the Transmit Level at V_{CC} = 5.0 V.

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (RTLA)
0	–12	Open Ckt
1	–11	19800 Ω
2	–10	9200 Ω
3	–9	5490 Ω
4*	–8*	3610 Ω
5*	–7*	2520 Ω
6*	–6*	1780 Ω
7*	–5*	1240 Ω
8*	–4*	866 Ω
9*	–3*	562 Ω
10*	–2*	336 Ω
11*	–1*	150 Ω
12*	0*	0 Ω

*Applies only to SC11002.

Receiver

The analog signal received from the line is buffered by the hybrid circuit and filtered by the receive filter. The receive filter is similar to the transmit filter except that it always operates at the band opposite to the transmit filter band. When the transmit filter operates at the high band, the receive filter operates at the low band and vice versa. The output of the receive filter is hard limited and demodulated by the FSK demodulator. The demodulator output appears at RXD (Pin 5).

Carrier Detector

An adaptive level detector responds to the presence of signal energy within the receive band and generates an active low logic level on the CD output (Pin 3). This circuit has a built-in hysteresis of 2 dB, minimum. Typically, CD is activated when the received signal power exceeds –44 dBm (V_{ON} = 4.9 mV_{rms} and CD is deactivated when the signal drops below –47 dBm V_{OFF} = 3.5 mV_{rms}). This hysteresis prevents oscillatory operation of the carrier detector when the received signal is close to the detection threshold.

Carrier Detect Thresholds

The threshold levels can be changed by applying a voltage to CDA (Pin 7) according to the equation below:

$V_{CDA} = 244 \times V_{ON}$ (V)

$V_{CDA} = 345 \times V_{OFF}$ (V)

V_{CDA} is referenced to Pin 19

The open circuit voltage on Pin 7 is 0.24 V_{CC}.

Converting V_{ON} and V_{OFF} to equivalent power level (across a 600 Ω resistor) in dBM

$$V_{CDA} = 189 \times 10^{P_{ON}/20} \text{ or}$$

$$P_{ON} = 20 \log_{10}\left(\frac{V_{CDA}}{189}\right)$$

$$V_{CDA} = 267 \times 10^{P_{OFF}/20} \text{ or}$$

$$P_{OFF} = 20 \log_{10}\left(\frac{V_{CDA}}{267}\right)$$

where P_{ON} and P_{OFF} are in dBm and V_{CDA} is in Volts.

Carrier Detect Timing

To reduce the effects of impulse noise and false triggering of the carrier detector, CD only goes low (active) when a carrier is detected and present for at least a time equal to T_{ON}. Also, to deactivated CD (i.e., going from low to high), the carrier must be removed for at least a time equal to T_{OFF}. T_{ON} and T_{OFF} can be adjusted by proper selection of the capacitor on CDT (Pin 4) according to the following equations:

$T_{ON} \cong 6.4 \times C_{CDT}$

$T_{OFF} \cong 0.54 \times C_{CDT}$

where C_{CDT} is in μF and T_{ON} and T_{OFF} are in seconds.

Line Hybrid

To attenuate the transmitted signal at TXA before it is fed back to the receiver input, TXA can be connected externally to RXA2 and also connected via a 600 Ω resistor to RXA1.

If the line impedance is also 600 Ω, then the transmit signal will appear as a common mode signal to the receiver and will effectively be eliminated. However, because the line impedance characteristics vary considerably, a perfect match with a fixed resistor rarely occurs and part of TXA is fed back to the receiver.

Transmit Squelch

When SQT is held high, the transmitter will be squelched and only the signals at EXI or DSI, if any, may be transmitted. See DSI below.

Analog Loopback

When ALB is held high, the output of the line driver is looped back to the input of the receive filter. This feature can be used for testing the modem. If the modem is in the originate mode, then the transmit and receive filters will be tuned to the low band. On the other hand, when the modem is in the Answer mode, both filters will tune to the high band.

Originate/Answer Modes

When the modem is in the originate mode ($O/\overline{A}$ = high), it will transmit in the low band and receive in the high band. This situation is reversed when the modem is in the answer mode ($O/\overline{A}$ = low).

Power Down Mode

To power down, SQT and ALB should be held high simultaneously.

DSI

This input can be used to transmit externally generated signals, such as DTMF tones, while the modem is in the squelched mode. The external tone should be capacitor coupled through a resistor into this pin. The gain of the transmit amplifier will then be determined by the ratio of the on-chip feedback resistor (typically 20 kΩ) and the external series resistor. Since the on chip resistor value can vary by ±25%, it is recommended that the EXI pin be

used as described below for accurate control of the transmitted tone level. When this pin is not used, it should be left open.

EXI

This input can be used to transmit externally generated signals, such as DTMF tones, while the modem is in squelched mode with DSI left open. The external tone should be capacitor coupled into this pin with a resistor (typically 100 kΩ) connected between this pin and the analog ground (Pin 19). Used in this manner, the transmitted tone level is twice the input tone level since the transmit amplifier is configured internally as a gain of 2 stage. When this pin is not used, it should be connected to Pin 19.

RFCR

This output pin is normally connected to the output of the full-wave rectifier of the carrier detect circuit. To test the output of the receive filter, CDT should be connected to Pin 12 to disable the rectifier circuit. In this case, RFCR will be connected to the receive filter output and can be used for testing the receive filter.

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS} SC11002 Only	–6 V
DC Input Voltage SC11002	V_{SS}–0.6 to V_{CC}+0.6 V
DC Input Voltage SC11003	–.6 V to V_{CC} to +.6 V
Storage Temperature Range	–65 to 150°C
Power Dissapation (Note 3)	500 mW
Lead Temperature (soldering 10 sec.)	300°C

OPERATING CONDITIONS

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient Temperature	SC11002C, SC11003C	0		70	°C
T_A	Ambient Temperature	SC11002E, SC11003E	–40		85	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage	SC11002 Only	–4.5	–5.0	–5.5	V
GND	Ground			0		V
GNDA	Analog Ground	SC11003 Only		1/2 V_{CC}		V
F_C	Crystal Frequency		3.576	3.5795	3.583	MHz
T_R, T_F	Input Rise or Fall Time				500	ns

DC ELECTRICAL CHARACTERISTICS (Note 4)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		3.15			V
V_{IL}	Low Level Input Voltage				1.0	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert = 20\ \mu A$ $\lvert I_{OUT} \rvert = 4$ mA, $V_{CC} = 4.5$ V	V_{CC}–0.1 3.7	V_{CC}		V V
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert = 20\ \mu A$ $\lvert I_{OUT} \rvert = 4$ mA, $V_{CC} = 4.5$ V $\lvert I_{OUT} \rvert = 12$ mA (Pin 3)			0.1 0.4 0.5	V V V
I_{IN}	Input Current	$V_{IN} = V_{CC}$ or GND			±1.0	µA
I_{CC}	Quiescent Supply Current	ALB or SQT = GND Transmit Level = –9 dBm		8		mA
I_{CC}	Power Down Supply Current	ALB = SQT = V_{CC} $V_{IH} = V_{CC}$, V_{IL} = GND		400		µA

Notes 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating: Plastic package: –12mW/C from 65°C to 85°C.
Ceramic package: –12mW/C from 100°C to 125°C
4. Min and max values are valid over the full temperature and operating voltage range.
Typical values are for 25°C and ±5 V operation.

PERFORMANCE CHARACTERISTICS

Unless otherwise specified, all specifications apply to the test circuit shown in Figure 1. The demodulator specifications apply to operating SC11002 with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better that the SC11002 modulator. Typicals are at 25°C and ±5 v.

Parameter	Conditions	Min	Typ	Max	Units
Transmitter					
Carrier Frequency Error				4	Hz
Power Output Delivered to Line	V_{CC} = 5 V, RL = 1200 Ω RTLA = 0 (SC11002 = 5490 (SC11003) RTLA open		0 –9 –12		dBM dBm dBm
2nd Harmonic Energy	RTLA open		–60		dBm
Receive Filter and Hybrid					
Hybrid Input Resistance (pins 15 and 16)			100		kΩ
RFCR Output Resistance	Pin 10, No External Capacitor		30		kΩ
Adjacent Channel Rejection	TXD = GND or V_{CC} Input to RXA1; RXA2 = GND (SC11002) = GNDA (SC11003)	60 60			dB dB
Demodulator (Including hybrid, receive filter and discriminator)					
Maximum Carrier Amplitude			–12		dBm
Minimum Carrier Amplitude			–47		dBm
Dynamic Range			35		dB
Bit Jitter	SNR = 30 dB Input = –38 dBm Baud Rate = 300		100		µs
Bit Bias Distortion			5		%
Carrier Detect Trip Points	CDA = 1.2 V, Off to On Referenced to Pin 19 On to Off		–44 –47		dBm dBm

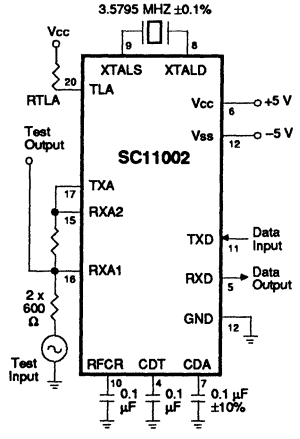


Figure 1. SC11002 AC Specification Circuit

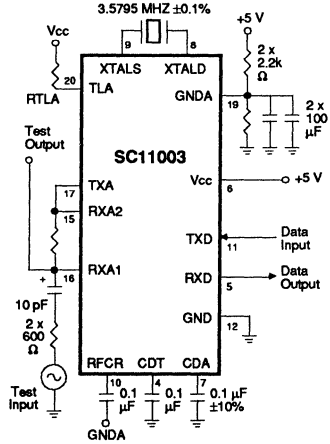


Figure 2. SC11003 AC Specification Circuit

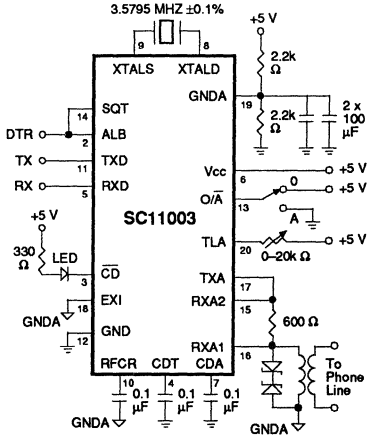


Figure 3. Simple, Direct Connect, 300 Baud Modem

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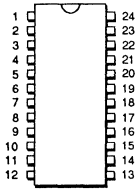
FEATURES

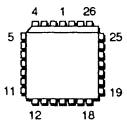
- ☐ All modulators, demodulators, and filters with compromise equalizers on chip
- ☐ Call progress mode, tone generators for DTMF, V.22 guard and calling tones
- ☐ On-chip hybrid
- ☐ Bell 212A and CCITT V.22 compatible; includes notch filter
- ☐ SC11014 supports V.21
- ☐ Serial control interface
- ☐ Programmable audio port
- ☐ All loopback diagnostics

24-PIN DIP PACKAGE



SC11004CN
SC11014CN

28-PIN PLCC PACKAGE



SC11004CV
SC11014CV

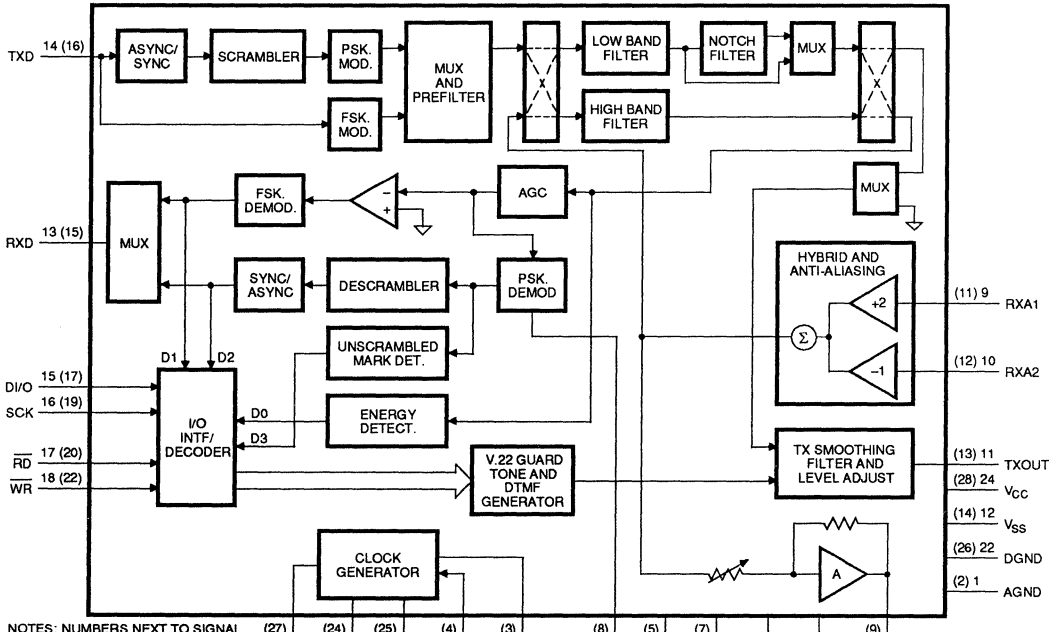
GENERAL DESCRIPTION

The SC11004 is a complete 300/1200 Bit Per Second (bps) modem. All signal processing functions needed for a full duplex, 300/1200 bps, Bell 103/212A or V.22 compatible modem, including the FSK and PSK modulators and demodulators and high-band and low-band filters with compromise amplitude and group delay equalizers are integrated on a single chip.

Built with Sierra's proprietary CMOS process that allows analog and digital functions to be combined on the same chip, the SC11004 features call progress monitoring and DTMF generation and V.22 guard tones. A two-to-four wire hybrid is also included on chip, simplifying the interface to a data access arrangement (DAA). An external hybrid may also be used, if desired. The SC11004 also includes analog, digital, and remote digital loopback diagnostics for self testing. The SC11014 contains all of the features of the SC11004 and, in addition, supports V.21 operation.

With the addition of a digital controller, such as an 8-bit microcontroller and a DAA, a highly cost effective, integrated, intelligent modem can be built. When used with the Sierra SC11007 modem controller—an 8-bit processor combined with a UART—a complete Hayes command set compatible modem can be configured, occupying minimum board area. All that is needed for stand-alone applications is the SC11004/14 modem, the SC11008 controller, a DAA and an RS232-interface. They operate in synchronous or asynchronous mode and handle 8, 9, 10 or 11 bit words.

BLOCK DIAGRAM



NOTES: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINS; NUMBERS IN ( ) ARE PLCC PINS. PINS (1), (6), (10), (18), (21) & (23) ARE NOT CONNECTED.

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1 (2)	AGND	Analog ground
2 (3)	TXCK0	Transmitter clock output. In high speed, synchronous, internal mode, this output supplies a 1200 Hz clock to the DTE.
3 (4)	TXCK1	In high speed, synchronous, external mode, this pin is an input for receiving a 1200 Hz clock from the DTE.
4 (5) 5 (7)	TEST 1, TEST 2	Used by Sierra for testing. Make no connection to these pins—they MUST be left floating.
6, (8)	RXCK	Receiver clock output. In high speed, synchronous mode, the modem supplies a 1200 Hz clock on this output.
7, (9)	Audio Out	Output of the hybrid is passed through a programmable attenuator and brought out on this pin. 4 levels of received signal can be programmed using the control codes listed in Table 1 (Page 8).
8,19 (1,6, 10,18,21,23)	NC	No Connect. These pins must be left floating. Do NOT ground these pins or tie them to V_{CC} or V_{SS}.
9 (11) 10 (12)	RXA1, RXA2	Received data carrier
11 (13)	TXOUT	Transmit data carrier output
12 (14)	V_{SS}	–5 V power supply
13 (15)	RXD	Receive data. The modem demodulates the received carrier and outputs data on the pin. A logic low level is space and a logic high level is mark. The controller can force the demodulator output to the mark state by sending the code 02.
14 (16)	TXD	Transmit data. Data on this input is modulated by the modem and output on TXOUT pin. A logic low is space and a logic high is mark.
15 (17)	D I/O	Data I/O pin. Data is shifted in serially when $\overline{WR}$ is low on rising edges of SCK clock. Data is transferred to a latch when $\overline{WR}$ goes high. Up to 7 data bits can be sent. Input codes are defined in Table 1. Data is read from the modem serially when $\overline{RD}$ is low, on rising edges of SCK clock. Up to 4 data bits can be read. Output codes are defined in Table 1 (Page 8).
16 (19)	SCK	Serial shift clock is applied to this pin. It is normally high until data is sent to or read from the modem.
17 (20)	$\overline{RD}$	Strobe output from controller for serially reading data from the modem.
18 (22)	$\overline{WR}$	Strobe output from the controller for shifting data to the modem.
20 (24) 21 (25)	XTAL1, XTAL2	Pins for connecting a 7.3728 MHz crystal. An external CMOS (+5 V) clock signal can be applied to the XTAL1 pin, with XTAL2 left open. If a TTL clock is used, it must be capacitively (100 pF) coupled into XTAL1.
22 (26)	DGND	Digital ground
23 (27)	CKOUT	Buffered crystal oscillator signal is output on this pin. It can drive one LS TTL load.
24 (28)	V_{CC}	+5 V power supply

Numbers in ( ) refer to 28-Pin PLCC Package.

FUNCTIONAL DESCRIPTION OF THE SC11004/14 MODEM

Major sections of the SC11004/14 modem are a transmitter, a receiver, low-band and high-band filters, a two-to-four wire hybrid, tone generators and interface logic. It also contains an energy detector that's used for detecting the carrier and call progress monitoring and an audio output for monitoring the line.

The SC11004/14 modem requires ±5 V and is available in a 24-pin DIP as well as a 28-lead plastic chip carrier with 'J' leads for surface mount applications. The transmitter section consists of an async/sync convertor, scrambler, PSK modulator and FSK modulator. In the high speed mode (1200 bps), the PSK modulator is connected to the filter. In the low speed mode (300 bps), the FSK modulator is connected to the filter.

Transmitter

Since data terminal and computers may not have the timing accuracy required for 1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync convertor accepts asynchronous serial data clocked at a rate between 1200 Hz + 1%, – 2.5%. It outputs serial data at a fixed rate of 1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync convertor is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first two stages of the shift register form the dibit that is applied to the PSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band centered at 2400 Hz or the low band, centered at 1200 Hz. A 1200 bps modem actually sends two bits at a time, called a dibit; dibits are sent at 600 baud, the actual rate of transmission; 600 baud is the optimum rate that can be transmitted over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

The dibit applied to the PSK modulator produces one of four differential phase shifts of the square wave carrier signal (1200 Hz or 2400 Hz) at the 600 Hz baud rate. The resultant waveform is passed through a wave shaping circuit that performs a raised cosine function (this is the shape factor called out in the CCITT V.22 spec, and it also meets the Bell 212A requirement for optimum transmission). The wave shaped signal is then passed through either the low-band or high-band filter depending upon originate or answer mode selection.

For low speed operation the FSK modulator is used. It produces one of four precision frequencies depending on orignate or answer mode and the 1 (mark) or 0 (space) level of the transmit data. Different frequencies are used for V.21 and 212A modes. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop. In the Call Progress Monitoring mode, the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog

loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second order low-pass switched-capacitor filter that adds the modem transmit signal to the DTMF or V.22 guard tones. It also provides a 3 dB per step programmable gain function to set the output level.

Receiver

The receiver section consists of an energy detector, AGC, PSK demodulator, FSK demodulator, descrambler, and sync/async convertor.

The received signal is routed through the appropriate band-pass filter and applied to both the energy detector and AGC circuit. The energy detector is based on a peak detection algorithm. It provides a detection within 17 to 24 ms. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels.

The AGC circuit is a programmable gain amplifier that covers a wide range. Output of the AGC amplifier is rectified and compared with two preset levels corresponding to desired high and low limits. Outputs of the comparators control an up/down counter such that the received signal is amplified to the desired level. Receive signal input range is 0 to –45 dBm measured at the chip.

The PSK demodulator uses a coherent demodulation technique. Output of the AGC amplifier is applied to a dual phase splitter that produces an in-phase and 90 degree out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by the recovered carrier. The baseband components are low-pass filtered to produce I and Q channel outputs. (In phase and Quadrature). The I and Q channel outputs are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. The signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled to produce the received dibit data. The recovered carrier for the demodulator is generated by another PLL which is controlled by the amplitude of the error signal formed by the difference of the I and Q outputs.

The descrambler is similar to the scrambler. The received dibit data is applied to the D input of a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with input data to produce received data.

In the asynchronous mode, data from the descrambler is applied to the sync/async convertor to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (over-speed data), these stop bits are reinserted. Underspeed data is passed essentially unchanged. Output of the sync/async convertor along with the output of the FSK demodulator is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed, and outputs received data on the RXD pin.

For low speed operation, the FSK demodulator is used. The output of the AGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, this matching is provided by an external resistor connected between the RXA1 and RXA2 pins on the SC11004/14. The filter section provides sufficient attenuation of the out of band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass anti-aliasing filter.

Internal Hybrid

The SC11004/14 internal hybrid, shown in Figure 1, is intended to simplify the phone line interface. In addition, there is a gain select feature to compensate for the loss in the line coupling transformer used in the DAA. By tying this pin to V_{SS}, ground or V_{DD}, compensation levels of 0, +2 or +3 dB, respectively, are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. With a 3 dB loss transformer for example, the energy detect on/off levels measured at the line will be in the range of –40/–45 dB rather than –43/–48 dB as specified at the chip. An external hybrid circuit, shown in Figure 2, can be used to overcome these losses and achieve maximum performance.

External Hybrid

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC110104/14 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. For example, if the TLC1, TLC0 level control codes are set to 0 and 1 respectively so as to obtain –9 dBm at the line, the chip actually puts out –3 dBm at the TXOUT pin (pin 11). Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired –9 dBm. In practice however there is impedance mismatch and a loss in the coupling transformer. Therefore it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain G_R and transmit gain G_T are set by the ratios of resistors R2, R1 and R6, R5 respectively (Figure 2).

The circuit can be analyzed as follows:

$$V_R = -\frac{R2}{R1}\left(V_{TR}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)V_y$$

$$V_y = -\frac{R6}{R5}V_x$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_Y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_Y = 2\,V_{TX}$,

$$V_R = -\frac{R2}{R1}\left(V_{TX}+V_{RX}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)2V_{TX}$$

$$= -\frac{R2}{R1}\,V_{RX} + \left[\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}$$

Solving for R3/R4

$$\frac{R3}{R4} = 1 + \frac{2R1}{R2}$$

Additionally,

$$G_R = \frac{R2}{R1} \text{ and } G_T = \frac{R6}{R5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive loss in the coupling transformer is 2.5 dB, then:

$$\frac{R2}{R1} = \text{INV Log}\left(\frac{G_{RdB}}{20}\right) = \text{INV Log}\left(\frac{2.5}{20}\right) = 1.333$$

Similarly, $\frac{R6}{R5} = 1.333$ and $\frac{R3}{R4} = 2.5$

Some typical values are:
R1=20 kΩ, R2=27 kΩ, R3=13 kΩ, R4=5.1 kΩ, R5=20 kΩ and R6=27 kΩ

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6 and capacitor C1 can be eliminated and point X connected to point Y in the circuit of Figure 2 to achieve a more cost effective external hybrid arrangement.

The SC11004/14 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, RXA2 is connected to ground and the receive signal is connected to RXA1. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

The tone generator section consists of a DTMF generator and a V.22 guard tone generator. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and * and # keys. The V.22 guard tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the Data I/O pin. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50 kΩ is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation — no attenuation, 6 dB attenuation, 12 dB attenuation and squelch are provided through the ALC1, ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Crystal Oscillator

The SC11004/14 includes an inverting amplifier between pins 20 and 21 with an internal bias resistor to simplify the design of the crystal oscillator. The parallel resonant, 7.3728 MHz ±0.001% crystal, designed for a load capacitance of 20 pF, should be connected across pins 20 and 21. Two capacitors of typical values 27 pF from pin 20 to digital ground (DGND pin 22) and 47 pF from pin 21 to DGND should be connected. With the recommended crystal, Saronix, NYMPH, NYP073-20 and these capacitor values, a highly accurate and stable crystal oscillator can be designed. Since the carrier frequency must be within ±0.01% of the normal 1200/2400 Hz, it is important to measure the actual crystal oscillator frequency at CKOUT (pin 23) and adjust the external capacitors for a given circuit board layout, if necessary.

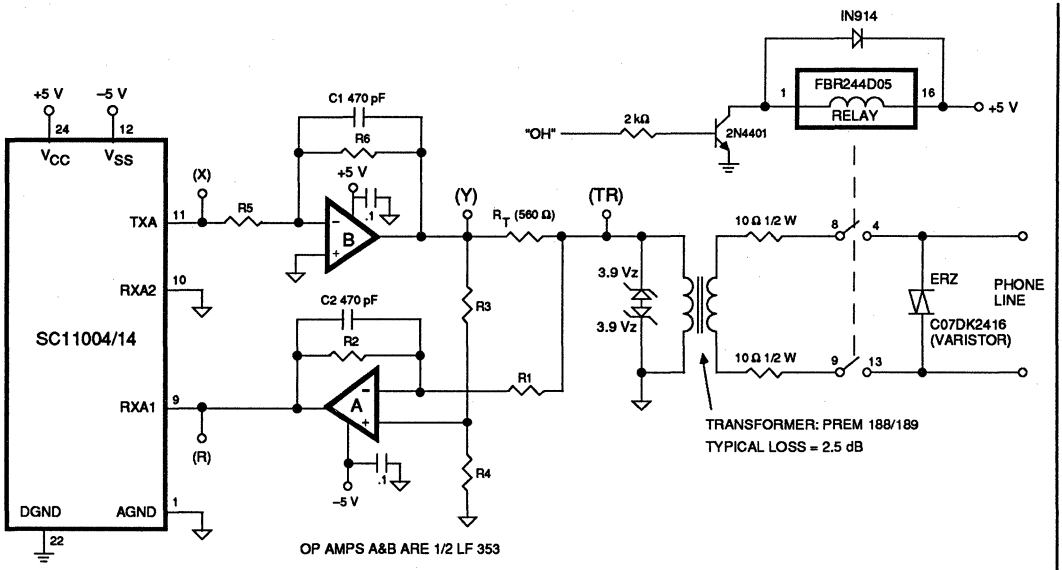


Figure 2. Using an External Hybrid with the SC11004/14

FUNCTIONAL DESCRIPTION OF THE SC11007 AND SC11008 CONTROLLERS

The SC11007 modem controller, implemented in Sierra's two micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including an 8-bit microprocessor, 8k by 8 bytes of ROM and 128 by 8 bytes of RAM, it also contains the functionality of an 8250B UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem for the PC consists of the SC11007 controller, the SC11004/14 modem and the DAA. All of the popular communications software written for the PC will work with the SC11004/14/SC11007 set.

Another version of the controller, the SC11008, is intended for RS-232 applications. It contains the same processor, memory and UART as the SC11007 and has the same interface to the modem chip. The difference is that the UART is turned around so the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The SC11008 provides a standard 5 V logic level interface—RS-232 drivers are required to interface to the port. Like the SC11007, the SC11008 comes preprogrammed with the Hayes 'AT' command set, and when used with the SC11004/14 modem, emulates a Hayes-type stand-alone modem. The SC11007 and SC11015 emulates a Hayes-type IBM PC plug-in card modem.

But the chip set is by no means limited to implementing a Hayes-type smart modem. Sierra is in the custom IC business and both chips were designed with this in mind. For example, only about 6k bytes of the SC11007's ROM is used for the handshaking and smart modem code, leaving 2k bytes for additional features that a customer may specify. And since the controller is ROM programmable, any command set, not just the Hayes 'AT' set, can be implemented.

Both the SC11007 and SC11008 require +5 V and are available in either a 28-pin DIP or a 28-lead plastic chip carrier with 'J' leads for surface mount applications. Besides the four-line interface for the SC11004/14 modem, the SC11007 controller has an 8-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 8250B UART. It also has control lines for ring indication, the off-hook relay and data/voice relay; these three lines connect to the DAA.

In the SC11008, the 8-bit port becomes the switch input lines and the address, chip select, DIST and DOST lines become the six lines for the RS-232 interface. These six lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control—so the main difference between the

SC11007 and SC11008 is the ROM code. It also contains the same modem and DAA interface lines as the SC11007.

The SC11007 and SC11008 are truly ASIC controllers—they are designed to control a modem or other peripheral that operates at a moderately slow rate up to 1200 bits per second. What's unique about the SC11007, for example is that it allows a slow peripheral to interface to a high speed bus, without making the main processor slow down.

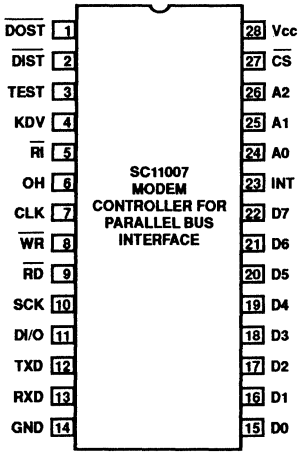
This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11007 compatible with this software, the registers were included.

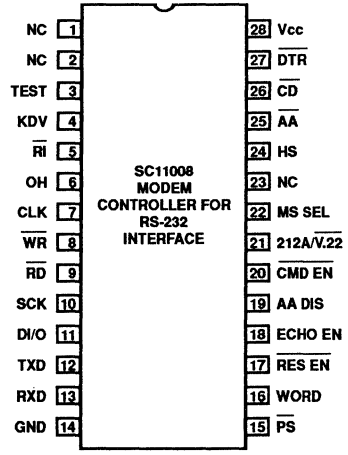
The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like in a Hayes-type modem. The escape sequence is three + signs—+++ —in the default mode, but it can be changed in software.

The actual processor contains an 8-bit data path and can execute 19 instructions with five different addressing modes: direct, indirect, immediate, register direct and register indirect. There is 8k by 8 of ROM on chip for program storage.

To the system bus, the SC11007 looks and acts just like an 8250B UART. Communications software written for this UART will work with the SC11007 and SC11008. The Sierra chip set is truly a Hayes-type modem in two chips.

CONNECTION DIAGRAMS—SC11007 AND SC11008 CONTROLLERS





THE SC11004/14 & SC11007/SC11008 SYSTEM

The only external components required by the SC11004/14 are the 600 Ω line matching resistor, a 7.3728 MHz crystal—a standard frequency—and a 20 pF capacitor from each leg of the crystal to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11004/14 can directly drive a high impedance (50 kΩ) earphone-type transducer.

The SC11007 modem controller's clock in line is driven by the SC11004/14's clock out line, so only one crystal is needed. The SC11007 interfaces directly to an IBM PC bus—no buffers are required. The only external parts may be a 8 input NAND gate for COM1 and COM2 decoding inside the PC.

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

All modems require a DAA. A DAA or data access arrangement is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω; a relay for disconnecting the modem from the line; a ring

detector, typically an optoisolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by any of many consultants and labs around the country. The fee is typically $2,000 and it takes several months. Another alternative is to buy a DAA, supplied by several manufacturers.

212A is a Bell specification that calls for 1200 bit per second, full or half duplex data transmission with a fallback mode of 300 baud (Bell 103). It is not 1200 baud; the spec calls for transmission of dibits—2 bits per baud so the 1200 bps transmission takes place at 600 baud. The same is true for V.22—it's 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; there is a CCITT standard for 300 and that's V.21.

V.22 also calls for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The SC11004/14 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone when in the receive mode.

All modems require a Hybrid. Hybrid is a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the SC11004/14, this is done with op amps, but the separate signals—TXOUT and RXA2—are also brought out so an external hybrid can be used, if desired. The combined signal comes out on the RXA1 pin and matching resistor—typically 600 Ω—is connected between RXA1 and RXA2.

SC11004/14 SPECIFICATIONS

Table 1. Definition of I/O Codes

1. Instructions to the modem IC (See Note 1 and 2). Data on the DI/O pin shifted into the modem when $\overline{WR}$ is low, on rising edges of the SCK clock. Data is transferred into a latch when $\overline{WR}$ goes high. (See Figure 2 for write cycle waveforms). Up to 7 data bits (D0–D6) can be sent to the device. These bits control the operating modes of the modem as shown below:

D6	D5	D4	D3–D0	HEX CODE	MODE/FUNCTION
Non tone mode:					
0	1/0	0	0	20/00	Reset (set default values)
0	1/0	0	1	21/01	Tone On/Off (tone mode enable/disable)
0	1/0	0	2	22/02	Force Receive Data to Mark Off/On (forces RXD pin High if On)
0	1/0	0	3	23/03	TLC0 Transmit Level Control bit 0 (default 0)
0	1/0	0	4	24/04	TLC1 Transmit Level Control bit 1 (default 0)
0	1/0	0	5	25/05	TX Transmitter On/Off (if Off, TXOUT is grounded)
0	1/0	0	6	26/06	ALB Analog Loopback On/Off
0	1/0	0	7	27/07	CPM Call Progress Monitor mode On/Off
0	1/0	0	8	28/08	Connection Indicator (CI) On/Off (see note 4 below)
0	1/0	0	9	29/09	ALC0 Audio Output Level Control bit 0 (default 0)
0	1/0	0	A	2A/0A	ALC1 Audio Output Level Control bit 1 (default 0)
0	1/0	0	B	2B/0B	WLS0 Word Length Select 0 (default 0)
0	1/0	0	C	2C/0C	WLS1 Word Length Select 1 (default 1)
0	1/0	0	D	2D/0D	Sync/Async
0	1/0	0	E	2E/0E	LS/HS: Low Speed/High Speed (FSK/PSK)
0	1/0	0	F	2F/0F	A/O: Answer/Originate
0	1/0	1	0	30/10	Transmit Mark On/Off
0	1/0	1	1	31/11	Transmit Space On/Off
0	1/0	1	2	32/12	Scrambler Off/On
0	1/0	1	3	33/13	DLB Digital Loopback On/Off (also sets Synchronous, Slave Mode)
0	1/0	1	4	34/14	TXDP Transit Dotting Pattern On/Off (Not valid for V.21 mode)
0	1/0	1	5	35/15	Sync Mode Transmit Timing Locked/Free Running
0	1/0	1	6	36/16	Sync Mode Transmit Timing Source External/Slave
0	1/0	1	7	37/17	2100 Hz tone On/Off. Must select low speed mode for operation.
0	2/0	1	8	38/18	1300 Hz tone On/Off. Must select low speed mode for operation.
0	1/0	1	9	39/19	V.21 mode. Must select low speed mode for operation.

D6	D5	D4	D3–D0	HEX CODE	MODE/FUNCTION
Tone mode:					
1	1/0	0	0	60/40	Dial 0
1	1/0	0	1	61/41	Dial 1
1	1/0	0	2	62/42	Dial 2
1	1/0	0	3	63/43	Dial 3
1	1/0	0	4	64/44	Dial 4
1	1/0	0	5	65/45	Dial 5
1	1/0	0	6	66/46	Dial 6
1	1/0	0	7	67/47	Dial 7
1	1/0	0	8	68/48	Dial 8
1	1/0	0	9	69/49	Dial 9
1	1/0	0	A	6A/4A	Dial *
1	1/0	0	B	6B/4B	Dial #
1	1/0	0	C	6C/4C	Output 550 Hz and insert 550 Hz notch in low-band filter
1	1/0	0	D	6D/4D	Output 1800 Hz and insert 1800 Hz notch in low-band filter
1	1/0	0	E	6E/4E	Row disable On/Off (For DTMF test only)
1	1/0	0	F	6F/4F	Column disable On/Off (For DTMF test only)

WLS1	WLS0	Word Length
0	0	8 bits
0	1	9 bits
1	0	10 bits (default)
1	1	11 bits

TLC1	TLC0	Transmitter Output Level (dBm) (Note 3).
0	0	–6 (default)
0	1	–3
1	0	0
1	1	+6

ALC1	ALC0	Audio Output Level
0	0	Output Off (default)
0	1	12 dB attenuation
1	0	6 dB attenuation
1	1	No attenuation

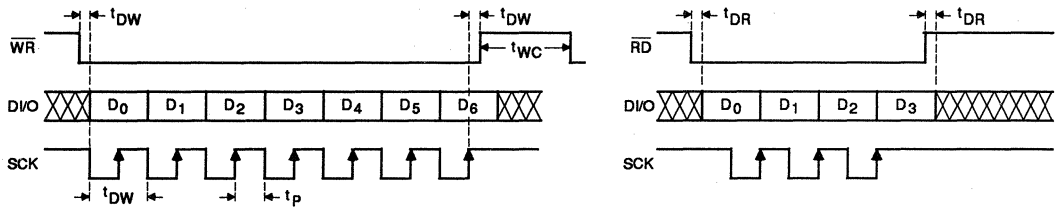
Notes: 1. Default values for the operating modes on power up are those shown to the right of the '/' unless otherwise specified.
2. Data is shifted in and out of the modem with LSB first.
3. SC11014 only.
4. Using the internal hybrid and a 600 Ω resistor, these levels will be 6 dB lower at the input to the transformer.
5. After a connection is established, turn CI on to disable unnecessary functions, i.e. if a PSK connection is established, turning CI on will turn off the FSK demodulator.

2. Information from the modem IC. Data is read serially from the modem when $\overline{RD}$ is low, on rising edges of the SCK clock. (See Figure 3 for read cycle waveforms). Up to 4 data bits (D0–D3) can be read as defined below:

D0 Energy Detect 0—no energy 1—energy present

In the CPM mode, the energy detector is connected to the output of the high band filter, if ALB is off, or the scaled low band filter, if ALB is on.

D1	Received data (FSK)	1—Mark	0—Space
D2	Received data (PSK)	1—Mark	0—Space
D3	Unscrambled Mark	1—Detected	0—Not Detected



t_{WC} = 4 µsec
t_{DW} = 200 nsec Min.
t_{PW} = 1 µsec Min.
t_p = 30% to 70% duty cycle
t_{DR} = 200 nsec Min.

Figure 3. Waveforms for Write and Read Cycles

Serial Interface — The 4 line serial interface consists of a bidirectional data pin (DI/O), a write control pin ($\overline{WR}$), a read control pin ($\overline{RD}$) and a clock pin (SCK). In the inactive state, $\overline{WR}$, $\overline{RD}$ and SCK lines must be held in the high state. The read and write functions are controlled only by the mircocomputer. To write data into the SC11004/14 (see timing waveforms of Figure 2), the controller must first make the $\overline{WR}$ line low. The least significant bit D0 of the data is then placed on the DI/O line. The SCK line is then toggled low and then high to shift the data bit into the SC11004/14 input register. Data is shifted into the input register on the rising edge of SCK.

There is no special requirement on the duty cycle of the clock signal. The minimum pulse width and data setup times specified in the specifications table must be met. The remaining data bits D1 thru D6 are shifted by repeating the above procedure. Only 7 data bits should be sent. If an 8th data bit is sent, the first data bit D0 will be lost from the input register. The received data will then be D7–D1 rather than D6–D0. To read data from the SC11004/14 (see timing waveforms of Figure 3), the $\overline{RD}$ line is first made low. The least significant bit D0 is now available on the DI/O line. The SCK line is toggled low and then high to shift the next data bit out of the SC11004/14 output register. The SC11004/14 shifts the data out on the rising edges of SCK. The controller should read data on the falling edges of SCK when it will be stable. Note that D0 appears on the DI/O line as soon as $\overline{RD}$ is taken low. If the controller only wants to read the status of the energy detector, there is no need to toggle SCK line. By making $\overline{RD}$ low, the energy detector level can be read by reading DI/O. $\overline{RD}$ can then be taken high. Read operation is terminated by making the $\overline{RD}$ line high. If more than 4 bits are read, the additional bits are returned as 0's.

In the READ mode, the values of D0, D1, D2 and D3 do not change as long as $\overline{RD}$ is low, even though the chip status may be changing. To read out the updated values of these bits, $\overline{RD}$ must be pulled high for at least 1 ms and then taken low again to initiate another read cycle.

The read and write operations can be performed by two simple I/O drivers shown in table 2. The RDMO–DEM subroutine reads data from the SC11004/14 and places it in the accumulator with the high nibble set to zero. The WTMODEM subroutine sends data placed in the accumulator to the SC11004/14. Both subroutines use register R7 in bank 1 as a data bit counter.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1 — SC11004/14 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 4.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11004/14 in the synchronous mode (2D). This provides a 1200 Hz clock on the TXCK0 Pin that can be used as a clock source for the DTE to synchronize its TXD to. The Transmit Phase-Locked-Loop (TX PLL) of the SC11004/14 will be in free-runing mode. As a result, External/Slave input codes will be ignored by the chip.

Case 2 —SC11004/14 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode (2D), also select "Locked" (35) and "External" (36) modes. The TX PLL of SC11004/14 will then synchronize itself to the clock provided on its "TXCK1" pin.

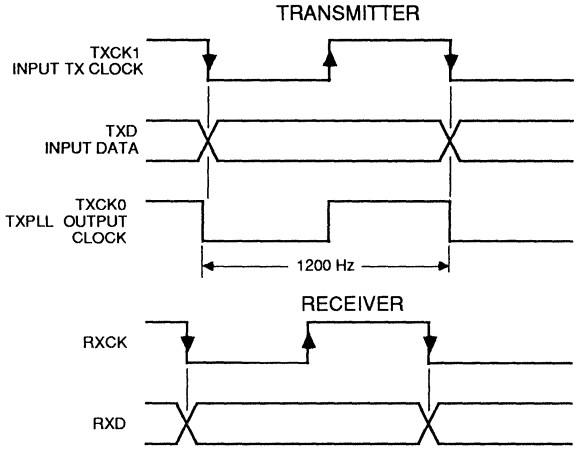
Receiver Timing

In synchronous mode, the recovered clock will be provided on the RXCK pin and the transitions of RXD will be on the falling edges of this clock.

SYNCHRONOUS MODE CHART

Transmitter Timing

Locked (35)	External (36)	TX PLL locks to clock provided on TXCK1
	Slave (16)	TX PLL locks to receiver timing. Should be used in DLB mode only.
Free Running (15)	External/Slave	TXPLL is free running and ignores External or Slave inputs.



Note: 1 SC11004/14 will sample the data on the rising edge of TXCK1 clock.

Figure 4. SC11004/14 Synchronous Mode Diagrams

ABSOLUTE MAXIMUM RATINGS (NOTES 1, 2 AND 3)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS}–0.6 to V_{CC}+0.6 V
DC Input Voltage (Digital Signals)	V_{SS}–0.6 to V_{CC}+0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 s)	300°C

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating — Plastic Package: –12 mW/C from 65°C to 85°C.

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
F_C	Crystal Frequency		7.3721	7.3728	7.3735	MHz
T_R, T_F	Input Rise or Fall Time	(Note 4)			500	ns

Notes: 4. Does not apply to CKOUT.

DC ELECTRICAL CHRACTERISTICS (NOTE 5)

PARAM.	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	V_{CC} = 5 V			15		mA
I_{SS}	Quiescent Current	V_{SS} = –5 V			15		mA
V_{IH}	High Level Input Voltage	Digital Signal Pins $\overline{RD}$, $\overline{WR}$, D I/O, SCK, TXCK1, TXD		2.0			V
V_{IL}	Low Level Input Voltage	Digital Signal Pins $\overline{RD}$, $\overline{WR}$, D I/O, SCK, TXCK1, TXD				0.8	V
V_{OH}	High Level Input Voltage	Digital Signal Pins D I/O, RXD, TXCK0, RXCK	I_{OH} = 40 µA	4.0			V
			I_{OH} = 500 µA	2.0			V
V_{OL}	Low Level Input Voltage	Digital Signal Pins D I/O, RXD, TXCK0, RXCK	I_{OL} = 1.6 mA		0.4	0.6	V
V_{OM}	Maximum Output Signal	TXOUT, RL = 1200 Ω (TLC = 1, TLC0 = 0)		4.0			V_{P-P}
V_{IM}	Maximum Input Signal	RXA1, RXA2 (Using Internal Hybrid)				4.0	V_{P-P}

Note: 5. Min and max values are valid over the full temperature and operating voltage range. Typical values are from 25°C and ±5 V operation.

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQ.	ALLOWABLE ERROR	ACTUAL ERROR
Row 1	697 Hz	±1%	+0.17%
Row 2	770 Hz	±1%	–0.26%
Row 3	852 Hz	±1%	+0.16%
Row 4	941 Hz	±1%	–0.47%
Column 1	1209 Hz	±1%	–0.74%
Column 2	1336 Hz	±1%	–0.89%
Column 3	1477 Hz	±1%	–0.01%
Guard Tones	550 Hz	±20 Hz	–1.4 Hz
	1800 Hz	±20 Hz	+7 Hz

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion			–40		dB
Row Output Level	V_{CC} = +5 V V_{SS} = –5 V TLC0 = 1 TLC1 = 1 Measured at TXOUT Pin		0		dBm
Column Output Level			2		dBm
550 Hz Guard Tone			–3		dB (Note 2)
1800 Hz Guard Tone			–6		dB (Note 2)

Notes: 1. This assumes a crystal of exactly 7.372800 MHz.
2. These levels are referenced to the TX signal level. When guard tones are added, the TXOUT level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

Modem Transmit Signals—Hz (Assume 7.372800 MHz Crystal)

MODE		BELL 103		CCITT V.21		212A/V.22	
		NOMINAL	ACTUAL	NOMINAL	ACTUAL	NOMINAL	ACTUAL
Answer	Mark	2225	2226	1650	1649.4	2400	2400
	Space	2025	2024.4	1850	1850.6		
Originate	Mark	1270	1269.4	980	978.34	1200	1200
	Space	1070	1070.4	1180	1181.53		
Calling Tone				1300	1301.7	1300	1301.7
Answer Tone				2100	2096.9	2100	2096.9

Transmitter

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Character Length	Start Bit + Data Bit + Stop Bit	8		11	bits
Intra-Character Bit Rate	AT TXD (Pin 14)	1170	1200	1212	bps
Input Break Sequence Length	M = Character Length	2M + 3			bits
Output Level Tolerance			±1		dB

Receiver

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Signal Range	AT RXA1	-45		0	dBm
Intra-Character Bit Rate	AT RXD (Pin 13)	1170	1200	1224	bps
Carrier Detect	AT RXA1 (Pin 9)	-48		-43	dBm
Carrier Detect Hysteresis		2			dB
Carrier Detect Delay	For 103, 212A and V.22	10	20	30	ms
Carrier Detect Hold	For 103, 212A and V.22	15	20	24	ms
Carrier Detect Delay	For V.21 Mode	15	30	40	ms
Carrier Detect Hold	For V.21 Mode	20	30	50	ms

APPLICATIONS INFORMATION

Why a Modem/What's a Modem

The voice frequency channels of the general switched telephone network have been used extensively for the transmission of digital data. To use these channels, the data must be put in a form that can be sent over a limited bandwidth line. In voice grade telephone networks, transformers, carrier systems and loaded lines attenuate all signals below 300 Hz and above 3400 Hz.

While the bandwidth from 300 Hz to 3400 Hz is fine for voice transmission, it is not suitable for the transmission of digital data because the data has many frequency components outside this range. To transmit data over phone lines, it is necessary to convert the digital data into a signal that is totally within the voice frequency range. This conversion is performed by a MODEM (MODulator DEModulator).

In full duplex data transmission—the simultaneous sending and receiving of data—Frequency Division Multiplexing (FDM) can be used for data rates up to 2400 bits per second. In FDM, the voice channel is divided into upper and lower bands (called the high band and the low band); one is used for sending and the other for receiving data. The originating terminal transmits in the low band and receives in the high band, while the answering terminal transmits in the high band and receives in the low band.

In low speed modems (300 bit per second transmission rate), the modulation technique commonly employed is called Frequency Shift Keying (FSK). In FSK modems, four separate frequencies are used; 1070 Hz for a zero (also called a space) in the low band, 1270 Hz for a one (a mark) in the low band, 2025 Hz for a zero in the high band and 2225 Hz for a one in the high band. The transmitting modem takes the digital ones and zeros from the terminal and converts them into the proper tones which are then sent over the phone line. The receiving modem takes the tones and converts them back to ones and zeros and sends them to the receiving terminal. Since four frequencies are used, simultaneous transmitting and receiving of data can be accomplished.

Because of the limited bandwidth of the phone line, FSK modems only work up to 600 bits per second for full duplex transmission. This is due to the fact that when the modem shifts between the two frequencies (for mark and space) it generates a frequency spectrum (it is a type of FM—frequency modulation—transmission). The faster the data rate, the wider the spectrum. The limit for full duplex FSK transmission is 600 bits per second, before the available audio spectrum is used up—allowing for enough separation between the frequency bands to reliably decode or demodulate the data. There are 1200 bps FSK modems, but these are half duplex—they can only send OR receive data at 1200 bps.

In higher speed, full duplex modems (1200 bit per second transmission rate) a different modulation technique is employed. Called PSK (for Phase Shift Keying), this technique uses one carrier frequency for the high band—2400 Hz—and one for the low band—1200 Hz—for sending and receiving data. For each carrier frequency (one for transmitting and one for receiving), one of four phase angles is used: 0, 90, 180, or 270 degrees. The data is sent two bits at a time, or in dibits. Since there are four ways to send two bits at a time—00, 01, 10 or 11—each of the four phases represents one unique dibit. While the data rate is 1200 bits per second, the baud rate (the rate at which information packets are sent) is 600 because two bits (dibits) are sent in each packet. Again, 600 packets per second (600 baud and, in this case, 1200 bps) is the limit for transmitting full duplex data over the general switched telephone network using FDM.

Call Progress Monitor Operation

The modem controller uses the high-band and low-band filters in the SC11004/14 for call progress monitoring. When the SC11004/14 is put in the CPM mode, the ALB mode provides a means of connecting either the high-band filter (ALB = 0) or the scaled low-band filter (290–660 Hz) (ALB = 1) to the energy detector. Output of the energy detector is monitored by reading bit D0 for detection of call progress or voice/answer information, using the duration and repetition rate as the criteria for detection.

A typical call establishment sequence is as follows:

Dial tone detection — The controller puts the SC11004/14 in the Originate, CPM mode with ALB = 1 and operates the off-hook relay in the DAA by making the OH output high. After a short delay (typically 300 ms), it monitors the output of the energy detector (ED). If the output is continuously high for at least 1 second; it is recognized as a valid dial tone. If the output is not continuous then the controller continues to monitor until a timeout occurs (typically 5 seconds). If a dial tone is not detected within this timeout, the controller returns a 'NO DIAL TONE' message to the DTE and aborts the call. If a dial tone is detected, it proceeds to dial the number as follows.

Dialing—The controller will use the specified format (tone or pulse) or determine the best way, if not specified. Assuming that the format is not specified, the controller will dial the first digit in the tone format. It will wait for a short time

(typically 80 ms) after dialing and check the output of the ED. If the output is low, it will mean that the dialing can proceed in the tone format. If the output is high, it will mean the dial tone is still present. The controller will then revert to the pulse format and redial the first digit. In all cases, the controller will check for loss of dial tone after a short delay (typically 80 ms) after dialing the first digit. If the dial tone is absent it will proceed to dial the remainder of the number. During the inter-digit pause (IDP), the controller will monitor the ED output after waiting for a short time (typically 80 ms). If the ED output is high, it will halt dialing, abort the call and return 'BUSY' message to the DTE.

If a pause is required in the dialing sequence for a second dial tone, the controller will repeat the above process. After dialing is done, the controller will wait for approximately 2.5 seconds and then start to monitor the ED output by alternately toggling the ALB mode at a rate of approximately 200 ms. This allows detection of ringback/busy call progress tones or voice/answer tone. The toggling rate is based on the settling times of the filters as well as the response time of the ED. Once energy is detected at the output of the ED, the controller will maintain the selected ALB mode until detection is made. The criteria for various detections are described below.

Ringback tone detection—Both duration and repetition rate are used to determine ringback tone. If the ED output is high for a cumulative duration of at least 0.7 second, but less than 3.8 seconds, with the number of transitions less than 7 over a period of 5 seconds, it is recognized as a valid ringback tone. The 5 second window is started when the ED output first goes high. Once the ringback is detected, the controller counts the number of ringback cycles and compares to the value stored in the ringback counter register (S1). If the ringback tone continues to be present after the preset number of cycles, the controller will abort the call and return 'NO ANSWER' message to the DTE.

If the ringback tone is removed prior to the preset value, the controller will switch the ALB to 0 to monitor the voice/answer tone. During the silent portion of the ringback cycle, the controller will also switch to monitor the high-band filter output to see if there is an answer. This speeds the response to an answer condition.

Busy tone detection—If the number of transitions of the ED output exceeds 7 over the 5 second window when looking for ringback tone, it will be assumed to be a busy signal. The controller will then abort the call and return a 'BUSY' message to the DTE.

Answer tone detection—If the output of the high-band filter is continously high for at least 2 seconds, the controller will assume it to be an answer tone from the distant modem, return a 'connect' message to the DTE and proceed with handshaking sequence necessary to establish a data call.

Voice detection—If the output of the ED is not continuously high over a 2 second period, it will be assumed to be voice and the controller will return a 'VOICE' message to the DTE and abort the call.

Silence detection—If the cumulative duration over the 5 second window is less than 0.7 second, once the window is started, it is recognized as silence. The controller then returns a 'NO ANSWER' message to the DTE and aborts the call.

Specific Applications

The SC11004/14 modem performs all the signal processing functions required in a 212A/V.22 modem. Like all modems, it requires an external controller to implement the handshaking protocols and control functions. The controller's task is simplified by the use of a 4 line serial interface as opposed to a multiline parallel interface. In particular, only I/O pins are used on a single chip microcomputer. More pins are then available for other interfaces such as DAA, RS-232, switches and lights. In most modem applications this will eliminate the need for external latches and buffers for additional I/O pins.

Figure 5 shows the SC11004/14 modem IC used with the SC11007 controller to make a complete parallel bus Hayes-type smart modem.

Figure 6 shows the SC11004/14 modem IC used with the SC11008 controller to make a complete RS-232 serial interface Hayes-type smart modem.

Figure 7 shows the schematic of a stand-alone smart modem implemented with the SC11004/14 and the 8031—the ROMless version of the 8051 microcomputer. Even though 16-port I/O pins are used up on the 8031 for interfacing with the external ROM, enough pins are still available for the other interfaces because of the serial interface used on the SC11004/14. The 8031 microcomputer was selected because of its wide use in current stand-alone and integrated smart modems.

Oscillator—The SC11004/14 includes an inverting amplifier and a bias resistor so that a crystal oscillator can be designed by connecting a 7.3728 MHz crystal and two capacitors (27 pF and 47 pF) to XTAL1 and XTAL2 pins as shown in the schematic. A buffered TTL compatible clock output is available on the CLOCK OUT pin to drive the microcomputer.

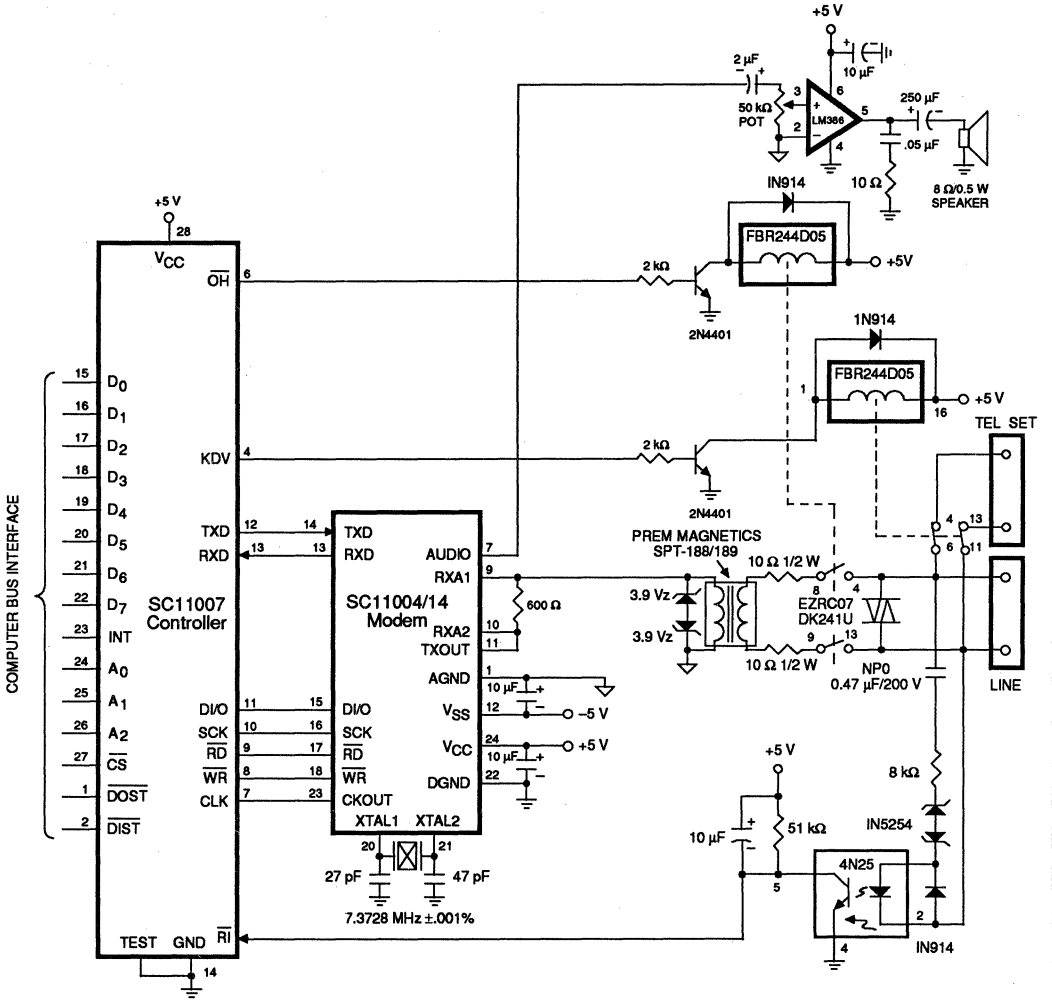


Figure 5. Internal 212A/V.22 Smart Modem Using the SC11004/14 Modem IC and the SC11007 Controller

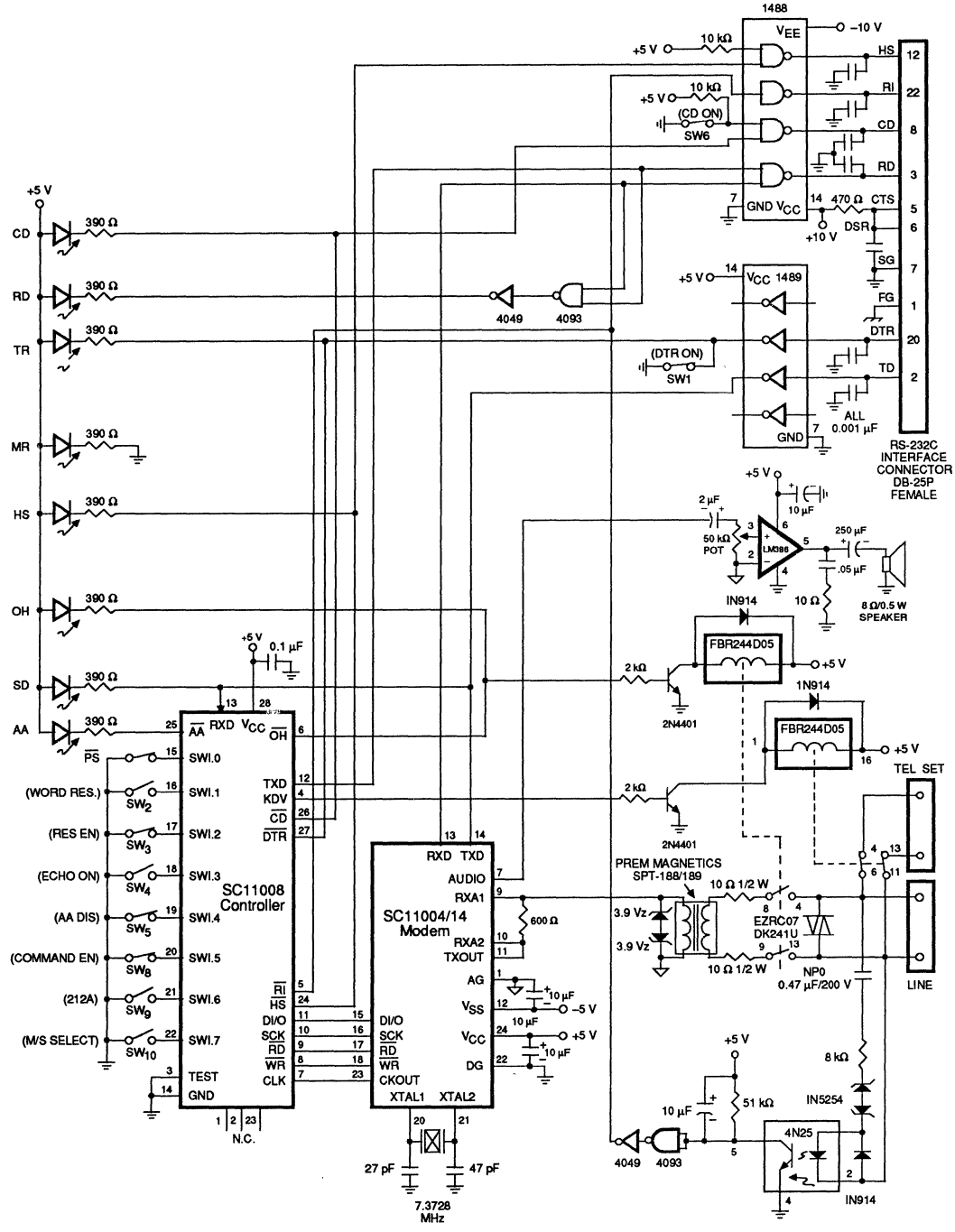


Figure 6. 212A/V.22 Stand-Alone Intelligent Modem Using the SC11004/14 Modem IC and the SC11008 Controller

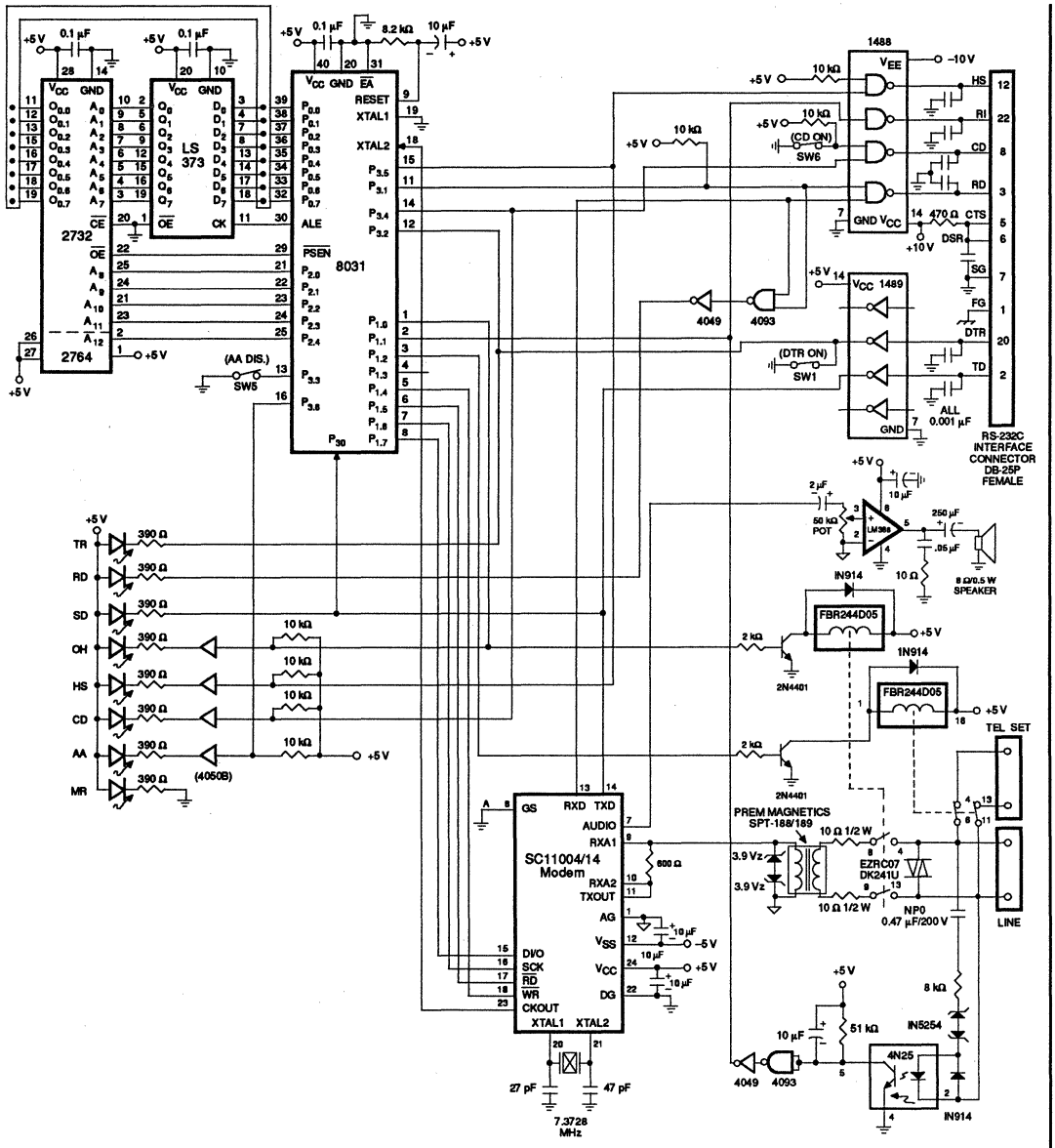


Figure 7. 212A/V.22 Stand-Alone Smart Modem Using the 8031 Controller with SC11004/14 Modem

```
WTMODEM:    CLR     P1.4        ;WR → 0; Initiate Write Cycle
            SETB    RS0         ;Select Bank 1
            MOV     R7, #7      ;Set Data Bit Counter to 7

OUTNEXT:    RRC     A           ;Bit → Carry
            CLR     P1.6        ;Toggle Clock Line Low
            JC      SETPB       ;Set/Clear DI/O Line on Carry
            CLR     P1.7
            LJMP    OUTPUT

SETPB:      SETB    P1.7

OUTPUT:     SETB    P1.6        ;Toggle Clock Line High
            DJNZ    R7, OUTNEXT ;Loop Till Data Bit Counter is Zero
            SETB    P1.7        ;Return to Initial Condition
            SETB    P1.4
            CLR     RS0
            RET

RDMODEM:    CLR     P1.5        ;RD → 0 ; Initiate Read Cycle
            SETB    RS0
            MOV     R7, #8

INNEXT:     CLR     P1.6
            MOV     C, P1.7     ;Data Bit → Carry
            RRC     A           ;And into Accumulator
            SETB    P1.6
            DJNZ    R7, INNEXT  ;Loop Till Data Bit Counter is Zero
            SETB    P1.5        ;Return to Initial Condition
            CLR     RS0
            RET
```

To dial a digit, the sequence shown below can be used. It is assumed that register R2 holds the digit to be dialed and memory location S11 holds the on/off duration of the tines in milliseconds.

```
TDIAL:      MOV     A, #21H     ;Turn on Tone Mode
            LCALL   WTMODEM
            MOV     A, R2       ;Read Digit
            ORL     A, #60H     ;Form Digit On Command
            LCALL   WTMODEM
            MOV     A, S11
            MOV     B, #10
            DIV     AB          ;Find Number of 10 ms Increments
            MOV     R1, A       ;Save It
            LCALL   DLOOP       ;Wait 10 ms Times Number in R1
            MOV     R1, A       ;Restore R1
            MOV     A, R2       ;Form Digit Off Command
            ORL     A, #40H
            LCALL   WTMODEM
            LCALL   DLOOP       ;Wait 10 ms Times Number in R1
            LJMP    NEXTDG      ;Go for Next Digit
```

Table 2. Serial I/O Driver Routines

In the following examples it is assumed that the clock frequency for the 8031 is 7.3728 MHz and that timer 0 is set in the auto-reload mode cycling at the rate of 416.66 µs. References are also made to certain registers used in Hayes compatible smart modems.

Initialization—The SC11004/14 does not have a power on reset circuit. The controller must put the device into the proper operating mode on power turn on. By sending a reset code, the device will enter a default mode as follows: high speed, asynchronous, originate, transmitter off, RX data clamped to mark, transmit level = –12 dBm, audio off and scrambler on. This mode is set up by the following lines of code:

```
MOV     A, #0          ;Reset Code
LCALL   WTMODEM        ;Write It
```

Dialing—The SC11004/14 includes an on chip DTMF dialer. It is necessary to adjust the transmit level during dialing since the tone level is internally set to be 6 dB below the transmitted carrier level. The following lines of code will set the tone level at the line to be –6 dBm for low group and –4 dBm for the high group tone:

```
MOV     A, #23H        ;TLC0 = 1
LCALL   WTMODEM
MOV     A, #24H        ;TLC1 = 1
LCALL   WTMODEM
```

Call Progress Monitoring—The progress tones can be monitored readily by activating the call progress monitor (code = 27H) and analog loopback (code = 26H) modes. The low band filter is then scaled down by a factor of 2.5 to center over the frequency range of 300 Hz to 660 Hz. Output of the energy detector monitored on the D0 bit then provides the necessary cadence information for detection of various call progress conditions. For example, dialtone is detected if the energy detector output is continuously high for at least 1 second. Busy line condition is recognized if the number of transitions of the energy detector output exceeds 7 over a period of 5 seconds and if the cumulative on duration exceeds 2 seconds.

Handshaking Sequences—Sequences necessary for establishing calls in various operating modes are provided in the following paragraphs. Numbers in parentheses indicate the hex code values sent to the SC11004/14 to implement that function of data bit received from the SC11004/14 for monitoring a given function.

A. Originating call in high speed (212A) mode:

1. Clamp receive data to mark condition (2)
2. Sample energy detector output (D0) to see if answer tone is present.
3. If continuous answer tone is detected for time set in register S9 (typically 600 ms) prior to timeout set in register S7 (typically 30 s) proceed with handshaking. Otherwise output NO CARRIER to data terminal and abort call.
4. Transmit mark (30).
5. Turn transmitter on (25).
6. Wiat for 300 ms.
7. Sample PSK data output (D2) at twice the bit rate (every 416.66 µs).
8. If continuous PSK data mark signal is received for 64 bit intervals, proceed to step 9. If PSK data mark signal is not received prior to timeout set in S7, output NO CARRIER to data terminal and abort call.
9. Wait for 700 ms.
10. Turn connection indicator on (28).
11. Turn transmitter mark off (10).
12. Unclamp receive data (22).
13. Turn on carrier detect output.
14. Send CONNECT or CONNECT 1200 message to data terminal.

B. Originating call in low speed (103) mode:

1. Perform steps 1 thru 3 as in A) above.
2. Put SC11015 in low speed mode (2E).
3. Carry out steps 4 thru 6 as in A) above.
4. Go to step 11 in A) above.

C. Answering call (212A–103) mode:

1. Put SC11004/14 in answer mode (2F).
2. Wait 2.1 seconds (billing timeout).
3. Put SC11004/14 in low speed mode (2E).
4. Transmit mark (30).
5. Turn transmitter on (25).
6. Sample energy detector output (D0) to see if carrier is present. If carrier is received continuously for 200 ms, proceed to step 7. If timeout set in S7 occurs, output NO CARRIER and abort call.
7. Sample PSK detector output (D2) at twice the bit rate (every 416.66 µs).
8. If continuous PSK data mark is received for 64 bit intervals, prior to one second timeout, proceed to step 9. If continuous FSK data mark is received for 256 bit intervals, proceed to step 10 in A) above. If neither PSK or FSK data mark is received prior to timeout set in S7, output NO CARRIER to data terminal and abort call.
9. Put SC11004/14 in high speed mode (0E).
10. Go to step 9 in A) above.

D. Originating call in high speed (V.22) mode:

1. Clamp receive data to mark condition (02).
2. Select low speed mode (2E), V.21 mode (39).
3. Turn on calling tone (38) for 0.6 seconds followed by 1.5 seconds of off period until answer tone is detected.
4. Turn off calling tone (18) and V.21 mode (19).
5. Select high speed mode (0E).
6. Wait for unscrambled mark.
7. Wait 456 ms, then proceed to step 4 in A) above.

E. Originating call in low speed (V.21) mode:

1. Perform steps 1 thru 4 as in D) above.
2. Wait for 1 second, then send FSK mark.
3. Wait for carrier to drop. Start a 3 second timer. If carrier drops prior to timeout proceed to step 4. Otherwise proceed to step 4 after timeout.
4. Wait for FSK mark.
5. Turn on connection indicator (28).
6. Turn transmit mark off (10).
7. Unclamp receive data (22).
8. Turn on carrier detect output.
9. Send CONNECT message to terminal.

F. Answering call (CCITT mode) with auto speed detection (V.22/V.21):

1. Select answer mode (2F).
2. Turn scrambler off (32).
3. Wait for 2.1 second billing timeout.
4. Select low speed mode (2E); V.21 mode (39).
5. Turn on 2100 Hz answer tone (37). Start 3.3 second timer.
6. Turn off 2100 Hz answer tone (17) after timeout.
7. Turn transmitter off (05).
8. Wait 60 ms.
9. For next 20 ms look for carrier and continuous FSK mark. If detected, assume low speed and proceed to step 14.
10. Turn transmitter on (25).
11. Select high speed mode (0E). Turn off V.21 mode (19).
12. Turn on 1800 Hz guard tone; (21), (6D).
13. Start 1 second timer. Look for continuous PSK mark for 64 bit intervals over 1 second period. If PSK mark is not detected within 1 second, turn off high speed mode, (select low speed mode), turn off guard tone, turn on V.21 mode and look for continuous FSK mark for 64 bit intervals over the next 1 second period. If FSK mark is not detected, repeat from start. If timeout set in S7 occurs prior to detecting either PSK or FSK mark, output NO CARRIER and abort call. If either PSK or FSK mark is detected, go to step 10 in A).
14. Turn transmitter on (25).
15. Send CONNECT message to terminal.
16. Turn connection indicator on (28).
17. Turn carrier detector on.

G. Requesting remote digital loopback to far end modem:

1. Clamp receive data to mark condition (2).
2. Force transmitter to mark (30).
3. Disable scrambler (32).
4. Wait for 180 ms (send unscrambled mark).
5. Sample PSK detector output (D2) to see if dotting pattern (alternating 1/0 pattern) is received. If dotting pattern is not received within 212 ms, output ERROR to data terminal and return to on line state.
6. Turn scrambler on (12).
7. Wait 270 ms (send scrambled mark).
8. Go to step 11 in A) above.

H. Terminating remote digital loopback:

1. Force transmitter to mark (30).
2. Clamp receive data to mark (2).
3. Turn transmitter off (5).
4. Wait 80 ms.
5. Turn transmitter on (25).
6. Wait 270 ms (send scrambled mark).
7. Go to step 11 in A) above.

I. Response to remote digital loopback request:

1. In on line state monitor unscrambled mark detector output (D3). Go to step 2 if unscrambled mark is detected.
2. Clamp receive data to mark (2).
3. Transmit dotting pattern (34).
4. Wait until unscrambled mark detector turns off.
5. Turn off dotting pattern (14).
6. Put SC11015 in digital loopback (33).
7. Remain in digital loopback until loss of carrier is detected.
8. Terminate digital loopback.
9. Return to on line state.

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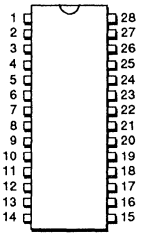
FEATURES

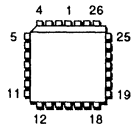
- ☐ Complete 2400 bps modem conforming to V.22 bis
- ☐ Compatible with CCITT V.22 bis, V.22, V.21 and Bell 212A and 103 standards
- ☐ Integrated DTMF/Guard Tone Generators, call progress monitor
- ☐ All loopback diagnostics
- ☐ Programmable audio port

28-PIN DIP PACKAGE



SC11006CN

28-PIN PLCC PACKAGE



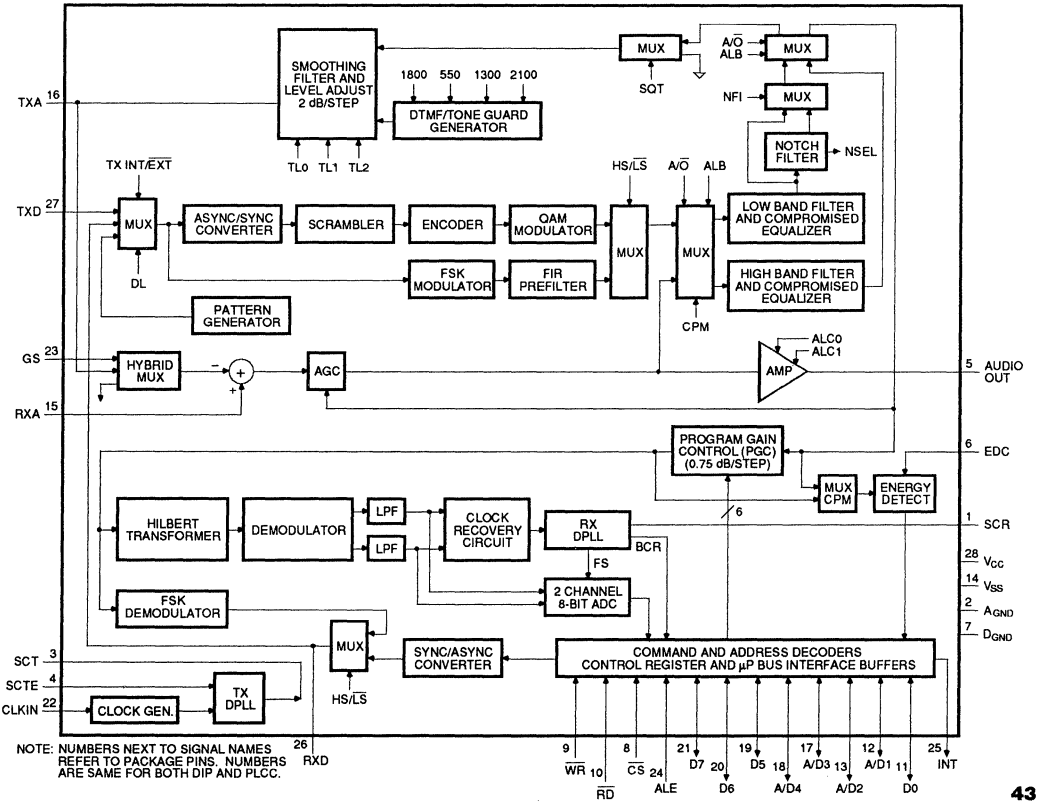
SC11006CV

GENERAL DESCRIPTION

The SC11006 is a complete 2400 bps modem IC containing all modem functions except the adaptive equalizer. It is used in conjunction with an external controller such as the Sierra SC11019 (for parallel bus applications), the SC11020 (for RS-232 applications), the SC11022 (for either configuration or ROMless microcontroller such as the Sierra SC11011, 11021, 11061 or 11091 to implement a 2400 bps full duplex intelligent modem, compatible with the CCITT V.22 bis recommendation. The controller performs all modem control and handshaking functions as well as the adaptive equalization.

The SC11006 operates in 2400 bps QPSK/QAM and 1200 bps PSK as well as 0 to 300 baud FSK modes, compatible with Bell 103 and 212A as well as CCITT V.21, V.22 and V.22bis standards. When used with the SC11019 or SC11020 controllers, the SC11006 becomes an intelligent modem controlled by the industry standard "AT" command set. The interface between the SC11006 modem and controller is a standard microcontoller interface that easily connects to the SC22201 (128 by 8) EE memory for permanent storage of configuration settings and phone numbers.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE SAME FOR BOTH DIP AND PLCC.

FUNCTIONAL DESCRIPTION OF THE SC11006 MODEM

The SC11006 includes:

- ☐ Full transmitter consisting of
  - – Async to Sync converter
  - – Scrambler
  - – Data encoder
  - – 75% square root of raised cosine pulse shaper
  - – Quadrature modulator
  - – FSK (Bell 103 and CCITT V.21) modulator
  - – Hybrid
- ☐ High band and low band filters
- ☐ High band and low band compromise equalizers
- ☐ V.22 notch filter (selectable at 550 or 1800 Hz)
- ☐ Transmit smoothing filter
- ☐ Programmable attenuator for transmit level adjust
- ☐ DTMF, 550 Hz, 1300 Hz, 1800 Hz, and 2100 Hz tone generator
- ☐ Transmit clock circuit for synchronous operation (slave, external, and internal modes)
- ☐ Pattern generator for generating fixed digital patterns in handshaking mode
- ☐ Receive section consisting of
  - – 64-step programmable gain controller (PGC)
  - – Energy detector at the output of the PGC
  - – Hilbert transformer
  - – Quadrature demodulator (free running carrier) with low pass filters
  - – Baud timing recovery circuit (sampling clock of 600 Hz)
  - – FSK demodulator
  - – Sync to Async converter
- ☐ 8-bit analog to digital converter (ADC)
- ☐ Control and Status registers
- ☐ 8-bit microprocessor interface with interrupt and multiplexed address/data lines
- ☐ Audio output with level adjust

Transmitter

Since data terminals and computers may not have the timing accuracy required for 2400/1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 2400/1200 Hz +2.3%, –2.5%. It outputs serial data at a fixed rate of 2400/1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 2400/1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first four/two stages of the shift register form the quad/dibit that is applied to the QAM/QPSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band, centered at 2400 Hz, or the low band, centered at 1200 Hz. In the 2400 bps mode, the modem actually sends four bits at a time, called a quadbit. The actual rate of transmission for a quadbit is 600 baud. This is the optimum rate of transmission over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

In the 2400 bps data rate, the data to be transmitted is divided into groups of four consecutive bits (quadbits). The first two bits of the quadbit are encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. The last two bits define one of the four signaling elements associated with the new quadrant.

In the 1200 bps data rate, the data stream is divided into groups of two consecutive bits (dibits). The dibits are used to determine the phase quadrant change relative to the quadrant occupied by the preceding signal element. The resulting signaling elements from the inphase (I) and quadrature (Q) channels are passed through baseband filters with a square root of raised cosine shape. The filtered signals subsequently modulate sine and cosine carriers, and add to form the QAM/QPSK signal. The wave-shaped signal is then passed through either the low-band or high-band filter, depending upon originate or answer mode selection.

For low speed operation, the FSK modulator is used. It produces one of four precision frequencies, depending upon originate or answer mode selection and the 1 (mark) or 0 (space) level of the transmit data. Different frequencies are used for V.21 and 212A modes. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands, and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.22 bis applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress

monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode, it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second-order low-pass switched-capacitor filter that adds the modem transmit signal to the V.22 guard tones. It also provides a 2 dB per step programmable gain function to set the output level.

Receiver

The receiver section consists of an energy detector, programmable gain control (PGC), part of the QAM/QPSK demodulator, FSK demodulator, 8-bit ADC and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to the energy detector and PGC circuit. The energy detector provides detection within 17 to 24 msec. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels. In call progress mode, the energy detector is connected to the output of the PGC to allow detection level adjustment.

The output of the receive filter is applied to the programmable gain control. This circuit has a wide overall range of 47.25 dB and provides 64 steps of 0.75 dB/step. The PGC gain is controlled by the external processor. It also provides auto-zeroing to minimize the output DC offset voltage.

The QAM/QPSK demodulator uses a coherent demodulation technique. Output of the programmable gain control (PGC) is applied to a Hilbert transformer that produces an in-phase and 90° out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by a free-running carrier. The baseband components are low-pass filtered to produce I and Q (Inphase and Quadrature) channel outputs. The I and Q channel outputs are both filtered by 300 Hz band-pass filters. Then they are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled and digitized into 8-bit samples by the ADC. Each channel (I and Q) is sampled twice during a baud period, once at the middle and once at the end of the baud period, allowing T/2 or T sampling operation. The external processor is interrupted once every baud period (1.667 msec). The processor should read the I and Q samples (within 100 µs from the time interrupt is issued), and perform adaptive equalization, carrier phase tracking, data decoding, and data descrambling. One quad/dibit is transferred from the SC11006 during each baud period.

In the asynchronous mode, data received from the processor is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are re-inserted. Underspeed data is passed essentially unchanged. The sync/async converter has two modes of operation. In the basic signaling mode, the buffer can accept an overspeed which corresponds to one missing stop bit in eight characters. The length of the start and data elements will be the same, and the stop bit will be reduced by 12.5%. In the extended-signaling range, the buffer can accept one missing stop bit in four characters and the stop bits will be reduced by 25% to allow for overspeed in the transmitting terminal. Output of the sync/async converter, along with the output of the FSK demodulator, is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed and output data received on the RXD pin.

For low-speed operation, the FSK demodulator is used. The output of

the PGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

To improve the performance of the receiver at low signal levels, while maintaining a wide amplitude range, a 1-bit AGC circuit is placed prior to the band-pass filter. The decision thresholds of this AGC are controlled by the AGCVT bit. When AGCVT = 1, the thresholds will be 6 dB further apart than when AGCVT = 0, so that the probability of gain change will be reduced. The status of the AGC gain is available through the AGCO bit. AGC will have 8 dB more gain when AGCO = 1. Status of AGCO should be monitored at every baud timing and when it makes a transition (causing a gain-hit) the PGC's gain should be modified accordingly to prevent divergence of the adaptive equalizer.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, by turning the "Hybrid" code on through the interface, this matching is provided by an external resistor connected between the TXA and RXA pins on the SC11006. The filter section provides sufficient attenuation of the out-of-band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter. The hybrid can be deactivated by the controller.

The SC11006 internal hybrid is intended to simplify the phone line interface. The internal hybrid can compensate for the loss in the line coupling transformer used in the DAA. By tying the GS pin to V_{SS}, ground, or V_{CC}, compensation levels of 0, +2, +3 dB, respectively, are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. An external hybrid circuit, shown in Figure 2, can be used to overcome these losses and achieve maximum performance. In this case, the internal hybrid must be turned off by setting bit 6 of the TXCR register to 0.

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC11006 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired value. In practice, however, there is impedance mismatch and a loss in the coupling transformer. Therefore, it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain (G_R) and transmit gain (G_T) are set by the ratios of resistors R2, R1 and R6, R5 respectively (Figure 2).

The circuit can be analyzed as follows:

$$V_R = -\frac{R2}{R1}\left(V_{TR}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)V_y$$

$$V_y = -\frac{R6}{R5}V_x$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_y = 2V_{TX}$,

$$V_R = -\frac{R2}{R1}\left(V_{TX}+V_{RX}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)2V_{TX}$$

$$= -\frac{R2}{R1}V_{RX} + \left[\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) = \frac{R2}{R1}$$

Solving for R3/R4:

$$\frac{R3}{R4} = 1 + \frac{2R1}{R2}$$

Additionally,

$$G_R = \frac{R2}{R1} \text{ and } G_T = \frac{R6}{R5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive loss in the coupling transformer is 2.5 dB, then:

$$\frac{R2}{R1} = \text{INV Log}\left(\frac{G_{RdB}}{20}\right) = \text{INV Log}\left(\frac{2.5}{20}\right) = 1.333$$

Similarly, $\frac{R6}{R5} = 1.333$ and $\frac{R3}{R4} = 2.5$

Some typical values are:

R1=20KΩ, R2=27KΩ, R3=13KΩ, R4= 5.1KΩ, R5=20KΩ, and R6=27KΩ

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6, and capacitor C1 can be eliminated, and point X can be connected to point Y in the circuit of Figure 2 to achieve a more cost effective external hybrid arrangement.

The SC11006 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, the "Hybrid" code must be turned off. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

The tone generator section consists of a DTMF generator, V.22 guard-tone, and 1300 and 2100 Hz tone generators. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and A, B, C, D, *, and # keys. The V.22 guard-tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the tone control register. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to 1300 and 2100 Hz and the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50K Ohms is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation—no attenuation, 6 dB attenuation, 12 dB attenuation, and squelch are provided through the ALC1 and ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Clock Input

CLKIN (Pin 22) of the SC11006 should be connected to a 9.8304 MHz clock source with an accuracy of ±0.01%. Alternatively, a 12.288 MHz clock can be used if the CLKSEL bit in the MCRB control register is set.

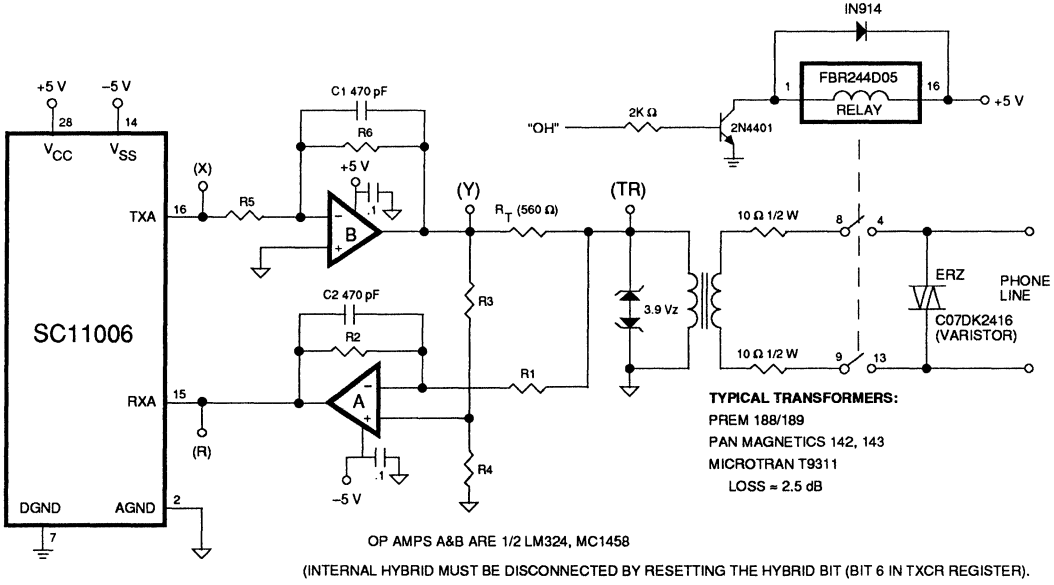


Figure 2. Using an External Hybrid with the SC11006

FUNCTIONAL DESCRIPTION OF THE SC11019, SC11020 SC11021, SC11022 AND SC11023 CONTROLLERS

The SC11019 modem controller, implemented in Sierra's 1.5 micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including a 16-bit microprocessor, 16K by 8 bytes of ROM and 128 by 8 bytes of RAM, it also contains the functionality of an 16C450 UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem for the PC consists of the SC11019 controller, the SC110024 modem and the DAA. All of the popular communications software written for the PC will work with the SC11006/SC11019 set.

Another version of the controller, the SC11020, is intended for RS-232 applications. It contains the same processor, memory, and UART as the SC11019 and has the same interface to the modem chip. The difference is that the UART is turned around so that the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The controller receives an 8-bit signal sample from the SC11006 and performs adaptive equalization, carrier phase recovery, data decode, and descrambling. SC11019 and SC11020 have identical silicon but are bonded differently in the 44 pin package. Each controller can be configured as an SC11019 or SC11020 by the software. The controller is designed by using a 16-bit 2900 processor to perform the digital signal processing and the control functions. Its instruction set is a subset of the Intel 8096 instruction set, but operates faster than the 8096.

The SC11020 provides a standard 5V logic level interface—RS-232 drivers are required to interface to the port. Like the SC11019, the SC11020 comes programmed with the Hayes "AT" command set, and when used with the SC11006 modem, emulates a Hayes-type stand-alone modem. The SC11019 and SC11024 emulate a Hayes-type IBM PC plug-in card modem.

But the chip set is by no means limited to implementing a Hayes-type smart modem. Sierra is in the custom IC business and both chips were designed with this in mind. For example, only about 15K bytes of the SC11019's ROM is used for the handshaking and smart modem code, leaving 1K bytes for additional features that a customer may specify. And since the controller is ROM programmable, any command set, not just the Hayes "AT" set, can be implemented.

Both the SC11019 and SC11020 are available in two pinout options. They are 48 pin DIP, and 44 pin PLCC.

Please refer to the SC11019 series data sheet for complete details on controller features and performance characteristics.

The SC11021 is a ROMless version of the SC11019 & 20. It is available in a 68 pin PLCC and operates with up to 24K external ROM. It can be configured for either serial or parallel operation.

A fourth version, SC11022, is available in 48 pin DIP and 68 pin PLCC. This version can be configured as either a serial or a parallel modem and comes in the 68 pin package. It can also address up to 24K external ROM.

The SC11022 includes 16K ROM programmed with the same code as SC11019 and SC11020.

Both the controllers require +5 V power supply. Besides the interface for the SC11006 modem, the SC11019 controller has an eight-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 16C450 UART. It also has control lines for ring indication, the off-hook relay, and a data/voice relay; these lines connect to the DAA.

In the SC11020, the eight-bit port becomes the switch input lines, and the address, chip select, INTO, DIST and DOST lines become the lines for the RS-232 interface, and modem status. These lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control—so the main difference between the SC11019 and SC11020 is the ROM code. The SC11020 also contains the same modem and DAA interface lines as the SC11019.

The interface to the SC11006 is via an 8-bit address/data bus and the control lines for read and write. The same interface is used for access to an electrical erasable random access memory (SC22201). There are six clock multiplexed address/data bus cycles. A ready signal is provided for the interface to a high speed PC-AT type bus cycle. For the 68 pin packages, there are 15 extra address lines and chip selects for external ROM and external RAM interfaces. An $\overline{EA}$ pin is also available for selection of internal ROM or external ROM.

The SC11019 and SC11020 are truly ASIC controllers—they are designed to control a modem or other peripheral that operates at a moderately slow data rate up to 2400 bits per second. What's unique about the SC11019, for example, is that it allows a slow peripheral to interface to a high speed bus without making the main processor add unnecessary wait states.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11019 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up, it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like a Hayes-type modem. The escape sequence is three + signs—+++ —in the default mode, but it can be changed in the software.

The actual processor contains a 16-bit data path and can execute 54 instructions with three different addressing modes: direct, indirect, and immediate. There is 16K by 8 of ROM on the chip for program storage.

To the system bus, the SC11019 looks and acts like a 16C450 UART. Communications software written for this UART will work with the SC11019 and SC11020. The Sierra chip set is truly a Hayes-type modem in two chips.

THE SC11006 & SC11019/SC11020 SYSTEM

The only external components required by the SC11006 are a 600 Ohm line matching resistor and a 1.0 μF capacitor from the EDC pin to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11024 can directly drive a high impedance (50 kΩ) earphone-type transducer.

The SC11006 modem's CLKIN pin line is driven by the SC11019 CKOUT line at 9.8304 MHz. The SC11019 interfaces directly to an IBM PC bus. The only external parts may be an 8 input NAND gate for COM1 and COM2 decoding inside the PC. A ready signal is provided to control the IOCHRDY pin on the bus to allow operation with higher speed computers (AT, XT TURBO, etc.)

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

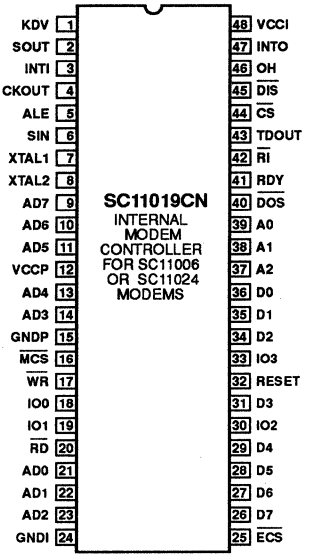
All modems require a DAA. A DAA or data access arrangement is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω; a relay for disconnecting the modem from the line; a ring detector, typically an optoisolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by one of many consultants and labs around the country. The fee is typically $2,000 and it takes several weeks. Another alternative is to buy a DAA, supplied by several manufacturers.

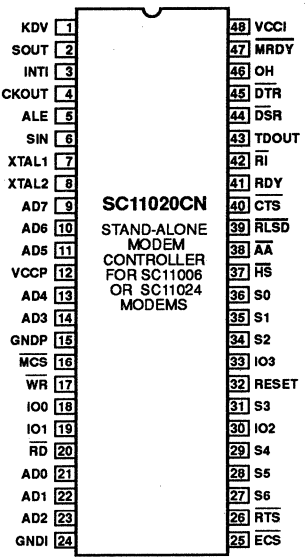
V.22bis is a CCITT specification that calls for 2400 bit per second, full or half duplex data transmission with a fallback mode of 1200 bps. It is not 2400 baud; the spec calls for transmission of quadbits—4 bits per baud so the 2400 bps transmission takes place at 600 baud. The same is true for V.22—it is 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; there is a CCITT standard for 300 bps and that's V.21.

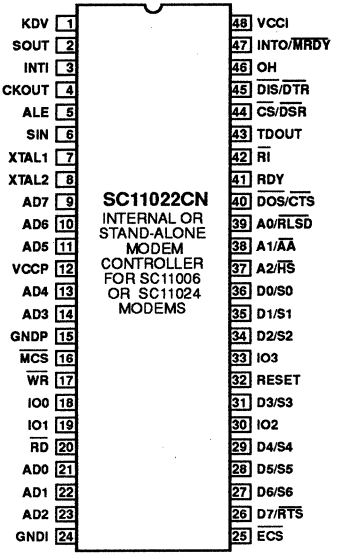
V.22 and V.22bis also call for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The SC11006 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone in the receiver.

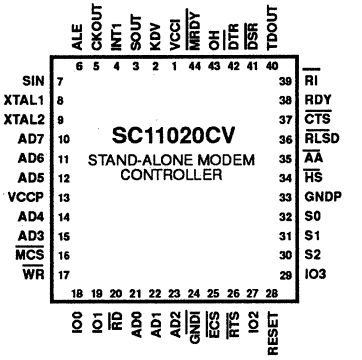
All modems require a Hybrid; a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the SC11006, this is done with op amps. The hybrid can be disabled so an external hybrid can be used, if desired.

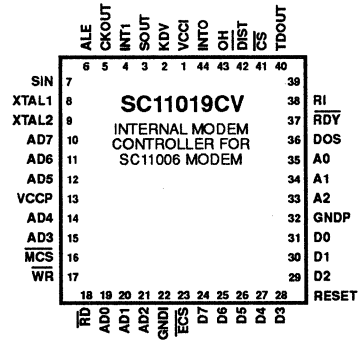
CONNECTION DIAGRAM FOR CONTROLLERS

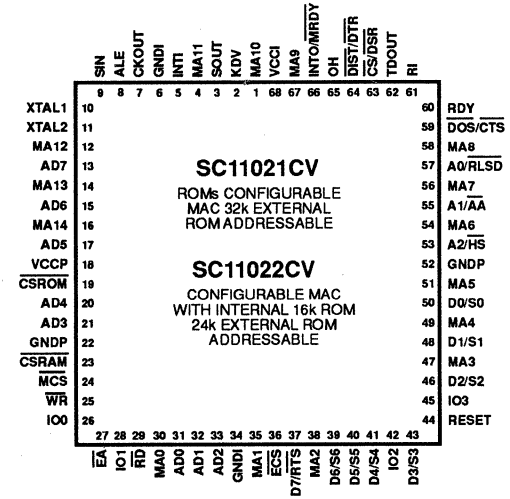












PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	SCR	Synchronous Clock Receive (Data set source); **Output; TTL;** Used only in bit synchronous mode; Recovered by the Receiver Phase Locked Loop from the far end modem. Data on RXD is valid at the rising edge of this clock.
2	AGND	Analog Ground.
3	SCT	Synchronous Clock Transmit (Data set source); **Output; TTL;** Used only in bit synchronous mode; Generated internally by the SC11006 Clock Generator; Rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
4	SCTE	Synchronous Clock Transmit External (DTE source); Input; TTL; Used only in bit synchronous mode; Data on TXD line is latched by the SC11006 at the rising edge of this clock. Clock rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
5	AUDIO	Audio output; The hybrid output is passed through a programmable attenuator and fed to this analog pin. Four different levels can be attained by controlling bit 0 and bit 1 of the AUDIO register as specified under AUDIO register description.
6	EDC	Capacitor for energy detect; A 1.0 µF capacitor should be connected between this pin and AGND.
7	DGND	Digital ground
8	$\overline{CS}$	Chip Select; Input; TTL; Active low.
9	$\overline{WR}$	Write; Input; TTL; Normally high; Data on AD7–AD0 is written into the SC11006 registers at the rising edge of this pulse.
10	$\overline{RD}$	Read; Input; TTL; Normally high; Data on AD7–AD0 is to be read by the processor at the rising edge of this pulse.
12,13,17,18	AD1–AD4	Multiplexed address/data bus (8-bits); Input/Output; TTL; A/D4–A/D1 (4-bits) are used for multiplexed addressing of internal registers.
14	V_{SS}	–5 V Supply
15	RXA	Receive analog; Input
16	TXA	Transmit analog; Output
11,19–21	D0, D5–D7	Bits 0, 5, 6 and 7 are don't cares as far as address is concerned.
22	CLKIN	Clock input; 9.8304 MHz or 12.288 MHz clock input from the controller.
23	GS	Gain Select to compensate for loss in line coupling transformer. When left open or tied to V_{SS}, the compensation is 0 dB; connected to ground, +2 dB compensation is provided; and when tied to V_{CC}, the compensation is +3 dB.
24	ALE	Address Latch Enable; Input; TTL; The address on A/D4–A/D1 is latched into the SC11006 Address decoder at the falling edge of this normally low pulse.
25	INT	Interrupt; **Output; TTL;** Normally low; A short (13 µs typical) positive pulse is generated after all A to D conversions are completed.
26	RXD	Received Data; **Output; TTL**
27	TXD	Transmit Data; Input; TTL
28	V_{CC}	+5 V supply

REGISTERS

There are twelve 8-bit registers interfacing to the microprocessor bus. Five of these registers can only be read by the processor (called READ registers) and the remaining seven can be written into by the processor (called CONTROL registers). Bit 1 of the "Tone" register can be read and written by the processor, Table 1 shows the address and bit assignments for these registers.

A chip select pin is provided for multi-peripheral addressing by the processor.

Table 1. READ Registers

ADDRESS BITS				NAME	MSB			BIT NUMBER				LSB
A4	A3	A2	A1		7	6	5	4	3	2	1	0
0	0	0	0	Q1	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
0	0	0	1	I1	I17	I16	I15	I14	I13	I12	I11	I10
0	0	1	0	Q2	Q27	Q26	Q25	Q24	Q23	Q22	Q21	Q20
0	0	1	1	I2	I27	I26	I25	I24	I23	I22	I21	I20
0	1	0	0	Status	X	X	X	AGCO	PA	PR	FSKD	ED
0	1	X	1	Unused		Unused						
0	1	1	X	Unused		Unused						

STATUS Register: Address (A4–A1) = 0100

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–5	Unused	
Bit 4	AGCO	Status of internal 1-bit AGC. When this bit is set, RXA signal is amplified by 8 dB before entering the bandpass filters.
Bit 3	PA	This bit is set whenever the clock recovery DPLL advances one step (skips a count) to lock. It is cleared only when STATUS register is read.
Bit 2	PR	This bit is set whenever the clock recovery DPLL retards one step (adds an extra count) to lock. It is cleared only when STATUS register is read.
Bit 1	FSKD	Received FSK data. FSKD = 1 when mark is received.
Bit 0	ED	Energy detect circuit output. ED = 1 when energy detected.

Note 1: When DPLL neither advances nor retards, then PA = PR = 0.
Note 2: When reading unused bits, the corresponding bus lines will not be driven by the SC11024 and will be floating.

Table 1a. READ Registers

Q1 Register:	Stores midbaud inphase sample output of ADC.
I1 Register:	Stores midbaud quadrature sample output of ADC.
Q2 Register:	Stores endbaud inphase sample output of ADC.
I2 Register:	Stores endbaud quadrature sample output of ADC.

Note: All samples are represented in two's complement form.

Table 2. CONTROL Registers

ADDRESS BITS				NAME	BIT NUMBER							
A4	A3	A2	A1		7	6	5	4	3	2	1	0
1	0	0	0	TXCR	X	HYBRID	TXSEL2	TXSEL1	TXSEL0	SQT	BR1	BR0
1	0	0	1	MCRA	X	LCK/$\overline{INT}$	RNGX	SYNC	WLS1	WLS0	A/$\overline{O}$	RXMRK
1	0	1	0	MCRB	X	X	CLKSEL	CPM	ALB	TL2	TL1	TL0
1	0	1	1	TONE	X	HNDSHK	TONEON	DTMF	D3	D2	D1	D0
1	1	0	0	PGCR	X	AGCVT	G5	G4	G3	G2	G1	G0
1	1	0	1	DATA	X	PLLJAM	PLLFRZ	PLLFAST	RD3	RD2	RD1	RD0
1	1	1	0	AUDIO	X	DISS	PGCZ	TST2	TST1	TST0	ALC1	ALC0
1	1	1	1					UNUSED				

Transmit Control Register (TXCR): Address (A4–A1) = 1000

(Note: When writing into these registers, the bus lines corresponding to the unused bits are ignored by the SC11006.)

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	HYBRID	When set, the transmitter output (TXA) is connected to the inverting input of the receive buffer to allow the use of the on-chip hybrid circuit for 2 to 4 wire conversion.
Bit 5 Bit 4 Bit 3	TXSEL2 and TXSEL1 and TXSEL0	Transmit Select bits. These 3 bits determine the data transmitted by the transmitter according to the following table:

TXSEL2	TXSEL1	TXSEL0	TRANSMITTED DATA
0	0	0	External data sent by DTE.
0	0	1	Unscrambled S1 (Note 1).
0	1	0	Unscrambled Space.
0	1	1	Unscrambled Mark.
1	0	0	Scrambled RX. Digital loop back mode (Note 2).
1	0	1	Scrambled Reversals (Notes 3 and 4).
1	1	0	Scrambled Space (Note 4).
1	1	1	Scrambled Mark (Note 4).

Note 1: S1 is a pattern of 0011 transmitted at 1200 bps rate regardless of BR1. If in FSK mode (BR0 = 1), then reversals are sent. This pattern cannot be sent at 2400 bps rate.

Note 2: In this mode, the received data, after being descrambled, is sent back to the scrambler. The modem will automatically go to the Synchronous mode with Slave timing.

Note 3: Reversals are continuous streams of 01.

Note 4: When in FSK mode (BR0 = 1), TXSEL2 is ignored since scrambling is not applicable.

Bit 2	SQT	When this bit is set, the transmitter is squelched by connecting the output of MUX1 (see the block diagram) to analog ground.
Bit 1 Bit 0	BR1 and BR0	Bit Rate Selection bits based on the following table:

BR1	BR0	BIT RATE
0	0	2400 bps V.22 bis
1	0	1200 bps V.22/212A
0	1	0–300 bps Bell 103
1	1	0–300 bps CCITT V.21

CONTROL REGISTERS (Cont.)

Mode Control Register A (MCRA): Address (A4–A1) = 1001

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	unused	
Bit 6	LCK/INTB	Determines the clock source for the transmitter. When this bit is set, the clock source is externally provided on SCTE (pin 4), and when cleared, it is internally generated (SCT). This bit can select the clock source independent of Sync/Async mode selection (see below). When in Digital Loop-Back mode, the clock source will be forced to the Slave mode (SCR).
Bit 5	RNGX	Range extender for the receiver Sync/Async converter. When set, the receiver Sync/Async can insert up to one stop bit per four (8, 9, 10 or 11-bit) characters to compensate for a far end DTE being up to 2.3% over speed. The transmitter Async/Sync always handles this overspeed condition regardless of this bit's condition.
Bit 4	SYNC	When set, operate in bit synchronous mode; when clear, operate in character asynchronous mode. When in Digital Loop-Back mode, the SC11006 will be forced to the Synchronous mode.
Bit 3 and Bit 2	WLS1 and WLS0	Word length select bits in asynchronous mode, according to the following table:

WLS1	WLS0	NUMBER OF BITS PER CHARACTER
1	0	8
1	1	9
0	0	10
0	1	11

Bit 1	A/$\overline{O}$	When set, operate in answer mode; when clear, operate in originate mode.
Bit 0	RXMARK	When set, the RXD pin is clamped to the high logical level.

Mode Control Register B (MCRB): Address (A4–A1) = 1010

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	unused	
Bit 6	unused	
Bit 5	CLKSEL	This bit must be set when CLKIN = 12.288 MHz, and clear when CLKIN = 9.8304 MHz.
Bit 4	CPM	Call progress monitor mode. When set, the receive path can be connected to the high band filter to detect answer tone (ALB=0) or to the low band filter scaled down 2.5 times (ALB=1) to listen for the call progress tones during auto dialing.
Bit 3	ALB	Analog Loop Back. When set, the transmitter output (TXA) is connected to the receive path, bypassing the receive filter.
Bit 2 and Bit 1 and Bit 0	TL2 and TL1 and TL0	Transmit level adjust bits based on the following table:

TL2	TL1	TL0	TRANSMIT LEVEL AT TXA PIN
0	0	0	0 dBm
0	0	1	–2 dBm
0	1	0	–4 dBm
0	1	1	–6 dBm
1	0	0	–8 dBm
1	0	1	–10 dBm
1	1	0	–12 dBm
1	1	1	–14 dBm

CONTROL REGISTERS (Cont.)

TONE Register: Address (A4–A1) = 1011

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	HNDSHK	This bit is set only during handshaking sequence. When set, both FSK and PSK/QAM demodulators are enabled. When cleared, FSK demodulator is disabled when in high speed mode.
Bit 5	TONEON	When set, the output of the tone generator appears at TXA. When cleared, the output of the tone generator is squelched.
Bit 4	DTMF*	When set, the DTMF generator is turned on. When cleared, the DTMF generator is turned off, but other tones can be generated.
Bits 3–0	D3–D0	Specify the desired tone (see the following table):

DTMF	D3	D2	D1	D0	DIGIT DIALED	TONE OUTPUT	FREQUENCIES (HZ)
1	0	0	0	0	0	941	1336
1	0	0	0	1	1	697	1209
1	0	0	1	0	2	697	1336
1	0	0	1	1	3	697	1477
1	0	1	0	0	4	770	1209
1	0	1	0	1	5	770	1336
1	0	1	1	0	6	770	1477
1	0	1	1	1	7	852	1209
1	1	0	0	0	8	852	1336
1	1	0	0	1	9	852	1477
1	1	0	1	0	*	941	1209
1	1	0	1	1	(A)	697	1633
1	1	1	0	0	(B)	770	1633
1	1	1	0	1	(C)	852	1633
1	1	1	1	0	#	941	1477
1	1	1	1	1	(D)	941	1633
0	0	0	0	0	No tone; tone generator turned off		
0	0	0	0	1	550		
0	0	0	1	0	1800		
0	0	0	1	1	2100		
0	0	1	0	0	1300		
0	0	1	0	1	No tone; tone generator turned off		
0	0	1	1	x	No tone; tone generator turned off		
0	1	x	x	x	No tone; tone generator turned off		

Note: TONEON must also be set to generate DTMF signals.

Programmable Gain Controller Register (PGCR): Address (A4–A1) = 1100

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	AGCVT	When set, prevents gain hit due to AGC's gain step. This bit must be set during the handshaking after detecting the four point constellation and before switching to 16-way decision making.
Bits 5–0	G5–G0	Control the gain of the PGC within a range from –10 to +37.5 dB in 0.75 dB steps. (See the following table):

CONTROL REGISTERS (Cont.)

G5	G4	G3	G2	G1	G0	PGC GAIN (dB)
0	0	0	0	0	0	–10.0
0	0	0	0	0	1	–9.25
0	0	0	0	1	0	–8.5
0	0	0	1	0	0	–7.0
0	0	1	0	0	0	–4.0
0	1	0	0	0	0	+2.0
1	0	0	0	0	0	+14.0
1	1	1	1	1	1	+37.25

Note: Signal level is adjusted (before entering the filter) by an internal AGC with +12 dB or 0 dB gain, plus a fixed gain of 5 dB.

DATA Register: Address (A4–A1) = 1101

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	PLLJAM	When this bit is set, the DPLL will be reset by the next rising edge of the received baud clock. This bit must remain high for at least one baud period. It should be cleared by the processor to end the jamming mode. PLLFRZ (see below) overrides PLLJAM when both are enabled.
Bit 5	PLLFRZ	Phase locked loop freeze. When this bit is set, the DPLL begins to run freely regardless of the received baud clock. To re-enable the DPLL locking, the bit must be cleared by the processor. PLLFRZ overrides PLLJAM when both are enabled.
Bit 4	PLLFAST	When set, the DPLL operates in "fast" locking mode. In this mode, the DPLL is updated on every baud period by 13 µs steps. When this bit is cleared (default mode), the DPLL operates in "normal" locking mode and is updated once every 8 baud periods by 6.5 µs steps.
Bit 3–0	RD3–RD0	Four-bit Received Data. Used only in high speed (1200 or 2400 bps) mode, they are descrambled by the processor and shifted out by the SC11006. Sync to Async is also done by the SC11006, when in the asynchronous mode. RD0 is the first bit appearing on the RXD pin, followed by RD1, RD2 and RD3. In the 1200 bps mode, only RD0 and RD1 are shifted out during one baud period.

AUDIO Register: Address (A4–A1) = 1110

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	DISS	When this bit is set, the scrambler is disabled, when cleared, it is enabled. Transmit select bits (TXSEL0–2) override this bit when in "transmit internal mode".
Bit 5	PGCZ	When set, the output of the PGC is grounded. DC offset of the demodulator can be stored and canceled by the controller.
Bit 4–2	TEST	Test bits used for factory testing. For normal chip operation, these bits must be cleared.
Bit 1	ALC1	Audio level control bit 1.
Bit 0	ALC0	Audio level control bit 0. These two bits are used to control the audio level at AUDIO pin according to the following table:

ALC1	ALC0	AUDIO ATTENUATION (dB)
0	0	Audio off
0	1	12
1	0	6
1	1	0 (no attenuation)

Note: The audio signal may be amplified by 12 dB by the line receiver AGC before being fed to the audio attenuator.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1—SC11006 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 3.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11006 in the synchronous mode. This provides a 2400/1200 Hz clock on the SCT pin that can be used as a clock source for the DTE. The Transmit Phase-Locked-Loop (TX PLL) of the SC11006 will be in free-running mode.

Case 2—SC11006 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode, also select "Locked" mode.

The TX PLL of SC11006 will then synchronize itself to the clock provided on its "SCTE" pin.

Case 3—Slave mode. The Transmit Timing is slaved to the receiver recovered clock. Select synchronous mode and connect SCTE to SCR.

In either case, the SC11006 will sample the data on the rising edge of the clock.

Receiver Timing

In synchronous mode, the recovered clock will be provided on the SCR pin and the transitions of RXD will be on the falling edges of this clock. Data is valid on the rising edge of the clock.

SYNCHRONOUS MODE CHART

Transmitter Timing

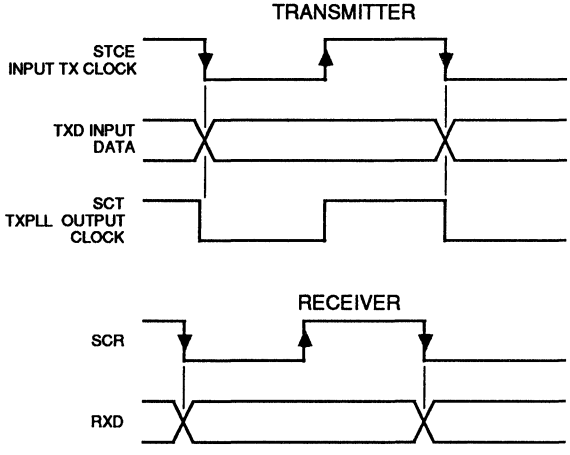


Figure 3. SC11006 Synchronous Mode Timing Diagrams.

SC11006 SPECIFICATIONS

Absolute Maximum Ratings (Notes 1–3)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS}–0.6 to V_{CC} +0.6 V
DC Input Voltage (Digital Signals)	V_{SS}–0.6 to V_{CC} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
F_C	Clock Frequency	CLKSEL = 0	9.8295	9.8304	9.8313	MHz
		CLKSEL = 1	12.2868	12.288	12.2892	MHz
T_R, T_F	Input Rise or Fall Time	All digital inputs except CLKIN			500	ns
T_R, T_F	Input Rise or Fall Time	CLKIN			20	ns

DC Electrical Characteristics (T_A = 0 TO 70°C, V_{CC} = +5 V ± 10%, V_{SS} = –5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	Normal		18	35	mA
I_{SS}	Quiescent Current			18	35	mA
V_{IH}	High Level Input Voltage; Digital pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital pins				0.8	V
V_{OH}	High Level Ouput (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Ouput (I_{OL} = 1.6 mA)				0.6	V
VXTA	Maximum Peak Output Level on TXA pin	V_{CC} = +5 V V_{SS} = –5 V	±3			V

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

SC11006 SPECIFICATIONS (Cont.)

AC Electrical Characteristics

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
		Processor Bus Interface: (See Figure 4)					
1	TMCAL	MCS low to ALE high		10			ns
2	TALE	ALE pulse width		40			ns
3	TAVLE	Address valid to ALE low		30			ns
4	THAD	Hold address after ALE low		40			ns
5	TALRD	Delay from ALE low to $\overline{RD}$ low		45			ns
6	TDVRL	Data valid after $\overline{RD}$ low				180	ns
7	TDH	Data hold after $\overline{RD}$ high		0			ns
8	TWR	Write pulse width		148			ns
9	TDVWR	Data setup before $\overline{WR}$ high		40			ns
10	TDHWR	Data hold after $\overline{WR}$ high		0			ns
11	TRHLH	End of $\overline{RD}$ to next ALE		55			ns
12	TWHLH	End of $\overline{WR}$ to next ALE		120			ns

BUS TIMING

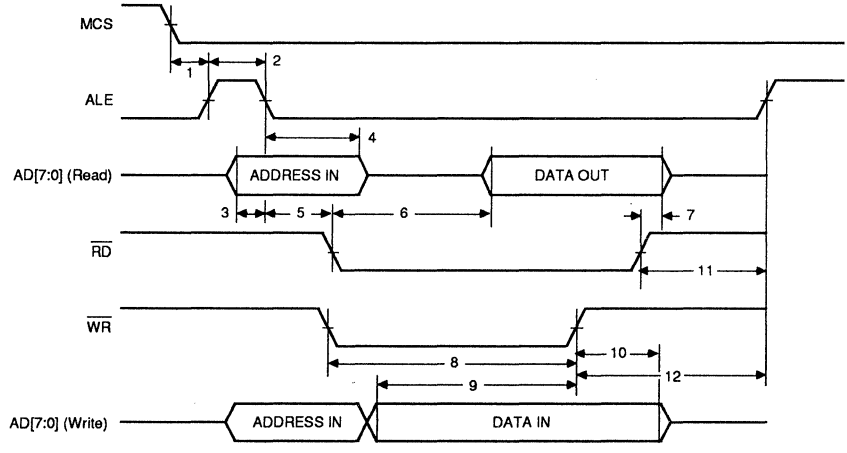


Figure 4. Processor Bus Timing

When the controller is reading or writing to the SC1106, the address must be valid at least 30 ns before ALE goes low and stay valid 40 ns or more.

When the controller is writing, data must be valid at least 40 ns before $\overline{WR}$ goes false and stay valid until at least 0 ns after $\overline{WR}$ goes false.

When reading from the MAP, data is valid a maximum of 185 ns after $\overline{RD}$ goes true and stays valid at least until 0 ns after $\overline{RD}$ goes false.

SC11006 SPECIFICATIONS (Cont.)

Modem Transmit Signals—Hz (Assume 9.8304 Crystal)

PARAMETER	CONDITIONS	NOM.	ACT.	UNITS
FSK Mod/Demod Frequencies				
Bell 103				
Answer Mark		2225	2226	Hz
Answer Space		2025	2024.4	Hz
Originate Mark		1270	1269.4	Hz
Originate Space		1070	1070.4	Hz
CCITT V.21				
Answer Mark		1650	1649.4	Hz
Answer Space		1850	1850.6	Hz
Originate Mark		980	978.34	Hz
Originate Space		1180	1181.53	Hz

Call progress monitor mode:		MIN	TYP	MAX	
Center frequency	ALB = 1		480		Hz
Detect level (ED high) measured at RXA		–43			dBm
Reject level (ED low) measured at RXA				–48	dBm
Hysterisis		2			dB
Delay time (ED low to high)	EDC = 1.0 µF	10	15	24	ms
Hold time (ED high to low)	EDC = 1.0 µF	10	15	24	ms

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQUENCY	ALLOWABLE ERROR	ACTUAL ERROR
Row 1	697 Hz	±1%	–0.23%
Row 2	770 Hz	±1%	–0.01%
Row 3	852 Hz	±1%	–0.12%
Row 4	941 Hz	±1%	–0.39%
Column 1	1209 Hz	±1%	–0.35%
Column 2	1336 Hz	±1%	–0.93%
Column 3	1477 Hz	±1%	–0.48%
Column 4	1633 Hz	±1%	–0.91%
Guard Tones	550 Hz	±20 Hz	–2 Hz
	1800 Hz	±20 Hz	–2 Hz
Calling Tone	1300 Hz		–6 Hz
Answer Tone	2100 Hz		–12 Hz

SC11006 SPECIFICATIONS (Cont.)

DTMF Generator (Cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion	VCC = +5 V VSS = –5 V TL2 = TL1 = TL0 = 0 Measured at TXA Pin		–40		dB
Row Output Level			0		dBm
Column Ouput Level			2		dBm
550 Hz Guard Tone			–3		dB (Note 2)
1800 Hz Guard Tone			–6		dB (Note 2)
1300 Hz Calling Tone			0		dB
2100 Hz Answer Tone			0		dB
Transmit level measured at TXA	Load = 1200 Ohms TL2 = TL1 = TL0 = 0 Squelched		0	 –50	dBm dBm

Notes: 1: This assumes a clock of exactly 9.8304 MHz.

2: These levels are referenced to the TX signal level. When guard tones are added, the TXA level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Mode	EDC = 1.0 µF; measured at RXA PGC = 0				
Energy detect level (ED low to high)				–43	dBm
Loss of energy detect level (ED low to high)		–48			dBm
Hysterisis		2	3		dB

Programmable Gain Controller (PGC)

Gain step size			0.75		dB
Dynamic range			47.25		dB
Response time (from change in PGC register to output of A to D converter)			1.0		ms

Filter Characteristics

Crosstalk rejection			70		dB
Power supply rejection			0		dB
DPLL Response times JAM or FRZ Fast			20 200		µs µs

APPLICATIONS INFORMATION

Applications

The SC11006 with an external control microprocessor, a telephone line interface and a suitable computer interface, can implement a complete 2400 bps modem for many applications with a minimum of components and cost. Figure 7 shows the common portion of such a modem using the SC11006 with a telephone line interface. Sierra's SC22101, 128 byte E^2 memory is used to store default parameters and often used phone numbers. The SC11019/20/21/22 controllers also support a serial E^2 memory as an alternative. Figures 6 and 7 show the stand-alone and PC bus integral modems implemented with Sierra's SC11019/20 controllers. Figure 8 shows the connections for an internal ROM special purpose controller using the SC11021. Figure 9 shows an RS-232C serial interface for implementing a stand-alone modem. Figure 10 shows a parallel bus interface for implementing an internal modem for an IBM PC/XT/AT compatible computer when used with Sierra's SC11019 controller shown in Figure 6, while Figure 13 shows the interface required for implementing the same internal modem when used with the controller shown in Figure 12. Figure 11 shows a power supply schematic for a stand-alone modem application.

Various modem configurations can be realized by combining schematics shown in Figures 5 thru 13.

A Hayes compatible stand-alone smart modem (Fig. 5) can be implemented by combining Figures 7, 8, 9 and 11.

The internal version for an IBM PC/XT/AT compatible (Fig. 6) can be implemented using Figures 7, 8 and 10.

An Alternative to the controller of Figure 8 is shown in Figures 12 and 13.

For performance evaluation, the circuit shown in Figure 14 can be used to obtain the receiver constellation. Quality of the signal processing performed by the modem can thus be visualized by observing the constellation for various line conditions and signal to noise ratios.

Power Supply Decoupling and Circuit Layout Consideration

For optimum performance at low received signal levels with low s/n ratios, it is important to use the recommended power supply decoupling circuit as shown in Figure 7.

Small inductors in series with the supplies help suppress RFI as well as improve the power supply noise rejection capability of the SC11006. A 10 Ω, 1/4 W resistor in place of, or in series with, the inductor in the SC11006 power leads has been found to be helpful in computer based products where the power supplies are particularly noisy.

The 10 µF capacitors should be a tantalum type while the 0.1 µF capacitors should have good high frequency rejection characteristics—monolithic ceramic types are recommended. It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11006 as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply. Avoid routing digital traces through the analog area.

Ferrite beads on the ±5 V input to the circuit board should also be considered, both from a modem performance standpoint, as well as an aid in reducing RF radiation from the phone lines.

Note: Crystal oscillator: The controller requires a parallel resonant 19.6608 MHz crystal designed with CL = 18 pF and tolerance of ± .01% (such as Saronix NYP196-18). With this crystal, use 27 pF to ground from XTAL1 (Pin 10) and XTAL2
(Pin 11). Clock frequency measured at CKOUT (Pin 7) must be within ±0.01% of 9.8308 MHz.

APPLICATIONS INFORMATION (Cont.)

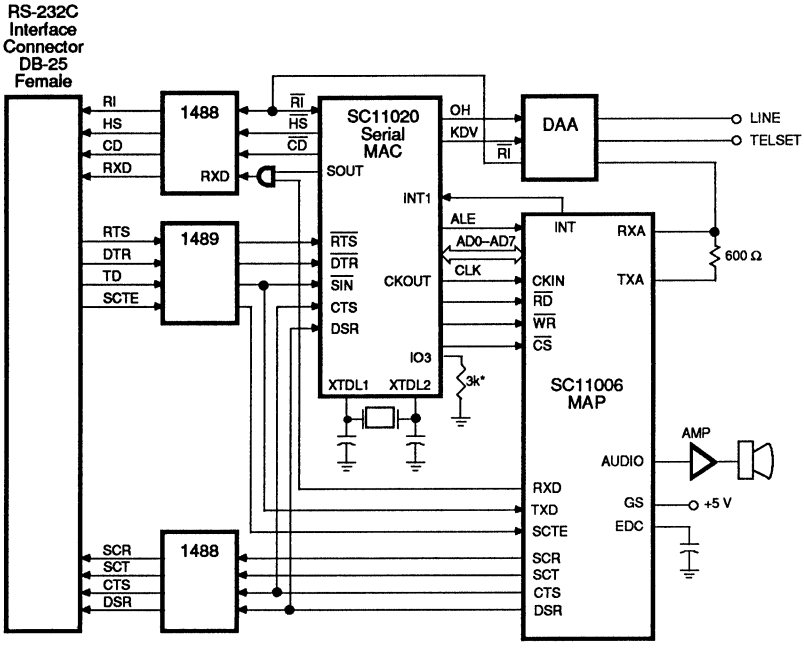


Figure 5. V22 bis Standalone Intelligent Modem with Internal ROM.

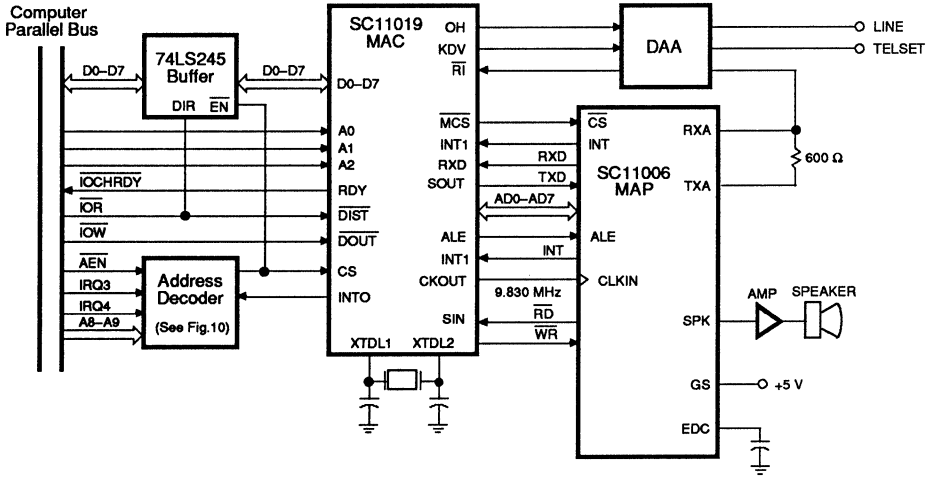
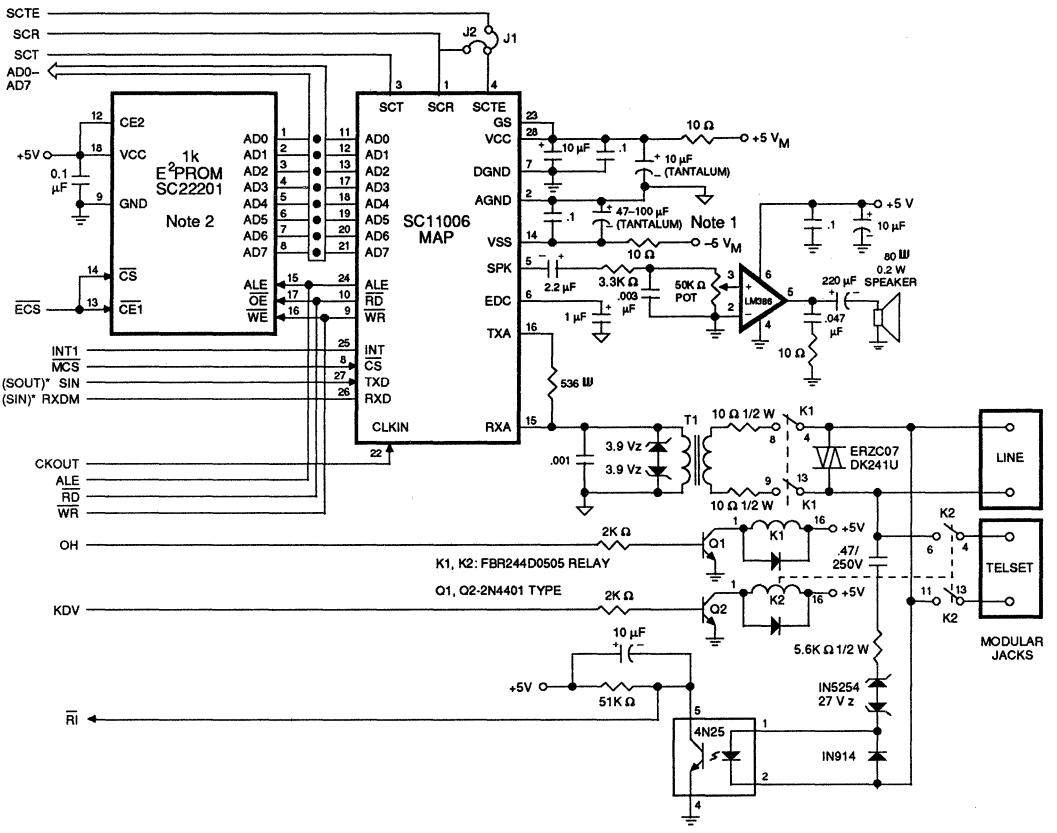


Figure 6. Internal Smart Modem for PC Bus Applications with Internal ROM.

APPLICATIONS INFORMATION (Cont.)



Note 1: Connect analog ground directly to common of the power supply filter capacitor.

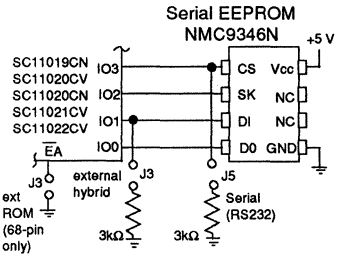
Note 2: A serial E^2PROM may be substituted when using the SC11019, SC11020, SC11021 or SC11022 Modem Advanced Controller (48 and 68 pin versions), or SC11020 44 pin version.

Note 3: For external clocking of the transmitter, install J1 and set bit 6 of the MCRA; omit J2.
For slave clocking of the transmitter, install J2 and set bit 6 of the MCRA; omit J1.
For normal operation, omit J1 and J2, and clear bit 6 of the MCRA.

*When used in the configuration as a parallel modem (Figure 6), connect Pin 27 of SC11006 to SOUT pin of controller and connect Pin 26 of SC11006 to SIN pin of controller.

Figure 7. Common Portion of 2400 BPS Modem.

CONFIGURATIONS FOR SC11019CN, 20CN, 20CV, 22CV BIG MACS



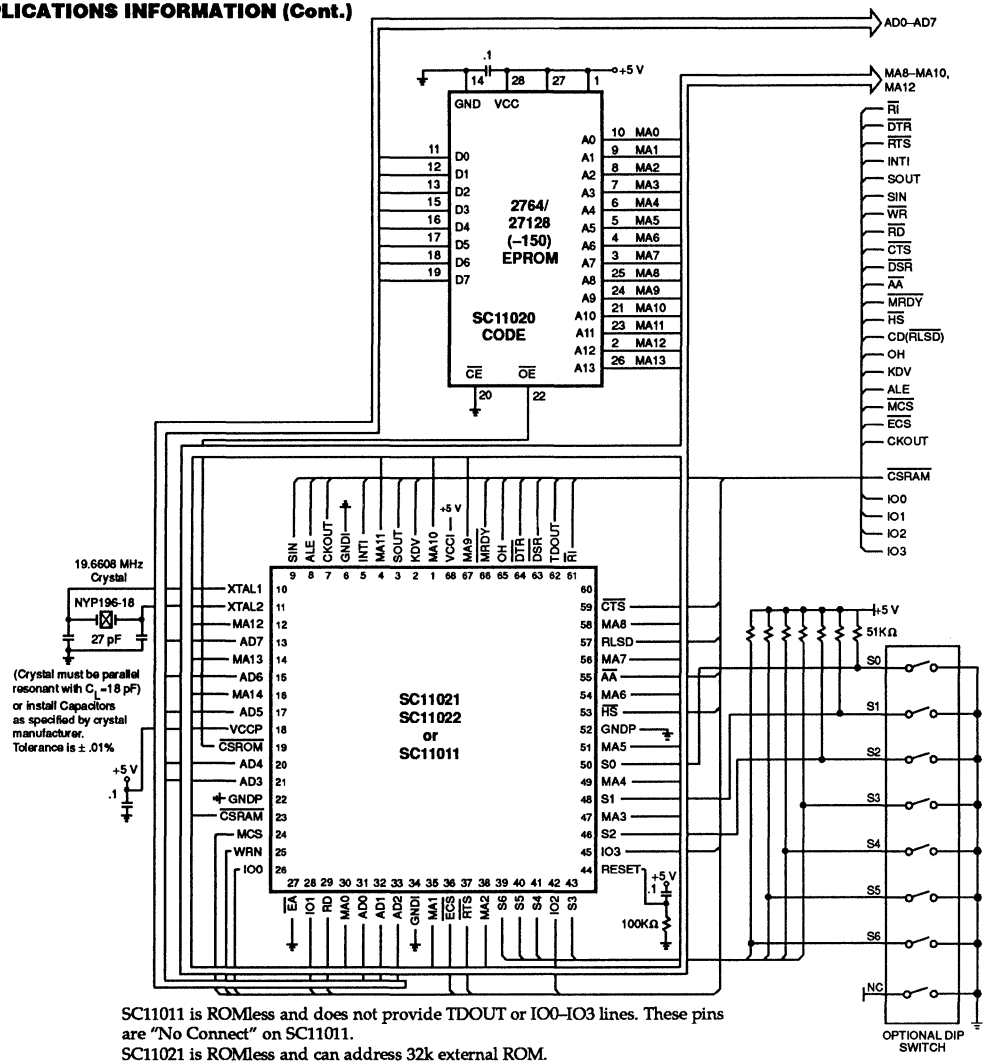
All models listed above can operate with either serial or multiplexed EEPROMs for configuration and number storage. The internal ROM program automatically determines which kind of EEPROM is connected and adapts accordingly.

Note that the SC11022 pin configuration matches that of the SC11011 controller except five new pins are used that were formerly not connected. Four of these are the I/O pins described above. One is the TDOUT pin which will be used in later versions for V.23 signalling.

When substituting SC11022 for SC11011 it is only necessary to open the EA pin and remove the external EPROM. Connect the jumpers as shown if required to operate with external hybrid or in serial mode.

Three of the four I/O pins on the specified models of the internal ROMed MAC are programmed to set the configuration at power-up or reset. Internal weak pull-up resistors will set the

APPLICATIONS INFORMATION (Cont.)



SC11011 is ROMless and does not provide TDOUT or IO0–IO3 lines. These pins are "No Connect" on SC11011.
SC11021 is ROMless and can address 32k external ROM.
SC11022 has 16k internal ROM and can address 24k external ROM.
Consult controller data sheet for programming information.

Figure 8. Special Purpose Control Processor for Stand-Alone or Parallel Applications.

default configuration to internal hybrid, and Parallel mode if there is no external pull-down.

External pull-down resistors must be added to select other options as indicated in the table. The I/O drivers will overcome these pull-up or pull-down resistors in normal operation to operate the serial EEPROM. The I/O pins may be directly grounded if the serial EEPROM is not used.

In the 44-pin version of SC11019, the I/O pins are not externally available.

CONT. PART NO.	PACKAGE	INT. ROM	EXT. ROM	UART MODE
SC11019CV	44-PLCC	16 k	–	Parallel
SC11019CN	48-DIP	16 k	–	Parallel
SC11020CV	44-PLCC	16 k	–	Serial
SC11020CN	48-DIP	16 k	–	Serial
SC11021CV	68-PLCC	0	32 k	Serial/Par.
SC11022CV	68-PLCC	16 k	24 k	Serial/Par.
SC11022CN	48-DIP	16 k	–	Serial/Par.
SC11023CV	44-PLCC	16 k	24 k	Parralel

APPLICATIONS INFORMATION (Cont.)

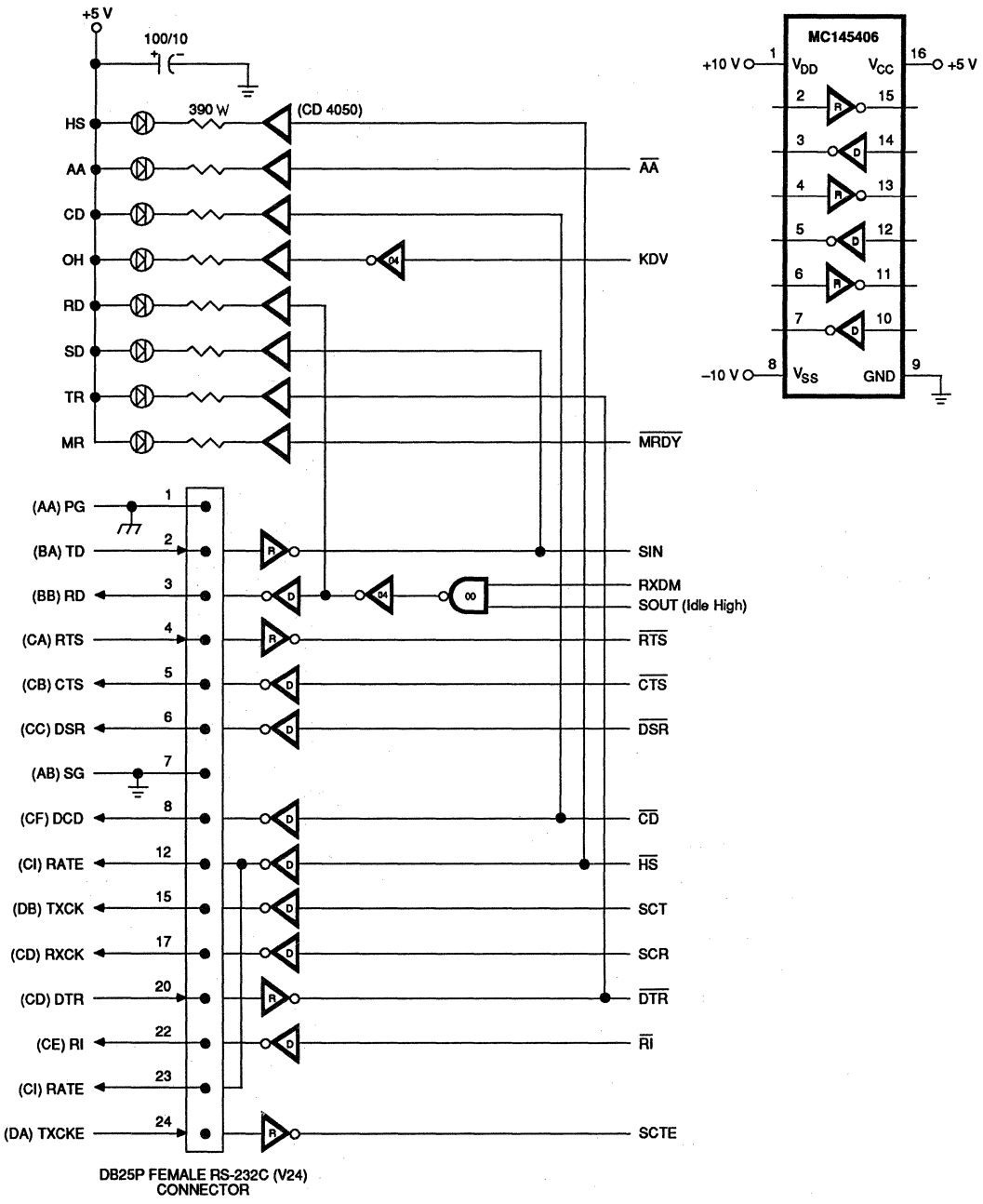


Figure 9. RS-232C Interface for Stand-Alone Modem Application.

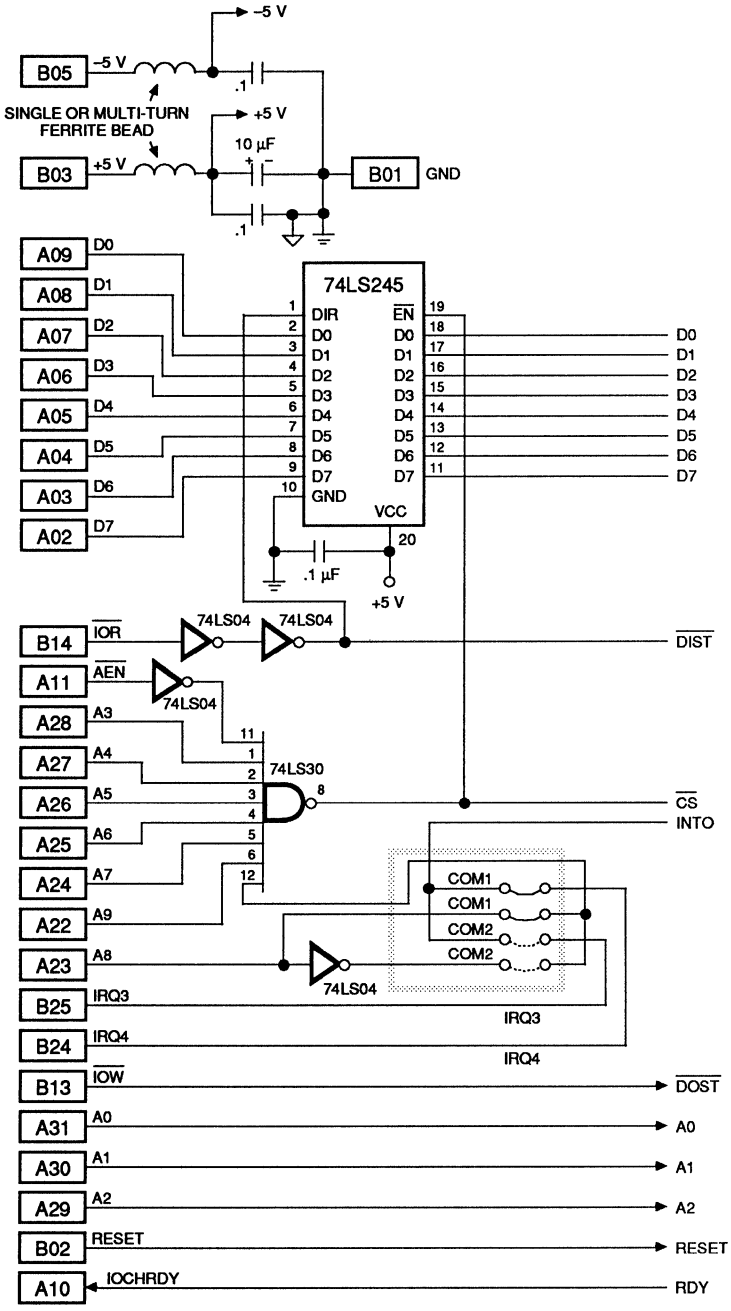


Figure 10. IBM PC/XT/AT Compatible Computer Bus Interface for SC11019 Controller of Figure 7.

APPLICATIONS INFORMATION (Cont.)

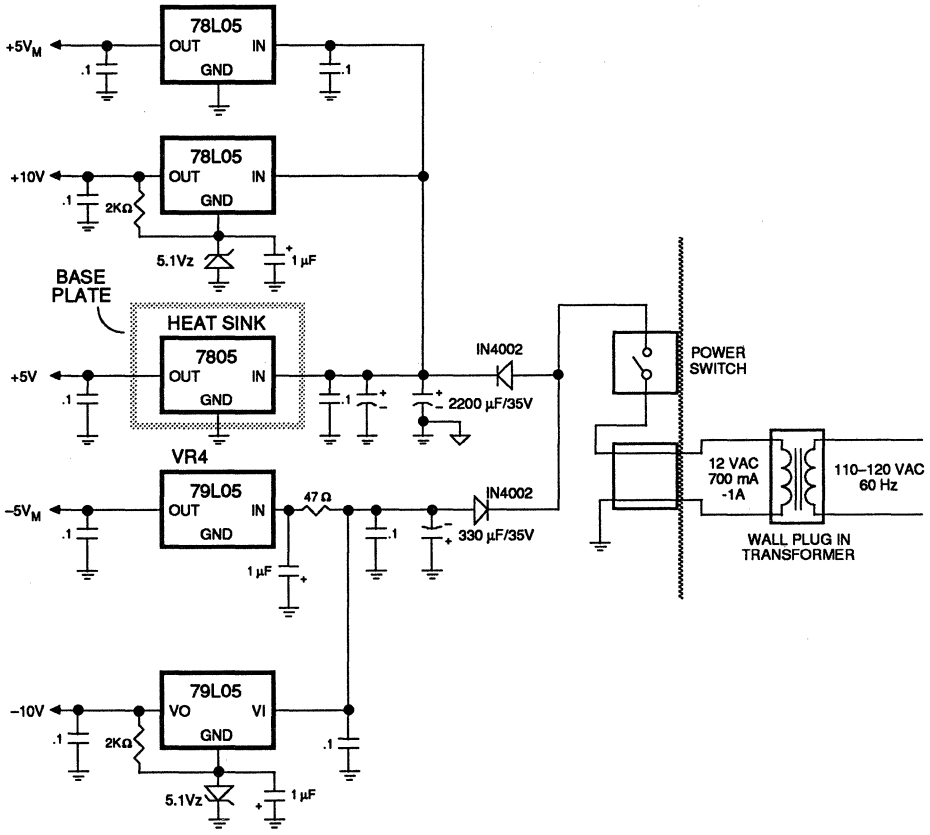


Figure 11. A Typical Power Supply for Stand-Alone Modem Application.

APPLICATIONS INFORMATION (Cont.)

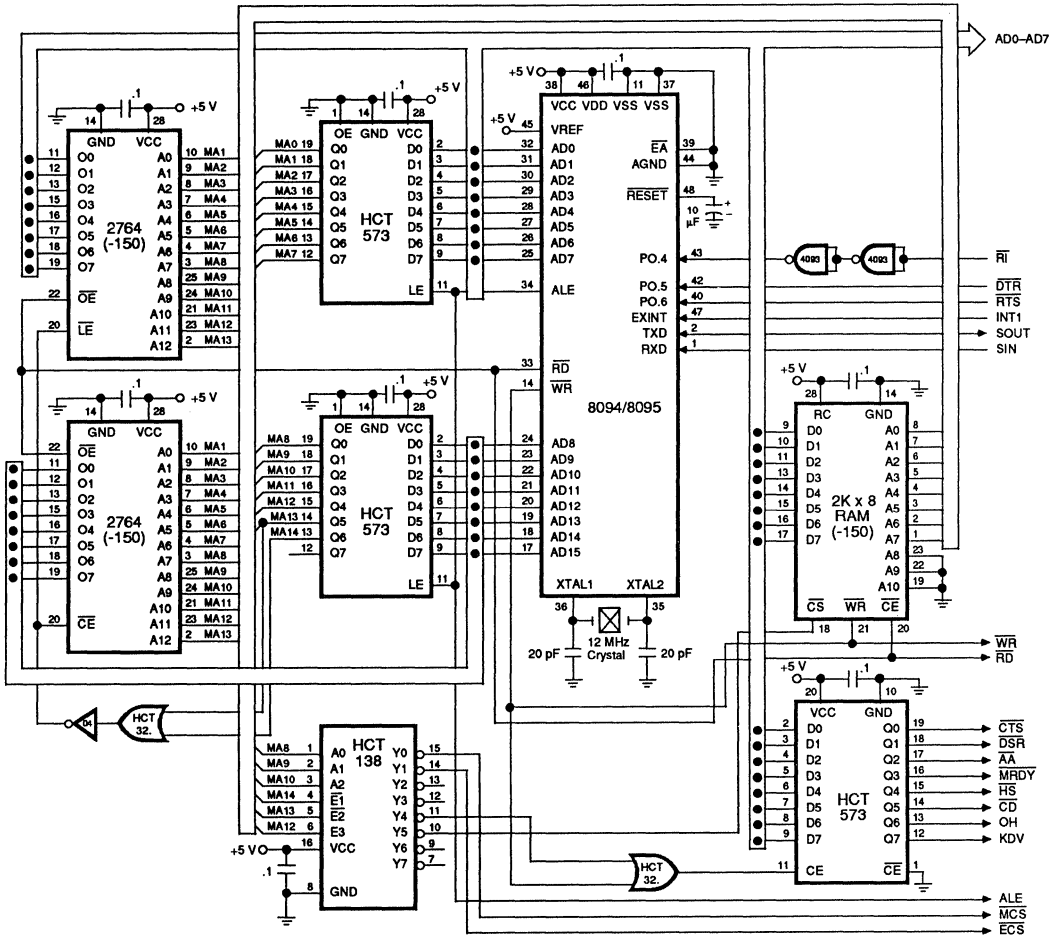


Figure 12. Control Processor Using 8095

APPLICATIONS INFORMATION (Cont.)

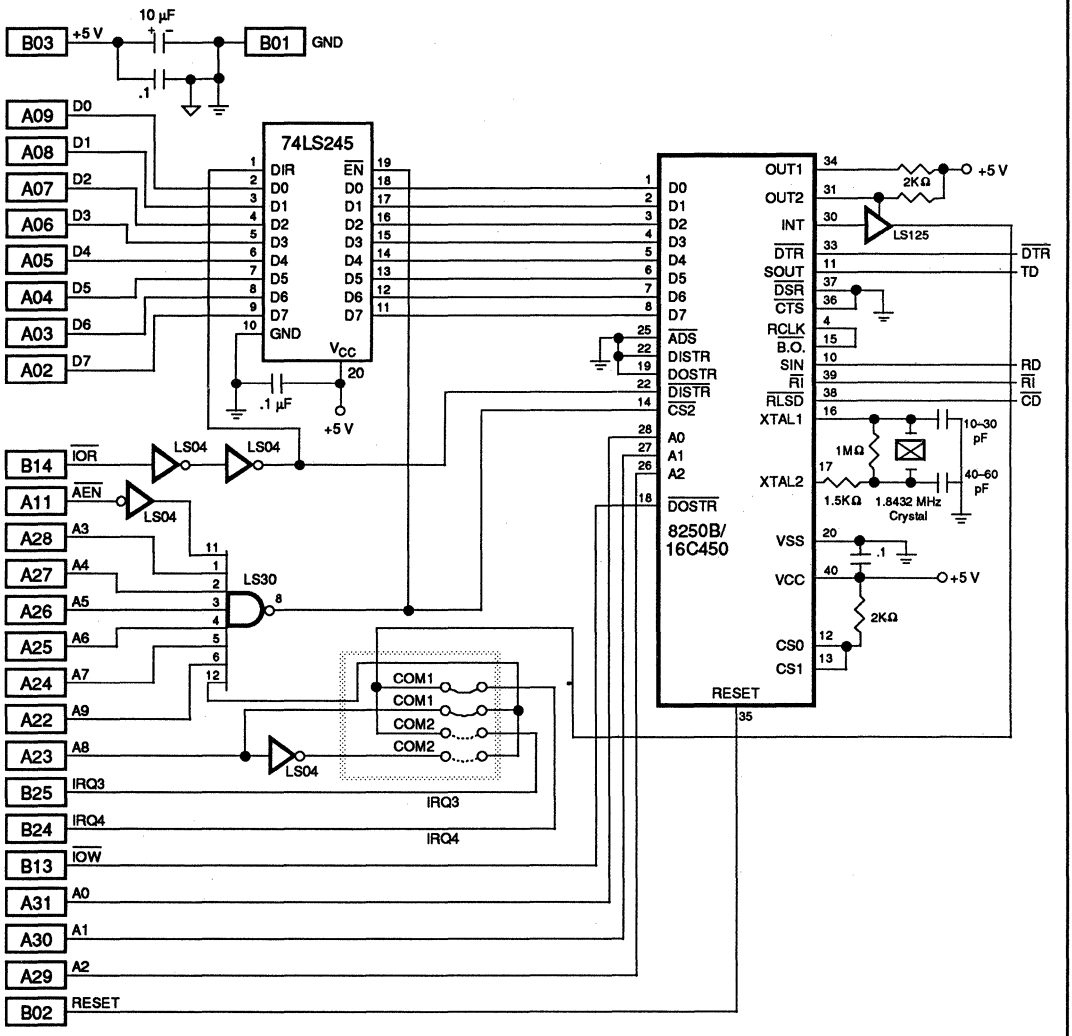
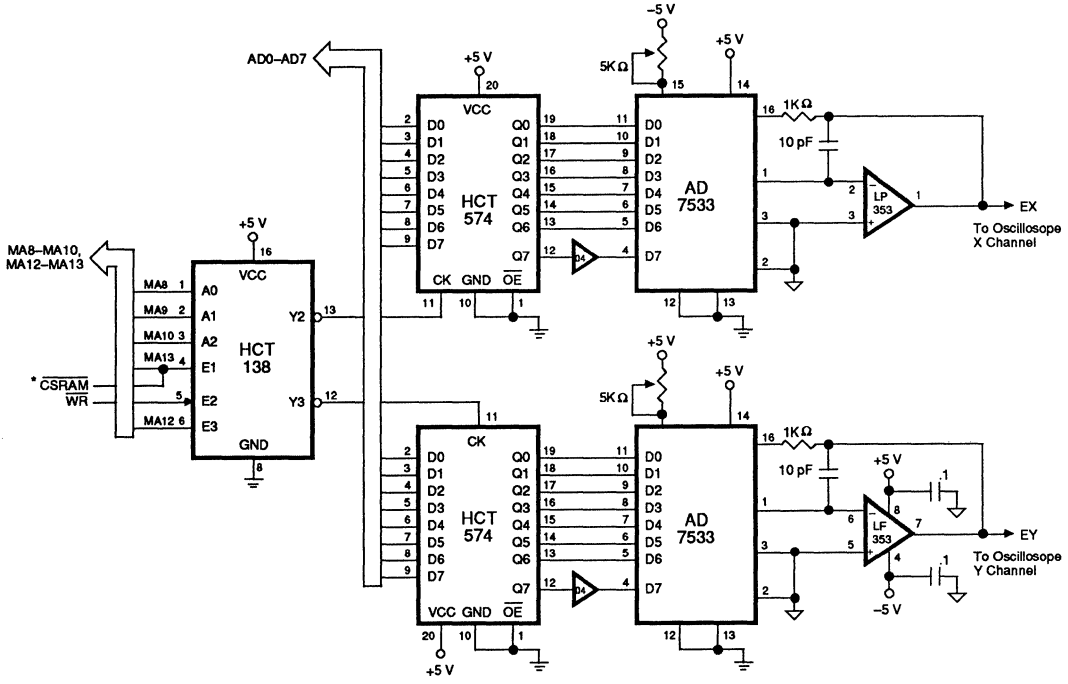


Figure 13. IBM PC/XT/AT Compatible Computer Bus Interface for 8095 Controller of Figure 12.

APPLICATIONS INFORMATION (Cont.)



*IF THE SC11019, SC11020 FAMILY IS USED, CONNECT $\overline{\text{CSRAM}}$, IF AN 8096 IS USED, CONNECT MA13.

Figure 14. Test Circuit to Generate "Eye Pattern".

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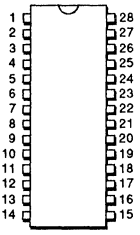
FEATURES

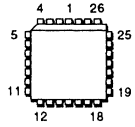
- ☐ Direct interface to SC11004 & SC11014 single chip modems
- ☐ Complete "AT" command set in firmware
- ☐ Built-in UART
- ☐ Direct IBM PC bus interface
- ☐ 28-pin DIP or PLCC package

28-PIN DIP PACKAGE



SC11007CN

28-PIN PLCC PACKAGE

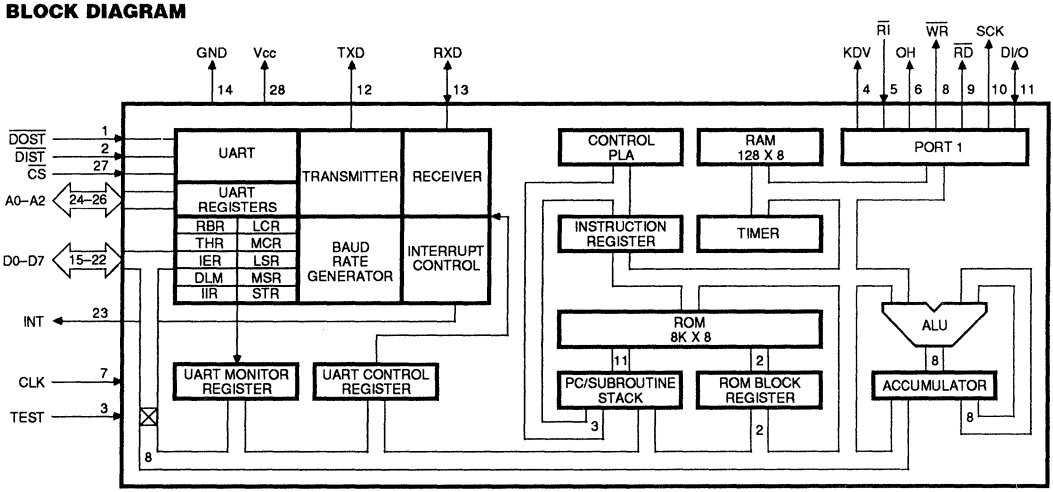


SC11007CV

GENERAL DESCRIPTION

The SC11007 Modem Interface Controller is specifically designed to control Sierra's SC11004 and SC11014 single chip, 300/1200 bit per second modems. Built with Sierra's advanced CMOS process, the SC11007 provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to the SC11004/14, with the addition of a data access arrangement (DAA), the SC11007 implements a Hayes-type smart modem for board level, integral modem applications. Because the SC11007 fully emulates the functionality of the 8250B UART with increased speed, and includes data bus transceivers, it can be directly interfaced to a computer's parallel data bus and in particular to the bus of the IBM PC, XT, or AT. All of the popular communications software written for the PC will work with the SC11004/SC11007 chip set. Besides including the functionality of the 8250B UART, the SC11007 contains an 8 bit microprocessor, 8K by 8 bytes of ROM and 128 by 8 bytes of RAM. For specific high volume applications, the control program can be modified by Sierra to include additional commands and functions.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE FOR BOTH DIP & PLCC

Figure 1.

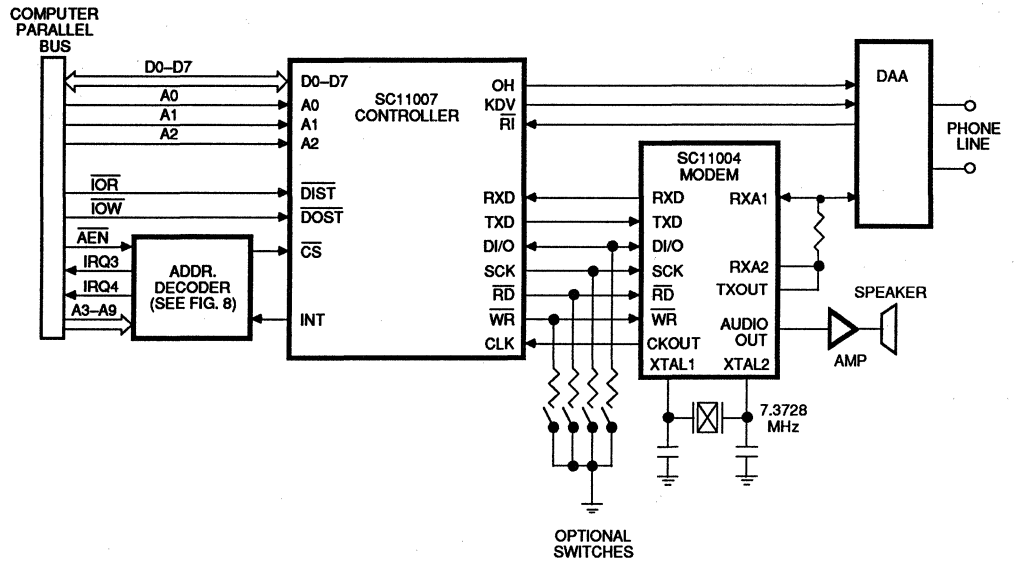


Figure 2. Integral Smart Modem Configuration for PC Bus Applications

PIN/FUNCTION DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	$\overline{DOST}$	I	The CPU can write data or control words into a selected register of the SC11007 when $\overline{DOST}$ is low and the chip is selected. Data is latched on the rising edge of the signal.
2	$\overline{DIST}$	I	The CPU can read data or status information from a selected register of the SC11007 when $\overline{DIST}$ is low and the chip is selected.
3	TEST	I	When the test input is high, the SC11007 enters a test mode—used for factory testing only. It must be connected to ground for normal operation.
4	KDV	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. During a data call, the SC11007 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
5	$\overline{RI}$	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the On duration of the ring cycle. This is a Schmidt Trigger input, allowing for slow rising and falling signals on this pin.
6	OH	0	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the SC11007 pulses this output at a rate of 10 pulses per second with appropriate mark/space ratio depending on 212A or V.22 mode.
7	CLK	I	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the SC11004/14 modem is connected to this pin. All internal timing is derived from this clock.
8	$\overline{WR}$	I/O	This pin is used to initiate writing of data to the SC11004/14 modem. On power-up, it is an input for a brief time in which the SC11007 reads the carrier status switch connected to this pin. If the switch is closed to ground thru an 18 kΩ resistor, the SC11007 sets the Received Line Signal Detect (RLSD) bit in the Modem Status Register. If the switch is open or tied to V_{CC} thru 18k, the SC11007 resets this bit and writes the actual status of the carrier detector during a data call. However, NO switch is required, since an internal pullup sets the status during power-up to the default state (pullup to V_{CC}) which is to follow the remote modem's carrier.

Pin No.	Pin Name	I/O	Description
9	$\overline{RD}$	I/O	This pin is used to initiate reading of data from the SC110104/14 modem. On power-up, this pin is an input for a brief time in which the SC11007 reads the DTR status switch connected to this pin. If this switch is open or tied to V_{CC} thru 18k, the SC11007 reacts to the status of the DTR bit in the UART Modem Control Register. If the switch is closed to ground thru 18 kΩ, the SC11007 ignores the state of the DTR bit. When the switch is open, writing a 0 to the DTR bit in the Modem Control Register forces the SC11007 into the command state and when on line, causes it to hang up. However, NO switch is required, since an internal pullup to V_{CC} sets the status during power-up to the default state — to follow the DTR status.
10	SCK	I/O	The SC11007 supplies a shift clock on this pin to the SC11004/14 modem for reading or writing data. On power-up, this pin is an input for a brief time in which the SC11007 reads the Bell/CCITT select switch connected to this pin. If this switch is open or tied to V_{CC} thru 18k, Bell protocol is selected. If this switch is closed to ground 18 kΩ, CCITT V.22 protocol is selected. However, NO switch is required, since an internal pullup sets the status during power-up to the default state—212A mode.
11	DI/O	I/O	The SC11007 shifts data serially out of this pin to SC11004/14 during a write operation and shifts data serially into this pin during a read operation from the SC11004/14. On power-up this pin is an input for a brief time in which the SC11007 reads the Make/Break ratio select switch connected to this pin for selecting the pulse dialing standard. With the switch open or tied to V_{CC} thru 18k, the Bell standard 39% Make, 61% Break is selected. With the switch closed to ground thru 18 kΩ, the CCITT standard 33% Make, 67% Break is selected. However, NO switch is required, since an internal pullup sets the status during power-up to the default state—Bell standard.
12	TXD	O	During a data call, after the connection is established, the SC11007 converts parallel data received from the computer bus and outputs it in a serial, asynchronous format to the SC11004/14 modem for modulation. At all other times the SC11007 holds this output in the Mark (high) condition.
13	RXD	I	Demodulated data from the SC11004/14 modem is received on this pin during a data call. A high level is considered Mark and a low level is a Space. The SC11007 converts the serial data into a parallel data byte and stores it in the Receiver Buffer Register (RBR). The Data Ready bit in the Line Status Register (LSR) is then set, and an appropriate interrupt indentification code is written in the Interrupt Identification Register (IIR) to signal to the computer, the reception of a new data byte.
14	GND	—	Ground reference (0 Volts).
15–22	D0–D7	I/O	This is the 8 bit data bus comprised of three state input/output lines. This bus provides bidirectional communication between the SC11007 and the CPU. Data, control words and status information are transferred via the D0–D7 data bus. Because on-chip high drive buffers are used, no external transceiver IC, such as the 74LS245, is needed between the computer bus and the SC11007.
23	INT	O	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER: Receiver Line Status Flag, Received Data Available, Transmitter Holding Register Empty and Modem Status. It is reset low upon the appropriate interrupt servicing. The INT pin is forced to a Hi-Z state when the OUT2 bit of the Modem Control Register (MCR) is low (power on state).
24–26	A0–A2	I	These three address inputs are used during read or write operation to select a UART register in the SC11007 as shown in Table 1. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2.
27	$\overline{CS}$	I	The SC11007 is selected when this input is low. When high, the SC11007 forces the Data bus lines into a high impedance state.
28	V_{CC}	—	Positive supply (+5 Volts).

SC11007 SPECIFICATIONS

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read only) (RBR)
0	0	0	0	Transmitter Holding (write only) (THR)
0	0	0	1	Interrupt Enable (IER)
X	0	1	0	Interrupt Identification (read only) (IIR)
X	0	1	1	Line Control (LCR)
X	1	0	0	Modem Control (MCR)
X	1	0	1	Line Status (LSR)
X	1	1	0	Modem Status (read only) (MSR)
X	1	1	1	Speed (STR)
1	0	0	0	Divisor Latch (LSB) (write only) (DLL)
1	0	0	1	Divisor Latch (MSB) (write only) (DLM)

Table 1. SC11007 UART Registers

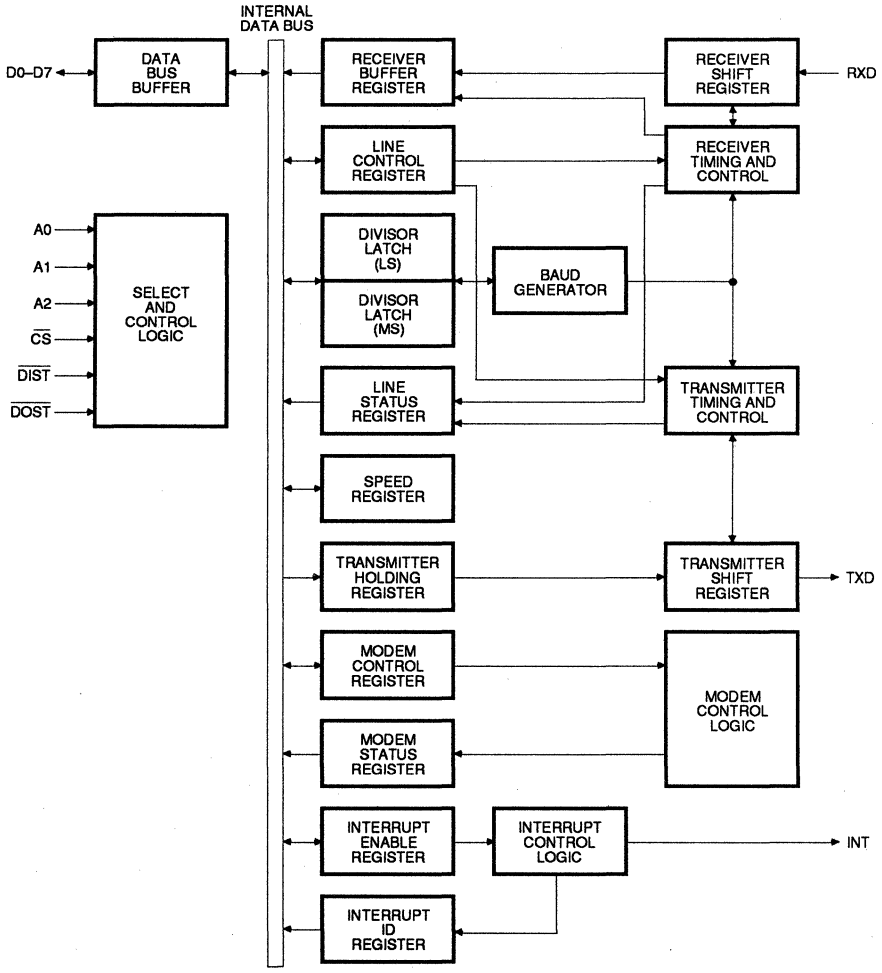


Figure 3. UART Block Diagram

Name	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
RBR	Data	Data	Data	Data	Data	Data	Data	Data
THR	Data	Data	Data	Data	Data	Data	Data	Data
IER	Receive Data Available Interrupt Enable	THRE Interrupt Enable	Receive Line Status Interrupt Enable	Modem Status Interrupt Enable	0	0	0	0
IIR	0 If Interrupt Pending	Interrupt ID Bit 0	Interrupt ID Bit 1	0	0	0	0	0
LCR	0 = 7 Bit Data 1 = 8 Bit Data	1	0 = 1 Stop Bit 1 = 2 Stop Bits	1 = Parity Enable	1 = Even Parity	1 = Stick Parity	1 = Set Break	DLAB
MCR	Data Terminal Ready	Request to Send	OUT1	OUT2 0 = INT Output to HI-Z	No Function	0	0	0
LSR	Data Ready	Overrun Error	Parity Error	Framing Error	Break Interrupt	THRE	TSRE	0
MSR	0	0	Trailing Edge Ring	Delta RLSD	1 (CTS)	1 (DSR)	Ring	RLSD
DLM	Data	Data	Data	Data	Data	Data	Data	Data
STR	Data	Data	Data	Data	Data	Data	Data	Data

Table 2. SC11007 UART Register Function Summary

Register	Range/Units	Description	Default
S0	0–255 rings	Ring to answer telephone on	0
S1	0–255 rings	Number of rings	0
S2	0–127 ASCII	Escape code character	43(+)
S3	0–127 ASCII	Character recognized as carriage return	13(CR)
S4	0–127 ASCII	Character recognized as line feed	10(LF)
S5	0–32, 127 ASCII	Character recognized as back space	8(BS)
S6	2–255 sec.	Wait time for dial tone	2
S7	1–255 sec.	Wait time for carrier	30
S8	0–255 sec.	Pause time (caused by comma)	2
S9	1–255 1/10 sec.	Carrier detect response time	6
S10	1–255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50–255 millisec.	Duration and spacing of Touch-Tones	70
S12	20–255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	—
S14	bit mapped	Option register	—
S15	bit mapped	Flag register	—
S16	0,1,2,4	Test modes	0

Table 3. SC11007 S Registers (Software Registers) Used by AT Commands

Command	Desc. (Notes 1 and 2)
Prefix, Repeat and Escape Commands	
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; + + + is not followed by carriage return)
Dialing Commands	
D	Dial
P	Pulse*
T	Touch-Tone
,	Pause
!	Flash
/	Wait for 1/8 second
@	Wait for silence
W	Wait for second dial tone
;	Return to command state after dialing
R	Reverse mode (to call originate-only modem)

Command	Desc. (Notes 1 and 2)
Other Commands	
A	Answer call without waiting for ring
B/B0	CCITT V.22 mode (Note3)
B1	Bell 103 and 212A mode*
C/C0	Transmit carrier off
C1	Carrier on*
E/E0	Characters not echoed
E1	Characters echoed*
F/F0	Half duplex
F1	Full duplex*
H/H0	On hook (hang up)
H1	Off hook, line and auxiliary relay
H2	Off hook, line relay only
I/I0	Request product ID code (130)
I1	Firmware revision number
I2	Test internal memory
L/L1	Low speaker volume
L2	Medium speaker volume*
L3	High speaker volume
M/M0	Speaker always off
M1	Speaker on until carrier detected*
M2	Speaker always on

Command	Desc. (Notes 1 and 2)
Other Commands	
O	Go to on-line state
O1	Remote digital loopback off*
O2	Remote digital loopback request
Q/Q0	Result codes displayed*
Q1	Result codes not displayed
Sr?	Requests current value of register r
Sr=n	Sets register r to value of n
V/V0	Digit result codes
V1	Word result codes*
X/X0	Compatible with Hayes-type 300 modems*
X1	Result code CONNECT 1200 enabled
X2	Enables dial tone detection
X3	Enables busy signal detection
X4	Enables dial tone and busy signal detection
Y/Y0	Long space disconnect disabled*
Y1	Long space disconnect enabled
Z	Software reset: restores all default settings

Notes: 1. Default Modes are indicated by *.
2. Commands entered with null parameters assume 0-X is the same as X0.
3. When used with the SC11014 modem IC, which has CCITT V.21 as well as V.22 modes, when the ATB command is used, in the answer mode, the SC11007 will put the SC11014 in either the V.21 mode or the V.22 mode, depending on the response from the remote modem. In the originate mode, the SC11007 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the SC11014 accordingly.

Table 4. Command Summary

Digit Code	Word Code	Description
0	OK	Command Executed
1	CONNECT	Connected at 300 or 1200 bps. Connected at 300 bps., if result of X1, X2, X3 or X4 command
2	RING	Ringing signal detected (Note 1)
3	NO CARRIER	Carrier signal not detected or lost
4	ERROR	Illegal command Error in command line Command line exceeds buffer (40 character, including punctuation) Invalid character format at 1200 bps.
5	CONNECT 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	NO DIALTONE	Dialtone not detected and subsequent commands not processed. Results from X2 or X4 commands only.
7	BUSY	Busy signal detected and subsequent commands not processed. Results from X3 or X4 commands only.
8	NO ANSWER	Silence not detected and subsequent commands not processed. Results from @ command only.

Note 1. When the SC11007 detects a ringing on the telephone line, it sends a RING result code. However, the SC11007 will answer the call only if it is in auto-answer mode or is given an A command.

Table 5. Result Codes

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	+6 V
Input Voltage	–0.6 V to V_{CC} + 0.6
Storage temperature range	–65° to +150°C.
Maximum power dissipation @ 25°C.	500 mW
Lead temperature (soldering, 10 sec)	300°C.
Operating temperature range	0° to 70°C.

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

DC ELECTRICAL CHARACTERISTICS

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Operating Current	@ V_{CC} = 5 V		10.0		mA
V_{ih}	High Level Input Voltage	all pins except $\overline{RI}$	2.0			V
V_{il}	Low Level Input Voltage	all pins except $\overline{RI}$			0.8	V
V_t+	Positive hysterisis threshold	$\overline{RI}$ pin		2.5		V
V_t-	Negative hysterisis threshold	$\overline{RI}$ pin		1.8		V
V_{oh}	High Level Output Voltage	Digital signal pins D0 to D7 & INT @ I_{oh} = 6 mA All other output or I/O pins @ I_{oh} = 2 mA	V_{CC} –1.0 V_{CC} –1.0			V V
V_{ol}	Low Level Output Voltage	Digital signal pins D0 to D7 & INT @ I_{ol} = 6 mA All other output or I/O pins @ I_{ol} = 2 mA			0.4 0.4	V V
I_l	Leakage Current (Note 2)			±1.0		µA
f_{clk}	Clock frequency		7.3721	7.3728	7.3735	MHz

Note 2. This applies to all pins except TEST, and $\overline{WR}$, $\overline{RD}$, SCK, and the DI/O pins which have internal pullups.

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{DIW}	$\overline{DIST}$ Strobe Width	1TTL Load	300		ns
t_{RC}	Read Cycle Delay	1TTL Load	300		ns
RC	Read Cycle = t_{DIW} + t_{RC} + 20 ns	1TTL Load	620		ns
t_{DDD}	Delay from $\overline{DIST}$ to Data	1TTL Load		300	ns
t_{HZ}	$\overline{DIST}$ to Floating Data Delay	1TTL Load	60		ns
t_{DOW}	$\overline{DOST}$ Strobe Width	1TTL Load	300		ns
t_{WC}	Write Cycle Delay	1TTL Load	300		ns
WC	Write Cycle = t_{DOW} + t_{WC} + 20 ns	1TTL Load	620		ns
t_{DS}	Data Setup Time	1TTL Load	60		ns
t_{DH}	Data Hold Time	1TTL Load	40		ns
t_{DIC}	$\overline{DIST}$ Delay from Select	1TTL Load	80		ns
t_{DOC}	$\overline{DOST}$ Delay from Select	1TTL Load	50		ns
t_{ACR}	Address and Chip Select Hold Time from $\overline{DIST}$	1TTL Load	10		ns
t_{ACW}	Address and Chip Select Hold Time from $\overline{DOST}$	1TTL Load	70		ns
Receiver					
t_{RINT}	Delay from $\overline{DIST}$ (Read RBR) to Reset Interrupt	100 pF Load		1	µs
Transmitter					
t_{HR}	Delay from $\overline{DOST}$ (Write THR) to Reset Interrupt	100 pF Load		1	µs
t_{IRS}	Delay from Initial INTR Reset to Transmit Start			1	Baud Cycle
t_{SI}	Delay from Initial Write to Interrupt			1	Baud Cycle
t_{SS}	Delay from Stop to Next Start			1	µs
t_{STI}	Delay from Stop to Interrupt (THRE)			1	Baud Cycle
t_{IR}	Delay from $\overline{DIST}$ (Read IIR) to Reset Interrupt (THRE)	100 pF Load		2.2	µs

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Power On Reset	All Bits Low
Interrupt Identification Register	Power On Reset	Bit 0 High; Bits 1–7 Low
Line Control Register	Writing into the LCR	Data
MODEM Control Register	Power On Reset	All Bits Low
Line Status Register	Power On Reset	Bits 0–4, 7 Low; Bits 5 and 6 High
Modem Status Register	Power Reset	Bits 0–3, 6–7 Low; Bits 4–5 High
Divisor Latch (high order bits)	Power On Reset	1200 BPS
TXD	Master Reset	High
INT	Power On Reset	Low (High-Z)

Table 6. Reset Control of Registers and Pinout Signals

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = +5V ± 10%)

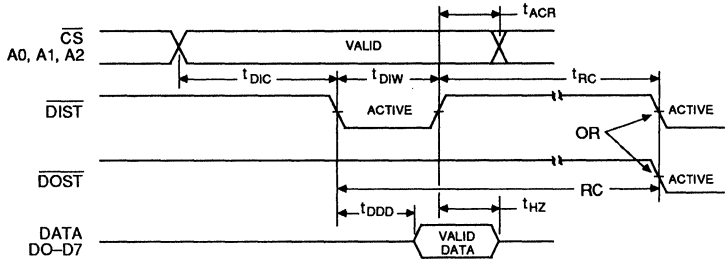


Figure 4. Read Cycle Timing

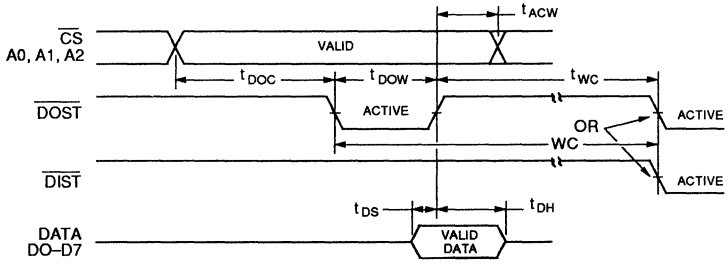


Figure 5. Write Cycle Timing

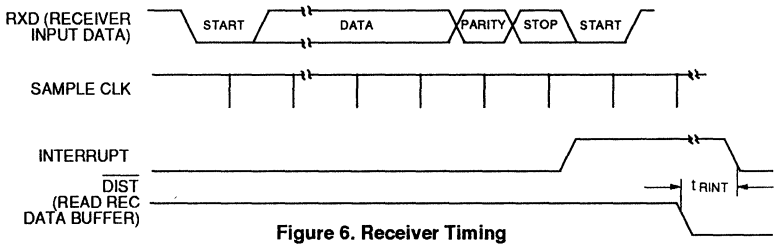


Figure 6. Receiver Timing

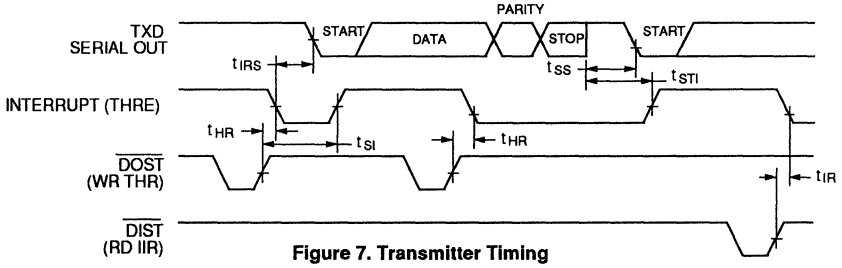


Figure 7. Transmitter Timing

UART REGISTERS

Line Control Register

This register controls the format of the asynchronous data communications.

Bits 0 and 1: Bit 1 is always high. Bit 0 specifies the number of bits in each transmitted or received serial character. The encoding of bit 0 is as follows:

Bit 1	Bit 0	Word Length
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1, when 7-bit word length with no Parity is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 0 is a logic 0 and bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed).

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is logic 1 and bit 5 is logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (TXD) is forced to the Spacing state (logic 0) and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Rate Generator

The SC11007's Baud Rate Generator can be programmed for one of six Baud rates. The desired speed is selected by writing into the Divisor Latch (DLM). On reset, the rate will be 1200 baud.

DLM (HEX Code)	Baud Rate
00	1200
01	300
03	150
04	110
06	75
09	50

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE bit is set to a logic 1 upon detection of parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time—the total time of Start bit + data bits + Parity + Stop bits.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the SC11007 is ready to accept a new character for transmission. In addition, this bit causes the SC11007 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register.

Bit 7: This bit is permanently set to logic 0.

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

UART REGISTERS

Interrupt Identification Register

The SC11007 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors. To provide minimum software overhead during data character transfers, the SC11007 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Table 7). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 7.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the SC11007 to separately activate the Interrupt (INT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Register. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Interrupt Identification Register			Interrupt Set and Reset Functions			
B2	B1	B0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Table 7: Interrupt Control Functions

MODEM Control Register

This 8-bit register controls the interface with the MODEM. The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls Data Terminal Ready (DTR) signal. If the external switch on the RD pin is set to V_{CC} thru an 18 kΩ resistor, setting the DTR low will force the SC11007 into the command state and, if on line, it will hang up.

Bit 1: This bit controls the Request to Send (RTS) signal. This signal is not used by the SC11007.

Bit 2: This bit controls the Output 1 (OUT 1) signal. This signal is not used by the SC11007.

Bit 3: This bit controls the Output 2 (OUT 2) signal. When OUT 2 is a 0, the interrupt output is in High-Z state.

Bit 4: Not used.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, two bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bit 0 and 1: These bits are always 0.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the carrier detector has changed state.

Bit 4: This bit is always 1.

Bit 5: This bit is always 1.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the Received Line Signal Detect (RLSD) signal.

Whenever bit 2 is set to logic 1, or bit 3 changes state, a MODEM Status Interrupt is generated if enabled.

APPLICATIONS

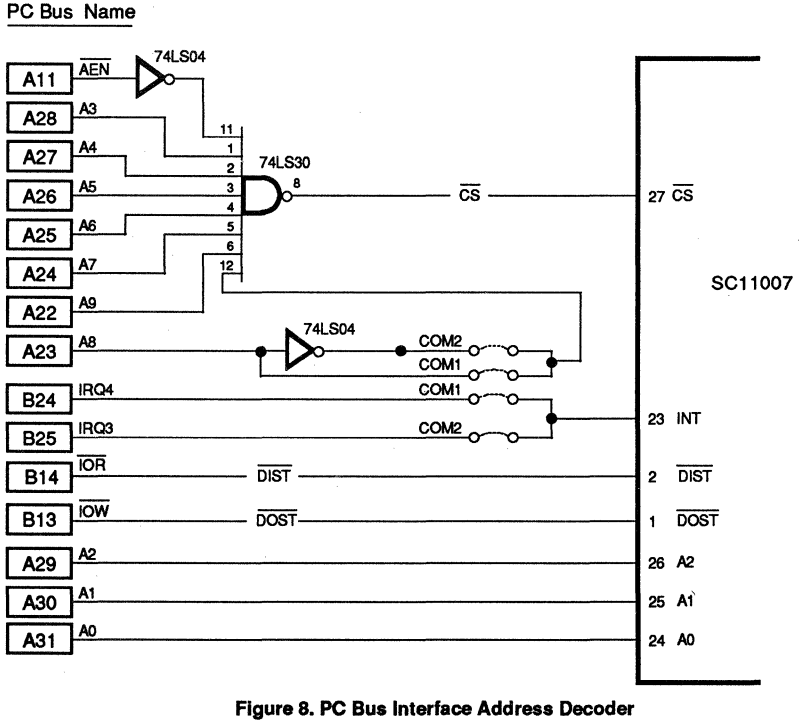
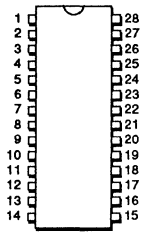


Figure 8. PC Bus Interface Address Decoder

FEATURES

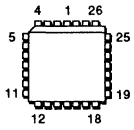
- ☐ Direct interface to SC11004, SC11014 and SC11015 single chip modems
- ☐ Built-in UART for RS-232C interface
- ☐ Complete AT command set in firmware for intelligent modems
- ☐ 28-pin DIP or PLCC package

28-PIN DIP PACKAGE



SC11008CN

28-PIN PLCC PACKAGE

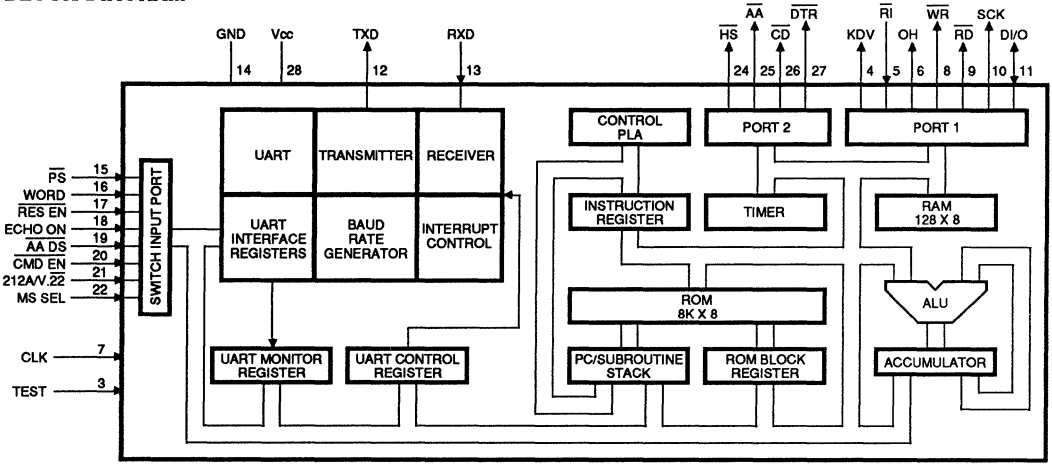


SC11008CV

GENERAL DESCRIPTION

The SC11008 Modem Interface Controller is specifically designed to control Sierra's SC11004, SC11014 and SC11015 single chip, 300/1200 bit per second modems. Built with Sierra's proprietary CMOS process, the SC11008 provides a highly cost effective solution for interfacing a modem IC to a computer's RS-232 port. When connected to the SC11004/14/15, with the addition of a data access arrangement (DAA), the SC11008 implements a Hayes-type smart modem for stand alone modem applications. All of the popular communications software written for the PC will work with the SC11004/SC11008 chip set. The SC11008 contains an 8-bit microprocessor, 8k bytes of ROM and 128 bytes of RAM and a UART. For specific high volume applications, the control program can be modified by Sierra to include additional commands and functions.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE FOR BOTH DIP & PLCC. PINS 1, 2, AND 23 ARE NOT CONNECTED.

PIN DESCRIPTIONS

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	N.C.	—	No connection
2	N.C.	—	No connection
3	TEST	I	When the test input is high, the SC11008 enters a test mode — used for factory testing only. For normal operation, this pin must be connected to ground.
4	KDV	O	This output controls the operation of the data/voice relay. The polarity of this output is selected by $\overline{PS}$ pin. If $\overline{PS}$ is connected to ground, this output is active high, i.e. it is low when the modem is on hook, causing the data/voice relay to be off and the phone line is connected to the phone set. During a data call, this output goes high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads. If $\overline{PS}$ pin is left open or connected to V_{CC}, this output is active low, i.e. it is high when the modem is on hook and low when the modem makes a data call.
5	$\overline{RI}$	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the On duration of the ring cycle. This is a Schmidt Trigger input, allowing for slow rising and falling signals on this pin.
6	OH	O	This output controls the operation of the hookswitch relay in the DAA. The polarity of this output is selected by $\overline{PS}$ pin. If $\overline{PS}$ pin is connected to ground, this output is active high, i.e. it is low when the modem is on hook. During a data call, it goes high to operate the hookswitch relay and seize the phone line. During rotary dialing, the SC11008 pulses this output at a rate of 10 pulses per second with appropriate mark/space ratio depending on 212A or V.22 mode. If $\overline{PS}$ pin is left open or connected to V_{CC}, this output is active low, i.e. it is high when the modem is on hook and low during data call.
7	CLK	I	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the SC11004/14/15 modem is connected to this pin. All internal timing is derived from this clock.
8	$\overline{WR}$	O	This pin is used to initiate writing of data to the SC11004/14/15 modem.
9	$\overline{RD}$	O	This pin is used to initiate reading of data from the SC11004/14/15 modem.
10	SCK	O	The SC11008 supplies a shift clock on this pin to the SC11004/14/15 modem for reading or writing data.
11	DI/O	I/O	The SC11008 shifts data serially out of this pin to SC11004/14/15 during a write operation and shifts data serially into this pin during a read operation from the SC11004/14/15.
12	TXD	O	The SC11008 outputs serial data in asynchronous start/stop format at the data rate selected by the terminal. This data is either echo of commands received from the terminal or result codes generated by the controller during processing of the commands. This output is normally high and should be "AND"ed with the RXD output of the SC11004/14/15 to form RXD data to the terminal.
13	RXD	I	The SC11008 receives command data from the terminal on this pin. The UART in the controller connects the serial asynchronous start/stop data into a parallel byte for processing by the controller.
14	GND	—	Ground reference (0 V)
15	$\overline{PS}$	I	This input controls the polarity of KDV and OH outputs. When left open or connected to V_{CC}, it forces the KDV and OH output to be active low. If this input is connected to ground, KDV and OH outputs are active high.

PIN NO.	PIN NAME	I/O	DESCRIPTION
16	WORD	I	When this input is open or connected to V_{CC}, the SC11008 sends result codes as words. When this input is low, result codes are sent as digits. This setting can also be changed by entering the V command.
17	$\overline{\text{RES EN}}$	I	When this input is low, the SC11008 sends result codes. When this input is high or left open, commands received from the terminal are performed but result codes are not sent. This setting can also be changed by entering the Q command.
18	ECHO EN	I	When this input is high or left open, the SC11008 echoes characters received from the terminal in the command state. When this input is low, the SC11008 won't echo characters unless it is set for half duplex and it is on line. This setting can also be charged by entering the E command.
19	$\overline{\text{AA DIS}}$	I	When this input is low, the SC11008 won't answer incoming calls. When this input is high or left open, the SC11008 automatically answers incoming calls on the first ring. This function can also be enabled/disabled by writing to the S0 register.
20	$\overline{\text{CMD EN}}$	I	When this input is low, the SC11008 recognizes commands sent to it. For some applications such as unattended answering operation it is better to disable this function by leaving this input open or connecting it to V_{CC}.
21	212A/$\overline{\text{V.22}}$	I	When this input is open or connected to V_{CC}, the SC11008 supports Bell 103 and 212A modes. When this input is low, the SC11008 supports the CCITT V.22 and V.21 modes. This setting can also be charged by entering the B command.
22	MS SEL	I	When this input is open or connected to V_{CC}, the Mark/Space ratio is U.S. standard, 40/60 Make/Break. When it is low, the Mark/Space ratio is European standard, 33/67 Make/Break.
23	N.C.	—	No connection
24	$\overline{\text{HS}}$	O	This output, when low, indicates that the modem is in the high speed (1200 bps) mode. When high, it indicates that it is in the low speed (300 bps) mode. This output can be directly connected to a light emitting diode thru a 330 Ω resistor.
25	$\overline{\text{AA}}$	O	This output is low when the SC11008 is set for auto-answer mode, either by switch input $\overline{\text{AA DIS}}$ (pin 19) or register S0. The output goes high during each ring. If the device is not set to answer the phone (pin 19 is low or S0 = 0), this output goes low each time the phone rings. A light emitting diode thru a 330 Ω resistor can be directly connected to this output.
26	$\overline{\text{CD}}$	O	This output goes low when the SC11008 detects a carrier signal from the remote modem. If the connection is broken or never established, it remains high. A light emitting diode can be directly connected to this output thru a 330 Ω resistor.
27	$\overline{\text{DTR}}$	I	When this input is low, the SC11008 executes data call commands. If during a data call, this input goes high, the SC11008 terminates the data call, hangs up the phone line and returns to command state.
28	V_{CC}	—	Positive supply (+5 V)

Register	Range/Units	Description	Default
S0	0–255 rings	Ring to answer telephone on	0
S1	0–255 rings	Number of rings	0
S2	0–127 ASCII	Escape code character	43(+)
S3	0–127 ASCII	Character recognized as carriage return	13(CR)
S4	0–127 ASCII	Character recognized as line feed	10(LF)
S5	0–32, 127 ASCII	Character recognized as back space	8(BS)
S6	2–255 sec.	Wait time for dial tone	2
S7	1–255 sec.	Wait time for carrier	30
S8	0–255 sec.	Pause time (caused by comma)	2
S9	1–255 1/10 sec.	Carrier detect response time	6
S10	1–255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50–255 millisec.	Duration and spacing of Touch-Tones	70
S12	20–255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	—
S14	bit mapped	Option register	—
S15	bit mapped	Flag register	—
S16	0,1,2,4	Test modes	0

Table 1. SC11008 S Registers (Software Registers) Used by AT Commands

Command	Desc. (Notes 1 and 2)
Prefix, Repeat and Escape Commands	
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; + + + is not followed by carriage return)
Dialing Commands	
D	Dial
P	Pulse*
T	Touch-Tone
,	Pause
!	Flash
/	Wait for 1/8 second
@	Wait for silence
W	Wait for second dial tone
;	Return to command state after dialing
R	Reverse mode (to call originate-only modem)

Command	Desc. (Notes 1 and 2)
Other Commands	
A	Answer call without waiting for ring
B/B0	CCITT V.22 mode (Note 3)
B1	Bell 103 and 212A mode*
C/C0	Transmit carrier off
C1	Carrier on*
E/E0	Characters not echoed
E1	Characters echoed*
F/F0	Half duplex
F1	Full duplex*
H/H0	On hook (hang up)
H1	Off hook, line and auxiliary relay
H2	Off hook, line relay only
I/I0	Request product ID code (130)
I1	Firmware revision number
I2	Test internal memory
L/L1	Low speaker volume
L2	Medium speaker volume*
L3	High speaker volume
M/M0	Speaker always off
M1	Speaker on until carrier detected*
M2	Speaker always on

Command	Desc. (Notes 1 and 2)
Other Commands	
O	Go to on-line state
O1	Remote digital loopback off*
O2	Remote digital loopback request
Q/Q0	Result codes displayed*
Q1	Result codes not displayed
Sr?	Requests current value of register r
Sr=n	Sets register r to value of n
V/V0	Digit result codes
V1	Word result codes*
X/X0	Compatible with Hayes-type 300 modems*
X1	Result code CONNECT 1200 enabled
X2	Enables dial tone detection
X3	Enables busy signal detection
X4	Enables dial tone and busy signal detection
Y/Y0	Long space disconnect disabled*
Y1	Long space disconnect enabled
Z	Software reset: restores all default settings

Notes: 1. Default Modes are indicated by *.
2. Commands entered with null parameters assume 0-X is the same as X0.
3. When used with the SC11014 or SC11015 modem IC, which has CCITT V.21 as well as V.22 modes, when the ATB command is used, in the answer mode, the SC11008 will put the SC11014 or SC11015 in either the V.21 mode or the V.22 mode, depending on the response from the remote modem. In the originate mode, the SC11008 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the SC11014 or SC11015 accordingly.

Table 2. Command Summary

Digit Code	Word Code	Description
0	OK	Command Executed
1	CONNECT	Connected at 300 or 1200 bps. Connected at 300 bps., if result of X1, X2, X3 or X4 command
2	RING	Ringing signal detected (Note 1)
3	NO CARRIER	Carrier signal not detected or lost
4	ERROR	Illegal command Error in command line Command line exceeds buffer (40 character, including punctuation) Invalid character format at 1200 bps.
5	CONNECT 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	NO DIALTONE	Dialtone not detected and subsequent commands not processed. Results from X2 or X4 commands only.
7	BUSY	Busy signal detected and subsequent commands not processed. Results from X3 or X4 commands only.
8	NO ANSWER	Silence not detected and subsequent commands not processed. Results from @ command only.

Note 1. When the SC11008 detects a ringing on the telephone line, it sends a RING result code. However, the SC11008 will answer the call only if it is in auto-answer mode or is given an A command.

Table 3. Result Codes

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	+ 6 V
Input Voltage	-0.6V to V_{CC}+0.6
Storage temperature range	–65 to +150°C.
Maximum power dissipation @ 25°C.	500mW
Lead temperature (soldering, 10 sec)	300°C.
Operating temperature range	0 to 70°C.

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

DC ELECTRICAL CHARACTERISTICS

Param.	Description	Conditions	Min	Typ	Max	Units
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Operating Current	@ V_{CC} = 5 V, outputs unloaded		10.0		mA
V_{ih}	High Level Input Voltage	all pins except $\overline{RI}$	2.0			V
V_{il}	Low Level Input Voltage	all pins except $\overline{RI}$			0.8	V
V_t+	Positive hysterisis threshold	$\overline{RI}$ pin		2.5		V
V_t–	Negative hysterisis threshold	$\overline{RI}$ pin		1.8		V
V_{oh}	High Level Output Voltage	@ I_{oh} = 2 mA	V_{CC} –1.0			V
V_{ol}	Low Level Output Voltage	@ I_{oh} = 2 mA			0.4	V
I_l	Leakage Current (Note 2)			±1.0		uA
f_{clk}	Clock frequency		7.3721	7.3728	7.3735	MHz

Note 2. This applies to all pins except TEST, $\overline{WR}$, $\overline{RD}$, SCK, DI/O and switch pins 15–21 which have internal pullups.

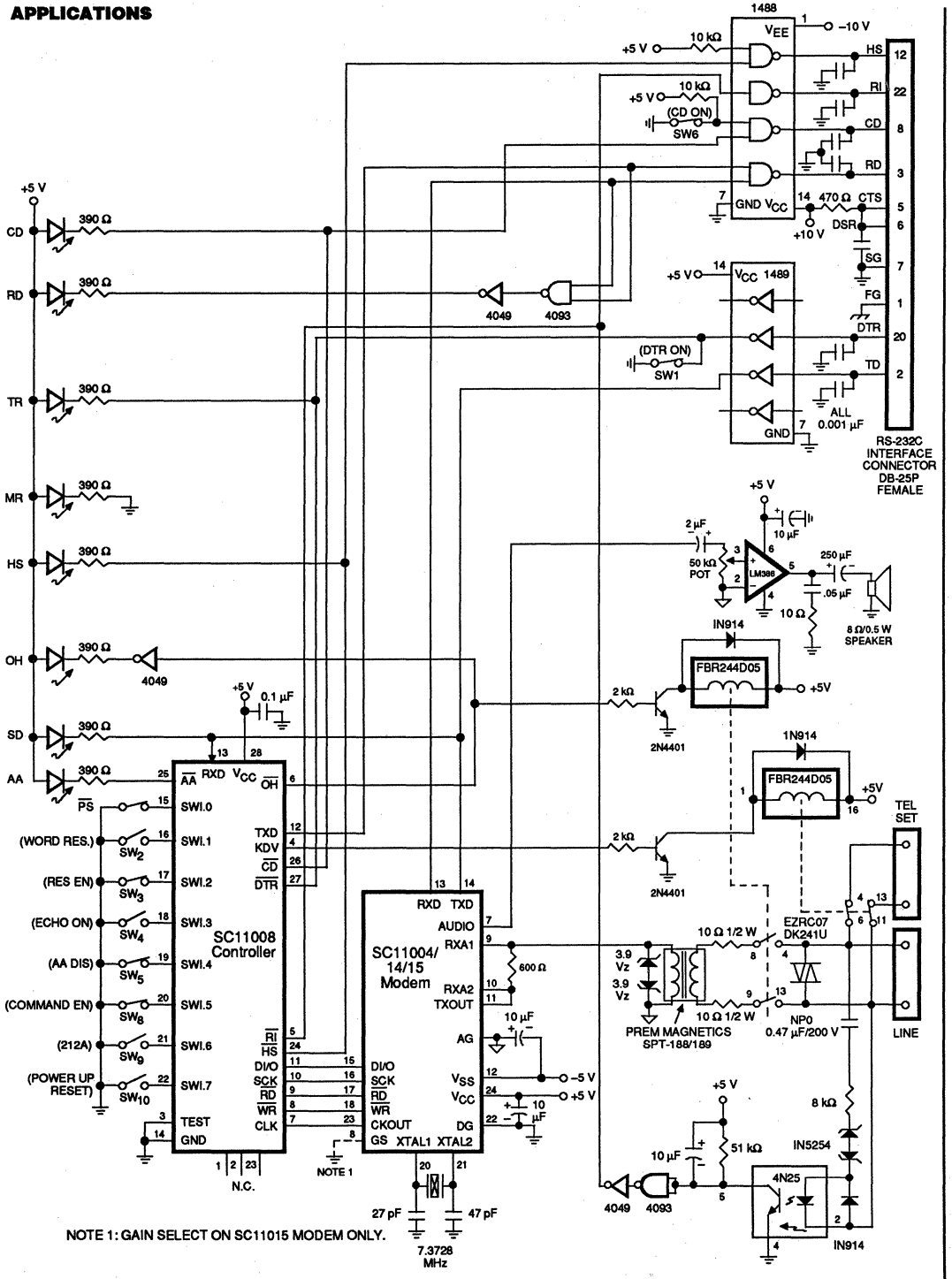
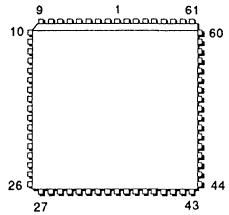


Figure 1. 212A/V.22 Stand-Alone Intelligent Modem Using the SC11004/14/15 Modem IC and the SC11008 Controller

FEATURES

- ☐ V.22 bis, V.22, V.21, 212A and 103 standards
- ☐ Direct interface to SC11006/024
- ☐ Complete "AT" command set available in firmware
- ☐ Built-in UART
- ☐ Direct IBM PC bus interface
- ☐ External ROM/RAM addressable for application flexibility
- ☐ CMOS technology
- ☐ 8k x 8 Internal ROM available for custom applications

68-PIN PLCC PACKAGE



SC11011CV

GENERAL DESCRIPTION

The Modem Advanced Controller (MAC) is a specialized controller which interfaces directly to the SC11006 or SC11024 Modem Analog Processor (MAP) to implement a 2400 bps full duplex intelligent modem. The two-chip set, when combined with an external ROM containing Sierra provided firmware, performs all the modem functions and automatic control features compatible with the Hayes "AT" Command Set. The chip set meets CCITT V.22bis standards with V.22 fallback and Bell 212A standards with 103 fallback, as well as V.21 standards.

The SC11011 interfaces to a parallel system bus, such as that in the IBM PC, or by changing one bit in the ROM code it interfaces to an RS232 port. The SC11011 includes an on board 8250B compatible, industry standard UART. With the RDY output which is used to inject "wait states" into the computer, the MAC can be used to directly interface with any speed computer. The MAC has a configuration bit which switches the UART to bring out the parallel or the serial side of the UART.

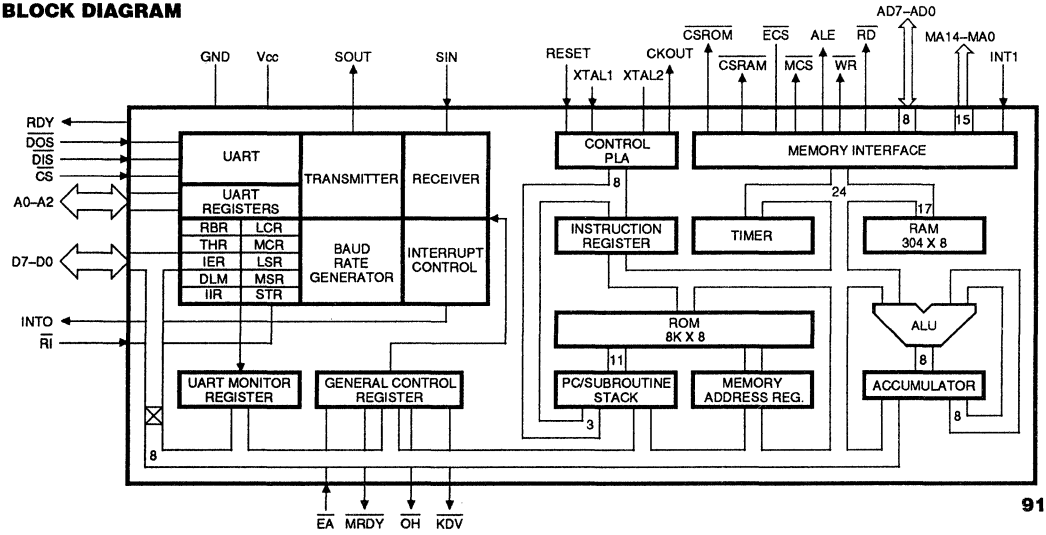
The MAC receives 8-bit signal samples from the MAP and performs adaptive equalization, carrier phase recovery, data decode, and descrambling.

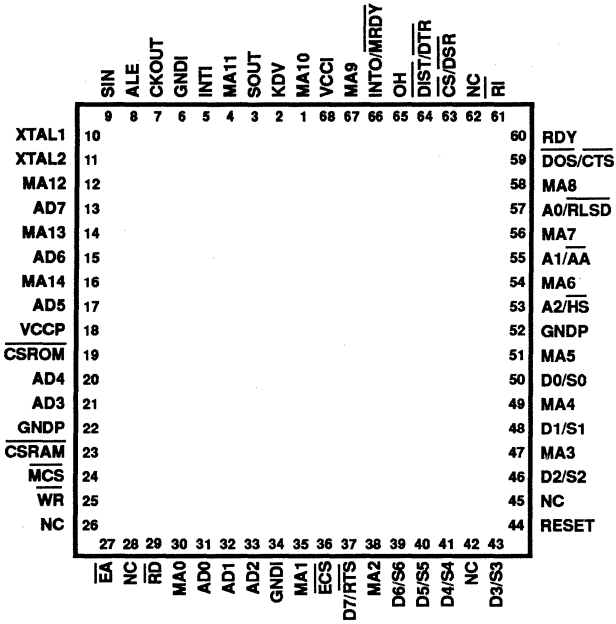
The SC11011 is for use with external memory. For fully internal ROM versions see the SC11019 series. Detailed application information is contained in SC11006, SC11024 and SC11046 data sheets.

The MAC is interrupted once every 1.667 msec (600 Hz). It reads two I channel samples and two Q channel samples (T/2 sampling) within 100 µsec of receiving the interrupt. After the samples are processed a quad-bit (4 bits) of descrambled data is written back to the MAP. The MAP performs the synchronous to asynchronous conversion function, if operating in asynchronous mode, and outputs the received data on the RXD pin.

The MAC uses a bit slice core processor to perform the digital signal processing (DSP) and the control functions. Its instruction set is a subset of the Intel 8096 instruction set but operates faster than the 8096. For instance, a signed (2's complement) 16 bit by 16 bit multiply with 32 bit result takes 3.5 µsec. (Intel 8096 takes 6.5 µsec with a 12 MHz clock.)

BLOCK DIAGRAM





Order Number:
SC11011CV, SC11013CV, SC11018CV

INTERFACE BLOCK DIAGRAMS

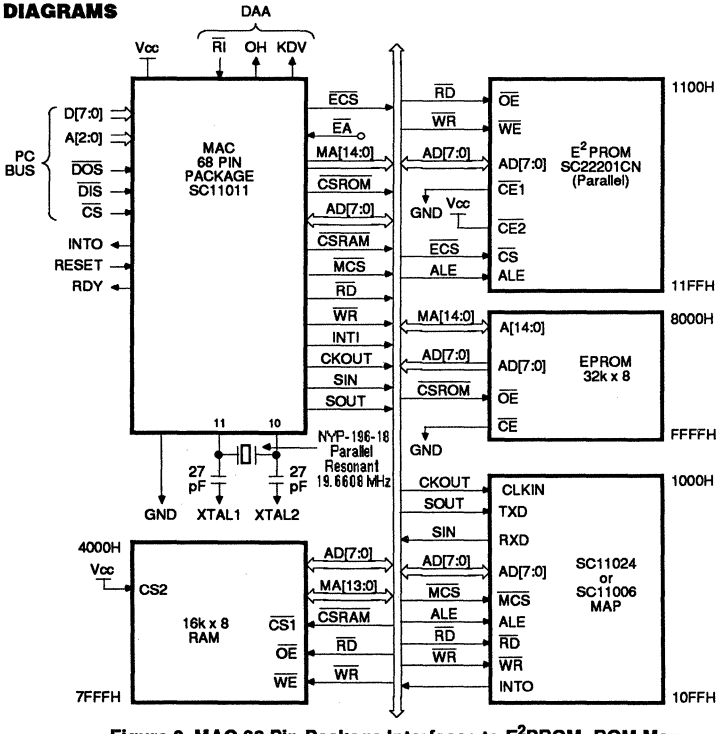


Figure 2. MAC 68 Pin Package Interfaces to E²PROM, ROM Map

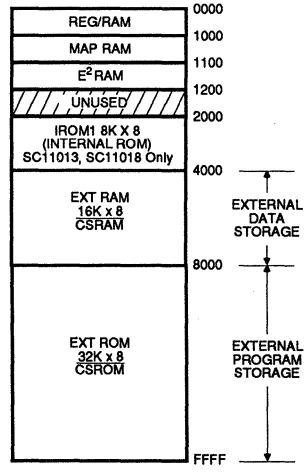


Figure 3. MAC Address Map

PIN DESCRIPTION

I Parallel System Interface (to PC Bus)

$\overline{CS}$	Chip select, active low, input, TTL.
A2–A0	Address lines for UART register select, input, TTL.
INTO	Interrupt, output, CMOS/TTL. Tristate™ *
D7–D0	8-bit data port, input-output, TTL.
$\overline{DOS}$	Data out strobe (PC writes into UART registers), active low, input, TTL.
$\overline{DIS}$	Data in strobe (PC reads from UART registers), active low, input, TTL.
RDY	Ouput, ready signal for high speed PC-AT interface.

II RS-232 (Data Set Mode) and Display Interface

$\overline{DTR}$	Data terminal ready, input, TTL.
$\overline{AA}$	Automatic answer enable (low), output, TTL/CMOS.
$\overline{HS}$	High speed indicator, output, TTL/CMOS. Low when operating at 2400 bps rate. High otherwise.
$\overline{MRDY}$	Modem ready.
$\overline{RLSD}$	Carrier detect, output, TTL/CMOS.
$\overline{DSR}$	Data set ready, output, TTL/CMOS.
$\overline{RTS}$	Request to send, input, TTL.
$\overline{CTS}$	Clear to send, output, TTL/CMOS.

III MAP Interface

AD7–AD0	8-bit bidirectional multiplexed address/data bus, CMOS.
$\overline{RD}$	RAM read, output, CMOS/TTL, normally high, data on AD7–AD0 must be valid at the rising edge of this pulse.
$\overline{WR}$	RAM write, output, CMOS/TTL, normally high, data on AD7–AD0 is valid at the rising edge of this pulse.
ALE	Address Latch Enable, output, CMOS/TTL, the address on $\overline{ECS}$, $\overline{MCS}$, AD7–AD0 are valid at the falling edge of this normally low pulse.
SOUT	Transmit data, output, CMOS/TTL. Serial data to be transmitted by the modem.
SIN	Received data, input; TTL. Serial data received from the MAP.
INTI	Interrupt input, TTL; interrupt received from the MAP at 600 Hz. Interrupt is detected when this pin has a low to high transition. The line has to stay high for at least 200 ns.
$\overline{MCS}$	Map chip select for MAP interface, output, TTL/CMOS, addressing space is from 1000H to 10FFH.
$\overline{ECS}$	External EERAM chip select or for second MAP chip select, output, TTL/CMOS, addressing space is fom 1100H to 11FFH.

IV Switch Port Pins (RS-232 Mode)

S6–S0	7-bit input port for sensing switch setting inputs. External pull-up resistors (10 kΩ) must be used on these inputs or tied to +5V if no switches used.

V DAA Interface

$\overline{RI}$	Ring indicator, input, TTL, when low, indicates the modem is receiving a ringing signal.
OH	Off-hook, output, TTL/CMOS, when high, indicates the DAA should go off-hook.
KDV	Data/voice Relay Control, output, TTL/CMOS. When high, indicates the voice (telephone set) relay is closed and the modem is in the voice mode.

VI External ROM/RAM Interface

MA0–MA14	Output, TTL/CMOS, 15 bit address bus for external program/data access.
$\overline{CSROM}$	Output, TTL/CMOS, chip select for external ROM, address from 8000H to DFFFH.
$\overline{CSRAM}$	Output, TTL/CMOS, chip select for external RAM, address from 4000H to 7FFFH.
$\overline{EA}$	Input, External access enable. Low will cause the chip to jump to external vector. Also when this pin is low, the chip will use external interrupt vector. These functions are controlled by internal ROM code.

VII Other Pins

RESET	Master reset Schmitt input, TTL, active high. When RESET is high, MAC program counter resets to location 2000H. It resumes counting after RESET goes low.
XTAL1	Together with XTAL2 for crystal input (19.6608 MHz).
XTAL2	Crystal output pin (19.6608 MHz).
CKOUT	Clock output pin, TTL/CMOS, from MAC (9.8304 MHz, ~100 ns. cycle time).
VCCI	+5 V
VCCP	Second Vcc pin
GNDI	Ground
GNDP	Second Gnd pin
GNDP	Third Gnd pin
GNDI	Fourth Gnd pin

Tristate is a trademark of National Semiconductor.
*INTO pin will be tristated with rev. G silicon and up.

SOFTWARE ARCHITECTURE

Operand Types

1. **Short Integers:** Short integers are 8-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –128 and +127 will set the overflow bit in the Program Status Byte (PSB). There are no alignment restrictions on short integers.

2. **Integers:** Integers are 16-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –32768 and +32767 will set the overflow bit in the PSB. The least significant byte of the integers is in the even byte address and the next most significant byte is in the next higher (odd) address. Therefore, the integers must be aligned at even byte boundaries in the address space. The address of a word is the address of its least significant byte (always an even address).

3. **Bits:** The bits within the bytes of the register file are numbered from 0 to 7 with 0 referring to the LSB. The only instructions that use bit addressing are JBC and JBS.

4. **Long Integers:** Long integers are 32-bit signed 2's complement variables. The result of a 16 x 16-bit multiply will be stored in a long integer. Only SHRL and SHLL manipulate this data type. Long integers are addressed by the address of their least significant byte in the register file. They should be aligned such that their address is evenly divisible by 4. The most significant byte of a long integer resides on "address" +3, where "address" is the long integer's address.

Operand Addressing

Three types of addressing are allowed:

1. **Immediate Addressing:** This is a direct field within the instruction. For short integers, this is an 8-bit field, whereas, for the integers this is a 16-bit field. Only one operand within an instruction can be immediate reference type. This operand must always be the last (right most) operand within an instruction.

   e.g. ADD AX, #340H is allowed

   ADD AX, #340H, BX is NOT allowed

2. **Register Direct Addressing:** In this mode an 8-bit field is used to access a register from the 320 byte register file. The regiter address must conform to the alignment rules.

   e.g. ADD AX, BX :AX, BX must be "even" numbers

   ADDB AX, BX :AX, BX can be "odd" or "even"

3. **Indirect Addressing:** A memory location can be addressed indirectly by placing its 16-bit address in the register file. Only one operand (the right most operand) within an instruction can be indirect.

   e.g. ADDB AL, BL, [CX] is allowed

   ADDB AL, [CX], BL is NOT allowed

Program Status Byte (PSB), location 0192H

This is an 8-bit register storing the condition flags of arithmetic, shift, and compare instructions (see the following table). The programmer can access these bits by using address 0192H.

Program Status Byte (PSB) Location 0192H

BIT	NAME	FUNCTION
7	Unused	N/A
6	Unused	N/A
5	IP	Global interrupt pending bit. Set upon receipt of interrupt. Cleared when interrupt service begins.
4	IE	Global interrupt enable bit; when zero, all interrupts are disabled.
3	Z	Zero bit; indicates the last arithmetic or compare instruction produced a zero result.
2	N	Negative bit; indicates the last arithmetic or compare instruction produced a negative result.
1	C	Carry bit; indicates the state of the arithmetic carry from the most significant bit of the ALU for an arithmetic operation or the state of the last bit shifted out of the operand for a shift. Arithmetic "Borrow" after a subtract is the complement of the C flag (i.e. if borrow generated then C = 0).
0	V	Overflow bit; indicates the last arithmetic operation produced an overflow.

SOFTWARE ARCHITECTURE (Cont.)

Interrupt Structure

Four interrupt sources exist in the MAC, namely the external interrupt, timer interrupt, ring leading edge interrupt, and UART interrupt. The interupt service routine address is 2004H.

1) External interrupt: A low to high transition on the INTI pin initiates this interrupt.

2) Timer interrupt: Timer overflow interrupt—4.8 kHz frequency.

3) Ring leading edge: Interrupt generated by leading edge of ring input.

4) UART interrupt: Interrupt from UART.

   a) Parallel version: From UMR register. Any one of the following can generate this interrupt.

      RBR was read by external processor

      Data was transferred from THR to TSR

      LCR was changed

      MCR was changed

      DLL or DLM was changed

   b) Serial version: In this configuration the interrupt signal from 8250B compatible UART is brought in as an interrupt source to the internal CPU.

INTERRUPT CONTROL REGISTER (ICR), location 0193H

This is an 8 bit register to enable or disable each of the four interrupt sources and to record the interrupt sources. The upper four bits are read/write registers while the lower four bits are read only registers. A read operation to the register will automatically clear the lower four bits.

BIT0: "1" indicates UART requested an interrupt.

BIT1: "1" indicates RING leading edge requested an interrupt.

BIT2: "1" indicates TIMER overflow requested an interrupt.

BIT3: "1" indicates EXTERNAL source requested an interrupt.

BIT4: "1" to enable UART interrupt.

BIT5: "1" to enable RING leading edge interrupt.

BIT6: "1" to enable TIMER overflow interrupt.

BIT7: "1" to enable EXTERNAL interrupt.

Any one of these four interrupts will drive the processor to address 2004H. From there the software can check interrupt sources and do priority control to branch to different service routines.

INSTRUCTION SET

The MAC instruction set is a subset of Intel 8096 instruction set. The object codes, formats and the flags they effect are identical to those of 8096. The differences are:

- No VT or ST flags exist in the MAC.
- Register locations in the UART section can only be accessed by using indirect addressing.
- The operands refer to one or more bytes of the register file. ROM locations can only be addressed using indirect addressing.
- If a memory location is addressed between 1000H and 11FFH, an external six clock multiplexed bus operation is initiated. The multiplexed address/data will use AD7–AD0 bus.
- When using ST or STB operations, the destinations are always considered to be indirect addresses.

  e.g. ST, AX, [BX] is allowed

  ST, AX, BX is NOT allowed

INSTRUCTION SET (Cont.)

Instruction Set Table

MNEMONIC	NO. OF OPERANDS	OPERATION	BYTES[1]	TIME[2]
ADD/ADDB	2	B ← A + B	3	10
ADD/ADDB	3	D ← A + B	4	10
AND/ANDB	2	B ← A AND B	3	10
AND/ANDB	3	D ← A AND B	4	10
CMP/CMPB	2	D – A	3	10
DJNZ	1	Decrement & JNZ	3	9/12
EXTB	1	Sign Extend Byte	2	7
JBC	0	Jump if bit clear	3	10/13
JBS	0	Jump if bit set	3	10/13
JC	0	Jump if Carry Set	2	5/8
JNC	0	Jump if no carry	2	5/8
JE	0	Jump if =	2	5/8
JNE	0	Jump if not =	2	5/8
JGT	0	Jump if >	2	5/8
JGE	0	Jump if >=	2	5/8
JLE	0	Jump if < or =	2	5/8
JLT	0	Jump if <	2	5/8
JV	0	Jump if Overflow	2	5/8
JNV	0	Jump if no overflow	2	5/8
JH	0	Jump if higher	2	5/8
JNH	0	Jump if not higher	2	5/8
LCALL	0	Long Call	3	11
LD/LDB	2	Load	3	10
MUL	3	D ← A * B	5	33
NOP	0	NO Operation	1	2
OR/ORB	2	D ← D OR A	3	10
XOR/XORB	2	D ← D XOR A	3	10
PUSHF	0	Push PSB	1	5
POPF	0	Pop PSB	1	5
RET	0	Return	1	10
SHL/SHLB	1	Shift Left	3	$11 + N^3$
SHLL	1	Shift Left Long	3	$15 + N^3$
SHR/SHRB	1	Shift Right	3	$11 + N^3$
SHRL	1	Shift Right Long	3	$15 + N^3$
SHRA	1	Arith. Right Shift	3	$10 + N^3$
SHRAL	1	Arith. Right Long	3	$15 + N^3$
SJMP	0	Short Jump	2	7
LJMP	0	Long Jump	3	9
ST/STB	2	Store to Memory	3	13[4]
SUB/SUBB	2	B ← B – A	3	10
SUB/SUBB	3	D ← B – A	4	10

[1]Add one for immediate words.

[2]Add 9 for indirect mode and 2 or 0 for immediate mode—see table. (Cycle times @ 100 ns)

[3]N is number of bit shifts.

[4]Indirect Mode.

HARDWARE ARCHITECTURE

The MAC device is organized with two buses that interconnect four main logic sections. The two buses are the internal data bus (DB) and address bus (Y). The four sections of the device are the internal processor, registers, memory, and dual port UART.

The two bus architecture was chosen to allow the MAC to execute the 8096 instruction set as fast or faster than the 8096 itself. The device is intended to run at 9.8304 MHz. A typical three operand instruction effectively executes in 10 clock cycles. The signed 16 x 16 multiply operation requires 34 clock cycles.

The internal data bus (DB) is the main bus of the device. It is an 8-bit bus that interconnects all four sections of the device. All internal data travels on DB. The Y bus is a 16-bit output only bus from the internal processor that provides addresses to the memory and register sections of the device. This bus allows memory control to be resident inside the internal processor without degrading performance.

The internal processor controls MAC operations and performs all of the required computation functions. The internal processor consists of a microcontrol PLA and a 16-bit registered arithmetic/logic unit (RALU). The microcontrol PLA accepts as input 8096 instruction opcodes and generates the control sequences necessary to implement the instructions. The RALU performs instruction execution, operand and address calculation, jump address calculation, program sequencing, and stack control. The program counter (PC) and stack pointer (SP) are contained within the RALU. The RALU is implemented with the 2901 silicon compiler.

The register section of the MAC includes RAM and the ports of the device. These locations are all treated as registers and may be accessed in register direct mode. Code can't be executed from registers. The UART registers are functionally, but not physically, part of the register section. The UART registers are accessed via indirect addressing mode only. There are 304 bytes of RAM to support DSP functions and the Hayes Smartmodem command set. The memory section of the MAC includes the program ROM and the external memory interface. The device contains 16K bytes of program ROM. The external memory interface allows the MAC to access program storage or data storage from external memory.

The UART section of the device implements the industry standard 8250 UART. In its parallel version the MAC appears as a 8250 to the user. The UART contains dual-port capability to allow the user and the internal processor access to its internal registers.

MEMORY DESCRIPTION

Internal ROM:

The 8k bytes of internal ROM are located at 2000H to 3FFFH

The ROM may be mask programmed for special applications. For example SC11013 MNP4 and SC11018 MNP5 modem controllers.

The SC11011 controller is built with the same architecture as the SC11019/20/21/22/23 so that firmware will be upward compatible.

External Read/Write:

Three different types of external memory operations are defined.

A) For address from 1000H to 11FFH:

These external operations occur through the AD bus. These operations take six clock cycles, four more than internal operations. These are mainly for MAP & EEROM interfaces, however, instructions and data can also be fetched from these memory spaces.

B) For address from 4000H to 7FFFH: 68 pin only.

These memory spaces are reserved for external DATA storage. The MAC can access external RAM through MA address bus and AD data bus. There are six clock memory cycles for each access.

C) For address from 8000H to FFFFH:

The chip fetches instructions from external program storage by MA0–MA14 and AD0–AD7. These operations are exactly the same as internal ROM fetch and they take 2 clock cycles.

Memory Address MAP

NAME	ABV	ADDRESS	R/W	SIZE (bytes)
INTERNAL RAM/REG	RAM*	0000H–013FH	R/W	304
	REG*	0180H–0193H	R/W	17 registers
EXTERNAL MAP/EERAM	MAP	1000H–10FFH	R/W	256
	EERAM	1100H–11FFH	R/W	256
INTERNAL ROM***	IROM1	2000–3FFFH	RO	8K
EXTERNAL RAM**	RAM	4000H–7FFFH	R/W	16K
EXTERNAL ROM**	ROM	8000H–FFFFH	RO	32K

* These may only be accessed as memory locations (16-bit address) in an indirect mode. For direct addressing a 9th bit (GCR [1], called Page Bit) must be set to switch from the first 256 bytes to the rest of the RAM.

** For 68 pin package only. Memory address has 15 bits (MA14–MA0); 16th bit is accessed through $\overline{\text{CSROM}}$ and $\overline{\text{CSRAM}}$.

REGISTER DESCRIPTION

This section contains a description of each of the registers in the MAC device. All of the registers of the device are 8-bits with 16-bit addresses. The registers are made up of bits that are either inputs or outputs. Input bits are read-only (RO). Output bits are read/write (R/W). The state of an output may be read back by the processor.

Test Mode:

RAM locations 00H and 100H are reserved for test mode. User access is prohibited.

Serial Mode:

In parallel mode (CONF = 0) the functions of the UART registers are exactly the same as those in 8250B UART. However in serial mode, (CONF = 1), the UART is turned around and controlled by the internal processor and it becomes a data set UART. The DTR, RTS, and OUT1 in MCR register becomes DSR, CTS, and RLSD outputs. The CTS, DSR in MSR register become RTS, DTR input status from $\overline{RTS}$, $\overline{DTR}$ pins.

Note:

In serial version to echo SIN to SOUT after RESET and then go back to normal operation.

1) Set "BI" in LCR to "1".
2) Sample RDI in UART monitor register.
3) Set CM = $\overline{RDI}$ in the same register.
4) SOUT will be the same state as $\overline{CM}$.
5) Receiver is functioning, ignoring it.
6) After finishing all echoing, reset "BI" in LCR.
7) Update DLL, DLM, and set CM = 1 for normal operation.
8) Do a SET then RESET to RTRST bit to RESET RCV and TMR. Do a READ to LSR to clear LSR.
9) The UART is ready for normal operaton.

Register Address MAP

NAME	ABV	INTERNAL[3]			EXTERNAL[6]	
		INDIRECT ADDRESS[4]	DIRECT ADDRESS[5]	R/W	ADDRESS A [2:0]	R/W
UART Registers:						
Receive Buffer[1]	RBR	80H	180H	R/W	00H	RO
Transmit Holding[1]	THR	8AH	18AH	R/W	00H	WO
Interrupt Enable[1]	IER	81H	181H	R/W	01H	R/W
Interrupt ID	IIR	82H	182H	RO	02H	RO
Line Control	LCR	83H	183H	R/W	03H	R/W
Modem Control	MCR	84H	184H	R/W	04H	R/W
Line Status	LSR	85H	185H	R/W	05H	R/W
Modem Status	MSR	86H	186H	R/W	06H	R/W
Scratch Pad (8 bit)	STR	87H	187H	R/W	07H	R/W
Divisor Latch LSB[2]	DLL	88H	188H	R/W	00H	R/W
Divisor Latch MSB[2]	DLM	89H	189H	R/W	01H	R/W
UART Monitor	UMR	8BH	18BH	R/W		
Internal Registers:						
Switch Port	SWP	8DH	18DH	RO		
General I/O Port						
Direction Register	DIR	8EH	18EH	WO		
Data Register	DAR	8FH	18FH	R/W		
General Control	GCR	90H	190H	R/W		
TIMER	TIM	91H	191H	R/W		
Processor Status Byte	PSB	92H	192H	R/W		
Interrupt Control	ICR	93H	193H	R/W		

[1] DLAB bit (LCR [7]) must be zero for external access.
[2] DLAB bit (LCR [7]) must be one for external access.
[3] Register access through MA bus.
[4] 8-bit addresses for indirect addressing only, with Page bit (GCR [1]) used.
[5] 16-bit addresses for direct addressing only.
[6] UART register access through PC parallel system bus.

ACCESSIBLE REGISTERS

The system programmer may access or control any of the UART registers summarized in Table 1 via the CPU. These registers are used to control UART operations and to transmit and receive data. Their reset functions are summarized in Table 2.

Line Control Register (LCR, location 183H)

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 1 and are described in the following.

Table 1: Summary of Accessible Registers

	Register Address										
	0(DLAB=0)	0(DLAB=0)	(DLAB=0)	2	3	4	5	6	7	(DLAB=1)	(DLAB=1)
Bit No	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Iden. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	STR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2 INT0 is High-Z when out2=0	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0, then the Parity bit is transmitted as a 0.

Table 2. Summary of Accessible Registers

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0–3) forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low, Bit 3–7 are permanently Low
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	"All Bits Low, Except Bits 5 and 6 are High"
MODEM Status Register	Master Reset	"Bits 0–3 Low, Bits 4–7— Input Signal"
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read BRR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read RBR/MR	Low

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has not effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Generator

The UART contains a programmable Baud Generator that takes an internal clock of (3/32)(XTAL1) = 1.8432 MHz and divides it by any divisor from 1 to (2^{16}–1). The output frequency of the Baud Generator is 16 x the Baud [(divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on the initial load.

Table 3 illustrates the used of the Baud Generator with a crystal frequency of 19.6608 MHz. The accuracy of the desired baud rate is dependent on the crystal accuracy. Communicaiton software writing values to the divisor latches typically expects the input to the UART to be 1.8432 MHz. They will work correctly only if the MAC input clock is maintained at 19.6608 MHz.

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Error Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.4	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
57600	2	—

Line Status Register (LSR, location 185H)

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 1 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: The bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is used for factory testing.

Interrupt Identification Register (IIR, location 182H)

The UART has on-chip interrupt capability that allows for flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification

Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts change the IIR, even though they are recorded, until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 1 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 4.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register (IER, location 181H)

The 8-bit register enables the four types of interrupts of the UART to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 1 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Modem Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 1 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Interrupt Identification Register				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receiver Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (If source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: Out1. Auxiliary user-designated bit. It is connected to MSR[6] (RI) during local loopback.

Bit 3: Out 2. Auxiliary user-designated bit. It is connect to MSR[7] (DCD) during local loopback. When Out2 = 0, INTO pin is Hi-Z.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input: the four MODEM. Status Register bits CTS, DSR, DCD and RI are disconnected internally; and the four MODEM Control Register bits DTR, RTS, OUT1 and OUT2 are internally connected to the four MODEM Status Register inputs, and the MODEM Control output pins $\overline{RLSD}$, $\overline{CTS}$, $\overline{DSR}$ are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5–7: These bits are permanently set to logic 0.

Modem Status Register (MSR, location 186H)

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU in addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 1 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Read (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent of DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: this bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Scratchpad Register (STR, location 187H)

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

MAC Operation

The MAC is interrupted once every 1.667 ms (600 Hz). It reads two I channel samples and two Q channel samples (T/2 sampling) within 100 µs of receiving the interrupt. After the samples are processed a quad-bit (4 bits) descrambled of data is written back to the MAP. The MAP will perform the synch to asynch conversion function, if operating in asynchronous mode, and outputs received data on SIN pin.

REGISTER DESCRIPTION

UART Monitor (UMR, location 18BH):

The UART Monitor register allows the processor to monitor UART operations. A read operation to the UART Monitor register will clear Bit 0 to Bit 4.

BIT	NAME	DESCRIPTION
7	RTRST	Reset receiver and transmitter. When set high both receiver and transmitter will be put into reset state.
6	CM	UART Command/Modem Output. When set HIGH the UART is placed in modem mode. At reset it is low, in command mode. This bit together with BI in LCR are used for bit by bit echoing. In serial version the user can set BI = 1 and CM = $\overline{RDI}$ to echo a bit. When CONF = 1 for normal operation set CM = 1.
5	RDI	Receive Data Input. This bit monitors the RXD input of the UART.
4	DLF	Divisor Latch Flag. This bit indicates if a new baud rate count has been written to the Divisor Latch.
3	LCF	Line Control Flag. This bit indicates if the line control register has been written.
2	TXF	Transmit Buffer Full Flag. This bit indicates if a new character is in the transmit shadow register.
1	RXF	Receive Buffer Empty Flag. This bit indicates if the last character has been read from the receive buffer.
0	MCF	Modem Control Flag. This bit indicates if the modem control register has been written.

Internal Registers:

Switch Port (SWP, location 18DH): for serial mode only

The Switch Port is a 7-bit input port used only in the serial mode of the MAC. It allows for reading of the external switches of a stand-alone modem.

BIT	NAME	DESCRIPTION
6–0	S 6–0	Switch Input. These bits monitor external switches.

REGISTER DESCRIPTION

Timer (TIM, location 191H):

The Timer includes an 11 bit counter and a timer flip-flop. It is used to aid software timing functions. The counter is not readable. It can only be reset by a write. The timer flip-flop can be read to test if it is already set.

The counter and flip-flop will be reset on a write (value is don't care). After that the counter sends out a pulse train at 4.8 kHz rate to set the timer flip-flop. The flip-flop can be cleared on a read. The Timer is constantly counting by the internal clock CP (9.8304 MHz).

BIT	NAME	DESCRIPTION
0	TFF0	Timer flip-flop bit.

General Control Register (GCR, location 0190H):

GCR contains a miscellaneous set of control and status bits.

BIT	NAME	DESCRIPTION
7	CONF	Configuration output. This bit controls the state of the MAC configuration. When HIGH, the MAC is configured with the SERIAL interface. It is configured with the PARALLEL interface after a reset.
6	OH	Off Hook Output. When set HIGH, the phone will be placed off hook.
5	KDV	KDV Output. Data/Voice Relay Control. When high, the modem is in the voice mode.
4	MRDY	Modem ready.
3	AA	Active HIGH AA indicator. When high this bit sets the $\overline{AA}$ pin low.
2	HS	Active HIGH HS indicator. When high this bit sets the $\overline{HS}$ pin low.
1	PAGE	Register Page Bit. This bit selects the active register page. When LOW, the lower 256 registers are accessed during register operations and when HIGH, the upper page is active.
0	EA	Inverted external access enable status from $\overline{EA}$ pin. When on it is high. Low indicates $\overline{EA}$ is off.

COMMAND SUMMARY

Configuration & Async/Sync Commands

General:

COMMAND	DESCRIPTION
B	BELL/CCITT Protocol
E	Command Echo
L	Speaker Volume
M	Speaker Control
Q	Quiet Command
S=	Writing to S-Register
S?	Reading S-Registers
V	Enable Short-form Result Codes
X	Enable Extended Result Code Set
&J	Telephone Jack Sel.*
&M	Async/Sync Mode Sel.

Async/Sync Commands—International:

&G	Guard Tone Sel.
&P	Make/Break Dial Pulse Ratio Sel.

Async-Only Commands:

Y	Enable Long Space Disconnect
&C	Data-Carrier-Detect (DCD) Options
&D	Data-Terminal-Ready (DTR) Options
&S	Data-Set-Ready (DSR) Options

Sync-Only Commands:

&R	Clear-to-Send (CTS)/Request-to-Send (RTS)
&X	Select Sync Transmit Clock Source

* See Figure 10 for Hardware Implementation.

Immediate Action Commands:

COMMAND	DESCRIPTION
A	Go OFF-Hook in Answer Mode
A/	Re-Execute Last Command
D	Dial Telephone Number
H	Switch Hook Control
O	Return to On-Line
Z	Fetch Configuraton Profile from Nonvolatile Memory
&F	Fetch Factory Configuration Profile
&W	Write Active Configuration Profile to Nonvolatile Memory
&Z	Store Telephone Number

Dial Modifiers:

P	Pulse Dial
T	Touch-Tone Dial
R	Originate Call in Answer Mode
W	Wait for Dial Tone B/4 Continue to Dial
,	Delay a Dial Sequence
@	Wait for Quiet Answer B/4 Continue to Dial
!	Initiate a Flash
;	Return to Command State after Dialing
S=n	Dial A Stored Number (n=0 to 3)

Self Test and Diagnostics:

I/IO	Request Prod Code
I1/I2	ROM Checksum
I3	Manufacturer's I.D.
I4	Configuration Mode (Serial or Parallel)
&T	Test Modes

These are the basic "Hayes" type commands shown here as an example.

Specific command sets contained in external ROM are separately documented. Sierra provides example source code for these commands as well as special applications including error correction, compression and facsimile operations. Please consult the nearest sales office for details.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

V_{CC} Supply Voltage	+6 V
Input Voltage	–0.6 V to V_{CC} +0.6 V
Storage Temperature Range	–65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range	0 to 70°C

DC ELECTRICAL CHARACTERISTICS: (T_A = 0 TO 70°C, V_{CC} = +5 V +10%)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I_{CC}	Nominal Operating Current @ V_{CC} = 5.5 V		50	75	mA
V_{IH}	High Level Input Voltage for TTL input pins for CMOS input pins	 2 0.8 V_{CC}			 V V
V_{IL}	Low Level Input Voltage for TTL input pins for CMOS input pins			 0.8 0.2 V_{CC}	 V V
VT+	Positive Hysteresis Threshold for RESET & /RI input pins		2.5		V
VT–	Negative Hysteresis Threshold for RESET & /RI input pins		1.8		V
V_{OH}	High Level Output Voltage for D7–D0, into @ I_{OH} = 8 mA for RDYP—open collector for other output @ I_{OH} = 2 mA	 0.7 V_{CC} +0.5			 V
V_{OL}	Low Level Output Voltage for D7–D0, into pins @ I_{OL} = 8 mA for RDYP @ I_{OL} = 8 mA for other output pins @ I_{OL} = 2 mA			 0.3 V_{CC} –0.5	 V
I_1	Leakage Current		±1	±20	µA
F_{CLK}	Crystal Clock Frequency		19.6608		MHz

TIMING DIAGRAMS

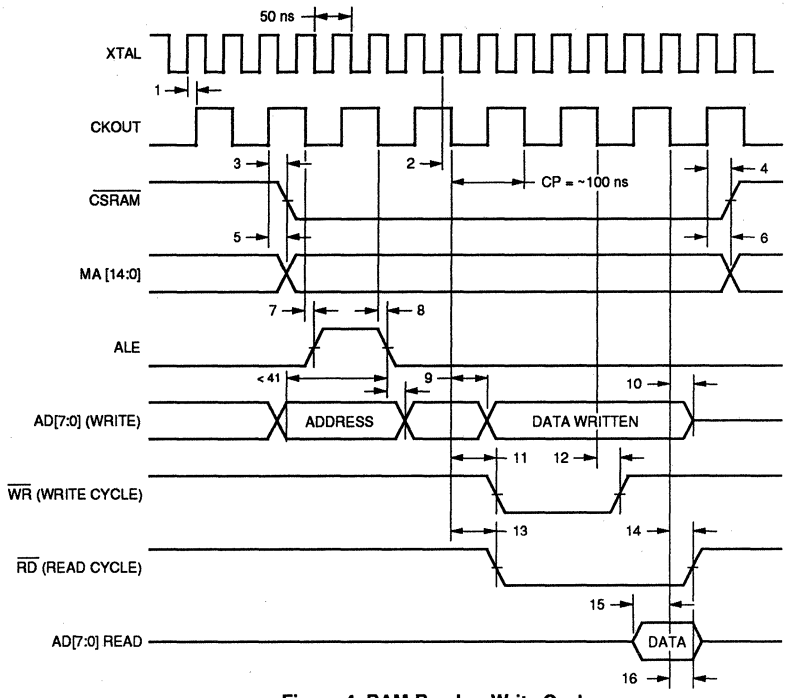


Figure 4. RAM Read or Write Cycle

RAM Read or Write Cycle Timing Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TXTHCH	XTAL high to CKOUT high				45	ns
2	TXTHCL	XTAL high to CKOUT low				45	ns
3	TCHCSL	CKOUT high to $\overline{\text{CSRAM}}$ low				25	ns
4	TCHCSH	CKOUT high to $\overline{\text{CSRAM}}$ high				25	ns
5	TCHMAV	CKOUT high to MA valid				25	ns
6	TCHMAI	CKOUT high to MA invalid				25	ns
7	TCLALH	CKOUT low to ALE high				15	ns
8	TCLALL	CKOUT low to ALE low				15	ns
9	TCLADV	CKOUT low to AD valid				35	ns
10	TCLADI	CKOUT low to AD invalid		5			ns
11	TCLWRL	CKOUT low to $\overline{\text{WR}}$ low				25	ns
12	TCLWRH	CKOUT low to $\overline{\text{WR}}$ high				25	ns
13	TCLRDL	CKOUT low to $\overline{\text{RD}}$ low				15	ns
14	TCLRDH	CKOUT low to $\overline{\text{RD}}$ high				15	ns
15	TADVCL	AD valid to CKOUT low (Read Set-up Time)		50			ns
16	TCLADI	CKOUT low to AD invalid (Read Hold Time)		0			ns

TIMING DIAGRAMS (Cont.)

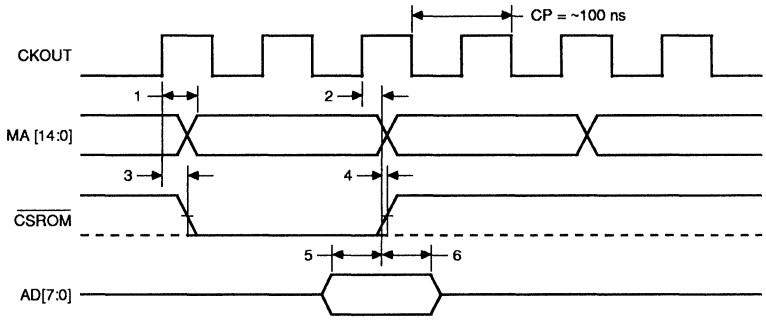


Figure 5. External Program Storage Read Bus Cycle

External Program Storage Read Bus Cycle Table

NO.	SYMBOL	PARAMETER	TEST COMMENTS	MIN	TYP	MAX	UNITS
1	TCHMAV	CKOUT high to MA valid				15	ns
2	TCHMAI	CKOUT high to MA invalid				15	ns
3	TCHCSL	CKOUT high to $\overline{\text{CSROM}}$ low	$\overline{\text{CSROM}}$ may already be low			15	ns
4	TCHCSH	CKOUT high to $\overline{\text{CSROM}}$ high	$\overline{\text{CSROM}}$ may not go high			15	ns
5	TADVCH	AD valid to CKOUT high		35			ns
6	TCHADZ	CKOUT high to AD high-Z		0			ns

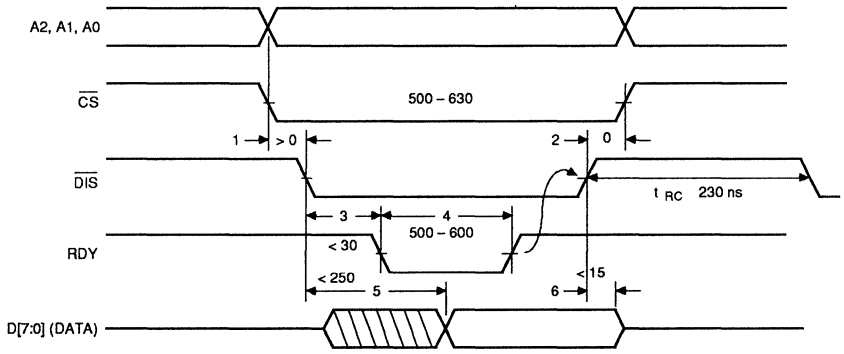


Figure 6. Read Cycle (PC Bus Read From UART Register)

Read Cycle (PC Bus Read From UART Register) Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDIL	$\overline{\text{CS}}$ low to $\overline{\text{DIS}}$ low				0	ns
2	TDIHCSH	$\overline{\text{DIS}}$ high to $\overline{\text{CS}}$ high				0	ns
3	TDILRDL	$\overline{\text{DIS}}$ low to RDY low				30	ns
4	TRDL	RDY low time (~5–6CP)		500		600	ns
5	TDILDV	$\overline{\text{DIS}}$ low to D valid				250	ns
6	TDIHDZ	$\overline{\text{DIS}}$ high to D high-Z				15	ns

TIMING DIAGRAMS (Cont.)

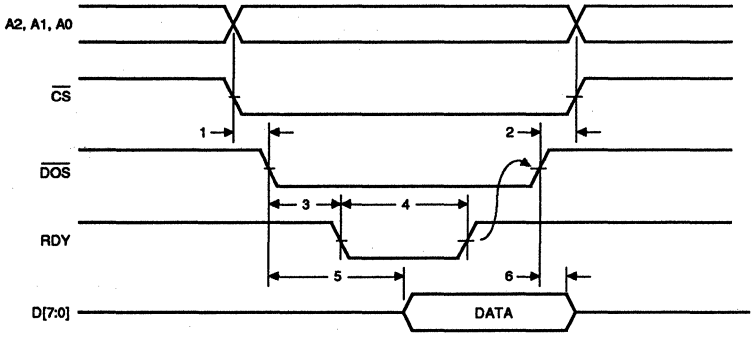


Figure 7. Write Cycle (PC Bus Write Into UART Register)

Write Cycle (PC Bus Write Into UART Register) Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDOL	$\overline{CS}$ low to $\overline{DOS}$ low				0	ns
2	TDOHCSH	$\overline{DOS}$ high to $\overline{CS}$ high				0	ns
3	TDOLRDL	$\overline{DOS}$ low to RDY low				30	ns
4	TRDL	RDY low time (~5–6CP)		500		600	ns
5	TDOLDV	$\overline{DOS}$ low to D valid				260	ns
6	TDOHDZ	$\overline{DOS}$ high to D high-Z		0			ns

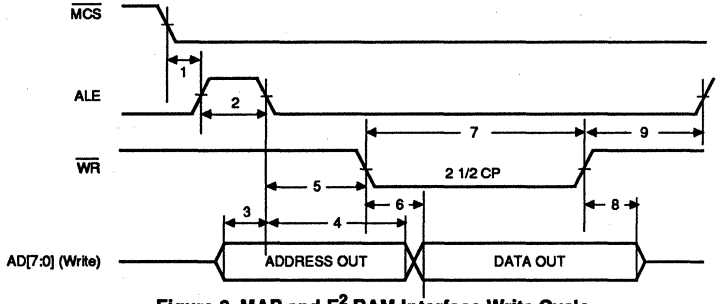


Figure 8. MAP and E^2 RAM Interface Write Cycle

MAP and E^2 RAM Interface Write Cycle Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TMCAL	$\overline{MCS}$ low to ALE high		10		20	ns
2	TALE	ALE pulse width		45			ns
3	TAVLE	Address valid to ALE low		30			ns
4	THAD	Hold address after ALE low		48			ns
5	TALRD	Delay from ALE low to $\overline{WR}$ low		45			ns
6	TDVRL	Data valid after $\overline{WR}$ low				25	ns
7	TWR	Write pulse width		230			ns
8	TDHWR	Data hold after $\overline{WR}$ high		30			ns
9	TWHLH	End of $\overline{WR}$ to next ALE		200			ns

When the SC11011 is reading or writing to the MAP, the address is valid at least 30 ns before ALE goes low and stays valid 48 ns or more beyond the trailing edge of ALE. When writing, data id valid within 25 sn afte WRn goes true and stays valid i=until at least 30 ns after WRn goes false

TIMING DIAGRAMS (Cont.)

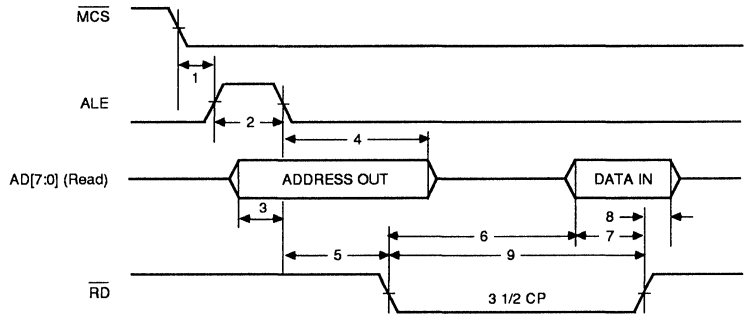


Figure 9. MAP and E²RAM Interface Read Cycle

MAP and E²RAM Interface Read Cycle Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TMCAL	$\overline{MCS}$ low to ALE high		10		20	ns
2	TALE	ALE pulse width		45			ns
3	TAVLE	Address valid to ALE low		30			ns
4	THAD	Hold address after ALE low		48			ns
5	TALRD	Delay from ALE low to $\overline{RD}/\overline{WR}$ low		45			ns
6	TDVRL	Data valid after RD low				300	ns
7	TDVRH	Data valid setup to $\overline{RD}$ high		15			ns
8	TDH	Data hold after $\overline{RD}$ high		0			ns
9	TRD	Read pulse width		330		370	ns

When reading from the MAP, data must be valid a maximum of 300ns after $\overline{RD}$ goes true and stays valid at least until 0ns after $\overline{RD}$ goes false.

CIRCUIT DIAGRAMS

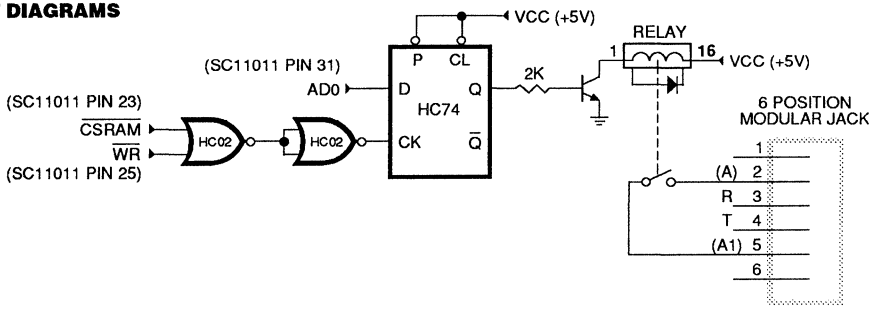


Figure 10. Circuit for Implementing & J1 Command

THE MAC AND INTEL 8096 SPEED COMPARISON

The attached is an instruction execution time comparison for the MAC and Intel 8096. The biggest improvement over 8096 is the 16 bit multiplication, it is 3.3 µs versus 6.5 µs. The jump instructions are twice as fast. The shift instructions are also about twice faster. The other arithmetic and logic instructions are about the same speed. Indirect addressing instructions in the MAC is about 20% slower than in the 8096.

The following comparison is for the 8096 with 12 MHz crystal and the MAC with 19.6608 MHz. The time unit is "µs". The instructions and operands are all from internal storage. Both the MAC and Intel 8096 will run slower for external storage access.

		DIRECT		IMMEDIATE		INDIRECT	
INSTRUCTION	OPERANDS	MAC	8096	MAC	8096	MAC	8096
ADD	2	1.02	1.00	1.22	1.25	1.94	1.50
ADD	3	1.02	1.25	1.22	1.50	1.94	1.75
ADDB	2	1.02	1.00	1.02	1.00	1.94	1.50
ADDB	3	1.02	1.25	1.02	1.25	1.94	1.75
AND	2	1.02	0.75	1.22	1.25	1.94	1.50
AND	3	1.02	1.00	1.22	1.50	1.94	1.75
ANDB	2	1.02	1.00	1.02	1.00	1.94	1.50
ANDB	3	1.02	1.25	1.02	1.25	1.94	1.75
CMP	2	1.02	1.00	1.22	1.25	1.94	1.50
CMPB	2	1.02	1.00	1.02	1.00	1.94	1.50
DJNZ		0.92/1.25	1.25/2.25	(NO JUMP/JUMP)			
EXTB		0.71	1.00				
JBC		1.02/1.32	1.25/2.25				
JBS		1.02/1.32	1.25/2.25				
JC		0.51/0.82	1.00/2.00				
JE		0.51/0.82	1.00/2.00				
JGE		0.51/0.82	1.00/2.00				
JGT		0.51/0.82	1.00/2.00				
JH		0.51/0.82	1.00/2.00				
JLE		0.51/0.82	1.00/2.00				
JLT		0.51/0.82	1.00/2.00				
JNC		0.51/0.82	1.00/2.00				
JNE		0.51/0.82	1.00/2.00				
JNH		0.51/0.82	1.00/2.00				
JNV		0.51/0.82	1.00/2.00				
JV		0.51/0.82	1.00/2.00				
LCALL		1.12	3.25				
LD	2	1.02	1.00	1.22	1.25	1.94	1.50
LDB	2	1.02	1.00	1.02	1.00	1.94	1.50
LJMP	1	0.92	2.00	1.02	1.00	1.94	1.50
MUL	3	3.36	6.50	(BIGGEST IMPROVEMENT)			
NOP		0.24	1.00				
OR	2	1.02	1.00	1.22	1.25	1.94	1.50
ORB	2	1.02	1.00	1.02	1.00	1.94	1.50
PUSHF		0.51	2.00				
POPF		0.51	2.25				
RET		1.02	3.00				
SHL		1.12+0.10N	1.75+0.25N	(N = SHIFT COUNT)			
SHLB		1.12+0.10N	1.75+0.25N				
SHLL		1.53+0.10N	1.75+0.25N				
SHR		1.12+0.10N	1.75+0.25N				
SHRB		1.12+0.10N	1.75+0.25N				
SHRL		1.53+0.10N	1.75+0.25N				
SHRA		1.02+0.10N	1.75+0.25N				
SHRAL		1.53+0.10N	1.75+0.25N				
SJMP		0.71	2.00				
ST		1.32	1.75				
STB		1.32	1.75				
SUB	2	1.02	1.00	1.22	1.25	1.94	1.50
SUBB	2	1.02	1.00	1.02	1.00	1.94	1.50
SUB	3	1.02	1.25	1.22	1.50	1.94	1.75
SUBB	3	1.02	1.25	1.02	1.25	1.94	1.75
XOR	2	1.02	1.00	1.22	1.25	1.94	1.50
XORB	2	1.02	1.00	1.02	1.00	1.94	1.50

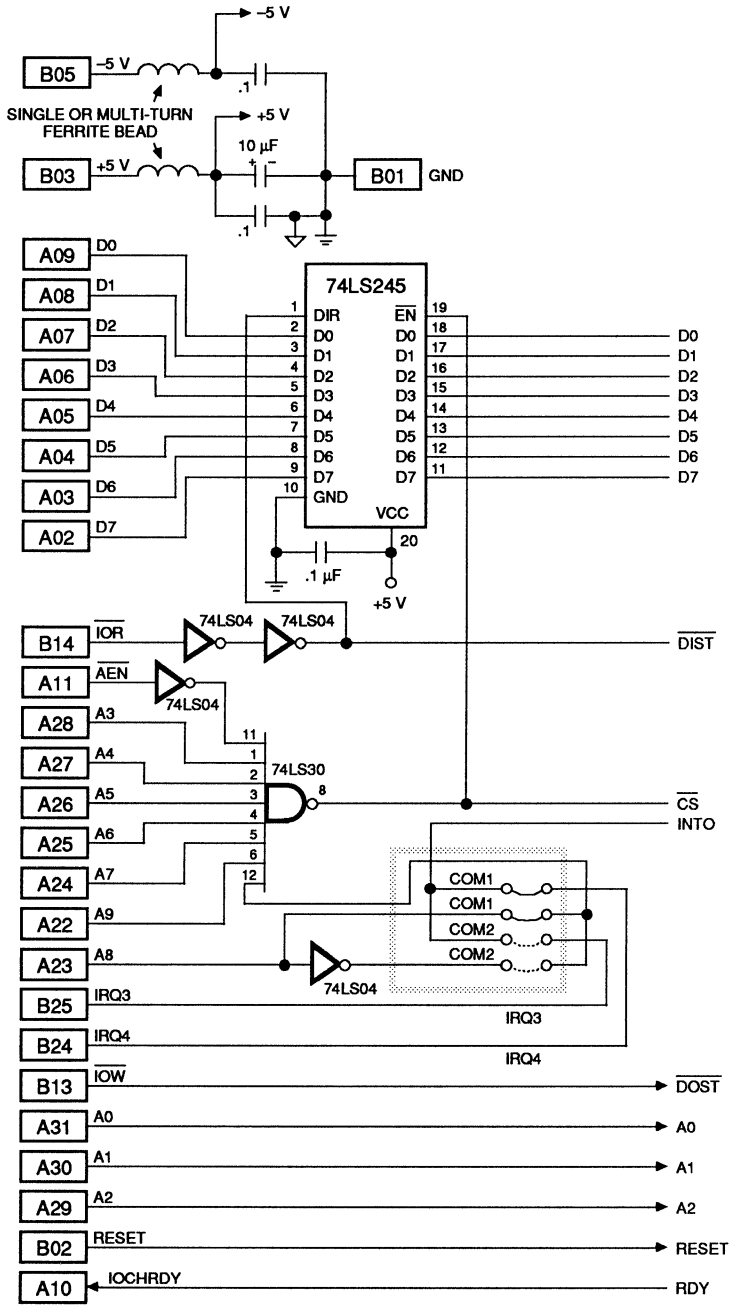


Figure 11. PC Bus Interface Address Decoder

For additional application information, consult the MAP data sheets (SC11006, SC11024, etc.).

Detailed firmware information is available through your local Sierra sales office.

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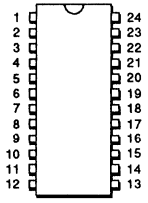
FEATURES

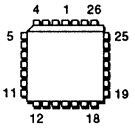
- ☐ All modulators, demodulators and filters with compromise equalizers on chip
- ☐ Call progress mode, tone generators for DTMF, V.22 guard and calling tones
- ☐ On-chip hybrid
- ☐ Pin programmable receiver gain
- ☐ Bell 212A/103 and CCITT V.22/V.21 compatible; V.22 notch filter included
- ☐ Serial control interface
- ☐ Programmable audio port
- ☐ All loopback diagnostics
- ☐ Pin compatible to SC11004/SC11014

24-PIN DIP PACKAGE



SC11015CN

28-PIN PLCC PACKAGE



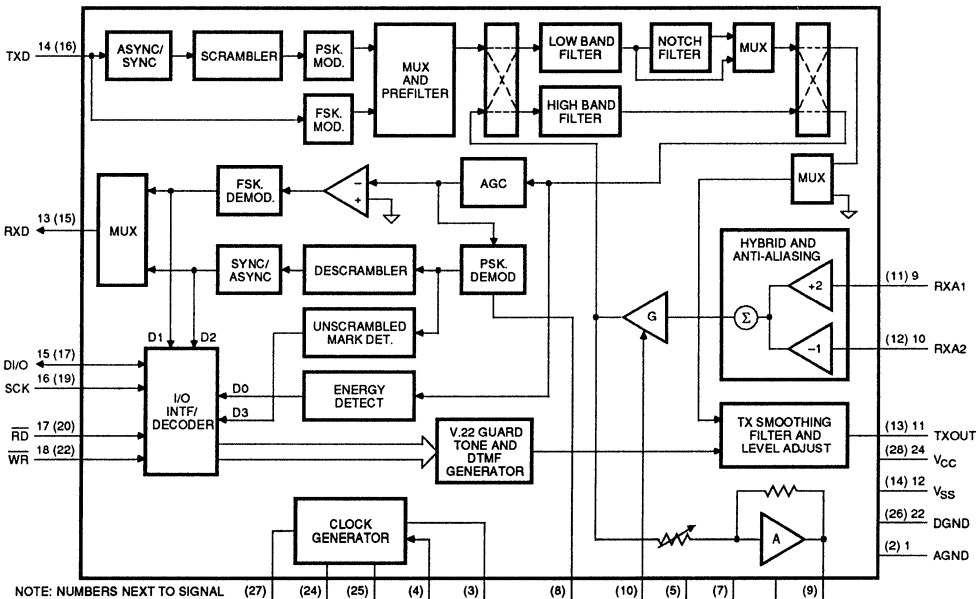
SC11015CV

GENERAL DESCRIPTION

The SC11015 is a complete 300/1200 bit per second modem. All signal processing functions needed for a full duplex, 300/1200 bps 212A/103 or V.22/V.21 compatible modem, including the FSK and PSK modulators and demodulators and the high-band and low-band filters with compromise amplitude and group delay equalizers are integrated on a single chip. Built with Sierra's proprietary CMOS process that allows analog and digital functions to be combined on the same chip, the SC11015 features call progress monitoring and circuits for generating DTMF and V.22 guard tones. A two-to-four wire hybrid with pin programmable receiver gain is also included on chip simplifying the interface to a DAA. An external hybrid may also be used, if desired. The SC11015 also includes analog, digital and remote digital loopback diagnostics for self-testing. The SC11015 contains all of the features of the SC11014 and, in addition, offers a pin programmable receiver gain amplifier to compensate for the insertion loss of the DAA coupling transformer.

With the addition of a digital controller, such as an 8-bit microcontroller and a data access arrangement (DAA), a highly cost effective, integrated, intelligent modem can be built. When used with the Sierra SC11007 modem controller—an 8-bit processor combined with a UART—a complete Hayes command set compatible modem can be configured, occupying minimum board area. All that is needed for stand-alone applications is the SC11015 modem, the SC11008 controller, a DAA and RS-232 interface. They can operate in synchronous or asynchronous mode and handle 8, 9 or 10 bit words.

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1 (2)	AGND	Analog ground
2 (3)	TXCK0	Transmitter clock output. In high speed, synchronous, internal mode, this output supplies a 1200 Hz clock to the DTE.
3 (4)	TXCK1	In high speed, synchronous, external mode, this pin is an input for receiving a 1200 Hz clock from the DTE.
4 (5) 5 (7)	TEST 1, TEST 2	Used by Sierra for testing. Make no connection to these pins — they MUST be left floating.
6, (8)	RXCK	Receiver clock output. In high speed, synchronous mode, the modem supplies a 1200 Hz clock on this output.
7, (9)	Audio Out	Output of the hybrid is passed through a programmable attenuator and brought out on this pin. 4 levels of received signal can be programmed using the control codes listed in Table 1 (Page 8).
8, (10)	GS	Gain Select. When left open or tied to V_{SS}, the compensation is 0 dB; connected to ground, +2 dB compensation is provided; And when tied to V_{CC}, the compensation is +3 dB.
19 (1, 6, 18, 21, 23)	NC	No Connect. These pins must be left floating. Do NOT ground these pins or tie them to V_{CC} or V_{SS}.
9 (11) 10 (12)	RXA1, RXA2	Received data carrier
11 (13)	TXOUT	Transmit data carrier output
12 (14)	V_{SS}	–5 V power supply
13 (15)	RXD	Receive data. The modem demodulates the received carrier and outputs data on the pin. A logic low level is space and a logic high level is mark. The controller can force the demodulator output to the mark state by sending the code 02.
14 (16)	TXD	Transmit data. Data on this input is modulated by the modem and output on TXOUT pin. A logic low is space and a logic high is mark.
15 (17)	D I/O	Data I/O pin. Data is shifted in serially when $\overline{WR}$ is low on rising edges of SCK clock. Data is transferred to a latch when $\overline{WR}$ goes high. Up to 7 data bits can be sent. Input codes are defined in Table 1. Data is read from the modem serially when $\overline{RD}$ is low, on rising edges of SCK clock. Up to 4 data bits can be read. Output codes are defined in Table 1 (Page 8).
16 (19)	SCK	Serial shift clock is applied to this pin. It is normally high until data is sent to or read from the modem.
17 (20)	$\overline{RD}$	Strobe output from controller for serially reading data from the modem.
18 (22)	$\overline{WR}$	Strobe output from the controller for shifting data to the modem.
20 (24) 21 (25)	XTAL1, XTAL2	Pins for connecting a 7.3728 MHz crystal. An external CMOS (+5 V) clock signal can be applied to the XTAL1 pin, with XTAL2 left open. If a TTL clock is used, it must be capacitively (100 pF) coupled into XTAL1.
22 (26)	DGND	Digital ground
23 (27)	CKOUT	Buffered crystal oscillator signal is output on this pin. It can drive one LS TTL load.
24 (28)	V_{CC}	+5 V power supply

Numbers in ( ) refer to 28-Pin PLCC Package.

FUNCTIONAL DESCRIPTION OF THE SC11015 MODEM

Major sections of the SC11015 modem are a transmitter, a receiver, low-band and high-band filters, a two-to-four wire hybrid, tone generators and interface logic. It also contains an energy detector that's used for detecting the carrier and call progress monitoring and an audio output for monitoring the line.

The SC11015 modem requires ±5 V and is available in a 24-pin DIP as well as a 28-lead plastic chip carrier with 'J' leads for surface mount applications. The transmitter section consists of an async/sync convertor, scrambler, PSK modulator and FSK modulator. In the high speed mode (1200 bps), the PSK modulator is connected to the filter. In the low speed mode (300 bps), the FSK modulator is connected to the filter.

Transmitter

Since data terminal and computers may not have the timing accuracy required for 1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync convertor accepts asynchronous serial data clocked at a rate between 1200 Hz + 1%, – 2.5%. It outputs serial data at a fixed rate of 1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync convertor is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first two stages of the shift register form the dibit that is applied to the PSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band centered at 2400 Hz or the low band, centered at 1200 Hz. A 1200 bps modem actually sends two bits at a time, called a dibit; dibits are sent at 600 baud, the actual rate of transmission; 600 baud is the optimum rate that can be transmitted over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

The dibit applied to the PSK modulator produces one of four differential phase shifts of the square wave carrier signal (1200 Hz or 2400 Hz) at the 600 Hz baud rate. The resultant waveform is passed through a wave shaping circuit that performs a raised cosine function (this is the shape factor called out in the CCITT V.22 spec, and it also meets the Bell 212A requirement for optimum transmission). The wave shaped signal is then passed through either the low-band or high-band filter depending upon originate or answer mode selection.

For low speed operation the FSK modulator is used. It produces one of four precision frequencies depending on orignate or answer mode and the 1 (mark) or 0 (space) level of the transmit data. Different frequencies are used for V.21 and 212A modes. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop. In the Call Progress Monitoring mode, the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog

loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second order low-pass switched-capacitor filter that adds the modem transmit signal to the DTMF or V.22 guard tones. It also provides a 3 dB per step programmable gain function to set the output level.

Receiver

The receiver section consists of an energy detector, AGC, PSK demodulator, FSK demodulator, descrambler, and sync/async convertor.

The received signal is routed through the appropriate band-pass filter and applied to both the energy detector and AGC circuit. The energy detector is based on a peak detection algorithm. It provides a detection within 17 to 24 ms. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels.

The AGC circuit is a programmable gain amplifier that covers a wide range. Output of the AGC amplifier is rectified and compared with two preset levels corresponding to desired high and low limits. Outputs of the comparators control an up/down counter such that the received signal is amplified to the desired level. Receive signal input range is 0 to –45 dBm measured at the chip.

The PSK demodulator uses a coherent demodulation technique. Output of the AGC amplifier is applied to a dual phase splitter that produces an in-phase and 90 degree out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by the recovered carrier. The baseband components are low-pass filtered to produce I and Q channel outputs. (In phase and Quadrature). The I and Q channel outputs are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. The signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled to produce the received dibit data. The recovered carrier for the demodulator is generated by another PLL which is controlled by the amplitude of the error signal formed by the difference of the I and Q outputs.

The descrambler is similar to the scrambler. The received dibit data is applied to the D input of a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with input data to produce received data.

In the asynchronous mode, data from the descrambler is applied to the sync/async convertor to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (over-speed data), these stop bits are reinserted. Underspeed data is passed essentially unchaged. Output of the sync/async convertor along with the output of the FSK demodulator is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed, and outputs received data on the RXD pin.

For low speed operation, the FSK demodulator is used. The output of the AGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, this matching is provided by an external resistor connected between the RXA1 and RXA2 pins on the SC11015. The filter section provides sufficient attenuation of the out of band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass anti-aliasing filter.

Internal Hybrid

The SC11015 internal hybrid, shown in Figure 1, is intended to simplify the phone line interface. In addition, there is a gain select feature to compensate for the loss in the line coupling transformer used in the DAA. By tying this pin to V_{SS}, ground or V_{DD}, compensation levels of 0, +2 or +3 dB, respectively, are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. With a 3 dB loss transformer for example, the energy detect on/off levels measured at the line will be in the range of –40/–45 dB rather than –43/–48 dB as specified at the chip, if the internal compensation is not used.

External Hybrid

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC11015 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. For example, if the TLC1, TLC0 level control codes are set to 0 and 1 respectively so as to obtain –9 dBm at the line, the chip actually puts out –3 dBm at the TXOUT pin (pin 11). Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired –9 dBm. In practice however there is impedance mismatch and a loss in the coupling transformer. Therefore it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain G_R and transmit gain G_T are set by the ratios of resistors R2, R1 and R6, R5 respectively (Figure 2).

The circuit can be analyzed as follows:

$$V_R = -\frac{R2}{R1}\left(V_{TR}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)V_y$$

$$V_y = -\frac{R6}{R5}V_x$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_Y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_Y = 2\,V_{TX}$,

$$V_R = -\frac{R2}{R1}\left(V_{TX}+V_{RX}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)2V_{TX}$$

$$= -\frac{R2}{R1}V_{RX} + \left[\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}$$

Solving for R3/R4

$$\frac{R3}{R4} = 1 + \frac{2R1}{R2}$$

Additionally,

$$G_R = \frac{R2}{R1} \text{ and } G_T = \frac{R6}{R5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive loss in the coupling transformer is 2.5 dB, then:

$$\frac{R2}{R1} = \text{INV Log}\left(\frac{G_{RdB}}{20}\right) = \text{INV Log}\left(\frac{2.5}{20}\right) = 1.333$$

Similarly, $\frac{R6}{R5} = 1.333$ and $\frac{R3}{R4} = 2.5$

Some typical values are:
R1=20 kΩ, R2=27 kΩ, R3=13 kΩ, R4=5.1 kΩ, R5=20 kΩ and R6=27 kΩ

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6 and capacitor C1 can be eliminated and point X connected to point Y in the circuit of Figure 2 to achieve a more cost effective external hybrid arrangement.

The SC11015 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, RXA2 is connected to ground and the receive signal is connected to RXA1. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

The tone generator section consists of a DTMF generator and a V.22 guard tone generator. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and * and # keys. The V.22 guard tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the Data I/O pin. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50 kΩ is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation — no attenuation, 6 dB attenuation, 12 dB attenuation and squelch are provided through the ALC1, ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Crystal Oscillator

The SC11015 includes an inverting amplifier between pins 20 and 21 with an internal bias resistor to simplify the design of the crystal oscillator. The parallel resonant, 7.3728 MHz ±0.001% crystal, designed for a load capacitance of 20 pF, should be connected across pins 20 and 21. Two capacitors of typical values 27 pF from pin 20 to digital ground (DGND pin 22) and 47 pF from pin 21 to DGND should be connected. With the recommended crystal, Saronix, NYMPH, NYP073-20 and these capacitor values, a highly accurate and stable crystal oscillator can be designed. Since the carrier frequency must be within ±0.01% of the normal 1200/2400 Hz, it is important to measure the actual crystal oscillator frequency at CKOUT (pin 23) and adjust the external capacitors for a given circuit board layout, if necessary.

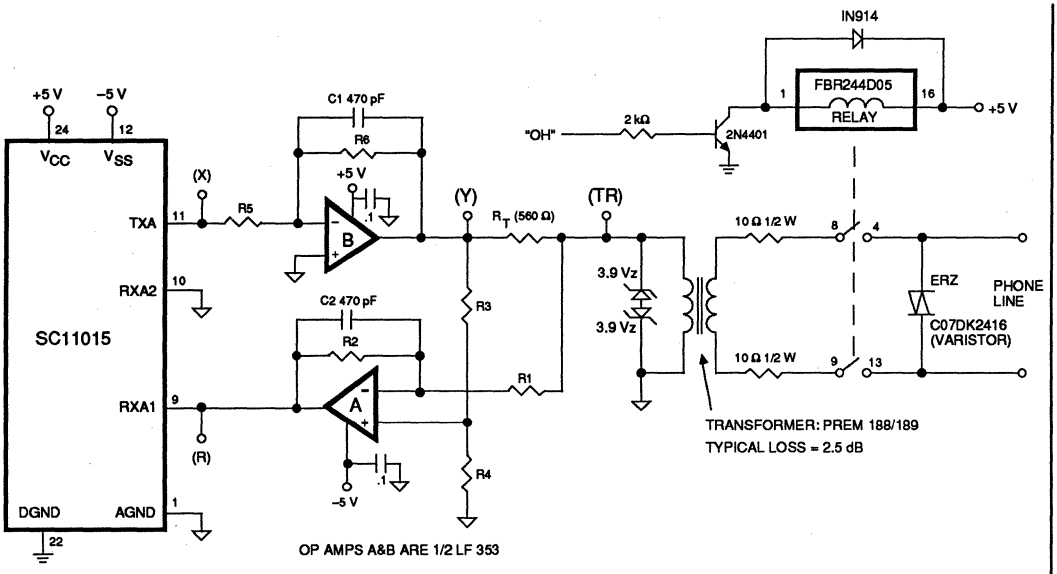


Figure 2. Using an External Hybrid with the SC11015

FUNCTIONAL DESCRIPTION OF THE SC11007 AND SC11008 CONTROLLERS

The SC11007 modem controller, implemented in Sierra's two micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including an 8-bit microprocessor, 8k by 8 bytes of ROM and 128 by 8 bytes of RAM, it also contains the functionality of an 8250B UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem for the PC consists of the SC11007 controller, the SC11004/14/15 modem and the DAA. All of the popular communications software written for the PC will work with the SC11004/14/15/SC11007 set.

Another version of the controller, the SC11008, is intended for RS-232 applications. It contains the same processor, memory and UART as the SC11007 and has the same interface to the modem chip. The difference is that the UART is turned around so the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The SC11008 provides a standard 5 V logic level interface—RS-232 drivers are required to interface to the port. Like the SC11007, the SC11008 comes preprogrammed with the Hayes 'AT' command set, and when used with the SC11015 modem, emulates a Hayes-type stand-alone modem. The SC11007 and SC11015 emulates a Hayes-type IBM PC plug-in card modem.

But the chip set is by no means limited to implementing a Hayes-type smart modem. Sierra is in the custom IC business and both chips were designed with this in mind. For example, only about 6K bytes of the SC11007's ROM is used for the handshaking and smart modem code, leaving 2K bytes for additional features that a customer may specify. And since the controller is ROM programmable, any command set, not just the Hayes 'AT' set, can be implemented.

Both the SC11007 and SC11008 require +5 V and are available in either a 28-pin DIP or a 28-lead plastic chip carrier with 'J' leads for surface mount applications. Besides the four-line interface for the SC11004/14/15 modem, the SC11007 controller has a 8-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 8250B UART. It also has control lines for ring indication, the off-hook relay and data/voice relay; these three lines connect to the DAA.

In the SC11008, the 8-bit port becomes the switch input lines and the address, chip select, DIST and DOST lines become the six lines for the RS-232 interface. These six lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control—so the

main difference between the SC11007 and SC11008 is the ROM code. It also contains the same modem and DAA interface lines as the SC11007.

The SC11007 and SC11008 are truly ASIC controllers—they are designed to control a modem or other peripheral that operates at a moderately slow rate up to 1200 bits per second. What's unique about the SC11007, for example is that it allows a slow peripheral to interface to a high speed bus, without making the main processor slow down.

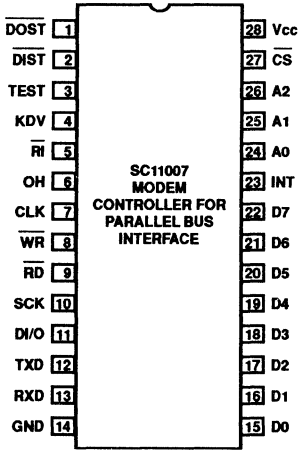
This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11007 compatible with this software, the registers were included.

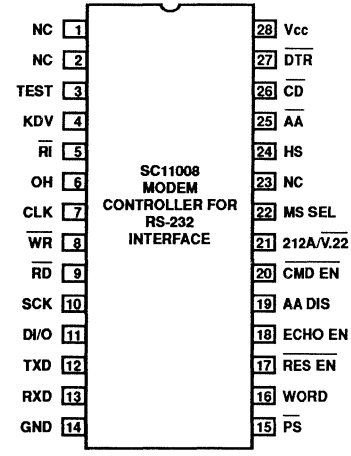
The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like in a Hayes-type modem. The escape sequence is three + signs—+++ —in the default mode, but it can be changed in software.

The actual processor contains an 8-bit data path and can execute 19 instructions with five different addressing modes: direct, indirect, immediate, register direct and register indirect. There is 8K by 8 of ROM on chip for program storage.

To the system bus, the SC11007 looks and acts just like an 8250B UART. Communications software written for this UART will work with the SC11007 and SC11008. The Sierra chip set is truly a Hayes-type modem in two chips.

CONNECTION DIAGRAMS—SC11007 AND SC11008 CONTROLLERS





THE SC11015 & SC11007/SC11008 SYSTEM

The only external components required by the SC11015 are the 600 Ω line matching resistor, a 7.3728 MHz crystal—a standard frequency—and a 20 & 47 pF capacitor from each leg of the crystal to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11015 can directly drive a high impedance (50 kΩ) earphone-type transducer.

The controllers support asynchronous, 10-bit words only.

The SC11007 modem controller's clock in line is driven by the SC11015's clock out line, so only one crystal is needed. The SC11007 interfaces directly to an IBM PC bus—no buffers are required. The only external parts may be for COM1, COM2 & $\overline{CS}$ decoding inside the PC.

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

All modems require a DAA. A DAA or data access arrangement is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω; a relay for disconnecting the modem from the line; a ring

detector, typically an optoisolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by any of many consultants and labs around the country. The fee is typically $2,000 and it takes several months. Another alternative is to buy a DAA, supplied by several manufacturers.

212A is a Bell specification that calls for 1200 bit per second, full or half duplex data transmission with a fallback mode of 300 baud (Bell 103). It is not 1200 baud; the spec calls for transmission of dibits—2 bits per baud so the 1200 bps transmission takes place at 600 baud. The same is true for V.22—it's 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; there is a CCITT standard for 300 and that's V.21.

V.22 also calls for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The SC11015 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone when in the receive mode.

All modems require a Hybrid. Hybrid is a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the SC11015, this is done with op amps, but the separate signals—TXOUT and RXA2—are also brought out so an external hybrid can be used, if desired. The combined signal comes out on the RXA1 pin and matching resistor—typically 600 Ω — is connected between RXA1 and RXA2.

SC11015 SPECIFICATIONS

Table 1. Definition of I/O Codes

1. Instructions to the modem IC (See Note 1 and 2). Data on the DI/O pin shifted into the modem when $\overline{WR}$ is low, on rising edges of the SCK clock. Data is transferred into a latch when $\overline{WR}$ goes high. (See Figure 2 for write cycle waveforms). Up to 7 data bits (D0–D6) can be sent to the device. These bits control the operating modes of the modem as shown below:

D6	D5	D4	D3–D0	HEX CODE	MODE/FUNCTION
Non tone mode:					
0	1/0	0	0	20/00	Reset (set default values)
0	1/0	0	1	21/01	Tone On/Off (tone mode enable/disable)
0	1/0	0	2	22/02	Force Receive Data to Mark Off/On (forces RXD pin High if On)
0	1/0	0	3	23/03	TLC0 Transmit Level Control bit 0 (default 0)
0	1/0	0	4	24/04	TLC1 Transmit Level Control bit 1 (default 0)
0	1/0	0	5	25/05	TX Transmitter On/Off (if Off, TXOUT is grounded)
0	1/0	0	6	26/06	ALB Analog Loopback On/Off
0	1/0	0	7	27/07	CPM Call Progress Monitor mode On/Off
0	1/0	0	8	28/08	Connection Indicator (CI) On/Off (see note 4 below)
0	1/0	0	9	29/09	ALC0 Audio Output Level Control bit 0 (default 0)
0	1/0	0	A	2A/0A	ALC1 Audio Output Level Control bit 1 (default 0)
0	1/0	0	B	2B/0B	WLS0 Word Length Select 0 (default 0)
0	1/0	0	C	2C/0C	WLS1 Word Length Select 1 (default 1)
0	1/0	0	D	2D/0D	Sync/Async
0	1/0	0	E	2E/0E	LS/HS: Low Speed/High Speed (FSK/PSK)
0	1/0	0	F	2F/0F	A/O: Answer/Originate
0	1/0	1	0	30/10	Transmit Mark On/Off
0	1/0	1	1	31/11	Transmit Space On/Off
0	1/0	1	2	32/12	Scrambler Off/On
0	1/0	1	3	33/13	DLB Digital Loopback On/Off (also sets Synchronous, Slave Mode)
0	1/0	1	4	34/14	TXDP Transit Dotting Pattern On/Off (Not valid for V.21 mode)
0	1/0	1	5	35/15	Sync Mode Transmit Timing Locked/Free Running
0	1/0	1	6	36/16	Sync Mode Transmit Timing Source External/Slave
0	1/0	1	7	37/17	2100 Hz tone On/Off. Must select low speed mode for operation.
0	2/0	1	8	38/18	1300 Hz tone On/Off. Must select low speed mode for operation.
0	1/0	1	9	39/19	V.21 mode. Must select low speed mode for operation.

D6	D5	D4	D3–D0	HEX CODE	MODE/FUNCTION
Tone mode:					
1	1/0	0	0	60/40	Dial 0
1	1/0	0	1	61/41	Dial 1
1	1/0	0	2	62/42	Dial 2
1	1/0	0	3	63/43	Dial 3
1	1/0	0	4	64/44	Dial 4
1	1/0	0	5	65/45	Dial 5
1	1/0	0	6	66/46	Dial 6
1	1/0	0	7	67/47	Dial 7
1	1/0	0	8	68/48	Dial 8
1	1/0	0	9	69/49	Dial 9
1	1/0	0	A	6A/4A	Dial *
1	1/0	0	B	6B/4B	Dial #
1	1/0	0	C	6C/4C	Output 550 Hz and insert 550 Hz notch in low-band filter
1	1/0	0	D	6D/4D	Output 1800 Hz and insert 1800 Hz notch in low-band filter
1	1/0	0	E	6E/4E	Row disable On/Off (For DTMF test only)
1	1/0	0	F	6F/4F	Column disable On/Off (For DTMF test only)

WLS1	WLS0	Word Length
0	0	8 bits
0	1	9 bits
1	0	10 bits (default)
1	1	11 bits

TLC1	TLC0	Transmitter Output Level (dBm) (Note 3).
0	0	–6
0	1	–3 (default)
1	0	0
1	1	+6

ALC1	ALC0	Audio Output Level
0	0	Output Off (default)
0	1	12 dB attenuation
1	0	6 dB attenuation
1	1	No attenuation

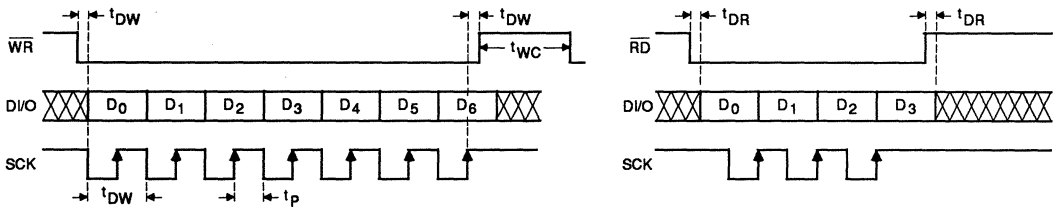
Notes: 1. Default values for the operating modes on power up are those shown to the right of the '/' unless otherwise specified.
2. Data is shifted in and out of the modem with LSB first.
3. Using the internal hybrid and a 600 Ω resistor, these levels will be 6 dB lower at the input to the transformer.
4. After a connection is established, turn CI on to disable unnecessary functions, i.e. if a PSK connection is established, turning CI on will turn off the FSK demodulator.

2. Information from the modem IC. Data is read serially from the modem when $\overline{RD}$ is low, on rising edges of the SCK clock. (See Figure 3 for read cycle waveforms). Up to 4 data bits (D0–D3) can be read as defined below:

D0 Energy Detect 0—no energy 1—energy present

In the CPM mode, the energy detector is connected to the output of the high band filter, if ALB is off, or the scaled low band filter, if ALB is on.

D1	Received data (FSK)	1—Mark	0—Space
D2	Received data (PSK)	1—Mark	0—Space
D3	Unscrambled Mark	1—Detected	0—Not Detected



t_{WC} = 4 µsec
t_{DW} = 200 nsec Min.
t_{PW} = 1 µsec Min.
t_P = 30% to 70% duty cycle
t_{DR} = 200 nsec Min.

Figure 3. Waveforms for Write and Read Cycles

Serial Interface — The 4 line serial interface consists of a bidirectional data pin (DI/O), a write control pin ($\overline{WR}$), a read control pin ($\overline{RD}$) and a clock pin (SCK). In the inactive state, $\overline{WR}$, $\overline{RD}$ and SCK lines must be held in the high state. The read and write functions are controlled only by the mircocomputer. To write data into the SC11015 (see timing waveforms of Figure 2), the controller must first make the $\overline{WR}$ line low. The least significant bit D0 of the data is then placed on the DI/O line. The SCK line is then toggled low and then high to shift the data bit into the SC11015 input register. Data is shifted into the input register on the rising edge of SCK.

There is no special requirement on the duty cycle of the clock signal. The minimum pulse width and data setup times specified in the specifications table must be met. The remaining data bits D1 thru D6 are shifted by repeating the above procedure. Only 7 data bits should be sent. If an 8th data bit is sent, the first data bit D0 will be lost from the input register. The received data will then be D7–D1 rather than D6–D0. To read data from the SC11015 (see timing waveforms of Figure 3), the $\overline{RD}$ line is first made low. The least significant bit D0 is now available on the DI/O line. The SCK line is toggled low and then high to shift the next data bit out of the SC11015 output register. The SC11015 shifts the data out on the rising edges of SCK. The controller should read data on the falling edges of SCK when it will be stable. Note that D0 appears on the DI/O line as soon as $\overline{RD}$ is taken low. If the controller only wants to read the status of the energy detector, there is no need to toggle SCK line. By making $\overline{RD}$ low, the energy detector level can be read by reading DI/O. $\overline{RD}$ can then be taken high. Read operation is terminated by making the $\overline{RD}$ line high. If more than 4 bits are read, the additional bits are returned as 0's.

In the READ mode, the values of D0, D1, D2 and D3 do not change as long as $\overline{RD}$ is low, even though the chip status may be changing. To read out the updated values of these bits, $\overline{RD}$ must be pulled high for at least 1 ms and then taken low again to initiate another read cycle.

The read and write operations can be performed by two simple I/O drivers shown in table 2. The RDMO–DEM subroutine reads data from the SC11015 and places it in the accumulator with the high nibble set to zero. The WTMODEM subroutine sends data placed in the accumulator to the SC11004/14. Both subroutines use register R7 in bank 1 as a data bit counter.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1 — SC11015 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 4.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11015 in the synchronous mode (2D). This provides a 1200 Hz clock on the TXCK0 Pin that can be used as a clock source for the DTE to synchronize its TXD to. The Transmit Phase-Locked-Loop (TX PLL) of the SC11015 will be in free-runing mode. As a result, External/Slave input codes will be ignored by the chip.

Case 2 — SC11015 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode (2D), also select "Locked" (35) and "External" (36) modes.

The TX PLL of SC11015 will then synchronize itself to the clock provided on its "TXCK1" pin.

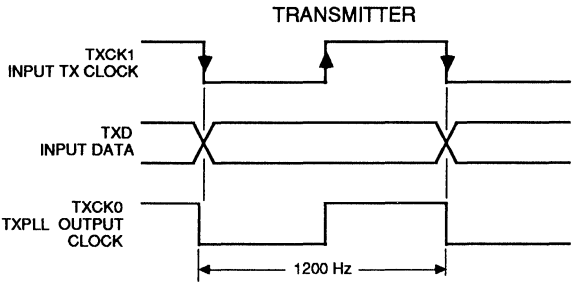
Receiver Timing

In synchronous mode, the recovered clock will be provided on the RXCK pin and the transitions of RXD will be on the falling edges of this clock.

SYNCHRONOUS MODE CHART

Transmitter Timing

Locked (35)	External (36)	TX PLL locks to clock provided on TXCK1
	Slave (16)	TX PLL locks to receiver timing. Should be used in DLB mode only.
Free Running (15)	External/Slave	TXPLL is free running and ignores External or Slave inputs.



Note: 1 SC11015 will sample the data on the rising edge of TXCK1 clock.

Figure 4. SC11015 Synchronous Mode Diagrams

Absolute Maximum Ratings (Notes 1, 2 and 3)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS}–0.6 to V_{CC}+0.6 V
DC Input Voltage (Digital Signals)	V_{SS}–0.6 to V_{CC}+0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 s)	300°C

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating — Plastic Package: –12 mW/C from 65°C to 85°C.

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
F_C	Crystal Frequency		7.3721	7.3728	7.3735	MHz
T_R, T_F	Input Rise or Fall Time	(Note 4)			500	ns

Notes: 4. Does not apply to CKOUT.

DC Electrical Chracteristics (Note 5)

PARAM.	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	V_{CC} = 5 V			15		mA
I_{SS}	Quiescent Current	V_{SS} = –5 V			15		mA
V_{IH}	High Level Input Voltage	Digital Signal Pins $\overline{RD}$, $\overline{WR}$, D I/O, SCK, TXCK1, TXD		2.0			V
V_{IL}	Low Level Input Voltage	Digital Signal Pins $\overline{RD}$, $\overline{WR}$, D I/O, SCK, TXCK1, TXD				0.8	V
V_{OH}	High Level Input Voltage	Digital Signal Pins D I/O, RXD, TXCK0, RXCK	I_{OH} = 40 µA	4.0			V
			I_{OH} = 500 µA	2.0			V
V_{OL}	Low Level Input Voltage	Digital Signal Pins D I/O, RXD, TXCK0, RXCK	I_{OL} = 1.6 mA		0.4	0.6	V
V_{OM}	Maximum Output Signal	TXOUT, RL = 1200 Ω (TLC = 1, TLC0 = 0)		4.0			V_{P-P}
V_{IM}	Maximum Input Signal	RXA1, RXA2 (Using Internal Hybrid)				4.0	V_{P-P}

Note: 5. Min and max values are valid over the full temperature and operating voltage range. Typical values are from 25°C and ±5 V operation.

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQ.	ALLOWABLE ERROR	ACTUAL ERROR
Row 1	697 Hz	±1%	+0.17%
Row 2	770 Hz	±1%	–0.26%
Row 3	852 Hz	±1%	+0.16%
Row 4	941 Hz	±1%	–0.47%
Column 1	1209 Hz	±1%	–0.74%
Column 2	1336 Hz	±1%	–0.89%
Column 3	1477 Hz	±1%	–0.01%
Guard Tones	550 Hz	±20 Hz	–1.4 Hz
	1800 Hz	±20 Hz	+7 Hz

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion			–40		dB
Row Output Level	V_{CC} = +5 V V_{SS} = –5 V TLC0 = 1 TLC1 = 1 Measured at TXOUT Pin		0		dBm
Column Output Level			2		dBm
550 Hz Guard Tone			–3		dB (Note 2)
1800 Hz Guard Tone			–6		dB (Note 2)

Notes: 1. This assumes a crystal of exactly 7.372800 MHz.
2. These levels are referenced to the TX signal level. When guard tones are added, the TXOUT level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

Modem Transmit Signals—Hz (Assume 7.372800 MHz Crystal)

MODE		BELL 103		CCITT V.21		212A/V.22	
		NOMINAL	ACTUAL	NOMINAL	ACTUAL	NOMINAL	ACTUAL
Answer	Mark	2225	2226	1650	1649.4	2400	2400
	Space	2025	2024.4	1850	1850.6		
Originate	Mark	1270	1269.4	980	978.34	1200	1200
	Space	1070	1070.4	1180	1181.53		
Calling Tone				1300	1301.7	1300	1301.7
Answer Tone				2100	2096.9	2100	2096.9

Transmitter

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Character Length	Start Bit + Data Bit + Stop Bit	8		11	bits
Intra-Character Bit Rate	AT TXD (Pin 14)	1170	1200	1212	bps
Input Break Sequence Length	M = Character Length	2M + 3			bits
Output Level Tolerance			±1		dB

Receiver

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Signal Range	AT RXA1	–45		0	dBm
Intra-Character Bit Rate	AT RXD (Pin 13)	1170	1200	1224	bps
Carrier Detect	AT RXA1 (Pin 9)	–48		–43	dBm
Carrier Detect Hysteresis		2			dB
Carrier Detect Delay	For 103, 212A and V.22	10	20	30	ms
Carrier Detect Hold	For 103, 212A and V.22	15	20	24	ms
Carrier Detect Delay	For V.21 Mode	15	30	40	ms
Carrier Detect Hold	For V.21 Mode	20	30	50	ms

APPLICATIONS INFORMATION

Why a Modem/What's a Modem

The voice frequency channels of the general switched telephone network have been used extensively for the transmission of digital data. To use these channels, the data must be put in a form that can be sent over a limited bandwidth line. In voice grade telephone networks, transformers, carrier systems and loaded lines attenuate all signals below 300 Hz and above 3400 Hz.

While the bandwidth from 300 Hz to 3400 Hz is fine for voice transmission, it is not suitable for the transmission of digital data because the data has many frequency components outside this range. To transmit data over phone lines, it is necessary to convert the digital data into a signal that is totally within the voice frequency range. This conversion is performed by a MODEM (MODulator DEModulator).

In full duplex data transmission—the simultaneous sending and receiving of data—Frequency Division Multiplexing (FDM) can be used for data rates up to 2400 bits per second. In FDM, the voice channel is divided into upper and lower bands (called the high band and the low band); one is used for sending and the other for receiving data. The originating terminal transmits in the low band and receives in the high band, while the answering terminal transmits in the high band and receives in the low band.

In low speed modems (300 bit per second transmission rate), the modulation technique commonly employed is called Frequency Shift Keying (FSK). In FSK modems, four separate frequencies are used; 1070 Hz for a zero (also called a space) in the low band, 1270 Hz for a one (a mark) in the low band, 2025 Hz for a zero in the high band and 2225 Hz for a one in the high band. The transmitting modem takes the digital ones and zeros from the terminal and converts them into the proper tones which are then sent over the phone line. The receiving modem takes the tones and converts them back to ones and zeros and sends them to the receiving terminal. Since four frequencies are used, simultaneous transmitting and receiving of data can be accomplished.

Because of the limited bandwidth of the phone line, FSK modems only work up to 600 bits per second for full duplex transmission. This is due to the fact that when the modem shifts between the two frequencies (for mark and space) it generates a frequency spectrum (it is a type of FM—frequency modulation—transmission). The faster the data rate, the wider the spectrum. The limit for full duplex FSK transmission is 600 bits per second, before the available audio spectrum is used up—allowing for enough separation between the frequency bands to reliably decode or demodulate the data. There are 1200 bps FSK modems, but these are half duplex—they can only send OR receive data at 1200 bps.

In higher speed, full duplex modems (1200 bit per second transmission rate) a different modulation technique is employed. Called PSK (for Phase Shift Keying), this technique uses one carrier frequency for the high band—2400 Hz—and one for the low band—1200 Hz—for sending and receiving data. For each carrier frequency (one for transmitting and one for receiving), one of four phase angles is used: 0, 90, 180, or 270 degrees. The data is sent two bits at a time, or in dibits. Since there are four ways to send two bits at a time—00, 01, 10 or 11—each of the four phases represents one unique dibit. While the data rate is 1200 bits per second, the baud rate (the rate at which information packets are sent) is 600 because two bits (dibits) are sent in each packet. Again, 600 packets per second (600 baud and, in this case, 1200 bps) is the limit for transmitting full duplex data over the general switched telephone network using FDM.

Call Progress Monitor Operation

The modem controller uses the high-band and low-band filters in the SC11015 for call progress monitoring. When the SC11015 is put in the CPM and originate mode, the ALB mode provides a means of connecting either the high-band filter (ALB = 0) or the scaled low-band filter (290–660 Hz) (ALB = 1) to the energy detector. Output of the energy detector is monitored by reading bit D0 for detection of call progress or voice/answer information, using the duration and repetition rate as the criteria for detection.

A typical call establishment sequence is as follows:

Dial tone detection— The controller puts the SC11015 in the Originate, CPM mode with ALB = 1 and operates the off-hook relay in the DAA by making the OH output high. After a short delay (typically 300 ms), it monitors the output of

the energy detector (ED). If the output is continuously high for at least 1 second; it is recognized as a valid dial tone. If the output is not continuous then the controller continues to monitor until a timeout occurs (typically 5 seconds). If a dial tone is not detected within this timeout, the controller returns a 'NO DIAL TONE' message to the DTE and aborts the call. If a dial tone is detected, it proceeds to dial the number as follows.

Dialing—The controller will use the specified format (tone or pulse).

If a pause is required in the dialing sequence for a second dial tone, then after dialing is done, the controller will wait for approximately 2.5 seconds and then start to monitor the ED output by alternately toggling the ALB mode at a rate of approximately 200 ms. This allows detection of ringback/busy call progress tones or voice/answer tone. The toggling rate is based on the settling times of the filters as well as the response time of the ED. Once energy is detected at the output of the ED, the controller will maintain the selected ALB mode until detection is made. The criteria for various detections are described below.

Busy tone detection—If the number of transitions of the ED output exceeds 7 over the 5 second window when looking for ringback tone, it will be assumed to be a busy signal. The controller will then abort the call and return a 'BUSY' message to the DTE (in X4 mode).

Answer tone detection—If the output of the high-band filter is continously high for at least 2 seconds, the controller will assume it to be an answer tone from the distant modem, then returns 'CONNECT' and proceeds with handshaking sequence necessary to establish a data call.

If bust tone or answer tone is not detected within the time specified in S7, the controller hangs up and returns 'NO CARRIER' message.

Silence detection—If the cumulative duration of ED over the 5 second window is less than 0.7 second, once the window is started, it is recognized as silence. The controller then returns a 'NO ANSWER' message to the DTE and aborts the call.

Specific Applications

The SC11015 modem performs all the signal processing functions required in a 212A/V.22 modem. Like all modems, it requires an external controller to implement the handshaking protocols and control functions. The controller's task is simplified by the use of a 4 line serial interface as opposed to a multiline parallel interface. In particular, only I/O pins are used on a single chip microcomputer. More pins are then available for other interfaces such as DAA, RS-232, switches and lights. In most modem applications this will eliminate the need for external latches and buffers for additional I/O pins.

Figure 5 shows the SC11015 modem IC used with the SC11007 controller to make a complete parallel bus Hayes-type smart modem.

Figure 6 shows the SC11015 modem IC used with the SC11008 controller to make a complete RS-232 serial interface Hayes-type smart modem.

Figure 7 shows the schematic of a stand-alone smart modem implemented with the SC11015 and the 8031—the ROMless version of the 8051 microcomputer. Even though 16-port I/O pins are used up on the 8031 for interfacing with the external ROM, enough pins are still available for the other interfaces because of the serial interface used on the SC11015. The 8031 microcomputer was selected because of its wide use in current stand-alone and integrated smart modems.

Oscillator—The SC11015 includes an inverting amplifier and a bias resistor so that a crystal oscillator can be designed by connecting a 7.3728 MHz crystal and two capacitors (27 pF and 47 pF) to XTAL1 and XTAL2 pins as shown in the schematic. A buffered TTL compatible clock output is available on the CLOCK OUT pin to drive the microcomputer.

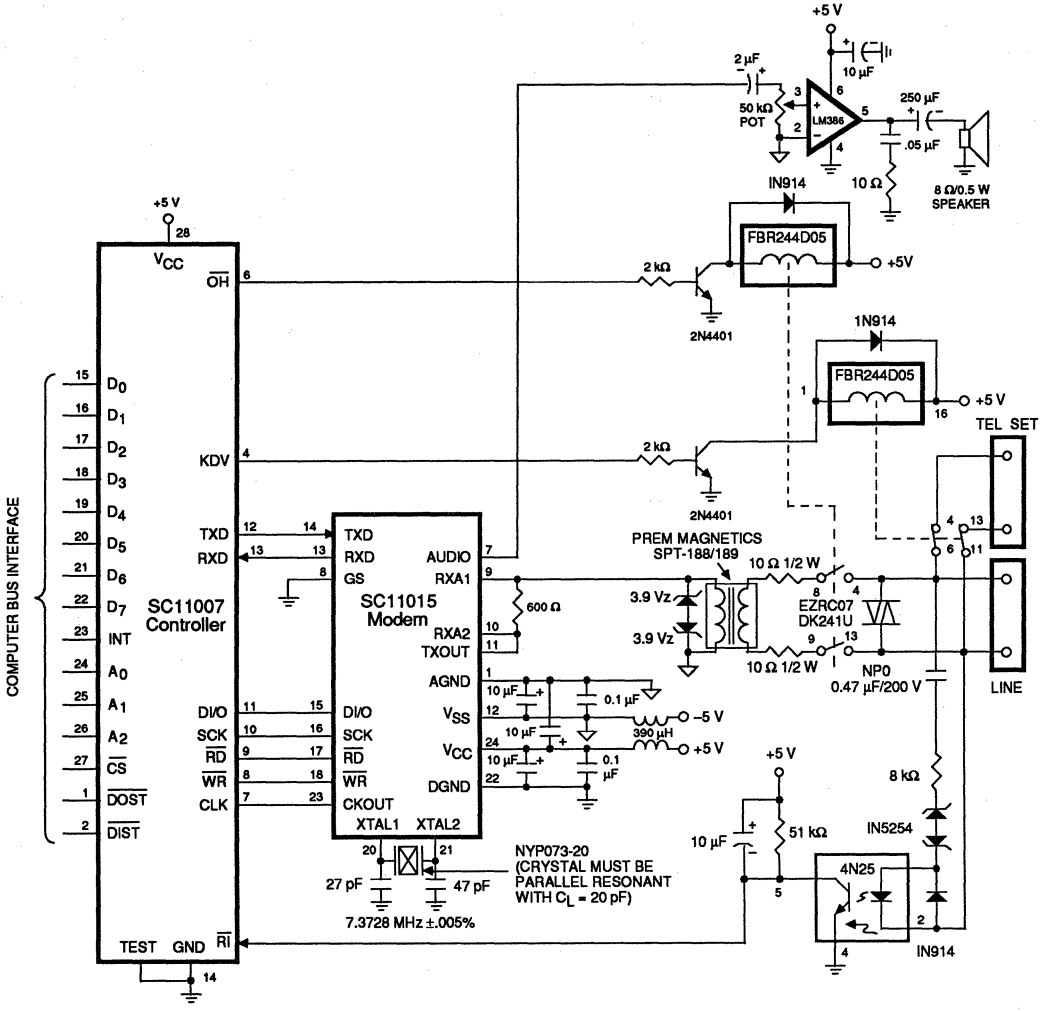


Figure 5. Internal 212A/V.22 Smart Modem Using the SC11015 Modem IC and the SC11007 Controller

Notes:
1. Connecting GS (pin 8) to ground compensates for 2 dB loss in the coupling transformer.
2. Analog ground (⏚) and digital ground (⏚) should be routed separately and connected together at the common point of the power supply for best performance.
3. Power supply decoupling capacitors should be tantalum type.

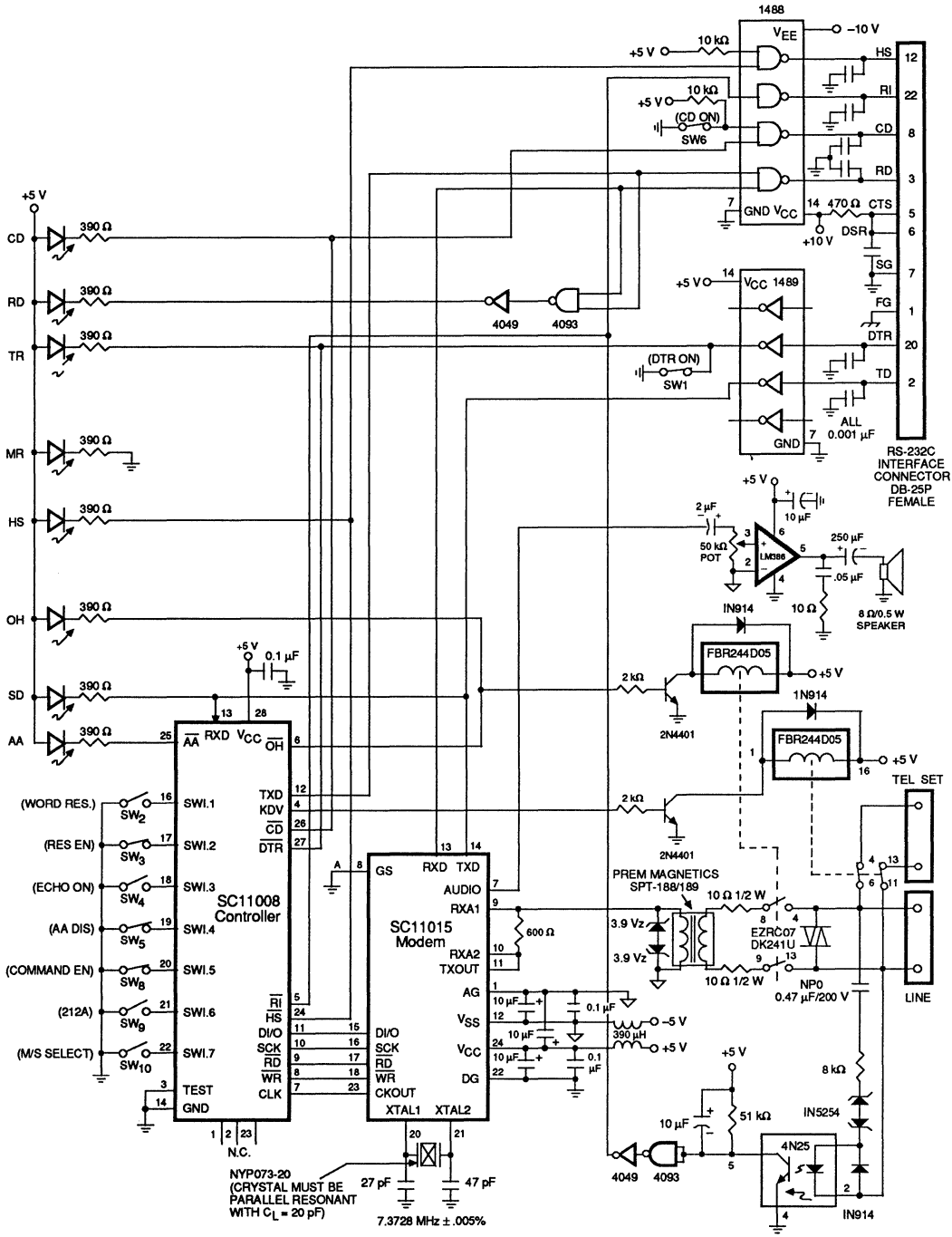


Figure 6. 212A/V.22 Stand-Alone Intelligent Modem Using the SC11015 Modem IC and the SC11008 Controller

Notes:
1. Connecting GS (pin 8) to ground compensates for 2 dB loss in the coupling transformer.
2. Analog ground (⏚) and digital ground (⏚) should be routed separately and connected together at the common point of the power supply for best performance.
3. Power supply decoupling capacitors should be tantalum type.

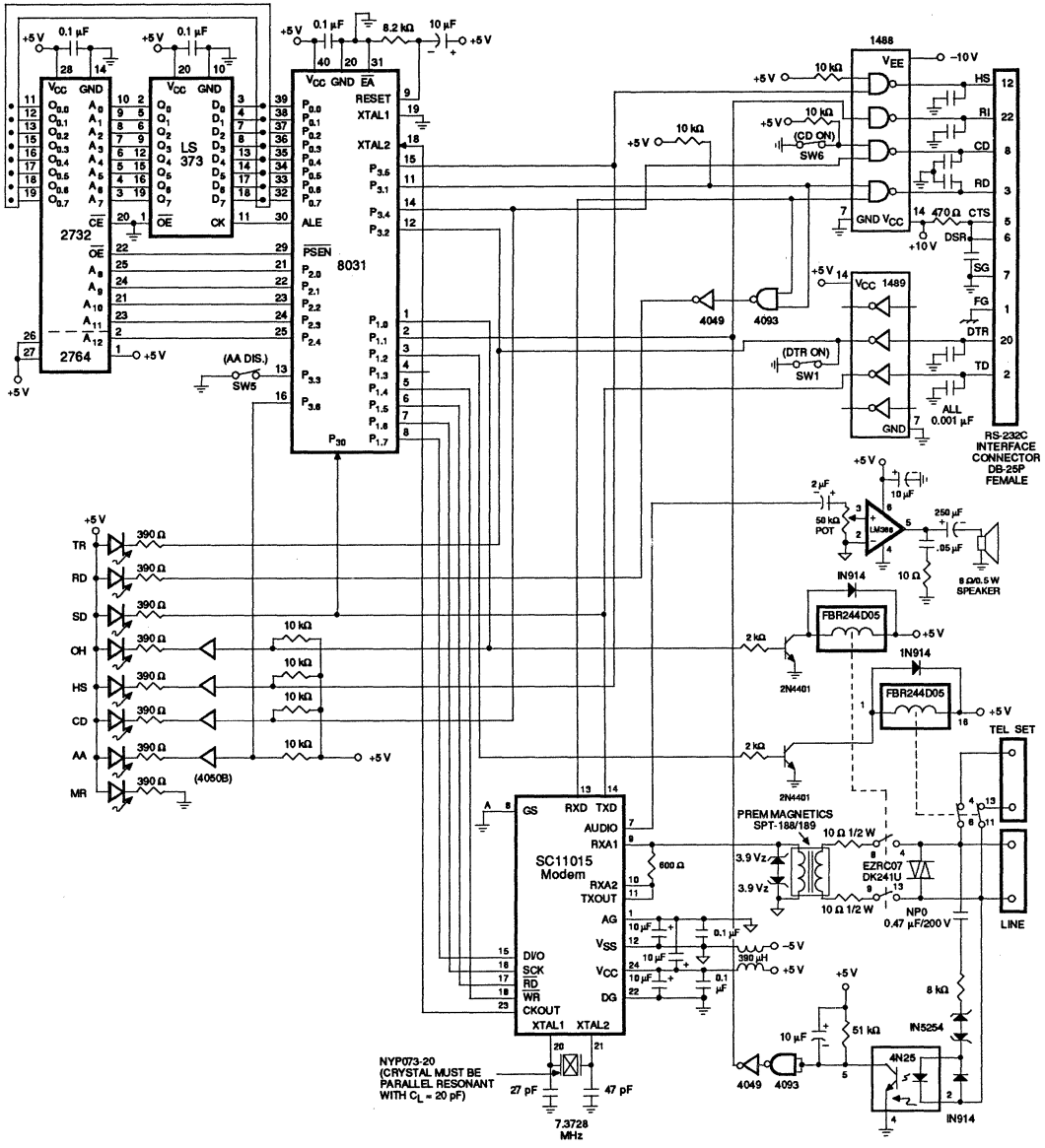


Figure 7. 212A/V.22 Stand-Alone Smart Modem Using the 8031 Controller with SC11015 Modem

Notes:
1. Connecting GS (pin 8) to ground compensates for 2 dB loss in the coupling transformer.
2. Analog ground (⏚) and digital ground (⏚) should be routed separately and connected together at the common point of the power supply for best performance.
3. Power supply decoupling capacitors should be tantalum type.

Power Supply Decoupling and Circuit Layout Considerations

For optimum performance and to obtain the best possible performance at low received signal levels with low S/N ratio, it is important to use the recommended power supply decoupling circuit as shown in Figures 5, 6, and 7. Small inductors in series with the positive and negative supplies help suppress RFI as well as improve the power supply noise rejection capability of the SC11015 when used with the decoupling capacitors. The 10 µF capacitors should be tantalum type while the 0.1 µF capacitors should have a good high frequency rejection characteristic, monolithic ceramic types are recommended. It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11015 as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply.

```
WTMODEM:    CLR     P1.4            ;WR → 0; Initiate Write Cycle
            SETB    RS0             ;Select Bank 1
            MOV     R7, #7          ;Set Data Bit Counter to 7

OUTNEXT:    RRC     A               ;Bit → Carry
            CLR     P1.6            ;Toggle Clock Line Low
            JC      SETPB           ;Set/Clear DI/O Line on Carry
            CLR     P1.7
            LJMP    OUTPUT

SETPB:      SETB    P1.7

OUTPUT:     SETB    P1.6            ;Toggle Clock Line High
            DJNZ    R7, OUTNEXT     ;Loop Till Data Bit Counter is Zero
            SETB    P1.7            ;Return to Initial Condition
            SETB    P1.4
            CLR     RS0
            RET

RDMODEM:    CLR     P1.5            ;RD → 0 ; Initiate Read Cycle
            SETB    RS0
            MOV     R7, #8

INNEXT:     CLR     P1.6
            MOV     C, P1.7         ;Data Bit → Carry
            RRC     A               ;And into Accumulator
            SETB    P1.6
            DJNZ    R7, INNEXT      ;Loop Till Data Bit Counter is Zero
            SETB    P1.5            ;Return to Initial Condition
            CLR     RS0
            RET
```

To dial a digit, the sequence shown below can be used. It is assumed that register R2 holds the digit to be dialed and memory location S11 holds the on/off duration of the tines in milliseconds.

```
TDIAL:      MOV     A, #21H         ;Turn on Tone Mode
            LCALL   WTMODEM
            MOV     A, R2           ;Read Digit
            ORL     A, #60H         ;Form Digit On Command
            LCALL   WTMODEM
            MOV     A, S11
            MOV     B, #10
            DIV     AB              ;Find Number of 10 ms Increments
            MOV     R1, A           ;Save It
            LCALL   DLOOP           ;Wait 10 ms Times Number in R1
            MOV     R1, A           ;Restore R1
            MOV     A, R2           ;Form Digit Off Command
            ORL     A, #40H
            LCALL   WTMODEM
            LCALL   DLOOP           ;Wait 10 ms Times Number in R1
            LJMP    NEXTDG          ;Go for Next Digit
```

Table 2. Serial I/O Driver Routines

In the following examples it is assumed that the clock frequency for the 8031 is 7.3728 MHz and that timer 0 is set in the auto-reload mode cycling at the rate of 416.66 µs. References are also made to certain registers used in Hayes compatible smart modems.

Initialization—The SC11015 does not have a power on reset circuit. The controller must put the device into the proper operating mode on power turn on. By sending a reset code, the device will enter a default mode as follows: high speed, asynchronous, originate, transmitter off, RX data clamped to mark, transmit level = –12 dBm, audio off and scrambler on. This mode is set up by the following lines of code:

```
MOV     A, #0          ;Reset Code
LCALL   WTMODEM        ;Write It
```

Dialing—The SC11015 includes an on chip DTMF dialer. It is necessary to adjust the transmit level during dialing since the tone level is internally set to be 6 dB below the transmitted carrier level. The following lines of code will set the tone level at the line to be –6 dBm for low group and –4 dBm for the high group tone:

```
MOV     A, #23H        ;TLC0 = 1
LCALL   WTMODEM
MOV     A, #24H        ;TLC1 = 1
LCALL   WTMODEM
```

Call Progress Monitoring—The progress tones can be monitored readily by activating the call progress monitor (code = 27H) and analog loopback (code = 26H) modes. The low band filter is then scaled down by a factor of 2.5 to center over the frequency range of 300 Hz to 660 Hz. Output of the energy detector monitored on the D0 bit then provides the necessary cadence information for detection of various call progress conditions. For example, dialtone is detected if the energy detector output is continuously high for at least 1 second. Busy line condition is recognized if the number of transitions of the energy detector output exceeds 7 over a period of 5 seconds and if the cumulative on duration exceeds 2 seconds.

Handshaking Sequences—Sequences necessary for establishing calls in various operating modes are provided in the following paragraphs. Numbers in parentheses indicate the hex code values sent to the SC11015 to implement that function of data bit received from the SC11015 for monitoring a given function.

A. Originating call in high speed (212A) mode:

1. Clamp receive data to mark condition (2)
2. Sample energy detector output (D0) to see if answer tone is present.
3. If continuous answer tone is detected for time set in register S9 (typically 600 ms) prior to timeout set in register S7 (typically 30 s) proceed with handshaking. Otherwise output NO CARRIER to data terminal and abort call.
4. Transmit mark (30).
5. Turn transmitter on (25).
6. Wiat for 300 ms.
7. Sample PSK data output (D2) at twice the bit rate (every 416.66 µs).
8. If continuous PSK data mark signal is received for 64 bit intervals, proceed to step 9. If PSK data mark signal is not received prior to timeout set in S7, output NO CARRIER to data terminal and abort call.
9. Wait for 700 ms.
10. Turn connection indicator on (28).
11. Turn transmitter mark off (10).
12. Unclamp receive data (22).
13. Turn on carrier detect output.
14. Send CONNECT or CONNECT 1200 message to data terminal.

B. Originating call in low speed (103) mode:

1. Perform steps 1 thru 3 as in A) above.
2. Put SC11015 in low speed mode (2E).
3. Carry out steps 4 thru 6 as in A) above.
4. Go to step 11 in A) above.

C. Answering call (212A–103) mode:

1. Put SC11015 in answer mode (2F).
2. Wait 2.1 seconds (billing timeout).
3. Put SC11015 in low speed mode (2E).
4. Transmit mark (30).
5. Turn transmitter on (25).
6. Sample energy detector output (D0) to see if carrier is present. If carrier is received continuously for 200 ms, proceed to step 7. If timeout set in S7 occurs, output NO CARRIER and abort call.
7. Sample PSK detector output (D2) at twice the bit rate (every 416.66 µs).
8. If continuous PSK data mark is received for 64 bit intervals, prior to one second timeout, proceed to step 9. If continuous FSK data mark is received for 256 bit intervals, proceed to step 10 in A) above. If neither PSK or FSK data mark is received prior to timeout set in S7, output NO CARRIER to data terminal and abort call.
9. Put SC11015 in high speed mode (0E).
10. Go to step 9 in A) above.

D. Originating call in high speed (V.22) mode:

1. Clamp receive data to mark condition (02).
2. Select low speed mode (2E), V.21 mode (39).
3. Turn on calling tone (38) for 0.6 seconds followed by 1.5 seconds of off period until answer tone is detected.
4. Turn off calling tone (18) and V.21 mode (19).
5. Select high speed mode (0E).
6. Wait for unscrambled mark.
7. Wait 456 ms, then proceed to step 4 in A) above.

E. Originating call in low speed (V.21) mode:

1. Perform steps 1 thru 4 as in D) above.
2. Wait for 1 second, then send FSK mark.
3. Wait for carrier to drop. Start a 3 second timer. If carrier drops prior to timeout proceed to step 4. Otherwise proceed to step 4 after timeout.
4. Wait for FSK mark.
5. Turn on connection indicator (28).
6. Turn transmit mark off (10).
7. Unclamp receive data (22).
8. Turn on carrier detect output.
9. Send CONNECT message to terminal.

F. Answering call (CCITT mode) with auto speed detection (V.22/V.21):

1. Select answer mode (2F).
2. Turn scrambler off (32).
3. Wait for 2.1 second billing timeout.
4. Select low speed mode (2E); V.21 mode (39).
5. Turn on 2100 Hz answer tone (37). Start 3.3 second timer.
6. Turn off 2100 Hz answer tone (17) after timeout.
7. Turn transmitter off (05).
8. Wait 60 ms.
9. For next 20 ms look for carrier and continuous FSK mark. If detected, assume low speed and proceed to step 14.
10. Turn transmitter on (25).
11. Select high speed mode (0E). Turn off V.21 mode (19).
12. Turn on 1800 Hz guard tone; (21), (6D).
13. Start 1 second timer. Look for continuous PSK mark for 64 bit intervals over 1 second period. If PSK mark is not detected within 1 second, turn off high speed mode, (select low speed mode), turn off guard tone, turn on V.21 mode and look for continuous FSK mark for 64 bit intervals over the next 1 second period. If FSK mark is not detected, repeat from start. If timeout set in S7 occurs prior to detecting either PSK or FSK mark, output NO CARRIER and abort call. If either PSK or FSK mark is detected, go to step 10 in A).
14. Turn transmitter on (25).
15. Send CONNECT message to terminal.
16. Turn connection indicator on (28).
17. Turn carrier detector on.

G. Requesting remote digital loopback to far end modem:

1. Clamp receive data to mark condition (2).
2. Force transmitter to mark (30).
3. Disable scrambler (32).
4. Wait for 180 ms (send unscrambled mark).
5. Sample PSK detector output (D2) to see if dotting pattern (alternating 1/0 pattern) is received. If dotting pattern is not received within 212 ms, output ERROR to data terminal and return to on line state.
6. Turn scrambler on (12).
7. Wait 270 ms (send scrambled mark).
8. Go to step 11 in A) above.

H. Terminating remote digital loopback:

1. Force transmitter to mark (30).
2. Clamp receive data to mark (2).
3. Turn transmitter off (5).
4. Wait 80 ms.
5. Turn transmitter on (25).
6. Wait 270 ms (send scrambled mark).
7. Go to step 11 in A) above.

I. Response to remote digital loopback request:

1. In on line state monitor unscrambled mark detector output (D3). Go to step 2 if unscrambled mark is detected.
2. Clamp receive data to mark (2).
3. Transmit dotting pattern (34).
4. Wait until unscrambled mark detector turns off.
5. Turn off dotting pattern (14).
6. Put SC11015 in digital loopback (33).
7. Remain in digital loopback until loss of carrier is detected.
8. Terminate digital loopback.
9. Return to on line state.

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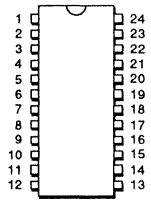
FEATURES

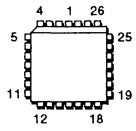
- ☐ All modulators, demodulators and filters with compromise equalizers on chip
- ☐ Call progress mode, tone generators for DTMF, V.22 guard and calling tones
- ☐ Single 5 V power supply with power down by pin or code
- ☐ On-chip hybrid
- ☐ Bell 212A/103 and CCITT V.22/V.21 compatible; V.22 notch filter included
- ☐ Pin programmable receiver gain
- ☐ Serial control interface
- ☐ Programmable audio output port
- ☐ All loopback diagnostics

24-PIN DIP PACKAGE



SC11016CN

28-PIN PLCC PACKAGE



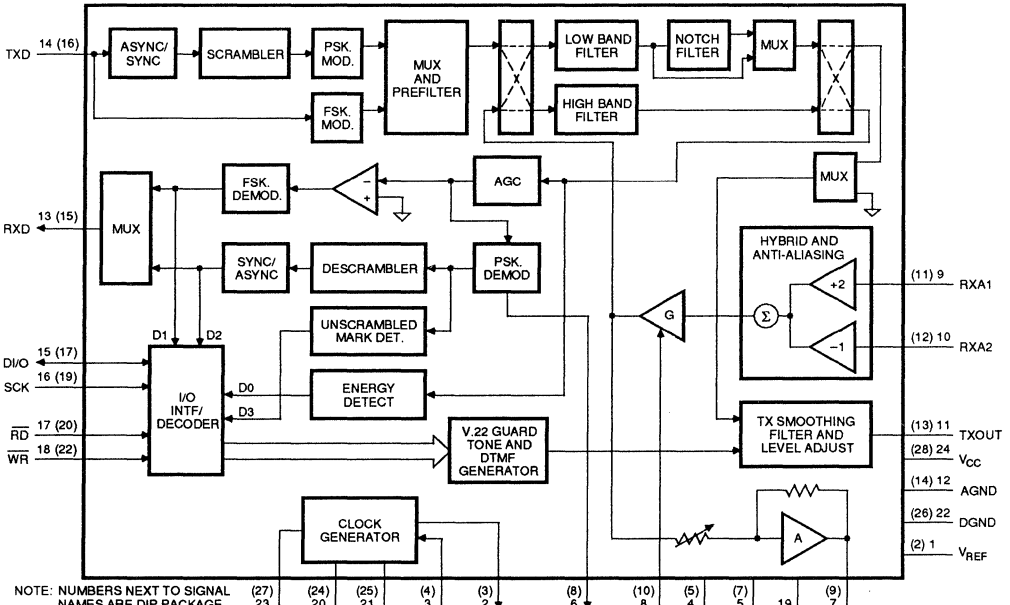
SC11016CV

GENERAL DESCRIPTION

The SC11016 is a complete 300/1200 Bit Per Second modem. All signal processing functions needed for a full duplex, 300/1200 bps 212A/103 or V.22/V.21 modem, including the FSK and PSK modulators and demodulators and the high-band and low-band filters with compromise amplitude and group delay equalizers are integrated on a single chip. Built with Sierra's proprietary CMOS process that allows analog and digital functions to be combined on the same chip, the SC11016 features call progress monitoring and circuits for generating DTMF and V.22 guard tones. A two-to-four wire hybrid with pin programmable receiver gain is also included on-chip simplifying the interface to a DAA. An external hybrid may also be used, if desired. The SC11016 also includes analog, digital and remote digital loopback diagnostics for self-testing. The SC11016 contains all of the features of the SC11015 and, in addition, provides for 5 V operation and offers power down mode controlled by pin or software.

With the addition of a digital controller, such as an 8-bit microcontroller and a data access arrangement (DAA), a highly cost effective, integrated, intelligent modem can be built. When used with the Sierra SC11027/SC11037 modem controller—8-bit processor combined with a UART—a complete Hayes command set compatible modem can be configured, occupying minimum board area. All that is needed for stand-alone applications is the SC11016 modem, the SC11028 controller, a DAA and RS-232 interface. The SC11016 is capable of asynchronous mode and can handle 8, 9 or 10 bit words.

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1 (2)	VREF	Reference ground generated inside the chip and is equal to $V_{CC}/_2$
2 (3)	TXCK0	Transmitter clock output. In high speed, synchronous, internal mode, this output supplies a 1200 Hz clock to the DTE.
3 (4)	TXCK1	In high speed, synchronous, external mode, this pin is an input for receiving a 1200 Hz clock from the DTE.
4 (5) 5 (7)	TEST 1, TEST 2	Used by Sierra for testing. Make no connection to these pins—they MUST be left floating.
6, (8)	RXCK	Receiver clock output. In high speed, synchronous mode, the modem supplies a 1200 Hz clock on this output.
7, (9)	Audio Out	Output of the hybrid is passed through a programmable attenuator and brought out on this pin. 4 levels of received signal can be programmed using the control codes listed in Table 1 (Page 7).
8, (10)	GS	Gain Select. When left open or tied to V_{SS}, the compensation is 0 dB; connected to ground, +2 dB compensation is provided; And when tied to V_{CC}, the compensation is +3 dB.
(1, 6, 18, 21)	NC	No Connect. These pins must be left floating. Do NOT ground these pins or tie them to V_{CC} or GND (In PLCC package)
9 (11) 10 (12)	RXA1, RXA2	Received data carrier
11 (13)	TXOUT	Transmit data carrier output
12 (14)	AGND	0 V
13 (15)	RXD	Receive data. The modem demodulates the received carrier and outputs data on the pin. A logic low level is space and a logic high level is mark. The controller can force the demodulator output to the mark state by sending the code 02.
14 (16)	TXD	Transmit data. Data on this input is modulated by the modem and output on TXOUT pin. A logic low is space and a logic high is mark.
15 (17)	D I/O	Data I/O pin. Data is shifted in serially when $\overline{WR}$ is low on rising edges of SCK clock. Data is transferred to a latch when $\overline{WR}$ goes high. Up to 7 data bits can be sent. Input codes are defined in Table 1. Data is read from the modem serially when $\overline{RD}$ is low, on rising edges of SCK clock. Up to 4 data bits can be read. Output codes are defined in Table 1 (Page 7).
16 (19)	SCK	Serial shift clock is applied to this pin. It is normally high until data is sent to or read from the modem.
17 (20)	$\overline{RD}$	Strobe output from controller for serially reading data from the modem.
18 (22)	$\overline{WR}$	Strobe output from the controller for shifting data to the modem.
19 (23)	PD	Power down. When high, chip will be powered down, but oscillator will keep running. When low, chip will go into normal power mode. (Power down is then controlled by firmware in the SC11027/28/37 microcontroller)
20 (24) 21 (25)	XTAL1, XTAL2	Pins for connecting a 7.3728 MHz crystal. An external CMOS (+5 V) clock signal can be applied to the XTAL1 pin, with XTAL2 left open. If a TTL clock is used, it must be capacitively (100 pF) coupled into XTAL1.
22 (26)	DGND	Digital ground
23 (27)	CKOUT	Buffered crystal oscillator signal is output on this pin. It can drive one LS TTL load.
24 (28)	V_{CC}	+5 V power supply

Numbers in ( ) refer to 28-Pin PLCC Package.

FUNCTIONAL DESCRIPTION OF THE SC11016 MODEM

Major sections of the SC11016 modem are a transmitter, a receiver, low-band and high-band filters, a two-to-four wire hybrid, tone generators and interface logic. It also contains an energy detector that's used for detecting the carrier and call progress monitoring and an audio output for monitoring the line.

The SC11016 modem requires +5 V and is available in a 24-pin DIP as well as a 28-lead plastic chip carrier with 'J' leads for surface mount applications. The transmitter section consists of an async/sync convertor, scrambler, PSK modulator and FSK modulator. In the high speed mode (1200 bps), the PSK modulator is connected to the filter. In the low speed mode (300 bps), the FSK modulator is connected to the filter.

Transmitter

Since data terminal and computers may not have the timing accuracy required for 1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync convertor accepts asynchronous serial data clocked at a rate between 1200 Hz + 1%, – 2.5%. It outputs serial data at a fixed rate of 1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync convertor is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first two stages of the shift register form the dibit that is applied to the PSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band centered at 2400 Hz or the low band, centered at 1200 Hz. A 1200 bps modem actually sends two bits at a time, called a dibit; dibits are sent at 600 baud, the actual rate of transmission; 600 baud is the optimum rate that can be transmitted over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

The dibit applied to the PSK modulator produces one of four differential phase shifts of the square wave carrier signal (1200 Hz or 2400 Hz) at the 600 Hz baud rate. The resultant waveform is passed through a wave shaping circuit that performs a raised cosine function (this is the shape factor called out in the CCITT V.22 spec, and it also meets the Bell 212A requirement for optimum transmission). The wave shaped signal is then passed through either the low-band or high-band filter depending upon originate or answer mode selection.

For low speed operation the FSK modulator is used. It produces one of four precision frequencies depending on orignate or answer mode and the 1 (mark) or 0 (space) level of the transmit data. Different frequencies are used for V.21 and 212A modes. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.22 applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop. In the Call Progress Monitoring mode, the filter response is scaled down by 2.5, moving the center frequency to 480 Hz.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog

loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second order low-pass switched-capacitor filter that adds the modem transmit signal to the DTMF or V.22 guard tones. It also provides a 3 dB per step programmable gain function to set the output level.

Receiver

The receiver section consists of an energy detector, AGC, PSK demodulator, FSK demodulator, descrambler, and sync/async convertor.

The received signal is routed through the appropriate band-pass filter and applied to both the energy detector and AGC circuit. The energy detector is based on a peak detection algorithm. It provides a detection within 17 to 24 ms. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels.

The AGC circuit is a programmable gain amplifier that covers a wide range. Output of the AGC amplifier is rectified and compared with two preset levels corresponding to desired high and low limits. Outputs of the comparators control an up/down counter such that the received signal is amplified to the desired level. Receive signal input range is 0 to –45 dBm measured at the chip.

The PSK demodulator uses a coherent demodulation technique. Output of the AGC amplifier is applied to a dual phase splitter that produces an in-phase and 90 degree out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by the recovered carrier. The baseband components are low-pass filtered to produce I and Q channel outputs. (In phase and Quadrature). The I and Q channel outputs are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. The signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled to produce the received dibit data. The recovered carrier for the demodulator is generated by another PLL which is controlled by the amplitude of the error signal formed by the difference of the I and Q outputs.

The descrambler is similar to the scrambler. The received dibit data is applied to the D input of a 17-bit shift register clocked at 1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with input data to produce received data.

In the asynchronous mode, data from the descrambler is applied to the sync/async convertor to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (over-speed data), these stop bits are reinserted. Underspeed data is passed essentially unchaged. Output of the sync/async convertor along with the output of the FSK demodulator is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed, and outputs received data on the RXD pin.

For low speed operation, the FSK demodulator is used. The output of the AGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, this matching is provided by an external resistor connected between the RXA1 and RXA2 pins on the SC11016. The filter section provides sufficient attenuation of the out of band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass anti-aliasing filter.

Internal Hybrid

The SC11016 internal hybrid, shown in Figure 1, is intended to simplify the phone line interface. In addition, there is a gain select feature to compensate for the loss in the line coupling transformer used in the DAA. By tying this pin to GND, V_{REF}, or V_{CC}, compensation levels of 0, +2 or +3 dB, respectively, are provided.

With a higher loss transformer, some degradation in performance will occur at lower signal levels. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy

detect on/off levels measured at the line will also be different from those specified at the chip.desired at the line.

Tone Generator

The tone generator section consists of a DTMF generator and a V.22 guard tone generator. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and * and # keys. The V.22 guard tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the Data I/O pin. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50 kΩ is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation—no attenuation, 6 dB attenuation, 12 dB attenuation and squelch are provided through the ALC1, ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Crystal Oscillator

The SC11016 includes an inverting amplifier between pins 20 and 21 with an internal bias resistor to simplify the design of the crystal oscillator. The parallel resonant, 7.3728 MHz ±0.001% crystal, designed for a load capacitance of 20 pF, should be connected across pins 20 and 21. Two capacitors of typical values 27 pF from pin 20 to digital ground (DGND pin 22) and 47 pF from pin 21 to DGND should be connected. With the recommended crystal, Saronix, NYMPH, NYP073-20 and these capacitor values, a highly accurate and stable crystal oscillator can be designed. Since the carrier frequency must be within ±0.01% of the normal 1200/2400 Hz, it is important to measure the actual crystal oscillator frequency at CKOUT (pin 23) and adjust the external capacitors for a given circuit board layout, if necessary.

Power Down

A power down Command from the attendant controller is issued to the modem when going "on hook". Power-up occurs with "off-hook" command or ring detection.

FUNCTIONAL DESCRIPTION OF THE SC11027, SC11028 AND SC11037 CONTROLLERS

The SC11027/SC11037 modem controllers, implemented in Sierra's low power CMOS process, were designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including an 8-bit microprocessor, 8k by 8 bytes of ROM and 128 by 8 bytes of RAM. They also contain the equivalent of an 8250B UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem for the PC consists of the SC11027 controller, the SC11016 modem and the DAA. All of the popular communications software written for the PC will work with the SC11016/SC11027 set. Compatibility with high-speed "turbo" PCs require the use of the SC11037 controller RDY output that is to be connected to the IOCHRDY pin of the PC bus (Pin A10).

Another version of the controller, the SC11028, is intended for RS-232 applications. It contains the same processor, memory and UART as the SC11027/SC11037 and has the same interface to the modem chip. The difference is that the UART is turned around so the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The SC11028 provides a standard 5 V logic level interface—RS-232 drivers are required to interface to the port. Like the SC11027, the SC11028 comes preprogrammed with the Hayes 'AT' command set, and when used with the SC11016 modem, emulates a Hayes-type stand-alone modem. All controllers automatically power-down the SC11016 modem when Data Terminal Ready (DTR) is off or when modem is "on-hook".

But the chip set is by no means limited to implementing a Hayes-type smart modem. Sierra is in the custom IC business and both chips were designed with this in mind. For example, only about 6k bytes of the SC11027/SC11037 ROM is used for the handshaking and smart modem code, leaving 2K bytes for additional features that a customer may specify. And since the controller is ROM programmable, any command set, not just the Hayes 'AT' set, can be implemented.

All the SC11027, SC11028 and SC11037 require +5 V and are available in either a 28-pin DIP or a

28-lead plastic chip carrier with 'J' leads for surface mount applications. Besides the four-line interface for the SC11016 modem, the SC11027 controller has a 8-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 8250B UART. It also has control lines for ring indication, the off-hook relay and data/voice relay; these three lines connect to the DAA.

In the SC11028, the 8-bit port becomes the switch input lines and the address, chip select, DIST and DOST lines become the six lines for the RS-232 interface. These six lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control—so the main difference between the SC11027, SC11028, and SC11037 is the ROM code. It also contains the same modem and DAA interface lines as the SC11027/SC11037.

The SC11027, SC11028, and SC11037 are truly ASIC controllers—they are designed to control a modem or other peripheral that operates at a moderately slow rate up to 1200 bits per second. What's unique about the SC11037, for example is that it allows a slow peripheral to interface to a high speed bus, without making the main processor slow down.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11027/SC11037 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like in a Hayes-type modem. The escape sequence is three + signs—+++ —in the default mode, but it can be changed in software.

The actual processor contains an 8-bit data path and can execute 19 instructions with five different addressing modes: direct, indirect, immediate, register direct and register indirect. There is 8K by 8 of ROM on chip for program storage.

To the system bus, the SC11027/SC11037 looks and acts just like an 8250B UART. Communications software written for this UART will work with the SC11027, SC11028 and SC11037. The Sierra chip set is truly a Hayes-type modem in two chips.

THE SC11016 & SC11027/SC11028/SC11037 SYSTEM—REFER TO APPLICATIONS INFORMATIONS FIGURES 4, 5 AND 6.

The only external components required by the SC11016 are the 600 Ω line matching resistor, a 7.3728 MHz crystal—a standard frequency—and a 20 pF capacitor from each leg of the crystal to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11016 can directly drive a high impedance (50 kΩ) earphone-type transducer.

The SC11027/SC11037 modem controller's clock in line is driven by the SC11016's clock out line, so only one crystal is needed. The SC11027 interfaces directly to an IBM PC bus—no buffers are required. The only external parts may be a 8 input NAND gate for COM1 and COM2 decoding inside the PC.

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

All modems require a DAA. A DAA or data access arrangement is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω; a relay for disconnecting the modem from the line; a ring detector, typically an optoisolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by any of many consultants and labs around the country. The fee is typically $2,000 and it takes several months. Another alternative is to buy a DAA, supplied by several manufacturers.

212A is a Bell specification that calls for 1200 bit per second, full or half duplex data transmission with a fallback mode of 300 baud (Bell 103). It is not 1200 baud; the spec calls for transmission of dibits—2 bits per baud so the 1200 bps transmission takes place at 600 baud. The same is true for V.22—it's 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; there is a CCITT standard for 300 and that's V.21.

V.22 also calls for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The SC11016 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone when in the receive mode.

All modems require a Hybrid. Hybrid is a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the SC11016, this is done with op amps, but the separate signals—TXOUT and RXA2—are also brought out so an external hybrid can be used, if desired. The combined signal comes out on the RXA1 pin and matching resistor—typically 600 Ω — is connected between RXA1 and RXA2.

SC11016 SPECIFICATIONS

Table 1. Definition of I/O Codes

1. Instructions to the modem IC (See Note 1 and 2). Data on the DI/O pin shifted into the modem when $\overline{WR}$ is low, on rising edges of the SCK clock. Data is transferred into a latch when $\overline{WR}$ goes high. (See Figure 2 for write cycle waveforms). Up to 7 data bits (D0–D6) can be sent to the device. These bits control the operating modes of the modem as shown below:

D6	D5	D4	D3–D0	HEX CODE	MODE/FUNCTION
Non tone mode:					
0	1/0	0	0	20/00	Reset (set default values)
0	1/0	0	1	21/01	Tone On/Off (tone mode enable/disable)
0	1/0	0	2	22/02	Force Receive Data to Mark Off/On (forces RXD pin High if On)
0	1/0	0	3	23/03	TLC0 Transmit Level Control bit 0 (default 0)
0	1/0	0	4	24/04	TLC1 Transmit Level Control bit 1 (default 0)
0	1/0	0	5	25/05	TX Transmitter On/Off (if Off, TXOUT is grounded)
0	1/0	0	6	26/06	ALB Analog Loopback On/Off
0	1/0	0	7	27/07	CPM Call Progress Monitor mode On/Off
0	1/0	0	8	28/08	Connection Indicator (CI) On/Off (see note 4 below)
0	1/0	0	9	29/09	ALC0 Audio Output Level Control bit 0 (default 0)
0	1/0	0	A	2A/0A	ALC1 Audio Output Level Control bit 1 (default 0)
0	1/0	0	B	2B/0B	WLS0 Word Length Select 0 (default 0)
0	1/0	0	C	2C/0C	WLS1 Word Length Select 1 (default 1)
0	1/0	0	D	2D/0D	Sync/Async
0	1/0	0	E	2E/0E	LS/HS: Low Speed/High Speed (FSK/PSK)
0	1/0	0	F	2F/0F	A/O: Answer/Originate
0	1/0	1	0	30/10	Transmit Mark On/Off
0	1/0	1	1	31/11	Transmit Space On/Off
0	1/0	1	2	32/12	Scrambler Off/On
0	1/0	1	3	33/13	DLB Digital Loopback On/Off (also sets Synchronous, Slave Mode)
0	1/0	1	4	34/14	TXDP Transit Dotting Pattern On/Off (Not valid for V.21 mode)
0	1/0	1	5	35/15	Sync Mode Transmit Timing Locked/Free Running
0	1/0	1	6	36/16	Sync Mode Transmit Timing Source External/Slave
0	1/0	1	7	37/17	2100 Hz tone On/Off. Must select low speed mode for operation.
0	2/0	1	8	38/18	1300 Hz tone On/Off. Must select low speed mode for operation.
0	1/0	1	9	39/19	V.21 mode. Must select low speed mode for operation.
0	1	1	A	3A	Power Down. To power up chip must be reset.

D6	D5	D4	D3–D0	HEX CODE	MODE/FUNCTION
Tone mode:					
1	1/0	0	0	60/40	Dial 0
1	1/0	0	1	61/41	Dial 1
1	1/0	0	2	62/42	Dial 2
1	1/0	0	3	63/43	Dial 3
1	1/0	0	4	64/44	Dial 4
1	1/0	0	5	65/45	Dial 5
1	1/0	0	6	66/46	Dial 6
1	1/0	0	7	67/47	Dial 7
1	1/0	0	8	68/48	Dial 8
1	1/0	0	9	69/49	Dial 9
1	1/0	0	A	6A/4A	Dial *
1	1/0	0	B	6B/4B	Dial #
1	1/0	0	C	6C/4C	Output 550 Hz and insert 550 Hz notch in low-band filter
1	1/0	0	D	6D/4D	Output 1800 Hz and insert 1800 Hz notch in low-band filter
1	1/0	0	E	6E/4E	Row disable On/Off (For DTMF test only)
1	1/0	0	F	6F/4F	Column disable On/Off (For DTMF test only)

WLS1	WLS0	Word Length
0	0	8 bits
0	1	9 bits
1	0	10 bits (default)
1	1	11 bits

TLC1	TLC0	Transmitter Output Level (dBm) (Note 3).
0	0	–8
0	1	–6
1	0	–4 (default)
1	1	–2

ALC1	ALC0	Audio Output Level
0	0	Output Off (default)
0	1	12 dB attenuation
1	0	6 dB attenuation
1	1	No attenuation

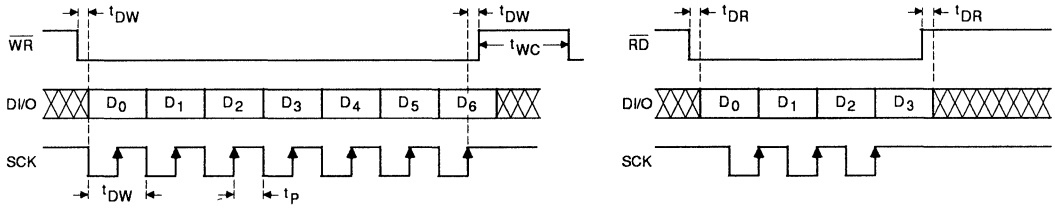
Notes: 1. Default values for the operating modes on power up are those shown to the right of the '/' unless otherwise specified.
2. Data is shifted in and out of the modem with LSB first.
3. Using the internal hybrid and a 600 Ω resistor, these levels will be 6 dB lower at the input to the transformer.
4. After a connection is established, turn CI on to disable unnecessary functions, i.e. if a PSK connection is established, turning CI on will turn off the FSK demodulator.

2. Information from the modem IC. Data is read serially from the modem when $\overline{RD}$ is low, on rising edges of the SCK clock. (See Figure 3 for read cycle waveforms). Up to 4 data bits (D0–D3) can be read as defined below:

D0 Energy Detect 0—no energy 1—energy present

In the CPM mode, the energy detector is connected to the output of the high band filter, if ALB is off, or the scaled low band filter, if ALB is on.

D1	Received data (FSK)	1—Mark	0—Space
D2	Received data (PSK)	1—Mark	0—Space
D3	Unscrambled Mark	1—Detected	0—Not Detected



t_{WC} = 4 µsec
t_{DW} = 200 nsec Min.
t_{PW} = 1 µsec Min.
t_P = 30% to 70% duty cycle
t_{DR} = 200 nsec Min.

Figure 2. Waveforms for Write and Read Cycles

Modem Interface — The 4 line serial interface consists of a bidirectional data pin (DI/O), a write control pin ($\overline{WR}$), a read control pin ($\overline{RD}$) and a clock pin (SCK). In the inactive state, $\overline{WR}$, $\overline{RD}$ and SCK lines must be held in the high state. The read and write functions are controlled only by the mircocomputer. To write data into the SC11016 (see timing waveforms of Figure 2), the controller must first make the $\overline{WR}$ line low. The least significant bit D0 of the data is then placed on the DI/O line. The SCK line is then toggled low and then high to shift the data bit into the SC11016 input register. Data is shifted into the input register on the rising edge of SCK.

There is no special requirement on the duty cycle of the clock signal. The minimum pulse width and data setup times specified in the specifications table must be met. The remaining data bits D1 thru D6 are shifted by repeating the above procedure. Only 7 data bits should be sent. If an 8th data bit is sent, the first data bit D0 will be lost from the input register. The received data will then be D7–D1 rather than D6–D0. To read data from the SC11016 (see timing waveforms of Figure 3), the $\overline{RD}$ line is first made low. The least significant bit D0 is now available on the DI/O line. The SCK line is toggled low and then high to shift the next data bit out of the SC11016 output register. The SC11016 shifts the data out on the rising edges of SCK. The controller should read data on the falling edges of SCK when it will be stable. Note that D0 appears on the DI/O line as soon as $\overline{RD}$ is taken low. If the controller only wants to read the status of the energy detector, there is no need to toggle SCK line. By making $\overline{RD}$ low, the energy detector level can be read by reading DI/O. $\overline{RD}$ can then be taken high. Read operation is terminated by making the $\overline{RD}$ line high. If more than 4 bits are read, the additional bits are returned as 0's.

In the READ mode, the values of D0, D1, D2 and D3 do not change as long as $\overline{RD}$ is low, even though the chip status may be changing. To read out the updated values of these bits, $\overline{RD}$ must be pulled high for at least 1 ms and then taken low again to initiate another read cycle.

The read and write operations can be performed by two simple I/O drivers shown in Table 2. The RDMO–DEM subroutine reads data from the SC11016 and places it in the accumulator with the high nibble set to zero. The WTMODEM subroutine sends data placed in the accumulator to the SC11016. Both subroutines use register R7 in bank 1 as a data bit counter.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1 — SC11016 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 3.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11016 in the synchronous mode (2D). This provides a 1200 Hz clock on the TXCK0 Pin that can be used as a clock source for the DTE to synchronize its TXD to. The Transmit Phase-Locked-Loop (TX PLL) of the SC11016 will be in free-runing mode. As a result, External/Slave input codes will be ignored by the chip.

Case 2 — SC11016 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode (2D), also select "Locked" (35) and "External" (36) modes.

The TX PLL of SC11016 will then synchronize itself to the clock provided on its "TXCK1" pin.

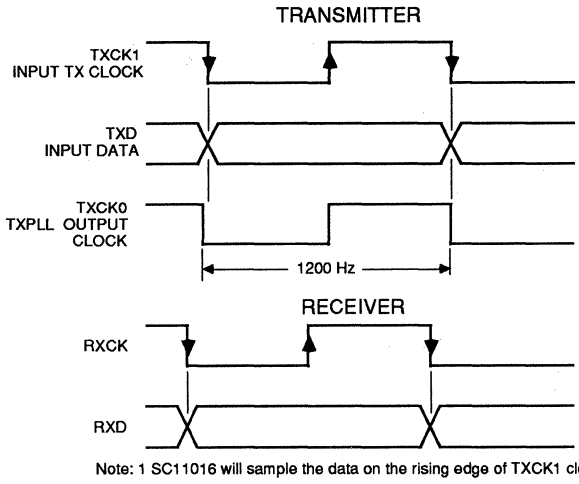
Receiver Timing

In synchronous mode, the recovered clock will be provided on the RXCK pin and the transitions of RXD will be on the falling edges of this clock.

SYNCHRONOUS MODE CHART

Transmitter Timing

Locked (35)	External (36)	TX PLL locks to clock provided on TXCK1
	Slave (16)	TX PLL locks to receiver timing. Should be used in DLB mode only.
Free Running (15)	External/Slave	TXPLL is free running and ignores External or Slave inputs.



Note: 1 SC11016 will sample the data on the rising edge of TXCK1 clock.

Figure 3. SC11016 Synchronous Mode Diagrams

Absolute Maximum Ratings (Notes 1, 2 and 3)

Supply Voltage, V_{CC}–GND	+7 V
DC Input Voltage (Analog Signals)	AGND–0.6 to V_{CC}+0.6 V
DC Input Voltage (Digital Signals)	DGND–0.6 to V_{CC}+0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 s)	300°C

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating — Plastic Package: –12 mW/C from 65°C to 85°C.

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
DGND, AGND	Ground			0		V
F_C	Crystal Frequency		7.3721	7.3728	7.3735	MHz
T_R, T_F	Input Rise or Fall Time	(Note 4)			500	ns

Notes: 4. Does not apply to CKOUT.

DC Electrical Chracteristics (Note 5)

PARAM.	DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current Power Down Current	V_{CC} = 5 V			12 3.5		mA mA
V_{IH}	High Level Input Voltage	Digital Signal Pins $\overline{RD}$, $\overline{WR}$, D I/O, SCK, TXCK1, TXD		2.0			V
V_{IL}	Low Level Input Voltage	Digital Signal Pins $\overline{RD}$, $\overline{WR}$, D I/O, SCK, TXCK1, TXD				0.8	V
V_{OH}	High Level Input Voltage	Digital Signal Pins D I/O, RXD, TXCK0, RXCK	I_{OH} = 40 µA	4.0			V
			I_{OH} = 500 µA	2.0			V
V_{OL}	Low Level Input Voltage	Digital Signal Pins D I/O, RXD, TXCK0, RXCK	I_{OL} = 1.6 mA		0.4	0.6	V
V_{OM}	Maximum Output Signal	TXOUT, RL = 1200 Ω (TLC = 1, TLC0 = 0)		3.0			V_{P-P}
V_{IM}	Maximum Input Signal	RXA1 (Using Internal Hybrid) RXA2				2.5 3.0	V_{P-P} V_{P-P}
V_{IM}	Maximum Receive Signal	RXA1 Receive Component RXA2 of Line Signal				1.5 2.0	V_{P-P} V_{P-P}

Note 5. Min and max values are valid over the full temperature and operating voltage range. Typical values are from 25°C and ±5 V operation.

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQ.	ALLOWABLE ERROR	ACTUAL ERROR
Row 1	697 Hz	±1%	+0.17%
Row 2	770 Hz	±1%	–0.26%
Row 3	852 Hz	±1%	+0.16%
Row 4	941 Hz	±1%	–0.47%
Column 1	1209 Hz	±1%	–0.74%
Column 2	1336 Hz	±1%	–0.89%
Column 3	1477 Hz	±1%	–0.01%
Guard Tones	550 Hz	±20 Hz	–1.4 Hz
	1800 Hz	±20 Hz	+7 Hz

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion			–40		dB
Row Output Level	V_{CC} = +5 V TLC0 = 1 TLC1 = 1 Measured at TXOUT Pin		–2		dBm
Column Output Level			0		dBm
550 Hz Guard Tone			–3		dB (Note 2)
1800 Hz Guard Tone			–6		dB (Note 2)

Notes: 1. This assumes a crystal of exactly 7.372800 MHz.
2. These levels are referenced to the TX signal level. When guard tones are added, the TXOUT level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

Modem Transmit Signals—Hz (Assume 7.372800 MHz Crystal)

MODE		BELL 103		CCITT V.21		212A/V.22	
		NOMINAL	ACTUAL	NOMINAL	ACTUAL	NOMINAL	ACTUAL
Answer	Mark	2225	2226	1650	1649.4	2400	2400
	Space	2025	2024.4	1850	1850.6		
Originate	Mark	1270	1269.4	980	978.34	1200	1200
	Space	1070	1070.4	1180	1181.53		
Calling Tone				1300	1301.7	1300	1301.7
Answer Tone				2100	2096.9	2100	2096.9

Transmitter

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Character Length	Start Bit + Data Bit + Stop Bit	8		11	bits
Intra-Character Bit Rate	AT TXD (Pin 14)	1170	1200	1212	bps
Input Break Sequence Length	M = Character Length	2M + 3			bits
Output Level Tolerance			±1		dB

Receiver

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Signal Range	AT RXA1	–45		–8	dBm
Intra-Character Bit Rate	AT RXD (Pin 13)	1170	1200	1224	bps
Carrier Detect	AT RXA1 (Pin 9)	–48		–43	dBm
Carrier Detect Hysteresis		2			dB
Carrier Detect Delay	For 103, 212A and V.22	10	20	30	ms
Carrier Detect Hold	For 103, 212A and V.22	15	20	24	ms
Carrier Detect Delay	For V.21 Mode	15	30	40	ms
Carrier Detect Hold	For V.21 Mode	20	30	50	ms

APPLICATIONS INFORMATION

Why a Modem/What's a Modem

The voice frequency channels of the general switched telephone network have been used extensively for the transmission of digital data. To use these channels, the data must be put in a form that can be sent over a limited bandwidth line. In voice grade telephone networks, transformers, carrier systems and loaded lines attenuate all signals below 300 Hz and above 3400 Hz.

While the bandwidth from 300 Hz to 3400 Hz is fine for voice transmission, it is not suitable for the transmission of digital data because the data has many frequency components outside this range. To transmit data over phone lines, it is necessary to convert the digital data into a signal that is totally within the voice frequency range. This conversion is performed by a MODEM (MODulator DEModulator).

In full duplex data transmission—the simultaneous sending and receiving of data—Frequency Division Multiplexing (FDM) can be used for data rates up to 2400 bits per second. In FDM, the voice channel is divided into upper and lower bands (called the high band and the low band); one is used for sending and the other for receiving data. The originating terminal transmits in the low band and receives in the high band, while the answering terminal transmits in the high band and receives in the low band.

In low speed modems (300 bit per second transmission rate), the modulation technique commonly employed is called Frequency Shift Keying (FSK). In FSK modems, four separate frequencies are used; 1070 Hz for a zero (also called a space) in the low band, 1270 Hz for a one (a mark) in the low band, 2025 Hz for a zero in the high band and 2225 Hz for a one in the high band. The transmitting modem takes the digital ones and zeros from the terminal and converts them into the proper tones which are then sent over the phone line. The receiving modem takes the tones and converts them back to ones and zeros and sends them to the receiving terminal. Since four frequencies are used, simultaneous transmitting and receiving of data can be accomplished.

Because of the limited bandwidth of the phone line, FSK modems only work up to 600 bits per second for full duplex transmission. This is due to the fact that when the modem shifts between the two frequencies (for mark and space) it generates a frequency spectrum (it is a type of FM—frequency modulation—transmission). The faster the data rate, the wider the spectrum. The limit for full duplex FSK transmission is 600 bits per second, before the available audio spectrum is used up—allowing for enough separation between the frequency bands to reliably decode or demodulate the data. There are 1200 bps FSK modems, but these are half duplex—they can only send OR receive data at 1200 bps.

In higher speed, full duplex modems (1200 bit per second transmission rate) a different modulation technique is employed. Called PSK (for Phase Shift Keying), this technique uses one carrier frequency for the high band—2400 Hz—and one for the low band—1200 Hz—for sending and receiving data. For each carrier frequency (one for transmitting and one for receiving), one of four phase angles is used: 0, 90, 180, or 270 degrees. The data is sent two bits at a time, or in dibits. Since there are four ways to send two bits at a time—00, 01, 10 or 11—each of the four phases represents one unique dibit. While the data rate is 1200 bits per second, the baud rate (the rate at which information packets are sent) is 600 because two bits (dibits) are sent in each packet. Again, 600 packets per second (600 baud and, in this case, 1200 bps) is the limit for transmitting full duplex data over the general switched telephone network using FDM.

Call Progress Monitor Operation

The modem controller uses the high-band and low-band filters in the SC11016 for call progress monitoring. When the SC11016 is put in the CPM and originate mode, the ALB mode provides a means of connecting either the high-band filter (ALB = 0) or the scaled low-band filter (290–660 Hz) (ALB = 1) to the energy detector. Output of the energy detector is monitored by reading bit D0 for detection of call progress or voice/answer information, using the duration and repetition rate as the criteria for detection.

A typical call establishment sequence is as follows:

Dial tone detection— The controller puts the SC11016 in the Originate, CPM mode with ALB = 1 and operates the off-hook relay in the DAA by making the OH output high. After a short delay (typically 300 ms), it monitors the output of the energy detector (ED). If the output is continuously high for at least 1 second; it is recognized as a valid dial tone. If the output is not continuous then the controller continues to monitor until a timeout occurs (typically 5 seconds). If a dial tone is not detected within this timeout, the controller returns a 'NO DIAL TONE' (if X4 mode has been selected) message to the DTE

and aborts the call. If a dial tone is detected, it proceeds to dial the number as follows.

Dialing—The controller will use the specified format (tone or pulse).

If a pause is required in the dialing sequence for a second dial tone, then after dialing is done, the controller will wait for approximately 2.5 seconds and then start to monitor the ED output by alternately toggling the ALB mode at a rate of approximately 100 ms. This allows detection of ringback/busy call progress tones or voice/answer tone. The toggling rate is based on the settling times of the filters as well as the response time of the ED. Once energy is detected at the output of the ED, the controller will maintain the selected ALB mode until detection is made. The criteria for various detections are described below.

Busy tone detection—If the number of transitions of the ED output exceeds 7 over the 5 second window when looking for ringback tone, it will be assumed to be a busy signal. The controller will then abort the call and return a 'BUSY' message to the DTE (in the X4 mode).

Answer tone detection—If the output of the high-band filter is continously high for at least 2 seconds, the controller will assume it to be an answer tone from the distant modem, then returns a 'CONNECT' message and proceeds with handshaking sequence necessary to establish a data call.

If tone or answer within the time specified in S7, the controller hangs up and returns 'NO CONNECT' message.

Silence detection—If the cumulative duration of ED over the 5 second window is less than 0.7 second, once the window is started, it is recognized as silence. The controller then returns a 'NO ANSWER' message to the DTE and aborts the call.

Specific Applications

The SC11016 modem performs all the signal processing functions required in a 212A/V.22 modem. Like all modems, it requires an external controller to implement the handshaking protocols and control functions. The controller's task is simplified by the use of a 4 line serial interface as opposed to a multiline parallel interface. In particular, only I/O pins are used on a single chip microcomputer. More pins are then available for other interfaces such as DAA, RS-232, switches and lights. In most modem applications this will eliminate the need for external latches and buffers for additional I/O pins.

Figure 4 shows the SC11016 modem IC used with the SC11027 controller to make a complete parallel bus Hayes-type smart modem.

Figure 5 shows the SC11016 modem IC used with the SC11028 controller to make a complete RS-232 serial interface Hayes-type smart modem.

Figure 6 shows the schematic of a stand-alone smart modem implemented with the SC11016 and the 8031—the ROMless version of the 8051 microcomputer. Even though 16-port I/O pins are used up on the 8031 for interfacing with the external ROM, enough pins are still available for the other interfaces because of the serial interface used on the SC11016. The 8031 microcomputer was selected because of its wide use in current stand-alone and integrated smart modems.

Oscillator—The SC11016 includes an inverting amplifier and a bias resistor so that a crystal oscillator can be designed by connecting a 7.3728 MHz crystal and two capacitors (27 pF and 47 pF) to XTAL1 and XTAL2 pins as shown in the schematic. A buffered TTL compatible clock output is available on the CLOCK OUT pin to drive the microcomputer.

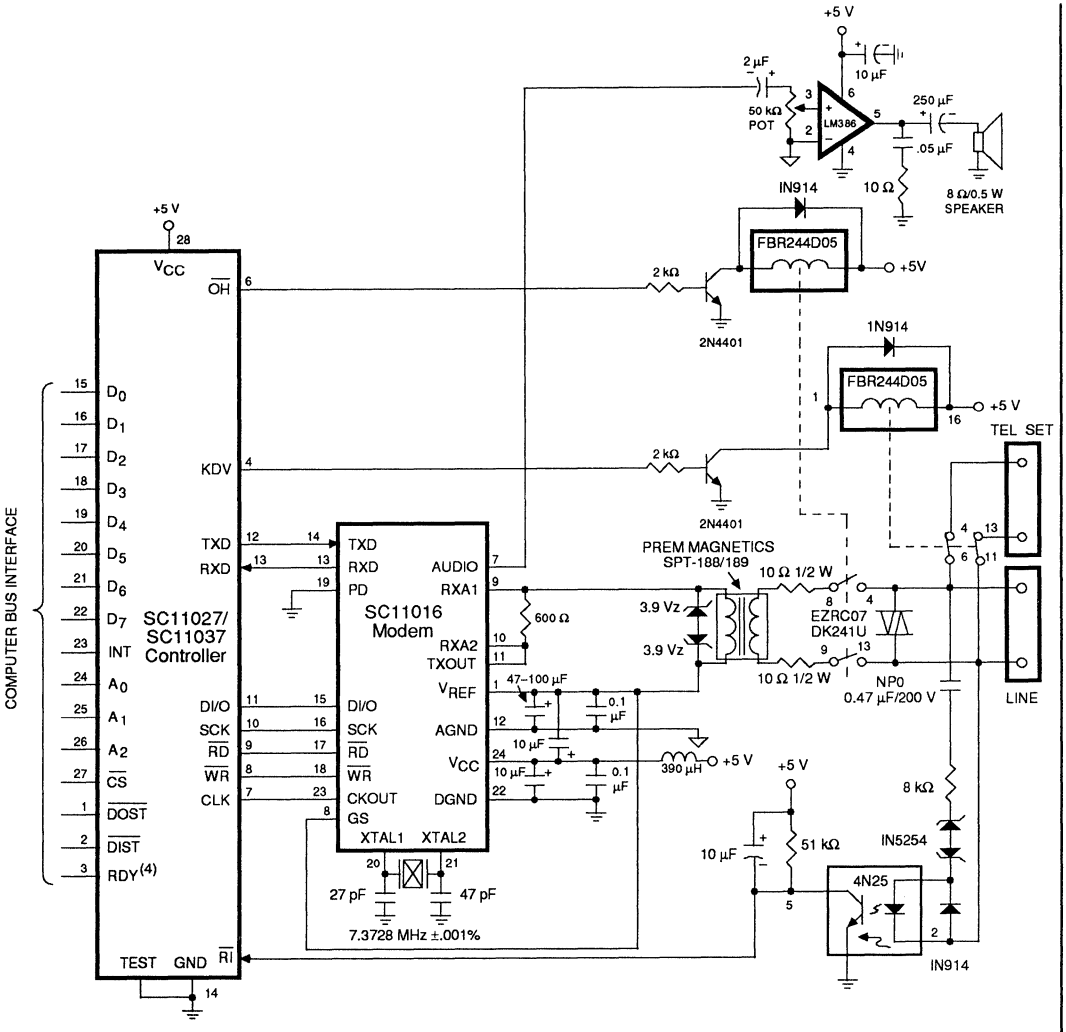


Figure 4. Internal 212A/V.22 Smart Modem Using the SC11016 Modem IC and the SC11027/37 Controller

Notes:
1. Connecting GS (pin 8) to V_{REF} compensates for 2 dB loss in the coupling transformer.
2. Analog ground (⏚) and digital ground (⏚) should be routed separately and connected together at the common point of the power supply for best performance.
3. Power supply decoupling capacitors (47 µF and 10 µF) should be tantalum type.
4. SC11037 only connect RDY line of SC11037 to IOCHRDY pin (A10) of PC bus.

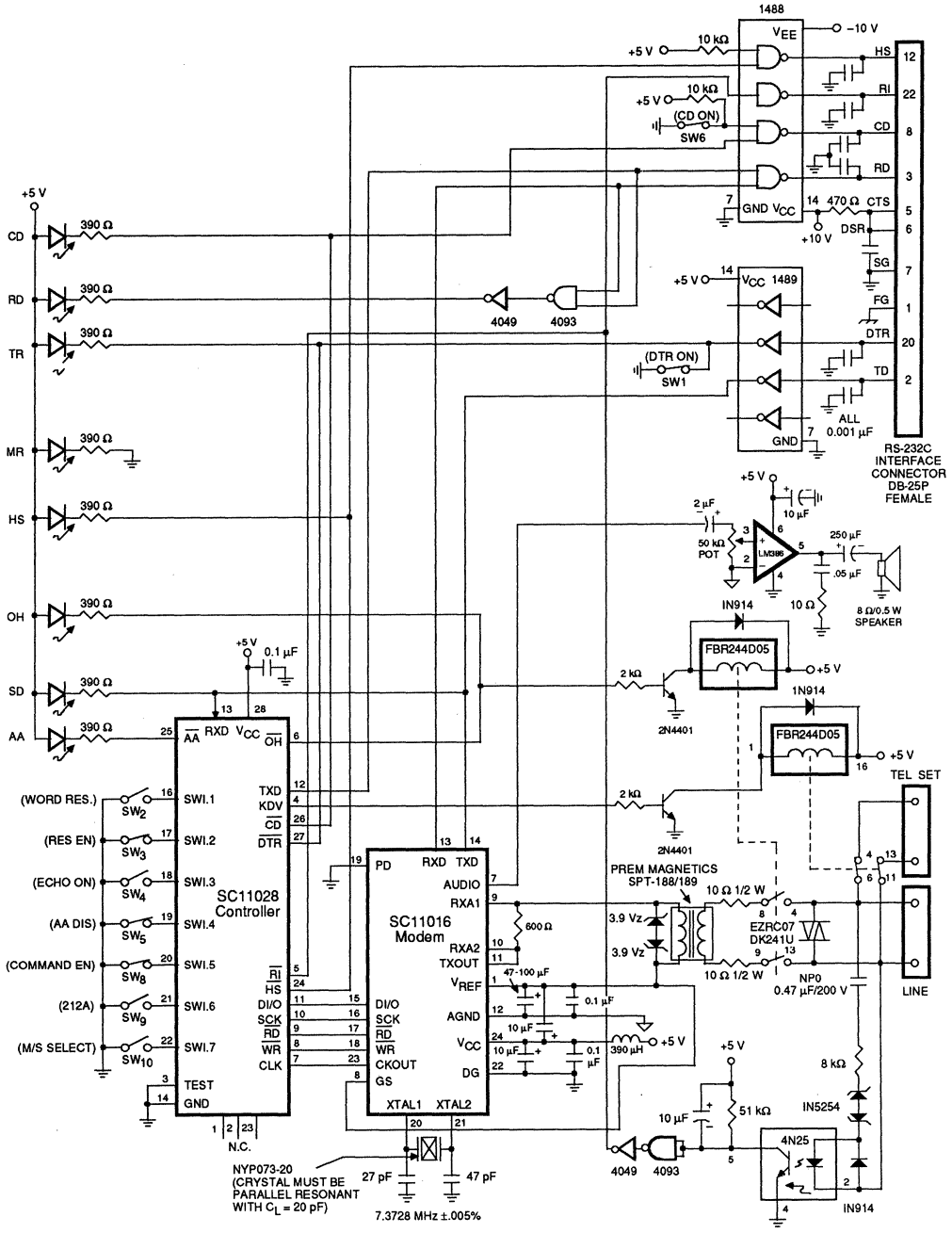


Figure 5. 212A/V.22 Stand-Alone Intelligent Modem Using the SC11016 Modem IC and the SC11028 Controller

Notes:
1. Connecting GS (pin 8) to V_{REF} compensates for 2 dB loss in the coupling transformer.
2. Analog ground (⏚) and digital ground (⏚) should be routed separately and connected together at the common point of the power supply for best performance.
3. Power supply decoupling capacitors (47 µF and 10 µF) should be tantalum type.

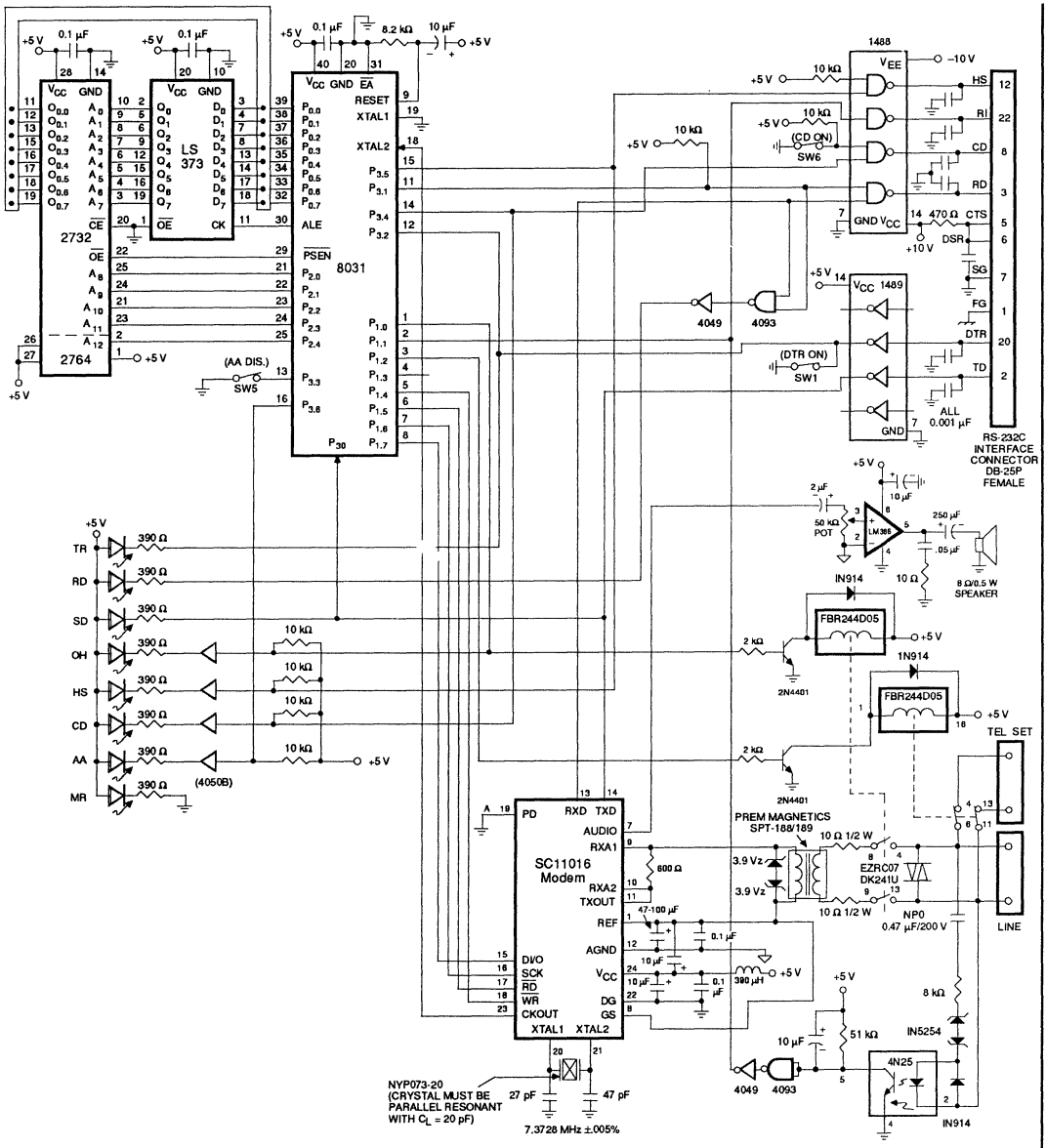


Figure 6. 212A/V.22 Stand-Alone Smart Modem Using the 8031 Controller with SC11016 Modem

Notes:
1. Connecting GS (pin 8) to V_{REF} compensates for 2 dB loss in the coupling transformer.
2. Analog ground (⏚) and digital ground (⏚) should be routed separately and connected together at the common point of the power supply for best performance.
3. Power supply decoupling capacitors (47 µF and 10 µF) should be tantalum type.

Power Supply Decoupling and Circuit Layout Considerations

For optimum performance and to obtain the best possible performance at low received signal levels with low S/N ratio, it is important to use the recommended power supply decoupling circuit as shown in Figures 4, 5, and 6. A small inductor in series with the positive supply helps suppress RFI as well as improve the power supply noise rejection capability of the SC11016 when used with the decoupling capacitors. The 10 µF capacitors should be tantalum type while the 0.1 µF capacitors should have a good high frequency rejection characteristic, monolithic ceramic types are recommended.

It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11016 as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply.

```
WTMODEM:    CLR     P1.4        ;WR → 0; Initiate Write Cycle
            SETB    RS0         ;Select Bank 1
            MOV     R7, #7      ;Set Data Bit Counter to 7

OUTNEXT:    RRC     A           ;Bit → Carry
            CLR     P1.6        ;Toggle Clock Line Low
            JC      SETPB       ;Set/Clear DI/O Line on Carry
            CLR     P1.7
            LJMP    OUTPUT

SETPB:      SETB    P1.7

OUTPUT:     SETB    P1.6        ;Toggle Clock Line High
            DJNZ    R7, OUTNEXT ;Loop Till Data Bit Counter is Zero
            SETB    P1.7        ;Return to Initial Condition
            SETB    P1.4
            CLR     RS0
            RET

RDMODEM:    CLR     P1.5        ;RD → 0 ; Initiate Read Cycle
            SETB    RS0
            MOV     R7, #8

INNEXT:     CLR     P1.6
            MOV     C, P1.7     ;Data Bit → Carry
            RRC     A           ;And into Accumulator
            SETB    P1.6
            DJNZ    R7, INNEXT  ;Loop Till Data Bit Counter is Zero
            SETB    P1.5        ;Return to Initial Condition
            CLR     RS0
            RET
```

To dial a digit, the sequence shown below can be used. It is assumed that register R2 holds the digit to be dialed and memory location S11 holds the on/off duration of the tines in milliseconds.

```
TDIAL:      MOV     A, #21H     ;Turn on Tone Mode
            LCALL   WTMODEM
            MOV     A, R2       ;Read Digit
            ORL     A, #60H     ;Form Digit On Command
            LCALL   WTMODEM
            MOV     A, S11
            MOV     B, #10
            DIV     AB          ;Find Number of 10 ms Increments
            MOV     R1, A       ;Save It
            LCALL   DLOOP       ;Wait 10 ms Times Number in R1
            MOV     R1, A       ;Restore R1
            MOV     A, R2       ;Form Digit Off Command
            ORL     A, #40H
            LCALL   WTMODEM
            LCALL   DLOOP       ;Wait 10 ms Times Number in R1
            LJMP    NEXTDG      ;Go for Next Digit
```

Table 2. Serial I/O Driver Routines

In the following examples it is assumed that the clock frequency for the 8031 is 7.3728 MHz and that timer 0 is set in the auto-reload mode cycling at the rate of 416.66 µs. References are also made to certain registers used in Hayes compatible smart modems.

Initialization—The SC11016 does not have a power on reset circuit. The controller must put the device into the proper operating mode on power turn on. By sending a reset code, the device will enter a default mode as follows: high speed, asynchronous, originate, transmitter off, RX data clamped to mark, transmit level ≡ –12 dBm, audio off and scrambler on. This mode is set up by the following lines of code:

```
MOV     A, #0          ;Reset Code
LCALL   WTMODEM        ;Write It
```

The reset code will lso power up the SC11016. To power it down, send the hex code 3A. The controller should keep the SC11016 in power down mode in the idle condition; i.e., when the modem is on hook or when DTR is off. The controller should wait about 1.25 ms after applying the reset code, to allow the modem to power up.

Dialing—The SC11016 includes an on chip DTMF dialer. It is necessary to adjust the transmit level during dialing since the tone level is internally set to be 6 dB below the transmitted carrier level. The following lines of code will set the tone level at the line to be –6 dBm for low group and –4 dBm for the high group tone:

```
MOV     A, #23H        ;TLC0 = 1
LCALL   WTMODEM
MOV     A, #24H        ;TLC1 = 1
LCALL   WTMODEM
```

Call Progress Monitoring—The progress tones can be monitored readily by activating the call progress monitor (code = 27H) and analog loopback (code = 26H) modes. The low band filter is then scaled down by a factor of 2.5 to center over the frequency range of 300 Hz to 660 Hz. Output of the energy detector monitored on the D0 bit then provides the necessary cadence information for detection of various call progress conditions. For example, dialtone is detected if the energy detector output is continuously high for at least 1 second. Busy line condition is recognized if the number of transitions of the energy detector output exceeds 7 over a period of 5 seconds and if the cumulative on duration exceeds 2 seconds.

Handshaking Sequences—Sequences necessary for establishing calls in various operating modes are provided in the following paragraphs. Numbers in parentheses indicate the hex code values sent to the SC11016 to implement that function of data bit received from the SC11016 for monitoring a given function.

A. Originating call in high speed (212A) mode:

1. Clamp receive data to mark condition (2)
2. Sample energy detector output (D0) to see if answer tone is present.
3. If continuous answer tone is detected for time set in register S9 (typically 600 ms) prior to timeout set in register S7 (typically 30 s) proceed with handshaking. Otherwise output NO CARRIER to data terminal and abort call.
4. Transmit mark (30).
5. Turn transmitter on (25).
6. Wiat for 300 ms.
7. Sample PSK data output (D2) at twice the bit rate (every 416.66 µs).
8. If continuous PSK data mark signal is received for 64 bit intervals, proceed to step 9. If PSK data mark signal is not received prior to timeout set in S7, output NO CARRIER to data terminal and abort call.
9. Wait for 700 ms.
10. Turn connection indicator on (28).
11. Turn transmitter mark off (10).
12. Unclamp receive data (22).
13. Turn on carrier detect output.
14. Send CONNECT or CONNECT 1200 message to data terminal.

B. Originating call in low speed (103) mode:

1. Perform steps 1 thru 3 as in A) above.
2. Put SC11016 in low speed mode (2E).
3. Carry out steps 4 thru 6 as in A) above.
4. Go to step 11 in A) above.

C. Answering call (212A–103) mode:

1. Put SC11016 in answer mode (2F).
2. Wait 2.1 seconds (billing timeout).
3. Put SC11016 in low speed mode (2E).
4. Transmit mark (30).
5. Turn transmitter on (25).
6. Sample energy detector output (D0) to see if carrier is present. If carrier is received continuously for 200 ms, proceed to step 7. If timeout set in S7 occurs, output NO CARRIER and abort call.
7. Sample PSK detector output (D2) at twice the bit rate (every 416.66 µs).
8. If continuous PSK data mark is received for 64 bit intervals, prior to one second timeout, proceed to step 9. If continuous FSK data mark is received for 256 bit intervals, proceed to step 10 in A) above. If neither PSK or FSK data mark is received prior to timeout set in S7, output NO CARRIER to data terminal and abort call.
9. Put SC11016 in high speed mode (0E).
10. Go to step 9 in A) above.

D. Originating call in high speed (V.22) mode:

1. Clamp receive data to mark condition (02).
2. Select low speed mode (2E), V.21 mode (39).
3. Turn on calling tone (38) for 0.6 seconds followed by 1.5 seconds of off period until answer tone is detected.
4. Turn off calling tone (18) and V.21 mode (19).
5. Select high speed mode (0E).
6. Wait for unscrambled mark.
7. Wait 456 ms, then proceed to step 4 in A) above.

E. Originating call in low speed (V.21) mode:

1. Perform steps 1 thru 4 as in D) above.
2. Wait for 1 second, then send FSK mark.
3. Wait for carrier to drop. Start a 3 second timer. If carrier drops prior to timeout proceed to step 4. Otherwise proceed to step 4 after timeout.
4. Wait for FSK mark.
5. Turn on connection indicator (28).
6. Turn transmit mark off (10).
7. Unclamp receive data (22).
8. Turn on carrier detect output.
9. Send CONNECT message to terminal.

F. Answering call (CCITT mode) with auto speed detection (V.22/V.21):

1. Select answer mode (2F).
2. Turn scrambler off (32).
3. Wait for 2.1 second billing timeout.
4. Select low speed mode (2E); V.21 mode (39).
5. Turn on 2100 Hz answer tone (37). Start 3.3 second timer.
6. Turn off 2100 Hz answer tone (17) after timeout.
7. Turn transmitter off (05).
8. Wait 60 ms.
9. For next 20 ms look for carrier and continuous FSK mark. If detected, assume low speed and proceed to step 14.
10. Turn transmitter on (25).
11. Select high speed mode (0E). Turn off V.21 mode (19).
12. Turn on 1800 Hz guard tone; (21), (6D).
13. Start 1 second timer. Look for continuous PSK mark for 64 bit intervals over 1 second period. If PSK mark is not detected within 1 second, turn off high speed mode, (select low speed mode), turn off guard tone, turn on V.21 mode and look for continuous FSK mark for 64 bit intervals over the next 1 second period. If FSK mark is not detected, repeat from start. If timeout set in S7 occurs prior to detecting either PSK or FSK mark, output NO CARRIER and abort call. If either PSK or FSK mark is detected, go to step 10 in A).
14. Turn transmitter on (25).
15. Send CONNECT message to terminal.
16. Turn connection indicator on (28).
17. Turn carrier detector on.

G. Requesting remote digital loopback to far end modem:

1. Clamp receive data to mark condition (2).
2. Force transmitter to mark (30).
3. Disable scrambler (32).
4. Wait for 180 ms (send unscrambled mark).
5. Sample PSK detector output (D2) to see if dotting pattern (alternating 1/0 pattern) is received. If dotting pattern is not received within 212 ms, output ERROR to data terminal and return to on line state.
6. Turn scrambler on (12).
7. Wait 270 ms (send scrambled mark).
8. Go to step 11 in A) above.

H. Terminating remote digital loopback:

1. Force transmitter to mark (30).
2. Clamp receive data to mark (2).
3. Turn transmitter off (5).
4. Wait 80 ms.
5. Turn transmitter on (25).
6. Wait 270 ms (send scrambled mark).
7. Go to step 11 in A) above.

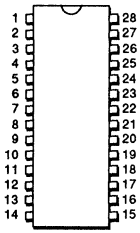
I. Response to remote digital loopback request:

1. In on line state monitor unscrambled mark detector output (D3). Go to step 2 if unscrambled mark is detected.
2. Clamp receive data to mark (2).
3. Transmit dotting pattern (34).
4. Wait until unscrambled mark detector turns off.
5. Turn off dotting pattern (14).
6. Put SC11015 in digital loopback (33).
7. Remain in digital loopback until loss of carrier is detected.
8. Terminate digital loopback.
9. Return to on line state.

FEATURES

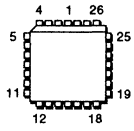
- ☐ Direct interface to SC11004, SC11014 and SC11015 single chip modems
- ☐ Built-in UART
- ☐ Complete "AT" command set in firmware
- ☐ Direct IBM PC bus interface
- ☐ 28-pin DIP or PLCC package

28-PIN DIP PACKAGE



SC11017CN

28-PIN PLCC PACKAGE

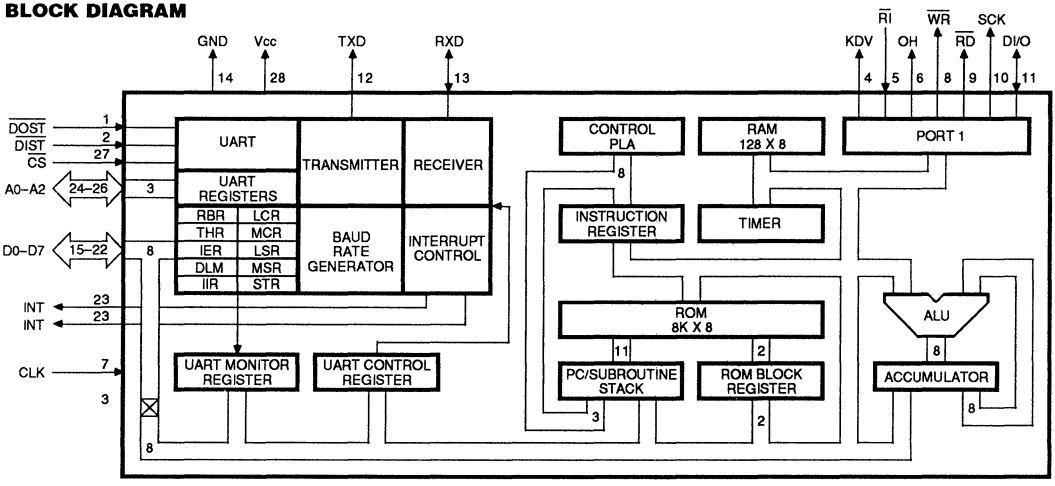


SC11017CV

GENERAL DESCRIPTION

The SC11017 Modem Interface Controller is specifically designed to control Sierra's SC11004, SC11014 and SC11015 single chip, 300/1200 bit per second modems. Built with Sierra's advanced CMOS process, the SC11017 provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to the SC11004/14/15, with the addition of a data access arrangement (DAA), the SC11017 implements a Hayes-type smart modem for board level, integral modem applications. Because the SC11017 fully emulates the functionality of the 8250B UART with increased speed, and includes data bus transceivers, it can be directly interfaced to a computer's parallel data bus and in particular to the bus of the IBM PC, XT or AT. In particular the SC11017 incorporates IO channel ready control circuitry and provides a RDY signal to inject wait states into the PC thus allowing the SC11017 to work inside any high speed PC compatible computer. All of the popular communications software written for the PC will work with the chip set. Besides including the functionality of the 8250B UART, the SC11017 contains an 8 bit microprocessor, 8k by 8 bytes of ROM and 128 by 8 bytes of RAM. For specific high volume applications, the control program can be modified by Sierra to include additional commands and functions.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE FOR BOTH DIP & PLCC

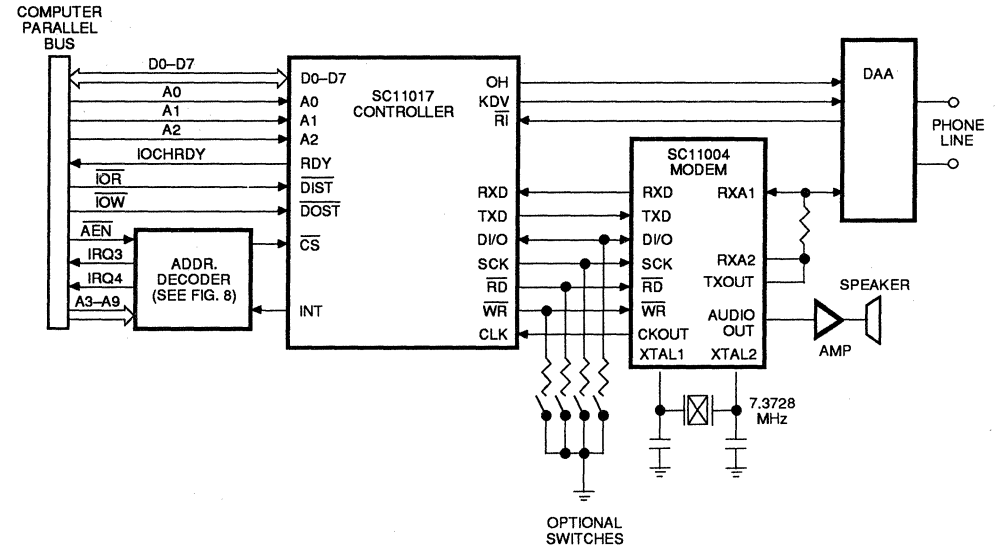


Figure 2. Integral Smart Modem Configuration for PC Bus Applications

PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	$\overline{DOST}$	I	The CPU can write data or control words into a selected register of the SC11017 when $\overline{DOST}$ is low and the chip is selected. Data is latched on the rising edge of the signal.
2	$\overline{DIST}$	I	The CPU can read data or status information from a selected register of the SC11017 when $\overline{DIST}$ is low and the chip is selected.
3	RDY	O	This **open drain output** to low to inject wait state into the computer. Following a self-timed delay (approximately 500 ns) wait state is released.
4	KDV	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. During a data call, the SC11017 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
5	$\overline{RI}$	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the On duration of the ring cycle. This is a Schmidt Trigger input, allowing for slow rising and falling signals on this pin.
6	OH	0	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the SC11017 pulses this output at a rate of 10 pulses per second with appropriate mark/space ratio depending on 212A or V.22 mode.
7	CLK	I	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the SC11004, SC11014 and SC11015 modem is connected to this pin. All internal timing is derived from this clock.
8	$\overline{WR}$	I/O	This pin is used to initiate writing of data to the SC11004, SC11014 and SC11015 modem. On power-up, it is an input for a brief time in which the SC11017 reads the carrier status switch connected to this pin. If the switch is closed to ground thru an 18 kΩ resistor, the SC11017 sets the Received Line Signal Detect (RLSD) bit in the Modem Status Register. If the switch is open or tied to V_{CC} thru 18 kΩ, the SC11017 resets this bit and writes the actual status of the carrier detector during a data call. However, NO switch is required, since an internal pullup sets the status during power-up to the default state (pullup to V_{CC}) which is to follow the remote modem's carrier.

Pin No.	Pin Name	I/O	Description
9	$\overline{RD}$	I/O	This pin is used to initiate reading of data from the SC11004, SC11014 and SC11015modem. On power-up, this pin is an input for a brief time in which the SC11017 reads the DTR status switch connected to this pin. If this switch is open or tied to V_{CC} thru 18 kΩ, the SC11017 reacts to the status of the DTR bit in the UART Modem Control Register. If the switch is closed to ground thru 18 kΩ, the SC11017 ignores the state of the DTR bit. When the switch is open, writing a 0 to the DTR bit in the Modem Control Register forces the SC11017 into the command state and when on line, causes it to hang up. However, NO switch is required, since an internal pullup to V_{CC} sets the status during power-up to the default state—to follow the DTR status.
10	SCK	I/O	The SC11017 supplies a shift clock on this pin to the SC11004, SC11014 and SC11015 modem for reading or writing data. On power-up, this pin is an input for a brief time in which the SC11017 reads the Bell/CCITT select switch connected to this pin. If this switch is open or tied to V_{CC} thru 18 kΩ, Bell protocol is selected. If this switch is closed to ground 18 kΩ, CCITT V.22 protocol is selected. However, NO switch is required, since an internal pullup sets the status during power-up to the default state—212A mode.
11	DI/O	I/O	The SC11017 shifts data serially out of this pin to SC11004, SC11014 and SC11015 during a write operation and shifts data serially into this pin during a read operation from the SC11004, SC11014 and SC11015. On power-up this pin is an input for a brief time in which the SC11017 reads the Make/Break ratio select switch connected to this pin for selecting the pulse dialing standard. With the switch open or tied to V_{CC} thru 18 kΩ, the Bell standard 39% Make, 61% Break is selected. With the switch closed to ground thru 18 kΩ, the CCITT standard 33% Make, 67% Break is selected. However, NO switch is required, since an internal pullup sets the status during power-up to the default state—Bell standard.
12	TXD	O	During a data call, after the connection is established, the SC11017 converts parallel data received from the computer bus and outputs it in a serial, asynchronous format to the SC11004, SC11014 and SC11015 modem for modulation. At all other times the SC11017 holds this output in the Mark (high) condition.
13	RXD	I	Demodulated data from the SC11004, SC11014 and SC11015 modem is received on this pin during a data call. A high level is considered Mark and a low level is a Space. The SC11017 converts the serial data into a parallel data byte and stores it in the Receiver Buffer Register (RBR). The Data Ready bit in the Line Status Register (LSR) is then set, and an appropriate interrupt indentification code is written in the Interrupt Identification Register (IIR) to signal to the computer, the reception of a new data byte.
14	GND	—	Ground reference (0 Volts).
15–22	D0–D7	I/O	This is the 8 bit data bus comprised of three state input/output lines. This bus provides bidirectional communication between the SC11017 and the CPU. Data, control words and status information are transferred via the D0–D7 data bus. Because on-chip high drive buffers are used, no external transceiver IC, such as the 74LS245, is needed between the computer bus and the SC11017.
23	INT	O	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER: Receiver Line Status Flag, Received Data Available, Transmitter Holding Register Empty and Modem Status. It is reset low upon the appropriate interrupt servicing. **The INT pin is forced to a Hi-Z state** when the OUT2 bit of the Modem Control Register (MCR) is low (power on state).
24–26	A0–A2	I	These three address inputs are used during read or write operation to select a UART register in the SC11017 as shown in Table 1. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2.
27	$\overline{CS}$	I	The SC11017 is selected when this input is low. When high, the SC11017 forces the Data bus lines into a high impedance state.
28	V_{CC}	—	Positive supply (+5 Volts).

SPECIFICATIONS

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read only) (RBR)
0	0	0	0	Transmitter Holding (write only) (THR)
0	0	0	1	Interrupt Enable (IER)
X	0	1	0	Interrupt Identification (read only) (IIR)
X	0	1	1	Line Control (LCR)
X	1	0	0	Modem Control (MCR)
X	1	0	1	Line Status (LSR)
X	1	1	0	Modem Status (read only) (MSR)
X	1	1	1	Speed (STR)
1	0	0	0	Divisor Latch (LSB) (write only) (DLL)
1	0	0	1	Divisor Latch (MSB) (write only) (DLM)

Table 1. SC11017 UART Registers

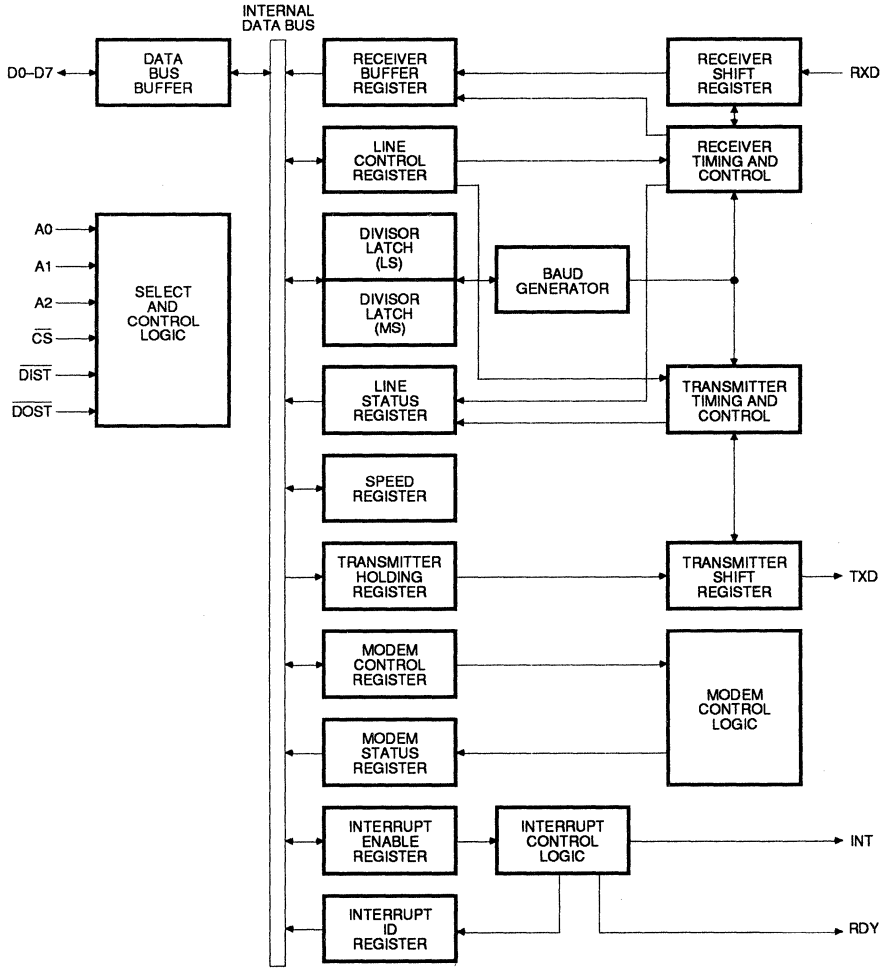


Figure 3. UART Block Diagram

Name	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
RBR	Data	Data	Data	Data	Data	Data	Data	Data
THR	Data	Data	Data	Data	Data	Data	Data	Data
IER	Receive Data Available Interrupt Enable	THRE Interrupt Enable	Receive Line Status Interrupt Enable	Modem Status Interrupt Enable	0	0	0	0
IIR	0 If Interrupt Pending	Interrupt ID Bit 0	Interrupt ID Bit 1	0	0	0	0	0
LCR	0 = 7 Bit Data 1 = 8 Bit Data	1	0 = 1 Stop Bit 1 = 2 Stop Bits	1 = Parity Enable	1 = Even Parity	1 = Stick Parity	1 = Set Break	DLAB
MCR	Data Terminal Ready	Request to Send	OUT1	OUT2 0 = INT Output to HI-Z	No Function	0	0	0
LSR	Data Ready	Overrun Error	Parity Error	Framing Error	Break Interrupt	THRE	TSRE	0
MSR	0	0	Trailing Edge Ring	Delta RLSD	1 (CTS)	1 (DSR)	Ring	RLSD
DLM	Data	Data	Data	Data	Data	Data	Data	Data
STR	Data	Data	Data	Data	Data	Data	Data	Data

Table 2. SC11017 UART Register Function Summary

Register	Range/Units	Description	Default
S0	0–255 rings	Ring to answer telephone on	0
S1	0–255 rings	Number of rings	0
S2	0–127 ASCII	Escape code character	43(+)
S3	0–127 ASCII	Character recognized as carriage return	13(CR)
S4	0–127 ASCII	Character recognized as line feed	10(LF)
S5	0–32, 127 ASCII	Character recognized as back space	8(BS)
S6	2–255 sec.	Wait time for dial tone	2
S7	1–255 sec.	Wait time for carrier	30
S8	0–255 sec.	Pause time (caused by comma)	2
S9	1–255 1/10 sec.	Carrier detect response time	6
S10	1–255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50–255 millisec.	Duration and spacing of Touch-Tones	70
S12	20–255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	—
S14	bit mapped	Option register	—
S15	bit mapped	Flag register	—
S16	0,1,2,4	Test modes	0

Table 3. SC11017 S Registers (Software Registers) Used by AT Commands

Command	Desc. (Notes 1 and 2)
Prefix, Repeat and Escape Commands	
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; + + + is not followed by carriage return)
Dialing Commands	
D	Dial
P	Pulse*
T	Touch-Tone
,	Pause
!	Flash
/	Wait for 1/8 second
@	Wait for silence
W	Wait for second dial tone
;	Return to command state after dialing
R	Reverse mode (to call originate-only modem)

Command	Desc. (Notes 1 and 2)
Other Commands	
A	Answer call without waiting for ring
B/B0	CCITT V.22 mode (Note 3)
B1	Bell 103 and 212A mode*
C/C0	Transmit carrier off
C1	Carrier on*
E/E0	Characters not echoed
E1	Characters echoed*
F/F0	Half duplex
F1	Full duplex*
H/H0	On hook (hang up)
H1	Off hook, line and auxiliary relay
H2	Off hook, line relay only
I/I0	Request product ID code (130)
I1	Firmware revision number
I2	Test internal memory
L/L1	Low speaker volume
L2	Medium speaker volume*
L3	High speaker volume
M/M0	Speaker always off
M1	Speaker on until carrier detected*
M2	Speaker always on

Command	Desc. (Notes 1 and 2)
Other Commands	
O	Go to on-line state
O1	Remote digital loopback off*
O2	Remote digital loopback request
Q/Q0	Result codes displayed*
Q1	Result codes not displayed
Sr?	Requests current value of register r
Sr=n	Sets register r to value of n
V/V0	Digit result codes
V1	Word result codes*
X/X0	Compatible with Hayes-type 300 modems*
X1	Result code CONNECT 1200 enabled
X2	Enables dial tone detection
X3	Enables busy signal detection
X4	Enables dial tone and busy signal detection
Y/Y0	Long space disconnect disabled*
Y1	Long space disconnect enabled
Z	Software reset: restores all default settings

Notes: 1. Default Modes are indicated by *.
2. Commands entered with null parameters assume 0-X is the same as X0.
3. When used with the SC11014 and SC11015 modem IC, which has CCITT V.21 as well as V.22 modes, when the ATB command is used, in the answer mode, the SC11017 will put the SC11014 and SC11015 in either the V.21 mode or the V.22 mode, depending on the response from the remote modem. In the originate mode, the SC11017 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the SC11014 and SC11015 accordingly.

Table 4. Command Summary

Digit Code	Word Code	Description
0	OK	Command executed
1	CONNECT	Connected at 300 or 1200 bps. Connected at 300 bps., if result of X1, X2, X3 or X4 command
2	RING	Ringing signal detected (Note 1)
3	NO CARRIER	Carrier signal not detected or lost
4	ERROR	Illegal command Error in command line Command line exceeds buffer (40 character, including punctuation) Invalid character format at 1200 bps.
5	CONNECT 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	NO DIALTONE	Dialtone not detected and subsequent commands not processed. Results from X2 or X4 commands only.
7	BUSY	Busy signal detected and subsequent commands not processed. Results from X3 or X4 commands only.
8	NO ANSWER	Silence not detected and subsequent commands not processed. Results from @ command only.

Note 1. When the SC11017 detects a ringing on the telephone line, it sends a RING result code. However, the SC11017 will answer the call only if it is in auto-answer mode or is given an A command.

Table 5. Result Codes

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	+ 6 V
Input Voltage	–0.6 V to V_{CC}+0.6
Storage temperature range	–65° to +150°C.
Maximum power dissipation @ 25°C.	500 mW
Lead temperature (soldering, 10 sec)	300°C.
Operating temperature range	0° to 70°C.

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

DC ELECTRICAL CHARACTERISTICS

Param.	Description	Conditions	Min	Typ	Max	Units
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Operating Current	@ V_{CC} = 5 V		10.0		mA
V_{ih}	High Level Input Voltage	all pins except $\overline{RI}$	2.0			V
V_{il}	Low Level Input Voltage	all pins except $\overline{RI}$			0.8	V
V_t+	Positive hysterisis threshold	$\overline{RI}$ pin		2.5		V
V_t–	Negative hysterisis threshold	$\overline{RI}$ pin		1.8		V
V_{oh}	High Level Output Voltage	Digital signal pins D0 to D7 & INT @ I_{oh} = 6 mA All other output or I/O pins @ I_{oh} = 2 mA	V_{CC} –1.0 V_{CC} –1.0			V V
V_{ol}	Low Level Output Voltage	Digital signal pins D0 to D7 & INT @ I_{ol} = 6 mA All other output or I/O pins @ I_{ol} = 2 mA			0.4 0.4	V V
I_l	Leakage Current (Note 2)			±1.0		uA
f_{clk}	Clock frequency		7.3721	7.3728	7.3735	MHz

Note 2. This applies to all pins except TEST, which has an internal pull-down, and $\overline{WR}$, $\overline{RD}$, SCK, and the DI/O pins which have internal pullups.

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{DIW}	$\overline{DIST}$ Strobe Width	1TTL Load	570		ns
t_{RC}	Read Cycle Delay	1TTL Load	300		ns
RC	Read Cycle = t_{DIW} + t_{RC} + 20 ns	1TTL Load	890		ns
t_{DDD}	Delay from $\overline{DIST}$ to Data	1TTL Load		570	ns
t_{HZ}	$\overline{DIST}$ to Floating Data Delay	1TTL Load	60		ns
t_{DOW}	$\overline{DOST}$ Strobe Width	1TTL Load	570		ns
t_{WC}	Write Cycle Delay	1TTL Load	300		ns
WC	Write Cycle = t_{DOW} + t_{WC} + 20 ns	1TTL Load	890		ns
t_{DS}	Data Setup Time	1TTL Load	60		ns
t_{DH}	Data Hold Time	1TTL Load	40		ns
t_{DIC}	$\overline{DIST}$ Delay from Select	1TTL Load	80		ns
t_{DOC}	$\overline{DOST}$ Delay from Select	1TTL Load	50		ns
t_{ACR}	Address and Chip Select Hold Time from $\overline{DIST}$	1TTL Load	10		ns
t_{ACW}	Address and Chip Select Hold Time from $\overline{DOST}$	1TTL Load	70		ns
Receiver					
t_{RINT}	Delay from $\overline{DIST}$ (Read RBR) to Reset Interrupt	100 pF Load		1	µs
Transmitter					
t_{HR}	Delay from $\overline{DOST}$ (Write THR) to Reset Interrupt	100 pF Load		1	µs
t_{IRS}	Delay from Initial INTR Reset to Transmit Start			1	Baud Cycle
t_{SI}	Delay from Initial Write to Interrupt			1	Baud Cycle
t_{SS}	Delay from Stop to Next Start			1	µs
t_{STI}	Delay from Stop to Interrupt (THRE)			1	Baud Cycle
t_{IR}	Delay from $\overline{DIST}$ (Read IIR) to Reset Interrupt (THRE)	100 pF Load		2.2	µs

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Power On Reset	All Bits Low
Interrupt Identification Register	Power On Reset	Bit 0 High; Bits 1–7 Low
Line Control Register	Writing into the LCR	Data
MODEM Control Register	Power On Reset	All Bits Low
Line Status Register	Power On Reset	Bits 0–4, 7 Low; Bits 5 and 6 High
Modem Status Register	Power Reset	Bits 0–3, 6–7 Low; Bits 4–5 High
Divisor Latch (high order bits)	Power On Reset	1200 BPS
TXD	Master Reset	High
INT	Power On Reset	Low (High-Z)

Table 6. Reset Control of Registers and Pinout Signals

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = +5V ± 10%) 1 Clock cycle = 135 ns

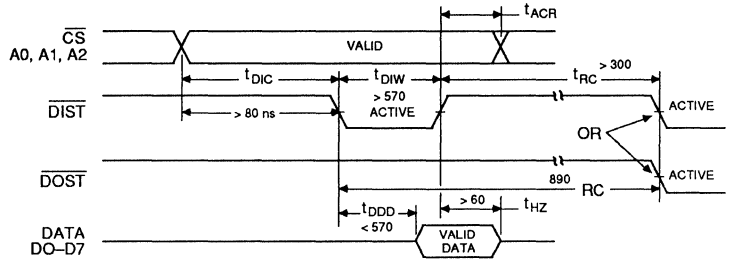


Figure 4. Read Cycle Timing

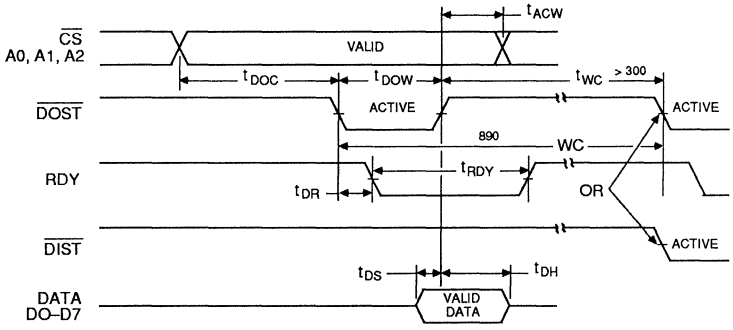


Figure 5. Write Cycle Timing

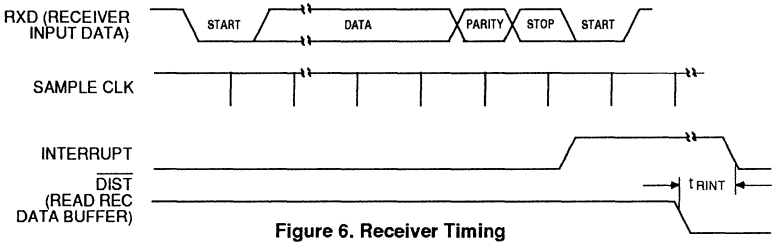


Figure 6. Receiver Timing

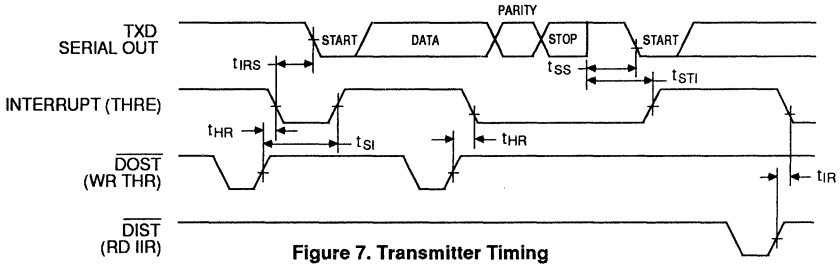


Figure 7. Transmitter Timing

UART REGISTERS

Line Control Register

This register controls the format of the asynchronous data communications.

Bits 0 and 1: Bit 1 is always high. Bit 0 specifies the number of bits in each transmitted or received serial character. The encoding of bit 0 is as follows:

Bit 1	Bit 0	Word Length
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1, when 7-bit word length with no Parity is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 0 is a logic 0 and bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed).

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is logic 1 and bit 5 is logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (TXD) is forced to the Spacing state (logic 0) and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Rate Generator

The SC11017's Baud Rate Generator can be programmed for one of six Baud rates. The desired speed is selected by writing into the Divisor Latch (DLM). On reset, the rate will be 1200 baud.

DLM (HEX Code)	Baud Rate
00	1200
01	300
03	150
04	110
06	75
09	50

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE bit is set to a logic 1 upon detection of parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time—the total time of Start bit + data bits + Parity + Stop bits.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the SC11017 is ready to accept a new character for transmission. In addition, this bit causes the SC11017 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register.

Bit 7: This bit is permanently set to logic 0.

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

UART REGISTERS

Interrupt Identification Register

The SC11017 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors. To provide minimum software overhead during data character transfers, the SC11017 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Table 7). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 7.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the SC11017 to separately activate the Interrupt (INT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Register. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Interrupt Identification Register			Interrupt Set and Reset Functions			
B2	B1	B0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Table 7. Interrupt Control Functions

MODEM Control Register

This 8-bit register controls the interface with the MODEM. The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls Data Terminal Ready (DTR) signal. If the external switch on the RD pin is set to V_{CC} thru an 18 kΩ resistor, setting the DTR low will force the SC11017 into the command state and, if on line, it will hang up.

Bit 1: This bit controls the Request to Send (RTS) signal. This signal is not used by the SC11017.

Bit 2: This bit controls the Output 1 (OUT 1) signal. This signal is not used by the SC11017.

Bit 3: This bit controls the Output 2 (OUT 2) signal. When OUT 2 is a 0, the interrupt output is in High-Z state.

Bit 4: Not used.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, two bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bit 0 and 1: These bits are always 0.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit indicates that the carrier detector has changed state.

Bit 4: This bit is always 1.

Bit 5: This bit is always 1.

Bit 6: This bit is the complement of the Ring Indicator (RI) input.

Bit 7: This bit is the Received Line Signal Detect (RLSD) signal.

Whenever bit 2 is set to logic 1, or bit 3 changes state, a MODEM Status Interrupt is generated if enabled.

Using SC11017's RDY Output

The basic concept behind the RDY circuit is to slow down the computer just during a read or a write cycle to SC11017 to insure (i) the setup time from CS to DIST, DOST is met and (ii) the address/data hold time after DOST is satisfied.

SC11017 requires a minimum of 80 ns for (i) and 70 ns for (ii).

When a read/write cycle starts, the circuit applies ground to IOCHRDY signal (Bus pin A10) causing the computer to stretch read/write pulses. IOCHRDY is released when read/write timing requirements are satisfied.

APPLICATIONS

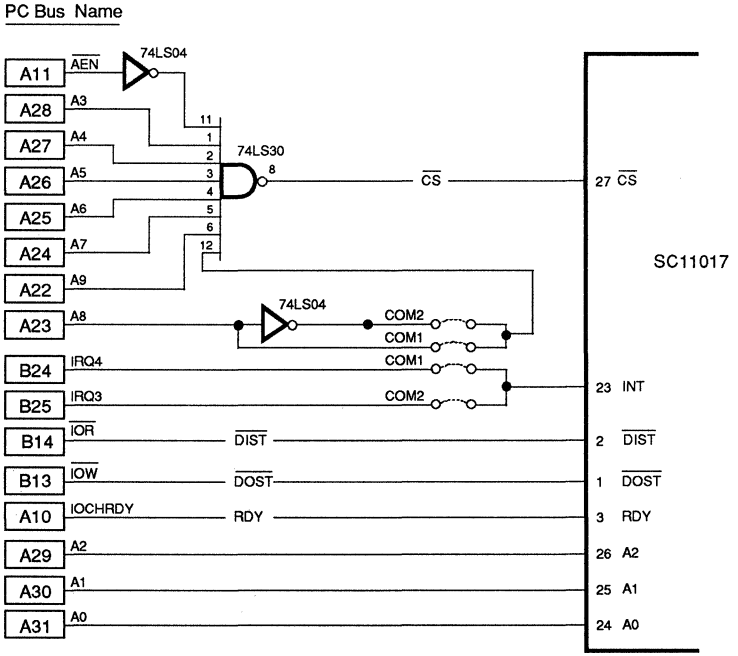


Figure 8. PC Bus Interface Address Decoder

FEATURES

- ☐ Direct interface to SC11024 or SC11006 single chip modem
- ☐ Complete "AT" command set in internal firmware
- ☐ Built-in UART
- ☐ Direct IBM PC bus interface
- ☐ CMOS technology
- ☐ G3 Fax added with SC11074,75
- ☐ External ROM/RAM addressable
- ☐ 40 mW Power-Down Mode
- ☐ Four-bit general I/O port
- ☐ RS-232 interface
- ☐ Synchronous and asynchronous communication supported

GENERAL DESCRIPTION

The Modem Advanced Controller (MAC) is a specialized controller which interfaces directly to SC11006 or SC11024 Modem Analog Processor (MAP) to implement a 2400 bps full duplex intelligent modem. The two-chip set performs all the modem functions as well as automatic control features compatible to the Hayes "AT" Command Set. The chip set conforms to CCITT V.22 bis with V.22 fallback, Bell 212A with 103 fallback, as well as V.21 standards.

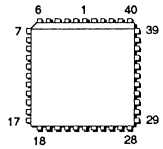
The SC11019 and SC11023 interface to a parallel system bus, such as that in the IBM PC, while the SC11020 interfaces to an RS-232 port. Both SC11019 and SC11023 have an on-board 16C450 equivalent UART. The new SC11074,75 versions are programmed to support the 9600 Sendfax MAC (SC11054). They are available only in 44-pin PLCC, offering the world's smallest fax and data modem chipset.

The SC11021 is the ROMless version capable of addressing 32 k bytes of external memory and is available in a 68-pin PLCC package.

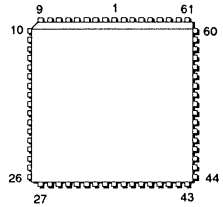
The SC11022 is the fully configurable version of both controllers and is available in 48-pin DIP and 68-pin PLCC package. The 68-pin version is capable of addressing up to 24 k bytes of external memory.

This MAC is similar to, and pin compatible with, the SC11011. The major differences are the addition of a 16k internal ROM containing all the DSP and Hayes compatible commands, plus a four bit I/O port which may be used to communicate with a low cost serial E^2 memory. The I/O port is also used to select the modem configuration—RS-232 or parallel interface, internal or external hybrid, SC11006 or SC11024 MAP. This port is not available in the 44-pin PLCC for parallel applications so these versions are factory programmed for internal hybrid. The SC11019CV is set for use with SC11006 MAP while SC11023CV is set for SC11024 MAP.

44- & 68-PIN PLCC PACKAGES

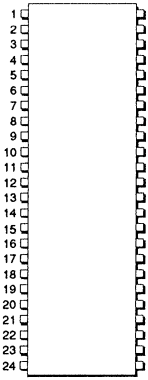


SC11019/SC11020/SC11023/SC11074/SC11075CV



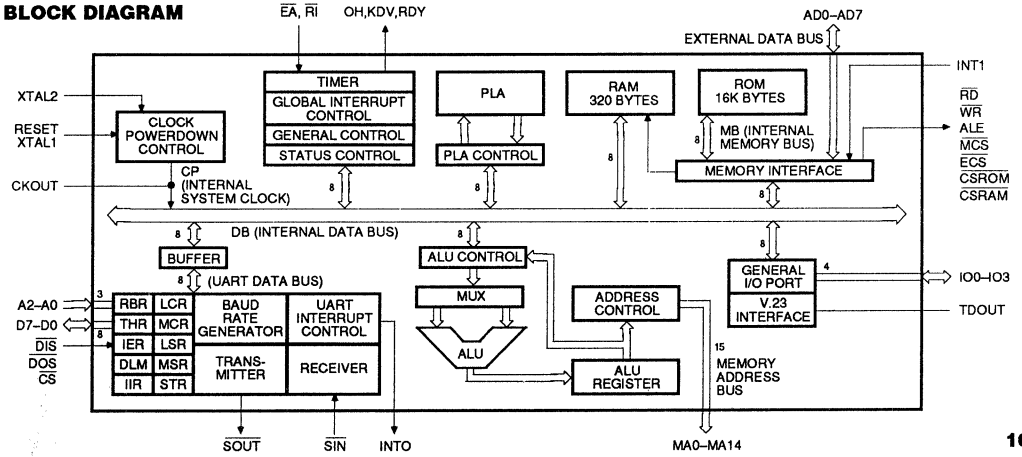
SC11021/SC11022CV

48-PIN DIP PACKAGE

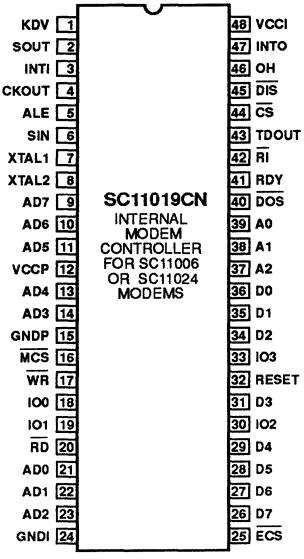


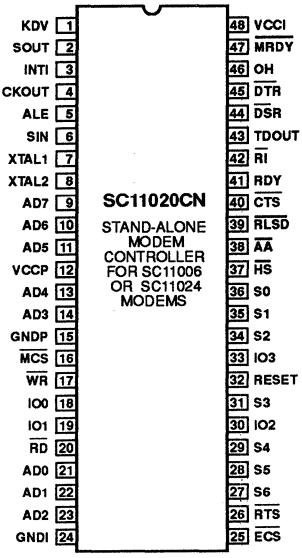
SC11019/SC11020/SC11022CN

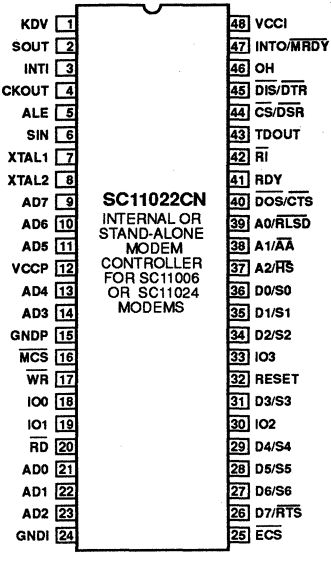
BLOCK DIAGRAM

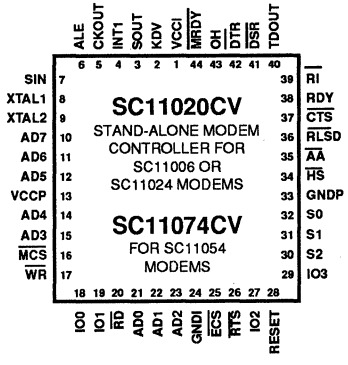


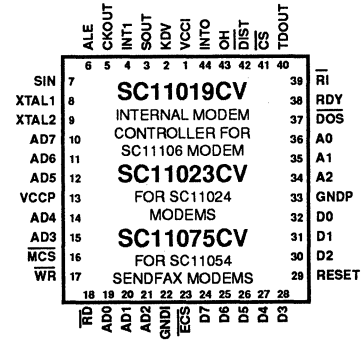
CONNECTION DIAGRAMS

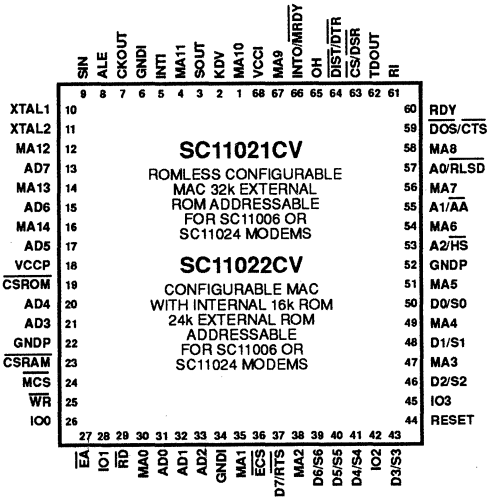




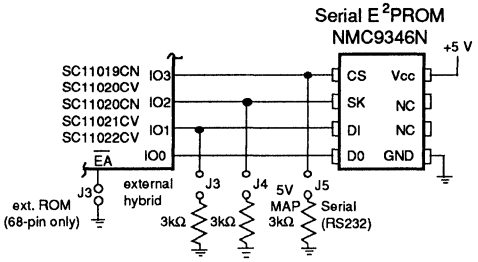








CONFIGURATIONS FOR SC11019CN, 20CN, 20CV, 22CV BIG MACS



All models listed above can operate with either serial or multiplexed E²PROMs for configuration and number storage. The internal ROM program automatically determines which kind of E²PROM is connected and adapts accordingly.

Note that the SC11022 pin configuration matches that of the SC11011 controller except five new pins are used that were formerly not connected. Four of these are the I/O pins described above. One is the TDOUT pin which will be used with SC11026 for V.23 signalling.

MAC PART NO.	PACKAGE	INT. ROM	EXT. ROM	UART MODE	MAP
SC11019CV	44-PLCC	16 k	–	Parallel	SC11006
SC11019CN	48-DIP	16 k	–	Parallel	SC11006/24
SC11020CV	44-PLCC	16 k	–	Serial	SC11006/24
SC11020CN	48-DIP	16 k	–	Serial	SC11006/24
SC11021CV	68-PLCC	0	32 k*	Serial/Par.	SC11006/24
SC11022CV	68-PLCC	16 k	24 k	Serial/Par.	SC11006/24
SC11022CN	48-DIP	16 k	–	Serial/Par.	SC11006/24
SC11023CV	44-PLCC	16 k	–	Parallel	SC11024

When substituting SC11022 for SC11011 it is only necessary to open the EA pin and remove the external EPROM. Connect the jumpers as shown if required to operate with SC11024 MAP, external hybrid or in serial mode.

Three of the four I/O pins on the specified models of the internal ROMed MAC are programmed to set the configuration at power-up or reset. Internal weak pull-up resistors will set the default configuration to internal hybrid, ±5 V SC11006 MAP interface and Parallel mode if there is no external pull-down.

External pull-down resistors must be added to select other options as indicated in the table. The I/O drivers will overcome these pull-up or pull-down resistors in normal operation to operate the serial E²PROM. The I/O pins may be directly grounded if the serial E²PROM is not used. The SC11074 and SC11075 do not support E²PROM.

In the 44-pin version of SC11019, the I/O pins are not externally available. The SC11023 is internally bonded to select the 5 V only MAP (SC11024) configuration.

INTERFACE BLOCK DIAGRAMS

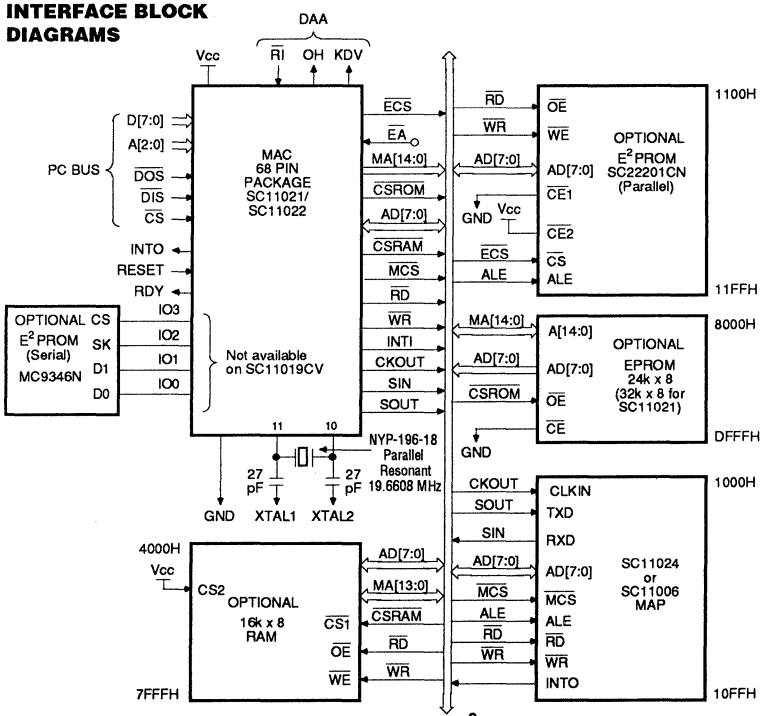


Figure 2. MAC 68 Pin Package Interfaces to E²PROM, ROM Map

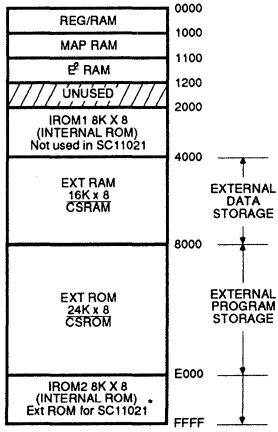


Figure 3. MAC Address Map

PIN DESCRIPTION

SC11019/21/22/23/75 Pin Description (Interfaces to Parallel System Bus)

I Parallel System Interface (to PC Bus)

$\overline{CS}$	Chip select, active low, input, TTL.
A2–A0	Address lines for UART register select, input, TTL.
INTO	Interrupt, output, CMOS/TTL, three-state. Pin is high impedance after reset.
D7–D0	8-bit data port, input-output, TTL, three-state.
$\overline{DOS}$	Data out strobe (PC writes into UART registers), active low, input, TTL.
$\overline{DIS}$	Data in strobe (PC reads from UART registers), active low, input, TTL.

II MAP Interface

AD7–AD0	8-bit bidirectional multiplexed address/data bus, CMOS.
$\overline{RD}$	RAM read, output, CMOS/TTL, normally high, data on AD7–AD0 must be valid at the rising edge of this pulse.
$\overline{WR}$	RAM write, output, CMOS/TTL, normally high, data on AD7–AD0 is valid at the rising edge of this pulse.
ALE	Address Latch Enable, output, CMOS/TTL, the address on $\overline{ECS}$, $\overline{MCS}$, AD7–AD0 are valid at the falling edge of this normally low pulse.
SOUT	Transmit data, output, CMOS/TTL. Serial data to be transmitted by the modem.
SIN	Received data, input; TTL. Serial data received from the MAP.
INTI	Interrupt input, TTL; interrupt received from the MAP at 600 Hz. Interrupt is detected when this pin has a low to high transition. The line has to stay high for at least 200 ns.
$\overline{MCS}$	Map chip select for MAP interface, output, TTL/CMOS, addressing space is from 1000H to 10FFH.
$\overline{ECS}$	External EERAM chip select or for second MAP chip select, output, TTL/CMOS, addressing space is fom 1100H to 11FFH.

III DAA Interface

$\overline{RI}$	Ring indicator, input, Schmitt, when low, indicates the modem is receiving a ringing signal.
OH	Off-hook, output, TTL/CMOS, when high, indicates the DAA should go off-hook.
KDV	Data/voice Relay Control, output, TTL/CMOS. When high, indicates the voice (telephone set) relay is closed and the modem is in the voice mode.

IV Other Pins

RESET	Master reset Schmitt input, TTL, active high. When RESET is high, MAC program counter resets to location 2000H. It resumes counting after RESET goes low.
XTAL1	Together with XTAL2 for crystal input (19.6608 MHz).
XTAL2	Crystal output pin (19.6608 MHz).
CKOUT	Clock output pin, TTL/CMOS, from MAC (9.8304 MHz, ~100 ns. cycle time).
VCCI	+5 V
GNDI	Ground
VCCP	Second Vcc pin
GNDP	Second Gnd pin
TDOUT	Output, TTL/CMOS, CCITT V.23 Transmit Data Output (General I/O Port), three-state. Controlled by General I/O Port. See page 17.
PD	Power Down Output, TTl/CMOS, Low indicates power down mode. SC11074, 75 only.
RDY	Ouput, ready signal for high speed PC-AT interface.

V Extra Pins For 48 Pin Package (SC11019/21/22)

IO3–0	General I/O Port, TTL/CMOS, three-state All these pins have weak internal 30 kΩ pull-ups to Vcc.
IO0	Serial E^2PROM data out Each I/O pin can be configured as either input or output under control of GIO (page 16). The internal ROM uses these pins as follows:
IO1	Serial E^2PROM D1/External 3 kΩ pull-down selects external hybrid configuration.
IO2	Serial E^2PROM clock/External 3 kΩ pull-down selects 5 V MAP (SC11024).
1O3	Serial E^2PROM $\overline{CS}$/External 3 kΩ pull-down selects serial mode.

VI Extra Pins For 68 Pin Package Only (SC11021/22)

MA0–MA14	Output, TTL/CMOS, 15 bit address bus for external program/data access.
$\overline{CSROM}$	Output, TTL/CMOS, chip select for external ROM, address from 8000H to DFFFH.
$\overline{CSRAM}$	Output, TTL/CMOS, chip select for external RAM, address from 4000H to 7FFFH.

PIN DESCRIPTION (Cont.)

VI Extra Pins For 68 Pin Package Only (SC11021/22)

$\overline{EA}$	Input, External access enable. Low will cause the chip to jump to external vector 8000H after a 2000H reset. Also when this pin is low, the chip will use external interrupt vector. These functions are controlled by internal ROM code. $\overline{EA}$ pin has a weak internal 30 kΩ pull-up to Vcc.
GNDI	Third Gnd pin for 68 pin package.

SC11020/21/22/74 Pin Description

(Interfaces to RS-232 port)

I MAP Interface

16 pins identical to SC11019 including: AD7–AD0, $\overline{RD}$, $\overline{WR}$, ALE, SOUT, SIN, INTI, $\overline{MCS}$, $\overline{ECS}$.

II RS-232 (Data Set Mode) and Display Interface

$\overline{DTR}$	Data terminal ready, input, TTL.
$\overline{AA}$	Automatic answer enable (low), output, TTL/CMOS.
$\overline{HS}$	High speed indicator, output, TTL/CMOS. Low when operating at 2400 bps rate. High otherwise.
$\overline{MRDY}$	Modem ready.
$\overline{RLSD}$	Carrier detect, output, TTL/CMOS.
$\overline{DSR}$	Data set ready, output, TTL/CMOS.
$\overline{RTS}$	Request to send, input, TTL.
$\overline{CTS}$	Clear to send, output, TTL/CMOS.

III DAA Interface

3 pins the same as SC11019 namely: OH, RI, KDV.

IV Switch Port Pins

S0–S4	5-bit input port for sensing switch setting inputs. External pull-up resistors (10 kΩ) must be used on these inputs or they may be hard wired to +5 V if not used. See Firmware release notes for functions supported.
S0	When low, selects dumb mode. Modem will not accept commands.
S1	S0 = 1 AA
S2	CCITS
S3	LDL

V Other Pins

10 pins, the same as SC11019 namely: RESET, XTAL1, XTAL2, CKOUT, VCC, GND1, VCCP, GND0, TDOUT, RDY, IO3–0.

VI Extra Pins For 48 Pin Package

S6–S3	3-bit input port for sensing switch setting inputs. External pull-up resistors (10 kΩ) must be used on these inputs or they may be hard wired to +5 V if not used. See Firmware release notes for functions supported.

VII Extra Pins For 68 Pin Package Only

MA0–MA14	Output, TTL/CMOS, 15 bit address bus for external program/data access.
$\overline{CSROM}$	Output, TTL/CMOS, chip select for external ROM, address from 8000H to DFFFH.
$\overline{CSRAM}$	Output, TTL/CMOS, chip select for external RAM, address from 4000H to 7FFFH.
$\overline{EA}$	Input, External access enable . Low will cause the chip to jump to external vector 8000H after a 2000H reset. Also when this pin is low, the chip will use external interrupt vector. These functions are controlled by internal ROM code. $\overline{EA}$ pin has a weak internal 30 kΩ pull-up to Vcc.
GNDI	Third gnd pin for 68 pin package.

MAC Operation

The MAC is interrupted once every 1.667 ms (600 Hz). It reads two I channel samples and two Q channel samples (T/2 sampling) within 100 µs of receiving the interrupt.

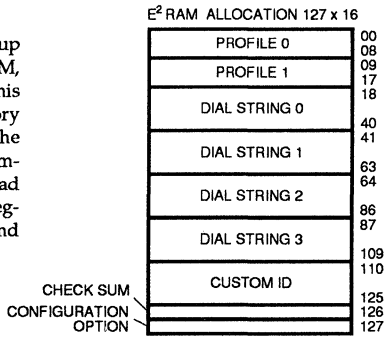
After the samples are processed a quad-bit (4 bits) descrambled of data is written back to the MAP. The MAP will perform the synch to asynch conversion function, if operating in asynchronous mode, and outputs received data on SIN pin.

Manufacturer Identification

The optional external E²PROM may be used to store your manufacturer's ID in bytes 6EH thru 7DH (16 characters). This ID will be returned on command ATI3. The manufacturer's ID must be pre-written to the E²PROM. Only the phone numbers and settings are user programmable.

Dial strings are packed 5 bits per character.

Checksum is monitored at power up reset. If it does not match internal ROM, the E²RAM is assumed to be new. This causes the program to write the factory default values into the E²ROM. If the checksum matches the internal number, the configuration profile is read from the E²PROM into the modem registers before going to the command state.



SOFTWARE ARCHITECTURE

Operand Types

1. **Short Integers:** Short integers are 8-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –128 and +127 will set the overflow bit in the Program Status Byte (PSB). There are no alignment restrictions on short integers.

2. **Integers:** Integers are 16-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –32768 and +32767 will set the overflow bit in the PSB. The least significant byte of the integers is in the even byte address and the next most significant byte is in the next higher (odd) address. Therefore, the integers must be aligned at even byte boundaries in the address space. The address of a word is the address of its least significant byte (always an even address).

3. **Bits:** The bits within the bytes of the register file are numbered from 0 to 7 with 0 referring to the LSB. The only instructions that use bit addressing are JBC and JBS.

4. **Long Integers:** Long integers are 32-bit signed 2's complement variables. The result of a 16 x 16-bit multiply will be stored in a long integer. Only SHRL and SHLL manipulate this data type. Long integers are addressed by the address of their least significant byte in the register file. They should be aligned such that their address is evenly divisible by 4. The most significant byte of a long integer resides on "address" +3, where "address" is the long integer's address.

Operand Addressing

Three types of addressing are allowed:

1. **Immediate Addressing:** This is a direct field within the instruction. For short integers, this is an 8-bit field, whereas, for the integers this is a 16-bit field. Only one operand within an instruction can be immediate reference type. This operand must always be the last (right most) operand within an instruction.

   e.g. ADD AX, #340H is allowed

   ADD AX, #340H, BX is NOT allowed

2. **Register Direct Addressing:** In this mode an 8-bit field is used to access a register from the 320 byte register file. The regiter address must conform to the alignment rules.

   e.g. ADD AX, BX :AX, BX must be "even" numbers

   ADDB AX, BX :AX, BX can be "odd" or "even"

3. **Indirect Addressing:** A memory location can be addressed indirectly by placing its 16-bit address in the register file. Only one operand (the right most operand) within an instruction can be indirect.

   e.g. ADDB AL, BL, [CX] is allowed

   ADDB AL, [CX], BL is NOT allowed

Program Status Byte (PSB), location 0192H

This is an 8-bit register storing the condition flags of arithmetic, shift, and compare instructions (see the following table). The programmer can access these bits by using address 0192H.

Firmware Revisions:

Firmware may be upgraded from time to time to add features and improve performance. Please call Sierra sales office for the current firmware documentation.

Program Status Byte (PSB) Location 0192H

BIT	NAME	FUNCTION
7	PD	Power-Down enable bit. Set HIGH to power-down. Set LOW to power-up. CKOUT slows down 32 times during power-down. Hardware reset on RI, DTR off ton in serial mode or RI, DIS, CS off to in parallel mode.
6	Unused	N/A
5	IP	Global interrupt pending bit. Set upon receipt of interrupt. Cleared when interrupt service begins.
4	IE	Global interrupt enable bit; when zero, all interrupts are disabled.
3	Z	Zero bit; indicates the last arithmetic or compare instruction produced a zero result.
2	N	Negative bit; indicates the last arithmetic or compare instruction produced a negative result.
1	C	Carry bit; indicates the state of the arithmetic carry from the most significant bit of the ALU for an arithmetic operation or the state of the last bit shifted out of the operand for a shift. Arithmetic "Borrow" after a subtract is the complement of the C flag (i.e. if borrow generated then C = 0).
0	V	Overflow bit; indicates the last arithmetic operation produced an overflow.

SOFTWARE ARCHITECTURE (Cont.)

Power-Down Feature

This MAC has the ability to operate in a standby or power-down mode in which the internal bus clock is divided by 32. This allows the CPU to continue to operate and monitor certain lines in readiness to resume normal operation. The process is fully automatic and transparent to the user.

When the SC11024 MAP is used with this MAC, it too is placed in the power-down mode. Together, the two chips consume typically 8.5 mA in this mode.

The MAC enters the power-down mode when the modem is off line and the DTE interface is inactive. Power-down is disabled in the test modes.

Normal operation resumes upon one or more of the following: DTR goes high (serial mode), RI goes true, SIN goes low (serial mode) or CS goes true (parallel mode). These inputs are hardwired to the power down register—bit 7 of program status byte.

(Note: Check with sales office listed for ROM code revision which supports power-down.)

Interrupt Structure

Four interrupt sources exist in the MAC, namely the external interrupt, timer interrupt, ring leading edge interrupt, and UART interrupt. The interupt service routine address is 2004H.

1) External interrupt: A low to high transition on the INTI pin initiates this interrupt.

2) Timer interrupt: Timer overflow interrupt—4.8 kHz frequency.

3) Ring leading edge: Interrupt generated by leading edge of ring input.

4) UART interrupt: Interrupt from UART.

   a) Parallel version: From UMR register. Any one of the following can generate this interrupt.

      RBR was read by external processor

      Data was transferred from THR to TSR

      LCR was changed

      MCR was changed

      DLL or DLM was changed

   b) Serial version: In this configuration the interrupt signal from 16C450 compatible UART is brought in as an interrupt source to the internal CPU.

INTERRUPT CONTROL REGISTER (ICR), location 0193H

This is an 8 bit register to enable or disable each of the four interrupt sources and to record the interrupt sources. The upper four bits are read/write registers while the lower four bits are read only registers. A read operation to the register will automatically clear the lower four bits.

BIT0: "1" indicates UART requested an interrupt.

BIT1: "1" indicates RING leading edge requested an interrupt.

BIT2: "1" indicates TIMER overflow requested an interrupt.

BIT3: "1" indicates EXTERNAL source requested an interrupt.

BIT4: "1" to enable UART interrupt.

BIT5: "1" to enable RING leading edge interrupt.

BIT6: "1" to enable TIMER overflow interrupt.

BIT7: "1" to enable EXTERNAL interrupt.

Any one of these four interrupts will drive the processor to address 2004H. From there the software can check interrupt sources and do priority control to branch to different service routines.

INSTRUCTION SET

The MAC instruction set is a subset of Intel 8096 instruction set. The object codes, formats and the flags they effect are identical to those of 8096. The differences are:

- No VT or ST flags exist in the MAC.
- Register locations in the UART section can only be accessed by using indirect addressing.
- The operands refer to one or more bytes of the register file. ROM locations can only be addressed using indirect addressing.
- If a memory location is addressed between 1000H and 11FFH, an external six clock multiplexed bus operation is initiated. The multiplexed address/data will use AD7–AD0 bus.
- When using ST or STB operations, the destinations are always considered to be indirect addresses.

  e.g. ST, AX, [BX] is allowed

  ST, AX, BX is NOT allowed

INSTRUCTION SET (Cont.)

Instruction Set Table

MNEMONIC	NO. OF OPERANDS	OPERATION	BYTES[1]	TIME[2]
ADD/ADDB	2	B ← A + B	3	10
ADD/ADDB	3	D ← A + B	4	10
AND/ANDB	2	B ← A AND B	3	10
AND/ANDB	3	D ← A AND B	4	10
CMP/CMPB	2	D – A	3	10
DJNZ	1	Decrement & JNZ	3	9/12
EXTB	1	Sign Extend Byte	2	7
JBC	0	Jump if bit clear	3	10/13
JBS	0	Jump if bit set	3	10/13
JC	0	Jump if Carry Set	2	5/8
JNC	0	Jump if no carry	2	5/8
JE	0	Jump if =	2	5/8
JNE	0	Jump if not =	2	5/8
JGT	0	Jump if >	2	5/8
JGE	0	Jump if >=	2	5/8
JLE	0	Jump if < or =	2	5/8
JLT	0	Jump if <	2	5/8
JV	0	Jump if Overflow	2	5/8
JNV	0	Jump if no overflow	2	5/8
JH	0	Jump if higher	2	5/8
JNH	0	Jump if not higher	2	5/8
LCALL	0	Long Call	3	11
LD/LDB	2	Load	3	10
MUL	3	D ← A * B	5	33
NOP	0	NO Operation	1	2
OR/ORB	2	D ← D OR A	3	10
XOR/XORB	2	D ← D XOR A	3	10
PUSHF	0	Push PSB	1	5
POPF	0	Pop PSB	1	5
RET	0	Return	1	10
SHL/SHLB	1	Shift Left	3	11 + N[3]
SHLL	1	Shift Left Long	3	15 + N[3]
SHR/SHRB	1	Shift Right	3	11 + N[3]
SHRL	1	Shift Right Long	3	15 + N[3]
SHRA	1	Arith. Right Shift	3	10 + N[3]
SHRAL	1	Arith. Right Long	3	15 + N[3]
SJMP	0	Short Jump	2	7
LJMP	0	Long Jump	3	9
ST/STB	2	Store to Memory	3	13[4]
SUB/SUBB	2	B ← B – A	3	10
SUB/SUBB	3	D ← B – A	4	10

[1]Add one for immediate words.

[2]Add 9 for indirect mode and 2 or 0 for immediate mode—see table. (Cycle times @ 100 ns)

[3]N is number of bit shifts.

[4]Indirect Mode.

HARDWARE ARCHITECTURE

The MAC device is organized with two buses that interconnect four main logic sections. The two buses are the internal data bus (DB) and address bus (Y). The four sections of the device are the internal processor, registers, memory, and dual port UART.

The two bus architecture was chosen to allow the MAC to execute the 8096 instruction set as fast or faster than the 8096 itself. The device is intended to run at 9.8304 MHz. A typical three operand instruction effectively executes in 10 clock cycles. The signed 16 x 16 multiply operation requires 34 clock cycles.

The internal data bus (DB) is the main bus of the device. It is an 8-bit bus that interconnects all four sections of the device. All intenal data travels on DB. The Y bus is a 16-bit output only bus from the internal processor that provides addresses to the memory and register sections of the device. This bus allows memory control to be resident inside the internal processor without degrading performance.

The internal processor controls MAC operations and performs all of the required computation functions. The internal processor consists of a microcontrol PLA and a 16-bit registered arithmetic/logic unit (RALU). The microcontrol PLA accepts as input 8096 instruction opcodes and generates the control sequences necessary to implement the instructions. The RALU performs instruction execution, operand address calculation, jump address calculation, program sequencing, and stack control. The program counter (PC) and stack pointer (SP) are contained within the RALU. The RALU is implemented with the 2901 silicon compiler.

The register section of the MAC includes RAM and the ports of the device. These locations are all treated as registers and may be accessed in register direct mode. Code can't be executed from registers. The UART registers are functionally, but not physically, part of the register section. The UART registers are accessed via indirect addressing mode only. There are 320 bytes of RAM to support DSP functions and the Hayes Smartmodem command set. The memory section of the MAC includes the program ROM and the external memory interface. The device contains 16K bytes of program ROM. The external memory interface allows the MAC to access program storage or data storage from external memory.

The UART section of the device implements the industry standard 16C450 UART. In its parallel version the MAC appears as a 16C450 to the user. The UART contains dual-port capability to allow the user and the internal processor access to its internal registers.

MEMORY DESCRIPTION

Internal ROM:

The 16K bytes of internal ROM is organized into 2 separate blocks of 8K bytes each: IROM1 and IROM2.

The SC11019/20/21/22/23 controllers are built with the same architecture as the SC11011 so that firmware will be upward compatible.

External Read/Write:

Three different types of external memory operations are defined.

A) For address from 1000H to 11FFH:

These external operations occur through the AD bus. These operations take six clock cycles, four more than internal operations. These are mainly for MAP & EEROM interfaces, however, instructions and data can also be fetched from these memory spaces.

B) For address from 4000H to 7FFFH: 68 pin only.

These memory spaces are reserved for external DATA storage. The MAC can access external RAM through MA address bus and AD data bus. There are six clock memory cycles for each access.

C) For address from 8000H to FFFFH: 68 pin only.

For 68 pin package the chip fetches instructions from external program storage by MA0–MA14 and AD0–AD7. These operations are exactly the same as internal ROM fetch and they take 2 clock cycles. For the SC11021 ROMless version, the 8k bytes from E000H to FFFFH are also mapped for external access.

Memory Address MAP

NAME	ABV	ADDRESS	R/W	SIZE (bytes)
INTERNAL RAM/REG	RAM*	0000H–013FH	R/W	320
	REG*	0180H–0193H	R/W	19 registers
EXTERNAL MAP/EERAM	MAP	1000H–10FFH	R/W	256
	EERAM	1100H–11FFH	R/W	256
INTERNAL ROM***	IROM1	2000–3FFFH	RO	8K
	IROM2	E000H–FFFFH	RO	8K
EXTERNAL RAM**	RAM	4000H–7FFFH	R/W	16K
EXTERNAL ROM**	ROM	8000H–DFFFH	RO	24K

* These may only be accessed as memory locations (16-bit address) in an indirect mode. For direct addressing a 9th bit (GCR [1], called Page Bit) must be set to switch from the first 256 bytes to the rest of the RAM.

** For 68 pin package only. Memory address has 15 bits (MA14–MA0); 16th bit is accessed through $\overline{\text{CSROM}}$ and $\overline{\text{CSRAM}}$.

*** The ROMless SC11021 uses external ROM E000H–DFFFH for a total 32 kbytes. Also, the SC11022CV when used with external ROM disables the upper 8k internal ROM and addresses 32k external (Eng. version uses only 24k).

REGISTER DESCRIPTION

This section contains a description of each of the registers in the MAC device. All of the registers of the device are 8-bits with 16-bit addresses. The registers are made up of bits that are either inputs or outputs. Input bits are read-only (RO). Output bits are read/write (R/W). The state of an output may be read back by the processor.

Test Mode:

RAM locations 00H and 100H are reserved for test mode. User access is prohibited.

Serial Mode:

In parallel mode (CONF = 0) the functions of the UART registers are exactly the same as those in 16C450 UART. However in serial mode, (CONF = 1), the UART is turned around and controlled by the internal processor and it becomes a data set UART. The DTR, RTS, and OUT1 in MCR register becomes DSR, CTS, and RLSD outputs. The CTS, DSR in MSR register become $\overline{RTS}$, DTR input status from $\overline{RTS}$, $\overline{DTR}$ pins.

Note:

In serial version to echo SIN to SOUT after RESET and then go back to normal operation.

1) Set "SB" in LCR to "1".
2) Sample RDI in UART monitor register.
3) Set CM = $\overline{RDI}$ in the same register.
4) SOUT will be the same state as $\overline{CM}$.
5) Receiver is functioning, ignoring it.
6) After finishing all echoing, reset "SB" in LCR.
7) Update DLL, DLM, and set CM = 1 for normal operation.
8) Do a SET then RESET to RTRST bit to RESET RCV and TMR. Do a READ to LSR to clear LSR.
9) The UART is ready for normal operaton.

Register Address MAP

NAME	ABV	INTERNAL[3] INDIRECT ADDRESS[4]	INTERNAL[3] DIRECT ADDRESS[5]	INTERNAL[3] R/W	EXTERNAL[6] ADDRESS A [2:0]	EXTERNAL[6] R/W
UART Registers:						
Receive Buffer[1]	RBR	80H	180H	R/W	00H	RO
Transmit Holding[1]	THR	8AH	18AH	R/W	00H	WO
Interrupt Enable[1]	IER	81H	181H	R/W	01H	R/W
Interrupt ID	IIR	82H	182H	RO	02H	RO
Line Control	LCR	83H	183H	R/W	03H	R/W
Modem Control	MCR	84H	184H	R/W	04H	R/W
Line Status	LSR	85H	185H	R/W	05H	R/W
Modem Status	MSR	86H	186H	R/W	06H	R/W
Scratch Pad (8 bit)	STR	87H	187H	R/W	07H	R/W
Divisor Latch LSB[2]	DLL	88H	188H	R/W	00H	R/W
Divisor Latch MSB[2]	DLM	89H	189H	R/W	01H	R/W
UART Monitor	UMR	8BH	18BH	R/W		
Internal Registers:						
Switch Port	SWP	8DH	18DH	RO		
General I/O Port						
Direction Register	DIR	8EH	18EH	WO		
Data Register	DAR	8FH	18FH	R/W		
General Control	GCR	90H	190H	R/W		
TIMER	TIM	91H	191H	R/W		
Processor Status Byte	PSB	92H	192H	R/W		
Interrupt Control	ICR	93H	193H	R/W		

[1] DLAB bit (LCR [7]) must be zero for external access.
[2] DLAB bit (LCR [7]) must be one for external access.
[3] Register access through MA bus.
[4] 8-bit addresses for indirect addressing only, with Page bit (GCR [1]) used.
[5] 16-bit addresses for direct addressing only.
[6] UART register access through PC parallel system bus.

ACCESSIBLE REGISTERS

The system programmer may access or control any of the UART registers summarized in Table 1 via the CPU. These registers are used to control UART operations and to transmit and receive data. Their reset functions are summarized in Table 2.

Line Control Register (LCR, location 183H)

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 1 and are described in the following.

Table 1: Summary of Accessible Registers

	Register Address										
	0(DLAB=0)	0(DLAB=0)	(DLAB=0)	2	3	4	5	6	7	(DLAB=1)	(DLAB=1)
Bit No	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Iden. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	STR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSi)	0	Parity Enable (PEN)	Out 2 INT0 is High-Z when out2=0	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0, then the Parity bit is transmitted as a 1.

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has not effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Table 2. Summary of Accessible Registers

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0–3) forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low, Bit 3–7 are permanently Low
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	"All Bits Low, Except Bits 5 and 6 are High"
MODEM Status Register	Master Reset	"Bits 0–3 Low, Bits 4–7—Input Signal"
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read BRR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read RBR/MR	Low

Programmable Baud Generator

The UART contains a programmable Baud Generator that takes an internal clock of (3/32)(XTAL1) = 1.8432 MHz and divides it by any divisor from 1 to (2^{16}–1). The output frequency of the Baud Generator is 16 x the Baud [(divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on the initial load.

Table 3 illustrates the used of the Baud Generator with a crystal frequency of 19.6608 MHz. The accuracy of the desired baud rate is dependent on the crystal accuracy. Communicaiton software writing values to the divisor latches typically expects the input to the UART to be 1.8432 MHz. They will work correctly only if the MAC input clock is maintained at 19.6608 MHz.

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Error Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.4	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
57600	2	—

Line Status Register (LSR, location 185H)

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 1 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: The bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is used for factory testing.

Interrupt Identification Register (IIR, location 182H)

The UART has on-chip interrupt capability that allows for flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification

Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts change the IIR, even though they are recorded, until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 1 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 4.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register (IER, location 181H)

The 8-bit register enables the four types of interrupts of the UART to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 1 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Modem Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 1 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Interrupt Identification Register				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receiver Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (If source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: Out1. Auxiliary user-designated bit. It is connected to MSR[6] (RI) during local loopback.

Bit 3: Out 2. Auxiliary user-designated bit. It is connect to MSR[7] (DCD) during local loopback. When Out2 = 0, INTO pin is Hi-Z.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input: the four MODEM. Status Register bits CTS, DSR, DCD and RI are disconnected internally; and the four MODEM Control Register bits DTR, RTS, OUT1 and OUT2 are internally connected to the four MODEM Status Register inputs, and the MODEM Control output pins $\overline{RLSD}$, $\overline{CTS}$, $\overline{DSR}$ are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5–7: These bits are permanently set to logic 0.

Modem Status Register (MSR, location 186H)

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU in addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 1 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Read (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent of DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: this bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Scratchpad Register (STR, location 187H)

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

REGISTER DESCRIPTION

UART Monitor (UMR, location 18BH):

The UART Monitor register allows the processor to monitor UART operations. A read operation to the UART Monitor register will clear Bit 0 to Bit 4.

BIT	NAME	DESCRIPTION
7	RTRST	Reset receiver and transmitter. When set high both receiver and transmitter will be put into reset state.
6	CM	UART Command/Modem Output. When set HIGH the UART is placed in modem mode. At reset it is low, in command mode. This bit together with SB in LCR are used for bit by bit echoing. In serial version the user can set SB = 1 and CM = $\overline{RDI}$ to echo a bit. When CONF = 1 for normal operation set CM = 1.
5	RDI	Receive Data Input. This bit monitors the RXD input of the UART.
4	DLF	Divisor Latch Flag. This bit indicates if a new baud rate count has been written to the Divisor Latch.
3	LCF	Line Control Flag. This bit indicates if the line control register has been written.
2	TXF	Transmit Buffer Full Flag. This bit indicates if a new character is in the transmit shadow register.
1	RXF	Receive Buffer Empty Flag. This bit indicates if the last character has been read from the receive buffer.
0	MCF	Modem Control Flag. This bit indicates if the modem control register has been written.

Internal Registers:

Switch Port (SWP, location 18DH): for serial version only

The Switch Port is a 7-bit input port used only in the serial version of the MAC. It allows for reading of the external switches of a stand-alone modem. Only S0–S2 are available on the 44 pin SC11020CV.

BIT	NAME	DESCRIPTION
6–0	S 6–0	Switch Input. These bits monitor external switches.

General I/O Port (GIO)

Direction Register (DIR, location 018EH):

BIT	NAME	DESCRIPTION
7	Unused	N/A
6	Unused	N/A
5	Unused	N/A
4	Unused	N/A
3	DIR3	When HIGH, IO3 is an output. When LOW, IO3 is an input.
2	DIR2	When HIGH, IO2 is an output. When LOW, IO2 is an input.
1	DIR1	When HIGH, IO1 is an output. When LOW, IO1 is an input.
0	DIR0	When HIGH, IO0 is an output. When LOW, IO0 is an input.

REGISTER DESCRIPTION

General I/O Port (GIO) (Cont.)

Data Register (DAR, location 018FH):

BIT	NAME	DESCRIPTION
7	Unused	N/A
6	Unused	N/A
5	DAR5	This bit is routed to TDOUT pin when DAR4 is set HIGH.
4	DAR4	When set HIGH, DAR5 is output to TDOUT pin. When set LOW, SOUT or SIN is output to TDOUT pin when GCR bit 7 (CONF) is set LOW or HIGH respectively. See Figure 11.
3–0	DAR3–0	Output to IO3–0.

Timer (TIM, location 191H):

The Timer includes an 11 bit counter and a timer flip-flop. It is used to aid software timing functions. The counter is not readable. It can only be reset by a write. The timer flip-flop can be read to test if it is already set.

The counter and flip-flop will be reset on a write (value is don't care). After that the counter sends out a pulse train at 4.8 kHz rate to set the timer flip-flop. The flip-flop can be cleared on a read. The Timer is constantly counting by the internal clock CP (9.8304 MHz).

BIT	NAME	DESCRIPTION
0	TFF0	Timer flip-flop bit.

General Control Register (GCR, location 0190H):

GCR contains a miscellaneous set of control and status bits.

BIT	NAME	DESCRIPTION
7	CONF	Configuration output. This bit controls the state of the MAC configuration. When HIGH, the MAC is configured with the SERIAL interface. It is configured with the PARALLEL interface after a reset.
6	OH	Off Hook Output. When set HIGH, the phone will be placed off hook.
5	KDV	KDV Output. Data/Voice Relay Control. When high, the modem is in the voice mode.
4	MRDY	Modem ready.
3	AA	Active HIGH AA indicator. When high this bit sets the $\overline{AA}$ pin low.
2	HS	Active HIGH HS indicator. When high this bit sets the $\overline{HS}$ pin low.
1	PAGE	Register Page Bit. This bit selects the active register page. When LOW, the lower 256 registers are accessed during register operations and when HIGH, the upper page is active.
0	EA	Inverted external access enable status from $\overline{EA}$ pin. When on it is high. Low indicates $\overline{EA}$ is off.

COMMAND SUMMARY

Configuration & Async/Sync Commands

General:

COMMAND		DESCRIPTION
B	1	BELL/CCITT Protocol
E	1	Command Echo
L	2	Speaker Volume
M	1	Speaker Control
Qn	0	Quiet Command Reset Code
Sn=		Writing to S-Register
Sn?		Reading S-Registers
V	1	Enable Short-form Result Codes
X	4	Enable Extended Result Code Set
&J[1]		Telephone Jack Sel.*
&M[1]		Async/Sync Mode Sel.

Async/Sync Commands—International:

&G	0	Guard Tone Sel.
&P	0	Make/Break Dial Pulse Ratio Sel.

Async-Only Commands:

Y[1]	0	Enable Long Space Disconnect
&C	0	Data-Carrier-Detect (DCD) Options
&D	0	Data-Terminal-Ready (DTR) Options
&S	0	Data-Set-Ready (DSR) Options

Sync-Only Commands:

&R	0	Clear-to-Send (CTS)/Request-to-Send (RTS)
&X	0	Select Sync Transmit Clock Source

* See Figure 10 for Hardware Implementation.

All commands are compliant with Hayes 1988 AT commands. A detailed command set document is available on request. Check our bulletin board – (408) 263-8294.

[1] Not supported in SC11074,75 Sendfax controllers

COMMAND	DESCRIPTION

Immediate Action Commands:

A	Go OFF-Hook in Answer Mode
A/	Re-Execute Last Command
D	Dial Telephone Number
Hn	Switch Hook Control
O	Return to On-Line
Z[1]	Fetch Configuraton Profile from Nonvolatile Memory
&F	Fetch Factory Configuration Profile
&W[1]	Write Active Configuration Profile to Nonvolatile Memory
&Z[1]	Store Telephone Number

Dial Modifiers:

P	Pulse Dial
T	Touch-Tone Dial
R	Originate Call in Answer Mode
W	Wait for Dial Tone B/4 Continue to Dial
,	Delay a Dial Sequence
@	Wait for Quiet Answer B/4 Continue to Dial
!	Initiate a Flash
;	Return to Command State after Dialing
S=n	Dial A Stored Number (n=0 to 3)

Self Test and Diagnostics:

I/IO	Request Prod Code
I1/I2	ROM Checksum
I3	Manufacturer's I.D.
I4	Configuration Mode (Serial or Parallel)
&T[1]	Test Modes
I33	Sierra I.D.
RV[1]	Display Profiles & Register Settings

COMMAND SUMMARY (continued)

Sendfax Command Set Summary

COMMAND	DESCRIPTION

Sendfax:

#Bn	Speed Control n = 0 Reserved n = 1 Reserved n = 2 Reserved for V.23 n = 3 Reserved for V.23 n = 4 Fax Transmission Speed of 2400 bps n = 5 Fax Transmission Speed of 4800 bps n = 6 Fax Transmission Speed of 7200 bps n = 7 Fax Transmission Speed of 9600 bps
#En	Received frame Display Format Selection n = 0 Disable Display of Received HLDC Frames n = 1 Display Frame in Binary Format n = 2 Display Frame in 2 Digit ASCII Hex Format
#Fn	Mode Control n = 0 Return to Normal Modem Mode (300 to 2400 bps Data Rate) n = 1 Enter Fax Mode (19,200 bps Data Rate)
#Kn	DTE Flow Control n = 0 Disable Flow Control n = 3 Enable CTS Flow Control n = 4 Enable XON/XOFF Flow Control
#Pn	Number of Pages to Be Transmitted (n = 1 to 255)
#Rn	Resolution Control n = 0 Send Document with Normal Resolution n = 1 Send Document with Fine Resolution

Detailed current documentation on the command set is available from Sierra on request and may be downloaded from our bulletin board at (408) 263-8294,

Extensions to the Hayes AT command set for Sendfax mode operation are outline in this section. In order to accomodate these added commands in the 16K ROM space avilable, we eliminated some of the rarely used Hayes commands as indicated on the previous page.

General

1. All extended Sendfax commands start with the AT# prefix. This provides upward compatibility with future EIA command sets which will use the + symbol.

2. Fax mode assumes XON/XOFF or CTS flow control in data mode. &D2 command must be issued for DTR controlled abort.

3. Once the hardware enters the Fax mode, it will remain in the Fax mode (and accept commands at 19.2 kbps) until one of the following occurs:

a) software issues a #F request to return to command mode

b) a call disconnect frame is received

c) application software issues an abort command by dropping DTR

During the Fax session the hardware will report the status of the call with result codes. An action by the software may or may not be necessary depending on the response. All the normal Hayes result codes will also be reported.

Verbose	Digit	Usage
CED	a	Answertone detected
CFR	g	Remote machine confirmation to receive
CONNECT2400/FAX	w	Connection speed 2400 bps
CONNECT4800/FAX	x	Connection speed 4800 bps
CONNECT7200/FAX	y	Connection speed 7200 bps
CONNECT9600/FAX	z	Connection speed 9600 bps
CRC ERROR	e	Error in received frame
CRP	c	Repeat request
CSI	-	Remote machine identification
DCN	d	Disconnect
DIS	b	Remote machine capabilities frame
FTT	f	Failure to train
INVALID FRAME	i	Received frame is invalid
MCF	m	Message received OK
RTN	h	Message not received OK
RTP	j	Retrain positive

SC11019/SC11020/SC11021 SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

V_{CC} Supply Voltage	+6 V
Input Voltage	–0.6 V to V_{CC} +0.6 V
Storage Temperature Range	–65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range	0 to 70°C

DC ELECTRICAL CHARACTERISTICS: (T_A = 0 TO 70°C, V_{CC} = +5 V +10%)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I_{CC}	Nominal Operating Current @ V_{CC} = 5.5 V		40	75	mA
I_{CCPD}	Power Down Current @ V_{CC} = 5.5 V		8	15	mA
V_{IH}	High Level Input Voltage for TTL input pins for CMOS input pins	 2 0.8 V_{CC}			 V V
V_{IL}	Low Level Input Voltage for TTL input pins for CMOS input pins			 0.8 0.2 V_{CC}	 V V
VT+	Positive Hysteresis Threshold for RESET & /RI input pins		2.5		V
VT–	Negative Hysteresis Threshold for RESET & /RI input pins		1.8		V
V_{OH}	High Level Output Voltage for D7–D0, into @ I_{OH} = 8 mA for RDY—open collector for other output @ I_{OH} = 2 mA	0.7 V_{CC} +0.5			V
V_{OL}	Low Level Output Voltage for D7–D0, into pins @ I_{OL} = 8 mA for RDY @ I_{OL} = 8 mA for other output pins @ I_{OL} = 2 mA			0.3 V_{CC} –0.5	V
I_1	Leakage Current		±1	±20	µA
F_{CLK}	Crystal Clock Frequency		19.6608		MHz

TIMING DIAGRAMS

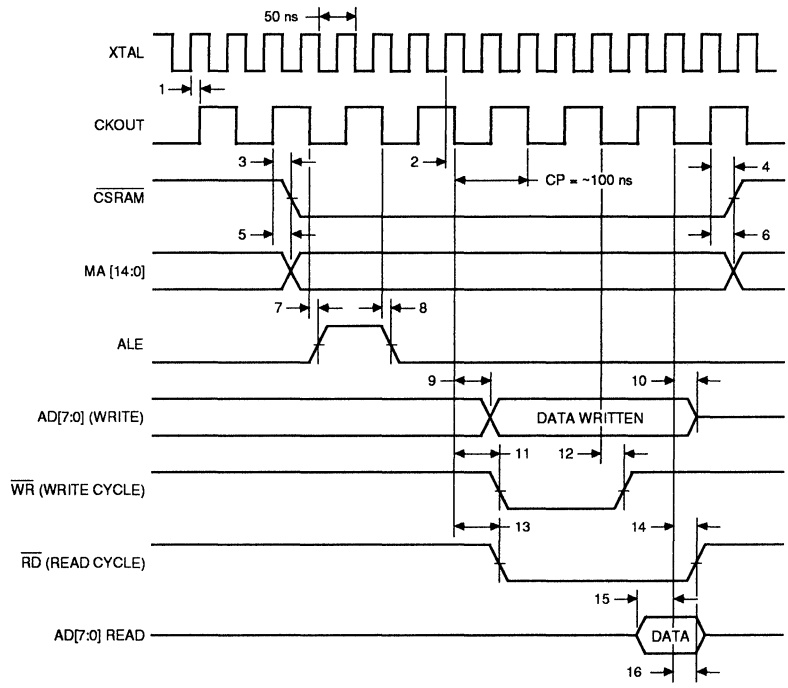


Figure 4. RAM Read or Write Cycle

RAM Read or Write Cycle Timing Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TXTHCH	XTAL high to CKOUT high				45	ns
2	TXTHCL	XTAL high to CKOUT low				45	ns
3	TCHCSL	CKOUT high to $\overline{\text{CSRAM}}$ low				25	ns
4	TCHCSH	CKOUT high to $\overline{\text{CSRAM}}$ high				25	ns
5	TCHMAV	CKOUT high to MA valid				25	ns
6	TCHMAI	CKOUT high to MA invalid				25	ns
7	TCLALH	CKOUT low to ALE high				15	ns
8	TCLALL	CKOUT low to ALE low				15	ns
9	TCLADV	CKOUT low to AD valid				35	ns
10	TCLADI	CKOUT low to AD invalid		5			ns
11	TCLWRL	CKOUT low to $\overline{\text{WR}}$ low				25	ns
12	TCLWRH	CKOUT low to $\overline{\text{WR}}$ high				25	ns
13	TCLRDL	CKOUT low to $\overline{\text{RD}}$ low				15	ns
14	TCLRDH	CKOUT low to $\overline{\text{RD}}$ high				15	ns
15	TADVCL	AD valid to CKOUT low (Read Set-up Time)		50			ns
16	TCLADI	CKOUT low to AD invalid (Read Hold Time)		0			ns

TIMING DIAGRAMS (Cont.)

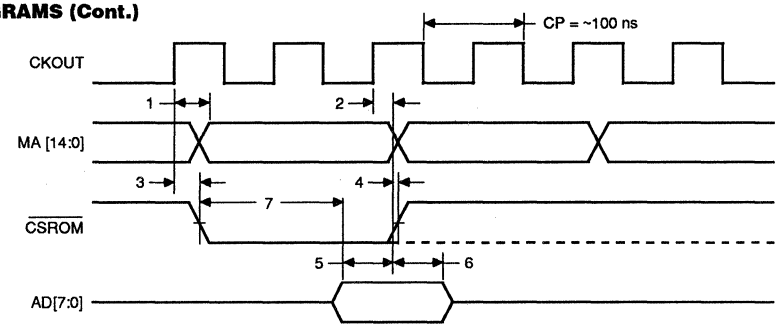


Figure 5. External Program Storage Read Bus Cycle

External Program Storage Read Bus Cycle Table

NO.	SYMBOL	PARAMETER	TEST COMMENTS	MIN	TYP	MAX	UNITS
1	TCHMAV	CKOUT high to MA valid				15	ns
2	TCHMAI	CKOUT high to MA invalid				15	ns
3	TCHCSL	CKOUT high to $\overline{\text{CSROM}}$ low	$\overline{\text{CSROM}}$ may already be low			15	ns
4	TCHCSH	CKOUT high to $\overline{\text{CSROM}}$ high	$\overline{\text{CSROM}}$ may not go high			15	ns
5	TADVCH	AD valid to CKOUT high		35			ns
6	TCHADZ	CKOUT high to AD high-Z		0			ns
7	TADRDA	$\overline{\text{RD}}$ valid to data valid				170	ns

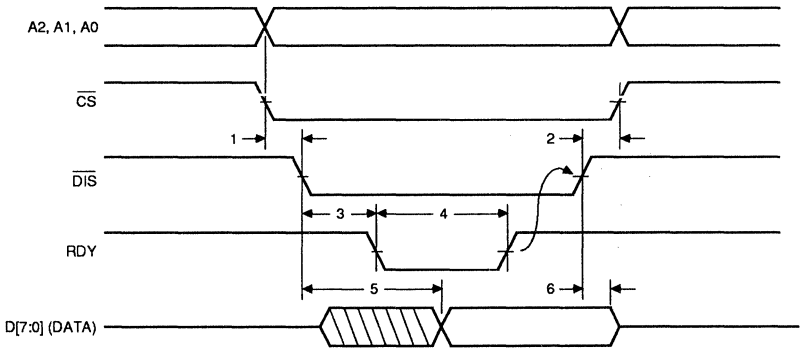


Figure 6. Read Cycle (PC Bus Read From UART Register)

Read Cycle (PC Bus Read From UART Register) Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDIL	$\overline{\text{CS}}$ low to $\overline{\text{DIS}}$ low				0	ns
2	TDIHCSH	$\overline{\text{DIS}}$ high to $\overline{\text{CS}}$ high				0	ns
3	TDILRDL	$\overline{\text{DIS}}$ low to RDY low				30	ns
4	TRDL	RDY low time (~5–6CP)		500		600	ns
5	TDILDV	$\overline{\text{DIS}}$ low to D valid				250	ns
6	TDIHDZ	$\overline{\text{DIS}}$ high to D high-Z				15	ns

TIMING DIAGRAMS (Cont.)

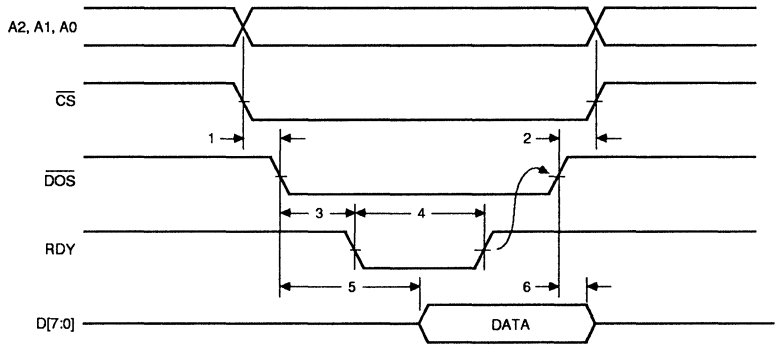


Figure 7. Write Cycle (PC Bus Write Into UART Register)

Write Cycle (PC Bus Write Into UART Register) Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDOL	$\overline{CS}$ low to $\overline{DOS}$ low				0	ns
2	TDOHCSH	$\overline{DOS}$ high to $\overline{CS}$ high				0	ns
3	TDOLRDL	$\overline{DOS}$ low to RDY low				30	ns
4	TRDL	RDY low time (~5–6CP)		500		600	ns
5	TDOLDV	$\overline{DOS}$ low to D valid				260	ns
6	TDOHDZ	$\overline{DOS}$ high to D high-Z		0			ns

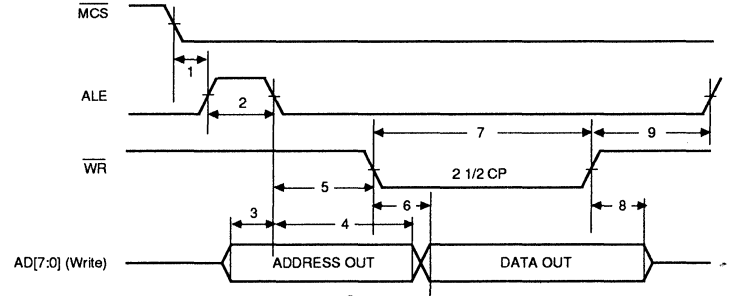


Figure 8. MAP and E^2 RAM Interface Write Cycle

MAP and E^2 RAM Interface Write Cycle Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TMCAL	$\overline{MCS}$ low to ALE high		10		20	ns
2	TALE	ALE pulse width		45			ns
3	TAVLE	Address valid to ALE low		30			ns
4	THAD	Hold address after ALE low		48			ns
5	TALRD	Delay from ALE low to $\overline{WR}$ low		45			ns
6	TDVRL	Data valid after $\overline{WR}$ low				25	ns
7	TWR	Write pulse width		230			ns
8	TDHWR	Data hold after $\overline{WR}$ high		30			ns
9	TWHLH	End of $\overline{WR}$ to next ALE		200			ns

When the SC11011 is reading or writing to the MAP, the address is valid at least 30 ns before ALE goes low and stays valid 48 ns or more beyond the trailing edge of ALE. When writing, data id valid within 25 sn afte WRn goes true and stays valid i=until at least 30 ns after WRn goes false

TIMING DIAGRAMS (Cont.)

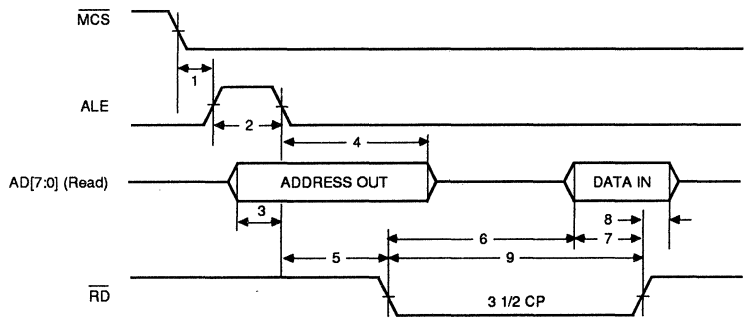


Figure 9. MAP and E²RAM Interface Read Cycle

MAP and E²RAM Interface Read Cycle Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TMCAL	$\overline{MCS}$ low to ALE high		10		20	ns
2	TALE	ALE pulse width		45			ns
3	TAVLE	Address valid to ALE low		30			ns
4	THAD	Hold address after ALE low		48			ns
5	TALRD	Delay from ALE low to $\overline{RD}/\overline{WR}$ low		45			ns
6	TDVRL	Data valid after RD low				300	ns
7	TDVRH	Data valid setup to $\overline{RD}$ high		15			ns
8	TDH	Data hold after $\overline{RD}$ high		0			ns
9	TRD	Read pulse width		330		370	ns

When reading from the MAP, data must be valid a maximum of 300ns after $\overline{RD}$ goes true and stays valid at least until 0ns after $\overline{RD}$ goes false.

CIRCUIT DIAGRAMS

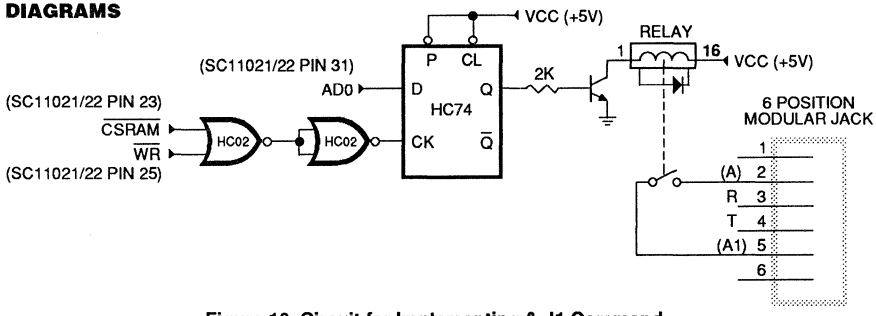


Figure 10. Circuit for Implementing & J1 Command

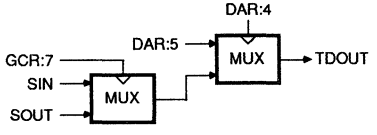


Figure 11. TDOUT Function

THE MAC AND INTEL 8096 SPEED COMPARISON

The attached is an instruction execution time comparison for the MAC and Intel 8096. The biggest improvement over 8096 is the 16 bit multiplication, it is 3.3 μs versus 6.5 μs. The jump instructions are twice as fast. The shift instructions are also about twice faster. The other arithmetic and logic instructions are about the same speed. Indirect addressing instructions in the MAC is about 20% slower than in the 8096.

The following comparison is for the 8096 with 12 MHz crystal and the MAC with 19.6608 MHz. The time unit is "μs". The instructions and operands are all from internal storage. Both the MAC and Intel 8096 will run slower for external storage access.

INSTRUCTION	OPERANDS	DIRECT MAC	DIRECT 8096	IMMEDIATE MAC	IMMEDIATE 8096	INDIRECT MAC	INDIRECT 8096
ADD	2	1.02	1.00	1.22	1.25	1.94	1.50
ADD	3	1.02	1.25	1.22	1.50	1.94	1.75
ADDB	2	1.02	1.00	1.02	1.00	1.94	1.50
ADDB	3	1.02	1.25	1.02	1.25	1.94	1.75
AND	2	1.02	0.75	1.22	1.25	1.94	1.50
AND	3	1.02	1.00	1.22	1.50	1.94	1.75
ANDB	2	1.02	1.00	1.02	1.00	1.94	1.50
ANDB	3	1.02	1.25	1.02	1.25	1.94	1.75
CMP	2	1.02	1.00	1.22	1.25	1.94	1.50
CMPB	2	1.02	1.00	1.02	1.00	1.94	1.50
DJNZ		0.92/1.25	1.25/2.25	(NO JUMP/JUMP)			
EXTB		0.71	1.00				
JBC		1.02/1.32	1.25/2.25				
JBS		1.02/1.32	1.25/2.25				
JC		0.51/0.82	1.00/2.00				
JE		0.51/0.82	1.00/2.00				
JGE		0.51/0.82	1.00/2.00				
JGT		0.51/0.82	1.00/2.00				
JH		0.51/0.82	1.00/2.00				
JLE		0.51/0.82	1.00/2.00				
JLT		0.51/0.82	1.00/2.00				
JNC		0.51/0.82	1.00/2.00				
JNE		0.51/0.82	1.00/2.00				
JNH		0.51/0.82	1.00/2.00				
JNV		0.51/0.82	1.00/2.00				
JV		0.51/0.82	1.00/2.00				
LCALL		1.12	3.25				
LD	2	1.02	1.00	1.22	1.25	1.94	1.50
LDB	2	1.02	1.00	1.02	1.00	1.94	1.50
LJMP	1	0.92	2.00	1.02	1.00	1.94	1.50
MUL	3	3.36	6.50	(BIGGEST IMPROVEMENT)			
NOP		0.24	1.00				
OR	2	1.02	1.00	1.22	1.25	1.94	1.50
ORB	2	1.02	1.00	1.02	1.00	1.94	1.50
PUSHF		0.51	2.00				
POPF		0.51	2.25				
RET		1.02	3.00				
SHL		1.12+0.10N	1.75+0.25N	(N = SHIFT COUNT)			
SHLB		1.12+0.10N	1.75+0.25N				
SHLL		1.53+0.10N	1.75+0.25N				
SHR		1.12+0.10N	1.75+0.25N				
SHRB		1.12+0.10N	1.75+0.25N				
SHRL		1.53+0.10N	1.75+0.25N				
SHRA		1.02+0.10N	1.75+0.25N				
SHRAL		1.53+0.10N	1.75+0.25N				
SJMP		0.71	2.00				
ST		1.32	1.75				
STB		1.32	1.75				
SUB	2	1.02	1.00	1.22	1.25	1.94	1.50
SUBB	2	1.02	1.00	1.02	1.00	1.94	1.50
SUB	3	1.02	1.25	1.22	1.50	1.94	1.75
SUBB	3	1.02	1.25	1.02	1.25	1.94	1.75
XOR	2	1.02	1.00	1.22	1.25	1.94	1.50
XORB	2	1.02	1.00	1.02	1.00	1.94	1.50

APPLICATIONS

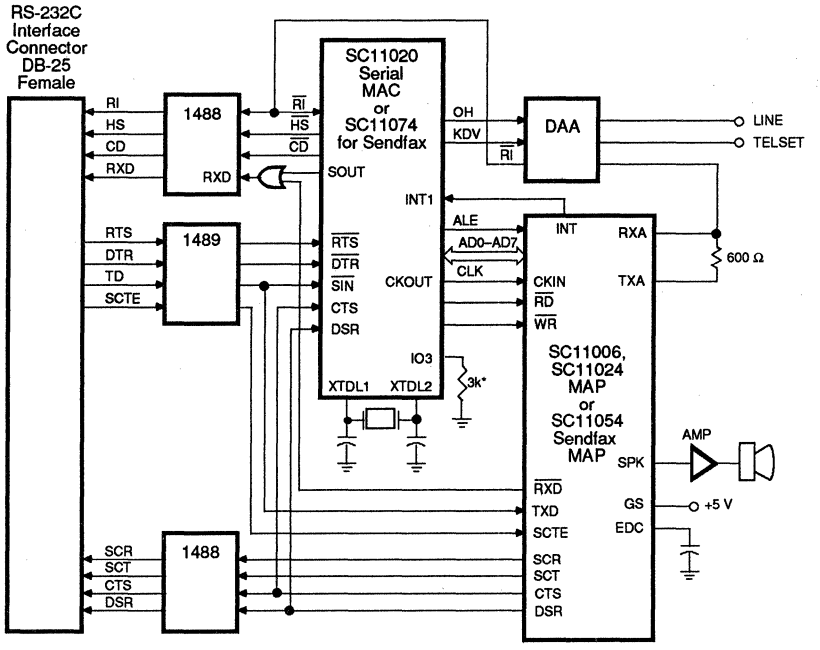


Figure 12. V22 bis Standalone Intelligent Modem with Internal ROM.

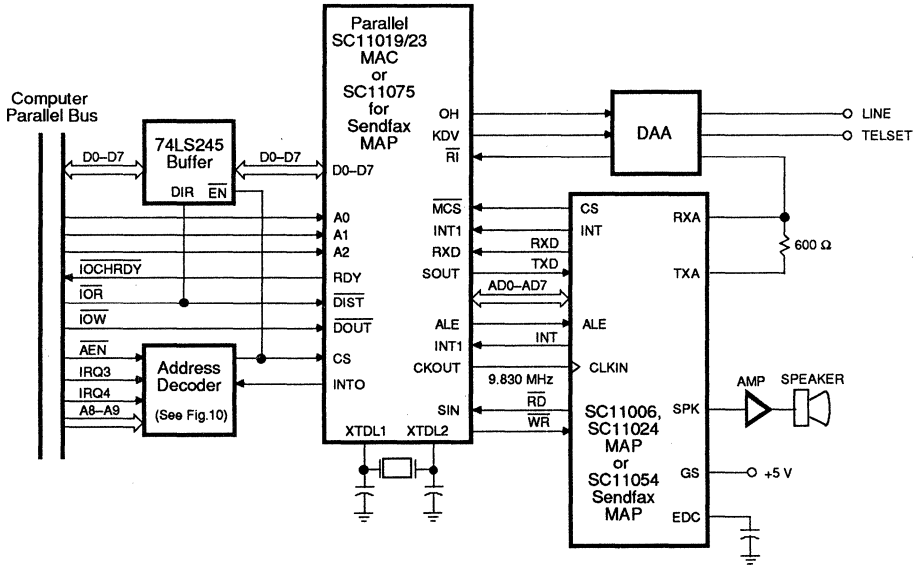


Figure 13. Internal Smart Modem for PC Bus Applications with Internal ROM.

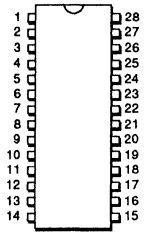
For additional application information, consult the MAP data sheets (SC11006, SC11024, SC11026, SC11046, SC11054 etc.).

Detailed firmware and schematic information is available through your local Sierra sales office and our BBS – (408) 263-8294.

FEATURES

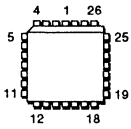
- ☐ Conforms to CCITT V.22 bis, V.22, V.21, and Bell 212A and 103 standards
- ☐ Single 5 V supply with 10 mW power down mode
- ☐ Analog, digital, and remote digital loopback
- ☐ Integrated DTMF/Guard Tone Generator, call progress monitor
- ☐ Contains an on-chip hybrid
- ☐ Programmable audio output
- ☐ CMOS technology

28-PIN DIP PACKAGE



SC11024CN

28-PIN PLCC PACKAGE



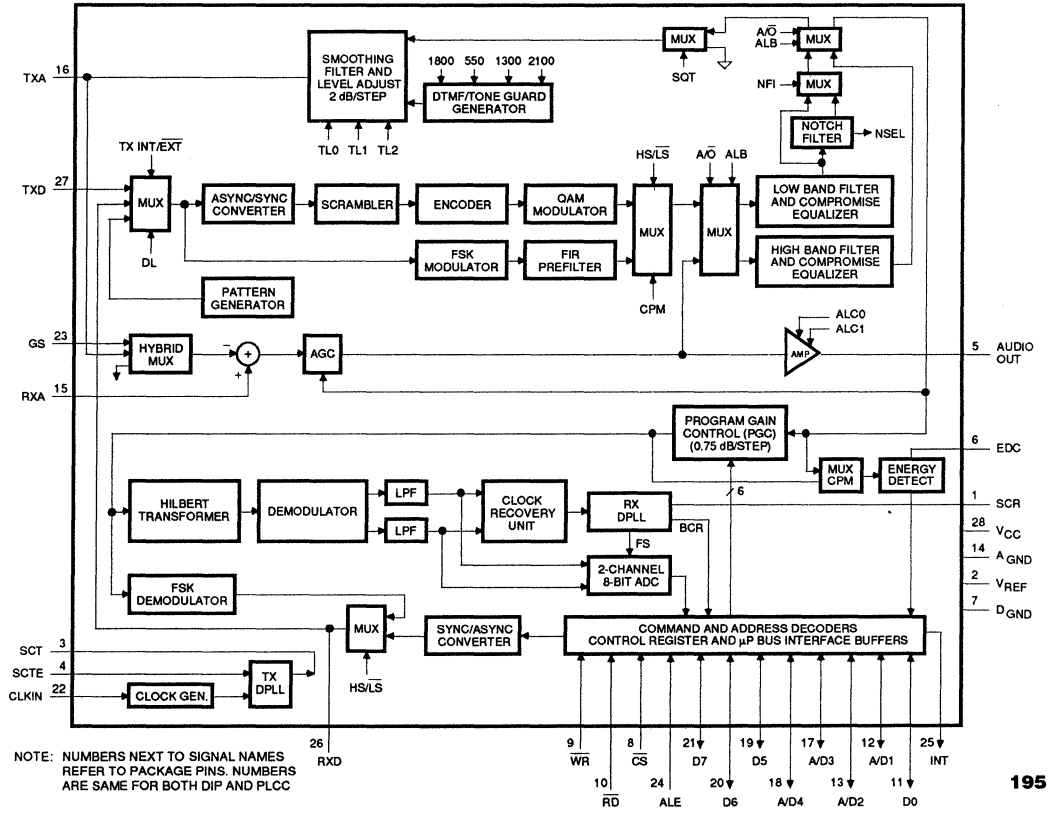
SC11024CV

GENERAL DESCRIPTION

The SC11024 is a complete 2400 bps 5 V only modem IC containing all modem functions except the adaptive equalizer. It is used in conjunction with an external controller, such as the Sierra SC11019 (for parallel bus applications), the SC11020 (for RS-232 applications), the SC11022 (for both configurations), SC11021, SC11061 or SC11091 ROMless controllers for customized firmware, to implement a 2400 bps full duplex modem, conforming to CCITT V.22 bis standards. The controller performs all modem control and handshaking functions as well as the adaptive equalization.

The SC11024 operates in 2400 bps QPSK/QAM and 1200 bps PSK as well as 0 to 300 baud FSK modes, compatible with Bell 103 and 212A as well as CCITT V.21, V.22, and V.22 bis standards. When used with the SC11019, SC11020 or SC11022 controllers, the SC11024 becomes an intelligent modem controlled by the industry standard "AT" command set. The interface between the SC11024 modem and the controller is a standard microcontroller interface that easily connects to the SC22201 (128 by 8) EE memory for permanent storage of configuration settings and phone numbers.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE SAME FOR BOTH DIP AND PLCC

FUNCTIONAL DESCRIPTION OF THE SC11024 MODEM

The SC11024 includes:

- ☐ Full transmitter consisting of
  - Async to Sync converter
  - Scrambler
  - Data encoder
  - 75% square root of raised cosine pulse shaper
  - Quadrature modulator
  - FSK (Bell 103 and CCITT V.21) modulator
  - Hybrid
- ☐ High band and low band filters
- ☐ High band and low band compromise equalizers
- ☐ V.22 notch filter (selectable at 550 or 1800 Hz)
- ☐ Transmit smoothing filter
- ☐ Programmable attenuator for transmit level adjust
- ☐ DTMF, 550 Hz, 1300 Hz, 1800 Hz, and 2100 Hz tone generator
- ☐ Transmit clock circuit for synchronous operation (slave, external, and internal modes)
- ☐ Pattern generator for generating fixed digital patterns in handshaking mode
- ☐ Receive section consisting of
  - 64-step programmable gain controller (PGC)
  - Energy detector at the output of the PGC
  - Hilbert transformer
  - Quadrature demodulator (free running carrier) with low pass filters
  - Baud timing recovery circuit (sampling clock of 600 Hz)
  - FSK demodulator
  - Sync to Async converter
- ☐ 8-bit analog to digital converter (ADC)
- ☐ Control and Status registers
- ☐ 8-bit microprocessor interface with interrupt and multiplexed address/data lines
- ☐ Audio output with level adjust

Transmitter

Since data terminals and computers may not have the timing accuracy required for 2400/1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 2400/1200 Hz +2.3%, –2.5%. It outputs serial data at a fixed rate of 2400/1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 2400/1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first four/two stages of the shift register form the quad/dibit that is applied to the QAM/QPSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band, centered at 2400 Hz, or the low band, centered at 1200 Hz. In the 2400 bps mode, the modem actually sends four bits at a time, called a quadbit. The actual rate of transmission for a quadbit is 600 baud. This is the optimum rate of transmission over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

In the 2400 bps data rate, the data to be transmitted is divided into groups of four consecutive bits (quadbits). The first two bits of the quadbit are encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. The last two bits define one of the four signaling elements associated with the new quadrant.

In the 1200 bps data rate, the data stream is divided into groups of two consecutive bits (dibits). The dibits are used to determine the phase quadrant change relative to the quadrant occupied by the preceding signal element. The resulting signaling elements from the inphase (I) and quadrature (Q) channels are passed through baseband filters with a square root of raised cosine shape. The filtered signals subsequently modulate sine and cosine carriers, and add to form the QAM/QPSK signal. The wave-shaped signal is then passed through either the low-band or high-band filter, depending upon originate or answer mode selection.

For low speed operation, the FSK modulator is used. It produces one of four precision frequencies, depending upon originate or answer mode selection and the 1 (mark) or 0 (space) level of the transmit data. Different frequencies are used for V.21 and 212A modes. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands, and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.22 bis applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress

monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode, it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second-order low-pass switched-capacitor filter that adds the modem transmit signal to the V.22 guard tones. It also provides a 2 dB per step programmable gain function to set the output level.

Receiver

The receiver section consists of an energy detector, programmable gain control (PGC), part of the QAM/QPSK demodulator, FSK demodulator, 8-bit ADC and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to the energy detector and PGC circuit. The energy detector provides detection within 17 to 24 msec. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels. In call progress mode, the energy detector is connected to the output of the PGC to allow detection level adjustment.

The output of the receive filter is applied to the programmable gain control (PGC). This circuit has a wide overall range of 47.25 dB and provides 64 steps of 0.75 dB/step. The PGC gain is controlled by the external processor. It also provides auto-zeroing to minimize the output DC offset voltage.

The QAM/QPSK demodulator uses a coherent demodulation technique. Output of the programmable gain control (PGC) is applied to a Hilbert transformer that produces an in-phase and 90° out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by a free-running carrier. The baseband components are low-pass filtered to produce I and Q (Inphase and Quadrature) channel outputs. The I and Q channel outputs are both filtered by 300 Hz band-pass filters. Then they are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled and digitized into 8-bit samples by the ADC. Each channel (I and Q) is sampled twice during a baud period, once at the middle and once at the end of the baud period, allowing T/2 or T sampling operation. The external processor is interrupted once every baud period (1.667 msec). The processor should read the I and Q samples (within 100 µs from the time interrupt is issued), and perform adaptive equalization, carrier phase tracking, data decoding, and data descrambling. One quad/dibit is transferred from the SC11024 during each baud period.

In the asynchronous mode, data received from the processor is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are re-inserted. Underspeed data is passed essentially unchanged. The sync/async converter has two modes of operation. In the basic signaling mode, the buffer can accept an overspeed which corresponds to one missing stop bit in eight characters. The length of the start bit and data elements will be the same, and the stop bit will be reduced by 12.5%. In the extended-signaling range, the buffer can accept one missing stop bit in four characters and the stop bits will be reduced by 25% to allow for overspeed in the transmitting terminal. Output of the sync/async converter, along with the output of the FSK demodulator, is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed and output data received on the RXD pin.

For low-speed operation, the FSK demodulator is used. The output of

the PGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

To improve the performance of the receiver at low signal levels, while maintaining a wide amplitude range, a 1-bit AGC circuit is placed prior to the band-pass filter. The decision thresholds of this AGC are controlled by the AGCVT bit. When AGCVT = 1, the thresholds will be 6 dB further apart than when AGCVT = 0, so that the probability of gain change will be reduced. The status of the AGC gain is available through the AGCO bit. AGC will have 8 dB more gain when AGCO = 1. Status of AGCO should be monitored at every baud timing period and when it makes a transition (causing a gain-hit) the PGC's gain shouldbe modified accordingly to prevent divergence of the adaptive equalizer.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, by turning the "Hybrid" code on through the interface, this matching is provided by an external resistor connected between the TXA and RXA pins on the SC11024. The filter section provides sufficient attenuation of the out-of-band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter. The hybrid can be deactivated by the controller.

The SC11024 internal hybrid is intended to simplify the phone line interface. The internal hybrid can compensate for the loss in the line coupling transformer used in the DAA. By tying the GS pin to AGND, V_{REF} or V_{CC}, compensation levels of 0, +2, +3 dB, respectively are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. An external hybrid circuit, shown in Figure 2, can be used to overcome these losses and achieve maximum performance. In this case, the internal hybrid must be turned off by setting bit 6 of the TXCR register to 0.

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC11024 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired value. In practice, however, there is impedance mismatch and a loss in the coupling transformer. Therefore, it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain (G_R) and transmit gain (G_T) are set by the ratios of resistors R2, R1 and R6, R5, respectively (Figure 2).

The circuit can be analyzed as follows:

$$V_R = -\frac{R2}{R1}(V_{TR}) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)V_y$$

$$V_y = -\frac{R6}{R5}V_x$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_y = 2V_{TX}$,

$$V_R = -\frac{R2}{R1}(V_{TX}+V_{RX}) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)2V_{TX}$$

$$= -\frac{R2}{R1}V_{RX} + \left[\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}$$

Solving for R3/R4:

$$\frac{R3}{R4} = 1 + \frac{2R1}{R2}$$

Additionally,

$$G_R = \frac{R2}{R1} \text{ and } G_T = \frac{R6}{R5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive loss in the coupling transformer is 2.5 dB, then:

$$\frac{R2}{R1} = \text{INV Log}\left(\frac{G_{RdB}}{20}\right) = \text{INV Log}\left(\frac{2.5}{20}\right) = 1.333$$

Similarly, $\frac{R6}{R5} = 1.333$ and $\frac{R3}{R4} = 2.5$

Some typical values are:

R1=20KΩ, R2=27KΩ, R3=13KΩ, R4= 5.1KΩ, R5=20KΩ, and R6=27KΩ

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6, and capacitor C1 can be eliminated, and point X can be connected to point Y in the circuit of Figure 2 to achieve a more cost effective external hybrid arrangement.

The SC11024 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, the "Hybrid" code must be turned off. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

The tone generator section consists of a DTMF generator, V.22 guard-tone, and 1300 and 2100 Hz tone generators. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and A, B, C, D, *, and # keys. The V.22 guard-tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the tone control register. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to 1300 and 2100 Hz and the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50K Ohms is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation—no attenuation, 6 dB attenuation, 12 dB attenuation, and squelch are provided through the ALC1 and ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Clock Input

CLKIN (Pin 22) of the SC11024 should be connected to a 9.8304 MHz clock source with an accuracy of ±0.01%.

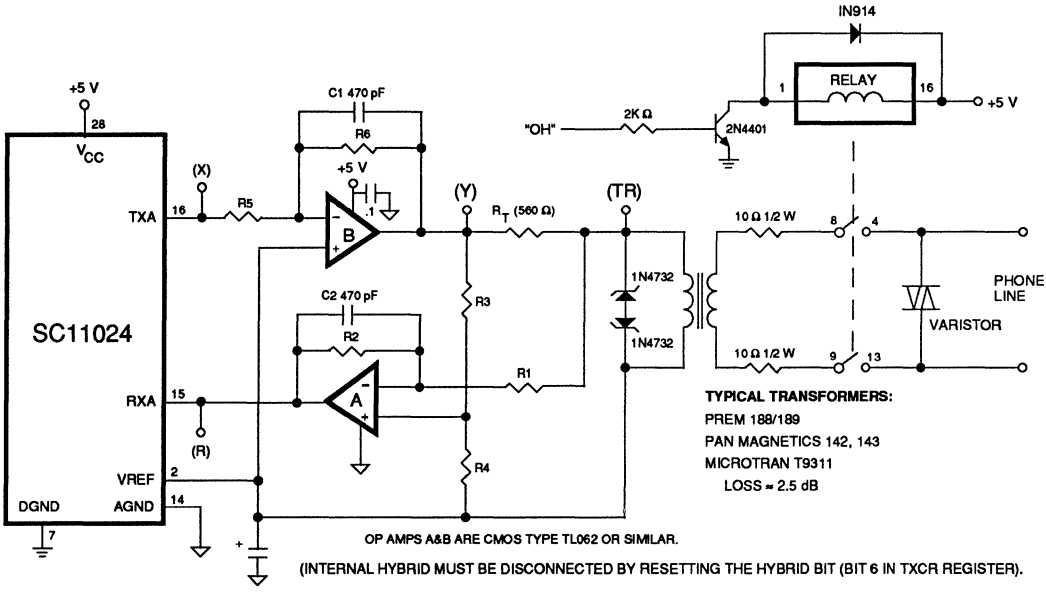


Figure 2. Using an External Hybrid with the SC11024

FUNCTIONAL DESCRIPTION OF THE SC11019 AND SC11020 CONTROLLERS

The SC11019 modem controller, implemented in Sierra's proprietary CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including a 16-bit microprocessor, 16K bytes of ROM and 320 bytes of RAM, it also contains the functionality of a 16C450 UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem for the PC consists of the SC11019 controller, the SC110024 modem and the DAA. All of the popular communications software written for the PC will work with the SC11024/SC11019 set.

Another version of the controller, the SC11020, is intended for RS-232 applications. It contains the same processor, memory, and UART as the SC11019 and has the same interface to the modem chip. The difference is that the UART is turned around so that the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The controller receives an 8-bit signal sample from the SC11024 and performs adaptive equalization, carrier phase recovery, data decode, and descrambling. SC11019 and SC11020 have identical hardware. Each controller can be configured as an SC11019 or SC11020 by the software. The controller is designed by using a 16-bit 2900-type bit slice processor to perform the digital signal processing and the control functions. Its instruction set is a subset of the Intel 8096 instruction set, which operates faster than the 8096.

The SC11020 provides a standard 5V logic level interface—RS-232 drivers are required to interface to the port. Like the SC11019, the SC11020 comes programmed with the Hayes "AT" command set, and when used with the SC11024 modem, emulates a Hayes-type stand-alone modem. The SC11019 and SC11024 emulate a Hayes-type IBM PC plug-in card modem.

But the chip set is by no means limited to implementing a Hayes-type smart modem. Sierra is in the custom IC business and both chips were designed with this in mind. For example, only about 15 kbytes of the SC11019's ROM is used for the handshaking and smart modem code, leaving 1 kbytes for additional features that a customer may specify. And since the controller is ROM programmable, any command set, not just the Hayes "AT" set, can be implemented.

Both the SC11019 and SC11020 are available in two pinout options. They are 48 pin DIP, and 44 pin PLCC. The 44 pin version of SC11019 is programmed to support a different modem (SC11006) and is not recommended for use with SC11024. The 44 pin version programmed for SC11024 is SC11023CV.

The SC11021 is a ROMless version of the SC11019 & 20. It is available in a 68 pin PLCC and operates with up to 32k external ROM. It can be configured for either serial or parallel operation.

A fourth version, SC11022, is available in 48 pin DIP and 68 pin PLCC. This version can be configured as either a serial or a parallel modem and in the 68 pin package, it can also address up to 24k external ROM.

Please refer to the SC11019 series data sheet for complete details on controller features and performance characteristics.

Both the controllers require +5 V power supply. Besides the interface for the SC11024 modem, the SC11019 controller has an eight-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 16C450 UART. It also has control lines for ring indication, the off-hook relay, and a data/voice relay; these lines connect to the DAA.

In the SC11020, the eight-bit port becomes the switch input lines, and I/O port, and the address, chip select, INTO, DIST and DOST lines become the lines for the RS-232 interface, and modem status. These lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control—so the main difference between the SC11019 and SC11020 is the ROM code. It also contains the same modem and DAA interface lines as the SC11019.

The interface to the SC11024 is via an 8-bit address/data bus and the control lines for read and write. The same interface is used for access to an electrical erasable random access memory (SC22201). There are six clock multiplexed address/data bus cycles. A ready signal is provided for the interface to a high speed PC-AT type bus cycle. For the 68 pin packages, there are 15 extra address lines and chip selects for external ROM and external RAM interfaces. An $\overline{EA}$ pin is also available for selection of internal ROM or external ROM.

The SC11019 and SC11020 are truly ASIC controllers—they are designed to control a modem or other peripheral that operates at a moderately slow data rate up to 2400 bits per second. What's unique about the SC11019, for example, is that it allows a slow peripheral to interface to a high speed bus without making the main processor add unnecessary wait states

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11019 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up, it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like a Hayes-type modem. The escape sequence is three + signs—+++ —in the default mode, but it can be changed in the software.

The actual processor contains a 16-bit data path and can execute 54 instructions with three different addressing modes: direct, indirect, and immediate. There is 16K by 8 of ROM on the chip for program storage.

To the system bus, the SC11019 looks and acts like a 16C450 UART. Communications software written for this UART will work with the SC11019 and SC11020. The Sierra chip set is truly a Hayes-type modem in two chips.

THE SC11024 & SC11019/SC11020 SYSTEM

The only external components required by the SC11024 are a 560 Ohm line matching resistor and a 1.0 μF capacitor from the EDC pin to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11024 can directly drive a high impedance (50 kΩ) earphone-type transducer.

The SC11024 modem's CLKIN pin line is driven by the SC11019 CKOUT line at 9.8304 MHz. The SC11019 interfaces directly to an IBM PC bus. External parts required will be an LS245 to drive the bus and an LS30 and L804 for COM1/COM2 decoding. A ready signal is provided to control the IOCHRDY pin on the bus to allow operation with higher speed computers (AT, XT TURBO, etc.)

For tone dialing, the controller sends a code to the modem chip which in turn puts out the required DTMF tones on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they can't delay dialing until a dial tone is detected.

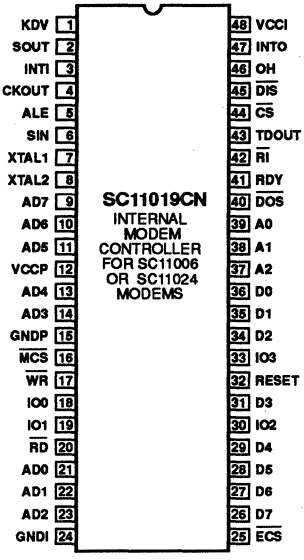
All modems require a DAA. A DAA or data access arrangement is a line interface required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω; a relay for disconnecting the modem from the line; a ring detector, typically an optoisolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by one of many consultants and labs around the country. The fee is typically $2,000 and it takes several weeks. Another alternative is to buy an approved DAA, supplied by several manufacturers. This covers part 68 of the FCC spec, but the modem will still be required to pass part 15 radiation tests.

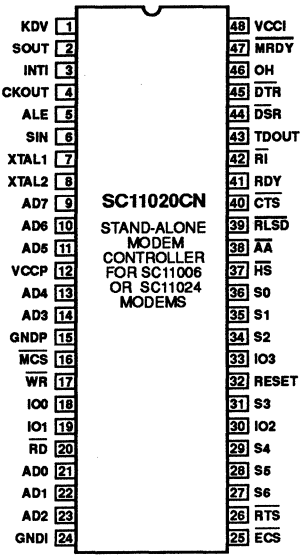
V.22bis is a CCITT specification that calls for 2400 bps, full or half duplex data transmission with a fallback mode of 1200 bps. It is not 2400 baud; the spec calls for transmission of quadbits—4 bits per baud so the 2400 bps transmission takes place at 600 baud. The same is true for V.22—it is 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; there is a CCITT standard for 300 bps and that's V.21.

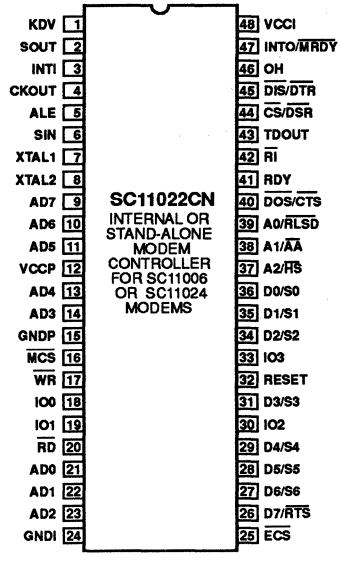
V.22 and V.22bis also call for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The SC11024 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone in the receiver.

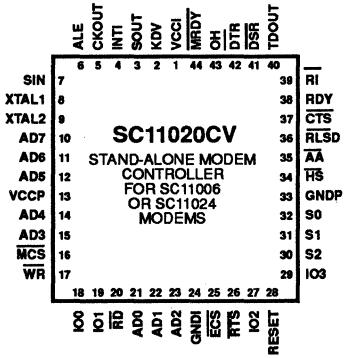
All modems require a Hybrid; a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them for the phone line. In the SC11024, this is done with on-chip op amps. The internal hybrid can be disabled so an external hybrid can be used, if desired.

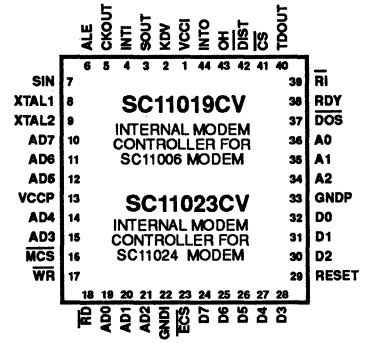
CONNECTION DIAGRAM FOR CONTROLLERS

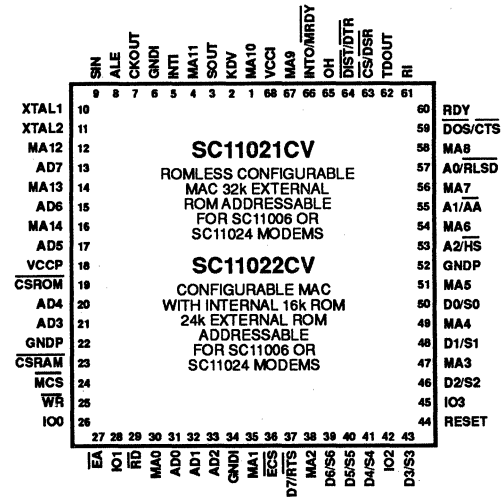












PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	SCR	Synchronous Clock Receive (Data set source); Output; TTL; Used only in bit synchronous mode; Recovered by the Receiver Phase Locked Loop from the far end modem. Data on RXD is valid at the rising edge of this clock.
2	V_{REF}	Reference Ground; Generated inside the chip and is equal to $V_{CC}/2$.
3	SCT*	Synchronous Clock Transmit (Data set source); Output; TTL; Used only in bit synchronous mode; Generated internally by the SC11024 Clock Generator; Rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
4	SCTE	Synchronous Clock Transmit External (DTE source); Input; TTL; Used only in bit synchronous mode; Data on TXD line is latched by the SC11024 at the rising edge of this clock. Clock rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
5	AUDIO	Audio output; The hybrid output is passed through a programmable attenuator and fed to this analog pin. Four different levels can be attained by controlling bit 0 and bit 1 of the AUDIO register as specified under AUDIO register description.
6	EDC	Capacitor for energy detect; A 1.0 µF capacitor should be connected between this pin and AGND.
7	DGND	Digital ground
8	$\overline{CS}$	Chip Select; Input; TTL; Active low.
9	$\overline{WR}$	Write; Input; TTL; Normally high; Data on AD7–AD0 is written into the SC11024 registers at the rising edge of this pulse.
10	$\overline{RD}$	Read; Input; TTL; Normally high; Data on AD7–AD0 is to be read by the processor at the rising edge of this pulse.
12,13,17,18	AD1–AD4	Multiplexed address/data bus (8-bits); Input/Output; TTL; A/D4–A/D1 (4-bits) are used for multiplexed addressing of internal registers.
14	AGND	Analog Ground
15	RXA	Receive analog; Input
16	TXA*	Transmit analog; Output
11,19–21	D0, D5–D7	Bits 0, 5, 6 and 7 are don't cares as far as address is concerned.
22	CLKIN	Clock input; 9.8304 MHz clock input from the controller.
23	GS	Gain Select to compensate for loss in line coupling transformer. When left open or tied to AGND, the compensation is 0 dB; connected to VREF, +2 dB compensation is provided; And when tied to V_{CC}, the compensation is +3 dB.
24	ALE	Address Latch Enable; Input; TTL; The address on A/D4–A/D1 is latched into the SC11024 Address decoder at the falling edge of this normally low pulse.
25	INT	Interrupt; Output; TTL; Normally low; A short (13 µs typical) positive pulse is generated after all A to D conversions are completed.
26	RXD*	Received Data; Output; TTL
27	TXD	Transmit Data; Input; TTL
28	V_{CC}	+5 V supply

* 1.6 nA drone

REGISTERS

There are twelve 8-bit registers interfacing to the microprocessor bus. Five of these registers can only be read by the processor (called READ registers) and the remaining seven can be written into by the processor (called CONTROL registers). Bit 1 of the "Tone" register can be read and written by the processor, Table 1 shows the address and bit assignments for these registers.

A chip select pin is provided for multi-peripheral addressing by the processor.

Table 1. READ Registers

ADDRESS BITS				NAME	MSB			BIT NUMBER				LSB
A4	A3	A2	A1		7	6	5	4	3	2	1	0
0	0	0	0	Q1	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
0	0	0	1	I1	I17	I16	I15	I14	I13	I12	I11	I10
0	0	1	0	Q2	Q27	Q26	Q25	Q24	Q23	Q22	Q21	Q20
0	0	1	1	I2	I27	I26	I25	I24	I23	I22	I21	I20
0	1	0	0	Status	X	X	X	AGCO	PA	PR	FSKD	ED
0	1	X	1	Unused		Unused						
0	1	1	X	Unused		Unused						

STATUS Register: Address (A4–A1) = 0100

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–5	Unused	
Bit 4	AGCO	Status of internal 1-bit AGC. When this bit is set, RXA signal is amplified by 8 dB before entering the bandpass filters.
Bit 3	PA	This bit is set whenever the clock recovery DPLL advances one step (skips a count) to lock. It is cleared only when STATUS register is read.
Bit 2	PR	This bit is set whenever the clock recovery DPLL retards one step (adds an extra count) to lock. It is cleared only when STATUS register is read.
Bit 1	FSKD	Received FSK data. FSKD = 1 when mark is received.
Bit 0	ED	Energy detect circuit output. ED = 1 when energy detected.

Note 1: When DPLL neither advances nor retards, then PA = PR = 0.
Note 2: When reading unused bits, the corresponding bus lines will not be driven by the SC11024 and will be floating.

Table 1a. READ Registers

Q1 Register:	Stores midbaud inphase sample output of ADC.
I1 Register:	Stores midbaud quadrature sample output of ADC.
Q2 Register:	Stores endbaud inphase sample output of ADC.
I2 Register:	Stores endbaud quadrature sample output of ADC.

Note: All samples are represented in two's complement form.

Table 2. CONTROL Registers

ADDRESS BITS				NAME	BIT NUMBER							
A4	A3	A2	A1		7	6	5	4	3	2	1	0
1	0	0	0	TXCR	X	HYBRID	TXSEL2	TXSEL1	TXSEL0	SQT	BR1	BR0
1	0	0	1	MCRA	X	LCK/$\overline{INT}$	RNGX	SYNC	WLS1	WLS0	A/$\overline{O}$	RXMRK
1	0	1	0	MCRB	X	PD	X	CPM	ALB	TL2	TL1	TL0
1	0	1	1	TONE	X	HNDSHK	TONEON	DTMF	D3	D2	D1	D0
1	1	0	0	PGCR	X	AGCVT	G5	G4	G3	G2	G1	G0
1	1	0	1	DATA	X	PLLJAM	PLLFRZ	PLLFAST	RD3	RD2	RD1	RD0
1	1	1	0	AUDIO	X	DISS	PGCZ	TST2	TST1	TST0	ALC1	ALC0
1	1	1	1					UNUSED				

Transmit Control Register (TXCR): Address (A4–A1) = 1000

(Note: When writing into these registers, the bus lines corresponding to the unused bits are ignored by the SC11024.)

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	HYBRID	When set, the transmitter output (TXA) is connected to the inverting input of the receive buffer to allow the use of the on-chip hybrid circuit for 2 to 4 wire conversion.
Bit 5 Bit 4 Bit 3	TXSEL2 and TXSEL1 and TXSEL0	Transmit Select bits. These 3 bits determine the data transmitted by the transmitter according to the following table:

TXSEL2	TXSEL1	TXSEL0	TRANSMITTED DATA
0	0	0	External data sent by DTE.
0	0	1	Unscrambled S1 (Note 1).
0	1	0	Unscrambled Space.
0	1	1	Unscrambled Mark.
1	0	0	Scrambled RX. Digital loop back mode (Note 2).
1	0	1	Scrambled Reversals (Notes 3 and 4).
1	1	0	Scrambled Space (Note 4).
1	1	1	Scrambled Mark (Note 4).

Note 1: S1 is a pattern of 0011 transmitted at 1200 bps rate regardless of BR1. If in FSK mode (BR0 = 1), then reversals are sent. This pattern cannot be sent at 2400 bps rate.

Note 2: In this mode, the received data, after being descrambled, is sent back to the scrambler. The modem will automatically go to the Synchronous mode with Slave timing.

Note 3: Reversals are continuous streams of 01.

Note 4: When in FSK mode (BR0 = 1), TXSEL2 is ignored since scrambling is not applicable.

Bit 2	SQT	When this bit is set, the transmitter is squelched by connecting the output of MUX1 (see the block diagram) to V_{REF}.
Bit 1 Bit 0	BR1 and BR0	Bit Rate Selection bits based on the following table:

BR1	BR0	BIT RATE
0	0	2400 bps V.22 bis
1	0	1200 bps V.22/212A
0	1	0–300 bps Bell 103
1	1	0–300 bps CCITT V.21

CONTROL REGISTERS (Cont.)

Mode Control Register A (MCRA): Address (A4–A1) = 1001

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	unused	
Bit 6	LCK/INTB	Determines the clock source for the transmitter. When this bit is set, the clock source is externally provided on SCTE (pin 4), and when cleared, it is internally generated (SCT). This bit can select the clock source independent of Sync/Async mode selection (see below). When in Digital Loop-Back mode, the clock source will be forced to the Slave mode (SCR).
Bit 5	RNGX	Range extender for the receiver Sync/Async converter. When set, the receiver Sync/Async can insert up to one stop bit per four (8, 9, 10 or 11-bit) characters to compensate for a far end DTE being up to 2.3% over speed. The transmitter Async/Sync always handles this overspeed condition regardless of this bit's condition.
Bit 4	SYNC	When set, operate in bit synchronous mode; when clear, operate in character asynchronous mode. When in Digital Loop-Back mode, the SC11024 will be forced to the Synchronous mode.
Bit 3 and Bit 2	WLS1 and WLS0	Word length select bits in asynchronous mode, according to the following table:
Bit 1	A/$\overline{O}$	When set, operate in answer mode; when clear, operate in originate mode.
Bit 0	RXMARK	When set, the RXD pin is clamped to the high logical level.

WLS1	WLS0	NUMBER OF BITS PER CHARACTER
1	0	8
1	1	9
0	0	10
0	1	11

Mode Control Register B (MCRB): Address (A4–A1) = 1010

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	unused	
Bit 6	PD	When this bit is set, chip will be powered down. When cleared, chip will go into normal power mode.
Bit 5	unused	
Bit 4	CPM	Call progress monitor mode. When set, the receive path can be connected to the high band filter to detect answer tone (ALB=0) or to the low band filter scaled down 2.5 times (ALB=1) to listen for the call progress tones during auto dialing.
Bit 3	ALB	Analog Loop Back. When set, the transmitter output (TXA) is connected to the receive path, bypassing the receive filter.
Bit 2 and Bit 1 and Bit 0	TL2 and TL1 and TL0	Transmit level adjust bits based on the following table:

TL2	TL1	TL0	TRANSMIT LEVEL AT TXA PIN
0	0	0	–3 dBm
0	0	1	–5 dBm
0	1	0	–7 dBm
0	1	1	–9 dBm
1	0	0	–11 dBm
1	0	1	–13 dBm
1	1	0	–15 dBm
1	1	1	–17 dBm

CONTROL REGISTERS (Cont.)

TONE Register: Address (A4–A1) = 1011

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	HNDSHK	This bit is set only during handshaking sequence. When set, both FSK and PSK/QAM demodulators are enabled. When cleared, FSK demodulator is disabled when in high speed mode.
Bit 5	TONEON	When set, the output of the tone generator appears at TXA. When cleared, the output of the tone generator is squelched.
Bit 4	DTMF*	When set, the DTMF generator is turned on. When cleared, the DTMF generator is turned off, but other tones can be generated.
Bits 3–0	D3–D0	Specify the desired tone (see the following table):

DTMF	D3	D2	D1	D0	DIGIT DIALED	TONE OUTPUT	FREQUENCIES (HZ)
1	0	0	0	0	0	941	1336
1	0	0	0	1	1	697	1209
1	0	0	1	0	2	697	1336
1	0	0	1	1	3	697	1477
1	0	1	0	0	4	770	1209
1	0	1	0	1	5	770	1336
1	0	1	1	0	6	770	1477
1	0	1	1	1	7	852	1209
1	1	0	0	0	8	852	1336
1	1	0	0	1	9	852	1477
1	1	0	1	0	*	941	1209
1	1	0	1	1	(A)	697	1633
1	1	1	0	0	(B)	770	1633
1	1	1	0	1	(C)	852	1633
1	1	1	1	0	#	941	1477
1	1	1	1	1	(D)	941	1633
0	0	0	0	0	No tone; tone generator turned off		
0	0	0	0	1	550		
0	0	0	1	0	1800		
0	0	0	1	1	2100		
0	0	1	0	0	1300		
0	0	1	0	1	No tone; tone generator turned off		
0	0	1	1	x	No tone; tone generator turned off		
0	1	x	x	x	No tone; tone generator turned off		

Note: TONEON must also be set to generate DTMF signals.

Programmable Gain Controller Register (PGCR): Address (A4–A1) = 1100

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	AGCVT	When set, prevents gain hit due to AGC's gain step. This bit must be set during the handshaking after detecting the four point constellation and before switching to 16-way decision making.
Bits 5–0	G5–G0	Control the gain of the PGC within a range from –10 to +37.5 dB in 0.75 dB steps. (See the following table):

CONTROL REGISTERS (Cont.)

G5	G4	G3	G2	G1	G0	PGC GAIN (dB)
0	0	0	0	0	0	–10.0
0	0	0	0	0	1	–9.25
0	0	0	0	1	0	–8.5
0	0	0	1	0	0	–7.0
0	0	1	0	0	0	–4.0
0	1	0	0	0	0	+2.0
1	0	0	0	0	0	+14.0
1	1	1	1	1	1	+37.25

Note: Signal level is adjusted (before entering the filter) by an internal AGC with +8 dB or 0 dB gain, plus a fixed gain of 5 dB.

DATA Register: Address (A4–A1) = 1101

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	PLLJAM	When this bit is set, the DPLL will be reset by the next rising edge of the received baud clock. This bit must remain high for at least one baud period. It should be cleared by the processor to end the jamming mode. PLLFRZ (see below) overrides PLLJAM when both are enabled.
Bit 5	PLLFRZ	Phase locked loop freeze. When this bit is set, the DPLL begins to run freely regardless of the received baud clock. To re-enable the DPLL locking, the bit must be cleared by the processor. PLLFRZ overrides PLLJAM when both are enabled.
Bit 4	PLLFAST	When set, the DPLL operates in "fast" locking mode. In this mode, the DPLL is updated on every baud period by 13 µs steps. When this bit is cleared (default mode), the DPLL operates in "normal" locking mode and is updated once every 8 baud periods by 6.5 µs steps.
Bit 3–0	RD3–RD0	Four-bit Received Data. Used only in high speed (1200 or 2400 bps) mode, they are descrambled by the processor and shifted out by the SC11024. Sync to Async is also done by the SC11024, when in the asynchronous mode. RD0 is the first bit appearing on the RXD pin, followed by RD1, RD2 and RD3. In the 1200 bps mode, only RD0 and RD1 are shifted out during one baud period.

AUDIO Register: Address (A4–A1) = 1110

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	DISS	When this bit is set, the scrambler is disabled, when cleared, it is enabled. Transmit select bits (TXSEL0–2) override this bit when in "transmit internal mode".
Bit 5	PGCZ	When set, the output of the PGC is grounded. DC offset of the demodulator can be stored and canceled by the controller.
Bit 4–2	TEST	Test bits used for factory testing. For normal chip operation, these bits must be cleared.
Bit 1	ALC1	Audio level control bit 1.
Bit 0	ALC0	Audio level control bit 0. These two bits are used to control the audio level at AUDIO pin according to the following table:

ALC1	ALC0	AUDIO ATTENUATION (dB)
0	0	Audio off
0	1	12
1	0	6
1	1	0 (no attenuation)

Note: The audio signal may be amplified by 12 dB by the line receiver AGC before being fed to the audio attenuator.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1—SC11024 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 3.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11024 in the synchronous mode. This provides a 2400/1200 Hz clock on the SCT pin that can be used as a clock source for the DTE. The Transmit Phase-Locked-Loop (TX PLL) of the SC11024 will be in free-running mode.

Case 2—SC11024 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode, also select "Locked" mode.

The TX PLL of SC11024 will then synchronize itself to the clock provided on its "SCTE" pin.

Case 3—Slave mode. The Transmit Timing is slaved to the receiver recovered clock. Select synchronous mode and connect SCTE to SCR.

In either case, the SC11024 will sample the data on the rising edge of the clock.

Receiver Timing

In synchronous mode, the recovered clock will be provided on the SCR pin and the transitions of RXD will be on the falling edges of this clock. Data is valid on the rising edge of the clock.

SYNCHRONOUS MODE CHART

Transmitter Timing

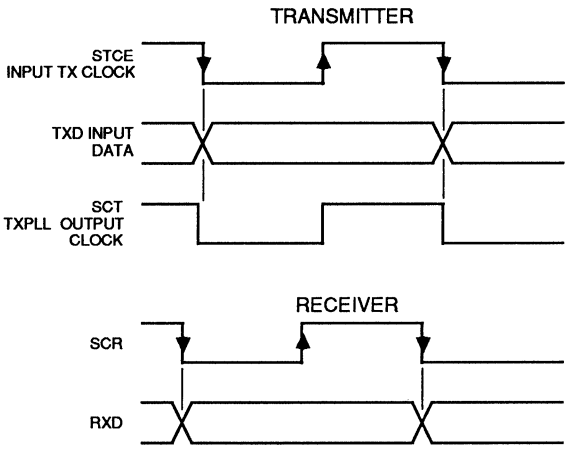


Figure 3. SC11024 Synchronous Mode Timing Diagrams.

SPECIFICATIONS

Absolute Maximum Ratings (Notes 1–3)

Supply Voltage, V_{CC}–GND	7 V
DC Input Voltage (Analog Signals)	AGND–0.6 to V_{CC} +0.6 V
DC Input Voltage (Digital Signals)	DGND–0.6 to V_{CC} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
AGND, DGND	Ground			0		V
F_C	Clock Frequency		9.8295	9.8304	9.8313	MHz
T_R, T_F	Input Rise or Fall Time	All digital inputs except CLKIN			500	ns
T_R, T_F	Input Rise or Fall Time	CLKIN			20	ns

DC Electrical Characteristics (T_A = 0 TO 70°C, V_{CC} = +5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	Normal Power Down Mode		13 1.0	25 4	mA mA
V_{IH}	High Level Input Voltage; Digital pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital pins				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Output (I_{OL} = 1.6 mA)				0.6	V
VXTA	Maximum Peak Output Level on TXA pin	V_{CC} = +5 V	3			V_{PP}

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

SPECIFICATIONS (Cont.)

AC Electrical Characteristics

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
		Processor Bus Interface: (See Figure 4)					
1	TMCAL	Address valid to end of ALE		10			ns
2	TALE	ALE pulse width		40			ns
3	TAVLE	Address valid to ALE low		30			ns
4	THAD	Hold address after ALE low		40			ns
5	TALRD	Delay from ALE low to $\overline{RD}$ low		45			ns
6	TDVRL	Data valid after $\overline{RD}$ low				180	ns
7	TDH	Data hold after $\overline{RD}$ high		0			ns
8	TWR	Write pulse width		148			ns
9	TDVWR	Data setup before $\overline{WR}$ high		40			ns
10	TDHWR	Data hold after $\overline{WR}$ high		0			ns
11	TRHLH	End of $\overline{RD}$ to next ALE		55			ns
12	TWHLH	End of WR to next ALE		120			ns

BUS TIMING

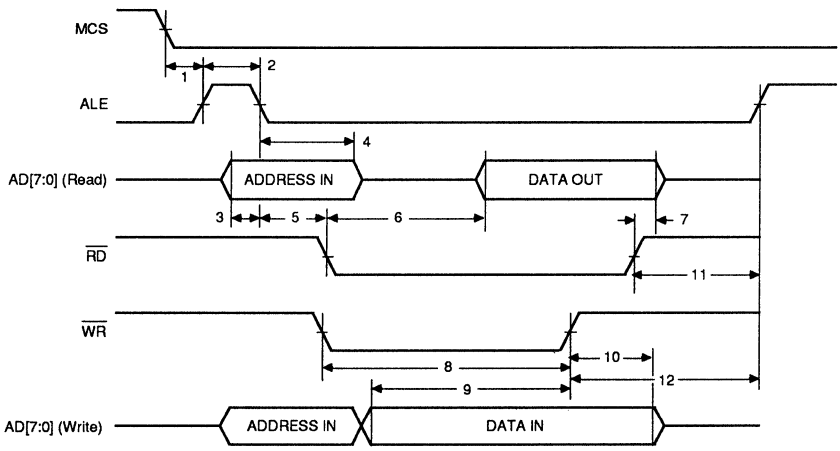


Figure 4. Processor Bus Timing

When the controller is reading or writing to the SC1106, the address must be valid at least 30 ns before ALE goes low and stay valid 40 ns or more.

When the controller is writing, data must be valid at least 40 ns before $\overline{WR}$ goes false and stay valid until at least 0 ns after $\overline{WR}$ goes false.

When reading from the MAP, data is valid a maximum of 185 ns after $\overline{RD}$ goes tru and stays valid at least until 0 ns after $\overline{RD}$ goes false.

SPECIFICATIONS (Cont.)

Modem Transmit Signals—Hz (Assume 9.8304 Crystal)

PARAMETER	CONDITIONS	NOM.	ACT.	UNITS
FSK Mod/Demod Frequencies				
Bell 103				
Answer Mark		2225	2226	Hz
Answer Space		2025	2024.4	Hz
Originate Mark		1270	1269.4	Hz
Originate Space		1070	1070.4	Hz
CCITT V.21				
Answer Mark		1650	1649.4	Hz
Answer Space		1850	1850.6	Hz
Originate Mark		980	978.34	Hz
Originate Space		1180	1181.53	Hz

Call progress monitor mode:		MIN	TYP	MAX	
Center frequency	ALB = 1, G5–G0 = 110111		480		Hz
Detect level (ED high) measured at RXA		–43			dBm
Reject level (ED low) measured at RXA				–48	dBm
Hysterisis		2			dB
Delay time (ED low to high)	EDC = 1.0 µF	10	15	24	ms
Hold time (ED high to low)	EDC = 1.0 µF	10	15	24	ms

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQUENCY	ALLOWABLE ERROR	ACTUAL ERROR
Row 1	697 Hz	±1%	–0.23%
Row 2	770 Hz	±1%	–0.01%
Row 3	852 Hz	±1%	–0.12%
Row 4	941 Hz	±1%	–0.39%
Column 1	1209 Hz	±1%	–0.35%
Column 2	1336 Hz	±1%	–0.93%
Column 3	1477 Hz	±1%	–0.48%
Column 4	1633 Hz	±1%	–0.91%
Guard Tones	550 Hz	±20 Hz	–2 Hz
	1800 Hz	±20 Hz	–2 Hz
Calling Tone	1300 Hz		–6 Hz
Answer Tone	2100 Hz		+1 Hz

SC11024 SPECIFICATIONS (Cont.)

DTMF Generator (Cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion	VCC = +5 V TL2 = TL1 = TL0 = 0 Measured at TXA Pin		–40		dB
Row Output Level			–2		dBm
Column Ouput Level			0		dBm
550 Hz Guard Tone			–6		dB (Note 2)
1800 Hz Guard Tone			–9		dB (Note 2)
1300 Hz Calling Tone			–3		dB
2100 Hz Answer Tone			–3		dB
Transmit level measured at TXA	Load = 1200 Ohms TL2 = TL1 = TL0 = 0 Squelched		–3	 –50	dBm dBm

Notes: 1: This assumes a clock of exactly 9.8304 MHz.

2: These levels are referenced to the TX signal level. When guard tones are added, the TXA level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Mode	EDC = 1.0 µF; measured at RXA PGC = 0				
Energy detect level (ED low to high)				–43	dBm
Loss of energy detect level (ED low to high)		–48			dBm
Hysterisis		2	3		dB

Programmable Gain Controller (PGC)

Gain step size			0.75		dB
Dynamic range			47.25		dB
Response time (from change in PGC register to output of A to D converter)			1.0		ms

Filter Characteristics

Crosstalk rejection			70		dB
Power supply rejection			0		dB
DPLL Response times JAM or FRZ Fast			20 200		µs µs

APPLICATIONS INFORMATION

Applications

The SC11024 with an external control microprocessor, a telephone line interface and a suitable computer interface, can implement a complete 2400 bps modem for many applications with a minimum of components and cost. Figure 7 shows the common portion of such a modem using the SC11024 with a telephone line interface. Sierra's SC22201, 128 byte E^2 memory is used to store default parameters and often used phone numbers. The SC11019/20/21/22/23 controllers also support a serial E^2 memory as an alternative. Figures 6 and 7 show the stand-alone and PC bus integral modems implemented with Sierra's SC11019/20 controllers. Figure 8 shows the connections for an internal ROM special purpose controller using the SC11022. Figure 9 shows an RS-232C serial interface for implementing a stand-alone modem. Figure 10 shows a parallel bus interface for implementing an internal modem for an IBM PC/XT/AT compatible computer when used with Sierra's SC11019 controller shown in Figure 6, while Figure 13 shows the interface required for implementing the same internal modem when used with the controller shown in Figure 12. Figure 11 shows a power supply schematic for a stand-alone modem application.

Various modem configurations can be realized by combining schematics shown in Figures 5 thru 13.

A Hayes compatible stand-alone smart modem (Fig. 5) can be implemented by combining Figures 7, 8, 9 and 11.

The internal version for an IBM PC/XT/AT compatible (Fig. 6) can be implemented using Figures 7, 8 and 10.

An alternative to the controller of Figure 8 is shown in Figures 12 and 13.

For performance evaluation, a circuit shown in Figure 14 can be used to obtain a constellation of the modem. Quality of the signal processing performed by the modem can thus be visualized by observing the constellation for various line conditions and signal to noise ratios.

Power Supply Decoupling and Circuit Layout Consideration

For optimum performance at low received signal levels with low S/N ratios, it is important to use the recommended power supply decoupling circuit as shown in Figure 7.

Small inductors in series with the supplies help suppress RFI as well as improve the power supply noise rejection capability of the SC11024. A 10 Ω, 1/4W resistor in place of, or in series with, the inductor in the SC11024 power lead has been found to be helpful in computer based products or where the power supply is particularly noisy.

The 10 µF capacitors should be a tantalum type while the 0.1 µF capacitors should have good high frequency rejection characteristics—monolithic ceramic types are recommended. It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11024 as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply.

A Ferrite bead on the 5V input to the circuit board should also be considered, both from a modem performance standpoint, as well as an aid in reducing RF radiation from the phone line.

Note: Crystal oscillator: The controller requires a parallel resonant 19.6608 MHz crystal designed with CL = 18 pF and tolerance of ± .01% (such as Saronix NYP196-18). With this crystal, use 27 pF to ground from both XTAL1 and XTAL2. Clock frequency measured at CKOUT (Pin 7) must be within ±0.01% of 9.3804 MHz.

APPLICATIONS INFORMATION (Cont.)

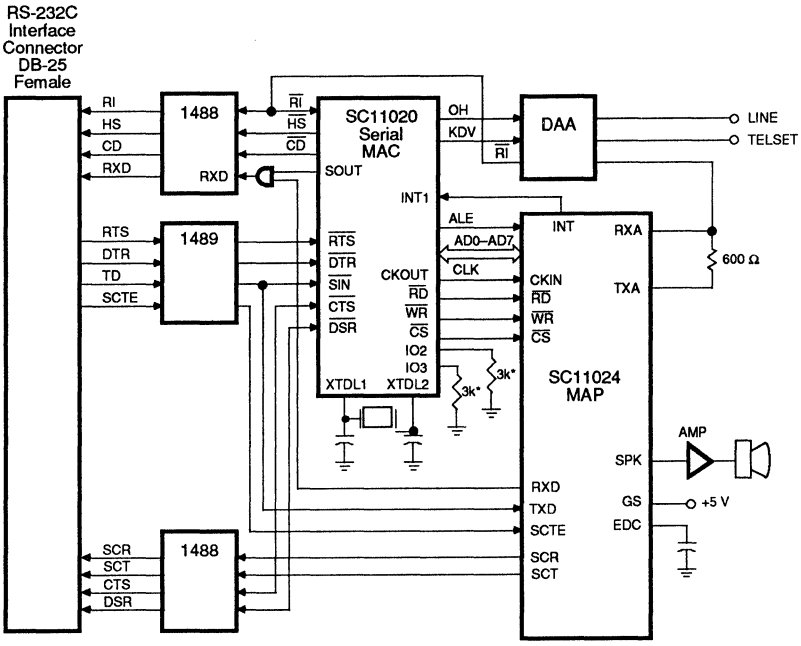


Figure 5. V22 bis Standalone Intelligent Modem with Internal ROM.

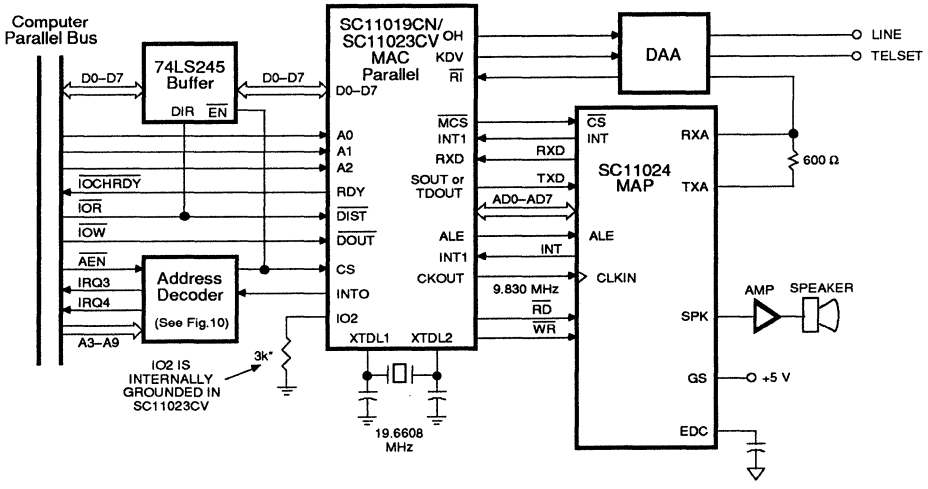
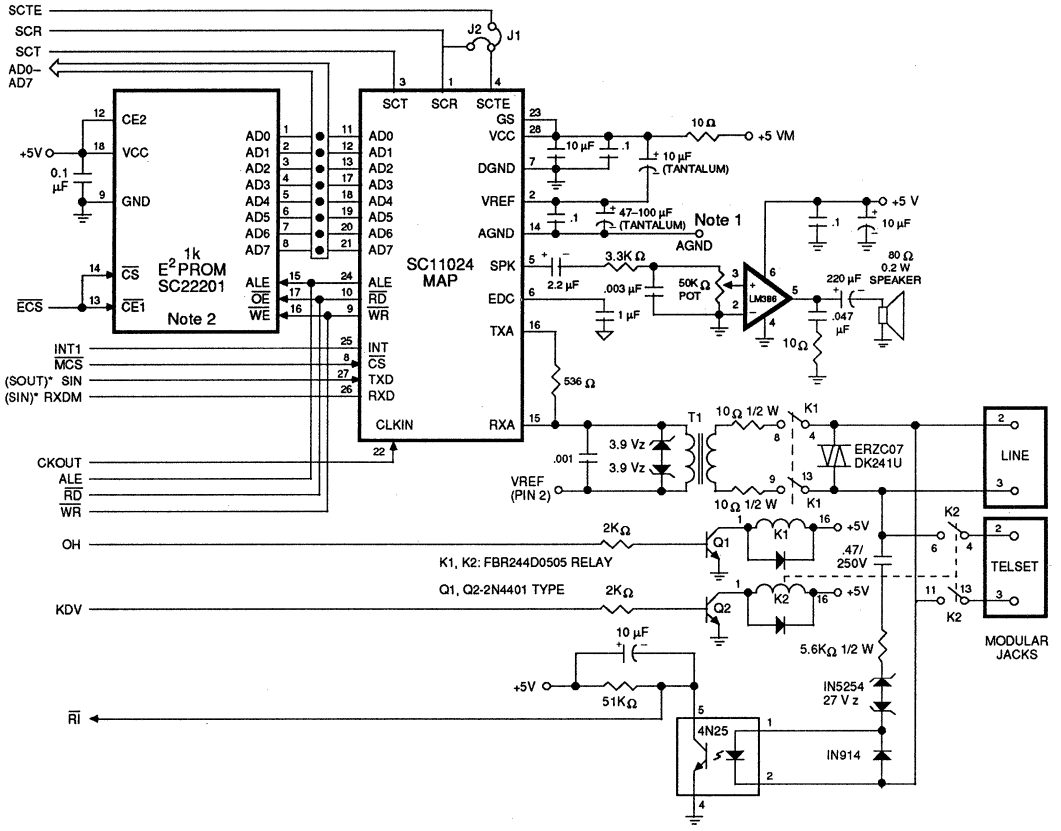


Figure 6. Internal Smart Modem for PC Bus Applications with Internal ROM.

* 3 kΩ only required if IO port is shared with serial E^2PROM otherwise the pin may be grounded.

APPLICATIONS INFORMATION (Cont.)



Note 1: Connect analog ground directly to common of the power supply filter capacitor.

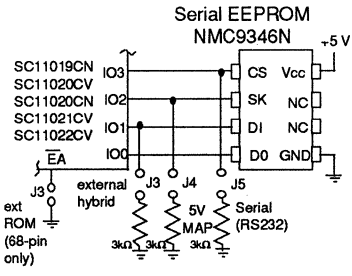
Note 2: A serial E^2 PROM may be substituted when using the SC11019, SC11020, SC11021 or SC11022 Modem Advanced Controller (48 and 68 pin versions), or SC11023 44 pin version.

Note 3: For external clocking of the transmitter, install J1 and set bit 6 of the MCRA; omit J2.
For slave clocking of the transmitter, install J2 and set bit 6 of the MCRA; omit J1.
For normal operation, omit J1 and J2, and clear bit 6 of the MCRA.

*When used in the configuration as a parallel modem (Figure 6), connect Pin 27 of SC11024 to SOUT pin of controller and connect Pin 26 of SC11024 to SIN pin of controller.

Figure 7. Common Portion of 2400 BPS Modem.

CONFIGURATIONS FOR SC11019CN, 20CN, 20CV, 22CV BIG MACS



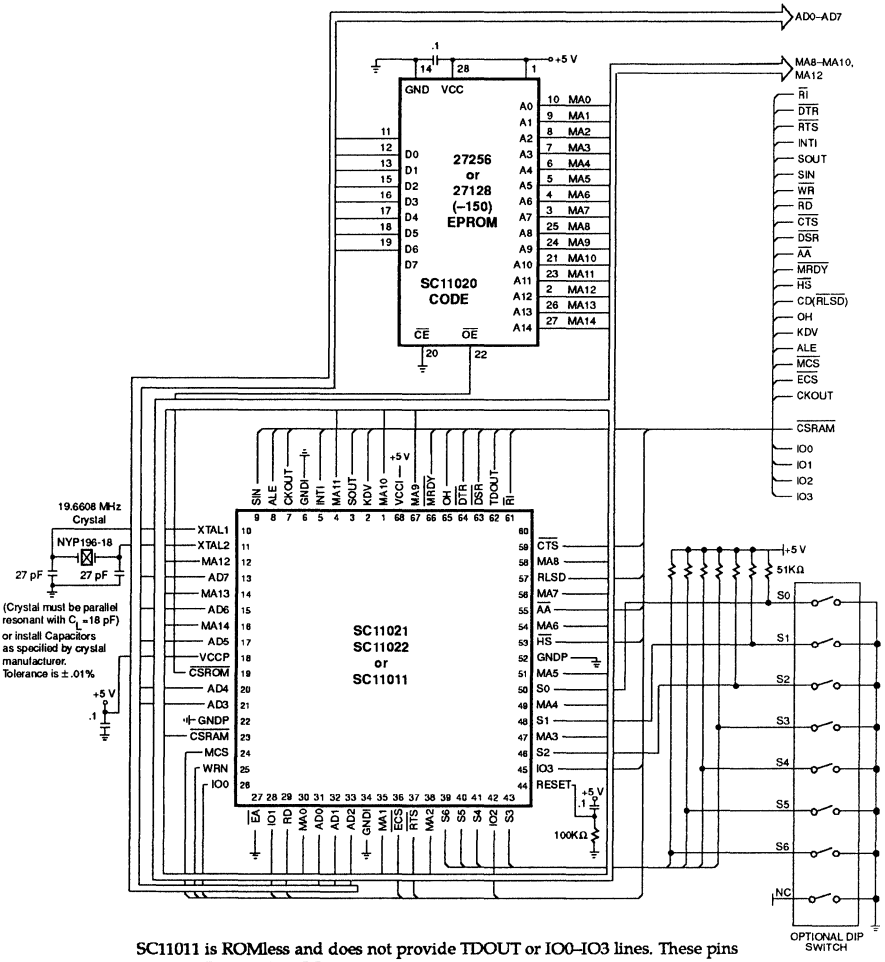
All models listed above can operate with either serial or multiplexed EEPROMs for configuration and number storage. The internal ROM program automatically determines which kind of EEPROM is connected and adapts accordingly.

Note that the SC11022 pin configuration matches that of the SC11011 controller except five new pins are used that were formerly not connected. Four of these are the I/O pins described above. One is the TDOUT pin which is used with SC11026 for V.23 signalling. For upward compatibility the TDOUT pin may be permanently wired to TXD.

When substituting SC11022 for SC11011 it is only necessary to open the EA pin and remove the external EPROM. Connect the jumpers as shown if required to operate with SC11024 MAP, external hybrid or in serial mode.

Three of the four I/O pins on the specified models of the internal ROMed MAC are programmed to set the configuration at power-up or reset.

APPLICATIONS INFORMATION (Cont.)



SC11011 is ROMless and does not provide TDOUT or IO0–IO3 lines. These pins are "No Connect" on SC11011.
SC11021 is ROMless and can address 32k external ROM.
SC11022 has 16k internal ROM and can address 24k external ROM.
Consult controller data sheet for programming information.

Figure 8. Special Purpose Control Processor for Stand-Alone or Parallel Applications.

Internal weak pull-up resistors will set the default configuration to internal hybrid, ±5 V SC11006 MAP interface and Parallel mode if there is no external pull-down.

External pull-down resistors must be added to select other options as indicated in the table. The I/O drivers will overcome these pull-up or pull-down resistors in normal operation to operate the serial EEPROM. The I/O pins may be directly grounded if the serial EEPROM is not used.

In the 44-pin version of SC11019, the I/O pins are not externally available. The SC11023 is internally bonded to select the 5 V only MAP (SC11024) configuration.

MAC PART NO.	PACKAGE	INT. ROM	EXT. ROM	UART MODE	MAP
SC11019CV	44-PLCC	16 k	–	Parallel	SC11006
SC11019CN	48-DIP	16 k	–	Parallel	SC11006/24
SC11020CV	44-PLCC	16 k	–	Serial	SC11006/24
SC11020CN	48-DIP	16 k	–	Serial	SC11006/24
SC11021CV	68-PLCC	0	24 k	Serial/Par.	SC11006/24
SC11022CV	68-PLCC	16 k	24 k	Serial/Par.	SC11006/24
SC11022CN	48-DIP	16 k	–	Serial/Par.	SC11006/24
SC11023CV	44-PLCC	16 k	–	Parallel	SC11024

APPLICATIONS INFORMATION (Cont.)

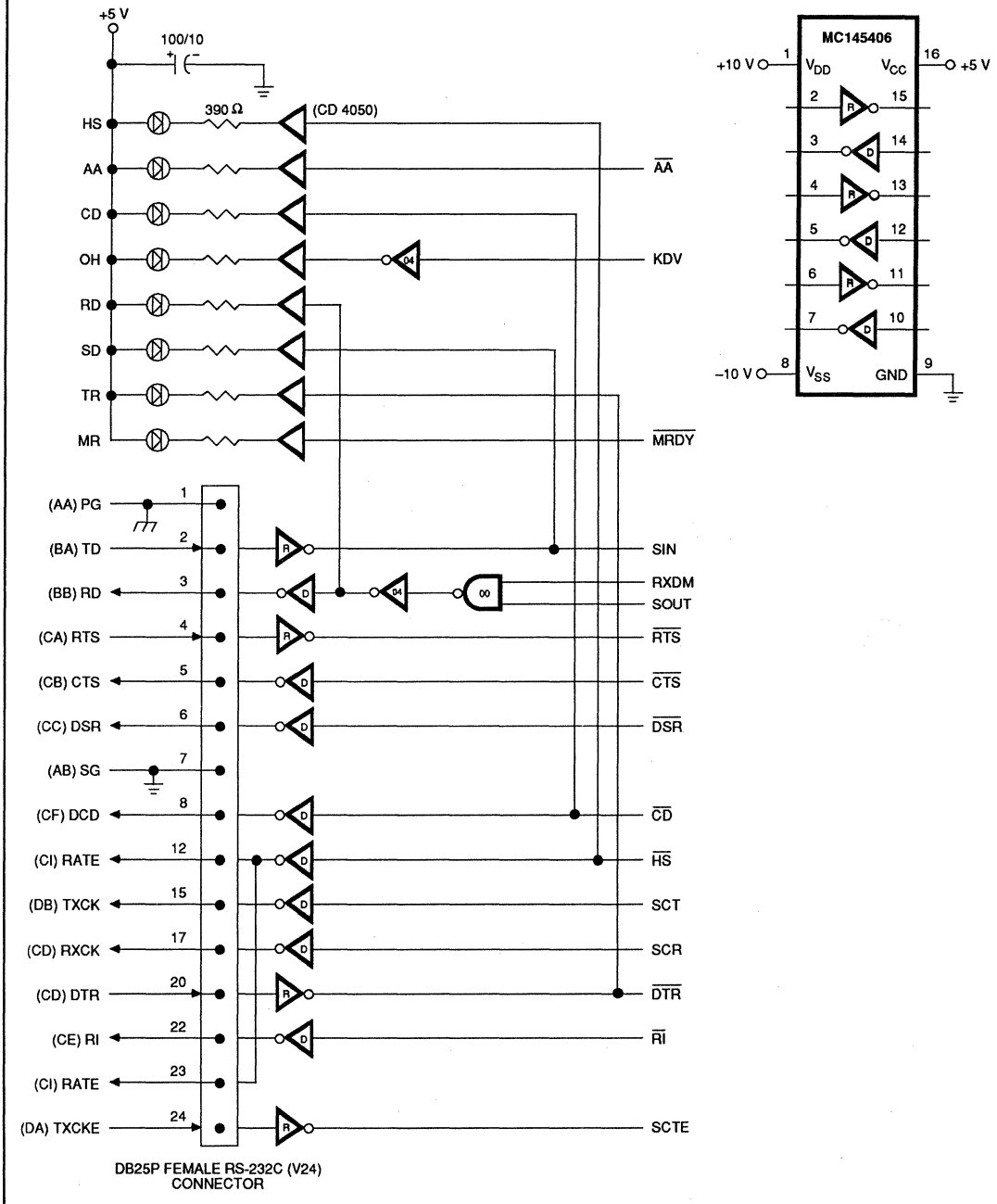


Figure 9. RS-232C Interface for Stand-Alone Modem Application.

APPLICATIONS INFORMATION (Cont.)

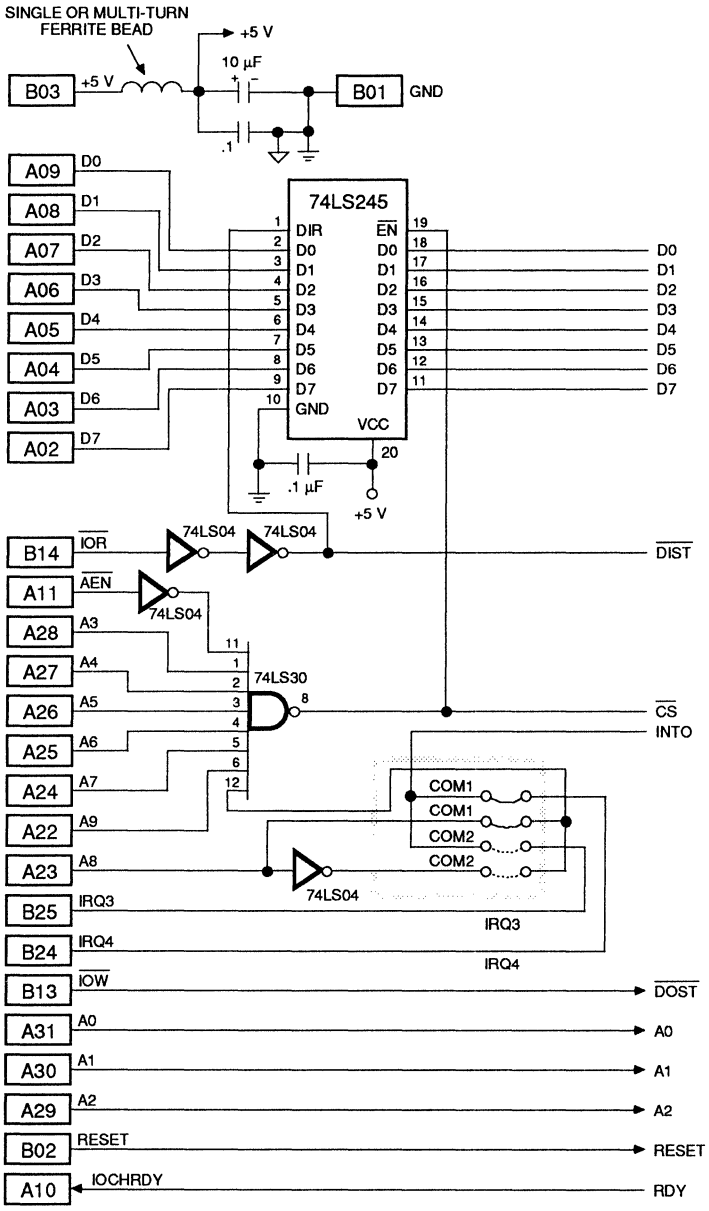


Figure 10. IBM PC/XT/AT Compatible Computer Bus Interface for SC11019 Controller of Figure 7.

APPLICATIONS INFORMATION (Cont.)

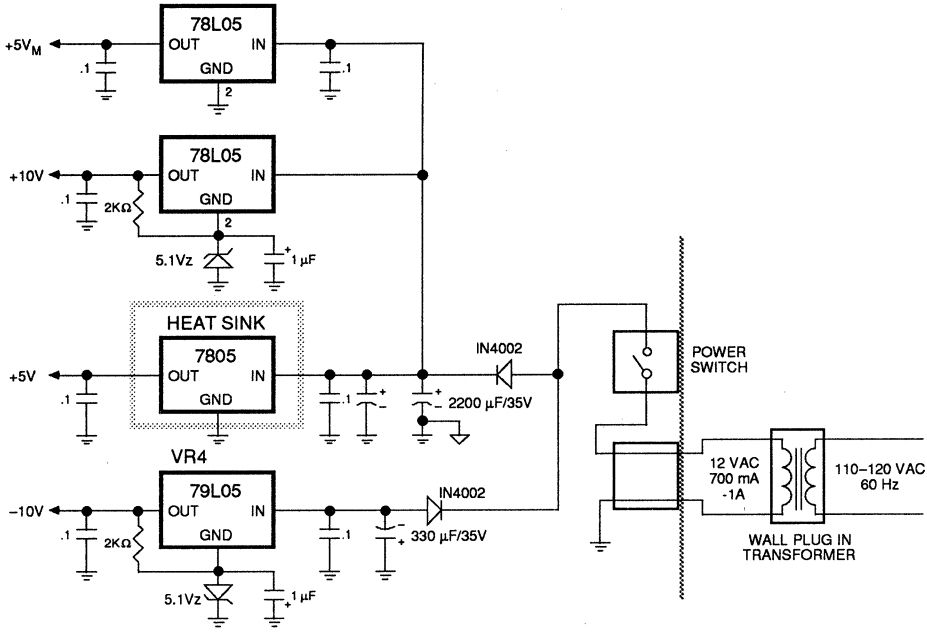


Figure 11. A Typical Power Supply for Stand-Alone Modem Application.

APPLICATIONS INFORMATION (Cont.)

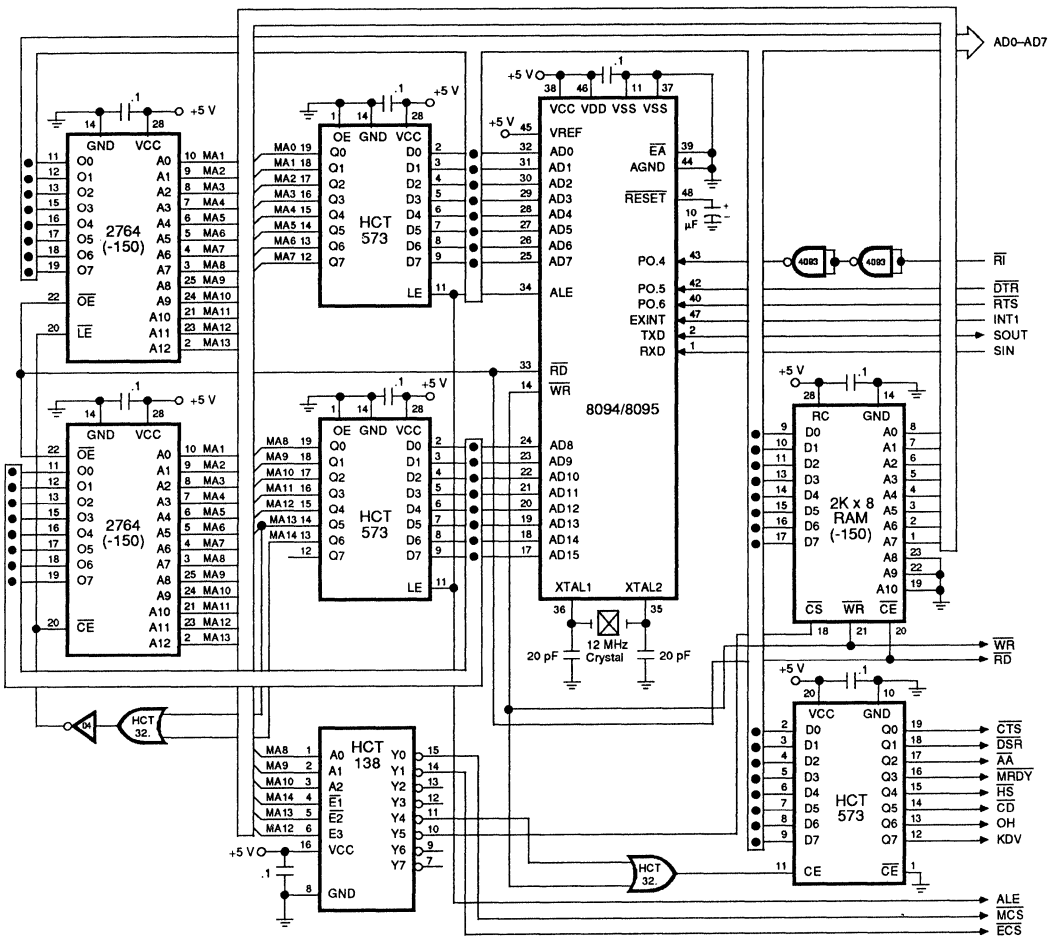


Figure 12. Control Processor Using 8095

APPLICATIONS INFORMATION (Cont.)

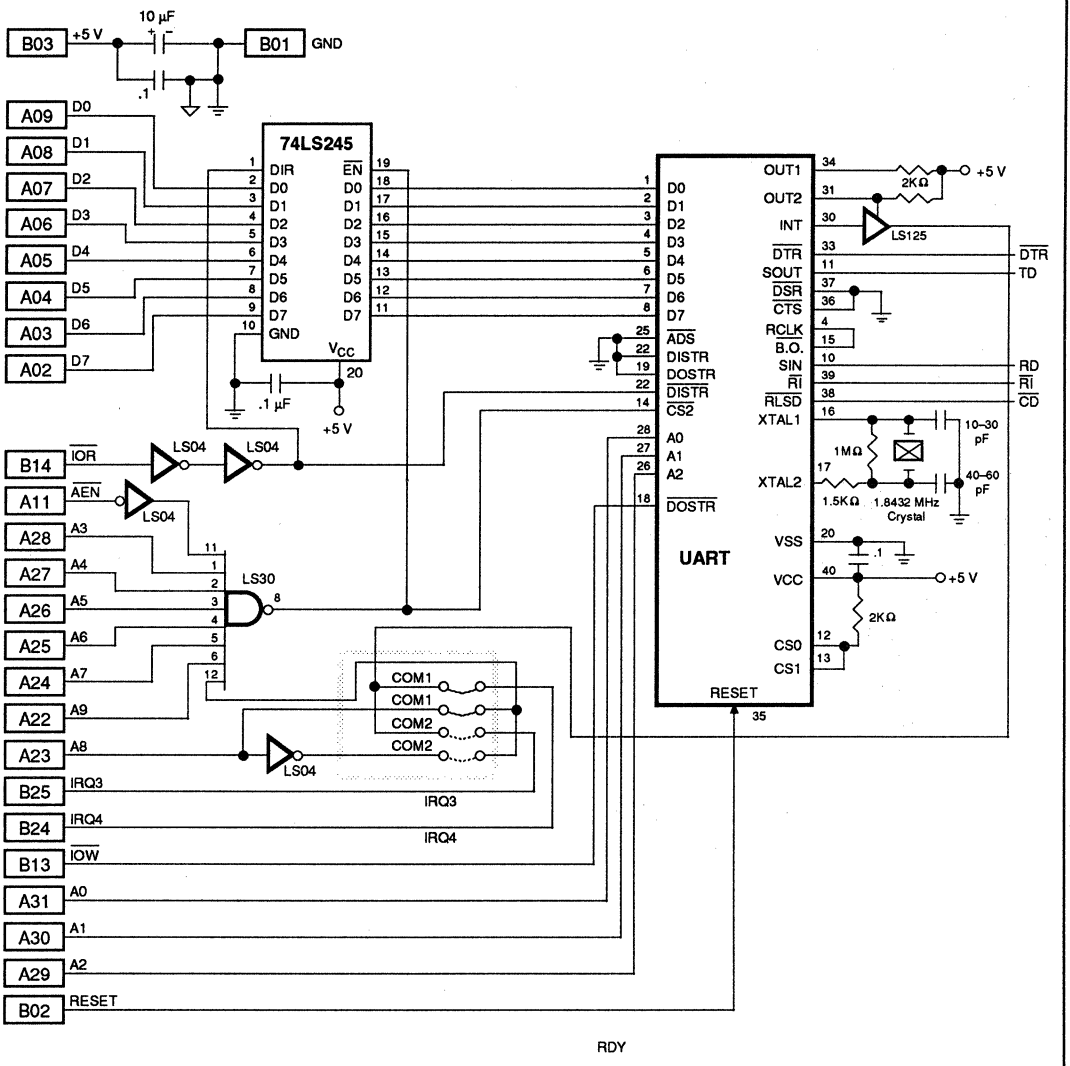
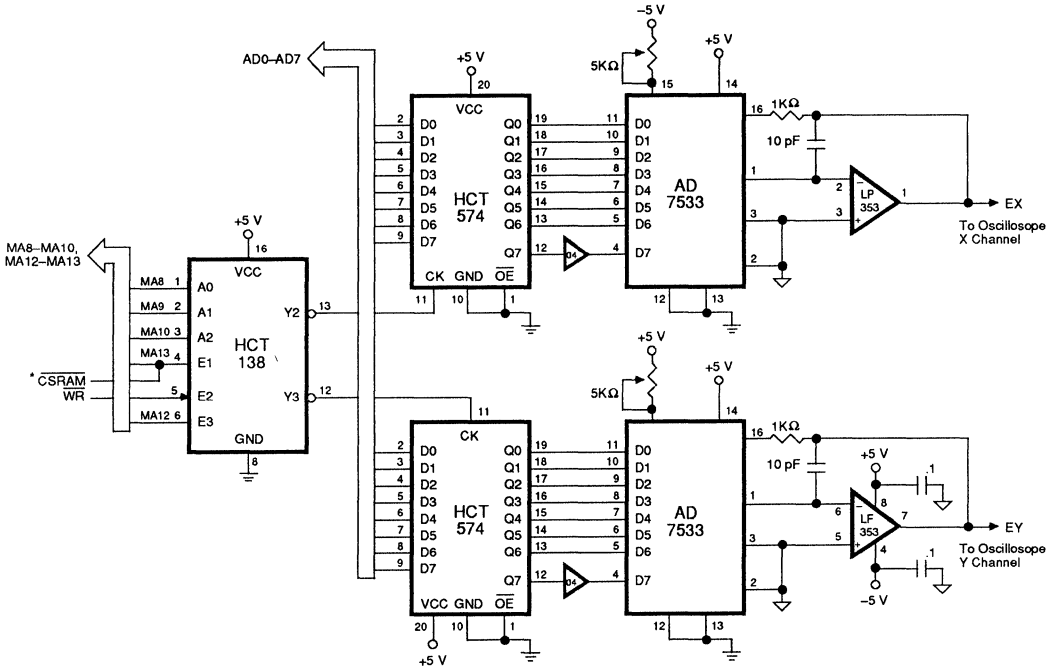


Figure 13. IBM PC/XT/AT Compatible Computer Bus Interface for 8095 Controller of Figure 12.

APPLICATIONS INFORMATION (Cont.)



IF THE SC11019 FAMILY IS USED, CONNECT $\overline{\text{CSRAM}}$, IF THE INTEL 8096 FAMILY IS USED, CONNECT MA13.

Figure 14a. Test Circuit to Generate Constellation Display.

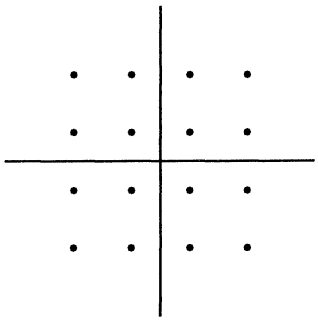


Figure 14b. Constellation for 2400 BPS Modem.

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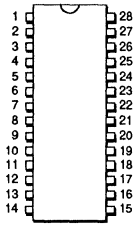
FEATURES

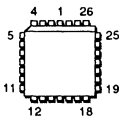
- ☐ Complete 2400 bps modem conforming to V.22 bis
- ☐ Compatible with CCITT V.22 bis, V.23, V.22, V.21 and Bell 212A and 103 standards
- ☐ Analog, digital, and remote digital loopback
- ☐ Pin compatible with SC11006
- ☐ Integrated DTMF/Guard Tone Generators, call progress monitor
- ☐ Contains an on-chip hybrid
- ☐ Programmable audio output
- ☐ CMOS technology
- ☐ DIP or PLCC packages

28-PIN DIP PACKAGE



SC11026CN

28-PIN PLCC PACKAGE



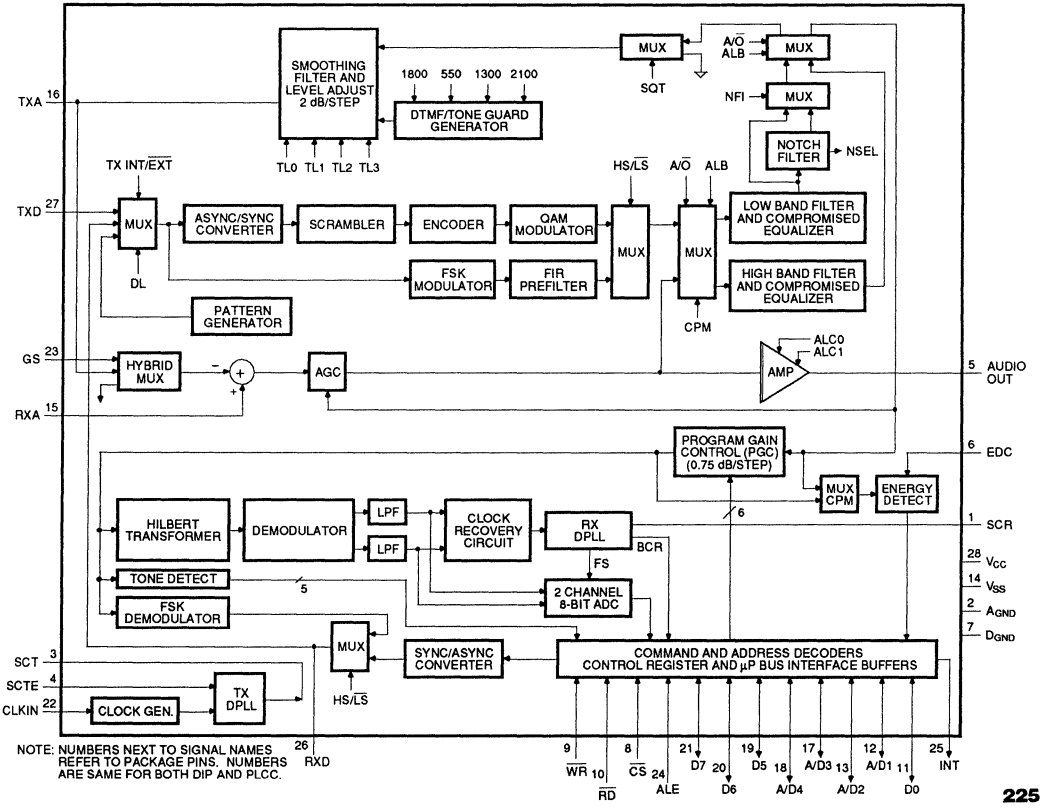
SC11026CV

GENERAL DESCRIPTION

The SC11026 is a complete 2400 bps modem IC containing all modem functions except the adaptive equalizer. It is used in conjunction with an external controller such as the Sierra SC11021 series ROMless controllers for customized firmware, to implement a 2400 bps full duplex modem, compatible with the CCITT V.22 bis recommendation. The controller performs all modem control and handshaking functions as well as the adaptive equalization. The SC11026 is pin compatible with the SC11006 MAP.

The SC11026 operates in 2400 bps QPSK/QAM and 1200 bps PSK as well as 0 to 300 baud FSK modes compatible with Bell 103 and 212A, as well as CCITT V.21, V.22, V.23 and V.22 bis standards. The SC11026 also operates in V.23 answer and originate modes with a buffered DTE interface that allows the DTE to operate at 1200 bps in both directions while the modem operates at 1200/75 bps. When used with the SC11021 controllers, the SC11026 becomes an intelligent modem controlled by the industry standard "AT" command set.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE SAME FOR BOTH DIP AND PLCC.

FUNCTIONAL DESCRIPTION OF THE SC11024 MODEM

The SC11026 includes:

- ☐ Full transmitter consisting of
  - – Async to Sync converter
  - – Scrambler
  - – Data encoder
  - – 75% square root of raised cosine pulse shaper
  - – Quadrature modulator
  - – FSK (Bell 103 and CCITT V.21) modulator
  - – Hybrid
- ☐ High band and low band filters
- ☐ High band and low band compromise equalizers
- ☐ V.22 notch filter (selectable at 550 or 1800 Hz)
- ☐ Transmit smoothing filter
- ☐ Programmable attenuator for transmit level adjust
- ☐ DTMF, 550 Hz, 1300 Hz, 1800 Hz, and 2100 Hz tone generator
- ☐ Transmit clock circuit for synchronous operation (slave, external, and internal modes)
- ☐ Pattern generator for generating fixed digital patterns in handshaking mode
- ☐ Receive section consisting of
  - – 64-step programmable gain controller (PGC)
  - – Energy detector at the output of the PGC
  - – Hilbert transformer
  - – Quadrature demodulator (free running carrier) with low pass filters
  - – Baud timing recovery circuit (sampling clock of 600 Hz)
  - – FSK demodulator
  - – Tone detector
  - – Sync to Async converter
- ☐ 8-bit analog to digital converter (ADC)
- ☐ Control and Status registers
- ☐ 8-bit microprocessor interface with interrupt and multiplexed address/data lines
- ☐ Audio output with level adjust

Transmitter

Since data terminals and computers may not have the timing accuracy required for 2400/1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 2400/1200 Hz +2.3%, –2.5%. It outputs serial data at a fixed rate of 2400/1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 2400/1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first four/two stages of the shift register form the quad/dibit that is applied to the QAM/QPSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band, centered at 2400 Hz, or the low band, centered at 1200 Hz. In the 2400 bps mode, the modem actually sends four bits at a time, called a quadbit. The actual rate of transmission for a quadbit is 600 baud. This is the optimum rate of transmission over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

In the 2400 bps data rate, the data to be transmitted is divided into groups of four consecutive bits (quadbits). The first two bits of the quadbit are encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. The last two bits define one of the four signaling elements associated with the new quadrant.

In the 1200 bps data rate, the data stream is divided into groups of two consecutive bits (dibits). The dibits are used to determine the phase quadrant change relative to the quadrant occupied by the preceding signal element. The resulting signaling elements from the inphase (I) and quadrature (Q) channels are passed through baseband filters with a square root of raised cosine shape. The filtered signals subsequently modulate sine and cosine carriers, and add to form the QAM/QPSK signal. The wave-shaped signal is then passed through either the low-band or high-band filter, depending upon originate or answer mode selection.

For low speed operation, the FSK modulator is used. It produces one of four precision frequencies, depending upon originate or answer mode selection and the 1 (mark) or 0 (space) level of the transmit data. Different frequencies are used for V.21, V.23 and Bell 103 modes. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands, smoothing filters for both bands, and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.22 bis applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress

monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode, it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second-order low-pass switched-capacitor filter that adds the modem transmit signal to the V.22 guard tones. It also provides a 1 dB per step programmable gain function to set the output level.

Receiver

The receiver section consists of an energy detector, programmable gain control (PGC), part of the QAM/QPSK demodulator, FSK demodulator, 8-bit ADC and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to the energy detector and PGC circuit. The energy detector provides detection within 17 to 24 msec. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels. In call progress mode, the energy detector is connected to the output of the PGC to allow detection level adjustment.

The output of the receive filter is applied to the programmable gain control (PGC). This circuit has a wide overall range of 47.25 dB and provides 64 steps of 0.75 dB/step. The PGC gain is controlled by the external processor. It also provides auto-zeroing to minimize the output DC offset voltage.

The QAM/QPSK demodulator uses a coherent demodulation technique. Output of the programmable gain control (PGC) is applied to a Hilbert transformer that produces an in-phase and 90° out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by a free-running carrier. The baseband components are low-pass filtered to produce I and Q (Inphase and Quadrature) channel outputs. The I and Q channel outputs are both filtered by 300 Hz band-pass filters. Then they are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled and digitized into 8-bit samples by the ADC. Each channel (I and Q) is sampled twice during a baud period, once at the middle and once at the end of the baud period, allowing T/2 or T sampling operation. The external processor is interrupted once every baud period (1.667 msec). The processor should read the I and Q samples (within 100 µs from the time interrupt is issued), and perform adaptive equalization, carrier phase tracking, data decoding, and data descrambling. One quad/dibit is transferred from the SC11026 during each baud period.

In the asynchronous mode, data received from the processor is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are re-inserted. Underspeed data is passed essentially unchanged. The sync/async converter has two modes of operation. In the basic signaling mode, the buffer can accept an overspeed which corresponds to one missing stop bit in eight characters. The length of the start and data elements will be the same, and the stop bit will be reduced by 12.5%. In the extended-signaling range, the buffer can accept one missing stop bit in four characters and the stop bits will be reduced by 25% to allow for overspeed in the transmitting terminal. Output of the sync/async converter, along with the output of the FSK demodulator, is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed and output data received on the RXD pin.

For low-speed operation, the FSK demodulator is used. The output of

the PGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

A tone detector is included to help the handshaking sequence by detecting the following frequencies: 2225 Hz Bell 103 Mark (Answer), 1650 Hz V.21 Mark (Answer) , 1300 Hz V.23 Forward Channel Mark, 390 Hz V.23 Reverse Channel Mark and 2100 Hz Answer Tone.

To improve the performance of the receiver at low signal levels, while maintaining a wide amplitude range, a 1-bit AGC circuit is placed prior to the band-pass filter. The decision thresholds of this AGC are controlled by the AGCVT bit. When AGCVT = 1, the thresholds will be 6 dB further apart than when AGCVT = 0, so that the probability of gain change will be reduced. The status of the AGC gain is available through the AGCO bit. AGC will have 8 dB more gain when AGCO = 1. Status of AGCO should be monitored at every baud timing and when it makes a transition (causing a gain-hit) the PGC's gain should be modified accordingly to prevent divergence of the adaptive equalizer.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, by turning the "Hybrid" code on through the interface, this matching is provided by an external resistor connected between the TXA and RXA pins on the SC11026. The filter section provides sufficient attenuation of the out-of-band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter. The hybrid can be deactivated by the controller.

The SC11026 internal hybrid is intended to simplify the phone line interface. The internal hybrid can compensate for the loss in the line coupling transformer used in the DAA. By tying the GS pin to AGND, V_{REF} or V_{CC} compensation levels of 0, +2, +3 dB, respectively, are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. An external hybrid circuit, shown in Figure 2, can be used to overcome these losses and achieve maximum performance. In this case, the internal hybrid must be turned off by setting bit 6 of the TXCR register to 0.

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC11026 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired value. In practice, however, there is impedance mismatch and a loss in the coupling transformer. Therefore, it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain (G_R) and transmit gain (G_T) are set by the ratios of resistors R2, R1 and R6, R5 respectively (Figure 2).

The circuit can be analyzed as follows:

$$V_R = -\frac{R2}{R1}\left(V_{TR}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)V_y$$

$$V_y = -\frac{R6}{R5}V_x$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_y = 2V_{TX}$,

$$V_R = -\frac{R2}{R1}\left(V_{TX}+V_{RX}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)2V_{TX}$$

$$= -\frac{R2}{R1}V_{RX} + \left[\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) = \frac{R2}{R1}$$

Solving for R3/R4:

$$\frac{R3}{R4} = 1 + \frac{2R1}{R2}$$

Additionally,

$$G_R = \frac{R2}{R1} \text{ and } G_T = \frac{R6}{R5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive loss in the coupling transformer is 2.5 dB, then:

$$\frac{R2}{R1} = \text{INV Log}\left(\frac{G_{RdB}}{20}\right) = \text{INV Log}\left(\frac{2.5}{20}\right) = 1.333$$

Similarly, $\frac{R6}{R5} = 1.333$ and $\frac{R3}{R4} = 2.5$

Some typical values are:

R1=20KΩ, R2=27KΩ, R3=13KΩ, R4= 5.1KΩ, R5=20KΩ, and R6=27KΩ

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6, and capacitor C1 can be eliminated, and point X can be connected to point Y in the circuit of Figure 2 to achieve a more cost effective external hybrid arrangement.

The SC11026 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, the "Hybrid" code must be turned off. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

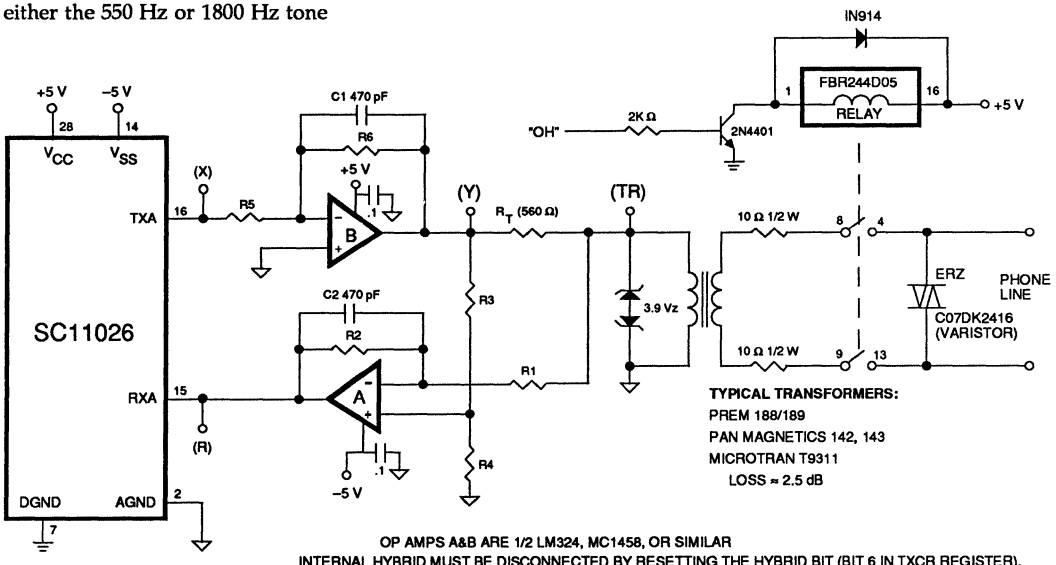
The tone generator section consists of a DTMF generator, V.22 guard-tone, and 1300 and 2100 Hz tone generators. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and A, B, C, D, *, and # keys. The V.22 guard-tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the tone control register. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to 1300 and 2100 Hz and the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50 kΩ is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation—no attenuation, 6 dB attenuation, 12 dB attenuation, and squelch are provided through the ALC1 and ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Clock Input

CLKIN (Pin 22) of the SC11026 should be connected to a 9.8304 MHz clock source with an accuracy of ±0.01%.



OP AMPS A&B ARE 1/2 LM324, MC1458, OR SIMILAR
INTERNAL HYBRID MUST BE DISCONNECTED BY RESETTING THE HYBRID BIT (BIT 6 IN TXCR REGISTER).
WITH INTERNAL ROM SC11039 CONTROLLER, THIS IS ACHIEVED BY A PULL-DOWN 3 kΩ on IO1.

Figure 2. Using an External Hybrid with the SC11026

FUNCTIONAL DESCRIPTION OF THE SC11021 CONTROLLER

The SC11021 modem controller, implemented in Sierra's CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus. Besides including a 16-bit microprocessor and 128 by 8 bytes of RAM, it also contains the functionality of an 16C450 UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem for the PC consists of the SC11021 controller, the SC11026 modem and the DAA. All of the popular communications software written for the PC will work with the SC11026/SC11021 set.

The SC11021 may also be configured for RS-232 applications by means of a configuration bit in the controller firmware. The difference is that the UART is turned around so that the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The controller receives an 8-bit signal sample from the SC11026 and performs adaptive equalization, carrier phase recovery, data decode, and descrambling. The controller is designed by using a 16-bit 2900 processor to perform the digital signal processing and the control functions. Its instruction set is a subset of the Intel 8096 instruction set, but operates faster than the 8096.

The SC11021 provides a standard 5V logic level interface—RS-232 drivers are required to interface to the port. Firmware is available from Sierra in modular source code form for easy user modification.

When used with the SC11021 and SC11026, the firmware emulates a Hayes-type stand-alone or IBM PC plug-in card modem with the addition of V.23 capability.

A 16K internal ROM version of the SC11021 is available for custom code masks. For example, only about 15 kbytes of the ROM is used for the handshaking and smart modem code, leaving 1 kbytes for additional features that a customer may specify. And since the controller is ROM programmable, any command set, not just the Hayes "AT" set, can be implemented.

The custom ROM model can be supplied in three pinout options. They are 68 pin PLCC, 48 pin DIP, and 44 pin PLCC.

The SC11021 is available in a 68 pin PLCC and operates with up to 32k external ROM.

In V.23 mode, the firmware uses internal ROM to buffer the 75 bps channel to 1200 bps so that two-way 1200 bps communication to the terminal can be employed, thus allowing the use of standard communication programs. Flow control is required to prevent overflow of the RAM.

Please refer to the SC11021 series data sheet for complete details on controller features and performance characteristics.

The controllers require +5 V power supply. Besides the interface for the SC11026 modem, the SC11021 controller has an eight-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 16C450 UART. It also has control lines for ring indication, the off-hook relay, and a data/voice relay; these lines connect to the DAA.

In the RS-232 mode, the eight-bit port becomes the switch input lines, and the address, chip select, INTO, DIST and DOST lines become the lines for the RS-232 interface, and modem status. These lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control.

The interface to the SC11026 is via an 8-bit address/data bus and the control lines for read and write. The same interface can be used for access to an electrically erasable random access memory (SC22201) or to access another modem IC such as a fax modem. There are six clock multiplexed address/data bus cycles. A ready signal is provided for the interface to a high speed PC-AT type bus cycle. For the 68 pin packages, there are 15 extra address lines and chip selects for external ROM and external RAM interfaces. An $\overline{EA}$ pin is also available for selection of internal ROM or external ROM.

The SC11021 series are truly ASIC controllers—they are designed to control a modem or other peripheral that operates at a moderately slow data rate up to 2400 bits per second. What's unique about the SC11021, for example, is that it allows a slow peripheral to interface to a high speed bus without making the main processor add unnecessary wait states

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11021 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up, it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like a Hayes-type modem. The escape sequence is three + signs—+++ —in the default mode, but it can be changed in the software.

The actual processor contains a 16-bit data path and can execute 54 instructions with three different addressing modes: direct, indirect, and immediate. There is 16k by 8 of ROM on the chip for program storage.

To the system bus, the SC11021 looks and acts like a 16C450 UART. Communications software written for this UART will work with the SC11021. The Sierra chip set is truly a Hayes-type modem in two chips.

THE SC11026/SC11021 SYSTEM

The only external components required by the SC11026 are a 600 Ω line matching resistor and a 1.0 μF capacitor from the EDC pin to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11026 can directly drive a high impedance (50 kΩ) earphone-type transducer.

If the modem is required to operate in V.23 answer and originate modes, a simple multiplexer switch is needed to divert the 75 bps signal through the special I/O port on the SC11021 controller. This MUX is not needed if the modem is to be used for V.23 originate only.

The SC11026 modem's CLKIN pin line is driven by the SC11021 CKOUT line at 9.8304 MHz. The SC11021 may be interfaced directly to an IBM PC bus, but use of a 74LS245 buffer is suggested. The only external parts may be an 8 input NAND gate for COM1 and COM2 decoding inside the PC. A ready signal is provided to control the IOCHRDY pin on the bus to allow operation with higher speed computers (AT, XT TURBO, etc.)

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

V.22 and V.22 bis also call for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The SC11026 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone in the receiver.

All modems require a Hybrid; a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the SC11026, this is done with op amps. The hybrid can be disabled so an external hybrid can be used, if desired.

V.23 CONFIGURATIONS

When converting from the SC11006 modem to the SC11026, the only changes to the board are shown here. If both originate and answer modes are needed, the multiplex switch must be inserted. But if originate is the only V.23 mode required, then the only change is to connect the Modem TXD input to the TDOUT pin on the controller instead of SIN or SOUT. The internal multiplexer selects the correct signal source for all operating modes. Note that this connection also works for the SC11006 so the circuit board can be layed out to accept either modem.

CONFIGURATIONS

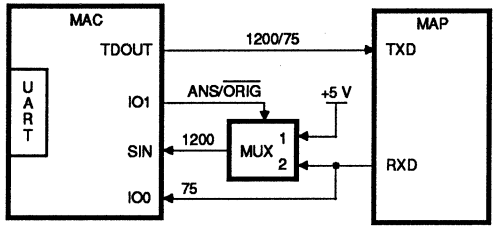


Figure 1a. Parallel Mode

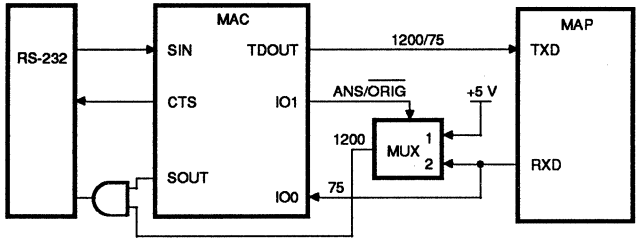


Figure 1b. Serial Mode

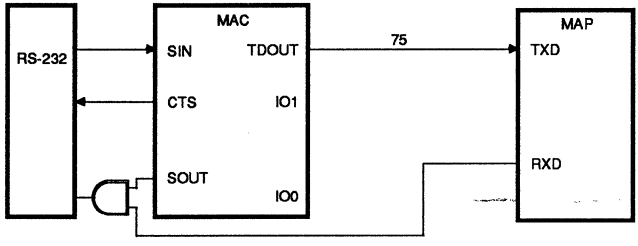


Figure 1c. Serial Mode—V.23 Originate Only

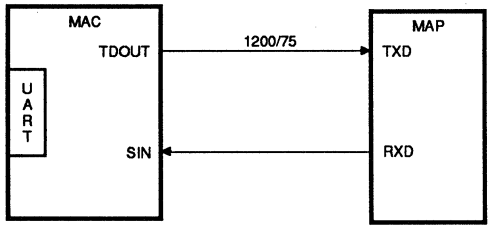


Figure 1d. Parallel Mode—V.23 Originate Only

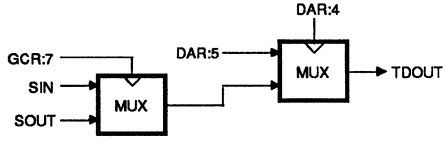
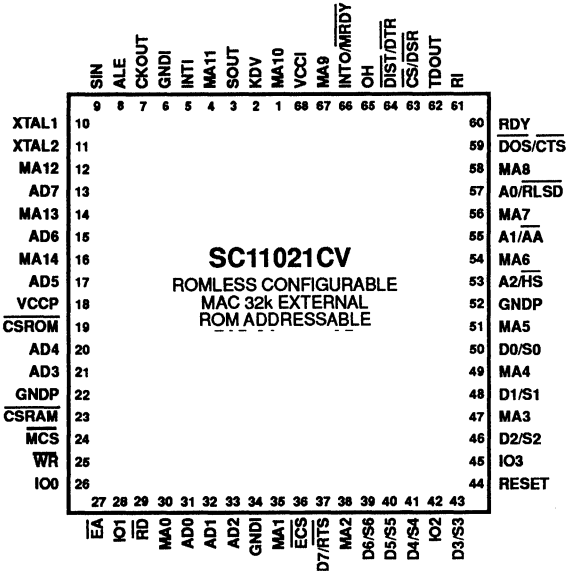
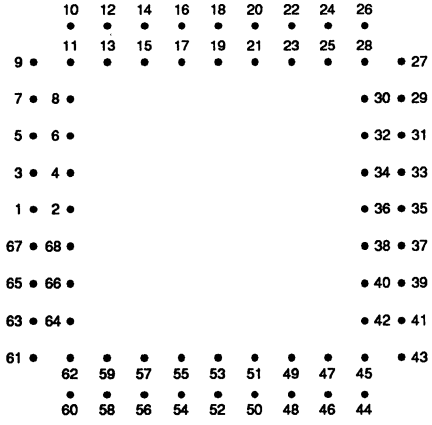


Figure 1e. TDOUT Function

CONNECTION DIAGRAM FOR THE MODEM CONTROLLER





68-Pin Socket (Underside View)

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	SCR	Synchronous Clock Receive (Data set source); Output; TTL; Used only in bit synchronous mode; Recovered by the Receiver Phase Locked Loop from the far end modem. Data on RXD is valid at the rising edge of this clock.
2	AGND	Analog Ground.
3	SCT	Synchronous Clock Transmit (Data set source); Output; TTL; Used only in bit synchronous mode; Generated internally by the SC11026 Clock Generator; Rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
4	SCTE	Synchronous Clock Transmit External (DTE source); Input; TTL; Used only in bit synchronous mode; Data on TXD line is latched by the SC11026 at the rising edge of this clock. Clock rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
5	AUDIO	Audio output; The hybrid output is passed through a programmable attenuator and fed to this analog pin. Four different levels can be attained by controlling bit 0 and bit 1 of the AUDIO register as specified under AUDIO register description.
6	EDC	Capacitor for energy detect; A 1.0 μF capacitor should be connected between this pin and AGND.
7	DGND	Digital ground
8	$\overline{CS}$	Chip Select; Input; TTL; Active low.
9	$\overline{WR}$	Write; Input; TTL; Normally high; Data on AD7–AD0 is written into the SC11026 registers at the rising edge of this pulse.
10	$\overline{RD}$	Read; Input; TTL; Normally high; Data on AD7–AD0 is to be read by the processor at the rising edge of this pulse.
12,13,17,18	AD1–AD4	Multiplexed address/data bus (8-bits); Input/Output; TTL; A/D4–A/D1 (4-bits) are used for multiplexed addressing of internal registers. CMOS.
14	V_{SS}	–5 V Supply
15	RXA	Receive analog; Input
16	TXA	Transmit analog; Output
11,19–21	D0, D5–D7	D2–D7 data I/O CMOS; Bits 0, 5, 6 and 7 are don't cares as far as address is concerned.
22	CLKIN	Clock input; 9.8304 MHz or 12.288 MHz clock input from the controller.
23	GS	Gain Select to compensate for loss in line coupling transformer. When left open or tied to V_{SS}, the compensation is 0 dB; connected to ground, +2 dB compensation is provided; and when tied to V_{CC}, the compensation is +3 dB.
24	ALE	Address Latch Enable; Input; TTL; The address on A/D4–A/D1 is latched into the SC11026 Address decoder at the falling edge of this normally low pulse.
25	INT	Interrupt; Output; TTL; Normally low; A short (13 μs typical) positive pulse is generated after all A to D conversions are completed.
26	RXD	Received Data; Output; TTL
27	TXD	Transmit Data; Input; TTL
28	V_{CC}	+5 V supply

REGISTERS

There are twelve 8-bit registers interfacing to the microprocessor bus. Five of these registers can only be read by the processor (called READ registers) and the remaining seven can be written into by the processor (called CONTROL registers). Bit 1 of "TONE" register can be read and written by the processor. Table 1 shows the address and bit assignments for these registers.

A chip select pin is provided for multi-peripheral addressing by the processor.

Table 1. READ Registers

ADDRESS BITS				NAME	MSB			BIT NUMBER				LSB
A4	A3	A2	A1		7	6	5	4	3	2	1	0
0	0	0	0	Q1	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
0	0	0	1	I1	I17	I16	I15	I14	I13	I12	I11	I10
0	0	1	0	Q2	Q27	Q26	Q25	Q24	Q23	Q22	Q21	Q20
0	0	1	1	I2	I27	I26	I25	I24	I23	I22	I21	I20
0	1	0	0	Status	T390	T2225	T2100	AGCO	T1300	T1650	FSKD	ED
0	1	X	1	Unused		Unused						
0	1	1	X	Unused		Unused						

STATUS Register: Address (A4–A1) = 0100

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–5*	T390,T2225 T2100	Outputs of the tone detector. When any of these bits is set, the corresponding frequency has been detected.
Bit 4	AGCO	Status of internal 1-bit AGC. When this bit is set, RXA signal is amplified by 8 dB before entering the bandpass filters.
Bit 3	T1300	
Bit 2	T1650	
Bit 1	FSKD	Received FSK data. FSKD = 1 when mark is received.
Bit 0	ED	Energy detect circuit output. ED = 1 when energy detected.

Note 1: To detect any of the tones ENTD bit (MCRB) must be set.
Note 2: When reading unused bits, the corresponding bus lines will not be driven by the SC11026 and will be floating.

Table 1a. READ Registers

Q1 Register:	Stores midbaud inphase sample output of ADC.
I1 Register:	Stores midbaud quadrature sample output of ADC.
Q2 Register:	Stores endbaud inphase sample output of ADC.
I2 Register:	Stores endbaud quadrature sample output of ADC.

Note: All samples are represented in two's complement form.

Table 2. CONTROL Registers

ADDRESS BITS				NAME	BIT NUMBER							
A4	A3	A2	A1		7	6	5	4	3	2	1	0
1	0	0	0	TXCR	V23	HYBRID	TXSEL2	TXSEL1	TXSEL0	SQT	BR1	BR0
1	0	0	1	MCRA	GDFLAT	LCK/$\overline{INT}$	RNGX	SYNC	WLS1	WLS0	A/$\overline{O}$	RXMRK
1	0	1	0	MCRB	ANS/$\overline{ANS}$	ENTD	TL3	CPM	ALB	TL2	TL1	TL0
1	0	1	1	TONE	X	HNDSHK	TONEON	DTMF	D3	D2	D1	D0
1	1	0	0	PGCR	X	AGCVT	G5	G4	G3	G2	G1	G0
1	1	0	1	DATA	X	PLLJAM	PLLFRZ	PLLFAST	RD3	RD2	RD1	RD0
1	1	1	0	AUDIO	X	DISS	PGCZ	TST2	TST1	TST0	ALC1	ALC0
1	1	1	1					UNUSED				

CONTROL REGISTERS

Transmit Control Register (TXCR): Address (A4–A1) = 1000

(Note: When writing into these registers, the bus lines corresponding to the unused bits are ignored by the SC11026.)

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	V23	When set, the chip is configured in V.23 mode. This bit overrides BR0 and BR1.
Bit 6	HYBRID	When set, the transmitter output (TXA) is connected to the inverting input of the receive buffer to allow the use of the on-chip hybrid circuit for 2 to 4 wire conversion.
Bit 5 Bit 4 Bit 3	TXSEL2 and TXSEL1 and TXSEL0	Transmit Select bits. These 3 bits determine the data transmitted by the transmitter according to the following table:

TXSEL2	TXSEL1	TXSEL0	TRANSMITTED DATA
0	0	0	External data sent by DTE.
0	0	1	Unscrambled S1 (Note 1).
0	1	0	Unscrambled Space.
0	1	1	Unscrambled Mark.
1	0	0	Scrambled RX. Digital loop back mode (Note 2).
1	0	1	Scrambled Reversals (Notes 3 and 4).
1	1	0	Scrambled Space (Note 4).
1	1	1	Scrambled Mark (Note 4).

Note 1: S1 is a pattern of 0011 transmitted at 1200 bps rate regardless of BR1. If in FSK mode (BR0 = 1), then reversals are sent. This pattern cannot be sent at 2400 bps rate.

Note 2: In this mode, the received data, after being descrambled, is sent back to the scrambler. The modem will automatically go to the Synchronous mode with Slave timing.

Note 3: Reversals are continuous streams of 01.

Note 4: When in FSK mode (BR0 = 1), TXSEL2 is ignored since scrambling is not applicable.

Bit 2	SQT	When this bit is set, the transmitter is squelched by connecting the output of MUX1 (see the block diagram) to analog ground.
Bit 1 Bit 0	BR1 and BR0	Bit Rate Selection bits based on the following table:

BR1	BR0	BIT RATE
0	0	2400 bps V.22 bis
1	0	1200 bps V.22/212A
0	1	0–300 bps Bell 103
1	1	0–300 bps CCITT V.21

CONTROL REGISTERS (Cont.)

Mode Control Register A (MCRA): Address (A4–A1) = 1001

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	GDFLAT	When set, the group delay of the transmit Band Split Filters will be flat. When clear, the Filter group delay response is Compromise Delay.
Bit 6	LCK/INTB	Determines the clock source for the transmitter. When this bit is set, the clock source is externally provided on SCTE (pin 4), and when cleared, it is internally generated (SCT). This bit can select the clock source independent of Sync/Async mode selection (see below). When in Digital Loop-Back mode, the clock source will be forced to the Slave mode (SCR).
Bit 5	RNGX	Range extender for the receiver Sync/Async converter. When set, the receiver Sync/Async can insert up to one stop bit per four (8, 9, 10 or 11-bit) characters to compensate for a far end DTE being up to 2.3% over speed. The transmitter Async/Sync always handles this overspeed condition regardless of this bit's condition.
Bit 4	SYNC	When set, operate in bit synchronous mode; when clear, operate in character asynchronous mode. When in Digital Loop-Back mode, the SC11026 will be forced to the Synchronous mode.
Bit 3 and Bit 2	WLS1 and WLS0	Word length select bits in asynchronous mode, according to the following table:

WLS1	WLS0	NUMBER OF BITS PER CHARACTER
1	0	8
1	1	9
0	0	10
0	1	11

Bit 1	A/$\overline{O}$	When set, operate in answer mode; when clear, operate in originate mode.
Bit 0	RXMARK	When set, the RXD pin is clamped to the high logical level.

Mode Control Register B (MCRB): Address (A4–A1) = 1010

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	ANS/$\overline{ANS}$	Switching this bit from 0 to 1 or 1 to 0 will reverse the phase of the 2100 Hz Answer Tone.
Bit 6	ENTD*	This bit must be set to enable the tone detector.
Bit 5	TL3	When set, the transmit level is further attenuated by 1 dB. (See TL0–TL2)
Bit 4	CPM	Call progress monitor mode. When set, the receive path can be connected to the high band filter to detect answer tone (ALB=0) or to the low band filter scaled down 2.5 times (ALB=1) to listen for the call progress tones during auto dialing.
Bit 3	ALB	Analog Loop Back. When set, the transmitter output (TXA) is connected to the receive path, bypassing the receive filter.
Bit 2 and Bit 1 and Bit 0	TL2 TL1 TL0	Transmit level adjust bits based on the following table:

TL2	TL1	TL0	TRANSMIT LEVEL AT TXA PIN
0	0	0	0 dBm
0	0	1	–2 dBm
0	1	0	–4 dBm
0	1	1	–6 dBm
1	0	0	–8 dBm
1	0	1	–10 dBm
1	1	0	–12 dBm
1	1	1	–14 dBm

* It is up to the user to make sure that the expected tone falls within the passband of the filter. If the receive filter is set to forward channel V.23 mode, all tones except 390 Hz can be detected. The 390 Hz tone can be detected when modem is in V.23 reverse channel mode.

CONTROL REGISTERS (Cont.)

TONE Register: Address (A4–A1) = 1011

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	HNDSHK	This bit is set only during handshaking sequence. When set, both FSK and PSK/QAM demodulators are enabled. When cleared, FSK demodulator is disabled when in high speed mode.
Bit 5	TONEON	When set, the output of the tone generator appears at TXA. When cleared, the output of the tone generator is squelched.
Bit 4	DTMF*	When set, the DTMF generator is turned on. When cleared, the DTMF generator is turned off, but other tones can be generated.
Bits 3–0	D3–D0	Specify the desired tone (see the following table):

DTMF	D3	D2	D1	D0	DIGIT DIALED	TONE OUTPUT	FREQUENCIES (HZ)
1	0	0	0	0	0	941	1336
1	0	0	0	1	1	697	1209
1	0	0	1	0	2	697	1336
1	0	0	1	1	3	697	1477
1	0	1	0	0	4	770	1209
1	0	1	0	1	5	770	1336
1	0	1	1	0	6	770	1477
1	0	1	1	1	7	852	1209
1	1	0	0	0	8	852	1336
1	1	0	0	1	9	852	1477
1	1	0	1	0	*	941	1209
1	1	0	1	1	(A)	697	1633
1	1	1	0	0	(B)	770	1633
1	1	1	0	1	(C)	852	1633
1	1	1	1	0	#	941	1477
1	1	1	1	1	(D)	941	1633
0	0	0	0	0	No tone; tone generator turned off		
0	0	0	0	1	550		
0	0	0	1	0	1800		
0	0	0	1	1	2100		
0	0	1	0	0	1300		
0	0	1	0	1	No tone; tone generator turned off		
0	0	1	1	x	No tone; tone generator turned off		
0	1	x	x	x	No tone; tone generator turned off		

Note: TONEON must also be set to generate DTMF signals.

Programmable Gain Controller Register (PGCR): Address (A4–A1) = 1100

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	AGCVT	When set, prevents gain hit due to AGC's gain step. This bit must be set during the handshaking after detecting the four point constellation and before switching to 16-way decision making.
Bits 5–0	G5–G0	Control the gain of the PGC within a range from –10 to +37.5 dB in 0.75 dB steps. (See the following table):

CONTROL REGISTERS (Cont.)

G5	G4	G3	G2	G1	G0	PGC GAIN (dB)
0	0	0	0	0	0	–10.0
0	0	0	0	0	1	–9.25
0	0	0	0	1	0	–8.5
0	0	0	1	0	0	–7.0
0	0	1	0	0	0	–4.0
0	1	0	0	0	0	+2.0
1	0	0	0	0	0	+14.0
1	1	1	1	1	1	+37.25

Note: Signal level is adjusted (before entering the filter) by an internal AGC with +12 dB or 0 dB gain, plus a fixed gain of 5 dB.

DATA Register: Address (A4–A1) = 1101

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	PLLJAM	When this bit is set, the DPLL will be reset by the next rising edge of the received baud clock. This bit must remain high for at least one baud period. It should be cleared by the processor to end the jamming mode. PLLFRZ (see below) overrides PLLJAM when both are enabled.
Bit 5	PLLFRZ	Phase locked loop freeze. When this bit is set, the DPLL begins to run freely regardless of the received baud clock. To re-enable the DPLL locking, the bit must be cleared by the processor. PLLFRZ overrides PLLJAM when both are enabled.
Bit 4	PLLFAST	When set, the DPLL operates in "fast" locking mode. In this mode, the DPLL is updated on every baud period by 13 µs steps. When this bit is cleared (default mode), the DPLL operates in "normal" locking mode and is updated once every 8 baud periods by 6.5 µs steps.
Bit 3–0	RD3–RD0	Four-bit Received Data. Used only in high speed (1200 or 2400 bps) mode, they are descrambled by the processor and shifted out by the SC11026. Sync to Async is also done by the SC11026, when in the asynchronous mode. RD0 is the first bit appearing on the RXD pin, followed by RD1, RD2 and RD3. In the 1200 bps mode, only RD0 and RD1 are shifted out during one baud period.

AUDIO Register: Address (A4–A1) = 1110

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	DISS	When this bit is set, the scrambler is disabled, when cleared, it is enabled. Transmit select bits (TXSEL0–2) override this bit when in "transmit internal mode".
Bit 5	PGCZ	When set, the output of the PGC is grounded. DC offset of the demodulator can be stored and canceled by the controller.
Bit 4–2	TEST	Test bits used for factory testing. For normal chip operation, these bits must be cleared.
Bit 1	ALC1	Audio level control bit 1.
Bit 0	ALC0	Audio level control bit 0. These two bits are used to control the audio level at AUDIO pin according to the following table:

ALC1	ALC0	AUDIO ATTENUATION (dB)
0	0	Audio off
0	1	12
1	0	6
1	1	0 (no attenuation)

Note: The audio signal may be amplified by 12 dB by the line receiver AGC before being fed to the audio attenuator.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1—SC11026 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 3.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11026 in the synchronous mode. This provides a 2400/1200 Hz clock on the SCT pin that can be used as a clock source for the DTE. The Transmit Phase-Locked-Loop (TX PLL) of the SC11026 will be in free-running mode.

Case 2—SC11026 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode, also select "Locked" mode.

The TX PLL of SC11026 will then synchronize itself to the clock provided on its "SCTE" pin.

Case 3—Slave mode. The Transmit Timing is slaved to the receiver recovered clock. Select synchronous mode and connect SCTE to SCR.

In any case, the SC11026 will sample the data on the rising edge of the clock.

Receiver Timing

In synchronous mode, the recovered clock will be provided on the SCR pin and the transitions of RXD will be on the falling edges of this clock. Data is valid on the rising edge of the clock.

SYNCHRONOUS MODE CHART

Transmitter Timing

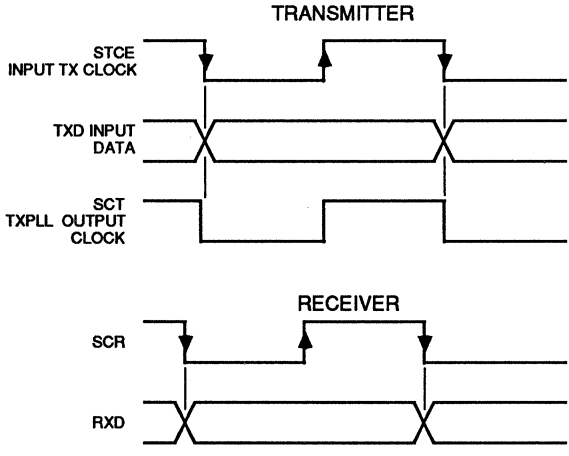


Figure 3. SC11026 Synchronous Mode Timing Diagrams.

SPECIFICATIONS

Absolute Maximum Ratings (Notes 1–3)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS}–0.6 to V_{CC} +0.6 V
DC Input Voltage (Digital Signals)	V_{SS}–0.6 to V_{CC} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
F_C	Clock Frequency		9.8295	9.8304	9.8313	MHz
T_R, T_F	Input Rise or Fall Time	All digital inputs except CLKIN			500	ns
T_R, T_F	Input Rise or Fall Time	CLKIN			20	ns

DC Electrical Characteristics (T_A = 0 TO 70°C, V_{CC} = +5 V ± 10%, V_{SS} = –5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	Normal		18	35	mA
I_{SS}	Quiescent Current			18	35	mA
V_{IH}	High Level Input Voltage; Digital pins		2.4			V
V_{IL} TTL CMOS	Low Level Input Voltage; Digital pins				0.8 0.3 x V_{CC}	V
V_{OH} TTL CMOS	High Level Output (I_{OH} = 0.5 mA)		2.4 0.7 x V_{CC}			V
V_{OL} TTL CMOS	Low Level Output (I_{OL} = 1.6 mA)				0.6 0.3 x V_{CC}	V
VXTA	Maximum Peak Output Level on TXA pin	V_{CC} = +5 V V_{SS} = –5 V	±3			V

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

SPECIFICATIONS (Cont.)

AC Electrical Characteristics

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
		Processor Bus Interface: (See Figure 4)					
1	TAVLL	Address valid to end of ALE		41			ns
2	TLLAX	Address hold after end of ALE		61			ns
3	TAVDV	Address valid to output data valid				336	ns
4	TRLDV	$\overline{RD}$ active low to output data valid				194	ns
5	TRXDZ	End of $\overline{RD}$ to output data Hi Z				61	ns
6	TLHLL	ALE pulse width		71			ns
7	TRLRH	$\overline{RD}$ pulse width		214			ns
8	TWLWH	$\overline{WR}$ pulse width		148			ns
9	TQVWX	Data valid to end of $\overline{WR}$ active		132			ns
10	TWXQX	Data hold after end of $\overline{WR}$		56			ns
11	TLLRL	End of ALE to $\overline{RD}$ or $\overline{WR}$ active		60			ns
12	TRHLH	End of $\overline{RD}$ to next ALE		55			ns
13	TWXLH	End of $\overline{WR}$ to next ALE		120			ns

BUS TIMING

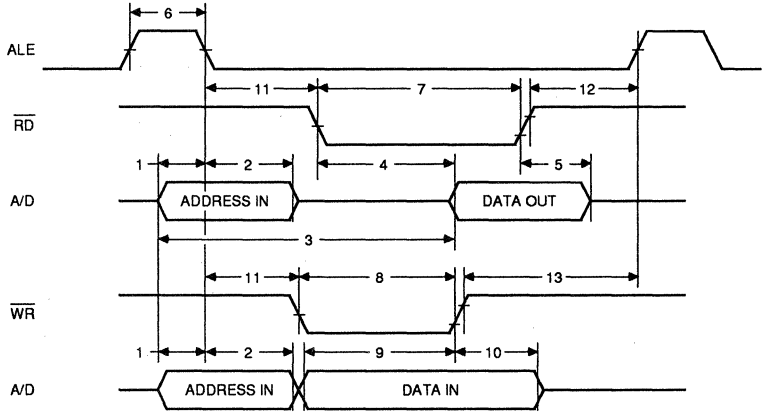


Figure 4. Processor Bus Timing

SPECIFICATIONS (Cont.)

Modem Transmit Signals—Hz (Assume 9.8304 Crystal)

PARAMETER	CONDITIONS	NOM.	ACT.	UNITS
FSK Mod/Demod Frequencies				
Bell 103				
Answer Mark		2225	2226	Hz
Answer Space		2025	2024.4	Hz
Originate Mark		1270	1269.4	Hz
Originate Space		1070	1070.4	Hz
CCITT V.21				
Answer Mark		1650	1649.4	Hz
Answer Space		1850	1850.6	Hz
Originate Mark		980	978.34	Hz
Originate Space		1180	1181.53	Hz
CCITT V.23				
Answer Mark		1300	1300.3	Hz
Answer Space		2100	2100.5	Hz
Originate Mark		390	389.3	Hz
Originate Space		450	450.1	Hz

Call progress monitor mode:		MIN	TYP	MAX	
Center frequency	ALB = 1		480		Hz
Detect level (ED high) measured at RXA		–43			dBm
Reject level (ED low) measured at RXA				–48	dBm
Hysterisis		2			dB
Delay time (ED low to high)	EDC = 1.0 µF	10	15	24	ms
Hold time (ED high to low)	EDC = 1.0 µF	10	15	24	ms

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQUENCY	ALLOWABLE ERROR	ACTUAL ERROR
Row 1	697 Hz	±1%	–0.23%
Row 2	770 Hz	±1%	–0.01%
Row 3	852 Hz	±1%	–0.12%
Row 4	941 Hz	±1%	–0.39%
Column 1	1209 Hz	±1%	–0.35%
Column 2	1336 Hz	±1%	–0.93%
Column 3	1477 Hz	±1%	–0.48%
Column 4	1633 Hz	±1%	–0.91%
Guard Tones	550 Hz	±20 Hz	–2 Hz
	1800 Hz	±20 Hz	–2 Hz
Calling Tone	1300 Hz		–6 Hz
Answer Tone	2100 Hz		+3 Hz

SPECIFICATIONS (Cont.)

DTMF Generator (Cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion	VCC = +5 V VSS = –5 V TL3 = TL2 = TL1 = TL0 = 0 Measured at TXA Pin		–40		dB
Row Output Level			0		dBm
Column Ouput Level			2		dBm
550 Hz Guard Tone			–3		dB (Note 2)
1800 Hz Guard Tone			–6		dB (Note 2)
1300 Hz Calling Tone			0		dB
2100 Hz Answer Tone			0		dB
Transmit level measured at TXA	Load = 1200 Ohms TL3 = TL2 = TL1 = TL0 = 0 Squelched		0	 –50	dBm dBm

Notes: 1: This assumes a clock of exactly 9.8304 MHz.

2: These levels are referenced to the TX signal level. When guard tones are added, the TXA level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Mode	EDC = 1.0 µF; measured at RXA PGC = 0				
Energy detect level (ED low to high)				–43	dBm
Loss of energy detect level (ED low to high)		–48			dBm
Hysterisis		2	3		dB

Programmable Gain Controller (PGC)

Gain step size			0.75		dB
Dynamic range			47.25		dB
Response time (from change in PGC register to output of A to D converter)			1.0		ms

Filter Characteristics

Crosstalk rejection			70		dB
Power supply rejection			0		dB
DPLL Response times JAM or FRZ Fast			20 200		µs µs

APPLICATIONS INFORMATION

Applications

The SC11026 with an external control microprocessor, a telephone line interface and a suitable computer interface, can implement a complete 2400 bps modem for many applications with a minimum of components and cost. Figure 7 shows the common portion of such a modem using the SC11026 with a telephone line interface. Sierra's SC22101, 128 byte E^2 memory is used to store default parameters and often used phone numbers. The SC11021 controller also supports a serial E^2 memory as an alternative. Figures 6 and 7 show the stand-alone and PC bus integral modems implemented with Sierra's SC11021 controllers. Figure 8 shows the connections for an internal ROM special purpose controller. Figure 9 shows an RS-232C serial interface for implementing a stand-alone modem. Figure 10 shows a parallel bus interface for implementing an internal modem for an IBM PC/XT/AT compatible computer as shown in Figure 6, while Figure 13 shows the interface required for implementing the same internal modem when used with the controller shown in Figure 12. Figure 11 shows a power supply schematic for a stand-alone modem application.

Various modem configurations can be realized by combining schematics shown in Figures 5 thru 13.

A Hayes compatible stand-alone smart modem (Fig. 5) can be implemented by combining Figures 7, 8, 9 and 11.

The internal version for an IBM PC/XT/AT compatible (Fig. 6) can be implemented using Figures 7, 8 and 10.

An Alternative to the controller of Figure 8 is shown in Figures 12 and 13.

For performance evaluation, the circuit shown in Figure 14 can be used to obtain the receiver constellation. Quality of the signal processing performed by the modem can thus be visualized by observing the constellation for various line conditions and signal to noise ratios.

Crystal Oscillator

The controller requires a parallel resonant 19.6608 MHz crystal designed with CL = 18 pF and tolerance of ±0.01% (such as Saronix NYP196-18). With this crystal, use 27 pF to ground from XTAL1 (Pin 10) and XTAL2 (Pin 11). Clock frequency measured at CKOUT (Pin 7) must be within ±0.01% of 9.8308 MHz.

Power Supply Decoupling and Circuit Layout Consideration

For optimum performance at low received signal levels with low s/n ratios, it is important to use the recommended power supply decoupling circuit as shown in Figure 7.

Small inductors in series with the supplies help suppress RFI as well as improve the power supply noise rejection capability of the SC11026. A 10 Ω, 1/4 W resistor in place of, or in series with, the inductor in the SC11026 power leads has been found to be helpful in computer based products where the power supplies are particularly noisy.

The 10 μF capacitors should be a tantalum type while the 0.1 μF capacitors should have good high frequency rejection characteristics—monolithic ceramic types are recommended. It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11026 as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply. Avoid routing digital traces through the analog area.

Ferrite beads on the ±5 V input to the circuit board should also be considered, both from a modem performance standpoint, as well as an aid in reducing RF radiation from the phone lines.

APPLICATIONS INFORMATION (Cont.)

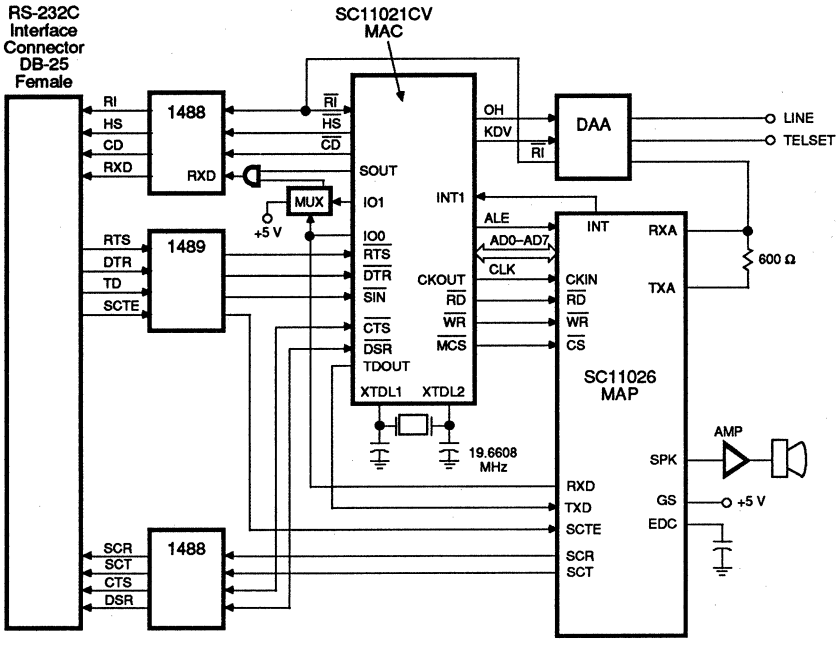


Figure 6a. V22 bis Standalone Intelligent Modem with External ROM. (Not Shown) (With V.23 Answer and Originate Modes)

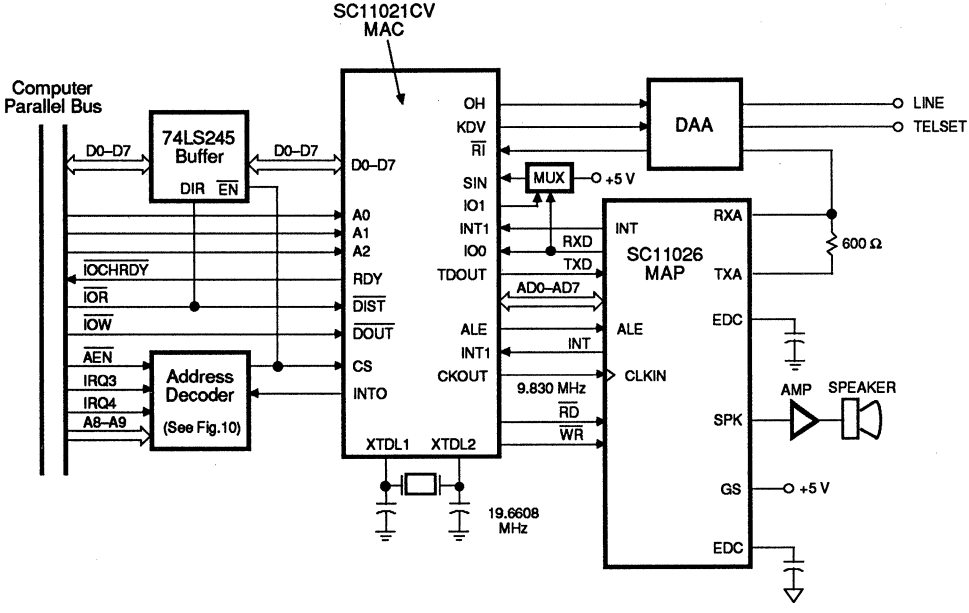
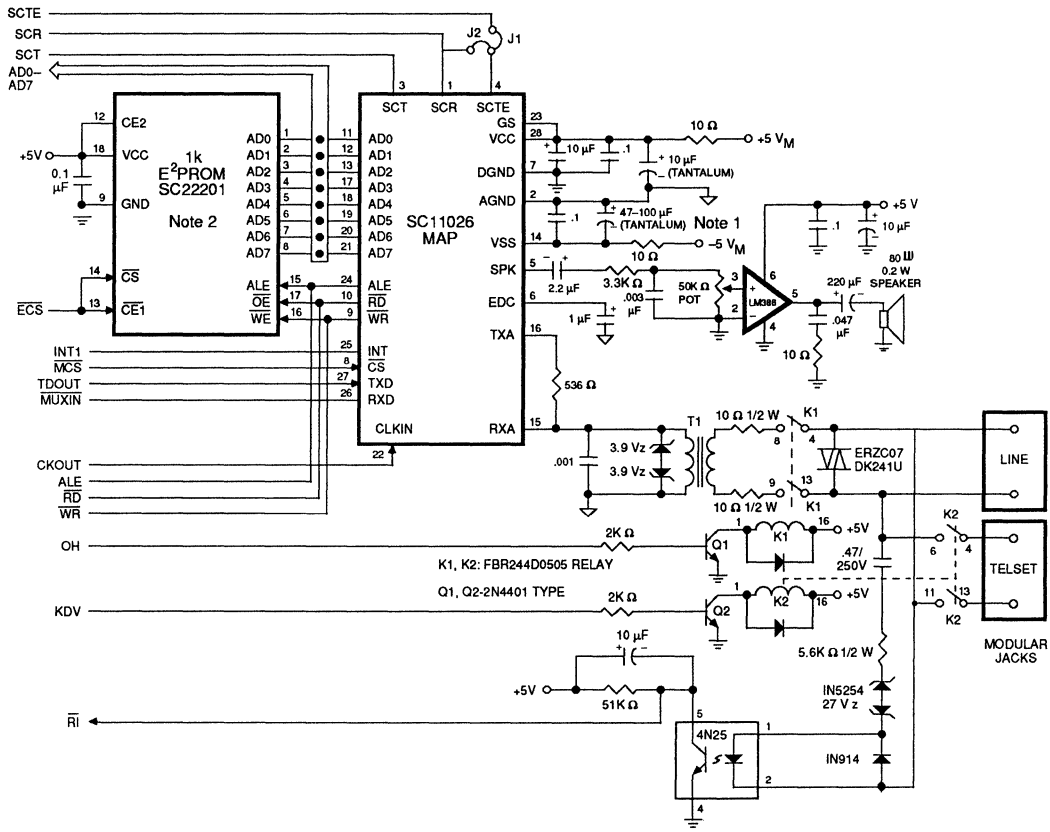


Figure 6b. Internal Smart Modem for PC Bus Applications with External ROM. (Not Shown) (With V.23 Answer and Originate Modes)

APPLICATIONS INFORMATION (Cont.)



Note 1: Connect analog ground directly to common of the power supply filter capacitor.

Note 2: A serial E² PROM may be substituted when using the SC11021 Modem Advanced Controller.

Note 3: For external clocking of the transmitter, install J1 and set bit 6 of the MCRA; omit J2.
For slave clocking of the transmitter, install J2 and set bit 6 of the MCRA; omit J1.
For normal operation, omit J1 and J2, and clear bit 6 of the MCRA.

Figure 7. Common Portion of 2400 bps Modem.

CONFIGURATIONS FOR SC11021CV AND SC11022CV CONTROLLERS

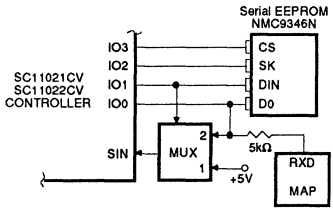
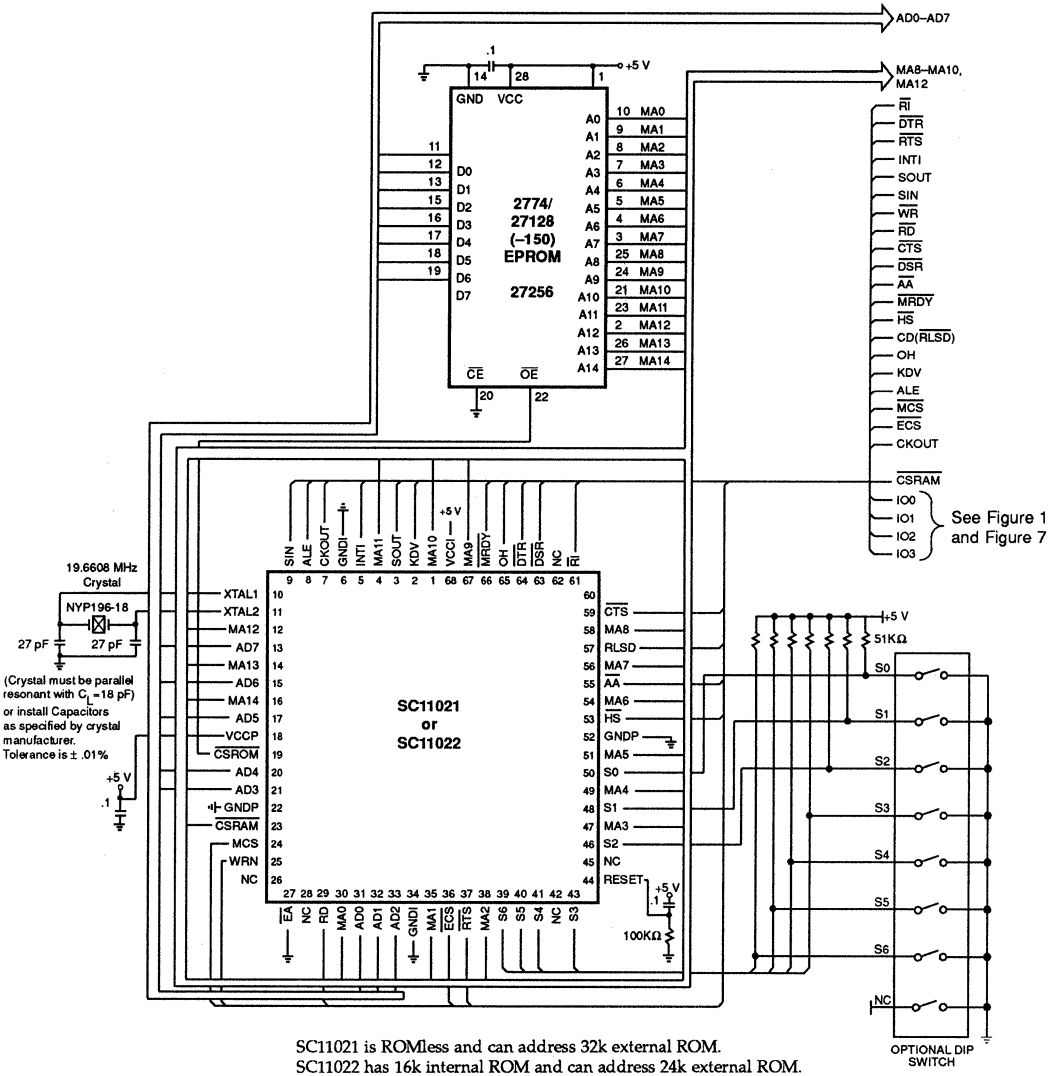


Figure 7b.

The I/O pins may be used to drive a serial E²PROM in addition to controlling the V.23 mux switch as shown. When reading from the E²PROM, the RXD output should be set high since the DOUT pin of the E²PROM has greater pull-down capability than pull-up. The 5 kΩ resistor must be added to isolate RXD since it is not tristatable.

In the majority of applications where answer mode is not required, there is no conflict and the I/O pins can be dedicated to the serial E²PROM function and RXD connected as shown in Figure 1, page 8.

APPLICATIONS INFORMATION (Cont.)



SC11021 is ROMless and can address 32k external ROM.
SC11022 has 16k internal ROM and can address 24k external ROM.
Consult controller data sheet for programming information.

Figure 8. Special Purpose Control Processor for Stand-Alone or Parallel Applications.

APPLICATIONS INFORMATION (Cont.)

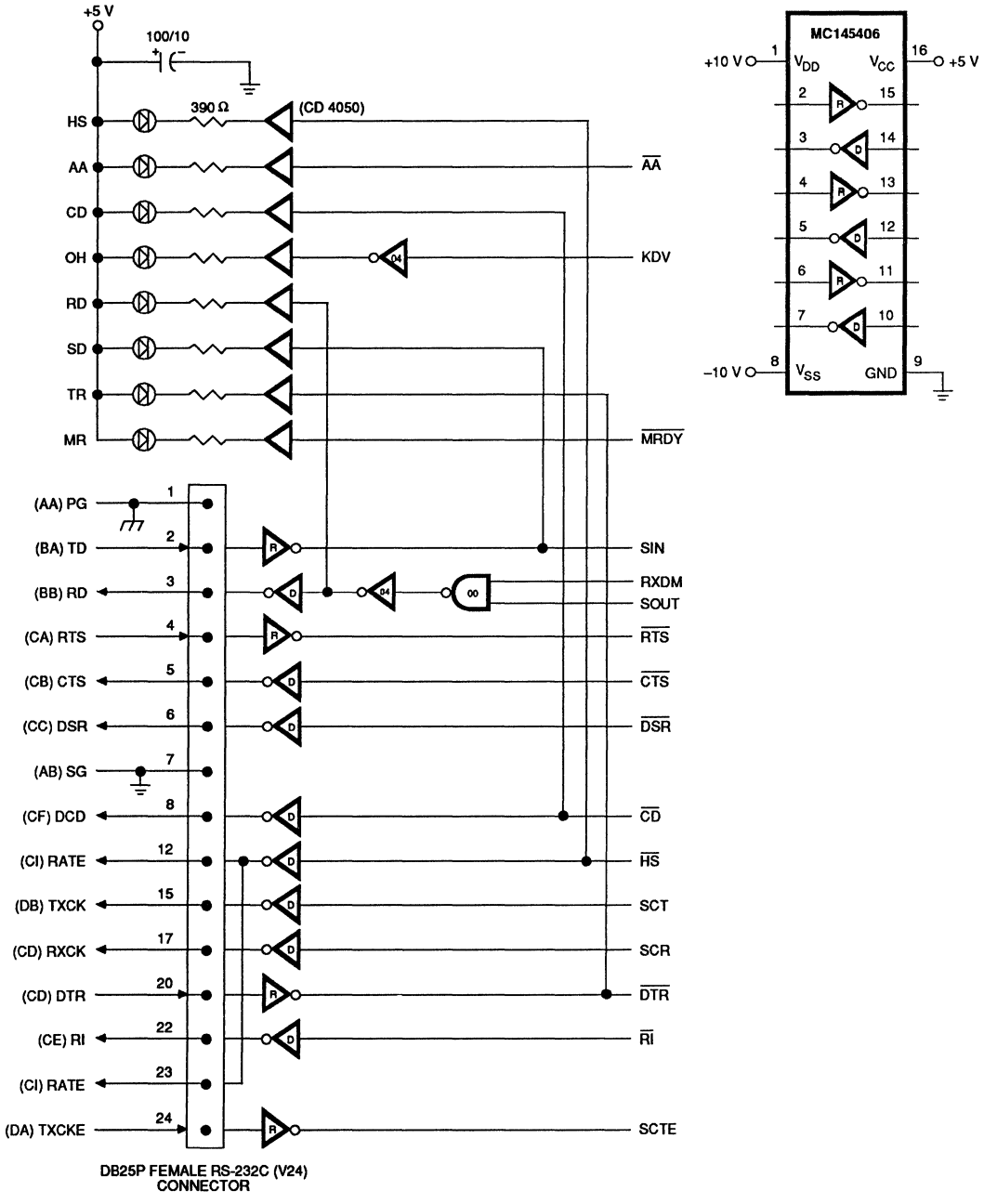


Figure 9. RS-232C Interface for Stand-Alone Modem Application.

APPLICATIONS INFORMATION (Cont.)

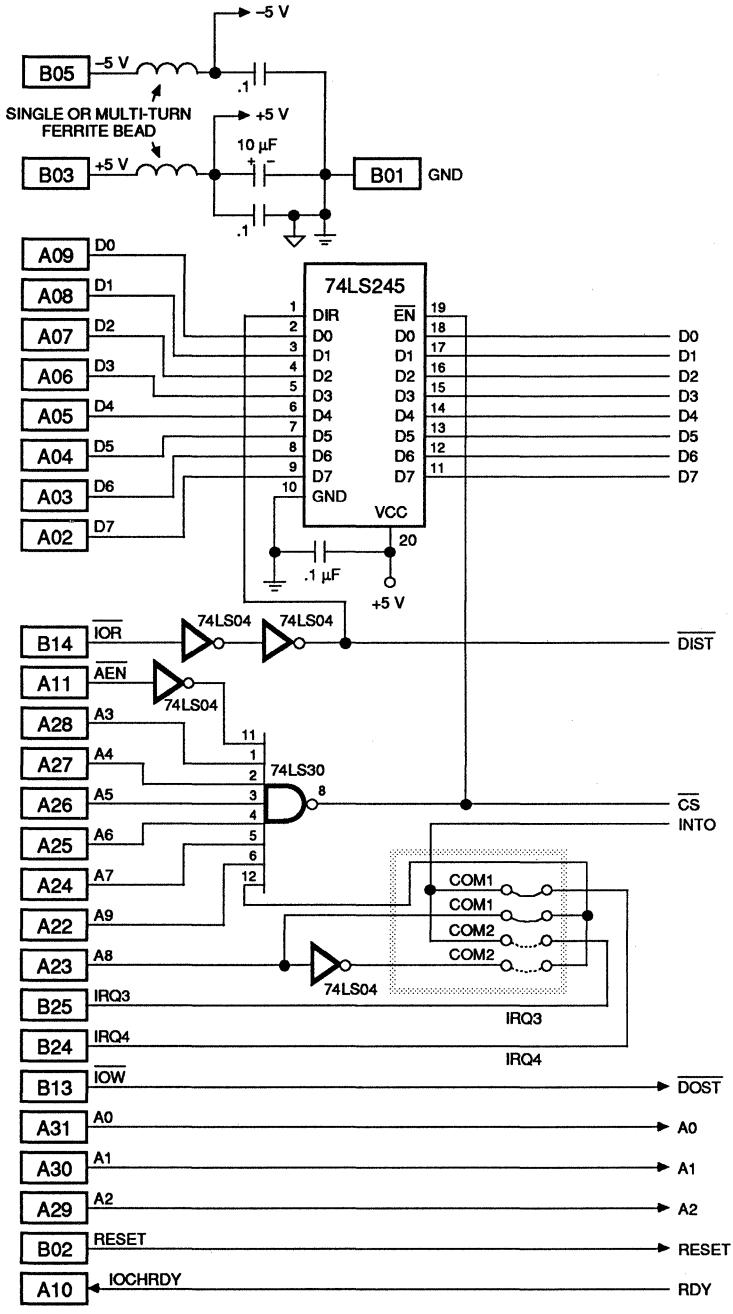


Figure 10. IBM PC/XT/AT Compatible Computer Bus Interface for SC11039 Controller of Figure 7.

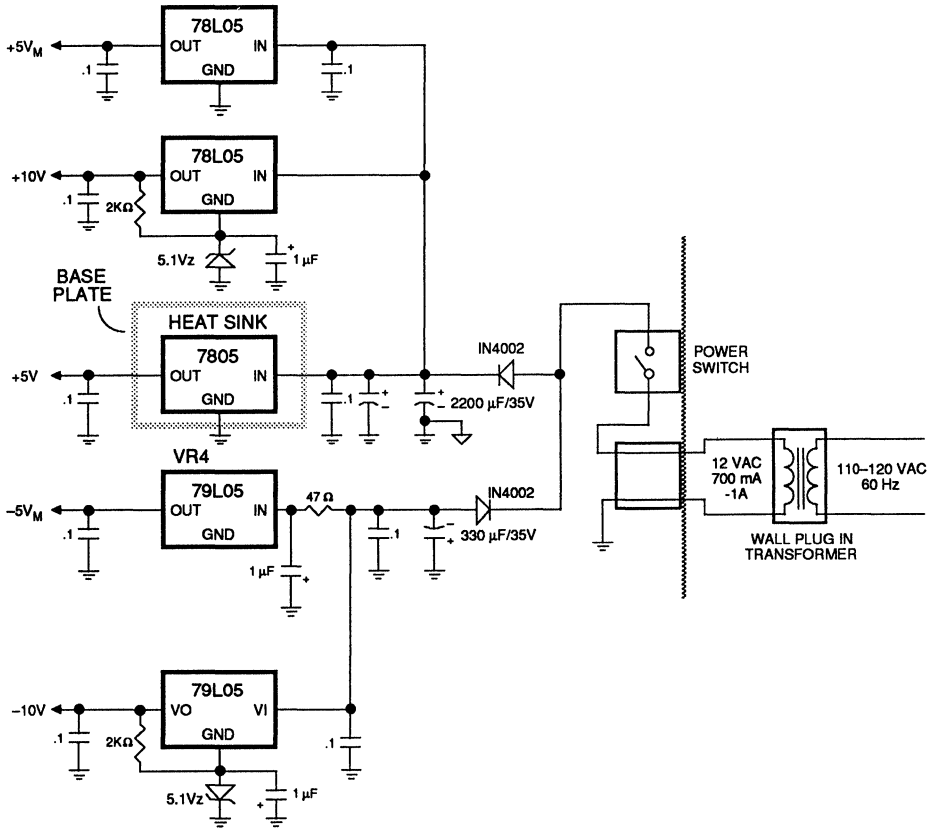
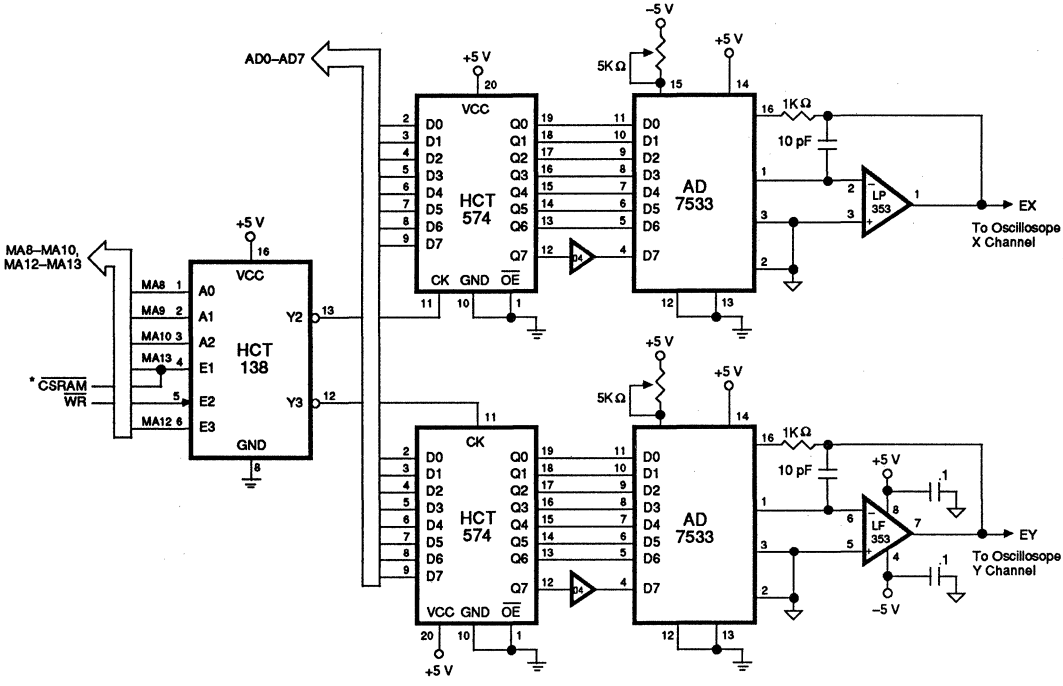


Figure 11. A Typical Power Supply for Stand-Alone Modem Application.

APPLICATIONS INFORMATION (Cont.)



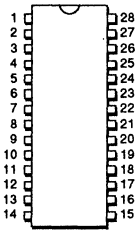
*IF THE SC11039, SC11021 FAMILY IS USED, CONNECT $\overline{\text{CSRAM}}$, IF AN 8096 IS USED, CONNECT MA13.

Figure 14. Test Circuit to Generate "Eye Pattern".

FEATURES

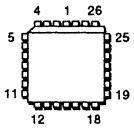
- ☐ Direct interface to SC11016 single chip modem
- ☐ Complete "AT" command set in firmware
- ☐ Auto power down
- ☐ Built-in UART
- ☐ Direct IBM PC XT bus interface
- ☐ 28-pin DIP or PLCC package

28-PIN DIP PACKAGE



SC11027CN

28-PIN PLCC PACKAGE

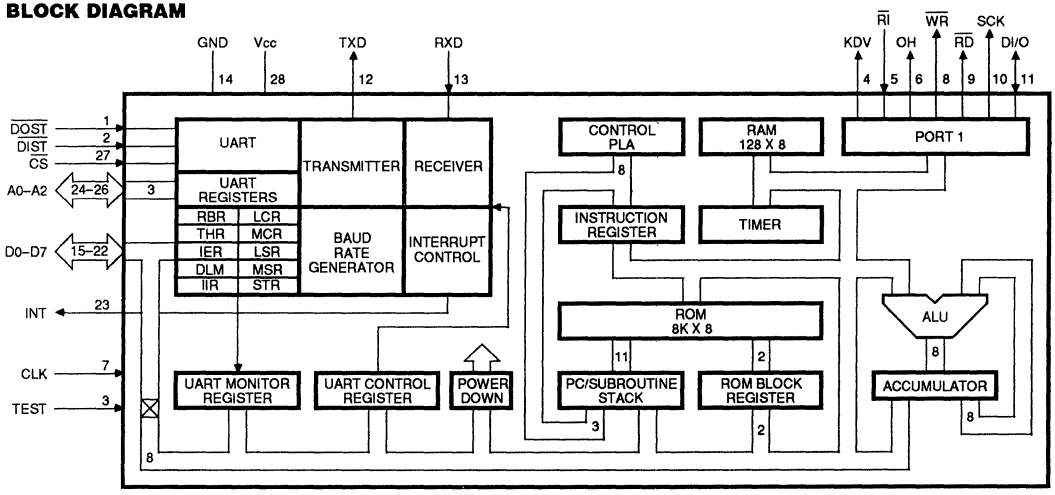


SC11027CV

GENERAL DESCRIPTION

The SC11027 Modem Interface Controller is specifically designed to control Sierra's 5-Volt only SC11016 single chip, 300/1200 bit per second modem. Built with Sierra's proprietary CMOS process, the SC11027 provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to the SC11016, with the addition of a data access arrangement (DAA), the SC11027 implements a Hayes-type smart modem for board level, integral modem applications. Because the SC11027 fully emulates the functionality of the 8250B UART with increased speed, and includes data bus transceivers, it can be directly interfaced to a computer's parallel data bus and in particular to the bus of the IBM PC XT (for PC AT applications, see SC11037). All of the popular communications software written for the PC will work with the SC11016/SC11027 chip set. The SC11027 contains an 8-bit microprocessor, 8k bytes of ROM and 128 bytes of RAM. For specific high volume applications, the control program can be modified by Sierra to include additional commands and functions.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE SAME FOR BOTH DIP & PLCC.

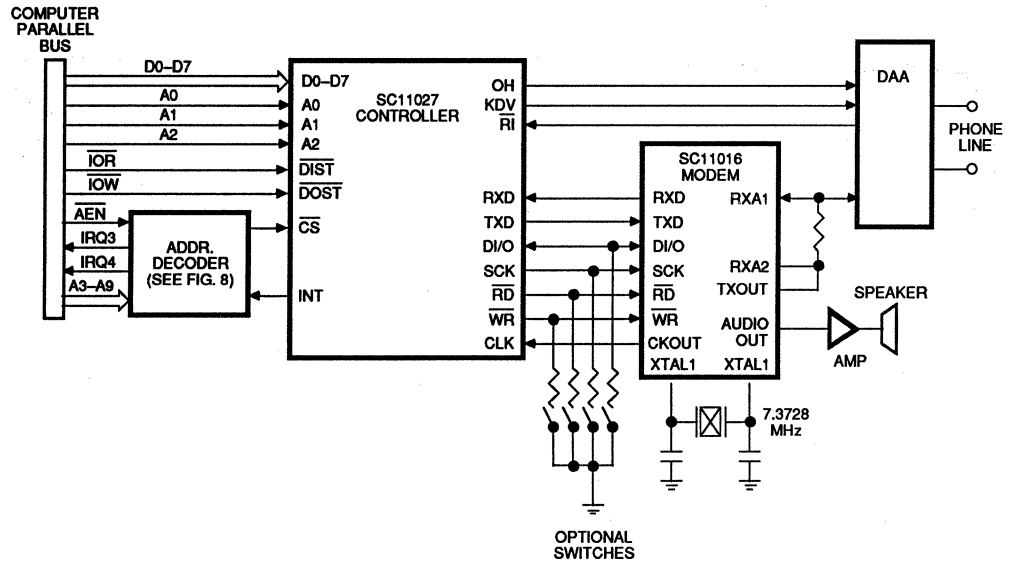


Figure 2. Integral Smart Modem Configuration for PC Bus Applications

PIN/FUNCTION DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	$\overline{DOST}$	I	The CPU can write data or control words into a selected register of the SC11027 when $\overline{DOST}$ is low and the chip is selected. Data is latched on the rising edge of the signal.
2	$\overline{DIST}$	I	The CPU can read data or status information from a selected register of the SC11027 when $\overline{DIST}$ is low and the chip is selected.
3	TEST	I	When the test input is high, the SC11027 enters a test mode—used for factory testing only. It mustbe connected to ground for normal operation.
4	KDV	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. During a data call, the SC11027 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
5	$\overline{RI}$	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the On duration of the ring cycle. This is a Schmidt Trigger input, allowing for slow rising and falling signals on this pin. $\overline{RI}$ causes the SC11027 to automatically power-up the SC11016 modem.
6	OH	0	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the SC11027 pulses this output at a rate of 10 pulses per second with appropriate mark/space ratio depending on 212A or V.22 mode.
7	CLK	I	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the SC11016 modem is connected to this pin. All internal timing is derived from this clock.
8	$\overline{WR}$	I/O	This pin is used to initiate writing of data to the SC11016 modem. On power-up, it is an input for a brief time in which the SC11027 reads the carrier status switch connected to this pin. If the switch is closed to ground thru an 18 kΩ resistor, the SC11027 sets the Received Line Signal Detect (RLSD) bit in the Modem Status Register. If the switch is open or tied to V_{CC} thru 18k, the SC11027 resets this bit and writes the actual status of the carrier detector during a data call. However, NO switch is required, since an internal pullup sets the status during power-up to the default state (pullup to V_{CC}) which is to follow the remote modem's carrier.

Pin No.	Pin Name	I/O	Description
9	$\overline{RD}$	I/O	This pin is used to initiate reading of data from the SC11016 modem. On power-up, this pin is an input for a brief time in which the SC11027 reads the DTR status switch connected to this pin. If this switch is open or tied to V_{CC} thru 18k, the SC11027 reacts to the status of the DTR bit in the UART Modem Control Register. If the switch is closed to ground thru 18k Ω, the SC11027 ignores the state of the DTR bit. When the switch is open, writing a 0 to the DTR bit in the Modem Control Register forces the SC11027 into the command state and when on line, causes it to hang up. However, NO switch is required, since an internal pullup to V_{CC} sets the status during power-up to the default state—to follow the DTR status.
10	SCK	I/O	The SC11027 supplies a shift clock on this pin to the SC11016 modem for reading or writing data. On power-up, this pin is an input for a brief time in which the SC11027 reads the Bell/CCITT select switch connected to this pin. If this switch is open or tied to V_{CC} thru 18k, Bell protocol is selected. If this switch is closed to ground 18 kΩ, CCITT V.22 protocol is selected. However, NO switch is required, since an internal pullup sets the status during power-up to the default state—212A mode.
11	DI/O	I/O	The SC11027 shifts data serially out of this pin to SC11016 during a write operation and shifts data serially into this pin during a read operation from the SC11016. On power-up this pin is an input for a brief time in which the SC11027 reads the Make/Break ratio select switch connected to this pin for selecting the pulse dialing standard. With the switch open or tied to VCC thru 18k, the Bell standard 39% Make, 61% Break is selected. With the switch closed to ground thru 18 kΩ, the CCITT standard 33% Make, 67% Break is selected. However, NO switch is required, since an internal pullup sets the status during power-up to the default state—Bell standard.
12	TXD	O	During a data call, after the connection is established, the SC11027 converts parallel data received from the computer bus and outputs it in a serial, asynchronous format to the SC11016 modem for modulation. At all other times the SC11027 holds this output in the Mark (high) condition.
13	RXD	I	Demodulated data from the SC11016 modem is received on this pin during a data call. A high level is considered Mark and a low level is a Space. The SC11027 converts the serial data into a parallel data byte and stores it in the Receiver Buffer Register (RBR). The Data Ready bit in the Line Status Register (LSR) is then set, and an appropriate interrupt indentification code is written in the Interrupt Identification Register (IIR) to signal to the computer, the reception of a new data byte.
14	GND	—	Ground reference (0 Volts).
15–22	D0–D7	I/O	This is the 8 bit data bus comprising of three state input/output lines. This bus provides bidirectional communication between the SC11027 and the CPU. Data, control words and status information are transferred via the D0–D7 data bus. Because on-chip high drive buffers are used, no external transceiver IC, such as the 74LS245, is needed between the computer bus and the SC11027.
23	INT	O	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER: Receiver Line Status Flag, Received Data Available, Transmitter Holding Register Empty and Modem Status. It is reset low upon the appropriate interrupt servicing. The INT pin is forced to a Hi-Z state when the OUT2 bit of the Modem Control Register (MCR) is low (power on state).
24–26	A0–A2	I	These three address inputs are used during read or write operation to select a UART register in the SC11027 as shown in Table 1. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2.
27	$\overline{CS}$	I	The SC11027 is selected when this input is low. When high, the SC11027 forces the Data bus lines into a high impedance state.
28	V_{CC}	—	Positive supply (+5 Volts).

SC11027 SPECIFICATIONS

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read only) (RBR)
0	0	0	0	Transmitter Holding (write only) (THR)
0	0	0	1	Interrupt Enable (IER)
X	0	1	0	Interrupt Identification (read only) (IIR)
X	0	1	1	Line Control (LCR)
X	1	0	0	Modem Control (MCR)
X	1	0	1	Line Status (LSR)
X	1	1	0	Modem Status (read only) (MSR)
X	1	1	1	Speed (STR)
1	0	0	0	Divisor Latch (LSB) (write only) (DLL)
1	0	0	1	Divisor Latch (MSB) (write only) (DLM)

Table 1. SC11027 UART Registers

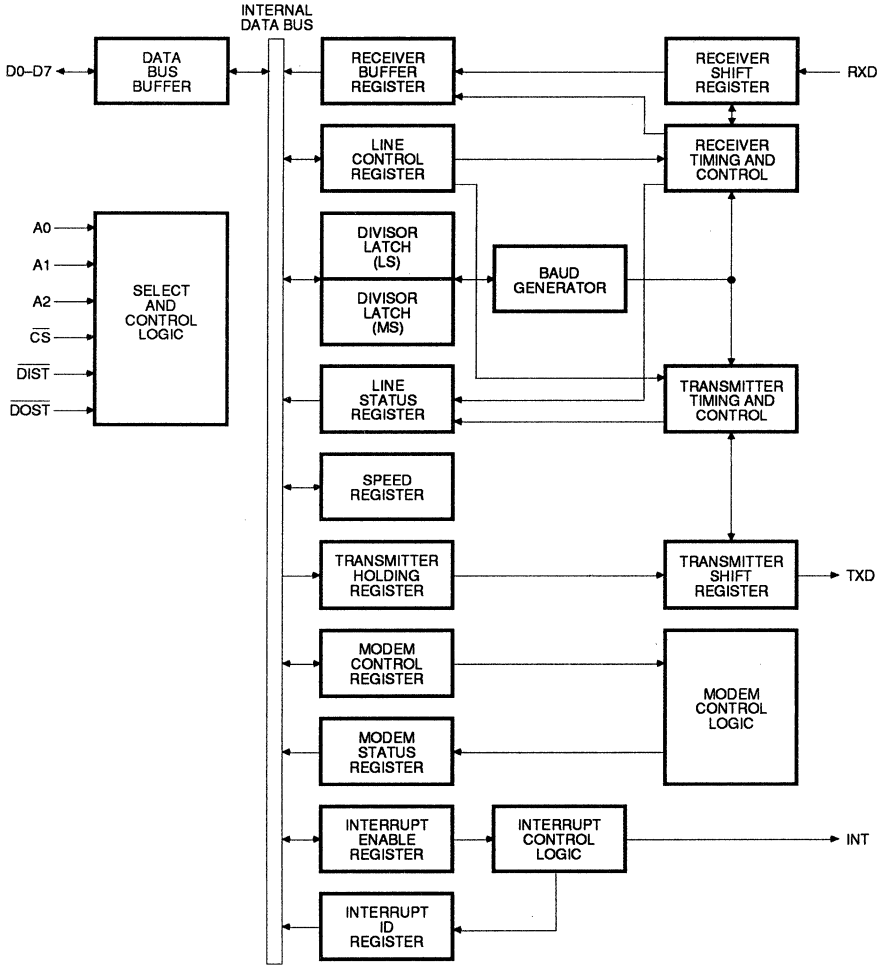


Figure 3. UART Block Diagram

Name	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
RBR	Data	Data	Data	Data	Data	Data	Data	Data
THR	Data	Data	Data	Data	Data	Data	Data	Data
IER	Receive Data Available Interrupt Enable	THRE Interrupt Enable	Receive Line Status Interrupt Enable	Modem Status Interrupt Enable	0	0	0	0
IIR	0 If Interrupt Pending	Interrupt ID Bit 0	Interrupt ID Bit 1	0	0	0	0	0
LCR	0 = 7 Bit Data 1 = 8 Bit Data	1	0 = 1 Stop Bit 1 = 2 Stop Bits	1 = Parity Enable	1 = Even Parity	1 = Stick Parity	1 = Set Break	DLAB
MCR	Data Terminal Ready	Request to Send	OUT1	OUT2 0 = INT Output to HI-Z	No Function	0	0	0
LSR	Data Ready	Overrun Error	Parity Error	Framing Error	Break Interrupt	THRE	TSRE	0
MSR	0	0	Trailing Edge Ring	Delta RLSD	1 (CTS)	1 (DSR)	Ring	RLSD
DLM	Data	Data	Data	Data	Data	Data	Data	Data
STR	Data	Data	Data	Data	Data	Data	Data	Data

Table 2. SC11027 UART Register Function Summary

Register	Range/Units	Description	Default
S0	0–255 rings	Ring to answer telephone on	0
S1	0–255 rings	Number of rings	0
S2	0–127 ASCII	Escape code character	43(+)
S3	0–127 ASCII	Character recognized as carriage return	13(CR)
S4	0–127 ASCII	Character recognized as line feed	10(LF)
S5	0–32, 127 ASCII	Character recognized as back space	8(BS)
S6	2–255 sec.	Wait time for dial tone	2
S7	1–255 sec.	Wait time for carrier	30
S8	0–255 sec.	Pause time (caused by comma)	2
S9	1–255 1/10 sec.	Carrier detect response time	6
S10	1–255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50–255 millisec.	Duration and spacing of Touch-Tones	70
S12	20–255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	—
S14	bit mapped	Option register	—
S15	bit mapped	Flag register	—
S16	0,1,2,4	Test modes	0

Table 3. SC11027 S Registers (Software Registers) Used by AT Commands

Command	Desc. (Notes 1 and 2)
Prefix, Repeat and Escape Commands	
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; + + + is not followed by carriage return)
Dialing Commands	
D	Dial
P	Pulse*
T	Touch-Tone
,	Pause
!	Flash
/	Wait for 1/8 second
@	Wait for silence
W	Wait for second dial tone
;	Return to command state after dialing
R	Reverse mode (to call originate-only modem)

Command	Desc. (Notes 1 and 2)
Other Commands	
A	Answer call without waiting for ring
B/B0	CCITT V.22 mode (Note3)
B1	Bell 103 and 212A mode*
C/C0	Transmit carrier off
C1	Carrier on*
E/E0	Characters not echoed
E1	Characters echoed*
F/F0	Half duplex
F1	Full duplex*
H/H0	On hook (hang up)
H1	Off hook, line and auxiliary relay
H2	Off hook, line relay only
I/I0	Request product ID code (130)
I1	Firmware revision number
I2	Test internal memory
L/L1	Low speaker volume
L2	Medium speaker volume*
L3	High speaker volume
M/M0	Speaker always off
M1	Speaker on until carrier detected*
M2	Speaker always on

Command	Desc. (Notes 1 and 2)
Other Commands	
O	Go to on-line state
O1	Remote digital loopback off*
O2	Remote digital loopback request
Q/Q0	Result codes displayed*
Q1	Result codes not displayed
Sr?	Requests current value of register r
Sr=n	Sets register r to value of n
V/V0	Digit result codes
V1	Word result codes*
X/X0	Compatible with Hayes-type 300 modems*
X1	Result code CONNECT 1200 enabled
X2	Enables dial tone detection
X3	Enables busy signal detection
X4	Enables dial tone and busy signal detection
Y/Y0	Long space disconnect disabled*
Y1	Long space disconnect enabled
Z	Software reset: restores all default settings

Notes: 1. Default Modes are indicated by *.
2. Commands entered with null parameters assume 0-X is the same as X0.
3. When used with the SC11016 modem IC, which has CCITT V.21 as well as V.22 modes, when the ATB command is used, in the answer mode, the SC11027 will put the SC11016 in either the V.21 mode or the V.22 mode, depending on the response from the remote modem. In the originate mode, the SC11027 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the SC11016 accordingly.

Table 4. Command Summary

Digit Code	Word Code	Description
0	OK	Command Executed
1	CONNECT	Connected at 300 or 1200 bps.
		Connected at 300 bps., if result of X1, X2, X3 or X4 command
2	RING	Ringing signal detected (Note 1)
3	NO CARRIER	Carrier signal not detected or lost
4	ERROR	Illegal command
		Error in command line
		Command line exceeds buffer (40 character, including punctuation)
		Invalid character format at 1200 bps.
5	CONNECT 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	NO DIALTONE	Dialtone not detected and subsequent commands not processed. Results from X2 or X4 commands only.
7	BUSY	Busy signal detected and subsequent commands not processed. Results from X3 or X4 commands only.
8	NO ANSWER	Silence not detected and subsequent commands not processed. Results from @ command only.

Note 1. When the SC11027 detects a ringing on the telephone line, it sends a RING result code. However, the SC11027 will answer the call only if it is in auto-answer mode or is given an A command.

Table 5. Result Codes

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	+ 6 V
Input Voltage	-0.6V to V_{CC}+0.6
Storage temperature range	–65 to +150°C.
Maximum power dissipation @ 25°C.	500mW
Lead temperature (soldering, 10 sec)	300°C.
Operating temperature range	0 to 70°C.

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

DC ELECTRICAL CHARACTERISTICS

Param.	Description	Conditions	Min	Typ	Max	Units
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Operating Current	@ V_{CC} = 5V		10.0		mA
V_{ih}	High Level Input Voltage	all pins except $\overline{RI}$	2.0			V
V_{il}	Low Level Input Voltage	all pins except $\overline{RI}$			0.8	V
V_t+	Positive hysterisis threshold	$\overline{RI}$ pin		2.5		V
V_t–	Negative hysterisis threshold	$\overline{RI}$ pin		1.8		V
V_{oh}	High Level Output Voltage	Digital signal pins D0 to D7 & INT @ I_{oh} = 6mA All other output or I/O pins @ I_{oh} = 2mA	V_{CC} —1.0 V_{CC} —1.0			V V
V_{ol}	Low Level Output Voltage	Digital signal pins D0 to D7 & INT @ I_{ol} = 6mA All other output or I/O pins @ I_{ol} = 2mA			0.4 0.4	V V
I_l	Leakage Current (Note 2)			±1.0		uA
f_{clk}	Clock frequency		7.3721	7.3728	7.3725	MHz

Note 2. This applies to all pins except TEST, $\overline{WR}$, $\overline{RD}$, SCK, and the DI/O pins which have internal pullups.

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{DIW}	$\overline{DIST}$ Strobe Width	1TTL Load	300		ns
t_{RC}	Read Cycle Delay	1TTL Load	300		ns
RC	Read Cycle = t_{DIW} + t_{RC} + 20 ns	1TTL Load	620		ns
t_{DDD}	Delay from $\overline{DIST}$ to Data	1TTL Load		300	ns
t_{HZ}	$\overline{DIST}$ to Floating Data Delay	1TTL Load	60		ns
t_{DOW}	$\overline{DOST}$ Strobe Width	1TTL Load	300		ns
t_{WC}	Write Cycle Delay	1TTL Load	300		ns
WC	Write Cycle = t_{DOW} + t_{WC} + 20 ns	1TTL Load	620		ns
t_{DS}	Data Setup Time	1TTL Load	60		ns
t_{DH}	Data Hold Time	1TTL Load	40		ns
t_{DIC}	$\overline{DIST}$ Delay from Select	1TTL Load	80		ns
t_{DOC}	$\overline{DOST}$ Delay from Select	1TTL Load	50		ns
t_{ACR}	Address and Chip Select Hold Time from $\overline{DIST}$	1TTL Load	10		ns
t_{ACW}	Address and Chip Select Hold Time from $\overline{DOST}$	1TTL Load	70		ns
Receiver					
t_{RINT}	Delay from $\overline{DIST}$ (Read RBR) to Reset Interrupt	100 pF Load		1	µs
Transmitter					
t_{HR}	Delay from $\overline{DOST}$ (Write THR) to Reset Interrupt	100 pF Load		1	µs
t_{IRS}	Delay from Initial INTR Reset to Transmit Start			1	Baud Cycle
t_{SI}	Delay from Initial Write to Interrupt			1	Baud Cycle
t_{SS}	Delay from Stop to Next Start			1	µs
t_{STI}	Delay from Stop to Interrupt (THRE)			1	Baud Cycle
t_{IR}	Delay from $\overline{DIST}$ (Read IIR) to Reset Interrupt (THRE)	100 pF Load		2.2	µs

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Power On Reset	All Bits Low
Interrupt Identification Register	Power On Reset	Bit 0 High; Bits 1–7 Low
Line Control Register	Writing into the LCR	Data
MODEM Control Register	Power On Reset	All Bits Low
Line Status Register	Power On Reset	Bits 0–4, 7 Low; Bits 5 and 6 High
Modem Status Register	Power On Reset	Bits 0–3, 6–7 Low; Bits 4–5 High
Divisor Latch (high order bits)	Power On Reset	1200 BPS
TXD	Master Reset	High
INT	Power On Reset	Low (High-Z)

Table 6. Reset Control of Registers and Pinout Signals

AC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = +5V ± 10%)

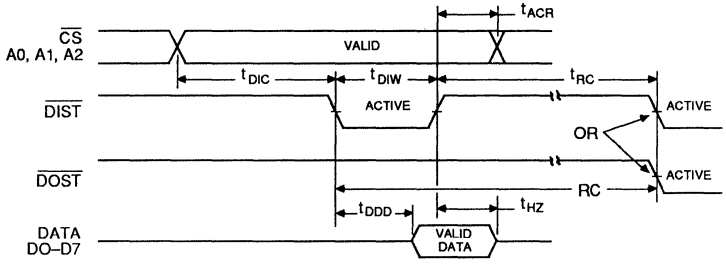


Figure 4. Read Cycle Timing

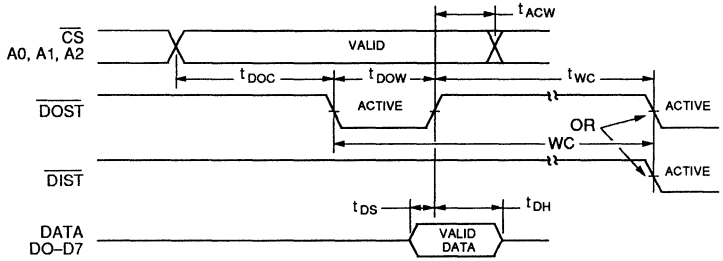


Figure 5. Write Cycle Timing

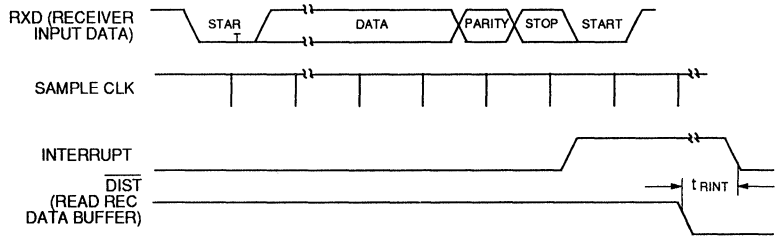


Figure 6. Receive Timing

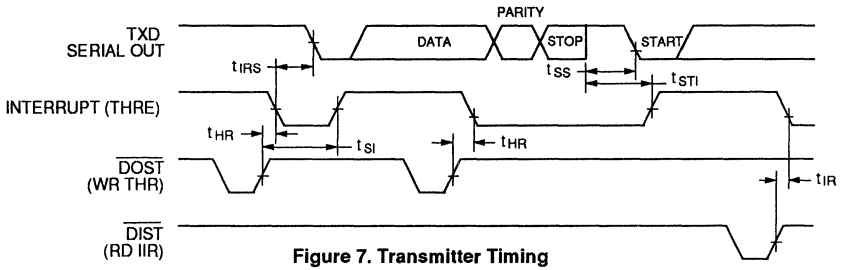


Figure 7. Transmitter Timing

UART REGISTERS

Line Control Register

This register controls the format of the asynchronous data communications.

Bits 0 and 1: Bit 1 is always high. Bit 0 specifies the number of bits in each transmitted or received serial character. The encoding of bit 0 is as follows:

Bit 1	Bit 0	Word Length
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1, when 7-bit word length with no Parity is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 0 is a logic 0 and bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed).

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is logic 1 and bit 5 is logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (TXD) is forced to the Spacing state (logic 0) and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Rate Generator

The SC11027's Baud Rate Generator can be programmed for one of six Baud rates. The desired speed is selected by writing into the Divisor Latch (DLM). On reset, the rate will be 1200 baud.

DLM (HEX Code)	Baud Rate
00	1200
01	300
03	150
04	110
06	75
09	50

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE bit is set to a logic 1 upon detection of parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time—the total time of Start bit + data bits + Parity + Stop bits.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the SC11037 is ready to accept a new character for transmission. In addition, this bit causes the SC11027 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register.

Bit 7: This bit is permanently set to logic 0.

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

UART REGISTERS

Interrupt Identification Register

The SC11027 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors. To provide minimum software overhead during data character transfers, the SC11027 prioritizes interrupts onto four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the source of that interrupt are stored in the Interrupt Identification Register (refer to Table 7). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 7.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the SC11027 to separately activate the Interrupt (INT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Register. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Interrupt Identification Register			Interrupt Set and Reset Functions			
B2	B1	B0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

MODEM Control Register

This 8-bit register controls the interface with the MODEM. The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls Data Terminal Ready (DTR) signal. If the external switch on the RD pin is set to V_{CC} thru an 18 kΩ resistor, setting the DTR low will force the SC11027 into the command state and, if on line, it will hang up.

Bit 1: This bit controls the Request to Send (RTS) signal. This signal is not used by the SC11027.

Bit 2: This bit controls the Output 1 (OUT 1) signal. This signal is not used by the SC11027.

Bit 3: This bit controls the Output 2 (OUT 2) signal. When OUT 2 is a 0, the interrupt output is in High-Z state.

Bit 4: Not used.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, two bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bit 0 and 1: These bits are always 0.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the carrier detector has changed state.

Bit 4: This bit is always 1.

Bit 5: This bit is always 1.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the Received Line Signal Detect (RLSD) signal.

Whenever bit 2 is set to logic 1, or bit 3 changes state, a MODEM Status Interrupt is generated if enabled.

APPLICATIONS

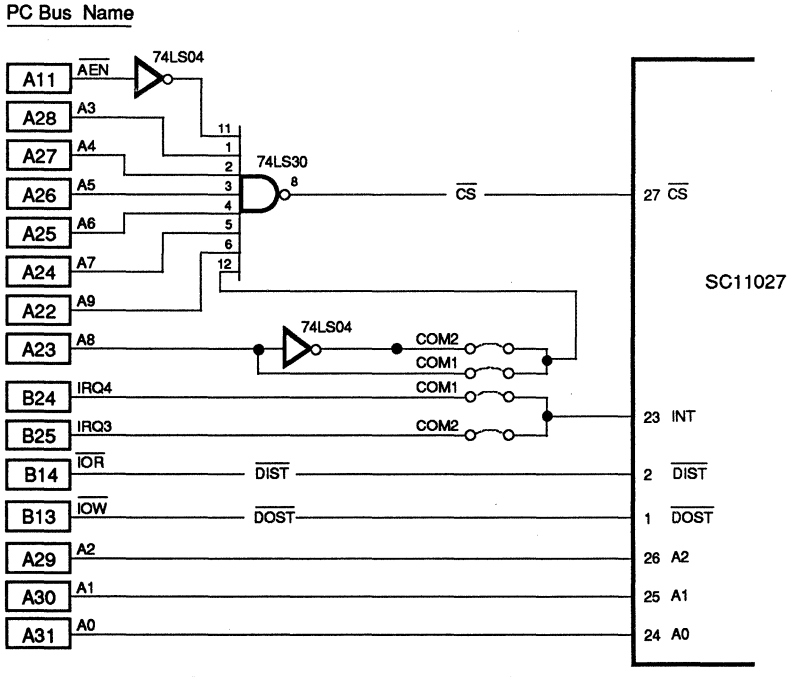
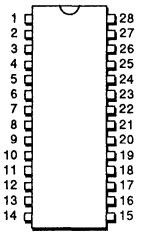


Figure 8. PC Bus Interface Address Decoder

FEATURES

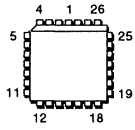
- ☐ Direct interface to SC11016 single chip modem
- ☐ Built-in UART for RS-232C interface
- ☐ Complete AT command set in firmware for intelligent modems
- ☐ 28-pin DIP or PLCC package

28-PIN DIP PACKAGE



SC11028CN

28-PIN PLCC PACKAGE

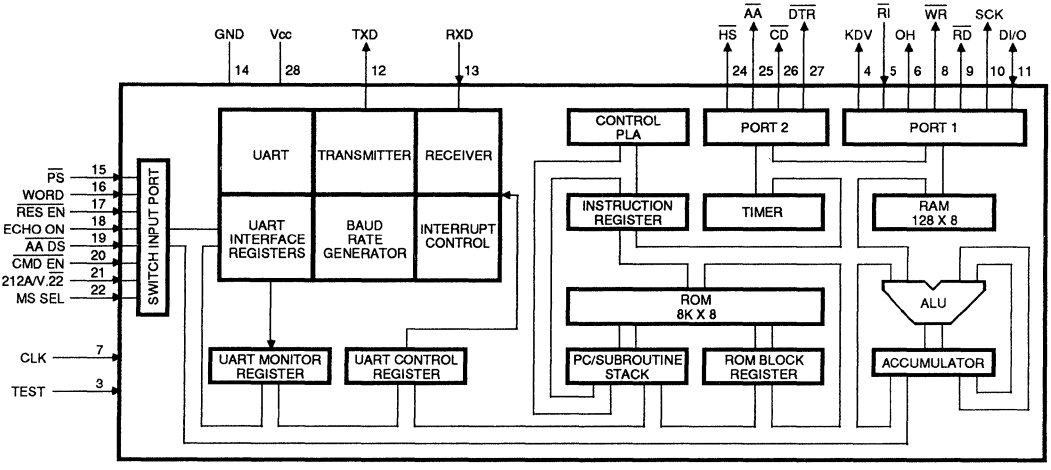


SC11028CV

GENERAL DESCRIPTION

The SC11028 Modem Interface Controller is specifically designed to control Sierra's 5 Volt only SC11016 single chip, 300/1200 bit per second modem. Built with Sierra's proprietary CMOS process, the SC11028 provides a highly cost effective solution for interfacing a modem IC to a computer's RS-232 port. When connected to the SC11016, with the addition of a data access arrangement (DAA), the SC11028 implements a Hayes-type smart modem for stand alone modem applications. The SC11028 automatically powers down the SC11016 when data terminal ready (DTR) is off or when the modem is "on-hook". All of the popular communications software written for the PC will work with the SC11016/SC11028 chip set. The SC11028 contains an 8-bit microprocessor, 8k bytes of ROM and 128 bytes of RAM and a UART. For specific high volume applications, the control program can be modified by Sierra to include additional commands and functions.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE FOR BOTH DIP & PLCC. PINS 1, 2, AND 23 ARE NOT CONNECTED.

PIN DESCRIPTIONS

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	N.C.	—	No connection
2	N.C.	—	No connection
3	TEST	I	When the test input is high, the SC11028 enters a test mode — used for factory testing only. For normal operation, this pin can be left open or connected to ground.
4	KDV	O	This output controls the operation of the data/voice relay. The polarity of this output is selected by $\overline{PS}$ pin. If $\overline{PS}$ is connected to ground, this output is active high, i.e. it is low when the modem is on hook, causing the data/voice relay to be off and the phone line is connected to the phone set. During a data call, this output goes high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads. If $\overline{PS}$ pin is left open or connected to V_{CC}, this output is active low, i.e. it is high when the modem is on hook and low when the modem makes a data call.
5	$\overline{RI}$	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the On duration of the ring cycle. This is a Schmidt Trigger input, allowing for slow rising and falling signals on this pin.
6	OH	O	This output controls the operation of the hookswitch relay in the DAA. The polarity of this output is selected by $\overline{PS}$ pin. If $\overline{PS}$ pin is connected to ground, this output is active high, i.e. it is low when the modem is on hook. During a data call, it goes high to operate the hookswitch relay and seize the phone line. During rotary dialing, the SC11028 pulses this output at a rate of 10 pulses per second with appropriate mark/space ratio depending on 212A or V.22 mode. If $\overline{PS}$ pin is left open or connected to V_{CC}, this output is active low, i.e. it is high when the modem is on hook and low during data call.
7	CLK	I	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the SC11016 modem is connected to this pin. All internal timing is derived from this clock.
8	$\overline{WR}$	O	This pin is used to initiate writing of data to the SC11016 modem.
9	$\overline{RD}$	O	This pin is used to initiate reading of data from the SC11016 modem.
10	SCK	O	The SC11028 supplies a shift clock on this pin to the SC11016 modem for reading or writing data.
11	DI/O	I/O	The SC11028 shifts data serially out of this pin to SC11016 during a write operation and shifts data serially into this pin during a read operation from the SC11016.
12	TXD	O	The SC11028 outputs serial data in asynchronous start/stop format at the data rate selected by the terminal. This data is either echo of commands received from the terminal or result codes generated by the controller during processing of the commands. This output is normally high and should be "AND"ed with the RXD output of the SC11016 to form RXD data to the terminal.
13	RXD	I	The SC11028 receives command data from the terminal on this pin. The UART in the controller connects the serial asynchronous start/stop data into a parallel byte for processing by the controller.
14	GND	—	Ground reference (0 V)
15	$\overline{PS}$	I	This input controls the polarity of KDV and OH outputs. When left open or connected to V_{CC}, it forces the KDV and OH output to be active low. If this input is connected to ground, KDV and OH outputs are active high.

PIN NO.	PIN NAME	I/O	DESCRIPTION
16	WORD	I	When this input is open or connected to V_{CC}, the SC11028 sends result codes as words. When this input is low, result codes are sent as digits. This setting can also be changed by entering the V command.
17	$\overline{\text{RES EN}}$	I	When this input is low, the SC11028 sends result codes. When this input is high or left open, commands received from the terminal are performed but result codes are not sent. This setting can also be changed by entering the Q command.
18	ECHO EN	I	When this input is high or left open, the SC11028 echoes characters received from the terminal in the command state. When this input is low, the SC11028 won't echo characters unless it is set for half duplex and it is on line. This setting can also be charged by entering the E command.
19	$\overline{\text{AA DIS}}$	I	When this input is low, the SC11028 won't answer incoming calls. When this input is high or left open, the SC11028 automatically answers incoming calls on the first ring. This function can also be enabled/disabled by writing to the S0 register.
20	$\overline{\text{CMD EN}}$	I	When this input is low, the SC11028 recognizes commands sent to it. For some applications such as unattended answering operation it is better to disable this function by leaving this input open or connecting it to V_{CC}.
21	212A/$\overline{\text{V.22}}$	I	When this input is open or connected to V_{CC}, the SC11028 supports Bell 103 and 212A modes. When this input is low, the SC11028 supports the CCITT V.22 and V.21 modes. This setting can also be charged by entering the B command.
22	MS SEL	I	When this input is open or connected to V_{CC}, the Mark/Space ratio is U.S. standard, 40/60 Make/Break. When it is low, the Mark/Space ratio is European standard, 33/67 Make/Break.
23	N.C.	—	No connection
24	$\overline{\text{HS}}$	O	This output, when low, indicates that the modem is in the high speed (1200 bps) mode. When high, it indicates that it is in the low speed (300 bps) mode. This output can be directly connected to a light emitting diode thru a 330 Ω resistor.
25	$\overline{\text{AA}}$	O	This output is low when the SC11028 is set for auto-answer mode, either by switch input $\overline{\text{AA DIS}}$ (pin 19) or register S0. The output goes high during each ring. If the device is not set to answer the phone (pin 19 is low or S0 = 0), this output goes low each time the phone rings. A light emitting diode thru a 330 Ω resistor can be directly connected to this output.
26	$\overline{\text{CD}}$	O	This output goes low when the SC11028 detects a carrier signal from the remote modem. If the connection is broken or never established, it remains high. A light emitting diode can be directly connected to this output thru a 330 Ω resistor.
27	$\overline{\text{DTR}}$	I	When this input is low, the SC11028 executes data call commands. If during a data call, this input goes high, the SC11028 terminates the data call, hangs up the phone line and returns to command state.
28	V_{CC}	—	Positive supply (+5 V)

Register	Range/Units	Description	Default
S0	0–255 rings	Ring to answer telephone on	0
S1	0–255 rings	Number of rings	0
S2	0–127 ASCII	Escape code character	43(+)
S3	0–127 ASCII	Character recognized as carriage return	13(CR)
S4	0–127 ASCII	Character recognized as line feed	10(LF)
S5	0–32, 127 ASCII	Character recognized as back space	8(BS)
S6	2–255 sec.	Wait time for dial tone	2
S7	1–255 sec.	Wait time for carrier	30
S8	0–255 sec.	Pause time (caused by comma)	2
S9	1–255 1/10 sec.	Carrier detect response time	6
S10	1–255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50–255 millisec.	Duration and spacing of Touch-Tones	70
S12	20–255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	—
S14	bit mapped	Option register	—
S15	bit mapped	Flag register	—
S16	0,1,2,4	Test modes	0

Table 2. SC11028 S Registers (Software Registers) Used by AT Commands

Command	Desc. (Notes 1 and 2)
Prefix, Repeat and Escape Commands	
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; + + + is not followed by carriage return)
Dialing Commands	
D	Dial
P	Pulse*
T	Touch-Tone
,	Pause
!	Flash
/	Wait for 1/8 second
@	Wait for silence
W	Wait for second dial tone
;	Return to command state after dialing
R	Reverse mode (to call originate-only modem)

Command	Desc. (Notes 1 and 2)
Other Commands	
A	Answer call without waiting for ring
B/B0	CCITT V.22 mode (Note 3)
B1	Bell 103 and 212A mode*
C/C0	Transmit carrier off
C1	Carrier on*
E/E0	Characters not echoed
E1	Characters echoed*
F/F0	Half duplex
F1	Full duplex*
H/H0	On hook (hang up)
H1	Off hook, line and auxiliary relay
H2	Off hook, line relay only
I/I0	Request product ID code (130)
I1	Firmware revision number
I2	Test internal memory
L/L1	Low speaker volume
L2	Medium speaker volume*
L3	High speaker volume
M/M0	Speaker always off
M1	Speaker on until carrier detected*
M2	Speaker always on

Command	Desc. (Notes 1 and 2)
Other Commands	
O	Go to on-line state
O1	Remote digital loopback off*
O2	Remote digital loopback request
Q/Q0	Result codes displayed*
Q1	Result codes not displayed
Sr?	Requests current value of register r
Sr=n	Sets register r to value of n
V/V0	Digit result codes
V1	Word result codes*
X/X0	Compatible with Hayes-type 300 modems*
X1	Result code CONNECT 1200 enabled
X2	Enables dial tone detection
X3	Enables busy signal detection
X4	Enables dial tone and busy signal detection
Y/Y0	Long space disconnect disabled*
Y1	Long space disconnect enabled
Z	Software reset: restores all default settings

Notes: 1. Default Modes are indicated by *.
2. Commands entered with null parameters assume 0-X is the same as X0.
3. When used with the SC11016 modem IC, which has CCITT V.21 as well as V.22 modes, when the ATB command is used, in the answer mode, the SC11028 will put the SC11016 in either the V.21 mode or the V.22 mode, depending on the response from the remote modem. In the originate mode, the SC11028 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the SC11016 accordingly.

Table 3. Command Summary

Digit Code	Word Code	Description
0	OK	Command Executed
1	CONNECT	Connected at 300 or 1200 bps. Connected at 300 bps., if result of X1, X2, X3 or X4 command
2	RING	Ringing signal detected (Note 1)
3	NO CARRIER	Carrier signal not detected or lost
4	ERROR	Illegal command Error in command line Command line exceeds buffer (40 character, including punctuation) Invalid character format at 1200 bps.
5	CONNECT 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	NO DIALTONE	Dialtone not detected and subsequent commands not processed. Results from X2 or X4 commands only.
7	BUSY	Busy signal detected and subsequent commands not processed. Results from X3 or X4 commands only.
8	NO ANSWER	Silence not detected and subsequent commands not processed. Results from @ command only.

Note 1. When the SC11028 detects a ringing on the telephone line, it sends a RING result code. However, the SC11028 will answer the call only if it is in auto-answer mode or is given an A command.

Table 3. Result Codes

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	+ 6 V
Input Voltage	-0.6V to V_{CC}+0.6
Storage temperature range	–65 to +150°C.
Maximum power dissipation @ 25°C.	500mW
Lead temperature (soldering, 10 sec)	300°C.
Operating temperature range	0 to 70°C.

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

DC ELECTRICAL CHARACTERISTICS

Param.	Description	Conditions	Min	Typ	Max	Units
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Operating Current	@ V_{CC} = 5 V, outputs unloaded		10.0		mA
V_{ih}	High Level Input Voltage	all pins except $\overline{RI}$	2.0			V
V_{il}	Low Level Input Voltage	all pins except $\overline{RI}$			0.8	V
V_t+	Positive hysterisis threshold	$\overline{RI}$ pin		2.5		V
V_t–	Negative hysterisis threshold	$\overline{RI}$ pin		1.8		V
V_{oh}	High Level Output Voltage	@ I_{oh} = 2 mA	V_{CC} –1.0			V
V_{ol}	Low Level Output Voltage	@ I_{oh} = 2 mA			0.4	V
I_l	Leakage Current (Note 2)			±1.0		µA
f_{clk}	Clock frequency		7.3721	7.3728	7.3725	MHz

Note 2. This applies to all pins except TEST, which has an internal pull-down, and $\overline{WR}$, $\overline{RD}$, SCK, DI/O and switch pins 15–21 which have internal pullups.

APPLICATIONS

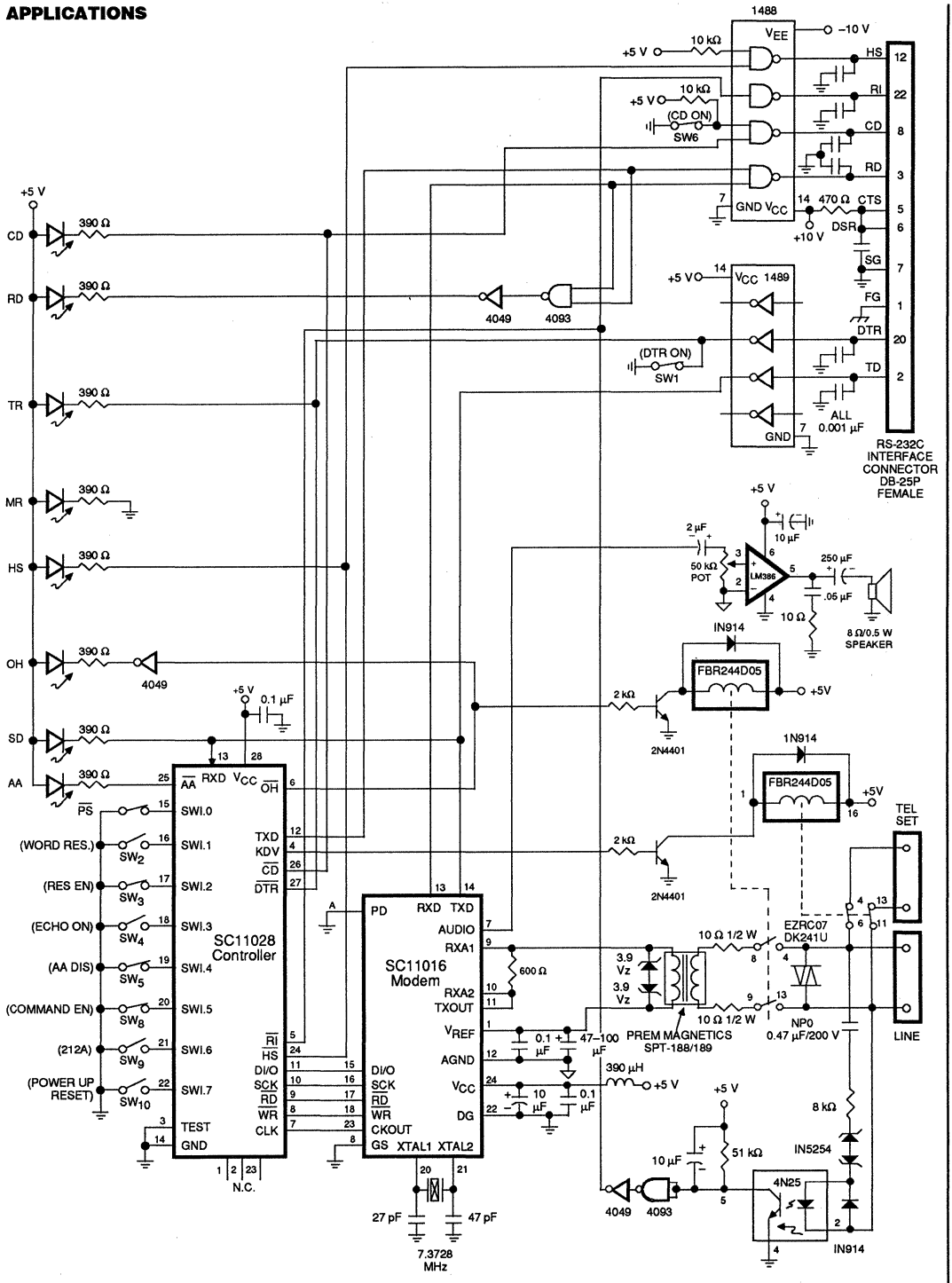
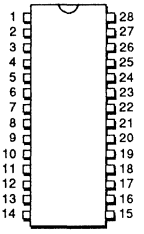


Figure 1. 212A/V.22 Stand-Alone Intelligent Modem Using the SC11016 Modem IC and the SC11028 Controller

FEATURES

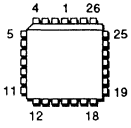
- ☐ Meets requirements of CCITT V.26, V.27, V.27bis/ter, V.29 and V.33
- ☐ Integrated call progress monitor and hybrid
- ☐ On-chip "Eye Dac"
- ☐ All transmit and receive filters on-chip including anti-aliasing and smoothing filters
- ☐ Serial I/O to DSP
- ☐ 16-step 1 dB/step transmit level adjust
- ☐ 128-step, 0.375 dB/step receiver programmable gain control
- ☐ Two code-controlled timing generators
- ☐ Analog and Digital loopback test diagnostics
- ☐ Available in DIP or PLCC package

28-PIN DIP PACKAGE



SC11033CN

28-PIN PLCC PACKAGE

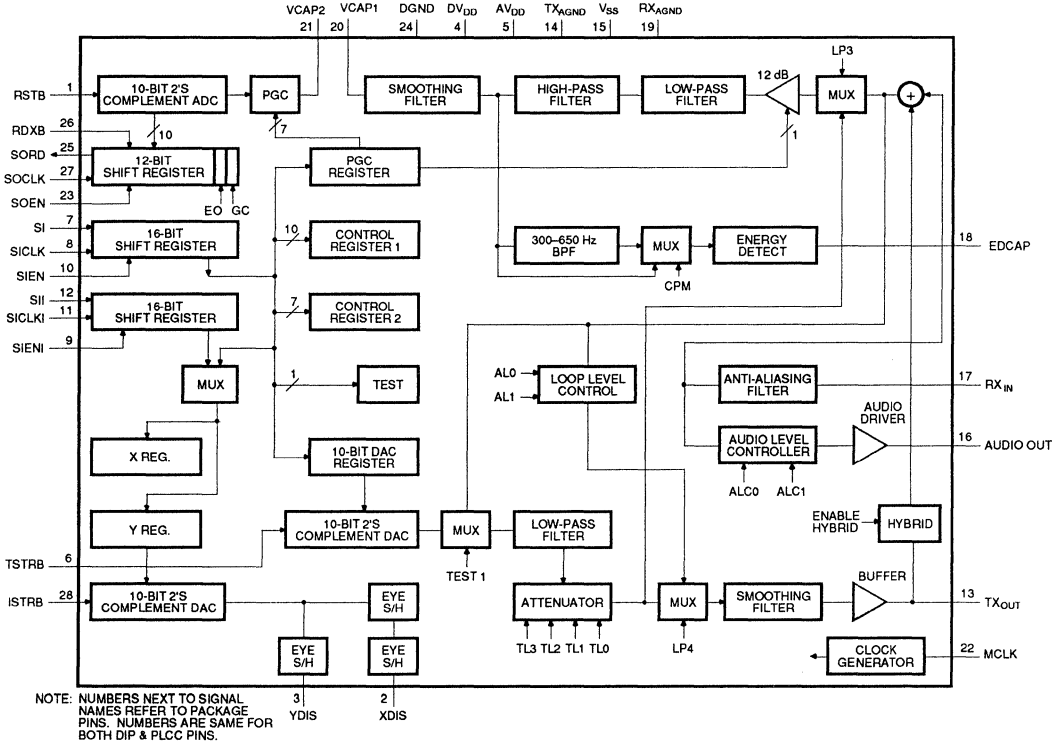


SC11033CV

GENERAL DESCRIPTION

This Analog Front End (AFE) circuit can be used with a digital signal processing element to implement high speed modems operating in 4-wire full duplex or 2-wire half duplex modes. It meets the requirements of the CCITT V.26, V.27, V.27bis/ter, V.29 and V.33 recommendations.

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	RSTRB	Receive strove whose rising edge triggers the A/D conversion. The outputs of A/D are latched into the serial output shift register on following rising edge. RSTRB is 9.6 kHz.
2	XDIS	10 bits D/A output from Eye-X register.
3	YDIS	10 bits D/A output from Eye-Y register. Both X and Y data words are transferred in one ISTRB cycle (see Figure 7 for timing details) and they are ready to display simultaneously at XDIS and YDIS two cycles later.
4	DV_{DD}	Digital positive power supply pin. DV_{DD}= +5 V ±5 %
5	AV_{DD}	Analog positive power supply pin. AV_{DD}= +5 V ±5 %
6	TSTRB	Transmit strobe whose rising edge triggers the 10 bits D/A conversion. Transmit data word (or 2 transmit data words if they are used to load Eye-X and Eye-Y registers) is transferred in one TSTRB cycle (see Figure 5 for timing details) and D/A output is available two cycles later. TSTRB is 9.6 kHz.
7	SI	Serial digital input. It is shifted serially into a 16-bit register. The three most significant bits (D15–D13) destinate the contents of 10 least significant bits (D9–D0) into data/control register . (See Figure 5 for timing details.)
8	SICLK	Serial input clock (2.0 MHz max.). It is used to shift data into a 16-bit register. (See Figure 5 for timing details.)
9	SIENI	Eye-port serial input enable. It enables the writing of data into a 16-bit Eye-register. (See Figure 5 for timing details.)
10	SIEN	Serial input enable. It enables the writing of data into a 16-bit register.. (See Figure 5 for timing details.)
11	SICLKI	Eye-Port serial input clock. It is used to shift data into a 16-bit Eye-register. (See Figure 5 for timing details.)
12	SII	Eye-Port serial digital input. It is shifted serially into a 16-bit register. Bit 12 (E11) and bit 11 (E10) destinate the contents of 10 least significant bits (E9–E0) into either Eye-X register or Eye-Y register.
13	TX_{OUT}	Analog transmit signal.
14	TX_{AGND}	Analog ground for transmit section TX_{AGND} = 0 V
15	V_{SS}	Negative power supply pin V_{SS} = –5 V ±5 %
16	$AUDIO_{OUT}$	Audio monitor. The analog receive signal is passed through a level controller and a buffer to drive a speaker for line audio monitoring.
17	RX_{IN}	Analog receive signal.
18	EDCAP	Energy detect capacitor. The output is a DC level which indicates the amount of energy received within the pass band (300 Hz–3.4 kHz or 300 Hz– 650 Hz in CPM mode). The output needs one external capacitor which together with the internal 25 kΩ resistor forms a low-pass filter with $f_{-3dB} = \frac{1}{2\pi(25{,}000)\ C_{ex}}$
19	RX_{AGND}	Analog ground for receive section RX_{AGND}= 0 V
20, 21	VCAP1, VCAP2	An external capacitor is required between these two pins. These capacitor together with the internal 25 kΩ resistor provides AC coupled between the output of receive filter (VCAP1) and input of PGC (VCAP2). The –3 dB frequency for the high pass filter is given by $f_{-3dB} = \frac{1}{2\pi(25{,}000)\ C_{ext}}$

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
22	MCLK	Master clock. Must be 2.4576 MHz. This is the main clock which is used to derive various clocks for filters, A/D and D/A.
23	SOEN	Serial output enable. It enables the data stored at output shift register to be shifted out. (See Figure 6 for timing details.)
24	DGND	Digital ground DGND = 0 V
25	SO_{RD}	Serial output data. The first 10 bits corresponds to the ADC receive data. Bit 11 (ED) is energy detect output and bit 12 (GC) is gain change acknowledge flag. (See Figure 6 for timing details.)
26	RD_{XB}	Open drain output which goes low during serial out. (See Figure 6 for timing details.)
27	SOCLK	Serial output clock. It is used to shift data out of output shift register. (See Figure 6 for timing details.)
28	ISTRB	Eye strobe whose rising edge triggers the 10 bits D/A conversion. Both X and Y data words are transferred in one ISTRB cycle and they are ready to display simultaneously at XDIS and YDIS pins two cycles later. (See Figure 7 for timing details.)

FUNCTIONAL DESCRIPTION (Refer to Block Diagram)

Transmit Section

The transmit signal is generated in 10-bit two's compliment format by an external processor and is shifted serially into a 16-bit control/data register. The contents of this shift register is converted to analog and passed through a switched-capacitor low-pass filter, an attenuator, a smoothing filter and a buffer to drive a 600 Ω load. The transmit filter has a 6th order transfer function. Figure 2a shows the overall amplitude response, Figure 2b shows the details of the transition region and Figure 2c shows the passband detail and the group delay response. As seen in Figure 2c the passband response of the transmit filter has an x/sin(x) shape and it compensates for the loss distortion due to 9.6 kHz sample-and-hold effect. The 16-step, 1 dB/step attenuator can be programmed to adjust the output signal level.

TRANSMIT LOW-PASS FILTER CHARACTERISTICS

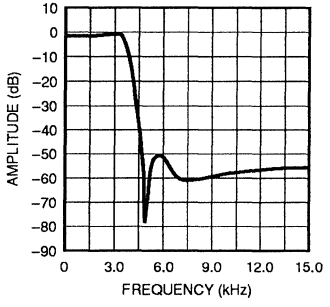


Figure 2a. Overall Response

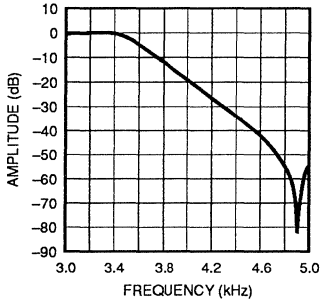


Figure 2b. Passband Detail

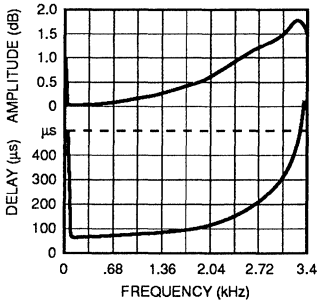


Figure 2c. Passband Amplitude and Group Delay Detail

Receive Section

On the receive side, the signal received from the line is passed through an antialiasing filter and a receive filter section. The receive filter section has 6th order low-pass, and 3rd order high-pass characteristics. The amplitude response of the filter is shown in Figure 3a. Figures 3b and 3c show the details of the upper and lower transition regions and Figure 3d shows the details of the passband amplitude and group-delay response.

The output of the smoothing filter is fed to a Programmable Gain Control stage (PGC) through an external capacitor for dc removal. The PGC can be programmed externally in 128 steps, 0.375 dB/step through a 7-bit control signal. To improve the signal to noise ratio under weak signal conditions a 12 dB front-end gain is enabled.

The output of the PGC is converted to digital 2's complement digital code by a 10-bit A/D converter (ADC). The ADC output can be read together with two other status bits by the external processor.

Test

An Eye DAC is provided to display the real and imaginary parts of any complex signal (i.e. eye patterns, signal constellations, etc.) at a sampling rate up to 14.4 kHz.

The 10-bit I and Q data are sent to the AFE through the 16-bit serial Tx-port under program control or through an independent 16-bit serial Eye-port with its separate enable and clock signals. Typically both data words are transferred in a bit cycle and they are ready to display simultaneously at XDIS and YDIS pins two cycles later. There are multiple sources of strobe for this DAC allowing it to be synchronized to Tx, Rx or be independently synchronized. The control word selects the DAC strobe from TxSTRB, RxSTRB and EyeSTRB.

If only one data word is sent per cycle the output will be available at XDIS pin and YDIS and will remain unchanged.

Call Progress Tone Monitor

The receive analog signal is passed through a bandpass filter with band edges at 300 and 650 Hz. The amplitude response of the call progress filter is shown in Figure 4. An energy detect circuit follows this filter. The energy detect needs one external capacitor. The detect level is selectable between two distinct levels. In the mode of operation where call progress is not selected (CPM = 0), the band-pass filter is removed from the signal path, and the energy detect monitors the signals that fall within the frequency band of the receive filter.

RECEIVE LOW-PASS AND HIGH-PASS FILTER CHARACTERISTICS

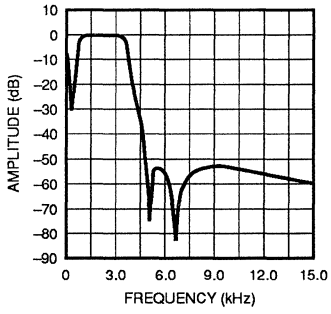


Figure 3a.

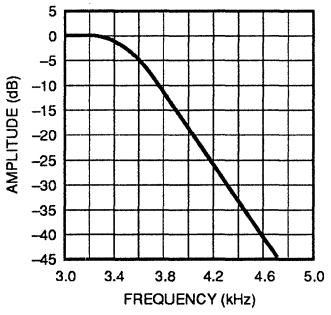


Figure 3b.

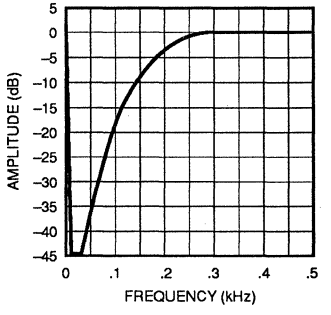


Figure 3c.

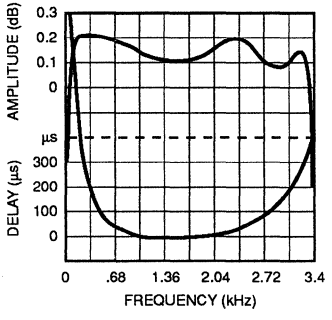


Figure 3d.

Audio Monitor

The analog receive signal is passed through a level controller and a buffer to drive a speaker for line audio monitoring.

This circuit is used during call progress detection to monitor call progress tones. The audio signal level can be controlled by ALC1 and ALC0 bits.

Serial I/O

The serial I/O is designed to be compatible with DSP chips such as TMS 320-series and matches standard codec interfaces.

Serial Input

Sixteen bits of control/data are shifted into the AFE using 16 periods of SICLK. The data on SI pin must be valid on the falling edge of the SICLK. The timing is shown in Figure 5a. A typical serial input example that illustrates the required relationship between SIEN and TSTRR is shown in Figure 5b.

After SIEN goes from Low to High, the data on SI pin is shifted into a 16-bit register on the falling edge of the SICLK.

MSB should be sent first. After the 16th bit (LSB) is received, no further bits are shifted in until SIEN has another Low to High transition.

The most significant 3 bits (D15–D13) are used for addressing as follows:

D15–D13	SOURCE AND DESTINATION
0	10 LSB's (D9–D0) Loaded into TX register
1	10 LSB's (D9–D0) Loaded into EYE-X register
2	10 LSB's (D9–D0) Loaded into EYE-Y register
3	10 LSB's (D9–D0) Loaded into CTRL-1 register
4	6 LSB's (D5–D0) Loaded into CTRL-2 register
5	8 LSB's (D7–D0) Loaded into PGC register
6	1 LSB (D0) Loaded into TEST register

CALL PROGRESS FILTER CHARACTERISTICS

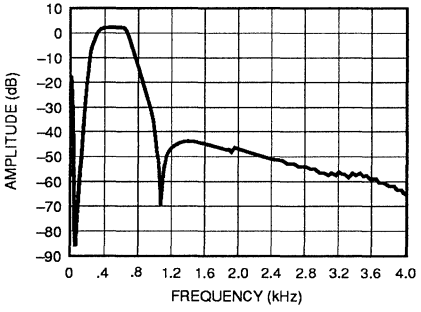


Figure 4a.

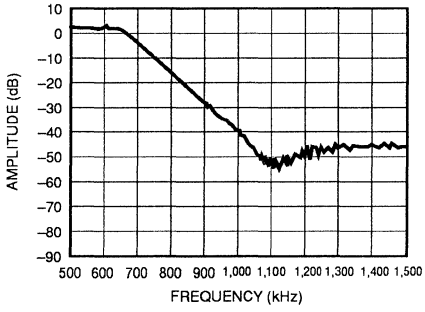


Figure 4b.

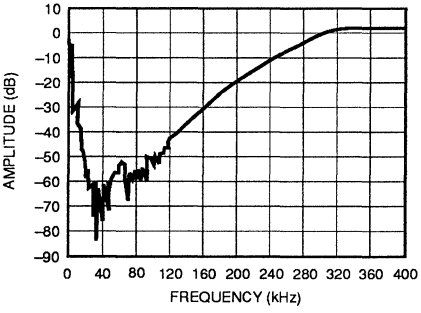


Figure 4c.

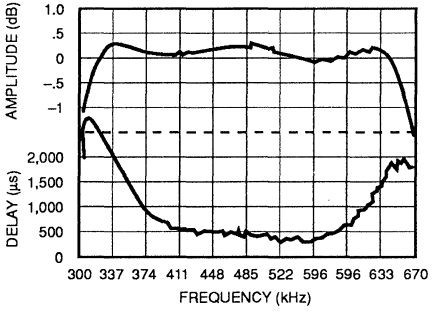


Figure 4d.

Serial Output

Twelve bits of data are shifted out of the AFE serial output (SO) pin using 12 periods of SOCLK. Transmission begins with an SOEN pulse as shown in Figure 6a. The data bits are valid on the falling edge of the SOCLK. The first output bit will be the MSB.

The first 10 bits of the data correspond to the ADC receive data. Bit 11 (ED) is energy detect output and bit 12 (GC) is gain change acknowledge flag. The gain change latch is reset whenever a new value of gain is loaded into the PGC register, and it becomes set when the gain change is taken into effect. A typical example of a serial output and the relationship between RSTRB and SOEN is shown in Figure 6b.

Eye Serial Port

A separate serial port is connected to the Eye pattern generator for sending 10-bit samples to the EYE DAC. The interface is identical to the transmit serial port. Sixteen bits are shifted in for each SIENI transition from low to high. The 10 MSB's of this shift register are transferred to the X and Y registers as selected by the bits E11 and E10 according to the table below.

The X and Y registers can also be loaded by the SI interface. In this case the contents of the Eye serial port will be ignored. The Eye-port serial timing and the relationship between ISTRB and SIENI is shown in Figure 7.

E11	E10	SOURCE AND DESTINATION
0	1	10 LSB's (D9–D0) Load into X register
1	0	10 LSB's (D9–D0) Load into Y register

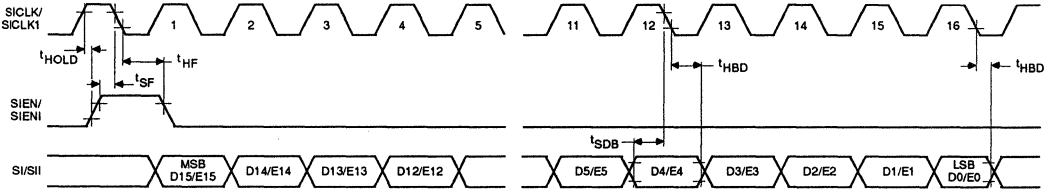


Figure 5a. Serial Input Timing

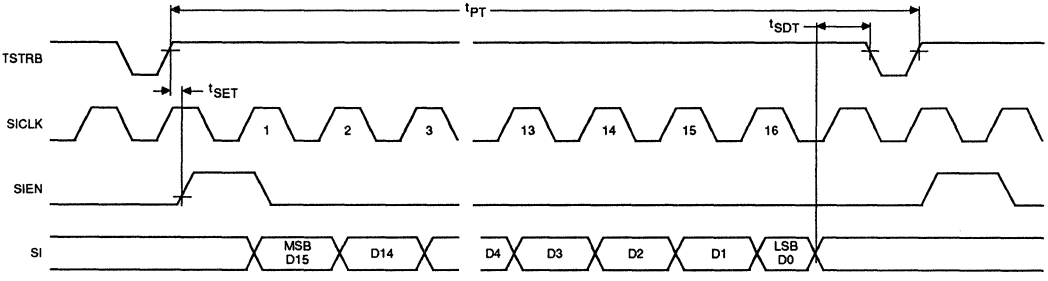


Figure 5b. Serial Input Timing with Respect to TSTRB

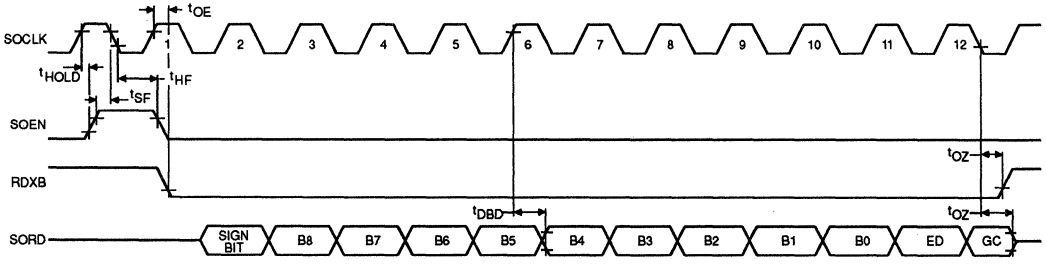


Figure 6a. Serial Output Timing

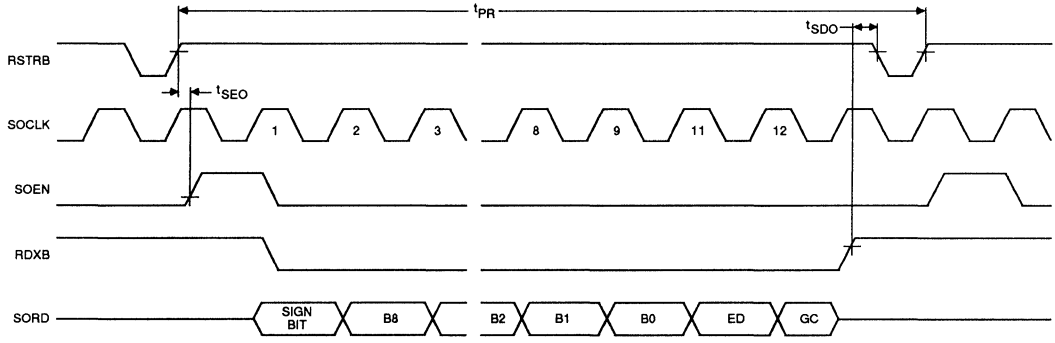


Figure 6b. Serial Output Timing with Respect to RSTRB

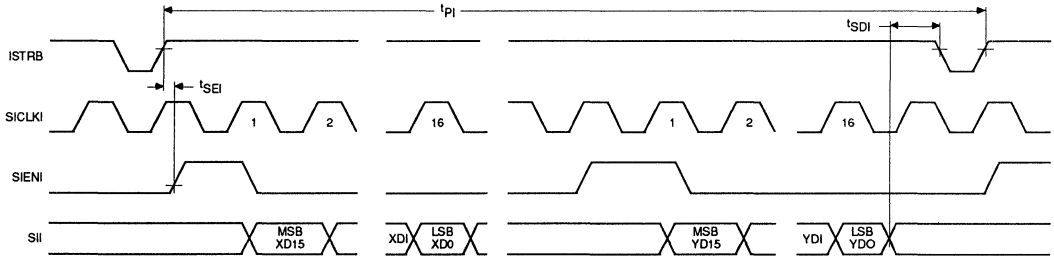


Figure 7. Eye-Port Serial Input Timing with Respect to ISTRB

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HOLD}	Holding time from Serial Clock high to Enable High	0			ns
t_{SF}	Set up time from Enable high to Serial Clock low	50			ns
t_{HF}	Hold time from Serial Clock low to Enable low	100			ns
t_{DBD}	Delay time from SOCLK high to data valid	0		180	ns
t_{OE}	Delay time to RDXB low			140	ns
t_{OZ}	Delay time from SOCLK low to data output disabled	50		165	ns
t_{SDB}	Set up time from SI/SII valid to SICLK/SICLKI low	50			ns
t_{HBD}	Hold time from SICLK/SICLKI low to SI/SII invalid	50			ns
t_{SEO}	Set up time from RSTRB high to SOEN high	0			ns
t_{SDO}	Hold time from RDXB high to RSTRB low	0			ns
t_{SET}	Set up time from TSTRB high to SIEN high	0			ns
t_{SDT}	Hold time from last input data to TSTRB low	0			ns
t_{SEI}	Set up time from ISTRB high to SIENI high	0			ns
t_{SDI}	Hold time from last input to ISTRB low	0			ns
$1/t_{PR}$	Frequency of receive strobe		9–6		kHz
$1/t_{PT}$	Frequency of transmit strobe		9–6		kHz
$1/t_{PI}$	Frequency of eye strobe		9–6		kHz

CONTROL REGISTERS

Control Register 1

Bit #	Function	
0 (LSB)	ALC0	Audio level control
1	ALC1	
2	AL0	Loop 4 gain control
3	AL1	
4	LP4	When set Loop 4 active
5	LP3	When set Loop 3 active
6	TL0	Transmit level control
7	TL1	
8	TL2	
9	TL3	

Code Definition

ALC1	ALC0	Audio Out
0	0	Off
0	1	12 dB loss
1	0	6 dB loss
1	1	0 dB

AL1	AL0	Loop Gain
1	1	–6 dB
0	0	0
0	1	+6 dB
1	0	+15 dB

LP3	LP4	Loop
0	0	Normal
1	0	Loop 3
0	1	Loop 4
1	1	Normal

TL3	TL2	TL1	TL0	Loss (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Control Register 2

Bit #	Function	
0 (LSB)	HBRD	Hybrid enable
1	EDLVL	Energy detect level control
2	CPM	Call progress mode selected
3	EYEC1	EYE DAC strobe select
4	EYEC2	
5	EYE DIS	Enables/disables EYE/DAC
6	SI/SIEB	Selects source for the X and Y registers of EYE DAC as SI or SIE

Code Definition

HBRD	Hybrid
1	Activated
0	Deactivated

EDLVL	Energy Detect
0	–43 dBm
1	–50 dBm

EYEC1	EYEC2	EYE DAC Strobe
0	0	EYESTRB
0	1	TXSTRB
1	0	RXSTRB
1	1	EYESTRB

EYE DIS	EYE DAC
1	Enabled
0	Disabled

SI/SIEB	EYE DAC Source
1	From SI interface
0	From SIE interface

PGC REGISTER

G6	G5	G4	G3	G2	G1	G0	Gain
0	0	0	0	0	0	0	0 dB
1	0	0	0	0	0	0	24 dB
0	1	0	0	0	0	0	12 dB
0	0	1	0	0	0	0	6 dB
0	0	0	1	0	0	0	3 dB
0	0	0	0	1	0	0	1.5 dB
0	0	0	0	0	1	0	0.75 dB
0	0	0	0	0	0	1	0.375 dB

G7	
1	RX low-pass has 12 dB gain
0	RX low-pass has 0 dB gain (default)

TEST REGISTER

There is one bit used for factory test and should be cleared in normal operation.

SPECIFICATIONS

Absolute Maximum Ratings (Notes 1, 2 and 3)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS}–0.6 to V_{DD}+0.6 V
DC Input Voltage (Digital Signals)	V_{SS}–0.6 to V_{DD}+0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 s)	300°C

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating — Plastic Package: –12 mW/C from 65°C to 85°C.

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
MCLK	Clock Frequency	CLKSEL = 0	2.4573	2.4576	2.4579	MHz
T_R, T_F	Input Rise or Fall Time	All Digital Inputs Except CLKIN			50	ns
T_R, T_F	Input Rise or Fall Time	CLKIN			50	ns

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = +5 V ±10%, V_{SS} = –5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current			18	35	mA
I_{SS}	Quiescent Current			18	35	mA
V_{IH}	High Level Input Voltage; Digital Pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital Pins				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Output (I_{OL} = 1.6 mA)				0.6	V
VXTA	Maximum Peak Output Level on TXA pin	V_{CC} = +5 V V_{SS}	±3			V

AC Electrical Characteristics

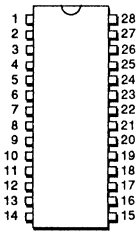
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	PSRR (V_{DD}) @ 1 kHz PSRR (V_{SS}) @ 1 kHz	Transmit Path		–30 –35		dB dB
	PSRR (V_{DD}) @ 1 kHz PSRR (V_{SS}) @ 1 kHz	Receive Path		–40 –30		dB dB
	Idle Channel Noise	Both Transmit and Receive Filters		10		dBrnCo
	Total Harmonic Distortion for Receive Filter	Rx_{IN} = 3 V_{PP} @ f = 1000 Hz		–70		dB
	Total Harmonic Distortion for Transmit Filter	Tx_{OUT} = 3 V_{PP} @ f = 1000 Hz		–65		dB
	Channel-to Channel Separation (Crosstalk)			–70		dB

Notes: 4. Does not apply to CKOUT.
5. Min and max values are valid over the full temperature and operating voltage range. Typical values are from 25° C and ±5 V operation.

FEATURES

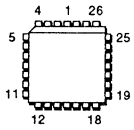
- ☐ Direct interface to SC11016 single chip modem
- ☐ Complete "AT" command set in firmware
- ☐ Built-in UART
- ☐ Direct IBM PC XT or AT bus interface
- ☐ 28 Pin DIP or PLCC package
- ☐ Auto power down

28-PIN DIP PACKAGE



SC11037CN

28-PIN PLCC PACKAGE

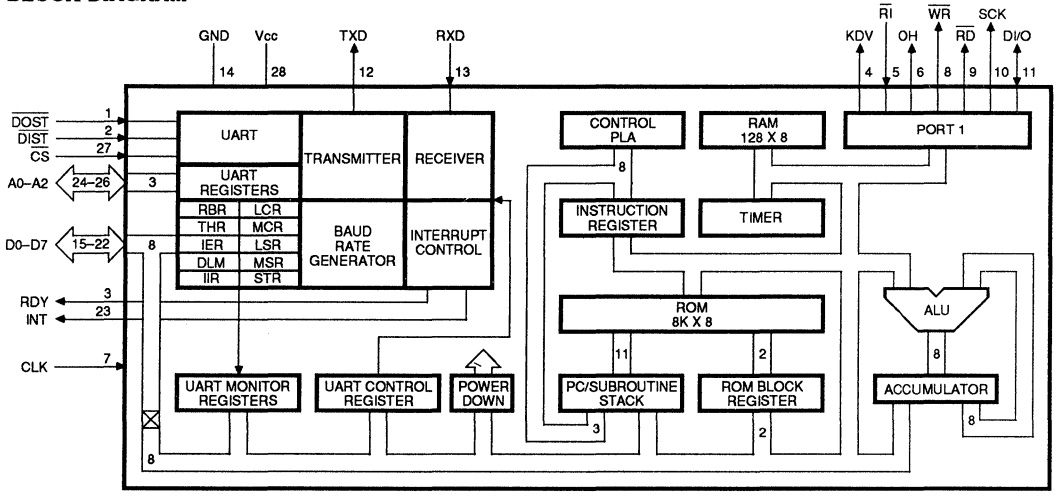


SC11037CV

GENERAL DESCRIPTION

The SC11037 Modem Interface Controller is specifically designed to control Sierra's 5-Volt only SC11016 single chip, 300/1200 bit per second modem. Built with Sierra's proprietary CMOS process, the SC11037 provides a highly cost effective solution for interfacing a modem IC to a system bus. When connected to the SC11016, with the addition of a data access arrangement (DAA), the SC11037 implements a Hayes-type smart modem for board level, integral modem applications. Because the SC11037 fully emulates the functionality of the 8250B UART with increased speed, and includes data bus transceivers, it can be directly interfaced to a computer's parallel data bus and in particular to the bus of the IBM PC, XT or AT. The SC11037 incorporates IO channel ready control circuitry and provides a RDY signal to inject wait states into the PC thus allowing the SC11037 to work inside any high speed PC compatible computer. All of the popular communications software written for the PC will work with the SC11016/SC11037 chip set. The SC11037 contains an 8-bit microprocessor, 8k byte of ROM and 128 bytes of RAM. For specific high volume applications, the control program can be modified by Sierra to include additional commands and functions.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE SAME FOR BOTH DIP & PLCC.

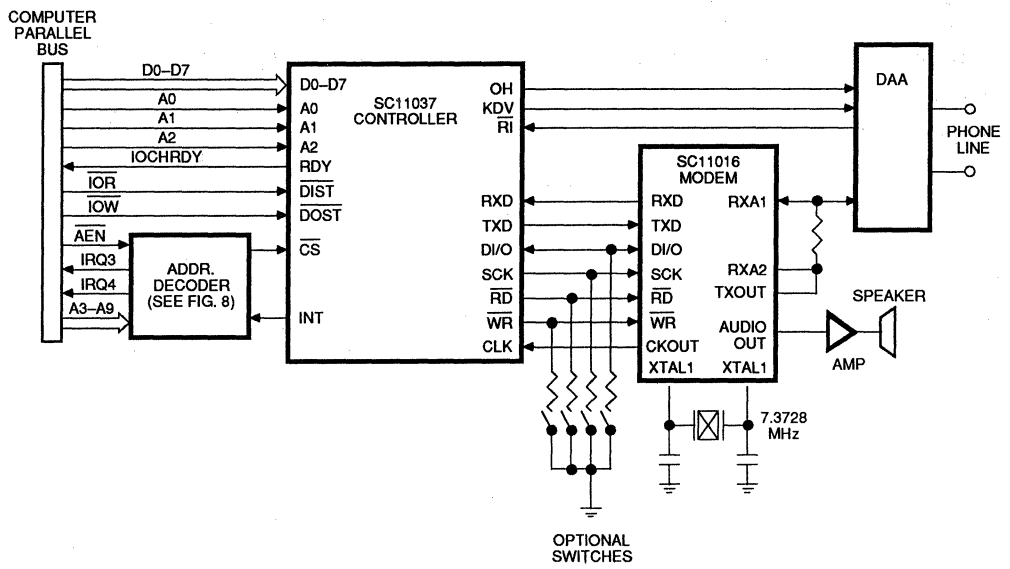


Figure 2. Integral Smart Modem Configuration for PC Bus Applications

PIN/FUNCTION DESCRIPTIONS

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	$\overline{DOST}$	I	The CPU can write data or control words into a selected register of the SC11037 when $\overline{DOST}$ is low and the chip is selected. Data is latched on the rising edge of the signal.
2	$\overline{DIST}$	I	The CPU can read data or status information from a selected register of the SC11037 when $\overline{DIST}$ is low and the chip is selected.
3	RDY	I	This open drain output goes low to inject a wait state into computer. Following a self-timed delay (approximately 500 ns), the wait state is released.
4	KDV	O	This output controls the operation of the data/voice relay. When low, the data/voice relay is off and the phone line is connected to the phone set. During a data call, the SC11037 makes this output high to operate the data/voice relay, disconnecting the phone set from the phone line. It may also be used to drive a relay for multi-line phone applications to close the A and A1 leads.
5	$\overline{RI}$	I	The output of the ring detector in the DAA is connected to this input. A low level on this input indicates the On duration of the ring cycle. This is a Schmidt Trigger input, allowing for slow rising and falling signals on this pin.
6	OH	0	This output controls the operation of the hookswitch relay in the DAA. During a data call, this output is high. It operates the hookswitch relay which causes the phone line to be seized. During rotary dialing, the SC11037 pulses this output at a rate of 10 pulses per second with appropriate mark/space ratio depending on 212A or V.22 mode.
7	CLK	I	A 7.3728 MHz clock signal must be connected to this input. Normally, the CKOUT pin of the SC11016 modem is connected to this pin. All internal timing is derived from this clock.
8	$\overline{WR}$	I/O	This pin is used to initiate writing of data to the SC11016 modem. On power-up, it is an input for a brief time in which the SC11037 reads the carrier status switch connected to this pin. If the switch is closed to ground thru an 18 kΩ resistor, the SC11037 sets the Received Line Signal Detect (RLSD) bit in the Modem Status Register. If the switch is open or tied to V_{CC} thru 18k, the SC11037 resets this bit and writes the actual status of the carrier detector during a data call. However, NO switch is required, since an internal pullup sets the status during power-up to the default state (pullup to V_{CC}) which is to follow the remote modem's carrier.

PIN NO.	PIN NAME	I/O	DESCRIPTION
9	$\overline{RD}$	I/O	This pin is used to initiate reading of data from the SC11016 modem. On power-up, this pin is an input for a brief time in which the SC11037 reads the DTR status switch connected to this pin. If this switch is open or tied to V_{CC} thru 18k, the SC11037 reacts to the status of the DTR bit in the UART Modem Control Register. If the switch is closed to ground thru 18 kΩ, the SC11037 ignores the state of the DTR bit. When the switch is open, writing a 0 to the DTR bit in the Modem Control Register forces the SC11037 into the command state and when on line, causes it to hang up. However, NO switch is required, since an internal pullup to V_{CC} sets the status during power-up to the default state—to follow the DTR status.
10	SCK	I/O	The SC11037 supplies a shift clock on this pin to the SC11016 modem for reading or writing data. On power-up, this pin is an input for a brief time in which the SC11037 reads the Bell/CCITT select switch connected to this pin. If this switch is open or tied to V_{CC} thru 18k, Bell protocol is selected. If this switch is closed to ground 18 kΩ, CCITT V.22 protocol is selected. However, NO switch is required, since an internal pullup sets the status during power-up to the default state—212A mode.
11	DI/O	I/O	The SC11037 shifts data serially out of this pin to SC11016 during a write operation and shifts data serially into this pin during a read operation from the SC11016. On power-up this pin is an input for a brief time in which the SC11037 reads the Make/Break ratio select switch connected to this pin for selecting the pulse dialing standard. With the switch open or tied to VCC thru 18k, the Bell standard 39% Make, 61% Break is selected. With the switch closed to ground thru 18 kΩ, the CCITT standard 33% Make, 67% Break is selected. However, NO switch is required, since an internal pullup sets the status during power-up to the default state—Bell standard.
12	TXD	O	During a data call, after the connection is established, the SC11037 converts parallel data received from the computer bus and outputs it in a serial, asynchronous format to the SC11016 modem for modulation. At all other times the SC11037 holds this output in the Mark (high) condition.
13	RXD	I	Demodulated data from the SC11016 modem is received on this pin during a data call. A high level is considered Mark and a low level is a Space. The SC11037 converts the serial data into a parallel data byte and stores it in the Receiver Buffer Register (RBR). The Data Ready bit in the Line Status Register (LSR) is then set, and an appropriate interrupt indentification code is written in the Interrupt Identification Register (IIR) to signal to the computer, the reception of a new data byte.
14	GND	—	Ground reference (0 Volts).
15–22	D0–D7	I/O	This is the 8 bit data bus comprising of three state input/output lines. This bus provides bidirectional communication between the SC11037 and the CPU. Data, control words and status information are transferred via the D0–D7 data bus. Because on-chip high drive buffers are used, no external transceiver IC, such as the 74LS245, is needed between the computer bus and the SC11037.
23	INT	O	This output goes high whenever any one of the following interrupt types has an active condition and is enabled via the IER: Receiver Line Status Flag, Received Data Available, Transmitter Holding Register Empty and Modem Status. It is reset low upon the appropriate interrupt servicing. The INT pin is forced to a Hi-Z state when the OUT2 bit of the Modem Control Register (MCR) is low (power on state).
24–26	A0–A2	I	These three address inputs are used during read or write operation to select a UART register in the SC11037 as shown in Table 1. The Divisor Latch Access Bit (DLAB) must be set high by the system software to access the bit rate divisor latches as shown in Table 2.
27	$\overline{CS}$	I	The SC11037 is selected when this input is low. When high, the SC11037 forces the Data bus lines into a high impedance state.
28	V_{CC}	—	Positive supply (+5 Volts).

SC11037 SPECIFICATIONS

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read only) (RBR)
0	0	0	0	Transmitter Holding (write only) (THR)
0	0	0	1	Interrupt Enable (IER)
X	0	1	0	Interrupt Identification (read only) (IIR)
X	0	1	1	Line Control (LCR)
X	1	0	0	Modem Control (MCR)
X	1	0	1	Line Status (LSR)
X	1	1	0	Modem Status (read only) (MSR)
X	1	1	1	Speed (STR)
1	0	0	0	Divisor Latch (LSB) (write only) (DLL)
1	0	0	1	Divisor Latch (MSB) (write only) (DLM)

Table 1. SC11037 UART Registers

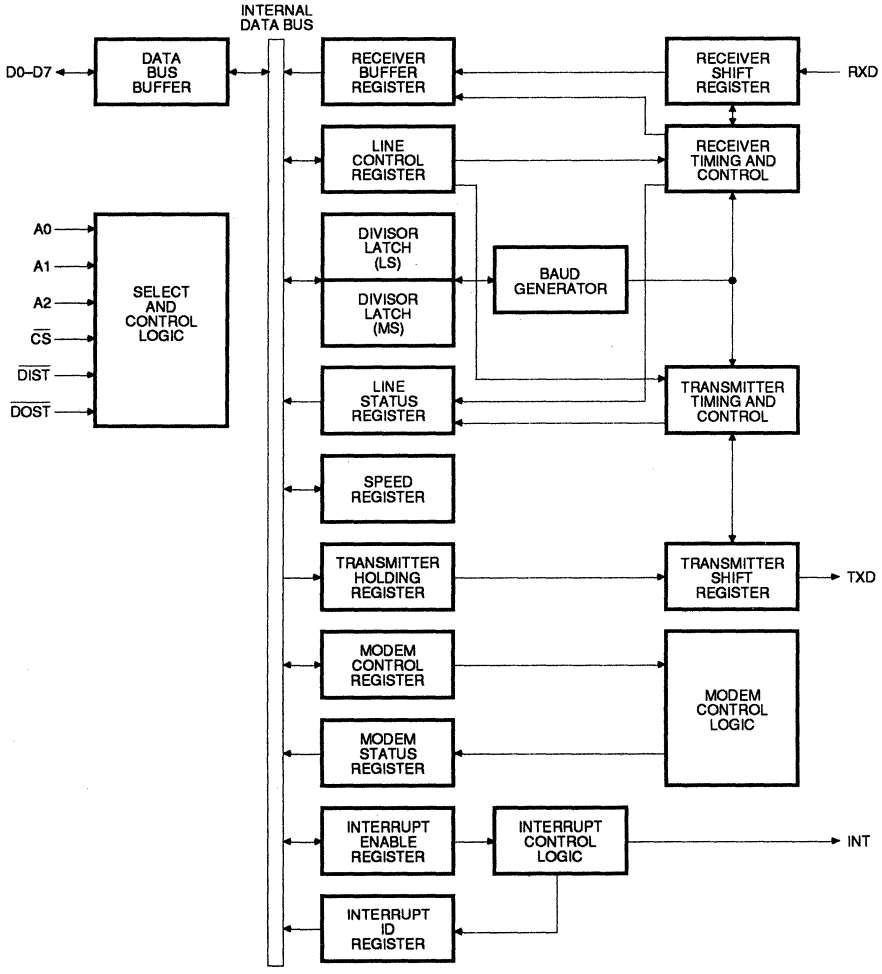


Figure 3. UART Block Diagram

NAME	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
RBR	Data	Data	Data	Data	Data	Data	Data	Data
THR	Data	Data	Data	Data	Data	Data	Data	Data
IER	Receive Data Available Interrupt Enable	THRE Interrupt Enable	Receive Line Status Interrupt Enable	Modem Status Interrupt Enable	0	0	0	0
IIR	0 If Interrupt Pending	Interrupt ID Bit 0	Interrupt ID Bit 1	0	0	0	0	0
LCR	0 = 7 Bit Data 1 = 8 Bit Data	1	0 = 1 Stop Bit 1 = 2 Stop Bits	1 = Parity Enable	1 = Even Parity	1 = Stick Parity	1 = Set Break	DLAB
MCR	Data Terminal Ready	Request to Send	OUT1	OUT2 0 = INT Output to HI-Z	No Function	0	0	0
LSR	Data Ready	Overrun Error	Parity Error	Framing Error	Break Interrupt	THRE	TSRE	0
MSR	0	0	Trailing Edge Ring	Delta RLSD	1 (CTS)	1 (DSR)	Ring	RLSD
DLM	Data	Data	Data	Data	Data	Data	Data	Data
STR	Data	Data	Data	Data	Data	Data	Data	Data

Table 2. SC11037 UART Register Function Summary

REGISTER	RANGE/UNITS	DESCRIPTION	DEFAULT
S0	0–255 rings	Ring to answer telephone on	0
S1	0–255 rings	Number of rings	0
S2	0–127 ASCII	Escape code character	43(+)
S3	0–127 ASCII	Character recognized as carriage return	13(CR)
S4	0–127 ASCII	Character recognized as line feed	10(LF)
S5	0–32, 127 ASCII	Character recognized as back space	8(BS)
S6	2–255 sec.	Wait time for dial tone	2
S7	1–255 sec.	Wait time for carrier	30
S8	0–255 sec.	Pause time (caused by comma)	2
S9	1–255 1/10 sec.	Carrier detect response time	6
S10	1–255 1/10 sec.	Delay between loss of carrier and hang up	7
S11	50–255 millisec.	Duration and spacing of Touch-Tones	70
S12	20–255 1/50 sec.	Escape code guard time	50
S13	bit mapped	UART status register	—
S14	bit mapped	Option register	—
S15	bit mapped	Flag register	—
S16	0,1,2,4	Test modes	0

Table 3. SC11037 S Registers (Software Registers) Used by AT Commands

COM-MAND	DESCRIPTION (Notes 1 and 2)
Prefix, Repeat and Escape Commands	
AT	Attention prefix: precedes all command lines except + + + (escape) and A/(repeat) commands
A/	Repeat last command line (A/ is not followed by carriage return)
+ + +	Escape code: go from on-line state to command state (one second pause before and after escape code entry; + + + is not followed by carriage return)
Dialing Commands	
D	Dial
P	Pulse*
T	Touch-Tone
,	Pause
!	Flash
/	Wait for 1/8 second
@	Wait for silence
W	Wait for second dial tone
;	Return to command state after dialing
R	Reverse mode (to call originate-only modem)

COM-MAND	DESCRIPTION (Notes 1 and 2)
Other Commands	
A	Answer call without waiting for ring
B/B0	CCITT V.22 mode (Note 3)
B1	Bell 103 and 212A mode*
C/C0	Transmit carrier off
C1	Carrier on*
E/E0	Characters not echoed
E1	Characters echoed*
F/F0	Half duplex
F1	Full duplex*
H/H0	On hook (hang up)
H1	Off hook, line and auxiliary relay
H2	Off hook, line relay only
I/I0	Request product ID code (130)
I1	Firmware revision number
I2	Test internal memory
L/L1	Low speaker volume
L2	Medium speaker volume*
L3	High speaker volume
M/M0	Speaker always off
M1	Speaker on until carrier detected*
M2	Speaker always on

COM-MAND	DESCRIPTION (Notes 1 and 2)
Other Commands	
O	Go to on-line state
O1	Remote digital loopback off*
O2	Remote digital loopback request
Q/Q0	Result codes displayed*
Q1	Result codes not displayed
Sr?	Requests current value of register r
Sr=n	Sets register r to value of n
V/V0	Digit result codes
V1	Word result codes*
X/X0	Compatible with Hayes-type 300 modems*
X1	Result code CONNECT 1200 enabled
X2	Enables dial tone detection
X3	Enables busy signal detection
X4	Enables dial tone and busy signal detection
Y/Y0	Long space disconnect disabled*
Y1	Long space disconnect enabled
Z	Software reset: restores all default settings

Notes: 1. Default Modes are indicated by *.
2. Commands entered with null parameters assume 0-X is the same as X0.
3. When used with the SC11016 modem IC, which has CCITT V.21 as well as V.22 modes, when the ATB command is used, in the answer mode, the SC11037 will put the SC11016 in either the V.21 mode or the V.22 mode, depending on the response from the remote modem. In the originate mode, the SC11037 will sense if the baud rate is set at 300 or 1200 bits per second and will adjust the SC11016 accordingly.

Table 4. Command Summary

DIGIT CODE	WORD CODE	DESCRIPTION
0	OK	Command Executed
1	CONNECT	Connected at 300 or 1200 bps. Connected at 300 bps., if result of X1, X2, X3 or X4 command
2	RING	Ringing signal detected (Note 1)
3	NO CARRIER	Carrier signal not detected or lost
4	ERROR	Illegal command Error in command line Command line exceeds buffer (40 character, including punctuation) Invalid character format at 1200 bps.
5	CONNECT 1200	Connected at 1200 bps. Results from X1, X2, X3, or X4 commands only
6	NO DIALTONE	Dialtone not detected and subsequent commands not processed. Results from X2 or X4 commands only.
7	BUSY	Busy signal detected and subsequent commands not processed. Results from X3 or X4 commands only.
8	NO ANSWER	Silence not detected and subsequent commands not processed. Results from @ command only.

Note 1. When the SC11037 detects a ringing on the telephone line, it sends a RING result code. However, the SC11037 will answer the call only if it is in auto-answer mode or is given an A command.

Table 5. Result Codes

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	+ 6 V
Input Voltage	-0.6V to V_{CC}+0.6
Storage temperature range	–65 to +150°C.
Maximum power dissipation @ 25°C.	500mW
Lead temperature (soldering, 10 sec)	300°C.
Operating temperature range	0 to 70°C.

DC ELECTRICAL CHARACTERISTICS

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Operating Current	@ V_{CC} = 5V		10.0		mA
V_{ih}	High Level Input Voltage	all pins except $\overline{RI}$	2.0			V
V_{il}	Low Level Input Voltage	all pins except $\overline{RI}$			0.8	V
V_t+	Positive hysterisis threshold	$\overline{RI}$ pin		2.5		V
V_t–	Negative hysterisis threshold	$\overline{RI}$ pin		1.8		V
V_{oh}	High Level Output Voltage	Digital signal pins D0 to D7 & INT @ I_{oh} = 6mA All other output or I/O pins @ I_{oh} = 2mA	V_{CC} —1.0 V_{CC} —1.0			V V
V_{ol}	Low Level Output Voltage	Digital signal pins D0 to D7 & INT @ I_{ol} = 6mA All other output or I/O pins @ I_{ol} = 2mA			0.4 0.4	V V
I_l	Leakage Current (Note 2)			±1.0		uA
f_{clk}	Clock frequency		7.3721	7.3728	7.3725	MHz

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

Note 2. This applies to all pins except $\overline{WR}$, $\overline{RD}$, SCK, and the DI/O pins which have internal pullups.

AC ELECTRICAL CHARACTARISTICS (T_A = 0 to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{DIW}	$\overline{DIST}$ Strobe Width	1TTL Load	570		ns
t_{RC}	Read Cycle Delay	1TTL Load	300		ns
RC	Read Cycle = t_{DIW} + t_{RC} + 20 ns	1TTL Load	890		ns
t_{DDD}	Delay from $\overline{DIST}$ to Data	1TTL Load		570	ns
t_{HZ}	$\overline{DIST}$ to Floating Data Delay	1TTL Load	60		ns
t_{DOW}	$\overline{DOST}$ Strobe Width	1TTL Load	570		ns
t_{WC}	Write Cycle Delay	1TTL Load	300		ns
WC	Write Cycle = t_{DOW} + t_{WC} + 20 ns	1TTL Load	890		ns
t_{DS}	Data Setup Time	1TTL Load	60		ns
t_{DH}	Data Hold Time	1TTL Load	40		ns
t_{DIC}	$\overline{DIST}$ Delay from Select	1TTL Load	0		ns
t_{DOC}	$\overline{DOST}$ Delay from Select	1TTL Load	50		ns
t_{ACR}	Address and Chip Select Hold Time from $\overline{DIST}$	1TTL Load	10		ns
t_{ACW}	Address and Chip Select Hold Time from $\overline{DOST}$	1TTL Load	70		ns
t_{DR}	Delay from $\overline{DOST}$ on $\overline{DIST}$ to RDY Low	1TTL Load		30	ns
t_{RDY}	Ready pulse width	1TTL Load	675	810	ns
Receiver					
t_{RINT}	Delay from $\overline{DIST}$ (Read RBR) to Reset Interrupt	100 pF Load		1	µs
Transmitter					
t_{HR}	Delay from $\overline{DOST}$ (Write THR) to Reset Interrupt	100 pF Load		1	µs
t_{IRS}	Delay from Initial INTR Reset to Transmit Start			1	Baud Cycle
t_{SI}	Delay from Initial Write to Interrupt			1	Baud Cycle
t_{SS}	Delay from Stop to Next Start			1	µs
t_{STI}	Delay from Stop to Interrupt (THRE)			1	Baud Cycle
t_{IR}	Delay from $\overline{DIST}$ (Read IIR) to Reset Interrupt (THRE)	100 pF Load		2.2	µs

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Power On Reset	All Bits Low
Interrupt Identification Register	Power On Reset	Bit 0 High; Bits 1–7 Low
Line Control Register	Writing into the LCR	Data
MODEM Control Register	Power On Reset	All Bits Low
Line Status Register	Power On Reset	Bits 0–4, 7 Low; Bits 5 and 6 High
Modem Status Register	Power On Reset	Bits 0–3, 6–7 Low; Bits 4–5 High
Divisor Latch (high order bits)	Power On Reset	1200 BPS
TXD	Master Reset	High
INT	Power On Reset	Low (High-Z)

Table 6. Reset Control of Registers and Pinout Signals

AC ELECTRICAL CHARACTARISTICS (T_A = 0 to +70°C, V_{CC} = +5V ± 10%)

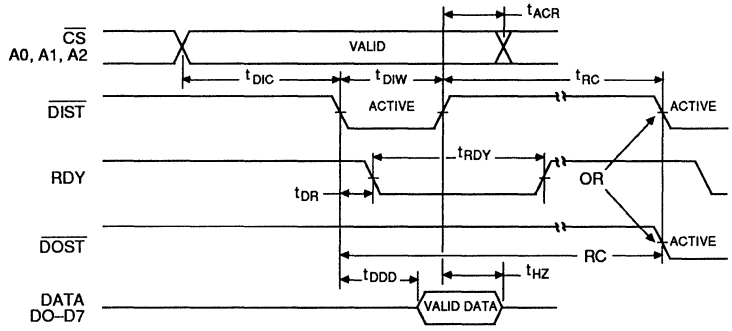


Figure 4. Read Cycle Timing

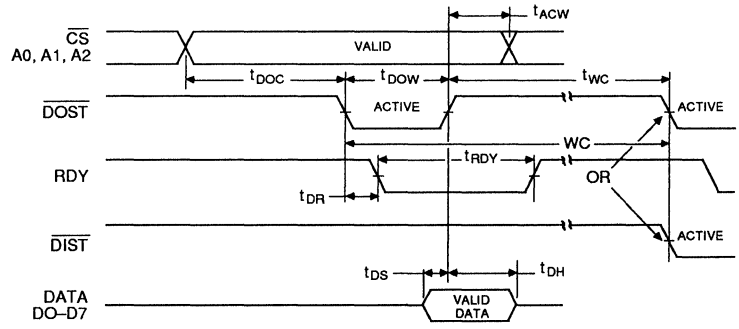


Figure 5. Write Cycle Timing

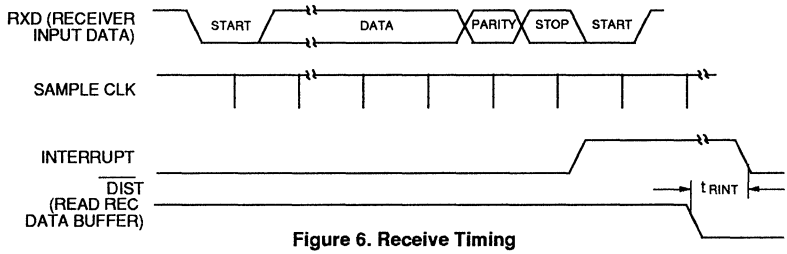


Figure 6. Receive Timing

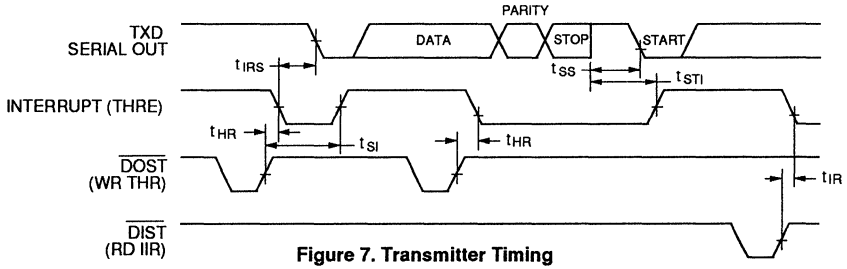


Figure 7. Transmitter Timing

UART REGISTERS

Line Control Register

This register controls the format of the asynchronous data communications.

Bits 0 and 1: Bit 1 is always high. Bit 0 specifies the number of bits in each transmitted or received serial character. The encoding of bit 0 is as follows:

Bit 1	Bit 0	Word Length
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1, when 7-bit word length with no Parity is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 0 is a logic 0 and bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed).

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is logic 1 and bit 5 is logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (TXD) is forced to the Spacing state (logic 0) and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Rate Generator

The SC11037's Baud Rate Generator can be programmed for one of six Baud rates. The desired speed is selected by writing into the Divisor Latch (DLM). On reset, the rate will be 1200 baud.

DLM (HEX Code)	Baud Rate
00	1200
01	300
03	150
04	110
06	75
09	50

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE bit is set to a logic 1 upon detection of parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time—the total time of Start bit + data bits + Parity + Stop bits.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the SC11037 is ready to accept a new character for transmission. In addition, this bit causes the SC11037 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register.

Bit 7: This bit is permanently set to logic 0.

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

UART REGISTERS

Interrupt Identification Register

The SC11037 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors. To provide minimum software overhead during data character transfers, the SC11037 prioritizes interrupts onto four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the source of that interrupt are stored in the Interrupt Identification Register (refer to Table 7). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 7.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the SC11037 to separately activate the Interrupt (INT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Register. The contents of the Interrupt Enable Register are indicated in Table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Interrupt Identification Register			Interrupt Set and Reset Functions			
B2	B1	B0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

MODEM Control Register

This 8-bit register controls the interface with the MODEM. The contents of the MODEM Control Register are indicated in Table 2 and are described below.

Bit 0: This bit controls Data Terminal Ready (DTR) signal. If the external switch on the RD pin is set to V_{CC} thru an 18 kΩ resistor, setting the DTR low will force the SC11037 into the command state and, if on line, it will hang up.

Bit 1: This bit controls the Request to Send (RTS) signal. This signal is not used by the SC11037.

Bit 2: This bit controls the Output 1 (OUT 1) signal. This signal is not used by the SC11037.

Bit 3: This bit controls the Output 2 (OUT 2) signal. When OUT 2 is a 0, the interrupt output is in High-Z state.

Bit 4: Not used.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, two bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 2 and are described below.

Bit 0 and 1: These bits are always 0.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the carrier detector has changed state.

Bit 4: This bit is always 1.

Bit 5: This bit is always 1.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the Received Line Signal Detect (RLSD) signal.

Whenever bit 2 is set to logic 1, or bit 3 changes state, a MODEM Status Interrupt is generated if enabled.

APPLICATIONS

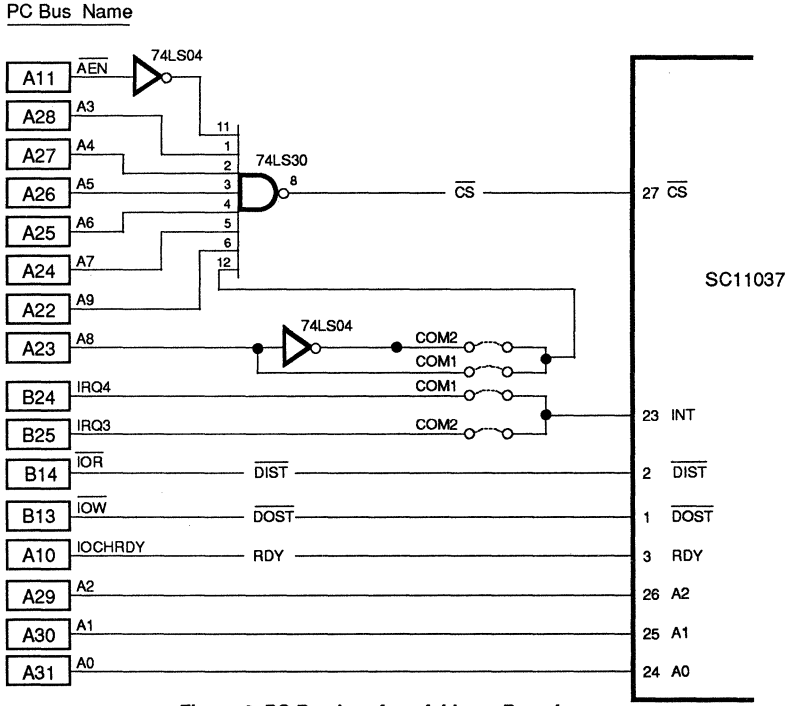
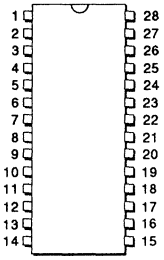


Figure 8. PC Bus Interface Address Decoder

FEATURES

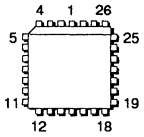
- ☐ Pin compatible with Sierra SC11006 industry standard 2400 bps modem
- ☐ Complete 2400 bps modem conforming to V.22 bis and 4800/2400 bps Sendfax conforming to V.27ter
- ☐ Compatible with CCITT V.27ter, V.22 bis, V.22, V.21, and BELL 212A and 103 standards
- ☐ Analog, digital, and remote digital loopback
- ☐ Contains an on-chip hybrid
- ☐ Integrated DTMF/GUARD TONE GENERATOR, call progress monitor
- ☐ 2100/2225 Hz tone detector
- ☐ Programmable audio output
- ☐ CMOS technology
- ☐ DIP or PLCC packages
- ☐ Synchronous & Asynchronous modes

28-PIN DIP PACKAGE



SC11046CN

28-PIN PLCC PACKAGE



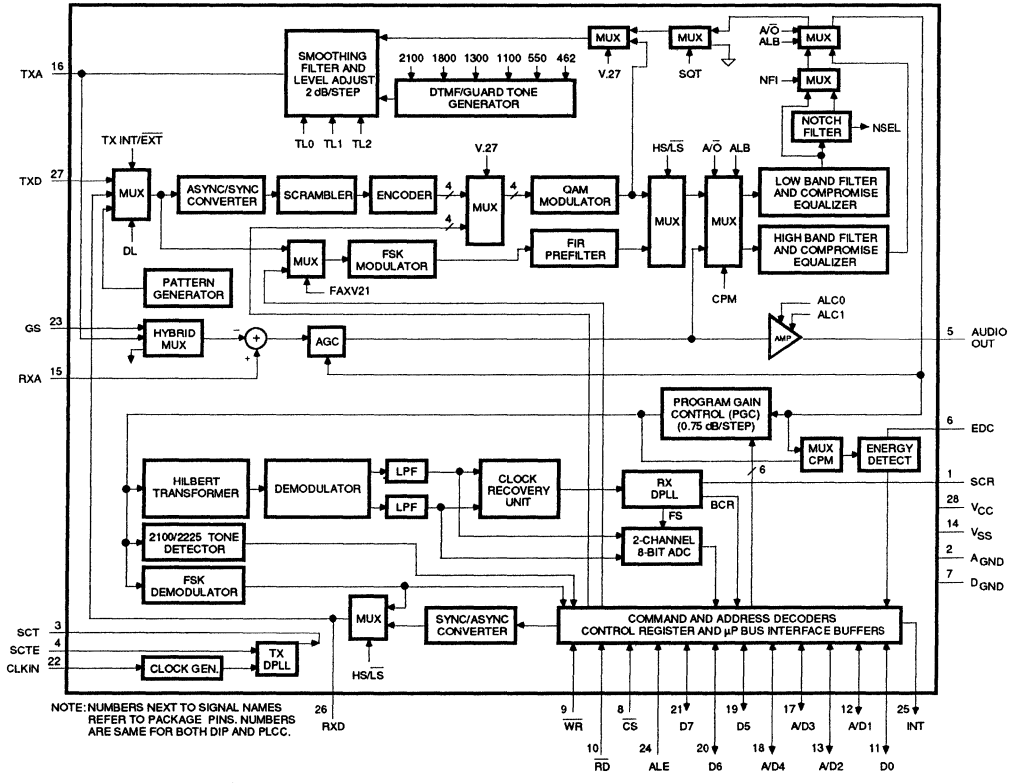
SC11046CV

GENERAL DESCRIPTION

The SC11046 is a complete 2400 bps modem IC including a Sendfax capability at 4800 bps. This IC contains all modem functions except the adaptive equalizer. It is used in conjunction with an external controller, such as the Sierra SC11011 (for either parallel bus or RS-232 applications) and memory to implement a 2400 bps full duplex modem, compatible with the CCITT V.22 bis recommendation, having a Sendfax capability at 4800/2400 bps compatible with the V.27 ter recommendation. The controller performs all modem control and handshaking functions including the Sendfax call set-up in accordance with T.30 recommendation as well as the adaptive equalization.

The SC11046 operates in 2400 bps QPSK/QAM and 1200 bps PSK as well as 0 to 300 baud FSK modes, compatible with Bell 103 and 212A as well as CCITT V.21, V.22, and V.22 bis standards. In addition, the SC11046 operates in 4800 bps APSK with fallback to 2400 bps compatible with V.27ter standards. When used with the SC11011 controller, the SC11046 becomes an intelligent modem controlled by the industry standard "AT" command set with the added Sendfax capability at 4800 bp s. The interface between the SC11046 modem

BLOCK DIAGRAM



GENERAL DESCRIPTION (continued)

and the controller is a standard microcontroller interface that easily connects to the SC22201 (128 by 8) EE memory for permanent storage of configuration settings and phone numbers.

FUNCTIONAL DESCRIPTION OF THE SC11046 MODEM

The SC11046 includes the following (See Block Diagram, Figure 1):

- ☐ Full transmitter consisting of
  - – Async to Sync converter
  - – Scrambler
  - – Data encoder
  - – 75% square root of raised cosine pulse shaper in V.22 mode, 50/90% square root of raised cosine shaping in V.27 4800/2400 BPS modes
  - – Quadrature amplitude and phase modulators
  - – FSK (Bell 103 and CCITT V.21) modulator
  - – Hybrid
- ☐ High band and low band filters
- ☐ High band and low band compromise equalizers
- ☐ V.22 notch filter (selectable at 550 or 1800 Hz)
- ☐ Transmit smoothing filter
- ☐ Programmable attenuator for transmit level adjust
- ☐ DTMF, 550 Hz, 1300 Hz, 1800 Hz, and 2100 Hz tone generator
- ☐ Tone detector for 2100/2225 Hz frequencies
- ☐ Transmit clock circuit for synchronous operation (slave, external, and internal modes)
- ☐ Pattern generator for generating fixed digital patterns in handshaking mode
- ☐ Receive section consisting of
  - – 64-step programmable gain controller (PGC)
  - – Energy detector at the output of the PGC
  - – Hilbert transformer
  - – Quadrature amplitude and phase demodulators (free running carrier) with low pass filters
  - – Baud timing recovery circuit (sampling clock of 600 Hz)
  - – FSK demodulator
  - – Sync to Async converter
- ☐ Two channel 8-bit analog to digital converter (ADC)
- ☐ Control and Status registers
- ☐ 8-bit microprocessor interface with interrupt and multiplexed address/data lines
- ☐ Audio output with level adjust

Transmitter (V.22bis, V.22, 212A and V.21 and 103)

Since data terminals and computers may not have the timing accuracy required for 2400/1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 2400/1200 Hz +2.3%, –2.5%. It outputs serial data at a fixed rate of 2400/1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 2400/1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first four/two stages of the shift register form the quad/dibit that is applied to the QAM/QPSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band, centered at 2400 Hz, or the low band, centered at 1200 Hz. In the 2400 bps mode, the modem actually sends four bits at a time, called a quadbit. The actual rate of transmission for a quadbit is 600 baud. This is the optimum rate of transmission over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

In the 2400 bps data rate, the data to be transmitted is divided into groups of four consecutive bits (quadbits). The first two bits of the quadbit are encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. The last two bits define one of the four signaling elements associated with the new quadrant.

In the 1200 bps data rate, the data stream is divided into groups of two consecutive bits (dibits). The dibits are used to determine the phase quadrant change relative to the quadrant occupied by the preceding signal element. The resulting signaling elements from the inphase (I) and quadrature (Q) channels are passed through baseband filters with a square root of raised cosine shape. The filtered signals subsequently modulate sine and cosine carriers, and add to form the QAM/QPSK signal. The wave-shaped signal is then passed through either the low-band or high-band filter, depending upon originate or answer mode selection.

For low speed operation, the FSK modulator is used. It produces one of four precision frequencies, depending upon originate or answer mode selection and the 1 (mark) or 0 (space) level of the transmit data. Different frequencies are used for V.21 and 212A modes. The frequencies are produced from the master clock oscillator using programmable dividers. The dividers respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence. The output of the FSK modulator is applied to the appropriate filter when the low speed mode of the operation is selected.

The filter section consists of low-band (1200 Hz) and high-band (2400 Hz) filters, half-channel compromise amplitude and group delay equalizers for both bands,

smoothing filters for both bands, and multiplexers for routing of the transmit and receive signals through the appropriate band filters. For CCITT V.22 bis applications, a notch filter is included that can be programmed for either 550 Hz or 1800 Hz. In the call progress monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode, it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second-order low-pass switched-capacitor filter that adds the modem transmit signal to the V.22 guard tones. It also provides a 2 dB per step programmable gain function to set the output level.

Transmitter (V.27 ter)

In this mode, the functions required to convert the transmit data to transmit analog signal are partitioned between the analog and controller chips. The firmware implemented in the controller chip performs the scrambling and also generates the training sequences required by the V.27 ter specification. Next, it carries out the encoding function based on the selected bit rate of 4800/2400 bps and determines the new location of the constellation point. A 4-bit word ($a_3a_2a_1a_0$) has been assigned to each constellation point to facilitate the quadrature modulation by the analog chip. (See Figure 2) Every two baud periods (1600/1200 bauds), the analog chip sends an interrupt to the controller, within 500 µs, the controller has to write an 8-bit word into the FAXR register of analog chip, that conveys the constellation point locations for two consecutive bauds (8-bit word corresponds to 6 bits of Tx data in 4800 BPS mode and 4 bits in 2400 BPS mode).

The analog chip will perform quadrature modulation on the 4 LSB's first and the 4 MSB's on the next baud period. It also carries out a 50/90 percent square root of raised cosine shaping depending on the selected rate of 4800/2400 bps. In V.27 mode, the modulated signal will directly feed the transmit smoothing filter, bypassing the bandpass filter and equalizer.

In FAX mode (BR2 = 1) the operation of the V.21 modem uses the high channel and is half duplex. The input/output data will be handled through the controller interface instead of the TXD/RXD pins. When transmitting in V.21 mode, the analog chip sends interrupts to the controller at a 300 Hz ±.01% rate which serves as a timing base. Within 2 ms after every eight interrupts, the controller has to write an 8-bit word into the FAXR register that corresponds to eight consecutive transmit data bits with the LSB to be sent first.

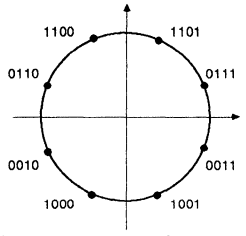


Figure 2. 4-Bit Words ($a_3a_2a_1a_0$) Identifying Constellation Points

The analog chip will perform a parallel-to-serial conversion on the 8-bit word and feed the result into the FSK modulator block. The signal path from FSK modulator input to TXA pin will be similar to the normal V.21 mode.

Receiver (V.22bis, V.22, 212A and V.21 and 103)

The receiver section consists of an energy detector, programmable gain control (PGC), part of the QAM/QPSK demodulator, FSK demodulator, 8-bit ADC and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to the energy detector and PGC circuit. The energy detector provides detection within 17 to 24 msec. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels. In call progress mode, the energy detector is connected to the output of the PGC to allow detection level adjustment.

The output of the receive filter is applied to the programmable gain control. This circuit has a wide overall range of 47.25 dB and provides 64 steps of 0.75 dB/step. The PGC gain is controlled by the external processor. It also provides auto-zeroing to minimize the output DC offset voltage.

The QAM/QPSK demodulator uses a coherent demodulation technique. Output of the programmable gain control (PGC) is applied to a Hilbert transformer that produces an in-phase and 90° out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by a free-running carrier. The baseband components are low-pass filtered to produce I and Q (Inphase and Quadrature) channel outputs. The I and Q channel outputs are both filtered by 300 Hz band-pass filters. Then they are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled and digitized into 8-bit samples by the ADC. Each channel (I and Q) is sampled twice during a baud period, once at the middle and once at the end of the baud period, allowing T/2 or T sampling operation. The external processor is interrupted once every baud period (1.667 msec). The processor should read the I and Q samples (within 100 µs from the time interrupt is issued), and perform adaptive equalization, carrier phase tracking, data decoding, and data descrambling. One quad/dibit is transferred from the SC11046 during each baud period.

In the asynchronous mode, data received from the processor is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are re-inserted. Underspeed data is passed essentially unchanged. The sync/async converter has two modes of operation. In the basic signaling mode, the buffer can accept an overspeed which corresponds to one missing stop bit in eight characters. The length of the start and data elements will be the same, and the stop bit will be reduced by 12.5%. In the extended-signaling range, the buffer can accept one missing stop bit in four characters and the stop bits will be reduced by 25% to allow for overspeed in the transmitting terminal. Output of the sync/async converter, along with the output of the FSK demodulator, is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed and output data received on the RXD pin.

For low-speed operation, the FSK demodulator is used. The output of the PGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

To improve the performance of the receiver at low signal levels, while maintaining a wide amplitude range, a 1-bit AGC circuit is placed prior to the band-pass filter. The decision thresholds of this AGC are controlled by the AGCVT bit. When AGCVT = 1, the thresholds will be 6 dB further apart than when AGCVT = 0, so that the probability of gain change will be reduced. The status of the AGC gain is available through the AGCO bit. AGC will have 8 dB more gain when AGCO = 1. Status of AGCO should be monitored at every baud timing and when it makes a transition (causing a gain-hit) the PGC's gain should be modified accordingly to prevent divergence of the adaptive equalizer.

Receiver (V.21 FAX)

When receiving in V.21FAX mode, which is half-duplex, the serial output data from FSK demodulator will be loaded into a serial-to-parallel register. The timing for serial shift as well as interrupt is derived from the received data through a resettable counter. The counter divides an input clock of 9.6 kHz by 32 to generate a 300 Hz signal. On every high to low transition of data the counter is reset and resynchronized to data timing. Assuming a received bit rate of 300 bps ±0.01%, the interrupt should have an average frequency of 300 Hz ±.01%. The controller should count the interrupt pulses and read the contents of FAXV21R register within 1.5 ms after every eighth pulse. The LSB corresponds to FSK demodulator output that has been received first in time.

Tone Detector

A digital tone detector has been implemented in the SC11046 to facilitate detection of 2100/2225 Hz tones. The output of the PGC is passed through a zero crossing detector which in turn feeds a digital timer that verifies the period of the tone. If four consecutive periods of input tone pass the requirements, then, the appropriate tone detector output (TD2100 or TD2225 bit in status register) goes high. To detect these tones user must insert the highband filter in the receive path to allow their passage, also, PGC gain must be set properly to amplify the input to the tone detector. It will be a good practice to monitor ED bit when reading TD to ensure that the signal energy is within acceptable limits.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, by turning the "Hybrid" code on through the interface, this matching is provided by an external resistor connected between the TXA and RXA pins on the SC11046. The filter section provides sufficient attenuation of the out-of-band signals to

eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter. The hybrid can be deactivated by the controller.

The SC11046 internal hybrid is intended to simplify the phone line interface. The internal hybrid can compensate for the loss in the line coupling transformer used in the DAA. By tying the GS pin to V_{SS}, ground, or V_{CC}, compensation levels of 0, +2, +3 dB, respectively, are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. An external hybrid circuit, shown in Figure 3, can be used to overcome these losses and achieve maximum performance. In this case, the internal hybrid must be turned off by setting bit 6 of the TXCR register to 0.

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC11046 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired value. In practice, however, there is impedance mismatch and a loss in the coupling transformer. Therefore, it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain (G_R) and transmit gain (G_T) are set by the ratios of resistors R2, R1 and R6, R5 respectively (Figure 3).

The circuit can be analyzed as follows:

$$V_R = -\frac{R2}{R1}\left(V_{TR}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)V_y$$

$$V_y = -\frac{R6}{R5}V_x$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_y = 2V_{TX}$,

$$V_R = -\frac{R2}{R1}\left(V_{TX}+V_{RX}\right) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)2V_{TX}$$

$$= -\frac{R2}{R1}V_{RX} + \left[\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) = \frac{R2}{R1}$$

Solving for R3/R4:

$$\frac{R3}{R4} = 1 + \frac{2R1}{R2}$$

Additionally,

$$G_R = \frac{R2}{R1} \text{ and } G_T = \frac{R6}{R5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive loss in the coupling transformer is 2.5 dB, then:

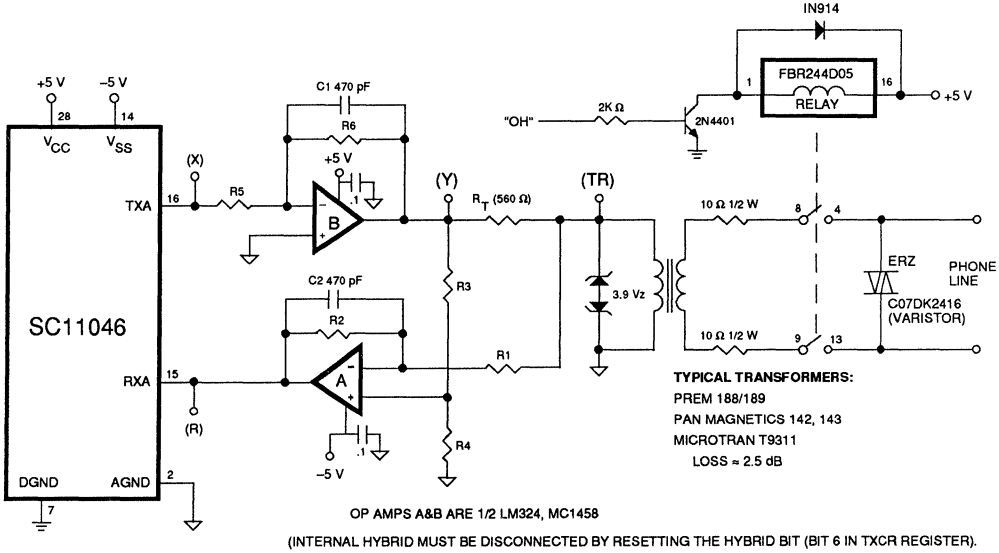
$$\frac{R2}{R1} = \text{INV Log}\left(\frac{G_{RdB}}{20}\right) = \text{INV Log}\left(\frac{2.5}{20}\right) = 1.333$$

Similarly, $\frac{R6}{R5} = 1.333$ and $\frac{R3}{R4} = 2.5$

Some typical values are:

R1=20KΩ, R2=27KΩ, R3=13KΩ, R4= 5.1KΩ, R5=20KΩ, and R6=27KΩ

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can



(INTERNAL HYBRID MUST BE DISCONNECTED BY RESETTING THE HYBRID BIT (BIT 6 IN TXCR REGISTER).

Figure 3. Using an External Hybrid with the SC11046

be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6, and capacitor C1 can be eliminated, and point X can be connected to point Y in the circuit of Figure 3 to achieve a more cost effective external hybrid arrangement.

The SC11046 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, the "Hybrid" code must be turned off. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

The tone generator section consists of a DTMF generator, V.22 guard-tone, and 1300 and 2100 Hz tone generators. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and A, B, C, D, *, and # keys. The V.22 guard-tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the tone control register. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to 1300 and 2100 Hz and the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50K Ohms is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation—no attenuation, 6 dB attenuation, 12 dB attenuation, and squelch are provided through the ALC1 and ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Clock Input

CLKIN (Pin 22) of the SC11046 should be connected to a 9.8304 MHz clock source with an accuracy of ±0.01%. Alternatively, a 12.288 MHz clock can be used if the CLKSEL bit in the MCRB control register is set.

FUNCTIONAL DESCRIPTION OF THE SC11011 CONTROLLER

The SC11011 modem controller, implemented in Sierra's 1.5 micron CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus or an RS-232 serial interface. Besides including a 16-bit microprocessor, 8k by 8 bytes of ROM and 128 by 8 bytes of RAM, it also contains the functionality of a 82C50B UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem with Sendfax capability for the PC consists of the SC11011 controller with external memory, the SC11046 modem and the DAA. All of the popular communications software written for the PC will work with the SC11046/SC11011 set.

The SC11011 can be configured for RS-232 applications. The difference is that the UART is wired so that the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The controller receives an 8-bit signal sample from the SC11046 and performs adaptive equalization, carrier phase recovery, data decode, and descrambling. The controller is configured for parallel or serial applications by the firmware. The controller is designed by using a 16-bit 2900 processor to perform the digital signal processing and the control functions. Its instruction set is a subset of the Intel 8096 instruction set, but operates faster than the 8096.

The SC11011 provides a standard 5V logic level interface—RS-232 drivers are required to interface to the port. Firmware for external memory comes with the SC11011. It includes the Hayes "AT" command set, and T.30 protocol. When used with the SC11046 modem, it emulates a Hayes-type stand-alone or internal modem with Sendfax.

The SC11011 is available in a 68 pin PLCC. The 68 pin package allows the controller to access external ROM of up to 32K bytes and external RAM of up to 16K bytes. This allows users to customize their own software, and provides a means for software development. The serial controller can talk to both an SC11046 and an SC22201 (EERAM).

The SC11011 requires a single +5 V power supply. Besides the interface for the SC11046 modem, when the SC11011 controller is used for internal applications, it has an eight-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 82C50B UART. It also has control lines for ring indication, the off-hook relay, and a data/voice relay; these lines connect to the DAA.

When used in RS-232 applications the SC11011's, eight-bit port becomes the switch input lines, and

the address, chip select, INTO, DIST and DOST lines become the lines for the RS-232 interface, and modem status. These lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control—so the main difference between the SC11011 application is the firmware in the external memory. It also contains the same modem and DAA interface lines.

The interface to the SC11046 is via an 8-bit address/data bus and the control lines for read and write. The same interface is used for access to an electrical erasable random access memory (SC22201). There are six clock multiplexed address/data bus cycles. A ready signal is provided for the interface to a high speed PC-AT type bus cycle. The 68 pin package, has 15 extra address lines and chip selects for external ROM and external RAM interfaces. An $\overline{EA}$ pin is also available for selection of internal ROM or external ROM.

The SC11011 is truly an ASIC controller—it is designed to control a modem or other peripheral that operates at a moderately slow data rate up to 2400 bits per second. What's unique about the SC11011, for example, is that it allows a slow peripheral to interface to a high speed bus without making the main processor add unnecessary wait states.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11011 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up, it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like a Hayes-type modem. The escape sequence is three + signs—+++ —in the default mode, but it can be changed in the software.

The actual processor contains a 16-bit data path and can execute 54 instructions with three different addressing modes: direct, indirect, and immediate. There is 8K by 8 of ROM on the chip for program storage.

To the system bus, the SC11011 looks and acts like a 8250B UART. Communications software written for this UART will work with the SC11011. The Sierra chip set is truly a Hayes-type modem in two chips, with the addition of Sendfax (The SC11021,22 controllers may also be used with the SC11046. They include a 16C450 type UART).

THE SC11046 & SC11011 SYSTEM

The only external components required by the SC11046 are a 600 Ohm line matching resistor and a 1.0 µF capacitor from the EDC pin to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11046 can directly drive a high impedance (50 kΩ) earphone-type transducer.

The SC11046 modem's CLKIN pin line is driven by the SC11011 CKOUT line at 9.8304 MHz. The SC11011 interfaces directly to an IBM PC bus. The only external parts may be an 8 input NAND gate for COM1 and COM2 decoding inside the PC. A ready signal is provided to control the IOCHRDY pin on the bus to allow operation with higher speed computers (AT, XT TURBO, etc.)

For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

All modems require a DAA. A DAA or data access arrangement is a piece of equipment required by the FCC to connect anything to the general switched telephone network. It consists of an isolation transformer, typically 600 Ω to 600 Ω; a relay for disconnecting the modem from the line; a ring detector, typically an optoisolator; and high voltage surge protectors. The DAA has to be FCC registered and this can be done by one of many consultants and labs around the country. The fee is typically $2,000 and it takes several weeks. Another alternative is to buy a DAA, supplied by several manufacturers.

V.22bis is a CCITT specification that calls for 2400 bit per second, full or half duplex data transmission with a fallback mode of 1200 bps. It is not 2400 baud; the spec calls for transmission of quadbits—4 bits per baud so the 2400 bps transmission takes place at 600 baud. The same is true for V.22—it is 1200 bps or 600 baud. V.22 does not call for a 300 baud fallback; there is a CCITT standard for 300 bps and that's V.21.

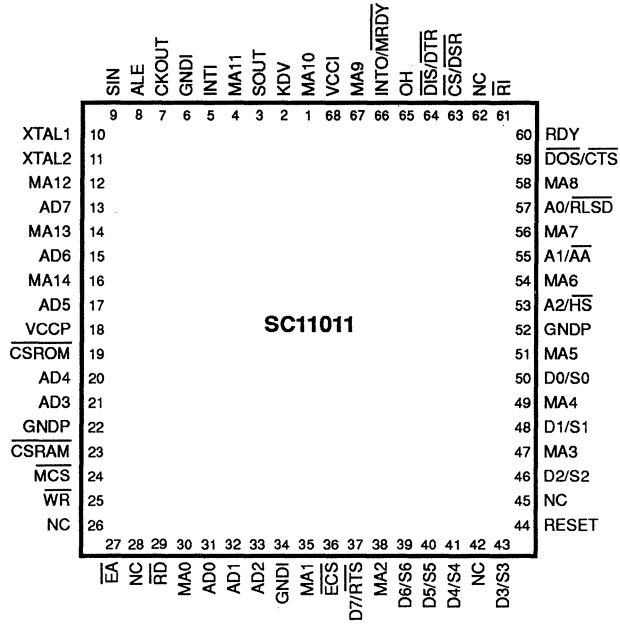
V.22 and V.22bis also call for guard tones to be sent along with the data.

In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The SC11046 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 550 and 1800 Hz notch filter to remove the guard tone in the receiver.

V.27ter is a CCITT specification calling for 4800 bps full or half duplex data transmission with a fallback to 2400 bps.

All modems require a Hybrid; a term used to describe a circuit, passive or active, that takes the separate transmit and receive signals and combines them to go over the phone line. In the SC11046, this is done with op amps. The hybrid can be disabled so an external hybrid can be used, if desired.

CONNECTION DIAGRAM



Note: INT0 is not three state on the SC11011 revs before "G".
(The revision letter is found on the underside of the package)

MAC Pinout Diagram: 68 Pin Package

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	SCR	Synchronous Clock Receive (Data set source); Output; TTL; Used only in bit synchronous mode; Recovered by the Receiver Phase Locked Loop from the far end modem. Data on RXD is valid at the rising edge of this clock.
2	AGND	Analog Ground.
3	SCT	Synchronous Clock Transmit (Data set source); Output; TTL; Used only in bit synchronous mode; Generated internally by the SC11046 Clock Generator; Rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
4	SCTE	Synchronous Clock Transmit External (DTE source); Input; TTL; Used only in bit synchronous mode; Data on TXD line is latched by the SC11046 at the rising edge of this clock. Clock rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
5	AUDIO	Audio output; The hybrid output is passed through a programmable attenuator and fed to this analog pin. Four different levels can be attained by controlling bit 0 and bit 1 of the AUDIO register as specified under AUDIO register description.
6	EDC	Capacitor for energy detect; A 1.0 μF capacitor should be connected between this pin and AGND.
7	DGND	Digital ground
8	$\overline{CS}$	Chip Select; Input; TTL; Active low.
9	$\overline{WR}$	Write; Input; TTL; Normally high; Data on AD7–AD0 is written into the SC11046 registers at the rising edge of this pulse.
10	$\overline{RD}$	Read; Input; TTL; Normally high; Data on AD7–AD0 is to be read by the processor at the rising edge of this pulse.
12,13,17,18	AD1–AD4	Multiplexed address/data bus (8-bits); Input/Output; TTL; A/D4–A/D1 (4-bits) are used for multiplexed addressing of internal registers.
14	V_{SS}	–5 V Supply
15	RXA	Receive analog; Input
16	TXA	Transmit analog; Output
11,19–21	D0, D5–D7	Bits 0, 5, 6 and 7 are don't cares as far as address is concerned.
22	CLKIN	Clock input; 9.8304 MHz or 12.288 MHz clock input from the controller.
23	GS	Gain Select to compensate for loss in line coupling transformer. When left open or tied to V_{SS}, the compensation is 0 dB; connected to ground, +2 dB compensation is provided; and when tied to V_{CC}, the compensation is +3 dB.
24	ALE	Address Latch Enable; Input; TTL; The address on A/D4–A/D1 is latched into the SC11006 Address decoder at the falling edge of this normally low pulse.
25	INT	Interrupt; Output; TTL; Normally low; A short (13 μs typical) positive pulse is generated after all A to D conversions are completed.
26	RXD	Received Data; Output; TTL
27	TXD	Transmit Data; Input; TTL
28	V_{CC}	+5 V supply

REGISTERS

There are fourteen 8-bit registers interfacing to the microprocessor bus. Six of these registers can only be read by the processor (called READ registers) and the remaining eight can be written into by the processor (called CONTROL registers). Bit 1 of the "Tone" register can be read and written by the processor, Table 1 shows the address and bit assignments for these registers.

A chip select pin is provided for multi-peripheral addressing by the processor.

Table 1. READ Registers

ADDRESS BITS				NAME	MSB			BIT NUMBER				LSB
A4	A3	A2	A1		7	6	5	4	3	2	1	0
0	0	0	0	Q1	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
0	0	0	1	I1	I17	I16	I15	I14	I13	I12	I11	I10
0	0	1	0	Q2	Q27	Q26	Q25	Q24	Q23	Q22	Q21	Q20
0	0	1	1	I2	I27	I26	I25	I24	I23	I22	I21	I20
0	1	0	0	Status	X	X	X	AGCO	TD2100	TD2225	FSKD	ED
0	1	0	1	FAXV21R	R7	R6	R5	R4	R3	R2	R1	R0
0	1	X	1	Unused		Unused						
0	1	1	X	Unused		Unused						

STATUS Register: Address (A4–A1) = 0100

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–5	Unused	
Bit 4	AGCO	Status of internal 1-bit AGC. When this bit is set, RXA signal is amplified by 8 dB before entering the bandpass filters.
Bit 3	TD2100	2100 Hz tone detector output. TD2100=1 when this tone is present.
Bit 2	TD2225	2225 Hz tone detector output. TD2225=1 when this tone is present.
Bit 1	FSKD	Received FSK data. FSKD = 1 when mark is received.
Bit 0	ED	Energy detect circuit output. ED = 1 when energy detected.

Note: When reading unused bits, the corresponding bus lines will not be driven by the SC11046 and will be floating.

FAXV21R Register: Address (A4–A1) = 0101

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–0	R7–R0	In V.21 FAX receive mode this register will be loaded by received data and should be read every eighth interrupt pulse. LSB (R0) corresponds to the data bit received first in time.

Table 1a. READ Registers

Q1 Register:	Stores midbaud inphase sample output of ADC.
I1 Register:	Stores midbaud quadrature sample output of ADC.
Q2 Register:	Stores endbaud inphase sample output of ADC.
I2 Register:	Stores endbaud quadrature sample output of ADC.

Note: All samples are represented in two's complement form.

Table 2. CONTROL Registers

ADDRESS BITS				NAME	BIT NUMBER							
A4	A3	A2	A1		7	6	5	4	3	2	1	0
1	0	0	0	TXCR	X	HYBRID	TXSEL2	TXSEL1	TXSEL0	SQT	BR1	BR0
1	0	0	1	MCRA	X	LCK/$\overline{\text{INT}}$	RNGX	SYNC	WLS1	WLS0	A/$\overline{\text{O}}$	RXMRK
1	0	1	0	MCRB	X	BR2	TONDETE	CPM	ALB	TL2	TL1	TL0
1	0	1	1	TONE	X	HNDSHK	TONEON	DTMF	D3	D2	D1	D0
1	1	0	0	PGCR	X	AGCVT	G5	G4	G3	G2	G1	G0
1	1	0	1	DATA	X	PLLJAM	PLLFRZ	PLLFAST	RD3	RD2	RD1	RD0
1	1	1	0	AUDIO	X	DISS	PGCZ	TST2	TST1	TST0	ALC1	ALC0
1	1	1	1	FAXR	B7	B6	B5	B4	B3	B2	B1	B0

Transmit Control Register (TXCR): Address (A4–A1) = 1000

(Note: When writing into these registers, the bus lines corresponding to the unused bits are ignored by the SC11006.)

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	HYBRID	When set, the transmitter output (TXA) is connected to the inverting input of the receive buffer to allow the use of the on-chip hybrid circuit for 2 to 4 wire conversion.
Bit 5 and Bit 4 and Bit 3	TXSEL2 and TXSEL1 and TXSEL0	Transmit Select bits. These 3 bits determine the data transmitted by the transmitter according to the following table:

TXSEL2	TXSEL1	TXSEL0	TRANSMITTED DATA
0	0	0	External data sent by DTE.
0	0	1	Unscrambled S1 (Note 1).
0	1	0	Unscrambled Space.
0	1	1	Unscrambled Mark.
1	0	0	Scrambled RX. Digital loop back mode (Note 2).
1	0	1	Scrambled Reversals (Notes 3 and 4).
1	1	0	Scrambled Space (Note 4).
1	1	1	Scrambled Mark (Note 4).

Note 1: S1 is a pattern of 0011 transmitted at 1200 bps rate regardless of BR1. If in FSK mode (BR0 = 1), then reversals are sent. This pattern cannot be sent at 2400 bps rate.

Note 2: In this mode, the received data, after being descrambled, is sent back to the scrambler. The modem will automatically go to the Synchronous mode with Slave timing.

Note 3: Reversals are continuous streams of 01.

Note 4: When in FSK mode (BR0 = 1), TXSEL2 is ignored since scrambling is not applicable.

Bit 2 — SQT — When this bit is set, the transmitter is squelched by connecting the output of MUX1 (see the block diagram) to analog ground.

Bit 1 and Bit 0 — BR1 and BR0 — Bit Rate Selection bits based on the following table:

BR2	BR1	BR0	BIT RATE
0	0	0	2400 bps V.22 bis
0	1	0	1200 bps V.22/212A
0	0	1	0–300 bps Bell 103
0	1	1	0–300 bps CCITT V.21
1	0	0	4800 bps V.27
1	1	0	2400 bps V.27
1	0	1	N.A.
1	1	1	0–300 bps V.21FAX

CONTROL REGISTERS (Cont.)

Mode Control Register A (MCRA): Address (A4–A1) = 1001

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	LCK/INTB	Determines the clock source for the transmitter. When this bit is set, the clock source is externally provided on SCTE (pin 4), and when cleared, it is internally generated (SCT). This bit can select the clock source independent of Sync/Async mode selection (see below). When in Digital Loop-Back mode, the clock source will be forced to the Slave mode (SCR).
Bit 5	RNGX	Range extender for the receiver Sync/Async converter. When set, the receiver Sync/Async can insert up to one stop bit per four (8, 9, 10 or 11-bit) characters to compensate for a far end DTE being up to 2.3% over speed. The transmitter Async/Sync always handles this overspeed condition regardless of this bit's condition.
Bit 4	SYNC	When set, operate in bit synchronous mode; when clear, operate in character asynchronous mode. When in Digital Loop-Back mode, the SC11046 will be forced to the Synchronous mode.
Bit 3 and Bit 2	WLS1 and WLS0	Word length select bits in asynchronous mode, according to the following table:
Bit 1	A/$\overline{O}$	When set, operate in answer mode; when clear, operate in originate mode.
Bit 0	RXMARK	When set, the RXD pin is clamped to the high logical level.

WLS1	WLS0	NUMBER OF BITS PER CHARACTER
1	0	8
1	1	9
0	0	10
0	1	11

Mode Control Register B (MCRB): Address (A4–A1) = 1010

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	BR2	This bit in conjunction with BR1 & BR0 selects the bit rate.
Bit 5	TONDETE	When this bit is set, 2100/2225 Hz tone detector will be enabled. However, for proper functioning, highband filter must be set in the receive path to pass these tones. Tone amplification before detection can be set by PGC.
Bit 4	CPM	Call progress monitor mode. When set, the receive path can be connected to the high band filter to detect answer tone (ALB=0) or to the low band filter scaled down 2.5 times (ALB=1) to listen for the call progress tones during auto dialing.
Bit 3	ALB	Analog Loop Back. When set, the transmitter output (TXA) is connected to the receive path, bypassing the receive filter.
Bit 2 and Bit 1 and Bit 0	TL2 and TL1 and TL0	Transmit level adjust bits based on the following table:

TL2	TL1	TL0	TRANSMIT LEVEL AT TXA PIN
0	0	0	0 dBm
0	0	1	–2 dBm
0	1	0	–4 dBm
0	1	1	–6 dBm
1	0	0	–8 dBm
1	0	1	–10 dBm
1	1	0	–12 dBm
1	1	1	–14 dBm

CONTROL REGISTERS (Cont.)

TONE Register: Address (A4–A1) = 1011

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	HNDSHK	This bit is set only during handshaking sequence. When set, both FSK and PSK/QAM demodulators are enabled. When cleared, FSK demodulator is disabled when in high speed mode.
Bit 5	TONEON	When set, the output of the tone generator appears at TXA. When cleared, the output of the tone generator is squelched.
Bit 4	DTMF*	When set, the DTMF generator is turned on. When cleared, the DTMF generator is turned off, but other tones can be generated.
Bits 3–0	D3–D0	Specify the desired tone (see the following table):

DTMF	D3	D2	D1	D0	DIGIT DIALED	TONE OUTPUT	FREQUENCIES (HZ)
1	0	0	0	0	0	941	1336
1	0	0	0	1	1	697	1209
1	0	0	1	0	2	697	1336
1	0	0	1	1	3	697	1477
1	0	1	0	0	4	770	1209
1	0	1	0	1	5	770	1336
1	0	1	1	0	6	770	1477
1	0	1	1	1	7	852	1209
1	1	0	0	0	8	852	1336
1	1	0	0	1	9	852	1477
1	1	0	1	0	*	941	1209
1	1	0	1	1	(A)	697	1633
1	1	1	0	0	(B)	770	1633
1	1	1	0	1	(C)	852	1633
1	1	1	1	0	#	941	1477
1	1	1	1	1	(D)	941	1633
0	0	0	0	0	No tone; tone generator turned off		
0	0	0	0	1	550		
0	0	0	1	0	1800		
0	0	0	1	1	2100		
0	0	1	0	0	1300		
0	0	1	0	1	1100		
0	0	1	1	x	462		
0	1	x	x	x	No tone; tone generator turned off		

Note: TONEON must also be set to generate DTMF signals.

Programmable Gain Controller Register (PGCR): Address (A4–A1) = 1100

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	AGCVT	When set, prevents gain hit due to AGC's gain step. This bit must be set during the handshaking after detecting the four point constellation and before switching to 16-way decision making.
Bits 5–0	G5–G0	Control the gain of the PGC within a range from –10 to +37.5 dB in 0.75 dB steps. (See the following table):

CONTROL REGISTERS (Cont.)

G5	G4	G3	G2	G1	G0	PGC GAIN (dB)
0	0	0	0	0	0	–10.0
0	0	0	0	0	1	–9.25
0	0	0	0	1	0	–8.5
0	0	0	1	0	0	–7.0
0	0	1	0	0	0	–4.0
0	1	0	0	0	0	+2.0
1	0	0	0	0	0	+14.0
1	1	1	1	1	1	+37.25

Note: Signal level is adjusted (before entering the filter) by an internal AGC with +12 dB or 0 dB gain, plus a fixed gain of 5 dB.

DATA Register: Address (A4–A1) = 1101

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	PLLJAM	When this bit is set, the DPLL will be reset by the next rising edge of the received baud clock. This bit must remain high for at least one baud period. It should be cleared by the processor to end the jamming mode. PLLFRZ (see below) overrides PLLJAM when both are enabled.
Bit 5	PLLFRZ	Phase locked loop freeze. When this bit is set, the DPLL begins to run freely regardless of the received baud clock. To re-enable the DPLL locking, the bit must be cleared by the processor. PLLFRZ overrides PLLJAM when both are enabled.
Bit 4	PLLFAST	When set, the DPLL operates in "fast" locking mode. In this mode, the DPLL is updated on every baud period by 13 µs steps. When this bit is cleared (default mode), the DPLL operates in "normal" locking mode and is updated once every 8 baud periods by 6.5 µs steps.
Bit 3–0	RD3–RD0	Four-bit Received Data. Used only in high speed (1200 or 2400 bps) mode, they are descrambled by the processor and shifted out by the SC11046. Sync to Async is also done by the SC11046, when in the asynchronous mode. RD0 is the first bit appearing on the RXD pin, followed by RD1, RD2 and RD3. In the 1200 bps mode, only RD0 and RD1 are shifted out during one baud period.

AUDIO Register: Address (A4–A1) = 1110

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	DISS	When this bit is set, the scrambler is disabled, when cleared, it is enabled. Transmit select bits (TXSEL0–2) override this bit when in "transmit internal mode".
Bit 5	PGCZ	When set, the output of the PGC is grounded. DC offset of the demodulator can be stored and canceled by the controller.
Bit 4–2	TEST	Test bits used for factory testing. For normal chip operation, these bits must be cleared.
Bit 1	ALC1	Audio level control bit 1.
Bit 0	ALC0	Audio level control bit 0. These two bits are used to control the audio level at AUDIO pin according to the following table:

ALC1	ALC0	AUDIO ATTENUATION (dB)
0	0	Audio off
0	1	12
1	0	6
1	1	0 (no attenuation)

Note: The audio signal may be amplified by 12 dB by the line receiver AGC before being fed to the audio attenuator.

CONTROL REGISTERS (Cont.)

FAX Register: Address (A4–A1) = 1111

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–0	B7–B0	In V.27 mode, this register has to be loaded at every interrupt with an 8-bit word that identifies constellation points for two consecutive baud periods. 4 LSB's correspond to first baud in time. In V.21FAX mode, when transmitting, the register should be loaded every eighth interrupt pulse. In V.21FAX, LSB is the data bit which is first in time.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1—SC11046 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 4.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11046 in the synchronous mode. This provides a 2400/1200 Hz clock on the SCT pin that can be used as a clock source for the DTE. The Transmit Phase-Locked-Loop (TX PLL) of the SC11046 will be in free-running mode.

Case 2—SC11046 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode, also select "Locked" mode.

The TX PLL of SC11046 will then synchronize itself to the clock provided on its "SCTE" pin.

Case 3—Slave mode. The Transmit Timing is slaved to the receiver recovered clock. Select synchronous mode and connect SCTE to SCR.

In either case, the SC11046 will sample the data on the rising edge of the clock.

Receiver Timing

In synchronous mode, the recovered clock will be provided on the SCR pin and the transitions of RXD will be on the falling edges of this clock. Data is valid on the rising edge of the clock.

SYNCHRONOUS MODE CHART

Transmitter Timing

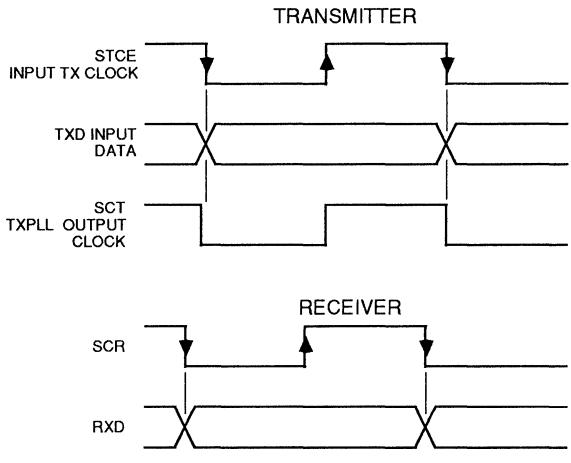


Figure 4. SC11046 Synchronous Mode Timing Diagrams.

SPECIFICATIONS

Absolute Maximum Ratings (Notes 1–3)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS}–0.6 to V_{CC} +0.6 V
DC Input Voltage (Digital Signals)	V_{SS}–0.6 to V_{CC} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
F_C	Clock Frequency	CLKSEL = 0	9.8295	9.8304	9.8313	MHz
		CLKSEL = 1	12.2868	12.288	12.2892	MHz
T_R, T_F	Input Rise or Fall Time	All digital inputs except CLKIN			500	ns
T_R, T_F	Input Rise or Fall Time	CLKIN			20	ns

DC Electrical Characteristics (T_A = 0 TO 70°C, V_{CC} = +5 V ± 10%, V_{SS} = –5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	Normal		18	35	mA
I_{SS}	Quiescent Current			18	35	mA
V_{IH}	High Level Input Voltage; Digital pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital pins				0.8	V
V_{OH}	High Level Ouput (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Ouput (I_{OL} = 1.6 mA)				0.6	V
VXTA	Maximum Peak Output Level on TXA pin	V_{CC} = +5 V V_{SS} = –5 V	±3			V

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

SPECIFICATIONS (Cont.)

AC Electrical Characteristics

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
		Processor Bus Interface: (See Figure 5)					
1	TAVLL	Address valid to end of ALE		41			ns
2	TLLAX	Address hold after end of ALE		61			ns
3	TAVDV	Address valid to output data valid				336	ns
4	TRLDV	$\overline{RD}$ active low to output data valid				194	ns
5	TRXDZ	End of $\overline{RD}$ to output data Hi Z				61	ns
6	TLHLL	ALE pulse width		71			ns
7	TRLRH	$\overline{RD}$ pulse width		214			ns
8	TWLWH	$\overline{WR}$ pulse width		148			ns
9	TQVWX	Data valid to end of $\overline{WR}$ active		132			ns
10	TWXQX	Data hold after end of $\overline{WR}$		56			ns
11	TLLRL	End of ALE to $\overline{RD}$ or $\overline{WR}$ active		60			ns
12	TRHLH	End of $\overline{RD}$ to next ALE		55			ns
13	TWXLH	End of $\overline{WR}$ to next ALE		120			ns

BUS TIMING

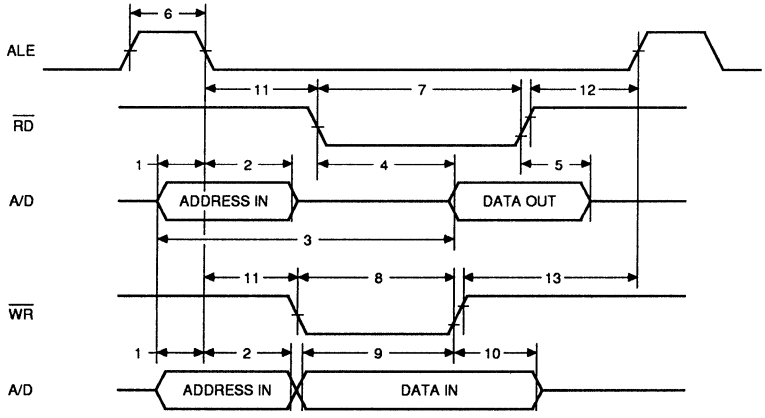


Figure 5. Processor Bus Timing

SPECIFICATIONS (Cont.)

AC Electrical Characteristics

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	TINT1	Interrupt period in V.21 FAX	Send mode AOB = 1		3.333		ms
1	TINT1	Interrupt period in V.21 FAX	Receive mode AOB = 0	1.6	3.333		ms
2	TWINT1	Interrupt pulse width	V.21 FAX mode		52		µs
3	TDWR1	Interrupt to $\overline{WR}$ active, delay	V.21 FAX, AOB = 1	0.01		2000	µs
4	TAWR1	End of $\overline{WR}$ to next interrupt	V.21 FAX, AOB = 1	1			µs
5	TDRD	Interrupt to $\overline{RD}$ active, delay	V.21 FAX, AOB = 0	0		3	ms
6	TARD	End of $\overline{RD}$ to next interrupt	V.21 FAX, AOB = 0	1			µs
7	TINT2	Interrupt period V.27	BR2 = 1, BR1 = BR0 = 0		1.25		ms
7	TINT2	Interrupt period V.27	BR2 = BR1 = 1, BR0 = 0		1.667		ms
8	TWINT2	Interrupt pulse width	V.27 mode		17		µs
9	TDWR2	Interrupt to $\overline{WR}$ active, delay	V.27 mode	0.01		500	µs
10	TAWR2	End of $\overline{WR}$ to next interrupt	V.27 mode	1			µs

BUS TIMING

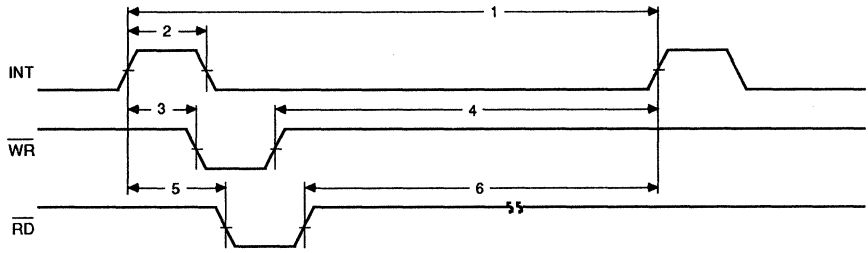


Figure 5a. V.21 FAX Timing W.R.T. Interrupt Signal

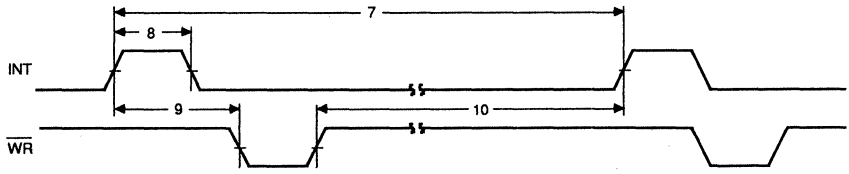


Figure 5b. V.27 Timing W.R.T. Interrupt Signal

SPECIFICATIONS (Cont.)

Modem Transmit Signals—Hz (Assume 9.8304 Crystal)

PARAMETER	CONDITIONS		NOM.	ACT.	UNITS
FSK Mod/Demod Frequencies					
Bell 103					
Answer Mark			2225	2226	Hz
Answer Space			2025	2024.4	Hz
Originate Mark			1270	1269.4	Hz
Originate Space			1070	1070.4	Hz
CCITT V.21					
Answer Mark			1650	1649.4	Hz
Answer Space			1850	1850.6	Hz
Originate Mark			980	978.34	Hz
Originate Space			1180	1181.53	Hz
Call progress monitor mode:		**MIN**	**TYP**	**MAX**	
Center frequency	ALB = 1		480		Hz
Detect level (ED high) measured at RXA		–43			dBm
Reject level (ED low) measured at RXA				–48	dBm
Hysterisis		2			dB
Delay time (ED low to high)	EDC = 1.0 µF	10	15	24	ms
Hold time (ED high to low)	EDC = 1.0 µF	10	15	24	ms

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQUENCY	ALLOWABLE ERROR	ACTUAL ERROR
Row 1	697 Hz	±1%	–0.23%
Row 2	770 Hz	±1%	–0.01%
Row 3	852 Hz	±1%	–0.12%
Row 4	941 Hz	±1%	–0.39%
Column 1	1209 Hz	±1%	–0.35%
Column 2	1336 Hz	±1%	–0.93%
Column 3	1477 Hz	±1%	–0.48%
Column 4	1633 Hz	±1%	–0.91%
Guard Tones	550 Hz	±20 Hz	–2 Hz
	1800 Hz	±20 Hz	–2 Hz
Calling Tone	1300 Hz		–6 Hz
Answer Tone	2100 Hz	±15 Hz	+3.2 Hz
Calling Tone	1100 Hz	±38 Hz	–3.8 Hz
PIS Tone	462 Hz	±1.5 Hz	–0.05 Hz

SPECIFICATIONS (Cont.)

DTMF Generator (Cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion	VCC = +5 V VSS = –5 V TL2 = TL1 = TL0 = 0 Measured at TXA Pin		–40		dB
Row Output Level			0		dBm
Column Ouput Level			2		dBm
550 Hz Guard Tone			–3		dB (Note 2)
1800 Hz Guard Tone			–6		dB (Note 2)
1300 Hz Calling Tone			0		dB
2100 Hz Answer Tone			0		dB
Transmit level measured at TXA	Load = 1200 Ohms TL2 = TL1 = TL0 = 0 Squelched		0	 –50	dBm dBm

Notes: 1. This assumes a clock of exactly 9.8304 MHz.
2. These levels are referenced to the TX signal level. When guard tones are added, the TXA level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Mode	EDC = 1.0 µF; measured at RXA PGC = 0				
Energy detect level (ED low to high)				–43	dBm
Loss of energy detect level (ED low to high)		–48			dBm
Hysterisis		2	3		dB

Programmable Gain Controller (PGC)

Gain step size			0.75		dB
Dynamic range			47.25		dB
Response time (from change in PGC register to output of A to D converter)			1.0		ms

Filter Characteristics

Crosstalk rejection			70		dB
Power supply rejection			0		dB
DPLL Response times JAM or FRZ Fast			20 200		µs µs

APPLICATIONS INFORMATION

Applications

The SC11046 with an external control microprocessor, a telephone line interface and a suitable computer interface, can implement a complete 2400 bps modem for many applications with a minimum of components and cost. Figure 6 shows the common portion of such a modem using the SC11046 with a telephone line interface. Sierra's SC22201, 128 byte E^2 memory is used to store default parameters and often used phone numbers. Figure 6 and 7 shows the common circuitry for both stand-alone and PC bus integral modems implemented with Sierra's SC11011 controller and SC11046 modem. Figure 8 shows an RS-232C serial interface for implementing a stand-alone modem. Figure 9 shows a parallel bus interface for implementing an internal modem for an IBM PC/XT/AT compatible computer. Figure 10 shows a power supply schematic for a stand-alone modem application.

Various modem configurations can be realized by combining schematics shown in Figures 6 thru 10.

A Hayes compatible stand-alone smart modem can be implemented by combining Figures 6, 7, 8 and 10.

The internal version for an IBM PC/XT/AT compatible can be implemented using Figures 6, 7 and 9.

For performance evaluation, the circuit shown in Figure 11 can be used to obtain the receiver constellation. Quality of the signal processing performed by the modem can thus be visualized by observing the constellation for various line conditions and signal to noise ratios.

Power Supply Decoupling and Circuit Layout Consideration

For optimum performance at low received signal levels with low s/n ratios, it is important to use the recommended power supply decoupling circuit as shown in Figure 7.

Small inductors in series with the supplies help suppress RFI as well as improve the power supply noise rejection capability of the SC11046. A 10 Ω, 1/4 W resistor in place of, or in series with, the inductor in the SC11046 power leads has been found to be helpful in computer based products where the power supplies are particularly noisy.

The 10 µF capacitors should be a tantalum type while the 0.1 µF capacitors should have good high frequency rejection characteristics—monolithic ceramic types are recommended. It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11046 as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply. Avoid routing digital traces through the analog area.

Ferrite beads on the ±5 V input to the circuit board should also be considered, both from a modem performance standpoint, as well as an aid in reducing RF radiation from the phone lines.

Note: Crystal oscillator: SC11011 requires a parallel resonant 19.6608 MHz crystal designed with CL = 18 pF and tolerance of ± .01% (such as Saronix NYP196-18). With this crystal, use 27 pF to ground from XTAL1 (Pin 10) and XTAL2 (Pin 11). Clock frequency measured at CKOUT (Pin 7) must be within ±0.01% of 9.8308 MHz.

APPLICATIONS INFORMATION (Cont.)

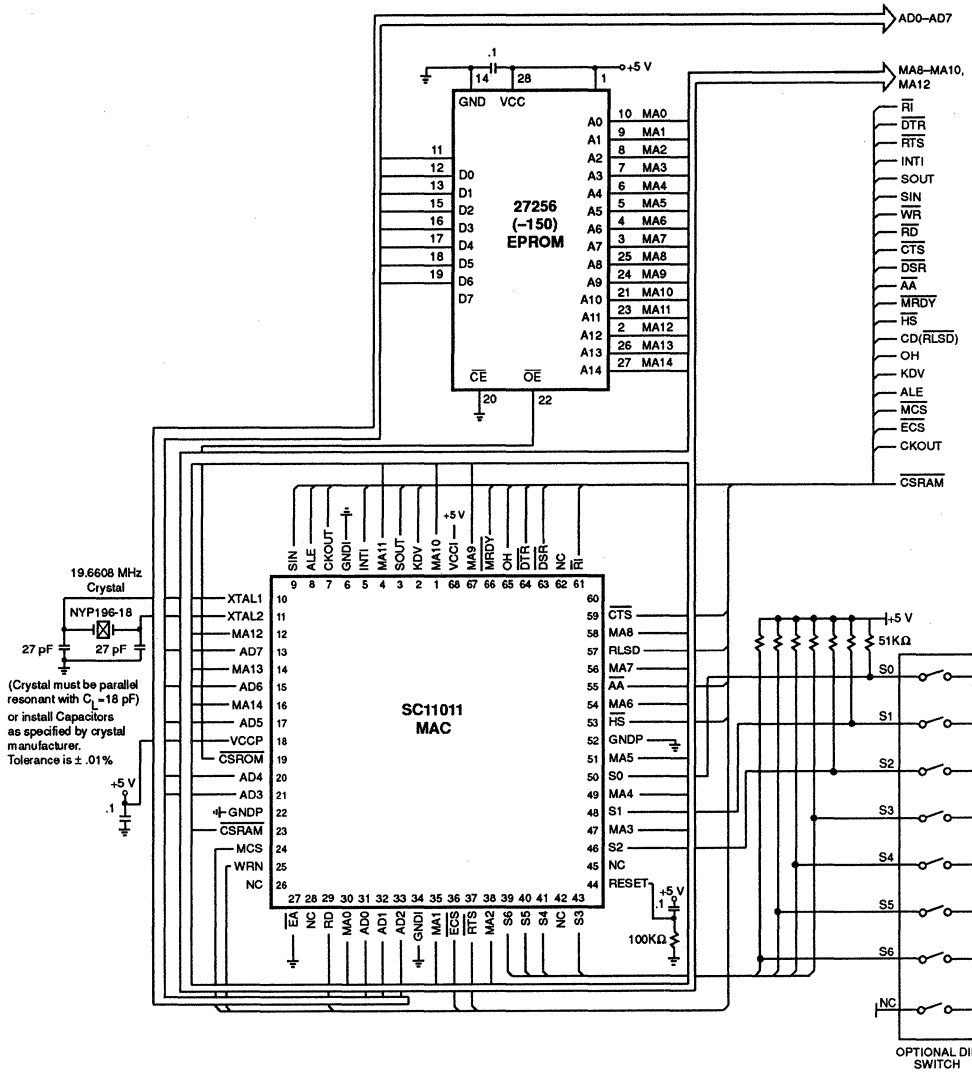
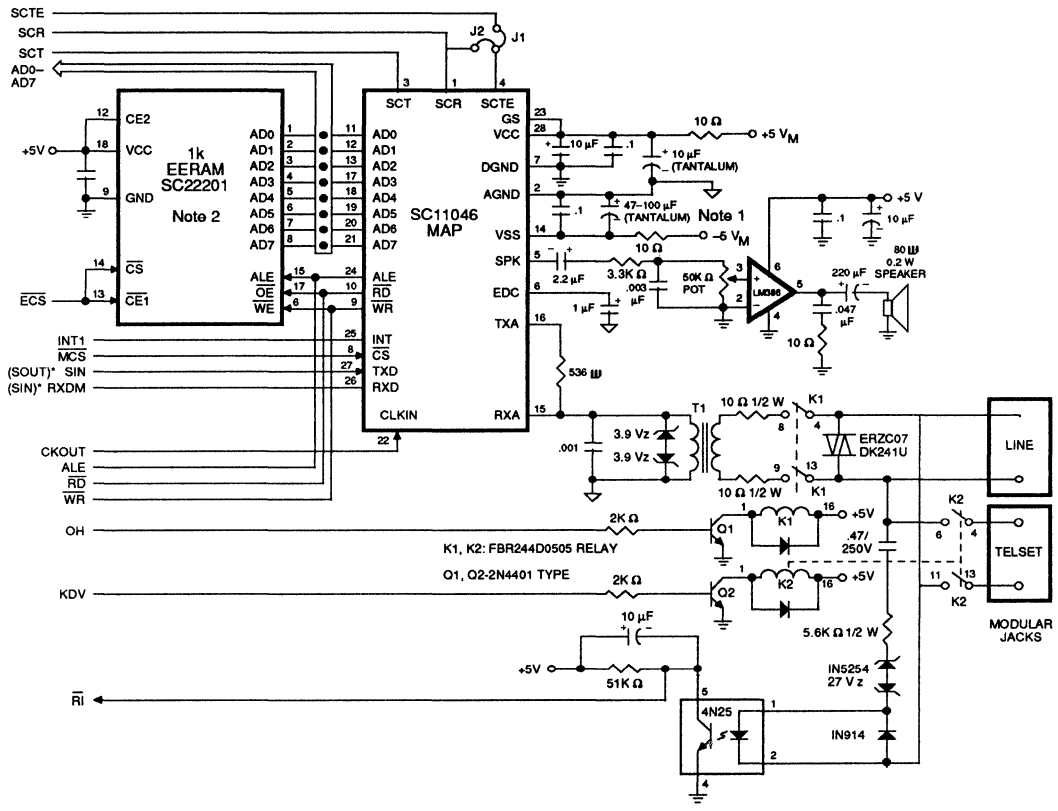


Figure 6. Special Purpose Control Processor for Stand-Alone or Parallel Applications.

Consult controller data sheet for programming information.

APPLICATIONS INFORMATION (Cont.)



Note 1: Connect analog ground directly to common of the power supply filter capacitor.

Note 2: A serial EERPROM may be substituted when using the SC11039, SC11040, SC11041 or SC11022 Modem Advanced Controller (48 and 68 pin versions), or SC11043 44 pin version.

Note 3: For external clocking of the transmitter, install J1 and set bit 6 of the MCRA; omit J2.
For slave clocking of the transmitter, install J2 and set bit 6 of the MCRA; omit J1.
For normal operation, omit J1 and J2, and clear bit 6 of the MCRA.

*When used in the configuration as a parallel modem (Figure 6), connect Pin 27 of SC11046 to SOUT pin of controller and connect Pin 26 of SC11046 to SIN pin of controller.

Figure 7. Common Portion of 2400 bps Modem.

APPLICATIONS INFORMATION (Cont.)

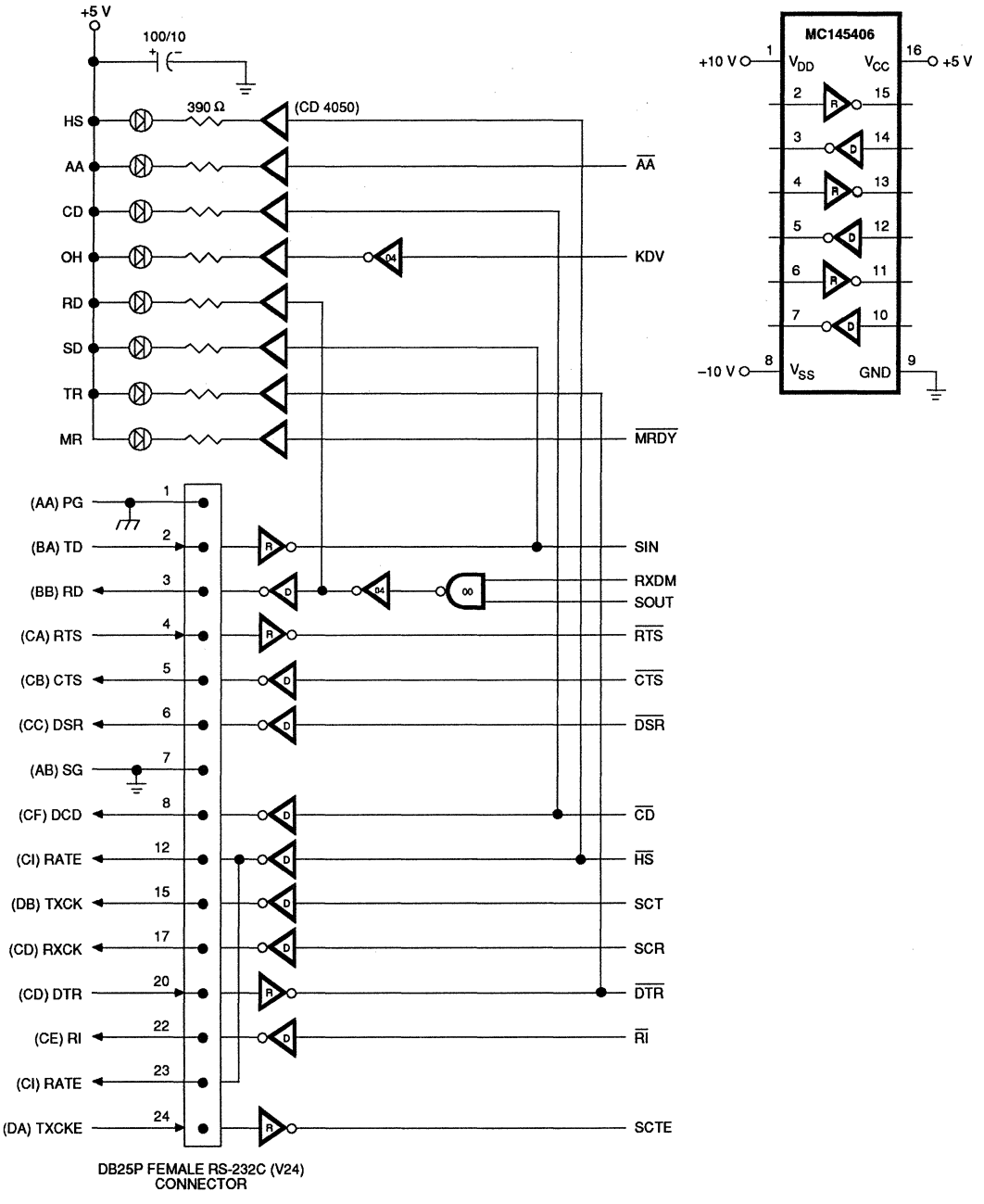


Figure 8. RS-232C Interface for Stand-Alone Modem Application.

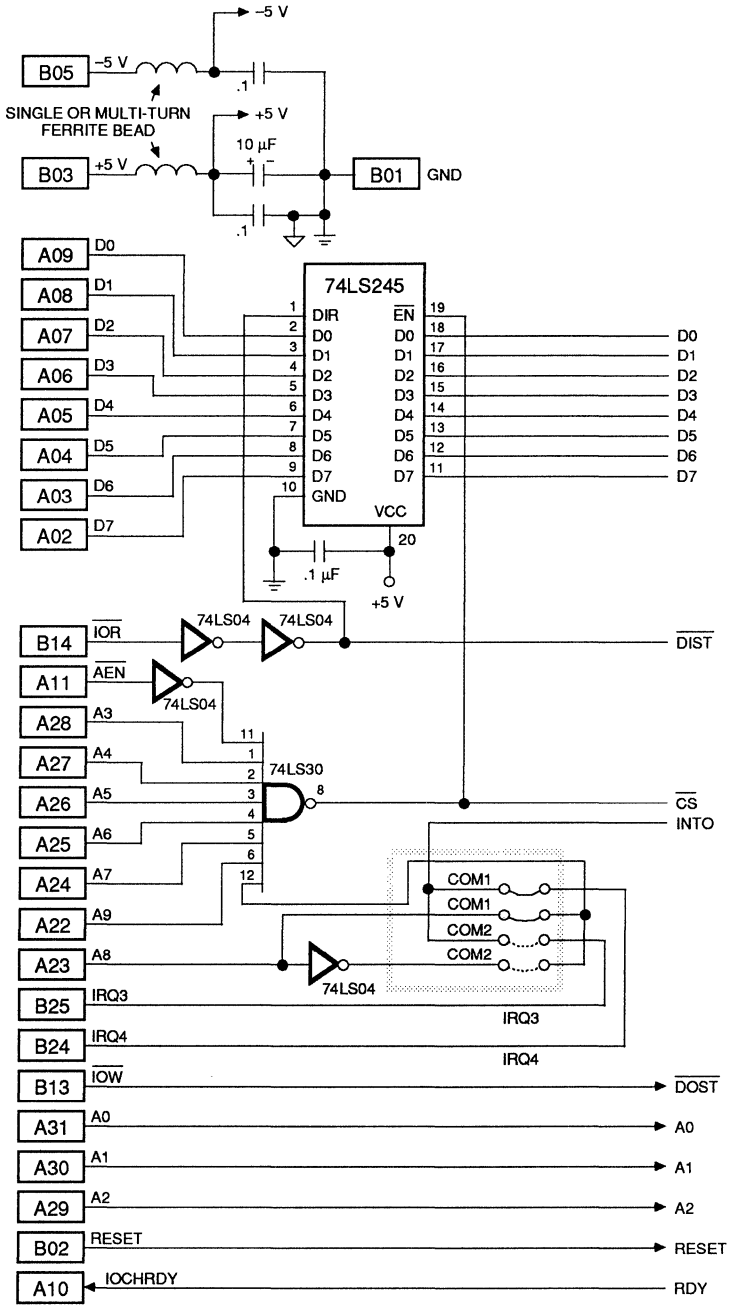


Figure 9. IBM PC/XT/AT Compatible Computer Bus Interface for SC11011 Controller of Figure 6.

APPLICATIONS INFORMATION (Cont.)

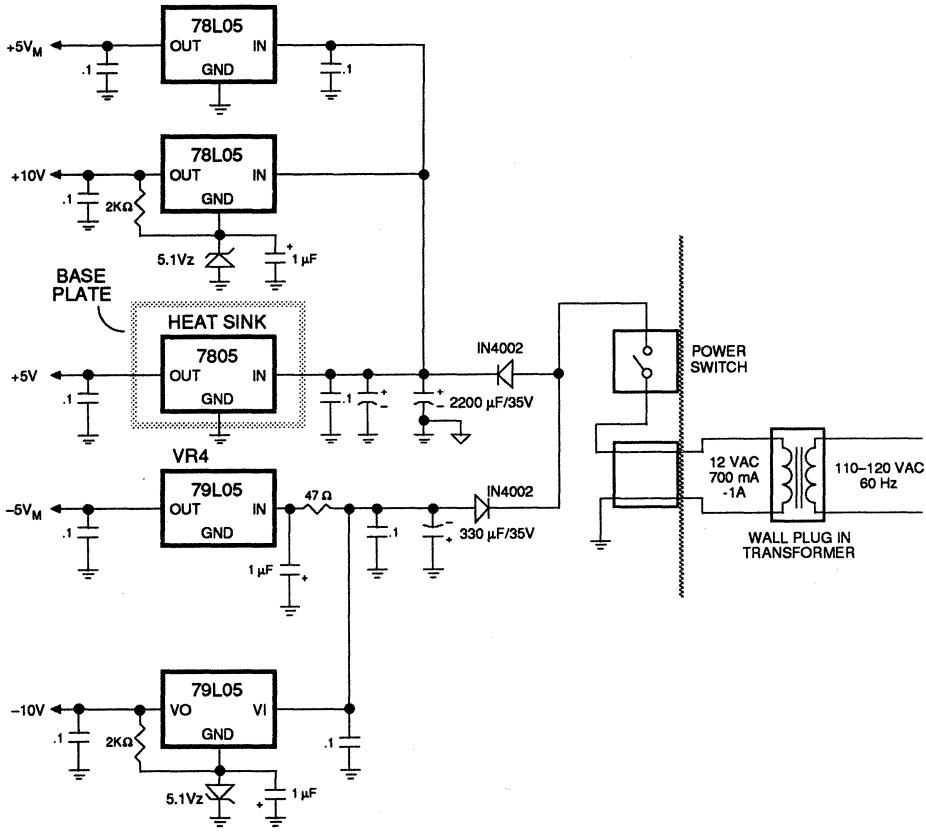
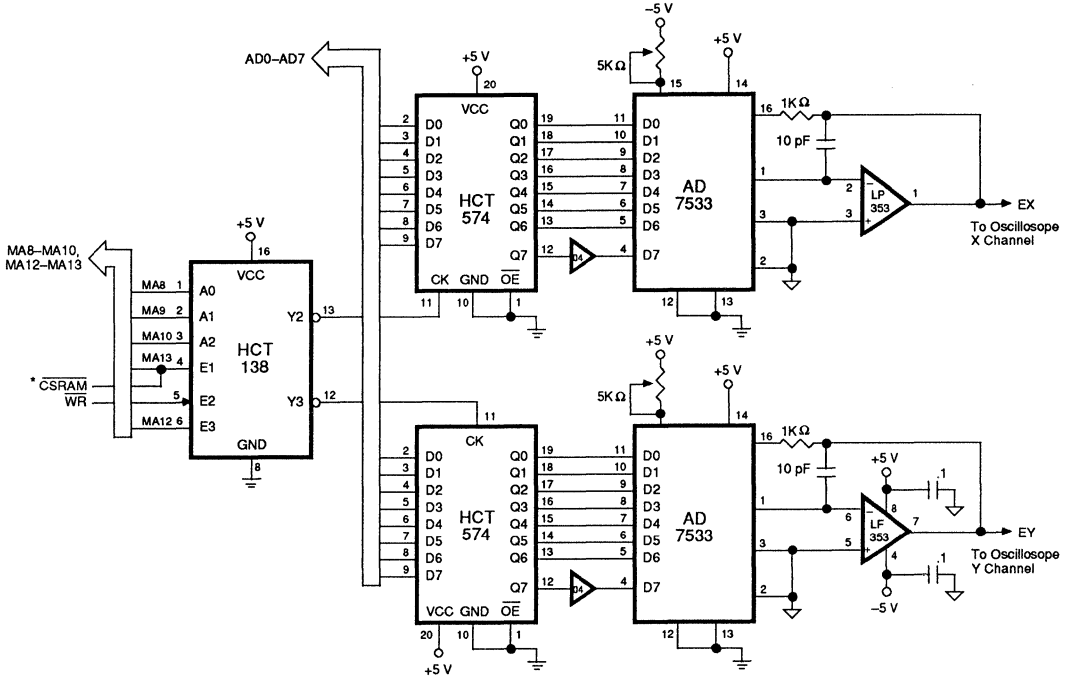


Figure 10. A Typical Power Supply for Stand-Alone Modem Application.



*IF THE SC11011, SC11019 FAMILY IS USED, CONNECT $\overline{\text{CSRAM}}$, IF AN 8096 IS USED, CONNECT MA13.

Figure 11. Test Circuit to Generate "Eye Pattern".

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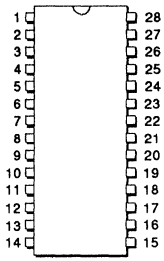
FEATURES

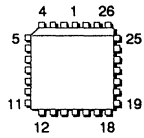
- ☐ Complete 2400 bps modem and 9600/7200/4800/2400 bps Sendfax
- ☐ Single 5V supply with 10 mW power down mode
- ☐ Pin compatible with Sierra SC11024 2400 bps modem
- ☐ Compatible with CCITT V.29, V.27ter, V.22 bis, V.22, V.21, and BELL 212A and 103 standards
- ☐ Integrated DTMF/Guard tone generator, call progress monitor
- ☐ 2100/2225 Hz tone detector
- ☐ Contains an on-chip hybrid
- ☐ Analog, digital, and remote digital loopback
- ☐ Compatible with SC11011, SC11021, SC11061, SC11074, SC11075 and SC11091 controllers
- ☐ Programmable audio output
- ☐ CMOS technology
- ☐ Synchronous & Asynchronous modes
- ☐ EIA 2188 Class 2 compatible firmware available

28-PIN DIP PACKAGE



SC11054CN

28-PIN PLCC PACKAGE

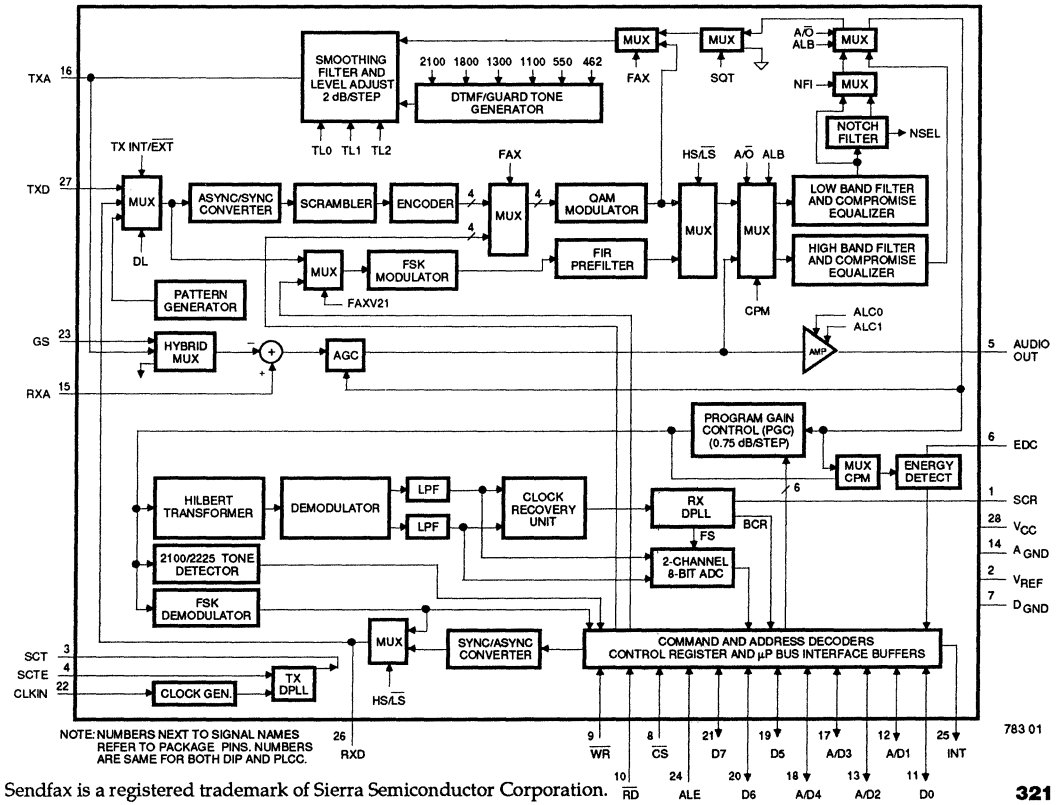


SC11054CV

GENERAL DESCRIPTION

The SC11054 is a complete 2400 bps, 5V only modem IC including a Sendfax capability up to 9600 bps. This IC contains all modem functions except the adaptive equalizer. It is used in conjunction with an external controller, such as the Sierra SC11011 (for either parallel bus or RS-232 applications) and memory to implement a 2400 bps full duplex modem, compatible with the CCITT V.22 bis recommendation, having Sendfax capability at 9600/7200 bps compatible with the V.29 recommendation or 4800/

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS. NUMBERS ARE SAME FOR BOTH DIP AND PLCC.

GENERAL DESCRIPTION (cont)

2400 bps compatible with V.27ter recommendation. The controller performs all modem control and handshaking functions including the Sendfax call set-up in accordance with T.30 recommendation as well as the adaptive equalization.

The SC11054 operates in 2400 bps QPSK/QAM and 1200 bps PSK as well as 0 to 300 baud FSK modes, compatible with Bell 103 and 212A as well as CCITT V.21, V.22, and V.22 bis standards. In addition the SC11054 can transmit 9600 bps QAM with fall back to 7200 bps per V.29 standard or 4800 bps PSK with fall back to 2400 bps compatible with V.27ter recommendation. When used with the SC11011 controller, the SC11054 becomes an intelligent modem controlled by the industry standard "AT" command set with the added Sendfax capability up to 9600 BPS. The interface between the SC11054 modem and the controller is a standard microcontroller interface that easily connects to the SC22201 (128 by 8) EEPROM memory for permanent storage of configuration settings and phone numbers.

The SC11054 may be used with several controllers. Currently they are:

CONTROLLER	APPLICATION
SC11101	General purpose; most economical
SC11021	For low power applications; < 50 mW standby and supports a serial EEPROM
SC11061	For MNP2-5 applications; operates with a 29.412 MHz crystal for greater processing. Most economical choice for MNP2-5 applications.
SC11074	5 V supply, < 30 mW standby, smallest footprint, best choice for stand alone, RS232 pocket modem applications
SC11075	Same as SC11074 except for internal parallel applications. Laptop applications.
SC11091	5 V supply, < 40 mW standby, lowparts count, MNP5, V.42bis. Most versatile controller offered.

FUNCTIONAL DESCRIPTION OF THE SC11054 MODEM

The SC11054 includes the following (See Block Diagram, Figure 1):

- ☐ Full transmitter consisting of
  - – Async to Sync converter
  - – Scrambler
  - – Data encoder
  - – 75% square root of raised cosine pulse shaper in V.22 mode, 50/90% square root of raised cosine shaping in V.27 4800/2400 bps modes and 20% square root of raised cosine shaping in V.29 9600/7200 bps modes
  - – Quadrature amplitude and phase modulators
  - – FSK (Bell 103 and CCITT V.21) modulator
  - – Hybrid
- ☐ High band and low band filters
- ☐ High band and low band compromise equalizers
- ☐ V.22 notch filter (selectable at 550 or 1800 Hz)
- ☐ Transmit smoothing filter
- ☐ Programmable attenuator for transmit level adjust
- ☐ DTMF, 462 Hz, 550 Hz, 1100 Hz, 1300 Hz, 1800 Hz, and 2100 Hz tone generator
- ☐ Tone detector for 2100/2225 Hz frequencies
- ☐ Transmit clock circuit for synchronous operation (slave, external, and internal modes)
- ☐ Pattern generator for generating fixed digital patterns in handshaking mode
- ☐ Receive section consisting of
  - – 64-step programmable gain controller (PGC)
  - – Energy detector at the output of the PGC
  - – Hilbert transformer
  - – Quadrature amplitude and phase demodulators (free running carrier) with low pass filters
  - – Baud timing recovery circuit (sampling clock of 600 Hz)
  - – FSK demodulator
  - – Sync to Async converter
- ☐ Two channel 8-bit analog to digital converter (ADC)
- ☐ Control and Status registers
- ☐ 8-bit microprocessor interface with interrupt and multiplexed address/data lines
- ☐ Audio output with level adjust

Transmitter (V.22bis, V.22, 212A and V.21 and 103)

Since data terminals and computers may not have the timing accuracy required for 2400/1200 bps transmission (0.01%), timing correction on the incoming data stream must be made. The async/sync converter accepts asynchronous serial data clocked at a rate between 2400/1200 Hz +2.3%, –2.5%. It outputs serial data at a fixed rate of 2400/1200 Hz ±0.01% derived from the master clock oscillator. To compensate for the input and output rate differences, a stop bit is either deleted or inserted when necessary. If the input data rate is slower than the output data rate, a stop bit is inserted. If the input data rate is faster than the output data rate, a stop bit is deleted. The output of the async/sync converter is applied to the scrambler.

The scrambler is a 17-bit shift register clocked at 2400/1200 Hz. Outputs from the 14th and 17th stages are exclusive OR'd and further exclusive OR'd with the input data. The resultant data is applied to the D input of the shift register. Outputs from the first four/two stages of the shift register form the quad/dibit that is applied to the QAM/QPSK modulator. The purpose of the scrambler is to randomize data so that the energy of the modulated carrier is spread over the band of interest—either the high band, centered at 2400 Hz, or the low band, centered at 1200 Hz.

In the 2400 bps mode, the modem actually sends four bits at a time, called a quadbit. The actual rate of transmission for a quadbit is 600 baud. This is the optimum rate of transmission over the general switched telephone network for a full duplex FDM (frequency division multiplexing) modem because band limit filters in the central office cut off at about 3000 Hz.

In the 2400 bps data rate, the data to be transmitted is divided into groups of four consecutive bits (quadbits). The first two bits of the quadbit are encoded as a phase quadrant change relative to the quadrant occupied by the preceding signal element. The last two bits define one of the four signaling elements associated with the new quadrant.

In the 1200 bps data rate, the data stream is divided into groups of two consecutive bits (dibits). The dibits are used to determine the phase quadrant change relative to the quadrant occupied by the preceding signal element. The resulting signaling elements from the inphase (I) and quadrature (Q) channels are passed through baseband filters with a square root of raised cosine shape. The filtered signals subsequently modulate sine and cosine carriers, and add to form the QAM/QPSK signal. The

monitor mode, the low-band filter is scaled down by a factor of 2.5 to center it over a frequency range of 300 to 660 Hz. Thus, during call establishment in the originate mode, call progress tones can be monitored through the scaled low-band filter and the modem answer tone or voice can be monitored through the unscaled high-band filter.

The low-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 1200 Hz. In the originate mode, this filter is used in the transmit direction; in the answer mode, it is used in the receive direction. When analog loopback is used in the originate mode, this filter, together with the low-band delay equalizer, is in the test loop.

The low-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the low-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band.

The high-band filter is a 10th order switched-capacitor band-pass filter with a center frequency of 2400 Hz. In the answer mode, this filter is used in the transmit direction; in the originate mode, it is used in the receive direction. When analog loopback is used in the answer mode, this filter, together with the high-band delay equalizer, will be in the test loop.

The high-band delay equalizer is a 10th order switched-capacitor all-pass filter that compensates for the group delay variation of the high-band filter and half of the compromise line characteristics, producing a flat delay response within the pass-band. The transmit smoothing filter is a second-order low-pass switched-capacitor filter that adds the modem transmit signal to the V.22 guard tones. It also provides a 2 dB per step programmable gain function to set the output level.

Transmitter (V.29 and V.27ter)

In these modes the functions required to convert the transmit data to transmit analog signal are partitioned between the analog and controller chips. The firmware implemented in the controller chip performs the scrambling and also generates the training sequences as required by the V.29 and V.27ter specifications. Next, it carries out the encoding function based on the selected mode and bit rate (9600/7200/4800/2400 bps) and determines the new location of the constellation point. A 4-bit word (a_3 a_2 a_1 a_0) has been assigned to each constellation point to facilitate the quadrature modulation by the analog chip. (See figures 2a and b).

Every two baud periods (2400/1600/1200 bauds), the analog chip sends an interrupt to the controller, within 250 µs, the controller has to write an 8-bit word into the FAXR register of the analog chip, that conveys the constellation point locations for two consecutive bauds (8-bit word corresponds to 8-bits of Tx data in 9600 bps mode, 6 bits in 7200 bps mode, 6 bits in 4800 bps mode and 4 bits in 2400 bps mode).

The analog chip will perform quadrature modulation on the 4 LSB's first and 4 MSB's on the next baud period. It also caries out square root of raised cosine shaping based on the selected baud rate. In fax mode (V.29, V.27ter) the modulated signal will directly feed the transmit smoothing filter, bypassing the band pass filter and equalizer.

Transmitter (V.21 FAX)

In FAX mode (BR3 =1 or BR2 =1) the operation of V.21 modem, referred to as V.21FAX, is half-duplex and uses the high channel.

The input/output data will be handled through the controller interface instead of the TXD/RXD pins.When transmitting in V.21 mode, the analog chip sends interrupts to the controller at a 300 Hz ±.01% rate which serves as a timing base. Within 2 ms after every eight interrupts, the controller has to

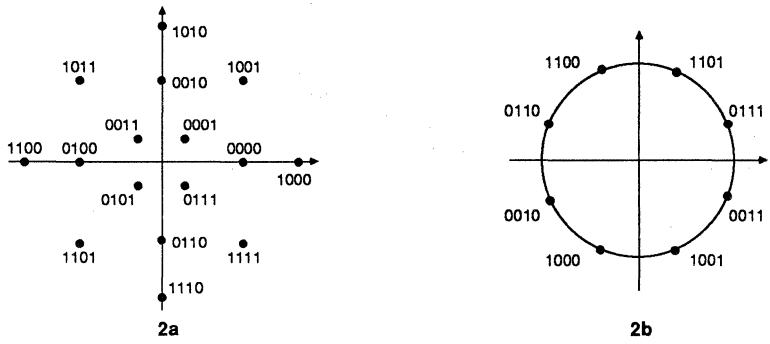


Figure 1. 4-Bit Words ($a_3a_2a_1a_0$) Identifying Constellation Points in V.29 (2a) and V.27ter (2b)

write an 8-bit word into the FAXR register that corresponds to eight consecutive transmit data bits with the LSB to be sent first.

The analog chip will perform a parallel-to serial conversion on the 8-bit word and feed the result into the FSK modulator block. The signal path from FSK modulator input to TXA pin will be similar to the normal V.21 mode.

Receiver (V.22 bis, V.22, 212A, V.21 and 103)

The receiver section consists of an energy detector, programmable gain control (PGC), part of the QAM/QPSK demodulator, FSK demodulator, 8-bit ADC and sync/async converter.

The received signal is routed through the appropriate band-pass filter and applied to the energy detector and PGC circuit. The energy detector provides detection within 17 to 24 msec. It is set to turn on when the signal exceeds –43 dBm and turn off when the signal falls below –48 dBm measured at the chip. A 2 dB minimum hysteresis is provided between the turn on and turn off levels. In call progress mode, the energy detector is connected to the output of the PGC to allow detection level adjustment.

The output of the receive filter is applied to the programmable gain control (PGC). This circuit has a wide overall range of 47.25 dB and provides 64 steps of 0.75 dB/step. The PGC gain is controlled by the external processor. It also provides auto-zeroing to minimize the output DC offset voltage.

The QAM/QPSK demodulator uses a coherent demodulation technique. Output of the programmable gain control (PGC) is applied to a Hilbert transformer that produces an in-phase and 90° out of phase component. These components are then demodulated to baseband in a mixer stage where individual components are multiplied by a free-running carrier. The baseband components are low-pass filtered to produce I and Q (Inphase and Quadrature) channel outputs. The I and Q channel outputs are both filtered by 300 Hz band-pass filters. Then they are rectified, summed and passed through a band-pass filter giving a 600 Hz signal. This signal is applied to a digital phase lock loop (DPLL) to produce a baud rate clock. Using the recovered clock signal, the I and Q channels are sampled and digitized into 8-bit samples by the ADC. Each channel (I and Q) is sampled twice during a baud period, once at the middle and once at the end of the baud period, allowing T/2 or T sampling operation. The external processor is interrupted once every baud period (1.667 msec). The processor should read the I and Q samples (within 100 µs from the time interrupt is issued), and perform adaptive equalization, carrier phase tracking, data decoding, and data descrambling. One quad/dibit is transferred from the SC11054 during each baud period.

In the asynchronous mode, data received from the processor is applied to the sync/async converter to reconstruct the originally transmitted asynchronous data. For data which had stop bits deleted at the transmitter (overspeed data), these stop bits are re-inserted. Underspeed data is passed essentially unchanged. The sync/async converter has two modes of operation. In the basic signaling mode, the buffer can accept an overspeed which corresponds to one missing stop bit in eight characters. The length of the start bit and data elements will be the same, and the stop bit will be reduced by 12.5%. In the extended-signaling range, the buffer can accept one missing stop bit in four characters and the stop bits will be reduced by 25% to allow for overspeed in the transmitting terminal. Output of the sync/async converter, along with the output of the FSK demodulator, is applied to a multiplexer. The multiplexer selects the appropriate output, depending on the operating speed and output data received on the RXD pin.

For low-speed operation, the FSK demodulator is used. The output of the PGC amplifier is passed through a zero crossing detector and applied to a counter that is reset on zero crossings. The counter is designed to cycle at a rate 4 times faster than the carrier signal. The counter output is low-pass filtered and hard limited to generate FSK data.

To improve the performance of the receiver at low signal levels, while maintaining a wide amplitude range, a 1-bit AGC circuit is placed prior to the band-pass filter. The decision thresholds of this AGC are controlled by the AGCVT bit. When AGCVT = 1, the thresholds will be 6 dB further apart than when AGCVT = 0, so that the probability of gain change will be reduced. The status of the AGC gain is available through the AGCO bit. AGC will have 8 dB more gain when AGCO = 1. Status of AGCO should be monitored at every baud timing period and when it makes a transition (causing a gain-hit) the PGC's gain shouldbe modified accordingly to prevent divergence of the adaptive equalizer.

Receiver (V.21 FAX)

When receiving in V.21FAX mode, which is half-duplex, the serial output data from FSK demodulator will be loaded into a serial-to-parallel register. The timing for serial shift as well as interrupt is derived from the received data through a resettable counter. The counter divides an input clock of 9.6 kHz by 32 to generate a 300 Hz signal. On every high to low transition of data the counter is reset and resynchronized to data timing. Assuming a received bit rate of 300 BPS ±0.01%, the interrupt should have an aver-

age frequency of 300 Hz ±.01%. The controller should count the interrupt pulses and read the contents of FAXV21R register within 1.5 ms after every eighth pulse. The LSB corresponds to FSK demodulator output that has been received first in time.

A flag detector is implemented on the chip to facilitate detection of flag sequences (Hex 7E) in V.21 FAX mode. The decoder, detects the flag itself or possible rotations of it; i.e. it detects 01111110, 00111111, 1001111, 11001111, 11100111, 11110011, 11111100. If any of these combinations is detected, then FLAGDET bit of the status register will go high and stay high until the condition goes away. The flag detector output is updated on every interrupt pulse in the V.21FAX receive mode. To ensure that the flag detector is not triggered by false data, it is recommended that the FLAGDET bit be checked for at least 16 consectutive interrupts after this bit gets set. If it does not stay high continuously the received data may not be a true flag sequence. Flag detector should be used in V.21FAX receive mode only.

Tone Detector

A digital tone detector has been implemented in the SC11054 to facilitate detection of 2100/2225 Hz tones. The output of the PGC is passed through a zero crossing detector which in turn feeds a digital timer that verifies the period of the tone. If four consecutive periods of input tone pass the requirements, then, the appropriate tone detector output (TD2100 or TD2225 bit in status register) goes high. To detect these tones user must insert the highband filter in the receive path to allow their passage, also, PGC gain must be set properly to amplify the input to the tone detector. It will be a good practice to monitor ED bit when reading TD to ensure that the signal energy is within acceptable limits.

With the PGC gain word (PGCR) set to 011111 the tone detector threshold will be typically -43dBm.

Hybrid

The signal on the phone line is the sum of the transmit and receive signals. The hybrid subtracts the transmitted signal from the signal on the line to form the received signal. It is important to match the hybrid impedance as closely as possible to the telephone line to produce only the received signal. When the internal hybrid is used, by turning the "Hybrid" code on through the interface, this matching is provided by an external resistor connected between the TXA and RXA pins on the SC11054. The filter section provides sufficient attenuation of the out-of-band signals to eliminate leftover transmit signals from the received signal. The hybrid also acts as a first order low-pass antialiasing filter. The hybrid can be deactivated by the controller.

The SC11054 internal hybrid is intended to simplify the phone line interface. The internal hybrid can compensate for the loss in the line coupling transformer used in the DAA. By tying the GS pin to AGND, V_{REF} or V_{CC}, compensation levels of 0, +2, +3 dB, respectively are provided.

With a higher loss transformer, some degradation in performance at lower signal levels will occur. Specifically, the bit error rate, when operating at receive signal levels below –40 dBm in the presence of noise, will be higher. The energy detect on/off levels measured at the line will also be different from those specified at the chip. An external hybrid circuit, shown in Figure 2, can be used to overcome these losses and achieve maximum performance. In this case, the internal hybrid must be turned off by setting bit 6 of the TXCR register to 0.

The external hybrid circuit uses two operational amplifiers, one in the transmit path and the other in the receive path. The SC11054 internal transmit stage provides a gain of 6 dB over the transmit signal level desired at the line. Under ideal conditions, with no loss in the transformer and perfect line matching, the signal level at the line will then be the desired value. In practice, however, there is impedance mismatch and a loss in the coupling transformer. Therefore, it may be desired to provide a gain in the transmit and receive paths to overcome the loss. The receive gain (G_R) and transmit gain (G_T) are set by the ratios of resistors R2, R1 and R6, R5, respectively (Figure 2).

The circuit can be analyzed as follows:

$$V_R = -\frac{R2}{R1}(V_{TR}) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)V_y$$

$$V_y = -\frac{R6}{R5}V_x$$

If R6/R5 is chosen to equal the loss in the transformer, it can be assumed that V_y is twice as high as V_{TX} (transmit portion of the total line signal). Since $V_{TR} = V_{TX} + V_{RX}$ and $V_y = 2V_{TX}$,

$$V_R = -\frac{R2}{R1}(V_{TX}+V_{RX}) + \left(1+\frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)2V_{TX}$$

$$= -\frac{R2}{R1}V_{RX} + \left[\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) - \frac{R2}{R1}\right]V_{TX}$$

To eliminate any transmit signal from appearing at the received signal input, the second term in the above equation must be set to zero, giving:

$$\left(1+\frac{R2}{R1}\right)\left(\frac{2R4}{R3+R4}\right) = \frac{R2}{R1}$$

Solving for R3/R4:

$$\frac{R3}{R4} = 1 + \frac{2R1}{R2}$$

Additionally,

$$G_R = \frac{R2}{R1} \text{ and } G_T = \frac{R6}{R5}$$

These equations can be solved to select component values that meet the desired requirements. For example, if the transmit and receive

loss in the coupling transformer is 2.5 dB, then:

$$\frac{R2}{R1} = \text{INV Log}\left(\frac{G_{RdB}}{20}\right) = \text{INV Log}\left(\frac{2.5}{20}\right) = 1.333$$

Similarly, $\frac{R6}{R5} = 1.333$ and $\frac{R3}{R4} = 2.5$

Some typical values are:

R1=20KΩ, R2=27KΩ, R3=13KΩ, R4= 5.1KΩ, R5=20KΩ, and R6=27KΩ

It should be noted that the transmit amplifier is only needed to overcome the loss in line coupling. It can be eliminated since the transmit signal level specification is typically stated as a maximum. Amplifier B, resistors R5 and R6, and capacitor C1 can be eliminated, and point X can be connected to point Y in the circuit of Figure 2 to achieve a more cost effective external hybrid arrangement.

The SC11054 with the internal hybrid may also be used on a 4-wire system where the transmit and receive signals are kept separate. In this mode, the "Hybrid" code must be turned off. The transmit signal is connected to a 600 Ω line transformer through a 600 Ω resistor.

Tone Generator

The tone generator section consists of a DTMF generator, V.22 guard-tone, and 1300 and 2100 Hz tone generators. The DTMF generator produces all of the tones corresponding to digits 0 through 9 and A, B, C, D, *, and # keys. The V.22 guard-tone generator produces either 550 Hz or 1800 Hz. Selection of either the 550 Hz or 1800 Hz tone will cascade the corresponding notch filter with the low-band filter. The tones are selected by applying appropriate codes through the tone control register. Before a tone can be generated, tone mode must be selected. Facility is also provided to generate single tones corresponding to 1300, 1100, 464 and 2100 Hz and the individual rows or columns of the DTMF signal.

Audio Output Stage

A programmable attenuator that can drive a load impedance of 50K Ohms is provided to allow monitoring of the received line signal through an external speaker. The attenuator is connected to the output of the hybrid. Four levels of attenuation—no attenuation, 6 dB attenuation, 12 dB attenuation, and squelch are provided through the ALC1 and ALC0 audio output level control codes. Output of the attenuator is available on the audio output pin where an external audio amplifier (LM386 type) can be connected to drive a low impedance speaker. The output can directly drive a high impedance transducer, but the volume level will be low.

Clock Input

CLKIN (Pin 22) of the SC11054 should be connected to a 9.8304 MHz clock source with an accuracy of ±0.01%.

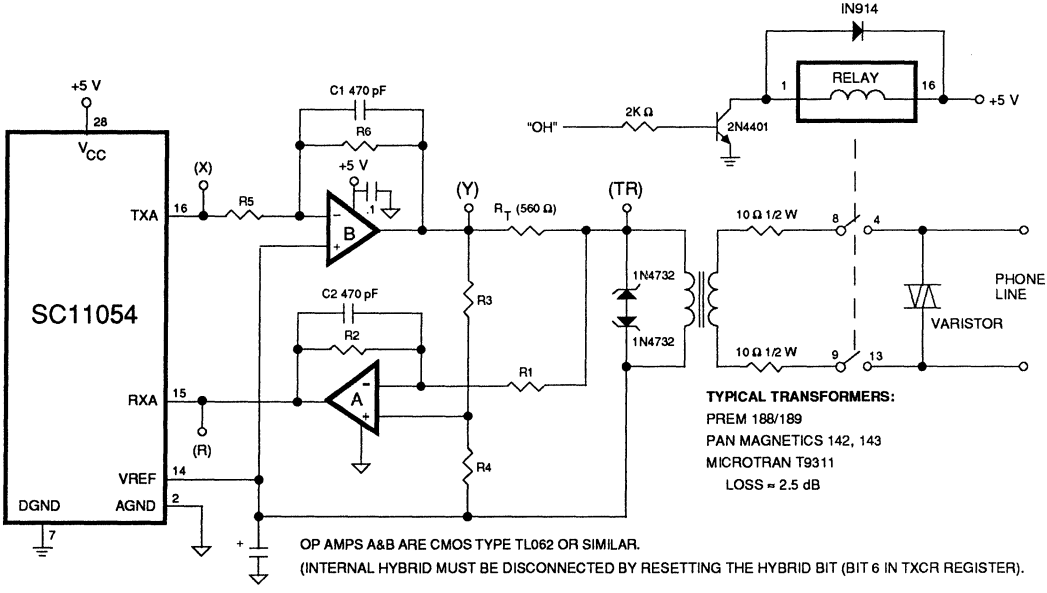


Figure 2. Using an External Hybrid with the SC11054

FUNCTIONAL DESCRIPTION OF THE SC11011 CONTROLLER

The SC11011 modem controller, implemented in Sierra's CMOS process, was designed specifically to handle all of the modem control functions, as well as the interface to a system bus or an RS-232 serial interface. Besides including a 16-bit microprocessor, 8k by 8 bytes of ROM and 128 by 8 bytes of RAM, it also contains the functionality of a 82C50B UART, greatly simplifying the interface to a parallel system bus, such as the one used in IBM's PC. In fact, a complete, Hayes compatible modem with Sendfax capability for the PC consists of the SC11011 controller with external memory, the SC11054 modem and the DAA. All of the popular communications software written for the PC will work with the SC11054/SC11011 set.

The SC11011 can be configured for RS-232 applications. The difference is that the UART is wired so that the serial data from the RS-232 port is converted to parallel data handled by the internal processor. Pins are provided for connecting the familiar switches and indicator lamps found on most stand-alone modems, although the switches and lamps are not needed for operation—all of the switch settings can be done through software.

The controller receives an 8-bit signal sample from the SC11054 and performs adaptive equalization, carrier phase recovery, data decode, and descrambling. The controller is configured for parallel or serial applications by the firmware. The controller is designed by using a 16-bit 2900 processor to perform the digital signal processing and the control functions. Its instruction set is a subset of the Intel 8096 instruction set, but operates faster than the 8096.

The SC11011 provides a standard 5V logic level interface—RS-232 drivers are required to interface to the port. Firmware for external memory is available for the SC11054. It includes the Hayes "AT" command set, and T.30 protocol. When used with the SC11011 controller, it emulates a Hayes-type stand-alone or internal modem with Sendfax.

The SC11011 is available in a 68 pin PLCC. The 68 pin package allows the controller to access external ROM of up to 32K bytes and external RAM of up to 16K bytes. This allows users to customize their own software, and provides a means for software development. The serial controller can talk to both an SC11054 and an SC22201 (EERAM).

The SC11011 requires a single +5 V power supply. Besides the interface for the SC11054 modem, when the SC11011 controller is used for internal applications, it has an eight-bit data port, three address lines, a chip select input, an interrupt line, and the DOST and DIST control lines found in the 82C50B UART. It also has control lines for ring indication, the off-hook relay, and a data/voice relay; these lines connect to the DAA.

When used in RS-232 applications the SC11011's, eight-bit port becomes the switch input lines, and the address, chip select, INTO, DIST and DOST lines become the lines for the RS-232 interface, and modem status. These lines are also used to drive the LEDs. Internally, all of these lines are treated as programmable I/O ports under software control.

The interface to the SC11054 is via an 8-bit address/data bus and the control lines for read and write. The same interface is used for access to an electrical erasable random access memory (SC22201). There are six clock multiplexed address/data bus cycles. A ready signal is provided for the interface to a high speed PC-AT type bus cycle. The 68 pin package, has 15 extra address lines and chip selects for external ROM and external RAM interfaces.

The SC11011 is truly an ASIC DSP & controller—it is designed to control a modem or other peripheral that operates at a moderately slow data rate up to 2400 bits per second. What's unique about the SC11011, for example, is that it allows a slow peripheral to interface to a high speed bus without making the main processor add unnecessary wait states.

This is done through the UART interface and the on-chip registers which look somewhat like dual port registers. The main processor can write to and read from them at will, while the on-chip controller can do the same. The controller was designed this way because most communications software has to have unrestrained access to the UART registers. To make the SC11011 compatible with this software, the registers were included.

The internal processor monitors the registers to determine the mode of operation—command mode or data mode; at power-up, it is automatically put in the command mode and it looks for instructions. Once carrier is detected, it goes into the data mode, and stays there until an escape sequence is entered, just like a Hayes-type modem. The escape sequence is three + signs—+++ —in the default mode, but it can be changed in the software.

The actual processor contains a 16-bit data path and can execute 54 instructions with three different addressing modes: direct, indirect, and immediate. There is 8K by 8 of ROM on the chip for program storage.

To the system bus, the SC11011 looks and acts like an 8250B UART. Communications software written for this UART will work with the SC11011.

THE SC11054 & SC11011 SYSTEM

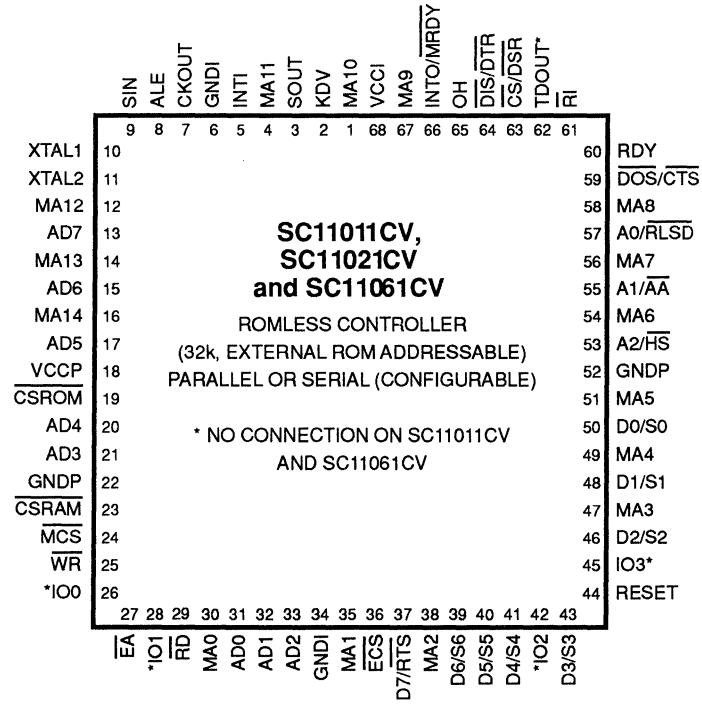
The only external components required by the SC11054 are a 600 Ohm line matching resistor and a 1.0 μF capacitor from the EDC pin to ground. That's all! If it is desired to drive a speaker to monitor the line, an amplifier like the LM386 can be added, but the output provided on the SC11054 can directly drive a high impedance (50 kΩ) earphone-type transducer.

The SC11054 modem's CLKIN pin line is driven by the SC11011 CKOUT line at 9.8304 MHz. The SC11011 interfaces to an IBM PC bus. The only external parts will be a 74LS245 bus interface and an 8 input NAND gate for COM1 and COM2 decoding. A ready signal is provided to control the IOCHRDY pin on the bus to allow operation with higher speed computers (AT, XT TURBO, etc.)

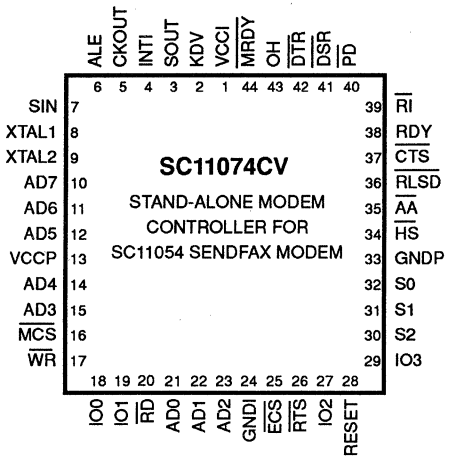
For tone dialing, the controller sends a code to the modem chip which in turn puts out the called for DTMF tone on the line via the on-chip DTMF generator. For pulse dialing, the controller pulses the OH (off-hook) relay. Both dialing modes work with the built-in call progress algorithm so they won't start dialing until a dial tone is detected.

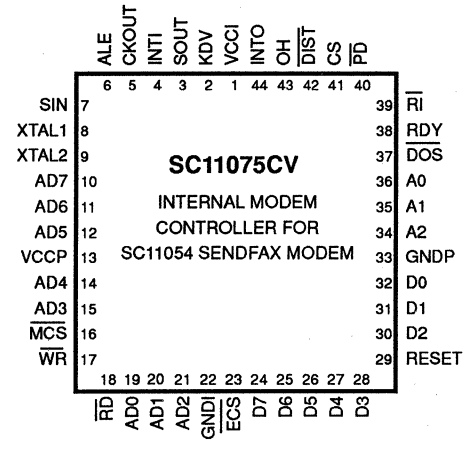
V.22 and V.22bis also call for guard tones to be sent along with the data. In most of Europe the tone is 1800 Hz except in Sweden where 550 Hz is used. The SC11054 modem has the 550 Hz and 1800 Hz tone generators built in as well as the 500 and 1800 Hz notch filter to remove the guard tone in the receiver.

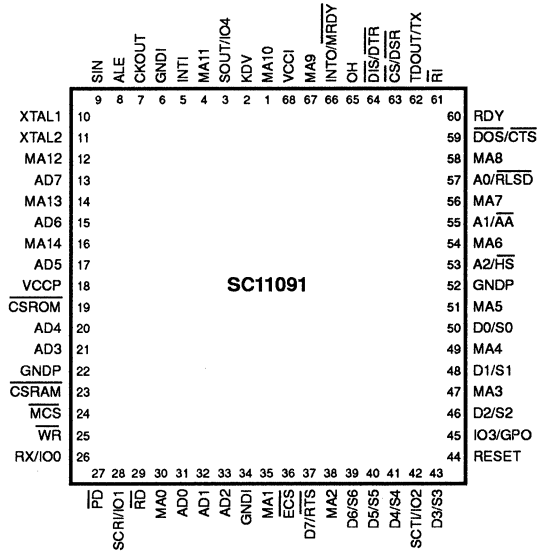
CONNECTION DIAGRAM FOR CONTROLLERS & MODEMS

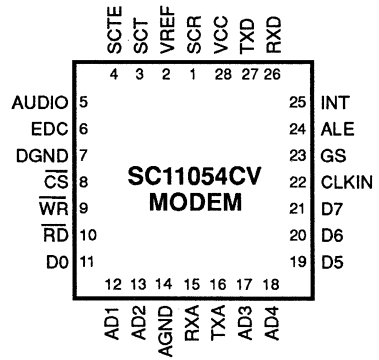


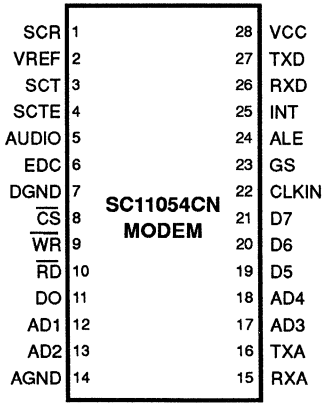
CONNECTION DIAGRAM FOR CONTROLLERS & MODEMS (continued)











PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	SCR	Synchronous Clock Receive (Data set source); Output; TTL; Used only in bit synchronous mode; Recovered by the Receiver Phase Locked Loop from the far end modem. Data on RXD is valid at the rising edge of this clock.
2	V_{REF}	Reference Ground; Generated inside the chip and is equal to $V_{CC}/2$.
3	SCT	Synchronous Clock Transmit (Data set source); Output; TTL; Used only in bit synchronous mode; Generated internally by the SC11024 Clock Generator; Rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
4	SCTE	Synchronous Clock Transmit External (DTE source); Input; TTL; Used only in bit synchronous mode; Data on TXD line is latched by the SC11024 at the rising edge of this clock. Clock rate = 1200 Hz ±0.01% or 2400 Hz ±0.01%.
5	AUDIO	Audio output; The hybrid output is passed through a programmable attenuator and fed to this analog pin. Four different levels can be attained by controlling bit 0 and bit 1 of the AUDIO register as specified under AUDIO register description.
6	EDC	Capacitor for energy detect; A 1.0 µF capacitor should be connected between this pin and AGND.
7	DGND	Digital ground
8	$\overline{CS}$	Chip Select; Input; TTL; Active low.
9	$\overline{WR}$	Write; Input; TTL; Normally high; Data on AD7–AD0 is written into the SC11024 registers at the rising edge of this pulse.
10	$\overline{RD}$	Read; Input; TTL; Normally high; Data on AD7–AD0 is to be read by the processor at the rising edge of this pulse.
12,13,17,18	AD1–AD4	Multiplexed address/data bus (8-bits); Input/Output; TTL; A/D4–A/D1 (4-bits) are used for multiplexed addressing of internal registers.
14	AGND	Analog Ground
15	RXA	Receive analog; Input
16	TXA	Transmit analog; Output
11,19–21	D0, D5–D7	Bits 0, 5, 6 and 7 are don't cares as far as address is concerned.
22	CLKIN	Clock input; 9.8304 MHz clock input from the controller.
23	GS	Gain Select to compensate for loss in line coupling transformer. When left open or tied to AGND, the compensation is 0 dB; connected to VREF, +2 dB compensation is provided; And when tied to V_{CC}, the compensation is +3 dB.
24	ALE	Address Latch Enable; Input; TTL; The address on A/D4–A/D1 is latched into the SC11054 Address decoder at the falling edge of this normally low pulse.
25	INT	Interrupt; Output; TTL; Normally low; A short (13 µs typical) positive pulse is generated after all A to D conversions are completed.
26	RXD	Received Data; Output; TTL
27	TXD	Transmit Data; Input; TTL
28	V_{CC}	+5 V supply

REGISTERS

There are fourteen 8-bit registers interfacing to the microprocessor bus. Six of these registers can only be read by the processor (called READ registers) and the remaining eight can be written into by the processor (called CONTROL registers). Bit 1 of the "Tone" register can be read and written by the processor, Table 1 shows the address and bit assignments for these registers.

A chip select pin is provided for multi-peripheral addressing by the processor.

Table 1. READ Registers

ADDRESS BITS				NAME	MSB			BIT NUMBER				LSB
A4	A3	A2	A1		7	6	5	4	3	2	1	0
0	0	0	0	Q1	Q17	Q16	Q15	Q14	Q13	Q12	Q11	Q10
0	0	0	1	I1	I17	I16	I15	I14	I13	I12	I11	I10
0	0	1	0	Q2	Q27	Q26	Q25	Q24	Q23	Q22	Q21	Q20
0	0	1	1	I2	I27	I26	I25	I24	I23	I22	I21	I20
0	1	0	0	Status	X	X	FLAGDET	AGCO	TD2100	TD2225	FSKD	ED
0	1	0	1	FAXV21R	R7	R6	R5	R4	R3	R2	R1	R0
0	1	X	1	Unused		Unused						
0	1	1	X	Unused		Unused						

STATUS Register: Address (A4–A1) = 0100

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–6	Unused	
Bits 5	FLAGDET	Flag Sequence detector output. When set, flag sequence is present in V.21FAX mode.
Bit 4	AGCO	Status of internal 1-bit AGC. When this bit is set, RXA signal is amplified by 8 dB before entering the bandpass filters.
Bit 3	TD2100	2100 Hz tone detector output. TD2100=1 when this tone is present.
Bit 2	TD2225	2225 Hz tone detector output. TD2225=1 when this tone is present.
Bit 1	FSKD	Received FSK data. FSKD = 1 when mark is received.
Bit 0	ED	Energy detect circuit output. ED = 1 when energy detected.

Note: When reading unused bits, the corresponding bus lines will not be driven by the SC11054 and will be floating.

FAXV21R Register: Address (A4–A1) = 0101

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–0	R7–R0	In V.21 FAX receive mode this register will be loaded by received data and should be read every eighth interrupt pulse. LSB (R0) corresponds to the data bit received first in time.

Table 1a. READ Registers

Q1 Register:	Stores midbaud inphase sample output of ADC.
I1 Register:	Stores midbaud quadrature sample output of ADC.
Q2 Register:	Stores endbaud inphase sample output of ADC.
I2 Register:	Stores endbaud quadrature sample output of ADC.

Note: All samples are represented in two's complement form.

Table 2. CONTROL Registers

ADDRESS BITS				NAME	BIT NUMBER							
A4	A3	A2	A1		7	6	5	4	3	2	1	0
1	0	0	0	TXCR	BR2	HYBRID	TXSEL2	TXSEL1	TXSEL0	SQT	BR1	BR0
1	0	0	1	MCRA	SLAVE	LCK/$\overline{\text{INT}}$	RNGX	SYNC	WLS1	WLS0	A/$\overline{\text{O}}$	RXMRK
1	0	1	0	MCRB	BR3	PD	TONDETE	CPM	ALB	TL2	TL1	TL0
1	0	1	1	TONE	X	HNDSHK	TONEON	DTMF	D3	D2	D1	D0
1	1	0	0	PGCR	X	AGCVT	G5	G4	G3	G2	G1	G0
1	1	0	1	DATA	X	PLLJAM	PLLFRZ	PLLFAST	RD3	RD2	RD1	RD0
1	1	1	0	AUDIO	X	DISS	PGCZ	TST2	TST1	TST0	ALC1	ALC0
1	1	1	1	FAXR	B7	B6	B5	B4	B3	B2	B1	B0

Transmit Control Register (TXCR): Address (A4–A1) = 1000

(Note: When writing into these registers, the bus lines corresponding to the unused bits are ignored by the SC11054.)

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	BR2	This bit in conjunction with BR3, BR1 and BR0 selects bit rate.
Bit 6	HYBRID	When set, the transmitter output (TXA) is connected to the inverting input of the receive buffer to allow the use of the on-chip hybrid circuit for 2 to 4 wire conversion.
Bit 5 Bit 4 Bit 3	TXSEL2 and TXSEL1 and TXSEL0	Transmit Select bits. These 3 bits determine the data transmitted by the transmitter according to the following table:

TXSEL2	TXSEL1	TXSEL0	TRANSMITTED DATA
0	0	0	External data sent by DTE.
0	0	1	Unscrambled S1 (Note 1).
0	1	0	Unscrambled Space.
0	1	1	Unscrambled Mark.
1	0	0	Scrambled RX. Digital loop back mode (Note 2).
1	0	1	Scrambled Reversals (Notes 3 and 4).
1	1	0	Scrambled Space (Note 4).
1	1	1	Scrambled Mark (Note 4).

Note 1: S1 is a pattern of 0011 transmitted at 1200 bps rate regardless of BR1. If in FSK mode (BR0 = 1), then reversals are sent. This pattern cannot be sent at 2400 bps rate.

Note 2: In this mode, the received data, after being descrambled, is sent back to the scrambler. The modem will automatically go to the Synchronous mode. Slave bit has to be set.

Note 3: Reversals are continuous streams of 01.

Note 4: When in FSK mode (BR0 = 1), TXSEL2 is ignored since scrambling is not applicable.

Bit 2	SQT	When this bit is set, the transmitter is squelched by connecting the output of MUX1 (see the block diagram) to analog ground.
Bit 1 Bit 0	BR1 and BR0	Bit Rate Selection bits based on the following table:

BR3	BR2	BR1	BR0	BIT RATE
0	0	0	0	2400 bps V.22 bis
0	0	1	0	1200 bps V.22/212A
0	0	0	1	0–300 bps Bell 103
0	0	1	1	0–300 bps CCITT V.21
0	1	0	0	4800 bps V.27
0	1	1	0	2400 bps V.27
X	1	0	1	N.A.
1	X	0	1	N.A.
X	1	1	1	0–300 bps V.21 FAX
1	X	1	1	0–300 bps V.21 FAX
1	0	0	0	9600 bps V.29
1	0	1	0	7200 bps V.29
1	1	X	0	N.A.

CONTROL REGISTERS (Cont.)

Mode Control Register A (MCRA): Address (A4–A1) = 1001

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	SLAVE	When set, receiver timing will be used as clock source for transmitter. LCK/INTB and SYNC bits must be high for slave mode
Bit 6	LCK/INTB	Determines the clock source for the transmitter. When this bit is set, the clock source is externally provided on SCTE (pin 4), and when cleared, it is internally generated (SCT). This bit can select the clock source independent of Sync/Async mode selection (see below). When in Digital Loop-Back mode, the clock source will be forced to the Slave mode (SCR).
Bit 5	RNGX	Range extender for the receiver Sync/Async converter. When set, the receiver Sync/Async can insert up to one stop bit per four (8, 9, 10 or 11-bit) characters to compensate for a far end DTE being up to 2.3% over speed. The transmitter Async/Sync always handles this overspeed condition regardless of this bit's condition.
Bit 4	SYNC	When set, operate in bit synchronous mode; when clear, operate in character asynchronous mode. When in Digital Loop-Back mode, the SC11046 will be forced to the Synchronous mode.
Bit 3 and Bit 2	WLS1 and WLS0	Word length select bits in asynchronous mode, according to the following table:

WLS1	WLS0	NUMBER OF BITS PER CHARACTER
1	0	8
1	1	9
0	0	10
0	1	11

Bit 1	A/$\overline{O}$	When set, operate in answer mode; when clear, operate in originate mode.
Bit 0	RXMARK	When set, the RXD pin is clamped to the high logical level.

Mode Control Register B (MCRB): Address (A4–A1) = 1010

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	BR3	This bit in conjunction with BR2–BR0 selects the bit rate.
Bit 6	PD	When this bit is set, chip will be powered down. When cleared normal operation is restored.
Bit 5	TONDETE	When this bit is set, 2100/2225 Hz tone detector will be enabled. However, for proper functioning, highband filter must be set in the receive path to pass these tones. Tone amplification before detection can be set by PGC.
Bit 4	CPM	Call progress monitor mode. When set, the receive path can be connected to the high band filter to detect answer tone (ALB=0) or to the low band filter scaled down 2.5 times (ALB=1) to listen for the call progress tones during auto dialing.
Bit 3	ALB	Analog Loop Back. When set, the transmitter output (TXA) is connected to the receive path, bypassing the receive filter.
Bit 2 and Bit 1 and Bit 0	TL2 and TL1 and TL0	Transmit level adjust bits based. In FAX modes maximum transmit level will be 2 dB lower than modem mode (BR3=BR2=0).

			TRANSMIT LEVEL AT TXA PIN	
TL2	TL1	TL0	MODEM MODE BR3=BR2=0	FAX MODE BR3=1 or BR2=1
0	0	0	–3 dBm	–5 dBm
0	0	1	–5 dBm	–5 dBm
0	1	0	–7 dBm	–7 dBm
0	1	1	–9 dBm	–9 dBm
1	0	0	–11 dBm	–11 dBm
1	0	1	–13 dBm	–13 dBm
1	1	0	–15 dBm	–15 dBm
1	1	1	–17 dBm	–17 dBm

CONTROL REGISTERS (Cont.)

TONE Register: Address (A4–A1) = 1011

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	HNDSHK	This bit is set only during handshaking sequence. When set, both FSK and PSK/QAM demodulators are enabled. When cleared, FSK demodulator is disabled when in high speed mode.
Bit 5	TONEON	When set, the output of the tone generator appears at TXA. When cleared, the output of the tone generator is squelched.
Bit 4	DTMF*	When set, the DTMF generator is turned on. When cleared, the DTMF generator is turned off, but other tones can be generated.
Bits 3–0	D3–D0	Specify the desired tone (see the following table):

DTMF	D3	D2	D1	D0	DIGIT DIALED	TONE OUTPUT	FREQUENCIES (HZ)
1	0	0	0	0	0	941	1336
1	0	0	0	1	1	697	1209
1	0	0	1	0	2	697	1336
1	0	0	1	1	3	697	1477
1	0	1	0	0	4	770	1209
1	0	1	0	1	5	770	1336
1	0	1	1	0	6	770	1477
1	0	1	1	1	7	852	1209
1	1	0	0	0	8	852	1336
1	1	0	0	1	9	852	1477
1	1	0	1	0	*	941	1209
1	1	0	1	1	(A)	697	1633
1	1	1	0	0	(B)	770	1633
1	1	1	0	1	(C)	852	1633
1	1	1	1	0	#	941	1477
1	1	1	1	1	(D)	941	1633
0	0	0	0	0	No tone; tone generator turned off		
0	0	0	0	1	550		
0	0	0	1	0	1800		
0	0	0	1	1	2100		
0	0	1	0	0	1300		
0	0	1	0	1	1100		
0	0	1	1	x	462		
0	1	x	x	x	No tone; tone generator turned off		

Note: TONEON must also be set to generate DTMF signals.

Programmable Gain Controller Register (PGCR): Address (A4–A1) = 1100

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	AGCVT	When set, prevents gain hit due to AGC's gain step. This bit must be set during the handshaking after detecting the four point constellation and before switching to 16-way decision making.
Bits 5–0	G5–G0	Control the gain of the PGC within a range from –10 to +37.5 dB in 0.75 dB steps. (See the following table):

CONTROL REGISTERS (Cont.)

G5	G4	G3	G2	G1	G0	PGC GAIN (dB)
0	0	0	0	0	0	–10.0
0	0	0	0	0	1	–9.25
0	0	0	0	1	0	–8.5
0	0	0	1	0	0	–7.0
0	0	1	0	0	0	–4.0
0	1	0	0	0	0	+2.0
1	0	0	0	0	0	+14.0
1	1	1	1	1	1	+37.25

Note: Signal level is adjusted (before entering the filter) by an internal AGC with +12 dB or 0 dB gain, plus a fixed gain of 5 dB.

DATA Register: Address (A4–A1) = 1101

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	PLLJAM	When this bit is set, the DPLL will be reset by the next rising edge of the received baud clock. This bit must remain high for at least one baud period. It should be cleared by the processor to end the jamming mode. PLLFRZ (see below) overrides PLLJAM when both are enabled.
Bit 5	PLLFRZ	Phase locked loop freeze. When this bit is set, the DPLL begins to run freely regardless of the received baud clock. To re-enable the DPLL locking, the bit must be cleared by the processor. PLLFRZ overrides PLLJAM when both are enabled.
Bit 4	PLLFAST	When set, the DPLL operates in "fast" locking mode. In this mode, the DPLL is updated on every baud period by 13 µs steps. When this bit is cleared (default mode), the DPLL operates in "normal" locking mode and is updated once every 8 baud periods by 6.5 µs steps.
Bit 3–0	RD3–RD0	Four-bit Received Data. Used only in high speed (1200 or 2400 bps) mode, they are descrambled by the processor and shifted out by the SC11054. Sync to Async is also done by the SC11054, when in the asynchronous mode. RD0 is the first bit appearing on the RXD pin, followed by RD1, RD2 and RD3. In the 1200 bps mode, only RD0 and RD1 are shifted out during one baud period.

AUDIO Register: Address (A4–A1) = 1110

BIT NUMBER	BIT NAME	DESCRIPTION
Bit 7	Unused	
Bit 6	DISS	When this bit is set, the scrambler is disabled, when cleared, it is enabled. Transmit select bits (TXSEL0–2) override this bit when in "transmit internal mode"
Bit 5	PGCZ	When set, the output of the PGC is grounded. DC offset of the demodulator can be stored and canceled by the controller.
Bit 4–2	TEST	Test bits used for factory testing. For normal chip operation, these bits must be cleared.
Bit 1	ALC1	Audio level control bit 1.
Bit 0	ALC0	Audio level control bit 0. These two bits are used to control the audio level at AUDIO pin according to the following table:

ALC1	ALC0	AUDIO ATTENUATION (dB)
0	0	Audio off
0	1	12
1	0	6
1	1	0 (no attenuation)

Note: The audio signal may be amplified by 8 dB by the line receiver AGC before being fed to the audio attenuator.

CONTROL REGISTERS (Cont.)

FAX Register: Address (A4–A1) = 1111

BIT NUMBER	BIT NAME	DESCRIPTION
Bits 7–0	B7–B0	In V.27 or V.29 modes, this register has to be loaded at every interrupt with an 8-bit word that identifies constellation points for two consecutive baud periods. 4 LSB's correspond to first baud in time. In V.21FAX mode, when transmitting, the register should be loaded every eighth interrupt pulse. In V.21FAX, LSB is the data bit which is first in time.

SYNCHRONOUS OPERATION

Transmitter Timing

Case 1—SC11054 Provides the Timing to the Data Terminal Equipment (DTE). See Figure 4.

If the DTE can lock to an external clock, then all that needs to be done is to put the SC11054 in the synchronous mode. This provides a 2400/1200 Hz clock on the SCT pin that can be used as a clock source for the DTE. The Transmit Phase-Locked-Loop (TX PLL) of the SC11054 will be in free-running mode.

Case 2—SC11054 Should Lock Its Transmit Timing to the Clock Source Provided by the DTE.

In this case, after selecting synchronous mode, also select "Locked" mode.

The TX PLL of SC11054 will then synchronize itself to the clock provided on its "SCTE" pin.

Case 3—Slave mode. The Transmit Timing is slaved to the receiver recovered clock. Select synchronous and "Locked" mode and set SLAVE bit.

In either case, the SC11054 will sample the data on the rising edge of the clock.

Receiver Timing

In synchronous mode, the recovered clock will be provided on the SCR pin and the transitions of RXD will be on the falling edges of this clock. Data is valid on the rising edge of the clock.

SYNCHRONOUS MODE CHART

Transmitter Timing

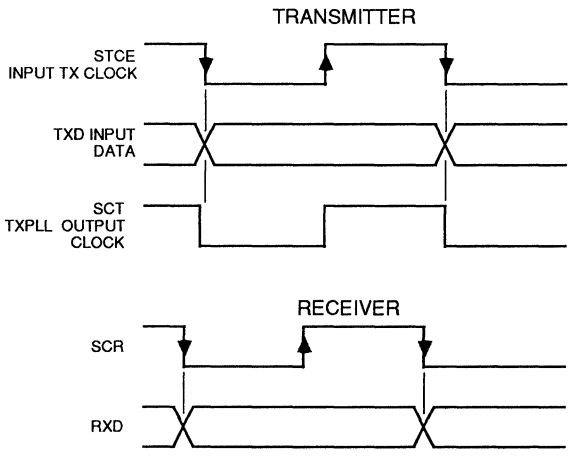


Figure 4a. SC11054 Synchronous Mode Timing Diagrams.

SPECIFICATIONS

Absolute Maximum Ratings (Notes 1–3)

Supply Voltage, V_{CC}–GND	7 V
DC Input Voltage (Analog Signals)	AGND–0.6 to V_{CC} +0.6 V
DC Input Voltage (Digital Signals)	DGND–0.6 to V_{CC} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
AGND, DGND	Ground			0		V
F_C	Clock Frequency		9.8295	9.8304	9.8313	MHz
T_R, T_F	Input Rise or Fall Time	All digital inputs except CLKIN			500	ns
T_R, T_F	Input Rise or Fall Time	CLKIN			20	ns

DC Electrical Characteristics (T_A = 0 TO 70°C, V_{CC} = +5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	Normal Power Down Mode		13 1.0	25 4	mA mA
V_{IH}	High Level Input Voltage; Digital pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital pins				0.8	V
V_{OH}	High Level Ouput (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Ouput (I_{OL} = 1.6 mA)				0.6	V
VXTA	Maximum Peak Output Level on TXA pin	V_{CC} = +5 V	3			V_{PP}

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

SPECIFICATIONS (Cont.)

AC Electrical Characteristics

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
		Processor Bus Interface: (See Figure 4)					
1	TAVLL	Address valid to end of ALE		41			ns
2	TLLAX	Address hold after end of ALE		61			ns
3	TAVDV	Address valid to output data valid				336	ns
4	TRLDV	$\overline{RD}$ active low to output data valid				194	ns
5	TRXDZ	End of $\overline{RD}$ to output data Hi Z				61	ns
6	TLHLL	ALE pulse width		71			ns
7	TRLRH	$\overline{RD}$ pulse width		214			ns
8	TWLWH	$\overline{WR}$ pulse width		148			ns
9	TQVWX	Data valid to end of $\overline{WR}$ active		132			ns
10	TWXQX	Data hold after end of $\overline{WR}$		56			ns
11	TLLRL	End of ALE to $\overline{RD}$ or $\overline{WR}$ active		60			ns
12	TRHLH	End of $\overline{RD}$ to next ALE		60			ns
13	TWXLH	End of $\overline{WR}$ to next ALE		60			ns

BUS TIMING

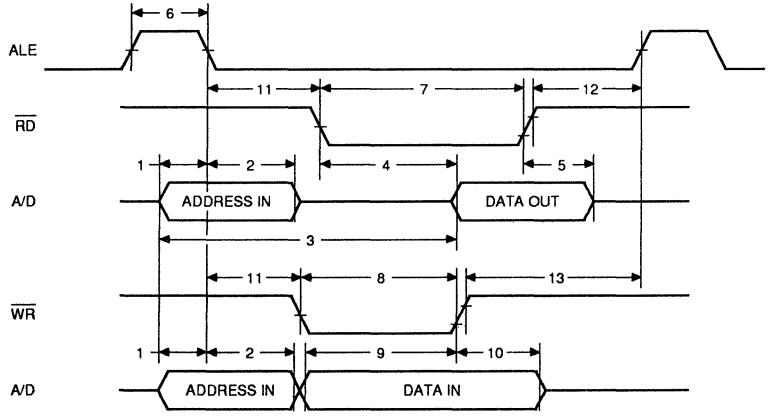


Figure 4b. Processor Bus Timing

SPECIFICATIONS (Cont.)

Modem Transmit Signals—Hz (Assume 9.8304 Crystal)

PARAMETER	CONDITIONS		NOM.	ACT.	UNITS
FSK Mod/Demod Frequencies					
Bell 103					
Answer Mark			2225	2226	Hz
Answer Space			2025	2024.4	Hz
Originate Mark			1270	1269.4	Hz
Originate Space			1070	1070.4	Hz
CCITT V.21					
Answer Mark			1650	1649.4	Hz
Answer Space			1850	1850.6	Hz
Originate Mark			980	978.34	Hz
Originate Space			1180	1181.53	Hz
Call progress monitor mode:		MIN	TYP	MAX	
Center frequency	ALB = 1, G5–G0 = 101111		480		Hz
Detect level (ED high) measured at RXA		–43			dBm
Reject level (ED low) measured at RXA				–48	dBm
Hysterisis		2			dB
Delay time (ED low to high)	EDC = 1.0 µF	10	15	24	ms
Hold time (ED high to low)	EDC = 1.0 µF	10	15	24	ms

DTMF Generator (Note 1)

PARAMETER	NOMINAL FREQUENCY	ALLOWABLE ERROR	ACTUAL ERROR
Row 1	697 Hz	±1%	–0.23%
Row 2	770 Hz	±1%	–0.01%
Row 3	852 Hz	±1%	–0.12%
Row 4	941 Hz	±1%	–0.39%
Column 1	1209 Hz	±1%	–0.35%
Column 2	1336 Hz	±1%	–0.93%
Column 3	1477 Hz	±1%	–0.48%
Column 4	1633 Hz	±1%	–0.91%
Guard Tones	550 Hz	±20 Hz	–2 Hz
	1800 Hz	±20 Hz	–2 Hz
Calling Tone	1300 Hz		–6 Hz
Answer Tone	2100 Hz	±15 Hz	+3.2 Hz
Calling Tone	1100 Hz	±38 Hz	–3.8 Hz
PIS Tone	462 Hz	±1.5 Hz	–0.05 Hz

SPECIFICATIONS (Cont.)

DTMF Generator (Cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Second Harmonic Distortion	VCC = +5 V TL2 = TL1 = TL0 = 0 Measured at TXA Pin		–40		dB
Row Output Level			–2		dBm
Column Ouput Level			0		dBm
550 Hz Guard Tone			–6		dB (Note 2)
1800 Hz Guard Tone			–9		dB (Note 2)
1300 Hz Calling Tone			–3		dBm
2100 Hz Answer Tone			–3		dBm
1100 Hz Calling Tone			–3		dBm
462 Hz PIS Tone			–3		dBm
Transmit level measured at TXA	Load = 1200 Ohms TL2 = TL1 = TL0 = 0 Squelched		–3	 –50	dBm dBm

Notes: 1: This assumes a clock of exactly 9.8304 MHz.

2: These levels are referenced to the TX signal level. When guard tones are added, the TXA level is adjusted to maintain a constant level on the line. For 1800 Hz, the adjustment is –0.97 dB; for 550 Hz, the adjustment is –1.76 dB, per the CCITT specification.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Mode	EDC = 1.0 µF; measured at RXA PGC = 0				
Energy detect level (ED low to high)				–43	dBm
Loss of energy detect level (ED low to high)		–48			dBm
Hysterisis		2	3		dB

Programmable Gain Controller (PGC)

Gain step size			0.75		dB
Dynamic range			47.25		dB
Response time (from change in PGC register to output of A to D converter)			1.0		ms

Filter Characteristics

Crosstalk rejection			70		dB
Power supply rejection			0		dB
DPLL Response times JAM or FRZ Fast			20 200		µs µs

APPLICATIONS INFORMATION

Applications

The SC11054 with an external control microprocessor, a telephone line interface and a suitable computer interface, can implement a complete 2400 bps Sendfax modem with a minimum of components and cost. Figure 7 shows the common portion of such a modem using the SC11054 with a telephone line interface. Sierra's SC22201, 128 byte E^2 memory is used to store default parameters and often used phone numbers. The SC11021 controller also supports a serial E^2 memory as an alternative. Figures 5 and 6 show the stand-alone and PC bus integral modems implemented with Sierra's SC11074/75 controllers. Figure 8 shows the connections for an external ROM special purpose controller using the SC11011. Figure 9 shows an RS-232C serial interface for implementing a stand-alone modem. Figure 10 shows a parallel bus interface for implementing an internal modem for an IBM PC/XT/AT compatible computer. Figure 11 shows a power supply schematic for a stand-alone modem application.

Various modem configurations can be realized by combining schematics shown in Figures 5 thru 11.

For performance evaluation, a circuit shown in Figure 12 can be used to obtain a constellation of the modem. Quality of the signal processing performed by the modem can thus be visualized by observing the constellation for various line conditions and signal to noise ratios.

Tone Detector Operation

The following circuit description clarifies the operation of Tone Detector, how it can be set up and how its output should be interpreted.

The Tone Detector works very differently from energy/carrier detect as follows:

a) Carrier/energy detect looks for the presence of energy and does not check the frequency.

b) Tone Detector is a digital timer. The input signal is passed through a Schmitt trigger with ±50mV hysteresis and the period of the output signal is checked by a digital timer to see if it falls within allowed limits. This block does not care about the energy of the signal unless it becomes so weak that it affects the period of the Schmitt-trigger output (i.e. close to hysteresis levels). The Tone Detector verifies 4 consecutive periods of signal before turning the corresponding bit "on". After this time, if one of the zero-crossings of the signal is corrupted (say, due to noise) it will not pass the period-check and the output bit will return "low" and wait for four new consecutive cycles of the tone with clean zero-crossings.

From the above explanation we see that:

1) Tone Detector and carrier/energy detect complement each other and for reliable tone detection, the output of both has to be monitored to check frequency and energy simultaneously.

2) Weak signals are more vulnerable to corruption by noise; consequently, the tone detector output may not stay steadily high, so its output should be integrated in software. In other words, if a given "tone bit" stays on at least 70% of the time within a time frame (say, within 40 msec) it should be considered present. Note that since the output of this block is updated at every 4 cycles of tone, then reading the output at shorter intervals just provides the same result.

As Figure 3 shows, for tone detect to function properly, its preceding

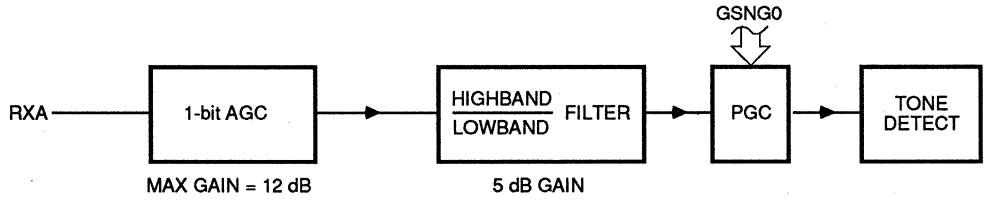


Figure 3. Tone Detector Signal Path

block has to be set up properly; i.e. Filter has to in the right band to allow passage of tone and the PGC gain has to be set up correctly to provide proper signal level to tone detect which has ±50 mV hysteresis at its input. Assuming that PGC gain code is "1F", the PGC gain will be 13.25 dB. If input level at RXA is -40dBm, the 1-bit AGC will be at its max gain and the overall gain from input pin (RXA) to tone detector input will be:

G = 12+5+13.25 = 30.25 dB
Tone Detector input = -40+30.25 = -9.75 dBm = 713 mVp-p

This is 7 times the hysteresis of Tone Detector!

So, the part should not have problems detecting -40dBm and even weaker signals if Filter and PGC are set up correctly. Reliability of detection in presence of noise can be improved by implementing the above recommendations.

Firmware

The SC11054 Sendfax modem provides all the signal processing required to dial, answer, connect, send and receive data and to send facsimile transmissions to any Group III fax machine or modem. Firmware is available from Sierra Semiconductor at no charge which works with our special controllers to perform adaptive equalization, T.30 handshake, call progress monitoring, dialing and data transmission while presenting a standard AT command set interface to the DTE. Compatible software is available from third parties for a variety of DTE environments, including MS-DOS, Windows 2 & 3, Macintosh and others. In addition, error correction and compression firmware is available, combining MNP and V.42 standards with data and Sendfax capability. Contact Sierra for details.

Power Supply Decoupling and Circuit Layout Consideration

For optimum performance at low received signal levels with low S/N ratios, it is important to use the recommended power supply decoupling circuit as shown in Figure 7.

Small inductors in series with the supplies help suppress RFI as well as improve the power supply noise rejection capability of the SC11024. A 10 Ω, 1/4W resistor in place of, or in series with, the inductor in the SC11054 power lead has been found to be helpful in computer based products or where the power supply is particularly noisy.

The 10 µF capacitors should be a tantalum type while the 0.1 µF capacitors should have good high frequency rejection characteristics—monolithic ceramic types are recommended. It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11054 as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply.

A Ferrite bead on the 5V input to the circuit board should also be considered, both from a modem performance standpoint, as well as an aid in reducing RF radiation from the phone line.

APPLICATIONS INFORMATION (Cont.)

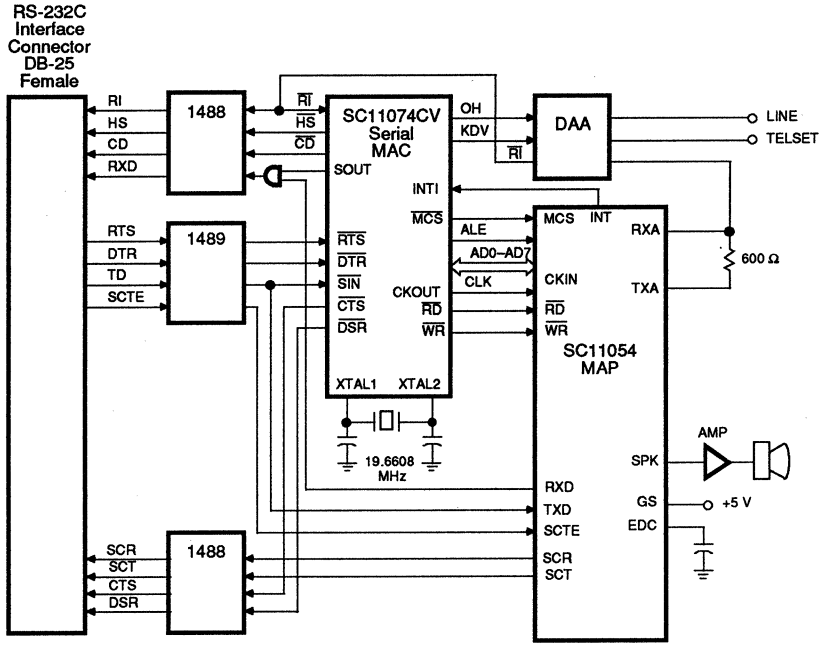


Figure 5. V22 bis Standalone Sendfax & Data Modem with Internal ROM.

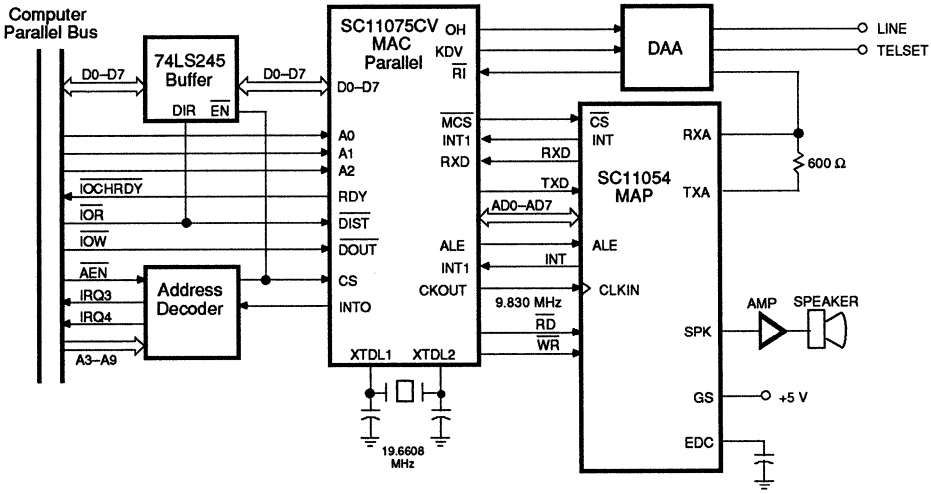
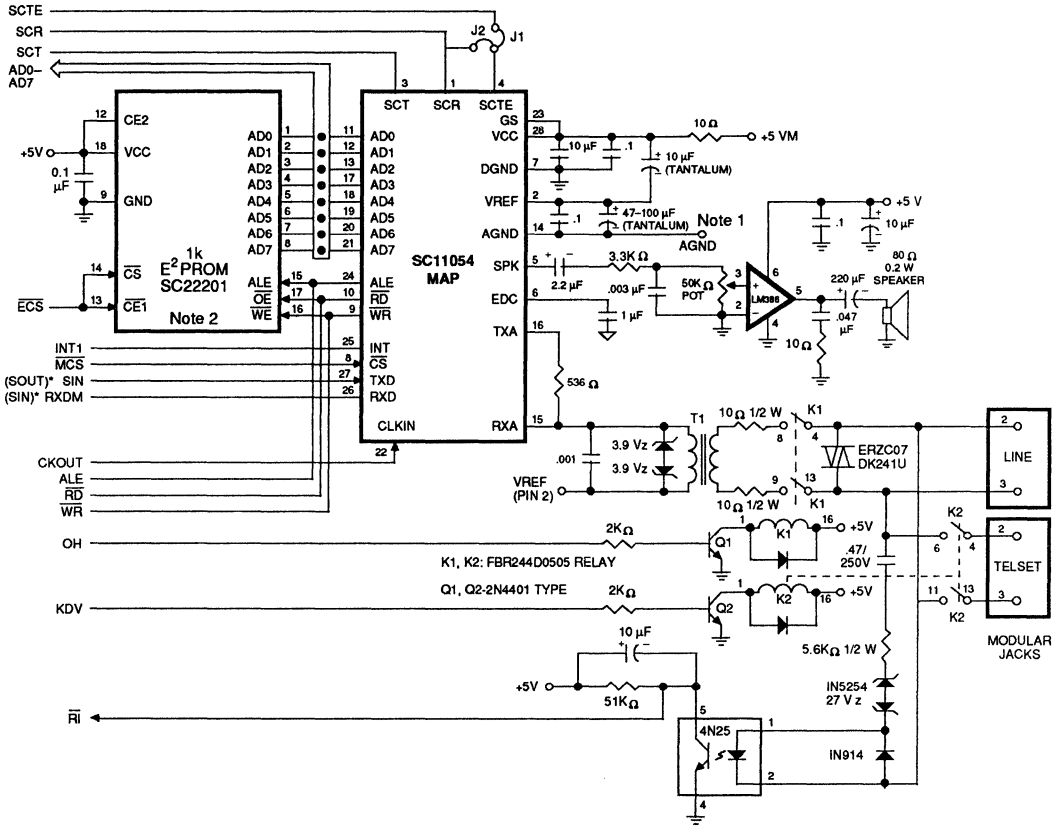


Figure 6. Internal Sendfax & Data Modem for PC Bus Applications with Internal ROM.

APPLICATIONS INFORMATION (Cont.)



Note 1: Connect analog ground directly to common of the power supply filter capacitor.

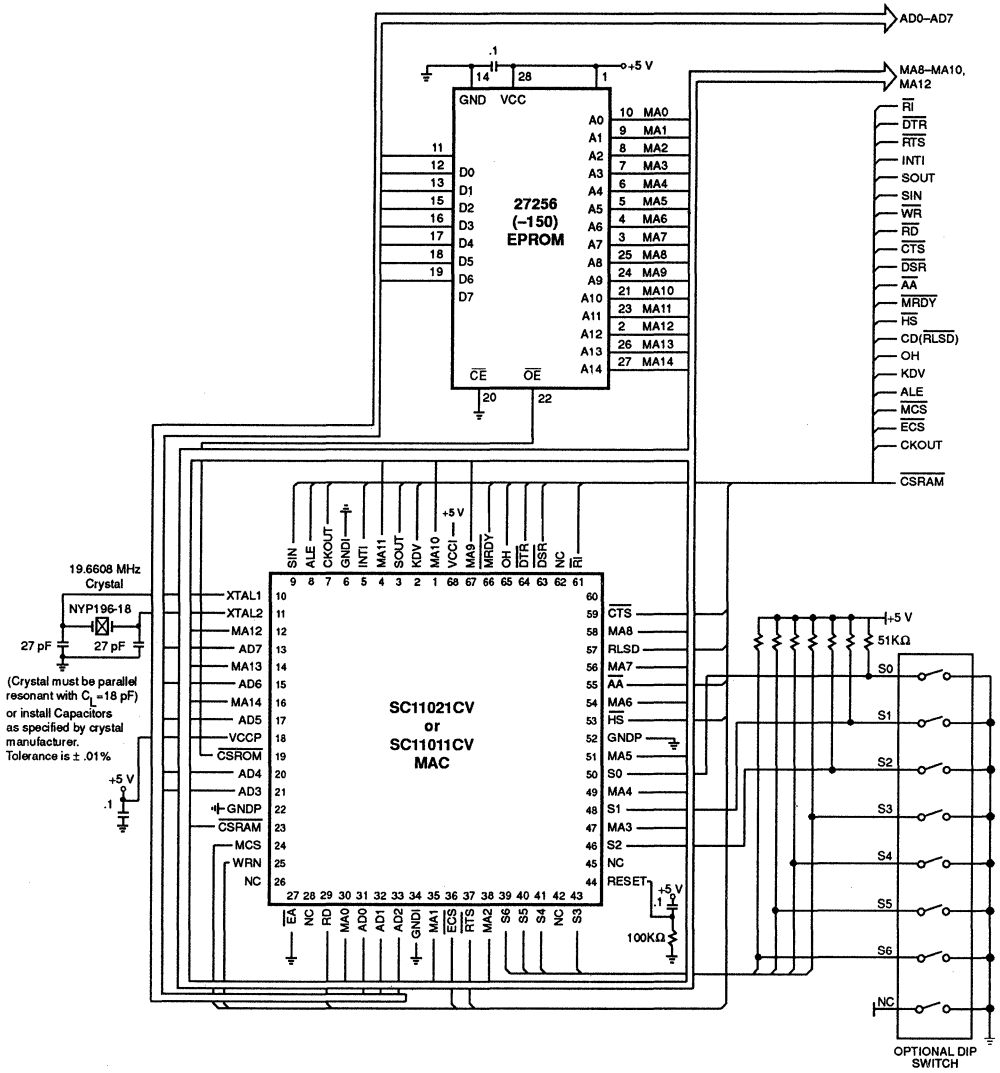
Note 2: A serial E^2 PROM may be substituted when using the SC11021 Modem Advanced Controller.

Note 3: For external clocking of the transmitter, install J1 and set bit 6 of the MCRA; omit J2.
For slave clocking of the transmitter, install J2 and set bit 6 of the MCRA; omit J1.
For normal operation, omit J1 and J2, and clear bit 6 of the MCRA.

*When used in the configuration as a parallel modem (Figure 6), connect Pin 27 of SC11054 to SOUT pin of controller and connect Pin 26 of SC11054 to SIN pin of controller.

Figure 7. Common Portion of Sendfax & Data Modem.

APPLICATIONS INFORMATION (Cont.)



SC11011 is ROMless and does not provide TDOUT or IO0–IO3 lines. These pins are "No Connect" on SC11011.
SC11021 is ROMless and can address 32k external ROM.
Consult controller data sheet for programming information.

Figure 8. Special Purpose Control Processor for Stand-Alone or Parallel Applications.

APPLICATIONS INFORMATION (Cont.)

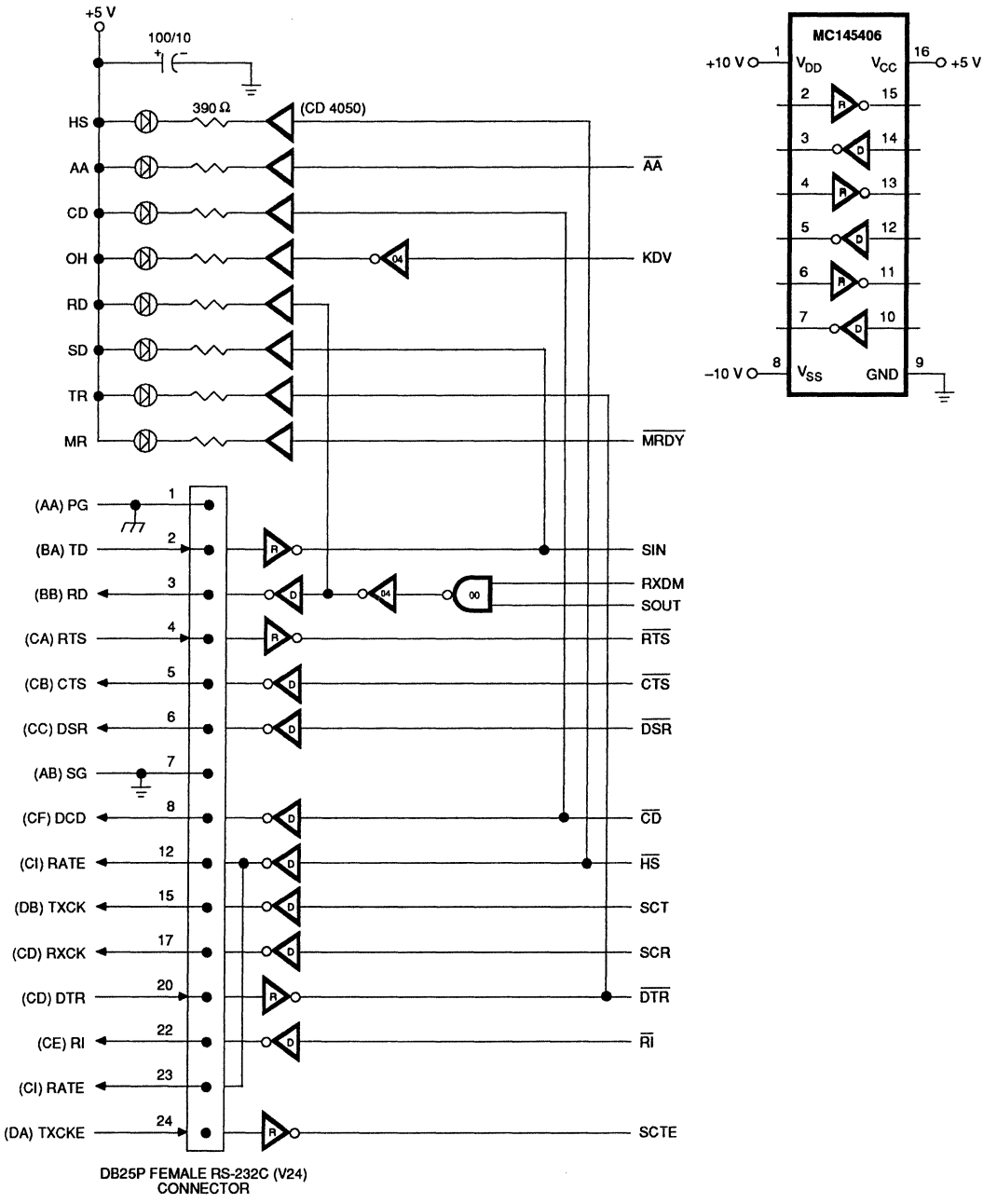


Figure 9. RS-232C Interface for Stand-Alone Modem Application.

APPLICATIONS INFORMATION (Cont.)

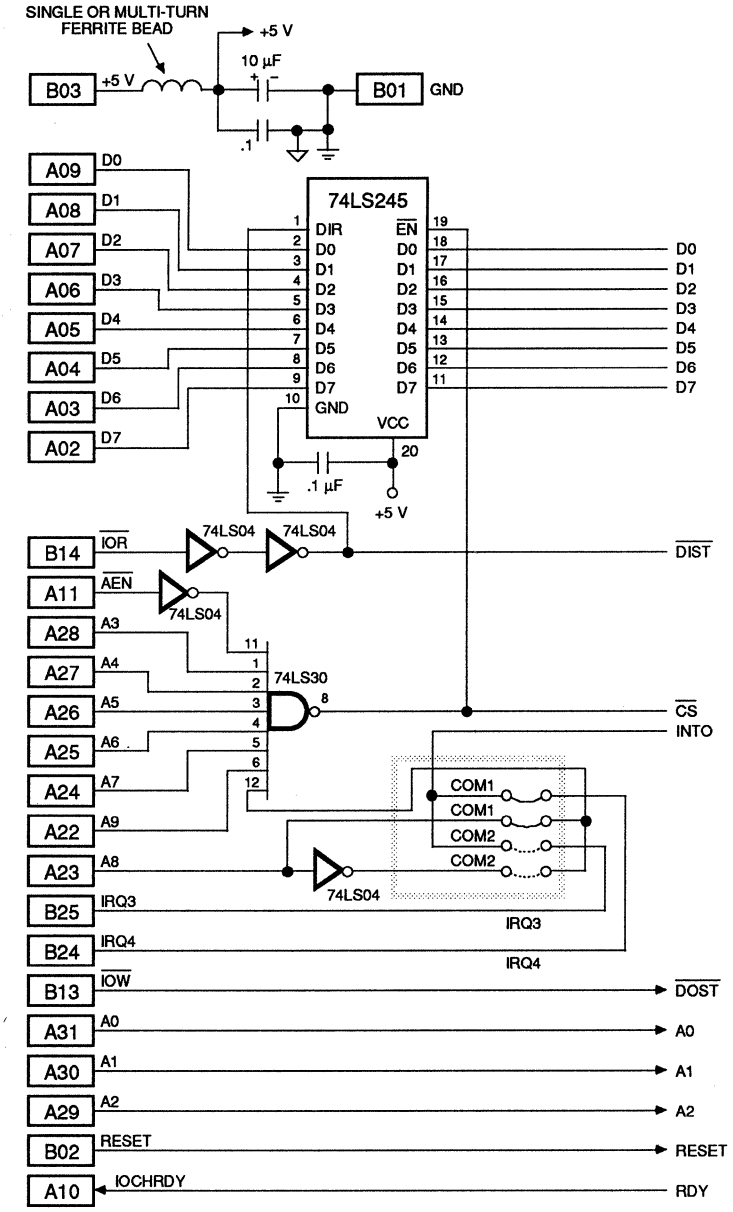


Figure 10. IBM PC/XT/AT Compatible Computer Bus Interface for SC11075 Controller of Figure 6.

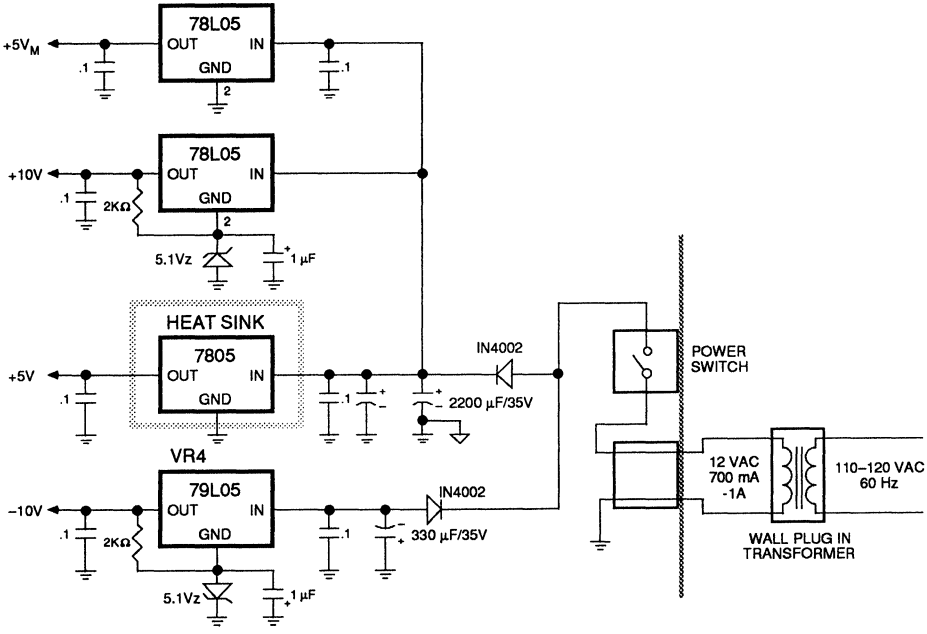


Figure 11. A Typical Power Supply for Stand-Alone Modem Application.

APPLICATIONS INFORMATION (Cont.)

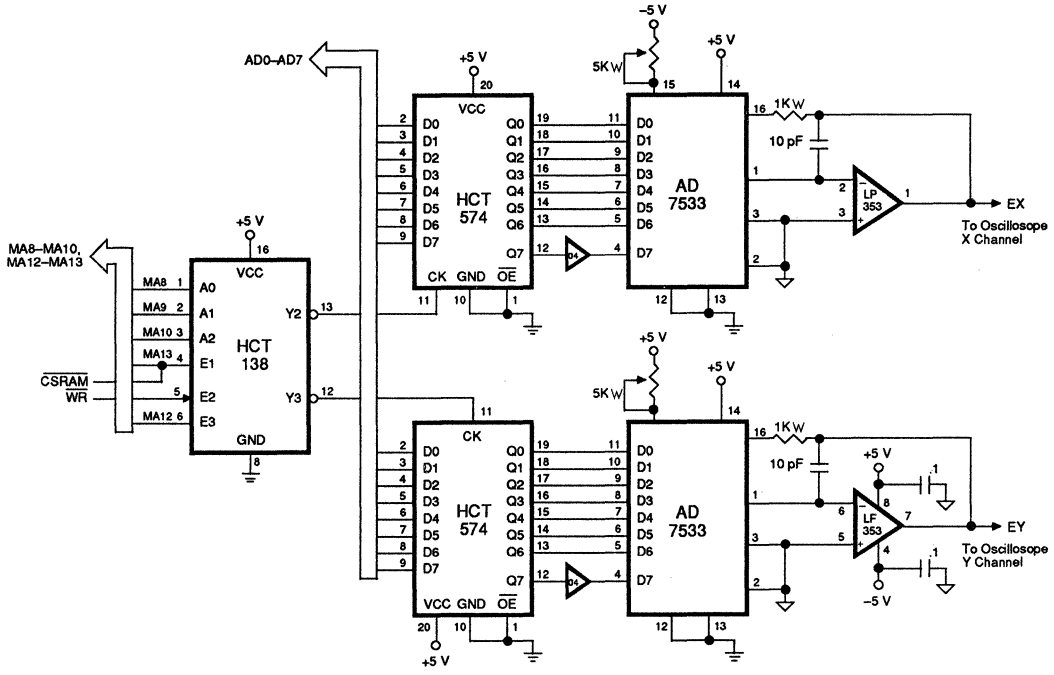


Figure 12a. Test Circuit to Generate Constellation Display.

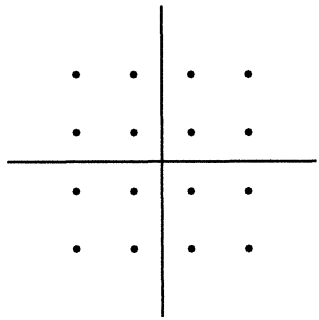
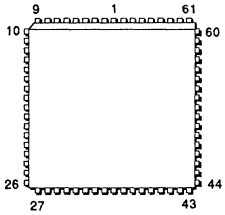


Figure 12b. Constellation for V22bis Mode Modem.

FEATURES

- ☐ V.22 bis, V.22, V.21, 212A and 103 standards
- ☐ Direct interface to SC11006/024
- ☐ Powerful enough to handle MNP5 as well as Hayes commands & DSP
- ☐ Built-in UART
- ☐ Direct IBM PC bus interface
- ☐ Performs 16 x 16 multiply in 2.2 µsec.
- ☐ Firmware compatible with SC11011CV
- ☐ CMOS technology
- ☐ 8k x 8 Internal ROM available for custom applications

68-PIN PLCC PACKAGE



SC11061CV

GENERAL DESCRIPTION

The Modem Advanced Controller (MAC) is a specialized controller which interfaces directly to the SC11006 or SC11024 Modem Analog Processor (MAP) to implement a 2400 bps full duplex intelligent modem. The two-chip set, when combined with an external EPROM containing Sierra provided firmware, performs all the modem functions associated with the Hayes "AT" Command Set. The chip set meets CCITT V.22bis standards with V.22 fallback and Bell 212A standards with 103 fallback, as well as V.21 standards.

The SC11061 interfaces to a parallel system bus, such as that in the IBM PC, or by changing one bit in the ROM code it interfaces to an RS232 port. The SC11061 includes an on board 8250B compatible, industry standard UART. With the RDY output which is used to inject "wait states" into the computer, the MAC can be used to directly interface with any speed computer. The MAC has a configuration bit which switches the UART to bring out the parallel or the serial side of the UART.

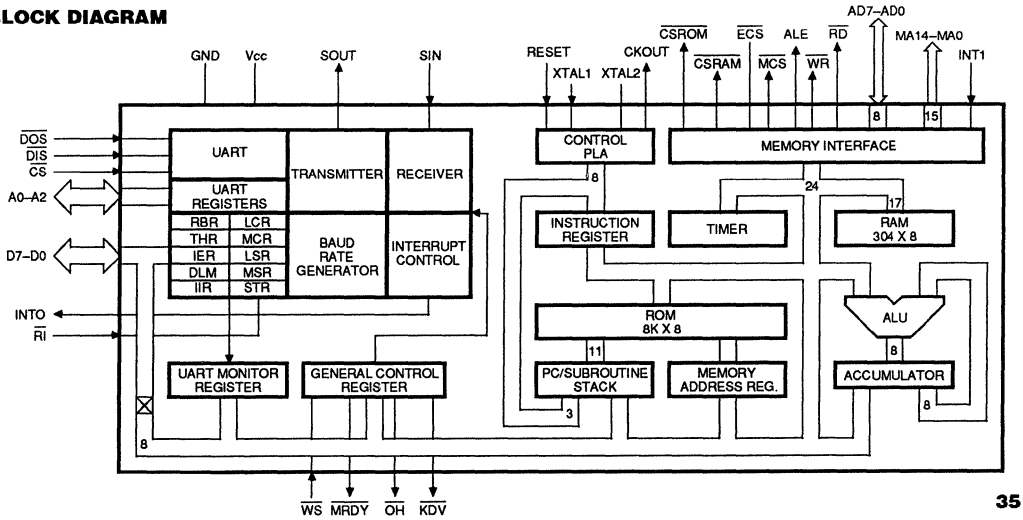
The MAC receives 8-bit signal samples from the MAP and performs adaptive equalization, carrier phase recovery, data decode, and descrambling.

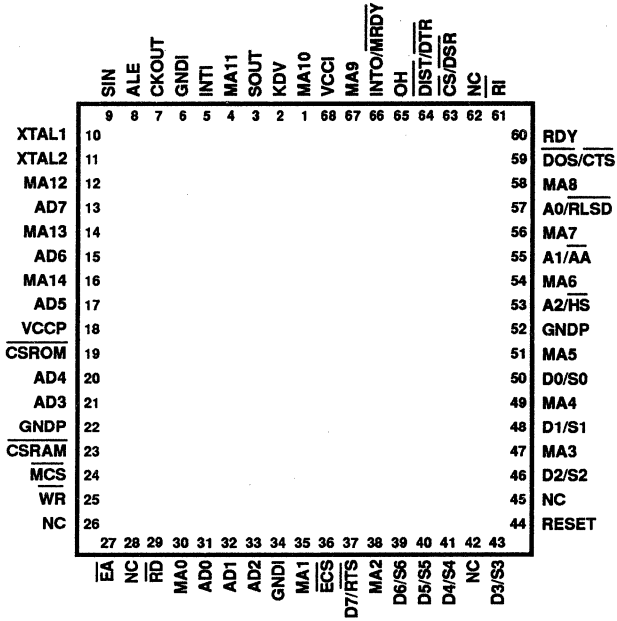
The MAC is interrupted once every 1.667 msec (600 Hz). It reads two I channel samples and two Q channel samples (T/2 sampling) within 100 µsec of receiving the interrupt. After the samples are processed a quad-bit (4 bits) of descrambled data is written back to the MAP. The MAP performs the synchronous to asynchronous conversion function, if operating in asynchronous mode, and outputs the received data on the RXD pin.

The MAC uses a bit slice core processor to perform the digital signal processing (DSP) and the control functions. Its instruction set is a subset of the Intel 8096 instruction set but operates faster than the 8096. For instance, a signed (2's complement) 16 bit by 16 bit multiply with 32 bit result takes 2.2 µsec. (Intel 8096 takes 6.5 µsec with a 12 MHz clock.) The set is compatible with 2500AD 4.0 Assembler.

For MNP2–5 applications, Sierra offers the SC11059 programmed version of the SC11061. Details are contained in the SC11059 data sheet.

BLOCK DIAGRAM





Order Number:
SC11061CV

INTERFACE BLOCK DIAGRAMS

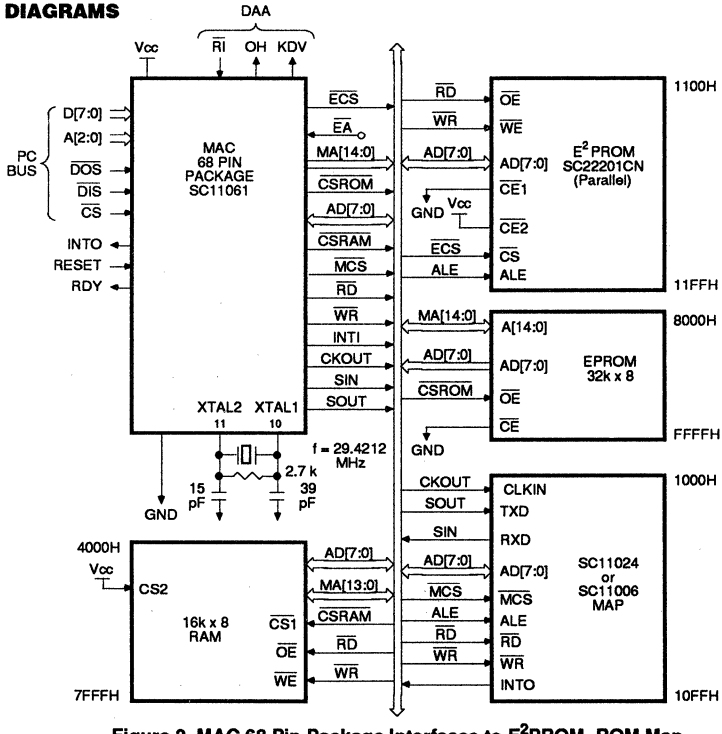


Figure 2. MAC 68 Pin Package Interfaces to E²PROM, ROM Map

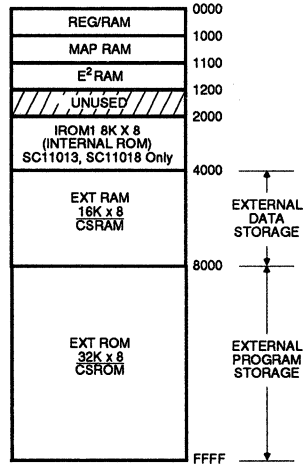


Figure 3. MAC Address Map

PIN DESCRIPTION

I Parallel System Interface (to PC Bus)

$\overline{CS}$	Chip select, active low, input, TTL.
A2–A0	Address lines for UART register select, input, TTL.
INTO	Interrupt, output, CMOS/TTL. Tristate™
D7–D0	8-bit data port, input-output, TTL.
$\overline{DOS}$	Data out strobe (PC writes into UART registers), active low, input, TTL.
$\overline{DIS}$	Data in strobe (PC reads from UART registers), active low, input, TTL.
RDY	Ouput, ready signal for high speed PC-AT interface.

II RS-232 (Data Set Mode) and Display Interface

$\overline{DTR}$	Data terminal ready, input, TTL.
$\overline{AA}$	Automatic answer enable (low), output, TTL/CMOS.
$\overline{HS}$	High speed indicator, output, TTL/CMOS. Low when operating at 2400 bps rate. High otherwise.
$\overline{MRDY}$	Modem ready.
$\overline{RLSD}$	Carrier detect, output, TTL/CMOS.
$\overline{DSR}$	Data set ready, output, TTL/CMOS.
$\overline{RTS}$	Request to send, input, TTL.
$\overline{CTS}$	Clear to send, output, TTL/CMOS.

III MAP Interface

AD7–AD0	8-bit bidirectional multiplexed address/data bus, CMOS.
$\overline{RD}$	RAM read, output, CMOS/TTL, normally high, data on AD7–AD0 must be valid at the rising edge of this pulse.
$\overline{WR}$	RAM write, output, CMOS/TTL, normally high, data on AD7–AD0 is valid at the rising edge of this pulse.
ALE	Address Latch Enable, output, CMOS/TTL, the address on $\overline{ECS}$, $\overline{MCS}$, AD7–AD0 are valid at the falling edge of this normally low pulse.
SOUT	Transmit data, output, CMOS/TTL. Serial data to be transmitted by the modem.
SIN	Received data, input; TTL. Serial data received from the MAP.
INTI	Interrupt input, TTL; interrupt received from the MAP at 600 Hz. Interrupt is detected when this pin has a low to high transition. The line has to stay high for at least 200 ns.
$\overline{MCS}$	Map chip select for MAP interface, output, TTL/CMOS, addressing space is from 1000H to 10FFH.
$\overline{ECS}$	External EERAM chip select or for second MAP chip select, output, TTL/CMOS, addressing space is fom 1100H to 11FFH.

IV Switch Port Pins (RS-232 Mode)

S6–S0	7-bit input port for sensing switch setting inputs. External pull-up registers (10 kΩ) must be used on these inputs.

V DAA Interface

$\overline{RI}$	Ring indicator, input, Schmitt, when low, indicates the modem is receiving a ringing signal.
OH	Off-hook, output, TTL/CMOS, when high, indicates the DAA should go off-hook.
KDV	Data/voice Relay Control, output, TTL/CMOS. When high, indicates the voice (telephone set) relay is closed and the modem is in the voice mode.

VI External ROM/RAM Interface

MA0–MA14	Output, TTL/CMOS, 15 bit address bus for external program/data access.
$\overline{CSROM}$	Output, TTL/CMOS, chip select for external ROM, address from 8000H to DFFFH.
$\overline{CSRAM}$	Output, TTL/CMOS, chip select for external RAM, address from 4000H to 7FFFH.
WS	Wait state, input, TTL, internal weak pull-up. When low addresses external ROM with no wait states. When high, inserts one wait state.

VII Other Pins

RESET	Master reset Schmitt input, TTL, active high. When RESET is high, MAC program counter resets to location 2000H. It resumes counting after RESET goes low.
XTAL1	Together with XTAL2 for crystal input (29.4912 MHz).
XTAL2	Crystal output pin (29.4912 MHz).
CKOUT	Clock output pin, TTL/CMOS, from MAC (9.8304 MHz).
VCCI	+5 V
VCCP	Second Vcc pin
GNDI	Ground
GNDP	Second Gnd pin
GNDP	Third Gnd pin
GNDI	Fourth Gnd pin

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SOFTWARE ARCHITECTURE

Operand Types

1. **Short Integers:** Short integers are 8-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –128 and +127 will set the overflow bit in the Program Status Byte (PSB). There are no alignment restrictions on short integers.

2. **Integers:** Integers are 16-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –32768 and +32767 will set the overflow bit in the PSB. The least significant byte of the integers is in the even byte address and the next most significant byte is in the next higher (odd) address. Therefore, the integers must be aligned at even byte boundaries in the address space. The address of a word is the address of its least significant byte (always an even address).

3. **Bits:** The bits within the bytes of the register file are numbered from 0 to 7 with 0 referring to the LSB. The only instructions that use bit addressing are JBC and JBS.

4. **Long Integers:** Long integers are 32-bit signed 2's complement variables. The result of a 16 x 16-bit multiply will be stored in a long integer. Only SHRL and SHLL manipulate this data type. Long integers are addressed by the address of their least significant byte in the register file. They should be aligned such that their address is evenly divisible by 4. The most significant byte of a long integer resides on "address" +3, where "address" is the long integer's address.

Operand Addressing

Three types of addressing are allowed:

1. **Immediate Addressing:** This is a direct field within the instruction. For short integers, this is an 8-bit field, whereas, for the integers this is a 16-bit field. Only one operand within an instruction can be immediate reference type. This operand must always be the last (right most) operand within an instruction.

   e.g. ADD AX, #340H is allowed

   ADD AX, #340H, BX is NOT allowed

2. **Register Direct Addressing:** In this mode an 8-bit field is used to access a register from the 320 byte register file. The regiter address must conform to the alignment rules.

   e.g. ADD AX, BX :AX, BX must be "even" numbers

   ADDB AX, BX :AX, BX can be "odd" or "even"

3. **Indirect Addressing:** A memory location can be addressed indirectly by placing its 16-bit address in the register file. Only one operand (the right most operand) within an instruction can be indirect.

   e.g. ADDB AL, BL, [CX] is allowed

   ADDB AL, [CX], BL is NOT allowed

Program Status Byte (PSB), location 0192H

This is an 8-bit register storing the condition flags of arithmetic, shift, and compare instructions (see the following table). It also sets the internal timer rate. The programmer can access these bits by using address 0192H.

Program Status Byte (PSB) Location 0192H

BIT	NAME	FUNCTION
7	Unused	N/A
6	TIM	Set timer rate (TIM, location 191H-Page 365) 0 = 4.8 kHz, 1=19.2 kHz
5	IP	Global interrupt pending bit. Set upon receipt of interrupt. Cleared when interrupt service begins.
4	IE	Global interrupt enable bit; when zero, all interrupts are disabled.
3	Z	Zero bit; indicates the last arithmetic or compare instruction produced a zero result.
2	N	Negative bit; indicates the last arithmetic or compare instruction produced a negative result.
1	C	Carry bit; indicates the state of the arithmetic carry from the most significant bit of the ALU for an arithmetic operation or the state of the last bit shifted out of the operand for a shift. Arithmetic "Borrow" after a subtract is the complement of the C flag (i.e. if borrow generated then C = 0).
0	V	Overflow bit; indicates the last arithmetic operation produced an overflow.

SOFTWARE ARCHITECTURE (Cont.)

Interrupt Structure

Four interrupt sources exist in the MAC, namely the external interrupt, timer interrupt, ring leading edge interrupt, and UART interrupt. The interupt service routine address is 2004H.

1) External interrupt: A low to high transition on the INTI pin initiates this interrupt.

2) Timer interrupt: Timer overflow interrupt—4.8 kHz frequency or 19.2 kHz.

3) Ring leading edge: Interrupt generated by leading edge of ring input.

4) UART interrupt: Interrupt from UART.

   a) Parallel version: From UMR register. Any one of the following can generate this interrupt.

      RBR was read by external processor

      Data was transferred from THR to TSR

      LCR was changed

      MCR was changed

      DLL or DLM was changed

   b) Serial version: In this configuration the interrupt signal from 16C450 compatible UART is brought in as an interrupt source to the internal CPU.

INTERRUPT CONTROL REGISTER (ICR), location 0193H

This is an 8 bit register to enable or disable each of the four interrupt sources and to record the interrupt sources. The upper four bits are read/write registers while the lower four bits are read only registers. A read operation to the register will automatically clear the lower four bits.

BIT0: "1" indicates UART requested an interrupt.

BIT1: "1" indicates RING leading edge requested an interrupt.

BIT2: "1" indicates TIMER overflow requested an interrupt.

BIT3: "1" indicates EXTERNAL source requested an interrupt.

BIT4: "1" to enable UART interrupt.

BIT5: "1" to enable RING leading edge interrupt.

BIT6: "1" to enable TIMER overflow interrupt.

BIT7: "1" to enable EXTERNAL interrupt.

Any one of these four interrupts will drive the processor to address 2004H. From there the software can check interrupt sources and do priority control to branch to different service routines.

INSTRUCTION SET

The MAC instruction set is a subset of Intel 8096 instruction set. The object codes, formats and the flags they effect are identical to those of 8096. The differences are:

- No VT or ST flags exist in the MAC.
- Register locations in the UART section can only be accessed by using indirect addressing.
- The operands refer to one or more bytes of the register file. ROM locations can only be addressed using indirect addressing.
- If a memory location is addressed between 1000H and 11FFH, an external six clock multiplexed bus operation is initiated. The multiplexed address/data will use AD7–AD0 bus.
- When using ST or STB operations, the destinations are always considered to be indirect addresses.

  e.g. ST, AX, [BX] is allowed

  ST, AX, BX is NOT allowed

INSTRUCTION SET (Cont.)

Instruction Set Table

MNEMONIC	NO. OF OPERANDS	OPERATION	BYTES[1]	TIME[2]
ADD/ADDB	2	B ← A + B	3	10
ADD/ADDB	3	D ← A + B	4	10
AND/ANDB	2	B ← A AND B	3	10
AND/ANDB	3	D ← A AND B	4	10
CMP/CMPB	2	D – A	3	10
DJNZ	1	Decrement & JNZ	3	9/12
EXTB	1	Sign Extend Byte	2	7
JBC	0	Jump if bit clear	3	10/13
JBS	0	Jump if bit set	3	10/13
JC	0	Jump if Carry Set	2	5/8
JNC	0	Jump if no carry	2	5/8
JE	0	Jump if =	2	5/8
JNE	0	Jump if not =	2	5/8
JGT	0	Jump if >	2	5/8
JGE	0	Jump if >=	2	5/8
JLE	0	Jump if < or =	2	5/8
JLT	0	Jump if <	2	5/8
JV	0	Jump if Overflow	2	5/8
JNV	0	Jump if no overflow	2	5/8
JH	0	Jump if higher	2	5/8
JNH	0	Jump if not higher	2	5/8
LCALL	0	Long Call	3	11
LD/LDB	2	Load	3	10
MUL	3	D ← A * B	5	33
NOP	0	NO Operation	1	2
OR/ORB	2	D ← D OR A	3	10
XOR/XORB	2	D ← D XOR A	3	10
PUSHF	0	Push PSB	1	5
POPF	0	Pop PSB	1	5
RET	0	Return	1	10
SHL/SHLB	1	Shift Left	3	$11 + N^3$
SHLL	1	Shift Left Long	3	$15 + N^3$
SHR/SHRB	1	Shift Right	3	$11 + N^3$
SHRL	1	Shift Right Long	3	$15 + N^3$
SHRA	1	Arith. Right Shift	3	$10 + N^3$
SHRAL	1	Arith. Right Long	3	$15 + N^3$
SJMP	0	Short Jump	2	7
LJMP	0	Long Jump	3	9
ST/STB	2	Store to Memory	3	13[4]
SUB/SUBB	2	B ← B – A	3	10
SUB/SUBB	3	D ← B – A	4	10

[1]Add one for immediate words.

[2]Add 9 for indirect mode and 2 or 0 for immediate mode—see table. (Cycle times @ 67 ns)

[3]N is number of bit shifts.

[4]Indirect Mode.

HARDWARE ARCHITECTURE

The FMAC device is organized with two buses that interconnect four main logic sections. The two buses are the internal data bus (DB) and address bus (Y). The four sections of the device are the internal processor, registers, memory, and dual port UART.

The two bus architecture was chosen to allow the MAC to execute the 8096 instruction set as fast or faster than the 8096 itself. The device is intended to run at 14.7456 MHz. A typical three operand instruction effectively executes in 10 clock cycles. The signed 16 x 16 multiply operation requires 34 clock cycles.

The internal data bus (DB) is the main bus of the device. It is an 8-bit bus that interconnects all four sections of the device. All intenal data travels on DB. The Y bus is a 16-bit output only bus from the internal processor that provides addresses to the memory and register sections of the device. This bus allows memory control to be resident inside the internal processor without degrading performance.

The internal processor controls MAC operations and performs all of the required computation functions. The internal processor consists of a microcontrol PLA and a 16-bit registered arithmetic/logic unit (RALU). The microcontrol PLA accepts as input 8096 instruction opcodes and generates the control sequences necessary to implement the instructions. The RALU performs instruction execution, operand address calculation, jump address calculation, program sequencing, and stack control. The program counter (PC) and stack pointer (SP) are contained within the RALU. The RALU is implemented with the 2901 silicon compiler.

The register section of the MAC includes RAM and the ports of the device. These locations are all treated as registers and may be accessed in register direct mode. Code can't be executed from registers. The UART registers are functionally, but not physically, part of the register section. The UART registers are accessed via indirect addressing mode only. There are 304 bytes of RAM to support DSP functions and the Hayes Smartmodem command set. The memory section of the MAC includes the program ROM and the external memory interface. The device contains 16K bytes of program ROM. The external memory interface allows the MAC to access program storage or data storage from external memory.

The UART section of the device implements the industry standard 8250B UART. In its parallel version the MAC appears as a 8250B to the user. The UART contains dual-port capability to allow the user and the internal processor access to its internal registers.

MEMORY DESCRIPTION

Internal ROM:

The 8k bytes of internal ROM is located at 2000H to 3FFFH may be masked for special applications. For example see SC11059 MNP5 application specific controller.

The SC11061 controller is built with the same architecture as the SC11011 so that firmware will be upward compatible.

External Read/Write:

Three different types of external memory operations are defined.

A) For address from 1000H to 11FFH:

These external operations occur through the AD bus. These operations take six clock cycles, four more than internal operations. These are mainly for MAP & EEROM interfaces, however, instructions and data can also be fetched from these memory spaces.

B) For address from 4000H to 7FFFH:

These memory spaces are reserved for external DATA storage. The MAC can access external RAM through MA address bus and AD data bus. There are six clock memory cycles for each access.

C) For address from 8000H to FFFFH:

The chip fetches instructions from external program storage by MA0–MA14 and AD0–AD7. These operations are exactly the same as internal ROM fetch and they take 2 clock cycles.

Memory Address MAP

NAME	ABV	ADDRESS	R/W	SIZE (bytes)
INTERNAL RAM/REG	RAM*	0000H–013FH	R/W	304
	REG*	0180H–0193H	R/W	17 registers
EXTERNAL MAP/EERAM	MAP	1000H–10FFH	R/W	256
	EERAM	1100H–11FFH	R/W	256
INTERNAL ROM***	IROM1	2000–3FFFH	RO	8K
EXTERNAL RAM**	RAM	4000H–7FFFH	R/W	16K
EXTERNAL ROM**	ROM	8000H–FFFFH	RO	32K

* These may only be accessed as memory locations (16-bit address) in an indirect mode. For direct addressing a 9th bit (GCR [1], called Page Bit) must be set to switch from the first 256 bytes to the rest of the RAM.

** Memory address has 15 bits (MA14–MA0); 16th bit is accessed through $\overline{\text{CSROM}}$ and $\overline{\text{CSRAM}}$.

REGISTER DESCRIPTION

This section contains a description of each of the registers in the MAC device. All of the registers of the device are 8-bits with 16-bit addresses. The registers are made up of bits that are either inputs or outputs. Input bits are read-only (RO). Output bits are read/write (R/W). The state of an output may be read back by the processor.

Test Mode:

RAM location 00H is reserved for test mode. User access is prohibited.

Serial Mode:

In parallel mode (CONF = 0) the functions of the UART registers are exactly the same as those in 8250B UART. However in serial mode, (CONF = 1), the UART is turned around and controlled by the internal processor and it becomes a data set UART. The DTR, RTS, and OUT1 in MCR register becomes DSR, CTS, and RLSD outputs. The CTS, DSR in MSR register become RTS, DTR input status from $\overline{RTS}$, $\overline{DTR}$ pins.

Note:

In serial version to echo SIN to SOUT after RESET and then go back to normal operation.

1) Set "SB" in LCR to "1".
2) Sample RDI in UART monitor register.
3) Set CM = $\overline{RDI}$ in the same register.
4) SOUT will be the same state as $\overline{CM}$.
5) Receiver is functioning, ignoring it.
6) After finishing all echoing, reset "SB" in LCR.
7) Update DLL, DLM, and set CM = 1 for normal operation.
8) Do a SET then RESET to RTRST bit to RESET RCV and TMR. Do a READ to LSR to clear LSR.
9) The UART is ready for normal operaton.

Register Address MAP

NAME	ABV	INTERNAL[3]			EXTERNAL[6]	
		INDIRECT ADDRESS[4]	DIRECT ADDRESS[5]	R/W	ADDRESS A [2:0]	R/W
UART Registers:						
Receive Buffer[1]	RBR	80H	180H	R/W	00H	RO
Transmit Holding[1]	THR	8AH	18AH	R/W	00H	WO
Interrupt Enable[1]	IER	81H	181H	R/W	01H	R/W
Interrupt ID	IIR	82H	182H	RO	02H	RO
Line Control	LCR	83H	183H	R/W	03H	R/W
Modem Control	MCR	84H	184H	R/W	04H	R/W
Line Status	LSR	85H	185H	R/W	05H	R/W
Modem Status	MSR	86H	186H	R/W	06H	R/W
Scratch Pad (8 bit)	STR	87H	187H	R/W	07H	R/W
Divisor Latch LSB[2]	DLL	88H	188H	R/W	00H	R/W
Divisor Latch MSB[2]	DLM	89H	189H	R/W	01H	R/W
UART Monitor	UMR	8BH	18BH	R/W		
Internal Registers:						
Switch Port	SWP	8DH	18DH	RO		
General I/O Port						
Direction Register	DIR	8EH	18EH	WO		
Data Register	DAR	8FH	18FH	R/W		
General Control	GCR	90H	190H	R/W		
TIMER	TIM	91H	191H	R/W		
Processor Status Byte	PSB	92H	192H	R/W		
Interrupt Control	ICR	93H	193H	R/W		

[1] DLAB bit (LCR [7]) must be zero for external access.
[2] DLAB bit (LCR [7]) must be one for external access.
[3] Register access through MA bus.
[4] 8-bit addresses for indirect addressing only, with Page bit (GCR [1]) used.
[5] 16-bit addresses for direct addressing only.
[6] UART register access through PC parallel system bus.

ACCESSIBLE REGISTERS

The system programmer may access or control any of the UART registers summarized in Table 1 via the CPU. These registers are used to control UART operations and to transmit and receive data. Their reset functions are summarized in Table 2.

Line Control Register (LCR, location 183H)

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 1 and are described in the following.

Table 1: Summary of Accessible Registers

	Register Address										
	0(DLAB=0)	0(DLAB=0)	(DLAB=0)	2	3	4	5	6	7	(DLAB=1)	(DLAB=1)
Bit No	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Iden. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	STR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSi)	0	Parity Enable (PEN)	Out 2 INT0 is High-Z when out2=0	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0, then the Parity bit is transmitted as a 0.

Table 2. Summary of Accessible Registers

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0–3) forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low, Bit 3–7 are permanently Low
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	"All Bits Low, Except Bits 5 and 6 are High"
MODEM Status Register	Master Reset	"Bits 0–3 Low, Bits 4–7— Input Signal"
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read BRR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read RBR/MR	Low

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has not effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Generator

The UART contains a programmable Baud Generator that takes an internal clock of (2/32)(XTAL1) = 1.8432 MHz and divides it by any divisor from 1 to (2^{16}–1). The output frequency of the Baud Generator should be 16 x the desired modem speed [(divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on the initial load.

Table 3 illustrates the used of the Baud Generator with a crystal frequency of 29.4912 MHz. The accuracy of the desired baud rate is dependent on the crystal accuracy. Communicaiton software writing values to the divisor latches typically expects the input to the UART to be 1.8432 MHz. They will work correctly only if the MAC input clock is maintained at 29.4912 MHz.

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Between Desired and Actual
50	2304	—
75	1536	—
110	1047	+0.026
134.4	857	+0.016
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	-0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
57600	2	—

Line Status Register (LSR, location 185H)

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 1 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: The bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is used for factory testing.

Interrupt Identification Register (IIR, location 182H)

The UART has on-chip interrupt capability that allows for flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification

Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts change the IIR, even though they are recorded, until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 1 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 4.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register (IER, location 181H)

The 8-bit register enables the four types of interrupts of the UART to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 1 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Modem Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 1 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Interrupt Identification Register				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receiver Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (If source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: Out1. Auxiliary user-designated bit. It is connected to MSR[6] (RI) during local loopback.

Bit 3: Out 2. Auxiliary user-designated bit. It is connect to MSR[7] (DCD) during local loopback. When Out2 = 0, INTO pin is Hi-Z.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input: the four MODEM. Status Register bits CTS, DSR, DCD and RI are disconnected internally; and the four MODEM Control Register bits DTR, RTS, OUT1 and OUT2 are internally connected to the four MODEM Status Register inputs, and the MODEM Control output pins $\overline{RLSD}$, $\overline{CTS}$, $\overline{DSR}$ are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5–7: These bits are permanently set to logic 0.

Modem Status Register (MSR, location 186H)

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU in addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 1 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Read (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent of DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: this bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Scratchpad Register (STR, location 187H)

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

MAC Operation

The MAC is interrupted once every 1.667 ms (600 Hz). It reads two I channel samples and two Q channel samples (T/2 sampling) within 67 μs of receiving the interrupt.

After the samples are processed a quad-bit (4 bits) descrambled of data is written back to the MAP. The MAP will perform the synch to asynch conversion function, if operating in asynchronous mode, and outputs received data on SIN pin.

REGISTER DESCRIPTION

UART Monitor (UMR, location 18BH):

The UART Monitor register allows the processor to monitor UART operations. A read operation to the UART Monitor register will clear Bit 0 to Bit 4.

BIT	NAME	DESCRIPTION
7	RTRST	Reset receiver and transmitter. When set high both receiver and transmitter will be put into reset state.
6	CM	UART Command/Modem Output. When set HIGH the UART is placed in modem mode. At reset it is low, in command mode. This bit together with SB in LCR are used for bit by bit echoing. In serial version the user can set SB = 1 and CM = $\overline{RDI}$ to echo a bit. When CONF = 1 for normal operation set CM = 1.
5	RDI	Receive Data Input. This bit monitors the RXD input of the UART.
4	DLF	Divisor Latch Flag. This bit indicates if a new baud rate count has been written to the Divisor Latch.
3	LCF	Line Control Flag. This bit indicates if the line control register has been written.
2	TXF	Transmit Buffer Full Flag. This bit indicates if a new character is in the transmit shadow register.
1	RXF	Receive Buffer Empty Flag. This bit indicates if the last character has been read from the receive buffer.
0	MCF	Modem Control Flag. This bit indicates if the modem control register has been written.

Internal Registers:

Switch Port (SWP, location 18DH): for serial mode only

The Switch Port is a 7-bit input port used only in the serial mode of the MAC. It allows for reading of the external switches of a stand-alone modem.

BIT	NAME	DESCRIPTION
6–0	S 6–0	Switch Input. These bits monitor external switches.

REGISTER DESCRIPTION

Timer (TIM, location 191H):

The Timer includes an 11 bit counter and a timer flip-flop. It is used to aid software timing functions. The counter is not readable. It can only be reset by a write. The timer flip-flop can be read to test if it is already set.

The counter and flip-flop will be reset on a write (value is don't care). After that the counter sends out a pulse train at 4.8 kHz or 19.2 kHz (PSB bit 6=1) rate to set the timer flip-flop. The flip-flop can be cleared on a read. The Timer is constantly counting by an internal clock of (9.8304 MHz).

BIT	NAME	DESCRIPTION
0	TFF0	Timer flip-flop bit.

General Control Register (GCR, location 0190H):

GCR contains a miscellaneous set of control and status bits.

BIT	NAME	DESCRIPTION
7	CONF	Configuration output. This bit controls the state of the MAC configuration. When HIGH, the MAC is configured with the SERIAL interface. It is configured with the PARALLEL interface after a reset.
6	OH	Off Hook Output. When set HIGH, the phone will be placed off hook.
5	KDV	KDV Output. Data/Voice Relay Control. When high, the modem is in the voice mode.
4	MRDY	Modem ready.
3	AA	Active HIGH AA indicator. When high this bit sets the $\overline{AA}$ pin low.
2	HS	Active HIGH HS indicator. When high this bit sets the $\overline{HS}$ pin low.
1	PAGE	Register Page Bit. This bit selects the active register page. When LOW, the lower 256 registers are accessed during register operations and when HIGH, the upper page is active.
0	$\overline{WS}$	Wait state enable status from $\overline{WS}$ pin. When high, no wait states are inserted in ROM read cycle. When low, one wait state is inserted.

COMMAND SUMMARY

Configuration & Async/Sync Commands

COMMAND	DESCRIPTION

General:

B	BELL/CCITT Protocol
E	Command Echo
L	Speaker Volume
M	Speaker Control
Q	Quiet Command
S=	Writing to S-Register
S?	Reading S-Registers
V	Enable Short-form Result Codes
X	Enable Extended Result Code Set
&J	Telephone Jack Sel.*
&M	Async/Sync Mode Sel.

Async/Sync Commands—International:

&G	Guard Tone Sel.
&P	Make/Break Dial Pulse Ratio Sel.

Async-Only Commands:

Y	Enable Long Space Disconnect
&C	Data-Carrier-Detect (DCD) Options
&D	Data-Terminal-Ready (DTR) Options
&S	Data-Set-Ready (DSR) Options

Sync-Only Commands:

&R	Clear-to-Send (CTS)/Request-to-Send (RTS)
&X	Select Sync Transmit Clock Source

* See Figure 10 for Hardware Implementation.

COMMAND	DESCRIPTION

Immediate Action Commands:

A	Go OFF-Hook in Answer Mode
A/	Re-Execute Last Command
D	Dial Telephone Number
H	Switch Hook Control
O	Return to On-Line
Z	Fetch Configuraton Profile from Nonvolatile Memory
&F	Fetch Factory Configuration Profile
&W	Write Active Configuration Profile to Nonvolatile Memory
&Z	Store Telephone Number

Dial Modifiers:

P	Pulse Dial
T	Touch-Tone Dial
R	Originate Call in Answer Mode
W	Wait for Dial Tone B/4 Continue to Dial
,	Delay a Dial Sequence
@	Wait for Quiet Answer B/4 Continue to Dial
!	Initiate a Flash
;	Return to Command State after Dialing
S=n	Dial A Stored Number (n=0 to 3)

Self Test and Diagnostics:

I/IO	Request Prod Code
I1/I2	ROM Checksum
I3	Manufacturer's I.D.
I4	Configuration Mode (Serial or Parallel)
&T	Test Modes

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

V_{CC} Supply Voltage	+6 V
Input Voltage	–0.6 V to V_{CC} +0.6 V
Storage Temperature Range	–65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range	0 to 70°C

DC ELECTRICAL CHARACTERISTICS: (T_A = 0 TO 70°C, V_{CC} = +5 V +10%) (Preliminary)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I_{CC}	Nominal Operating Current @ V_{CC} = 5.5 V		60	80	mA
V_{IH}	High Level Input Voltage for TTL input pins for CMOS input pins	 2 0.8 V_{CC}			 V V
V_{IL}	Low Level Input Voltage for TTL input pins for CMOS input pins			 0.8 0.2 V_{CC}	 V V
VT+	Positive Hysteresis Threshold for RESET & /RI input pins		2.5		V
VT–	Negative Hysteresis Threshold for RESET & /RI input pins		1.8		V
V_{OH}	High Level Output Voltage for D7–D0, into @ I_{OH} = 8 mA for RDYP—open collector for other output @ I_{OH} = 2 mA	0.7 V_{CC} +0.5			V
V_{OL}	Low Level Output Voltage for D7–D0, into pins @ I_{OL} = 8 mA for RDYP @ I_{OL} = 8 mA for other output pins @ I_{OL} = 2 mA			0.3 V_{CC} –0.5	V
I_I	Leakage Current		±1	±20	µA
F_{CLK}	Crystal Clock Frequency		29.4912		MHz

TIMING DIAGRAMS

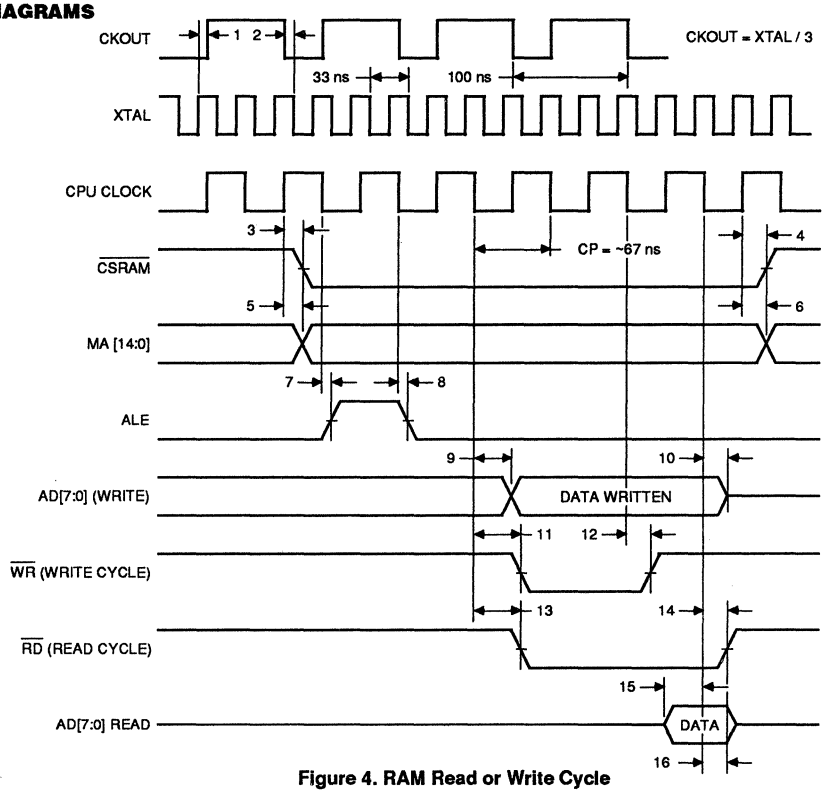


Figure 4. RAM Read or Write Cycle

RAM Read or Write Cycle Timing Table (Preliminary)

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TXTHCH	XTAL high to CKOUT high				36	ns
2	TXTHCL	XTAL high to CKOUT low				36	ns
3	TCHCSL	CPU Clk high to $\overline{\text{CSRAM}}$ low				20	ns
4	TCHCSH	CPU Clk high to $\overline{\text{CSRAM}}$ high				20	ns
5	TCHMAV	CPU Clk high to MA valid				20	ns
6	TCHMAI	CPU Clk high to MA invalid				20	ns
7	TCLALH	CPU Clk low to ALE high				12	ns
8	TCLALL	CPU Clk low to ALE low				12	ns
9	TCLADV	CPU Clk low to AD valid				28	ns
10	TCLADI	CPU Clk low to AD invalid		4			ns
11	TCLWRL	CPU Clk low to $\overline{\text{WR}}$ low				20	ns
12	TCLWRH	CPU Clk low to $\overline{\text{WR}}$ high				20	ns
13	TCLRDL	CPU Clk low to $\overline{\text{RD}}$ low				12	ns
14	TCLRDH	CPU Clk low to $\overline{\text{RD}}$ high				12	ns
15	TADVCL	AD valid to CPU Clk low (Read Set-up Time)		50			ns
16	TCLADI	CPU Clk low to AD invalid (Read Hold Time)		0			ns

TIMING DIAGRAMS (Cont.)

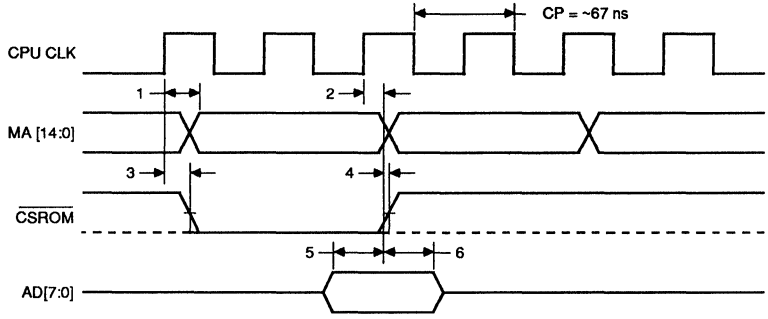


Figure 5. External Program Storage Read Bus Cycle

External Program Storage Read Bus Cycle Table (Preliminary)

NO.	SYMBOL	PARAMETER	TEST COMMENTS	MIN	TYP	MAX	UNITS
1	TCHMAV	CPU Clock high to MA valid				12	ns
2	TCHMAI	CPU Clock high to MA invalid				12	ns
3	TCHCSL	CPU Clock high to $\overline{\text{CSROM}}$ low	$\overline{\text{CSROM}}$ may already be low			12	ns
4	TCHCSH	CPU Clock high to $\overline{\text{CSROM}}$ high	$\overline{\text{CSROM}}$ may not go high			12	ns
5	TADVCH	AD valid to CPU Clock high		28			ns
6	TCHADZ	CPU Clock high to AD high-Z		0			ns

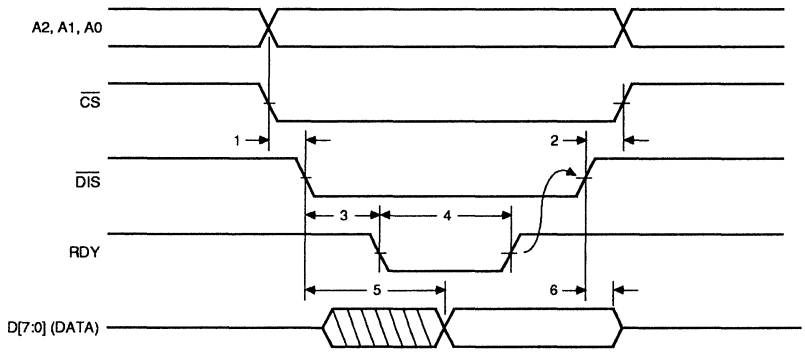


Figure 6. Read Cycle (PC Bus Read From UART Register)

Read Cycle (PC Bus Read From UART Register) Table (Preliminary)

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDIL	$\overline{\text{CS}}$ low to $\overline{\text{DIS}}$ low				0	ns
2	TDIHCSH	$\overline{\text{DIS}}$ high to $\overline{\text{CS}}$ high				0	ns
3	TDILRDL	$\overline{\text{DIS}}$ low to RDY low				26	ns
4	TRDL	RDY low time (~5–6CP)		330		400	ns
5	TDILDV	$\overline{\text{DIS}}$ low to D valid				180	ns
6	TDIHDZ	$\overline{\text{DIS}}$ high to D high-Z				12	ns

TIMING DIAGRAMS (Cont.)

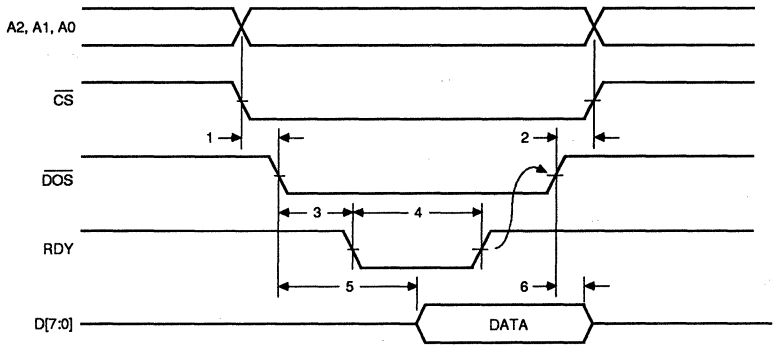


Figure 7. Write Cycle (PC Bus Write Into UART Register)

Write Cycle (PC Bus Write Into UART Register) Table (Preliminary)

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDOL	$\overline{CS}$ low to $\overline{DOS}$ low				0	ns
2	TDOHCSH	$\overline{DOS}$ high to $\overline{CS}$ high				0	ns
3	TDOLRDL	$\overline{DOS}$ low to RDY low				26	ns
4	TRDL	RDY low time (~5–6CP)		330		400	ns
5	TDOLDV	$\overline{DOS}$ low to D valid				200	ns
6	TDOHDZ	$\overline{DOS}$ high to D high-Z		0			ns

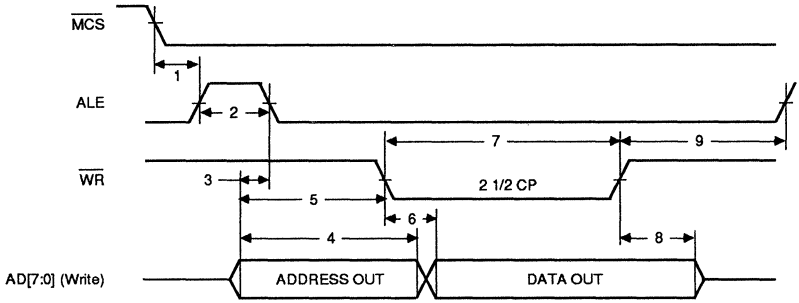


Figure 8. MAP and EERAM Bus Interface Write Cycle

MAP and EERAM Bus Interface Write Cycle Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TMCAL	$\overline{MCS}$ low to ALE high		10		20	ns
2	TALE	ALE pulse width		45			ns
3	TAVLE	Address valid to ALE low		30			ns
4	THAD	Hold address after ALE low		48			ns
5	TALRD	Delay from ALE low to $\overline{WR}$ low		45			ns
6	TDVRL	Data valid after $\overline{WR}$ low				20	ns
7	TWR	Write pulse width		160			ns
8	TDHWR	Data hold after $\overline{WR}$ high		30			ns
9	TWHLH	End of $\overline{WR}$ to next ALE		120			ns

TIMING DIAGRAMS (Cont.)

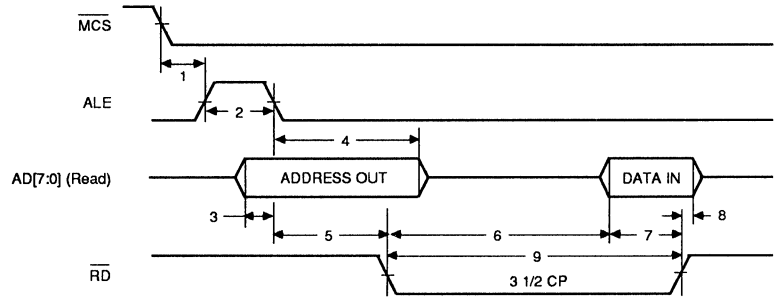


Figure 9. MAP and EERAM Bus Interface Read Cycle

MAP and EERAM Bus Interface Read Cycle Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TMCAL	$\overline{MCS}$ low to ALE high		10		20	ns
2	TALE	ALE pulse width		45			ns
3	TAVLE	Address valid to ALE low		30			ns
4	THAD	Hold address after ALE low		48			ns
5	TALRD	Delay from ALE low ro $\overline{RD}$/$\overline{WR}$ low		45			ns
6	TDVRL	Data valid after $\overline{RD}$ low				185	ns
7	TDVRH	Data valid setup to $\overline{RD}$ high		15			ns
8	TDH	Data hold after $\overline{RD}$ high		0			ns
9	TRD	Read pulse width		220		250	ns

CIRCUIT DIAGRAMS

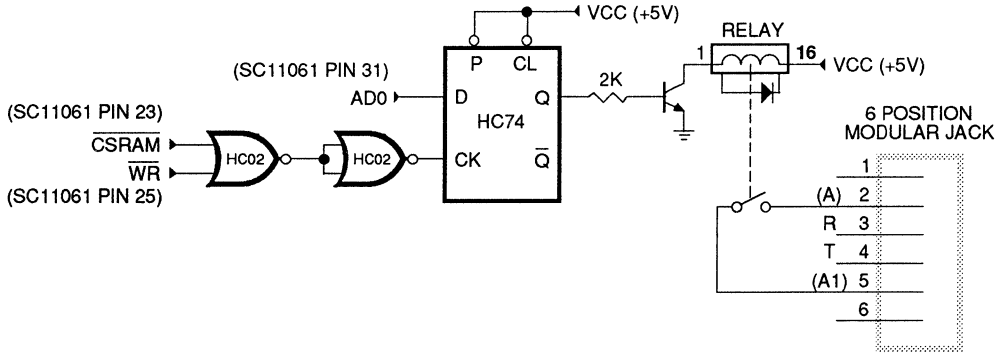


Figure 10. Circuit for Implementing & J1 Command

THE MAC AND INTEL 8096 SPEED COMPARISON

The attached is an instruction execution time comparison for the MAC and Intel 8096. The biggest improvement over 8096 is the 16 bit multiplication, it is 2.2 µs versus 6.5 µs. The jump instructions are 3 times as fast. The shift instructions are also about 3 times faster. The other arithmetic and logic instructions are about 50% faster. Indirect addressing instructions in the MAC are about the same speed as the 8096.

The following comparison is for the 8096 with 12 MHz crystal and the FMAC with 29.4912 MHz. The time unit is "µs". The instructions and operands are all from internal storage. Both the MAC and Intel 8096 will run slower for external storage access.

		DIRECT		IMMEDIATE		INDIRECT	
INSTRUCTION	OPERANDS	MAC	8096	MAC	8096	MAC	8096
ADD	2	.680	1.00	.81	1.25	1.29	1.50
ADD	3	.680	1.25	.81	1.50	1.29	1.75
ADDB	2	.680	1.00	.68	1.00	1.29	1.50
ADDB	3	.680	1.25	.68	1.25	1.29	1.75
AND	2	.680	0.75	.81	1.25	1.29	1.50
AND	3	.680	1.00	.81	1.50	1.29	1.75
ANDB	2	.680	1.00	.68	1.00	1.29	1.50
ANDB	3	.680	1.25	.68	1.25	1.29	1.75
CMP	2	.680	1.00	.81	1.25	1.29	1.50
CMPB	2	.680	1.00	.68	1.00	1.29	1.50
DJNZ		.61/.83	1.25/2.25	(NO JUMP/JUMP)			
EXTB		.47	1.00				
JBC		.68/.88	1.25/2.25				
JBS		.68/.88	1.25/2.25				
JC		.34/.55	1.00/2.00				
JE		.34/.55	1.00/2.00				
JGE		.34/.55	1.00/2.00				
JGT		.34/.55	1.00/2.00				
JH		.34/.55	1.00/2.00				
JLE		.34/.55	1.00/2.00				
JLT		.34/.55	1.00/2.00				
JNC		.34/.55	1.00/2.00				
JNE		.34/.55	1.00/2.00				
JNH		.34/.55	1.00/2.00				
JNV		.34/.55	1.00/2.00				
JV		.34/.55	1.00/2.00				
LCALL		.75	3.25				
LD	2	.68	1.00	.81	1.25	1.29	1.50
LDB	2	.68	1.00	.68	1.00	1.29	1.50
LJMP	1	.61	2.00	.68	1.00	1.29	1.50
MUL	3	2.24	6.50	(BIGGEST IMPROVEMENT)			
NOP		.16	1.00				
OR	2	.68	1.00	.81	1.25	1.29	1.50
ORB	2	.68	1.00	.68	1.00	1.29	1.50
PUSHF		.34	2.00				
POPF		.34	2.25				
RET		.68	3.00				
SHL		.75+0.06N	1.75+0.25N	(N = SHIFT COUNT)			
SHLB		.75+0.06N	1.75+0.25N				
SHLL		1.02+0.06N	1.75+0.25N				
SHR		.75+0.06N	1.75+0.25N				
SHRB		.75+0.06N	1.75+0.25N				
SHRL		1.02+0.06N	1.75+0.25N				
SHRA		.68+0.06N	1.75+0.25N				
SHRAL		1.02+0.06N	1.75+0.25N				
SJMP		.47	2.00				
ST		.88	1.75				
STB		.88	1.75				
SUB	2	.68	1.00	.81	1.25	1.29	1.50
SUBB	2	.68	1.00	.68	1.00	1.29	1.50
SUB	3	.68	1.25	.81	1.50	1.29	1.75
SUBB	3	.68	1.25	.68	1.25	1.29	1.75
XOR	2	.68	1.00	.81	1.25	1.29	1.50
XORB	2	.68	1.00	.68	1.00	1.29	1.50

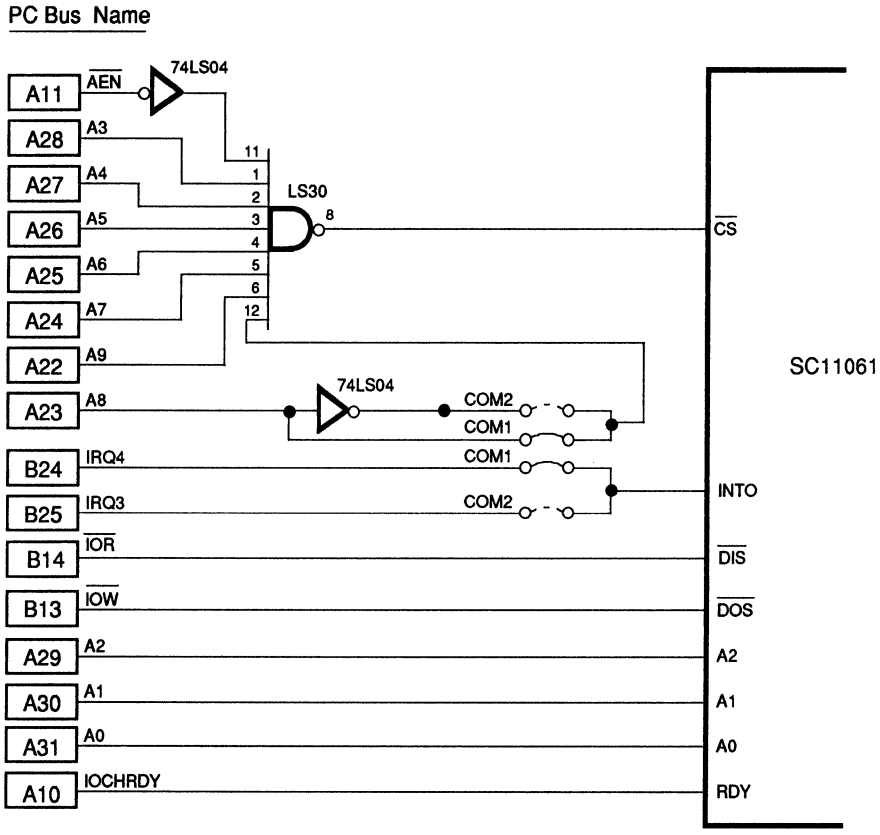


Figure 12. PC Bus Interface Address Decoder

For additional application information, consult the MAP data sheets (SC11006, SC11024, etc.).

Detailed firmware information is available through your local Sierra sales office.

The suggested crystal for the SC11061 is a third overtone parallel resonant unit with the following specifications:

Frequency: 29.4912 MHz ± 50 ppm
Load Capacitance: 12 pF
Shunt Capacitance: 5.5 pF

The following suppliers offer such a crystal:

Savoy Electronics Inc.
1175 N.E. 24 Street
P.O. Box 5727
Ft. Lauderdale, FA 33310
Phone: (305) 563-1333
Fax: (305) 563-1378

Part No: J5P312A8-29.4912
Case No: HC 49/V

Sa Ronix
4010 Transport at San Antonio
Palo Alto, CA 94043
Phone: (415) 856-6900
(800) 227-8974

Part No: SRX3860
Case No: HC 49/V

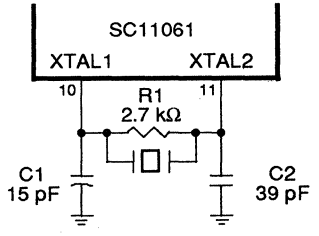
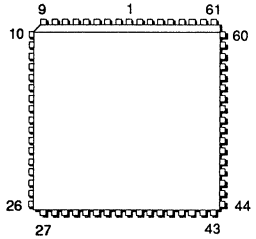


Figure 13. Crystal Oscillator Schematic

FEATURES

- ☐ Supports CCITT V.42bis & MNP1-5
- ☐ Supports SDLC, HDLC,Bisync, Monosync & Async.protocols in software
- ☐ Internal Serial Synchronous Comm. Circuit
- ☐ Can address 64K ROM,32K RAM
- ☐ Selectable Clock Frequency
- ☐ 16X16 multiply in 2μs
- ☐ Low Power Power-down (Standby) Mode
- ☐ Hardware Autobaud
- ☐ Reverse compatible with SC11011, 21,61
- ☐ Direct interface to SC11006, 24, 26, 54 Modems
- ☐ 384 Byte internal RAM
- ☐ 256 byte Internal ROM
- ☐ Power Down mode indicator on PD pin
- ☐ Supports asymmetric protocols
- ☐ Built-in UART with 80ns data access time in parallel mode
- ☐ Direct IBM PC bus interface
- ☐ Selectable IORDY Interface
- ☐ CMOS technology

68-PIN PLCC PACKAGE



SC11091

GENERAL DESCRIPTION

The UMAC is designed to perform the DSP and control functions for V.42bis and MNP5 modems operating at 2400 bps.(Complete firmware and licence available from Sierra) It supports all of Sierra's V.22bis modems including Sendfax™ SC11046 and SC11054, send/receive fax SK9698 as well as the standard SC11006, SC11024 and the Quatro modem SC11026.

Besides preserving the MAC (Modem Advanced Controller—SC11011) and Big MAC (SC11021 series) structure, the UMAC includes a one bit Serial Synchronous Comm. Circuit (SSCC) which, with firmware support, eliminates the need for an external SSCC to support HDLC and other synchronous protocols.

The SSCC is implemented as a 1 bit input, 1 bit output, 1 receive clock and 1 transmit clock. This SSCC can interrupt the CPU each time a bit is received or when a bit has been transmitted.

The SC11091 contains a 16C450 compatible UART which can be configured to provide a serial or

BLOCK DIAGRAM (Parallel Mode Callout)

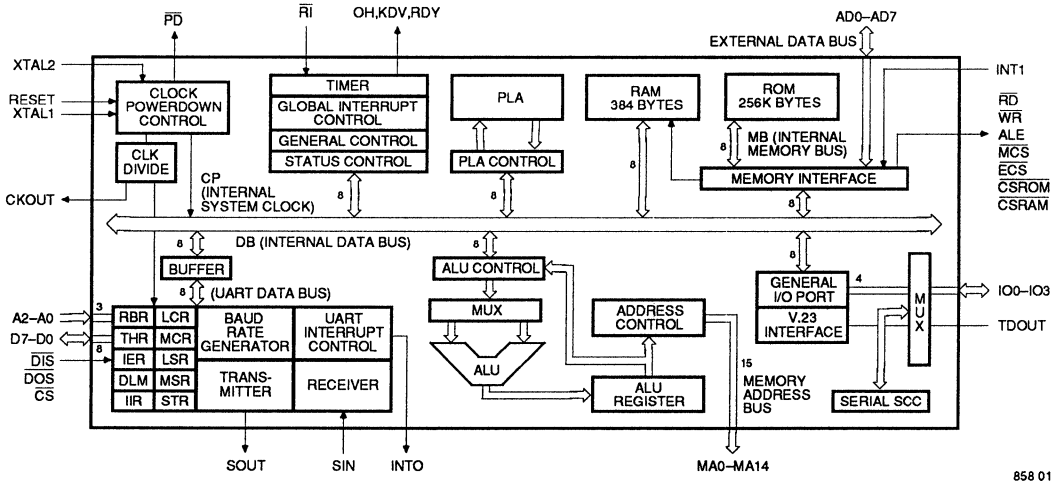


Figure 1.

DESCRIPTION (continued)

parallel DTE interface. In the RDY mode, the UMAC provides an I/O channel ready (RDY) signal to insert wait states in the PC bus read/write cycle to allow reliable data transfer with any speed bus. This can be changed by a register setting to a no-wait-state-mode. This provides a high speed UART interface, with a minimum read time of 80 n. On original power up reset, the default mode is active RDY mode. When RDY is deselected, the IORDY pin is tristated and the parallel interface timing is speeded up.

APPLICATIONS

- ☐ V.22bis modem with V.42bis compression
- ☐ MNP1-5 modems
- ☐ Class 2 Fax & Data modems
- ☐ Feature rich International modems
- ☐ Upgrade from SC11011, 11021, 11061
- ☐ Synchronous data links

CONNECTION DIAGRAM

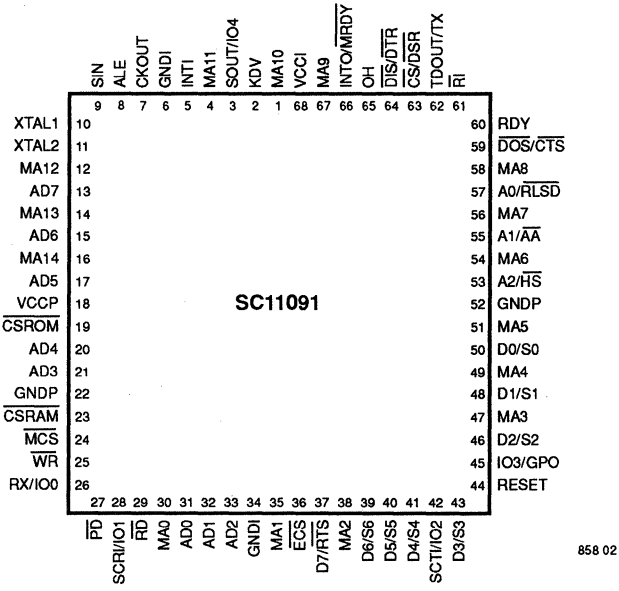


Figure 2. SC11091 Pinout Order Number
SC11091CV or in kit form SKxx91xCxVx where x depends on other options in the kit. See kit number guide at front of data book.

INTERFACE BLOCK DIAGRAMS

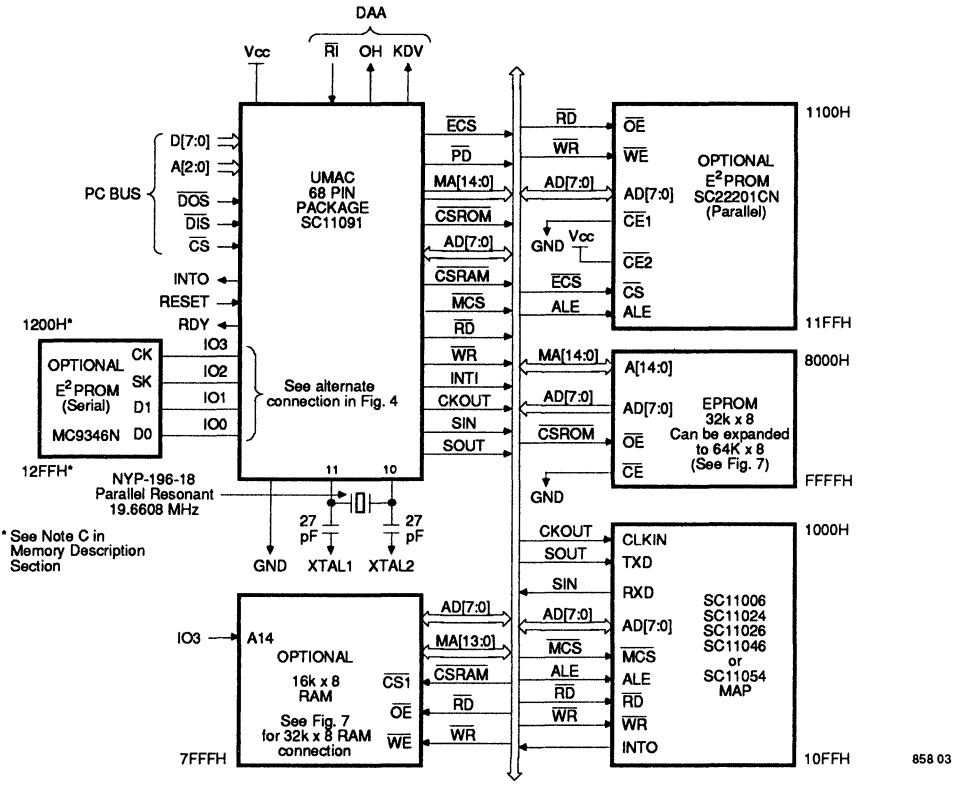


Figure 3. UMAC 68 Pin Package Interfaces to E²PROM, ROM Map
See Figure 4 for optional connection.

FUNCTIONAL DESCRIPTION

The UMAC (Universal MAC) incorporates all the features of MAC (SC11011), Big MAC (SC11021) and fast MAC (SC11061) plus other enhancements for greater capability and added value.

New Features (compared to SC11011, SC1021, SC11061)

The UMAC has External ROM address space of 64K. On power up the original 32K ROM is selected. A register select is provided to switch over to the expanded 32K ROM using the ECS pin. Bank switching is simplified through the use of instruction activated address synchronization.

Whereas the other controllers are built with 8 or 16K of internal ROM, the UMAC is designed to always use external ROM. It's internal ROM is just 256 bytes. This is for the purpose of program execution at startup and execution during power down mode. Expanded internal RAM of 384 bytes allows for more features including buffering for Fax and asymmetrical modem protocols such as V.23.

The external RAM space is doubled to 32K. The original 16K address space is allocated to RAM but provision is made for bank switching to select 32K as required for full V.42bis implementation.

In Power Down (or Standby) mode, the internal CPU clock is divided by 32 to reduce power while still remaining active and ready to respond to any input. The chip is placed in this mode by the external ROM firmware which will set the power-down bit when it determines there is no activity. The power-down bit is reset by hardware when DTR, CS, SIN or RI signals go true. An internal program loop monitors this bit and returns to normal modem operations when it is reset. By using the internal ROM for this loop, the external ROM may be de-selected so its power dissipation is minimized. A power-down mode

indication is available from the PD pin to control external power switches.

In normal operation, the PD pin behaves as a tristate pin. When power down is activated, the PD pin becomes output active low. It can be used to drive an LED indicator.

By means of register selection, the RDY interface for the parallel PC can be de-activated. This is to cater to certain LAP TOP applications where the RDY line is not supported.

When the UMAC is first powered up or reset, it defaults to Big MAC mode, which is also the mode for MAC(11011). All programs written for ROMless Big MAC (11021) and MAC (11011) or the Fast MAC (11061) should run with no or minimal modifications.

An internal timer provides hardware autobaud by counting the width of the start bit in serial applications. This eliminates the latency of software timers and permits fast, accurate autobaud on line. The timer is selectable for 4.8,9.6,19.2 or 38.4KHz.

Weak pullups are provided on switch inputs so that external pullup resistors are not needed when option switches are employed.

Internal multiplexing for asymmetrical protocols such as V.23 (1200/75 bps) is provided to allow both answer and originate modes without additional chips.

The former EA pin of MAC and Big MAC (pin 27) is redefined on the SC11091 to indicate power down status and re-named PD. (Since the SC11091 always requires external ROM the External Access option is not used) On power down activation PD pin becomes output low. Otherwise it is tristated.

The SC11011 requires a 19.6608 MHz crystal. The SC11061 (Fast MAC) requires a 29.4912MHz crystal. The UMAC has a selectable internal clock divider so it can be used with either crystal. Start-up assumes a 19.6608 MHz crystal for compatibility with SC11011 or SC11021.

Functions in common with SC11011

The SC11091 interfaces to a parallel system bus, such as that in the IBM PC, or by changing one bit in a register it interfaces to an RS232 port.

The UMAC receives 8-bit signal samples from the MAP and performs adaptive equalization, carrier phase recovery, data decode, and descrambling.

The UMAC is interrupted once every 1.667 msec (600 Hz). It reads two I channel samples and two Q channel samples (T/2 sampling) within 100 µsec of receiving the interrupt.

After the samples are processed a quad-bit (4 bits) of descrambled data is written back to the MAP. The MAP performs the synchronous to asynchronous conversion function, if operating in asynchronous mode, and outputs the received data on the RXD pin.

The UMAC uses a bit slice core processor to perform the digital signal processing (DSP) and the control functions. Its instruction set is a subset of the Intel 8096 instruction set but operates faster than the 8096. For instance, a signed (2's complement) 16 bit by 16 bit multiply with 32 bit result takes 3.5 µsec when operating with 19.6608 MHz crystal or 2µs with a 29.4912 MHz crystal. (Intel 8096 takes 6.5 µsec with a 12 MHz clock.)

When a 29.4912 MHz crystal is used, the ROM code must select a divide by 3 internal clock divider for compatibility with SC11061.

PIN DESCRIPTIONS

I Parallel Systems Interface (to PC bus)

$\overline{CS}$	Chip select, active low, input, TTL.
A2–A0	Address lines for UART register select, input, TTL.
INTO	Interrupt, output, CMOS/TTL. Tristate™
D7–D0	8-bit data port, input-output, TTL.
$\overline{DOS}$	Data out strobe (PC writes into UART registers), active low, input, TTL.
$\overline{DIS}$	Data in strobe (PC reads from UART registers), active low, input, TTL.
RDY	Ouput, ready signal for high speed PC-AT interface.

II RS-232 (Data Set Mode) and Display Interface

$\overline{DTR}$	Data terminal ready, input, TTL.
$\overline{AA}$	Automatic answer enable indicator (low), output, TTL/CMOS.
$\overline{HS}$	High speed indicator, output, TTL/CMOS. Low when operating at 2400 bps rate. High otherwise.
$\overline{MRDY}$	Modem ready.
$\overline{RLSD}$	Carrier detect, output, TTL/CMOS.
$\overline{DSR}$	Data set ready, output, TTL/CMOS.
$\overline{RTS}$	Request to send, input, TTL.
$\overline{CTS}$	Clear to send, output, TTL/CMOS.

III MAP Interface

AD7–AD0	8-bit bidirectional multiplexed address/data bus, CMOS.
$\overline{RD}$	RAM read, output, CMOS/TTL, normally high, data on AD7–AD0 must be valid at the rising edge of this pulse.
$\overline{WR}$	RAM write, output, CMOS/TTL, normally high, data on AD7–AD0 is valid at the rising edge of this pulse.
ALE	Address Latch Enable, output, CMOS/TTL, the address on ECS, MCS, AD7–AD0 are valid at the falling edge of this normally low pulse.
SOUT	Transmit data, output, CMOS/TTL. Serial data to be transmitted by the modem.
SIN	Received data, input; TTL. Serial data received from the MAP.
INTI	Interrupt input, TTL; interrupt received from the MAP at 600 Hz. Interrupt is detected when this pin has a low to high transition. The line has to stay high for at least 200 ns.
$\overline{MCS}$	Map chip select for MAP interface, output, TTL/CMOS, addressing space is from 1000H to 10FFH and 1200H to RFFH
$\overline{ECS}$	External EERAM chip select or for second MAP chip select, output, TTL/CMOS, addressing space is from 1100H to 11FFH. When used for ROM expanded mode, the ECS functions as the second chip select.

IV Switch Port Pins (RS-232 Mode)

S6–S0	7-bit input port for sensing switch setting inputs. Weak internal pull-ups (30 kΩ) are provided on these inputs.

V DAA Interface

$\overline{RI}$	Ring indicator, input, Schmitt, when low, indicates the modem is receiving a ringing signal.
OH	Off-hook, output, TTL/CMOS, when high, indicates the DAA should go off-hook.
KDV	Data/voice Relay Control, output, TTL/CMOS. When high, indicates the voice (telephone set) relay is closed and the modem is in the voice mode.

VI External ROM/RAM Interface

MA0–MA14	Output, TTL/CMOS, 15 bit address bus for external program/data access.
$\overline{CSROM}$	Output, TTL/CMOS, chip select for external ROM, address from 8000H to FFFFH.
$\overline{CSRAM}$	Output, TTL/CMOS, chip select for external RAM, address from 4000H to 7FFFH.
$\overline{PD}$	Output, CMOS open drain, indicates power down mode by active low.

VII Other Pins

RESET	Master reset Schmitt input, TTL, active high. When RESET is high, UMAC program counter resets to location 2000H. It resumes counting after RESET goes low.
XTAL1	Together with XTAL2 for crystal input (19.6608 MHz or 29.4912MHz).
XTAL2	Crystal output pin (19.6608 MHz or 29.4912 MHz).
CKOUT	Clock output pin, TTL/CMOS, from UMAC (9.8304 MHz).
VCCI	+5 V
VCCP	Second Vcc pin
GNDI	Ground
GNDP	Second Gnd pin
GNDP	Third Gnd pin
GNDI	Fourth Gnd pin

VIII Special Pin Functions

The UMAC can be configured to emulate the BigMAC (SC11021) which has four IO pins and a TDOUT pin added. For the UMAC, the functions of these 5 pins are preserved on power up or reset. When the SSCC mode is selected, the functions of these 5 pins will conform to the requirements for a firmware SSCC. (See figure 4)

Tristate is a trademark of National Semiconductor.

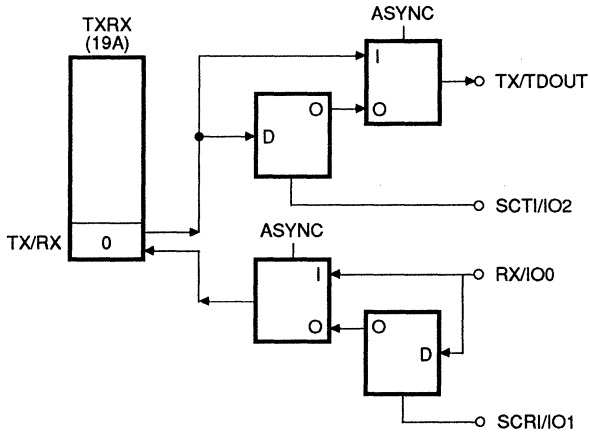
The function of the five pins and the SIN and SOUT pins are defined as follows:

In SSCC Mode

SCRI	Synchronous clock receive. TTL input. Data from the MAP is valid on the rising edge of the clock.
SCTI	Synchronous clock transmit. TTL input. Data to the MAP is strobed in on the rising edge of this clock.
RX	Receive data from MAP. TTL input.
TDOUT	Transmit data to MAP. TTL output.
GPO	General purpose output. TTL/CMOS compatible. RAM bank select.
SIN	Input bit 7 of Data Register. Serial input to UART when XUART set low.
SOUT	UART serial output when XUART set low.
IO4	General purpose output when XUART set high. Output follows the state of Bit 6 of Data Register

In BigMAC mode

IO3-0	General I/O Port, TTL/CMOS, tri-state. Each I/O can be configured as input or output under the control of GIO register.



858 04

Figure 4a. Simplified Schematic of 1 bit SSCC

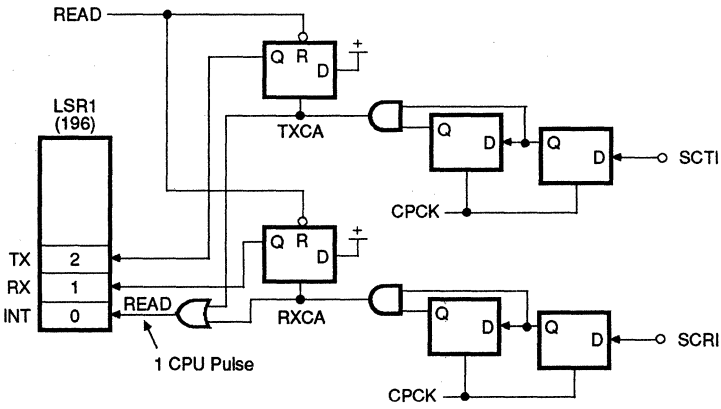


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Figure 4b. SSCC Interrupt Circuit (Simplified)

FIRMWARE ARCHITECTURE

The SC11091 uses a subset of 8096 instructions and can be compiled with an 8096 cross assembler such as AD2500. Rev 4.0 up of this assembler is recommended.

Operand Types

1. Short Integers: Short integers are 8-bit signed 2's complement variables. Results outside the range –128 and +127 will set the overflow bit in the Program Status Byte (PSB). There are no alignment restrictions on short integers.

2. Integers: Integers are 16-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –32768 and +32767 will set the overflow bit in the PSB. The least significant byte of the integers is in the even byte address and the next most significant byte is in the next higher (odd) address. Therefore, the integers must be aligned at even byte boundaries in the address space. The address of a word is the address of its least significant byte (always an even address).

3. Bits: The bits within the bytes of the register file are numbered from 0 to 7 with 0 referring to the LSB. The only instructions that use bit addressing are JBC and JBS.

4. Long Integers: Long integers are 32-bit signed 2's complement variables. The result of a 16 x 16-bit multiply will be stored in a long integer. Only SHRL and SHLL manipulate this data type. Long integers are addressed by the address of their least significant byte in the register file. They should be aligned such that their address is evenly divisible by 4. The most significant byte of a long integer resides on "address" +3, where "address" is the long integer's address.

Operand Addressing

Three types of addressing are allowed:

1. Immediate Addressing: This is a direct field within the instruction. For short integers, this is an 8-bit field, whereas, for the integers this is a 16-bit field. Only one operand within an instruction can be an immediate reference type. This operand must always be the last (right most) operand within an instruction.

   e.g. ADD AX, #340H is allowed

   ADD AX, #340H, BX is NOT allowed

2. Register Direct Addressing: In this mode an 8-bit field is used to access a register from the 320 byte register file. The register address must conform to the alignment rules.

   e.g. ADD AX, BX :AX, BX must be "even" numbers

   ADDB AX, BX :AX, BX can be "odd" or "even"

3. Indirect Addressing: A memory location can be addressed indirectly by placing its 16-bit address in the register file. Only one operand (the right most operand) within an instruction can be indirect.

   e.g. ADDB AL, BL, [CX] is allowed

   ADDB AL, [CX], BL is NOT allowed

Software Considerations for SSCC Implementation

The one bit SSCC approach saves a significant portion of hardware needed to implement the SSCC. The drawback is that the workload of the CPU is increased to emulate the SSCC. When operated at 1200 baud, the time window between data bits is 833 μs and at 2400 baud, it is 417 uS. The CPU must juggle between UART communication and DSP execution.

The following items should be considered:

SDLC:

1. Send flags (01111110) for start, stop or idle operation. (SC11054 Sendfax MAP included hardware flag detectors)
2. For data and CRC result, a zero must be inserted after five ones has been transmitted.
3. If five ones have been received and the next bit is zero, this zero bit is deleted
4. Detection of flag (01111110) or abort (11111111) sequence.
5. Generation and checking of CRC-CCITT or the newer CRC-32 for 32 bit CRC.
6. Intepret, transmit and receive error conditions and make corrective actions for data integrity.

BISYNC & MONOSYNC:

1. Generation and detection of SYNC character.
2. Selectable character length.
3. Parity may be included.
4. 6 or 8 bit (12 or 16 for bisync) sync character.
5. Detect escape sequence to prevent false sync detection and exclusion from CRC-16 calculation and checking.
6. Go into hunt mode to detect sync characters.
7. Interpret transmit and receive error conditions and make corrective actions for data integrity.

ASYNC:

1. Generation and detection of start and stop bits.
2. Selectable character length.
3. Parity may be included.
4. Selectable baud rates. Auto-bauding may be required. Independent baud rates for transmit and receive may be needed.
5. In MNP operation, CRC-16 generation and checking are required.
6. In MNP operation, detect escape sequence to prevent false sync detection and exclusion from CRC-16 calculation and checking.
7. Intepret transmit and receive error conditions and make corrective actions for data integrity.

Program Status Byte (PSB), location 0192H

This is an 8-bit register storing the condition flags of arithmetic, shift, and compare instructions (see Table 1). The programmer can access these bits by using address 0192H.

Interrupt Structure

Five interrupt sources exist in the UMAC, namely the external interrupt, timer interrupt, ring leading edge interrupt, SSCC and UART interrupt. The interupt service routine address is 2004H.

1. External interrupt: A low to high transition on the INTI pin initiates this interrupt.
2. Timer interrupt: Timer overflow interrupt—4.8 kHz frequency.
3. Ring leading edge: Interrupt generated by leading edge of ring input.
4. UART interrupt: Interrupt from UART.
   a. Parallel version: From UMR register. Any one of the following can generate this interrupt:
      - RBR was read by external processor
      - Data was transferred from THR to TSR
      - LCR was changed
      - MCR was changed
      - DLL or DLM was changed

   b. Serial version: In this configuration the interrupt signal from 16C450 compatible UART is brought in as an interrupt source to the internal CPU.

Program Status Byte (PSB)

BIT	NAME	FUNCTION
7	PD	Power-Down enable bit. Set HIGH to power down. Set LOW to power-up. CKOUT slows down to 32 times during power-down. Hardware reset on RI, DTR off ton in serial mode or RI, DIS, CS off to in parallel mode.
6	ROBK/TM	ROM bank switch when GCR2.5=1 else set TIMER rate TIM, location 191H, O = 4.8 kHz, I = 19.2 kHz)
5	IP	Global interrupt pending bit. Set upon receipt of interrupt. Cleared when interrupt service begins.
4	IE	Global interrupt enable bit; when zero, all interrupts are disabled.
3	Z	Zero bit; indicates the last arithmetic or compare instruction produced a zero result.
2	N	Negative bit; indicates the last arithmetic or compare instruction produced a negative result.
1	C	Carry bit; indicates the state of the arithmetic carry from the most significant bit of the ALU for an arithmetic operation or the state of the last bit shifted out of the operand for a shift. Arithmetic "Borrow" after a subtract is the complement of the C flag (i.e. if borrow generated then C = 0).
0	V	Overflow bit; indicates the last arithmetic operation produced an overflow.

Table 1. PSB Table

INTERRUPT CONTROL REGISTER (ICR), LOCATION 0193H

This is an 8 bit register to enable or disable each of the five interrupt sources and to record the interrupt sources. The upper four bits are read/write registers while the lower four bits are read only registers. A read operation to the register will automatically clear the lower four bits.

BIT 0: "1" indicates UART requested an interrupt.

BIT 1: "1" indicates RING leading edge requested an interrupt.

BIT 2: "1" indicates TIMER overflow requested an interrupt.

BIT 3: "1" indicates EXTERNAL source requested an interrupt.

BIT 4: "1" to enable UART interrupt.

BIT 5: "1" to enable RING leading edge interrupt.

BIT 6: "1" to enable TIMER overflow interrupt.

BIT 7: "1" to enable EXTERNAL interrupt.

Any one of these five interrupts will drive the processor to address 2004H. From there the software can check interrupt sources and do priority control to branch to different service routines.

5. SSCC Interrupt.

INSTRUCTION SET

The UMAC instruction set is a subset of Intel 8096 instruction set. The object codes, formats and the flags they effect are identical to those of 8096. The differences are:

- No VT or ST flags exist in the UMAC.
- Register locations in the UART section can only be accessed by using indirect addressing.
- The operands refer to one or more bytes of the register file. ROM locations can only be addressed using indirect addressing.
- If a memory location is addressed between 1000H and 12FFH, an external six clock multiplexed bus operation is initiated. The multiplexed address/data will use AD7–AD0 bus.
- When using ST or STB operations, the destinations are always considered to be indirect addresses.

  e.g. ST, AX, [BX] is allowed

  ST, AX, BX is NOT allowed

MNEMONIC	NO. OF OPERANDS	OPERATION	BYTES[1]	TIME[2]
ADD/ADDB	2	B ← A + B	3	10
ADD/ADDB	3	D ← A + B	4	10
AND/ANDB	2	B ← A AND B	3	10
AND/ANDB	3	D ← A AND B	4	10
CMP/CMPB	2	D – A	3	10
DJNZ	1	Decrement & JNZ	3	9/12
EXTB	1	Sign Extend Byte	2	7
JBC	0	Jump if bit clear	3	10/13
JBS	0	Jump if bit set	3	10/13
JC	0	Jump if Carry Set	2	5/8
JNC	0	Jump if no carry	2	5/8
JE	0	Jump if =	2	5/8
JNE	0	Jump if not =	2	5/8
JGT	0	Jump if >	2	5/8
JGE	0	Jump if >=	2	5/8
JLE	0	Jump if < or =	2	5/8
JLT	0	Jump if <	2	5/8
JV	0	Jump if Overflow	2	5/8
JNV	0	Jump if no overflow	2	5/8
JH	0	Jump if higher	2	5/8
JNH	0	Jump if not higher	2	5/8
LCALL	0	Long Call	3	11
LD/LDB	2	Load	3	10
MUL	3	D ← A * B	5	33
NOP	0	NO Operation	1	2
OR/ORB	2	D ← D OR A	3	10
XOR/XORB	2	D ← D XOR A	3	10
PUSHF	0	Push PSB	1	5
POPF	0	Pop PSB	1	5
RET	0	Return	1	10
SHL/SHLB	1	Shift Left	3	11 + N[3]
SHLL	1	Shift Left Long	3	15 + N[3]
SHR/SHRB	1	Shift Right	3	11 + N[3]
SHRL	1	Shift Right Long	3	15 + N[3]
SHRA	1	Arith. Right Shift	3	10 + N[3]
SHRAL	1	Arith. Right Long	3	15 + N[3]
SJMP	0	Short Jump	2	7
LJMP	0	Long Jump	3	9
ST/STB	2	Store to Memory	3	13[4]
SUB/SUBB	2	B ← B – A	3	10
SUB/SUBB	3	D ← B – A	4	10

[1]Add one for immediate words.
[2]Add 9 for indirect mode and 2 or 0 for immediate mode—see table. (Cycle times @ 1.02 ns) for 19.6608 MHz crystal or 68 ns for 29.4916 MHz crystal)
[3]N is number of bit shifts.
[4]Indirect Mode.

Table 2. Instruction Set

HARDWARE ARCHITECTURE

The UMAC device is organized with two buses that interconnect four main logic sections. The two buses are the internal data bus (DB) and address bus (Y). The four sections of the device are the internal processor, registers, memory, and dual port UART.

The two bus architecture was chosen to allow the UMAC to execute the 8096 instruction set as fast or faster than the 8096 itself. The device is intended to run at 9.8304 MHz or 14.745MHz . (The internal divider provides these clock speeds from an external 19.6608 MHz or 29.4912 MHz crystal) A typical three operand instruction effectively executes in 10 clock cycles. The signed 16 x 16 multiply operation requires 34 clock cycles.

The internal data bus (DB) is the main bus of the device. It is an 8-bit bus that interconnects all four sections of the device. All internal data travels on DB. The Y bus is a 16-bit output only bus from the internal processor that provides addresses to the memory and register sections of the device. This bus allows memory control to be resident inside the internal processor without degrading performance.

The internal processor controls UMAC operations and performs all of the required computation functions. The internal processor consists of a microcontrol PLA and a 16-bit registered arithmetic/logic unit (RALU). The microcontrol PLA accepts as input 8096 instruction opcodes and generates the control sequences necessary to implement the instructions. The RALU performs instruction execution, operand address calculation, jump address calculation, program sequencing, and stack control. The program counter (PC) and stack pointer (SP) are contained within the RALU. The RALU is implemented with the 2901 silicon compiler.

The register section of the UMAC includes RAM and the ports of the device. These locations are all treated as registers and may be accessed in register direct mode. Code can't be executed from registers. The UART registers are functionally, but not physically, part of the register section. The UART registers are accessed via indirect addressing mode only. There are 384 bytes of RAM to support DSP functions and the command set. The memory section of the UMAC includes the program ROM and the external memory interface. The device contains 256 bytes of program ROM. The external memory interface allows the UMAC to access program storage or data storage from external memory.

The UART section of the device implements, in hardware, the industry standard 16C450 UART. In its parallel version the UMAC appears as a 16C450 to the user. The UART contains true dual-port capability to allow the user and the internal processor access to its internal registers.

Hardware Definition of the SSCC

Figure 4a shows a simplified diagram of the single bit Serial Synchronous Communication Circuit. In synchronous operation, the internally generated transmit signal is clocked out by the SCT clock and the received signal is clocked in by the SCR clock In asynchronous mode the latches are bypassed.Figure 4b shows how the SSCC interrupts are generated. Figure 5 shows the timing relation between the MAP to SSCC interface and the internal synchronization for clock and data.

The SSCC can be operated either in the synchronous or asynchronous modes. In synchronous mode SCR and SCT clocks are supplied by the MAP. To operate in asynchronous mode, the CPU must generate the neccessary timing for the transmit and receive.

Synchronous Operation

If SSCC is selected and the SSCC mode select bits are both low, the SSCC operates in synchronous mode.

Receiver Operation—When SCR is low, the d_latch is enabled to pass in Rx input. When the SCR goes high, it latches the Rx input, generates a pulse of 1 cp period to interrupt the processor and sets the Rx available flip flop. When the CPU reads the Rx data, the Rx flip flop is reset. If the interrupt mode is disabled, the CPU can scan the Rx available flip flop to determine if data is available.

Transmitter Operation—To transmit a bit the CPU writes the bit data into the transmit buffer. This resets the transmit buffer empty flip flop. When the SCT is low, this data bit passes through to the Tx (transmit) pin. When the SCT goes high, this data bit is latched. The SCT also causes an interrupt pulse and also sets the Tx Buffer Empty flip flop. If the interrupt mode is disabled, the CPU can scan the Tx Buffer Empty flip flop to determine if data has been strobed out.

Asynchronous Operation

If SSCC is selected and the SSCC mode select bits are both high, the SSCC operates in asynchronous mode.

Receiver Operation—The d_latch is always open. If the interrupt is enabled, a high to low transistion will generate an interrupt pulse and latch the Rx available flip flop. This interrupt should then be disabled

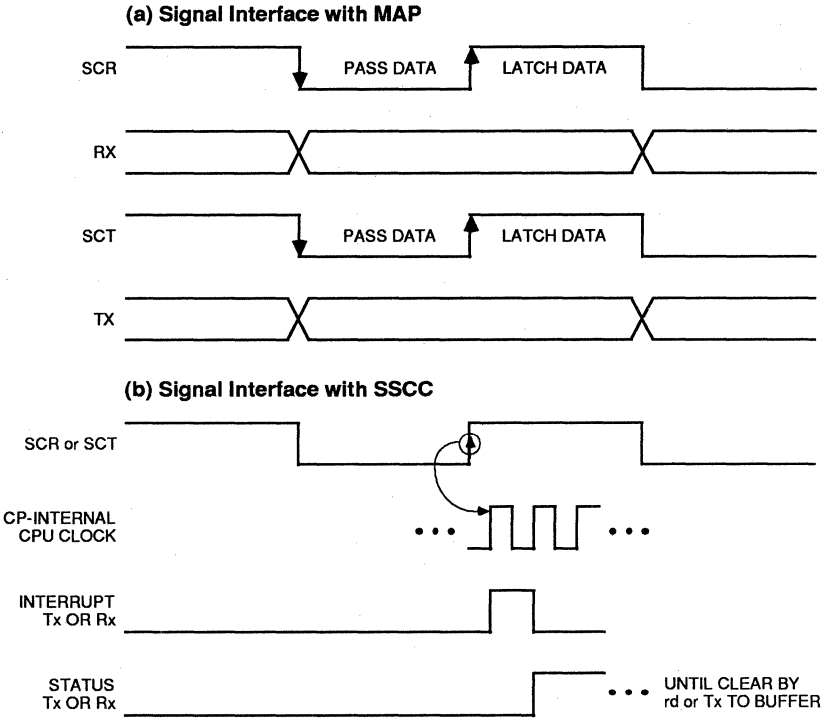


Figure 5. Synchronous Mode Timing

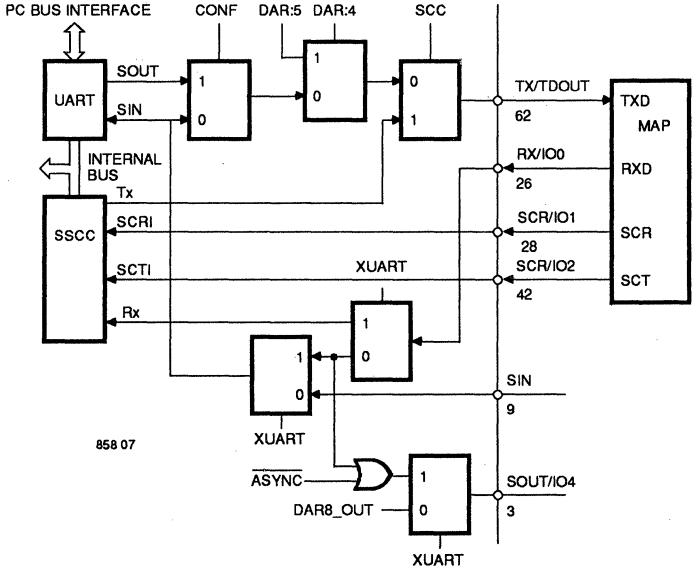


Figure 6a. UMAC Internal Data Path

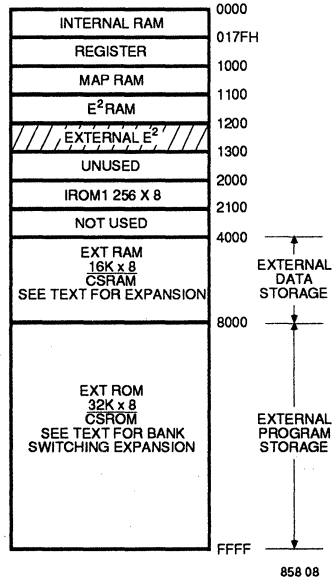


Figure 6b. UMAC Address Map

until the character is fully assembled. The CPU must internally synchronize with the incoming data stream.

Transmitter Operation—The d_latch is always open. To transmit a bit the CPU writes the bit into the transmit buffer. The CPU must take care of start stop bits and the timing to strobe the data out to the TX pin.

Other Modes of Operation

If the SSCC local loopback is set to 1, the transmitted data is routed back to the receive buffer.

If the Auto echo is set to 1, received signal is echoed back to the transmitter. The receiver will still receive the data.

If the SCTI SCRI is set to 1, the transmit clock provides clock input to the receiver.

Datapath & Description

Figure 6a shows the data path portion of UMAC. The function of the I/O pins affected by the UMAC is described. The rest of the I/O functions remains the same as SC11021. See GIO register information on page 26.

The control signals are described in Table 3 to aid analysis of the data path.

SIGNAL NAME	DESCRIPTION
SCC(B0 in GCR1)	When high, the firmware SSCC is selected for communication. Default is low after reset.
CONF	Refers to GCR bit 7 in MAC. When high, the configuration is serial. Default is low after reset.
DIR0-3	Direction registers as in GPIO of Big MAC.(SC11021) When high, the IOs are defined as outputs. When low, they become inputs.
DAR0-5	Data registers as defined in Big MAC.(SC11021)
DAR6-7	2 Additional registers utilizing the SIN and SOUT pins when UMAC is configured in parallel mode. DAR6 is output only and DAR7is input only.
XUART	Exclude UART. When high, signal from SIN and SOUT will not be communicated to the UART. When the UMAC has the SSCC selected and configured for parallel operation, this control enables the SIN pin to be used as IO pin and SOUT to be used for output pin. Default is low after reset.
$\overline{\text{ASYNC}}$	When bit B1 and B2 of general control register 1 (GCR1) are high, $\overline{\text{ASYNC}}$ will be low. The signal from the RX/IO0 can be directed to the SOUT/O4 pin. This control enables full V.23 implementation of originate and answer mode without having to add external components to the route.

Table 3.

The following operating modes are allowed:

MODE	DESCRIPTION
Stand-alone	UART communicates with MAP and RS232. Conditions: SCC=0, DAR4=1, CONF=1, XUART=0, $\overline{\text{ASYNC}}$=0. This configuration is used to establish handshake.
Stand-alone	SSCC communicates with MAP. UART communicates with RS232. Conditions: SCC=1, DAR4=X, CONF=1, XUART=0, $\overline{\text{ASYNC}}$=1. This configuration is used for MNP and V.42bis operation.
Parallel	UART communicates with MAP andPC interface. Conditions: SCC=0, DAR4=1, CONF=0, XUART=1, $\overline{\text{ASYNC}}$=1. This configuration is used to establish handshake.
Parallel	UART communicates with PC interface. SSCC communicates with MAP. Conditions: SCC=1, DAR4=X, CONF=0, XUART=1. $\overline{\text{ASYNC}}$=1. This configuration is used for MNP and V.42 bis operation.
Stand-alone	UMAC operating as replacement for MAC (SC11011, 61) or Big MAC (SC11021). Conditions: SCC=0, DAR4=X, CONF=1, XUART=0, $\overline{\text{ASYNC}}$=1
Parallel	UMAC operating as replacement for MAC or Big Mac. Conditions: SCC=0, DAR4=X, CONF=0, XUART=0, $\overline{\text{ASYNC}}$=1

Clock Generation and Powerdown

The MAC and Big MAC run on a 19.6608 MHz crystal. This frequency is divided by two and the 9.8304 MHz is used for internal hardware timing and for the CKOUT clock. When the UMAC is operated at 29.4912MHz (1.5X) the internal CPU clock remains at half the crystal oscillator speed. However, the UART baud rate, the timers and the CKOUT to the MAP are kept at the normal speed to maintain software compatibility. This is done by setting the clock selection to divide by 3.

CKOUT—is maintained at 9.8304 MHz out. When the divide by 3 is selected, the CKOUT will be out of phase to the internal divide by 2 clock at certain cycles. When divide by 2 is selected, the CKOUT will be synchronized with the internal clock.

UART—Maintains the same base clock into the baud rate generator. This is achieved by modulating the counter input.

Clock selection. Register refers to bits B0 and B1 in GCR2.

REGISTER B0	B1	SELECT	CRYSTAL USED
0	0	divide by 3	29.4912 MHz
0	1	divide by 2	19.6608 MHz - default
1	x	reserved	

When switching from one frequency to another the transitions are glitch free. The CKOUT is phase synchronized with the internal CPU clock when the divide by 2 is selected.

Power down mode is activated in the same manner as in BigMAC when bit 7 of the PSB byte is set high and inputs RI, CS, DTR and SIN are all high. In this mode, the switch-over to divide by 32 clock is synchronized to prevent glitching. The UMAC comes out of power down mode when any of the inputs or bit 7 of PSB is set low. A short subroutine loop is included in the UMAC ROM which examines bit 7 of the PSB byte. When it goes low, a return is executed and the external code execution resumes. By using the internal ROM for this function, there is no need to select the external ROM so that it can be in a low power state.

Hardware Autobaud

When hardware autobaud is selected by writing a 1 to bit 6 of the GCR2 register, the timer output feeds a 7 bit counter. The count begins when the SIN signal goes low and stops when SIN goes high. When SIN goes high, it generates an interrupt and also sets a flag in bit 0 of the timer register. The value of the 7 bit count appears in bit 1 (LSB) to bit 7 (MSB) of the timer register. If the Timer interrupt is disabled, the interrupt will not be generated.

The timer time out rate can be changed from 4.8 KHz to 38.4 KHz through the General Control register GCR2 or PSB depending on the state of GCR2.5.

When the hardware autobaud is deselected, normal timer function is operational. This is the default selection.

RDY Interface

The RDY pin is used to inject wait states to synchronize the UMAC with the PC's parallel access. Some Laptops do not incorporate this wait mechanism. By setting bit 7 in GCR2 high, the UMAC operates in the NO-RDY mode that interfaces to the PC without the need for the RDY pin.

MEMORY DESCRIPTION

Internal ROM:

The 256 bytes of internal ROM are located at 2000H to 20FFH.

The SC11091 controller is built with the same basic architecture as the SC11019/20/21/22/23 so that firmware will be upward compatible.

External Read/Write:

Three different types of external memory operations are defined.

A) For address from 1000H to 12FFH:

These external operations occur through the AD bus. These operations take six clock cycles, four more than internal operations. These are mainly for MAP & EEROM interfaces, however, instructions and data can also be fetched from these memory spaces.

B) For address from 4000H to 7FFFH:

These memory spaces are reserved for external DATA storage. The UMAC can access external RAM through MA address bus and AD data bus. There are six clock memory cycles for each access.

C) For address from 8000H to FFFFH:

The chip fetches instructions from external program storage by MA0–MA14 and AD0–AD7. These operations are exactly the same as internal ROM fetch and they take 2 clock cycles.

Extended ROM bank switching and addressing

With increased code needed to service MNP and V.42bis classes of communication, the usual 32K ROM may not be sufficient to hold all the code. An improved method of hardware switching and software selection of the desired 32K ROM bank is implemented in the UMAC. No external Hardware decoder is needed to select the 2 ROM banks. However, one extra gate is needed to select the MAP when the 64k mode is used. The extended ROM can be two 32K x 8 ROMs (27256) or one 64Kx8 ROM (27512). Fig 7a and 7b show the two configurations. If two 32K x 8 ROMs are used the ROM CONFIG bit in B4 of GCR2 must be set to 0 (default state). If one 64K x 8 ROM is used, then the ROM CONFIG bit is set to 1.

The ECS pin is used for the ROM extension. This is normally used for the EEPROM selection. If used for ROM extension, then the EEPROM must be addressed differently. The memory location 1100H to 11FFH must not be accessed if extended ROM is used. Instead, the EEPROM access will be mapped at 1200H to 12FFH using the MCS pin as the chip select. External decoding is needed. Fig 7c shows how it is done. If multiplexed EEPROM is not used, there is no need for this extra decoding.

The original ROM bank is called bank 0 and the extended bank is called bank 1. Bank 0 is the power-on or reset default when two 32K x 8 ROMs are used. However when one 64K x 8 ROM is used, the external ROM access starts at Bank 1 as the ECS pin is high by default. Switching from bank 0 to bank 1 is done using a method known as instruction activated bank switching. The 3 instructions LCALL, LJMP and RET will activate the ROM bank selection at the appropriate moment when a new address is strobed onto the memory bus. The advantage of this method is that interbank access can take place even when the program is executing from the external ROMs.

The ROM selection bit is bit 6 of PSB (0192H). However this is currently used by Fast MAC (SC11061) for switching the timer from 4800Hz to 19.2kHz which presents a compatibility issue. The UMAC design satisfies both demands. On power up or reset, the PSB bit 6 is used for the timer selection. By setting bit 5 of GCR2 to 1, the function of the PSB bit 6 is changed to ROM select bit as defined. The timer frequencies can be selected from bits 2 and 3 in the GCR2.

The selection of the ROM banks during interrupt servicing is further enhanced by a modified PUSHF instruction. If bit 5 in the GCR2 is set to 1 to activate the ROM bank mode, the PUSHF instruction will set the PSB bit 6 to 0 after the PSB status is saved onto the stack. Thus, no additional software is needed to set this bit. The POPF instruction will restore the correct bank status on return from interrupt. The PUSHF and POPF are included in the interrupt servicing routine in the internal ROM. It need not be repeated externally.

Table 4a illustrates how an LCALL can be done into the other bank. Table 4b illustrates how LJMP can be done into the other bank. Table 4c illustrates how the interrupt is serviced.

RD indication During External ROM Access

The SC11011, 21 & 61 do not provide an indication when the ROM contents are read into the CPU. In the SC11091, the RD pin goes low for 1 clock cycle when the ROM contents are being read into the UMAC CPU. Figure 10 shows the timing. The RD function is the same for extended ROM operation.

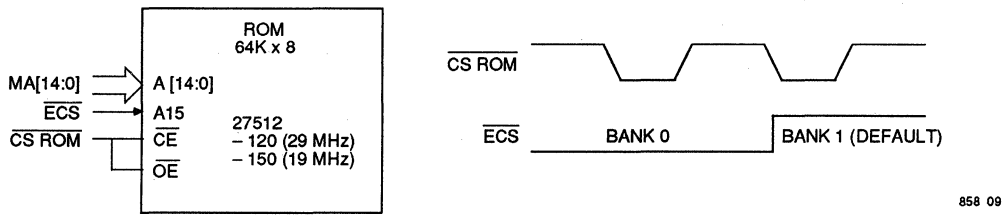


Figure 7a. OE Could be Grounded, But Above Connection Saves Power in PD Mode.

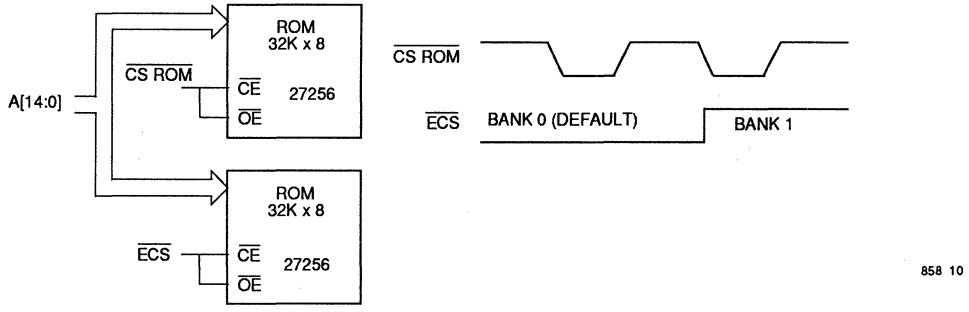
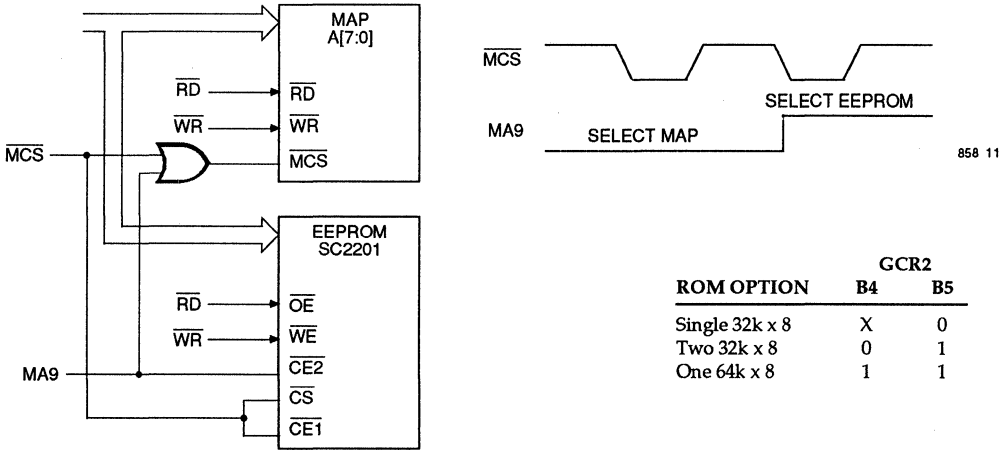


Figure 7b. Alternative Use of Two 27256 ROMs



ROM OPTION	GCR2 B4	GCR2 B5
Single 32k x 8	X	0
Two 32k x 8	0	1
One 64k x 8	1	1

Figure 7c. If EEPROM is Used and If $\overline{ECS}$ is Used for Expanded ROM Options then Additional Decoding is Required

Figure 7. Interface Block Diagrams for Optional Modes.

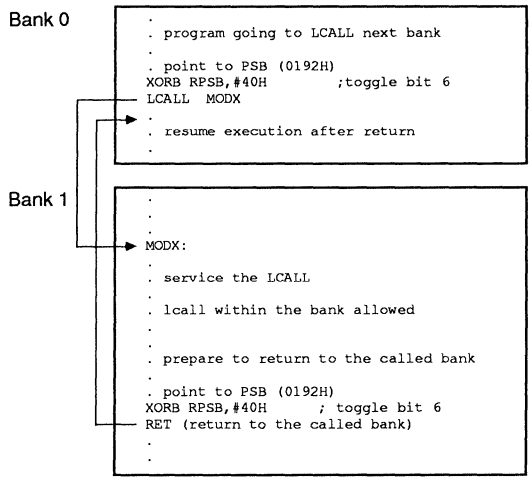


Table 4a. LCALL Across Bank

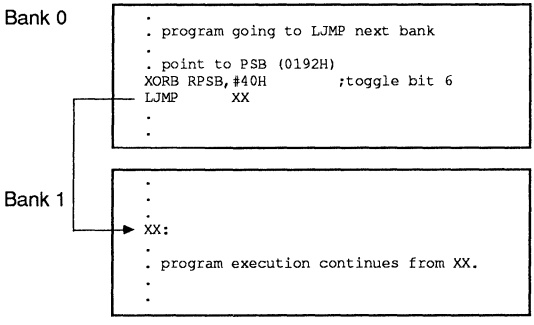


Table 4b. LJMP Across Bank

When an interrupt occurs, the program vectors to internal adddress 2004H. Here the internal firmware performs a PUSHF instruction. If the ROM extension mode is enabled, the PSB bit 6 will be set to 0 to point to external bank 0. The firmware then does an LCALL to external address 8004H. The user interrupt service routine begins here. The last instruction must be "RET" to return the execution to the internal ROM. The firmware executes a "POP" instruction to restore the flags and bank pointer. A "RET" instruction returns the execution to the last address before the interrupt.

```
2004          ORG     INTV
2004                  EINT:
2004   F2             PUSHF                ; SAVE PSB,
                                            ; SET BANK
2005   EF FC 5F       LCALL   INTE         ; BIT TO 0
2008   F3             POPF                 ; JLCALL 8004H
2009   F0             RET                  ; RESTORE PSB
                                            ; RETURN FROM
                                            ; INTERRUPT
```

Table 4c. Interrupt Servicing

ADDRESS	FUNCTION	R/W	BYTES	COMMENTS
0000H-017FH	Internal RAM *	R/W	384	(a)
0180H-019AH	Internal REG*	R/W	24	(b)
1000H-10FFH	External MAP	R/W	256	(c)
1100H-11FFH	External EEPROM	R/W	256	(c)
2000H-20FFH	Internal ROM	RO	256	(d)
4000H-7FFFH	External RAM	R/W	16K	(e)
8000H-FFFFH	External ROM	RO	32K	(f)
1200H-12FFH	External EEPROM	R/W	256	(g)

* These may only be accessed as memory locations (16-bit address) in an indirect mode. For direct addressing a 9th bit (GCR [1], called Page Bit) must be set to switch from the first 256 bytes to the rest of the RAM.

(a) The SC11011,61 have 304 bytes and SC11021 has 320 bytes

(b) The internal register is compatible with the MAC and Big MAC. Registers 194H to 19AH controls the selection of SSCC mode. The SSCC function is completed in firmware.

(c) In the normal mode of operation, the MCS and ECS chip select for MAP and EERAM remain the same as in MAC or Big MAC. A provision is made to extend the ROM capacity by another 32K bytes. If selected, the ECS pin becomes a chip select to address a 32K ROM from 8000H to FFFFH. If extended ROM is used, the address 1100 to 11FF must not be accessed. The EEPROM will be selected using the MCS pin and an external memory decode will select either the MAP or the EEPROM.

(d) Internal ROM size is 256 bytes.

(e) The external RAM address remains the same as the SC11011. It has a maximum addressable space of 16K bytes. With multiplexing using the GPO pin (pin 45), it can address 32K bytes.

(f) The 32K bytes ROM address remains the same as in MAC or Big MAC. With the ECS pin, the ROM address is expanded to a total of 64K bytes.

(g) If extended ROM is used, The EEPROM will be addressed from 1200H to 12FFH. See the hardware configuration section.

(h) SC11011, 1102X, 11061 stack is reset to 302 on power up. SC11091 stack is reset to 320.

REGISTER DESCRIPTION

This section contains a description of each of the registers in the UMAC device. All of the registers of the device are 8-bits with 16-bit addresses. The registers are made up of bits that are either inputs or outputs. Input bits are read-only (RO). Output bits are read/write (R/W). The state of an output may be read back by the processor.

Serial Mode

In parallel mode (CONF = 0) the functions of the UART registers are exactly the same as those in 16C450 UART. However in serial mode, (CONF = 1), the UART is turned around and controlled by the internal processor and it becomes a data set UART. The DTR, RTS, and OUT1 in MCR register becomes DSR, CTS, and RLSD outputs. The CTS, DSR in MSR register become RTS, DTR input status from RTS, DTR pins.

Note:
In serial version to echo SIN to SOUT after RESET and then go back to normal operation.

1. Set "BI" in LCR to "1".
2. Sample RDI in UART monitor register.
3. Set CM = RDI in the same register.
4. SOUT will be the same state as CM.
5. Receiver is functioning, ignoring it.
6. After finishing all echoing, reset "BI" in LCR.
7. Update DLL, DLM, and set CM = 1 for normal operation.
8. Do a SET then RESET to RTRST bit to RESET RCV and TMR. Do a READ to LSR to clear LSR.
9. The UART is ready for normal operation.

Table 5. Register Address MAP

NAME	ABV	INTERNAL[3]			EXTERNAL[6]	
		INDIRECT ADDRESS[4]	DIRECT ADDRESS[5]	R/W	ADDRESS A [2:0]	R/W
UART Registers:						
Receive Buffer[1]	RBR	80H	180H	R/W	00H	RO
Transmit Holding[1]	THR	8AH	18AH	R/W	00H	WO
Interrupt Enable[1]	IER	81H	181H	R/W	01H	R/W
Interrupt ID	IIR	82H	182H	RO	02H	RO
Line Control	LCR	83H	183H	R/W	03H	R/W
Modem Control	MCR	84H	184H	R/W	04H	R/W
Line Status	LSR	85H	185H	R/W	05H	R/W
Modem Status	MSR	86H	186H	R/W	06H	R/W
Scratch Pad (8 bit)	STR	87H	187H	R/W	07H	R/W
Divisor Latch LSB[2]	DLL	88H	188H	R/W	00H	R/W
Divisor Latch MSB[2]	DLM	89H	189H	R/W	01H	R/W
UART Monitor	UMR	8BH	18BH	R/W		
Internal Registers:						
Switch Port	SWP	8DH	18DH	RO		
General I/O Port						
Direction Register	DIR	8EH	18EH	WO		
Data Register	DAR	8FH	18FH	R/W		
General Control	GCR	90H	190H	R/W		
General Control 1	GCR1	94H	194H	R/W		
General Control 2	GCR2	95H	195H	R/W		
TIMER	TIM	91H	191H	R/W		
Processor Status Byte	PSB	92H	192H	R/W		
Interrupt Control	ICR	93H	193H	R/W		
Interrupt Enables	ITEN	99H	199H	R/W		
TX/RX Buffer	TXRX	9AH	19AH	R/W		
Line Status 1	LSR1	96H	196H	R		

[1] DLAB bit (LCR [7]) must be zero for external access.
[2] DLAB bit (LCR [7]) must be one for external access.
[3] Register access through MA bus.
[4] 8-bit addresses for indirect addressing only, with Page bit (GCR [1]) used.
[5] 16-bit addresses for direct addressing only.
[6] UART register access through PC parallel system bus.

ACCESSIBLE UART REGISTERS

The system programmer may access or control any of the UART registers summarized in Table 6 via the CPU. These registers are used to control UART operations and to transmit and receive data. Their reset functions are summarized in Table 7.

Line Control Register (LCR, location 183H)

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 6 and are described in the following table.

Bit No	Register Address										
	0(DLAB=0)	0(DLAB=0)	(DLAB=0)	2	3	4	5	6	7	(DLAB=1)	(DLAB=1)
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Iden. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	STR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2 INT0 is High-Z when out2=0	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Table 6. Summary of Accessible UART Registers

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the programmed number of Stop-bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0, then the Parity bit is transmitted as a 1.

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0–3) forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low, Bit 3–7 are permanently Low
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	"All Bits Low, Except Bits 5 and 6 are High"
MODEM Status Register	Master Reset	"Bits 0–3 Low, Bits 4–7— Input Signal"
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read BRR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read RBR/MR	Low

Table 7. Summary of Accessible UART Registers

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has not effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Generator

The UART contains a programmable Baud Generator that takes an internal clock of (3/32)(XTAL1) = 1.8432 MHz and divides it by any divisor from 1 to (2^{16}–1). The output frequency of the Baud Generator is 16 x the Baud [(divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on the initial load.

Table 8 illustrates the use of the Baud Generator with a crystal frequency of 19.6608 MHz. The accuracy of the desired baud rate is dependent on the crystal accuracy. Communicaiton software writing values to the divisor latches typically expects the input to the UART to be 1.8432 MHz. They will work correctly only if the UMAC input clock is maintained at 19.6608 MHz.

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Error Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.4	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
57600	2	—

Table 8. Baud Rate Generator Divisors

Line Status Register (LSR, location 185H)

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 5 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: The bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is used for factory testing.

Interrupt Identification Register (IIR, location 182H)

The UART has on-chip interrupt capability that allows for flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are

stored in the Interrupt Identification Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts change the IIR, even though they are recorded, until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 9 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 9

Bits 3 through 7: These five bits of the IIR are always logic 0.

UART Interrupt Enable Register (IER, location 181H)

The 8-bit register enables the four types of interrupts of the UART to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 1 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

SSCC Interrupt Enable Register (ITEN location 199H)

B0: Transmit Interrupt Enable. When set high, the transmitter request an interrupt whenever the transmit buffer becomes empty. Default is low after reset.

B1: Receive Interrupt Enable. When set high, the receiver request an interrupt when the Rx Buffer indicates character available. Default is low after reset.

B2 through B7: Unused.

The present architecture allows interrupt to the CPU (if enabled) each time the SCR or SCT clocks change to a 1. Asynchronous receive data can also interrupt the CPU. This relieves the CPU from having to scan the status continously.

IIR

Interrupt Identification Register				Interrupt Set and Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receiver Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (If source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Table 9. Interrupt Identification Register

Modem Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 6 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Bit 1: This bit controls the Request to Send (RTS) output. Bit 1 affects the RTS output in a manner identical to that described above for bit 0.

Bit 2: Out1. Auxiliary user-designated bit. It is connected to MSR[6] (RI) during local loopback.

Bit 3: Out 2. Auxiliary user-designated bit. It is connect to MSR[7] (DCD) during local loopback. When Out2 = 0, INTO pin is Hi-Z.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input: the four MODEM Status Register bits CTS, DSR, DCD and RI are disconnected internally; and the four MODEM Control Register bits DTR, RTS, OUT1 and OUT2 are internally connected to the four MODEM Status Register inputs, and the MODEM Control output pins RLSD, CTS, DSR are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5–7: These bits are permanently set to logic 0.

Modem Status Register (MSR, location 186H)

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU in addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 1 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Read (DDSR) indicator. Bit 1 indicates that the DSR input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI input to the chip has changed from a low to a high state.

Bit 3: This is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the DCD input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send (CTS) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR. Read/Write inparallel mode.

Bit 5: This bit is the complement of the Data Set Ready (DSR) input. If bit 4 of the MCR is set to a 1, this bit is equivalent of DTR in the MCR. Read/Write inparallel mode.

Bit 6: This bit is the complement of the Ring Indicator (RI) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR. Read only.

Bit 7: This bit is the complement of the Data Carrier Detect (DCD) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR. Read/Write in parallel mode. Always = 1 in serial mode.

Scratchpad Register (STR, location 187H)

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Interrupts Enables (ITEN location 199H)

B0 Transmit Interrupt Enable
B1 Receive Interrupt Enable
B2–B7 UNUSED

TX/RX Buffer (TX/RX location19AH)

Transmit and receive bit are communicated through the LSB (B0) of the read and write register.

Line Status 1 (LSR1 location 196H)

B0 SSCC request interrupt
B1 Rx Character available
B2 Tx Buffer Empty
B3–B7 UNUSED

This register contains the status of the transmit and receive buffers. It also include the interrupt status.

B0 SSCC request interrupt. A high indicates that any of the SSCC enabled interrupt sources requested an interrupt. This bit is cleared after this register is read.

B1 Rx bit available. A high indicates that a bit is available in the receive buffer. If the receive interrupt is enabled, an interrupt will be requested. This bit is cleared after this register is read.

B2 Tx Buffer Empty. This bit is set to a "1" when a bit is shifted out of the transmit buffer. If the transmit interrupt is enabled, an interrupt will be requested. It is reset when a character is loaded into the transmit buffer. This bit is set to "1" after a reset.

B3–B7 Unused.

REGISTER DESCRIPTION

UART Monitor (UMR, location 18BH):

The UART Monitor register allows the processor to monitor UART operations. A read operation to the UART Monitor register will clear Bit 0 to Bit 4.

BIT	NAME	DESCRIPTION
7	RTRST	Reset receiver and transmitter. When set high both receiver and transmitter will be put into reset state.
6	CM	UART Command/Modem Output. When set HIGH the UART is placed in modem mode. At reset it is low, in command mode. This bit together with BI in LCR are used for bit by bit echoing. In serial version the user can set BI = 1 and CM = $\overline{RDI}$ to echo a bit. When CONF = 1 for normal operation set CM = 1.
5	RDI	Receive Data Input. This bit monitors the RXD input of the UART.
4	DLF	Divisor Latch Flag. This bit indicates if a new baud rate count has been written to the Divisor Latch.
3	LCF	Line Control Flag. This bit indicates if the line control register has been written.
2	TXF	Transmit Buffer Full Flag. This bit indicates if a new character is in the transmit shadow register.
1	RXF	Receive Buffer Empty Flag. This bit indicates if the last character has been read from the receive buffer.
0	MCF	Modem Control Flag. This bit indicates if the modem control register has been written.

Internal Registers:

Switch Port (SWP, location 18DH): for serial version only

The Switch Port is a 7-bit input port used only in the serial version of the MAC. It allows for reading of the external switches of a stand-alone modem. Only S0–S2 are available on the 44 pin SC11020CV.

BIT	NAME	DESCRIPTION
6–0	S 6–0	Switch Input. These bits monitor external switches.

General I/O Port (GIO)

Direction Register (DIR, location 018EH):

BIT	NAME	DESCRIPTION
7	Unused	N/A
6	Unused	N/A
5	Unused	N/A
4	Unused	N/A
3	DIR3	When HIGH, GPO/IO3 is an output. When LOW, GPO/IO3 is an input.
2	DIR2	When HIGH, IO2 is an output. When LOW, IO2 is an input.
1	DIR1	When HIGH, IO1 is an output. When LOW, IO1 is an input.
0	DIR0	When HIGH, IO0 is an output. When LOW, IO0 is an input.

REGISTER DESCRIPTION

General I/O Port (GIO) (Cont.)

Data Register (DAR, location 018FH):

BIT	NAME	DESCRIPTION
7	Unused	N/A
6	Unused	N/A
5	DAR5	This bit is routed to TDOUT pin when DAR4 is set HIGH.
4	DAR4	When set HIGH, DAR5 is output to TDOUT pin. When set LOW, SOUT or SIN is output to TDOUT pin when GCR bit 7 (CONF) is set LOW or HIGH respectively. See Figure 11.
3–0	DAR3–0	Output to IO3–0.

Timer (TIM, location 191H):

The Timer includes an 11 bit counter and a timer flip-flop. It is used to aid software timing functions. The counter is readable only in autobaud mech (GCR2.6 = 1. See Hardware Autobaud section). It can only be reset by a write.

The timer flip-flop can be read to test if it is already set.

The counter and flip-flop will be reset on a write (value is don't care). After that the counter sends out a pulse train at 4.8 kHz rate to set the timer flip-flop. The flip-flop can be cleared on a read. The Timer is constantly counting by the internal clock (9.8304 MHz).

BIT	NAME	DESCRIPTION
0	TFF0	Timer flip-flop bit.
1–7	TFF1–7	Seven bit autobaud timer result if GCR2.6 = 1.

General Control Register (GCR, location 0190H):

GCR contains a miscellaneous set of control and status bits.

BIT	NAME	DESCRIPTION
7	CONF	Configuration output. This bit controls the state of the MAC configuration. When HIGH, the MAC is configured with the SERIAL interface. It is configured with the PARALLEL interface after a reset.
6	OH	Off Hook Output. When set HIGH, the phone will be placed off hook.
5	KDV	KDV Output. Data/Voice Relay Control. When high, the modem is in the voice mode.
4	MRDY	Modem ready.
3	AA	Active HIGH AA indicator. When high this bit sets the $\overline{AA}$ pin low.
2	HS	Active HIGH HS indicator. When high this bit sets the $\overline{HS}$ pin low.
1	PAGE	Register Page Bit. This bit selects the active register page. When LOW, the lower 256 registers are accessed during register operations and when HIGH, the upper page is active.
0	PD	Power Down Mode.

General Control 1 (GCR1 location 0194H)

BIT	NAME	DESCRIPTION
B0	SSCC	SSCC select
B1, B2	USART	USART modes
0 0	SDLC	SDLC
1 0		BISYNC
0 1		MONOSYNC
1 1		ASYNC
B3		XUART
B4		SSCC LOCAL LOOPBACK
B5		SSCC AUTO ENABLE
B6		SCTI SCRI CONNECT
B7		GPO/IO3

This register controls the switching between the SSCC and the UART (in MAC or Big MAC), and selects the SSCC modes.

B0 SSCC select. When high, the SSCC is connected to the MAP for MNP operation. Default is low after reset.

B1, B2 SSCC modes: The SSCC defaults to synchronous mode if B1 and B2 are not set to high. The program can use this as a flag when performing the function of the software SSCC by reading the status of these 2 bits. For async mode B1 and B2 must be set high.

0 0 Indicate SDLC mode select.
1 0 Indicate BISYNC mode select.
0 1 Indicate MONOSYNC mode select.
1 1 ASYNC.

B3 XUART. When high, the UART is disconnected from the SIN and SOUT pin. These 2 pins can then be used for general purpose IO.

B4 SSCC LOCAL LOOPBACK. When high, the internal transmitted data is routed back to the receiver as well as to the Tx output pin. Default is low after reset.

B5 SSCC AUTO ECHO ENABLE. When high, signal into the Rx pin is routed to the Tx pin but the receiver still listens to the Rx input. Transmitted data from the SSCC is not routed to the Tx pin. Default is low after reset.

B6 SCTI SCRI CONNECT . When high, the transmit clock input SCTI drives the receive clock internally. The SCRI serves as a general purpose input and its state is readable in DAR1 (Bit 2, reg 18FH in Big MAC). Default is low after reset.

B7 GPO. The state of this bit sets the general purpose output port at pin GPO. This bit can be used to indicate SSCC operation or bank switching of the external RAM. Default is low after reset.

General Control 2 (GCR2 location 0195H)

B0, B1	OSCILLATOR DIVIDE
0 0	OSC DIV 3
1 0	OSC DIV 4
0 1	OSC DIV 2
1 1	OSC DIV 2.5
B2, B3	**TIMER FREQUENCIES**
0 0	4800 Hz timer
1 0	9600 Hz timer
0 1	19200 Hz timer
1 1	38400 Hz timer
B4	ROM CONFIG
B5	ROM EXTENSION ACTIVATE
B6	AUTOBAUD
B7	NORDY

Clock divide for crystal oscillator, timer frequency, and SSCC modes are selected in this register.

B0, B1 OSCILLATOR DIVIDE
0 0 OSC DIV 3. For 29.4912 MHz crystal.
0 1 OSC DIV 2. For 19.6608 MHz crystal. This is the default after reset.
1 0 reserved
1 1 reserved

B2, B3 TIMER FREQUENCIES
0 0 4800 Hz TIMER . Timer interrupts once every 208.33uS. This is the default state.
1 0 9600 Hz TIMER . Timer interrupts once every 104.16uS.
0 1 19200 Hz TIMER . Timer interrupts once every 52.08 uS.
1 1 38400 Hz TIMER . Timer interrupts once every 26.04 uS.

B4 ROM CONFIG. This bit determines the configuration for the extended ROM. If this bit is 0, two 32K x 8 ROMS are used. If this bit is 1, a single 64K x 8 ROM is used. Refer to Figure 7 for clarification. Default is low after reset.

***B5** ROM EXTENSION ACTIVATE. This bit should be set high to activate bank switching. Default is low after reset.

B6 AUTOBAUD. When set high, autobaud mode is selected. Default is low after reset.

B7 NORDY. When set high, the parallel interface operates without the need of the RDY pin.

SC11091 SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

V_{CC} Supply Voltage	+6 V
Input Voltage	–0.6 V to V_{CC} +0.6 V
Storage Temperature Range	–65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range	0 to 70°C

DC ELECTRICAL CHARACTERISTICS: (T_A = 0 TO 70°C, V_{CC} = +5 V +10%)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I_{CC}	Nominal Operating Current @ V_{CC} = 5.5 V		40	75	mA
I_{CCPD}	Power Down Current @ V_{CC} = 5.5 V		8	15	mA
V_{IH}	High Level Input Voltage for TTL input pins for CMOS input pins	 2 0.8 V_{CC}			 V V
V_{IL}	Low Level Input Voltage for TTL input pins for CMOS input pins			 0.8 0.2 V_{CC}	 V V
VT+	Positive Hysteresis Threshold for RESET & /RI input pins		2.5		V
VT–	Negative Hysteresis Threshold for RESET & /RI input pins		1.8		V
V_{OH}	High Level Output Voltage for D7–D0, into @ I_{OH} = 8 mA for RDY—open collector for other output @ I_{OH} = 2 mA	 0.7 V_{CC} +0.5			 V
V_{OL}	Low Level Output Voltage for D7–D0, into pins @ I_{OL} = 8 mA for RDY @ I_{OL} = 8 mA for other output pins @ I_{OL} = 2 mA			 0.3 V_{CC} –0.5	 V
I_1	Leakage Current		±1	±20	µA
F_{CLK}	Crystal Clock Frequency (GCR2:0, 1 - 01)		19.6608		MHz
F_{CLK}	Crystal Clock Frequency (GCR2:0, 1 - 00)		29.4912		MHz

TIMING DIAGRAMS

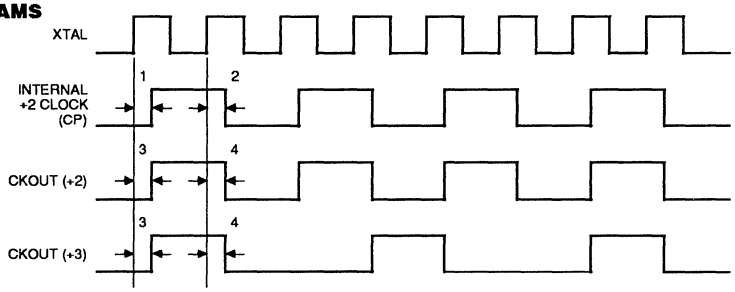


Figure 8. Oscillator, Internal (÷2) Clock and CKOUT Timing

NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TXTCPH	XTAL high to internal ÷2 clock high			20	ns
2	TXTERL	XTAL high to internal ÷2 clock low			20	ns
3	TXTCKH	XTAL high toCKOUT high			30	ns
4	TXTCKL	XTAL high toCKOUT low			30	ns

*Note: CP is the internal ÷2 clock. CP = 102 ns for 19.6608 MHz crystal or 68 ns for 29.4912 MHz crystal.

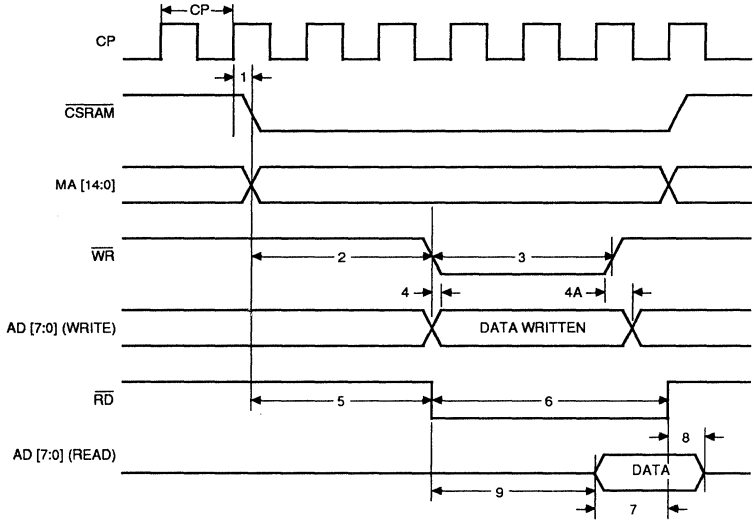


Figure 9. RAM Read or Write Cycle

NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TCPCSR	CP to CSRAM low			20	ns
2	TCSRWR	CSRAM low to WR low		2.5		cp
3	TRW	WR width		2.5		cp
4	TWRADV	WR low to data valid			5	ns
4a	TWRADI	WR high to data invalid		.5		cp
5	TCSRRD	CSRAM low to RD low		2.5		cp
6	TRD	RD width		3.5		cp
7	TADVCL	Read set up time	20			ns
8	TCLADI	Read hold time	0			ns
9	TRLDV	Read low to data valid 29.4912 MHz 19.6608 MHz			170 320	ns ns

*Note: CP = 102 ns for 19.6608 MHz XTAL & 68 ns for 29.4912 MHz crystal.

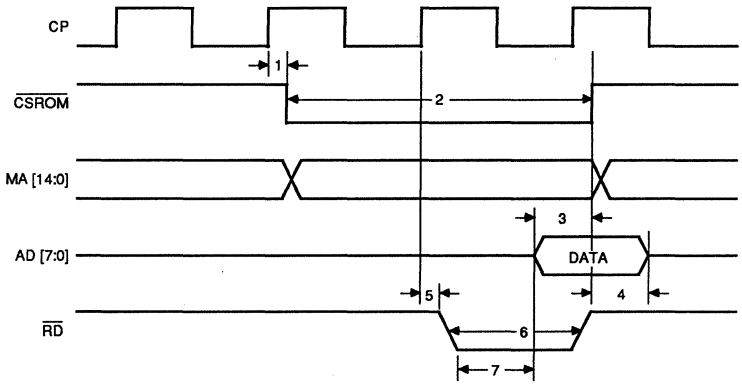


Figure 10. External Program Storage Read Bus Cycle

NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TCPCRM	CP to CSROM low			20	ns
2	TCSROM	CSROM width		2		cp
3	TCSRAD	Read setup time	20			ns
4	TCSRDH	Read hold time	0			ns
5	TCPRD	CP to RD low			20	ns
6	TRD	RD width		1		cp
7	TADDV	Address valid to data valid 29.4912 MHz 19.6608 MHz			110 170	ns ns

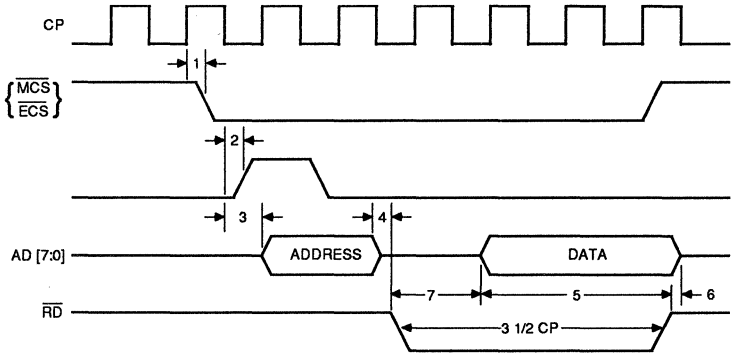


Figure 11. MAP and EERAM Read

NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TCHCSL	CP high to MCS, ECS low			20	ns
2	TCLALH	CP high to ALE high			12	ns
3	TCLAV	CP low to address valid			16	ns
4	TCLAI	CP low to address invalid	4			ns
5	TADVCL	Read set up time	20			ns
6	TCLADI	Read hold time	0			ns
7	TRLDV	Read low to data valid 29.4912 MHz 19.6608 MHz			200 320	ns ns

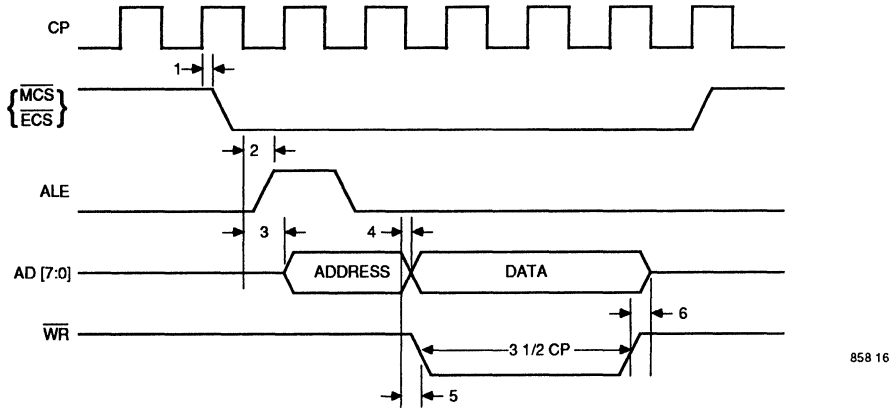


Figure 12. MAP and EERAM Write Cycle

NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TCHCSL	CP high to MCS, ECS low			20	ns
2	TCLALH	CP low to ALE high			12	ns
3	TCLAV	CP low to address valid			16	ns
4	TCLDV	CP low to data valid			4	ns
5	TCLWRL	CP low to $\overline{WR}$ low			20	ns
6	TWRADI	WR high to data invalid			.5	cp

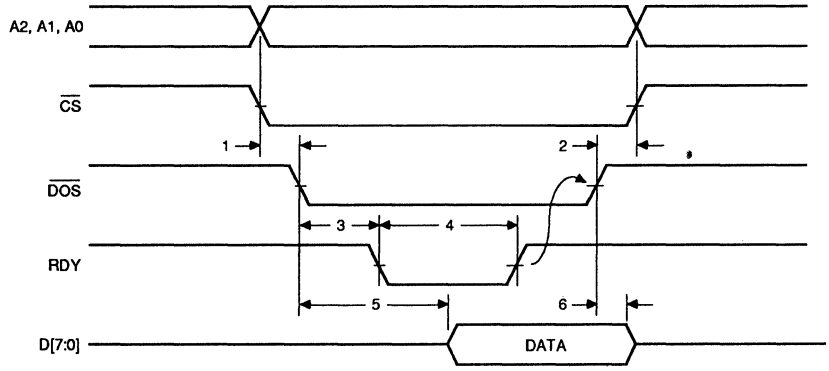


Figure 13. Write Cycle (PC Bus Write Into UART Register)

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDOL	$\overline{CS}$ low to $\overline{DOS}$ low				0	ns
2	TDOHCSH	$\overline{DOS}$ high to $\overline{CS}$ high				0	ns
3	TDOLRDL	$\overline{DOS}$ low to RDY low				26	ns
4	TRDL	RDY low time (~5–6CP)		330		400	ns
5	TDOLDV	$\overline{DOS}$ low to D valid				200	ns
6	TDOHDZ	$\overline{DOS}$ high to D high-Z		0			ns

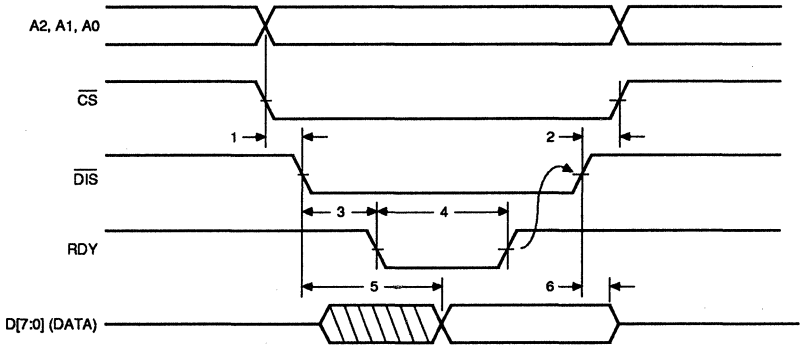


Figure 14. Read Cycle (PC Bus Read From UART Register)

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDIL	$\overline{CS}$ low to $\overline{DIS}$ low				0	ns
2	TDIHCSH	$\overline{DIS}$ high to $\overline{CS}$ high				0	ns
3	TDILRDL	$\overline{DIS}$ low to RDY low				26	ns
4	TRDL	RDY low time (~5–6CP)		330		400	ns
5	TDILDV	$\overline{DIS}$ low to D valid				180	ns
6	TDIHDZ	$\overline{DIS}$ high to D high-Z				12	ns

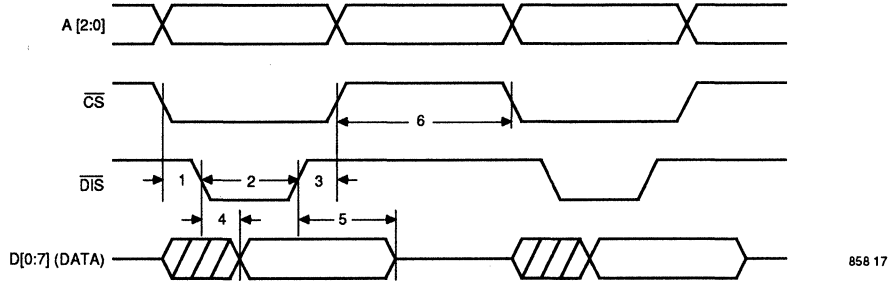


Figure 15. Read Cycle (No Ready Mode) (PC Bus Read From UART Register)

NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TCSLDIL	$\overline{CS}$ low to $\overline{DIS}$ low			0	ns
2	TDIS	$\overline{DIS}$ width	80			ns
3	TDIHCSH	$\overline{DIS}$ high to $\overline{CS}$ high			0	ns
4	TDILDV	$\overline{DIS}$ low to D valid			40	ns
5	TDIHDZ	DIS high to high-Z			12	ns
6	TCYCRD	Wait time before next access	2			cp

*Note: CP is +2 clock

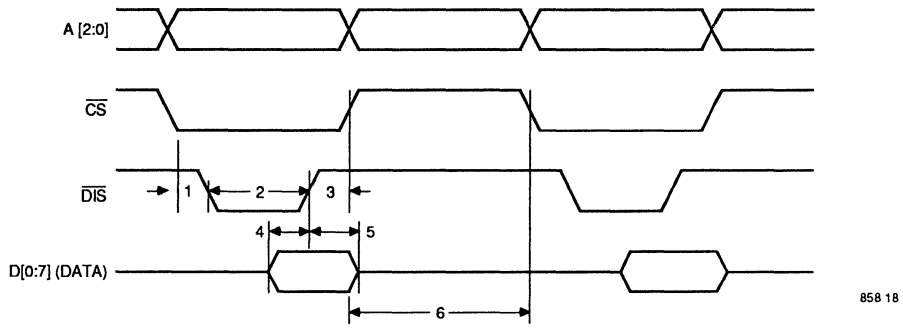


Figure 16. Write Cycle (No Ready Mode) (PC Bus Read Into UART Register)

NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TCSLDOL	$\overline{CS}$ low to $\overline{DOS}$ low			0	ns
2	TDOS	$\overline{DOS}$ width	80			ns
3	TDOHCSH	$\overline{DOS}$ high to $\overline{CS}$ high			0	ns
4	TDSUP	Data set up time	20			ns
5	TDHLD	Data hold time	0			ns
6	TCYCWRD	Wait time before next access	2			cp

*Note: CP is internal +2 clock

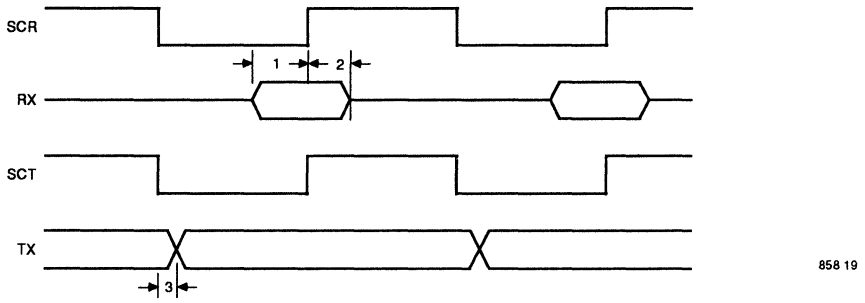


Figure 17. Single Bit USART Read and Write Timing

NO.	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	TRXSH	Bit set up time	20			ns
2	TRXHD	Bit hold time	0			ns
3	TTXBIT	XCT low to bit out			30	ns

THE UMAC AND INTEL 8096 SPEED COMPARISON

The attached is an instruction execution time comparison for the UMAC and Intel 8096. The biggest improvement over 8096 is the 16 bit multiplication; it is 2 μs versus 6.5 μs. The jump instructions are twice as fast. The shift instructions are also about twice faster. The other arithmetic and logic instructions are about the same speed. Indirect addressing instructions in the UMAC is about 20% slower than in the 8096.

The following comparison is for the 8096 with 12 MHz crystal and the UMAC with 29.4912 MHz. The time unit is "μs". The instructions and operands are all from internal storage. Both the UMAC and Intel 8096 will run slower for external storage access.

		DIRECT		IMMEDIATE		INDIRECT	
INSTRUCTION	OPERANDS	UMAC	8096	UMAC	8096	UMAC	8096
ADD	2	.680	1.00	.81	1.25	1.29	1.50
ADD	3	.680	1.25	.81	1.50	1.29	1.75
ADDB	2	.680	1.00	.68	1.00	1.29	1.50
ADDB	3	.680	1.25	.68	1.25	1.29	1.75
AND	2	.680	0.75	.81	1.25	1.29	1.50
AND	3	.680	1.00	.81	1.50	1.29	1.75
ANDB	2	.680	1.00	.68	1.00	1.29	1.50
ANDB	3	.680	1.25	.68	1.25	1.29	1.75
CMP	2	.680	1.00	.81	1.25	1.29	1.50
CMPB	2	.680	1.00	.68	1.00	1.29	1.50
DJNZ		.61/.83	1.25/2.25	(NO JUMP/JUMP)			
EXTB		.47	1.00				
JBC		.68/.88	1.25/2.25				
JBS		.68/.88	1.25/2.25				
JC		.34/.55	1.00/2.00				
JE		.34/.55	1.00/2.00				
JGE		.34/.55	1.00/2.00				
JGT		.34/.55	1.00/2.00				
JH		.34/.55	1.00/2.00				
JLE		.34/.55	1.00/2.00				
JLT		.34/.55	1.00/2.00				
JNC		.34/.55	1.00/2.00				
JNE		.34/.55	1.00/2.00				
JNH		.34/.55	1.00/2.00				
JNV		.34/.55	1.00/2.00				
JV		.34/.55	1.00/2.00				
LCALL		.75	3.25				
LD	2	.68	1.00	.81	1.25	1.29	1.50
LDB	2	.68	1.00	.68	1.00	1.29	1.50
LJMP	1	.61	2.00	.68	1.00	1.29	1.50
MUL	3	2.24	6.50	(BIGGEST IMPROVEMENT)			
NOP		.16	1.00				
OR	2	.68	1.00	.81	1.25	1.29	1.50
ORB	2	.68	1.00	.68	1.00	1.29	1.50
PUSHF		.34	2.00				
POPF		.34	2.25				
RET		.68	3.00				
SHL		.75+0.66N	1.75+0.25N	(N = SHIFT COUNT)			
SHLB		.75+0.66N	1.75+0.25N				
SHLL		1.02+0.66N	1.75+0.25N				
SHR		.75+0.66N	1.75+0.25N				
SHRB		.75+0.66N	1.75+0.25N				
SHRL		1.02+0.66N	1.75+0.25N				
SHRA		.68+0.66N	1.75+0.25N				
SHRAL		1.02+0.66N	1.75+0.25N				
SJMP		.47	2.00				
ST		.88	1.75				
STB		.88	1.75				
SUB	2	.68	1.00	.81	1.25	1.29	1.50
SUBB	2	.68	1.00	.68	1.00	1.29	1.50
SUB	3	.68	1.25	.81	1.50	1.29	1.75
SUBB	3	.68	1.25	.68	1.25	1.29	1.75
XOR	2	.68	1.00	.81	1.25	1.29	1.50
XORB	2	.68	1.00	.68	1.00	1.29	1.50

APPLICATION NOTES

The SC11091CV UMAC was designed to perform the DSP and control functions for a wide range of Sierra Modem Advanced Peripherals (MAPs) including Sendfax, Quatro and facsimile data pumps. The UMAC is specifically aimed at V.42bis applications where the ability to address a 32K x 8 SRAM dictionary is required. It also provides an expanded ROM address capacity to allow other powerful combinations. As an application specific Controller, the UMAC has several features specific to the Modem functions including hardware autobaud, V.23 multiplexer and a serial synchronous communication circuit (SSCC) to efficiently handle synchronous protocols such as MNP and V.42.

The firmware to support the DSP and Controller functions, including extended AT commands, MNP, V.42bis and T.30 fax handshaking are available from Sierra in modular form for easy maintenance and upgrading.

The schematics on the following pages show detailed schematics with all components needed to build a V.42bis 2400 bps modem for internal PC bus or external standalone applications. Additional configurations are avilable from Sierra including EIA Class 2 Dat plus fax modems, pocket and lap-top models.

Figure 18 shows the core of the modem. The UMAC interfaces directly with ROM, RAM, EEPROM and MAC. No buffers or latches are required. U7A is not needed if the optional EEPROM is omitted. The crystal shown for 29.4912 MHz operation is a third overtone, parallel resonant type designed for 12pF load and 5.5pF shunt capacitance. Suggested sources are indicated in Figure 23.

The interface circuit for RS232 (V.24) serial interface and standalone modems is shown in Figure 19. The power on reset circuit is also indicated. This circuit is risetime sensitive. In some applications it may be necessary to increase the value of C. With worst case power supply ramp up, the reset signal should rise above the RESET threshold for a minimum of 600µs. During power down mode the LEDs may be shut off by the controller firmware to reduce power.

For internal PC Bus (parallel) interface, refer to Figure 20. The bi-directional buffer is required to interface the CMOS controller with standard PC bus. In some applications where the loading is controlled (e.g. Laptops) the buffer may not be needed. Power from the PC should be carefully filtered for optimum performance. Separate digital and analog grounds on the board should be commoned close to the edge connector and decoupling capacitors.

Data Access Arrangement and Speaker interface are shown in Figure 21 for both standalone and internal modems. Ferrite beads on the phone line input help to reduce noise input and RF conduction.

Figure 22 illustrates a typical power supply for the standalone modem. Note that the -5V supply is not required with many of Sierra's modem chips. The ±10V supply is for the RS232 drivers.

For optimum performance at low received signal levels with low S/N ratios, it is important to use the recommended power supply decoupling circuit as shown in the figures.

Small inductors in series with the supplies help suppress RFI as well as improve the power supply noise rejection capability of the MAP. A 10Ω, 1/4W resistor in place of, or in series with, the inductor in the MAP power lead has been found to be helpful in computer based products or where the power supply is particularly noisy.

The 10µF capacitors should be a tantalum type while the 0.1µF capacitors should have good high frequency rejection characteristics—monolithic ceramic types are recommended. It is important to locate the decoupling capacitors as close to the actual power supply pins of the chips as possible. It is also recommended that the analog ground and digital ground buses be routed separately and connected at the common ground point of the power supply.

For maximum power down efficiency in parallel configuration, the CS input should be fully decoded or coded with RD or WR inputs.

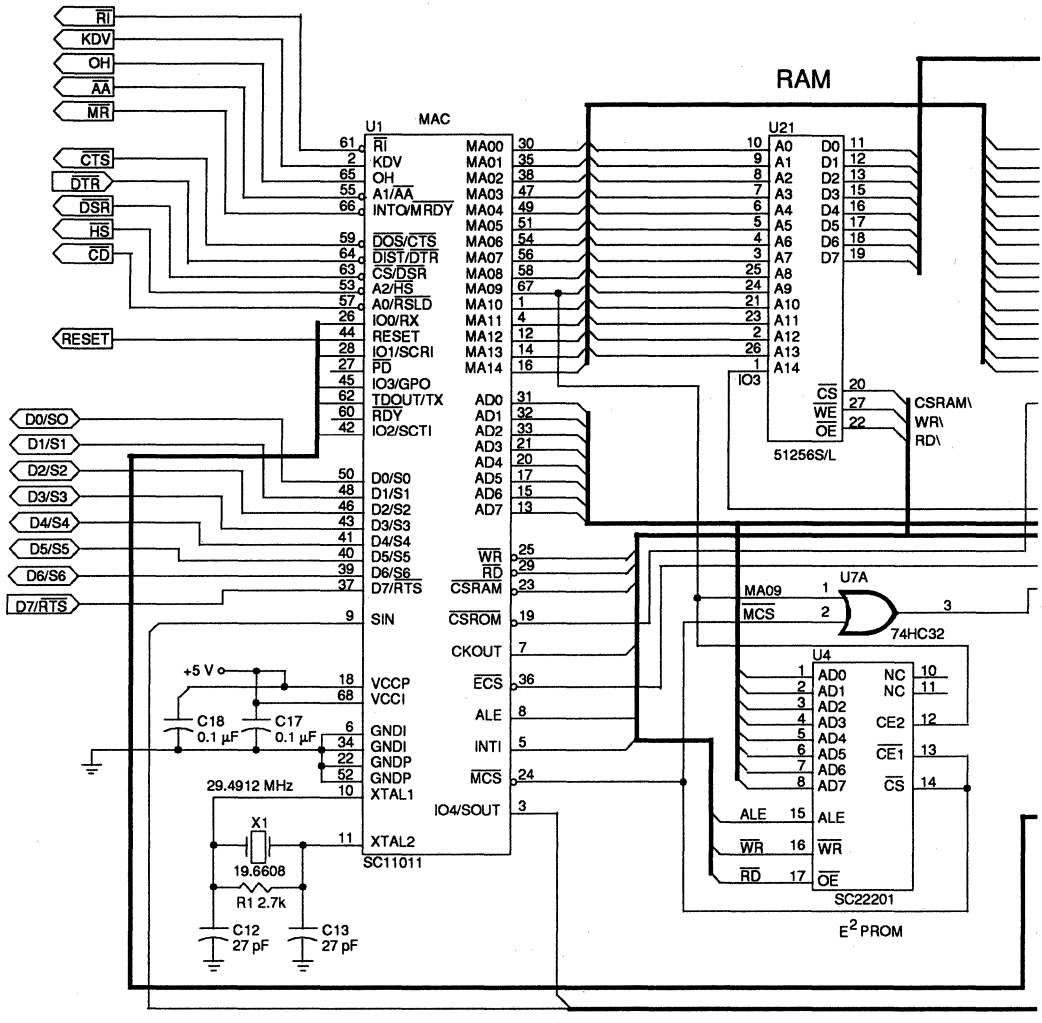
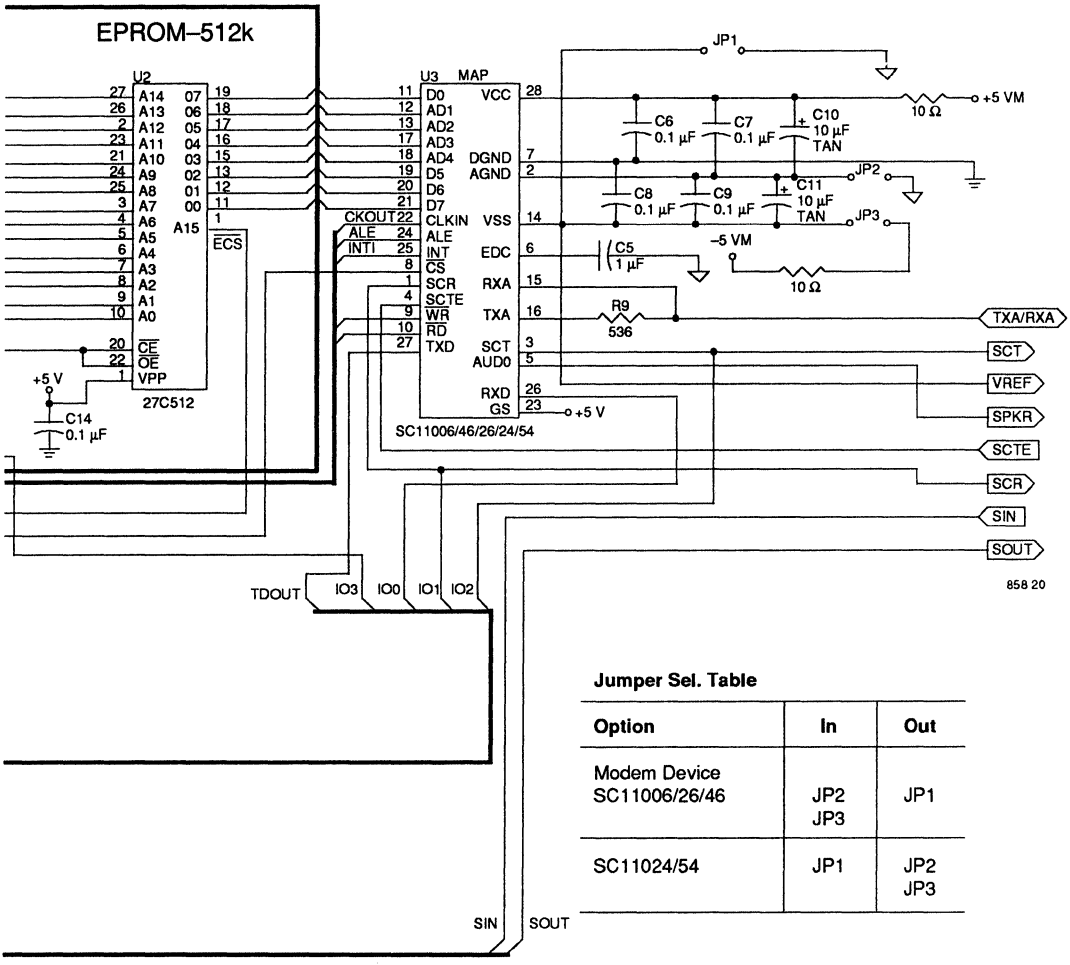

RAM
MAC
U1
U21
51256S/L
SC11011
SC22201
E2 PROM
74HC32
U7A
U4
RI
KDV
OH
AA
MR
CTS
DTR
DSR
HS
CD
RESET
D0/SO
D1/S1
D2/S2
D3/S3
D4/S4
D5/S5
D6/S6
D7/RTS
+5 V
C18 0.1 µF
C17 0.1 µF
29.4912 MHz
X1
19.6608
R1 2.7k
C12 27 pF
C13 27 pF
CSRAM\
WR\
RD\

Figure 18.



Jumper Sel. Table

Option	In	Out
Modem Device SC11006/26/46	JP2 JP3	JP1
SC11024/54	JP1	JP2 JP3

V.42bis and MAP Modem with optional Sendfax

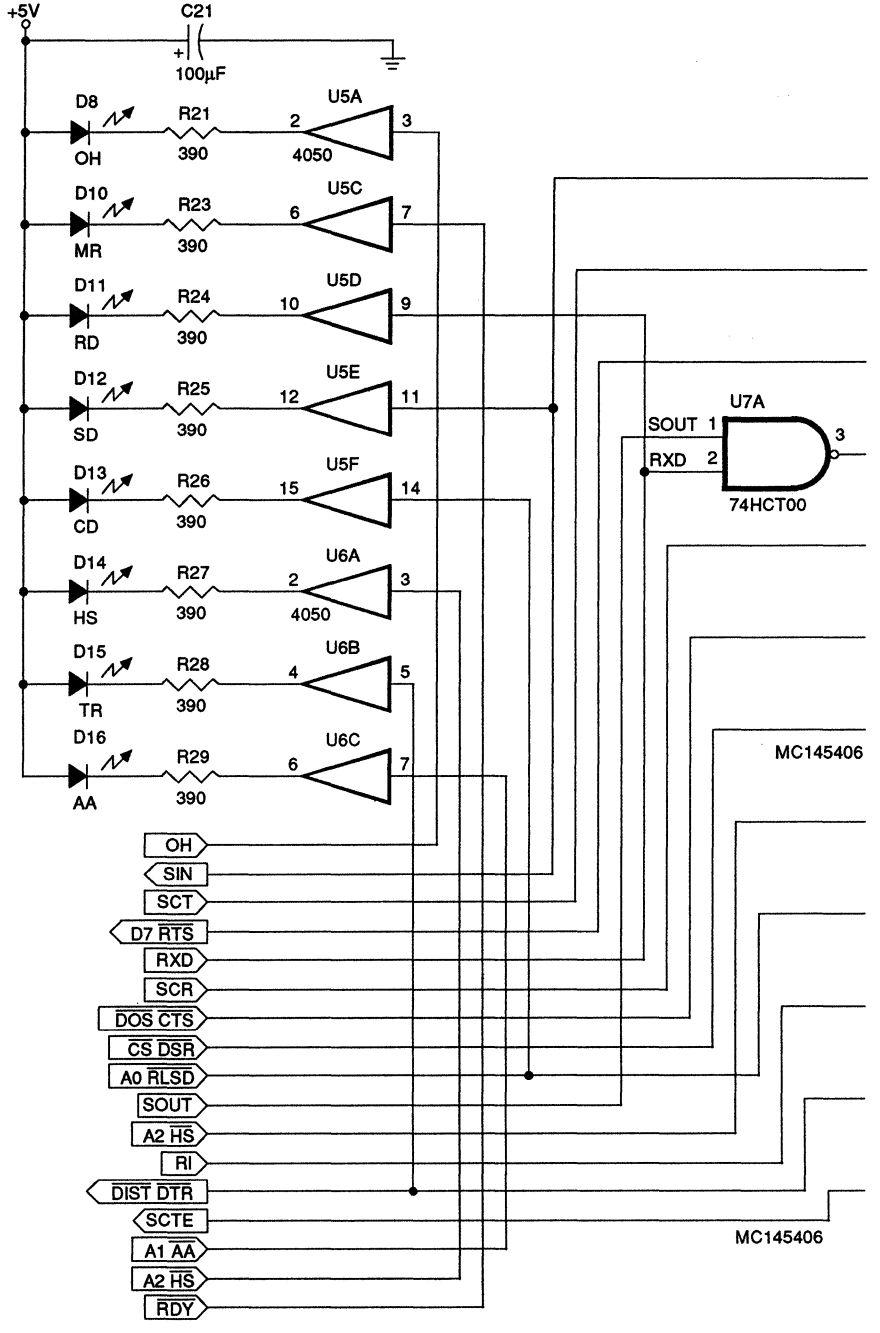
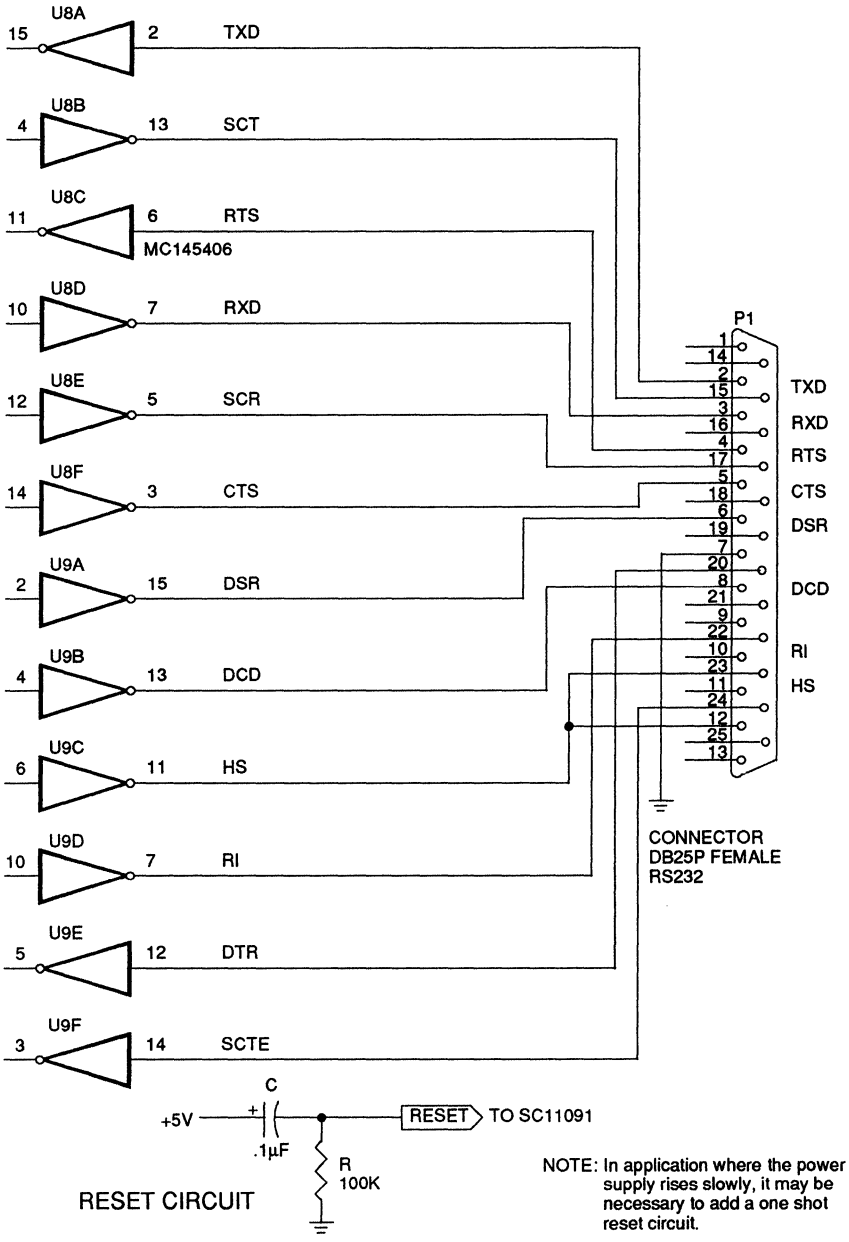

+5V
C21
100µF
D8
R21
390
OH
U5A
2
3
4050
D10
R23
390
MR
U5C
6
7
D11
R24
390
RD
U5D
10
9
D12
R25
390
SD
U5E
12
11
D13
R26
390
CD
U5F
15
14
D14
R27
390
HS
U6A
2
3
4050
D15
R28
390
TR
U6B
4
5
D16
R29
390
AA
U6C
6
7
U7A
SOUT 1
RXD 2
3
74HCT00
MC145406
MC145406
OH
SIN
SCT
D7 RTS
RXD
SCR
DOS CTS
CS DSR
A0 RLSD
SOUT
A2 HS
RI
DIST DTR
SCTE
A1 AA
A2 HS
RDY

Figure 19.



Serial Interface (RS232) (continued)

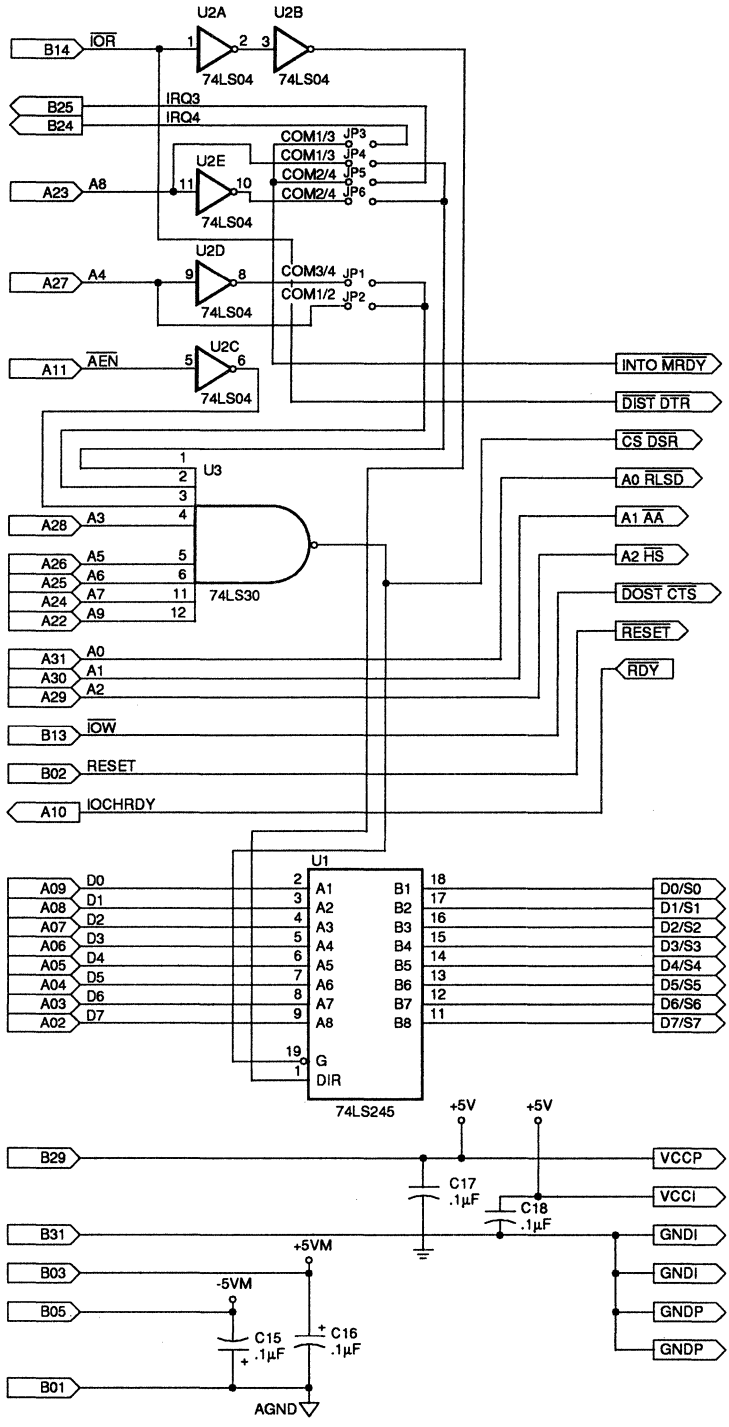


Figure 20. Parallel Bus Interface

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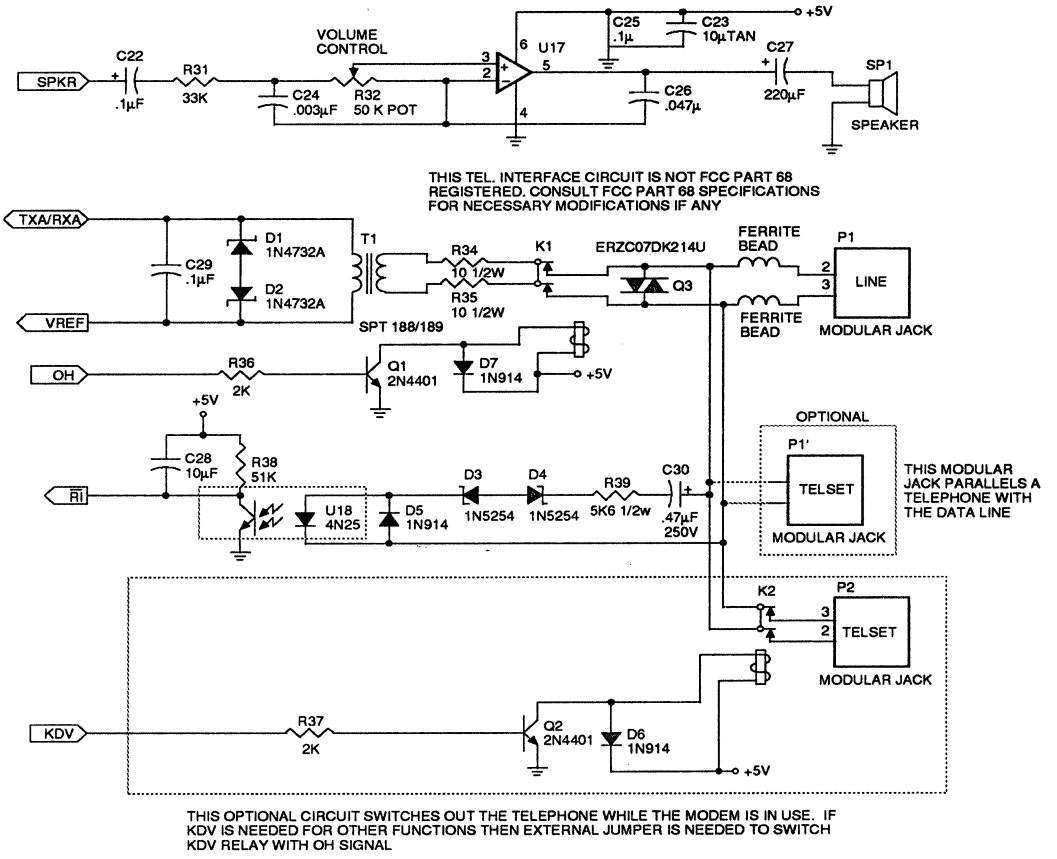


Figure 21. Audio & Telephone Interface Circuit

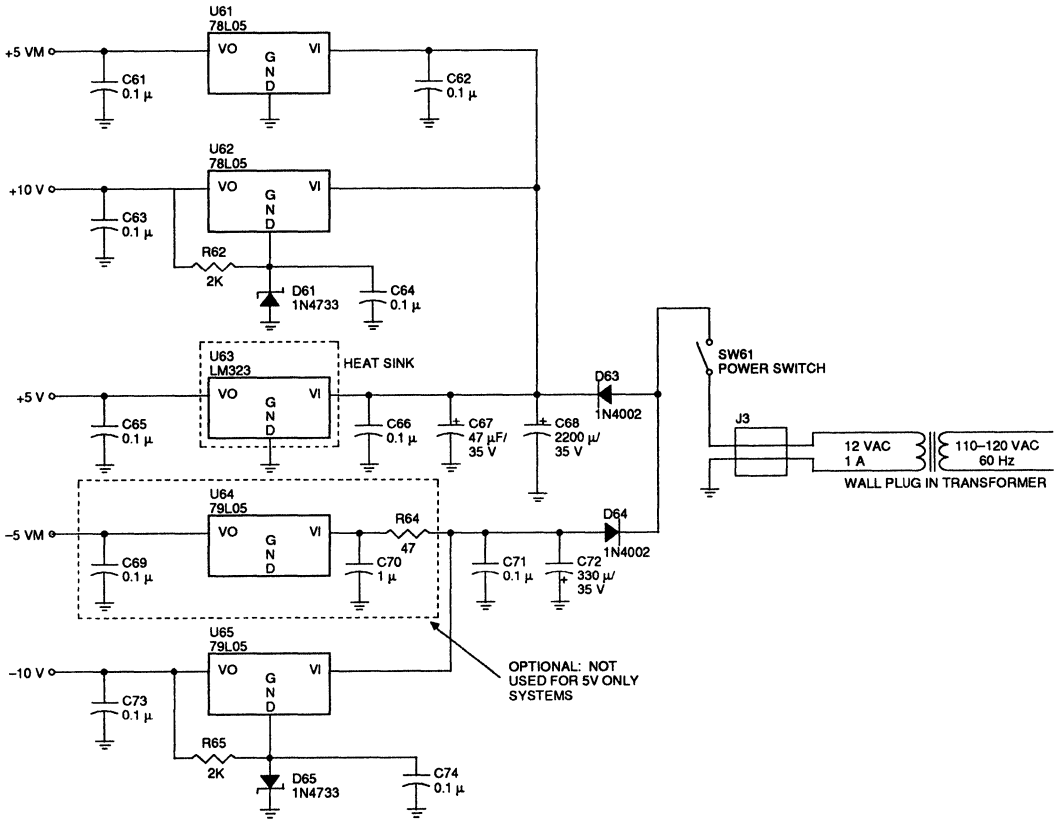
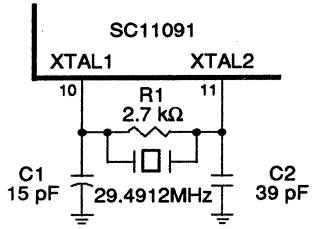


Figure 22. A Typical Power Supply for a Standalone Modem

The suggested crystal for the SC11091 is a third overtone parallel resonant unit with the following specifications:

Frequency: 29.4912 MHz ± 50 ppm
Load Capacitance: 12 pF
Shunt Capacitance: 5.5 pF



Note: 3rd Overtone crystals take longer to stabilize than fundamental crystals.
It may be necessary to increase the time constant of the reset circuit on pin 44 to accomodate this.

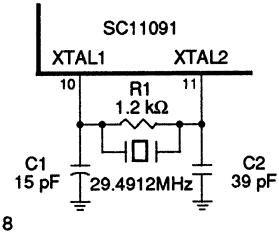
Figure 23a. Crystal Oscillator Schematic and Sources

The following suppliers offer such a crystal:

Savoy Electronics Inc.
1175 N.E. 24 Street
P.O. Box 5727
Ft. Lauderdale, FA 33310
Phone: (305) 563-1333
Fax: (305) 563-1378
Part No: J5P312A8-29.4912
Case No: HC 49/V

SaRonix
4010 Transport at San Antonio
Palo Alto, CA 94043
Phone: (415) 856-6900
(800) 227-8974
Part No: SRX3860
Case No: HC 49/V

Frequency: 19.6608 MHz ± 50 ppm
Load Capacitance: 18 pF
Shunt Capacitance: 7 pF



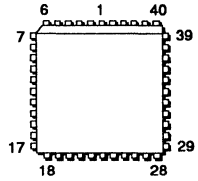
SaRomix Part Po. NYp196-18

Figure 23b. Crystal Oscillator Schematic and Sources

FEATURES

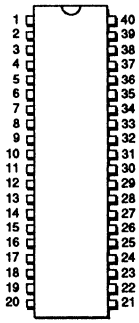
- ☐ ±5 V CMOS technology
- ☐ 7th order receive low-pass filter
- ☐ Adaptive hybrid function for near-end echo cancellation
- ☐ Support multi-mode modems from 300 bps to 14.4 kbps
- ☐ Supports voice processing
- ☐ Serial DSP interface compatible with TMS320-25 series
- ☐ Band split filters for V.22, V.22 bis, V.21, V.23 and 103 modes with 55 dB minimum adjacent band rejection
- ☐ 0–12 dB coarse PGC (programmable gain control) in the receive path
- ☐ 12-bit ADC for echo cancelling and adaptive hybrid training
- ☐ 0–48 dB, 128 step PGC in the receive path
- ☐ 12-bit ADC for receive signal
- ☐ Programmable energy detect circuit
- ☐ 12-bit DAC for transmit and echo canceller
- ☐ 7th order low-pass reconstruction filter with sin x/x correction for the transmit signal
- ☐ 0–15 dB programmable attenuation for the transmit signal
- ☐ Means for line audio monitoring
- ☐ Analog and digital loopbacks

44-PIN PLCC PACKAGE



SC11296CV

40-PIN DIP PACKAGE



SC11296CN

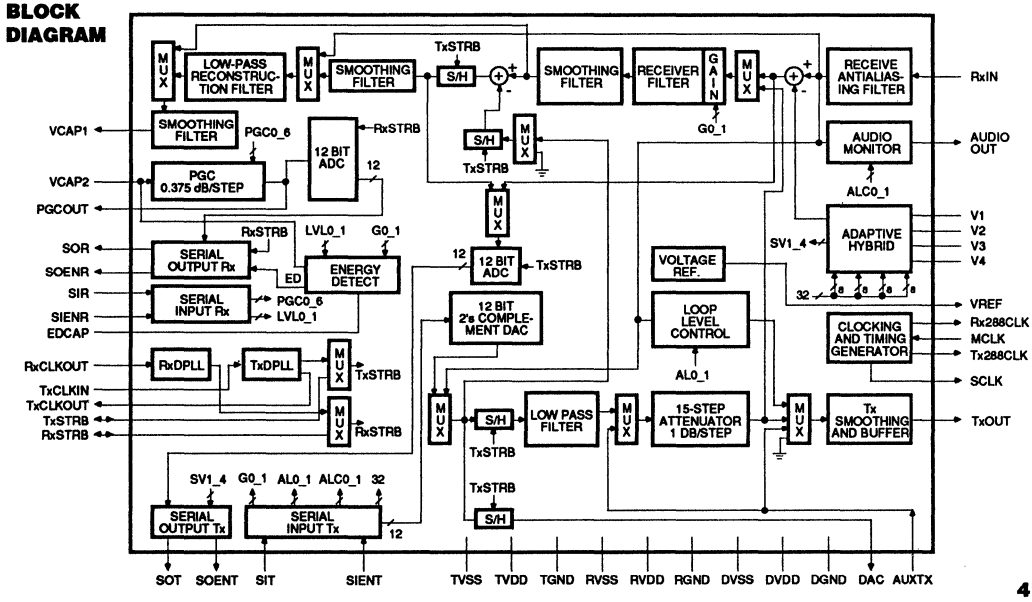
GENERAL DESCRIPTION

This Modem Analog Front End (MAFE) can be used with a digital signal processing unit to implement high speed, 2-wire, full duplex, echo cancelling modems based on CCITT V.32 recommendations. It is also capable of operating in 4-wire full duplex, 2-wire half duplex and 2-wire full duplex modes based on CCITT V.26, V.27, V.27 ter/bis, V.29, V.33, V.32 bis, V.22 bis, V.22, V.23, V.21 and Bell 103 recommendations.

One of the main features of the chip is the inclusion of means to implement an adaptive hybrid. This feature, in conjunction with four external RC networks, can cancel the local echo by minimum of 25 dB. The adaptation process for the hybrid will take place during the echo canceller training period.

Band-split filters are also provided to separate the receive and transmit signals, which allows the modem to operate in the V.22, V.22 bis, V.23, V.21 and Bell 103 modes.

BLOCK DIAGRAM

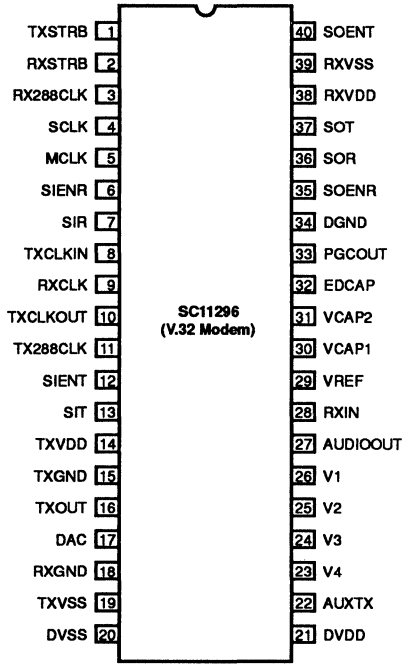


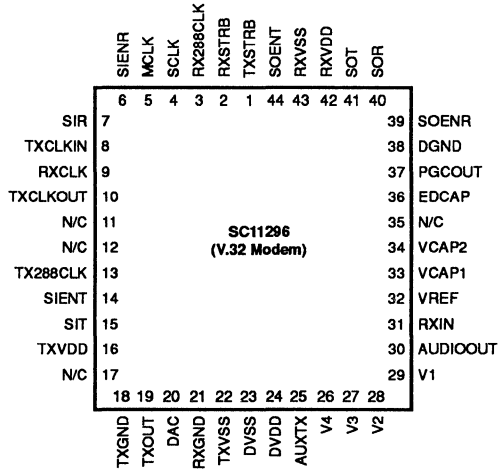
PIN/FUNCTION DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1 (1)	TXSTRB	Transmit strobe; TTL input/output. This pin will be input if TSIN/$\overline{EX}$ in transmit input interface is low otherwise, it will be an output. Falling edge of this signal triggers the transmit DAC and echo canceller ADC.
2 (2)	RXSTRB	Receive strobe; TTL input/output. This pin will be input if RSINT in receive interface is low, otherwise it will be an output. The falling edge of this signal will trigger the receive ADC.
3 (3)	RX288CLK	TTL output. This pin provides a clock frequency which is 288 kHz and synchronous to RXCLK.
4 (4)	SCLK	Shift clock; TTL output and its frequency is 1/3 of the MCLK. This clock is used for serially shifting data in or out of the chip.
5 (5)	MCLK	Master clock; TTL input. Must be 9.216 MHz. This clock generates various timing signals for the chip.
6 (6)	SIENR	Receive serial input enable; TTL input. A positive pulse on this input allows the serial data on SIR pin to enter the receive interface register.
7 (7)	SIR	Receive serial input; TTL input. Data is shifted serially into a 16-bit register with MSB entering first. If additional bits are sent in, they will be ignored.
8 (8)	TXCLKIN	Transmit clock input; TTL input. This is the external timing source which transmit phase-locked loop locks onto.
9 (9)	RXCLK	Receive data clock; TTL output. This signal which is generated internally by receive phase-locked loop provides timing for receive data stream.
10 (10)	TXCLKOUT	Transmit data clock; TTL output. This signal which is generated internally by transmit phase-locked loop provides timing for transmit data stream.
11 (13)	TX288CLK	TTL output. This pin provides a clock frequency which is 288 kHz and synchronous to TXCLKOUT.
12 (14)	SIENT	Transmit serial input enable; TTL input. A positive pulse on this input allows the serial data on SIT to enter the transmit interface register.
13 (15)	SIT	Transmit serial input; TTL input. Data is shifted serially into a 16-bit register with MSB entering first. If additional bits are sent in, they will be ignored.
14 (16)	TXVDD	Transmit analog V_{DD}; TXV_{DD} = +5 V.
15 (18)	TXGND	Transmit analog GND; TXGND = 0 V.
16 (19)	TXOUT	Transmit output; analog signal.
17 (20)	DAC	Transmit DAC's sampled and held output; analog signal. This auxiliary output is used for trimming the 12-bit transmit DAC output.
18 (21)	RXGND	Receive analog GND; RXGND = 0 V.
19 (22)	TXV_{SS}	Transmit analog V_{SS}; TXV_{SS} = –5 V.
20 (23)	DV_{SS}	Digital V_{SS}; DV_{SS} = –5 V.
21 (24)	DV_{DD}	Digital V_{DD}; DV_{DD} = +5 V.
22 (25)	AUXTX	Transmit auxiliary input; analog signal.
23–26 (26–29)	V_4–V_1	Four inputs to the adaptive hybrid; analog signal.
27 (30)	AUDIOUT	Audio output. The analog receive signal is passed through a gain-stage buffer to drive a speaker for line monitoring.
28 (31)	RXIN	Receive input; analog signal.
29 (32)	VREF	Reference voltage; analog signal.

PIN NO.	PIN NAME	DESCRIPTION
30, 31 (33, 34)	VCAP1, VCAP2	An external capacitor is required between these two pins. This capacitor together with an internal 25 kΩ resistor forms a high-pass filter that removed the DC component of the signal before entering the PGC. The -3 dB frequency for this high pass filter is given by; $f_{-3dB} = \frac{1}{50{,}000\pi\ C_{ext}}$
32 (36)	EDCAP	Energy detect capacitor; analog input. An external 1 μF capacitor should be connected between this pin and RXGND.
33 (37)	PGCOUT	Programmable gain-control section's sampled and held output; analog signal.
34 (38)	DGND	Digital GND; DGND = 0 V.
35 (39)	SOENR	Receive serial output enable; TTL output. A positive pulse on this pin enables the data stored in receive output register to be serially shifted out through SOR pin.
36 (40)	SOR	Receive serial output; TTL output. Data is shifted in 13-bit blocks. The first 12-bit correspond to ADC data. Bit 13 (ED) indicates the status of energy detect.
37 (41)	SOT	Transmit serial output; TTL output. During each transmit strobe cycle, this pin outputs two blocks of data. First one carries echo signal information and the second one corresponds to adaptive hybrid output.
38 (42)	RXV_{DD}	Receive analog V_{DD}; RXV_{DD} = +5V.
39 (43)	RXV_{SS}	Receive analog V_{SS}; RXV_{SS} = -5V.
40 (44)	SOENT	Transmit serial output enable; TTL output. A positive pulse on this pin enables the data stored in the transmit register to be serially shifted out through SOT pin.
(11,12,17,35)	N/C	

Numbers in ( ) refer to 44-Pin PLCC Package.





Pinouts for 40-pin DIP and 44-pin PLCC are subject to change without notice.

GENERAL CHIP DESCRIPTION

A simplified block diagram of the chip is shown on Page 369. In the receive direction, the receive signal is passed through the antialising filter. The filtered signal is summed with the output of the adaptive hybrid, which cancels the near-end echo, and is fed to the receive filter. The receive filter consists of a low-pass, two high-pass, and a notch section. These filters under the transmit interface control can be configured in different ways to support the appropriate modes of operation. The output of the receive filter is subsequently smoothed by an analog filter. In the V.32 mode, where the echo canceller is active, the output of the smoothing filter is sampled by the transmit strobe and summed with the estimated echo signal. The sampled-and-held signal goes to two blocks. It feeds a 12-bit analog-to-digital converter which converts the analog signal to a 12-bit 2's complement number and sends it through the transmit serial output interface to the signal processor chip. It also goes to a reconstruction filter which smooths the sampled-and-held signal and compensates for the sin x/x distortion effects. The output signal from the smoothing filter is brought out of the chip and is AC coupled by an external capacitor to the input of a 128-step, 0.375 dB/step, Programmable Gain Control (PGC). The output of the programmable gain control is sampled with the receive strobe and converted to a digital word by a 12-bit 2's complement Analog-to-Digital Converter. The digital code is transferred to the digital signal processor chip through the receive serial output interface. In all other modes of operation where the echo-canceller is deactivated, the summer, sample-and-hold and reconstruction filters are bypassed and the output of the receive filter is directly fed into the programmable gain control.

The chip also includes an energy detect circuit which determines the presence of the signal. The threshold levels of the energy detect are programmable through the receive interface.

The transmit section consists of a 12-bit 2's complement Digital-to-Analog Converter (DAC), a sample-and-hold reconstruction filter, a programmable attenuator and a smoothing filter/buffer circuit. When the echo canceller is active, in each period of the transmit strobe, two 12-bit words are supplied to the 12-bit DAC. The DAC performs two consecutive conversions. The first output is the estimated echo sample which is added to the receive signal. The second output is the transmit signal which is fed to a sample-and-hold circuit and subsequently a reconstruction filter with a sin x/x correction for 9.6 kHz sample rate. The output signal from the low-pass filter goes through a 15-step, 1 dB/step attenuator and a transmit smoothing filter which is capable of driving an off-chip 600 Ω load.

The chip also includes a transmit digital phase-lock loop and a receive digital oscillator that, under the receive interface control, can be used as digital phase-lock loop. An audio monitor with a programmable attenuator allows monitoring of the line activities in the call progress monitor mode.

The master clock input to the chip is a 9.216 MHz clock. All necessary timing and filter clocks are internally generated by a timing generator.

The chip has four serial interfaces, two for transmit and two for receive directions. The subsequent sections will give a more detailed description of the individual blocks.

Receive Filter

Details of the receive filter section are shown in Figure 2. The input signal first goes through a 2nd order continuous time antialiasing filter. The output of the antialiasing filter is summed with the output of the adaptive hybrid and is filtered by a 2nd order low-pass filter. The filter is clocked at a 256 kHz rate. The input section takes two samples at every clock cycle and implements a cosine filter. This effectively increases the sampling rate to 512 kHz. When the adaptive hybrid is disabled, the corresponding signal path is connected to ground. The summing section is followed by a 2nd order smoothing filter which in turn drives a 7th order low-pass filter with two transmission zeros. The pass band edge of the filter which is clocked at 256 kHz is at 3200 Hz

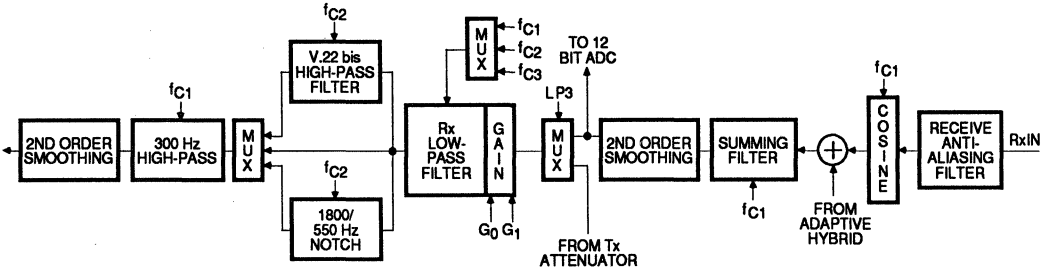


Figure 2. Receive Filter Block Diagram

and provides a minimum of 55 dB loss in the stopband region.

The low-pass filter is followed by a high-pass section clocked at 256 kHz. The filter has a third order transfer function and the passband edge is 300 Hz. It provides 30 dB loss at 60 Hz. The low-pass, high-pass combination realizes a band-pass filter with a passband extending from 300–3200 Hz. The frequency response of this band-pass filter along with the details of the passband and the group delay response are shown in Fig. 3a, 3b, and 3c repectively. The high-pass filter is followed by a second order smoothing section which eliminates the clock noise from the output signal. In V.22 bis/V.22/103/V.21/V.23 modes, where full duplex operation is achieved by frequency division multiplexing, the receive filter is configured as a bandsplit section to reject the adjacent band. In the Answer mode, where the modem transmits in high-band and receives in low-band, the clock of the Rx low-pass filter is reduced by a factor of two to 128 kHz, while the high-pass clock is kept at 256 kHz. This moves the low-pass filter passband edge to 1600 Hz and in conjunction with the high-pass, it realizes a bandpass filter which extends from 300 Hz to 1600 Hz. It also provides a minimum of 55 dB rejection in the high channel region. An additional programmable notch filter can be inserted in the signal path to remove the guard tone in the Answer mode. A notch frequency at 1800 or 550 Hz can be selected through the transmit serial interface. In the V.21 mode the same arrangement is used except that the filter clock is reduced by a factor of 2.5. This moves the low-pass filter pass band edge to 1280 Hz.

In the Originate mode, the modem transmits in the lowband and receives in the highband. The receive low-pass filter in this case is clocked at its nominal rate of 256 kHz and an additional 7th order high-pass filter is inserted between the low-pass and the 300 Hz high-pass filters. The passband edge of the high-pass filter, which is clocked at 128 kHz, is 2000 Hz and it introduces a minimum of 55 dB rejection in the lowband region. The combination of the low-pass and high-pass filters realizes a bandpass filter with a passband that extends from 2000 Hz to 3200 Hz. In the V.21 mode the filter clock is reduced by a factor of 1.25, which moves the pass bands of the band-pass filter to 1600–2560 Hz.

In V.23 forward-channel transmission mode the clock of the Rx low-pass filter is kept at 256 kHz, while the V.22 bis high-pass clock is reduced to 64 kHz. This arrangement realizes a bandpass filter that covers a band of 1000–3200 Hz which passes the forward channel and rejects the backward channel. In the reverse mode where the received signal is in the backward channel, the V.22 bis high-pass filter is bypassed and the clock of the Rx low-pass filter is reduced by a factor of 5 to 51.2 kHz. The Rx low-pass and the 300 Hz high-pass combination realize a band-pass filter which extends from 300–640 Hz. This filter will pass the backward channel and reject the forward channel.

The overall frequency response and the group delay of the various highband and lowband filters for different modes of operation are shown in Figures 4–7.

Implemented at the input of the receive low-pass filter is a 2-bit programmable gain control. Depending on the amount of rejection of the adaptive hybrid and the magnitude of the receive signal, the input gain can be increased to improve the noise performance of the modem.

Receive Reconstruction Filter

In the V.32 mode, when the echo canceller is active, the output of the receive filter is sampled by the transmit strobe and summed with the estimated echo signal. The sampled-and-held signal goes to two blocks. It feeds a 12-bit Analog-to-Digital Converter which converts the analog signal to a 12-bit 2's complement number. It also goes to a reconstruction filter. The first section of this filter is a 2nd order active RC circuit which removes the high frequency components of the signal to allow sampling it with a 256 kHz clock. The smoothed signal is subsequently applied to a switched capacitor low-pass filter section which removes the remaining high frequency signal components and also compensates for the sin x/x distortion effects for a 9.6 kHz sampling rate. The output of the low-pass filter is passed through a second order active RC filter to remove the clock noise, and is brought off-chip to be AC coupled to the programmable gain control. The block diagram of the receive reconstruction filter is shown in Figure 8a. The details of the amplitude and delay responses are shown in Figures 8b, 8c and 8d

Echo Analog-to-Digital Converter

The 12-bit Analog-to-Digital Converter (ADC) is operational only when the echo canceller is active. The input to the ADC is taken from two points, the echo canceller sample-and-hold and receive input summing filter. The ADC is capable of doing two conversions in one period of the transmit strobe. In a typical example of echo cancellation process, adaptive hybrid and echo canceller are enabled at first and their outputs are sampled by two sample-and-hold circuits on the falling edge of transmit strobe signal. The 12-bit ADC converts both samples to digital codes during each strobe period, however, in the beginning echo samples are ignored and digital processor concentrates on adjusting the adaptive hybrid. This phase takes T1 seconds after which both samples will be used to adjust

Figure 3a. Overall Frequency Response (Normal Mode)

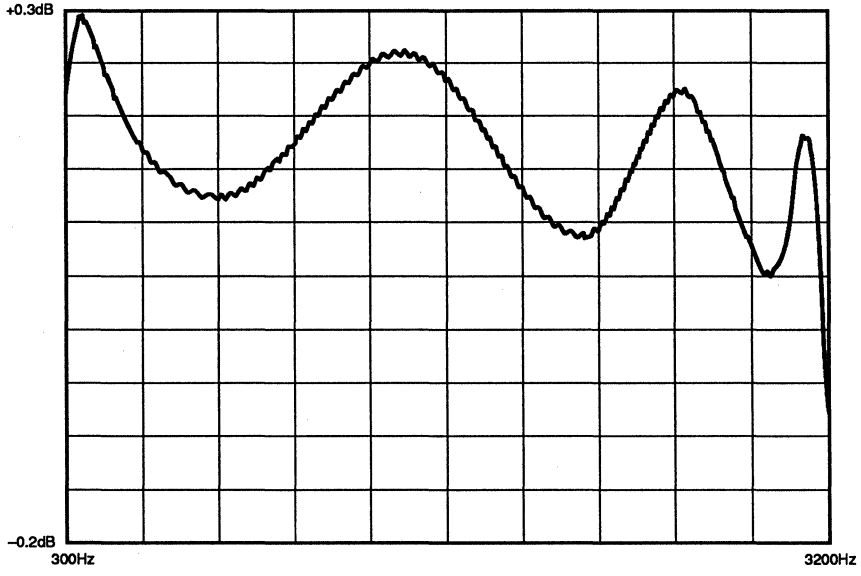


Figure 3b. Details of Passband (Normal Mode)

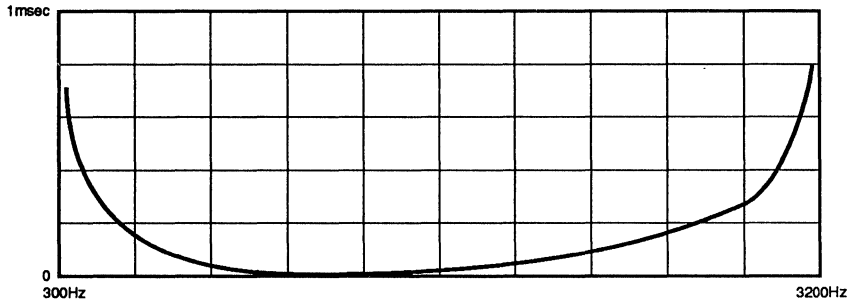


Figure 3c. Passband Group Delay (Normal Mode)

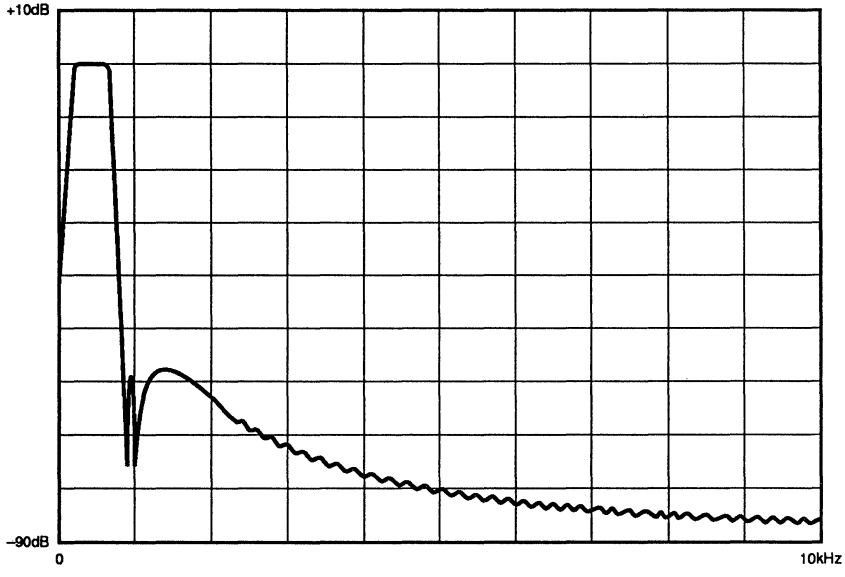


Figure 4a. Overall Frequency Response (V.23BC/CPM)

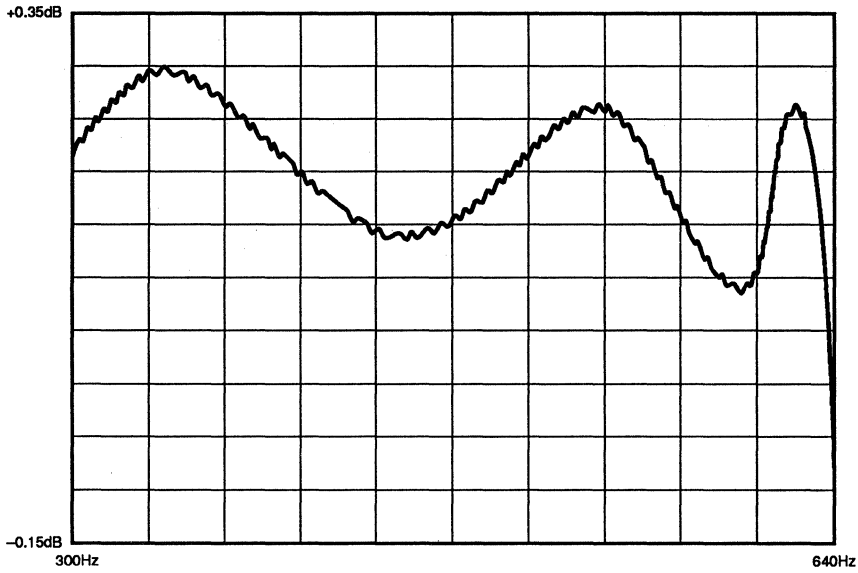


Figure 4b. Details of Passband (V.23BC/CPM)

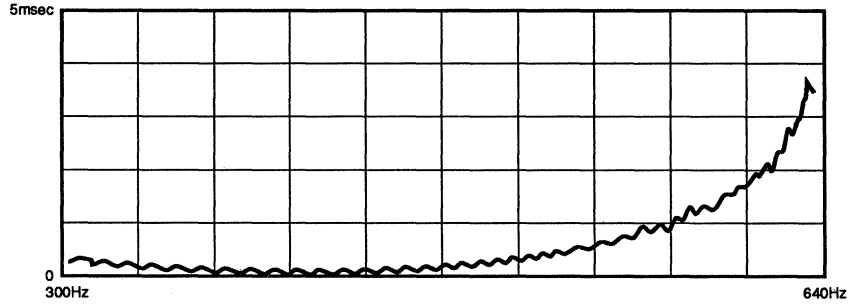


Figure 4c. Passband Group Delay (V.23BC/CPM)

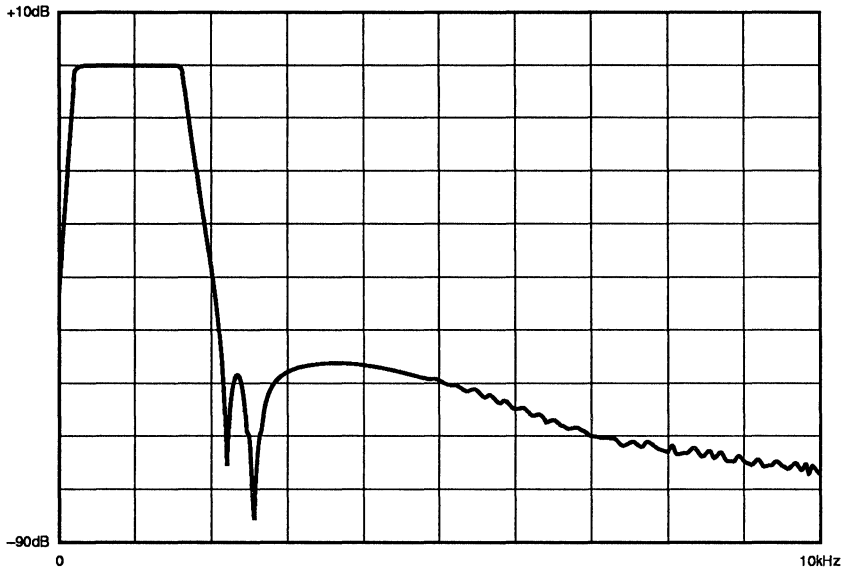


Figure 5.1a. Overall Frequency Response (103A)

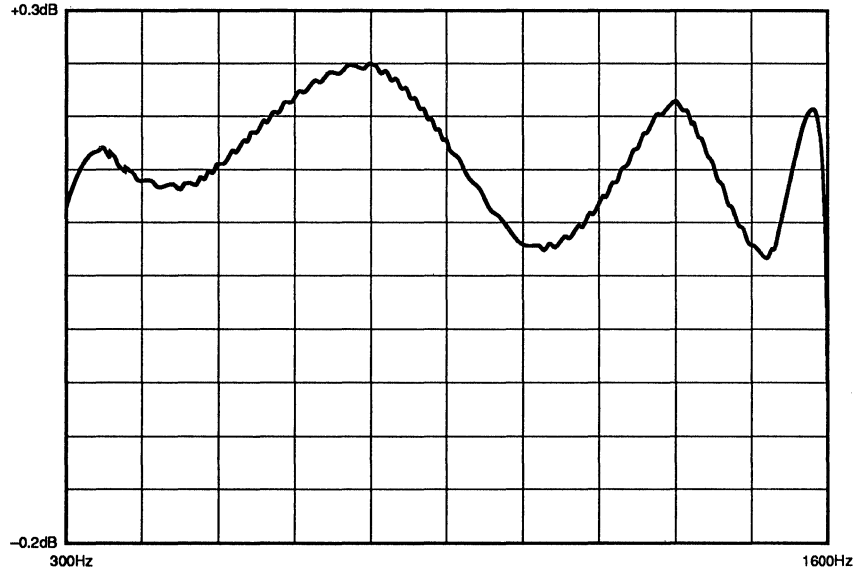


Figure 5.1b. Details of Passband (103A)

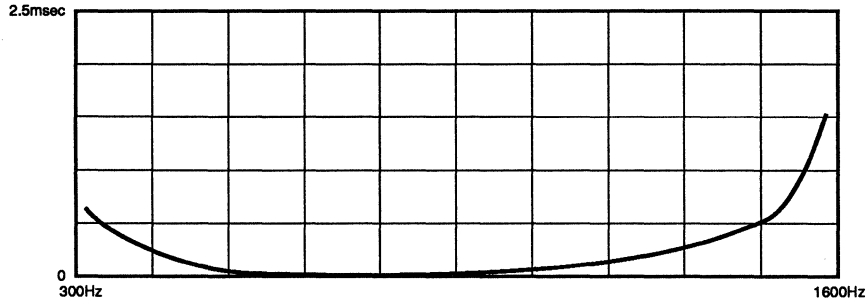


Figure 5.1c. Passband Group Delay (103A)

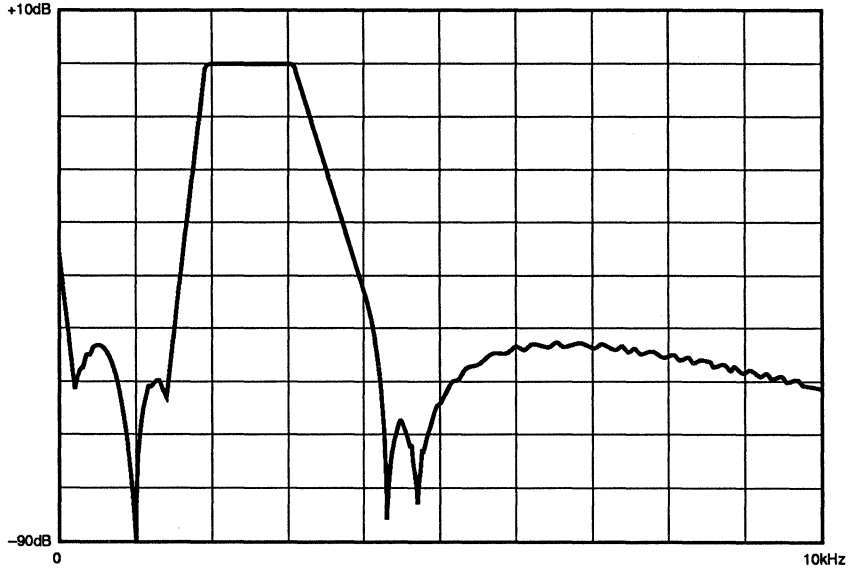


Figure 5.2a. Overall Frequency Response (103O)

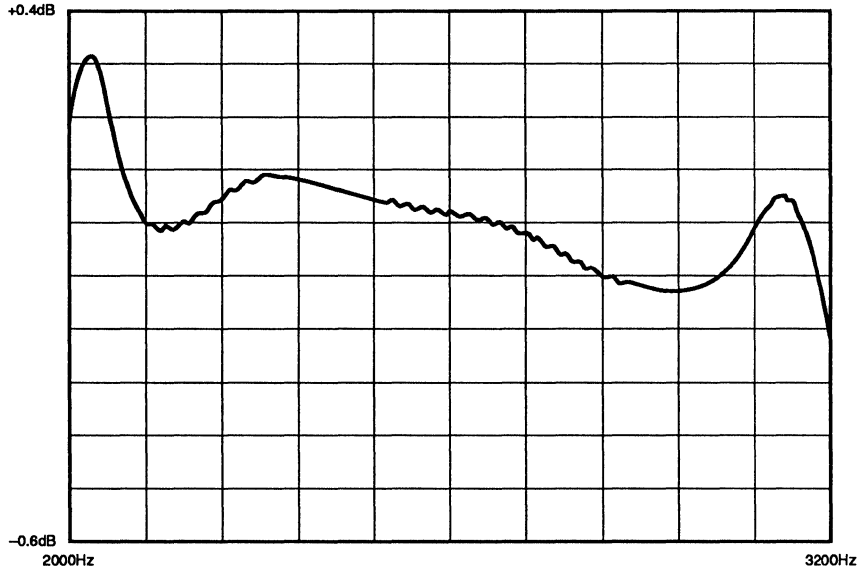


Figure 5.2b. Details of Passband (103O)

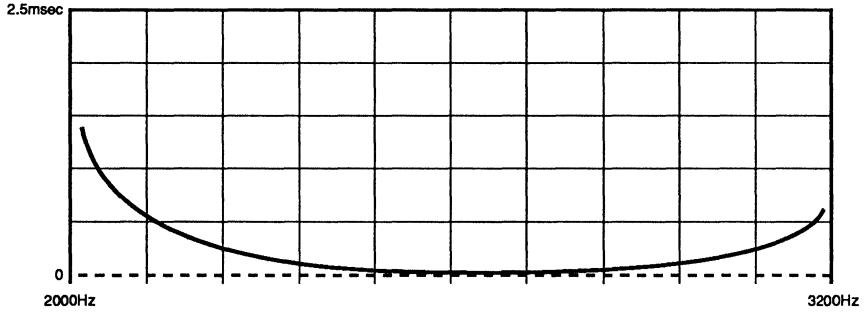


Figure 5.2c. Passband Group Delay (103O)

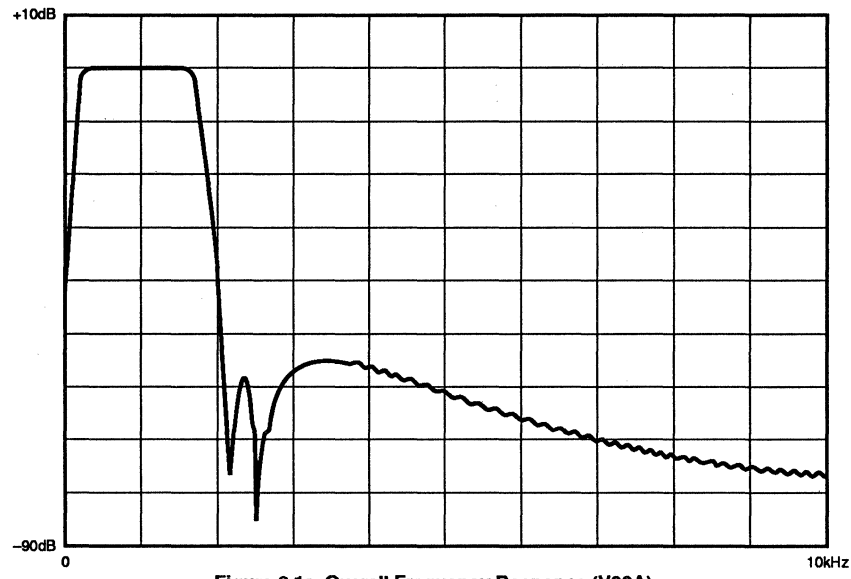


Figure 6.1a. Overall Frequency Response (V22A)

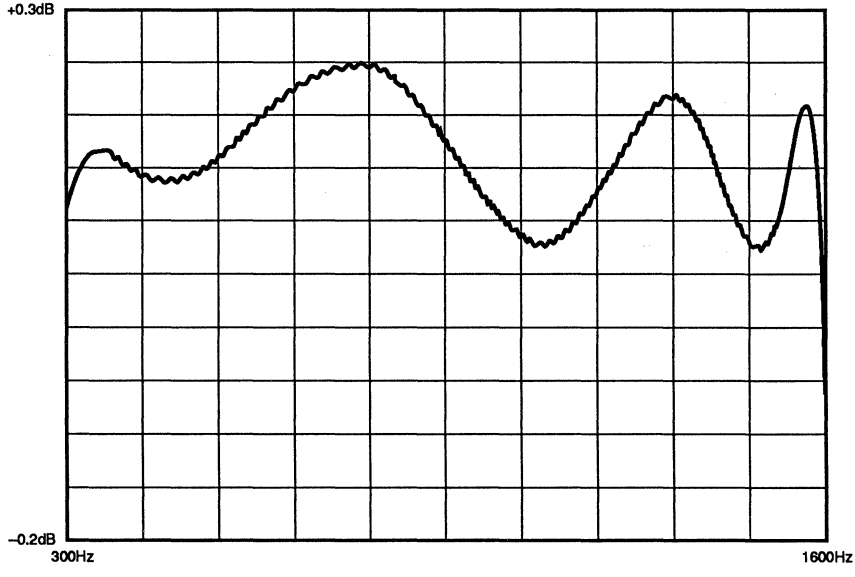


Figure 6.1b. Details of Passband (V22A)

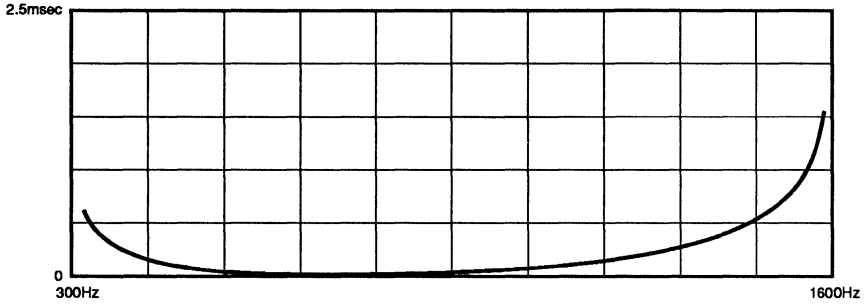


Figure 6.1c. Passband Group Delay (V22A)

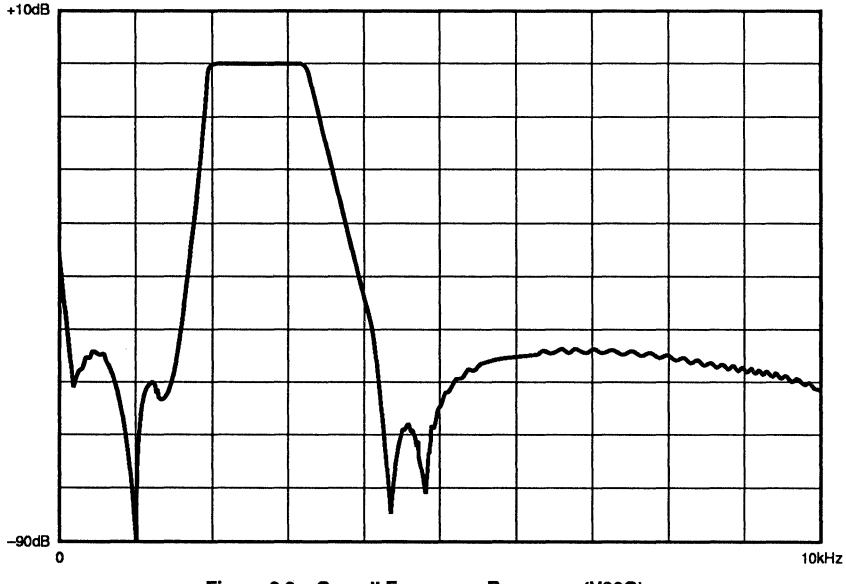


Figure 6.2a. Overall Frequency Response (V22O)

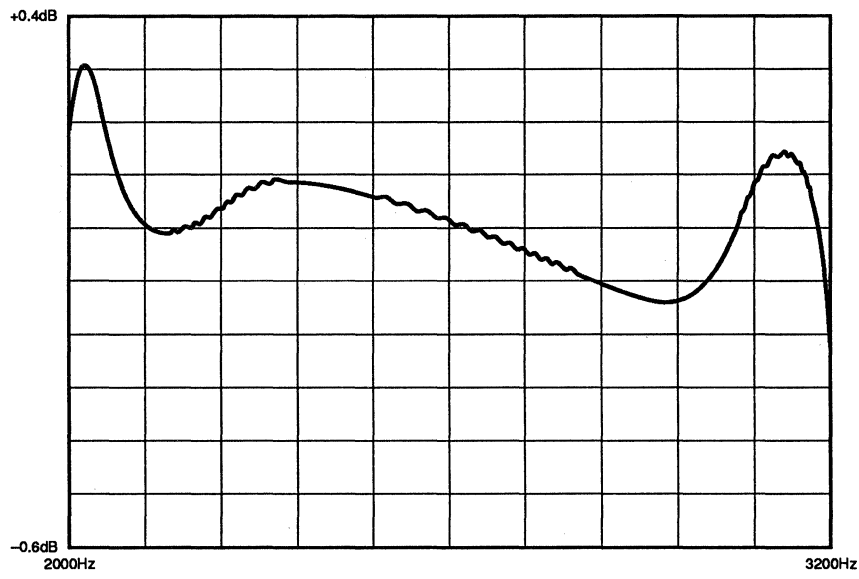


Figure 6.2b. Details of Passband (V22O)

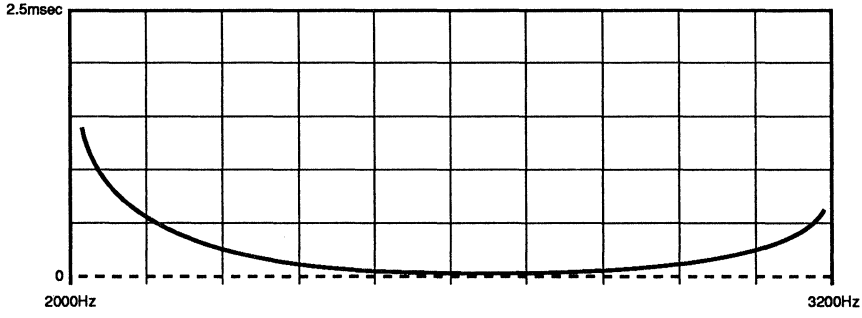


Figure 6.2c. Passband Group Delay (V22O)

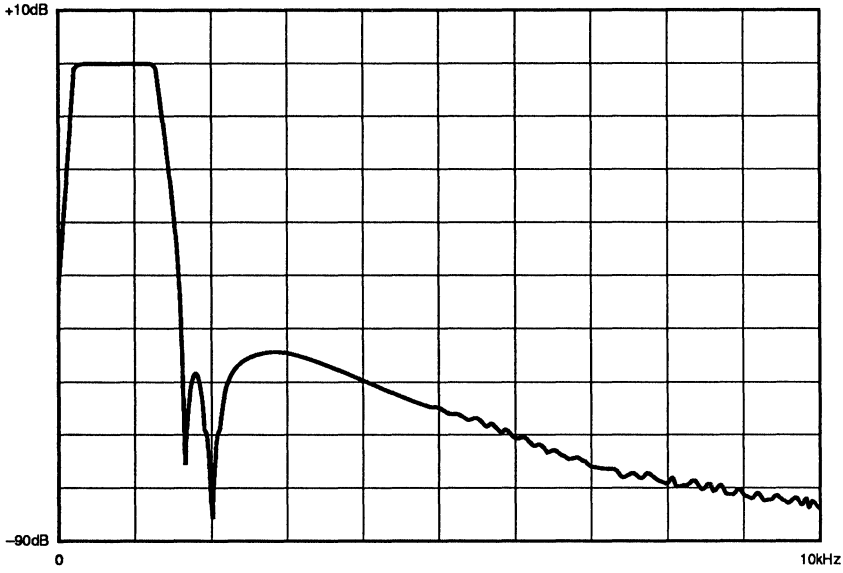


Figure 7.1a. Overall Frequency Response (V21A)

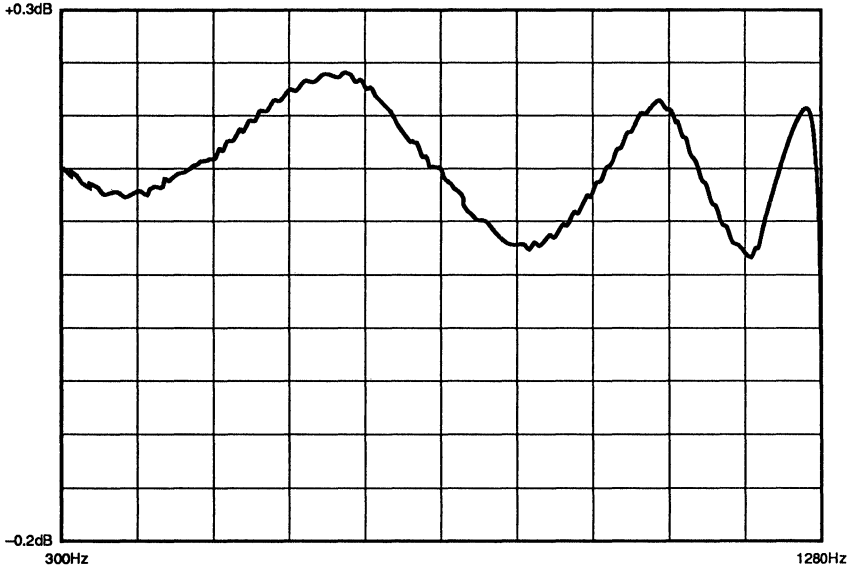


Figure 7.1b. Details of Passband (V21A)

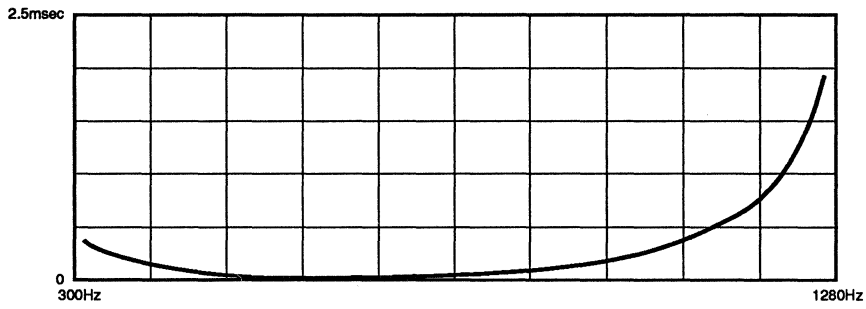


Figure 7.1c. Passband Group Delay (V21A)

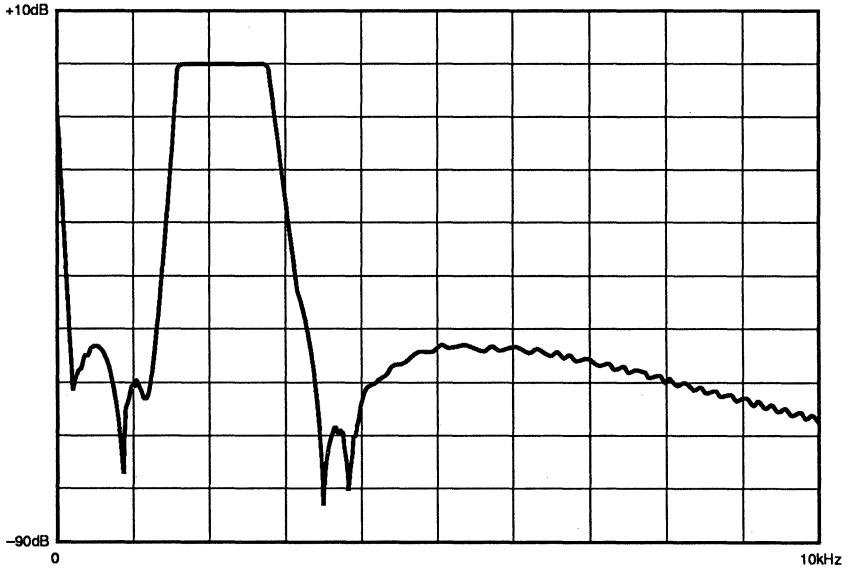


Figure 7.2a. Overall Frequency Response (V21O)

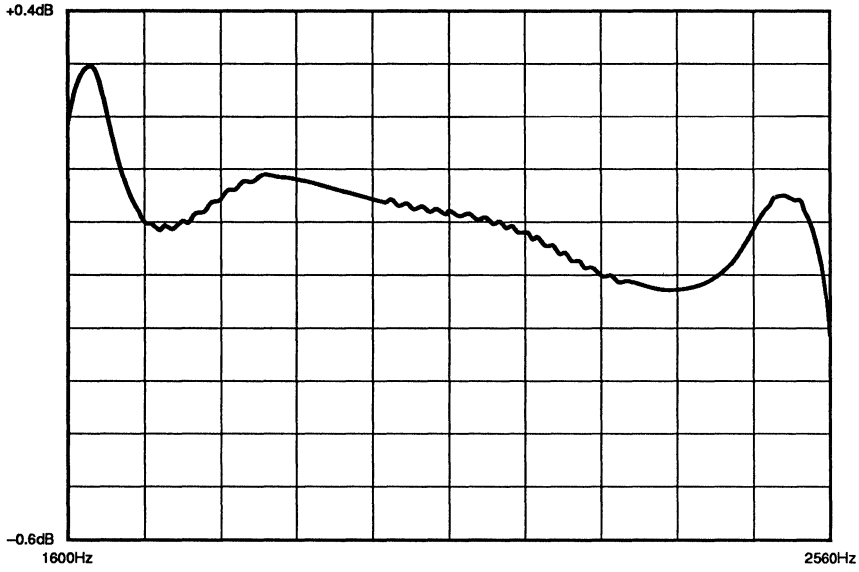


Figure 7.2b. Details of Passband (V21O)

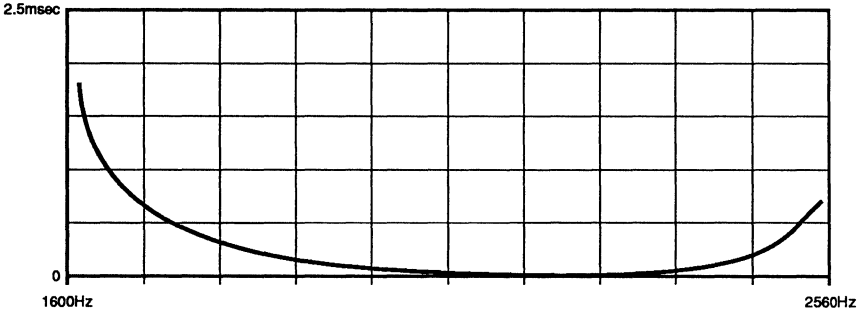


Figure 7.2c. Passband Group Delay (V21O)

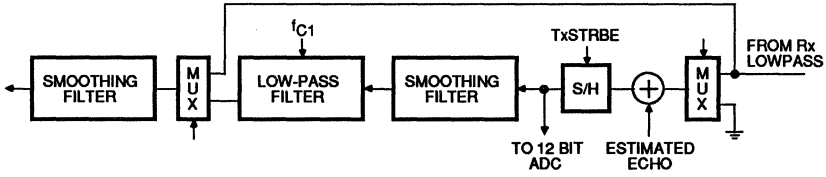


Figure 8a. Receive Reconstruction Filter Block Diagram

Figure 8b. Overall Frequency Response (RX Reconstruction)

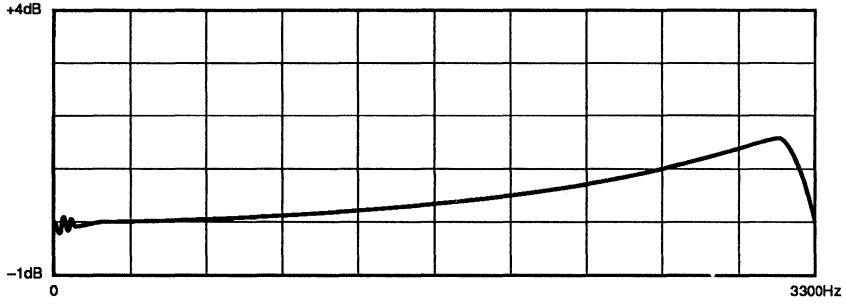


Figure 8c. Details of Passband (RX Reconstruction)

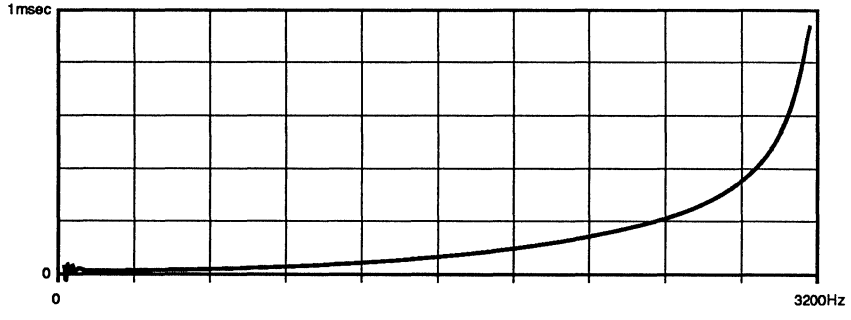


Figure 8d. Passband Group Delay (RX Reconstruction)

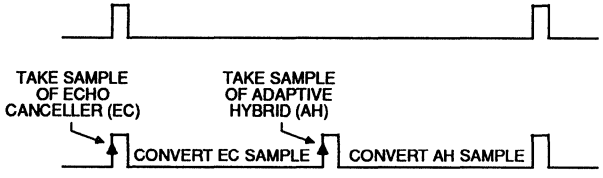


Figure 9. 12 Bit ADC Timing

adaptive hybrid and echo canceller. This process takes T2 seconds after which the adaptive hybrid coefficients are frozen and the echo canceller takes over. During the following period, T3, the ADC converts only one sample which is taken from the output of the echo canceller sample-and-hold. It is worth mentioning that the overlap time, T2, where both the adaptive hybrid and echo canceller are adjusted can be zero. In that case, the adaptation of the echo canceller starts only after the hybrid adaptation has stopped. Figure 9 shows the internal timing of the 12-bit ADC. In a non V.32 mode, when the echo canceller is deactivated, the 12-bit ADC is disabled and no conversion is made.

Adaptive Hybrid (AH)

The Adaptive Hybrid serves as the front-end, local-loop, near-end echo canceller. Using four RC networks and adjusting their individual attenuations with four 8-bit multiplying DACs to match the inverse of the incoming echo, the echo can be cancelled by a minimum of 25 dB. Figure 10 presents the arrangement of the Adaptive Hybrid where the three networks are simple RC circuits. The actual implementation of the Adaptive Hybrid is shown in Figure 11 with the three external RC networks and one direct connection. The four 8-bit multiplying DACs attenuate the RC network outputs with gains in the range of ±0–0.99. The switched-capacitor summer adds the output of the four DAC sets and subtracts it from the echo input. The output of the summer feeds into the 12-bit ADC for conversion. The outputs of the four RC networks are also fed to four comparators for sign extraction. When performing adaptive hybrid cancellation the signal processor reads the magnitude of the echo and the sign of the four individual RC sections (note that one RC section is just a direct connection). It then calculates the new coefficients for the DACs so as to drive the near-end echo magnitude towards zero. A more detailed description of the adaptation algorithm and recommendations for RC networks will be presented in a later section.

Transmit Section

The transmit section shown in Figure 12 includes a 12-bit DAC, two sample-and-holds, an analog smoothing filter, a switched-capacitor low-pass filter and a programmable 15-step 1 dB/step attenuator. In the V.32 mode, when the echo canceller is active, the signal processor chip supplies two 12-bit digital codes to the DAC during each period of the transmit strobe. The first code is the echo estimate and the other is the transmit signal. The DAC does two consecutive conversions and feeds the analog samples to two sample-and-hold circuits. The echo sample-and-hold output goes to the receive section and cancels the echo from the receive signal. The transmit sample-and-hold output goes to an analog antialiasing filter before it is fed to the low-pass reconstruction filter. This filter has a seventh order transfer function and it compensates for the sin x/x distortion effects due to a 9.6 kHz sample-and-hold. The frequency response of the transmit filter is shown in Figure 13, where Figure 13a shows the details of the passband amplitude response, 13b is the passband group delay response and 13c is the overall amplitude response. It is important to mention that the overall transmit amplitude response is achieved by combining the transmit filter response with the sin(ωT/2)/(ωT/2) response of

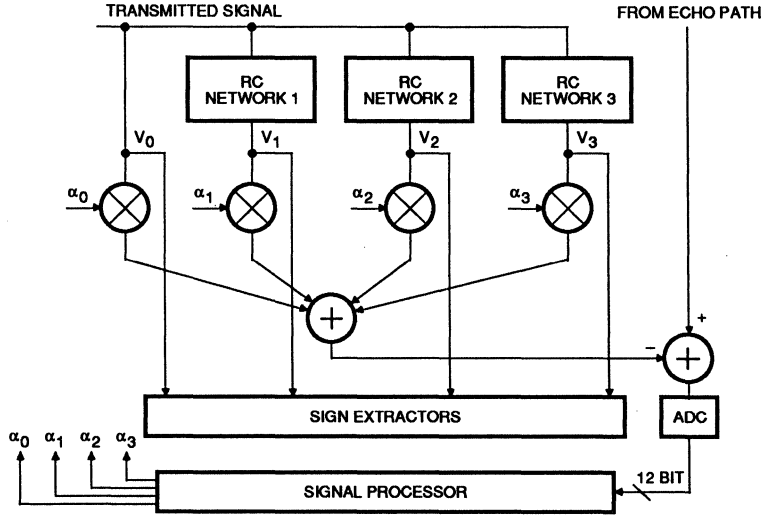


Figure 10. Adaptive Hybrid Block Diagram

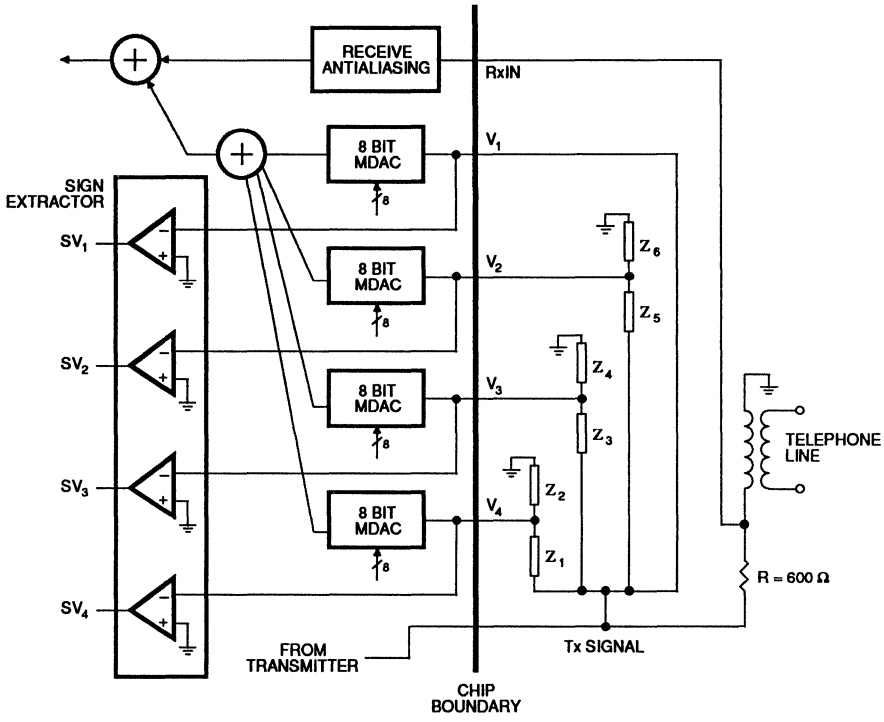


Figure 11. Adaptive Hybrid

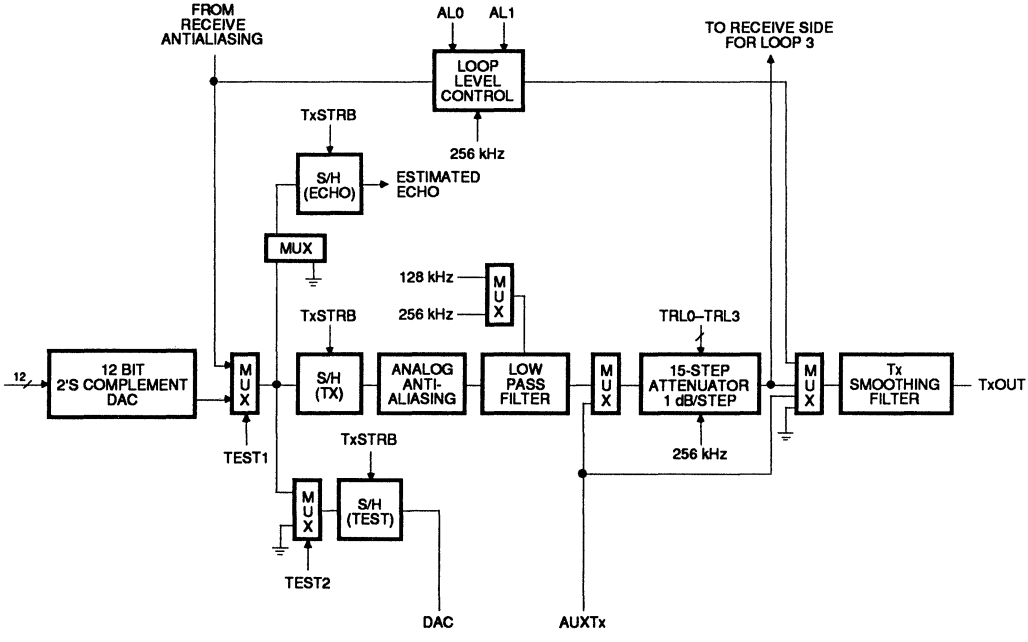


Figure 12. Transmit Block Diagram

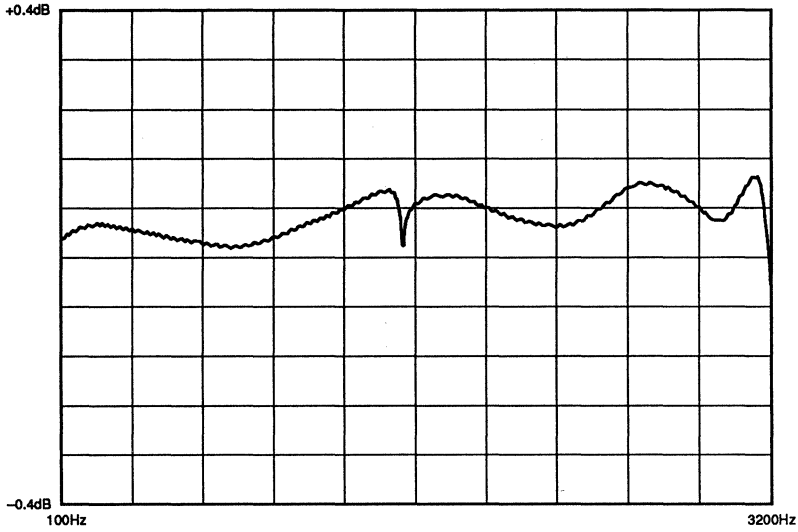


Figure 13a. Details of Passband (TX Reconstruction)

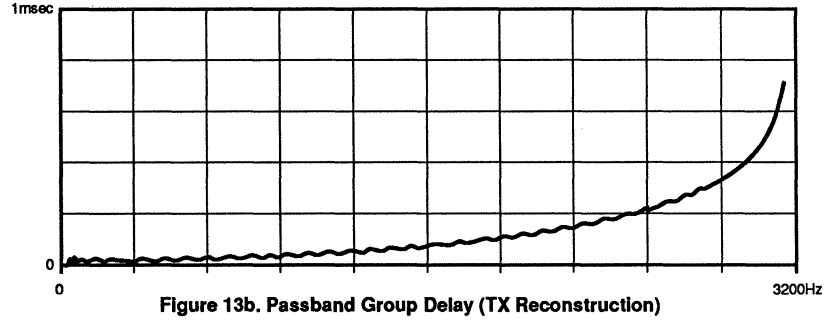


Figure 13b. Passband Group Delay (TX Reconstruction)

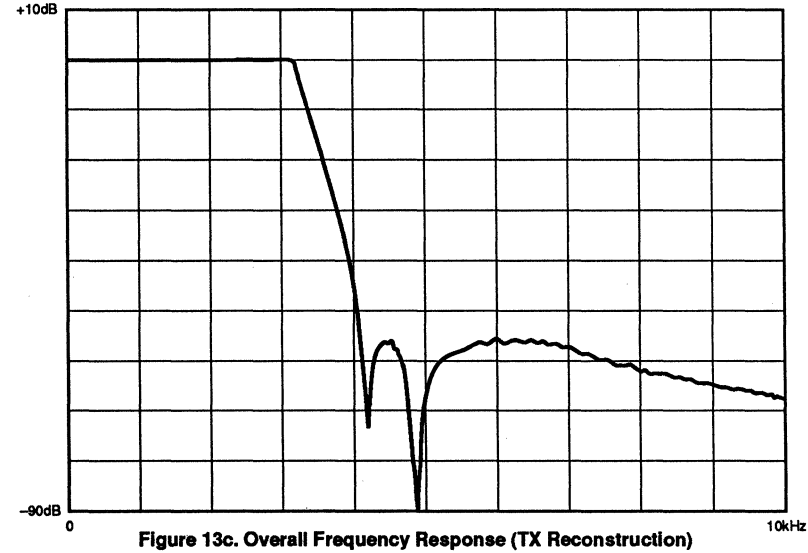


Figure 13c. Overall Frequency Response (TX Reconstruction)

the sample-and-hold circuit. The overall response of the transmit filter and sample-and-hold combination for a 9.6 kHz sampling rate is shown in Figure 13c.

The transmit filter is followed by a 15-step 1 dB/step attenuator. The output of the attenuator is smoothed by the transmit continuous time smoothing filter which drives the telephone line. An auxiliary input signal can be injected into the chip through the AUXTX pin. This input goes to the line either directly through the transmit smoothing filter or it can be routed through the transmit attenuator for amplitude control.

In those modes of operation when the echo canceller is disabled, the processor will not supply the sample of the echo estimate and the echo sample-and-hold input will be connected to ground. The 12-bit DAC will do one conversion in one period of the transmit strobe.

The clock of the transmit filter can be reduced by a factor of 2 or 2.5 under processor control. For the low sampling clock, the passband edge of the filter moves to 1.6 or 1.28 kHz. This feature is useful in the V.23 backward channel or V.22 bis, 103 or V.21 originate modes when the transmit signal is in the lowband. The filter can be used to eliminate the components of the lowband signal that fall into the highband region. However, since the filter amplitude response is optimized to compensate for a 9.6 kHz sample-and-hold effect, reducing the clock frequency by a factor of 2 or 2.5 will introduce an additional amplitude distortion. In the mode where the transmit signal is in the highband, the transmit filter can be used without reducing the clock frequency. If the adjacent band filtering is done digitally, then it may not be necessary to reduce the transmit filter clock frequency.

Loopback

Two loopback modes are supported by the SC11296. In loop 3 mode, the transmit signal is routed to the input of the receive filter, and the receive input signal is ignored. In loop 4 mode, the analog receive signal is routed to the transmitter through a four level programmable gain control.

Call Progress Tone Monitor

In the Call Progress Mode (CPM), the clock frequency of the receive low-pass filter is reduced to 1/5 of its normal value. This moves the pass-band edge of the low-pass filter to 640 Hz. The low-pass and high-pass combination form a band-pass filter with a pass-band range of 300–640 Hz. The response of this filter is shown in Figure 4.2. The received analog signal passes through the band-pass filter and then into the energy detect circuit. The energy detect output can be monitored by the signal processor to indicate the presence of energy.

Audio Monitor

The analog receive signal is passed through a level controller and a buffer to drive a speaker for line audio monitoring.

This circuit is used during call progress detection to monitor call progress tones. The audio signal level can be controlled by ALC1 and ALC0.

Energy Detector

The energy detector monitors the receive signal and indicates the presence of the signal through ED logic output. The detection level is selected between four distinct levels by control bits LVL0 and LVL1 in receive input interface. The energy detector needs one external capacitor.

Serial I/O

The chip has four serial input/output ports; two for the transmit and two for the receive strobes. The serial I/O is designed to be compatible with DSP chips such as TI TMS320-25.

Transmit Serial Input Interface

This block accepts 16-bit serial words that consist of address and control/data bits. The 4 MSB's correspond to the addresses of internal registers and the remaining bits convey the information about transmit signal, echo, adaptive hybrid or SC11296 set up. The data on SIT pin will be shifted in this serial port on the falling edges of the SCLK and must be valid at these time points. Figure 14a shows the timing diagram for the transmit serial input port and timing requirements are given in Table 1. When writing into the 12-bit DAC registers (Tx data or echo data), the timing of Figure 14b with respect to Tx strobe (TxSTRB) should be followed to ensure proper conversion by DAC. MSB of data is shifted in first. Table 2 shows the register structure of the transmit input interface, followed by bit descriptions.

Reference Voltage

This section provides a reference voltage with a nominal value of 2.5 V for on-chip use. A buffered version of this voltage is provided off-chip for external power supply low voltage detect purposes.

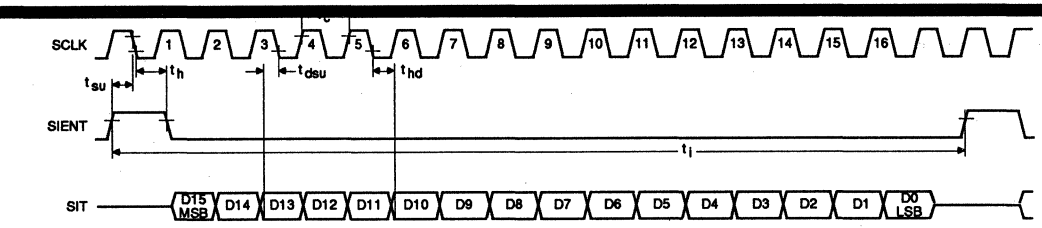


Figure 14a. Tx Serial Input Timing

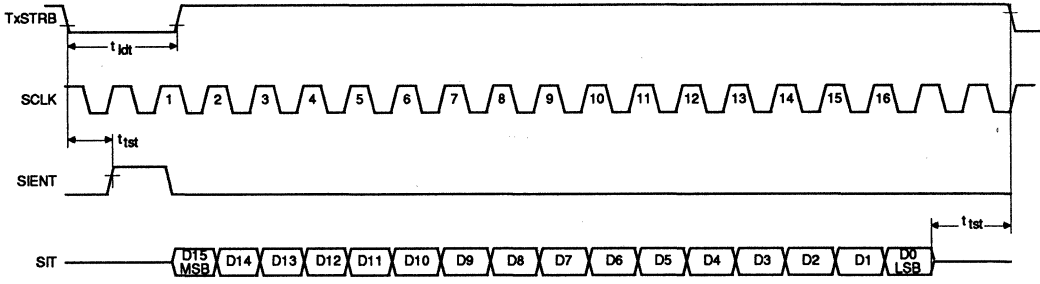


Figure 14b. Tx Serial Input Timing With Respect to TxSTRB (For Tx D/A Only)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{su}	Set up time from SIENT high to SCLK low	80			ns
t_h	Hold time from SCLK low to SIENT low	50			ns
t_{hd}	Hold time from SCLK low to SIT transition	50			ns
t_{dsu}	Data set up time from SIT valid to SCLK low	80			ns
t_i	Interval between consecutive SIENT pulses	5.9			µs
t_{ldt}	Low duration of TxSTRB	.2		102	µs
t_{tst}	Set up time from TxSTRB low to SIENT high	0			ns
t_{sdt}	Delay time from last input data to TxSTRB low	2			µs
t_{tso}	Delay time from TxSTRB low to SOENT high	60		425	ns
t_{do}	Delay time from SCLK high to SOENT high			100	ns
t_{ti}	Time interval between two SOENT pulses following a high-to-low transition of TxSTRB		5.9		µs
t_{db}	Delay time from SCLK high to SOT valid			100	ns
t_{hz}	Hold time from SCLK low to SOT high impedance	50			ns
t_C	Serial clock period		325		ns

Table 1. Timing Requirements for Tx Serial Input/Output Interfaces

Register	Add. Bits	Data/Control Bits											
	D15–D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TxD	0000	TxD11	TxD10	TxD9	TxD8	TxD7	TxD6	TxD5	TxD4	TxD3	TxD2	TxD1	TxD0
ECHO	0001	EC11	EC10	EC9	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
AHDAC1	0010	—	—	—	—	DH17	DH16	DH15	DH14	DH13	DH12	DH11	DH10
AHDAC2	0011	—	—	—	—	DH27	DH26	DH25	DH24	DH23	DH22	DH21	DH20
AHDAC3	0100	—	—	—	—	DH37	DH36	DH35	DH34	DH33	DH32	DH31	DH30
AHDAC4	0101	—	—	—	—	DH47	DH46	DH45	DH44	DH43	DH42	DH41	DH40
CR1	0110	AL1	AL0	TR1	TR0	CLK2	CLK1	CLK0	TPLL Jam	TPLL IN/$\overline{EX}$	TPLL LK/$\overline{FR}$	TS IN/$\overline{EX}$	TxST
CR2	0111	ENAH	ENEC	SQEC	LP3	G1	G0	HYEN	TR3	TRL3	TRL2	TRL1	TRL0
CR3	1000	TEST3	TEST2	TEST1	NSEL	NI	TXFC	MD3	MD2	MD1	MD0	ALC1	ALC0

Table 2. Transmit Input Interface

TXD0–11	12-bit 2's complement data representing transmit data sample.
EC0–11	12-bit 2's complement data representing echo estimate sample.
DH 10–17	8-bit 2's complement data representing scale factor for the output voltage of network #1.
DH20–27	8-bit 2's complement data representing scale factor for the output voltage of network #2.
DH30–37	8-bit 2's complement data representing scale factor for the output voltage of network #3.
DH40–47	8-bit 2's complement data representing scale factor for the output voltage of network #4.

TXST

Determines the rate of the transmit strobe.

TXST = 1	9.6 kHz
TXST = 0	7.2 kHz

TS IN/EX

Determines whether the TX strobe is generated internally or supplied externally.

TS IN/EX = 1	Internal
TS IN/EX = 0	External

In the external mode, the TX DPLL will be disabled, and the TXCLKOUT pin will go to a high or low state.

TPLL LK/FR

Determines whether the transmit DPLL is in the locked or free run mode.

TPLL Lk/FR = 1	Locked
TPLL Lk/FR = 0	Free Run

TPLL IN/EX

In the locked mode, this bit determines the signal that the TX DPLL locks to.

TPLL IN/EX = 1	Locked to RXCLK
TPLL IN/EX = 0	Locked to TXCLKIN

If TPLL Lk/FR = 0, this bit will be ignored.

TPLL JAM

When this bit is set, the transmit DPLL will reset itself on the next rising edge of the clock that it locks to. Once the DPLL is jammed, the bit will be automatically reset. After the jam is exercised, the distance between the previous and next TX strobe will always be greater or equal to the normal period.

CLK0–2

These three bits determine the transmit and receive bit clock rates.

			BIT RATE (KHZ)	
CLK2	CLK1	CLK0	MD3=0	MD3=1
0	0	0	1.2	1.2
0	0	1	2.4	2.4
0	1	0	4.8	4.8
0	1	1	7.2	7.2
1	0	0	9.6	9.6
1	0	1	12.0	0.6
1	1	0	14.4	0.3
1	1	1	14.4	0.075

TR0, TR1

These two bits select the transmit signal according to the following table.

TR1	TR0	SIGNAL SELECTED
0	0	Normal (Transmit Signal)
0	1	Transmit Squelch
1	0	AUXTX
1	1	Loopback (Loop 4)

AL0, AL1

Loop 4 gain control

AL1	AL0	GAIN
1	1	–6 dB
0	0	0 dB
0	1	6 dB
1	0	15 dB

TRL 0–3

Determines transmit level according to the following table.

TRL3	TRL2	TRL1	TRL0	Gain
0	0	0	0	0 dB
0	0	0	1	–1 dB
0	0	1	0	–2 dB
0	1	0	0	–4 dB
1	0	0	0	–8 dB

TR3

This bit controls the TX attenuator input mux.

TR3 = 1 Normal Mode. Connects Transmit Output to the Attenuator.
TR3 = 0 Connects AUXTX to the attenuator

HYEN

Enables hybrid

HYEN= 1 Enabled
HYEN= 0 Disabled

G0, G1

Determines programmable gain at the input of the RX filter after the adaptive hybrid. This gain will be set by evaluating the energy at the output of the adaptive hybrid and setting the gain based on the maximum receive signal level (–12 dBm).

G1	G0	GAIN
0	0	0 dB
0	1	4 dB
1	0	8 dB
1	1	12 dB

LP3

Loop 3 control bit. When this bit is set, the transmit signal is looped back to the receiver.

LP3= 1 Loop 3 Activated
LP3= 0 Loop 3 Deactivated

SQEC

This bit squelches the echo component from the echo summer sample-and-hold.

SQEC = 1 Squelch Echo Path
SQEC = 0 Enable Echo Path

ENEC

This bit enables and disables the echo canceller. In half-duplex two wire, or full-duplex four wire modes, the echo canceller can be disabled. In such a case, the receive reconstruction filter will be bypassed and both inputs to the echo summer sample-and-hold will be grounded.

ENEC = 1 Enable Echo Canceller
ENEC = 0 Disable Echo Canceller

ENAH

This bit controls the transfer of the digitized hybrid error signal through the serial interface.

ENAH = 1 Enable Data Transfer
ENAH = 0 Disable Data Transfer

When ENAH and ENEC are both zero, no data will be transferred and the 12-bit ADC will be disabled.

ALC0, ALC1

These bits control the audio output levels. A programmable attenuator that can drive a load impedance of 50 kΩ is provided to allow monitoring of the received line signal through an external speaker.

ALC1	ALC0	AUDIO OUTPUT LEVEL ATTENUATION
0	0	Squelch
0	1	12 dB
1	0	6 dB
1	1	0 dB

MD0–MD3

Mode Select bits. These bits control the mode operation according to the following table.

MD3	MD2	MD1	MD0		MODE
1	X	X	X	Normal	Normal Mode
0	1	1	1	V.23 FC	V.23 Forward Channel
0	1	1	0	V.23 BC/CPM	V.23 Backward Channeled Call Progress Mode
0	1	0	1	103A	103 Answer Mode
0	1	0	0	103O	103 Originate Mode
0	0	1	1	V22A	V.22 and V.22 bis Answer Mode
0	0	1	0	V22O	V.22 and V.22 bis Originate Mode
0	0	0	1	V21A	V.21 Answer Mode
0	0	0	0	V21O	A.21 Originate Mode

V22A Mode—This mode supports band split answering modems that operate according to the CCITT V.22 and V.22 bis recommendations. In this mode the receive and transmit signals are separated by passing the composite signal through the receive filter which is configured as a low-band filter with a pass band range of 300–1600 Hz.

V21A Mode—This mode supports a band split answering modem that operates according to the CCITT V.21 recommendation. In this mode the receive and transmit signals are separated by passing the composite signal through the receive filter which is configured as a low-band filter with a pass band range of 300–1280 Hz.

V22O Mode—This mode supports bandsplit originating modems that operate according to the CCITT V.22 and V.22 bis recommendations. In this mode the receive and transmit signals are separated by passing the composite signal though the receive filter which is configured as a band-pass filter with pass band edges extending from 2000–3200 Hz.

V21O Mode—This mode supports a band split originating modem that operates according to the CCITT V.21 recommendation. In this mode the receive and transmit signals are separated by passing the composite signal through the receive filter which is configured as a band-pass filter with pass band edges extending from 1600–2560 Hz.

V.23 BC/Call Progress mode (CPM)—In these modes the clock of the receive low-pass filter is reduced by a factor of 5. This moves the pass band edge to 640 Hz. The low-pass and high-pass filters form a band-pass which extends from 300–640 Hz and rejects the V.23 forward channel signal. This filter and the energy detect can be used for call progress monitoring.

V.23FC Mode—In this mode the clock of the receive V.22b bis high-pass filter is reduced to 64 kHz. This moves the pass band edge down to 1000 Hz. The low-pass and high-pass filters form a band pass which extends from 1000–3200 Hz. This filter passes the V.23 forward channel and rejects the backward channel.

103A Mode—This mode supports band split answering modems that operate according to the Bell 103 recommendation. In this mode the receive and transmit signals are separated by passing the composite signal through the receive filter which is configured as a low-band filter with a pass band range of 300–1600 Hz.

103O Mode—This mode supports a band split originating modem that operates according to the Bell 103 recommendation. In this mode the receive and transmit signals are separated by passing the composite signal through the receive filter which is configured as a band-pass filter with pass band edges extending from 2000–3200 Hz.

Normal mode—In this mode the receive filter consisting of the low-pass/high-pass combination form a band-pass which extends from 300–3200 Hz. This mode supports modems that operate according to the CCITT V.26, V.27, V.27 ter/bis, V.29, V.32 and V.33 recommendations. It can also be used for voice processing.

Note 1. In all the above modes, the echo canceller can still be operational and the filtered signal can go through the reconstruction filter unless it is independently disabled by the (ENEC) bit.

Note 2. In the Bell 103 and V.21 modes the receive signal should be sampled by a free running RxSTRB at the specified rate. This can be achieved by putting the RxDPLL in the free run mode. The TxDPLL should be placed in the free run mode due to the same reason.

TxFC	Transmit filter clock control. This bit controls the clock frequency for the transmit low-pass filter. If MD3=0, MD2=X, MD1=X, MD0=0 and TxFC=1 the transmit filter clock is cut to 1/2 of its nominal value. This moves the pass-band edge from 3.2 kHz to 1.6 or 1.28 kHz. In V.22/V.21/103 modes when the modem is set to operate as the originating modem the low-pass filter will clean the transmit spectrum in the high-band region. It is important to note that the transmit low-pass filter has a x/sin(x) shape in the pass band which is optimized for a 9.6 kHz sampling rate. If the clock frequency is cut into half, the x/sin(x) compensation will correspond to a 4.8 kHz sampling rate. This will put an additional 1 dB slope in the pass band of the low band signal. TXFC=1 TX filter clock cut into half TXFC=0 Normal operation (The above condition is only valid when the modem operates in the originating mode.)
NI	This bit (Notch Insert) controls the insertion of the 1800/550 Hz notch in the V.22 bis and answer mode. NI = 1 Notch Inserted NI = 0 Notch Bypassed
NSEL	This bit (Notch Select) selects the frequency of the notch. NSEL = 1 1800 Hz NSEL = 0 550 Hz
TEST1	This bit puts the chip in the test mode. When activated, the transmit sample-and-hold will be disconnected from the 12-bit DAC and will be connected to the output of the receive antialiasing filter. TEST1 = 1 Activate Test Mode TEST1 = 0 Deactivate Test Mode
TEST2	This bit activates a S/H circuit that is connected to the TX DAC output and is strobed by the TX STRB. This mode makes the output of the TX DAC accessible from outside and can be used to calibrate the 12-bit DAC. TEST2 = 1 Activate Test Mode TEST2 = 0 Deactivate Test Mode When the test mode is deactivated, the input of the S/H will be connected to ground.
TEST3	This bit activates a test mode which allows the testing of SCF2. In this mode, the input of SCF2 is connected to the output of the receive antialiasing filter and the output can be monitored at pin C1. TEST3 = 1 Activate Test Mode TEST3 = 0 Deactivate Test Mode

Transmit Serial Out Interface

This block converts the digital output of the 12-bit echo cancelling ADC to 16-bit serial words. Data transmission will start with a pulse on SOENT pin within 1 μsec after the falling edge of TxSTRB signal. A 16-bit word will be shifted out on the rising edges of SCLK, the 12 MSBs correspond to echo sample. This will be followed by another pulse on SOENT pin and a second 16-bit word corresponding to adaptive-hybrid output sample. The latter will not be generated if adaptive-hybrid is disabled (ENAH=0). If echo canceller is disabled there will not be any output on this port. Figure 15 shows the timing diagram of transmit serial output, with values specified in Table 1. The bit structure of output words are shown below:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT
EB11	EB10	EB9	EB8	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	—	—	—	—	ECHO Error Sample
HB11	HB10	HB9	HB8	HB7	HB6	HB5	HB4	HB3	HB2	HB1	HB0	SV4	SV3	SV2	SV1	AH Error Sample

EB0–11	12-bit 2's complement data representing the echo error sample. EB11 is the sign bit.
HB0–11	12-bit 2's complement data representing the error output from the adaptive hybrid. HB11 is the sign bit.
SV1–SV4	Sign of the signals V1–V4 sampled at the transmit strobe. SVi = 0 Vi Positive SVi = 1 Vi Negative

Note that MSB (D15) is shifted out first in time. The output digital words correspond to the samples taken on the falling edge of previous TxSTRB signal.

Receive Serial IN Interface

This block accepts 16-bit serial words consisting of address and control bits. MSB is the address bit and identifies one of the two internal registers. Following a pulse on SIENR, the data one SIR pin will be shifted in on the falling edges of SCLK (with MSB first in time) as shown in Figure 16a. The timing requirements are given in Table 3. When updating PGCR register the timing of Figure 16b should be followed which will result in implementation of new gain value on the next falling edge of RXSTRB.

The bit structure of receive serial input interface is shown below and is followed by bit definitions.

REG. NAME	ADD. BITS	CONTROL BITS														
	(MSB) D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PGCR	0	DPLL2	DPLL1	DPLL0	RDPF	RDPR	RDPA	PGC6	PGC5	PGC4	PGC3	PGC2	PGC1	PGC0	—	—
LVLR	1	—	—	—	—	—	—	—	—	—	RxST	RSINT	LV1	LVO	—	—

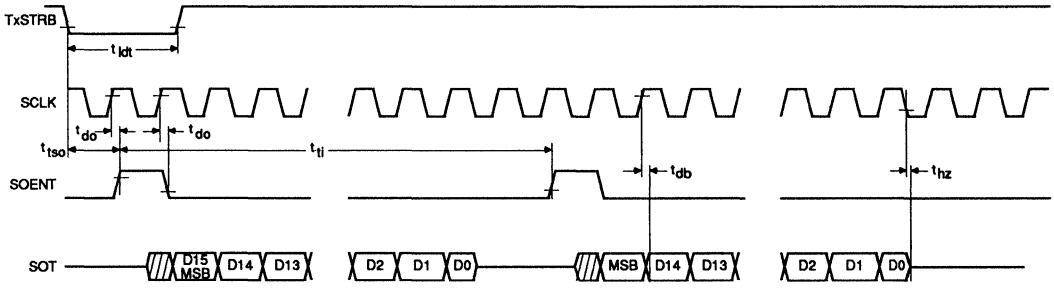


Figure 15. Tx Serial Output Timing With Respect to TxSTRB (For Echo/AH A/D)

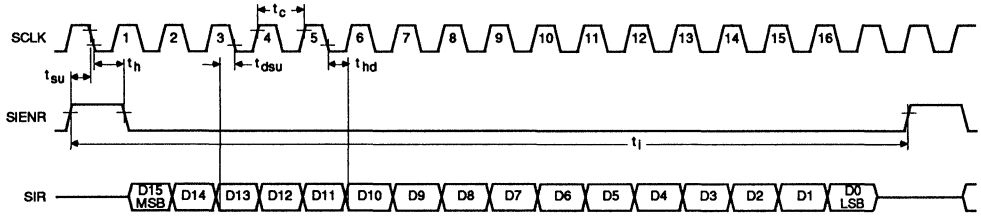


Figure 16a. Rx Serial Input Timing

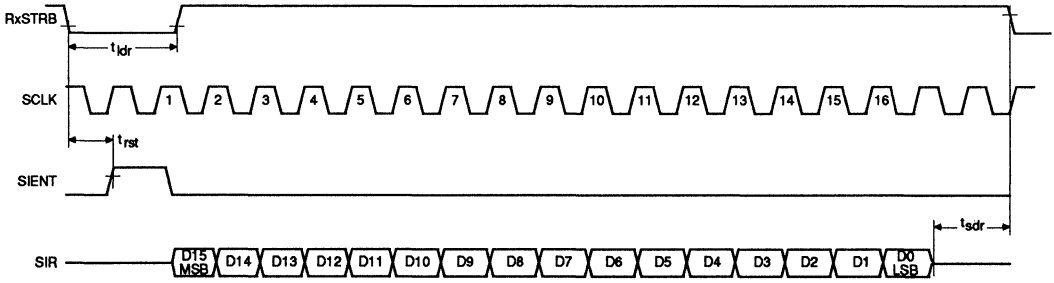


Figure 16b. Rx Serial Input Timing With Respect to RxSTRB (For Rx PGC Register)

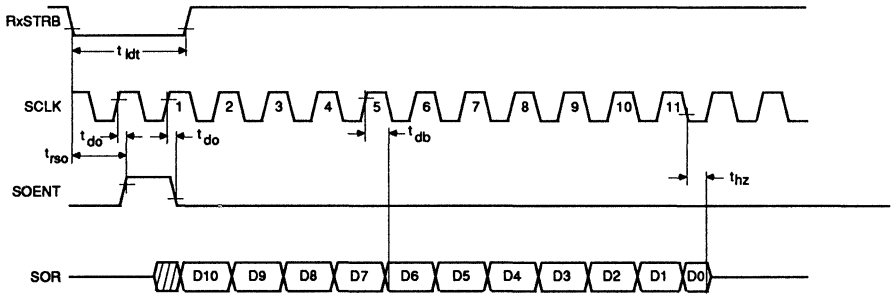


Figure 17. Rx Serial Output Timing With Respect to RxSTRB (For Rx A/D)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{su}	Set up time from SIENR high to SCLK low	80			ns
t_h	Hold time from SCLK low to SIENR low	50			ns
t_{hd}	Hold time from SCLK low to SIR transition	50			ns
t_{dsu}	Data set up time from SIR valid to SCLK low	80			ns
t_i	Interval between consecutive SIENR pulses	6.0			µs
t_{ldr}	Low duration of RxSTRB	.2		102	µs
t_{rst}	Set up time from RxSTRB low to SIENR high	20		92	µs
t_{sdr}	Delay time from last input data to RxSTRB low	0			ns
t_{rso}	Delay time from RxSTRB low to SOENR high	60		425	ns
t_{do}	Delay time from SCLK high to SOENR high			100	ns
t_{db}	Delay time from SCLK high to SOR valid			100	ns
t_{hz}	Hold time from SCLK low to SOR high impedance	50			ns
t_c	Serial clock period		325		ns

Table 3. Timing Requirements for Rx Serial Input/Output Interfaces

PGCR Register:

PGC0–PGC6

These bits control the programmable gain stage according to the following table:

PGC6	PGC5	PGC4	PGC3	PGC2	PGC1	PGC0	GAIN (dB)
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	.375
0	0	0	0	0	1	0	.75
0	0	0	0	1	0	0	1.5
0	0	0	1	0	0	0	3
0	0	1	0	0	0	0	6
0	1	0	0	0	0	0	12
1	0	0	0	0	0	0	24

RDPA, RDPR, RDPF

These bits control the receive DPLL as follows:

RDPA = 1 Advance Phase by Inserting Pulse(s)
RDPA = 0 No Operation

RDPR = 1 Retard Phase by Deleting Pulse(s)
RDPR = 0 No Operation

RDPF = 1 Fast Correction Mode
RDPF = 0 Slow Correction Mode

In slow correction mode, only one pulse (217 ns) will be inserted or deleted (per RDPA and RDPR state), whereas in fast mode the phase correction will be 8 times faster. Bits RDPA and RDPR will reset automatically after performing their correction.

DPLL0–2

These bits determine the mode of operation for receive DPLL. When all three are zero, then, DPLL will be controlled by RDPA, RDPR and RDPF bits. If any of DPLL0–2 bits is one, then, register bits RDPA, RDPR and RDPF will be ignored and DPLL will enter the coarse mode where its operation is determined according to the following table:

DPLL2	DPLL1	DPLL0	OPERATION
0	0	0	See RDPA, RDPR, RDPF bits
0	0	1	Delete 16 pulses
0	1	0	Delete 32 pulses
0	1	1	Delete 64 pulses
1	0	0	Delete 128 pulses
1	0	1	Delete 256 pulses
1	1	0	Delete 512 pulses
1	1	1	Delete 1024 pulses

LVLR Register:

LVL0—LVL1	The contents of these registers set the carrier detect level threshold. LVL1 LVL0 Off-to-On On-to-Off 0 0 –43 dBm –48 dBm 0 1 –33 dBm –38 dBm 1 0 –26 dBm –31 dBm 1 1 –16 dBm –21 dBm
RSINT	This bit determines whether the RX strobe is generated internally or supplied externally. RSINT = 1 Internal RSINT = 0 External In the external mode the RX DPLL will be disabled and the RXCLK will go to a high or low state.
RXST	Determines the rate of receive strobe. RXST = 1 9.6 kHz RXST = 0 7.2 kHz

Receive Serial Out Interface

This block generates an 11-bit serial word on SOR pin, following a pulse on SOEN pin. Data is shifted out on the rising edges of the shift clock as shown in Figure 17 which also illustrates the relationship with strobe. Timing specifications are given in Table 3. The bit structure of output word and their definition is as follows:

D12 (MSB)	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	ED

ED	This bit indicates the status of energy detect circuit. ED = 1 Energy Detected ED = 0 Energy not Detected
RD0–11	12-bit, 2's compliment data representing the receive signal sample. RD11 is the sign bit.

SPECIFICATIONS

Absolute Maximum Ratings (Notes 1, 2 and 3)

Supply Voltage, V_{DD}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS}–0.6 to V_{DD} +0.6 V
DC Input Voltage (Digital Signals)	V_{SS}–0.6 to V_{DD} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 s)	300°C

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating — Plastic Package: –12 mW/C from 65°C to 85°C.

Operating Conditions

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{DD}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
MCLK	Clock Frequency		9.2151	9.2160	9.2169	MHz
T_R, T_F	Input Rise or Fall Time	All Digital inputs except MCLK			50	ns
T_R, T_F	Input Rise or Fall Time	MCLK			30	ns

DC Electrical Characteristics (T_A = 0 to 70°C, V_{DD} = +5 V ± 10 %, V_{SS} = –5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current			25	50	mA
I_{SS}	Quiescent Current			25	50	mA
V_{IH}	High Level Input Voltage; Digital Pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital Pins				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Output (I_{OL} = 1.6 mA)				0.6	V
V_{OM}	Maximum Peak Output Level on TxOUT Pin	R_L = 1 kΩ	±2.5			V
V_{IM}	Maximum Peak Output Level on RxIN Pin				±2.5	V

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating — Plastic package: –12 mW/°C from 65°C to 85°C.

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Appendix A
Applications Aspects of the Adaptive Hybrid

Overview

An adaptive hybrid has been devised to significantly attenuate the near-end echoes. For example, Figure A.1 shows how the adaptive hybrid fits into a V.32 modem. A four stage correction network provides versatile correction of echoes with various characteristics. The echo reduction, by this network, consistently exceeds 25 dB, and is higher in most cases. In the V.32 modem application, this echo reduction makes it feasible to provide high performance without requiring the following:

1. A precision (14-bit) ADC.
2. 24-bit digital words in part of the echo canceller.

By reducing the echo by about 25 dB in the worst case, the word accuracy requirements are reduced by about 4 bits.

Correction Network

Figure A.2 shows the correction network without the learning. The four α's are learned during training. Then, in the V.32 modem, the α's are fixed, although they could adjust continually in some applications.

The following shows the basis of the correction. Let the echo path characteristic be $R(\omega) + jI(\omega)$. Each corrector stage has a characteristic $R_n(\omega) + jI_n(\omega)$. The overall corrector has the characteristic $R_C(\omega) + jI_C(\omega)$, where:

$$R_C(\omega) = \alpha_0 + \alpha_1 R_1(\omega) + \alpha_2 R_2(\omega) + \alpha_3 R_3(\omega) \quad \text{A2 · 1}$$

$$I_C(\omega) = \alpha_1 I_1(\omega) + \alpha_2 I_2(\omega) + \alpha_3 I_3(\omega) \quad \text{A2 · 2}$$

The objectives are to:

1. Select RC values for the individual stages such that various realistic echoes can be corrected.
2. Adapt to each echo path by selecting the α's to obtain $R_C(\omega) \approx R(\omega)$ and $I_C(\omega) \approx I(\omega)$.

The versatility is indicated by Equations A2.1 and A2.2, which show that we can exactly obtain any two desired points on each of the curves $R(\omega)$ and $I(\omega)$, although this would be generally sub-optimum. The smoothness of all curves involved indicates that we can obtain fairly accurate approximations of the realistic characteristics.

One recommendation for the RC values are:

$$R_1C_1 = 5 \times 10^{-5};$$
$$R_2C_2 = 2 \times 10^{-5}; \text{ and}$$
$$R_3C_3 = 1.5 \times 10^{-4}.$$

These RC selections were based upon trade-offs involving the following conflicting considerations. The capability to correct echo paths with large bends in the frequency domain characteristics can be enhanced by using stages that have large bends in their characteristics. Also, the stages need to substantially differ from each other to enhance versatility and to avoid excessive inter-stage inter-dependence in learning. Further, to avoid implementation complexity, it is desirable to constrain the α values to $-1<\alpha_n<1$. All of these considerations call for large RC values as well as using one high-pass stage and two low-pass stages. However, when the echo path frequency domain characteristic has small bends, these characteristics can be more accurately matched by stages with small RC values. The RC values were selected to enable us to meet the various objectives, including coverage of wide ranges and shapes of characteristics without using excessive RC values, which would degrade performance against moderately distorted echoes.

After preliminary estimates, we refined the RC selection by computer. First we selected some approximately worst case echo paths, which are typified by:

1. Large bends in the curves $R(\omega)$ and $I(\omega)$
2. Large ratios of $I(\omega)$ and $R(\omega)$

Then, we tried combinations of RC values to obtain a set of values that is approximately optimum, considering the stated objectives.

The Algorithm for Learning

Figure A.2 shows the meaning of symbols below. In a simple version of the learning, each coefficient, α_n, is updated once each sample time as follows:

$$(\Delta\alpha)_{m,n} = k\, E_m\, \mathrm{Sgn} V_n = \pm k |E_m| \quad \text{A3-1}$$

$$\alpha_{m,n} = \alpha_{m-1,n} + (\Delta\alpha)_{m,n} \quad \text{A3-2}$$

Where

m refers to the mth sample;
E_m = output Error;
k = constant; and
V_n = nth stage signal at input α_n.

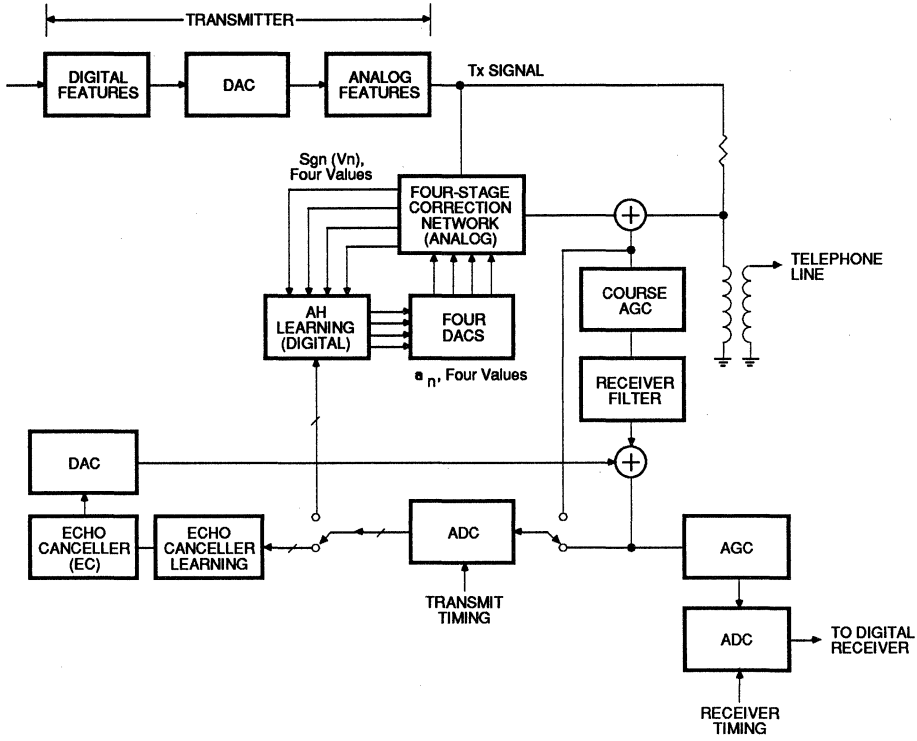

Figure A.1. Overview of Adaptive Hybrid and How it Fits Into A V.32 Modem

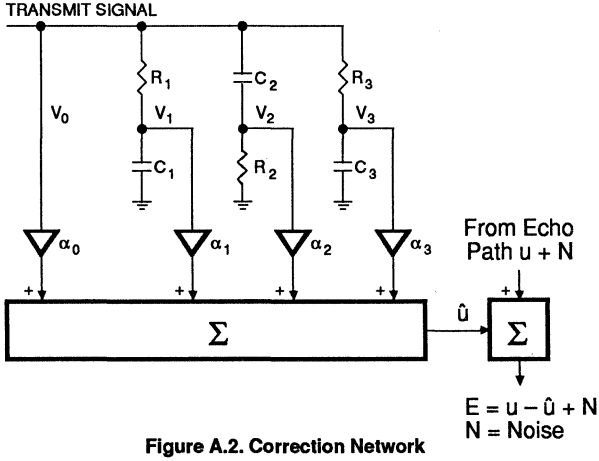

Figure A.2. Correction Network

If U_m represents the mth echo sample, and $\hat{U}_m$ is the echo correction sample, and N_m is random noise, we have:

$$E_m = U_m - \hat{U}_m + N_m = U_m - \sum_n(\alpha_{m,n} V_n) + N_m \qquad \text{A3-3}$$

For voiceband channels, practical sampling rates are in the range of 7200 to 9600 sps. Initially, $\alpha_0 = 0.5$, $\alpha_n = 0$ for n = 1–3 in the simplest case.

Let q_p be the optimum α_p, then neglecting noise,

$$E_m \, Sgn(V_n) = \sum_p [(q_p - \alpha_{m,p}) \, V_p] \, Sgn(V_n) \qquad \text{A3-4}$$

For the case of p = n, $V_n Sgn(V_n)$ is always positive. In the case of a random data signal for example, the effects of terms where $p \neq n$ tend to average to near zero. Thus, the $(q_n - \alpha_{m,n})V_n Sgn(V_n)$ always tries to drive α_n in the direction to reduce $(q_n - \alpha_n)$, and from Equation A.1, $\Delta\alpha$ has the right polarity to reduce the error most of the time. Since the increments, the $[\Delta\alpha]$, are very small, each α is driven generally in the correct direction, although a small percentage of the increments will be in the wrong direction.

If we had used V_n instead of $Sgn(V_n)$, this algorithm would have closely resembled the "Least-Mean-Square", LMS, algorithm often used for adaptive equalization and echo cancellation. For any particular E_m, at an arbitrary stage of the learning process, $E_m Sgn(V_n)$ will have the same polarity as $E_m V_n$. Therefore, at any particular error value, E_m, the proposed algorithm drives each α_n in the same direction as the LMS algorithm.

From Figure A.1 we see that use of the $\{Sgn(V_n)\}$ instead of the $\{V_n\}$ eliminates the need for four ADCs that would otherwise be needed.

Actually, we use a refined version of the algorithm described above. This version is given by:

$$(\Delta\alpha)_{m,n} = k_q \sum_{p=m}^{m-31} [E_p Sgn(V_{p,n})] \text{ for } m = 0, 4, 8, \text{etc.}$$

Updating occurs once every four sample times and each update is based upon the last 32 values of $E_p Sgn(V_{p,n})$. This version improves each updating loop characteristic. Also, it reduces the digital word size requirement, compared to the simple version, because it allows the error E_m to become smaller before $\Delta\alpha$ becomes smaller than the least significant bit.

Also, instead of a constant, k_q is reduced once every 32 sample times as follows:

$$k_q = 0.05(0.96)^q, \; q = m/32$$

and m = 0 at the start of training. This procedure allows the training to proceed rapidly at first, then slow down for higher precision.

Adaptation Procedure

The following general procedure is recommended for training the Adaptive Hybrid (See Figure A.3):

1. Train the Adaptive Hybrid (AH) from the same signal as the Echo Canceller (EC). However, some coarse training of the AH from earlier signals (with only a few frequency components) can be considered.
2. Use the total time duration allowed for the EC training signal, 8192/2400 = 3.413 sec.
3. Start the AH training at the beginning of this signal and finish it at about the middle.
4. At the end of the AH training, freeze the coefficients and leave them frozen until the next train or retrain. It is better not to have both the AH and EC adapting during data reception. Also, the EC can finish the last (precise) part of its training better if the AH is not fluctuating concurrently.
5. Start the EC training about 0.4 seconds after the AH training starts.

During the AH and EC training, no signal from the far end is present; and no AGC action occurs. When signal from the far end arrives, the AGC that precedes the EC is coarsely trained while the EC is temporarily frozen. The EC adaptation continues after the AGC is trained. However, the AGC gain should be automatically considered in selecting the coefficients that determines the echo estimates.

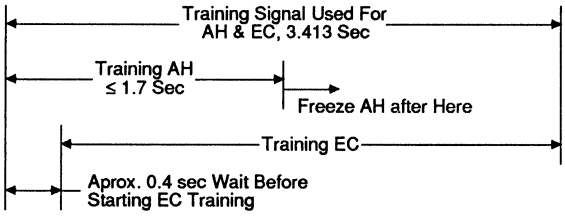

Figure A.3 AH & EC Training Procedure

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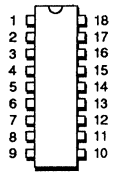
FEATURES

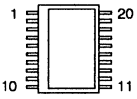
- ☐ CMOS EE Technology
- ☐ Single 5 V supply
- ☐ Reliable CMOS floating gate process
- ☐ 18-pin package
- ☐ Self-timed write operation
- ☐ Multiplexed address and data bus
- ☐ Data polling
- ☐ Typical 10,000 erase/write cycles
- ☐ Typical 10 years data retention

18-PIN DIP PACKAGE



SC22201CN

20-PIN SOIC PACKAGE



SC22201CM

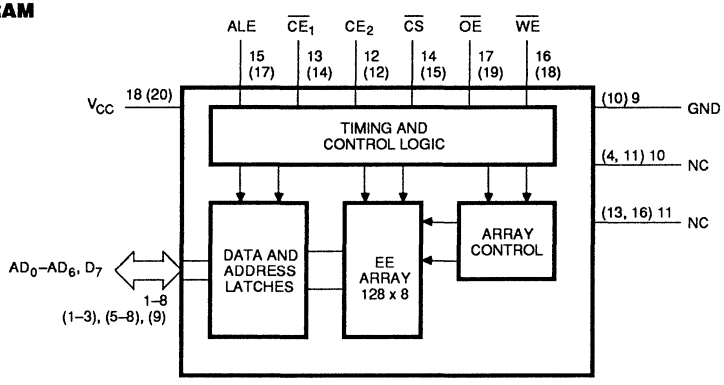
GENERAL DESCRIPTION

The SC22201 is a 128 by 8 programmable, non-volatile, parallel access memory built with Sierra's proprietary CMOS floating gate process. Data and address lines are multiplexed, enabling these devices to be packaged in an 18-pin DIP, saving board space. The pin-out is identical to the Intel 8185 static RAM and the 2001 Nonvolatile RAM, allowing the memories to directly interface with Intel and other popular 8-bit and 16-bit microprocessors and microcontrollers.

The write cycle is simplified by a self-timed erase before write circuit on-chip. The end of write cycle can be determined by polling the data pins, or the controller can simply allow a minimum time between a write command and the subsequent command. To prevent undesirable modification of the memory contents during system power up or power down, a lockout circuit ignores write commands while V_{CC} is below the prescribed level of VLKO.

Applications for these memories include storing position data in robotic systems, storing local area network node address and parameter settings in data communications equipment, storing set-up and last position data in industrial control systems and storing PBX switch data in telecommunications equipment.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PIN NUMBERS; NUMBERS IN ( ) ARE SOIC PIN NUMBERS.

PIN DESCRIPTIONS

PIN*	NAME	DESCRIPTION
1–8 (1–3), (5–8), (9)	AD_0–AD_6, D_7	Multiplexed address and data bits. D_7, Pin 8 and Pin (9), is DATA only.
(4)	NC	No connection
9 (10)	GND	Ground, 0 V.
10 (11)	NC	No connection
11 (13)	NC	No connection. No internal connection is made to this pin and it may be left floating.
12 (12)	CE2	Chip Enable 2 (see Table 1)
13 (14)	$\overline{CE1}$	Chip Enable 1 (see Table 1)
14 (15)	$\overline{CS}$	Chip Select (see Table 1)
(16)	NC	No connection
15 (17)	ALE	Address Latch Enable
16 (18)	$\overline{WE}$	Write Enable
17 (19)	$\overline{OE}$	Output Enable
18 (20)	V_{CC}	Positive power supply, 5 V.

* Pin numbers not in ( ) are for 18-pin DIP; those in ( ) are for 20 pin SOIC.

FUNCTIONAL DESCRIPTION

Table 1 shows the different modes of operation as a function of the control signals. Standby powered down mode: Both write and read are inhibited and the device's power consumption is greatly reduced. Standby powered up mode: the device consumes the operating power, but read and write are inhibited. Inhibit mode: the device is write protected to avoid inadvertent modifications while the read and write pins are changing.

Read Operation

Figure 2 shows the timing diagram for READ operation. The address as well as the states of $\overline{CE1}$ and CE2 are latched on the falling edge of ALE. Pins 1 through 7 are used for address bits.

Data appear on pins 1 through 8 after $\overline{OE}$ becomes active (low).

Write Operation

Write operation's timing is shown in Figure 3. Similar to the READ operation, the address and states of $\overline{CE1}$ and CE2 are latched on the falling edge of the ALE. After the address is latched, the $\overline{WE}$ becomes active (low) for the minimum time of TCC and returns to inactive state. This initiates the internally timed write operation. No external erase before write operation is needed and data lines as well as control lines may change after the write operation is initiated.

$\overline{DATA}$ Polling

After the write operation is initiated, its conclusion can be monitored by putting the device in the READ mode and polling the D7 data bit. The data bit will be logical inverse of the bit being written to a location in memory until the write operation is completed. At this time the D7 data bit will be the same as the last D7 data bit written into memory.

Write Lockout

During system power up or power down, an on-chip write lockout circuit prevents spurious WRITES into the memory locations while V_{CC} is lower than the specified lockout voltage VLKO. This frees the system designer from having to design external write protection circuits.

MODE	$\overline{CE1}$	CE2	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	AD_0–AD_7
Standby Powered Down	V_{IH}	X	X	X	X	Hi-Z
Standby Powered Down	X	V_{IL}	X	X	X	Hi-Z
Standby Powered Up	V_{IL}	V_{IH}	V_{IH}	X	X	Hi-Z
Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data In
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Hi-Z

Notes: V_{IL} = Logical Low Input V_{IH} = Logical High Input
Hi-Z = High Impedance State X = Don't Care
The $\overline{CE1}$ and CE2 inputs are latched by the falling edge of ALE.

Table 1. Modes

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}	7 V
Voltage on Any Pin	V_{CC}+0.5 V GND–0.5 V
Storage Temperature Range	–65 to +150°C
Maximum Power Dissipation @ 25°C (Note 2)	500 mW
Lead Temperature (Soldering 10 s)	300°C

A.C. TEST CONDITIONS

Output Load	1TTL gate and C_L = 100 pF
Input Rise and Fall Times (10% to 90%)	20 ns
Input Pulse Levels	0.0 V to 3.0 V
Input/Output Timing Reference Level	0.8 V and 2.0 V

OPERATING CONDITIONS (Applies to DC and AC Characteristics)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{IH}	High Level Input Voltage		2.0		V_{cc}+0.5	V
V_{IL}	Low Level Input Voltage		–0.5		0.8	V
V_{LKO}	V_{CC} Level for Write Lockout		3.8		4.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{CC}			±10.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC}			±10.0	µA
I_{CC}	Operating Supply Current	TTL Inputs			15.0	mA
		CMOS Inputs			10.0	mA
I_{CCPD}	Standby Supply Current	TTL Inputs			5.0	mA
		CMOS Inputs			100	µA
I_{SC}	Short-Circuit Current	1 Output Pin Shorted		40		mA
	Endurance			10,000		

Notes: 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", the device should not be operated at these limits. The table of "Electrical Characteristics" provides actual operating limits.
2. Power dissipation temperature derating—Plastic "N" package: –12 mW/°C from 65°C to 85°C.

CAPACITANCE (T_A = 25°C, f = 1 MHz) (Note 3)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0 V		5	10	pF
$C_{I/O}$	Input/Output Capacitance	$\overline{OE}$ = $\overline{CE1}$ = $\overline{CS}$ = V_{IH} CE2 = V_{IL}			10	pF

Note: 3. These parameters are sampled and not 100% tested.

AC CHARACTERISTICS

PARAMETER*	DESCRIPTION	MIN	MAX	UNITS
TAL	Address to Latch Setup Time	50		ns
TLA	Address Hold Time After Latch	45		ns
TLC	Latch to OE/WE Control	80		ns
TOE	Valid Data Out Delay from Read Control		170	ns
TLD	ALE to Data Out Valid		300	ns
TLL	Latch Enable Width	100		ns
TOH	Output Held from Addresses, $\overline{CS}$, or $\overline{OE}$ (whichever changes first)	0		ns
TOLZ	$\overline{OE}$ Low to Output Driven	10		ns
TRDF	Data Bus Float After Read	0	95	ns
TCL	OE/WE Control to Latch Enable	0		ns
TCC	OE/WE Control Width	250		ns
TDW	Data In to Write Setup Time	150		ns
TWD	Data In Hold Time After Write	20		ns
TSC	Chip Select Set-Up to OE/WE Control	50		ns
TCS	Chip Select Hold Time After OE/WE Control	10		ns
TALCE	Chip Enable Set-Up to ALE Falling	30		ns
TLACE	Chip Enable Hold Time After ALE Falling	45		ns
TWR	Byte Write Cycle Time		40	ms
TWH	Data Invalid After $\overline{WE}$ Falling		1	ms

*See Figures 2 and 3.

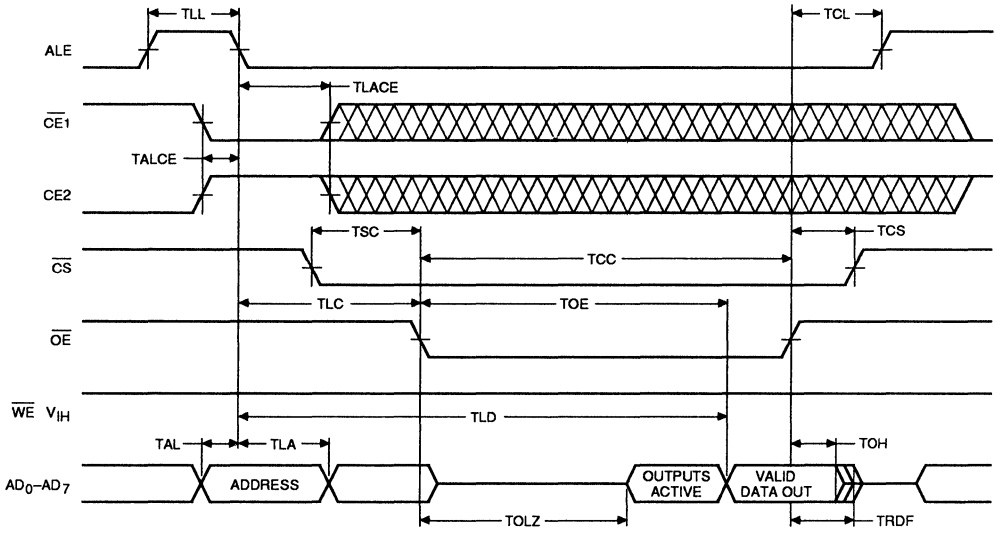


Figure 2. Read Timing

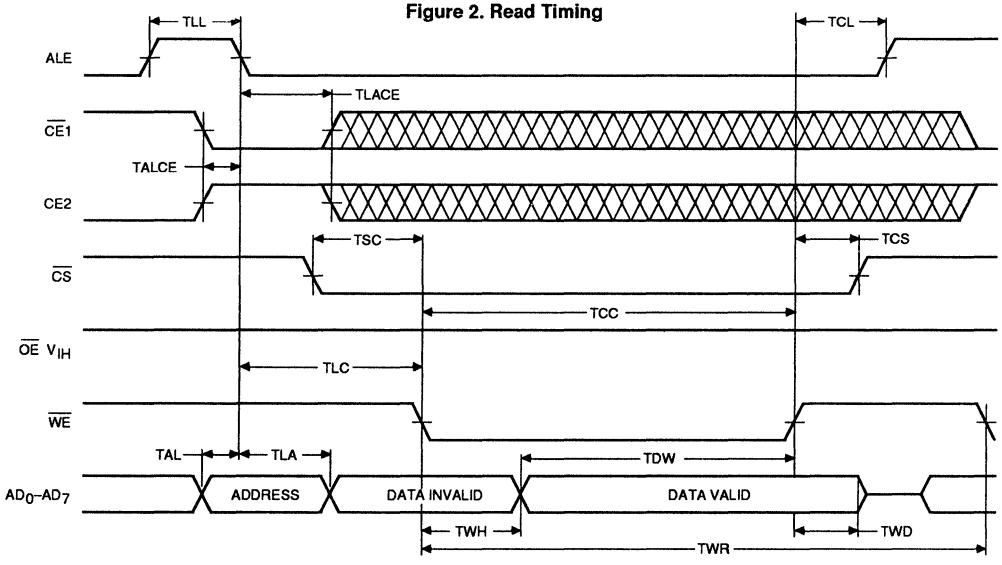
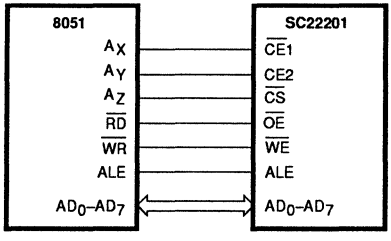


Figure 3. Write Timing



Note: A_X, A_Y, A_Z are any three of the 8051 address pins A_8–A_{15}. By connecting $\overline{CE1}$, CE2, and $\overline{CS}$ to specific address lines, the SC22201, can be mapped to a particular range in memory, without the need for an external memory address decoder.

Figure 4. Using The SC22201 with an 8051 Microcontroller

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Telecommunication Products 2

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FEATURES

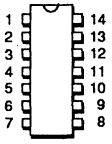
- ☐ Built-in dial tone rejection
- ☐ Single 5 Volt supply
- ☐ Three-state outputs
- ☐ Narrow 14 or 18 pin package

GENERAL DESCRIPTION

The SC11202, SC11203 and SC11204 are central office quality dual-tone, multi-frequency (DTMF)—touch tone—receivers built with Sierra's proprietary 3 micron CMOS process. They receive analog DTMF signals and decode them into the 16 standard digits. The SC11202 and SC11203 provide either a 4-bit hexadecimal code or binary coded 2 of 8, while the SC11204 provides 4-bit hex code only. The outputs are three state, CMOS logic compatible, facilitating bus interfaces. A built-in dial tone rejection circuit eliminates the need for any front-end or prefiltering. The only external components required are an inexpensive 3.58 MHz crystal and a bias resistor for the time base. Up to ten DTMF receivers may be operated from a single crystal through the Alternate Time Base (ATB) pin. The SC11202 is pin and function compatible to Silicon Systems' 202 (18 pin), the SC11203 is pin and function compatible with Silicon Systems' 203 (18 pin with an Early Detect output) and the SC11204 is a 14-pin device compatible with SSI's 204. Unlike the SSI parts, all Sierra DTMF Receivers include an integral dial tone rejection filter.

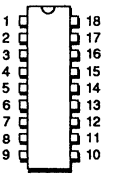
Applications include central office switches, PBXs, auto dialers for redialing a number over an alternate carrier, subscriber equipment such as telephone answering machines, remote banking or other transaction systems that employ DTMF signals for remote operation and voice/DTMF response systems.

14-PIN DIP PACKAGE



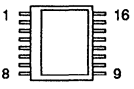
SC11204CN

18-PIN DIP PACKAGE



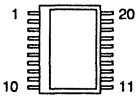
SC11202CN
SC11203CN

16-PIN SOIC PACKAGE



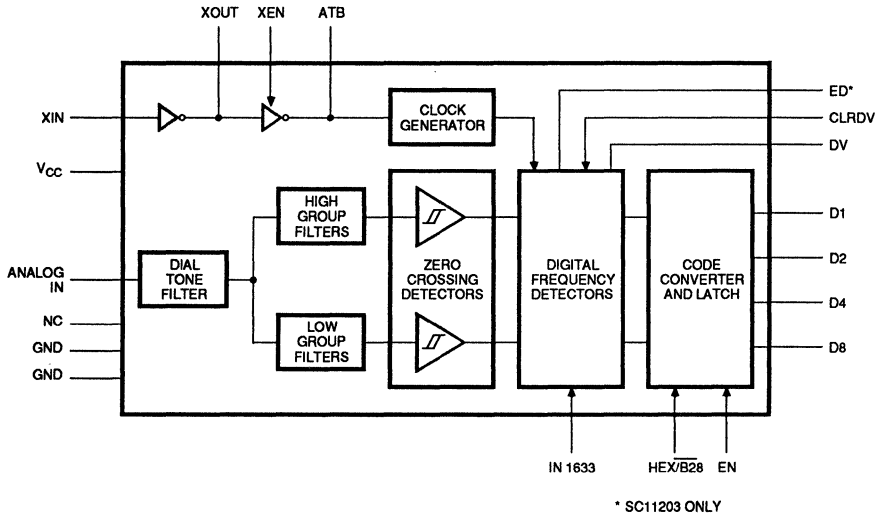
SC11204CM

20-PIN SOIC PACKAGE



SC11202CM
SC11203CM

BLOCK DIAGRAM



* SC11203 ONLY

PIN DESCRIPTION

PIN NAME	PIN NO.				FUNCTION
	SC11202 SC11203		SC11204		
	P1	P2	P3	P4	
D1 D2 D3 D4	1 18 17 16	1 20 19 18	2 1 14 13	2 1 16 15	Digital outputs that provide the code corresponding to the detected digit. These outputs are push-pull CMOS when EN (pin 3) is high and are a high impedance, open circuit, when EN is low. In the SC11202 and SC11203, the digital output format is programmed by the HEX/$\overline{B28}$ pin (2) to be either hexadecimal or binary coded 2 of 8 (see Table 3). In the SC11204 the output is hexadecimal and is on pins 2, 1, 14 and 13. These outputs become valid after a tone pair has been detected and they are cleared when a valid pause is timed.
HEX/$\overline{B28}$	2	2			Selects the digital output format on the SC11202 and SC11203. When HEX/$\overline{B28}$ is high, the outputs on D1, D2, D4 and D8 are hexadecimal; when it is low, the outputs are binary coded 2 of 8. See Table 3 for the hexadecimal and binary 2 of 8 codes.
EN	3	3	3	3	Enables the digital outputs D1, D2, D4 and D8.
IN1633	4	5			When tied high, this pin inhibits the detection of tone pairs containing the 1633 Hz component. To detect all 16 standard digits, IN1633 must be tied low. It has an internal pull-down to ground.
V_{CC}	5	6	4	4	Positive supply: 5 Volts.
ED	6*	8			Provided only on the SC11203, the ED output goes high as soon as a DTMF tone pair begins to be detected, and goes low when a pause begins to be detected. D1, D2, D4 and D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.
GND	7, 10	9, 12	8	9	Ground; 0 Volts. Pin 10 must be tied to ground; pin 7 is optional.
XEN	8	10	6	7	Enables the crystal oscillator. When high, the crystal oscillator is enabled. This pin should be tied low if the device is driven by an external oscillator through the ATB input.
Analog IN	9	11	7	8	Accepts the analog input. This pin is internally biased so that the input signal may be AC coupled through a 0.01 µF capacitor. The input may be DC coupled as long as it does not exceed the positive supply.
XOUT XIN	11 12	13 14	9 10	10 11	Crystal oscillator output and input. A 3.58 MHz crystal in parallel with a 1 MΩ, 10% resistor is connected between these pins. The oscillator is enabled by tying XEN (pin 8) high. In this mode, the clock frequency is also provided at the ATB output (pin 13).
ATB	13	15	11	12	Alternate time-base. For a device with a crystal and a resistor connected between pins 11 and 12, and XEN tied high. ATB is a 447.5 KHz clock output that can be used to drive up to ten other DTMF receivers. For these devices, XEN must be tied low and ATB is an input.
DV	14	16	12	14	Data valid and clear data valid. DV goes high after a valid tone pair is sensed and decoded at the output of pins D1, D2, D4 and D8. DV remains high until a valid pause occurs or until the CLRDV input is taken high, whichever occurs first.
NC			5		NC indicated that no internal connection is made to the pin and it may be left floating.

NOTES: P1 is the 18-pin DIP; P2 is the 20-pin SOIC; P3 is the 14-pin DIP; P4 is the 16-pin SOIC
* Pin 6 not connected on SC11202

PIN DESCRIPTIONS (Cont.)

Table 1. DTMF Dialing Matrix

	COL 0	COL 1	COL 2	COL 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

Table 2. Detection Frequency

LOW GROUP f_o	HIGH GROUP f_o
Row 0 = 697 Hz	Col. 0 = 1209 Hz
Row 1 = 770 Hz	Col. 1 = 1336 Hz
Row 2 = 852 Hz	Col. 2 = 1477 Hz
Row 3 = 941 Hz	Col. 3 = 1633 Hz

Table 3. HEX/$\overline{B28}$ Output Codes

	HEXADECIMAL				BINARY CODED 2 OF 8			
DIGIT	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, V_{CC}	7 V
DC Input Voltage	–0.5 to V_{CC} + 0.5 V
Analog Input Voltage	V_{CC} – 10 V to V_{CC} + 0.5 V
Storage Temperature Range	–65°C to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (soldering 10 sec)	300°C

OPERATING CONDITIONS (Note 4)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5		5.5	V
GND	Ground			0		V
F_C	Crystal Frequency		3.576	3.579545	3.583	MHz

Notes:
1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified all voltages are referenced to ground.
3. Power dissipation temperature derating:
   Plastic package: –12mW/C from 65°C to 85°C
   Ceramic package: –12mW/C from 100°C to 125°C.

ELECTRICAL CHARACTERISTICS (Note 4)

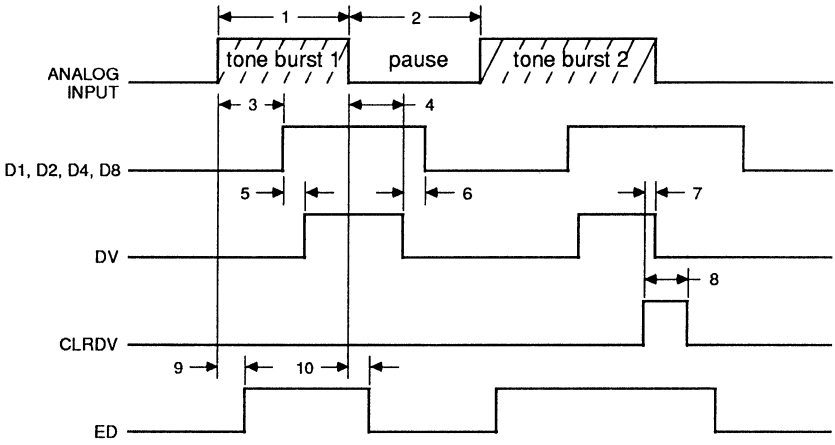
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5+2 Hz)	±2.3	±3.5	% of f_o
Amplitude for Detection	Each Tone	–32		–2	dBM Referenced to 600Ω
Minimum Acceptable Twist	Twist = $\frac{\text{High Tone}}{\text{Low Tone}}$	–10		+10	dB
60 Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	'Precise' Dial Tone			18.0	dB Referenced to Lower Amplitude Tone
Talk Off	MITEL Tape #CM 7291		2		Hits
Digital Ouputs (except XOUT)	'0' Level 400 µA Load	0		0.5	Volts
	'1' Level 200 µA Load	V_{CC}–0.5		V_{CC}	Volts
Digital Inputs	'0' Level	0		0.3 V_{CC}	Volts
	'1' Level	0.7 V_{CC}		V_{CC}	Volts
Power Supply Noise	Wide Band			10	mVp–p
Supply Current	T_A = 25°C		10	16	mA
Noise Tolerance	MITEL Tape #CM 7291			–12	dB Referenced to Lowest Amplitude Tone
Input Impedance	$V_{CC} \geq V_{IN}$ V_{CC}–10	100 kΩ//15 pFk			

Notes: 4. Min and max values are valid over the full temperature and operating voltage range. Typical values are for 25°C and 5 V operation.

TIMING CHARACTERISTICS (at 25°C and 5 V supply)

NO	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
1	TON	Tone Time for Detection		40			ms
1	TON	Tone Time for Rejection				20	ms
2	TOFF	Pause Time for Detection		40			ms
2	TOFF	Pause Time for Rejection				20	ms
3	TD	Detect Time		25		46	ms
4	TR	Release Time		35		50	ms
5	TSU	Data Setup Time		7			µs
6	TH	Data Hold Time		4.2		5.0	ms
7	TCL	DV Clear Time			160	250	ns
8	TPW	CLRDV Pulse Width		200			ns
9	TED	ED Detect Time		7		22	ms
10	TER	ED Release Time		2		18	ms
	TOE	Output Enable Time	C_L = 50 pF, R_L = 1 kΩ		200	300	ns
	TOD	Output Disable Time	C_L = 35 pF, R_L = 500 Ω		150	200	ns
	TOR	Output Rise Time	C_L = 50 pF		200	300	ns
	TOF	Output Fall Time	C_L = 50 pF		160	250	ns

TIMING CHARACTERISTICS (Cont.)

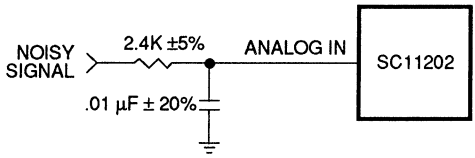


APPLICATION NOTES

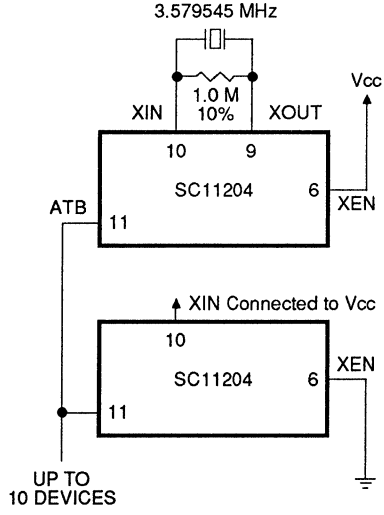
The DTMF receiver will tolerate total input rms noise up to 12 dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to the DTMF receiver unnecessary. However, noise near the 74.6 kHz internal sampling frequency will be aliased (folded back) into the audio spectrum; if excessive noise is present above 37.3 kHz, the simple RC filter shown below can be employed to band limit the incoming signal. Noise will also be reduced by placing a ground trace around the XIN and XOUT pins on the circuit board layout when using a crystal. XOUT is not intended to drive an additional device. XIN may be driven externally in which case XOUT must be left floating.

Crystal Oscillator

The DTMF receivers contain an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television color-burst crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ, 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other DTMF receivers may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single DTMF receiver with a crystal as shown below.



For use in extreme high frequency input noise environment.



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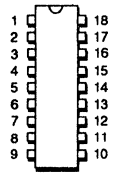
FEATURES

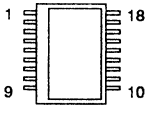
- ☐ Complete receiver in an 18-pin package
- ☐ Excellent performance
- ☐ CMOS, single 5 Volt operation

18-PIN DIP PACKAGE



SC11270CN/
SC11271CN

18-PIN SOIC PACKAGE

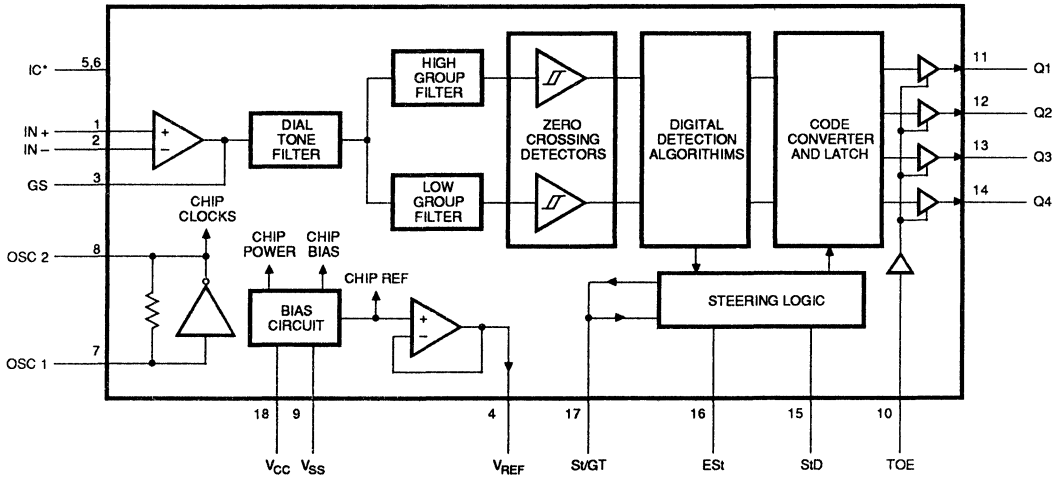


SC11270CM/
SC11271CM

GENERAL DESCRIPTION

The SC11270/SC11271 are complete DTMF receivers integrating both the bandsplit filter and digital decoder functions. They are fabricated with Sierra Semiconductor's double-poly CMOS technology and are pin and function compatible with the MITEL, MT8870 and MT8870B-1 DTMF receivers, respectively. The filter section uses switched capacitor techniques for high- and low-group filters and dial tone rejection. Digital counting techniques are employed in the decoder to detect and decode all 16 DTMF tone-pairs into a 4 bit code. External component count is minimized by on-chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface. The SC11271 conforms to CEPT specifications for DTMF receivers systems by providing a must reject signal level of –37 dBm.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINS; NUMBERS IN ( ) ARE PLCC PINS. PINS (5), (7), (8), (9), (10), (11), (17), (18), (20), (24), (25), AND (26), ARE NOT CONNECTED.

* CONNECT TO V_{SS}

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION	
1	IN+	Non-Inverting Input	Connections to the front-end differential amplifier.
2	IN–	Inverting Input	
3	GS	Gain Select. Gives access to output of front-end differential amplifier for connection of of feedback resistor.	
4	V_{REF}	Reference voltage output, nominally $V_{CC}/2$. May be used to bias the inputs at mid-rail (see application diagram).	
5, 6	IC	Internal Connection. Must be tied to V_{SS}.	
7	OSC1	Clock Input	3.579545 MHz crystal connected between these pins completes internal oscillator.
8	OSC2	Clock Output.	
9	V_{SS}	Negative power supply, normally connected to 0 V.	
10	TOE	3-state output enable (input). Logic high enables the outputs Q_1–Q_4. Internal pull-up.	
11–14	Q_1–Q_4	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see code table).	
15	StD	Delayed steering output. Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.	
16	ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
17	St/GT	Steering input/guard time output (bi-directional). A voltage greater than VTS_t detected at St causes the device to register the detected tone-pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St (see truth table).	
18	V_{CC}	Positive power supply, +5 V.	

FUNCTIONAL DESCRIPTION

The SC11270/271 monolithic DTMF receivers offer small size, low power consumption and high performance. The architecture consists of a bandsplit filter section, which separates the high and low tones of a receiver pair, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two filters—a sixth order for the high group and an eight order for the low group. The bandwidths of which correspond to the bands enclosing the low-group and high-group tones (see Figure 5). The filter section also incorporates notches at 350 Hz and 440 Hz for exceptional dial-tone rejection. Each filter output is followed by a second order switched-capacitor section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals and noise; the outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The decoder uses digital counting techniques to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals, such as voice, while providing tolerance to small

frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals ("third tones") and noise. When the detector recognizes the simultaneous presence of two valid tones (referred to as "signal condition" in some industry specifications), it raises the "early steering" flag (ESt). Any subsequent loss of signal-condition will cause ESt to fall.

Steering Circuit

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time-constant driven by ESt. A logic high on ESt causes V_C (see Figure 6) to rise as the capacitor discharges. Provided signal-condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone-pair, latching its corresponding 4-bit code (see Figure 3) into the output latch. At this point, the GT output is activated and drives V_C to V_{CC}. GT continues to drive high as long as ESt remains high. Finally after a short delay to allow the output latch to settle, the "delayed-steering" output flag, StD, goes high, signaling that a received tone-pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the 3-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions ("drop-out") too short to be considered a valid pause. The facility, together with the capability of selecting the steering time-constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring independent selection of receive and pause, the simple steering circuit of Figure 6 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a parameter of the device (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 ms would be 300k.

Different steering arrangements may be used to select independently the guard-times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and inter-digital pause.

Guard-time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard-time adjustment is shown in Figure 7.

Input Configuration

The input arrangement of the SC11270 provides a differential-input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 2 with the op-amp connected for unity gain and V_{REF} biasing the input at 1/2 V_{CC}. Figure 8 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

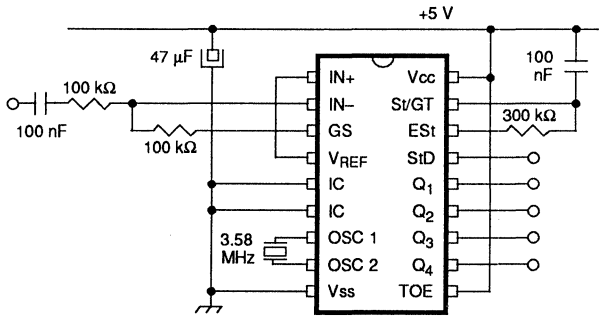
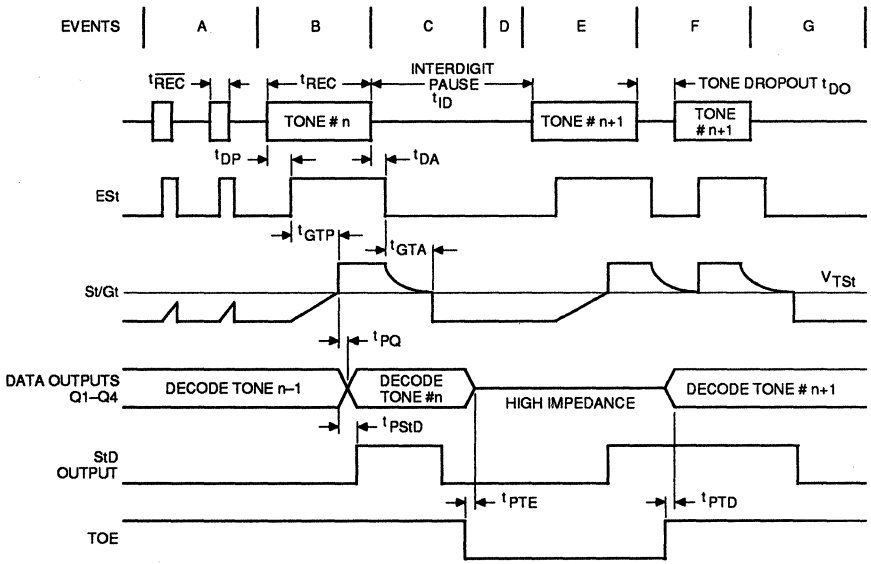


Figure 2. Single Ended Input Configuration

F_{low}	F_{high}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
–	–	ANY	L	Z	Z	Z	Z

"L = Logic Low, H = Logic High, Z = High Impedance"

Figure 3. Logic Table



A. Short tone bursts: detected. Tone duration is invalid.
B. Tone #n is detected. Tone duration is valid. Decoded to outputs.
C. End of tone #n is detected and validated.
D. 3 State outputs disabled (high impedance).
E. Tone #n+1 is detected. Tone duration is valid. Decoded to outputs.
F. Tristate outputs are enabled. Acceptable drop out of tone #n+1 does not register at outputs
G. End of tone #n+1 is detected and validated.

Figure 4. Timing Diagram

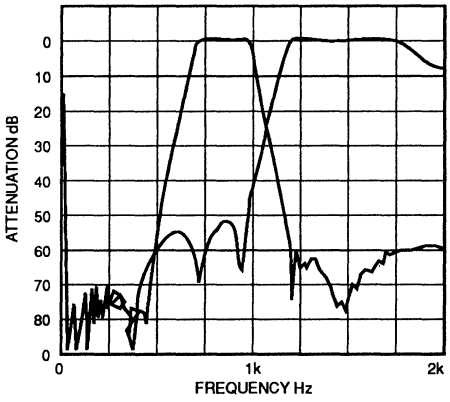
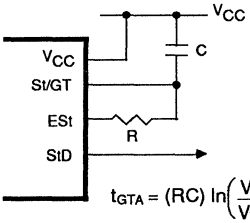


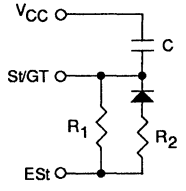
Figure 5. Typical Filter Characteristic



$$t_{GTA} = (RC)\ln\left(\frac{V_{CC}}{V_{TST}}\right)$$

$$t_{GTP} = (RC)\ln\left(\frac{V_{CC}}{V_{CC} - V_{TST}}\right)$$

Figure 6. Basic Steering Circuit

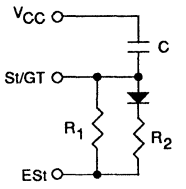


$$t_{GTP} = (Rp\ C)\ln\left(\frac{V_{CC}}{V_{CC} - V_{TST}}\right)$$

$$t_{GTA} = (R_1C)\ln\left(\frac{V_{CC}}{V_{TST}}\right)$$

$$Rp = \frac{R_1R_2}{R_1 + R_2}$$

a) Decreasing t_{GTP} ($t_{GTP} > t_{GTA}$)



$$t_{GTP} = (R_1C)\ln\left(\frac{V_{CC}}{V_{CC} - V_{TST}}\right)$$

$$t_{GTA} = (Rp\ C)\ln\left(\frac{V_{CC}}{V_{TST}}\right)$$

$$Rp = \frac{R_1R_2}{R_1 + R_2}$$

b) Decreasing t_{GTA} ($t_{GTP} > t_{GTA}$)

Figure 7. Guard Time Adjustment

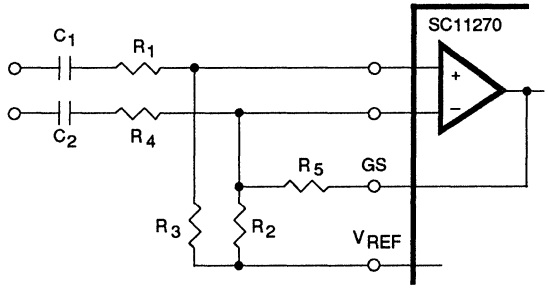


Figure 8 Differential Input Configuration

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, V_{CC} – V_{SS}	+6 V
Voltage on any Pin	V_{SS}–0.3 to V_{CC}+0.3 V
Current at any Pin	10 mA
Operating Temperature	–40 to +85°C
Storage Temperature	–65 to +150°C
Power Dissipation (Note 3)	500 mW

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

DC ELECTRICAL CHARACTERISTICS (Notes 1 and 2)

PARAMETER	DESCRIPTION		TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY							
V_{CC}	Operating Supply Voltage			4.75		5.25	V
I_{CC}	Operating Supply Current				3.0	7	mA
P_O	Power Consumption		f=3.579 MHz; V_{CC}=5 V		15	35	mW
INPUTS							
V_{IL}	Low Level Input Voltage					1.5	V
V_{IH}	High Level Input Voltage			3.5			V
I_{IH}/I_{IL}	Input Leakage Current		V_{IN}=V_{SS} or V_{CC}		0.1		µA
I_{SO}	Pull Up (Source) Current		TOE (Pin 10)=0 V		7.5	15.0	µA
R_{IN}	Input Impedance	Signal Inputs 1, 2	@ 1 kHz		10		MΩ
V_{TSt}	Steering Threshold Voltage				2.35		V
OUTPUTS							
V_{OL}	Low Level Output Voltage		No Load		0.03		V
V_{OH}	High Level Output Voltage		No Load		4.97		V
I_{OL}	Output Low (Sink) Current		V_{OUT}=0.4 V	1.0	2.5		mA
I_{OH}	Output High (Source) Current		V_{OUT}=4.6 V	0.4	0.8		mA
V_{REF}	Output Voltage	V_{REF}	No Load	2.4		2.7	V
R_{OR}	Output Resistance				10		kΩ

OPERATING CHARACTERISTICS

Gain Setting Amplifier

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_N	Input Leakage Current	$V_{SS}<V_{IN}<V_{CC}$		±100		nA
R_{IN}	Input Resistance			10		MΩ
V_{OS}	Input Offset Voltage			±25		mV
PSRR	Power Supply Rejection	1 kHz		60		dB
CMRR	Common Mode Rejection	$-3.0\ V<V_{IN}<3.0\ V$		60		dB
A_{VOL}	DC Open Loop Voltage Gain			65		dB
f_C	Open Loop Unity Gain Bandwidth			1.5		MHz
V_O	Output Voltage Swing	$R_L \geq 100\ k\Omega$ to V_{SS}		4.5		V_{PP}
C_L	Tolerable Capacitive Load (GS)			100		pF
R_L	Tolerable Resistive Load (GS)			50		kΩ
V_{CM}	Common Mode Range	No Load		3.0		V_{PP}

Notes: 1. All voltages referenced to V_{SS} unless otherwise noted.
2. $V_{CC} = 5.0\ V$, $V_{SS} = 0\ V$, $T_A = 25°C$.

AC ELECTRICAL CHARACTERISTICS

All voltages referenced to V_{SS} unless otherwise noted. $V_{CC} = 5.0\ V$, $V_{SS} = 0\ V$, $T_A = 25°C$, $F_{CLK} = 3.579545$ MHz, using test circuit of Figure 2.

PARAMETER	DESCRIPTION			MIN	TYP	MAX	UNITS	NOTES
SIGNAL CONDITIONS								
	Valid Input Signal Level (each tone of composite signal)	MIN				-29	dBm	1,2,3,5,6,9
						27.5	mV_{RMS}	1,2,3,5,6,9
		MAX		+1			dBm	1,2,3,5,6,9
				883			mV_{RMS}	
	Twist Accept Limit		Positive		10		dB	2,3,6,9
			Negative		10		dB	
NON-ACCEPT LEVEL						**-37**	**dBm**	**1,2,3,4,5,9**
	Freq. Deviation Accept Limit					±1.5% ±2 Hz	Nom.	2,3,5,9
	Freq. Deviation Reject Limit			±3.5%			Nom.	2,3,5
	Third Tone Tolerance				-16		dB	2,3,4,5,9,10
	Noise Tolerance				-12		dB	2,3,4,5,7,9,10
	Dial Tone Tolerance				+18		dB	2,3,4,5,8,9,10

AC ELECTRICAL CHARACTERISTICS

All voltages referenced to V_{SS} unless otherwise noted. V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = 25°C, F_{CLK} = 3.579545 MHz, using test circuit of Figure 2.

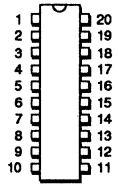
PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS	NOTES
TIMING							
t_{DP}	Tone Present Detection Time		5	14	16	ms	Refer to Fig. 4
t_{DA}	Tone Absent Detection Time		0.5	4	8.5	ms	
t_{REC}	Tone Duration Accept				40	ms	(User Adjustable)
t_{REC}	Tone Duration Reject		20			ms	
t_{ID}	Interdigit Pause Accept				40	ms	Refer to "Guard Time Adjustment"
t_{DO}	Interdigit Pause Reject		20			ms	
OUTPUTS							
t_{PQ}	Propagation Delay (St to Q)			8	11	µs	TOE=V_{CC}
t_{PSED}	Propagation Delay (St to StD)			12		µs	
t_{QSED}	Output Data Set Up (Q to StD)			4.5		µs	
t_{PTE}	Propagation Delay (TOE to Q)	DISABLE		50	60	ns	R_L=10 kΩ
t_{PTD}		ENABLE		300		ns	C_L=50 pF
CLOCK							
f_{CLK}	Crystal/Clock Frequency		3.5759	3.5795	3.581	MHz	
C_{LO}	Clock Output (OSC2)	Capacitive Load			30	pF	

Notes:
1. dBm = decibels above or below a reference power of 1 mW into a 600 Ω load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms, Tone pause = 40 ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ±2 Hz.
7. Bandwidth limited (3 kHz) Gaussian Noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%.
9. For an error rate of less than 1 in 10,000.
10. Referenced to the lowest level frequency component in DTMF signal.

FEATURES

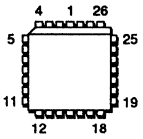
- ☐ Complete DTMF transmitter/receiver
- ☐ Excellent performance
- ☐ Single 5 Volt supply CMOS technology
- ☐ Microprocessor port
- ☐ Adjustable guard time/Automatic tone burst mode/Call progress mode

20-PIN DIP PACKAGE



SC11280CN

28-PIN PLCC PACKAGE

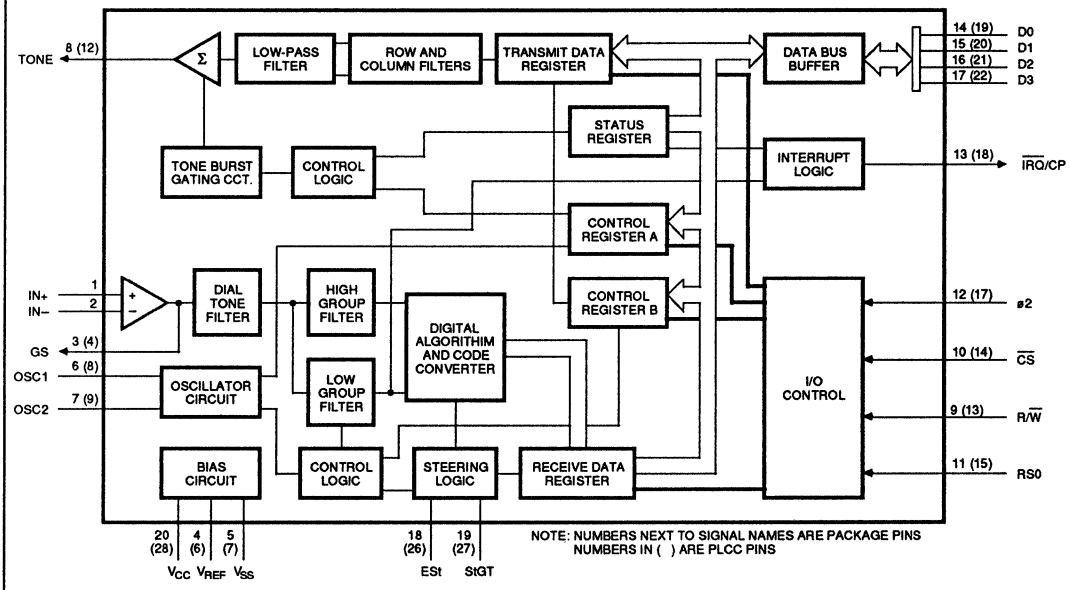


SC11280CV

GENERAL DESCRIPTION

The SC11280 is a monolithic DTMF transceiver with call progress filter. It is fabricated in Sierra's proprietary 3 micron CMOS technology which provides low power dissipation and high reliability. The DTMF receiver is based upon the industry standard SC11270 monolithic DTMF receiver; the transmitter utilizes a switched capacitor filter for low distortion, high accuracy DTMF signaling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones. A standard microprocessor bus is provided and is directly compatible with 6800 series microprocessors.

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	IN+	Non-inverting op-amp input.
2	IN–	Inverting op-amp input.
3 (4)	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4 (6)	V_{REF}	Reference voltage output, nominally $V_{CC}/2$ is used to bias inputs at mid-rail (see application diagram).
5 (7)	V_{SS}	Negative power supply input.
6 (8)	OSC1	DTMF clock/oscillator input.
7 (9)	OSC2	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.
8 (12)	TONE	Dual Tone Multi-Frequency output.
9 (13)	R/$\overline{W}$	Read/Write input. Controls the direction of data transfer to and from the MPU and the receiver/transmitter, TTL compatible.
10 (14)	$\overline{CS}$	Chip Select, TTL input ($\overline{CS}$ = 0 to select the chip).
11 (15)	RS0	Register select input. See register decode table, TTL compatible.
12 (17)	ø2	System clock input, TTL compatible.
13 (18)	$\overline{IRQ}$/CP	Interrupt request to MPU (open drain output). Also, when call progress (CP) mode has been selected and interrupt enabled the $\overline{IRQ}$/CP pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter. See Figure 11.
14–17 (19–22)	D0–D3	Microprocessor data bus (TTL compatible).
18 (26)	ESt	Early Steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19 (27)	StGT	Steering input/Guard Time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
20 (28)	V_{CC}	Positive power supply input.
(3, 5, 10, 11, 16, 23, 24, 25)	N.C.	No Connection.

FUNCTIONAL DESCRIPTION

The SC11280 integrated DTMF Transceiver architecture consists of a high performance DTMF receiver with internal gain setting amplifier and a DTMF generator which employs a burst counter such that precise tone bursts and pauses can be synthesized. A call progress mode can be selected such that frequencies within the specified pass band can be detected. A standard microprocessor interface allows access to an internal status register, two control registers and two data registers.

Input Configuration

The input arrangement of the SC11280 provides a differential-input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at $V_{CC}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single ended configuration, the input pins are connected as shown in Figure 1. Figure 2 shows the necessary connections for a differential input configuration.

Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched-capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies (see Figure 5). The low group filter also incorporates notches at 350 Hz and 440 Hz for exceptional dial-tone rejection. Each filter output is followed by a second-order switched-capacitor filter section which

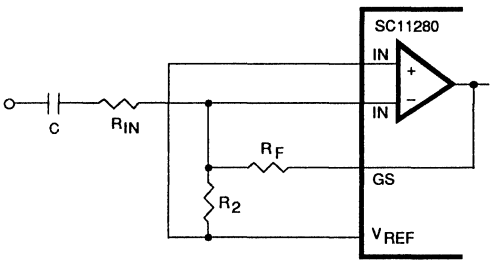


Figure 1. Single Ended Input Configuration

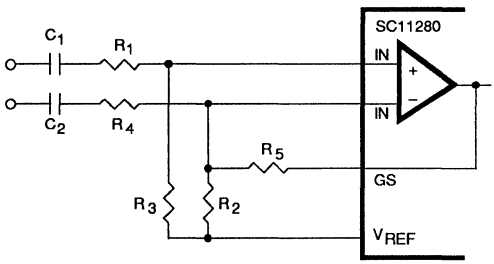


Figure 2. Differential Input Configuration

smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see Steering Circuit).

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (see Figure 3) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Figure 5) into the Receive Data Register. At this point the GT output is activated and drives V_C to V_{CC}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signalling that a received tone pair has been registered. It is possible to monitor the status of the delayed steering flag by checking the appropriate bit in the status register. If interrupt mode has been selected, the IRQ/CP pin will pull low when the delayed steering flag is active.

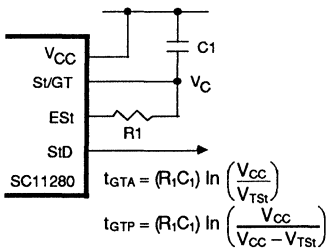


Figure 3. Basic Steering Circuit

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the 4-bit bi-directional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

The simple steering circuit shown in Figure 3 is adequate for most applications. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer. Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC}

with a long t_{DO} would be appropriate for extremely noisy environments where fast drop-outs are required. Design information for guard time adjustment is shown in Figure 4.

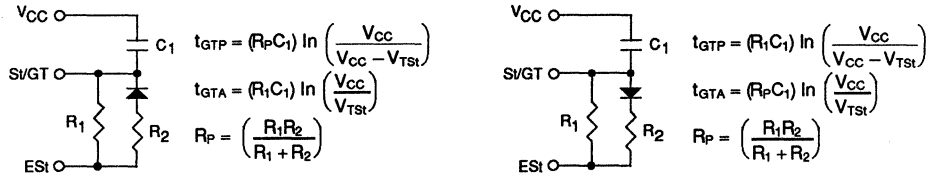


Figure 4. Guard Time Adjustment

Call Progress Filter

A call progress mode can be selected allowing the detection of various tones which identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common, however, call progress tones can only be detected when CP mode has been selected. DTMF signals cannot be detected if CP mode has been selected (see Table 1). Figure 6 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input (IN+ and IN–) which are within the 'accept' bandwidth limits of the filter are hard limited by a high gain comparator with the IRQ/CP pin serving as the output. The square wave output obtained from the Schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies which are in the 'reject' area will not be detected and consequently there will be no activity on IRQ/CP as a result of these frequencies.

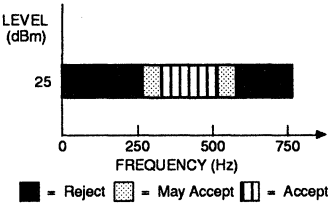


Figure 6. Call Progress Monitor

DTMF Generator

The DTMF transmitter employed in the SC11280 is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.58 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched-capacitor filters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Figure 5 must be written to the transmit data register. Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as Low Group and High Group tones. As seen from the table in Figure 5, the low group frequencies are 697, 770, 852, and 941 Hz. The high group frequencies are 1209, 1336, 1477, and 1633 Hz. Typically the high group to low group amplitude ratio (twist) is 2 dB to compensate for high group attenuation on long loops.

F_{low}	F_{high}	DGT	D_4	D_3	D_2	D_1
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

Figure 5. Functional Encode/Decode Table

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		
	SPECIFIED	ACTUAL	% ERROR
L1	697	699.1	+0.30
L2	770	766.2	–0.49
L3	852	847.4	–0.54
L4	941	948.0	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	–0.32
H3	1447	1477.9	–0.35
H4	1633	1645.0	+0.73

Table 1. Actual Frequencies Versus Standard Requirements

DTMF Generator Operation

The period of a tone is controlled by varying the divide ratio of a programmable divider. During write operations to the Transmit Data Register, the 4 bit data on the bus is latched and converted to 2 of 8 coding for use by the divider circuitry. The divider output is passed through a switched-capacitor low-pass filter to attenuate harmonic components. Two similar circuits are emplyed to produce row and column tones which are then mixed using a summing amplifier. The oscillator described needs no "start-up" time as in other DTMF generators since the crystal oscillator is running continuously thus providing a high degree of tone burst accuracy. Under conditions when there is no tone output signal, the TONE OUT pin assumes a DC level of 2.5 V (typ.).

Burst Mode

In certain telephony applications it is required that DTMF signals being generated are of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms ±1 ms which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register indicating that the transmitter is ready for more data. The timing described above is available when DTMF mode has been selected. However, when CP mode (Call Progress mode) is selected, a secondary burst/pause time is available such that this interval is extended to 102 ms ±2 ms. The extended interval is useful when precise tone bursts of longer than 51 ms duration and 51 ms pause are desired. Note that when CP mode *and* Burst mode have been selected, DTMF tones may be transmitted only and not received. In certain applications where a nonstandard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

The SC11280 is initialized on power-up sequence such that DTMF mode and Burst mode are selected.

Single Tone Generation

A single tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgement tone generation and distortion measurements. Refer to Control Register B description for details.

Distortion Calculations

The SC11280 is capable of producing precise tone bursts with minimal error in frequency (see Table 1). The internal summing amplifier is followed by a first-order low pass switched-capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single tone* can be calculated using Equation 1 which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage. The Fourier components of the tone output correspond to $V_{2f}...V_{nf}$ as measured on the output waveform. The total harmonic distortion for a *dual tone* can be calculated using Equation 2. V_L and V_H correspond to the low group amplitude and high group amplitude, respectively and V^2_{IMD} is the sum of all the interdemodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 7.

$$THD\ (\%) = 100\frac{\left(\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + V^2_{nf}}\right)}{V_{fundamental}}$$

Equation 1. THD (%) For a Single Tone

$$THD\ (\%) = 100\frac{\left(\sqrt{\begin{matrix}V^2_{2L} + V^2_{3L} + \ldots V^2_{NL} \\ + V^2_{2H} + \ldots V^2_{NH} + V^2_{IMD}\end{matrix}}\right)}{\sqrt{V^2_L + V^2_H}}$$

Equation 2. THD (%) For a Dual Tone

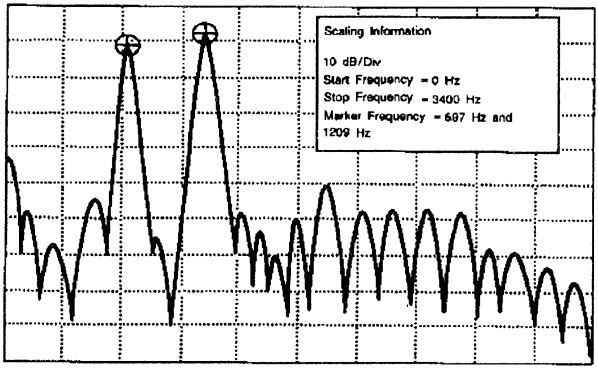


Figure 7. Spectrum Plot

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television color burst crystal having a resonant frequency of 3.579545 MHz. A number of SC11280 devices can be connected as shown in Figure 8 such that only one crystal is required.

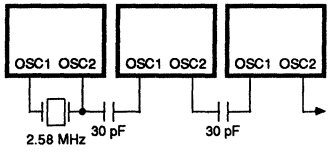


Figure 8. Common Crystal Connection

Microprocessor Interface

The SC11280 employs a microprocessor interface which allows precise control of transmitter and receiver functions. There are five internal registers associated with the microprocessor interface which can be subdivided into three categories, ie; data transfer, transceiver control, and transceiver status.

There are two registers associated with data transfer operations. The Receive Data Register contains the output code of the last valid DTMF tone pair to be decoded and is a read only register. The data entered in the Tranmit Data Register will determine which tone pair is to be generated (see Figure 5 for coding details). Data can only be written to the transmit register. Transceiver control is accomplished with two control registers (CRA and CRB) which occupy the same address space. A write operation to CRB can be executed by setting the appropriate bit in CRA. The following write operation to the same address will then be directed to CRB and subsequent write cycles will then be directed back to CRA. Internal reset circuitry will clear the control registers on power up, however, as a precautionary measure the initialization software should include a routine to clear the registers. Refer to Table 5 and Table 6 for details concerning the Control Registers. The IRQ/CP pin can be programmed such that it will provide an interrupt request signal upon validation of DTMF signals or when the transmitter is ready for more data (Burst mode only). The IRQ/CP pin is configured as an open drain output device and as such requires a pull-up resistor (see Figure 9).

RSO	R/$\overline{W}$	FUNCTION
0	0	Write to Transmitter
0	1	Read from Receiver
1	0	Write to Control Register
1	1	Read from Status Register

Table 2. Internal Register Functions

b3	b2	b1	b0
RSEL	IRQ	CP/$\overline{DTMF}$	TOUT

Table 3. CRA Bit Positions

b3	b2	b1	b0
C/R	S/$\overline{D}$	TEST	BURST

Table 4. CRB Bit Positions

BIT	NAME	FUNCTION	DESCRIPTION
b0	TOUT	TONE OUTPUT	A Logic '1' enables the tone output. This function can be implemented in either the burst mode or non-burst mode.
b1	CP/$\overline{DTMF}$	MODE CONTROL	In DTMF mode (logic '0') the device is capable of generating and receiving Dual Tone Multi-Frequency signals. When the CP (Call Progress) mode is selected (logic '1') a 6th order bandpass filter is enabled to allow call progress tones to be detected.
b2	IRQ	INTERRUPT ENABLE	A logic '1' enables the INTERRUPT mode. When this mode is active and the DTMF mode has been selected (b1 = 0) the IRQ/CP pin will pull to a logic '0' condition when either 1) a valid DTMF signal has been received and has been present for the guard time duration or 2) the transmitter is ready for more data (BURST mode only).
b3	RSEL	REGISTER SELECT	A logic '1' selects Control Register B on the next Write cycle to the Control Register address. Subsequent Write cycles to the Control Register are directed back to Control Register A.

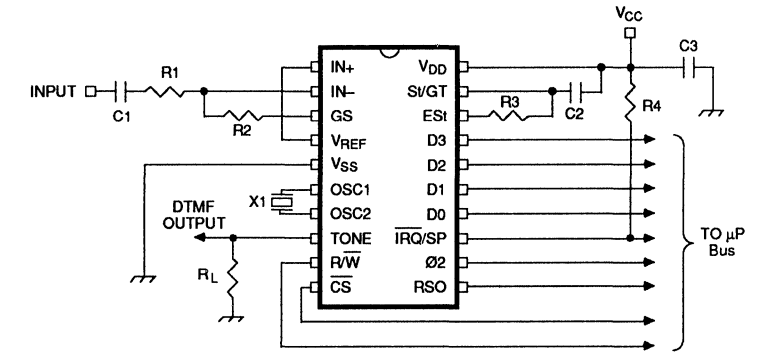
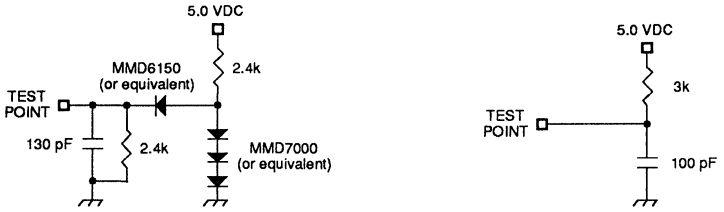


Figure 9. Application Circuit (Single Ended Input)



Test Load for D0–D3 Pins **Test Load for IRQ/CP PIN**

Figure 10. Test Circuits

BIT	NAME	FUNCTION	DESCRIPTION
b0	BURST	BURST MODE	A logic '0' enables the burst mode. When this mode is selected, data corresponding to the desired DTMF tone pair can be written to the Transmit Register resulting in a tone burst of a specific duration (see AC Characteristics). Subsequently, a pause of the same duration is induced. Immediately following the pause, the Status Register is updated indicating that the Transmit Register is ready for further instructions and an interrupt will be generated if the interrupt mode has been enabled. Additionally, if call progress (CP) mode has been enabled, the burst and pause duration is increased by a factor of two. When the burst mode is not selected (logic '1') tone bursts of any desired duration may be generated.
b1	TEST	TEST MODE	By enabling the test mode (logic '1') the IRQ/CP pin will present the delayed steering (inverted) signal from the DTMF receiver. Refer to Figure 7 (b3 waveform) for details concerning the output waveform. DTMF mode must be selected (CRA1 = 0) before test mode can be implemented.
b2	S/$\overline{D}$	SINGLE/DUAL TONE GENERATION	A logic '0' will allow Dual Tone Multi-Frequency signals to be produced. If single tone generation is enabled (logic '1'), either row or column tones (low group or high group) can be generated depending on the state of b3 in Control Register B.
b3	C/$\overline{R}$	COLUMN/ROW TONES	When used in conjunction with b2 (above) the transmitter can be made to generate single row or single column frequencies. A logic '0' will select row frequencies and a logic '1' will select column frequencies.

Table 6. Control Register B Description

BIT	NAME	STATUS FLAG SET	STATUS FLAG CLEARED
b0	IRQ	Interrupt has occurred. Bit one (b1) and/or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	TRANSMIT DATA REGISTER EMPTY (BURST MODE ONLY)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in non-burst mode.
b2	RECEIVE DATA REGISTER FULL	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	$\overline{\text{DELAYED STEERING}}$	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

Table 7. Status Register Description

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Power Supply Voltage, V_{CC}– V_{SS}	+6 V
Voltage on any Pin	V_{SS}–0.3 to V_{CC}+0.3 V
Current at any Pin (Except V_{CC} and V_{SS})	10 mA
Operating Temperature	–40 to +85°C
Storage Temperature	–65 to +150°C
Package Power Dissipation (Note 3)	500 mW

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

OPERATING CHARACTERISTICS

Gain Setting Amplifier (Notes 1 and 2)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_N	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$		±100		nA
R_{IN}	Input Resistance			10		MΩ
V_{OS}	Input Offset Voltage			±25		mV
PSRR	Power Supply Rejection	1 kHz		60		dB
CMRR	Common Mode Rejection	$-3.0\ V \leq V_{IN} \leq 3.0\ V$		60		dB
A_{VOL}	DC Open Loop Voltage Gain			65		dB
f_C	Open Loop Unity Gain Bandwidth			1.5		MHz
V_O	Output Voltage Swing	$R_L \geq 100$ kΩ to V_{SS}		4.5		V_{PP}
C_L	Maximum Capacitive Load (GS)			100		pF
R_L	Maximum Resistive Load (GS)			50		kΩ
V_{CM}	Common Mode Range	No Load		3.0		V_{PP}

Notes: 1. V_{CC} = 5 V, V_{SS}= 0 V, Voltages are with respect to ground (V_{SS}) unless otherwise stated.
2. Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
V_{CC}	Operating Supply Voltage		4.75	5.0	5.25	V
I_{CC}	Operating Supply Current			10		mA
P_O	Power Consumption			50		mW
INPUTS						
V_{IHO}	High Level Input Voltage (OSC1)		3.5			V
V_{ILO}	Low Level Input Voltage (OSC1)				1.5	V
	Input Impedance Inputs 1, 2			10		MΩ
V_{TSt}	Steering Threshold Voltage		2.2		2.5	V
OUTPUTS						
V_{OLO}	Low Level Output Voltage (OSC2)	No Load			0.1	V
V_{OHO}	High Level Output Voltage (OSC2)	No Load	4.9			V
I_{OL}	Output Low (Sink) Current	V_{OUT}=0.4 V		1	10	µA
V_{REF}	V_{REF} Output Voltage	No Load	2.4		2.7	V
R_{OR}	V_{REF} Output Resistance			10		kΩ
DATA BUS						
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			0.4	V
V_{OH}	High Level Output Voltage	I_{OH} = 400 µA	2.4			V
I_{IZ}	Input Leakage Current	V_{IN} = 0.4 to 2.4 V			10	µA

Note: 1. Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC ELECTRICAL CHARACTERISTICS All voltages referenced to V_{SS} unless otherwise stated. V_{CC} = 5.0 V, V_{SS} = 0 V = 1 MHz, F_C = 3.579545 MHz.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS	NOTES
RX SIGNAL CONDITION						
	Valid Input Signal Level (each tone of composite signal)	–29			dBm	1,2,3,5,6,9
		27.5			mV_{RMS}	1,2,3,5,6,9
				+1	dBm	1,2,3,5,6,9
				883	mV_{RMS}	1,2,3,5,6,9
	Positive Twist Accept		10		dB	2,3,6,9
	Negative Twist Accept		10		dB	2,3,6,9
	Freq. Deviation Accept Limit	±1.5% ±2 Hz			Nom.	2,3,5,9
	Freq. Deviation Reject Limit	±3.5%			Nom.	2,3,5
	Third Tone Tolerance		–16		dB	2,3,4,5,9,10
	Noise Tolerance		–12		dB	2,3,4,5,7,9,10
	Dial Tone Tolerance		+22		dB	2,3,4,5,8,9,11
CALL PROGRESS						
f_{LA}	Lower Frequency (ACCEPT)		320		Hz	@ –25 dBm
f_{HA}	Upper Frequency (ACCEPT)		510		Hz	@ –25 dBm
f_{LR}	Lower Frequency (REJECT)		290		Hz	@ –25 dBm
f_{HR}	Upper Frequency (REJECT)		540		Hz	@ –25 dBm

Notes:
1. dBm = decibels above or below a reference power of 1 mW into a 600 Ω load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms. Tone pause = 40 ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ±2 Hz.
7. Bandwidth limited (3 kHz) Gaussian Noise.
8. The precise dial tone frequencies are 350 Hz and 440 Hz ±2%.
9. For an error rate of less than 1 in 10,000.
10. Referenced to the lowest amplitude tone in the DTMF signal.
11. Referenced to the minimum valid accept level.

AC ELECTRICAL CHARACTERISTICS (Notes 1 and 2)

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
RX TIMING						
t_{DP}	Tone Present Detect Time		5	12	16	ms
t_{DA}	Tone Absent Detect Time		0.5	4	8.5	ms
t_{REC}	Tone Duration Accept				40	ms
$t_{\overline{REC}}$	Tone Duration Reject	See Figure 9	20			ms
t_{ID}	Interdigit Pause Accept	See Figure 9			40	ms
t_{DO}	Interdigit Pause Reject	See Figure 9	20			ms
t_{PStb3}	Delay St to b3			13		µs
t_{PStRX}	Delay St to RX_0–RX_3			8		µs
TX TIMING						
t_{BST}	Tone Burst Duration	DTMF Mode	50		52	ms
t_{PS}	Tone Pause Duration	DTMF Mode	50		52	ms
$t_{BST}E$	Tone Burst Duration (Extended)	Call Progress Mode	100		104	ms
$t_{PS}E$	Tone Pause Duration (Extended)	Call Progress Mode	100		104	ms
TONE OUT						
V_{HOUT}	High Group Output Level	R_L = 10 kΩ	–8	–5		dBm
V_{LOUT}	Low Group Output Level	R_L = 10kΩ	–10	–5		dBm
dBp	Pre-emphasis	R_L = 10kΩ	0	2	3	dB
THD	Output Distortion	3.4 kHz Bandwidth R_L = 10 kΩ		–25		dB
f_D	Frequency Deviation	f = 3.5795 MHz		±0.7%	±1.5%	
$R_L T$	Output Load Resistance		10		50	kΩ
MPU INTERFACE						
t_{CYC}	ø2 Cycle Period			1		µs
t_{CH}	ø2 High Pulse Width		450			ns
t_{CL}	ø2 Low Pulse Width		430			ns
t_R, t_F	ø2 Rise and Fall Time				25	ns
t_{AH}	Address Hold Time		10			ns
t_{AS}	Address Set-Up Time (Before ø2)		80			ns
t_{DHR}	Data Hold Time (Read)		20		100	ns
t_{DDR}	ø2 to Valid Data Delay (Read)				290	ns
t_{DSW}	Data Set-Up Time (Write)		165			ns
t_{DHW}	Data Hold Time (Write)		10			ns
C_{IN}	Input Capacitance (Data Bus)			5		pF
C_{OUT}	Output Capacitance (IRQ/CP)			5		pF

AC ELECTRICAL CHARACTERISTICS (Cont.)

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
DTMF CLK						
f_C	Crystal/Clock Frequency		3.5759	3.5795	3.5831	MHz
t_{LHCL}	Clock Input Rise Time	Ext. Clock			110	ns
t_{HLCL}	Clock Input Fall Time	Ext. Clock			110	ns
DC_{CL}	Clock Input Duty Cycle	Ext. Clock	40	50	60	%
C_{LO}	Capacitive Load (OSC2)				30	pF

Notes: 1. Timing is over recommended temperature & Power Supply voltages. f_C = 3.579545 MHz.
2. Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

TIMING DIAGRAMS

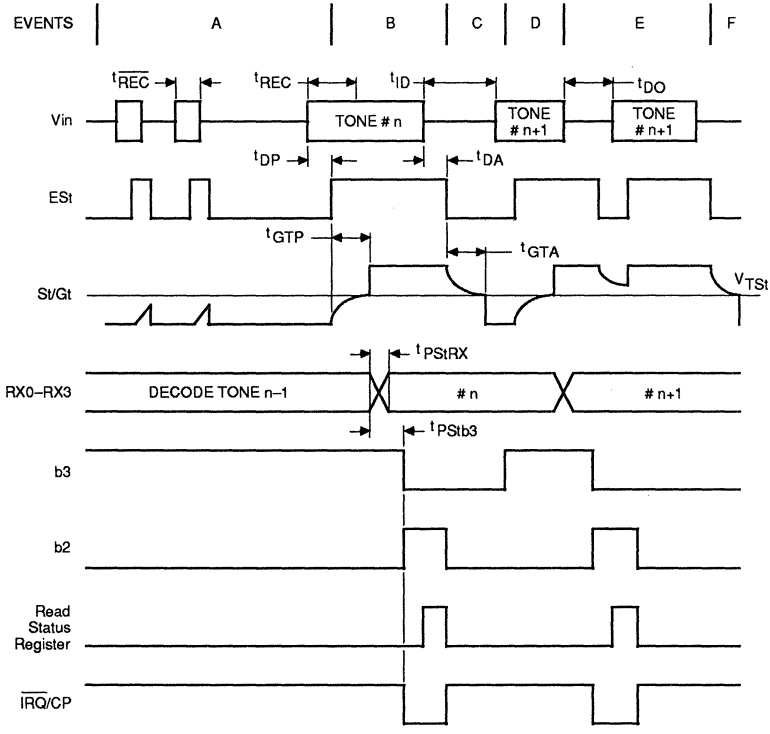


Figure 11. Timing Diagram

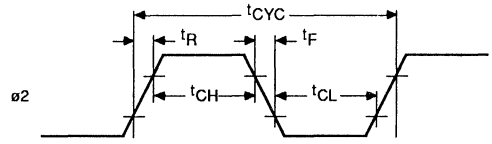


Figure 12. ø2 Pulse

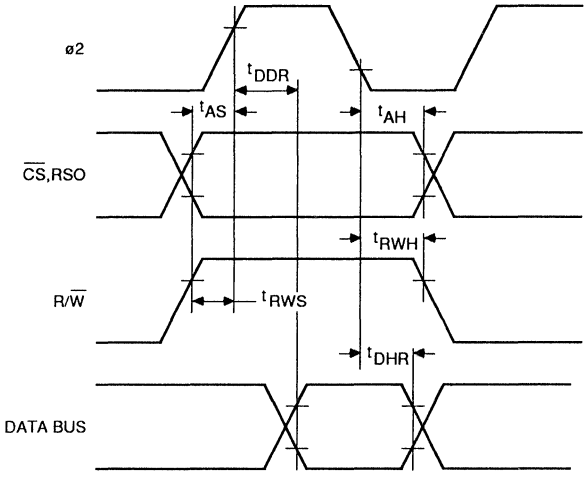


Figure 13. MPU Read Cycle

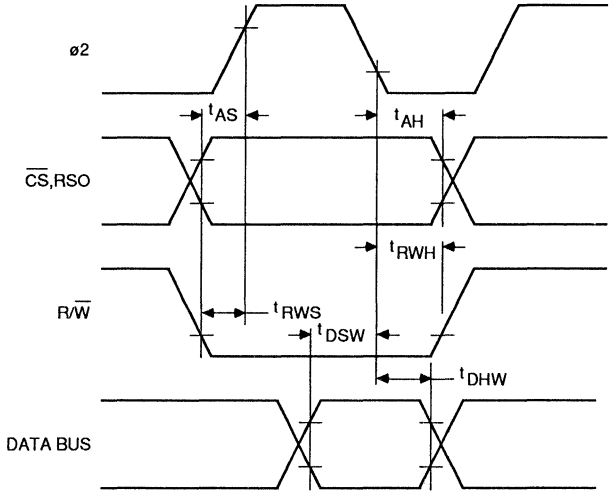


Figure 14. MPU Write Cycle

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FEATURES

- ☐ DTMF Generator and Receiver on one chip
- ☐ CMOS single 5 Volt operation
- ☐ Uses inexpensive 3.579545MHz crystal

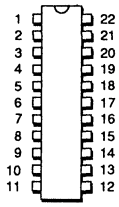
GENERAL DESCRIPTION

The SC11289 is a complete Dual Tone Multiple Frequency (DTMF) Transceiver that can both generate and detect all 16 standard Touch-Tone digits. The SC11289 circuit integrates the performance of the SC11202 DTMF Receiver with a DTMF generator circuit.

The DTMF receiver electrical characteristics are identical to the SC11202 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved output amplitude range specification and with the addition of independent latch and reset controls.

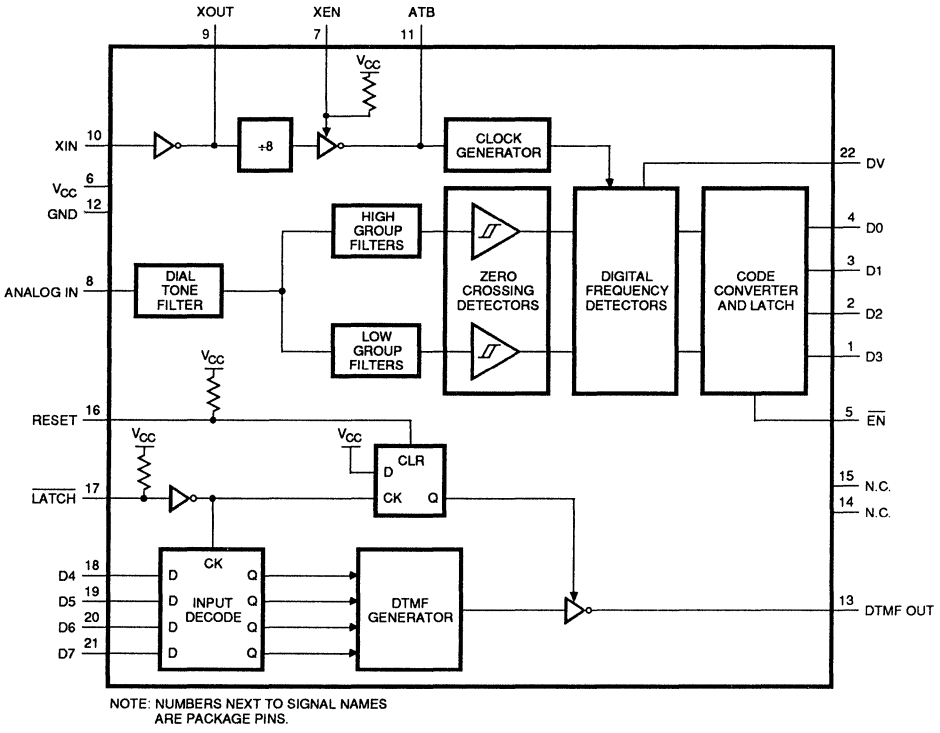
The only external components necessary for the SC11289 are a single 3.58 MHz crystal with a parallel 1 MΩ resistor. This provides the time base for digital functions and switched capacitor filters in the device. No external filtering is required.

22-PIN DIP PACKAGE



SC11289CN

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE PACKAGE PINS.

CIRCUIT OPERATION

Receiver

The DTMF receiver in the SC11289 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60 Hz reject and band splitting filters, then hard-limited to provide Automatic Gain Control. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

Analog In

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

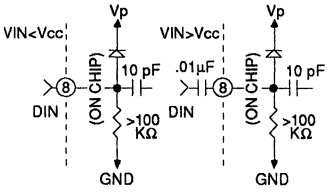


Figure 1.

The SC11289 is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than 20 dB below the fundamental.

Crystal Oscillator

The SC11289 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television 3.58 MHz crystal. The crystal is placed between XIN and XOUT in parallel with a 1 MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the SC11289 depends on the time base tolerance. The DTMF receiver frequency response and timing is specified for a time base accuracy of at least ± 0.005%. ATB is a clock frequency output. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected SC11289 as shown in Figure 2.

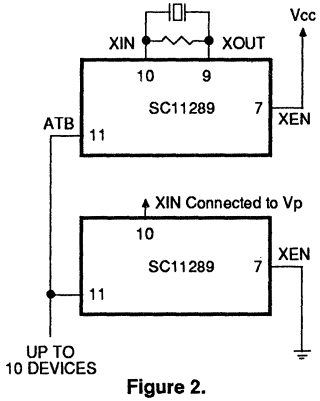


Figure 2.

Receiver Outputs and the $\overline{EN}$ Pin

Outputs D0, D1, D2, D3 are CMOS push-pull when enabled ($\overline{EN}$ low) and open-circuited (high impedance) when disabled ($\overline{EN}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. Table 1 shows that code.

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

Generator

The DTMF generator on the SC11289 responds to a hexadecimal code input with a valid tone pair. Pins D4–D7 are the data inputs for the generator. A high to low transition on $\overline{LATCH}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

Digital Inputs

The D4, D5, D6, D7, $\overline{LATCH}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Table 1 shows the code for each digit. Figure 3 shows the dialing matrix and detection frequency table.

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0 V. However, the output level is directly proportional to the supply, so variations in it will affect the

Table 1.

		Hexadecimal code			
	Input:	D7	D6	D5	D4
Digit	Output:	D3	D2	D1	D0
1		0	0	0	1
2		0	0	1	0
3		0	0	1	1
4		0	1	0	0
5		0	1	0	1
6		0	1	1	0
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
0		0	1	1	0
*		1	0	1	1
#		1	1	0	0
A		1	1	0	1
B		1	1	1	0
C		1	1	1	1
D		0	0	0	0

DTMF Dialing Matrix

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

Note: Column 3 is for special applications and is not normally used in telephone dialing.

Detection Frequency

Low Group fo	High Group fo
Row 0=697 Hz	Column 0=1209 Hz
Row 1=700 Hz	Column 1=1336 Hz
Row 2=852 Hz	Column 2=1477 Hz
Row 3=941 Hz	Column 3=1633 Hz

Figure 3.

DTMF output. A recommended line interface for this output is show in Figure 4.

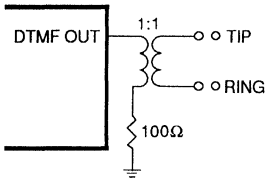


Figure 4.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage (Vp–Vn)	+7 V
Voltage at any Pin (Vn=0)	–0.3 to Vcc+0.3 V
Analog Voltage	Vcc+0.5 to Vcc–10 V
Current through any protection device	±1.0 mA
Storage Temperature	–40°C to +150°C

*Operation above absolute maximum ratings may damage the device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	MAX.	UNIT
Supply voltage	4.5	5.5	V
Power supply noise (wide band)	—	10	mVcc
Ambient temperature	0	+70	°C
Crystal Frequency (F Nominal = 3.579545 MHz)	–0.005	+0.005	%
Crystal shunt resistor	0.8	1.2	MΩ
DTMF OUT load resistance	100	—	Ω

DIGITAL AND DC REQUIREMENTS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: ANALOG IN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. GND=0 unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
Supply current*	—	—	30	mA
Power dissipation	—	—	225	mW
Input voltage high	—	0.7 Vcc	—	V
Input voltage low	—	—	0.3 Vcc	V
Input current high	—	—	10	µA
Input current low	—	–10	—	µA
Output voltage high	Ioh = –0.2 mA	Vcc–0.5	—	V
Output voltage low	Iol = +0.4 mA	—	GND+0.5	V

*With DTMF output disabled

DTMF RECEIVER

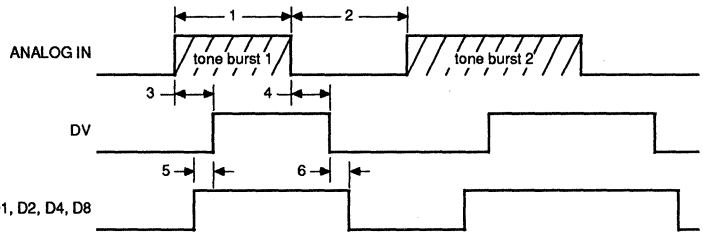
Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN.	Typ.	MAX.	UNIT
Frequency detect bandwidth	—	±(1.5+2 Hz)	±2.3	±3.5	%Fo
Amplitude for detection	Each tone	-32	—	-2	dBm/tone
Twist tolerance	—	-10	—	+10	dB
60 Hz tolerance	—	—	—	0.8	Vrms
Dial tone tolerance	Precise dial tone	—	—	0	dB*
Speech immunity	MITEL Tape #CM7290	—	2	—	hits
Noise tolerance	MITEL Tape #CM7290	—	—	-12	dB*
Input impedance	—	100	—	—	KΩ

* Referenced to lowest amplitude tone.

Timing Characteristics

NO.	SYMBOL	PARAMETER	MIN.	MAX.	UNIT
1	ton	Tone time for detect	40	—	ms
1	ton	Tone time for no detect	—	20	ms
2	toff	Pause time for redetection	40	—	ms
2	toff	Pause time for bridging	—	20	ms
3	td1	Detect time	25	46	ms
4	tr1	Release time	35	50	ms
5	tsu1	Data set up time	7	—	µs
6	thd1	Data hold time	4.2	5.0	ms
	—	Output enable time	—	200	ns
	—	Output disable time	—	200	ns



DTMF Decoder

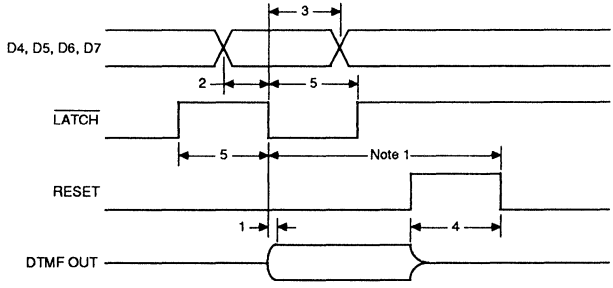
DTMF GENERATOR

Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
Frequency accuracy	—	–1.0	+1.0	%Fo
Output amplitude	R1 = 100 Ω to Vn, Vcc–GND = 5.0 V	—	—	—
Low Band	—	–9.2	–7.2	dBm
High Band	—	–6.6	–4.6	dBm
Output distortion	DC to 50 KHz	—	–20	dB

Timing Characteristics

NO.	SYMBOL	PARAMETER	MIN.	MAX.	UNIT
1	tstart	Start-up time	—	4.5	µs
2	tsu2	Data set-up time	400	—	ns
3	thd2	Data hold time	30	—	ns
4	trp	RESET pulse width	450	—	ns
5	tpw	$\overline{\text{LATCH}}$ pulse width	450	—	ns



DTMF Generator

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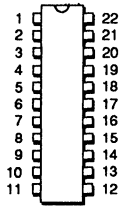
FEATURES

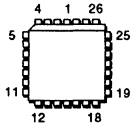
- ☐ DTMF generator and receiver
- ☐ Excellent speech immunity
- ☐ Tri-State outputs (4-bit hexadecimal) from receiver
- ☐ AC-Coupled, internally-biased analog input
- ☐ Analog input –32 to –2 dBm
- ☐ DTMF output –8 dBm (low band) and –5.5 dBm (high band)
- ☐ Microprocessor dialing
- ☐ Call progress detection

22-PIN DIP PACKAGE



SC11290CN

28-PIN PLCC PACKAGE



SC11290CV

GENERAL DESCRIPTION

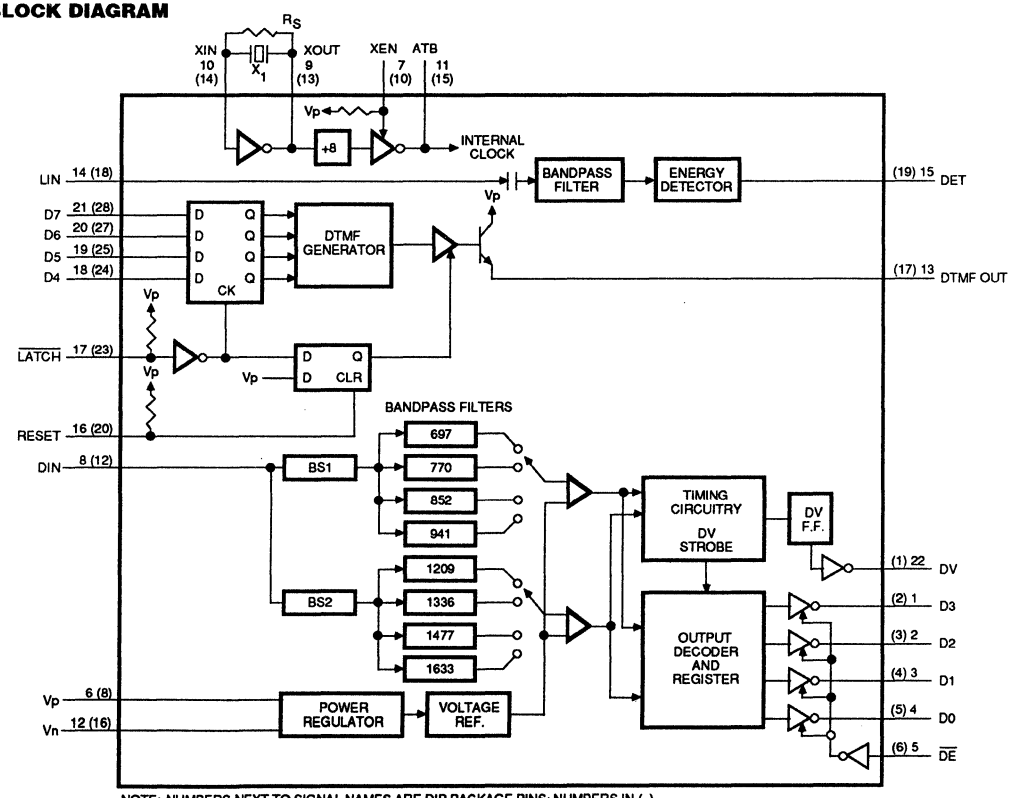
Sierra Semiconductor's new SC11290 is a complete Dual Tone Multiple Frequency (DTMF) Transceiver that can both generate and detect all 16 standard Touch-Tone digits. The SC11290 circuit integrates the performance proven SC11202 DTMF Receiver with a new DTMF generator circuit.

The DTMF Receiver electrical characteristics are identical to the standard SC11202 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved (tighter) output amplitude range specification and with the addition of independent latch and reset controls.

An additional feature of the SC11290 is "imprecise" call progress detector. The detector detects the presence of signals in the 305–640 Hz band.

The only external components necessary for the SC11290 are a 3.58 MHz "colorburst" crystal with a parallel 1M Ω resistor. This provides the time base for digital functions and switched capacitor filters in the device. No external filtering is required.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINS; NUMBERS IN ( ) ARE PLCC PINS. PINS (7), (9), (11), (21), (22), & (26) ARE NOT CONNECTED.

CIRCUIT OPERATION

Receiver

The DTMF receiver in the SC11290 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60 Hz reject and band splitting filters, then hard-limited to provide automatic gain control. Eight bandpass filters detect the individual tones. The digital post processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

DIN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

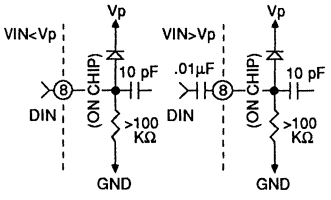


Figure 1.

The SC11290 is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than 20 dB below the fundamental.

Crystal Oscillator

The SC11290 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal is placed between XIN and XOUT in parallel with a 1M Ω resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the SC11290 depends on the time base tolerance. The Sierra Semiconductor DTMF receiver frequency response and timing is specified for a time base accuracy of at least ± 0.005%. ATB is a clock frequency output. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected SC11290 as shown in Figure 2.

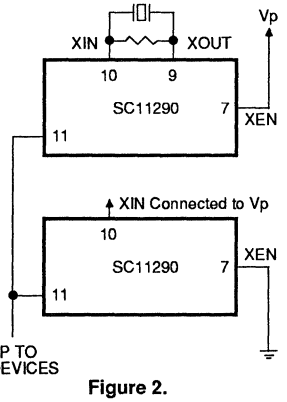


Figure 2.

Receiver Outputs and the $\overline{DE}$ Pin

Outputs D0, D1, D2, D3 are CMOS push-pull when enabled ($\overline{DE}$ low) and open-circuited (high impedance) when disabled ($\overline{DE}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. Table 1 shows that code.

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

Generator

The DTMF generator on the SC11290 responds to a hexadecimal code input with a valid tone pair. Pins D4–D7 are the data inputs for the generator. A high to low transition on $\overline{LATCH}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

Digital Inputs

The D4, D5, D6, D7, $\overline{LATCH}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Table 1 shows the code for each digit. Figure 3 shows the dialing matrix and detection frequency table.

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0 V. However, the output level is directly proportional to the supply, so variations in it will affect the

Table 1.

		Hexadecimal code			
	Input:	D7	D6	D5	D4
Digit	Output:	D3	D2	D1	D0
1		0	0	0	1
2		0	0	1	0
3		0	0	1	1
4		0	1	0	0
5		0	1	0	1
6		0	1	1	0
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
0		1	0	1	0
*		1	0	1	1
#		1	1	0	0
A		1	1	0	1
B		1	1	1	0
C		1	1	1	1
D		0	0	0	0

DTMF Dialing Matrix

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

Note: Column 3 is for special applications and is not normally used in telephone dialing.

Detection Frequency

Low Group fo	High Group fo
Row 0=697 Hz	Column 0=1209 Hz
Row 1=700 Hz	Column 1=1336 Hz
Row 2=852 Hz	Column 2=1477 Hz
Row 3=941 Hz	Column 3=1633 Hz

Figure 3.

DTMF output. A recommended line interface for this output is show in Figure 4.

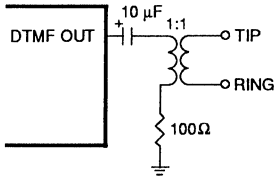


Figure 4.

Call Progress Detection

The call progress detector consists of a bandpass filter and an energy detector for turning the on/off cadences into a microprocessor compatible signal.

LIN Input

This analog input accepts the call progress signal and should be used in the same manner as the receiver input DIN.

DET Output

This output is TTL compatible and will be of a frequency corresponding to the various cadences of call progress signals such as, on 0.5 sec/off 0.5 sec for a busy tone, on 0.25 sec/off 0.25 sec for a reorder tone and on 0.8–1.2 sec/off 2.7–3.3 sec for an audible ring tone.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage (Vp–Vn)	+7 V
Voltage at any Pin (Vn=0)	–0.3 to Vp+0.3 V
DIN Voltage	Vp+0.5 to Vp–10 V
Current through any protection device	±20 mA
Operating Temp. Range	–40°C to +85°C
Storage Temperature	–65°C to 150°C

* Operation above absolute maximum ratings may damage the device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	MAX.	UNIT
Supply voltage	4.5	5.5	V
Power supply noise (wide band)	—	10	mV pp
Ambient temperature	–40	+85	°C
Crystal Frequency (F Nominal = 3.579545 MHz)	–0.01	+0.01	%
Crystal shunt resistor	0.8	1.2	MΩ
DTMF OUT load resistance	100	—	Ω

DIGITAL AND DC REQUIREMENTS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: LIN, DIN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. Vn=0 unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
Supply current*	—	—	30	mA
Power dissipation	—	—	225	mW
Input voltage high	—	0.7 Vp	—	V
Input voltage low	—	—	0.3 Vp	V
Input current high	—	—	10	µA
Input current low	—	–10	—	µA
Output voltage high	Ioh = –0.2 mA	Vp–0.5	—	V
Output voltage low	Iol = +0.4 mA	—	Vn+0.5	V

*With DTMF output disabled

DTMF RECEIVER

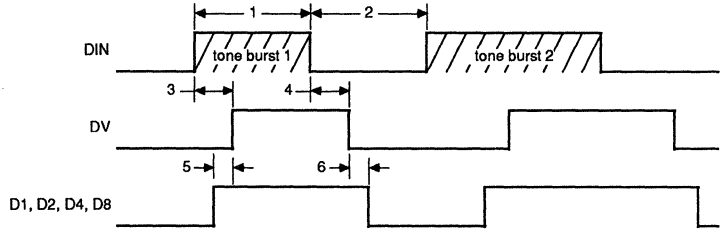
Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN.	Typ.	MAX.	UNIT
Frequency detect bandwidth	—	±(1.5+2 Hz)	±2.3	±3.5	%Fo
Amplitude for detection	—	-32	—	-2	dBm/tone
Twist tolerance	—	-10	—	+10	dB
60 Hz tolerance	—	—	—	0.8	Vrms
Dial tone tolerance	Precise dial tone	—	—	0	dB*
Speech immunity	MITEL Tape #CM7290	—	2	—	hits
Noise tolerance	MITEL Tape #CM7290	—	—	-12	dB*
Input impedance	—	100	—	—	KΩ

* Referenced to lowest amplitude tone.

Timing Characteristics

NO.	SYMBOL	PARAMETER	MIN.	MAX.	UNIT
1	ton	Tone time for detect	40	—	ms
1	ton	Tone time for no detect	—	20	ms
2	toff	Pause time for redetection	40	—	ms
2	toff	Pause time for bridging	—	20	ms
3	td1	Detect time	25	46	ms
4	tr1	Release time	35	50	ms
5	tsu1	Data set up time	7	—	µs
6	thd1	Data hold time	4.2	5.0	ms
	—	Output enable time	—	200	ns
	—	Output disable time	—	200	ns



DTMF GENERATOR

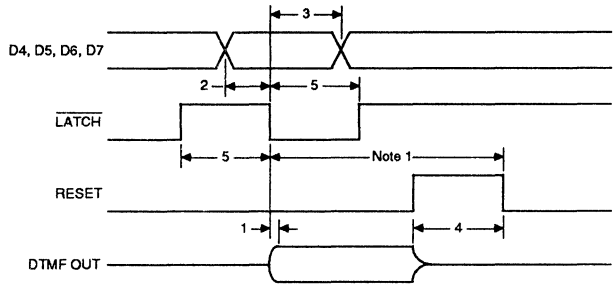
Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
Frequency accuracy	—	-1.0	+1.0	%Fo
Output amplitude	R1 = 100Ω to Vn, Vp–Vn = 5.0 V	—	—	—
Low Band	—	-9.2	-7.2	dBm
High Band	—	-6.6	-4.6	dBm
Output distortion	DC to 50 KHz	—	-20	dB

DTMF GENERATOR (Cont.)

Timing Characteristics

NO.	SYMBOL	PARAMETER	MIN.	MAX.	UNIT
1	tstart	Start-up time	—	2.5	µs
2	tsu2	Data set-up time	100	—	ns
3	thd2	Data hold time	50	—	ns
4	trp	RESET pulse width	100	—	ns
5	tpw	$\overline{\text{LATCH}}$ pulse width	100	—	ns



Note 1: The indicated time may be as small as 0 sec meaning that the $\overline{\text{LATCH}}$ and RESET lines may be tied together

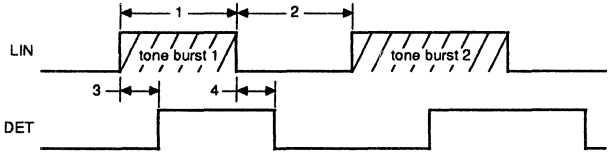
CALL PROGRESS DETECTOR

Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
Amplitude for detection	305 Hz—640 Hz	–40	0	dBm
Amplitude for no detection	305 Hz—640 Hz	—	–50	dBm
	160 Hz > f > 2200 Hz	—	–25	dBm
Detect output	Logic 0	—	.5	V
	Logic 1	4.5	—	V
"LIN" input	Max voltage	V_{DD}–10	V_{DD}	V
Input impedence	500 Hz	100	—	KΩ

Timing Characteristics

NO.	SYMBOL	PARAMETER	MIN.	MAX.	UNIT
1	ton	Signal time for detect	40	—	ms
1	ton	Signal time for no detect	—	10	ms
2	toff	Interval time for detect	40	—	ms
2	toff	Interval time for no detect	—	20	ms
3	td2	Detect time	—	40	ms
4	tr2	Release time	—	40	ms



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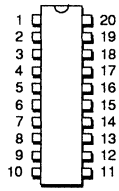
FEATURES

- ☐ Complete CODEC and Filtering System
- ☐ Meets or Exceeds All D3/D4 and CCITT Specifications
- ☐ Low Operating Power —Typically 60 mW
- ☐ ±5 V Operation
- ☐ Power-Down Standby Mode—Typically 3 mW
- ☐ High Speed TRI-STATE® Data Bus
- ☐ 2 Loopback Test Modes

20-PIN DIP PACKAGE



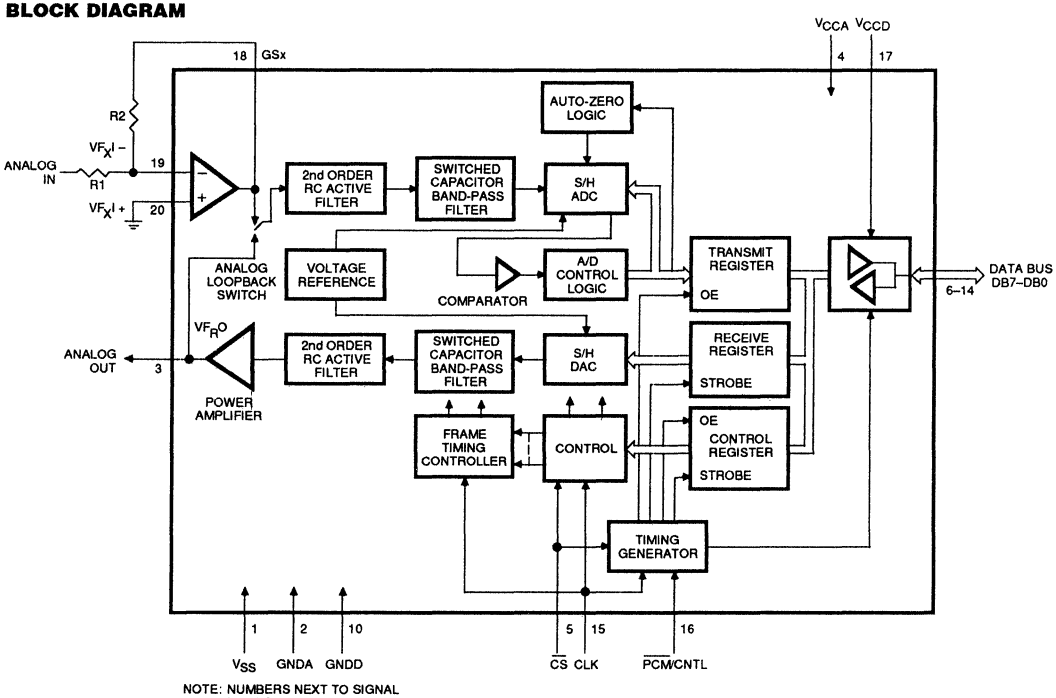
SC11305CN
SC11306CN

GENERAL DESCRIPTION

The SC11305/SC11306 family consists of a μ-law and A-law monolithic PCM CODEC/filter set utilizing the A/D and D/A conversion architecture shown in Figure 1, and a parallel I/O data bus interface. The devices are fabricated using Sierra's proprietary Double-poly CMOS process technology.

The transmit section consists of an input gain adjust amplifier, an active RC pre-filter, and a switched-capacitor bandpass filter that rejects signals below 200 Hz and above 3400 Hz. A compressing coder samples the filtered signal and encodes it in the μ-255 law or A-law PCM format. Auto-zero circuitry is included on-chip. The receive section consists of an expanding decoder which reconstructs the analog signal from the compressed μ-law or A-law code, and a low pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz. The receive output is a signal-ended power amplifier capable of driving low impedance loads. The SC11305 μ-law and SC11306 A-law devices are pin compatible parallel interface CODEC/filters for bus-oriented systems.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINS.

PIN DESCRIPTION

Pin #	Name	Function
1	V_{SS}	Negative power supply pin. V_{SS} = -5V ±5%
2	GNDA	Analog ground. All analog signals are referenced to this pin
3	VF_RO	Analog output of the receive power amplifier. This output can drive a 600 Ω load to ±2.5 V.
4	V_{CCA}	Positive power supply voltage pin for the analog circuitry. V_{CCA} = 5 V ±5%. Must be connected to V_{CCD}.
5	$\overline{CS}$	Device chip select input which controls READ, WRITE and TRI-STATE operations on the data bus. $\overline{CS}$ does not control the state of any analog functions.
6	DB7	Bit 7 I/O on the data bus. The PCM LSB.
7	DB6	Bit 6 I/O on the data bus.
8	DB5	Bit 5 I/O on the data bus.
9	DB4	Bit 4 I/O on the data bus.
10	GNDD	Digital ground. All digital signals are referenced to this pin.
11	DB3	Bit 3 I/O on the data bus.
12	DB2	Bit 2 I/O on the data bus.
13	DB1	Bit 1 I/O on the data bus.
14	DB0	Bit 0 I/O on the data bus. This is the PCM sign bit.
15	CLK	The clock input for the switched-capacitor filters and CODEC. Clock frequency must be 768 kHz, 772 kHz, 1.024 MHz or 1.28 MHz and must be synchronous with the system clock input.
16	$\overline{PCM}$/ CNTL	This control input determines whether the information on the data bus is PCM data or control data.
17	V_{CCD}	Positive power supply pin for the bus drivers. V_{CCD} = 5 V ±5%. Must be connected to V_{CCA}.
18	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
19	VF_XI^-	Inverting input of the transmit input amplifier.
20	VF_XI^+	Non-inverting input of the transmit input amplifier.

Clock and Data Bus Control

The CLK input signal provides timing for the encode and decode logic and the switched-capacitor filters. It must be one of the frequencies listed in Table 1 and must be correctly selected by control bits C0 and C1.

CLK also functions as a READ/ $\overline{WRITE}$ control signal, with the device reading the data bus on a positive half-clock cycle and writing the bus on a negative half-clock cycle, as shown in Figure 4.

FUNCTIONAL DESCRIPTION

Power-Up

When power is first applied, power-on reset circuitry initializes the CODEC/filter and sets it in the power-down mode. All non-essential circuits are deactivated and the data bus outputs, DB0–DB7, and receive power amplifier output, VF_RO, are high impedance states.

The SC11305/SC11306 is powered-up via a command to the control register (see Control Register Functions). This sets the device in the standby mode with all circuitry activated, but encoding and decoding do not begin until PCM READ and PCM WRITE chip selects occur.

Data Bus Nomenclature

The normal order for serial PCM transmission is sign bit first, whereas the normal order for serial data is LSB first.

Reading the Bus

If CLK is low when $\overline{CS}$ goes low, bus data is gated in during the next positive half-clock cycle of CLK and latched on the negative-going transition. If $\overline{PCM}$/CNTL is low during the falling $\overline{CS}$ transition, then the bus data is defined as PCM voice

Control Bits	Functions
C0, C1	Select Clock Frequency C0 C1 Frequency 0 X 1.024 MHz 1 0 0.768 MHz or 0.772 MHz 1 1 1.28 MHz
C2,C3	Digital and Analog Loopback C2 C3 Mode 1 X Digital loopback 0 1 Analog loopback 0 0 Normal
C4	Power-Down/Power-Up 1 = Power-down 0 = Power-up
C5	SC11305—Don't care SC11306 1 = A-law without even bit inversion 0 = A-law with even bit inversion
C6–C7	Don't Care

Table 1. Control Bit Functions

data, which is latched into the receive register. This also functions as an internal receive frame synchronization pulse to start a decode cycle and must occur once per receive frame; i.e., at an 8 KHz rate.

If $\overline{PCM}$/CNTL is high during the falling $\overline{CS}$ transition, the bus data is latched into the control register. This does not affect frame synchronization.

Writing the Bus

If CLK is high when $\overline{CS}$ goes low, at next falling transition of CLK, the bus drivers are enabled and either the PCM transmit data or the contents of the control register are gated onto the bus, depending on the level of $\overline{PCM}$/CNTL at the $\overline{CS}$ transition. If $\overline{PCM}$/CNTL is low during the $\overline{CS}$ falling transition, the transmit register data is written to the bus. An internal transmit frame synchronization pulse is also generated to start an encode cycle, and this must occur once per transmit frame; i.e., at an 8 KHz rate.

If $\overline{PCM}$/CNTL is high during the $\overline{CS}$ falling transition, the control register data is written to the bus. This does not affect frame synchronization.

The receive register contents may also be written back to the bus, as described in the Digital Loopback section.

Except during a WRITE cycle, the bus drivers are in TRI-STATE mode.

Control Register Functions

Writing to the control register allows the user to set the various operating states of the SC11305 and SC11306. The control register can also be read back via the data bus to verify the current operating mode of the device.

1. **CLK Select.**
   Since one of three distinct clock frequencies may be used, the actual frequency must be known by the device for proper operation of the switched-capacitor filters. This is achieved by writing control register bits C0 and C1, normally in the same WRITE cycle that powers-up the device, and before any PCM data transfers take place.

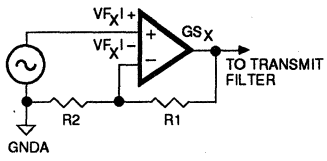
2. **Digital Loopback.**
   In order to establish that a valid path has been selected through a network, it is sometimes desirable to be able to send data through the network to its destination, then loop it back through the network return path to the originating source where the data can be verified. This loopback function can be performed in the SC11305/SC11306 by setting control register bit C2 to 1. With C2 set, the PCM data in the receive register will be written back onto the data bus during the next PCM WRITE cycle. In the digital loopback mode, the receive section is set to an idle channel condition in order to maintain a low impedance termination of VF_RO.

3. **Analog Loopback.**
   In the analog loopback mode, the transmit filter input is switched from the gain adjust amplifier to the receive power amplifier output, forming a unity-gain loop from the receive register back to the transmit register. This mode is entered by setting control register bits C2 to 0 and C3 to 1. The receive power amplifier continues to drive the load in this mode.

4. **Power-Down/Power-Up.**
   The SC11305/SC11306 may be put in the power-down mode by setting control register bit C4 to 1. Conversely, setting bit C4 to 0 powers-up the device.

Transmit Filter and Encode Section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see Figure 2. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of a 2nd order RC active pre-filter, followed by an 8th order switched-capacitor bandpass



Non-inverting transmit gain = $20 \log_{10} \left(\frac{R1 + R2}{R2} \right)$

Set gain to provide peak overload level = t_{MAX} at GS_X
(see Transmission Characteristics)

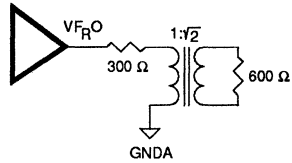
Figure 2. Transmit Gain Adjustment

filter clocked at 256 KHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-255 law (SC11305) or A-law (SC11306) coding schemes. A precision voltage reference is trimmed in manufacturing to provide an input overload (V_{MAX}) of nominally 2.5 V peak (see table of Transmission Characteristics). Any offset voltage due to the filters or comparator is cancelled by sign bit integration in the auto-zero circuit.

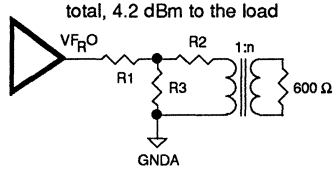
The total encoding delay referenced to a PCM WRITE chip select will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs.

Decoder and Receive Filter Section

The receive section consists of an expanding DAC which drives a 5th order switched-capacitor low pass filter clocked at 256 KHz. The decoder is of A-law (SC11306) or μ-law (SC11305) coding law and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 KHz sample/hold. The filter is then followed by a 2nd order RC active post-filter. The power amplifier output stage is capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section has unity-gain. Following a PCM READ chip select, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (1/2 frame), which gives approximately 180 μs.



Maximum output power = 7.2 dBm total, 4.2 dBm to the load



See Applications Information for attenuator design guide

Figure 3. Receive Gain Adjustment

ABSOLUTE MAXIMUM RATINGS

GNDD to GNDA	±0.3 V
V_{CCA} or V_{CCD} to GNDD or GNDA	7 V
V_{SS} to GNDD or GNDA	–7 V
Voltage at Any Analog Input or Output	V_{CC}+0.3 V to V_{SS}–0.3 V
Voltage at Any Digital Input or Output	V_{CC}+0.3 V to GNDD–0.3 V
Operating Temperature Range	–25°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: $V_{CCA} = V_{CCD} = 5.0$ V ±5%, $V_{SS} = -5$ V ±5%, GNDD = GNDA = 0 V, T_A = 0°C to 70°C; typical characteristics specified at nominal supply voltages, T_A = 25°C; all digital signals are referenced to GNDD, all analog signals are referenced to GNDA.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Digital Interface						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	DB0–DB7, I_L = 2.5 mA			0.4	V
V_{OH}	Output High Voltage	DB0–DB7, I_H = –2.5 mA	2.4			V
I_{IL}	Input Low Current	GNDD ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	–10		10	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	–10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	DB0–DB7, GNDD ≤ V_O ≤ V_{CC}	–10		10	μA

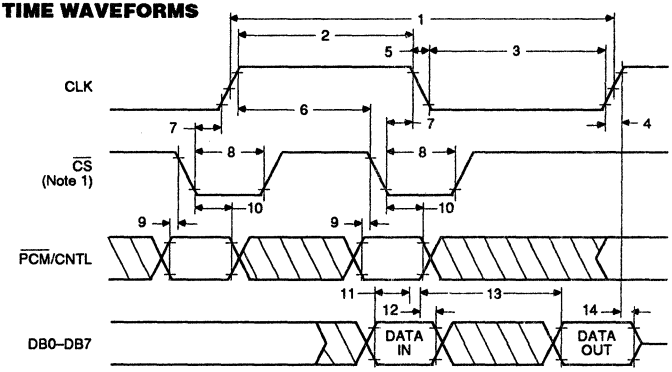
ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Analog Interface with Transmit Input Amplifier (All Devices)						
I_IXA	Input Leakage Current	–2.5 V≤V≤+2.5 V, VF_XI^+ or VF_XI^-	–200		200	nA
R_IXA	Input Resistance	–2.5 V≤V≤+2.5 V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance, GS_X	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance, GS_X		10			kΩ
C_LXA	Load Capacitance, GS_X				50	pF
V_OXA	Output Dynamic Range, GS_X	R_L = 10 kΩ	±2.8			V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	5000			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		–20		20	mV
$V_{CM}XA$	Common-Mode Voltage		–2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB
Receiver Power Amplifier (All Devices)						
R_ORF	Output Resistance, VF_RO			1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5 V	600			Ω
C_LRF	Load Capacitance				50	pF
VOS_RO	Output DC Offset Voltage		–200		200	mV
Power Dissipation (All Devices)						
I_{CCO}	Power-Down Current			0.5	1.5	mA
I_{SSO}	Power-Down Current			0.05	0.3	mA
I_{CC1}	Active Current			6.0	9.0	mA
I_{SS1}	Active Current			6.0	9.0	mA

TIMING SPECIFICATIONS

No.	Symbol	Parameter	Test Conditions	Min	Max	Units
1	t_{PC}	Period of Clock		760		ns
2	t_{WCH}	Width of Clock High		330		ns
3	t_{WCL}	Width of Clock Low		330		ns
4	t_{RC}	Rise Time of Clock			50	ns
5	t_{FC}	Fall Time of Clock			50	ns
6	t_{SCS}	Set-up Time of CLK High or Low		100		ns
7	t_{HCS}	Hold Time from $\overline{CS}$ Low to CLK		100		ns
8	t_{WCS}	Width of Chip Select		100		ns
9	t_{SPCM}	Set-up Time of $\overline{PCM}$/CNTL		0		ns
10	t_{HPCM}	Hold Time of $\overline{PCM}$/CNTL		100		ns
11	t_{SDI}	Set-up Time of Data In		50		ns
12	t_{HDI}	Hold Time of Data In		20		ns
13	t_{DDO}	Delay Time to Data Out Valid	C_L = 0 pF to 200 pF	90	260	ns
14	t_{DDZ}	Delay Time to Data Output Disabled	C_L = 0 pF to 200 pF	20	80	ns

SWITCHING TIME WAVEFORMS



Note 1: This diagram shows that Read and Write $\overline{CS}$ pulses occur on consecutive half-cycles of CLK, although this is not a restriction. Read and Write $\overline{CS}$ pulses must each occur at an 8 kHz rate.

TRANSMISSION CHARACTERISTICS

Unless otherwise noted: T_A = 0°C to 70°C, $V_{CCA} = V_{CCD}$ = 5.0 V ±5%, V_{SS} = –5 V ±5%, GNDD = GNDA = 0 V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Amplitude Response						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600 Ω)				
	0 dBm0	SC11305 SC11306		1.2276 1.2276		Vrms Vrms
t_{MAX}	Maximum Overload Level	SC11305 (+3.17 dBm0) SC11306 (+3.14 dBm0)		2.501 2.492		V_{DC} V_{DC}
G_{XA}	Transmit Gain, Absolute	T_A = 25°C, $V_{CCA} = V_{CCD}$ = 5.0 V V_{SS} = –5.0 V, Input at GSX = 0 dBm0 at 1020 Hz	–0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f= 16 Hz f= 50 Hz f= 60 Hz f= 200 Hz f= 300–3000 Hz f= 3300 Hz f= 3400 Hz f= 4000 Hz f= 4600 Hz and Up, Measured Response from 0 Hz to 4000 Hz	 –1.8 –0.15 –0.35 –0.7		 –0.1 0.15 0.05 0 –14 –32	 dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T_A = 0°C to 70°C			±0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V_{CCA} = V_{CCD}$ = 5.0 V ±5% V_{SS} = –5.0 V ±5%			±0.05	dB
G_{XRL}	Transmit Gain Variation with Level	Sinusoidal Test Method Reference Level = –10 dBm0 VF_XI^+ = –40 dBm0 to +3 dBm0 VF_XI^+ = –50 dBm0 to –40 dBm0 VF_XI^+ = –55 dBm0 to –50 dBm0	 –0.2 –0.4 –1.2		 0.2 0.4 1.2	 dB dB dB

TRANSMISSION CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
G_{RA}	Receive Gain, Absolute	T_A = 25°C, V_{CCA} = V_{CCD} = 5 V, V_{SS} = –5.0 V, Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	–0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f= 0–3000 Hz f= 3300 Hz f= 3400 Hz f= 4000 Hz	–0.15 –0.35 –0.7		0.15 0.05 0 –14	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T_A = 0°C to 70°C			±0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V_{CCA} = V_{CCD} = 5.0 V ±5%, V_{SS} = –5.0 V ±5%			±0.05	dB
G_{RRL}	Receive Gain Variation with Level	Sinusoidal Test Method: Reference Input PCM Code Corresponds to an Ideally Encoded –10 dBm0 Signal PCM Level = –40 dBm0 to +3 dBm0 PCM Level = –50 dBm0 to –40 dBm0 PCM Level = –55 dBm0 to –50 dBm0	 –0.2 –0.4 –1.2		 0.2 0.4 1.2	 dB dB dB
V_{RO}	Receive Output Drive Level	RL = 600 Ω	–2.5		2.5	V
Envelope Delay Distortion with Frequency						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz f = 600 Hz–800 Hz f = 800 Hz–1000 Hz f = 1000 Hz–1600 Hz f = 1600 Hz–2600 Hz f = 2600 Hz–2800 Hz f = 2800 Hz–3000 Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	µs µs µs µs µs µs µs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz f = 1000 Hz–1600 Hz f = 1600 Hz–2600 Hz f = 2600 Hz–2800 Hz f = 2800 Hz–3000 Hz	–40 –30	–25 –20 70 100 145	 90 125 175	µs µs µs µs µs
Noise						
N_{XC}	Transmit Noise, C Message Weighted	SC11305, VF_XI^+ = 0 V		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	SC11306, VF_XI^+ = 0 V		–74	–69 Note 1	dBm0p
N_{RC}	Receive Noise, C Message Weighted	SC11305, PCM Code Equals Alternating Positive and Negative Zero		8	11	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	SC11306, PCM Code Equals Positive Zero		–82	–79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0 V			–53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	VF_XI^+ = 0 V, V_{CCA} = V_{CCD} = 5.0 V_{DC} +100 mVrms, f = 0–50 kHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	VF_XI^+ = 0 Vrms, V_{SS} = –5.0 V_{DC} +100 mVrms, f = 0–50 kHz	40			dBC

TRANSMISSION CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero for SC11305 and SC11306, V_{CC} = –5.0 V_{DC} +100 mVrms				
		f = 0 Hz–4000 Hz	40			dBC
		f= 4k Hz–25k Hz	40			dBC
		f = 25k Hz–50k Hz	36			dBC
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero for SC11305 and SC11306 V_{SS} = 5.0 V_{DC} +100 mVrms				
		f = 0 Hz–4000 Hz	40			dBC
		f= 4k Hz–25k Hz	40			dBC
		f = 25k Hz–50k Hz	36			dBC
SOS	Spurious Out-of Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz–3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO				
		4600 Hz–7600 Hz			–32	dB
		7600 Hz–8400 Hz			–40	dB
		8400 Hz–100,000 Hz			–32	dB
Distortion						
STD_X	Signal to Total Distortion	Sinusoidal Test Method				
STD_R	Transmit or Receive Half-Channel	Level = 3.0 dBm0	33			dBC
		= 0 dBm0 to –30 dBm0	36			dBC
		= –40 dBm0 XMT	29			dBC
		RCV	30			dBC
		= –55 dBm0 XMT	14			dBC
		RCV	15			dBC
SFD_X	Single Frequency Distortion, Transmit				–46	dB
SFD_R	Single Frequency Distortion, Receive				–46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI^+ = –4 dBm0 to –21 dBm0, Two Frequencies in the Range 300–3400 Hz			–41	dB
Crosstalk						
CT_{X-R}	Transmi to Receive Crosstalk 0 dBm0 Transmit Level	f = 300–3400 Hz at 0 dBm0 Steady PCM Receive Code		–90	–75	dB
CT_{R-X}	Receive to Receive Crosstalk 0 dBm0 Receive Level	f = 300–3400 Hz		–90	–70 Note 2	dB

Note 1: Measured by extrapolation from the distortion test result.
Note 2: CT_{R-X} is measured with a –40 dBm0 activating signal applied at VF_XI^+.

	SC11305 μLaw								SC11306 True A-Law, C5 = 0 (Includes Even Bit Inversion)							
	MSB							LSB	MSB							LSB
V_{IN} = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = 0 V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
V_{IN} = –Full-Scale	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0
	Not Applicable (C5 is Don't Care)								Sign + Magnitude A-Law, C5 = 1 (Before Even Bit Inversion							
V_{IN} = +Full-Scale									1	1	1	1	1	1	1	1
V_{IN} = 0 V									1	0	0	0	0	0	0	0
V_{IN} = –Full-Scale									0	0	0	0	0	0	0	0
									1	1	1	1	1	1	1	1

APPLICATIONS INFORMATION

Power Supplies

While the pins of the SC11305 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used. GNDA and GNDD MUST be connected together adjacent to each CODEC/filter, not on the connector or backplane wiring.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 µF supply decoupling capacitors should be connected from this common ground point to V_{CCA} and V_{SS}.

For best performance, the ground point of each CODEC/filter on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{SS} with 10 µF capacitors.

The positive power supply to the bus drivers, V_{CCD}, is provided on a separate pin from the positive supply for the CODEC and filter circuits to minimize noise injection when driving the bus. V_{CCA} and V_{CCD} MUST be connected together close to the CODEC/filter at the point where the 0.1 µF decoupling capacitor is connected.

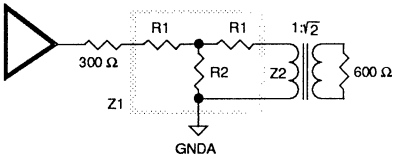
Receive Gain Adjustment

For applications where an SC1130X family CODEC/filter receive output must drive a 600 Ω load, but a peak swing lower than ±2.5 V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table 2 lists the required resistor values for 600 Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example, a 30 dB return loss against 600 Ω is obtained if the output impedance of the attenuator is in the range 282 Ω to 319 Ω (assuming a perfect transformer).

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Table 2. Attenuator Tables for Z1=Z2=300 Ω (All Values in Ω)

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{WHERE: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

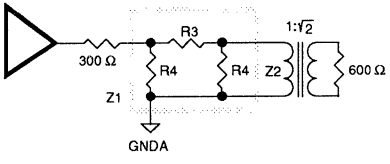
and

$$S = \sqrt{\frac{Z1}{Z2}}$$

Also: $Z = \sqrt{Z_{SC} \cdot Z_{OC}}$

Where Z_{SC} = Impedance with short circuit termination and Z_{OC} = Impedance with open circuit termination

π-Pad Attenuator



$$R3 = \sqrt{\frac{Z1.Z2}{2}}\,\frac{N^2-1}{N}$$

$$R4 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

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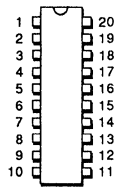
FEATURES

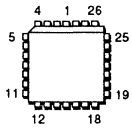
- ☐ Gain adjustable from –25.5 to +25.5 dB in steps of 0.1 dB
- ☐ 0.05 dB gain/loss error
- ☐ Gain/loss setting via parallel, serial and through interfaces
- ☐ Two modes for gain/loss values (binary-weighted and quasi binary-weighted)
- ☐ Monotonic gain/loss setting
- ☐ 200 kHz large signal and 1.5 MHz small signal bandwidth for gain of +25.5 dB
- ☐ –60 dB total harmonic distortion
- ☐ 10 dBrnC idle channel noise
- ☐ 40 mW power dissipation

20-PIN DIP PACKAGE



SC11310CN

28-PIN PLCC PACKAGE



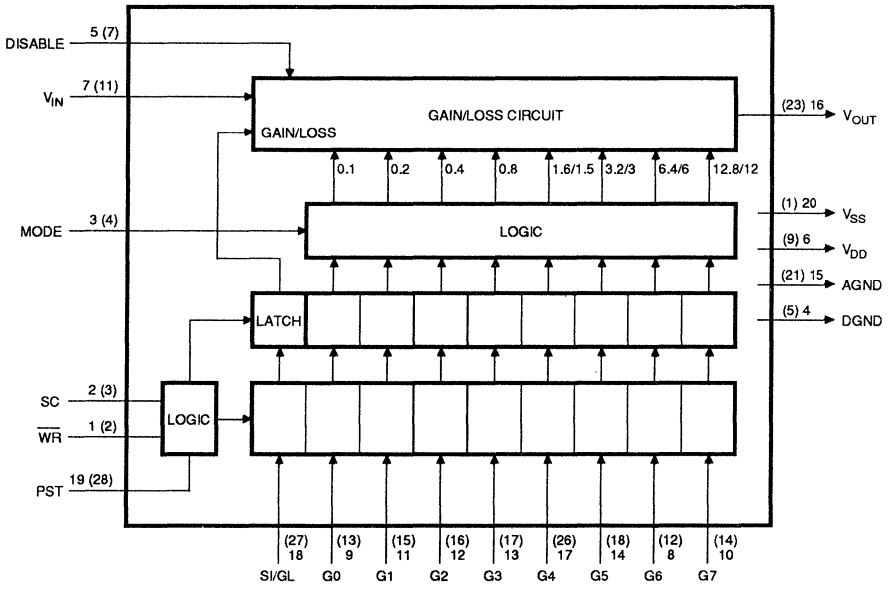
SC11310CV

GENERAL DESCRIPTION

The programmable gain/loss circuit is a general purpose programmable amplifier/attenuator. It can be used in applications where a signal amplitude has to be precisely controlled over a wide dynamic range. The control is done by an 8 bit binary word, which results in 256 steps of 0.1 dB each. Another bit selects between gain and loss.

The PGLC has two modes of gain control. The circuit has three digital interfaces: serial, parallel clocked input and parallel fixed input (through). The PGLC is processed in low power CMOS technology. It is housed in a 20-pin DIP package and uses a ±5 Volt power supply for operation. A block diagram of the chip is shown below.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINOUTS. NUMBERS IN ( ) ARE PLCC PINS. PINS (6), (8), (10), (19), (20), (22), (24), & (25) ARE NOT CONNECTED.

PIN DESCRIPTIONS (SC11401 AND SC11403)

PIN	NAME	DESCRIPTION
1 (2)	$\overline{WR}$	Write enable
2 (3)	SC	Serial clock
3 (4)	MODE	Selects the gain control mode (See Table 1)
4 (5)	DGND	Digital ground
5 (7)	DISABLE	Disables the analog output. To disable, tie to V_{CC}.
6 (9)	V_{CC}	Positive supply voltage +5 V
7 (11)	V_{IN}	Analog input
8 (12) 9 (13) 10 (14) 11 (15) 12 (16) 13 (17) 14 (18) 17 (26)	G6 G0 G7 G1 G2 G3 G5 G4	Gain/Loss control bits used in the parallel and through modes of operation.
15 (21)	AGND	Analog ground
16 (23)	V_{OUT}	Analog output
18 (27)	Si/GL	In paralle or through mode it constitutes the gain/loss control (Si/GL = (1) gain (0) loss). In serial mode it is the serial input port.
19 (28)	PST	Interface select: PST = V_{CC} Parallel interface PST = GND Serial interface PST = V_{SS} Through mode
20 (1)	V_{SS}	Negative supply voltage -5 V

Numbers in ( ) refer to 28-pin PLCC package.

FUNCTIONAL DESCRIPTION

The operation of the IC is controlled by 10 inputs, G0–G7, Si/GL and MODE. The G0–G7 inputs constitute an 8 bit word that controls the magnitude of the gain/loss setting. The Si/GL input selects between amplification or attenuation. MODE pin selects the two different control modes, shown in Table 1.

For MODE = 1 the circuit has 511 distinct steps and the gain varies from –25.5 dB to +25.5 dB. The gain or loss is selected through the Si/GL pin. The total dynamic range in this mode is 51 dB.

For MODE = 0 the circuit has 481 distinct steps and the gain varies from –24 dB to +24 dB, which results in a dynamic range of 48 dB.

G7	G6	G5	G4	G3	G2	G1	G0	GAIN/LOSS (DB) MODE = 1	MODE = 0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.1	0.1
0	0	0	0	0	0	1	0	0.2	0.2
0	0	0	0	0	1	0	0	0.4	0.4
0	0	0	0	1	0	0	0	0.8	0.8
0	0	0	1	0	0	0	0	1.6	1.5
0	0	1	0	0	0	0	0	3.2	3.0
0	1	0	0	0	0	0	0	6.4	6.0
1	0	0	0	0	0	0	0	12.8	12.0

Table 1.

The interface to the chip can be accomplished in three different ways controlled by the PST (parallel/serial/through) pin.

a) Parallel Mode

When PST = V_{CC}, the interface to the chip is accomplished through the parallel bus. The G0–G7 constitute the gain/loss control bits and Si/GL is the gain/loss control.

If Si/GL = V_{CC}, the IC will have gain and when Si/GL=GND, it will have loss. The $\overline{WR}$ pin is used to write the

data into the chip. The timing is shown in Figure 2.

The data is latched into the chip on the rising edge of $\overline{WR}$ and the new value of gain/loss will be effective at the same time.

b) Serial Mode

When PST = GND (0 V), the interface will be accomplished through the serial port. In this mode, Si/GL constitutes the serial input port, where SC is the shift clock and $\overline{WR}$ is the enable clock. The timing is shown in Figure 3.

After applying nine SC clock pulses the data is latched into the chip on the rising edge of $\overline{WR}$ and the gain/loss becomes effective. At the same time, during the serial shift the internal register will hold the previous gain/loss value preventing the output from making unpredictable changes.

c) Through Mode

When PST = V_{SS}, the interface will operate in the through mode. In this mode, $\overline{WR}$ and SC are ignored, and the data that is placed on the parallel bus will be effective at all times.

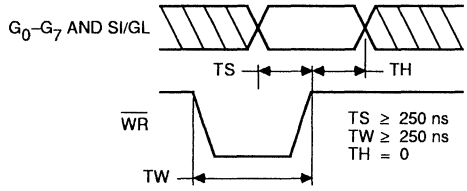


Figure 2. Waveforms for Write Cycle In Parallel Mode

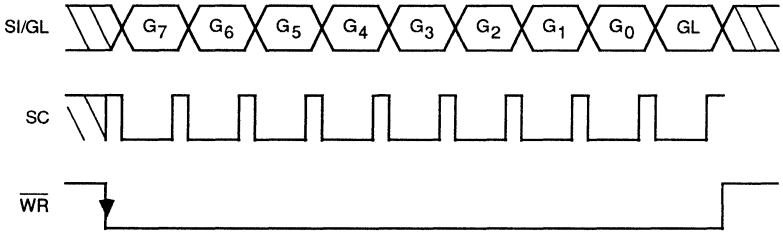


Figure 3. Waveforms for Write Cycle In Serial Mode

POWER SUPPLY DECOUPLING AND CIRCUIT LAYOUT CONSIDERATIONS

For optimum performance and lowest idle channel noise figure, it is important to decouple the power supplies as shown in Figure 4. Small inductors in series with the positive and negative supplies help suppress RFI as well as improve the power supply noise rejection capability of the SC11310 when used with the decoupling capacitors. The 10 µF capacitors should be tantalum type while the 0.1 µF capacitors should have a good high frequency rejection characteristic, monolithic ceramic types are recommended.

It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11310 as possible.

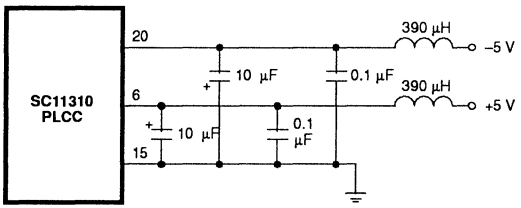


Figure 4. Power Supply Decoupling

ABSOLUTE MAXIMUM RATINGS (Note 1, 2 and 3)

Supply Voltage, V_{CC}	+6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signal)	V_{SS}–0.6 V to V_{CC}+0.6
DC Input Voltage (Digital Signal)	V_{SS}–0.6 V to V_{CC}+0.6
Storage Temperature Range	–65 to +150°C.
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering, 10 sec)	300°C.

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

2. Unless otherwise specified, all voltages are referenced to ground

3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

OPERATING CONDITIONS

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature					
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
SC	Clock Frequency			3		MHz
T_R,T_F	Input Rise or Fall Time	All Digital Inputs Except SC			500	ns
T_R,T_F	Input Rise or Fall Time	SC			20	ns

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = +5 V ±10%, V_{SS} = –5 V ±10%

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current			4	6	mA
I_{SS}	Quiescent Current			4	6	mA
V_{IH}	High Level Input Voltage; Digital Pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital Pins				0.8	V

AC ELECTRICAL CHARACTERISTICS

PARAM.	DESCRIPTION	COND.	MIN	TYP	MAX	UNITS
	PSRR (V_{CC}) @ 1 kHz PSRR (V_{SS}) @ 1 kHz			60 70		dB dB
	Offset Voltage for 0 dB Gain 25.5 dB Gain			 15 60		 mV mV
	Idle Channel Noise for 25.5 dB Gain			10		dBrnC
	Total Harmonic Distortion for			60		dB
	0.1 dB Large-Signal Bandwidth (Note 1)			200		kHz
	–3 dB Small-Signal Gain-Bandwidth Product (Note 2)			1.5		MHz
	Response Time to Gain-Switching			5		µs
	Maximum Gain Error				0.05	dB

Notes: 1. The –0.1 dB large-signal (7.5 Vpp) bandwidth of the chip when driving 600 Ω parallel with 100 pF and for a gain of 25.5 dB.
2. The –3 dB small signal (100 mVpp) gain-bandwidth when driving 600 Ω parallel with 100 pF load.

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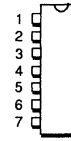
FEATURES

- ☐ Programming frequency from DC to 3.5 KHz with ±0.1 dB amplitude attenuation
- ☐ Gain error—±1.0 dB
- ☐ Harmonic distortion—45 dB
- ☐ On chip crystal oscillator
- ☐ No external components required
- ☐ Uncommited op-amp for smoothing the sinewave output
- ☐ 32 bit data in shift register
- ☐ 5 Volt & 10 Volt operation
- ☐ 200 mW absolute maximum power dissipation
- ☐ 0°C to 70°C operating temperature range

8-PIN DIP PACKAGE

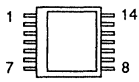
SC11314CN

14-PIN DIP PACKAGE



SC11313CN

14-PIN SOIC PACKAGE



SC11313CM
SC11314CM

GENERAL DESCRIPTION

The Programmable Sine/Squarewave Generator are CMOS integrated circuits which allow the users to generate either a sinewave or a squarewave from DC to 3.5 KHz with an accuracy of 0.1 dB in amplitude or from 3.5 KHz to 8 KHz with an accuracy of ±1.0 dB. This function is implemented with no external components.

The SC11313/SC11314 contains a serial input interface, two programmable counters, and a band pass switched capacitor filter. One of the programmable counters is used to generate squarewave tones, while the other is the sampling clock for the bandpass switched capacitor filter. Sinewaves are generated by attenuating the harmonics of the squarewave tones through the filter.

The SC11314CN is an 8-pin plastic DIP, while the SC11313CN is offered in a 14-pin plastic DIP. The SC11314CM and the SC11313CM are offered in a 14-pin SOIC package.

The difference between SC11314 and SC11313 is that the SC11314 is a single 5 Volt power supply, while the SC11313 can be powered with a 10 Volt power supply. The 10 Volt can be either a dual 5 Volt or a single 10 Volt supply.

Furthermore, the SC11313 is provided with an uncommitted operational amplifier and the squarewave generator is externally accessible rather than internally connected.

The output amplitude for the SC11313/SC11314 is adjustable from 0 dB to –15 dB in steps of 1 dB.

The SC11313 and SC11314 are intended to provide low cost, accurate generation of precise test and signaling tones.

BLOCK DIAGRAM

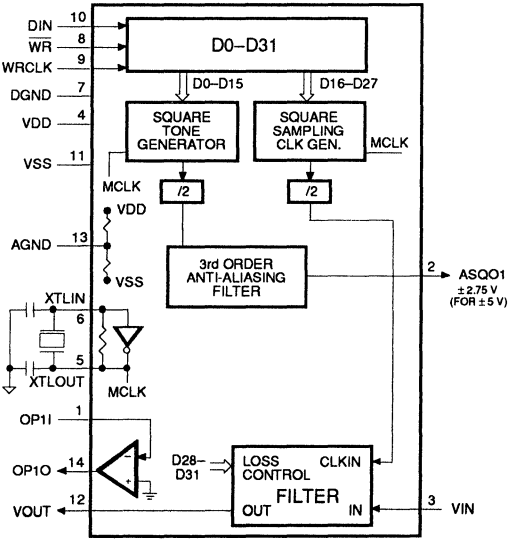


Figure 1. SC11313CN, CM

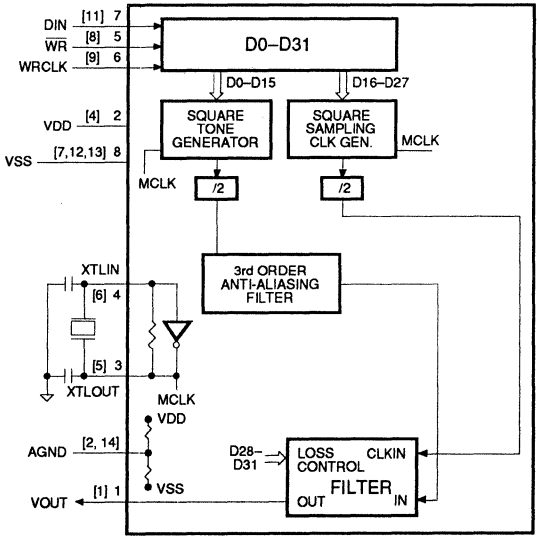


Figure 2. SC11314CN, SC11314CM [ ]

* Note: Numbers in [ ] are for 11314 SOIC package.

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	OP1I	The negative-input of the uncommitted 600 Ω opamp
2	ASQO1	The analog output of the square tone attenuator
3	VIN	The input of the switched-capacitor filter
4 (2) [4]	VDD	Positive power supply VDD = +5 V ±5%
5 (3) [5]	XTLOUT	The output pin of the oscillator
6 (4) [6]	XTLIN	The input pin of the oscillator
7	DGND	Digital Ground
8 (5) [8]	$\overline{WR}$	Write Select Input: This digital input is used to address the chip to write the data register
9 (6) [9]	WRCLK	Write Clock Input: This digital input is used to signal each serial bit transfer to the shift register
10 (7) [11]	DIN	Serial Data Input: This digital input is used to provide 32-bit serial data to the internal shift register.
11 (8) [7,12,13]	VSS	Negative power supply VSS = –5 V ±5% for 10 V power supply or analog ground for 5 V power supply
12 (1) [1]	VOUT	The output of the switched-capacitor filter
13 [2] [14]	AGND	Analog ground for 10 V power supply or open as 2.5 V vref for 5 V power supply
14	OP1O	The output of the uncommitted 600 Ω opamp

Numbers are SC11313CN and SC11313CM, in ( ) are SC11314CN, in [ ] are SC11314CM

FUNCTIONAL DESCRIPTION

Programming the SC11313/ SC11314

The SC11313/SC11314 is programmed by a 32 bit serial word. Programming is initiated by $\overline{WR}$ and WRCLK (See Figure 3) both being low. Once the 32 bits of data has been loaded into the shift register the rising edge of $\overline{WR}$ will load the data into internal latches.

Squarewave Generation

The squarewave generator is a divider that is programmed by bits D0–D15. A divide by two stage has been inserted after the squarewave generator to insure a symmetrical squarewave. The frequency of the squarewave is determined by the following formula:

Mclk / [2 • (D15D14...D0)]

Mclk is the frequency of the master clock. In order to attenuate the high frequency harmonics of the squarewave a 3rd order anti-aliasing filter follows the squarewave generator.

Sinewave Generation

A sinewave is generated by filtering the output of the squarewave generator. The filter used is a 5th order bandpass switched capacitor filter with a 0–15 dB attenuator. It consists of 16 steps with each step equal to 1 dB. Attenuation is selected by bits D28–D32. For a sampling frequency of fc, the cutoff frequency is fc/51. Also there is a notch at 3fc/51. An uncommitted op-amp has been included on chip to be used to smooth the output of the switched capacitor filter. This op-amp is capable of driving 600 Ω.

Switched-Capacitor Bandpass Filter

This is a 5th-order bandpass filter. Given a sampling frequency fc, the cutoff frequency will be fc/51 and a notch at 3fc/51. The minimum attenuation of the stopband is 50 dB (Fig. 4). D31–D28 adjusts the attenuation of signal, according to the following table. The maximum attenuation is 15 dB.

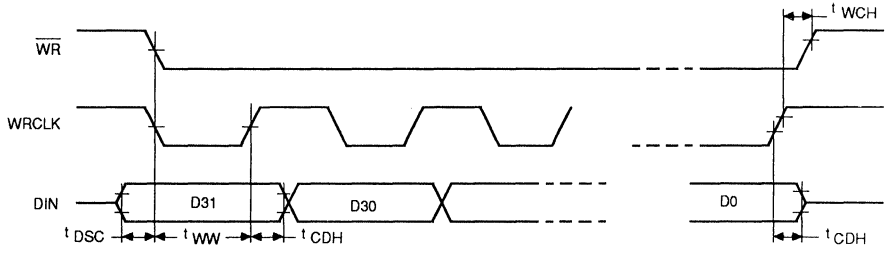
D31	D30	D29	D28	ATT. (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	1	0	0	4
1	0	0	0	8

Uncommitted 600 Ω Driver

The 600 Ω driver can be configured as an RC active filter to smooth the filter output.

Crystal Oscillators

Figure 5 shows a typical crystal implementation. The capacitors C1 and C2 have a range of 5 to 20 pF. For frequencies less than 10 MHz capacitance values of less than 20 pF, for frequencies above 10 MHz capacitance values of 5 pF to 10 pF are recommended.



Note 1: t_{DSC}, this timing refers to $\overline{WR}$ and WRCLK, they need both to be low

Serial Input Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DSC}	Data Set-up Time to Clock	10			ns
t_{WW}	Write Clock Pulse Width	300			ns
t_{CDH}	Clock to Data Hold Time	60			ns
t_{WCH}	Clock to Write Enable Hold Time	60			ns
CLK_{OUT}	Clock Frequency			2.5	MHz

Figure 3. The Timing of the Input Interface

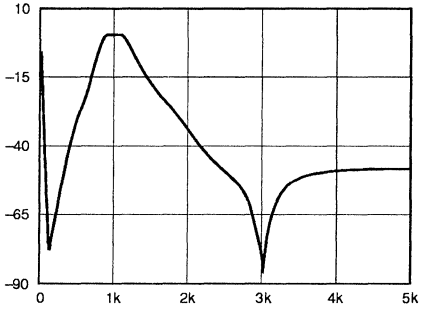


Figure 4. The Response of the Switched-Capacitor Filter With Sampling Frequency 51 kHz.

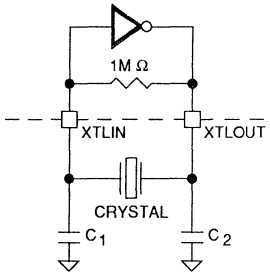


Figure 5. Typical Crystal Implementation

TYPICAL APPLICATIONS

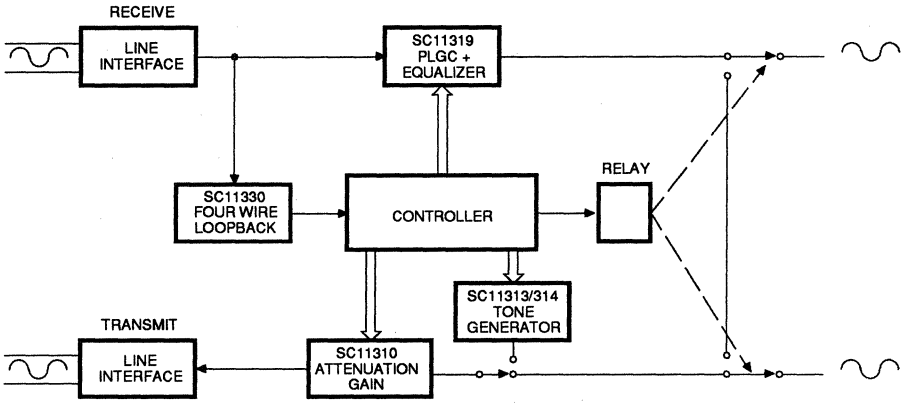


Figure 6. 4-Wire Termination Equipment

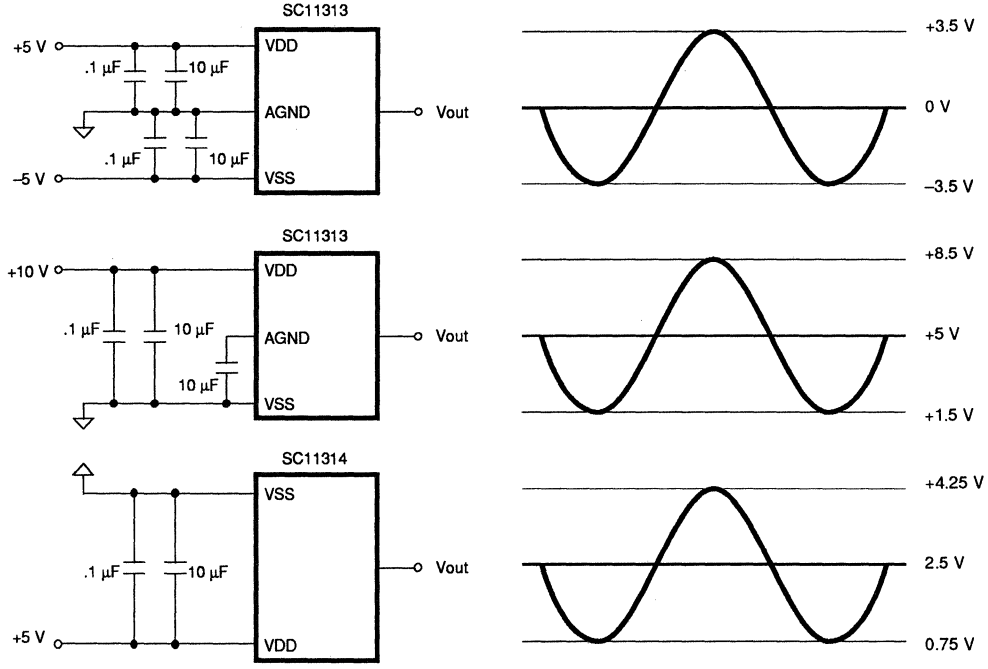


Figure 7. Typical Output

ABSOLUTE MAXIMUM RATINGS (Note 1, 2 and 3)

Supply Voltage, V_{CC}	+6 V
Supply Voltage, V_{SS} (For dual power supply)	– 6 V
DC Input Voltage (Analog Signal)	V_{SS}–0.6 V to V_{CC}+0.6
DC Input Voltage (Digital Signal)	V_{SS}–0.6 V to V_{CC}+0.6
Storage Temperature Range	–65 to +150°C.
Power Dissipation (Note 3)	200 mW
Lead Temperature (Soldering, 10 sec)	300°C.

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

2. Unless otherwise specified, all voltages are referenced to ground

3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

OPERATING CONDITIONS

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature					
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
F_{ms}	Master Clock				20	MHz
T_R,T_F	Input Rise or Fall Time	All Digital Inputs			30	ns

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = +5 V ±10%, V_{SS} = –5 V ±10%

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	20 MHz Master Clock		10	15	mA
I_{SS}	Quiescent Current	20 MHz Master Clock		10	15	mA
V_{IH}	High Level Input Voltage; Digital Pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital Pins				0.8	V

SC11313

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage; XTLIN		V_{DD} – 1.5			V
V_{IL}	Low Level Input Voltage; XTLIN				V_{SS} + 1.5	V
V_{OH}	High Level Output Voltage; XTLOUT (I_{OH} = 100 µA)			V_{DD} – 1		V
V_{OL}	Low Level Output Voltage; XTLOUT (I_{OL} = 100 µA)				V_{SS} + 1	V

SC11314

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage; XTLIN		V_{DD} – 3			V
V_{IL}	Low Level Input Voltage; XTLIN				V_{SS} + 3	V
V_{OH}	High Level Output Voltage; XTLOUT (I_{OH} = 100 µA)		V_{DD} – 2			V
V_{OL}	Low Level Output Voltage; XTLOUT (I_{OL} = 100 µA)				V_{SS} + 2	V

AC ELECTRICAL CHARACTERISTICS

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vos	Offset Voltage of Sinewave			15		mV
THD	Total Harmonics Distortion for a 10 Vp–p 1 kHz Sinewave			60		dB
HD	Harmonic Distortion				–45	dB
AR	Amplitude Ripple	F_{OUT} < 3.5 KHz 3.5 < F_{OUT} > 8 KHz			±.1 ±1	dB dB
V_{OUT}	Max. Sinewave Amplitude	SC11313 SC11314			10 4	dBm dBm
V_{LN}	V_{OUT} Loss Error				±.5	dB

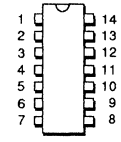
SIERRA SEMICONDUCTOR

SC11319
Telephone Line Equalizer With Programmable Gain/Loss Circuit

FEATURES

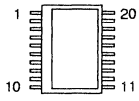
- ☐ Telephone Line Equalizer with adjustable slope, height and bandwidth
- ☐ 60 Hz rejection filter
- ☐ On-chip continuous anti-aliasing and smoothing filters
- ☐ Logarithmic Gain/Attenuator adjustable from –25.5 to +25.5 dB in steps of 0.1 dB
- ☐ Various bypass and loopback modes
- ☐ Two modes for gain/loss values (binary-weighted and quasi binary-weighted)
- ☐ Monotonic gain/loss setting
- ☐ Selectable master clock (1.536 MHz, 1.544 MHz, 2.048 MHz, or 3.5795454 MHz)
- ☐ Low supply current. 15 mA typical from ±5 V supplies.
- ☐ Standard 14-pin 0.3" DIP or 20-pin SOIC

14-PIN DIP PACKAGE



SC11319CN

20-PIN SOIC PACKAGE



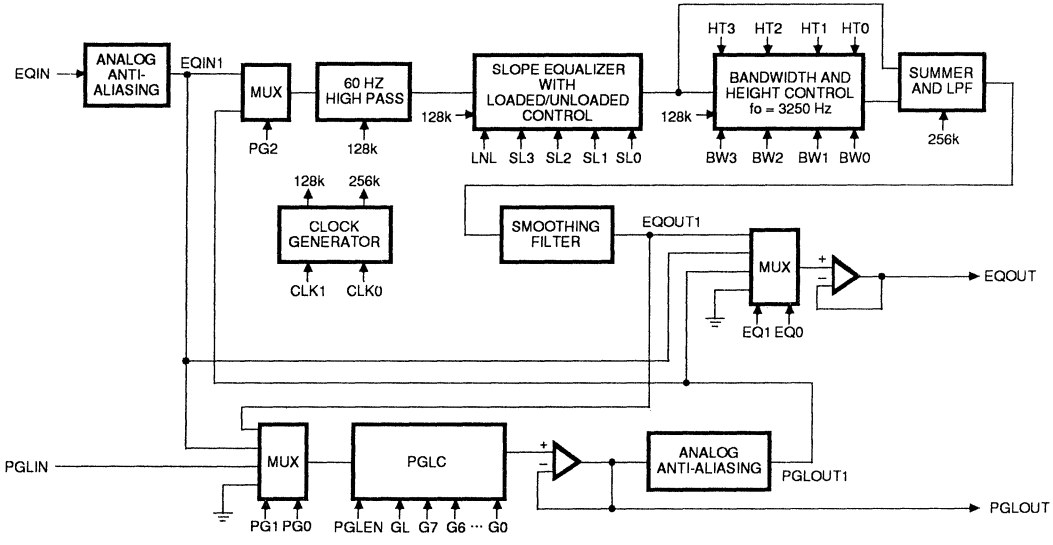
SC11319CM

GENERAL DESCRIPTION

The SC11319 combines the functions of a telephone line equalizer with a programmable gain/loss circuit. The telephone line equalizer is a telephone industry standard for equalizing long lengths of cable. It consists of several programmable switched capacitor filter sections that realize a family of frequency response curves optimized for telephone line equalization. Integrated on the chip are continuous anti-aliasing filters, 60 Hz high-pass filter, three programmable sections for slope, height and bandwidth adjustments, an output smoothing filter and a 600 Ω driver (See Block Diagram).

The programmable gain/loss circuit is a general purpose programmable amplifier/attenuator. The control is done by an eight bit binary word which results in 256 steps of 0.1 dB each. Another bit selects between gain and loss. The programmable gain/loss circuit also has two modes of gain/loss values (binary-weighted and quasi binary-weighted).

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	Mode	Gain control mode, TTL input. Selects between binary/quasi binary steps. (See Table 3)
2 (3)	PGLIN	Analog input to the Programmable Gain/Loss circuit
3 (4,5)	V_{CC}	Positive power supply pin. V_{CC} = +5 V ±10%
4 (6)	EQIN	Analog input to the Line Equalizer circuit
5 (7)	$\overline{WR}$	Serial interface write signal, TTL input. During the low period of this signal, the data shifts into the SIN pin.
6 (9)	SCLK	Input shift clock, TTL input. This clock shifts the data into the SIN pin after the falling edge of WRB.
7 (10)	DGND	Digital ground. All digital signals are referenced to this pin.
8,9 (11,13)	XTLOUT XTLIN	Crystal oscillator pins. XTLOUT and XTLIN connect to a crystal to generate a crystal locked clock for the chip. If a suitable clock is already available in the system, the XTLIN pin can be driven.
10 (14)	SIN	Serial interface input data pin, TTL input.
11 (15,16)	V_{SS}	Negative power supply pin. V_{SS} = –5 V ±10%
12 (17)	EQOUT	Analog output of the Line Equalizer circuit.
13 (19)	AGND	Analog ground. All analog signals are referenced to this pin.
14 (20)	PGLOUT	Analog output of the Programmable Gain/Loss circuit.
(2,8,12,18)	NC	Not connected

NOTE: Pin numbers are 14-pin DIP; pin numbers in ( ) are 20-pin SOIC

FUNCTIONAL DESCRIPTION

The block diagram of SC11319 consists of a telephone line equalizer, a programmable gain/loss circuit, a digital section for the serial interface and clock generator, and several loopback and bypass modes.

Equalizer Section

The equalizer section consists of a continuous time anti-aliasing filter with a typical 3 dB frequency at 25 kHz and 28 dB of rejection at 128 kHz. This is followed by a 60 Hz highpass filter with a typical 3 dB frequency at 120 Hz. The highpass filter is followed by the slope equalizer section. The slope equalizer is a highpass filter with a high frequency pole added. The gain, poles and zeros are adjusted by the SL1–4 and L/NL control bits. (See Table 1). This provides a slope like response in the 200 to 3000 Hz region in the nonloaded mode (L/NL = 0) or low frequency attenuation in the loaded mode (L/NL = 1). The output of the slope section is connected to a summing amplifier and to the input of a biquad bandpass filter whose output is also connected to the summing amplifier. The biquad bandpass has its Q and gain controlled by the BW1–4 (bandwidth) and HT1–3 (height) control bits. (See Table 2). The bandpass filter output summed with its input can provide either a bump (bandpass + 1) at 3250 Hz (its center frequency) in high Q setting or a slope-type response in the 200 to 3000 Hz region in the low Q setting. The output of the summing amplifier goes through a continuous smoothing filter with a typical 3 dB frequency at 25 kHz and 28 dB of rejection at 128 kHz.

Programmable Gain/Loss Section

The programmable gain/loss circuit is a general purpose programmable amplifier/attenuator. It is controlled by an eight bit binary word (G0–G7) which results in 256 steps of 0.1 dB each. Another bit (GL) selects between gain and loss. (See Table 3).

The programmable gain/loss circuit also has two different modes of gain control. (See Table 3). For Mode = 1, the circuit has 511 steps and the gain varies from –25.5 dB to +25.5 dB. For Mode = 0, the circuit has 481 steps and the gain varies from –24 dB to +24 dB.

Clock Generator

The clocks for the filters in the equalizer section are provided by an on-chip oscillator that needs an external crystal. Four different oscillation frequencies can be used; 1.536 MHz, 1.544 MHz, 2.048 MHz and 3.5795454 MHz. The selection of clock source is made by control bits CLK1 and CLK0. (See Table 4).

Serial Interface

The integrated circuit has a three pin serial interface. When $\overline{WR}$ goes low, sixteen bits of data are shifted serially into the chip through the SIN pin. The sixteen bits constitute 15 bits of control data and 1 bit of destination address. The data is sampled on the rising edge of the

Slope Equalizer = $1 + \frac{H_{hp} \bullet S}{S + \omega_{hp}}$

Loaded (L/NL = 1), $\omega_{hp} = 2 \times 400 \bullet 7$

Nonloaded (L/NL = 0), $\omega_{hp} = 2 \times 1820$

SL3	SL2	SL1	SL0	HIGHPASS GAIN (H_{hp})
0	0	0	0	0
0	0	0	1	0.2
0	0	1	0	0.4
0	0	1	1	0.6
0	1	0	0	0.8
0	1	0	1	1.0
0	1	1	0	1.2
0	1	1	1	1.4
1	0	0	0	1.6
1	0	0	1	1.8
1	0	1	0	2.0
1	0	1	1	2.2
1	1	0	0	2.4
1	1	0	1	2.6
1	1	1	0	2.8
1	1	1	1	3.0

Table 1

shift clock (SCLK). When $\overline{WR}$ goes high, the contents of the internal latches selected by bit 15 is updated. (See Figure 1 for serial timing and data destination). For proper operation of the interface, there has to be exactly sixteen shift clock pulses within the $\overline{WR}$ high-to-low and low-to-high transition period.

Loopback and Bypass Modes

The integrated circuit provides several loopback and bypass options. The Programmable Gain/Loss section can be configured as a pre-amplifier or post-attenuator for the Equalizer section. It can also be operated independently as a separate unit.

The filter section of the Equalizer can also be bypassed by setting the control bits EQ0 = 1 and EQ1 = 0. In this mode, frequency response effects of the switched-capacitor filters are eliminated. It, therefore offers very flat frequency response and low noise over the 200 to 3000 Hz range. (See Table 5 for various loopback and bypass paths).

Bandpass Equalizer = $1 + \frac{(k-1)\frac{\omega_{BQ}}{Q_{BQ}} \bullet S}{S^2 + \frac{\omega_{BQ}}{Q_{BQ}} \bullet S + \omega^2_{BQ}}$

$\omega_{BQ} = 2 \bullet 3250$ Hz

HT3	HT2	HT1	HT0	k	BW3	BW2	BW1	BW0	Q_{BQ}
0	0	0	0	1.0	0	0	0	0	16.2
0	0	0	1	1.07	0	0	0	1	14.5
0	0	1	0	1.148	0	0	1	0	12.9
0	0	1	1	1.23	0	0	1	1	11.25
0	1	0	0	1.32	0	1	0	0	9.6
0	1	0	1	1.43	0	1	0	1	8.0
0	1	1	0	1.57	0	1	1	0	6.3
0	1	1	1	1.73	0	1	1	1	4.6
1	0	0	0	1.95	1	0	0	0	3.6
1	0	0	1	2.08	1	0	0	1	3.25
1	0	1	0	2.24	1	0	1	0	2.9
1	0	1	1	2.42	1	0	1	1	2.5
1	1	0	0	2.64	1	1	0	0	2.1
1	1	0	1	2.9	1	1	0	1	1.7
1	1	1	0	3.2	1	1	1	0	1.3
1	1	1	1	3.63	1	1	1	1	0.9

Table 2

G7	G6	G5	G4	G3	G2	G1	G0	GAIN/LOSS (dB) MODE = 1	MODE = 0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.1	0.1
0	0	0	0	0	0	1	0	0.2	0.2
0	0	0	0	0	1	0	0	0.4	0.4
0	0	0	0	1	0	0	0	0.8	0.8
0	0	0	1	0	0	0	0	1.6	1.5
0	0	1	0	0	0	0	0	3.2	3.0
0	1	0	0	0	0	0	0	6.4	6.0
1	0	0	0	0	0	0	0	12.8	12.0

Table 3

CLK1	CLK0	CLOCK SELECT
0	0	1.536 MHz
0	1	1.544 MHz
1	0	2.048 MHz
1	1	3.5795454 MHz

Table 4

PG1	PG0	PGL (Programmable Gain/Loss) Input
0	0	PGLIN
0	1	EQIN1
1	0	EQOUT1
1	1	GND

Table 5b

EQ1	EQ0	EQOUT (Equalizer Output)
0	0	EQOUT1
0	1	EQIN1
1	0	PGLOUT1
1	1	GND

Table 5a

PG2	Equalizer Input
0	PGLOUT1
1	EQIN1
PGLEN	**PGL (Programmable Gain/Loss) Block**
0	Disabled (PGLOUT Grounded)
1	Enabled

Table 5c

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, V_{CC}	+6V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signal)	V_{SS}–0.5 V to V_{DD}+0.5 V
DC Input Voltage (Digital Signal)	V_{SS}–0.5 V to V_{DD}+0.5 V
Storage Temperature Range	–65 to +150°C.
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 sec.)	300°C.

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

OPERATING CONDITIONS

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
XTLIN, XTLOUT	Crystal Frequency		1.544		3.579	MHz
T_R, T_F	Input Rise or Fall Time	All Digital Inputs			50	ns
V_I	Analog Input Voltage	PLGC section	–3.75		+3.75	V
V_I	Analog Input Voltage	Line Equalizer section	–3.0		+3.0	V

DC ELECTRICAL CHARACTERISTICS (T_A = 0–70°C, V_{CC} = +5 V ±10%, V_{SS} = –5 V ±10%

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current			15		mA
I_{SS}	Quiescent Current			15		mA
V_{IH}	High Level Input Voltage; All Inputs Except XTLIN		2.2			V
V_{IL}	Low Level Input Voltage; All Inputs Except XTLIN				0.8	V
V_{OH}	High Level Output; All Outputs Except XTLOUT (I_{OH} = 0.5 mA) (I_{OH} = 100 µA)		 2.4 4.5			 V V
V_{OL}	Low Level Output; All Outputs Except XTLOUT (I_{OL} = 1.6 mA) (I_{OL} = 100 µA)				 0.6 –4.5	 V V
V_{IH}	High Level Input Voltage; XTLIN		V_{DD}–3			V
V_{IL}	Low Level Input Voltage; XTLIN				V_{SS}+3	V
V_{OH}	High Level Output XTLOUT (I_{OH} = 100 µA)		V_{DD}–2			V
V_{OL}	Low Level Output XTLOUT (I_{OL} = 100 µA)				V_{SS}+2	V

SERIAL INPUT TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{WCS}	Write Enable to Clock Set Up Time	50			ns
t_{DCS}	Data Ready to Clock Set-Up Time	50			ns
t_{CDH}	Clock to Data Hold Time	50			ns
t_{WCH}	Clock to Write Enable Hold Time	50			ns
t_{CSW}	Clock Set Up Time to Write Enable			50	ns
CLK_{FREQ}	Clock Frequency			2.5	MHz

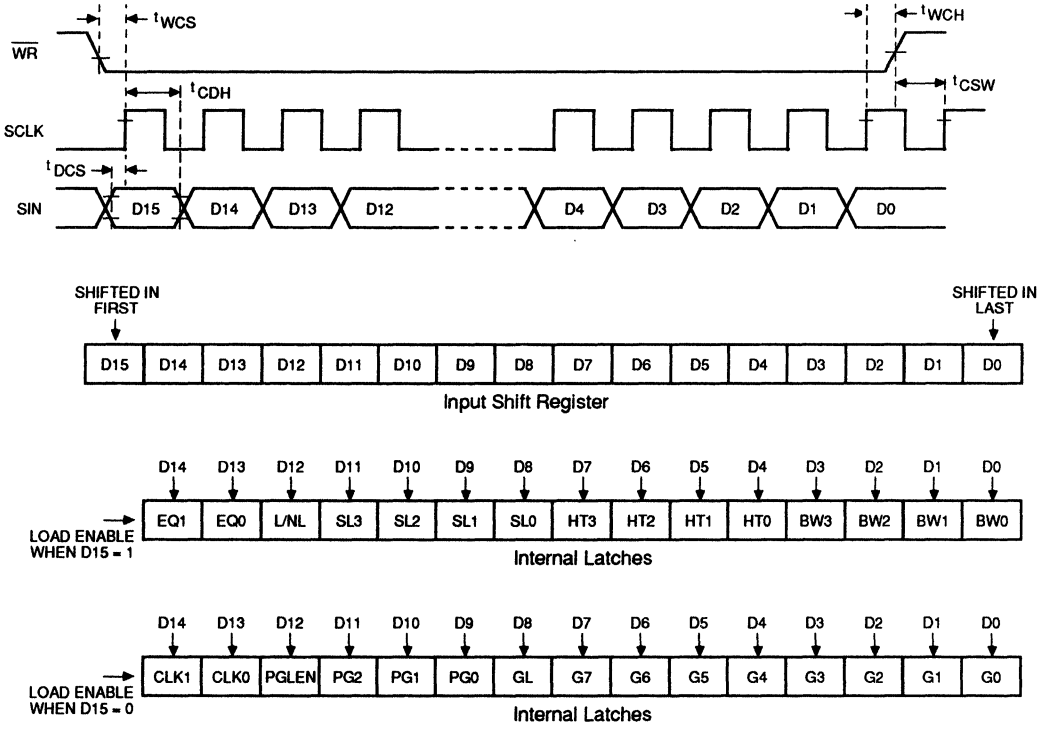


Figure 1. Serial Interface

AC ELECTRICAL CHARACTERISTICS (PGLC section)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	PSRR (Vcc) @ 1 KHz and 200 mVp-p PSRR (Vcc) @ 1 KHz and 200 mVp-p PSRR (Vss) @ 1 KHz and 200 mVp-p PSRR (Vss) @ 1 KHz and 200 mVp-p	0 dB gain +25.5 dB gain 0 dB gain +25.5 dB gain		–40 –30 –50 –45		dB dB dB dB
	Offset Voltage for 0 dB gain 25.5dB gain			 15 60		 mV mV
	Idle channel noise for +25.5dB gain			10		dBrnC
	Total harmonic distortion for an 7.5Vp-p, 1 KHz sine wave			60		dB
	0.1dB large-signal bandwidth (Note 1) –3dB small-signal gain bandwidth product (Note 2)			200 1.5		KHz MHz
	Response time to gain-switching			5		µsec
	Maximum gain error				.05	dB

Note(s): 1. The -0.1dB large signal (7.5Vp-p) bandwidth of the chip when driving 600Ω parallel with 100pF and for a gain of 25.5dB.
2. The -3dB small signal (100mVp-p) gain-bandwidth when driving 600Ω parallel with 100pF load.

AC ELECTRICAL CHARACTERISTICS (Line Equalizer section)

(T_A = 0–70°C, V_{CC} = +5 V ±10%, V_{SS} = –5 V ±10%, V_{IN} = –7dBm, 1 KHz sinusoid $C_{CRYSTAL\ FREQ}$ = 3.579 MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Slope Response	1KHz response BW3 - BW0 = 0000 HT3 - HT0 = 0000 L/NL SL3 SL2 SL1 SL0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 1 1 1 1 1 0 0 0 1 1 0 0 1 0 1 0 1 0 0 1 1 0 0 0 1 1 1 1 1 Referenced to 0 0 0 0 0		 0.5 1.0 2.1 3.9 6.7 1.5 2.8 4.9 7.8 11.5		 dB dB dB dB dB dB dB dB dB dB
	Height Response	3250 Hz response referenced to 1KHz BW3 - BW0 = 0000 SL3 - SL0 = 0000 L/NL HT3 HT2 HT1 HT0 0 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0 1 1 1 1		 0 0.5 1.1 2.3 5.6 10.8		 dB dB dB dB dB dB
	Bandwidth Response	L/NL = 0 HT3 - HT0 = 1111 SL3 - SL0 = 0000 BW3 BW2 BW1 BW0 0 0 0 0 0 0 0 1 0 0 1 0 0 1 0 0 1 0 0 0 1 1 1 1		 14.4 13.0 11.6 8.6 3.3 0.9		 dB dB dB dB dB dB
	Peak Frequency			3250		Hz
ICN	Idle Channel Noise	0dB gain SL3 - SL0 = 0 BW3 - BW0 = 0 HT3 - HT0 = 0		 5		 dBrnC
PSRR	Power Supply Rejection	@1KHz and 200mVp-p SL3 - SL0 = 0 BW3 - BW0 = 0 HT3 - HT0 = 0 on Vcc on Vss		 –20 –25		 dB dB

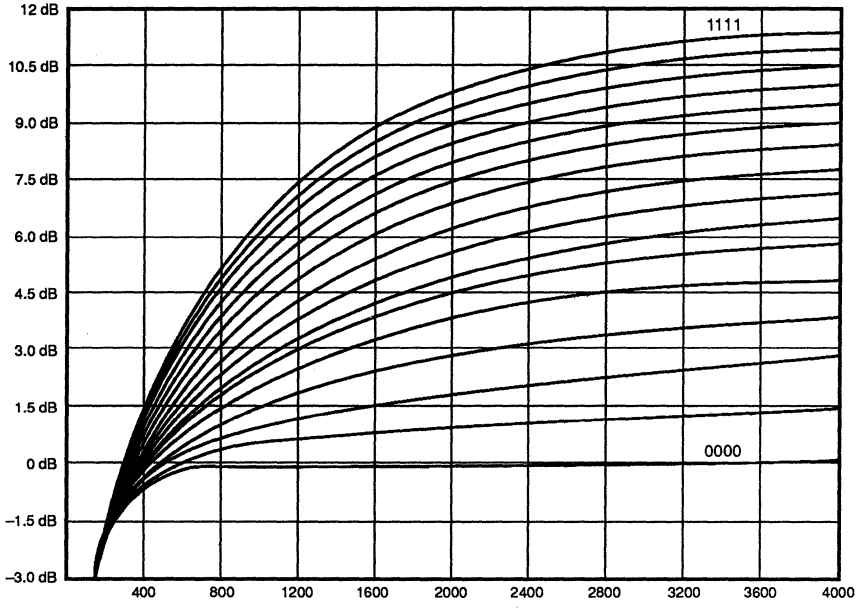


Figure 2a. Slope Filter Response

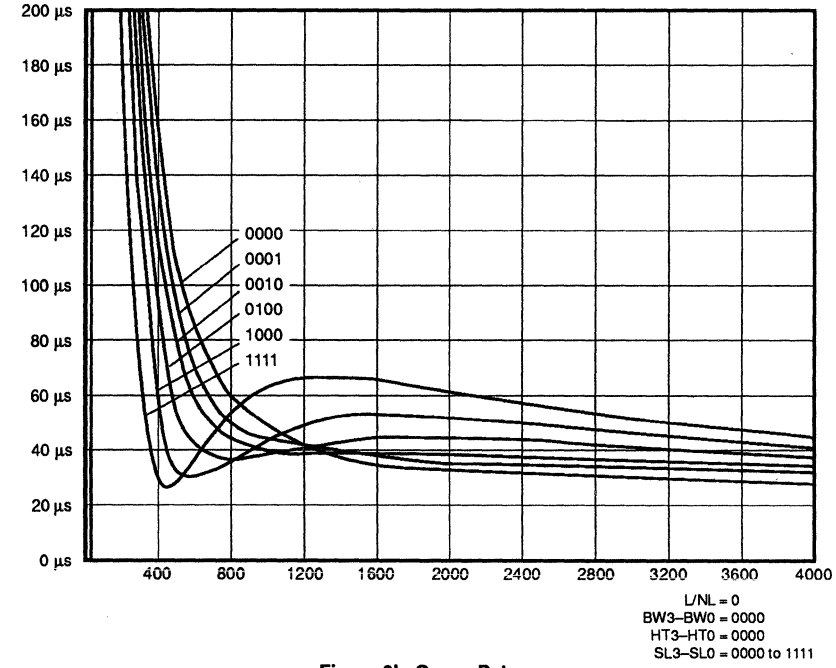


Figure 2b. Group Delay

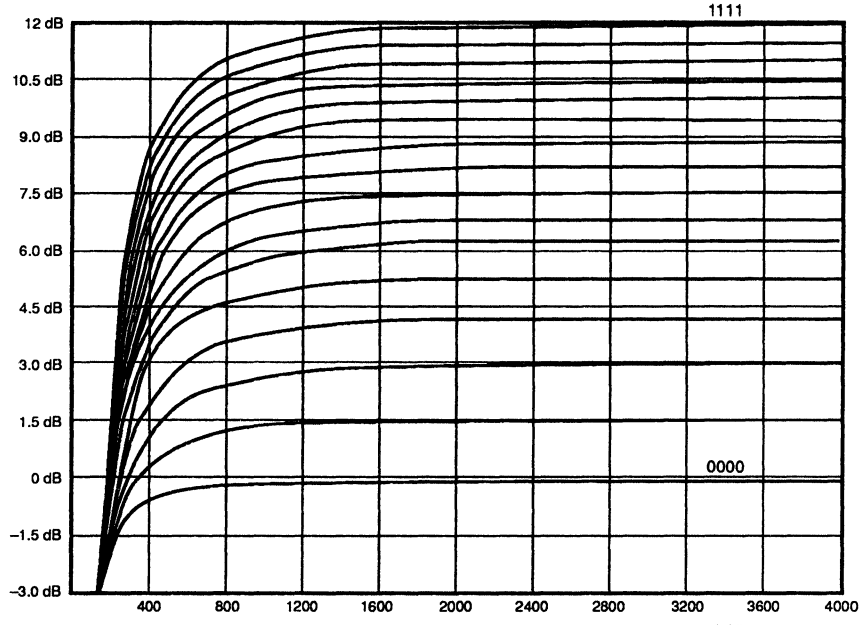


Figure 3a. Slope Filter Response

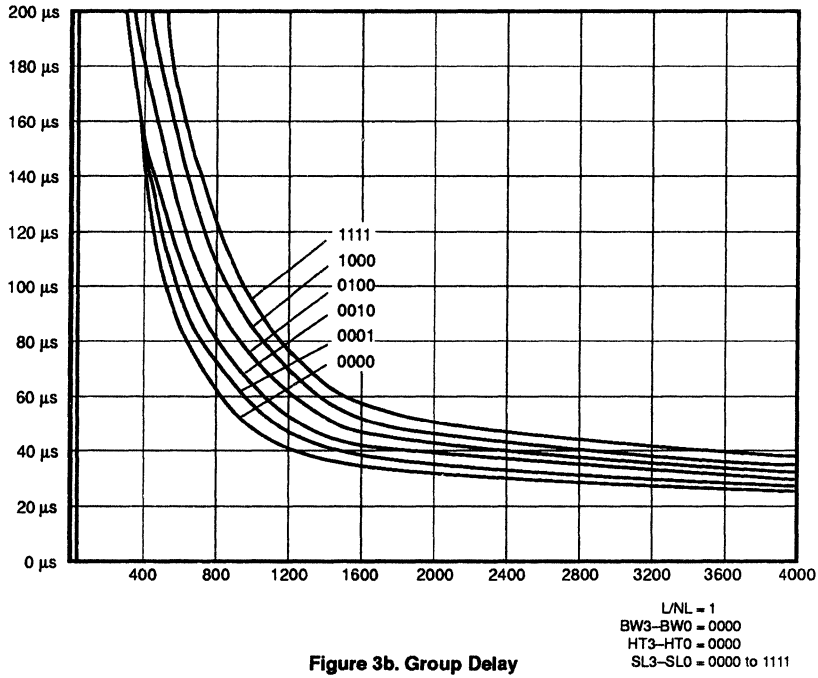


Figure 3b. Group Delay

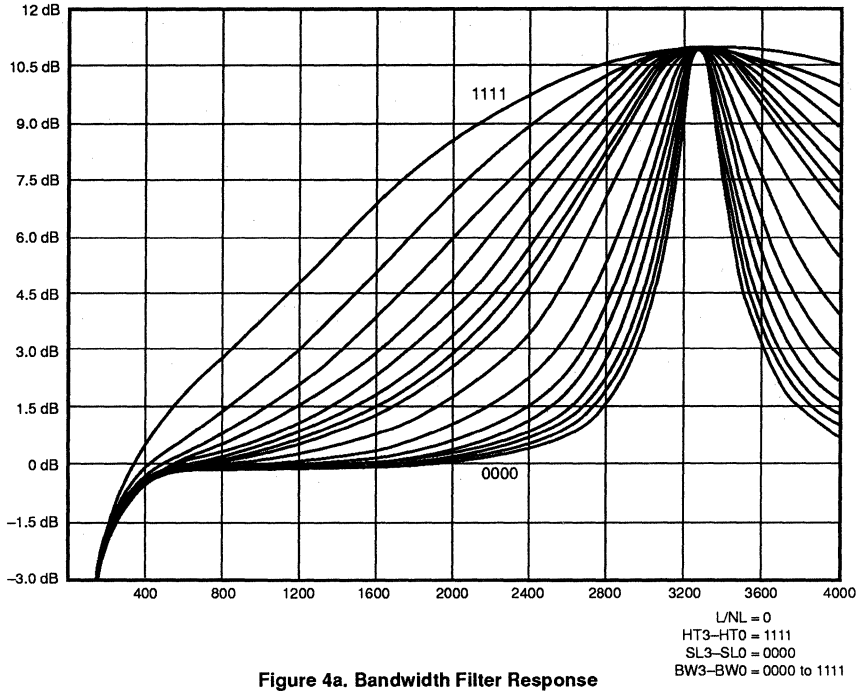


Figure 4a. Bandwidth Filter Response

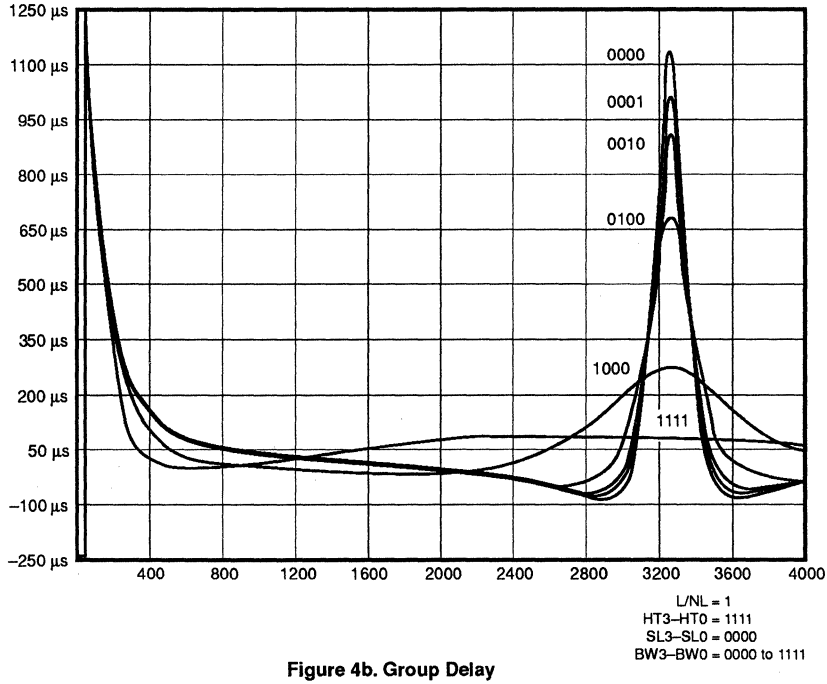


Figure 4b. Group Delay

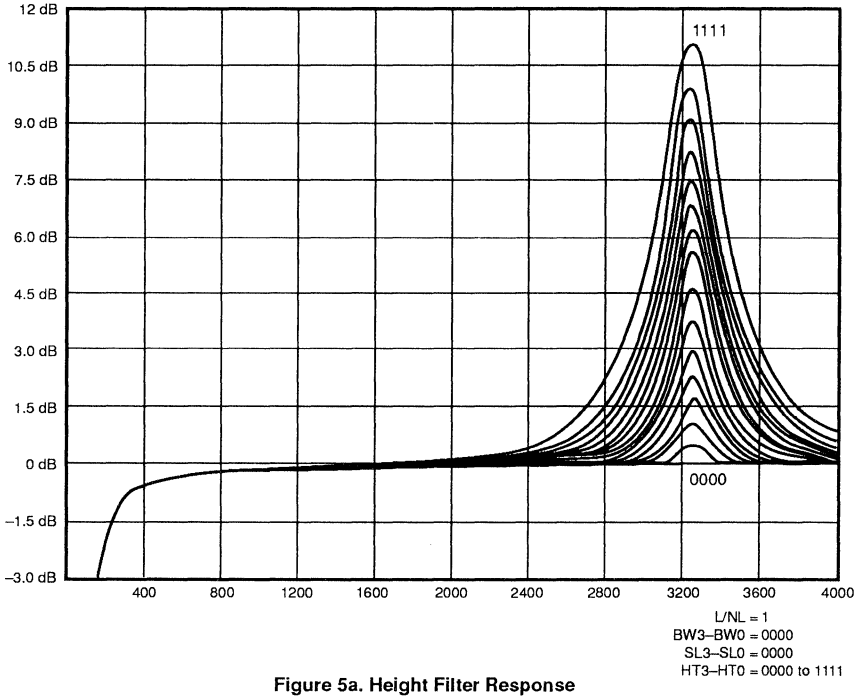


Figure 5a. Height Filter Response

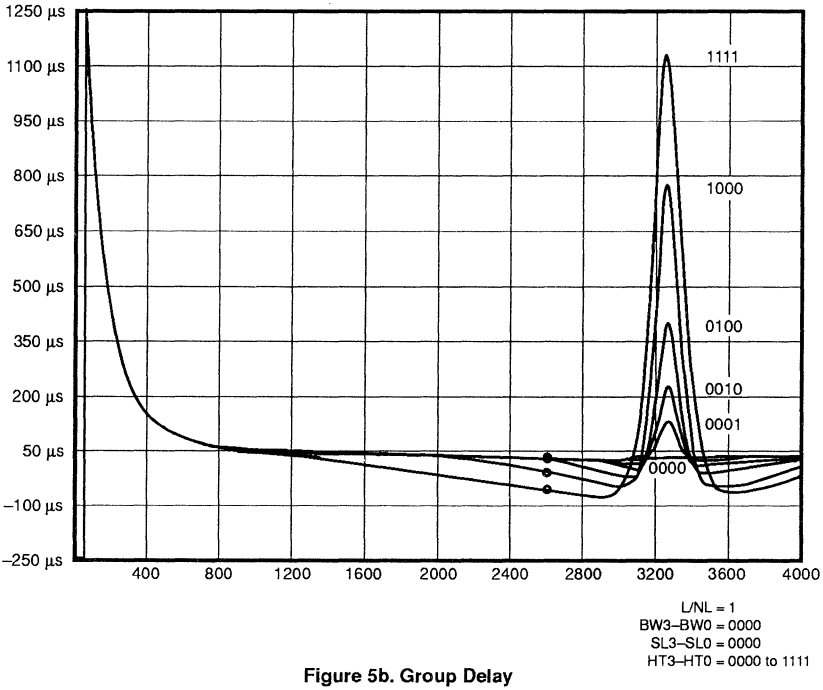


Figure 5b. Group Delay

APPLICATIONS INFORMATION

For optimum performance and lowest possible idle channel noise, it is important to decouple the power supply pins as follows:

Decouple the power supply inputs to the chip (at the pins of the chip) using a 0.1 µF ceramic in parallel with a 10 µF tantalum capacitor between V_{CC} and analog ground and between V_{SS} and analog ground at the pins of the SC11319. It is advisable to put a 10 Ω resistor between the supply voltage source and the capacitor network for V_{CC} and V_{SS}. Also, the analog and digital grounds to the chip should be tied together only at one point which is considered the lowest impedance point normally at the power supply regulator source. (See Figure 6).

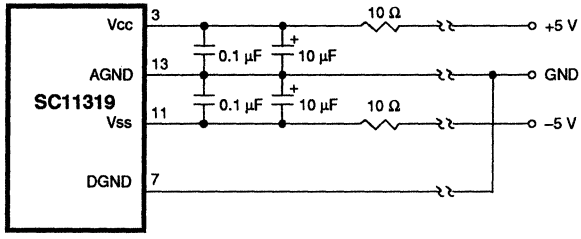
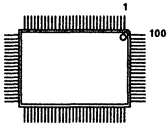


Figure 6.

FEATURES

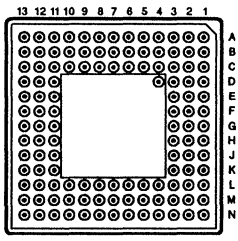
- ☐ 32 x 32 Digital crosspoint structure
- ☐ CMOS low power
- ☐ 3 ns skew, typical
- ☐ 50 MHz operation
- ☐ CMOS compatible inputs/tri-statable outputs
- ☐ Multiple package options

100-PIN QFP PACKAGE



SC11320CQ

121-PIN PGA PACKAGE
(Bottom View)

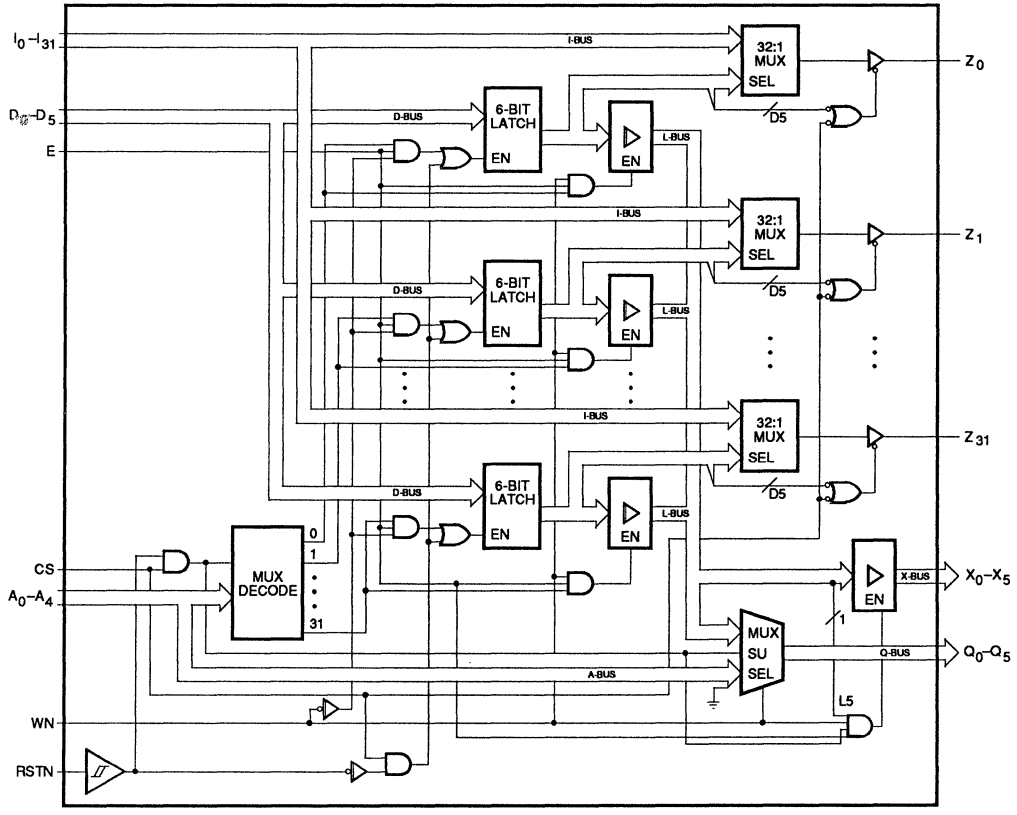


SC11320CT

GENERAL DESCRIPTION

The 32 x 32 Crosspoint Switch is a design which allows each of the 32 outputs to be independently connected to any of its 32 inputs. Thirty-two 1 of 32 muxes are employed (each with its own register which the user loads to specify the desired input for that output channel). Outputs can also be individually tri-stated by setting bit D5 low when loading these same registers. See Table 1 for pin definitions.

BLOCK DIAGRAM



I-Bus: Channel input data to be switched.
D-Bus: 32:1 MUX Register input data.
A-Bus: Address of specific latch whose contents is to be read on X-bus.
X-Bus: Permits readback of state of latch addressed via A-bus (tri-state). Only the active latch enabled by L5 (most significant bit) will be read*. *Useful in multi-chip applications.

Q-Bus: Same as X-bus. Also feeds back address of latch selected. (Defaults low/not tri-state).
Z-Bus: Channel output data.

PIN DEFINITIONS Table 1

100 Pin QFP Pad #	121 Pin PGA Pin #		Name	I/O Type	Description
100	120	A1	V_{SS}	Power	Pad ring ground.
99	119	B3	N.C.		No connection.
98	118	C4	FACTORY TEST		Float (do not ground).
N.C.	117	A2	N.C.		No connection.
N.C.	116	A3	N.C.		No connection.
97	115	B4	Z28	Output	Output channel (tri-state).
96	114	C5	Z29	Output	Output channel (tri-state).
95	113	A4	Z30	Output	Output channel (tri-state).
94	112	B5	Z31	Output	Output channel (tri-state).
N.C.	111	A5	N.C.		No connection.
N.C.	110	C6	N.C.		No connection.
N.C.	109	B6	N.C.		No connection.
N.C.	108	A6	N.C.		No connection.
N.C.	107	A7	N.C.		No connection.
93	106	C7	V_{DD}	Power	Interal logic +5.0 VDC.
92	105	B7	V_{SS}	Power	Internal logic ground.
N.C.	104	A8	MZ	Output	Not supported.
91	103	B8	D0	CMOS Input	Mux register input data (write operation).
90	102	C8	D1	CMOS Input	Mux register input data (write operation).
89	101	A9	D2	CMOS Input	Mux register input data (write operation).
88	100	B9	D3	CMOS Input	Mux register input data (write operation).
87	99	A10	D4	CMOS Input	Mux register input data (write operation).
86	98	C9	D5	CMOS Input	Register data for output tri-state control.
85	97	B10	I0	CMOS Input	Channel input data.
84	96	A11	Z0	Output	Output channel (tri-state).
83	95	B11	Z1	Output	Output channel (tri-state).
82	94	C10	Z2	Output	Output channel (tri-state).
81	93	A12	Z3	Output	Output channel (tri-state).
N.C.	92	B12	N.C.		No connection.
D.B.	91	C11	V_{SS}	Power	Pad ring ground.
80	90	A13	V_{DD}	Power	Pad ring +5.0 VDC.
79	89	C12	I1	CMOS Input	Channel input data.
78	88	D11	I2	CMOS Input	Channel input data.
77	87	B13	I3	CMOS Input	Channel input data.
76	86	C13	I4	CMOS Input	Channel input data.
75	85	D12	I5	CMOS Input	Channel input data.
74	84	E11	I6	CMOS Input	Channel input data.
73	83	D13	I7	CMOS Input	Channel input data.
72	82	E12	Z4	Output	Channel output (tri-state).
71	81	E13	Z5	Output	Channel output (tri-state).
70	80	F11	Z6	Output	Channel output (tri-state).
69	79	F12	Z7	Output	Channel output (tri-state).
68	78	F13	Z8	Output	Channel output (tri-state).
D.B.	77	G13	V_{SS}	Power	Pad ring ground.
D.B.	76	G11	V_{SS}	Power	Pad ring ground.
N.C.	75	G12	V_{DD}	Power	Pad ring +5.0 VDC.
67	74	H13	Z9	Output	Channel output (tri-state).
66	73	H12	Z10	Output	Channel output (tri-state).

100 Pin QFP Pad #	120 Pin PGA Pin #		Name	I/O Type	Description
65	72	H11	Z11	Output	Channel output (tri-state).
64	71	J13	Z12	Output	Channel output (tri-state).
63	70	J12	Z13	Output	Channel output (tri-state).
62	69	K13	I8	CMOS Input	Channel input data.
61	68	J11	I9	CMOS Input	Channel input data.
60	67	K12	I10	CMOS Input	Channel input data.
59	66	L13	I11	CMOS Input	Channel input data.
58	65	L12	I12	CMOS Input	Channel input data.
57	64	K11	I13	CMOS Input	Channel input data.
56	63	M13	I14	CMOS Input	Channel input data.
55	62	M12	I15	CMOS Input	Channel input data.
	61	L11	V_{DD}	Power	Pad ring +5.0 VDC.
D.B.	60	N13	V_{SS}	Power	Pad ring ground.
54	59	M11	X5	Output	Bit 5 of L-Bus (tri-state).
53	58	L10	Z14	Output	Channel output (tri-state).
52	57	N12	Z15	Output	Channel output (tri-state).
51	56	N11	Z16	Output	Channel output (tri-state).
50	55	M10	Z17	Output	Channel output (tri-state).
49	54	L9	I16	CMOS Input	Channel input data.
48	53	N10	I17	CMOS Input	Channel input data.
47	52	M9	A0	CMOS Input	Address for channel mux selection.
46	51	N9	A1	CMOS Input	Address for channel mux selection.
45	50	L8	A2	CMOS Input	Address for channel mux selection.
44	49	M8	A3	CMOS Input	Address for channel mux selection.
43	48	N8	A4	CMOS Input	Address for channel mux selection.
42	47	N7	V_{DD}	Power	Internal logic +5.0 VDC.
41	46	L7	X0	Output	Bit 0 of L-Bus (tri-state).
D.B.	45	M7	V_{SS}	Power	Internal logic ground.
40	44	N6	E	CMOS Input	Enable. Active high enable for read and write operations.
39	43	M6	WN	CMOS Input	Write Not. Active low write strobe.
38	42	L6	RSTN	CMOS Input	Reset Not. Active low chip reset (Schmitt trigger input).
37	41	N5	CS	CMOS Input	Chip Select. Active high enable for all operations. (Z and X outputs float when CS is low.)
36	40	M5	Q0	Output	A-Bus contents (write operation).
35	39	N4	Q1	Output	
34	38	L5	Q2	Output	
33	37	M4	Q3	Output	L-Bus contents (read operation).
32	36	N3	Q4	Output	
31	35	M3	Q5	Output	Mux register output data (read operation).
30	34	L4	X1	Output	Bit 1 of L-Bus (tri-state).
29	33	N2	X2	Output	Bit 2 of L-Bus (tri-state).
28	32	M2	X3	Output	Bit 3 of L-Bus (tri-state).
27	31	L3	VSS	Power	Pad ring ground.
	30	N1	V_{DD}	Power	Pad ring +5.0 VDC.
26	29	L2	X4	Output	Bit 4 of L-Bus (tri-state).
25	28	K3	I18	CMOS Input	Channel input data.
24	27	M1	I19	CMOS Input	Channel input data.
23	26	L1	I20	CMOS Input	Channel input data.

PIN DEFINITIONS

100 Pin QFP Pad #	120 Pin PGA Pin #		Name	I/O Type	Description
22	25	K2	I21	CMOS Input	Channel input data.
21	24	J3	I22	CMOS Input	Channel input data.
20	23	K1	I23	CMOS Input	Channel input data.
19	22	J2	Z18	Output	Channel output (tri-state).
18	21	J1	Z19	Output	Channel output (tri-state).
17	20	H3	Z20	Output	Channel output (tri-state).
16	19	H2	Z21	Output	Channel output (tri-state).
15	18	H1	Z22	Output	Channel output (tri-state).
D.B.	17	G1	V_{SS}	Power	Pad ring ground.
D.B.	16	G3	V_{SS}	Power	Pad ring ground.
N.C.	15	G2	V_{DD}	Power	Pad ring +5.0 VDC.
14	14	F1	Z23	Output	Channel output (tri-state).
13	13	F2	Z24	Output	Channel output (tri-state).
12	12	F3	Z25	Output	Channel output (tri-state).
11	11	E1	Z26	Output	Channel output (tri-state).
10	10	E2	Z27	Output	Channel output (tri-state).
9	9	D1	I24	CMOS Input	Channel input data.
8	8	E3	I25	CMOS Input	Channel input data.
7	7	D2	I26	CMOS Input	Channel input data.
6	6	C1	I27	CMOS Input	Channel input data.
5	5	C2	I28	CMOS Input	Channel input data.
4	4	D3	I29	CMOS Input	Channel input data.
3	3	B1	I30	CMOS Input	Channel input data.
2	2	B2	I31	CMOS Input	Channel input data.
1	1	C3	V_{DD}	Power	Pad ring +5.0 VDC

FUNCTIONAL DESCRIPTION

Overview

As a 32 x 32 cross-point switch, this IC's primary mission is to allow a user to independently connect any of the 32 inputs to one of its 32 outputs. The circuit must also support applications where multiple switches are placed in parallel (outputs wire-ored together) to create even larger systems.

Structure

To provide the flexible switching behavior required (no inputs blocking), 32 muxes are used (one for each output). Each of these muxes is a 32:1 type as there are 32 input channels to choose from. A six bit latch is also provided for every mux to allow the user to individually load the desired input address for each output channel. Five of the six latch bits (D0–D4) are for describing the mux input while bit D5 is reserved for enabling the channel's output driver (0=tri-state, 1=driving). As the host needs to update a mux's latch without interfering with the other outputs, a decoder using five address lines as inputs is included. To enhance in-circuit testability, the outputs of all 32 six bit latches are wire-ored to form the L-bus which can be read by the host on the X-bus tri-statable outputs. Another diagnostic output bus (the Q-bus) can relay the status of both the L-bus and the A-bus (WN=0: A-bus, WN=1: L-bus), but cannot be tri-stated.

A summary of the circuit's behavior is presented in the truth table format (Table 2). A detailed discussion of the various operational modes follows.

		Read Mode	Write Mode	Idle Mode	Reset Mode	Unselect Mode
IN	CS	H	H	H	H	L
	RSTN	H	H	H	L	H
	E	H	H	L	X	X
	WN	H	L	X	X	X
Out	Q-Bus	D0–D5	A0–A5 Q5=0	L	L	L
	X-Bus	D0–D5**	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	Z-Bus	Respective selected input**				Hi-Z

*Don't Care
**If D5=1, else Hi-Z.

Table 2. Truth Table

Idle Mode

As indicated in Table 2, the idle mode is encountered when both CS and RSTN are high but E is low. In this case, each mux uses the previously stored contents of its latch to choose an input to pass to its output. The Z-bus drivers are enabled (subject to D5 as discussed previously) while the Q-bus and the X-bus are inactive.

Reset Mode

In the case where RSTN=0, the reset mode begins. Here, all the mux latches are enabled at once (NOT CLEARED!). Depending on CS and the contents of the D-bus, the Z-bus outputs will either all reflect the state of the input specified (CS and D5=1) or all be floating (CS or D5=0). To clear the mux latches, the host must assure the presence of low inputs on the D-bus before and after the RSTN line is brought high. For in-circuit testing, the host can use this mode to exercise all 32 muxes simultaneously. Both the Q-bus and X-bus outputs are inactive while RSTN is low. A Schmitt trigger input is provided for RSTN to support the slow rise times seen when external capacitance is used for holding RSTN low during power-up.

Unselected Mode

As Table 2 suggests, the chip immediately enters the unselected mode when CS is taken low (regardless of the other control inputs). In this state, the Q-bus outputs go low while the Z-bus and X-bus float. The contents of the mux latches are not affected.

Write Mode

To modify the contents of a single mux's latch, the WN line must be low while CS, RSTN, and E are all high per Table 2. The latch selected by the A-bus is immediately loaded with the contents of the D-bus and this information is latched by the rising edge of the WN line. The E pulse must occur while WN is low for the Write operation to take place on the rising edge of WN. While WN is low, the Q-bus outputs the contents of the A-bus (A0–A4 on lines Q0–Q4, Q5 always low). It should be noted that only the selected mux's output can change during a write cycle. This insures that the other output channels can continue to pass their data independently of the operation.

Read Mode

Per Table 2, when all four of the control lines (CS, RSTN, E, WN) are high, the chip is in the read mode. During this

TIMING DIAGRAMS

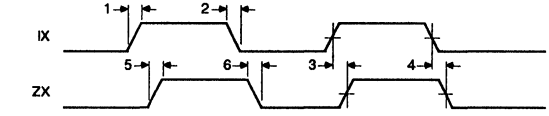


Figure 3.1 Idle

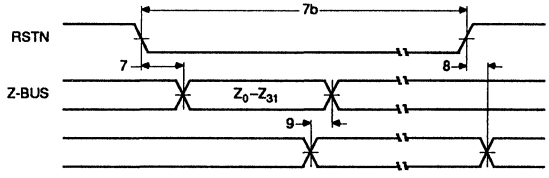


Figure 3.2 Reset

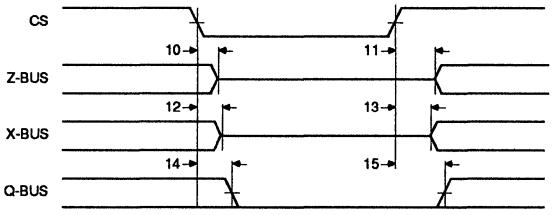


Figure 3.3 Unselected

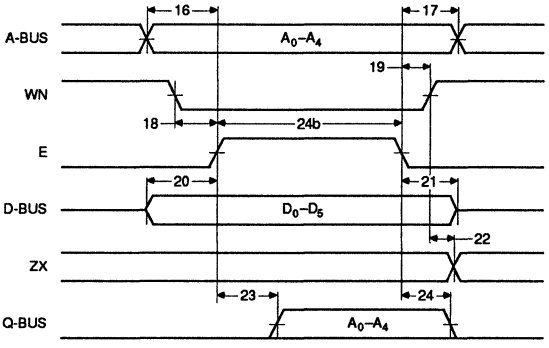


Figure 3.4 Write

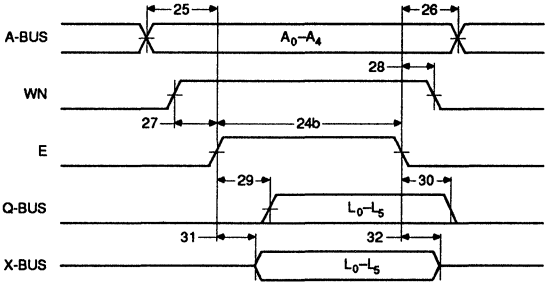


Figure 3.5 Read

time, the X-bus reflects the contents of the L-bus if L5 is high, otherwise the X-bus floats. Meanwhile, the Q-bus also displays the L-bus status but without regard to L5.

Expandability for the SC11320

In order to expand the SC11320 to larger Cross-Point-Switches, it must be configured such that any input can be multiplexed to any output. Figure 4 is an example of a 64 X 64 Cross-Point-Switch. The top two SC11320's (1 & 2) correspond to the first 32 outputs and the bottom two SC11320's (3 & 4) to the last 32 outputs. The SC11320's on the left (1 & 3) correspond to the first 32 inputs, and the two SC11320's on the right (2 & 4) to the last 32 inputs. All like outputs are then joined to form the Z and Q output busses. The four SC11320's are connected in such a way that only one or none of the outputs will drive any of the 64 Z channels at a time. This will prevent contention on the Z bus.

The D5 input is still the disable input for the Z outputs. The D6 input specifies which set of I inputs to multiplex through to the Z outputs. When D6 is LOW, the first 32 I inputs are selected; and when D6 is HIGH, the second 32 I inputs are selected.

The A5 input selects between the first 32 control latches and the second 32 control latches when the device is in the READ or WRITE mode. This is done by gating A5 with the E and WN signals of each SC11320. To keep the deselected SC11320's from accidentally WRITING data into the control latches, the A5 input is gated with both the E and WN signals. This will prevent any internal race conditions between the E and WN signals.

In this example, the CSn and RSTNn signals are all separate inputs. This is not necessary for the expansion of the SC11320 and is system dependent. The In, Dn and An inputs, and the Zn and Qn outputs must stay in this format in order to maintain correct functionality of a Cross-Point-Switch.

The gating needed to perform this expansion is minimal (8 gates), and can be done on or off chip. Further expansion can be accomplished using the same technique.

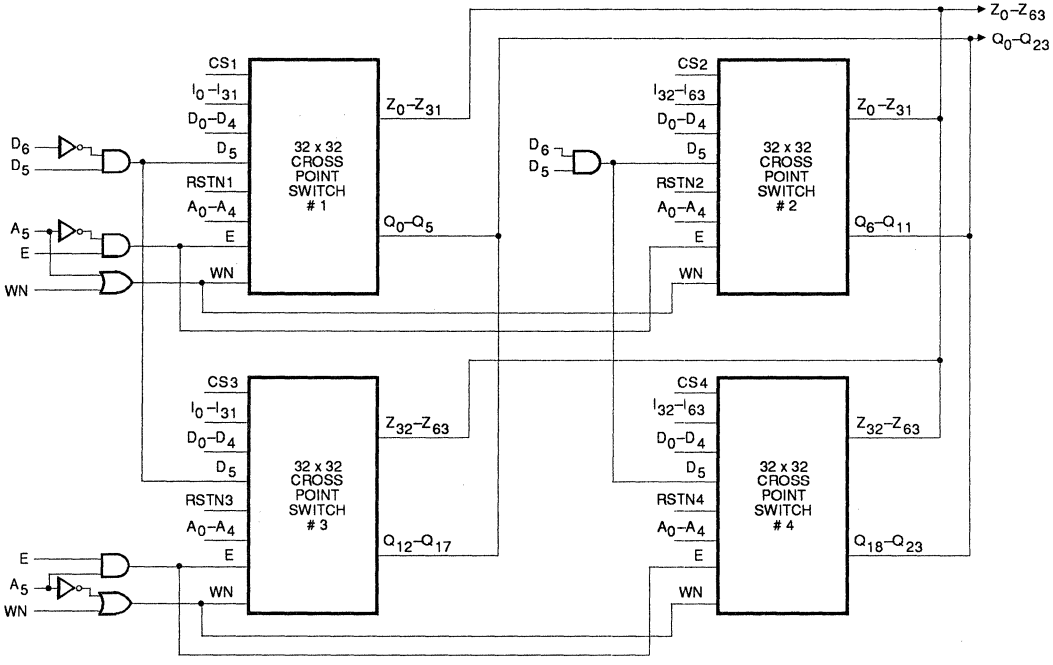


Figure 4. Expansion to 64 x 64 Crosspoint Switch

DC OPERATING CONDITIONS

Description	Min	Typ	Max	Units	Notes
Operating Ambient Air Temperature Range	0	25	70	°C	Junction Range 0 to 85
Power Supplies					
V_{DD} Supply Voltage	4.5	5.0	5.5	V	
V_{SS} Supply Voltage	0	0	0	V	
I_{DD} Supply Current		170		mA	20 MHz
Leakage Current (all inputs & tri-state outputs)	–10		+10	µA	
Input Voltages					
Logic "0" (V_{IL}) all except RSTN			1.5	V	
Logic "1" (V_{IH}) all except RSTN	3.5			V	
Logic "0" (V_{IL}) RSTN only	1.3	1.8	2.0	V	
Logic "1" (V_{IH}) RSTN only	3.0	3.5	3.8	V	
Schmitt Trigger Hysteresis	1.0	1.7	2.0	V	
Output Voltages					
Z0–Z31					
Logic "0" (V_{OL})	V_{SS}		0.8	V	I_{OL} = +8 mA
Logic "1" (V_{OH})	V_{DD}–0.8		V_{DD}	V	I_{OH} = –8 mA
X0–X5, Q0–Q5					
Logic "0" (V_{OL})	V_{SS}		0.8	V	I_{OL} = +4 mA
Logic "1" (V_{OH})	V_{DD}–0.8		V_{DD}	V	I_{OH} = –4 mA
Input Capacitance			10	pF	w/package
Output Capacitance			10	pF	w/package
Output Loading					
Q0–Q5			20	pF	
Z0–Z31			50	pF	
X0–Z5			170	pF	

AC CHARACTERISTICS

(Refer to Figures 1.1–1.5)
(@ V_{DD}=5.0 V ±10% V_{SS}=0 V, T_A=0 to 70°C. Outputs loaded and timing measured at CMOS levels.
All input rise and fall times < 10 ns, unless otherwise specified)

No	Description	Min	Typ	Max	Units	Notes
1	I-Bus Rise Time			5	ns	Figure 3.1 (symmetry: 50/50 in 45/55 out at 50 MHz)
2	I-Bus Fall Time			5	ns	
3	Propagation Time (Rising)		25	40	ns	
4	Propagation Time (Falling)		25	40	ns	
5	Z-Bus Rise Time	4		11	ns	(with 50 pF load on Z-bus)
6	Z-Bus Fall Time	4		11	ns	
	Z-Bus Skew Time		2	4	ns	
	I-Bus Frequency			50	MHz	
7	Reset Fall to Z-Bus Change			55	ns	
7b	Reset Pulse Width	100			ns	
8	D-Bus Hold From Reset Rise	20			ns	Figure 3.2
9	D-Bus to Z-Bus Delay			40	ns	
10	CS Fall to Z-Bus Float			25	ns	
11	CS Rise to Z-Bus Driven			25	ns	(If D5 = 1) Figure 3.3
12	CS Fall to X-Bus Float			30	ns	
13	CS Rise to X-Bus Driven			30	ns	(If D5 = 1)
14	CS Fall to Q-Bus Low			40	ns	
15	CS Rise to Q-Bus Enabled			50	ns	
16	A-Bus Setup Before E Rise	50			ns	
17	A-Bus Hold After E Fall	20			ns	Figure 3.4
18	WN Setup Before E Rise	50			ns	
19	WN Hold After E Fall	20			ns	
20	D-Bus Setup Before E Rise	50			ns	
21	D-Bus Hold After E Fall	20			ns	
22	WN Rise to Zx Change			85	ns	
23	E Rise to Q-Bus Active			40	ns	(A0–A4, 0)
24	E Fall to Q-Bus Low			35	ns	
24b	E Pulse Width	20			ns	
25	A-Bus Setup Before E Rise	50			ns	
26	A-Bus Hold After E Fall	50			ns	Figure 3.5
27	WN Setup Before E Rise	50			ns	
28	WN Hold After E Fall	20			ns	
29	E Rise to Q-Bus Active			55	ns	
30	E Fall to Q-Bus Low			35	ns	(L0–L5)
31	E Rise to X-Bus Active			85	ns	(L0–L5)
32	E Fall to X-Bus Float			30	ns	

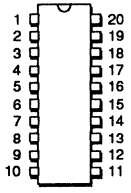
MECHANICAL SPECIFICATION

Package
121 pin grid array (plastic, one locating pin)

FEATURES

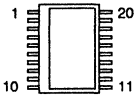
- ☐ Mask programmable switched-capacitor filter sections to obtain different filter responses including high-pass, low-pass, band-pass, notch, and all-pass types.
- ☐ Mask programmable filter clock frequency.
- ☐ Two uncommitted operational amplifiers available for use as anti-aliasing and/or smoothing filters.
- ☐ Low power consumption.
- ☐ 20-pin DIP/20-pin SOIC
- ☐ Emulation with (E^2) PROM pin compatible part (SC22324/2)

20-PIN DIP PACKAGE



SC11324CN
SC11322CN

20-PIN SOIC PACKAGE

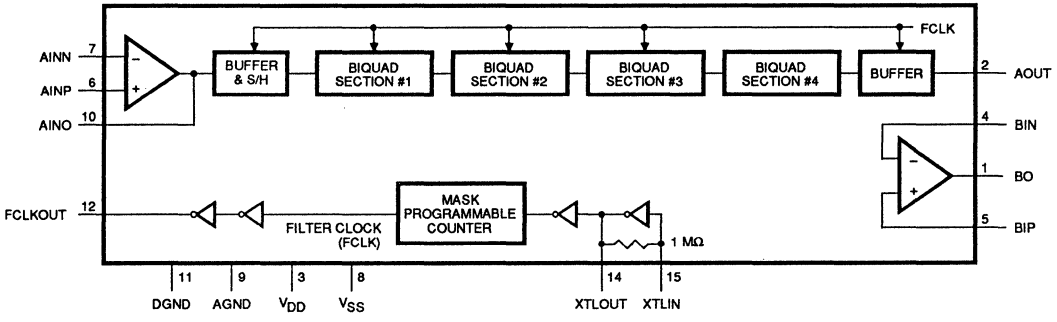


SC11324CM
SC11322CM

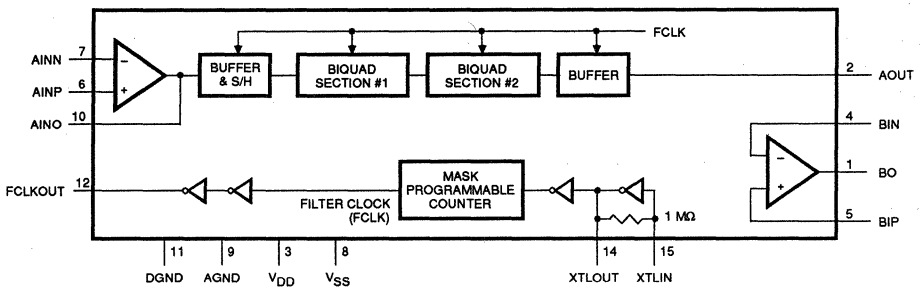
GENERAL DESCRIPTION

The SC11324/2 are CMOS quad/dual second-order mask programmable universal switched-capacitor filters. They are mask programmed to provide a variety of combinations of high-pass, low-pass, band-pass, notch and all-pass filter functions without a need for any external components. The device can be cascaded to provide higher order filter function. The clock for the filters is provided from an on-chip oscillator that needs an external crystal, and a mask programmable digital counter. The SC11324/2 are supported by easy to use development tools and design software to assist the implementation of the required filter responses. Both devices are fabricated in a CMOS process and are available in a 20-pin DIP/20-pin SOIC.

BLOCK DIAGRAM



SC11324 Block Diagram



SC11322 Block Diagram

PIN DESCRIPTIONS

PIN NO.	PIN NAME	FUNCTION
1	BO	Uncommitted op amp output.
2	AOUT	Analog output of programmable filter.
3	V_{DD}	Positive power supply pin. V_{DD} = +5 V ±10%
4	BIN	Uncommitted op amp negative input.
5	BIP	Uncommitted op amp positive input.
6	AINP	Uncommitted op amp positive input.
7	AINN	Uncommitted op amp negative input.
8	V_{SS}	Negative power supply pin. V_{SS} = –5 V ±10%
9	AGND	Analog ground. All analog signals are referenced to this pin.
10	AINO	Uncommitted op amp output node.
11	DGND	Digital ground. All digital signals are referenced to this pin.
12	FCLKOUT	Filter clock out. Buffered filter clock output.
13	NC	
14	XTLOUT	Crystal oscillator output pin. XTLOUT and XTLIN connect to a crystal to generate a crystal locked clock for the chip. If a suitable clock is already available in the system the XTLIN pin can be driven.
15	XTLIN	Crystal oscillator input pin. Refer to pin 14 for details.
16–20	NC	

CHIP ARCHITECTURE

The block diagram of SC11324/2 is shown on Pages 1 & 2. Each chip consists of four/two independently programmable biquadratic sections which may be configured through mask programming to achieve filter responses of 8th/4th order or less. Each chip has an uncommitted operational amplifier (op amp) at the input to facilitate implementation of an anti-aliasing section to eliminate aliasing effects in the subsequent switched-capacitor filters. The output of the op amp is followed by a buffer section that acts as a sample-and-hold (S/H) stage. The buffer feeds the signal to the biquad stages. The four/two biquad sections can be configured as one, two, three or four, (one or two for SC11322), cascaded sections. The output of the last cascaded stage is connected to an output buffer which drives the output pin. Provided at the output is another uncommitted op amp that can be used to implement a smoothing filter used for removing the clock noise from the output signal. The clock for the filter is supplied from an on-chip oscillator and mask programmable counter that need an external crystal.

The total number of bits for mask programming the SC11324/2 is 246/128. Two bits determine the number of BiQUAD sections used on the particular application and eight additional bits are required to set the counter divide ratio. Each BiQUAD needs 59 bits of programming, four of which are decoded to set the filter type. The other 55 bits correspond to the five Z-Domain transfer function coefficients.

After the filter response is optimized with the use of a pin compatible E^2PROM device SC22324/2, the coeffients file can be transfered to Sierra Semiconductor for coding and generation of the SC11324/2 programming mask.

SC11324/2 are available in 20-pin DIP and 20-pin SOIC and they use a ±5 V power supply for operation.

BIQUAD SECTIONS

Each biquad filter section can be programmed to achieve band-pass, low-pass, low-pass notch, high-pass, high-pass notch, notch, and all-pass filter responses. Any combination of these sections can be combined to form 2nd, 4th, 6th or 8th order filters (2nd and 4th order for SC11322). The block diagram of the biquad is shown in Fig.1. Each biquad section can be configured into one of the sixteen possible types. Table 1 shows the filter name and the corresponding filter type. The z- domain transfer functions of all sixteen biquad types are given in Table 2, where V1 and V2 are the outputs of first and second op amps shown in Fig. 1. Each of the five coefficients that define the filter transfer function is made up of eleven bits.

Between one and four BIQUADs (one and two for 11322) can be selected as shown in Figure 2.

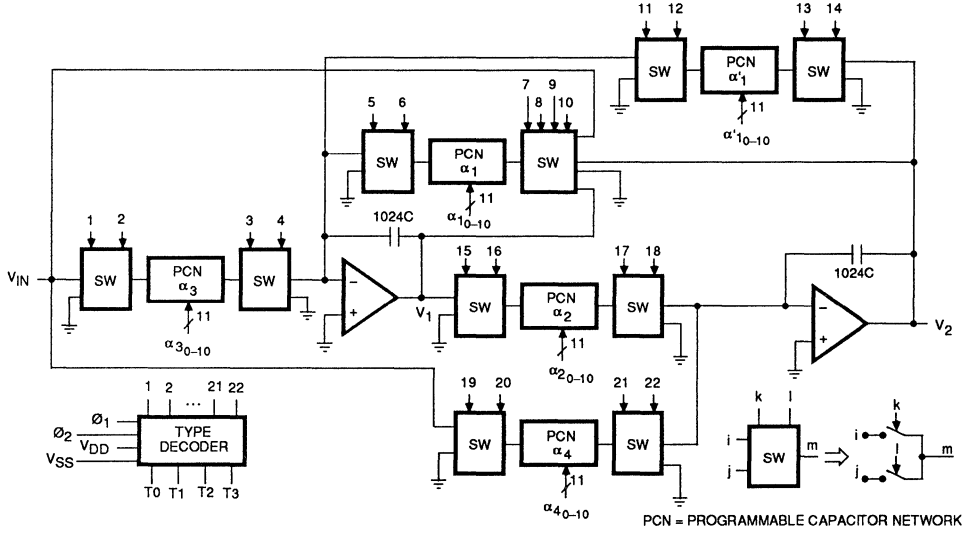


Figure 1. Mask Programmable Biquad Block Diagram (One Second-Order Section)

NAME	FILTER TYPE
N1	Notch Type I
HP1	High-pass Type I
BP1	Band-pass Type I
LP1N	Low-pass Type I Noninverting
LP1I	Low-pass Type I Inverting
BP2N	Band-pass Type II Noninverting
BP2I	Band-pass Type II Inverting
N2	Notch Type II
HP2	High-pass Type II
BP3	Band-pass Type III
LP2N	Low-pass Type II Noninverting
LP2I	Low-pass Type II Inverting
BP4N	Band-pass Type IV Noninverting
BP4I	Band-pass Type IV Inverting
BP5	Band-pass Type V
AP	All-pass

Table 1. Mask Programmable Biquad Types

FILTER TYPE	z DOMAIN TRANSFER FUNCTION
N1	$H(z) = \frac{V_2}{Vin} = -\alpha_4\left[1 + \left(\frac{\alpha_2\,\alpha_3}{\alpha_4} - 2\right) z^{-1} + z^{-2}\right] / D_1(z)$
HP1	$H(z) = \frac{V_1}{Vin} = -\left[\alpha_3\,(1 - z^{-1})^2\right] / D_1(z)$
BP1	$H(z) = \frac{V_2}{Vin} = \left[-\alpha_2\,\alpha_3\,z^{-1}\,(1 - z^{-1})\right] / D_1(z)$
LP1N	$H(z) = \frac{V_2}{Vin} = \alpha_2\,\alpha_3\,z^{-2} / D_1(z)$
LP1I	$H(z) = \frac{V_2}{Vin} = -\alpha_2\,\alpha_3\,z^{-1} / D_1(z)$
BP2N	$H(z) = \frac{V_1}{Vin} = \alpha_3\,z^{-1}\,(1 - z^{-1}) / D_1(z)$
BP2I	$H(z) = \frac{V_1}{Vin} = -\alpha_3\,(1 - z^{-1}) / D_1(z)$
N2	$H(z) = \frac{V_2}{Vin} = \left(\frac{-\alpha_3}{1+\alpha_1}\right)\left[1 + \left(\frac{\alpha_1'\,\alpha_4}{\alpha_3} - 2\right) z^{-1} + z^{-2}\right] / D_2(z)$
HP2	$H(z) = \frac{V_1}{Vin} = \left(\frac{-\alpha_3}{1+\alpha_1}\right)(1 - z^{-1})^2 / D_2(z)$
BP3	$H(z) = \frac{V_2}{Vin} = \left(\frac{-\alpha_2\,\alpha_3}{1+\alpha_1}\right) z^{-1}(1 - z^{-1}) / D_2(z)$
LP2N	$H(z) = \frac{V_2}{Vin} = \frac{\alpha_2\,\alpha_3}{1+\alpha_1} z^{-2} / D_2(z)$
LP2I	$H(z) = \frac{V_2}{Vin} = -\frac{\alpha_2\,\alpha_3}{1+\alpha_1} z^{-2} / D_2(z)$
BP4N	$H(z) = \frac{V_1}{Vin} = \frac{\alpha_3}{1+\alpha_1} z^{-1}(1 - z^{-1}) / D_2(z)$
BP4I	$H(z) = \frac{V_1}{Vin} = \frac{-\alpha_3}{1+\alpha_1}(1 - z^{-1}) / D_2(z)$
BP5	$H(z) = \frac{V_1}{Vin} = \frac{-\alpha_3}{1+\alpha_1}(1 - z^{-1})(1 + z^{-1}) / D_2(z)$
AP	$H(z) = \frac{V_1}{Vin} = \frac{-1}{1+\alpha_1}\left[1 + \left(\alpha_1'\,\alpha_4 - \alpha_1 - 2\right) z^{-1} + (1 + \alpha_1) z^{-2}\right] / D_2(z)$
	$D_1(z) = 1 + \left(\alpha_1'\,\alpha_2 + \alpha_1\,\alpha_2 - 2\right) z^{-1} + (1 - \alpha_1\,\alpha_2) z^{-2}$
	$D_2(z) = 1 + \left(\frac{\alpha_1'\,\alpha_2 - \alpha_1 - 2}{1+\alpha_1}\right) z^{-1} + \left(\frac{1}{1+\alpha_1}\right) z^{-2}$

Table 2. Biquad Filter Transfer Functions

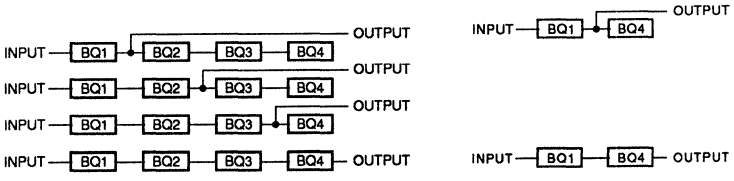


Figure 2. Number of Biquad Sections

PROGRAMMABLE COUNTER

The filter clock is derived from an on-chip oscillator and a programmable counter. The counter is shown in Figure 3. The mask programmable divide ratios to genertate a filter clock from the oscillator clock are shown in Table 3.

DIVIDE RATIO
510
508
506
•
•
4
2
1

Table 3. Mask Programmable Counter Divide Ratios Versus Control Codes

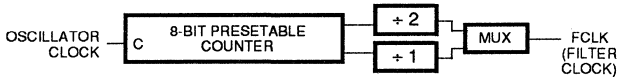


Figure 3. Programmable Counter

FILTER DESIGN SOFTWARE

Sierra provides a software program (BiQUAD) to help speed the transition from frequency design requirements to working hardware. This program will run on a personal computer and is composed of:

A routine that will calculate the number of sections weeded, the quadratic factors of the transfer function and includes a subroutine to equalize the group delay.

A routine that uses the coeffecient of the quadratic factors to select the type and calculates the capacitor values of each second order filter section. It plots the frequency response with the quantized capacitor values.

A routine to program the coefficient filter type and clock divider constants into a SC22324/22322 with a personal computer.

DESIGN PROCEDURE

The SC11324 and SC11322, with Sierra's filter design software, greatly simplfy the design procedure for active filters. Most designs can be realized using the four step process described in this section.

Step 1: Filter Design. Start with the program "BiQUAD" to determine the type and order of the filter needed. The program plots the frequency response and generates the quadratic factors of the filter transfer function. A crystal frequency and filter clock frequency must also be selected.

Step 2: Generate Programming Data. Start with the quadratic factors and the crystal and filter clock frequencies obtained in Step 1, use the program "BiQUAD" to generate the clock divide ratio and the coefficients which program each second order section.

Step 3: Loading an SC22324/2. When the clock divide ratio, the type and capacitor values of each second order filter section are determined, a SC22324/2 can be programmed and operated. The program "FP" loads data into the device via a personal computer serial port and an interface board. This program may be used with or without Sierra's other filter design software.

Step 4: Creating a Database for production parts. Once the filter design is complete and verified with a SC22324/2, the "coefficient output file" and crystal frequency used in the design can be sent to Sierra Semiconductor for generation of the programming mask necessary to realize the filter response desired.

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS} –0.6 to V_{DD} +0.6 V
DC Input Voltage (Digital Signals)	V_{SS} –0.6 to V_{DD} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 sec)	300°C

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
XTLIN,XTLOUT	Crystal Frequency				15	MHz
T_R, T_F	Input Rise or Fall Time	All Digital Inputs			50	ns
V_I	Analog Input Voltage		–3.0		+3.0	V

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—
Plastic package: –12mW/°C from 65° to 85°C

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = +5 V ±10%, V_{SS} = –5 V ±10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current			25		mA
I_{SS}	Quiescent Current			25		mA
V_{IH}	High Level Input Voltage		2.2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Output (I_{OL} = 1.6 mA)				0.6	V

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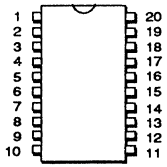
SIERRA SEMICONDUCTOR

SC11327
Programmable Frequency Synthesizer (PFS)

FEATURES

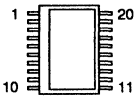
- ☐ Output frequencies up to a maximum of 100 MHz.
- ☐ High resolution frequency synthesis.
- ☐ Digitally programmable high resolution phase locked frequency.
- ☐ 20-pin DIP or 20-pin SOIC.
- ☐ Dynamically programmable frequency.
- ☐ Microprocessor compatible serial digital interface.
- ☐ Internal mask programmable ROM for fixed frequency configuration.

20-PIN DIP PACKAGE



SC11327CN

20-PIN SOIC PACKAGE



SC11327CM

GENERAL DESCRIPTION

The SC11327 is a CMOS Frequency Synthesizer. This part utilizes two 14-bit programmable Counters, an on chip oscillator (which requires an external crystal), a voltage-controlled oscillator and a phase detector to generate a 1 MHz to 100 MHz clock. The SC11327 is digitally programmed through a serial interface to provide clock frequencies with an accuracy of 14-bits. The device can be implemented in a fixed configuration with the counter divide ratios stored in a mask programmable on-chip ROM. In a microprocessor based system, it can be dynamically programmed to the application requirement. The SC11327 is available in both 20-pin DIP and 20-pin SOIC packages.

BLOCK DIAGRAM

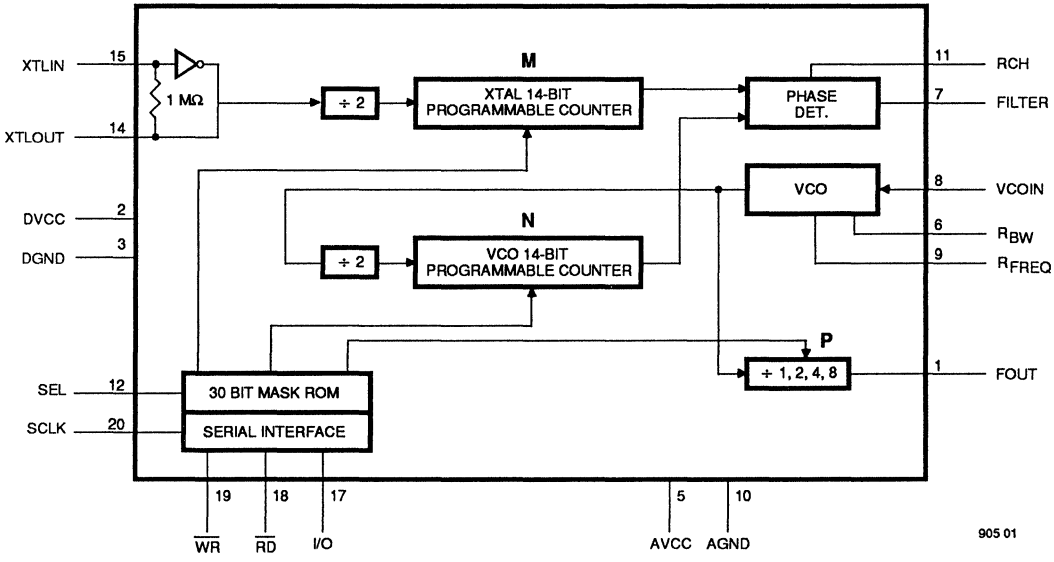


Figure 1.

PIN DESCRIPTION

PIN NO.	PIN NAME	FUNCTION
1	FOUT	Voltage controlled oscillator output.
2	DVcc	Digital power supply.
3	DGND	Digital ground.
4		Not used.
5	AVcc	Analog power supply.
6	R_{BW}	Resistor to set VCO bandwidth (driven by VCOIN).
7	FILTER	Phase locked loop filter.
8	VCOIN	Input of VCO.
9	RFREQ	Resistor to set VCO free running frequency (R_{FREQ}).
10	AGND	Analog ground.
11	RCH	Resistor to set the charge pump current (1.25 V).
12	SEL	Mode select pin. For SEL = High, source of divide ratios is mask programmable ROM. For SEL = Low, source of divide ratios is internal registers.
13		Not used.
14	XTLOUT	Crystal oscillator output pin. XTLOUT and XTLIN connect to a crystal to generate a crystal locked clock for the chip. If a suitable clock is already available in the system the XTLIN pin can be driven.
15	XTLIN	Crystal oscillator input pin.
16		Not used.
17	I/O	Serial interface input/output.
18	$\overline{RD}$	Serial interface read signal. During low period of this signal the data in the internal shift register is shifted out through the I/O pin.
19	$\overline{WR}$	Serial interface write signal. During low period of this signal the data is shifted in the internal shift register from the I/O pin.
20	SCLK	Serial interface clock signal.

FUNCTIONAL DESCRIPTION

Chip Architecture

The block diagram of the SC11327 is shown on Page 1 Fig. 1. It consists of two programmable 14-bit dividers, a crystal oscillator, a Phase-Locked Loop (PLL) system, a serial microprocessor interface, a metal mask programmable ROM and a Post-scaler 2 bit divider. The two 14-bit programmable counters divide the outputs of the oscillator and VCO by "M" and "N" respectively, where "M" and "N" are two integer numbers in the range of 1 to 16,383. The divided outputs are phase-locked to each other by the PLL circuit. The output of the VCO is then divided by the post-scaler modulo "P", where "P" can have a value of 1, 2, 4 or 8. For operation in the range between 1 and 10 MHz the post scaler is required. Above 10 MHz, the post scaler can be used to improve the jitter performance. The output frequency, F_{OUT}, can be calculated as follows:

$F_{OUT} = F_{VCO}/P$
$= [N/(M \times P)] \times F_{OSC}$

F_{VCO} = VCO Frequency

F_{OSC} = Oscillation frequency

M , N range from 1 to 16,383 and P = 1, 2, 4 or 8.

The M and N counters need 16 bits for programming (two bits of address and 14 bits of data), and the P-scaler needs 2 bits. These bits can be loaded into the registers that can be addressed through the four pin serial interface. The M, N and P values stored in the metal mask programmable ROM may be selected insted of using the serial interface.

Circuit Description

Phase-Locked Loop (PLL) Circuit

The PLL circuit consists of a voltage controlled oscillator (VCO), a phase detector circuit, a charge-pump and an external loop-filter. The VCO center frequency and bandwidth are determined by the two external resistors R_{FREQ} and R_{BW}, respectively. V_{VCOIN} represents the VCO input voltage from the loop-filter.

Choosing suitable R_{FREQ} and R_{BW} (bandwidth) values can be accomplished using several different iterative methods. Below are several defining equations and one method for choosing R_{FREQ} and R_{BW}. Note that F_{VCO} is the input frequency of the post-scaler. In general, F_{VCOMIN} should be greater than 10 MHz, F_{VCOMAX} should be less than 100 MHz and F_{VCOMAX}/F_{VCOMIN} should not exceed EQ. 3, which can range typically from 1 to 3.

The PLL incorporates phase/frequency detector (PFD) logic. A charge pump is used to convert the logic states of the PFD into analog signals suitable for controlling the

DEFINING EQUATIONS:

EQ. 1

$$I_{BIAS} = \frac{V_{VCOIN}}{R_{BW}} + \frac{2.2V}{R_{FREQ}}$$

V_{VCOIN} typically can range from 1V to 3V; 2V is nominal.

EQ. 2

$$F_{VCO} = \frac{1000}{\frac{4400}{I_{BIAS}} + 3}$$

EQ. 3

$$\frac{F_{VCOMAX}}{F_{VCOMIN}} = \frac{V_{VCOMAX} + 2.2\frac{R_{BW}}{R_{FREQ}}}{V_{VCOMIN} + 2.2\frac{R_{BW}}{R_{FREQ}}}$$

Outlined below is a method for calculating R_{FREQ} and R_{BW} using EQ. 1 and EQ. 2.

Step 1. Choose the desired F_{VCOMIN} and F_{VCOMAX}.

Step 2. Calculate $I_{BIASMIN}$ and $I_{BIASMAX}$ using EQ. 4 and EQ.5.

EQ. 4
$$I_{BIASMIN} = \frac{4400}{\frac{1000}{F_{VCOMIN}} - 3}$$

EQ. 5
$$I_{BIASMAX} = \frac{4400}{\frac{1000}{F_{VCOMAX}} - 3}$$

Step 3. Calculate R_{BW} by using EQ. 6 and subtracting $I_{BIASMAX}$ from $I_{BIASMIN}$.

EQ. 6
$$R_{BW} = \frac{V_{COMAX} - V_{COMIN}}{I_{BIASMAX} - I_{BIASMIN}} = \frac{3V - 1V}{\Delta I_{BIAS}}$$

Step 4. Calculate R_{FREQ} using EQ. 7.

EQ. 7
$$R_{FREQ} = \frac{2.2V}{I_{BIASMAX} - \frac{3V}{R_{BW}}}$$

R_{BW} in MΩ , I_{BIAS} in μA

Step 5. If either R_{FREQ} or R_{BW} is negative, then choose a smaller ΔF_{VCO} and repeat steps 1 through 4.

VCO. The charge pump current is determined by the external resistor RCH, and its value is given by:

ICH = 1.25V/RCH; RCH ~1.6 KΩ

A filter is added after the charge-pump to smooth the VCO control voltage. Figure 2 shows the complete PLL circuit. The states of the PFD are determined by the edges of the input wave-form. If the R-input (reference) phase leads the V-input (VCO) phase, then an edge of the R input sets the U (up) terminal true. The next V edge resets the U terminal false. Conversely, if V leads R, a V edge sets D (down) true and the next R edge resets D false. Both U and D can be false simultaneously, or either one alone can be true, but both can never be true simultaneously. Therefore a PFD has three allowable states at its output terminals, up (U), down (D) and neutral(N).

A typical circuit for the charge-pump and two possible loop-filters are shown in Figure 3. The loop filter consisting of the simple resistor capacitor combination has the disadvantage of having some granularity effect. Upon each cycle of the PFD, the pumping current Ip is driven into the filter impedance which responds with an instantaneous voltage jump of delta (Vc) = ICH*R2.

At the end of the charging interval, the pump current switches off and a voltage jump of equal magnitude occurs in the opposite direction. The frequency of the VCO follows the voltage steps so there will be frequency excursion. The second loop filter has an additional capacitor C3 is parallel with the R2-C2 impedance. Because of this capacitor, the VCO control voltage has a continuous ramp-like, exponential function for each pump pulse, instead of the rectangular jump that is present in the filter without the additional capacitor.

Mask Programmable ROM

For fixed frequency configuration the M, N and P divide ratios can be stored in an on-chip ROM with a custom metal mask. To access the counter divide ratios in the ROM, the SEL pin should be tied high. Contact Sierra Semiconductor for generation of a custom metal mask for ROM storage.

Serial Interface

Each counter needs 16 bits for programming, out of which 2 bits are for the destination's address and 14 are for data bits (see Table 1 and 2). The programming bits are loaded into the chip through the serial interface and are stored in the registers shown in Fig. 4.

The divider programming data is stored in the internal temporary register through a four pin serial interface. When $\overline{WR}$ goes low, sixteen bits of data are shifted serially into the chip through the I/O pin.The sixteen bits constitute fourteen bits of programming data and two bits of destination address. The data is sampled on the rising edge of the shift clock (SCLK). When $\overline{WR}$ goes high, the contents of the memory location selected by the two bit destination address is updated by the fourteen bit data. For proper operation of the interface, there has to be exactly sixteen SCLK pulses

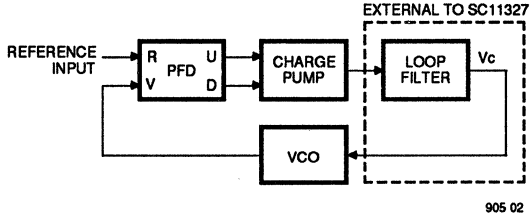


Figure 2. PLL with Three-State Phase Detector and Charge Pump

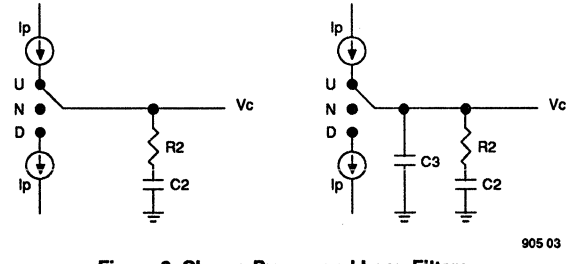


Figure 3. Charge Pumps and Loop Filters

A1	A0	DESTINATION
0	0	P (D0–D1)
0	1	N (D0-D13)
1	0	M (D0–D13)
1	1	Reserved

Table 1.

Note: When writing to the P Register D2 to D13 = 0, see Table 2 for D0, D1 values.

D1	D0	DATA
0	0	÷1
0	1	÷2
1	0	÷4
1	1	÷8

Table 2.

Note: This table is for use with the P Register only.

D13	...	D3	D2	D1	D0	DATA
0		0	0	0	0	÷1
0		0	0	0	1	÷1
0		0	0	1	0	÷2
0		0	1	0	0	÷4
						⋮
1		0	0	0	0	÷8192
	...					⋮
1		1	1	1	1	÷16383

Table 3.

Note: This table is for use with the M and N register.

within the $\overline{WR}$ high-to low and low to high transition period. After WR goes high, an additional 10 SCLK pulses are required to load the new data. Also, the first Write after a Power Up requires 10 SCLK pulses before WR goes low. After the 10 SCLK pulses, the user can read the data into the temporary register or EEPROM memory by controlling the SEL pin. Every read of a selected location should be preceded by a write into the same location. To read the data out, The $\overline{RD}$ signal should be pulled low. After sixteen clock pulses all the data inside the shift register will be clocked out of the I/O pin. The data appears at the output, on the rising edge of the shift clock (SCLK). To avoid conflicts, the falling edge of the $\overline{RD}$ signal should be at least ten SCLK periods away from the rising edge of $\overline{WR}$.

The same rule applies to consecutive write cycles. The serial interface timing diagram is shown in Figure 6 and Figure 7.

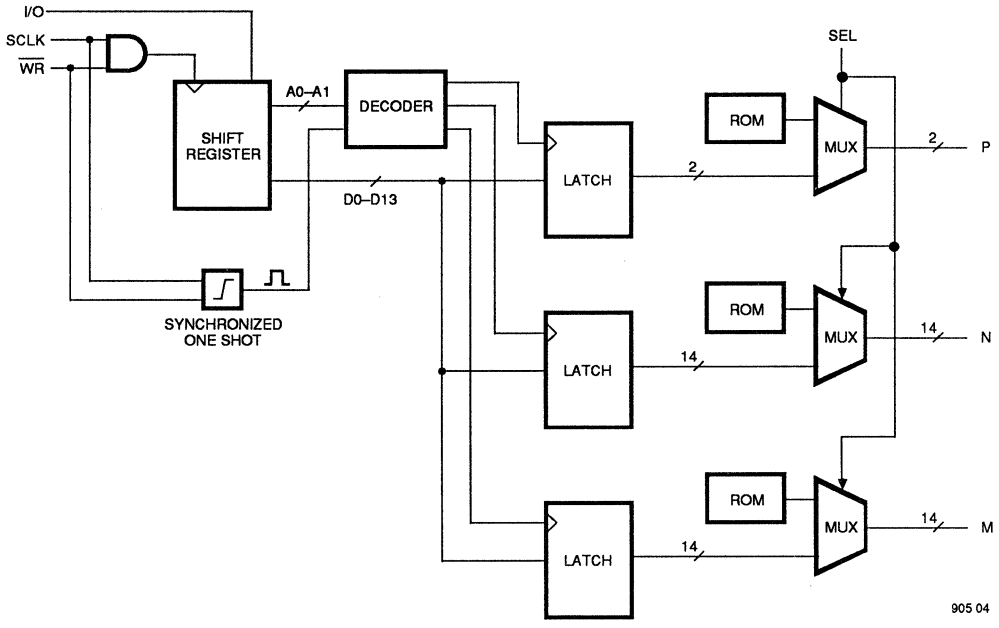


Figure 4. Storage Unit For Programming of Dividers

CRYSTAL CONNECTION

Figure 5 shows a typical crystal implementation. The capacitors C1 and C2 have a range of 20pF to 5 pF. Depending on the frequency of the crystal, it is recommended to use maximum 20 pF for frequencies lower than 10 MHz, and for frequencies above 10 MHz capacitor values between 10pF and 5 pF are recommended.

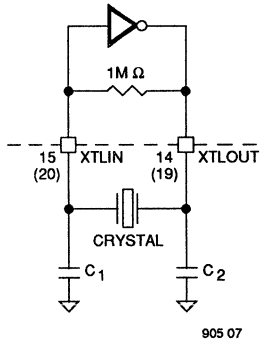


Figure 5. Typical Crystal Implementation

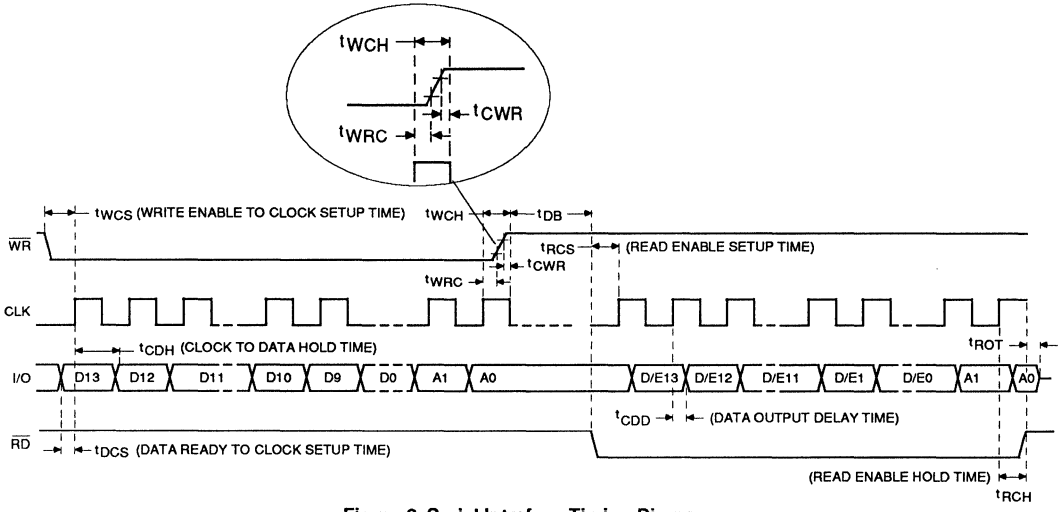


Figure 6. Serial Interface Timing Diagram

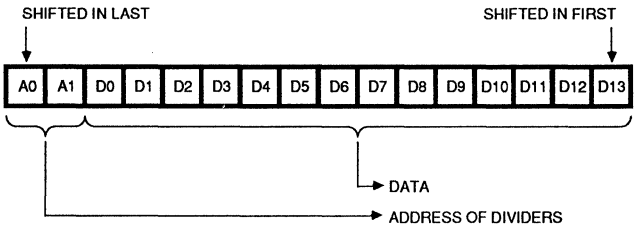


Figure 7. Address/Data Allocations for the Input Bits

SERIAL INPUT TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{WCS}	Write Enable to Clock Set Up Time	50			ns
t_{DCS}	Data Ready to Clock Set-Up Time	50			ns
t_{CDH}	Clock to Data Hold Time	50			ns
t_{CWR}	Clock to Write Enable Rising Edge	40			ns
t_{WRC}	Write Enable Rising Edge to Clock	40			ns
t_{WCH}	Clock to Write Enable Hold Time	50			ns
t_{DB}	The number of SCLK periods after Power Up, before the first Write Cycle and after aech Write Cycle	10			SCLK Periods
t_{RCS}	Read Enable to Clock Set-up Time	50			ns
t_{CDD}	Clock to Data Output Delay Time			75	ns
t_{RCH}	Clock to Read Enable Hold Time	75			ns
SCLK	Clock Frequency			5	MHz
t_{ROT}	Read Enable High to Output Tristate			50	ns

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, Vcc–GND	6 V
DC Input Voltage	GND–0.5 to Vcc +0.5 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 sec.)	300°C

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
Ta	Ambient Temperature		0		70	°C
Vcc	Positive Supply Voltage		4.5	5.0	5.5	V
GND	Ground			0		V
XTLIN, XTLOUT	Crystal Frequency			20	30	MHz
Tr,Tf	Input Rise or Fall Time				50	ns

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package –12mW/°C from 65–85°C

DC ELECTRICAL CHARACTERISTICS (Ta = 0 TO 70°C, DVcc = 5V ±10%, AVcc = 5V ±10%)

PARAM.	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
Icc	Quiescent Current			30		mA
Vih	High Level Input Voltage, All Inputs		2.2			V
Vil	Low Level Input Voltage, All Inputs				.8	V
Voh	High Level Output, All Outputs Except XTLOUT (Ioh = 0.5 mA) (Ioh = 100 µA)		 2.4 4.5			 V V
Vol	Low Level Output, All Outputs Except XTLOUT (Iol = 1.6 mA) (Iol = 100 µA)				 0.6 0.2	 V V
Voh	High Level Output XTLOUT (Ioh = 20 µA)		 4			 V
Vol	Low Level Output XTLOUT (Iol = 20 µA)				0.2	V

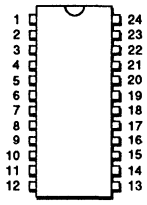
SIERRA SEMICONDUCTOR

SC11328
Programmable Frequency Synthesizer (PFS)

FEATURES

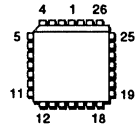
- ☐ Output frequencies up to a maximum of 100 MHz.
- ☐ High resolution frequency synthesis.
- ☐ Digitally programmable high resolution phase locked frequency.
- ☐ Dynamically programmable frequency.
- ☐ Internal mask programmable ROM for fixed frequency configuration
- ☐ Microprocessor compatible serial digital interface.
- ☐ 24-pin DIP or 28-pin PLCC.
- ☐ Pin compatible with SC22318 E^2 device

24-PIN DIP PACKAGE



SC11328CN

28-PIN PLCC PACKAGE

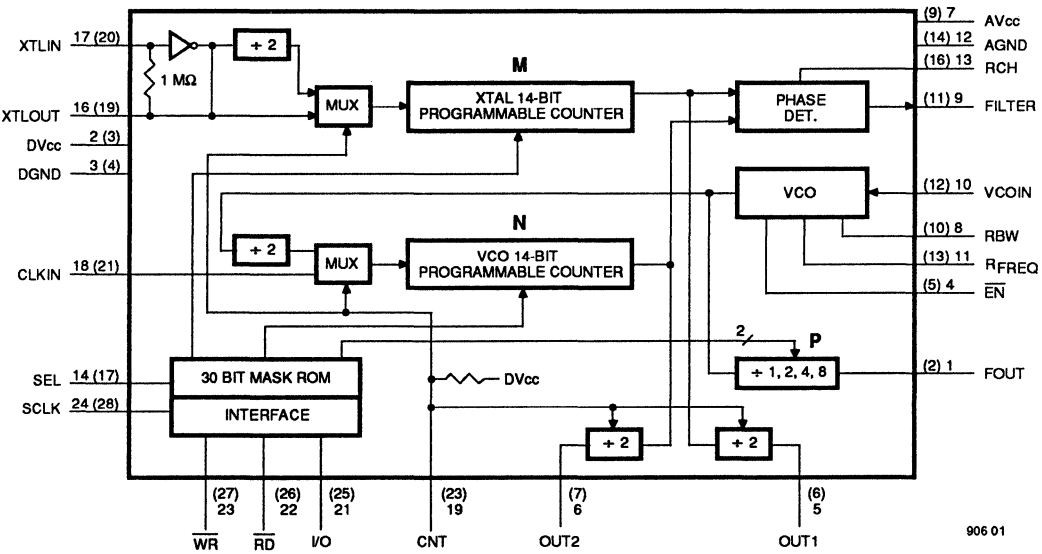


SC11328CV

GENERAL DESCRIPTION

The SC11328 is a CMOS Frequency Synthesizer. This part utilizes two 14-bit programmable Counters, an on chip oscillator (which requires an external crystal), a voltage-controlled oscillator and a phase detector to generate a 1 MHz to 100 MHz clock. The SC11328 is digitally programmed through a serial interface to provide clock frequencies with an accuracy of 14-bits. The device can be implemented in a fixed configuration with the counter divide ratio stored in a mask programmable on-chip ROM. In a microprocessor based system, it can be dynamically programmed to the application requirement. The part can also be operated as two independently programmable 14-bit dividers. The SC11328 is available in both 24-pin DIP and 28-pin PLCC packages.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINOUTS. NUMBERS IN ( ) ARE PLCC PINS.

Figure 1.

PIN DESCRIPTION

PIN NO. DIP	PIN NO. PLCC	PIN NAME	FUNCTION
1	2	FOUT	Voltage controlled oscillator output.
2	3	DVcc	Digital power supply.
3	4	DGND	Digital ground.
4	5	$\overline{EN}$	VCO enable pin (Active low).
5	6	OUT1	Output of divider "M".
6	7	OUT2	Output of divider "N".
7	9	AVcc	Analog power supply.
8	10	R_{BW}	Resistor to set VCO bandwidth (driven by VCOIN).
9	11	FILTER	Phase locked loop filter.
10	12	VCOIN	Input of VCO.
11	13	R_{FREQ}	Resistor to set VCO free running frequency (R_{FREQ}).
12	14	AGND	Analog ground.
13	16	RCH	Resistor to set the charge pump current (1.25 V).
14	17	SEL	Mode select pin. For SEL = High, source of divide ratios is mask programmable ROM. For SEL = Low, source of divide ratios is internal registers.
15	—	—	Not used.
16	19	XTLOUT	Crystal oscillator output pin. XTLOUT and XTLIN connect to a crystal to generate a crystal locked clock for the chip. If a suitable clock is already available in the system the XTLIN pin can be driven.
17	20	XTLIN	Crystal oscillator input pin.
18	21	CLKIN	Input to divider "N".
19	23	CNT	Straight divider select pin. When CNT = low, PLL mode is disabled and straight divider mode is enabled.
20	—	—	Not used.
21	25	I/O	Serial interface input/output.
22	26	$\overline{RD}$	Serial interface read signal. During low period of this signal the data in the internal shift register is shifted out through the I/O pin.
23	27	$\overline{WR}$	Serial interface write signal. During low period of this signal the data is shifted in the internal shift register from the I/O pin.
24	28	SCLK	Serial interface clock signal.

FUNCTIONAL DESCRIPTION

Chip Architecture

The block diagram of the SC11328 is shown on Page 1 Fig. 1. It consists of two programmable 14-bit dividers, a crystal oscillator, a Phase-Locked Loop (PLL) system, a serial microprocessor interface, a metal mask programmable ROM, and a Post-scaler 2 bit divider. The two 14-bit programmable counters divide the outputs of the oscillator and VCO by "M" and "N" respectively, where "M" and "N" are two integer numbers in the range of 1 to 16,383. The divided outputs are phase-locked to each other by the PLL circuit. The output of the VCO is then divided by the post-scaler modulo "P", where "P" can have a value of 1, 2, 4 or 8. For operation in the range between 1 and 10 MHz the post scaler is required. Above 10 MHz, the post scaler can be used to improve the jitter performance. The output frequency, F_{OUT}, can be calculated as follows:

$$F_{OUT} = F_{VCO}/P = [N/(M \times P)] \times F_{OSC}$$

F_{VCO} = VCO Frequency

F_{OSC} = Oscillation frequency

M , N range from 1 to 16,383 and P = 1, 2, 4 or 8.

The M and N counters need 16 bits for programming (two bits of address and 14 bits of data), and the P-scaler needs 2 bits. These bits can be loaded into the temporary registers that can be addressed through the four-pin serial interface. The M, N and P values stored in the metal mask programmable ROM may be selected instead of using the serial interface.

Circuit Description

Phase-Locked Loop (PLL) Circuit

The PLL circuit consists of a voltage controlled oscillator (VCO), a phase detector circuit, a charge-pump and an external loop-filter. The VCO center frequency and bandwidth are determined by the two external resistors R_{FREQ} and R_{BW}, respectively. V_{VCOIN} represents the VCO input voltage from the loop-filter.

Choosing suitable R_{FREQ} and R_{BW} (bandwidth) values can be accomplished using several different iterative methods. Below are several defining equations and one method for choosing R_{FREQ} and R_{BW}. Note that F_{VCO} is the input frequency of the post-scaler. In general, F_{VCOMIN} should be greater than 10 MHz, F_{VCOMAX} should be less than 100 MHz and F_{VCOMAX}/F_{VCOMIN} should not exceed EQ. 3, which can range typicallyfrom 1 to 3.

The PLL incorporates phase/frequency detector (PFD) logic. A charge pump is used to convert the logic states of the PFD into analog signals suitable for controlling the VCO. The charge pump current is

DEFINING EQUATIONS:

EQ. 1

$$I_{BIAS} = \frac{V_{VCOIN}}{R_{BW}} + \frac{2.2V}{R_{FREQ}}$$

V_{VCOIN} typically can range from 1V to 3V; 2V is nominal.

EQ. 2

$$F_{VCO} = \frac{1000}{\frac{4400}{I_{BIAS}} + 3}$$

EQ. 3

$$\frac{F_{VCOMAX}}{F_{VCOMIN}} = \frac{V_{VCOMAX} + 2.2\frac{R_{BW}}{R_{FREQ}}}{V_{VCOMIN} + 2.2\frac{R_{BW}}{R_{FREQ}}}$$

Outlined below is a method for calculating R_{FREQ} and R_{BW} using EQ. 1 and EQ. 2.

Step 1. Choose the desired F_{VCOMIN} and F_{VCOMAX}.

Step 2. Calculate $I_{BIASMIN}$ and $I_{BIASMAX}$ using EQ. 4 and EQ.5.

EQ. 4

$$I_{BIASMIN} = \frac{4400}{\frac{1000}{F_{VCOMIN}} - 3}$$

EQ. 5

$$I_{BIASMAX} = \frac{4400}{\frac{1000}{F_{VCOMAX}} - 3}$$

Step 3. Calculate R_{BW} by using EQ. 6 and subtracting $I_{BIASMAX}$ from $I_{BIASMIN}$.

EQ. 6

$$R_{BW} = \frac{V_{COMAX} - V_{COMIN}}{I_{BIASMAX} - I_{BIASMIN}} = \frac{3V - 1V}{\Delta I_{BIAS}}$$

Step 4. Calculate R_{FREQ} using EQ. 7.

EQ. 7

$$R_{FREQ} = \frac{2.2V}{I_{BIASMAX} - \frac{3V}{R_{BW}}}$$

R_{BW} in MΩ , I_{BIAS} in μA

Step 5. If either R_{FREQ} or R_{BW} is negative, then choose a smaller ΔF_{VCO} and repeat steps 1 through 4.

determined by the external resistor RCH, and its value is given by:

ICH = 1.25V/RCH; RCH ~1.6 KΩ

A filter is added after the charge-pump to smooth the VCO control voltage. Figure 2 shows the complete PLL circuit. The states of the PFD are determined by the edges of the input wave-form. If the R-input (reference) phase leads the V-input (VCO) phase, then an edge of the R input sets the U (up) terminal true. The next V edge resets the U terminal false. Conversely, if V leads R, a V edge sets D (down) true and the next R edge resets D false. Both U and D can be false simultaneously, or either one alone can be true, but both can never be true simultaneously. Therefore a PFD has three allowable states at its output terminals, up (U), down (D) and neutral(N).

A typical circuit for the charge-pump and two possible loop-filters are shown in Figure 3. The loop filter consisting of the simple resistor capacitor combination has the disadvantage of having some granularity effect. Upon each cycle of the PFD, the pumping current Ip is driven into the filter impedance which responds with an instataneous voltage jump of delta (Vc) = ICH*R2.

At the end of the charging interval, the pump current switches off and a voltage jump of equal magnitude occurs in the opposite direction. The frequency of the VCO follows the voltage steps so there will be frequency excursion. The second loop filter has an additional capacitor C3 is parallel with the R2-C2 impedance. Because of this capacitor, the VCO control voltage has a continuous ramp-like, exponential function for each pump pulse, instead of the rectangular jump that is present in the filter without the additional capacitor.

Mask Programmable ROM

For fixed frequency configuration, the M, N and P divide ratios can be stored in an on-chip ROM with a custom metal mask. To access the counter divide ratios in the ROM, the SEL pin should be tied high. Contact Sierra Semiconductor for generation of a custom metal mask for ROM storage.

Serial Interface

Each counter needs 16 bits for programming, out of which 2 bits are for the destination's address and 14 are for data bits (see Table 1 and 2). The programming bits are loaded into the chip through the serial interface and are stored in the registers in Figure 4.

The divider programming data is stored in the internal temporary register through a four pin serial interface. When $\overline{WR}$ goes low, sixteen bits of data are shifted serially into the chip through the I/O pin.The sixteen bits constitute fourteen bits of programming data and two bits of destination address. The data is sampled on the rising edge of the shift clock (SCLK). When $\overline{WR}$ goes high, the contents of the memory location selected by the two bit destination address is updated by the fourteen bit data. For proper

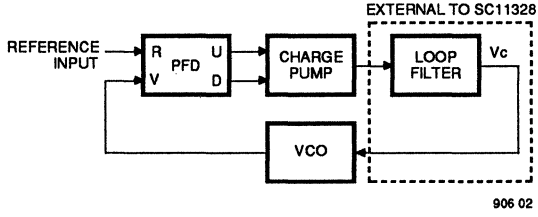


Figure 2. PLL with Three-State Phase Detector and Charge Pump

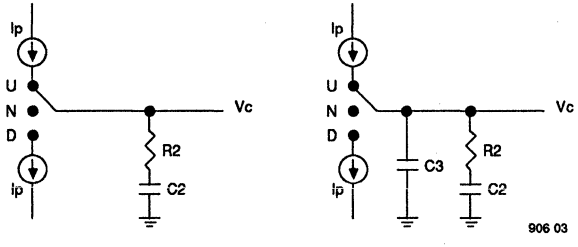


Figure 3. Charge Pumps and Loop Filters

A1	A0	DESTINATION
0	0	P (D0–D1)
0	1	N (D0-D13)
1	0	M (D0–D13)
1	1	Reserved

Table 1.

Note: When writing to the P Register D2 to D13 = 0, see Table 2 for D0, D1 values.

D1	D0	DATA
0	0	÷1
0	1	÷2
1	0	÷4
1	1	÷8

Table 2.

Note: This table is for use with the P Register only.

D13	...	D3	D2	D1	D0	DATA
0		0	0	0	0	÷1
0		0	0	0	1	÷1
0		0	0	1	0	÷2
0		0	1	0	0	÷4
						⋮
1		0	0	0	0	÷8192
	...					⋮
1		1	1	1	1	÷16383

Table 3.

Note: This table is for use with the M and N register.

operation of the interface, there has to be exactly sixteen SCLK pulses within the $\overline{WR}$ high-to low and low to high transition period. After WR goes high, an additional 10 SCLK pulses are required to load the new data. Also, the first Write after a Power Up requires 10 SCLK pulses before WR goes low. After the 10 SCLK pulses, the user can read the data into the temporary register. Every read of a selected location should be preceded by a write into the same location. To read the data out, The $\overline{RD}$ signal should be pulled low. After sixteen clock pulses all the data inside the shift register will be clocked out of the I/O pin. The data appears at the output, on the rising edge of the shift clock (SCLK). To avoid conflicts, the falling edge of the $\overline{RD}$ signal should be at least ten SCLK periods away from the rising edge of $\overline{WR}$.

The same rule applies to consecutive write cycles. The serial interface timing diagram is shown in Figure 6 and Figure 7.

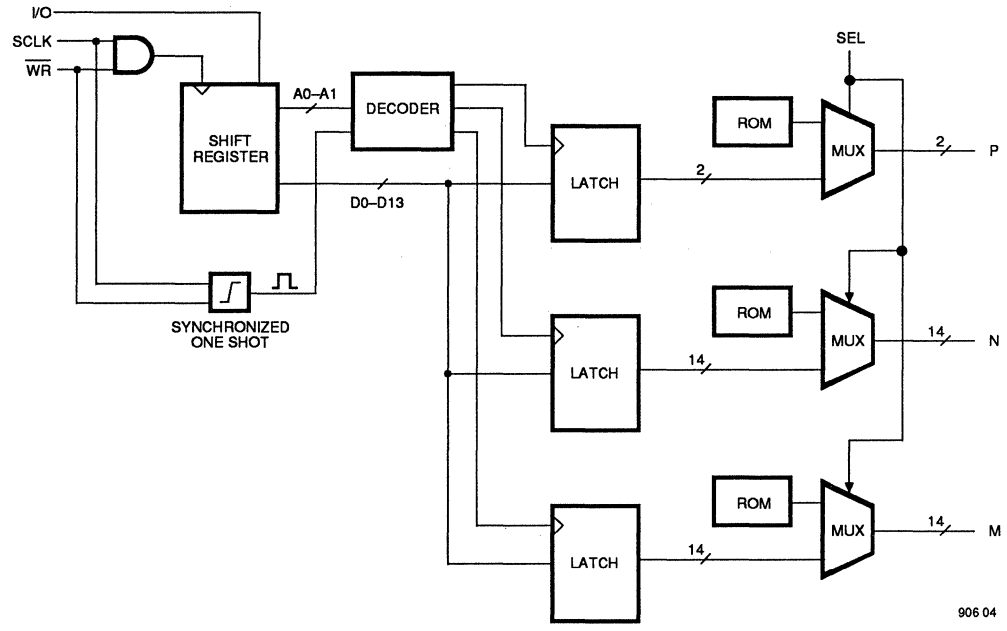


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Figure 5 shows a typical crystal implementation. The capacitors C1 and C2 have a range of 20pF to 5 pF. Depending on the frequency of the crystal, it is recommended to use maximum 20 pF for frequencies lower than 10 MHz, and for frequencies above 10 MHz capacitor values between 10pF and 5 pF are recommended.

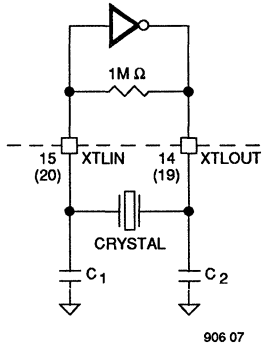

Figure 5. Typical Crystal Implementation

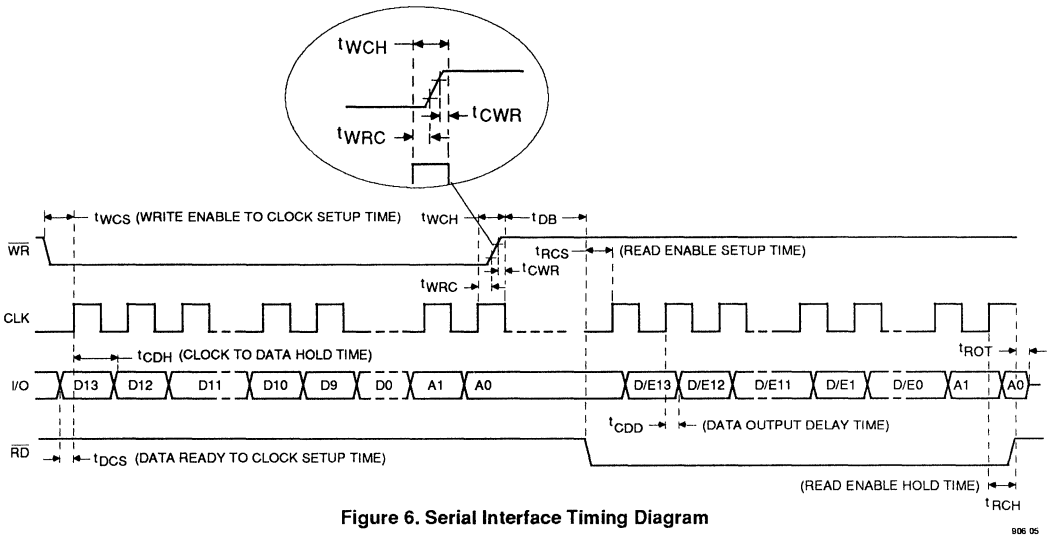

Figure 6. Serial Interface Timing Diagram

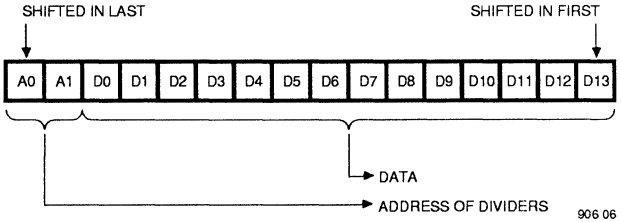

Figure 7. Address/Data Allocations for the Input Bits

SERIAL INPUT TIMING

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t_{WCH}	Clock to Write Enable Hold Time	50			ns
t_{DB}	The number of SCLK periods after Power Up, before the first Write Cycle and after aech Write Cycle	10			SCLK Periods
t_{RCS}	Read Enable to Clock Set-up Time	50			ns
t_{CDD}	Clock to Data Output Delay Time			75	ns
t_{RCH}	Clock to Read Enable Hold Time	75			ns
SCLK	Clock Frequency			5	MHz
t_{ROT}	Read Enable High to Output Tristate			50	ns

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Supply Voltage, Vcc–GND	6 V
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GND	Ground			0		V
XTLIN, XTLOUT	Crystal Frequency			20	30	MHz
Tr,Tf	Input Rise or Fall Time				50	ns

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package –12mW/°C from 65–85°C

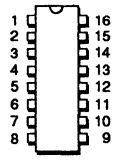
DC ELECTRICAL CHARACTERISTICS (Ta = 0 TO 70°C, DVcc = 5V ±10%, AVcc = 5V ±10%)

PARAM.	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
Icc	Quiescent Current			30		mA
Vih	High Level Input Voltage, All Inputs		2.2			V
Vil	Low Level Input Voltage, All Inputs				.8	V
Voh	High Level Output, All Outputs Except XTLOUT (Ioh = 0.5 mA) (Ioh = 100 µA)		 2.4 4.5			 V V
Vol	Low Level Output, All Outputs Except XTLOUT (Iol = 1.6 mA) (Iol = 100 µA)				 0.6 0.2	 V V
Voh	High Level Output XTLOUT (Ioh = 20 µA)		 4			 V
Vol	Low Level Output XTLOUT (Iol = 20 µA)				 0.2	 V

FEATURES

- ☐ Bell 43003/43004 compatible
- ☐ Precise 2713 Hz detector with fail-safe timer
- ☐ Manual loopback activation and release
- ☐ On-chip anti-aliasing filter
- ☐ 2.048, 3.579 or 6.144 MHz clock input or crystal
- ☐ 1.5, 4.0 or 20.0 minute timeout select
- ☐ 16-pin DIP package

16-PIN DIP PACKAGE



SC11330CN

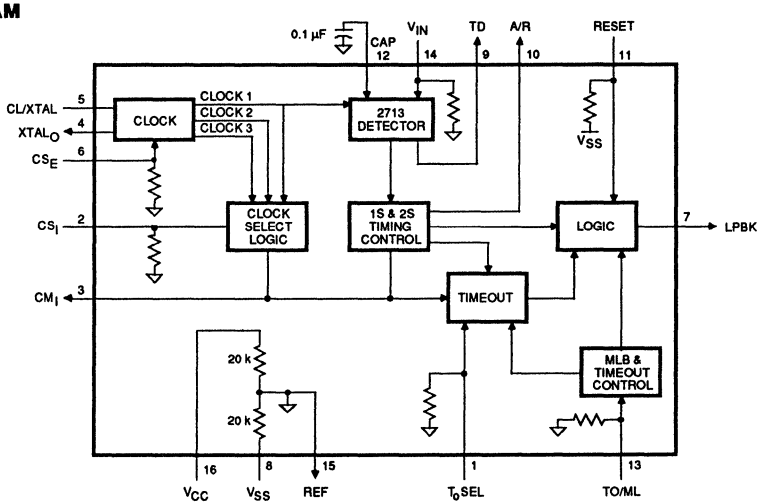
GENERAL DESCRIPTION

The SC11330 is a low-power CMOS IC designed to provide the 2713 Hz Detection and Control for the purpose of initiating a Loopback Command. This IC contains a precise Tone Detector with Guardband filter and Signal Timing Qualification, a Loopback Fail-safe Timer and a Loopback output for controlling an external relay.

The primary application for the SC11330 is in Local Loop diagnostics, specifically for 4-wire private line circuits. Through the use of this IC, detection of the 2713 Hz tone will cause the Receive pair to be connected to the Transmit pair through a gain control circuit such as the Sierra SC11310 Gain/Loss Control or appropriate external circuitry to permit troubleshooting of the Local Loop. The SC11330 responds to loopback tones of proper level and duration received in the frequency range 2701–2725 Hz and rejects as invalid any tone received outside the frequency range 2681–2745 Hz at the signal input pin V_{IN}. A tone of proper frequency and duration must be at a level between –33 and 0 dBm to be detected and a tone lower than –38 dBm will be rejected.

To provide proper signal-to-guard margin, the SC11330 will not respond to loopback tones unless the tone is 9–15 dB stronger than the sum of all other tones present. This signal-to-guard margin prevents data signals, voice signals or their harmonics from initiating false activation.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINS.

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	ToSEL	Timeout Period select. After tone activation, the SC11330 remains in the activation mode, unless manually deactivated, or after timeout period T, after which the IC automatically resets. The timeout period is selected in accordance with Table 1.
2	CS_I	Internal Clock Select. Provides for the selection of one of three internal clock frequencies in accordance with Table 2.
3	CM_I	Internal Clock Monitor. Used for monitoring the frequency of the internal clock that was selected.
4	$XTAL_O$	Crystal Output.
5	CL/XTAL	Crystal or Clock Input
6	CS_E	External Clock/Crystal Frequency Select. See Table 3. Other frequencies are determined by the relationship: $\text{XTAL Freq} = \text{Normal XTAL Freq} \times \frac{\text{(Desired Frequency)}}{2713\ \text{Hz}}$
7	LPBK	Loopback Detect. Low (V_{SS}) when loopback is active. High (V_{CC}) when loopback in not active
8	V_{SS}	Negative supply –9.0 to –11.0 Vdc relative to V_{CC} for 10 V operation, –4.5 to –5.5 Vdc relative to V_{CC} for 5 V operation.
9	TD	Tone Detect. Goes low within 60 milliseconds after loopback or other selected tone is applied. Returns to high upon removal of loopback tone.
10	A/R	Activation/Restoral. This pin will be low in idle state and go high within 60 milliseconds after a valid activation or deactivation tone is applied. The pin will go low within 60 milliseconds after a valid activation tone has been present for the required 2 seconds (and before the activation tone is removed). This pin will also go low within 60 milliseconds after a valid deactivation tone has been present for the required 1 second. See Figure 2 for timing diagram.
11	Reset	Loopback reset. A high input resets an active loopback state and restores the SC11330 to an idle state clearing all counters and readying the IC to perform another loopback sequence.
12	CAP	External Capacitor. Equal to 0.1 µF ±20%, non-polar.
13	TO/ML	Time out enable/Manual loopback. After tone activation, the SC11330 will remain in the activation mode, unless deactivated, for a period T after which the IC will automatically revert to the idle state. The time T will be either 1.5, 4.0, or 20.0 minutes ±1% selected via a timeout period select pin. This pin also permits timeout function to be disabled and provides for manual loopback. See Table 4 for mode select.
14	V_{IN}	Signal Input. 200 kΩ (min) imput impedance.
15	Ref	Reference or Common Output. Internal divider, typically = $\frac{V_{CC} + V_{SS}}{2}$
16	V_{CC}	Positive supply +9.0 to +11.0 Vdc relative to V_{SS}, for 10 V operation, +4.5 to +5.5 Vdc relative to V_{SS} for 5 V operation.

Input	Timeout (Minutes)
High	1.5
Low	20
Ref	4

Table 1. Timeout Select

Input	Frequency (kHz)
High (Test)	4
Low (Test)	16 if 1.5 Min. Timeout is selected 64 if 4 or 20 Min. Timeout is selected
Ref	31.25

Table 2. Internal Clock Select

Input	Frequency (MHz)
High	2.048
Low	6.144
Ref	3.579545

Table 3. External Clock/Crystal Frequency Selection

Input	Mode
High	Active Manual Loopback
Low	Timeout Enable
Ref	Timeout Disable

Table 4. Mode Select

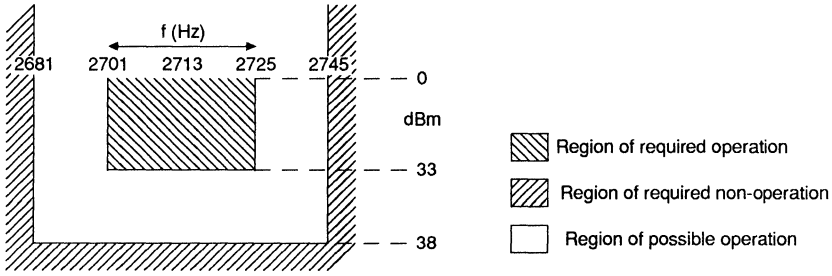


Figure 1. Control Tone Selectivity and Sensitivity

FUNCTIONAL DESCRIPTION

Signal-to-Guard Margin

The SC11330 will not respond to any loopback tone of the proper level and frequency as previously described if any other single frequency or combination of frequencies within the range of 500–2500 or 2926–5000 Hz is present at a power level of the loopback tone less 9–15 dB.

Control Logic

Refer to Figure 2 for timing diagrams. Loopback activation corresponds to a continuous low state at the LPBK pin. Deactivation or idle corresponds to a high state.

The SC11330 will respond to a loopback activation tone received for at least 2.0 ±0.1 seconds. Once the minimum period requirement has been met, there is no restriction on the length of time the tone may be present. The loopback function will not operate until, but upon, removal of tone. The SC11330 will reject as invalid any loopback activation tone received for 1.9 seconds or less.

Prior to meeting the minimum 2.0 ±0.1 second period requirement, the IC will ignore an activation tone interruption of 2 milliseconds or less. Also, prior to the minimum period requirement, an activation tone interruption of 20 milliseconds or greater will reset the nominal 2-second timer.

The SC11330 will not respond to a manual activation signal while in a tone-activated mode.

A loopback tone activated restoral function is included in the IC. The SC11330, in its activated mode, returns to the idle mode in response to the application of a loopback tone at its input for a minimum of 1.0 ±0.1 seconds and does not reactivate until the tone has been removed and a valid loopback

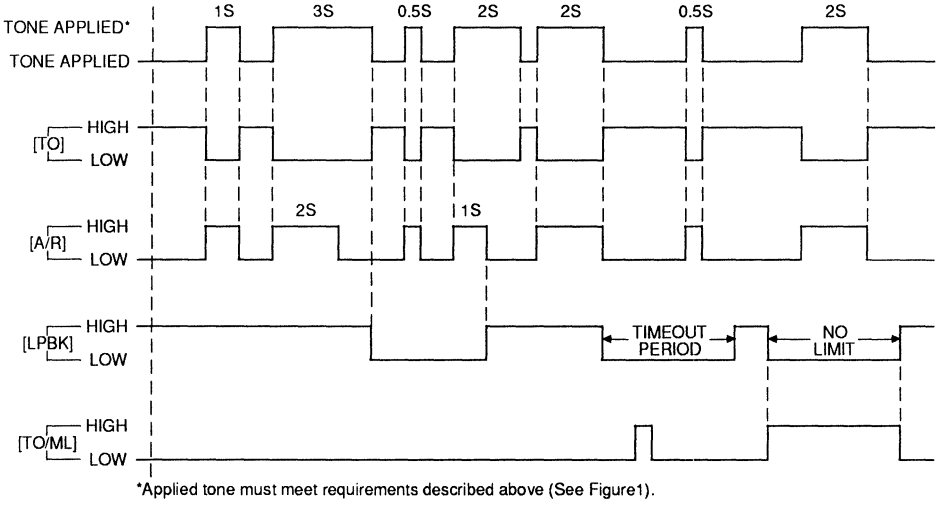


Figure 2. Tiiming Diagram

activation tone reapplied. As soon as the loopback restoral tone has been present for at least 1.0 ±0.1 second, the IC returns to an idle state without removal of the tone.

Once the minimum 1.0 ±0.1 second period has been met, there is no restriction on the length of time the tone may be present. The IC will not deactivate if this restoral tone is present for less than 0.9 seconds.

Prior to meeting the minimum 1.0 ±0.1 second period requirement, the IC ignores a deactivation tone interruption of 2 milliseconds or less. Also prior to meeting the minimum period requirement, a deactivation tone interruption of 20 milliseconds or greater shall reset the nominal 1 second timer.

Once the minimum activation or deactivation tone period requirement has been met, the IC ignores a tone interruption of 100 milliseconds or less. Also after meeting the minimum period requirement, a tone interruption of 200 milliseconds or greater will be responded to as a valid tone removal.

After tone activation, the IC remains in the activation mode, unless deactivated, for a period T after which the unit will automatically revert to the idle state. Time T is either 1.5, 4.0, or 20.0 min. ±1% selected via a timeout period select pin 1 (T_OSEL). In addition, Pin 13 (TO/ML) disables the timeout function, leaving tone activated restoral operation. This pin will place the device in the loopback mode manually (See Table 4).

The SC11330 will not respond to 2713 Hz tone while in a manual activation mode. Returning the manual activation line to the idle state immediately returns the device to the idle state.

To inhibit tone operation, the input Pin 14 (Vin) can be switched open.

The LPBK pin provides the indication of loopback. A low state indicates loopback, a high state indicates idle. The pin sources or sinks 1 mA of DC currect. Loopback occurs after an idle period when a proper frequency and level loopback activation tone satisfying the signal to guard requirements has been met or occurs when the manual loopback pin is pulled high.

External Reset

Pin 11 (Reset) is provided to force the device into the idle mode regardless of the current state. All counters are subsequently cleared, readying the IC to perform another loopback sequence. This pin can be used to aid in testing and troubleshooting.

False Activation

In the idle mode, power interruption of any length will not cause false activation. Upon reapplication or initial application of power the IC stabilzes to the idle state within 10 milliseconds.

Anti-Aliasing

The input stage of the SC11330 includes a low-pass antialiasing filter, with a cutoff frequency of 5.9 kHz and 12 dB/octave roll-off

5 Volt Operation

For 5 Volt operation the min supply voltage is 4.5 Vdc, max voltage 5.5 Vdc. With a 5 Volt supply, the threshold levels for operate & non-operate are reduced 6 dB (–39 dBm must, –44 dBm must not) detect. This difference can be compensated for with a 1/2 resistor divider from the signal source to the loopback IC input Pin 14.

Power Supply Decoupling and Circuit Layout Considerations

For optimum performance and miximum immunity to power supply noise, it is important to decouple the power supplies as shown in Figure 4. Small inductors in series with the positive and negative supplies help suppress RFI as well as improve the power supply noise rejection capability of the SC11330 when used with the decoupling capacitors. The 10 µF capacitors should be tantalum type while the 0.1 µF capacitors should have a good high frequency rejection characteristic; monolithic ceramic types are recommended.

It is important to locate the decoupling capacitors as close to the actual power supply pins of the SC11330 as possible.

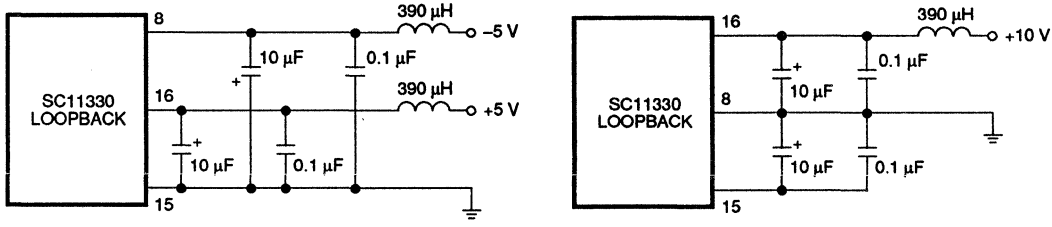


Figure 3. Power Supply Decoupling

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, V_{CC} –V_{SS}	+14 V
DC Input Voltage (Analog Signals)	V_{SS}-0.6V to V_{CC}+0.6
DC Input Voltage (Digital Signals)	V_{SS}-0.6V to V_{SS}+0.6
Storage Temperature Range	–65 to +150°C.
Power Dissipation (Note 3)	500mW
Lead Temperature (Soldering, 10 sec)	300°C.

Note 1. Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

2. Unless otherwise specified, all voltages are referenced to ground.

3. Power dissipation temperature derating—Plastic package: –12mW/C from 65°C to 85°C

OPERATING CONDITIONS (Note 4)

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient Temperature		0		70	°C
V_{CC}–V_{SS}	Positive Supply Voltage		9.0	10.0	11.0	V
REF	Reference Output			5.0		V

Note 4. Min and Max values are valid over the full temperature and operating voltage range. Typical values are from 25°C and ±5 volt operation.

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = +5 V ±10%, V_{SS} = –5 V ±10%)

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Quiescent Current	V_{CC}–V_{SS} = 10 Volts		6.0	10.0	mA
I_{SS}	Quiescent Current	V_{CC}–V_{SS} = 10 Volts		6.0	10.0	mA
I_{CC}	Quiescent Current	V_{CC}–V_{SS} = 5 Volts		4.0		mA
I_{SS}	Quiescent Current	V_{CC}–V_{SS} = 5 Volts		4.0		mA

INPUTS

V_{IH}	High Level Input	=	V_{CC}+0/–1.5 V
V_{IL}	Low Level Input	=	V_{SS}–0/+1.5 V
V_{OPN}	Common	=	REF ±0.6 V

OUTPUTS

V_{OH}	High Level Input	=	V_{CC}+0/–1.5 V
V_{OL}	Low Level Input	=	V_{SS}–0/+1.5 V

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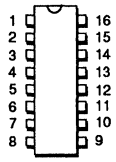
SIERRA SEMICONDUCTOR

SC11346
Phase-Locked Loop (PLL)

FEATURES

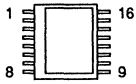
- ☐ Operating freq. range up to 80 MHz at V_{DD}= 5 V
- ☐ Choice of three phase comparators
- ☐ Lock indication output
- ☐ Fast comparator response time (V_{DD} = 4.5v)
  - Comparator I: 20 ns
  - Comparator II: 20 ns
  - Comparator III: 25 ns
- ☐ Full power down capability
- ☐ VCO enable control for ON-OFF keying and low power consumption
- ☐ High VCO linearity:<1% at V_{DD} = 5 V
- ☐ Buffered output of VCO control input
- ☐ Output duty cycle: 50 ±1% at 20 MHz
- ☐ 16 pin DIP or 16 pin SOIC

16-PIN DIP PACKAGE



SC11346CN

16-PIN SOIC PACKAGE



SC11346CM

GENERAL DESCRIPTION

The SC11346 is a low-power phase-locked loop (PLL) fabricated using SIERRA's advanced 1.5 µm CMOS technology that can accommodate frequency synthesis or multiplication up to 80 MHz.

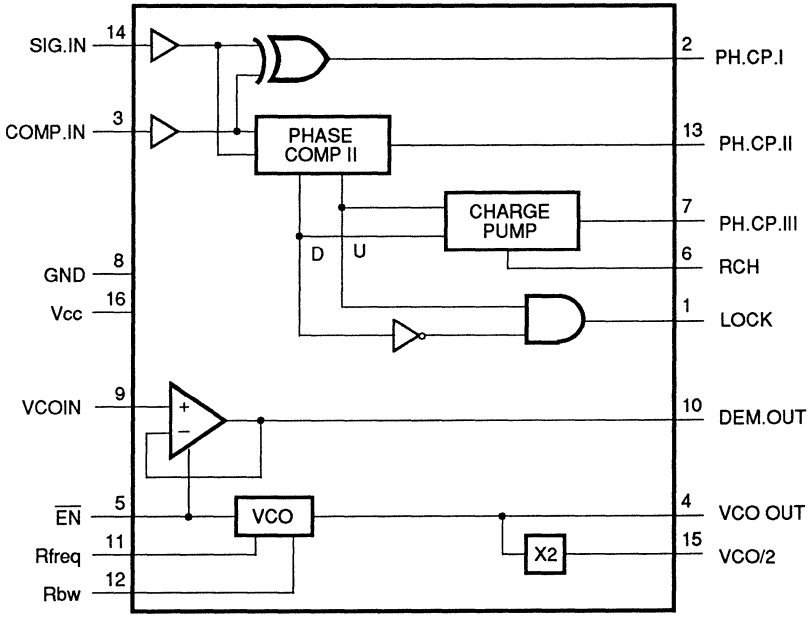
The SC11346 consists of a linear voltage-controlled oscillator (VCO) and three different phase comparators having a common signal-input amplifier and a common comparator input.

The signal input can be direct-coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for signals as low as 200 mV.

APPLICATIONS

- ☐ Frequency synthesis or multiplication up to 80 MHz
- ☐ FM demodulation/modulation
- ☐ High frequency PLL systems
- ☐ Voltage-to frequency converter
- ☐ Frequency discrimination
- ☐ Data synchronization
- ☐ Tone decoding
- ☐ FSK modem
- ☐ Signal conditioning

BLOCK DIAGRAM



833 02

FUNCTIONAL DESCRIPTION

Phase comparator I is an exclusive OR(XOR) gate. It provides a digital signal that maintains a 90 phase shift between the VCO's center frequency and the input signal (50% duty cycle input) waveforms. This phase detector is more susceptible to locking onto harmonics of the input frequency than phase comparator II, but provides better noise rejection.

Phase comparator II and III are edge sensitive digital sequential networks. Three signal outputs are provided, two comparator outputs and a phase pulse output. The comparator outputs are TRI-STATE outputs that provide a signal that locks the VCO output signal to the input signal with 0 phase shift between them. These comparators are more susceptible to noise throwing the loop out of lock, but are less likely to lock onto harmonics than the comparator I. Comparator II provides a voltage output while comparator III provides a current charge up/charge down output.

In a typical application all three comparators feed an external filter network which in turn feeds the VCO input. This input is a very high impedance CMOS input which also drives the voltage follower. The VCO's operating frequency is set by two external components connected to the RF and RG pins.

An inhibit pin is provided to disable the VCO and the source follower, providing a method of putting the IC in a low power state.

The voltage follower is a CMOS high speed op amp, and provides a means of looking at the VCO input without loading down the characteristics of the PLL filter.

PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	LOCK used	Indicates the locked state of the phase-locked loop when phase comparators II or III are
2	PH.CP.I	Phase comparator 1 output
3	COMP.IN	Input to the comparator
4	VCOOUT	Output of the voltage controlled oscillator
5	$\overline{EN}$	VCO enable pin. When $\overline{EN}$ = low then the VCO is running
6	RCH	Resistor to set the charge pump current (1.25 V)
7	PH.CP.III	Phase comparator III output (charge pump)
8	GND	Ground
9	VCOIN	Input of VCO
10	DEM.OUT	Demodulator output
11	RF	Resistor to set VCO free running frequency (Rcenter)
12	R_{BW}	Resistor to set VCO bandwidth (driven by VCOIN)
13	PH.CP.II	Phase comparator II output
14	SIG.IN	Signal input
15	VCO/2	Output of the VCO divided by two
16	V_{CC}	Positive power supply voltage V_{CC} = + 5V ±10%

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, V_{CC}–GND	7V
DC Input Voltage	GND–0.5 to V_{CC}+0.5 V
Storage Temperature Range	-65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 sec.)	300°C

Note 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

OPERATING CONDITIONS

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
GND	Ground			0		V
SIG.IN	Signal Frequency		2.0		80	MHz
T_R, T_F	Input Rise or Fall Time				50	ns

DC ELECTRICAL CHARACTERISTICS (T_A = 0–70°C, V_{CC} = +5 V ±10%,

PARAM.	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	80 MHz		60		mA
V_{IH}	High Level Input Voltage; All Inputs		2.2			V
V_{IL}	Low Level Input Voltage; All Inputs				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA) (I_{OH} = 100 µA)		 2.4 4.5			 V V
V_{OL}	Low Level Output - All Outputs (I_{OL} = 1.6 mA) (I_{OL} = 100 µA)				 0.6 0.2	 V V

CIRCUIT DESCRIPTION

Phase-Lock Loop (PLL) Circuit

The block diagram of the SC11346 is show on the first page. It consists of a voltage controlled oscillator (VCO), a phase detector circuit, a charge-pump, an XOR gate, lock detector, buffer amplifier, and a divide by two. The VCO center frequency and bandwidth are determined by the two external resistors RF and RG. V_{COIN} represents the VCO input voltage from the loop-filter, where the VCO frequency is given by the equations:

$$I_{bias,\,VCO} = (4.4 * 10^{-12}) * F_{VCO}$$

$$Fvco = (2.2/RF + V_{COIN}/RG) * 2.273 * 10^{11}$$

RG&RF are in Ω, Fvco in Hz

where V_{COIN} has a range of 1 to 3 Volts. If Fvco(center) and Fvco(max) represent the center and maximum VCO frequencies for V_{COIN} = 2V and V_{COIN} = 3V respectively, the values of RF and RG can be calculated from the following two equations:

$$RF = (5*10^{11}) / (3F_{VCO}(center) - 2F_{VCO}(max))$$

$$RG = 1/([F_{VCO}(max) - F_{VCO}(center)] * (4.4 * 10^{-12}))$$

The phase comparator ll incorporates a sequential-logic phase/frequency detector (PFD). A charge pump accompanies the phase comparator ll to convert the logic states of the comparator into charge up/charge down signals suitable for controlling the VCO. The charge pump current is determined by the external resistor RCH, and its value is given by:

$$ICH = 2.5V/RCH$$

A filter is added after the charge-pump to smooth the VCO control voltage.

Figure 2 shows the complete PLL circuit. The states of the PFD are determined by the edges of the input wave-form. If the R-input (reference) phase leads the V-input (VCO) phase, then a rising edge on R input sets the U (up) terminal true. The next rising V edge resets the U terminal false. Conversely, if V leads R, a V edge sets D (down) true and the next R edge resets D false. Both U and D can be false simultaneously, or either one alone can be true, but both can never be true simultaneously. Therefore a PFD has three allowable states at its output terminals, up (U), down (D) and neutral(N).

A typical circuit for the charge-pump and two possible loop-filters are shown in Figure 3. The loop filter consisting of the simple resistor-capacitor combination has the disadvantage of having some granularity effect. Upon each cycle of the PFD. The pumping current Ip is driven into the filter impedance which responds with an instantaneous voltage jump of delta(Vc) = I_p * R2.

At the end of the charging interval, the pump current switches off and a voltage jump of equal magnitude occurs in the opposite direction. The frequency of the VCO follows the voltage steps so there will be corresponding frequency excursions. The second loop filter has an additional capacitor C3 in parallel with the R2-C2 network. Because of this capacitor, the VCO control voltage has a continuous ramp-like, exponential function for each pump pulse, instead of the rectangular jump that is present in the filter without the additional capacitor. This provides reduced phase noise at the VCO output.

Phase comparator l, an exclusive OR gate, provides a digital error signal (PH.CP.l) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle) it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator ll is an edge-controlled digital memory network. It provides a digital error voltage signal (PH.CP.ll).The lock-in (phase pulses) indicates a locked condition (0° phase shift between signal input and comparator input) when comparator ll or lll is used.

Phase comparator lll is using the information of the phase comparator ll, namely up and down signals, to generate out of a charge pump a constant current that will in turn provide a voltage that is centered at 2V if the VCO is at the frequency of the signal input, if the signal lags

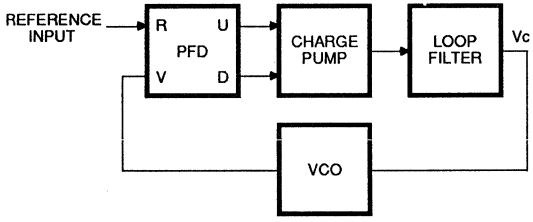


Figure 2. PLL with Three-State Phase Detector and Charge Pump

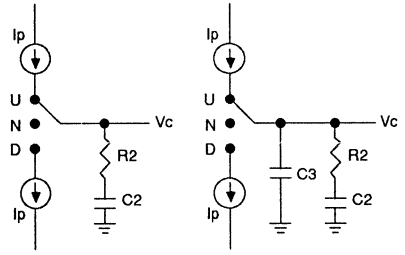


Figure 3. Charge Pumps and Loop Filters

then the voltage will decrease and if the signal input is faster then the voltage will increase.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCOOUT) whose frequency is determined by the voltage at the VCOIN Input, and resistors connected to pin RF and RG.

The source follower output of the VCOIN (DEM.OUT) is the output of a unity-gain connected opamp.

The $\overline{EN}$ input, when high, disables the VCO and the source follower to minimize the standby power consumption.

DETAILED CIRCIUT DESCRIPTION

Votlage Controlled Oscillator/ Source Follower

The VCO requires two external components to operate. These are RF and RG. Resistor RF is selected to determine the center frequency of the VCO (see typical performance curves). RF can be used to set the offset frequency with 0V at VCO input. If RF is omitted the VCO range is from 0 Hz; as RF is decreased, the offset frequency is increased. The effect of RF is shown in the design information table and typical performance curves. By increasing the value of RG the lock range of the PLL is decreased and the gain (volts/Hz) is increased. Thus, for a narrow lock range, large swings on the VCO input will cause less frequency variation.

Internally, the resistors set a current in a current mirror, as show conceptually in Figure 4. The mirrored current drives two capacitors alternatly; once a capacitor charges up to the threshold of the biased inverter the oscillator logic flips the capacitor over and causes the mirror to charge the other capacitor. The output from internal logic is then taken to pin 4.

The input to the VCO is a very high impedance CMOS input and thus will not load down the loop filter, easing the filters design. In order to make signals at the VCO input accessible without degrading the loop performance, a voltage follower opamp is provided.

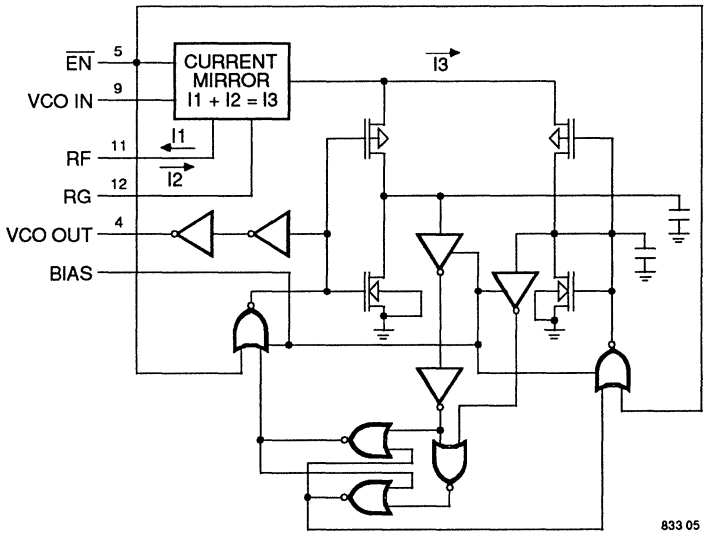


Figure 4.

PHASE COMPARATORS

All three phase comparators have two inputs, Signal in and Comparator in. They both have high speed Schmitt comparators with special DC bias network that enables AC coupling of input signals. If the signals are not AC coupled then these input require logic levels the same as standard 54HC/74HC.

In normal operation Vcc and ground voltage levels are fed to the loop filter. Comparator lll provides a charge-up/charge down current output the value of which is given by $I_{CH} = 2.5/Rch$.

Figure 5 shows the state tables for all three comparators.

Phase Comparator I

This comparator is a balanced XOR gate, and its operation is similar to an overdriven balanced modulator. To maximize lock range the input frequencies must have a 50% duty cycle. Typical input and output waveforms are shown in Figure 7. The output of the phase detector feeds the loop filter which averages the output voltage. The frequency range upon which the PLL will lock onto if initially out of lock is defined as the capture range. The capture range for phase detector 1 is dependent on the loop filter employed. The capture range can be as large as the lock range, which is equal to the VCO frequency range.

To see how the detector operates, refer to Figure 7. When two square wave inputs are applied to this comparator, an output waveform whose duty cycle is dependent on the phase difference between the two signals results. As the phase difference increases, the output duty cycle increases and the voltage after the loop filter increases. Thus, in order to achieve lock when the PLL input frequency increases, the VCO input voltage must increase and the phase difference between comparator in (COMP. IN) and signal in (SIG. IN) will increase. At an input frequency equal to Fmin, the VCO input is at 0V. This requires the phase detector output to be grounded; hence, the two input

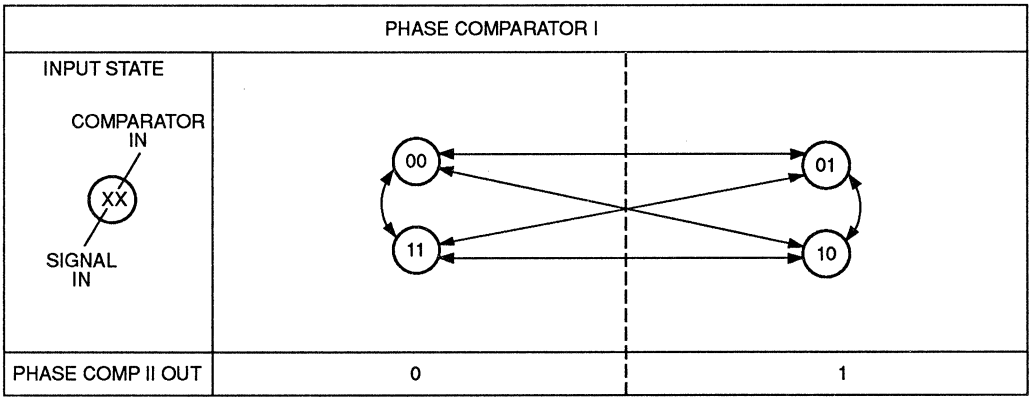


Figure 5.

signals must be in phase. When the input frequency is Fmax, the VCO input must be Vcc and the phase detector inputs must be 180 out of phase.

The XOR is more susceptible to locking onto harmonics of the signal input than the digital phase detector II. For instance, a signal 2 times the VCO frequency results in the same output duty cycle as a signal to the VCO frequency. The difference is that the output frequency of the 2f example is twice that of the other example. The loop filter and the VCO range should be designed to prevent locking on to the harmonics.

Phase Comparator II

This detector is a memory based network. It consists of two flip-flops and some gating logic, a three state output and a phase pulse output as shown in Figure 8. This comparator acts only on the negative edges of the input signals and is thus independent of a signal duty cycle.

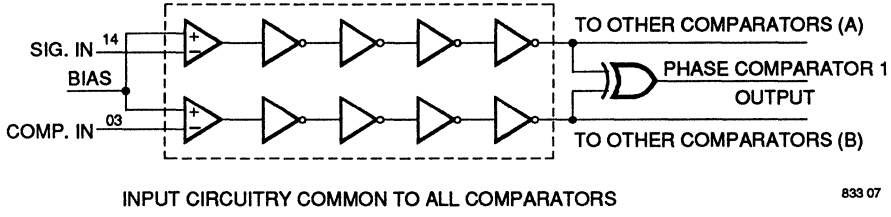


Figure 6.

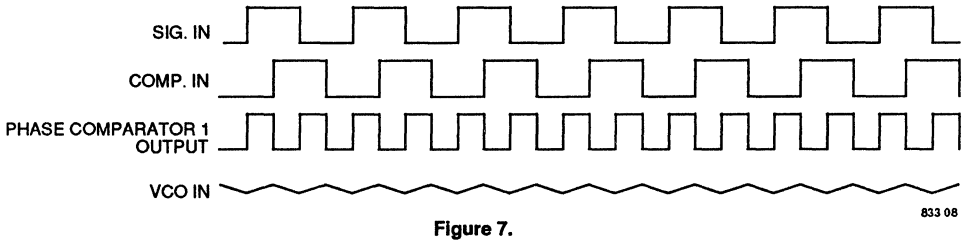


Figure 7.

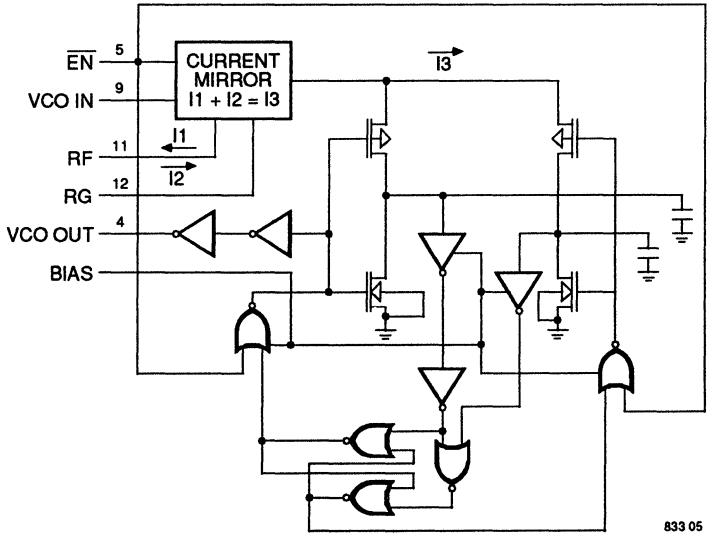


Figure 8.

Phase comparator ll operates in such a way as to force the PLL into lock with 0 phase difference between the VCO output and the signal input negative waveform edges, figure 9 shows some typical loop waveforms. First assume that the signal input phase is leading the comparator input. This means that the VCO's frequency must be increased to bring its leading edge into proper phase alignment. Thus the phase detector ll output is set high. This will cause the loop filter to charge up the VCO input, increasing the VCO frequency. Once the leading edge of the comparator input is detected, the output goes tri state holding the VCO input at the loop filter voltage. If the VCO still lags the signal then the phase detector will again charge up to VCO input for the time between the leading edges of both waveforms.

If the VCO leads the signal then when the leading edge of the comparator in is seen, the output of the phase comparator goes low. This discharges the loop filter until the leading edge of the signal in is detected at which time the output disables itself again. This has the effect of slowing down the VCO to again make the rising edges of both waveforms coincidental.

When the PLL is out of lock, the VCO will be running either slower or faster than the signal input. If it is running slower the phase detector will see more signal rising edges and so the output of the phase comparator will be high a majority of the time, raising the VCO's frequency. Conversely, if the VCO is running faster than the signal, the output of the detector will be low most of the time and the VCO's output frequency will be decreased.

As one can see, when the PLL is locked the output of phase comparator ll will be almost always disabled except for minor corrections at the leading edge of the waveforms. When the detector is tri-state the phase pulse output is high. This output can be used to determine when the PLL is in the locked condition.

This detector has several interesting characteristics. Over the entire VCO frequency range there is no phase difference between the comparator input and the signal input. The lock range of the PLL is the same as the capture range. Minimal power is consumed in the loop filter since in lock the detector output is a high impedance. Also, when no signal is present, the detector will see only VCO falling edges, so the comparator output will stay low , forcing the VCO to Fmin operating frequency.

Phase comparator ll is more susceptible to noise, however, causing the phase lock loop to unlock, if a noise pulse is seen on the signal input, the comparator treats it as another negative edge of the signal and will cause it to go high until the VCO falling edge is seen, potentially for a whole signal input period. This would cause the VCO to speed up during that time. When using the phase comparator l, the output of that phase detector would be disturbed for only the short duration of the spike and would cause less upset.

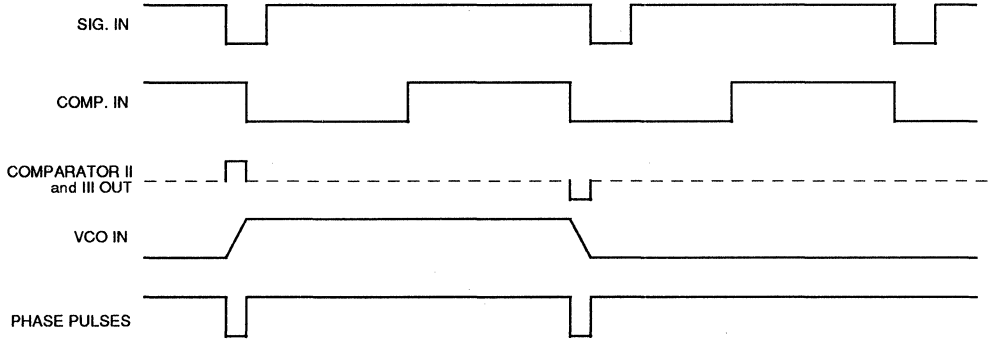
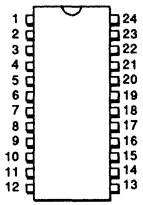


Figure 9. Typical Phase Comparator 11 and 111 Output Waveforms.

FEATURES

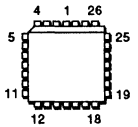
- ☐ CCITT G.721/ANSI T1.301 compatible
- ☐ 24 kBPS robbed-bit ADPCM mode
- ☐ 16 and 8 kBPS digital speech interpolation (DSI) modes
- ☐ Operates on 8 independent channels in 8 kHz frame
- ☐ Each channel individually configurable
- ☐ Accommodates μ-law (7- or 8-bit), A-law or 16-bit linear PCM input
- ☐ Power saving feature for unused channels

28-PIN DIP PACKAGE



SC11360CN

28-PIN PLCC PACKAGE

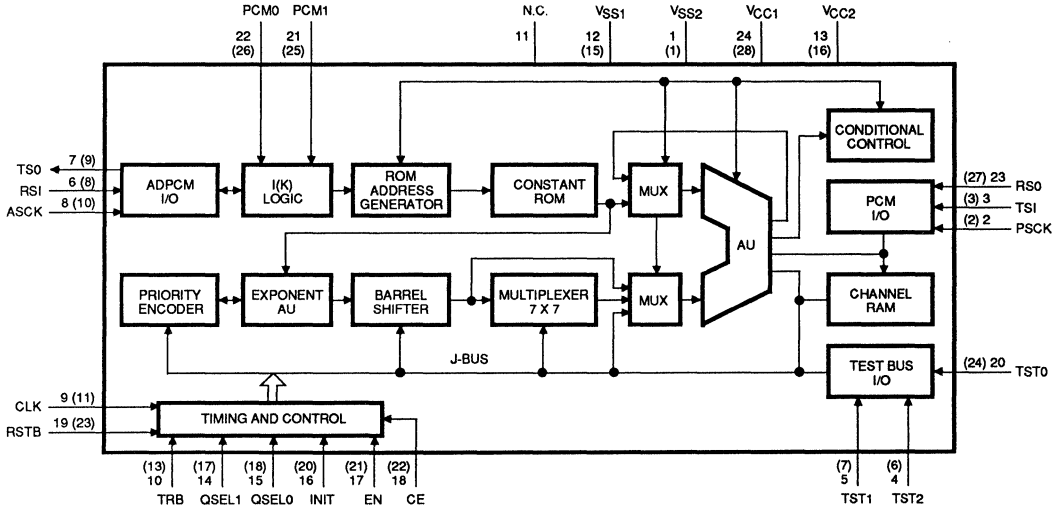


SC11360CV

GENERAL DESCRIPTION

The ADPCM processor was designed to provide fully compatible CCITT/ANSI 32 kBPS and 24 kBPS ADPCM transcoding. In addition to the standard algorithms, the processor also features 16, and 8 kBPS digital speech interpolation (DSI) algorithms. Designed for multichannel systems, the processor operates on 8 independent channels in a 8 kHz frame. Each channel is individually configurable, therefore supporting both full and half duplex operation. All input/output transfers occur on an interupt basis using serial, double buffered data registers. Additionally, the processor incorporates test modes and test pins for increased testability.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINS; NUMBERS IN ( ) ARE PLCC PINS. PINS (4), (5), (12), (14), & (19) ARE NOT CONNECTED.

PIN DESCRIPTIONS

PIN	NAME	I/O TYPE	DESCRIPTION
1 (1)	VSS2	Power	Ground
2 (2)	PSCK	Input	PCM Serial Clock. One serial data bit is transferred on both TSI and RSO while CE is active. The transfer depends on TRB.
3 (3)	TSI	Input	Transmit Serial Input. Transmitter PCM (8 bits) or linear (16 bits) input. Data is read on the falling edge of PSCK while CE and TRB are high.
4 (6)	TST2	Input	Test mode control bit 2. Connect to a logic 0 for normal operation.
5 (7)	TST1	Input	Test mode control bit 1. Connect to a logic 0 for normal operation.
6 (8)	RSI	Input	Receiver Serial Input. Receiver ADPCM (4 bits) input. Data is read on the falling edge of ASCK while CE is high and TRB is low.
7 (9)	TSO	Output	Transmitter Serial Output. Transmitter ADPCM (4 bits) output. Data is output after the rising edge of ASCK while CE is high following the processing of a transmitter.
8 (10)	ASCK	Input	ADPCM Serial Clock. One serial data bit is transferred on both TSO and RSI while CE is active. The transfer depends on TRB.
9 (11)	CLK	Input	Chip Clock (8.50 MHz). This clock does not need to be synchronous with any I/O operation. CE is synchronized internally.
10 (13)	TRB	Input	Transmitter/Receiver select. A logic 1 (0) indicates that the channel to be processed is a transmitter (receiver). TRB should be stable while CE is high.
11 (4,5,12,14,19)	NC		
12 (15)	VSS1	Power	Ground
13 (16)	VCC2	Power	+5.0 VDC
14 (17)	QSEL1	Input	Quantizer Select bit 1. See Table 1.
15 (18)	QSEL0	Input	Quantizer Select bit 0. See Table 1.
16 (20)	INIT	Input	Per channel initialization (active high). Read at the beginning of each channel, this pin causes the processor to disregard other control inputs and initialize the corresponding channel variables.
17 (21)	EN	Input	Enable channel processing (active high). Read at the beginning of each channel, this pin indicates whether the channel is active.
18 (22)	CE	Input	Chip Enable. This pin enables all data transfers when high. The falling edge is used as the start of a new channel (interrupt) and indicates when the channel control information (INIT, TRB, EN, PCM1, PCM0, QSEL1, and QSEL0) is read. CE should change when PSCK and ASCK are high.
19 (23)	RSTB	Input	Chip Reset (active low). A low to high transition initiates the reset sequence which initializes the channel variables for all 8 channels. RSTB = 1 for normal processing.
20 (24)	TST0	Input	Test mode control bit 0. Connect to a logic 0 for normal operation.
21 (25)	PCM1	Input	Selects μ-law or A-law. See Table 2.
22 (26)	PCM0	Input	Selects 7 or 8 bit μ-law. See Table 2.
23 (27)	RSO	Output	Receiver Serial Output. Receiver PCM (8 bits) or linear (16 bits) output. Data is output after the rising edge of PSCK following the processing of a receiver.
24 (28)	VCC1	Power	+5.0 VDC

Numbers in ( ) refer to 28-pin PLCC

QSEL1	QSEL0	LEVEL	MODE
0	0	15	32 KBPS ANSI/CCITT
0	1	7	24 KBPS ANSI (Proposed)
1	0	4	16 KBPS Proprietary
1	1	2	8 KBPS Proprietary

Table 1. ADPCM Algorithms

PCM1	PCM0	MODE (for TSI & RSO)
0	0	8 Bit μ-Law
0	1	7 Bit μ-Law
1	0	8 Bit A-Law
1	1	16 Bit Linear

Note: If A-law, the processor assumes even bit inversion for TSI & RSO.

Table 2. CODEC Interface

FUNCTIONAL DESCRIPTION

Adaptive Differential Pulse Code Modulation (ADPCM)

Adaptive Differential Pulse Code Modulation (ADPCM) is a class of waveform encoding techniques for voice and voice band data which provides "toll quality" performance at 32 kbps with reduced performance at lower rates. The use of ADPCM reduces channel bandwidth requirements from the 64 kbps PCM standard by a factor of two or more. In July 1986, the International Telegraphy and Telephone Consultative Committee (CCITT) approved Recommendation G.721 (1) a 32 kbps ADPCM standard.

The CCITT ADPCM algorithms is characterized by three structures; an adaptive predictor, an adaptive quantizer, and a synchronous coding adjuster. The adaptive predictor consists of both a second order recursive predictor and a sixth order non-recursive predictor. The use of a mixed recursive and non-recursive predictor allows for more efficient modeling of incoming speech and voice band data signals. The coefficients of the non-recursive predictor are updated using a simplified sign-sign technique. The coefficients of the recursive predictor are updated using an algorithm that ensures stability and prevents adaptation mistracking.

The ADPCM algorithm employs a 15-level non-uniform backward adaptive quantizer. The quantizer is sequentially adjusted using an algorithm that adapts slowly for voice band data and quickly for speech inputs.

The ADPCM algorithm includes synchronous coding adjustment to prevent cumulative quantization distortion in synchronous tandem codings. When a decoder is synchronously connected to an encoder, synchronous coding adjustment estimates the quantization in the encoder and compensates the decoder PCM value accordingly.

To allow for bit-robbed ADPCM transmission and lower transcoding rates, three additional quantizers were implemented following the general structure of the ADPCM specification. The only significant difference between these algorithms is the number of quantization levels in the adaptive quantizer. The seven-level quantizer was designed and optimized for use in bit-robbing application and 24 kbps transcoding. The four-level and two-level quantizers were optimized for use in a Digital Speech Interpolation (DSI) environment.

See the block diagram for the SC11360 ADPCM Transcoder Architecture.

I/O TIMING

Interrupt Timing

The ADPCM PROCESSOR operates on an interrupt basis, indicated by the falling edge of CE. CE is synchronized internally using a pulse synchronizer. The only relationship between the "asynchronous" I/O timing and CLK is the time between interrupts; however, the processing time is dependent on which mode the device is operating. Additionally, due to internal pipelining and uncertainty in the pulse synchronizer, CE must remain low long enough for an interrupt to be preocessed. Therefore, the constraints on CE are as follows:

a. The period of CE (falling edge to falling edge) must be greater than or equal to the number listed in Table 3 for the desired mode of operation.

b. CE must be low for at least 4 CLK cycles.

As an example, assume the processor processes 8 receivers in 125 μs. Further, assume the environment is a T1 based system where the I/O timing is related to 1.544 MHz. Most channels (from the chip's point of view) are contained in twenty-four (24) 1.544 MHz periods. This period is 15.54 μs. According to Table 3, CE can have a period of 131 CLK cycles; therefore, the processor clock rate should be: (131/15.54) MHz = 8.43 MHz. Allowing for jitter and inaccuracies in the CLK rate, a nominal frequency of 8.5 MHz was chosen.

Figure 2 provides a block diagram for the I/O Structure, and Figure 3 illustrates timing for Full Duplex Operation.

Data Interface

Figure 4 shows the I/O structure. The ADPCM processor uses serial double buffered registers for all data transfers. All data and control signals are transferred on an interrupt basis. CE should change only when the data clocks (ASCK & PSCK) are high. ASCK and PSCK need only be valid while CE is high. TRB determines which input register is loaded and which output register is enabled.

Because of the varying data lengths, Tables 4–7 are shown on the following pages.

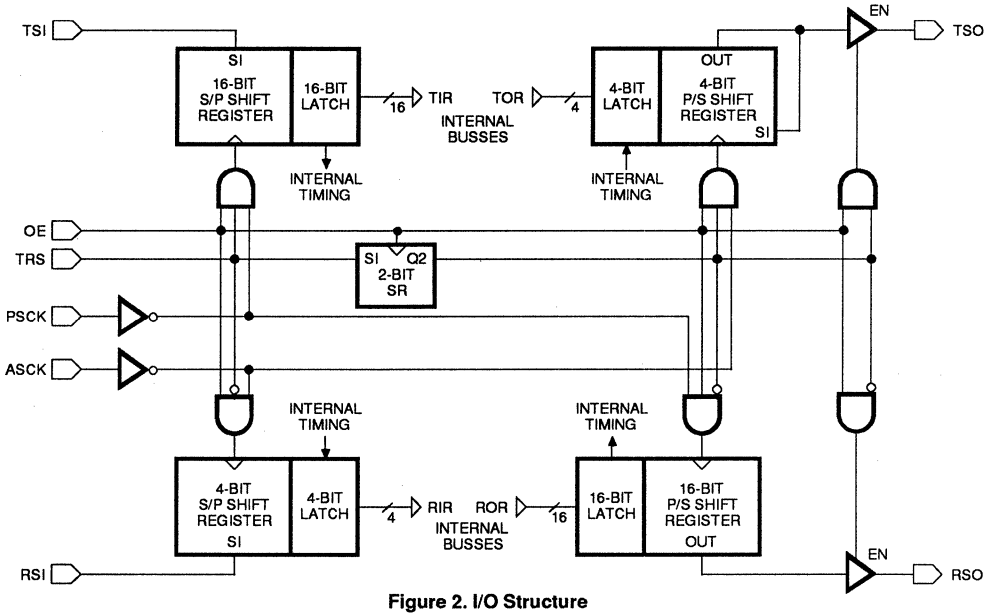


Figure 2. I/O Structure

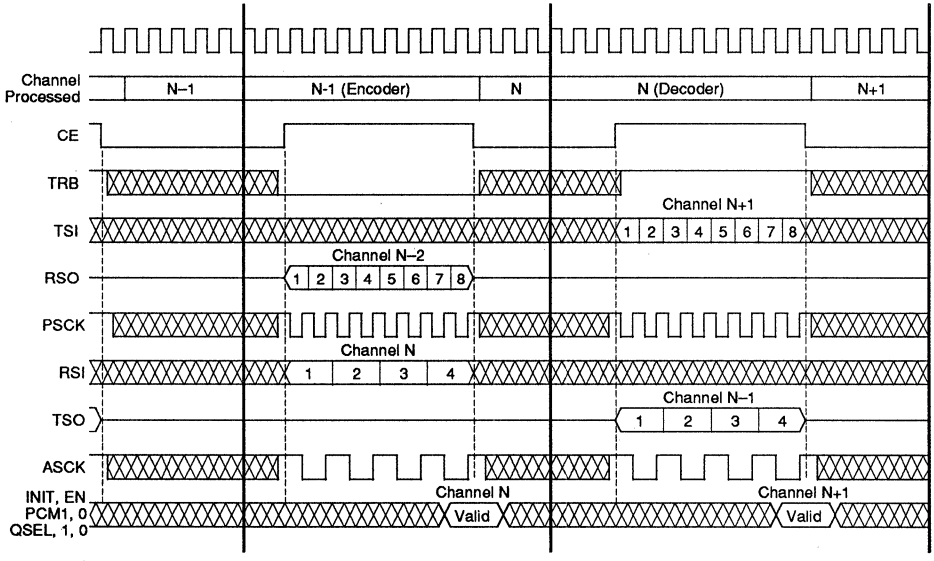


Figure 3.

MODE OF OPERATION	# OF CLK CYCLES
Transmitter—Log PCM	125
Transmitter—Linear	127
Receiver—Log PCM	131
Receiver—Linear	114
Initialized (INIT = 1)	27
Disabled (EN = 0)	4

Table 3. Maximum Processing Time

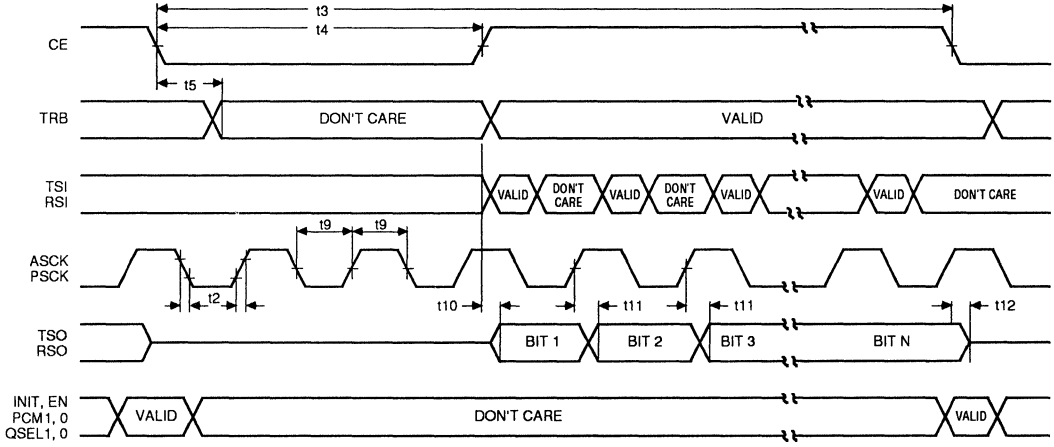
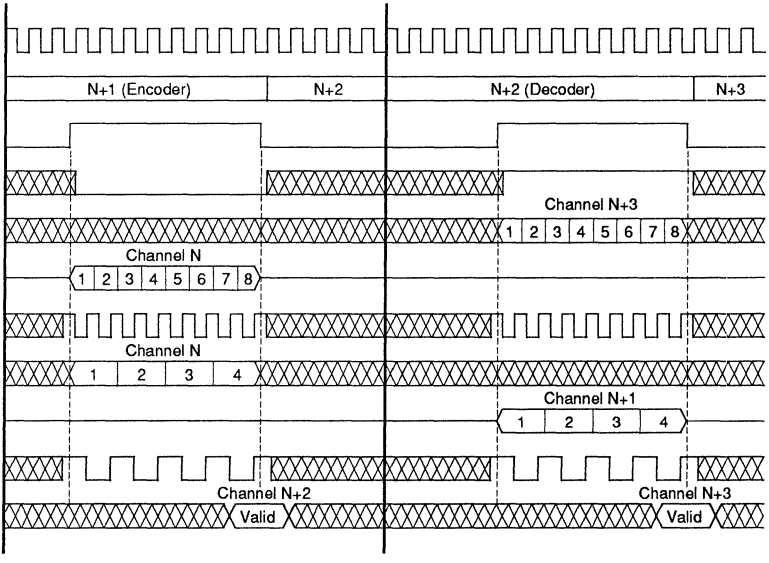


Figure 4. I/O Timing Parameters



Full Duplex Timing

PCM1	PCM0	MODE	ORDER OF BITS TRANSFERRED 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	8 Bitμ-law	x	x	x	x	x	x	x	x	7	6	5	4	3	2	1	0
0	1	7 Bit μ-law	x	x	x	x	x	x	x	x	7	6	5	4	3	2	1	*
1	0	8 Bit A-law	x	x	x	x	x	x	x	x	7	6	5	4i	3	2i	1	0i
1	1	16 Bit Linear	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 4. PCM Data Input (TSI)

Notes:

a) The above table assumes 16 PSCK periods occur while CE is high. For other cases, the falling edge of CE should be used as a reference: the last bit input prior to the falling edge of CE should be the LSB of the data word.

b) For μ-law and A-law, bit 7 is the sign bit and bit 0 is the LSB. The "x" denotes a don't care state. At least eight (8) bits must be loaded into TSI; the last 8 bits transferred must conatin the LOG PCM word.

c) For μ-law, "S" is the signaling bit. It must be clocked in TSI, but is not used internally.

d) For A-law, the "i" denotes the even bit inversion.

e) For linear, the 16 bits is assumed to be 14 bit sign extended two's complement. At least eight (8) bits must be loaded into TSI; the last 16 bits transferred must contain the PCM word.

PCM1	PCM0	MODE	ORDER OF BITS TRANSFERRED 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	8 Bitμ-law	7	6	5	4	3	2	1	0	x	x	x	x	x	x	x	x
0	1	7 Bit μ-law	7	6	5	4	3	2	1	sx	x	x	x	x	x	x	x	x
1	0	8 Bit A-law	7	6i	5	4i	3	2i	1	0i	x	x	x	x	x	x	x	x
1	1	16 Bit Linear	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 5. PCM Data Output (RSO)

Notes:

a) The above table assumes 16 PSCK periods occur while CE is high. For other cases, the rising edge of CE should be used as a reference: the first bit output following the rising edge of CE will be the sign of the data word. If more than 16 bits are transferred, the output repeats, starting with the sign bit.

b) For μ-law and A-law, bit 7 is the sign bit and bit 0 is the LSB. The "x" denotes an unknown state.

c) For 7 bit μ-law, "sx" designates the signaling bit position. It is an unknown state. EXTERNAL CIRCUITS must re-insert the signaling bit.

d) For A-law, the "i" denotes the even bit inversion.

e) For linear, the 16 bits is 14 bit sign extended two's complement.

QSEL1	QSEL0	MODE	ORDER OF BITS TRANSFERRED 1	2	3	4	5	6	7	8
0	0	32 KBPS	3	2	1	0	3	2	1	0
0	1	24 KBPS	2	1	0	x	2	1	0	x
1	0	16 KBPS	1	0	x	x	1	0	x	x
1	1	8 KBPS	0	x	x	x	0	x	x	x

Table 6. ADPCM Data Input (RSI)

Notes:

a) The above table assumes 8 ASCK periods occur while CE is high. For other cases, the falling edge of CE should be used as a reference: the last bit input prior to the falling edge of CE should be the LSB of the data word. Normally, only 4 bits need to be transferred.

b) "x" denotes a don't care state.

QSEL1	QSEL0	MODE	ORDER OF BITS TRANSFERRED 1	2	3	4	5	6	7	8
0	0	32 KBPS	3	2	1	0	3	2	1	0
0	1	24 KBPS	2	1	0	x	2	1	0	x
1	0	16 KBPS	1	0	x	x	1	0	x	x
1	1	8 KBPS	0	x	x	x	0	x	x	x

Table 7. ADPCM Data Output (TSO)

Notes:

a) The above table assumes 8 ASCK periods occur while CE is high. For other cases, the rising edge of CE should be used as a reference: the first bit output following the rising edge of CE will be the sign of the data word. If more than 4 bits are transferred, the output repeats, starting with the sign bit. Normally only 4 bits need to be transferred.

b) "x" denotes an unknown state.

Control information (INIT, EN, PCM1, PCM0, QSEL1, QSEL0, & TRB) is presented at the interrupt time. Each channel can be configured for any quantizer or PCM format as long as the following conditions are met:

a) The number of data bits transferred meets the requirements of Tables 4–7; and

b) The correct input register was loaded prior to the interrupt. Selection of input register is via TRB when CE is high.

TSO and RSO have tri-state outputs which are enabled if CE is high and the previous channel processed was a transmitter or a receiver, respectively. See Figure 3 & 4.

Reset Sequence

The ADPCM processor includes circuitry to permit a single pin to initialize the ADPCM channel variables for all 8 channels. This feature is intended to be used for power up initialization as well as to aid IC and PC board testing. The reset sequence requires the pin RSTB to be held low for two (or more) CLK cycles followed by at least 216 CLK cycles with RSTB held high. To begin normal processing, CE must first make a low to high transition. Once this has been done, the processor can not accept interrupts (high to low transitions of CE). RSTB is held high for normal processing.

Channel NOP

When a channel is disabled (EN = 0), the processor requires 4 cycles to maintain all channel variables in addition to placing the data output ports in a known state. After this the processor waits for the next interrupt. Power is conserved during this time by disabling the internal CHANNEL RAM. TSO and RSO output the following data after a channel NOP:

QSEL1	QSEL0	MODE	TSO			
0	0	32 KBPS	0	0	0	0
0	1	24 KBPS	0	0	0	x
1	0	16 KBPS	0	0	x	x
1	1	8 KBPS	0	x	x	x

Table 8. ADPCM Output (NOP)

PCM1	PCM0	MODE	RSO															
0	0	8 Bitμ-law	1	1	1	1	1	1	1	1	–	–	–	–	–	–	–	–
0	1	7 Bit μ-law	1	1	1	1	1	1	1	x	–	–	–	–	–	–	–	–
1	0	8 Bit A-law	1	1	0	1	0	1	0	1	–	–	–	–	–	–	–	–
1	1	16 Bit Linear	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 9. PCM Output (NOP)

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (See note below)

Supply Voltage, V_{CC}	+6V
Input Voltage	$-0.6\ V_{SS}$ to $V_{CC}+0.6$ V
Storage Temperature Range	–65 to +150°C
Maximum Power Dissipation @ 25°C	500 mW
Lead Temperature (Soldering 10 s)	300°C
Operating Temperature Range	0 to 70°C

Note: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating temperature range, the device should not be operated at these limits. The Table of Electrical Characteristics provides actual operating limits.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC1} & V_{CC2}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS1} & V_{SS2}	Ground		0	0	0	V
I_{CC}	Supply Current			60		mA
P_D	Total Power Dissipation	Includes Loading on Outputs		330		mW
I_L	Leakage Current	All Inputs & Tri-state Outputs	–10		+10	µA
V_{IL}	Logic "0" All Inputs			0.8		V
V_{IH}	Logic "1" All Inputs		2.0			V
V_{OL}	Logic "0" All Outputs	I_{OL} = +4 mA	V_{SS}		0.8	V
V_{OH}	Logic "1" All Outputs	I_{OH} = –0.4 mA	V_{CC}–0.8		V_{CC}	V
C_I	Input Capacitance				10	pF
C_O	Output Capacitance				10	pF
C_L	Load Capacitance				100	pF

AC CHARACTERISTICS

(@ $V_{CC1} = V_{CC2} = 5.0\ V \pm 5\%$, $V_{SS1} = V_{SS2} = 0\ V$, $T_A = 0$ to 85°C)
(All outputs loaded with 100 pF. All input rise and fall times 10 ns, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
f1	CLK Frequency	Assuming 50% Duty Cycle		8.5	9.0	MHz
t1	CLK High & Low Times		55	59		ns
t2	Rise & Fall Times (CLK, CE, ASCK, PSCK)			5	10	ns
t3	CE Period (rov—LOG PCM)		131			CLK Cycles
t4	CE Pulse Width Low		4			CLK Cycles
t5	TRB Hold Time	ref: CE (–)	20			ns
t6	TRB Setup Time	ref: ASCK (–) & PSCK (–)	20			ns
t7	TSI and RSI Setup Times	ref: ASCK (–) or PSCK (–)	20			ns
t8	TSI and RSI Hold Times	ref: ASCK (–) or PSCK (–)	20			ns
t9	PSCK, ASCK High & Low Times		55			ns
t10	TSO & RSO Turn On Time (Tri-state to Valid Data)	ref: CE (+)	20		40	ns
t11	TSO & RSO Prop. Delay	ref: ASCK (+) or PSCK (+)			40	ns
t12	TSO & RSO Turn Off Time (Valid Data to Tri-state)	ref: CE (–)			20	ns
t13	Control Info. Setup Time	ref: CE (–)	20			ns
t14	Control Info. Hold Time (INIT, EN, PCM1, PCM0, QSEL1, QSEL0)	ref: CE (–)	20			ns
t15	RSTB Pulse Width Low		2			CLK Cycles

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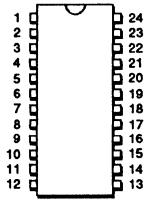
SIERRA SEMICONDUCTOR

SC22318
Programmable Frequency Synthesizer (PFS)

FEATURES

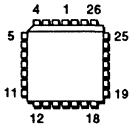
- ☐ Output frequencies up to a maximum of 100 MHz.
- ☐ High resolution frequency synthesis.
- ☐ Digitally programmable high resolution phase locked frequency.
- ☐ Fixed frequency configuration by storing divide ratios in an on chip EEPROM.
- ☐ Dynamically programmable frequency.
- ☐ Low current EEPROM programming (Typ. = 10 µA).
- ☐ External selection between EEPROM and REGISTER DATA.
- ☐ Microprocessor compatible serial digital interface.
- ☐ 24-pin DIP or 28-pin PLCC.

24-PIN DIP PACKAGE



SC22318CN

28-PIN PLCC PACKAGE

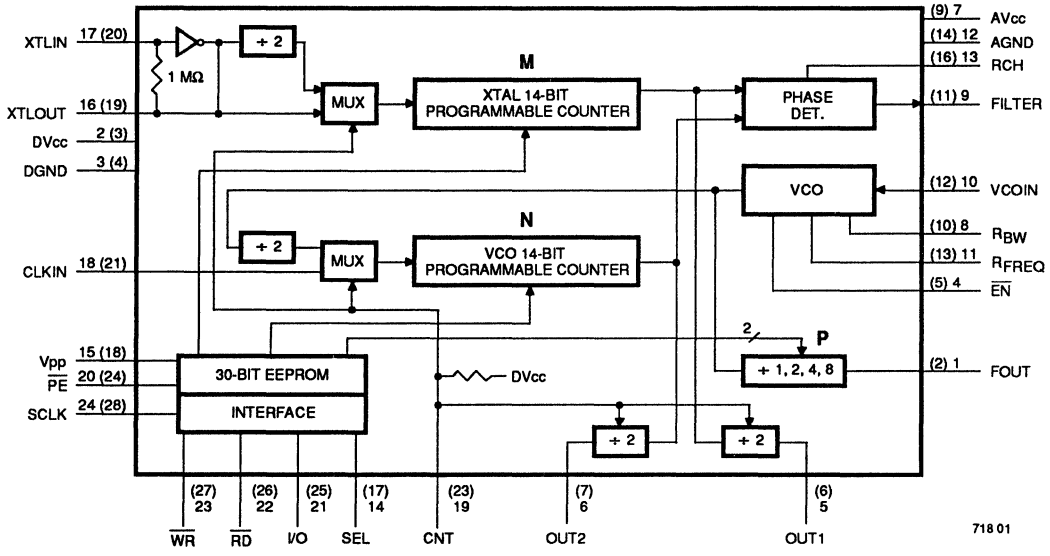


SC22318CV

GENERAL DESCRIPTION

The SC22318 is a CMOS Frequency Synthesizer. This part utilizes two 14-bit programmable Counters, an on chip oscillator (which requires an external crystal), a voltage-controlled oscillator and a phase detector to generate a 1 MHz to 100 MHz clock. The SC22318 can be digitally programmed through a serial interface to provide clock frequencies with an accuracy of 14-bits. The device can be implemented in a fixed configuration with the counter divide ratios stored in an on chip EEPROM. In a microprocessor based system, it can be dynamically programmed to the application requirement. The part can also be operated as two independently programmable 14-bit dividers. The SC22318 is available in both 24-pin DIP and 28-pin PLCC packages.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINOUTS. NUMBERS IN ( ) ARE PLCC PINS.

Figure 1.

PIN DESCRIPTION

PIN NO. DIP	PIN NO. PLCC	PIN NAME	FUNCTION
1	2	FOUT	Voltage controlled oscillator output.
2	3	DVcc	Digital power supply.
3	4	DGND	Digital ground.
4	5	$\overline{EN}$	VCO enable pin (Active low).
5	6	OUT1	Output of divider "M".
6	7	OUT2	Output of divider "N".
7	9	AVcc	Analog power supply.
8	10	R_{BW}	Resistor to set VCO bandwidth (driven by VCOIN).
9	11	FILTER	Phase locked loop filter.
10	12	VCOIN	Input of VCO.
11	13	R_{FREQ}	Resistor to set VCO free running frequency (R_{FREQ}).
12	14	AGND	Analog ground.
13	16	RCH	Resistor to set the charge pump current (1.25 V).
14	17	SEL	Memory select pin. For SEL = high, source of divide ratios is the E^2 memory. For SEL = low, source of divide ratios is temporary registers.
15	18	Vpp	EEPROM programming high-voltage pin. In normal operation this pin should be connected to DVcc. It is ramped to a high voltage only when the EEPROM is to be programmed.
16	19	XTLOUT	Crystal oscillator output pin. XTLOUT and XTLIN connect to a crystal to generate a crystal locked clock for the chip. If a suitable clock is already available in the system the XTLIN pin can be driven.
17	20	XTLIN	Crystal oscillator input pin.
18	21	CLKIN	Input to divider "N".
19	23	CNT	Straight divider select pin. When CNT = low, PLL mode is disabled and straight divider mode is enabled.
20	24	$\overline{PE}$	Program enable pin (Active low).
21	25	I/O	Serial interface input/output.
22	26	$\overline{RD}$	Serial interface read signal. During low period of this signal the data in the internal shift register is shifted out through the I/O pin.
23	27	$\overline{WR}$	Serial interface write signal. During low period of this signal the data is shifted in the internal shift register from the I/O pin.
24	28	SCLK	Serial interface clock signal.

FUNCTIONAL DESCRIPTION

Chip Architecture

The block diagram of the SC22318 is shown on Page 1 Fig. 1. It consists of two programmable 14-bit dividers, a crystal oscillator, a Phase-Locked Loop (PLL) system, a serial microprocessor interface, an EEPROM section and a Post-scaler 2 bit divider. The two 14-bit programmable counters divide the outputs of the oscillator and VCO by "M" and "N" respectively, where "M" and "N" are two integer numbers in the range of 1 to 16,383. The divided outputs are phase-locked to each other by the PLL circuit. The output of the VCO is then divided by the post-scaler modulo "P", where "P" can have a value of 1, 2, 4 or 8. For operation in the range between 1 and 10 MHz the post scaler is required. Above 10 MHz, the post scaler can be used to improve the jitter performance. The output frequency, F_{OUT}, can be calculated as follows:

$F_{OUT} = F_{VCO}/P$
$= [N/(M \times P)] \times F_{OSC}$

F_{VCO} = VCO Frequency

F_{OSC} = Oscillation frequency

M, N range from 1 to 16,383 and P = 1, 2, 4 or 8.

The M and N counters need 16 bits for programming (two bits of address and 14 bits of data), and the P scaler needs 2 bits. These bits can be loaded into the temporary registers that can be addressed through the serial interface. After the desired frequency is achieved, the data from the temporary registers can be transferred into the EEPROM memory for permanent storage. The chip uses a four pin serial interface for communications.

Circuit Description

Phase-Locked Loop (PLL) Circuit

The PLL circuit consists of a voltage controlled oscillator (VCO), a phase detector circuit, a charge-pump and an external loop-filter. The VCO center frequency and bandwidth are determined by the two external resistors R_{FREQ} and R_{BW}, respectively. V_{VCOIN} represents the VCO input voltage from the loop-filter.

Choosing suitable R_{FREQ} and R_{BW} (bandwidth) values can be accomplished using several different iterative methods. Below are several defining equations and one method for choosing R_{FREQ} and R_{BW}. Note that F_{VCO} is the input frequency of the post-scaler. In general, F_{VCOMIN} should be greater than 10 MHz, F_{VCOMAX} should be less than 100 MHz and F_{VCOMAX}/F_{VCOMIN} should not exceed EQ. 3, which can range typicallyfrom 1 to 3.

DEFINING EQUATIONS:

EQ. 1

$$I_{BIAS} = \frac{V_{VCOIN}}{R_{BW}} + \frac{2.2V}{R_{FREQ}}$$

V_{VCOIN} typically can range from 1V to 3V; 2V is nominal.

EQ. 2

$$F_{VCO} = \frac{1000}{\frac{4400}{I_{BIAS}} + 3}$$

EQ. 3

$$\frac{F_{VCOMAX}}{F_{VCOMIN}} = \frac{V_{VCOMAX} + 2.2\,\frac{R_{BW}}{R_{FREQ}}}{V_{VCOMIN} + 2.2\,\frac{R_{BW}}{R_{FREQ}}}$$

Outlined below is a method for calculating R_{FREQ} and R_{BW} using EQ. 1 and EQ. 2.

Step 1. Choose the desired F_{VCOMIN} and F_{VCOMAX}.

Step 2. Calculate $I_{BIASMIN}$ and $I_{BIASMAX}$ using EQ. 4 and EQ.5.

EQ. 4

$$I_{BIASMIN} = \frac{4400}{\frac{1000}{F_{VCOMIN}} - 3}$$

EQ. 5

$$I_{BIASMAX} = \frac{4400}{\frac{1000}{F_{VCOMAX}} - 3}$$

Step 3. Calculate R_{BW} by using EQ. 6 and subtracting $I_{BIASMAX}$ from $I_{BIASMIN}$.

EQ. 6

$$R_{BW} = \frac{V_{COMAX} - V_{COMIN}}{I_{BIASMAX} - I_{BIASMIN}} = \frac{3V - 1V}{\Delta I_{BIAS}}$$

Step 4. Calculate R_{FREQ} using EQ. 7.

EQ. 7

$$R_{FREQ} = \frac{2.2V}{I_{BIASMAX} - \frac{3V}{R_{BW}}}$$

R_{BW} in MΩ, I_{BIAS} in μA

Step 5. If either R_{FREQ} or R_{BW} is negative, then choose a smaller ΔF_{VCO} and repeat steps 1 through 4.

The PLL incorporates phase/frequency detector (PFD) logic. A charge pump is used to convert the logic states of the PFD into analog signals suitable for controlling the VCO. The charge pump current is determined by the external resistor RCH, and its value is given by:

ICH = 1.25V/RCH; RCH ~1.6 KΩ

A filter is added after the charge-pump to smooth the VCO control voltage. Figure 2 shows the complete PLL circuit. The states of the PFD are determined by the edges of the input wave-form. If the R-input (reference) phase leads the V-input (VCO) phase, then an edge of the R input sets the U (up) terminal true. The next V edge resets the U terminal false. Conversely, if V leads R, a V edge sets D (down) true and the next R edge resets D false. Both U and D can be false simultaneously, or either one alone can be true, but both can never be true simultaneously. Therefore a PFD has three allowable states at its output terminals, up (U), down (D) and neutral(N).

A typical circuit for the charge-pump and two possible loop-filters are shown in Figure 3. The loop filter consisting of the simple resistor capacitor combination has the disadvantage of having some granularity effect. Upon each cycle of the PFD, the pumping current Ip is driven into the filter impedance which responds with an instantaneous voltage jump of delta (Vc) = ICH*R2.

At the end of the charging interval, the pump current switches off and a voltage jump of equal magnitude occurs in the opposite direction. The frequency of the VCO follows the voltage steps so there will be frequency excursion. The second loop filter has an additional capacitor C3 is parallel with the R2-C2 impedance. Because of this capacitor, the VCO control voltage has a continuous ramp-like, exponential function for each pump pulse, instead of the rectangular jump that is present in the filter without the additional capacitor.

Modulo Storage Unit

Each counter needs 16 bits for programming, out of which 2 bits are for the destination's address and 14 are for data bits (see Table 1 and 2). The programming bits are loaded into the chip through the serial interface and are stored in temporary registers. After the optimum frequency is achieved, the programming bits can be transferred into non-volatile EEPROM memory, the permanent storage unit for all three dividers is shown in Figure 4.

The source of the control bits for the dividers can be switched between temporary registers and EEPROM memory by the signal labeled SEL which is brought out to a pin.

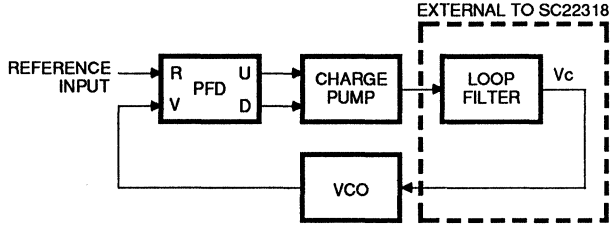


Figure 2. PLL with Three-State Phase Detector and Charge Pump

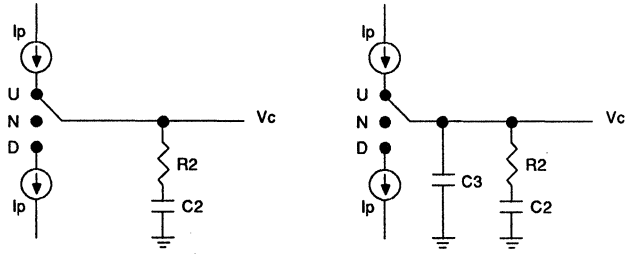


Figure 3. Charge Pumps and Loop Filters

A1	A0	DESTINATION
0	0	P (D0–D1)
0	1	N (D0-D13)
1	0	M (D0–D13)
1	1	Reserved

Table 1.

Note: When writing to the P Register D2 to D13 = 0, see Table 2 for D0, D1 values.

D1	D0	DATA
0	0	÷1
0	1	÷2
1	0	÷4
1	1	÷8

Table 2.

Note: This table is for use with the P Register only.

D13	...	D3	D2	D1	D0	DATA
0		0	0	0	0	÷1
0		0	0	0	1	÷1
0		0	0	1	0	÷2
0		0	1	0	0	÷4
						⋮
1		0	0	0	0	÷8192
	...					⋮
1		1	1	1	1	÷16383

Table 3.

Note: This table is for use with the M and N register.

Programming EEPROM

The EEPROM can be programmed by enabling $\overline{PE}$ low. The Vpp pulse must be a 16V pulse with controlled rise and fall times as shown in Figure 5. During the program cycle, the contents of the temporary registers of all three dividers are written into the EEPROM. After the programming is completed Vpp should be returned to Vcc(5V). The SEL pin is used to control the selection between temporary registers and EEPROM. When SEL is low the temporary registers are selected and when SEL is high the EEPROM becomes the source of the divide ratios.

Serial Interface

The divider programming data is stored in the internal temporary register through a four pin serial interface. When $\overline{WR}$ goes low, sixteen bits of data are shifted serially into the chip through the I/O pin.The sixteen bits constitute fourteen bits of programming data and two bits of destination address. The data is sampled on the rising edge of the shift clock (SCLK). When $\overline{WR}$ goes high, the contents of the memory location selected by the two bit destination address is updated by the fourteen bit data. For proper operation of the interface, there has to be exactly sixteen SCLK pulses within the $\overline{WR}$ high-to low and low to high transition period. After $\overline{WR}$ goes high, an additional 10 SCLK pulses are required to load the new data. Also, the first Write after a Power Up requires 10 SCLK pulses before $\overline{WR}$ goes low. After the 10 SCLK pulses, the user can read the data into the temporary register or EEPROM memory by controlling the SEL pin. Every read of a selected location should be preceded by a write into the same location. To read the data out, The $\overline{RD}$ signal should be pulled low. After sixteen clock pulses all the data inside the shift register will be clocked out of the I/O pin. The data appears at the output, on the rising edge of the shift clock (SCLK). To avoid conflicts, the falling edge of the $\overline{RD}$ signal should be at least ten SCLK periods away from the rising edge of $\overline{WR}$.

The same rule applies to consecutive write cycles. The serial interface timing diagram is shown in Figure 6 and Figure 7.

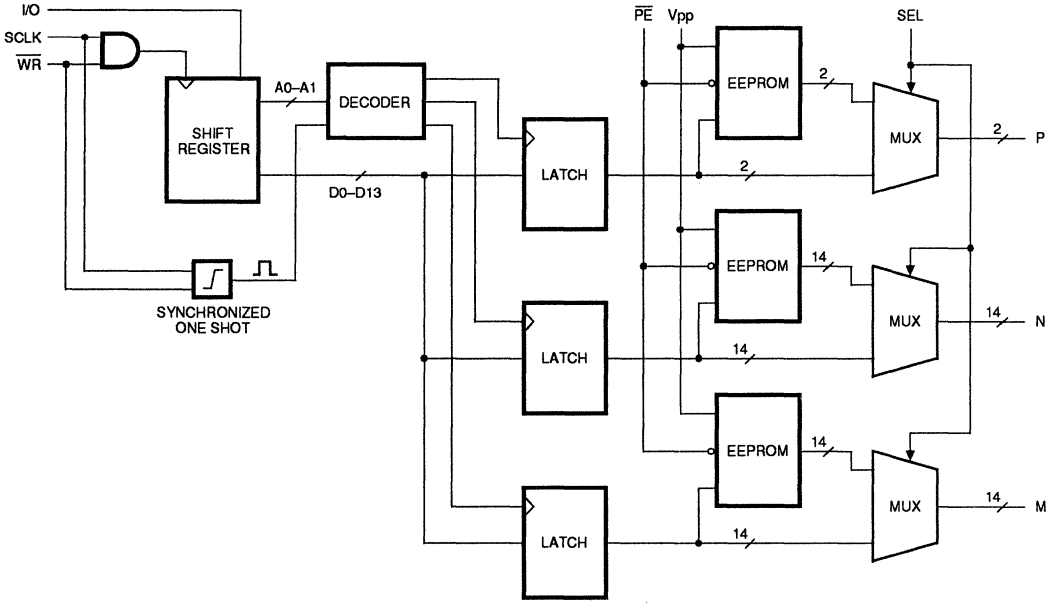


Figure 4. Storage Unit For Programming of Dividers

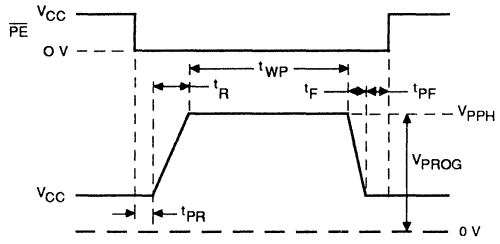


Figure 5. EEPROM Programming Timing Waveforms

EEPROM PROGRAMMING TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{PR}	$\overline{PE}$ Low to Initiation of Vpp	0			ns
t_R	Vpp Rise Time	4		20	mV/µs
t_{WP}	Duration of Vpp High	5		20	ms
t_F	Vpp Fall Rate	4		20	V/µs
t_{PF}	Vpp Low to $\overline{PE}$ High	0			ns
V_{PROG}	Programming Voltage (Ref:GND)	+15.5	+16.0	+16.5	V

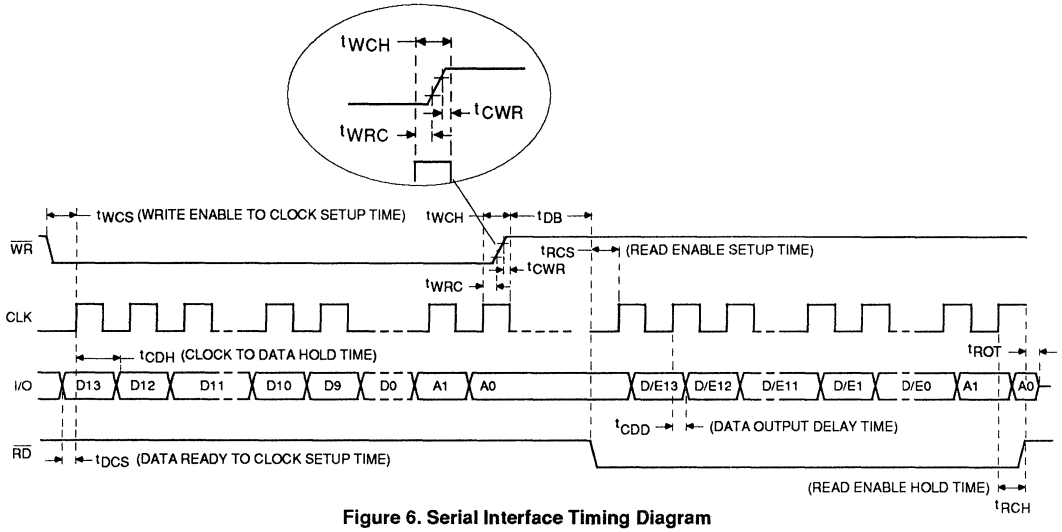


Figure 6. Serial Interface Timing Diagram

SERIAL INPUT TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{WCS}	Write Enable to Clock Set Up Time	50			ns
t_{DCS}	Data Ready to Clock Set-Up Time	50			ns
t_{CDH}	Clock to Data Hold Time	50			ns
t_{CWR}	Clock to Write Enable Raising Edge	40			ns
t_{WRC}	Write Enable Raising Edge to Clock	40			ns
t_{WCH}	Clock to Write Enable Hold Time	50			ns
t_{DB}	The number of SCLK periods after Power Up, before the first Write Cycle and after aech Write Cycle	10			SCLK Periods
t_{RCS}	Read Enable to Clock Set-up Time	50			ns
t_{CDD}	Clock to Data Output Delay Time			75	ns
t_{RCH}	Clock to Read Enable Hold Time	75			ns
SCLK	Clock Frequency			5	MHz
t_{ROT}	Read Enable High to Output Tristate			50	ns

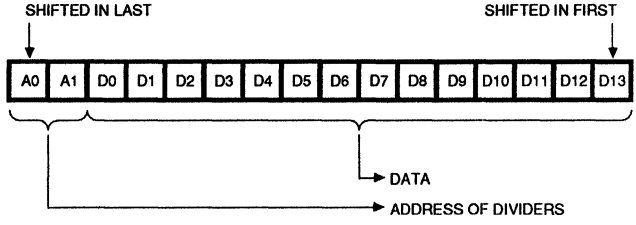


Figure 7. Address/Data Allocations for the Input Bits

CRYSTAL CONNECTION

Figure 8 shows a typical crystal implementation. The capacitors C1 and C2 have a range of 20pF to 5 pF. Depending on the frequency of the crystal, it is recommended to use maximum 20 pF for frequencies lower than 10 MHz, and for frequencies above 10 MHz capacitor values between 10pF and 5 pF are recommended.

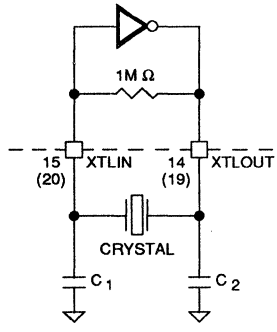


Figure 8. Typical Crystal Implementation

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, Vcc–GND	6 V
DC Input Voltage	GND–0.5 to Vcc +0.5 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 sec.)	300°C

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
Ta	Ambient Temperature		0		70	°C
Vcc	Positive Supply Voltage		4.5	5.0	5.5	V
GND	Ground			0		V
XTLIN, XTLOUT	Crystal Frequency			20	30	MHz
Tr,Tf	Input Rise or Fall Time				50	ns

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package –12mW/°C from 65–85°C

DC ELECTRICAL CHARACTERISTICS (Ta = 0 TO 70°C, DVcc = 5V ±10%, AVcc = 5V ±10%)

PARAM.	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNITS
Icc	Quiescent Current			30		mA
Vih	High Level Input Voltage, All Inputs		2.2			V
Vil	Low Level Input Voltage, All Inputs				.8	V
Voh	High Level Output, All Outputs Except XTLOUT (Ioh = 0.5 mA) (Ioh = 100 µA)		 2.4 4.5			 V V
Vol	Low Level Output, All Outputs Except XTLOUT (Iol = 1.6 mA) (Iol = 100 µA)				 0.6 0.2	 V V
Voh	High Level Output XTLOUT (Ioh = 20 µA)		 4			 V
Vol	Low Level Output XTLOUT (Iol = 20 µA)				 0.2	 V
Ipp	Programming Current	Vpp = 5 V		10		µA
		Vpp = 16 V		25		µA

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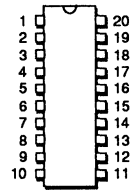
FEATURES

- ☐ Digitally programmable switched-capacitor filter sections to obtain different filter responses including high-pass, low-pass, band-pass, notch, and all-pass types.
- ☐ Dynamically programmable for adaptive filtering applications.
- ☐ Microprocessor compatible serial digital interface.
- ☐ Low power consumption.
- ☐ Fixed filter configurations by storing filter coefficients in an on-chip Electrically Erasable (E^2)PROM.
- ☐ Digitally programmable filter clock frequency.
- ☐ Two uncommitted operational amplifiers available for use as anti-aliasing and/or smoothing filters.
- ☐ 20-pin DIP.

20-PIN DIP PACKAGE

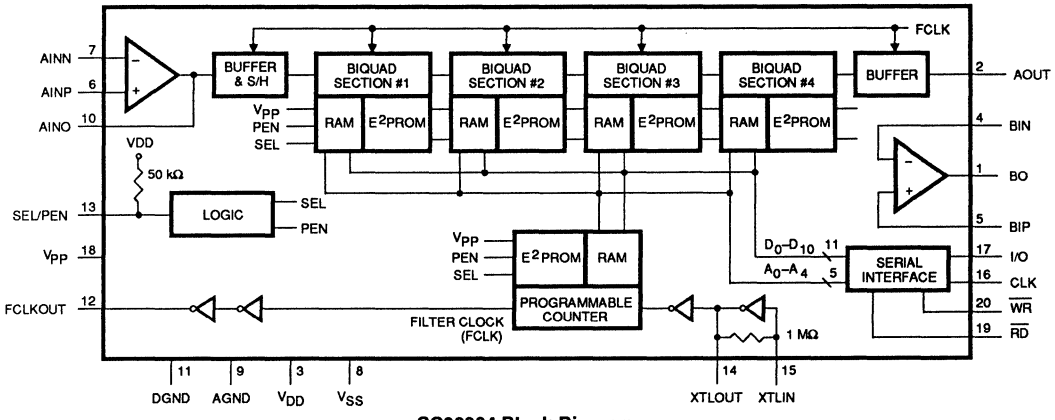


SC22324CN
SC22322CN

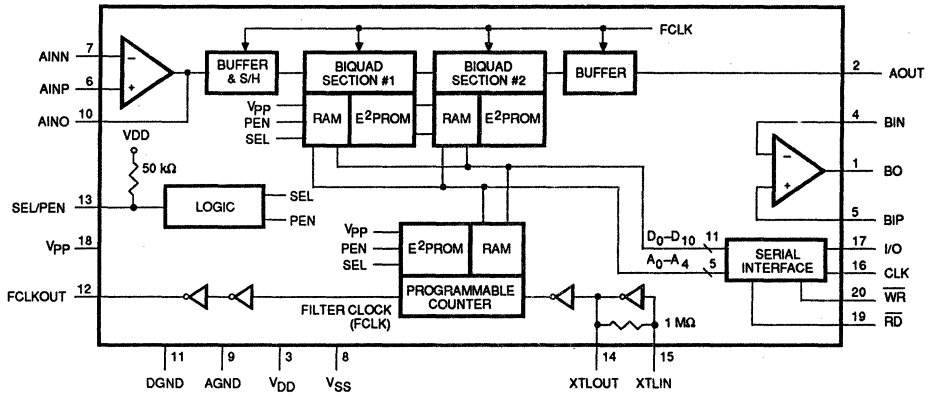
GENERAL DESCRIPTION

The SC22324/2 are CMOS quad/dual second-order programmable universal switched-capacitor filters. They can be digitally programmed through a serial interface to provide a variety of combinations of high-pass, low-pass, band-pass, notch and all-pass filter functions without a need for any external components. The device can be cascaded to provide higher order filter functions. The SC22324/2 can be implemented in a fixed configuration with the filter parameters stored in an on-chip E^2PROM. Or, in a microprocessor based system, it can be dynamically configured to the application requirement. The clock for the filters is provided from an on-chip oscillator that needs an external crystal, with an internal programmable digital counter. For fixed filter configurations, the divider ratio for the counter can be stored in the on-chip E^2PROM. The SC22324/2 are supported by easy to use development tools and design software to assist the implementation of the required filter responses. Both devices are fabricated in a CMOS process and are available in a 20-pin DIP.

BLOCK DIAGRAM



SC22324 Block Diagram



SC22322 Block Diagram

PIN DESCRIPTIONS

PIN NO.	PIN NAME	FUNCTION
1	BO	Uncommitted op amp output.
2	AOUT	Analog output of programmable filter.
3	V_{DD}	Positive power supply pin. V_{DD} = +5 V ±10%
4	BIN	Uncommitted op amp negative input.
5	BIP	Uncommitted op amp positive input.
6	AINP	Uncommitted op amp positive input.
7	AINN	Uncommitted op amp negative input.
8	V_{SS}	Negative power supply pin. V_{SS} = –5 V ±10%
9	AGND	Analog ground. All analog signals are referenced to this pin.
10	AINO	Uncommitted op amp output node.
11	DGND	Digital ground. All digital signals are referenced to this pin.
12	FCLKOUT	Filter clock out. Buffered filter clock output.
13	SEL/PEN	Memory select/program enable pin. This is a tri-level input pin. For SEL/PEN = 0 V, the temporary registers are selected as the programming source for the filter. For SEL/PEN = V_{DD}, the source is switched to the E^2 memory. When SEL/PEN = V_{SS}, the E^2 programming is enabled. This pin has an internal pull up. If left open it will be pulled to V_{DD}.
14	XTLOUT	Crystal oscillator output pin. XTLOUT and XTLIN connect to a crystal to generate a crystal locked clock for the chip. If a suitable clock is already available in the system the XTLIN pin can be driven.
15	XTLIN	Crystal oscillator input pin. Refer to pin 14 for details.
16	CLK	Input shift clock. This clock shifts the data in or out of the I/O pin after the falling edge of $\overline{WR}/\overline{RD}$.
17	I/O	Serial interface input/output pin.
18	V_{PP}	E^2 programming high-voltage source. In normal operation this pin should be connected to V_{SS}. It is ramped to a high voltage only when the E^2 PROM is to be programmed.
19	$\overline{RD}$	Serial interface read signal. During the low period of this signal the data in the internal shift-register starts to shift out of the I/O pin.
20	$\overline{WR}$	Serial interface write signal. During the low period of this signal the data shifts into the I/O pin.

CHIP ARCHITECTURE

The block diagram of SC22324/2 is shown on Pages 1 & 2. Each chip consists of four/two independently programmable biquadratic sections which may be configured through digital programming to achieve filter responses of 8th/4th order or less. Each chip has an uncommitted operational amplifier (op amp) at the input to facilitate implementation of an anti-aliasing section to eliminate aliasing effects in the subsequent switched-capacitor filters. The output of the op amp is followed by a buffer section that acts as a sample-and-hold (S/H) stage. The buffer feeds the signal to the biquad stages. The four/two biquad sections can be configured as one, two, three or four, (one or two for SC22322), cascaded sections. The output of the last cascaded stage is connected to an output buffer which drives the output pin. Provided at the output is another uncommitted op amp that can be used to implement a smoothing filter used for removing the clock noise from the output signal. The clock for the filter is supplied from an on-chip oscillator that needs an external crystal with an internal programmable counter. The counter can be programmed through the serial interface by an 8-bit word.

Each biquad needs 59 bits for programming. These bits can be loaded into temporary registers that can be addressed through the serial interface. After the filter response is optimized the bits can be transferred into E^2 memory for permanent storage. Eight additional bits are required for the programmable counter and two more bits determine the number of the biquad sections used in the particular application. The total number of temporary storage registers and E^2 bits for programming the SC22324/2 is 246/128.

The chip uses a four pin serial interface for communication. Sixteen bits are shifted into the chip, where five bits constitute the destination's address and eleven bits the data. The bidirectional input/output (I/O) pin allows reading back the contents of the internal registers for diagnostic purposes. SC22324/2 are available in 20-pin DIP and they use a ±5 V power supply for operation.

BIQUAD SECTIONS

Each biquad filter section can be programmed to achieve band-pass, low-pass, low-pass notch, high-pass, high-pass notch, notch, and all-pass filter responses. Any combination of these sections can be combined to form 2nd, 4th, 6th or 8th order filters (2nd and 4th order for SC22322). The block diagram of the programmable biquad is shown in Fig.1. Each biquad is first programmed by a four bit word (T0–T3) into the appropriate configuration. Subsequently five eleven bit coefficients define the transfer function. Each biquad section can be programmed into one of the sixteen possible types. Table 1 shows the control bits and the corresponding filter type. The z-domain transfer functions of all sixteen biquad types are given in Table 2, where V1 and V2 are the outputs of first and second op amps shown in Fig. 1.

Each of the five coefficients that define the filter transfer function is made up of eleven bits. These bits are loaded into each section through the serial interface.

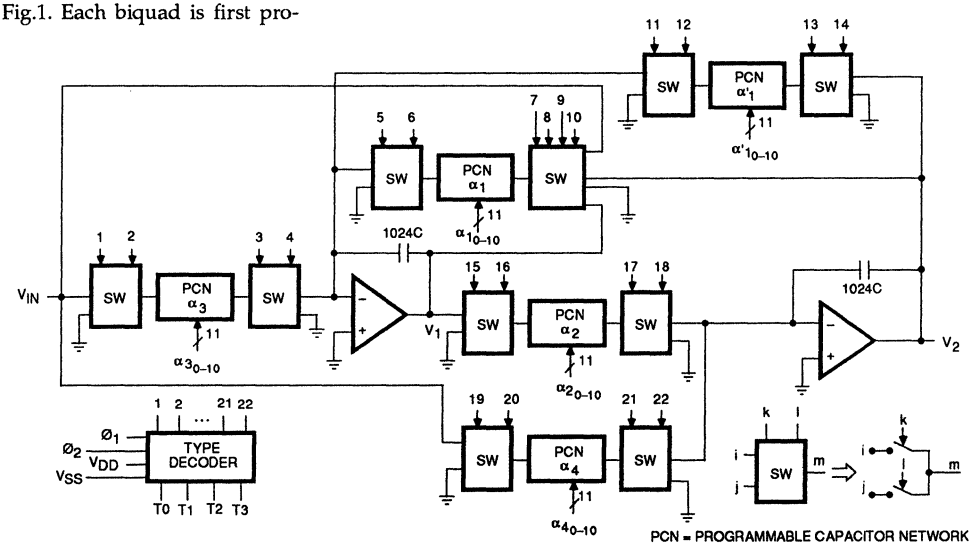


Figure 1. Programmable Biquad Block Diagram (One Second-Order Section)

T3 (D3)	T2 (D2)	T1 (D1)	T0 (D0)	FILTER TYPE	NAME
0	0	0	0	Notch Type I	N1
0	0	0	1	High-pass Type I	HP1
0	0	1	0	Band-pass Type I	BP1
0	0	1	1	Low-pass Type I Noninverting	LP1N
0	1	0	0	Low-pass Type I Inverting	LP1I
0	1	0	1	Band-pass Type II Noninverting	BP2N
0	1	1	0	Band-pass Type II Inverting	BP2I
0	1	1	1	Notch Type II	N2
1	0	0	0	High-pass Type II	HP2
1	0	0	1	Band-pass Type III	BP3
1	0	1	0	Low-pass Type II Noninverting	LP2N
1	0	1	1	Low-pass Type II Inverting	LP2I
1	1	0	0	Band-pass Type IV Noninverting	BP4N
1	1	0	1	Band-pass Type IV Inverting	BP4I
1	1	1	0	Band-pass Type V	BP5
1	1	1	1	All-pass	AP

Table 1. Programmable Biquad Types

COEFFICIENT STORAGE UNIT

Each biquad section needs 59 bits for programming, out of which, 55 bits are for the five filter coefficients and four bits are for the filter type. The programming bits are loaded into the chip through the serial interface and are stored in temporary registers. After the filter design is completed and the response meets the specifications, the programming bits can be transferred into non-volatile E^2 memory for permanent storage. The storage unit for one biquad section is shown in Figure 2. The details of one bit storage is shown in Figure 3. The source of the control bits for the biquad sections can be switched between the temporary registers and E^2 memory by a signal labeled SEL which is brought out to a pin. The E^2PROM can be programmed when the Program Enable (PE) signal is made high. The PE signal is controlled through the SEL/PEN pin, which accepts a tri-level input signal.

In the normal mode, SEL/PEN changes between DGND and V_{DD}, which controls the selection between the temporary registers and E^2PROM. Where, SEL/PEN = 0 V selects the temporary registers and SEL/PEN = V_{DD} (5 V) selects the E^2 PROM as the source of the filter control bits. The pin has an internal pull up, such that if it is left floating, the E^2PROM will be selected. When SEL/PEN pin is connected to V_{SS} (–5 V) the E^2 program enable signal PE will be activated. The actual programming takes place when V_{PP} (the E^2 programming voltage) is ramped from V_{SS} (–5 V) to a high voltage in the range of 12.5–13.5 V. When this happens the contents of the temporary registers are transferred to the E^2PROM. After the programming is completed V_{PP} should be returned to V_{SS} (–5 V). The E^2 programming timing waveforms are shown in Figure 4.

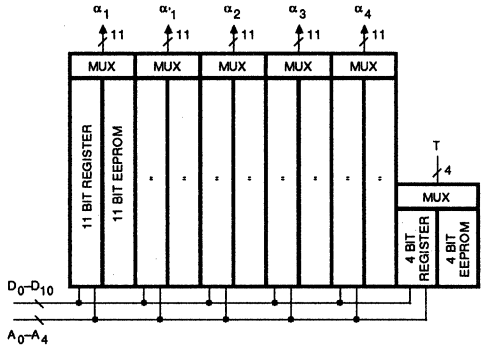


Figure 2. Storage Unit For Programming Bits in a Single Biquad Section

FILTER TYPE	z DOMAIN TRANSFER FUNCTION
N1	$H(z) = \frac{V_2}{Vin} = -\alpha_4\left[1 + \left(\frac{\alpha_2\,\alpha_3}{\alpha_4} - 2\right) z^{-1} + z^{-2}\right] / D_1(z)$
HP1	$H(z) = \frac{V_1}{Vin} = -\left[\alpha_3\,(1 - z^{-1})^2\right] / D_1(z)$
BP1	$H(z) = \frac{V_2}{Vin} = \left[-\alpha_2\,\alpha_3\,z^{-1}\,(1 - z^{-1})\right] / D_1(z)$
LP1N	$H(z) = \frac{V_2}{Vin} = \alpha_2\,\alpha_3\,z^{-2} / D_1(z)$
LP1I	$H(z) = \frac{V_2}{Vin} = -\alpha_2\,\alpha_3\,z^{-1} / D_1(z)$
BP2N	$H(z) = \frac{V_1}{Vin} = \alpha_3\,z^{-1}\,(1 - z^{-1}) / D_1(z)$
BP2I	$H(z) = \frac{V_1}{Vin} = -\alpha_3\,(1 - z^{-1}) / D_1(z)$
N2	$H(z) = \frac{V_2}{Vin} = \left(\frac{-\alpha_3}{1 + \alpha_1}\right)\left[1 + \left(\frac{\alpha_1'\,\alpha_4}{\alpha_3} - 2\right) z^{-1} + z^{-2}\right] / D_2(z)$
HP2	$H(z) = \frac{V_1}{Vin} = \left(\frac{-\alpha_3}{1 + \alpha_1}\right)(1 - z^{-1})^2 / D_2(z)$
BP3	$H(z) = \frac{V_2}{Vin} = \left(\frac{-\alpha_2\,\alpha_3}{1 + \alpha_1}\right) z^{-1}(1 - z^{-1}) / D_2(z)$
LP2N	$H(z) = \frac{V_2}{Vin} = \frac{\alpha_2\,\alpha_3}{1 + \alpha_1} z^{-2} / D_2(z)$
LP2I	$H(z) = \frac{V_2}{Vin} = -\frac{\alpha_2\,\alpha_3}{1 + \alpha_1} z^{-2} / D_2(z)$
BP4N	$H(z) = \frac{V_1}{Vin} = \frac{\alpha_3}{1 + \alpha_1} z^{-1}(1 - z^{-1}) / D_2(z)$
BP4I	$H(z) = \frac{V_1}{Vin} = \frac{-\alpha_3}{1 + \alpha_1}(1 - z^{-1}) / D_2(z)$
BP5	$H(z) = \frac{V_1}{Vin} = \frac{-\alpha_3}{1 + \alpha_1}(1 - z^{-1})(1 + z^{-1}) / D_2(z)$
AP	$H(z) = \frac{V_1}{Vin} = \frac{-1}{1 + \alpha_1}\left[1 + \left(\alpha_1'\,\alpha_4 - \alpha_1 - 2\right) z^{-1} + (1 + \alpha_1) z^{-2}\right] / D_2(z)$
	$D_1(z) = 1 + \left(\alpha_1'\,\alpha_2 + \alpha_1\,\alpha_2 - 2\right) z^{-1} + (1 - \alpha_1\,\alpha_2) z^{-2}$
	$D_2(z) = 1 + \left(\frac{\alpha_1'\,\alpha_2 - \alpha_1 - 2}{1 + \alpha_1}\right) z^{-1} + \left(\frac{1}{1 + \alpha_1}\right) z^{-2}$

Table 2. Biquad Filter Transfer Functions

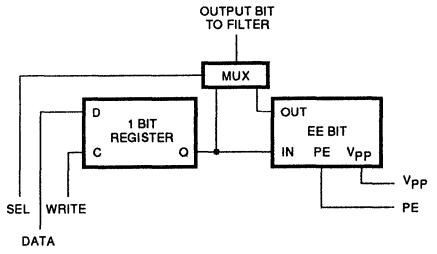


Figure 3. 1 Bit Storage Unit

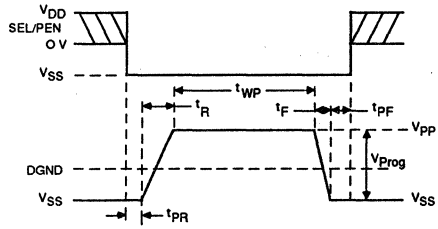


Figure 4. EE Programming Timing Waveforms

SERIAL INTERFACE

The filter programming data is stored in the internal temporary register through a four pin serial interface. When $\overline{WR}$ goes low, sixteen bits of data are shifted serially into the chip through the I/O pin. The sixteen bits constitute eleven bits of programming data and five bits of destination address. The data is sampled on the rising edge of the shift clock (clk). When $\overline{WR}$ goes high, the contents of the memory location selected by the five bit destination address is updated by the eleven bit data. For proper operation of the interface, there has to be exactly sixteen shift clock pulses within the $\overline{WR}$ high-to-low and low-to-high transition period. After data is latched into the selected register, the internal timing automatically loads the contents of the same location back into the serial interface shift register so that it can be read back. The data that is loaded back however, can be selected between the temporary register or E^2 memory by controlling the SEL/PEN pin. This feature is useful for diagnostic purposes. Every read of a selected location should be preceeded by a write into the same location. To read the data out, the $\overline{RD}$ signal should be pulled low. After sixteen clock pulses all the data inside the shift register will be clocked out of the I/O pin. The data appears at the output, on the rising edge of the shift clock (clk). To avoid any conflicts, the falling edge of the $\overline{RD}$ signal should be at least eight crystal clock periods away from the rising edge of $\overline{WR}$. The same rule applies to consecutive write cycles. The serial interface timing diagram is shown in Figure 5.

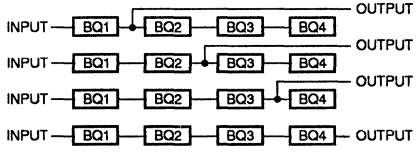
The five address bits A0–A4 are divided into two groups, A3, A4 and A0, A1, A2. The first group selects the biquad section and the second group addresses the filter coefficients and type of the selected biquad section. A map of the memory locations is shown in Tables 3a and b. As shown in Fig. 6, the address A4 = A3 = A2 = A1 = A0 = 0 selects the programmable counter and a two bit register that contains the number of the biquad sections according to Table 4. Out of the 32 possible address locations, 25 are utilized and 7 locations are unused.

A2	A1	A0	DATA
0	0	1	α1 (FILTER COEFFICIENT, D_0-D_{10})
0	1	0	α'1 (FILTER COEFFICIENT, D_0-D_{10})
0	1	1	α2 (FILTER COEFFICIENT, D_0-D_{10})
1	0	0	α3 (FILTER COEFFICIENT, D_0-D_{10})
1	0	1	α4 (FILTER COEFFICIENT, D_0-D_{10})
1	1	0	T (filter type, D_0-D_3)

Table 3a. Filter Coefficient and Type Address Location

A4	A3	Section #
0	0	1
0	1	2 Don't care for SC22322
1	0	3 Don't care for SC22322
1	1	4

Table 3b. Biquad Section Address Location



D1	D0	NO. OF SECTIONS
0	0	1
0	1	2 Don't care for SC22322
1	0	3 Don't care for SC22322
1	1	4

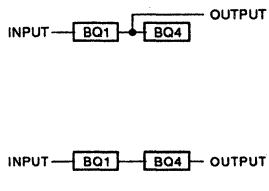


Table 4. Number of Biquad Sections

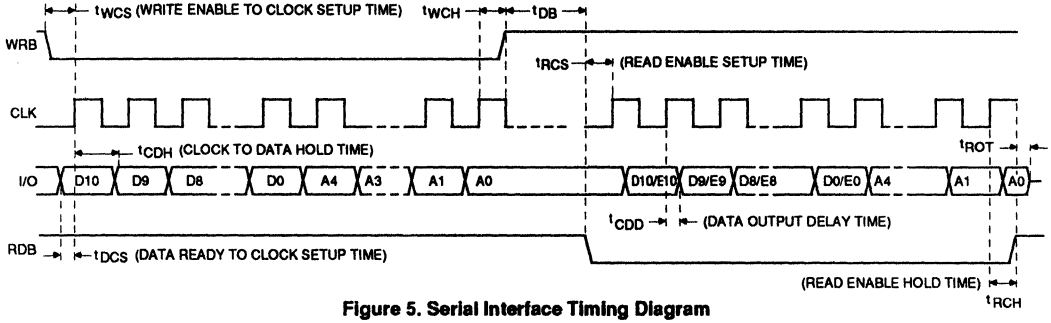


Figure 5. Serial Interface Timing Diagram

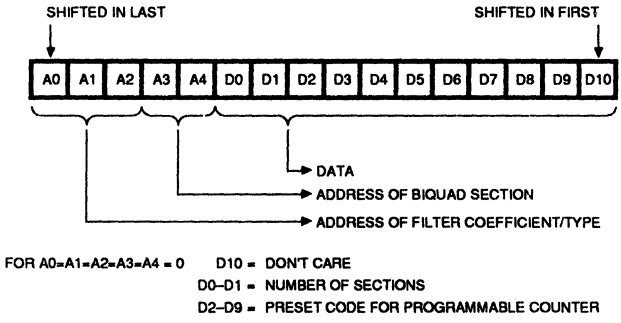


Figure 6. Address/Data Allocations for the Input Bits

PROGRAMMABLE COUNTER

The filter clock is derived from an on-chip oscillator and a programmable counter. The counter is shown in Figure 7. The presetable counter is at address location A4 = A3 = A2 = A1 = A0 = 0 and it is programmed by the eight bit word D_2–D_9 from the serial interface shift register. The output of the programmable counter is divided by two before it is applied to the filter. The divide ratio is shown in Table 5. It is always an even number (except when D_2–D_9 are all 0). It ranges from 2 to 510 in increments of two. When D_2–D_9 are all 0 the divide ratio is 1.

D9	D8	D7	D6	D5	D4	D3	D2	DIVIDE RATIO
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	510
0	0	0	0	0	0	1	0	508
0	0	0	0	0	0	1	1	506
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	0	4
1	1	1	1	1	1	1	1	2

Table 5. Programmable Counter Divide Ratios Versus Control Codes

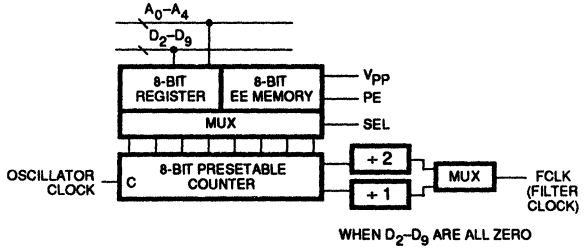


Figure 7. Programmable Counter

FILTER DESIGN SOFTWARE

Sierra provides a software program (BiQUAD) to help speed the transition from frequency design requirements to working hardware. This program will run on a personal computer and is composed of:

A routine that will calculate the number of sections weeded, the quadratic factors of the transfer function and includes a subroutine to equalize the group delay.

A routine that uses the coeffecient of the quadratic factors to select the type and calculates the capacitor values of each second order filter section. It plots the frequency resaponse with the quantized capacitor values.

A routine to program the coefficient filter type and clock divider constants into a SC22324/22322 with a personal computer.

DESIGN PROCEDURE

The SC22324 and SC22322, with Sierra's filter design software, greatly simplfy the design procedure for active filters. Most designs can be realized using a three step process described in this section.

Step 1: Filter Design. Start with the program "BIQUAD" to determine the type and order of the filter needed. The program plots the frequency response and generates the quadratic factors of the filter transfer function. A crystal frequency and filter clock frequency must also be selected.

Step 2: Generate Programming Data. With the quadratic factors and the crystal and filter clock frequencies obtained in Step 1, use the program "BIQUAD" to generate the clock divide ratio and the coefficients which program each second order section.

Step 3: Loading the Filter. When the clock divide ratio, the type and capacitor values of each second order filter section are determined, the filter can be programmed and operated. The program "FP" loads data into the device via a personal computer serial port and an interface board. This program may be used with or without Sierra's other filter design software.

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS} –0.6 to V_{DD} +0.6 V
DC Input Voltage (Digital Signals)	V_{SS} –0.6 to V_{DD} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 sec)	300°C

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
XTLIN,XTLOUT	Crystal Frequency				15	MHz
T_R, T_F	Input Rise or Fall Time	All Digital Inputs			50	ns
V_I	Analog Input Voltage		–3.0		+3.0	V

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—
Plastic package: –12mW/°C from 65° to 85°C

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = +5 V ±10%, V_{SS} = –5 V ±10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current			25		mA
I_{SS}	Quiescent Current			20		mA
V_{IH}	High Level Input Voltage; Digital Pins		2.2			V
V_{IL}	Low Level Input Voltage; Digital Pins				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Output (I_{OL} = 1.6 mA)				0.6	V

E^2 PROGRAMMING TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{PR}	PEN Low to Initiation of V_{PP}	0			ns
t_R	V_{PP} Rise time			20	mV/µs
t_{WP}	Duration of V_{PP} High	5		20	ms
t_F	V_{PP} Fall rate			20	V/µs
t_{pf}	V_{pp} Low to PEN High	0			ns
V_{PROG}	Programming Voltage (V_{PP}–V_{SS})	+17.5		+18.5	V

SERIAL INPUT TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{WCS}	Write Enable to Clock Set-Up Time	50			ns
t_{DCS}	Data Ready to Clock Set-Up Time	50			ns
t_{CDH}	Clock to Data Hold Time	50			ns
t_{WCH}	Clock to Write Enable Hold Time	50			ns
t_{DB}	End of Write Cycle to Read Enable Wait Time	8			Crystal Clock Periods
t_{RCS}	Read Enable to Clock Set-up Time	50			ns
t_{CDD}	Clock to Data Output Delay Time			75	ns
t_{RCH}	Clock to Read Enable Hold Time	75			ns
CLK_{freq}	Clock Frequency			5	MHz
t_{ROT}	Read Enable High to Output Tristate			50	ns

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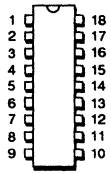
FEATURES

- ☐ 16-bit resolution / 84 dB dynamic range
- ☐ Full-scale signal to total harmonic distortion—80 dB typ.
- ☐ Output rate—20 kHz max.
- ☐ On-chip voltage reference
- ☐ Internal track and hold amplifier
- ☐ Linear phase digital filter
- ☐ DSP compatible codec-like serial interface
- ☐ Low power dissipation—220 mW typ.

18-PIN DIP PACKAGE



SC11036CN

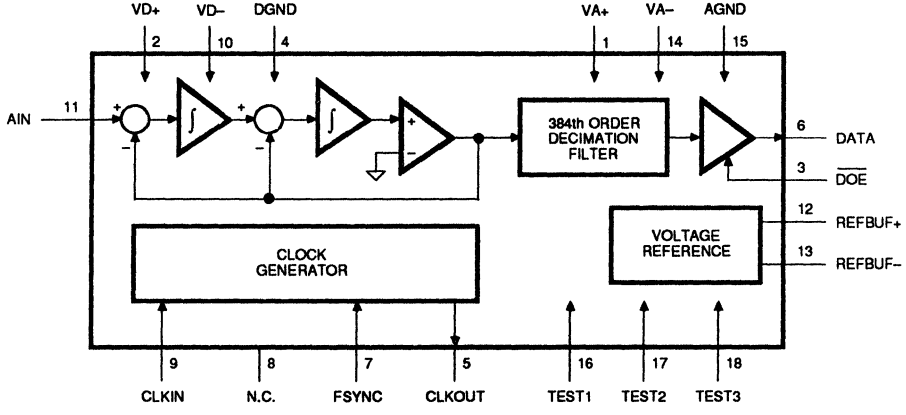
GENERAL DESCRIPTION

The SC11036 analog to digital converter is a unique, very high resolution A/D converter with excellent AC characteristics for voice-band signal processing applications such as high performance modems and voice recognition systems.

Delta-sigma modulation, a technique which utilizes oversampling followed by a digital decimation process, provides a digital output of 84 dB dynamic range, and 80 dB signal to distortion, for input signals with bandwidths from 0 to 10 kHz.

Sierra's 3 micron CMOS process ensures high reliability and power dissipation of less than 250 mW.

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES REFER TO PACKAGE PINS.

PIN DESCRIPTION

PIN NO.	PIN NAME	FUNCTION
1	VA+	Positive analog supply voltage. 5 V typical.
2	VD+	Positive digital supply voltage. 5 V typical.
3	$\overline{\text{DOE}}$	Data Output Enable. Tri-state control for DATA. When low, DATA is active and when high, DATA is in a high impedance state.
4	DGND	Digital ground reference. 0 V typical.
5	CLKOUT	Data output clock. See section on Data Output Characteristics for a complete explanation.
6	DATA	Serial data output pin. Converted data is clocked out on this pin by CLKOUT.
7	FSYNC	Frame synchronization pulse input. A pulse with frequency CLKIN/256 is applied to this pin to start data output and synchronize internal circuitry.
8	N.C.	No connection.
9	CLKIN	Master clock input. CMOS compatible input for a 5.12 MHz (maximum) clock generated externally.
10	VD–	Negative digital supply voltage. –5 V typical.
11	AIN	Analog input for the signal to be converted.
12	REFBUF+	Positive voltage reference noise buffer. Pin used to attenuate noise on the internal positive voltage reference. Should be connected to the analog ground through a 0.1 µF ceramic capacitor.
13	REFBUF–	Negative voltage reference noise buffer. Pin used to attenuate noise on the internal negative voltage reference. Should be connected to the analog ground through a 0.1 µF ceramic capacitor.
14	VA–	Negative analog supply voltage. –5 V typical.
15	AGND	Analog ground reference. 0 V typical.
16,17,18	TEST1 TEST2 TEST3	For factory use. Tied to digital ground during operation.

SYSTEM DESIGN WITH THE SC11036

Overview

The SC11036 functions as a complete data conversion subsystem for a voice-band signal processing system. The voltage reference, sample & hold, and much of the anti-aliasing filter required for most applications are all implemented on the chip. The chip has low power dissipation at about 220 mW typical, and has excellent power supply rejection, making it less sensitive to board layout and power supply characteristics than other A/D converters of comparable specifications. A general system connection diagram is shown in Figure 1.

Power Supplies

Although the SC11036 requires less attention to grounding and layout arrangements than other 16-bit A/D converters, care should still be taken. Independent analog and digital power supply pins are intended to isolate digital noise from the analog circuitry. The analog supplies, VA+ (pin 1) and VA– (pin 14), should be decoupled with respect to analog ground, AGND (pin 15). The digital supplies, VD+ (pin 2) and VD– (pin 10), should be decoupled with respect to digital ground, DGND (pin 4). Decoupling should be accomplished with 0.1 µF ceramic capacitors under all circumstances. If significant low frequency noise is present in the supplies, 10 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

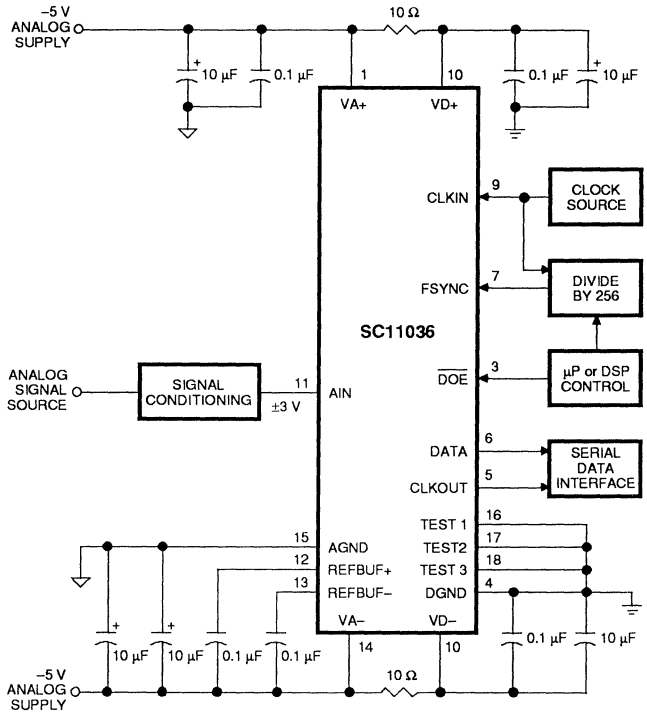


Figure 1. System Connection Diagram

The positive digital power supply of the SC11036 must never exceed the positive analog supply by more than a diode drop or the chip could be permanently damaged. If the two supplies are derived separately, the analog supply must come up first at power-up. Figure 1 shows a decoupling scheme which allows the SC11036 to be powered from a single set of ±5 V rails. The positive digital supply is derived from the analog supply through a 10 Ω resistor to prevent the analog supply from dropping below the digital supply.

Digital Design Considerations

Clocking

Two clocks should be supplied to the SC11036, the 5.12 MHz (max) 50% duty cycle master clock, input to CLKIN, and the frame synchronization clock, input to FSYNC (pin 7). The frame synchronization clock rate is the master clock rate divided by 256. The FSYNC input must be clocked synchronously with the master clock and should be derived from the master clock. An asynchronous FSYNC pulse will reset the digital filter and conversion errors will result.

The output rate may be set as needed by adjusting the master clock. If the output rate of the SC11036 must be varied to phase lock to some arbitrary signal, the period of the master clock may safely be varied to accomplish this as long as it is always kept greater than 150 ns. As the CLKIN period is reduced below 200 ns, signal to noise plus distortion performance will degrade smoothly to a typical level of about 70 dB at a constant 6.66 MHz CLKIN (150 ns periods).

The master clock is divided by two on-chip to generate an internal clock (INTCLK) used for sampling and digital timing. The timing diagram on Page 9 shows the relationship of this internal clock, INTCLK, with CLKIN and FSYNC. FSYNC is sampled on the falling edge of INTCLK and must be stable at that time. Since the phase of INTCLK is not known to the user, FSYNC should be generated on CLKIN rising edges, settle within 35 ns, and be at least two CLKIN periods in length. The internal logic will only react to FSYNC transitions from low to high, so the maximum length of the pulse is governed by the requirement that FSYNC be low for one INTCLK falling edge before it returns high signalling a new frame.

Data Output Characteristics & Coding Format

As shown in Figure 2, the SC11036 outputs a 16-bit data word in a serial burst at the INTCLK rate (the master clock rate divided by two). The data is output on DATA (pin 6) on the first rising edge of INTCLK after FSYNC has been

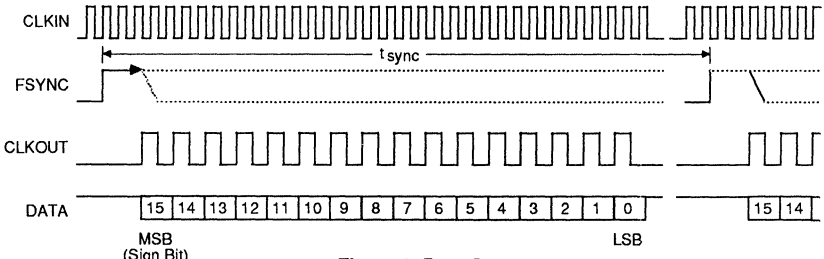


Figure 2. Data Output

recognized as going high. The data is then output on 16 consecutive INTCLK rising edges. CLKOUT (pin 5) is a gated version of INTCLK that is active while data is being output. Data will be stable on the falling edge of CLKOUT. After 16 CLKOUT pulses, DATA will go high, and CLKOUT will go low, until the next FSYNC rising edge.

Data read from the SC11036 is a two's complement digital representation of the analog input. The most significant bit (MSB), which is the sign bit, is output first in the serial data stream. Bits are output in descending order to the least significant bit (LSB).

A tri-state option, data output enable, $\overline{DOE}$ (pin 3), is available for bus oriented applications. However, it is asynchronous with respect to the rest of the SC11036. If $\overline{DOE}$ goes high during a data burst, DATA goes to a high impedance state. Any data output while $\overline{DOE}$ is high is lost.

Analog Design Characteristics

DC Characteristics

The SC11036 is intended for signal acquisition, or AC applications. Its absolute offset and gain characteristics are not specified and will vary with temperature. If the SC11036 is used in an application where DC measurement is important, a system level calibration scheme to adjust for gain and offset errors is recommended.

The Analog Input Range

The input range of the SC11036 is ±2.75 V. Internal voltage references set the analog input full-scale to the ±2.75 V limit. Note that differences in ground potential between the analog input common and AGND will appear as a signal added at the input of the device.

Dynamic Range

Processing the output of the SC11036 with a digital lowpass filter serves to increase the dynamic range of the unfiltered portion of the input bandwidth by eliminating the noise energy contributed by the filtered portion of the original input bandwidth. The unfiltered portion of the original input bandwidth can then be described with fewer output samples, according to the Nyquist criterion. For example, if the input bandwidth is cut in half with the digital lowpass filter, the unfiltered portion can now be described by dropping every other output sample, a process known as decimation.

Input Bandwidth			Dynamic Range	
Min	Max	Units	Typ	Units
0	5	kHz	88	dB
0	2.5	kHz	90	dB

Table 1. Dynamic Range with Additional Digital Filtering

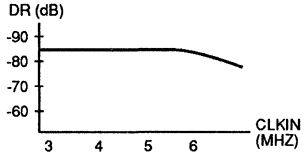


Figure 3. Typical Dynamic Range vs. CLKIN Frequency at 1 kHz Input

Anti-Aliasing Considerations

The two sources of potential aliasing in the SC11036 are the initial sampling of the analog input and the digital decimation process.

Initial Sampling

The analog input, AIN, is sampled at the INTCLK rate (1/2 CLKIN) by an on-chip track and hold amplifier. Input frequencies above 1/2 INTCLK (the Nyquist frequency) will alias, or wrap, around 1/2 INTCLK such that input frequencies in the region of INTCLK will appear as noise in the band of interest. If signals in this region are expected, a simple single-pole low-pass anti-aliasing filter can be used as shown in Figure 4. This filter ensures that any noise generated by aliasing around 1/2 INTCLK (at 1.28 MHz) is attenuated by at least 40 dB. Use of other CLKIN rates may require that the cutoff frequency of the filter shown be adjusted.

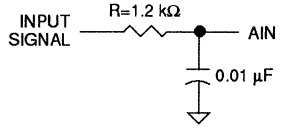


Figure 4. Antialiasing Filter

NOTE: ATTENUATION BY THIS ANTIALIASING FILTER IS GIVEN BY:
$\alpha = -10\text{Log}\,[1 + (f/f_O)^2]$ dB
where $f_O = {}^1/_{2\pi RC}$

Decimation

The output of the first stage of the SC11036, the delta-sigma modulator, is fed into an on-chip low-pass digital filter which has the frequency response defined in Figure 5. The output of the filter is then decimated such that the sampling rate is reduced from the INTCLK rate to F = INTCLK/128. This means that the output of the digital filter is effectively resampled at rate F, which has aliasing implications. Signals at multiples of F will alias into the baseband (wrap around multiples of F/2) after being attenuated according to the filter response defined in Figure 5. For example, if F = 20 kHz (INTCLK = 2.56 MHz), an input tone at 28 kHz will be attenuated by 39.9 dB and will appear at 8 kHz in the output spectrum.

Anti-aliasing to compensate for the effect of sample rate reduction, or decimation, in the SC11036 will depend upon the input bandwidth desired.

–F/4 Input Bandwidth

If the band of interest is from 0 to F/4, an off-chip low-pass filter and decimation step to reduce the output rate to F/2 and reject the band greater than F/4 is recommended. This increases the dynamic range of the SC11036 and eases the anti-aliasing task. Signals from 3F/4 to F will alias into the 0 to F/4 band but will be attenuated at least 31.4 dB by the on-chip filter. Aliased signals can be attenuated further by an analog anti-aliasing filter preceding the SC11036.

The F/2 data rate, needed to describe the 0 to F/4 input band, can also be obtained by simply dropping every other output of the SC11036. If this is done, input signals will now alias around multiples of F/4 (including the band from F/4 to F/2 which is minimally attenuated by the on-chip filter), and a more complex analog anti-aliasing filter is required. The analog filter's response will still be added to the response of the on-chip FIR filter however, so the analog filter's complexity will be slightly less than that required for a traditional A/D converter.

$$20 \log\left|\left(\frac{\sin(N\pi f T)}{N \sin(\pi f T)}\right)^3\right| = \text{Magnitude (dB)}$$

Where $T = 1/f_S = 2/f_{clk}$

$N = 128$

f_S = input sampling frequency

f = input frequency

$F = f_S/128$ = output data rate

EXAMPLES:

for $f_S = 2.56$ MHz

at $f = 5$ kHz Magnitude is –2.74 dB

at $f = 10$ kHz Magnitude is –11.8 dB

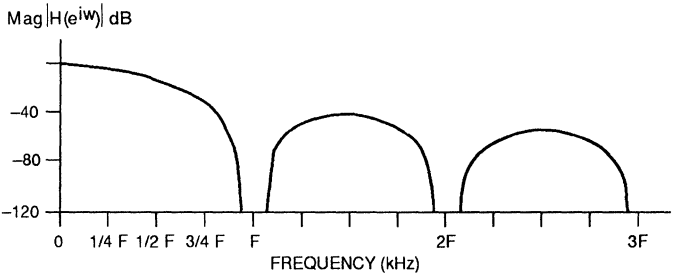


Figure 5. Low-Pass Filter Response

0–F/2 Input Bandwidth

If the band from F/4 to F/2 is also of interest, an analog anti-aliasing filter must be used. The filter complexity required will be similar to the case where output samples are dropped to obtain the F/2 output rate described above. Also, the attenuation of input signals in this band by the on-chip digital filter must be taken into account (see Figure 5).

SC11036 PERFORMANCE

The SC11036 features 100% tested dynamic performance. The following section is included to illustrate the test method used for the SC11036, the SC11036's error sources, and their effect on a signal's spectral content.

FFT Tests and Windowing

The SC11036 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sine wave is applied to the SC11036 and a "time record" of of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins". Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and DC can only be due to quantization effects and errors in the SC11036.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an exact integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, removing the discontinuities. The effect of the "window" in the frequency domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used to test the SC11036 has a maximum side-lobe level of –92 dB.

Figure 6 shows an FFT plot of a typical SC11036 with a 1 kHz sinewave input generated by an "ultra-pure" sinewave generator and the output multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records, without disturbing the total energy outside the fundamental. All harmonics and the –92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots.

Full-scale signal-to-noise plus distortion [S/(N+D)] is calculated as

the ratio of the RMS power of the fundamental to the sum of the RMS power of the FFT's other frequency bins, which include both noise and distortion. Full-scale signal-to-noise is calculated in the same way but excludes frequency bins where harmonics are expected. In this case, signal-to-noise plus distortion is shown to be better than 84 dB for an input frequency range of 0 to 9.6 kHz (fs/2).

The graph in Figure 7 is also derived from measurements taken of a SC11036 and shows the linear relationship between input signal level and signal-to-noise plus distortion. The dotted line beginning at a signal level of about –40 dB indicates the range of performance variation that can be expected from SC11036's at low input signal levels. Any input signal greater than –40 dB, regardless of frequency, will keep the S/(N+D) performance relative to the signal of interest on the solid line. However, if no input signal greater than –40 dB is present, the performance of a SC11036 may vary to the limit indicated by the dotted line.

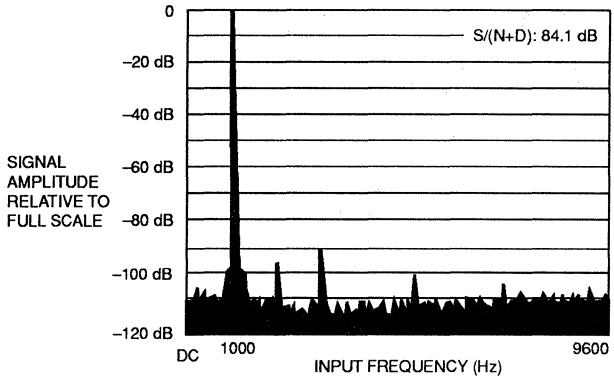


Figure 6. SC11036 Dynamic Performance

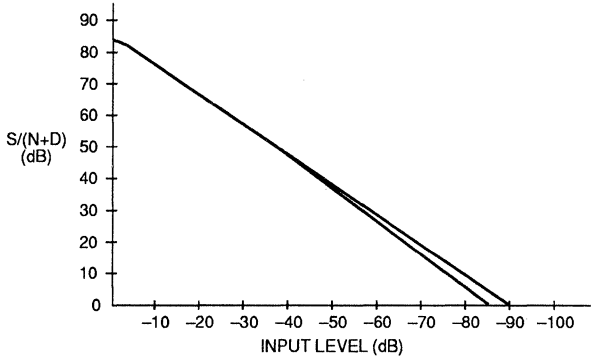


Figure 7. Typical Signal to Noise plus Distortion vs. Input Signal Level

Error Sources in the SC11036

Noise

The noise floor of an ideal 16-bit A/D converter is –98.08 dB, determined by the formula 6.02N+1.76, where N is the number of bits of the converter's resolution. This noise, called quantization noise, is a consequence of errors generated by digitizing any continuous time signal. Each A/D conversion approximates an analog value with a digital value, and the difference between the analog input and the digital approximation is the quantization error. Quantization noise is typically assumed to be white, spread evenly between DC and the input sampling frequency.

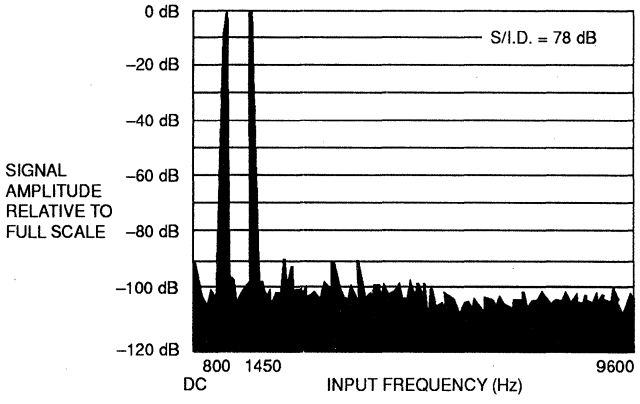


Figure 8. Intermodulation Distortion.

If the integrated noise of an A/D converter is any higher than –98.08 dB, other noise sources are present in the device. In the case of the SC11036 (typical noise floor –84 dB for 0–F/2 bandwidth and –90 dB for 0–F/4) the additional noise comes mainly from "1/f" noise sources, and aliasing of quantization noise.

"1/f" noise is so named because the noise energy is roughly inversely proportional to the noise frequency. 1/f noise is caused by "surface effects" on the chip and it varies with the semiconductor process.

Aliasing of quantization noise from higher frequency bands occurs due to the effect of the decimation filter (as described in Anti-aliasing Considerations). Aliasing of quantization noise accounts for much of the additional noise of the SC11036. In contrast, the contribution of thermal noise to the noise floor of the SC11036 is negligible due to the effect of the same on-chip decimation filter.

Distortion

The primary cause of harmonic distortion in the SC11036 is a phenomenon called charge injection. Charge injection is a consequence of non-ideal switches being used to switch charge between capacitors on the same chip, and is a nonlinear function of the voltage involved, in this case, the analog input voltage. Charge injection results in some minor linearity errors in the SC11036, which translates into harmonic distortion in the frequency domain.

Harmonic distortion characteristics of the SC11036 are excellent at 80 dB full-scale signal to THD (typical), as are intermodulation distortion characteristics, shown in Figure 8. Intermodulation distortion results from the modulation of two or more input frequencies by a nonlinear transfer function.

ABSOLUTE MAXIMUM RATINGS (DGND, AGND = 0 V)

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC Supply				
Positive Analog	VA+	—	6.0	V
Negative Analog	VA–	—	–6.0	V
Positive Digital	VD+	—	6.0	V
Negative Digital (Note 1)	VD–	—	–6.0	V
Input Voltage	V_{IN}			
Any Digital Input		DGND – 0.3	VD +0.3	V
AIN		VA – 0.3	VA + 0.3	V
Input Current	I_{IN}		10	mA
Any Pin Except Power Supplies (Note 2)				
Ambient Operating Temperature	T_A	–55	125	°C
Storage Temperature	T_{stg}	–65	150	°C

Notes: 1. VD+ must never exceed VA+ by more than +0.3 V.
2. The SC11036 will tolerate a transient input current of up to 100 mA without latching up.

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation of the part is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (DGND, AGND = 0 V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DC Supply					
Positive Analog	VA+	4.5	5.0	5.5	V
Negative Analog	VA–	–4.5	–5.0	–5.5	V
Positive Digital	VD+	4.5	5.0	5.5	V
Negative Digital	VD–	–4.5	–5.0	–5.5	V
Ambient Operating Temp. (Note 3)	T_A	T_{MIN}	25	T_{MAX}	°C
CLKIN Frequency	f_C	0.01	—	5.12	MHz

ANALOG CHARACTERISTICS (NOTE 4)

($T_A = T_{MIN} - T_{MAX}$; VA+ = 5 V ±10%; VA– = –5 V ±10%; AGND = 0 V; CLKIN = 4.9152 MHz)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
BW	Input Signal Bandwidth	0	—	9.6	kHz
V_{IN}	Input Voltage Range	–2.75	—	+2.75	Vp–p
DR	Dynamic Range (1 kHz Input) (Note 5)	78	84	—	dB
SDR	Signal to Distortion (1 kHz) (Note 6)	72	80	—	dB
P_D	Power Dissipation	—	220	250	mW
Z_{in}	AC Input Impedance (1 kHz)	—	30	—	kW
D_G	Absolute Group Delay (Note 7)	78.125	—	—	µs
PSR	Power Supply Rejection (1 kHz)				
	VA+	—	35	—	dB
	VA–	—	55	—	dB
	VD+	—	60	—	dB
	VD– (Note 8)	—	55	—	dB

Notes:
4. Analog characteristics are measured at 4.9152 MHz CLKIN, corresponding to an output rate of 19.2 kHz. The device is guaranteed to function up to 5.12 MHz CLKIN, corresponding to 20 kHz output, and will typically function, with some degradation in performance, to beyond 6 MHz CLKIN (see graph of typical dynamic range vs. frequency on page 4).
5. Full-scale signal to noise plus distortion measured with input 20 dB below full-scale (RMS measurements).
6. Full-scale signal to harmonic distortion measured with input at full-scale (RMS measurements).
7. Group delay is constant with respect to analog input frequency, and is determined by the formula $D_G = 384/\text{CLKIN}$.
8. Power supply rejection increases above 4 kHz due to the effect of the on-chip FIR filter.

DIGITAL CHARACTERISTICS (T_A=T_{MIN}–T_{MAX}; VD+ = 5 V ±10%; VD– = –5 V ±10%; DGND = 0 V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage All Except CLKIN (Note 9)	2.0	—	—	V
V_{IH}	High-Level Input Voltage CLKIN (Note 9)	3.5	—	—	V
V_{IL}	Low-Level Input Voltage All Except CLKIN (Note 9)	—	—	0.8	V
V_{IL}	Low-Level Input Voltage CLKIN (Note 9)	—	—	1.5	V
V_{OH}	High-Level Output Voltage (Note 10)	VD ±1.0 V	—	—	V
V_{OL}	Low-Level Output Voltage I_{OUT} = 1.6 mA	—	—	0.4	V
I_{LKG}	Input Leakage Current	—	—	10	µA
I_{OZ}	Tri-State Leakage Current	—	—	10	µA

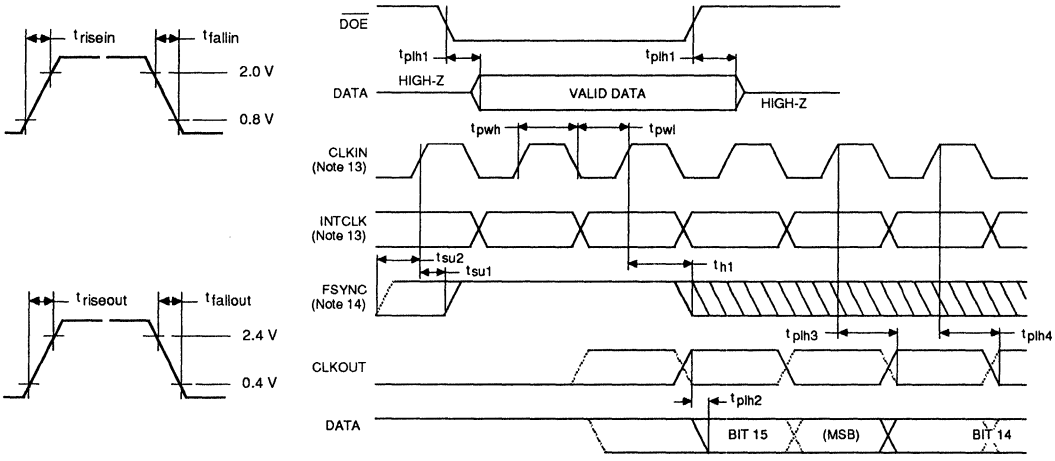
Notes:
9. Input current = 0.5 µA.
10. I_{OUT} = –100 µA. This specification guarantees TTL compatibility. (V_{OH} = 2.4 V @ I_{OUT} = –40 µA)

SWITCHING CHARACTERISTICS

($T_A = T_{MIN} - T_{MAX}$; C_L = 50 pF; VD+ = 5 V ± 10%; VD– = –5 V ± 10 %; DGND = 0 V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{riseout}$	Output Rise Time (Note 11)	—	15	20	ns
$t_{fallout}$	Output Fall Time (Note 11)	—	15	20	ns
t_{risein}	Input Rise Time	—	20	1000	ns
t_{fallin}	Input Fall Time	—	20	1000	ns
f_{clk}	CLKIN Frequency (256 t_{sync}) (Note 4)	—	—	5.12	MHz
t_{sync}	FSYNC Period ($256/f_{clk}$)	50	—	—	µs
	Setup Times				
t_{su1}	CLKIN Rising to FSYNC Rising	—	—	35	ns
t_{su2}	FSYNC Rising to CLKIN Rising	—	—	50	ns
	Hold Times				
t_{h1}	CLKIN Rising to FSYNC Falling	0	—	—	ns
t_{pwh}	CLKIN Pulse Width (Note 12)	40	—	—	ns
t_{pwl}		40	—	—	ns
	Propagation Delays				
t_{plh1}	DOE Falling to Data Valid	—	30	—	ns
t_{plh1}	DOE Rising to Hi-Z	—	30	—	ns
t_{plh2}	CLKOUT Rising to Data Valid	—	—	75	ns
t_{plh3}	CLKIN Rising to CLKOUT Rising	—	—	200	ns
t_{plh4}	CLKIN Rising to CLKOUT Falling	—	—	200	ns

Notes: 11. 50 pF load (includes probe and jig capacitance).
12. $t_{pwh} + t_{pwl} = 1/f_{clk}$



Notes: 13. INTCLK is an internal free-running clock derived by dividing CLKIN by 2. Its phase is not known by the user and may follow either the solid or the dotted line. When the phase is the same as the dotted line, CLKOUT and DATA will also behave as shown by the dotted lines.
14. FSYNC is recognized on the falling edge of INTCLK. To guarantee FSYNC is recognized, it should be generated on the rising edge of CLKIN and must settle within 35 ns. It should then remain active two CLKIN cycles as shown in the above diagram.

THEORY OF OPERATION

The SC11036 is an "oversampling" A/D converter making use of a "delta-sigma" modulation loop followed by a finite impulse response (FIR) digital filter. Oversampling refers to the fact that the analog input is sampled at a rate far greater than twice the highest frequency of interest as required by the Nyquist theorem. The A/D conversion actually takes place in the modulation loop while the filter is used both to convert the modulation loop output to a DSP compatible format and to filter frequencies higher than the band of interest.

The fundamental principle behind delta-sigma conversion is that of a rough single bit A/D converter embedded in an analog negative feedback loop with high open loop gain.

The Voltage-Follower Analogy

A comparison can be made with the simple voltage-follower op amp circuit shown in Figure A1. Output stage noise sources are represented by e_n. At low frequencies, e_n has little effect on the analog output. The two differential amplifier input devices dominate the noise. The linearity of the amplifier is excellent as long as the open loop gain is high.

In the case of the delta-sigma modulation loop shown in Figure A2, the ADC-DAC combination creates a unity gain signal path much like the op amp output stage of Figure A1. Here, e_n is dominated by the random errors of quantization, or quantization noise.

The high performance of the SC11036 can be understood by analogy to the voltage-follower circuit. First, the quantization noise of the comparator is white, spread uniformly in frequency between DC and the high sampling rate. Second, at low frequencies, the gain from e_n to the digital output is very low. As a result, because of the high frequency oversampling process, when the modulator output is processed by a digital lowpass filter, a high resolution, low noise representation of the low frequency input signal is obtained. This lowpass filter function, as well as decimation of the high speed (input sampling rate) output to a rate 256 times lower, is accomplished by the 384th order FIR filter on the SC11036.

Because the ADC on the SC11036 is a comparator and the DAC has only two output levels, plus and minus full-scale, both blocks are inherently linear. Overall modulator linearity is limited only by imperfection in the sample and hold and analog gain stage, or integrator.

Modulation Loop Walk-Through

The delta-sigma A/D converter can be understood more intuitively by demonstration. A simple first order delta-sigma modulation loop is shown in Figure A2. Full-scale input is ±1 V and nodes are labeled V1, V2, and V3 representing the outputs of the differential amplifier, the switched-capacitor integrator, and the comparator respectively. The output of the comparator, node V3, is the output of the loop (input to the digital decimation filter) and will be converted into plus or minus full-scale (+1 or –1) by the DAC. At the differential amplifier, the 1 or –1 is subtracted from the analog input voltage and the result, the voltage at node V1, is input to the switched-capacitor integrator. The switched-capacitor integrator acts as an analog accumulator; ie. the input voltage, at node V1, is added to the voltage on node V2 and the sum of the two becomes the new voltage on node V2. Node V2 is then compared to ground and generates a 1 on node V3 if greater than ground and a –1 if less. This completes the loop. Each operation occurs once during each clock cycle.

An example is shown in Table A. If all of the nodes are initially set to 0 and the analog input voltage is set

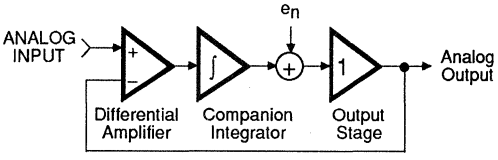


Figure A1. Op Amp Voltage-Follower

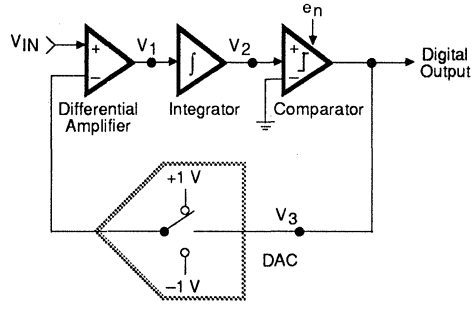


Figure A2. Delta-Sigma Modulation Loop

to .6 V, the state of each node for 8 clock cycles is shown in the table. Since the voltages on each node in clock cycle 2 and clock cycle 7 are identical, the period defined by clock cycles 2 through 6 will repeat if the analog input remains unchanged. Therefore, the average value of node V3 for that period, .6, reflects the average value of any large number of node V3 values. In other words, the average value of a number of the single bit modulation loop outputs is a numerical representation of the value of the analog input.

As pointed out in the initial discussion, this process is only valid for low frequency inputs. For a given sampling frequency, the accuracy achievable degrades as the input frequency increases. In the case of the SC11036, a 384th order FIR digital filter is used both to decimate (reduce the sampling rate of) the output of the modulation loop to sixteen bit words at 20 kHz max output rate and to filter out higher frequency components of the input.

This example is a simplification of the actual process taking place in the SC11036. The simple averaging step shown does not extract any information from the sequence of the pattern, while the weighted averaging process actually used on the chip extracts that information, resulting in a sharper frequency response for the FIR filter. Also, the SC11036 actually makes use of a second-order delta-sigma modulation loop, rather than a first order loop. This serves to increase the gain in the loop and, in turn, increases the dynamic range of the device. In fact, for a given input frequency band, a second order delta-sigma modulation loop will realize a 15 dB improvement in dynamic range every time the sampling rate is doubled, while a first order loop realizes only a 9 dB improvement. A first order version of the SC11036 could achieve only ~72 dB of dynamic range compared to ~90 dB for the SC11036, for the nominal 0–5 kHz input range.

The SC11036's maximum output rate of 20 kHz, twice the 10 kHz Nyquist rate of the nominal input bandwidth (0–5 kHz), was implemented to give the user the option of doubling the input bandwidth (0–10 kHz) keeping in mind the attenuation effects of the digital filter in the 5–10 kHz region. Several system design options are available, depending upon input bandwidth requirements, as described in this data sheet in the section on anti-aliasing considerations.

CLOCK PERIOD	V_1 DIFF. AMP. OUT	V_2 INTEGRATOR OUT	V_3 COMPARATOR/DAC OUT	PERIOD AVAERAGE
0	0	0	0	
1	.6	.6	1	
2	–.4	.2	1 ←	
3	–.4	–.2	–1	
4	1.6	1.4	1 Period	.6
5	–.4	1.0	1	
6	–.4	.6	1	
7	–.4	.2	1 ←	
8	–.4	–.2	–1	

Table A

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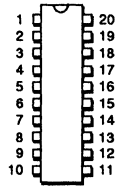
FEATURES

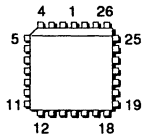
- ☐ Easy to use
- ☐ Clock to center frequency ratio accuracy ±0.6%
- ☐ Filter cutoff frequency stability directly dependent on external clock quality
- ☐ Separate highpass (or notch or allpass), bandpass, lowpass outputs
- ☐ $f_0 \times Q$ range up to 200 kHz
- ☐ Operation up to 30 kHz
- ☐ DIP and PLCC package options

20-PIN DIP PACKAGE



SC11122CN

28-PIN PLCC PACKAGE

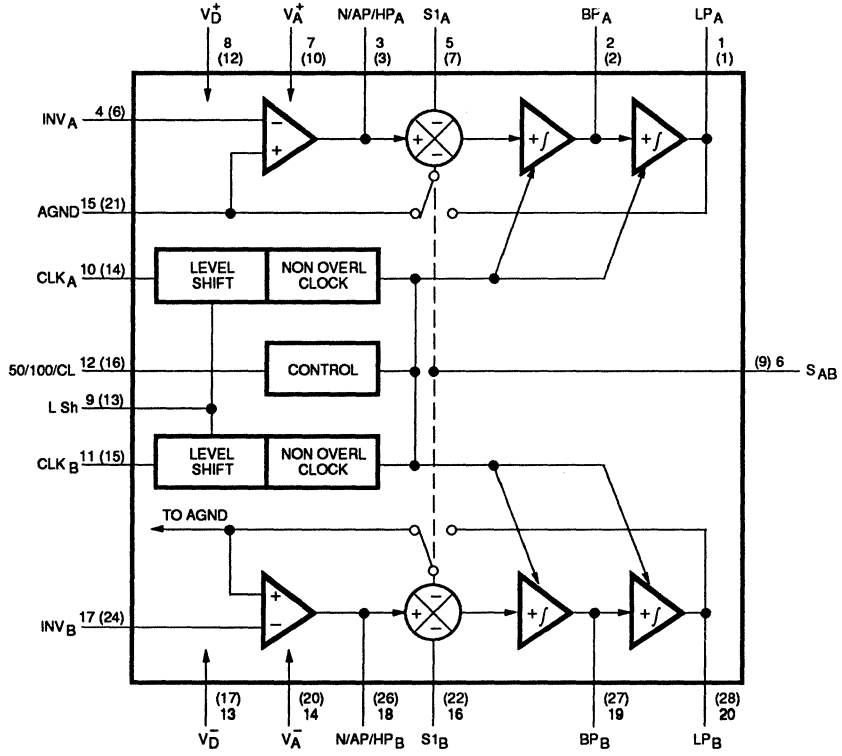


SC11122CV

GENERAL DESCRIPTION

The SC11122 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the SC11122; higher than 4th order functions can be obtained by cascading SC11122 packages. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

BLOCK DIAGRAM



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NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE DIP PACKAGE PINS; NUMBERS IN ( ) ARE PLCC PINS. PINS (4), (5), (8), (11), (18), (19), (23), AND (25) ARE NOT CONNECTED.

DEFINITION OF TERMS

f_{CLK}: The switched capacitor filter external clock frequency

f_O: Center frequency of the 2nd order function complex pole pair. f_O is measured at the bandpass output of each 1/2 SC11122, and it is the frequency of the band pass peak occurence (Figure 1).

Q: Quality factor of the 2nd order function complex pole pair. Q is also measured at the bandpass output of each 1/2 SC11122 and it is the ratio of f_O over the –3 dB bandwidth of the 2nd order bandpass filter, Figure 1. The value of Q is not measured at the lowpass or highpass outputs of the filter, but its value relates to the possible amplitude peaking at the above outputs.

H_{OBP}: The gain in (V/V) of the bandpass output at $f=f_O$.

H_{OLP}: The gain in (V/V) of the lowpass output of each 1/2 SC11122 at $f\rightarrow 0$ Hz, Figure 2.

H_{OHP}: The gain in (V/V) of the highpass output of each 1/2 SC11122 as $f\rightarrow f_{CLK}/2$, Figure 3.

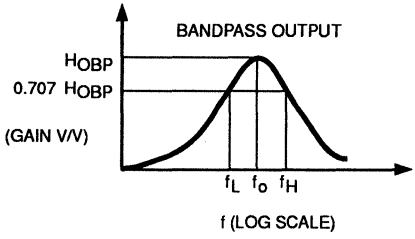
Q_Z: The quality factor of the 2nd order function complex zero pair, if any. (Q_Z is a parameter used when an allpass output is sought and unlike Q it cannot be directly measured.)

f_Z: The center frequency of the 2nd order function complex zero pair, if any. If f_Z is different from f_O, and if the Q_Z is quite high it can bc observed as a notch frequency at the allpass output.

f_{NOTCH}: The notch frequency observed at the notch output(s) of the SC11122.

H_{ON1}: The notch output gain as $f\rightarrow 0$ Hz.

H_{ON2}: The notch output gain as $f\rightarrow f_{CLK}/2$.

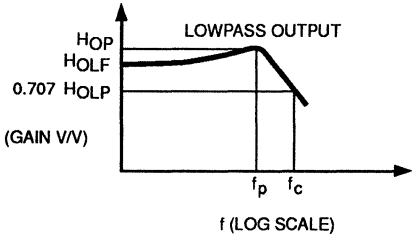


$$Q=\frac{f_o}{f_H-f_L};\ f_o=\sqrt{f_L f_H}$$

$$f_L=f_o\left(\frac{-1}{2Q}+\sqrt{\left(\frac{1}{2Q}\right)^2+1}\right)$$

$$f_H=f_o\left(\frac{1}{2Q}+\sqrt{\left(\frac{1}{2Q}\right)^2+1}\right)$$

Figure 1.

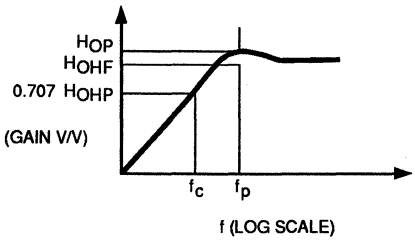


$$f_c=f_o\ x\sqrt{\left(1-\frac{1}{2Q^2}\right)+\sqrt{\left(1-\frac{1}{2Q^2}\right)^2+1}}$$

$$f_P=f_o\sqrt{1-\frac{1}{2Q^2}}$$

$$H_{OP}=H_{OLP}\ x\frac{1}{\frac{1}{Q}\sqrt{1-\frac{1}{4Q^2}}}$$

Figure 2.



$$f_c=f_o\ x\left(1-\frac{1}{2Q^2}\right)+\left[\sqrt{\sqrt{\left(1-\frac{1}{2Q^2}\right)^2+1}}\right]^{-1}$$

$$f_P=f_o\ x\left[\sqrt{1-\frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP}=H_{OLP}\ x\frac{1}{\frac{1}{Q}\sqrt{1-\frac{1}{4Q^2}}}$$

Figure 3.

PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1–3, 18–20	LP,BP, N/AP/HR	These are the lowpass, bandpass, notch or allpass or highpass outputs of each 2nd order section. The LP and BP outputs can sink typically 1 mA and source 3 mA. The N/AP/HP output can typically sink and source 1.5 mA and 3 mA, respectively.
4, 17	INV	This is the inverting input of the summing op amp of each filter. The pin has static discharge protection.
5, 16	S1	S1 is a signal input pin used in the allpass filter configurations (see modes of operation 4 and 5). The pin should be driven with a source impedance of less than 1 KΩ.
6	$S_{A/B}$	It activates a switch connecting one of the inputs of the filter's 2nd summer either to analog ground ($S_{A/B}$ low to V_A–) or to the lowpass output of the circuit ($S_{A/B}$ high to V_A+). This allows flexibility in the various modes of operation of the IC. $S_{A/B}$ is protected against static discharge.
7–8	V_A+, V_D+	Analog positive supply and digital positive supply. These pins are internally connected and therefore V_A+ and V_D+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.
13–14	V_A–, V_D–	Analog and digital negative supply respectively. The same comments as for V_A+ and V_D+ apply here.
9	L Sh	Level shift pin; it accommodates various clock levels with dual or single supply operation. With dual ±5 V supplies, the SC11122 can be driven with CMOS clock levels (±5 V) and the L Sh pin should be tied either to the system ground or to the negative supply pin. If the same supplies as above are used but T^2L clock levels, derived from 0 V to 5 V supply, are only available, the L Sh pin should be tied to the system ground. For single supply operation (0 V and 10 V) the V_D–, V_A– pins should be connected to the system ground, the AGND pin should be biased at 5 V and the L Sh pin should also be tied to the system ground. This will accommodate both CMOS and T^2L clock levels.
10–11	CLK (A or B)	Clock inputs for cach switched capacitor filter building block. They should both be of the same level (T^2L or CMOS). The level shift (L Sh) pin description discusses how to accommodate their levels. The duty cycle of the clock should preferably be close to 50% especially when clock frequencies above 200 KHz are used. This allows the maximum time for the op amps to settle which yields optimum filter operation.
12	50/100/CL	By tying the pin high a 50:1 clock to filter center frequency operation is obtained. Tying the pin at mid supplies (i.e. analog ground with dual supplies) allows the filter to operate at a 100:1 clock to center frequency ratio. When the pin is tied low, a simple current limiting circuitry is triggered to limit the overall supply current down to about 2.5 mA. The filtering action is then aborted.
15	AGND	Analog ground pin; it should be connected to the system ground for dual supply operation or biased at mid supply for single supply operation. The positive inputs of the filter op amps are connected to the AGND pin so "clean" ground is mandatory. The AGND pin is protected against static discharge.

MODES OF OPERATION

The SC11122 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach will be appropriate. Since this may appear cumbersome and, since the SC11122 closely approximates continuous filters, the following discussion is based on the well known frequency domain approach. The following illustrations refer to 1/2 of the SC11122; the other 1/2 is identical. Each SC11122 can produce a full 2nd order function, so up to 4th order functions can be performed by using cascading techniques.

Mode 1: Notch 1, Bandpass, Lowpass Outputs: $f_{NOTCH} = f_o$ (See Figure 4)

f_o = center frequency of the complex pole pair

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

f_{notch} = center frequency of the imaginary zero pair $= f_o$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (as $f = f_o$) $= -\frac{R3}{R1}$

H_{ON} = Notch output gain as $\begin{cases} f \rightarrow 0 & -\frac{R2}{R1} \\ f \rightarrow f_{CLK} & \end{cases}$

$Q = \frac{f_o}{BW} = \frac{R3}{R2}$

= quality factor of the complex pole pair.

BW = the –3 dB bandwidth of the bandpass output.

$H_{OLP} = \frac{H_{OBP}}{Q}$ or $H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q$

$H_{OLP\,(PEAK)} \cong xQ \times H_{OLP}$ (for high Q's)

The above expressions are important. They determine the swing at each each output as a function of the desired Q of the 2nd order function.

Mode 1a: Non-inverting BP,LP (See Figure 5)

$f_o = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

$H_{OLP} = -1\ H_{OLP\,(PEAK)} \cong x\ Q \times H_{OLP}$ (for high Q's)

$H_{OBP_1} = -\frac{R3}{R1}$

H_{OBP_2} = 1 (non-inverting)

Circuit dynamics:

$H_{OBP1} = Q$

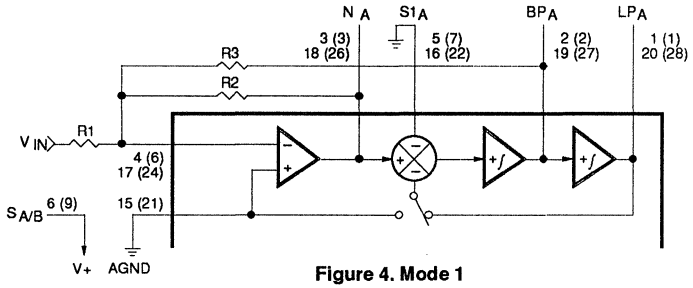


Figure 4. Mode 1

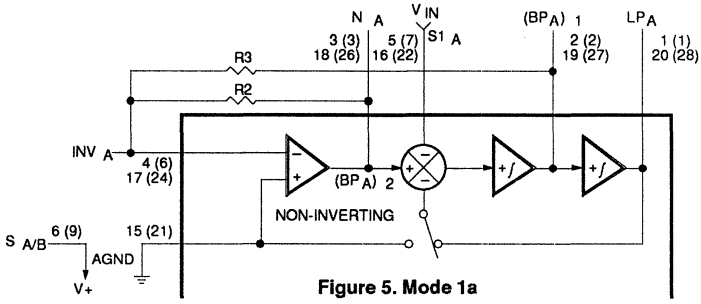


Figure 5. Mode 1a

Mode 2: Notch 2, Bandpass, Lowpass: $f_{NOTCH} \leq f_o$ (See Figure 6)

f_o = center frequency

$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1}$ or $\frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$

$f_{notch} = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

Q = quality factor of the complex pole pair

$= \frac{\sqrt{R2/R4+1}}{R2/R3}$

H_{OLP} = Lowpass output gain (as $f \rightarrow 0$)

$= -\frac{R2/R1}{R2/R4+1}$

H_{OBP} = Bandpass output gain (at $f = f_o$) – R3/R1

H_{ON_1} = Notch output gain (as $f \rightarrow 0$)

$= -\frac{R2/R1}{R2/R4+1}$

H_{ON_2} Notch output gain as $\left(f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$

Filter Dynamics:

$H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = Q\sqrt{H_{ON_1}\,H_{ON_2}}$

Mode 2: Highpass, Bandpass, Lowpass Outputs (See Figure 7)

$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}}$ or $\frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$

Q = quality factor of the complex pole pair

$= \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$

H_{OHP} = Highpass output gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_o$) $= -\frac{R2}{R1}$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R4}{R1}$

Circuit Dynamics:

$\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$; $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP} \times Q}$

$H_{OLP\,(PEAK)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP\,(PEAK)} \cong Q \times H_{OHP}$ (for high Q's)

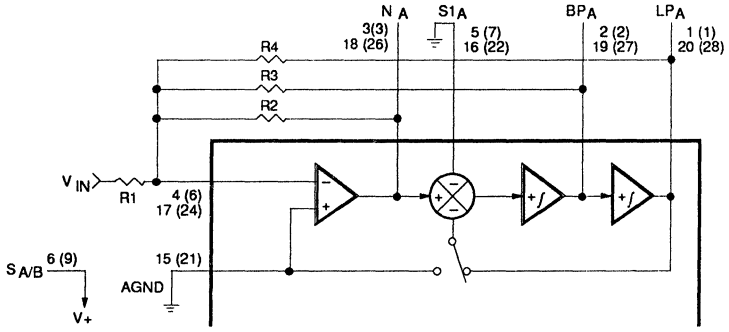


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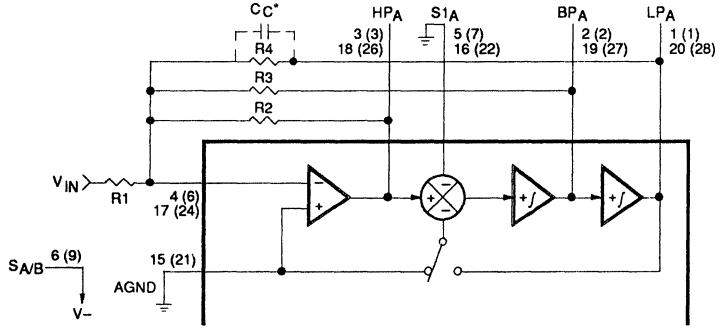
Figure 6. Mode 2



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*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF–100 pF) accross R4 to provide some phase lead.

Figure 7. Mode 3

Mode 3a: HP, BP, LP and Notch with External Op Amp (See Figure 8)

$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}}$ or $\frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$

$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$

$H_{OHP} = -\frac{R2}{R1}$

$H_{OBP} = -\frac{R3}{R1}$

$H_{OLP} = -\frac{R4}{R1}$

f_n = notch frequency = $\frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}}$ or $\frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$

H_{ON} = gain of notch at $f = f_o = Q\left(\frac{R_h}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)$

H_{n1} = gain of notch (as $f \to 0$) = $\frac{R_g}{R_l} \times H_{OLP}$

H_{n2} = gain of notch $\left(\text{as } f \to \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP}$

Mode 4: Allpass, Bandpass, Lowpass Outputs (See Figure 9)

f_o = center frequency

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

f_Z* = center frequency of the complex zero pair = f_o

$Q = \frac{f_o}{BW} = \frac{R3}{R2}$;

Q_Z = quality factor of complex zero pair $\frac{R3}{R1}$

For AP output make R1 = R2

H_{OAP} = Allpass gain at $\left(0 < 1 < \frac{f_{CLK}}{2}\right) = -\frac{R3}{R1} = -1$

H_{OLP} = Lowpass gain (as $f \to 0$)

$= -\left(\frac{R2}{R1} + 1\right) = -2$

H_{OBP} = Bandpass gain at ($f = f_o$)

$= \frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$

Circuit Dynamics:

$H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)\, Q$

* Due to the sampled data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4 dB peaking around f_o of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

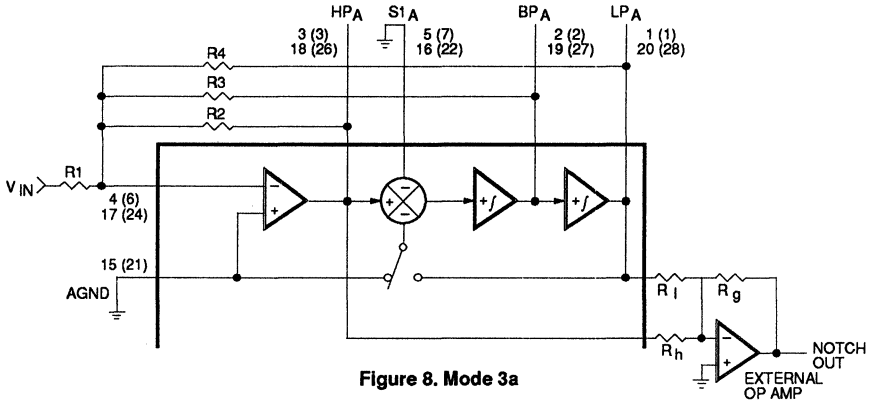

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Figure 8. Mode 3a

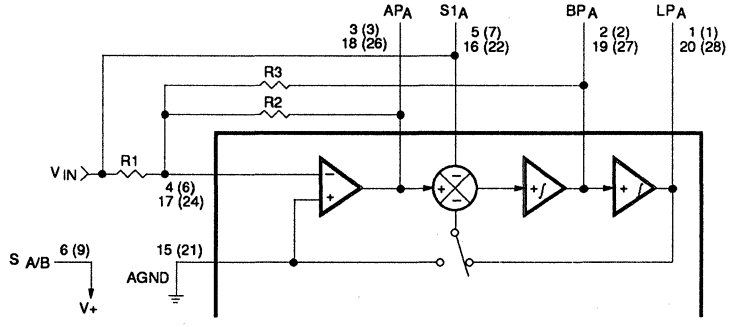

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Figure 9. Mode 4

Mode 5: Numerator Complex Zeros, BP, LP (See Figure 10)

$$f_O = \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_Z = \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1+R2/R4} \times \frac{R3}{R2}$$

$$Q_Z = \sqrt{1-R2/R4} \times \frac{R3}{R1}$$

H_{Oz1} = gain at C.z output (as $f \rightarrow 0$) $= -\frac{R2(R4-R1)}{R1(R2+R4)}$

H_{Oz2} = gain at C.z output as $\left(f \rightarrow \frac{f_{CLK}}{?}\right) = -\frac{R2}{R1}$

$$H_{OBP} = \left(\frac{R2}{R1}+1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = \left(\frac{R2+R1}{R2+R4}\right) \times \frac{R4}{R1}$$

Mode 6a: Single Pole, HP, LP filter (See Figure 11)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R3}{R1}$$

Mode 6b: Single Pole LP filter (Inverting and Non-inverting) (See Figure 12)

f_c = cutoff frequency of LP outputs

$$\equiv \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

H_{OLP1} = 1 (non-inverting)

$$H_{OLP2} = -\frac{R3}{R2}$$

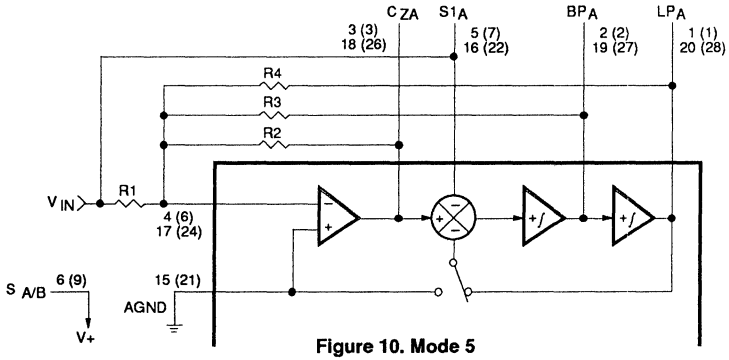

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Figure 10. Mode 5

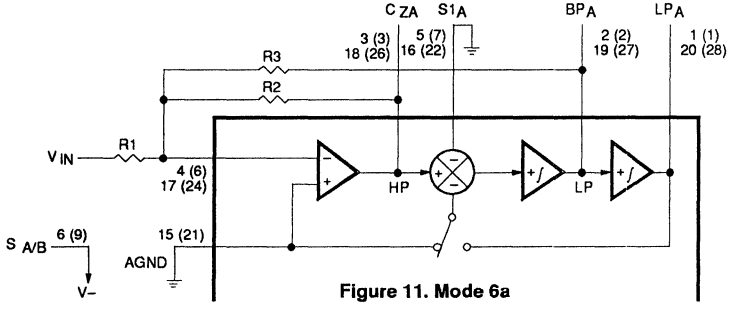

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Figure 11. Mode 6a

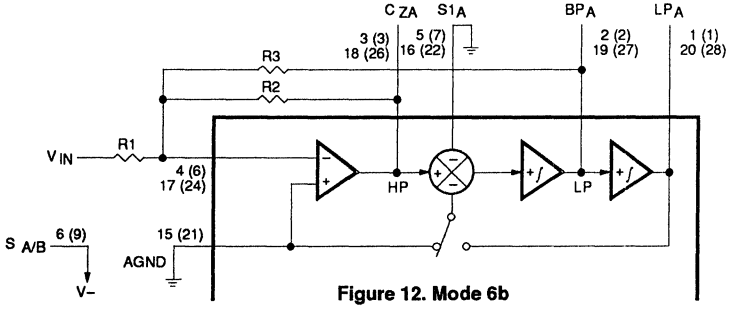

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Figure 12. Mode 6b

APPLICATIONS INFORMATION

How to Use the f_{CLK}/f_o Ratio Specification

The SC11122 is a switched capacitor filter designed to approximate the response of a 2nd order state variable filter. When the sampling frequency is much larger than the frequency band of interest, the sampled data filter is a good approximation to its continuous time equivalent. In the case of the SC11122, this ratio is about 50:1 or 100:1. Nevertheless the filter's response must be examined in the z-domain in order to obtain the actual response. It can be shown that the clock frequency to center frequency ratio, f_{CLK}/f_o and the quality factor, Q, deviate from their ideal values determined in the continuous time domain. These deviations are shown graphically in Figures 14 and 15. The ratio, f_{CLK}/f_o, is a function of the ideal Q and the largest errors occur for the lowest values of Q.

The curve for the f_{CLK}/f_o ratio versus the ideal Q has been normalized for a Q of 10 which is the Q value used for the f_{CLK}/f_o ratio testing of the SC11122. At this point the f_{CLK}/f_o ratio is 49.94 in the 50:1 mode and 99.35 in the 100:1 mode. These values are within a maximum tolerance of ±0.6% (SC11122B) and ±1.5% (SC11122C). The above tolerances hold for the entire range of Q's; in other words, at 50:1, an SC11122B has a ratio of 49.94 ±0.6% (Q = 10) and this ratio becomes (49.44 ±0.6%) at Q = 2.1. If these small errors cannot be tolerated, the clock frequency or the resistor's ratio, in Mode 3 and Mode 2, can be adjusted accordingly.

A Simple and Informative Filter Design Using the SC11122

Example 1:

Design a 4th order 2KHz lowpass maximally flat (Butterworth filter). The overall gain of the filter is desired to be equal to 1V/V.

The 4th order filter can be built by cascading two 2nd order sections of (f_o, Q) equal to: Q = 0.541, f_o = 2 KHz, Q = 1.306, f_o = 2 KHz.

Due to the low Q values of the filter, the dynamics of the circuit are very good. Any of the modes of operation can be used but Mode 1a is the most simple:

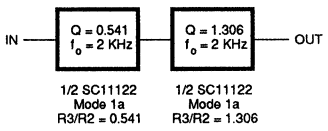

Figure 13.

Since for the first section the smallest resistor is R3, choose R3>5K. Assume R3 = 10K then R2 = 18.48K. For the second section choose R2 = 10K and then R3 = 13.06K. Both clock input pins (10,11) can be tied together and then driven with a single extemal clock. If the approximate ratio $f_{CLK}/100$ is chosen (pin 12 is grounded), then with a 200 KHz clock, the cutoff frequency, f_c will be at 2 KHz with a 1.5% maximum error.

The filter schematic is shown in Figure 16.

With a ±5 V supply, each output node of the IC (pins 1, 2, 3, 18, 19, 20) will swing to ±3.8 V (SC11122B) and ±3.2 V (SC11122C). The maximum gain of 1.306 occurs at pin 19 at $f_o \approx 2$ KHz. The input voltage amplitude should be limited to less than 7.6 Vp-p/1.306 = 5.8 Vp-p. If the Q of 1.306 section of the SC11122 precedes the Q of 0.541 section, the maximum gain is at pin 1. This gain can be calculated from the expression for H_{OP} given in Definition of Terms, and equals 1.41.

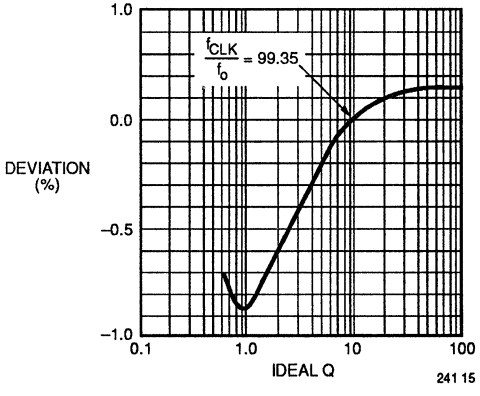

Figure 14.

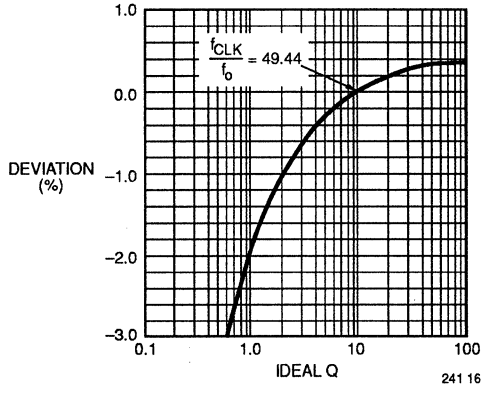

Figure 15.

Getting Optimum Cutoff Frequency, f_o, Accuracy (if needed):

In the previous example, an approximate 100:1 ratio was assumed. The true f_{CLK}/f_o ratio should be read from the curves, Figures 14 and 15. At 100:1 the normalized ratio to Q = 10 is: f_{CLK}/f_o = 99.35. For Q's of 0.541 and 1.306 this ratio becomes 99.35–0.75% = 98.6. For a 2 KHz f_C, the clock frequency should be 2 KHz x 98.6 = 197.2 KHz.

With an SC11122 and a 197.2 KHz clock, the maximum error on the 2 KHz cutoff frequency is ±0.6% as indicated in the specs.

If only a 200 KHz is available in Mode 1a, the true value of f_C and its maximum error is: 200 KHz/(98.6±0.6%) = 2028±0.6%.

If only a 200 KHz is available and there is need for a tight tolerance cutoff frequency, then Mode 3 should be used instead of Mode 1a. The resistor ratios are:

1st Section, Q = 0.541	2nd Section, Q = 1.306
R2/R4 = 0.972	R2/R4 = 0.972
R3/R2 = 0.548	R3/R2 = 1.324
R4/R1 = 1	R4/RI = 1

SC11122 OFFSETS

The switched capacitor integrators of the SC11122 have higher equivalent input offset than the typical R, C integrator of a discrete active filter. These offsets are created by a parasitic charge injection from the switches into the integrating capacitors; they are temperature and clock frequency independent and their sign is shown to be consistent from part to part. The input offsets of the CMOS op amps also add to the overall offset, but their contribution is very small. Figure 16 shows an equivalent circuit from where output DC offsets can be calculated.

V_{OS1} = 0 mVto ±10 mV

V_{OS2} = charge injected offset plus op amp offset ≅ 120 mV to -170 mV (at 50:1)

V_{OS3} = charge injected offset plus op amp offset ≅ 100 mV to 150 mV (at 50:1)

The V_{OS2} and V_{OS3} numbers approximately double at 100:1.

Output Offsets

The DC offset at the BP output(s) of the SC11122 is equal to the input offset of the lowpass switched capacitor integrator, V_{OS3}.

The DC offsets at the remaining outputs are roughly dependent upon the mode of operation and resistor ratios.

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\frac{1}{Q} + (1 + |H_{OLP}|) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

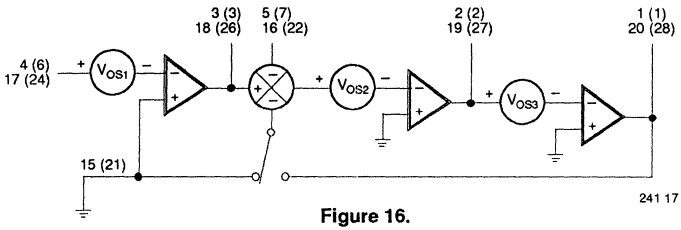

Figure 16.

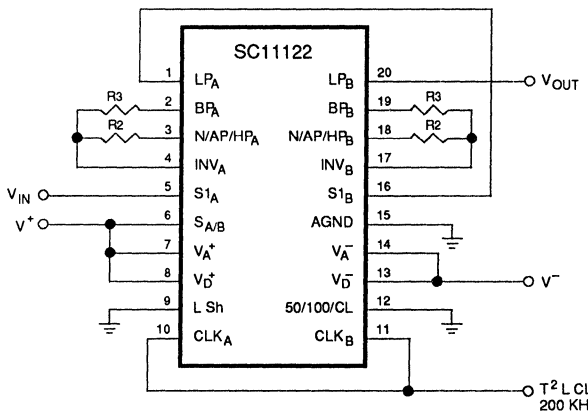

Figure 17. 4th Order, 2KHz Lowpass Butterworth Filter

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{R_p} \pm 1\right) V_{OS1} \times \frac{1}{1 + R2/R4} + V_{OS2} \frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}}$$

$$R_P = R1//R2//R3$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = -\frac{R4}{R2}\left(\frac{R2}{R3} V_{OS3} + V_{OS2}\right) + \frac{R4}{R2}\left(1 + \frac{R2}{Rp}\right) V_{OS1};$$

$$Rp = R1//R3//R4$$

Mode 1a

$$V_{OS\,(N.INV.BP)} = \left(1 + \frac{1}{Q}\right) V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS\,(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS\,(N.INV,BP)} - V_{OS2}$$

Comments on Output DC Offsets:

For most applications, the outputs are AC coupled and the DC offsets are not bothersome unless large input voltage signals are applied to the filter. For instance, if the BP output is used and it is AC coupled, the remaining two outputs should not be allowed to saturate. If so, gain nonlinearities and f_O, Q errors will occur. For Mode 3 of operation a word of caution is necessary: by allowing small R2/R4 ratios and high Q, the LP output will exhibit a couple of volts of DC offset and an adjustment should be made.

An Extreme Example: Design a 1.76 KHz BP filter with a Q of 21 and a gain equal to unity. The SC11122 will be driven with a 250 KHz clock, and it will be switched 50:1.

Resistor values: $\sqrt{\frac{R2}{R4}} = \frac{f_O}{f_{CLK}} \times 50 = 0.352; \frac{R2}{R4} = 0.124$

$\frac{R3}{R2} = 21 \times \frac{1}{0.353} = 59.63; \frac{R3}{R1} = 1$

Since R3/R2 is the highest resistor ratio, start with R2 = 10K, then R3 = 600K, R1 = 600K, R4 = 80K. Assuming V_{OS1} = 2 mV, V_{OS2} = –150 mV, V_{OS3} = 150 mV, the DC offset at the LP output is $V_{OS(LP)}$ = +1.2 V. The offset adjustment will be done by injecting a small amount of current into the inverting input of the first op amp, Figure 18. This will change the effect V_{OS1}, but the output DC offset of the HP and BP will remain unchanged.

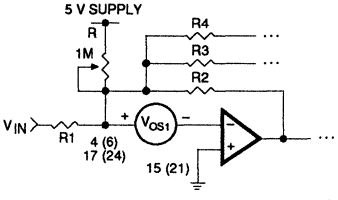

Figure 18. V_{OS} Adjust Scheme

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	14 V
Power Dissipation	500 mW
Operating Temperature	0°C to 70°C
Storage Temperature	150°C
Lead Temperature (Soldering 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (Complete filter) V_S = ±5 V, T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency range	f_O x Q < 200 KHz	20	30		KHz
Clock to center frequency ratio, f_{CLK}/f_O					
SC11122BN	Pin 12 High, Q = 10		49.94±0.2%	±0.6%	
SC11122CN	f_O x Q < 50 KHz, Mode 1		49.94±0.2%	±1.5%	
SC11122BN	Pin 12 at Mid Supplies		99.35±0.2%	±0.6%	
SC11122CN	Q = 10, f_O x Q < 50 KHz, Mode 1		99.35±0.2%	±1.5%	
Q Accuracy (Q Deviation From an Ideal Continuous Filter)					
SC11122BN	Pin 12 High, Mode 1		±2%	±4%	
SC11122CN	f_O x Q < 100 KHz, f_O < 5 KHz		±2%	±6%	
SC11122BN	Pin 12 at Mid Supplies		±2%	±3%	
SC11122CN	f_O x Q < 100 KHz, f_O < 5 KHz, Mode 1		±2%	±6%	
f_O Temperature Coefficient	Pin 12 High (~50:1)		±10		ppm/°C
	Pin 12 Mid Supplies (~100:1)		±100		ppm/°C
	f_O x Q < 100 KHz, Mode 1				
	Ext Clock Temp Independent				
Q Temperature Coefficient	f_O x Q < 100 KHz, Q Setting Resistors Temp Independent		±500		ppm/°C
DC Low Pass Gain Accuracy	Mode 1, R1=R2=10K			±2	%
Crosstalk			50		dB
Clock Feedthrough			10		mV
Maximum Clock Frequency		1	1.5		MHz
Power Supply Current			8	10	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		±4	±5		V
Voltage Swing Pins 1, 2, 19, 20	V_S = ±5 V, R_L = 5K				
SC11122BN		±3.8	±4.1		V
SC11122CN		±3.8	±3.9		V
Voltage Swing Pins 3 and 18	V_S = ±5 V, R_L = 3.5K				
SC11122BN		±4.0	±4.1		V
SC11122CN		±3.8	±3.9		V
Op Amp Gain BW Product			2.5		MHz
Op Amp Slew Rate			7		V/μs

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Graphics Products

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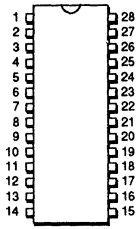
FEATURES

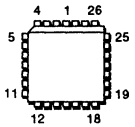
- ☐ Anti-sparkle circuitry.
- ☐ Compatible With the RS170 Video Standard.
- ☐ Pixel Rates Up to 65 MHz.
- ☐ 256k Possible Colors.
- ☐ Single Monolithic, High Performance CMOS.
- ☐ Low DAC Glitch Energy.
- ☐ TTL Compatible Inputs.
- ☐ RGB Analog Output, 6 bit DAC per Gun, Composite Blank.
- ☐ Video Signal Output into 37.5 or 75 Ω.
- ☐ Microprocessor Compatible Write Interface.
- ☐ Single +5 V ± 10% Power Supply.

28-PIN DIP PACKAGE



SC11171CN
SC11176CN

28-PIN PLCC PACKAGE



SC11171CV
SC11176CV

Clock Rate Options:
50 MHz or
35 Mhz

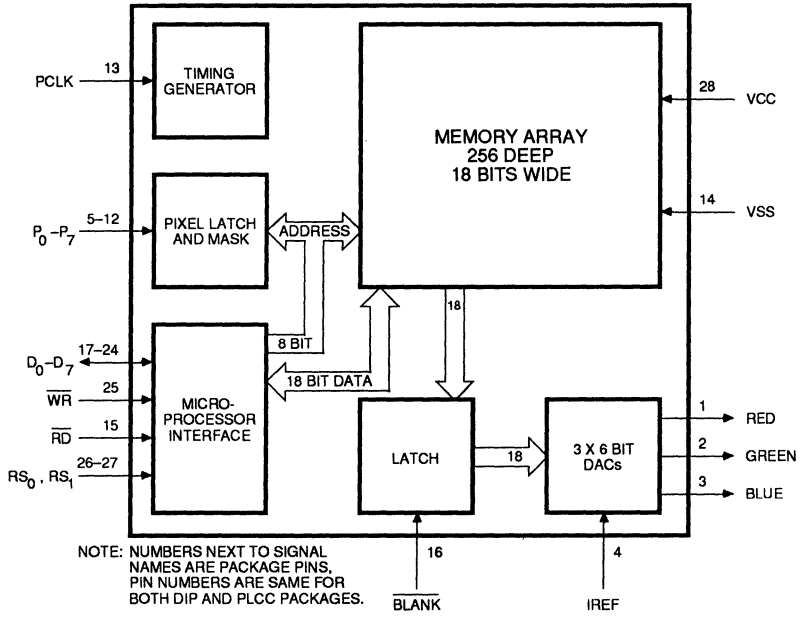
GENERAL DESCRIPTION

The SC11171 integrates the function of a color look-up table (or color palette), digital analog converters (designed to drive into a doubly terminated 75 Ω line) and bi-directional microprocessor interface into a single 28 pin package.

Capable of displaying 256 colors from a total of 262,144 colors, the SC11171 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The SC11176 is pin & function compatible with SC11171. It offers a pixel rate of 65 MHz. The pixel word mask allows displayed colors to be changed in a single write cycle rather than by modifying the look-up table.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SC11171 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store of 256x18 bit words, three 6 bit high speed DACs, a microprocessor interface and a pixel word mask.

An 8 bit value read in on the Pixel Address inputs is used as a read address for the store and results in an 18 bit data word. This data is partitioned as three fields of 6 bits, each field being applied to the inputs of a 6 bit DAC.

Pixel rates of up to 50 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the SC11171; this signal acts on all three of the analog outputs. The $\overline{\text{BLANK}}$ signal is delayed internally so that it appears at the analog outputs with the correct relationship to the pixel stream.

The contents of the look-up table can be accessed via an 8 bit wide microprocessor interface. The use of an internal synchronizing circuit allows color value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the Color Look-Up Table to facilitate such operations as animation and flashing objects. The pixel mask register is directly in the pixel stream, thus operations on the contents of the mask register should be synchronized to the pixel stream.

Video Path

Pixel Address and $\overline{\text{BLANK}}$ inputs are sampled on the rising edge of Pixel Clock, their effect appears at the analog outputs after three further rising edges of Pixel Clock.

Analog Outputs

The outputs of the DACs are intended to produce 0.7 V peak white amplitude when driving either a 75 Ω load with an IREF of 4.44 mA or when driving a doubly terminated 75 Ω load with an IREF of 8.88 mA.

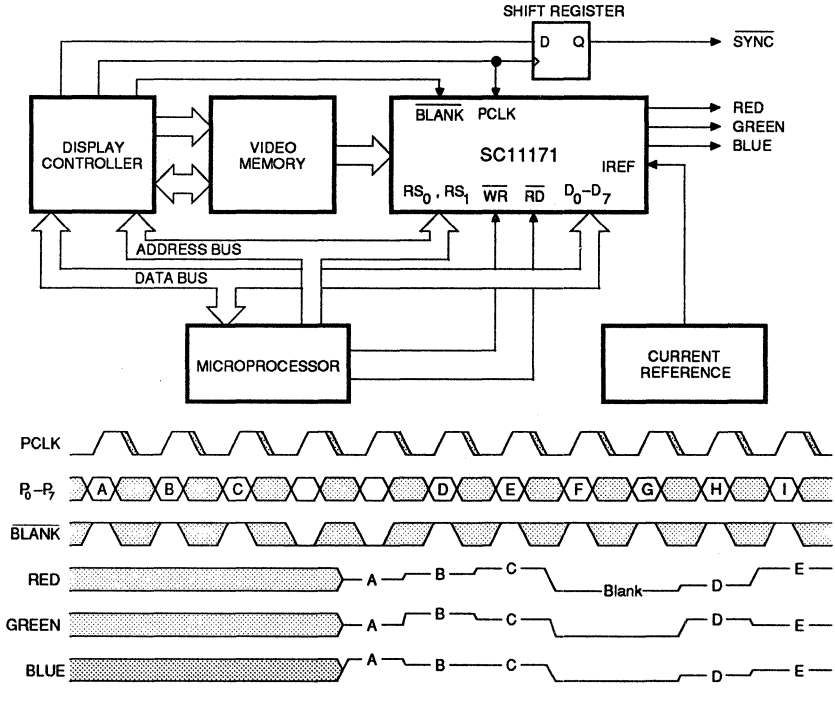
The $\overline{\text{BLANK}}$ input to the SC11171 acts on all three of the analog outputs. When the $\overline{\text{BLANK}}$ input is low, a binary zero is applied to the inputs of the DACs.

The expressions for peak white voltage/output loading combinations are given below:

$$V_{\text{peak white}} = \frac{\text{IREF} \times 63 \times R_{\text{load}}}{30}$$

$$V_{\text{black level}} = 0$$

TYPICAL APPLICATION



Microprocessor Interface

Below are listed the three microprocessor interface registers within the SC11171 and the four register addresses through which they can be accessed:

RS1	RS0	REGISTER NAME
0	0	Pixel Address (Write Mode)
1	1	Pixel Address (Read Mode)
0	1	Color Value
1	0	Pixel Mask

The contents of the color look-up table can be accessed via the Color Value register and the Pixel Address registers.

Writing to the Look-Up Table

To set a new color definition, a value specifying a location in the color look-up table is first written to the write mode Pixel Address register. The values for the red, green and blue intensities are then written in succession to the Color Value register. After the blue data is written to the Color Value register, the new color definition is transferred to the color look-up table and the Pixel Address register is automatically incremented.

As the Pixel Address register increments after each new color definition has been transferred from the Color Value register to the color look-up table, it is simple to write a set of consecutive locations with new color definitions. First the start address of the set of locations is written to the write mode Pixel Address register. Then the color definiations for each location are written sequentially to the Color Value register.

Reading From the Look-Up Table

To read a color definition, a value specifying the location in the look-up table to be read is written to the read mode Pixel Address register. After this value has been written, the contents of the location specified are copied to the Color Value register and the Pixel Address register is then automatically incremented.

The red, green and blue intensity values can be read by a sequence of three reads from the Color Value register. After the blue value has been read, the location in the look-up table currently specified by the Pixel Address register is copied to the Color Value register and the Pixel Address register is again incremented automatically.

Thus, a set of color definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Pixel Address register and then sequentially reading the color definitions for each location in the set.

Whenever the Pixel Address register is updated, any unfinished color definition read or write is aborted and a new one may begin.

Asynchronous Look-Up Table Access

Accesses to the Pixel Address and Color Value registers may occur without reference to the high speed timing of the pixel stream being processed by the SC11171. Internal logic synchronizes data transfers between the look-up table and the Color Value register to the Pixel Clock in the period between microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers to take place.

The Pixel Mask Register

The pixel address used to access the color look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory of the look-up table contents. Thus, by partitioning the color definitions by one or more bits in the pixel address, such effects as rapid animation , overlays and flashing objects can be produced.

The Pixel Mask register is independent of the Pixel Address and Color Value registers. Operations on the Pixel Mask register are required to be synchronous to the pixel stream. The requirements for pixel mask register synchronization are described in the application section of this specification.

PIN DISCRIPTION

PIN	NAME	DESCRIPTION
Pixel Interface		
13	PCLK	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address and Blanking inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the Color Look-Up Table to the analog outputs.
5–12	P0–P7	The byte wide value sampled on these inputs is masked by the Pixel Mask register and then used as the address into the Color Look-Up Table. This causes an 18 bit wide color value to be produced.
16	$\overline{\text{BLANK}}$	A low value on this input, when sampled, will cause a color value of zero to be applied to the inputs of the DACs regardless of the color value of the current pixel.
Analog Interface		
1 2 3	RED GREEN BLUE	These signals are the outputs of the 6 bit DACs. Each DAC is composed of 63 current sources sources whose outputs are summed. The number of current sources active is controlled by the 6 bit binary value applied.
4	IREF	The Reference Current drawn from Vcc via the IREF Current pin determines the current sourced by each of the current sources in the DACs. Each current source produces 1/30 of IREF when turned on.
Microprocessor Interface		
25	$\overline{\text{WR}}$	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
15	$\overline{\text{RD}}$	Most of the operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the color look-up table. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behavior. The Read and Write Enable signals should not be asserted at the same time.
26,27	RS0, RS1	The values on these inputs are sampled on the falling edge of the active enable signal ($\overline{\text{RD}}$ or $\overline{\text{WR}}$); they specify which one of the internal registers is to be accessed next. See Internal Register description for the function of these registers.
17–24	D0–D7	Data is transferred between the 8 bit wide program data bus and the registers within the SC11171 under the control of the active enable signal ($\overline{\text{RD}}$ or $\overline{\text{WR}}$). In a write cycle, the rising edge of $\overline{\text{WR}}$ validates the data on the program data bus and causes it to be written to the register addressed. The rising edge of the $\overline{\text{RD}}$ signal signifies the end of a read cycle; after which the program data bus will cease to carry contents of the register addressed and will go to a high impedance state.

INTERNAL REGISTERS

RS_1	RS_0	SIZE (bits)	REGISTER NAME	DESCRIPTION (All Registers Can be Written to and Read From)
0	0	8	Pixel Address (write mode)	There is a single Pixel Address register within the SC1171. This register can be accessed through either register address 0,0 or register address 1,1.
1	1	8	Pixel Address (read mode)	A read from address 0,0 is identical to a read address 1,1. Writing a value to address 0,0 performs the following operations which would normally precede writing one or more new color definitions to the color look-up table: a) Specifies an address within the color look-up table. b) Initializes the Color Value register. Writing a value to address 1,1 performs the following operations which would normally precede reading one or more color definitions from the color look-up table: a) Specifies an address within the color look-up table. b) Loads the Color Value register with the contents of the location in the color look-up table addressed and then increments the Pixel Address register.
0	1	18	Color Value	The Color Value register is internally an 18 bit wide register used as a buffer between the microprocessor interface and the color look-up table. A value can be read from or written to this register by a sequence of three byte transfers at this register address. When a byte is written to this register, only the least significant six bits (D0–D5) are used. When a byte is read, only the least significant six bits contain information — the most significant two bits being set to zero. The sequence of data transfer is red first, green second and blue last. After writing three values to this register, its contents are written to the location in the color look-up table specified by the Pixel Address register. The Pixel Address register then increments. After reading three values from this register, the contents of the location in the color look-up table specified by the Pixel Address register are copied into the Color Value register. The Pixel Address register then increments. Each transfer between the Color Value register and the color look-up table replaces the normal pixel mapping operations of the SC11171 for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0–P7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, a zero setting that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the microprocessor interface when the look-up table is being accessed.

POWER SUPPLY

The SC11171 is a high speed CMOS device. As such, it has relatively low DC power requirements. However, CMOS devices may draw large transient currents from the power supply. To ensure proper operation of the SC11171 it is necessary to adopt high frequency board layout and power distribution techniques.

To supply the transient currents required by the SC11171, the impedence in the decoupling path between the power supply pins (VCC pin 28 and VSS pin 14) should be kept to a minimum. It is recommended that the decoupling capacitance between VCC and VSS should be a 0.1 µF high frequency capacitor in parallel with a larger tantalum capacitor with a value between 22 µF and 47 µF. An inductance may be added in series with the positive supply to form a low pass filter and so further improve the power supply to the SC11171.

The combination of series impedance in the ground supply to the SC11171 and transients in the current drawn by the SC11171 will appear as differences in the VSS voltages to the SC11171 and to the digital devices driving it. To minimize this differential ground noise, the impedance in the ground supply between the SC11171 and the digital devices driving it should be minimized.

ANALOG OUTPUT—LINE DRIVING

The DACs in the SC11171 are made from summed, switched current sources. IREF sets the current sourced by each current source. The digital input to each DAC determines how many current sources are active. The load resistance between the DAC output and VSS determines the voltage produced by each DAC.

A single load resistor may be placed near the DAC output or at the input to the monitor which is to display the SC11171 output. Alternatively, the system may be double terminated by placing a load resistor at both the DAC output and the monitor input. The choice of resistor placement will depend on the requirements of the application.

The connection between the DAC outputs of the SC11171 and the RGB inputs of the monitor it is driving should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor.

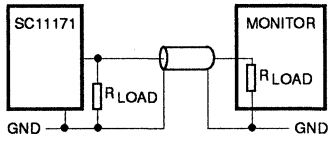
To ensure good signal fidelity, RF techniques should be observed. The PCB trace connecting the SC11171 to the off board connector should be sized so as to form a transmission line of the correct impedance. Correctly matched RF connectors should be used to connect from the PCB to the coaxial cable leading to the monitor and from the cable to the monitor.

Four methods of DAC termination and their relative merits are described below:

Double termination (Figure 1)

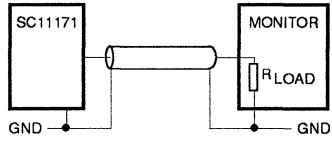
Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched, and thus should result in an ideal reflection free system.

The rise time of the DAC outputs is largely controlled by the RC time constant of the load it is driving. Thus, a double terminated DAC output will rise significantly faster than a singly terminated output.



Termination at destination (Figure 2)

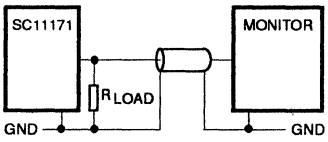
The input termination resistor of the monitor acts both as the load resistor for the DAC and as the terminating impedance of the transmission line. The connection between the SC11171 and the monitor is a correctly terminated transmission line so no reflections will occur. However, if there are any variations in the transmission line impedance (for instance a mismatched connector), a ghost image will appear on the display. This occurs because there is a reflection from the point where the mismatch occurs back towards the DAC output. The signal is then reflected from the DAC back towards the monitor, arriving a significant time after the original signal and so resulting in a ghost image.



Termination at source (Figure 3)

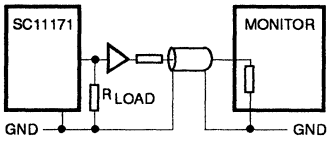
The load resistor for the DAC is placed at the output of the SC11171. No other terminating load is present as a high input impedance monitor is used. The AC load driven by the DAC is the transmission line impedance in parallel with the (matching) load resistor. Thus, the initial signal amplitude output by the DAC is half the DC value expected. This half amplitude signal is 100% reflected by the open

circuit presented by the monitor input, restoring the signal amplitude to the design value. The reflections from the monitor propagate back towards the DAC output. The load resistor at the DAC output presents a correctly terminated transmission line so no further reflections occur. This arrangement is relatively tolerant to mismatches in the transmission line between the DAC and the monitor as no reflections will occur from the DAC end of the transmission line. However, as there is always a substantial reflection from the monitor input, the signal cannot be looped through multiple monitors.



Buffered signal (Figure 4)

If the SC11171 is required to drive large capacitative loads (for instance long lossy cable runs), it may be necessary to buffer the DAC outpus. The buffer will have a relatively high imput impedance. The connection between the DAC outputs and the buffer inputs should be considered as a transmission line and will have the properties given in the previous examples when the DAC load resistor is placed at the DAC output or at the buffer input. The buffer output will have a relatively low impedance so should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.



ANALOG OUTPUT PROTECTION

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the SC11171 during system manufacture.

Once assembled into a system, devices are much less exposed to static damage. However, if the analog outputs of the SC11171 are made available at connectors outside the graphic system, they are still exposed to static damage and other hazardous voltages. Protection devices should be considered at this exposed interface.

CURRENT REFERENCE DECOUPLING

The DACs in the SC11171 are made from switched current sources. Each current source is based on a current mirror such that the current source will provide one thirtieth of the reference current IREF when it is active. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

The current IREF develops a voltage reference relative to VCC for the current mirror. Voltage variations on the VCC supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these VCC variations, it is recommended that a high frequency capacitor in parallel with a larger capacitor be used to couple the IREF input to VCC. This wil enable the current reference to track both low and high frequency variations in VCC. A coupling capacitor in the range 47 µF to 100 µF is appropriate for most applications. If the VCC variations are minor or managed by the current reference circuit, no coupling capacitor should be used.

CURRENT REFERENCE DESIGN

To ensure that the output current of the DACs is predictable and stable with temperature variations, an active current reference is recommended. Figures 8 to 11 show four designs of current reference.

Figures 8 to 10 are similar circuits. Each circuit uses three resistors and the power supply voltage VCC to set the reference current IREF through a transistor. In circuits 9 and 10, the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 10).

Figure 11 shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (30 Ω in this case) and is independent of the value of VCC.

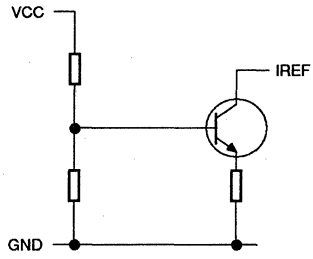


Figure 8.

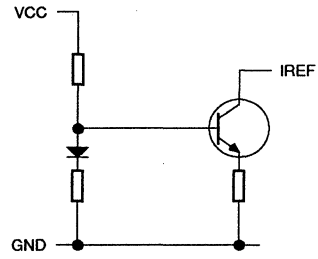


Figure 9.

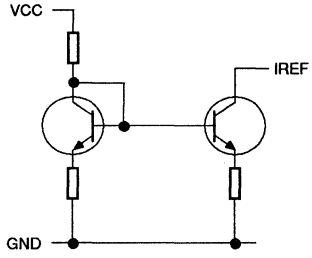


Figure 10.

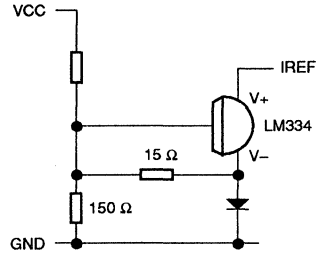


Figure 11.

DIGITAL INPUT TERMINATION

The PCB trace lines between the outputs of the TTL devices driving the SC11171 and the input to the SC11171 behave like low impedance transmission lines driven from a low impedance source and terminated with a high impedance. In accordance with transmission line principles, signal transitions will be reflected from the high impedance input to the SC11171, similarly, signal transitions will be inverted and reflected from the low impedance TTL output. To reduce or eliminate the ringing and in particular the undershoot that reflections cause, line termination is recommended. The termination may either be series or parallel.

The recommended technique is to use series termination. Series termination has the advantage of drawing no DC current and using fewer components. Series termination is accomplished by placing a resistor in series with the signal line at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and so ensures that any signal incident on the TTL output is not reflected.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a value around 100 Ω will be required. Because each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be found empirically.

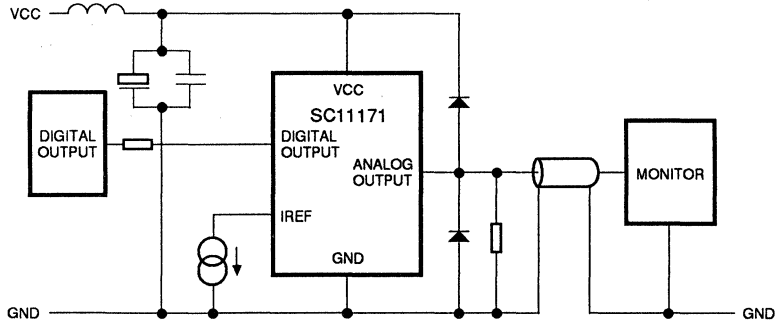


Figure 12.

PIXEL MASK REGISTER SYNCHRONIZATION

Each pixel address used as an address into the color look-up table is masked by the Pixel Mask register. If the contents of the Pixel Mask register are modified asynchronously to PCLK there is a possibility that the data held within the Pixel Mask register will change at such an instant as to corrupt the address applied to the look-up table as it is being latched.

If the Pixel Mask register is only initialized once on power up, the synchronization precautions described below need not be taken. It is sufficient to ensure that the color look-up table is initialized after the Pixel Mask regiater. The synchronous properties of the Pixel Mask register in no way affect the ability to update the look-up table asynchronously.

If the Pixel Mask register is to be updated on a regular basis, asynchronously to PCLK, corruption of the look-up table contents will inevitably occur. To prevent such corruption, the update of the mask register should occur at a time which ensures that the internal mask pixel value is not transitioning between values as it is being sampled. This requires that certain timing constraints synchronizing $\overline{WR}$ to PCLK are met. See the table given below.

The circuit given in Figure 13 should be suitable for systems with pixel rates up to 35 MHz. The synchronization circuitry required for systems working above 35 MHz may be more complex.

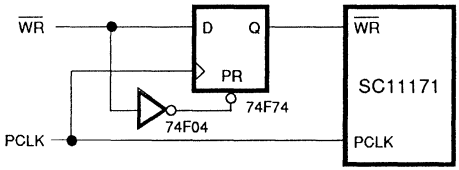
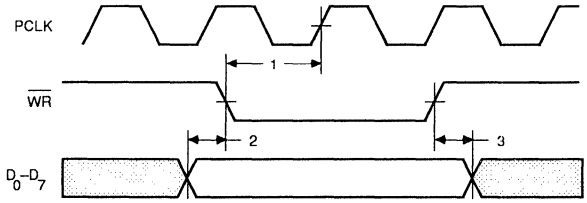


Figure 13.

			50 MHz		35 MHz			
NO	SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
1	t_{WLCH}	$\overline{WR}$ Illegal Transition Window	1	12	1	12	ns	1, 2
2	t_{DVWL}	Data Setup Time	15		15		ns	2
3	t_{WHDX}	Data Hold Time	10		15		ns	

1. $\overline{WR}$ should not transition from high to low within the window delimited by the minimum and maximum times specified.
2. This parameter need only be observed if modifications of the value held in the Pixel Mask register are required to occur synchronously to the pixel stream.



ABSOLUTE MAXIMUM RATINGS* (Note a)

Voltage on VCC	7.0 V
Voltage on any other pin	VSS–1.0 V to VCC+0.5 V
Temperature under bias	–40°C to 85°C
Storage temperature (ambient)	–65°C to 150°C
Power dissipation	1 W
Reference current	–15 mA
Analog output current (per output)	45 mA
DC digital output current	25 mA (one output at a time, one second duration)

* Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS (Note a)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VCC	Positive Supply Voltage	4.5	5.0	5.5	Volts	c
VSS	Ground		0		Volts	
VIH	Input Logic "1" Voltage	2.0		VCC+0.5	Volts	
VIL	Input Logic "0" Voltage	–0.5		0.8	Volts	d
TA	Ambient Operating Temperature	0		70	°C	
IREF	Reference Current	–3.0		–10	mA	e

DC ELECTRICAL CHARACTERISTICS (Notes a,b,f)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
ICC	Average Power Supply Current		190	mA	g, 65 MHz
ICC	Average Power Supply Current		160	mA	g, 50 MHz
ICC	Average Power Supply Current		150	mA	g, 35 MHz
VREF	Voltage at IREF Input (pin 4)	VCC–3	VCC	Volts	
IIN	Digital Input Current (any Input)		±10	µA	h,i
IOZ	Off State Digital Output Current		±50	µA	h,j
VOH	Output Logic "1"	2.4		Volts	IO=–5 mA
VOL	Output Logic "0"		0.4	Volts	IO=5 mA

DAC CHARACTERISTICS (Notes a,b,k)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
	Resolution	6		bits	
VO(max)	Maximum Output Voltage		1.5	Volts	IO≤10 mA
IO(max)	Maximum Output Current		–21	mA	VO≤1 V
	Full Scale Error		–7 to +3	%	l
	DAC to DAC Correlation		±2	%	m
	Integral Linearity		±0.5	LSB	n
	Rise Time (10% to 90%)		6	ns	o
	Full Scale Settling Time		20	ns	o,p,q, 50 MHz
	Full Scale Settling Time		28	ns	o,p,q, 35 MHz
	Full Scale Settling Time		15.3	ns	o,p,q, 65 MHz
	Glitch Energy		200	pv/sec	o,q

AC TEST CONDITIONS

Input pulse levels	VSS to 3 V
Input rise and fall times (10% to 90%)	6 ns
Digital input timing reference level	1.5 V
Digital output timing reference level	0.8 V and 2.4 V
Digital output load	see Figure 14

CAPACITANCE (Notes q, r)

SYMBOL	PARAMETER	MAX	NOTES
CI	Digital input	7 pF	
CO	Digital output	7 pF	s
COA	Analog output	10 pF	t

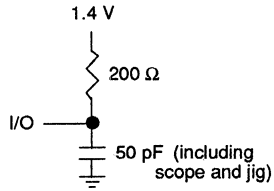
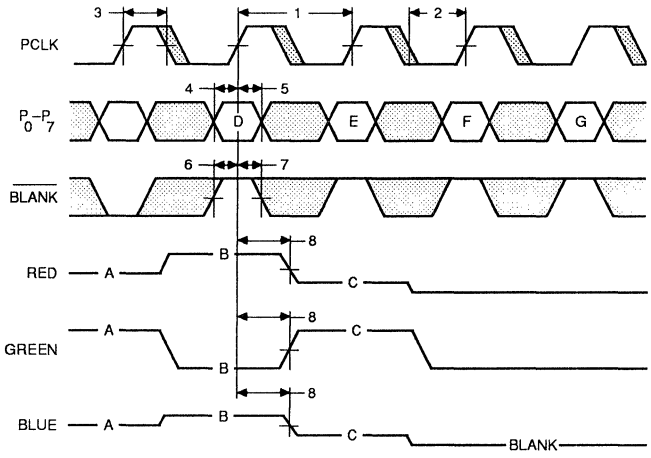


Figure 14. Output Load.

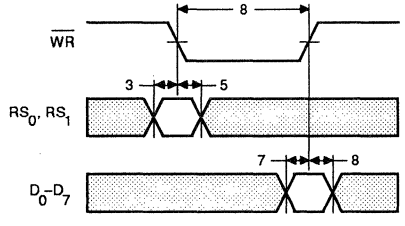
VIDEO OPERATION

			65 MHz	50 MHz	35 MHz	ALL		
NO	SYMBOL	PARAMETER	MIN	MIN	MIN	MAX	UNITS	NOTES
1	t_{CHCH}	PCLK Period	15.3	20	28	10000	ns	
2	Δt_{CHCH}	PCLK Jitter				±2.5	%	u
3	t_{CLCH}	PCLK Width Low	5	6	9	10000	ns	
4	t_{CHCL}	PCLK Width High	5	6		7	10000	ns
5	t_{PVCH}	Pixel Word Setup Time	3	4	4		ns	v
6	t_{CHPX}	Pixel Word Hold Time	3	4	4		ns	v
7	t_{BVCH}	$\overline{\text{BLANK}}$ Setup Time	3	4	4		ns	
8	t_{CHBX}	$\overline{\text{BLANK}}$ Hold Time	3	4	4		ns	
9	t_{CHAV}	PCLK to Valid DAC Output	5	5	5	30	ns	w
10	Δt_{CHAV}	Differential Output Delay				2	ns	x
		Pixel Clock Transition Time				50	ns	

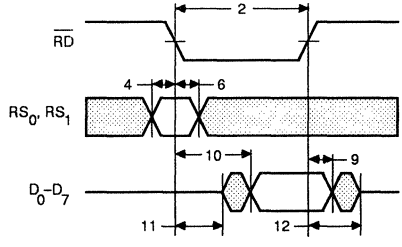


MICROPROCESSOR INTERFACE OPERATION

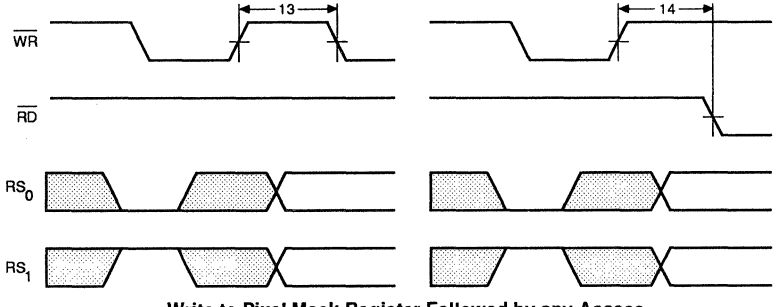
			65MHz	50 MHz	35 MHz	ALL		
NO	SYMBOL	PARAMETER	MIN	MIN	MIN	MAX	UNITS	NOTES
1	t_{WLWH}	$\overline{WR}$ Pulse Width Low	50	50	50		ns	
2	t_{RLRH}	$\overline{RD}$ Pulse Width Low	50	50	50		ns	
3	t_{SVWL}	Register Select Setup Time	10	10	15		ns	
4	t_{SVRL}	Register Select Setup Time	10	10	15		ns	
5	t_{WLSX}	Register Select Hold Time	10	10	15		ns	
6	t_{RLSX}	Register Select Hold Time	10	10	15		ns	
7	t_{DVWH}	Write Data Setup Time	10	10	15		ns	
8	t_{WHDX}	Write Data Hold Time	10	10	15		ns	
9	t_{RLQX}	Output Turn-On Delay	5	5	5		ns	
10	t_{RLQV}	Read Enable Access Time				40	ns	
11	t_{RHQX}	Output Hold Time	5	5	5		ns	
12	t_{RHQZ}	Output Turn-Off Delay				20	ns	y
13	t_{WHWL1}	Successive Write Interval	$4 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$		ns	
14	t_{WHRL1}	Write Followed by Read Interval	$3 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$		ns	
15	t_{RHRL1}	Successive Read Interval	$4 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$		ns	
16	t_{RHWL1}	Read Followed by Write Interval	$4 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$		ns	
17	t_{WHWL2}	Write After Color Write	$4 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$		ns	z
18	t_{WHRL2}	Read After Color Write	$4 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$	$3 \cdot t_{CHCH}$		ns	z
19	t_{RHRL2}	Read After Color Read	$6 \cdot t_{CHCH}$	$6 \cdot t_{CHCH}$	$6 \cdot t_{CHCH}$		ns	z
20	t_{RHWL2}	Write After Color Read	$6 \cdot t_{CHCH}$	$6 \cdot t_{CHCH}$	$6 \cdot t_{CHCH}$		ns	z
21	t_{WHRL3}	Read After Read Address Write	$6 \cdot t_{CHCH}$	$6 \cdot t_{CHCH}$	$6 \cdot t_{CHCH}$		ns	z
		Write/Read Enable Transition Time				50	ns	



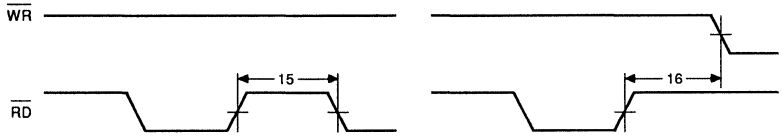
Basic Write Cycle



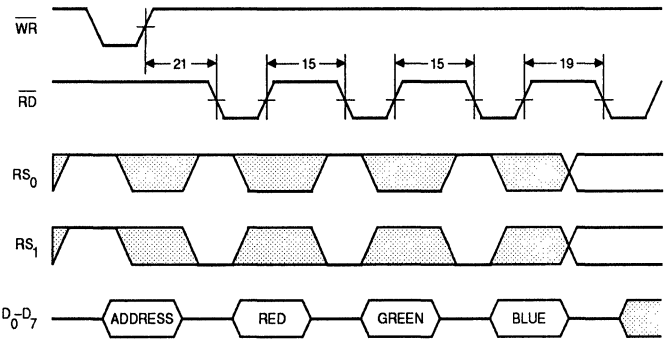
Basic Read Cycle



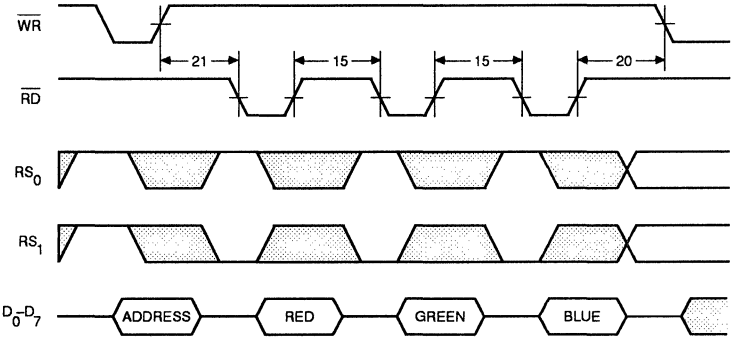
Write to Pixel Mask Register Followed by any Access



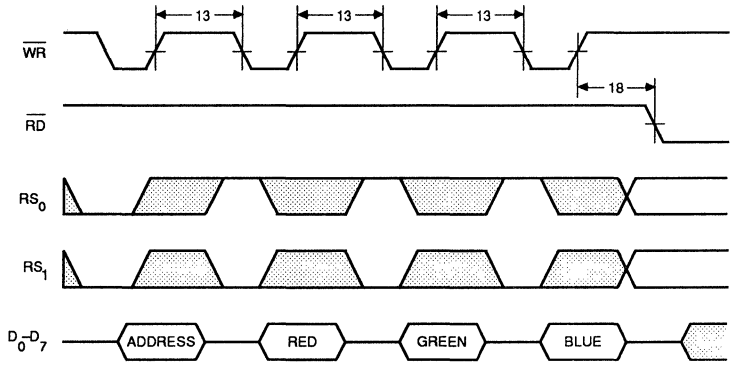
Read From
A. Pixel Mask Register
B. Pixel Address Register (Read Mode)
C. Pixel Address Register (Write Mode)
Followed by Any Access



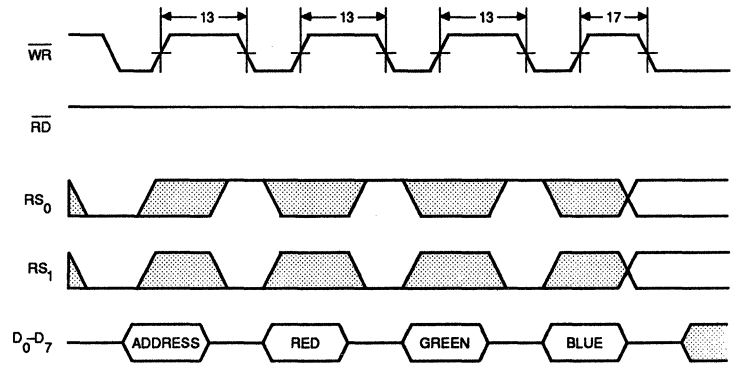
Color Value Read Followed by Any Read



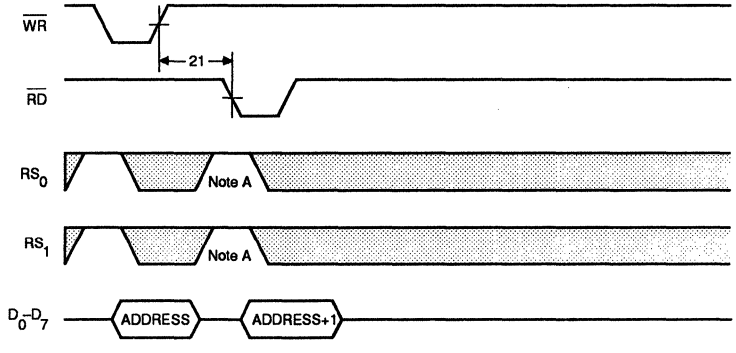
Color Value Read Followed by Any Write



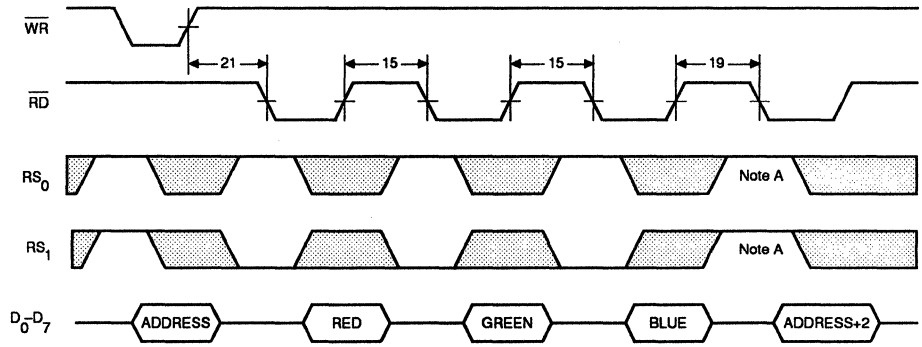
Color Value Write Followed by Any Read



Color Value Write Followed by Any Write



Write and Read Back Read Address Register



Note A: The timing for reading from address 0,0 is identical to that for reading from address 1,1

Read Color Value Then Read Read Address Register

NOTES

Note a: All voltages in this data sheet are with respect to VSS unless specified otherwise.

Note b: The Pixel Clock frequency must be stable for a period of at least 20 µs after power-up (or after a change in Pixel Clock frequency) before proper device operation is guaranteed.

Note c: This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

Note d: VIL(min) = –1.0 V for a pulse width not exceeding 10 ns.

Note e: Reference currents below the minimum specified may cause the analog outputs to become invalid.

Note f: Over the range of the DC Operating Conditions unless specified otherwise.

Note g: IO = IO(max). ICC is dependent on digital output loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

Note h: VCC = max, VSS ≤ VIN ≤ VCC.

Note i: On digital inputs, pins 5–13, 15, 16, 25–27.

Note j: On digital input/output, pins 17–24.

Note k: Tested over the operating temperature range and at nominal supply voltage.

Note l: Full scale error from the value predicted by the design equations.

Note m: About the mid point of the distribution of the three DACs.

Note n: Linearity measured from the least squares best fit line through the DAC characteristic. Monotonicity guaranteed.

Note o: Load = 75 Ω + 30 pF.

Note p: From a 2% change in the output voltage until settling to within 2% of the final value.

Note q: This parameter is sampled, not 100% tested.

Note r: Measured on a BOONTON METER.

Note s: $\overline{READ} \geq$ VIH(min) to disable D0–D7.

Note t: $\overline{BLANK} \leq$ VIL(max) to disable RED, GREEN and BLUE.

Note u: This parameter for allowed variation in the Pixel Colck frequency does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (t_{CHCH}) period specified above.

Note v: It is required that the Pixel Address input to the color look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising edge of PCLK (this requirement includes the blanking period).

Note w: A valid analog output is defined as when the changing analog signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

Note x: Between different analog outputs on the same device.

Note y: Measured ±200 mV from steady state output voltage.

Note z: This parameter allows for synchronization between operations on the microprocessor interface and the pixel stream being processed by the color look-up table.

ORDERING INFORMATION

DEVICE	CLOCK RATE	PACKAGE	PART NUMBER
SC11171	35 MHz	Plastic DIP	SC11171CN-35
SC11171	50 MHz	Plastic DIP	SC11171CN-50
SC11176	65 MHz	Plastic DIP	SC11176CN-65
SC11171	35 MHz	Plastic LCC	SC11171CV-35
SC11171	50 MHz	Plastic LCC	SC11171CV-50
SC11176	65 MHz	Plastic LCC	SC11176CV-65

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FEATURES

- ☐ TTL or CMOS compatible
- ☐ RS-170 and RS-343A compatible
- ☐ Low power (100 mW)
- ☐ Up to 75 MHz update rate
- ☐ Single 5 V operation
- ☐ Internal reference

GENERAL DESCRIPTION

The SC11401, SC11402, SC11403 and SC11404 are monolithic CMOS video Digital to Analog Converters (DACs) that provide RS-170 and RS-343A composite video signals. The 24-pin SC11401 and SC11403 are pin and function compatible with the Telmos TLM1840, and TLM1850 (25 MHz device), but Sierra DACs operate at 40 MHz (Telmos TLM1842 and TLM1852).

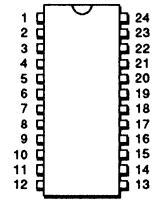
The SC11402 and SC11404 are 20 pin versions in which the Sync Adjust (SADJ), Composite Blank Adjust (CADJ), Bright Adjust (BADJ) and INVERT lines are not brought out. In these devices, INVERT is tied low and data is NOT complemented.

The video DACs take an 8-bit data word, in either true or complement logic, and output a current (Io) with a full scale value set by an external resistor (FS ADJ pin). Normally, the full scale value is adjusted to give 661 millivolts (=255 LSB) across a 75 Ω load. Input data is latched when the CLOCK line is high, and transferred to the output when the CLOCK line goes low. The DACs can be set to zero or full scale with the $\overline{\text{CLEAR}}$ or $\overline{\text{SET}}$ lines, respectively. The $\overline{\text{CLEAR}}$ line requires a clock pulse, just like the data lines, but the $\overline{\text{SET}}$ line is asynchronous and overrides the $\overline{\text{CLEAR}}$ line.

An auxiliary output current (Io') is used when composite video is desired. In this case, Io and Io' are tied together. Their combined values are normally set to 13.33 mA to give a total full scale value (Reference White) of 1,000 mV across a 75 Ω load. Io' is controlled by the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ lines.

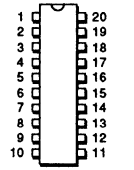
Additionally, Io' can be boosted 28 LSB by pulling the $\overline{\text{BRIGHT}}$ line low. This is useful for intensifying an image.

24-PIN DIP PACKAGE



SC11401CN (40 MHz)
SC11401CN-2 (40 MHz)
SC11403CN (75 MHz)
SC11403CN-2 (75 MHz)

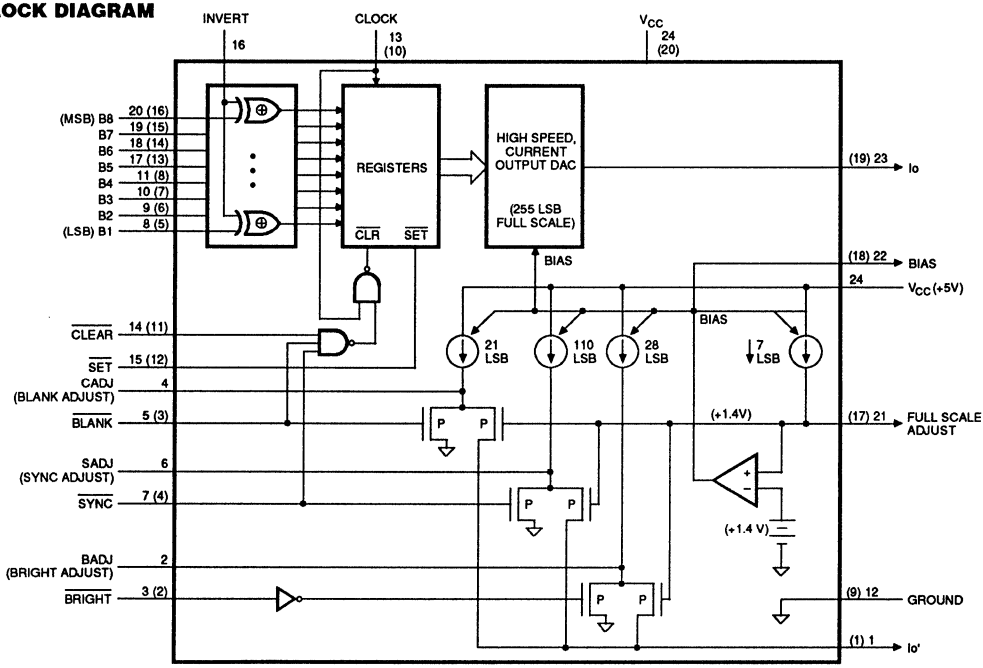
20-PIN DIP PACKAGE



SC11402C (40 MHz)
SC11402CN-2 (40 MHz)
SC11404CN (75 MHz)
SC11404CN-2 (75 MHz)

-2 signifies ± 2 LSB linearity not 1 LSB

BLOCK DIAGRAM



NOTE: NUMBERS NEXT TO SIGNAL NAMES ARE 24-PIN DIP PINS FOR SC11401 AND SC11403. NUMBERS IN ( ) ARE 20-PIN DIP PINS FOR SC11402 AND SC11404.

PIN DESCRIPTIONS (SC11401 AND SC11403)

PIN	NAME	DESCRIPTION
1, 23	Io', Io	Current source outputs. Io is the output of the 8 bit DAC, Io' is the composite output consisting of Sync, Blank, and Bright components.
2, 4, 6	BADJ, CADJ SADJ	Adjust the values of Bright, Blank, and Sync current sources. See Figure 2 for a typical connection. The current that is fed into these pins will sum with their nominal values.
3, 5, 7	$\overline{\text{BRIGHT}}$,	Control the Bright, Blank, and Sync current sources. Note that $\overline{\text{BLANK}}$, $\overline{\text{BRIGHT}}$ turns on the Bright current source by going LOW. $\overline{\text{BLANK}}$ $\overline{\text{SYNC}}$ and $\overline{\text{SYNC}}$ are the opposite.
8–11, 17–20	B1–B8	The data lines. B1 is the LSB line.
12	GND	GND is digital and analog ground.
24	V_{CC}	V_{CC} is +5 V and should be bypassed directly to GND with at least a 0.1 µF capacitor.
13	CLOCK	Strobes in the data on lines B1–B8. Also used to strobe in $\overline{\text{CLEAR}}$. Data is loaded into the registers while the CLOCK line is high, and transferred to the 8 bit DAC when the CLOCK line goes low.
14	$\overline{\text{CLEAR}}$	Sets the 8 bit DAC to zero (Reference Black) if this line is held low while CLOCK is high. $\overline{\text{CLEAR}}$ is overridden by $\overline{\text{SET}}$.
15	$\overline{\text{SET}}$	Asynchronously sets the registers to full scale (all 1's) if pulled low. This sets the DAC to full scale (Reference White) independent of the CLOCK $\overline{\text{CLEAR}}$, $\overline{\text{SYNC}}$ or $\overline{\text{BLANK}}$ lines.
16	INVERT	Complements the data if pulled high. If left low, the data is unchanged on its way to the registers.
21	FS ADJ	Adjusts the full scale output of the DAC. Since Io' tracks Io, its value is also set by this pin. An internal op amp holds this pin at about +1.4 V. A resistor, Rfs, between this pin and GND sets up the full scale current. The current through the resistor (1.4 V/Rfs) represents 7 LSB. Thus full scale (255 LSB) is (1.4 V/Rfs) • (255/7) = 51/Rfs, where Rfs is expressed in Ω. Normally, for a full scale DAC output of 92.5 IRE (92.5/140 = 0.661 V) and a 75 Ω load, one would use a value of 0.661 V/75 Ω = 51/Rfs. This gives a value of about 5780 W for Rfs. Half this value would produce twice the current — as would be the case if the load was a doubly terminated 75 Ω cable (75 Ω resistors on both ends of the cable).
22	BIAS	Internal line for setting up the current sources. It should be bypassed to V_{CC} (+5 V) with a 0.1 µF capacitor.

FUNCTIONAL DESCRIPTION

The SC11401 family of video DACs differ only in pinout and performance. All have a high speed, current output (Io), 8 bit DAC for the video part of the signal and three separate current sources (Sync, Blank, and Bright) compromising the composite signal (Io').

Figure 1 is a functional block diagram of the SC11401 and SC11403. The SC11402 and SC11404 are similar but the SADJ (Sync Adjust), CADJ (Composite Blank Adjust), BADJ (Bright Adjust) and INVERT lines are not brought out—INVERT is tied low—data is NOT complemented.

Data, B1 through B8, comes into the chip where it is complemented if the INVERT line is high. The data then is latched, and the latches drive an 8 bit DAC. The full scale output of the DAC is determined by a resistor connected from the FS ADJ pin to ground (GND). The current through this resistor represents a value of 7 LSB. Voltage across this resistor is held at about 1.4 V by an op amp that holds the resistor voltage at the same potential as an internal 1.4 V reference. The op amp's output, BIAS, should be bypassed to VCC with a 0.1 µF capacitor.

The three current sources that compromise Io' work independently of the 8 bit DAC. However, both $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$, if pulled low, will clear the registers that drive the DAC. The CLOCK line must be high to accomplish this. The DAC's output then goes low when the CLOCK line goes low—register contents are transferred to the DAC when the CLOCK line falls.

ABSOLUTE MAXIMUM RATINGS (Note 1) Operating beyond these limits may damage the device

Supply Voltage, V_{CC}	+6 V
Supply Current (I_{CC})	6 mA
8 Bit DAC Output Current (Io)	30 mA
Drive Current Into Any Pin	±20 mA
Io Output Voltage (Vo)	–10 V to +2.5 V
Io' Output Voltage (Vo')	–0.3 V to +2.5 V
Logic Input Voltage	GND–0.3 V to V_{CC}+0.3 V

OPERATING CONDITIONS

Ambient Temp. = 25°C, V_{CC} = +5.0 V ±5%, GND = 0.0 V. Io nominally adjusted to give a full scale value of 0.661 V across a 75 Ω load.

Operating Current (Typical)			15 mA
Maximum Output Current (Io + Io') at Vo = +1.2 V			33 mA
Maximum Undistorted Output Voltage, Vo			1.5 V
Resolution			8 Bits
Integral Linearity Error (Max.): SC11401, 1, 3, 4			1 LSB
Differential Nonlinearity Error (Max.): SC11401, 2, 3, 4			1 LSB
Full Scale Adjust Reference Voltage: SC11401, 2, 3, 4	1.26 V Min.	1.4 V Typ.	1.54 V Max.
Offset Current with Current Sources Off — Io + Io' = 10 µA Max.			
Io' Match to Io (Io Nominally 255 LSB at Full Scale):			
Sync			110 LSB ±6 LSB
Blank			21 LSB ±2 LSB
Bright			28 LSB ±3 LSB
Logic Levels:			
Logic 0 Input Voltage			0.8 V Max.
Logic 1 Input Voltage			2.4 V Max.
Input Current			50 µA Max.

Dynamic Characteristics (Clock Amplitude 0.8 V to 3.0 V)

	SC11401, 2	SC11403, 4
Update Rate (Min.)	40 MHz	75 MHz
Data Set-Up Time, Tsu	10 ns Min.	6 ns Min.
Data Hold Time, Th	10 ns Min.	6 ns Min.
Clock to Vo Delay (Typ.), Td	15 ns	15 ns
Output Glitch Voltage	60 mV Max.	60 mV Max.
Output Glitch Energy (Typ.)	100 pV-s	100 pV-s

Notes:
1. DATA is an 8 bit binary value shown here in base 10. "X" means that the code has no effect on the output.
2. LSB = Least Significant Bit of DAC = Full Scale/255, where Full Scale is the DAC output (Io) with a code of 1s.
3. IRE = unit of measurement per RS-170 specification. Full scale is defined to be 140 IRE (=1 V) of which 40 IRE are assigned to Sync, 7.5 IRE to Blank, and 92.5 IRE to the video information (the output of the 8 bit DAC). An additional 10 IRE is supplied by the Bright control line (BRIGHT*).
4. The output represents the sum of the two currents Io and Io' into a 75 Ω load. Io is the current from the 8 bit DAC, and Io' is the current from Sync, Blank, and Bright controls.
5. If either $\overline{\text{BLANK}}$ or $\overline{\text{SYNC}}$ are low, the DAC is set to zero (Io = 0). $\overline{\text{CLEAR}}$ = 0 will also set the DAC to zero. $\overline{\text{SET}}$ = 1 sets the DAC to 255 (full scale). $\overline{\text{SET}}$ overrides $\overline{\text{CLEAR}}$, both override DATA.

ELECTRICAL SPECIFICATIONS

DATA (code)	$\overline{\text{BLANK}}$	$\overline{\text{SYNC}}$	$\overline{\text{BRIGHT}}$	Output, Expressed in: LSB	IRE	VOLTS
X	0	0	1	0	0.0	0.000
X	1	0	1	21	7.5	0.054
X	0	0	0	28	10.0	0.073
X	0	1	1	110	40.0	0.285
0	1	1	1	131	47.5	0.339
1	1	1	1	132	47.9	0.342
2	1	1	1	133	48.2	0.345
:	:	:	:	:	:	:
:	:	:	:	:	:	:
255	1	1	1	386	140.0	1.000
255	1	1	0	414	150.0	1.073

255 LSB 92.5 IRE

Table 1. Output Signal vs. Data and Control Lines

Figure 2 shows a typical video application. Notice that Io and Io' are tied together. If the composite signal is not dersired, Io' can be connected to ground. The Sync, Blank, and Bright current sources are adjusted by three individual potentiometers connected between +5 V and ground. Normally, these components aren't used since the composite video signals are pre-set to their nominal values. Full scale adjustment is achieved using a fixed resistor in series with a potentiometer to give a combined sum of about 5780 Ω.

Figure 3 shows a typical composite video signal.

Figure 4 is a timing diagram. Data is clocked into the registers while the CLOCK line is high and transferred to the DAC when the CLOCK line goes low.

Figure 5 shows a non-video application of the SC11401. In this situation, Io' is not used and is left floating. $\overline{\text{BRIGHT}}$ is tied low and $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ are tied high. This shuts off the current sources of Io' and thus reduces power dissipation.

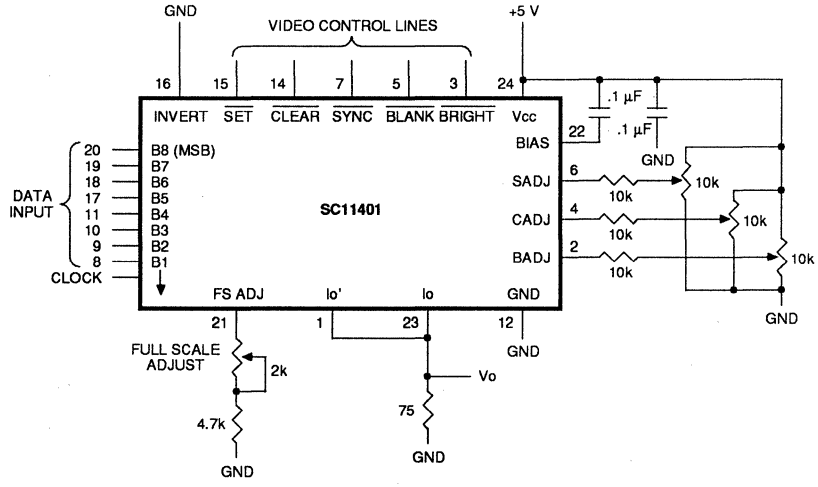


Figure 2. Typical Video Application
The BADJ, CADJ, and SADJ Adjustments are Optional.

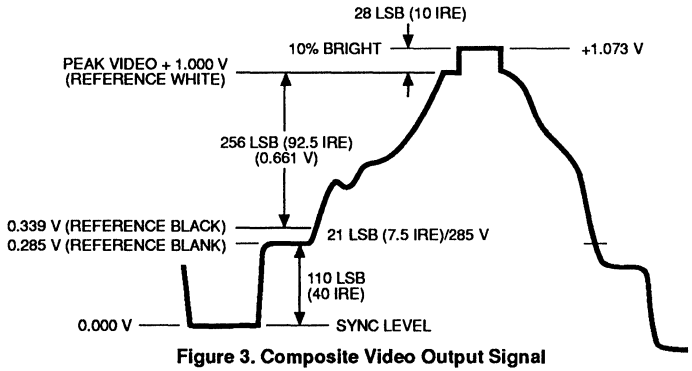


Figure 3. Composite Video Output Signal

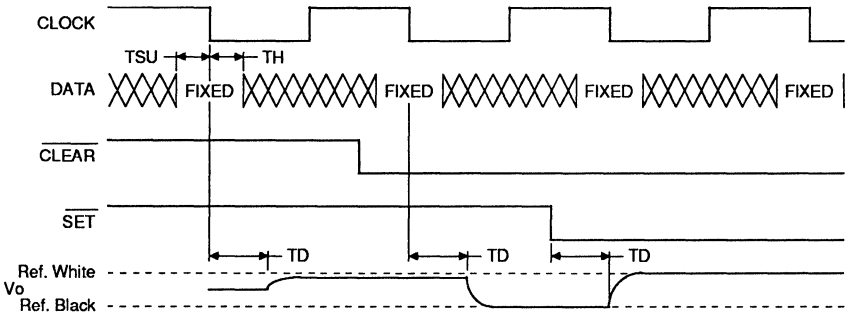


Figure 4. Timing Diagram

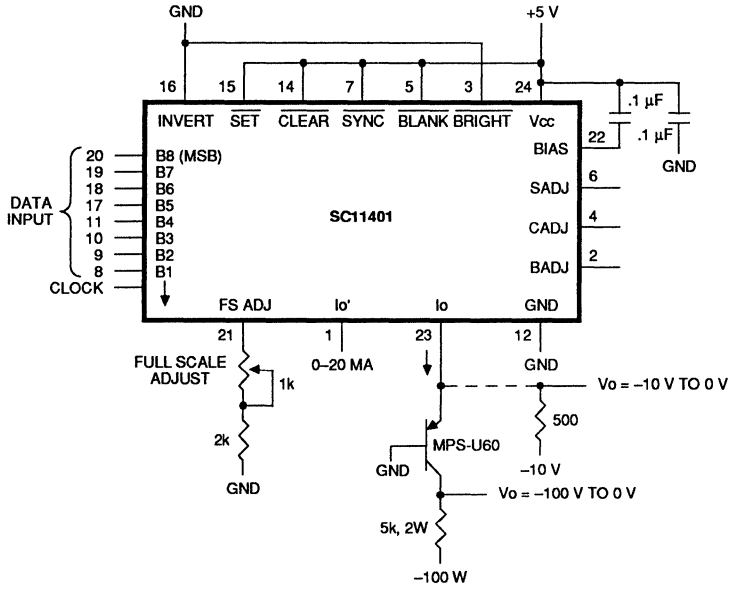


Figure 5. Non-Video Application: High speed DAC with 10 V or 100 V output swing. $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ are pulled high while $\overline{\text{BRIGHT}}$ is low and Io' is left open. This minimizes power consumption by effectively turning off the Io' current sources. The SC11401 can directly drive a 500 Ω load connected to a –10 V supply. For higher voltage swings, a high voltage PNP transistor, such as the MPS-U60 can be used, along with a 5K, 2 Ω resistor.

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FEATURES

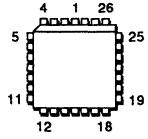
- ☐ On chip Phase Lock Loop with VCO for clock generation
- ☐ Set of 8 programmed frequencies
- ☐ Single mask option to create customer specific frequency set
- ☐ Microprocessor serial interface for unique frequencies
- ☐ Anti-jitter circuitry
- ☐ Provision for external frequency input
- ☐ Maximum frequency - 100 Mhz
- ☐ Low power CMOS technology
- ☐ Single 5 Volt power supply
- ☐ Small footprint - 16 pin SOIC, 20 pin DIP, 28 pin PLCC

GENERAL DESCRIPTION

The SC11410/SC11411 is a digitally controlled frequency synthesizer capable of generating any one of 8 video dot clock frequencies. Externally generated system bus clock (14.318 Mhz) may be used as the reference frequency, alternatively a crystal can be used without additional components. In addition to the programmed frequencies (shown in Table 1), the SC11410 can be programmed by a microprocessor through the serial interface to generate any desired frequency, within VCO frequency range. The microprocessor serial interface circuitry is not supported by the SC11411 circuit.

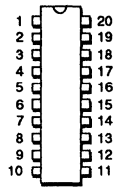
The SC11410/SC11411 is designed using advanced 1.5 micron double metal, double poly CMOS technology to provide a small footprint and cost effective generation of video dot clocks. Frequency outputs are compatible with VGA, EGA, MCGA, CGA, MDA as well as the higher frequencies needed for advanced applications.

28-PIN PLCC PACKAGE



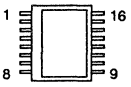
SC11410CV

20-PIN PDIP PACKAGE



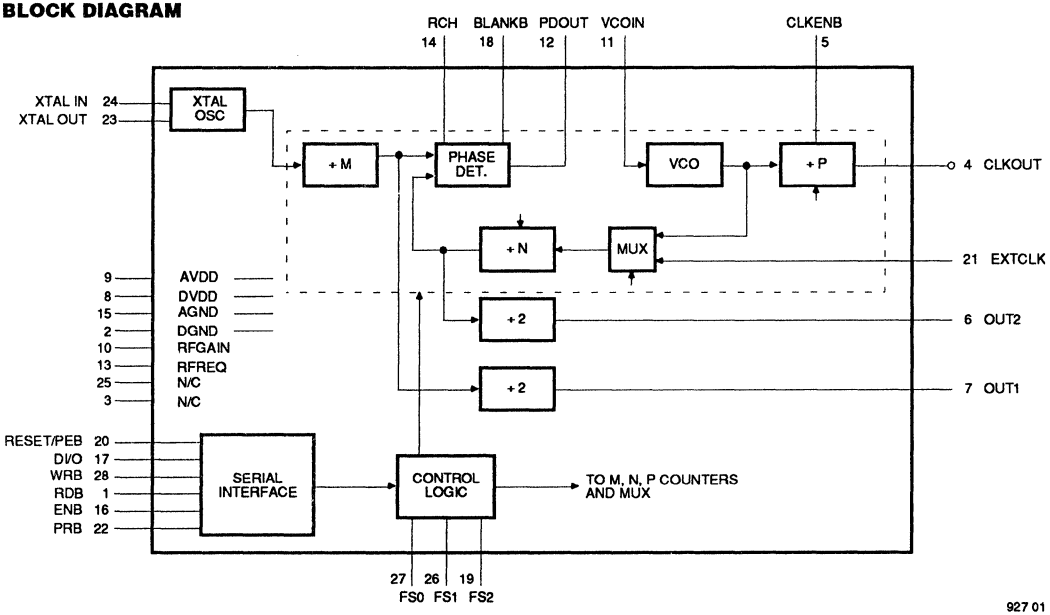
SC11411CN

16-PIN SOIC PACKAGE



SC11411CM

BLOCK DIAGRAM



927 01

Note: The pin numbers shown are for the 28 pin PLCC package only.

Figure 1.

CIRCUIT DESCRIPTION

A block diagram of the chip is shown in Figure 1. The oscillator and the VCO output is divided by M and N integer numbers in the range of 1 to 127. The divided outputs are phase-locked to each other by the PLL circuit. The VCO output is divided by the post scaler modulo "P". The VCO output frequency (CLKOUT) can be calculated by using the following equation:

CLKOUT = (N/MP)*Fosc
where
Fosc = Oscillator frequency (at XTALIN pin)
P = 1,2,4,8
M,N = 1 to 127 (divide ratios of 0 and 1 will be divided by 1)

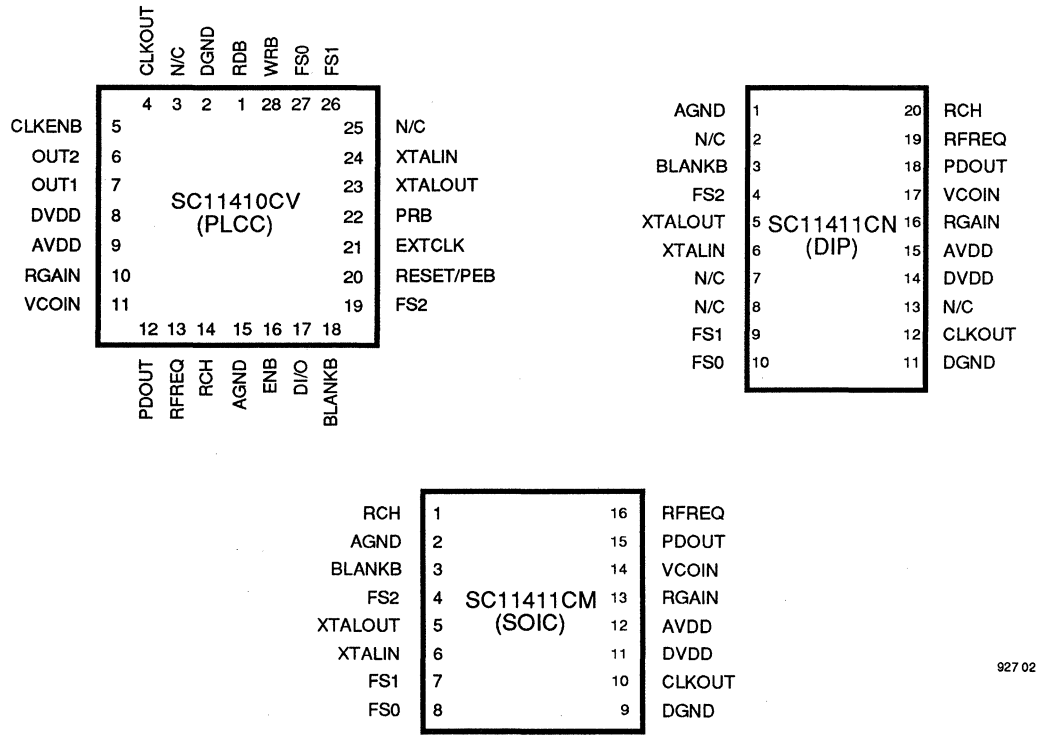
The SC11410 supports two frequency program modes: Internal frequency selection mode and the External frequency program mode. In the Internal mode, input pins FS0,FS1 and FS2 are used to make the frequency selection from 8 preprogrammed frequencies. Customer specific frequency sets can be easily implemented via a single level metal mask change.

In the External mode, the frequency program code is supplied through the microprocessor serial interface. In this mode any frequency within the available VCO frequency range can be generated.

The RESET/PEB pin is used to select the mode. In applications where only the internal mode is desired the RESET/PEB pin should be permanently tied to a logic one. In applications using the microprocessor serial interface, the RESET/PEB pin should be tied to a Power-On Reset signal.

Additionally, the SC11410 has an External Clock mode (selected by the serial data bit: DS3) where the PLL is disabled and the EXTCLK signal is divided by (N*2) and is fed to the OUT2 pin. The XTALIN Signal is divided by (M*2) and is available on the OUT1 pin. This mode can only be accessed via the serial interface. When using this external clock mode, the CLKOUT signal should be disabled by tying CLKENB pin to a logic one.

CONNECTION DIAGRAM



927 02

PIN DESCRIPTION

NAME	DESCRIPTION
DI/O	Data I/O pin. Used to read from or write into the serial shift register. (Internal pullup).
RDB	Input. Read strobe, active low. (Internal pullup)
WRB	Input. Write strobe, active low. (Internal pullup)
ENB	Input. Enable read or write, active low. (Internal pullup).
RESET/PEB	Input. Serial programming enable. When this signal is high pre-programmed frequencies can be selected. When low, a desired frequency can be programmed by the microprocessor through serial interface. (Internal pullup)
PRB	Input. Pointer reset, active low. Initialize the serial interface pointer. Any read or write operation to the serial shift register (DS) should be preceded by a pointer reset. (Internal pullup)
FS[2:0]	Inputs. Frequency select lines for pre-programmed frequencies.
XTALIN	Crystal oscillator input. AC coupled TTL or a CMOS level signal can be applied.
XTALOUT	Crystal oscillator output.
EXTCLK	External frequency Input. (Internal pullup).
DVDD	Digital positive supply
AVDD	Analog positive supply
DGND	Digital ground.
AGND	Analog ground
BLANKB	Input. When low, the R2 resistor of the phi loop filter is shorted by an on-chip switch.
OUT2	Output. Output signal from N divider, divided by two.
OUT1	Output. Output signal from M divider, divided by two.
RGAIN	Resistor to set VCO gain (bandwidth) is connected between this pin and the ground.
RFREQ	Resistor to set the minimum frequency of the VCO is connected between this pin and the ground.
CLKENB	Input. When pulled down, CLKOUT drives out, when high CLKOUT is tri-stated. (Internal pulldown).
PDOUT	Phase detector output (drives loop filter).
VCOIN	VCO input control voltage. Loop filter is connected between this pin and PDOUT.
RCH	Resistor to set the charge pump current is connected between this pin and the ground.
CLKOUT	VCO clock output. Disabled when CLKENB is selected.

MICROPROCESSOR INTERFACE

The microprocessor interface is designed to work with the "PC" bus with minimum external logic. The serial interface consists of an 18 bit shift register DS[17:0]. READ/WRITE operations are performed using DI/O, RDB, WRB, ENB and PRB signals. The shift register is defined as shown in Figure 2.

DS0: Mode select bit.

DS0 = 1 - Internal mode (frequency determined by FS0 - FS2 inputs)

DS0 = 0 - External mode (frequency determined by the serial data)

The DS0 bit is set to "1" when RESET/PEB pin is forced high, when RESET/PEB goes low the DS0 bit will stay high until altered by the serial interface. This assures proper operation when the serial interface is not used.

DS[2:1]: Auxiliary VCO output divider

This post scaler permits restricted VCO range, which is helpful in optimizing for low jitter.

DS2	DS1	CLKOUT
0	0	VCOOUT
0	1	VCOOUT/2
1	0	VCOOUT/4
1	1	VCOOUT/8

DS3: Programmable divider clock select

DS3 = "1" - EXTCLK is selected as counter clock.

DS3 = "0" - VCO is selected as counter clock.

VCO is disabled when EXTCLK is selected.

DS[10:4]: VCO divider control word (N).

DS10 is MSB and the DS4 is LSB.

DS[17:11]:VCO divider control word (M).

DS17 is MSB and DS11 is LSB.

The serial interface control section consists of DI/O, RDB, WRB, ENB, and PRB control signals. A read or a write to the serial shift register should be preceded by the pointer reset (PRB) for at least one cycle. The pointer reset can be applied by the microprocessor by writing D1="0" (D0, D2..D7=" Don't care) into SC11410 followed by either read or write operation. When the SC11410 is addressed by the processor (ENB="0"), any I/O read or write operation will cause the contents of the shift register to be shifted by one place. The SC11410 shift register can be read after applying a pointer reset followed by 18 consecutive reads. The contents of the shift register will be shifted out one bit at a time on the DI/O pin of the SC11410 chip. The shift register can be written by the microprocessor by applying a pointer reset followed by 18 consecutive writes (D0 =data bits, D1 = 1 and D[7:2] = X) to the SC11410 shift register.

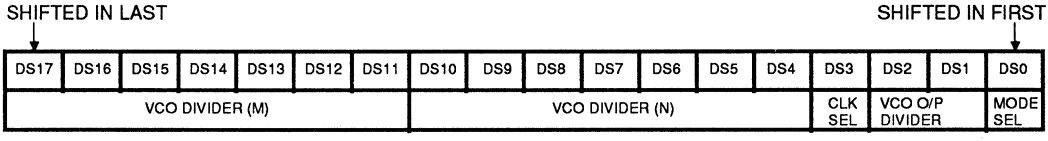


Figure 2. Microprocessor Interface Shift Register

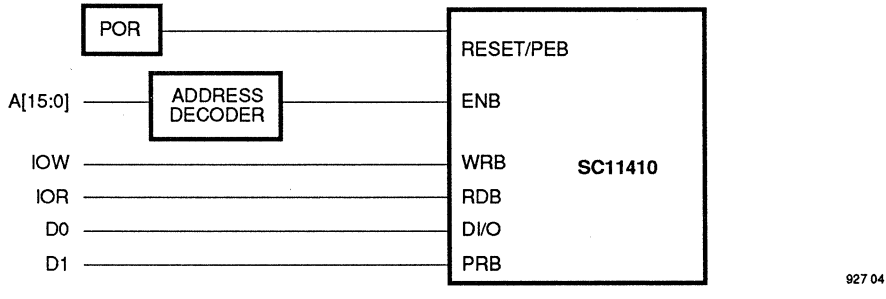


Figure 3. PC Bus Interface to SC11410

FREQUENCY SELECT LINES

In the internal mode, three pins labeled FS0,FS1 and FS2 select the output frequency from eight pre-programmed frequencies. The following is the list of pre-programmed frequencies for an oscillator frequency of 14.31828 Mhz.

The chip is metal mask programmable, and a new list of frequencies can be easily generated by changing the metal mask.

PHASE LOCK LOOP (PLL) CIRCUIT

The PLL circuit is shown in Figure 4. The phase detector is implemented with switched current sources that provide current pulses (phase -error signals) to the low pass filter.

A charge pump converts the logic states of the phase detector into analog signals suitable for controlling the VCO. The charge pump current is determined by the external resistor RCH, and its value is given by

ICH = 1.25V/RCH; RCH ~ 1.6K-Ohm (typical)

An external filter is used to smooth the VCO control voltage. The states of the PFD are determined by the edges of the input wavefroms. If the R-input (reference) phase leads the V-input (VCO) phase, then an edge of R input sets the U (up) terminal true. The next V edge resets the U terminal false. Conversely, if V leads R, a V edge sets D (down) true and the next R edge resets D false. Both U and D can be false simultaneously, or either one alone can be true, but both can never be true simultaneously. Therefore a phase detector has three allowable states at its two output terminals, up (U), down (D), and neutral (N).

A typical circuit for the charge-pump and a loop-filter is shown in Figure 5.

PLL CIRCUIT OPERATING EQUATIONS

The VCO frequency is set by a stable internal band-gap reference, by input voltage VCOIN, and by two external resistors: RFREQ and RGAIN. The oscillator frequency is a function of the current IBIAS, which is the sum of currents determined by the on-chip reference and the VCOIN voltage.

EQ #1

$$IBIAS = \frac{VCOIN}{RGAIN} + \frac{2.2}{RFREQ}$$

Units: IBIAS – micro amps
RGAIN, RFREQ – MΩ
VCOIN is nominal filter voltage (1V – 3V), nominal value is 2V.

FS2	FS1	FS0	DESIRED FREQUENCY	N/M	POST SCALER	CLKOUT	UNITS
0	0	0	25.175	102/29	1/2	25.1804	Mhz
0	0	1	28.321	91/23	1/2	28.3253	Mhz
0	1	0	32.500	59/13	1/2	32.4915	Mhz
0	1	1	44.900	69/22	1/1	44.9073	Mhz
1	0	0	50.350	109/31	1/1	50.3450	Mhz
1	0	1	65.000	59/13	1/1	64.9830	Mhz
1	1	0	38.000	69/26	1/1	37.9985	Mhz
1	1	1	40.000	81/29	1/1	39.9924	Mhz

Table 1. Programmed Frequencies for 14.31828 MHz crystal

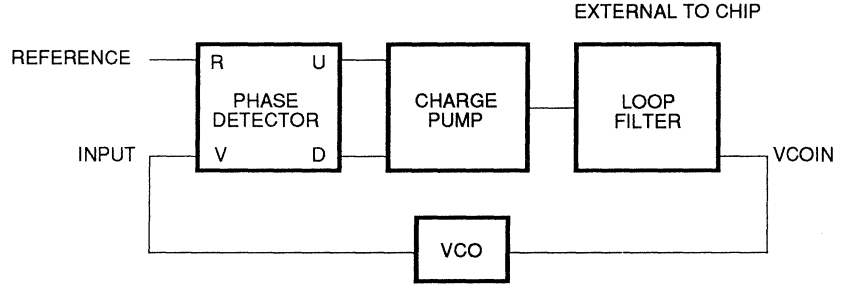


Figure 4. PLL with Three-State Phase Detector and Charge Pump

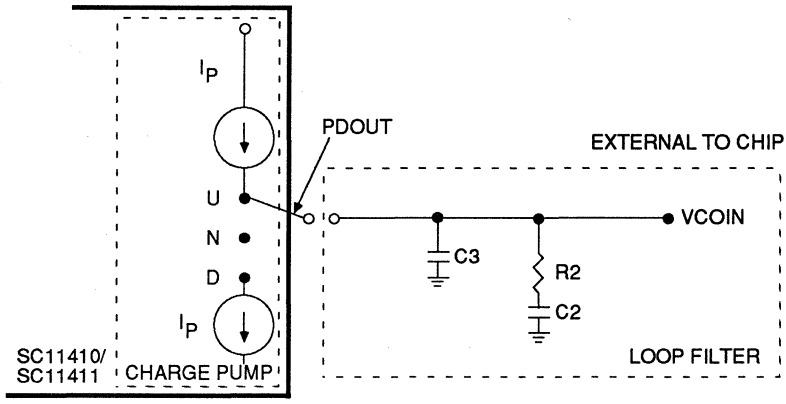


Figure 5. Charge Pump and the Loop Filter

The following equation describes the frequency output of the VCO (FVCO), which is also the input to the post-scaler.

EQ #2

$$FVCO = \frac{1000}{\frac{4400}{IBIAS} + 3}$$

Unit: FVCO is in Mhz

In general, FVCO should be greater than 10MHz (FVCOmin) but less than 100 Mhz (FVCOmax). The range of FVCOmax / FVCOmin is defined by EQ 3, and in general, ranges from 1 to 3.

EQ #3

$$\frac{FVCOmax}{FVCOmin} \cong \frac{3 + 2.2\,(RGAIN/RFREQ)}{1 + 2.2\,(RGAIN/RFREQ)}$$

Selecting the desired FVCOmin and FVCOmax frequencies allows calculation of IBIAS. Knowing IBIAS and further selecting the desired range of VCOIN (about the nominal voltage) allows calculation of RGAIN and RFREQ.

EQ #4

$$IBIASmin = \frac{4400}{\frac{1000}{FVCOmin} - 3}$$

EQ #5

$$IBIASmax = \frac{4400}{\frac{1000}{FVCOmax} - 3}$$

Solving equation #1

$$RGAIN = \frac{VCOINmax - VCOINmin}{IBIASmax - IBIASmin}$$

$$RFREQ = \frac{2.2V}{IBIASmax - 3V/RGAIN}$$

Units: RFREQ and RGAIN are in mega-Ohms

ANTI-JITTER CIRCUITRY

The SC11410/SC11411 includes an anti-jitter circuitry to minimize the jitter on the generated frequency. The phase detector circuit has a control signal (BLANKB) that, in essence, changes the response of the low pass filter. In video application BLANKB signal can be used in conjunction with the ⩛ loop-filter (shown in figure 6) to minimize the jitter. When BLANKB goes low, the filter response time is reduced and consequently phase correction will be faster. When BLANKB is pulled high, the voltage variation at VCO input will slow down resulting in slower phase correction and less jitter. For video dot clock generation, the BLANKB input can be driven by a horizontal sync signal so that phase corrections will be more rapid during the retrace interval.

To optimize for low jitter, the designer must address several critical circuit areas, including PC board layout, power supply bypassing, low pass filter response, and VCO frequency range.

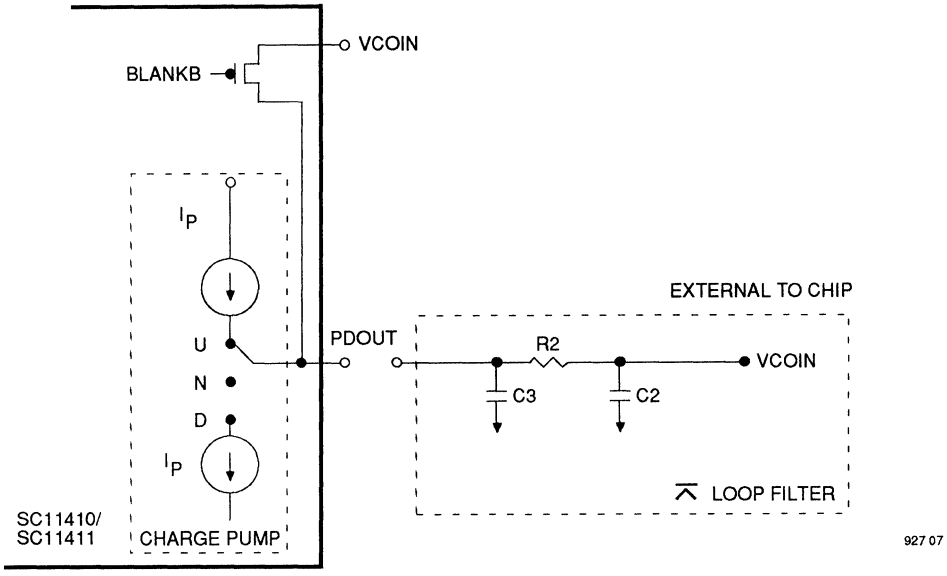


Figure 6. Charge Pump and the $\overline{\wedge}$ Loop Filter

ABSOLUTE MAXIMUM RATINGS (NOTES 1–3)

Supply Voltage, AVDD, DVDD	7 V
DC Input Voltage	GND–0.5 to V_{CC} +0.5 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

OPERATING CONDITIONS

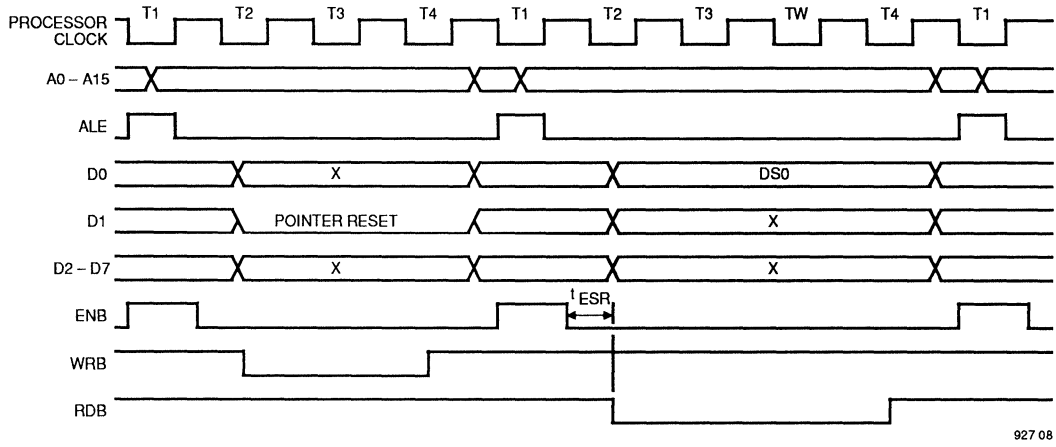
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
GND	Ground			0		V
XTLIN, XTLOUT	Crystal Frequency			14.3	30	MHz
T_R, T_F	Input Rise or Fall Time				50	ns

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

DC ELECTRICAL CHARACTERISTICS (T_A = 0 TO 70°C, V_{CC} = +5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	AVDD & DVDD Quiescent Current			30		mA
V_{IH}	High Level Input Voltage, All Inputs		2.2			V
V_{IL}	Low Level Input Voltage, All Inputs				0.8	V
V_{OH}	High Level Output, All Outputs Except XTLOUT (I_{OH} = 0.5 mA) (I_{OH} = 100 µA)		 2.4 4.5			 V V
V_{OL}	Low Level Output, All Outputs Except XTLOUT (I_{OL} = 1.6 mA) (I_{OL} = 100 µA)				 0.6 0.2	 V V
V_{OH}	High Level Output XTLOUT (I_{OH} = 20µA)		 4			 V
V_{OL}	Low Level Output XTLOUT (I_{OL} = 20 µA)				 0.2	 V

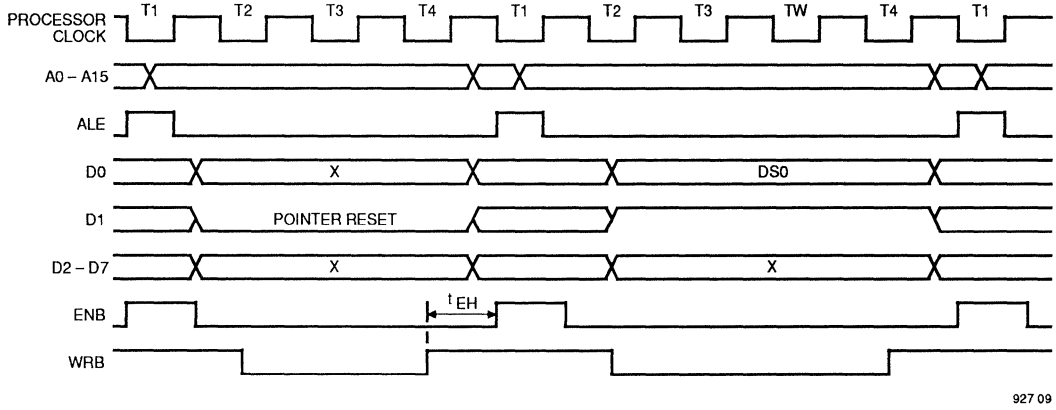
TIMING DIAGRAMS



t_{ESR} – Enable Setup Time (Min. 50ns)

X – Don't Care

Figure 7. SC11410 Microprocessor Interface Read Bus Cycle Timings



ENB – Enable signal generated external to the chip

t_{EH} – Enable Hold Time Min. 50ns

X – Don't Care

Figure 8. SC11410 Microprocessor Interface Write Bus Cycle Timings

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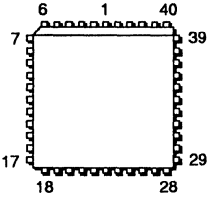
FEATURES

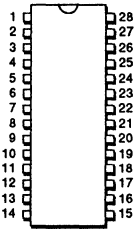
- ☐ Personal System/2™ Compatible
- ☐ 80 MHz Pipelined Operation
- ☐ Triple 6-bit or 8-bit D/A Converters
- ☐ 256 Word Color Palette RAM
- ☐ 15 Overlay Registers (SC11471/478)
- ☐ RS-343A/RS-170 Compatible Outputs
- ☐ Sync on all Three Channels (SC11471/478)
- ☐ Anti-Sparkle Circuitry
- ☐ Programmable Pedestal (SC11471/478)
- ☐ External Voltage or Current Reference
- ☐ Standard MPU Interface
- ☐ +5V CMOS Monolithic Construction
- ☐ Available Clock Rates
  - 80 MHz • 50 MHz
  - 66 MHz • 35 MHz

44-PIN PLCC PACKAGE



SC11471CV
SC11476CV
SC11478CV

28-PIN DIP PACKAGE



SC11476CN

GENERAL DESCRIPTION

The SC11471, SC11476 and SC11478 are pin-compatible and software-compatible Color Palettes designed specifically for Personal System/2™ compatible color graphics. The SC11476 is also available in a 28-pin DIP package that is pin compatible with the IMSG176.

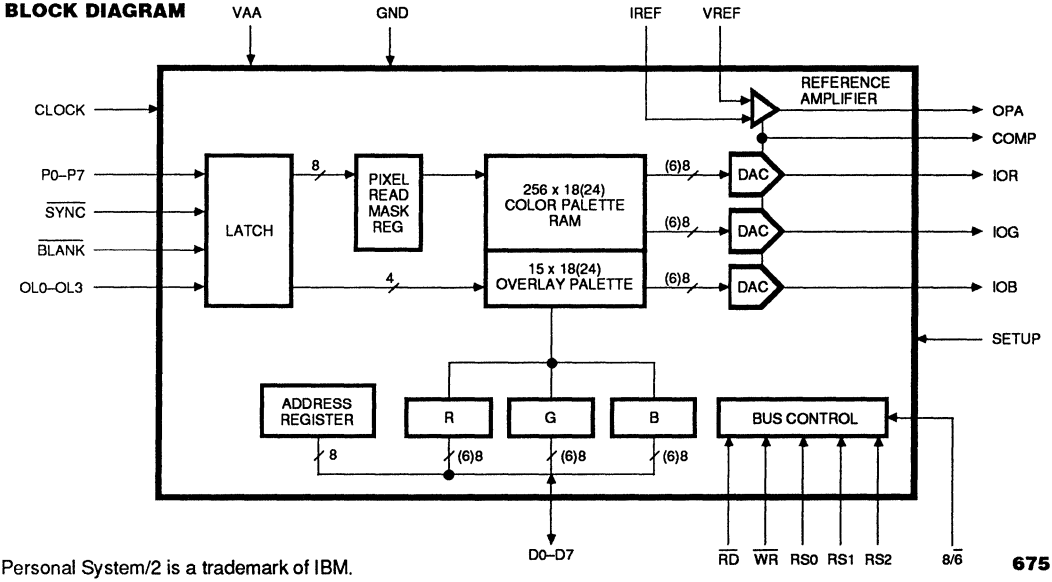
The SC11471 has a 256 x 18 color lookup table with triple 6-bit video D/A converters. The SC11478 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. It may be configured for either 6 bits or 8 bits per color operation.

The SC11471 and SC11478 also include 15 overlay registers to provide for overlaying cursors, grids, menus, EGA emulation, etc. Sync generation on all three channels, a programmable pedestal (0 or 7.5 IRE), and use of either an external voltage or current reference is also supported.

The SC11476 is similar to the SC11471, but has no overlays or sync information on the analog outputs.

The SC11471/476/478 generate RS-343A compatible red, green, and blue video signals, and are capable of driving doubly-terminated 75 Ω coax directly, and generate RS-170 compatible video signals into a singly-terminated 75 Ohm load, without requiring external buffering.

BLOCK DIAGRAM



Personal System/2 is a trademark of IBM.

FUNCTIONAL DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the SC11471/476/478 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers.

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address register (RAM write mode)
0	1	1	Address register (RAM read mode)
0	0	1	Color palette RAM
0	1	0	Pixel read mask register
1	0	0	Address register (overlay write mode)
1	1	1	Address register (overlay read mode)
1	0	1	Overlay registers
1	1	0	Reserved

Table 1. Control Input Truth Table

Writing Color Palette RAM and Overlay Color Data

To write color data, the MPU writes the address register (selecting RAM write or overlay write mode) with the address of either the color palette RAM location or the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select either the color palette RAM or the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the SC11471/476) and written to the location specified by the address register. The address register then increments to the next location which MPU may modify by simply writing another sequence of red, green and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Color Palette RAM and Overlay Color Data

To read color data, the MPU loads the address register (selecting RAM or overlay read mode) with the address of the color palette RAM location or overlay register to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select either the color palette RAM or overlay registers. Following the blue read cycle, the contents of the color palette RAM or the contents of the overlay location specified by the address register are copied into the R, G, B registers and the address register gets incremented again. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the four most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. As only one pixel clock cycle is required to complete the transfer, the color palette RAM and overlay registers may be accessed at any time with no noticeable disturbance on the display screen.

To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMS or the overlay registers, an internal anti-sparkle logic is implemented to maintain the previous output color data on the three D/A Converters output while the transfer between the color look-up table RAMS and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

SC11471/476 Data Bus Interface

Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

SC11478 Data Bus Interface

On the SC11478, the 8/$\overline{6}$ control input is used to specify whether the MPU is reading and writing 8-bits (8/$\overline{6}$ = logical one) or 6-bits (8/$\overline{6}$ = logical zero) of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation (and also when using the SC11471/476), color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero. Note that in the 6-bit mode, the SC11478's full scale output current will be about 1.5% lower than when it is in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being logic zero in the 6-bit mode.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the SC11471/476) of color information to the three D/A converters.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 1 and 2. Tables 4 and 5 detail how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs modify the output levels.

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal is to be used. Note that the SC11476 generates only a 0 IRE blanking pedestal (Figure 2).

The analog outputs of the SC11471/476/478 are capable of directly driving a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

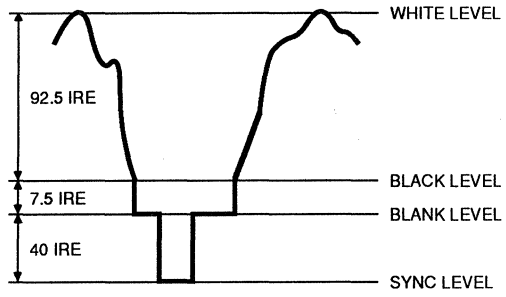
	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				Red value Green value Blue value
ADDR0–7 (counts binary)	$00-$FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	Color palette RAM Reserved Overlay Color 1 : Overlay Color 15

Table 2. Address Register (ADDR) Operation

OL0–OL3	P0–P7	Addressed by Frame Buffer
$0	$00	Color Palette RAM Location $00
$0	$01	Color Palette RAM Location $01
:	:	:
$0	$FF	Color Palette RAM Location $FF
$1	$xx	Overlay Color 1
:	$xx	:
$F	$xx	Overlay Color 15

Table 3. Pixel and Overlay Control Truth Table. (Pixel Read Mask Register = $FF)

SC11471/478 w/o SYNC		SC11471/478 with SYNC	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, SETUP = VAA, VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

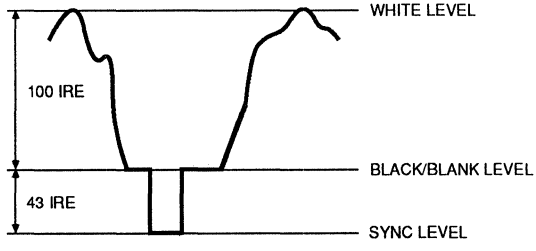
Figure 1. Composite Video Output Waveforms (SETUP = VAA)

Description	SC11471/478 IOUT (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	Data + 9.05	1	1	Data
DATA–SYNC	Data + 1.44	0	1	Data
BLACK	9.05	1	1	$00
BLACK–SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75 doubly-terminated load, SETUP = VAA, VREF = 1.235 V, RSET = 147 .

Table 4. Video Output Truth Table (SETUP = VAA)

SC11476 or SC11471/478 w/o Sync		SC11471/478 with Sync	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.256
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load, SETUP = GND. VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms (SETUP = GND)

Description	SC11476 IOUT (mA)	SC11471/478 IOUT (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	17.62	26.67	1	1	$FF
DATA	Data	Data + 8.05	1	1	Data
DATA-SYNC	Data	Data	0	1	Data
BLACK	0	8.05	1	1	$00
BLACK-SYNC	0	0	0	1	$00
BLANK	0	8.05	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load, SETUP = VAA, VREF = 1.235 V, RSET = 147 Ω.

Table 5. Video Output Truth Table (SETUP = GND)

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
$\overline{BLANK}$	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 4 and 5. It is latched on the rising edge of CLOCK. When $\overline{BLANK}$ is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal.
$\overline{SYNC}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1 and 2). $\overline{SYNC}$ does not override any other control or data input, as shown in Tables 4 and 5; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not to be generated on the analog outputs, this pin should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, $\overline{SYNC}$, and $\overline{BLANK}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75 Ω coaxial cable (Figures 3 and 4).

<table>
<tr><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>IREF</td><td>Full scale adjust control. Note that the IRE relationships in Figures 1 and 2 are maintained, regardless of the full scale output current.

When using an external voltage reference (Figure 3), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is:

RSET (Ω) = K • 1000 • VREF (V)/Iout (mA)

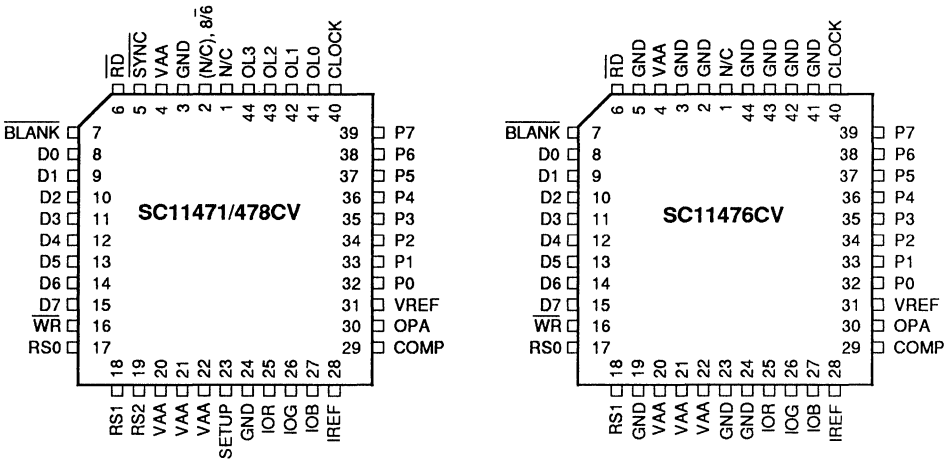
K is defined in the table below for doubly-terminated 75 Ω loads. It is recommended that a 147 Ω RSET resistor be used.

When using an external current reference (Figures 4 and 5) the relationship between IREF and the full scale output current on each output is:

IREF (mA) = Iout (mA)/K

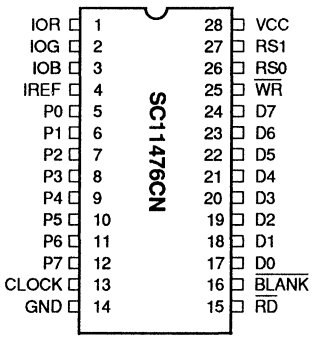
<table>
<tr><th>Part Number</th><th>Mode</th><th>Pedestal</th><th>K</th></tr>
<tr><td>SC11478</td><td>6-bit
8-bit
6-bit
8-bit</td><td>7.5 IRE
7.5 IRE
0.0 IRE
0.0 IRE</td><td>3.170
3.195
3.000
3.025</td></tr>
<tr><td>SC11471</td><td>6-bit</td><td>7.5 IRE
0.0 IRE</td><td>3.170
3.000</td></tr>
<tr><td>SC11476</td><td>6-bit</td><td>0.0 IRE</td><td>2.100</td></tr>
</table>
</td></tr>
<tr><td>COMP</td><td>Compensation pin. If an external voltage reference is used (Figure 3), this pin should be connected to OPA. If an external current reference is used (Figure 4), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum.</td></tr>
<tr><td>VREF</td><td>Voltage reference input. If an external voltage reference is used (Figure 3), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 4), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figures 3 and 4. The decoupling capacitor must be as close to the device as possible to keep the lead lengths to an absoloute minimum.</td></tr>
<tr><td>OPA</td><td>Reference amplifier output. If an external voltage reference is used (Figure 3), this pin must be connected to COMP. When using an external current reference (Figure 4), this pin should be left floating.</td></tr>
<tr><td>VAA</td><td>Analog power. All VAA pins must be connected.</td></tr>
<tr><td>GND</td><td>Analog ground. All GND pins must be connected.</td></tr>
<tr><td>$\overline{WR}$</td><td>Write control input (TTL compatible). D0–D7 data is latched on the rising edge of $\overline{WR}$, and RS0–RS2 are latched on the falling edge of $\overline{WR}$ during MPU write operations.</td></tr>
<tr><td>$\overline{RD}$</td><td>Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS0–RS2 are latched on the falling edge of $\overline{RD}$ during MPU read operations.</td></tr>
<tr><td>RS0, RS1, RS2</td><td>Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation RS2 being performed, as illustrated in Tables 1 and 2.</td></tr>
<tr><td>D0–D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.</td></tr>
<tr><td>8/$\overline{6}$</td><td>8-bit/$\overline{6}$-bit select input (TTL compatible). This bit specifies whether the MPU is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant bit during color read/write cycles (D6 and D7 are ignored during color write cycles and logical zero during color read cycles). This bit is implemented only on the SC11478.</td></tr>
</table>

CONNECTION DIAGRAM



44-Pin PLCC

N/C pins may be left unconnected without affecting the performance of the SC11471/476/478. Names in parentheses are pin names for SC11471.



28-Pin DIP

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

The layout should be optimized for lowest noise on the SC11471/476/478 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all SC11471/476/478 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the SC11471/476/478, the analog output traces, and all the digital signal traces leading up to the SC11471/476/478.

Power Planes

The SC11471/476/478 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figures 3, 4 and 5. This bead should be located within three inches of the SC11471/476/478.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all SC11471/476/478 power pins and current/voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that

portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the SC11471/476/478 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the SC11471/476/478 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the SC11471/476/478 should be avoided to reduce noise pickup.

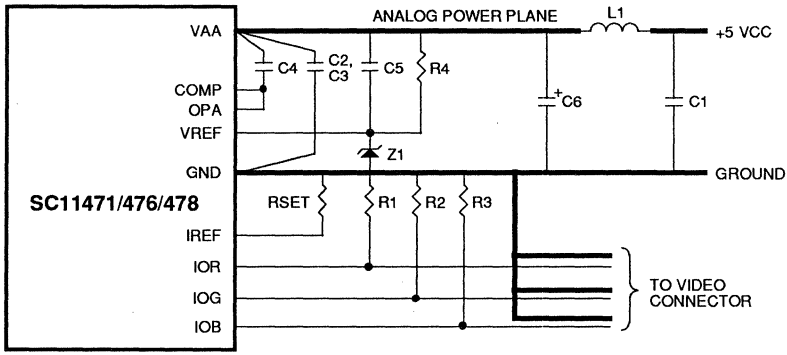
Any active termination resistors for the digital inputs should be connected to the regular PCB power plane, and not the analog power plane.

Analog Signal Interconnect

The SC11471/476/478 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

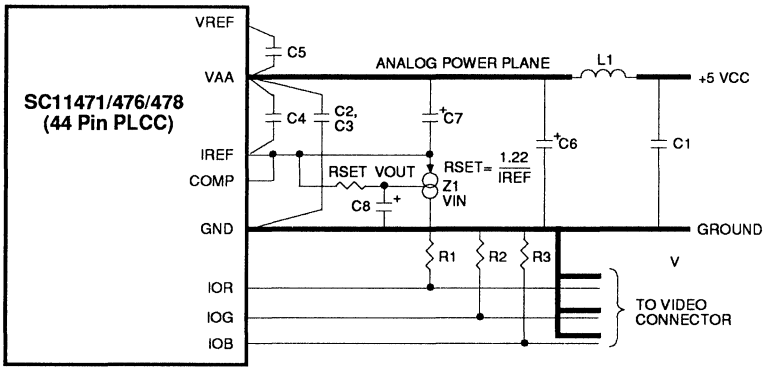
For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the SC11471/476/478 to minimize reflections.



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Tantalum Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
RSET	1% Metal Film Resistor	Dale CMF-55C
Z1	1.2 V Voltage Reference	National Semiconductor LM385BZ-1.2
R4	1K Ω 5% Resistor	

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11471/476/478.

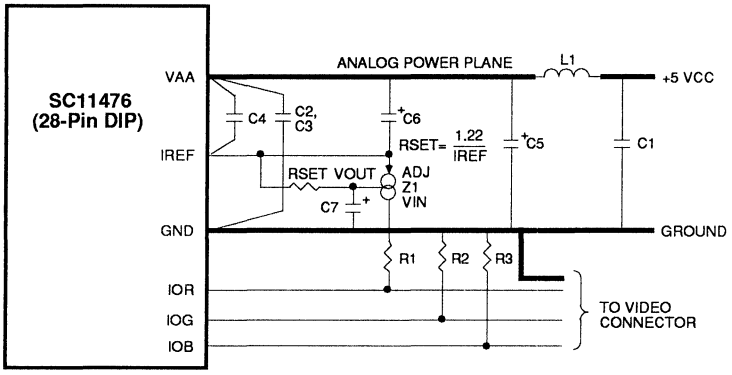
Figure 3. Typical Connection Diagram and Parts List (External Voltage Reference)



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Tantalum Capacitor	Mallory CSR13G106KM
C7	47 µF Tantalum Capacitor	Mallory CSR13F476KM
C8	1 µF Capacitor	Mallory CSR13G105KM
RSET	1% Metal Film Resistor	Dale CMF-55C
L1	Ferrite Bead	Fair-Rite 2743001111
Z1	Adjustable Regulator	National Semiconductor LM337LZ
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11471/476/478.

Figure 4. Typical Connection Diagram and Parts List (External Current Reference)



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C4	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C5	10 µF Tantalum Capacitor	Mallory CSR13G106KM
C6	47 µF Tantalum Capacitor	Mallory CSR13F476KM
C7	1 µF Capacitor	Mallory CSR13G105KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
Z1	Adjustable Regulator	National Semiconductor LM337LZ
RSET	1% Metal Film Resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11476.

Figure 5. Typical Connection Diagram and Parts List (External Current Reference)

ABSOLUTE MAXIMUM RATINGS

VAA (measured to GND)	+7.0 V
Voltage on Any Digital Pin	– 0.5 V to VAA + 0.5 V
Analog Output Short Circuit Duration to any Power Supply or Common (ISC)	Indefinite
Ambient Operating Temperature (TA)	–55 to +125°C
Storage Temperature (TS)	–65 to +150°C
Junction Temperature (TJ)	+150°C
Vapor Phase Soldering (2 minutes) TVSOL	TBD

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply (VAA)				
80, 66 MHz PRVTS	+4.75	5.0	5.25	V
50, 35 MHz PRVTS	+4.5	5.0	5.5	V
Ambient Operating Temperature (TA)	0	25	70	°C
Output Load (RL)		37.5		Ω
Voltage Reference (VREF)	+1.14	1.235	1.26	V
Current Reference (IREF)				
Standard RS-343A	–3	–8.39	–10	mA
PS/2 Compatible	–3	–8.88	–10	mA

DC ELECTRICAL CHARACTERISTICS

DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
Resolution (each DAC)					
SC11478		8	8	8	Bits
SC11471/476		6	6	6	Bits
Accuracy (each DAC)					
Integral Linearity Error	I_L				
SC11478				±1	LSB
SC11476				±1/2	LSB
SC11471				±1/4	LSB
Differential Linearity Error	D_L				
SC11478				±1	LSB
SC11476				±1/2	LSB
SC11471				±1/4	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	V_{IH}	2.0		V_{AA} + 0.5	V
Input Low Voltage	V_{IL}	GND–0.5		0.8	V
Input High Current (V_{IN} = 2.4 V)	I_{IH}			1	µA
Input Low Current (V_{IN} = 0.4 V)	I_{IL}			–1	µA
Input Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}			7	pF
Digital Outputs					
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4			V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}			0.4	V
3-State Current	I_{OZ}			50	µA
Output Capacitance	CD_{OUT}			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black*		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SC11471/478					
SETUP = VAA		0.95	1.44	1.90	mA
SETUP = GND		0	5	50	µA
SC11476		0	0	0	µA
Blank Level					
SC11471/478		6.29	7.62	8.96	mA
SC11476		0	5	50	µA
Sync Level (SC11471/478 only)		0	5	50	µA
LSB Size					
SC11478 (8/$\overline{6}$ = Logical One)			69.1		µA
SC11471/476			279.68		µA
DAC to DAC Matching			2	5	%
Output Compliance	V_{OC}	–1.0		+1.5	V
Output Impedence	RA_{OUT}		10		kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}			30	pF
Voltage Reference Input Current	IV_{REF}		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	% / %ΔVAA

ANALOG OUTPUT LEVELS—P/S 2 COMPATIBILITY

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SC11471/478					
SETUP = VAA		1.01	151	2.0	mA
SETUP = GND		0	5	50	µA
SC11476		0	5	50	µA
Blank Level					
SC11471/478		6.6	8	9.4	mA
SC11476		0	5	50	µA
Sync Level (SC11471/478 only)		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, V_{REF} = 1.235 V, SETUP = VAA, $8/\overline{6}$ = Logical one. For 28-pin DIP version of the SC11476, IREF = –8.88 mA.

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = VAA, $8/\overline{6}$ = Logical one. For 28-pin DIP version of the SC11476, IREF = –8.39 mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

* Since the SC11471/476 have 6-bit DACs (and the SC11478 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

AC ELECTRICAL CHARACTERISTICS

		80 MHZ DEVICES			66 MHZ DEVICES			
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Clock Rate	Fmax			80			66	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup	7	10			10			ns
Write Data Hold Time	8	10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	4•P13			4•P13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (P13)	13	12.5			15.5			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		13			13		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV–sec
DAC to DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

See test conditions on the next page.

		50 MHZ DEVICES			35 MHZ DEVICES			
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup	7	10			10			ns
Write Data Hold Time	8	10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	4•P13			4•P13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (P13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV–sec
DAC to DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

Test conditions: "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = VAA, $8/\overline{6}$ = Logical one. For 28-pin DIP version of SC11476, IREF = -8.39 mA. TTL input values are 0 to 3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 50 pF. See timing notes in Figures 6 and 7.

* Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k Ω resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

** At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

TIMING WAVEFORMS

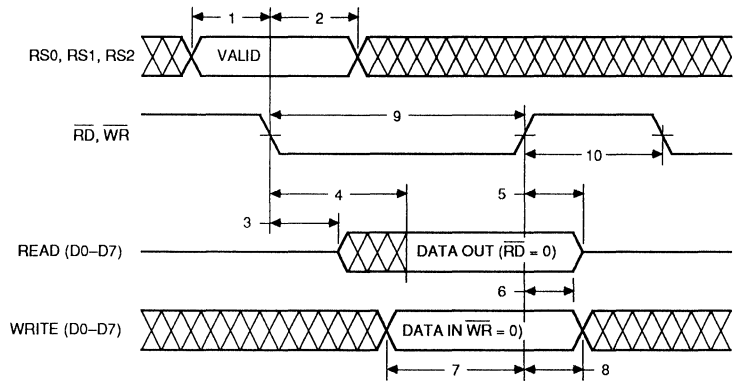
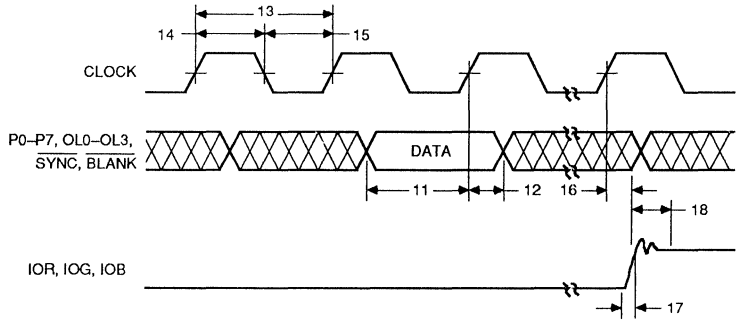


Figure 6. MPU Read/Write Timing



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB. (SC11478), ± 1/4 LSB (SC11471), or ± 1/2 LSB (SC11476).

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 7. Video Input/Output Timing

ORDERING INFORMATION

PART NO.	COLOR PALETTE RAM	OVERLAY PALETTE	SYNC. GENERATION	SPEED	PACKAGE	AMBIENT TEMP. RANGE
SC11471CV-80	256 x 18	15 x 18	yes	80 MHz	44-pin Plastic J-Lead	0° to +70°C.
SC11471CV-66	256 x 18	15 x 18	yes	66 MHz	44-pin Plastic J-Lead	0° to +70°C.
SC11471CV-50	256 x 18	15 x 18	yes	50 MHz	44-pin Plastic J-Lead	0° to +70°C.
SC11471CV-35	256 x 18	15 x 18	yes	35 MHz	44-pin Plastic J-Lead	0° to +70°C.
SC11476CV-66	256 x 18	–	no	66 MHz	44-pin Plastic J-Lead	0° to +70°C.
SC11476CV-50	256 x 18	–	no	50 MHz	44-pin Plastic J-Lead	0° to +70°C.
SC11476CV-35	256 x 18	–	no	35 MHz	44-pin Plastic J-Lead	0° to +70°C.
SC11476CN-66	256 x 18	–	no	66 MHz	28-pin 0.6" Plastic DIP	0° to +70°C.
SC11476CN-50	256 x 18	–	no	50 MHz	28-pin 0.6" Plastic DIP	0° to +70°C.
SC11476CN-35	256 x 18	–	no	35 MHz	28-pin 0.6" Plastic DIP	0° to +70°C.
SC11478CV-80	256 x 24	15 x 24	yes	80 MHz	44-pin Plastic J-Lead	0° to +70°C.
SC11478CV-66	256 x 24	15 x 24	yes	66 MHz	44-pin Plastic J-Lead	0° to +70°C.
SC11478CV-50	256 x 24	15 x 24	yes	50 MHz	44-pin Plastic J-Lead	0° to +70°C.
SC11478CV-35	256 x 24	15 x 24	yes	35 MHz	44-pin Plastic J-Lead	0° to +70°C.

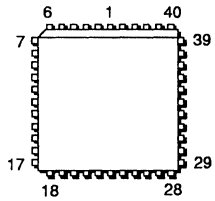
SC11481/SC11486/SC11488
32K HiColor™/80 MHz 256 Palette For Personal System/2™

SIERRA SEMICONDUCTOR

FEATURES

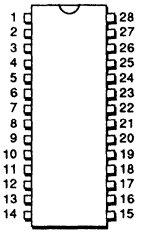
- ☐ 32K HiColor™ Mode (Hardware/Software Selectable)
- ☐ 80 MHz Pipelined Operation–Psuedo-color mode
- ☐ 40 MHz Pipelined Operation–HiColor™ Mode
- ☐ Triple 6-bit or 8-bit D/A Converters
- ☐ Supports 15-bit HiColor RGB inputs and 8-bit Pseudo-Color
- ☐ Analog Output Comparators
- ☐ On-chip Voltage Reference
- ☐ Anti-Sparkle Circuitry
- ☐ 15 Overlay Registers (SC11481/SC11488)
- ☐ 256 Word Color Palette RAM
- ☐ RS-343A/RS-170 Compatible Outputs
- ☐ Sync on all Three Channels (SC11481/SC11488)
- ☐ Programmable Pedestal (SC11481/SC11488)
- ☐ Standard MPU Interface
- ☐ +5V CMOS Monolithic (EPI) Construction
- ☐ Available Clock Rates FOR Pseudo-Color
  - • 80 MHz • 50 MHz
  - • 66 MHz • 35 MHz

44-PIN PLCC PACKAGE



SC11481CV
SC11486CV
SC11488CV

28-PIN DIP PACKAGE



SC11486CN

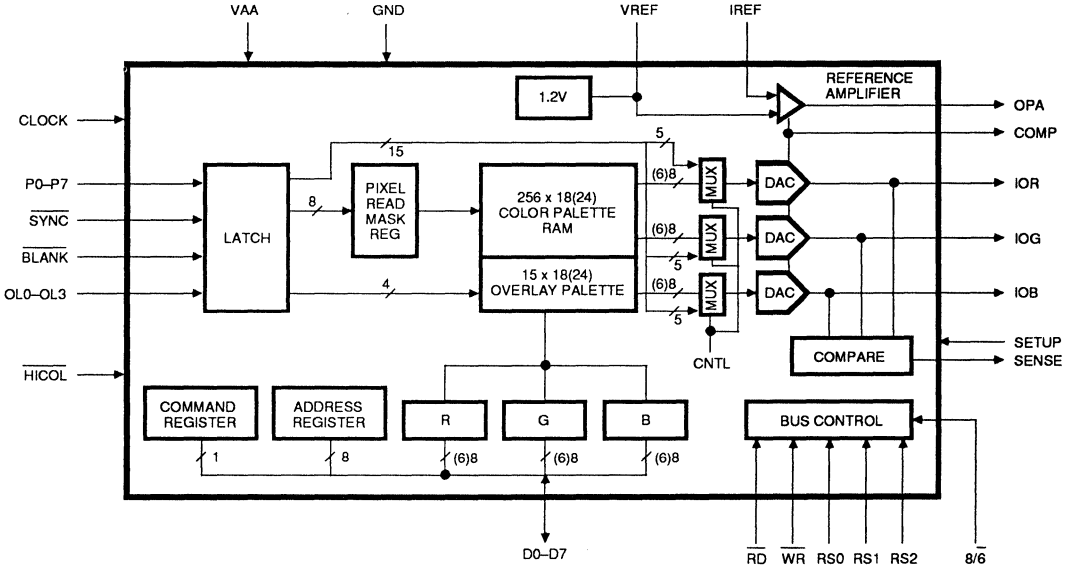
GENERAL DESCRIPTION

The SC11481, SC11486 and SC11488 are pin-compatible and software-compatible with the SC11471, SC11476 and SC11478 Color Palettes designed specifically for Personal System/2™ compatible color graphics. The SC11486 is also available in a 28-pin DIP package that is pin compatible with the IMSG171/IMSG176.

The SC11481/SC11486/SC11488 supports 15-bit HiColor™ and 8-bit pseudo-color. The HiColor™ mode provides the ability to display 32K colors simultaneously. It is specifically tailored to work with the Tseng Labs ET4000 VGA controller chip in the high-color mode.

The SC11481 has a 256 x 18 color lookup table with triple 6-bit video D/A converters. The SC11488 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. It

BLOCK DIAGRAM



Personal System/2 is a trademark of IBM.

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may be configured for either 6 bits or 8 bits per color operation.

The SC11481 and SC11488 also include 15 overlay registers to provide for overlaying cursors, grids, menus, EGA emulation, etc. Sync generation on all three channels, a programmable pedestal (0 or 7.5IRE), and use of either an external voltage or current reference is also supported.

The SC11486 is similar to the SC11481, but has no overlays or sync information on the analog outputs.

On-chip analog comparators are included to simplify diagnostics and debugging, with the resulting output onto the SENSE pin. Also included is an on-chip voltage reference to simplify using the device.

When the HiColor™ mode is not activated, SC11481/486/488 behave exactly as SC11471/476/478 with anti-sparkle capabilities, on chip voltage/current reference, and analog comparators.

The SC11481/486/488 generate RS-343A compatible red, green, and blue video signals, and are capable of driving doubly-terminated 75 Ω coax directly, and generate RS-170 compatible video signals into a singly-terminated 75 Ohm load, without requiring external buffering.

FUNCTIONAL DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the SC11481/486/488 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, command registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers.

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address register (RAM write mode)
0	1	1	Address register (RAM read mode)
0	0	1	Color palette RAM
0	1	0	Pixel read mask register
1	0	0	Address register (overlay write mode)
1	1	1	Address register (overlay read mode)
1	0	1	Overlay registers
1	1	0	Command Register

Table 1. Control Input Truth Table

Writing Color Palette RAM and Overlay Color Data

To write color data, the MPU writes the address register (selecting RAM write or overlay write mode) with the address of either the color palette RAM location or the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select either the color palette RAM or the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the SC11481/486) and written to the location specified by the address register. The address register then increments to the next location which MPU may modify by simply writing another sequence of red, green and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Color Palette RAM and Overlay Color Data

To read color data, the MPU loads the address register (selecting RAM or overlay read mode) with the address of the color palette RAM location or overlay register to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select either the color palette RAM or overlay registers. Following the blue read cycle, the contents of the color palette RAM or the contents of the overlay location specified by the address register are copied into the R, G, B registers and the address register gets incremented again. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the four most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses.

To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMS or the overlay registers, an internal anti-sparkle logic is implemented to maintain the previous output color data on the three D/A Converters output while the transfer between the color look-up table RAMS and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

SC11481/486 Data Bus Interface

Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

SC11488 Data Bus Interface

On the SC11488, the $8/\overline{6}$ control input is used to specify whether the MPU is reading and writing 8-bits ($8/\overline{6}$ = logical one) or 6-bits ($8/\overline{6}$ = logical zero) of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation (and also when using the SC11481/486), color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero. Note that in the 6-bit mode, the SC11488's full scale output current will be about 1.5% lower than when it is in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being logic zero in the 6-bit mode.

Color Modes

Two color modes are supported by the SC11481/486/488: 8-bit psuedo-color and 16-bit high-color. The mode of operation is determined either by the command register or by the $\overline{\text{HICOL}}$ pin.

HiColor™ Mode

When the HiColor™ mode is activated, the input stage accepts 16-bits of pixel information from the pixel select lines P0-P7, by latching the lower 8 bits on the rising edge, and the upper 8 bits on the falling edge of the pixel clock. The two bytes form a 16 bit word which is used as a direct input to the triple video DACs. The color palette RAM and pixel read mask register are bypassed.

HiColor™ Mode Data Format

The data captured on the rising edge of the pixel clock constitute the LSB (B7-B0) and the data captured on the falling edge of the pixel clock constitute the MSB (B15-B8) bytes of the color data. The 16 bit word (B15-B0) is assigned to the color DACs in the following format:

B14 - B10	Red DAC
B7 - B5	Green DAC
B4 - B0	Blue DAC
B15	Ignored

The three LSBs of all three DACs are forced to zero.

SENSE Output

SENSE is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This output is used to determine the presence of a CRT monitor and via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 335 mV reference has a ±5% tolerance (when using an external 1.235 V voltage reference). The tolerance is ±10% when using the internal voltage reference or an external current reference. Note that SYNC should be logical zero for SENSE to be stable.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the SC11481/486) of color information to the three D/A converters.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 1 and 2. Tables 4 and 5 detail how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs modify the output levels.

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal is to be used. Note that the SC11476 generates only a 0 IRE blanking pedestal (Figure 2).

The analog outputs of the SC11481/486/488 are capable of directly driving a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

Command Register

This register is active in all modes. It may be written to or read by the MPU at any time and is initialized to a logical zero after the power on reset.

D7	HiColor™ mode	A logical one will activate the HiColor™ mode. A logical zero will set it in the psuedo-color mode.
D6-D0	Not used	

In the SC11486, where the RS2 pin is not available, the command register is accessed by using the following special sequence of events:

A flag will be set when the pixel read mask register (RS1 = 1 & RS0 = 0) is read four times consecutively. The next write to the pixel mask register will be directed to the command register and can be used to set the D7 bit of the command register. A write to any address or a read from any address other than the pixel read mask register will reset the flag. This flag will also get reset after the power on reset.

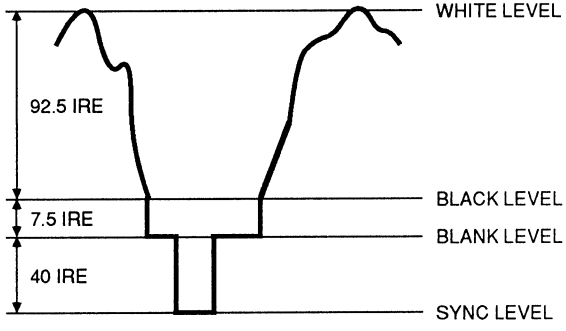
	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				Red value Green value Blue value
ADDR0–7 (counts binary)	$00-$FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	Color palette RAM Reserved Overlay Color 1 : Overlay Color 15

Table 2. Address Register (ADDR) Operation

OL0–OL3	P0–P7	Addressed by Frame Buffer
$0	$00	Color Palette RAM Location $00
$0	$01	Color Palette RAM Location $01
:	:	:
$0	$FF	Color Palette RAM Location $FF
$1	$xx	Overlay Color 1
:	$xx	:
$F	$xx	Overlay Color 15

Table 3. Pixel and Overlay Control Truth Table. (Pixel Read Mask Register = $FF)

SC11481/488 w/o SYNC		SC11481/488 with SYNC	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, SETUP = VAA, VREF = 1.235 V, RSET = 147 Ω.
RS-343A levels and tolerances assumed on all levels.

793 03

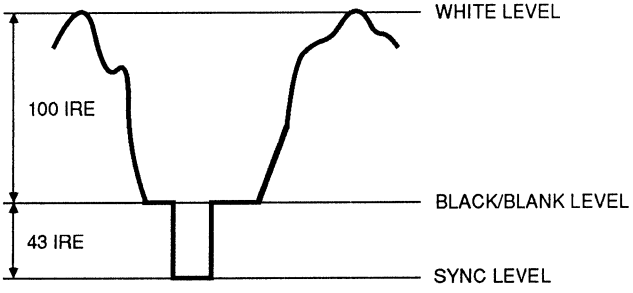
Figure 1. Composite Video Output Waveforms (SETUP = VAA)

Description	SC11481/488 IOUT (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	Data + 9.05	1	1	Data
DATA–SYNC	Data + 1.44	0	1	Data
BLACK	9.05	1	1	$00
BLACK–SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75 doubly-terminated load, SETUP = VAA, VREF = 1.235 V, RSET = 147 .

Table 4. Video Output Truth Table (SETUP = VAA)

SC11486 or SC11481/488 w/o Sync		SC11481/488 with Sync	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.256
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load, SETUP = GND. VREF = 1.235 V, RSET = 147 Ω.
RS-343A levels and tolerances assumed on all levels.

793 04

Figure 2. Composite Video Output Waveforms (SETUP = GND)

Description	SC11486 IOUT (mA)	SC11481/488 IOUT (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	17.62	26.67	1	1	$FF
DATA	Data	Data + 8.05	1	1	Data
DATA–SYNC	Data	Data	0	1	Data
BLACK	0	8.05	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	0	8.05	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load, SETUP = VAA, VREF = 1.235 V, RSET = 147 Ω.

Table 5. Video Output Truth Table (SETUP = GND)

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
$\overline{BLANK}$	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 4 and 5. It is latched on the rising edge of CLOCK. When $\overline{BLANK}$ is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal.
$\overline{SYNC}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1 and 2). $\overline{SYNC}$ does not override any other control or data input, as shown in Tables 4 and 5; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not to be generated on the analog outputs, this pin should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, $\overline{SYNC}$, and $\overline{BLANK}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75 Ω coaxial cable.
SENSE	Sense output (TTL compatible). SENSE is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). Note that SENSE may not be stable while SYNC is toggling.
$\overline{HICOL}$	HiColor Mode select input (TTL compatible). A logic zero will enable the HiColor mode. The $\overline{HICOL}$ pin should be tied to VAA to disable hardware selection of the HiColor mode.

<table>
<tr><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>IREF</td><td>Full scale adjust control. Note that the IRE relationships in Figures 1 and 2 are maintained, regardless of the full scale output current.

When using an external voltage reference (Figure 3), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is:

RSET (Ω) = K • 1000 • VREF (V)/Iout (mA)

K is defined in the table below for doubly-terminated 75 Ω loads.

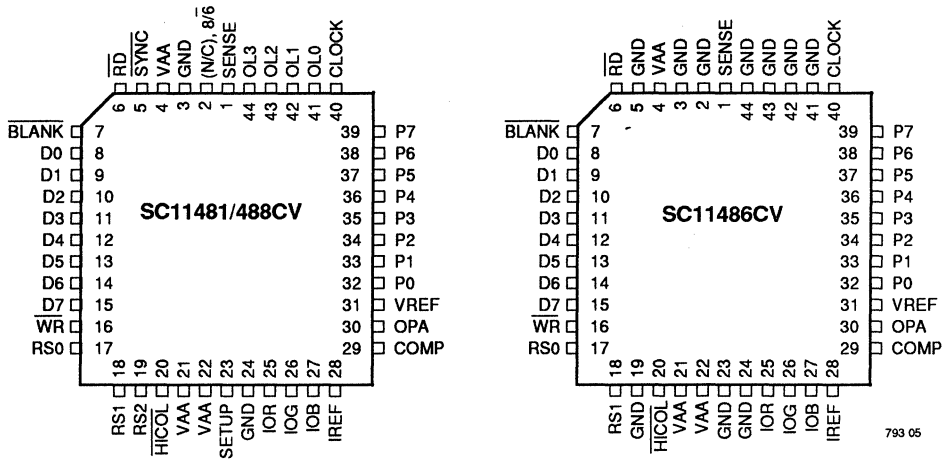
When using an external current reference (Figures 4 and 5) the relationship between IREF and the full scale output current on each output is:

IREF (mA) = Iout (mA)/K

<table>
<tr><th>Part Number</th><th>Mode</th><th>Pedestal</th><th>K</th></tr>
<tr><td>SC11488</td><td>6-bit
8-bit
6-bit
8-bit</td><td>7.5 IRE
7.5 IRE
0.0 IRE
0.0 IRE</td><td>3.170
3.195
3.000
3.025</td></tr>
<tr><td>SC11481</td><td>6-bit</td><td>7.5 IRE
0.0 IRE</td><td>3.170
3.000</td></tr>
<tr><td>SC11486</td><td>6-bit</td><td>0.0 IRE</td><td>2.100</td></tr>
</table>
</td></tr>
<tr><td>COMP</td><td>Compensation pin. If an external voltage reference is used (Figure 3), this pin should be connected to OPA. If an external current reference is used (Figure 4), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum.</td></tr>
<tr><td>VREF</td><td>Voltage reference input. If an external voltage reference is used (Figure 3), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 4), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figures 3 and 4. The decoupling capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum.

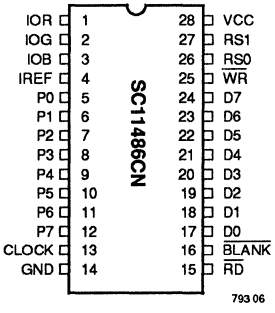
When using internal reference this pin should not drive any external circuitry except for the decoupling capacitor.</td></tr>
<tr><td>OPA</td><td>Reference amplifier output. If an external voltage reference is used (Figure 3), this pin must be connected to COMP. When using an external current reference (Figure 4), this pin should be left floating.</td></tr>
<tr><td>VAA</td><td>Analog power. All VAA pins must be connected.</td></tr>
<tr><td>GND</td><td>Analog ground. All GND pins must be connected.</td></tr>
<tr><td>$\overline{WR}$</td><td>Write control input (TTL compatible). D0–D7 data is latched on the rising edge of $\overline{WR}$, and RS0–RS2 are latched on the falling edge of $\overline{WR}$ during MPU write operations.</td></tr>
<tr><td>$\overline{RD}$</td><td>Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS0–RS2 are latched on the falling edge of $\overline{RD}$ during MPU read operations.</td></tr>
<tr><td>RS0, RS1, RS2</td><td>Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation RS2 being performed, as illustrated in Tables 1 and 2.</td></tr>
<tr><td>D0–D7</td><td>Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.</td></tr>
<tr><td>8/$\overline{6}$</td><td>8-bit/$\overline{6}$-bit select input (TTL compatible). This bit specifies whether the MPU is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant bit during color read/write cycles (D6 and D7 are ignored during color write cycles and logical zero during color read cycles). This bit is implemented only on the SC11488.</td></tr>
</table>

CONNECTION DIAGRAM



44-Pin PLCC

N/C pins may be left unconnected without affecting the performance of the SC11481/486/488. Names in parentheses are pin names for SC11481.



28-Pin DIP

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

The layout should be optimized for lowest noise on the SC11481/486/488 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all SC11481/486/488 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the SC11481/486/488, the analog output traces, and all the digital signal traces leading up to the SC11471/476/478.

Power Planes

The SC11481/486/488 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figures 3, 4 and 5. This bead should be located within three inches of the SC11481/486/488.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all SC11481/486/488 power pins and current/voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that

portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the SC11481/486/488 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the SC11481/486/488 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the SC11481/486/488 should be avoided to reduce noise pickup.

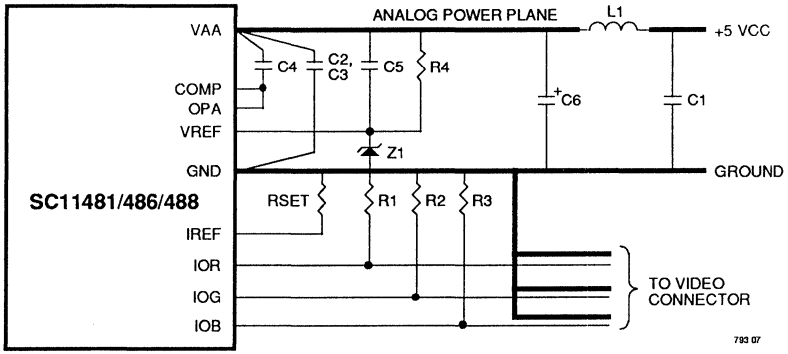
Any active termination resistors for the digital inputs should be connected to the regular PCB power plane, and not the analog power plane.

Analog Signal Interconnect

The SC11481/486/488 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

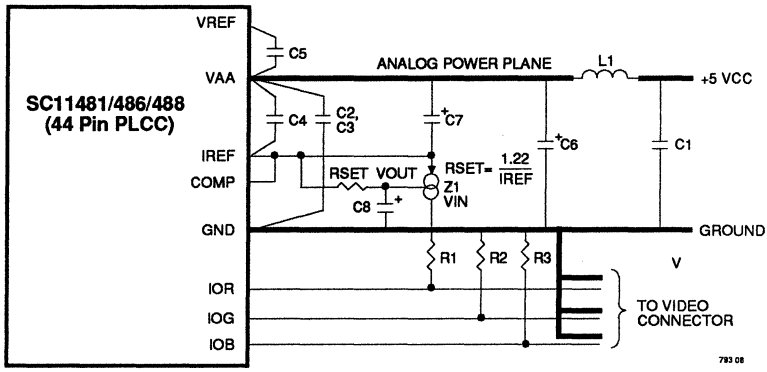
For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the SC11481/486/488 to minimize reflections.



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Tantalum Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
RSET	1% Metal Film Resistor	Dale CMF-55C
Z1	1.2 V Voltage Reference	National Semiconductor LM385BZ-1.2
R4	1K Ω 5% Resistor	

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11481/486/488.

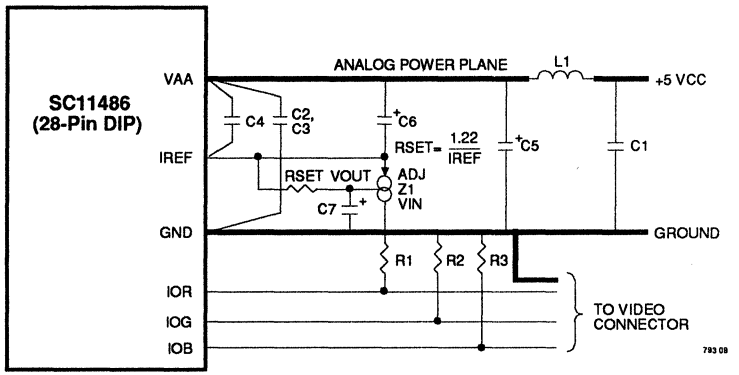
Figure 3. Typical Connection Diagram and Parts List (External Voltage Reference)



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Tantalum Capacitor	Mallory CSR13G106KM
C7	47 µF Tantalum Capacitor	Mallory CSR13F476KM
C8	1 µF Capacitor	Mallory CSR13G105KM
RSET	1% Metal Film Resistor	Dale CMF-55C
L1	Ferrite Bead	Fair-Rite 2743001111
Z1	Adjustable Regulator	National Semiconductor LM337LZ
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11481/486/488.

Figure 4. Typical Connection Diagram and Parts List (External Current Reference)



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C4	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C5	10 µF Tantalum Capacitor	Mallory CSR13G106KM
C6	47 µF Tantalum Capacitor	Mallory CSR13F476KM
C7	1 µF Capacitor	Mallory CSR13G105KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
Z1	Adjustable Regulator	National Semiconductor LM337LZ
RSET	1% Metal Film Resistor	Dale CMF-55C

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11876.

Figure 5. Typical Connection Diagram and Parts List (External Current Reference)

ABSOLUTE MAXIMUM RATINGS	
VAA (measured to GND)	+7.0 V
Voltage on Any Digital Pin	– 0.5 V to VAA + 0.5 V
Analog Output Short Circuit Duration to any Power Supply or Common (ISC)	Indefinite
Ambient Operating Temperature (TA)	–55 to +125°C
Storage Temperature (TS)	–65 to +150°C
Junction Temperature (TJ)	+150°C
Vapor Phase Soldering (2 minutes) TVSOL	TBD

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply (VAA)				
80, 66 MHz PRVTS	+4.75	5.0	5.25	V
50, 35 MHz PRVTS	+4.5	5.0	5.5	V
Ambient Operating Temperature (TA)	0	25	70	°C
Output Load (RL)		37.5		Ω
Voltage Reference (VREF)	+1.14	1.235	1.26	V
Current Reference (IREF)				
Standard RS-343A	–3	–8.39	–10	mA
PS/2 Compatible	–3	–8.88	–10	mA

DC ELECTRICAL CHARACTERISTICS

DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
Resolution (each DAC)					
SC11488		8	8	8	Bits
SC11481/486		6	6	6	Bits
Accuracy (each DAC)					
Integral Linearity Error	I_L				
SC11488				±1	LSB
SC11486				±1/2	LSB
SC11481				±1/4	LSB
Differential Linearity Error	D_L				
SC11488				±1	LSB
SC11486				±1/2	LSB
SC11481				±1/4	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	V_{IH}	2.0		V_{AA} + 0.5	V
Input Low Voltage	V_{IL}	GND–0.5		0.8	V
Input High Current (V_{IN} = 2.4 V)	I_{IH}			1	µA
Input Low Current (V_{IN} = 0.4 V)	I_{IL}			–1	µA
Input Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}			7	pF
Digital Outputs					
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4			V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}			0.4	V
3-State Current	I_{OZ}			50	µA
Output Capacitance	CD_{OUT}			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black*		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SC11481/488					
SETUP = VAA		0.95	1.44	1.90	mA
SETUP = GND		0	5	50	µA
SC11486		0	0	0	µA
Blank Level					
SC11481/488		6.29	7.62	8.96	mA
SC11486		0	5	50	µA
Sync Level (SC11481/488 only)		0	5	50	µA
LSB Size					
SC11488 (8/$\overline{6}$ = Logical One)			69.1		µA
SC11481/486			279.68		µA
DAC to DAC Matching			2	5	%
Output Compliance	V_{OC}	–1.0		+1.5	V
Output Impedence	RA_{OUT}		10		kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}			30	pF
Voltage Reference Input Current	IV_{REF}		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	% / %ΔVAA

ANALOG OUTPUT LEVELS—P/S 2 COMPATIBILITY

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SC11481/488					
SETUP = VAA		1.01	1.51	2.0	mA
SETUP = GND		0	5	50	µA
SC11486		0	5	50	µA
Blank Level					
SC11481/488		6.6	8	9.4	mA
SC11486		0	5	50	µA
Sync Level (SC11481/488 only)		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, V_{REF} = 1.235 V, SETUP = VAA, $8/\overline{6}$ = Logical one. For 28-pin DIP version of the SC11486, IREF = –8.88 mA.

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = VAA, $8/\overline{6}$ = Logical one. For 28-pin DIP version of the SC11486, IREF = –8.39 mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

* Since the SC11481/486 have 6-bit DACs (and the SC11478 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

AC ELECTRICAL CHARACTERISTICS

		80 MHZ DEVICES			66 MHZ DEVICES			
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Clock Rate (Pseudo Color)	Fmax			80			66	MHz
Clock Rate (HiColor™ Mode)	Fmax(HC)			40			40	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup	7	10			10			ns
Write Data Hold Time	8	10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	4•P13			4•P13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Pixel and Control Setup Time LSB (HiColor™ Mode)	20	-1.0			-1.0			ns
Pixel and Control Hold Time LSB (HiColor™ Mode)	21	7.0			7.0			ns
Pixel and Control Setup Time MSB (HiColor™ Mode)	22	-1.0			-1.0			ns
Pixel and Control Hold Time MSB (HiColor™ Mode)	23	7.0			7.0			ns
Clock Cycle Time (P13)	13	12.5			15.5			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Clock Cycle Time (HiColor™ Mode)	13	25			25			ns
Clock Pulse Width High Time (HiColor™ Mode)	14	9			9			ns
Clock Pulse Width Low Time (HiColor™ Mode)	15	9			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		13			15		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV–sec
DAC to DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE Output Delay	19		1			1		µs
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

See test conditions on page 706.

PARAMETER	SYMBOL	50 MHZ DEVICES MIN	50 MHZ DEVICES TYP	50 MHZ DEVICES MAX	35 MHZ DEVICES MIN	35 MHZ DEVICES TYP	35 MHZ DEVICES MAX	UNITS
Clock Rate (Pseudo Color)	Fmax			50			35	MHz
Clock Rate (HiColor™ Mode)	Fmax(HC)			35			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup	7	10			10			ns
Write Data Hold Time	8	10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	4•P13			4•P13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Pixel and Control Setup Time LSB (HiColor™ Mode)	20	-1.0			-1.0			ns
Pixel and Control Hold Time LSB (HiColor™ Mode)	21	7.0			7.0			ns
Pixel and Control Setup Time MSB (HiColor™ Mode)	22	-1.0			-1.0			ns
Pixel and Control Hold Time MSB (HiColor™ Mode)	23	7.0			7.0			ns
Clock Cycle Time (P13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Clock Cycle Time (HiColor™ Mode)	13	28			28			ns
Clock Pulse Width High Time (HiColor™ Mode)	14	9			9			ns
Clock Pulse Width Low Time (HiColor™ Mode)	15	9			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV–sec
DAC to DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE Output Delay	19		1			1		µs
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

See test conditions on the next page.

Test conditions: "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = VAA, $8/\overline{6}$ = Logical one. For 28-pin DIP version of SC11486, IREF = -8.39 mA. TTL input values are 0 to 3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 50 pF. See timing notes in Figures 6 and 7.

* Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k Ω resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

** At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

TIMING WAVEFORMS

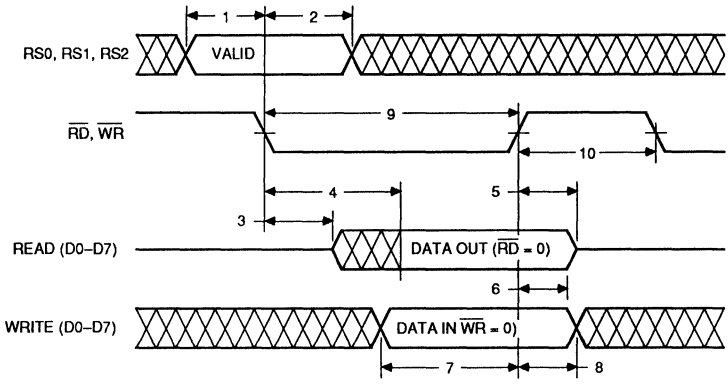
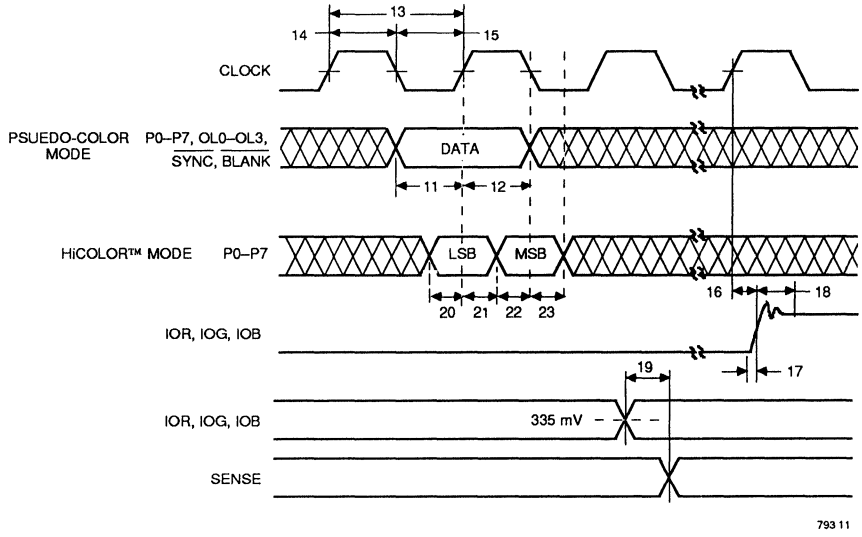


Figure 6. MPU Read/Write Timing



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB. (SC11488), ± 1/4 LSB (SC11481), or ± 1/2 LSB (SC11486).

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 7. Video Input/Output Timing

ORDERING INFORMATION

PART NO.	COLOR PALETTE RAM	OVERLAY PALETTE	SYNC. GENERATION	SPEED PSEUDO	SPEED HiCOLOR	PACKAGE	AMBIENT TEMP. RANGE
SC11481CV-80	256 x 18	15 x 18	yes	80 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11481CV-66	256 x 18	15 x 18	yes	66 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11481CV-50	256 x 18	15 x 18	yes	50 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11481CV-35	256 x 18	15 x 18	yes	35 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11486CV-66	256 x 18	–	no	66 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11486CV-50	256 x 18	–	no	50 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11486CV-35	256 x 18	–	no	35 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11486CN-66	256 x 18	–	no	66 MHz	40 Mhz	28-pin 0.6" Plastic DIP	0° to +70°C.
SC11486CN-50	256 x 18	–	no	50 MHz	40 Mhz	28-pin 0.6" Plastic DIP	0° to +70°C.
SC11486CN-35	256 x 18	–	no	35 MHz	40 Mhz	28-pin 0.6" Plastic DIP	0° to +70°C.
SC11488CV-80	256 x 24	15 x 24	yes	80 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11488CV-66	256 x 24	15 x 24	yes	66 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11488CV-50	256 x 24	15 x 24	yes	50 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.
SC11488CV-35	256 x 24	15 x 24	yes	35 MHz	40 Mhz	44-pin Plastic J-Lead	0° to +70°C.

Semicustom Capabilities

4

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Analog, Digital and EEPROM combined on the same chip.

Sierra is a leading supplier of mixed-signal standard cell ASICs. The Company's unique Triple Technology™ process permits the integration of analog, digital and EEPROM functions on a single chip. This, combined with the industry's most comprehensive cell library and the Company's MONTAGE™ System Integration software enables customers to quickly and efficiently design highly complex mixed-signal ASICs in their own environment. Sierra guarantees ASICs designed with MONTAGE will perform as simulated—virtually assuring first time silicon success.

Industry's Most Comprehensive Cell Library

The mainstay of Sierra's ASIC technology is its large library of standard cells. The table at the end of this section lists the Company's complete 1.5 micron digital, analog and EEPROM cell library.

Sierra's exceptionally rich analog library features, a 65 MHz phase-locked loop, A/D converters up to 12 bits, D/A converters up to 8 bits, a wide range of operational amplifiers and high-speed comparators, crystal oscillators, differential driver/receivers, and circuits for power-on reset and low-voltage detection.

About 250 cells comprise the digital portion of Sierra's library. Included are buffers gates, flip-flops and latches, adders, subtractors, and output drivers up to 48 mA. Compilers are available for PLA, datapath, multiplier, and 2901 Bit Slice cells.

Also available are a microcontroller and peripherals. The COP880® is the smallest 8-bit microcontroller in the industry; it is based on National Semiconductor's popular device. The peripheral functions that work with the microcontroller include a 32-segment triplex LCD controller, a universal asynchronous receiver/transmitter (8250 subset), a real-time clock, a watchdog timer, an external ROM interface, and 8-bit ports.

Sierra offers several types of memory cells, including a variety of EEPROM cells. The latter range from bits and bytes to arrays as large as 8K bits. On-chip high-voltage programming generators are also available. Compilers are provided for creating RAM and ROM.

Custom Cells Provided Routinely

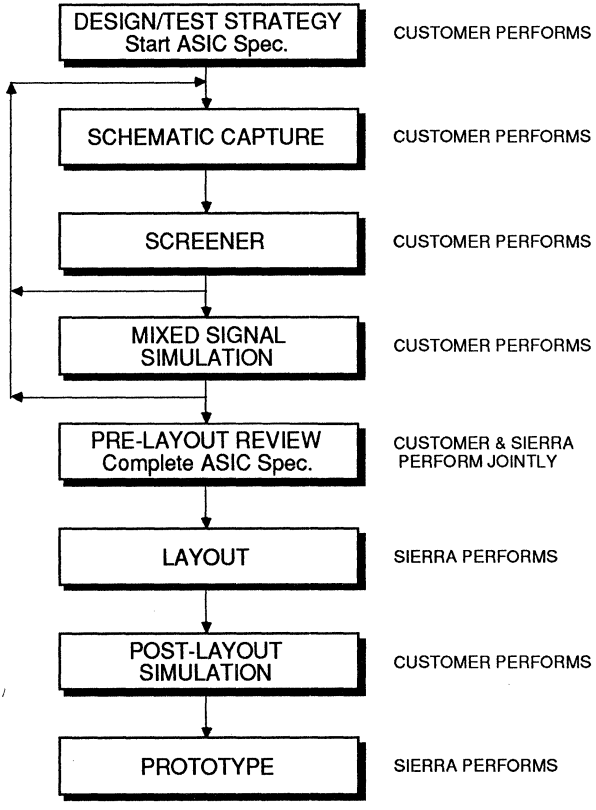
If a design requires a custom function, Sierra routinely creates analog, digital and EEPROM cells to meet special requirements—usually without any appreciable delay in producing the final product.

Sierra Customers Can Design and Simulate Complete Mixed-Signal ASIC Designs in Their Own Environment

ASICs based on Sierra's Triple-Technology process can be designed by either the customer, Sierra, or jointly. Sierra provides any level of design support required. Most of the recent ASICs produced resulted from a joint design effort on the part of Sierra and its customers. However, MONTAGE now allows customers to design and simulate their own ASICs in their own environment.

Many Triple-Technology ASICs are single-chip implementations of systems that already exist in the form of a PC board. In these cases the first step in designing the chip is to map the board's circuitry onto the functions in Sierra's standard cell library. A critical consideration in doing this is to find out whether any cells must be altered to perform the required functions. Although digital cells tend to be fairly standard across discrete and semicustom devices, analog functions often need specific characteristics. When cells that require customization are discovered early in the design process, Sierra can modify those cells while the rest of the design effort goes forward.

MONTAGE Design Flow



Minimum Pin Count Ensures Low Cost

When the circuit has been designed, pinouts are defined. This is an important step because Sierra can multiplex test pins with functional pins. The test pins access the chip's internal functions only when the chip is in test mode; otherwise these pins function as normal I/O pins. This approach avoids any need to add extra pins just for test purposes, which would increase the chip's cost. To ensure that the test mode cannot interfere with the chip's operation, Sierra works with the customer to determine the pins that should be multiplexed and the algorithm that should be used to put the chip in test mode.

The next step—checking out the design—can be done in two different ways. Historically designers have used a list of standard cell equivalent functions so that they can breadboard the chip to be designed. This is a time consuming process. The second way to check out the design—the easiest and safest—is to simulate it using the mixed-mode simulator in Sierra's MONTAGE design system. Sierra guarantees first time performance in silicon.

After both the customer and Sierra are satisfied with the design, Sierra performs automatic placement and routing of the chip. The chip is then resimulated using capacitances extracted from the layout; the results are compared with those of the pre-layout simulation. When the design has passed this test to the customer's satisfaction, the chip is released for mask-making and prototype fabrication.

TESTING
Mixed Signal ASICs Require Mixed Signal Testers

The prototypes, usually mounted in ceramic packages for fast assembly turnaround, are fully tested by Sierra on an ATE system capable of testing analog/digital mixed circuits. Sierra testers include Teradyne A500, Sentry Series 80, Axion, Semiconductor Test Solution, and Megatest machines. To save time, automated tools help create the test programs. And because Sierra provides test vectors for the standard-cell microcontroller and peripherals, you only have to write test vectors for any customized logic you create.

PACKAGES
A Variety of Choices

After testing the prototypes and allowing the customer to prove them out, Sierra fabricates and tests the final chips at either our Singapore manufacturing facilities or one of our many independent foundries. A wide variety of packages are available, including surface-mount types such as small-outline, leaded chip carriers and gull-wing packages, in addition to DIPs and pin-grid-array packages. Sierra can also accommodate requirements for custom packaging.

Industry-Leading MONTAGE System Integration Software

Conceived for use by systems designers, Sierra's MONTAGE system provides the means to create state-of-the-art mixed-signal ASICs. Because MONTAGE operates with Sierra's standard cell library, knowledge of the intricacies of transistor-level design is not required. MONTAGE allows simulation and evaluation of what-if design tradeoffs quickly, even on highly complex ASICs. Once satisfied the design works on the MONTAGE simulator, Sierra guarantees that the finished ASICs will perform as expected—on the first pass.

MONTAGE includes everything needed to design mixed-signal ASICs, with plenty of expansion capability for future enhancements. Both the schematic capture facility and the simulator that form the heart of MONTAGE are based on tools from Mentor Graphics. The tools are thus compatible with ASIC libraries from other vendors and can be expanded to include other Mentor Graphics software, such as logic synthesizers, compiler libraries, automatic test-program generators, and layout tools. In addition to the Mentor Graphics tools and Sierra's Triple-Technology cell libraries, MONTAGE include the Sierra-designed Screener facility, which performs specialized error checking and generates several useful reports on your design's characteristics.

High Speed Mixed-Signal Simulation Makes Designer's Speed Pacing Item—not the Simulator

The most important aspect of MONTAGE is its simulator. The first commercially available tool that allows systems designers to effectively simulate complex mixed-signal ASICs, the MONTAGE simulator performs at very high speed. With MONTAGE, new mixed-signal designs are paced by the system designer, not the simulator.

The MONTAGE simulator employs several strategies that allow it to simulate complex analog/digital ASICs in nearly the same time required for comparable digital-only circuits. The first strategy is to use behavioral models for simulating both the analog and digital cells; this avoids the transistor-level calculations that make analog simulators such as SPICE so slow. In addition to allowing faster simulations, MONTAGE's behavioral models furnish the details necessary to verify your circuit's operation fully.

The MONTAGE simulator also uses an event-driven algorithm, which avoids needless calculations. If a comparator is far from its trip point, for example, there is no need to calculate the effect of a small input-voltage change. The simulator works with the behavioral models to ensure that accuracy is maintained without wasting time.

Another strategy that saves time is the use of multiple levels of models that progressively test more and more of the design's functions. MONTAGE includes three levels of models. In the first level, MONTAGE checks basic items such as connectivity and operating ranges. The simplicity of the simulation at this level makes it easy to find errors that would take a great deal of time to unravel at higher levels of simulation. The remaining two simulation levels check functional issues such as capacitive loading and some worst-case analog evaluations, respectively.

The very structure of the MONTAGE simulator helps simulations run quickly. Unlike most analog/digital simulators, which tie together separate analog and digital simulators, MONTAGE has only one simulator for handling both analog and digital models. This approach eliminates the need for separate analog and digital netlists, avoids the problems of synchronizing separate simulators, and eliminates the need for artificial interface elements between analog and digital models.

MONTAGE runs on the Unix® operating system on Sun workstations.

MANUFACTURING
The Right Facility for the Right Product

Sierra Semiconductor's manufacturing needs are served by a facility in Singapore and independent foundries.

The company's Singapore facility has the capacity to produce 6,000, 6-inch, submicron-geometry wafers per month. A Class 10 clean room ensures pristine conditions. It is dedicated to the production of high-volume, low-cost, state-of-the-art products.

As an alternative for high-volume, low-cost production of mature, yield-stabilized products, Sierra utilizes independent foundries. Sierra has taken great care to make sure its customers have a dependable source of ASICs throughout the life span of ASIC-based products.

1.5μ ANALOG CELL LIBRARY

- All cells have power down mode where appropriate.
- All analog specifications are typical, 5 V, 25°C, and use a single 5 V supply, unless otherwise indicated.

ANALOG-TO-DIGITAL CONVERTERS

CELL NAME	DESCRIPTION	CONVERSION TIME	POWER	NON-LINEARITY INTEGRAL	NON-LINEARITY DIFFERENTIAL	SIZE SQ. MILS
ADC4BT	4-Bit Flash					TBA
ADC10B	10-Bit Successive Approximation	5 μsec	8 mW	0.5 LSB	0.5 LSB	
ADC12B	12-Bit Dual Slope	133 msec	7.5 mW	1 LSB	1 LSB	
HADC8B	8-Bit High Speed					TBA

DIGITAL-TO-ANALOG CONVERTERS

CELL NAME	DESCRIPTION	SETTLING TIME	POWER	NON-LINEARITY INTEGRAL	NON-LINEARITY DIFFERENTIAL	SIZE SQ. MILS
DAC4BT	4-Bit Flash, Current Output					TBA
DAC8UB	8-Bit Resistor String, Unbuffered	1.1 μsec	5 μW	0.2 LSB	0.1 LSB	908
DAC10B	10-Bit Charge Integration	17 μsec	20 mW	0.5 LSB	0.5 LSB	2569
FDAC8B	8-Bit Flash, Current Output	20 nsec	130 mW	0.5 LSB	0.5 LSB	1294

OPERATIONAL AMPLIFIERS

CELL NAME	GAIN	BAND-WIDTH	PHASE MARGIN	SLEW RATE	POWER	VCM+	VCM–	LOAD	SIZE SQ. MILS
OP02N1	107 dB	1.8 MHz	64	2.7 V/μsec	8 mW	AVD–.15	AVS+1.7	2k/100 pF	412
OP10N1	105 dB	3.0 MHz	65	4 V/μsec	5 mW	AVD–.3	AVS+.3	10k/25 pF	369
OP02P1	110 dB	2.0 MHz	64	3 V/μsec	7 mW	AVD–.5	AVS+.5	2k/100 pF	317
OP10P1	110 dB	3.5 MHz	71	4.5 V/μsec	4 mW	AVD–.4	AVS+.4	10k/25 pF	278
OP02R1									TBA
OP10R1									TBA

1. The suffix N1 means n-channel inputs, P1 means p-channel inputs, R1 means rail to rail inputs.
2. Output current is specified driving minimum Resistive and maximum Capacitive Loads. The R value is indicated by the number in the Op Amp's cell name, and has units in kΩ. Typical input current is negligible; input offset voltage < 10 mV.
3. All cells can drive both on and off chip loads.

ANALOG MULTIPLEXERS/SWITCHES

CELL NAME	FUNCTION	RDS ON*	SIZE SQ. MILS
M21200	2:1 Analog MUX	200 Ω	147
M2101K	2:1 Analog MUX	1000 Ω	91
M2110K	2:1 Analog MUX	10000 Ω	79
M41200	4:1 Analog MUX	200 Ω	229
M4101K	4:1 Analog MUX	1000 Ω	151
M4110K	4:1 Analog MUX	10000 Ω	85
ASW200	Analog Switch	200 Ω	98
ASW01K	Analog Switch	1000 Ω	62
ASW10K	Analog Switch	10000 Ω	56

* RDS On = peak on resistance (worst case, 4.5–5.5 V, 0–70°C)

HIGH/LOW VOLTAGE DETECT/POWER ON RESET

CELL NAME	DESCRIPTION	Vtrip–*	Vtrip+*	Vhyst	POWER	SIZE SQ. MILS
PORID1	Power On Reset (Threshold Ref)					TBA
HVDET1	High Voltage Detect					TBA
LVDET1	Band Gap Reference POR	3.7 V	4.5 V	0.2 V	5 mW	543

* Worst case, 4.5–5.5 V, 0–70°C

VCO/RC OSCILLATORS/PLL

CELL NAME	MAX. FREQUENCY	FREQUENCY ACCURACY	VCO LINEARITY	POWER	SIZE SQ. MILS
OSCHEB	500 kHz				TBA
OSCLEB	50 kHz				TBA
PLL65M	70 MHz Phase Lock Loop Subsystem	±20%	±1%	200 mW	3033

CRYSTAL OSCILLATORS

PC6X01	Low Frequency Crystal Oscillator (1 K–3 MHz)	PC6X11	Low Frequency Crystal Oscillator (1 K–3 MHz)
PC6X02	Intermediate Frequency Crystal Oscillator (1–8 MHz)	PC6X12	Intermediate Frequency Crystal Oscillator (1–8 MHz)
PC6X03	High Frequency Crystal Oscillator (1–25 MHz)	PC6X13	High Frequency Crystal Oscillator (1–25 MHz) (These are Bonding Pad Cells)

VOLTAGE COMPARATORS

CELL NAME	GAIN	RESPONSE TIME†	COMMON MODE	POWER	VOS	SIZE SQ. MILS
CPHSI1	120 dB	35 ns	3.5 V	3.0 mW	4.0 mV	118
CPLSIB						TBA
CPVHS1	80 dB	12 ns	2.5 V	22 mW	25 mV	180
CPVLO1						TBA
CPVLP1						TBA

† For ±10 mV input overdrive (except CPVHSI with ±300 mV).

RS422 Type Driver/Receiver

CELL NAME	DESCRIPTION	V–	V+	PROP. DELAY	POWER	SIZE SQ. MILS
RSRCVR	RS422 Type Differential Receiver	–1.0	5.5	7 ns	44 mW	396
RSDRVR*	RS422 Type Differential Driver			7 ns	0	7

* Soft macro composed of digital standard cells

ANALOG BONDING PADS

PANBID	I/O PAD	PANAVD	Analog Power PAD
PANBSP	Low Leakage I/O PAD	PANAVS	Analog Ground PAD
PANIER	Extended Range Input PAD	PCGHVI	Pad for Test Modes

VOLTAGE-TO-CURRENT CONVERTER

CELL NAME	INPUT RANGE	OUTPUT RANGE	POWER	SIZE SQ. MILS
VTCCEI				TBA

1.5μ DIGITAL CELL LIBRARY

ALL DELAYS AND SPEEDS ARE 4.5 V, 70°C, WORST CASE PROCESS, FAN OUT = 2

BUFFERS

CELL NAME	DESCRIPTION	DELAY NS	GATE EQUIV.
CK01D1	Non-Inverting Clock Buffer, 1X Drive	2.9	1
CK01D2	Non-Inverting Clock Buffer, 2X Drive	1.9	2
CK01D3	Non-Inverting Clock Buffer, 3X Drive	1.6	3
CK02D1	Inverting Clock Buffer, 1X Drive	2.9	1
CK02D2	Inverting Clock Buffer, 2X Drive	1.9	2
CK02D3	Inverting Clock Buffer, 3X Drive	1.6	3
IN01D1	Inverting Buffer, 1X Drive	1.4	1
IN01D2	Inverting Buffer, 2X Drive	0.9	1
IN01D3	Inverting Buffer, 3X Drive	0.6	2
IT01D1	Inverting 3-State Buffer with OE, 1X Drive	3.1	2
IT01D2	Inverting 3-State Buffer with OE, 2X Drive	2.0	2
IT01D3	Inverting 3-State Buffer with OE, 3X Drive	1.9	3
IT02D1	Inverting 3-State Buffer with OEN, 1X Drive	2.8	2
IT02D2	Inverting 3-State Buffer with OEN, 2X Drive	1.7	3
IT02D3	Inverting 3-State Buffer with OEN, 3X Drive	1.5	3
NI01D1	Non-Inverting Buffer, 1X Drive	2.5	1
NI01D2	Non-Inverting Buffer, 2X Drive	1.7	2
NI01D3	Non-Inverting Buffer, 3X Drive	1.8	2
NT01D1	Non-Inverting 3-State Buffer with OE, 1X Drive	3.8	2
NT01D2	Non-Inverting 3-State Buffer with OE, 2X Drive	2.4	3
NT01D3	Non-Inverting 3-State Buffer with OE, 3X Drive	2.5	4
NT02D1	Non-Inverting 3-State Buffer with OEN, 1X Drive	3.8	2
NT01D2	Non-Inverting 3-State Buffer with OE, 2X Drive	2.4	3
NT01D3	Non-Inverting 3-State Buffer with OE, 3X Drive	2.5	4

GATES

CELL NAME	DESCRIPTION	DELAY NS	GATE EQUIV.
AN02D1	2-Input AND	2.4	2
AN03D1	3-Input AND	3.2	2
AN04D1	4-Input AND	3.4	3
AN05D1	5-Input AND	3.8	3
AN06D1	6-Input AND	4.2	4
AN07D1	7-Input AND	4.6	4
AN08D1	8-Input AND	5.3	5
AO01D1	2/2 AND-OR-INVERT	2.7	2
AO02D1	3/3 AND-OR-INVERT	3.9	3
AO03D1	2/2/1 AND-OR-INVERT	4.4	3
AO04D1	2/1 AND-OR-INVERT	3.0	2
AO05D1	2/1/1 AND-OR-INVERT	4.7	2
ND02D1	2-Input NAND	1.7	1
ND03D1	3-Input NAND	2.6	2
ND04D1	4-Input NAND	3.5	2
ND05D1	5-Input NAND	4.0	3
ND06D1	6-Input NAND	4.3	3
ND07D1	7-Input NAND	4.8	4
ND08D1	8-Input NAND	6.2	4
NR02D1	2-Input NOR	3.0	1

CELL NAME	DESCRIPTION	DELAY NS	GATE EQUIV.
NR03D1	3-Input NOR	4.3	2
NR04D1	4-Input NOR	5.6	2
NR05D1	5-Input NOR	7.3	3
NR06D1	6-Input NOR	8.9	3
NR07D1	7-Input NOR	11.3	4
NR08D1	8-Input NOR	13.6	4
OA01D1	2/2 OR-AND-INVERT	3.6	2
OA02D1	3/3 OR-AND-INVERT	7.0	3
OA03D1	2/2/1 OR-AND-INVERT	7.0	3
OA04D1	2/1 OR-AND-INVERT	3.6	2
OA05D1	2/1/1 OR-AND-INVERT	4.1	2
OR02D1	2-Input OR	3.2	2
OR03D1	3-Input OR	3.6	2
OR04D1	4-Input OR	4.6	3
OR05D1	5-Input OR	6.1	3
OR06D1	6-Input OR	7.4	4
OR07D1	7-Input OR	9.0	4
OR08D1	8-Input OR	10.2	5
XN02D1	2-Input Exclusive NOR	3.0	3
XO02D1	2-Input Exclusive OR	4.1	3

DECODERS/MULTIPLEXERS

CELL NAME	DESCRIPTION	DELAY NS	GATE EQUIV.
DC24D1	2-to-4 Line Decoder	4.1	5
DC38D1	3-to-8 Line Decoder	6.5	14
DE24D1	2-to-4 Line Decoder with Enable	5.7	8
ME41D1	4-to-1 Multiplexer with Enable	6.9	10
MX21D1	2-to-1 Multiplexer	4.1	3
MX41D1	4-to-1 Multiplexer	5.7	7
MX81D1	8-to-1 Multiplexer	8.1	16

ARITHMETIC FUNCTIONS

CELL NAME	DESCRIPTION	DELAY NS	GATE EQUIV.
AD01D1	1-Bit Full Adder	7.4	10
AD02D1	2-Bit Full Adder	9.2	18
AS01D1	1-Bit Adder/Subtractor	9.5	12
AS02D1	2-Bit Adder/Subtractor	11.3	23

FLIP-FLOPS/LATCHES

CELL NAME	DESCRIPTION	SPEED MHZ	GATE EQUIV.
DFBNNB	D Flip-Flop with Clear, Preset, Buffered Outputs	97	8
DFBNNN	D Flip-Flop with Clear, Preset	72	7
DFBNNT	D Flip-Flop with Clear, Preset, 3-State Output	97	10
DFBTNB	Buffered D Flip-Flop with Clear, Preset	83	9
DFBTNN	D Flip-Flop with Clear, Preset, Buffered Clock	55	8
DFBTNT	Buffered D Flip-Flop with Clear, Preset, 3-State Output	83	11
DFCNNB	D Flip-Flop with Clear, Buffered Outputs	122	7
DFCNNN	D Flip-Flop with Clear	77	6
DFCNNT	D FLip-Flop with Clear, 3-State Output	123	9
DFCTNB	Buffered D Flip-Flop with Clear	102	8
DFCTNN	D Flip-Flop with Clear, Buffered Clock	–	7
DFCTNT	Buffered D Flip-Flop with Clear, 3-State Output	102	10
DFNNNB	D Flip-Flop with Buffered Outputs	123	6
DFNNNN	D Flip-Flop	26	5
DFNNNT	D Flip-Flop with 3-State Output	123	8
DFNTNB	Buffered D Flip-Flop	101	7
DFNTNN	D Flip-Flop with Buffered Clock	–	6
DFNTNT	Buffered D Flip-Flop with 3-State Output	101	9
DFPNNB	D Flip-Flop with Preset, Buffered Outputs	95	7
DFPNNN	D Flip-Flop with Preset	83	6
DFPNNT	D Flip-Flop with Preset, 3-State Output	96	9
DFPTNB	Buffered D Flip-Flop with Preset	82	8
DFPTNN	D Flip-Flop with Preset, Buffered Clock	–	7
DFPTNT	Buffered D Flip-Flop with Preset, 3-State Output	83	10
JKBNNB	JK Flip-Flop with Clear, Preset, Buffered Outputs	65	11
JKBNNN	JK Flip-Flop with Clear, Preset	59	10
JKBNNT	JK Flip-Flop with Clear, Preset, 3-State Output	65	13
JKBTNB	Buffered JK Flip-Flop with Clear, Preset	64	12
JKBTNN	JK Flip-Flop with Clear, Preset, Buffered Clock	–	11
JKBTNT	Buffered JK Flip-Flop with Clear, Preset, 3-State Output	64	14
JKCNNB	JK Flip-Flop with Clear, Buffered Outputs	63	10
JKCNNN	JK Flip-Flop with Clear	63	9
JKCTNB	Buffered JK Flip-Flop with Clear	63	11
JKCTNN	JK Flip-Flop with Clear, Buffered Clock	–	10
JKNNNB	JK Flip-Flop with Buffered Outputs	67	9
JKNNNN	JK Flip-Flop	60	8
JKNTNB	Buffered JK Flip-Flop	67	10
JKNTNN	JK Flip-Flop with Buffered Clock	–	9
LABFNB	Buffered Latch with Clear, Preset	94	6
LABFNN	Latch with Clear, Preset, Buffered Clock	–	5
LABFNT	Buffered Latch with Clear, Preset, 3-State Output	95	8
LABNNB	Latch with Clear, Preset, Buffered Outputs	113	5
LABNNN	Latch with Clear, Preset	88	4
LABNNT	Latch with Clear, Preset, 3-State Output	114	7
LACFNB	Buffered Latch with Clear	77	5
LACFNN	Latch with Clear, Buffered Clock	–	4
LACFNT	Buffered Latch with Clear, 3-State Output	78	7
LACNNB	Latch with Clear, Buffered Outputs	90	4
LACNNN	Latch with Clear	84	3

FLIP-FLOPS/LATCHES (CONT.)

CELL NAME	DESCRIPTION	SPEED MHZ	GATE EQUIV.
LACNNT	Latch with Clear, 3-State Output	90	6
LACTNN	Latch with Clear, Active High Buffered Clock	–	4
LANFNB	Buffered Latch	86	5
LANFNN	Latch with Buffered Clock	–	4
LANFNT	Buffered Latch with 3-State Output	85	7
LANNNB	Latch with Buffered Outputs	101	4
LANNNN	Latch	113	3
LANNNT	Latch with 3-State Output	101	6
LANTNB	Buffered Latch, Active High Buffered Clock	87	5
LANTNN	Latch with Active High Buffered Clock	–	4
LAPFNB	Buffered Latch with Preset	107	6
LAPFNN	Latch with Clear, Preset, Buffered Clock	–	5
LAPFNT	Buffered Latch with Preset, 3-State Output	107	8
LAPNNB	Latch with Preset, Buffered Outputs	134	5
LAPNNN	Latch with Preset	45	4
LAPNNT	Latch with Preset, 3-State Output	133	7
MFBTNB	Buffered MUX Flip-Flop with Clear, Preset	83	12
MFBTNT	Buffered MUX Flip-Flop with Clear, Preset, 3-State Output	83	14
MFCTNB	Buffered MUX Flip-Flop with Clear, Buffered Clock and Output	82	11
SCBNNB	Synchronous Counter with Clear, Preset, Buffered Outputs	59	11
SCBNNN	Synchronous Counter with Clear, Preset	53	10
SCBNNT	Synchronous Counter with Clear, Preset, 3-State Outputs	59	13
SCBTNB	Buffered Synchronous Counter with Clear, Preset	59	12
SCBTNN	Synchronous Counter Clear, Preset, Buffered Clock	–	11
SCBTNT	Buffered Synchronous Counter with Clear, Preset, 3-State O/P	59	14
SCCNNB	Synchronous Counter with Clear, Buffered Outputs	58	10
SCCNNN	Synchronous Counter with Clear	63	9
SCCNNT	Synchronous Counter with Clear, 3-State Output	58	12
SCCTNB	Buffered Synchronous Counter with Clear	58	11
SCCTNN	Synchronous Counter with Clear, Buffered Clock	–	10
SCCTNT	Buffered Synchronous Counter with Clear, 3-State Output	58	13
TFBNNB	T Flip-Flop with Clear, Preset, Buffered Outputs	78	8
TFBNNN	T Flip-Flop with Clear, Preset	74	7
TFBNNT	T Flip-Flop with Clear, Preset, 3-State Output	79	10
TFBTNB	T Flip-Flop with Clear, Preset	80	9
TFCNNB	T Flip-Flop with Clear, Buffered Outputs	85	7
TFCNNN	T Flip-Flop with Clear	88	6
TFCTNB	T Flip-Flop with Clear	85	8
TFPNNB	T Flip-Flop with Preset, Buffered Outputs	80	7
TFPNNN	T Flip-Flop with Preset	72	6

COP880 CORE MICROCONTROLLER FAMILY

CELL NAME	ROM (BYTES)	RAM (BYTES)	SIZE (SQ. MILS)	CELL NAME	ROM (BYTES)	RAM (BYTES)	SIZE (SQ. MILS)
M0K64B	0K	64	5730	M2K192B	2K	192	8050
M0K128B	0K	128	6110	M4K64B	4K	64	7640
M0K192B	0K	192	6960	M4K128B	4K	128	8490
M1K64B	1K	64	5730	M4K192B	4K	192	9330
M1K128B	1K	128	6530	M8K64B	8K	64	10210
M1K192B	1K	192	7410	M8K128B	8K	128	11050
M2K64B	2K	64	6360	M8K192B	8K	192	11905
M2K128B	2K	128	7200				

SOFT MACRO PERIPHERALS

CELL NAME	DESCRIPTION	GATE COUNT
COPLCD	36-Segment Triplex LCD Controller	950
COPIP8	8-Bit Input Port	70
COPOP8	8-Bit Output Port	120
COPBP8	8-Bit Input/Output Port	200
COPRTC	Real Time Clock (Equivalent to NSC 58174)	1848
COPURT	UART (8250 Subset)	1769

* COPS is a trademark of National Semiconductor Corporation

PADs, PAD DRIVERS, LEVEL SHIFTERS

CELL NAME	DESCRIPTION	CELL NAME	DESCRIPTION
PC6O01	CMOS Output Pad (2 mA)	PT6O01	TTL Output Pad (2 mA)
PC6O02	CMOS Output Pad (4 mA)	PT6O02	TTL Output Pad (4 mA)
PC6O03	CMOS Output Pad (8 mA)	PT6O03	TTL Output Pad (8 mA)
PC6O04	CMOS Output Only Pad (12 mA)	PT6O04	TTL Output Only Pad (12 mA)
PC6O05	CMOS Output Only Pad (16 mA)	PT6O05	TTL Output Only Pad (16 mA)
PC6O11	3-State Output Pad with Input, Pullup (2 mA)	PT6O11	3-State Output Pad with Input, Pullup (2 mA)
PC6O12	3-State Output Pad with Input, Pullup (4 mA)	PT6O12	3-State Output Pad with Input, Pullup (4 mA)
PC6O13	3-State Output Pad with Input, Pullup (8 mA)	PT6O13	3-State Output Pad with Input, Pullup (8 mA)
PC6O14	3-State Output Pad with Input, Pullup (12 mA)	PT6O14	3-State Output Pad with Input, Pullup (12 mA)
PC6O15	3-State Output Pad with Input, Pullup (16 mA)	PT6O15	3-State Output Pad with Input, Pullup (16 mA)
PC6O21	3-State Output Pad with Input, Pulldown (2 mA)	PT6O21	3-State Output Pad with Input, Pulldown (2 mA)
PC6O22	3-State Output Pad with Input, Pulldown (4 mA)	PT6O22	3-State Output Pad with Input, Pulldown (4 mA)
PC6O23	3-State Output Pad with Input, Pulldown (8 mA)	PT6O23	3-State Output Pad with Input, Pulldown (8 mA)
PC6O24	3-State Output Pad with Input, Pulldown (12 mA)	PT6O24	3-State Output Pad with Input, Pulldown (12 mA)
PC6O25	3-State Output Pad with Input, Pulldown (16 mA)	PT6O25	3-State Output Pad with Input, Pulldown (16 mA)
PC6O41	3-State Output Pad with Input (2 mA)	PT6O41	3-State Output Pad with Input (2 mA)
PC6O42	3-State Output Pad with Input (4 mA)	PT6O42	3-State Output Pad with Input (4 mA)
PC6O43	3-State Output Pad with Input (8 mA)	PT6O43	3-State Output Pad with Input (8 mA)
PC6O44	3-State Output Pad with Input (12 mA)	PT6O44	3-State Output Pad with Input (12 mA)
PC6O45	3-State Output Pad with Input (16 mA)	PT6O45	3-State Output Pad with Input (16 mA)
PC6D00	Input Pad	LSCC00	CMOS Input Buffer
PC6D10	Input Pad with Pullup	LSSC00	Schmitt Trigger Input Buffer
PC6D20	Input Pad with Pulldown	LSTC00	TTL Level Shifter

TTL MACRO LIBRARY

CELL NAME	DESCRIPTION	GATE COUNT
VSC85	4-Bit Magnitude Comparator	39
VSC90	4-Bit Decade Ripple Counter	47
VSC92	Divide by 12 Ripple Counter	42
VSC93	4-Bit Binary Ripple Counter	34
VSC94	4-Bit Shift Register	47
VSC95	4-Bit Right/Left Shift Register	44
VSC137	1 of 8 Decoder/Demultiplexer	30
VSC138	1 of 8 Decoder/Demultiplexer	20
VSC148	8 Input Priority Encoder	38
VSC150	16 Input Multiplexer	64
VSC154	1 of 16 Decoder/Demultiplexer	47
VSC157	Quad 2 Input Data Selector	19
VSC160	Synchronous BCD Decade Counter	66
VSC161	Synchronous 4-Bit Binary Counter	68
VSC162	Synchronous BCD Counter	64
VSC163	Synchronous 4-Bit Binary Counter	61
VSC164	8-Bit Serial-In-Parallel-Out Shift Register	69
VSC165	8-Bit Parallel-In-Serial-Out Shift Register	92
VSC166	8-Bit Parallel-In-Serial-Out Shift Register	89
VSC168	Synchronous BCD Decade Up/Down Counter	88
VSC169	Synchronous 4-Bit Binary Up/Down Counter	81
VSC173	Quad D Type Flip-Flop (3-State)	56
VSC174	Hex D Type Flip-Flop with Reset	50
VSC175	Quad D Type Edge-Triggered Flip-Flop with Reset	32
VSC180	8-Bit Odd/Even Parity Generator/Checker	23
VSC181	4-Bit ALU	93
VSC182	Look-Ahead Carry Generator	37
VSC190	Presettable BCD Decade Up/Down Counter	84
VSC191	Presettable 4-Bit Binary Up/Down Counter	80
VSC191D		
_4 Bit	4-Bit Binary Down Counter	67
_5 Bit	5-Bit Binary Down Counter	82
_6 Bit	6-Bit Binary Down Counter	98
VSC191U		
_4 Bit	4-Bit Binary Up Counter	67
_5 Bit	5-Bit Binary Up Counter	82
_6 Bit	6-Bit Binary Up Counter	98
VSC192	Presettable BCD Decade Up/Down Counter	77
VSC193	Presettable 4-Bit Binary Up/Down Counter	71
VSC194	4-Bit Bidirectional Universal Shift Register	60
VSC195	4-Bit Parallel Access Shift Register	50
VSC198	8-Bit Right/Left Shift Register	108
VSC199	8-Bit Parallel Access Shift Register	95
VSC240	Octal Inverter/Buffer (3-State)	20
VSC242	Octal Bus Inverting Transceiver (3-State)	18
VSC244	Octal Buffer (3-State)	22
VSC245	Octal Bus Transceiver (3-State)	44
VSC253	Dual 4 to 1 Multiplexer (3-State)	18
VSC258	Quad 2 Line to 1 Line Data Selector/MUX (3-State)	19
VSC273	Octal D Type Flip-Flop with Reset	67
VSC274	4-Bit by 4-Bit Binary Multiplier	154
VSC280	9-Bit Odd/Even Parity Generator/Checker	23
VSC283	4-Bit Full Adder with Fast Carry	36
VSC373	Octal Transparent Latch (3-State)	53
VSC374	Octal D Type Flip-Flop (3-State)	73
VSC521	8-Bit Parity Checker	27

1.5μ COMPILER LIBRARY

- ROM
- RAM
- PLA
- N X M MULTIPLIER
- STATE MACHINE
- DATA PATH

1.5μ NON-VOLATILE LIBRARY

RUGGED EEPROM†

CELL NAME	TOTAL BITS*	DESCRIPTION	WRITE CYCLE	ACCESS TIME	SIZE SQ. MILS
EEARRY	16	16 x 1 EEPROM ARRAY	10 ms	80 ns	640
	32	32 x 1 EEPROM ARRAY	10 ms	80 ns	774
	64	64 x 1, 16 x 4, 8 x 8 EEPROM ARRAY	10 ms	80 ns	1044
	128	128 x 1, 32 x 4, 16 x 8, 8 x 16 EEPROM ARRAY	10 ms	80 ns	1585
	256	64 x 4, 32 x 8, 16 x 16 EEPROM ARRAY	10 ms	80 ns	2130

† Rugged EE is a failure tolerant, redundant dual transistor cell design which facilitates simple application and testing.
* Larger arrays are available on a custom basis; consult factory.

RUGGED EELOGIC†

CELL NAME	DESCRIPTION	MAX. CLOCK FREQUENCY	WRITE CYCLE	GATE EQUIV.
EEDFFC	4-Bit EE D Register with Clear	9 MHz	21 ms	89
EEDFSC	4-Bit EE D Register with Clear, Preset	9 MHz	21 ms	93
EEDFST	4-Bit EE D Register	9 MHz	21 ms	102
EEDUAL	2-Bit EE D Register with Individual Program Enable Not	9 MHz	21 ms	66
EENLAC	4-Bit EE Latch with Clear	9 MHz	21 ms	74
EETFST	4-Bit EE Counter with Parallel Load	9 MHz	21 ms	110

† Rugged EE is a failure tolerant, redundant dual transistor cell design which facillitates simple application and testing. The term "EE" is for electrically erasable; all EELOGIC devices are electrically erasable and programmable.

RUGGED EEPROM SHIFT REGISTERS

CELL NAME	DESCRIPTION	WRITE TIME	CLOCK TO Q DELAY	RECALL TIME	SIZE SQ. MILS
EER004	4-Bit EEPROM Shift Register	21 ms	30 ns	50 ns	135
EER008	8-Bit EEPROM Shift Register	21 ms	30 ns	50 ns	233
EER016	16-Bit EEPROM Shift Register	21 ms	30 ns	50 ns	429
EER032	32-Bit EEPROM Shift Register	21 ms	30 ns	50 ns	822
EER064	64-Bit EEPROM Shift Register	21 ms	30 ns	50 ns	1607
EER128	128-Bit EEPROM Shift Register	21 ms	30 ns	50 ns	3341

* All Delay and Recall times assume 1 pF load.

PROGRAMMING SUPPLIES

CELL NAME	DESCRIPTION	MAX BITS	SIZE SQ. MILS
EEHVP0	Port for Controlled External Vpp	–	28
EEHVS4	Internal Vpp Generator	TBA	868

Programming supply operation is 15 V to 17 V, Tj = 0° to 85°C, unless otherwise indicated.

HIGH VOLTAGE PADS

CELL NAME	DESCRIPTION
EEPAD1	High Voltage PAD for Vpp
EEPAD2	High Voltage PAD for EEHVS4 Interface

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Packaging/Ordering Information 5

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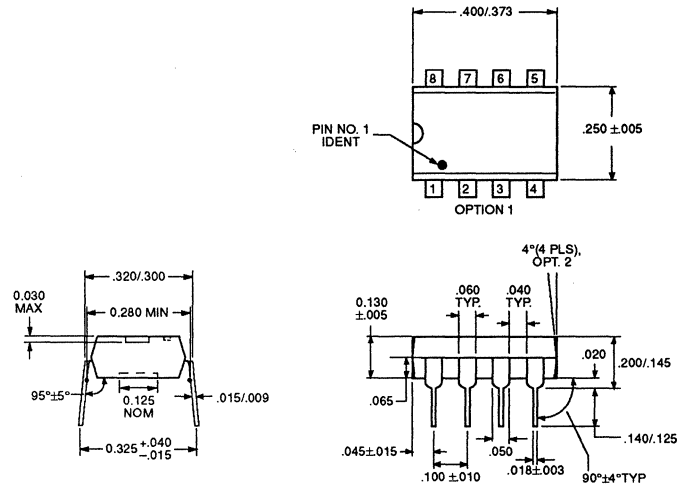
Product Number/Physical Dimension Cross Reference

Product Number	Package Type	No. Pins	Page No.
SC11000CN	DIP	24	731
SC11001CN	DIP	24	731
SC11001CV	PLCC	28	735
SC11002CN	DIP	20	730
SC11002CM	SOIC	20	734
SC11003CN	DIP	20	730
SC11003CM	SOIC	20	734
SC11004CN	DIP	24	731
SC11004CV	PLCC	28	735
SC11005CN	DIP	24	731
SC11005CV	PLCC	28	735
SC11006CN	DIP	28	732
SC11006CV	PLCC	28	735
SC11007CN	DIP	28	732
SC11007CV	PLCC	28	735
SC11008CN	DIP	28	732
SC11008CV	PLCC	28	735
SC11011CV	PLCC	68	735
SC11014CN	DIP	24	731
SC11014CV	PLCC	28	735
SC11015CN	DIP	24	731
SC11015CV	PLCC	28	735
SC11016CN	DIP	24	731
SC11016CV	PLCC	28	735
SC11017CN	DIP	28	732
SC11017CV	PLCC	28	735
SC11019CN	DIP	48	733
SC11019CV	PLCC	44	735
SC11020CN	DIP	48	733
SC11020CV	PLCC	44	735
SC11021CV	PLCC	68	735
SC11022CN	DIP	48	733
SC11022CV	PLCC	68	735
SC11023CV	PLCC	44	735
SC11024CN	DIP	28	732
SC11024CV	PLCC	28	735
SC11026CN	DIP	28	732
SC11026CV	PLCC	28	735
SC11027CN	DIP	28	732
SC11027CV	PLCC	28	735
SC11028CN	DIP	28	732
SC11028CV	PLCC	28	735
SC11033CN	DIP	28	732
SC11033CV	PLCC	28	735
SC11036CN	DIP	18	729
SC11037CN	DIP	28	732
SC11037CV	PLCC	28	735
SC11046CN	DIP	28	732
SC11046CV	PLCC	28	735
SC11054CN	DIP	28	732
SC11054CV	PLCC	28	735
SC11061CV	PLCC	68	735
SC11074CV	PLCC	44	735
SC11075CV	PLCC	44	735
SC11091CV	PLCC	68	735
SC11122CN	DIP	20	730
SC11122CV	PLCC	28	735
SC11171CN	DIP	28	732
SC11171CV	PLCC	28	735
SC11176CN	DIP	28	732
SC11176CV	PLCC	28	735
SC11202CN	DIP	18	729
SC11202CM	SOIC	16	734
SC11203CN	DIP	18	729
SC11203CM	SOIC	20	734
SC11204CN	DIP	14	728
SC11204CM	SOIC	16	734
SC11270CN	DIP	18	729
SC11270CM	SOIC	18	734
SC11271CN	DIP	18	729
SC11271CM	SOIC	18	734
SC11280CN	DIP	20	730
SC11280CV	PLCC	28	735
SC11289CN	DIP	22	730
SC11290CN	DIP	22	730
SC11290CV	PLCC	28	735
SC11296CN	DIP	40	732
SC11296CV	PLCC	44	735
SC11305CN	DIP	20	730
SC11306CN	DIP	20	730
SC11310CN	DIP	20	730
SC11310CV	PLCC	28	735
SC11313CN	DIP	14	728
SC11313CM	SOIC	14	733
SC11314CN	DIP	8	728
SC11314CM	SOIC	14	733
SC11319CN	DIP	14	728
SC11319CM	SOIC	20	734
SC11320CT	PGA	121	736
SC11320CQ	QFP	100	736
SC11322CN	DIP	20	730
SC11322CM	SOIC	20	734
SC11324CN	DIP	20	730
SC11324CM	SOIC	20	734
SC11327CN	DIP	20	730
SC11327CM	SOIC	20	734
SC11328CN	DIP	24	731
SC11328CV	PLCC	28	735
SC11330CN	DIP	16	729
SC11346CN	DIP	16	729
SC11346CM	SOIC	16	734
SC11360CN	DIP	28	732
SC11360CV	PLCC	28	735
SC11401CN	DIP	24	731
SC11402CN	DIP	20	730
SC11403CN	DIP	24	731
SC11404CN	DIP	20	730
SC11410CV	PLCC	28	735
SC11411CN	DIP	20	730
SC11411CM	SOIC	16	734
SC11471CV	PLCC	44	735
SC11476CN	DIP	28	732
SC11476CV	PLCC	44	735
SC11478CV	PLCC	44	735
SC11481CV	PLCC	44	735
SC11486CN	DIP	28	732
SC11486CV	PLCC	44	735
SC11488CV	PLCC	44	735
SC22201CN	DIP	18	729
SC22201CM	SOIC	20	734
SC22318CN	DIP	24	731
SC22318CV	PLCC	28	735
SC22322CN	DIP	20	730
SC22324CN	DIP	20	730

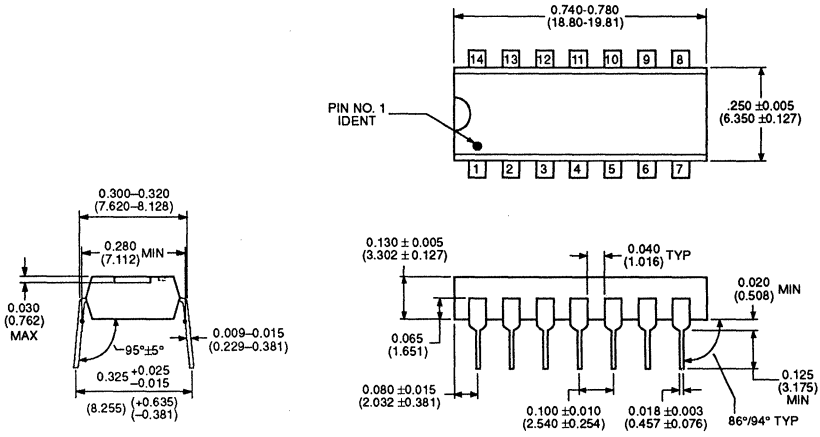
PHYSICAL DIMENSIONS—Inches (Millimeters)

Package 8-Lead Molded DIP

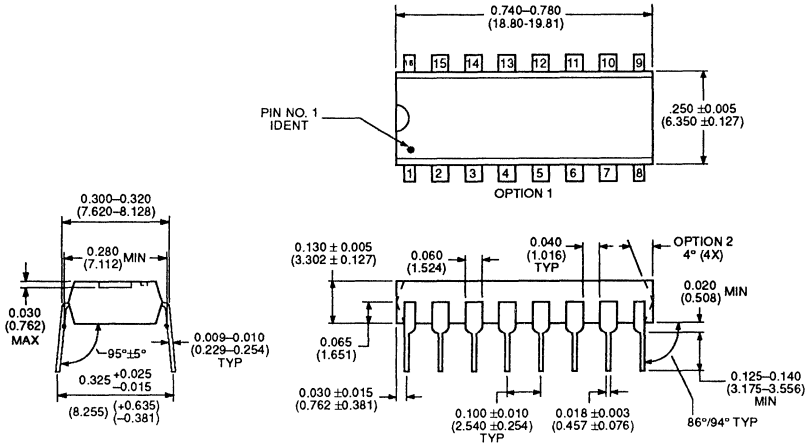


Package 14-Lead Molded DIP

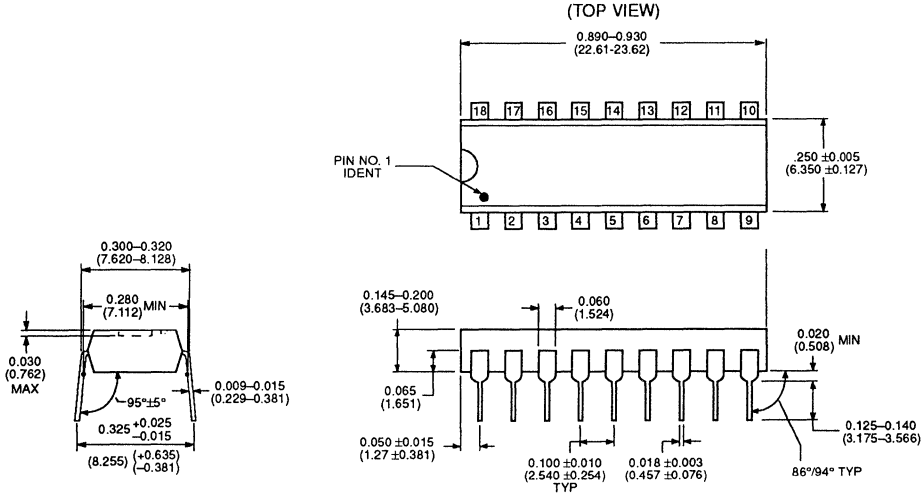
(TOP VIEW)



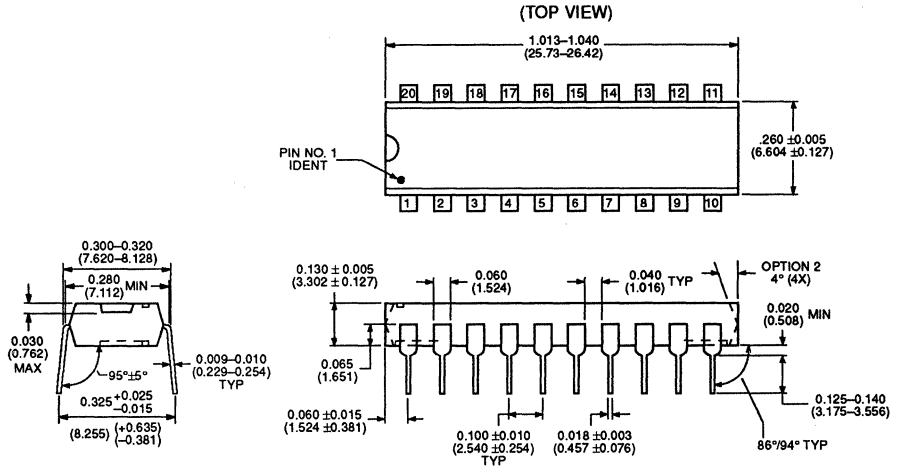
Package 16-Lead Molded DIP



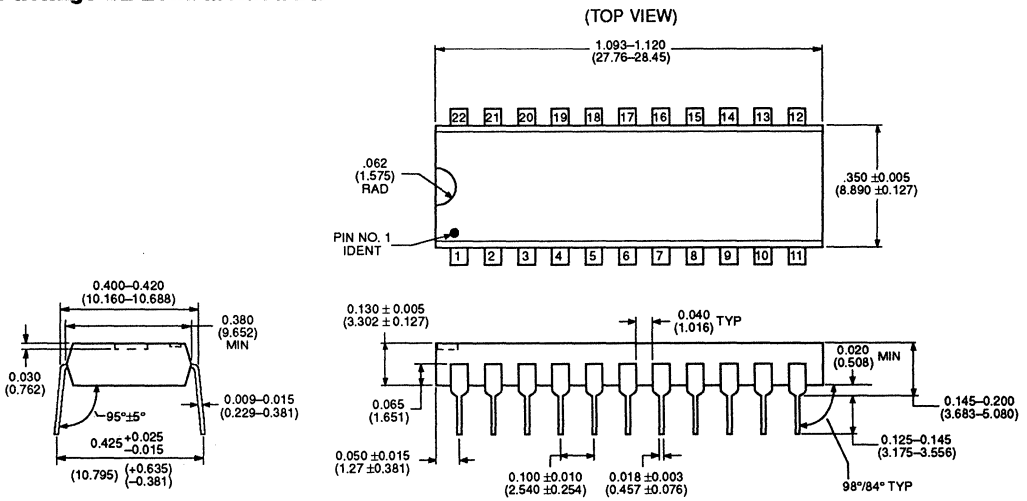
Package 18-Lead Molded DIP



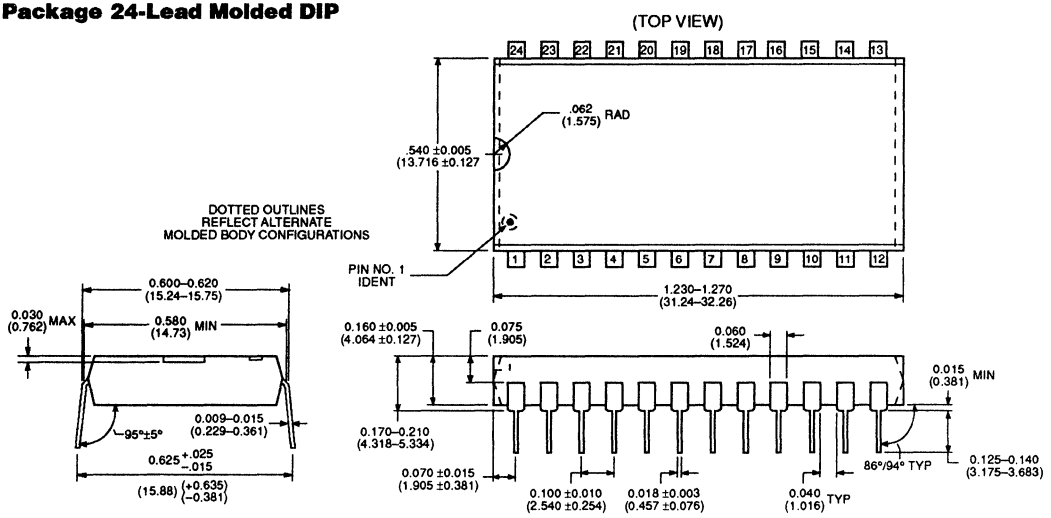
Package 20-Lead Molded DIP



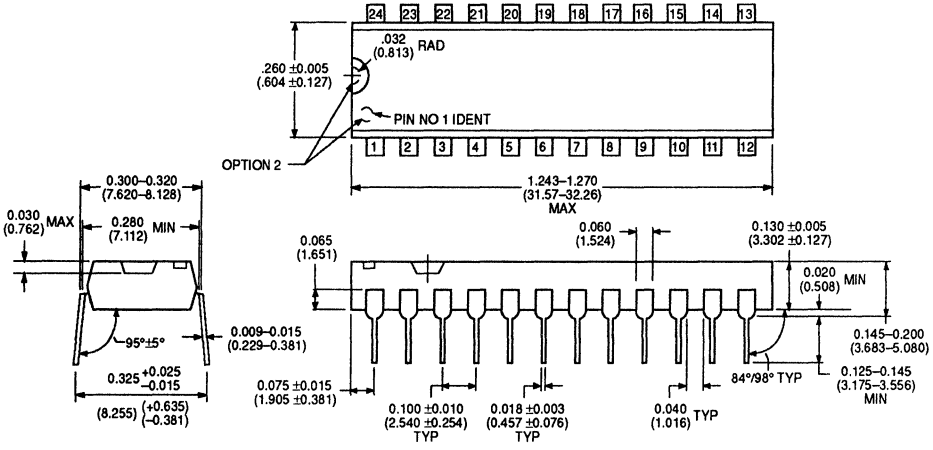
Package 22-Lead Molded DIP



Package 24-Lead Molded DIP

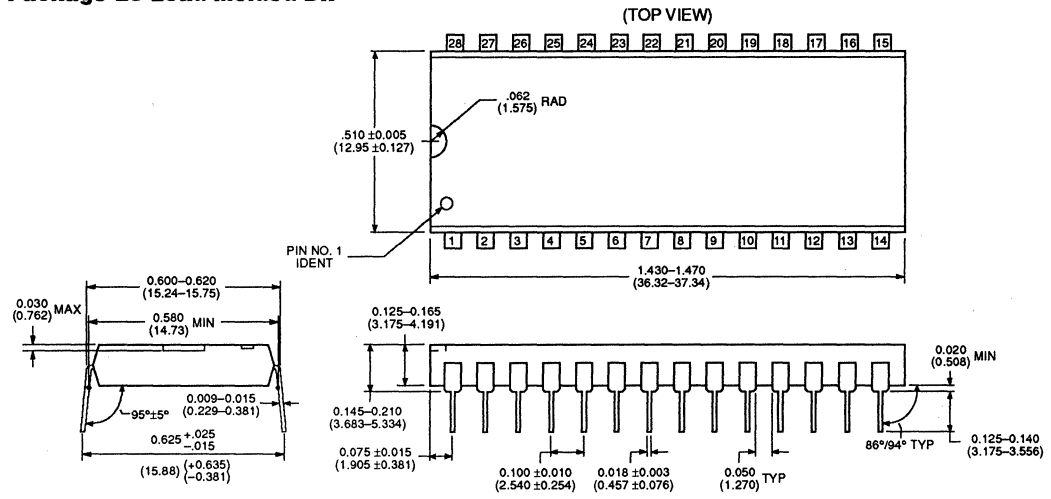


Package 24-Lead Molded Skinny DIP

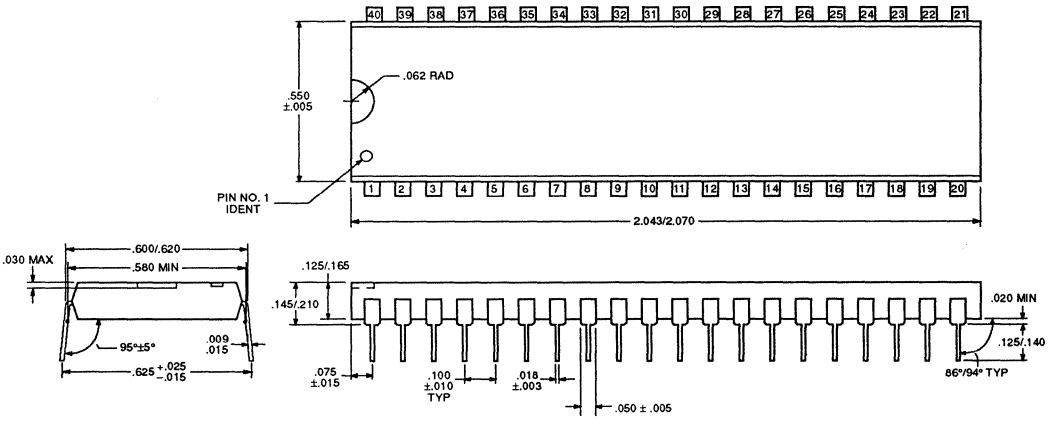


5

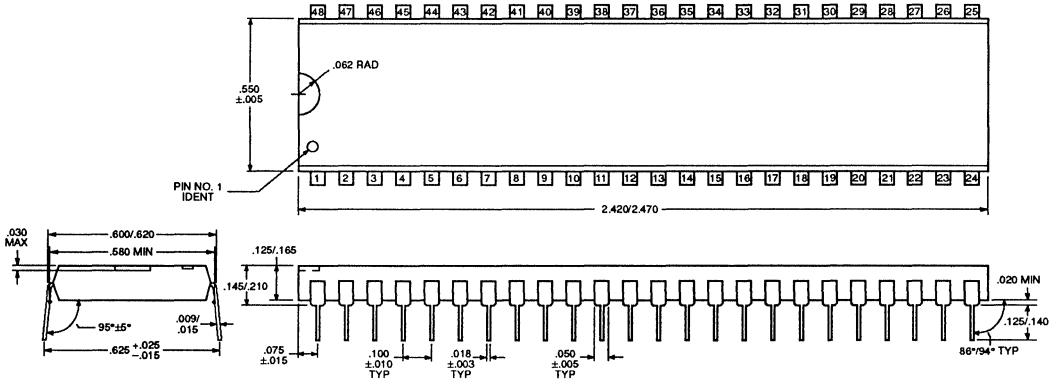
Package 28-Lead Molded DIP



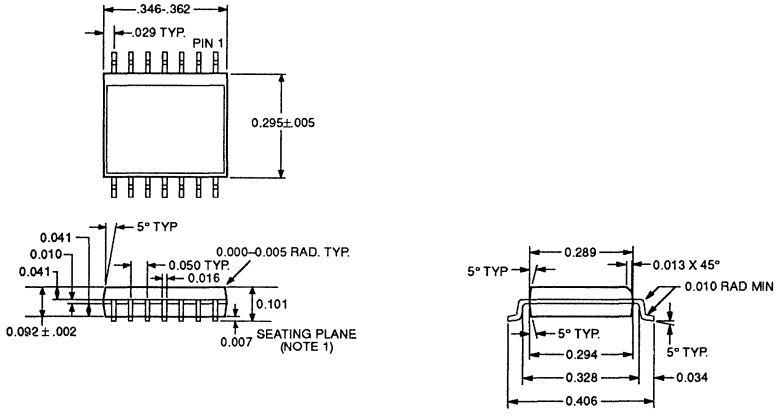
Package 40-Lead Molded DIP



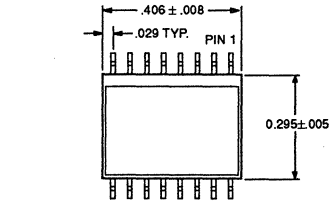
Package 48-Lead Molded DIP

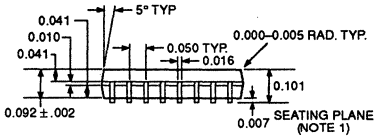


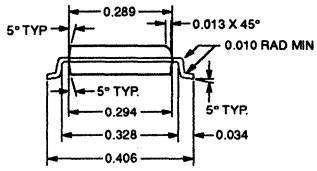
Package 14-Lead SOIC



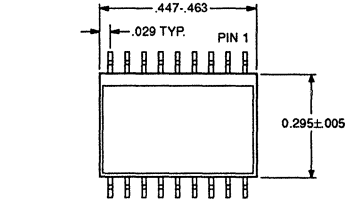
Package 16-Lead SOIC

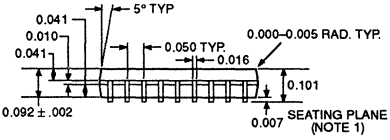


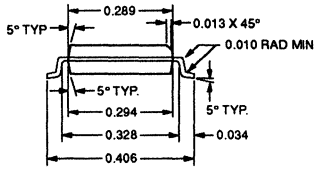




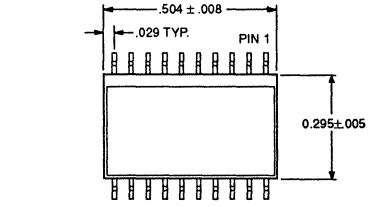
Package 18-Lead SOIC

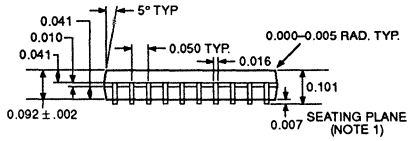


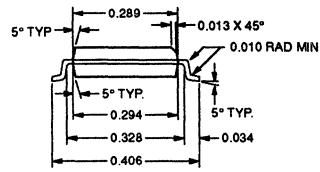




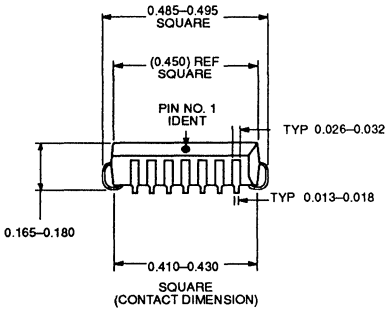
Package 20-Lead SOIC

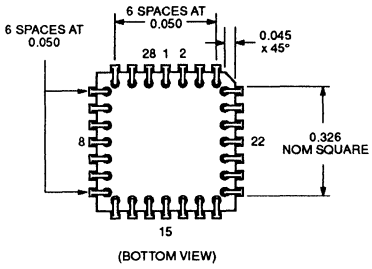




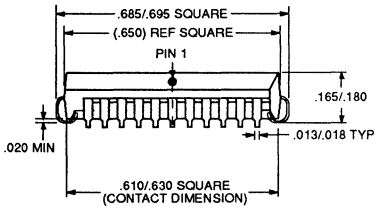


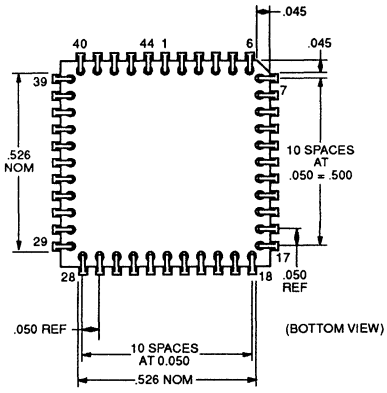
Package 28-Lead Plastic Chip Carrier



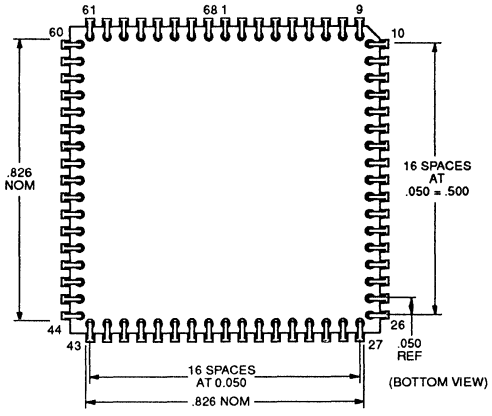


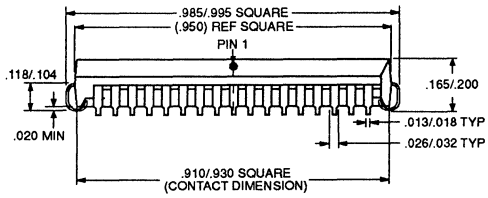
Package 44-Lead Plastic Chip Carrier



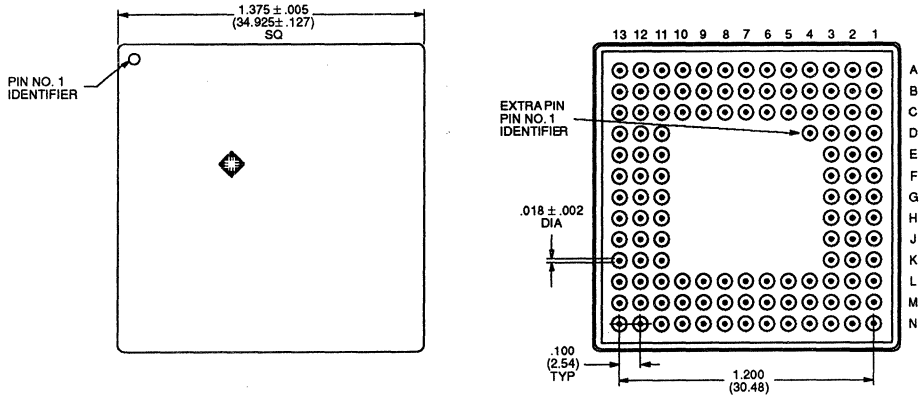


Package 68-Lead Plastic Chip Carrier

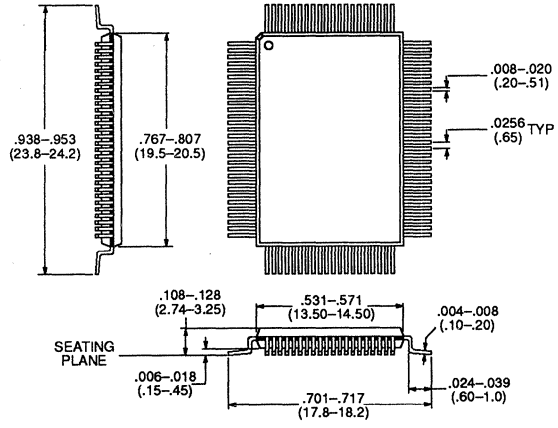


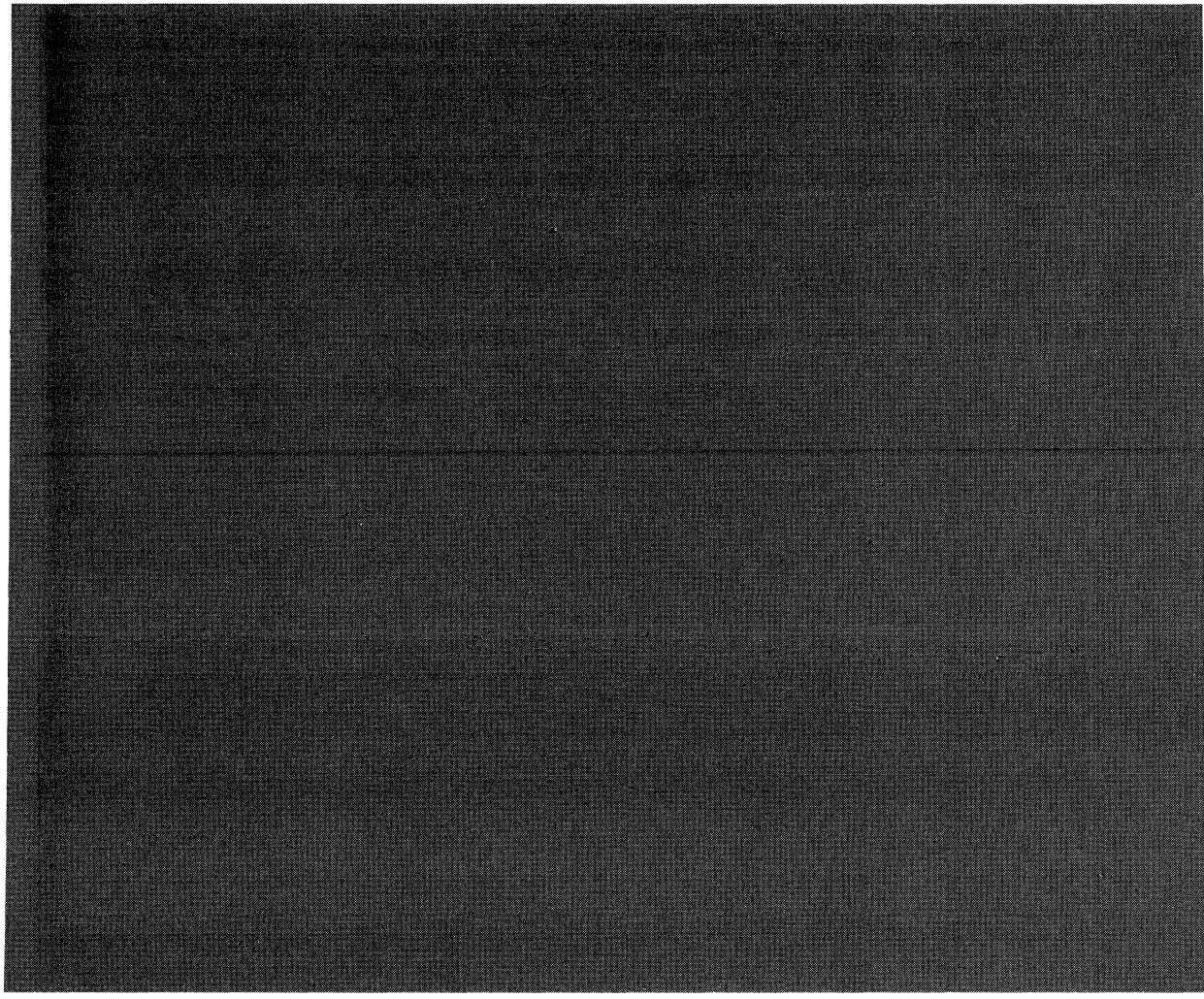


Package 121-Pin Plastic Grid Array



Package 100-Pin Quad Flat Pack





Sales Office/Distributors 6

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SIERRA SEMICONDUCTOR NORTH AMERICAN SALES OFFICES

Corporate Headquarters
SIERRA SEMICONDUCTOR
2075 No. Capitol Ave.
San Jose, CA 95132
PH: 408-263-9300
FAX: 408-263-3337

Northwest Regional Office
(Same as Headquarters)

N. Central Regional Office
SIERRA SEMICONDUCTOR
3100 W. Higgins Road, Suite 175
Hoffman Estates, IL 60195
PH: 708-882-0490
FAX: 708-882-0668

Southwest Regional Office
SIERRA SEMICONDUCTOR
17870 Sky Park Circle, Ste. 107
Irvine, CA 92714-6242
PH: 714-261-5707
FAX: 714-261-2738

Northeast Regional Office
SIERRA SEMICONDUCTOR
101 Cambridge St.
Burlington, MA 01803
PH: 617-229-6868
FAX: 617-229-6849

S. Central Regional Office
SIERRA SEMICONDUCTOR
801 E. Campbell Rd., Ste. 255
Richardson, TX 75081
PH: 214-783-8284
FAX: 214-680-2271

Southeast Regional Office
SIERRA SEMICONDUCTOR
6525 The Corners Pkwy., Ste. 400
Norcross, GA 30092
PH: 404-729-6860
FAX: 404-729-6862

ALABAMA
MONTGOMERY MKTG., INC.
1910 Sparkman Drive
Huntsville, AL 35816
PH: 205-830-0498
FAX: 205-837-7049

ARIZONA
SUMMIT SALES
7802 East Gray Rd., Ste. 600
Scottsdale, AZ 85260
PH: 602-998-4850
FAX: 602-998-5274

ARKANSAS
LOGIC 1 SALES
200 East Spring Valley, Ste. A
Richardson, TX 75081
PH: 214-234-0765
FAX: 214-669-3042

CALIFORNIA
BROOKS TECHNICAL GROUP
883 N. Shoreline Blvd.
Mountain View, CA 94043
PH: 415-960-3880
FAX: 415-960-3615

BROOKS TECHNICAL GROUP
3025 Alhambra Dr. #14
Cameron Park, CA 95682
PH: 916-676-2025
FAX: 916-676-1218

PATHFINDER ELECTRONICS
9747 Business Park Ave.
Ste 202-C
San Diego, CA 92131
PH: 619-578-2555
FAX: 619-578-7659

SPINNAKER SALES
17870 Sky Park Circle
Suite 107
Irvine, CA 92714-6242
PH: 714-261-7233
FAX: 714-261-0963

COLORADO
WESCOM
4891 Independence St., Ste. 235
Wheat Ridge, CO 80033
PH: 303-422-8957
FAX: 303-422-9892

CONNECTICUT
LINDCO ASSOCIATES, INC.
Corner Stone Professional Park
Suite C101
Woodbury, CT 06798
PH: 203-266-0728
FAX: 203-266-0784

DELAWARE
THIRDWAVE SOLUTIONS
8335-H Guilford Rd.
Columbia, MD 21046
PH: 301-290-5990
FAX: 301-381-5846

DIST. OF COLUMBIA
THIRD WAVE SOLUTIONS
8335 H Guilford Road
Columbia, MD 21046
PH: 301-290-5990
FAX: 301-381-5846

FLORIDA
S.E.C.
901 Douglas Ave, Ste. 200
Altamonte Springs, FL 32714
PH: 407-682-4800
FAX: 407-682-6491

S.E.C.
776 S. Military Trail
Deerfield Beach, FL 33442-3025
PH: 305-426-4601
FAX: 305-427-7338

GEORGIA
MONTGOMERY MKTG., INC.
3000 Northwoods Parkway
Suite 110
Norcross, GA 30071
PH: 404-447-6124
FAX: 404-447-0422

HAWAII
BROOKS TECHNICAL GROUP
883 N. Shoreline Blvd.
Mountain View, CA 94043
PH: 415-960-3880
FAX: 415-960-3615

IDAHO
WESCOM
5322 Oraga Place
Boise, ID 83706
PH: 208-336-6654
FAX: 208-338-9348

ILLINOIS
EAGLE TECHNICAL SALES
1805 Hicks Road, Suite G
Rolling Meadows, IL 60008
PH: 708-991-0700
FAX: 708-991-0714

INDIANA
ELECTRONIC SALES & ENG.
7739 E. 88th Street
P.O. Box 50009
Indianapolis, IN 46250
PH: 317-849-4260
FAX: 317-841-0231

KENTUCKY
ARTHUR BAIER COMPANY
7480 Kingswood Drive
P.O. Box 425
West Chester, OH 45069
PH: 513-779-2395
FAX: 513-779-9011

LOUISIANA
LOGIC 1 SALES, INC.
200 East Spring Valley
Suite A
Richardson, TX 75081
PH: 214-234-0765
FAX: 214-669-3042

SIERRA SEMICONDUCTOR NORTH AMERICAN SALES OFFICES (Cont.)

MAINE
NEW TECH SOLUTIONS
111 South Bedford Street, Ste. 102
Burlington, MA 01803
PH: 617-229-8888
FAX: 617-229-1614

MARYLAND
THIRD WAVE SOLUTIONS
8335 H Guilford Rd.
Columbia, MD 21046
PH: 301-290-5990
FAX: 301-381-5846

MASSACHUSETTS
NEW TECH SOLUTIONS
111 South Bedford Street, Ste. 102
Burlington, MA 01803
PH: 617-229-8888
FAX: 617-229-1614

MICHIGAN
TRITECH SALES INC.
32823 W. 12 Mile Rd., Ste. 110
Farmington Hills
Michigan, MI 48018
PH: 313-553-3370
FAX: 313-553-4670

MINNESOTA
P.S.I. COMPANY
7732 W. 78th Street
Minneapolis, MN 55435
PH: 612-944-8545
FAX: 612-944-6249

MISSISSIPPI
MONTGOMERY MKTG., INC.
1910 Sparkman Drive
Huntsville, AL 35816
PH: 205-830-0498
FAX: 205-837-7049

MONTANA
L-SQUARED LTD.
105 Central Way, Suite 203
Kirkland, WA 98033
PH: 206-827-8555
FAX: 206-828-6102

NEVADA
BROOKS TECHNICAL GROUP
883 N. Shoreline Blvd.
Mountain View, CA 94043
PH: 415-960-3880
FAX: 415-960-3615

NEVADA-LAS VEGAS SUMMIT SALES
7802 East Gray Road, Suite 600
Scottsdale, AZ 85260
PH: 602-998-4850
FAX: 602-998-5274

NEW HAMPSHIRE
NEW TECH SOLUTIONS
111 South Bedford Street, Ste. 102
Burlington, MA 01803
PH: 617-229-8888
FAX: 617-229-1614

NEW JERSEY
EMTEC SALES, INC.
299 Ridgedale Ave.
East Hanover, NJ 07936
PH: 201-428-0600
FAX: 201-428-9594

THE McCOY GROUP, INC.
291 B-1 Chester Avenue
Medford, NJ 08055
PH: 609-953-0770
FAX: 609-953-1238

NEW MEXICO SUMMIT SALES
7704 Ranchwood Dr. N.W.
Albuquerque, NM 87120
PH: 505-345-5003
FAX: 505-839-4057

NEW YORK
Upstate
PITRONICS, INC.
Pickard Bldg, Office 110
5858 Molloy Road
Syracuse, NY 13211
PH: 315-455-7346
FAX: 315-455-2630

Long Island
EMTEC SALES, INC.
299 Ridgedale Ave.
East Hanover, NJ 07936
PH: 201-428-0600
FAX: 201-428-9594

NORTH CAROLINA
MONTGOMERY MKTG., INC.
1391 N. Harrison Ave.
Cary, NC 27513
PH: 919-467-6319
FAX: 919-467-1028

MONTGOMERY MKTG., INC.
1200 Trinity Road
Raleigh, NC 27607
PH: 919-851-0010
FAX: 919-851-6620

NORTH DAKOTA
P.S.I. COMPANY
7732 W. 78th Street
Minneapolis, MN 55435
PH: 612-944-8545
FAX: 612-944-6249

OHIO
ARTHUR BAIER COMPANY
6690 Beta Drive, Suite 106
Cleveland, OH 44143
PH: 216-461-6161
FAX: 216-461-9091

ARTHUR BAIER COMPANY
7480 Kingswood Drive
P.O. Box 425
West Chester, OH 45069
PH: 513-779-2395
FAX: 513-779-9011

ARTHUR BAIER COMPANY
7395 Mapleleaf Blvd
Worthington, OH 43235
PH: 614-764-1144
FAX: 614-764-1157

ARTHUR BAIER COMPANY
2105 Needmore Road
Dayton, OH 45414
PH: 513-276-4128
FAX: 513-276-5486

OKLAHOMA
LOGIC 1 SALES, INC.
200 E. Spring Valley, Suite B
Richardson, TX 75081
PH: 214-234-0765
FAX: 214-669-3042

OREGON
L-SQUARED LTD.
15234 N.W. Greenbrier Pkwy.
Beaverton, OR 97006
PH: 503-629-8555
FAX: 503-645-6196

PENNSYLVANIA
Western Penn.
ARTHUR BAIER COMPANY
1230 Duncan Avenue
Pittsburgh, PA 15237
PH: 412-367-7799
FAX: 412-367-7073

Eastern Penn.
THE McCOY GROUP, INC.
P.O. Box 326
Exton, PA 19341
PH: 215-363-0350
FAX: 609-953-1238

PUERTO RICO
G.A. ASSOCIATES, INC.
Calle Fresa No. 35, Milaville
Rio Piedras, PR 00925
PH: 809-790-4090
FAX: 809-764-2060

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FAX: 716-381-9495

PHASE 1 TECHNOLOGY CORP
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N. Lindenhurst, NY 11757
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Edmonton, Alta T6E 5P3
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FAX: 403-458-4983

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300 North Rivermede Rd.
Concord, Ontario L4K 2Z4
PH: 416-736-1144
FAX: 416-736-4831

SIERRA SEMICONDUCTOR EUROPEAN SALES OFFICES

European Corporate Headquarters
SIERRA SEMICONDUCTOR B.V.
Bruistensingel 242
5232 AD s' -Hertogenbosch
The Netherlands
PN: 011-31-73-408888
FAX: 011-31-73-423155

NOTE: Design Center located at European Headquarters

Northern Europe Area Office
SIERRA SEMICONDUCTOR LTD.
Terminal 3-382
382 Stonehill Green, Westlea,
Swindon, SN5 7HB
England
PH: 011-44-793-618492
FAX: 011-44-793-618589

Central Europe Area Office
SIERRA SEMICONDUCTOR GmbH
Arabella Strasse 5
8000 Muenchen 81
Federal Republic of Germany
PH: 011-49-89-9101088
FAX: 011-49-89-9102232
Telex: 5216193

Southern Europe Area Office
SIERRA SEMICONDUCTOR SRL
Piazza de Angeli 1
20146 Milano
Italy
PH: 011-39-2-4819212/222
FAX: 011-39-2-4819197

BELGIUM
INELCO ELECTRONICS S.A.
Avenue des Croix de Guerre, 94
1120 Bruxelles
Belgium
PH: 011-32-2-2442811
FAX: 011-32-2-2164606

DENMARK
EXATEC A/S
Dortheavej 1-3
DK-2400 Copenhagen
Denmark
PH: 011-45-31-191022
FAX: 011-45-31-193129

FINLAND
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Heikkilantie 2A
00210 Helsinki
Finland
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France
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94588 Rungis Cedex
France
PH: 011-33-1-45-60-0021
FAX: 011-33-1-45-60-0186

GERMANY
BEKA ELECTRONIC GmbH
Industriestrasse 39-43
2000 Wedel
Federal Republic of Germany
PH: 011-49-4103-84061
FAX: 011-49-4103-15111
Telex: 189582

GERMANY (Cont.)
VSC ELECTRONIK VERTRIEBS GmbH
Gewerbestrasse 8
D-7049 Steinenbronn
Federal Republic of Germany
PH: 011-49-7157-4057
FAX: 011-49-7157-72607

ELECTRONIK GmbH
Zum Degenhardt 12
7770 Ueberlingen
DDR/East Europa
PH: 011-49-7024-8868-69
FAX: 011-49-7551-8008-34

BODAMER GmbH
Sudl. Muencher Strausse 24a
D-8022 Gruenwald
Federal Republic of Germany
PH: 011-49-4103-84061
FAX: 011-49-4103-15111
Telex: 189582

ITALY
INTER-REP (SPA HEADQUARTERS)
Centro-Direz Colleoni
17, Palazzo Orione-Ingresso 3
20041 Agrate B. Milano
Italy
PH: 011-39-6056171
FAX: 011-39-6050364

INTER-REP S.P.A.
Via Orbetello 98
10148 Torino
Italy
PH: 011-39-11-216-5901
FAX: 011-39-11-216-5915

THE NETHERLANDS
SEMICON B.V.
Gulberg 33
5674 AG Nuenen
The Netherlands
PH: 31-40-83-7075
FAX: 31-40-83-2300

NORWAY
NORDISK ELEKTRONIK A/S
Smedsvigen 4
P.O. Box 123
N-1364 Hvalstad
Norway
PH: 011-47-2-846210
FAX: 011-47-2-846545

SPAIN
CIOCE (SA HEADQUARTERS)
Numancia, 117-121
Local 1Y2
Planta 1
08029 Barcelona
Spain
PH: 011-34-3-3228052
FAX: 011-34-3-3215210
Telex: 50089

CIOCE S.A.
C/ San Sotero 8
Planta 3a
Madrid 28037
Spain
PH: 011-34-1-3271866
FAX: 011-34-1-3270848
Telex: 44476

SWEDEN
NORDISK ELEKTRONIK AB
Torshamnsgatan 39
P.O. Box 36
S-16493 Krista
Sweden
PH: 011-46-8-703-4630
FAX: 011-46-8-703-9845

SWITZERLAND
ASCOM PRIMOTEC AG
Taefernstrasse 37
CH 5405 Baden-Daettwil
Switzerland
PH: 011-41-56-84-0171
FAX: 011-41-56-83-3454
Telex: 58949

UNITED KINGDOM
AMEGA ELECTRONICS LTD.
Armstrong Rd.
Daneshill East
Basingstroke, Hants RG24 OPF
United Kingdom
PH: 011-44-256-843166
FAX: 011-44-256-842956

SIERRA SEMICONDUCTOR INTERNATIONAL SALES OFFICES

NOTE: Design Center located at Chartered Semiconductor, PTE, LTD, Singapore Science Park

AUSTRALIA

ADVANCED COMPONENT DIST.
106 Belmore Road North
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Australia
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FAX: 011-61-2-534-4910

REPTECHNIC
3/36 Bydown St.
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Australia
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India
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CHARTERED SEMI. PTE LTD.
No. 2 Science Park Drive
Singapore Science Park
Singapore 0511
PH: 011-65-777-773
FAX: 011-65-777-1933

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FAX: 011-65-778-9568

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Taipei 10479
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In the U.S. — **SIERRA SEMICONDUCTOR CORPORATION,** 2075 North Capitol Avenue, San Jose, CA 95132.
Telephone (408) 263-9300. Telex 384467. Fax (408) 263-3337.

In Europe — **SIERRA SEMICONDUCTOR B.V.,** Bruistensingel 242, 5232 AD 's-Hertogenbosch, The Netherlands.
Telephone 073-408485. Telex 50050. Fax 073-423557.

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