EPROM AND FLASH MEMORY PRODUCTS

DATABOOK

1st EDITION

SGS-THOMSON MICROELECTRONICS

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JUNE 1995

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED 489

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

INTRODUCTION

SGS-THOMSON Microelectronics is a broad range semiconductor company. The product range includes memory products which satisfy the needs of a wide range of applications. They include

- Non-Volatile Memories: OTP Memories, UV EPROMs, FLASH Memories, Serial and Parallel EEPROMs and NVRAMs (battery backed SRAMs)
- Synchronous and Asynchronous Fast SRAMs

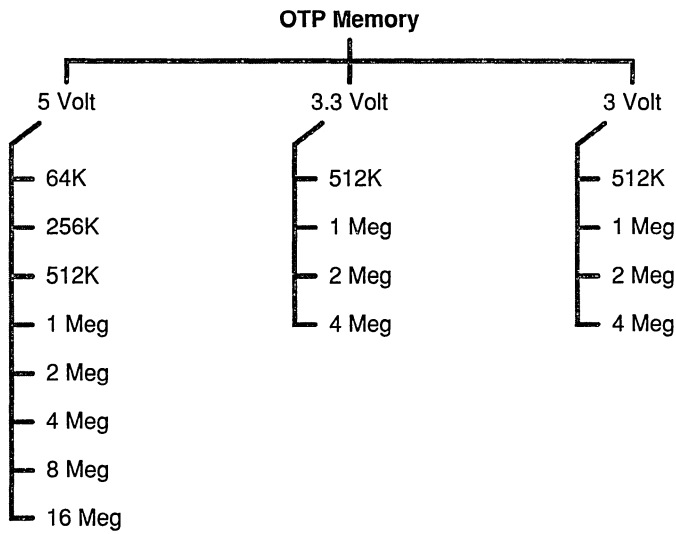
This databook provides comprehensive technical information on the OTP Memory, UV EPROM and FLASH Memory products.

OTP Memories (One Time Programmable Memories).

These devices are in many ways similar to UV EPROMs but are packaged in plastic packages, including both through hole mounting, Dual-In-Line Packages and surface mounting types. The surface mounting types include both the PLCC (Plastic Leaded Chip Carrier) and the TSOP (Thin Small Outline Package).

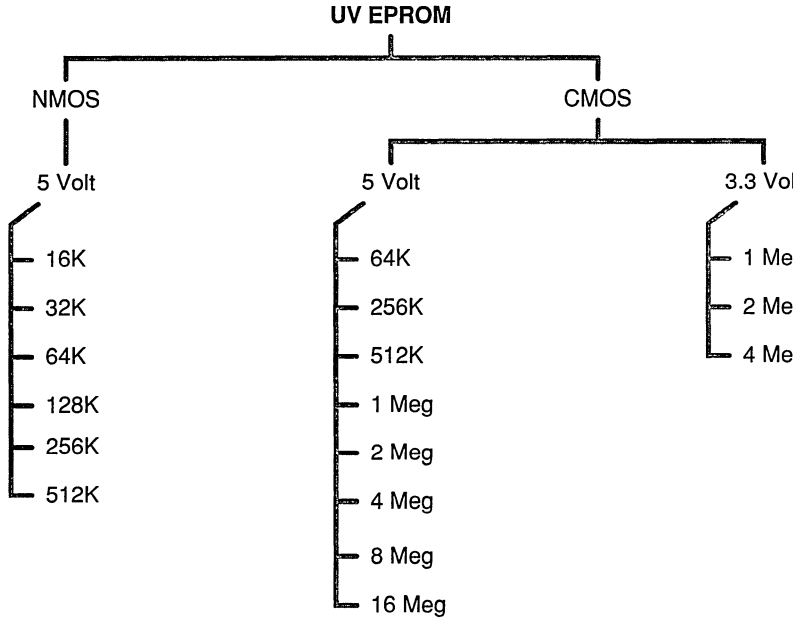
OTP Memories are not eraseable, but are programed one time only using the same programming techniques as for UV EPROMs. Memory densities range from 64K to 8 Megabits using modern CMOS technologies. New technologies allow operation down to supply voltages as low as 2.7 Volts, suitable for battery powered, portable applications.

OTP Memories often can be used to replace FLASH Memories, giving a significant saving in costs, when the memory content is stable and not likely to need re-programing during the system life. Like FLASH they offer the advantage over Mask ROMs of having their content programed at the final moment of equipment assembly, rather than weeks beforehand.



UV EPROMs (UV light eraseable Electrically Programmable Read Only Memories).

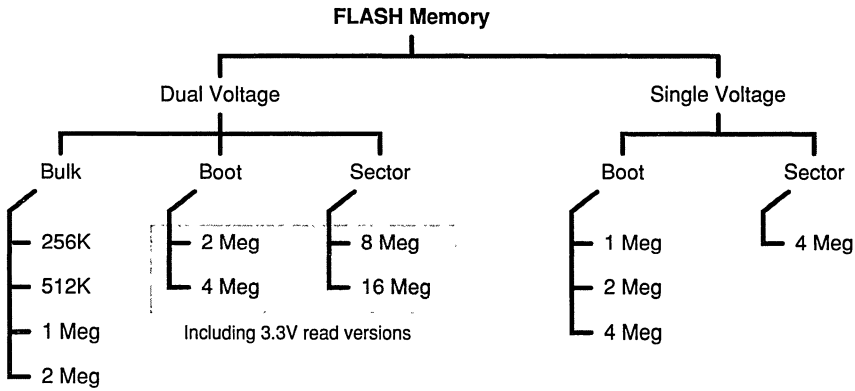
This is a family of EPROMs which can be electrically programed and erased by exposure to UV light through a quartz window in the package. SGS-THOMSON supports both the older NMOS ranges from 16K through 512K bits and the most modern CMOS technologies with products from 64K to 16 Megabit.



FLASH Memories (Electrically programmable and eraseable memories).

The FLASH Memory provides a new flexibility for the system designer by implementing both electrical programming, like the EPROM, and electrical erase. Erasure is in bulk, for the whole chip, or in blocks or sectors.

The FLASH Memory can be erased and re-programed in the equipment and finds applications wherever there is a requirement to change the contents of the non-volatile memory.



SGS-THOMSON has an extensive program of both process R & D and product design which results in many new products updates and introductions every year.

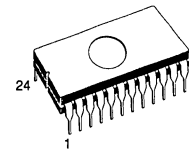
Please contact your nearest Sales Office to learn about new products that have been introduced since this databook was published.

GENERAL INDEX

NMOS UV EPROM

NMOS 16K (2K x 8) UV EPROM

- 2048 x 8 ORGANIZATION
- 525mW Max ACTIVE POWER, 132mW Max STANDBY POWER
- ACCESS TIME:
  - M2716-1 is 350ns
  - M2716 is 450ns
- SINGLE 5V SUPPLY VOLTAGE
- STATIC-NO CLOCKS REQUIRED
- INPUTS and OUTPUTS TTL COMPATIBLE DURING BOTH READ and PROGRAM MODES
- THREE-STATE OUTPUT with TIED-OR-CAPABILITY
- EXTENDED TEMPERATURE RANGE
- PROGRAMMING VOLTAGE: 25V



FDIP24W (F)

DESCRIPTION

The M2716 is a 16,384 bit UV erasable and electrically programmable memory EPROM, ideally suited for applications where fast turn around and pattern experimentation are important requirements.

The M2716 is housed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

A0 - A10	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}P$	Chip Enable / Program
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

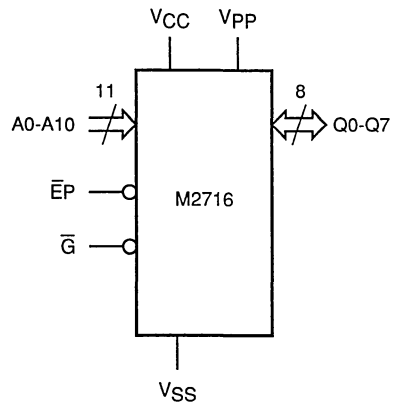
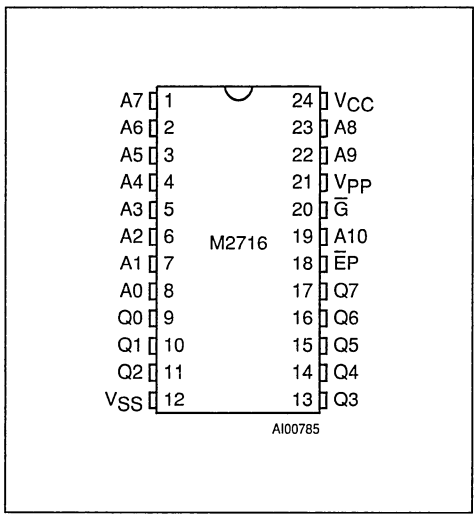


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{CC}	Supply Voltage		–0.3 to 6	V
V_{IO}	Input or Output Voltages		–0.3 to 6	V
V_{PP}	Program Supply		–0.3 to 26.5	V
P_D	Power Dissipation		1.5	W

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The M2716 has 3 modes of operation in the normal system environment. These are shown in Table 3.

Read Mode. The M2716 read operation requires that $\overline{G}$ = V_{IL}, $\overline{EP}$ = V_{IL} and that addresses A0-A10 have been stabilized. Valid data will appear on the output pins after time t_{AVQV}, t_{GLQV} or t_{ELQV} (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode. The M2716 is deselected by making $\overline{G}$ = V_{IH}. This mode is independent of $\overline{EP}$ and the condition of the addresses. The outputs are Hi-Z when $\overline{G}$ = V_{IH}. This allows tied-OR of 2 or more M2716's for memory expansion.

Standby Mode (Power Down). The M2716 may be powered down to the standby mode by making $\overline{EP}$ = V_{IH}. This is independent of $\overline{G}$ and automatically puts the outputs in the Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. V_{CC} and V_{PP} must be maintained at 5V. Access time at power up remains either t_{AVQV} or t_{ELQV} (see Switching Time Waveforms).

Programming

The M2716 is shipped from SGS-THOMSON completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table 3 shows the 3 programming modes.

Program Mode. The M2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, sequential addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the $\overline{EP}$ pin. All input voltage levels including the program pulse on chip enable are TTL compatible.

The programming sequence is: with V_{PP} = 25V, V_{CC} = 5V, $\overline{G}$ = V_{IH} and $\overline{EP}$ = V_{IL}, an address is selected and the desired data word is applied to the output pins (V_{IL} = "0" and V_{IH} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a

DEVICE OPERATION (cont'd)

pulse width between 45ms and 55ms. Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) must not be maintained longer than t_{PHPL} (max) on the program pin during programming. M2716's may be programmed in parallel in this mode.

Program Verify Mode. The programming of the M2716 may be verified either one byte at a time during the programming (as shown in Figure 6) or by reading all of the bytes out at the end of the programming sequence. This can be done with V_{PP} = 25V or 5V in either case. V_{PP} must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

Program Inhibit Mode. The program inhibit mode allows several M2716's to be programmed simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the M2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{G}$ = V_{IH} will put its outputs in the Hi-Z state.

ERASURE OPERATION

The M2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm^2 power rating is used. The M2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age, it is therefore important to periodically check that the UV system is in good order.

This will ensure that the EPROMs are being completely erased. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

Table 3. Operating Modes

Mode	$\overline{EP}$	$\overline{G}$	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IH} Pulse	V_{IH}	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{PP} or V_{CC}	Data Out
Program Inhibit	V_{IL}	V_{IH}	V_{PP}	Hi-Z
Deselect	X	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Note: X = V_{IH} or V_{IL}.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

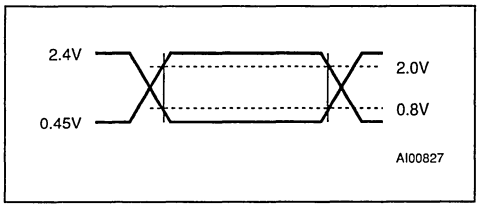


Figure 4. AC Testing Load Circuit

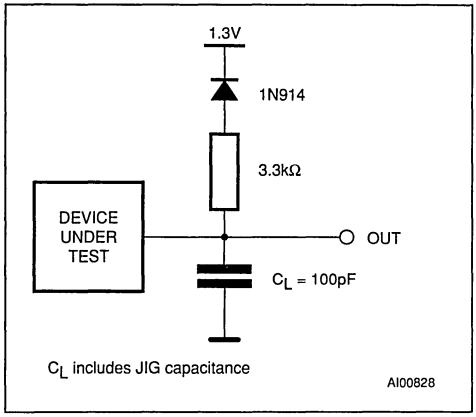


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$, $\overline{E}P = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E}P = V_{IL}$, $\overline{G} = V_{IL}$		100	mA
I_{CC1}	Supply Current (Standby)	$\overline{E}P = V_{IH}$, $\overline{G} = V_{IL}$		25	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 6. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2716				Unit
				-1		blank		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}P$ = V_{IL}, $\overline{G}$ = V_{IL}		350		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		350		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}P$ = V_{IL}		120		120	ns
t_{EHQZ} (2)	t_{OD}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	100	0	100	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}P$ = V_{IL}	0	100	0	100	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}P$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

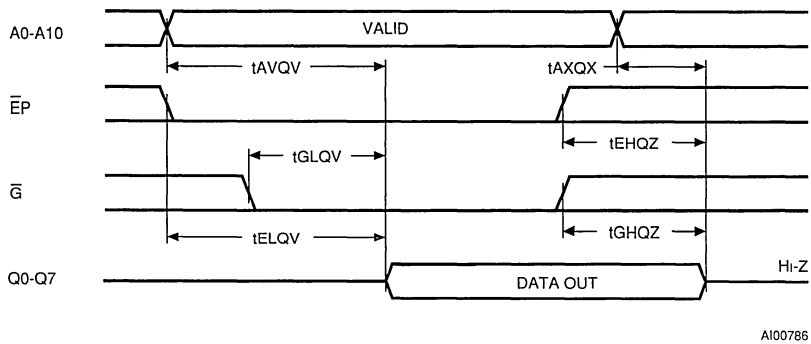


Table 7. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 25V ± 1V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current			5	mA
I_{PP1}	Program Current Pulse	$\overline{E}P$ = V_{IH} Pulse		30	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V

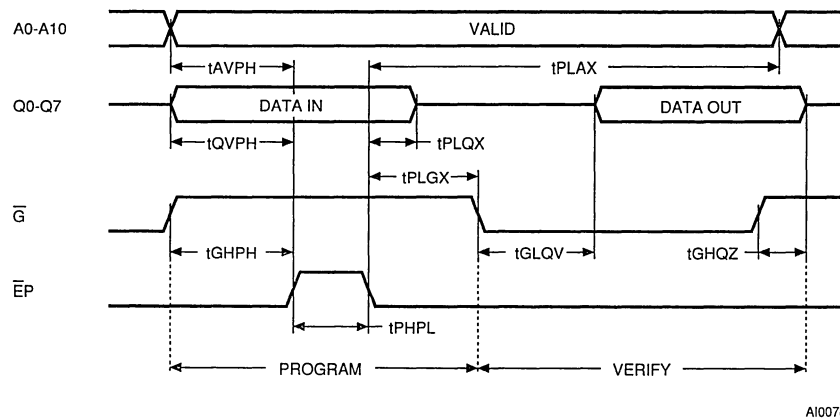
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 8. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 25V ± 1V)

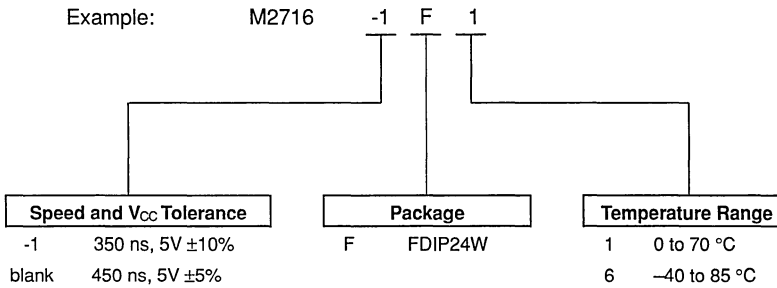
Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVPH}	t_{AS}	Address Valid to Program High	$\overline{G}$ = V_{IH}	2		µs
t_{QVPH}	t_{DS}	Input Valid to Program High	$\overline{G}$ = V_{IH}	2		µs
t_{GHPH}	t_{OS}	Output Enable High to Program High		2		µs
t_{PL1PL2}	t_{PR}	Program Pulse Rise Time		5		ns
t_{PH1PH2}	t_{PF}	Program Pulse Fall Time		5		ns
t_{PHPL}	t_{PW}	Program Pulse Width		45	55	ms
t_{PLQX}	t_{DH}	Program Low to Input Transition		2		µs
t_{PLGX}	t_{OH}	Program Low to Output Enable Transition		2		µs
t_{GLQV}	t_{OE}	Output Enable to Output Valid	$\overline{EP}$ = V_{IL}		120	ns
t_{GHQZ}	t_{DF}	Output Enable High to Output Hi-Z		0	100	ns
t_{PLAX}	t_{AH}	Program Low to Address Transition		2		µs

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



ORDERING INFORMATION SCHEME



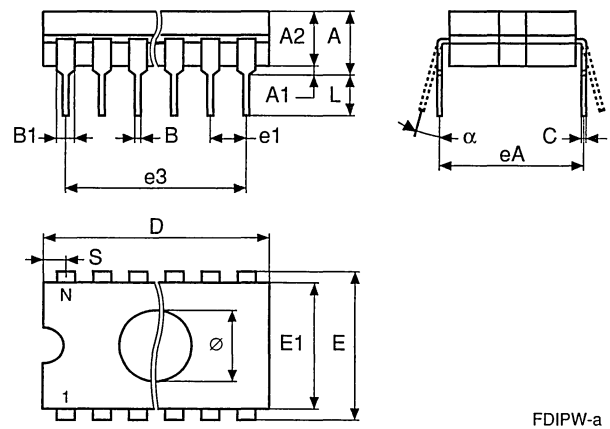
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP24W - 24 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			32.30			1.272
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	27.94	–	–	1.100	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N	24			24		

FDIP24W

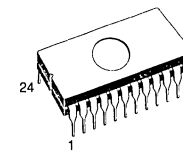


FDIPW-a

Drawing is out of scale

NMOS 32K (4K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- INPUTS and OUTPUTS TTL COMPATIBLE DURING READ and PROGRAM
- COMPLETELY STATIC



FDIP24W (F)

DESCRIPTION

The M2732A is a 32,768 bit UV erasable and electrically programmable memory EPROM. It is organized as 4,096 words by 8 bits. The M2732A with its single 5V power supply and with an access time of 200 ns, is ideal suited for applications where fast turn around and pattern experimentation one important requirements.

The M2732A is honsed in a 24 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can be then written to the clerice by following the programming procedure.

Figure 1. Logic Diagram

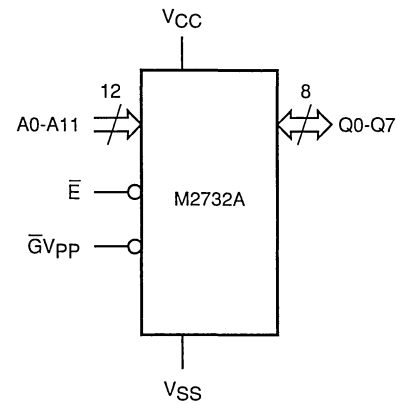


Table 1. Signal Names

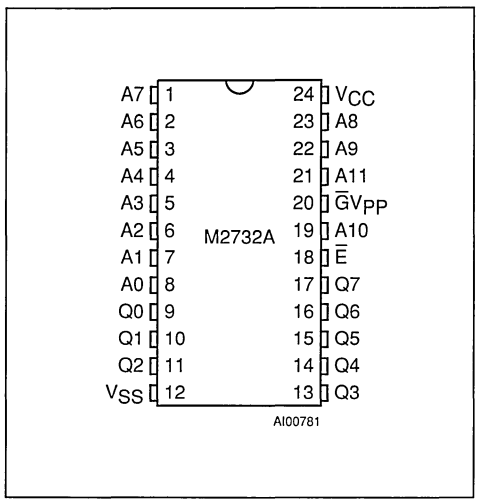
A0 - A11	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6	V
V_{CC}	Supply Voltage		–0.6 to 6	V
V_{PP}	Program Supply Voltage		–0.6 to 22	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

Figure 2. DIP Pin Connections



DEVICE OPERATION

The six modes of operation for the M2732A are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL level except for V_{PP}.

Read Mode

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVAQ}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M2732A has a standby mode which reduces the active power current by 70 %, from 125 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to $\overline{E}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{G}/V_{PP}$ input.

Two Line Output Control

Because M2732A's are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{E}$ be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Programming

When delivered, and after each erasure, all bits of the M2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2732A is in the programming mode when the $\overline{G}V_{PP}$ input is at 21V. A 0.1µF capacitor must be placed across $\overline{G}V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50ms, active low, TTL program pulse is applied to the $\overline{E}$ input. A program pulse must be applied at each address location to be programmed. Any location can be programmed at any time - either individually, sequentially, or at random. The program pulse has a maximum width of 55ms. The M2732A must not be programmed with a DC signal applied to the $\overline{E}$ input.

Programming of multiple M2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{E}$ input programs the paralleled 2732As.

Program Inhibit

Programming of multiple M2732As in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}V_{PP}$) of the parallel M2732As may be common. A TTL level program pulse applied to a M2732A's $\overline{E}$ input with $\overline{G}V_{PP}$ at 21V will program that M2732A. A high level $\overline{E}$ input inhibits the other M2732As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is carried out with $\overline{G}V_{PP}$ and $\overline{E}$ at V_{IL}.

ERASURE OPERATION

The erasure characteristics of the M2732A are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to the direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2732A window to prevent unintentional erasure.

The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M2732A should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	V_{CC}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{CC}	Data Out
Program	V_{IL} Pulse	V_{PP}	V_{CC}	Data In
Verify	V_{IL}	V_{IL}	V_{CC}	Data Out
Program Inhibit	V_{IH}	V_{PP}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Note: X = V_{IH} or V_{IL}.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

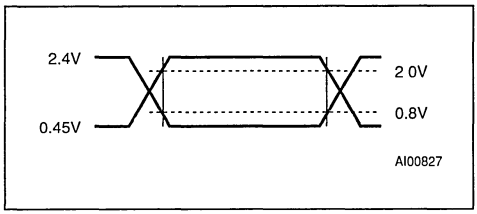


Figure 4. AC Testing Load Circuit

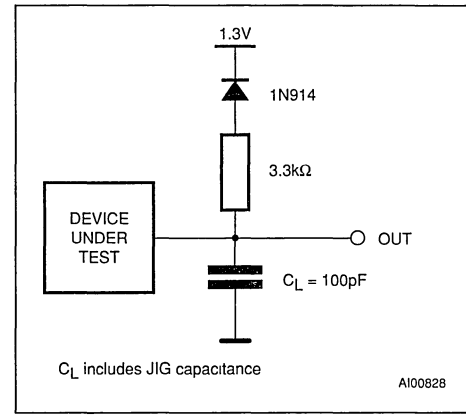


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except $\overline{G}V_{PP}$)	V_{IN} = 0V		6	pF
C_{IN1}	Input Capacitance ($\overline{G}V_{PP}$)	V_{IN} = 0V		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

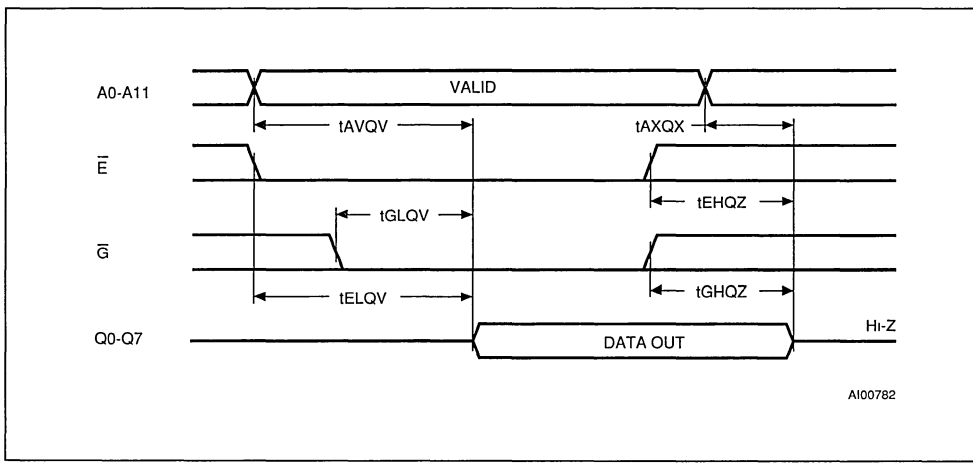


Table 5. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Value		Unit
			Min	Max	
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$, $\overline{G} = V_{IL}$		35	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 6. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2732A								Unit
				-2, -20		blank, -25		-3		-4		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		100		100		150		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	60	0	60	0	130	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	60	0	60	0	130	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Table 7. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 21V ± 0.5V)

Symbol	Parameter	Test Condition	Min	Max	Units
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$		30	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

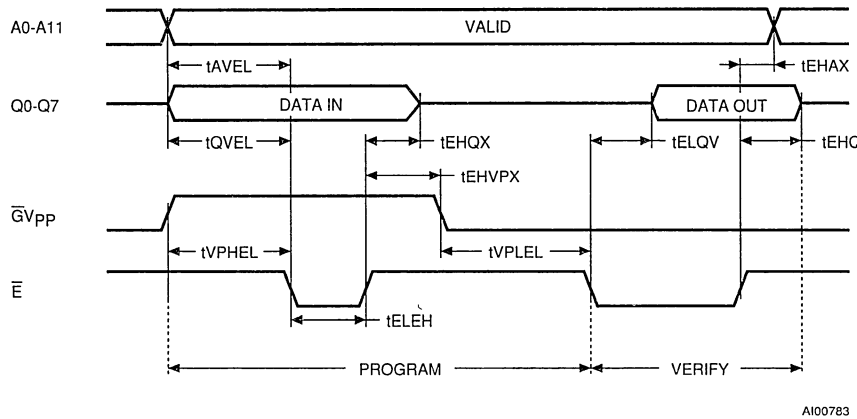
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Table 8. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 5V ± 5%; V_{PP} = 21V ± 0.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
$t_{VPL1VPL2}$	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		45	55	ms
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		1	µs
t_{EHQZ}	t_{DF}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Figure 6. Programming and Verify Modes AC Waveforms



ORDERING INFORMATION SCHEME

Example: M2732A -2 F 1

Speed and V_{CC} Tolerance		Package		Temperature Range	
-2	200 ns, 5V ±5%	F	FDIP24W	1	0 to 70 °C
blank	250 ns, 5V ±5%			6	–40 to 85 °C
-3	300 ns, 5V ±5%				
-4	450 ns, 5V ±5%				
-20	200 ns, 5V ±10%				
-25	250 ns, 5V ±10%				

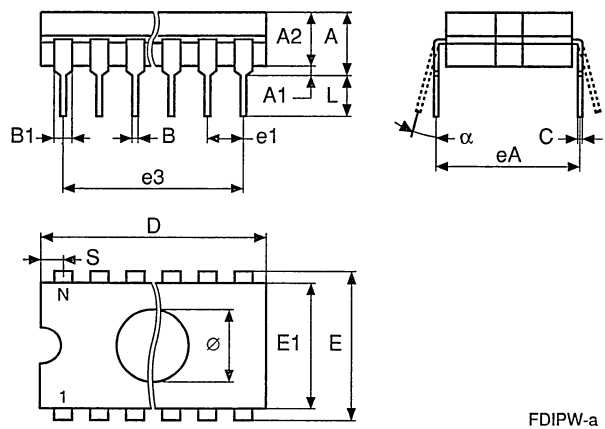
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP24W - 24 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			32.30			1.272
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	27.94	–	–	1.100	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N		24			24	

FDIP24W

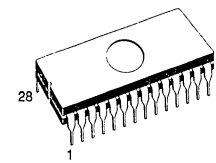


FDIPW-a

Drawing is out of scale

NMOS 64K (8K x 8) UV EPROM

- FAST ACCESS TIME: 180ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M2764A is a 65,536 bit UV erasable and electrically programmable memory EPROM. It is organized as 8,192 words by 8 bits.

The M27C64A is housed in a 28 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Figure 1. Logic Diagram

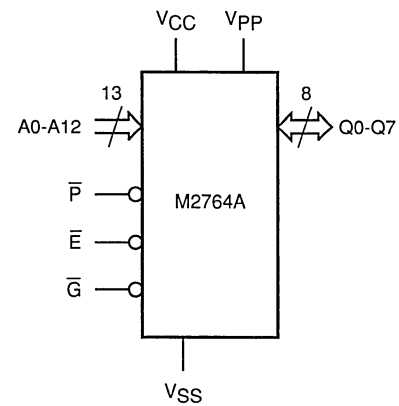


Table 1. Signal Names

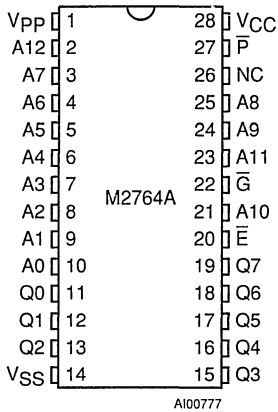
A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.6 to 6.5	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



Warning: NC = No Connection.

DEVICE OPERATION

The seven modes of operations of the M2764A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M2764A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M2764A has a standby mode which reduces the maximum active power current from 75mA to 35mA. The M2764A is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M2764A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2764A is in the programming mode when V_{PP} input is at 12.5V and $\overline{E}$ and $\overline{P}$ are at TTL low. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M2764A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes Out

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	1	0	0	0	08h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

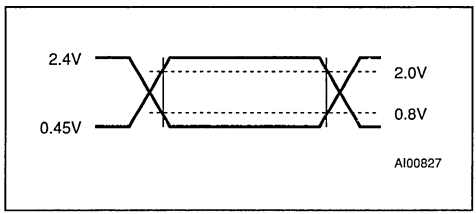


Figure 4. AC Testing Load Circuit

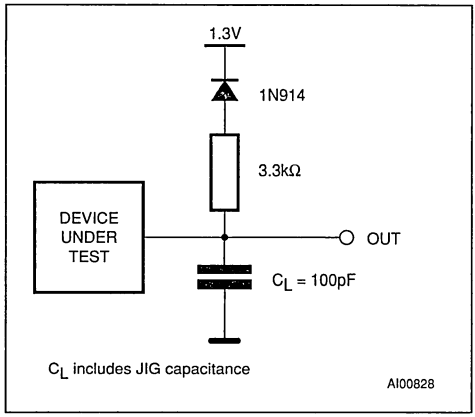


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

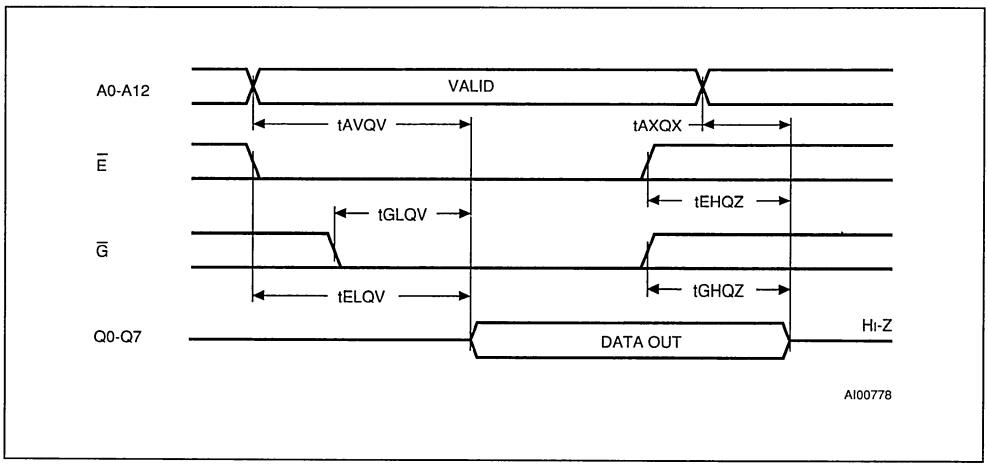


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		75	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		35	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2764A						Unit
				-1		-2, -20		blank, -25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		180		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		180		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		65		75		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	55	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	55	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M2764A				Unit
				-3		-4		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$,		120		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	105	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	105	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Units
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			75	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
VA9	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{PLPH}	t_{OPW}	Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			150	ns
t_{GHQZ} (4)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. The Initial Program Pulse width tolerance is 1 ms ± 5%.
3. The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending of the multiplication value of the iteration counter.
4. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

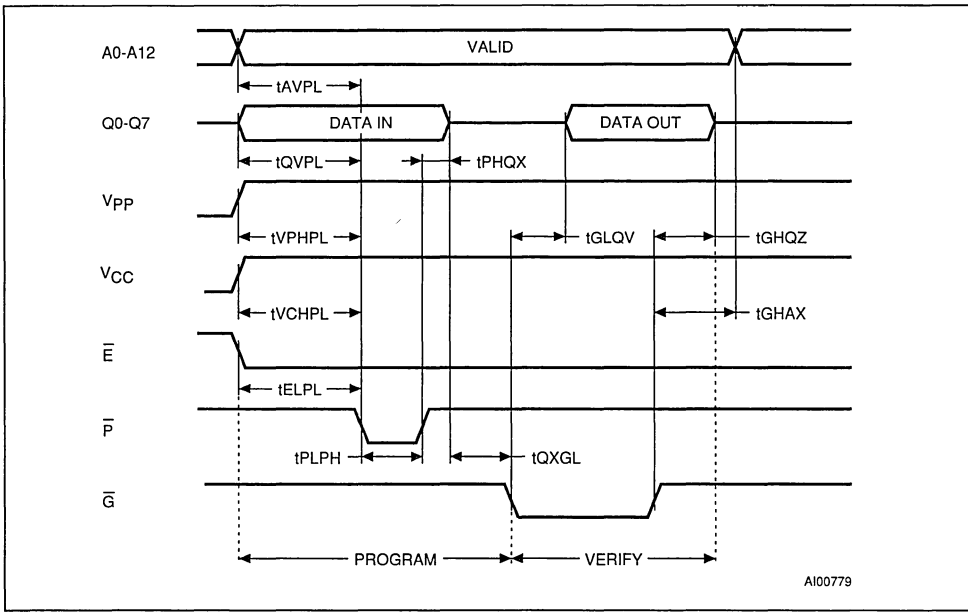
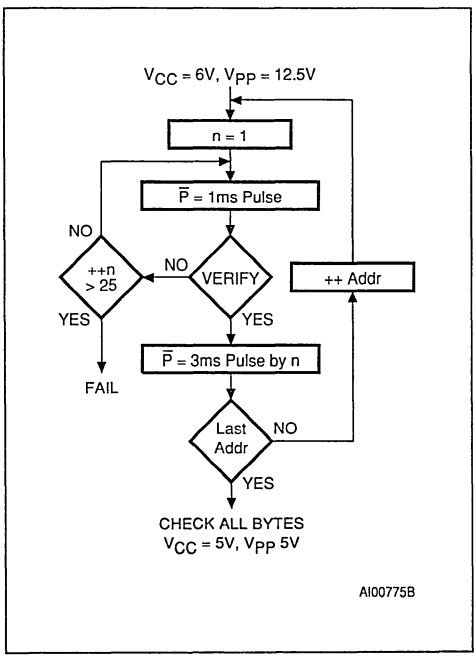


Figure 7. Fast Programming Flowchart



DEVICE OPERATION (cont'd)

been successfully programmed. A flowchart of the M2764A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program.

The duration of the initial $\overline{P}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ms by n (n is equal to the number of the initial one millisecond pulses applied to a particular M2764A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V and V_{PP} = 5V.

Program Inhibit

Programming of multiple M2764A in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}$) of the parallel M2764A may be common. A TTL low pulse applied to a M2764A's $\overline{E}$ input, with V_{PP} at 12.5V, will program that M2764A. A high level $\overline{E}$ input inhibits the other M2764As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, $\overline{P} = V_{IH}$ and $V_{PP} = 12.5V$.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M2764A.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M2764A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M2764A, these two identifier bytes are given below.

ERASURE OPERATION (applies to UV EPPROM)

The erasure characteristic of the M2764A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2764A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M2764A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2764A window to prevent unintentional erasure. The recommended erasure procedure for the M2764A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M2764A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M2764A -1 F 1

Speed and V_{CC} Tolerance		Package		Temperature Range	
-1	180 ns, 5V ±5%	F	FDIP28W	1	0 to 70 °
-2	200 ns, 5V ±5%			6	–40 to 85 °C
blank	250 ns, 5V ±5%				
-3	300 ns, 5V ±5%				
-4	450 ns, 5V ±5%				
-20	200 ns, 5V ±10%				
-25	250 ns, 5V ±10%				

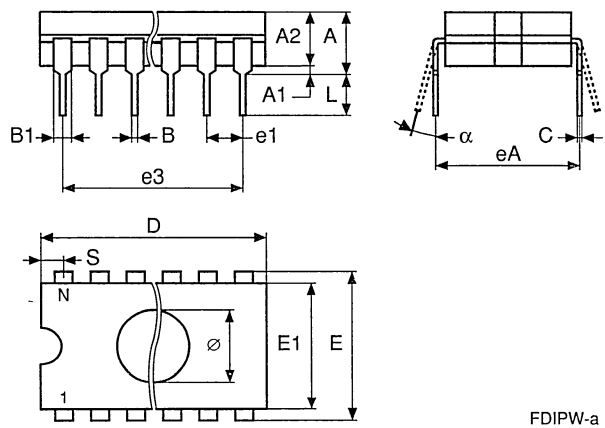
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP28W - 28 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	33.02	–	–	1.300	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N	28			28		

FDIP28W

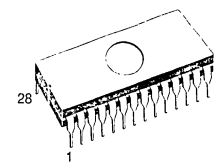


FDIPW-a

Drawing is out of scale

NMOS 128K (16K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5 V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M27128A is a 131,072 bit UV erasable and electrically programmable memory EPROM. It is organized as 16,384 words by 8 bits.

The M27128A is housed in a 28 Pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Figure 1. Logic Diagram

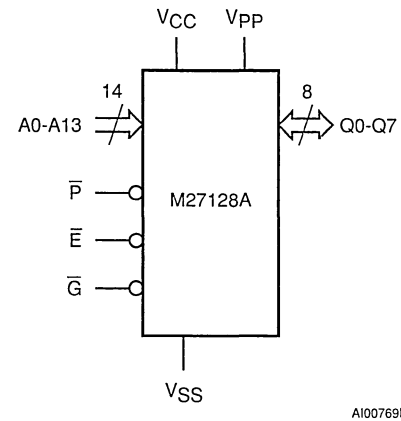


Table 1. Signal Names

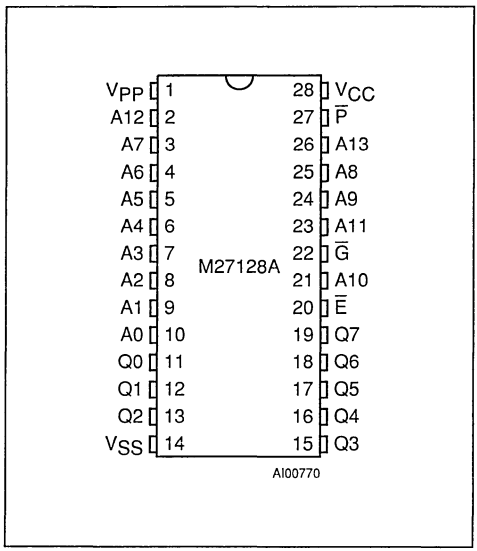
A0 - A13	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.25	V
V_{CC}	Supply Voltage		–0.6 to 6.25	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The seven modes of operation of the M27128A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27128A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27128A has a standby mode which reduces the maximum active power current from 85mA to 40mA. The M27128A is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPPROM), all bits of the M27128A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M27128A is in the programming mode when V_{PP} input is at 12.5V and $\overline{E}$ and $\overline{P}$ are at TTL low. The data to be programmed is applied 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27128A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes Out

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	0	0	1	89h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

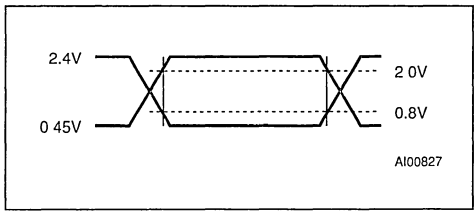


Figure 4. AC Testing Load Circuit

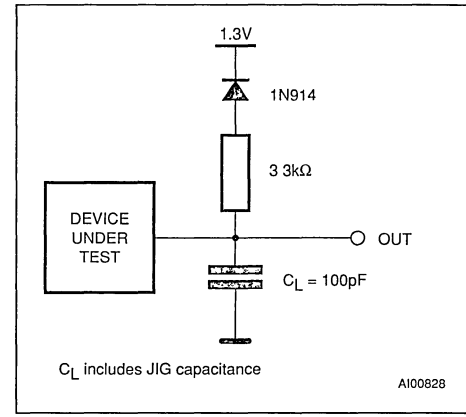


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	=	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	=	12	pF

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

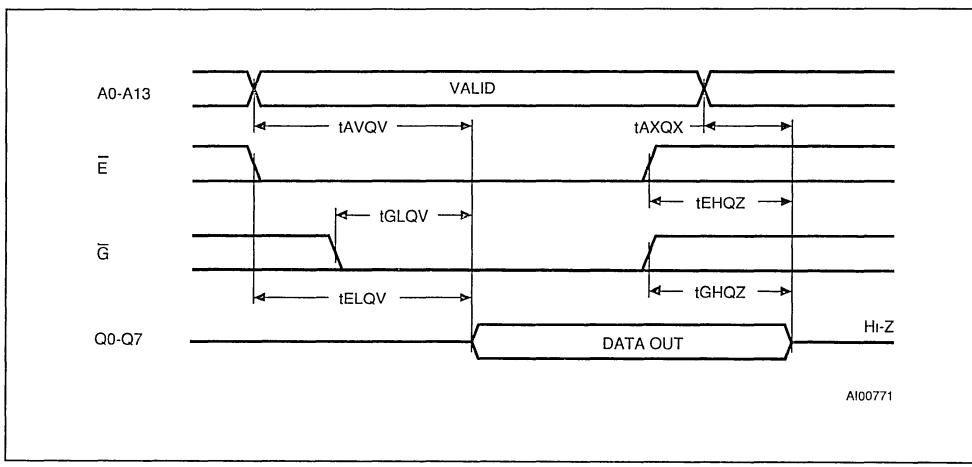


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		75	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		35	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	=	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27128A								Unit
				-2, -20		blank, -25		-3, -30		-4		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		200		250		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		200		250		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		75		100		120		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	0	105	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	55	0	60	0	105	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{PLPH}	t_{OPW}	Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			150	ns
t_{GHQZ} (4)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. The Initial Program Pulse width tolerance is 1 ms ± 5%
3 The length of the Over-program Pulse varies from 2.85 ms to 78 95 ms, depending on the multiplication value of the iteration counter.
4. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

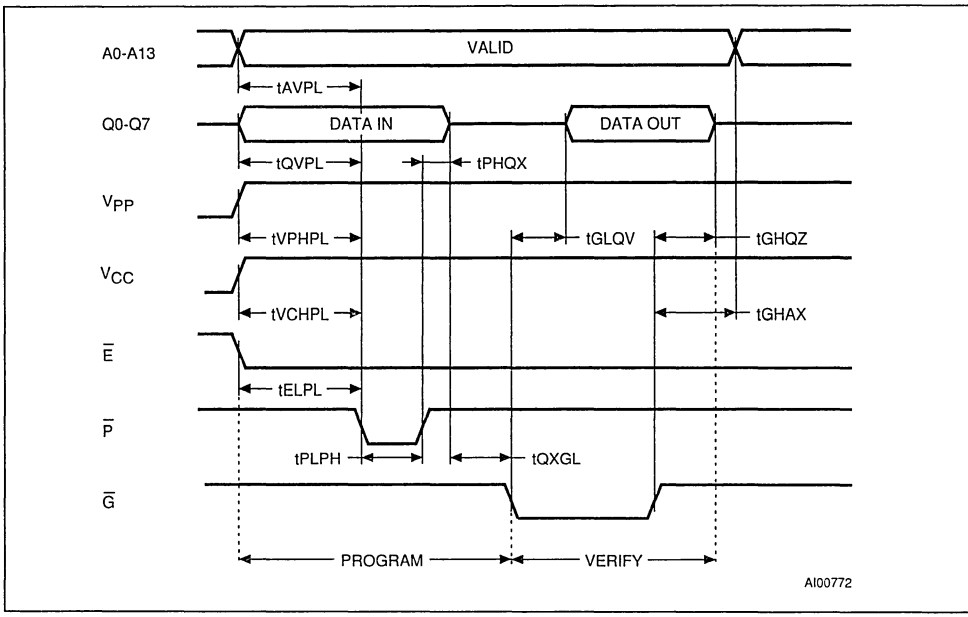
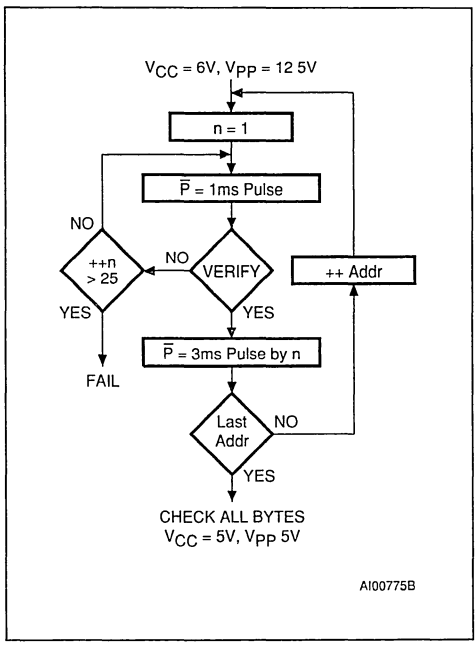


Figure 7. Programming Flowchart



DEVICE OPERATION (cont'd)

continually monitored to determine when it has been successfully programmed. A flowchart of the M27128A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program.

The duration of the initial $\overline{P}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ms by n (n is equal to the number of the initial one millisecond pulses applied to a particular M27128A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5 and V_{PP} = 5V.

Program Inhibit

Programming of multiple M27128A's in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}$) of the parallel M27128A may be common. A TTL low pulse applied to a M27128A's $\overline{E}$ input, with V_{PP} = 12.5V, will program that M27128A. A high level $\overline{E}$ input inhibits the other M27128As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, $\overline{P} = V_{IH}$ and V_{PP} at 12.5V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the25°C ± 5°C ambient temperature range that is required when programming the M27128A.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27128A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M27128A, these two identifier bytes are given below.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristic of the M27128A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27128A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27128A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27128A window to prevent unintentional erasure. The recommended erasure procedure for the M27128A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27128A should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27128A -2 F 1

Speed and V_{CC} Tolerance		Package		Temperature Range	
-2	200 ns, 5V ±5%	F	FDIP28W	1	0 to 70 °C
blank	250 ns, 5V ± 5%			6	–40 to 85 °C
-3	300 ns, 5V ± 5%				
-4	450 ns, 5V ± 5%				
-20	200 ns, 5V ± 10%				
-25	250 ns, 5V ± 10%				
-30	300 ns, 5V ± 10%				

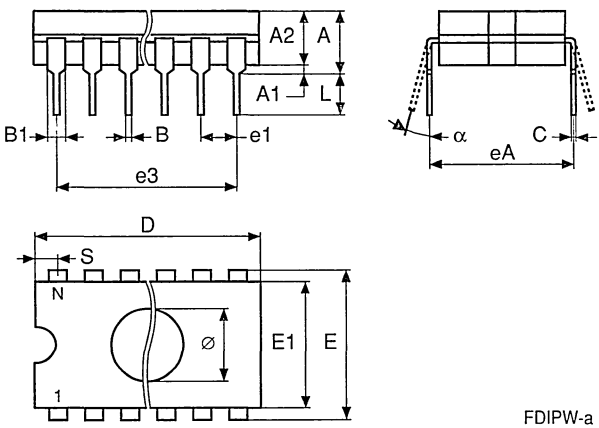
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP28W - 28 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	33.02	–	–	1.300	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
Ø	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N		28			28	

FDIP28W

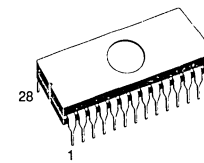


FDIPW-a

Drawing is out of scale

NMOS 256K (32K x 8) UV EPROM

- FAST ACCESS TIME: 170ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M27256 is a 262,144 bit UV erasable and electrically programmable memory EPROM. It is organized as 32.768 words by 8 bits.

The M27256 is housed in a 28 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Figure 1. Logic Diagram

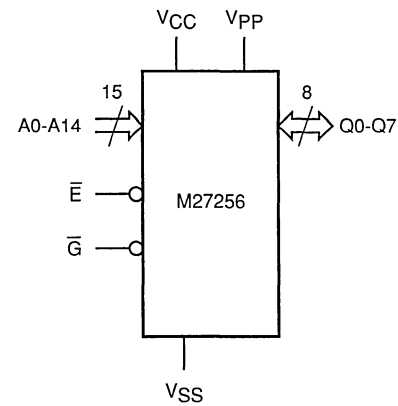


Table 1. Signal Names

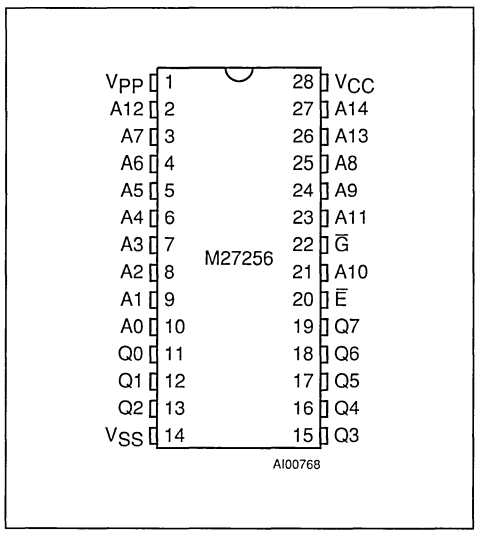
A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.25	V
V_{CC}	Supply Voltage		–0.6 to 6.25	V
V_{A9}	VA9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The eight modes of operations of the M27256 are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27256 has a standby mode which reduces the maximum active power current from 100mA to 40mA. The M27256 is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitors should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programmain

When delivered, (and after each erasure for UV EPROM), all bits of the M27256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27256 is in the programming mode when V_{PP} input is at 12.5V and $\overline{E}$ is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27256 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27256 Fast Programming Algorithm is shown on the Flowchart. The Fast Programming Algorithm utilizes two different pulse types : initial and over-program. The duration of the initial $\overline{E}$ pulse(s) is 1ms, which will then be followed by a longer over-program pulse of length 3ms by n (n is equal to the number of the initial one millisecond pulses applied

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Optional Verify	V_{IL}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

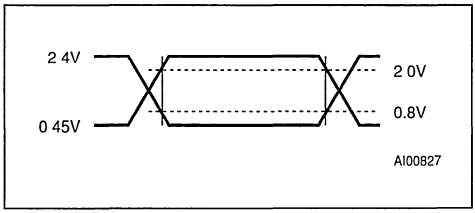


Figure 4. AC Testing Load Circuit

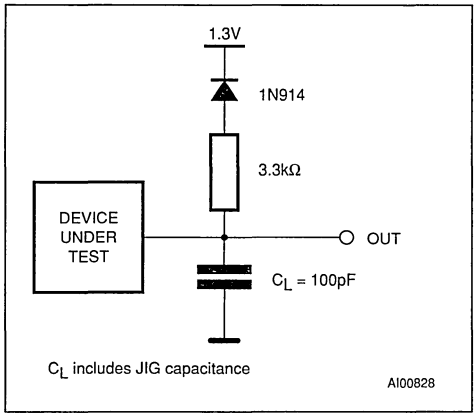


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

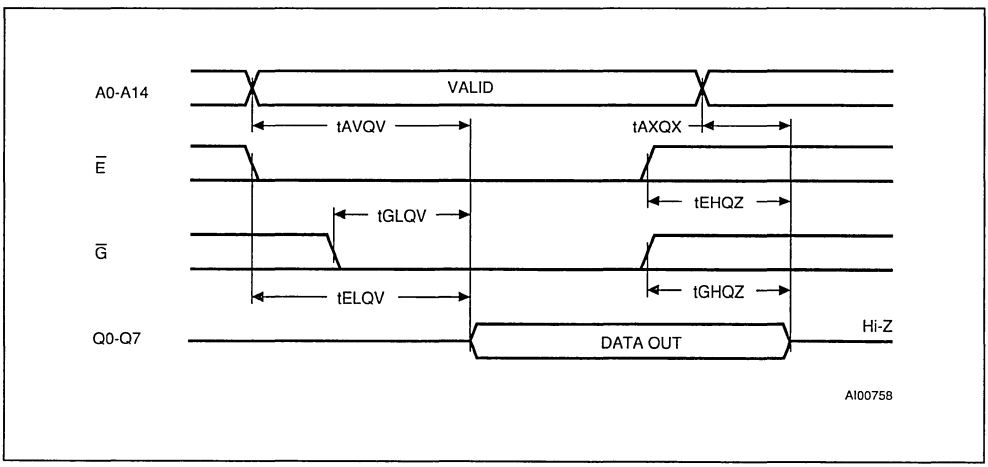


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		40	mA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		5	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27256						Unit
				-1		-2, -20		blank, -25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		170		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		170		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		70		75		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	35	0	55	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	35	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27256				Unit
				-3		-4		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		300		450	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		300		450	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$,		120		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	105	0	130	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	105	0	130	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			100	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{ELEH}	t_{OPW}	Chip Enable Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			150	ns
t_{GHQZ} (4)	t_{DFP}	Output Enable Low to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. The Initial Program Pulse width tolerance is 1 ms ± 5%
3. The length of the Over-program Pulse varies from 2 85 ms to 78.95 ms, depending on the multiplication value of the iteration counter
4 Sampled only, not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms

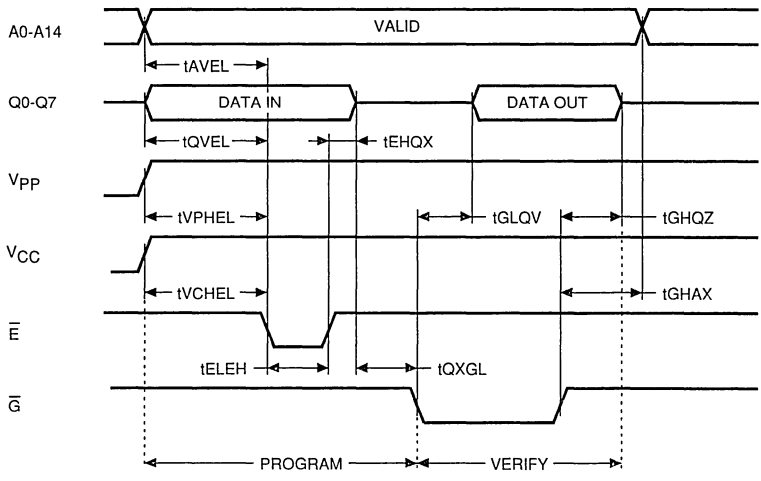
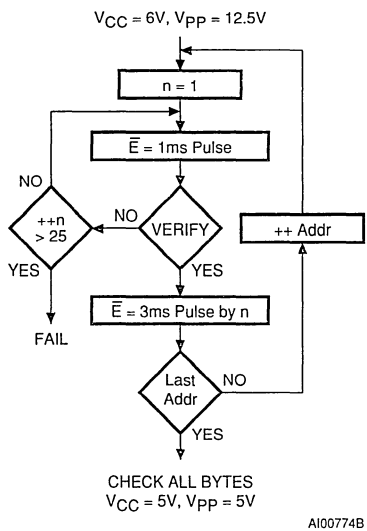


Figure 7. Programming Flowchart



DEVICE OPERATION (cont'd)

to a particular M27256 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V.

When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V and V_{PP} = 5V.

Program Inhibit

Programming of multiple M27256s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}$) of the parallel M27256 may be common. A TTL low pulse applied to a M27256's $\overline{E}$ input, with V_{PP} = 12.5V, will program that M27256. A high level $\overline{E}$ input inhibits the other M27256s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E} = V_{IH}$, $\overline{G} = V_{IL}$ and V_{PP} = 12.5V.

Optional Verify

The optional verify may be performed instead of the verify mode. It is performed with $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$ (as opposed to the standard verify which has $\overline{E}$ =

DEVICE OPERATION (cont'd)

V_{IH}), and V_{PP} = 12.5V. The outputs will be in a Hi-z state according to the signal presented to $\overline{G}$. Therefore, all devices with V_{PP} = 12.5V and $\overline{G}$ = V_{IL} will present data on the bus independent of the $\overline{E}$ state. When parallel programming several devices which share the common bus, V_{PP} should be lowered to V_{CC} (6V) and the normal read mode used to execute a program verify.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27256. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M27256, these two identifier bytes are given below.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristic of the M27256 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27256 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27256 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque lables be put over the M27256 window to prevent unintentional erasure. The recommended erasure procedure for the M27256 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27256 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27256 -1 F 1

Speed and V_{CC} Tolerance		Package		Temperature Range	
-1	170 ns, 5V ±5%	F	FDIP28W	1	0 to 70 °C
-2	200 ns, 5V ±5%			6	–40 to 85 °C
blank	250 ns, 5V ±5%				
-3	300 ns, 5V ±5%				
-4	400 ns, 5V ±5%				
-20	200 ns, 5V ±10%				
-25	250 ns, 5V ±10%				

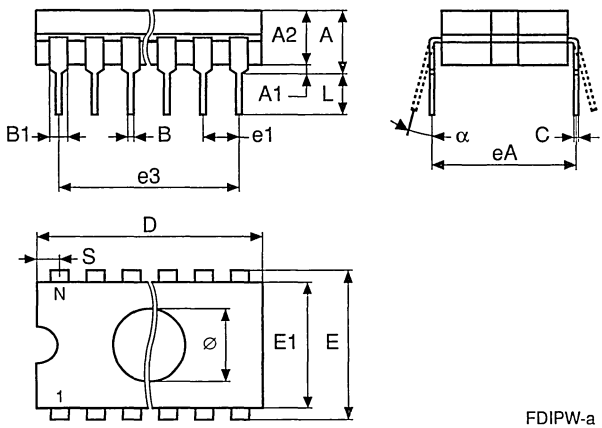
For a list of available options (Speed, V_{CC} Tolerance, Package, etc) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP28W - 28 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	33.02	–	–	1.300	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N	28			28		

FDIP28W

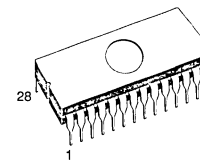


FDIPW-a

Drawing is out of scale

NMOS 512K (64K x 8) UV EPROM

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



FDIP28W (F)

DESCRIPTION

The M27512 is a 524,288 bit UV erasable and electrically programmable memory EPROM. It is organized as 65,536 words by 8 bits.

The M27512 is housed in a 28 Pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

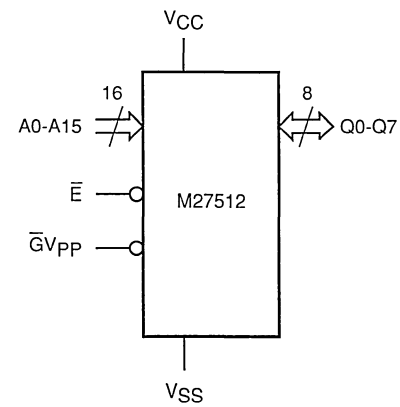
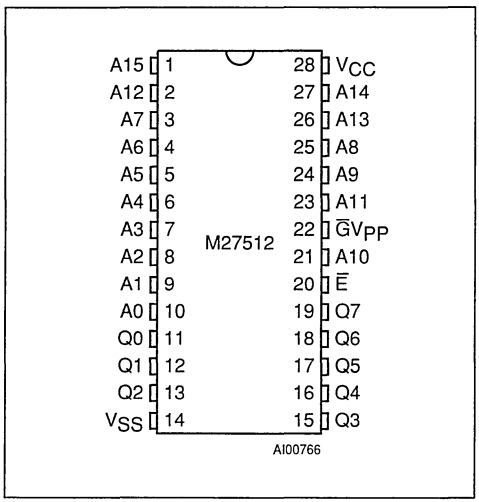


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	Grade 1 Grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	Grade 1 Grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.6 to 6.5	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality document

Figure 2. DIP Pin Connections



DEVICE OPERATION

The six modes of operations of the M27512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27512 has a standby mode which reduces the maximum active power current from 125mA to 40mA. The M27512 is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices.

The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommenced that a 1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered, and after each erasure, all bits of the M27512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27512 is in the programming mode when $\overline{G}V_{PP}$ input is at 12.5V and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. The M27512 can use PRESTO Programming Algorithm that drastically reduces the programming time (typically less than 50 seconds). Nevertheless to achieve compatibility with all programming equipment, the standard Fast Programming Algorithm may also be used.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27512 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27512 Fast Programming Algorithm is shown in Figure 8.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Verify	V_{IH}	V_{IL}	X	Data Out
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5%.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	1	1	0	1	0Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

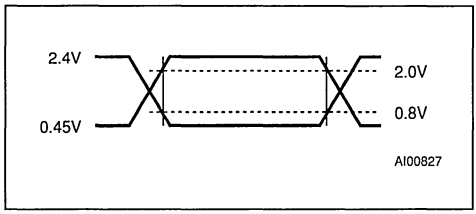


Figure 4. AC Testing Load Circuit

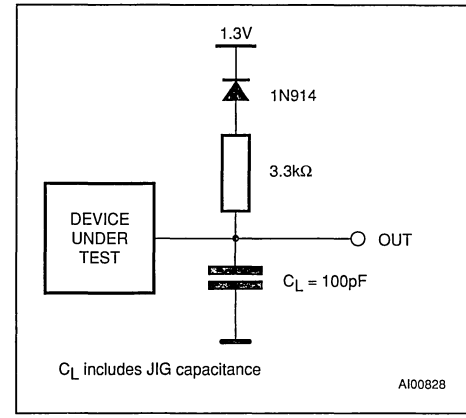


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

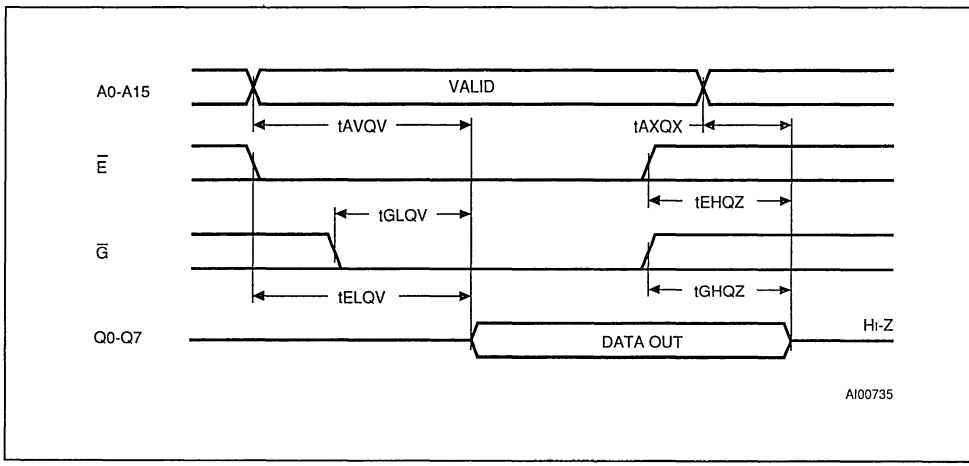


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{IH}$		40	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27512						Unit
				-2, -20		blank, -25		-3		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		75		100		120	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	55	0	60	0	105	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	55	0	60	0	105	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			150	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. MARGIN MODE AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

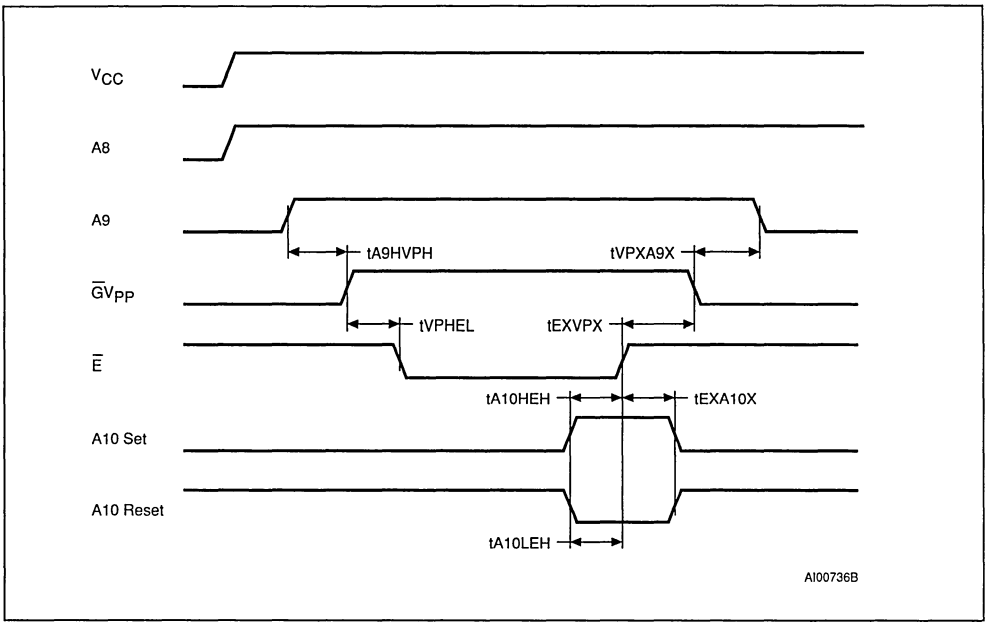
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t_{ELEH}	t_{OPW}	Chip Enable Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (4)	t_{DF}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. The Initial Program Pulse width tolerance is 1 ms ± 5%.
3. The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending on the multiplication value of the iteration counter.
4. Sampled only, not 100% tested

Figure 6. MARGIN MODE AC Waveform



Note: A8 High level = 5V; A9 High level = 12V.

Figure 7. Programming and Verify Modes AC Waveforms

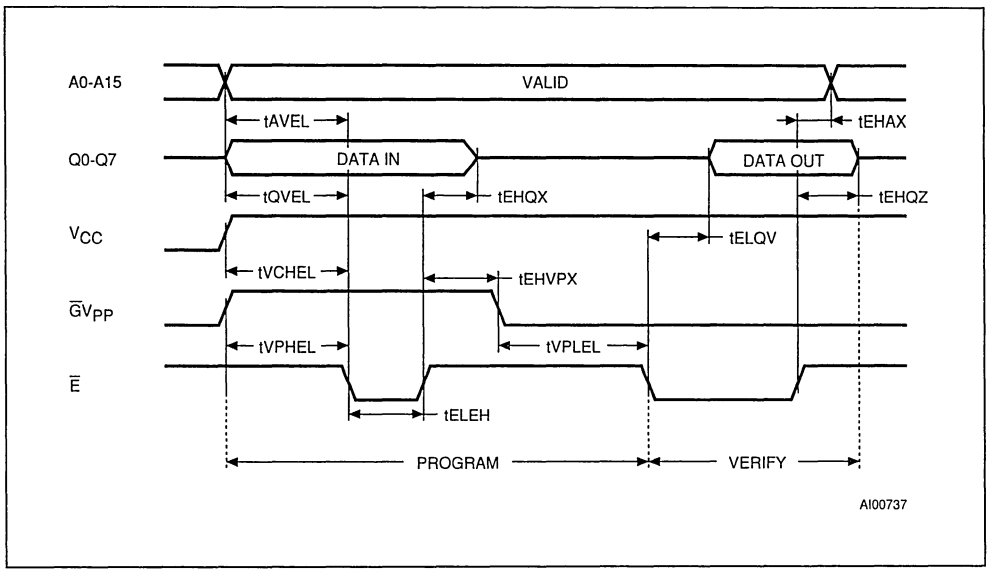


Figure 8. Fast Programming Flowchart

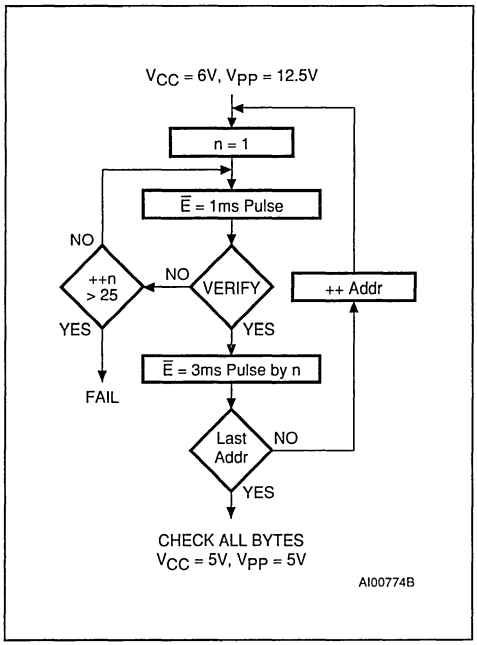
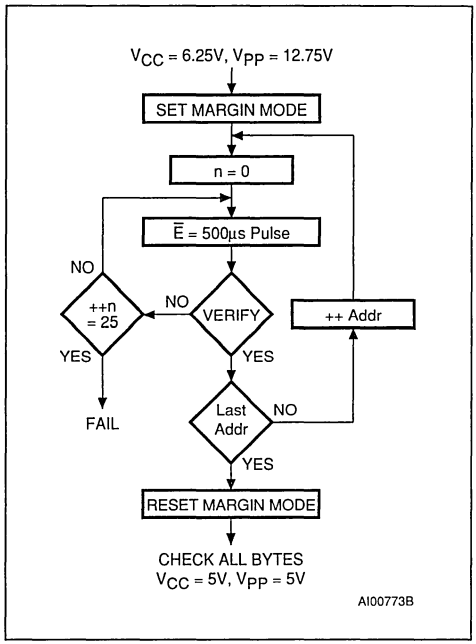


Figure 9. PRESTO Programming Flowchart



DEVICE OPERATION (cont'd)

The Fast Programming Algorithm utilizes two different pulse types : initial and overprogram. The duration of the initial $\overline{E}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ms by n (n is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27512 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

The entire sequence of program pulses is performed at V_{CC} = 6V and $\overline{G}V_{PP}$ = 12.5V (byte verifications at V_{CC} = 6V and $\overline{G}V_{PP} = V_{IL}$). When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V.

PRESTO Programming Algorithm

PRESTO Programming Algorithm allows to program the whole array with a guaranted margin, in a typical time of less than 50 seconds (to be compared with 283 seconds for the Fast algorithm). This can be achieved with the SGS-THOMSON M27512 due to several design innovations described in the next paragraph that improves programming efficiency and brings adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin.

Then a sequence of 500µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27512s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}V_{PP}$) of the parallel M27512 may be common. A TTL low level pulse applied to a M27512's $\overline{E}$ input, with $\overline{G}V_{pp}$ at 12.5V, will program that M27512. A high level $\overline{E}$ input inhibits the other M27512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}V_{pp}$ and $\overline{E}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{E}$.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25 °C ± 5 °C ambient temperature range that is required when programming the M27512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode, except for A14 and A15 which should be high. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristic of the M27512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27512 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27512 window to prevent unintentional erasure. The recommended erasure procedure for the M27512 is exposure to short wave ultraviolet light which has wavelength 2537 Å.

The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27512 -2 F 1

Speed and V_{CC} Tolerance		Package		Temperature Range	
-2	200 ns, 5V ±5%	F	FDIP28W	1	0 to 70 °C
blank	250 ns, 5V ±5%			6	–40 to 85 °C
-3	300 ns, 5V ±5%				
-20	200 ns, 5V ±10%				
-25	250 ns, 5V ±10%				

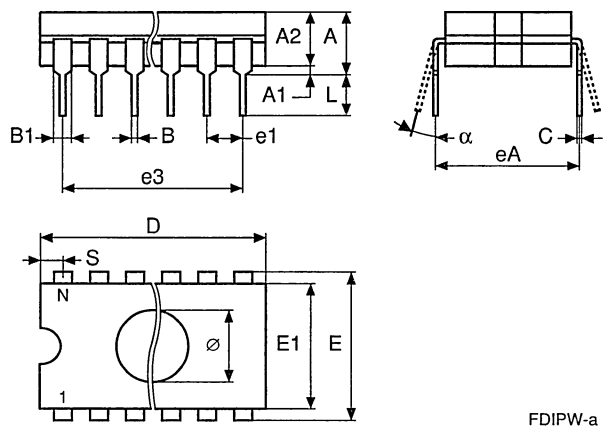
For a list of available options (Speed, V_{CC} Tolerance, Package, etc) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP28W - 28 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	33.02	–	–	1.300	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N	28			28		

FDIP28W



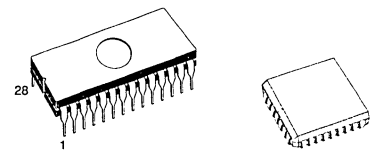
FDIPW-a

Drawing is out of scale

CMOS UV EPROM and OTP MEMORIES

64K (8K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 150ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.5V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- HIGH SPEED PROGRAMMING (less than 1 minute)



FDIP28W (F)

PLCC32 (C)

DESCRIPTION

The M27C64A is a high speed 65,536 bit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems requiring large programs. It is organized as 8,192 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only on time and erasure is not required, the M27C64A is offered in Plastic Leaded Chip Carrier package.

Figure 1. Logic Diagram

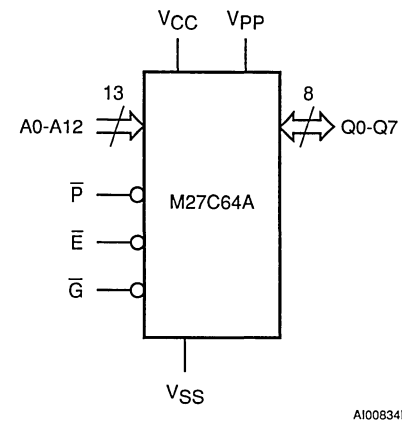
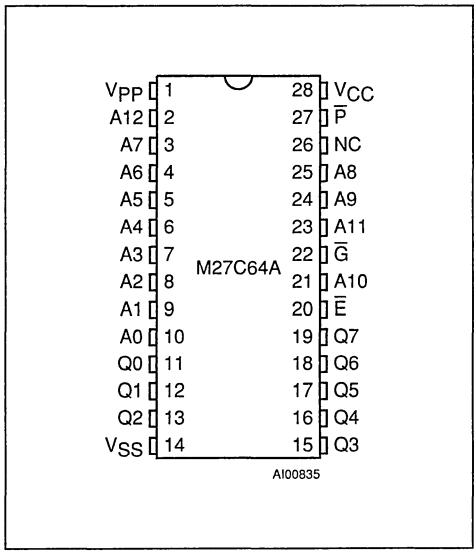


Table 1. Signal Names

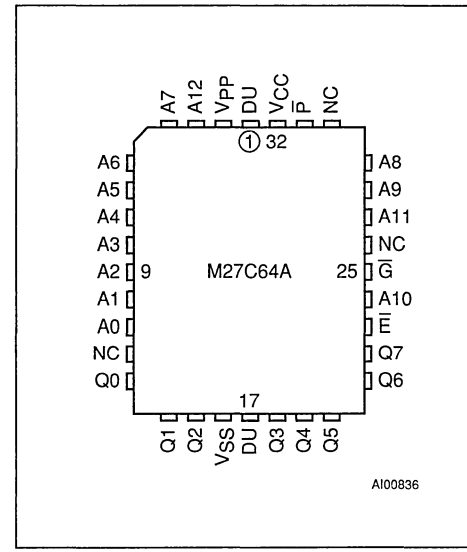
A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operation of the M27C64A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should

be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C64A has a standby mode which reduces the active current from 30mA to 100µA. The M27C64A is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	1	0	0	1	1	0	1	1	9Bh
Device Code	V_{IH}	0	0	0	0	1	0	0	0	08h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

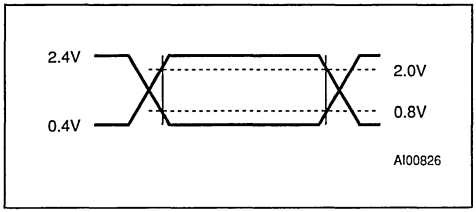


Figure 4. AC Testing Load Circuit

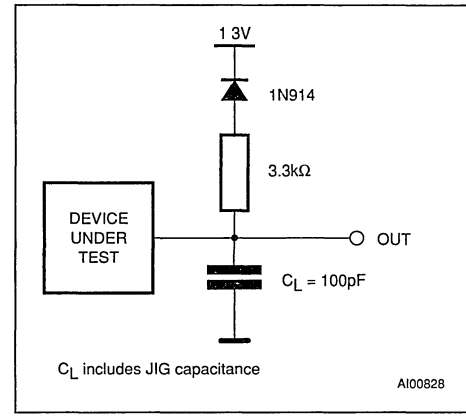


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

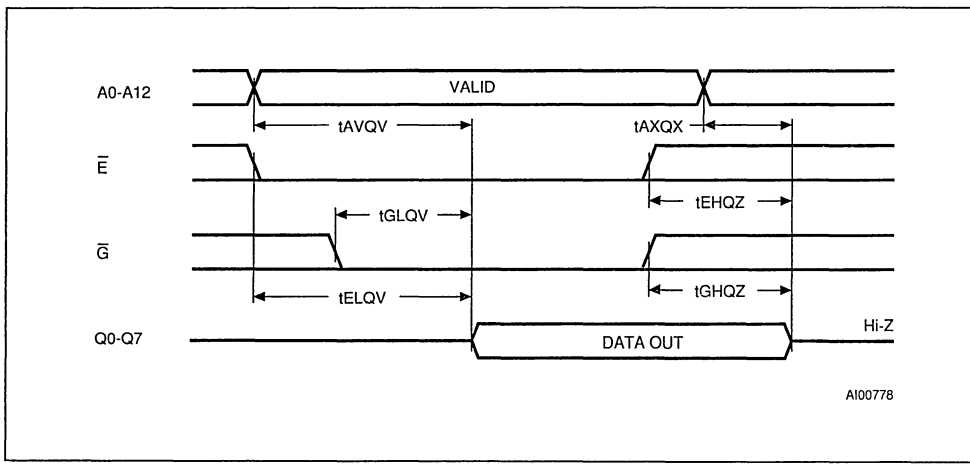


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C: V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C: V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C64A								Unit
				-15		-20		-25		-30		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		150		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		150		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		75		80		100		120	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	50	0	50	0	60	0	105	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	50	0	50	0	60	0	105	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			30	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		30	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width (Initial)		0.95	1.05	ms
		Program Pulse Width (Over Program)		2.85	78.75	ms
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

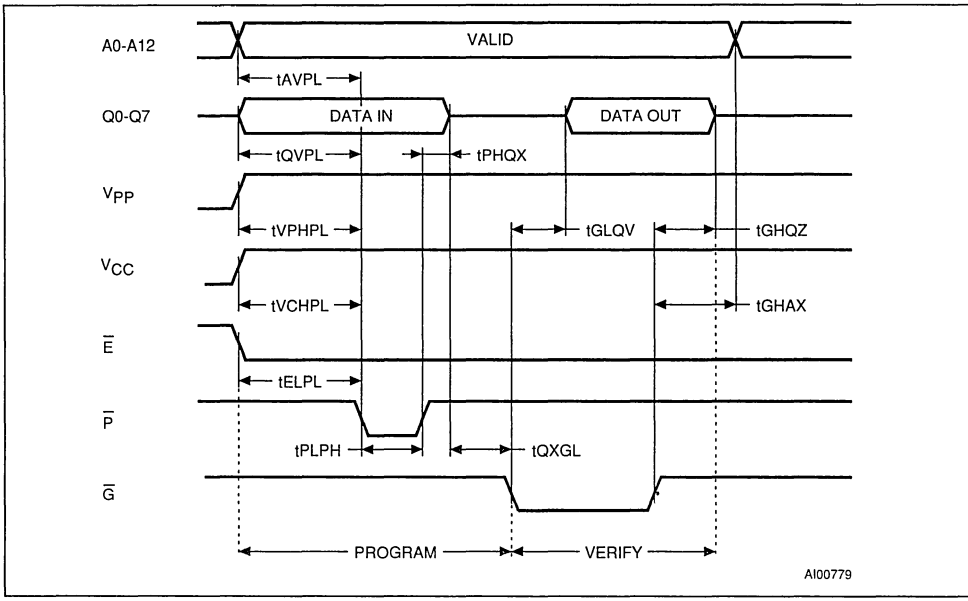
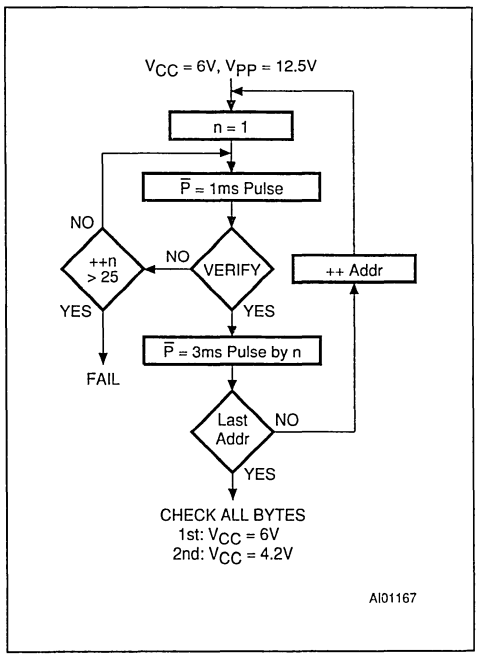


Figure 7. Programming Flowchart



Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C64A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C64A is in the programming mode when V_{pp} input is at 12.5V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6V ± 0.25V.

High Speed Programming

The high speed programming algorithm, described in the flowchart, rapidly programs the M27C64A using an efficient and reliable method, particularly suited to the production programming environment. An individual device will take around 1 minute to program.

Program Inhibit

Programming of multiple M27C64A in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C64A may be common. A TTL low level pulse applied to a M27C64A $\overline{E}$ input, with $\overline{P}$ low and V_{PP}

DEVICE OPERATIONS (cont'd)

at 12.5V, will program that M27C64A. A high level $\overline{E}$ input inhibits the other M27C64A from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.5V and V_{CC} at 6V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C64A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C64A, with $V_{PP}=V_{CC}=5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C64A, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C64A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C64A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C64A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C64A window to prevent unintentional erasure. The recommended erasure procedure for the M27C64A is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C64A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C64A -15 F 1 TR

Speed		Package		Temperature Range		Option	
-15	150 ns	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-20	200 ns	C	PLCC32	6	–40 to 85 °C		
-25	250 ns					TR	Tape & Reel Packing
-30	300 ns						

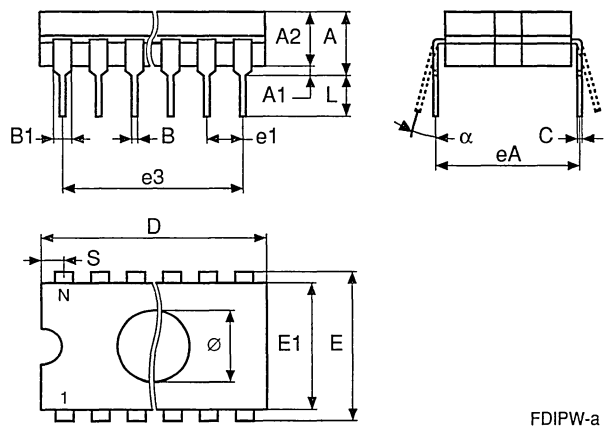
For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP28W - 28 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	33.02	–	–	1.300	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N		28			28	

FDIP28W



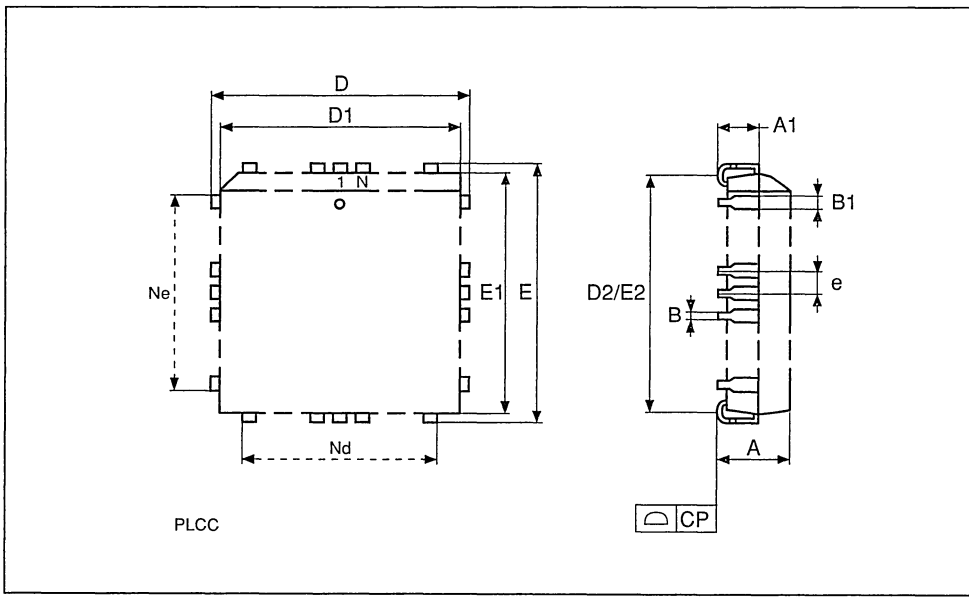
FDIPW-a

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier - rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

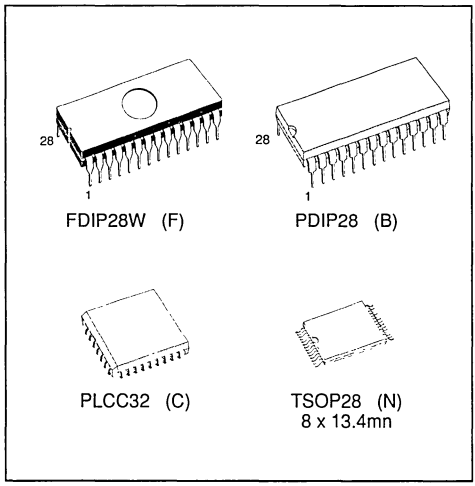
PLCC32



Drawing is out of scale

256K (32K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 3sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C256B is a high speed 262,144 bit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems. It is organized as 32,768 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C256B is offered in Plastic Dual-in-Line, Plastic Leaded Chip Carrier, and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

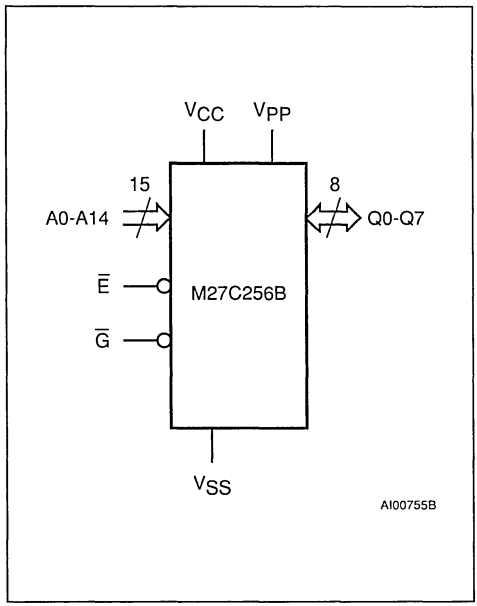


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2A. DIP Pin Connections

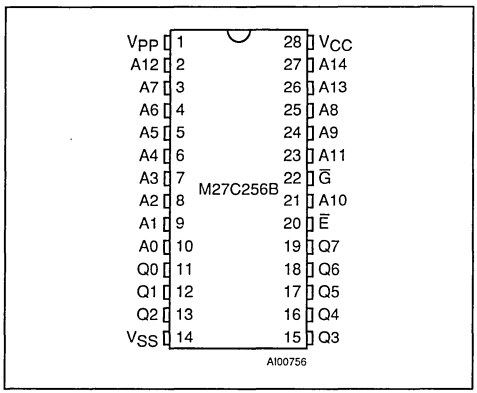
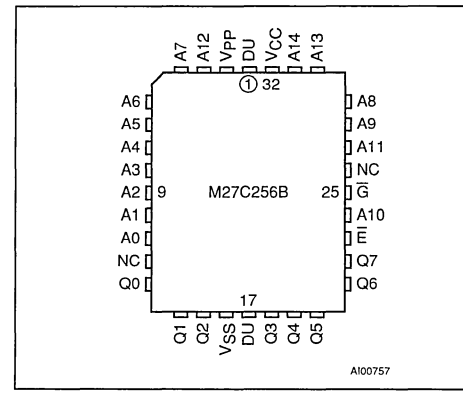
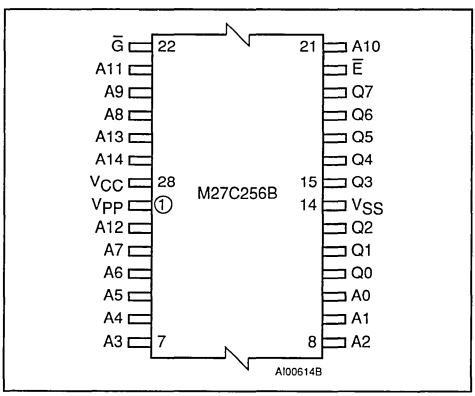


Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Dont't Use.

Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operation of the M27C256B are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C256B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time

DEVICE OPERATION (cont'd)

(t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C256B has a standby mode which reduces the active current from 30 mA to 100µA. The M27C256B is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

The power switching characteristics of Advance CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	1	0	1	8Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

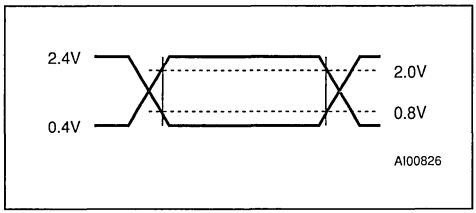


Figure 4. AC Testing Load Circuit

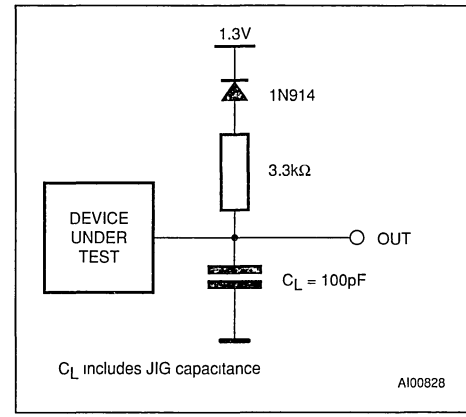


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C256B						Unit
				-70		-80		-90		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		80		90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C256B						Unit
				-10		-12		-15/-20/-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		60		65	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

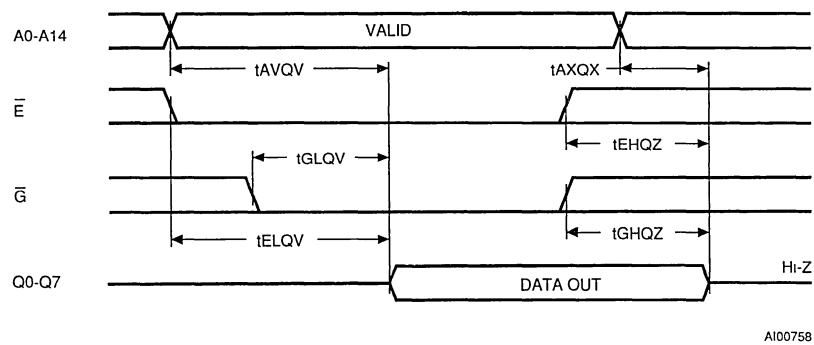


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

DEVICE OPERATION (cont'd)

4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C256B are in the '1' state. Data is introduced by selectively programming '0' into the desired bit locations. Although only '0' will be programmed, both '1' and '0' can be present in the data word. The only way to change a '0' to a '1' is by die exposition to ultraviolet light (UV EPROM). The M27C256B is in the programming mode when V_{PP} input is at 12.75 V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

Figure 6. Programming and Verify Modes AC Waveforms

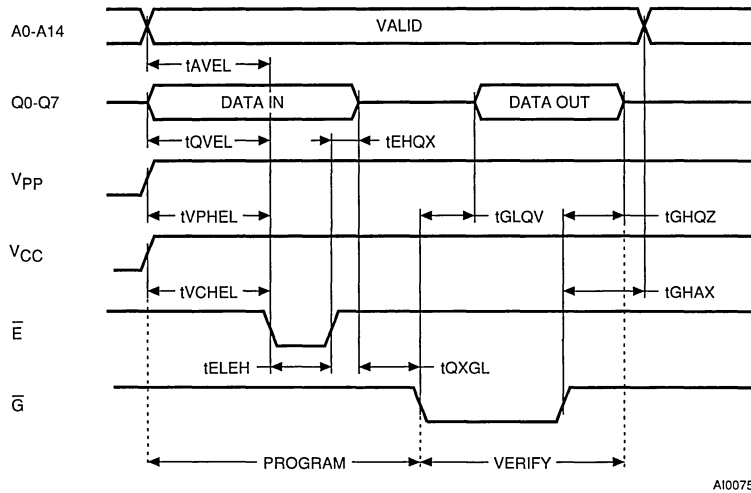
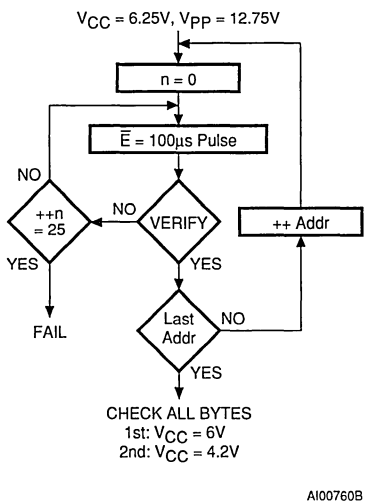


Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of 3.5 seconds. Programming with PRESTO II involves the application of a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C256Bs in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C256B may be common. A TTL low level pulse applied to a M27C256B's $\overline{E}$ input, with V_{PP} at 12.75 V, will program that M27C256B. A high level $\overline{E}$ input inhibits the other M27C256Bs from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C256B. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C256B, with V_{CC} = V_{PP} = 5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C256B, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C256B is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C256B in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C256B is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C256B window to prevent unintentional erasure. The recommended erasure procedure for the M27C256B is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C256B should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C256B -70 X C 1 TR

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-70	70 ns	X	± 5%	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-80	80 ns	blank	± 10%	B	PDIP28	3	–40 to 125 °C	TR	Tape & Reel Packing
-90	90 ns			C	PLCC32	6	–40 to 85 °C		
-10	100 ns			N	TSOP28 8 x 13.4mm	7	–40 to 105 °C		
-12	120 ns								
-15	150 ns								
-20	200 ns								
-25	250 ns								

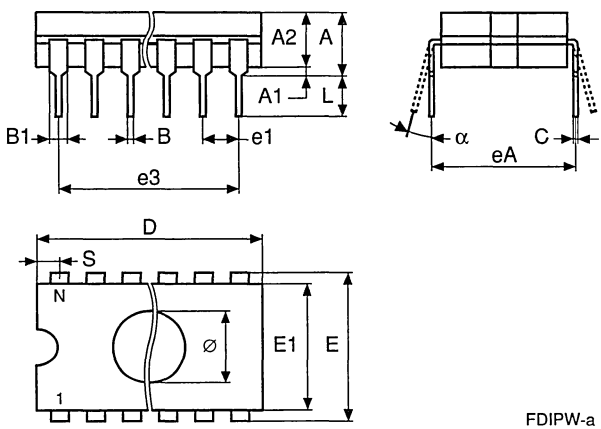
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP28W - 28 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	33.02	–	–	1.300	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N	28			28		

FDIP28W



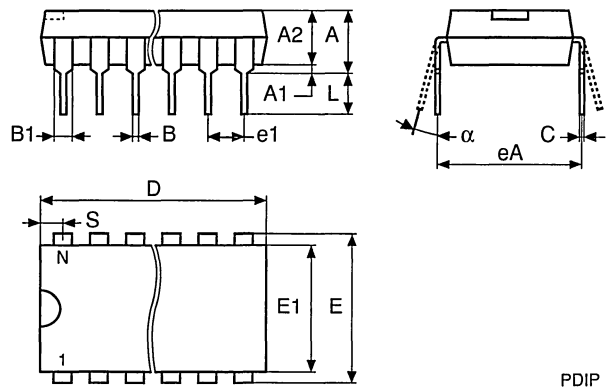
FDIPW-a

Drawing is out of scale

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28



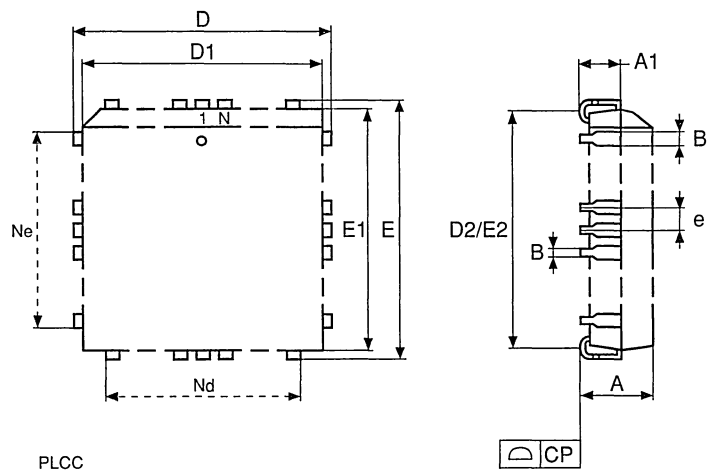
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier - rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32



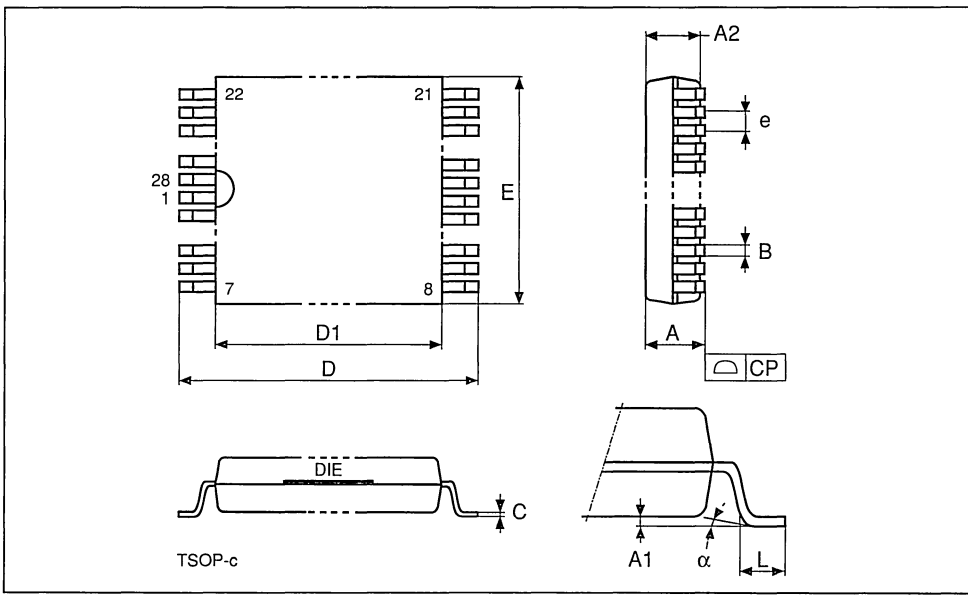
PLCC

Drawing is out of scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.00	1.25		0.039	0.049
A1			0.20			0.008
A2		0.95	1.05		0.037	0.041
B			0.30			0.012
C		0.10	0.21		0.004	0.008
D		13.10	13.70		0.516	0.539
D1		11.70	11.90		0.461	0.469
E		7.90	8.25		0.311	0.325
e	0.55	-	-	0.022	-	-
L		0.30	0.70		0.012	0.028
α		0°	5°		0°	5°
N		28			28	
CP			0.10			0.004

TSOP28

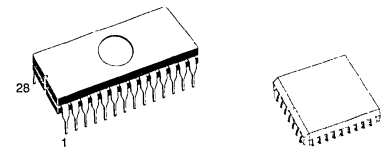


Drawing is out of scale

M87C257

ADDRESS LATCHED 256K (32K x 8) UV EPROM and OTP ROM

- INTEGRATED ADDRESS LATCH
- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 3sec. (PRESTO II ALGORITHM)



FDIP28W (F)

PLCC32 (C)

DESCRIPTION

The M87C257 is a high speed 262,144 bit UV erasable and electrically programmable memory EPROM. The M87C257 incorporates latches for all address inputs to minimize chip count, reduce cost, and simplify the design of multiplexed bus systems.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M87C257 is offered in Plastic Leaded Chip Carrier, package.

Table 1. Signal Names

A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{ASV}_{PP}$	Address Strobe / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

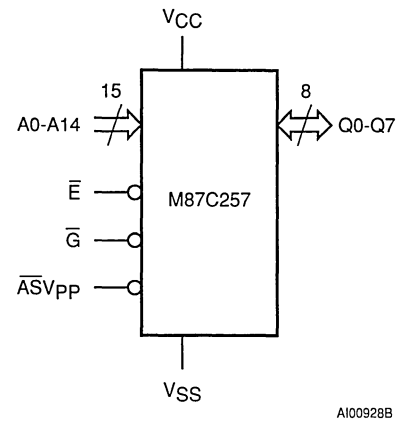


Figure 2A. DIP Pin Connections

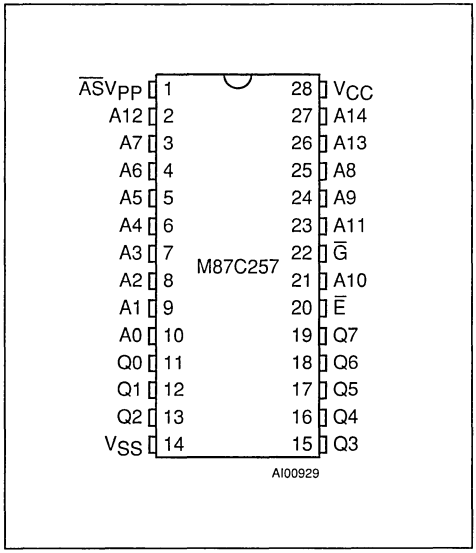
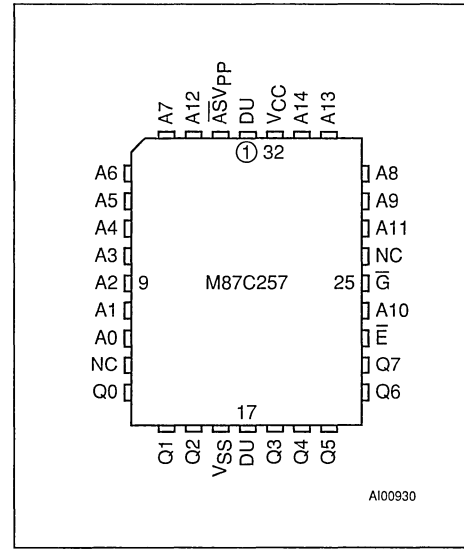


Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Dont't Use.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operation of the M87C257 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M87C257 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should

be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable ($\overline{AS}$ = V_{IH}) or latched ($\overline{AS}$ = V_{IL}), the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

The M87C257 reduces the hardware interface in multiplexed address-data bus systems. The processor multiplexed bus (AD0-AD7) may be tied to the M87C257's address and data pins. No separate address latch is needed because the M87C257 latches all address inputs when $\overline{AS}$ is low.

Standby Mode

The M87C257 has a standby mode which reduces the active current from 30mA to 100µA (Address Stable). The M87C257 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Considerations

The power switching characteristics of Advance CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	$\overline{AS}/V_{PP}$	Q0 - Q7
Read (Latched Address)	V_{IL}	V_{IL}	X	V_{IL}	Data Out
Read (Applied Address)	V_{IL}	V_{IL}	X	V_{IH}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{IL}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

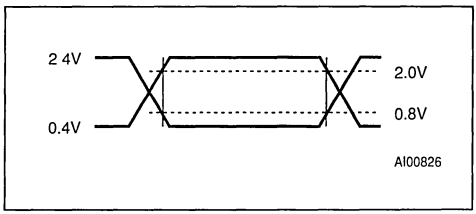


Figure 4. AC Testing Load Circuit

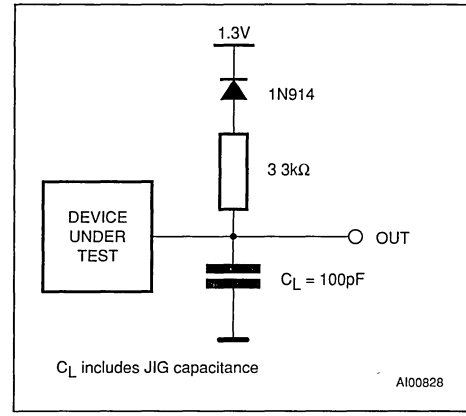


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

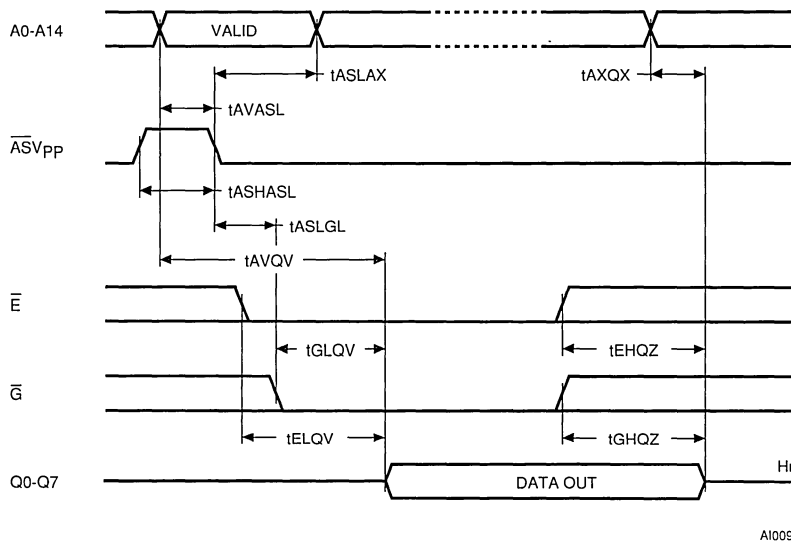
Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}, $\overline{ASV}_{PP}$ = V_{IH}, Address Switching		10	mA
		$\overline{E}$ = V_{IH}, $\overline{ASV}_{PP}$ = V_{IL}, Address Stable		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ ≥ V_{CC} – 0.2V, $\overline{ASV}_{PP}$ ≥ V_{CC} – 0.2V, Address Switching		6	mA
		$\overline{E}$ ≥ V_{CC} – 0.2V, $\overline{ASV}_{PP}$ = V_{SS}, Address Stable		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	V_{CC} – 0.8V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Figure 5. Read Mode AC Waveforms



DEVICE OPERATION (cont'd)

capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M87C257 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M87C257 is in the programming mode when V_{PP} input is at 12.75 V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of 3.5 seconds. Programming with PRESTO II involves the application of a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M87C257s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M87C257 may be common. A TTL low level pulse applied to a M87C257's $\overline{E}$ input, with V_{PP} at 12.75 V, will program that M87C257. A high level $\overline{E}$ input inhibits the other M87C257s from being programmed.

Table 7A. Read Mode AC Characteristics (1)

(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M87C257						Unit
				-70		-80		-90		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, G = V_{IL}		70		80		90	ns
t_{AVASL}	t_{AL}	Address Valid to Address Strobe Low		7		7		7		ns
t_{ASHASL}	t_{LL}	Address Strobe High to Address Strobe Low		35		35		35		ns
t_{ASLAX}	t_{LA}	Address Strobe Low to Address Transition		20		20		20		ns
t_{ASLGL}	t_{LOE}	Address Strobe Low to Output Enable Low		20		20		20		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)

(T_A = 0 to 70°C, –40 to 85°C, –40 to 105°C or –40 to 125°C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M87C257								Unit
				-10		-12		-15		-20		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150		200	ns
t_{AVASL}	t_{AL}	Address Valid to Address Strobe Low		7		7		7		15		ns
t_{ASHASL}	t_{LL}	Address Strobe High to Address Strobe Low		35		35		35		50		ns
t_{ASLAX}	t_{LA}	Address Strobe Low to Address Transition		20		20		20		30		ns
t_{ASLGL}	t_{LOE}	Address Strobe Low to Output Enable Low		20		20		20		30		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		50		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	40	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	40	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	V_{CC} -0.8V		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Figure 6. Programming and Verify Modes AC Waveforms

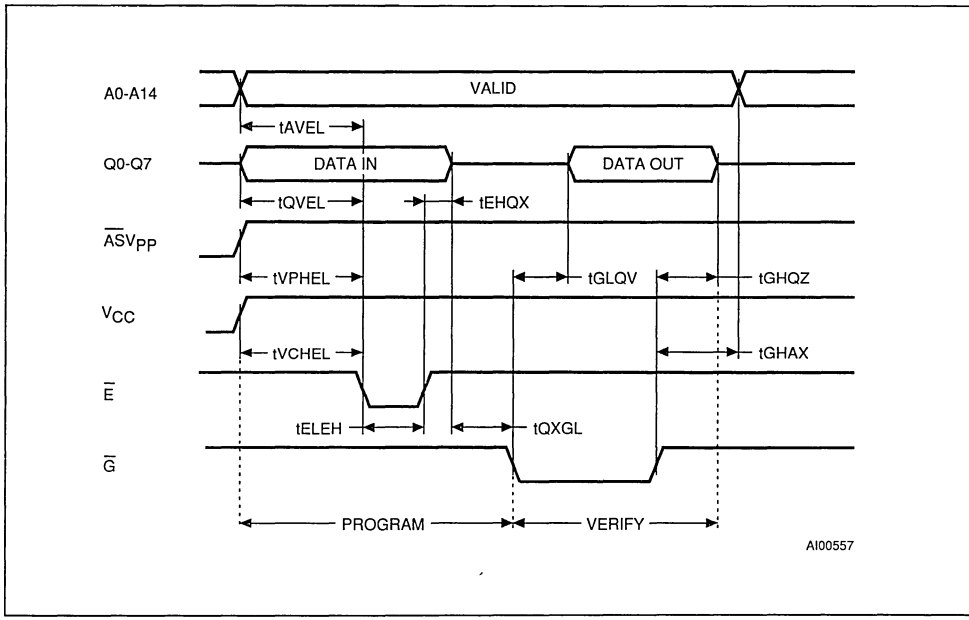
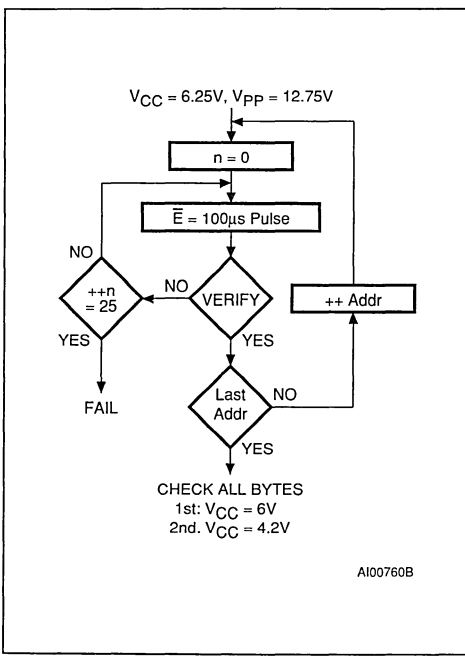


Figure 7. Programming Flowchart



Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M87C257.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M87C257, with $V_{CC} = V_{PP} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. When $A9 = V_{ID}$, $\overline{AS}$ need not be toggled to latch each identifier address. For the SGS-THOMSON M87C257, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M87C257 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M87C257 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M87C257 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M87C257 window to prevent unintentional erasure. The recommended erasure procedure for the M87C257 is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M87C257 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M87C257 -10 X F 1 X

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-70	70 ns	X	± 5%	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-80	80 ns	blank	± 10%	C	PLCC32	3	–40 to 125 °C	TR	Tape & Reel Packing
-90	90 ns					6	–40 to 85 °C		
-10	100 ns					7	–40 to 105 °C		
-12	120 ns								
-15	150 ns								
-20	200 ns								

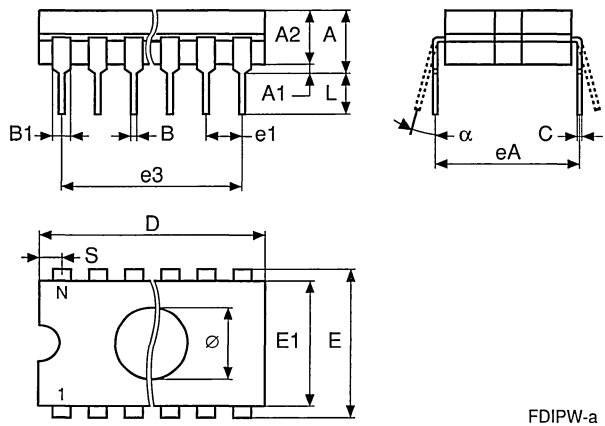
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP28W - 28 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	33.02	–	–	1.300	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N	28			28		

FDIP28W



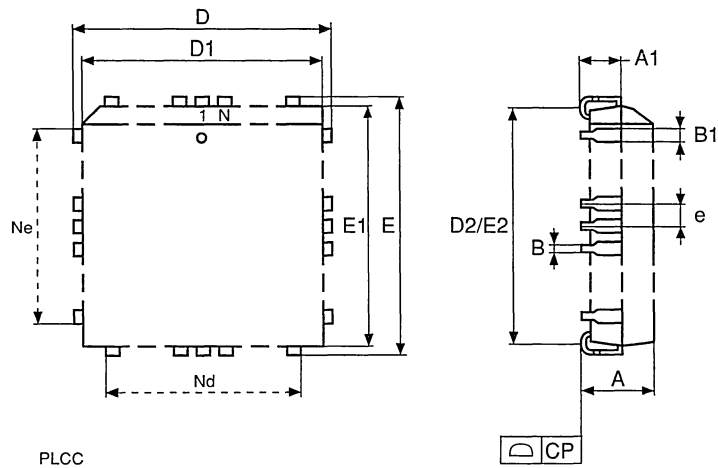
FDIPW-a

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

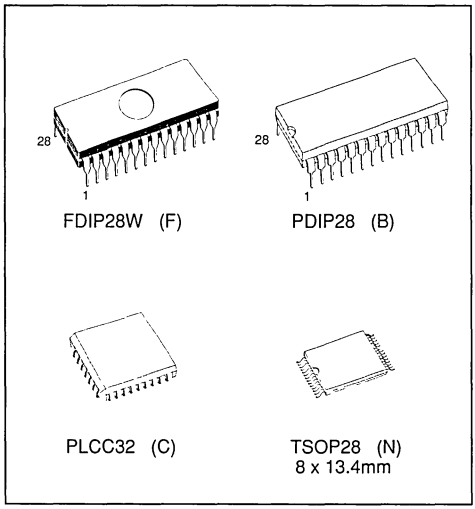


PLCC

Drawing is out of scale

512K (64K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 60ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 6sec. (PRESTO IIB ALGORITHM)



DESCRIPTION

The M27C512 is a high speed 524,288 bit UV erasable and electrically programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. Its is organized as 65,536 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C512 is offered in Plastic Dual-in-Line, Plastic Thin Small Outline and Plastic Leaded Chip Carrier packages.

Figure 1. Logic Diagram

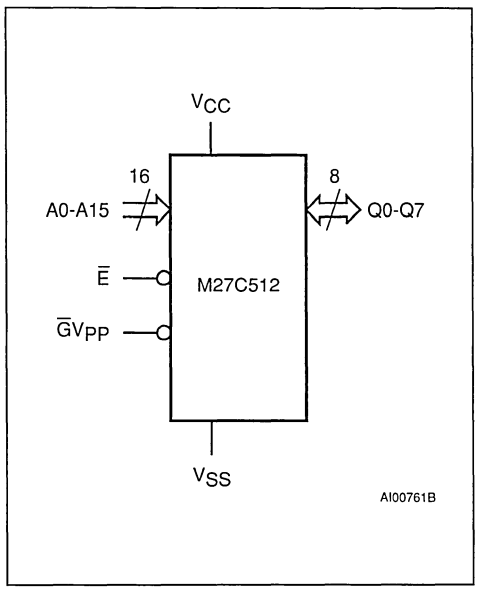


Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2A. DIP Pin Connections

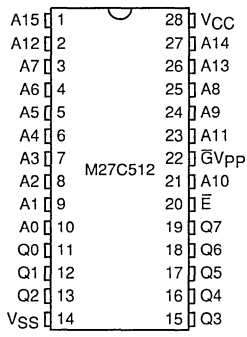
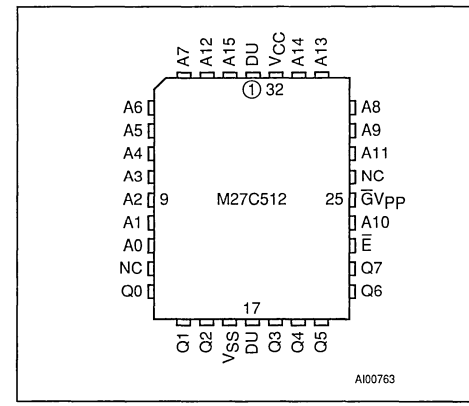
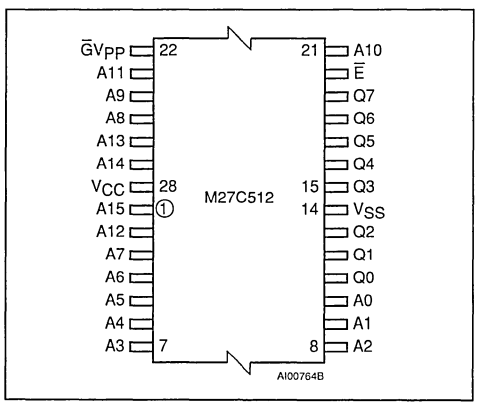


Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Don't Use

Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operations of the M27C512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}).

DEVICE OPERATION (cont'd)

Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C512 has a standby mode which reduces the active current from 30mA to 100µA The M27C512 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C512 are in the '1' state. Data is introduced by selectively programming '0' into the desired bit locations. Although only '0' will be programmed, both '1' and '0' can be present in the data word. The only way to change a '0' to a '1' is by die exposure to ultraviolet light (UV EPROM). The M27C512 is in the programming mode when V_{PP} input is at 12.75V and $\overline{E}$ is at

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	1	1	1	1	0	1	3Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

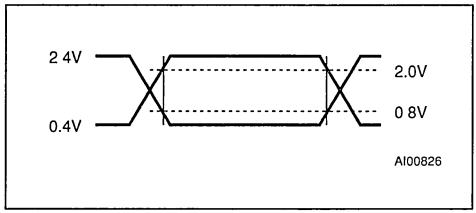


Figure 4. AC Testing Load Circuit

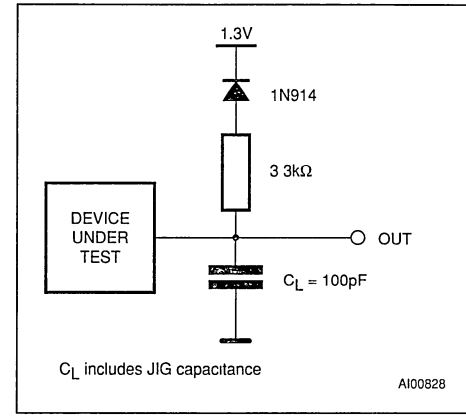


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note. 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C512								Unit
				-60		-70		-80		-90		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		60		70		80		90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		60		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		30		35		40		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	25	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	25	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C512						Unit
				-10		-12		-15/-20/-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

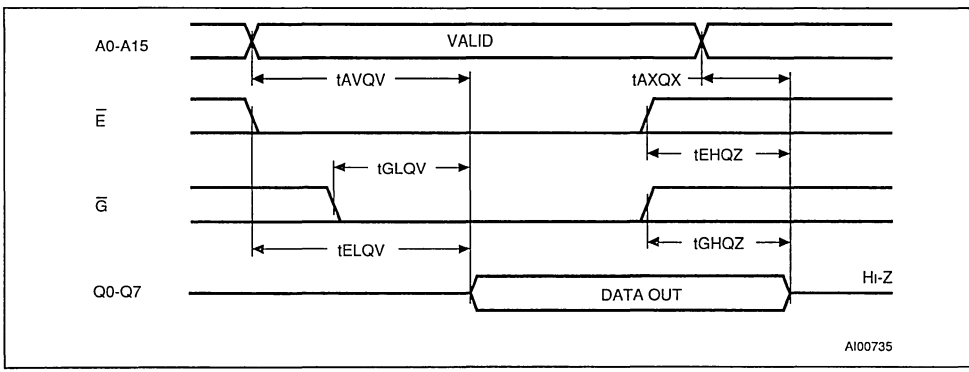


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}

Table 9. MARGIN MODE AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

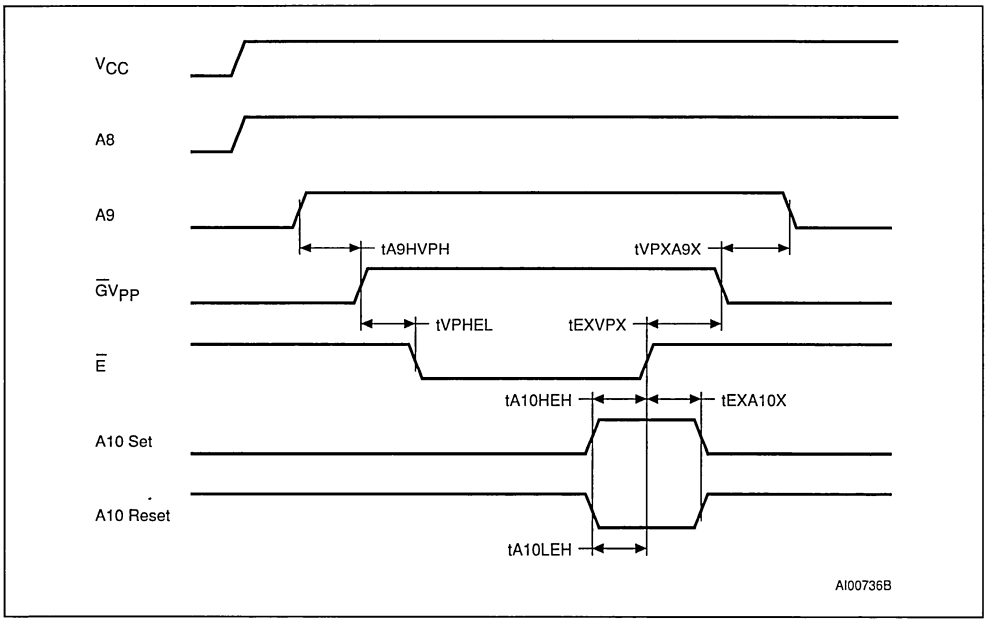
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (2)	t_{DFP}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. MARGIN MODE AC Waveforms



Note: A8 High level = 5V; A9 High level = 12V.

Figure 7. Programming and Verify Modes AC Waveforms

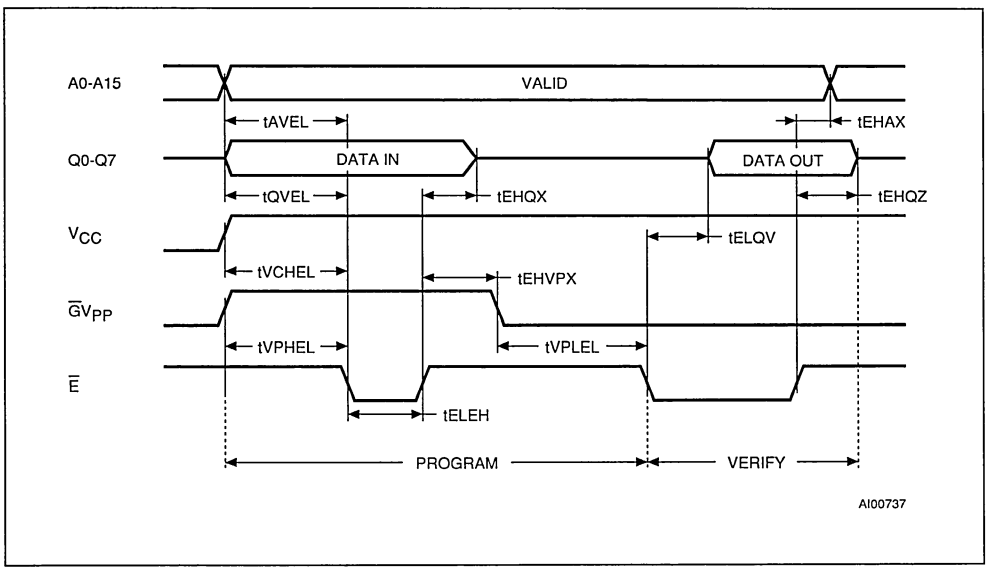
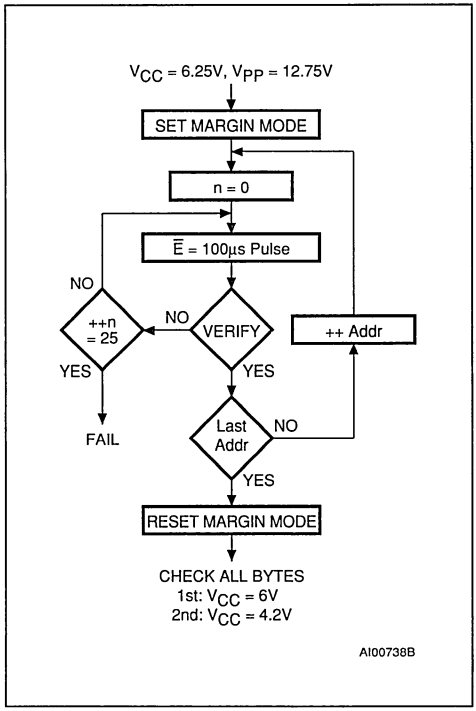


Figure 8. Programming Flowchart



DEVICE OPERATION (cont'd)

TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

The M27C512 can use PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically less than 6 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used as well.

PRESTO IIB Programming Algorithm

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 6.5 seconds. This can be achieved with SGS-THOMSON M27C512 due to several design innovations described in the M27C512 datasheet to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 100µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

Program Inhibit

Programming of multiple M27C512s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}V_{PP}$ of the parallel M27C512 may be common. A TTL low level pulse applied to a M27C512's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C512. A high level $\overline{E}$ input inhibits the other M27C512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C512, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range.

Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C512 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C512 window to prevent unintentional erasure. The recommended erasure procedure for the M27C512 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C512 -70 X C 1 TR

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-60	60 ns	X	± 5%	F	FDIP28W	1	0 to 70 °C	X	Additional Burn-in
-70	70 ns	blank	± 10%	B	PDIP28	3	–40 to 125 °C	TR	Tape & Reel Packing
-80	80 ns			C	PLCC32	6	–40 to 85 °C		
-90	90 ns			N	TSOP28 8 x 13.4mm				
-10	100 ns								
-12	120 ns								
-15	150 ns								
-20	200 ns								
-25	250 ns								

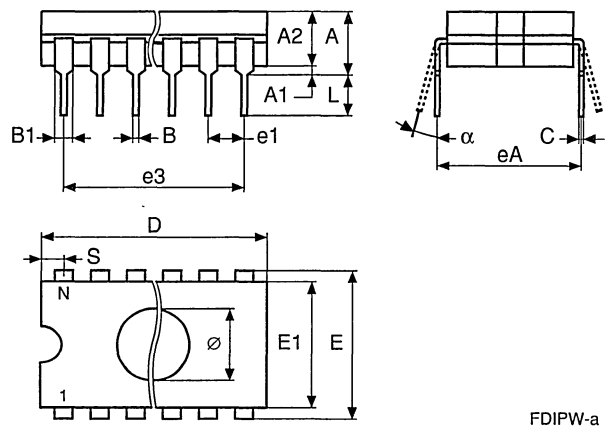
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP28W - 28 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	33.02	–	–	1.300	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N		28			28	

FDIP28W



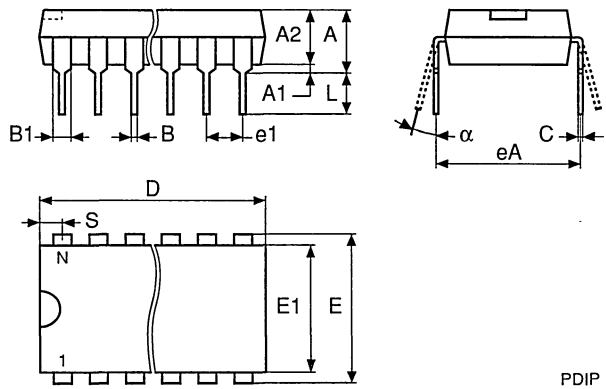
FDIPW-a

Drawing is out of scale

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28



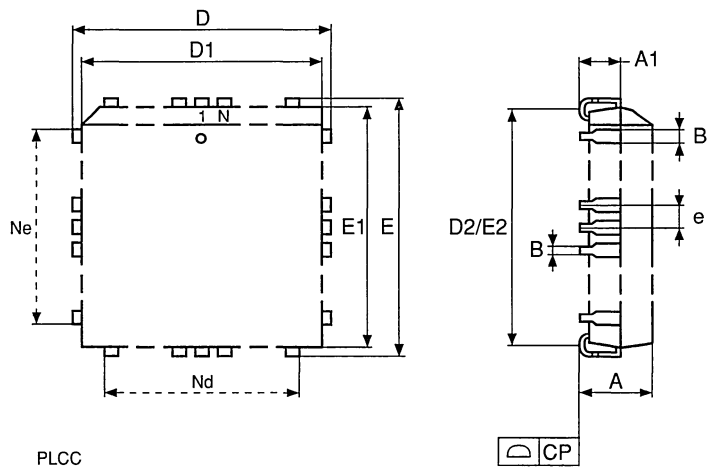
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32



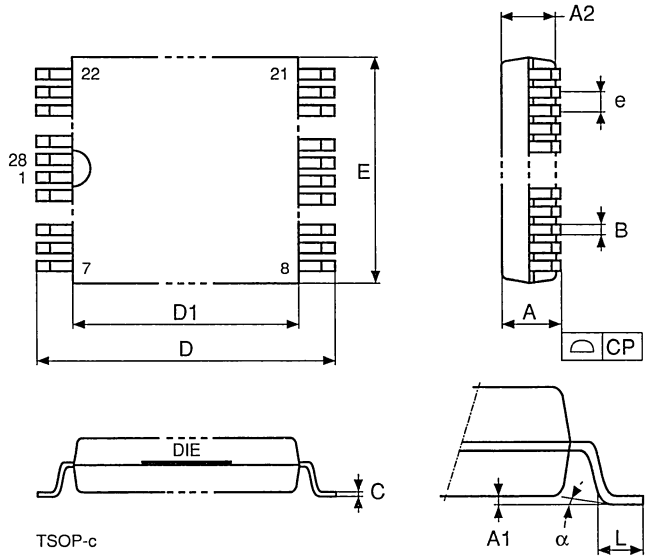
PLCC

Drawing is out of scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004

TSOP28

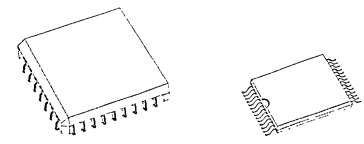


TSOP-c

Drawing is out of scale

LOW VOLTAGE 512K (64K x 8) OTP ROM

- LOW VOLTAGE READ OPERATION: 3V to 5.5V
- ACCESS TIME: 120, 150 and 200ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 10mA
  - Standby Current 10µA
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 6sec. (PRESTO IIB ALGORITHM)
- M27V512 is PROGRAMMABLE as M27C512 with IDENTICAL SIGNATURE



PLCC32 (K)

TSOP28 (N)
8 x 13.4mm

DESCRIPTION

The M27V512 is a low voltage, low power 512K One Time Programmable ROM ideally suited for handheld and portable microprocessor systems requiring large programs. Its is organized as 524,288 by 8 bits.

The M27V512 operates in the read mode with a supply voltage as low as 3V. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges. The M27V512 can also be operated as a standard 512 EPROM (similar to M27C512) with a 5V power supply.

For equipment requiring a surface monted, low profile package, theM27V512 is offered in Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Figure 1. Logic Diagram

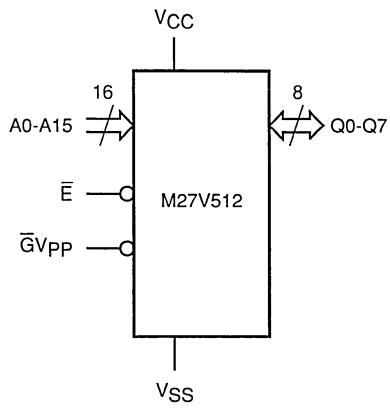
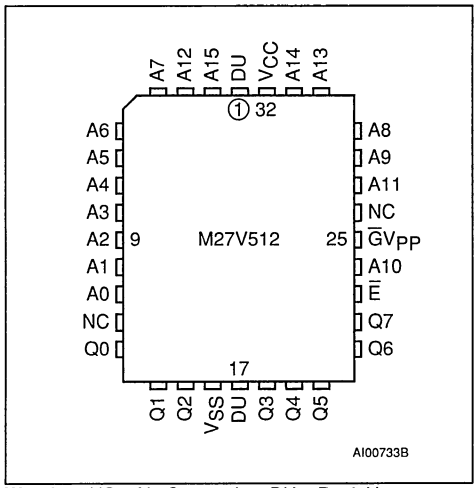


Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. LCC Pin Connections



Warning: NC = No Connection, DU = Don't Use.

Figure 2B. TSOP Pin Connections

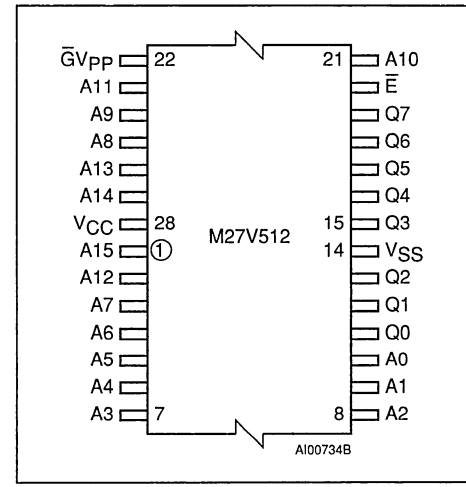


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operations of the M27V512 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27V512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, inde-

DEVICE OPERATION (Cont'd)

pendent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V512 has a standby mode which reduces the active current from 10mA to 10µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V512 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because OTP ROMs are often used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS OTP ROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	1	1	1	1	0	1	3Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

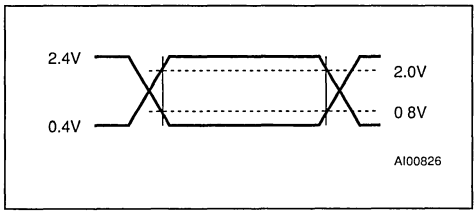


Figure 4. AC Testing Load Circuit

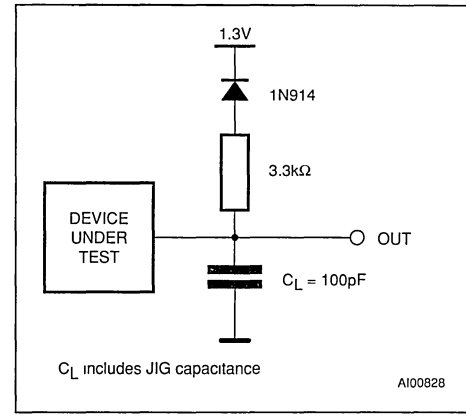


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C ; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 3.2V		10	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		10	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or −40 to 85 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27V512						Unit
				-120		-150		-200		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		65		70		80	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	60	0	60	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	60	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

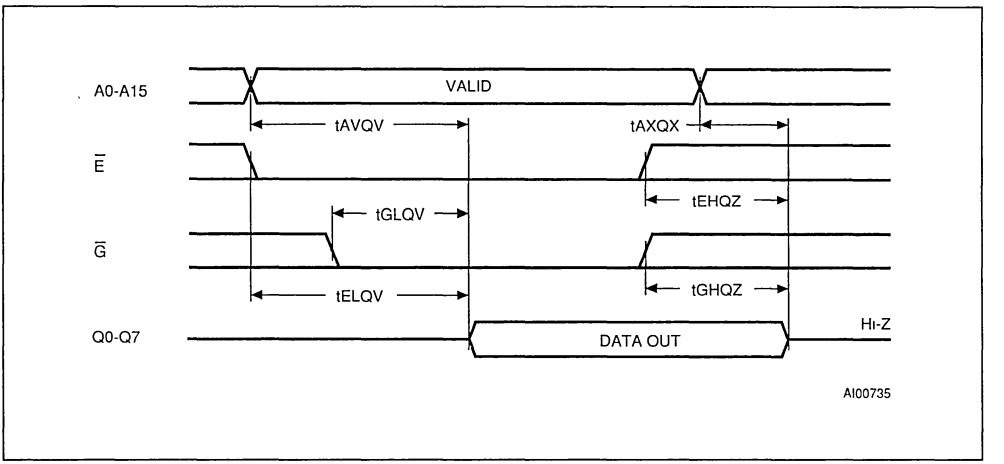


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Table 9. MARGIN MODE AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

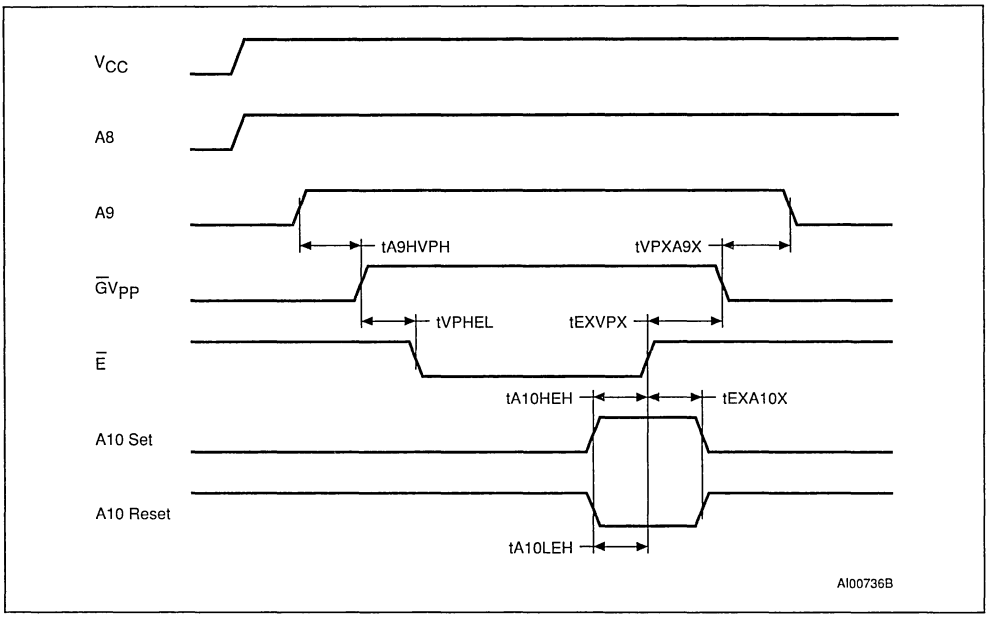
Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		0		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (2)	t_{DFP}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested

Figure 6. MARGIN MODE AC Waveforms



Note: A8 High level = 5V; A9 High level = 12V.

Figure 7. Programming and Verify Modes AC Waveforms

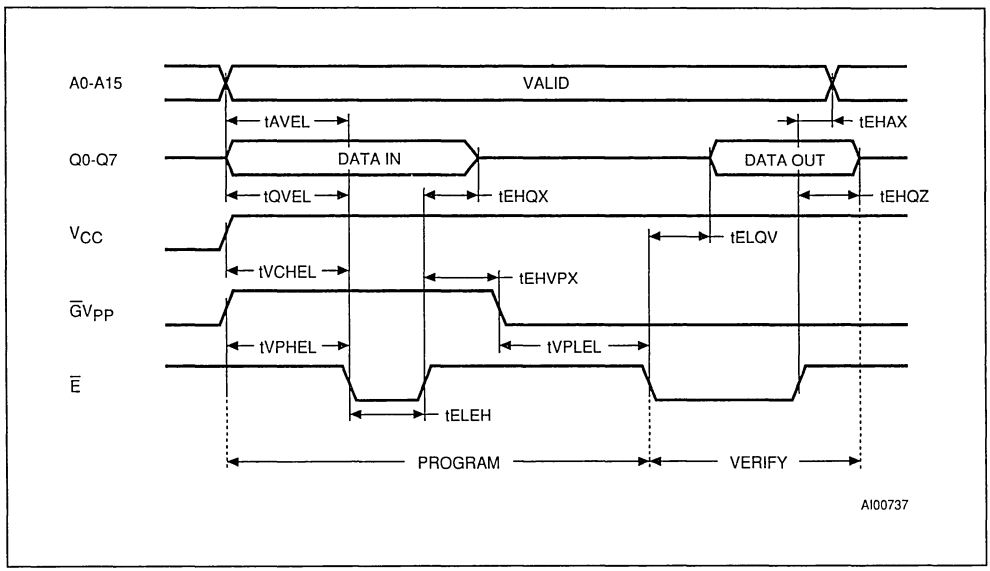
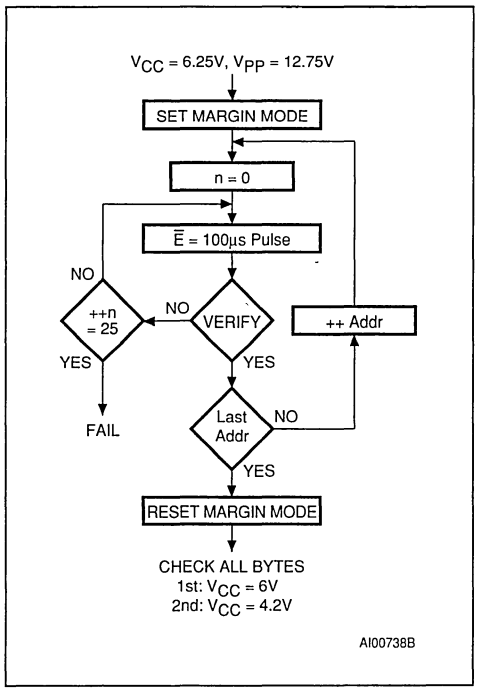


Figure 8. Programming Flowchart



Programming

The M27V512 has been designed to be fully compatible with the M27C512. As a result the M27V512 can be programmed as the M27C512 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V512 has the same electronic signature and uses the same PRESTO IIB algorithm.

When delivered, all bits of the M27V512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The M27V512 is in the programming mode when V_{PP} input is at 12.75V and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

The M27V512 uses the PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically less than 6 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used as well.

PRESTO IIB Programming Algorithm

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, a typical time of 6.5 seconds. This can be achieved with SGS-THOMSON M27V512 due to several design innovations to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 100µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

Program Inhibit

Programming of multiple M27V512s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}V_{PP}$ of the parallel M27V512 may be common. A TTL low level pulse applied to a M27V512's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27V512. A high level $\overline{E}$ input inhibits the other M27V512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

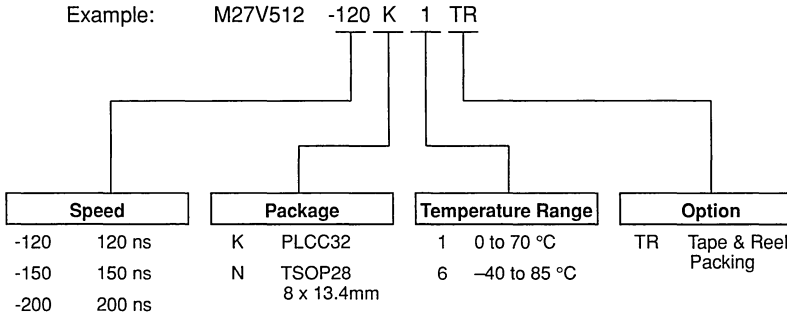
Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V512. To activate this mode, the programming equipment must apply a Supply Voltage V_{CC} of 5V and force 11.5V to 12.5V on address line A9 of the M27V512.

Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27V512, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

Note that the M27V512 and the M27C512 have the same identifier bytes.

ORDERING INFORMATION SCHEME



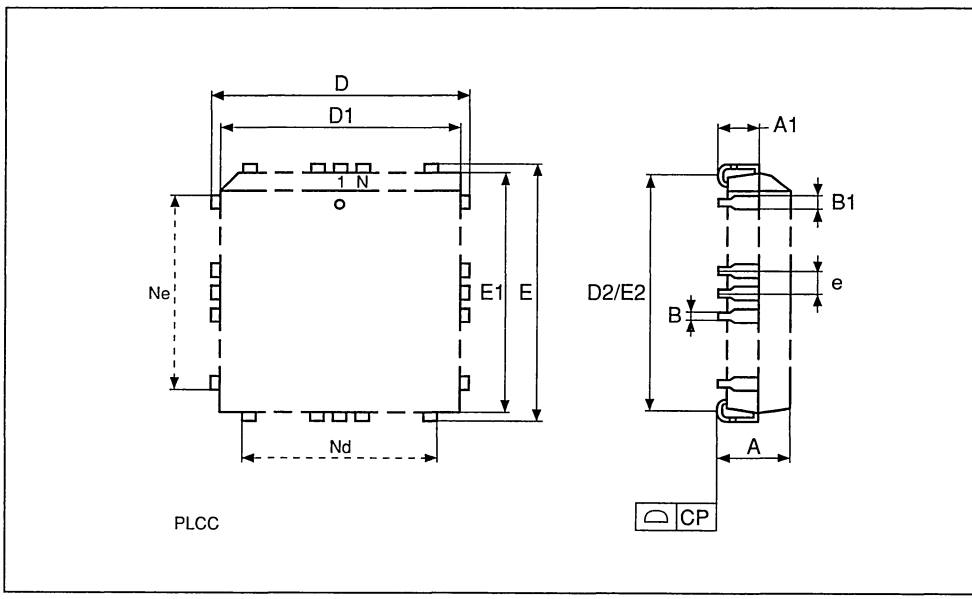
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

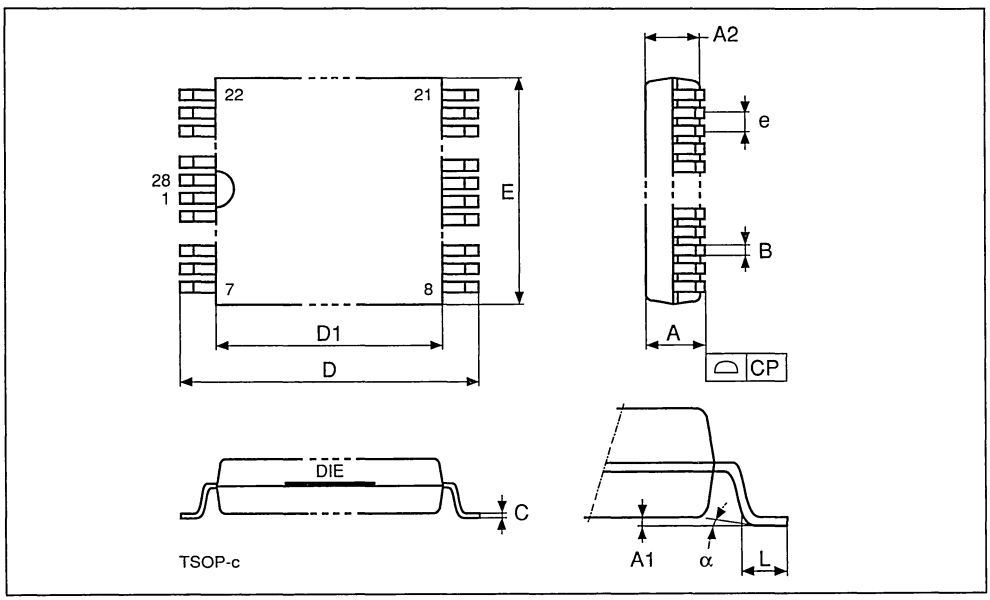


Drawing is out of scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		28			28	
CP			0.10			0.004

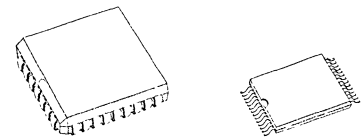
TSOP28



Drawing is out of scale

VERY LOW VOLTAGE 512K (64K x 8) OTP ROM

- VERY LOW VOLTAGE READ OPERATION: 2.7V to 5.5V
- ACCESS TIME:
  - 150ns (T_A = 0 to 70 °C)
  - 200ns (T_A = –20 to 70 °C)
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 10mA
  - Standby Current 10µA
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 6sec. (PRESTO IIB ALGORITHM)
- M27W512 is PROGRAMMABLE as M27C512 with IDENTICAL SIGNATURE



PLCC32 (K)

TSOP28 (N)
8 x 13.4mm

DESCRIPTION

The M27W512 is a very low voltage, low power 512K One Time Programmable ROM ideally suited for handheld and portable microprocessor systems requiring large programs. Its is organized as 524,288 by 8 bits.

The M27W512 operates in the read mode with a supply voltage as low as 2.7V at –20 to 70 °C temperature range. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges. The M27W512 can also be operated as a standard 512 EPROM (similar to M27C512) with a 5V power supply.

For equipment requiring a surface monted, low profile package, the M27W512 is offered in Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Figure 1. Logic Diagram

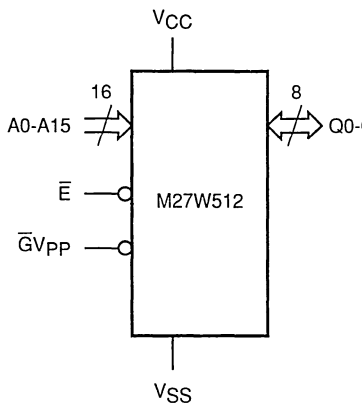


Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. LCC Pin Connections

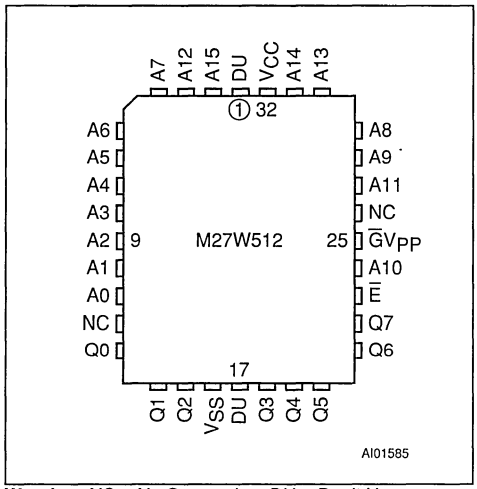
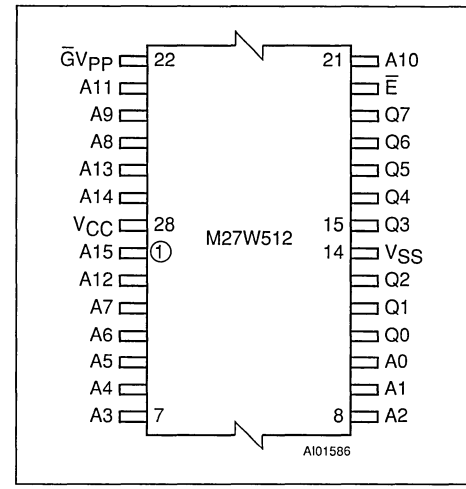


Figure 2B. TSOP Pin Connections



Warning: NC = No Connection, DU = Don't Use.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–20 to 70	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operations of the M27W512 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27W512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, inde-

DEVICE OPERATION (Cont'd)

pendent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27W512 has a standby mode which reduces the active current from 10mA to 10µA with low voltage operation $V_{CC} \leq 2.7V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27W512 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because OTP ROMs are often used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS OTP ROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	1	1	1	1	0	1	3Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

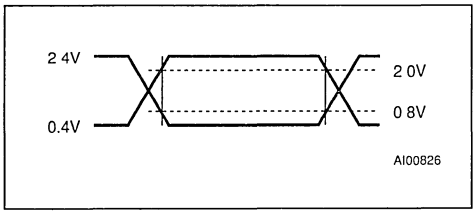


Figure 4. AC Testing Load Circuit

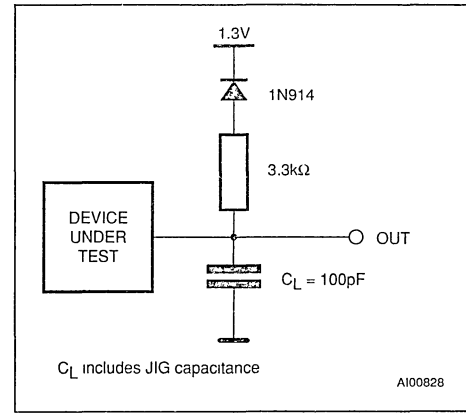


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 6. Read Mode DC Characteristics (1)
(T_A = –20 to 70 °C ; V_{CC} = 2.7V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 2.7V		10	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 2.7V		10	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = –20 to 70 °C; V_{CC} = 2.7V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27W512				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		75		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	60	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

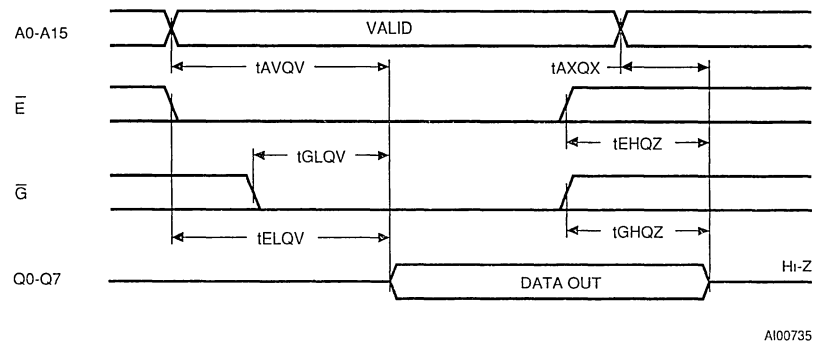


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Table 9. MARGIN MODE AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

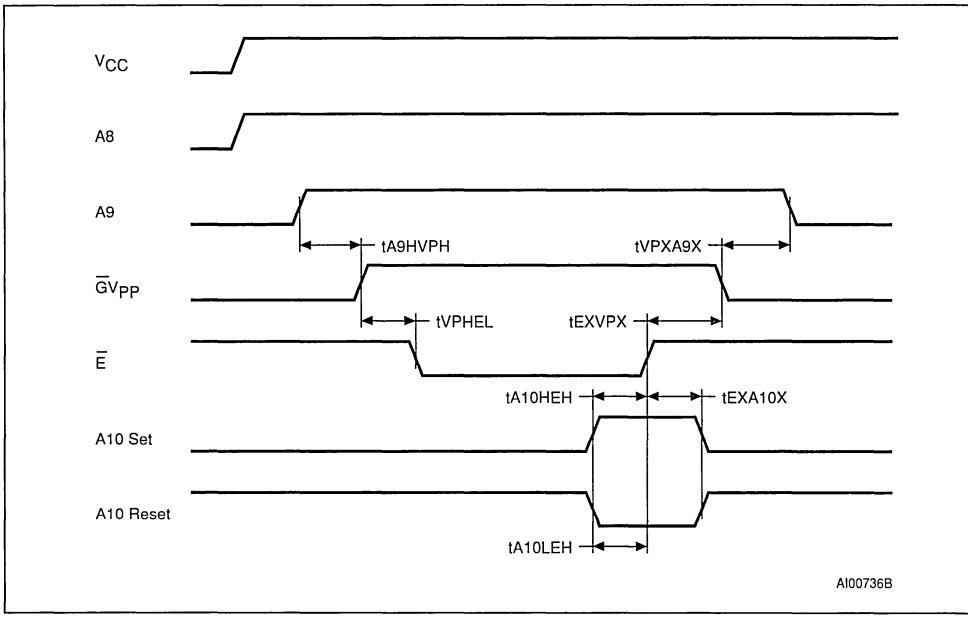
Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Units
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		0		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (2)	t_{DFP}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested

Figure 6. MARGIN MODE AC Waveforms



Note: A8 High level = 5V, A9 High level = 12V.

Figure 7. Programming and Verify Modes AC Waveforms

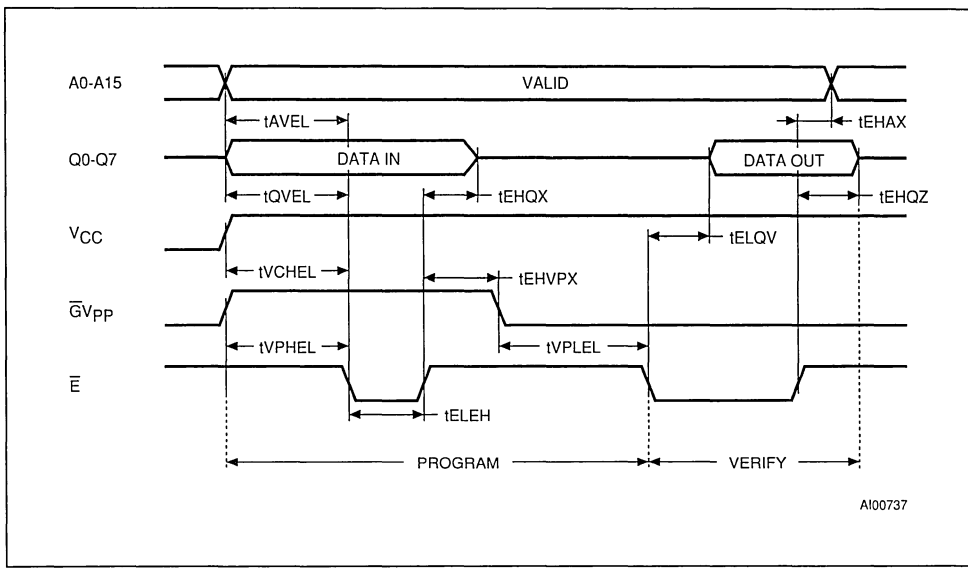
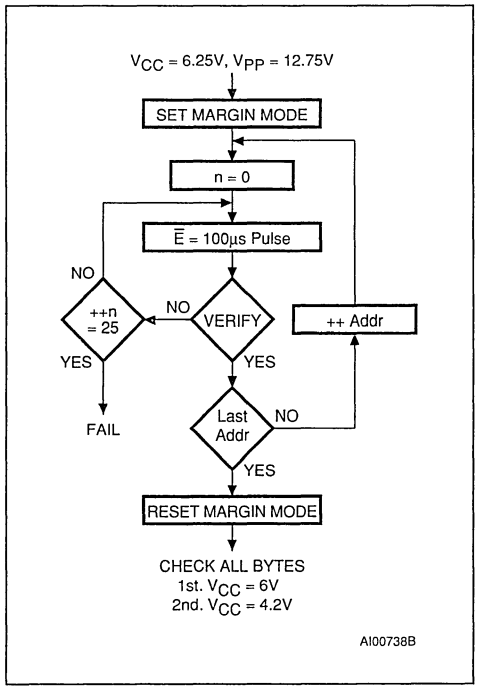


Figure 8. Programming Flowchart



Programming

The M27W512 has been designed to be fully compatible with the M27C512. As a result the M27W512 can be programmed as the M27W512 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27W512 has the same electronic signature and uses the same PRESTO IIB algorithm.

When delivered, all bits of the M27W512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The M27W512 is in the programming mode when V_{PP} input is at 12.75V and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

The M27W512 uses the PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically less than 6 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used as well.

PRESTO IIB Programming Algorithm

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, a typical time of 6.5 seconds. This can be achieved with SGS-THOMSON M27W512 due to several design innovations to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 100µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

Program Inhibit

Programming of multiple M27W512s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}V_{PP}$ of the parallel M27W512 may be common. A TTL low level pulse applied to a M27W512's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27W512. A high level $\overline{E}$ input inhibits the other M27W512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

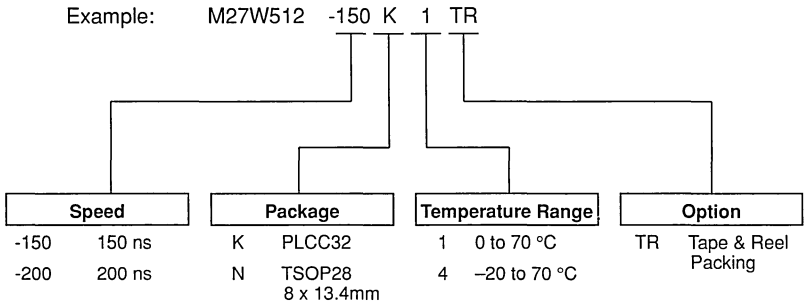
Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27W512. To activate this mode, the programming equipment must apply a Supply Voltage V_{CC} of 5V and force 11.5V to 12.5V on address line A9 of the M27W512.

Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27W512, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

Note that the M27W512 and the M27C512 have the same identifier bytes.

ORDERING INFORMATION SCHEME



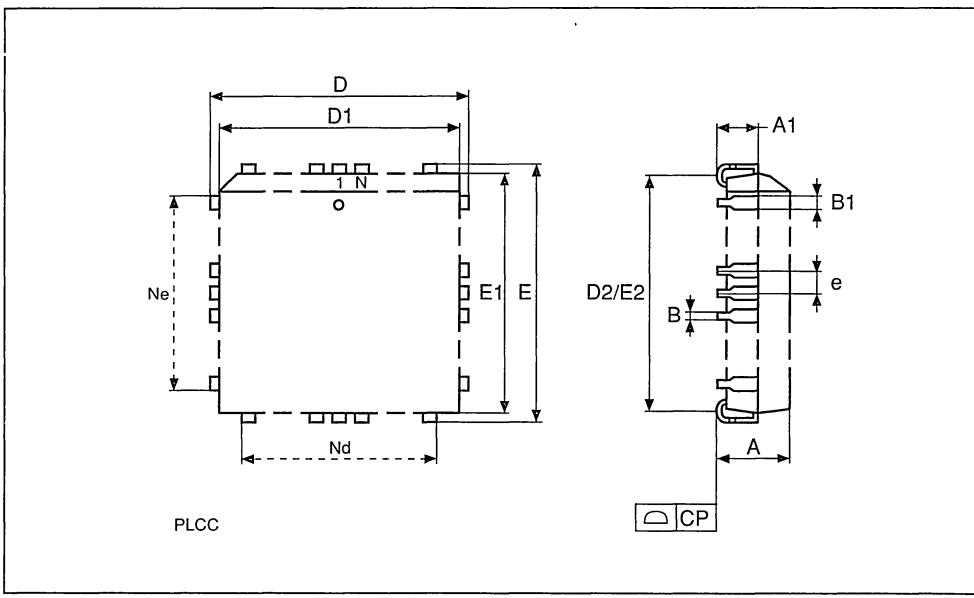
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

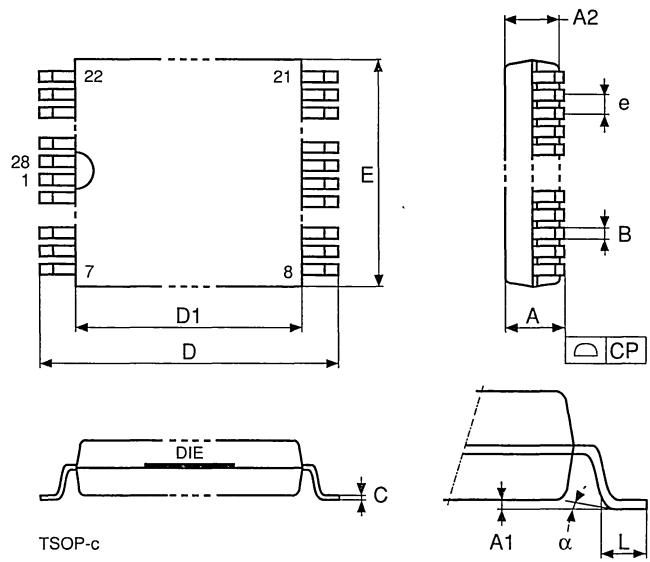


Drawing is out of scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004

TSOP28

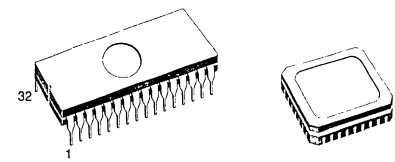


TSOP-c

Drawing is out of scale

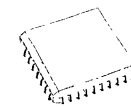
1 Megabit (128K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 55ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 12sec. (PRESTO II ALGORITHM)



FDIP32W (F)

LCCC32W (L)



PLCC32 (C)

TSOP32 (N)
8 x 20mm

DESCRIPTION

The M27C1001 is a high speed 1 Megabit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems requiring large programs. It is organized as 131,072 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27C1001 is offered in both Plastic Dual-in-Line, Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

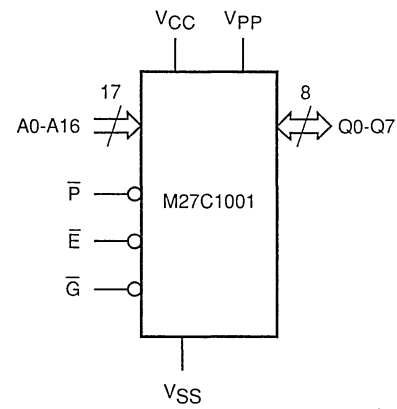
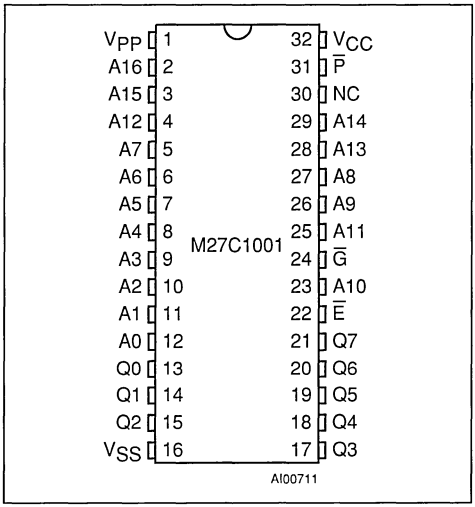
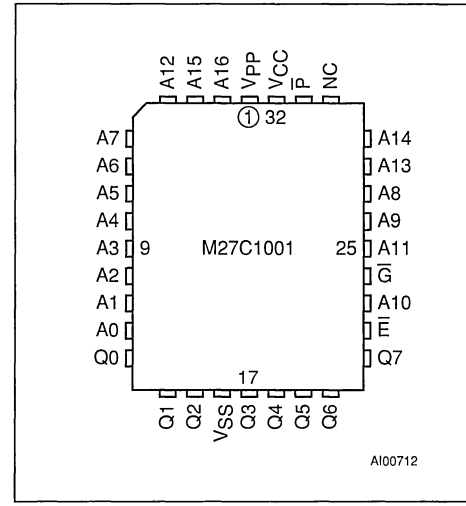


Figure 2A. DIP Pin Connections



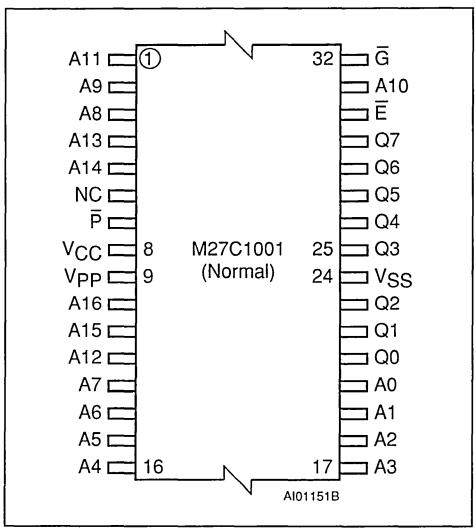
Warning: NC = No Connection.

Figure 2B. LCC Pin Connections



Warning: NC = No Connection.

Figure 2C. TSOP Pin Connections



Warning: NC = No Connection.

DEVICE OPERATION

The modes of operation of the M27C1001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C1001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C1001 has a standby mode which reduces the active current from 30mA to 100µA. The M27C1001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2 Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0 5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	1	05h

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

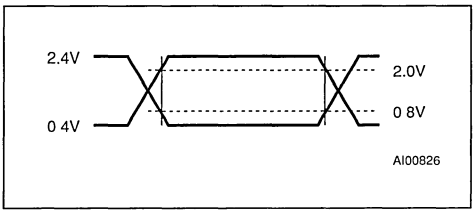
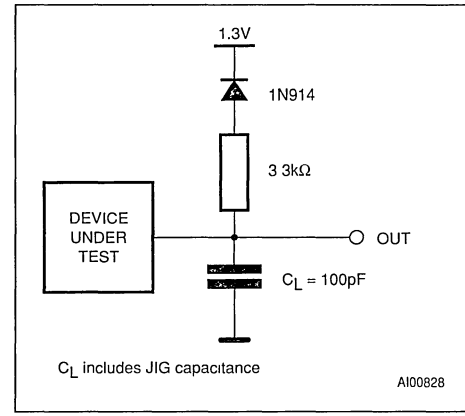


Figure 4. AC Testing Load Circuit



Note: For 55ns class: input pulse voltages are 0V to 3V, input output test points are at 1.5V, C_L is 30 pF.

Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Note: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Maximum DC voltage on Output is V_{CC} +0.5V

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1001								Unit
				-55		-60		-70		-80		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		55		60		70		80	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		55		60		70		80	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		30		35		35		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	25	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	25	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1001						Unit
				-90		-10		-12/-15/ -20/-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2 Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

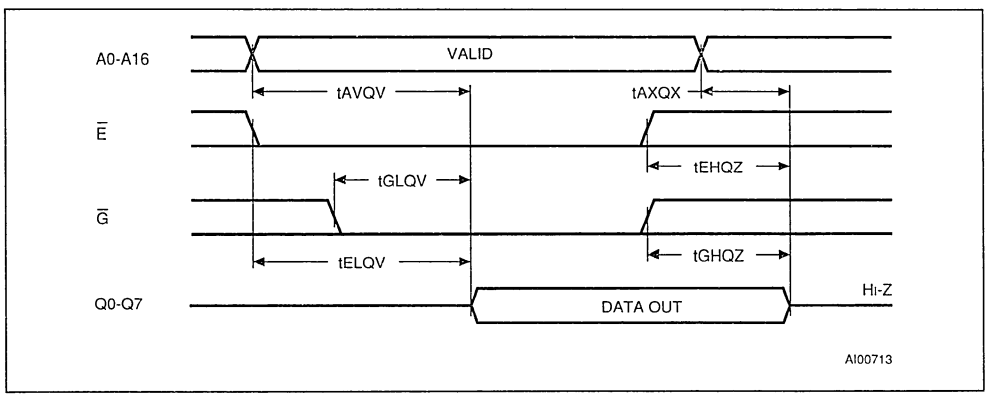


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

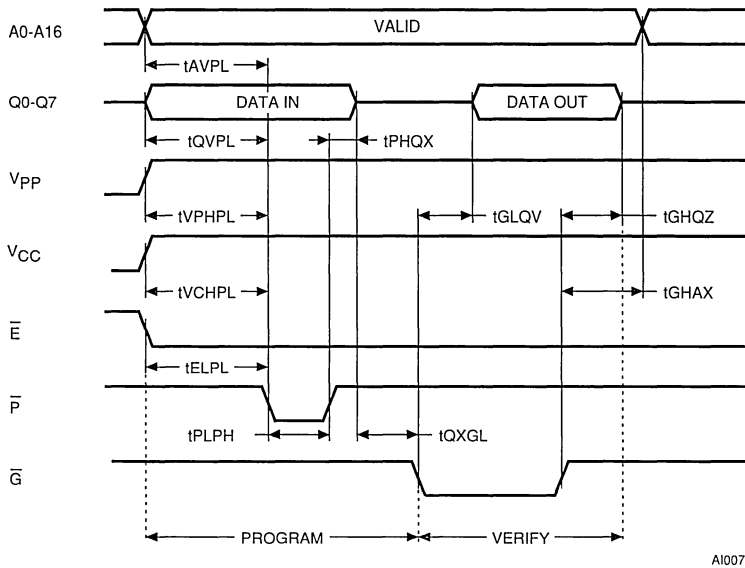
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



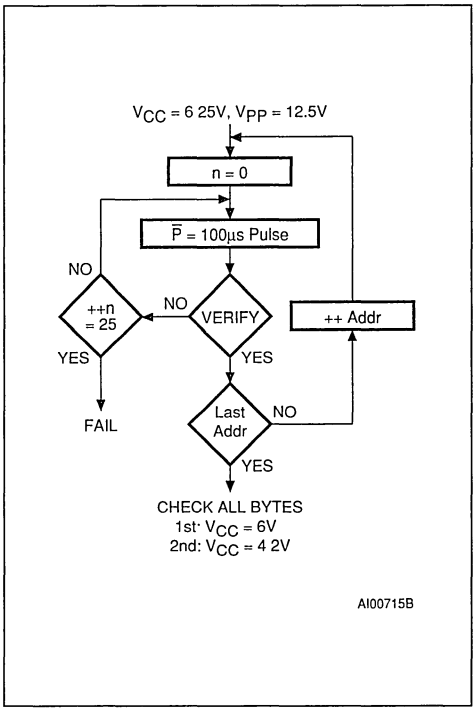
DEVICE OPERATION (cont'd)

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C1001 are in the '1' state. Data is introduced by selectively programming '0' into the desired bit locations. Although only '0' will be programmed, both '1' and '0' can be present in the data word. The only way to change a '0' to a '1' is by die exposition to ultraviolet light (UV EPROM). The M27C1001 is in the programming mode when V_{pp} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in a typical time of 13 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C1001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C1001 may be common. A TTL low level pulse applied to a M27C1001's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C1001. A high level $\overline{E}$ input inhibits the other M27C1001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1001, with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C1001, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C1001 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1001 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C1001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C1001 -70 X C 1 TR

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-55	55 ns	X	± 5%	F	FDIP32W	1	0 to 70 °C	X	Additional Burn-in
-60	60 ns	blank	± 10%	L	LCCC32W	3	–40 to 125 °C	TR	Tape & Reel Packing
-70	70 ns			B	PDIP32	6	–40 to 85 °C		
-80	80 ns			C	PLCC32				
-90	90 ns			N	TSOP32 8 x 20mm				
-10	100 ns								
-12	120 ns								
-15	150 ns								
-20	200 ns								
-25	250 ns								

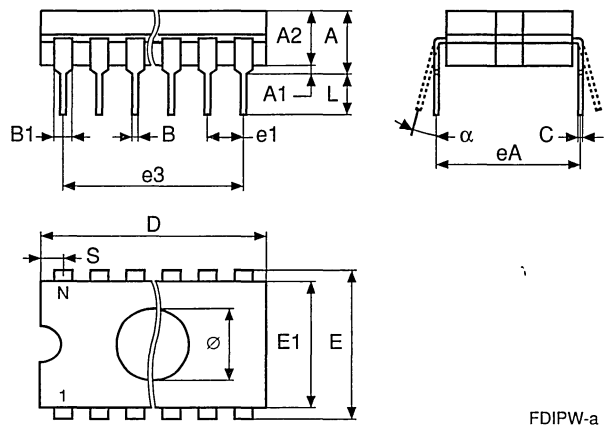
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP32W - 32 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			42.78			1.684
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	38.10	–	–	1.500	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	9.65	–	–	0.380	–	–
α		4°	15°		4°	15°
N	32			32		

FDIP32W



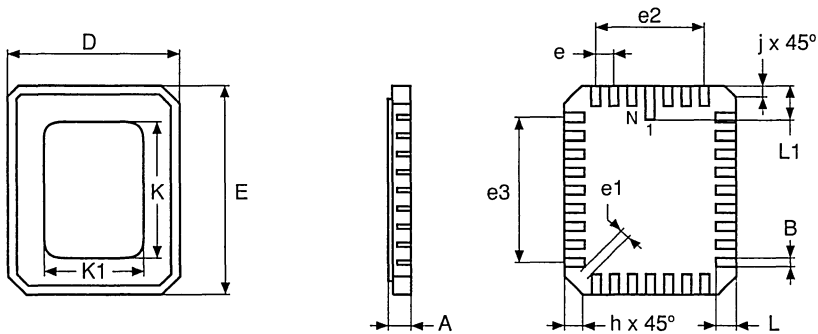
FDIPW-a

Drawing is out of scale

LCCC32W - 32 lead Leadless Ceramic Chip Carrier, square window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.28			0.090
B		0.51	0.71		0.020	0.028
D		11.23	11.63		0.442	0.458
E		13.72	14.22		0.540	0.560
e	1.27	–	–	0.050	–	–
e1		0.39	–		0.015	–
e2	7.62	–	–	0.300	–	–
e3	10.16	–	–	0.400	–	–
h	1.02	–	–	0.040	–	–
j	0.51	–	–	0.020	–	–
L		1.14	1.40		0.045	0.055
L1		1.96	2.36		0.077	0.093
K		10.50	10.80		0.413	0.425
K1		8.03	8.23		0.316	0.324
N	32			32		

LCCC32W



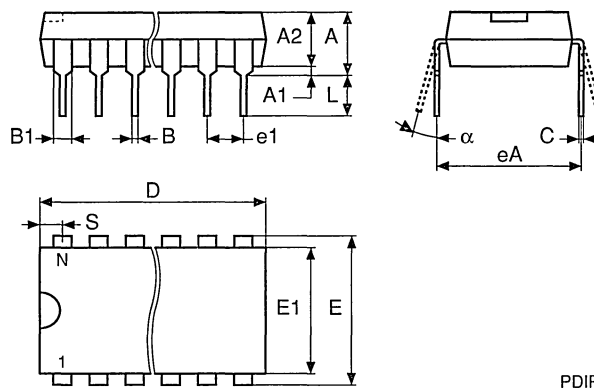
LCCCW-a

Drawing is out of scale

PDIP32 - 32 lead Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N	32			32		

PDIP32



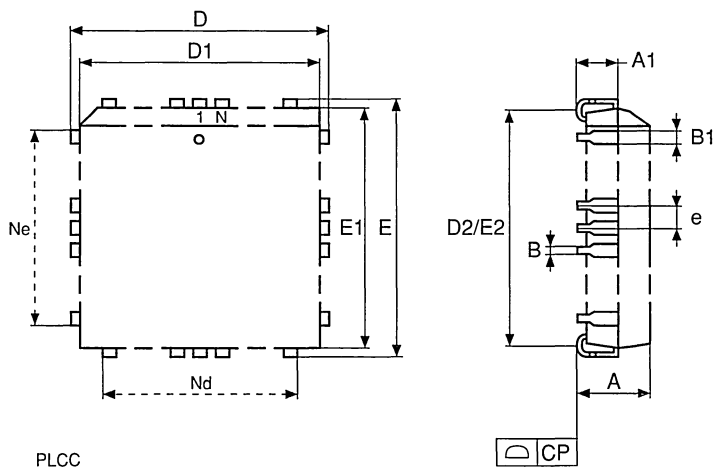
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

PLCC32

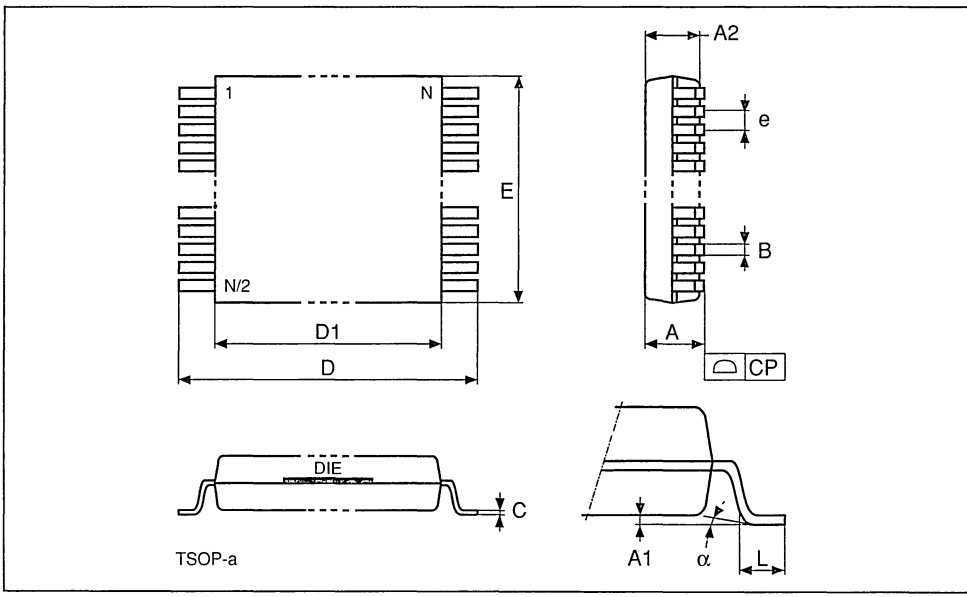


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32

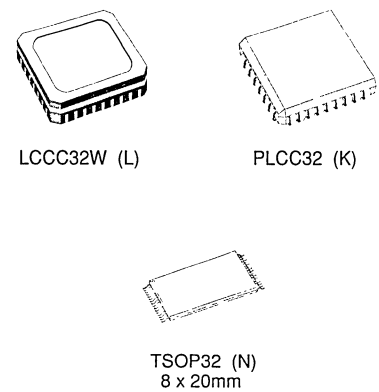


TSOP-a

Drawing is out of scale

LOW VOLTAGE 1 Megabit (128K x 8) UV EPROM and OTP ROM

- LOW VOLTAGE READ OPERATION: 3V to 5.5V
- ACCESS TIME: 120, 150 and 200ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES for SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32 and TSOP32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 12sec. (PRESTO II ALGORITHM)
- M27V101 is PROGRAMMABLE as M27C1001 with IDENTICAL SIGNATURE



DESCRIPTION

The M27V101 is a low voltage, low power 1 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 131,072 by 8 bits.

The M27V101 operates in the read mode with a supply voltage as low as 3V. The decrease in operating power allows either a reduction of the

Table 1. Signal Names

A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

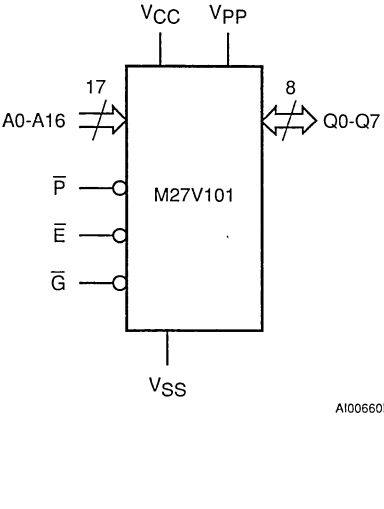
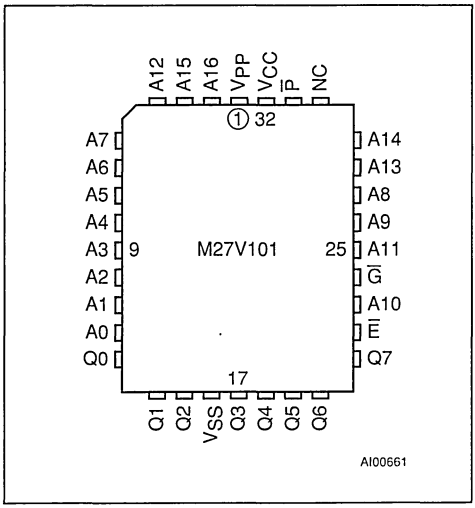
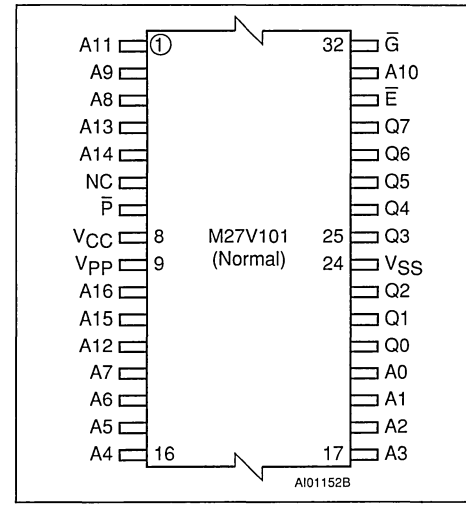


Figure 2A. LCC Pin Connections



Warning: NC = No Connection.

Figure 2B. TSOP Pin Connections



Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

size of the battery or an increase in the time between battery recharges. The M27V101 can also be operated as a standard 1 Megabit EPROM (similar to M27C1001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27V101 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

DEVICE OPERATION

The modes of operation of the M27V101 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27V101 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V101 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V101 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer:

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note. X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	1	05h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

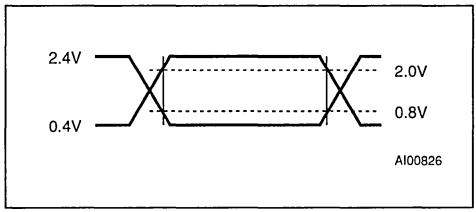


Figure 4. AC Testing Load Circuit

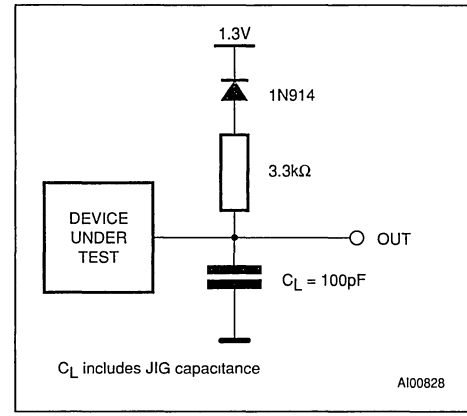


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 3.2V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0 5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27V101						Unit
				-120		-150		-200		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		80		85		90	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	70	0	70	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	70	0	70	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

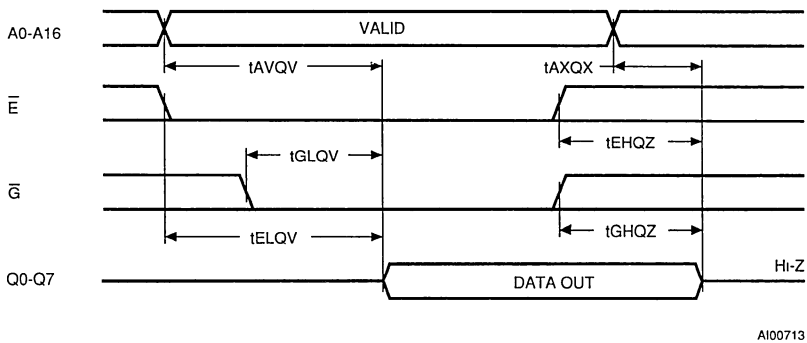


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

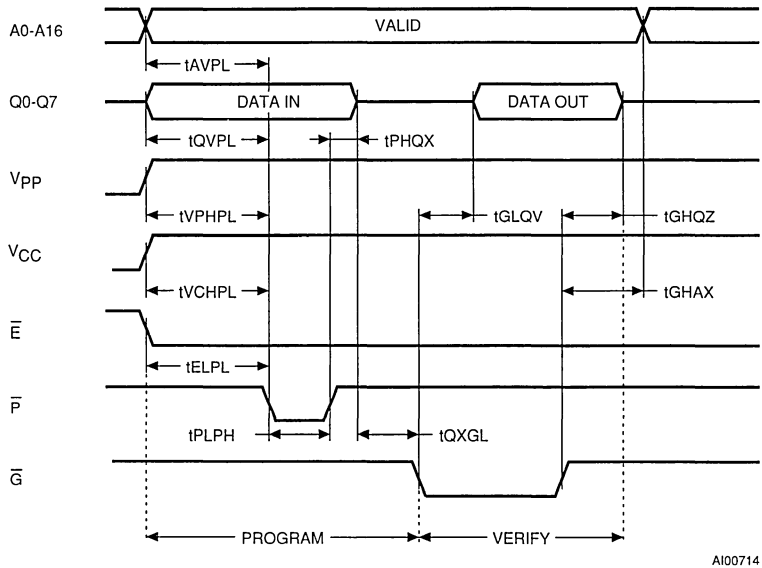
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



DEVICE OPERATION (cont'd)

the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

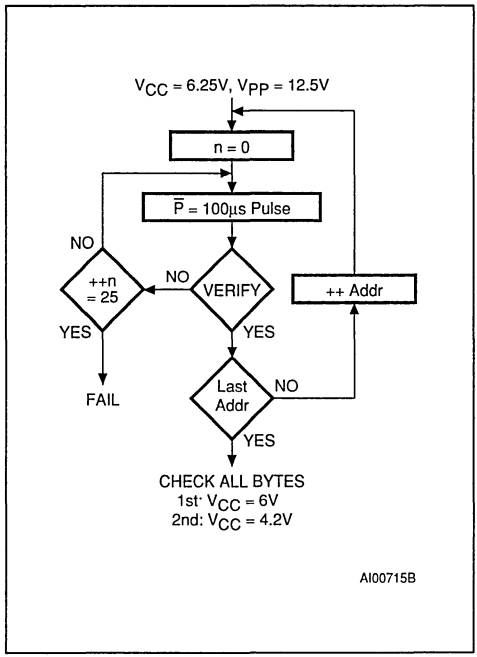
The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27V101 has been designed to be fully compatible with the M27C1001. As a result the M27V101 can be programmed as the M27C1001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V101 has the same electronic signature and uses the same PRESTO II algorithm .

When delivered (and after each erasure for UV EPROM), all bits of the M27V101 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27V101 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in a typical time of 13 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V101s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V101 may be common. A TTL low level pulse applied to a M27V101's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27V101. A high level $\overline{E}$ input inhibits the other M27V101s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

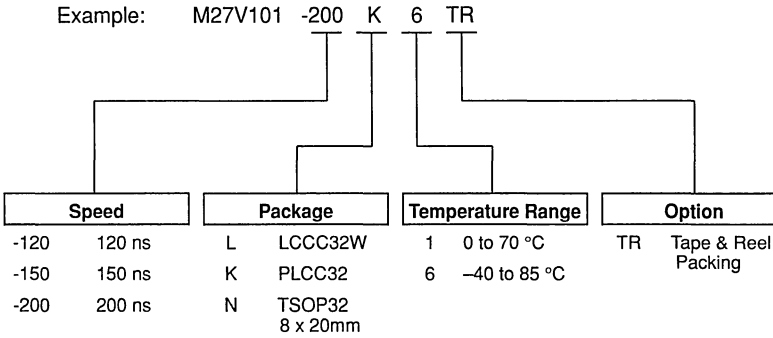
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V101. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V101, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27V101, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7. Note that the M27V101 and M27C1001 have the same identifier bytes .

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V101 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V101 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V101 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V101 window to prevent unintentional erasure. The recommended erasure procedure for the M27V101 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27V101 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME



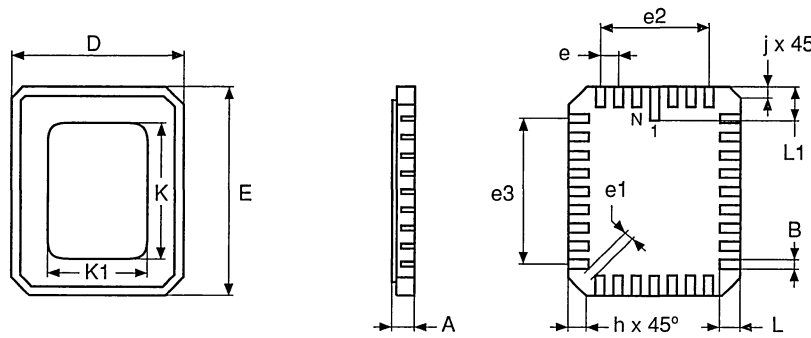
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

LCCC32W - 32 lead Leadless Ceramic Chip Carrier, square window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.28			0.090
B		0.51	0.71		0.020	0.028
D		11.23	11.63		0.442	0.458
E		13.72	14.22		0.540	0.560
e	1.27	–	–	0.050	–	–
e1		0.39	–		0.015	–
e2	7.62	–	–	0.300	–	–
e3	10.16	–	–	0.400	–	–
h	1.02	–	–	0.040	–	–
j	0.51	–	–	0.020	–	–
L		1.14	1.40		0.045	0.055
L1		1.96	2.36		0.077	0.093
K		10.50	10.80		0.413	0.425
K1		8.03	8.23		0.316	0.324
N	32			32		

LCCC32W



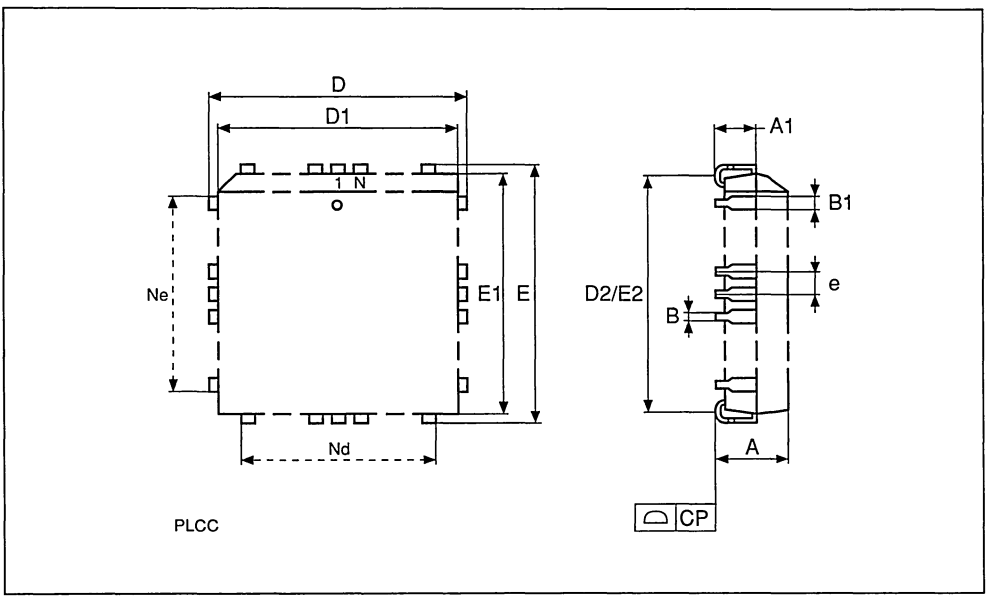
LCCCW-a

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

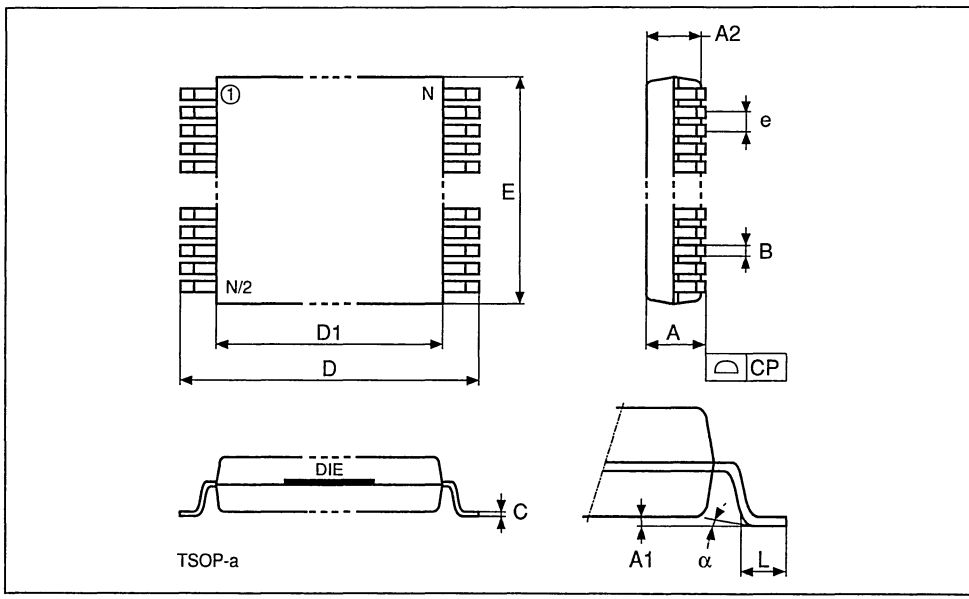


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32

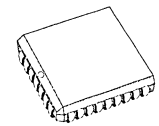


TSOP-a

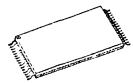
Drawing is out of scale

VERY LOW VOLTAGE 1 Megabit (128K x 8) OTP ROM

- VERY LOW VOLTAGE READ OPERATION: 2.7V to 5.5V
- ACCESS TIME:
  - 150ns (T_A = 0 to 70 °C)
  - 200ns (T_A = –20 to 70 °C)
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 12sec. (PRESTO II ALGORITHM)
- M27W101 is PROGRAMMABLE as M27C1001 with IDENTICAL SIGNATURE



PLCC32 (K)



TSOP32 (N)
8 x 20mm

DESCRIPTION

The M27W101 is a very low voltage, low power 1 Megabit One Time Programmable ROM, ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 131,072 by 8 bits.

The M27W101 operates in the read mode with a supply voltage as low as 2.7V at –20 to 70 °C temperature range. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges. The M27W101 can also be operated as a standard 1 Megabit EPROM (similar to M27C1001) with a 5V power supply.

Table 1. Signal Names

A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

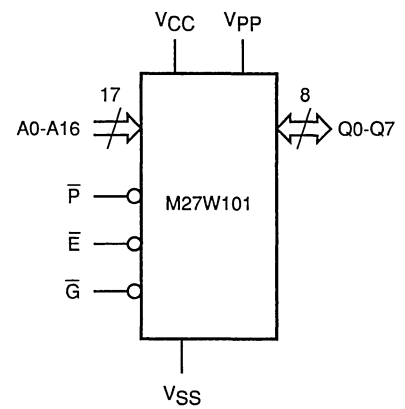
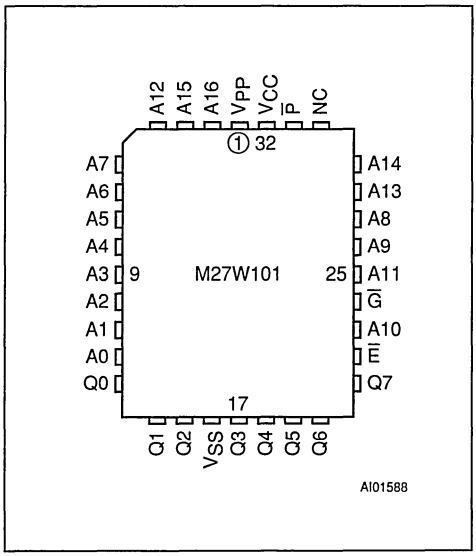
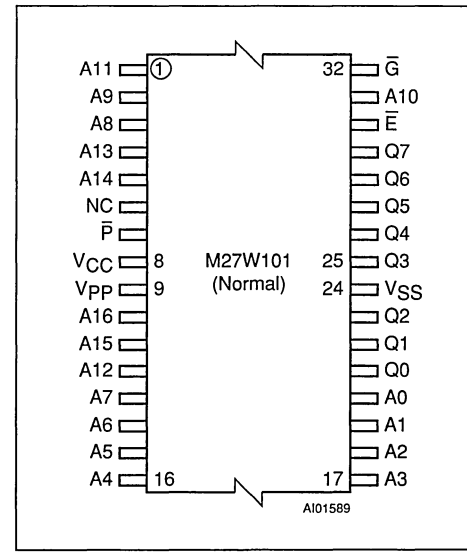


Figure 2A. LCC Pin Connections



Warning: NC = No Connection.

Figure 2B. TSOP Pin Connections



Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–20 to 70	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

For applications where the content is programmed only one time and erasure is not required, the M27W101 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

DEVICE OPERATION

The modes of operation of the M27W101 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27W101 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27W101 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 2.7V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27W101 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because OTP ROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS OTP ROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	0	1	05h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

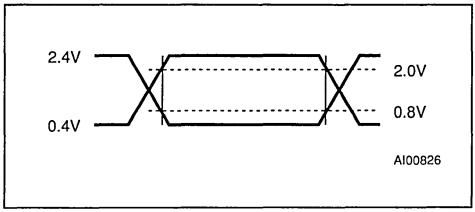


Figure 4. AC Testing Load Circuit

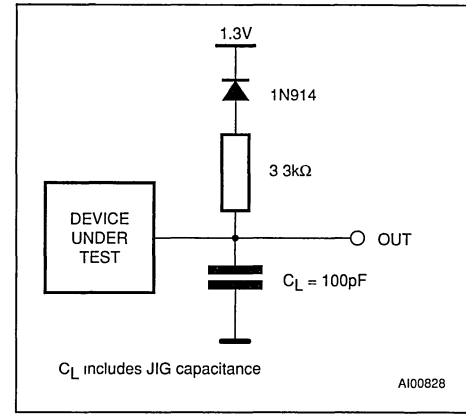


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = –20 to 70 °C; V_{CC} = 2.7V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 2.7V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 2.7V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = –20 to 70 °C; V_{CC} = 2.7V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27W101				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		75		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	70	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	70	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

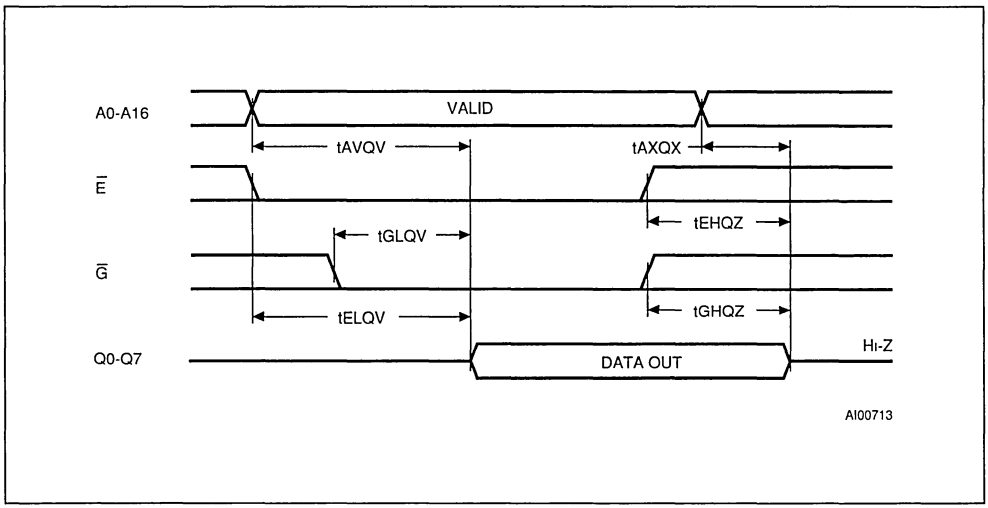


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

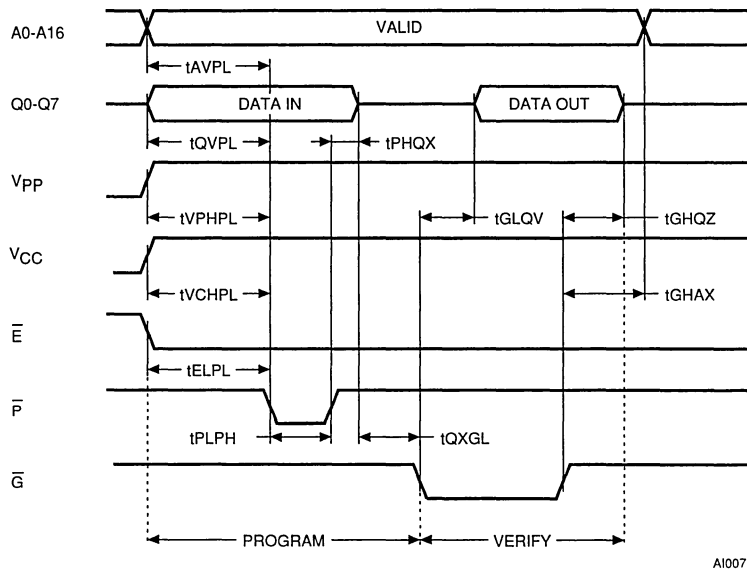
Note: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms



DEVICE OPERATION (cont'd)

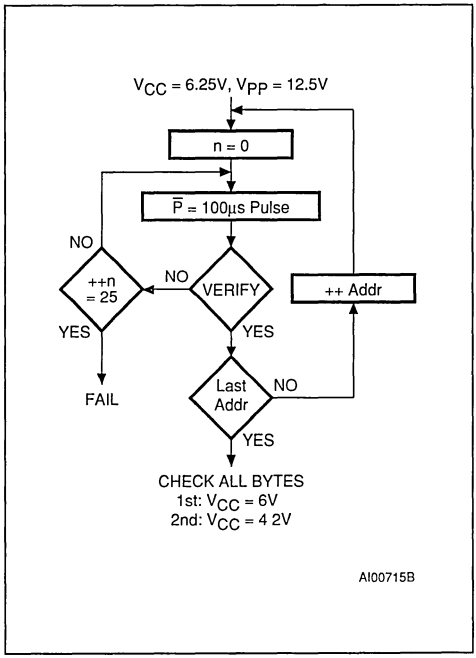
The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27W101 has been designed to be fully compatible with the M27C1001. As a result the M27W101 can be programmed as the M27C1001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27W101 has the same electronic signature and uses the same PRESTO II algorithm .

When delivered, all bits of the M27W101 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The M27W101 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in a typical time of 13 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27VW01s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27W101 may be common. A TTL low level pulse applied to a M27W101's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27W101. A high level $\overline{E}$ input inhibits the other M27W101s from being programmed.

Program Verify

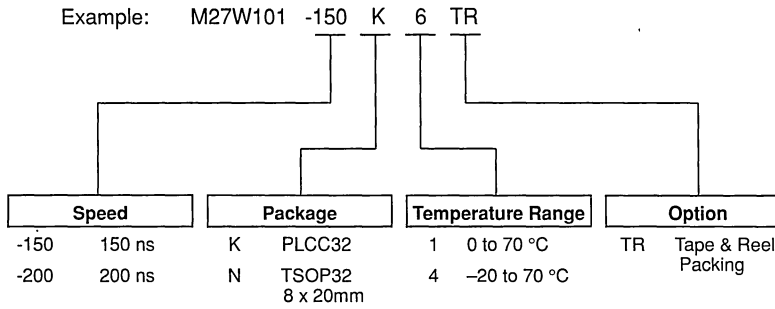
A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27W101. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27W101, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27W101, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7. Note that the M27W101 and M27C1001 have the same identifier bytes .

ORDERING INFORMATION SCHEME



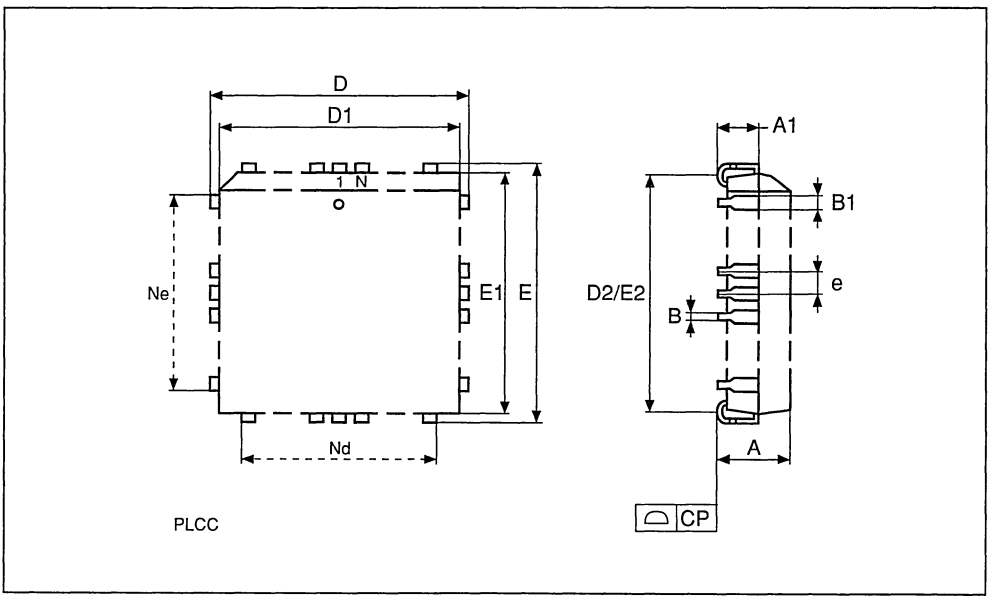
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

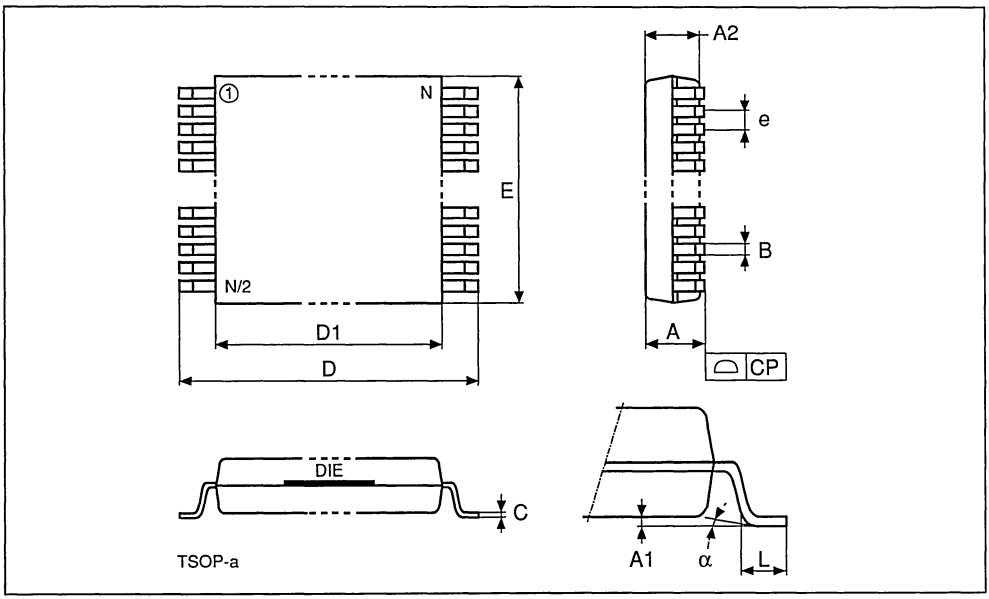


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.004

TSOP32



TSOP-a

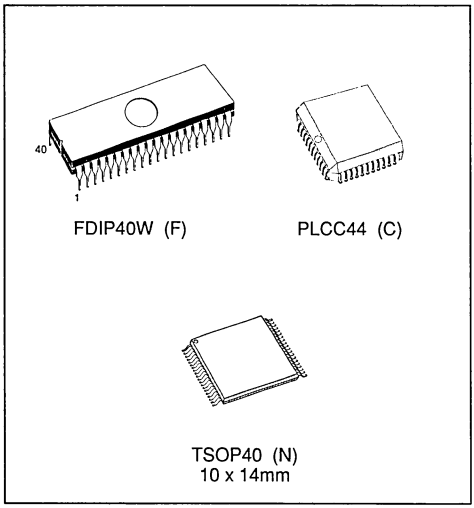
Drawing is out of scale

SGS-THOMSON MICROELECTRONICS

M27C1024

1 Megabit (64K x16) UV EPROM and OTP ROM

- FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 35mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIME of AROUND 6 sec. (PRESTO II ALGORITHM)



FDIP40W (F)

PLCC44 (C)

TSOP40 (N)
10 x 14mm

DESCRIPTION

The M27C1024 is a 1 Megabit UV erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 16 bits.

The 40 pin Ceramic Frit Seal Window package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For application where the content is programmed only one time and erasure is not required, the M27C1024 is offered in a Plastic Leaded Chip Carrier package.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

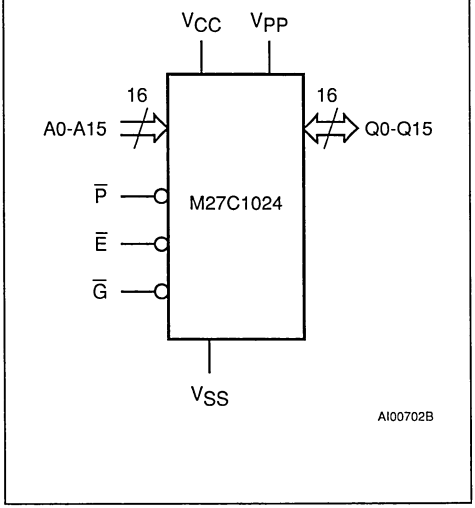
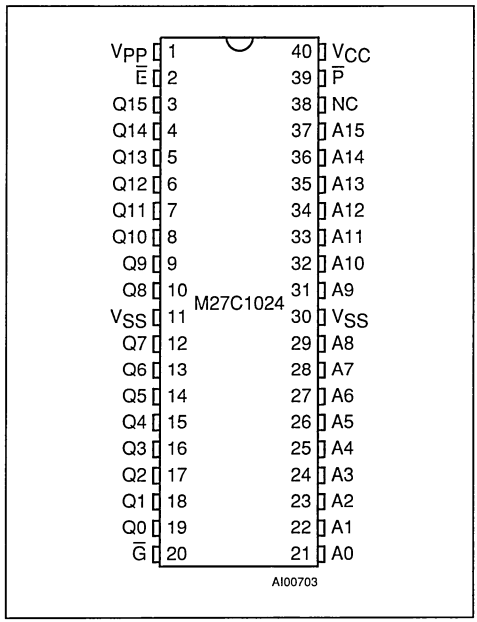
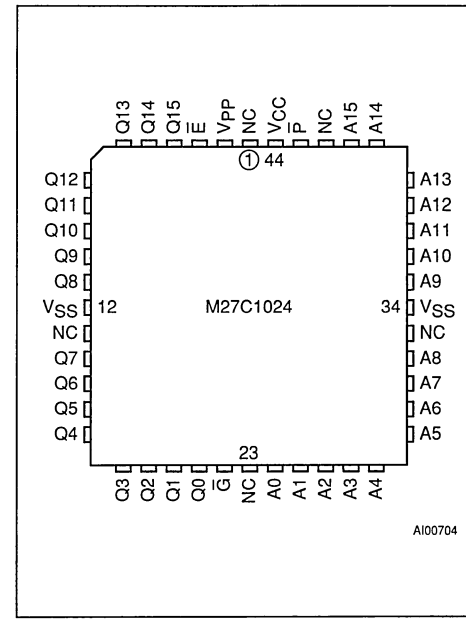


Figure 2A. DIP Pin Connections



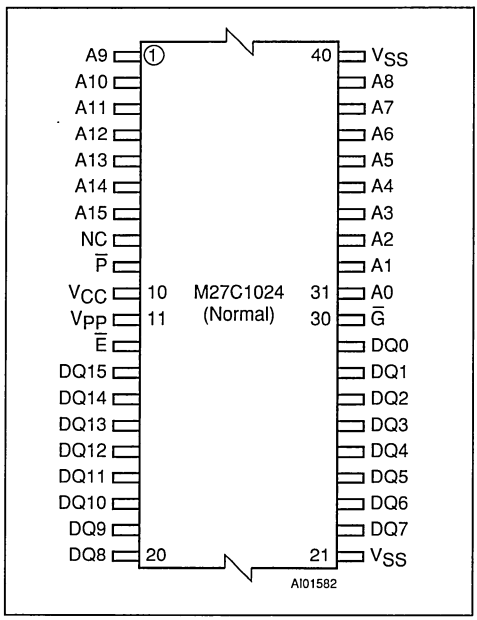
Warning: NC = No Connection.

Figure 2B. LCC Pin Connections



Warning: NC = No Connection.

Figure 2C. TSOP Pin Connections



Warning: NC = No Connection.

DEVICE OPERATION

The modes of operations of the M27C1024 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for Vpp and 12V on A9 for Electronic Signature.

Read Mode

The M27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C1024 has a standby mode which reduces the active current from 35mA to 100µA.

The M27C1024 is placed in the standby mode by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q15
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Data Output
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	X	V_{IL} Pulse	X	V_{PP}	Data Input
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Output
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ±0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	0	0	1	1	0	0	8Ch

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

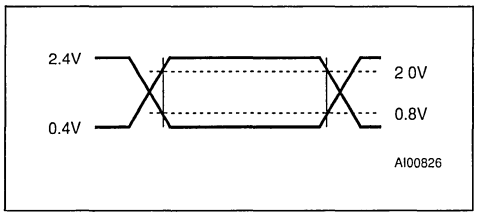


Figure 4. AC Testing Load Circuit

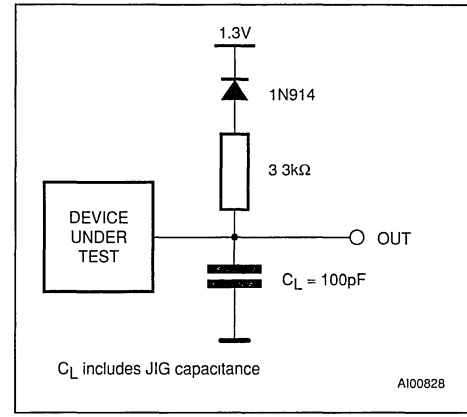


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 105 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		35	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}
2 Maximum DC voltage on Output is V_{CC} +0.5V

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 105 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1024								Unit
				-70		-80		-90		-10		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		80		90		100	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		80		90		100	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		45		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

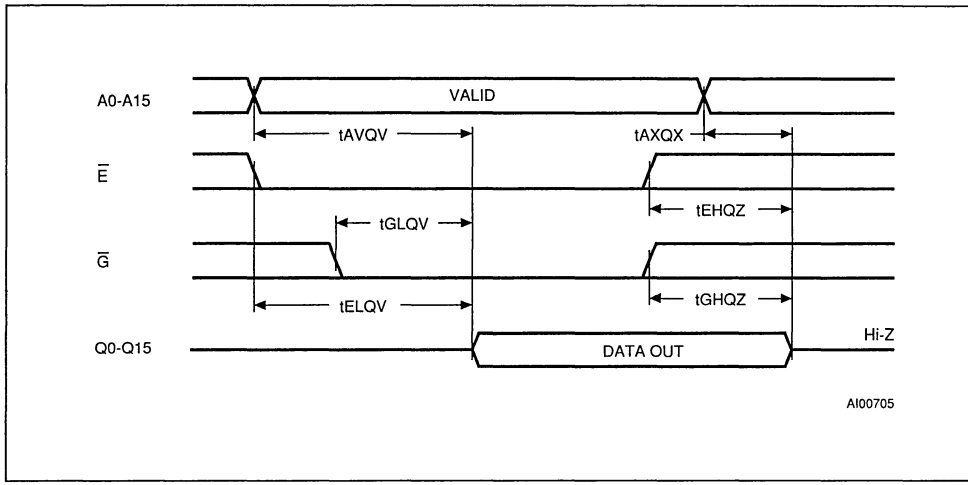
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}
2 Sampled only, not 100% tested.

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 105 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C1024						Unit
				-12		-15		-20/-25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		60		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	50	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}
2 Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms



System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between Vcc and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C1024 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C1024 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied, 16 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

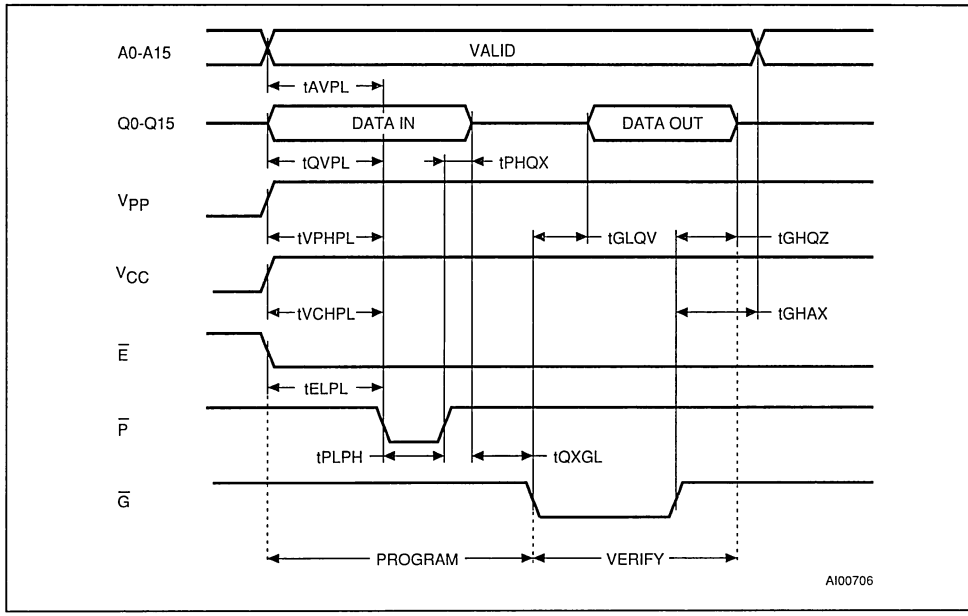
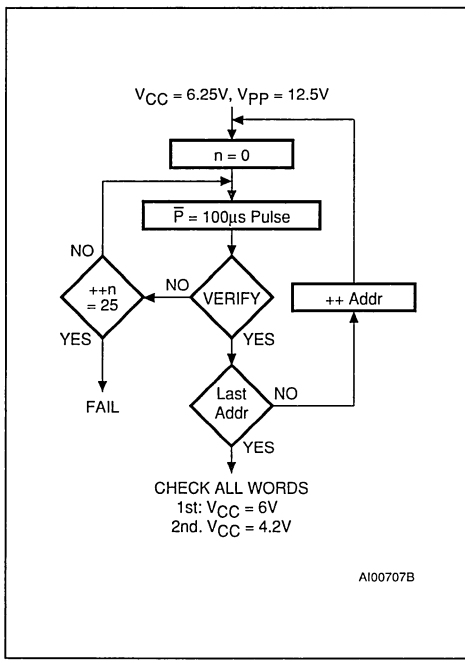


Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows programming of the whole array with a guaranteed margin, in a typical time of 6.5 seconds. Programming with PRESTO II consists of applying a sequence of 100 µs program pulses to each word until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C1024s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C1024 may be common. A TTL low level pulse applied to a M27C1024's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C1024. A high level $\overline{E}$ input inhibits the other M27C1024s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1024. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1024 with V_{PP} = V_{CC} = 5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C1024, these two iden-tifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C1024 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1024 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1024 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1024 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1024 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C1024 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C1024 -12 X F 1 X

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-70	70ns	X	± 5%	F	FDIP40W	1	0 to 70 °C	X	Additional Burn-in
-80	80ns	blank	± 10%	C	PLCC44	6	–40 to 85 °C	TR	Tape & Reel Packing
-90	90ns			N	TSOP40 10 x 14mm	7	–40 to 105 °C		
-10	100ns								
-12	120ns								
-15	150ns								
-20	200ns								
-25	250ns								

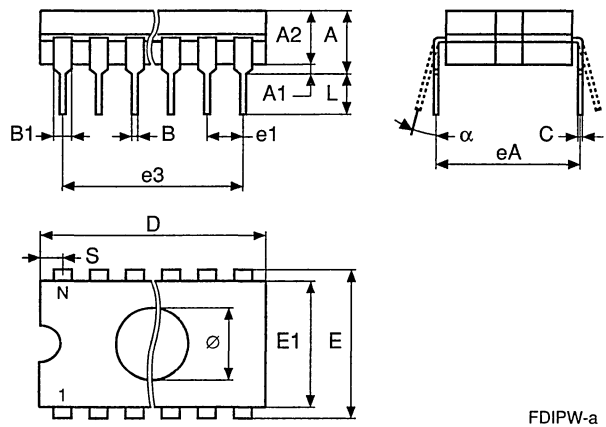
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP40W - 40 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			53.40			2.102
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	48.26	–	–	1.900	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	9.65	–	–	0.380	–	–
α		4°	15°		4°	15°
N		40			40	

FDIP40W



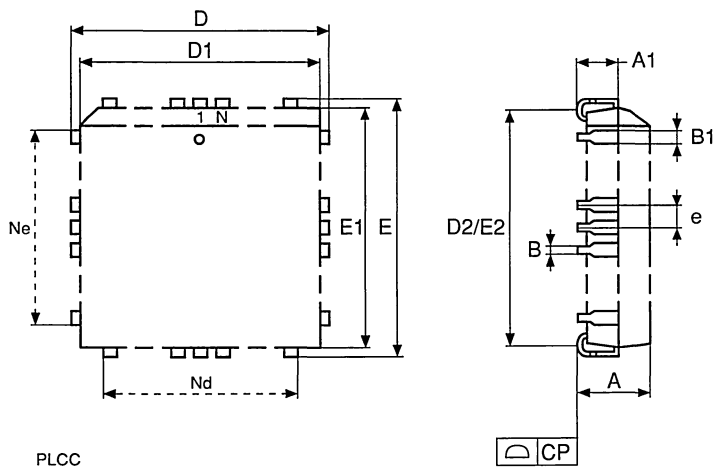
FDIPW-a

Drawing is out of scale

PLCC44 - 44 lead Plastic Leaded Chip Carrier, square

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		4.20	4.70		0.165	0.185
A1		2.29	3.04		0.090	0.120
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		17.40	17.65		0.685	0.695
D1		16.51	16.66		0.650	0.656
D2		14.99	16.00		0.590	0.630
E		17.40	17.65		0.685	0.695
E1		16.51	16.66		0.650	0.656
E2		14.99	16.00		0.590	0.630
e	1.27	–	–	0.050	–	–
N		44			44	
CP			0.10			0.004

PLCC44



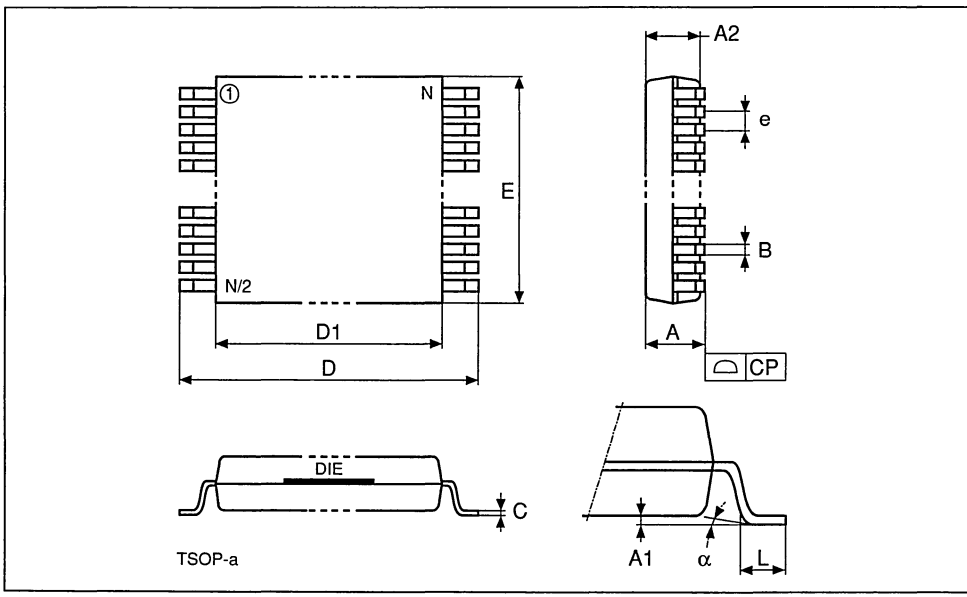
PLCC

Drawing is out of scale

TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 14mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.80	14.20		0.543	0.559
D1		12.30	12.50		0.484	0.492
E		9.90	10.10		0.390	0.398
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		40			40	
CP			0.10			0.004

TSOP40

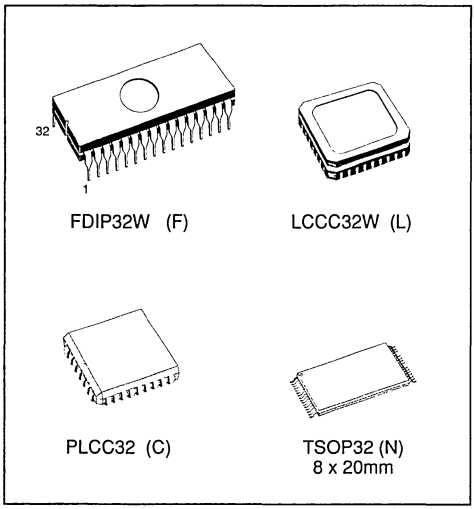


TSOP-a

Drawing is out of scale

2 Megabit (256K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C2001 is a high speed 2 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 262,144 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C2001 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

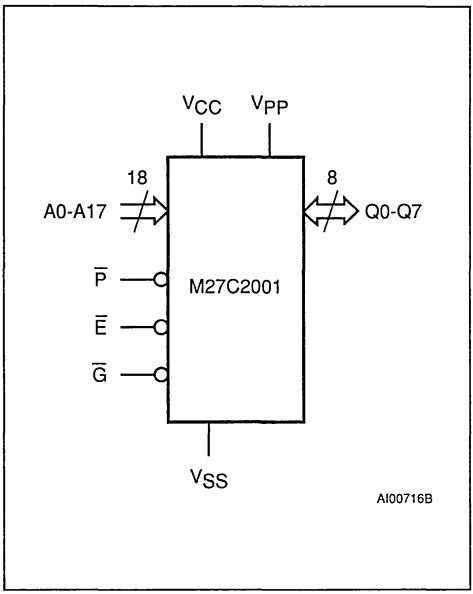


Figure 2A. DIP Pin Connections

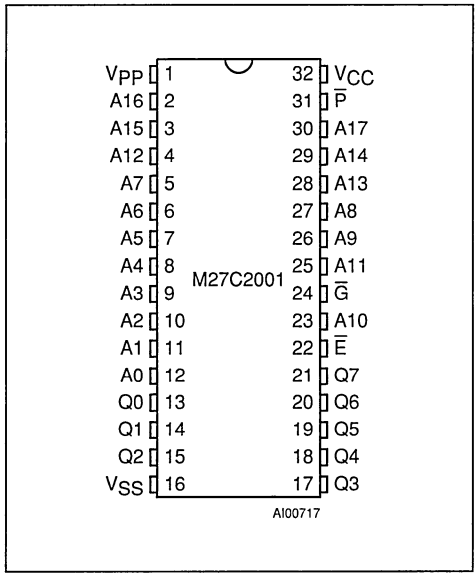


Figure 2B. LCC Pin Connections

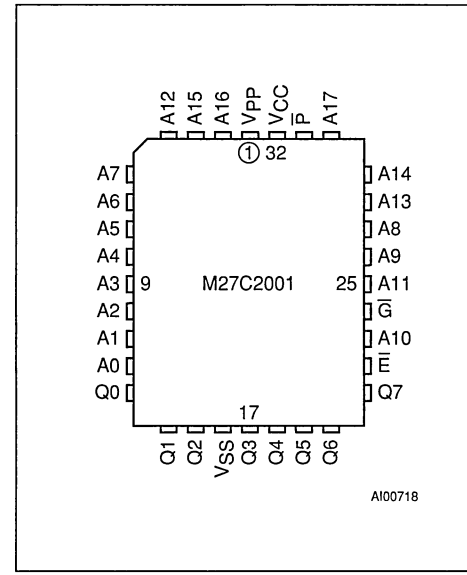
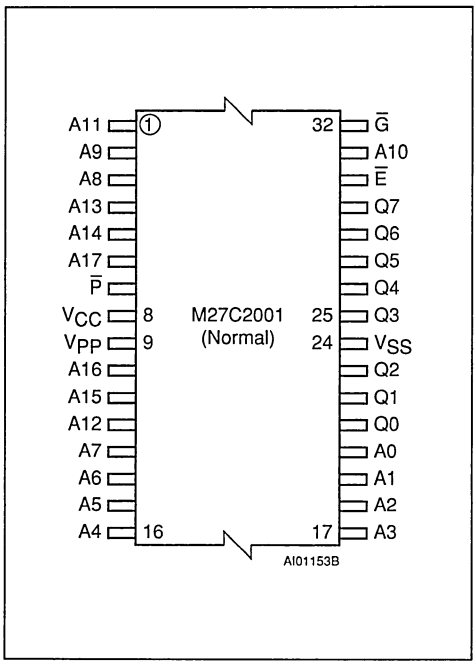


Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operations of the M27C2001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C2001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C2001 has a standby mode which reduces the active current from 30mA to 100µA. The M27C2001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	1	0	0	0	0	1	61h

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,
b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

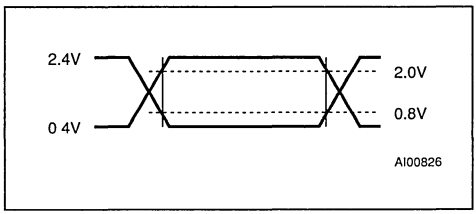


Figure 4. AC Testing Load Circuit

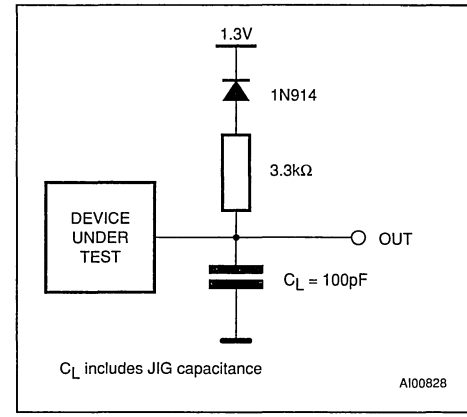


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C2001						Unit
				-70		-80		-90		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		80		90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C2001						Unit
				-10		-12		-15/-20/ -25		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

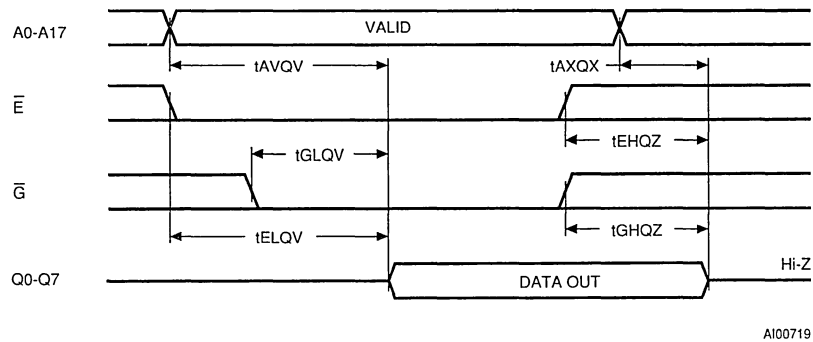


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

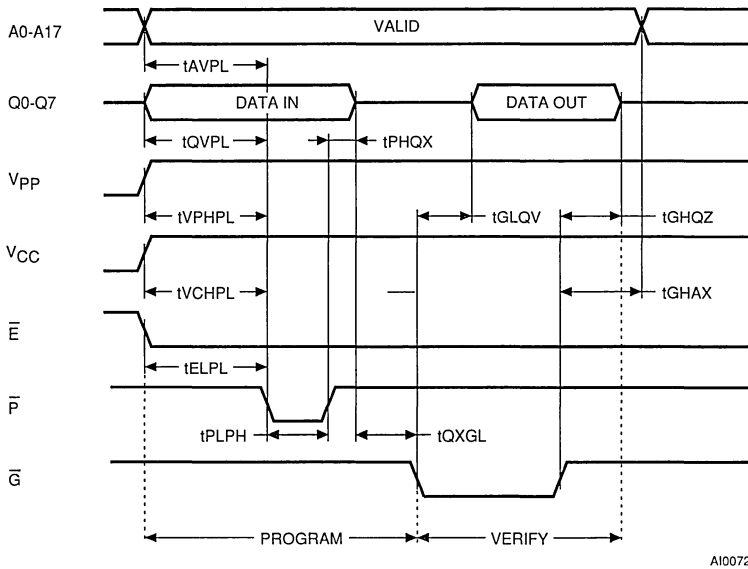
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 Sampled only, not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms



System Considerations

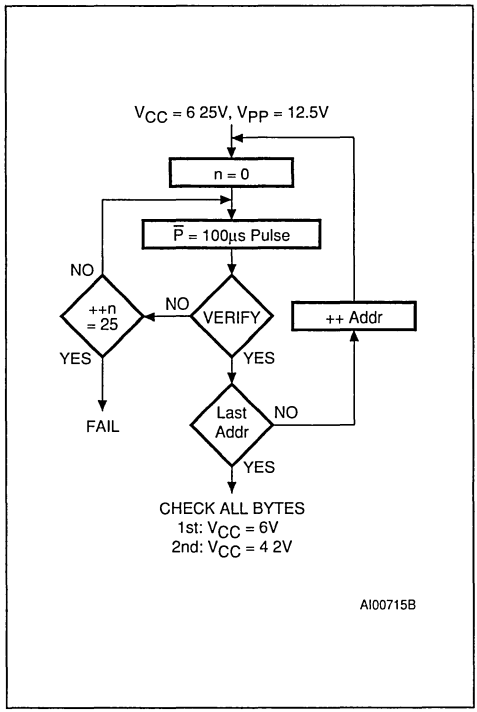
The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C2001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C2001 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 26.5 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C2001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C2001 may be common. A TTL low level pulse applied to a M27C2001's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27C2001. A high level $\overline{E}$ input inhibits the other M27C2001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C2001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C2001 with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C2001, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C2001 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C2001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C2001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C2001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C2001 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C2001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C2001 -80 X F 1 X

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-70	70 ns	X	± 5%	F	FDIP32W	1	0 to 70 °C	X	Additional Burn-in
-80	80 ns	blank	± 10%	L	LCCC32W	6	–40 to 85 °C	TR	Tape & Reel Packing
-90	90 ns			C	PLCC32				
-10	100 ns			N	TSOP32 8 x 20mm				
-12	120 ns								
-15	150 ns								
-20	200 ns								
-25	250 ns								

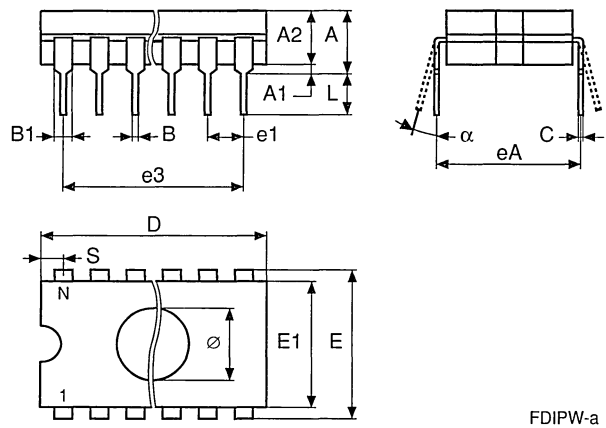
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP32W - 32 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			42.78			1.684
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	38.10	–	–	1.500	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	9.65	–	–	0.380	–	–
α		4°	15°		4°	15°
N	32			32		

FDIP32W



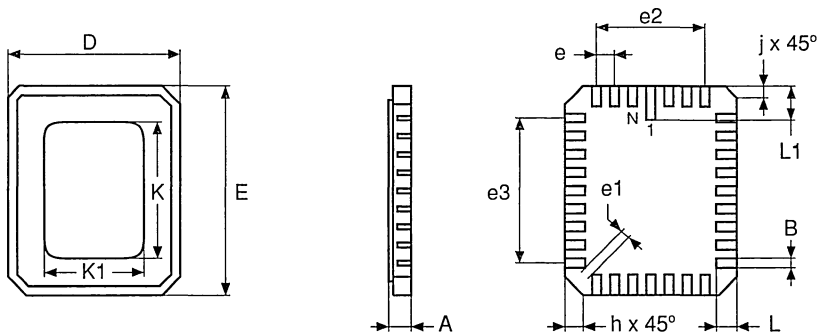
FDIPW-a

Drawing is out of scale

LCCC32W - 32 lead Leadless Ceramic Chip Carrier, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.28			0.090
B		0.51	0.71		0.020	0.028
D		11.23	11.63		0.442	0.458
E		13.72	14.22		0.540	0.560
e	1.27	–	–	0.050	–	–
e1		0.39	–		0.015	–
e2	7.62	–	–	0.300	–	–
e3	10.16	–	–	0.400	–	–
h	1.02	–	–	0.040	–	–
j	0.51	–	–	0.020	–	–
L		1.14	1.40		0.045	0.055
L1		1.96	2.36		0.077	0.093
K		10.50	10.80		0.413	0.425
K1		8.03	8.23		0.316	0.324
N	32			32		

LCCC32W



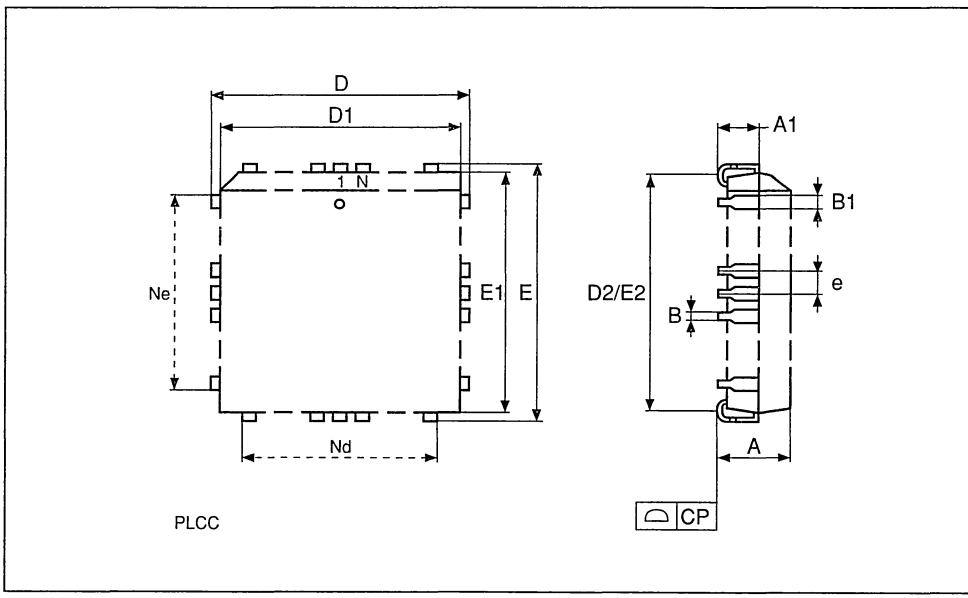
LCCCW-a

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

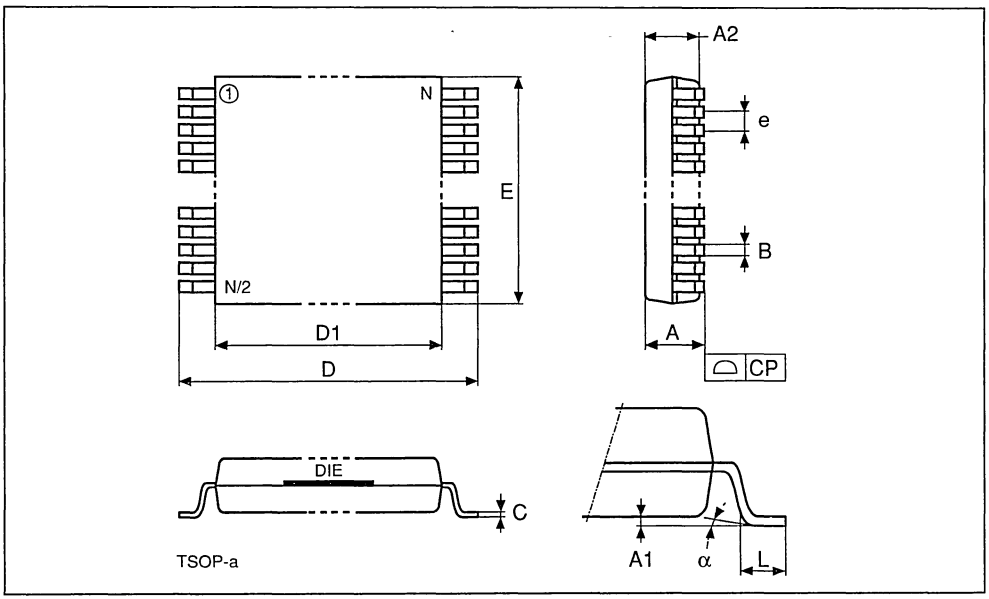


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32



TSOP-a

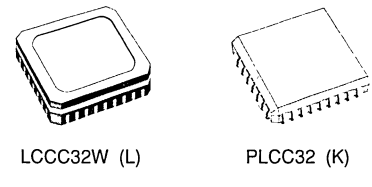
Drawing is out of scale

SGS-THOMSON MICROELECTRONICS

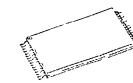
M27V201

LOW VOLTAGE 2 Megabit (256K x 8) UV EPROM and OTP ROM

- LOW VOLTAGE READ OPERATION: 3V to 5.5V
- ACCESS TIME: 200 and 250ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES for SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32 and TSOP32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)
- M27V201 is PROGRAMMABLE as M27C2001 with IDENTICAL SIGNATURE



LCCC32W (L) PLCC32 (K)



TSOP32 (N)
8 x 20mm

DESCRIPTION

The M27V201 is a low voltage, low power 2 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 262,144 by 8 bits.

The M27V201 operates in the read mode with a supply voltage as low as 3V. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

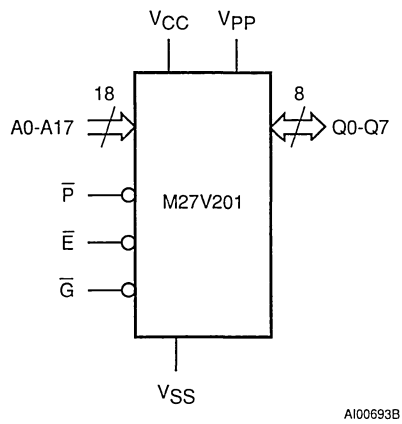


Figure 2A. LCC Pin Connections

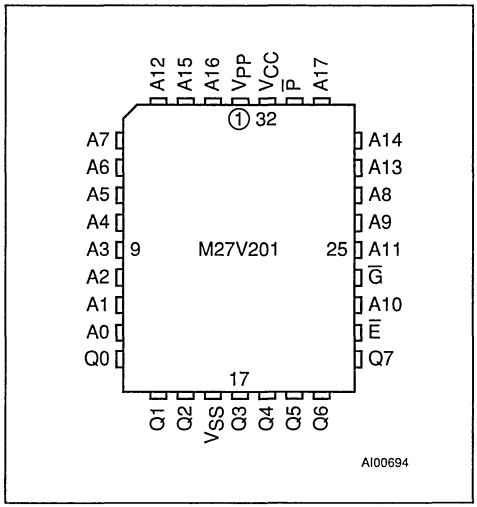


Figure 2B. TSOP Pin Connections

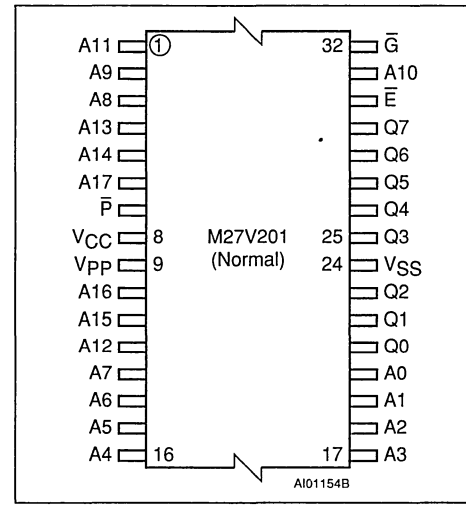


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns

DESCRIPTION (cont'd)

The M27V201 can also be operated as a standard 2 Megabit EPROM (similar to M27C2001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27V201 is offered in both Plastic Leaded Chip Carrier and Plastic thin Small Outline packages.

DEVICE OPERATION

The modes of operation of the M27V201 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27V201 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V201 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V201 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer:

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	1	0	0	0	0	1	61h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

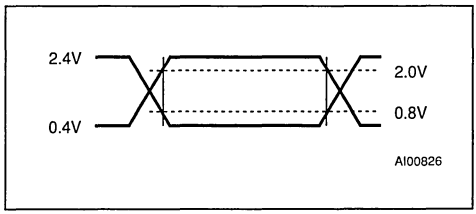


Figure 4. AC Testing Load Circuit

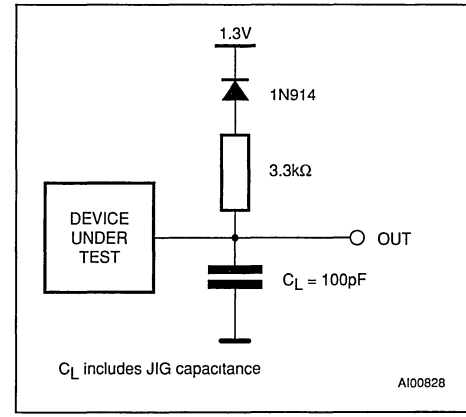


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 3.2V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27V201				Unit
				-200		-250		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		100		120	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	80	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	80	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

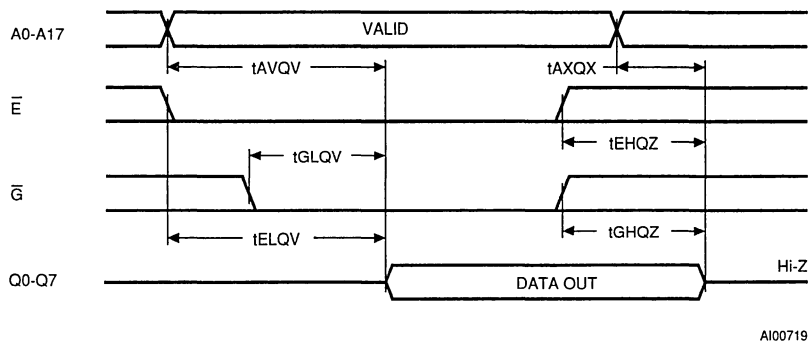


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

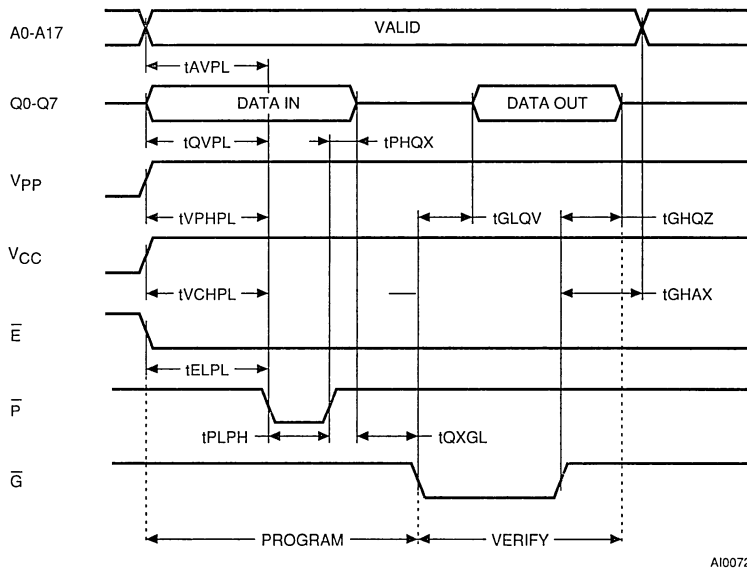
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2 Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



DEVICE OPERATION (cont'd)

the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

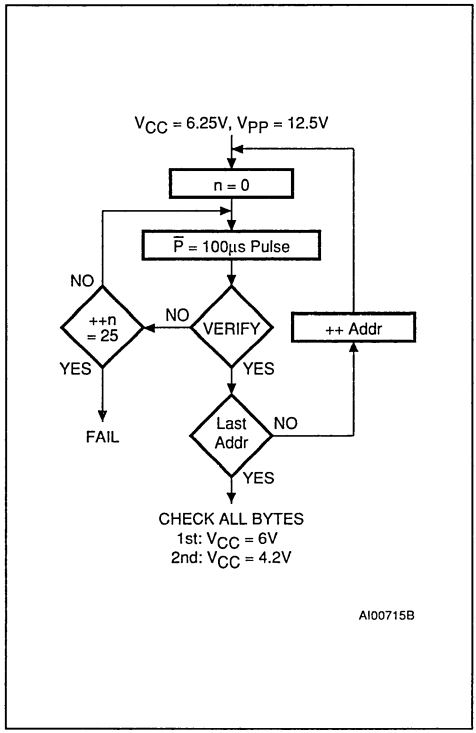
The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27V201 has been designed to be fully compatible with the M27C2001. As a result the M27V201 can be programmed as the M27C2001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V201 has the same electronic signature and uses the same PRESTO II algorithm .

When delivered (and after each erasure for UV EPROM), all bits of the M27V201 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27V201 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in a typical time of 26.5 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V201s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V201 may be common. A TTL low level pulse applied to a M27V201's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27V201. A high level $\overline{E}$ input inhibits the other M27V201s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

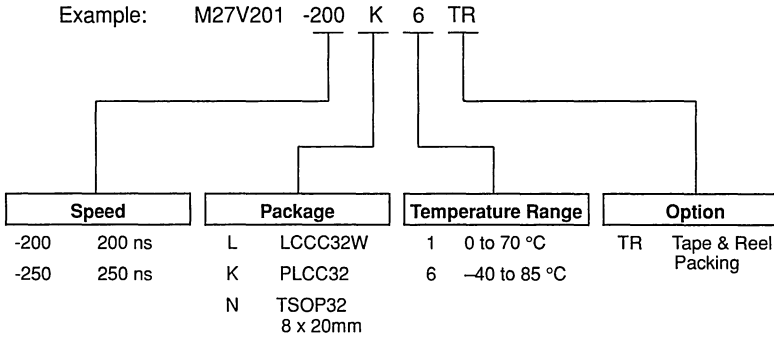
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V201. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V201, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27V201, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7. Note that the M27V201 and M27C2001 have the same identifier bytes .

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V201 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V201 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V201 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V201 window to prevent unintentional erasure. The recommended erasure procedure for the M27V201 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27V201 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME



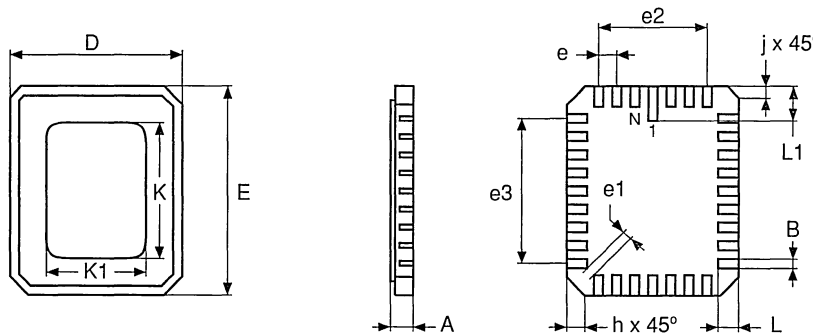
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

LCCC32W - 32 lead Leadless Ceramic Chip Carrier, square window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.28			0.090
B		0.51	0.71		0.020	0.028
D		11.23	11.63		0.442	0.458
E		13.72	14.22		0.540	0.560
e	1.27	–	–	0.050	–	–
e1		0.39	–		0.015	–
e2	7.62	–	–	0.300	–	–
e3	10.16	–	–	0.400	–	–
h	1.02	–	–	0.040	–	–
j	0.51	–	–	0.020	–	–
L		1.14	1.40		0.045	0.055
L1		1.96	2.36		0.077	0.093
K		10.50	10.80		0.413	0.425
K1		8.03	8.23		0.316	0.324
N	32			32		

LCCC32W



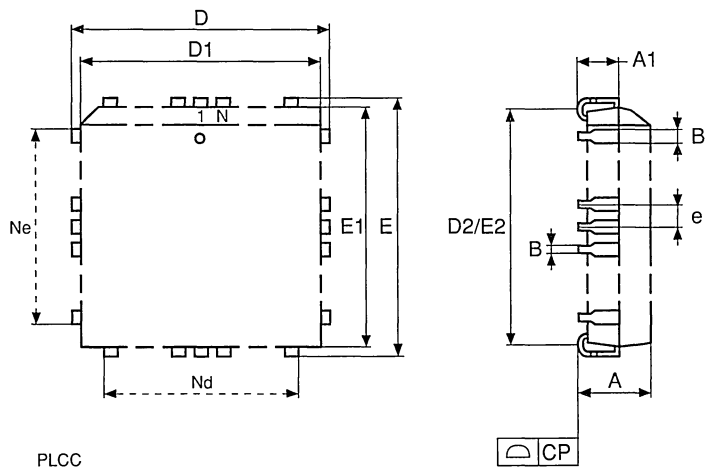
LCCCW-a

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

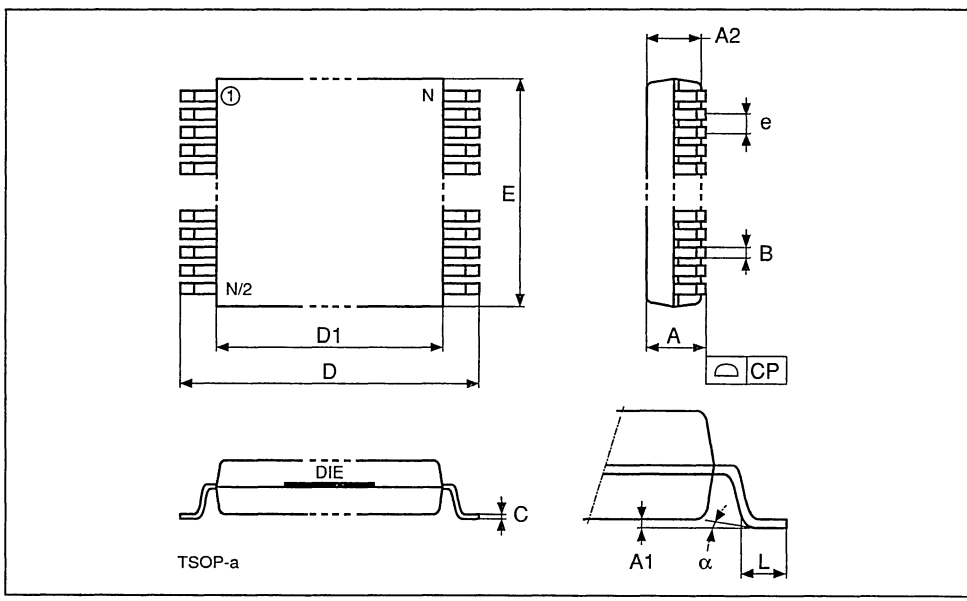


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32

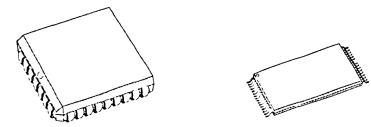


TSOP-a

Drawing is out of scale

VERY LOW VOLTAGE 2 Megabit (256K x 8) OTP ROM

- VERY LOW VOLTAGE READ OPERATION: 2.7V to 5.5V
- ACCESS TIME
  - 150ns (T_A = 0 to 70°C)
  - 200ns (T_A = –20 to 70°C)
- LOW POWER CONSUMPTION
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES for SURFACE MOUNTING: PLCC32 and TSOP32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)
- M27W201 is PROGRAMMABLE as M27C2001 with IDENTICAL SIGNATURE



PLCC32 (K)

TSOP32 (N)
8 x 20mm

DESCRIPTION

The M27W201 is a very low voltage, low power 2 Megabit One Time Programmable ROM, ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 262,144 by 8 bits.

The M27W201 operates in the read mode with a supply voltage as low as 2.7V at –20 to 70°C temperature range. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges. The M27W201 can also be operated as a standard 2 Megabit EPROM (similar to M27C2001) with a 5V power supply .

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

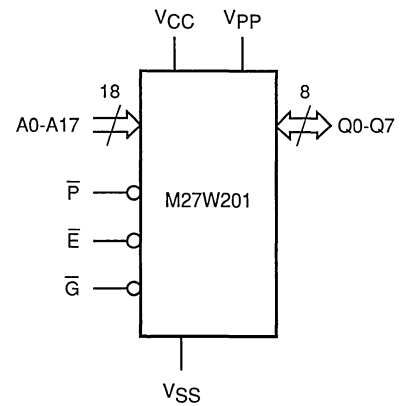


Figure 2A. LCC Pin Connections

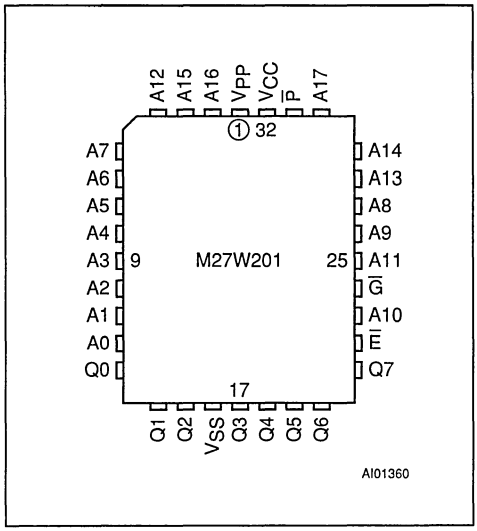


Figure 2B. TSOP Pin Connections

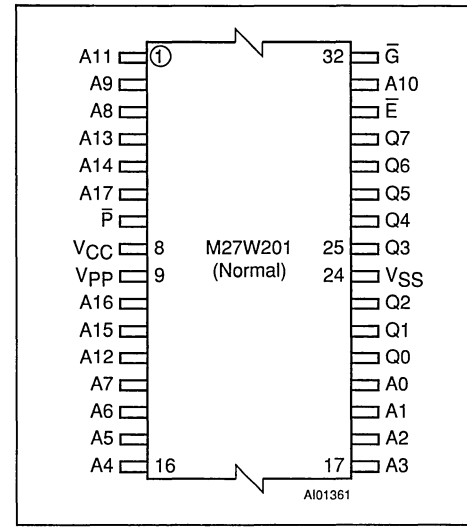


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–20 to 70	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

For applications where the content is programmed only one time and erasure is not required, the M27W201 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

DEVICE OPERATION

The modes of operation of the M27W201 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27W201 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27W201 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation V_{CC} = 2.7V (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27W201 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because OTP ROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS OTP ROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	X	X	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	1	0	0	0	0	1	61h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

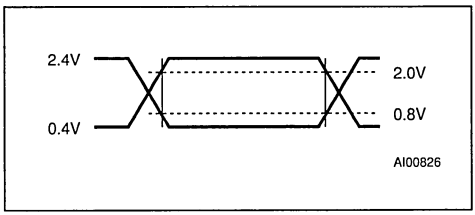


Figure 4. AC Testing Load Circuit

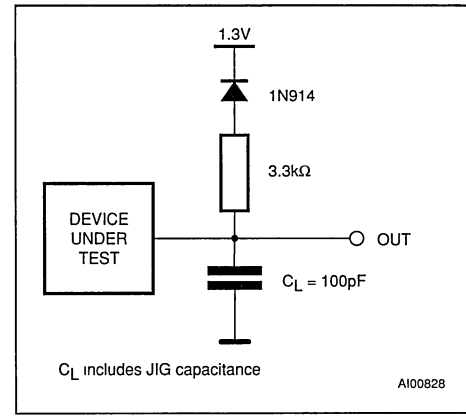


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = –20 to 70 °C; V_{CC} = 2.7V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 2.7V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 2.7V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7. Read Mode AC Characteristics (1)
(T_A = –20 to 70 °C; V_{CC} = 2.7V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27W201				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		75		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	70	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	70	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

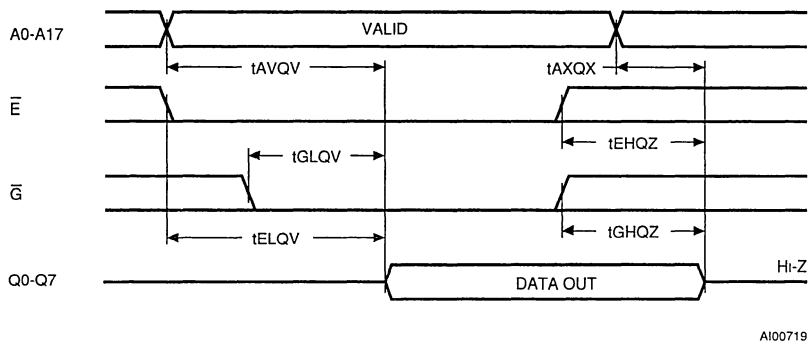


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

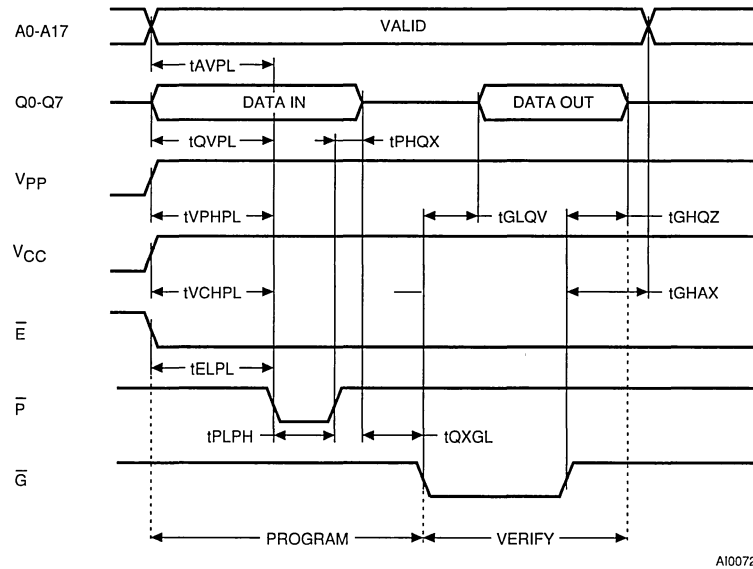
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested

Figure 6. Programming and Verify Modes AC Waveforms



DEVICE OPERATION (cont'd)

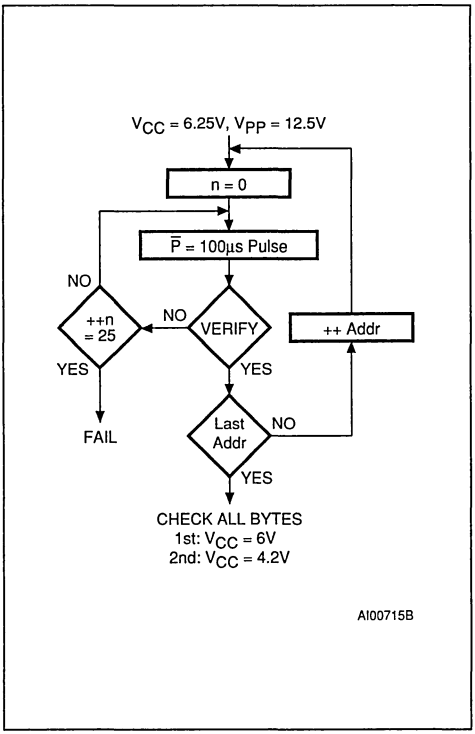
The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27W201 has been designed to be fully compatible with the M27C2001. As a result the M27W201 can be programmed as the M27C2001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27W201 has the same electronic signature and uses the same PRESTO II algorithm .

When delivered, all bits of the M27W201 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The M27W201 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in a typical time of 26.5 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27W201s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27W201 may be common. A TTL low level pulse applied to a M27W201's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27W201. A high level $\overline{E}$ input inhibits the other M27W201s from being programmed.

Program Verify

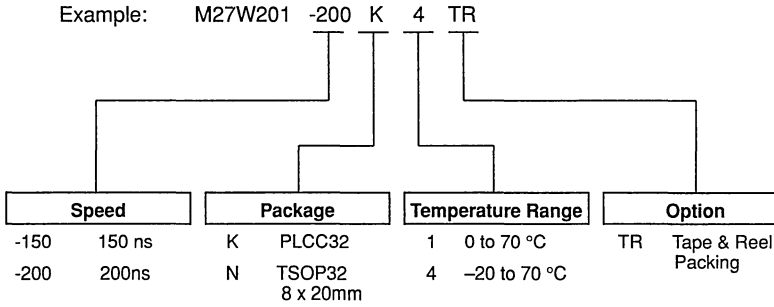
A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at V_{IL}, $\overline{P}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27W201. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27W201, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27W201, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7. Note that the M27W201, M27V201 and M27C2001 have the same identifier bytes.

ORDERING INFORMATION SCHEME



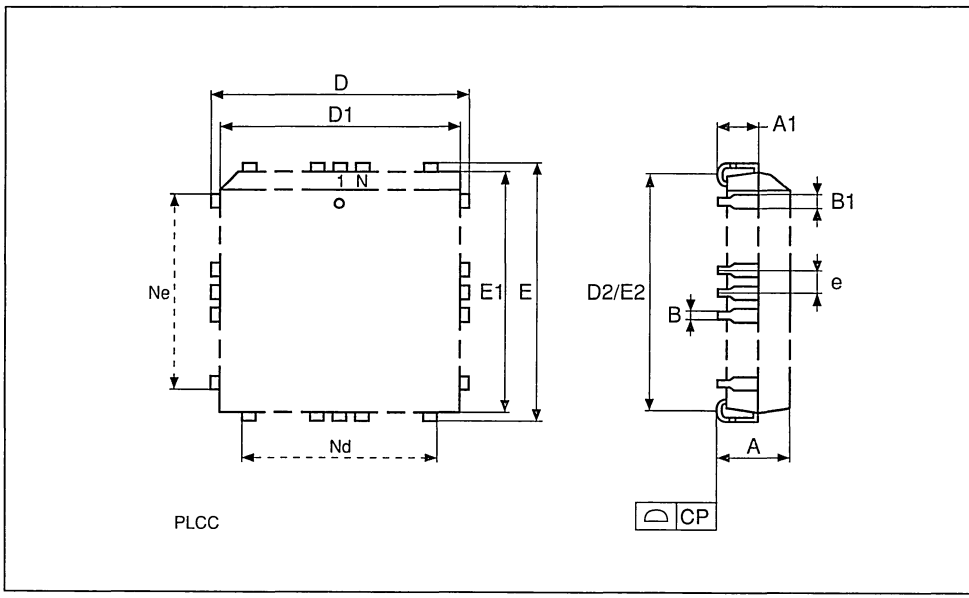
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32



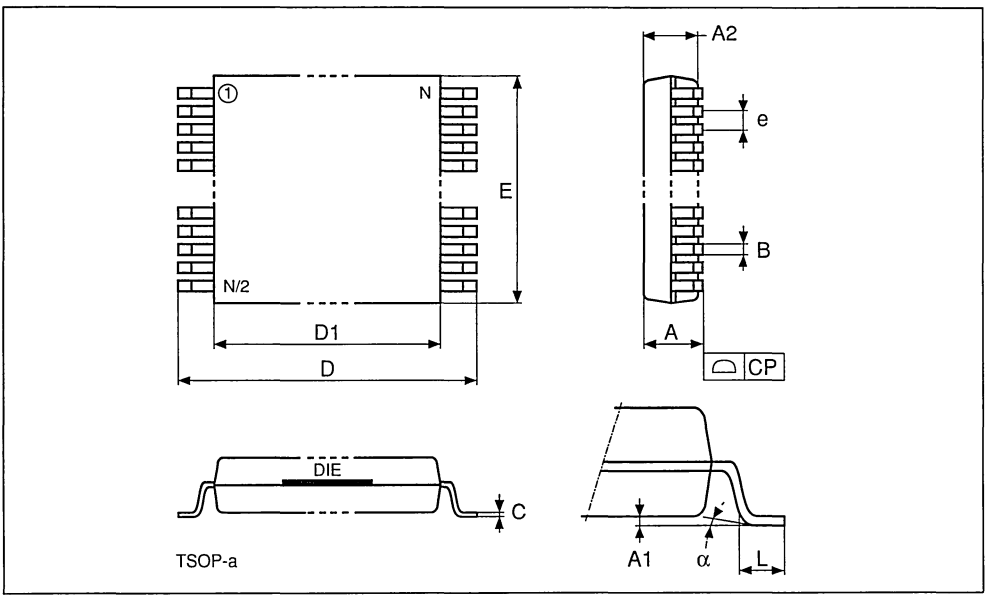
PLCC

Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

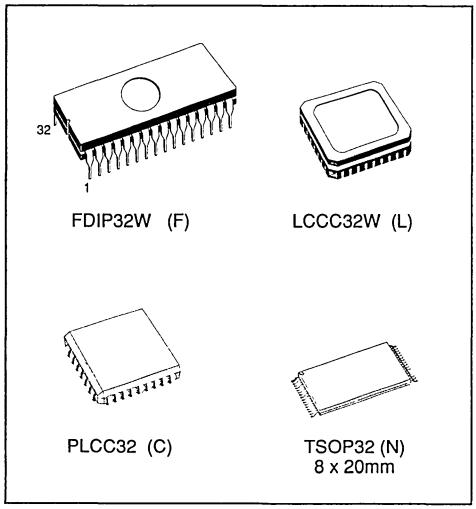
TSOP32



Drawing is out of scale

4 Megabit (512K x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA at 5MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 48sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C4001 is a high speed 4 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 524,288 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C4001 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

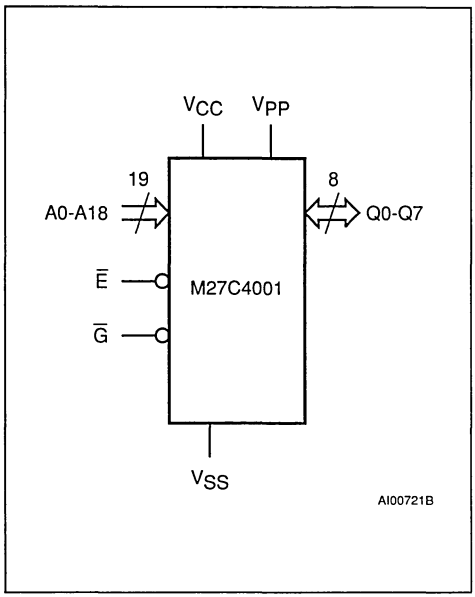


Figure 2A. DIP Pin Connections

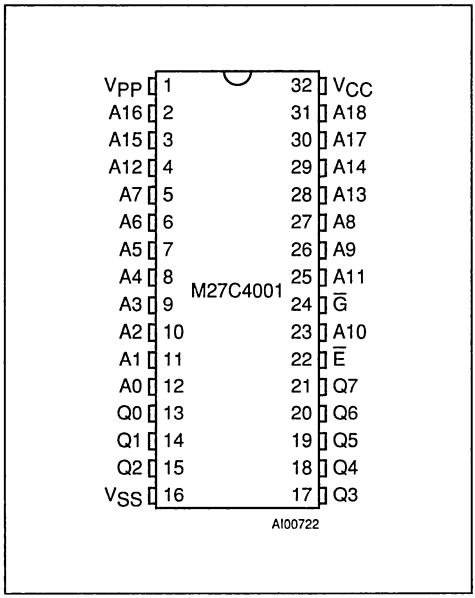


Figure 2B. LCC Pin Connections

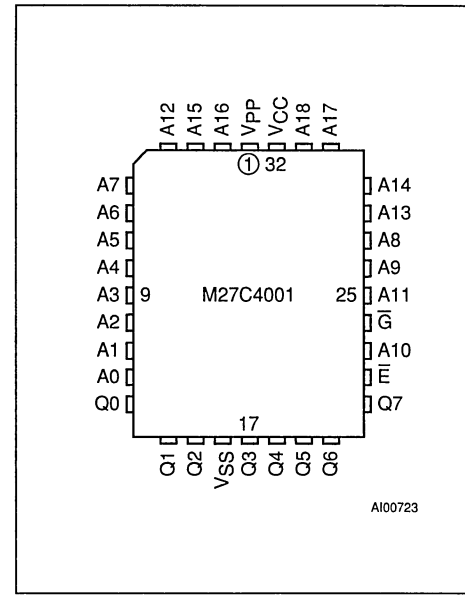
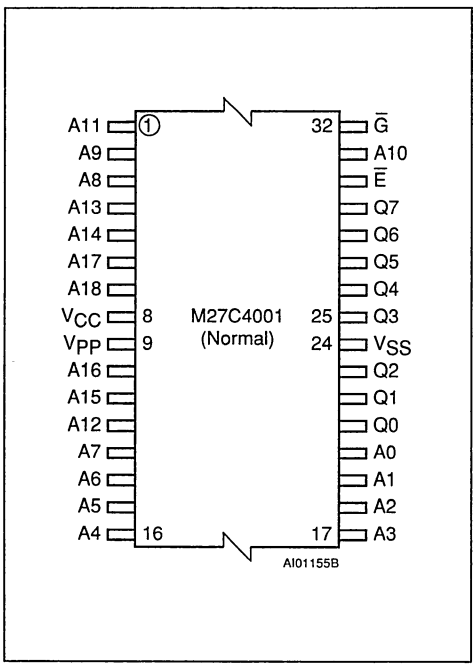


Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operations of the M27C4001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C4001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C4001 has a standby mode which reduces the active current from 30mA to 100µA. The M27C4001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	0	1	41h

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,
b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

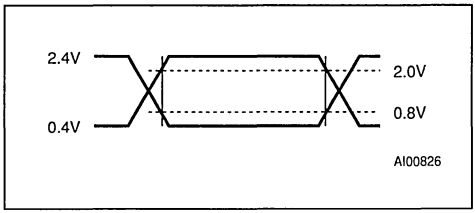


Figure 4. AC Testing Load Circuit

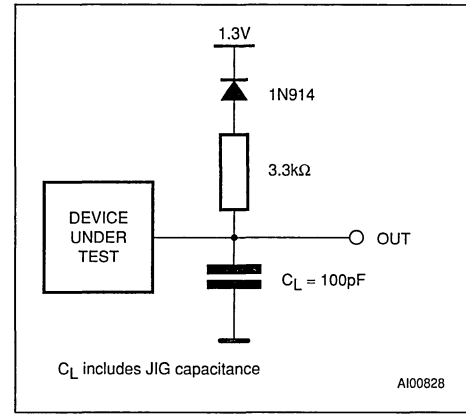


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

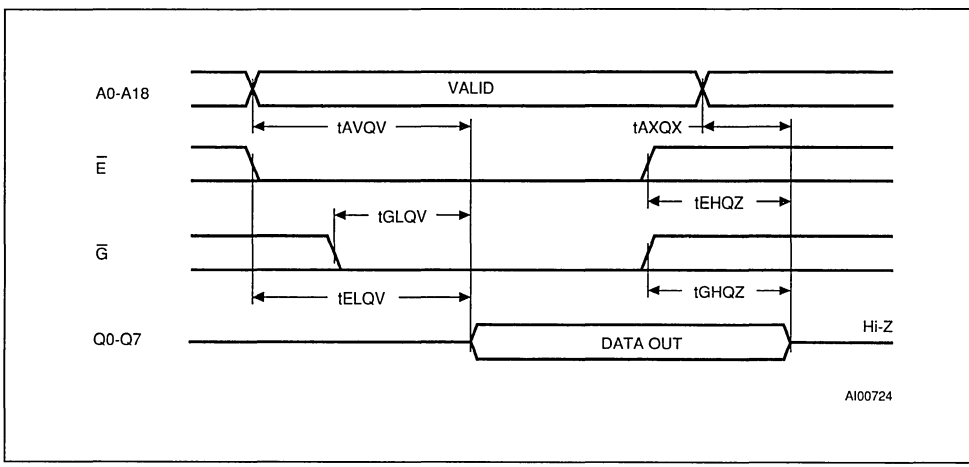


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Maximum DC voltage on Output is V_{CC} +0 5V

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4001						Unit
				-70		-80		-90		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		70		80		90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		35		40		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4001						Unit
				-10		-12		-15		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		50		60		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes: 1 V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2 Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

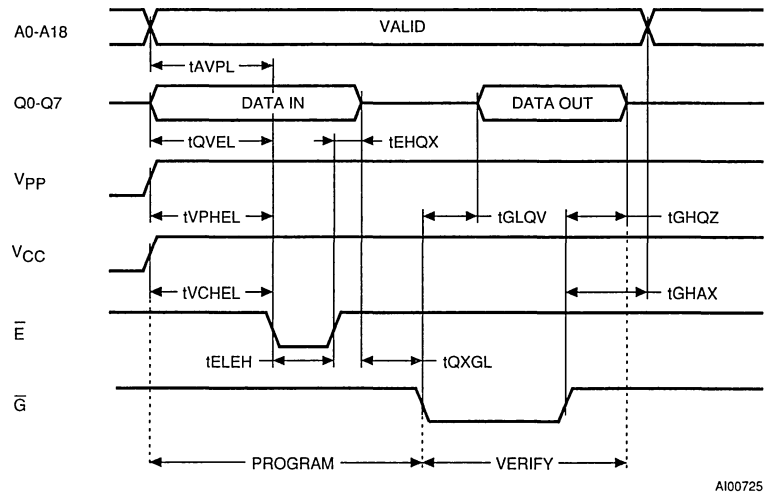
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



System Considerations

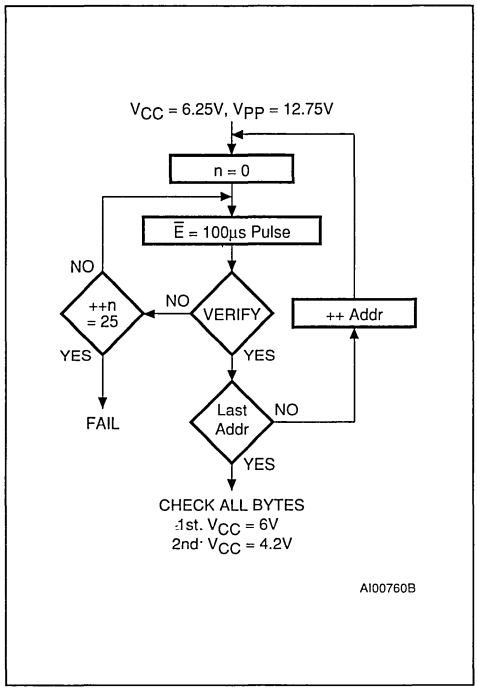
The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C4001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C4001 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 52.5 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C4001s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C4001 may be common. A TTL low level pulse applied to a M27C4001's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C4001. A high level $\overline{E}$ input inhibits the other M27C4001s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C4001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C4001 with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C4001, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C4001 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C4001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C4001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C4001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C4001 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C4001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C4001 -80 X F 1 X

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-70	70 ns	X	± 5%	F	FDIP32W	1	0 to 70 °C	X	Additional Burn-in
-80	80 ns	blank	± 10%	L	LCCC32W	6	–40 to 85 °C	TR	Tape & Reel Packing
-90	90 ns			C	PLCC32				
-10	100 ns			N	TSOP32 8 x 20mm				
-12	120 ns								
-15	150 ns								

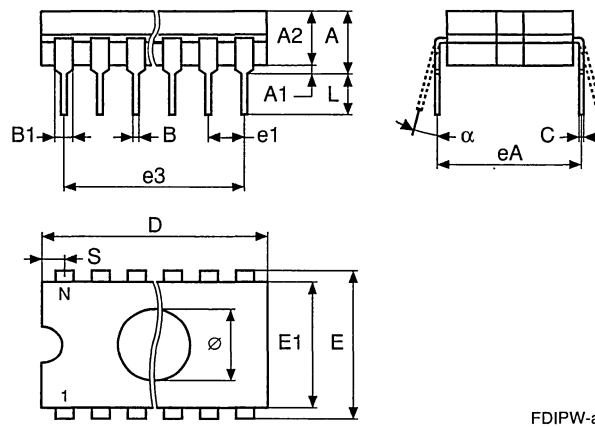
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP32W - 32 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			42.78			1.684
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	38.10	–	–	1.500	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	9.65	–	–	0.380	–	–
α		4°	15°		4°	15°
N		32			32	

FDIP32W



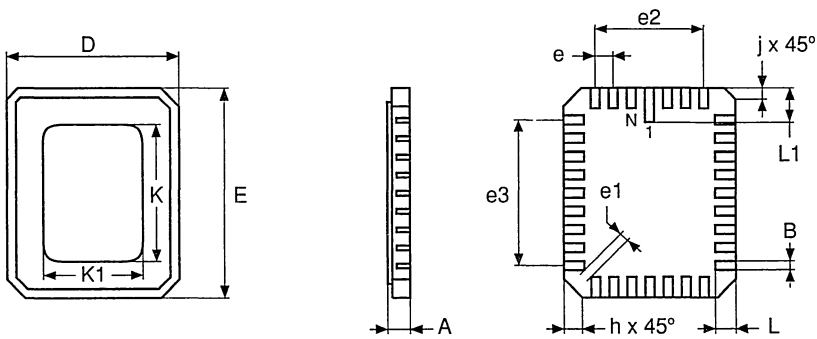
FDIPW-a

Drawing is out of scale

LCCC32W - 32 lead Leadless Ceramic Chip Carrier, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.28			0.090
B		0.51	0.71		0.020	0.028
D		11.23	11.63		0.442	0.458
E		13.72	14.22		0.540	0.560
e	1.27	–	–	0.050	–	–
e1		0.39	–		0.015	–
e2	7.62	–	–	0.300	–	–
e3	10:16	–	–	0.400	–	–
h	1.02	–	–	0.040	–	–
j	0.51	–	–	0.020	–	–
L		1.14	1.40		0.045	0.055
L1		1.96	2.36		0.077	0.093
K		10.50	10.80		0.413	0.425
K1		8.03	8.23		0.316	0.324
N	32			32		

LCCC32W



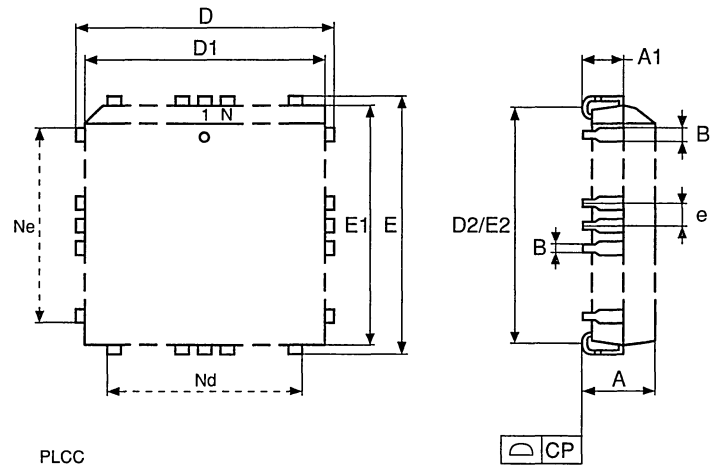
LCCCW-a

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

PLCC32



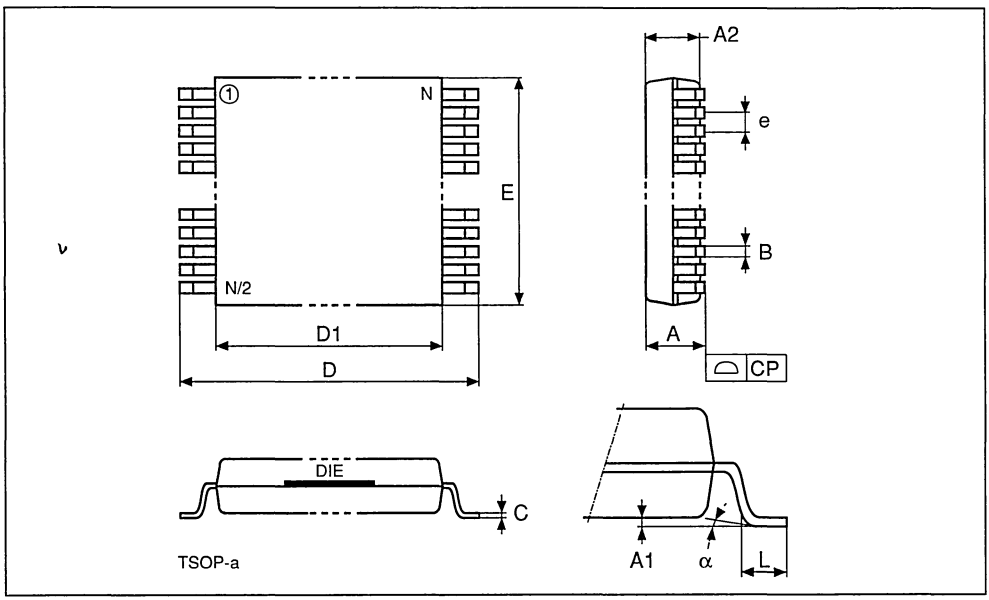
PLCC

Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5É		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32



TSOP-a

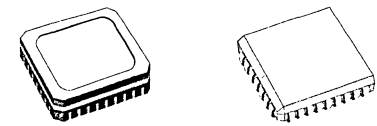
Drawing is out of scale

SGS-THOMSON MICROELECTRONICS

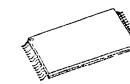
M27V401

LOW VOLTAGE 4 Megabit (512K x 8) UV EPROM and OTP ROM

- LOW VOLTAGE READ OPERATION: 3V to 5.5V
- ACCESS TIME: 200 and 250ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES for SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32 and TSOP32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 48sec. (PRESTO II ALGORITHM)
- M27V401 is PROGRAMMABLE as M27C4001 with IDENTICAL SIGNATURE



LCCC32W (L) PLCC32 (K)



TSOP32 (N)
8 x 20mm

DESCRIPTION

The M27V401 is a low voltage, low power 4 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 524,288 by 8 bits.

The M27V401 operates in the read mode with a supply voltage as low as 3V. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

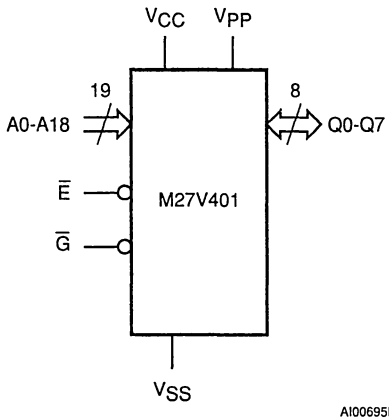


Figure 2A. LCC Pin Connections

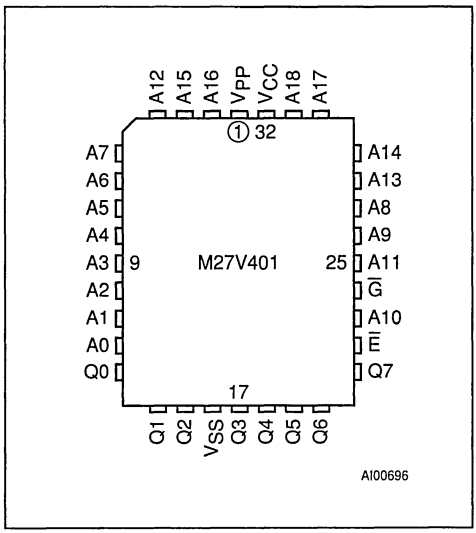


Figure 2B. TSOP Pin Connections

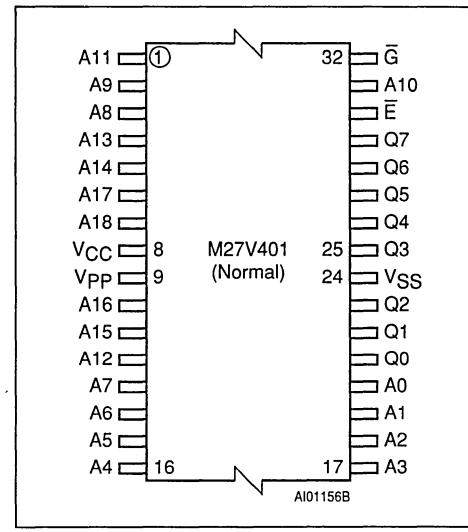


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

The M27V401 can also be operated as a standard 4 Megabit EPROM (similar to M27C4001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27V401 is offered in both Plastic Leaded Chip Carrier and Plastic thin Small Outline packages.

DEVICE OPERATION

The modes of operation of the M27V401 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27V401 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V401 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 3.2V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V401 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	0	1	41h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

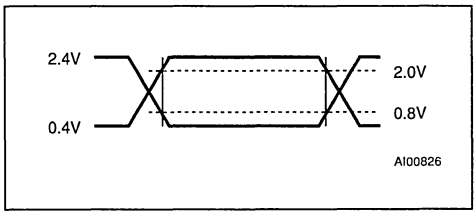


Figure 4. AC Testing Load Circuit

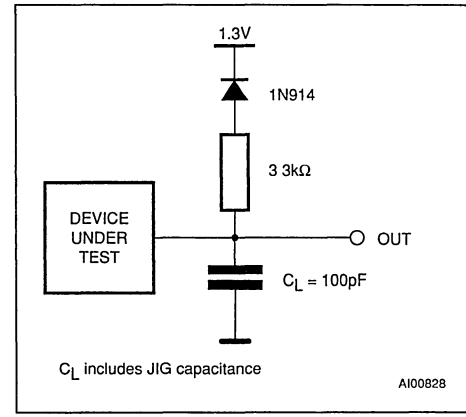


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 3.2V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.2V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V

Table 7. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 3V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27V401				Unit
				-200		-250		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		130		150	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	80	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	80	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested..

Figure 5. Read Mode AC Waveforms

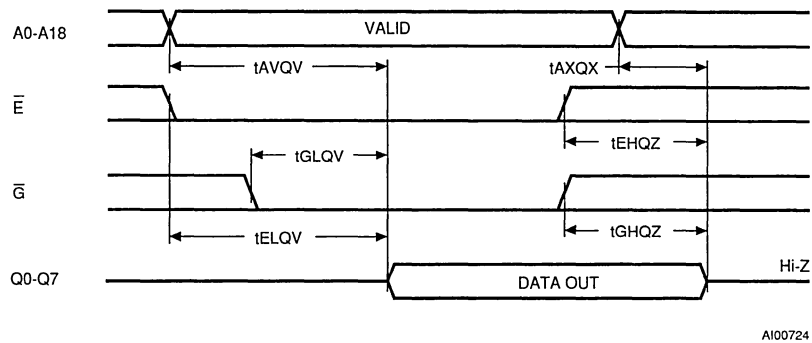


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

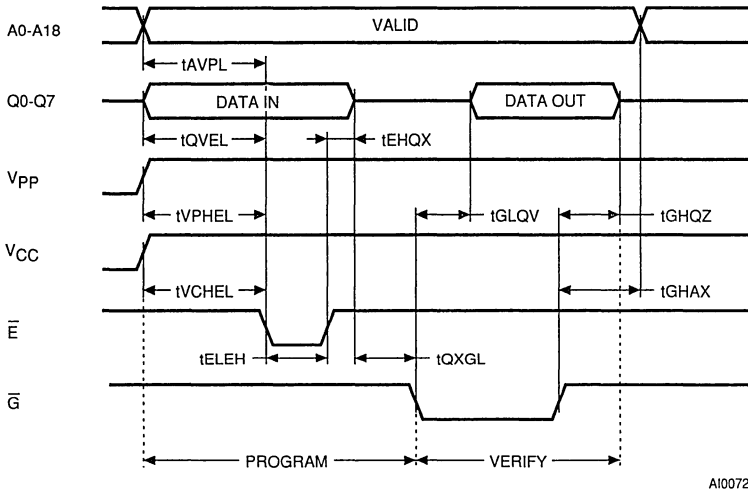
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested..

Figure 6. Programming and Verify Modes AC Waveforms



DEVICE OPERATION (cont'd)

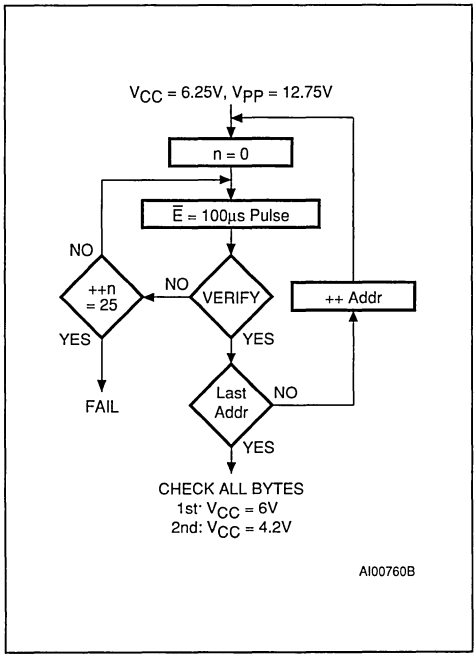
The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27V401 has been designed to be fully compatible with the M27C4001. As a result the M27V401 can be programmed as the M27C4001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27V401 has the same electronic signature and uses the same PRESTO II algorithm .

When delivered (and after each erasure for UV EPROM), all bits of the M27V401 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27V401 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in a typical time of 52.5 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V401s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V401 may be common. A TTL low level pulse applied to a M27V401's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27V401. A high level $\overline{E}$ input inhibits the other M27V401s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH},, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

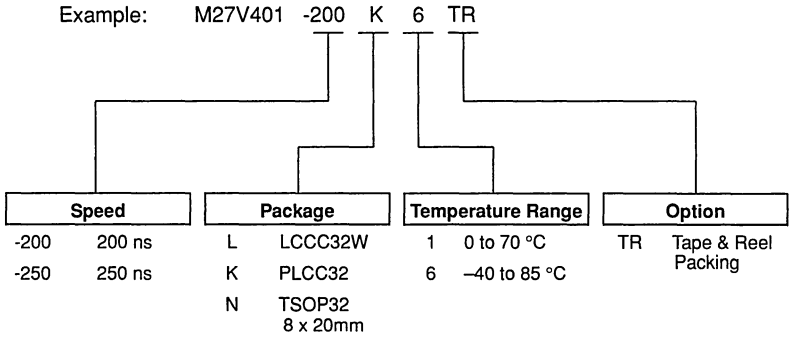
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V401. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V401, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27V401, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7. Note that the M27V401 and M27C4001 have the same identifier bytes .

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27V401 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V401 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27V401 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V401 window to prevent unintentional erasure. The recommended erasure procedure for the M27V401 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27V401 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME



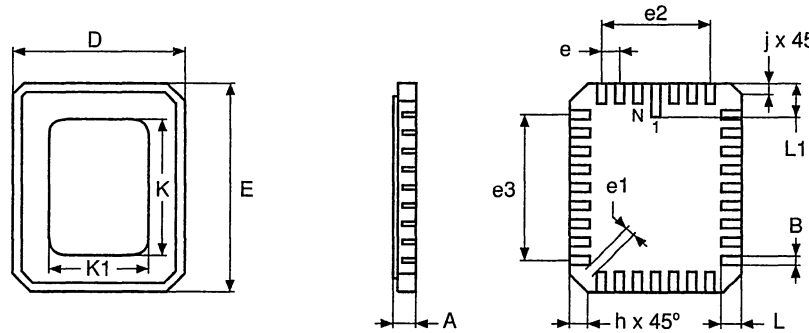
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

LCCC32W - 32 lead Leadless Ceramic Chip Carrier, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.28			0.090
B		0.51	0.71		0.020	0.028
D		11.23	11.63		0.442	0.458
E		13.72	14.22		0.540	0.560
e	1.27	–	–	0.050	–	–
e1		0.39	–		0.015	–
e2	7.62	–	–	0.300	–	–
e3	10.16	–	–	0.400	–	–
h	1.02	–	–	0.040	–	–
j	0.51	–	–	0.020	–	–
L		1.14	1.40		0.045	0.055
L1		1.96	2.36		0.077	0.093
K		10.50	10.80		0.413	0.425
K1		8.03	8.23		0.316	0.324
N	32			32		

LCCC32W



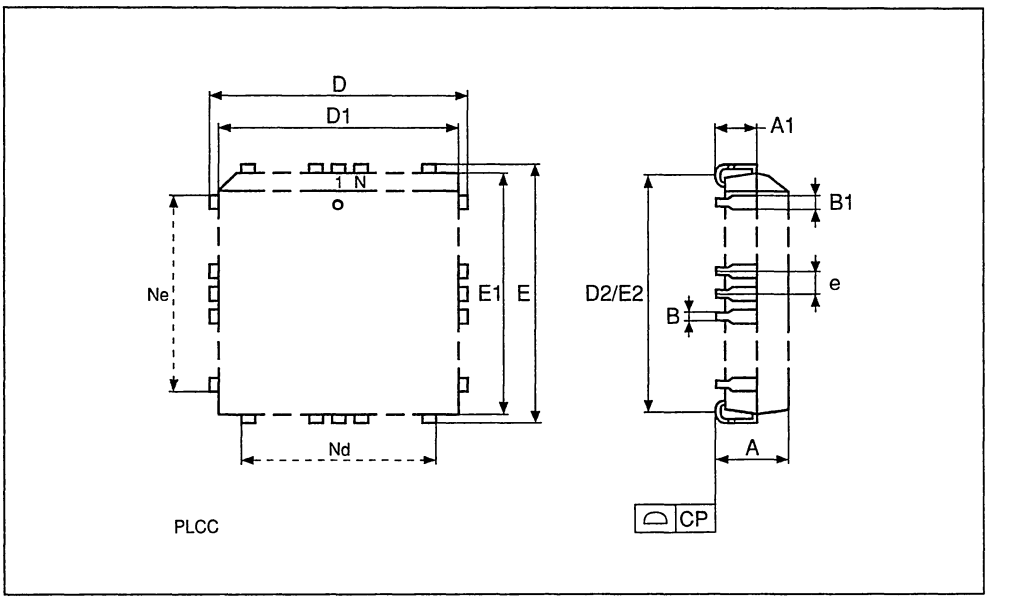
LCCCW-a

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

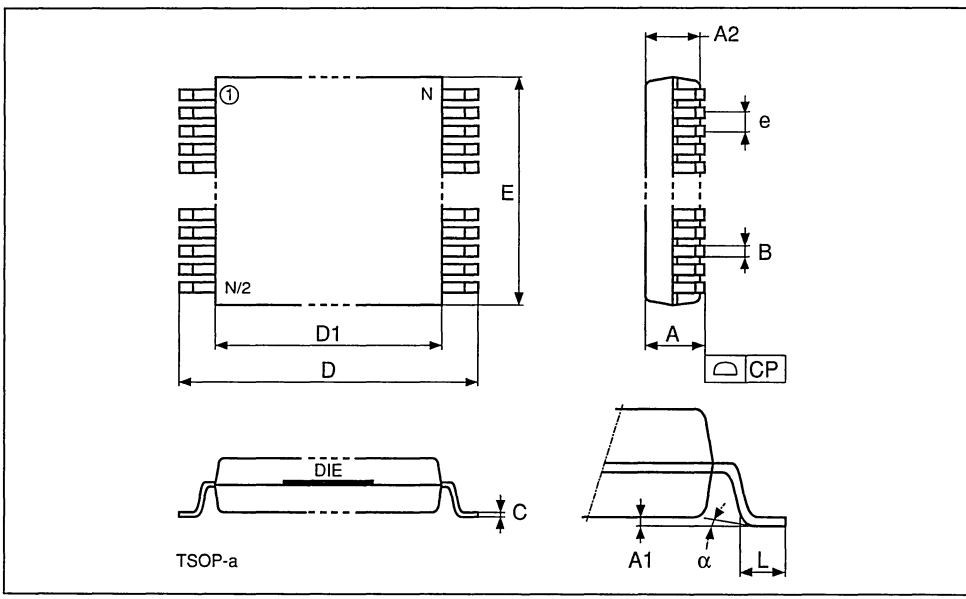


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32

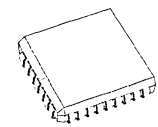


TSOP-a

Drawing is out of scale

VERY LOW VOLTAGE 4 Megabit (512K x 8) OTP ROM

- VERY LOW VOLTAGE READ OPERATION: 2.7V to 5.5V
- ACCESS TIME:
  - 150ns (T_A = 0 to 70 °C)
  - 200ns (T_A = –20 to 70 °C)
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 48sec. (PRESTO II ALGORITHM)
- M27W401 is PROGRAMMABLE as M27C4001 with IDENTICAL SIGNATURE



PLCC32 (K)

TSOP32 (N)
8 x 20mm

DESCRIPTION

The M27W401 is a very low voltage, low power 4 Megabit One Time Programmable ROM, ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 524,288 by 8 bits.

The M27W401 operates in the read mode with a supply voltage as low as 2.7V at –20 to 70 °C temperature range. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges. The M27W401 can also be operated as a standard 4 Megabit EPROM (similar to M27C4001) with a 5V power supply.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

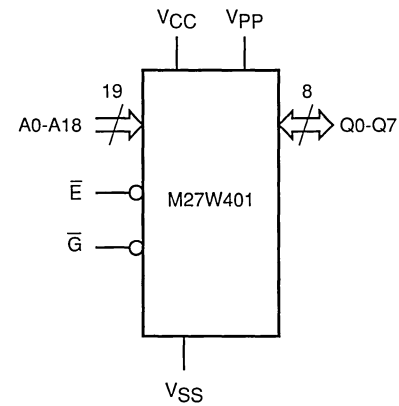


Figure 2A. LCC Pin Connections

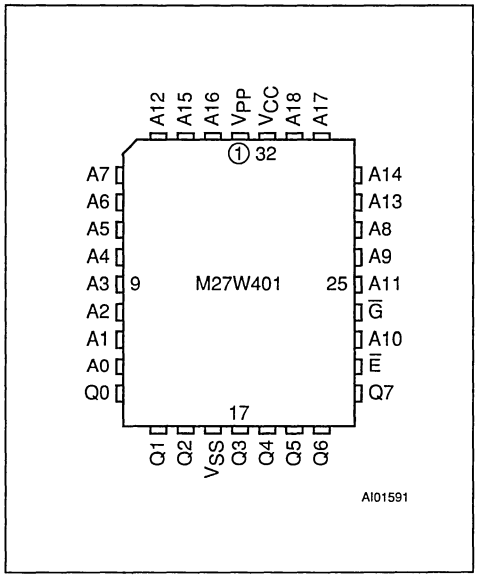


Figure 2B. TSOP Pin Connections

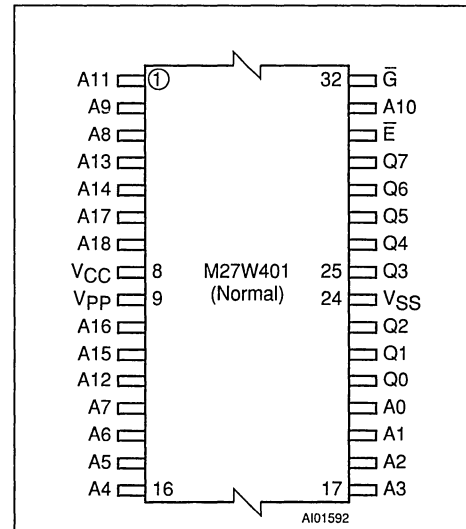


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–20 to 70	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0 5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

For applications where the content is programmed only one time and erasure is not required, the M27W401 is offered in both Plastic Leaded Chip Carrier and Plastic thin Small Outline packages.

DEVICE OPERATION

The modes of operation of the M27W401 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27W401 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27W401 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 2.7V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27W401 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because OTP ROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS OTP ROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	0	1	41h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4 to 2.4V
Input and Output Timing Ref. Voltages	0.8 to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

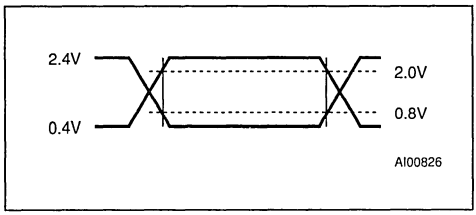


Figure 4. AC Testing Load Circuit

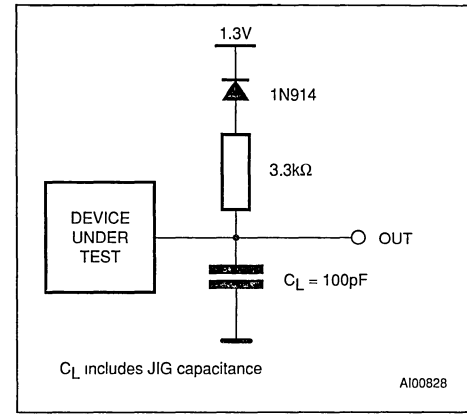


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 6. Read Mode DC Characteristics (1)
(T_A = –20 to 70 °C; V_{CC} = 2.7V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 2.7V		15	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} = 5.5V		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 2.7V		20	µA
		$\overline{E}$ > V_{CC} – 0.2V, V_{CC} = 5.5V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0 5V

Table 7. Read Mode AC Characteristics (1)
(T_A = –20 to 70 °C; V_{CC} = 2.7V to 5.5V unless specified; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27W401				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		75		100	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	70	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	70	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested..

Figure 5. Read Mode AC Waveforms

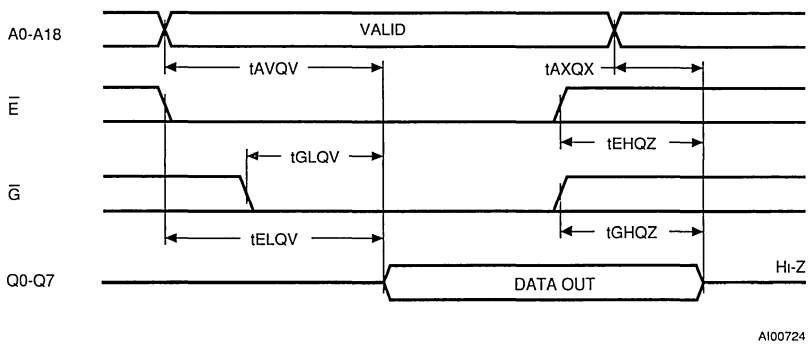


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

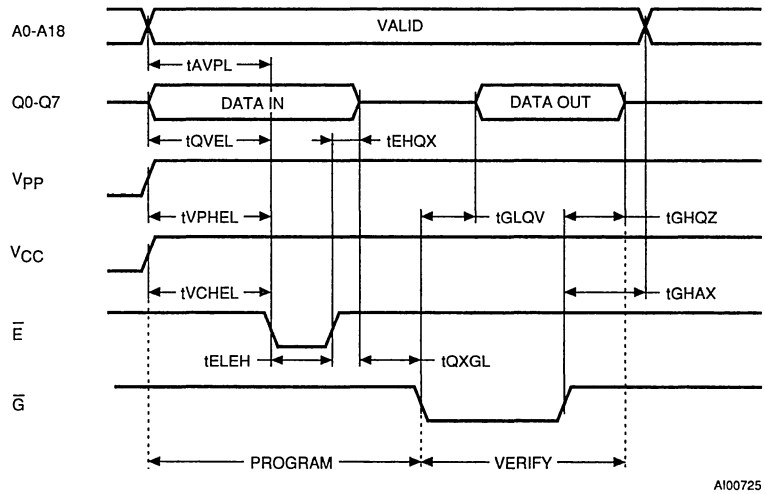
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested..

Figure 6. Programming and Verify Modes AC Waveforms



DEVICE OPERATION (cont'd)

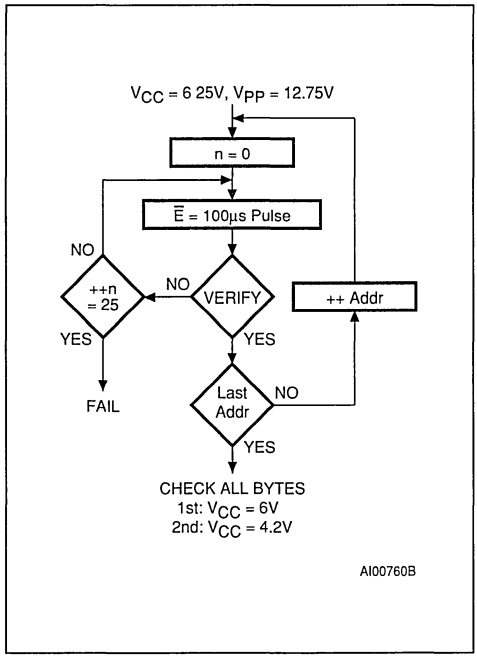
The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

The M27W401 has been designed to be fully compatible with the M27C4001. As a result the M27W401 can be programmed as the M27C4001 on the same programmers applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27W401 has the same electronic signature and uses the same PRESTO II algorithm .

When delivered, all bits of the M27W401 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The M27W401 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{P}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in a typical time of 52.5 seconds. Programming with PRESTO II involves in applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No over-program pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27W401s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27W401 may be common. A TTL low level pulse applied to a M27W401's $\overline{E}$ input, with $\overline{P}$ low and V_{PP} at 12.75V, will program that M27W401. A high level $\overline{E}$ input inhibits the other M27W401s from being programmed.

Program Verify

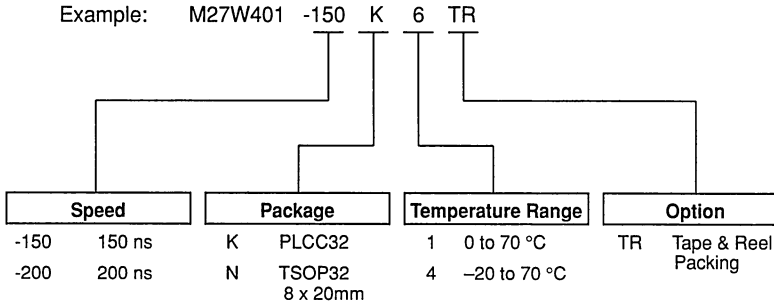
A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH},, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27W401. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27W401, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27W401, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7. Note that the M27W401 and M27C4001 have the same identifier bytes.

ORDERING INFORMATION SCHEME



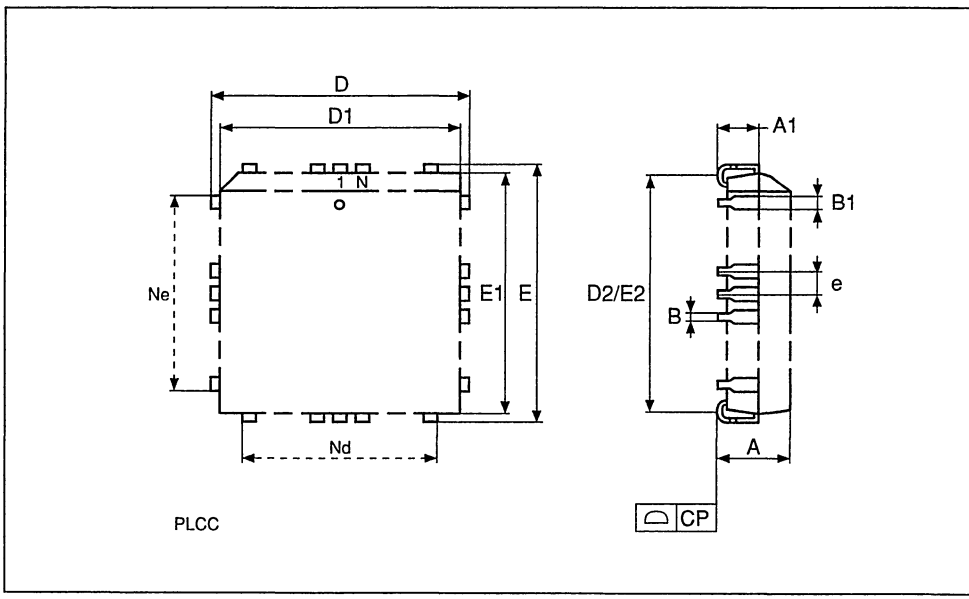
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

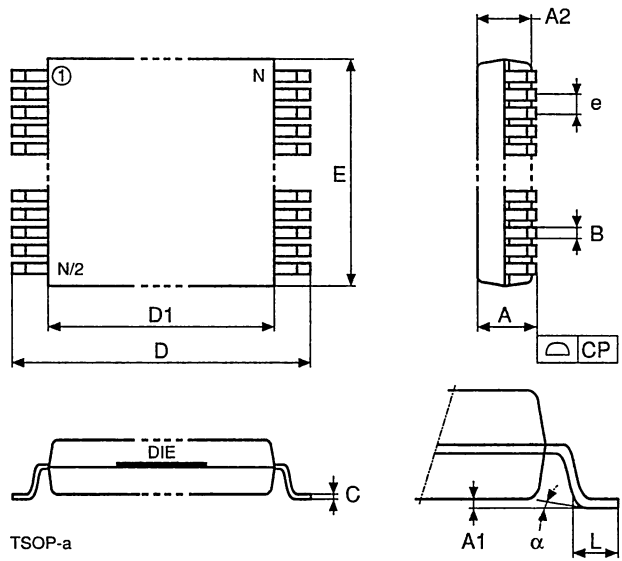


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.004

TSOP32

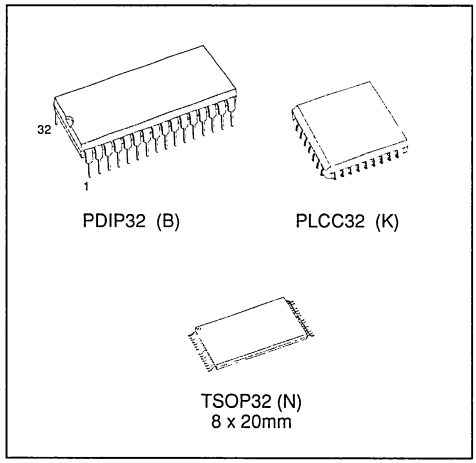


TSOP-a

Drawing is out of scale

4 Megabit (512K x 8) OTP ROM

- PIN COMPATIBLE with the 4 MEGABIT, 5V ONLY FLASH MEMORY (M29F040)
- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA at 5MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 48sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C405 is an high speed 4 Megabit One Time Programmable ROM, organised as 524,288 by 8 bits. It is ideally suited for microprocessor systems requiring large programs, in the application where the contents is stable and needs to be programmed only one time.

The M27C405 is pin compatible with the M29F040, the industry standard 4 Megabit, 5V only FLASH Memory. It can be considered as a FLASH Low Cost solution for production quantities.

The M27C405 is offered in Plastic Dual-in-Line, Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

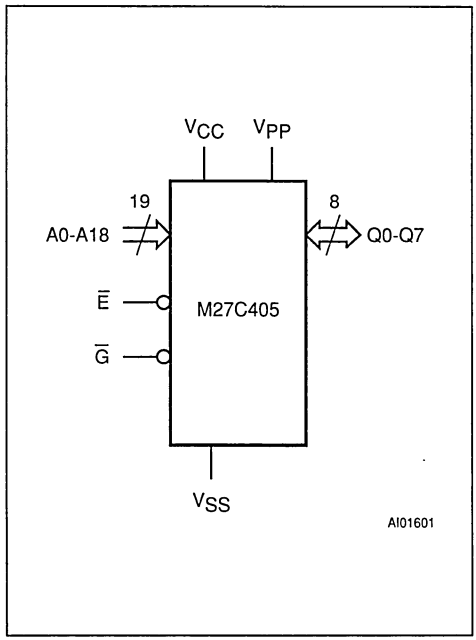


Figure 2A. DIP Pin Connections

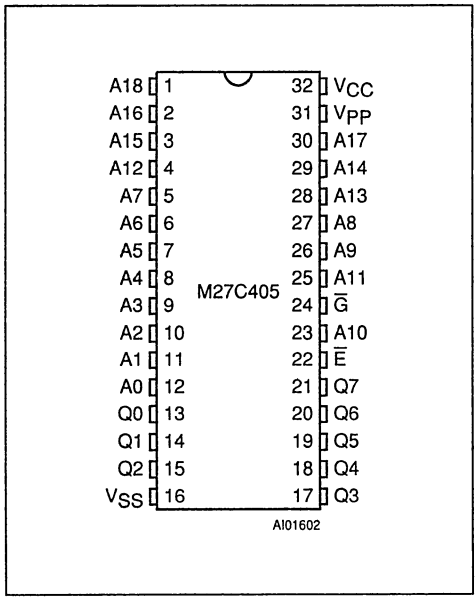


Figure 2B. LCC Pin Connections

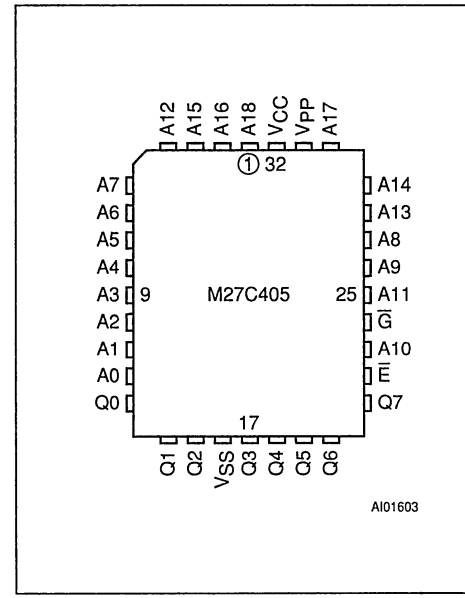
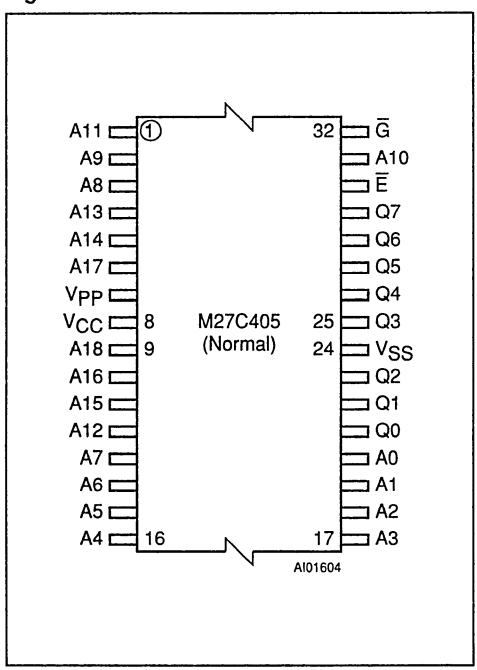


Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operations of the M27C405 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C405 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C405 has a standby mode which reduces the active current from 30mA to 100µA. The M27C405 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q7
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	1	0	0	1	0	B4h

Two Line Output Control

Because OTP ROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,
b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

Table 5. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 20ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

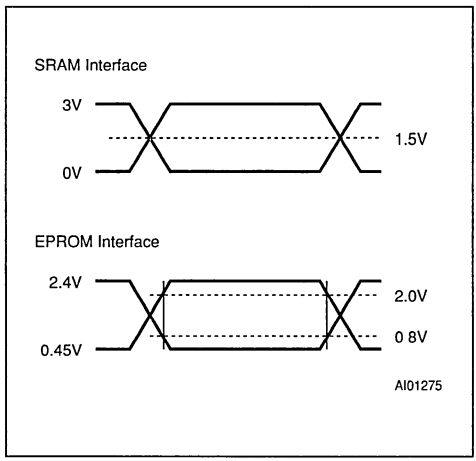


Figure 4. AC Testing Load Circuit

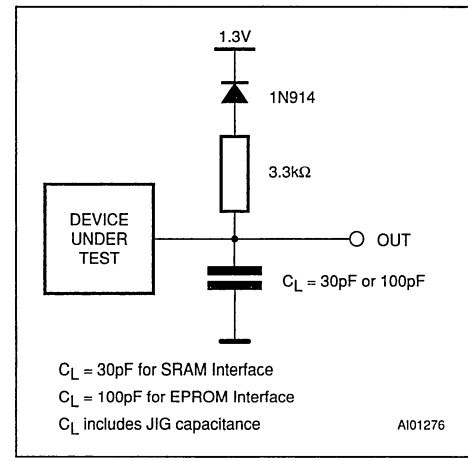


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 8A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C405						Unit
				-70		-80		-90		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
				SRAM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		70		80		90	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		70		80		90	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		35		40		40	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Table 8B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C405						Unit
				-10		-12		-15		
				V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
				EPROM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		60		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

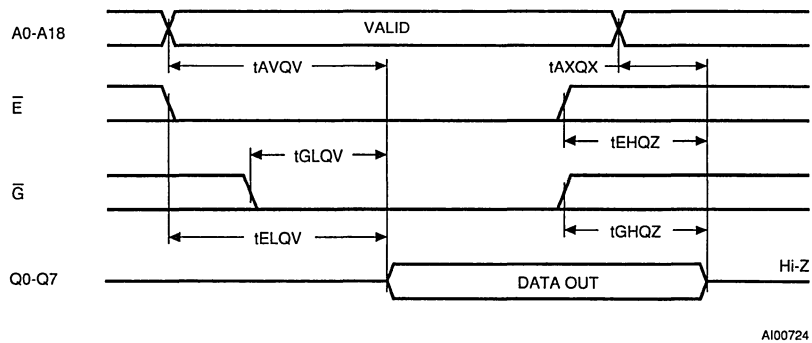


Table 9. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

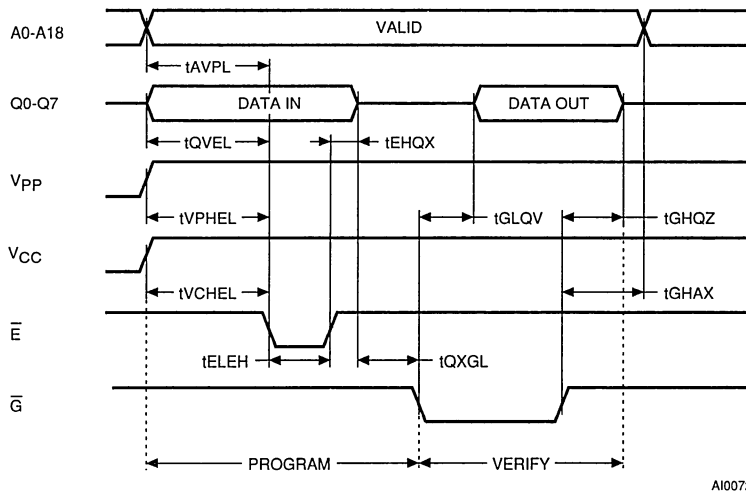
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms



System Considerations

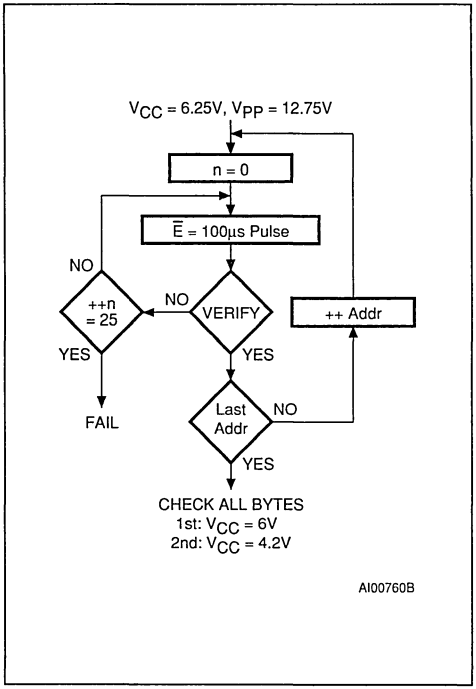
The power switching characteristics of Advanced CMOS OTP ROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered, all bits of the M27C405 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The M27C405 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 52.5 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C405s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C405 may be common. A TTL low level pulse applied to a M27C405's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C405. A high level $\overline{E}$ input inhibits the other M27C405s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an OTP ROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C405. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C405 with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C405, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ORDERING INFORMATION SCHEME

Example: M27C405 -80 K 1 TR

Speed		Package		Temperature Range		Option	
-70	70 ns	B	PDIP32	1	0 to 70 °C	TR	Tape & Reel Packing
-80	80 ns	K	PLCC32	6	–40 to 85 °C		
-90	90 ns	N	TSOP32 8 x 20mm				
-10	100 ns						
-12	120 ns						
-15	150 ns						

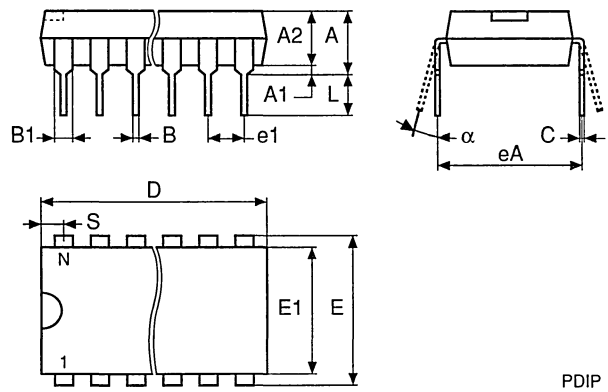
For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP32 - 32 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N	32			32		

PDIP32



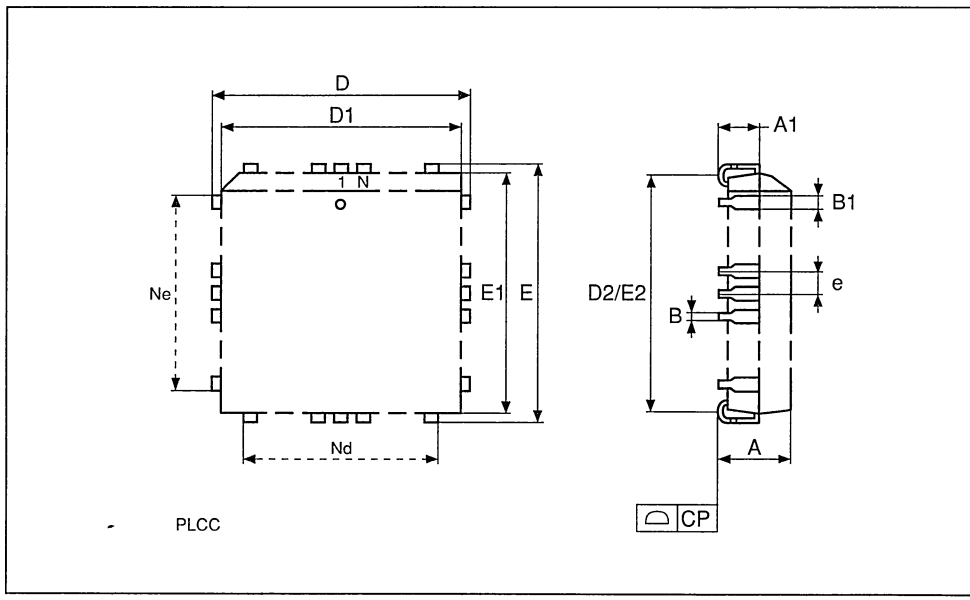
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

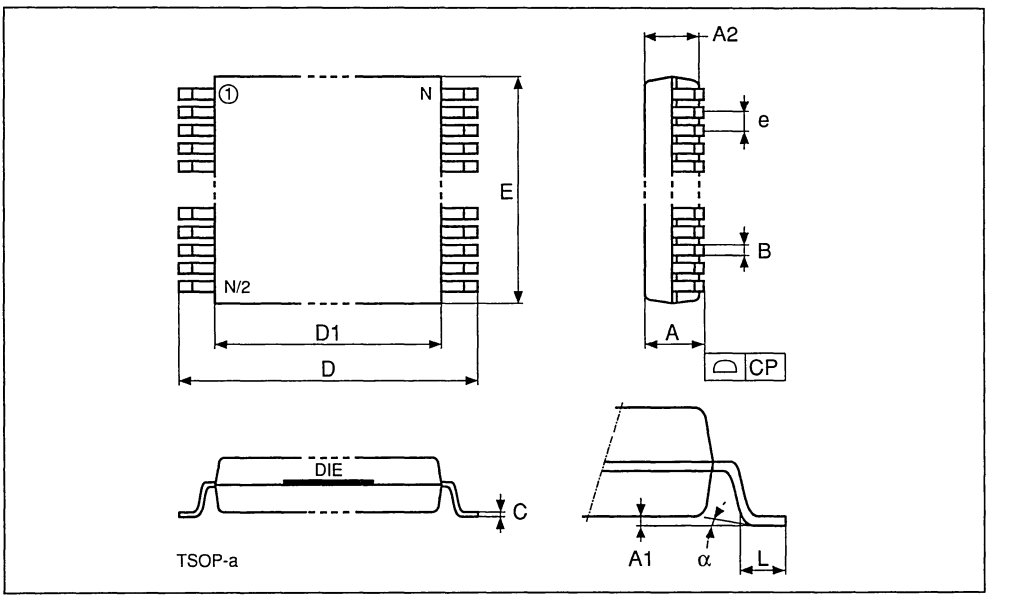


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5É		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32

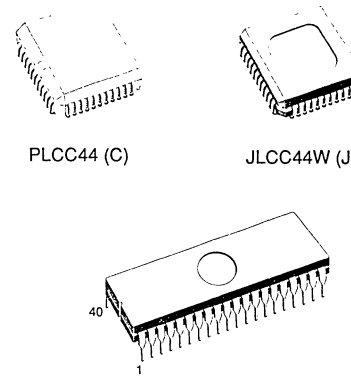


TSOP-a

Drawing is out of scale

4 Megabit (256K x 16) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 50mA at 5MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C4002 is a high speed 4 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 262,144 by 16 bits.

The Window Ceramic Frit-Seal Dual-in-Line and J-Lead Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C4002 is offered in Plastic Leaded Chip Carrier package.

Figure 1. Logic Diagram

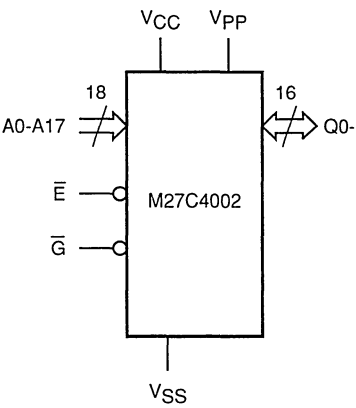


Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

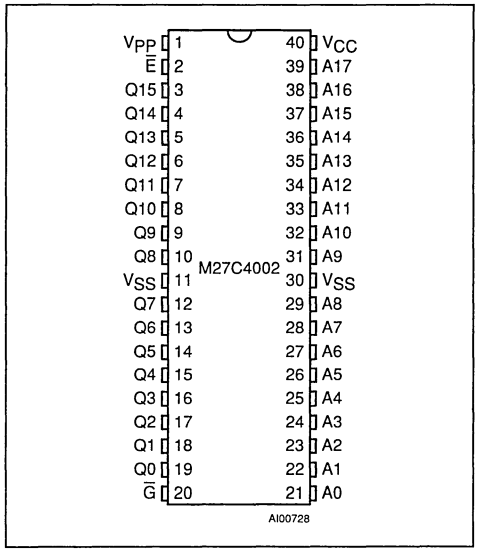
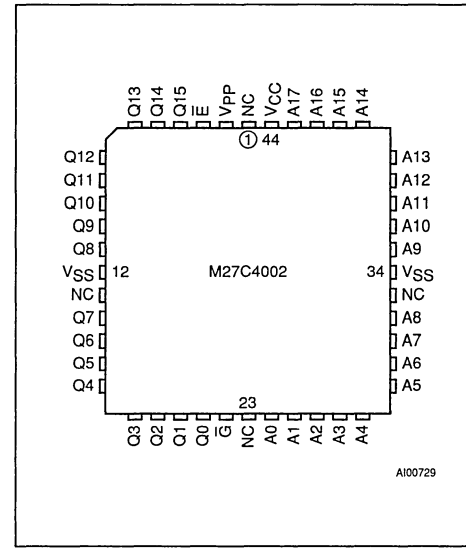


Figure 2B. LCC Pin Connections



Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operations of the M27C4002 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C4002 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C4002 has a standby mode which reduces the active current from 50mA to 100µA. The M27C4002 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the output capacitive and inductive loading of the device.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C4002 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C4002 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ is at TTL-low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q0 - Q15
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note. X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0 5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	1	0	0	44h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

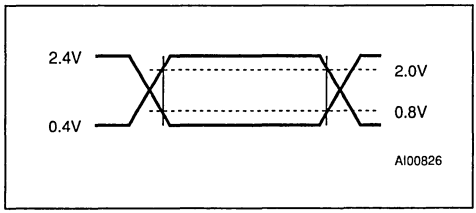


Figure 4. AC Testing Load Circuit

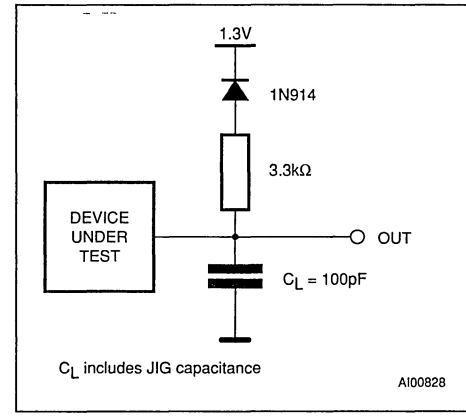


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

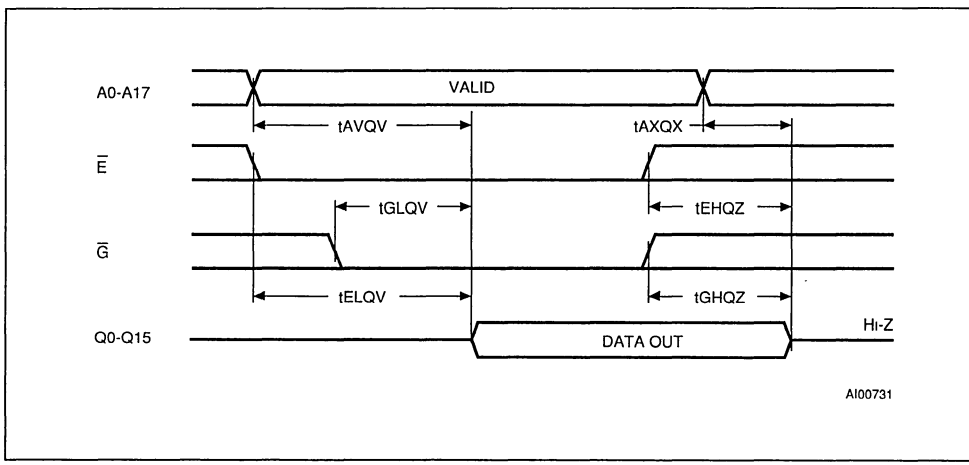


Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 10MHz		70	mA
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4002						Unit
				-80		-90		-10		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		80		90		100	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		80		90		100	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		40		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	30	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C4002						Unit
				-12		-15		-20		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		60		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	50	0	80	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	50	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ}	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

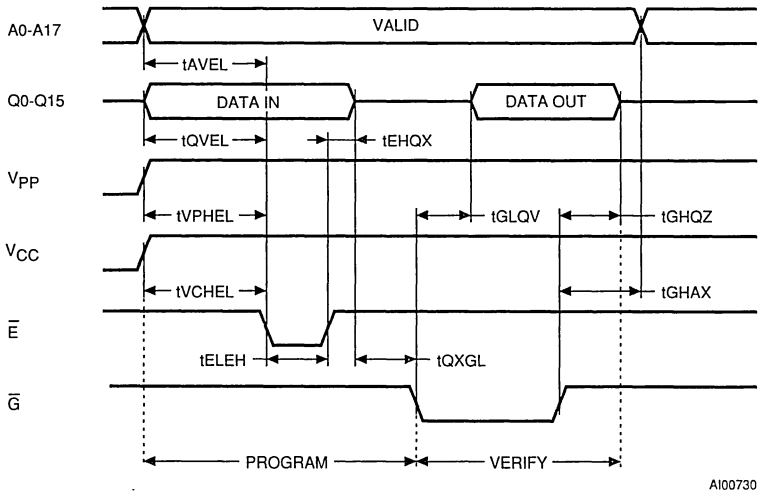
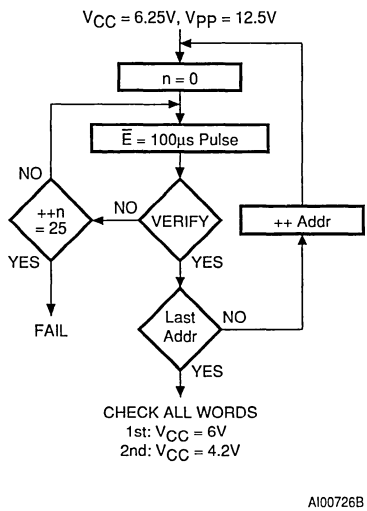


Figure 7. Programming Flowchart



PRESTO II Programming Algorithm

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 26.5 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27C4002s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C4002 may be common. A TTL low level pulse applied to a M27C4002's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C4002. A high level $\overline{E}$ input inhibits the other M27C4002s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C4002. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C4002 with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C4002, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C4002 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C4002 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C4002 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C4002 window to prevent unintentional erasure. The recommended erasure procedure for the M27C4002 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C4002 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C4002 -10 X F 1 X

Speed		V_{CC} Tolerance		Package		Temperature Range		Option	
-80	80 ns	X	± 5%	F	FDIP40W	1	0 to 70 °C	X	Additional Burn-in
-90	90 ns	blank	± 10%	C	PLCC44	6	–40 to 85 °C	TR	Tape & Reel Packing
-10	100 ns			J	JLCC44W				
-12	120 ns								
-15	150 ns								
-20	200 ns								

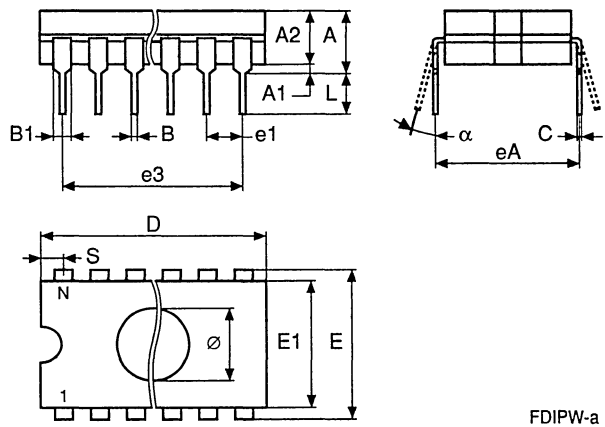
For a list of available options (Speed, V_{CC} Tolerance, Package etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP40W - 40 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			53.40			2.102
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	48.26	–	–	1.900	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
Ø	9.65	–	–	0.380	–	–
α		4°	15°		4°	15°
N		40			40	

FDIP40W



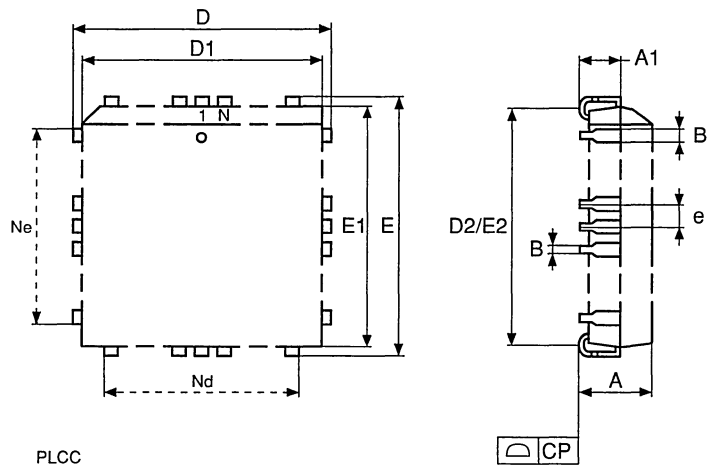
FDIPW-a

Drawing is out of scale

PLCC44 - 44 lead Plastic Leaded Chip Carrier, square

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		4.20	4.70		0.165	0.185
A1		2.29	3.04		0.090	0.120
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		17.40	17.65		0.685	0.695
D1		16.51	16.66		0.650	0.656
D2		14.99	16.00		0.590	0.630
E		17.40	17.65		0.685	0.695
E1		16.51	16.66		0.650	0.656
E2		14.99	16.00		0.590	0.630
e	1.27	–	–	0.050	–	–
N		44			44	
CP			0.10			0.004

PLCC44

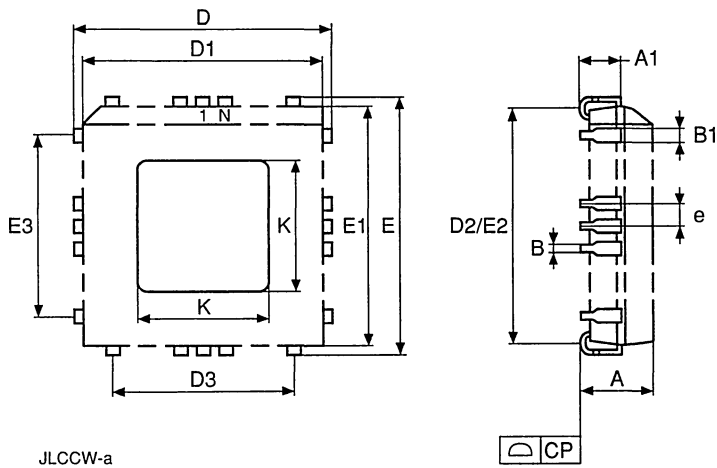


Drawing is out of scale

JLCC44W - 44 lead Ceramic Chip Carrier J-lead, square window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	4.83		0.155	0.190
A1		2.29	3.05		0.090	0.120
B		0.43	0.53		0.017	0.021
B1		0.66	0.81		0.026	0.032
D		17.40	17.65		0.685	0.695
D1		16.00	16.89		0.630	0.665
D2		14.74	16.26		0.580	0.640
D3	12.70	–	–	0.500	–	–
E		17.40	17.65		0.685	0.695
E1		16.00	16.89		0.630	0.665
E2		14.74	16.26		0.580	0.640
E3	12.70	–	–	0.500	–	–
e	1.27	–	–	0.050	–	–
K	10.16	–	–	0.400	–	–
N		44			44	
CP			0.10			0.004

JLCC44W

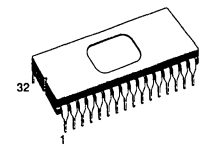


JLCCW-a

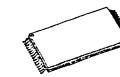
Drawing is out of scale

8 Megabit (1Meg x 8) UV EPROM and OTP ROM

- VERY FAST ACCESS TIME: 90ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 35mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 52sec. (PRESTO IIB ALGORITHM)



FDIP32W (F)



TSOP32 (N)
8 x 20mm

DESCRIPTION

The M27C801 is an high speed 8 Megabit UV erasable and electrically programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. Its is organized as 1,048,576 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C801 is offered in Plastic Thin Small Outline package.

Table 1. Signal Names

A0 - A19	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

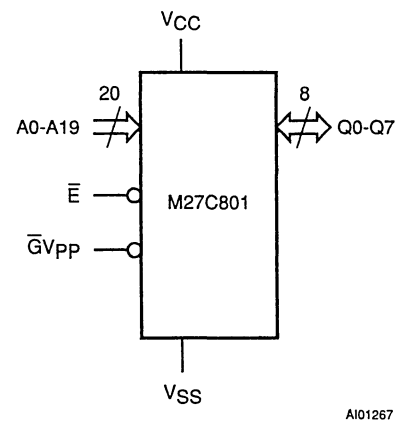


Figure 2A. DIP Pin Connections

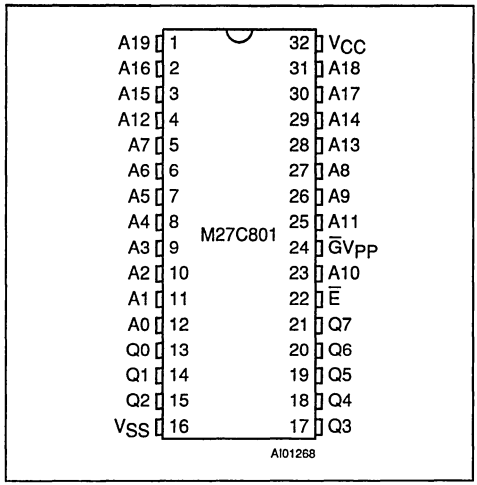
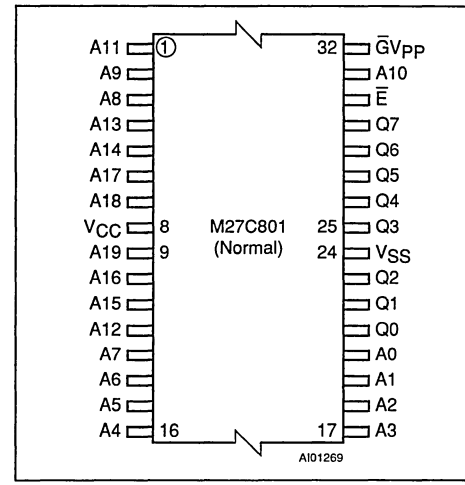


Figure 2B. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operations of the M27C801 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature and Margin Mode Set or Reset .

Read Mode

The M27C801 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C801 has a standby mode which reduces the active current from 35mA to 100µA The M27C801 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C801 are in the '1' state. Data is introduced by selectively programming '0' into the desired bit locations. Although only '0' will be programmed, both '1' and '0' can be present in the data word. The only way to change a '0' to a '1' is by die exposure to ultraviolet light (UV EPROM). The M27C801 is in the programming mode when V_{PP} input is at 12.75V and $\overline{E}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q0 - Q7
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	1	0	42h

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

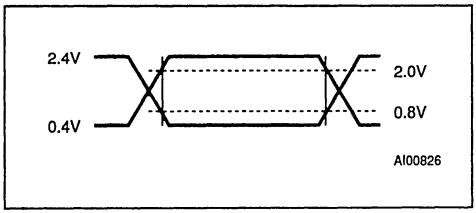


Figure 4. AC Testing Load Circuit

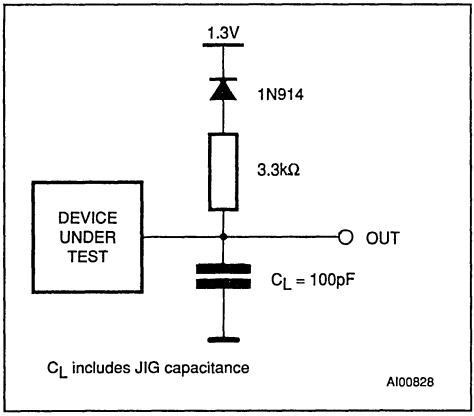


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note. 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		35	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (2)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.7V		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 7A. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C801						Unit
				-90		-100		-120		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}		90		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}V_{PP}$ = V_{IL}		90		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}V_{PP}$ = V_{IL}	0	30	0	30	0	40	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}	0		0		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Table 7B. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C801				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}V_{PP}$ = V_{IL}		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		60		70	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}V_{PP}$ = V_{IL}	0	50	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}	0		0		ns

Notes. 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

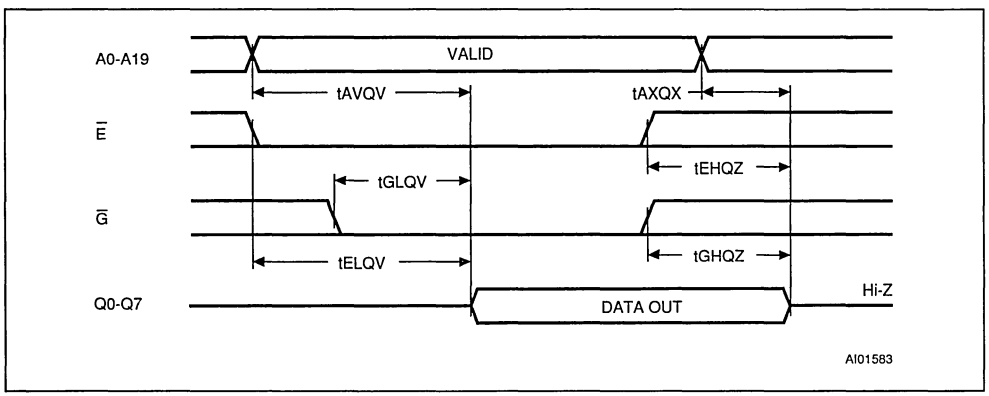


Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. MARGIN MODE AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	VA9 High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	VA10 High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	VA10 Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to VA10 Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to VA9 Transition		2		µs

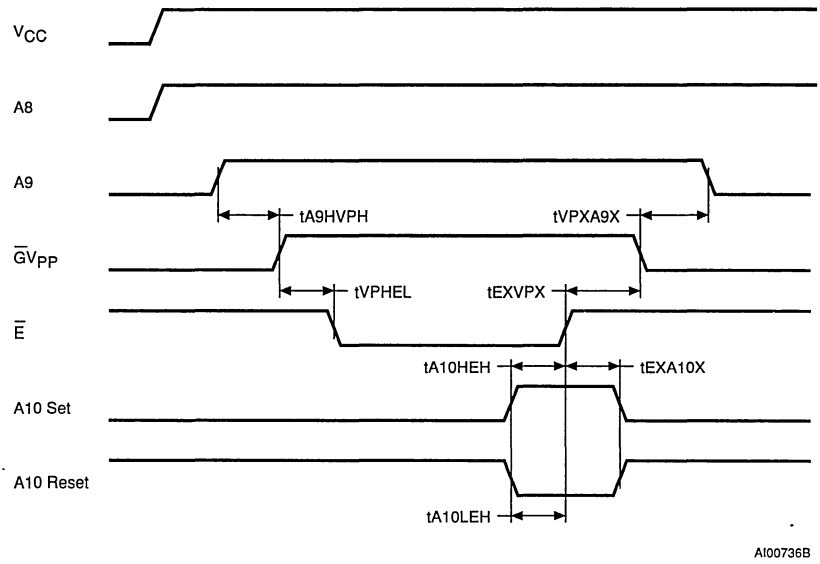
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)		45	55	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		2		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} (2)	t_{DFP}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 6. MARGIN MODE AC Waveforms



Note: A8 High level = 5V; A9 High level = 12V.

Figure 7. Programming and Verify Modes AC Waveforms

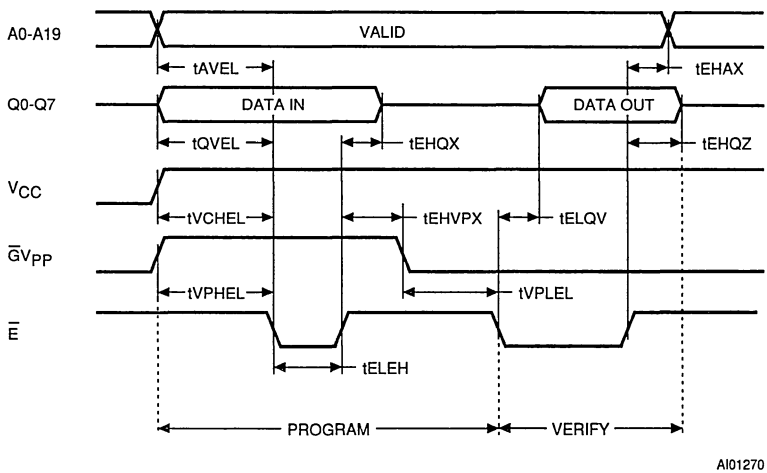
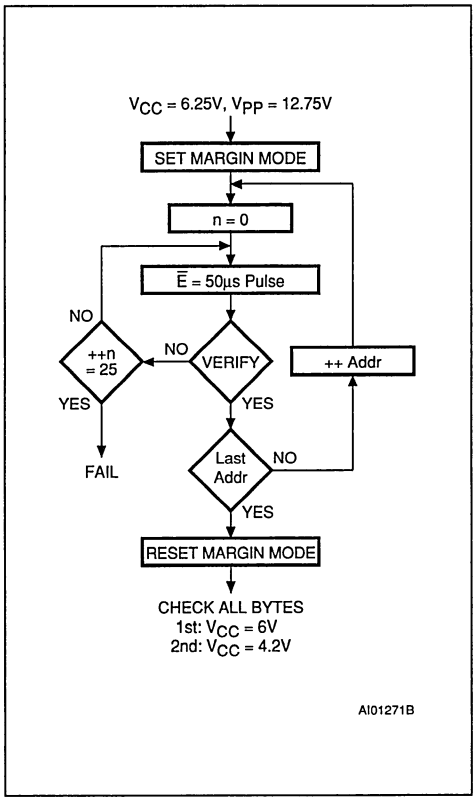


Figure 8. Programming Flowchart



DEVICE OPERATION (cont'd)

The M27C801 can use PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically 52 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used as well.

PRESTO IIB Programming Algorithm

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 52.5 seconds. This can be achieved with SGS-THOMSON M27C801 due to several design innovations to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 50µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

Program Inhibit

Programming of multiple M27C801s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}V_{PP}$ of the parallel M27C801 may be common. A TTL low level pulse applied to a M27C801's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27C801. A high level $\overline{E}$ input inhibits the other M27C801s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C801. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C801. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C801, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C801 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range.

Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C801 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C801 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C801 window to prevent unintentional erasure. The recommended erasure procedure for the M27C801 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C801 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27C801 -100 N 1 TR

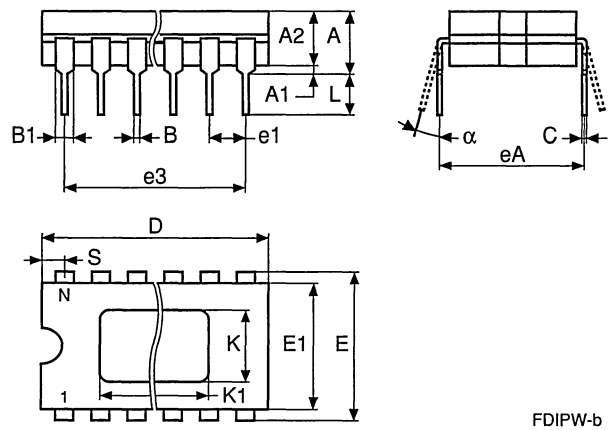
Speed		Package		Temperature Range		Option	
-90	90 ns	F	FDIP32W	1	0 to 70 °C	X	Additional Burn-in
-100	100 ns	N	TSOP32 8 x 20mm	6	–40 to 85 °C	TR	Tape & Reel Packing
-120	120 ns						
-150	150 ns						
-200	200 ns						

For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP32W - 32 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			42.78			1.684
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	38.10	–	–	1.500	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
K		8.79	8.99		0.346	0.354
K1		9.30	9.50		0.366	0.374
α		4°	15°		4°	15°
N	32			32		

FDIP32W



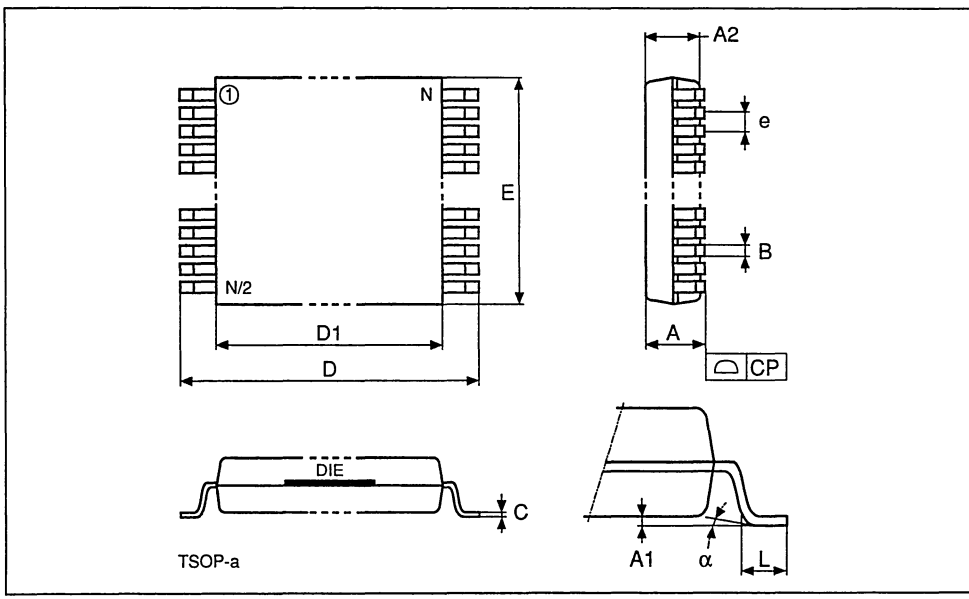
FDIPW-b

Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32

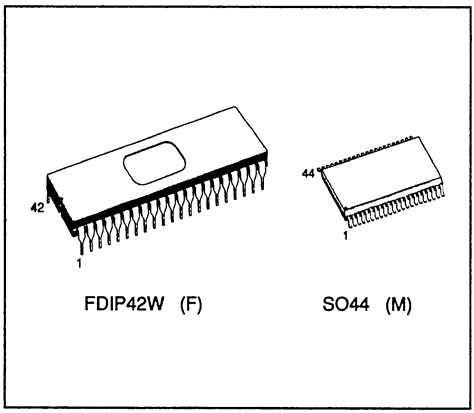


Drawing is out of scale

8 Megabit (1Meg x 8 or 512K x 16) UV EPROM and OTP ROM

PRODUCT PREVIEW

- FAST ACCESS TIME
  - 100ns (Random Address)
- WORD-WIDE or BYTE-WIDE CONFIGURABLE
- 8 Megabit MASK ROM COMPATIBLE
- LOW POWER CONSUMPTION
  - Active Current 70mA at 8MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE 12.5V ± 0.3V
- PROGRAMMING TIME of AROUND 5sec. (PRESTO IV ALGORITHM)
- FDIP42W and SO44 PACKAGES



FDIP42W (F) SO44 (M)

DESCRIPTION

The M27C800 is an 8 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 1Meg words of 8 bit or 512K words of 16 bit. The pin-out is compatible with a 8 Megabit Mask ROM.

The 42 pin Window Ceramic Frit-Seal package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C800 is offered in 44 pin Plastic Small Outline package.

Figure 1. Logic Diagram

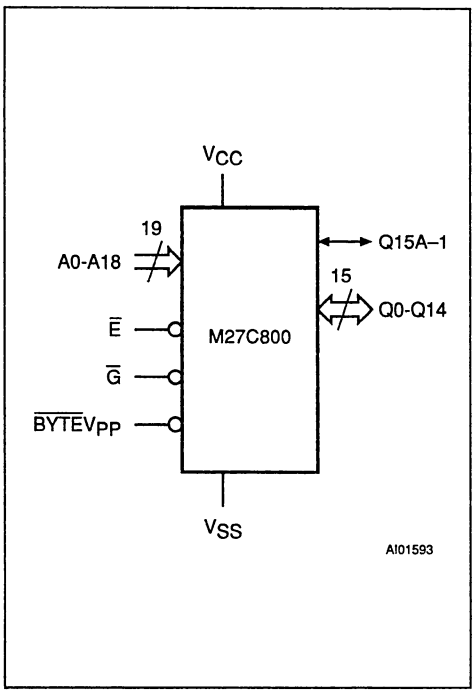
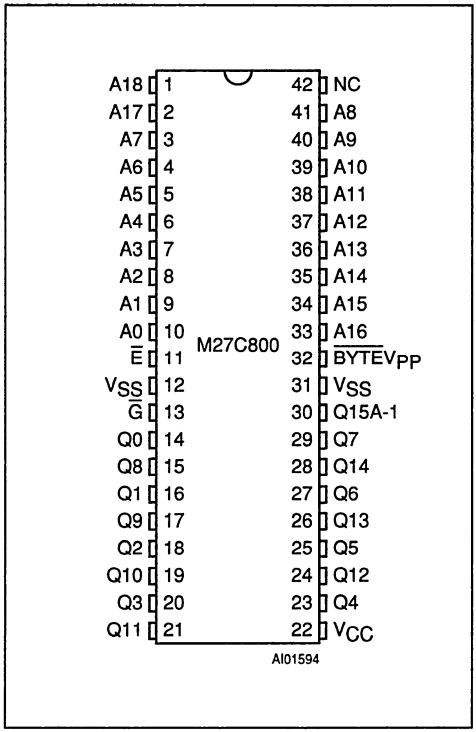


Table 1. Signal Names

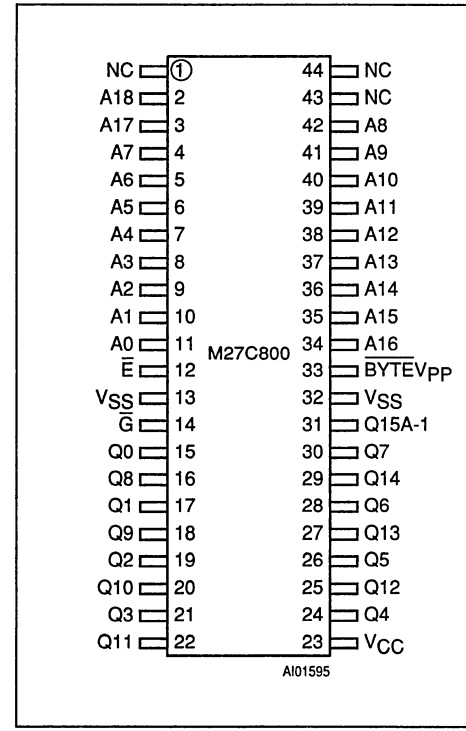
A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
Q8 - Q14	Data Outputs
Q15A-1	Data Output / Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{BYTE}V_{PP}$	Byte Mode / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{BYTE}V_{PP}$	A9	Q0 - Q7	Q8 - Q14	Q15A-1
Read Word-wide	V_{IL}	V_{IL}	V_{IH}	X	Data Out	Data Out	Data Out
Read Byte-wide Upper	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IH}
Read Byte-wide Lower	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IL}
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z	Hi-Z	Hi-Z
Program	V_{IL} Pulse	V_{IH}	V_{PP}	X	Data In	Data In	Data In
Verify	X	V_{IL}	V_{PP}	X	Data Out	Data Out	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes	Codes	Code

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7 or Q15	Q6 or Q14	Q5 or Q13	Q4 or Q12	Q3 or Q11	Q2 or Q10	Q1 or Q9	Q0 or Q8	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	1	0	0	1	0	B2h

Table 5. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 8Mhz		70	mA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
I_{OS}	Output Short Circuit Current	Note 2 and 3		100	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (4)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

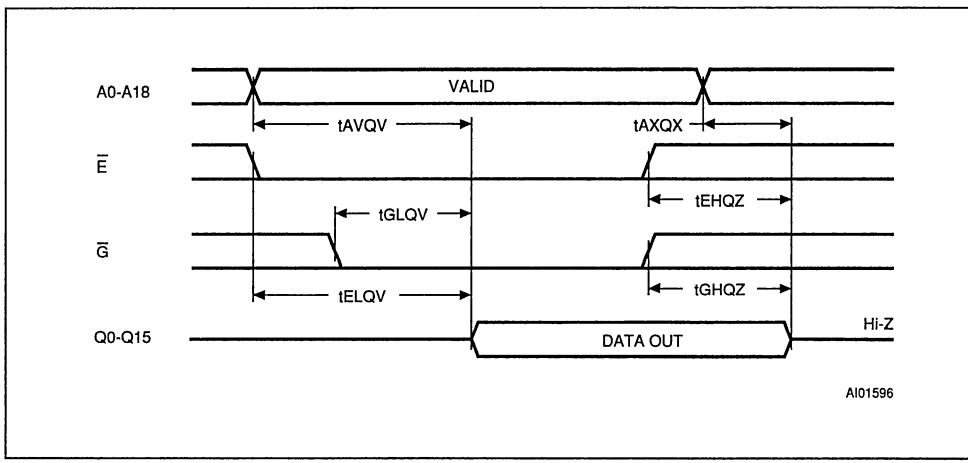
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. Sampled only, not 100% tested.
3. Output shortcircuited for no more than one second. No more than one output shorted at a time.
4. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 6. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C800				Unit
				-100		-120		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{BHQV}	t_{ST}	BYTE High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		60	ns
t_{BLQZ} (2)	t_{STD}	BYTE Low to Output Hi-Z	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		40		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	5		5		ns
t_{BLQX}	t_{OH}	BYTE Low to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	5		5		ns

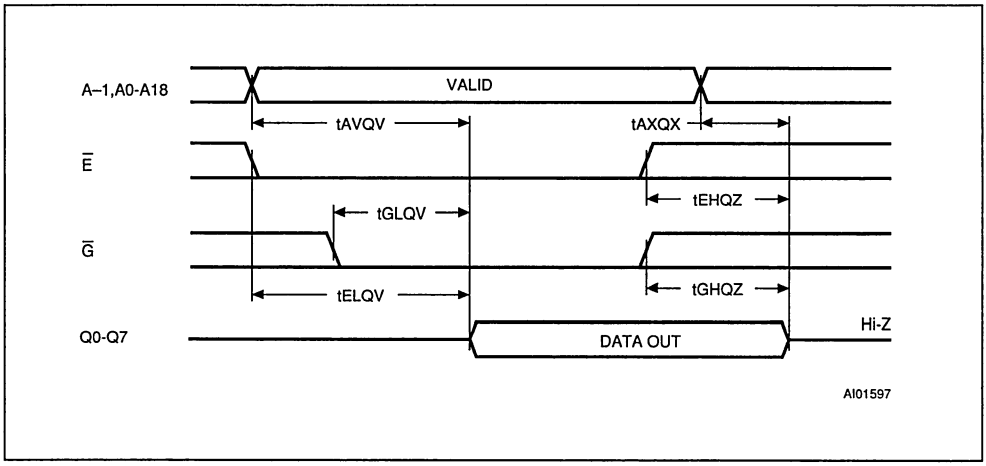
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Figure 3. Word-Wide Read Mode AC Waveforms



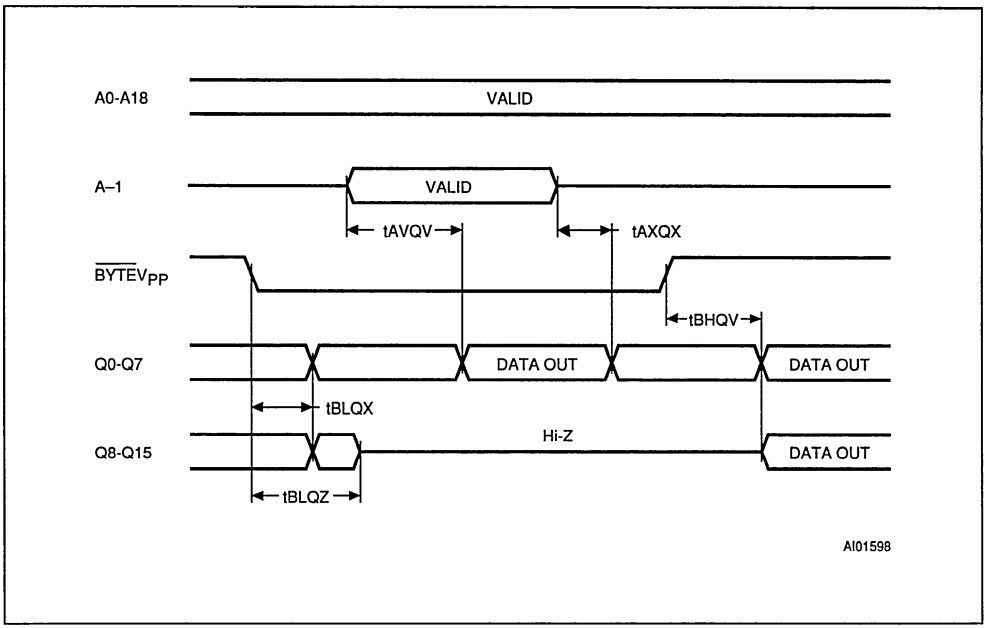
Note: $\overline{BYTE}V_{PP}$ = V_{IH}

Figure 4. Byte-Wide Read Mode AC Waveforms



Note: $\overline{BYTE}V_{PP} = V_{IL}$

Figure 5. $\overline{BYTE}$ Transition AC Waveforms



Note: $\overline{E}$ and $\overline{G} = V_{IL}$

AC Measurement Conditions

Input Rise and Fall Times	< 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 6. AC Testing Input Output Waveforms

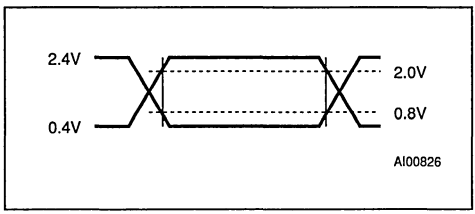


Figure 7. AC Testing Load Circuit

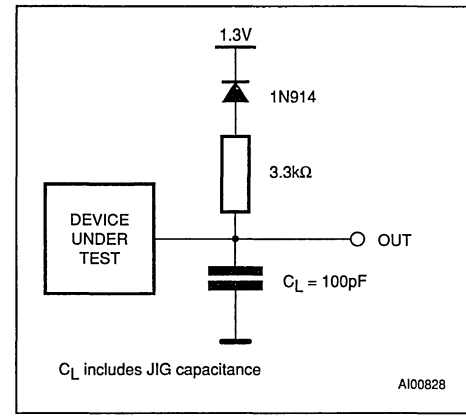


Table 7. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except $\overline{BYTE}V_{PP}$)	V_{IN} = 0V		10	pF
	Input Capacitance ($\overline{BYTE}V_{PP}$)	V_{IN} = 0V		120	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±1	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.4	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	3.5		V
V_{ID}	A9 Voltage		11.5	12.5	V

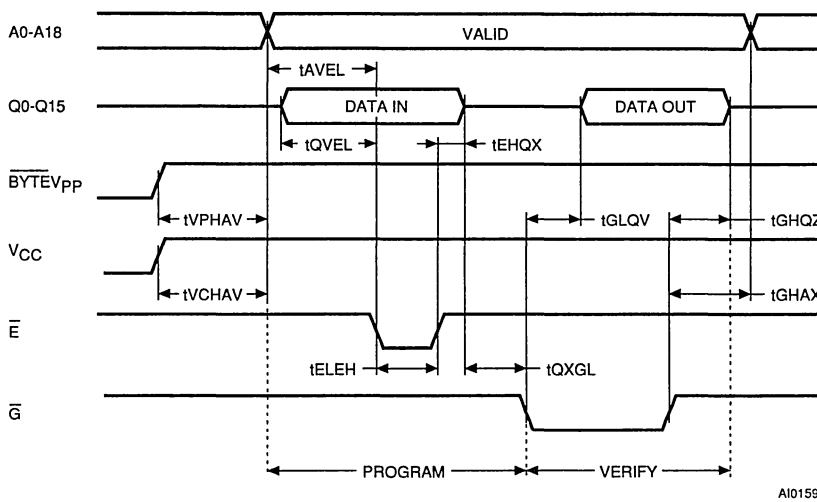
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHAV}	t_{VPS}	V_{PP} High to Address Valid		2		µs
t_{VCHAV}	t_{VCS}	V_{CC} High to Address Valid		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		9.5	10.5	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			120	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 8. Programming and Verify Modes AC Waveforms



DEVICE OPERATION

The operating modes of the M27C800 are listed in the Operating Modes Table. A single 5V supply is required in the read mode. All inputs are TTL compatible except for V_{PP} and 12V on A9 for the Electronic Signature.

Read Mode

The M27C800 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the $\overline{BYTE}V_{PP}$ pin. When $\overline{BYTE}V_{PP}$ is at V_{IH} the Word-wide organisation is selected and the Q15A-1 pin is used for Q15 Data Output. When the $\overline{BYTE}V_{PP}$ pin is at V_{IL} the Byte-wide organisation is selected and the Q15A-1 pin is used for the Address Input A-1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A-1 at V_{IL} the lower 8 bits of the 16 bit data are selected and with A-1 at V_{IH} the upper 8 bits of the 16 bit data are selected.

The M27C800 has two control inputs, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte- wide organisation must be selected.

The $\overline{E}$ signal is the power control and should be used for device selection. The $\overline{G}$ signal is the output control and should be used to gate data to the output pins. With $\overline{E}=V_{IL}$ and $\overline{G}=V_{IL}$ the output data will be valid in a time t_{AVQV} after the all address lines are valid and stable.

The Chip Enable to Output Valid time t_{ELQV} is equal to the Address Valid to output Valid time t_{AVQV}. When the Addresses are valid and $\overline{E}=V_{IL}$, the output data is valid after a time of t_{GLQV} from the falling edge of the Output Enable signal.

Standby Mode

The M27C800 has a standby mode which reduces the active current from 50mA (f = 5MHz) to 100µA. The standby mode is entered by applying a CMOS high level V_{CC} –0.2V to $\overline{E}$. When in the standby mode the outputs are in an high impedance state, independant of the $\overline{G}$ input level.

Output Disable Mode

When EPROMs are used in memory arrays two line output control should be used. This function uses the output disable mode which allows:

a. the lowest possible power consumption

b. complete assurance that output bus contention will not occur

For the best use of the two control lines $\overline{E}$ and $\overline{G}$, the input $\overline{E}$ should be decoded and used as the primary selection, while $\overline{G}$ should be made a common connection to all memories in the array. $\overline{G}$ should be connected to the $\overline{READ}$ signal of the system bus. This will ensure that all deselected devices are in the low power standby mode and that the output lines are only active when data is required from a particular memory device.

System Considerations

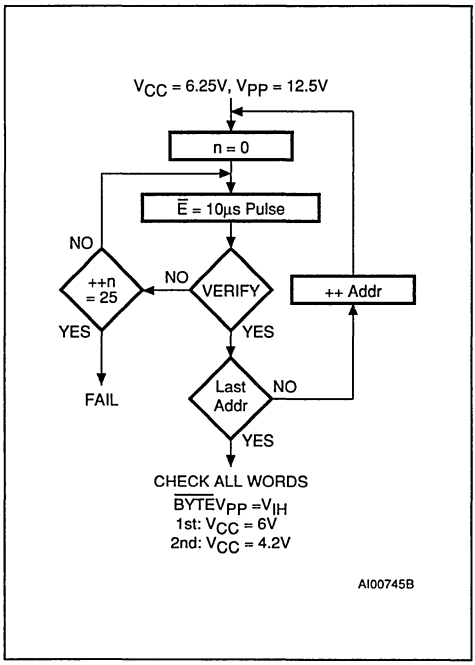
The power switching characteristics of Advanced CMOS EPROMs require carefull decoupliing of the supplies to the devices. The supply current I_{CC} has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of $\overline{E}$.

The magnitude of the transient current peaks is dependant on the capacititive and inductive loading of the device outputs. The associated transient voltage peaks can be supressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor is used on every device between V_{CC} and V_{SS}. This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a 4.7µF electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programing

When first delivered, and after erasure for UV EPROMs, all bits are in the "1" logic state (Output High). Data with both "1's" and "0's" is applied and the "0s'" are programed into the memory array. For programing V_{CC} is raised to 6.25V. The M27C800 is in the Program Mode when V_{PP} is at 12.75V, $\overline{G}$ is at V_{IH} and $\overline{E}$ is pulsed to V_{IL}. Data to be programed is applied 16 bits in parallel to the data output pins Q0-Q15.

Figure 9. Programming Flowchart



PRESTO IV Program Algorithm

The PRESTO IV Algorithm allows the whole 8 Megabit array to be programed with a guaranteed margin in a typical time of 5 seconds. The algorithm applies a series of 10µs program pulses to each word until a correct verify is made. During programing and verify a MARGIN MODE circuit is automatically activated to guarantee that each cell is programed with an adequate margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the neccessary threshold margin for each cell.

Program Inhibit

Multiple M27C800s may be programed in parallel with different data. This is done by putting in parallel all inputs except $\overline{E}$ and $\overline{G}$. With V_{CC} at 6.25V and V_{PP} at 12.5V, data should be applied to all devices and $\overline{G}$ placed at V_{IH}. Low level pulses on the $\overline{E}$ of one device will program that device.

Program Verify

After each program pulse a verify read is made by reading the data output with V_{CC} at 6.25V, V_{PP} at 12.5V and $\overline{G}$ placed at V_{IL}.

Electronic Signature

The Electronic Signature Mode allows a binary code to be read from the EPROM which identifies the Manufacturer and Device Type. These codes are intended to be used to match the programing equipment to the device being programed and its corresponding algorithm.

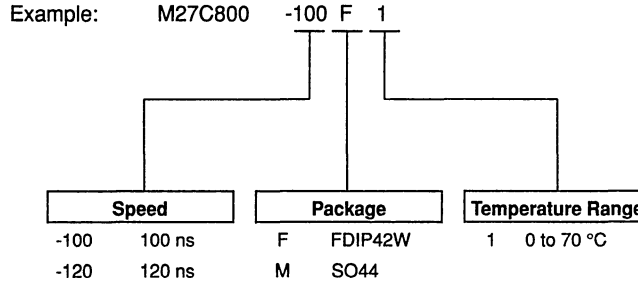
The Electronic Signature Mode is activated by applying a voltage V_{ID} of 12V to the Address line A9 and V_{IL} to all other Address lines, with $\overline{E}$ and $\overline{G}$ at V_{IL} and $\overline{BYTE}$ at V_{IH}. The identifier bytes may be read from either Q0-Q7 or Q8-Q15. With Address line A0 at V_{IL} the byte output is the Manufacture's code, with A0 at V_{IH} the byte identifies the Device Type. The codes for the SGS-THOMSON M27C800 are given in Table 4.

Erasure

The erasure of the M27C800 begins when the cells are exposed to light of wavelengths shorter than approximately 4000 Å. Sunlight and some types of fluorescent lamps have wavelengths in the 3000 - 4000 Å range. Constant exposure to room level fluorescent lighting could erase a typical EPROM in about 3 years, while it takes approximately 170 hours to cause erasure when exposed to direct sunlight. To prevent accidental erasure it is recommended that opaque labels be placed over the M27C800 window.

The erase procedure for the M27C800 is exposure to UV light with a wavelength of 2537 Å. The integrated dose (UV intensity x time) for erasure should be a minimum of 15 W-sec/cm^2. The erase time with this dosage is 15 to 20 minutes using an UV lamp with 12,000 µW/cm^2 rating. The M27C800 should be placed within 2.5cm of the lamp tube during erasure. No filter should be used on the lamp.

ORDERING INFORMATION SCHEME



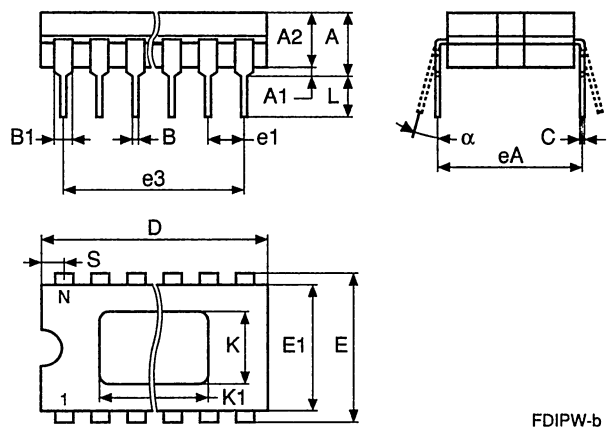
For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP42W - 42 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			54.81			2.158
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	50.80	–	–	2.000	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
K	–	–	–	–	–	–
K1	–	–	–	–	–	–
α		4°	15°		4°	15°
N	42			42		

FDIP42W



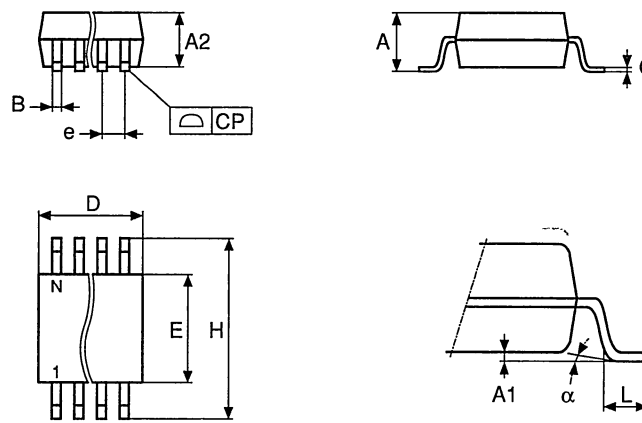
FDIPW-b

Drawing is out of scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27	–	–	0.050	–	–
H		15.90	16.10		0.626	0.634
L	0.80	–	–	0.031	–	–
α	3°	–	–	3°	–	–
N		44			44	
CP			0.10			0.004

SO44

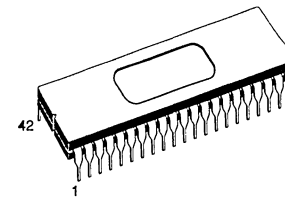


SO-b

Drawing is out of scale

16 Megabit (2Meg x 8 or 1Meg x 16) UV EPROM

- FAST ACCESS TIME: 140ns
- WORD-WIDE or BYTE-WIDE CONFIGURABLE
- 16 Megabit, 42 Pin, MASK ROM COMPATIBLE
- LOW POWER CONSUMPTION
  - Active Current 70mA at 8MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE 12.5V ± 0.3V
- PROGRAMMING TIME of AROUND 50sec. (PRESTO III ALGORITHM)
- ***SPECIFICATION VARIATION: Please refer to the last page of this data sheet for specification variation on Electronic Signature.***



FDIP42W (F)

DESCRIPTION

The M27C160 is a 16 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 2Meg words of 8 bit or 1Meg words of 16 bit. The pin-out is compatible with a 16 Megabit Mask ROM.

The 42 pin Window Ceramic Frit-Seal package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.

Table 1. Signal Names

A0 - A19	Address Inputs
Q0 - Q7	Data Outputs
Q8 - Q14	Data Outputs
Q15A-1	Data Output / Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{BYTE}V_{PP}$	Byte Mode / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

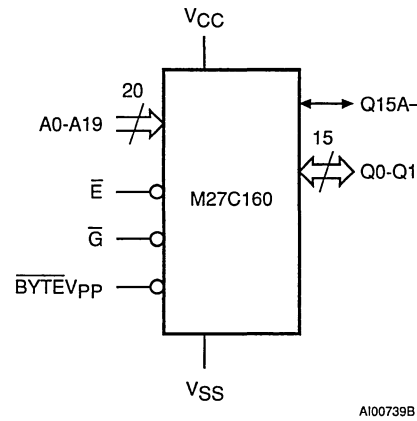
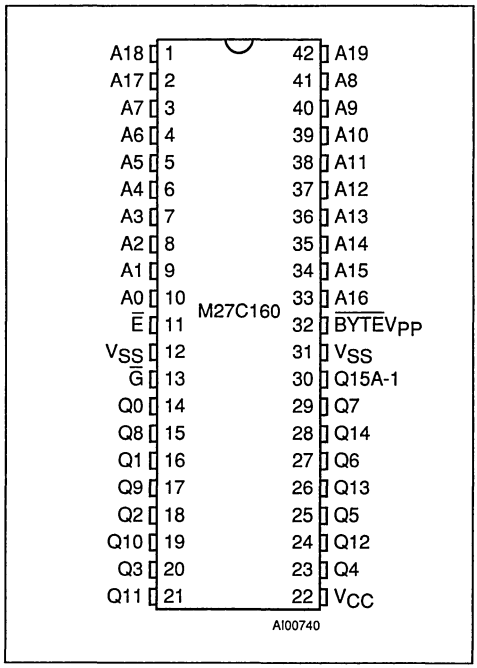


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The operating modes of the M27C160 are listed in the Operating Modes Table. A single 5V supply is required in the read mode. All inputs are TTL compatible except for V_{PP} and 12V on A9 for the Electronic Signature.

Read Mode

The M27C160 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the $\overline{BYTE}V_{PP}$ pin. When $\overline{BYTE}V_{PP}$ is at V_{IH} the Word-wide organisation is selected and the Q15A-1 pin is used for Q15 Data Output. When the $\overline{BYTE}V_{PP}$ pin is at V_{IL} the Byte-wide organisation is selected and the Q15A-1 pin is used for the Address Input A-1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A-1 at V_{IL} the lower 8 bits of the 16 bit data are selected and with A-1 at V_{IH} the upper 8 bits of the 16 bit data are selected.

The M27C160 has two control inputs, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte-wide organisation must be selected. The $\overline{E}$ signal is the power control and should be used for device selection. The $\overline{G}$ signal is the output control and should be used to gate data to the output pins. With $\overline{E}=V_{IL}$ and $\overline{G}=V_{IL}$ the output data will be valid in a time t_{AVQV} after the all address lines are valid and stable. The Chip Enable to Output Valid time t_{ELQV} is equal to the Address Valid to output Valid time t_{AVQV}. When the Addresses are valid and $\overline{E}=V_{IL}$, the output data is valid after a time of t_{GLQV} from the falling edge of the Output Enable signal.

Standby Mode

The M27C160 has a standby mode which reduces the active current from 50mA (f = 5MHz) to 100µA. The standby mode is entered by applying a CMOS high level V_{CC} –0.2V to $\overline{E}$. When in the standby mode the outputs are in an high impedance state, independant of the $\overline{G}$ input level.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{BYTE}V_{PP}$	A9	Q0 - Q7	Q8 - Q14	Q15A-1
Read Word-wide	V_{IL}	V_{IL}	V_{IH}	X	Data Out	Data Out	Data Out
Read Byte-wide Upper	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IH}
Read Byte-wide Lower	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IL}
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z	Hi-Z	Hi-Z
Program	V_{IL} Pulse	V_{IH}	V_{PP}	X	Data In	Data In	Data In
Verify	X	V_{IL}	V_{PP}	X	Data Out	Data Out	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes	Codes	Code

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7 or Q15	Q6 or Q14	Q5 or Q13	Q4 or Q12	Q3 or Q11	Q2 or Q10	Q1 or Q9	Q0 or Q8	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	1	0	0	0	1	B1h

Note: See Specification Variation (Ref. 94-07) on last page.

Table 5. Read Mode DC Characteristics (1)

(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 8Mhz		70	mA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V		100	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
I_{OS}	Output Short Circuit Current	Note 2 and 3		100	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (4)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

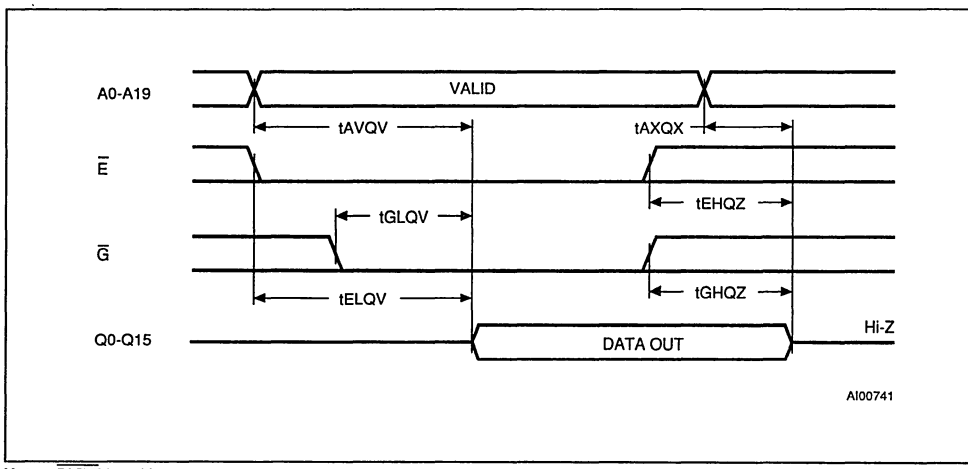
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. Sampled only, not 100% tested.
3. Output shortcircuited for no more than one second. No more than one output shorted at a time.
4. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 6. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C160						Unit
				-140		-150		-200		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		140		150		200	ns
t_{BHQV}	t_{ST}	BYTE High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		140		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		140		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		60		70	ns
t_{BLQZ} (2)	t_{STD}	BYTE Low to Output Hi-Z	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		50		50		60	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	50	0	60	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		5		5		ns
t_{BLQX}	t_{OH}	BYTE Low to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		5		5		ns

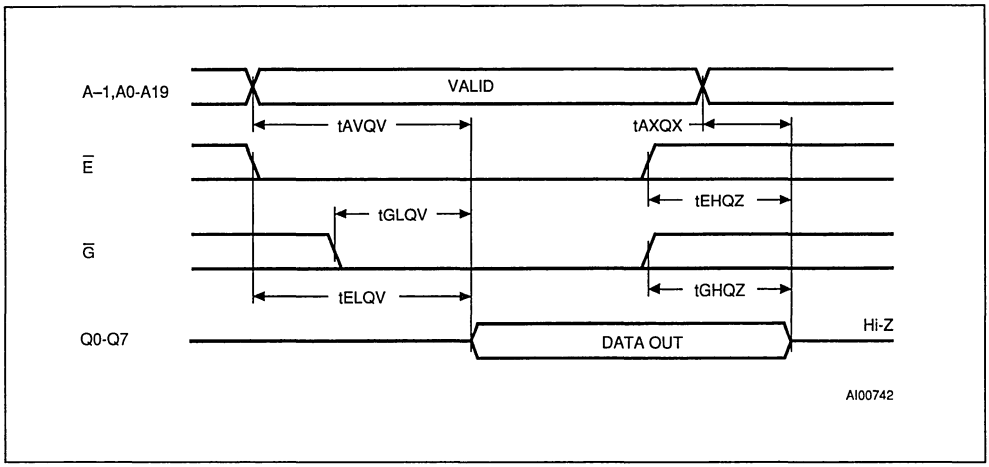
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Figure 3. Word-Wide Read Mode AC Waveforms



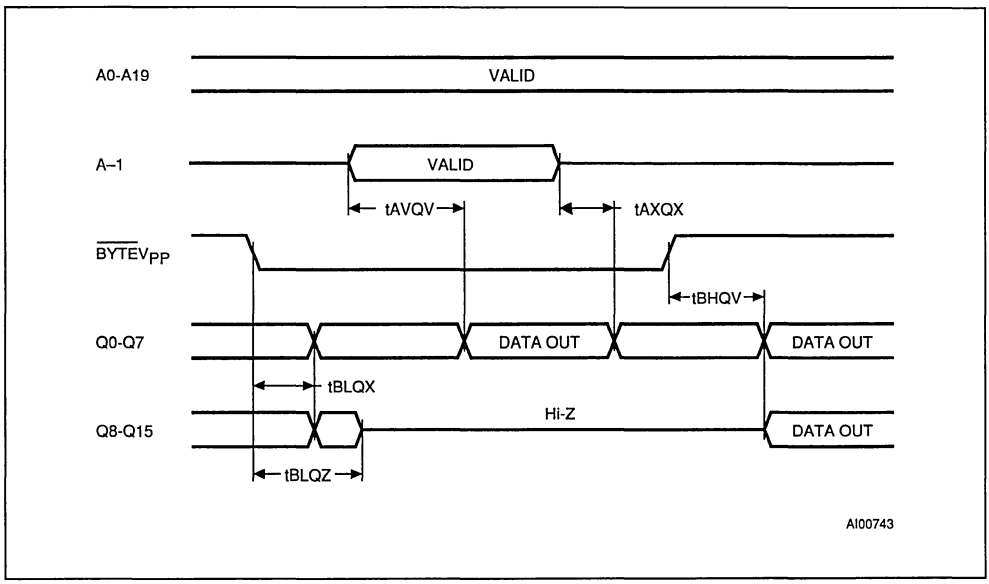
Note: $\overline{BYTE}V_{PP}$ = V_{IH}

Figure 4. Byte-Wide Read Mode AC Waveforms



Note: $\overline{BYTEV}_{PP} = V_{IL}$

Figure 5. $\overline{BYTE}$ Transition AC Waveforms



Note: $\overline{E}$ and $\overline{G} = V_{IL}$

AC Measurement Conditions

Input Rise and Fall Times	< 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 6. AC Testing Input Output Waveforms

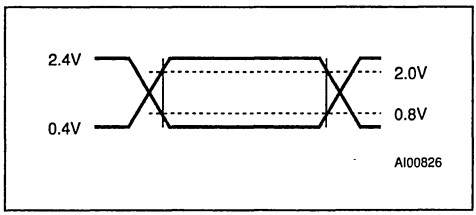


Figure 7. AC Testing Load Circuit

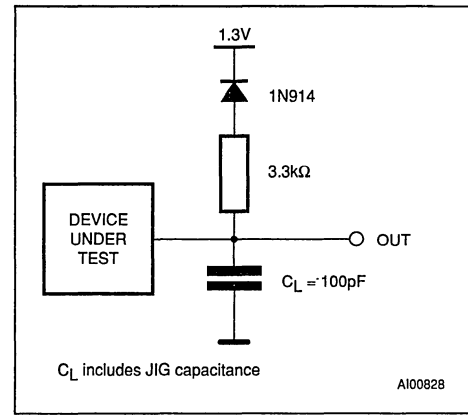


Table 7. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except $\overline{BYTE}V_{PP}$)	V_{IN} = 0V		10	pF
	Input Capacitance ($\overline{BYTE}V_{PP}$)	V_{IN} = 0V		120	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±1	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.4	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	3.5		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHAV}	t_{VPS}	V_{PP} High to Address Valid		2		µs
t_{VCHAV}	t_{VCS}	V_{CC} High to Address Valid		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		45	55	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			120	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 8. Programming and Verify Modes AC Waveforms

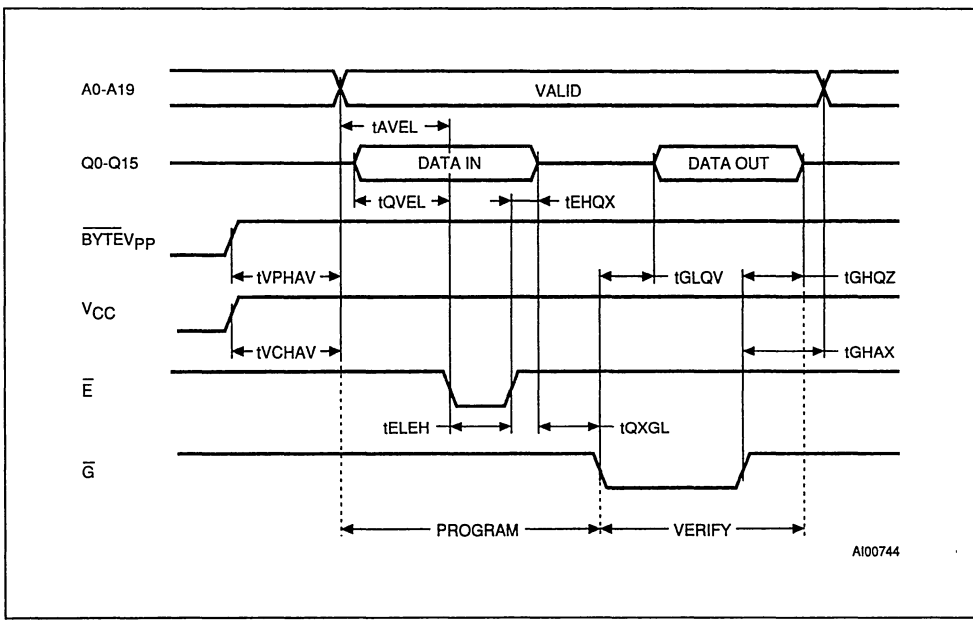
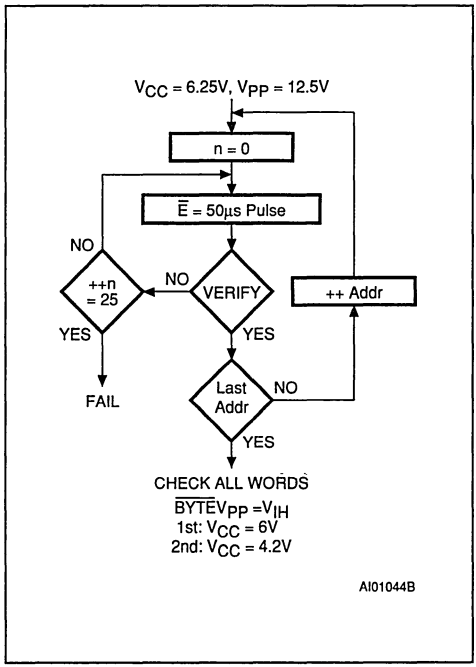


Figure 9. Programming Flowchart



Output Disable Mode

When EPROMs are used in memory arrays two line output control should be used. This function uses the output disable mode which allows:

a. the lowest possible power consumption

b. complete assurance that output bus contention will not occur

For the best use of the two control lines $\overline{E}$ and $\overline{G}$, the input $\overline{E}$ should be decoded and used as the primary selection, while $\overline{G}$ should be made a common connection to all memories in the array. $\overline{G}$ should be connected to the $\overline{READ}$ signal of the system bus. This will ensure that all deselected devices are in the low power standby mode and that the output lines are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require carefull decoupliing of the supplies to the devices. The supply current I_{CC} has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of $\overline{E}$.

The magnitude of the transient current peaks is dependant on the capacititive and inductive loading of the device outputs. The associated transient voltage peaks can be supressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor is used on every device between V_{CC} and V_{SS}. This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a 4.7µF electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programing

When first delivered, and after erasure for UV EPROMs, all bits are in the "1" logic state (Output High). Data with both "1's" and "0's" is applied and the "0s'" are programed into the memory array. For programing V_{CC} is raised to 6.25V. The M27C160 is in the Program Mode when V_{PP} is at 12.75V, $\overline{G}$ is at V_{IH} and $\overline{E}$ is pulsed to V_{IL}. Data to be programed is applied 16 bits in parallel to the data output pins Q0 - Q15.

PRESTO III Programming Algorithm

The PRESTO III Algorithm allows the whole 16 Megabit array to be programed with a guaranteed margin in a typical time of 52.5 seconds. The algorithm applies a series of 50µs program pulses to each word until a correct verify is made. During programing and verify a MARGIN MODE circuit is automatically activated to guarantee that each cell is programed with an adequate margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the neccessary threshold margin for each cell.

Program Inhibit

Multiple M27C160s may be programed in parallel with different data. This is done by putting in parallel all inputs except $\overline{E}$ and $\overline{G}$. With V_{CC} at 6.25V and V_{PP} at 12.5V, data should be applied to all devices and $\overline{G}$ placed at V_{IH}. Low level pulses on the $\overline{E}$ of one device will program that device.

Program Verify

After each program pulse a verify read is made by reading the data output with V_{CC} at 6.25V, V_{PP} at 12.5V and $\overline{G}$ placed at V_{IL}.

Electronic Signature

See Specification Variation (Ref. 94-07) on last page.

The Electronic Signature Mode allows a binary code to be read from the EPROM which identifies

the Manufacturer and Device Type. These codes are intended to be used to match the programing equipment to the device being programed and its corresponding algorithm.

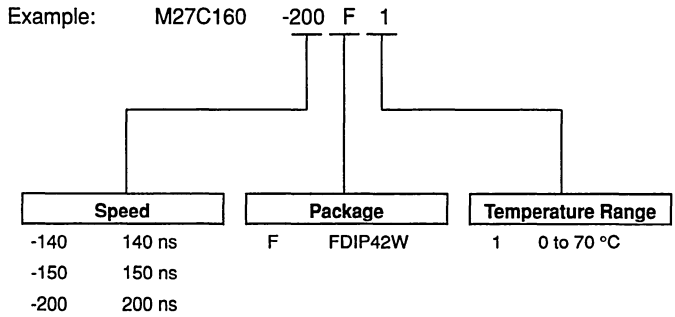
The Electronic Signature Mode is activated by applying a voltage V_{ID} of 12V to the Address line A9 and V_{IL} to all other Address lines, with $\overline{E}$ and $\overline{G}$ at V_{IL} and $\overline{BYTE}$ at V_{IH}. The identifier bytes may be read from either Q0-Q7 or Q8-Q15. With Address line A0 at V_{IL} the byte output is the Manufacture's code, with A0 at V_{IH} the byte identifies the Device Type. The codes for the SGS-THOMSON M27C160 are given in Table 4.

Erasure

The erasure of the M27C160 begins when the cells are exposed to light of wavelengths shorter than approximately 4000 Å. Sunlight and some types of fluorescent lamps have wavelengths in the 3000 - 4000 Å range. Constant exposure to room level fluorescent lighting could erase a typical EPROM in about 3 years, while it takes approximately 170 hours to cause erasure when exposed to direct sunlight. To prevent accidental erasure it is recommended that opaque labels be placed over the M27C160 window.

The erase procedure for the M27C160 is exposure to UV light with a wavelength of 2537 Å. The integrated dose (UV intensity x time) for erasure should be a minimum of 15 W-sec/cm^2. The erase time with this dosage is 15 to 20 minutes using an UV lamp with 12,000 µW/cm^2 rating. The M27C160 should be placed within 2.5cm of the lamp tube during erasure. No filter should be used on the lamp.

ORDERING INFORMATION SCHEME



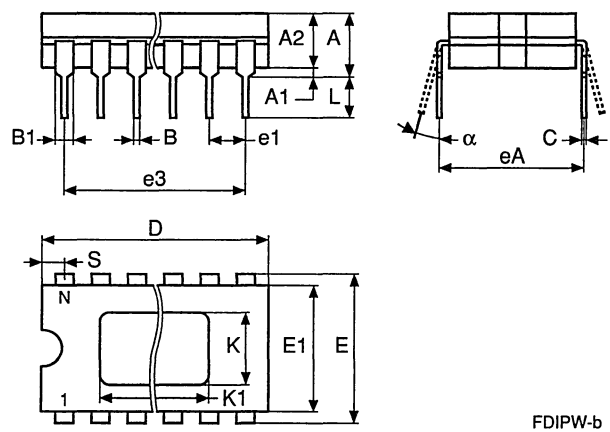
For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP42W - 42 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			54.81			2.158
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	50.80	–	–	2.000	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
K		8.56	8.71		0.337	0.343
K1		20.19	20.45		0.795	0.805
α		4°	15°		4°	15°
N		42			42	

FDIP42W



FDIPW-b

Drawing is out of scale

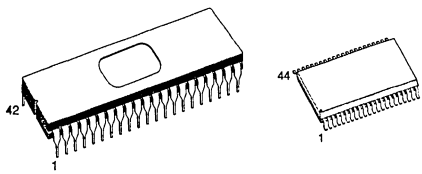
SGS-THOMSON MICROELECTRONICS

M27C160

16 Megabit (2Meg x 8 or 1Meg x 16) UV EPROM and OTP ROM

PRODUCT PREVIEW

- FAST ACCESS TIME
  - 100ns (Random Address)
- WORD-WIDE or BYTE-WIDE CONFIGURABLE
- 16 Megabit MASK ROM COMPATIBLE
- LOW POWER CONSUMPTION
  - Active Current 70mA at 8MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE 12.5V ± 0.3V
- PROGRAMMING TIME of AROUND 10sec. (PRESTO IV ALGORITHM)
- FDIP42W and SO44 PACKAGES



FDIP42W (F) SO44 (M)

DESCRIPTION

The M27C160 is a 16 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 2Meg words of 8 bit or 1Meg words of 16 bit. The pin-out is compatible with a 16 Megabit Mask ROM.

The 42 pin Window Ceramic Frit-Seal package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C160 is offered in 44 pin Plastic Small Outline package.

Table 1. Signal Names

A0 - A19	Address Inputs
Q0 - Q7	Data Outputs
Q8 - Q14	Data Outputs
Q15A-1	Data Output / Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{BYTE}V_{PP}$	Byte Mode / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

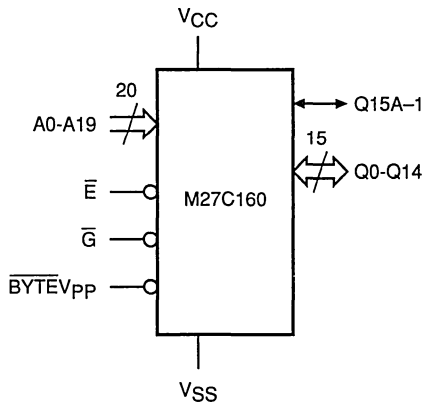


Figure 2A. DIP Pin Connections

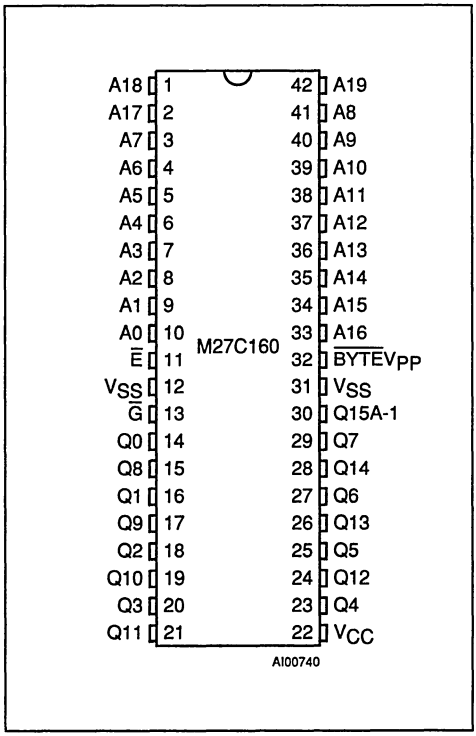
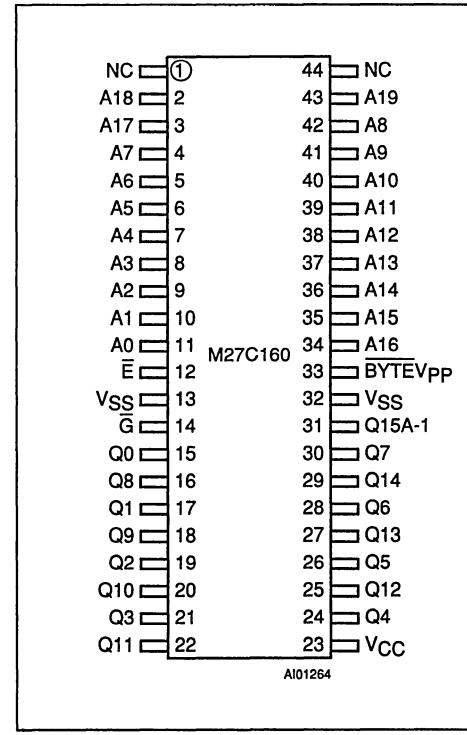


Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{BYTE}V_{PP}$	A9	Q0 - Q7	Q8 - Q14	Q15A-1
Read Word-wide	V_{IL}	V_{IL}	V_{IH}	X	Data Out	Data Out	Data Out
Read Byte-wide Upper	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IH}
Read Byte-wide Lower	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IL}
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z	Hi-Z	Hi-Z
Program	V_{IL} Pulse	V_{IH}	V_{PP}	X	Data In	Data In	Data In
Verify	X	V_{IL}	V_{PP}	X	Data Out	Data Out	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes	Codes	Code

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7 or Q15	Q6 or Q14	Q5 or Q13	Q4 or Q12	Q3 or Q11	Q2 or Q10	Q1 or Q9	Q0 or Q8	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	1	0	0	0	1	B1h

Table 5. Read Mode DC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 8Mhz		70	mA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$		100	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	µA
I_{OS}	Output Short Circuit Current	Note 2 and 3		100	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH} (4)	Input High Voltage		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

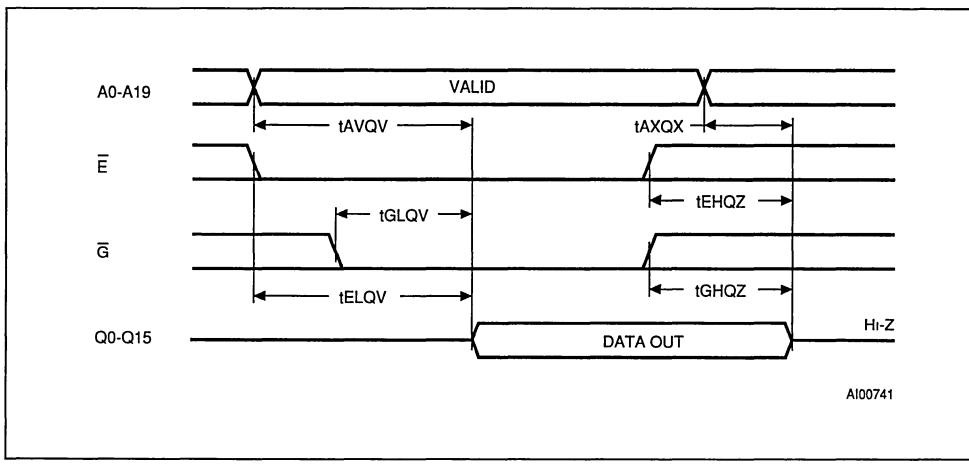
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. Sampled only, not 100% tested.
3. Output shortcircuited for no more than one second. No more than one output shorted at a time.
4. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 6. Read Mode AC Characteristics (1)
(T_A = 0 to 70 °C; V_{CC} = 5V ± 10%; V_{PP} = V_{CC})

Symbol	Alt	Parameter	Test Condition	M27C160				Unit
				-100		-120		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{BHQV}	t_{ST}	BYTE High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		60	ns
t_{BLQZ} (2)	t_{STD}	BYTE Low to Output Hi-Z	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		40		50	ns
t_{EHQZ} (2)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	50	ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	5		5		ns
t_{BLQX}	t_{OH}	BYTE Low to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	5		5		ns

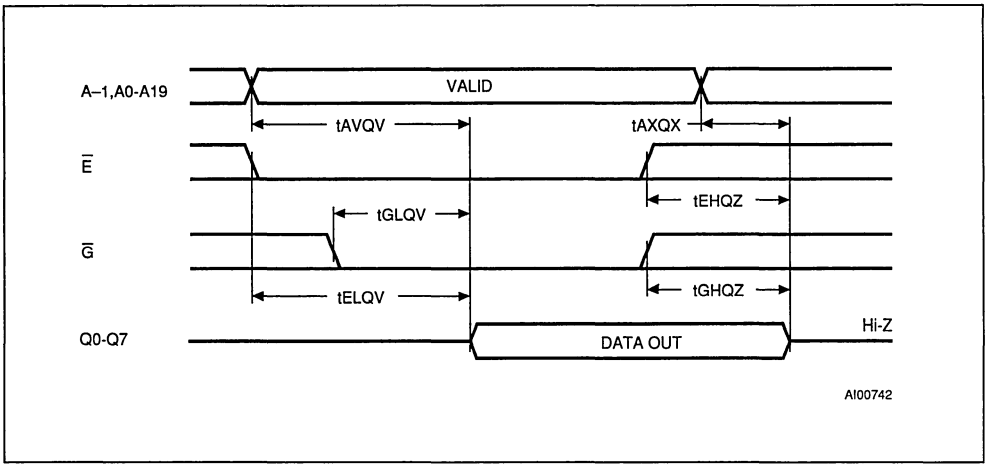
Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}
2. Sampled only, not 100% tested.

Figure 3. Word-Wide Read Mode AC Waveforms



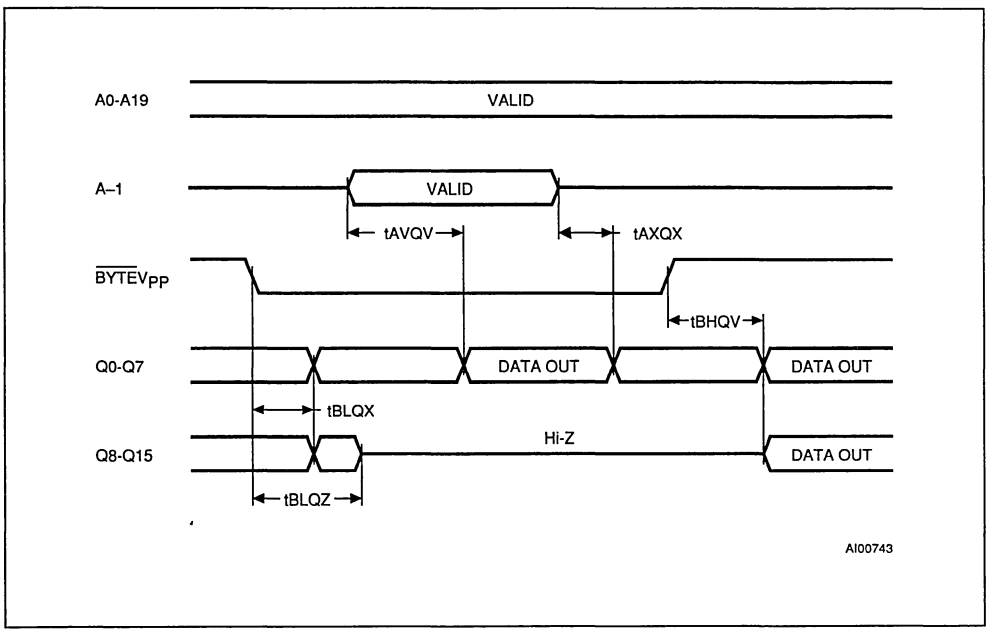
Note: $\overline{BYTE}$/V_{PP} = V_{IH}

Figure 4. Byte-Wide Read Mode AC Waveforms



Note: $\overline{BYTE}V_{PP} = V_{IL}$

Figure 5. $\overline{BYTE}$ Transition AC Waveforms



Note: $\overline{E}$ and $\overline{G} = V_{IL}$

AC Measurement Conditions

Input Rise and Fall Times	< 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 6. AC Testing Input Output Waveforms

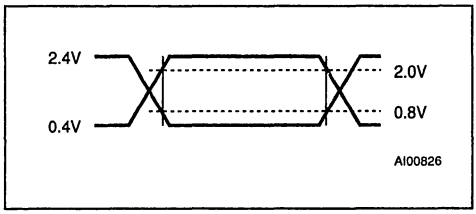


Figure 7. AC Testing Load Circuit

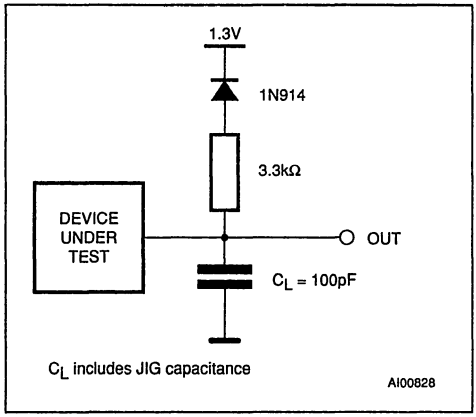


Table 7. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except $\overline{BYTE}V_{PP}$)	V_{IN} = 0V		10	pF
	Input Capacitance ($\overline{BYTE}V_{PP}$)	V_{IN} = 0V		120	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±1	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.4	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	3.5		V
V_{ID}	A9 Voltage		11.5	12.5	V

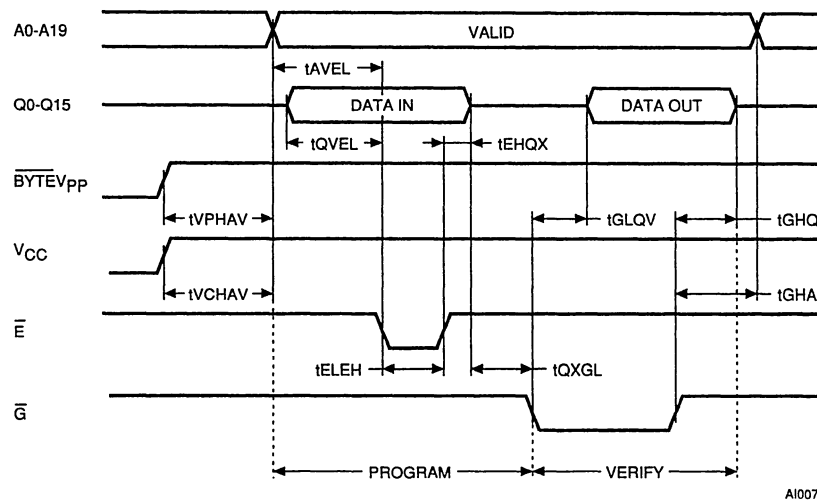
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 9. Programming Mode AC Characteristics (1)
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		2		µs
t_{VPHAV}	t_{VPS}	V_{PP} High to Address Valid		2		µs
t_{VCHAV}	t_{VCS}	V_{CC} High to Address Valid		2		µs
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width		9.5	10.5	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			120	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 8. Programming and Verify Modes AC Waveforms



DEVICE OPERATION

The operating modes of the M27C160 are listed in the Operating Modes Table. A single 5V supply is required in the read mode. All inputs are TTL compatible except for V_{PP} and 12V on A9 for the Electronic Signature.

Read Mode

The M27C160 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the $\overline{BYTE}V_{PP}$ pin. When $\overline{BYTE}V_{PP}$ is at V_{IH} the Word-wide organisation is selected and the Q15A-1 pin is used for Q15 Data Output. When the $\overline{BYTE}V_{PP}$ pin is at V_{IL} the Byte-wide organisation is selected and the Q15A-1 pin is used for the Address Input A-1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A-1 at V_{IL} the lower 8 bits of the 16 bit data are selected and with A-1 at V_{IH} the upper 8 bits of the 16 bit data are selected.

The M27C160 has two control inputs, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte- wide organisation must be selected.

The $\overline{E}$ signal is the power control and should be used for device selection. The $\overline{G}$ signal is the output control and should be used to gate data to the output pins. With $\overline{E}=V_{IL}$ and $\overline{G}=V_{IL}$ the output data will be valid in a time t_{AVQV} after the all address lines are valid and stable.

The Chip Enable to Output Valid time t_{ELQV} is equal to the Address Valid to output Valid time t_{AVQV}. When the Addresses are valid and $\overline{E}=V_{IL}$, the output data is valid after a time of t_{GLQV} from the falling edge of the Output Enable signal.

Standby Mode

The M27C160 has a standby mode which reduces the active current from 50mA (f = 5MHz) to 100µA. The standby mode is entered by applying a CMOS high level V_{CC} –0.2V to $\overline{E}$. When in the standby mode the outputs are in an high impedance state, independant of the $\overline{G}$ input level.

Output Disable Mode

When EPROMs are used in memory arrays two line output control should be used. This function uses the output disable mode which allows:

a. the lowest possible power consumption

b. complete assurance that output bus contention will not occur

For the best use of the two control lines $\overline{E}$ and $\overline{G}$, the input $\overline{E}$ should be decoded and used as the primary selection, while $\overline{G}$ should be made a common connection to all memories in the array. $\overline{G}$ should be connected to the $\overline{READ}$ signal of the system bus. This will ensure that all deselected devices are in the low power standby mode and that the output lines are only active when data is required from a particular memory device.

System Considerations

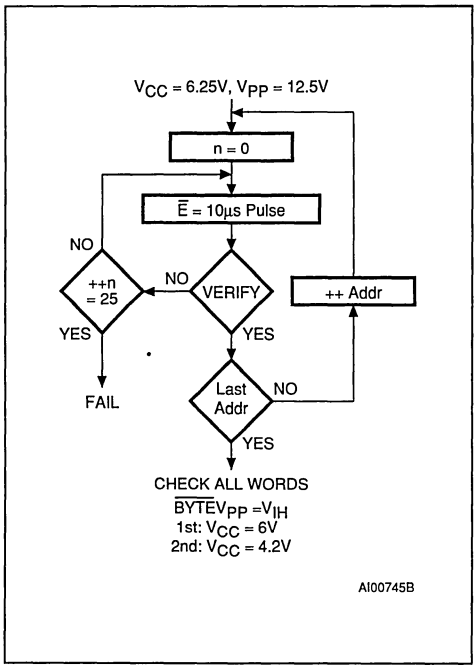
The power switching characteristics of Advanced CMOS EPROMs require carefull decoupliing of the supplies to the devices. The supply current I_{CC} has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of $\overline{E}$.

The magnitude of the transient current peaks is dependant on the capacititive and inductive loading of the device outputs. The associated transient voltage peaks can be supressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor is used on every device between V_{CC} and V_{SS}. This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a 4.7µF electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programing

When first delivered, and after erasure for UV EPROMs, all bits are in the "1" logic state (Output High). Data with both "1's" and "0's" is applied and the "0s'" are programed into the memory array. For programing V_{CC} is raised to 6.25V. The M27C160 is in the Program Mode when V_{PP} is at 12.75V, $\overline{G}$ is at V_{IH} and $\overline{E}$ is pulsed to V_{IL}. Data to be programed is applied 16 bits in parallel to the data output pins Q0-Q15.

Figure 9. Programming Flowchart



PRESTO IV Program Algorithm

The PRESTO IV Algorithm allows the whole 16 Megabit array to be programed with a guaranteed margin in a typical time of 10 seconds. The algorithm applies a series of 10µs program pulses to each word until a correct verify is made. During programing and verify a MARGIN MODE circuit is automatically activated to guarantee that each cell is programed with an adequate margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the neccessary threshold margin for each cell.

Program Inhibit

Multiple M27C160s may be programed in parallel with different data. This is done by putting in parallel all inputs except $\overline{E}$ and $\overline{G}$. With V_{CC} at 6.25V and V_{PP} at 12.5V, data should be applied to all devices and $\overline{G}$ placed at V_{IH}. Low level pulses on the $\overline{E}$ of one device will program that device.

Program Verify

After each program pulse a verify read is made by reading the data output with V_{CC} at 6.25V, V_{PP} at 12.5V and $\overline{G}$ placed at V_{IL}.

Electronic Signature

The Electronic Signature Mode allows a binary code to be read from the EPROM which identifies the Manufacturer and Device Type. These codes are intended to be used to match the programing equipment to the device being programed and its corresponding algorithm.

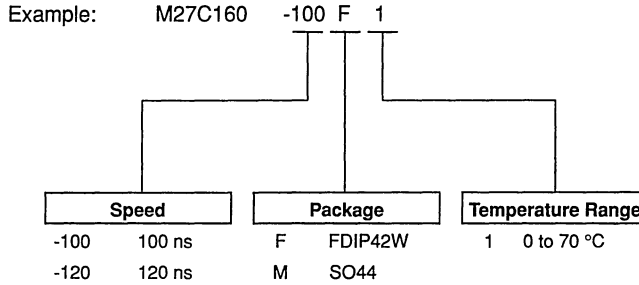
The Electronic Signature Mode is activated by applying a voltage V_{ID} of 12V to the Address line A9 and V_{IL} to all other Address lines, with $\overline{E}$ and $\overline{G}$ at V_{IL} and $\overline{BYTE}$ at V_{IH}. The identifier bytes may be read from either Q0-Q7 or Q8-Q15. With Address line A0 at V_{IL} the byte output is the Manufacture's code, with A0 at V_{IH} the byte identifies the Device Type. The codes for the SGS-THOMSON M27C160 are given in Table 4.

Erasure

The erasure of the M27C160 begins when the cells are exposed to light of wavelengths shorter than approximately 4000 Å. Sunlight and some types of fluorescent lamps have wavelengths in the 3000 - 4000 Å range. Constant exposure to room level fluorescent lighting could erase a typical EPROM in about 3 years, while it takes approximately 170 hours to cause erasure when exposed to direct sunlight. To prevent accidental erasure it is recommended that opaque labels be placed over the M27C160 window.

The erase procedure for the M27C160 is exposure to UV light with a wavelength of 2537 Å. The integrated dose (UV intensity x time) for erasure should be a minimum of 15 W-sec/cm^2. The erase time with this dosage is 15 to 20 minutes using an UV lamp with 12,000 µW/cm^2 rating. The M27C160 should be placed within 2.5cm of the lamp tube during erasure. No filter should be used on the lamp.

ORDERING INFORMATION SCHEME



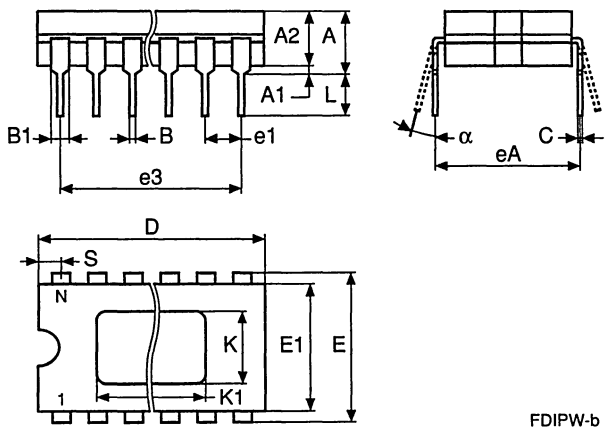
For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

FDIP42W - 42 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.27	1.52		0.050	0.060
C		0.22	0.31		0.009	0.012
D			54.81			2.158
E		15.40	15.80		0.606	0.622
E1		14.50	14.90		0.571	0.587
e1	2.54	–	–	0.100	–	–
e3	50.80	–	–	2.000	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
K	–	–	–	–	–	–
K1	–	–	–	–	–	–
α		4°	15°		4°	15°
N		42			42	

FDIP42W



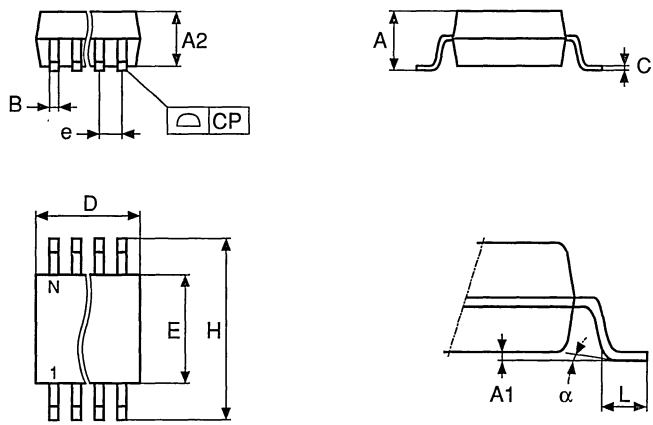
FDIPW-b

Drawing is out of scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27	–	–	0.050	–	–
H		15.90	16.10		0.626	0.634
L	0.80	–	–	0.031	–	–
α	3°	–	–	3°	–	–
N		44			44	
CP			0.10			0.004

SO44



SO-b

Drawing is out of scale

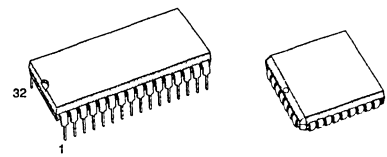
DUAL VOLTAGE FLASH MEMORY

SGS-THOMSON MICROELECTRONICS

M28F256

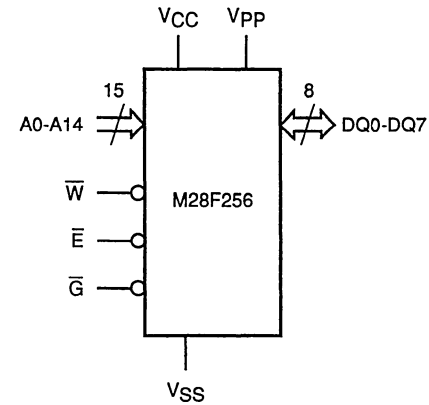
256K (32K x 8, Chip Erase) FLASH MEMORY

- FAST ACCESS TIME: 90ns
- 1,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 100µs (PRESTO F PROGRAMMING)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- EXTENDED TEMPERATURE RANGES
- INTEGRATED PROGRAM/ERASE STOP TIMER



PDIP32 (P) PLCC32 (K)

Figure 1. Logic Diagram



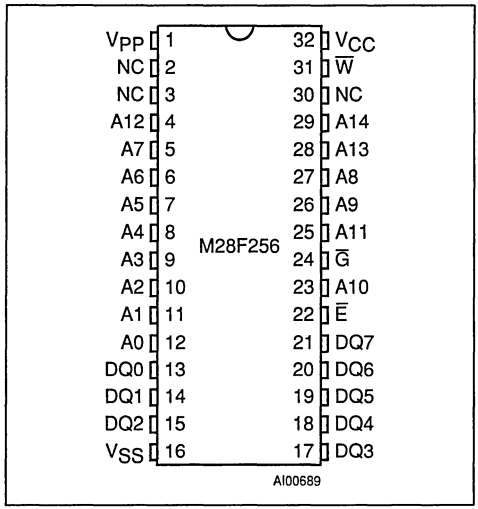
DESCRIPTION

The M28F256 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 32K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F256 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

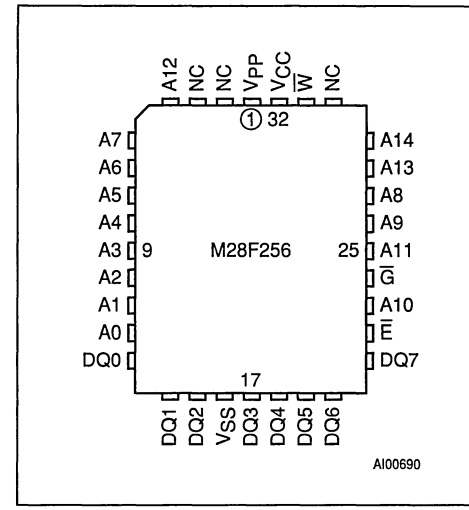
A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F256 FLASH MEMORY employs a technology similar to a 256K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F256 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F256 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 200µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes. The electronic signature may also be accessed in Read/Write modes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

The supply voltage V_{CC} and the program voltage V_{PP} can be applied in any order. When the device is powered up or when V_{PP} is $\leq 6.5V$ the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Notes: 1. X = V_{IL} or V_{IH}

2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	0	1	0	0	0	0A8h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A14	DQ0-DQ7	Operation	A0-A14	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	0000h	20h
					Read	0001h	0A8h
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A14	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A14	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this second cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

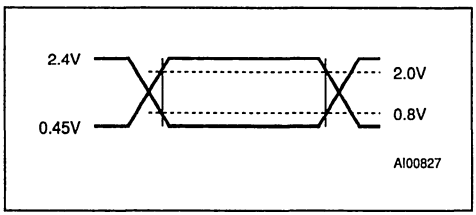


Figure 4. AC Testing Load Circuit

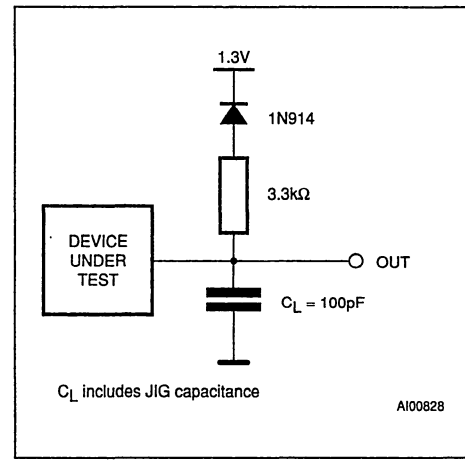


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 5MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		200	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±100	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±100	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High Voltage TTL	IOH = –2.5mA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	4.1		V
		I_{OH} = –1mA	V_{CC} –0.8		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA

Note: 1. Not 100% Tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256						Unit
				-90		-10		-12		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	90		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		100		120	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		100		120	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		50	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	20	0	30	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	20	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
((T_A = 0 to 70 °C, –40 to 85 °C, –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256				Unit
				-15		-20		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		55		60	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

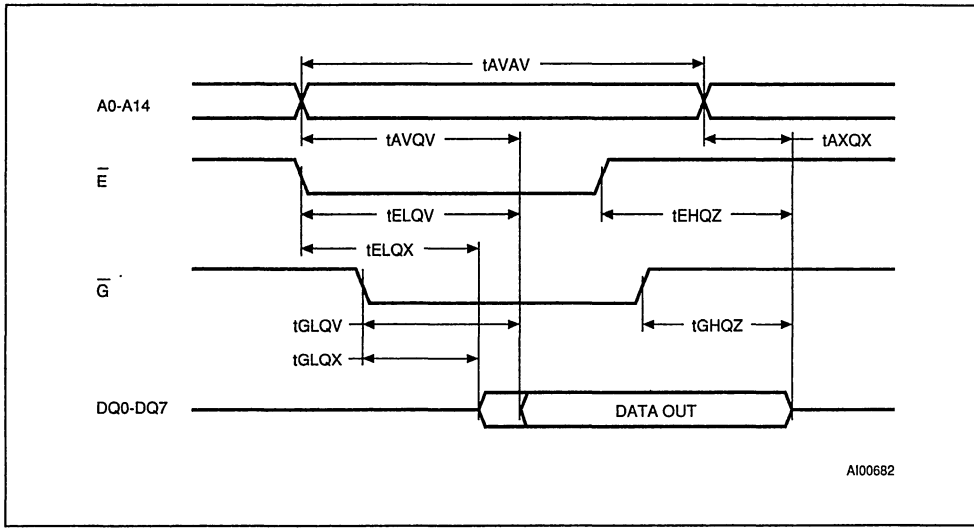


Figure 6. Read Command Waveforms

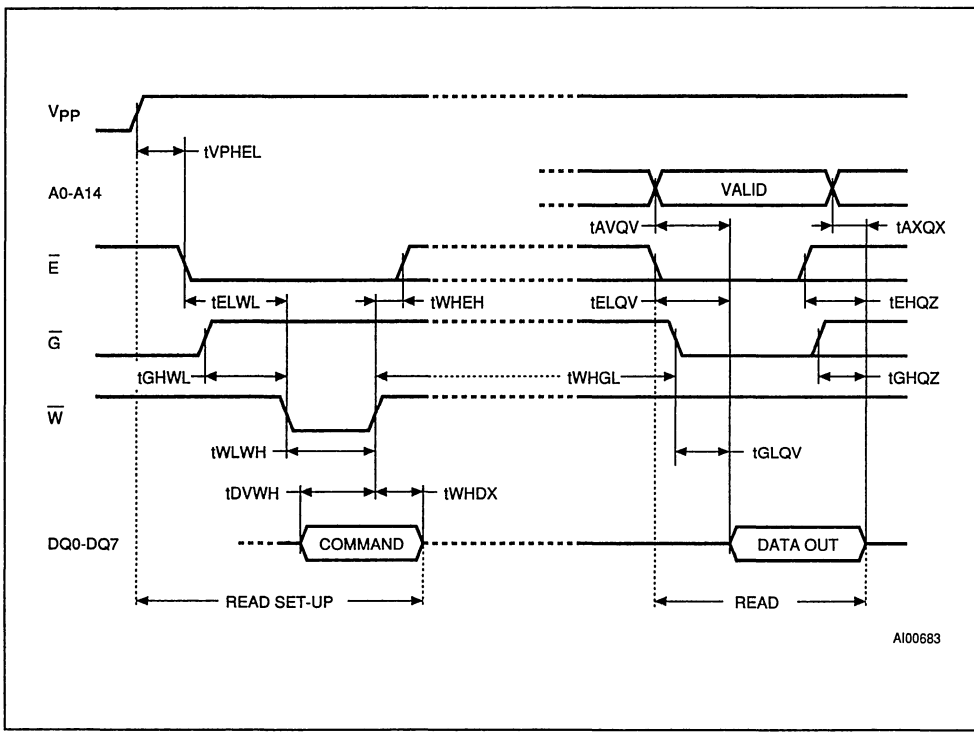


Figure 7. Electronic Signature Command Waveforms

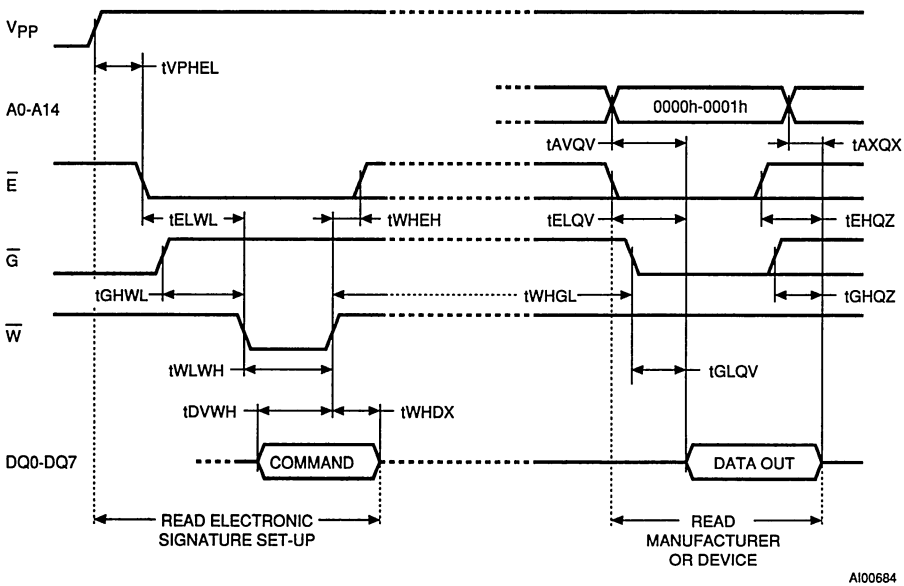


Table 9A. Read/Write Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256						Unit
			-90		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		100		100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	90		100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		50		60		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	15		15		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	45		50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	45		50		60		ns
t_{ELEH} (2)		Chip Enable Low to Chip Enable High (Write Pulse)	45		45		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		10		ns
t_{WHWH1}		Duration of Program Operation	95	105	95	105	95	105	µs
t_{WHWH2}		Duration of Erase Operation	9.5	10.5	9.5	10.5	9.5	10.5	ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		90		100		120	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		90		100		120	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		35		45		50	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		20		30		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z						30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Table 9B. Read/Write Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256				Unit
			-15		-20		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH} (2)		Chip Enable Low to Chip Enable High (Write Pulse)	60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	95	105	95	105	µs
t_{WHWH2}		Duration of Erase Operation	9.5	10.5	9.5	10.5	ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

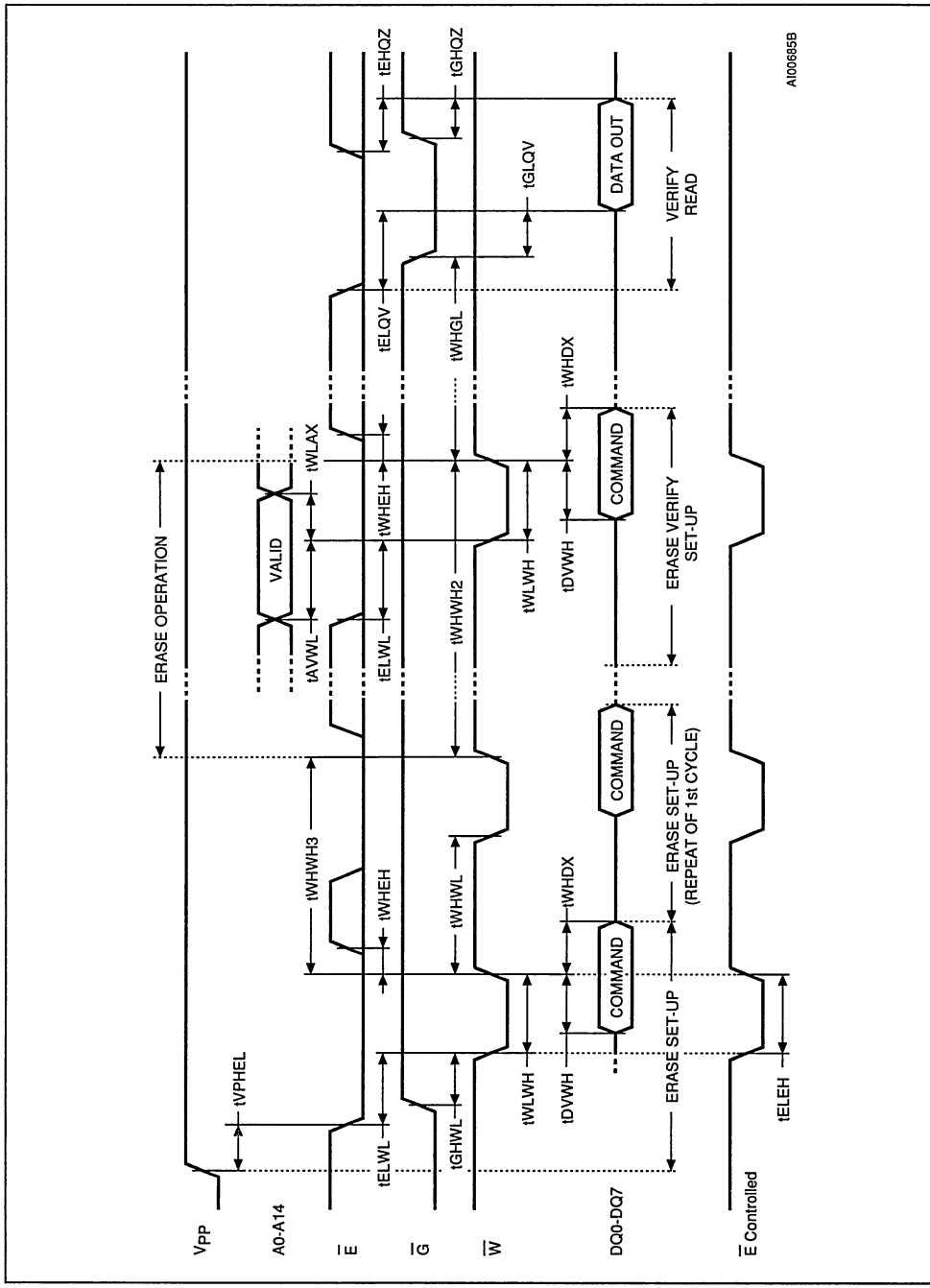


Figure 9. Program Set-up and Program Verify Commands Waveforms

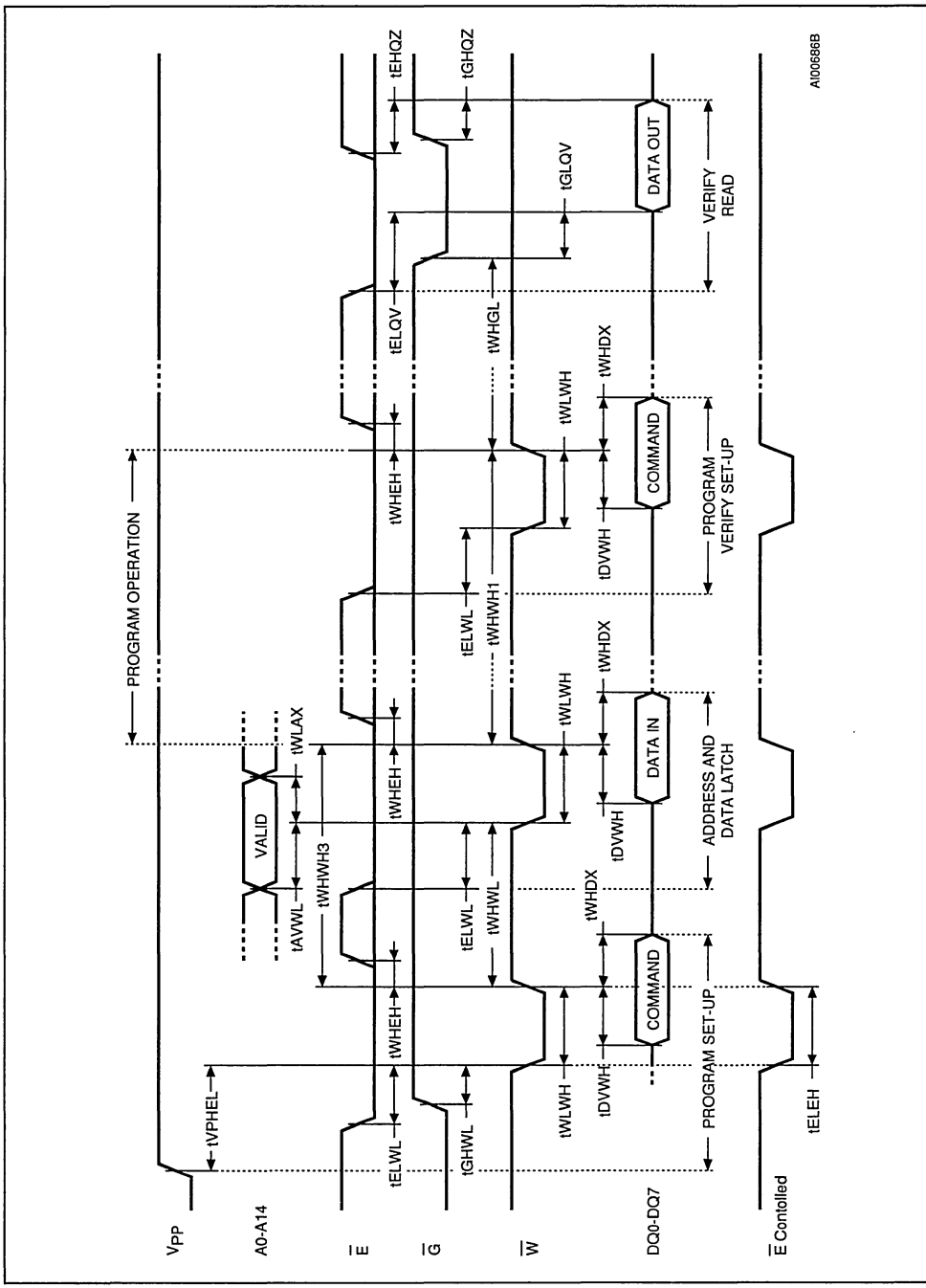


Figure 10. Erasing Flowchart

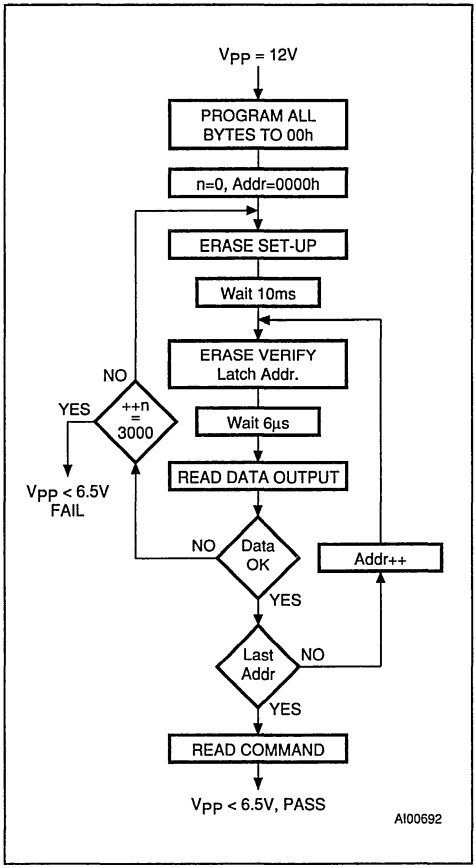
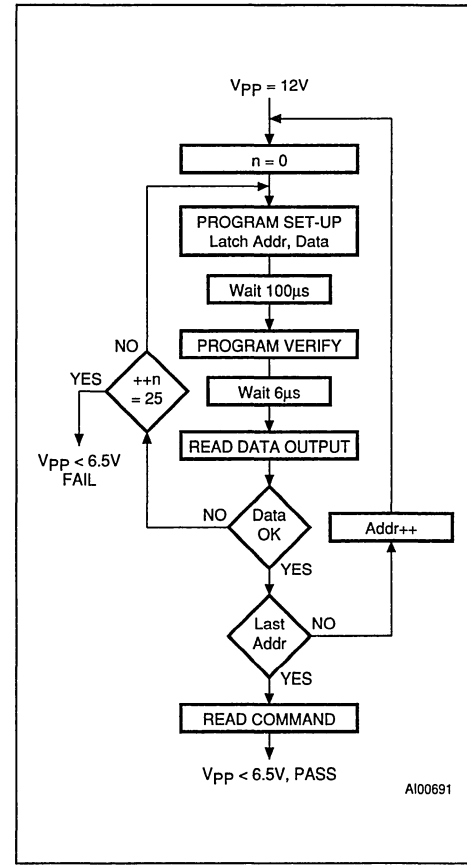


Figure 11. Programming Flowchart



PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programs all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 100µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME

Example: M28F256 -12 X B 1 TR

Speed		V_{CC} Tolerance		Package		Temp. Range		Option	
-90	90 ns	blank	± 10%	B	PDIP32	1	0 to 70 °C	TR	Tape & Reel Packing
-10	100 ns	X	± 5%	C	PLCC32	3	–40 to 125 °C		
-12	120 ns					6	–40 to 85 °C		
-15	150 ns								
-20	200 ns								

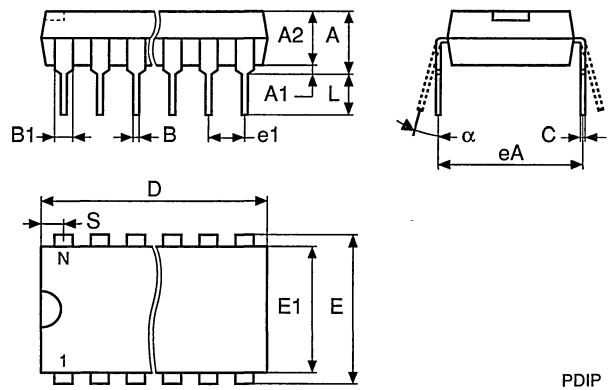
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP32 - 32 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N		32			32	

PDIP32



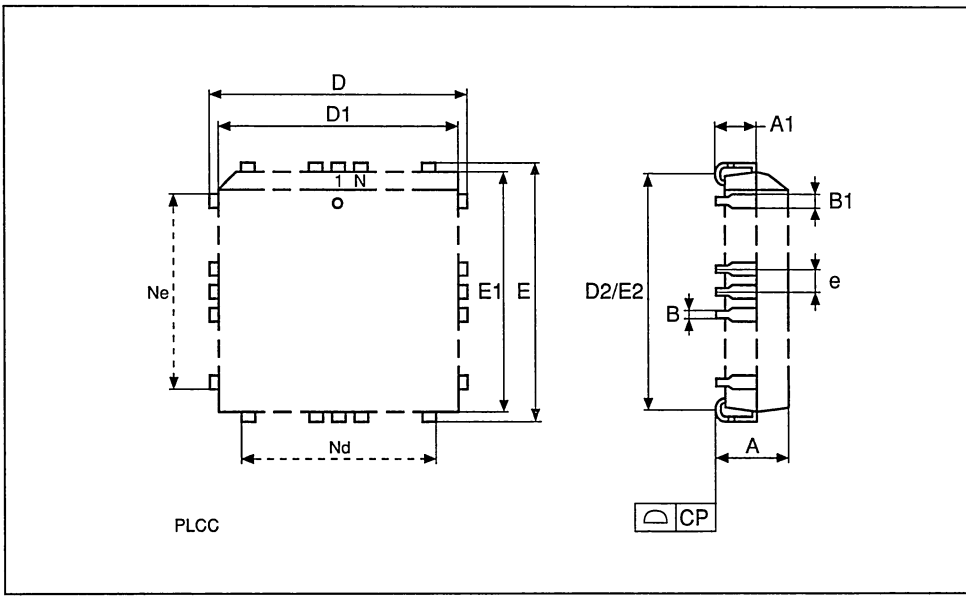
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

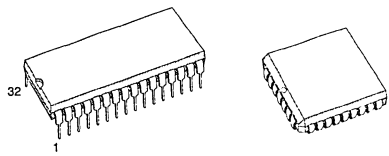
PLCC32



Drawing is out of scale

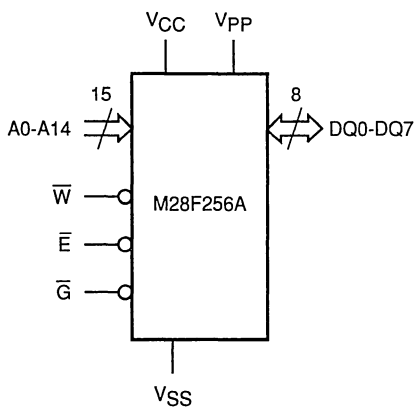
256K (32K x 8, Chip Erase) FLASH MEMORY

- FAST ACCESS TIME: 90ns
- LOW POWER CONSUMPTION
  - Standby Current: 200µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER
- EXTENDED TEMPERATURE RANGES



PDIP32 (B) PLCC32 (C)

Figure 1. Logic Diagram



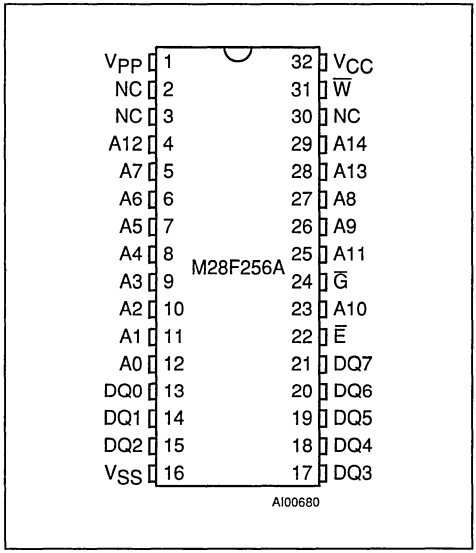
DESCRIPTION

The M28F256A FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 32K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F256A FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

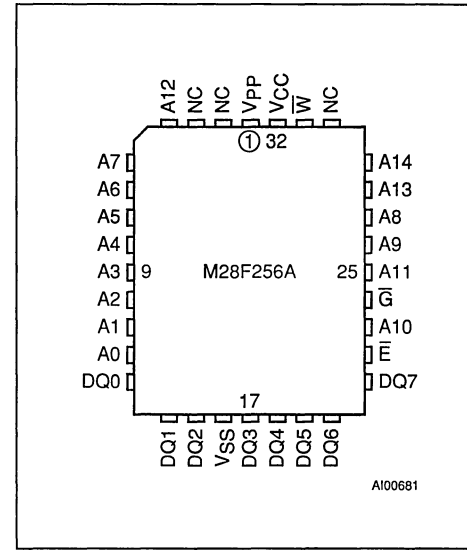
A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F256A FLASH MEMORY employs a technology similar to a 256K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F256A functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is don't care.

Read Mode. The M28F256A has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 200µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes. The electronic signature may also be accessed in Read/Write modes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

The supply voltage V_{CC} and the program voltage V_{PP} can be applied in any order. When the device is powered up or when $V_{PP} \leq 6.5V$ the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory. The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Notes: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	0	1	0	1	0	0AAh

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A14	DQ0-DQ7	Operation	A0-A14	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	0000h	20h
					Read	0001h	0AAh
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A14	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A14	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising

edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

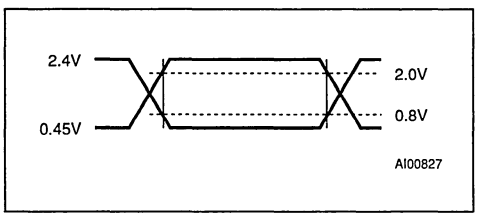


Figure 4. AC Testing Load Circuit

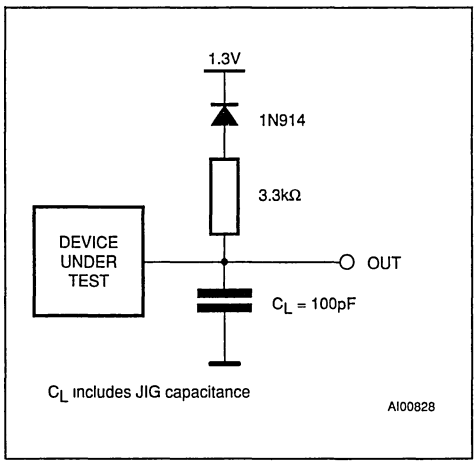


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		200	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±100	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±100	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 6)		0.45	V
V_{OH}	Output High Voltage CMOS	$I_{OH} = -100\mu A$	4.1		V
		I_{OH} = –1mA	V_{CC} –0.8		V
		I_{OH} = –2.5mA (grade 1)	V_{CC} –0.8		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID} (grade 1)		200	µA
		A9 = V_{ID} (grade 6)		500	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% Tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256A						Unit
				-90		-10		-12		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	90		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	20	0	30	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	20	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
((T$_A$ = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F256A				Unit
				-15		-20		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0	=	0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

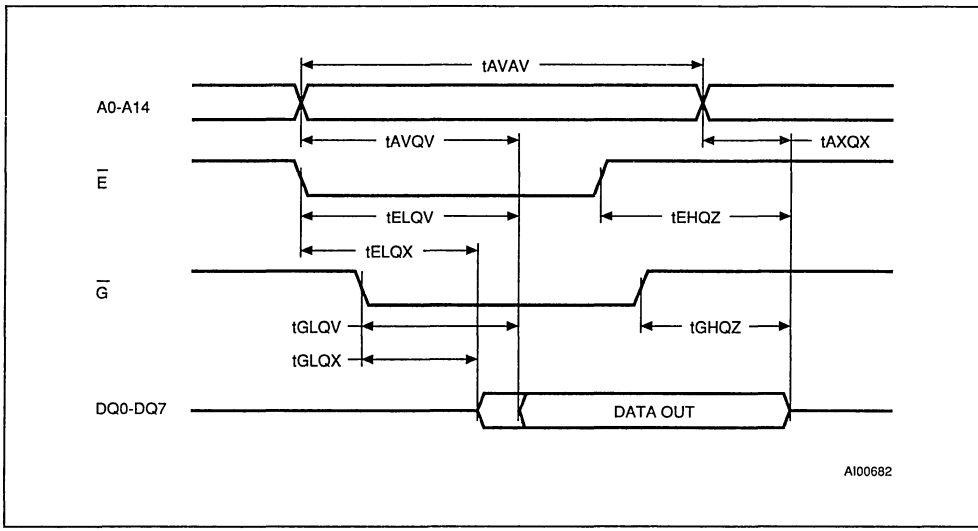


Figure 6. Read Command Waveforms

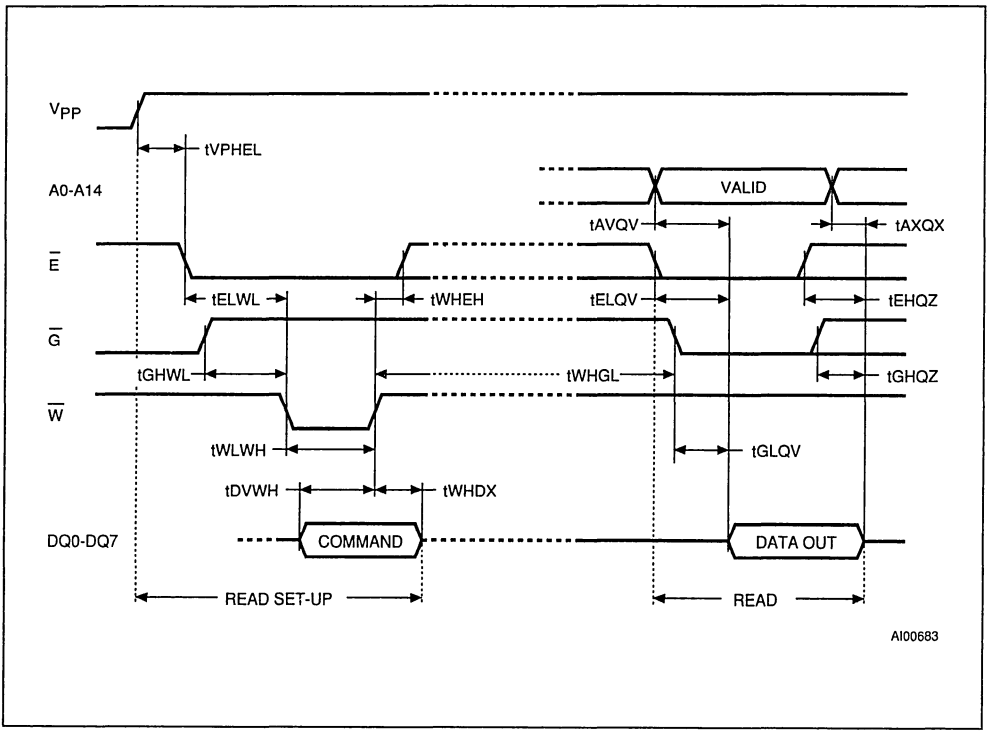


Figure 7. Electronic Signature Command Waveforms

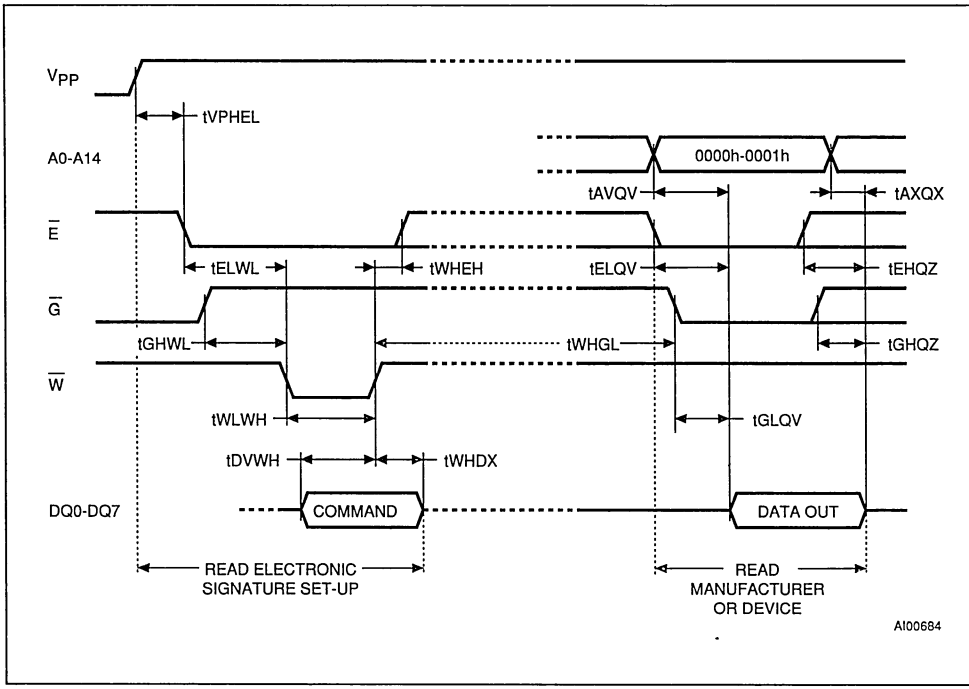


Table 9A. Read/Write Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or V_{CC} = 5V ± 10%: V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256A						Unit
			-90		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		100		100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	90		100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		50		60		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low					20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	45		50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	45		50		60		ns
t_{ELEH} (2)		Chip Enable Low to Chip Enable High (Write Pulse)	45		45		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		10		ns
t_{WHWH1}		Duration of Program Operation	10		10		10		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		90		100		120	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		90		100		120	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		35		45		50	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		20		30		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z						30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Table 9B. Read/Write Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or V_{CC} = 5V ± 10%: V_{PP} = 12V)

Symbol	Alt	Parameter	M28F256A				Unit
			-15		-20		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	100		100		ns
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH} (2)		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	10		10		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX}	t_{CEL}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX}	t_{OEL}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)	t_{CDF}	Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Figure 8. Erase Set-up and Erase Verify Commands Waveforms

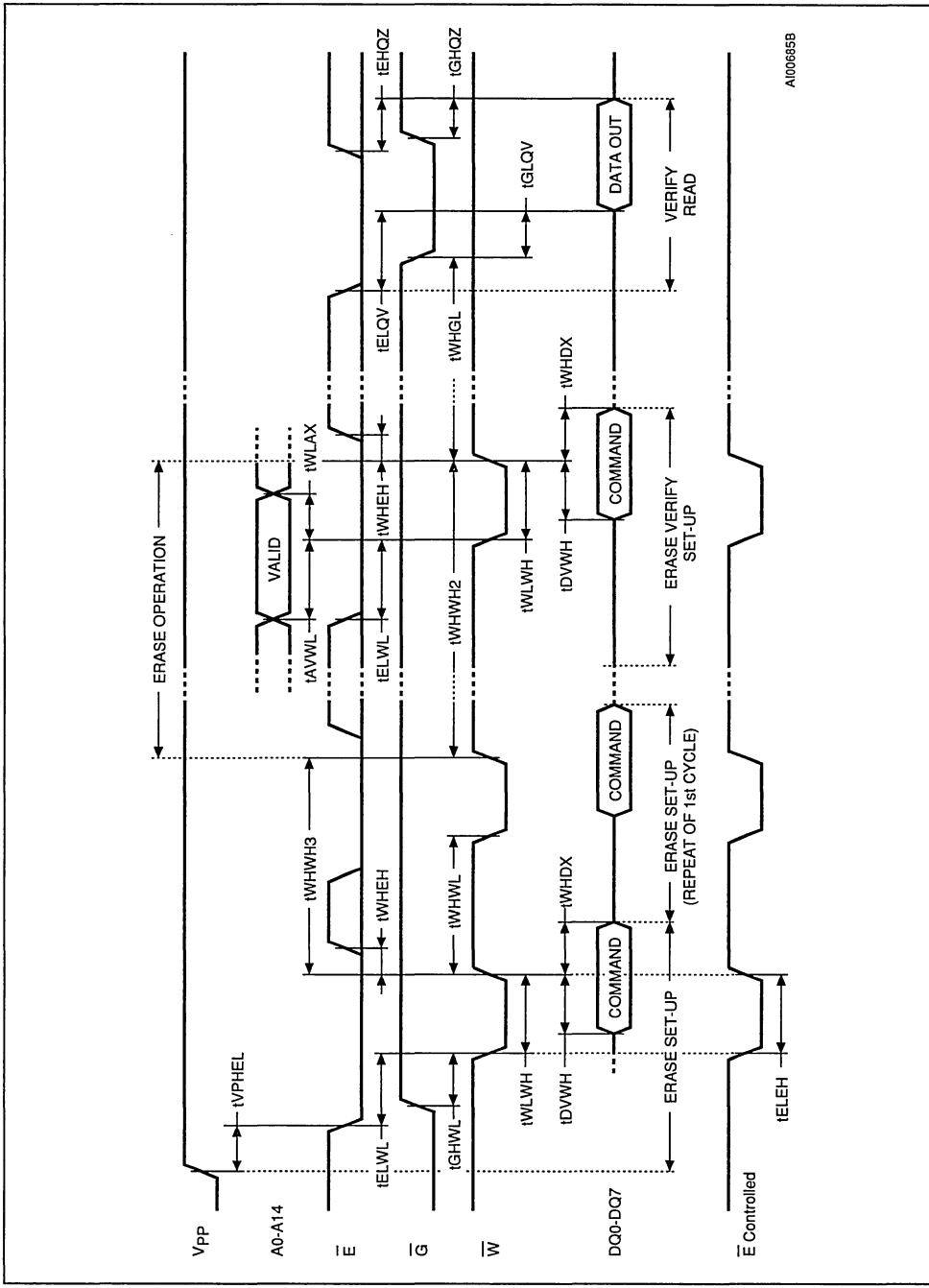


Figure 9. Program Set-up and Program Verify Commands Waveforms

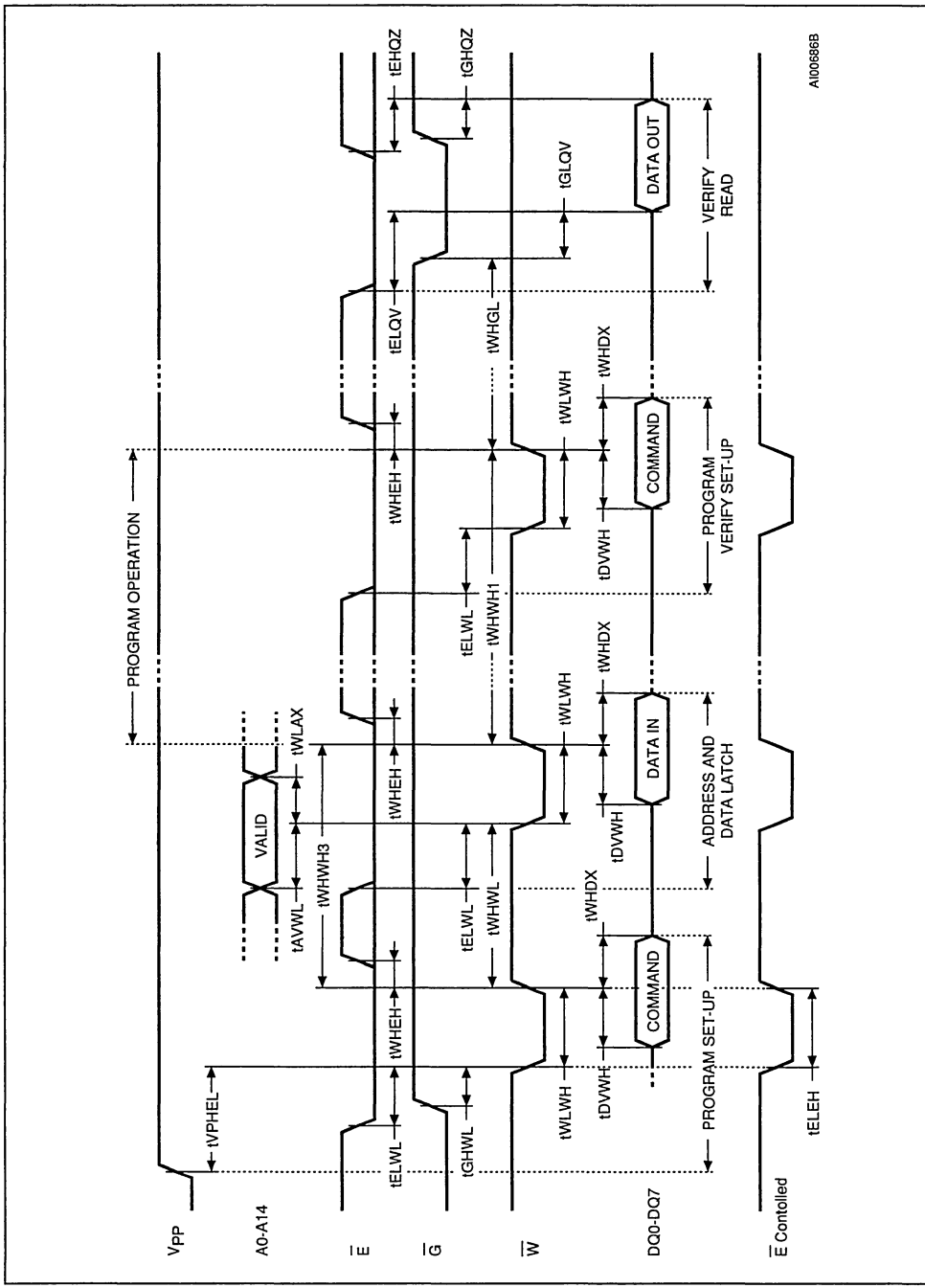


Figure 10. Erasing Flowchart

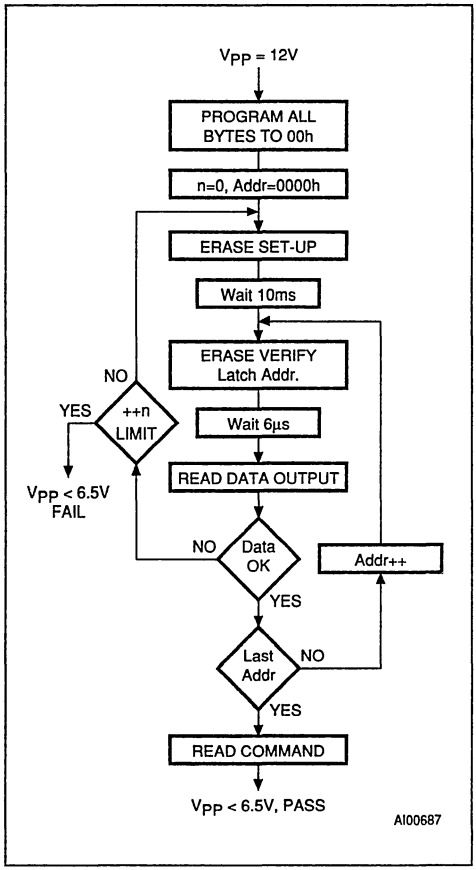
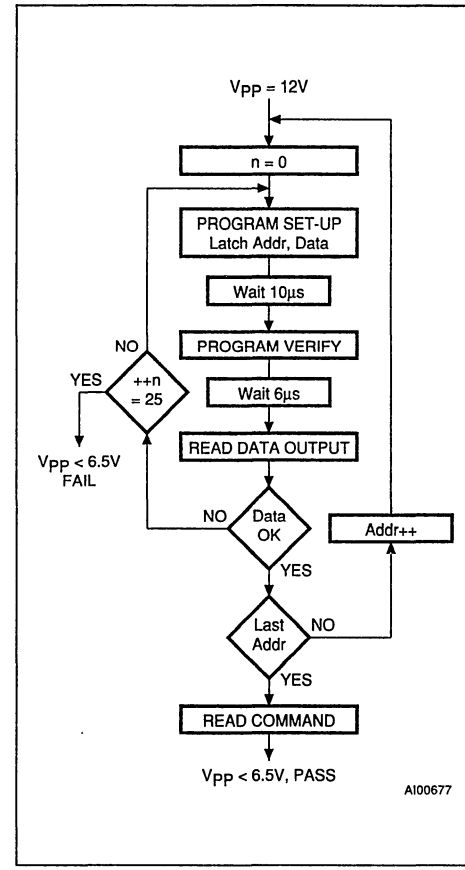


Figure 11. Programming Flowchart



Limit: 1000 at grades 1 & 6; 6000 at grade 3.

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME

Example: M28F256A -12 X B 1 TR

Speed		V_{CC} Tolerance		Package		Temp. Range		Option	
-90	90 ns	blank	± 10%	B	PDIP32	1	0 to 70 °C	Y3	1,000 Cycles
-10	100 ns	X	± 5%	C	PLCC32	3	–40 to 125 °C	TR	Tape & Reel Packing
-12	120 ns					6	–40 to 85 °C		
-15	150 ns								
-20	200 ns								

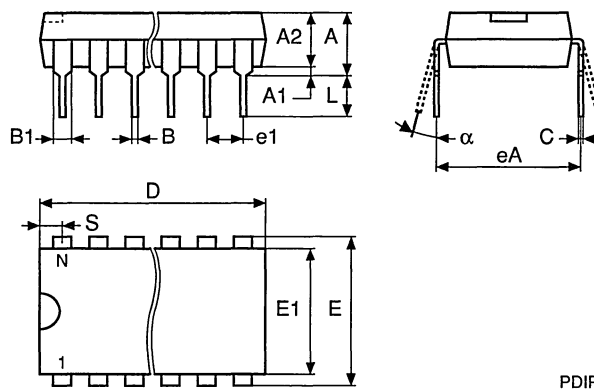
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP32 - 32 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N		32			32	

PDIP32



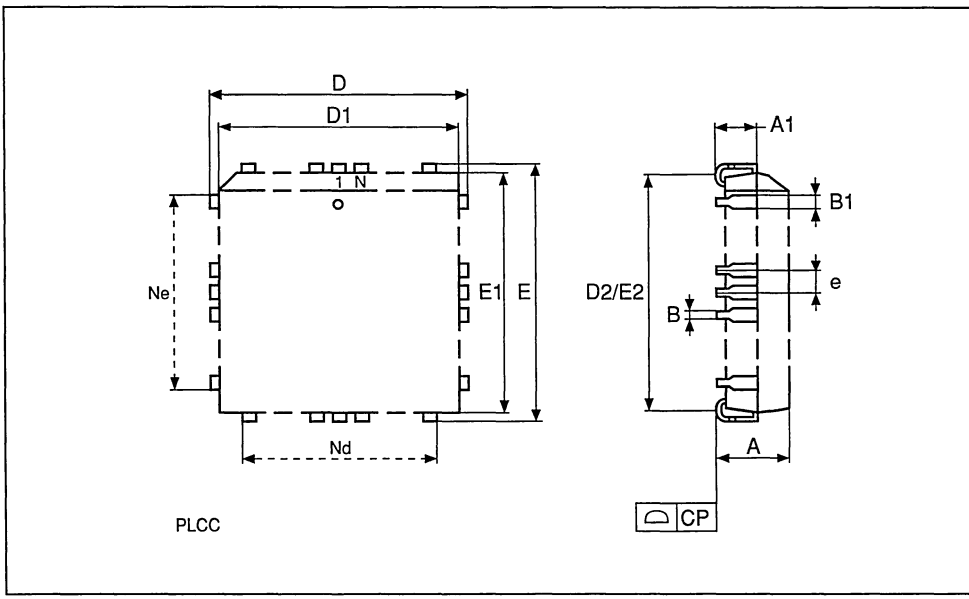
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

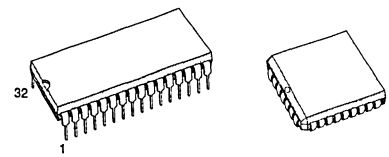


PLCC

Drawing is out of scale

512K (64K x 8, Chip Erase) FLASH MEMORY

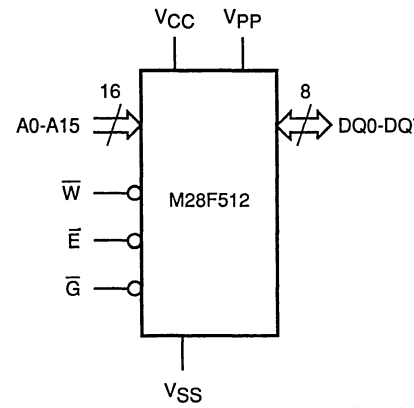
- FAST ACCESS TIME: 90ns
- LOW POWER CONSUMPTION
  - Standby Current: 200µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER
- EXTENDED TEMPERATURE RANGES



PDIP32 (B)

PLCC32 (C)

Figure 1. Logic Diagram



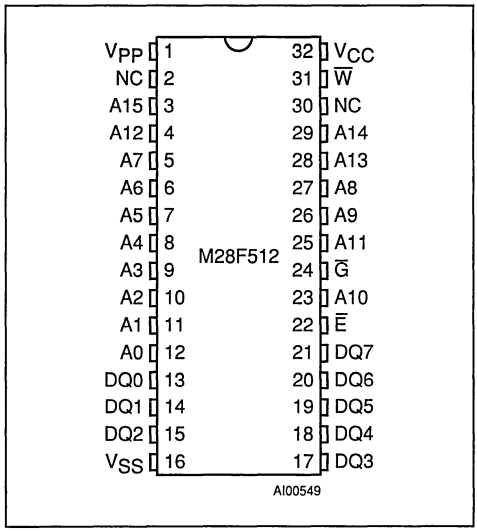
DESCRIPTION

The M28F512 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 64K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F512 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

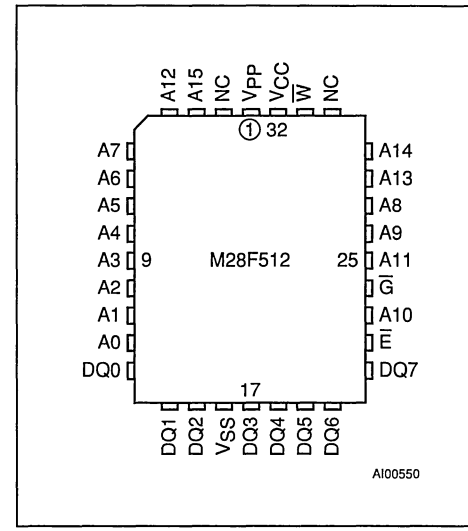
A0 - A15	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F512 FLASH MEMORY employs a technology similar to a 512K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F512 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F512 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 200µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allcws the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes. The electronic signature may also be accessed in Read/Write modes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

The supply voltage V_{CC} and program voltage V_{PP} can be applied in any order. When the device is powered up or when V_{PP} is $\leq 6.5V$ the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Notes: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	0	1	0	02h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A15	DQ0-DQ7	Operation	A0-A15	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	0000h	20h
					Read	0001h	02h
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A15	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A15	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is

followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

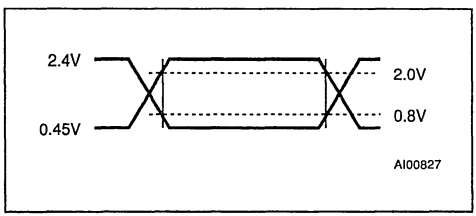


Figure 4. AC Testing Load Circuit

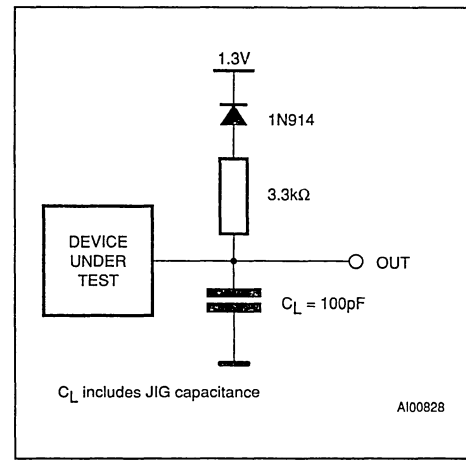


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		200	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±100	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±100	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 6)		0.45	V
V_{OH}	Output High Voltage CMOS	$I_{OH} = -100\mu A$	4.1		V
		I_{OH} = –1mA	V_{CC} –0.8		V
		I_{OH} = –2.5mA (grade 1)	V_{CC} –0.8		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	$A9 = V_{ID}$		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F512						Unit
				-90		-10		-12		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	90		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		40		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	20	0	30	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	20	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
((T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F512				Unit
				-15		-20		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0	=	0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

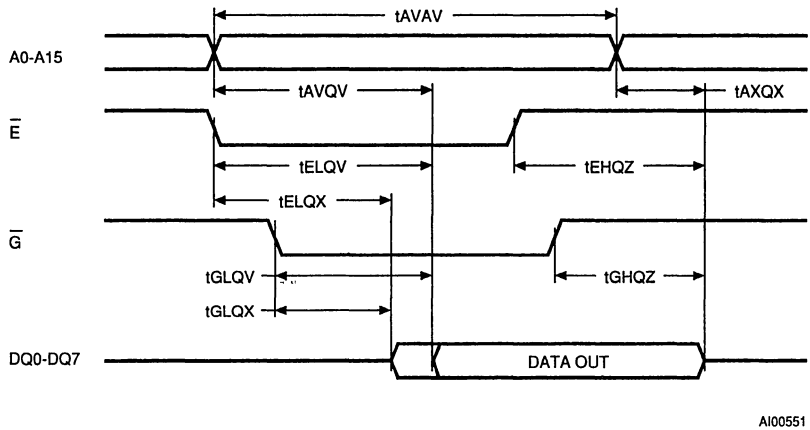


Figure 6. Read Command Waveforms

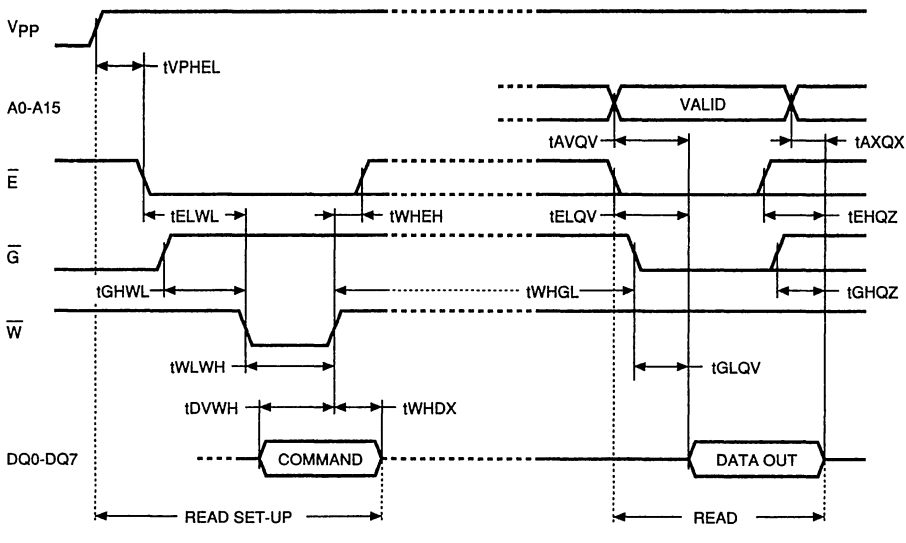


Figure 7. Electronic Signature Command Waveforms

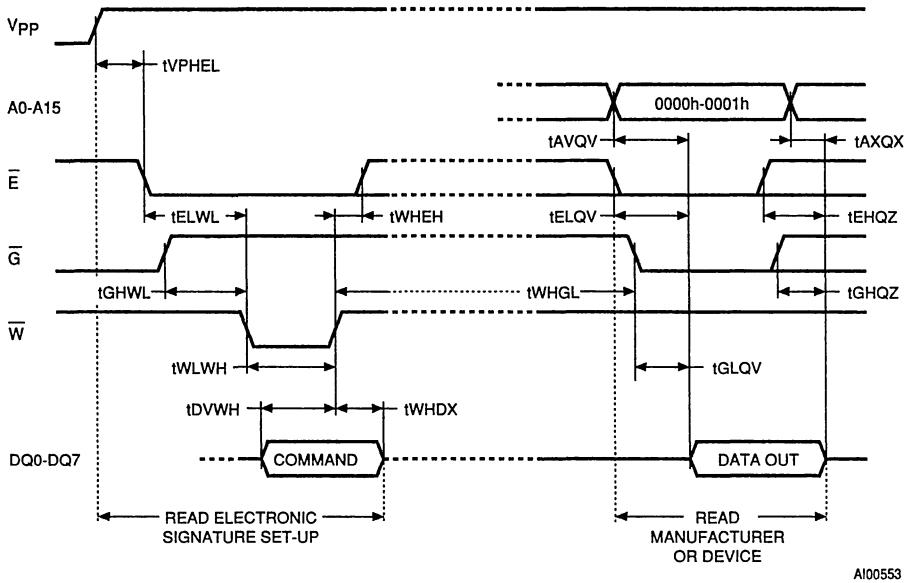


Table 9A. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled

(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F512						Unit
			-90		-10		-12		
			Min	Max	Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	90		100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		50		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	50		60		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	15		15		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	45		50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	35		40		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	45		50		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	45		45		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		90		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		90		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		35		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		20		30		50	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		20		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested

2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Table 9B. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F512				Unit
			-15		-20		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Notes: 1. Sampled only, not 100% tested
2. A Write is enabled by a valid combination of Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When Write is controlled by Chip Enable (with a Chip Enable pulse width smaller than Write Enable), all timings should be measured relative to Chip Enable waveform.

Figure 8. Erase Set-up and Erase Verify Commands Waveforms, $\overline{W}$ Controlled

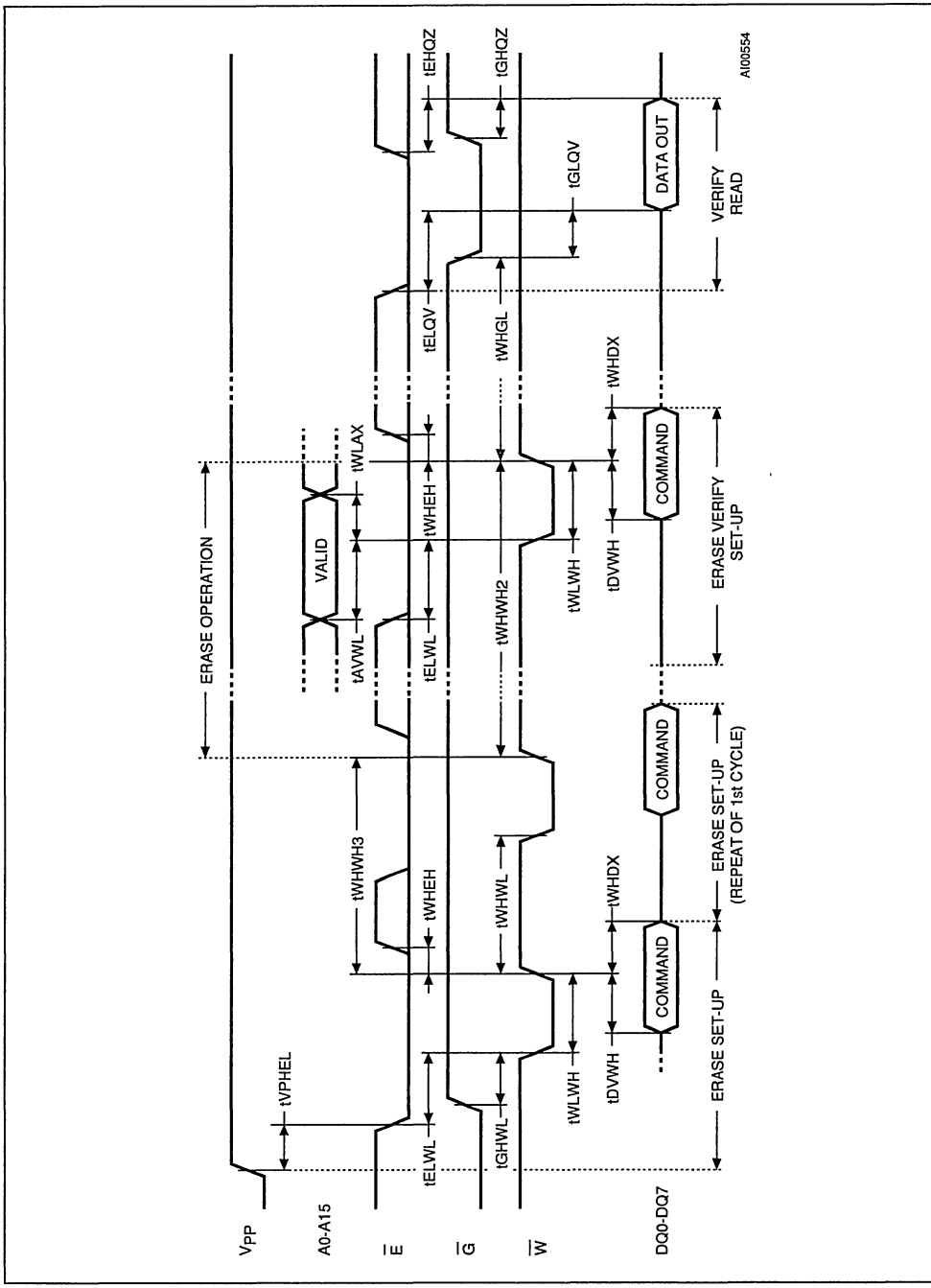


Figure 9. Erase Set-up and Erase Verify Commands Waveforms, $\overline{E}$ Controlled

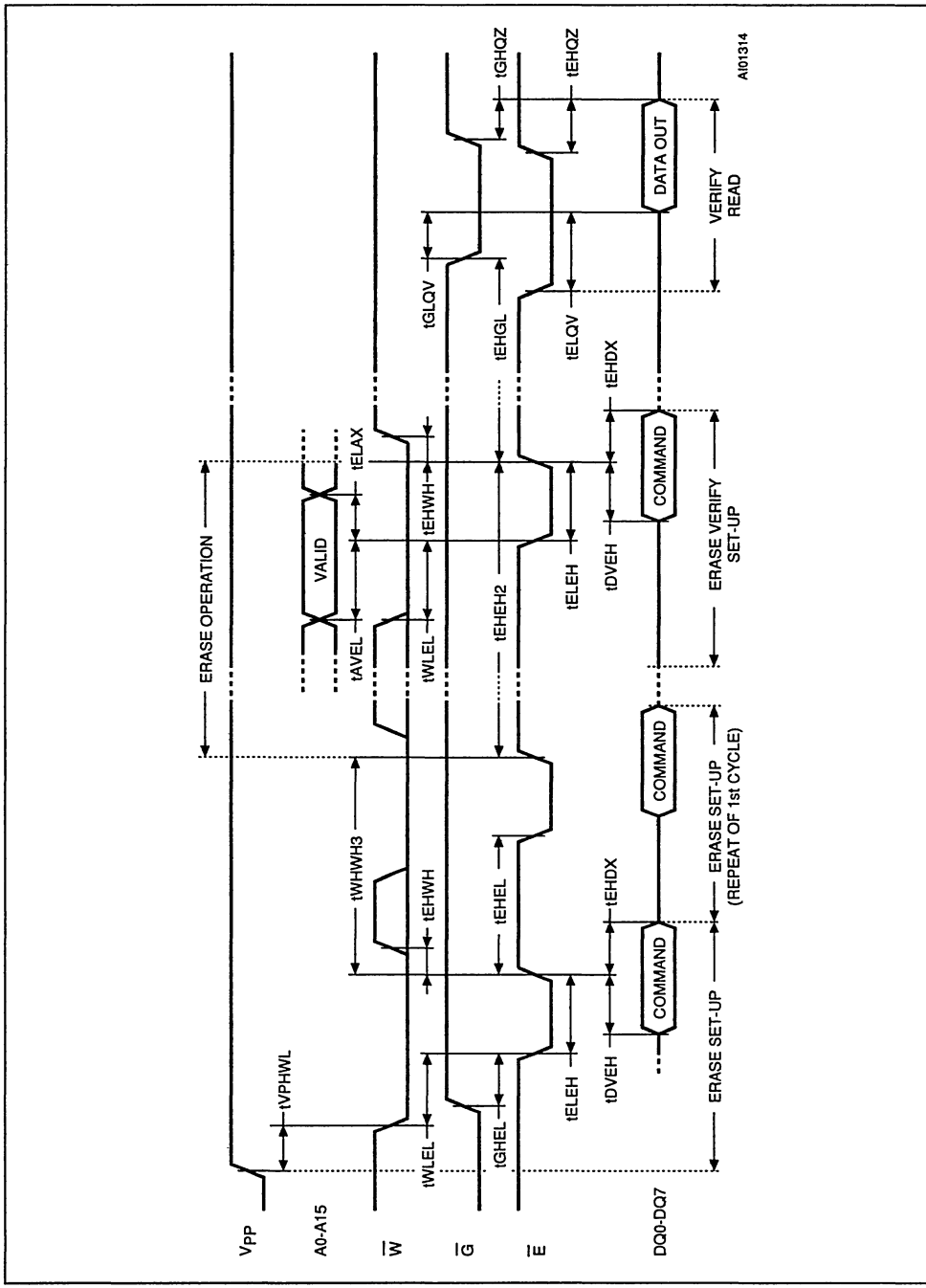


Figure 10. Program Set-up and Program Verify Commands Waveforms, $\overline{W}$ Controlled

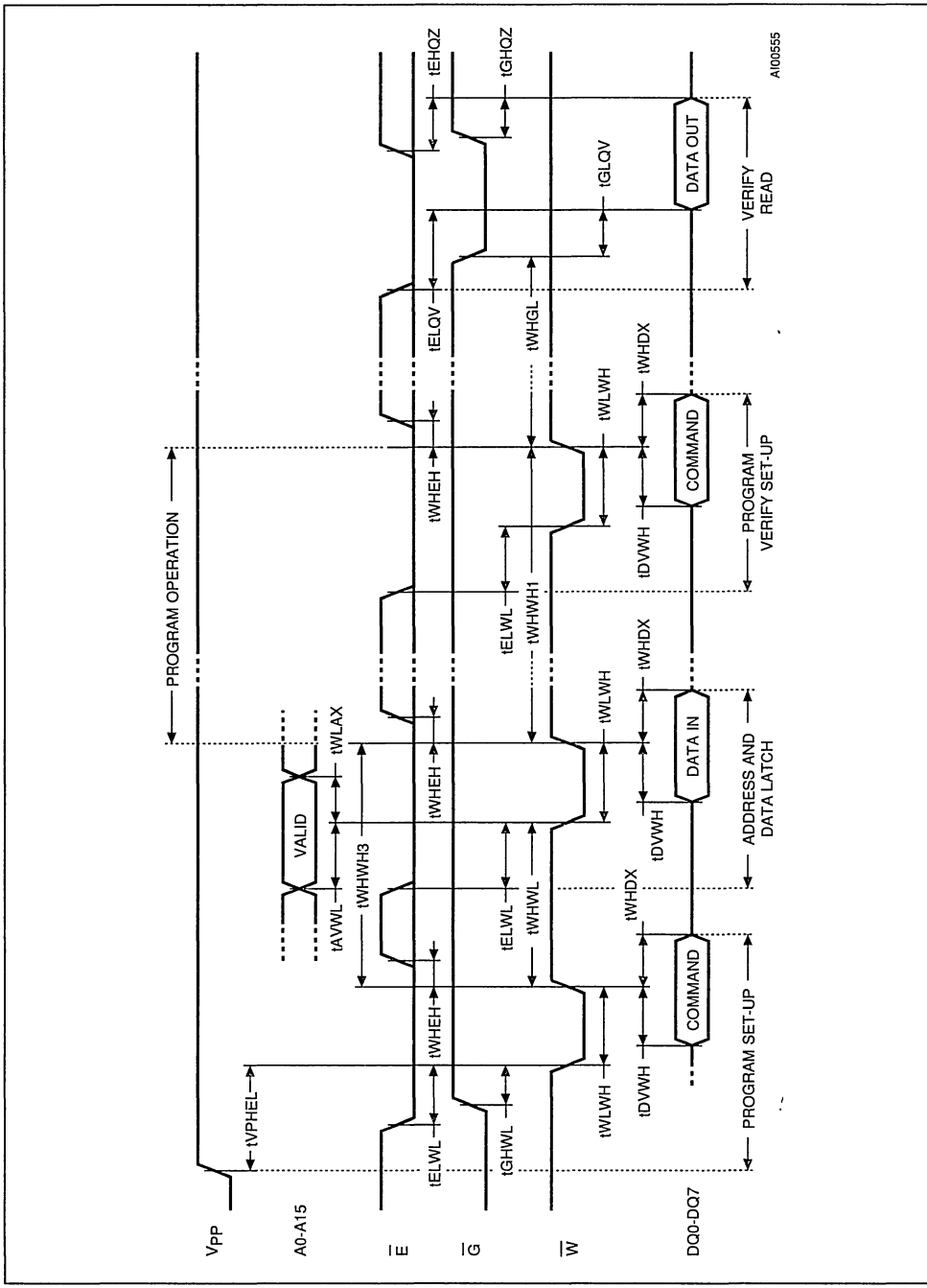


Figure 11. Program Set-up and Program Verify Commands Waveforms, $\overline{E}$ Controlled

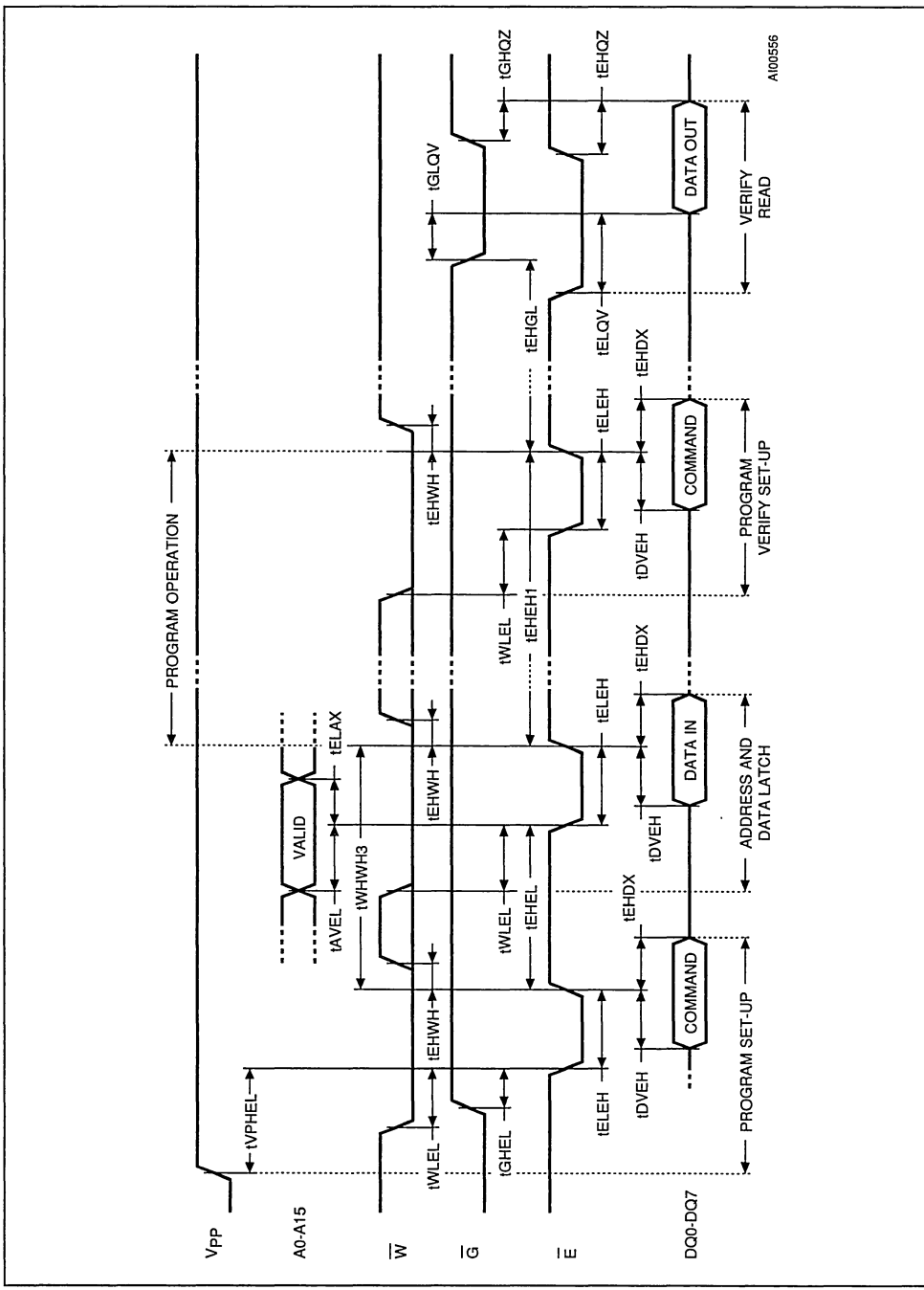
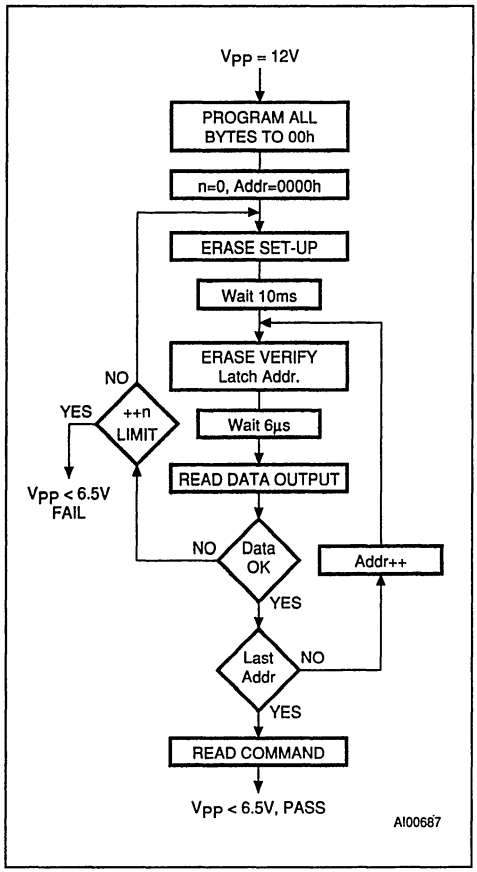
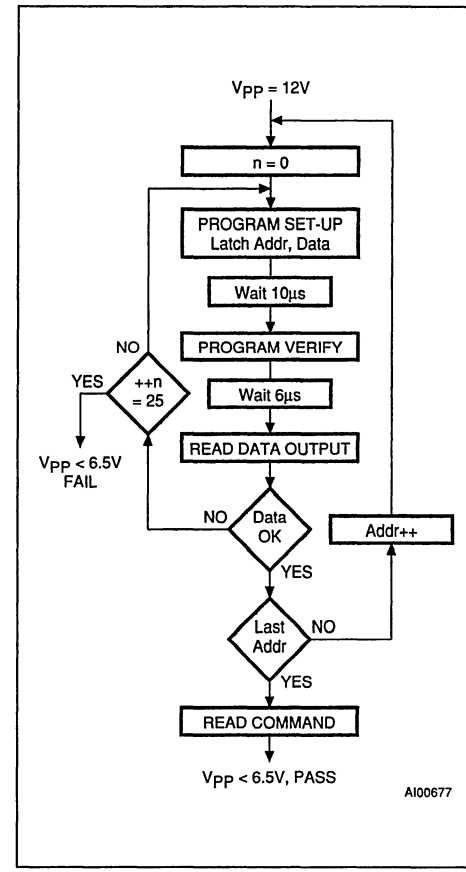


Figure 12. Erasing Flowchart



Limit: 1000 at grades 1 & 6; 6000 at grade 3.

Figure 13. Programming Flowchart



PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME

Example: M28F512 -12 X C 1 TR

Speed		V_{CC} Tolerance		Package		Temp. Range		Option	
-90	90 ns	blank	± 10%	B	PDIP32	1	0 to 70 °C	Y3	1,000 Cycles
-10	100 ns	X	± 5%	C	PLCC32	3	–40 to 125 °C	TR	Tape & Reel Packing
-12	120 ns					6	–40 to 85 °C		
-15	150 ns								
-20	200 ns								

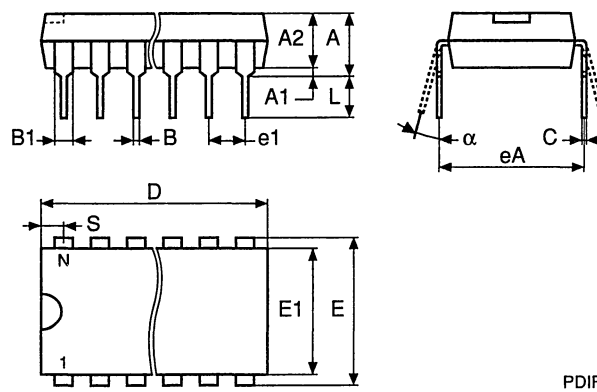
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP32 - 32 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N	32			32		

PDIP32



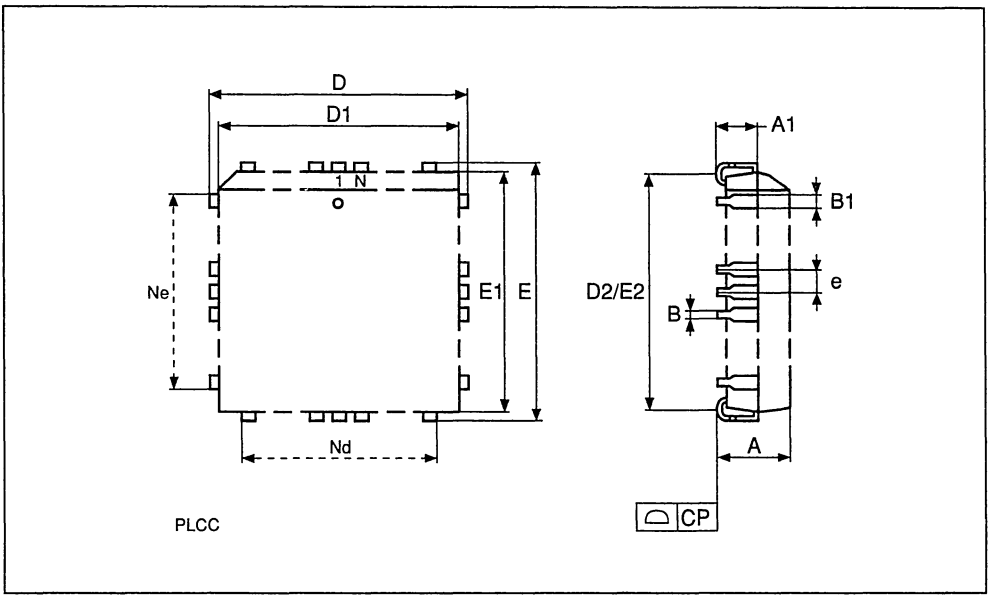
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

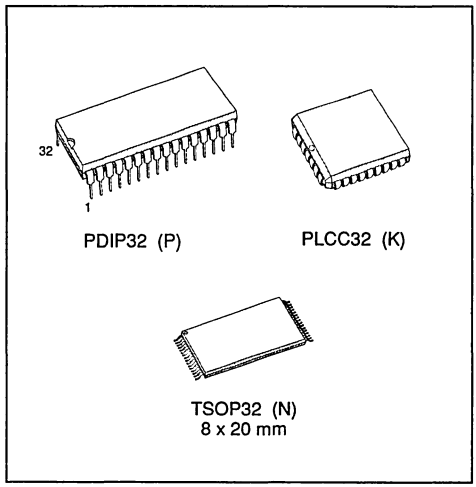
PLCC32



Drawing is out of scale

1 Megabit (128K x 8, Chip Erase) FLASH MEMORY

- FAST ACCESS TIME: 90ns
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER
- OTP COMPATIBLE PACKAGES and PINOUTS
- EXTENDED TEMPERATURE RANGES



DESCRIPTION

The M28F101 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 128K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F101 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

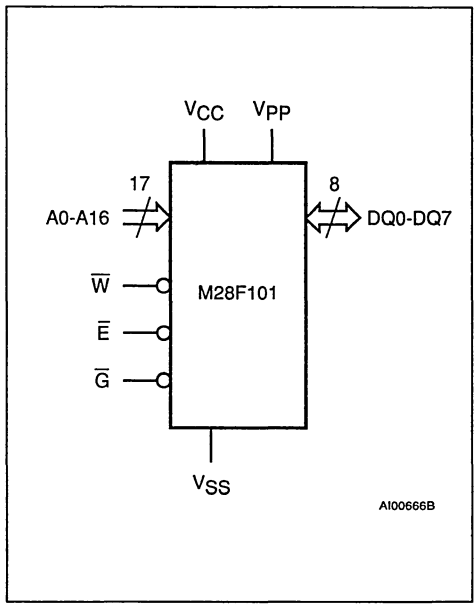
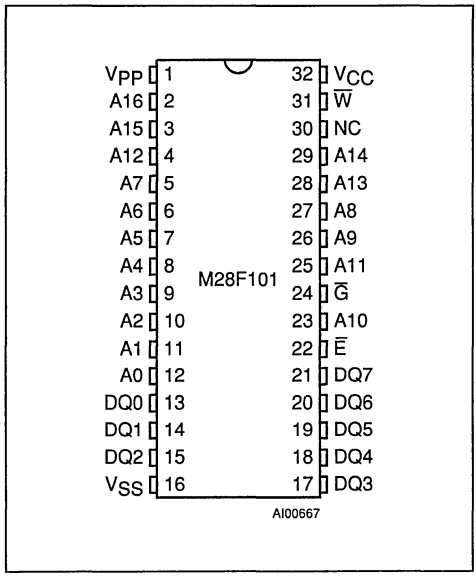
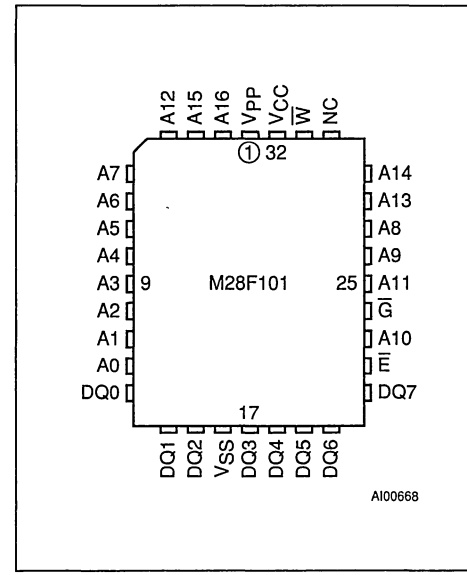


Figure 2A. DIP Pin Connections



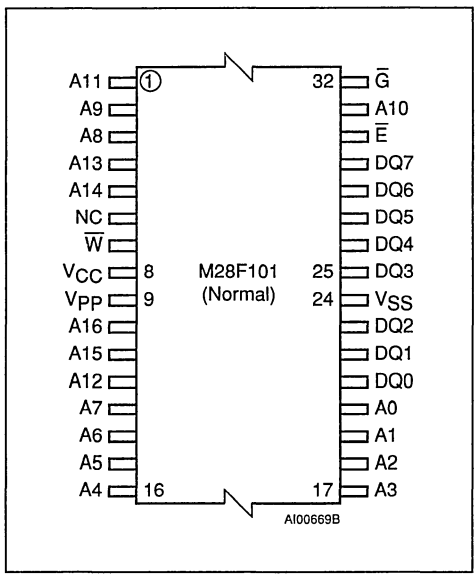
Warning: NC = No Connection

Figure 2B. LCC Pin Connections



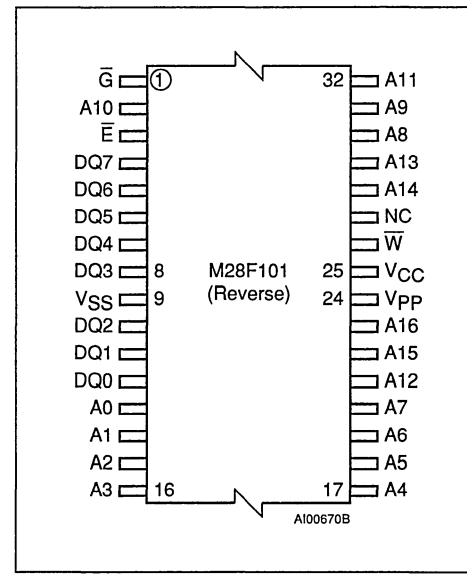
Warning: NC = No Connection

Figure 2C. TSOP Pin Connections



Warning: NC = No Connection

Figure 2D. TSOP Reverse Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F101 FLASH MEMORY employs a technology similar to a 1 Megabit EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F101 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command regsiter is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is don't care.

Read Mode. The M28F101 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 100µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes. The electronic signature may also be accessed in Read/Write modes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Notes: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	0	0	0	1	1	1	07h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A16	DQ0-DQ7	Operation	A0-A16	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature	2	Write	X	90h	Read	00000h	20h
					Read	00001h	07h
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A16	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A16	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}

READ/WRITE MODES (cont'd)

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

The supply voltage V_{CC} and the program voltage V_{PP} can be applied in any order. When the device is powered up or when V_{PP} is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 90h to the command register. The following read cycle, with address inputs 00000h or 00001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

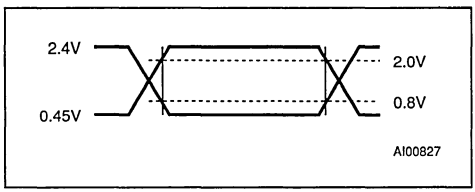


Figure 4. AC Testing Load Circuit

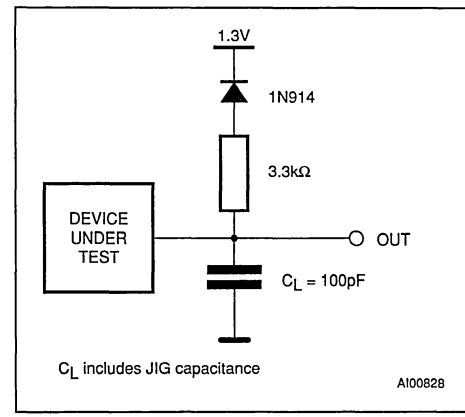


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 6MHz		30	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		15	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		15	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±10	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 6)		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	4.1		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	$A9 = V_{ID}$		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: 1. Not 100% tested. Characterisation Data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F101						Unit
				-90		-100		-120		
				Min	Max	Min	Max	Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	90		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	45	0	45	0	55	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
(((T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F101				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

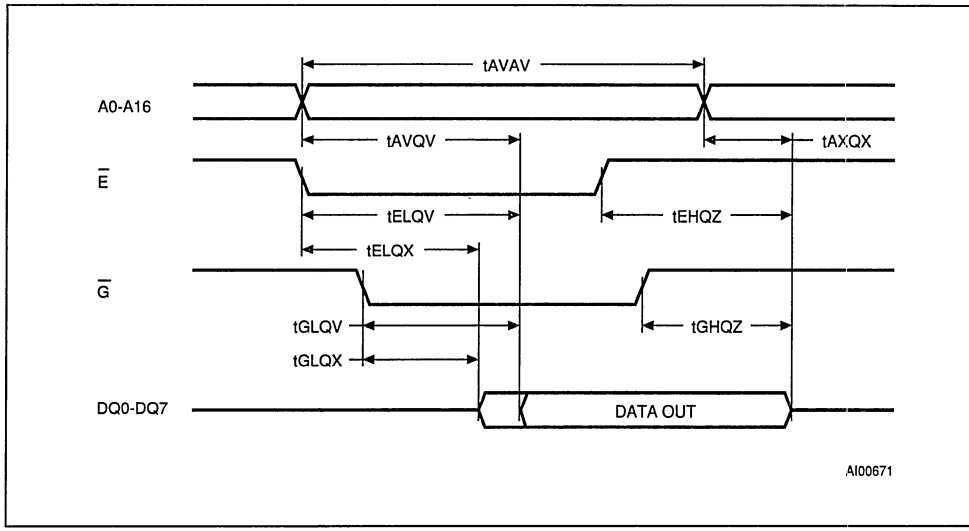


Figure 6. Read Command Waveforms

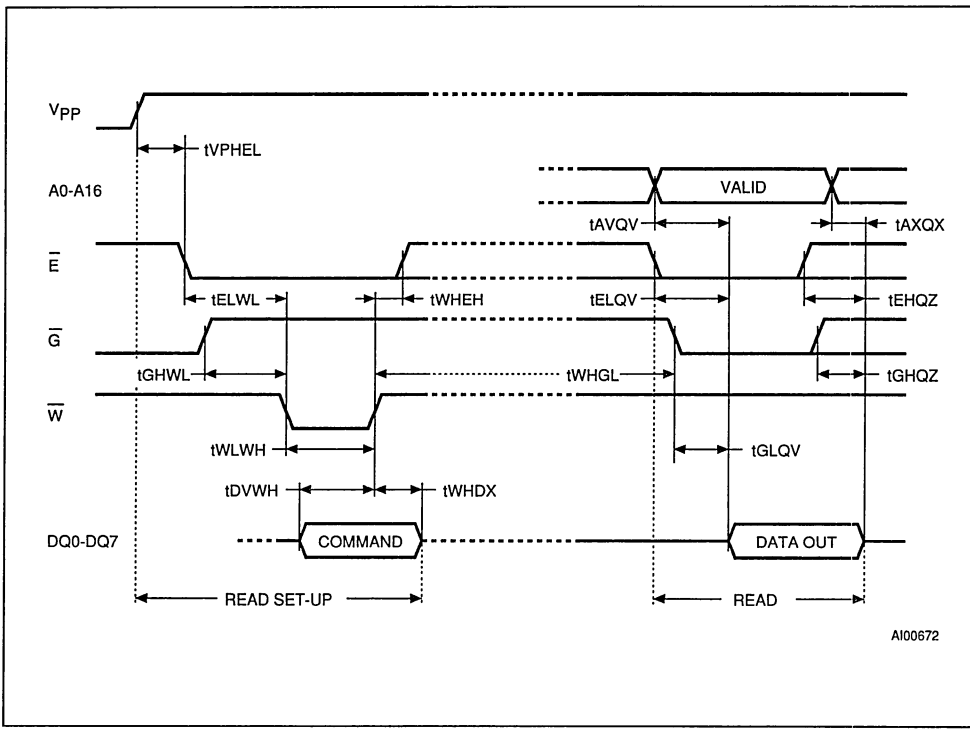
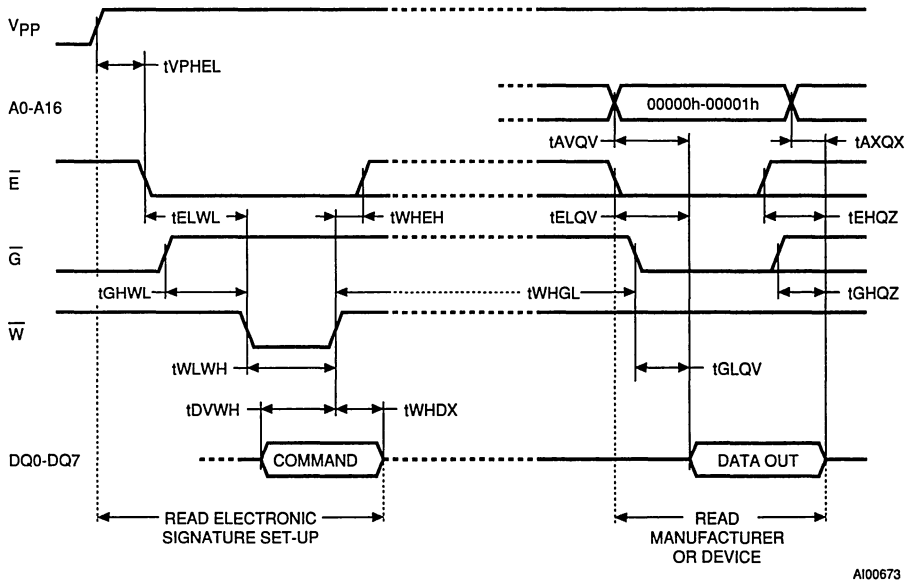


Figure 7. Electronic Signature Command Waveforms



READ/WRITE MODES (cont'd)

memory byte-by-byte for a content of 0FFh. The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

Table 9A. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F101						Unit
			-90		-100		-120		
			Min	Max	Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	90		100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	40		40		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	60		60		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	15		15		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	40		40		50		ns
t_{DVEH}		Input Valid to Chip Enable High	35		40		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	40		40		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	45		45		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		90		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		90		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		35		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		40		40		50	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Table 9B. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 5% or 5V ± 10%)

Symbol	Alt	Parameter	M28F101				Unit
			-150		-200		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time	150		200		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms, $\overline{W}$ Controlled

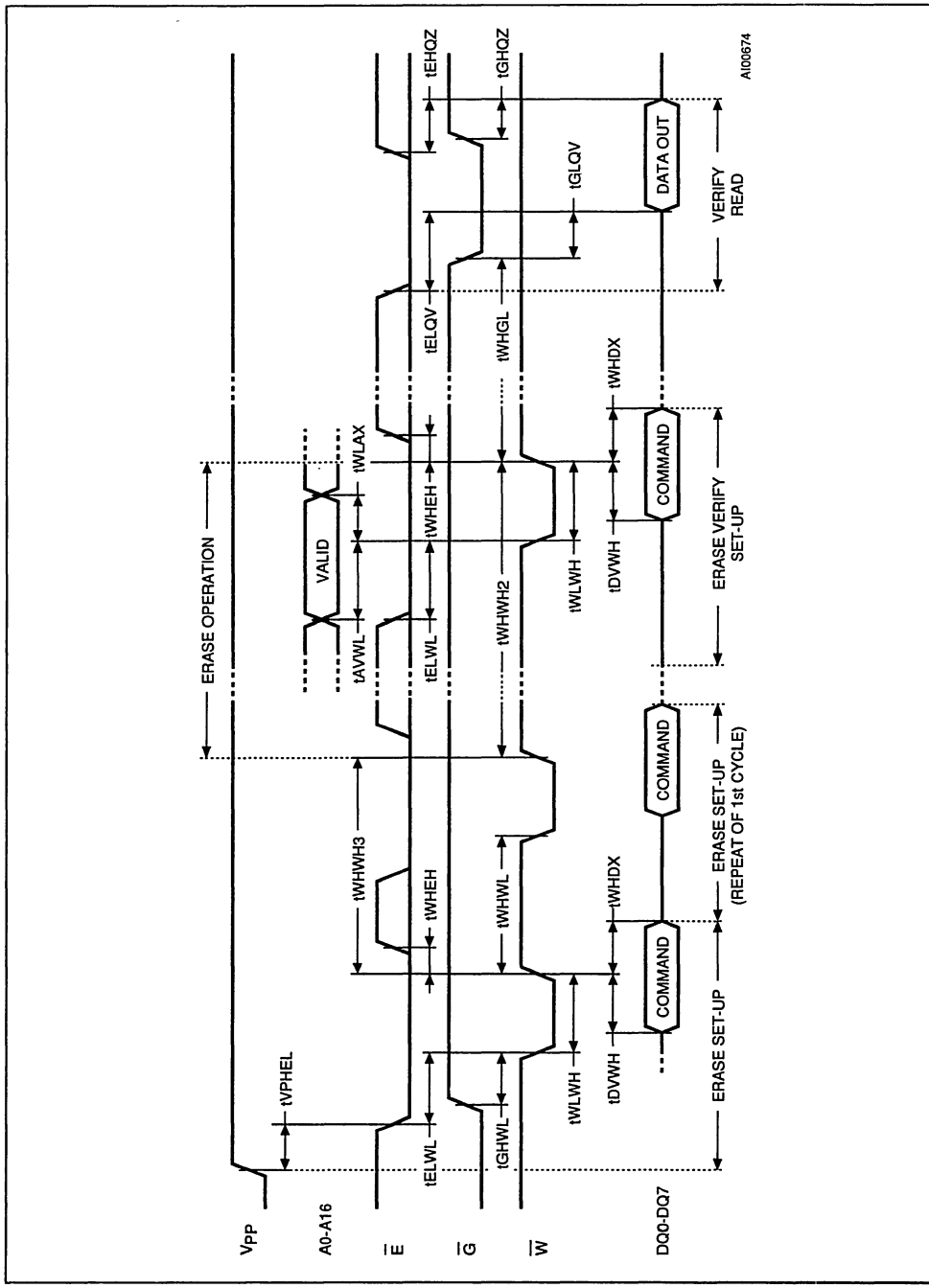


Figure 9. Erase Set-up and Erase Verify Commands Waveforms, $\overline{E}$ Controlled

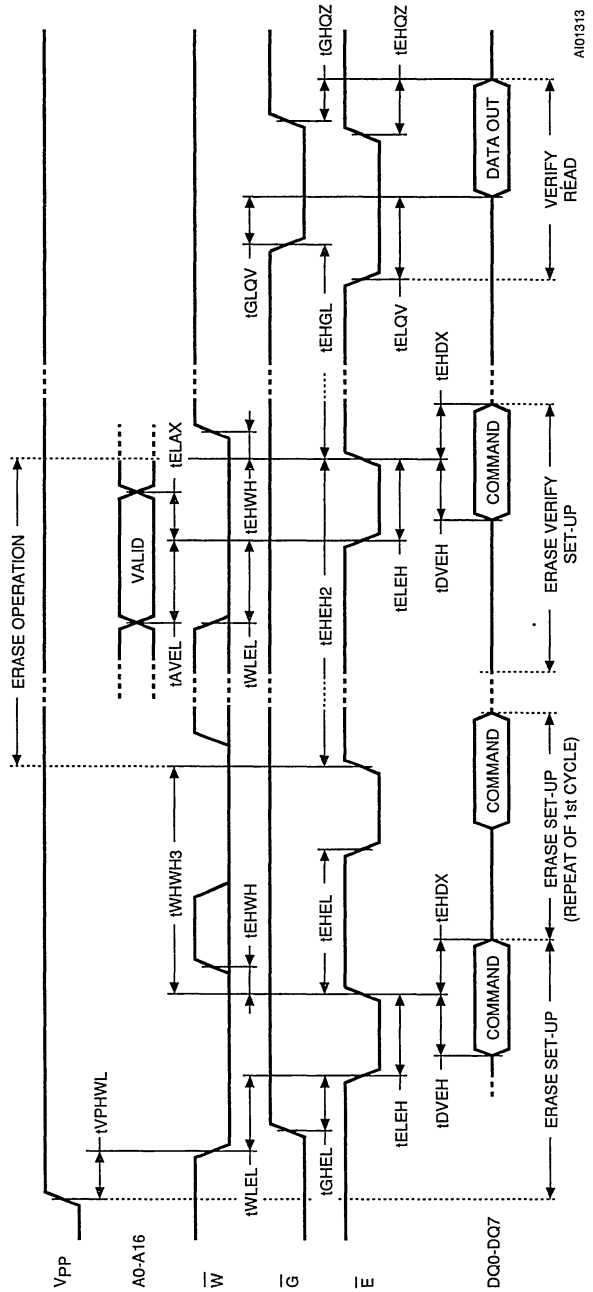


Figure 10. Program Set-up and Program Verify Commands Waveforms, $\overline{W}$ Controlled

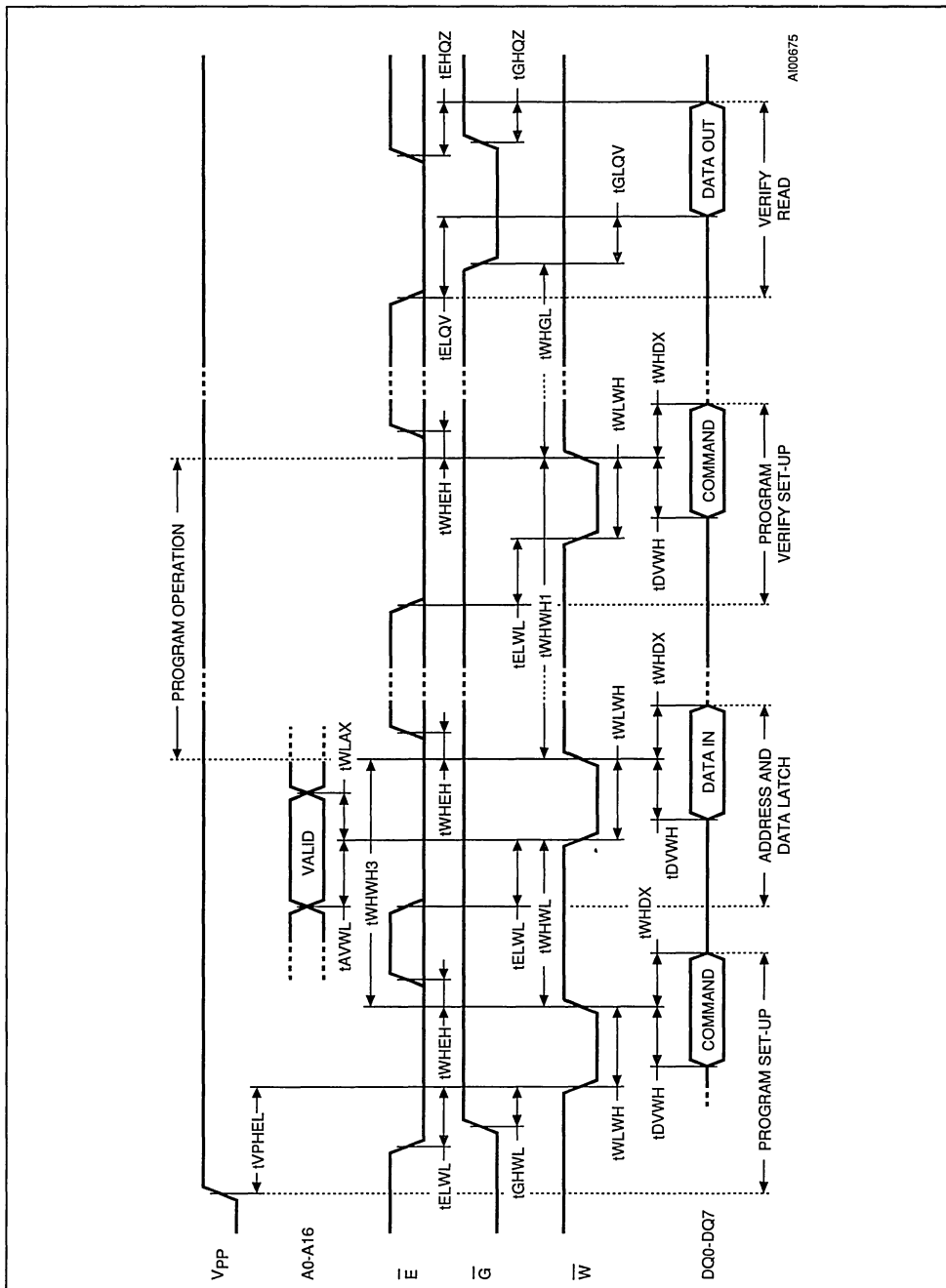


Figure 11. Program Set-up and Program Verify Commands Waveforms, $\overline{E}$ Controlled

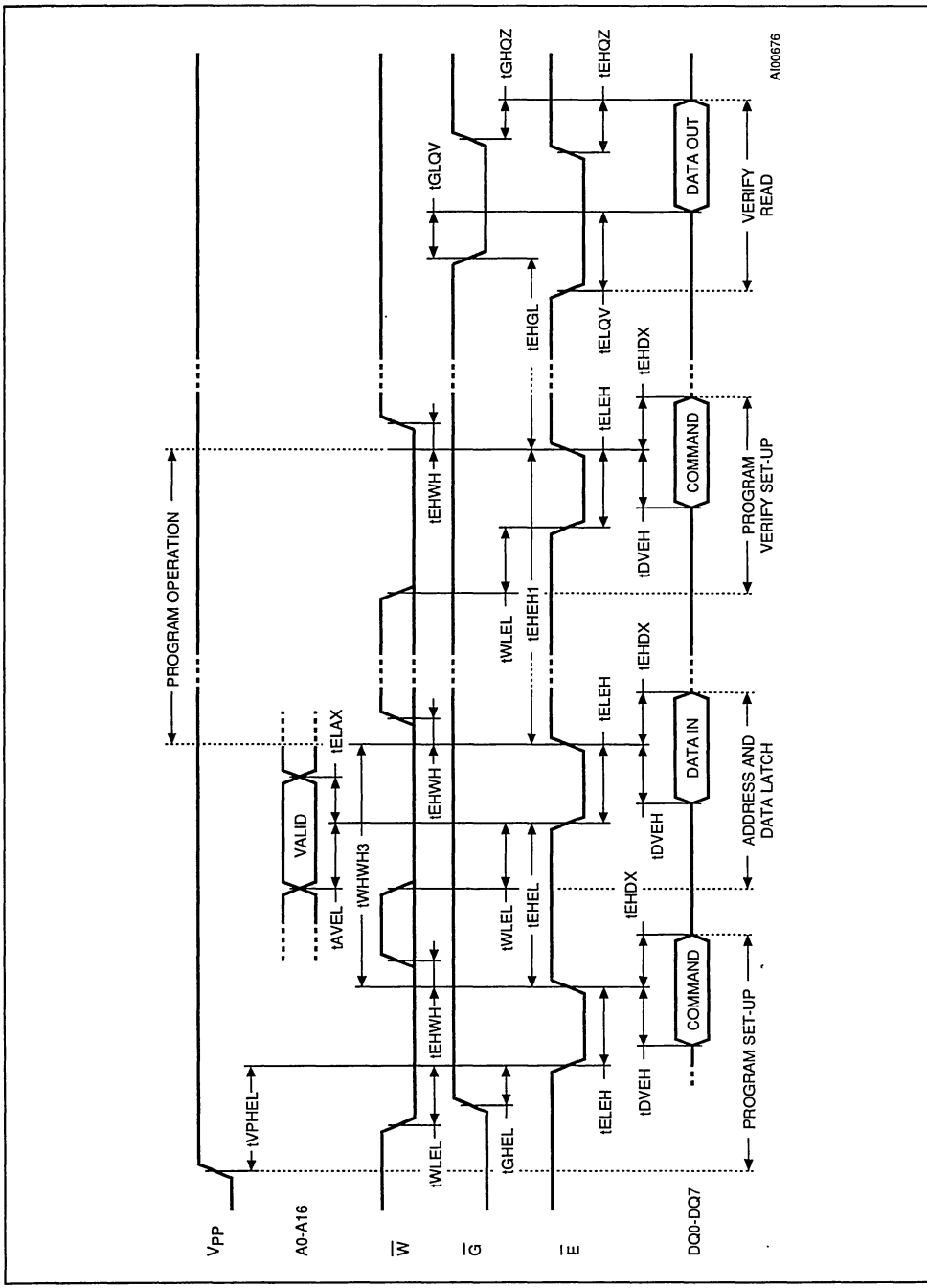


Figure 12. Erasing Flowchart

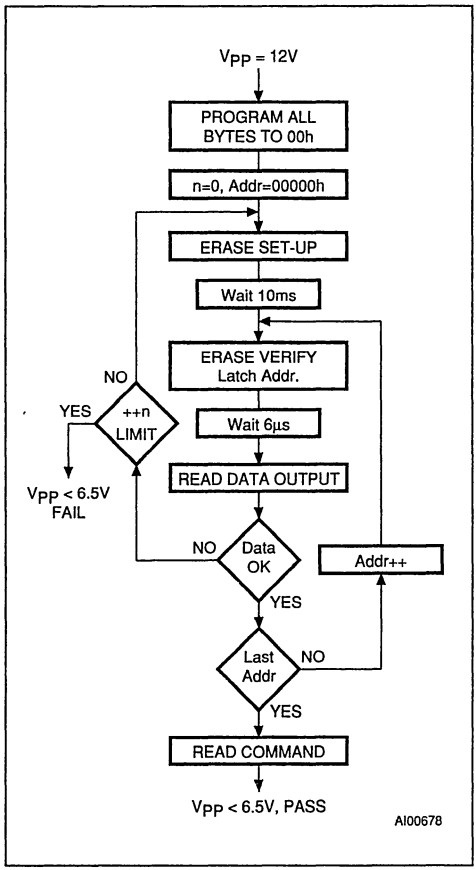
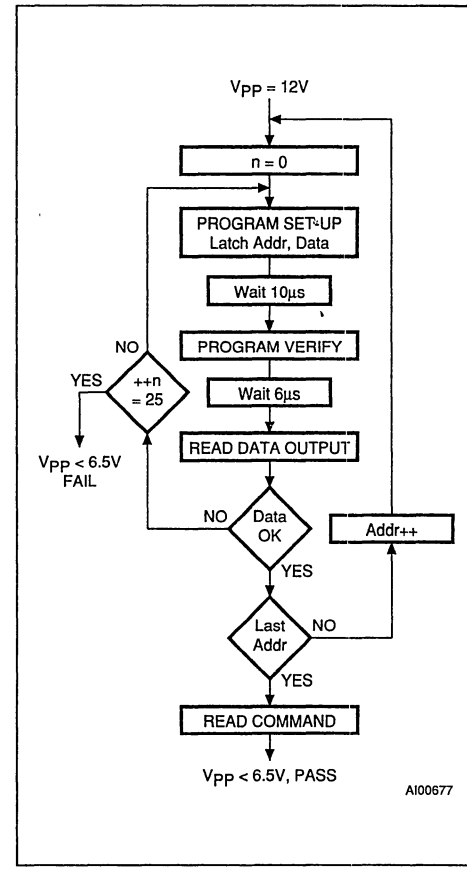


Figure 13. Programming Flowchart



Limit: 1000 at grade 1; 6000 at grades 3 & 6.

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programms all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME

Example: M28F101 -100 X N 1 R

Speed		V_{CC} Tolerance		Package		Temp. Range		Option	
-90	90 ns	blank	±10%	P	PDIP32	1	0 to 70 °C	R	Reverse Pin-Out
-100	100 ns	X	±5%	K	PLCC32	3	–40 to 125 °C	Y3	1,000 Cycles
-120	120 ns			N	TSOP32 8 x 20 mm	6	–40 to 85 °C	TR	Tape & Reel Packing
-150	150 ns								
-200	200 ns								

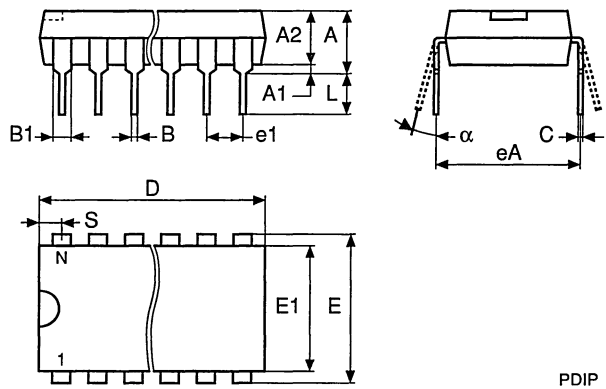
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP32 - 32 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N	32			32		

PDIP32



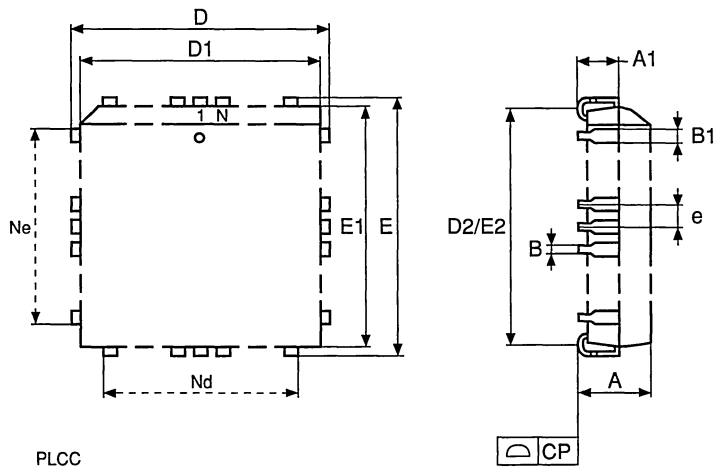
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32



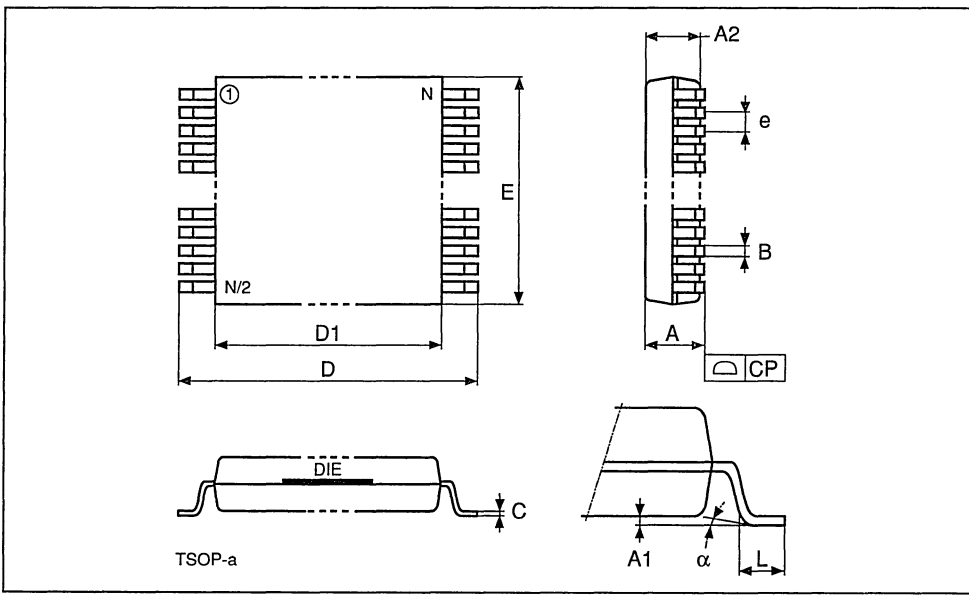
PLCC

Drawing is out of scale

TSOP32 Normal Pinout - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.04	1.24		0.041	0.049
A1		0.05	0.20		0.002	0.008
A2		0.95	1.06		0.037	0.042
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.90	20.12		0.783	0.792
D1		18.24	18.49		0.718	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.30	0.70		0.012	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32



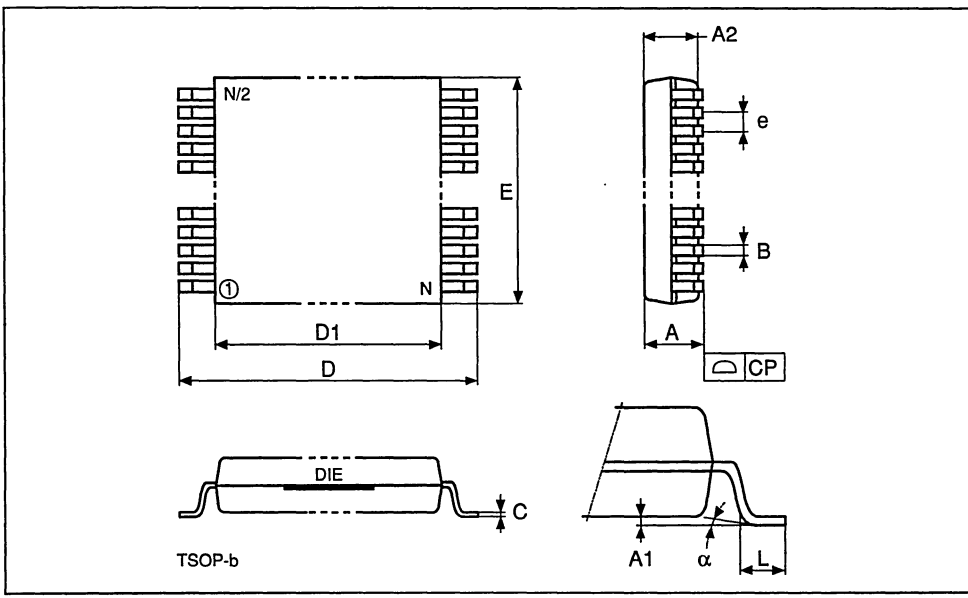
TSOP-a

Drawing is out of scale

TSOP32 Reverse Pinout - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.04	1.24		0.041	0.049
A1		0.05	0.20		0.002	0.008
A2		0.95	1.06		0.037	0.042
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.90	20.12		0.783	0.792
D1		18.24	18.49		0.718	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.30	0.70		0.012	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

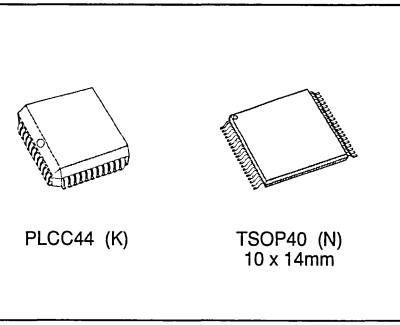
TSOP32



Drawing is out of scale

1 Megabit (64K x 16, Chip Erase) FLASH MEMORY

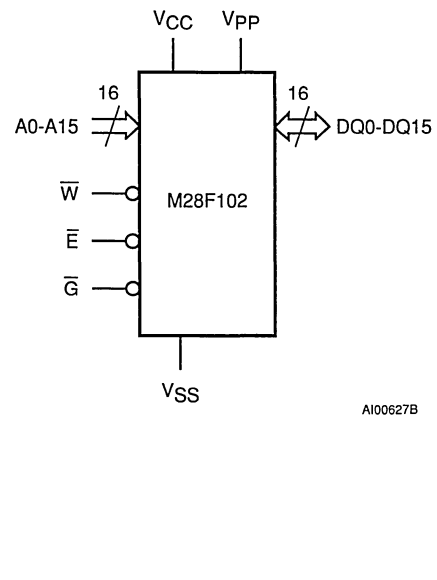
- FAST ACCESS TIME: 90ns
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER
- OTP COMPATIBLE PACKAGES and PINOUTS for PLCC44 and TSOP40
- EXTENDED TEMPERATURE RANGES



PLCC44 (K)

TSOP40 (N)
10 x 14mm

Figure 1. Logic Diagram



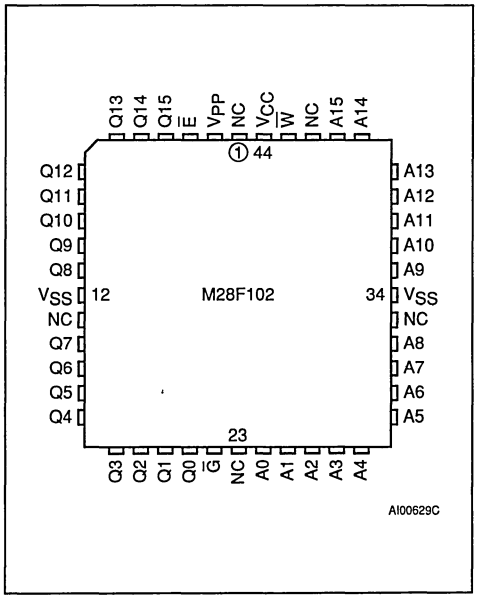
DESCRIPTION

The M28F102 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed word-by-word. It is organised as 64K words of 16 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F102 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

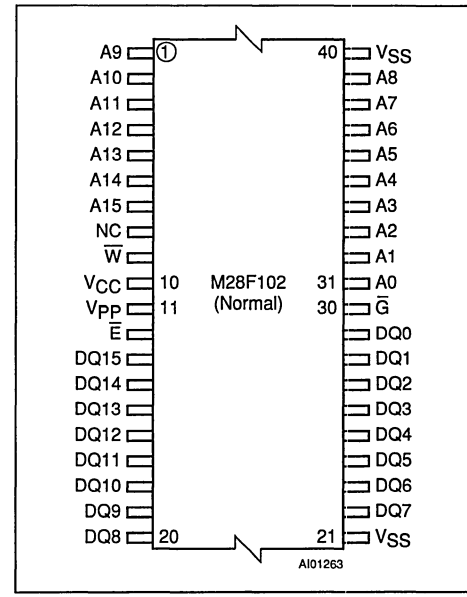
A0 - A15	Address Inputs
DQ0 - DQ15	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. LCC Pin Connections



Warning: NC = No Connection

Figure 2B. TSOP Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F102 FLASH MEMORY employs a technology similar to a 1 Megabit EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F102 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F102 has two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 50mA to 100µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device type code. All other address lines should be maintained Low while reading the codes. The electronic signature may also be accessed in Read/Write modes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output.

The supply voltage V_{CC} and the program voltage V_{PP} can be applied in any order. When the device is powered up or when V_{PP} is $\leq 6.5V$ the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ15
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Notes: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ15-DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	0	1	0	0	0	0	0	0020h
Device Code	V_{IH}	0	0	1	0	1	0	0	0	0	0050h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A15	DQ0-DQ15 (2)	Operation	A0-A15	DQ0-DQ15 (2)
Read	1	Write	X	xx00h			
Electronic Signature	2	Write	X	xx90h	Read	0000h	0020h
					Read	0001h	0050h
Setup Erase/ Erase	2	Write	X	xx20h			
					Write	X	xx20h
Erase Verify	2	Write	A0-A15	xxA0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	xx40h			
					Write	A0-A15	Data Input
Program Verify	2	Write	X	xxC0h	Read	X	Data Output
Reset	2	Write	X	0FFFFh	Write	X	0FFFFh

Notes: 1. X = V_{IL} or V_{IH}
2. x = Don't Care.

READ/WRITE MODES (cont'd)

V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 'xx00h' to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 'xx90h' to the command register. The following read cycle, with address inputs 0000h or 0001h, output the manufacturer or device type codes. The command is terminated by writing another valid command to the command register (for example Reset).

Erase and Erase Verify Modes. The memory is erased by first Programming all words to 0000h, the Erase command then erases them to 0FFFFh. The Erase Verify command is then used to read the memory word-by-word for a content of 0FFFFh.

The Erase Mode is set-up by writing 'xx20h' to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle.

Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 'xxA0h' to the command register and at the same time supplying the address of the word to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFFFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 'xxA0h' with the address of the word to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFFFh, another Erase operation is performed and verification continues from the address of the last verified word. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 'xx40h' to the command register. This is followed by a second write cycle which latches the address and data of the word to be programmed. The rising edge of $\overline{W}$ during this secind cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 'xxC0h' to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice '0FFFFh' to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

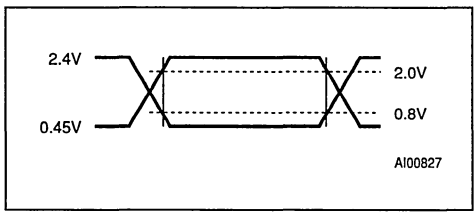


Figure 4. AC Testing Load Circuit

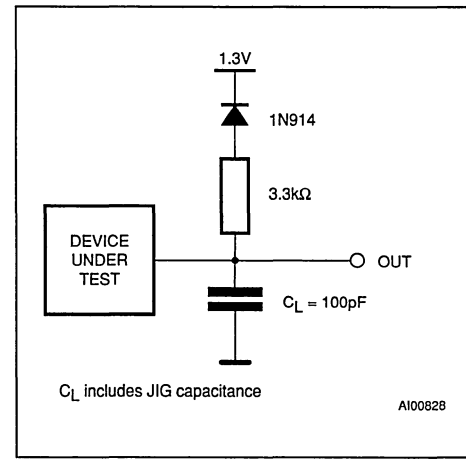


Table 6. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Table 7. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 8MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		30	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		15	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify		30	mA
I_{CC6} (1)	Supply Current (Electronic Signature)	$A9 = V_{ID}$		30	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±10	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		50	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		50	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
I_{PP5} (1)	Program Current (Electronic Signature)	$A9 = V_{ID}$		500	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA (grade 1)		0.45	V
		I_{OL} = 2.1mA (grade 3&6)		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	$A9 = V_{ID}$		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out		2.5		V

Note: Not 100% tested. Characterisation data available.

Table 8A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F102						Unit
				-90		-100		-120		
				Min	Max	Min	Max	Min	Max	
t_{WHGL}	-	Write Enable High to Output Enable Low		6		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	90		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		50		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	40	0	40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Table 8B. Read Only Mode AC Characteristics
(((T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%; 0V ≤ V_{PP} ≤ 6.5V)

Symbol	Alt	Parameter	Test Condition	M28F102				Unit
				-150		-200		
				Min	Max	Min	Max	
t_{WHGL}	-	Write Enable High to Output Enable Low		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		200		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	35	0	45	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 5. Read Mode AC Waveforms

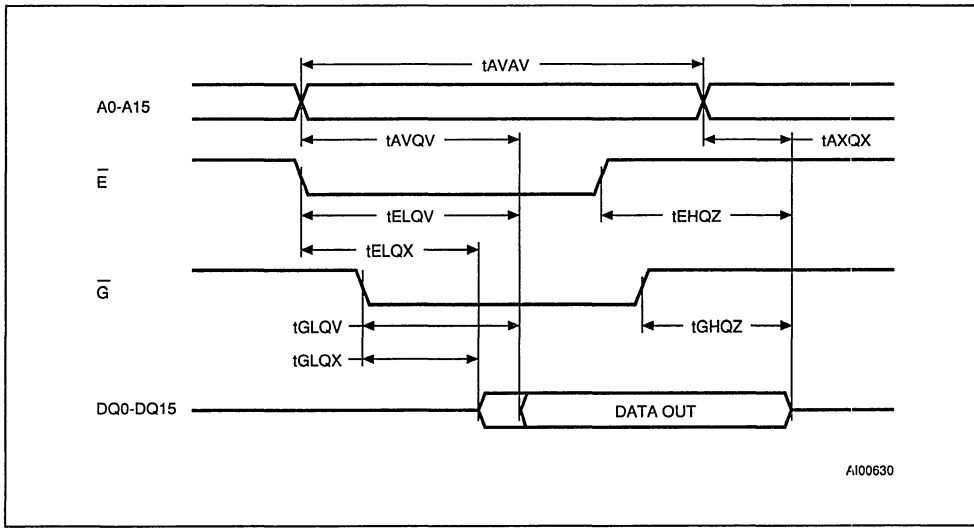


Figure 6. Read Command Waveforms

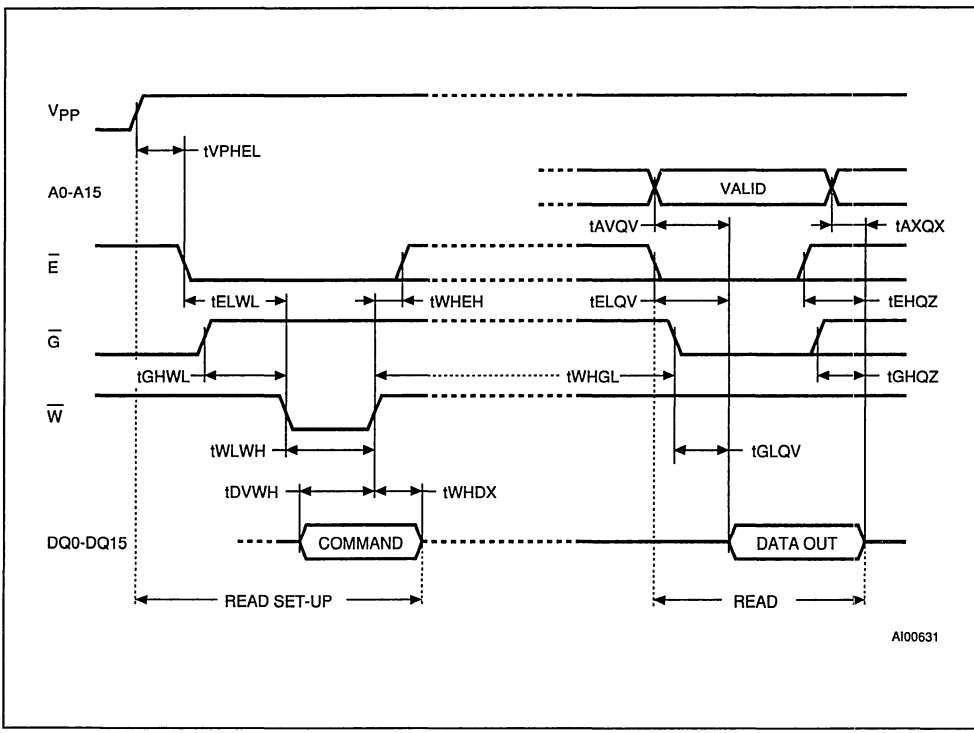


Figure 7. Electronic Signature Command Waveforms

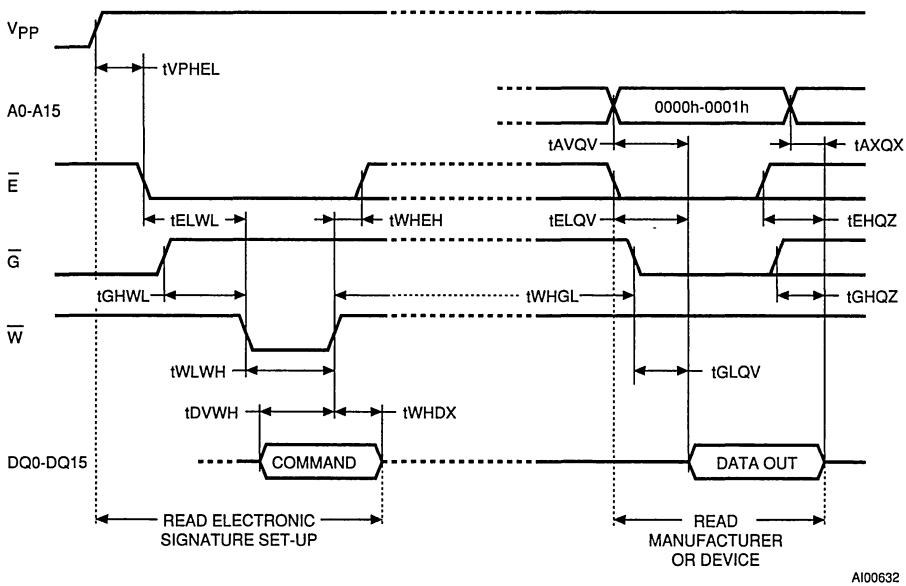


Table 9A. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10% or 5V ± 5%)

Symbol	Alt	Parameter	M28F102						Unit
			-90		-100		-120		
			Min	Max	Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time ($\overline{W}$ controlled)	90		100		120		ns
t_{EHEH3}	t_{WC}	Write Cycle Time ($\overline{E}$ controlled)	90		100		120		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	40		60		60		ns
t_{ELAX}		Chip Enable Low to Address Transition	60		80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	15		20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	40		50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	35		50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	40		60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	45		70		70		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		10		ns
t_{WHWH1}		Duration of Program Operation ($\overline{W}$ contr.)	9.5		9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation ($\overline{E}$ contr.)	9.5		9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation ($\overline{W}$ contr.)	9.5		9.5		9.5		ms
t_{EHEH2}		Duration of Erase Operation ($\overline{E}$ contr.)	9.5		9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		90		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		90		100		120	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		35		45		50	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		40		40		40	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Table 9B. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10% or 5V ± 5%)

Symbol	Alt	Parameter	M28F102				Unit
			-150		-200		
			Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time ($\overline{W}$ controlled)	150		200		ns
t_{EHEH3}	t_{WC}	Write Cycle Time ($\overline{E}$ controlled)	150		200		120
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	60		75		ns
t_{ELAX}		Chip Enable Low to Address Transition	80		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	20		20		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	60		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	70		80		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		ns
t_{WHWH1}		Duration of Program Operation ($\overline{W}$ controlled)	9.5		9.5		µs
t_{EHEH1}		Duration of Program Operation ($\overline{E}$ controlled)	9.5		9.5		µs
t_{WHWH2}		Duration of Erase Operation ($\overline{W}$ controlled)	9.5		9.5		ms
t_{EHEH2}		Duration of Erase Operation ($\overline{E}$ controlled)	9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		150		200	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		150		200	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55		60	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		55		60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		35		45	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms, $\overline{W}$ Controlled

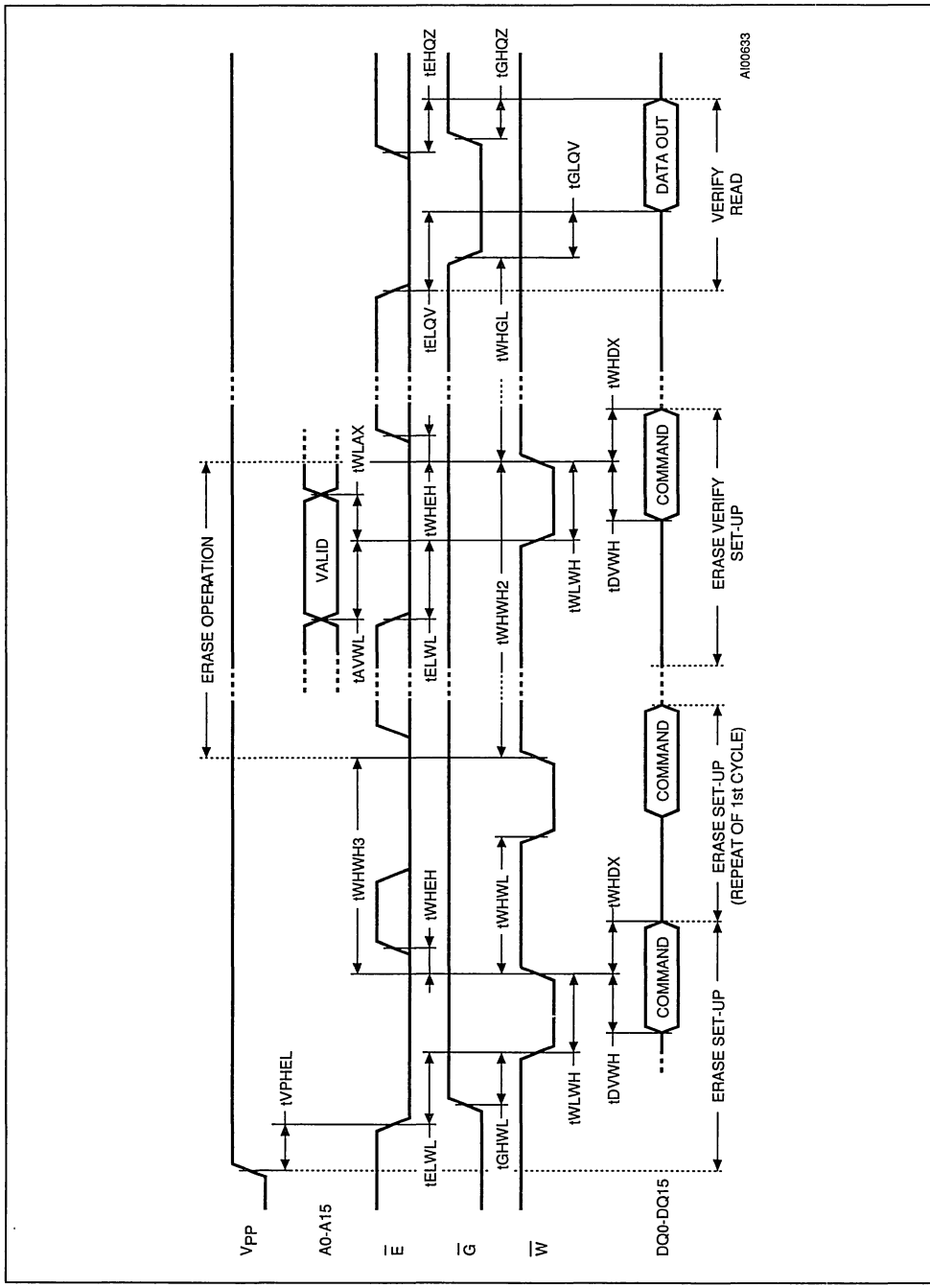


Figure 9. Erase Set-up and Erase Verify Commands Waveforms, $\overline{E}$ Controlled

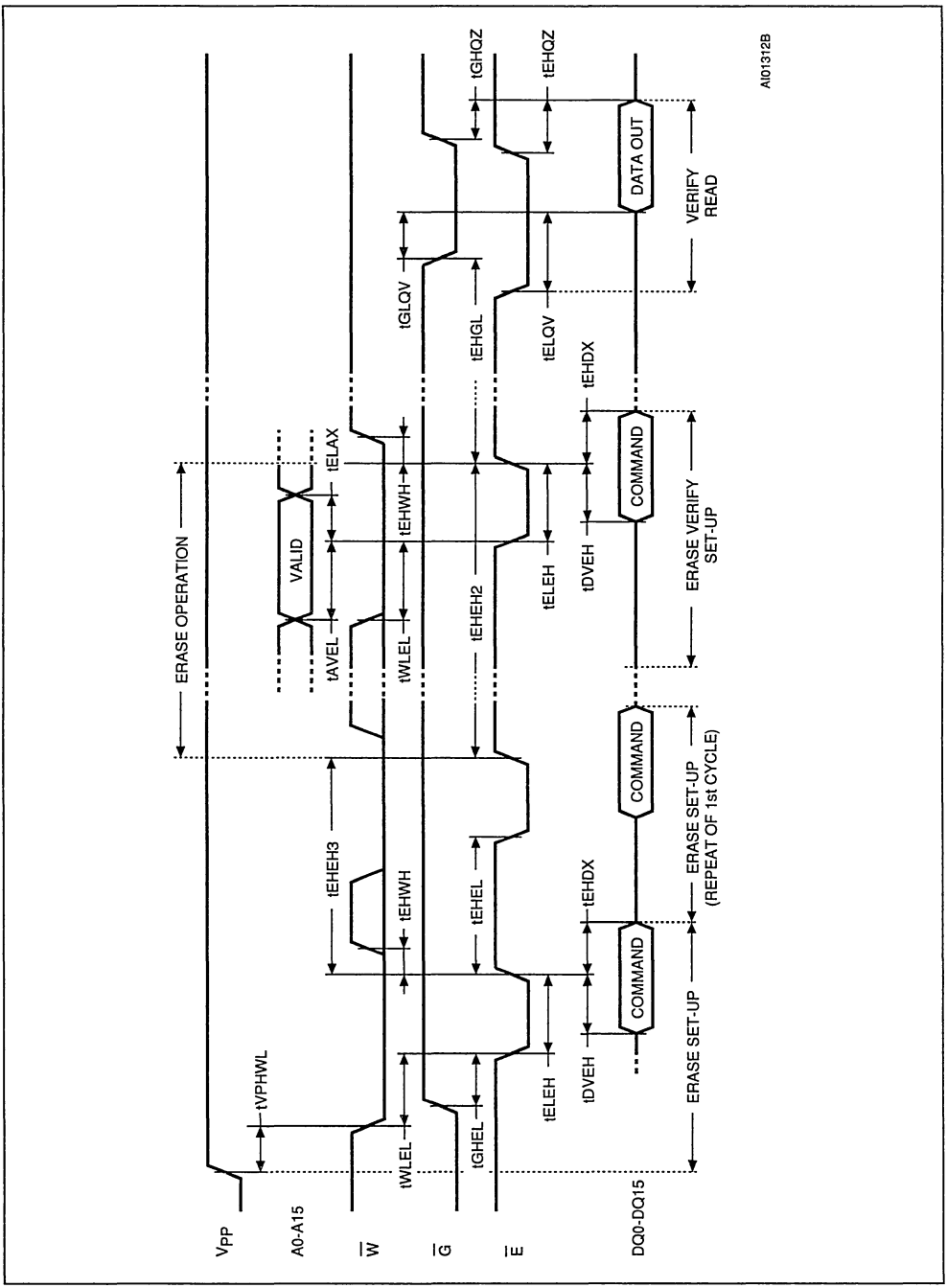


Figure 10. Program Set-up and Program Verify Commands Waveforms, $\overline{W}$ Controlled

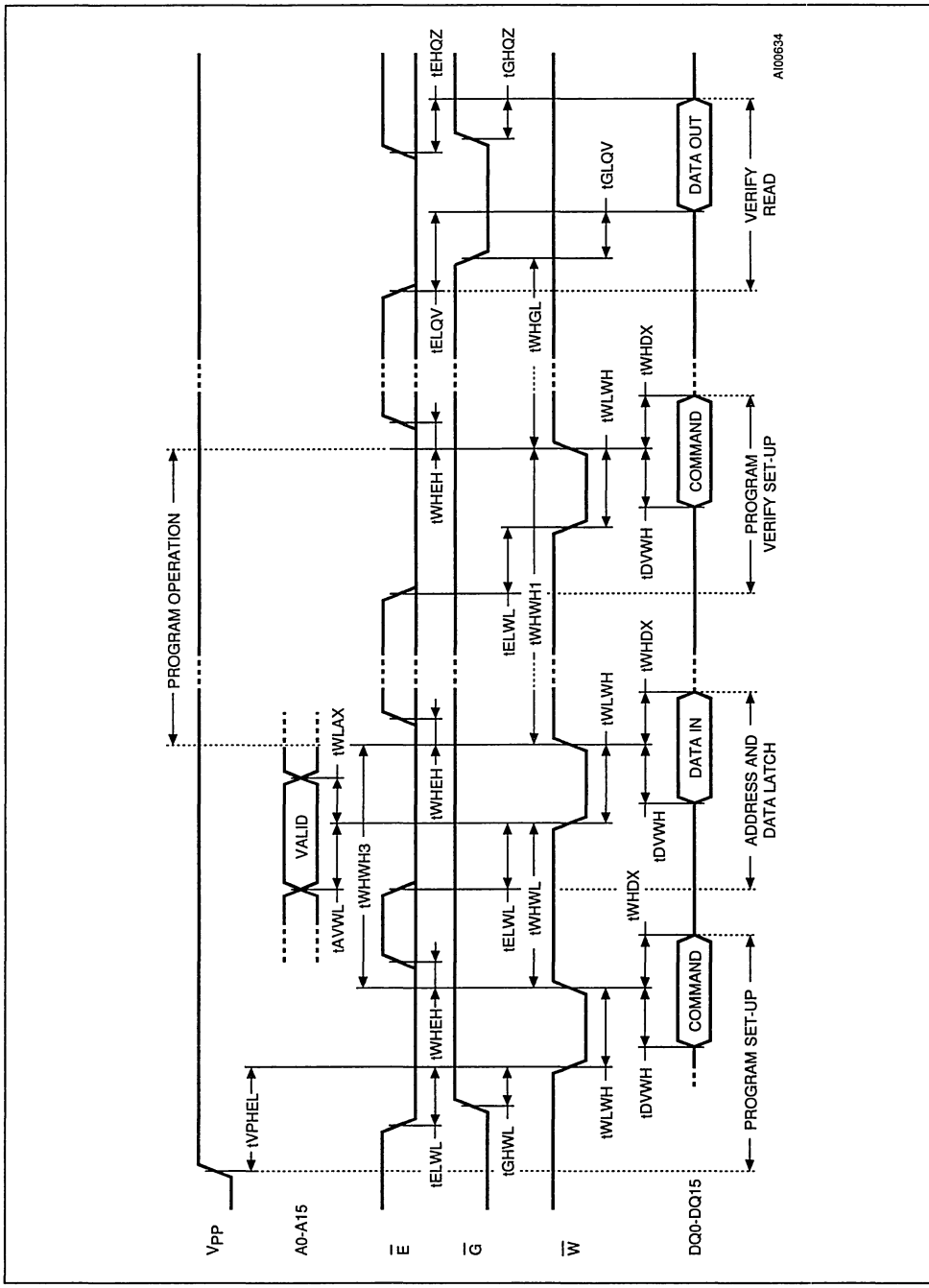


Figure 11. Program Set-up and Program Verify Commands Waveforms, $\overline{E}$ Controlled

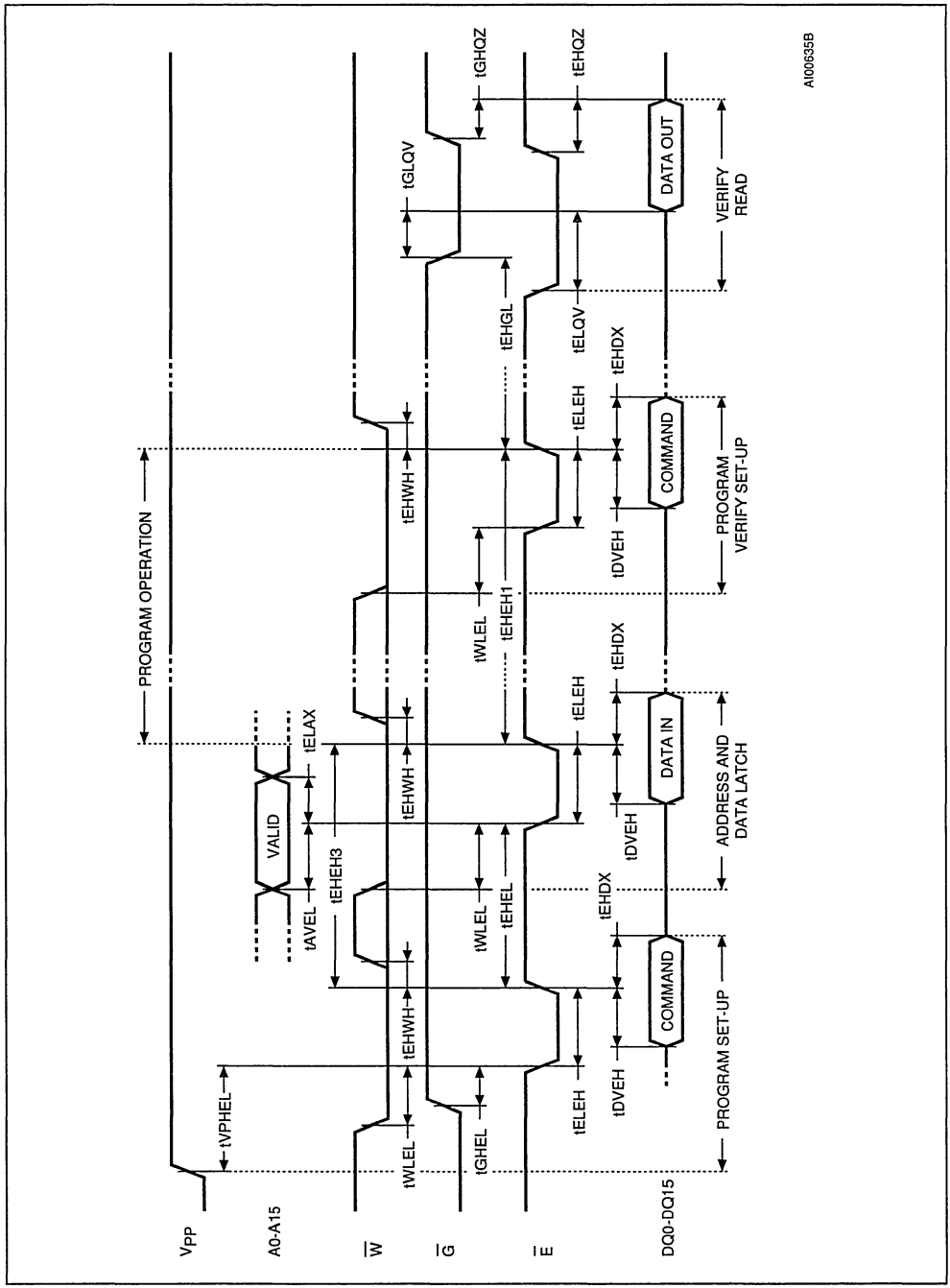


Figure 12. Erasing Flowchart

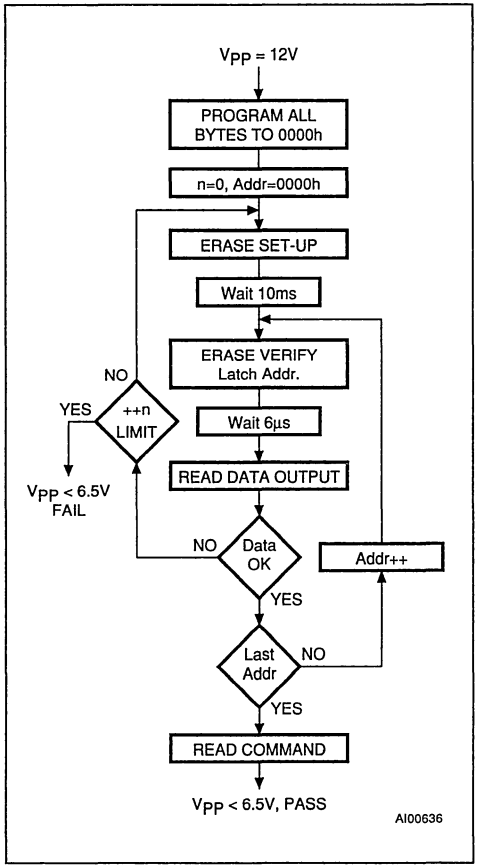
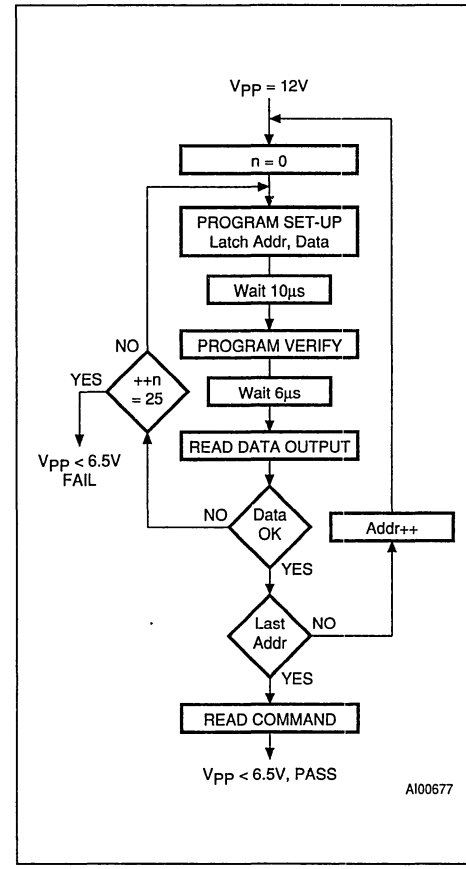


Figure 13. Programming Flowchart



Limit: 1000 at grade 1; 6000 at grades 3 & 6.

PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programs all words to 0000h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 'xx20h' to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 'xxA0h' to the command register together with the address of the word to be verified. The subsequent read cycle reads the data which is compared to 0FFFFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFFFh fails. If this occurs, the address of the last word checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a word until a correct verify occurs. Up to 25 programming operations are allowed for one word. Program is set-up by writing 'xx40h' to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 'xxC0h' to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME

Example: M28F102 -100 X K 1 TR

Speed		V_{CC} Tolerance		Package		Temp. Range		Option	
-90	90 ns	blank	± 10%	K	PLCC44	1	0 to 70 °C	TR	Tape & Reel Packing
-100	100 ns	X	± 5%	N	TSOP40 10 x 14mm	3	–40 to 125 °C		
-120	120 ns					6	–40 to 85 °C		
-150	150 ns								
-200	200 ns								

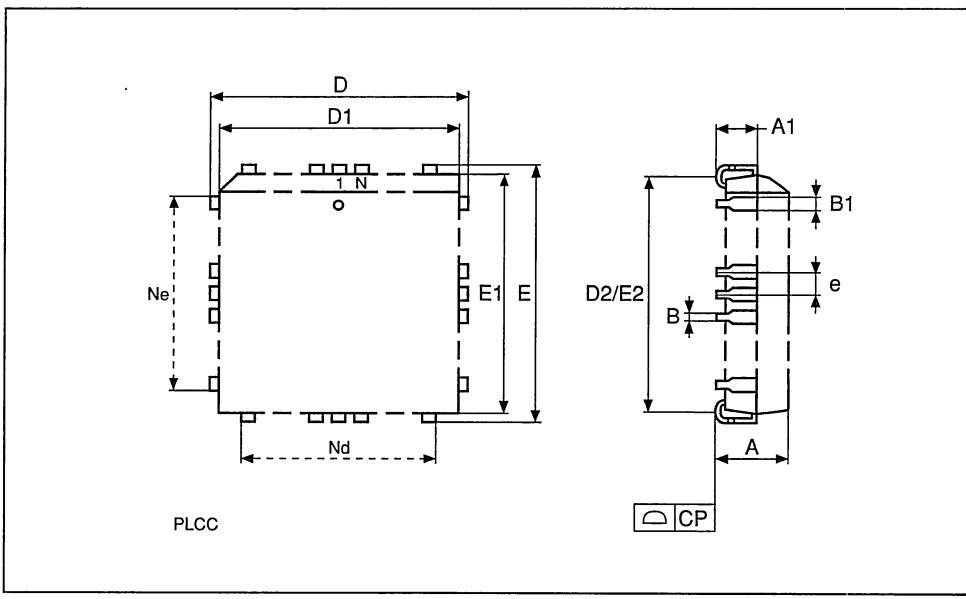
For a list of available options (Speed, V_{CC} Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PLCC44 - 44 lead Plastic Leaded Chip Carrier, square

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		4.20	4.70		0.165	0.185
A1		2.29	3.04		0.090	0.120
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		17.40	17.65		0.685	0.695
D1		16.51	16.66		0.650	0.656
D2		14.99	16.00		0.590	0.630
E		17.40	17.65		0.685	0.695
E1		16.51	16.66		0.650	0.656
E2		14.99	16.00		0.590	0.630
e	1.27	–	–	0.050	–	–
N		44			44	
CP			0.10			0.004

PLCC44

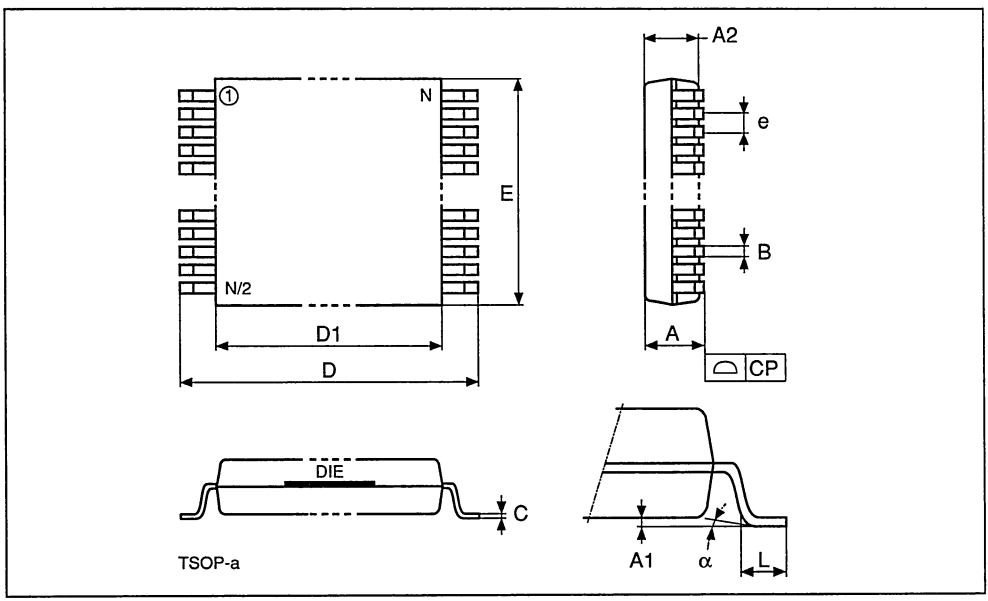


Drawing is out of scale

TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 14mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.80	14.20		0.543	0.559
D1		12.30	12.50		0.484	0.492
E		9.90	10.10		0.390	0.398
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		40			40	
CP			0.10			0.004

TSOP40



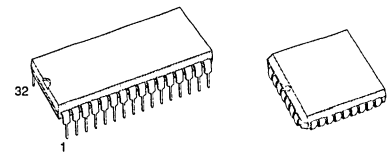
TSOP-a

Drawing is out of scale

2 Megabit (256K x 8, Chip Erase) FLASH MEMORY

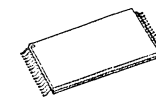
PRODUCT PREVIEW

- FAST ACCESS TIMES
  - 60ns for M28F201 version
  - 150ns for M28V201 version
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 PROGRAM/ERASE CYCLES
- 12V PROGRAMMING VOLTAGE
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F201 version
  - 3.3V ± 0.3V for M28V201 version
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER
- OTP COMPATIBLE PACKAGES and PINOUTS
- EXTENDED TEMPERATURE RANGES



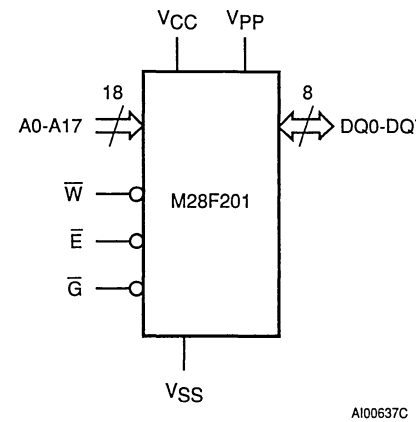
PDIP32 (P)

PLCC32 (K)



TSOP32 (N)
8 x 20 mm

Figure 1. Logic Diagram



DESCRIPTION

The M28F201, M28V201 FLASH MEMORY products are non-volatile memories which may be erased electrically at the chip level and programmed byte-by-byte. They are organised as 256K bytes. They use a command register architecture to select the operating modes and thus provide a simple microprocessor interface.

Table 1. Signal Names

A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

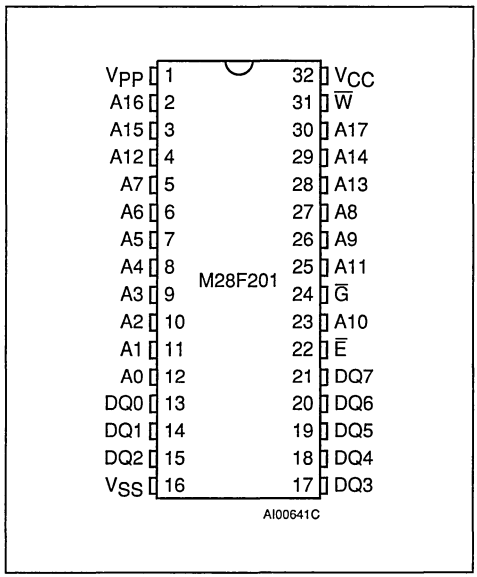


Figure 2B. LCC Pin Connections

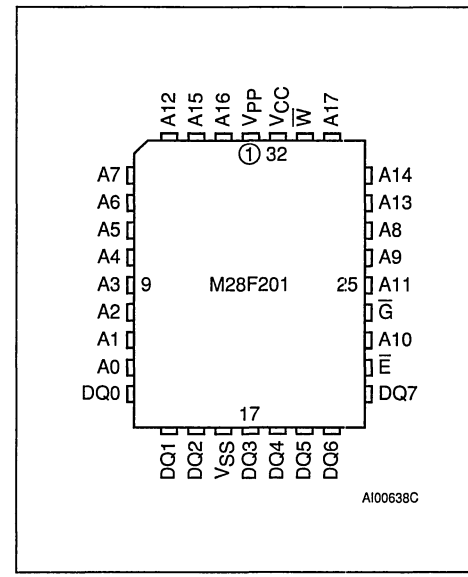


Figure 2C. TSOP Pin Connections

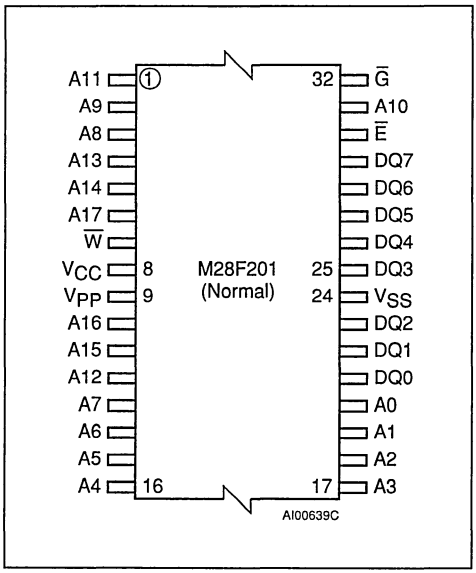


Figure 2D. TSOP Reverse Pin Connections

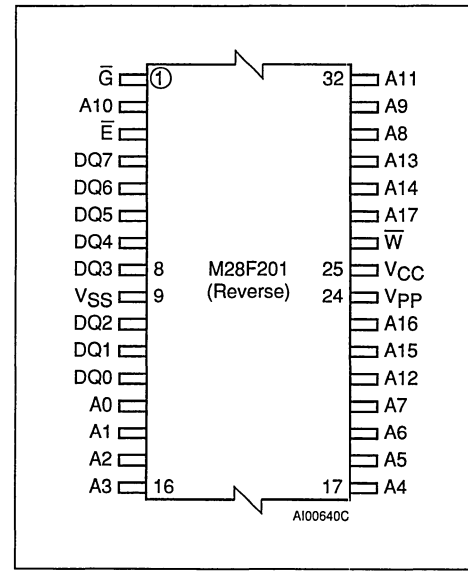


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DESCRIPTION (cont'd)

The M28F201, M28V201 FLASH MEMORY products are suitable for applications where the memory has to be reprogrammed in the equipment.

The access time of 60ns makes the device suitable for use in high speed microprocessor systems, while the low supply voltage capability makes it ideal for portable applications.

DEVICE OPERATION

The M28F201, M28V201 FLASH MEMORY products employ a technology similar to a 2 Megabit EPROM but add to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and the M28F201 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

READ ONLY MODES, $V_{PP} \leq 6.5V$

For all Read Only Modes, except Standby Mode, the Write Enable input $\overline{W}$ should be High. In the Standby Mode this input is 'don't care'.

Read Mode. The M28F201, M28V201 have two enable inputs, $\overline{E}$ and $\overline{G}$, both of which must be Low in order to output data from the memory. The Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data on to the output, independant of the device selection.

Standby Mode. In the Standby Mode the maximum supply current is reduced from 30mA to 100µA. The device is placed in the Standby Mode by applying a High to the Chip Enable ($\overline{E}$) input. When in the Standby Mode the outputs are in a high impedance state, independant of the Output Enable ($\overline{G}$) input.

Output Disable Mode. When the Output Enable ($\overline{G}$) is High the outputs are in a high impedance state.

Electronic Signature Mode. This mode allows the read out of two binary codes from the device which identify the manufacturer and device type. This mode is intended for use by programming equipment to automatically select the correct erase and programming algorithms. The Electronic Signature Mode is active when a high voltage (11.5V to 13V) is applied to address line A9 with $\overline{E}$ and $\overline{G}$ Low. With A0 Low the output data is the manufacturer code, when A0 is High the output is the device code. All other address lines should be maintained Low while reading the codes. The electronic signature can also be accessed in Read/Write modes.

READ/WRITE MODES, $11.4V \leq V_{PP} \leq 12.6V$

When V_{PP} is High both read and write operations may be performed. These are defined by the contents of an internal command register. Commands

Table 3. Operations (1)

	V_{PP}	Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	A9	DQ0 - DQ7
Read Only	V_{PPL}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z
		Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes
Read/Write (2)	V_{PPH}	Read	V_{IL}	V_{IL}	V_{IH}	A9	Data Output
		Write	V_{IL}	V_{IH}	V_{IL} Pulse	A9	Data Input
		Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
		Standby	V_{IH}	X	X	X	Hi-Z

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Command Table

Table 4. Electronic Signature

Identifier	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code: M28F201	V_{IH}	1	1	1	1	0	1	0	0	0F4h
Device Code: M28V201	V_{IH}	1	1	1	1	0	1	0	1	0F5h

Table 5. Commands (1)

Command	Cycles	1st Cycle			2nd Cycle		
		Operation	A0-A17	DQ0-DQ7	Operation	A0-A17	DQ0-DQ7
Read	1	Write	X	00h			
Electronic Signature (2)	2	Write	X	80h or 90h	Read	00000h	20h
					Read	00001h	0F4h or 0F5h
Setup Erase/ Erase	2	Write	X	20h			
					Write	X	20h
Erase Verify	2	Write	A0-A17	0A0h	Read	X	Data Output
Setup Program/ Program	2	Write	X	40h			
					Write	A0-A17	Data Input
Program Verify	2	Write	X	0C0h	Read	X	Data Output
Reset	2	Write	X	0FFh	Write	X	0FFh

Note: 1. X = V_{IL} or V_{IH}
2. Refer also to the Electronic Signature Table

Table 6. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

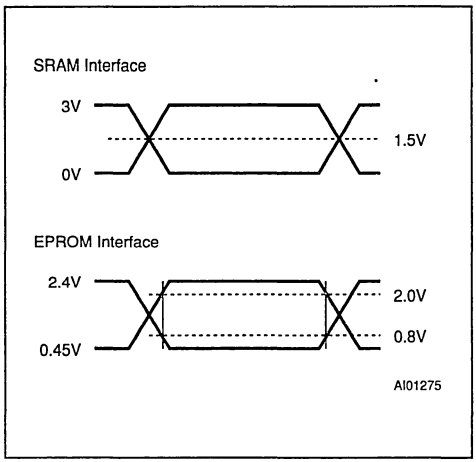


Figure 4. AC Testing Load Circuit

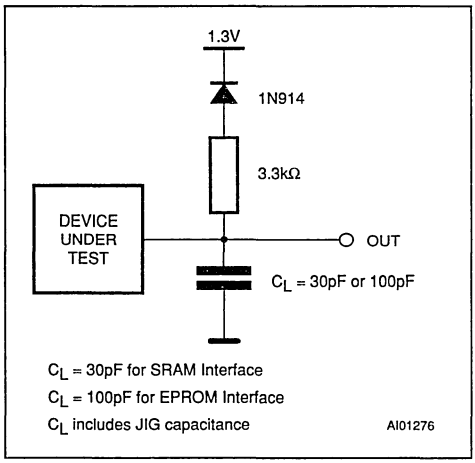


Table 7. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

READ/WRITE MODES (cont'd)

may be written to this register to set-up and execute, Erase, Erase Verify, Program, Program Verify and Reset modes. Each of these modes needs 2 cycles. Every mode starts with a write operation to set-up the command, this is followed by either read or write operations. The device expects the first cycle to be a write operation and does not corrupt data at any location in memory. Read mode is set-up with one cycle only and may be followed by any number of read operations to output data. Electronic Signature Read mode is set-up with one cycle and followed by a read cycle to output the manufacturer or device codes.

A write to the command register is made by bringing $\overline{W}$ Low while $\overline{E}$ is Low. The falling edge of $\overline{W}$ latches Addresses, while the rising edge latches Data, which are used for those commands that require address inputs, command input or provide data output. The supply voltage V_{CC} and the program voltage V_{PP} can be applied in any order. When the device is powered up or when V_{PP} is ≤ 6.5V the contents of the command register default to 00h, thus automatically setting-up Read operations. In addition a specific command may be used to set the command register to 00h for reading the memory.

The system designer may chose to provide a constant high V_{PP} and use the register commands for

Table 8. DC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current (Read)	$\overline{E} = V_{IL}$, f = 10MHz		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1)	Supply Current (Programming)	During Programming		10	mA
I_{CC3} (1)	Supply Current (Program Verify)	During Verify		20	mA
I_{CC4} (1)	Supply Current (Erase)	During Erasure		20	mA
I_{CC5} (1)	Supply Current (Erase Verify)	During Erase Verify)		20	mA
I_{LPP}	Program Leakage Current	$V_{PP} \le V_{CC}$		±10	µA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
		$V_{PP} \le V_{CC}$		±10	µA
I_{PP1} (1)	Program Current (Programming)	$V_{PP} = V_{PPH}$, During Programming		30	mA
I_{PP2} (1)	Program Current (Program Verify)	$V_{PP} = V_{PPH}$, During Verify		5	mA
I_{PP3} (1)	Program Current (Erase)	$V_{PP} = V_{PPH}$, During Erase		30	mA
I_{PP4} (1)	Program Current (Erase Verify)	$V_{PP} = V_{PPH}$, During Erase Verify		5	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage TTL		2	V_{CC} + 0.5	V
	Input High Voltage CMOS		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.4		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Read Operations)		0	6.5	V
V_{PPH}	Program Voltage (Read/Write Operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	13	V
I_{ID} (1)	A9 Current (Electronic Signature)	A9 = V_{ID}		200	µA
V_{LKO}	Supply Voltage, Erase/Program Lock-out	M28F201	2.2		V
		M28V201	2.0		V

Note: 1. Not 100% tested. Characterisation Data available.

READ/WRITE MODES (cont'd)

all operations, or to switch the V_{PP} from low to high only when needing to erase or program the memory. All command register access is inhibited when V_{CC} falls below the Erase/Write Lockout Voltage (V_{LKO}) of 2.5V.

If the device is deselected during Erasure, Programming or Verification it will draw active supply currents until the operations are terminated.

The device is protected against stress caused by long erase or program times. If the end of Erase or Programming operations are not terminated by a Verify cycle within a maximum time permitted, an internal stop timer automatically stops the operation. The device remains in an inactive state, ready to start a Verify or Reset Mode operation.

Read Mode. The Read Mode is the default at power up or may be set-up by writing 00h to the command register. Subsequent read operations output data from the memory. The memory remains in the Read Mode until a new command is written to the command register.

Electronic Signature Mode. In order to select the correct erase and programming algorithms for on-board programming, the manufacturer and devices code may be read directly. It is not neccessary to apply a high voltage to A9 when using the command register. The Electronic Signature Mode is set-up by writing 80h or 90h to the command register. The following read cycle, with address inputs 00000h or 00001h, output the manufacturer or device codes. The command is terminated by writing another valid command to the command register (for example Reset).

Table 9A. Read Only Mode AC Characteristics
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C)

Symbol	Alt	Parameter	Test Condition	M28F201						Unit
				-60		-70		-80		
				V_{CC} = 5V±5%		V_{CC} = 5V±10%		V_{CC} = 5V±10%		
				SRAM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	60		70		80		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		60		70		80	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		60		70		80	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		25		30		35	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	25	0	25	0	30	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	25	0	25	0	30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Table 9B. Read Only Mode AC Characteristics
((T$_A$ = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C)

Symbol	Alt	Parameter	Test Condition	M28F201						Unit
				-90		-120		-150		
				V_{CC} = 5V±10%		V_{CC} = 5V±10%		V_{CC} = 5V±10%		
				EPROM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{WHGL}		Write Enable High to Output Enable Low		6		6		6		µs
t_{AVAV}	t_{RC}	Read Cycle Time	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	90		120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		35		50		55	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	30	0	30	0	35	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	30	0	30	0	35	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Erase and Erase Verify Modes. The memory is erased by first Programming all bytes to 00h, the Erase command then erases them to 0FFh. The Erase Verify command is then used to read the memory byte-by-byte for a content of 0FFh.

The Erase Mode is set-up by writing 20h to the command register. The write cycle is then repeated to start the erase operation. Erasure starts on the rising edge of $\overline{W}$ during this second cycle. Erase is followed by an Erase Verify which reads an addressed byte.

Erase Verify Mode is set-up by writing 0A0h to the command register and at the same time supplying the address of the byte to be verified. The rising edge of $\overline{W}$ during the set-up of the first Erase Verify Mode stops the Erase operation. The following read cycle is made with an internally generated margin voltage applied, reading 0FFh indicates that all bits of the addressed byte are fully erased. The whole contents of the memory are verified by repeating the Erase Verify Operation, first writing the set-up code 0A0h with the address of the byte to be verified and then reading the byte contents in a second read cycle.

As the Erase algorithm flow chart shows, when the data read during Erase Verify is not 0FFh, another Erase operation is performed and verification continues from the address of the last verified byte. The command is terminated by writing another valid command to the command register (for example Program or Reset).

Program and Program Verify Modes. The Program Mode is set-up by writing 40h to the command register. This is followed by a second write cycle which latches the address and data of the byte to be programmed. The rising edge of $\overline{W}$ during this

Figure 5. Read Mode AC Waveforms

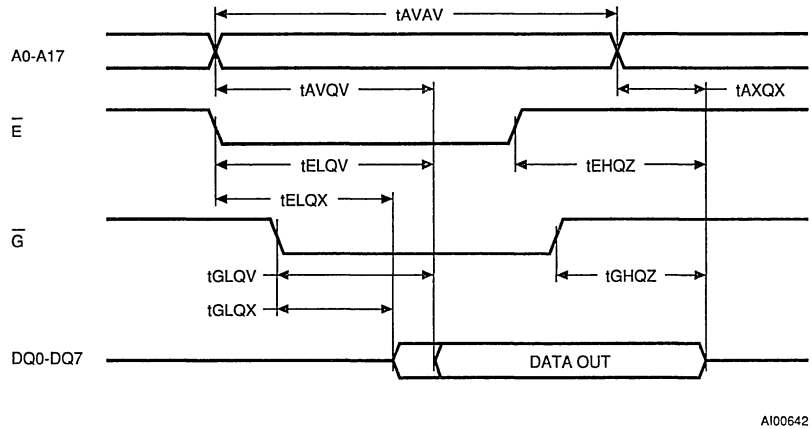


Figure 6. Read Command Waveforms

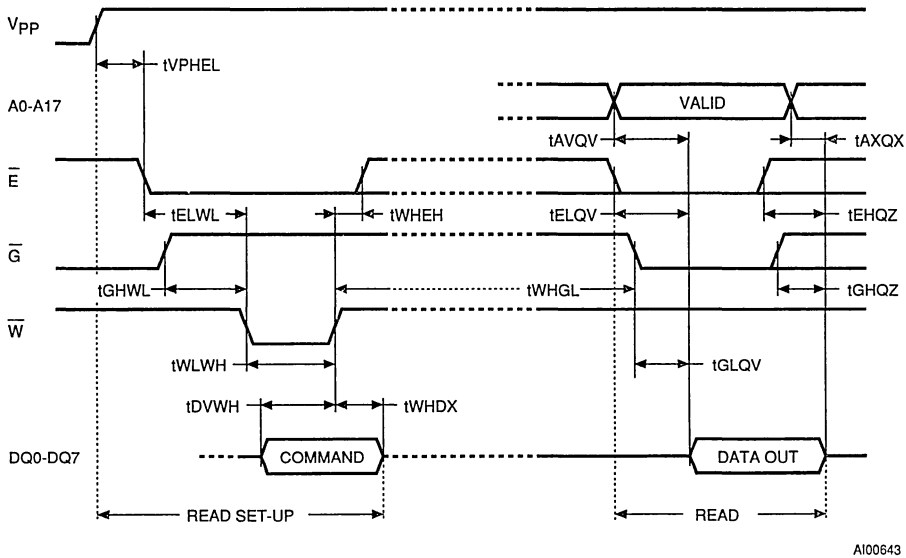
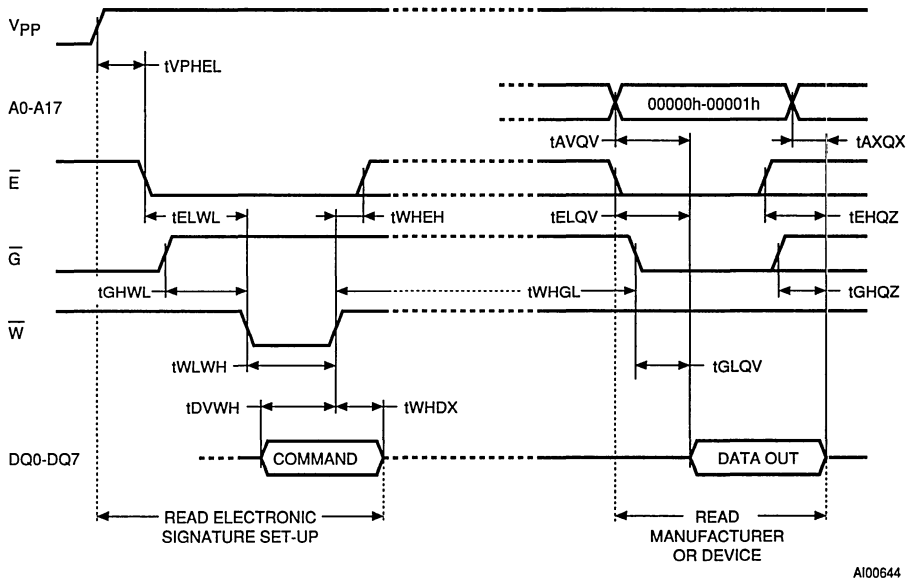


Figure 7. Electronic Signature Command Waveforms



READ/WRITE MODES (cont'd)

second cycle starts the programming operation. Programming is followed by a Program Verify of the data written.

Program Verify Mode is set-up by writing 0C0h to the command register. The rising edge of $\overline{W}$ during the set-up of the Program Verify Mode stops the Programming operation. The following read cycle, of the address already latched during programming, is made with an internally generated margin voltage applied, reading valid data indicates that all bits have been programmed.

Reset Mode. This command is used to safely abort Erase or Program Modes. The Reset Mode is set-up and performed by writing twice 0FFh to the command register. The command should be followed by writing a valid command to the the command register (for example Read).

Table 10A. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C)

Symbol	Alt	Parameter	M28F201						Unit
			-60		-70		-80		
			V_{CC} = 5V±5%		V_{CC} = 5V±10%		V_{CC} = 5V±10%		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time ($\overline{W}$ controlled)	60		70		80		ns
t_{EHEH3}	t_{WC}	Write Cycle Time ($\overline{E}$ controlled)	60		70		80		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	40		40		45		ns
t_{ELAX}		Chip Enable Low to Address Transition	50		50		60		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	40		40		45		ns
t_{DVEH}		Input Valid to Chip Enable High	40		40		45		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	40		40		45		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	50		50		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		10		ns
t_{WHWH1}		Duration of Program Operation ($\overline{W}$ contr.)	10		10		10		µs
t_{EHEH1}		Duration of Program Operation ($\overline{E}$ contr.)	10		10		10		µs
t_{WHWH2}		Duration of Erase Operation ($\overline{W}$ contr.)	9.5		9.5		9.5		ms
t_{EHEH2}		Duration of Erase Operation ($\overline{E}$ contr.)	9.5		9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		60		70		80	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		60		70		80	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		30		30		30	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		25		25		30	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		25		25		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Table 10B. Read/Write Mode AC Characteristics, $\overline{W}$ and $\overline{E}$ Controlled
(T_A = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C)

Symbol	Alt	Parameter	M28F201						Unit
			-90		-120		-150		
			V_{CC} = 5V±10%		V_{CC} = 5V±10%		V_{CC} = 5V±10%		
			EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{VPHEL}		V_{PP} High to Chip Enable Low	1		1		1		µs
t_{VPHWL}		V_{PP} High to Write Enable Low	1		1		1		µs
t_{WHWH3}	t_{WC}	Write Cycle Time ($\overline{W}$ controlled)	90		120		150		ns
t_{EHEH3}	t_{WC}	Write Cycle Time ($\overline{E}$ controlled)	90		120		150		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}		Address Valid to Chip Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		50		50		ns
t_{ELAX}		Chip Enable Low to Address Transition	60		60		80		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLEL}		Write Enable Low to Chip Enable Low	0		0		0		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		µs
t_{GHEL}		Output Enable High to Chip Enable Low	0		0		0		µs
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	45		50		50		ns
t_{DVEH}		Input Valid to Chip Enable High	45		50		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High (Write Pulse)	45		50		60		ns
t_{ELEH}		Chip Enable Low to Chip Enable High (Write Pulse)	60		70		80		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	10		10		10		ns
t_{EHDX}		Chip Enable High to Input Transition	10		10		10		ns
t_{WHWH1}		Duration of Program Operation ($\overline{W}$ contr.)	10		10		10		µs
t_{EHEH1}		Duration of Program Operation ($\overline{E}$ contr.)	10		10		10		µs
t_{WHWH2}		Duration of Erase Operation ($\overline{W}$ contr.)	9.5		9.5		9.5		ms
t_{EHEH2}		Duration of Erase Operation ($\overline{E}$ contr.)	9.5		9.5		9.5		ms
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{EHWH}		Chip Enable High to Write Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		20		ns
t_{EHEL}		Chip Enable High to Chip Enable Low	20		20		20		ns
t_{WHGL}		Write Enable High to Output Enable Low	6		6		6		µs
t_{EHGL}		Chip Enable High to Output Enable Low	6		6		6		µs
t_{AVQV}	t_{ACC}	Addess Valid to data Output		90		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid		90		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		30		35		40	ns
t_{EHQZ} (1)		Chip Enable High to Output Hi-Z		30		30		35	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z		30		30		35	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	0		0		0		ns

Note: 1. Sampled only, not 100% tested

Figure 8. Erase Set-up and Erase Verify Commands Waveforms, $\overline{W}$ Controlled

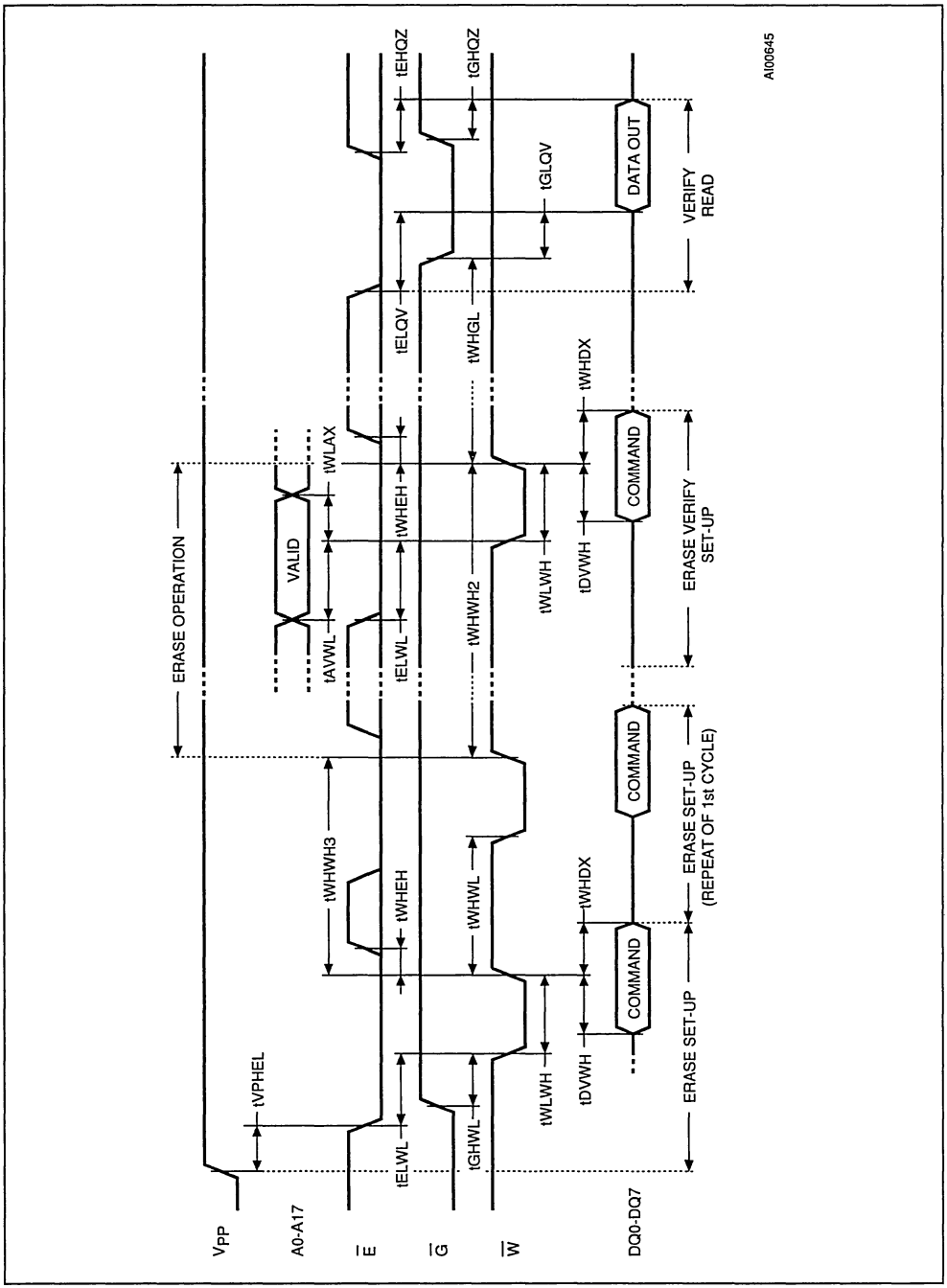


Figure 9. Erase Set-up and Erase Verify Commands Waveforms, $\overline{E}$ Controlled

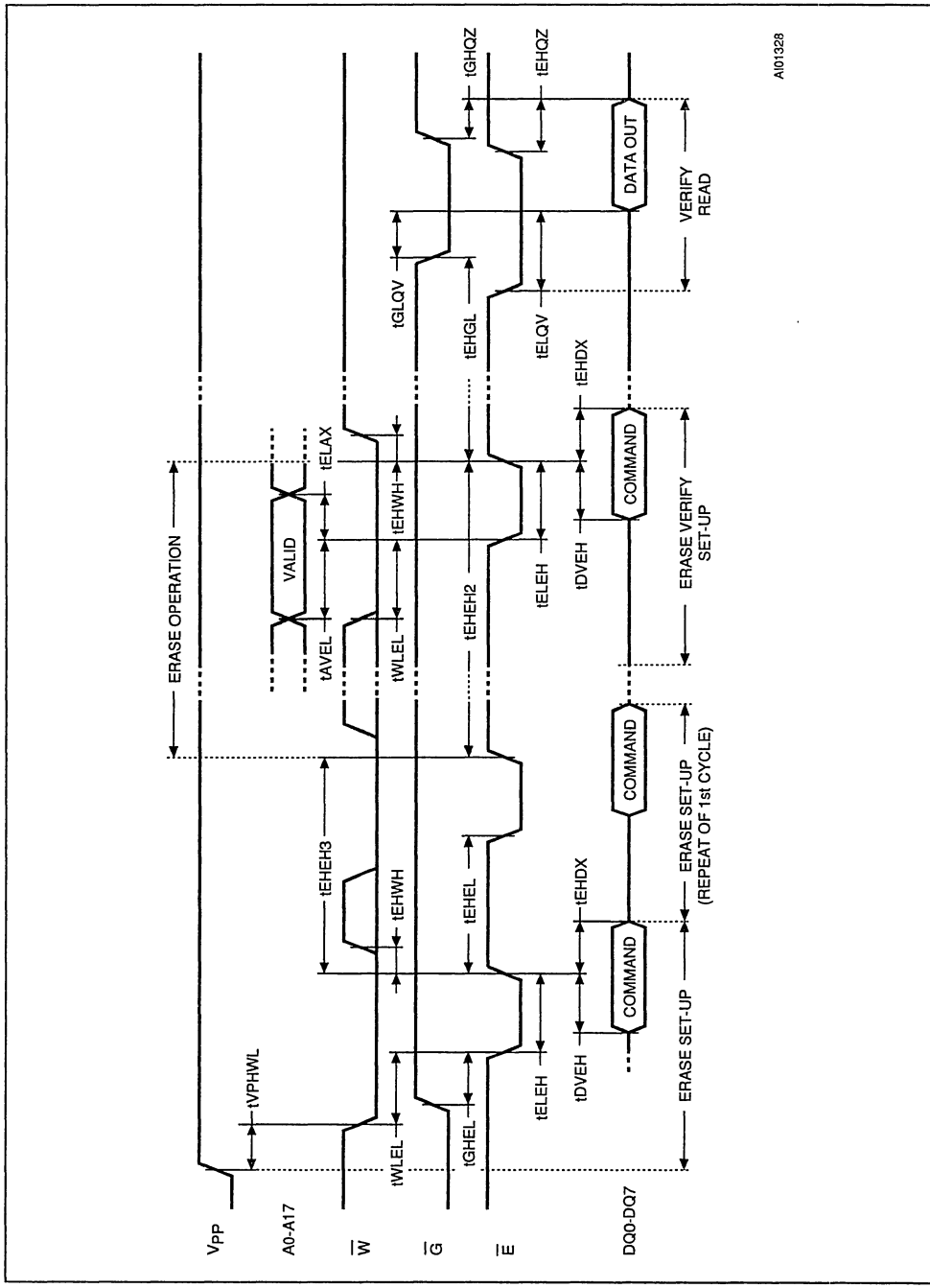


Figure 10. Program Set-up and Program Verify Commands Waveforms - $\overline{W}$ Controlled

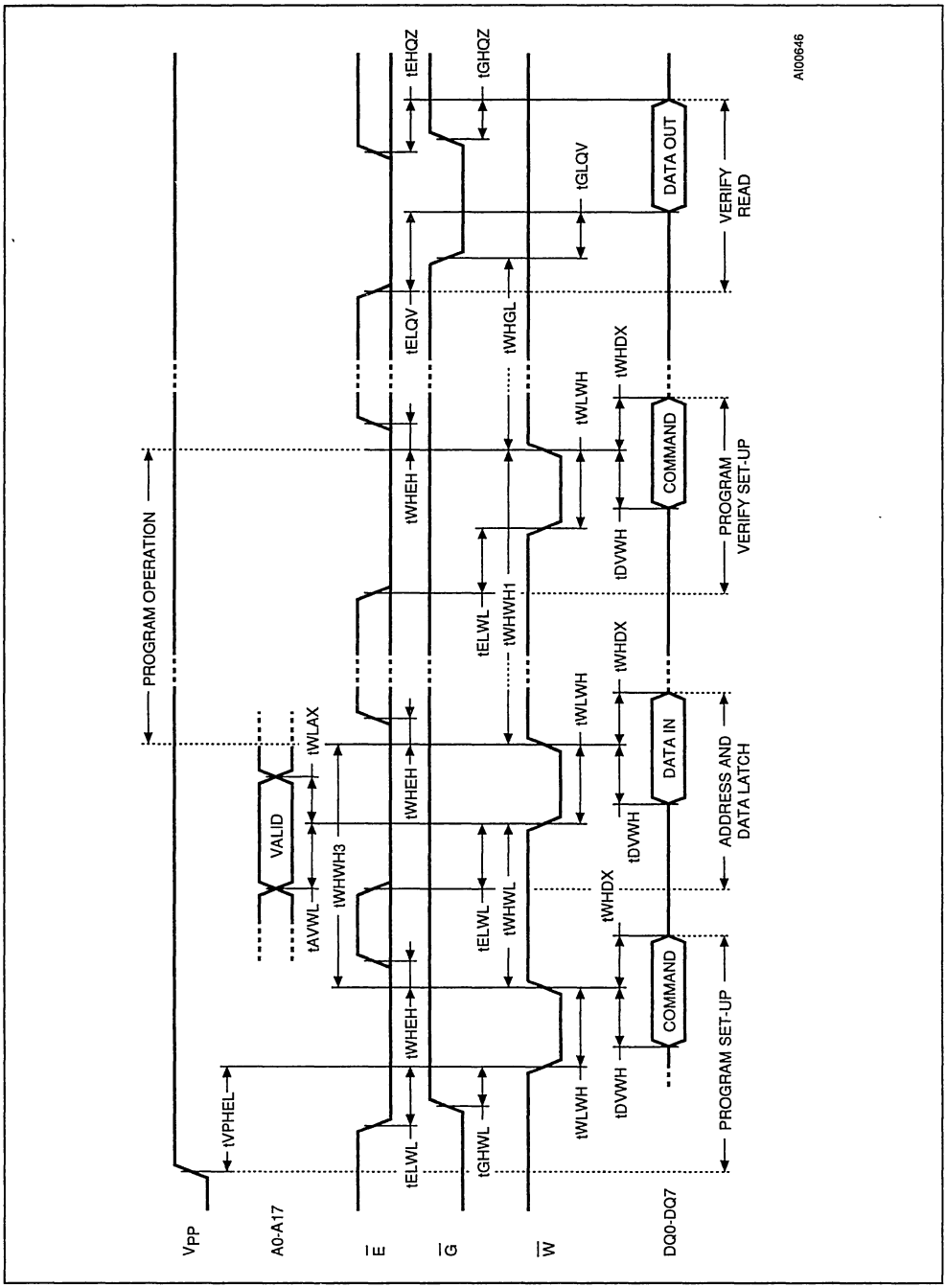


Figure 11. Program Set-up and Program Verify Commands Waveforms - $\overline{E}$ Controlled

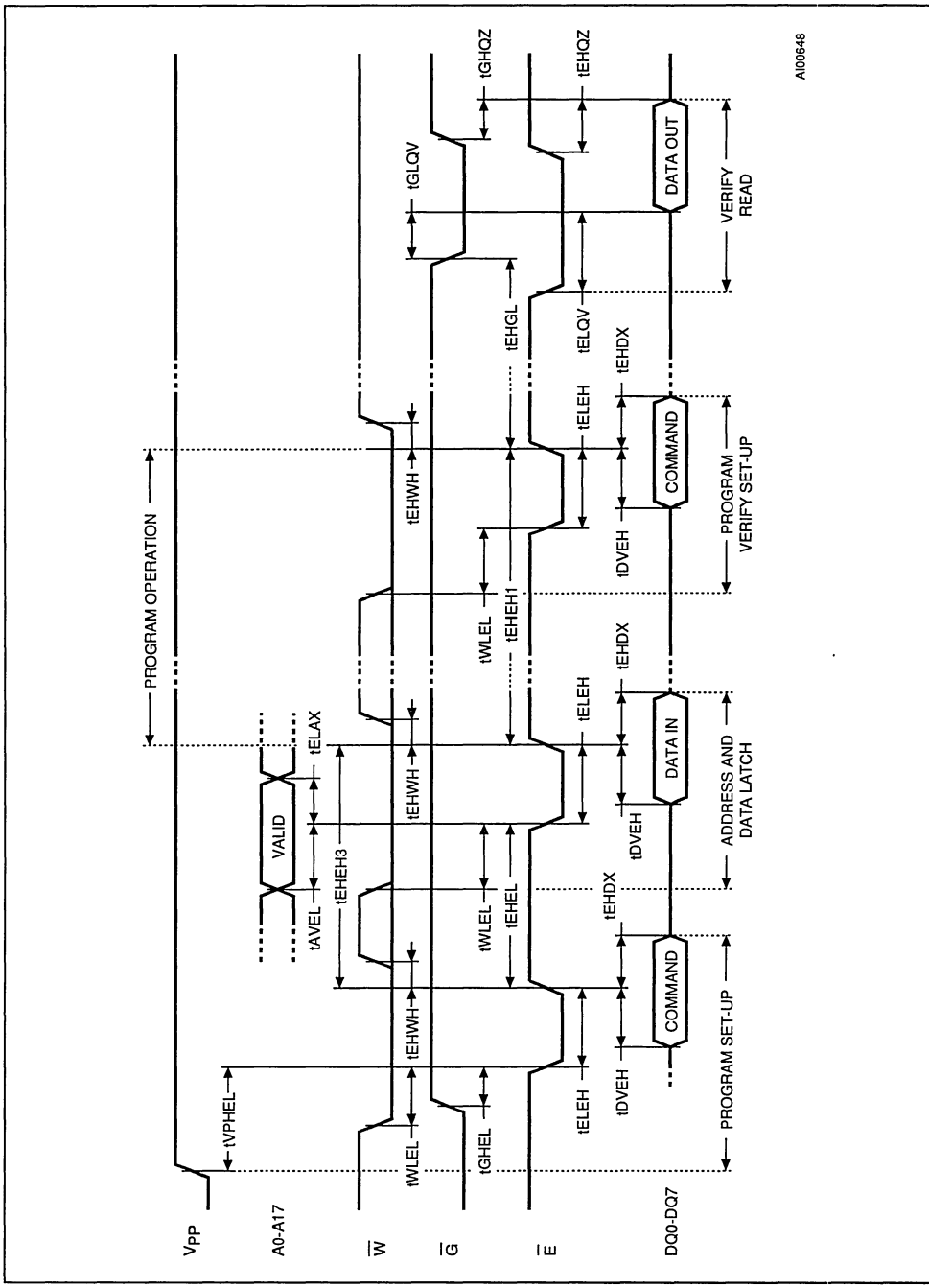


Figure 12. Erasing Flowchart

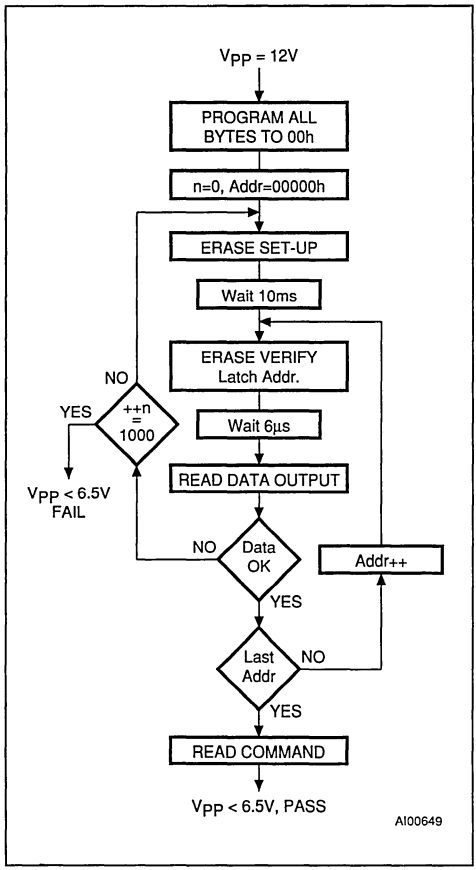
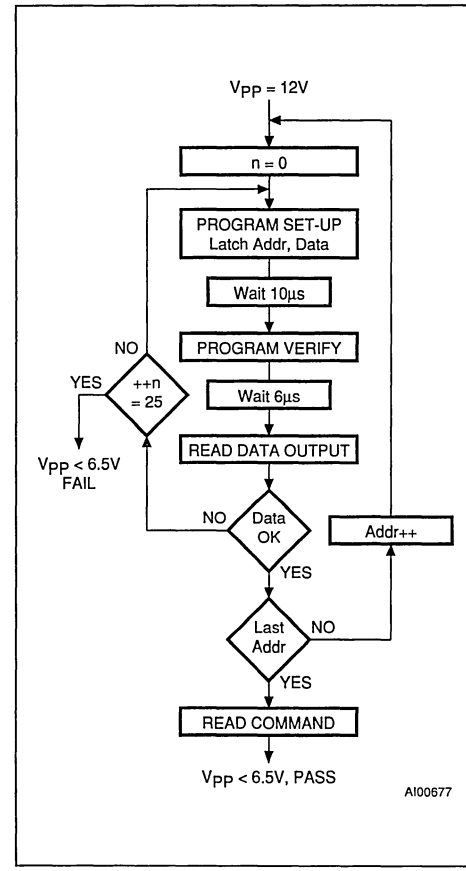


Figure 13. Programming Flowchart



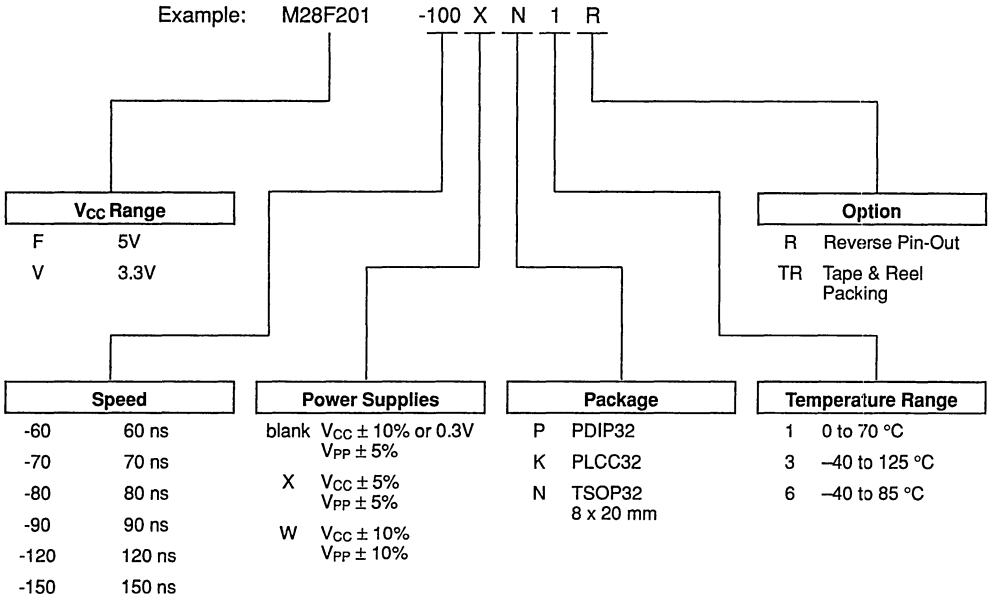
PRESTO F ERASE ALGORITHM

The PRESTO F Erase Algorithm guarantees that the device will be erased in a reliable way. The algorithm first programs all bytes to 00h in order to ensure uniform erasure. The programming follows the Presto F Programming Algorithm (see below). Erase is set-up by writing 20h to the command register, the erasure is started by repeating this write cycle. Erase Verify is set-up by writing 0A0h to the command register together with the address of the byte to be verified. The subsequent read cycle reads the data which is compared to 0FFh. Erase Verify begins at address 0000h and continues to the last address or until the comparison of the data to 0FFh fails. If this occurs, the address of the last byte checked is stored and a new Erase operation performed. Erase Verify then continues from the address of the stored location.

PRESTO F PROGRAM ALGORITHM

The PRESTO F Programming Algorithm applies a series of 10µs programming pulses to a byte until a correct verify occurs. Up to 25 programming operations are allowed for one byte. Program is set-up by writing 40h to the command register, the programming is started after the next write cycle which also latches the address and data to be programmed. Program Verify is set-up by writing 0C0h to the command register, followed by a read cycle and a compare of the data read to the data expected. During Program and Program Verify operations a MARGIN MODE circuit is activated to guarantee that the cell is programmed with a safety margin.

ORDERING INFORMATION SCHEME



Full data on the 3V product M28V201 will be added to this document in the near future.

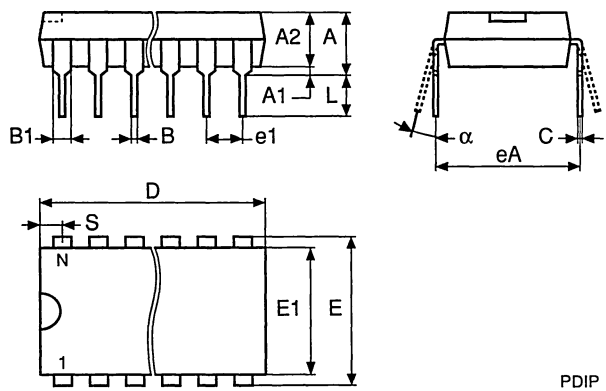
For a list of available options (V_{CC} Range, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP32 - 32 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N	32			32		

PDIP32



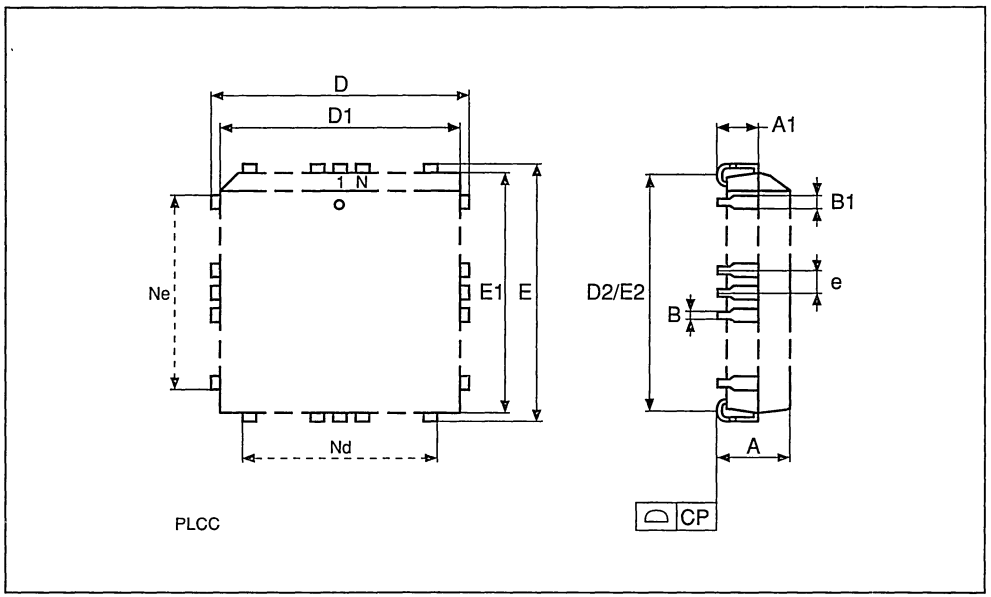
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

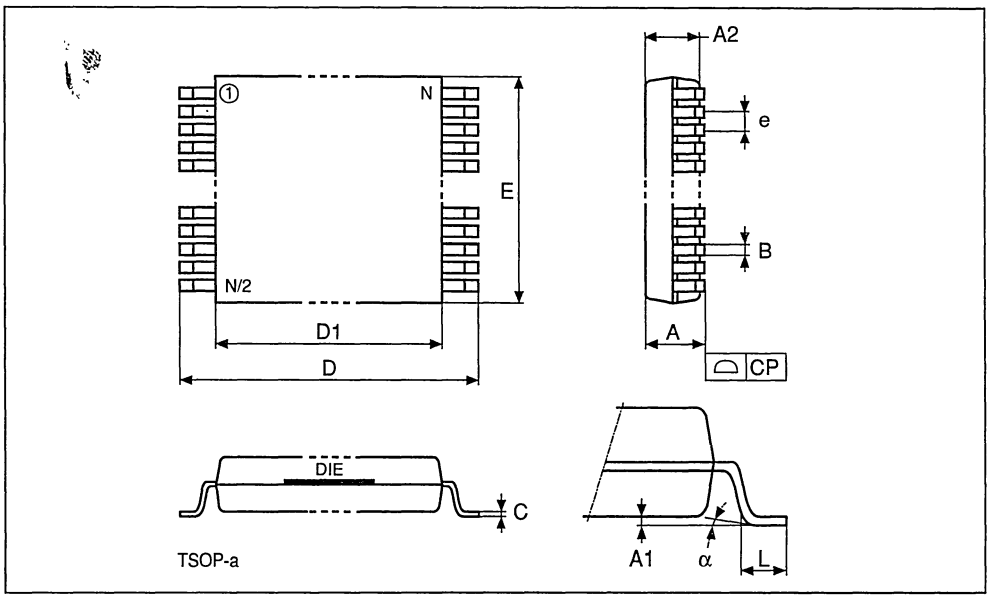


Drawing is out of scale

TSOP32 Normal Pinout - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32



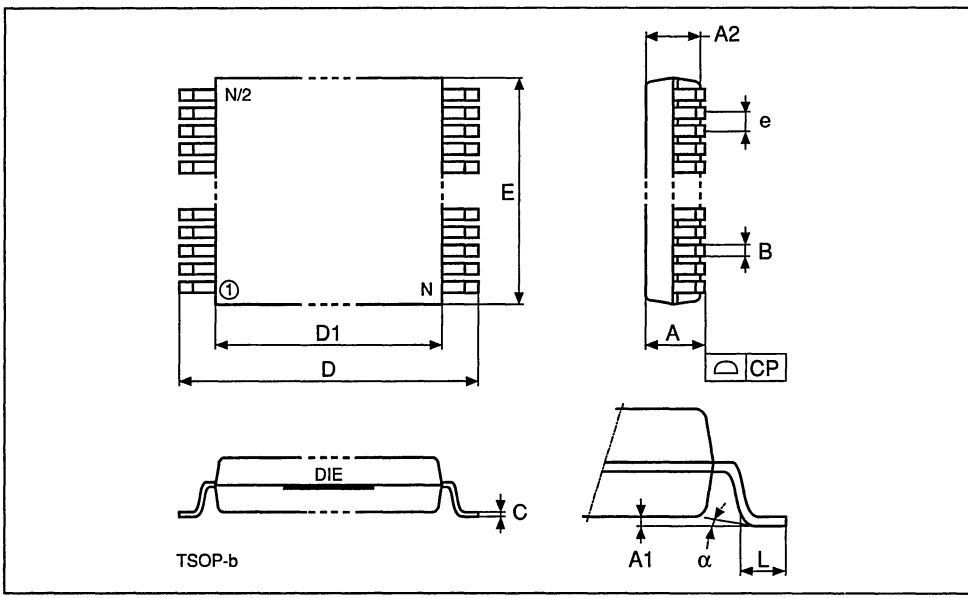
TSOP-a

Drawing is out of scale

TSOP32 Reverse Pinout - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

TSOP32



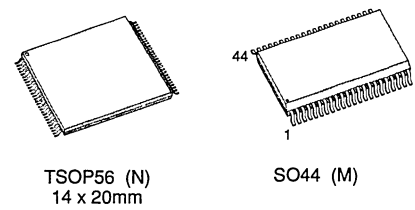
TSOP-b

Drawing is out of scale

2 Megabit (x8 or x16, Block Erase) FLASH MEMORY

PRODUCT PREVIEW

- DUAL x8 and x16 ORGANIZATION
- SMALL SIZE PLASTIC PACKAGES TSOP56 and SO44
- MEMORY ERASE in BLOCKS
  - One 16K Byte or 8K Word Boot Block (top or bottom location) with hardware write and erase protection
  - Two 8K Byte or 4K Word Key Parameter Blocks
  - One 96K Byte or 48K Word Main Block
  - One 128K Byte or 64K Word Main Block
- V_{CC} SUPPLY VOLTAGE
  - 5V ± 10% for M28F210, F220 versions
  - 3.3V ± 0.3V for M28V210, V220 versions
- 12V ± 10% or 5% PROGRAMMING VOLTAGE
- 100,000 PROGRAM/ERASE CYCLES
- PROGRAM/ERASE CONTROLLER
- AUTOMATIC STATIC MODE
- LOW POWER CONSUMPTION
  - 2mA Typical in Static Operation
  - 60µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
  - 20/25mA Typical Operating Consumption (Byte/Word)
- HIGH SPEED ACCESS TIMES
  - 60-70ns for M28F210, F220 versions
- EXTENDED TEMPERATURE RANGES



TSOP56 (N)
14 x 20mm

SO44 (M)

Figure 1. Logic Diagram

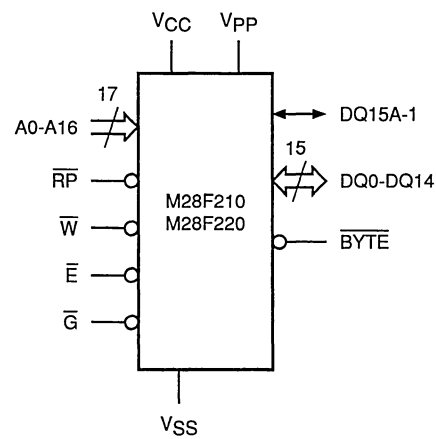
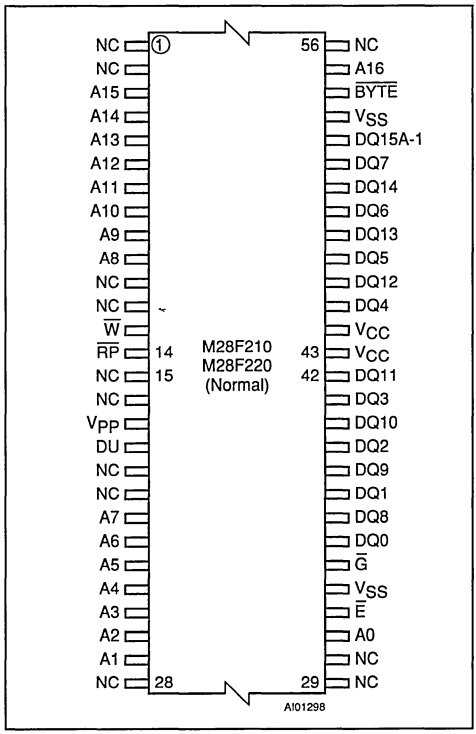


Table 1. Signal Names

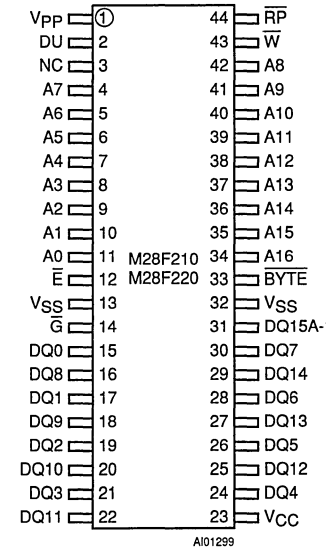
A0-A16	Address Inputs
DQ0-DQ7	Data Input / Outputs
DQ8-DQ14	Data Input / Outputs
DQ15A-1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{BYTE}$	Byte/Word Organization
$\overline{RP}$	Reset/Power Down/Boot Block Unlock
V_{PP}	Program & Erase Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. TSOP Pin Connections



Warning: NC = No Connections, DU = Don't Use

Figure 2B. SO Pin Connections



Warning: NC = No Connections, DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9} (2)	A9 Voltage		–0.6 to 13.5	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
V_{RP} (2)	$\overline{RP}$ Voltage		–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 7V allowed for less than 20ns.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{BYTE}$	DQ0 - DQ7	DQ8 - DQ14	DQ15A-1
Read Word	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Data Output	Data Output	Data Output
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Hi-Z	Address Input
Write Word	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Data Input	Data Input	Data Input
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data Input	Hi-Z	Address Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	X	Hi-Z	Hi-Z	Hi-Z
Power Down	X	X	X	V_{IL}	X	Hi-Z	Hi-Z	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}

Table 4. Electronic Signature

Organi-sation	Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{BYTE}$	A0	A9	A1-A8 & A10-A16	DQ0 - DQ7	DQ8 - DQ14	DQ15 A-1
Word-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{ID}	Don't Care	20h	00h	0
	Device Code	M28F210	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0E0h	00h	0
		M28F220	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0E6h	00h	0
		M28V210	V_{IL}	VIL	V_{IH}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0E1h	00h	0
		M28V220	V_{IL}	VIL	V_{IH}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0E7h	00h	0
Byte-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h	Hi-Z	Don't Care
	Device Code	M28F210	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{ID}	Don't Care	0E0h	Hi-Z	Don't Care
		M28F220	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{ID}	Don't Care	0E6h	Hi-Z	Don't Care
		M28V210	V_{IL}	VIL	V_{IH}	V_{IL}	V_{IH}	V_{ID}	Don't Care	0E1h	Hi-Z	Don't Care
		M28V220	V_{IL}	VIL	V_{IH}	V_{IL}	V_{IH}	V_{ID}	Don't Care	0E7h	Hi-Z	Don't Care

Note: $\overline{RP}$ = V_{IH}

DESCRIPTION

The M28F210 and M28F220 FLASH MEMORIES are non-volatile memories that may be erased electrically at the block level and programmed by byte or word. The interface is directly compatible with most microprocessors. SO44 and TSOP56 packages are used.

Organization

The organization, as 256K x 8 or 128K x 16, is selectable by an external $\overline{BYTE}$ signal. When $\overline{BYTE}$ is Low and the x8 organization is selected, the Data Input/Output signal DQ15 acts as Address line A-1 and selects the lower or upper byte of the memory word for output on DQ0-DQ7, DQ8-DQ14 remain high impedance. When $\overline{BYTE}$ is High the memory uses the Address inputs A0-A16 and the Data Input/Outputs DQ0-DQ15. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down/Boot block unlock, tri-level input, places the memory in deep power down, normal operation or enables programming and erasure of the Boot block.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data (4)	Operation	Address	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Signature
EE	Erase	2	Write	X	20h	Write	Block Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSR or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of Read cycle can occur after one command cycle.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.
4. When word organization is used, upper byte is don't care for command input.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Array

Blocks

Erasure of the memories is in blocks. There are 5 blocks in the memory address space, one Boot Block of 16K Bytes or 8K Words, two 'Key Parameter Blocks' of 8K Bytes or 4K Words, one 'Main Block' of 96K Bytes or 48K Words, and one 'Main Block' of 128K Bytes or 64K Words. The M28F210 memory has the Boot Block at the top of the memory address space (1FFFFh) and the M28F220 locates the Boot Block starting at the bottom (00000h). Erasure of each block takes typically 1 second and each block can be programmed and erased over 100,000 cycles.

The Boot Block is hardware protected from accidental programming or erasure depending on the $\overline{RP}$ signal. Program/Erase commands in the Boot Block are executed only when $\overline{RP}$ is at 12V. Block erasure may be suspended while data is read from other blocks of the memory, then resumed.

Bus Operations

Six operations can be performed by the appropriate bus cycles, Read Byte or Word from the Array, Read Electronic Signature, Output Disable, Standby, Power Down and Write the Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor the memory's status. When power is first applied, on exit from power down or if V_{CC}

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits b4 or b5 for Program or Erase Success
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction P/ECS and ESS bits are set to '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte or word.
			'0'	Program Success	
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction has been executed.
			'0'	V_{PP} OK	
	2	Reserved			
	1	Reserved			
	0	Reserved			

Notes: Logic level '1' is High, '0' is Low.

falls below V_{LKO}, the command interface is reset to Read Memory Array.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte or word program and block erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte or word programming takes typically 9µs, block erase typically 1 second. Erasure of a memory block may be suspended in order to read data from another block and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation.

Power Saving

The M28F210 and M28F220 have a number of power saving features. Following a Read access the memory enters a static mode in which the supply current is typically 2mA. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down ($\overline{RP}$) signals are at V_{CC}, when the supply current drops to typically 60µA. A deep power down mode is enabled when the Reset/Power Down ($\overline{RP}$) signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 300ns maximum, with instructions to the C.I. recognised after only 210ns.

Table 8. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

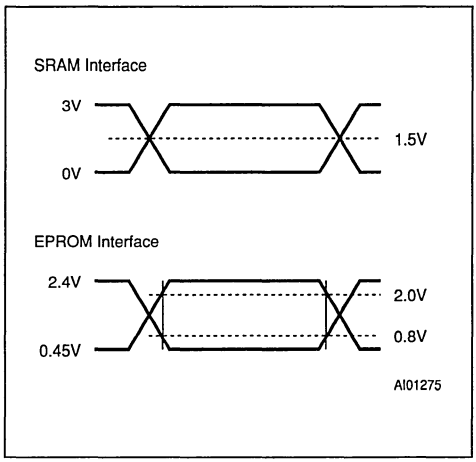


Figure 4. AC Testing Load Circuit

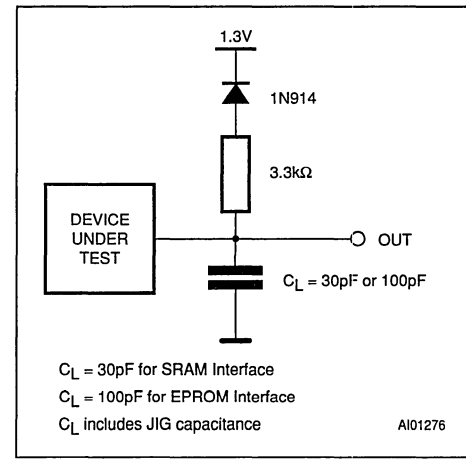


Table 9. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

DEVICE OPERATION

Signal Descriptions

A0-A16 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

A9 Address Input is also used for the Electronic Signature Operation. When A9 is raised to 12V the Electronic Signature may be read. The A0 signal is used to read two words or bytes, when A0 is Low the Manufacturer code is read and when A0 is High the Device code is read. When $\overline{BYTE}$ is Low DQ0-DQ7 output the codes and DQ8-DQ15 are don't care, when $\overline{BYTE}$ is High DQ0-DQ7 output the codes and DQ8-DQ15 output 00h.

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte or the lower byte of a word to be programmed or a command to the C.I., are latched when both Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output from the memory Array, the Electronic Signature or Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

DQ8-DQ14 and DQ15A-1 Data Input/Outputs. These input/outputs are used in the word-wide organization. When $\overline{BYTE}$ is High for the most significant byte of the input or output, functioning as described for DQ0-DQ7 above. When $\overline{BYTE}$ is Low, DQ8-DQ14 are high impedance, DQ15A-1 is the Address A-1 input.

Table 10. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V±10% or 5V±5%; V_{PP} = 12V±5% or 12V±10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read Byte-wide) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 10MHz		50	mA
I_{CC} (1, 3)	Supply Current (Read Word-wide) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 10MHz		55	mA
I_{CC} (1, 3)	Supply Current (Read Byte-wide) CMOS	$\overline{E} = V_{SS}$, $\overline{G} = V_{SS}$, f = 10MHz		45	mA
	Supply Current (Read Word-wide) CMOS	$\overline{E} = V_{SS}$, $\overline{G} = V_{SS}$, f = 10MHz		50	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$, $\overline{BYTE} = V_{CC} \pm 0.2V$ or V_{SS}		100	µA
I_{CC2} (3)	Supply Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{CC3}	Supply Current (Program Byte-wide)	Byte program in progress		50	mA
	Supply Current (Program Word-wide)	Word program in progress		60	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Current (Read or Standby)	$V_{PP} \ge V_{CC}$		200	µA
I_{PP1}	Program Leakage Current (Read or Standby)	$V_{PP} \le V_{CC}$		±10	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program Byte-wide)	Byte program in progress		30	mA
I_{PP3}	Program Current (Program Word-wide)	Word program in progress		40	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations) 5% range		11.4	12.6	V
	Program Voltage (Program or Erase operations) 10% range		10.8	13.2	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 2mA typical in static operation.
2. Current increases to I_{CC} + I_{CCS} during a read operation.
3. CMOS levels V_{CC} ± 0.2V and V_{SS} ± 0.2V. TTL levels V_{IH} and V_{IL}.

Table 11A. Read AC Characteristics
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	Test Condition	M28F210 / 220						Unit
				-60		-70		-80		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
				SRAM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	60		70		80		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		60		70		80	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		300		300		300	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		60		70		80	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		30		35		40	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		20		25		30	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		20		25		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Table 11B. Read AC Characteristics
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	Test Condition	M28F210 / 220						Unit
				-100		-120		-150		
				V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
				EPROM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		300		300		300	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		50		55	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		35		35		35	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		35		35		35	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 5. Read Mode AC Waveforms

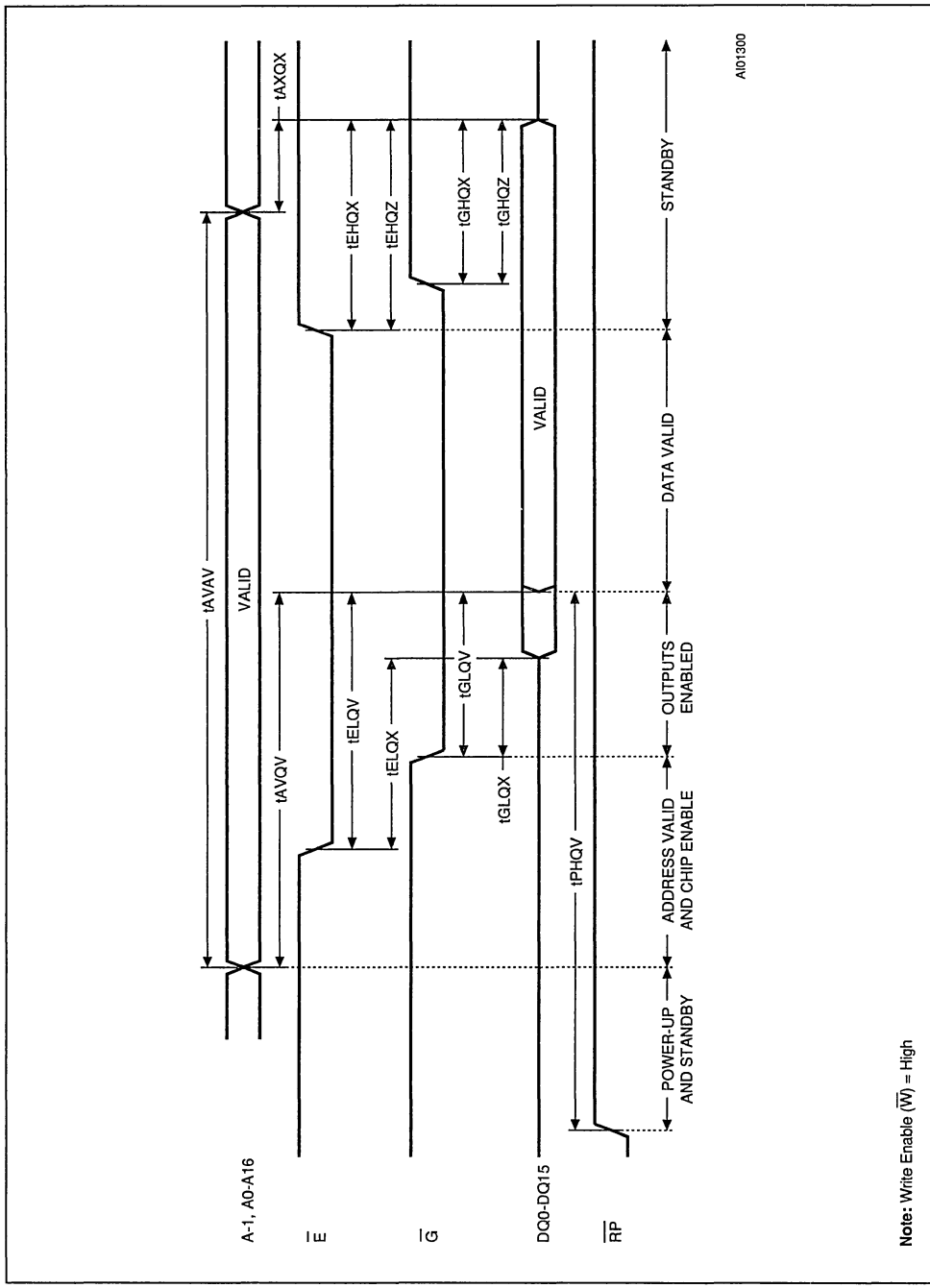


Table 12A. $\overline{BYTE}$ AC Characteristics (1)
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Parameter	Test Condition	M28F210 / 220						Unit
			-60		-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{ELBL}	Chip Enable Low to BYTE Low			5		5		5	ns
t_{ELBH}	Chip Enable Low to BYTE High			5		5		5	ns
t_{BLQV}	$\overline{BYTE}$ Low to Output Valid			60		70		80	ns
t_{BHQV}	$\overline{BYTE}$ High to Output Valid			60		70		80	ns
t_{BLQZ}	$\overline{BYTE}$ Low to Output Hi-Z			20		25		30	ns

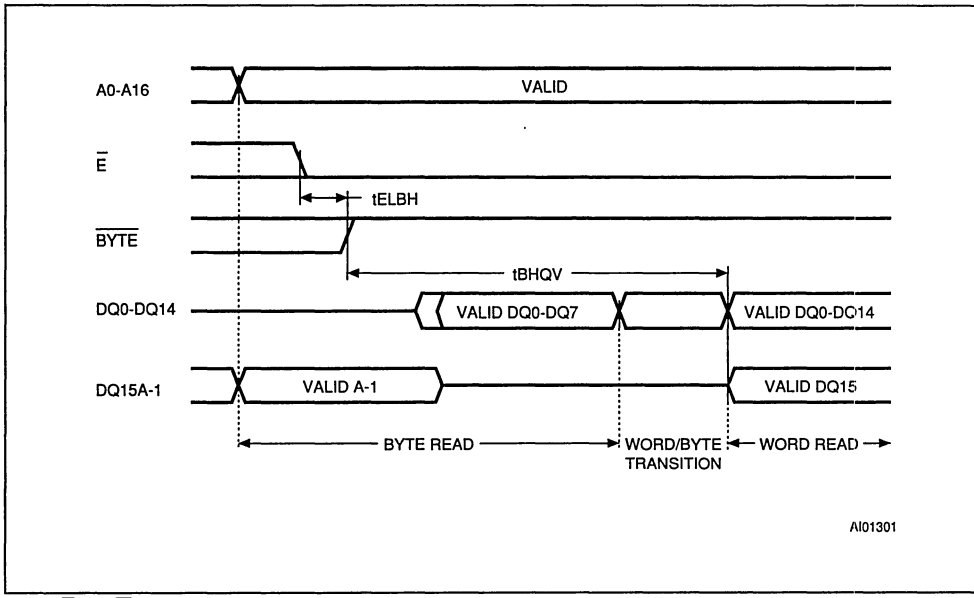
Note: 1. Sampled only, not 100% tested.

Table 12B. $\overline{BYTE}$ AC Characteristics (1)
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Parameter	Test Condition	M28F210 / 220						Unit
			-100		-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{ELBL}	Chip Enable Low to BYTE Low			5		5		5	ns
t_{ELBH}	Chip Enable Low to BYTE High			5		5		5	ns
t_{BLQV}	$\overline{BYTE}$ Low to Output Valid			100		120		150	ns
t_{BHQV}	$\overline{BYTE}$ High to Output Valid			100		120		150	ns
t_{BLQZ}	$\overline{BYTE}$ Low to Output Hi-Z			30		30		30	ns

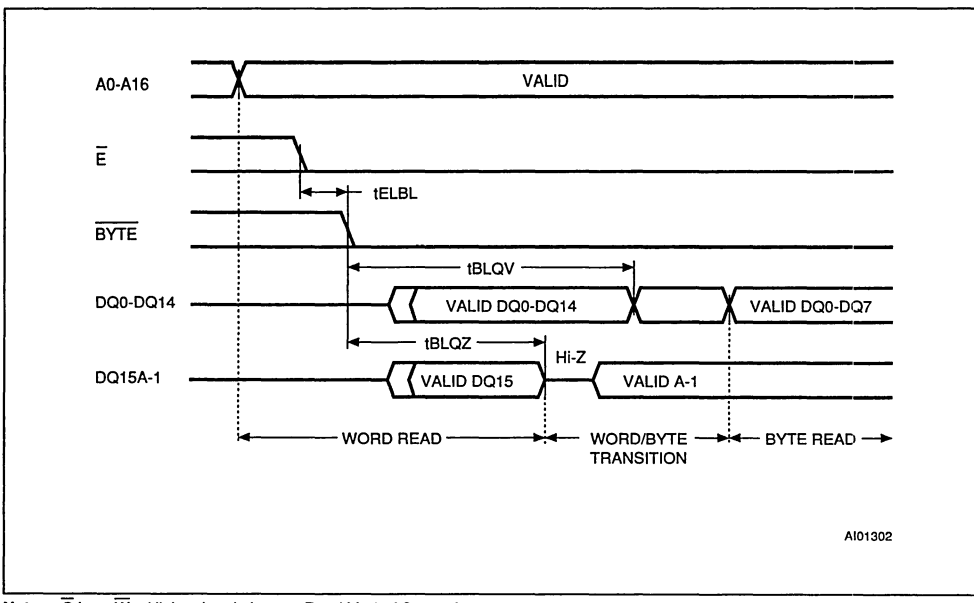
Note: 1. Sampled only, not 100% tested.

Figure 6. $\overline{BYTE}$ Mode AC Waveforms, $\overline{BYTE}$ Low to High



Note: $\overline{G}$ Low, $\overline{W}$ = High, other timings as Read Mode AC waveforms.

Figure 7. $\overline{BYTE}$ Mode AC Waveforms, $\overline{BYTE}$ High to Low



Note: $\overline{G}$ Low, $\overline{W}$ = High, other timings as Read Mode AC waveforms.

Table 13A. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	M28F210 / 220						Unit
			-60		-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	60		70		80		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	10		20		30		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	50		50		50		ns
t_{PHHWH}	t_{PHS}	Power Down VHH (Boot Block Unlock) to Write Enable High	100		100		100		ns
t_{VPHWH}	t_{VPS}	V_{PP} High to Write Enable High	100		100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		10		ns
t_{WHQV1} (1, 2)		Write Enable High to Output Valid (Word/Byte Program)	6		6		6		µs
t_{WHQV2} (1, 2)		Write Enable High to Output Valid (Boot Block Erase)	0.3		0.3		0.3		sec
t_{WHQV3} (1)		Write Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		0.3		sec
t_{WHQV4} (1)		Write Enable High to Output Valid (Main Block Erase)	0.6		0.6		0.6		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		100		100		100	ns

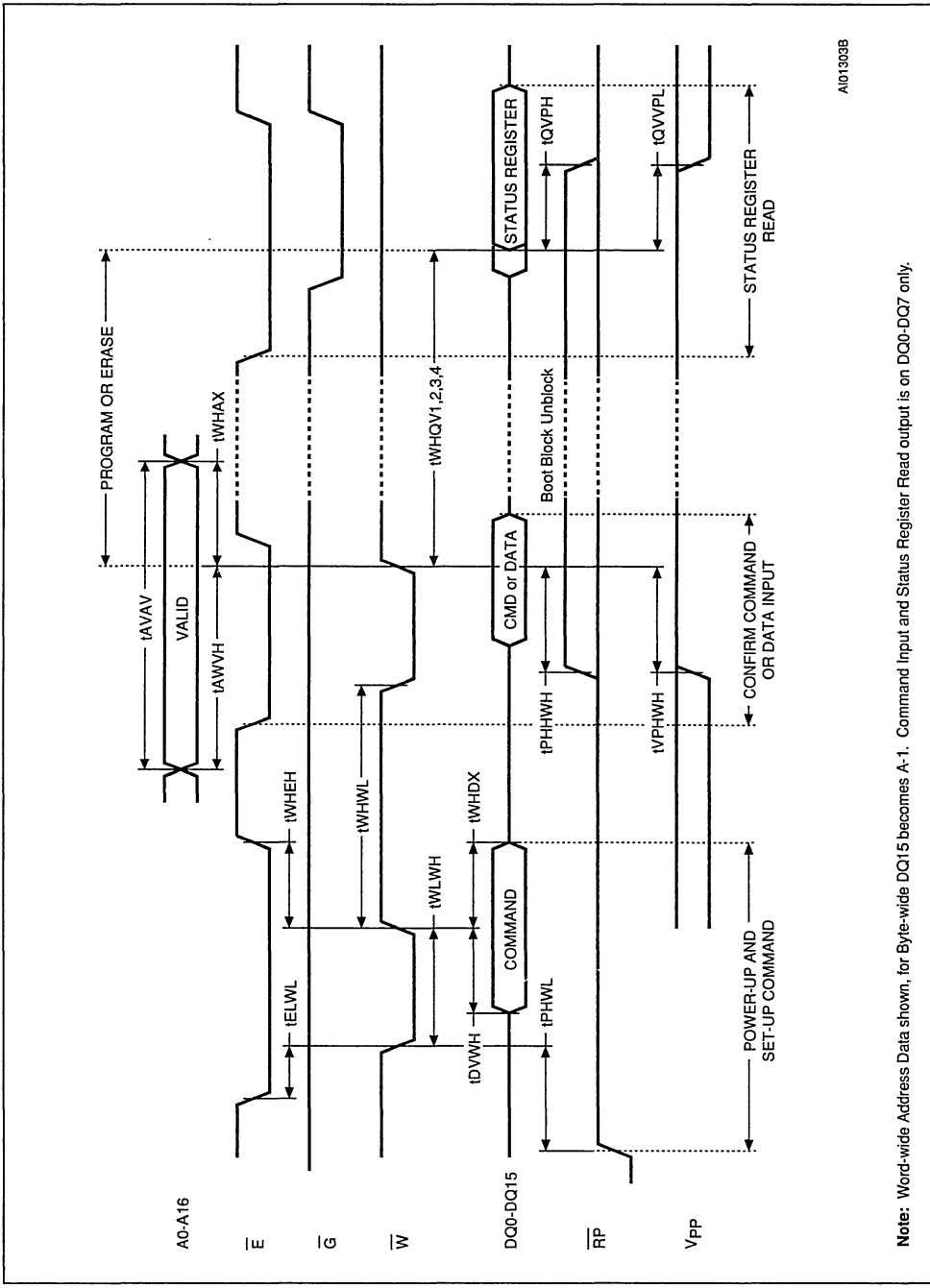
Notes: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Table 13B. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	M28F210 / 220						Unit
			-100		-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	60		70		90		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	60		60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	40		50		60		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	60		60		60		ns
t_{PHHWH}	t_{PHS}	Power Down VHH (Boot Block Unlock) to Write Enable High	100		100		100		ns
t_{VPHWH}	t_{VPS}	V_{PP} High to Write Enable High	100		100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		10		ns
t_{WHQV1} (1, 2)		Write Enable High to Output Valid (Word/Byte Program)	7		7		7		µs
t_{WHQV2} (1, 2)		Write Enable High to Output Valid (Boot Block Erase)	0.4		0.4		0.4		sec
t_{WHQV3} (1)		Write Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		0.4		sec
t_{WHQV4} (1)		Write Enable High to Output Valid (Main Block Erase)	0.7		0.7		0.7		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		100		100		100	ns

Notes: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Figure 8. Program & Erase AC Waveforms, $\overline{W}$ Controlled



Note: Word-wide Address Data shown, for Byte-wide DQ15 becomes A-1. Command Input and Status Register Read output is on DQ0-DQ7 only.

Table 14A. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	M28F210 / 220						Unit
			-60		-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	60		70		80		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	50		50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	10		20		30		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	50		50		50		ns
t_{PHHEH}	t_{PHS}	Power Down VHH (Boot Block Unlock) to Chip Enable High	100		100		100		ns
t_{VPHEH}	t_{VPS}	V_{PP} High to Chip Enable High	100		100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		10		ns
t_{EHQV1} (1, 2)		Chip Enable High to Output Valid (Word/Byte Program)	6		6		6		µs
t_{EHQV2} (1, 2)		Chip Enable High to Output Valid (Boot Block Erase)	0.3		0.3		0.3		sec
t_{EHQV3} (1)		Chip Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		0.3		sec
t_{EHQV4} (1)		Chip Enable High to Output Valid (Main Block Erase)	0.6		0.6		0.6		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		100		100		100	ns

Note: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Table 14B. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	M28F210 / 220						Unit
			-100		-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	60		70		90		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	60		60		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	40		50		60		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	60		60		60		ns
t_{PHHEH}	t_{PHS}	Power Down VHH (Boot Block Unlock) to Chip Enable High	100		100		100		ns
t_{VPHEH}	t_{VPS}	V_{PP} High to Chip Enable High	100		100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		10		ns
t_{EHQV1} (1, 2)		Chip Enable High to Output Valid (Word/Byte Program)	7		7		7		µs
t_{EHQV2} (1, 2)		Chip Enable High to Output Valid (Boot Block Erase)	0.4		0.4		0.4		sec
t_{EHQV3} (1)		Chip Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		0.4		sec
t_{EHQV4} (1)		Chip Enable High to Output Valid (Main Block Erase)	0.7		0.7		0.7		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		100		100		100	ns

Note: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Figure 9. Program & Erase AC Waveforms, $\overline{E}$ Controlled

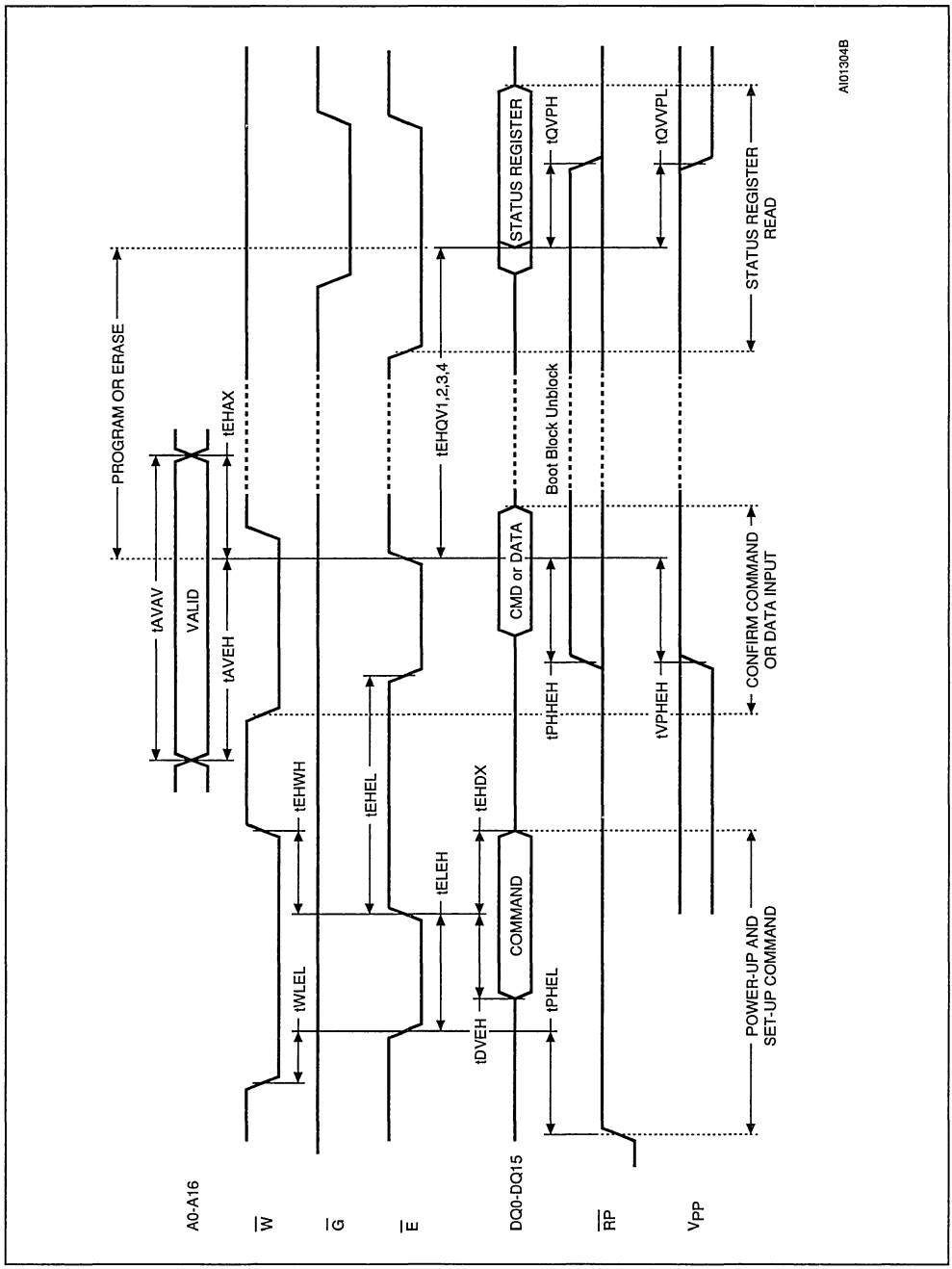


Table 15. Word/Byte Program, Erase Times
(T_A = 0 to 70°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	Test Conditions	M28F210 / 220			Unit
		Min	Typ	Max	
Main Block Program (Byte)	V_{PP} = 12V ±5%		1.2	4.2	sec
Main Block Program (Word)	V_{PP} = 12V ±5%		0.6	2.1	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±5%		1	7	sec
Main Block Erase	V_{PP} = 12V ±5%		2.4	14	sec
Main Block Program (Byte)	V_{PP} = 12V ±10%		6	20	sec
Main Block Program (Word)	V_{PP} = 12V ±10%		3	10	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±10%		5.8	40	sec
Main Block Erase	V_{PP} = 12V ±10%		14	60	sec

DEVICE OPERATION (cont'd)

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This is a tri-level input which locks the Boot Block from programming and erasure, and allows the memory to be put in deep power down.

When $\overline{RP}$ is High (up to 6.5V maximum) the Boot Block is locked and cannot be programmed or erased. When $\overline{RP}$ is above 11.4V the Boot Block is unlocked for programming or erasure. With $\overline{RP}$ Low the memory is in deep power down, and if $\overline{RP}$ is within V_{SS}+0.2V the lowest supply current is absorbed.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. It controls writing to the Command Register and Input Address and Data latches. Both Addresses and Data Inputs are latched on the rising edge of $\overline{W}$.

$\overline{BYTE}$ Byte/Word Organization Select. This input selects either byte-wide or word-wide organization of the memory. When $\overline{BYTE}$ is Low the memory is organized x8 or byte-wide and data input/output uses DQ0-DQ7 while A-1 acts as the additional, LSB, of the memory address that multiplexes the upper or lower byte. In the byte-wide organization DQ8-DQ14 are high impedance. When $\overline{BYTE}$ is High the memory is organized x16 and data input/output uses DQ0-DQ15 with the memory addressed by A0-A16.

V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{PP} ±10% tolerance option is provided for application requiring maximum 100 write and erase cycles.

V_{CC} Supply Voltage. It is the main circuit supply.

V_{SS} Ground. It is the reference for all voltage measurements.

Memory Blocks

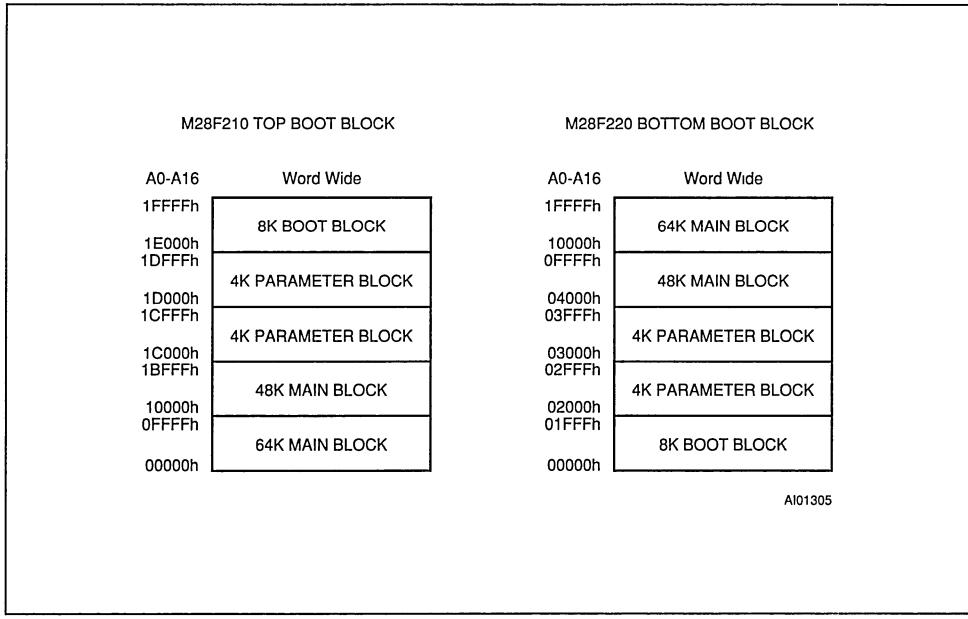
The memory blocks of the M28F210 and M28F220 are shown in Figure 10. The difference between the two products is simply an inversion of the block map to position the Boot Block at the top or bottom of the memory. The selection of the Boot Block at the top or bottom of the memory depends on the microprocessor needs.

Each block of the memory can be erased separately, but only by one block at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another block and then resumed.

Programming and erasure of the memory is disabled when the program supply is at V_{PPL}. For successful programming and erasure the program supply must be at V_{PPH}.

The Boot Block provides additional hardware security by use of the $\overline{RP}$ signal which must be at V_{HH} before any program or erase operation will be executed by the P/E.C. on the Boot Block.

Figure 10. Memory Map, Word-wide Addresses



Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down, and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. A read operation will output either a byte or a word depending on the $\overline{BYTE}$ signal level. When $\overline{BYTE}$ is Low the output byte is on DQ0-DQ7, DQ8-DQ14 are Hi-Z and A-1 is an additional address input. When $\overline{BYTE}$ is High the output word is on DQ0-DQ15.

The data read depends on the previous command written to the memory (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$. As for the Read operation, when $\overline{BYTE}$ is Low a byte is input, DQ8-DQ14 are 'don't care' and A-1 is an additional address. When $\overline{BYTE}$ is High a word is input.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is low. The power consumption is reduced to the Power Down level, and Outputs are in high impedance, independant of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memories, the manufacturer code for SGS-THOMSON is 20h, and the device codes are 0E0h for the M28F210 (Top Boot Block) and 0E6h for the M28F220 (Bottom Boot Block). These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product.

The Electronic Signature is output by a Read Array operation when the voltage applied to A9 is at V_{ID}, the manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored. The codes are output on DQ0-DQ7. When the $\overline{BYTE}$ signal is High the outputs DQ8-DQ15 output 00h, when Low these outputs are high impedance and Address input A-1 is ignored.

The Electronic Signature can also be read, without raising A9 to V_{ID}, after giving the memory the instruction RSIG (see below).

Instructions and Commands

The memories include a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from 1 to 3 operations, the first of which is always a write operation and is followed by either a further write operation to confirm the first command or a read operation(s) to output data.

A Status Register indicates the P/E.C. status Ready or Busy, the suspend/in-progress status of erase operations, the failure/success of erase and program operations and the low/correct value of the Program Supply voltage V_{PP}.

The P/E.C. automatically sets bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The register can be read by the Read Status Register (RSR) instruction and cleared by the Clear Status Register (CLRS) instruction. The meaning of the bits b3 to b7 is shown in Table 7. Bits b0 to b2 are reserved for future use (and should be masked out during status checks).

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read the addressed memory array content and output a byte or word depending on the level of the $\overline{BYTE}$ input.

Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent Read operations output the contents of the Status Register. The contents of the status register are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the Status Register.

Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h followed by two read operations to output the manufacturer and device codes. The manufacturer code, 20h, is output when the address line A0 is Low, and the device code, 0E0h for the M28F210 or 0E6h for the M28F220, when A0 is High.

Erase (EE) instruction. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second command is the Erase Confirm command 0D0h. During the input of the second command an address of the block to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 and b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the RSR (Read Status Register) and ES (Erase Suspend) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it has completed. After completion the Status Register bit b5 returns '1' if there has been an Erase Failure because erasure has not been verified even after the maximum number of erase cycles have been executed. Status Register bit b3 returns '1' if V_{PP} does not remain at V_{PPH} level when the erasure is attempted and/or proceeding.

V_{PP} must be at V_{PPH} when erasing, erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register (CLRS).

The Boot Block can only be erased when $\overline{RP}$ is also at V_{HH}.

Program (PG) instruction. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or 10h). A second write operation latches the Address and the Data to be written and starts the P/E.C. Read operations output the status register after the programming has started.

Memory programming is only made by writing '0' in place of '1' in a byte or word.

DEVICE OPERATION (cont'd)

During the execution of the programming by the P/E.C., the memory accepts only the RSR (Read Status Register) instruction. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status Register bit b3 returns a '1' if V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming.

V_{PP} must be at V_{PPH} when programming, programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect. Then after having cleared the Status Register (CLRS), the memory must be erased and re-programmed.

The Boot Block can only be programmed when $\overline{RP}$ is at V_{HH}.

Clear Status Register (CLRS) instruction. The Clear Status Register uses a single write operation which clears bits b3, b4 and b5, if latched to '1' by the P/E.C., to '0'. Its use is necessary before any new operation when an error has been detected.

Erase Suspend (ES) instruction. The Erase operation may be suspended by this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates whether the erase has actually been suspended, b6 = '1', or whether the P/E.C. cycle was the last and the erase is completed, b6 = '0'.

During the suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Read operations initially output the status register while erase is suspended but, following a Read instruction, data from other blocks of the memory can be read. V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or the $\overline{RP}$ signal goes Low while erase is suspended then erase is aborted while bits b5 and b3 of the status register are set. Erase operation must be repeated after having cleared the status register, to be certain to erase the block.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 0D0h. The status register bit b6 is cleared when erasure resumes. Read operations output the status register after the erase is resumed.

The suggested flow charts for programs that use the programming, erasure and erase suspend/resume features of the memories are shown in Figure 11 to Figure 13.

Programming. The memory can be programmed byte-by-byte (or word-by-word in x16 organization). The Program Supply voltage V_{PP} must be applied before program instructions are given, and if the programming is in the Boot Block, $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Program Supply voltage may be applied continuously during programming. The program sequence is started by writing a Program Set-up command (40h) to the Command Interface, this is followed by writing the address and data byte or word to the memory. The Program/Erase Controller automatically starts and performs the programming after the second write operation, providing that the V_{PP} voltage (and $\overline{RP}$ voltage if programming the Boot Block) are correct. During the programming the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that programming is completed.

A full status check can be made after each byte/word or after a sequence of data has been programmed. The status check is made on bit b3 for any possible V_{PP} error and on bit b4 for any possible programming error.

Erase. The memory can be erased by blocks. The Program Supply voltage V_{PP} must be applied before the Erase instruction is given, and if the Erase is of the Boot Block $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Erase sequence is started by writing an Erase Set-up command (20h) to the Command Interface, this is followed by an address in the block to be erased and the Erase Confirm command (0D0h). The Program/Erase Controller automatically starts and performs the block erase, providing the V_{PP} voltage (and the $\overline{RP}$ voltage if the erase is of the Boot Block) is correct. During the erase the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that erase is completed.

A full status check can be made after the block erase by checking bit b3 for any possible V_{PP} error, bits b5 and b6 for any command sequence errors (erase suspended) and bit b5 alone for an erase error.

Reset. Note that after any program or erase instruction has completed with an error indication or after any V_{PP} transitions down to V_{PPL} the Command Interface must be reset by a Clear Status Register Instruction before data can be accessed.

Automatic Power Saving

The M28F210 and M28F220 memories place themselves in a lower power state when not being accessed. Following a Read operation, after a delay equal to the memory access time, the Supply Current is reduced from a typical read current of 25mA (CMOS inputs, word wide organization) to less than 2mA.

Power Down

The memories provide a power down control input $\overline{RP}$. When this signal is taken to below V_{SS} + 0.2V all internal circuits are switched off and the supply current drops to typically 0.2µA and the program current to typically 0.1µA. If $\overline{RP}$ is taken low during a memory read operation then the memory is deselected and the outputs become high impedance. If $\overline{RP}$ is taken low during a program or erase sequence then it is aborted and the memory content is no longer valid.

Recovery from deep power down requires 300ns to a memory read operation, or 210ns to a command write. On return from power down the status register is cleared to 00h.

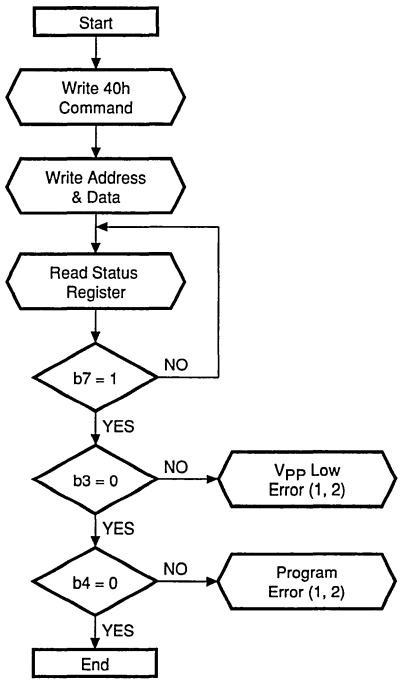
Power Up

The Supply voltage V_{CC} and the Program Supply voltage V_{PP} can be applied in any order. The memory Command Interface is reset on power up to Read Memory Array, but a negative transition of Chip Enable $\overline{E}$ or a change of the addresses is required to ensure valid data outputs. Care must be taken to avoid writes to the memory when V_{CC} is above V_{LKO} and V_{PP} powers up first. Writes can be inhibited by driving either $\overline{E}$ or $\overline{W}$ to V_{IH}. The memory is disabled until $\overline{RP}$ is up to V_{IH}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} and V_{PP} rails decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{PP} program and erase currents required.

Figure 11. Program Flow-chart and Pseudo Code



PG instruction:
– write 40h command
– write Address & Data
(memory enters read status state after the PG instruction)

do:
– read status register
(E or G must be toggled)

while b7 = 1

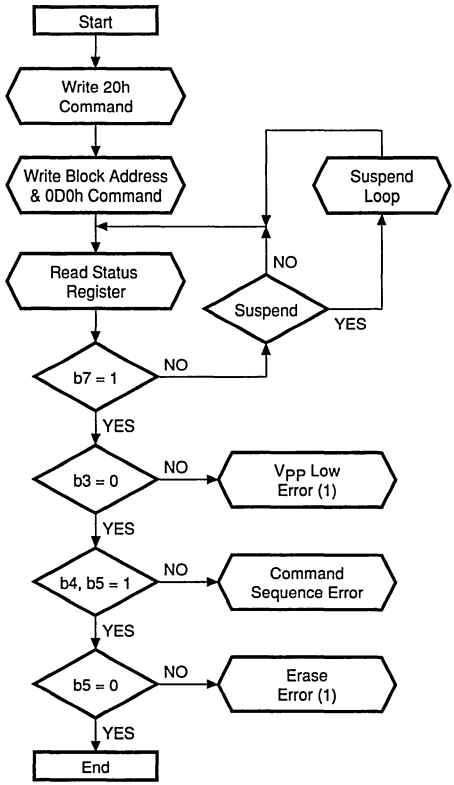
If b3 = 0, V_{PP} low error:
– error handler

If b4 = 0, Program error:
– error handler

AI01278

Notes: 1. Status check of b3 (V_{PP} Low) and b4 (Program Error) can be made after each byte/word programming or after a sequence.
2. If a V_{PP} Low or Program Erase is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 12. Erase Flow-chart and Pseudo Code



EE instruction:
– write 20h command
– write Block Address (A12-A17) & command 0D0h
(memory enters read status state after the EE instruction)

do:
– read status register ($\overline{E}$ or $\overline{G}$ must be toggled)
if EE instruction given execute suspend erase loop

while b7 = 1

If b3 = 0, V_{PP} low error:
– error handler

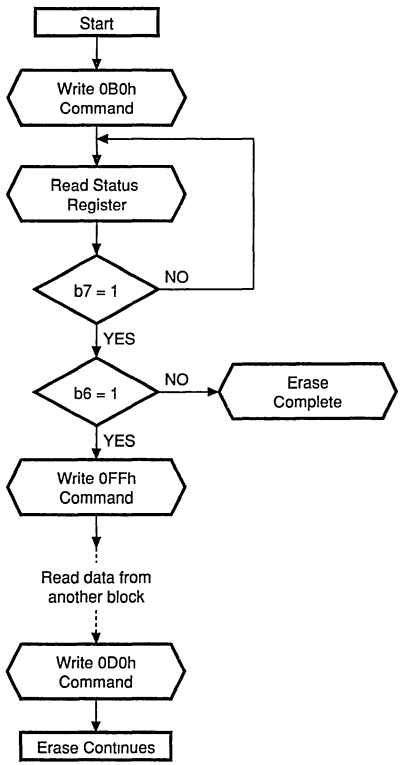
If b4, b5 = 0, Command Sequence error:
– error handler

If b5 = 0, Erase error:
– error handler

AI01279

Note: 1. If V_{PP} Low or Erase Error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 13. Erase Suspend & Resume Flow-chart and Pseudo Code



ES instruction:
– write 0B0h command
(memory enters read register state after the ES instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

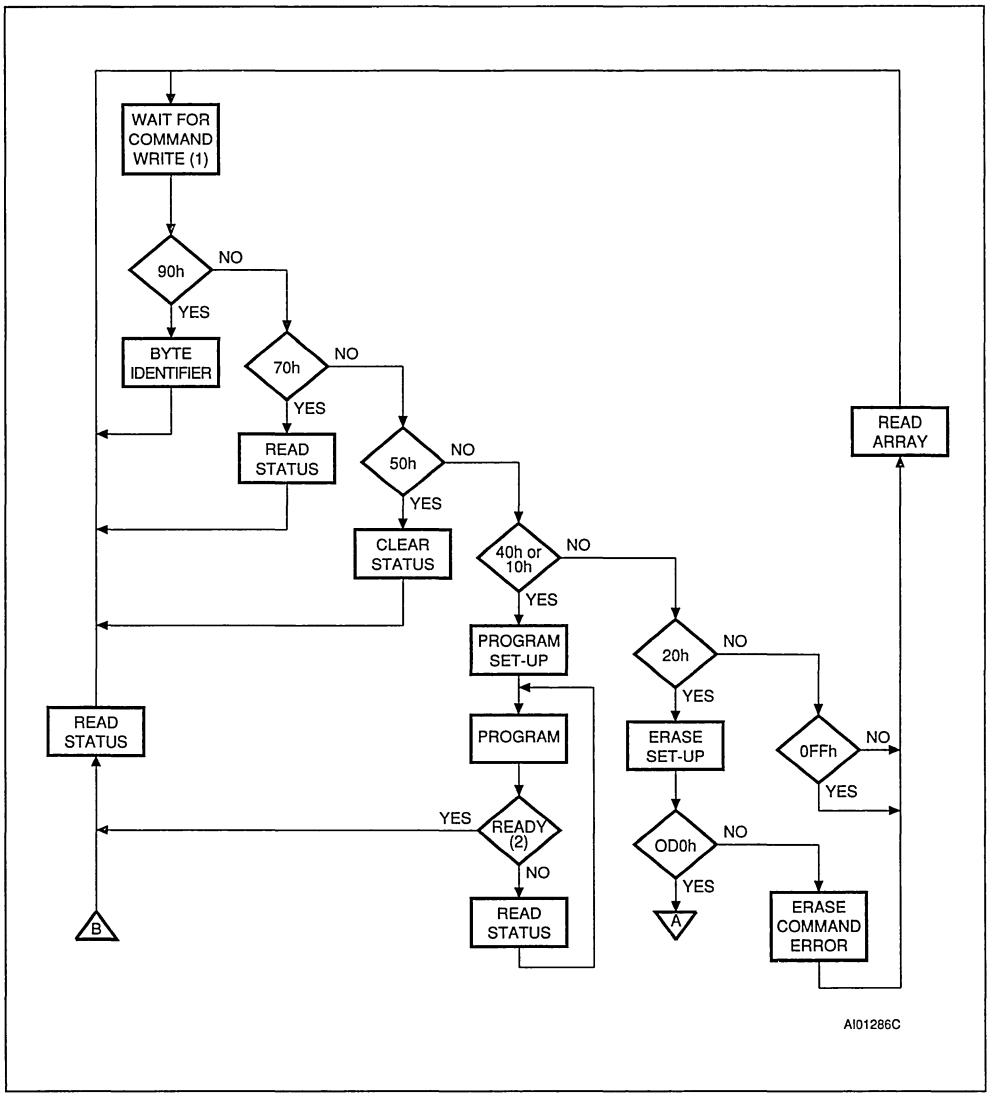
If b6 = 0, Erase completed
(at this point the memory wich accept only the RD or ER instruction)

RD instruction:
– write 0FFh command
– one o more data reads from another block

ER instruction:
– write 0D0h command to resume erasure

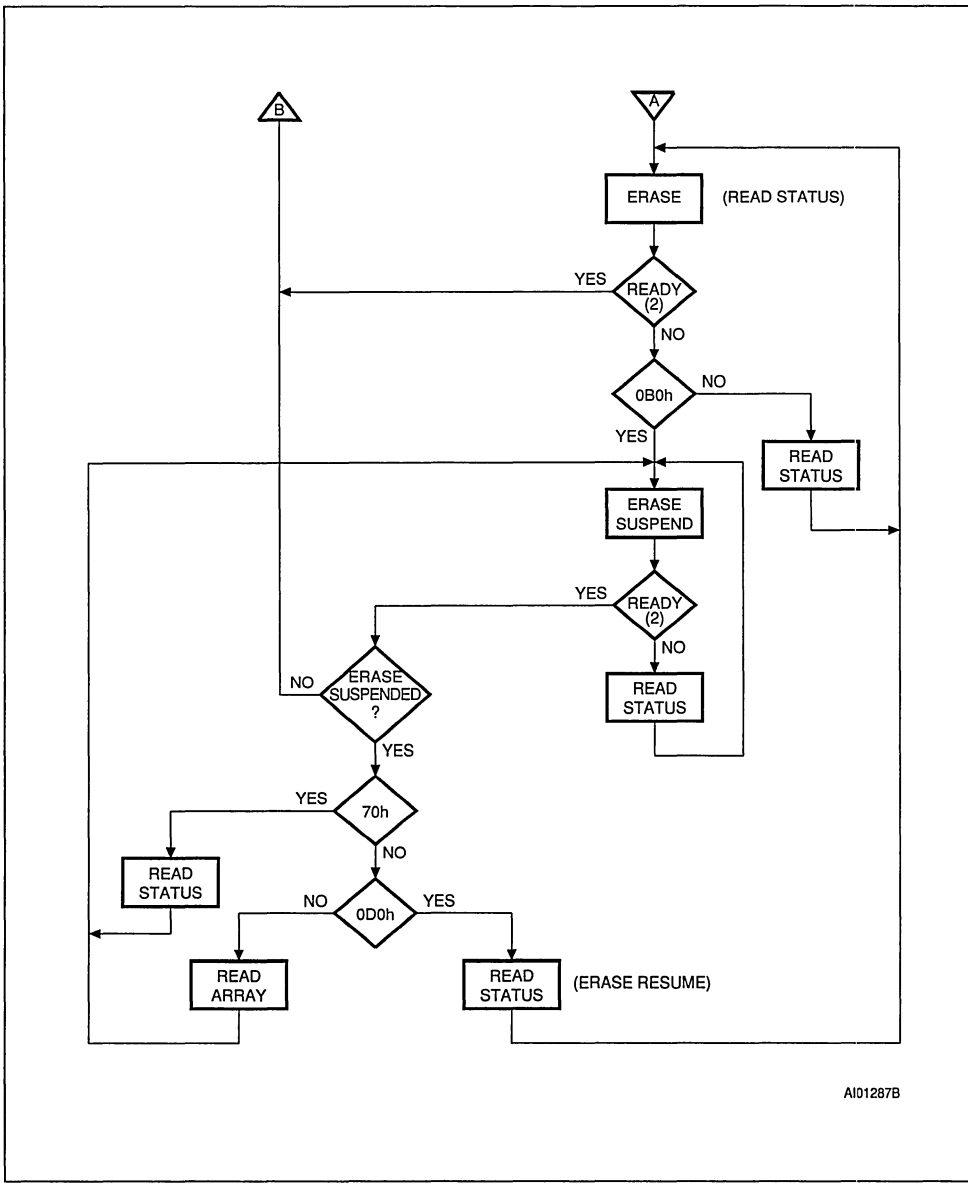
AI01280

Figure 14. Command Interface and Program Erase Controller Flow-diagram (a)



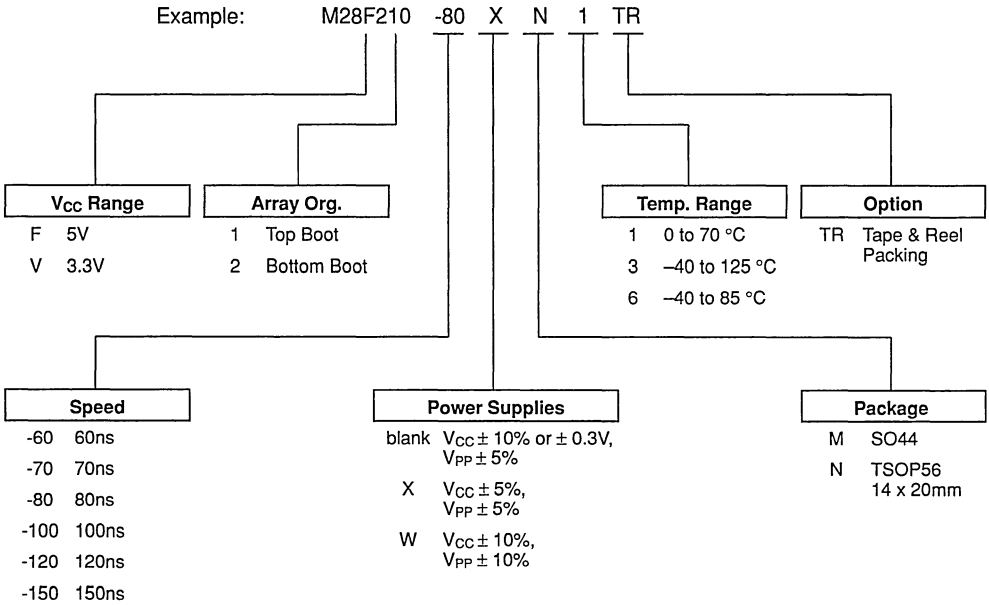
Notes: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 15. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME



Full data on the 3V products, M28V210 and M28V220, will be added to this document in the near future.

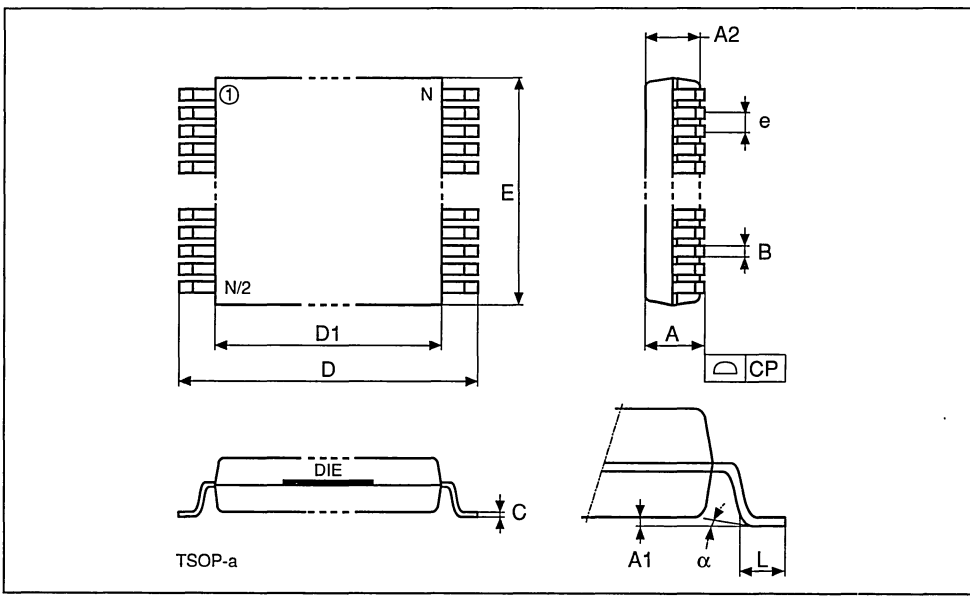
For a list of available options (V_{CC} Range, Array Organization, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		13.90	14.10		0.547	0.555
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		56			56	
CP			0.10			0.004

TSOP56



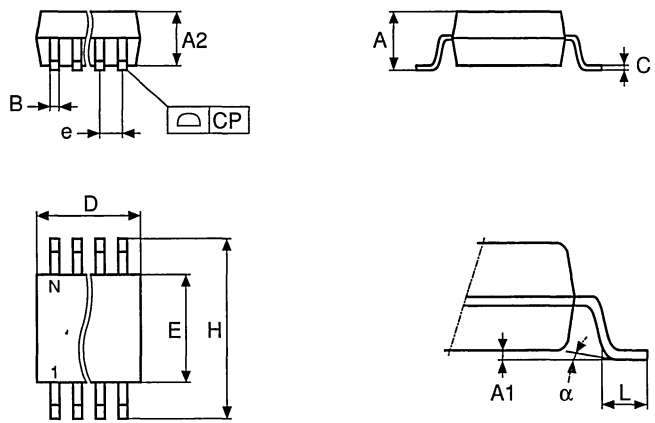
TSOP-a

Drawing is out of scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27	–	–	0.050	–	–
H		15.90	16.10		0.626	0.634
L	0.80	–	–	0.031	–	–
α	3°	–	–	3°	–	–
N		44			44	
CP			0.10			0.004

SO44



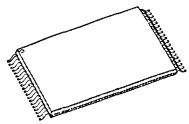
SO-b

Drawing is out of scale

2 Megabit (x 8, Block Erase) FLASH MEMORY

PRODUCT PREVIEW

- SMALL SIZE PLASTIC PACKAGE TSOP40
- MEMORY ERASE in BLOCKS
  - One 16K Byte Boot Block (top or bottom location) with hardware write and erase protection
  - Two 8K Byte Key Parameter Blocks
  - One 96K Byte Main Block
  - One 128K Byte Main Block
- V_{CC} SUPPLY VOLTAGE
  - 5V ± 10% for M28F211, F221 versions
  - 3.3V ± 0.3V for M28V211, V221 versions
- 12V ± 10% or 5% PROGRAMMING VOLTAGE
- 100,000 PROGRAM/ERASE CYCLES
- PROGRAM/ERASE CONTROLLER
- AUTOMATIC STATIC MODE
- LOW POWER CONSUMPTION
  - 1mA Typical in Static Operation
  - 60µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
  - 20/25mA Typical Operating Consumption
- HIGH SPEED ACCESS TIMES
  - 60-70ns for M28F211, F221 versions
- EXTENDED TEMPERATURE RANGES



TSOP40 (N)
10 x 20mm

Figure 1. Logic Diagram

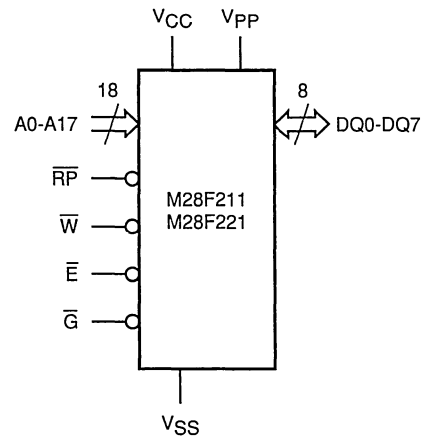


Table 1. Signal Names

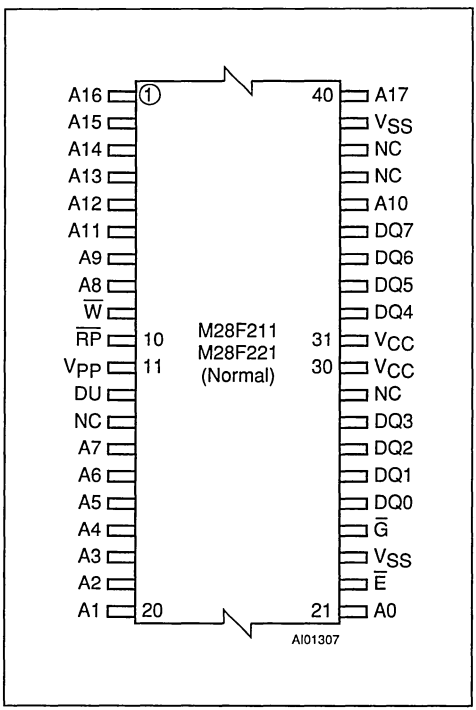
A0-A17	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power Down/Boot Block Unlock
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9} (2)	A9 Voltage		–0.6 to 13.5	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
V_{RP} (2)	$\overline{RP}$ Voltage		–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 7V allowed for less than 20ns.

Figure 2. TSOP Pin Connections



Warning: NC = No Connections, DU = Don't Use

DESCRIPTION

The M28F211 and M28F221 FLASH MEMORIES are non-volatile memories that may be erased electrically at the block level and programmed by byte. The interface is directly compatible with most microprocessors. TSOP40 (10 x 20mm) package in used.

Organization

The M28F211 and M28F221 are organized as 256K x 8. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down/Boot block unlock, tri-level input, places the memory in deep power down, normal operation or enables programming and erasure of the Boot block.

Blocks

Erasure of the memories is in blocks. There are 5 blocks in the memory address space, one Boot Block of 16K Bytes, two 'Key Parameter Blocks' of 8K Bytes, one 'Main Block' of 96K Bytes, and one 'Main Block' of 128K Bytes. The M28F211 memory has the Boot Block at the top of the memory address space (3FFFFh) and the M28F221 locates the Boot Block starting at the bottom (00000h). Erasure of each block takes typically 1 second and each block can be programmed and erased over 100,000 cycles.

The Boot Block is hardware protected from accidental programming or erasure depending on the $\overline{RP}$ signal. Program/Erase commands in the Boot Block are executed only when $\overline{RP}$ is at 12V.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	DQ0 - DQ7
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data Output
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	Hi-Z
Power Down	X	X	X	V_{IL}	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}

Table 4. Electronic Signature

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A9	A1-A8 & A10-A16	DQ0 - DQ7
Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	Don't Care	20h
Device Code	M28F211	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0E4h
	M28F221	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0E8h
	M28V211	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0E5h
	M28V221	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0E9h

Note: $\overline{RP}$ = V_{IH}

Block erasure may be suspended while data is read from other blocks of the memory, then resumed.

Bus Operations

Six operations can be performed by the appropriate bus cycles, Read Byte from the Array, Read Electronic Signature, Output Disable, Standby, Power Down and Write the Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor the memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and block erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte programming takes typically 9µs, block erase typically 1 second. Erasure of a memory block may be suspended in order to read data from another block and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation.

Power Saving

The M28F211 and M28F221 have a number of power saving features. Following a Read access the memory enters a static mode in which the supply current is typically 1mA. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down ($\overline{RP}$) signals are at V_{CC}, when the supply current drops to typically 60µA. A deep power down mode is enabled when the Reset/Power Down ($\overline{RP}$) signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 300ns maximum, with instructions to the C.I. recognised after only 210ns.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address (1)	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Signature
EE	Erase	2	Write	X	20h	Write	Block Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSR or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of Read cycle can occur after one command cycle.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Array

DEVICE OPERATION

Signal Descriptions

A0-A16 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

A9 Address Input is also used for the Electronic Signature Operation. When A9 is raised to 12V the Electronic Signature may be read. The A0 signal is used to read two bytes, when A0 is Low the Manufacturer code is read and when A0 is High the Device code is read.

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte to be programmed or a command to the C.I., are latched when both Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output from the memory Array, the Electronic Signature or Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits b4 or b5 for Program or Erase Success
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction P/ECS and ESS bits are set to '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte.
			'0'	Program Success	
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction has been executed.
			'0'	V_{PP} OK	
	2	Reserved			
	1	Reserved			
	0	Reserved			

Notes: Logic level '1' is High, '0' is Low.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This is a tri-level input which locks the Boot Block from programming and erasure, and allows the memory to be put in deep power down.

When $\overline{RP}$ is High (up to 6.5V maximum) the Boot Block is locked and cannot be programmed or erased. When $\overline{RP}$ is above 11.4V the Boot Block is unlocked for programming or erasure. With $\overline{RP}$ Low the memory is in deep power down, and if $\overline{RP}$ is within V_{SS}+0.2V the lowest supply current is absorbed.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. It controls writing to the Command Register and Input Address and Data latches. Both Addresses and Data Inputs are latched on the rising edge of $\overline{W}$.

V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{PP} ±10% tolerance option is provided for application requiring maximum 100 write and erase cycles.

V_{CC} Supply Voltage. It is the main circuit supply.

V_{SS} Ground. It is the reference for all voltage measurements.

Table 8. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

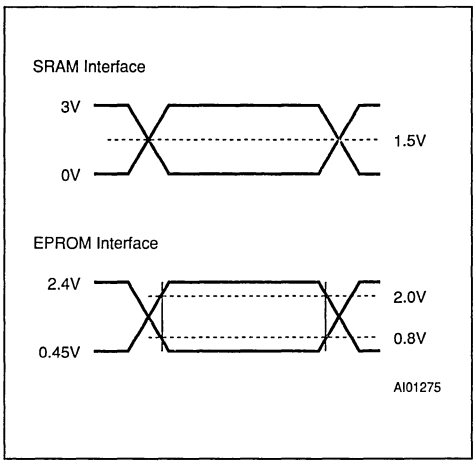


Figure 4. AC Testing Load Circuit

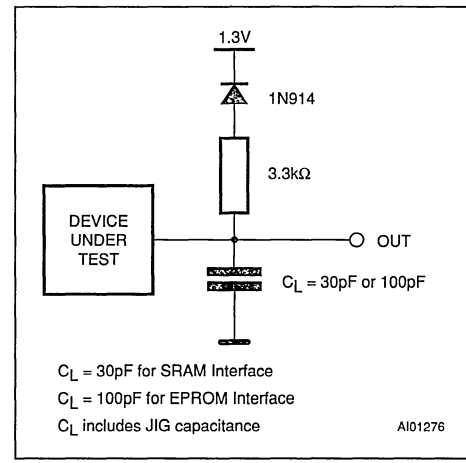


Table 9. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Memory Blocks

The memory blocks of the M28F211 and M28F221 are shown in Figure 8. The difference between the two products is simply an inversion of the block map to position the Boot Block at the top or bottom of the memory. The selection of the Boot Block at the top or bottom of the memory depends on the microprocessor needs.

Each block of the memory can be erased separately, but only by one block at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another block and then resumed. Programming and erasure of the memory is disabled when the program supply is at V_{PPL}. For successful programming and erasure the program supply must be at V_{PPH}. The Boot Block provides additional hardware security by use of the $\overline{RP}$ signal which must be at V_{HH} before any program or erase operation will be executed by the P/E.C. on the Boot Block.

Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down, and Electronic Signature Read. They are shown in Table 3.

Table 10. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V±10% or 5V±5%; V_{PP} = 12V±5% or 12V±10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 10MHz		50	mA
I_{CC} (1, 3)	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, $\overline{G} = V_{SS}$, f = 10MHz		45	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (3)	Supply Current (Power Down) CMOS	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{CC3}	Supply Current (Program)	Program in progress		50	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Current (Read or Standby)	$V_{PP} \ge V_{CC}$		200	µA
I_{PP1}	Program Leakage Current (Read or Standby)	$V_{PP} \le V_{CC}$		±10	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Program in progress		30	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations) 5% range		11.4	12.6	V
	Program Voltage (Program or Erase operations) 10% range		10.8	13.2	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot Block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 2mA typical in static operation.
2. Current increases to I_{CC} + I_{CC5} during a read operation
3. CMOS levels V_{CC} ± 0.2V and V_{SS} ± 0.2V. TTL levels V_{IH} and V_{IL}.

Table 11A. Read AC Characteristics
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	Test Condition	M28F211 / 221						Unit
				-60		-70		-80		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
				SRAM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	60		70		80		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		60		70		80	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		300		300		300	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		60		70		80	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		30		35		40	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		20		25		30	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		20		25		30	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Table 11B. Read AC Characteristics
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	Test Condition	M28F211 / 221						Unit
				-100		-120		-150		
				V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
				EPROM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		300		300		300	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		50		55	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		35		35		35	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		35		35		35	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 5. Read Mode AC Waveforms

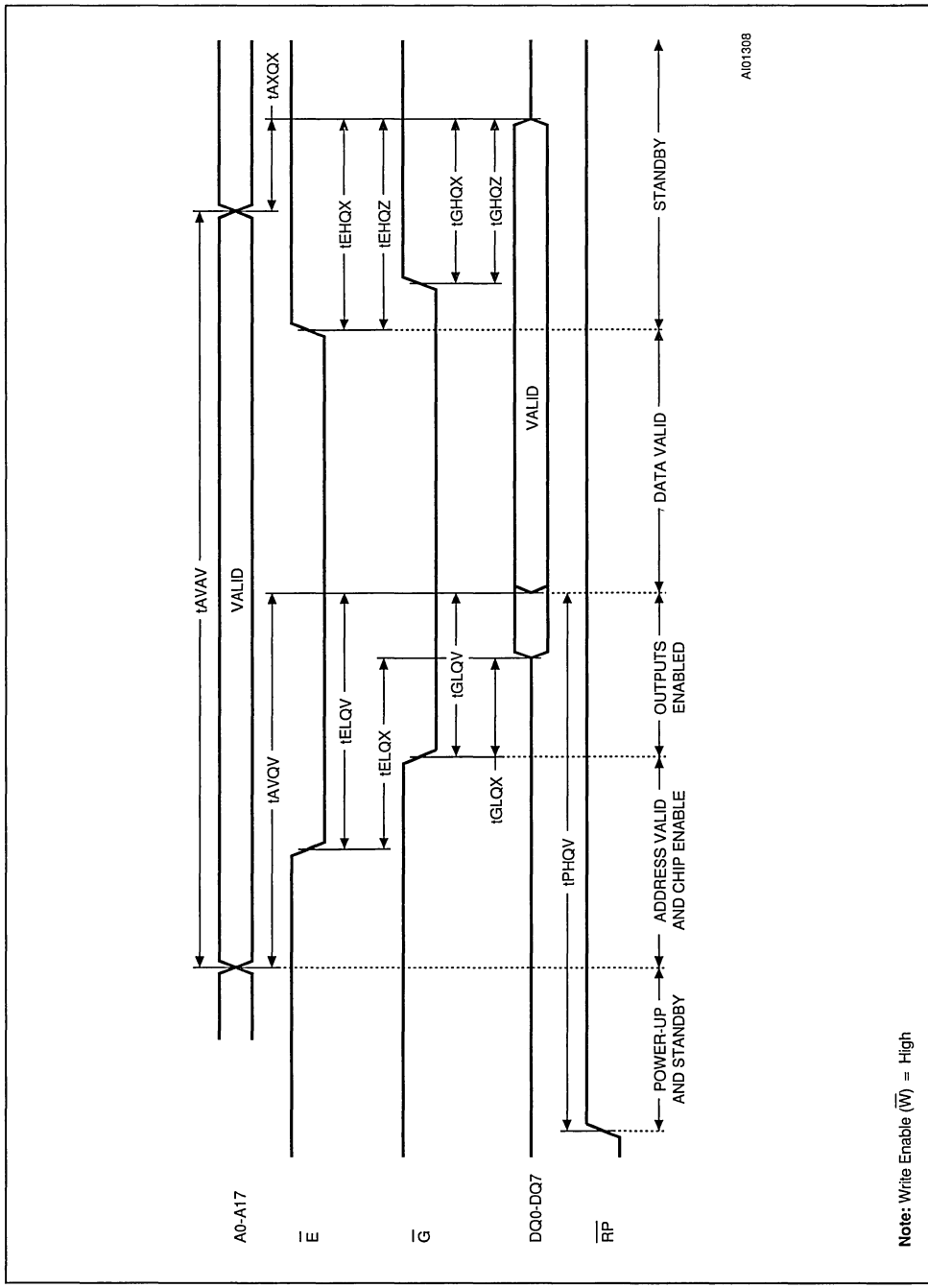


Table 12A. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	M28F211 / 221						Unit
			-60		-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	60		70		80		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	10		20		30		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	50		50		50		ns
t_{PHHWH}	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	100		100		100		ns
t_{VPHWH}	t_{VPS}	V_{PP} High to Write Enable High	100		100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		10		ns
t_{WHQV1} (1, 2)		Write Enable High to Output Valid	6		6		6		µs
t_{WHQV2} (1, 2)		Write Enable High to Output Valid (Boot Block Erase)	0.3		0.3		0.3		sec
t_{WHQV3} (1)		Write Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		0.3		sec
t_{WHQV4} (1)		Write Enable High to Output Valid (Main Block Erase)	0.6		0.6		0.6		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		100		100		100	ns

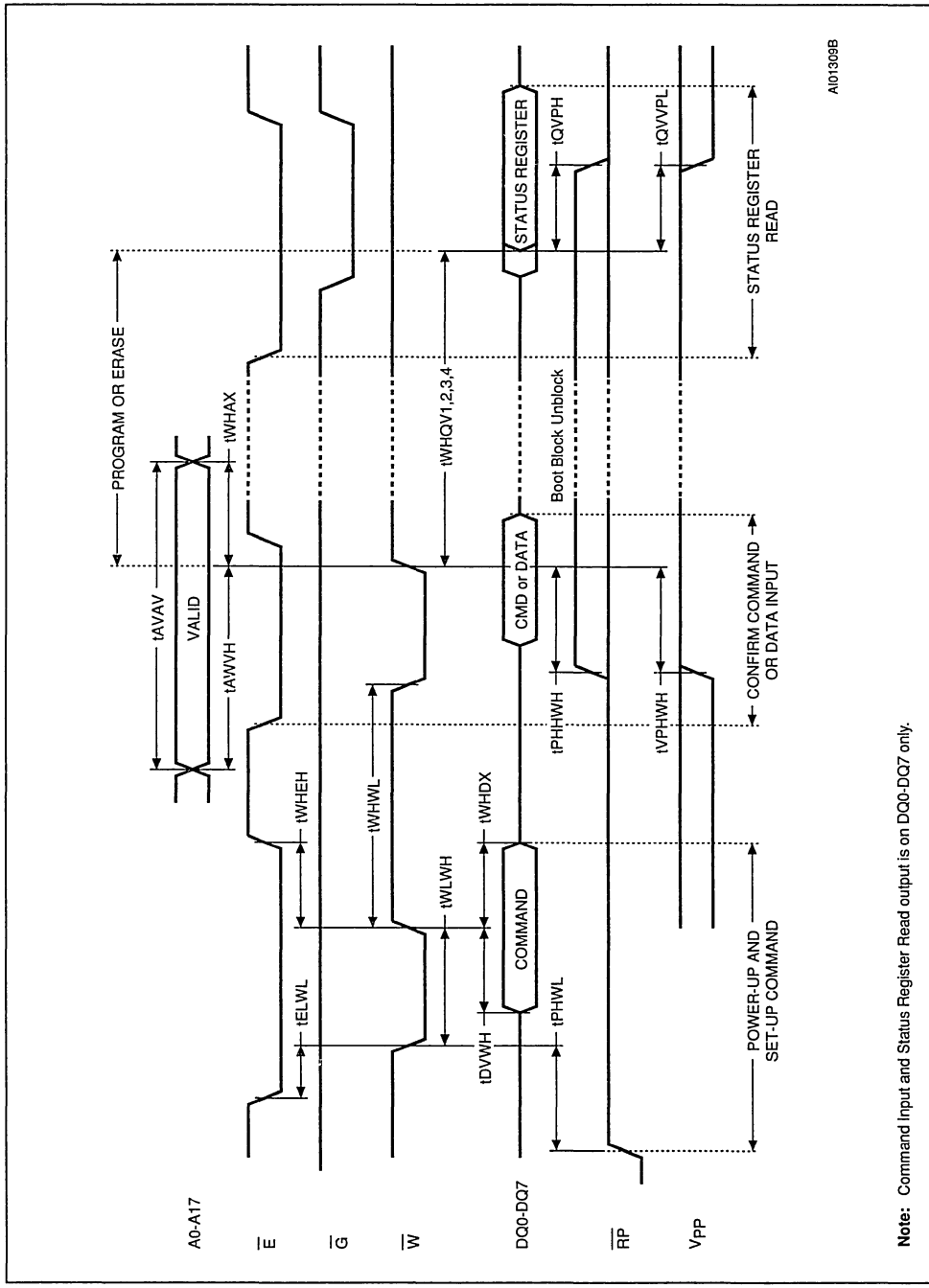
Notes: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Table 12B. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	M28F211 / 221						Unit
			-100		-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	60		70		90		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	60		60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	40		50		60		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	60		60		60		ns
t_{PHHWH}	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	100		100		100		ns
t_{VPHWH}	t_{VPS}	V_{PP} High to Write Enable High	100		100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		10		ns
t_{WHQV1} (1, 2)		Write Enable High to Output Valid	7		7		7		µs
t_{WHQV2} (1, 2)		Write Enable High to Output Valid (Boot Block Erase)	0.4		0.4		0.4		sec
t_{WHQV3} (1)		Write Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		0.4		sec
t_{WHQV4} (1)		Write Enable High to Output Valid (Main Block Erase)	0.7		0.7		0.7		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		100		100		100	ns

Notes: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Figure 6. Program & Erase AC Waveforms, $\overline{W}$ Controlled



Note: Command Input and Status Register Read output is on DQ0-DQ7 only.

Table 13A. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	M28F211 / 221						Unit
			-60		-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	60		70		80		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	50		50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	10		20		30		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	50		50		50		ns
t_{PHHEH}	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	100		100		100		ns
t_{VPHEH}	t_{VPS}	V_{PP} High to Chip Enable High	100		100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		10		ns
t_{EHQV1} (1, 2)		Chip Enable High to Output Valid	6		6		6		µs
t_{EHQV2} (1, 2)		Chip Enable High to Output Valid (Boot Block Erase)	0.3		0.3		0.3		sec
t_{EHQV3} (1)		Chip Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		0.3		sec
t_{EHQV4} (1)		Chip Enable High to Output Valid (Main Block Erase)	0.6		0.6		0.6		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		100		100		100	ns

Note: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Table 13B. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	M28F211 / 221						Unit
			-100		-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	60		70		90		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	60		60		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	40		50		60		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	60		60		60		ns
t_{PHHEH}	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	100		100		100		ns
t_{VPHEH}	t_{VPS}	V_{PP} High to Chip Enable High	100		100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		10		ns
t_{EHQV1} (1, 2)		Chip Enable High to Output Valid	7		7		7		µs
t_{EHQV2} (1, 2)		Chip Enable High to Output Valid (Boot Block Erase)	0.4		0.4		0.4		sec
t_{EHQV3} (1)		Chip Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		0.4		sec
t_{EHQV4} (1)		Chip Enable High to Output Valid (Main Block Erase)	0.7		0.7		0.7		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		100		100		100	ns

Note: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}
3. Time required for Relocking the Boot Block.

Figure 7. Program & Erase AC Waveforms, $\overline{E}$ Controlled

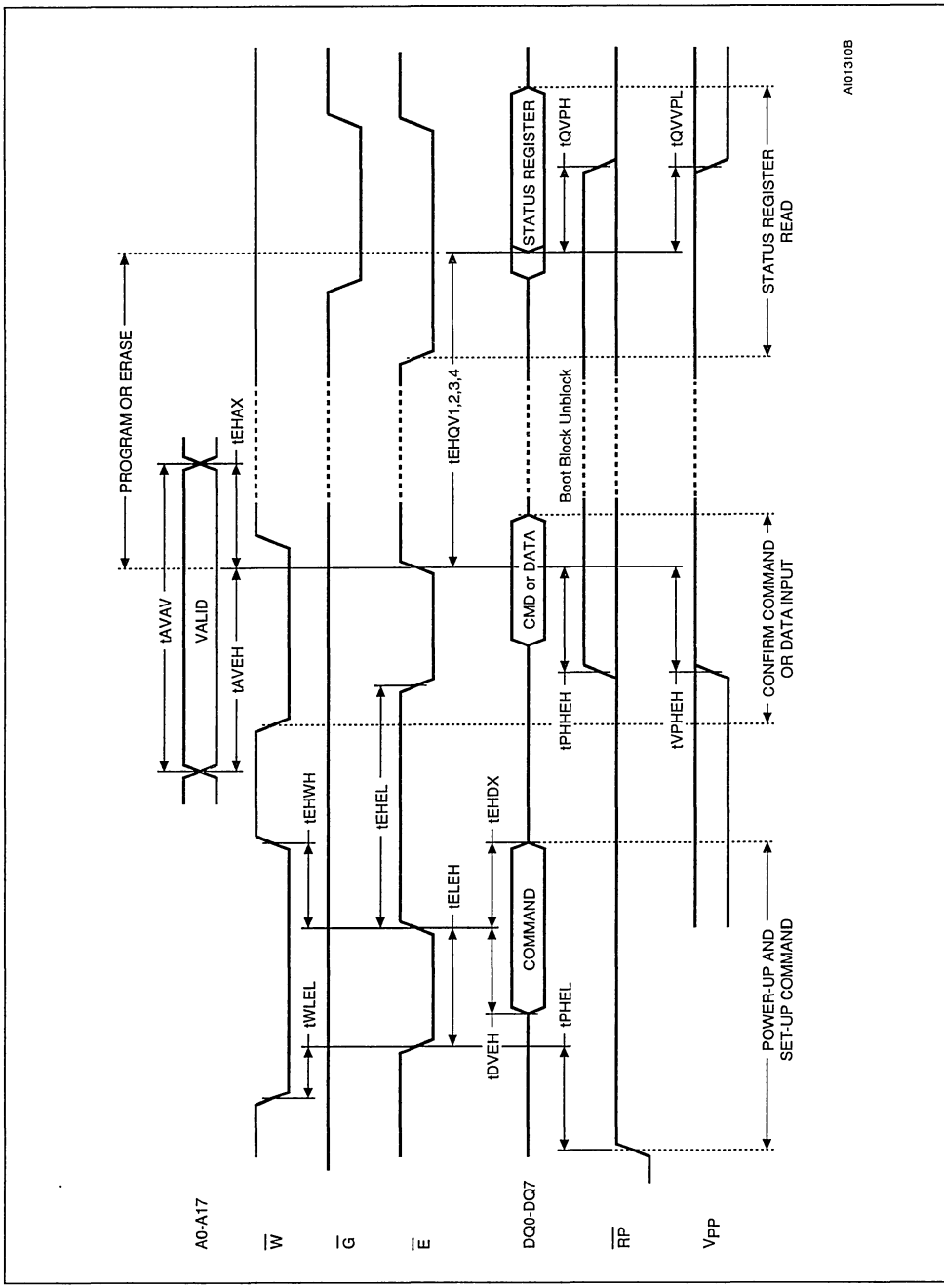


Table 14. Byte Program, Erase Times
(T_A = 0 to 70°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	Test Conditions	M28F211 / 221			Unit
		Min	Typ	Max	
Main Block Program	V_{PP} = 12V ±5%		1.2	4.2	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±5%		1	7	sec
Main Block Erase	V_{PP} = 12V ±5%		2.4	14	sec
Main Block Program	V_{PP} = 12V ±10%		6	20	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±10%		5.8	40	sec
Main Block Erase	V_{PP} = 12V ±10%		14	60	sec

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. The data read depends on the previous command written to the memory (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is low. The power consumption is reduced to the Power Down level, and Outputs are in high impedance, independant of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memories, the manufacturer code for SGS-THOMSON is 20h, and the device codes are 0E4h for the M28F211 (Top Boot Block) and 0E8h for the M28F221 (Bottom Boot Block). These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product.

The Electronic Signature is output by a Read Array operation when the voltage applied to A9 is at V_{ID}, the manufacturer code is output when the Address input A0 is Low and the device code is output when A0 is High. Other Address inputs are ignored.

Instructions and Commands

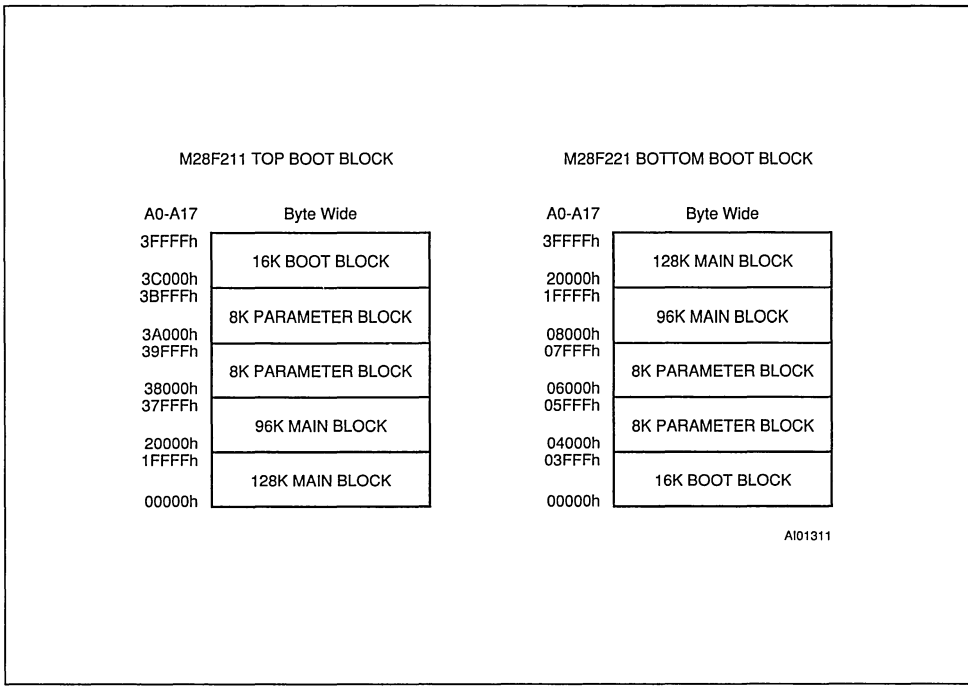
The memories include a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from 1 to 3 operations, the first of which is always a write operation and is followed by either a further write operation to confirm the first command or a read operation(s) to output data.

A Status Register indicates the P/E.C. status Ready or Busy, the suspend/in-progress status of erase operations, the failure/success of erase and program operations and the low/correct value of the Program Supply voltage V_{PP}.

The P/E.C. automatically sets bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The register can be read by the Read Status Register (RSR) instruction and cleared by the Clear Status Register (CLRS) instruction. The meaning of the bits b3 to b7 is shown in Table 7. Bits b0 to b2 are reserved for future use (and should be masked out during status checks).

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read the addressed memory array content.

Figure 8. Memory Map, Byte-wide Addresses



Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent Read operations output the contents of the Status Register. The contents of the status register are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the Status Register.

Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h followed by two read operations to output the manufacturer and device codes. The manufacturer code, 20h, is output when the address line A0 is Low, and the device code, 0E4h for the M28F211 or 0E8h for the M28F221, when A0 is High.

Erase (EE) instruction. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second command is the Erase Confirm command 0D0h. During the input of the second command an address of the block to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 and b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the RSR (Read Status Register) and ES (Erase Suspend) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it has completed. After completion the Status Register bit b5 returns '1' if there has been an Erase Failure because erasure has not been verified even after the maximum number of erase cycles have been executed. Status Register bit b3 returns '1' if V_{PP} does not remain at V_{PPH} level when the erasure is attempted and/or proceeding.

V_{PP} must be at V_{PPH} when erasing, erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register (CLRS).

The Boot Block can only be erased when $\overline{RP}$ is also at V_{HH}.

Program (PG) instruction. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or 10h). A second write operation latches the Address and the Data to be written and starts the P/E.C. Read operations output the status register after the programming has started.

Memory programming is only made by writing '0' in place of '1' in a byte.

During the execution of the programming by the P/E.C., the memory accepts only the RSR (Read Status Register) instruction. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status Register bit b3 returns a '1' if V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming. V_{PP} must be at V_{PPH} when programming, programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect. Then after having cleared the Status Register (CLRS), the memory must be erased and re-programmed.

The Boot Block can only be programmed when $\overline{RP}$ is at V_{HH}.

Clear Status Register (CLRS) instruction. The Clear Status Register uses a single write operation which clears bits b3, b4 and b5, if latched to '1' by the P/E.C., to '0'. Its use is necessary before any new operation when an error has been detected.

Erase Suspend (ES) instruction. The Erase operation may be suspended by this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates whether the erase has actually been suspended, b6 = '1', or whether the P/E.C. cycle was the last and the erase is completed, b6 = '0'. During the suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Read operations initially output the status register while erase is suspended but, following a Read instruction, data from other blocks of the memory can be read. V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or the $\overline{RP}$ signal goes Low while erase is suspended then erase is aborted while bits b5 and b3 of the status register are set. Erase operation must be repeated after having cleared the status register, to be certain to erase the block.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 0D0h. The status register bit b6 is cleared when erasure resumes. Read operations output the status register after the erase is resumed. The suggested flow charts for programs that use the programming, erasure and erase suspend/resume features of the memories are shown in Figure 9 to Figure 11.

Programming. The memory can be programmed byte-by-byte. The Program Supply voltage V_{PP} must be applied before program instructions are given, and if the programming is in the Boot Block, $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Program Supply voltage may be applied continuously during programming. The program sequence is started by writing a Program Set-up command (40h) to the Command Interface, this is followed by writing the address and data byte or word to the memory. The Program/Erase Controller automatically starts and performs the programming after the second write operation, providing that the V_{PP} voltage (and $\overline{RP}$ voltage if programming the Boot Block) are correct. During the programming the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that programming is completed.

A full status check can be made after each byte/word or after a sequence of data has been programmed. The status check is made on bit b3 for any possible V_{PP} error and on bit b4 for any possible programming error.

Erase. The memory can be erased by blocks. The Program Supply voltage V_{PP} must be applied before the Erase instruction is given, and if the Erase is of the Boot Block $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Erase sequence is started by writing an Erase Set-up command (20h) to the Command Interface, this is followed by an address in the block to be erased and the Erase Confirm command (0D0h). The Program/Erase Controller automatically starts and performs the block erase, providing the V_{PP} voltage (and the $\overline{RP}$ voltage if the erase is of the Boot Block) is correct. During the erase the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that erase is completed.

DEVICE OPERATION (cont'd)

A full status check can be made after the block erase by checking bit b3 for any possible V_{PP} error, bits b5 and b6 for any command sequence errors (erase suspended) and bit b5 alone for an erase error.

Reset. Note that after any program or erase instruction has completed with an error indication or after any V_{PP} transitions down to V_{PPL} the Command Interface must be reset by a Clear Status Register Instruction before data can be accessed.

Automatic Power Saving

The M28F211 and M28F221 memories place themselves in a lower power state when not being accessed. Following a Read operation, after a delay equal to the memory access time, the Supply Current is reduced from a typical read current of 25mA (CMOS inputs) to less than 2mA.

Power Down

The memories provide a power down control input $\overline{RP}$. When this signal is taken to below V_{SS} + 0.2V all internal circuits are switched off and the supply current drops to typically 0.2µA and the program current to typically 0.1µA. If $\overline{RP}$ is taken low during a memory read operation then the memory is deselected and the outputs become high impedance. If $\overline{RP}$ is taken low during a program or erase sequence then it is aborted and the memory content is no longer valid.

Recovery from deep power down requires 300ns to a memory read operation, or 210ns to a command write. On return from power down the status register is cleared to 00h.

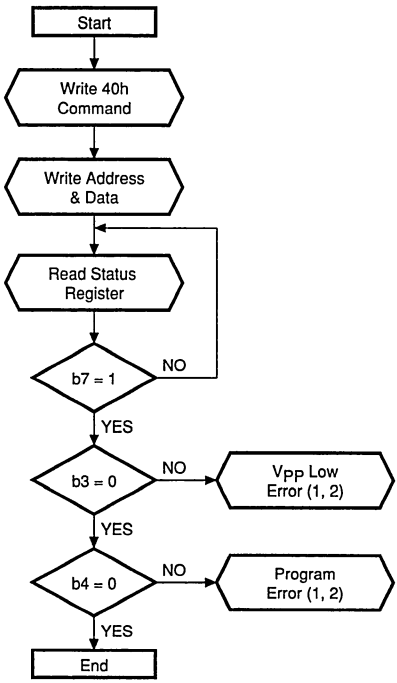
Power Up

The Supply voltage V_{CC} and the Program Supply voltage V_{PP} can be applied in any order. The memory Command Interface is reset on power up to Read Memory Array, but a negative transition of Chip Enable $\overline{E}$ or a change of the addresses is required to ensure valid data outputs. Care must be taken to avoid writes to the memory when V_{CC} is above V_{LKO} and V_{PP} powers up first. Writes can be inhibited by driving either $\overline{E}$ or $\overline{W}$ to V_{IH}. The memory is disabled until $\overline{RP}$ is up to V_{IH}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} and V_{PP} rails decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{PP} program and erase currents required.

Figure 9. Program Flow-chart and Pseudo Code



PG instruction:
– write 40h command
– write Address & Data
(memory enters read status state after the PG instruction)

do:
– read status register
(E or G must be toggled)

while b7 = 1

If b3 = 0, V_{PP} low error:
– error handler

If b4 = 0, Program error:
– error handler

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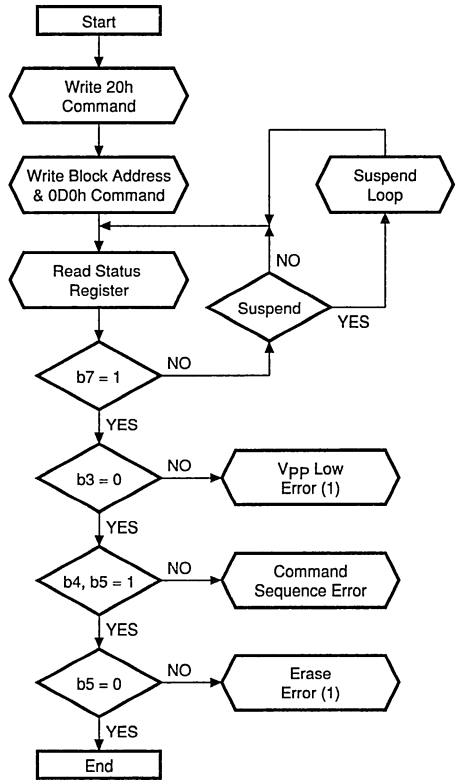
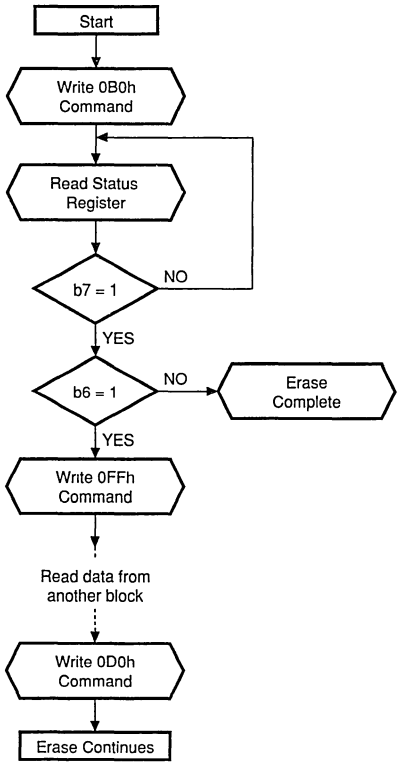
Notes: 1. Status check of b3 (V_{PP} Low) and b4 (Program Error) can be made after each byte/word programming or after a sequence.
2. If a V_{PP} Low or Program Erase is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 10. Erase Flow-chart and Pseudo Code



Note: 1. If V_{PP} Low or Erase Error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 11. Erase Suspend & Resume Flow-chart and Pseudo Code



ES instruction:
– write 0B0h command
(memory enters read register state after the ES instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

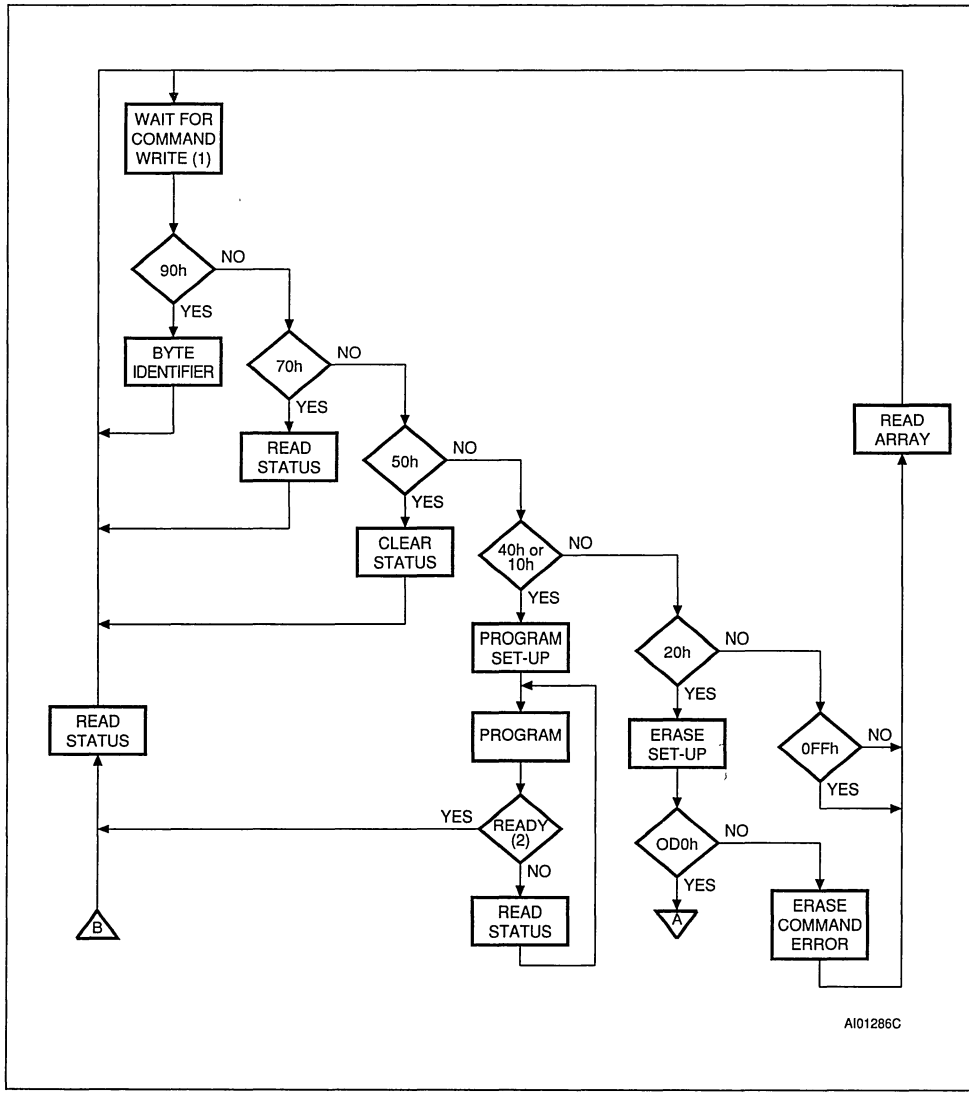
If b6 = 0, Erase completed
(at this point the memory wich accept only the RD or ER instruction)

RD instruction:
– write 0FFh command
– one o more data reads from another block

ER instruction:
– write 0D0h command to resume erasure

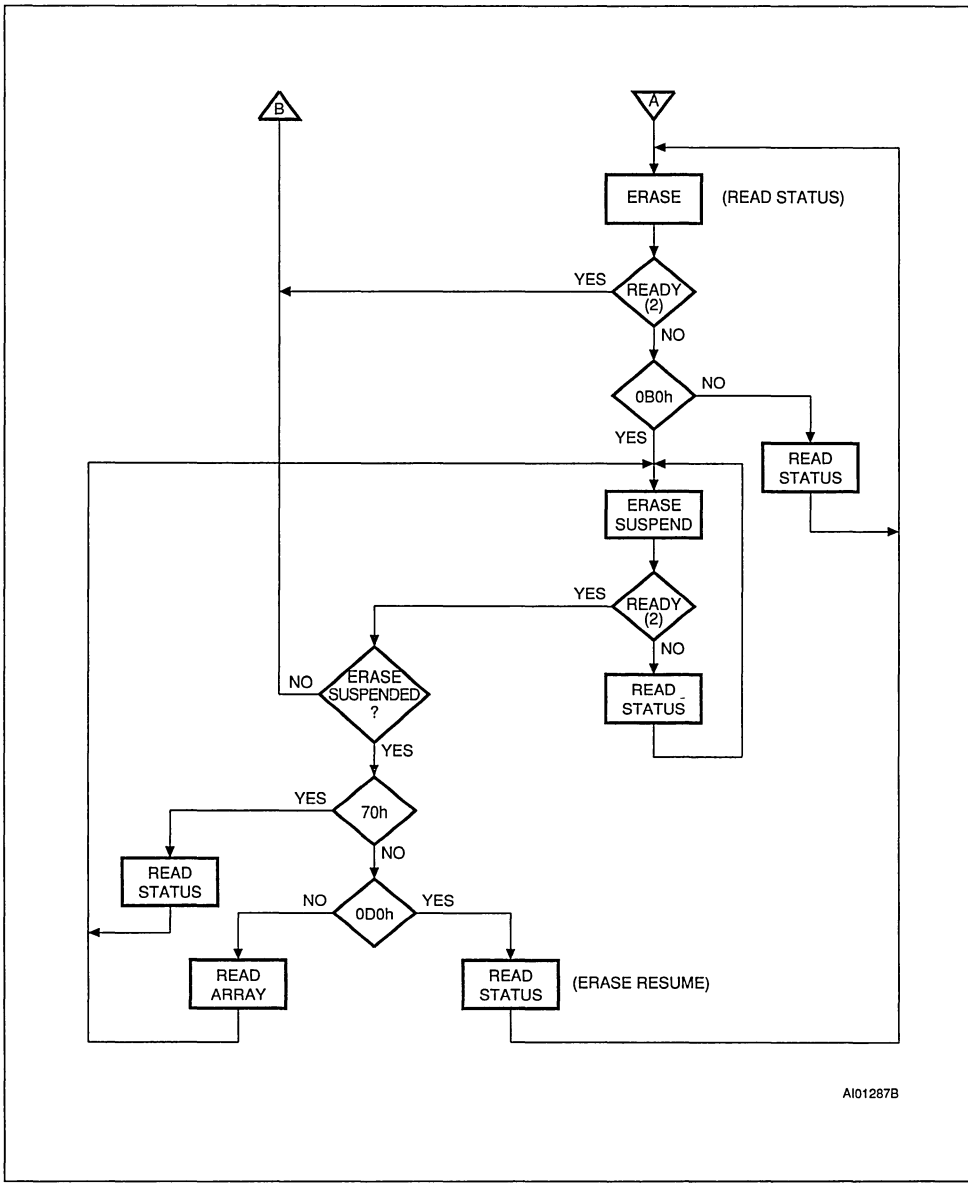
AI01280

Figure 12. Command Interface and Program Erase Controller Flow-diagram (a)



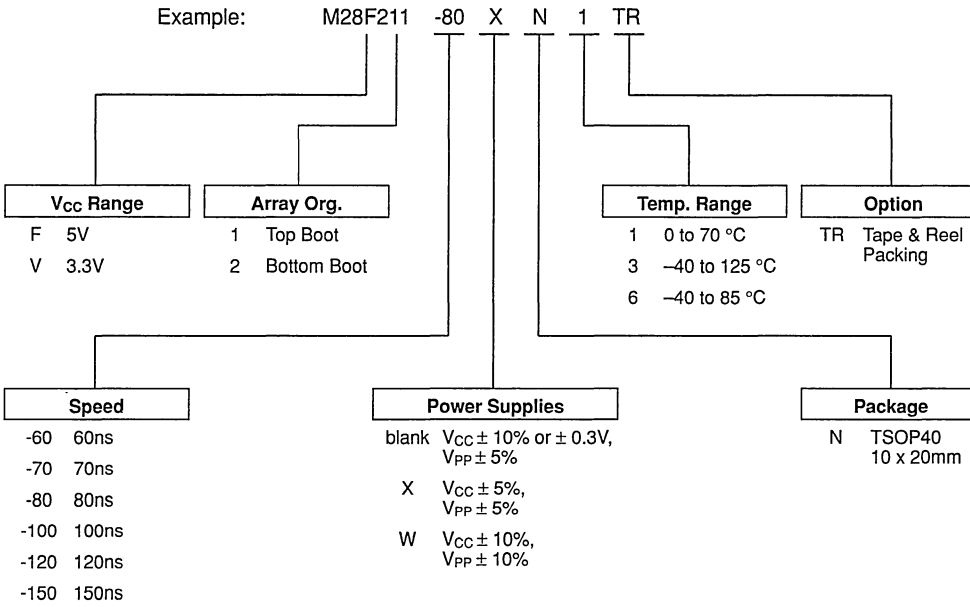
Notes: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 13. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME



Full data on the 3V products, M28V211 and M28V221, will be added to this document in the near future.

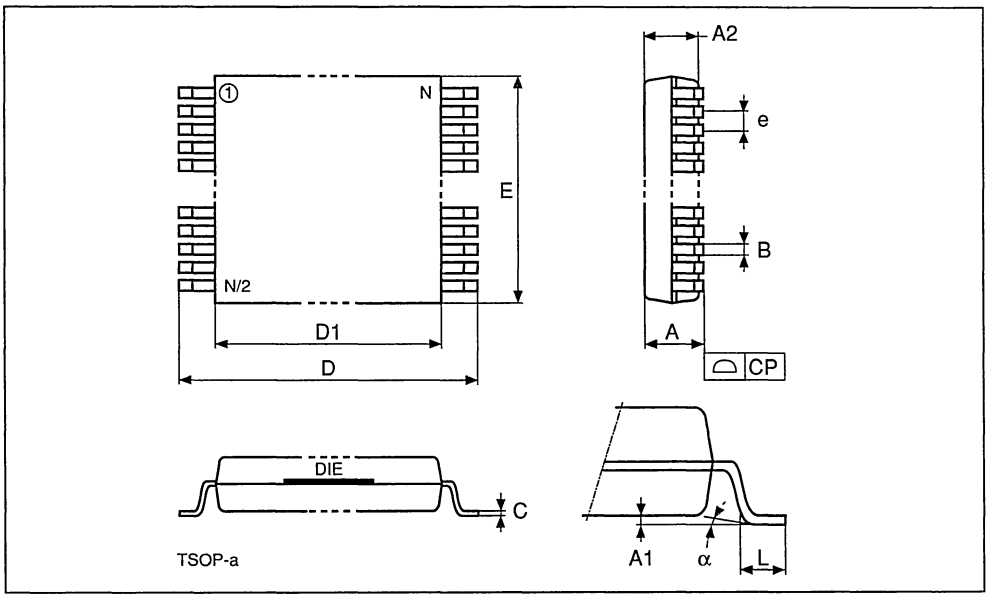
For a list of available options (V_{CC} Range, Array Organization, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		40			40	
CP			0.10			0.004

TSOP40



TSOP-a

Drawing is out of scale

4 Megabit (x8 or x16, Block Erase) FLASH MEMORY

PRELIMINARY DATA

- DUAL x8 and x16 ORGANIZATION
- SMALL SIZE PLASTIC PACKAGES TSOP56 and SO44
- MEMORY ERASE in BLOCKS
  - One 16K Byte or 8K Word Boot Block (top or bottom location) with hardware write and erase protection
  - Two 8K Byte or 4K Word Key Parameter Blocks
  - One 96K Byte or 48K Word Main Block
  - Three 128K Byte or 64K Word Main Blocks
- 5V ± 10% SUPPLY VOLTAGE
- 12V ± 5% PROGRAMMING VOLTAGE
- 100,000 PROGRAM/ERASE CYCLES
- PROGRAM/ERASE CONTROLLER
- AUTOMATIC STATIC MODE
- LOW POWER CONSUMPTION
  - 60µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
  - 20/25mA Typical Operating Consumption (Byte/Word)
- HIGH SPEED ACCESS TIME: 70ns
- EXTENDED TEMPERATURE RANGES

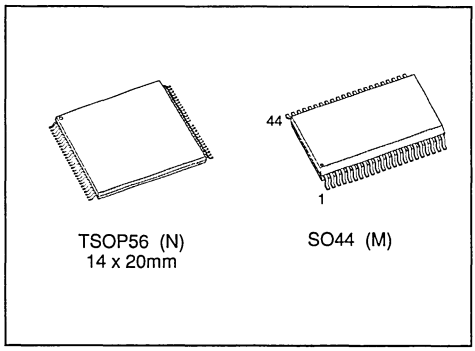


Figure 1. Logic Diagram

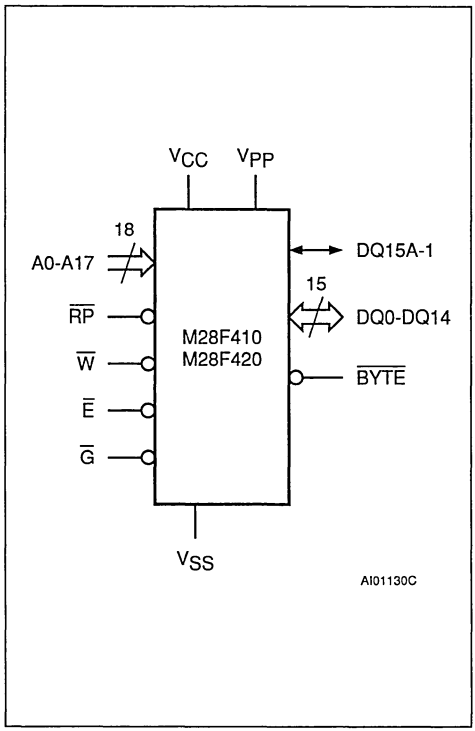
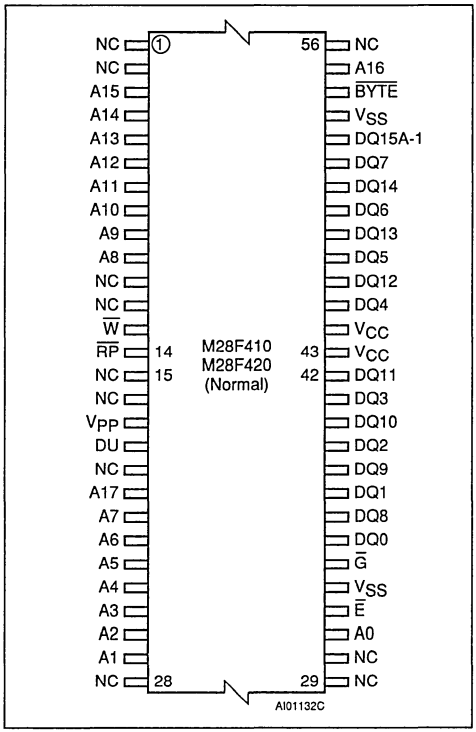


Table 1. Signal Names

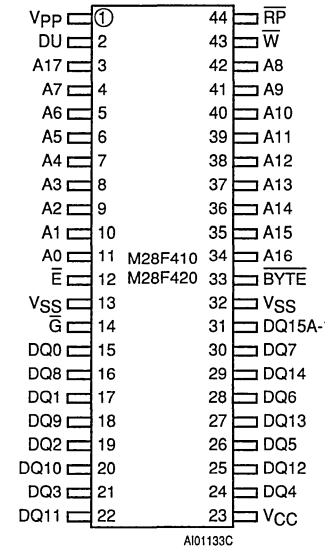
A0-A17	Address Inputs
DQ0-DQ7	Data Input / Outputs
DQ8-DQ14	Data Input / Outputs
DQ15A-1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{BYTE}$	Byte/Word Organization
$\overline{RP}$	Reset/Power Down/Boot Block Unlock
V_{PP}	Program & Erase Supply Voltage
V_{CC}	Supply Voltage

Figure 2A. TSOP Pin Connections



Warning: NC = No Connections, DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9} (2)	A9 Voltage		–0.6 to 13.5	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
V_{RP} (2)	$\overline{RP}$ Voltage		–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 7V allowed for less than 20ns

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{BYTE}$	DQ0 - DQ7	DQ8 - DQ14	DQ15A-1
Read Word	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Data Output	Data Output	Data Output
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Hi-Z	Address Input
Write Word	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Data Input	Data Input	Data Input
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data Input	Hi-Z	Address Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	X	Hi-Z	Hi-Z	Hi-Z
Power Down	X	X	X	V_{IL}	X	Hi-Z	Hi-Z	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}

Table 4. Electronic Signature

Organi-sation	Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{BYTE}$	A0	A9	A1-A8 & A10-A17	DQ0 - DQ7	DQ8 - DQ14	DQ15 A-1
Word-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{ID}	Don't Care	20h	00h	0
	Device Code	M28F410	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0F2h	00h	0
		M28F420	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0FAh	00h	0
Byte-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h	Hi-Z	Don't Care
	Device Code	M28F410	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{ID}	Don't Care	0F2h	Hi-Z	Don't Care
		M28F420	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{ID}	Don't Care	0FAh	Hi-Z	Don't Care

Note: $\overline{RP}$ = V_{IH}

DESCRIPTION

The M28F410 and M28F420 FLASH MEMORIES are non-volatile memories that may be erased electrically at the block level and programmed by byte or word. The interface is directly compatible with most microprocessors. SO44 and TSOP56 packages are used.

Organization

The organization, as 512K x 8 or 256K x 16, is selectable by an external $\overline{BYTE}$ signal. When $\overline{BYTE}$ is Low and the x8 organization is selected, the Data Input/Output signal DQ15 acts as Address line A-1 and selects the lower or upper byte of the memory word for output on DQ0-DQ7, DQ8-DQ14 remain high impedance. When $\overline{BYTE}$ is High the memory uses the Address inputs A0-A17 and the Data Input/Outputs DQ0-DQ15. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down/Boot block unlock, tri-level input, places the memory in deep power down, normal operation or enables programming and erasure of the Boot block.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data (4)	Operation	Address	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Signature
EE	Erase	2	Write	X	20h	Write	Block Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSR or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of Read cycle can occur after one command cycle.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.
4. When word organization is used, upper byte is don't care for command input.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Array

Blocks

Erasure of the memories is in blocks. There are 7 blocks in the memory address space, one Boot Block of 16K Bytes or 8K Words, two 'Key Parameter Blocks' of 8K Bytes or 4K Words, one 'Main Block' of 96K Bytes or 48K Words, and three 'Main Blocks' of 128K Bytes or 64K Words. The M28F410 memory has the Boot Block at the top of the memory address space (3FFFFh) and the M28F420 locates the Boot Block starting at the bottom (00000h). Erasure of each block takes typically 1 second and each block can be programmed and erased over 100,000 cycles.

The Boot Block is hardware protected from accidental programming or erasure depending on the $\overline{RP}$ signal. Program/Erase commands in the Boot Block are executed only when $\overline{RP}$ is at 12V. Block erasure may be suspended while data is read from other blocks of the memory, then resumed.

Bus Operations

Six operations can be performed by the appropriate bus cycles, Read Byte or Word from the Array, Read Electronic Signature, Output Disable, Standby, Power Down and Write the Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor the memory's status. When power

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits b4 or b5 for Program or Erase Success
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction P/ECS and ESS bits are set to '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte or word.
			'0'	Program Success	
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction has been executed.
			'0'	V_{PP} OK	
	2	Reserved			
	1	Reserved			
	0	Reserved			

Notes: Logic level '1' is High, '0' is Low.

is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte or word program and block erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte or word programming takes typically 9µs, block erase typically 1 second. Erasure of a memory block may be suspended in order to read data from another block and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation.

Power Saving

The M28F410 and M28F420 have a number of power saving features. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down ($\overline{RP}$) signals are at V_{CC}, when the supply current drops to typically 60µA. A deep power down mode is enabled when the Reset/Power Down ($\overline{RP}$) signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 300ns maximum, with instructions to the C.I. recognised after only 210ns.

Table 8. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

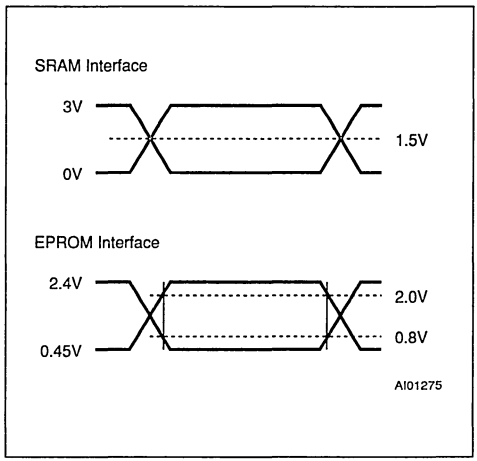


Figure 4. AC Testing Load Circuit

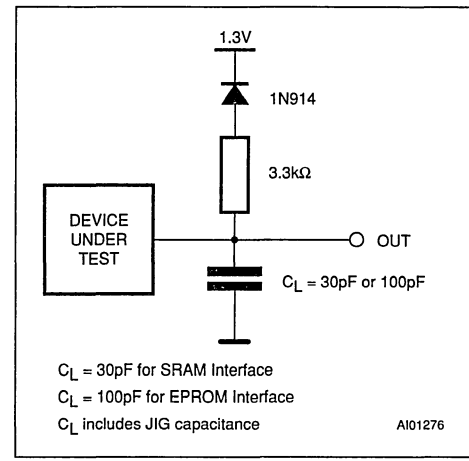


Table 9. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

DEVICE OPERATION

Signal Descriptions

A0-A17 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

A9 Address Input is also used for the Electronic Signature Operation. When A9 is raised to 12V the Electronic Signature may be read. The A0 signal is used to read two words or bytes, when A0 is Low the Manufacturer code is read and when A0 is High the Device code. When $\overline{BYTE}$ is Low DQ0-DQ7 output the codes and DQ8-DQ15 are don't care, when $\overline{BYTE}$ is High DQ0-DQ7 output the codes and DQ8-DQ15 output 00h.

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte or the lower byte of a word to be programmed or a command to the C.I., are latched when both Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output from the memory Array, the Electronic Signature or Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

DQ8-DQ14 and DQ15A-1 Data Input/Outputs. These input/outputs are used in the word-wide organization. When $\overline{BYTE}$ is High for the most significant byte of the input or output, functioning as described for DQ0-DQ7 above. When $\overline{BYTE}$ is Low, DQ8-DQ14 are high impedance, DQ15A-1 is the Address A-1 input.

Table 10. DC Characteristics
(T_A = 0 to 70°C; V_{CC} = 5V±10% or 5V±5% ; V_{PP} = 12V±5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read Byte-wide) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		50	mA
I_{CC} (1, 3)	Supply Current (Read Word-wide) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		55	mA
I_{CC} (1, 3)	Supply Current (Read Byte-wide) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		45	mA
	Supply Current (Read Word-wide) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		50	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$, $\overline{BYTE} = V_{CC} \pm 0.2V$ or V_{SS}		100	µA
I_{CC2} (3)	Supply Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{CC3}	Supply Current (Program Byte-wide)	Byte program in progress		50	mA
	Supply Current (Program Word-wide)	Word program in progress		60	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Leakage Current (Read or Standby)	$V_{PP} \le V_{CC}$		±10	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program Byte-wide)	Byte program in progress		30	mA
I_{PP3}	Program Current (Program Word-wide)	Word program in progress		40	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	$A9 = V_{ID}$		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 8mA typical in static operation.
2. Current increases to $I_{CC} + I_{CC5}$ during a read operation.
3. CMOS levels $V_{CC} \pm 0.2V$ and $V_{SS} \pm 0.2V$. TTL levels V_{IH} and V_{IL}.

Table 11. DC Characteristics
(T_A = –40 to 85°C; V_{CC} = 5V±10% or 5V±5% ; V_{PP} = 12V±5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read Byte-wide) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		65	mA
I_{CC} (1, 3)	Supply Current (Read Word-wide) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		70	mA
I_{CC} (1, 3)	Supply Current (Read Byte-wide) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		60	mA
	Supply Current (Read Word-wide) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		65	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$, $\overline{BYTE} = V_{CC} \pm 0.2V$ or V_{SS}		100	µA
I_{CC2} (3)	Supply Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		8	µA
I_{CC3}	Supply Current (Program Byte-wide)	Byte program in progress		50	mA
	Supply Current (Program Word-wide)	Word program in progress		60	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Leakage Current (Read or Standby)	$V_{PP} \le V_{CC}$		±15	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program Byte-wide)	Byte program in progress		30	mA
I_{PP3}	Program Current (Program Word-wide)	Word program in progress		40	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 8mA typical in static operation.
2. Current increases to I_{CC} + I_{CC5} during a read operation.
3. CMOS levels V_{CC} ± 0.2V and V_{SS} ± 0.2V. TTL levels V_{IH} and V_{IL}.

Table 12. DC Characteristics
(T_A = –40 to 125°C; V_{CC} = 5V±10% or 5V±5% ; V_{PP} = 12V±5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read Byte-wide) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		65	mA
I_{CC} (1, 3)	Supply Current (Read Word-wide) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		70	mA
I_{CC} (1, 3)	Supply Current (Read Byte-wide) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		60	mA
	Supply Current (Read Word-wide) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		65	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$, $\overline{BYTE} = V_{CC} \pm 0.2V$ or V_{SS}		130	µA
I_{CC2} (3)	Supply Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		80	µA
I_{CC3}	Supply Current (Program Byte-wide)	Byte program in progress		50	mA
	Supply Current (Program Word-wide)	Word program in progress		60	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Leakage Current (Read or Standby)	$V_{PP} \le V_{CC}$		±10	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program Byte-wide)	Byte program in progress		30	mA
I_{PP3}	Program Current (Program Word-wide)	Word program in progress		40	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 8mA typical in static operation.
2. Current increases to I_{CC} + I_{CC5} during a read operation.
3. CMOS levels V_{CC} ± 0.2V and V_{SS} ± 0.2V. TTL levels V_{IH} and V_{IL}.

Table 13. Read AC Characteristics (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F410 / 20								Unit
			-70		-80		-100		-120		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	70		80		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid		70		80		100		120	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid		300		300		300		300	ns
t_{ELQX} (2)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		0		ns
t_{ELQV} (3)	t_{CE}	Chip Enable Low to Output Valid		70		80		100		120	ns
t_{GLQX} (2)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		0		ns
t_{GLQV} (3)	t_{OE}	Output Enable Low to Output Valid		35		40		45		50	ns
t_{EHQX} (2)	t_{OH}	Chip Enable High to Output Transition	0		0		0		0		ns
t_{EHQZ} (2)	t_{HZ}	Chip Enable High to Output Hi-Z		25		30		35		35	ns
t_{GHQX} (2)	t_{OH}	Output Enable High to Output Transition	0		0		0		0		ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z		25		30		35		35	ns
t_{AXQX} (2)	t_{OH}	Address Transition to Output Transition	0		0		0		0		ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Sampled only, not 100% tested.
3. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Table 14. Read AC Characteristics (1)
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F410 / 20								Unit
			-80		-90		-100		-120		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	80		90		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid		80		90		100		120	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid		300		300		300		300	ns
t_{ELQX} (2)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		0		ns
t_{ELQV} (3)	t_{CE}	Chip Enable Low to Output Valid		80		90		100		120	ns
t_{GLQX} (2)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		0		ns
t_{GLQV} (3)	t_{OE}	Output Enable Low to Output Valid		40		45		50		55	ns
t_{EHQX} (2)	t_{OH}	Chip Enable High to Output Transition	0		0		0		0		ns
t_{EHQZ} (2)	t_{HZ}	Chip Enable High to Output Hi-Z		30		35		40		45	ns
t_{GHQX} (2)	t_{OH}	Output Enable High to Output Transition	0		0		0		0		ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z		30		35		40		45	ns
t_{AXQX} (2)	t_{OH}	Address Transition to Output Transition	0		0		0		0		ns

Notes: 1. See Figure 3 and Table 8 for timing measurements
2. Sampled only, not 100% tested.
3. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 5. Read Mode AC Waveforms

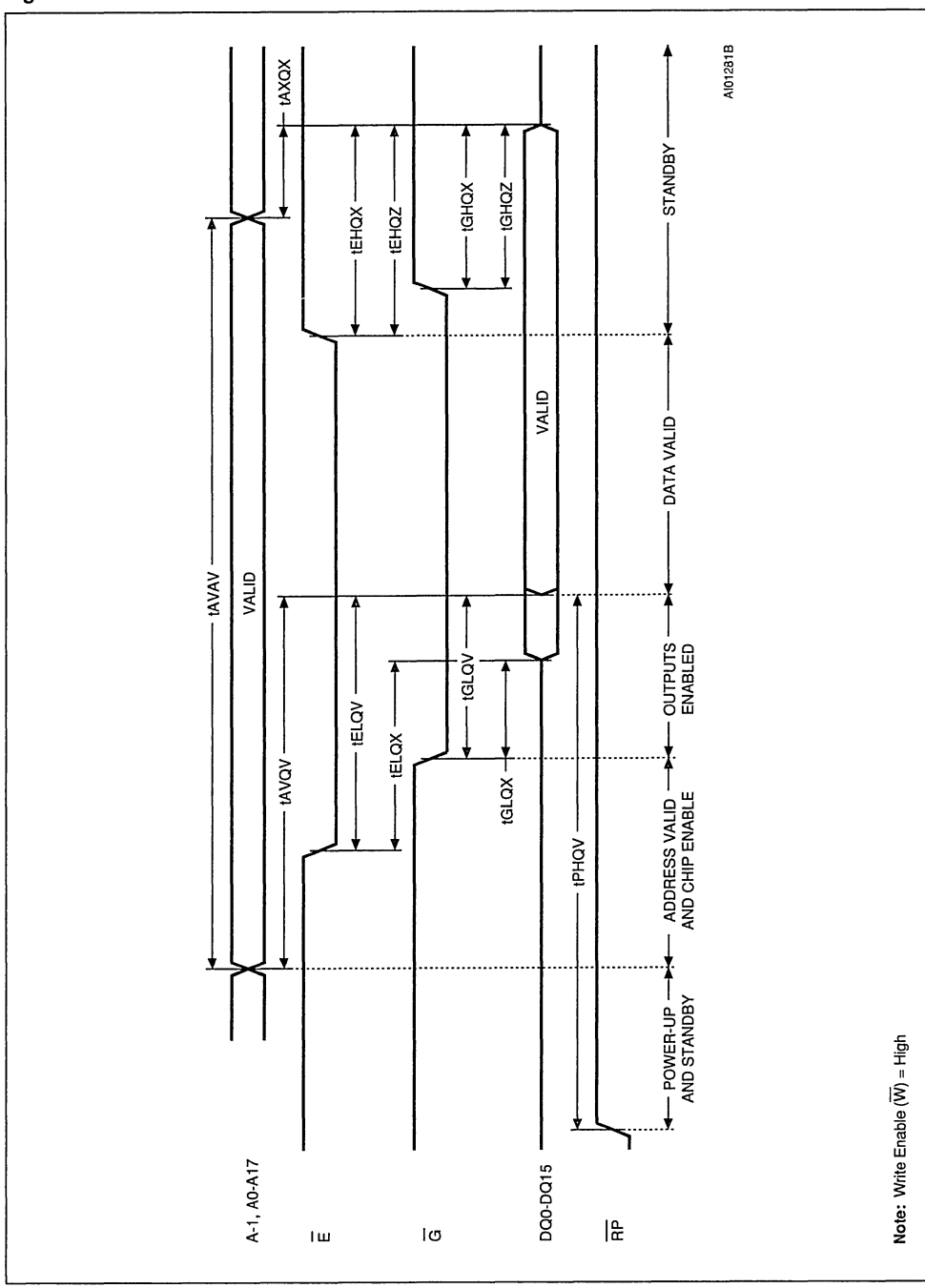


Table 15. $\overline{BYTE}$ AC Characteristics (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Parameter	M28F410 / 20								Unit
		-70		-80		-100		-120		
		V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
		SRAM Interface		EPROM Interface		EPROM Interface		EPROM Interface		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ELBL}	Chip Enable Low to BYTE Low		5		5		5		5	ns
t_{ELBH}	Chip Enable Low to BYTE High		5		5		5		5	ns
t_{BLQV} (2)	$\overline{BYTE}$ Low to Output Valid		70		80		100		120	ns
t_{BHQV}	$\overline{BYTE}$ High to Output Valid		70		80		100		120	ns
t_{BLQZ}	$\overline{BYTE}$ Low to Output Hi-Z		25		30		35		35	ns

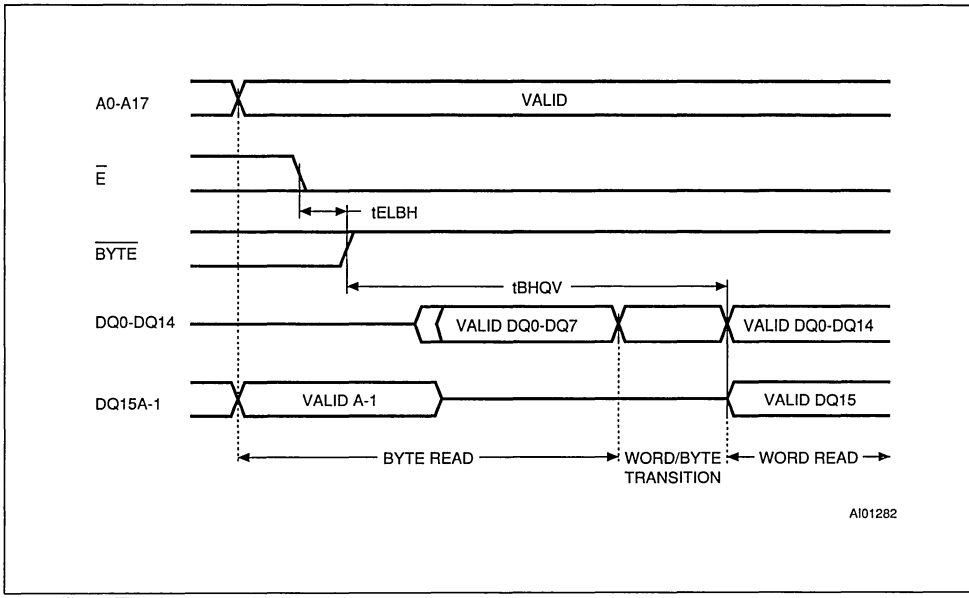
Notes: 1. Sampled only, not 100% tested.
2. It is equal to t_{AVQV} when measured from DQ15A-1 valid.

Table 16. $\overline{BYTE}$ AC Characteristics (1)
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Parameter	M28F410 / 20								Unit
		-80		-90		-100		-120		
		V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
		SRAM Interface		EPROM Interface		EPROM Interface		EPROM Interface		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ELBL}	Chip Enable Low to BYTE Low		5		5		5		5	ns
t_{ELBH}	Chip Enable Low to BYTE High		5		5		5		5	ns
t_{BLQV} (2)	$\overline{BYTE}$ Low to Output Valid		80		90		100		120	ns
t_{BHQV}	$\overline{BYTE}$ High to Output Valid		80		90		100		120	ns
t_{BLQZ}	$\overline{BYTE}$ Low to Output Hi-Z		30		35		40		45	ns

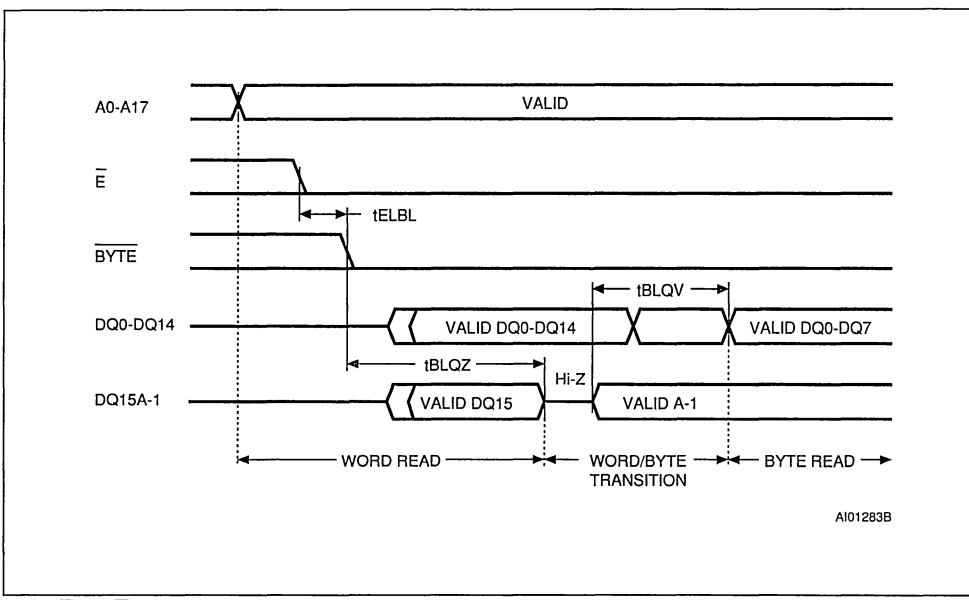
Notes: 1. Sampled only, not 100% tested.
2. It is equal to t_{AVQV} when measured from DQ15A-1 valid.

Figure 6. $\overline{BYTE}$ Mode AC Waveforms, $\overline{BYTE}$ Low to High



Note: $\overline{G}$ Low, $\overline{W}$ = High, other timings as Read Mode AC waveforms.

Figure 7. $\overline{BYTE}$ Mode AC Waveforms, $\overline{BYTE}$ High to Low



Note: $\overline{G}$ Low, $\overline{W}$ = High, other timings as Read Mode AC waveforms.

Table 17A. Write AC Characteristics, Write Enable Controlled (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F410 / 20				Unit
			-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	70		80		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		30		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	50		50		ns
t_{PHHWH} (5)	t_{PHS}	Power Down VHH (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid (Word/Byte Program)	6		6		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.3		0.3		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.6		0.6		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 17B. Write AC Characteristics, Write Enable Controlled (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F410 / 420				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	60		70		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	40		50		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	60		60		ns
t_{PHHWH} (5)	t_{PHS}	Power Down VHH (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid (Word/Byte Program)	7		7		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 18A. Write AC Characteristics, Write Enable Controlled (1)
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F410 / 20				Unit
			-80		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	80		90		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		60		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	50		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		40		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	50		60		ns
t_{PHHWH} (5)	t_{PHS}	Power Down VHH (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid (Word/Byte Program)	6		7		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.3		0.4		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.3		0.4		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.6		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

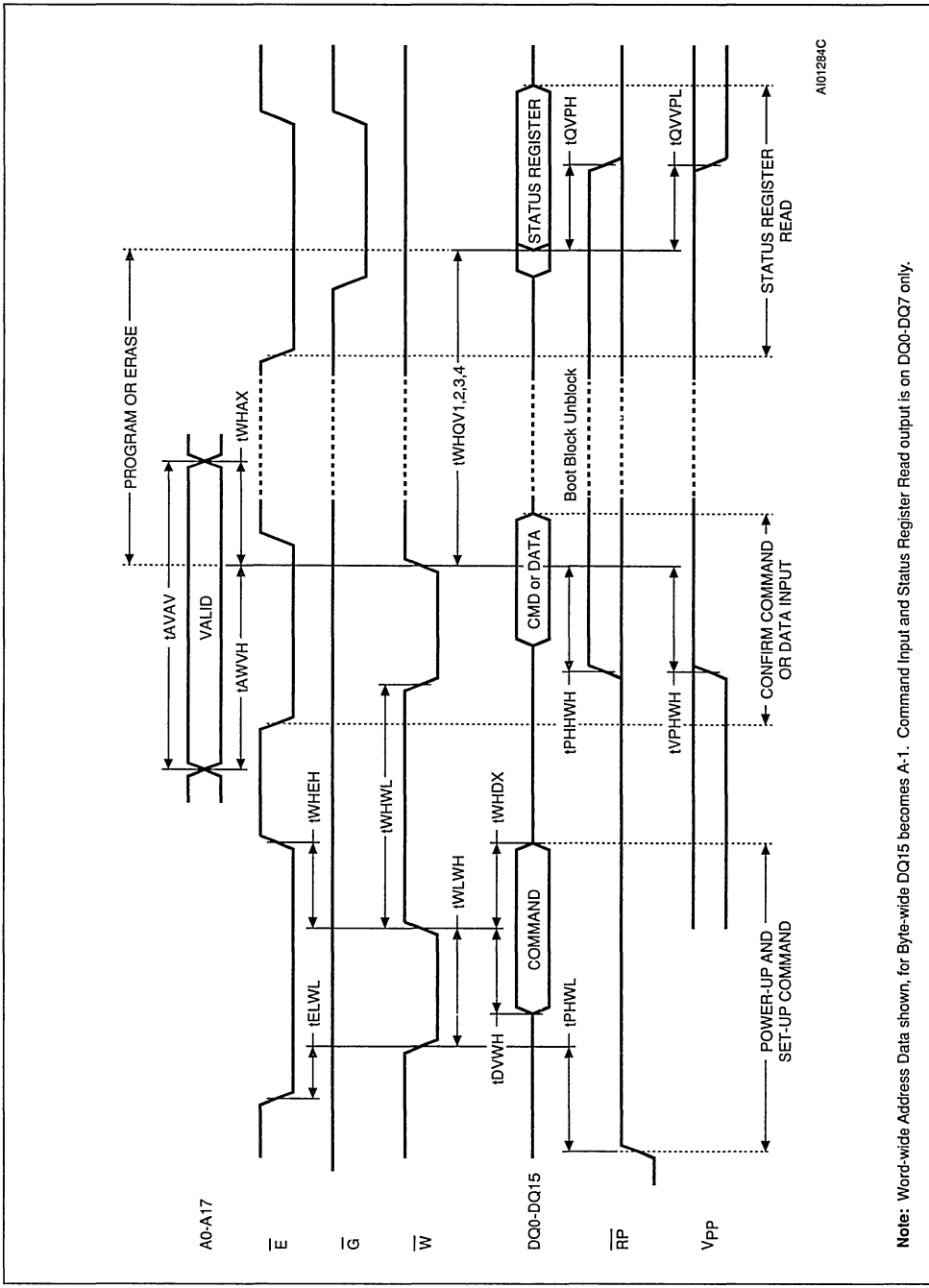
Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 18B. Write AC Characteristics, Write Enable Controlled (1)
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F410 / 420				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	60		70		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	40		50		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	60		60		ns
t_{PHHWH} (5)	t_{PHS}	Power Down VHH (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid (Word/Byte Program)	7		7		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Figure 8. Program & Erase AC Waveforms, $\overline{W}$ Controlled



Note: Word-wide Address Data shown, for Byte-wide DQ15 becomes A-1. Command Input and Status Register Read output is on DQ0-DQ7 only.

Table 19A. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F410 / 20				Unit
			-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	70		80		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	20		30		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	50		50		ns
t_{PHHEH} (5)	t_{PHS}	Power Down VHH (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid (Word/Byte Program)	6		6		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.3		0.3		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.6		0.6		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 19B. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F410 / 420				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	60		70		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	60		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	40		50		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	60		60		ns
t_{PHHEH} (5)	t_{PHS}	Power Down VHH (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid (Word/Byte Program)	7		7		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 20A. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F410 / 20				Unit
			-80		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	80		90		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	50		60		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	50		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	30		40		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	50		60		ns
t_{PHHEH} (5)	t_{PHS}	Power Down VHH (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid (Word/Byte Program)	6		7		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.3		0.4		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.3		0.4		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.6		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 20B. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F410 / 420				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	60		70		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	60		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	40		50		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	60		60		ns
t_{PHHEH} (5)	t_{PHS}	Power Down VHH (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid (Word/Byte Program)	7		7		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Figure 9. Program & Erase AC Waveforms, $\overline{E}$ Controlled

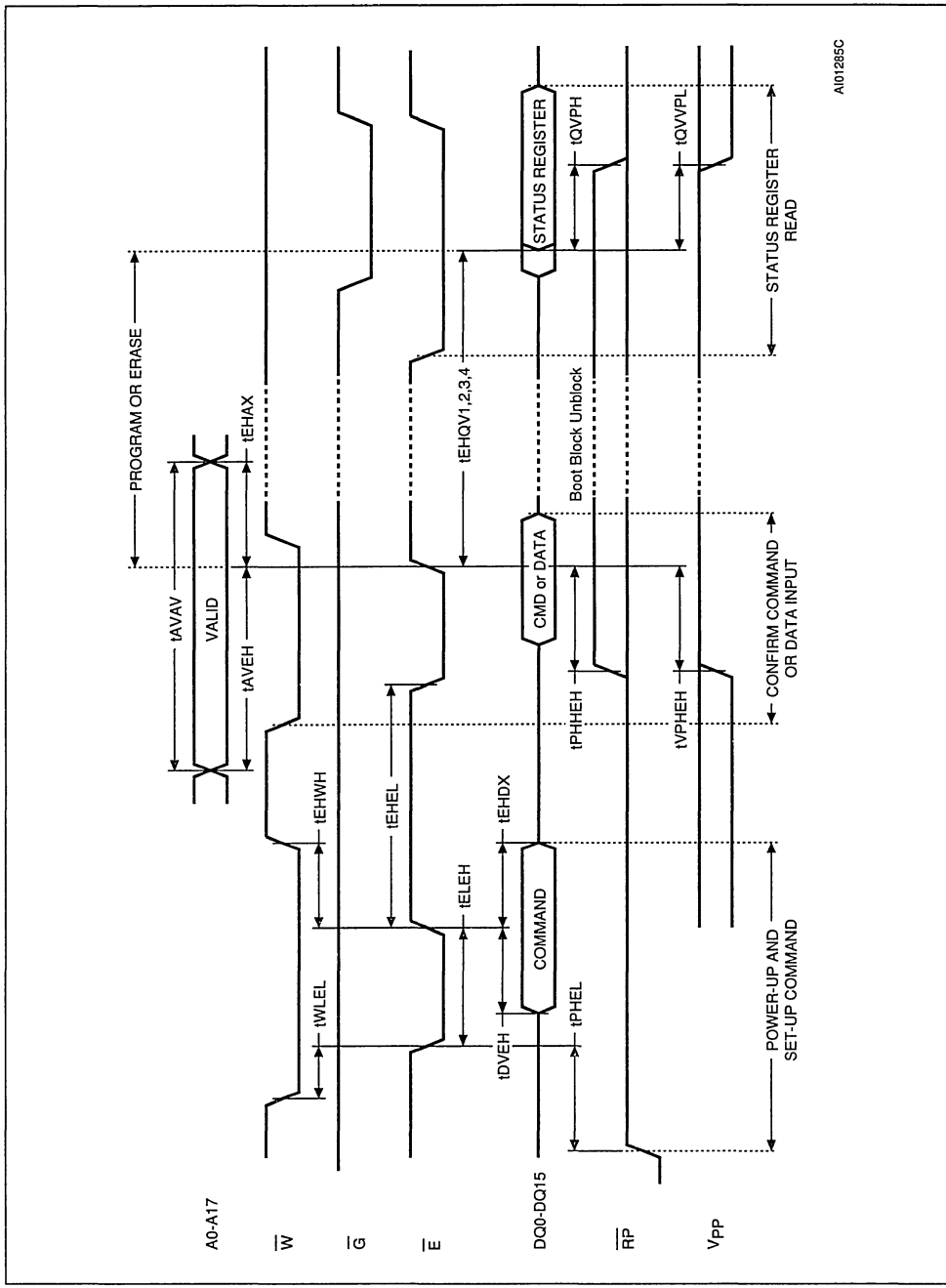


Table 21. Word/Byte Program, Erase Times
(T_A = 0 to 70°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	Test Conditions	M28F410 / 420			Unit
		Min	Typ	Max	
Main Block Program (Byte)	V_{PP} = 12V ±5%		1.2	4.2	sec
Main Block Program (Word)	V_{PP} = 12V ±5%		0.6	2.1	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±5%		1	7	sec
Main Block Erase	V_{PP} = 12V ±5%		2.4	14	sec

Table 22. Word/Byte Program, Erase Times
(T_A = –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	Test Conditions	M28F410 / 420			Unit
		Min	Typ	Max	
Main Block Program (Byte)	V_{PP} = 12V ±5%		1.4	5	sec
Main Block Program (Word)	V_{PP} = 12V ±5%		0.7	2.5	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±5%		1.5	10.5	sec
Main Block Erase	V_{PP} = 12V ±5%		3	18	sec

DEVICE OPERATION (cont'd)

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This is a tri-level input which locks the Boot Block from programming and erasure, and allows the memory to be put in deep power down.

When $\overline{RP}$ is High (up to 6.5V maximum) the Boot Block is locked and cannot be programmed or erased. When $\overline{RP}$ is above 11.4V the Boot Block is unlocked for programming or erasure. With $\overline{RP}$ Low the memory is in deep power down, and if $\overline{RP}$ is within V_{SS}+0.2V the lowest supply current is absorbed.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. It controls writing to the Command Register and Input Address and Data latches. Both Addresses and Data Inputs are latched on the rising edge of $\overline{W}$.

$\overline{BYTE}$ Byte/Word Organization Select. This input selects either byte-wide or word-wide organization of the memory. When $\overline{BYTE}$ is Low the memory is organized x8 or byte-wide and data input/output uses DQ0-DQ7 while A-1 acts as the additional, LSB, of the memory address that multiplexes the upper or lower byte. In the byte-wide organization DQ8-DQ14 are high impedance. When $\overline{BYTE}$ is High the memory is organized x16 and data input/output uses DQ0-DQ15 with the memory addressed by A0-A17.

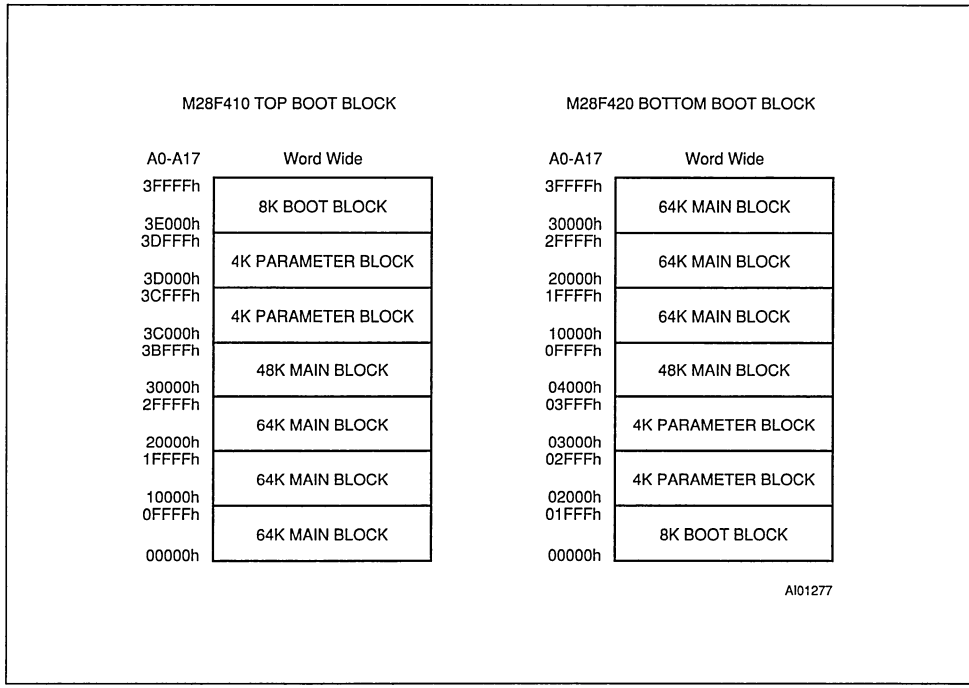
V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{PP} ±10% tolerance option is provided for application requiring maximum 100 write and erase cycles.

V_{CC} Supply Voltage. It is the main circuit supply.

V_{SS} Ground. It is the reference for all voltage measurements.

Figure 10. Memory Map, Word-wide Addresses



Memory Blocks

The memory blocks of the M28F410 and M28F420 are shown in Figure 10. The difference between the two products is simply an inversion of the block map to position the Boot Block at the top or bottom of the memory. The selection of the Boot Block at the top or bottom of the memory depends on the microprocessor needs.

Each block of the memory can be erased separately, but only by one block at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another block and then resumed.

Programming and erasure of the memory is disabled when the program supply is at V_{PPL}. For successful programming and erasure the program supply must be at V_{PPH}.

The Boot Block provides additional hardware security by use of the $\overline{RP}$ signal which must be at V_{HH} before any program or erase operation will be executed by the P/E.C. on the Boot Block.

Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down, and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. A read operation will output either a byte or a word depending on the $\overline{BYTE}$ signal level. When $\overline{BYTE}$ is Low the output byte is on DQ0-DQ7, DQ8-DQ14 are Hi-Z and A-1 is an additional address input. When $\overline{BYTE}$ is High the output word is on DQ0-DQ15.

The data read depends on the previous command written to the memory (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$. As for the Read operation, when $\overline{BYTE}$ is Low a byte is input, DQ8-DQ14 are 'don't care' and A-1 is an additional address. When $\overline{BYTE}$ is High a word is input.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is low. The power consumption is reduced to the Power Down level, and Outputs are in high impedance, independant of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memories, the manufacturer code for SGS-THOMSON is 20h, and the device codes are 0F2h for the M28F410 (Top Boot Block) and 0FAh for the M28F420 (Bottom Boot Block). These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product.

The Electronic Signature is output by a Read Array operation when the voltage applied to A9 is at V_{ID}, the manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored. The codes are output on DQ0-DQ7. When the $\overline{BYTE}$ signal is High the outputs DQ8-DQ15 output 00h, when Low these outputs are high impedance and Address input A-1 is ignored.

The Electronic Signature can also be read, without raising A9 to V_{ID}, after giving the memory the instruction RSIG (see below).

Instructions and Commands

The memories include a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from 1 to 3 operations, the first of which is always a write operation and is followed by either a further write operation to confirm the first command or a read operation(s) to output data.

A Status Register indicates the P/E.C. status Ready or Busy, the suspend/in-progress status of erase operations, the failure/success of erase and program operations and the low/correct value of the Program Supply voltage V_{PP}.

The P/E.C. automatically sets bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The register can be read by the Read Status Register (RSR) instruction and cleared by the Clear Status Register (CLRS) instruction. The meaning of the bits b3 to b7 is shown in Table 7. Bits b0 to b2 are reserved for future use (and should be masked out during status checks).

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read the addressed memory array content and output a byte or word depending on the level of the $\overline{BYTE}$ input.

Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent Read operations output the contents of the Status Register. The contents of the status register are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the Status Register.

Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h followed by two read operations to output the manufacturer and device codes. The manufacturer code, 20h, is output when the address line A0 is Low, and the device code, 0F2h for the M28F410 or 0FAh for the M28F420, when A0 is High.

Erase (EE) instruction. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second command is the Erase Confirm command 0D0h. During the input of the second command an address of the block to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 and b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the RSR (Read Status Register) and ES (Erase Suspend) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it has completed. After completion the Status Register bit b5 returns '1' if there has been an Erase Failure because erasure has not been verified even after the maximum number of erase cycles have been executed. Status Register bit b3 returns '1' if V_{PP} does not remain at V_{PPH} level when the erasure is attempted and/or proceeding.

V_{PP} must be at V_{PPH} when erasing, erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register (CLRS).

The Boot Block can only be erased when $\overline{RP}$ is also at V_{HH}.

Program (PG) instruction. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or 10h). A second write operation latches the Address and the Data to be written and starts the P/E.C. Read operations output the status register after the programming has started.

Memory programming is only made by writing '0' in place of '1' in a byte or word.

During the execution of the programming by the P/E.C., the memory accepts only the RSR (Read Status Register) instruction. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status Register bit b3 returns a '1' if V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming.

V_{PP} must be at V_{PPH} when programming, programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect. Then after having cleared the Status Register (CLRS), the memory must be erased and re-programmed.

The Boot Block can only be programmed when $\overline{RP}$ is at V_{HH}.

Clear Status Register (CLRS) instruction. The Clear Status Register uses a single write operation which clears bits b3, b4 and b5, if latched to '1' by the P/E.C., to '0'. Its use is necessary before any new operation when an error has been detected.

Erase Suspend (ES) instruction. The Erase operation may be suspended by this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates whether the erase has actually been suspended, b6 = '1', or whether the P/E.C. cycle was the last and the erase is completed, b6 = '0'.

During the suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Read operations initially output the status register while erase is suspended but, following a Read instruction, data from other blocks of the memory can be read. V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or the $\overline{RP}$ signal goes Low while erase is suspended then erase is aborted while bits b5 and b3 of the status register are set. Erase operation must be repeated after having cleared the status register, to be certain to erase the block.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 0D0h. The status register bit b6 is cleared when erasure resumes. Read operations output the status register after the erase is resumed.

The suggested flow charts for programs that use the programming, erasure and erase suspend/resume features of the memories are shown in Figure 11 to Figure 13.

Programming. The memory can be programmed byte-by-byte (or word-by-word in x16 organization). The Program Supply voltage V_{PP} must be applied before program instructions are given, and if the programming is in the Boot Block, $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Program Supply voltage may be applied continuously during programming.

The program sequence is started by writing a Program Set-up command (40h) to the Command Interface, this is followed by writing the address and data byte or word to the memory. The Program/Erase Controller automatically starts and performs the programming after the second write operation, providing that the V_{PP} voltage (and $\overline{RP}$ voltage if programming the Boot Block) are correct. During the programming the memory status is checked by reading the status register bit b7 which

shows the status of the P/E.C. Bit b7 = '1' indicates that programming is completed.

A full status check can be made after each byte/word or after a sequence of data has been programmed. The status check is made on bit b3 for any possible V_{PP} error and on bit b4 for any possible programming error.

Erase. The memory can be erased by blocks. The Program Supply voltage V_{PP} must be applied before the Erase instruction is given, and if the Erase is of the Boot Block $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Erase sequence is started by writing an Erase Set-up command (20h) to the Command Interface, this is followed by an address in the block to be erased and the Erase Confirm command (0D0h).

The Program/Erase Controller automatically starts and performs the block erase, providing the V_{PP} voltage (and the $\overline{RP}$ voltage if the erase is of the Boot Block) is correct. During the erase the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that erase is completed.

A full status check can be made after the block erase by checking bit b3 for any possible V_{PP} error, bits b5 and b6 for any command sequence errors (erase suspended) and bit b5 alone for an erase error.

Reset. Note that after any program or erase instruction has completed with an error indication or after any V_{PP} transitions down to V_{PPL} the Command Interface must be reset by a Clear Status Register Instruction before data can be accessed.

Automatic Power Saving

The M28F410 and M28F420 memories place themselves in a lower power state when not being accessed. Following a Read operation, after a delay equal to the memory access time, the Supply Current is reduced from a typical read current of 25mA (CMOS inputs, word-wide organization) to less than 2mA.

Power Down

The memories provide a power down control input $\overline{RP}$. When this signal is taken to below V_{SS} + 0.2V all internal circuits are switched off and the supply current drops to typically 0.2µA and the program current to typically 0.1µA. If $\overline{RP}$ is taken low during a memory read operation then the memory is deselected and the outputs become high impedance. If $\overline{RP}$ is taken low during a program or erase sequence then it is aborted and the memory content is no longer valid.

Recovery from deep power down requires 300ns to a memory read operation, or 210ns to a command write. On return from power down the status register is cleared to 00h.

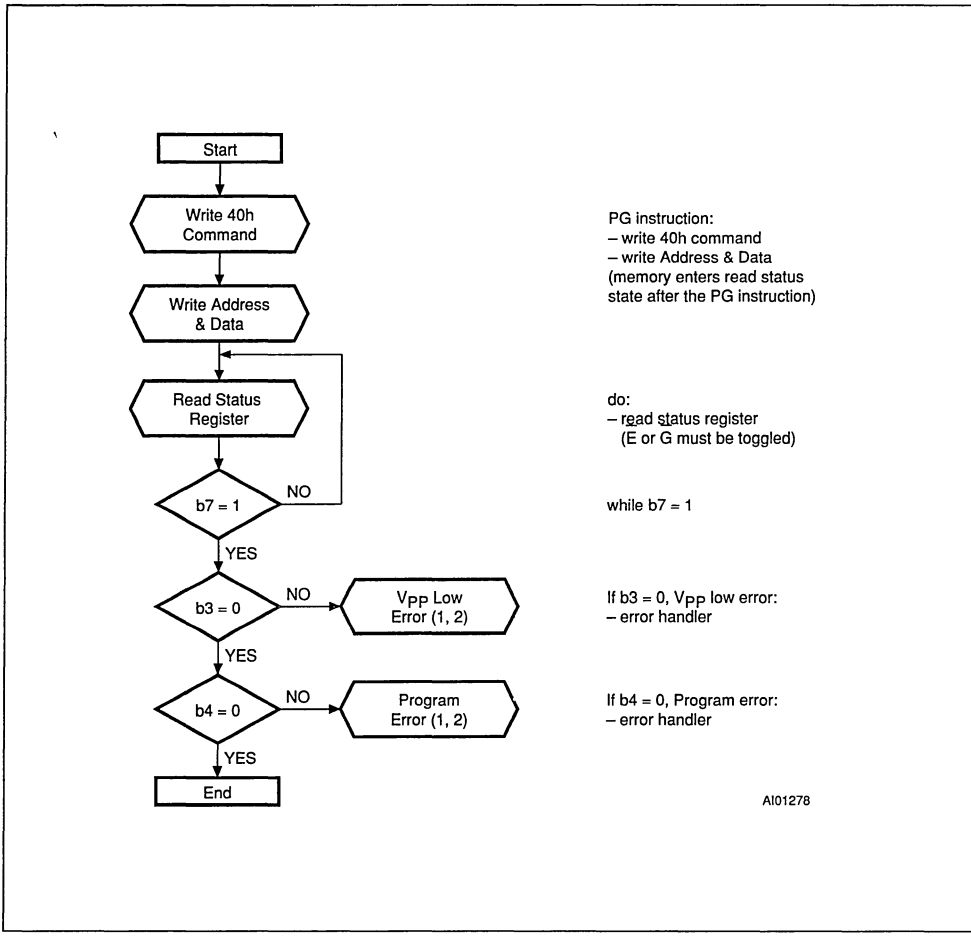
Power Up

The Supply voltage V_{CC} and the Program Supply voltage V_{PP} can be applied in any order. The memory Command Interface is reset on power up to Read Memory Array, but a negative transition of Chip Enable $\overline{E}$ or a change of the addresses is required to ensure valid data outputs. Care must be taken to avoid writes to the memory when V_{CC} is above V_{LKO} and V_{PP} powers up first. Writes can be inhibited by driving either $\overline{E}$ or $\overline{W}$ to V_{IH}. The memory is disabled until $\overline{RP}$ is up to V_{IH}.

Supply Rails

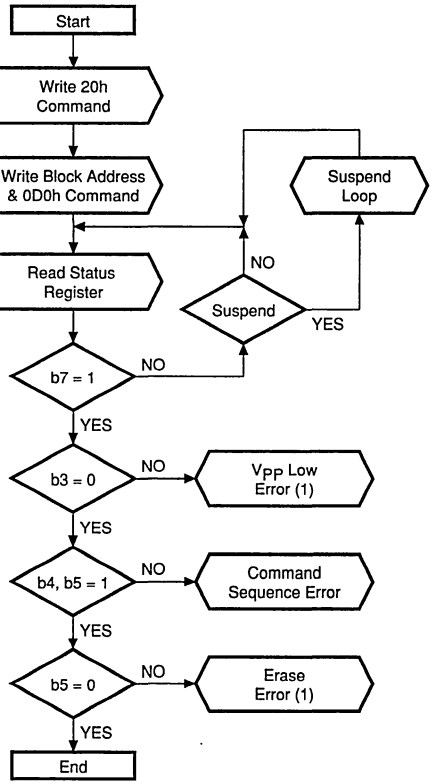
Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} and V_{PP} rails decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{PP} program and erase currents required.

Figure 11. Program Flow-chart and Pseudo Code



Notes: 1. Status check of b3 (V_{PP} Low) and b4 (Program Error) can be made after each byte/word programming or after a sequence.
2. If a V_{PP} Low or Program Erase is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 12. Erase Flow-chart and Pseudo Code



EE instruction:
– write 20h command
– write Block Address (A12-A17) & command 0D0h
(memory enters read status state after the EE instruction)

do:
– read status register ($\overline{E}$ or $\overline{G}$ must be toggled)
if EE instruction given execute suspend erase loop

while b7 = 1

If b3 = 0, V_{PP} low error:
– error handler

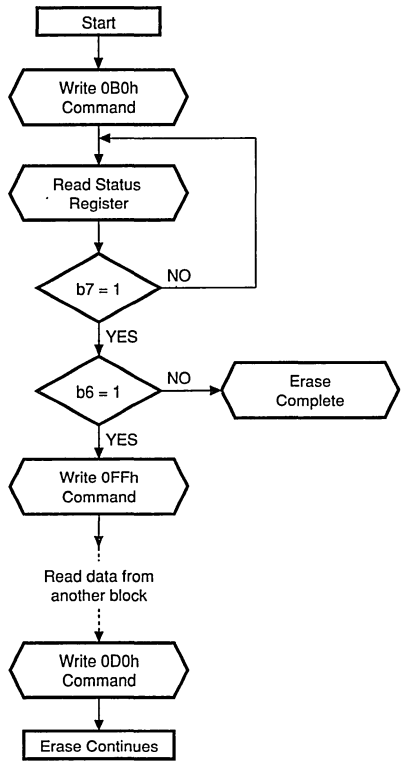
If b4, b5 = 0, Command Sequence error:
– error handler

If b5 = 0, Erase error:
– error handler

AI01279

Note: 1. If V_{PP} Low or Erase Error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 13. Erase Suspend & Resume Flow-chart and Pseudo Code



ES instruction:
– write 0B0h command
(memory enters read register state after the ES instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

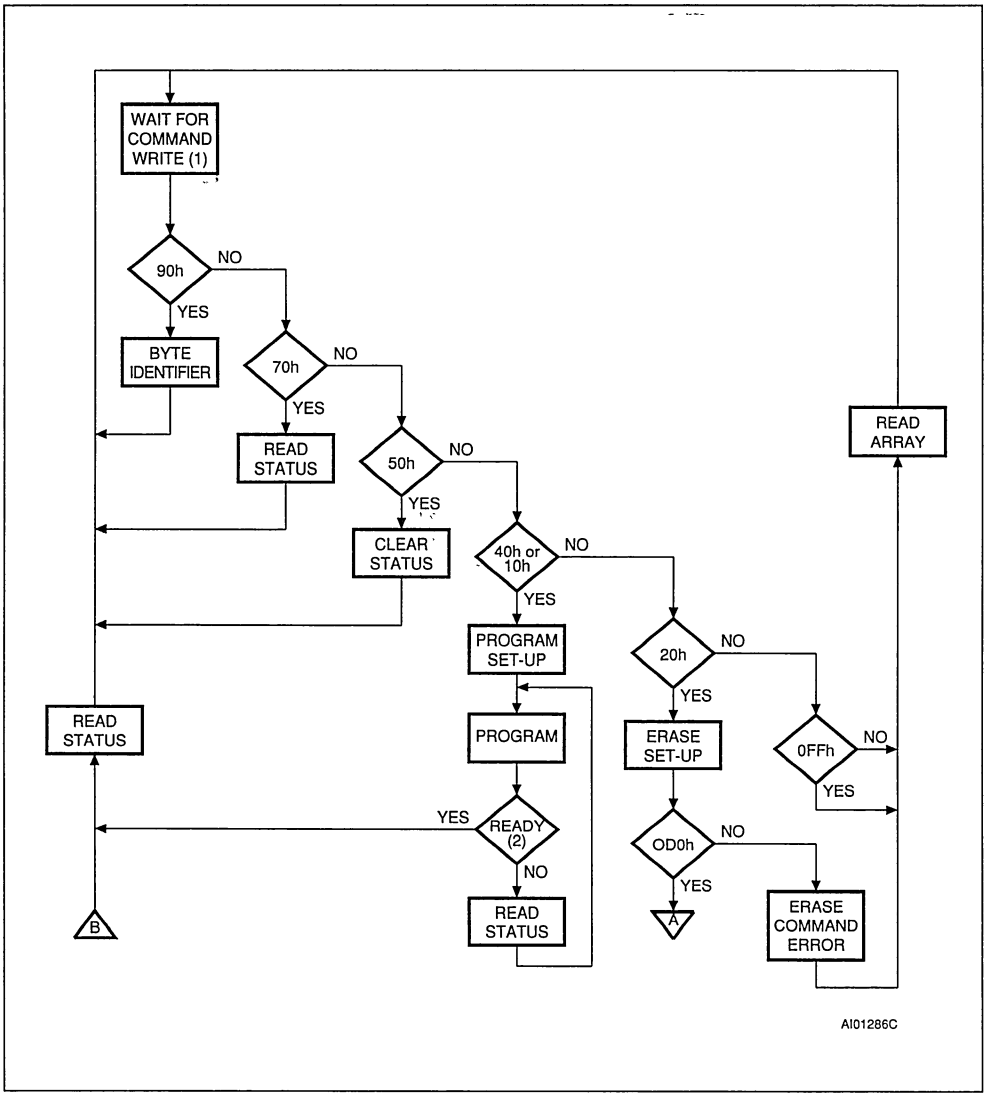
If b6 = 0, Erase completed
(at this point the memory wich accept only the RD or ER instruction)

RD instruction:
– write 0FFh command
– one o more data reads from another block

ER instruction:
– write 0D0h command to resume erasure

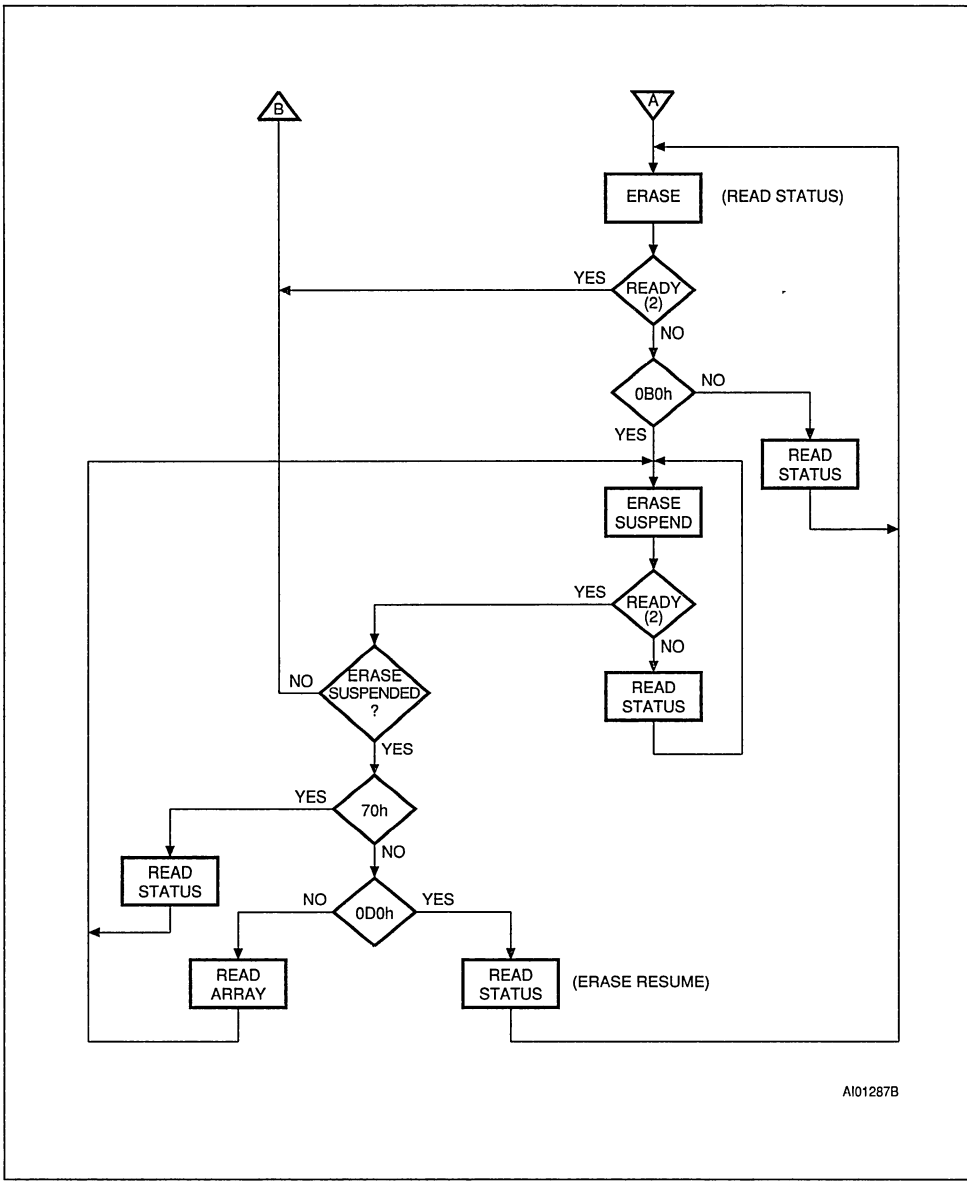
AI01280

Figure 14. Command Interface and Program Erase Controller Flow-diagram (a)



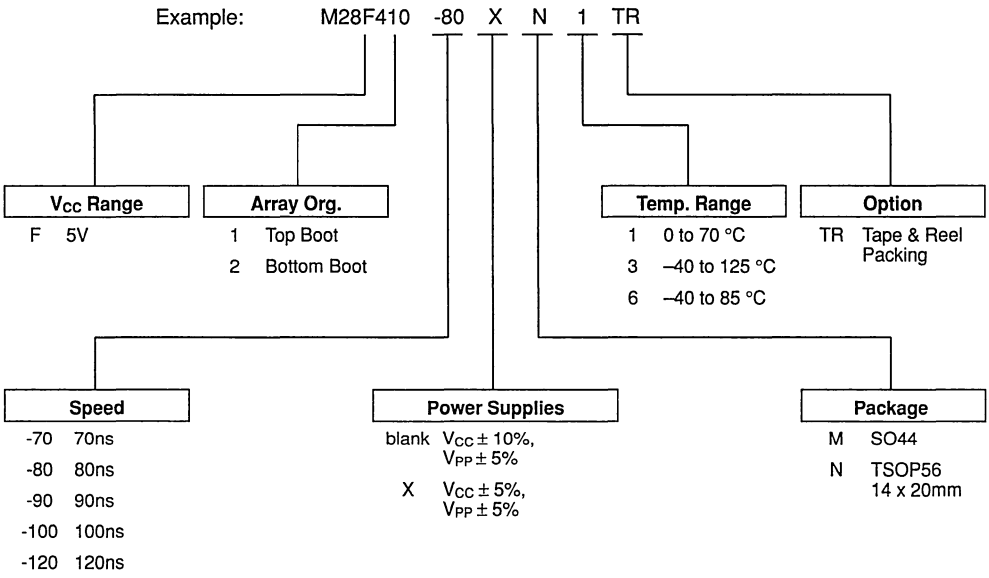
Notes: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 15. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME



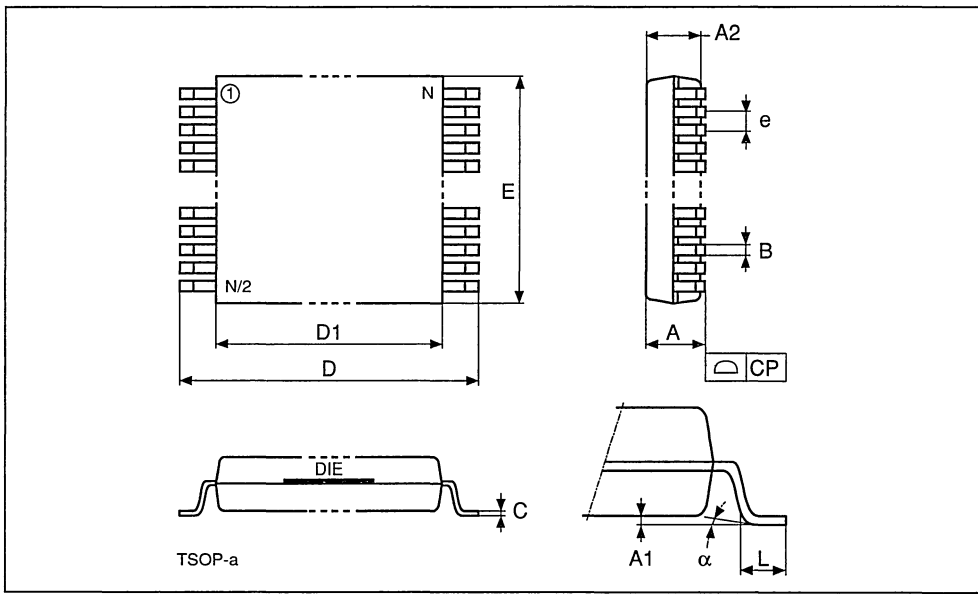
For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		13.90	14.10		0.547	0.555
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	56			56		
CP			0.10			0.004

TSOP56



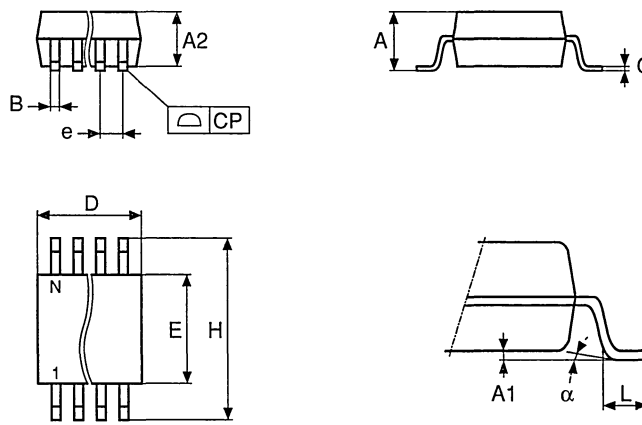
TSOP-a

Drawing is out of scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27			0.050		
H		15.90	16.10		0.626	0.634
L	0.80			0.031		
α	3°			3°		
N	44			44		
CP			0.10			0.004

SO44



SO-b

Drawing is out of scale

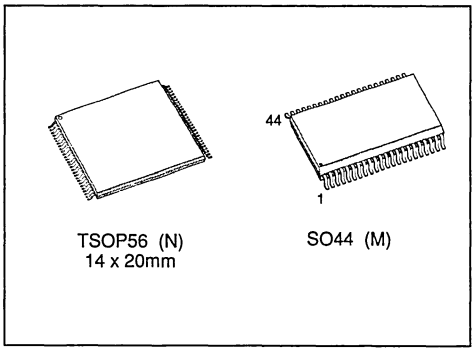
SGS-THOMSON MICROELECTRONICS

M28V410
M28V420

LOW VOLTAGE
4 Megabit (x8 or x16, Block Erase) FLASH MEMORY

PRODUCT PREVIEW

- DUAL x8 and x16 ORGANIZATION
- SMALL SIZE PLASTIC PACKAGES TSOP56 and SO44
- MEMORY ERASE in BLOCKS
  - One 16K Byte or 8K Word Boot Block (top or bottom location) with hardware write and erase protection
  - Two 8K Byte or 4K Word Key Parameter Blocks
  - One 96K Byte or 48K Word Main Block
  - Three 128K Byte or 64K Word Main Blocks
- 3.3V ± 0.3V SUPPLY VOLTAGE
- 12V ± 10% or 5% PROGRAMMING VOLTAGE
- 10,000 PROGRAM/ERASE CYCLES
- PROGRAM/ERASE CONTROLLER
- AUTOMATIC STATIC MODE
- LOW POWER CONSUMPTION
  - 2mA Typical in Static Operation
  - 55µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
  - 15/20mA Typical Operating Consumption (Byte/Word)
- HIGH SPEED ACCESS TIME: 120ns
- EXTENDED TEMPERATURE RANGES



TSOP56 (N)
14 x 20mm

SO44 (M)

Figure 1. Logic Diagram

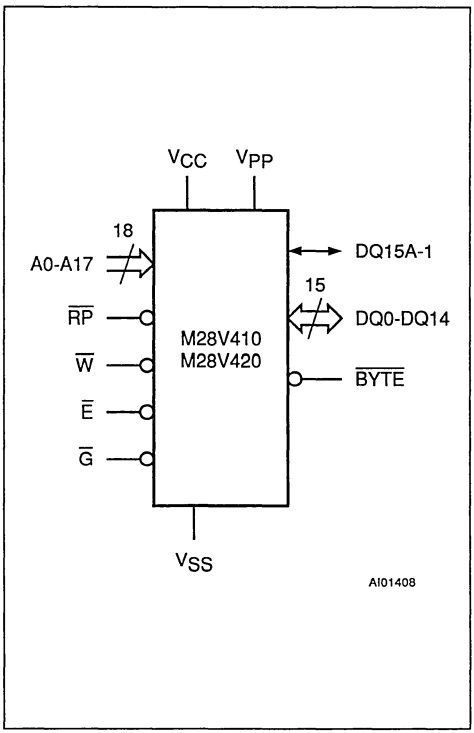
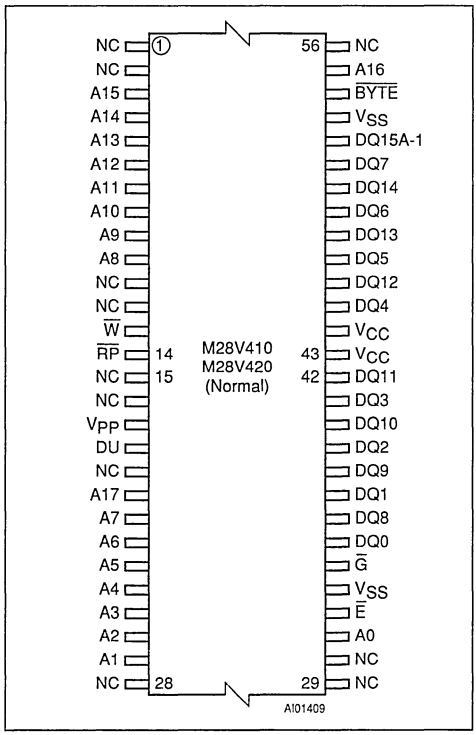


Table 1. Signal Names

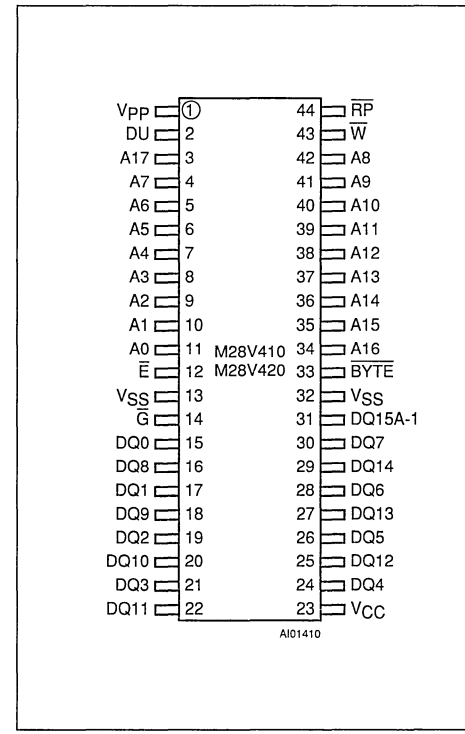
A0-A17	Address Inputs
DQ0-DQ7	Data Input / Outputs
DQ8-DQ14	Data Input / Outputs
DQ15A-1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{BYTE}$	Byte/Word Organization
$\overline{RP}$	Reset/Power Down/Boot Block Unlock
V_{PP}	Program & Erase Supply Voltage
V_{CC}	Supply Voltage

Figure 2A. TSOP Pin Connections



Warning: NC = No Connections, DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9} (2)	A9 Voltage		–0.6 to 13.5	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
V_{RP} (2)	$\overline{RP}$ Voltage		–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3 Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 7V allowed for less than 20ns

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{BYTE}$	DQ0 - DQ7	DQ8 - DQ14	DQ15A-1
Read Word	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Data Output	Data Output	Data Output
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Hi-Z	Address Input
Write Word	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Data Input	Data Input	Data Input
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data Input	Hi-Z	Address Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	X	Hi-Z	Hi-Z	Hi-Z
Power Down	X	X	X	V_{IL}	X	Hi-Z	Hi-Z	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}

Table 4. Electronic Signature

Organi-sation	Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{BYTE}$	A0	A9	A1-A8 & A10-A17	DQ0 - DQ7	DQ8 - DQ14	DQ15 A-1
Word-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{ID}	Don't Care	20h	00h	0
	Device Code	M28V410	V_{IL}	VIL	VIH	VIH	VIH	VID	Don't Care	0F3h	00h	0
		M28V420	V_{IL}	VIL	VIH	VIH	VIH	VID	Don't Care	0FBh	00h	0
Byte-wide	Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h	Hi-Z	Don't Care
	Device Code	M28V410	V_{IL}	VIL	VIH	VIL	VIH	VID	Don't Care	0F3h	Hi-Z	Don't Care
		M28V420	V_{IL}	VIL	VIH	VIL	VIH	VID	Don't Care	0FBh	Hi-Z	Don't Care

Note: $\overline{RP}$ = V_{IH}

DESCRIPTION

The M28V410 and M28V420 FLASH MEMORIES are non-volatile memories that may be erased electrically at the block level and programmed by byte or word. The interface is directly compatible with most microprocessors. SO44 and TSOP56 packages are used.

Organization

The organization, as 512K x 8 or 256K x 16, is selectable by an external $\overline{BYTE}$ signal. When $\overline{BYTE}$ is Low and the x8 organization is selected, the Data Input/Output signal DQ15 acts as Address line A-1 and selects the lower or upper byte of the memory word for output on DQ0-DQ7, DQ8-DQ14 remain high impedance. When $\overline{BYTE}$ is High the memory uses the Address inputs A0-A17 and the Data Input/Outputs DQ0-DQ15. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down/Boot block unlock, tri-level input, places the memory in deep power down, normal operation or enables programming and erasure of the Boot block.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data (4)	Operation	Address	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Signature
EE	Erase	2	Write	X	20h	Write	Block Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSR or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of Read cycle can occur after one command cycle.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.
4. When word organization is used, upper byte is don't care for command input.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Array

Blocks

Erasure of the memories is in blocks. There are 7 blocks in the memory address space, one Boot Block of 16K Bytes or 8K Words, two 'Key Parameter Blocks' of 8K Bytes or 4K Words, one 'Main Block' of 96K Bytes or 48K Words, and three 'Main Blocks' of 128K Bytes or 64K Words. The M28V410 memory has the Boot Block at the top of the memory address space (3FFFFh) and the M28V420 locates the Boot Block starting at the bottom (00000h). Erasure of each block takes typically 1 second and each block can be programmed and erased over 10,000 cycles.

The Boot Block is hardware protected from accidental programming or erasure depending on the $\overline{RP}$ signal. Program/Erase commands in the Boot Block are executed only when $\overline{RP}$ is at 12V. Block erasure may be suspended while data is read from other blocks of the memory, then resumed.

Bus Operations

Six operations can be performed by the appropriate bus cycles, Read Byte or Word from the Array, Read Electronic Signature, Output Disable, Standby, Power Down and Write the Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor the memory's status. When power

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits b4 or b5 for Program or Erase Success
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction P/ECS and ESS bits are set to '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte or word.
			'0'	Program Success	
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction has been executed.
			'0'	V_{PP} OK	
	2	Reserved			
	1	Reserved			
	0	Reserved			

Notes: Logic level '1' is High, '0' is Low.

is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte or word program and block erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte or word programming takes typically 9µs, block erase typically 1 second. Erasure of a memory block may be suspended in order to read data from another block and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation.

Power Saving

The M28V410 and M28V420 have a number of power saving features. Following a Read access the memory enters a static mode in which the supply current is typically 2mA. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down ($\overline{RP}$) signals are at V_{CC}, when the supply current drops to typically 60µA. A deep power down mode is enabled when the Reset/Power Down ($\overline{RP}$) signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 700ns maximum, with instructions to the C.I. recognised after only 580ns.

Table 8. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

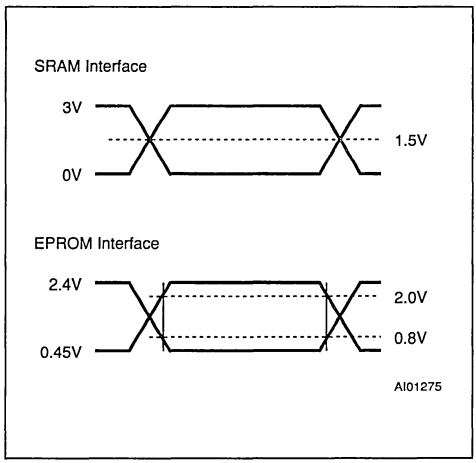


Figure 4. AC Testing Load Circuit

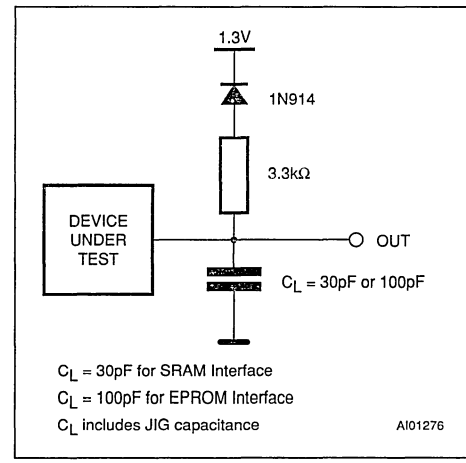


Table 9. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

DEVICE OPERATION

Signal Descriptions

A0-A17 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

A9 Address Input is also used for the Electronic Signature Operation. When A9 is raised to 12V the Electronic Signature may be read. The A0 signal is used to read two words or bytes, when A0 is Low the Manufacturer code is read and when A0 is High the Device code. When $\overline{BYTE}$ is Low DQ0-DQ7 output the codes and DQ8-DQ15 are don't care, when $\overline{BYTE}$ is High DQ0-DQ7 output the codes and DQ8-DQ15 output 00h.

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte or the lower byte of a word to be programmed or a command to the C.I., are latched when both Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output from the memory Array, the Electronic Signature or Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

DQ8-DQ14 and DQ15A-1 Data Input/Outputs. These input/outputs are used in the word-wide organization. When $\overline{BYTE}$ is High for the most significant byte of the input or output, functioning as described for DQ0-DQ7 above. When $\overline{BYTE}$ is Low, DQ8-DQ14 are high impedance, DQ15A-1 is the Address A-1 input.

Table 10. DC Characteristics
(T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V±5% or 12V±10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read Byte-wide) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		40	mA
I_{CC} (1, 3)	Supply Current (Read Word-wide) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		45	mA
I_{CC} (1, 3)	Supply Current (Read Byte-wide) CMOS	$\overline{E} = V_{SS}$, $\overline{G} = V_{SS}$, f = 5MHz		35	mA
	Supply Current (Read Word-wide) CMOS	$\overline{E} = V_{SS}$, $\overline{G} = V_{SS}$, f = 5MHz		40	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$, $\overline{BYTE} = V_{CC} \pm 0.2V$ or V_{SS}		150	µA
I_{CC2} (3)	Supply Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{CC3}	Supply Current (Program Byte-wide)	Byte program in progress		50	mA
	Supply Current (Program Word-wide)	Word program in progress		60	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Leakage Current (Read or Standby)	$V_{PP} \le V_{CC}$		±15	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program Byte-wide)	Byte program in progress		30	mA
I_{PP3}	Program Current (Program Word-wide)	Word program in progress		40	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –2mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	4.1	V
V_{PPH}	Program Voltage (Program or Erase operations) 5% range		11.4	12.6	V
	Program Voltage (Program or Erase operations) 10% range		10.8	13.2	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 2mA typical in static operation.
2. Current increases to I_{CC} + I_{CC5} during a read operation.
3. CMOS levels V_{CC} ± 0.2V and V_{SS} ± 0.2V. TTL levels V_{IH} and V_{IL}.

Table 11. Read AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V±5% or 12V±10%)

Symbol	Alt	Parameter	Test Condition	M28V410 / 420						Unit
				-120		-150		-180		
				SRAM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		150		180		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		180	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		700		700		700	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		180	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		60		65		70	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		50		55		60	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		45		50		55	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 5. Read Mode AC Waveforms

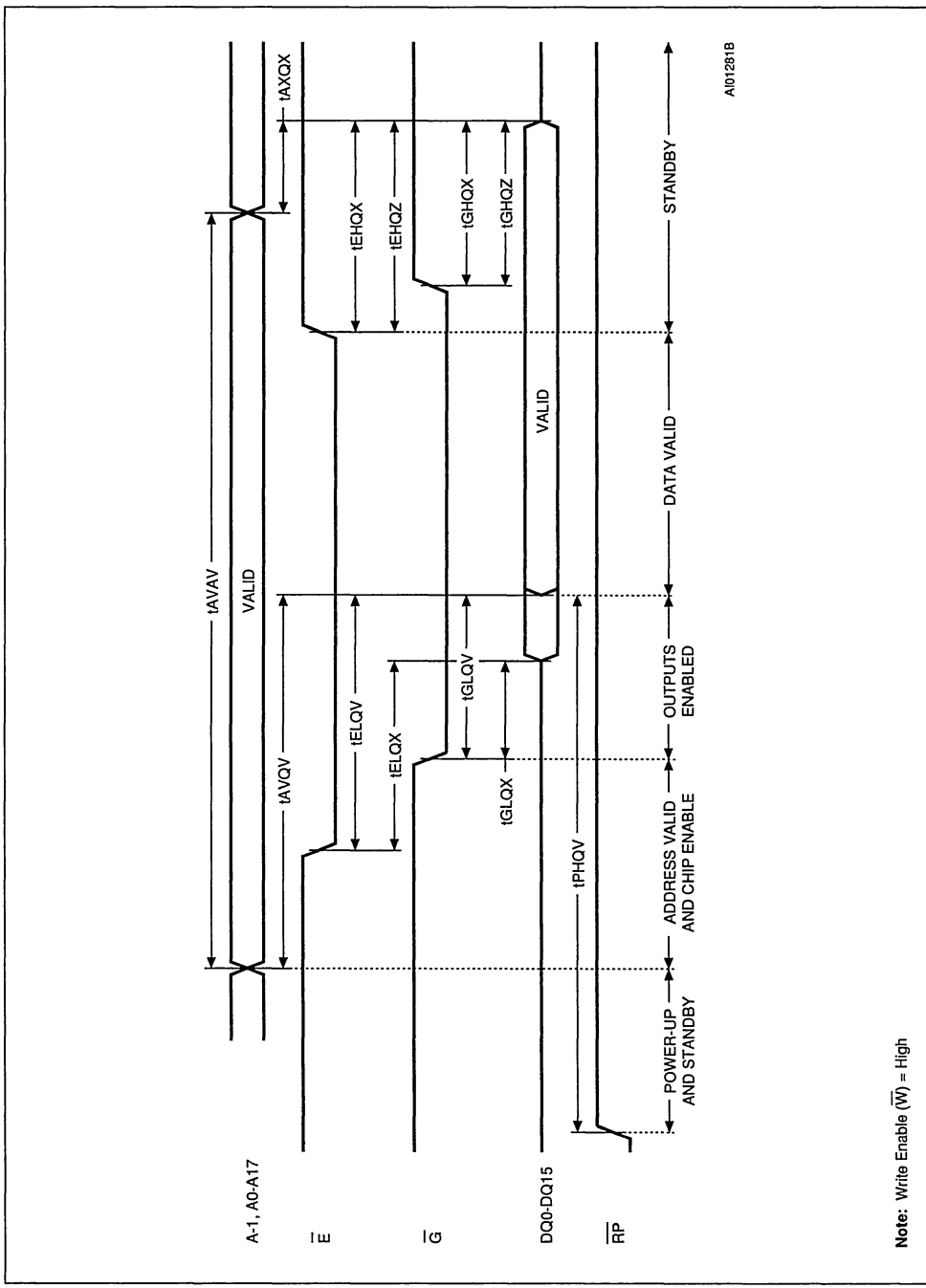
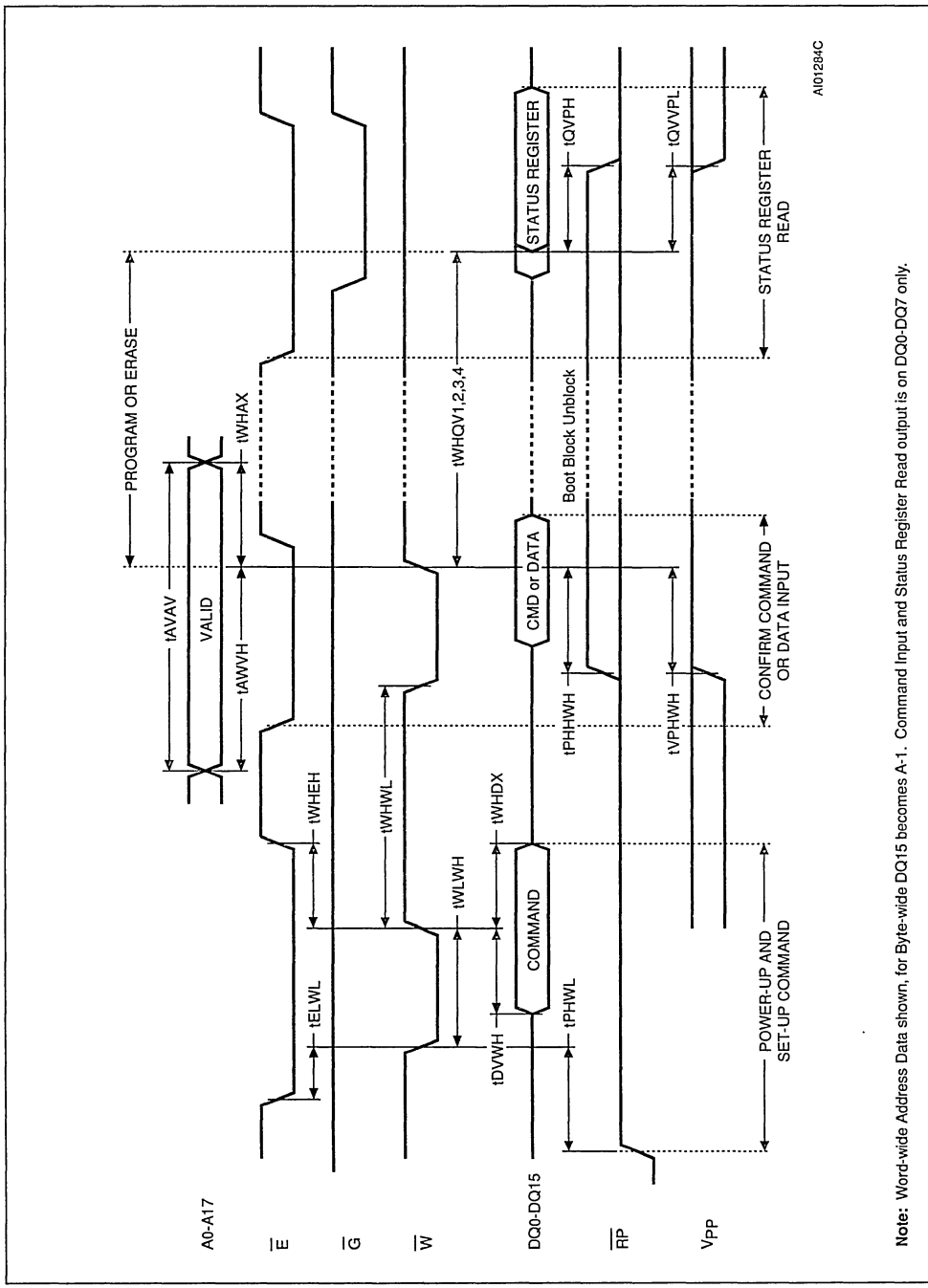


Table 12. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V±5% or 12V±10%)

Symbol	Alt	Parameter	M28V410 / 420						Unit
			-120		-150		-180		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	120		150		180		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	1		1		1		µs
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	100		100		100		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	100		100		100		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	50		50		50		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	95		95		95		ns
t_{PHHWH}	t_{PHS}	Power Down VHH (Boot Block Unlock) to Write Enable High	200		200		200		ns
t_{VPHWH}	t_{VPS}	V_{PP} High to Write Enable High	200		200		200		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		10		ns
t_{WHQV1} (1, 2)		Write Enable High to Output Valid (Word/Byte Program)	6		6		6		µs
t_{WHQV2} (1, 2)		Write Enable High to Output Valid (Boot Block Erase)	0.3		0.3		0.3		sec
t_{WHQV3} (1)		Write Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		0.3		sec
t_{WHQV4} (1)		Write Enable High to Output Valid (Main Block Erase)	0.6		0.6		0.6		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		200		200		200	ns

Notes: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Figure 6. Program & Erase AC Waveforms, $\overline{W}$ Controlled



Note: Word-wide Address Data shown, for Byte-wide DQ15 becomes A-1. Command Input and Status Register Read output is on DQ0-DQ7 only.

Table 13. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V±5% or 12V±10%)

Symbol	Alt	Parameter	M28V410 / 420						Unit
			-120		-150		-180		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	120		150		180		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	1		1		1		µs
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	100		100		100		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	100		100		100		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	50		50		50		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	95		95		95		ns
t_{PHHEH}	t_{PHS}	Power Down VHH (Boot Block Unlock) to Chip Enable High	200		200		200		ns
t_{VPHEH}	t_{VPS}	V_{PP} High to Chip Enable High	200		200		200		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		10		ns
t_{EHQV1} (1, 2)		Chip Enable High to Output Valid (Word/Byte Program)	6		6		6		µs
t_{EHQV2} (1, 2)		Chip Enable High to Output Valid (Boot Block Erase)	0.3		0.3		0.3		sec
t_{EHQV3} (1)		Chip Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		0.3		sec
t_{EHQV4} (1)		Chip Enable High to Output Valid (Main Block Erase)	0.6		0.6		0.6		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		200		200		200	ns

Note: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Figure 7. Program & Erase AC Waveforms, $\overline{E}$ Controlled

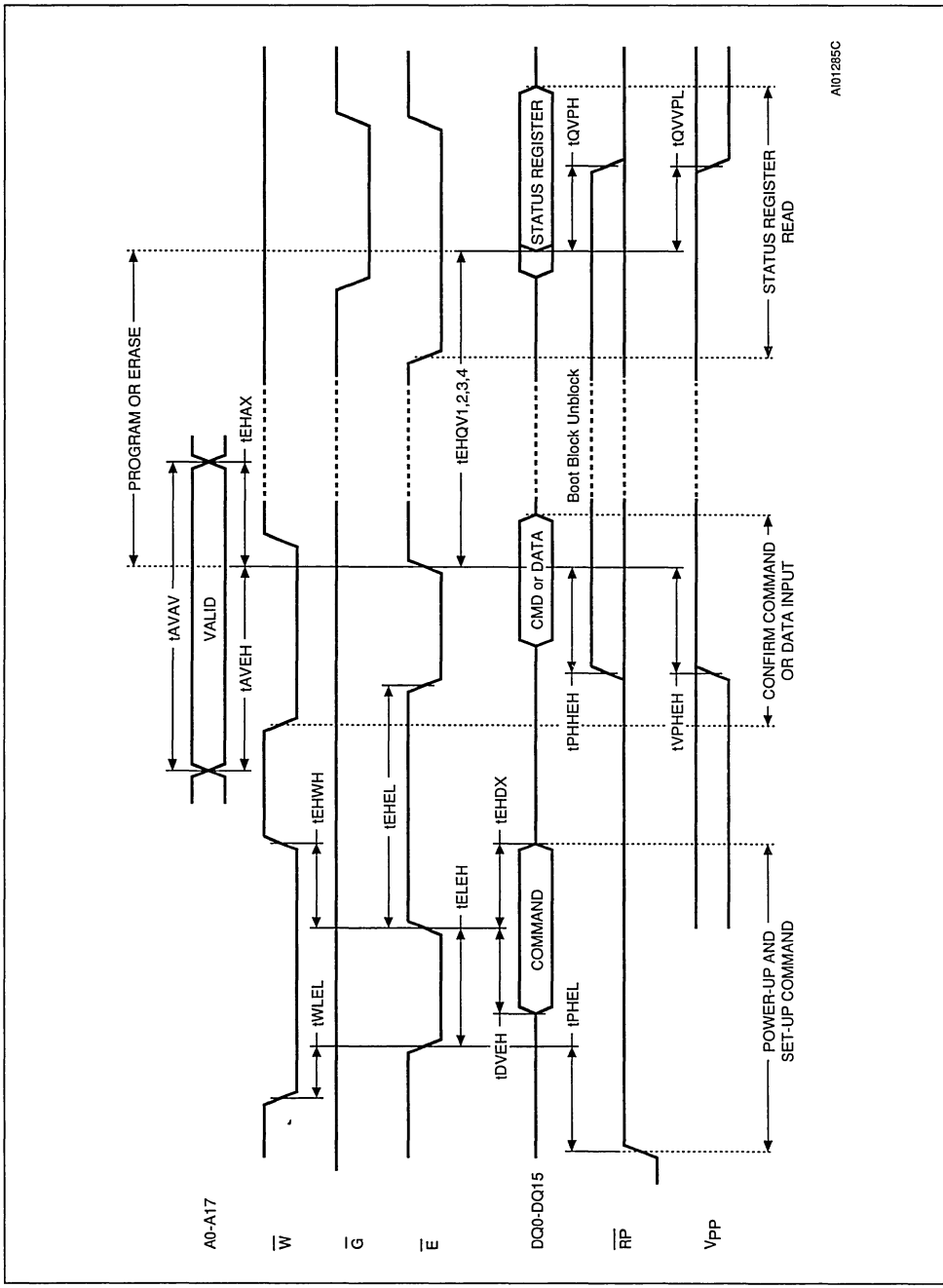


Table 14. Word/Byte Program, Erase Times
(T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V)

Parameter	Test Conditions	M28V410 / 420			Unit
		Min	Typ	Max	
Main Block Program (Byte)	V_{PP} = 12V ±5%		1.2	4.2	sec
Main Block Program (Word)	V_{PP} = 12V ±5%		0.6	2.1	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±5%		1	7	sec
Main Block Erase	V_{PP} = 12V ±5%		2.4	14	sec
Main Block Program (Byte)	V_{PP} = 12V ±10%		6	20	sec
Main Block Program (Word)	V_{PP} = 12V ±10%		3	10	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±10%		5.8	40	sec
Main Block Erase	V_{PP} = 12V ±10%		14	60	sec

DEVICE OPERATION (cont'd)

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This is a tri-level input which locks the Boot Block from programming and erasure, and allows the memory to be put in deep power down.

When $\overline{RP}$ is High (up to 6.5V maximum) the Boot Block is locked and cannot be programmed or erased. When $\overline{RP}$ is above 11.4V the Boot Block is unlocked for programming or erasure. With $\overline{RP}$ Low the memory is in deep power down, and if $\overline{RP}$ is within V_{SS}+0.2V the lowest supply current is absorbed.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. It controls writing to the Command Register and Input Address and Data latches. Both Addresses and Data Inputs are latched on the rising edge of $\overline{W}$.

$\overline{BYTE}$ Byte/Word Organization Select. This input selects either byte-wide or word-wide organization of the memory. When $\overline{BYTE}$ is Low the memory is organized x8 or byte-wide and data input/output uses DQ0-DQ7 while A-1 acts as the additional, LSB, of the memory address that multiplexes the upper or lower byte. In the byte-wide organization DQ8-DQ14 are high impedance. When $\overline{BYTE}$ is High the memory is organized x16 and data input/output uses DQ0-DQ15 with the memory addressed by A0-A17.

V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{PP} ±10% tolerance option is provided for application requiring maximum 100 write and erase cycles.

V_{CC} Supply Voltage. It is the main circuit supply.

V_{SS} Ground. It is the reference for all voltage measurements.

Memory Blocks

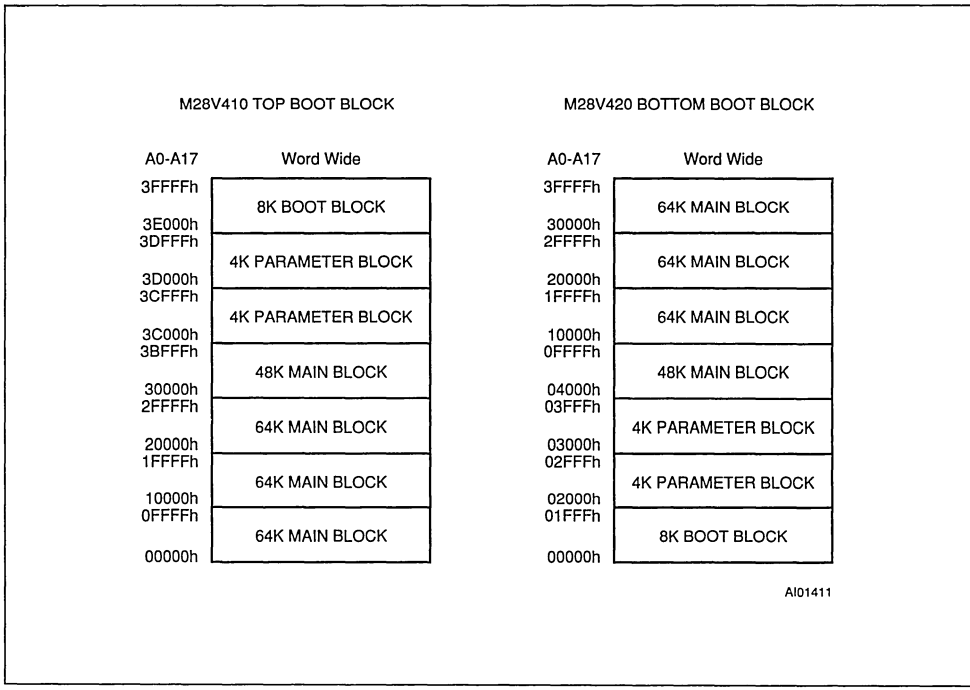
The memory blocks of the M28V410 and M28V420 are shown in Figure 8. The difference between the two products is simply an inversion of the block map to position the Boot Block at the top or bottom of the memory. The selection of the Boot Block at the top or bottom of the memory depends on the microprocessor needs.

Each block of the memory can be erased separately, but only by one block at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another block and then resumed.

Programming and erasure of the memory is disabled when the program supply is at V_{PPL}. For successful programming and erasure the program supply must be at V_{PPH}.

The Boot Block provides additional hardware security by use of the $\overline{RP}$ signal which must be at V_{HH} before any program or erase operation will be executed by the P/E.C. on the Boot Block.

Figure 8. Memory Map, Word-wide Addresses



Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down, and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. A read operation will output either a byte or a word depending on the $\overline{BYTE}$ signal level. When $\overline{BYTE}$ is Low the output byte is on DQ0-DQ7, DQ8-DQ14 are Hi-Z and A-1 is an additional address input. When $\overline{BYTE}$ is High the output word is on DQ0-DQ15.

The data read depends on the previous command written to the memory (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$. As for the Read operation, when $\overline{BYTE}$ is Low a byte is input, DQ8-DQ14 are 'don't care' and A-1 is an additional address. When $\overline{BYTE}$ is High a word is input.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is low. The power consumption is reduced to the Power Down level, and Outputs are in high impedance, independant of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memories, the manufacturer code for SGS-THOMSON is 20h, and the device codes are 0F3h for the M28V410 (Top Boot Block) and 0FBh for the M28V420 (Bottom Boot Block). These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product.

The Electronic Signature is output by a Read Array operation when the voltage applied to A9 is at V_{ID}, the manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored. The codes are output on DQ0-DQ7. When the $\overline{BYTE}$ signal is High the outputs DQ8-DQ15 output 00h, when Low these outputs are high impedance and Address input A-1 is ignored.

The Electronic Signature can also be read, without raising A9 to V_{ID}, after giving the memory the instruction RSIG (see below).

Instructions and Commands

The memories include a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from 1 to 3 operations, the first of which is always a write operation and is followed by either a further write operation to confirm the first command or a read operation(s) to output data.

A Status Register indicates the P/E.C. status Ready or Busy, the suspend/in-progress status of erase operations, the failure/success of erase and program operations and the low/correct value of the Program Supply voltage V_{PP}.

The P/E.C. automatically sets bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The register can be read by the Read Status Register (RSR) instruction and cleared by the Clear Status Register (CLRS) instruction. The meaning of the bits b3 to b7 is shown in Table 7. Bits b0 to b2 are reserved for future use (and should be masked out during status checks).

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read the addressed memory array content and output a byte or word depending on the level of the $\overline{BYTE}$ input.

Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent Read operations output the contents of the Status Register. The contents of the status register are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the Status Register.

Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h followed by two read operations to output the manufacturer and device codes. The manufacturer code, 20h, is output when the address line A0 is Low, and the device code, 0F3h for the M28V410 or 0FBh for the M28V420, when A0 is High.

Erase (EE) instruction. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second command is the Erase Confirm command 0D0h. During the input of the second command an address of the block to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 and b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the RSR (Read Status Register) and ES (Erase Suspend) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it has completed. After completion the Status Register bit b5 returns '1' if there has been an Erase Failure because erasure has not been verified even after the maximum number of erase cycles have been executed. Status Register bit b3 returns '1' if V_{PP} does not remain at V_{PPH} level when the erasure is attempted and/or proceeding.

V_{PP} must be at V_{PPH} when erasing, erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register (CLRS).

The Boot Block can only be erased when $\overline{RP}$ is also at V_{HH}.

Program (PG) instruction. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or 10h). A second write operation latches the Address and the Data to be written and starts the P/E.C. Read operations output the status register after the programming has started.

Memory programming is only made by writing '0' in place of '1' in a byte or word.

DEVICE OPERATION (cont'd)

During the execution of the programming by the P/E.C., the memory accepts only the RSR (Read Status Register) instruction. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status Register bit b3 returns a '1' if V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming.

V_{PP} must be at V_{PPH} when programming, programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect. Then after having cleared the Status Register (CLRS), the memory must be erased and re-programmed.

The Boot Block can only be programmed when $\overline{RP}$ is at V_{HH}.

Clear Status Register (CLRS) instruction. The Clear Status Register uses a single write operation which clears bits b3, b4 and b5, if latched to '1' by the P/E.C., to '0'. Its use is necessary before any new operation when an error has been detected.

Erase Suspend (ES) instruction. The Erase operation may be suspended by this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates whether the erase has actually been suspended, b6 = '1', or whether the P/E.C. cycle was the last and the erase is completed, b6 = '0'.

During the suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Read operations initially output the status register while erase is suspended but, following a Read instruction, data from other blocks of the memory can be read. V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or the $\overline{RP}$ signal goes Low while erase is suspended then erase is aborted while bits b5 and b3 of the status register are set. Erase operation must be repeated after having cleared the status register, to be certain to erase the block.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 0D0h. The status register bit b6 is cleared when erasure resumes. Read operations output the status register after the erase is resumed.

The suggested flow charts for programs that use the programming, erasure and erase suspend/resume features of the memories are shown in Figure 9 to Figure 11.

Programming. The memory can be programmed byte-by-byte (or word-by-word in x16 organization). The Program Supply voltage V_{PP} must be applied before program instructions are given, and if the programming is in the Boot Block, $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Program Supply voltage may be applied continuously during programming.

The program sequence is started by writing a Program Set-up command (40h) to the Command Interface, this is followed by writing the address and data byte or word to the memory. The Program/Erase Controller automatically starts and performs the programming after the second write operation, providing that the V_{PP} voltage (and $\overline{RP}$ voltage if programming the Boot Block) are correct. During the programming the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that programming is completed.

A full status check can be made after each byte/word or after a sequence of data has been programmed. The status check is made on bit b3 for any possible V_{PP} error and on bit b4 for any possible programming error.

Erase. The memory can be erased by blocks. The Program Supply voltage V_{PP} must be applied before the Erase instruction is given, and if the Erase is of the Boot Block $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Erase sequence is started by writing an Erase Set-up command (20h) to the Command Interface, this is followed by an address in the block to be erased and the Erase Confirm command (0D0h).

The Program/Erase Controller automatically starts and performs the block erase, providing the V_{PP} voltage (and the $\overline{RP}$ voltage if the erase is of the Boot Block) is correct. During the erase the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that erase is completed.

A full status check can be made after the block erase by checking bit b3 for any possible V_{PP} error, bits b5 and b6 for any command sequence errors (erase suspended) and bit b5 alone for an erase error.

Reset. Note that after any program or erase instruction has completed with an error indication or after any V_{PP} transitions down to V_{PPL} the Command Interface must be reset by a Clear Status Register Instruction before data can be accessed.

Automatic Power Saving

The M28V410 and M28V420 memories place themselves in a lower power state when not being accessed. Following a Read operation, after a delay equal to the memory access time, the Supply Current is reduced from a typical read current of 20mA (CMOS inputs, word-wide organization) to less than 2mA.

Power Down

The memories provide a power down control input $\overline{RP}$. When this signal is taken to below V_{SS} + 0.2V all internal circuits are switched off and the supply current drops to typically 0.2µA and the program current to typically 0.1µA. If $\overline{RP}$ is taken low during a memory read operation then the memory is deselected and the outputs become high impedance. If $\overline{RP}$ is taken low during a program or erase sequence then it is aborted and the memory content is no longer valid.

Recovery from deep power down requires 700ns to a memory read operation, or 580ns to a command write. On return from power down the status register is cleared to 00h.

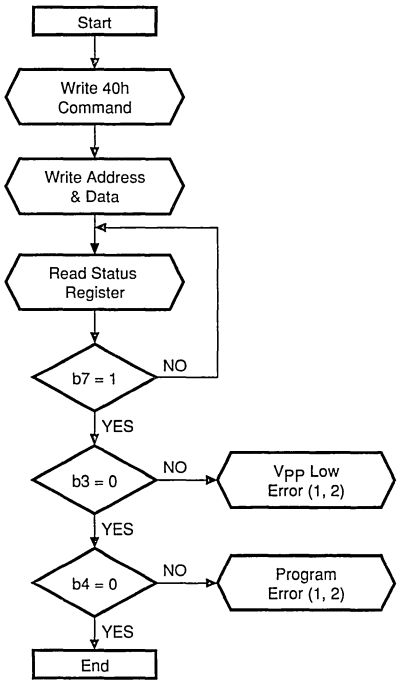
Power Up

The Supply voltage V_{CC} and the Program Supply voltage V_{PP} can be applied in any order. The memory Command Interface is reset on power up to Read Memory Array, but a negative transition of Chip Enable $\overline{E}$ or a change of the addresses is required to ensure valid data outputs. Care must be taken to avoid writes to the memory when V_{CC} is above V_{LKO} and V_{PP} powers up first. Writes can be inhibited by driving either $\overline{E}$ or $\overline{W}$ to V_{IH}. The memory is disabled until $\overline{RP}$ is up to V_{IH}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} and V_{PP} rails decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{PP} program and erase currents required.

Figure 9. Program Flow-chart and Pseudo Code



PG instruction:
– write 40h command
– write Address & Data
(memory enters read status state after the PG instruction)

do:
– read status register
(E or G must be toggled)

while b7 = 1

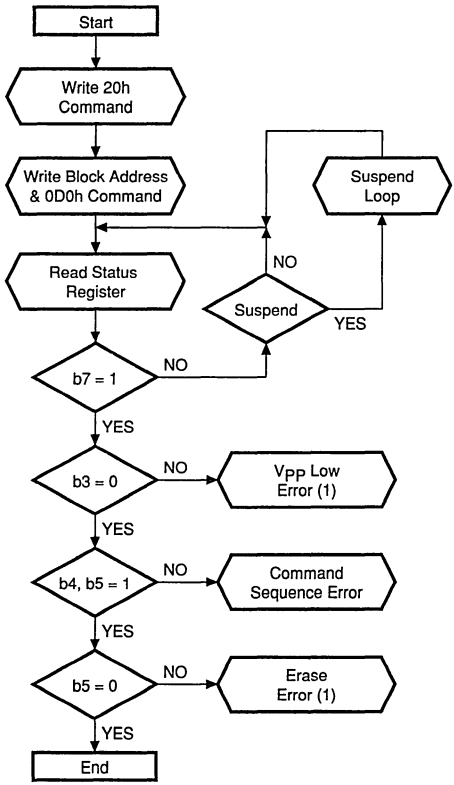
If b3 = 0, V_{PP} low error:
– error handler

If b4 = 0, Program error:
– error handler

AI01278

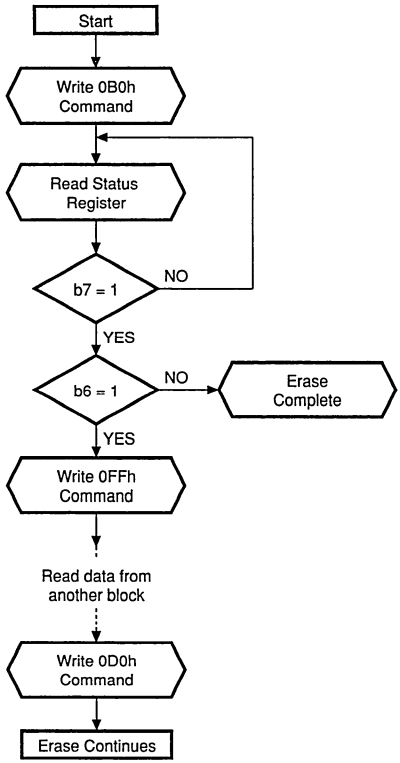
Notes: 1. Status check of b3 (V_{PP} Low) and b4 (Program Error) can be made after each byte/word programming or after a sequence.
2. If a V_{PP} Low or Program Erase is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 10. Erase Flow-chart and Pseudo Code



Note: 1. If V_{PP} Low or Erase Error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 11. Erase Suspend & Resume Flow-chart and Pseudo Code



ES instruction:
– write 0B0h command
(memory enters read register state after the ES instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

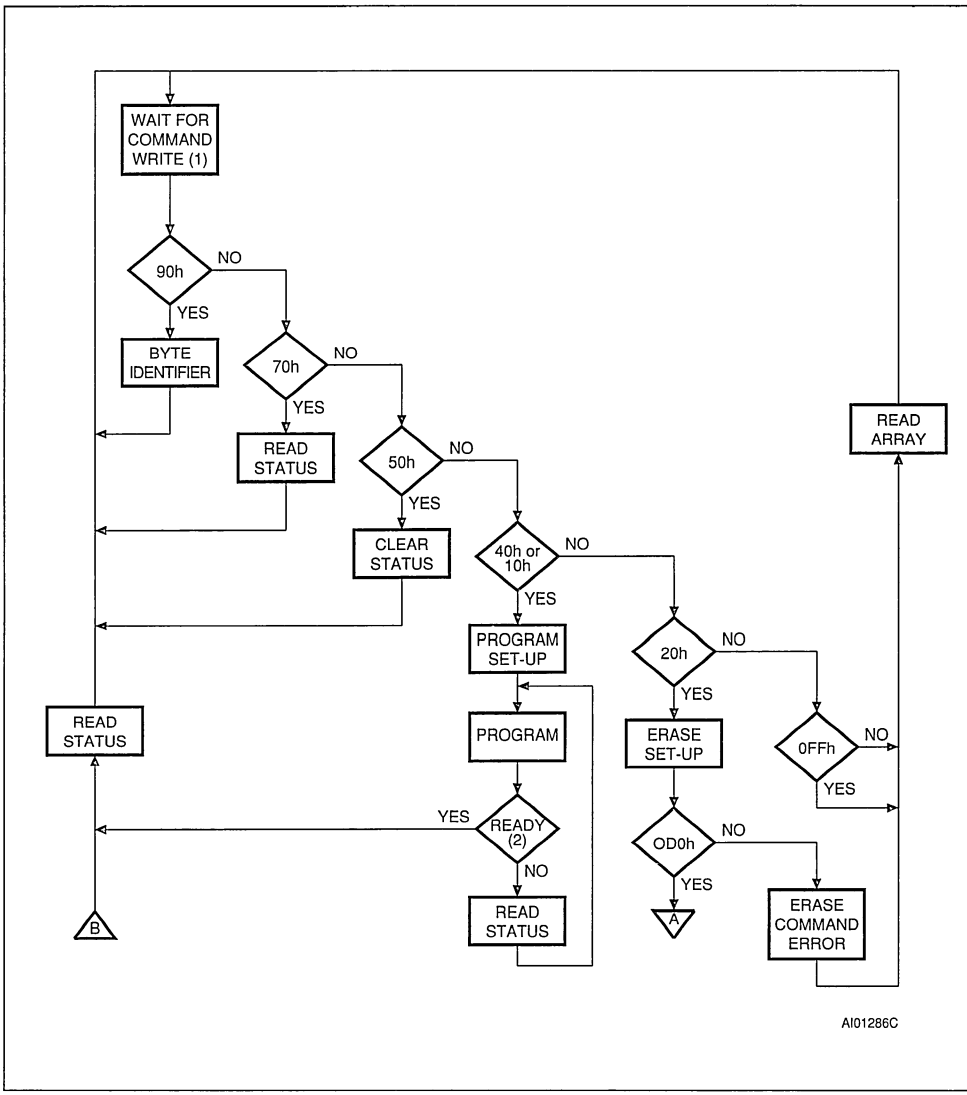
If b6 = 0, Erase completed
(at this point the memory wich accept only the RD or ER instruction)

RD instruction:
– write 0FFh command
– one o more data reads from another block

ER instruction:
– write 0D0h command
to resume erasure

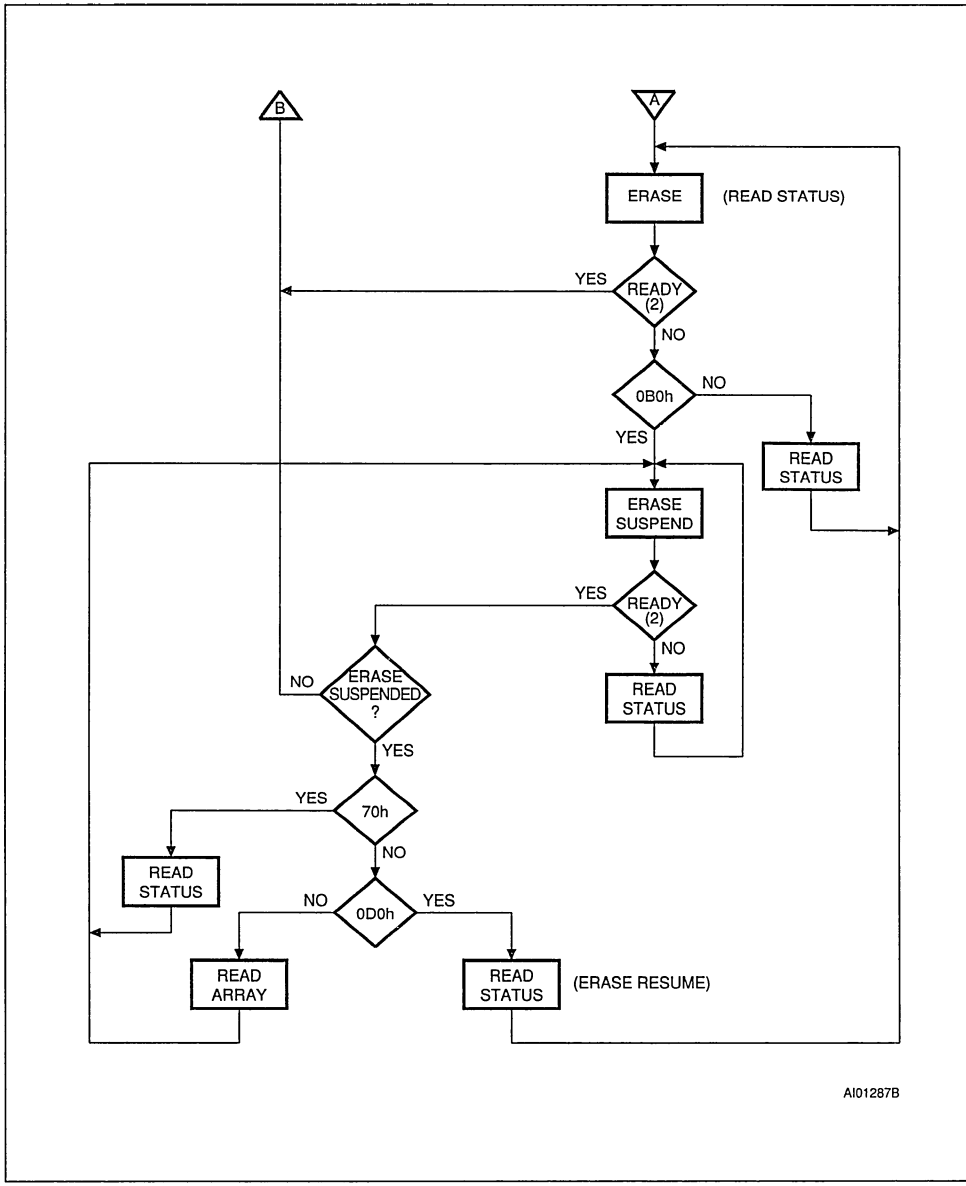
AI01280

Figure 12. Command Interface and Program Erase Controller Flow-diagram (a)



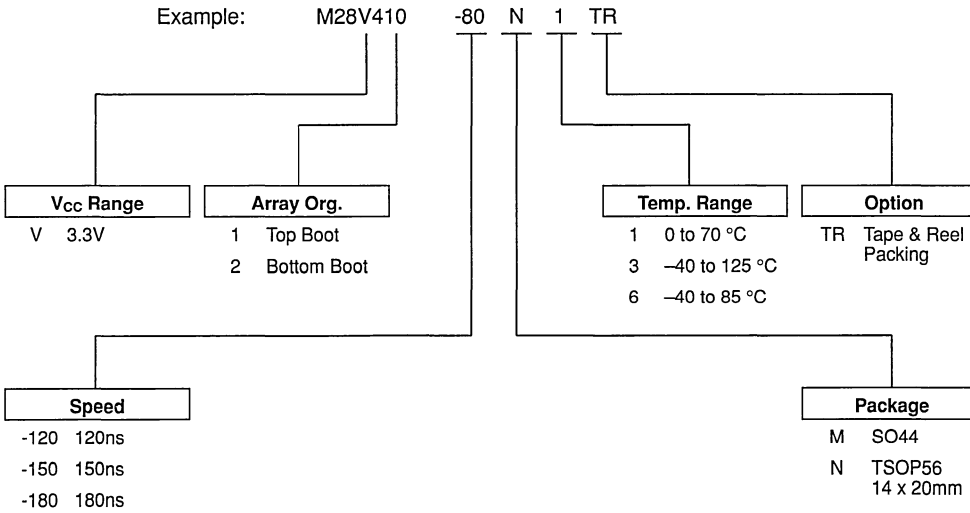
Notes: 1 If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode
2 P/E C. status (Ready or Busy) is read on Status Register bit 7.

Figure 13. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME



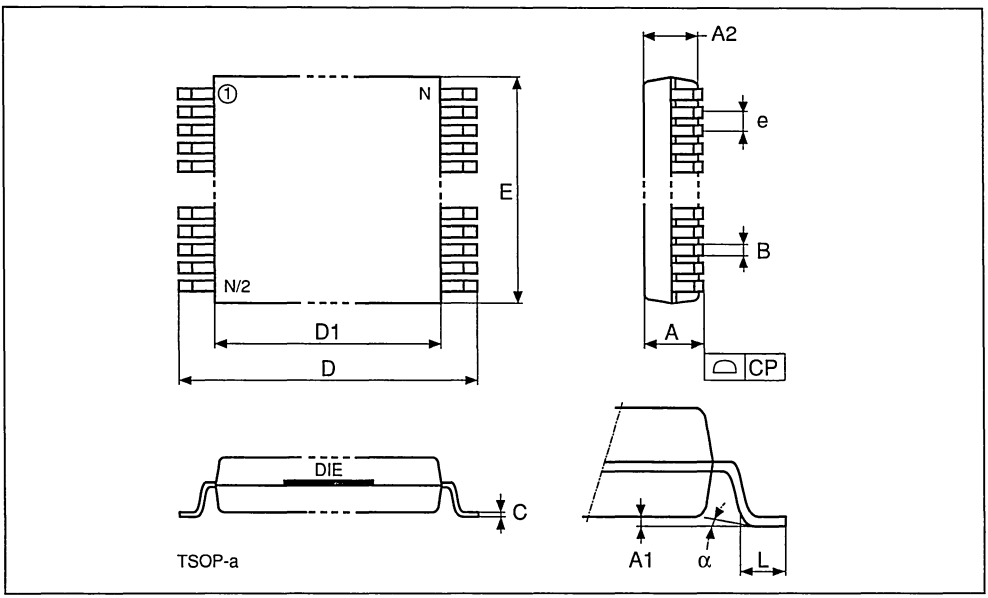
For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		13.90	14.10		0.547	0.555
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		56			56	
CP			0.10			0.004

TSOP56

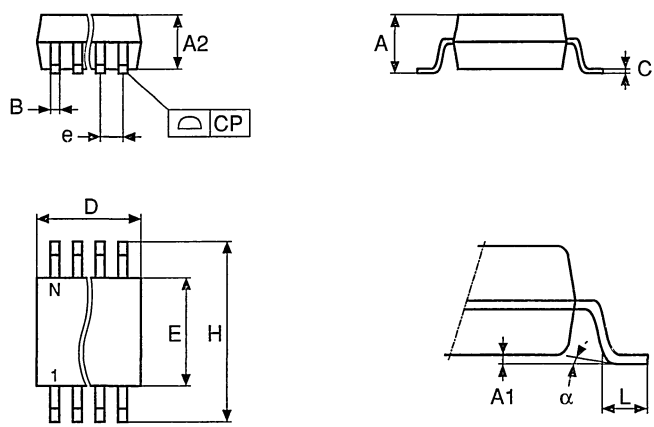


Drawing is out of scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27			0.050		
H		15.90	16.10		0.626	0.634
L	0.80			0.031		
α	3°			3°		
N	44			44		
CP			0.10			0.004

SO44



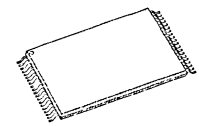
SO-b

Drawing is out of scale

4 Megabit (x 8, Block Erase) FLASH MEMORY

PRELIMINARY DATA

- SMALL SIZE PLASTIC PACKAGE TSOP40
- MEMORY ERASE in BLOCKS
  - One 16K Byte Boot Block (top or bottom location) with hardware write and erase protection
  - Two 8K Byte Key Parameter Blocks
  - One 96K Byte Main Block
  - Three 128K Byte Main Blocks
- 5V ± 10% SUPPLY VOLTAGE
- 12V ± 5% PROGRAMMING VOLTAGE
- 100,000 PROGRAM/ERASE CYCLES
- PROGRAM/ERASE CONTROLLER
- AUTOMATIC STATIC MODE
- LOW POWER CONSUMPTION
  - 60µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
  - 20/25mA Typical Operating Consumption
- HIGH SPEED ACCESS TIME: 70ns
- EXTENDED TEMPERATURE RANGES



TSOP40 (N)
10 x 20mm

DESCRIPTION

The M28F411 and M28F421 FLASH MEMORIES are non-volatile memories that may be erased electrically at the block level and programmed by byte.

Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power Down/Boot Block Unlock
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

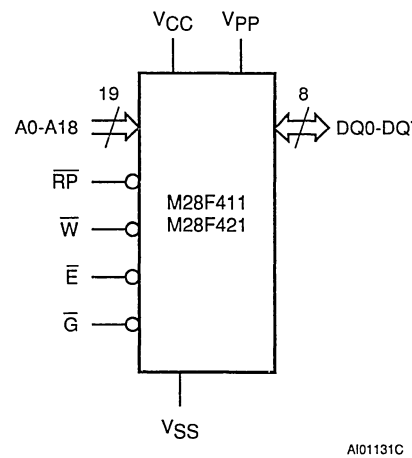
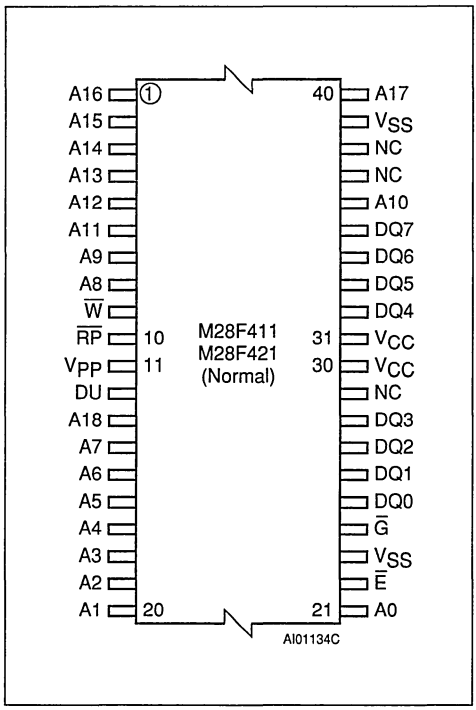


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 5 grade 6	0 to 70 –40 to 125 –20 to 85 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9} (2)	A9 Voltage		–0.6 to 13.5	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
V_{RP} (2)	$\overline{RP}$ Voltage		–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 7V allowed for less than 20ns.

Figure 2. TSOP Pin Connections



Warning: NC = No Connections, DU = Don't Use

DEVICE OPERATION (cont'd)

The interface is directly compatible with most microprocessors. TSOP40 (10 x 20mm) package is used.

Organization

The M28F411 and M28F421 are organized as 512K x 8. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down/Boot block unlock, tri-level input, places the memory in deep power down, normal operation or enables programming and erasure of the Boot block.

Blocks

Erasure of the memories is in blocks. There are 7 blocks in the memory address space, one Boot Block of 16K Bytes, two 'Key Parameter Blocks' of 8K Bytes, one 'Main Block' of 96K Bytes, and three 'Main Blocks' of 128K Bytes. The M28F411 memory has the Boot Block at the top of the memory address space (7FFFFh) and the M28F421 locates the Boot Block starting at the bottom (00000h). Erasure of each block takes typically 1 second and each block can be programmed and erased over 100,000 cycles.

The Boot Block is hardware protected from accidental programming or erasure depending on the $\overline{RP}$ signal. Program/Erase commands in the Boot Block are executed only when $\overline{RP}$ is at 12V.

Block erasure may be suspended while data is read from other blocks of the memory, then resumed.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	DQ0 - DQ7
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data Output
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	Hi-Z
Power Down	X	X	X	V_{IL}	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}

Table 4. Electronic Signature

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A9	A1-A8 & A10-A18	DQ0 - DQ7
Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	Don't Care	20h
Device Code	M28F411	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0F6h
	M28F421	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	Don't Care	0FEh

Note: $\overline{RP}$ = V_{IH}

Bus Operations

Six operations can be performed by the appropriate bus cycles, Read Byte from the Array, Read Electronic Signature, Output Disable, Standby, Power Down and Write the Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor the memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and block erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte programming takes typically 9µs, block erase typically 1 second. Erasure of a memory block may be suspended in order to read data from another block and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation.

Power Saving

The M28F411 and M28F421 have a number of power saving features. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down ($\overline{RP}$) signals are at V_{CC}, when the supply current drops to typically 60µA. A deep power down mode is enabled when the Reset/Power Down ($\overline{RP}$) signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 300ns maximum, with instructions to the C.I. recognised after only 210ns.

DEVICE OPERATION

Signal Descriptions

A0-A18 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

A9 Address Input is also used for the Electronic Signature Operation. When A9 is raised to 12V the Electronic Signature may be read. The A0 signal is used to read two bytes, when A0 is Low the Manufacturer code is read and when A0 is High the Device code.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address (1)	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Signature
EE	Erase	2	Write	X	20h	Write	Block Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSR or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of Read cycle can occur after one command cycle.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Array

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte to be programmed or a command to the C.I., are latched when both Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output from the memory Array, the Electronic Signature or Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This is a tri-level input which locks the Boot Block from programming and erasure, and allows the memory to be put in deep power down.

When $\overline{RP}$ is High (up to 6.5V maximum) the Boot Block is locked and cannot be programmed or erased. When $\overline{RP}$ is above 11.4V the Boot Block is unlocked for programming or erasure.

With $\overline{RP}$ Low the memory is in deep power down, and if $\overline{RP}$ is within V_{SS}+0.2V the lowest supply current is absorbed.

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits b4 or b5 for Program or Erase Success
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction P/ECS and ESS bits are set to '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte.
			'0'	Program Success	
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction has been executed.
			'0'	V_{PP} OK	
	2	Reserved			
	1	Reserved			
	0	Reserved			

Notes: Logic level '1' is High, '0' is Low.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. It controls writing to the Command Register and Input Address and Data latches. Both Addresses and Data Inputs are latched on the rising edge of $\overline{W}$.

V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{PP} ±10% tolerance option is provided for application requiring maximum 100 write and erase cycles.

V_{CC} Supply Voltage. It is the main circuit supply.

V_{SS} Ground. It is the reference for all voltage measurements.

Memory Blocks

The memory blocks of the M28F411 and M28F421 are shown in Figure 8. The difference between the two products is simply an inversion of the block map to position the Boot Block at the top or bottom of the memory. The selection of the Boot Block at the top or bottom of the memory depends on the microprocessor needs.

Each block of the memory can be erased separately, but only by one block at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another block and then resumed.

Programming and erasure of the memory is disabled when the program supply is at V_{PPL}. For successful programming and erasure the program supply must be at V_{PPH}.

The Boot Block provides additional hardware security by use of the $\overline{RP}$ signal which must be at V_{HH} before any program or erase operation will be executed by the P/E.C. on the Boot Block.

Table 8. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

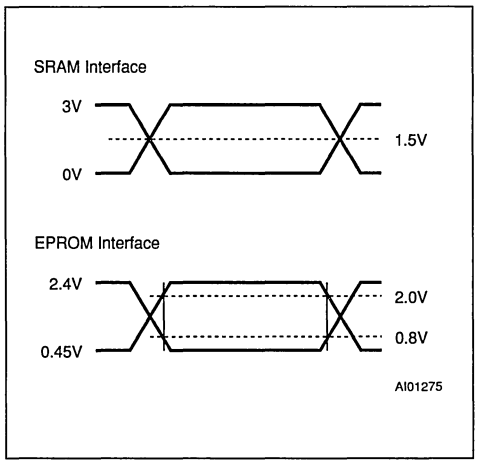


Figure 4. AC Testing Load Circuit

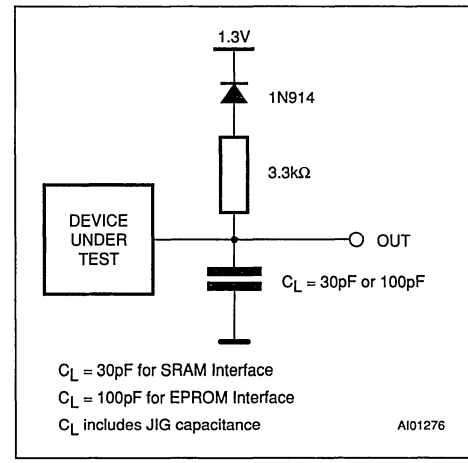


Table 9. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down, and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. The data read depends on the previous command written to the memory (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$.

Table 10. DC Characteristics
(T_A = 0 to 70°C; V_{CC} = 5V±5% or 5V±10%; V_{PP} = 12V±5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		50	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		45	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (3)	Supply Current (Power Down) CMOS	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{CC3}	Supply Current (Program)	Program in progress		50	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Leakage Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Read or Standby)	$V_{PP} \le V_{CC}$		±10	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Program in progress		30	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	$A9 = V_{ID}$		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot Block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 8mA typical in static operation.
2. Current increases to $I_{CC} + I_{CC5}$ during a read operation.
3. CMOS levels $V_{CC} \pm 0.2V$ and $V_{SS} \pm 0.2V$. TTL levels V_{IH} and V_{IL}.

Table 11. DC Characteristics
(T_A = –20 to 85°C or –40 to 85°C ; V_{CC} = 5V±5% or 5V±10%; V_{PP} = 12V±5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		65	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		60	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (3)	Supply Current (Power Down) CMOS	$\overline{RP} = V_{SS} \pm 0.2V$		8	µA
I_{CC3}	Supply Current (Program)	Program in progress		50	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Leakage Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Read or Standby)	$V_{PP} \le V_{CC}$		±15	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Program in progress		30	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot Block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 8mA typical in static operation.
2. Current increases to I_{CC} + I_{CC5} during a read operation.
3. CMOS levels V_{CC} ± 0.2V and V_{SS} ± 0.2V. TTL levels V_{IH} and V_{IL}.

Table 12. DC Characteristics
(T_A = –40 to 125°C; V_{CC} = 5V±5% or 5V±10%; V_{PP} = 12V±5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, f = 10MHz, I_{OUT} = 0mA		65	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, f = 10MHz, I_{OUT} = 0mA		60	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		130	µA
I_{CC2} (3)	Supply Current (Power Down) CMOS	$\overline{RP} = V_{SS} \pm 0.2V$		80	µA
I_{CC3}	Supply Current (Program)	Program in progress		50	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Leakage Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Read or Standby)	$V_{PP} \le V_{CC}$		±15	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Program in progress		30	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –2.5mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	6.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	$A9 = V_{ID}$		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot Block Program or Erase	11.4	13	V

Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 8mA typical in static operation.
2. Current increases to $I_{CC} + I_{CC5}$ during a read operation.
3. CMOS levels $V_{CC} \pm 0.2V$ and $V_{SS} \pm 0.2V$. TTL levels V_{IH} and V_{IL}.

Table 13. Read AC Characteristics (1)
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421								Unit
			-70		-80		-100		-120		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	70		80		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid		70		80		100		120	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid		300		300		300		300	ns
t_{ELQX} (2)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		0		ns
t_{ELQV} (3)	t_{CE}	Chip Enable Low to Output Valid		70		80		100		120	ns
t_{GLQX} (2)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		0		ns
t_{GLQV} (3)	t_{OE}	Output Enable Low to Output Valid		35		40		45		50	ns
t_{EHQX} (2)	t_{OH}	Chip Enable High to Output Transition	0		0		0		0		ns
t_{EHQZ} (2)	t_{HZ}	Chip Enable High to Output Hi-Z		25		30		35		35	ns
t_{GHQX} (2)	t_{OH}	Output Enable High to Output Transition	0		0		0		0		ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z		25		30		35		35	ns
t_{AXQX} (2)	t_{OH}	Address Transition to Output Transition	0		0		0		0		ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Sampled only, not 100% tested.
3. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Table 14. Read AC Characteristics (1)
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421								Unit
			-80		-90		-100		-120		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	80		90		100		120		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid		80		90		100		120	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid		300		300		300		300	ns
t_{ELQX} (2)	t_{LZ}	Chip Enable Low to Output Transition	0		0		0		0		ns
t_{ELQV} (3)	t_{CE}	Chip Enable Low to Output Valid		80		90		100		120	ns
t_{GLQX} (2)	t_{OLZ}	Output Enable Low to Output Transition	0		0		0		0		ns
t_{GLQV} (3)	t_{OE}	Output Enable Low to Output Valid		40		45		50		55	ns
t_{EHQX} (2)	t_{OH}	Chip Enable High to Output Transition	0		0		0		0		ns
t_{EHQZ} (2)	t_{HZ}	Chip Enable High to Output Hi-Z		30		35		40		45	ns
t_{GHQX} (2)	t_{OH}	Output Enable High to Output Transition	0		0		0		0		ns
t_{GHQZ} (2)	t_{DF}	Output Enable High to Output Hi-Z		30		35		40		45	ns
t_{AXQX} (2)	t_{OH}	Address Transition to Output Transition	0		0		0		0		ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Sampled only, not 100% tested.
3. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 5. Read Mode AC Waveforms

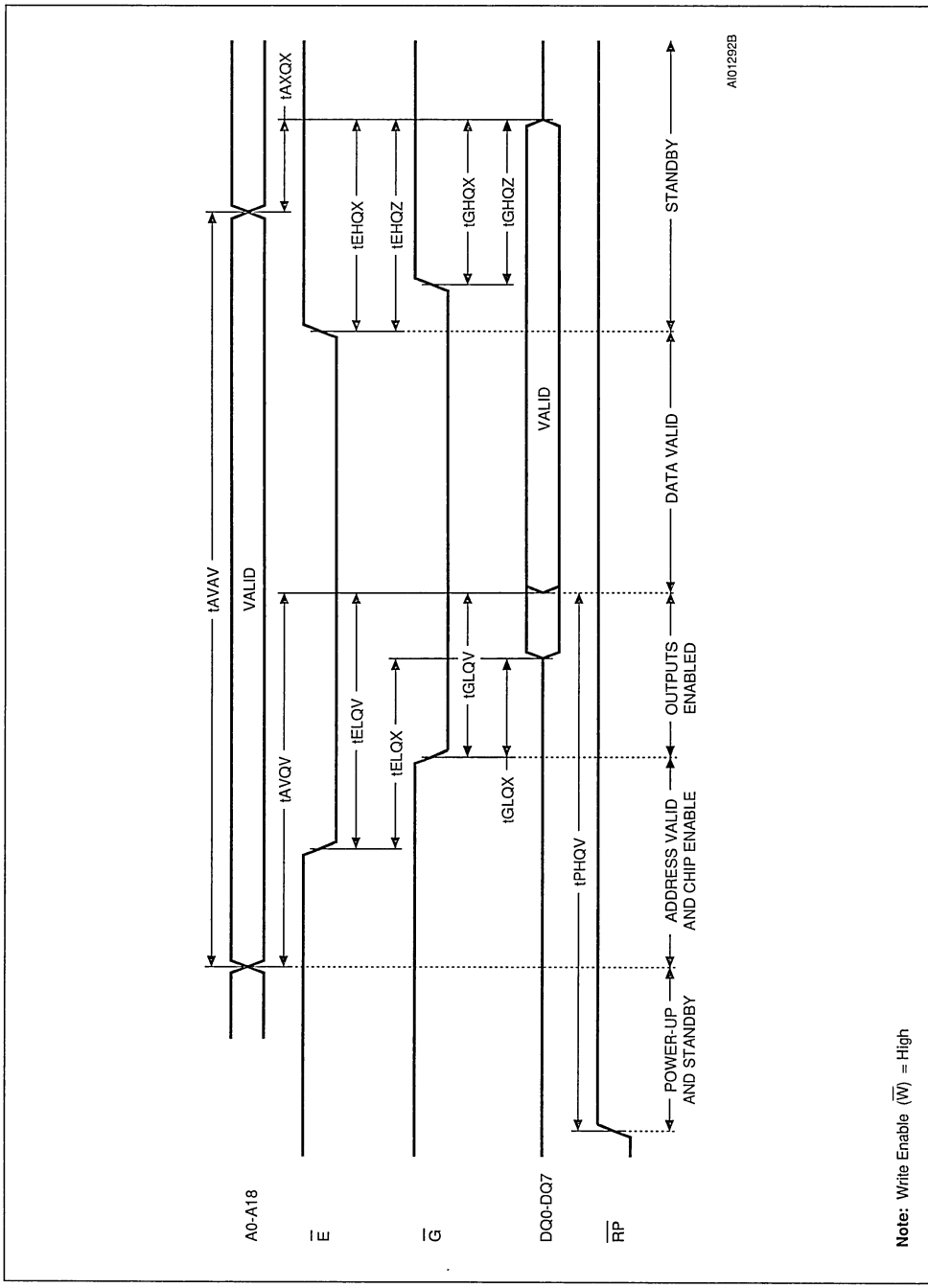


Table 15A. Write AC Characteristics, Write Enable Controlled (1)
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	70		80		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		30		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	50		50		ns
t_{PHHWH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid	6		6		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.3		0.3		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.6		0.6		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements
2 Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block
5. Sampled only, not 100% tested.

Table 15B. Write AC Characteristics, Write Enable Controlled (1)
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	60		70		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	40		50		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	60		60		ns
t_{PHHWH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid	7		7		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 16A. Write AC Characteristics, Write Enable Controlled (1)
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-80		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	80		90		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		60		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	50		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		40		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	50		60		ns
t_{PHHWH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} (5)	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} (2, 3)		Write Enable High to Output Valid	6		7		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Boot Block Erase)	0.3		0.4		sec
t_{WHQV3} (2)		Write Enable High to Output Valid (Parameter Block Erase)	0.3		0.4		sec
t_{WHQV4} (2)		Write Enable High to Output Valid (Main Block Erase)	0.6		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

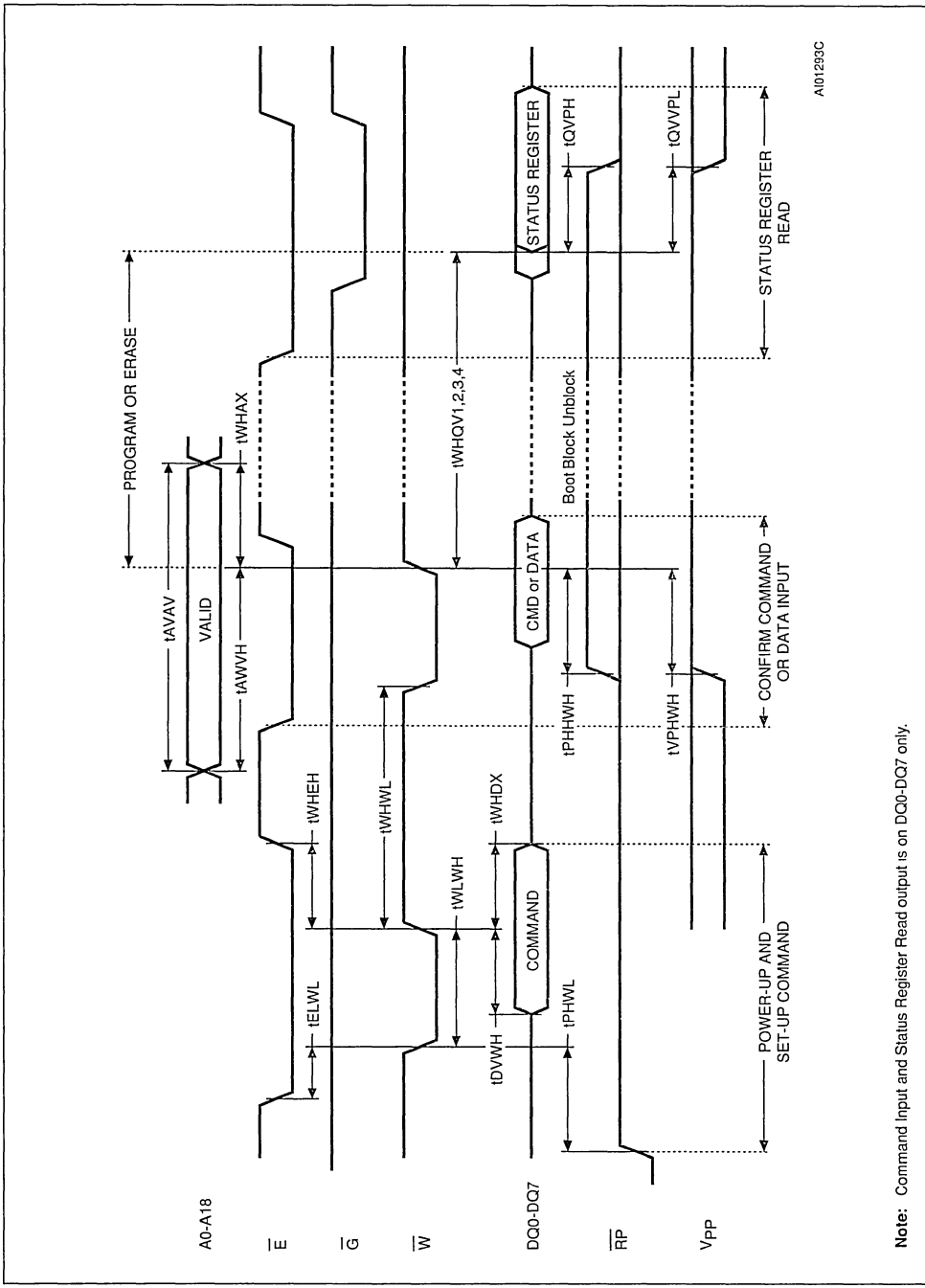
Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 16B. Write AC Characteristics, Write Enable Controlled [1]
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	210		210		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	60		70		ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	60		60		ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	40		50		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	60		60		ns
t_{PHHWH} [5]	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	100		100		ns
t_{VPHWH} [5]	t_{VPS}	V_{PP} High to Write Enable High	100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		ns
t_{WHQV1} [2, 3]		Write Enable High to Output Valid	7		7		µs
t_{WHQV2} [2, 3]		Write Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{WHQV3} [2]		Write Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{WHQV4} [2]		Write Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} [5]	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} [5]		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} [4, 5]		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1 See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3 For Program or Erase of the Boot Block RP must be at V_{HH}.
4 Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested

Figure 6. Program & Erase AC Waveforms, $\overline{W}$ Controlled



Note: Command Input and Status Register Read output is on DQ0-DQ7 only.

Table 17A. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-70		-80		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	70		80		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	20		30		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	50		50		ns
t_{PHHEH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid	6		6		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.3		0.3		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.6		0.6		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 17B. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	60		70		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	60		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	40		50		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	60		60		ns
t_{PHHEH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid	7		7		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 18A. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = –40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-80		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	80		90		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	50		60		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	50		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	30		40		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	50		60		ns
t_{PHHEH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid	6		7		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.3		0.4		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.3		0.4		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.6		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1 See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Table 18B. Write AC Characteristics, Chip Enable Controlled (1)
(T_A = -40 to 125°C; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F411 / 421				Unit
			-100		-120		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	210		210		ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	60		70		ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	60		60		ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	40		50		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	60		60		ns
t_{PHHEH} (5)	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	100		100		ns
t_{VPHEH} (5)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		ns
t_{EHQV1} (2, 3)		Chip Enable High to Output Valid	7		7		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Boot Block Erase)	0.4		0.4		sec
t_{EHQV3} (2)		Chip Enable High to Output Valid (Parameter Block Erase)	0.4		0.4		sec
t_{EHQV4} (2)		Chip Enable High to Output Valid (Main Block Erase)	0.7		0.7		sec
t_{QVPH} (5)	t_{PHH}	Output Valid to Reset/Power Down High	0		0		ns
t_{QVVPL} (5)		Output Valid to V_{PP} Low	0		0		ns
t_{PHBR} (4, 5)		Reset/Power Down High to Boot Block Relock		100		100	ns

Notes: 1. See Figure 3 and Table 8 for timing measurements.
2. Time is measured to Status Register Read giving bit b7 = '1'.
3. For Program or Erase of the Boot Block RP must be at V_{HH}.
4. Time required for Relocking the Boot Block.
5. Sampled only, not 100% tested.

Figure 7. Program & Erase AC Waveforms, $\overline{E}$ Controlled

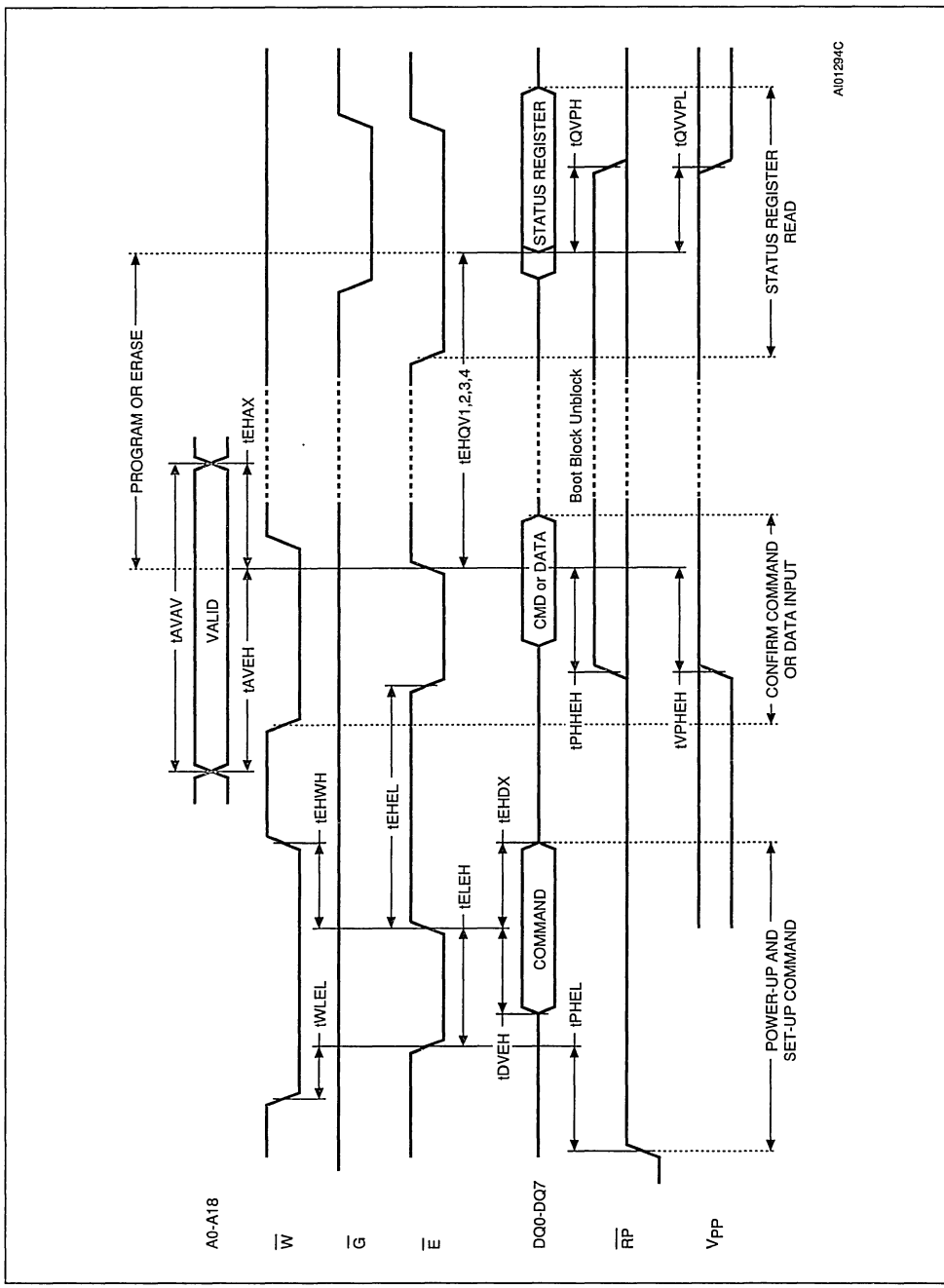


Table 19. Byte Program, Erase Times
(T_A = 0 to 70°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	Test Conditions	M28F411 / 421			Unit
		Min	Typ	Max	
Main Block Program	V_{PP} = 12V ±5%		1.2	4.2	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±5%		1	7	sec
Main Block Erase	V_{PP} = 12V ±5%		2.4	14	sec

Table 20. Byte Program, Erase Times
(T_A = –20 to 85°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	Test Conditions	M28F411 / 421			Unit
		Min	Typ	Max	
Main Block Program	V_{PP} = 12V ±5%		1.4	5	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±5%		1.5	10.5	sec
Main Block Erase	V_{PP} = 12V ±5%		3	18	sec

DEVICE OPERATION (cont'd)

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is low. The power consumption is reduced to the Power Down level, and Outputs are in high impedance, independant of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memories, the manufacturer code for SGS-THOMSON is 20h, and the device codes are 0F6h for the M28F411 (Top Boot Block) and 0FEh for the M28F421 (Bottom Boot Block). These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product.

The Electronic Signature is output by a Read Array operation when the voltage applied to A9 is at V_{ID}, the manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored.

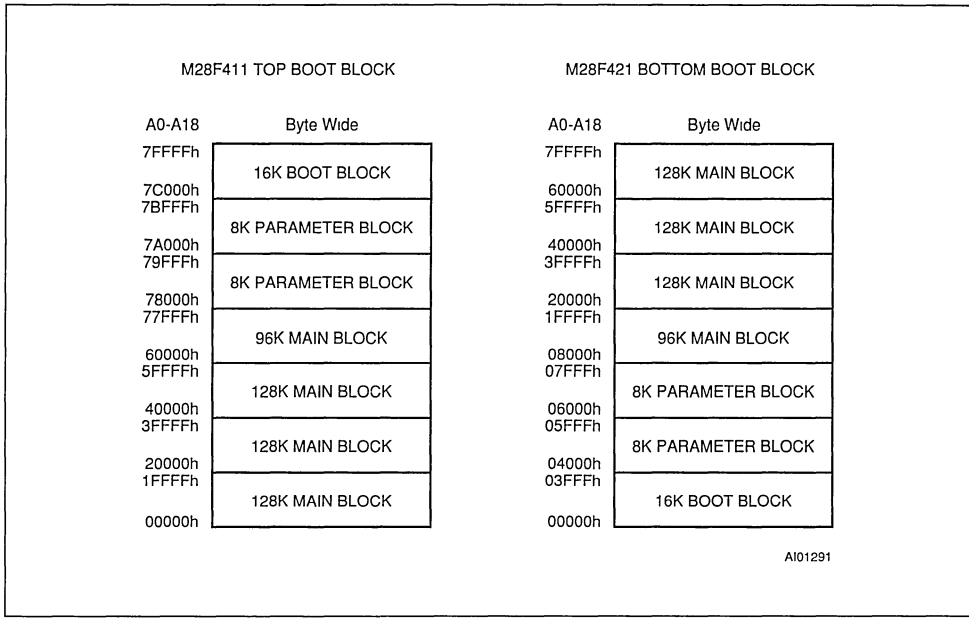
Instructions and Commands

The memories include a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from 1 to 3 operations, the first of which is always a write operation and is followed by either a further write operation to confirm the first command or a read operation(s) to output data.

A Status Register indicates the P/E.C. status Ready or Busy, the suspend/in-progress status of erase operations, the failure/success of erase and program operations and the low/correct value of the Program Supply voltage V_{PP}.

The P/E.C. automatically sets bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The register can be read by the Read Status Register (RSR) instruction and cleared by the Clear Status Register (CLRS) instruction. The meaning of the bits b3 to b7 is shown in Table 7. Bits b0 to b2 are reserved for future use (and should be masked out during status checks).

Figure 8. Memory Map, Byte-wide Addresses



Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read the addressed memory array content.

Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent Read operations output the contents of the Status Register. The contents of the status register are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the Status Register.

Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h followed by two read operations to output the manufacturer and device codes. The manufacturer code, 20h, is output when the address line A0 is Low, and the device code, 0F6h for the M28F411 or 0FEh for the M28F421, when A0 is High.

Erase (EE) instruction. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second command is the Erase Confirm command 0D0h. During the input of the second command an address of the block to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 and b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the RSR (Read Status Register) and ES (Erase Suspend) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it has completed. After completion the Status Register bit b5 returns '1' if there has been an Erase Failure because erasure has not been verified even after the maximum number of erase cycles have been executed. Status Register bit b3 returns '1' if V_{PP} does not remain at V_{PPH} level when the erasure is attempted and/or proceeding.

V_{PP} must be at V_{PPH} when erasing, erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register (CLRS). The Boot Block can only be erased when $\overline{RP}$ is also at V_{HH}.

Program (PG) instruction. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or 10h). A second write operation latches the Address and the Data to be written and starts the P/E.C. Read operations output the status register after the programming has started.

Memory programming is only made by writing '0' in place of '1' in a byte.

During the execution of the programming by the P/E.C., the memory accepts only the RSR (Read Status Register) instruction. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status Register bit b3 returns a '1' if V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming. V_{PP} must be at V_{PPH} when programming, programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect. Then after having cleared the Status Register (CLRS), the memory must be erased and re-programmed.

The Boot Block can only be programmed when $\overline{RP}$ is at V_{HH}.

Clear Status Register (CLRS) instruction. The Clear Status Register uses a single write operation which clears bits b3, b4 and b5, if latched to '1' by the P/E.C., to '0'. Its use is necessary before any new operation when an error has been detected.

Erase Suspend (ES) instruction. The Erase operation may be suspended by this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates whether the erase has actually been suspended, b6 = '1', or whether the P/E.C. cycle was the last and the erase is completed, b6 = '0'. During the suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Read operations initially output the status register while erase is suspended but, following a Read instruction, data from other blocks of the memory can be read. V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or the $\overline{RP}$ signal goes Low while erase is suspended then erase is aborted while bits b5 and b3 of the status register are set. Erase operation must be repeated after having cleared the status register, to be certain to erase the block.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 0D0h. The status register bit b6 is cleared when erasure resumes. Read operations output the status register after the erase is resumed. The suggested flow charts for programs that use the programming, erasure and erase suspend/resume features of the memories are shown in Figure 9 to Figure 11.

Programming. The memory can be programmed byte-by-byte. The Program Supply voltage V_{PP} must be applied before program instructions are given, and if the programming is in the Boot Block, $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Program Supply voltage may be applied continuously during programming. The program sequence is started by writing a Program Set-up command (40h) to the Command Interface, this is followed by writing the address and data byte or word to the memory. The Program/Erase Controller automatically starts and performs the programming after the second write operation, providing that the V_{PP} voltage (and $\overline{RP}$ voltage if programming the Boot Block) are correct. During the programming the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that programming is completed.

A full status check can be made after each byte/word or after a sequence of data has been programmed. The status check is made on bit b3 for any possible V_{PP} error and on bit b4 for any possible programming error.

Erase. The memory can be erased by blocks. The Program Supply voltage V_{PP} must be applied before the Erase instruction is given, and if the Erase is of the Boot Block $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Erase sequence is started by writing an Erase Set-up command (20h) to the Command Interface, this is followed by an address in the block to be erased and the Erase Confirm command (0D0h). The Program/Erase Controller automatically starts and performs the block erase, providing the V_{PP} voltage (and the $\overline{RP}$ voltage if the erase is of the Boot Block) is correct. During the erase the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that erase is completed.

A full status check can be made after the block erase by checking bit b3 for any possible V_{PP} error, bits b5 and b6 for any command sequence errors (erase suspended) and bit b5 alone for an erase error.

Reset. Note that after any program or erase instruction has completed with an error indication or after any V_{PP} transitions down to V_{PPL} the Command Interface must be reset by a Clear Status Register Instruction before data can be accessed.

Automatic Power Saving

The M28F411 and M28F421 memories place themselves in a lower power state when not being accessed. Following a Read operation, after a delay equal to the memory access time, the Supply Current is reduced from a typical read current of 25mA (CMOS inputs) to less than 2mA.

Power Down

The memories provide a power down control input $\overline{RP}$. When this signal is taken to below V_{SS} + 0.2V all internal circuits are switched off and the supply current drops to typically 0.2µA and the program current to typically 0.1µA. If $\overline{RP}$ is taken low during a memory read operation then the memory is de-selected and the outputs become high impedance. If $\overline{RP}$ is taken low during a program or erase sequence then it is aborted and the memory content is no longer valid.

Recovery from deep power down requires 300ns to a memory read operation, or 210ns to a command write. On return from power down the status register is cleared to 00h.

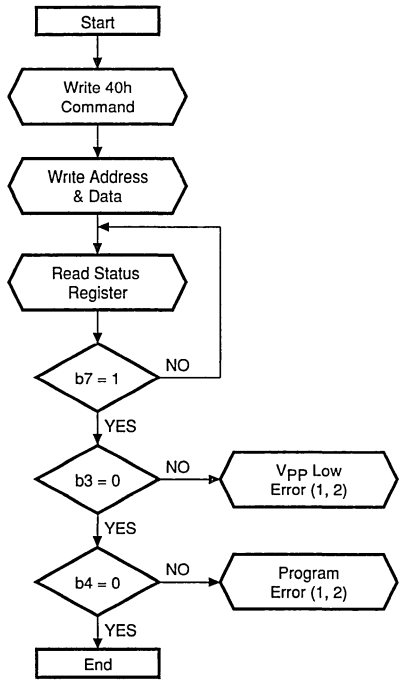
Power Up

The Supply voltage V_{CC} and the Program Supply voltage V_{PP} can be applied in any order. The memory Command Interface is reset on power up to Read Memory Array, but a negative transition of Chip Enable $\overline{E}$ or a change of the addresses is required to ensure valid data outputs. Care must be taken to avoid writes to the memory when V_{CC} is above V_{LKO} and V_{PP} powers up first. Writes can be inhibited by driving either $\overline{E}$ or $\overline{W}$ to V_{IH}. The memory is disabled until $\overline{RP}$ is up to V_{IH}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} and V_{PP} rails decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{PP} program and erase currents required.

Figure 9. Program Flow-chart and Pseudo Code



PG instruction:
– write 40h command
– write Address & Data
(memory enters read status state after the PG instruction)

do:
– read status register
(E or G must be toggled)

while b7 = 1

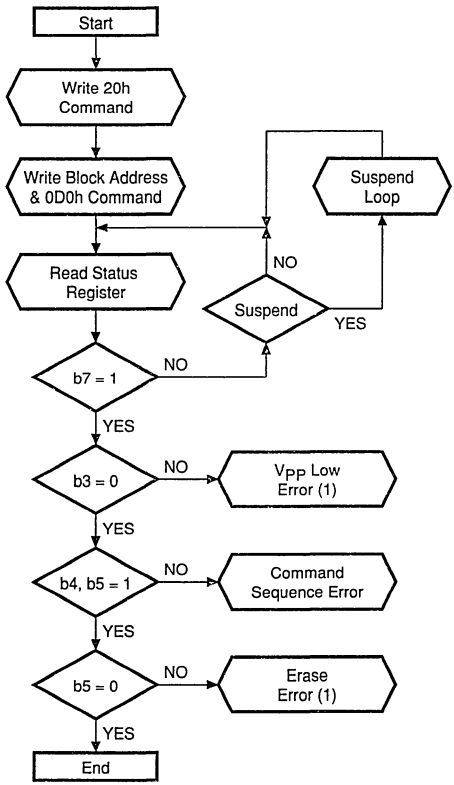
If b3 = 0, V_{PP} low error:
– error handler

If b4 = 0, Program error:
– error handler

AI01278

Notes: 1. Status check of b3 (V_{PP} Low) and b4 (Program Error) can be made after each byte/word programming or after a sequence.
2. If a V_{PP} Low or Program Erase is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 10. Erase Flow-chart and Pseudo Code



EE instruction:
– write 20h command
– write Block Address (A12-A17) & command 0D0h
(memory enters read status state after the EE instruction)

do:
– read status register ($\overline{E}$ or $\overline{G}$ must be toggled)
If EE instruction given execute suspend erase loop

while b7 = 1

If b3 = 0, V_{PP} low error:
– error handler

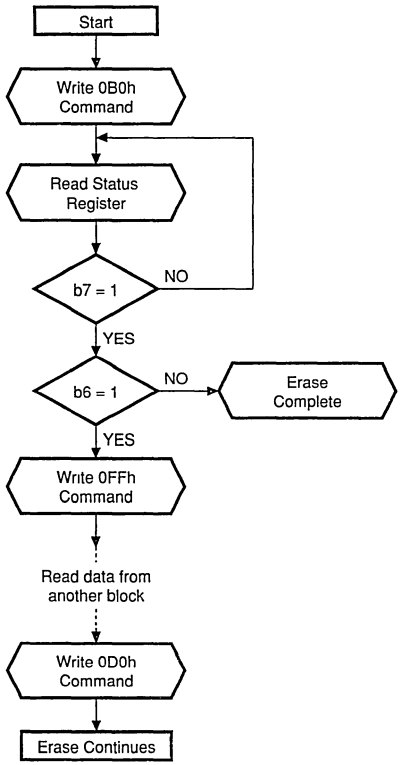
If b4, b5 = 0, Command Sequence error:
– error handler

If b5 = 0, Erase error:
– error handler

AI01279

Note: 1. If V_{PP} Low or Erase Error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 11. Erase Suspend & Resume Flow-chart and Pseudo Code



ES instruction:
– write 0B0h command
(memory enters read register state after the ES instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

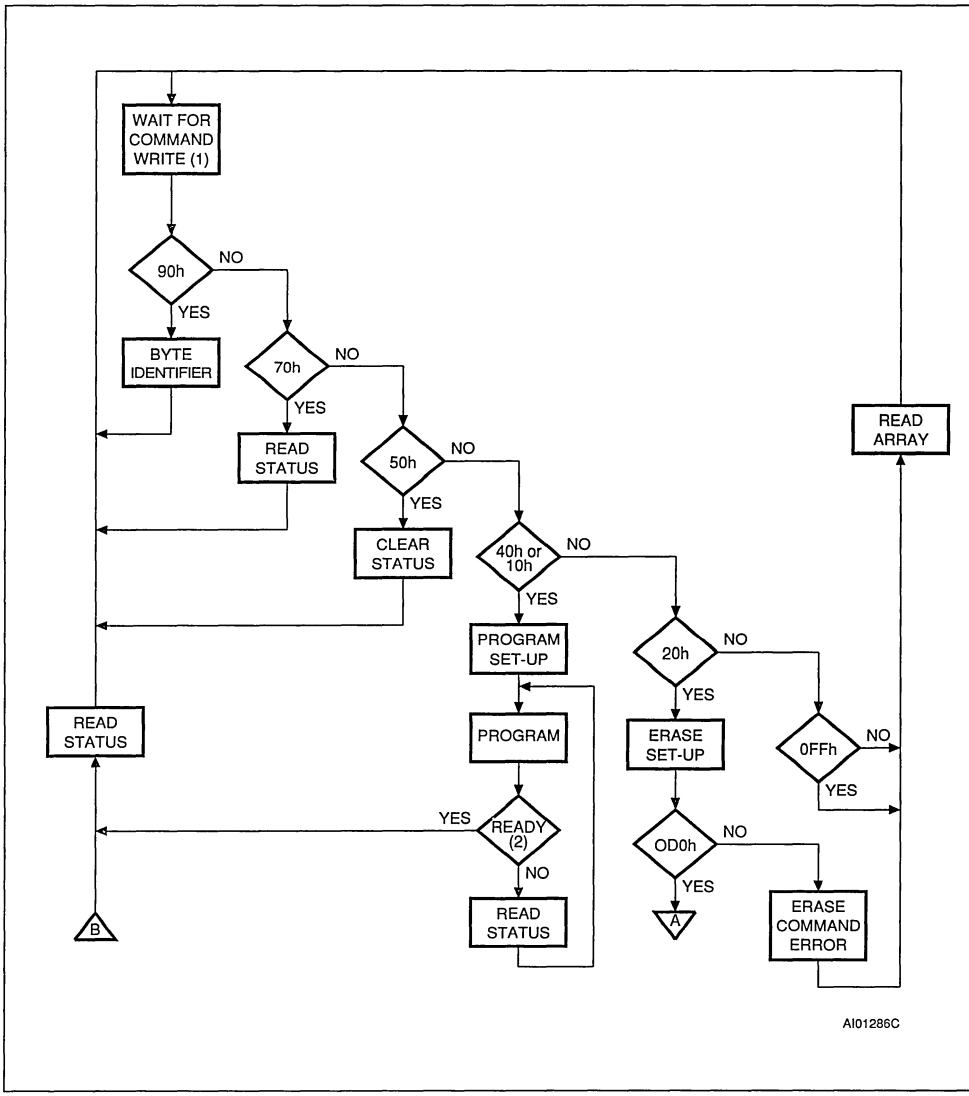
If b6 = 0, Erase completed
(at this point the memory wich accept only the RD or ER instruction)

RD instruction:
– write 0FFh command
– one o more data reads from another block

ER instruction:
– write 0D0h command to resume erasure

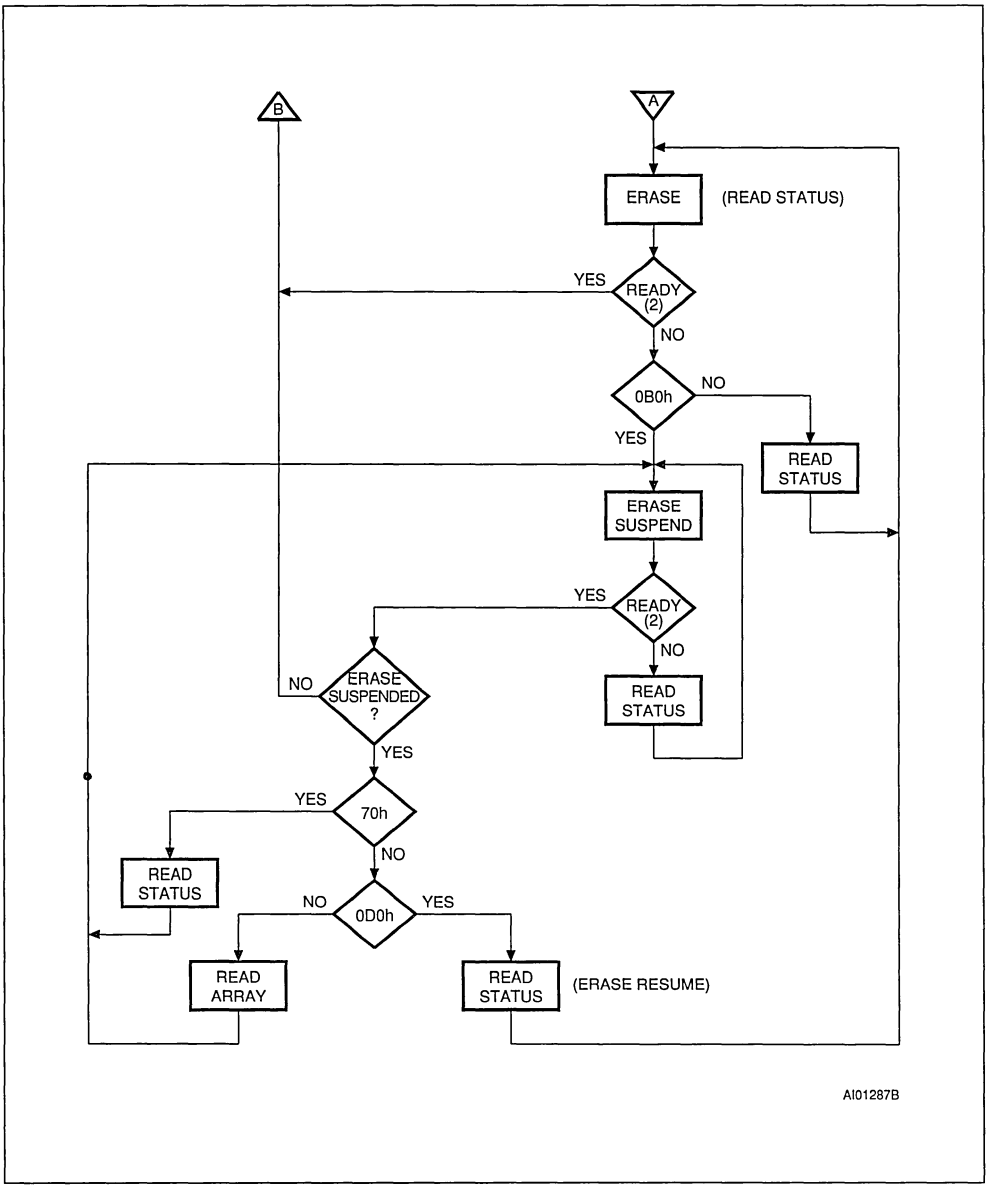
AI01280

Figure 12. Command Interface and Program Erase Controller Flow-diagram (a)



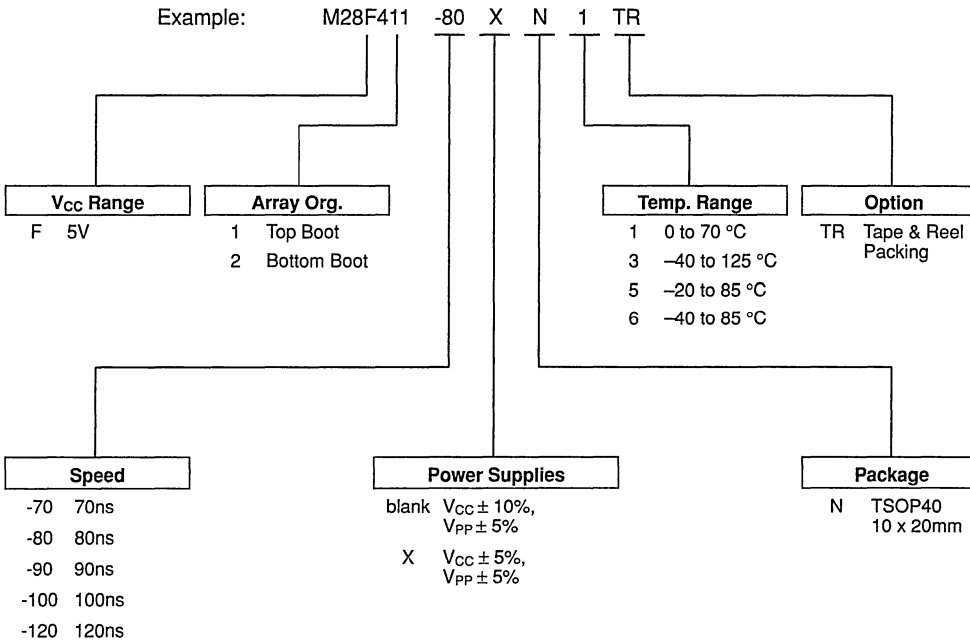
Notes: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E C. status (Ready or Busy) is read on Status Register bit 7.

Figure 13. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME



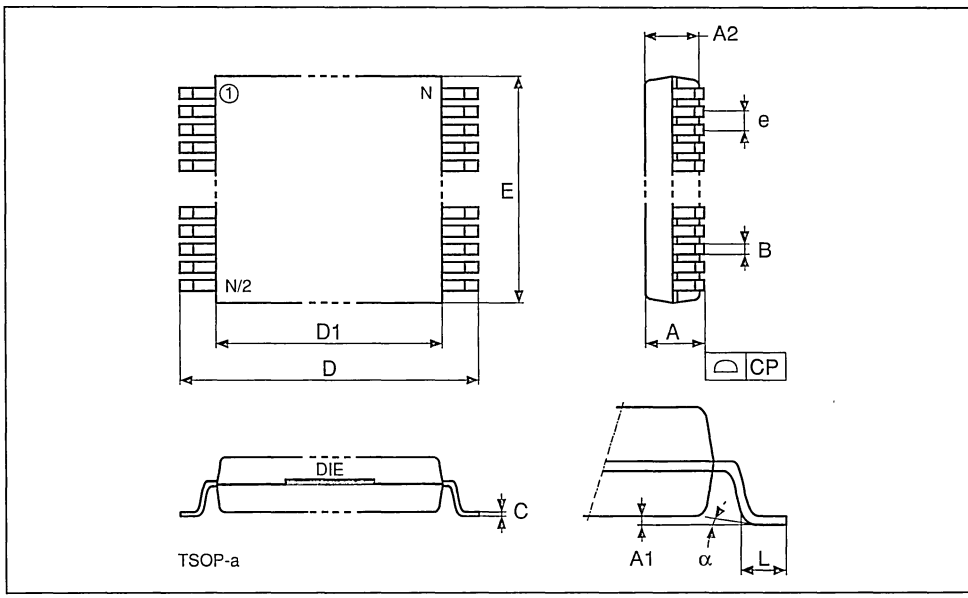
For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		40			40	
CP			0.10			0.004

TSOP40



TSOP-a

Drawing is out of scale

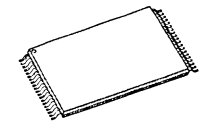
SGS-THOMSON MICROELECTRONICS

M28V411
M28V421

LOW VOLTAGE
4 Megabit (x 8, Block Erase) FLASH MEMORY

PRELIMINARY DATA

- SMALL SIZE PLASTIC PACKAGE TSOP40
- MEMORY ERASE in BLOCKS
  - One 16K Byte Boot Block (top or bottom location) with hardware write and erase protection
  - Two 8K Byte Key Parameter Blocks
  - One 96K Byte Main Block
  - Three 128K Byte Main Blocks
- 3.3V ± 0.3V SUPPLY VOLTAGE
- 12V ± 10% or 5% PROGRAMMING VOLTAGE
- 10,000 PROGRAM/ERASE CYCLES
- PROGRAM/ERASE CONTROLLER
- AUTOMATIC STATIC MODE
- LOW POWER CONSUMPTION
  - 1mA Typical in Static Operation
  - 55µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
  - 15/20mA Typical Operating Consumption
- HIGH SPEED ACCESS TIME: 120ns
- EXTENDED TEMPERATURE RANGES



TSOP40 (N)
10 x 20mm

DESCRIPTION

The M28V411 and M28V421 FLASH MEMORIES are non-volatile memories that may be erased electrically at the block level and programmed by byte.

Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power Down/Boot Block Unlock
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

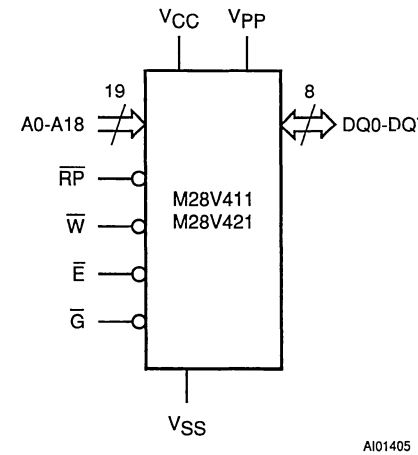
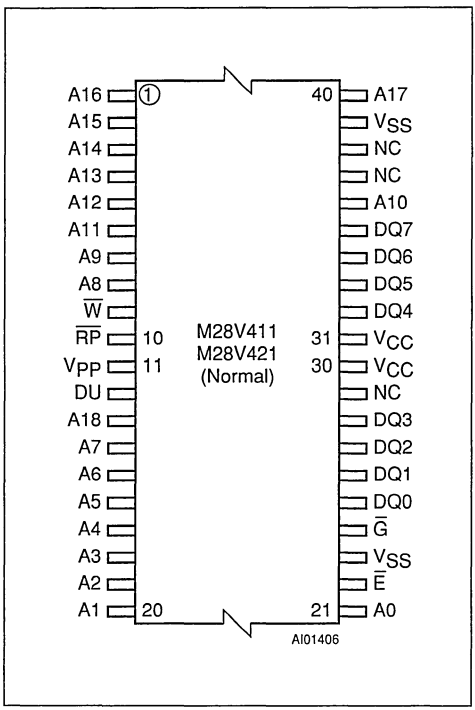


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9} (2)	A9 Voltage		–0.6 to 13.5	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
V_{RP} (2)	$\overline{RP}$ Voltage		–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 7V allowed for less than 20ns.

Figure 2. TSOP Pin Connections



Warning: NC = No Connections, DU = Don't Use

DESCRIPTION (cont'd)

The interface is directly compatible with most microprocessors. TSOP40 (10 x 20mm) package is used.

Organization

The M28V411 and M28V421 are organized as 512K x 8. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down/Boot block unlock, tri-level input, places the memory in deep power down, normal operation or enables programming and erasure of the Boot block.

Blocks

Erasure of the memories is in blocks. There are 7 blocks in the memory address space, one Boot Block of 16K Bytes, two 'Key Parameter Blocks' of 8K Bytes, one 'Main Block' of 96K Bytes, and three 'Main Blocks' of 128K Bytes. The M28V411 memory has the Boot Block at the top of the memory address space (7FFFFh) and the M28V421 locates the Boot Block starting at the bottom (00000h). Erasure of each block takes typically 1 second and each block can be programmed and erased over 10,000 cycles.

The Boot Block is hardware protected from accidental programming or erasure depending on the $\overline{RP}$ signal. Program/Erase commands in the Boot Block are executed only when $\overline{RP}$ is at 12V.

Block erasure may be suspended while data is read from other blocks of the memory, then resumed.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	DQ0 - DQ7
Read Byte	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data Output
Write Byte	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	Hi-Z
Power Down	X	X	X	V_{IL}	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}

Table 4. Electronic Signature

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A9	A1-A8 & A10-A18	DQ0 - DQ7
Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	Don't Care	20h
Device Code	M28V411	V_{IL}	VIL	VIH	VIH	VID	Don't Care	0F7h
	M28V421	V_{IL}	VIL	VIH	VIH	VID	Don't Care	0FFh

Note: $\overline{RP}$ = V_{IH}

Bus Operations

Six operations can be performed by the appropriate bus cycles, Read Byte from the Array, Read Electronic Signature, Output Disable, Standby, Power Down and Write the Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor the memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and block erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte programming takes typically 9µs, block erase typically 1 second. Erasure of a memory block may be suspended in order to read data from another block and then resumed. A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation.

Power Saving

The M28V411 and M28V421 have a number of power saving features. Following a Read access the memory enters a static mode in which the supply current is typically 1mA. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down ($\overline{RP}$) signals are at V_{CC}, when the supply current drops to typically 60µA. A deep power down mode is enabled when the Reset/Power Down ($\overline{RP}$) signal is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 700ns maximum, with instructions to the C.I. recognised after 580ns.

DEVICE OPERATION

Signal Descriptions

A0-A18 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

A9 Address Input is also used for the Electronic Signature Operation. When A9 is raised to 12V the Electronic Signature may be read. The A0 signal is used to read two bytes, when A0 is Low the Manufacturer code is read and when A0 is High the Device code.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address (1)	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Signature
EE	Erase	2	Write	X	20h	Write	Block Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2 The first cycle of the RD, RSR or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of Read cycle can occur after one command cycle.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Array

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte to be programmed or a command to the C.I., are latched when both Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output from the memory Array, the Electronic Signature or Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This is a tri-level input which locks the Boot Block from programming and erasure, and allows the memory to be put in deep power down.

When $\overline{RP}$ is High (up to 6.5V maximum) the Boot Block is locked and cannot be programmed or erased. When $\overline{RP}$ is above 11.4V the Boot Block is unlocked for programming or erasure.

With $\overline{RP}$ Low the memory is in deep power down, and if $\overline{RP}$ is within V_{SS}+0.2V the lowest supply current is absorbed.

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits b4 or b5 for Program or Erase Success
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction P/ECS and ESS bits are set to '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte.
			'0'	Program Success	
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction has been executed.
			'0'	V_{PP} OK	
	2	Reserved			
	1	Reserved			
	0	Reserved			

Notes: Logic level '1' is High, '0' is Low.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. It controls writing to the Command Register and Input Address and Data latches. Both Addresses and Data Inputs are latched on the rising edge of $\overline{W}$.

V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{PP} ±10% tolerance option is provided for application requiring maximum 100 write and erase cycles.

V_{CC} Supply Voltage. It is the main circuit supply.

V_{SS} Ground. It is the reference for all voltage measurements.

Memory Blocks

The memory blocks of the M28V411 and M28V421 are shown in Figure 8. The difference between the two products is simply an inversion of the block map to position the Boot Block at the top or bottom of the memory. The selection of the Boot Block at the top or bottom of the memory depends on the microprocessor needs.

Each block of the memory can be erased separately, but only by one block at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another block and then resumed.

Programming and erasure of the memory is disabled when the program supply is at V_{PPL}. For successful programming and erasure the program supply must be at V_{PPH}.

The Boot Block provides additional hardware security by use of the $\overline{RP}$ signal which must be at V_{HH} before any program or erase operation will be executed by the P/E.C. on the Boot Block.

Table 8. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

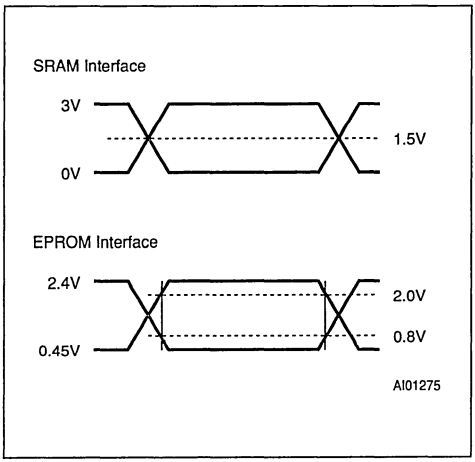


Figure 4. AC Testing Load Circuit

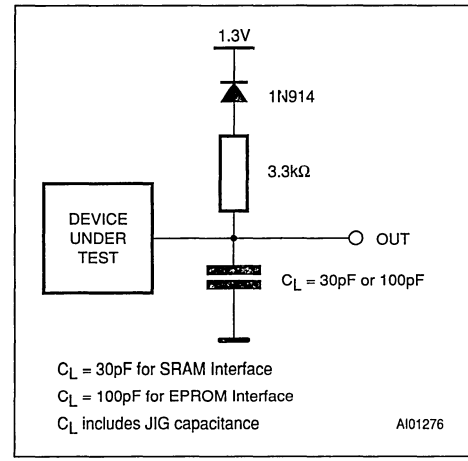


Table 9. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down, and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. The data read depends on the previous command written to the memory (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$.

Table 10. DC Characteristics
(T_A = 0 to 70°C; V_{CC} = 3V±0.3V; V_{PP} = 12V±5% or 12V±10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5MHz		40	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, $\overline{G} = V_{SS}$, f = 5MHz		35	mA
I_{CC1} (3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		3	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		150	µA
I_{CC2} (3)	Supply Current (Power Down) CMOS	$\overline{RP} = V_{SS} \pm 0.2V$		1.2	µA
I_{CC3}	Supply Current (Program)	Program in progress		50	mA
I_{CC4}	Supply Current (Erase)	Erase in progress		30	mA
I_{CC5} (2)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		10	mA
I_{PP}	Program Leakage Current (Read or Standby)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Read or Standby)	$V_{PP} \le V_{CC}$		±15	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Program in progress		30	mA
I_{PP4}	Program Current (Erase)	Erase in progress		30	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –2mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	4.1	V
V_{PPH}	Program Voltage (Program or Erase operations) 5% range		11.4	12.6	V
	Program Voltage (Program or Erase operations) 10% range		10.8	13.2	V
V_{ID}	A9 Voltage (Electronic Signature)		11.4	13	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		500	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		2		V
V_{HH}	Input Voltage ($\overline{RP}$, Boot unlock)	Boot Block Program or Erase	11.4	13	V

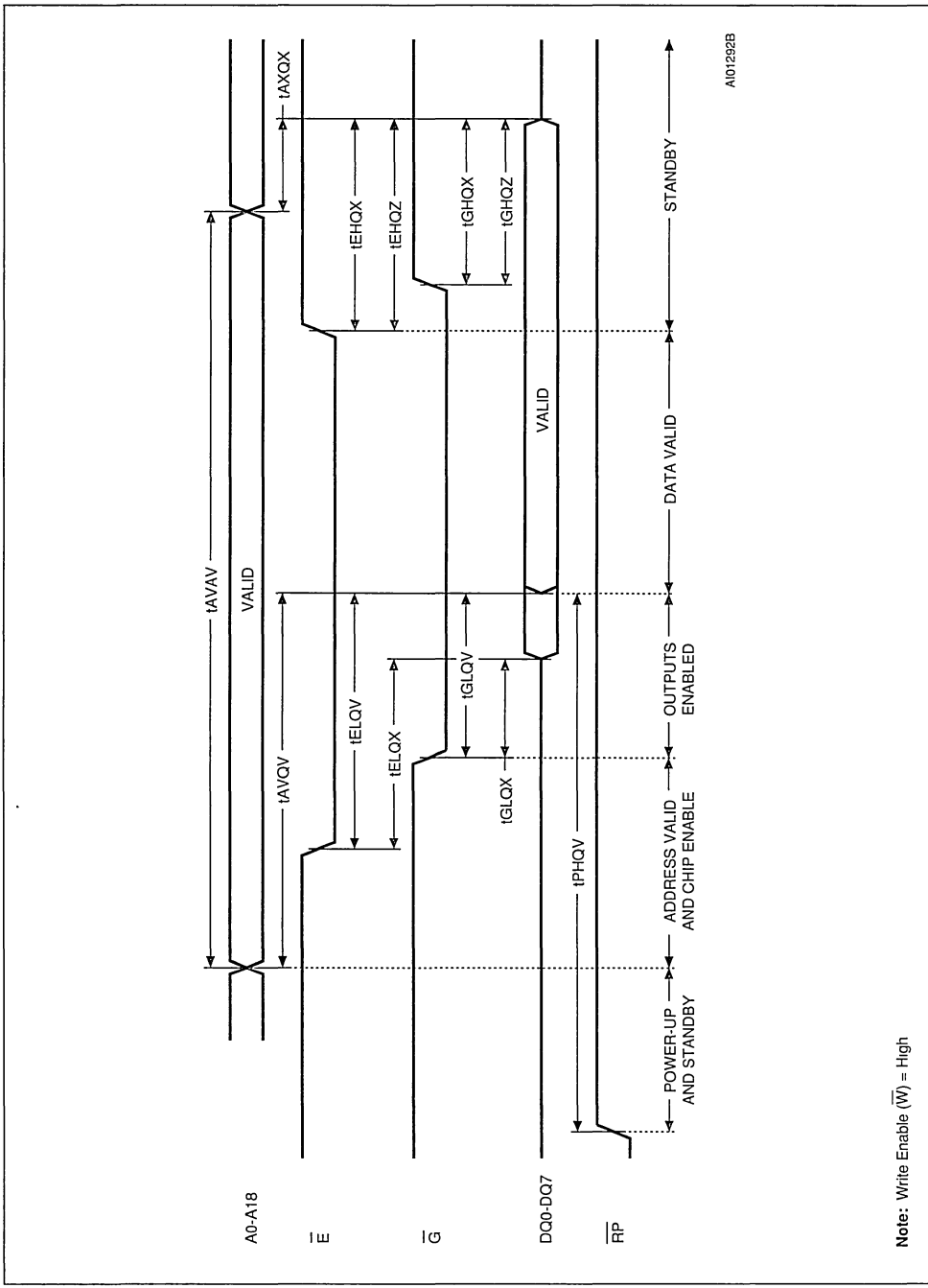
Notes: 1. Automatic Power Saving reduces I_{CC} to ≤ 2mA typical in static operation.
2. Current increases to $I_{CC} + I_{CC5}$ during a read operation.
3. CMOS levels $V_{CC} \pm 0.2V$ and $V_{SS} \pm 0.2V$. TTL levels V_{IH} and V_{IL}.

Table 11. Read AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	Test Condition	M28V411 / 421						Unit
				-120		-150		-180		
				SRAM Interface		EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		150		180		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		180	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		700		700		700	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		180	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		60		65		70	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		50		55		60	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		45		50		55	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 5. Read Mode AC Waveforms



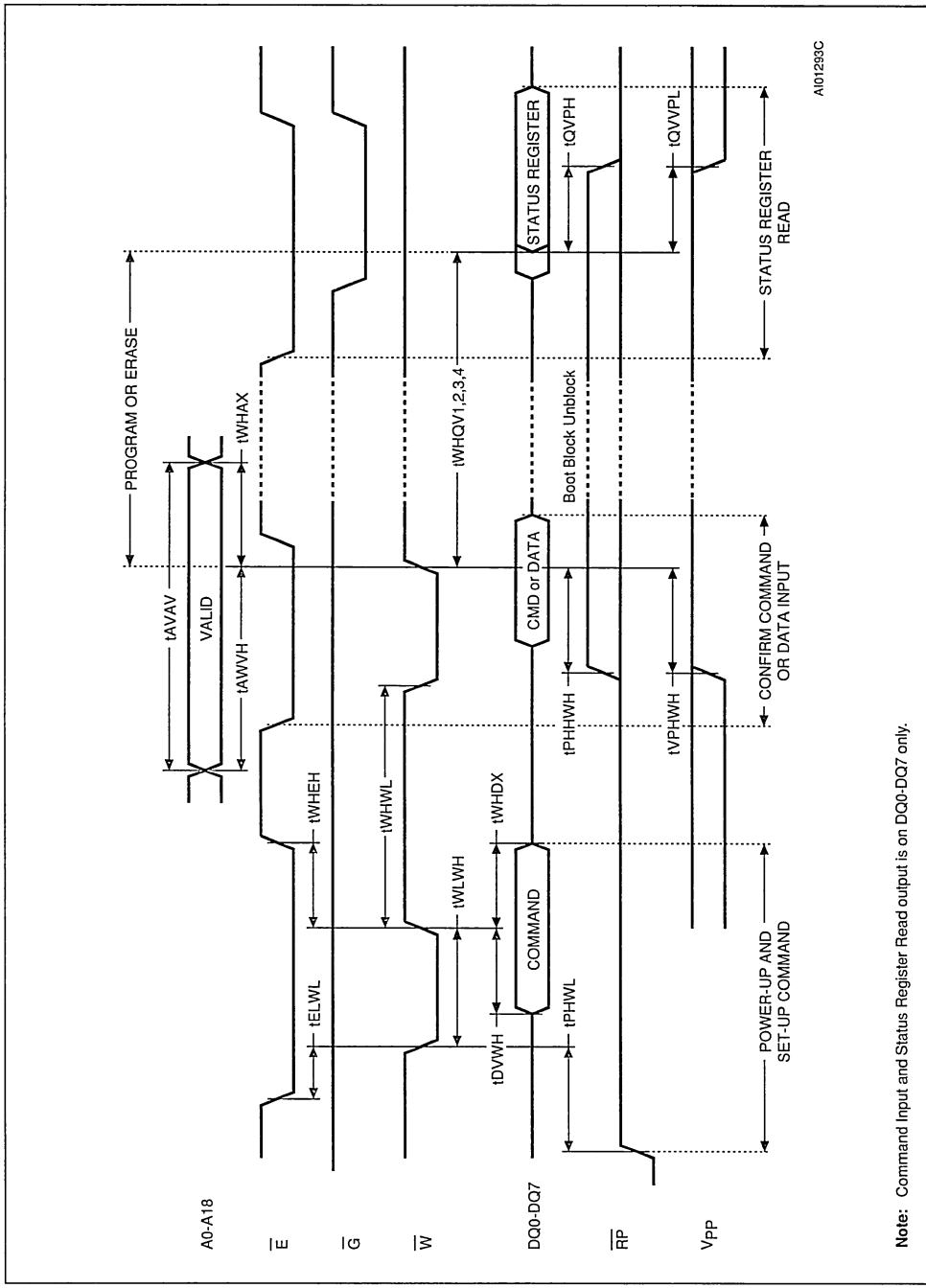
Note: Write Enable ($\overline{W}$) = High

Table 12. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	M28V411 / 421						Unit
			-120		-150		-180		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	120		150		180		ns
t_{PHWL}	t_{PS}	Power Down High to Write Enable Low	1		1		1		µs
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	100		100		100		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	100		100		100		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		10		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	50		50		50		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	95		95		95		ns
t_{PHHWH}	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Write Enable High	200		200		200		ns
t_{VPHWH}	t_{VPS}	V_{PP} High to Write Enable High	200		200		200		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	10		10		10		ns
t_{WHQV1} (1, 2)		Write Enable High to Output Valid	6		6		6		µs
t_{WHQV2} (1, 2)		Write Enable High to Output Valid (Boot Block Erase)	0.3		0.3		0.3		sec
t_{WHQV3} (1)		Write Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		0.3		sec
t_{WHQV4} (1)		Write Enable High to Output Valid (Main Block Erase)	0.6		0.6		0.6		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		200		200		200	ns

Notes: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Figure 6. Program & Erase AC Waveforms, $\overline{W}$ Controlled



Note: Command Input and Status Register Read output is on DQ0-DQ7 only.

Table 13. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5% or 12V ± 10%)

Symbol	Alt	Parameter	M28V411 / 421						Unit
			-120		-150		-180		
			SRAM Interface		EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	120		150		180		ns
t_{PHEL}	t_{PS}	Power Down High to Chip Enable Low	1		1		1		µs
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	100		100		100		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	100		100		100		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		0		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	10		10		10		ns
t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	50		50		50		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	95		95		95		ns
t_{PHHEH}	t_{PHS}	Power Down V_{HH} (Boot Block Unlock) to Chip Enable High	200		200		200		ns
t_{VPHEH}	t_{VPS}	V_{PP} High to Chip Enable High	200		200		200		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	10		10		10		ns
t_{EHQV1} (1, 2)		Chip Enable High to Output Valid	6		6		6		µs
t_{EHQV2} (1, 2)		Chip Enable High to Output Valid (Boot Block Erase)	0.3		0.3		0.3		sec
t_{EHQV3} (1)		Chip Enable High to Output Valid (Parameter Block Erase)	0.3		0.3		0.3		sec
t_{EHQV4} (1)		Chip Enable High to Output Valid (Main Block Erase)	0.6		0.6		0.6		sec
t_{QVPH}	t_{PHH}	Output Valid to Reset/Power Down High	0		0		0		ns
t_{QVVPL}		Output Valid to V_{PP} Low	0		0		0		ns
t_{PHBR} (3)		Reset/Power Down High to Boot Block Relock		200		200		200	ns

Note: 1. Time is measured to Status Register Read giving bit b7 = '1'.
2. For Program or Erase of the Boot Block RP must be at V_{HH}.
3. Time required for Relocking the Boot Block.

Figure 7. Program & Erase AC Waveforms, $\overline{E}$ Controlled

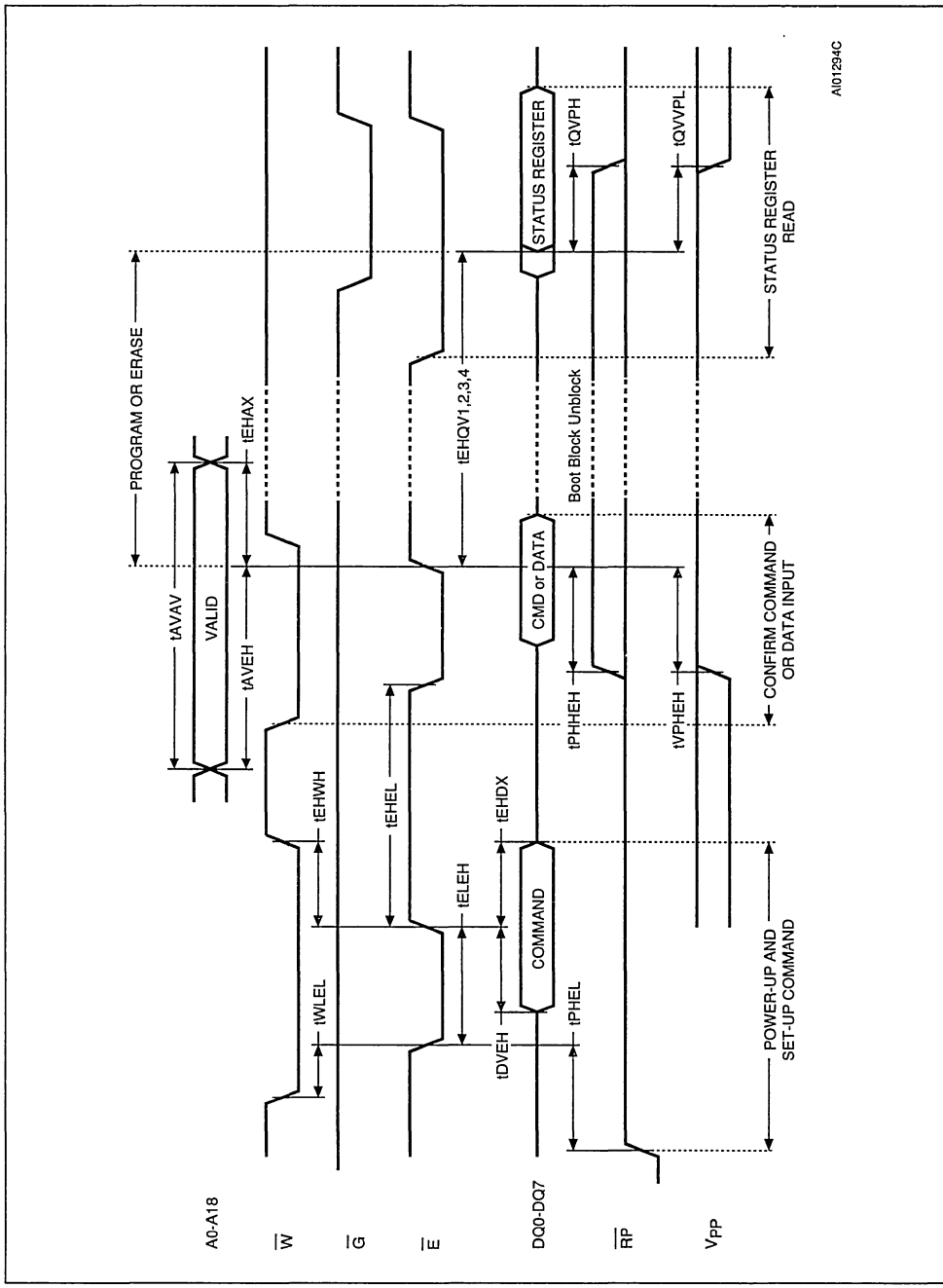


Table 14. Byte Program, Erase Times
(T_A = 0 to 70°C; V_{CC} = 3.3V ± 0.3V)

Parameter	Test Conditions	M28VF411 / 421			Unit
		Min	Typ	Max	
Main Block Program	V_{PP} = 12V ±5%		1.2	4.2	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±5%		1	7	sec
Main Block Erase	V_{PP} = 12V ±5%		2.4	14	sec
Main Block Program	V_{PP} = 12V ±10%		6	20	sec
Boot or Parameter Block Erase	V_{PP} = 12V ±10%		5.8	40	sec
Main Block Erase	V_{PP} = 12V ±10%		14	60	sec

DEVICE OPERATION (cont'd)

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is low. The power consumption is reduced to the Power Down level, and Outputs are in high impedance, independant of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memories, the manufacturer code for SGS-THOMSON is 20h, and the device codes are 0F7h for the M28VF411 (Top Boot Block) and 0FFh for the M28V421 (Bottom Boot Block). These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product.

The Electronic Signature is output by a Read Array operation when the voltage applied to A9 is at V_{ID}, the manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored.

Instructions and Commands

The memories include a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from 1 to 3 operations, the first of which is always a write operation and is followed by either a further write operation to confirm the first command or a read operation(s) to output data.

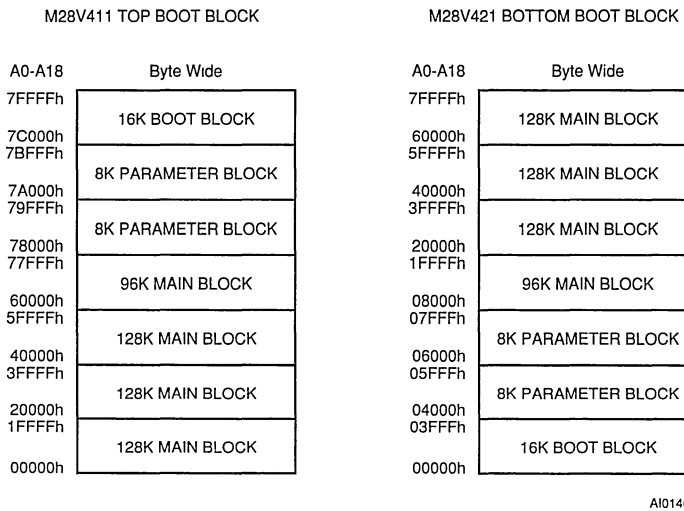
A Status Register indicates the P/E.C. status Ready or Busy, the suspend/in-progress status of erase operations, the failure/success of erase and program operations and the low/correct value of the Program Supply voltage V_{PP}.

The P/E.C. automatically sets bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The register can be read by the Read Status Register (RSR) instruction and cleared by the Clear Status Register (CLRS) instruction. The meaning of the bits b3 to b7 is shown in Table 7. Bits b0 to b2 are reserved for future use (and should be masked out during status checks).

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read the addressed memory array content.

Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent Read operations output the contents of the Status Register. The contents of the status register are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the Status Register.

Figure 8. Memory Map, Byte-wide Addresses



Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h followed by two read operations to output the manufacturer and device codes. The manufacturer code, 20h, is output when the address line A0 is Low, and the device code, 0F7h for the M28V411 or 0FFh for the M28V421, when A0 is High.

Erase (EE) instruction. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second command is the Erase Confirm command 0D0h. During the input of the second command an address of the block to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 and b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the RSR (Read Status Register) and ES (Erase Suspend) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it has completed. After completion the Status Register bit b5 returns '1' if there has been an Erase Failure because erasure has not been verified even after the maximum number of erase cycles have been executed. Status Register bit b3 returns '1' if V_{PP} does not remain at V_{PPH} level when the erasure is attempted and/or proceeding.

V_{PP} must be at V_{PPH} when erasing, erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register (CLRS).

The Boot Block can only be erased when $\overline{RP}$ is also at V_{HH}.

Program (PG) instruction. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or 10h). A second write operation latches the Address and the Data to be written and starts the P/E.C. Read operations output the status register after the programming has started.

Memory programming is only made by writing '0' in place of '1' in a byte.

During the execution of the programming by the P/E.C., the memory accepts only the RSR (Read Status Register) instruction. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status Register bit b3 returns a '1' if V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming. V_{PP} must be at V_{PPH} when programming, programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect. Then after having cleared the Status Register (CLRS), the memory must be erased and re-programmed.

The Boot Block can only be programmed when $\overline{RP}$ is at V_{HH}.

Clear Status Register (CLRS) instruction. The Clear Status Register uses a single write operation which clears bits b3, b4 and b5, if latched to '1' by the P/E.C., to '0'. Its use is necessary before any new operation when an error has been detected.

Erase Suspend (ES) instruction. The Erase operation may be suspended by this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates whether the erase has actually been suspended, b6 = '1', or whether the P/E.C. cycle was the last and the erase is completed, b6 = '0'. During the suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Read operations initially output the status register while erase is suspended but, following a Read instruction, data from other blocks of the memory can be read. V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or the $\overline{RP}$ signal goes Low while erase is suspended then erase is aborted while bits b5 and b3 of the status register are set. Erase operation must be repeated after having cleared the status register, to be certain to erase the block.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 0D0h. The status register bit b6 is cleared when erasure resumes. Read operations output the status register after the erase is resumed. The suggested flow charts for programs that use the programming, erasure and erase suspend/resume features of the memories are shown in Figure 9 to Figure 11.

Programming. The memory can be programmed byte-by-byte. The Program Supply voltage V_{PP} must be applied before program instructions are given, and if the programming is in the Boot Block, $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Program Supply voltage may be applied continuously during programming. The program sequence is started by writing a Program Set-up command (40h) to the Command Interface, this is followed by writing the address and data byte or word to the memory. The Program/Erase Controller automatically starts and performs the programming after the second write operation, providing that the V_{PP} voltage (and $\overline{RP}$ voltage if programming the Boot Block) are correct. During the programming the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that programming is completed.

A full status check can be made after each byte/word or after a sequence of data has been programmed. The status check is made on bit b3 for any possible V_{PP} error and on bit b4 for any possible programming error.

Erase. The memory can be erased by blocks. The Program Supply voltage V_{PP} must be applied before the Erase instruction is given, and if the Erase is of the Boot Block $\overline{RP}$ must also be raised to V_{HH} to unlock the Boot Block. The Erase sequence is started by writing an Erase Set-up command (20h) to the Command Interface, this is followed by an address in the block to be erased and the Erase Confirm command (0D0h). The Program/Erase Controller automatically starts and performs the block erase, providing the V_{PP} voltage (and the $\overline{RP}$ voltage if the erase is of the Boot Block) is correct. During the erase the memory status is checked by reading the status register bit b7 which shows the status of the P/E.C. Bit b7 = '1' indicates that erase is completed.

A full status check can be made after the block erase by checking bit b3 for any possible V_{PP} error, bits b5 and b6 for any command sequence errors (erase suspended) and bit b5 alone for an erase error.

Reset. Note that after any program or erase instruction has completed with an error indication or after any V_{PP} transitions down to V_{PPL} the Command Interface must be reset by a Clear Status Register Instruction before data can be accessed.

Automatic Power Saving

The M28V411 and M28V421 memories place themselves in a lower power state when not being accessed. Following a Read operation, after a delay equal to the memory access time, the Supply Current is reduced from a typical read current of 20mA (CMOS inputs) to less than 2mA.

Power Down

The memories provide a power down control input $\overline{RP}$. When this signal is taken to below V_{SS} + 0.2V all internal circuits are switched off and the supply current drops to typically 0.2µA and the program current to typically 0.1µA. If $\overline{RP}$ is taken low during a memory read operation then the memory is deselected and the outputs become high impedance. If $\overline{RP}$ is taken low during a program or erase sequence then it is aborted and the memory content is no longer valid.

Recovery from deep power down requires 700ns to a memory read operation, or 580ns to a command write. On return from power down the status register is cleared to 00h.

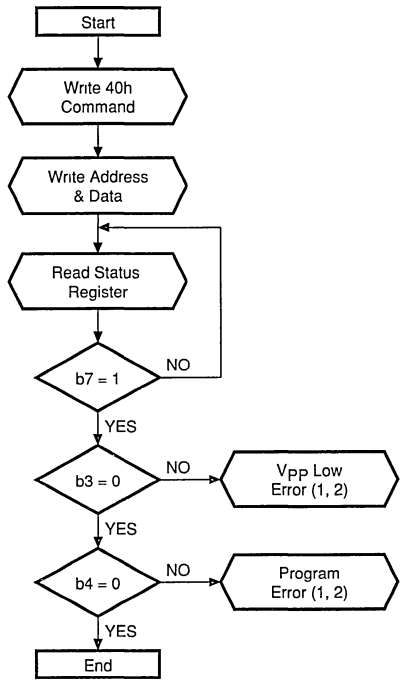
Power Up

The Supply voltage V_{CC} and the Program Supply voltage V_{PP} can be applied in any order. The memory Command Interface is reset on power up to Read Memory Array, but a negative transition of Chip Enable $\overline{E}$ or a change of the addresses is required to ensure valid data outputs. Care must be taken to avoid writes to the memory when V_{CC} is above V_{LKO} and V_{PP} powers up first. Writes can be inhibited by driving either $\overline{E}$ or $\overline{W}$ to V_{IH}. The memory is disabled until $\overline{RP}$ is up to V_{IH}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} and V_{PP} rails decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{PP} program and erase currents required.

Figure 9. Program Flow-chart and Pseudo Code



PG instruction:
– write 40h command
– write Address & Data
(memory enters read status state after the PG instruction)

do:
– read status register
(E or G must be toggled)

while b7 = 1

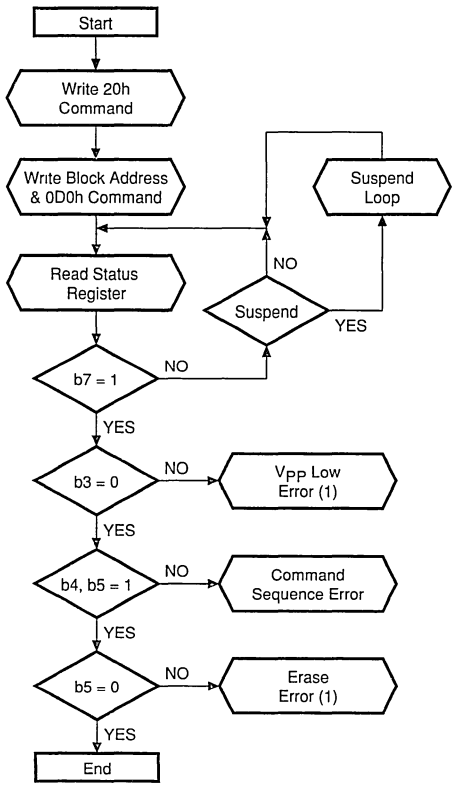
If b3 = 0, V_{PP} low error:
– error handler

If b4 = 0, Program error:
– error handler

AI01278

Notes: 1. Status check of b3 (V_{PP} Low) and b4 (Program Error) can be made after each byte/word programming or after a sequence.
2 If a V_{PP} Low or Program Erase is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 10. Erase Flow-chart and Pseudo Code



EE instruction:
– write 20h command
– write Block Address (A12-A17) & command 0D0h
(memory enters read status state after the EE instruction)

do:
– read status register ($\overline{E}$ or $\overline{G}$ must be toggled)
If EE instruction given execute suspend erase loop

while b7 = 1

If b3 = 0, V_{PP} low error:
– error handler

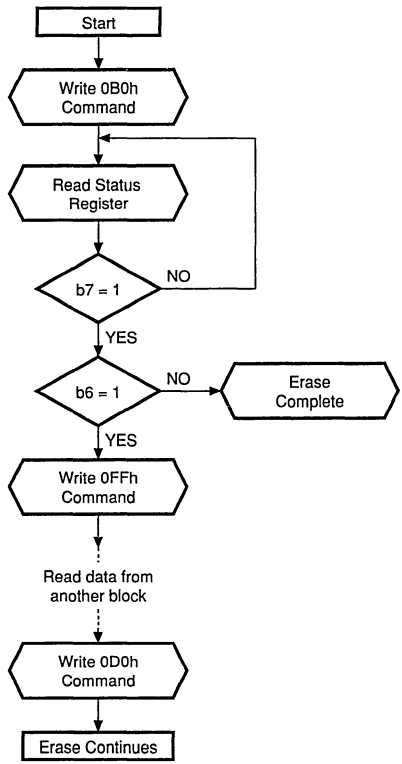
If b4, b5 = 0, Command Sequence error:
– error handler

If b5 = 0, Erase error:
– error handler

AI01279

Note: 1. If V_{PP} Low or Erase Error is found, the Status Register must be cleared (CLRS instruction) before further P/E C. operations

Figure 11. Erase Suspend & Resume Flow-chart and Pseudo Code



ES instruction:
– write 0B0h command
(memory enters read register state after the ES instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

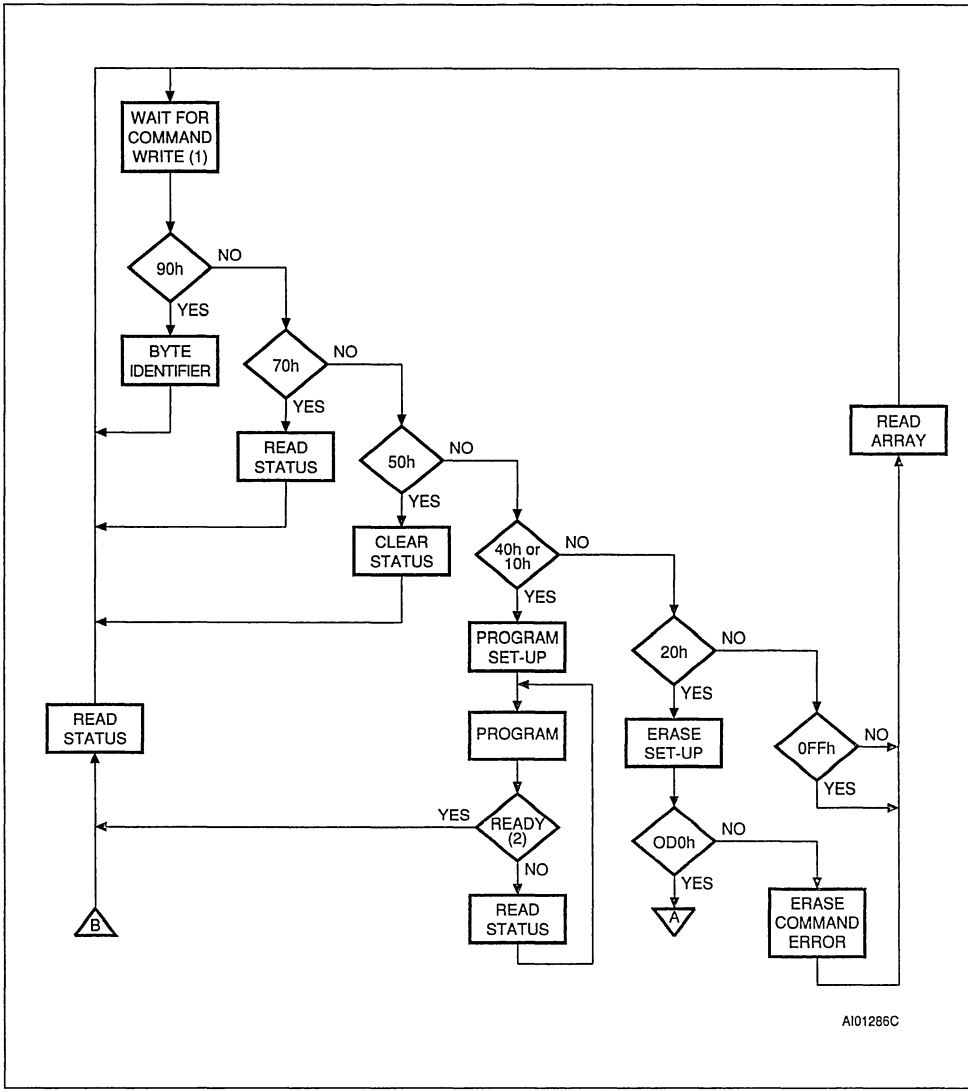
If b6 = 0, Erase completed
(at this point the memory wich accept only the RD or ER instruction)

RD instruction:
– write 0FFh command
– one o more data reads from another block

ER instruction:
– write 0D0h command to resume erasure

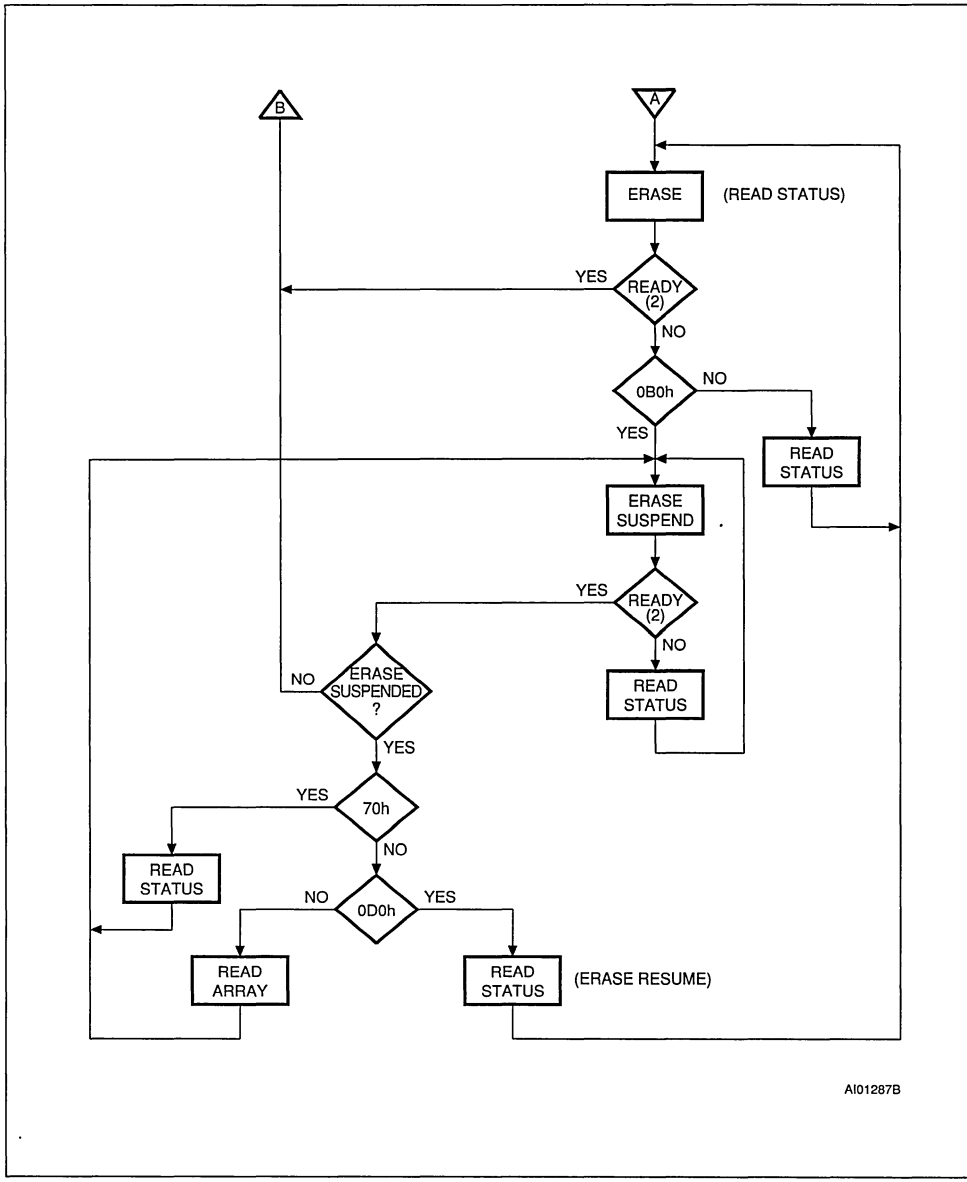
AI01280

Figure 12. Command Interface and Program Erase Controller Flow-diagram (a)



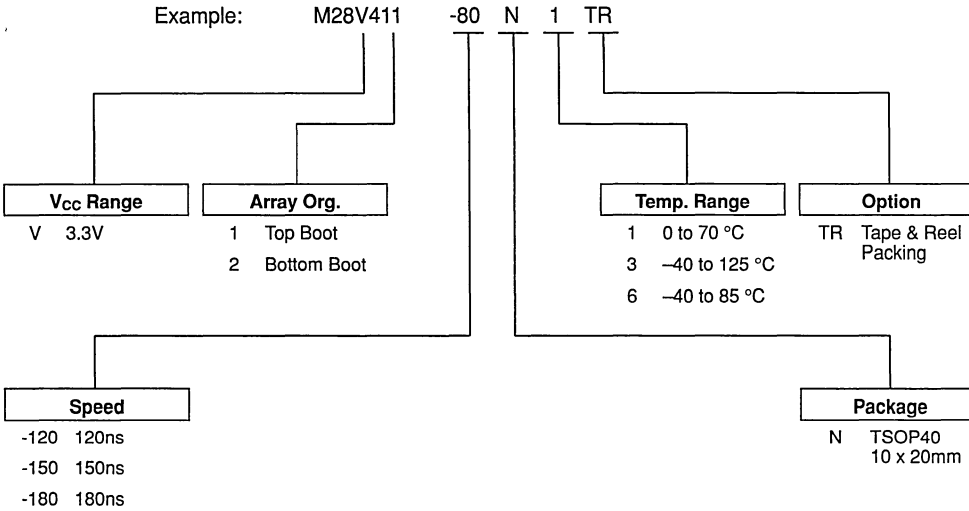
Notes: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 13. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME



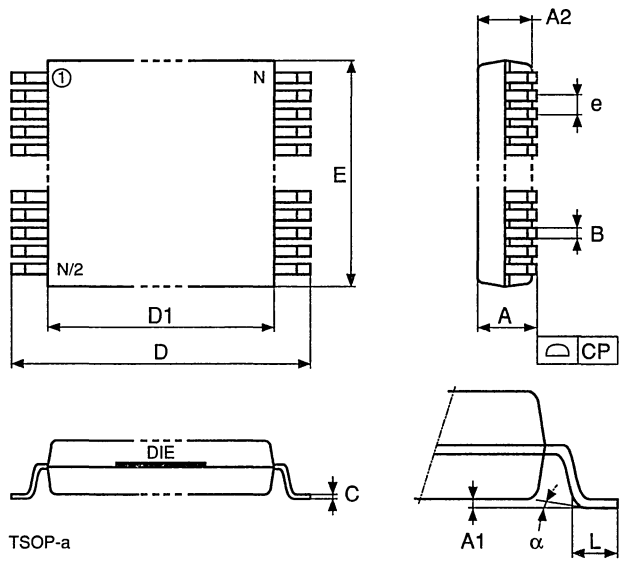
For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		40			40	
CP			0.10			0.004

TSOP40



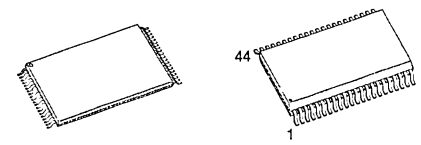
TSOP-a

Drawing is out of scale

8 Megabit (1 Meg x 8, Sector Erase) FLASH MEMORY

PRELIMINARY DATA

- SMALL SIZE PLASTIC PACKAGES TSOP40 and SO44
- MEMORY ERASE in SECTORS
  - 16 Sectors of 64K Bytes each
- 5V ± 0.5V SUPPLY VOLTAGE
- 12V ± 5% PROGRAMMING VOLTAGE
- 100,000 PROGRAM/ERASE CYCLES per SECTOR
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Erase by Sector, Erase Suspend/Resume Ready/Busy Output
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
- HIGH SPEED ACCESS TIME: 100ns
- EXTENDED TEMPERATURE RANGE
- COMPATIBLE to 16 MEGABIT FLASH MEMORY
  - Equal Software Command Set
  - Pinout Compatible



TSOP40 (N)
10 x 20mm

SO44 (M)

Figure 1. Logic Diagram

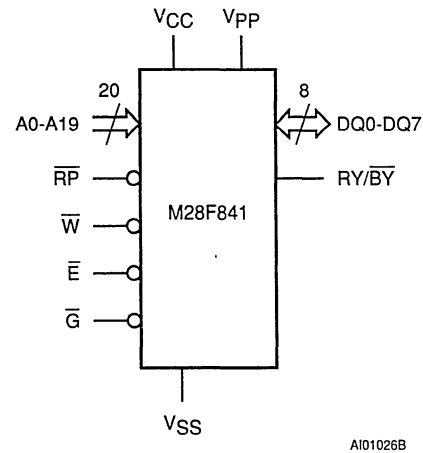
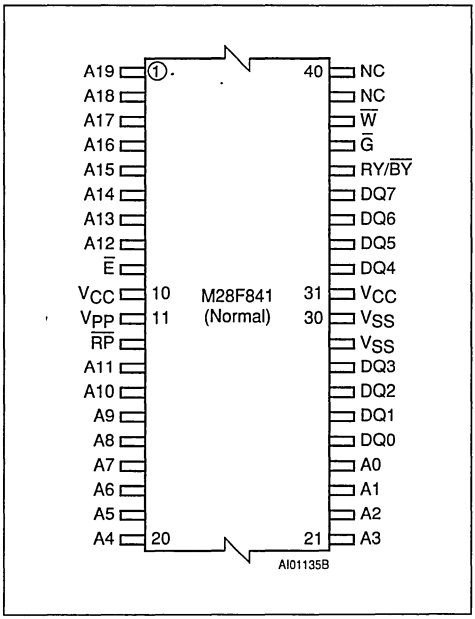


Table 1. Signal Names

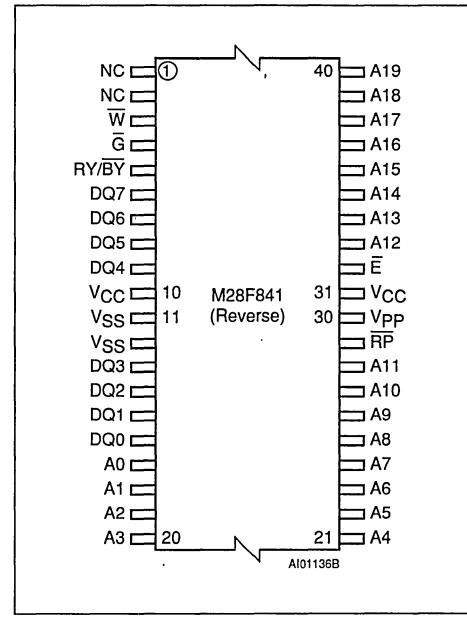
A0-A19	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power Down
RY/$\overline{BY}$	Ready/Busy Output
V_{PP}	Program & Erase Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. TSOP Pin Connections



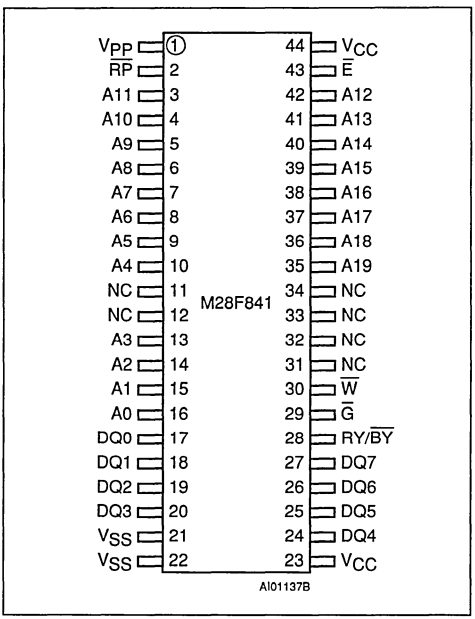
Warning: NC = No Connections

Figure 2B. TSOP Reverse Pin Connections



Warning: NC = No Connections

Figure 2C. SO Pin Connections



Warning: NC = No Connections

DESCRIPTION

The M28F841 FLASH MEMORY product is a non-volatile memory that may be erased electrically at the sector level and programmed byte-by-byte. The interface is directly compatible with most microprocessors. It is intended for computer file systems and mass data storage applications. TSOP40 and S044 packages are used. The M28F841 is software and pin-out, footprint compatible with the M28V161, 16 Megabit FLASH Memory, with the simple substraction of an address line.

Organization

The organization is 1 Meg x 8 with Address lines A0-A19 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down input places the memory in deep power down. A Ready/Busy output indicates the status of the internal Program/Erase Controller (P/E.C.).

Sectors

Erasure of the memory is in sectors. There are 16 sectors in the memory address space, each of 64K bytes. Programming of each sector takes typically 0.6 seconds and erasure 1.6 seconds, each sector may be programmed and erased over 100,000 cycles. All sectors are protected from programming

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
I_{OUT} (4)	Output Short Circuit Current		100	mA

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 7V allowed for less than 20ns.
4. Only one output shorted at a time for no longer than 1 second.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	RY/$\overline{BY}$ (2)	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OH}	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{OL} / V_{OH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{OH}	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	V_{OH}	Hi-Z
Power Down	X	X	X	V_{IL}	V_{OH}	Hi-Z

Notes: 1. X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}
2. RY/$\overline{BY}$ = V_{OL} when the P/E.C. is executing a Sector Erase or Write operation. It is at V_{OH} when the P/E.C. is not busy, in the Erase Suspend or Power Down modes.

Table 4. Electronic Signature

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	A0	RY/$\overline{BY}$	DQ0 - DQ7
Manufact. Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{OH}	20h
Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{OH}	0FCh

DESCRIPTION (cont'd)

or erasure when the Reset/Power Down $\overline{RP}$ signal is Low. Sector erase may be suspended while data is read from other sectors of the memory, then resumed.

Bus operations

Five operations can be performed by the appropriate bus cycles, Read a Byte from the Array, Output Disable, Standby, Power Down and Write a Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor then memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address (1)	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data Output
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register Output
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Code Input
EE	Erase	2	Write	X	20h	Write	Sector Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSR or RSIG instruction is followed by read operations to Read Memory Array, Read Status Register or Read Electronic Signature codes. Any number or read cycles may be performed after an RD, RSR or RSIG instructions.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Memory Array / Reset

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the Array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and sector erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte programming takes typically 9µs, sector erase typically 1.6 seconds. Erasure of a memory sector may be suspended in order to read data from another sector and then resumed.

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	The RY/$\overline{BY}$ output or the P/E.C. status bit may be checked during Program or Erase. The bit should be checked on completion before checking bits b4 or b5 for success.
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction the ESS bit is set to '1' and the P/ECS bit remains at '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In Progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte or word.
			'0'	Program Success	If PS and ES bits are set to '1' during a sector erase attempt, an improper command sequence was entered and the instruction should be given again.
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction is executed and the instruction is aborted. The Status Register must be cleared before another write or erase operation is attempted.
			'0'	V_{PP} OK	
	2	Reserved			Bits b2, b1 and b0 are reserved for future use and should be masked out when polling the Status Register.
	1	Reserved			
	0	Reserved			

Note: Logic level '1' is High, '0' is Low.

A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. In addition a Ready/Busy output RY/$\overline{BY}$ indicates the status of the P/E.C. After Programming or Erasure the command interface must be reset by giving the Read Memory Array instruction before the memory contents can be accessed.

Power Saving

The M28F841 memory have a number of power saving features. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down $\overline{RP}$ signals are at V_{CC}, when the supply current drops to typically 30µA. A deep power down mode is enabled when the Reset/Power Down signal $\overline{RP}$ is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 1µs maximum, with instructions to the C.I. recognized after 400ns.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

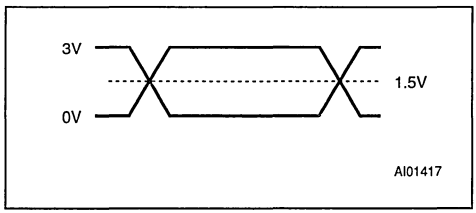


Figure 4. AC Testing Load Circuit

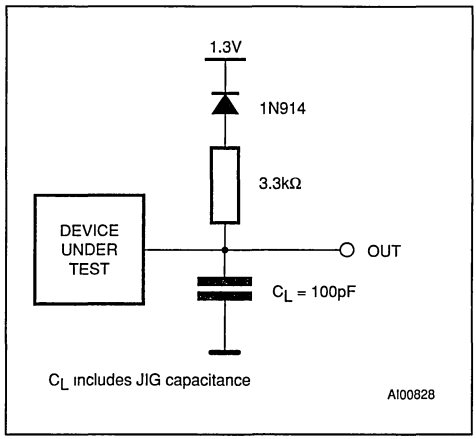


Table 8. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

DEVICE OPERATION

Signal Descriptions

A0-A19 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte to be programmed or a command to the C.I., are latched on the rising edge of Chip Enable $\overline{E}$ and Write Enable $\overline{W}$, whichever occurs first. The data output from the memory Array, the Electronic Signature or the Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the C.I. and the memory Array while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This input allows the memory to be placed in a deep power down mode. If $\overline{RP}$ is within V_{SS} ± 0.2V the lowest supply current is absorbed.

RY/$\overline{BY}$ Read/Busy. This output indicates when the Program Erase Controller is executing a program or erase. It is always active, even during power down. If RY/$\overline{BY}$ is at V_{OL}, the P/E.C. is active.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. This controls writing to the C.I., Address and Input Data latches. Both Addresses and Input Data are latched on the rising edge of $\overline{W}$.

V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{CC} Supply Voltage. This is the main circuit supply.

V_{SS} Ground. This is the reference for all the voltage measurements.

Table 9. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 0.5V; V_{PP} = 12V ± 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 8MHz		30	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, $\overline{G} = V_{SS}$, f = 8MHz		20	mA
I_{CC1} (1, 3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1, 3)	Supply Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{CC3} (1, 3)	Supply Current (Program)	Byte program in progress		30	mA
I_{CC4} (1, 3)	Supply Current (Erase)	Sector Erase in progress		30	mA
I_{CC5} (1, 2, 3)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		6	mA
I_{PP}	Program Current (Read)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Standby)	$V_{PP} \le V_{CC}$		±10	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Byte program in progress		15	mA
I_{PP4}	Program Current (Erase)	Sector Erase in progress		10	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –2mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	V_{CC} + 0.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{LKO}	Supply Voltage (Program or Erase Lock-out)		2		V

Notes: 1. Supply Current specified with I_{OUT} ($RY/\overline{BY}$) = 0.
2. Current increases to $I_{CC} + I_{CC5}$ during a read operation with erase suspended.
3. CMOS levels $V_{CC} \pm 0.2V$ and $V_{SS} \pm 0.2V$. TTL levels V_{IH} and V_{IL}.

Memory Sectors

There are 16, 64K Byte memory sectors. Each sector of the memory can be erased separately, but only one sector at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another sector and then resumed.

Programming and erasure of the memory is disabled when the Program Supply Voltage is at V_{PPL}. For successful programming and erasure the Program Supply Voltage must be at V_{PPH} throughout the operation.

Table 10. Read AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 0.5V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	Test Condition	M28F841						Unit
				-100		-120		-150		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		1		1		1	µs
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		50		50	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		50		50		55	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		40		50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be Low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. A read operation will output a byte on DQ0-DQ7.

The data read depends on the previous command written to the C.I. (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$. As for read operations data is transferred on DQ0-DQ7.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Figure 5. Read Mode AC Waveforms

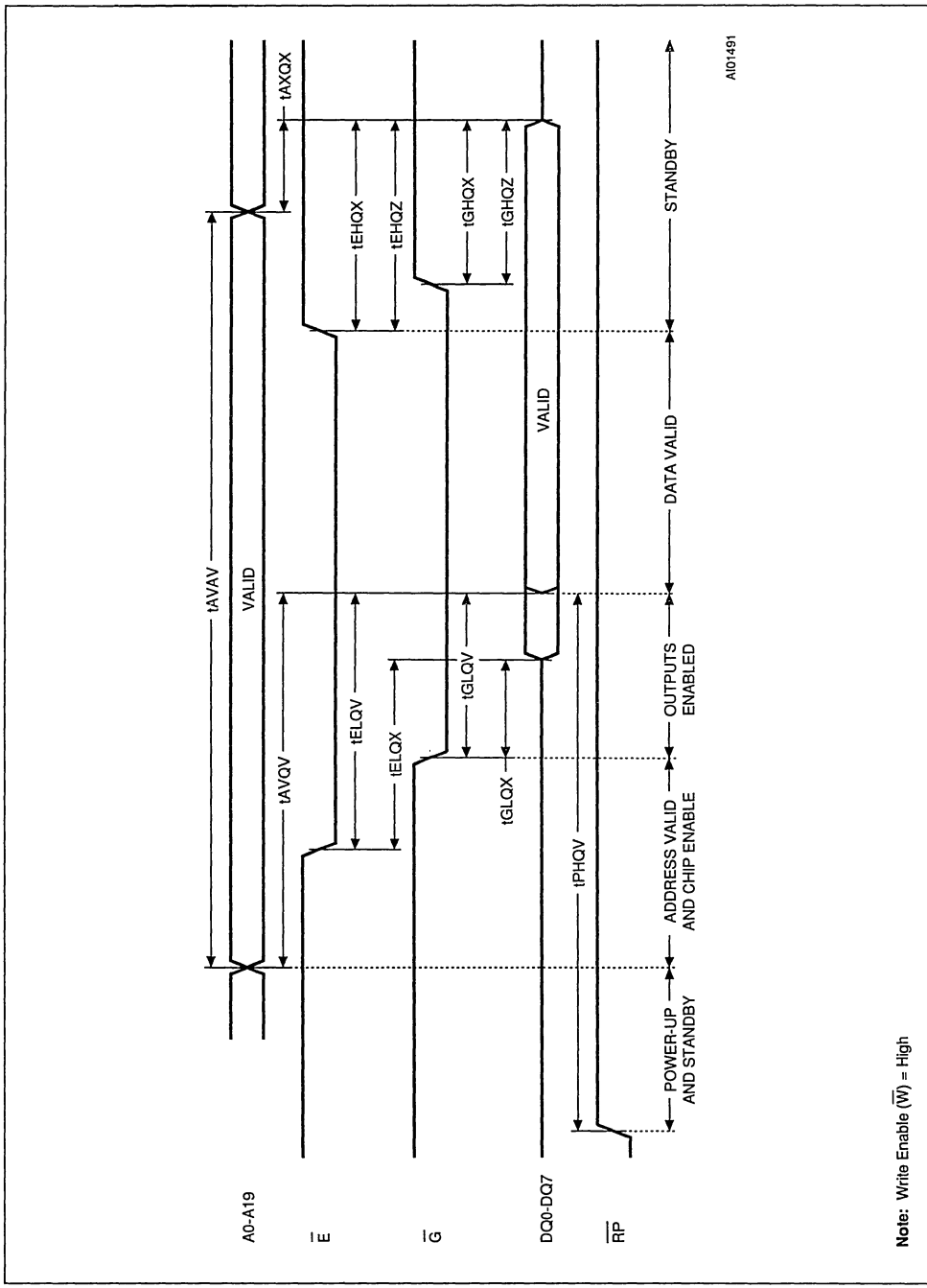


Table 11. Byte Program, Erase Time
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 0.5V)

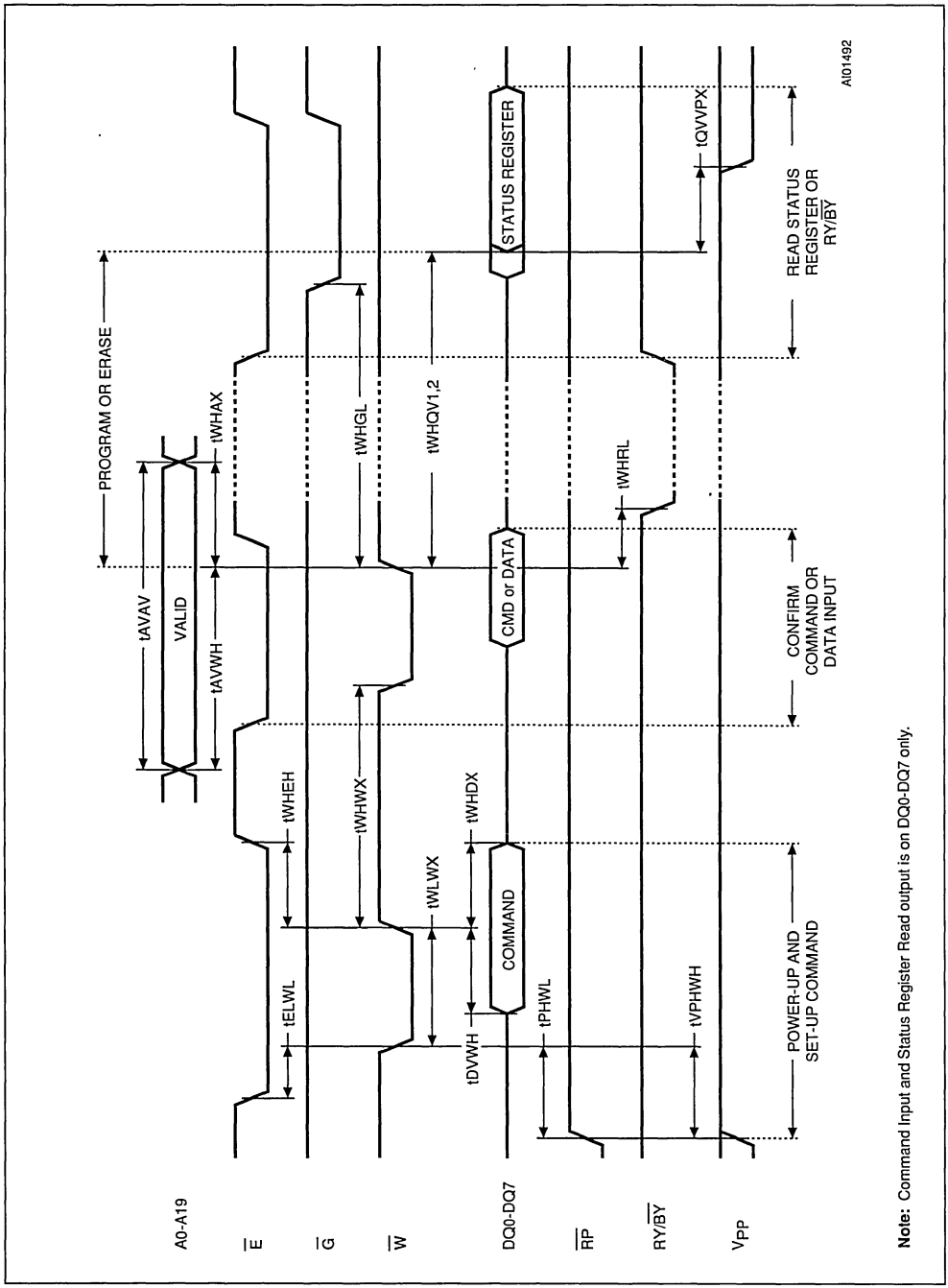
Parameter	Test Conditions	M28F841			Unit
		Min	Typ	Max	
Block Program	V_{PP} = 12V ± 5%		0.6	2.1	sec
Block Erase	V_{PP} = 12V ± 5%		1.6	10	sec

Table 12. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 0.5V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F841						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHWL} (1)	t_{PS}	Power Down High to Write Enable Low	1		1		1		µs
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWX}	t_{WP}	Write Enable Low to Write Enable Transition	40		40		40		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	40		40		40		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	5		5		5		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		10		ns
t_{WHWX}	t_{WPH}	Write Enable High to Write Enable Transition	30		30		30		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	40		40		40		ns
t_{VPHWH} (1)	t_{VPS}	V_{PP} High to Write Enable High	100		100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	5		5		5		ns
t_{WHGL}		Write Enable High to Output Enable Low	0		0		0		ns
t_{WHRL}		Write Enable High to Ready Busy Low		100		100		100	ns
t_{WHQV1} (2)		Write Enable High to Output Valid (Byte Program)	6		6		6		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Sector Erase)	0.3		0.3		0.3		sec
t_{QVVPX} (1, 2)	t_{VPH}	Output Valid or Ready Busy High to V_{PP} Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. Byte Program and Sector Erase durations are measured to completion as indicated by Status Register b7 = 1 or RY/$\overline{BY}$ = high. V_{PP} is held high until Status Register bits b3, b4 and b5 indicate Program or Sector Erase success.
3. Temperature range 0 to 70 °C (grade 1) only.

Figure 6. Program & Erase AC Waveforms, $\overline{W}$ Controlled



Note: Command Input and Status Register Read output is on DQ0-DQ7 only.

Table 13. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{CC} = 5V ± 0.5V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F841						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHEL} (1)	t_{PS}	Power Down High to Chip Enable Low	1		1		1		µs
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEX}	t_{CP}	Chip Enable Low to Chip Enable Transition	50		50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	40		40		40		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	5		5		5		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	5		5		5		ns
t_{EHEX}	t_{EPH}	Chip Enable High to Chip Enable Transition	25		25		25		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	40		40		40		ns
t_{VPHEH} (1)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	5		5		5		ns
t_{EHGL}		Chip Enable High to Output Enable Low	0		0		0		ns
t_{EHRL}		Chip Enable High to Ready Busy Low		100		100		100	ns
t_{EHQV1} (2)		Chip Enable High to Output Valid (Byte Program)	6		6		6		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Sector Erase)	0.3		0.3		0.3		sec
t_{QVVPX} (1, 2)	t_{VPH}	Output Valid or Ready Busy High to V_{PP} Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. Byte Program and Sector Erase durations are measured to completion as indicated by Status Register b7 = 1 or RY/$\overline{BY}$ = high. V_{PP} is held high until Status Register bits b3, b4 and b5 indicate Program or Sector Erase success.
3. Temperature range 0 to 70 °C (grade 1) only.

Figure 7. Program & Erase AC Waveforms, $\overline{E}$ Controlled

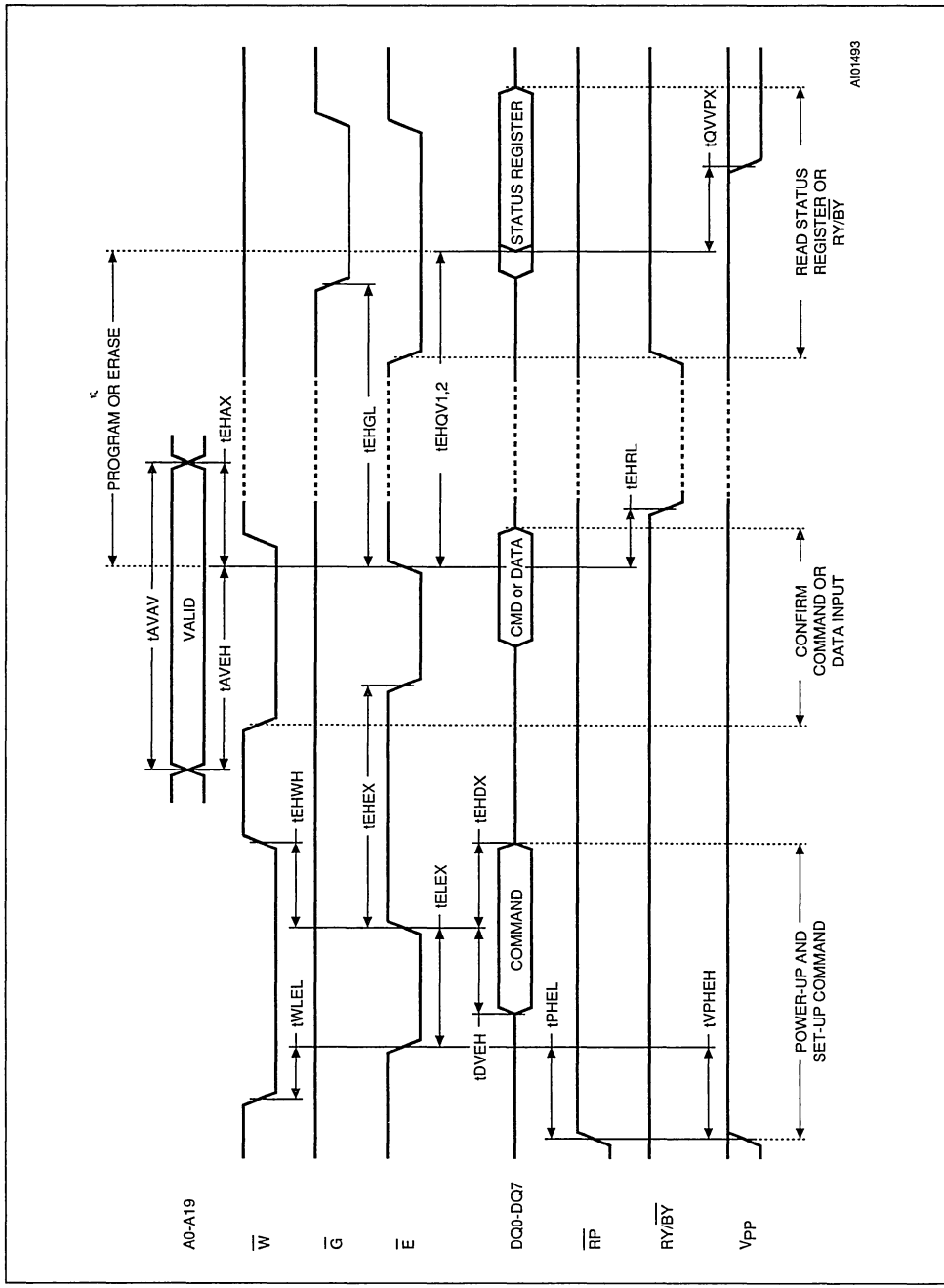
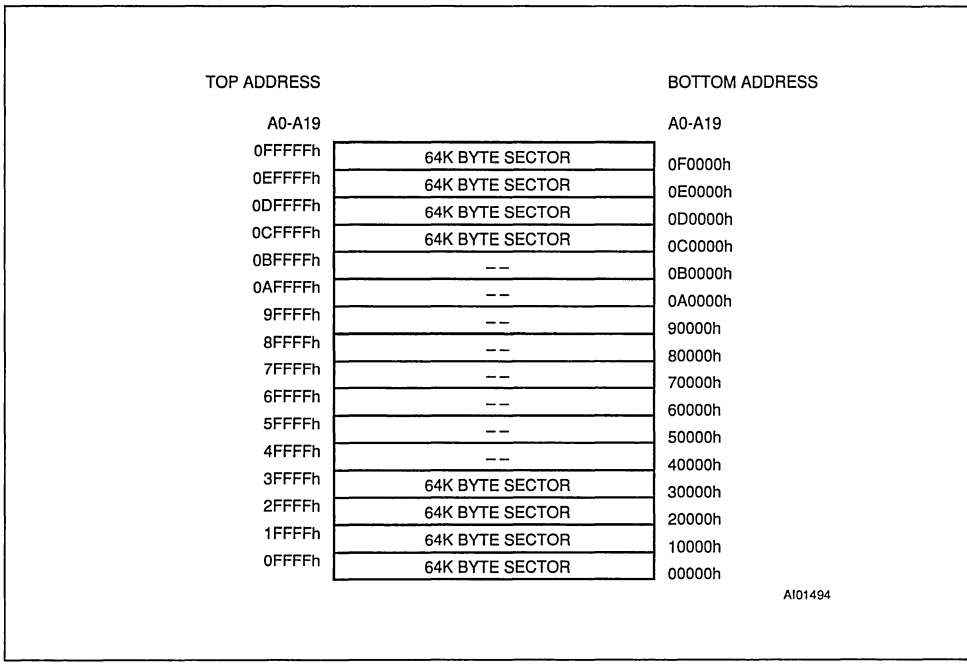


Figure 8. Memory Map, Byte-wide Addresses



Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is Low. The power consumption is reduced to the power down level and the outputs are high impedance independent of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory, the manufacturer code for SGS-THOMSON is 20h and the device code for the M28F841 is 0FCh. These codes allow applications to match their interfaces to the characteristics of the particular manufacturer's product.

The two Electronic Signature codes are output by a read operations with the Address line A0 at V_{IL} or V_{IH}, following an instruction RSIG to the memory.

Instructions and Commands

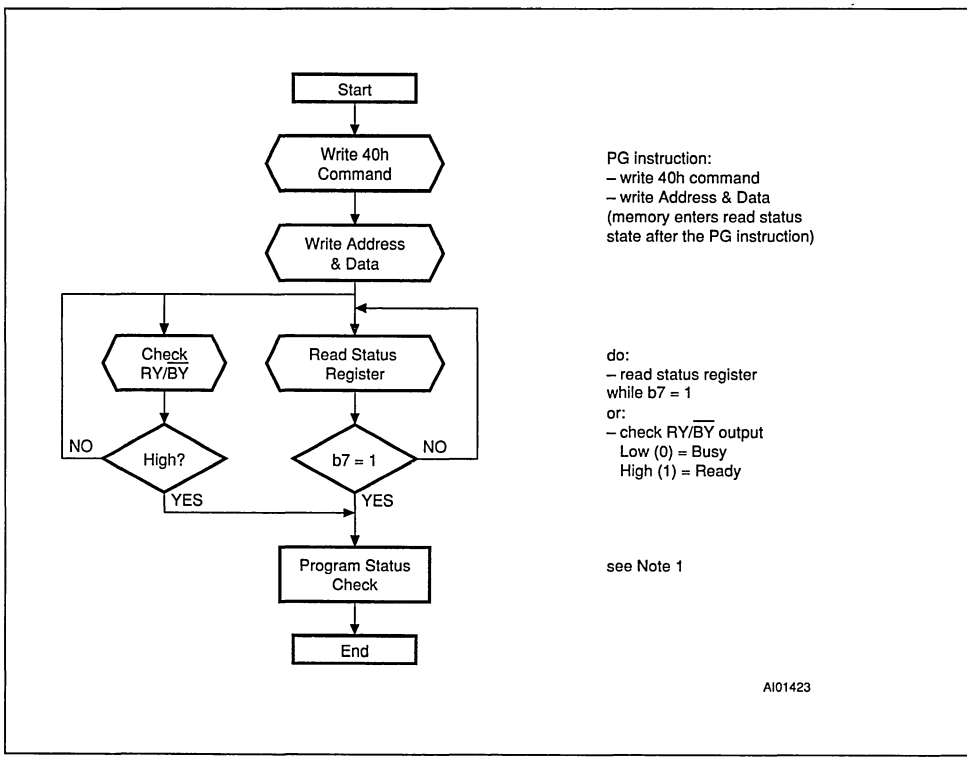
The memory includes a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from one to 3 operations, the first of which is always a write operation followed by either a further write operation to input address and data or to confirm the command, or a read operation to output data.

A Status Register indicates the P/E.C. status Ready/Busy, the suspend/in-progress status of erase operations, the failure/success of erase and program operations and the low/correct value of the V_{PP} Program Supply Voltage.

The P/E.C. sets status bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The status register can be read by the Read Status Register RSR instruction and cleared by the Clear Status Register CLRS instruction. The meaning of the register bits b3 to b7 is shown in Table 7. Bit b0 to b2 are reserved for future use and should be masked out during status checks.

The P/E.C. Ready/Busy status is also indicated by the RY/$\overline{BY}$ output.

Figure 9. Program Flow-chart and Pseudo Code



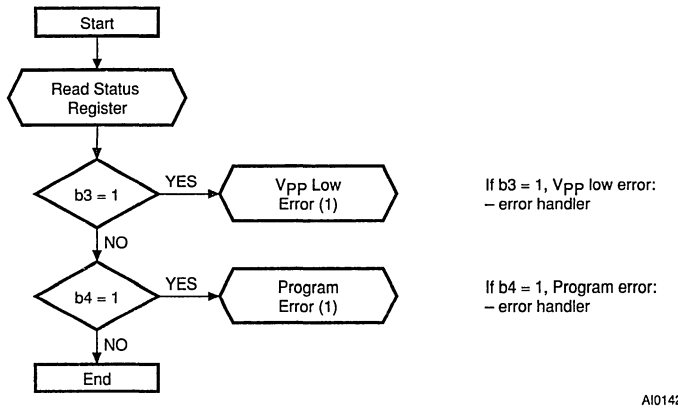
Note: 1. Status check of b7 can be made after each byte programming or after a sequence.

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read data from the addressed byte of the memory array, until a new command is written to the C.I.

Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent read operations output the contents of the status register. The contents are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the status register.

Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h, followed by two read operations to output the manufacturer and device codes. The manufacturer code is output when the address line A0 is Low and the device code when A0 is High.

Figure 10. Program Status Check Flow-chart and Pseudo Code



Note: 1. If a V_{PP} Low or Program error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Erase (EE) instruction. The memory can be erased in sectors. The Program Supply Voltage V_{PPH} must be applied before the Erase (EE) instruction is given. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second is the Erase Confirm command 0D0h. During the input of the second command an address within the sector to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 & b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the Read Status Register (RSR) or Erase Suspend (ES) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it is completed. After completion the Status Register bit b5 returns '1' if there has been an erase failure because erasure has not been verified after even the maximum number of erase pulses have been given. The Status Register bit b3 returns '1' if the Program Supply Voltage V_{PP} does not remain at V_{PPH} when erasure is attempted and/or proceeding.

V_{PP} must be at V_{PPH} when erasing. Erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or if $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register with the CLRS instruction.

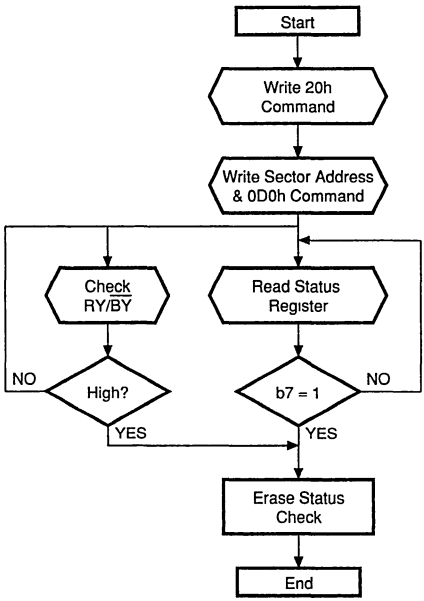
The execution of the erase by the P/E.C. is also indicated by the RY/$\overline{BY}$ output.

A full status check can be made after sector erase. The status check is made on the Status Register bit b3 for any possible V_{PP} error, on bit b5 for an erase error or on both bits b4 & b5 for a command sequence error.

Program (PG) instruction. The memory is programmed byte-by-byte. The Program Supply Voltage V_{PPH} must be applied before the Program (PG) instruction is given and may be applied continuously during programming of a sequence of bytes. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or alternatively 10h). A second write operation latches the address and input data and starts the P/E.C. execution. Read operations output the Status Register after programming has started.

Memory programming is only made by writing a '0' in place of a '1' in a byte. To write a '1' in place of a '0' the Sector must first be erased to all '1's.

Figure 11. Erase Flow-chart and Pseudo Code



Notes: 1. An Erase Suspend may be executed during this loop.
2. See separate flow-chart.

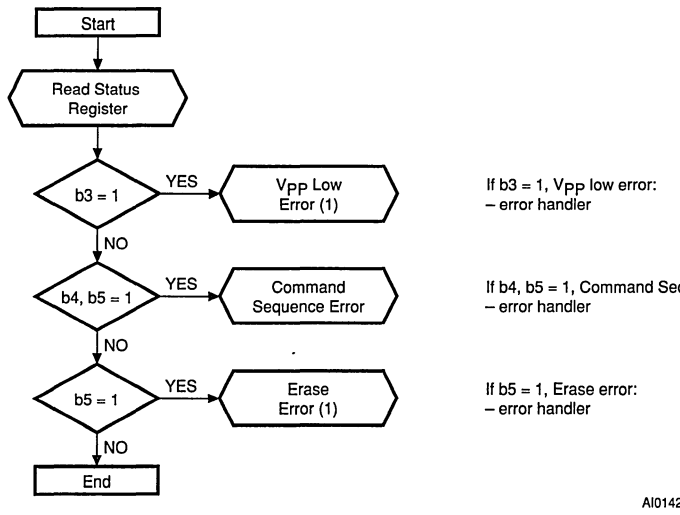
During the execution of the programming the memory accepts only the Read Status Register (RSR) instruction. The Status Register bit b7 returns '0' while programming is in progress and '1' when it is completed. After completion the Status Register bit b4 returns '1' if there has been a program failure. Status Register bit b3 returns a '1' if the Program Supply Voltage V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming.

V_{PP} must be at V_{PPH} when programming. Programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect, the Status Register must be cleared with the Clear Status Register (CLRS) instruction, the sector erased and reprogrammed.

The execution of the programming by the P/E.C. is also indicated by the RY/$\overline{BY}$ output.

A full status check can be made after each byte or after a sequence of bytes has been programmed. The status check is made on the Status Register bit b3 for any possible V_{PP} error and on bit b4 for a programming error.

Figure 12. Erase Status Check Flow-chart and Pseudo Code



Note: 1. If V_{PP} Low or Erase error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Clear Status Register (CLRS) instruction. This instruction uses a single write operation which clears the Status Register bits b3, b4 & b5 to '0'. The CLRS instruction reverts the device to the Read Array mode and is used before any new operation when errors have been detected during programming or erasure.

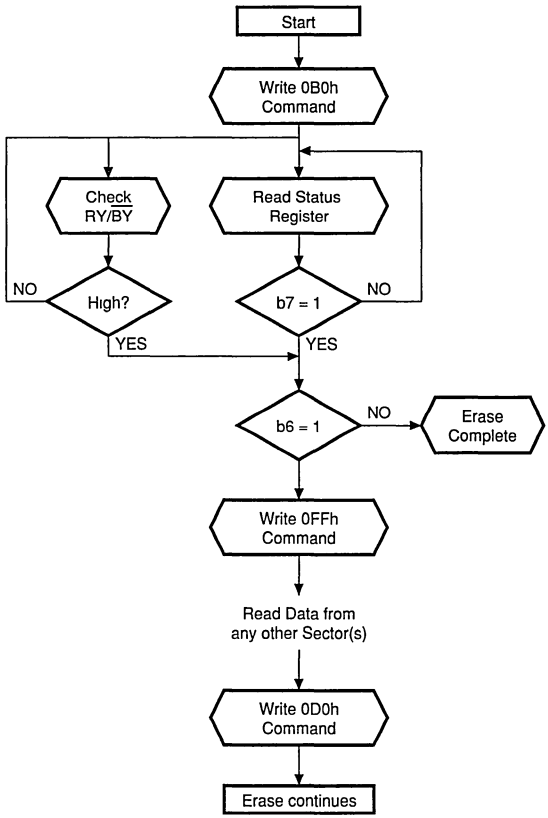
Erase Suspend (ES) instruction. An Erase operation may be suspended by using this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates wether the P/E.C. is suspended, bit b6 = '1', or whether the P/E.C. cycle was the last and the erase is complete, bit b6 = '0'. During suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Immediately following the ES instruction, read operations initially output the contents of the Status Register while erase is suspended, but if a Read (RD) instruction is given data may be read from other sectors of the memory. The Program Supply Voltage V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or if the $\overline{RP}$ input goes Low, the erase operation is aborted and Status Register bits b3 & b5 are set. In this case the Status Register must be cleared and the erase operation repeated to be certain to erase the sector.

Erase Resume (ER) instruction. If an Erase Suspend instruction has been previously executed, the erase operation may be resumed giving the command 0D0h. The Status Register bit b6 will be cleared when erase resumes. Read operations output the Status Register after the erase is resumed.

Reset. After any error has occurred during programming or erase the Status Register must be cleared by giving the Clear Status Register instruction before the memory array may be read.

After a successful program or erase operation either the Read or Clear Status Register instruction must be given before the memory array may be read.

Figure 13. Erase Suspend & Resume Flow-chart and Pseudo Code



ES instruction:
– write 0B0h command
(memory enters read status register state after the ES instruction)

do:
– read status register
while b7 = 1
or:
– check RY/$\overline{BY}$ output
Low (0) = Busy
High (1) = Suspended

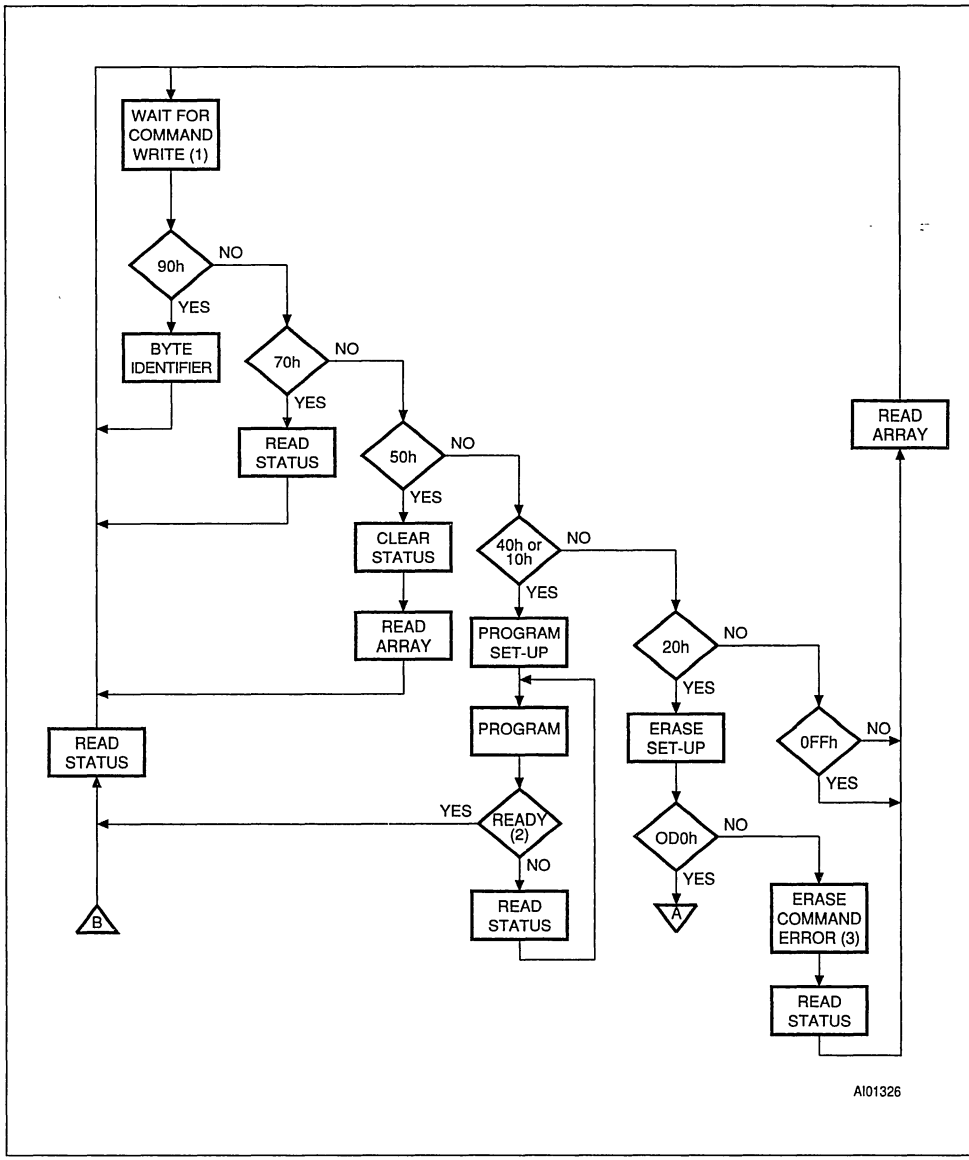
if b6 = 1, Erase is complete

RD instruction:
– write 0FFh command
– read one a more bytes from any other sector(s)

ER instruction:
– write 0D0h command to resume erase

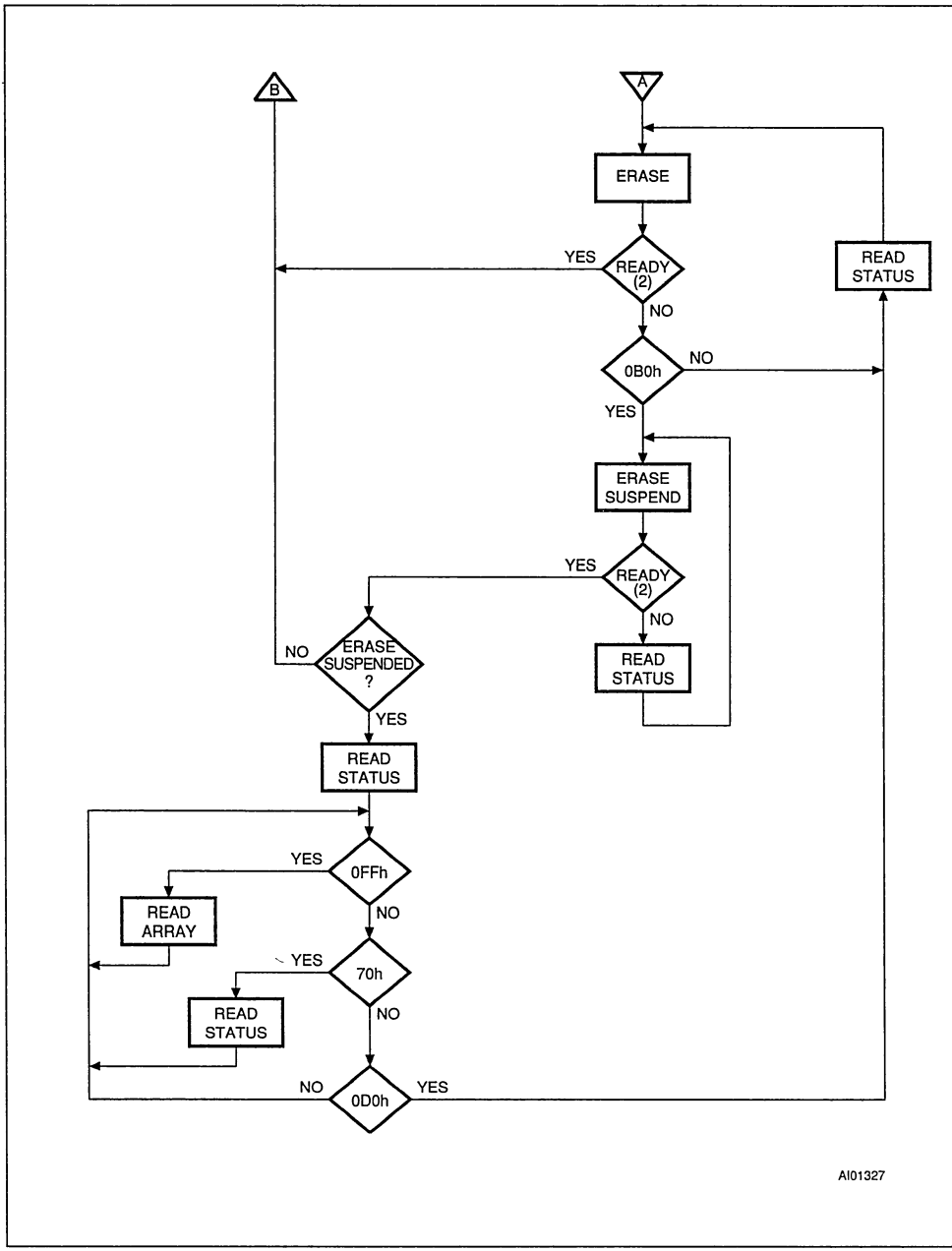
AI01427

Figure 14. Command Interface and Program Erase Controller Flow-diagram (a)



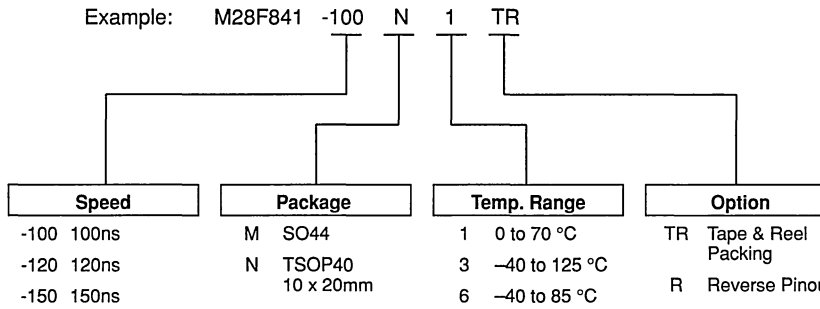
Notes: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.
3. Upon Erase command error, the P/E.C. defaults to Read status and sets bits b4 and b5 of the Status Register. Program and Erase commands will be accepted only after the Status Register has been reset by a CLRS command.

Figure 15. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME



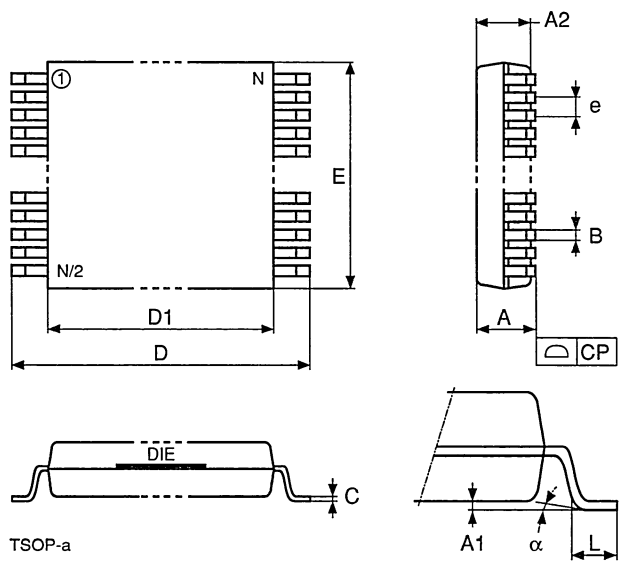
For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP40 Normal Pinout - 40 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		40			40	
CP			0.10			0.004

TSOP40



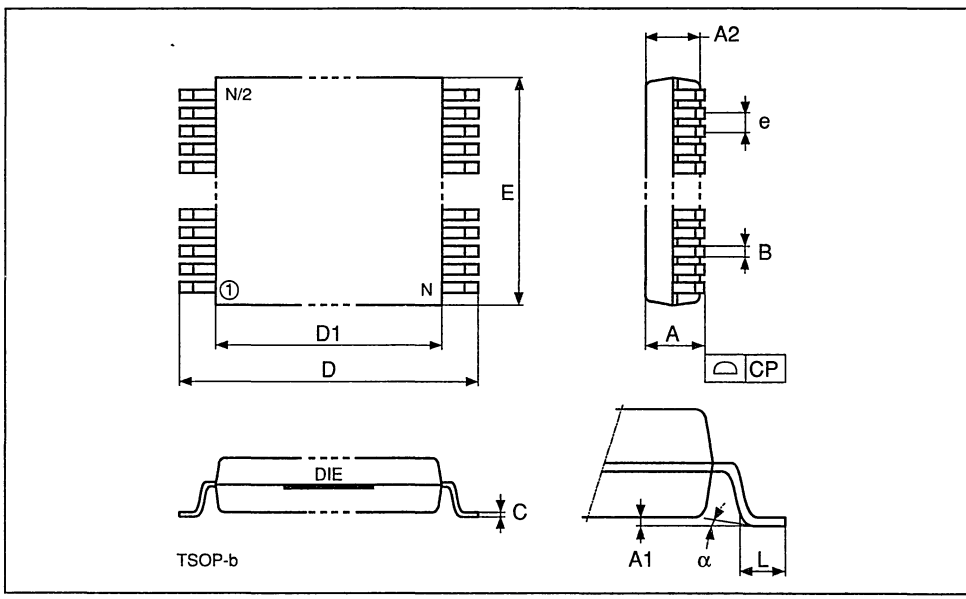
TSOP-a

Drawing is out of scale

TSOP40 Reverse Pinout - 40 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		40			40	
CP			0.10			0.004

TSOP40



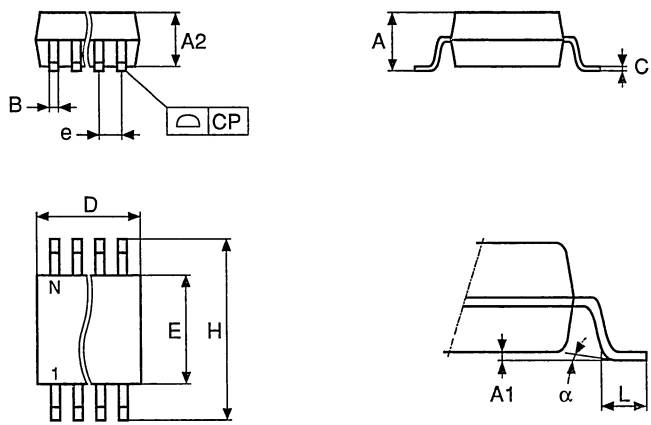
TSOP-b

Drawing is out of scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27	–	–	0.050	–	–
H		15.90	16.10		0.626	0.634
L	0.80	–	–	0.031	–	–
α	3°	–	–	3°	–	–
N		44			44	
CP			0.10			0.004

SO44



SO-b

Drawing is out of scale

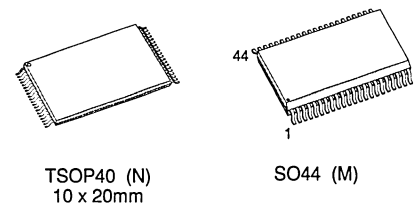
SGS-THOMSON MICROELECTRONICS

M28V841

LOW VOLTAGE 8 Megabit (1 Meg x 8, Sector Erase) FLASH MEMORY

PRODUCT PREVIEW

- SMALL SIZE PLASTIC PACKAGES TSOP40 and SO44
- MEMORY ERASE in SECTORS
  - 16 Sectors of 64K Bytes each
- 3V ± 0.3V SUPPLY VOLTAGE
- 12V ± 5% PROGRAMMING VOLTAGE
- 100,000 PROGRAM/ERASE CYCLES per SECTOR
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Erase by Sector, Erase Suspend/Resume Ready/Busy Output
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
- HIGH SPEED ACCESS TIME: 100ns
- EXTENDED TEMPERATURE RANGE
- COMPATIBLE to 16 MEGABIT FLASH MEMORY
  - Equal Software Command Set
  - Pinout Compatible



TSOP40 (N)
10 x 20mm

SO44 (M)

Figure 1. Logic Diagram

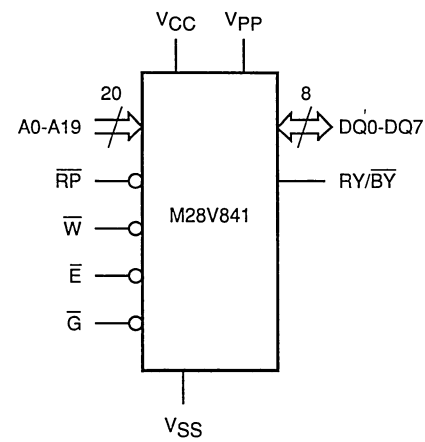
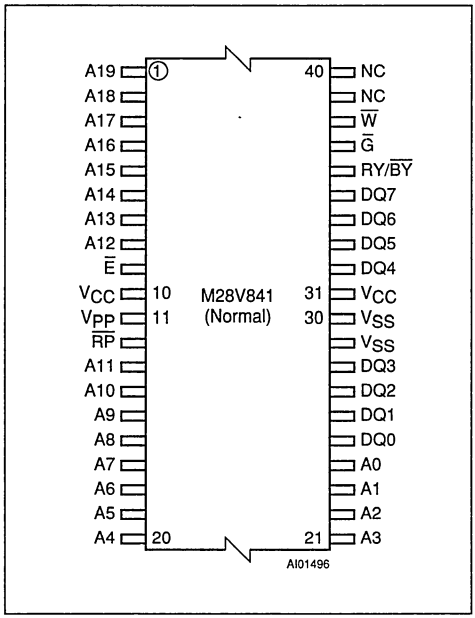


Table 1. Signal Names

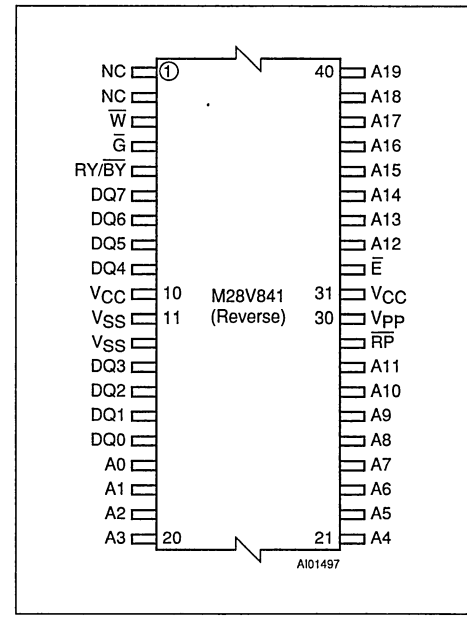
A0-A19	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power Down
RY/$\overline{BY}$	Ready/Busy Output
V_{PP}	Program & Erase Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. TSOP Pin Connections



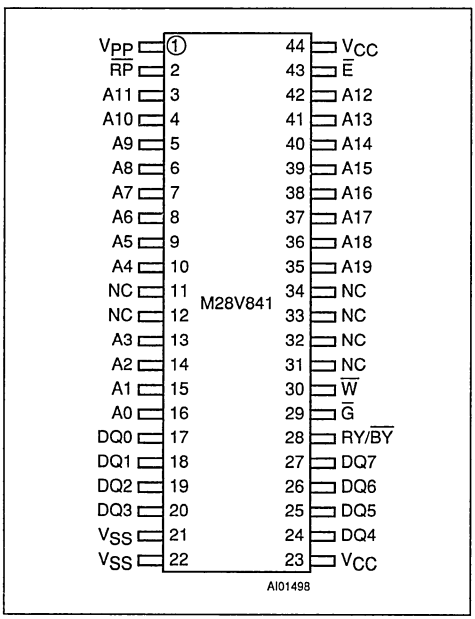
Warning: NC = No Connections

Figure 2B. TSOP Reverse Pin Connections



Warning: NC = No Connections

Figure 2C. SO Pin Connections



Warning: NC = No Connections

DESCRIPTION

The M28V841 FLASH MEMORY product is a non-volatile memory that may be erased electrically at the sector level and programmed byte-by-byte. The interface is directly compatible with most microprocessors. It is intended for computer file systems and mass data storage applications. TSOP40 and S044 packages are used. The M28V841 is software and pin-out, footprint compatible with the M28V161, 16 Megabit FLASH Memory, with the simple substraction of an address line.

Organization

The organization is 1 Meg x 8 with Address lines A0-A19 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down input places the memory in deep power down. A Ready/Busy output indicates the status of the internal Program/Erase Controller (P/E.C.).

Sectors

Erasure of the memory is in sectors. There are 16 sectors in the memory address space, each of 64K bytes. Programming of each sector takes typically 0.6 seconds and erasure 1.6 seconds, each sector may be programmed and erased over 100,000 cycles. All sectors are protected from programming

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 5	V
V_{CC}	Supply Voltage		–0.6 to 5	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
I_{OUT} (4)	Output Short Circuit Current		100	mA

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 5V allowed for less than 20ns.
4. Only one output shorted at a time for no longer than 1 second.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	RY/$\overline{BY}$ (2)	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OH}	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{OL} / V_{OH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{OH}	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	V_{OH}	Hi-Z
Power Down	X	X	X	V_{IL}	V_{OH}	Hi-Z

Notes: 1. X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}
2. RY/$\overline{BY}$ = V_{OL} when the P/E.C. is executing a Sector Erase or Write operation. It is at V_{OH} when the P/E.C. is not busy, in the Erase Suspend or Power Down modes.

Table 4. Electronic Signature

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	A0	RY/$\overline{BY}$	DQ0 - DQ7
Manufact. Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{OH}	20h
Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{OH}	0FDh

DESCRIPTION (cont'd)

or erasure when the Reset/Power Down $\overline{RP}$ signal is Low. Sector erase may be suspended while data is read from other sectors of the memory, then resumed.

Bus operations

Five operations can be performed by the appropriate bus cycles, Read a Byte from the Array, Output Disable, Standby, Power Down and Write a Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor then memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address (1)	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data Output
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register Output
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Code Input
EE	Erase	2	Write	X	20h	Write	Sector Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSR or RSIG instruction is followed by read operations to Read Memory Array, Read Status Register or Read Electronic Signature codes. Any number or read cycles may be performed after an RD, RSR or RSIG instructions.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Memory Array / Reset

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the Array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and sector erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte programming takes typically 9µs, sector erase typically 1.6 seconds. Erasure of a memory sector may be suspended in order to read data from another sector and then resumed.

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	The RY/$\overline{BY}$ output or the P/E.C. status bit may be checked during Program or Erase. The bit should be checked on completion before checking bits b4 or b5 for success.
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction the ESS bit is set to '1' and the P/ECS bit remains at '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In Progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte or word.
			'0'	Program Success	If PS and ES bits are set to '1' during a sector erase attempt, an improper command sequence was entered and the instruction should be given again.
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction is executed and the instruction is aborted. The Status Register must be cleared before another write or erase operation is attempted.
			'0'	V_{PP} OK	
	2	Reserved			Bits b2, b1 and b0 are reserved for future use and should be masked out when polling the Status Register.
	1	Reserved			
	0	Reserved			

Note: Logic level '1' is High, '0' is Low.

A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. In addition a Ready/Busy output RY/$\overline{BY}$ indicates the status of the P/E.C. After Programming or Erasure the command interface must be reset by giving the Read Memory Array instruction before the memory contents can be accessed.

Power Saving

The M28V841 memory have a number of power saving features. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down $\overline{RP}$ signals are at V_{CC}, when the supply current drops to typically 30µA. A deep power down mode is enabled when the Reset/Power Down signal $\overline{RP}$ is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 1µs maximum, with instructions to the C.I. recognized after 400ns.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

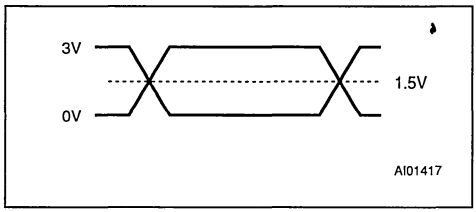


Figure 4. AC Testing Load Circuit

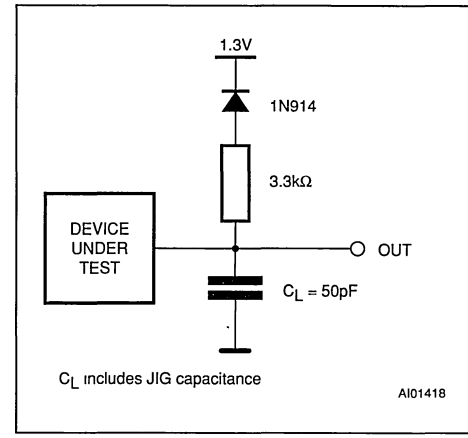


Table 8. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

DEVICE OPERATION

Signal Descriptions

A0-A19 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte to be programmed or a command to the C.I., are latched on the rising edge of Chip Enable $\overline{E}$ and Write Enable $\overline{W}$, whichever occurs first. The data output from the memory Array, the Electronic Signature or the Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the C.I. and the memory Array while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This input allows the memory to be placed in a deep power down mode. If $\overline{RP}$ is within V_{SS} ± 0.2V the lowest supply current is absorbed.

RY/$\overline{BY}$ Read/Busy. This output indicates when the Program Erase Controller is executing a program or erase. It is always active, even during power down. If RY/$\overline{BY}$ is at V_{OL}, the P/E.C. is active.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. This controls writing to the C.I., Address and Input Data latches. Both Addresses and Input Data are latched on the rising edge of $\overline{W}$.

V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{CC} Supply Voltage. This is the main circuit supply.

V_{SS} Ground. This is the reference for all the voltage measurements.

Table 9. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 8MHz		30	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, $\overline{G} = V_{SS}$, f = 8MHz		20	mA
I_{CC1} (1, 3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1, 3)	Supply Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{CC3} (1, 3)	Supply Current (Program)	Byte program in progress		30	mA
I_{CC4} (1, 3)	Supply Current (Erase)	Sector Erase in progress		30	mA
I_{CC5} (1, 2, 3)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		6	mA
I_{PP}	Program Current (Read)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Standby)	$V_{PP} \le V_{CC}$		±10	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Byte program in progress		15	mA
I_{PP4}	Program Current (Erase)	Sector Erase in progress		10	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –2mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	V_{CC} + 0.3	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{LKO}	Supply Voltage (Program or Erase Lock-out)		2		V

Notes: 1. Supply Current specified with I_{OUT} ($RY/\overline{BY}$) = 0.
2. Current increases to I_{CC} + I_{CC5} during a read operation with erase suspended.
3. CMOS levels V_{CC} ± 0.2V and V_{SS} ± 0.2V. TTL levels V_{IH} and V_{IL}.

Memory Sectors

There are 16, 64K Byte memory sectors. Each sector of the memory can be erased separately, but only one sector at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another sector and then resumed.

Programming and erasure of the memory is disabled when the Program Supply Voltage is at V_{PPL}. For successful programming and erasure the Program Supply Voltage must be at V_{PPH} throughout the operation.

Table 10. Read AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	Test Condition	M28V841						Unit
				-100		-120		-150		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		1		1		1	µs
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		50		50	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		50		50		55	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		40		50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down and Electronic Signature Read. They are shown in Table 3.

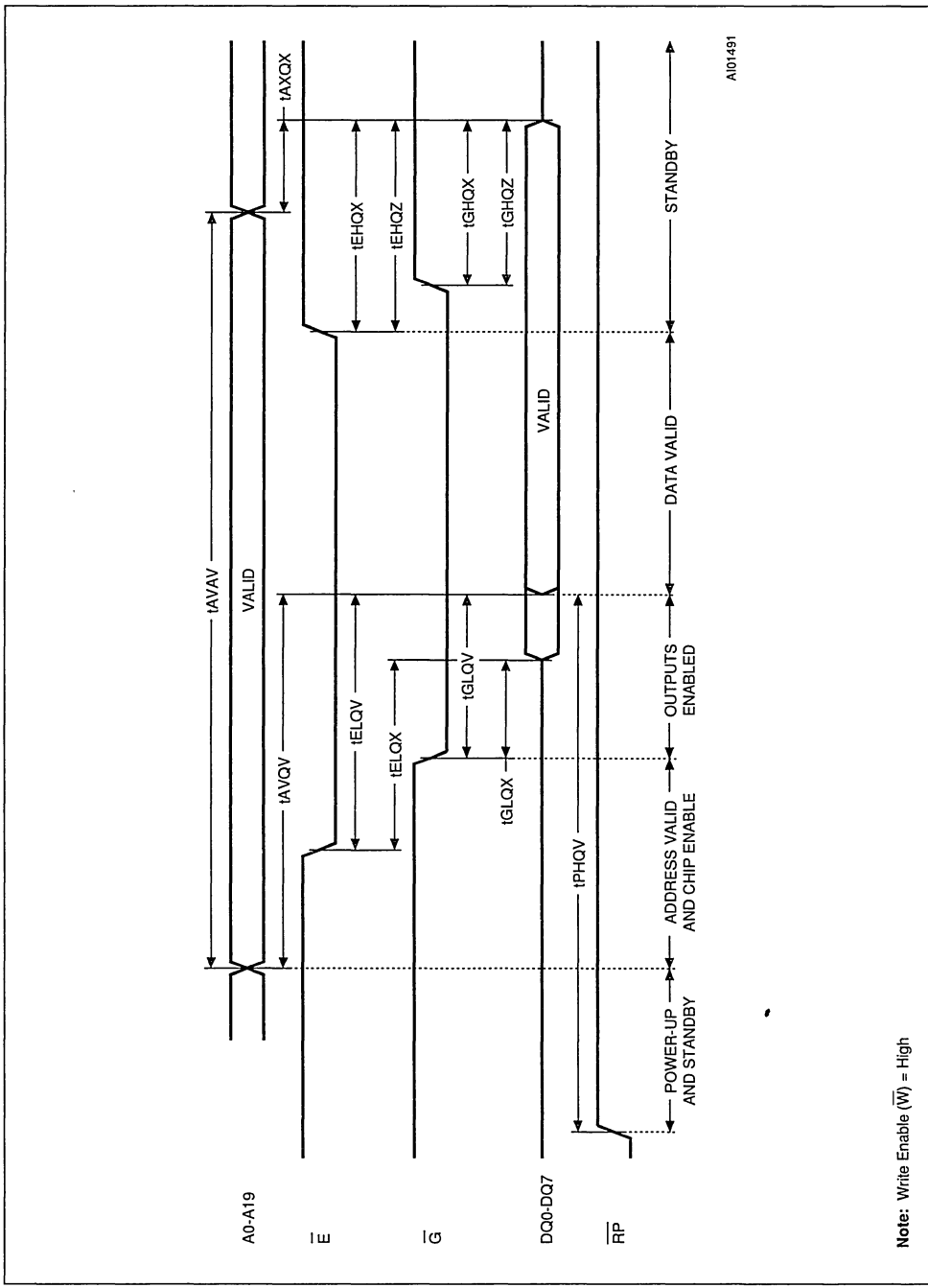
Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be Low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. A read operation will output a byte on DQ0-DQ7.

The data read depends on the previous command written to the C.I. (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$. As for read operations data is transferred on DQ0-DQ7.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Figure 5. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Table 11. Byte Program, Erase Time
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 3.3V ± 0.3V)

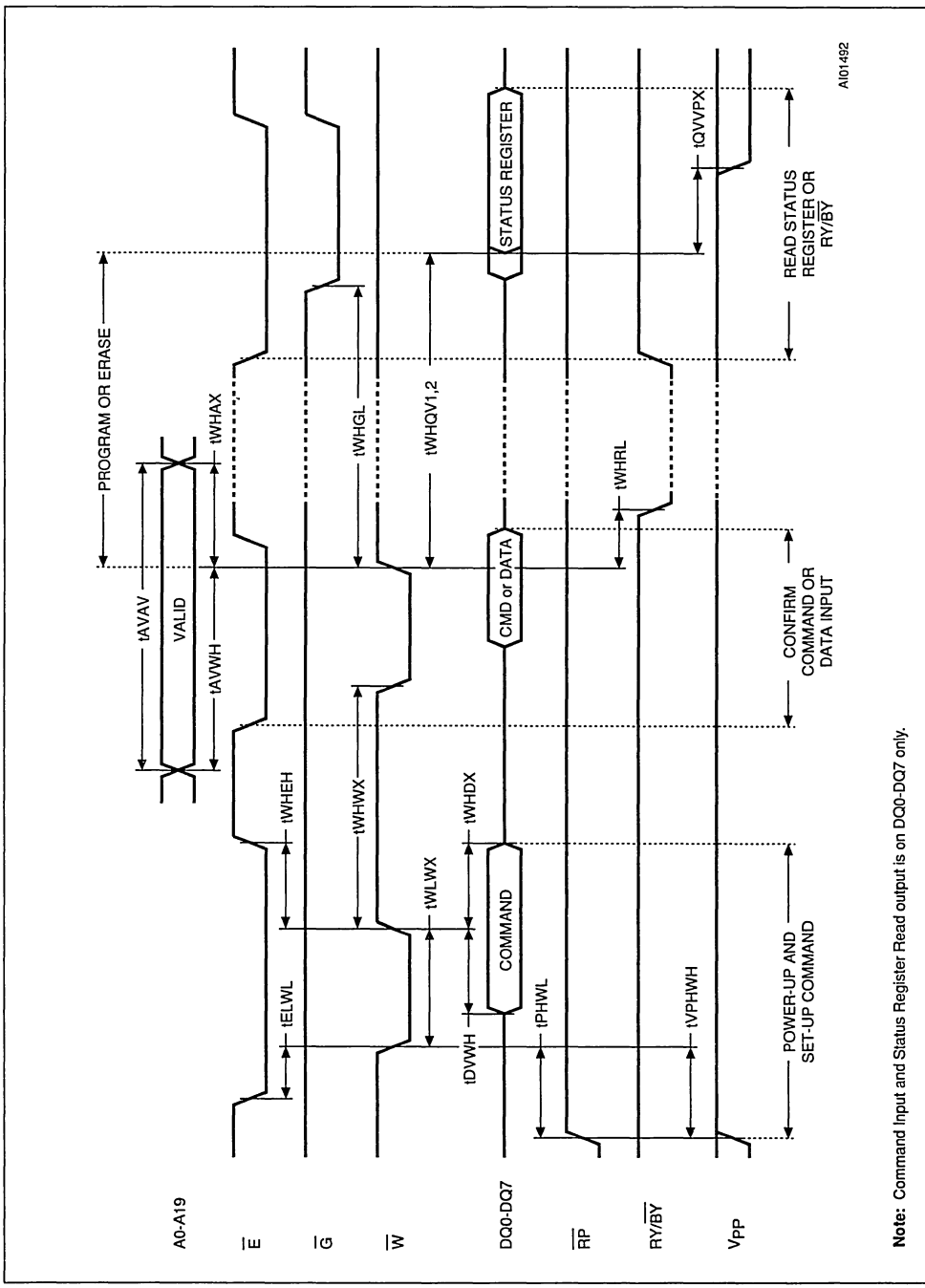
Parameter	Test Conditions	M28V841			Unit
		Min	Typ	Max	
Block Program	V_{PP} = 12V ± 5%		0.6	2.1	sec
Block Erase	V_{PP} = 12V ± 5%		1.6	10	sec

Table 12. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28V841						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHWL} (1)	t_{PS}	Power Down High to Write Enable Low	1		1		1		µs
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWX}	t_{WP}	Write Enable Low to Write Enable Transition	40		40		40		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	40		40		40		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	5		5		5		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		10		ns
t_{WHWX}	t_{WPH}	Write Enable High to Write Enable Transition	30		30		30		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	40		40		40		ns
t_{VPHWH} (1)	t_{VPS}	V_{PP} High to Write Enable High	100		100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	5		5		5		ns
t_{WHGL}		Write Enable High to Output Enable Low	0		0		0		ns
t_{WHRL}		Write Enable High to Ready Busy Low		100		100		100	ns
t_{WHQV1} (2)		Write Enable High to Output Valid (Byte Program)	6		6		6		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Sector Erase)	0.3		0.3		0.3		sec
t_{QVVPX} (1, 2)	t_{VPH}	Output Valid or Ready Busy High to V_{PP} Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. Byte Program and Sector Erase durations are measured to completion as indicated by Status Register b7 = 1 or RY/$\overline{BY}$ = high. V_{PP} is held high until Status Register bits b3, b4 and b5 indicate Program or Sector Erase success.
3. Temperature range 0 to 70 °C (grade 1) only.

Figure 6. Program & Erase AC Waveforms, $\overline{W}$ Controlled



Note: Command Input and Status Register Read output is on DQ0-DQ7 only.

Table 13. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28V841						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHEL} (1)	t_{PS}	Power Down High to Chip Enable Low	1		1		1		µs
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEX}	t_{CP}	Chip Enable Low to Chip Enable Transition	50		50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	40		40		40		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	5		5		5		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	5		5		5		ns
t_{EHEX}	t_{EPH}	Chip Enable High to Chip Enable Transition	25		25		25		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	40		40		40		ns
t_{VPHEH} (1)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	5		5		5		ns
t_{EHGL}		Chip Enable High to Output Enable Low	0		0		0		ns
t_{EHRL}		Chip Enable High to Ready Busy Low		100		100		100	ns
t_{EHQV1} (2)		Chip Enable High to Output Valid (Byte Program)	6		6		6		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Sector Erase)	0.3		0.3		0.3		sec
t_{QVVPX} (1, 2)	t_{VPH}	Output Valid or Ready Busy High to V_{PP} Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. Byte Program and Sector Erase durations are measured to completion as indicated by Status Register b7 = 1 or RY/$\overline{BY}$ = high. V_{PP} is held high until Status Register bits b3, b4 and b5 indicate Program or Sector Erase success.
3. Temperature range 0 to 70 °C (grade 1) only.

Figure 7. Program & Erase AC Waveforms, $\overline{E}$ Controlled

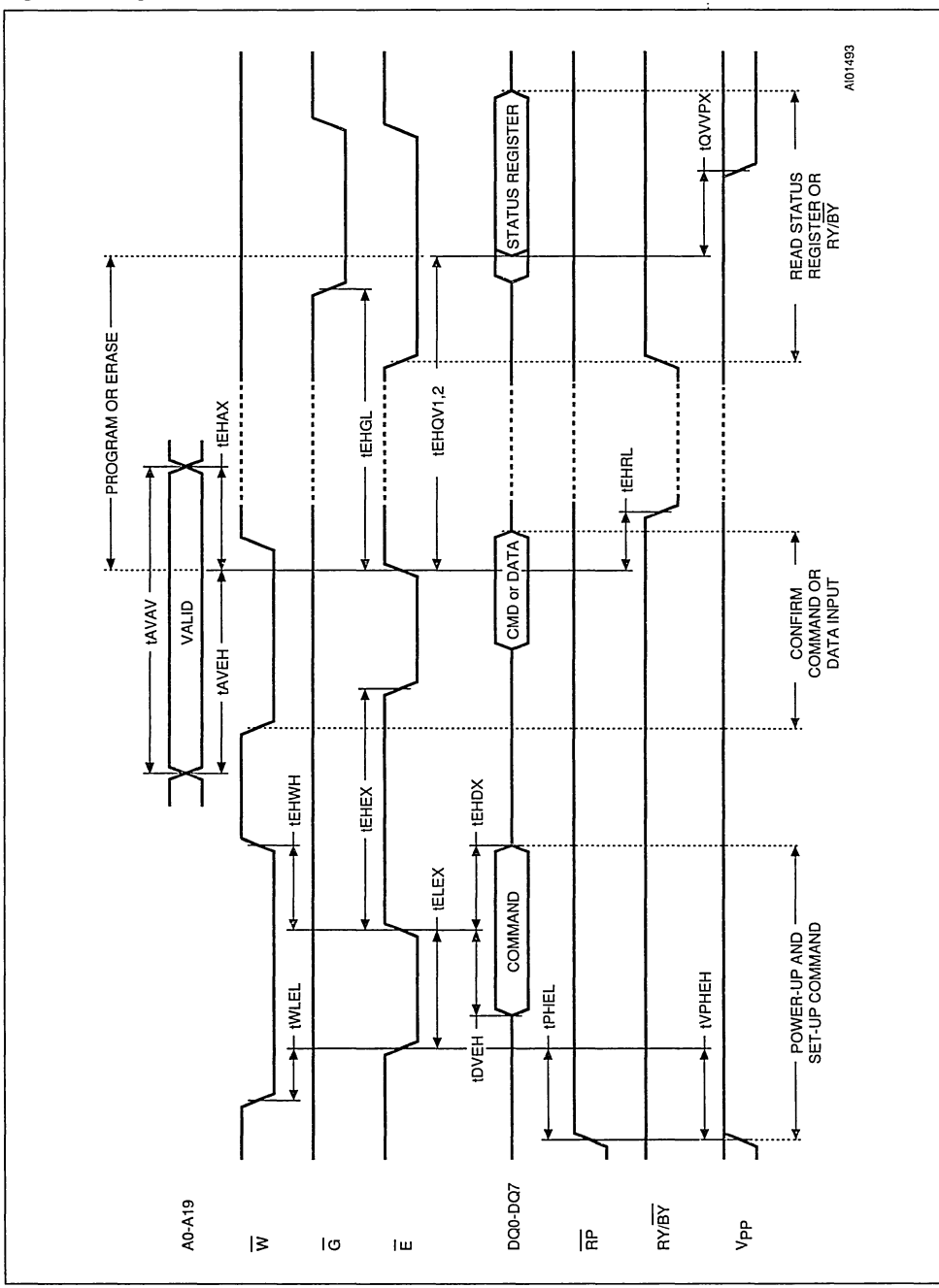
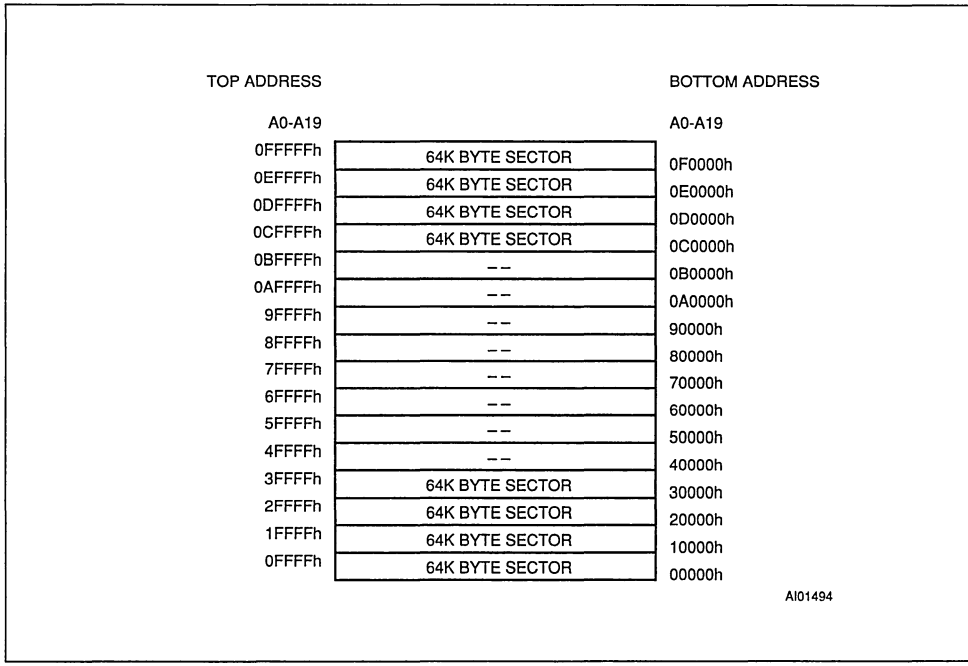


Figure 8. Memory Map, Byte-wide Addresses



Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is Low. The power consumption is reduced to the power down level and the outputs are high impedance independent of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory, the manufacturer code for SGS-THOMSON is 20h and the device code for the M28V841 is 0FDh. These codes allow applications to match their interfaces to the characteristics of the particular manufacturer's product.

The two Electronic Signature codes are output by a read operations with the Address line A0 at V_{IL} or V_{IH}, following an instruction RSIG to the memory.

Instructions and Commands

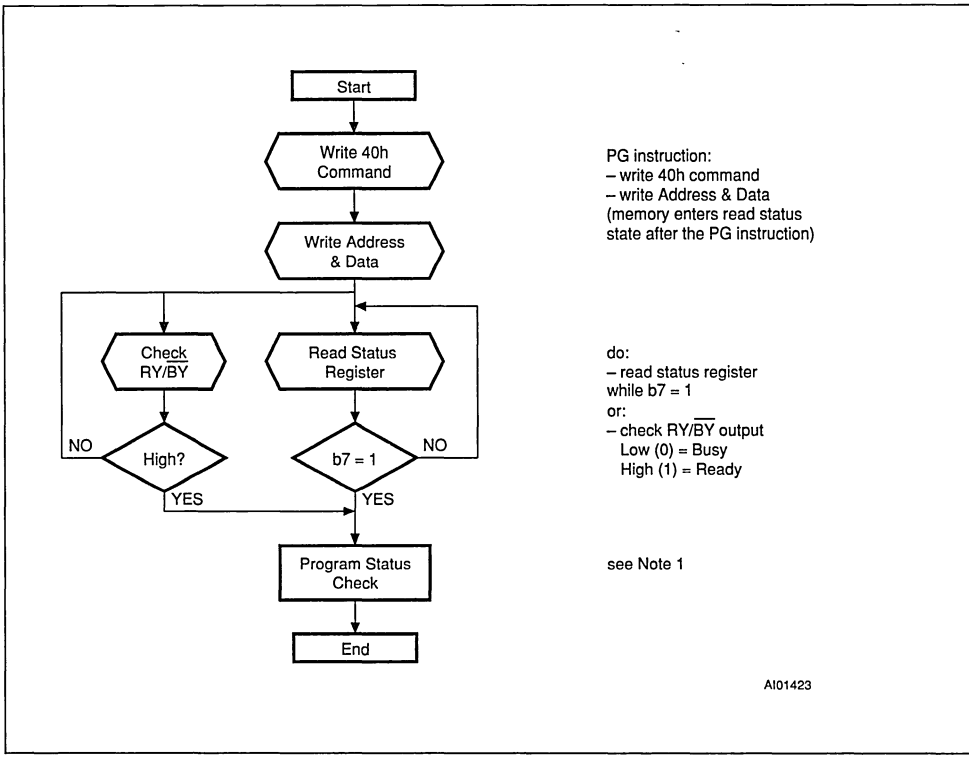
The memory includes a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from one to 3 operations, the first of which is always a write operation followed by either a further write operation to input address and data or to confirm the command, or a read operation to output data.

A Status Register indicates the P/E.C. status Ready/Busy, the suspend/in-progress status of erase operations, the failure/success of erase and program operations and the low/correct value of the V_{PP} Program Supply Voltage.

The P/E.C. sets status bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The status register can be read by the Read Status Register RSR instruction and cleared by the Clear Status Register CLRS instruction. The meaning of the register bits b3 to b7 is shown in Table 7. Bit b0 to b2 are reserved for future use and should be masked out during status checks.

The P/E.C. Ready/Busy status is also indicated by the RY/$\overline{BY}$ output.

Figure 9. Program Flow-chart and Pseudo Code



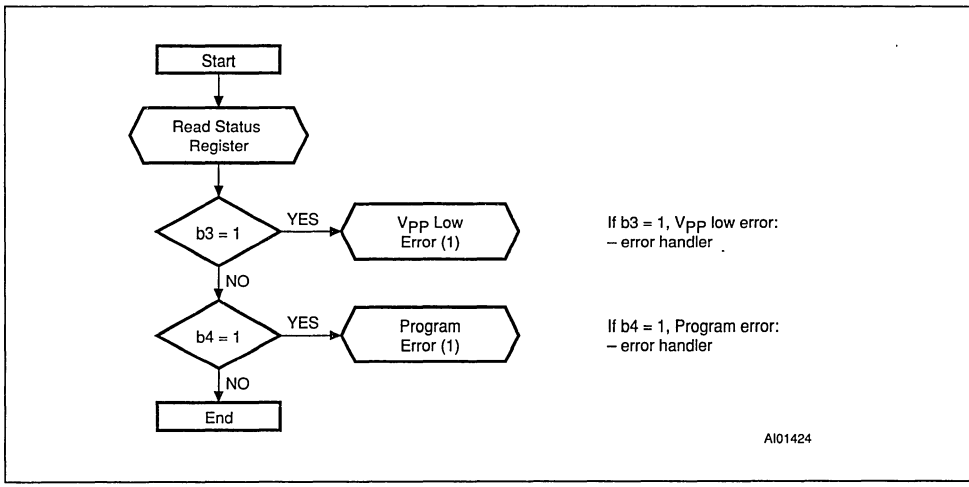
Note: 1. Status check of b7 can be made after each byte programming or after a sequence.

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read data from the addressed byte of the memory array, until a new command is written to the C.I.

Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent read operations output the contents of the status register. The contents are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the status register.

Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h, followed by two read operations to output the manufacturer and device codes. The manufacturer code is output when the address line A0 is Low and the device code when A0 is High.

Figure 10. Program Status Check Flow-chart and Pseudo Code



Note: 1. If a V_{PP} Low or Program error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Erase (EE) instruction. The memory can be erased in sectors. The Program Supply Voltage V_{PPH} must be applied before the Erase (EE) instruction is given. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second is the Erase Confirm command 0D0h. During the input of the second command an address within the sector to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 & b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the Read Status Register (RSR) or Erase Suspend (ES) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it is completed. After completion the Status Register bit b5 returns '1' if there has been an erase failure because erasure has not been verified after even the maximum number of erase pulses have been given. The Status Register bit b3 returns '1' if the Program Supply Voltage V_{PP} does not remain at V_{PPH} when erasure is attempted and/or proceeding.

V_{PP} must be at V_{PPH} when erasing. Erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or if $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register with the CLRS instruction.

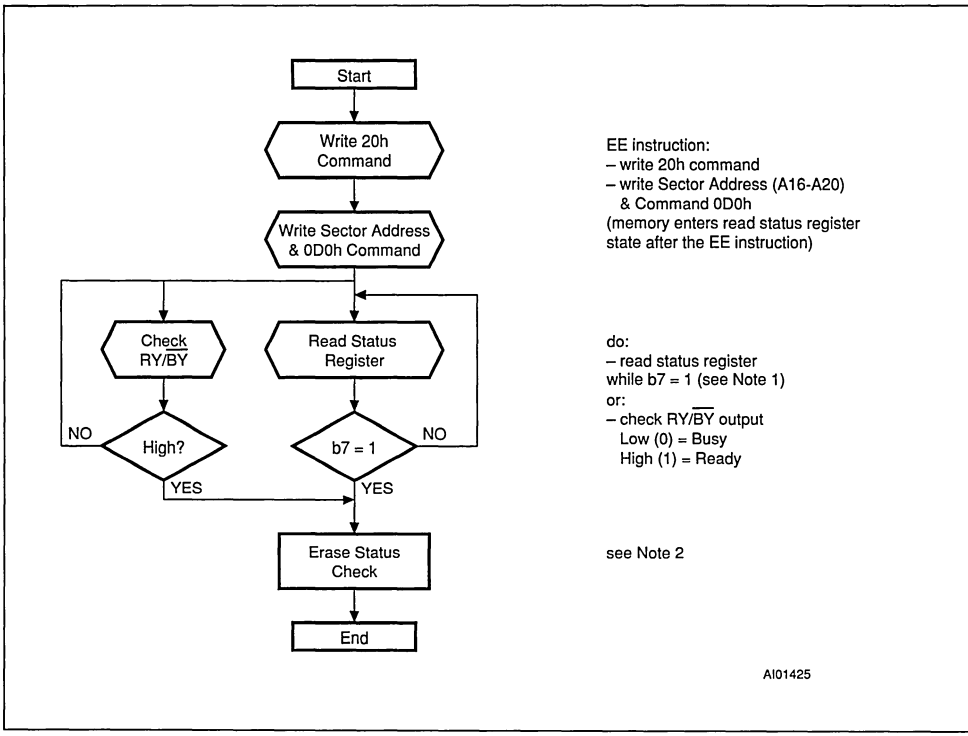
The execution of the erase by the P/E.C. is also indicated by the RY/$\overline{BY}$ output.

A full status check can be made after sector erase. The status check is made on the Status Register bit b3 for any possible V_{PP} error, on bit b5 for an erase error or on both bits b4 & b5 for a command sequence error.

Program (PG) instruction. The memory is programmed byte-by-byte. The Program Supply Voltage V_{PPH} must be applied before the Program (PG) instruction is given and may be applied continuously during programming of a sequence of bytes. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or alternatively 10h). A second write operation latches the address and input data and starts the P/E.C. execution. Read operations output the Status Register after programming has started.

Memory programming is only made by writing a '0' in place of a '1' in a byte. To write a '1' in place of a '0' the Sector must first be erased to all '1's.

Figure 11. Erase Flow-chart and Pseudo Code



Notes: 1. An Erase Suspend may be executed during this loop.
2. See separate flow-chart.

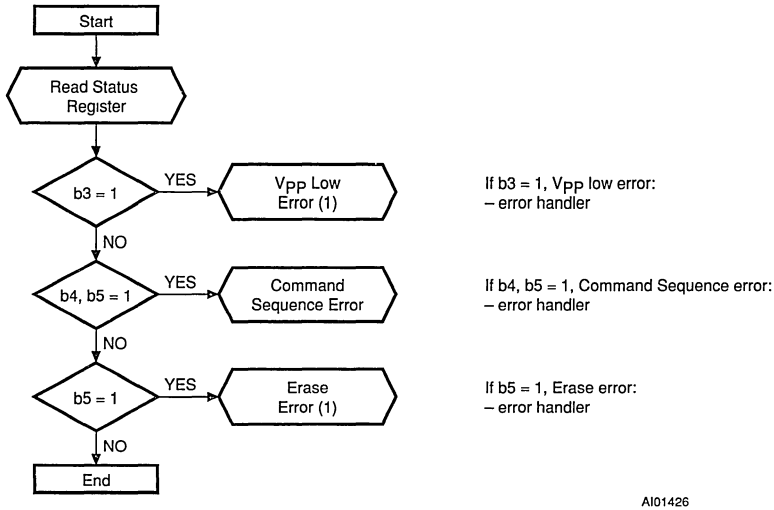
During the execution of the programming the memory accepts only the Read Status Register (RSR) instruction. The Status Register bit b7 returns '0' while programming is in progress and '1' when it is completed. After completion the Status Register bit b4 returns '1' if there has been a program failure. Status Register bit b3 returns a '1' if the Program Supply Voltage V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming.

V_{PP} must be at V_{PPH} when programming. Programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect, the Status Register must be cleared with the Clear Status Register (CLRS) instruction, the sector erased and reprogrammed.

The execution of the programming by the P/E.C. is also indicated by the RY/$\overline{BY}$ output.

A full status check can be made after each byte or after a sequence of bytes has been programmed. The status check is made on the Status Register bit b3 for any possible V_{PP} error and on bit b4 for a programming error.

Figure 12. Erase Status Check Flow-chart and Pseudo Code



Note: 1. If V_{PP} Low or Erase error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Clear Status Register (CLRS) instruction. This instruction uses a single write operation which clears the Status Register bits b3, b4 & b5 to '0'. The CLRS instruction reverts the device to the Read Array mode and is used before any new operation when errors have been detected during programming or erasure.

Erase Suspend (ES) instruction. An Erase operation may be suspended by using this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates wether the P/E.C. is suspended, bit b6 = '1', or whether the P/E.C. cycle was the last and the erase is complete, bit b6 = '0'. During suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Immediately following the ES instruction, read operations initially output the contents of the Status Register while erase is suspended, but if a Read (RD) instruction is given data may be read from other sectors of the memory. The Program Supply Voltage V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or if the $\overline{RP}$ input goes Low, the erase operation is aborted and Status Register bits b3 & b5 are set. In this case the Status Register must be cleared and the erase operation repeated to be certain to erase the sector.

Erase Resume (ER) instruction. If an Erase Suspend instruction has been previously executed, the erase operation may be resumed giving the command 0D0h. The Status Register bit b6 will be cleared when erase resumes. Read operations output the Status Register after the erase is resumed.

Reset. After any error has occurred during programming or erase the Status Register must be cleared by giving the Clear Status Register instruction before the memory array may be read.

After a successful program or erase operation either the Read or Clear Status Register instruction must be given before the memory array may be read.

Figure 13. Erase Suspend & Resume Flow-chart and Pseudo Code

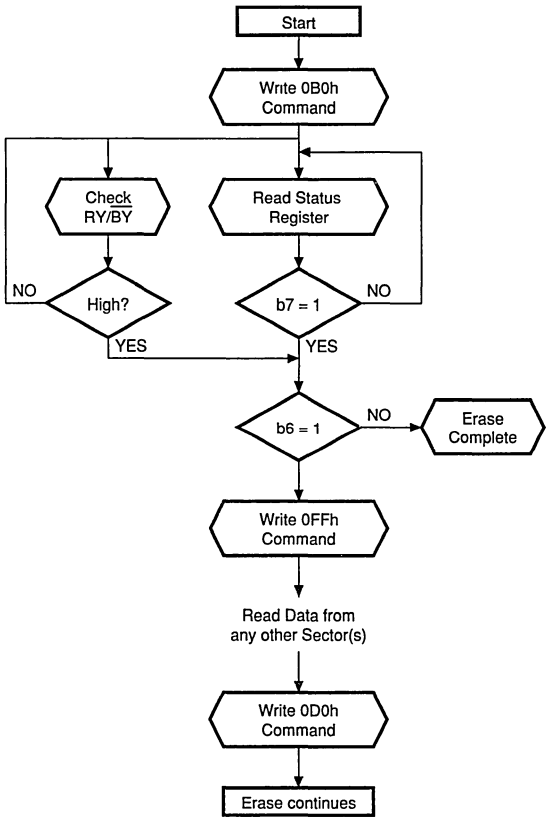
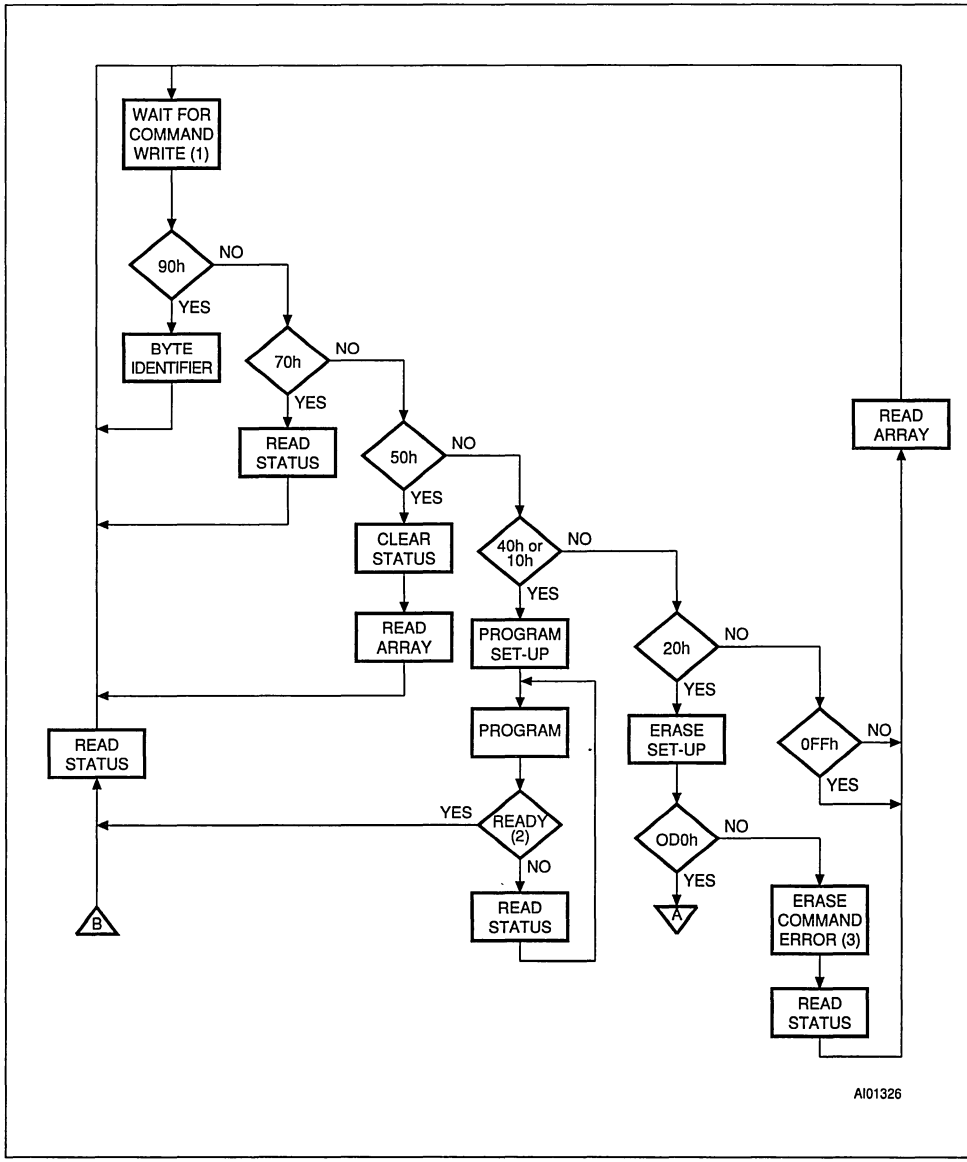
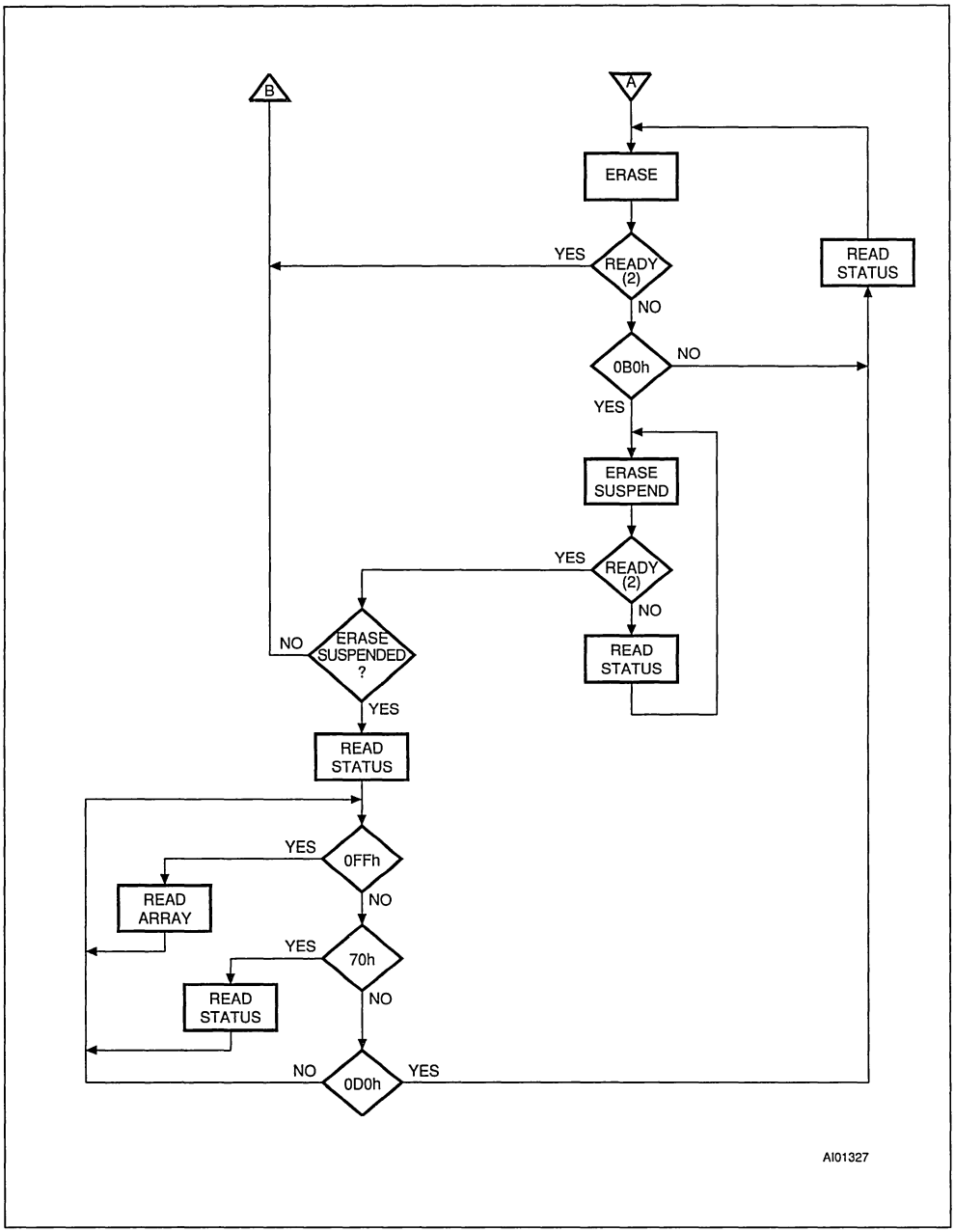


Figure 14. Command Interface and Program Erase Controller Flow-diagram (a)



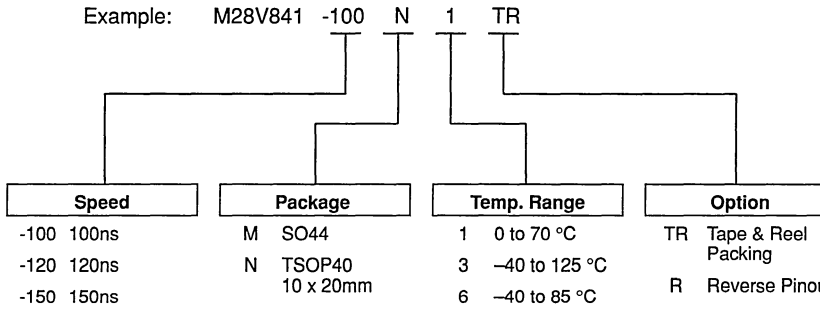
Notes: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.
3. Upon Erase command error, the P/E.C. defaults to Read status and sets bits b4 and b5 of the Status Register. Program and Erase commands will be accepted only after the Status Register has been reset by a CLRS command.

Figure 15. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME



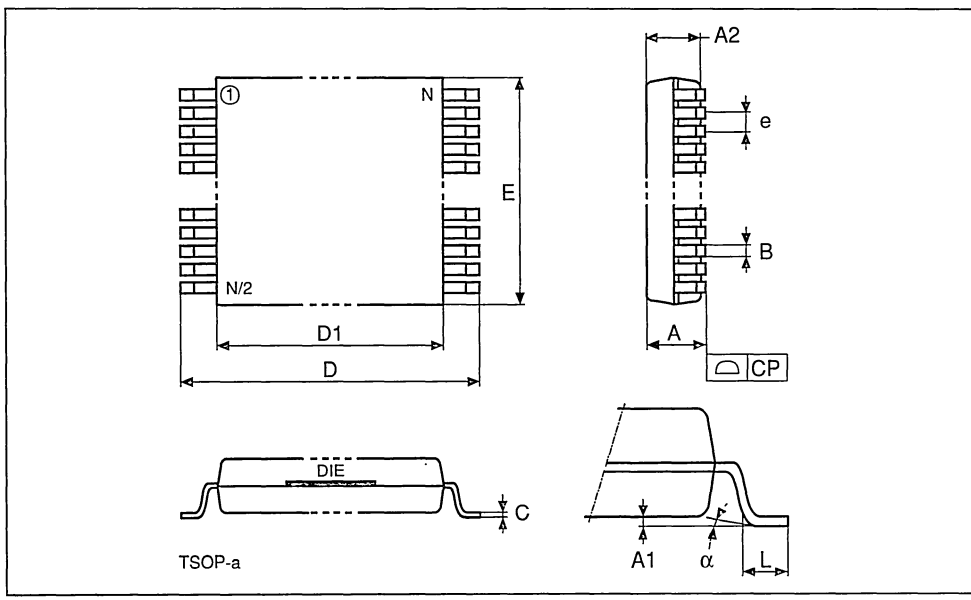
For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP40 Normal Pinout - 40 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	40			40		
CP			0.10			0.004

TSOP40



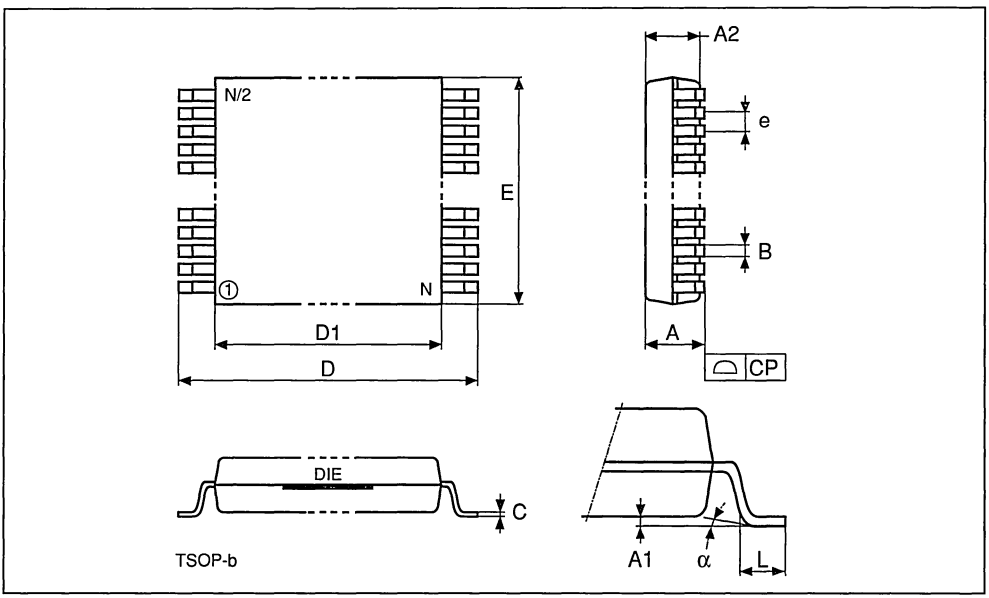
TSOP-a

Drawing is out of scale

TSOP40 Reverse Pinout - 40 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	40			40		
CP			0.10			0.004

TSOP40



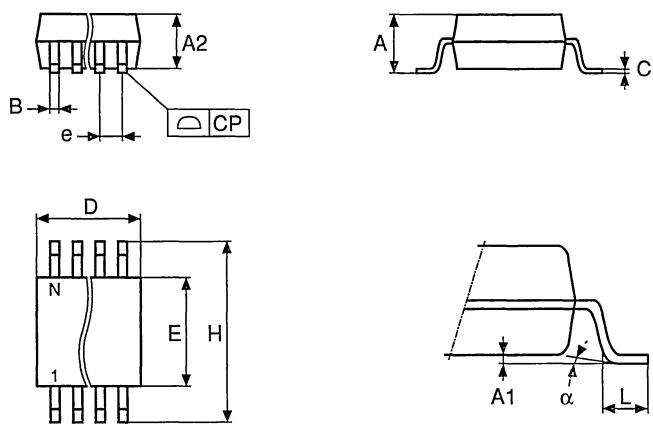
TSOP-b

Drawing is out of scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27	–	–	0.050	–	–
H		15.90	16.10		0.626	0.634
L	0.80	–	–	0.031	–	–
α	3°	–	–	3°	–	–
N		44			44	
CP			0.10			0.004

SO44



SO-b

Drawing is out of scale

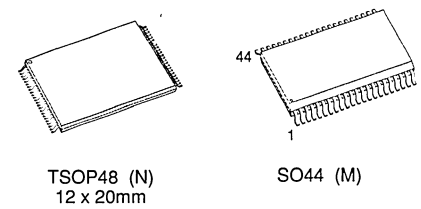
SGS-THOMSON MICROELECTRONICS

M28V161

LOW VOLTAGE 16 Megabit (2 Meg x 8, Sector Erase) FLASH MEMORY

PRODUCT PREVIEW

- SMALL SIZE PLASTIC PACKAGES TSOP48 and SO44
- MEMORY ERASE in SECTORS
  - 32 Sectors of 64K Bytes each
- 3.3V ± 0.3V SUPPLY VOLTAGE
- 12V ± 5% PROGRAMMING VOLTAGE
- 100,000 PROGRAM/ERASE CYCLES per SECTOR
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Erase by Sector, Erase Suspend/Resume Ready/Busy Output
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
- HIGH SPEED ACCESS TIME: 100ns
- EXTENDED TEMPERATURE RANGE
- COMPATIBLE to 8 MEGABIT FLASH MEMORY
  - Equal Software Command Set
  - Pinout Compatible



TSOP48 (N)
12 x 20mm

SO44 (M)

Figure 1. Logic Diagram

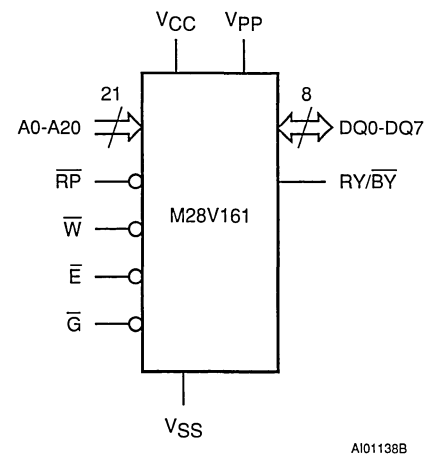
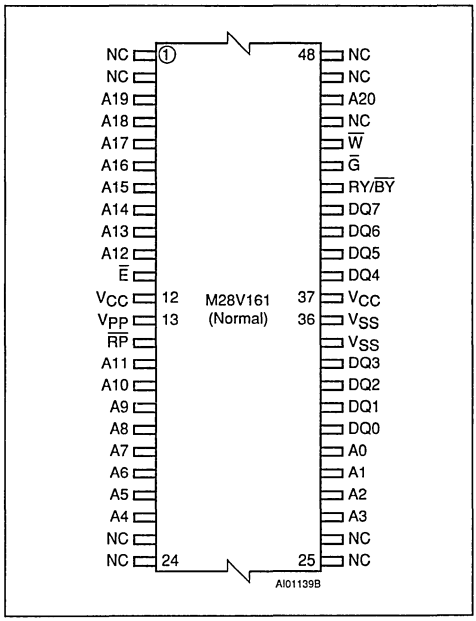


Table 1. Signal Names

A0-A20	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power Down
RY/$\overline{BY}$	Ready/Busy Output
V_{PP}	Program & Erase Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

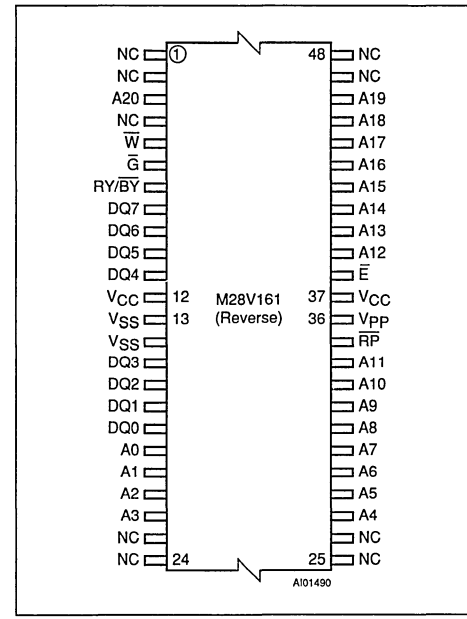
This is preliminary information on a new product now in development. Details are subject to change without notice.

Figure 2A. TSOP Pin Connections



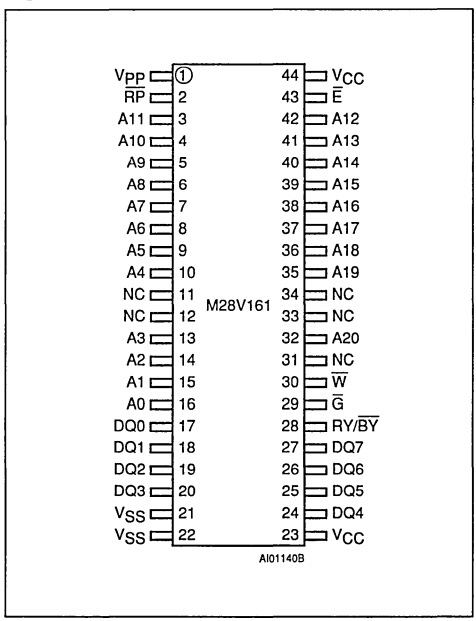
Warning: NC = No Connections

Figure 2B. TSOP Reverse Pin Connections



Warning: NC = No Connections

Figure 2C. SO Pin Connections



Warning: NC = No Connections

DESCRIPTION

The M28V161 FLASH MEMORY product is a non-volatile memory that may be erased electrically at the sector level and programmed byte-by-byte. The interface is directly compatible with most microprocessors. It is intended for computer file systems and mass data storage applications. TSOP48 and S044 packages are used. The M28V161 is software and pin-out, footprint compatible with the M28F841 and M28V841, 8 Megabit FLASH Memory, with the simple addition of an address line.

Organization

The organization is 2 Meg x 8 with Address lines A0-A20 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down input places the memory in deep power down. A Ready/Busy output indicates the status of the internal Program/Erase Controller (P/E.C.).

Sectors

Erasure of the memory is in sectors. There are 32 sectors in the memory address space, each of 64K bytes. Programming of each sector takes typically 0.6 seconds and erasure 1.6 seconds, each sector may be programmed and erased over 100,000 cycles. All sectors are protected from programming

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 5	V
V_{CC}	Supply Voltage		–0.6 to 5	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
I_{OUT} (4)	Output Short Circuit Current		100	mA

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 5V allowed for less than 20ns.
4. Only one output shorted at a time for no longer than 1 second.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	RY/$\overline{BY}$ (2)	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OH}	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{OL} / V_{OH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{OH}	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	V_{OH}	Hi-Z
Power Down	X	X	X	V_{IL}	V_{OH}	Hi-Z

Notes: 1. X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}
2. RY/$\overline{BY}$ = V_{OL} when the P/E.C. is executing a Sector Erase or Write operation. It is at V_{OH} when the P/E.C. is not busy, in the Erase Suspend or Power Down modes.

Table 4. Electronic Signature

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	A0	RY/$\overline{BY}$	DQ0 - DQ7
Manufact. Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{OH}	20h
Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{OH}	58h

DESCRIPTION (cont'd)

or erasure when the Reset/Power Down $\overline{RP}$ signal is Low. Sector erase may be suspended while data is read from other sectors of the memory, then resumed.

Bus operations

Five operations can be performed by the appropriate bus cycles, Read a Byte from the Array, Output Disable, Standby, Power Down and Write a Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor then memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address (1)	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data Output
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register Output
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Code Input
EE	Erase	2	Write	X	20h	Write	Sector Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSR or RSIG instruction is followed by read operations to Read Memory Array, Read Status Register or Read Electronic Signature codes. Any number or read cycles may be performed after an RD, RSR or RSIG instructions.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Memory Array / Reset

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the Array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and sector erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte programming takes typically 9µs, sector erase typically 1.6 seconds. Erasure of a memory sector may be suspended in order to read data from another sector and then resumed.

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	The RY/$\overline{BY}$ output or the P/E.C. status bit may be checked during Program or Erase. The bit should be checked on completion before checking bits b4 or b5 for success.
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction the ESS bit is set to '1' and the P/ECS bit remains at '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In Progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte or word.
			'0'	Program Success	If PS and ES bits are set to '1' during a sector erase attempt, an improper command sequence was entered and the instruction should be given again.
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction is executed and the instruction is aborted. The Status Register must be cleared before another write or erase operation is attempted.
			'0'	V_{PP} OK	
	2	Reserved			Bits b2, b1 and b0 are reserved for future use and should be masked out when polling the Status Register.
	1	Reserved			
	0	Reserved			

Note: Logic level '1' is High, '0' is Low.

A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. In addition a Ready/Busy output RY/$\overline{BY}$ indicates the status of the P/E.C. After Programming or Erasure the command interface must be reset by giving the Read Memory Array instruction before the memory contents can be accessed.

Power Saving

The M28V161 memory have a number of power saving features. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down $\overline{RP}$ signals are at V_{CC}, when the supply current drops to typically 30µA. A deep power down mode is enabled when the Reset/Power Down signal $\overline{RP}$ is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 1µs maximum, with instructions to the C.I. recognized after 400ns.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

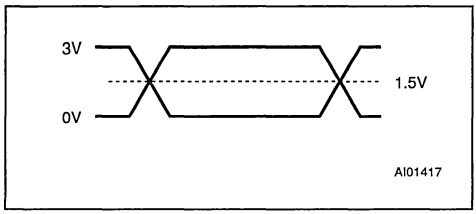


Figure 4. AC Testing Load Circuit

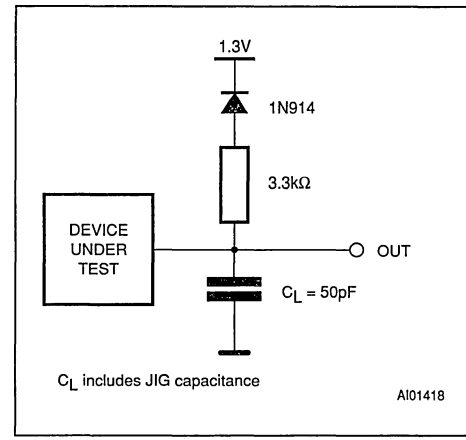


Table 8. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

DEVICE OPERATION

Signal Descriptions

A0-A20 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte to be programmed or a command to the C.I., are latched on the rising edge of Chip Enable $\overline{E}$ and Write Enable $\overline{W}$, whichever occurs first. The data output from the memory Array, the Electronic Signature or the Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the C.I. and the memory Array while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This input allows the memory to be placed in a deep power down mode. If $\overline{RP}$ is within V_{SS} ± 0.2V the lowest supply current is absorbed.

RY/$\overline{BY}$ Read/Busy. This output indicates when the Program Erase Controller is executing a program or erase. It is always active, even during power down. If RY/$\overline{BY}$ is at V_{OL}, the P/E.C. is active.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. This controls writing to the C.I., Address and Input Data latches. Both Addresses and Input Data are latched on the rising edge of $\overline{W}$.

V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{CC} Supply Voltage. This is the main circuit supply.

V_{SS} Ground. This is the reference for all the voltage measurements.

Table 9. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 8MHz		30	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, $\overline{G} = V_{SS}$, f = 8MHz		20	mA
I_{CC1} (1, 3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1, 3)	Supply Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{CC3} (1, 3)	Supply Current (Program)	Byte program in progress		30	mA
I_{CC4} (1, 3)	Supply Current (Erase)	Sector Erase in progress		30	mA
I_{CC5} (1, 2, 3)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		6	mA
I_{PP}	Program Current (Read)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Standby)	$V_{PP} \le V_{CC}$		±10	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Byte program in progress		15	mA
I_{PP4}	Program Current (Erase)	Sector Erase in progress		10	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –2mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	V_{CC} + 0.3	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{LKO}	Supply Voltage (Program or Erase Lock-out)		2		V

Notes: 1. Supply Current specified with I_{OUT} ($RY/\overline{BY}$) = 0.
2. Current increases to $I_{CC} + I_{CC5}$ during a read operation with erase suspended.
3. CMOS levels $V_{CC} \pm 0.2V$ and $V_{SS} \pm 0.2V$. TTL levels V_{IH} and V_{IL}.

Memory Sectors

There are 32, 64K Byte memory sectors. Each sector of the memory can be erased separately, but only one sector at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another sector and then resumed.

Programming and erasure of the memory is disabled when the Program Supply Voltage is at V_{PPL}. For successful programming and erasure the Program Supply Voltage must be at V_{PPH} throughout the operation.

Table 10. Read AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	Test Condition	M28V161						Unit
				-100		-120		-150		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		1		1		1	µs
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		50		50	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		50		50		55	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		40		50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be Low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. A read operation will output a byte on DQ0-DQ7.

The data read depends on the previous command written to the C.I. (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$. As for read operations data is transferred on DQ0-DQ7.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Figure 5. Read Mode AC Waveforms

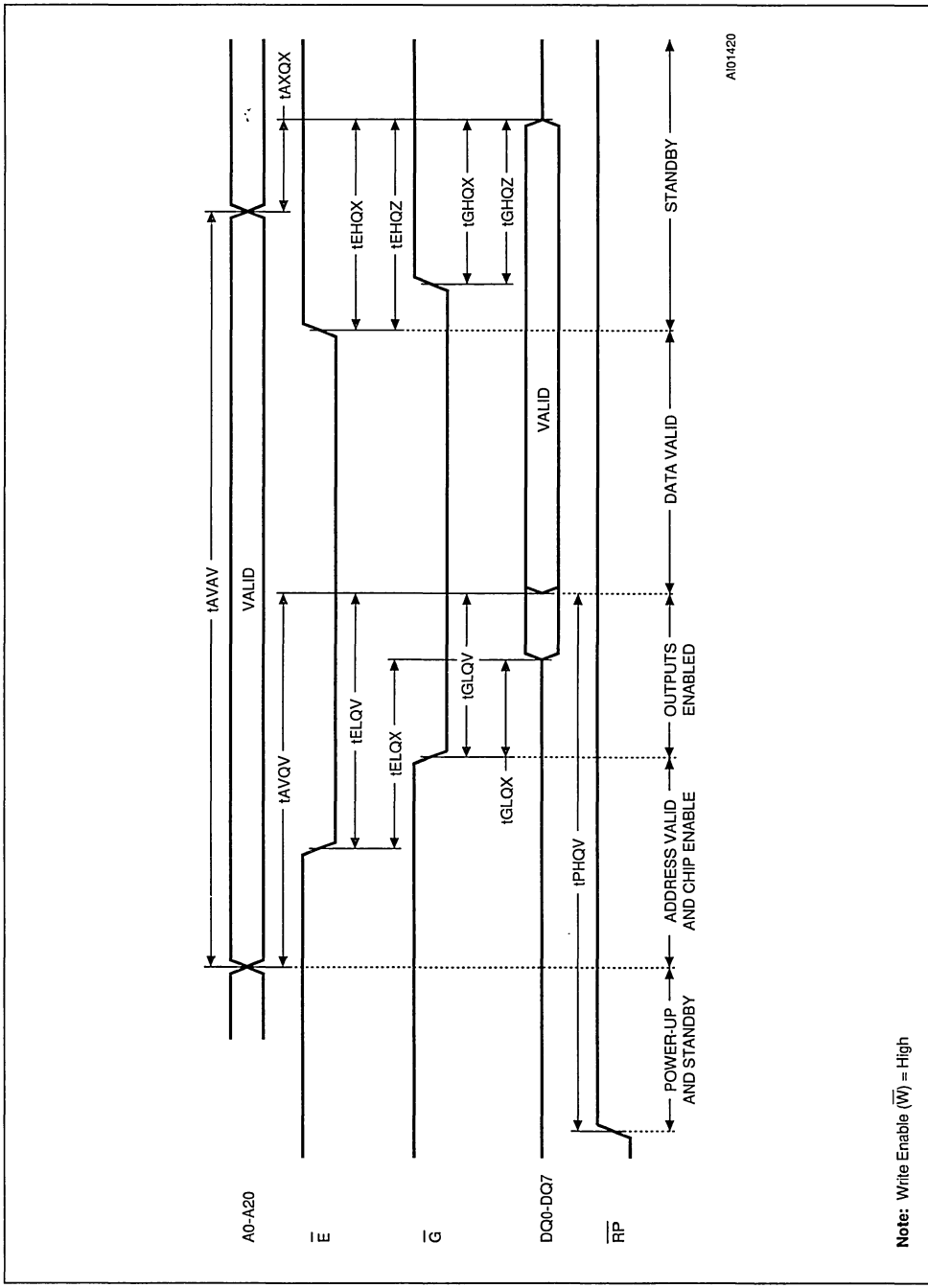


Table 11. Byte Program, Erase Time
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 3.3V ± 0.3V)

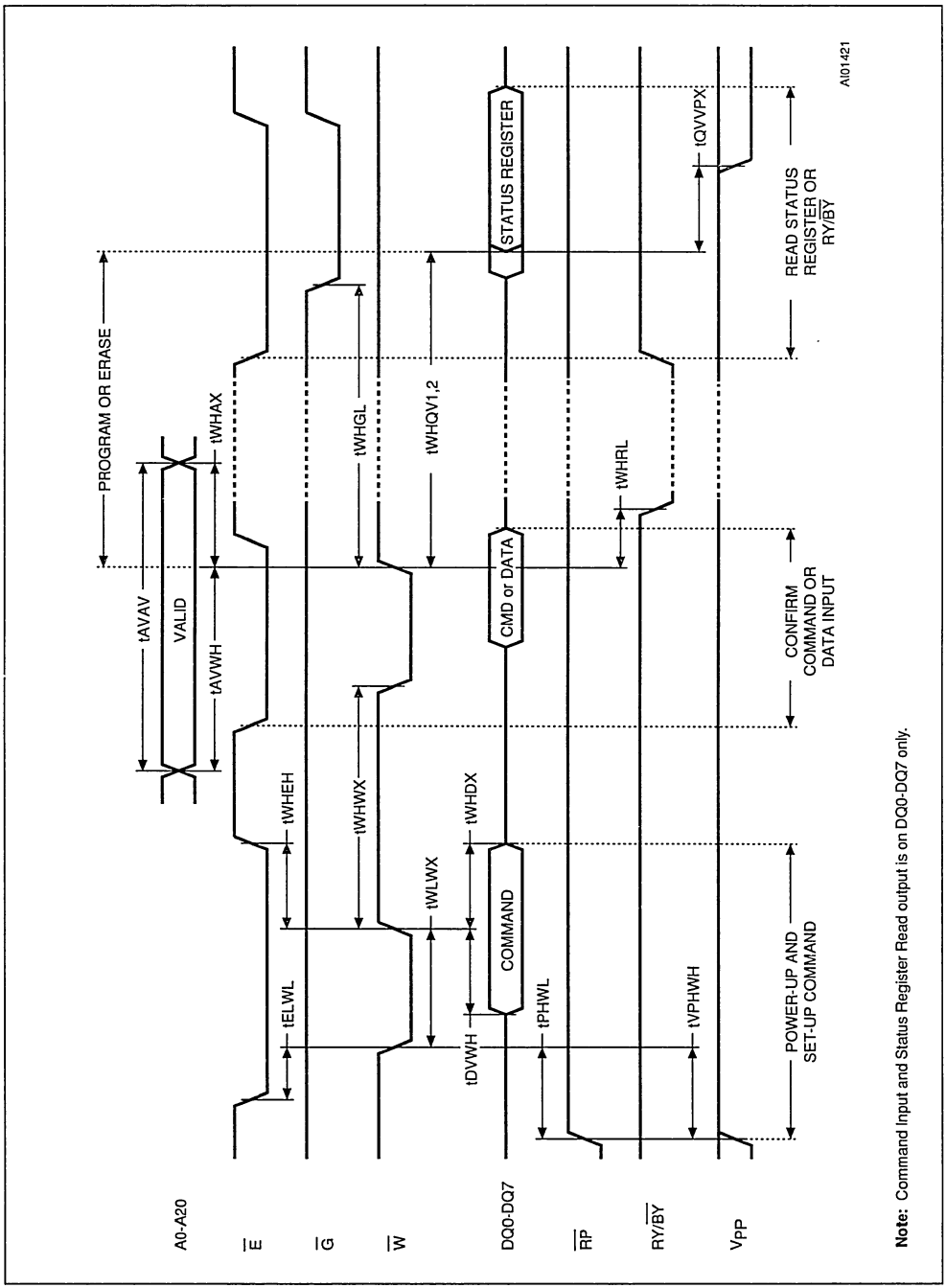
Parameter	Test Conditions	M28V161			Unit
		Min	Typ	Max	
Sector Program	V_{PP} = 12V ± 5%		0.6	2.1	sec
Sector Erase	V_{PP} = 12V ± 5%		1.6	10	sec

Table 12. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28V161						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHWL} (1)	t_{PS}	Power Down High to Write Enable Low	1		1		1		µs
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWX}	t_{WP}	Write Enable Low to Write Enable Transition	40		40		40		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	40		40		40		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	5		5		5		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		10		ns
t_{WHWX}	t_{WPH}	Write Enable High to Write Enable Transition	30		30		30		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	40		40		40		ns
t_{VPHWH} (1)	t_{VPS}	V_{PP} High to Write Enable High	100		100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	5		5		5		ns
t_{WHGL}		Write Enable High to Output Enable Low	0		0		0		ns
t_{WHRL}		Write Enable High to Ready Busy Low		100		100		100	ns
t_{WHQV1} (2)		Write Enable High to Output Valid (Byte Program)	6		6		6		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Sector Erase)	0.3		0.3		0.3		sec
t_{QVVPX} (1, 2)	t_{VPH}	Output Valid or Ready Busy High to V_{PP} Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. Byte Program and Sector Erase durations are measured to completion as indicated by Status Register b7 = 1 or RY/$\overline{BY}$ = high. V_{PP} is held high until Status Register bits b3, b4 and b5 indicate Program or Sector Erase success.
3. Temperature range 0 to 70 °C (grade 1) only.

Figure 6. Program & Erase AC Waveforms, $\overline{W}$ Controlled



Note: Command Input and Status Register Read output is on DQ0-DQ7 only.

Table 13. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{CC} = 3.3V ± 0.3V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28V161						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHEL} (1)	t_{PS}	Power Down High to Chip Enable Low	1		1		1		µs
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEX}	t_{CP}	Chip Enable Low to Chip Enable Transition	50		50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	40		40		40		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	5		5		5		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	5		5		5		ns
t_{EHEX}	t_{EPH}	Chip Enable High to Chip Enable Transition	25		25		25		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	40		40		40		ns
t_{VPHEH} (1)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	5		5		5		ns
t_{EHGL}		Chip Enable High to Output Enable Low	0		0		0		ns
t_{EHRL}		Chip Enable High to Ready Busy Low		100		100		100	ns
t_{EHQV1} (2)		Chip Enable High to Output Valid (Byte Program)	6		6		6		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Sector Erase)	0.3		0.3		0.3		sec
t_{QVVPX} (1, 2)	t_{VPH}	Output Valid or Ready Busy High to V_{PP} Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. Byte Program and Sector Erase durations are measured to completion as indicated by Status Register b7 = 1 or RY/$\overline{BY}$ = high. V_{PP} is held high until Status Register bits b3, b4 and b5 indicate Program or Sector Erase success.
3. Temperature range 0 to 70 °C (grade 1) only.

Figure 7. Program & Erase AC Waveforms, $\overline{E}$ Controlled

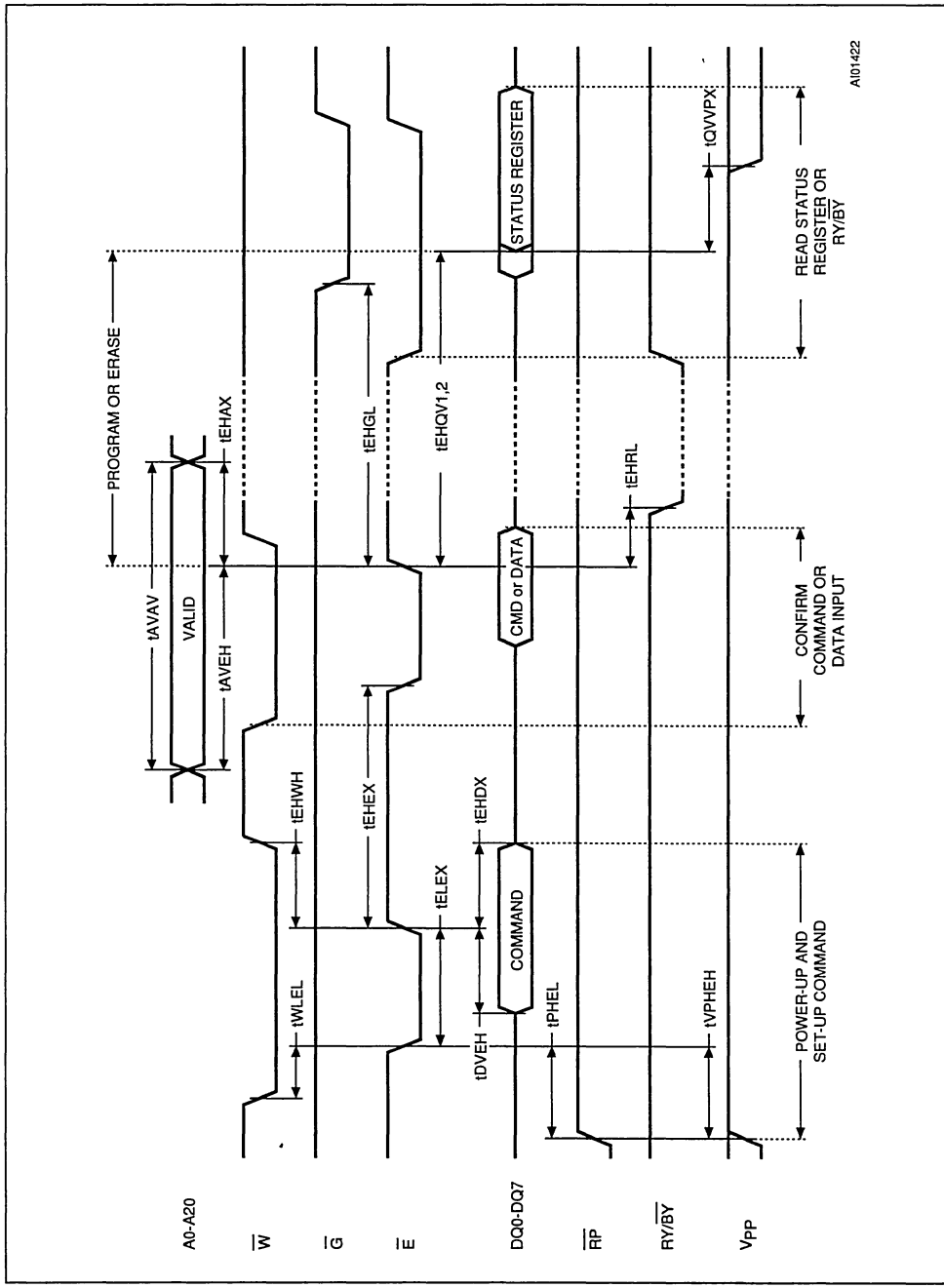


Figure 8. Memory Map, Byte-wide Addresses

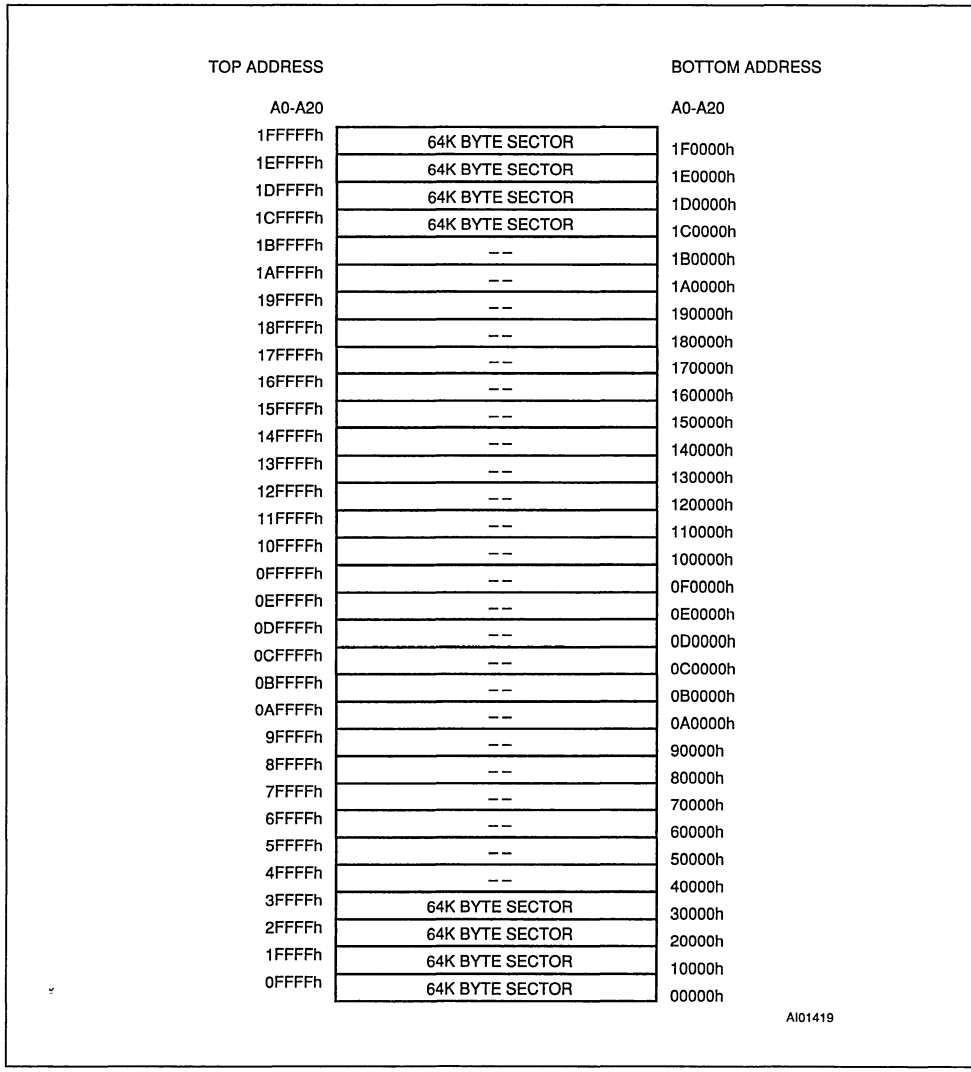
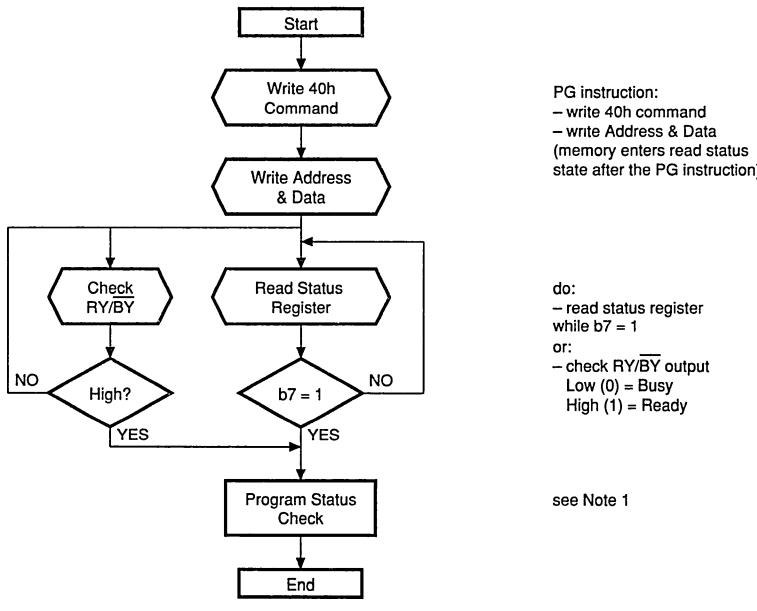


Figure 9. Program Flow-chart and Pseudo Code



Note: 1. Status check of b7 can be made after each byte programming or after a sequence.

Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is Low. The power consumption is reduced to the power down level and the outputs are high impedance independent of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory, the manufacturer code for SGS-THOMSON is 20h and the device code for the M28V161 is 58h. These codes allow applications to match their interfaces to the characteristics of the particular manufacturer's product.

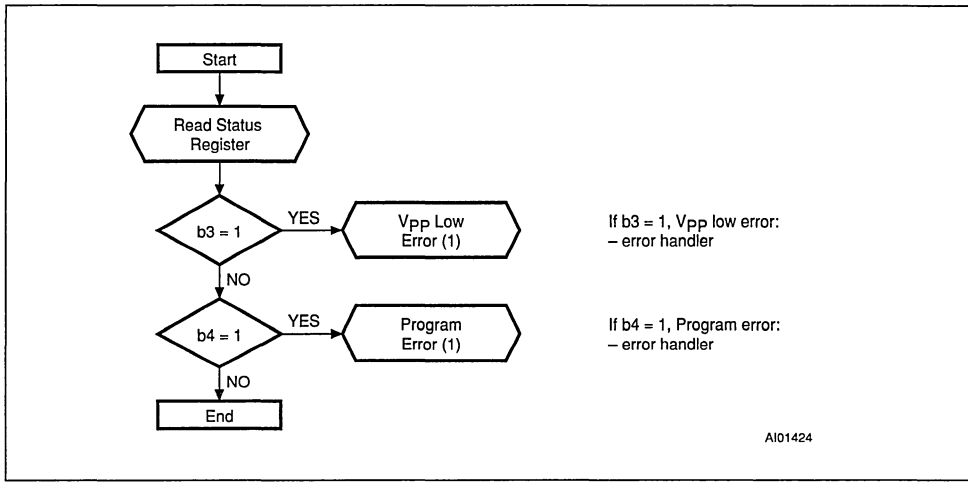
The two Electronic Signature codes are output by a read operations with the Address line A0 at V_{IL} or V_{IH}, following an instruction RSIG to the memory.

Instructions and Commands

The memory includes a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from one to 3 operations, the first of which is always a write operation followed by either a further write operation to input address and data or to confirm the command, or a read operation to output data.

A Status Register indicates the P/E.C. status Ready/Busy, the suspend/in-progress status of

Figure 10. Program Status Check Flow-chart and Pseudo Code



Note: 1. If a V_{PP} Low or Program error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

DEVICE OPERATION (cont'd)

erase operations, the failure/success of erase and program operations and the low/correct value of the V_{PP} Program Supply Voltage.

The P/E.C. sets status bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The status register can be read by the Read Status Register RSR instruction and cleared by the Clear Status Register CLRS instruction. The meaning of the register bits b3 to b7 is shown in Table 7. Bit b0 to b2 are reserved for future use and should be masked out during status checks.

The P/E.C. Ready/Busy status is also indicated by the RY/$\overline{BY}$ output.

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read data from the addressed byte of the memory array, until a new command is written to the C.I.

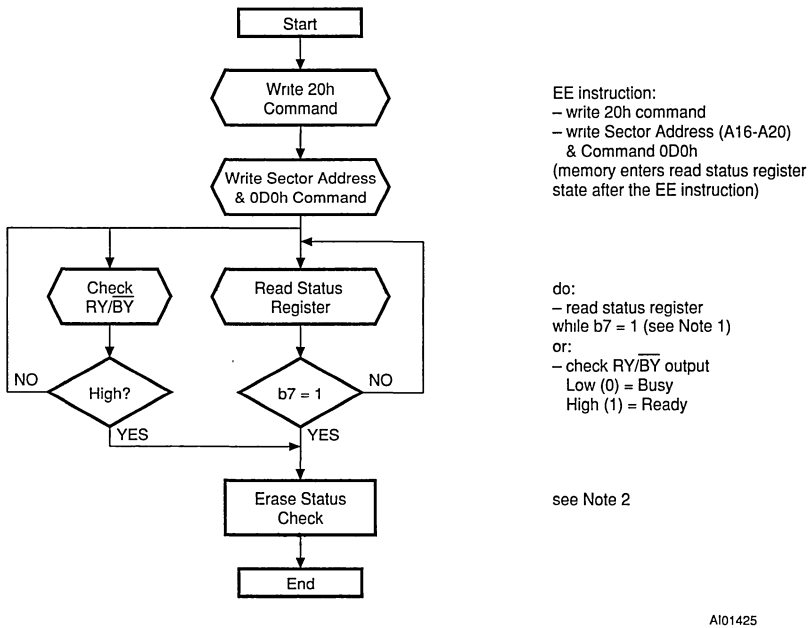
Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent read operations output the contents of the status register. The contents are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the status register.

Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h, followed by two read operations to output the manufacturer and device codes. The manufacturer code is output when the address line A0 is Low and the device code when A0 is High.

Erase (EE) instruction. The memory can be erased in sectors. The Program Supply Voltage V_{PPH} must be applied before the Erase (EE) instruction is given. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second is the Erase Confirm command 0D0h. During the input of the second command an address within the sector to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 & b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the Read Status Register (RSR) or Erase Suspend (ES) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it is completed. After completion the Status Register bit b5 returns '1' if there has been an erase failure because erasure has not been verified after even the maximum number of erase pulses have been given. The Status Register bit b3 returns '1' if the Program Supply Voltage V_{PP} does not remain at V_{PPH} when erasure is attempted and/or proceeding.

Figure 11. Erase Flow-chart and Pseudo Code



Notes: 1. An Erase Suspend may be executed during this loop.
2. See separate flow-chart.

V_{PP} must be at V_{PPH} when erasing. Erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or if $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register with the CLRS instruction.

The execution of the erase by the P/E.C. is also indicated by the RY/$\overline{BY}$ output.

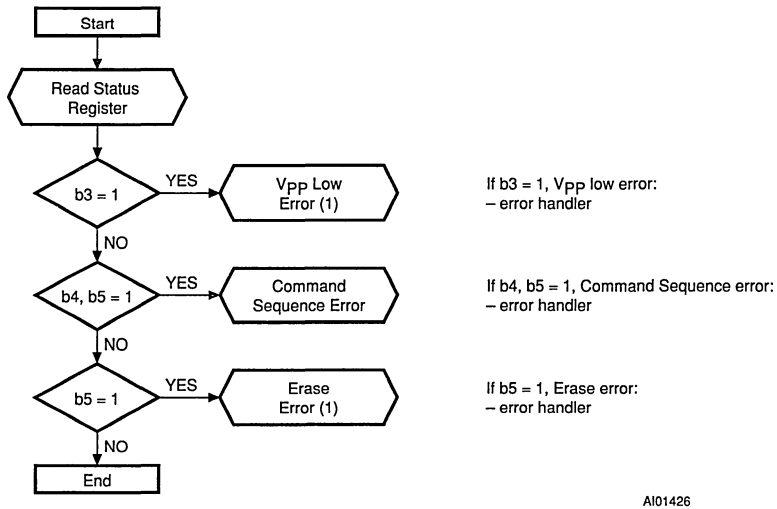
A full status check can be made after sector erase. The status check is made on the Status Register bit b3 for any possible V_{PP} error, on bit b5 for an erase error or on both bits b4 & b5 for a command sequence error.

Program (PG) instruction. The memory is programmed byte-by-byte. The Program Supply Voltage V_{PPH} must be applied before the Program (PG) instruction is given and may be applied continuously during programming of a sequence of bytes. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or alternatively 10h). A second write operation latches the address and input data and starts the P/E.C. execution. Read operations output the Status Register after programming has started.

Memory programming is only made by writing a '0' in place of a '1' in a byte. To write a '1' in place of a '0' the Sector must first be erased to all '1's.

During the execution of the programming the memory accepts only the Read Status Register (RSR) instruction. The Status Register bit b7 returns '0' while programming is in progress and '1' when it is completed. After completion the Status Register bit b4 returns '1' if there has been a program failure. Status Register bit b3 returns a '1' if the Program Supply Voltage V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming.

Figure 12. Erase Status Check Flow-chart and Pseudo Code



Note: 1. If V_{PP} Low or Erase error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

DEVICE OPERATION (cont'd)

V_{PP} must be at V_{PPH} when programming. Programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect, the Status Register must be cleared with the Clear Status Register (CLRS) instruction, the sector erased and reprogrammed.

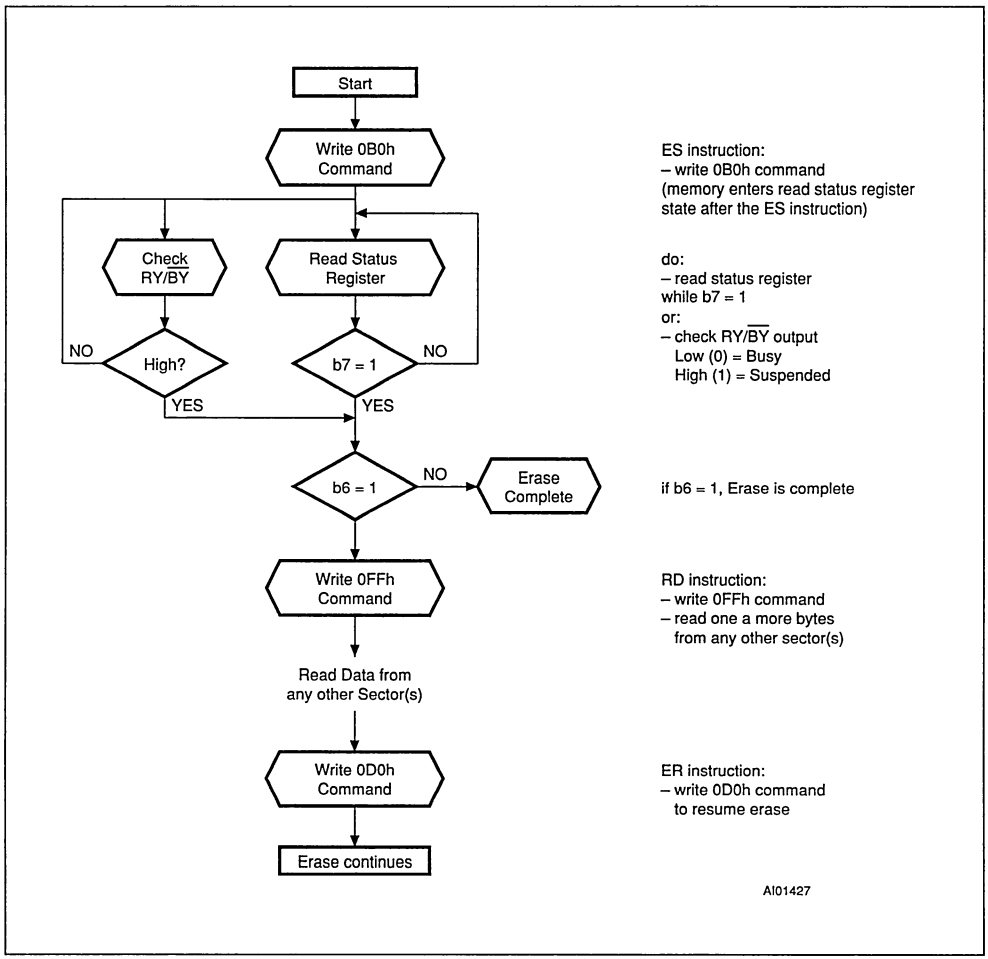
The execution of the programming by the P/E.C. is also indicated by the RY/$\overline{BY}$ output.

A full status check can be made after each byte or after a sequence of bytes has been programmed. The status check is made on the Status Register bit b3 for any possible V_{PP} error and on bit b4 for a programming error.

Clear Status Register (CLRS) instruction. This instruction uses a single write operation which clears the Status Register bits b3, b4 & b5 to '0'. The CLRS instruction reverts the device to the Read Array mode and is used before any new operation when errors have been detected during programming or erasure.

Erase Suspend (ES) instruction. An Erase operation may be suspended by using this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates wether the P/E.C. is suspended, bit b6 = '1', or whether the P/E.C. cycle was the last and the erase is complete, bit b6 = '0'. During suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Immediately following the ES instruction, read operations initially output the contents of the Status Register while erase is suspended, but if a Read (RD) instruction is given data may be read from other sectors of the memory. The Program Supply Voltage V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or if the $\overline{RP}$ input goes Low, the erase operation is aborted and Status Register bits b3 & b5 are set. In this case the Status Register must be cleared and the erase operation repeated to be certain to erase the sector.

Figure 13. Erase Suspend & Resume Flow-chart and Pseudo Code

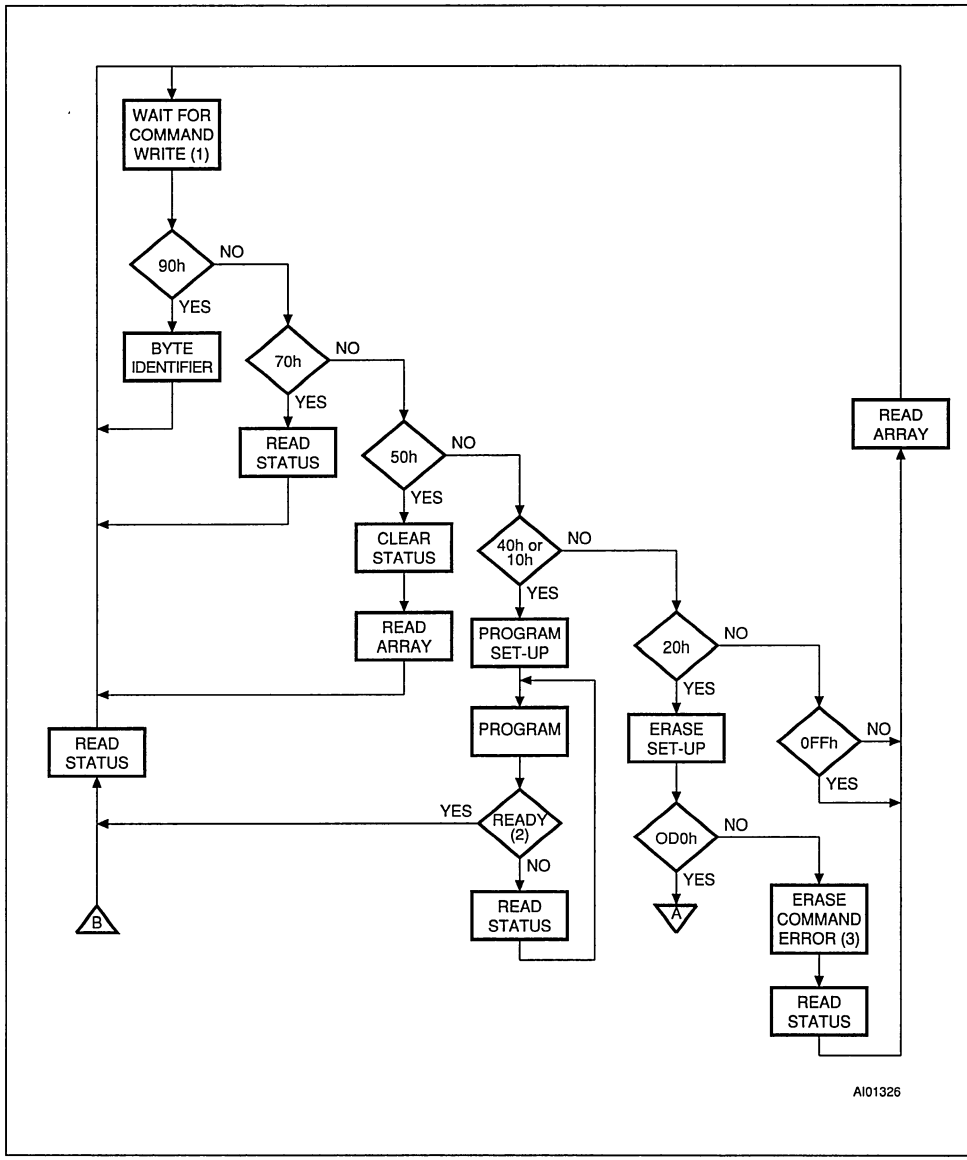


Erase Resume (ER) instruction. If an Erase Suspend instruction has been previously executed, the erase operation may be resumed giving the command 0D0h. The Status Register bit b6 will be cleared when erase resumes. Read operations output the Status Register after the erase is resumed.

Reset. After any error has occurred during programming or erase the Status Register must be cleared by giving the Clear Status Register instruction before the memory array may be read.

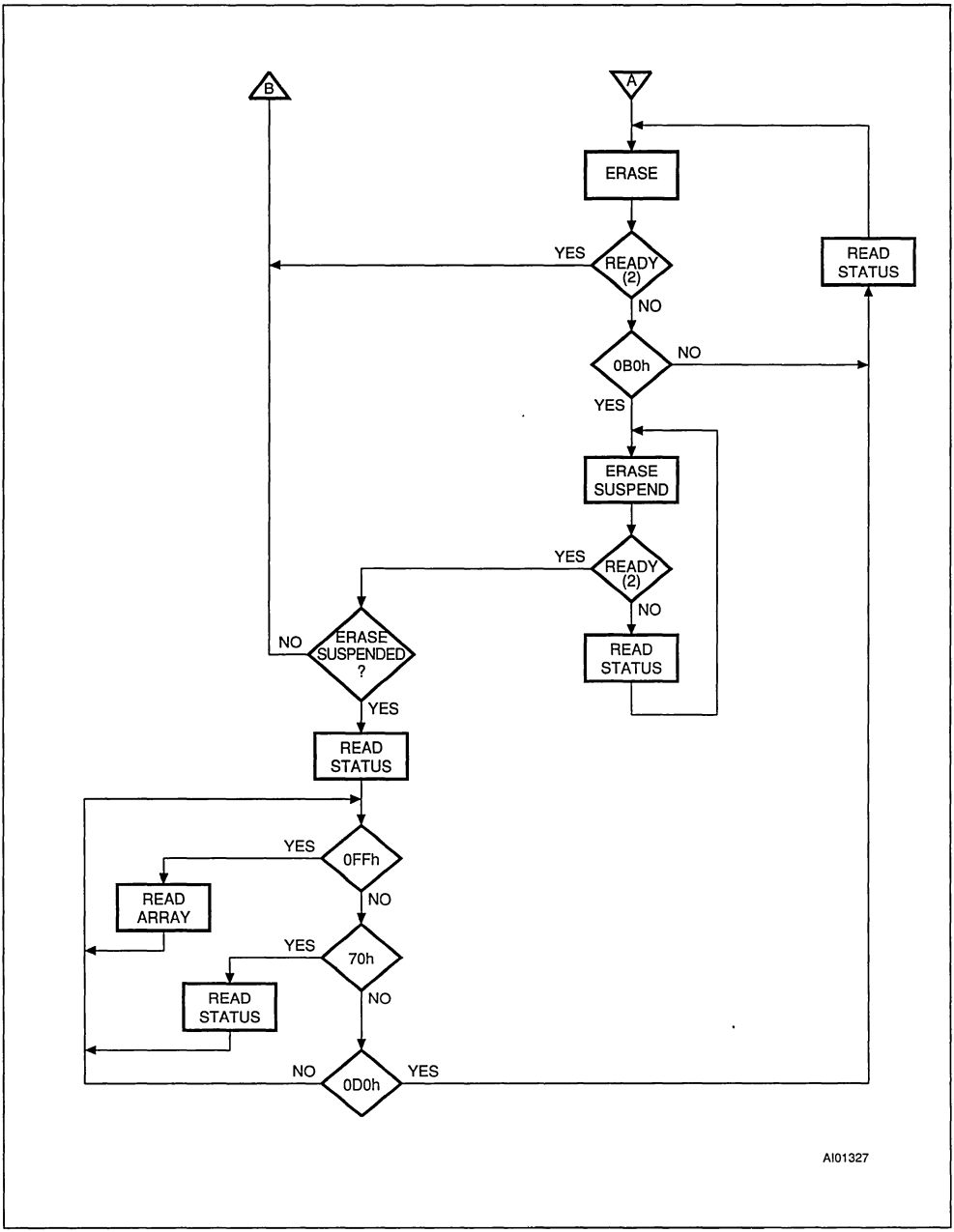
After a successful program or erase operation either the Read or Clear Status Register instruction must be given before the memory array may be read.

Figure 14. Command Interface and Program Erase Controller Flow-diagram (a)



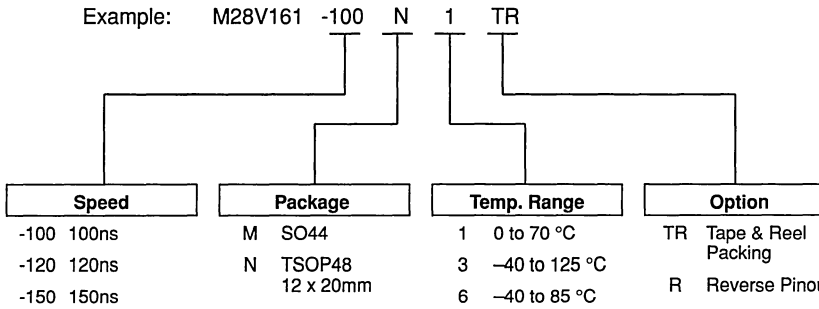
Notes: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.
3. Upon Erase command error, the P/E.C. defaults to Read status and sets bits b4 and b5 of the Status Register. Program and Erase commands will be accepted only after the Status Register has been reset by a CLRS command.

Figure 15. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME



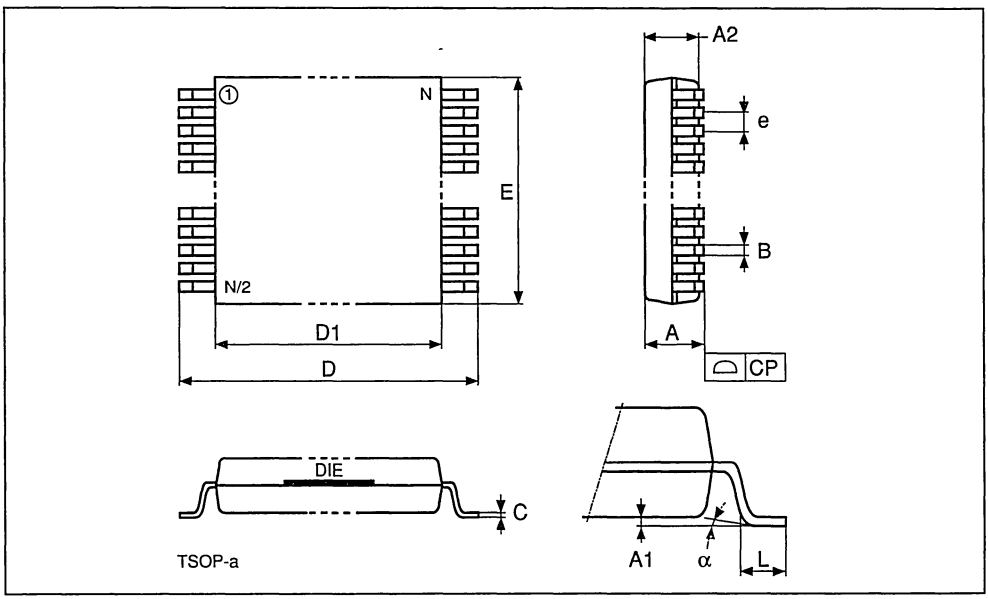
For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP48 Normal Pinout - 48 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		11.90	12.10		0.469	0.476
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		48			48	
CP			0.10			0.004

TSOP48



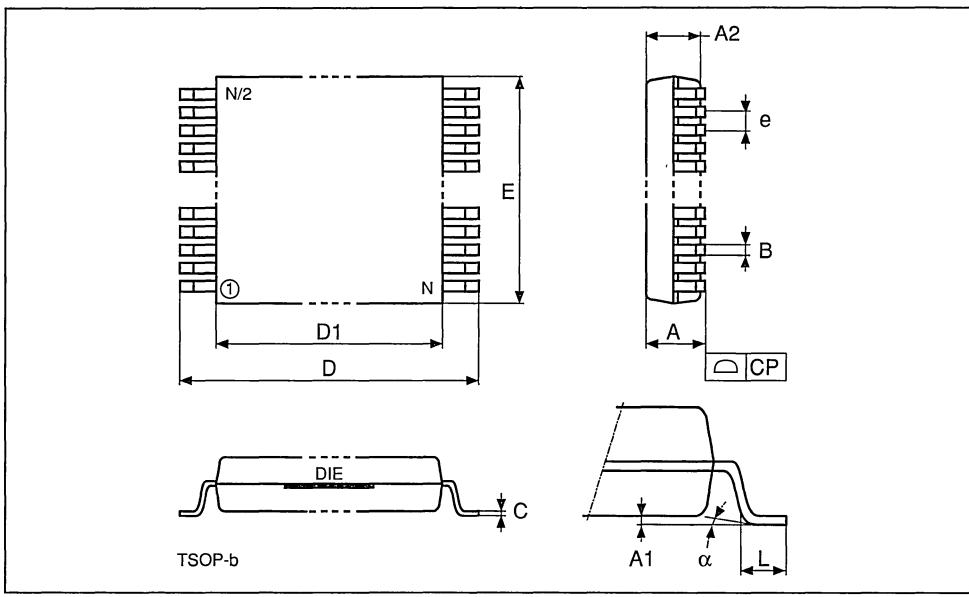
TSOP-a

Drawing is out of scale

TSOP48 Reverse Pinout - 48 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		11.90	12.10		0.469	0.476
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.004

TSOP48



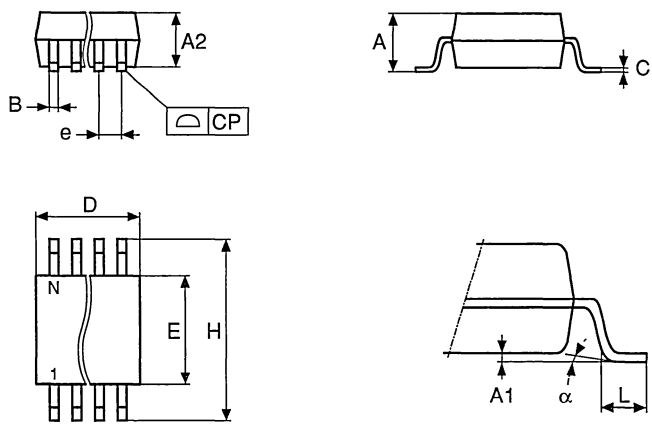
TSOP-b

Drawing is out of scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27	–	–	0.050	–	–
H		15.90	16.10		0.626	0.634
L	0.80	–	–	0.031	–	–
α	3°	–	–	3°	–	–
N	44			44		
CP			0.10			0.004

SO44



SO-b

Drawing is out of scale

SINGLE VOLTAGE FLASH MEMORY

SGS-THOMSON MICROELECTRONICS

M29F040

SINGLE SUPPLY 4 Megabit (512K x 8, Sector Erase) FLASH MEMORY

PRODUCT PREVIEW

- VERY FAST ACCESS TIME: 70ns
- 5V ± 10% SUPPLY VOLTAGE for PROGRAM and ERASE OPERATIONS
- 5V ± 10% SUPPLY VOLTAGE in READ OPERATIONS
- 10µs TYPICAL PROGRAMMING TIME
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Data Polling and Toggle Protocol for P/E.C. Status
- MEMORY ERASE in SECTORS
  - 8 Sectors of 64K Bytes each
  - Sector Protection
  - Multisector Erase
- ERASE SUSPEND and RESUME
- 100,000 PROGRAM/ERASE CYCLES per SECTOR
- LOW POWER CONSUMPTION
  - 25µA Typical in Standby
- STANDARD EPROM/OTP MEMORY PACKAGES: TSOP32, PLCC32 and PDIP32
- EXTENDED TEMPERATURE RANGES

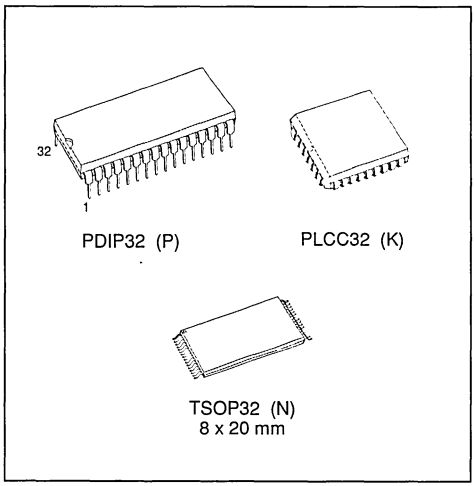


Figure 1. Logic Diagram

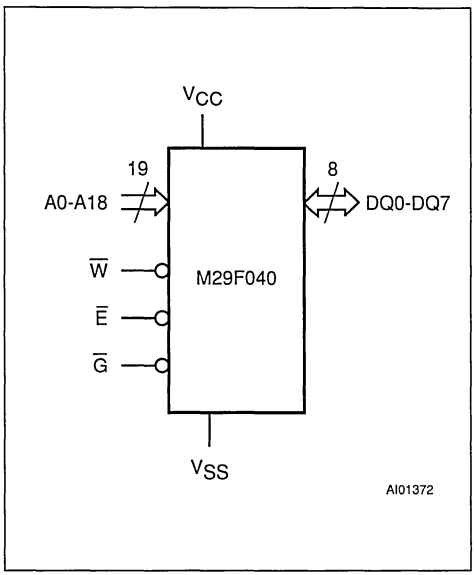


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

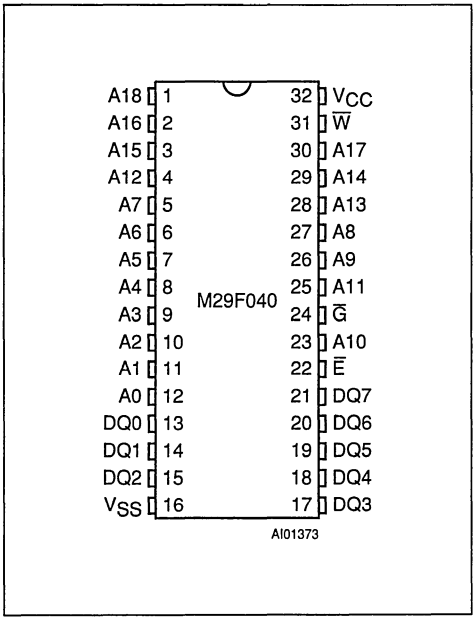


Figure 2B. LCC Pin Connections

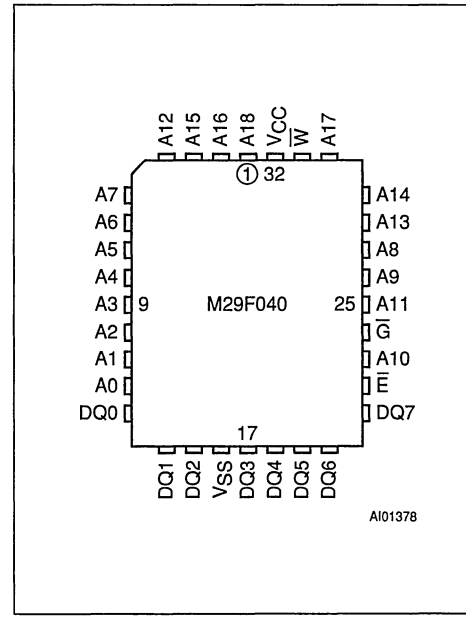
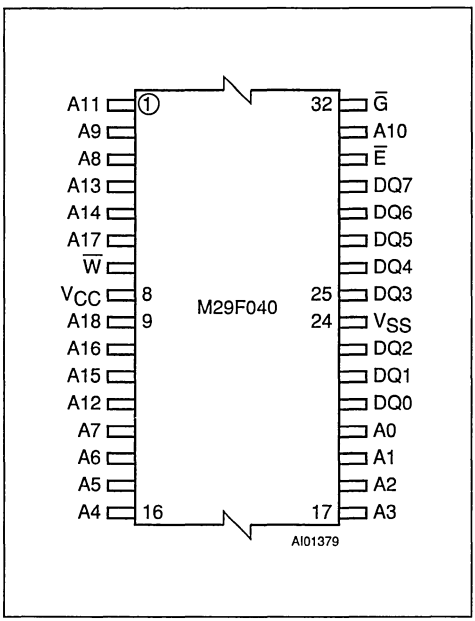


Figure 2C. TSOP Pin Connections



DESCRIPTION

The M29F040 is a non-volatile memory that may be erased electrically at the sector level, and programmed Byte-by-Byte.

The interface is directly compatible with most microprocessors. PDIP32, PLCC32 and TSOP32 (8 x 20mm) packages are used. Both normal and reverse pin outs are available for the TSOP32 package.

Organisation

The Organisation is 512K x 8 bits with Address lines A0-A18 and Data Inputs/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable Inputs.

Erase and Program are performed through the internal Program/Erase Controller (P/E.C.).

Data Outputs bits DQ7 and DQ6 provide polling or toggle signals during Automatic Program or Erase to indicate the Ready/Busy state of the internal Program/Erase Controller.

Sectors

Erasure of the memory is in sectors. There are 8 sectors of 64K bytes each in the memory address space. Erasure of each sector takes typically 1.5 seconds and each sector can be programmed and

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2)	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9} (2)	A9 Voltage		–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	Hi-Z

Note: X = V_{IL} or V_{IH}

Table 4. Electronic Signature

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	Other Addresses	DQ0 - DQ7
Manufact. Code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h
Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	0E2h

Table 5. Sector Protection Status

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A16	A17	A18	Other Addresses	DQ0 - DQ7
Protected Sector	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	SA	SA	SA	Don't Care	01h
Unprotected Sector	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	SA	SA	SA	Don't Care	00h

Note: SA = Address of sector being checked

Table 6A. Instructions

Mne.	Instr.	Cyc.	1st Cycle			2nd Cycle			3rd Cycle			4th Cycle		
			Op.	Addr. (1,5)	Data	Op.	Addr. (1,5)	Data	Op.	Addr. (1,5)	Data	Op.	Addr. (1)	Data
RD	Read/ Reset Memory Array	1+	Write	X	0F0h	Read	Read Address	Data	Read	Read Address	Data	Read	Read Address	Data
RD	Read Memory Array	3+	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	0F0h	Read	Read Address	Data
RSIG	Read Electronic Signature	3+	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	90h	Read (2,3)	Signature Address	Signature
RSP	Read Sector Protection	3+	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	90h	Read (2,4)	Protection Address	Protect Status (6)
PG	Program	4	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	0A0h	Write	Address	Data Input
SE	Sector Erase	6	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	80h	Write	x5555h (4)	0AAh
BE	Bulk Erase	6	Write	x5555h	0AAh	Write	x2AAAh	55h	Write	x5555h	80h	Write	x5555h (4)	0AAh
ES	Erase Suspend	1	Write	X	0B0h	Read until Toggle stops, then read all the data needed from any sector(s) not being erased then Resume Erase								
ER	Erase Resume	1	Write	X	30h	Read Data Polling or Toggle Bit until Erase completes or Erase is suspended another time								

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSP or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes Any number of read cycles can occur after one command cycle
3 Signature Address bits A0, A1, A6 at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1, A6 at V_{IL} will output Device code (0E2h)
4. Protection Address· A0, A6 at V_{IL} and A1 at V_{IH}, other addresses within the sector to be checked A16, A17, A18 define this Sector Address
5. Address bits A16, A17, A18 are don't care for coded address inputs
6 Optional, additional sectors addresses must be entered within a 80µs delay after last write entry, timeout status can be verified through DQ3 value When full command is entered, read Data Polling or Toggle bit until Erase is completed

Table 6B. Instructions

Mne.	Instr.	Cyc.	5th Cycle			6th Cycle			7th Cycle		
			Op.	Addr. (1)	Data	Op.	Addr.	Data Out.	Op.	Addr.	Data Out.
RD	Read/ Reset Memory Array	1+	Read	Read Address	Data	Read	Read Address	Data	Read	Read Address	Data
RD	Read Memory Array	3+	Read	Read Address	Data	Read	Read Address	Data	Read	Read Address	Data
RSIG	Read Electronic Signature	3+	Read (2,3)	Signature Address	Signature	Read (2,3)	Signature Adress	Signature	Read (2 3)	Signature Adress	Signature
RSP	Read Sector Protection	3+	Read (2,4)	Protection Address	Protect Status (6)	Read (2,4)	Protection Address	Protect Status (6)	Read (2,4)	Protection Address	Protect Status (6)
PG	Program	4	Read Data Polling or Toggle Bit until Program completes								
SE	Sector Erase	6	Write	x2AAAh (5)	55h	Write	Sector Address	30h	Write (6)	Additional Sector	30h
BE	Bulk Erase	6	Write	x2AAAh (5)	55h	Write	x5555h (5)	10h	Read Data Polling or Toggle bit until Erase completes or Erase is suspended another time		
ES	Erase Suspend	1	Read until Toggle stops, then read all the data needed from any sector(s) not being erased then Resume Erase								
ER	Erase Resume	1	Read Data Polling or Toggle Bit until Erase completes or Erase is suspended another time								

Notes: 1. X = Don't Care.
2 The first cycle of the RD, RSP or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of read cycles can occur after one command cycle
3. Signature Address bits A0, A1, A6 at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1, A6 at V_{IL} will output Device code (0E2h)
4. Protection Address· A0, A6 at V_{IL} and A1 at V_{IH}, other addresses within the sector to be checked A16, A17, A18 define this Sector Address.
5 Address bits A16, A17, A18 are don't care for coded address inputs
6. Optional, additional sectors addresses must be entered within a 80µs delay after last write entry, timeout status can be verified through DQ3 value When full command is entered, read Data Polling or Toggle bit until Erase is completed

DESCRIPTION (cont'd)

erased over 100,000 cycles. Each sector may separately be protected and unprotected against program and erase. Sector erasure may be suspended, while data is read from other blocks of the memory, and then resumed.

Bus Operations

Seven operations can be performed by the appropriate bus cycles, Read Array, Read Electronic Signature, Output Disable, Standby, Protect Sector, Unprotect Sector, and Write the Command of an Instruction.

Command Interface

Command Bytes can be written to a Command Interface (C.I.) latch to perform Reading (from the

Table 7. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Bulk Erase Confirm
30h	Sector Erase Resume/Confirm
80h	Set-up Erase
90h	Read Electronic Signature/ Sector protection Status
0A0h	Program
0B0h	Erase Suspend
0F0h	Read Array/Reset

Table 8. Status Register

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase on Going	
		DQ	Program Complete	
		$\overline{DQ}$	Program on Going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program on Going	Sucessive read output complementary datas on DQ6 while Programming or Erase operations are going on. DQ6 remain at constant level when P/E.C. operations are completed.
		'-0-0-0-0-0-0-0-'	Program ('0' on DQ6) Complete	
		'-1-1-1-1-1-1-1-'	Erase or Program ('1' on DQ6) Complete	
5	Error Bit	'1'	Program or Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
		'0'	Program or Erase Success	
4		'1'		
		'0'		
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES). Additional sector to be erased in parallel can be entered to the P/E.C.
		'0'	Erase Timeout Period on Going	
2				
1				
0	Reserved			

Notes: Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations.

DESCRIPTION (cont'd)

Array or Electronic Signature), Erasure or Programming. For added data protection, command execution starts after 4 or 6 command cycles. First, second, fourth and fifth cycles are used to input a code sequence to the Command Interface (C.I.). This sequence is equal for all P/E.C. instructions. Command itself and its confirmation - if it applies - are given on the third and fourth cycles.

Instructions

Seven instructions are defined to perform Read Memory Array, Read Electronic Signature, Auto Program, Sector Auto Erase, Auto Bulk Erase, Sector Erase Suspend and Sector Erase Resume. The internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides Data Polling, Toggle, and Status data to indicate completion of Program and Erase Operations.

Instructions are composed of up to six cycles. The first two input a code sequence to the Command Interface which is common to all P/E. C. instructions (see Table 7 for Command Descriptions). The third cycle inputs the instruction set up command instruction to the Command Interface. Subsequent cycles output the addressed data for Read operations. For added data protection, the instructions for program and sector or bulk erase require further command inputs. For a Program instruction, the fourth command cycle inputs the address and data to be programmed. For an Erase instruction (sector or bulk), the fourth and fifth cycles input a further code sequence before the Erase confirm command on the sixth cycle. Byte programming takes typically 10µs while erase is performed in typically 1.5 seconds.

Erasure of a memory sector may be suspended, in order to read data from another sector, and then resumed. Data Polling, Toggle and Error data may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. When power is first applied or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Array.

DEVICE OPERATION

Signal Descriptions

A0-A18 Address Inputs. The address inputs for the memory array are latched during a write operation. The A9 address input is used also for the Electronic Signature read and Sector Protect verification. When A9 is raised to V_{ID}, either a Read Manufacturer Code, Read Device Code or Verify Sector Proctection is enabled depending on the combination of levels on A0, A1 and A6. When A0, A1 and A6 are Low, the Electronic Signature Manufacturer code is read, when A0 is High and A1 and A6 are Low, the Device code is read, and when A1 is High and A0 and A6 are low, the Sector Protection Status is read.

DQ0-DQ7 Data Input/Outputs. The data input a byte to be programmed or a command written to the C.I., are latched when both Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output is from the memory Array, the Electronic Signature, the Data Polling bit (DQ7), the Toggle Bit (DQ6), the Error bit (DQ5) or the Erase Timer bit (DQ3). Ouputs are valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High deselects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Addresses are then latched on the falling edge of $\overline{E}$ while datas on the rising edge of $\overline{E}$.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation. $\overline{G}$ is forced to V_{ID} level during Sector Protect and Sector Unprotect operations.

$\overline{W}$ Write Enable. This input controls writing to the Command Register and Address and Data latches. Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

V_{CC} Supply Voltage. The power supply for all operations (Read, Program and Erase).

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

Memory Sectors

The memory sectors of the M29F040 are shown in Figure 5. The memory array is divided in 8 sectors of 64K bytes. Each sector can be erased separately or any combination of sectors can be erased simultaneously. The Sector Erase operation is managed automatically by the P/E.C. The operation can be suspended in order to read from any another sector, and then resumed.

Sector Protection provides additional data security. Each sector can be separately protected or unprotected against Program or Erase. Bringing A9 and $\overline{G}$ to V_{ID} initiates protection, while bringing A9, $\overline{G}$ and $\overline{E}$ to V_{ID} cancels the protection. The sector affected is addressed by the inputs on A16, A17, and A18.

Table 9. AC Measurement Conditions

	SRAM Interface Levels	EPROM Interface Levels
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 3. AC Testing Input Output Waveform

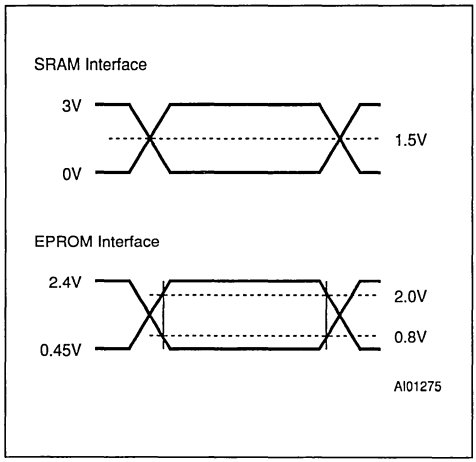


Figure 4. AC Testing Load Circuit

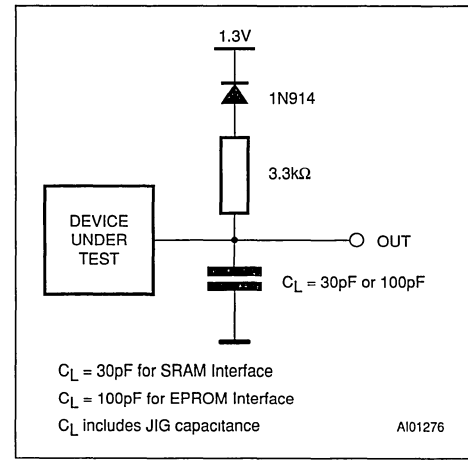


Table 10. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

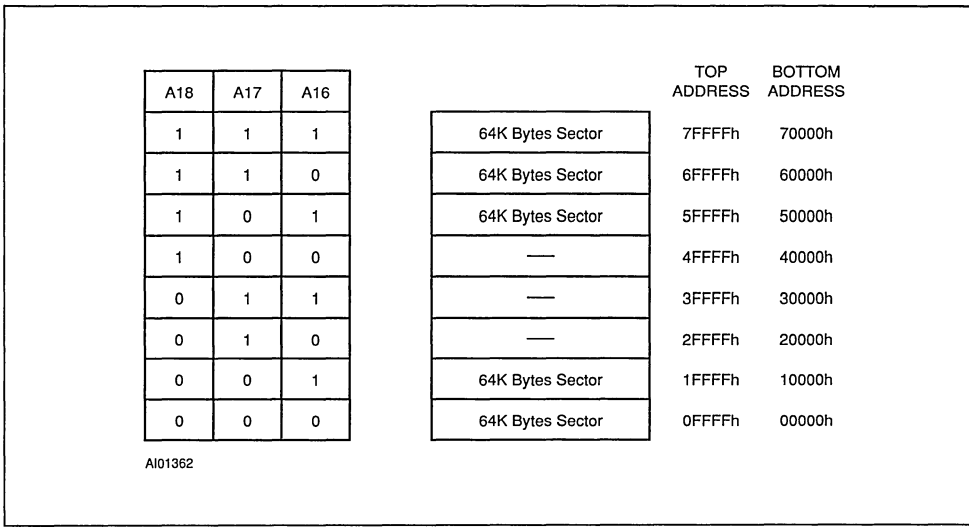
Operations

Operations are defined as specific bus cycles and signals which allow Memory Read, Command Write, Output Disable, Standby, Read Status Bits, Sector Protect/Unprotect, Sector Protection Check and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. The data read depends on the previous command written to the memory (see instructions RD and RSIG, and Status Bits).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs last.

Figure 5. Memory Map and Sector Address Table



A18	A17	A16		TOP ADDRESS	BOTTOM ADDRESS
1	1	1	64K Bytes Sector	7FFFFh	70000h
1	1	0	64K Bytes Sector	6FFFFh	60000h
1	0	1	64K Bytes Sector	5FFFFh	50000h
1	0	0	—	4FFFFh	40000h
0	1	1	—	3FFFFh	30000h
0	1	0	—	2FFFFh	20000h
0	0	1	64K Bytes Sector	1FFFFh	10000h
0	0	0	64K Bytes Sector	0FFFFh	00000h

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Table 11. DC Characteristics
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 6MHz		40	mA
I_{CC2}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		100	µA
I_{CC4}	Supply Current (Program or Erase)	Byte program, Sector or Bulk Erase in progress		60	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12mA		0.45	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4V		V
		I_{OH} = –2.5mA	0.85 x V_{CC}		V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	12.5	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		50	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		3.2	4.2	V

Table 12A. Read AC Characteristics
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	Test Condition	M29F040				Unit
				-70		-90		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
				SRAM Interface		EPROM Interface		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	70		90		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		90	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		90	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		30		35	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		20		20	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		20		20	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory, the manufacturer's code for SGS-THOMSON is 20h, and the device codes is E2h for the M29F040. These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product. The Electronic Signature is output by a Read operation when the voltage applied to A9 is at V_{ID} and address inputs A1 and A6 are at Low. The manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored. The codes are output on DQ0 DQ7. This is shown in Table 4.

The Electronic Signature can also be read, without raising A9 to V_{ID} by giving the memory the instruction RSIG (see below).

Sector Protection. Each sector can be separately protected against Program or Erase. Sector Protection provides additional data security, as it disables all program or erase operations. This

Table 12B. Read AC Characteristics
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	Test Condition	M29F040				Unit
				-120		-150		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
				EPROM Interface		EPROM Interface		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		55	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		35	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		35	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

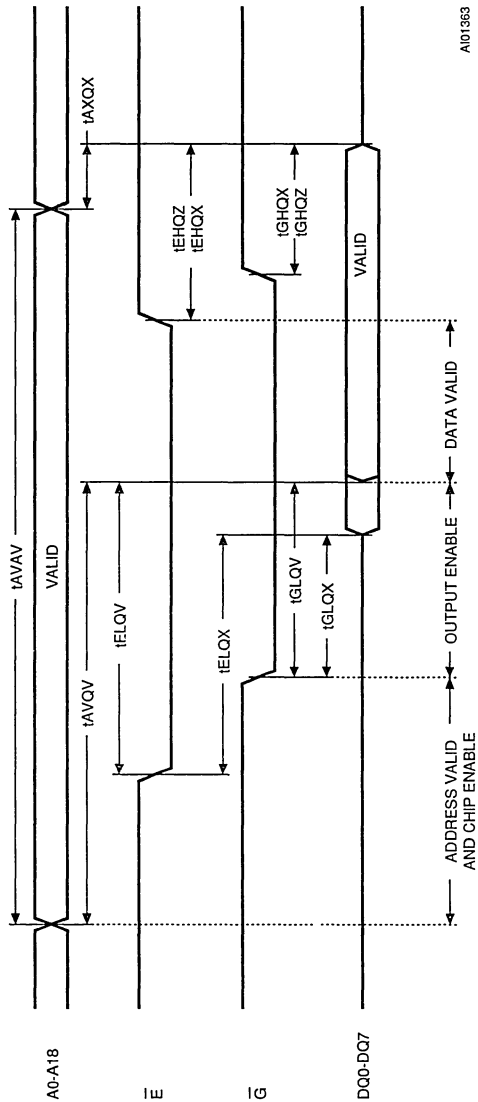
Notes: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

DEVICE OPERATION (cont'd)

mode is activated when both A9 and $\overline{G}$ are set to V_{ID} and the sector address is applied on A16, A17 and A18. Sector protection is programmed using a Presto F program like algorithm. Protection is initiated by edge of $\overline{W}$ falling to V_{IL}. Then after a delay of 100us, the edge of $\overline{W}$ rising to V_{IH} will end the protection operation. Protection verify is achieved by bringing $\overline{G}$, $\overline{E}$ and A6 to V_{IL} while $\overline{W}$ is at V_{IH} and A9 at V_{ID}. Under these conditions, reading the data output will yield 01h if the sector defined by the inputs on A16, A17 and A18 is protected. Any attempt to program or erase a protected sector will be ignored by the device.

Any protected sector can be unprotected to allow content updating. All sectors must be protected before an unprotect operation. Sector unprotect is activated when A9, $\overline{G}$ and $\overline{E}$ are at V_{ID}. The addresses inputs A6, A16, A12 must be maintained at V_{IH}. Sector unprotect is performed through a Presto F Erase like algorithm. Unprotect is initiated by the edge of $\overline{W}$ falling to V_{IL}. After a delay of 10ms, the edge of $\overline{W}$ rising to V_{IH} will end the unprotection operation. Unprotect verify is achieved by bringing $\overline{G}$ and $\overline{E}$ to V_{IL} while A6 and $\overline{W}$ are at V_{IH} and A9 at V_{ID}. In these conditions, reading the output data will yield 00h if the sector defined by the inputs on A16, A17 and A18 is protected. All combinations of A16, A17 and A18 must be addressed in order to ensure that all of the 8 sectors have been unprotected. Sector Protection Status is shown in Table 5.

Figure 6. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Table 13A. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	70		90		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	35		45		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	30		45		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		45		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$

Instructions and Commands

The Command Interface (C.I.) latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Electronic Signature, Sector Erase, Bulk Erase, Program, Sector Erase Suspend and Erase Resume. Commands are made of address and data sequences. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ and data is latched on the rising of $\overline{W}$ or $\overline{E}$. The instructions require from 1 to 6 cycles, the first or first three of which are always write operations used to initiate the command. They are followed by either further write cycles to confirm the first command or execute the command immediately. Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to assure maximum data security. Commands are initialised by two preceding coded cycles which unlock the Command Interface. In addition, for Erase, command confirmation is again preceeded by the two coded cycles.

P/E.C. status is indicated during command execution by Data Polling on DQ7, detection of Toggle on DQ6, or Error on DQ5 and Erase Timer DQ3 bits. Any read attempt during Program or Erase command execution will automatically output those four bits. The P/E.C. automatically sets bits DQ3, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1, DQ2 and DQ4) are reserved for future use and should be masked.

Table 13B. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C)

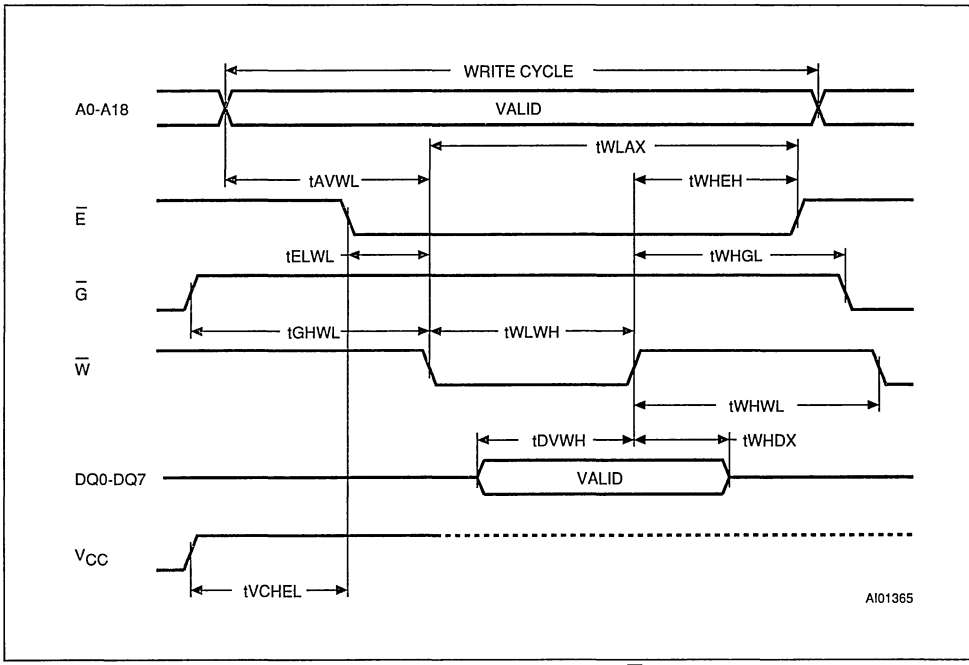
Symbol	Alt	Parameter	M29F040				Unit
			-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		50		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$

Data Polling Bit DQ7. When Programming operations are in progress, this bit outputs the complement of the bit being programmed on DQ7. During Erase operation, it will outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid only effective during P/E.C. operation, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. It must be performed at the address being programmed or at an address within the sector being erased. If the sector to be erased is protected, if the byte to be programmed belongs to a protected sector or if all of the sectors are protected, DQ7 will set to data complement for about 100µs for erase, and then return to previous addressed memory data. The programming of a protection sector is ignored. See Figure 9 for the Data Polling flowchart and Figure 10 for the Data Polling waveforms.

Toggle Bit DQ6. When Programming operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following toggling of either $\overline{G}$ or $\overline{E}$ when $\overline{G}$ is low. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit is valid only effective during P/E.C. operations, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. If the sector to be erased is protected, if the byte to be programmed belongs to a protected sector or if all of the sectors are protected, DQ6 will toggle for about 2µs for programming and 100us for erase and then stop toggling and return back to Read. See Figure 11 for Toggle Bit flowchart and Figure 12 for Toggle Bit waveforms.

Figure 7. Write AC Waveforms, $\overline{W}$ Controlled



Note: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.

Error bit DQ5. This bit is set to '1' by the P/E.C when there is a failure of byte programming, sector erase, or bulk erase that results in invalid data being programmed in the memory sector. In case of error in sector erase or byte program, the sector in which the error occured or to which the programmed byte belongs, must be discarded. Other sectors may still be used. Error bit resets to '0' after Read/Reset (RD) instruction.

Erase Timer bit DQ3. This bit is set to '0' by the P/E.C. when the last Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the waiting period is finished, DQ3 returns back to '1'.

Coded Cycles. The two coded cycles unlock the Command Interface. They are followed by a command input or a comand confirmation. They consist in writing the data 0AAh at address 5555h during first cycle and data 55h at address 2AAAh during second cycle. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ while data is latched on the rising edge of $\overline{W}$ or $\overline{E}$. They happen on first and second cycles of the command write or on the fourth and fifth cycle.

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0F0h at address 2555h. It can be optionally preceded by the two coded cycles. Subsequent read operations will read the memory array addressed and output the read byte.

Table 14A. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	70		90		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	35		45		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	30		45		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	45		45		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		ns
t_{EHQV1} (1)		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2} (1)		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$

Read Electronic Signature (RSIG) instruction. This instruction uses the two coded cycles followed by one write cycle giving the command 90h to address 5555h for command setup. Subsequent read will output the manufacturer code, the device code or the sector protection status depending on the levels of A0, A1, A6, A16, A17 and A18. The manufacturer code, 20h, is output when the addresses lines A0, A1 and A6 are Low, the device code, 0E2h is output when A0 is High with A1 and A6 Low.

Read Sector Protection. The use of Read Electronic Signature (RSIG) command also allows access to the sector protection status verify. After giving the RSIG command, A0 and A6 are set to V_{IL} with A1 at V_{IH}, while A16, A17 and A18 define the sector of the sector to be verified. A read in these conditions will output a 01h if sector is protected and a 00h if sector is not protected.

Bulk Erase (BE) instruction. This instruction uses six write cycles. The Erase Set-up command 80h is written on third cycle to address 5555h after the two coded cycles. The Bulk Erase Confirm command 10h is written at address 5555h on sixth cycle after another two coded cycles. If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing to 0FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register bits. During the execution of the erase by the P/E.C., Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle Bit DQ6 toggles during erase operation and stops when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure because the erasure has not been verified even after the maximum number of erase cycles have been executed.

Table 14B. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	50		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		ns
t_{EHQV1} (1)		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2} (1)		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns

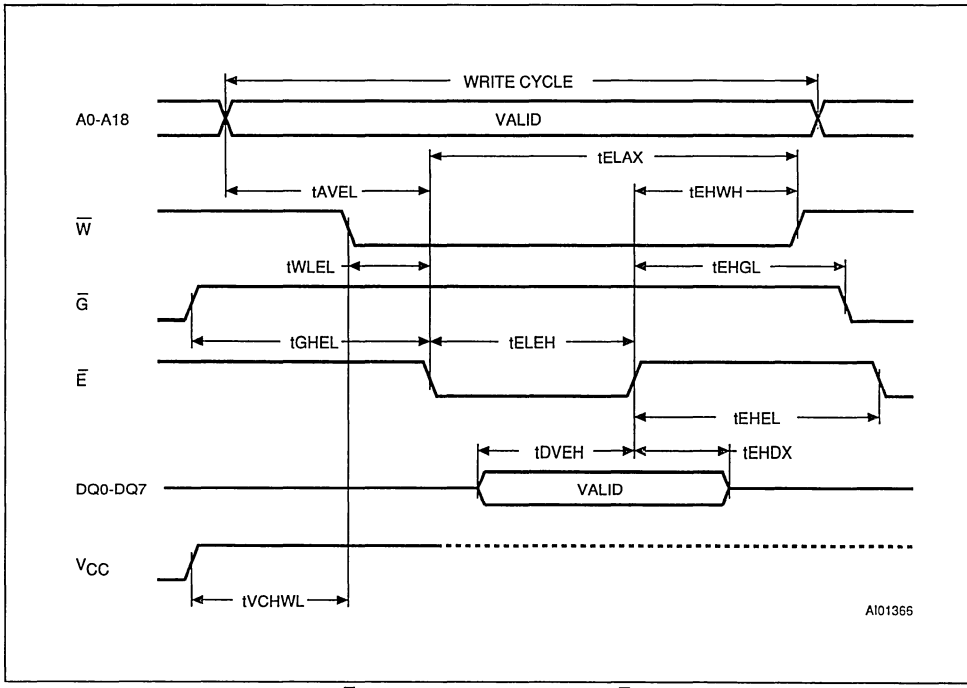
Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$

Sector Erase (SE) instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written on third cycle to address 5555h after the two coded cycles. The Sector Erase Confirm command 30h is written on sixth cycle after another two coded cycles. During the input of the second command an address within the sector to be erased is given and latched into the memory. Additional Sector Erase confirm commands and sector addresses can be written subsequently to erase other sectors in parallel without further coded cycles. The erase will start after an Erase timeout period of about 100us. Thus, additional Sector Erase commands must be given within this delay. The input of a new Sector Erase command will restart the timeout period.

The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Sector Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the P/E.C is erasing the sector(s). If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the sector with 00h as the P/E.C. will do this automatically before to erasing to 0FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register status bits.

During the execution of the erase by the P/E.C., the memory accepts only the ES (Erase Suspend) instruction. Data Polling bit DQ7 returns '0' while the erasure is in progress and '1' when it has

Figure 8. Write AC Waveforms, $\overline{E}$ Controlled



Note: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.

completed. The Toggle Bit DQ6 toggles during erase operation. It stops when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure because erasure has not been verified even after the maximum number of erase cycles have been executed.

Program (PG) instruction. This instruction uses four write cycles. The Program command A0h is written on third cycle after two coded cycles. A fourth write operation latches the Address on the falling edge of $\overline{W}$ or $\overline{E}$ and the Data to be written on its rising edge and starts the P/E.C. Read operations output the status bits after the programming has started. Memory programming is made only by writing '0' in place of '1' in a Byte.

Erase Suspend (ES) instruction. The Sector Erase operation may be suspended by this instruction which consists of writing the command 0B0h without any specific address code. No coded cycles are required. It allows reading of data from another sector while erase is in progress. Erase suspend is accepted only during the Sector Erase instruction execution. Writing this command during Erase timeout will, in addition to suspending the erase, terminate the timeout. The Toggle Bit DQ6 stops toggling when the P/E.C. is suspended. Toggle Bit status must be monitored at an address out of the sector being erased. During the suspension the memory will respond only to Read (RD), or Erase Resume (ER) instructions. Read operations initially output the status bits while erase is suspended but, following a Read instruction, data from other sectors of the memory can be read.

Table 15A. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
			SRAM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{WHQ7V1} (2)		Write Enable High to DQ7 Valid (Program W Control		10		10	µs
t_{WHQ7V2} (2)		Write Enable High to DQ7 Valid (Erase W Controller	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)		Chip Enable High to DQ7 Valid (Program E Controller		10		10	µs
t_{EHQ7V2} (2)		Chip Enable High to DQ7 Valid (Erase E Controlled	1.5	30	1.5	30	sec
t_{Q7VQV}		Q7 Valid to Output Valid (Data Polling)		30		35	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2}		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHQV1}		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2}		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any coded cycle.

Programing. The memory can be programmed byte-by-byte. The program sequence is started by two coded cycles, followed by writing the Program command (0A0h) to the Command Interface, this is followed by writing the address and data byte to the memory. The Program/Erase Controller automatically starts and performs the programming after the fourth write operation. During programming the memory status is checked by reading the status bits DQ3, DQ5, DQ6 and DQ7 which shows the status of the P/E.C. DQ6 and DQ7 determine if programming is on going or has completed and DQ5 allows a check to be made for any possible error.

Power Up

The memory Command Interface is reset on power up to Read Array. Either $\overline{E}$ or $\overline{W}$ should be tied to V_{IH} to allow maximum security. Any write cycle initiation is blocked when V_{CC} is below V_{LKO}.

Supply Rails

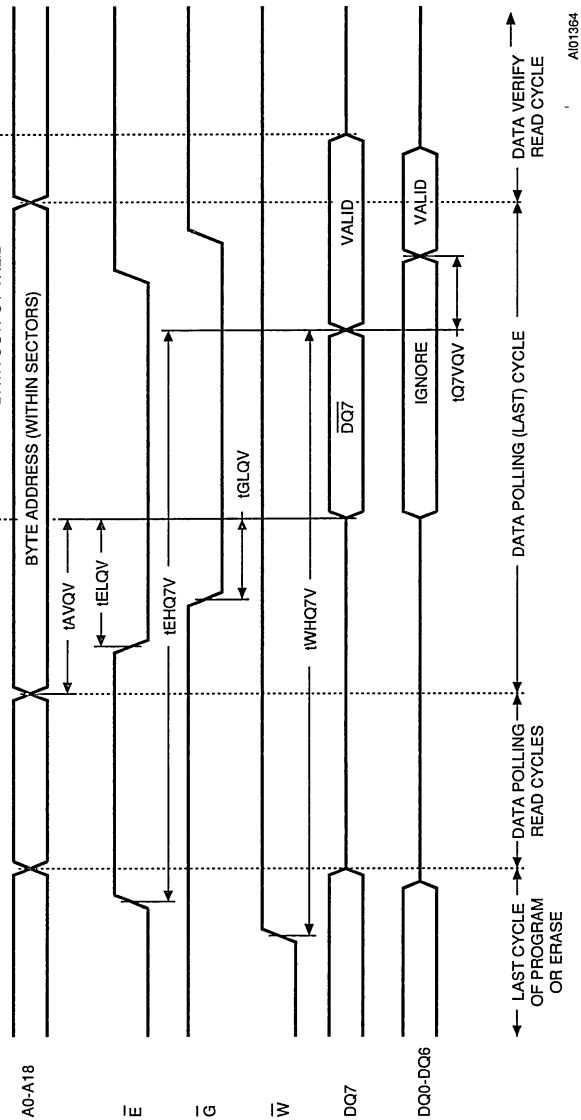
Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{CC} program and erase currents required.

Table 15B. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-120		150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			EPROM Interface		EPROM Interface		
			Min	Max	Min	Max	
t_{WHQ7V1} (2)		Write Enable High to DQ7 Valid (Program W Control		10		10	µs
t_{WHQ7V2} (2)		Write Enable High to DQ7 Valid (Erase $\overline{W}$ Controller	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)		Chip Enable High to DQ7 Valid (Program $\overline{E}$ Controller		10		10	µs
t_{EHQ7V2} (2)		Chip Enable High to DQ7 Valid (Erase $\overline{E}$ Controlled	1.5	30	1.5	30	sec
t_{Q7VQV}		Q7 Valid to Output Valid (Data Polling)		50		55	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)		10		10	µs
t_{WHQV2}		Write Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec
t_{EHQV1}		Chip Enable High to Output Valid (Program)		10		10	µs
t_{EHQV2}		Chip Enable High to Output Valid (Erase)	1.5	30	1.5	30	sec

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Figure 9. Data Polling DQ7 AC Waveforms



Notes: 1. All other timings are as a normal Read cycle.
2. DQ7 and DQ0-DQ6 can transmit to valid at any point during the data output valid period.
3. t_{WHQ7V} is the Program or Erase time.
4. During erasing operation Byte address must be within Sector being erased.

Figure 10. Data Polling Flow-chart

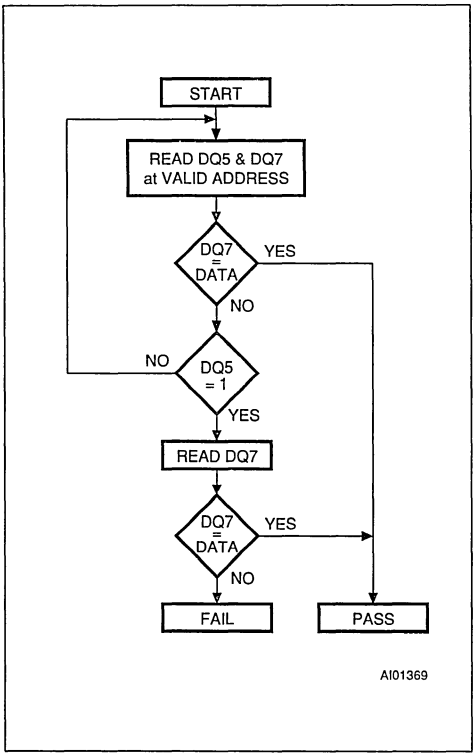


Figure 11. Data Toggle Flow-chart

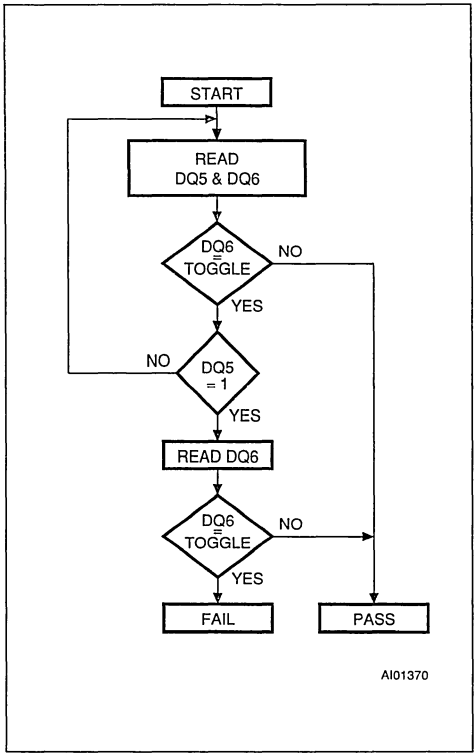
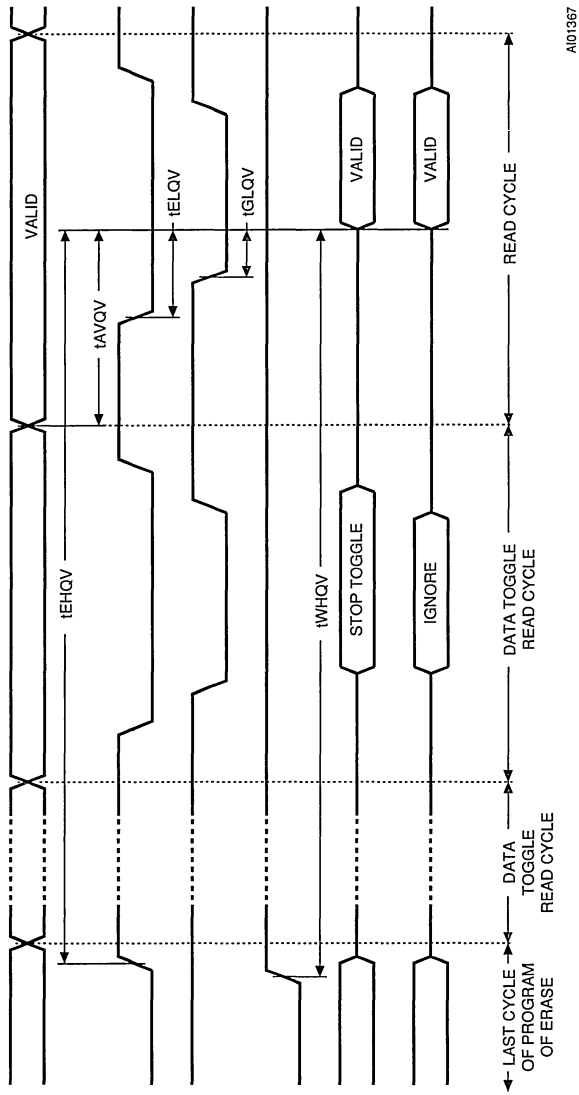


Table 16. Program, Erase Times and Program, Erase Endurance Cycles
(T_A = 0 to 70°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	M29F040			Unit
	Min	Typ	Max	
Chip Program (Byte)		8.5		sec
Bulk or Sector Erase		1.5	30	sec
Byte Program		10		µs
Program/Erase Cycles	100,000			cycles

Figure 12. Data Toggle DQ6 AC Waveforms



Note: All other timings are as a normal Read cycle.

Figure 13. Sector Protection Flow-chart

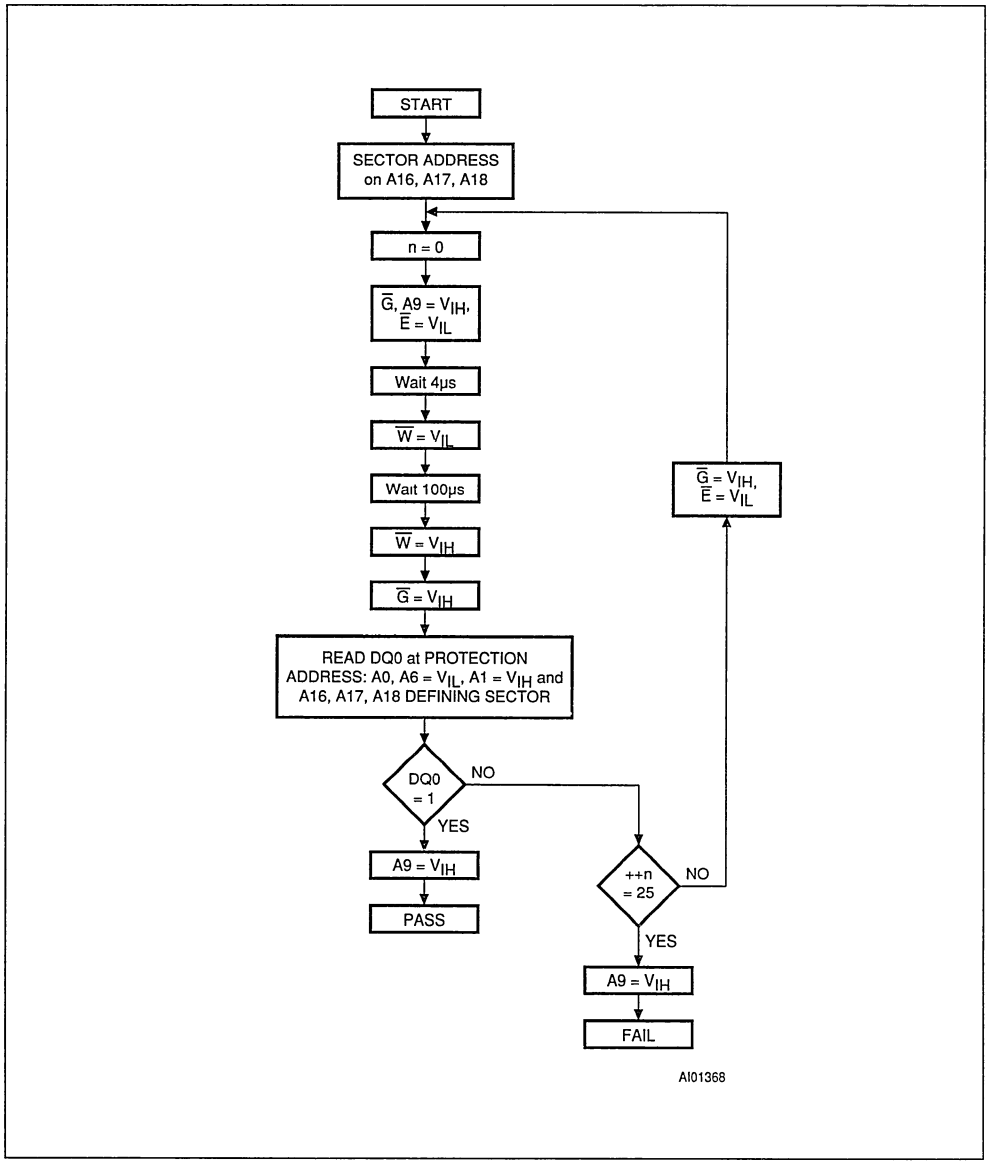
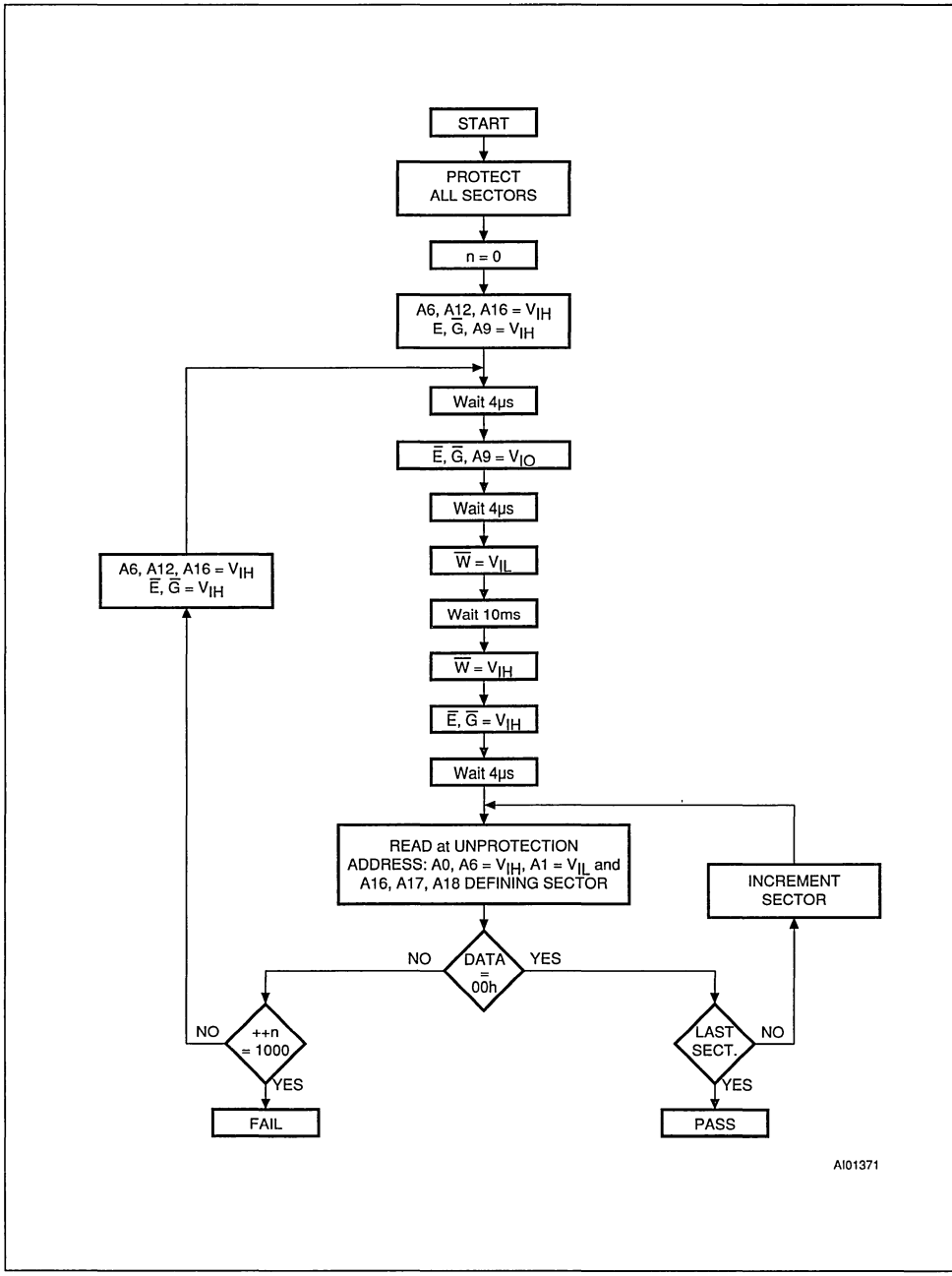
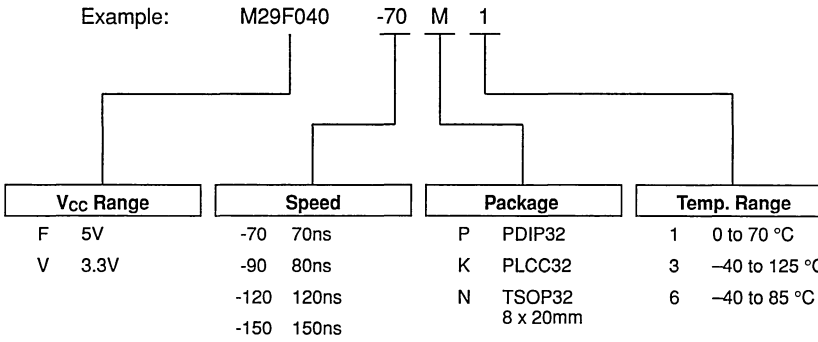


Figure 14. Sector Unprotecting Flow-chart



ORDERING INFORMATION SCHEME



Full data on the 3V product, M29V040, will be added to this document in the near future.

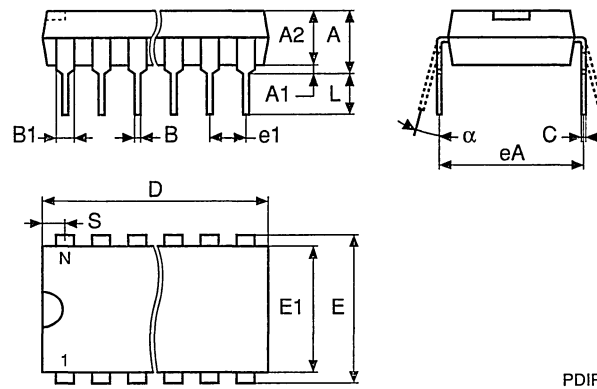
For a list of available options (V_{CC} Range, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PDIP32 - 32 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.83			0.190
A1		0.38	–		0.015	–
A2	–	–	–	–	–	–
B		0.41	0.51		0.016	0.020
B1		1.14	1.40		0.045	0.055
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
E		15.24	15.88		0.600	0.625
E1		13.46	13.97		0.530	0.550
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	15°		0°	15°
N	32			32		

PDIP32



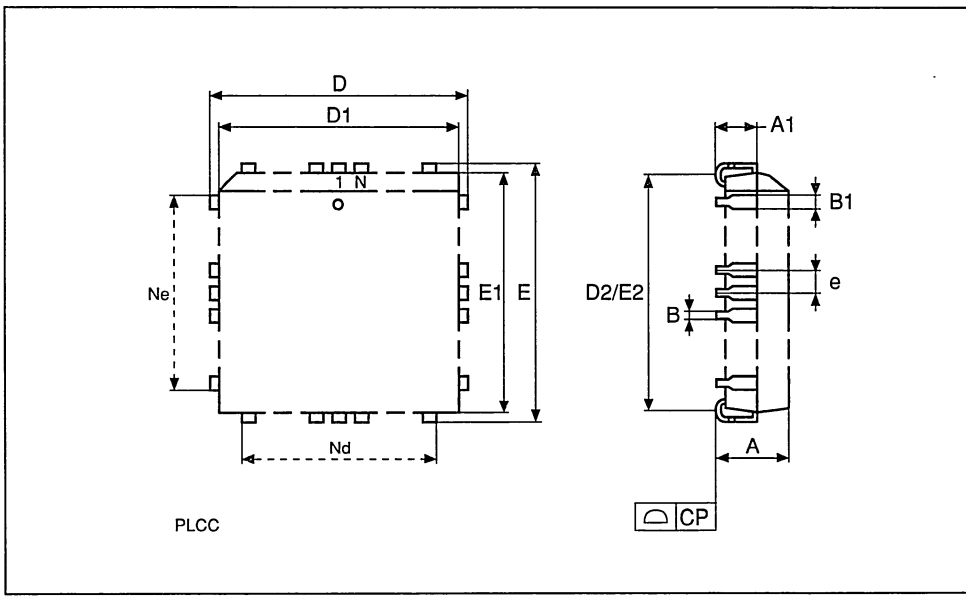
PDIP

Drawing is out of scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

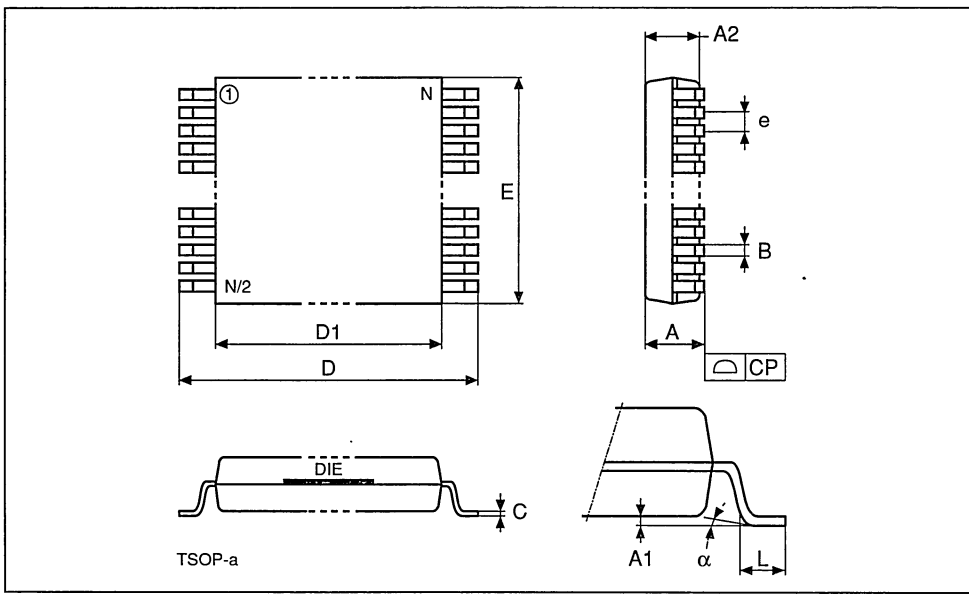


Drawing is out of scale

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.50		0.037	0.059
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0 °C	5 °C		0 °C	5 °C
N		32			32	
CP			0.10			0.004

TSOP32



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