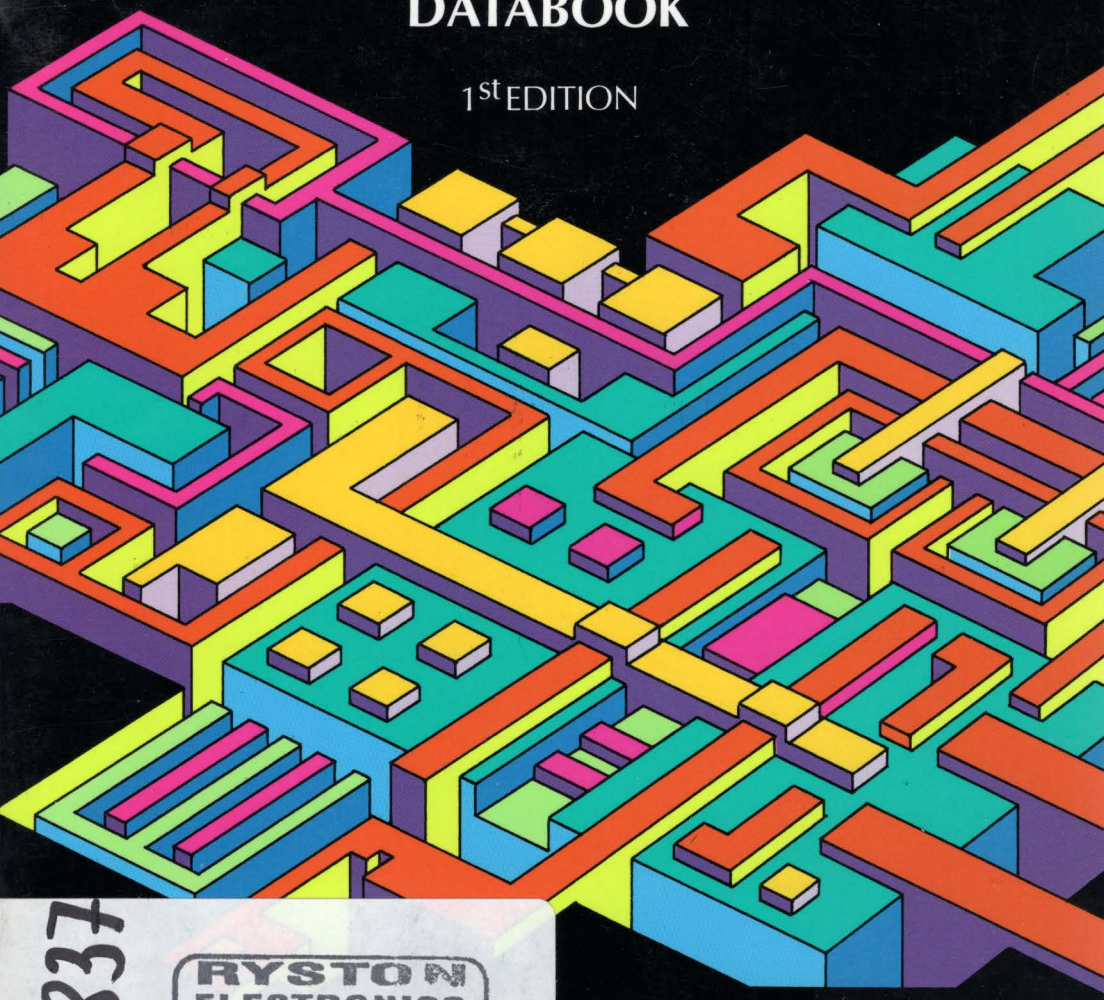
ISB24000 SERIES
CONTINUOUS ARRAYS
MODULE GENERATORS

DATABOOK

1st EDITION



SGS-THOMSON
MICROELECTRONICS

ISB24000 SERIES
CONTINUOUS ARRAYS
MODULE GENERATORS

DATABOOK

1st EDITION

OCTOBER 1992

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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SGS-THOMSON Microelectronics Semicustom Product Portfolio - 1992

Family	Product	Process	Complexity/ Density	Features
Sea Of Gates	ISB12000	CMOS 1.2µm, DLM	1,000 to 50,000 Gates	Cost effective
Sea Of Gates	ISB18000	CMOS 0.8µm, DLM	2,500 to 19,500 Gates	Bus Optimized Array
Sea Of Gates	ISB24000	CMOS 0.7µm, TLM	3,100 to 216,000 Gates	Performance/Compilers
Standard Cells	CB12000	CMOS 1.2µm, DLM	500 Gates/mm^2	Compilers
Standard Cells	CB22000	CMOS 0.7µm, DLM	1250 Gates/mm^2	High Density Compilers
Analog Arrays	Polyuse K	Bipolar 3µm, SLM	906 Components	3GHz NPN
Mixed A/D Arrays	Polyuse J	Bipolar 3µm, DLM	400-23000 Components	3GHz NPN
Filter Arrays	TSGF	CMOS 3µm, SLM	4 to 12th Order	DC-30KHz
Mixed A/D Standard Cells	TSGSM	CMOS 3.5µm, SLM	1Kgates + Analog	
Mixed A/D Standard Cells	STKM2000	BiCMOS 2µm, DP, DLM	10Kgates + Analog	6GHz NPN

THE COMPANY

SGS-THOMSON Microelectronics is a broad-range supplier of advanced semiconductor products. With extensive manufacturing capability in Europe, North-America and the Far-East, the company is dedicated to meeting customer needs with cost effective, world-class technologies and products.

The company is a leading semiconductor supplier with total 1991 revenues of approx 1.5 billion US dollars, and employs 17,000 worldwide. From a predominantly European revenue basis in the '70s, the company has penetrated markets farther afield so that in 1991, 40% of is revenue came from regions outside of Europe.

With 17 production facilities, 25 design centers, and 8 advanced Research and Development sites, the company continues to demonstrate its world-wide commitment to excellence in technology and product design. Additionally, with 42 direct sales offices in 20 countries, and over 500 distributors and sales representatives, customers are never far from the service and support needed to be successful in utilizing these products.

With Research and Development expenditure as well as capital investment well above the industry average, SGS-THOMSON Microelectronics is dedicated to bring an increasing portfolio of innovative and advanced new products with the service level needed to succeed in today's and tomorrow's electronics.

THE PRODUCTS

The ISB24000 is a high performance Continuous Array series intended for computer, telecommunications and data processing applications.

Manufactured with a 0.7 micron triple level metal HCMOS process, the ISB24000 Series has a library containing more than 200 SSI elements, 200 macrofunctions and compilable megacells for SPRAM, DPRAM and ROM.

This product features 0.25 ns internal speeds while offering high current, off-chip drive capability up to 24 mA. The total gate count ranges from 3,100 to 216,000 usable gates and the I/O cell count ranges from 48 to 400 full function cells. Extended features include buskeeper I/O cells, fully supported IEEE JTAG 1149.1 I/O and optional 3.3 V power supply for macrocells. The ISB24000 also support variable slew rate, independent power supply distribution and double drive output devices.The full semicuston product portfolio includes Digital Standard Cells, Customer Owned Tooling and Mixed Analog/Digital Products as well as Sea Of Gates.

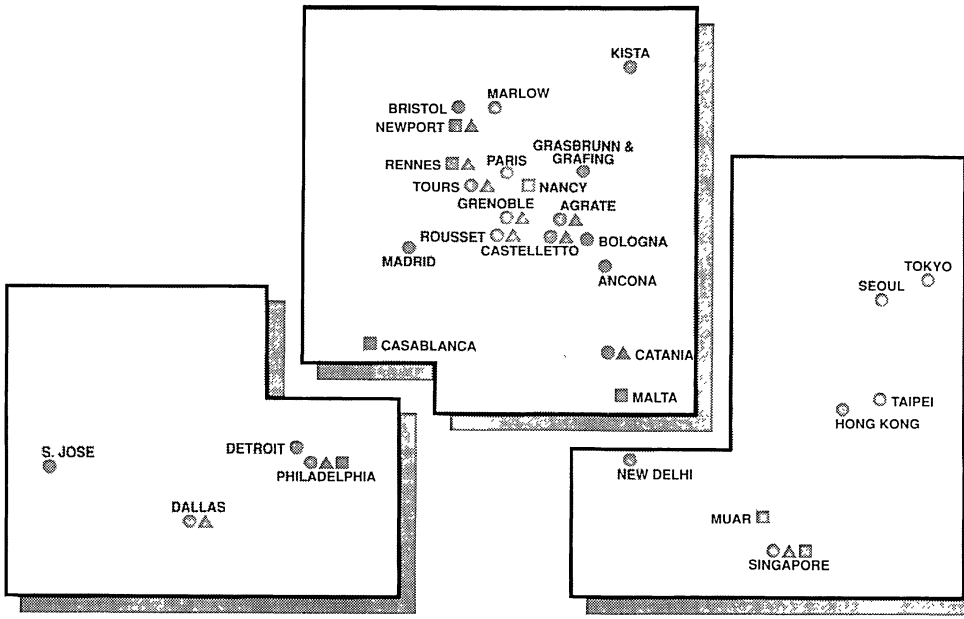
Contact your nearest SGS-THOMSON Microelectronics Sales Office for full details on all products, technologies and services.

SUPPORT

With an extensive network of Design Centers, customers from all the major countries can obtain support for feasibility studies, architecture analysis and design.

These design centers are fully equipped with design capability and their computers are interconnected with the center to allow efficient design transfer and fast response time.

THE SGS-THOMSON GROUP



▲ Front-End
■ Back-End
● Research/Design Centers

SGS-THOMSON MICROELECTRONICS

ISB24000 SERIES

SINGLE PORT RAM GENERATOR

DESCRIPTION

The ISB24000 SERIES SINGLE PORT RAM generator builds a single port static RAM, each RAM cell having a six transistor implementation. Standard read and write operations are supported as well as a read-modify-write cycle.

FEATURES

- Fully static, synchronous operation.
- Total memory capacity (words x bits) : 8K bits.
- Word range of 8 to 2048 words.
- Bit range from 1 to 64 bits in single bit increments limited by mux selection.
- Selectable aspect ratio by use of the Row/Column multiplexing.
- Row/Column multiplexing factor 1, 2, 4, 8 or 16.
- Separate data input and output buses.
- Tristate double drive output buffers.
- Read-modify-write and write-thru operations supported.

RAM OPERATION

The single port RAM uses a static synchronous architecture with timing dependent on the chip select input. A RAM cycle is defined as the time between two consecutive falling edges of the CSN (chip select) signal. When CSN is low the RAM is selected, when CSN is high the RAM is deselected.

The RAM cell is a fully static 6 transistor implementation. Differential sense amplifiers are used to speed up the read access times. These sense amplifiers are powered down after access to provide minimum standby current.

For correct functionality of the RAM during a read or write operation, the address signals must be setup for time 't_{as}' before CSN is enabled and must remain stable for time 't_{ah}' after CSN goes high. Additionally, it is important to note that in order to ensure correct functionality, the CSN signal must be toggled (1- 0 -1) for each individual RAM cycle to allow for precharge between consecutive cycles.

The output buffers are controlled by both OEN and CSN. If both CSN and OEN are low the output bus is in alow impedance state. If either OEN or CSN are high the bus is in a high impedance state. In all cases CSN high will disable the output bus.

Note: It is the responsibility of the user to make sure all tristate buses on chip are controlled, i.e. not floating. A floating bus will cause high Icc standby current and possible operational problems in other parts of the circuit. The SPRAM output bus is always floating when CSN is high.

Read Cycle

A read cycle is initiated by the falling edge of the CSN signal and ends when CSN returns high. Valid data will be available after time 't_{aa}'. Throughout the read cycle the WEN (write enable) signal must be high and the OEN (output enable) signal must be low in order for the selected data to appear on the dataout bus. See timing diagram, page 5.

Note: In non power of 2 RAM configurations it is possible to select non-existent row addresses and put the RAM into a high power consumption mode. It is up to the user to supply only valid addresses to the RAM core. Invalid addresses are those greater than the maximum word count but less than the next power of 2 address boundary.

Write Cycle

A write cycle is initiated by the falling edge of OR(CSN,WEN) and ends when OR(CSN,WEN) returns high. During a write operation, input data must be setup before the rising edge of OR(CSN,WEN) and must be held for a minimum hold time after OR(CSN,WEN) has returned high. The datain bus may change during OR(CSN,WEN) low as long as the setup and hold times are satisfied. The status of OEN does not effect either the write or write thru operations, only the impedance of the output bus. If OEN is low the input data will write thru the sense amplifiers and be available on the dataout bus. If WEN goes high before CSN, the write operation will cease and the RAM will be in a read mode until CSN returns high. The written data will remain valid on the dataout bus as long as both CSN and OEN remain low. See figure 2 for timing diagram.

Note: OR(CSN,WEN) is the logical OR of signals CSN and WEN.

Note: In non power of 2 RAM configurations it is permissible to write to non-existent addresses. The RAM will not draw high current. The data will not be written to any RAM location, but will appear on the dataout bus if OEN is low (write thru).

Note: If a write cycle is terminated by disabling WEN (high) prior to the positive transition of CSN, the output drivers will be at an indeterminate state resulting in excessive power consumption until CSN is deactivated. The output bus (if OEN low) will also drive an indeterminate state which can propagate through connected gate logic causing excessive power consumption

Read-Modify -Write Cycle

The read-modify-write operation allows a value to be read and modified during a single RAM cycle. The read-modify-write cycle is initiated in the same manner as a read cycle, with the falling edge of the CSN signal while WEN is high and a valid address present on the address bus. The write operation in the read-modify-write cycle begins on the falling edge of WEN, while CSN is still low. Before this time, OEN must be low to allow the placing of data on the dataout bus. The total time required for the operation of a read-modify-write cycle is greater than for either a read or write cycle. See figure 3 for timing diagram. All cautions mentioned in the read and write cycle descriptions remain in effect for the read-modify-write operation.

Write-thru Operation

Data being written to the RAM will appear at the inputs to the sense amplifiers. If OEN is low this data will appear on the dataout bus while CSN is low. See other operations for more details.

ROW/COLUMN MULTIPLEXING

The MUX parameter is user programmable to allow varying internal RAM architecture options. Specifically, the parameter will be used to determine the row and column decoding scheme for the RAM bit array. The value chosen will determine how many words of requested bit width are to be defined on each row of memory array. Due to the direct implication on RAM architecture, the MUX parameter will affect the aspect ratio (width/height), performance, and power consumption of the targeted RAM. The automatic datasheet generators within each SGS-THOMSON design kit allows investigation of each alternative MUX option.

Note: All limits regarding the choice of MUX factor are outlined in the CONSTRAINTS section, page 4.

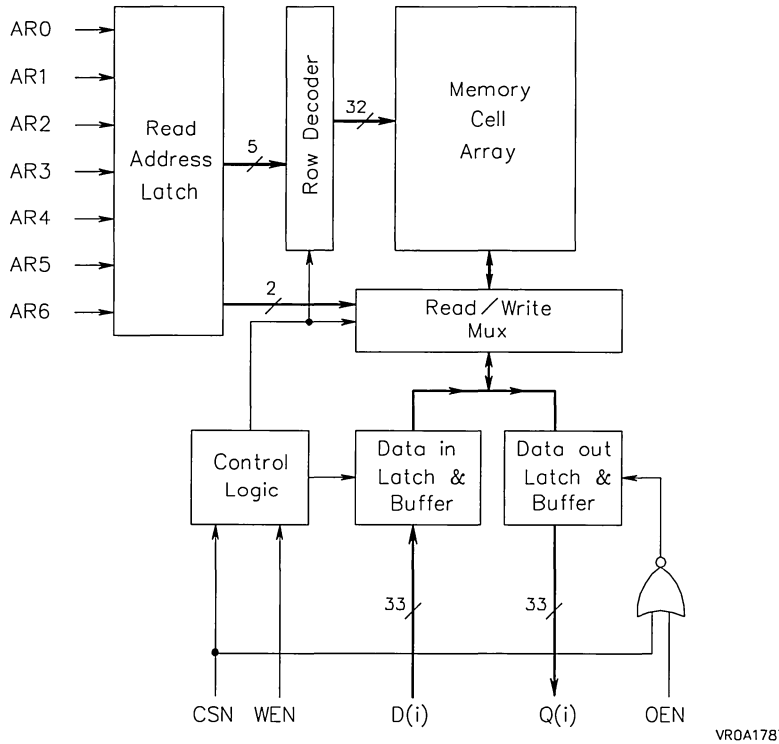
MINIMUM WORD ORGANISATION

As described in the constraints section (page 4) the user defined words parameter must be a multiple of the chosen MUX factor. The ram bit array is symmetrical in nature with an equal number of words on each row. Hence, the user is provided with full access to all RAM array bits through complete bit array decoding. The generator provided in each SGS-THOMSON design kit includes a rules checker to ensure the generation of a RAM which is compliant with this constraint, and which provides the user with the maximum word depth available from the resultant RAM bit array.

Example :	User Defined	Generated
N° of words	33	36
N° of bits	9	9
MUX option	4	4

The resulting generated RAM would be defined with a word witdth of 36 instead of 33 in order to provide full access to the compiled symmetrical RAM bit array.

FUNCTIONAL BLOCK DIAGRAM



CONSTRAINTS

Minimum size available	: 8 bits	
Maximum size available	: 8K bits	
Maximum load on any output	: 82 SL	
Input load	: CSN = 3.58 SL	Chip Select
	WEN = 1 SL	Write Enable
	OEN = 1.58 SL	Output Enable
	A[i] = 3 SL	Address
	D[n] = 2 SL	Datain
Output Load	: Q[n] = .75 SL	Dataout

Possible SPRAM configurations are limited by the number of rows and columns generated as follows:

Number of columns : cols = mux x bits

Minimum number of cols = 1

Maximum number of cols = 64

Number of rows : rows = words / mux

Minimum number of rows = 8

Maximum number of rows = 128

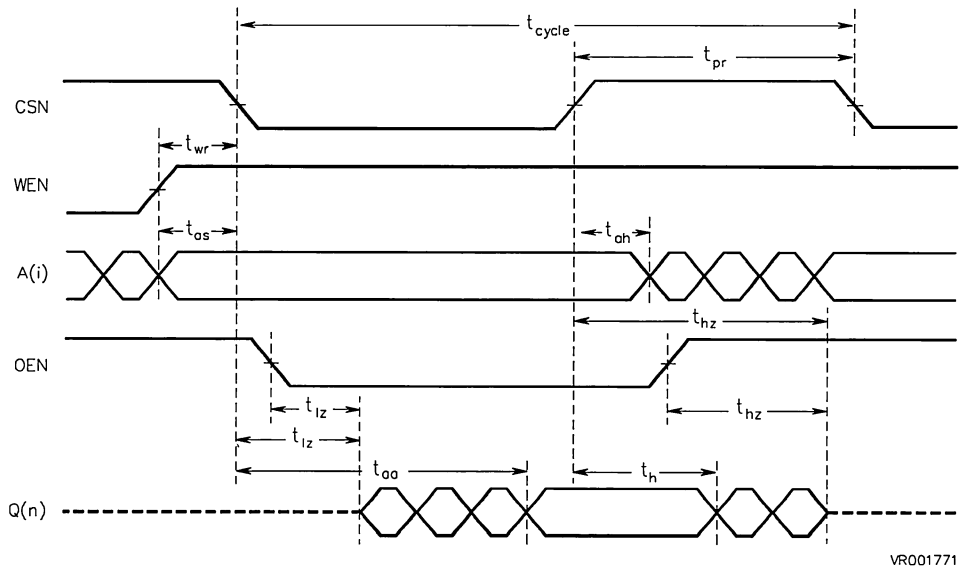
Mux Option	Max Bit	Max Word
1	64	128
2	32	256
4	16	512
8	8	1024
16	4	2048

PERFORMANCE, AREA AND POWER CONSUMPTION ESTIMATIONS

For specific performance, power and area estimations please refer to the ISB24000 SERIES Generator Program available with each SGS-THOMSON design kit or at your local design center.

TIMING DIAGRAMS

Read Cycle

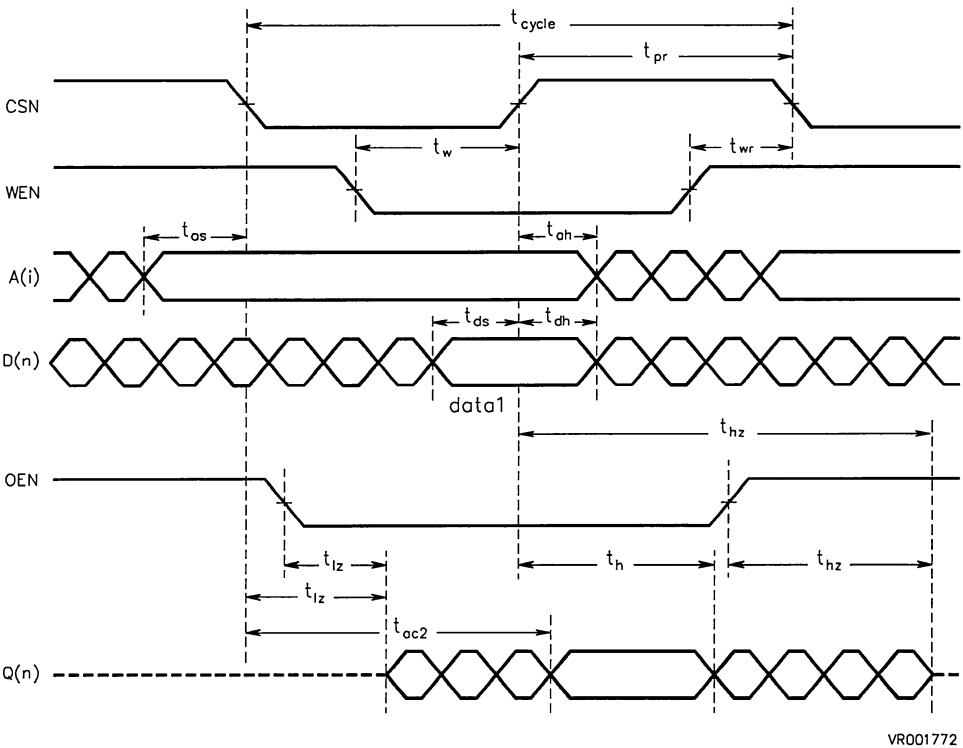


Note: For simulation models 'tcycle' is checked by other parameters

TIMING DIAGRAMS

Write Cycle

CSN Controlled, t_{wh} = Negative Value

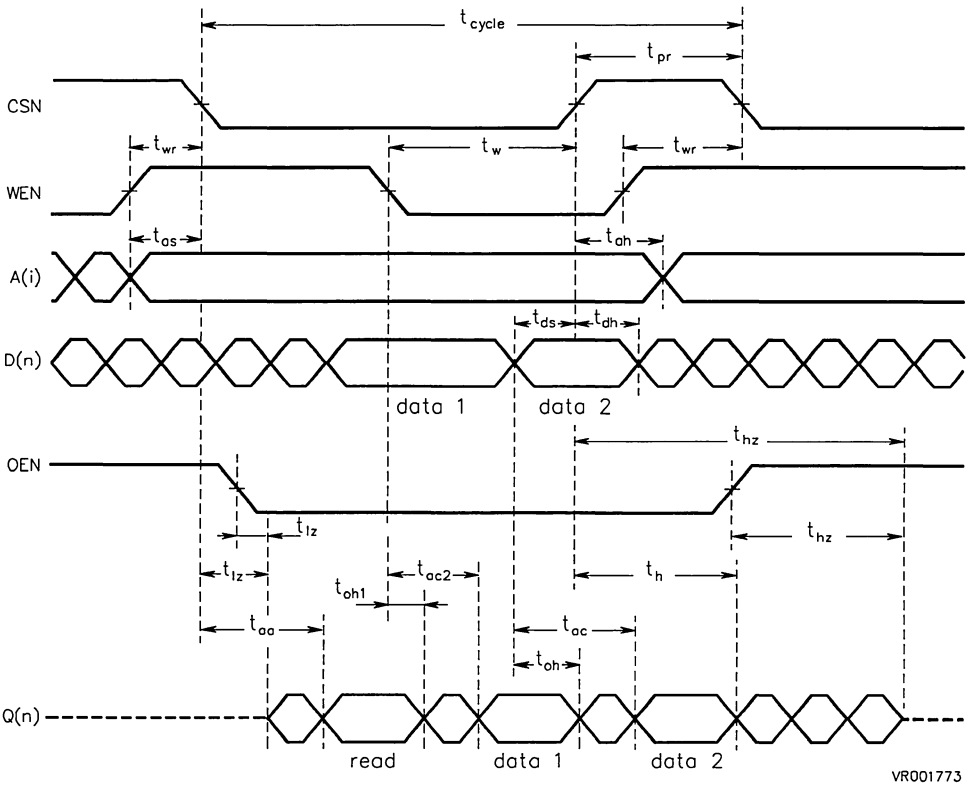


Note: For simulation models 'tcycle' is checked by other parameters.

TIMING DIAGRAMS

Read Modify/Write Cycle

CSN Controlled



Note 1 : For simulation models 't_{cycle}' is checked by other parameters.
Note 2 : For simulation models 't_{oh}' and 't_{oh1}' are assumed to be zero.

Key:-

Parameter	Symbol
ADDRESS	A[i]
CHIP SELECT (active low)	CSN
WRITE ENABLE (active low)	WEN
OUTPUT ENABLE (active low)	OEN
DATA INPUT	D[n]
DATA OUTPUT	Q[n]

AC CHARACTERISTICS (V_{DD} = 5V, T_A = 25°C)

SPRAM GENERATOR 32 words x 8 bits

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading ns/SL
		mux = 1	mux = 2	mux = 4	
t_{pr}	Precharge Time	2.86	2.88	3.03	-
t_{aa}	Address Access Time	2.80	2.98	3.42	0.022
t_{as}	Address Setup Time	1.05	0.53	0.53	-
t_{ah}	Address Hold Time	1.05	1.05	1.05	-
t_w	Write Pulse Width	1.58	1.90	2.36	-
t_{ac}	Write-Thru Access - data	2.22	2.46	2.55	0.022
t_{ac2}	Write-Thru Access - CSN	1.73	2.11	2.36	0.022
t_{wr}	WEN Recovery to CSN	0.53	0.53	0.53	
t_{ds}	Data Setup Time	0.53	0.63	0.73	-
t_{dh}	Data Hold Time	1.13	1.02	1.17	-
t_{lz}	OEN to Low Impedance	0.57	0.57	0.56	0.022
t_{hz}	OEN to High Impedance	1.27	1.27	1.27	-

SPRAM GENERATOR 32 words x 16 bits

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading ns/SL
		mux = 1	mux = 2	mux = 4	
t_{pr}	Precharge Time	3.04	3.21	3.62	-
t_{aa}	Address Access Time	3.08	3.58	4.41	0.022
t_{as}	Address Setup Time	1.05	0.53	0.53	-
t_{ah}	Address Hold Time	1.05	1.05	1.05	-
t_w	Write Pulse Width	1.89	2.52	3.43	-
t_{ac}	Write-Thru Access - data	2.22	2.46	2.55	0.022
t_{ac2}	Write-Thru Access - CSN	1.91	2.48	2.97	0.022
t_{wr}	WEN Recovery to CSN	0.53	0.53	0.53	
t_{ds}	Data Setup Time	0.53	0.63	0.73	-
t_{dh}	Data Hold Time	1.22	1.22	1.57	-
t_{lz}	OEN to Low Impedance	0.64	0.64	0.63	0.022
t_{hz}	OEN to High Impedance	1.73	1.73	1.73	-
t_h	Data Valid after CSN	0.36	0.86	0.86	-

AC CHARACTERISTICS (V_{DD} = 5V, T_A = 25°C)

SPRAM GENERATOR 256 words x 8 bits

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading ns/SL
		mux = 2	mux = 4	mux = 8	
t_{pr}	Precharge Time	4.05	3.64	3.84	-
t_{aa}	Address Access Time	4.61	4.29	4.65	0.022
t_{as}	Address Setup Time	2.10	1.05	1.05	-
t_{ah}	Address Hold Time	2.10	1.58	1.05	-
t_w	Write Pulse Width	2.44	2.62	3.36	-
t_{ac}	Write-Thru Access - data	3.73	3.19	3.10	0.022
t_{ac2}	Write-Thru Access - CSN	2.28	2.45	2.93	0.022
t_{wr}	WEN Recovery to CSN	0.53	0.53	0.53	
t_{ds}	Data Setup Time	0.63	0.73	0.84	-
t_{dh}	Data Hold Time	1.73	1.52	1.72	-
t_{lz}	OEN to Low Impedance	0.57	0.56	0.56	0.022
t_{hz}	OEN to High Impedance	1.27	1.27	1.27	-
t_h	Data Valid after CSN	0.63	0.63	0.63	-

SPRAM 1024 words x 8 bits

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading ns/SL
		mux = 2	mux = 4	mux = 8	
t_{pr}	Precharge Time	-	-	4.81	-
t_{aa}	Address Access Time	-	-	6.26	0.022
t_{as}	Address Setup Time	-	-	2.10	-
t_{ah}	Address Hold Time	-	-	2.10	-
t_w	Write Pulse Width	-	-	3.76	-
t_{ac}	Write-Thru Access - data	-	-	4.30	0.022
t_{ac2}	Write-Thru Access - CSN	-	-	3.10	0.022
t_{wr}	WEN Recovery to CSN	-	-	0.53	
t_{ds}	Data Setup Time	-	-	0.84	-
t_{dh}	Data Hold Time	-	-	2.28	-
t_{lz}	OEN to Low Impedance	-	-	0.56	0.022
t_{hz}	OEN to High Impedance	-	-	1.27	-
t_h	Data Valid after CSN	-	-	0.63	-

DUAL PORT RAM GENERATOR

DESCRIPTION

The ISB24000 Series Dual Port RAM generator builds a static dual port RAM, each RAM cell having a ten transistor implementation. Standard read and write operations are supported.

FEATURES

- Fully static, asynchronous read operation.
- Fully static, clocked write port implementation.
- 1 READ port and 1 WRITE port.
- Total memory capacity (words x bits) 4K bits.
- Word range from 8 to 1024 words.
- Bit range from 1 to 64 bits in single bit increments limited by mux selection.
- Selectable aspect ratio by use of the Row/Column multiplexing.
- Row/Column multiplexing Factor 1, 2, 4, 8 or 16.
- Separate data input and output buses.
- Tristate double drive output buffers.
- RAM supports write-thru when read address equals write address.

RAM OPERATION

The dual port RAM uses a fully static asynchronous read architecture. A read cycle is defined as the time between 2 consecutive read address transitions. No clock is required for reading and the read operations are completely asynchronous with respect to the write operations.

A RAM write cycle is defined as the time between two consecutive falling edges of the WEN (write enable) signal. When WEN is low the RAM is selected and the write operation active. When WEN is high the RAM is deselected and is precharged ready for the next write operation.

When the read address and write address point to the same location and WEN is active, a write thru operation is performed. Data on the datain port will write thru the RAM bits and come out on the dataout ports if the outputs are enabled.

The dataout bus is controlled by OEN (output enable). When OEN is active the dataout bus is low impedance. When OEN is high the dataout bus is tristated. This action is independent of any other operation.NOTE that it is the user's responsibility to make sure all tristate buses on chip are controlled, i.e. not floating. A floating bus will cause high Icc standby current and possible operational problems in other parts of the circuit.

For correct functionality of the RAM during a write operation, the write address signals must be valid for time 'tas' before WEN is enabled and must remain stable for time 'tah' after WEN goes high. Additionally, it is important to note that in order to ensure correct functionality, the WEN signal must be toggled (1-0-1) for each individual write operation to allow for precharge between successive write cycles.

Read Cycle

A read cycle is initiated by any read address transition, valid data will be available after time 'taa'. The RAM is always performing a read operation even when the data outputs are not enabled. See timing diagram, page 16.

Note: In non power of 2 RAM configurations it is possible to select non-existent row addresses and put the RAM into a high power consumption mode. It is up to the user to supply only valid addresses to the RAM core. Invalid addresses are addresses greater than the maximum word count but less than the next power of 2 address boundary.

Write Cycle

A write cycle is initiated by the falling edge of WEN and ends when WEN returns high (WEN controlled). During a write operation, input data must be valid before the rising edge of WEN and must be held for a minimum hold time after the rising edge of WEN. The datain bus may change during WEN active as long as the setup and hold times are satisfied. The status of OEN does not effect either the write or write thru operations, only the impedance of the output bus. See figure 2 for timing diagram.

Note: In non power of 2 RAM configurations it is permissible to write to non-existent addresses. The RAM will not draw high current. This operation is the same as no operation.

Write thru Operation

The DPRAM design supports a write-thru feature. Write thru is defined as the ability to write thru the RAM cells and have the data show up on the dataout bus. This condition will occur when the read and write addresses are equal. The status of OEN does not effect write-thru, it only controls the impedance of the output bus. Since the read operation is asynchronous with respect to the write, one can enter the write-thru condition in the middle of a write operation with no problems. See figure 3 for timing diagram.

ROW/COLUMN MULTIPLEXING

The MUX parameter is user programmable to allow the user varying internal RAM architecture options. Specifically, the parameter will be used to determine the row and column decoding scheme for the RAM bit array. The value chosen will determine how many words of requested bit width are to be defined on each row of memory array. Due to the direct implication on RAM architecture, the MUX parameter will affect the aspect ratio (width/height), performance, and power consumption of the targeted RAM. The automatic datasheet generators within each SGS-THOMSON design kit allows investigation of each alternative MUX option.

Note. All limits regarding the choice of MUX factor are outlined in the CONSTRAINTS section

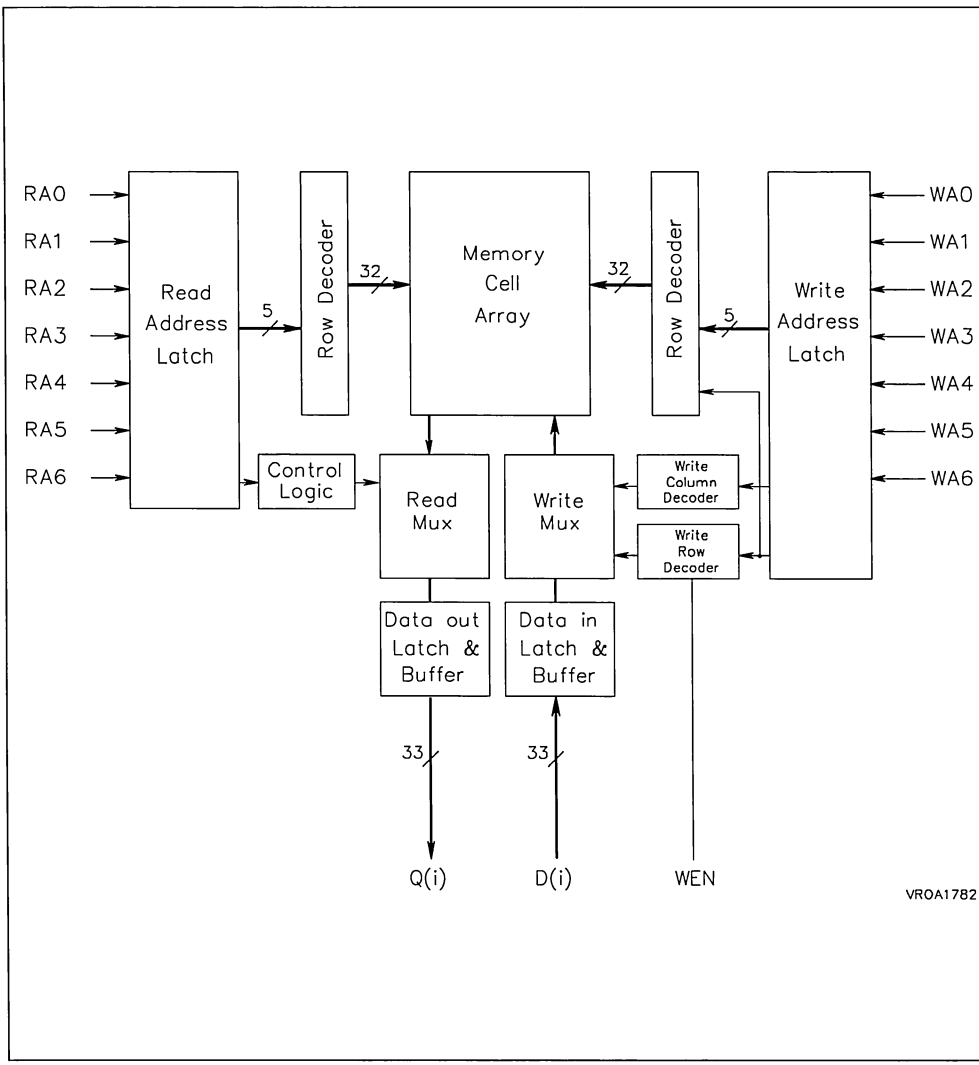
MINIMUM WORD ORGANISATION

As described in the constraints section (page 14) the user defined words parameter must be a multiple of the chosen MUX factor. The RAM bit array is symmetrical in nature with an equal number of words on each row. Hence, the user is provided full access to all ram array bits through complete bit array decoding. The generator provided in each SGS-THOMSON design kit includes a rules checker to ensure the generation of a ram which is compliant with this constraint, and which provides the user with the maximum word depth available from the resultant ram bit array.

Example :	User Defined	Generated
N° of words	33	36
N° of bits	9	9
MUX option	4	4

The resulting generated RAM would be defined with a word width of 36 instead of 33 in order to provide full access to the compiled symmetrical RAM bit array.

FUNCTIONAL BLOCK DIAGRAM



CONSTRAINTS

Minimum size available	: 8 bits	
Maximum size available	: 4K bits	
Maximum load on any output	: 82 SL	
Input load	: WEN = 2 SL	Write Enable
	OEN = 1 SL	Output Enable
	RA[i] = 3 SL	Read Address
	WA[i] = 3 SL	Write Address
	D[n] = 2 SL	Datain
Output Load	: Q[n] = 0.75 SL	Dataout

Possible DPRAM configurations are limited by the number of rows and columns generated as follows:

Number of columns : cols = mux x bits
Minimum number of cols = 1
Maximum number of cols = 64

Number of rows : rows = words / mux
Minimum number of rows = 8
Maximum number of rows = 64

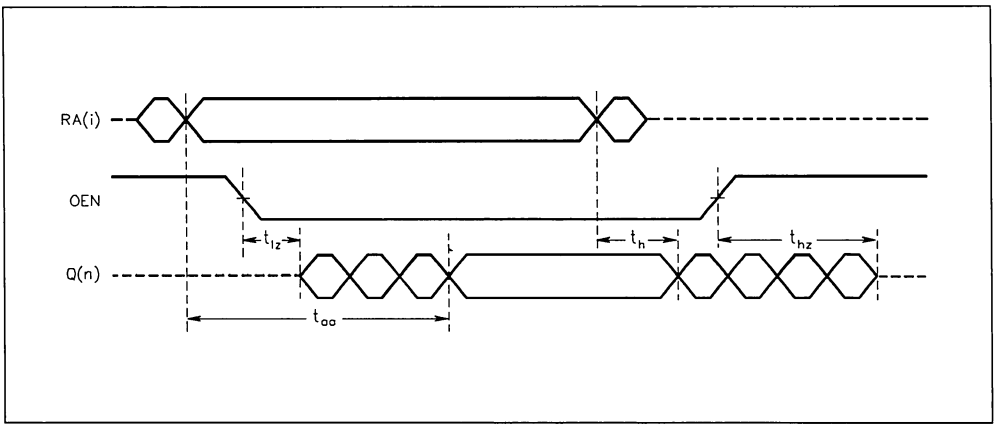
Mux Option	Max Bit	Max Word
1	64	64
2	32	128
4	16	256
8	8	512
16	4	1024

PERFORMANCE AREA AND POWER CONSUMPTION ESTIMATIONS

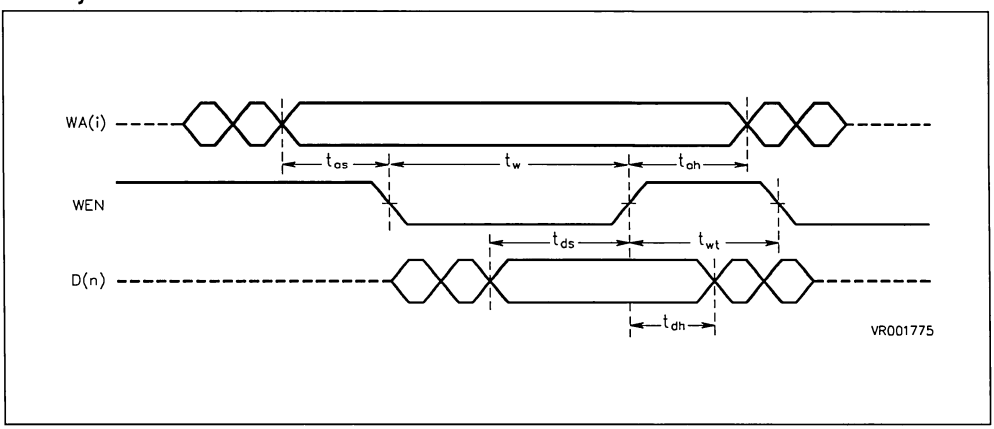
For specific performance, power, and area estimations please refer to the ISB24000 SERIES DPRAM Generator available with each SGS-THOMSON design kit or at your local design center.

TIMING DIAGRAMS

Read Cycle



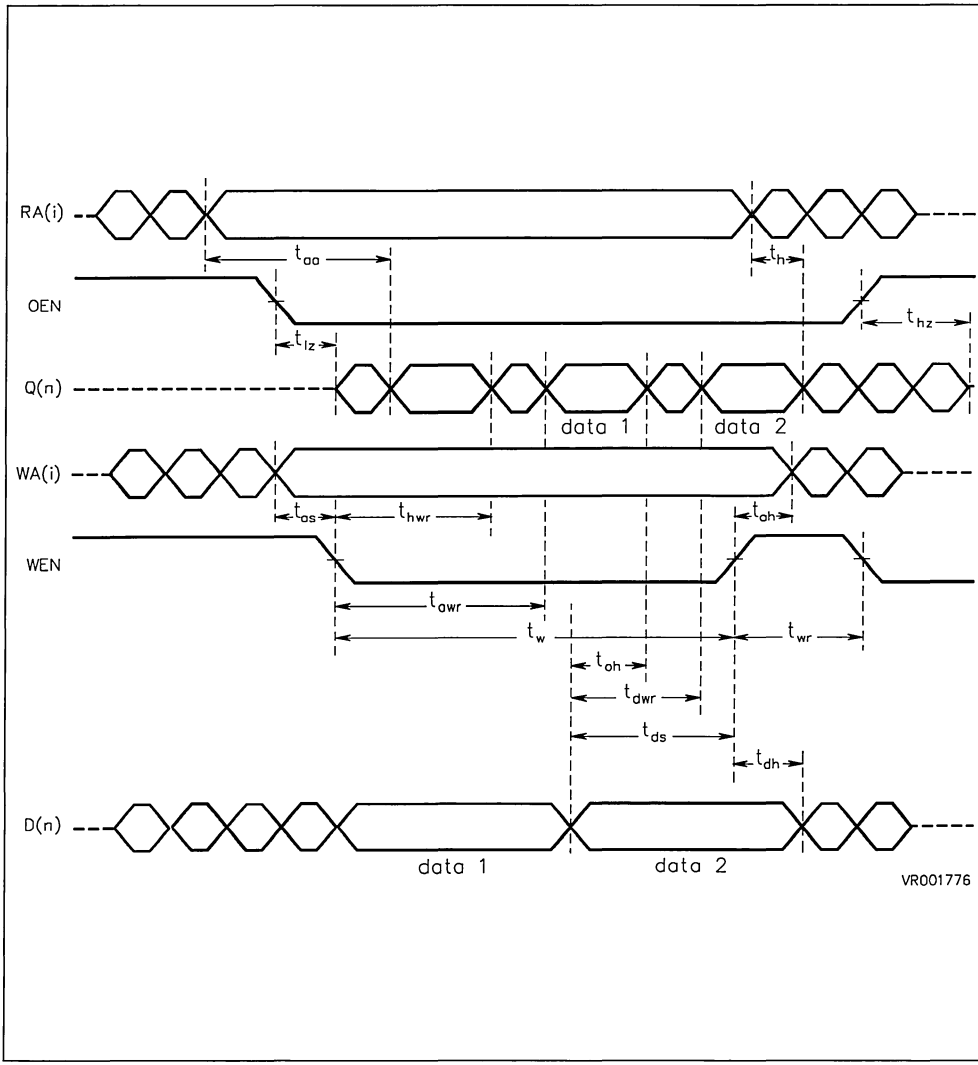
Write Cycle



Note: For the simulation models 'twr' is checked by other parameters.

TIMING DIAGRAMS

Write-thru Mode



Note: For the simulation models 'toh' is set to 'thwr'. For the simulation models 'tdwr' is set to 'tawr' For the simulation models 'twr' is checked by other parameters

AC CHARACTERISTICS (V_{DD} = 5V, T_A = 25°C)

DPRAM 32 words x 8 bits

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading ns/SL
		mux = 2	mux = 4	mux = 8	
t_{aa}	Address Access Time	4.20	4.34	5.69	0.026
t_{as}	Address SetupTime	0.55	0.20	0.20	-
t_{ah}	Address Hold Time	1.15	1.05	1.05	-
t_w	WEN Pulse Width Low	2.21	2.61	3.49	-
t_{ds}	Datain SetupTime	1.46	1.88	2.89	-
t_{dh}	Datain Hold Time	1.27	1.12	1.05	-
t_{lz}	OEN to Low Impedance	1.73	1.82	2.02	-
t_{hz}	OEN to High Impedance	1.03	1.12	1.32	-
t_h	Data Valid	2.57	2.65	3.67	-
t_{hwr}	Data Valid	3.99	4.65	6.44	-
t_{awr}	Write Thru Access Time	5.02	5.62	7.37	0.026

DPRAM 32 words x 16 bits

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading ns/SL
		mux = 2	mux = 4	mux = 8	
t_{aa}	Address Access Time	5.06	6.05	-	0.026
t_{as}	Address SetupTime	0.55	0.20	-	-
t_{ah}	Address Hold Time	1.15	1.05	-	-
t_w	WEN Pulse Width Low	2.67	3.52	-	-
t_{ds}	Datain SetupTime	2.00	2.95	-	-
t_{dh}	Datain Hold Time	1.19	1.05	-	-
t_{lz}	OEN to Low Impedance	2.06	2.25	-	-
t_{hz}	OEN to High Impedance	1.36	1.55	-	-
t_h	Data Valid	3.23	3.96	-	-
t_{hwr}	Data Valid	4.96	6.59	-	-
t_{awr}	Write Thru Access Time	5.99	7.56	-	0.026

AC CHARACTERISTICS (V_{DD} = 5V, T_A = 25°C)

DPRAM 128 words x 8 bits

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading ns/SL
		mux = 2	mux = 4	mux = 8	
t_{aa}	Address Access Time	8.54	6.50	6.77	0.026
t_{as}	Address SetupTime	2.35	1.35	0.55	-
t_{ah}	Address Hold Time	1.40	1.25	1.15	-
t_w	WEN Pulse Width Low	2.60	2.80	3.58	-
t_{ds}	Datain SetupTime	2.16	2.23	3.06	-
t_{dh}	Datain Hold Time	1.66	1.32	1.15	-
t_{lz}	OEN to Low Impedance	1.73	1.82	2.02	-
t_{hz}	OEN to High Impedance	1.03	1.12	1.32	-
t_h	Data Valid	6.05	4.39	4.54	-
t_{hwr}	Data Valid	5.85	5.58	6.90	-
t_{awr}	Write Thru Access Time	7.26	6.74	7.93	0.026

DPRAM 512 words x 8 bits

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading ns/SL
		mux = 2	mux = 4	mux = 8	
t_{aa}	Address Access Time	-	-	11.11	0.026
t_{as}	Address SetupTime	-	-	2.35	-
t_{ah}	Address Hold Time	-	-	1.40	-
t_w	WEN Pulse Width Low	-	-	3.97	-
t_{ds}	Datain SetupTime	-	-	3.76	-
t_{dh}	Datain Hold Time	-	-	1.42	-
t_{lz}	OEN to Low Impedance	-	-	2.02	-
t_{hz}	OEN to High Impedance	-	-	1.32	-
t_h	Data Valid	-	-	8.02	-
t_{hwr}	Data Valid	-	-	8.76	-
t_{awr}	Write Thru Access Time	-	-	10.17	0.026

ROM GENERATOR

DESCRIPTION

The ISB24000 Series ROM builds a static, contact programmable Read Only Memory.

FEATURES

- Fully static, synchronous operation.
- Total memory capacity (words x bits) up to 16K bits.
- Words range from 32 to 2048.
- Bit range 1 to 32 bits wide (limited conditions).
- Selectable aspect ratio (4, 8 and 16 multiplexing factors available).
- Maximum density of 7000 bits/mm^2.
- Fast access time.

ROM OPERATION

The ROM architecture is synchronous with timing dependent on the chip select (CSN) input. Address lines must be set up before CSN is enabled (positive edge). The read is terminated by CSN disabling the ROM (negative edge). The arrival of a new address during the low pulse of CSN generates a spurious output. During deselection (CSN high), the ROM is precharged.The output is set in a high impedance mode by OEN high. If the outputs are enabled during deselection (OEN low and CSN high), all the bits in the output bus are forced high.

Incomplete decoding is allowed, i.e. a number of locations can be generated that is not a power of two. In case a location is addressed that is not physically present, the ROM outputs the precharged value (the high level logic model, however, will consider such an operation illegal and generate a spurious output).

WORD PARAMETER

The architecture imposes that every physical row of the ROM is completely built. The increment of words is possible in steps given by the aspect ratio selector MUX multiplied by a layout dependent constant ROWSTEP (which is the number of row drivers present in each row decoders' leaf cell).

For instance, if the MUX is selected as 8, every physical row of the ROM contains 8 words, each NBITS wide, multiplexed into the NBITS wide output bus. If two drivers are laid out together as a single leaf cell (ROWSTEP = 2) the words can be incremented in steps of 16.

Words	Multiplex Factor	Step(1)	Row Drivers
64	4	8	16
128	8	16	16
50(2)	4	8	14
100(3)	8	16	14

Notes: 1. Rowsteps in increments of 2

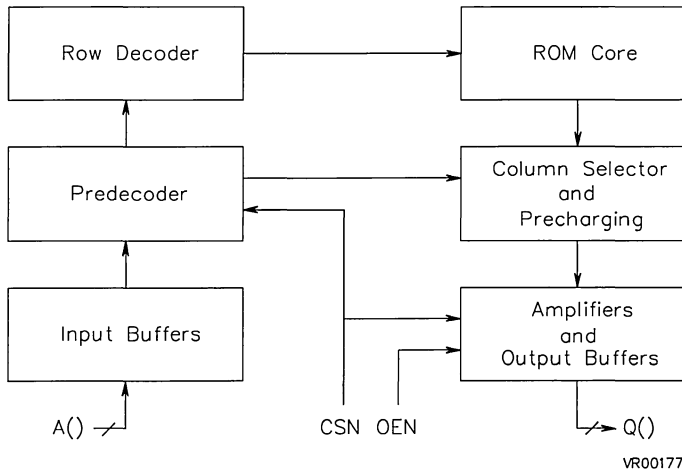
2. Words rounded up to 56

3. Words rounded up to 112.

The rule checker of the generator will automatically round off the number of words to the minimum allowed organisation, if an illegal choice is made.

If the selected ROM size is such that 8 row drivers are present, one extra address bit is generated that MUST be tied to ground.

FUNCTIONAL BLOCK DIAGRAM



WORDS PARAMETER

Words	Multiplex Factor	Row Drivers	Address Pins	Ground Pin
32	4	8	A0 to A5	A5
64	8	8	A0 to A6	A6
128	16	8	A0 to A7	A7

NBITS PARAMETER

The NBITS parameter defines how many bits are contained in each address location. Up to 32 bits can be selected. The bit limit of any particular organization is highly limited by the MUX parameter.

ROW/COLUMN MULTIPLEXING

The MUX selector allows the user to specify the aspect ratio of the ROM and hence tailor it optimally to the desired floor plan. The higher the value of MUX all other parameters frozen, the larger the memory bank will grow in the column direction and shrink in the row direction.

CONSTRAINTS

WORDS	32 thru 2k	number of memory locations physically accessible
NBITS	1 thru 32	number of bits per word
MUX	4, 8, 16	number of words for each row of the memory bank

ROM Input load (SL)				Max. Output Drive (SL)
Q0 - Qn	A0 - Ak	CSN	OEN	
1[1]	3	4	4	50

Note 1. tristate mode

Possible ROM configurations are limited by the number of rows and columns as follows:

Number of cols = MUX * NBITS (max 128)

Number of rows = WORDS / MUX (max 128)

In general the following limits apply for a given MUX factor:

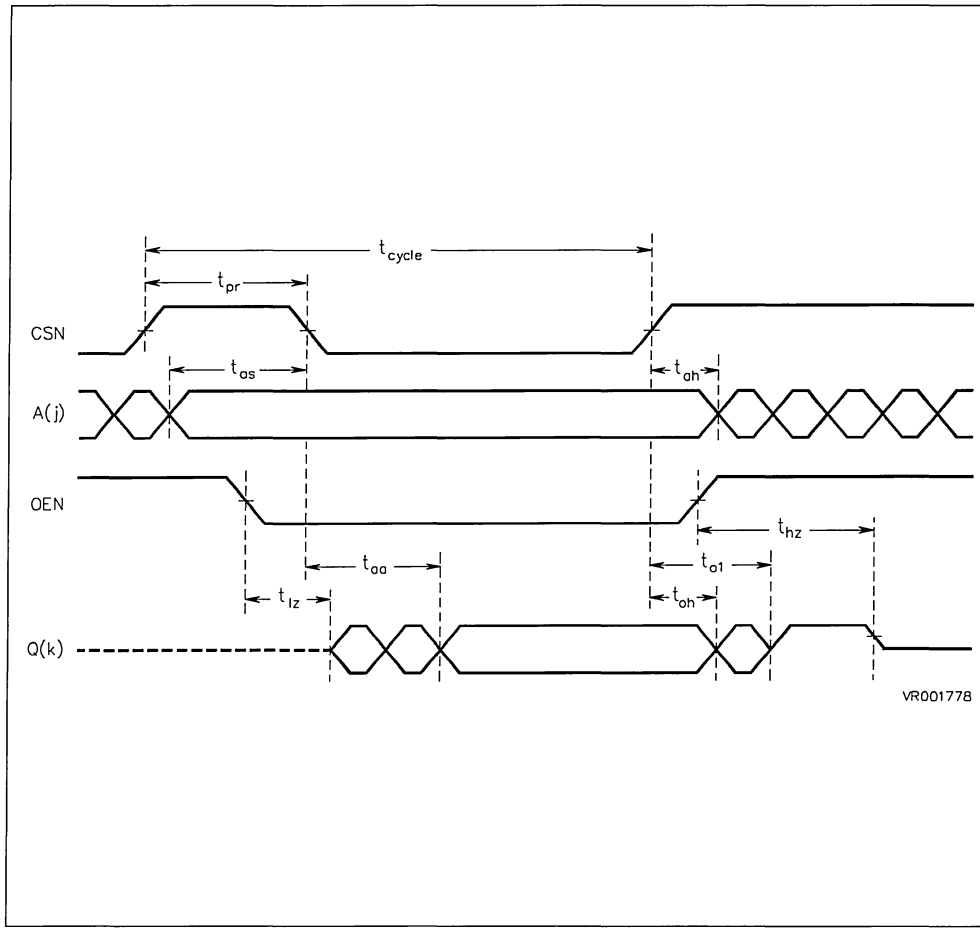
Multiplex Factor	Maximum NBits	Maximum Words	Column Decoder Bits	Row Decoder Bits (max)
4	32	512	A0, A1	7
8	16	1024	A0,A1,A2	7
16	8	2048	A0,A1,A2,A3	7

The least significant address bits are always used to form the decoder controlling the column multiplexer.

PERFORMANCE, AREA AND POWER CONSUMPTION ESTIMATIONS

For specific performance, power, and area estimations please refer to the ISB24000 SERIES ROM Generator available with each SGS-THOMSON design kit or at your local design center.

TIMING DIAGRAMS



AC CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C)

ROM GENERATOR 256 words x 16 bit

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading (ns/SL)
		mux = 4	mux = 8	mux = 16	
t_{pr}	Minimum Precharge Time	2.3	2.6	-	-
t_{aa}	Maximum Access Time	3.6	3.9	-	0.02
t_{as}	Minimum Address SetupTime	1.3	1.7	-	-
t_{ah}	Minimum Address Hold Time	0.0	0.0	-	-
t_{lz}	Maximum OEN to Low Impedance	0.1	0.1	-	-
t_{hz}	Maximum OEN to High Impedance	1.2	1.2	-	-
t_{o1}	Maximum CSN to Data High	2.8	3.3	-	0.02
t_{oh}	Minimum Data Hold After CSN	0.5	0.5	-	-

ROM GENERATOR 512 words x 8 bit

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading (ns/SL)
		mux = 4	mux = 8	mux = 16	
t_{pr}	Minimum Precharge Time	2.8	2.5	2.8	-
t_{aa}	Maximum Access Time	4.2	3.8	4.4	0.02
t_{as}	Minimum Address SetupTime	2.3	1.3	1.7	-
t_{ah}	Minimum Address Hold Time	0.0	0.0	0.0	-
t_{lz}	Maximum OEN to Low Impedance	0.1	0.1	0.1	-
t_{hz}	Maximum OEN to High Impedance	0.8	0.8	0.8	-
t_{o1}	Maximum CSN to Data High	3.5	3.0	3.8	0.02
t_{oh}	Minimum Data Hold After CSN	0.5	0.5	0.5	-

A.C. CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C)

ROM GENERATOR 512 words x 32 bit

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading (ns/SL)
		mux = 4	mux = 8	mux = 16	
t_{pr}	Minimum Precharge Time	3.6	-	-	-
t_{aa}	Maximum Access Time	5.0	-	-	0.02
t_{as}	Minimum Address SetupTime	2.3	-	-	-
t_{ah}	Minimum Address Hold Time	0.0	-	-	-
t_{lz}	Maximum OEN to Low Impedance	0.1	-	-	-
t_{hz}	Maximum OEN to High Impedance	1.9	-	-	-
t_{o1}	Maximum CSN to Data High	4.1	-	-	0.02
t_{oh}	MinimumData Hold After CSN	0.5	-	-	-

ROM GENERATOR 2048 words x 8 bit

Symbol	Parameter	Intrinsic Delay (ns)			Sensitivity to Loading (ns/SL)
		mux = 4	mux = 8	mux = 16	
t_{pr}	Minimum Precharge Time	-	-	4.0	-
t_{aa}	Maximum Access Time	-	-	5.8	0.02
t_{as}	Minimum Address SetupTime	-	-	2.3	-
t_{ah}	Minimum Address Hold Time	-	-	0.0	-
t_{lz}	Maximum OEN to Low Impedance	-	-	0.1	-
t_{hz}	Maximum OEN to High Impedance	-	-	0.8	-
t_{o1}	Maximum CSN to Data High	-	-	4.8	0.02
t_{oh}	MinimumData Hold After CSN	-	-	0.5	-

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