VIDEO PRODUCTS
VOL. 1
SIGNAL PROCESSING

DATABOOK

1st EDITION

SGS-THOMSON MICROELECTRONICS

RYSTON
ELECTRONICS
spol. s r.o.
Na hřebenech II 1062
147 00 Praha 4

000555
RYSTON Electronics

VIDEO PRODUCTS VOL. 1 SIGNAL PROCESSING

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AUGUST 1991

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED 555

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

SGS-THOMSON's dedicated video product range is now so extensive that it has been necessary to divide the databook into two volumes: one for power devices and graphic circuits and one for signal devices. Application notes for video products have been gathered together in the video products Application Manual.

Volume 1, Signal Processing Products, covers chroma and video ICs, single-chip processors, video switch matrices and other signal level parts. In this area the company specializes in offering complete solutions all of the ICs needed for a specific TV or monitor chassis type and gives special attention to the basic solutions. Much of the knowhow in this field has been gained in the demanding Asia/Pacific market for the cost effective aspect, and in western Europe for PAL/SECAM multistandard design, placing SGS-THOMSON in a very strong position in the emergent East European market the new frontier in consumer electronics.

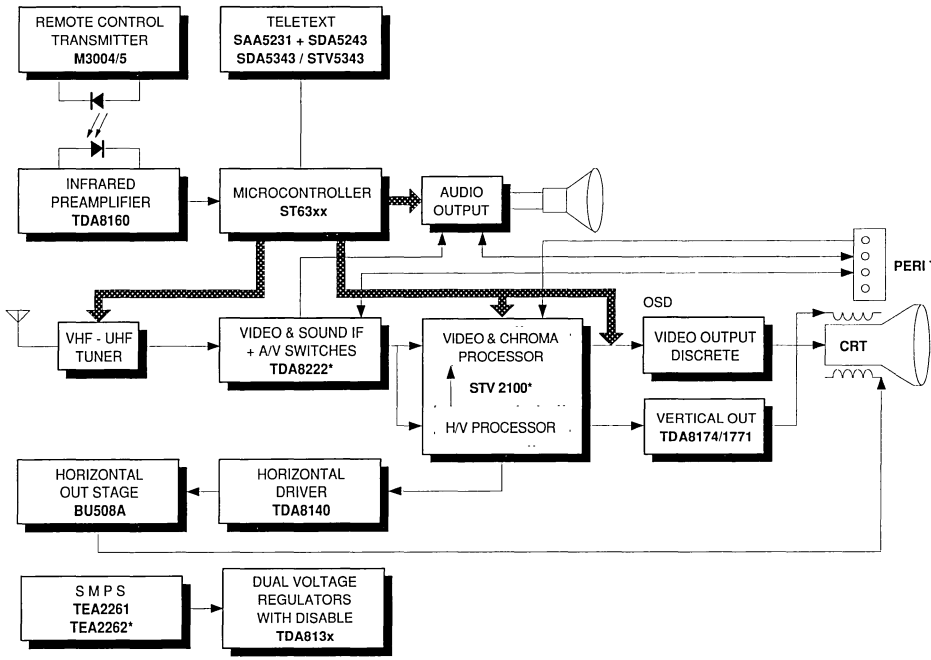
Volume 2, Power & Graphics Products, covers power ICs such as deflection boosters and sound channels, plus other ICs for graphics monitor deflection applications. In the monitor market SGS-THOMSON is the recognized world leader; in fact today 7 out of 10 monitors produced in the world include SGS-THOMSON ICs. Power ICs in general are a traditional specialty of the company, which began producing monolithic power amplifiers in the 60's and has remained at the forefront of power technology development ever since.

With these two volumes SGS-THOMSON Microelectronics proposes a dedicated video product range that satisfies virtually every need in television, monitor, VCR and related applications. And if you don't find the product you are looking for in these volumes contact the nearest SGS-THOMSON office; it may be that the product you want is included in other books covering micros, memories, standard ICs or discretes.

The Video Products Application Manual is part of the comprehensive technical support offered by SGS-THOMSON's Video Division to make application design fast and productive. This support also includes PC design aids and evaluation boards.

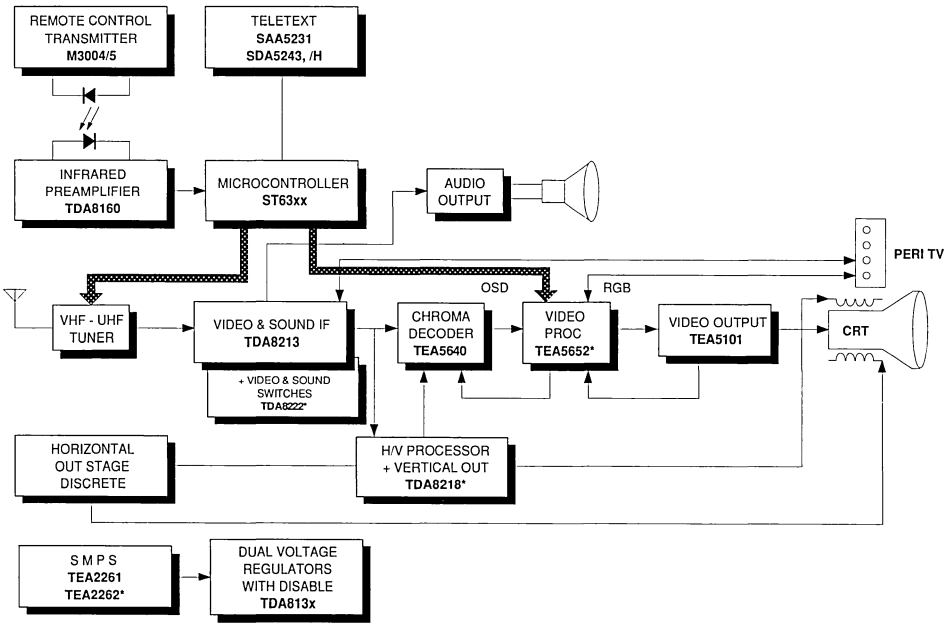
TYPICAL CONFIGURATION BLOCK DIAGRAMS

PAL CTV WITH PERI-TV PLUG



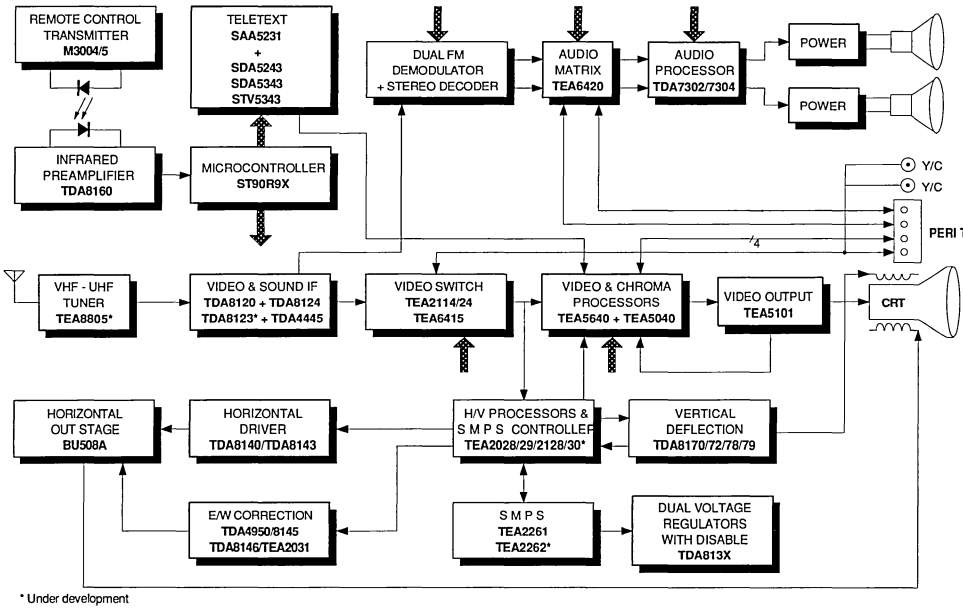
* Under development

PAL/SECAM MONOSOUND CHASSIS



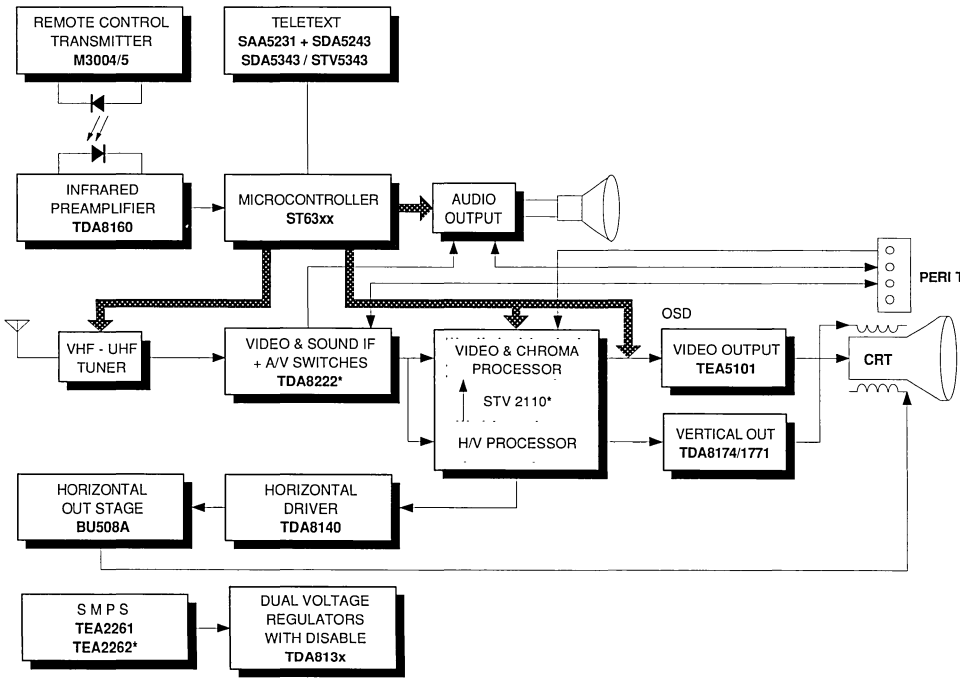
* Under development

MULTISTANDARD MID-RANGE CTV



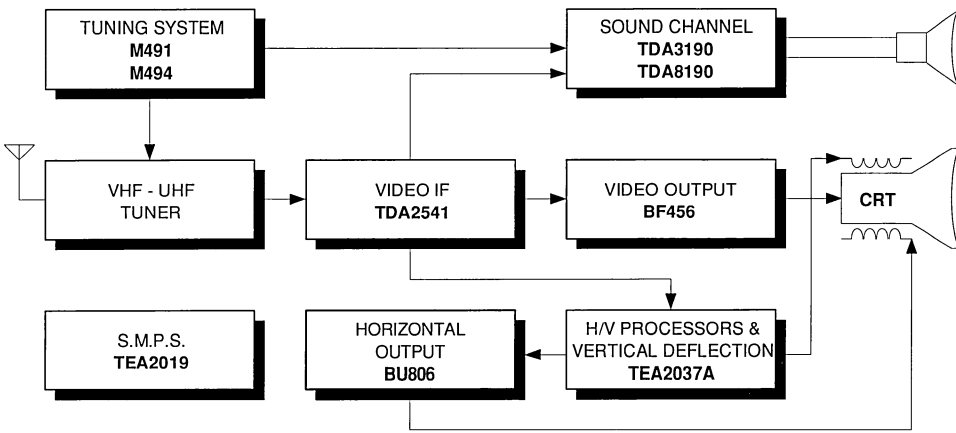
* Under development

PAL/SECAM CTV WITH PERI-TV PLUG

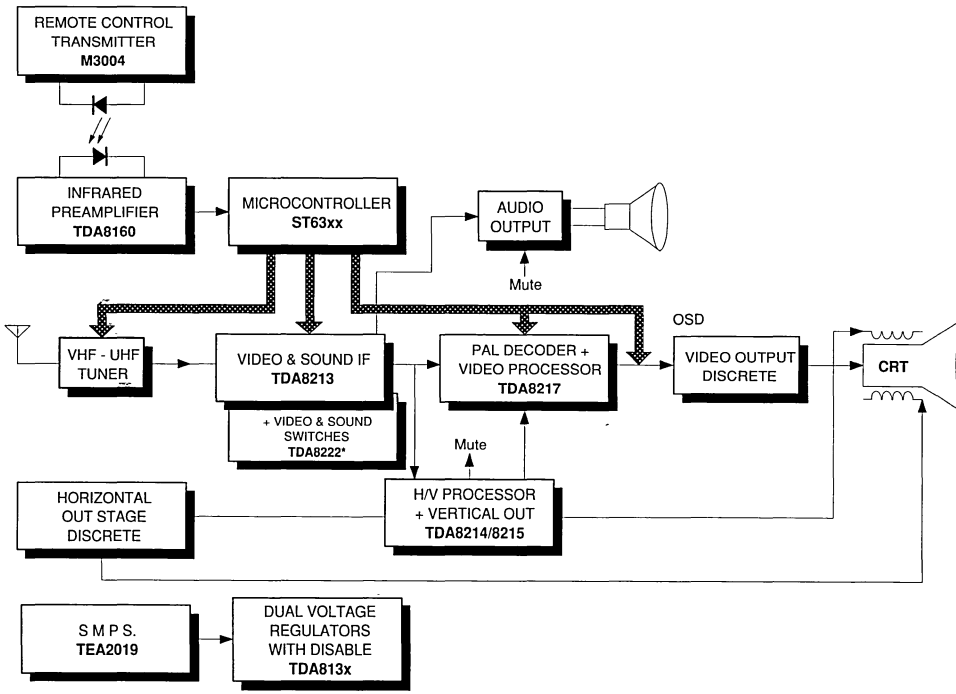


* Under development

BLACK & WHITE TV

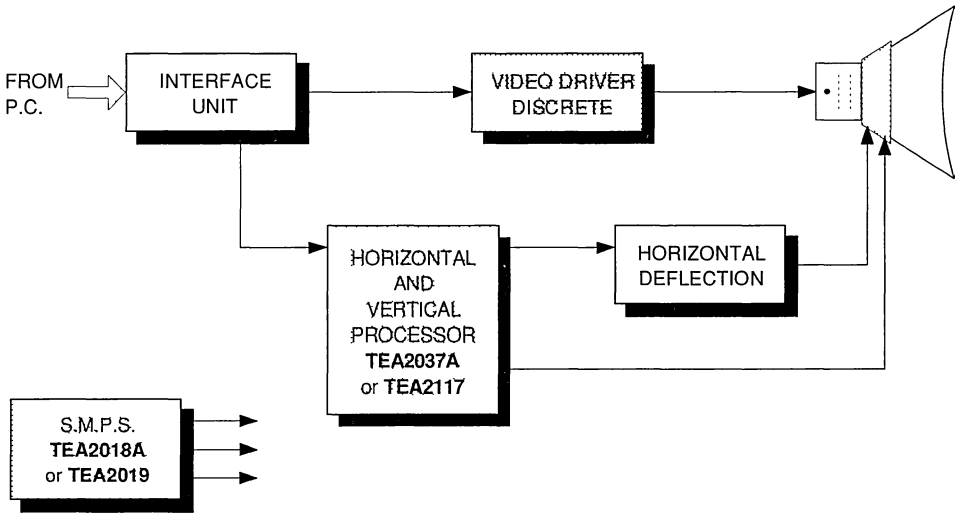


LOW-COST PAL CTV

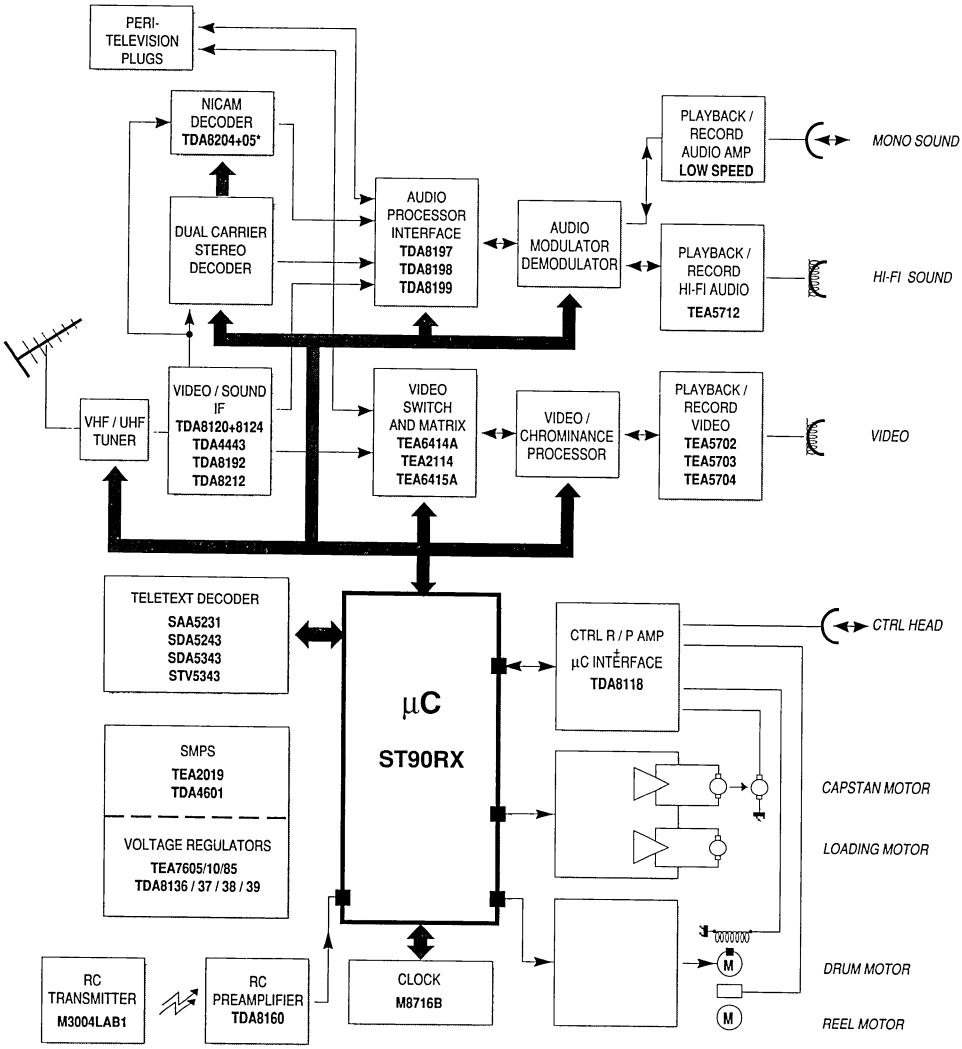


* Under development

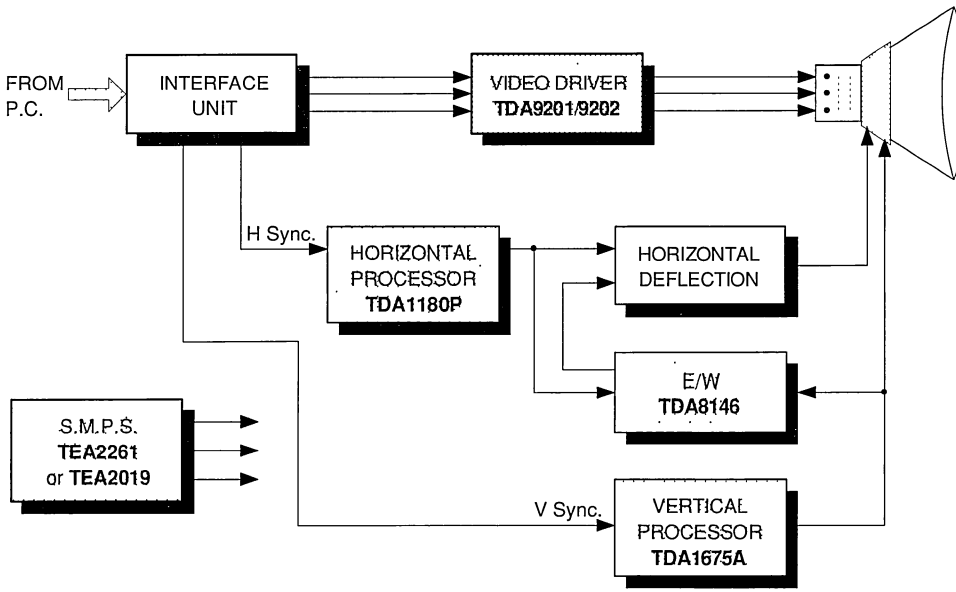
MONOCHROME LOW-COST MONITOR



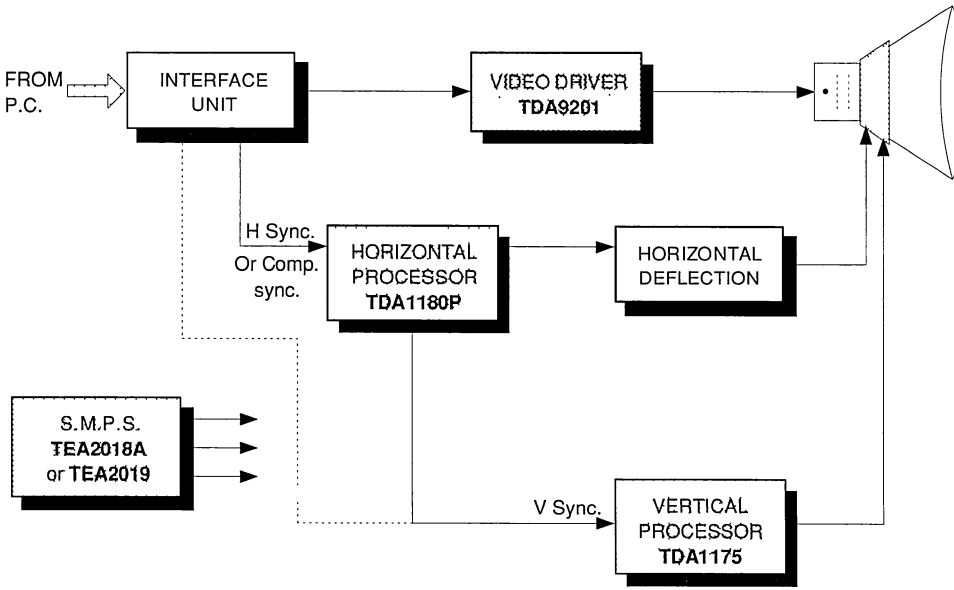
MID- & HIGH-END VCR



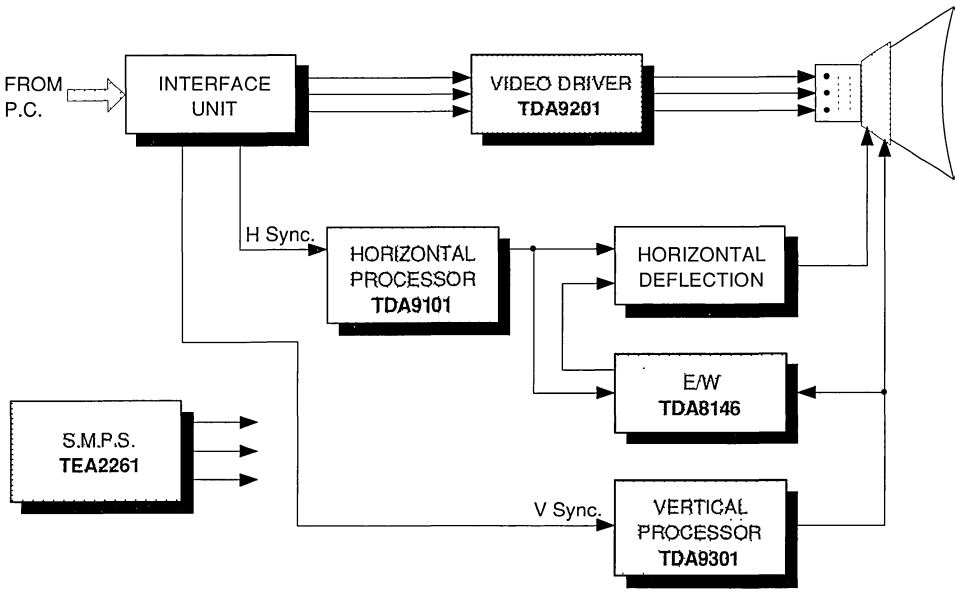
MID-RANGE COLOR MONITOR



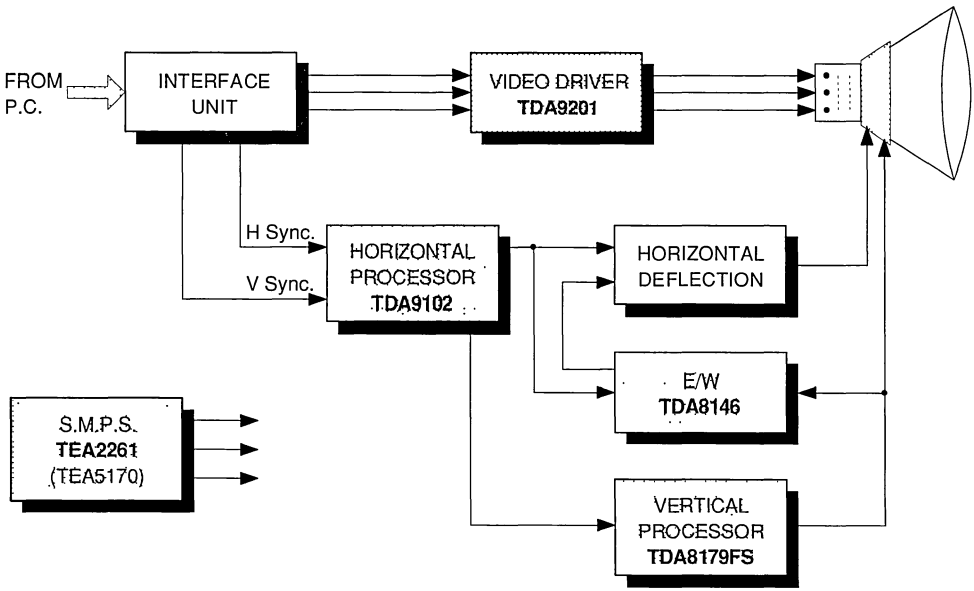
MONOCHROME LOW-COST MONITOR



SELF-ADAPTIVE MULTIFREQUENCY COLOR MONITORS



MEDIUM HIGH-END COLOR MONITOR



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SELECTION GUIDE

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in column "DB"

SGS-THOMSON DATABOOKS

DB		ORDER CODE
a	4 BIT MCU FAMILY ET9400	DBET9400ST/1
b	8 BIT MCU FAMILIES EF6801/04/05	DB68XXST/1
c	16 BIT MPUs & ASSOCIATED PERIPHERALS	DB6800ST/1
d	AUDIO POWER and PROCESSING ICs	DBAUDIOPROST/1
e	AUTOMOTIVE PRODUCTS	DBAMOTIVEST/1
f	ANALOG CELLS AND ARRAYS	DBANACA/1090
g	CB12000 SERIES STANDARD CELLS	DBCB12ST/1
h	CB12000 SERIES STANDARD CELLS MODULE GENERATORS	DBCB12GEN/1
i	CMOS B SERIES	DBCMOSBST/1
j	CMOS LINEAR	BKCMOSLIN/0490
k	DATACOM PRODUCTS	DBDATACOMST/1
l	HIGH SPEED CMOS	DBHSCMOSST/1
m	IMAGE PROCESSING	DBIMAGEPROST/1
n	INDUSTRIAL and COMPUTER PERIPHERAL ICs	DBINDCOMPST/1
o	INDUSTRY STANDARD ANALOG ICs	DBSTANDANAST/1
p	ISB12000 SERIES CONTINUOUS ARRAYS	DBISB12/1
q	ISB9000 SERIES CHANNELLESS LOGIC ARRAYS	DBISB9/2
r	ISB18000 SERIES CONTINUOS ARRAYS	DBISB18/1
s	LINE CARD ICs	DBLINCARDST/1
t	LOW POWER SCHOTTKY TTL ICs	DBLPSST/1
u	MACROFUNCTION LIBRARY DATABOOK	DBMACRO/1
v	MODEM	DBMODEMST/1
w	NON-VOLATILE MEMORIES	DBNVMST/1
y	POWER BIPOLAR TRANSISTORS	DBBIPTRANST/1
z	POWER MODULES	DBPOMODULEST/1
aa	POWER MOS DEVICES	DBPOWERMOSST/1
ab	PROTECTION DEVICES	DBPROTECST/1
ac	RF & MICROWAVE POWER TRANSISTORS	DBRFST/1
ad	SMALL SIGNAL TRANSISTORS	DBSMSIGST/1
ae	STANDARD CELL LIBRARY	DASTACELL/2
af	STATIC RAMs	DBSRAM/1
ag	ST8 MCU FAMILY	SGST8ST/1
ah	TELEPHONE SET ICs	DBTELSETST/1
ai	THE GRAPHICS DATABOOK	72TRN20400
aj	THE L4970 SWITCHING REGULATOR IC FAMILY	BKL4970FA/0489
ak	THE TRANSPUTER DATABOOK	72TRN20300
al	THE TRANSPUTER DEVELOPMENT AND iq SYSTEMS DATABOOK	72TRN21900
am	THE T9000 TRANSPUTER	DBTRANSPST/1
an	THYRISTORS & TRIACS	DBTHYTRIACST/1
ao	VIDEO PRODUCT POWER & GRAPHICS	DBPOMGRAST/1
ap	Z8 MCU FAMILY	BKZ8SELEC/0289
aq	Z80 MICROPROCESSORS FAMILY	DBZ80ST/1
ar	ZENER, SCHOTTKY & RECTIFIER DIODES	DBDIODEST/1
*	NOT INCLUDED IN CURRENT DATABOOKS, CONTACT YOUR NEAREST SGS-THOMSON SALES OFFICE	

DEFLECTION - ICs

VERTICAL DEFLECTION

Type Number	Description	Packages	Page/DB
TDA1170D	Vertical Deflection System	DIP16	ao
TDA1170N	Vertical Deflection System	FINDIP	ao
TDA1170S	Vertical Deflection System	FINDIP	ao
TDA1175	Low-noise Vertical Deflection System	FINDIP	ao
TDA1670A	Vertical Deflection System	MULTIWATT15	ao
TDA1675A	Vertical Deflection System	MULTIWATT15	ao
TDA1770A	Vertical Deflection System	DIP20	ao
TDA1771	Ramp Generator & Vertical Output	SIP10	ao
TDA1872A	Vertical Deflection System	MULTIWATT15	ao
TDA2170	Vertical Deflection Output Stage	MULTIWATT11	ao
TDA2270	Vertical Deflection Output Stage	DIP16	ao
TDA8170	Vertical Deflection Output Circuit	HEPTAWATT	ao
TDA8170A	Vertical Deflection Output Circuit	HEPTAWATT	ao
TDA8172	Vertical Deflection Output Circuit	HEPTAWATT	ao
TDA8172A	Vertical Deflection Output Circuit	HEPTAWATT	ao
TDA8173	Vertical Deflection Output Circuit	DIP16	ao
TDA8174	Ramp Generator & Vertical Output	MULTIWATT11	ao
TDA8175	Vertical Deflection Output Circuit	HEPTAWATT	ao
TDA8176	Vertical Deflection System	MULTIWATT15	ao
TDA8178FS	Vertical Deflection Output Circuit	HEPTAWATT	ao
TDA8178S	Vertical Deflection Output Circuit	HEPTAWATT	ao
TDA8179FS	Vertical Deflection Output Circuit	HEPTAWATT	ao
TDA8179S	Vertical Deflection Output Circuit	HEPTAWATT	ao
TDA9302	Vertical Deflection Output Circuit	CLIPWATT8	ao

HORIZONTAL DRIVER

Type Number	Description	Packages	Page/DB
TDA8140/A	Horizontal Deflection Power Driver	POWERDIP (8+8)	ao
TDA8143/A	Horizontal Deflection Power Driver	SIP9	ao

DEFLECTION ICs (Cont'd)

HORIZONTAL AND VERTICAL DEFLECTION PROCESSORS

Type Number	Description	Packages	Page/DB
TDA1180P	Horizontal Deflection Processor	DIP16	853
TDA2593	Horizontal Deflection Processor	DIP16	883
TDA8102B	H/V Processor for TTL V.D.U.	DIP20	997
TDA8128	Sync. Separator and Video Signal Identification	DIP8/MINIDIP	1027
TDA8185I	H/V Deflection Processor	DIP24	1039
TDA8214A	H/V Deflection Circuit	POWERDIP (16+2+2)	1087
TDA8215A	H/V Deflection Circuit	POWERDIP (16+2+2)	1097
TDA8218	H/V Deflection Circuit	POWERDIP (16+2+2)	1115
TDA9102B/C	H/V Processor for TLL V.D.U.	1125	1125
TEA2028B	Color TV Scanning and Power Supply Processor	DIP28	1141
TEA2029C	Color TV Scanning and Power Supply Processor	DIP28	1151
TEA2037A	H/V Deflection Monitor	DIP16	ao
TEA2117	H/V Deflection Monitor	MULTIWATT15	ao
TEA2128	Color TV Scanning and Power Supply Processor	SDIP24	1171
TEA2130	Color TV Scanning Processor	DIP20	1179

EAST/WEST CORRECTION

Type Number	Description	Packages	Page/DB
TDA4950	E/W Correction Circuit	DIP8/MINIDIP	ao
TDA8145	E/W Correction Circuit (Square Tube)	DIP8/MINIDIP	ao
TDA8146	E/W Correction Circuit (Universal)	DIP14	ao
TEA2031A	E/W Correction Circuit	DIP8	ao

DEFLECTION TRANSISTORS

Type Number	V_{CBO}	I_C	$V_{CE(sat)}$ @I_C I_B			t_s	t_f	Dissipation @ - I_{B2}		Packages	Page/ DB
	(V)	max (A)	max (V)	(A)	(A)	max (ms)	(ms)	@ 16 KHz (W)	(A)		
BU406	400	7	1	5	0.5	–	–	–	–	TO -220	ao
BU406 H	400	7	1	5	0.8	–	–	–	–	TO -220	ao
BU408	400	7	1	6	1.2	–	–	–	–	TO -220	ao
BU806 *	400	8	1.5	5	0.5	0.55•	0.2•	–	–	TO -220	ao
BU806 FI *	400	8	1.5	5	0.5	0.55•	0.2•	–	–	ISOWATT 220	ao
BU807 *	330	8	1.5	5	0.5	0.55•	0.2•	–	–	TO -220	ao
BU807 FI *	330	8	1.5	5	0.5	0.55•	0.2•	–	–	ISOWATT 220	ao
BU808FI *	1400	10	1.6	5	0.5	3	0.8	–		ISOWATT 218	ao

* Darlington
• Typical Value
▲ Also Ideal for SMPS

DEFLECTION TRANSISTORS (Cont'd)

Type Number	V_{CBO} (V)	I_C max (A)	$V_{CE(sat)}$ @ I_C I_B max (V)	(A)	(A)	t_s max (ms)	t_f (ms)	Dissipation @ - I_{B2} @ 16 KHz (W)	(A)	Packages	Page/ DB
BU808DFI *	1400	10	1.6	5	0.5	3	0.8	–	–	ISOWATT 218	ao
BU810 *	600	7	2.5	4	0.2	1.5	0.4	–	–	TO -220	ao
BUH313 ▲	1300	5	1.5	3	0.75	–	–	1	1.35	ISOWATT 218	ao
BUH313D	1300	5	1.5	3	0.75	–	–	1.9	1.65	ISOWATT 218	ao
BUH315 ▲	1500	5	1.5	3	0.75	–	–	1	1.35	ISOWATT 218	ao
BUH315D	1500	5	2	3	1	–	–	1.9	1.65	ISOWATT 218	ao
BUH417	1700	7	1.5	4	1	–	–	1.6	1.8	ISOWATT 218	ao
BUH515 ▲	1500	8	1.5	5	1.25	–	–	2.1	2.2	ISOWATT 218	ao
BUH515D	1500	8	1.5	5	1.25	–	–	3.1	2.2	ISOWATT 218	ao
BUH517	1700	8	1.5	5	1.25	–	–	1.7	2.5	ISOWATT 218	ao
BUH517D	1700	8	1.5	5	1.5	–	–	3.1	2.8	ISOWATT 218	ao
BUH715 ▲	1500	10	1.5	7	1.5	–	–	2.5	3.5	ISOWATT 218	ao
BUH1015T▲	1500	16	1.5	10	2	–	–	–	–	TO -218	ao
BUH1215T▲	1500	19	1.5	12	2.4	–	–	–	–	TO -218	ao
SGSF664	1200	20	1.5	12	2.4	3	0.25	–	–	TO -3	ao
SGSF665	1300	20	1.5	10	2	3	0.25	–	–	TO -3	ao

* Darlington
• Typical Value
▲ Also Ideal for SMPS

The Fastswitching BUH Series is a new family of high voltage Bipolar Transistors fully dedicated to TV and Monitor application. Their switching performance coupled with a new style of characterization make then ideal for horizontal deflection in most standard and high definition displays.

DEFLECTION DIODE

Type Number	Description	Package	Page/DB
DTV32-1500A	High Voltage Diode for Horizontal Deflection Circuits for High-End Monitors and TV	TO -220AC	ao

CHROMA

CHROMA VIDEO CIRCUITS

Type Number	Description	Packages	Page/DB
TDA3562A	PAL/NTSC One-Chip Decoder & Video Processor	DIP28	901
TDA8217	PAL Decoder & Video Processor	DIP20	1107
TEA5040	Bus-controlled Video Processor	DIP40	1187
TEA5640E	PAL/SECAM/NTSC 3.58/NTSC 4.53 Decoder	DIP28	1227
TEA5640F	PAL/SECAM Decoder	DIP28	1241
TEA5652	Wide Band Video Processor	DIP28	1255

RGB HIGH VOLTAGE OUTPUT STAGE

Type Number	Description	Packages	Page/DB
TDA8153	RGB Video Output Amplifier	MULTIWATT15	ao
TEA5101A	RGB Video Output Amplifier	MULTIWATT15	ao

VIDEO CHROMA & DEFLECTION PROCESSOR

Type Number	Description	Packages	Page/DB
STV2100	PAL Luma-Chroma & Deflection Processor	SDIP30	397

INTERMEDIATE FREQUENCY (IF)

VIDEO IF CIRCUITS

Type Number	Description	Packages	Page/DB
TDA2540/41	Video IF System With AFC	DIP16	875
TDA4443	Multistandard Video IF	DIP16	927
TDA8123A	Multistandard Video IF System	DIP16	1015

SOUND IF CIRCUITS

Type Number	Description	Packages	Page/DB
TDA1190Z	TV Sound Channel	FINDIP	865
TDA3190	TV Sound Channel	DIP16	891,d
TDA4190	TV Sound Channel	DIP20	909,d
TDA4445A/B	Multistandard Sound IF	DIP16	935
TDA8190	TV Sound Channel With DC Control	DIP20	1047,d
TDA8191	TV Sound Channel With DC Control	DIP20	1059,d
TDA8192	Multistandard AM & FM Sound IF	DIP20	1065,d

INTERMEDIATE FREQUENCY (IF) (Cont'd)

VIDEO AND SOUND IF

Type Number	Description	Packages	Page/DB
TDA8120B	Multistandard Video and Sound IF System	DIP24	1009
TDA8124	Multistandard Video IF Interface	DIP20	1023
TDA8213	Video & Sound IF System	DIP20	1077
TDA8222	Video & Sound IF System With Video and Sound Switches	SDIP24	1123

VIDEO AND SOUND SWITCHES

Type Number	Description	Packages	Page/DB
TDA8196	Audio Switch & DC Volume Control	DIP8/MINIDIP	1069,d
TDA8199	Stereo Amplifier & DC Volume Control for TV	DIP8/MINIDIP	1075,d
TEA1014	Video & Audio Switch	DIP14	1129
TEA2014A	Video Switch	DIP8/MINIDIP	1137
TEA2114	Large Bandwidth Video Switch	DIP8/MINIDIP	1163
TEA2124	Large Bandwidth Video Switch	DIP8/MINIDIP	1167
TEA5114A	RGB Switch Circuit	DIP16	1199
TEA5115	5 Channels Video Switch	DIP18	1205
TEA5116	5 Channels Video Switch	DIP18	1217
TEA6414A	Bus-Controlled Video Matrix Switch	DIP20	1305
TEA6415B	Bus-Controlled Video Matrix Switch	DIP20	1315
TEA6420	Bus-Controlled Audio Matrix Switch	SDIP24	1323

REMOTE CONTROL

Type Number	Description	Packages	Page/DB
M708/A	PCM Remote Control Transmitter	DIP20	181
M708L	PCM Remote Control Transmitter	DIP20	189
M709/A/710/A	PCM Remote Control Transmitter	DIP24-DIP28	197
M709L/710L	PCM Remote Control Transmitter	DIP24-DIP28	207
M3004AB1	Remote Control Transmitter	DIP20	217,d
M3004LAB1	Remote Control Transmitter	DIP20	225,d
M3005AB1	Remote Control Transmitter	DIP20	233,d
M3005LAB1	Remote Control Transmitter	DIP20	241,d
M3006LAB1	Remote Control Transmitter	DIP16	249,d
M145026/7/8	Remote Control Encoder	DIP16, SO-16	263,d
TDA8160	Infrared Remote Control Receiver	DIP8/MINIDIP	1031,d
TDA8162	Infrared Remote Control Receiver	DIP14	1035,d
UAA4000	PCM Remote Control Transmitter	DIP18	1335

TUNING SYSTEMS

VOLTAGE SYNTHESIS

Type Number	Description	Packages	Page/DB
M491B	Single-Chip Voltage Tuning System	DIP40	143
M494	Single-Chip Voltage Tuning System	DIP40	159
TDA4433	Signal Identification Circuit and AFC Interface	DIP14	921

FREQUENCY SYNTHESIS

Type Number	Description	Packages	Page/DB
M206	PLL TV Microcomputer Interface	DIP28	129
TEA8805	1.3 GHz PLL and Prescaler Circuit	DIP18, SO-20L	1327

VIDEO RECORDER CIRCUITS

Type Number	Description	Packages	Page/DB
M8716B	Clock Calendar with Serial I^2C BUS	DIP8/MINIDIP	257,d
TDA8118D	Control Head Play-Back & Record Amplifier and Signal Interface	SO-20	1005
TEA5701	3 Channels Large Band Head Amplifier for VCR	SO-20	1257
TEA5702	Advanced Playback & Record 2-Head Amplifier for VCR	SO-20	1267
TEA5703	Advanced Playback & Record 3-Head Amplifier for VCR	SO-20	1277
TEA5704	Advanced Playback & Record 4-Head Amplifier for VCR	SO-20	1287
TEA5712	Advanced FM Audio Play Back & Record Amplifier for VCR	SO-16	1297

TELETEXT DECODER

Type Number	Description	Packages	Page/DB
SAA5231	Data Slicer for Teletext Processor	DIP28	275
SDA5243/H	Computer-Controlled Teletext Decoder	DIP40	287
SDA5343	Computer-Controlled Teletext Decoder	DIP40	319
STV5343	Computer-Controlled Teletext Decoder	DIP40, SDIP42	407

SWITCH MODE POWER SUPPLY

Type Number	Description	Packages	Page/DB
TDA4601/B	Switch Mode Power Supply Controller	SIP9, DIP(8+8)	ao
TEA2018A	Current Mode SMPS Controller	DIP8/MINIDIP	ao
TEA2019	Current Mode SMPS Controller	DIP14	ao
TEA2164	Primary SMPS Controller (Slave)	DIP16	ao
TEA2260/61	Primary SMPS Controller (Slave)	DIP16	ao
TEA2262	Primary SMPS Controller (Slave)	DIP16	ao
TEA5170	Secondary SMPS Controller (Master)	DIP8/MINIDIP	ao
UC3842/3/4/5	PWM Controllers	DIP14, DIP8/MINIDIP	ao, n, o

GRAPHIC CIRCUITS

Type Number	Description	Packages	Page/DB
EF9345	HMOS2 Single-Chip Semi-Graphic Display Processor	DIP40, PLCC44	ao
EF9367	MOS Graphic Display Processor (GDP)	DIP40	ao
TS9347	Single-Chip Semi-Graphic Display Processor	DIP40, PLCC44	ao
TS68483	HMOS2 Advanced Graphic & Alphanumeric Controller	PLCC68	ao

INMOS GRAPHIC CIRCUITS

Type Number	Description	Speed (MHz)	Packages	Page/DB
IMS G171	High Performance CLUT	35, 50	DIP28	ai
IMS G176/176L	High Performance CLUT	40, 50, 66, (80)	DIP28,PLCC32, PLCC44	ai
IMS G177	Low Power CLUT	50	PLCC32	*
IMS G300C	Colour Video Controller	85, 100, 110	PGA84,CQFP100	ai
IMS G332	Colour Video Controller	85, 100, 110, (135)	CQFP100	*
IMS G364	Colour Video Controller	85, 100, 110, (135)	PGA132	*

DIGITAL SIGNAL PROCESSING DEVICES

Type Number	Description	Data Rate (MHz)	MOPS	Military Version	Package	Page/DB
IMSA100-17	1 Dimensional Filter / Convolver, 32 Taps	17	68-272	Yes	PGA84	m
IMSA100-21	1 Dimensional Filter / Convolver, 32 Taps	21	80-320	Yes	PGA84	m
IMSA100-30	1 Dimensional Filter / Convolver, 32 Taps	30	120-480	No	PGA84	m

IMAGE CODING DEVICES

Type Number	Description	Data Rate (MHz)	Package	Page/DB
IMSA121	Discrete Cosine Transform Processor (DCT) 8 x 8 Pixel Block Size Operation DCT, IDCT, Filter, Transpose Operation Post-Adder, Pre-Substractor	20	PLCC44	m
STV3200	Discrete Cosine Transform Processor (DCT) Multi Pixel Block Size Operation From 4 x 4 to 16 x 16 Pixels	15.0	DIP40, PLCC44	m
STV3208	Discrete Cosine Transform Processor (DCT) 8 x 8 Pixel Block Size Operation Zig-Zag Scan of Coefficients	20/27	DIP40	m
STI3220	Motion Estimator Processor Block Matching, full Search Algorithm -8/+7 displacements 8 x 8 to 16 x 16 Pixel Block Size Operation	18	PLCC68	m
IMSA113	Programmable - Length Digital Delay Line Variable Length 5-1317 Cycles	20	PLCC44	61,m

IMAGE PRE-POST PROCESSING DEVICES

Type Number	Description	Data Rate (MHz)	Package	Page/DB
IMSA110	2 Dimensional Filter / Convolver 21 x 1 or 7 x 3 Kermel 3 Delay Lines Back-end Processor	20	PGA100	m
STV3300	Filter and Dematrixing Chip Y, U, V to R, G, B Converter	27	PLCC52	399,m
STV8438	Triple 8-Bit D/A Converter Voltage Outputs Internal Voltage Reference External Analog Inputs With Switching Capability	70	SHRINK/ SDIP42	441,m

AUDIO POWER AMPLIFIERS

Type Number	Description	Packages	Page/DB
TDA1904	4W Audio Amplifier	POWERDIP (8+8)	ao,d
TDA1905	5W Audio Amplifier + Mute	POWERDIP (8+8)	ao,d
TDA2006	12W Audio Amplifier	PENTAWATT	ao,d
TDA2007	6+6W Stereo Amplifier	SIP9	ao,d
TDA2007A	6+6W Stereo Amplifier	SIP9	ao,d
TDA2009	10+10W Quality Stereo Amplifier	MULTIWATT 11	ao,d
TDA2009A	10+10W Quality Stereo Amplifier	MULTIWATT 11	ao,d
TDA2030	14W Hi-Fi Audio Amplifier	PENTAWATT	ao,d
TDA2030A	18W Hi-FI Audio Amplifier	PENTAWATT	ao,d
TDA2040	20W Hi-Fi Audio Amplifier	PENTAWATT	ao,d
TDA2050	28W Hi-Fi Audio Amplifier	PENTAWATT	ao,d
TDA2051	40W Hi-Fi Audio Amplifier	PENTAWATT	ao,d
TDA2052	65W Hi-Fi Audio Amplifier With Mute/Stand-By	HEPTAWATT	ao,d
TDA2822	Dual 1.7W Amplifier	DIP16	ao,d
TDA2822D	Dual 1 W Amplifier	SO-8	ao,d
TDA2822M	Dual 1W Amplifier	DIP8/MINIDIP	ao,d
TDA2824	Dual 1.7W Amplifier	POWERDIP (12+2+2)	ao,d
TDA2824S	Dual 1.7W Amplifier	SIP9	ao,d
TDA7231A	1.6W Audio Amplifier	DIP8/MINIDIP	ao,d
TDA7233/D	1W Audio Amplifier + Mute	MINIDIP, SO-8	ao,d
TDA7233S	1W Audio Amplifier + Mute	SIP9	ao,d
TDA7245	5W Audio Amplifier	POWER DIP (9+9)	ao,d
TDA7246	10W Audio Amplifier + Mute and Stand-By	HEPTAWATT	ao,d
TDA7250	Hi-Fi Dual Driver	DIP20	ao,d
TDA7262	20+20W High-Quality TV Amplifier	MULTIWATT11	ao,d

PREAMPLIFIERS AND AUDIO PROCESSORS

Type Number	Description	Packages	Page/DB
TDA7273	Stereo Cassette Playback System	SO-16	941,d
TDA7300	Digital Control Stereo Audio Processor	DIP28, SO-28	947,d
TDA7302	Digital Control Stereo Audio Processor	DIP28	961,d
TDA7306	Digital Control Stereo Audio Processor	DIP28	973,d
TDA7318	S-Bus Controlled Audio Processor	DIP28, SO-28	785,d

VOLTAGE REGULATORS

Type Number	Description	Packages	Page/DB
L4901A	Dual 5V Regulator With Reset	HEPTAWATT	ao,d
L4902A	Dual 5V Regulator With Reset and Disable	HEPTAWATT	ao,d
L4903	Dual 5V Regulator With Reset and Disable	DIP8/MINIDIP	ao,d
L4904A	Dual 5V Regulator With Reset	DIP8/MINIDIP	ao,d
L4905	Dual 5V Regulator With Reset and Disable	HEPTAWATT	ao,d
TDA8134	Dual Voltage Regulator With Disable (+5.1V, +12V)	HEPTAWATT	ao
TDA8135	Dual Voltage Regulator With Disable (+5V, Adjustable)	HEPTAWATT	ao
TDA8136	Dual Voltage Regulator With Disable (+12V)	HEPTAWATT	ao
TDA8137	Dual Voltage Regulator With Disable & Reset (+5.1V)	HEPTAWATT	ao
TDA8138	Dual Voltage Regulator With Disable & Reset (+5.1V)	SIP9 , HEPTAWATT	ao
TDA8139	Dual Voltage Regulator With Disable & Reset (+5.1V)	SIP9	ao
TEA7605	Low Dropout Voltage Regulator (+5V)	TO -220	ao
TEA7610	Low Dropout Voltage Regulator (+10)	TO -220	ao
TEA7685	Low Dropout Voltage Regulator (+8.5)	TO -220	ao

AUTOMATIC VOLTAGE SWITCH

Type Number	Description	Packages	Page/DB
AVS08	Automatic Mains Selector (110/220V AC) for SMPS < 200W	TO -220AB	43,ao
AVS10	Automatic Mains Selector (110/220V AC) for SMPS < 300W	TO -220AB	49,ao
AVS12	Automatic Mains Selector (110/220V AC) for SMPS < 500W	TO -220AB	55,ao

HIGH CURRENT SWITCHING REGULATORS

Type Number	Description	Packages	Page/DB
L4960	2.5A Power Switching Regulator	HEPTAWATT	ao
L4962	1.5A Power Switching Regulator	HEPTAWATT,(12+2+2)	ao
L4963	1.5A Power Switching Regulator	DIP18,(12+3+3)	ao
L4972A	2A Power Switching Regulator	POWERDIP (16+2+2), SO -20	ao

MOTOR CONTROLLERS

Type Number	Description	Packages	Page/DB
L272D	Dual Power Operational Amplifier	SO -16	79,d
L272/M	Dual Power Operational Amplifier	DIP8/MINIDIP	73,d
L2720/2/4	Low Drop Dual Power Operational Amplifier	POWERDIP (8+8), MINIDIP, SIP9	83,d
L2726	Low Drop Dual Power Operational Amplifier	SO -20	91,d
L6232A	Brushless Motor Drivers	PLCC28, PLCC44	95
L6243/D	Voice Coil Motor Drivers	SO -20, PLCC44	103

LED DISPLAY DRIVERS

Type Number	Description	Packages	Page/DB
M5450/51	LED Display Driver	DIP40, PLCC44	ao
M5480	LED Display Driver	DIP28	ao
M5481	LED Display Driver	DIP20	ao
M5482	LED Display Driver	DIP20	ao

SPECIAL FUNCTIONS

Type Number	Description	Packages	Page/DB
L6603/04	Smart Card Interface	DIP28, PLCC28	113
L6605	Smart Card Interface	POWERDIP (12+2+2)	121
L6720/21	Minitel Interface	POWERDIP (16+2+2)	ao
STV1389AQ	Cable Driver for Digital Transfer	QFP32	349
STV1601A	Serial Interface Transmission Encoder	PGA37	357
STV1602A	Serial Interface Transmission Decoder	PGA37	375

PROTECTION DEVICES

Type Number	Description	Packages	Page/DB
SM4T	400W/1ms Expo - Uni and Bidirectional Surface Mount Devices	SOD 6	ab
SM6T	600W/1ms Expo - Uni and Bidirectional Surface Mount Devices	SOD 6	ab
SM15T	1500W/1 ms Expo - Uni and Bidirectional Surface Mount Devices	SOD15	ab
TH6P04T	Transil Array	DIP20	ab

EEPROMS

Capacity	Organization	Bus type	Part Number	Package	Power Supply	Remark*	DB
256 Bits	16x16 SERIAL	MICROWIRE®	ST93C06B^x	PDIP8	5V		w
		MICROWIRE	ST93C06M^x	PSO8	5V		w
1K Bits	64x16 SERIAL or 128x8 SERIAL	MICROWIRE	ST93C46AB^x	PDIP8	5V		w
		MICROWIRE	ST93C46AM^x	PSO8	5V		w
1K Bits	64x16 SERIAL	MICROWIRE	ST93CS46B^x	PDIP8	5V	Write Protection Feature	w
		MICROWIRE	ST93CS46M^x	PSO8	5V	Write Protection Feature	w
		MICROWIRE	ST93CS47B^x	PDIP8	2,5V	Write Protection Feature	w
		MICROWIRE	ST93CS47M^x	PSO8	2,5V	Write Protection Feature	w
2K Bits	128x16 SERIAL	MICROWIRE	ST93CS56B^x	PDIP8	5V	Write Protection Feature	w
		MICROWIRE	ST93CS56M^x	PSO8	5V	Write Protection Feature	w
		MICROWIRE	ST93CS56ML^x	PSO14	5V	Write Protection Feature	w
		MICROWIRE	ST93CS57B^x	PDIP8	2,5V	Write Protection Feature	w
		MICROWIRE	ST93CS57M^x	PSO8	2,5V	Write Protection Feature	w
		MICROWIRE	ST93CS57ML^x	PSO14	2,5V	Write Protection Feature	w
2K Bits	256x8 SERIAL	I^2C	ST24C02AB^x	PDIP8	4,5 to 5,5V		w
		I^2C	ST24C02AM^x	PSO8	4,5 to 5,5V		w
		I^2C	ST25C02AB^x	PDIP8	2,5 to 5,5V		w
		I^2C	ST25C02AM^x	PSO8	2,5 to 5,5V		w
4K Bits	512x8 SERIAL	I^2C	ST24C04B^x	PDIP8	4,5 to 5,5V	Write Protection Feature	w
		I^2C	ST24C04ML^x	PSO14	4,5 to 5,5V	Write Protection Feature	w
		I^2C	ST25C04B^x	PDIP8	2,5 to 5,5V	Write Protection Feature	w
		I^2C	ST25C04ML^x	PSO14	2,5 to 5,5V	Write Protection Feature	w
8K Bits	1024x8 SERIAL	I^2C	ST24C08B^x	PDIP8	4,5 to 5,5V	Write Protection Feature	w

All products are available in 3 temperature ranges
Suffix x = 1 : 0°C to 70°C
Suffix x = 3 : -40°C to 125°C
Suffix x = 6 : -40°C to 85°C
• User defined size of memory section protected against write.

TIMEKEEPER

Capacity	Organization	Bus Type	Part Number	Packages	Power Supply	Remak	Page/DB
512 Bits	64x8 SERIAL REAL TIME CLOCK	I^2C	MK41T56	PDIP8	V_{DD} 4.5V to 5.5V V_{BAT} 2.4V to 3.6V	RTC With Software Calibration	a

Note: Operating Temperature, 0°C to 70°C

MICROCONTROLLERS

Type Number	Description	Packages	Page/DB
ST62, 63	Programming Manual		453
ST6326/27/28/ ST6356/57/58	8 Bit HCMOS MCUs for TV Frequency and Voltage Synthesis With OSD	DIP40, DIP48, SDIP42	497
ST6340/42/44/46	8 Bit Low Cost MCUs for TV Frequency & Voltage Synthesis With OSD	DIP28, DIP40	559
ST6385/86/87/88	8 Bit MCUs for TV Voltage Synthesis With OSD	SDIP42	613
ST6391/93/94/95/ 96/99	8 Bit HCMOS MCUs for TV Frequency Synthesis With OSD	SDIP42	675
ST6398	On Screen Display	DIP20	735
ST90R40	8/16 Bit Romless MCU With EEPROM	PLCC68	763
ST90R50	8/16 Bit Romless MCU With Bankswitch	PLCC84	783

DATASHEETS

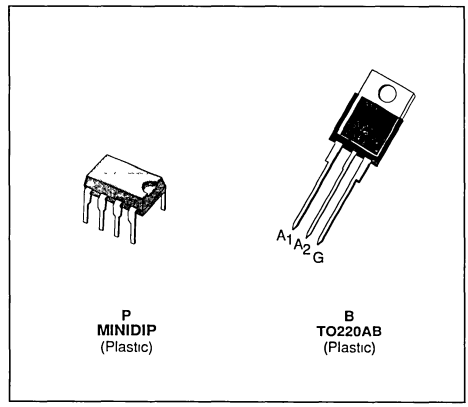
AUTOMATIC VOLTAGE SWITCH (SMPS < 200W)

CONTROLLER

- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIGGERING PULSE TRAIN OF THE TRIAC
- PARASITIC FILTER
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS08CB
- INSULATED PACKAGE (2500V_{RMS}) : AVS08CBI
- $V_{DRM} = \pm 500$ V
- $I_{T(RMS)}$: 5A



P
MINIDIP
(Plastic)

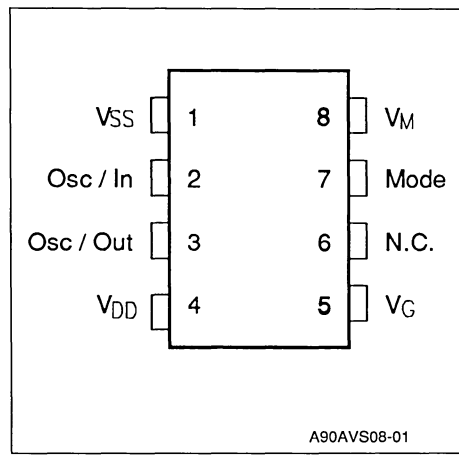
B
TO220AB
(Plastic)

DESCRIPTION

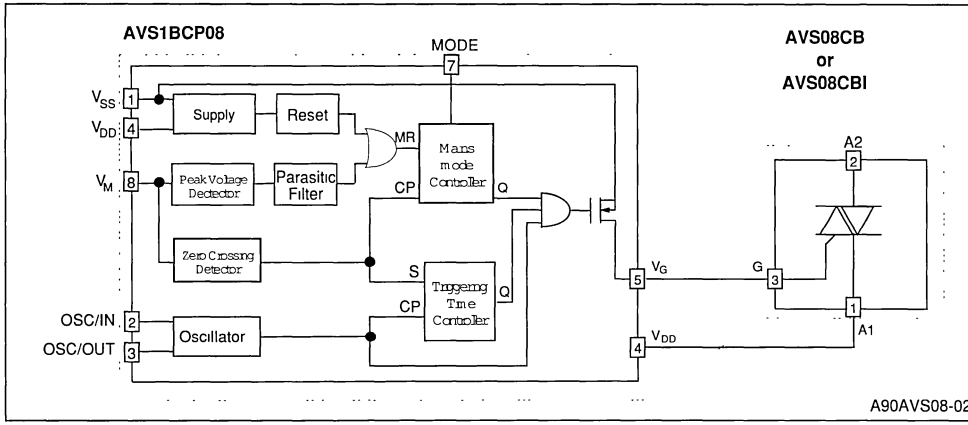
The AVS08 kit is an automatic mains selector (110/220V AC) to be used in SMPS < 200 W. It is composed of 2 devices :

- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option**. If the main power drops from 220V to 110V, the triac control remains locked to the 220V mode and avoids any high voltage spike when the voltage is restored to 220V.
  When connected to V_{DD}, the **mode** input desactivates this **option**.
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against disturbances.

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS1BCP08

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C " " T "	0 - 40	+ 70 + 105	°C

TRIAC AVS08CB / AVS08CBI T_j = +25°C (unless otherwise specified)

Symbol	Parameter			Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2)			± 500	V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle)	AVS08CB	T_C = 100°C	5	A
		AVS08CBI	T_C = 95°C		
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C)		t = 8.3ms t = 10ms	70 65	A
I^2t	I^2t value		t = 10ms	21	A^2s
dI/dt	Critical rate of rise of on-state current (1)		Repetitive f = 50Hz	20	A/µs
			Non Repetitive	100	
T_{stg} T_j	Storage Temperature Junction Temperature Range			- 40 + 125 - 10 + 125	°C

(1) Gate supply : I_G = 100mA – di/dt = 1A/µs
(2) T_j = 125°C

THERMAL RESISTANCES

TRIAC AVS08CB / AVS08CBI

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-to-ambient		60	°C/W
$R_{th\ (j-c)}$ DC	Junction-to-case for DC	AVS08CB	5.4	°C/W
		AVS08CBI	6.3	
$R_{th\ (j-c)}$ AC	Junction-to-case for 360° conduction angle (f = 50Hz)	AVS08CB	4.0	°C/W
		AVS08CBI	4.7	

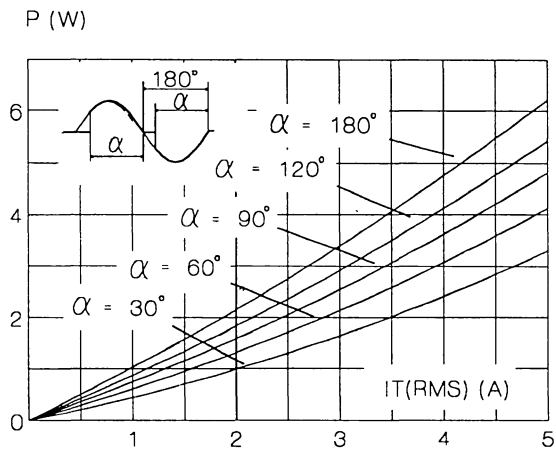
DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS08CB / AVS08CBI

Symbol	Parameter		Value		Unit
			Min.	Max.	
V_{TM} *	I_{TM} = 7A t_p = 10ms	T_j = 25°C		1.65	V
I_{DRM} *	V_{DRM} rated Gate open	T_j = 25°C		10	µA

* For either polarity of electrode A_2 voltage with reference to electrode A_1.

Figure 1 : Maximum RMS power dissipation versus RMS on-state current (f = 60Hz).



A90AVS08-03

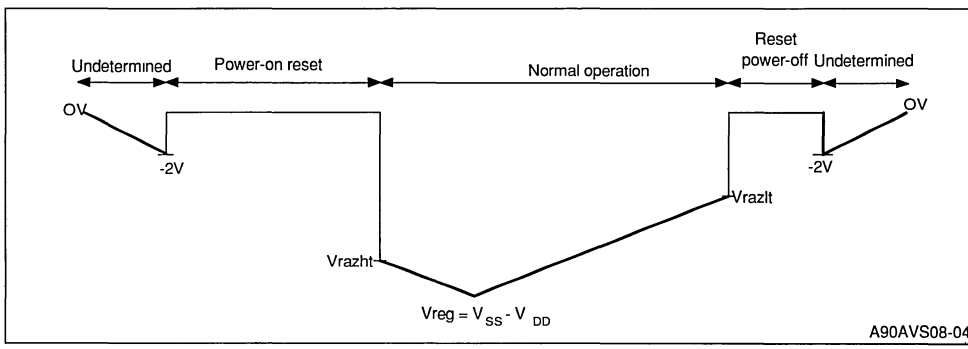
DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

CONTROLLER AVS1BCP08 T_{oper} = 25°C (unless otherwise specified)

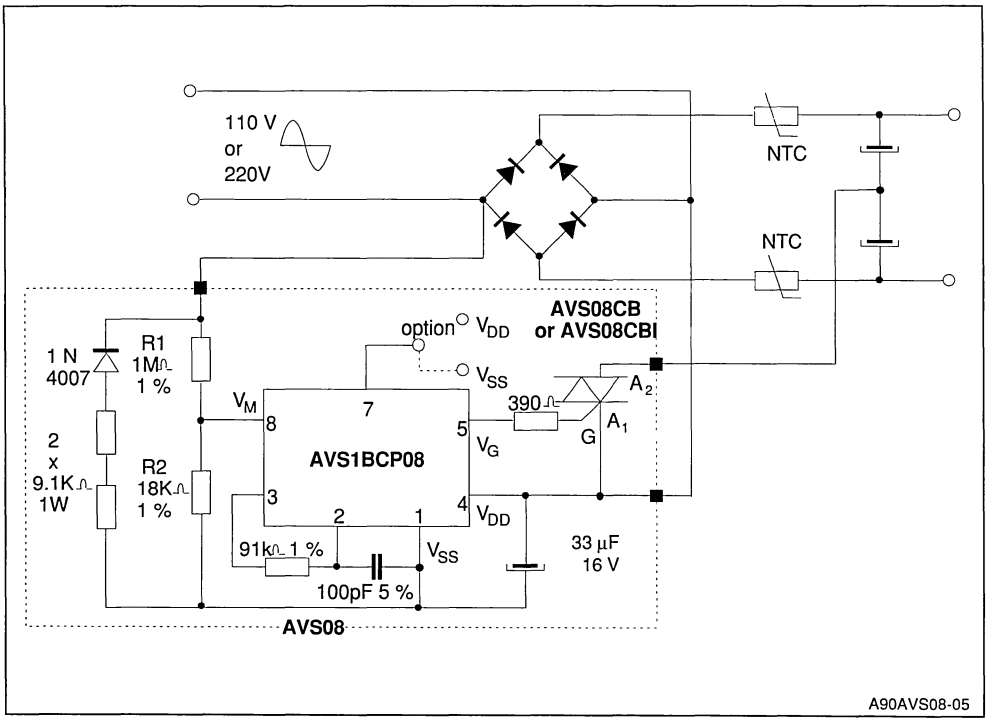
Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{SS} (pin 1) (Vreg)	Shunt regulator	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = 9V)	Supply current	0.4		25	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent current			1	mA
F (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator frequency	42	44	46	KHz
V_M (pin 8) Vth (3)	Peak voltage of detection high-threshold	4.08	4.25	4.42	V
V_M (pin 8) Vh (3)	Peak voltage of detection hysteresis	0.370	0.4	0.420	V
(1) V_M (pin 8) Vth (3)	Zero-crossing detection high-threshold	95	110	125	mV
V_M (pin 8) Vh (3)	Zero-crossing detection hysteresis	20	30	40	mV
(2) Vrazht (4)	Power-on-reset activation threshold		Vreg x 0.89		
(2) Vrazlt (4)	Power-down-reset activation threshold		Vreg x 0.55		
Mode (pin 7)	V_{IL} (4) V_{IH} (4)	0.7 Vreg		0.3 Vreg	
V_G (pin 5)	V_{OL} (I_{VG} = 25mA) Leakage current (V_G = V_{DD})			1 + 50	V µA

NOTES :
(1) . This value gives a typical noise immunity on the zero-crossing detectionof 110mV x 1018/18 = 6 20V on the main supply
(2) : See following diagram
(3) : Voltage referred to V_{SS}
(4) . Voltage referred to V_{DD}

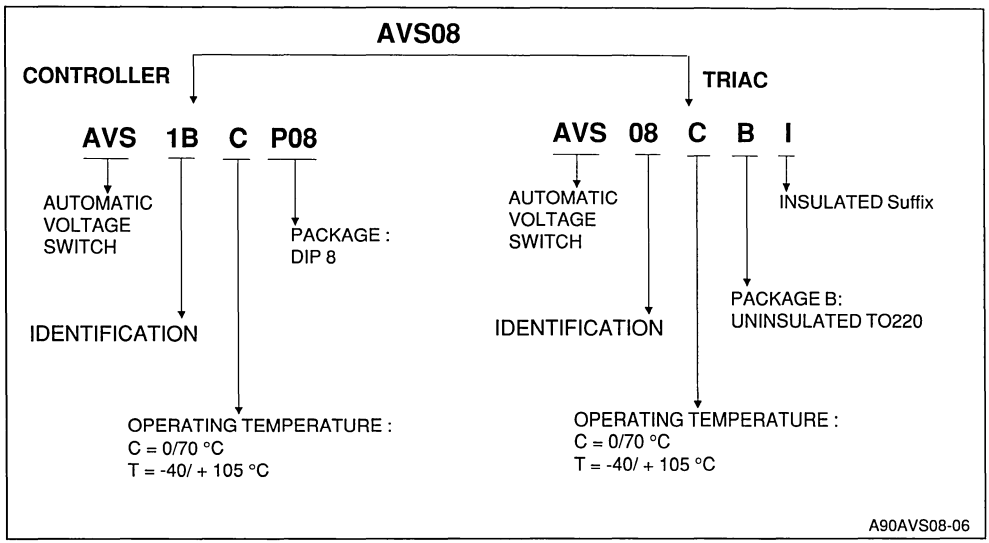
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION



ORDERING INFORMATION



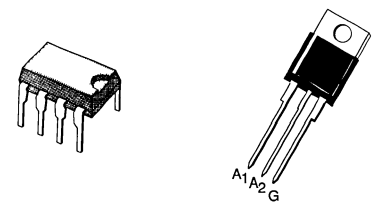
AUTOMATIC VOLTAGE SWITCH (SMPS < 300W)

CONTROLLER

- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIGGERING PULSE TRAIN OF THE TRIAC
- PARASITIC FILTER
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS10CB
- INSULATED PACKAGE (2500V_{RMS}) : AVS10CBI
- V_{DRM} = ± 600V
- $I_{T(RMS)}$: 8A



P
MINIDIP
(Plastic)

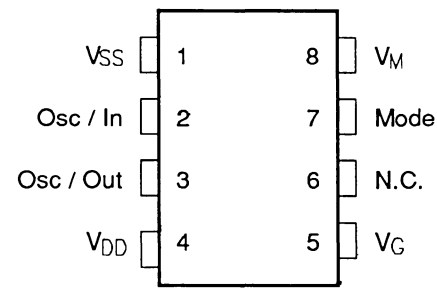
B
TO220AB
(Plastic)

DESCRIPTION

The AVS10 kit is an automatic mains selector (110/220V AC) to be used in SMPS < 300 W. It is composed of 2 devices :

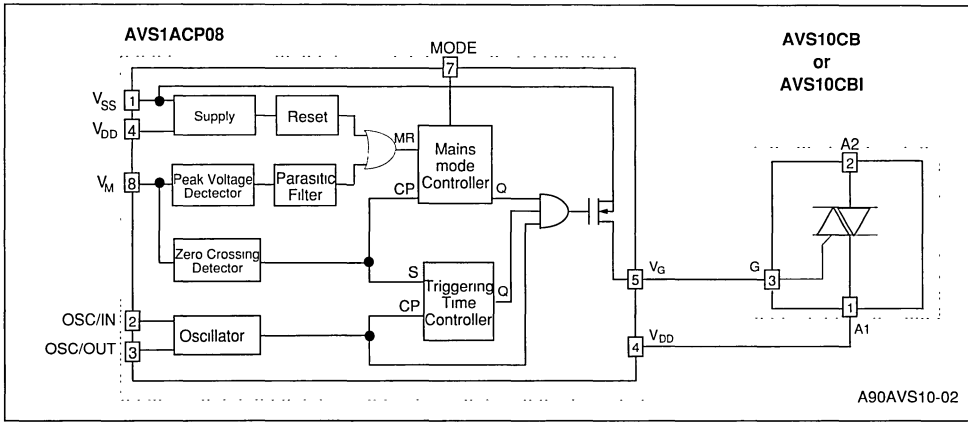
- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option**. If the main power drops from 220V to 110V, the triac control remains locked to the 220V mode and avoids any high voltage spike when the voltage is restored to 220V.
  When connected to V_{DD}, the **mode** input desactivates this **option**.
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against disturbances.

PIN CONNECTION



A90AVS10-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS1ACP08

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C " " T "	0 - 40	+ 70 + 105	°C

TRIAC AVS10CB / AVS10CBI T_j = +25°C (unless otherwise specified)

Symbol	Parameter			Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2)			± 600	V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle)	AVS10CB	T_C = 80°C	8	A
		AVS10CBI	T_C = 70°C		
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C)		t = 8.3ms t = 10ms	85 80	A
I^2t	I^2t value		t = 10ms	32	A^2s
di/dt	Critical rate of rise of on-state current (1)		Repetitive f = 50Hz	20	A/µs
			Non Repetitive	100	
dv/dt *	Linear slope up to 0.67 V_{DRM} Gate open		T_j = 110°C	50	V/µs
T_{stg} T_j	Storage Temperature Operating Junction Temperature			- 40 + 150 0 + 110	°C

(1) Gate supply : I_G = 100mA – di/dt = 1Aµs
(2) T_j = 110°C
* For either polarity of electrode A_2 voltage with reference to electrode A_1

THERMAL RESISTANCES

TRIAC AVS10CB / AVS10CBI

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-to-ambient		60	°C/W
$R_{th\ (j-c)}$ DC	Junction-to-case for DC	AVS10CB	3.5	°C/W
		AVS10CBI	4.4	
$R_{th\ (j-c)}$ AC	Junction-to-case for 360° conduction angle (f = 50Hz)	AVS10CB	2.6	°C/W
		AVS10CBI	3.3	

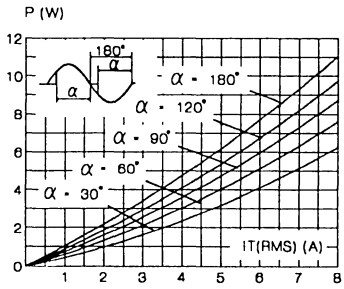
DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS10CB / AVS10CBI

Symbol	Parameter		Value		Unit
			Min.	Max.	
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3k\Omega$ Pulse duration> 20µs	T_j = 110°C	0.2		V
V_{TM} *	I_{TM} = 11A t_p = 10ms	T_j = 25°C		1.75	V
I_{DRM} *	V_{DRM} rated Gate open	T_j = 25°C		10	µA
		T_j = 110°C		500	

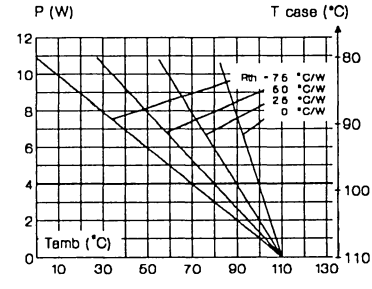
* For either polarity of electrode A_2 voltage with reference to electrode A_1.

Figure 1 : Maximum RMS power dissipation versus RMS on-state current (f = 60Hz).



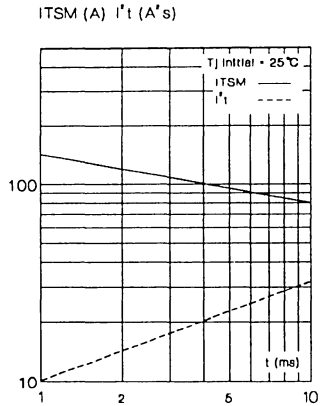
A90AVS10-03

Figure 2 : Correlation between maximum mean power dissipation and maximum allowable temperatures (T_A and T_C) for different thermal resistances heatsink + contact (AVS10CB).

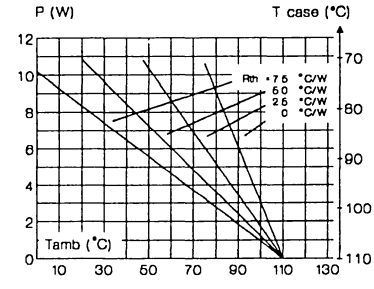


AVS10CB A90AVS10-04

Figure 3 : Non repetitive surge peak on-state current for a sinusoidal pulse with width : t ≤ 10ms, and corresponding value of I^2t.

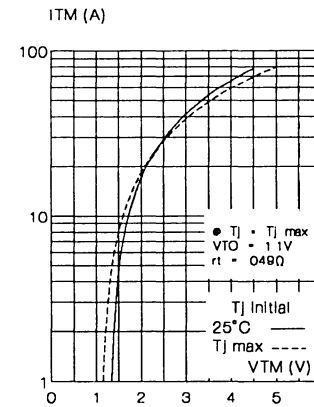


AVS10-06



AVS10CBI A90AVS10-05

Figure 4 : On-state characteristics (maximum values).



A90AVS10-07

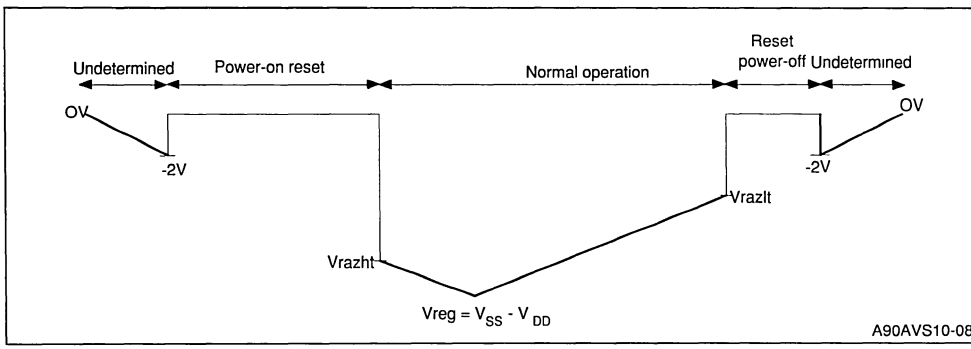
DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

CONTROLLER AVS1ACP08 T_{oper} = 25°C (unless otherwise specified)

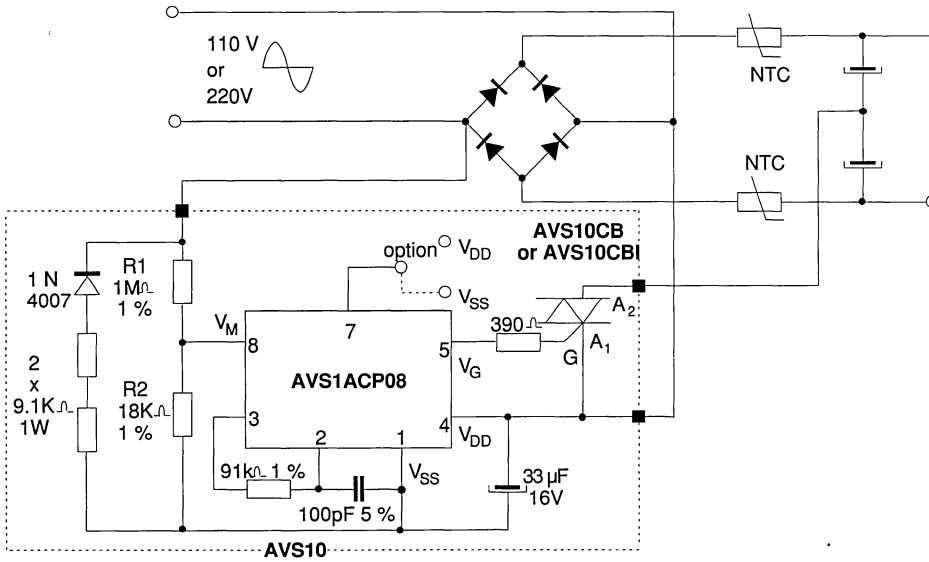
Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{SS} (pin 1) (Vreg)	Shunt regulator	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = 9V)	Supply current	0.4		30	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent current			0.7	mA
f (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator frequency	42	44	46	kHz
V_M (pin 8) Vth (3)	Peak voltage of detection high-threshold	4.08	4.25	4.42	V
V_M (pin 8) Vh (3)	Peak voltage of detection hysteresis	0.370	0.4	0.420	V
(1) V_M (pin 8) Vth (3)	Zero-crossing detection high-threshold	95	110	125	mV
V_M (pin 8) Vh (3)	Zero-crossing detection hysteresis	20	30	40	mV
(2) Vrazht (4)	Power-on-reset activation threshold		Vreg x 0.89		
(2) Vrazlt (4)	Power-down-reset activation threshold		Vreg x 0.55		
Mode (pin 7)	V_{IL} (4) V_{IH} (4)	0.7 Vreg		0.3 Vreg	
V_G (pin 5)	V_{OL} (I_{VG} = 25mA) Leakage current (V_G = V_{DD})			650 + 10	mV µA

NOTES :
(1) : This value gives a typical noise immunity on the zero-crossing detectionof 110mV x 1018/18 = 6.20V on the main supply
(2) : See following diagram
(3) : Voltage referred to V_{SS}
(4) : Voltage referred to V_{DD}

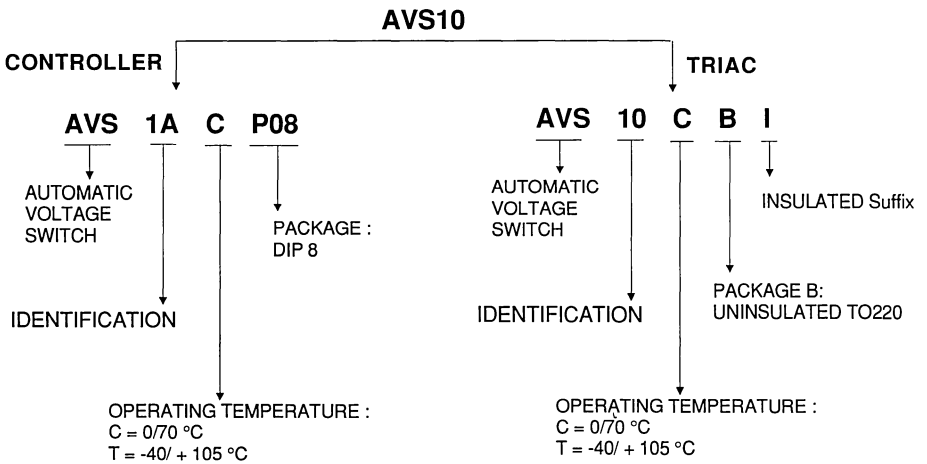
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION



ORDERING INFORMATION



SGS-THOMSON MICROELECTRONICS

AVS12

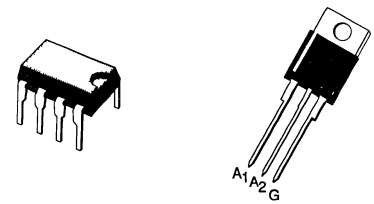
AUTOMATIC VOLTAGE SWITCH (SMPS < 500W)

CONTROLLER

- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIGGERING PULSE TRAIN OF THE TRIAC
- PARASITIC FILTER
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS12CB
- $V_{DRM} = \pm 600V$
- $I_{T(RMS)}$: 12A



P
MINIDIP
(Plastic)

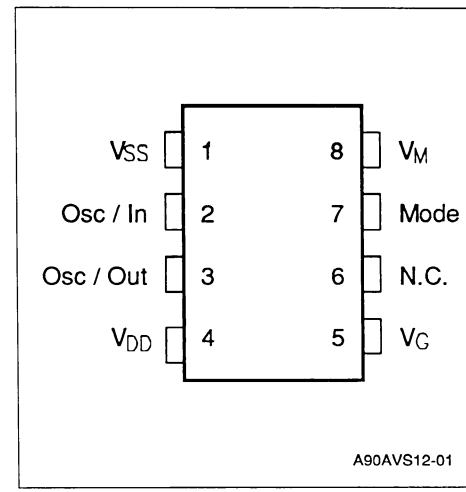
B
TO220AB
(Plastic)

DESCRIPTION

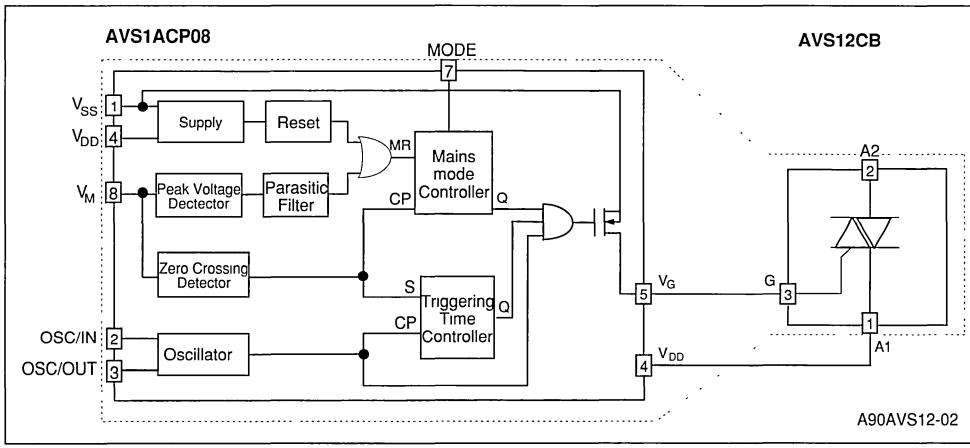
The AVS12 kit is an automatic mains selector (110/220V AC) to be used in SMPS < 500 W. It is composed of 2 devices :

- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option**. If the main power drops from 220V to 110V, the triac control remains locked to the 220V mode and avoids any high voltage spike when the voltage comes back to 220V.
  When connected to V_{DD}, the **mode** input desactivates this **option**.
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against disturbances.

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS1ACP08

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C " " T "	0 - 40	+ 70 + 105	°C

TRIAC AVS12CB T_j = 25°C (unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2)		± 600	V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle)	T_C = 70°C	12	A
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C)	t = 8.3ms t = 10ms	105 100	A
I^2t	I^2t value	t = 10ms	50	A^2s
di/dt	Critical rate of rise of on-state current (1)	Repetitive f = 50Hz	20	A/µs
		Non Repetitive	100	
dv/dt *	Linear slope up to 0.67 V_{DRM} Gate open	T_j = 110°C	50	V/µs
T_{stg} T_j	Storage Temperature Operating Junction Temperature		- 40 + 150 0 + 110	°C

(1) Gate supply : I_G =100mA – di/dt = 1A/µs * For either polarity of electrode A_2 voltage with reference to electrode A_1
(2) Tj = 110°C

THERMAL RESISTANCES

TRIAC AVS12CB

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-to-ambient	60	°C/W
$R_{th\ (j-c)}$ DC	Junction-to-case for DC	3	°C/W
$R_{th\ (j-c)}$ AC	Junction-to-case for 360° conduction angle (f= 50Hz)	2.3	°C/W

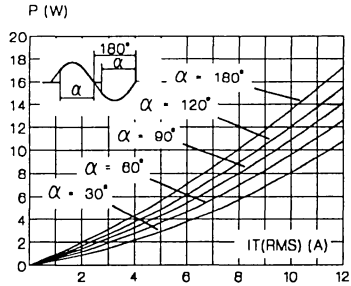
DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS12CB

Symbol	Parameter		Value		Unit
			Min.	Max.	
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3k\Omega$ Pulse duration> 20µs	$T_j = 110°C$	0.2		V
V_{TM} *	$I_{TM} = 17A$ tp = 10ms	$T_j = 25°C$		1.75	V
I_{DRM} *	V_{DRM} rated Gate open	$T_j = 25°C$		10	µA
		$T_j = 110°C$		500	

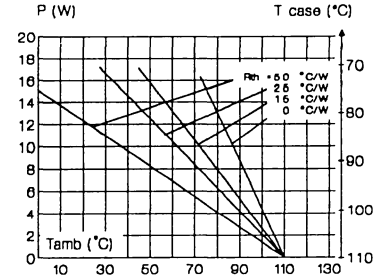
* For either polarity of electrode A_2 voltage with reference to electrode A_1.

Figure 1 : Maximum RMS power dissipation versus RMS on-state current (f = 60Hz).



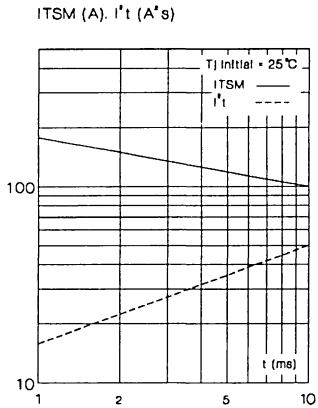
A90AVS12-03

Figure 2 : Correlation between maximum mean power dissipation and maximum allowable temperatures (T_A and T_c) for different thermal resistances heatsink + contact.



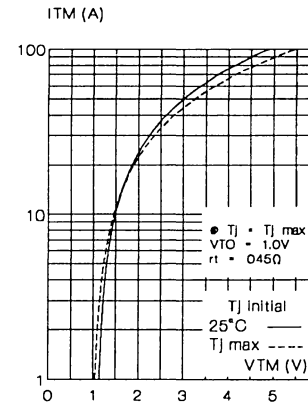
A90AVS12-04

Figure 3 : Non repetitive surge peak on state current for a sinusoidal pulse with width : t ≤ 10ms, and corresponding value of I^2t.



A90AVS12-05

Figure 4 : On-state characteristics (maximum values).



A90AVS12-06

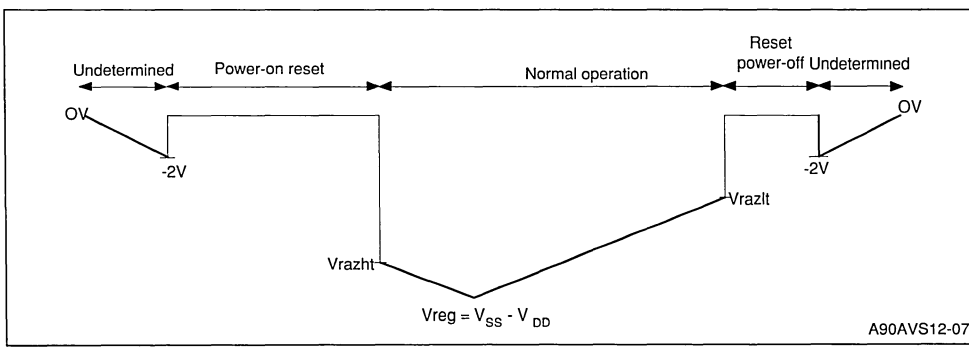
DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

CONTROLLER AVS1ACP08 T_{oper} = 25°C (unless otherwise specified)

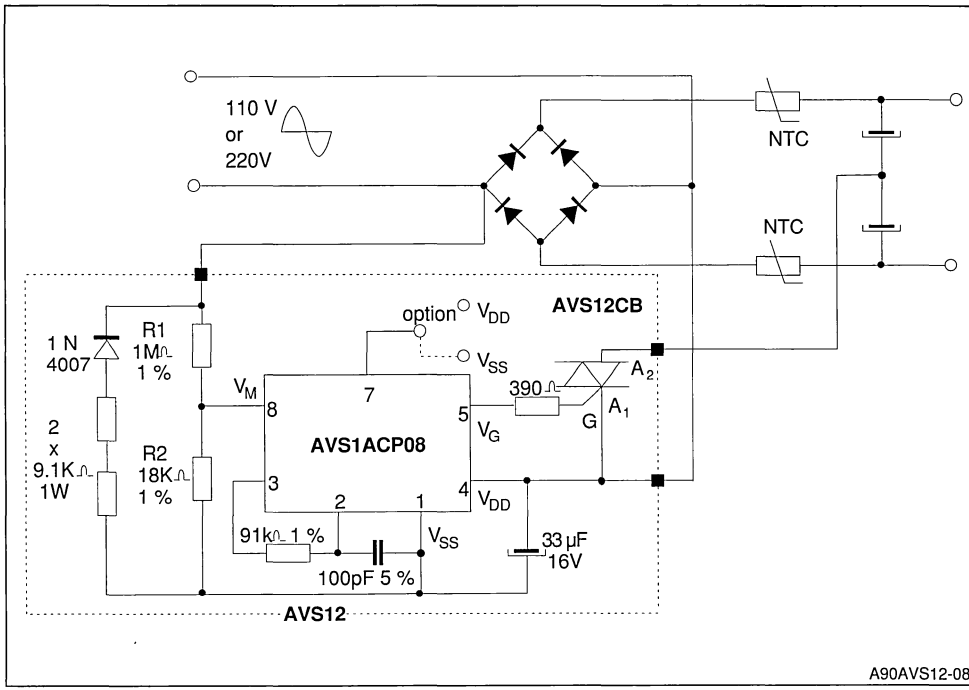
Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{SS} (pin 1) (Vreg)	Shunt regulator	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = 9V)	Supply current	0.4		30	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent current			0.7	mA
f (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator frequency	42	44	46	kHz
V_M (pin 8) Vth (3)	Peak voltage of detection high-threshold	4.08	4.25	4.42	V
V_M (pin 8) Vh (3)	Peak voltage of detection hysteresis	0.370	0.4	0.420	V
(1) V_M (pin 8) Vth (3)	Zero-crossing detection high-threshold	95	110	125	mV
V_M (pin 8) Vh (3)	Zero-crossing detection hysteresis	20	30	40	mV
(2) Vrazht (4)	Power-on-reset activation threshold		Vreg x 0.89		
(2) Vrazlt (4)	Power-down-reset activation threshold		Vreg x 0.55		
Mode (pin 7)	V_{IL} (4) V_{IH} (4)	0.7 Vreg		0.3 Vreg	
V_G (pin 5)	V_{OL} (I_{VG} = 25mA) Leakage current (V_G = V_{DD})			650 + 10	mV µA

NOTES :
(1) : This value gives a typical noise immunity on the zero-crossing detection of 110mV x 1018/18 = 6 20V on the main supply
(2) : See following diagram
(3) : Voltage referred to V_{SS}
(4) : Voltage referred to V_{DD}

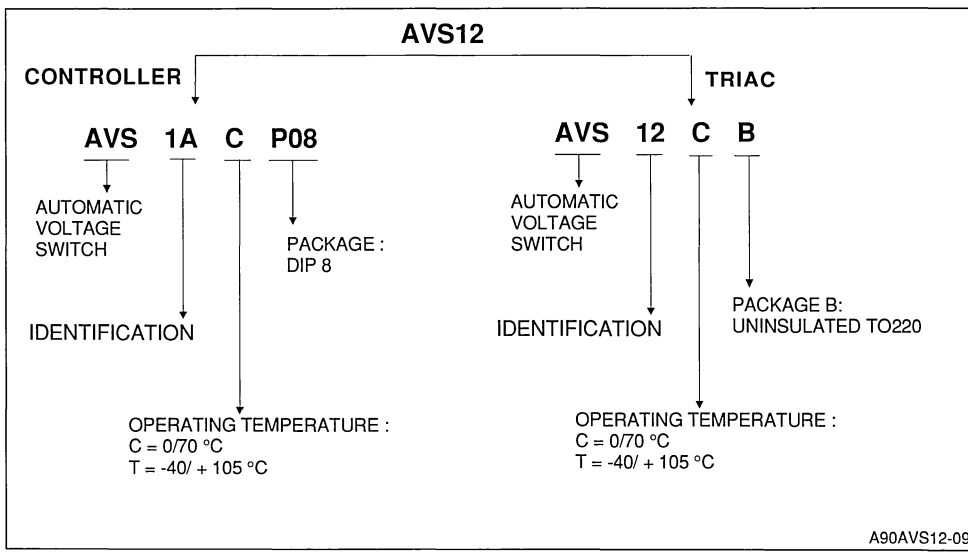
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION



ORDERING INFORMATION



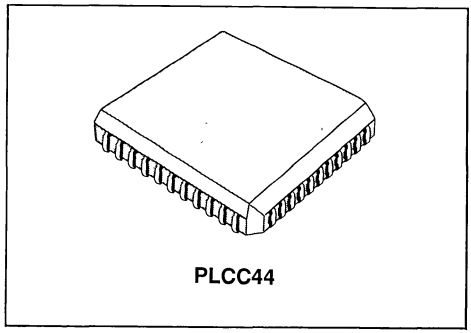
PROGRAMMABLE - LENGTH DIGITAL DELAY LINE

FEATURES

Variable length 5–1317 cycles (latencies of 6–1318)
Fully cascadable in width and length
Auto-zeroing of data on length change
Up to 20 MHz data rate
Fully static high speed CMOS implementation
TTL compatible
Single +5V ±10% Supply
Power dissipation < 250mWatts
44 pin PLCC package

APPLICATIONS

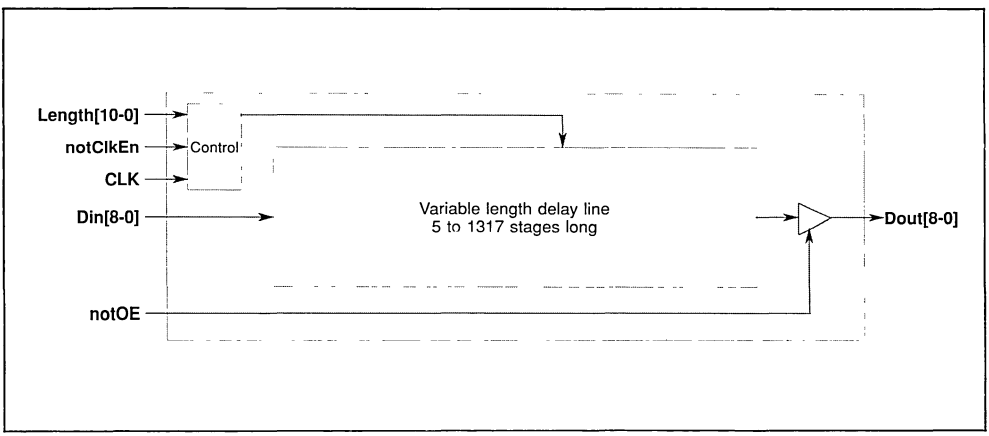
Image processing
Audio processing
Enhancment of A100/A110/A121 applications
Ghost/echo cancellation
Radar/Sonar Beamforming
Digital TV line buffer
Latency equaliser



PLCC44

DESCRIPTION

The **IMS A113** is a digital Delay line of programmable length. The device can be set up to delay input data from 5 clock cycles up to 1317 clock cycles. The delay line can be viewed as a data queue of prespecified length. On the rising edge of each clock pulse the data word on the **Din[8-0]** bus is placed onto the back of the queue and the data word at the front of the queue is placed onto the **Dout[8-0]** bus. Data is thus delayed by a number of clock cycles equal to the value present on the pins **Length[10-0]**.



1 PIN DESIGNATIONS

System services

Pin	In/out	Function
VCC, GND		Power supply and return
CLK	In	Input clock

Synchronous input/output

Pin	In/out	Function
Din[8-0]	In	Data input port
Dout[8-0]	Out	Data output port
notClkEn	In	Enable internal clock
Length[10-0]	In	Delay line length input port

Asynchronous input

Pin	In/out	Function
notOE	In	Output port tristate control

1.1 System services

Power

Power is supplied to the device via the **VCC** and **GND** pins. All supply pins must be connected. The supply must be decoupled close to the chip by at least one 100nF low inductance (e.g. ceramic) capacitor between **VCC** and **GND**. Four layer boards are recommended; if two layer boards are used, extra care should be taken in decoupling.

Input voltages must not exceed specification with respect to **VCC** and **GND**.

CLK

The clock input signal **CLK** controls the timing of input and the output on the three dedicated interfaces, and controls the progress of data through the line delay. Since the IMS A113 is fully static, the clock can be stopped in either phase without corrupting data.

Resetting the device

The IMS A113 does not have a reset pin. A reset is initiated automatically when power is first applied to the device. This reset will be completed once four cycles of **CLK** have occurred after **VCC** is valid.

1.2 Synchronous input/output

Din[8-0]

The data input port is sampled on every clock cycle. Data must be valid on the rising edge of **CLK**.

Dout[8-0]

The data output port is driven on the rising edge of **CLK**.

notClkEn

The **notClkEn** pin is sampled on the rising edge of **CLK**. The signal is active low. When it is inactive the device's internal clock is stopped, thus stopping the progress of data through the line delay.

Length[10-0]

The length of the delay line is specified by the binary number present on **Length[10-0]**. **Length[0]** is the least signifigant bit. The length set will give a *latency* of Length + 1 after the output data has been clocked on the following rising clock edge. For example to achieve a *latency* of 6 cycles **Length[10-0]** must be set to 5. Since **Din[8-0]** is latched on the rising clock edge when cascading devices for increased length the overall *latency* is the sum of the individual *latencies*.

For a fixed delay **Length[10-0]** are simply wired to **Vdd** or **Gnd** as appropriate. In order to accomodate variable delay lengths the **Length[10-0]** bus is sampled on the rising edge of **CLK**. When a delay length change is detected the line delay is reset. The value on the **Din[8-0]** bus at the time of the delay length change will appear at the **Dout[8-0]** bus after a period equal to the new delay length.

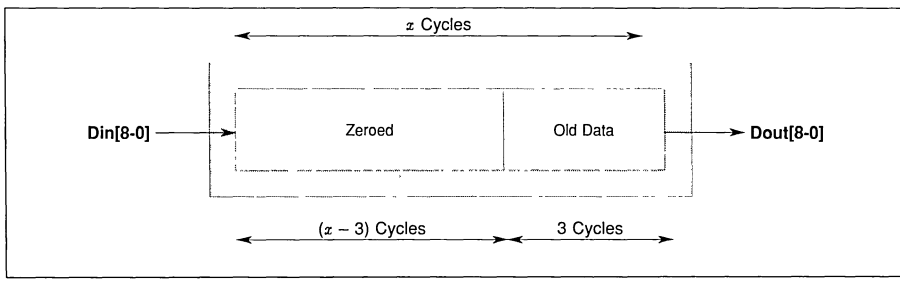
When the delay length on **Length[10-0]** is changed the contents of the delay line are zeroed, excepting the three data samples at the front of the queue. At power on the delay length on **Length[10-0]** is treated as a new length.

The exception to this is changing to the minimum delay length of five cycles, when no zeroing takes place.

When an illegal delay length (less than 5 or greater than 1317) is programmed no data is taken from the **Din[8-0]** bus. So effectively the **Dout[8-0]** bus will continue to be zero. The delay lengths from 1984 to 2015 are used for testing purposes and therefore should not be set.

Example of a length Change

If the delay length is changed for example to an x cycles delay, the status of the delay line immediately after the change is shown in the diagram below.



Thus the order of data pushed from the front of the queue immediately following the length change will be :–

- 3 cycles of original data (including data output as new length latched)
- $x - 3$ cycles of zeroed data
- Valid data, beginning with that sampled at the time of the length change

Refer to the timing diagram, Figure 1, for an example of changing the length to 6.

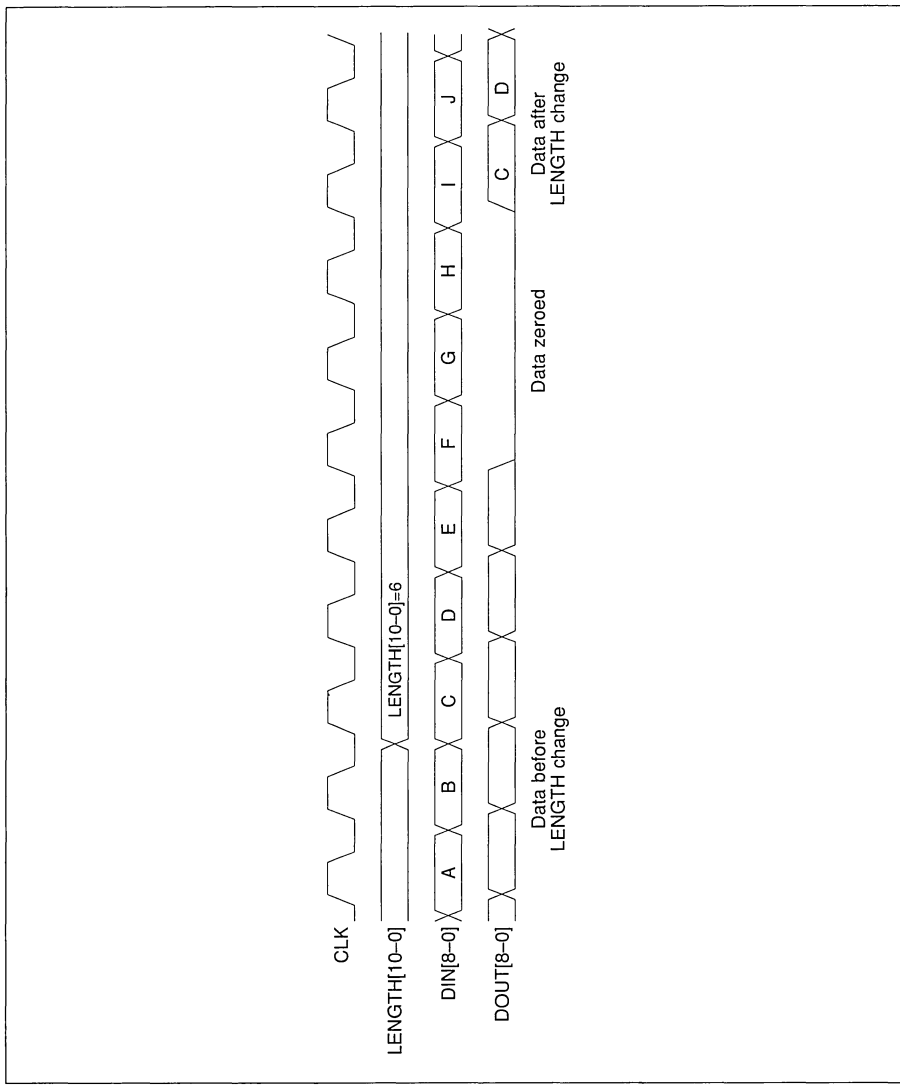


Figure 1 Example of length change

1.3 Asynchronous input/output

notOE

This pin is asynchronous to **CLK**. The signal is active low. When it is inactive the **Dout[8-0]** pins are high impedance.

2 ELECTRICAL SPECIFICATION

2.1 DC electrical characteristics

Absolute maximum ratings

Symbol	Parameter	Min	Max	Units	Notes (1)
VCC	DC supply voltage	0	7.0	V	2
VI, VO	Voltage on input and output pins	−1.0	VCC+0.5	V	2
TA	Temperature under bias	−40	85	°C	2
TS	Storage temperature	−65	150	°C	2
PDmax	Power dissipation		250	mW	

1 All voltages are with respect to GND.

2 This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC operating conditions

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes (1)
VCC	DC supply Voltage	4.5	5.0	5.5	V	
VIH	Input Logic '1' Voltage	2.0		VCC+0.5	V	2
VIL	Input Logic '0' Voltage	−0.5		0.8	V	2
TA	Ambient Operating Temperature	0		70	°C	3

Notes

1 All voltages are with respect to GND. All **GND** pins must be connected to GND.

2 Input signal transients 10 ns wide, are permitted in the voltage ranges GND − 0.5 V to GND − 1.0 V and VCC + 0.5 V to VCC + 1.0 V.

3 400 linear ft/min transverse air flow.

DC characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2)
VOH	Output Logic '1' Voltage	2.4	VCC	V	IO ≤ -4.4 mA
VOL	Output Logic '0' Voltage	0	0.4	V	IO $\leq$ 4.4 mA
IIN	Input leakage current (any input)		± 10	μA	3
ICC	Average power supply current		55	mA	4

Notes

1 All voltages are with respect to GND. All **GND** pins must be connected to GND.

2 Under the conditions specified by the DC operating conditions.

3 VCC = VCC(max), GND $\leq$ VIN $\leq$ VCC

4 This applies with no DC loading on the output pins at 20 MHz and it will be less at slower clock rates

2.2 A.C. timing characteristics

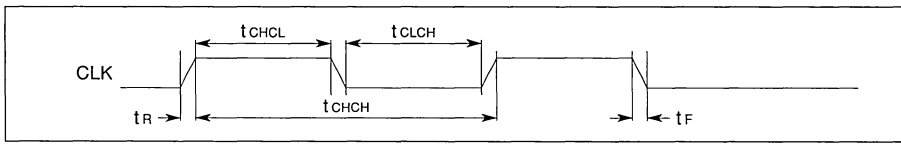
All timings are given for a load of 30pF unless otherwise stated.

Clock requirements

Symbol	Parameter	Min	Max	Units	Notes
t_{CHCL}	Clock Pulse High Width	20		ns	
t_{CLCH}	Clock Pulse Low Width	20		ns	
t_{CHCH}	Clock Period	50		ns	
t_R	Clock rise time	0	50	ns	1
t_F	Clock fall time	0	50	ns	1

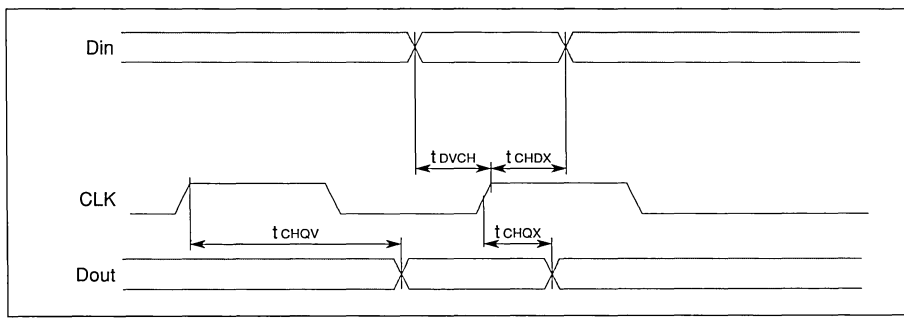
Notes

1 The clock edges should be monotonic between VIL and VIH.



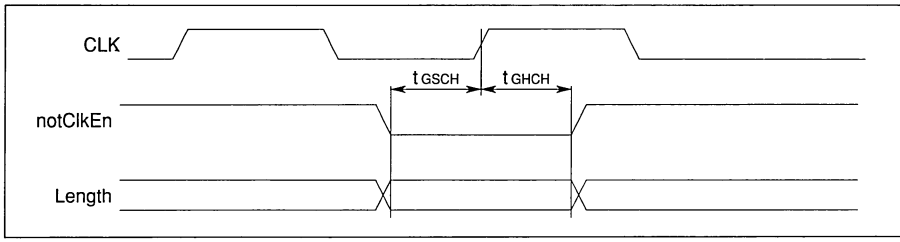
Synchronous input and output (Din, Dout)

Symbol	Parameter	Min	Max	Units	Notes
t_{CHQV}	CLK high to Dout Valid		38	ns	
t_{CHQX}	Dout hold time after CLK	2		ns	
t_{DVCH}	Din setup time to CLK high	10		ns	
t_{CHDX}	Din hold time to CLK high	0		ns	



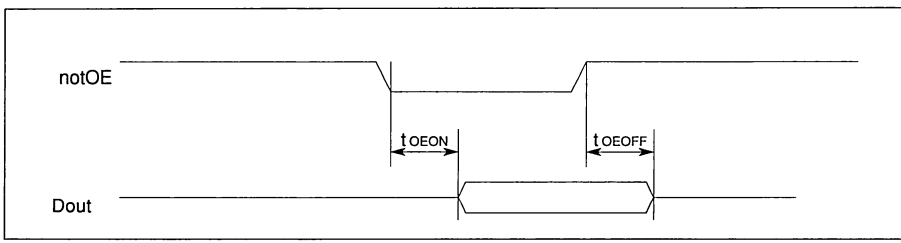
Synchronous control (notClkEn, Length[10-0])

Symbol	Parameter	Min	Max	Units	Notes
t_{GHCH}	notClkEn/Length hold to clock high	0		ns	
t_{GSCH}	notClkEn/Length setup to clock high	10		ns	

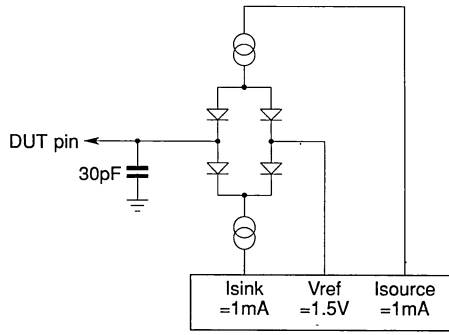


Asynchronous control (notOE)

Symbol	Parameter	Min	Max	Units	Notes
t_{OEON}	notOE to Dout enabled		15	ns	
t_{OEOFF}	notOE to Dout high impedance		15	ns	



Output load (output turn-off tests)



3 PACKAGE SPECIFICATIONS

3.1 44 pin PLCC package

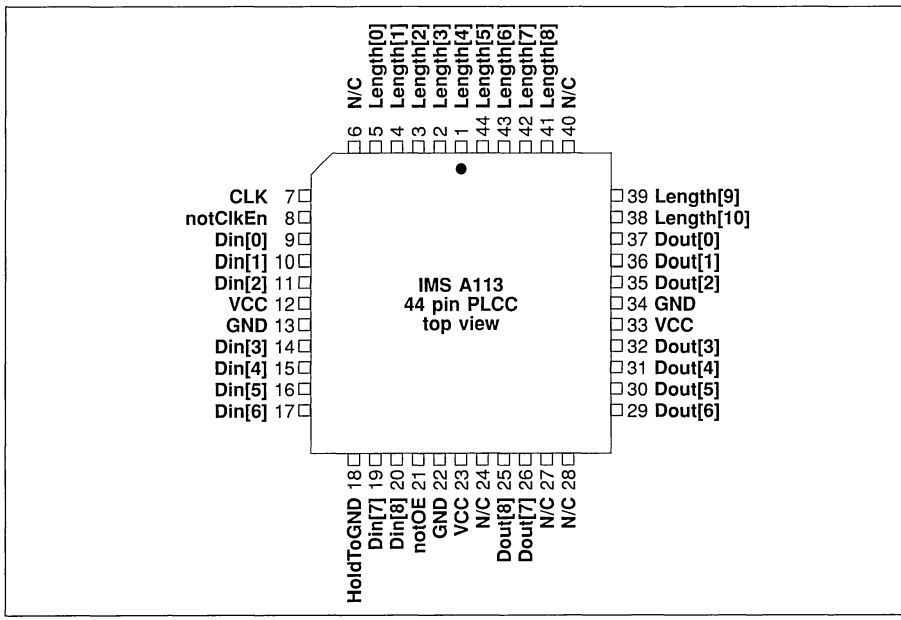


Figure 2 IMS A113 44 pin PLCC J-bend package pinout

Note

All **VCC** pins **must** be connected to the 5 Volt power supply.
All **GND** pins **must** be connected to ground.
N/C indicates pin not connected.

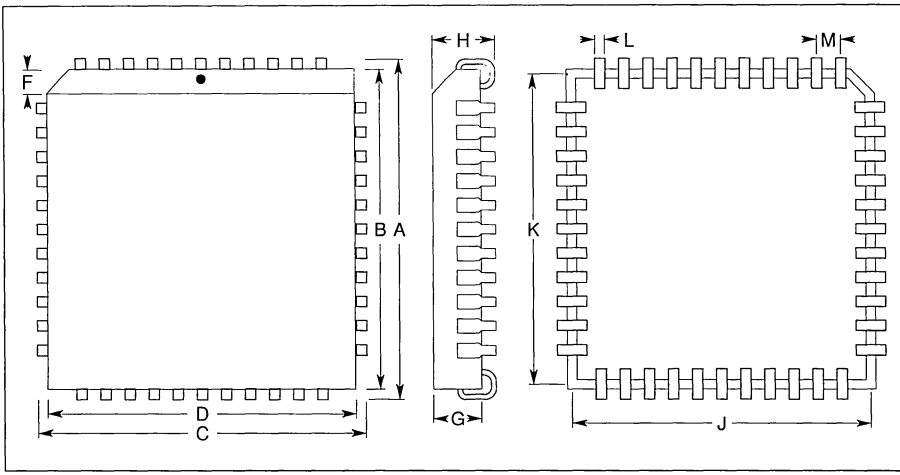


Figure 3 44 pin PLCC J-bend package dimensions

DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	17.577	±	0.692	±	
B	16.612	±	0.654	±	
C	17.577	±	0.692	±	
D	16.612	±	0.654	±	
F	1.143		0.045		
G	3.861		0.152		
H	4.369	±	0.172	±	
J	15.748	±	0.620	±	
K	15.748	±	0.620	±	
L	0.457		0.018		
M	1.270		0.050		

Table 1 44 pin PLCC J-bend package dimensions

PLCC thermal characteristics

Symbol	Parameter	Min	Nom	Max	Units	Notes
θ JA	Junction to ambient thermal resistance				°C /W	1,2

Notes

1 Measured at 400 linear ft/min transverse air flow.

2 This parameter is sampled and not 100% tested.

4 ORDERING DETAILS

The following table indicates the designation of the IMS A113 variants.

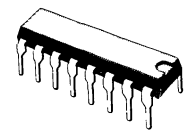
INMOS designation	Package	Clock speed	Military/commercial
IMS A113-J20S	Plastic LCC	20 MHz	commercial

DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8) **Minidip Plastic**

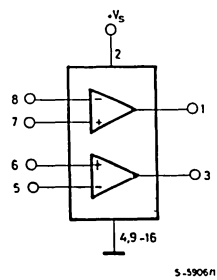
ORDERING NUMBERS:

L272 L272M

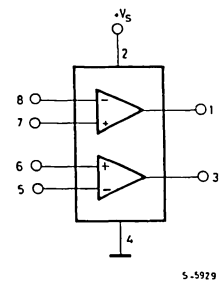
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C **(L272)**, T_{amb} = 50°C **(L272M)** T_{case} = 75°C **(L272)**	1.2 5	W W
T_{op}	Operating Temperature	−40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

BLOCK DIAGRAM

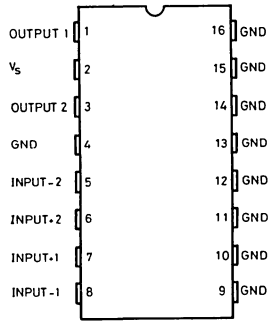


L272

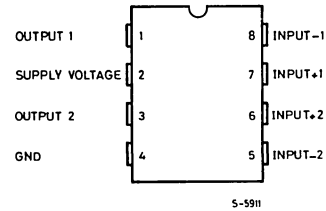


L272M

CONNECTION DIAGRAM
(Top view)

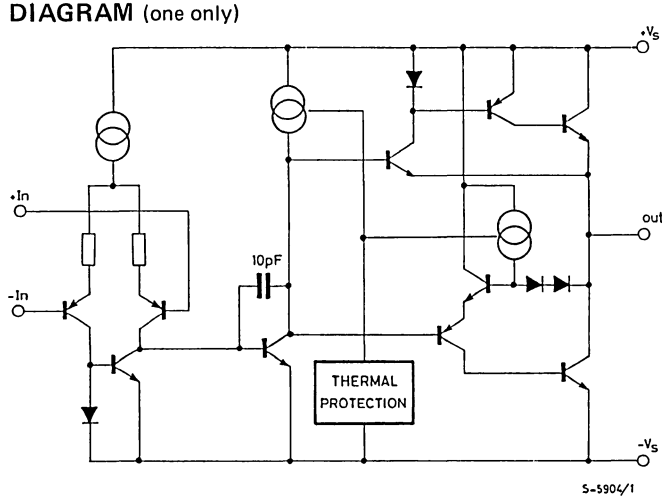


L272



L272M

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

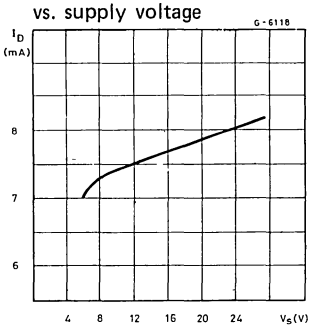


Fig. 2 - Quiescent drain current vs. temperature

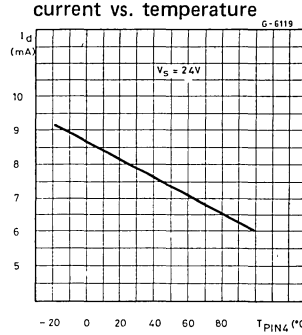


Fig. 3 - Open loop voltage gain

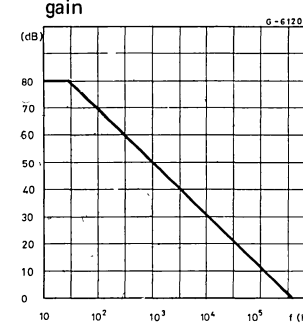


Fig. 4 - Output voltage swing vs. load current

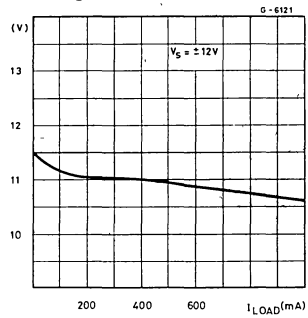


Fig. 5 - Output voltage swing vs. load current

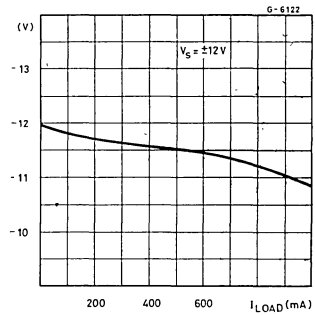


Fig. 6 - Supply voltage rejection vs. frequency

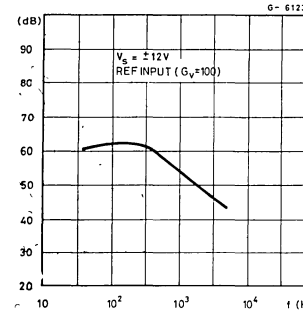


Fig. 7 - Channel separation vs. frequency

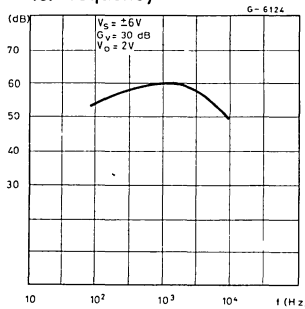
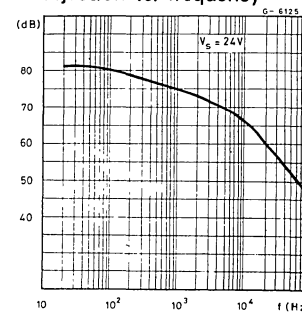


Fig. 8 - Common mode rejection vs. frequency



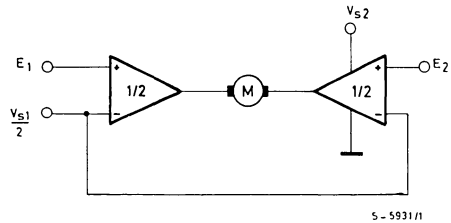
APPLICATION SUGGESTION

NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF +1Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

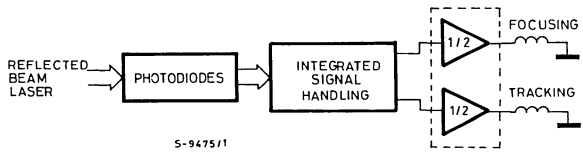


Fig. 11 - Capstan motor control in video recorders

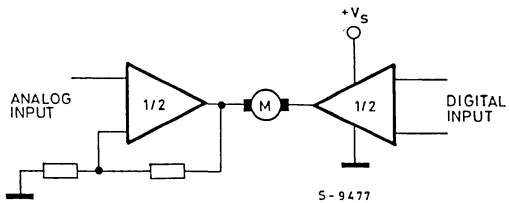
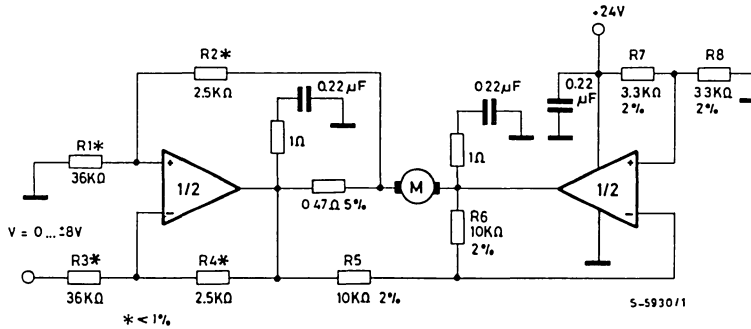


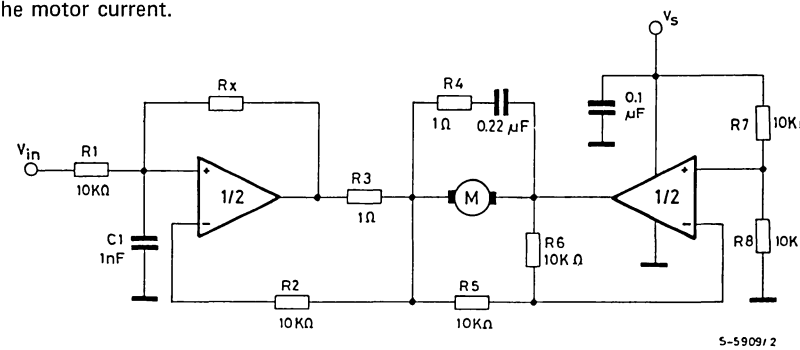
Fig. 12 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\left(V_I - \frac{V_s}{2}\right) + |R_o|.\ I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.

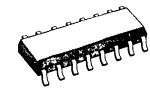


DUAL POWER OPERATIONAL AMPLIFIER

PRELIMINARY DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272D is a monolithic integrated circuit in SO-16 packages intended for use as power operational amplifier in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc. The high gain and high output power capability provide superior performance wheatever an operational amplifier/power booster combination is required.



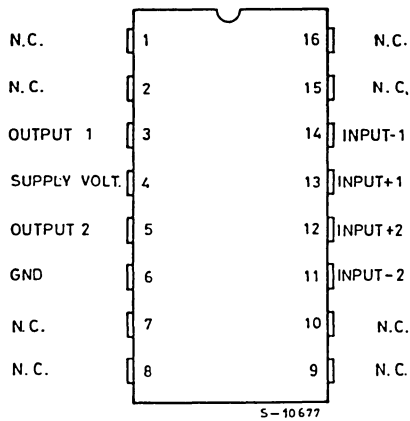
SO-16J

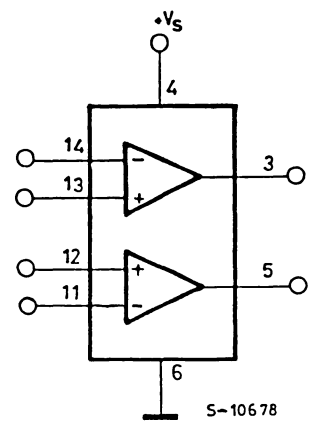
ORDERING NUMBER: L272D

ABSOLUTE MAXIMUM RATINGS

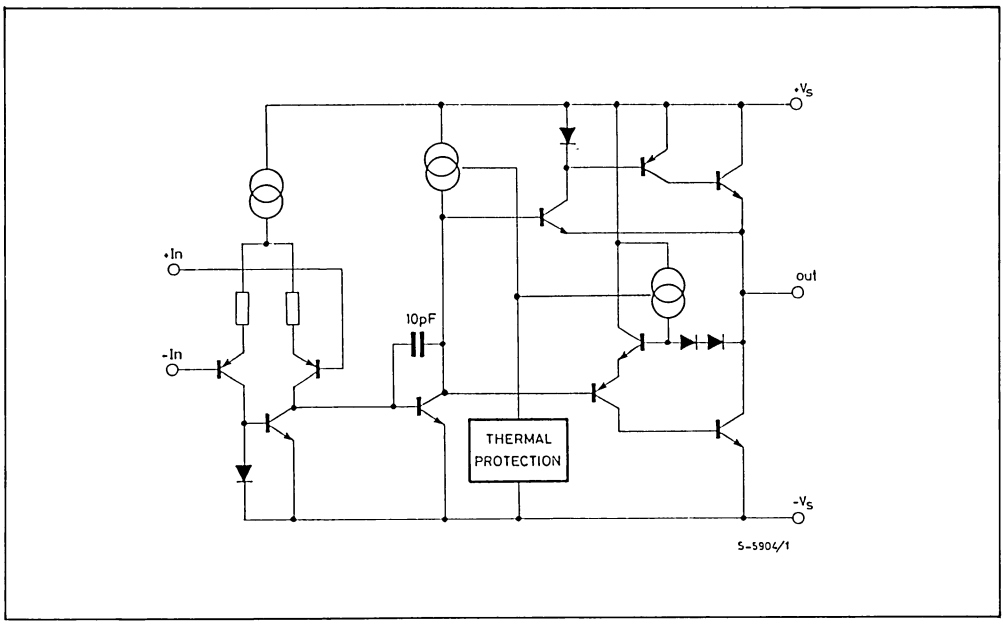
Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	1.2	W
T_{op}	Operating Temperature Range	−40 to +85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

CONNECTION DIAGRAMS





SCHEMATIC DIAGRAM (one only)



THERMAL DATA

$R_{thj-alumina(*)}$	Thermal resistance junction-alumina	max 50	°C/W

(*) Thermal resistance junctions-pins with the chip soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness and infinite heathsink.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

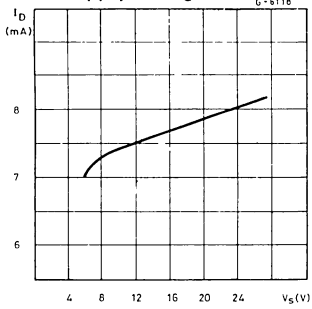


Fig. 2 - Quiescent drain current vs. temperature

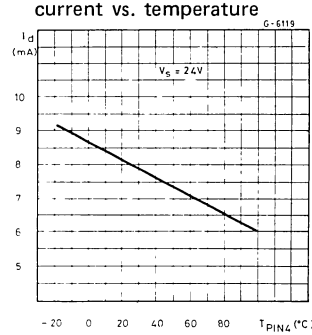


Fig. 3 - Open loop voltage gain

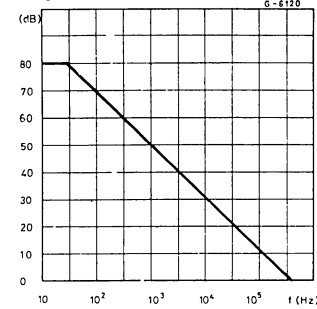


Fig. 4 - Output voltage swing vs. load current

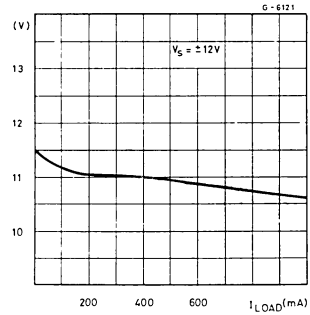


Fig. 5 - Output voltage swing vs. load current

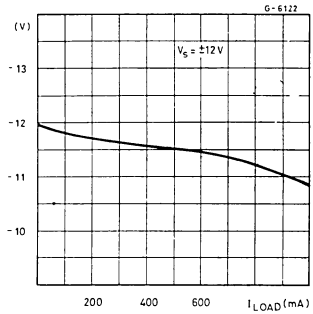


Fig. 6 - Supply voltage rejection vs. frequency

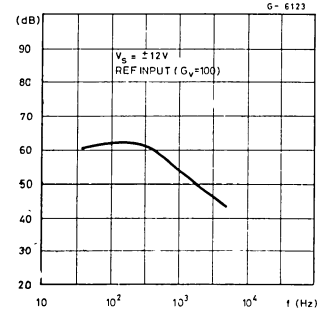


Fig. 7 - Channel separation vs. frequency

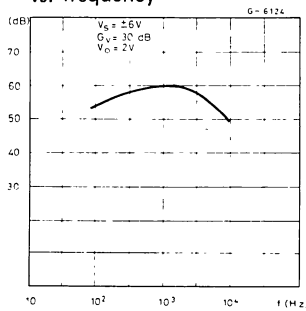
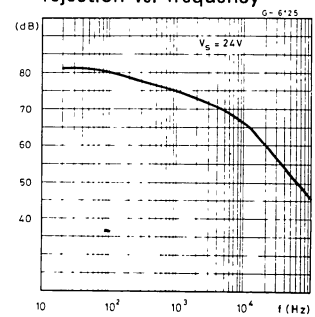


Fig. 8 - Common mode rejection vs. frequency



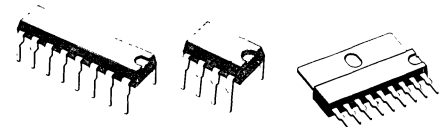
LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE
- ESD PROTECTION
- DUMP PROTECTION

The L2720, L2722 and L2724 are monolithic integrated circuits in powerdip, minidip and SIP-9 packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8) | **Minidip Plastic** | **SIP-9**

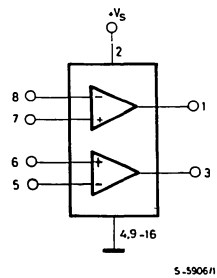
ORDERING NUMBERS:

L2720 L2722 L2724

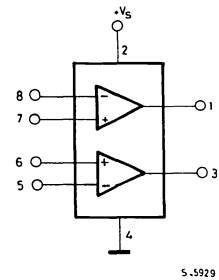
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C **(L2720)**, T_{amb} = 50°C **(L2722)** T_{case} = 75°C **(L2720)** T_{case} = 50°C **(L2724)**	1 5 10	W W W
T_{op}	Operating Temperature	−40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

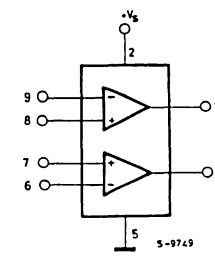
BLOCK DIAGRAMS



L2720

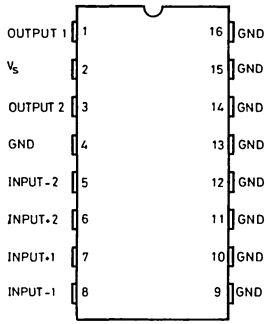


L2722

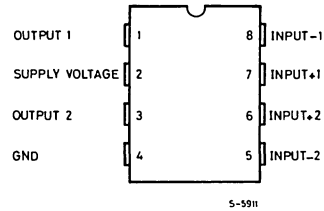


L2724

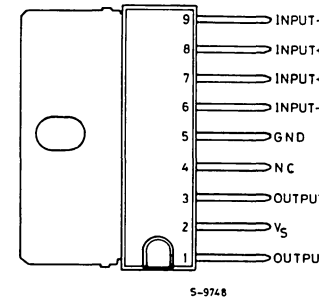
CONNECTION DIAGRAMS
(Top view)



L2720

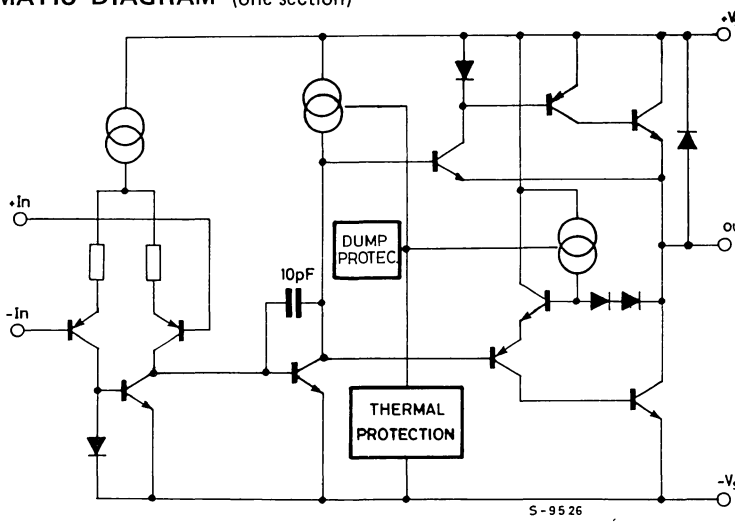


L2722



L2724

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			SIP-9	Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	10°C/W	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-albient	max	70°C/W	70°C/W	100°C/W

* Thermal resistance junction-pin 4.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/μs
B	Gain-bandwidth product				1.2		MHz
R_I	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		μV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

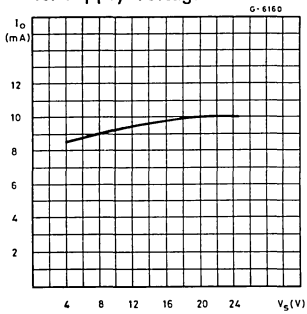


Fig. 2 - Open loop gain vs. frequency

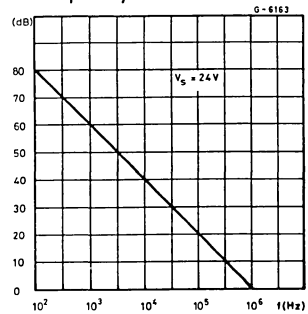


Fig. 3 - Common mode rejection vs. frequency

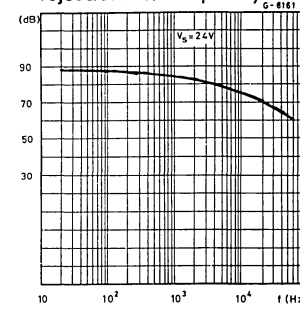


Fig. 4 - Output swing vs. load current (V_S = ± 5V)

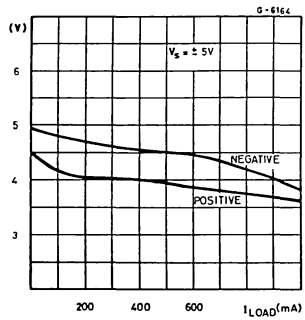


Fig. 5 - Output swing vs. load current (V_S = ± 12V)

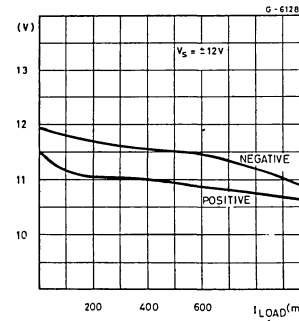


Fig. 6 - Supply voltage rejection vs. frequency

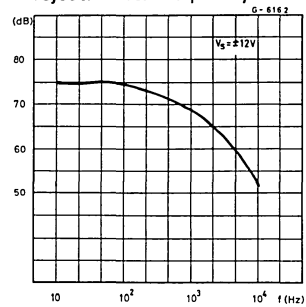
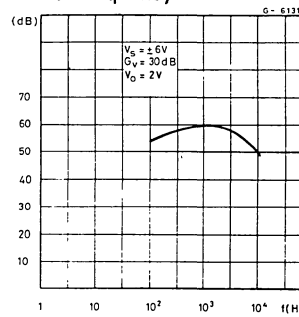


Fig. 7 - Channel separation vs. frequency

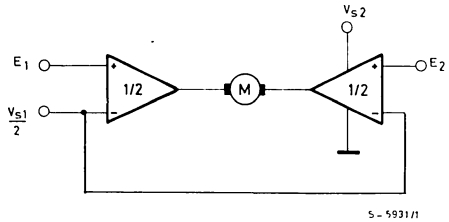


APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor connected between supply pins and ground;
- boucherot cell (0.1 to 0.2 μF + 1Ω series) between outputs and ground or across the load. With single supply operation, a resistor (1KΩ) between the output and supply pin can be necessary for stability.

Fig. 8 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 9 - Servocontrol for compact-disc

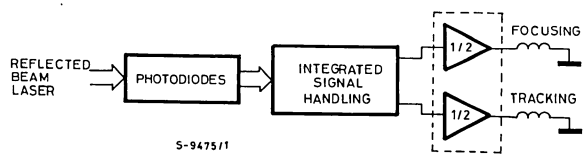


Fig. 10 - Capstan motor control in video recorders

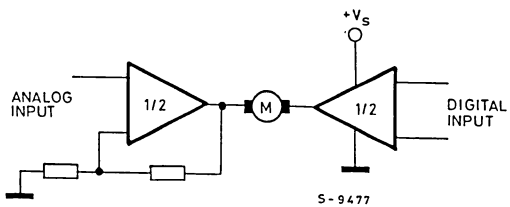
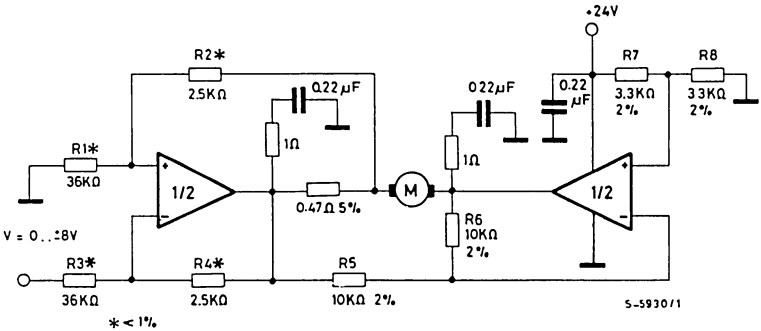


Fig. 11 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 12 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2 (V_I - \frac{V_s}{2}) + |R_o|. I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.

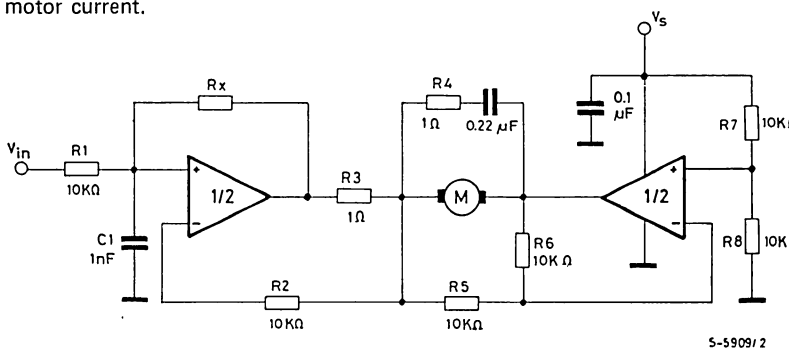
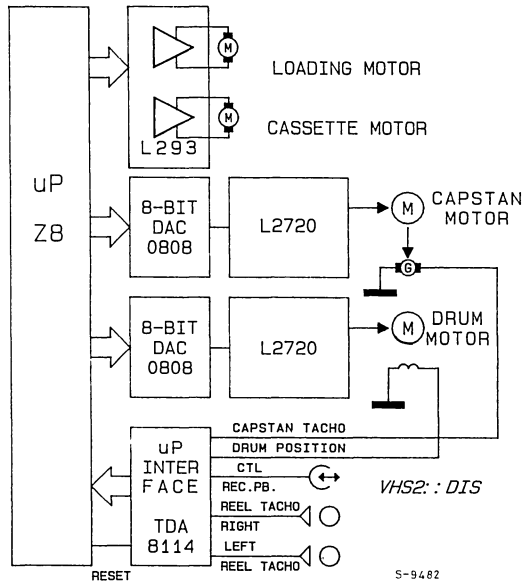


Fig. 13 - VHS-VCR Motor control circuit



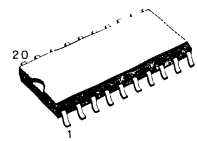
LOW DROP DUAL POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE
- ESD PROTECTION
- DUMP PROTECTION

The L2726 is a monolithic integrated circuit in SO-20 package intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

It is particularly indicated for driving inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



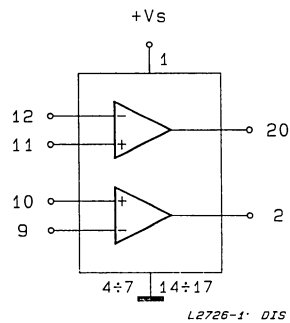
SO-20
(12 + 4 + 4)

ORDER NUMBER: L2726

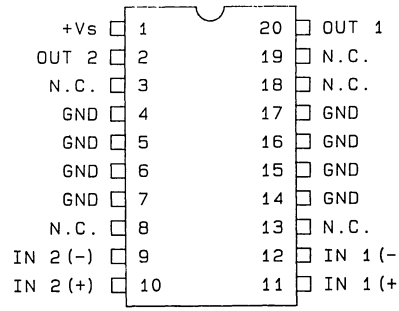
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 85°C T_{case} = 75°C	1 5	W W
T_{op}	Operating Temperature	−40 to 85	°C
T_{stg}, T_j	Storage and junction temperature	−40 to 150	°C

BLOCK DIAGRAM

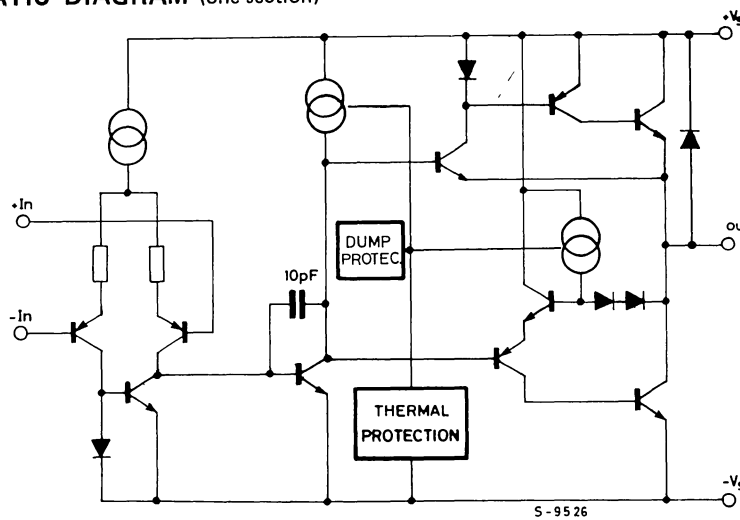


CONNECTION DIAGRAM
(Top view)



L2726-2::DIS

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	15.0 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (*)	max	65 °C/W

(*) With 4 sq. cm copper area heatsink

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_O = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	µA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/µs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		µV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

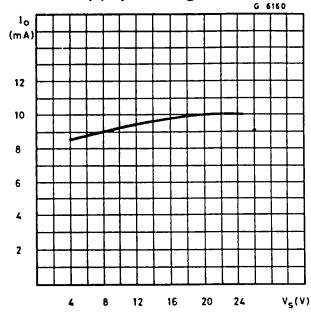


Fig. 2 - Open loop gain vs. frequency

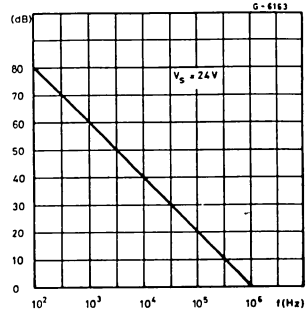


Fig. 3 - Common mode rejection vs. frequency

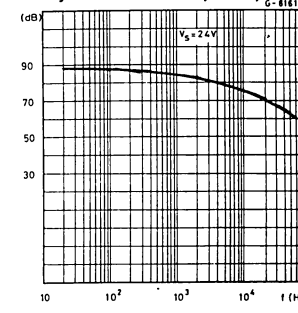


Fig. 4 - Output swing vs. load current (V_s = ± 5V)

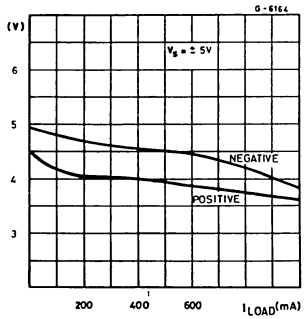


Fig. 5 - Output swing vs. load current (V_s = ± 12V)

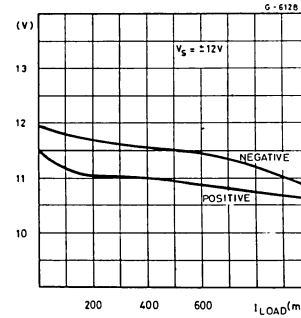


Fig. 6 - Supply voltage rejection vs. frequency

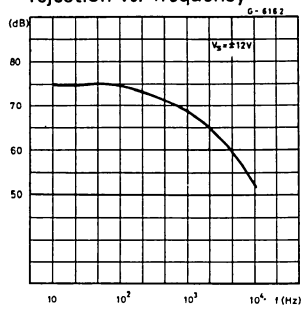
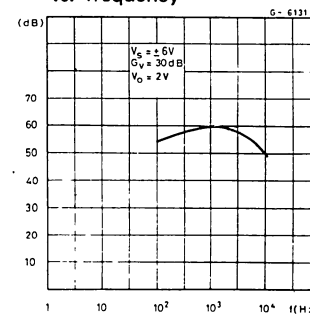


Fig. 7 - Channel separation vs. frequency



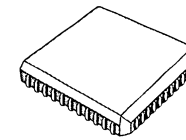
SGS-THOMSON MICROELECTRONICS

L6232A

SPINDLE DRIVER

ADVANCE DATA

- 2.5A MAXIMUM PEAK CURRENT
- CONTROLLED SLEW RATE
- CENTRAL CHARGE PUMP
- PWM AND LINEAR MODES
- CUTOFF TIME USER CONFIGURABLE
- FAST, FREE-WHEELING DIODES ON CHIP
- OVER-TEMPERATURE PROTECTION
- BRAKE FUNCTION INPUT

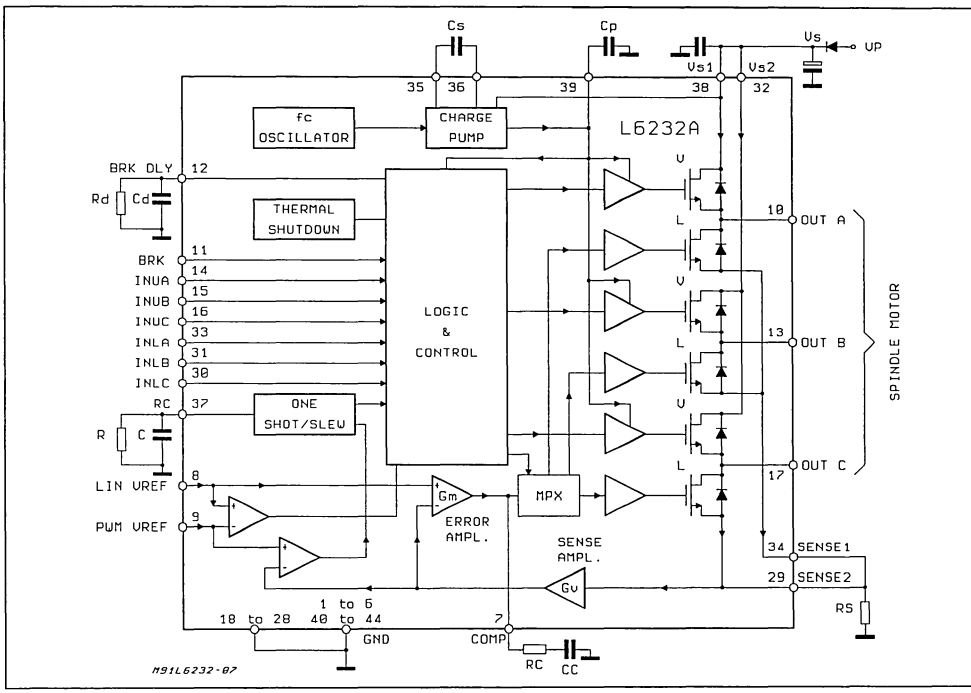


PLCC44
ORDERING NUMBER: L6232A

DESCRIPTION

The L6232A is a triple half bridge driver intended for use in brushless DC motor applications. This part can be used to form the power stage of a three-phase, brushless DC motor control loop, and is especially useful for disk drive applications. Power drivers are Integrated DMOS transistors and feature fast recirculating diodes as an integral part of their structure. The logic inputs are TTL-level compatible, with internal pull-up, allowing interfacing to open collector outputs. All necessary circuitry to perform PWM and linear motor speed control is included. A central charge pump is utilized to drive the upper DMOS transistors, and also to power the braking function. The L6232A is packaged in PLCC44.

BLOCK DIAGRAM

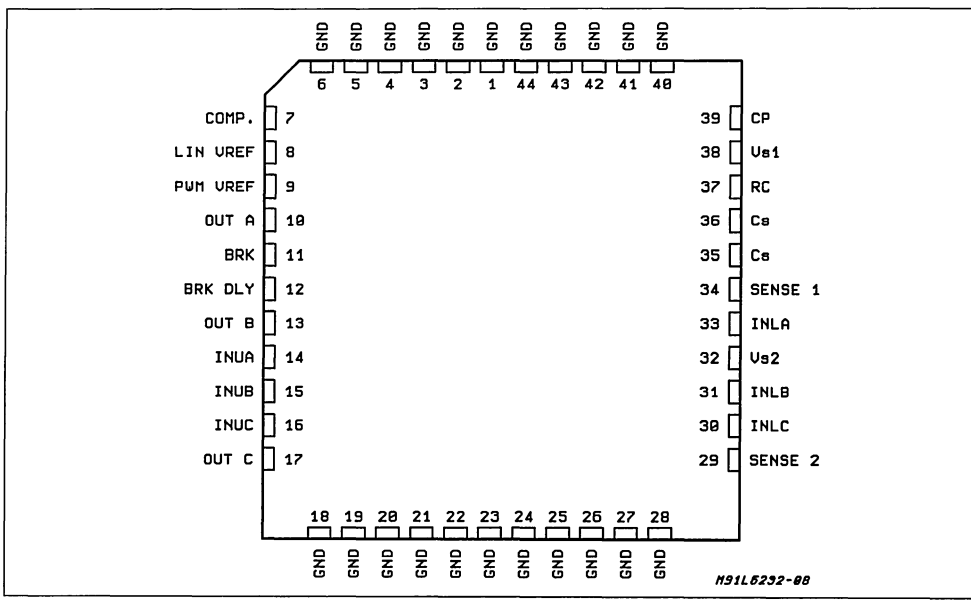


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION

Pin	Name	Function
1 to 6	GND	Common Ground. Also provides heat-sink to PCB.
7	COMP	External compensation for error amplifier.
8	LIN Vref	Input for Reference Control voltage in LIN mode.
9	PWM Vref	Input for Reference Control in PWM mode.
10	OUTA	DMOS Half-bridge A Out.
13	OUTB	DMOS Half-bridge B Out.
17	OUTC	DMOS Half-bridge C Out.
11	BRK	Active LOW logic input that triggers the delayed brake.
12	BRK DLY	External RC network for the brake delay.
14	INUA	Logic Inputs to turn on the upper drivers (Active Low).
15	INUB	
16	INUC	
18 to 28	GND	Common Ground. Also provides heat-sink to PCB.
29, 34	SENSE	Output for current sense resistors.
30	INLC	Logic inputs to turn on the lower drivers (Active High).
31	INLB	
33	INLA	
32, 38	V_S	Supply Voltage.
35, 36	C_S	External Charge Pump Capacitor.
37	RC	Cutoff Time RC Network in PWM mode. The Resistor value is also used to define the slew-rate in linear mode (LIN).
39	C_P	External Main Charge Pump capacitor.
40 to 44	GND	Common Ground. Also provides heat-sink to PCB.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DS\ sus}$	Peak Output Sustaining Voltage	18	V
V_S	Supply Voltage	15	V
V_i	Logic Input Voltage	-0.3 to 7	V
V_{REF}	PWM VREF--LIN VREF Input Voltage	-0.3 to 7	V
V_{is}	Sense Input Voltage	-1 to 7	V
I_p	Sink-Source Peak Output Current(*)	5	A
I_O	Sink-Source DC Output Current	2.5	A
P_{tot}	Total Power Dissipation (T_{amb} = 60°C)	2	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction-pins	Max.	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (**)	Max.	45	°C/W

Notes
(*) Pulsed T_{on}=5sec; DC=10%
(**) Mounted on board with minimized dissipating copper area

ELECTRICAL CHARACTERISTICS (See the block diagram, V_S =12V, R = 100KΩ; C = 180pF; T_j = 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		10.5	12	13.5	V
I_S	Quiescent Supply Current	BRK = L; INUA = INUB = INUC = L; INLA = INLB = INLC = H; Table 1		0.3	0.5	mA
		BRK = H; INUA = INUB = INUC = H; INLA = INLB = INLC = L; Table 1		4	6	mA
I_{OL}	Output Leakage Current	V_O = V_S = 13.5V			1	mA
R_{DSon}	Sink Out ON Resistance	T_j = 25°C (see Fig.4)		0.42	0.47	Ω
		T_j = 125°C		0.7		Ω
R_{DSon}	Source Out ON Resistance	T_j = 25°C (see Fig.4)		0.42	0.47	Ω
		T_j = 125°C		0.7		Ω
V_F	Body Diode Forward Drop (sink and source)	I_{DS} = 1A		1	1.5	V
$t_{d(BRK)}$	Brake Delay Time	See Fig. 1, 3; note1		100	300	ms
T_{BRK}	Braking Time		10			s
$I_{B(LIN)}$	LIN Vref Input Bias Current	LIN V_{ref} = 0.4 to 5.5V		400	800	nA
$I_{B(PWM)}$	PWM Vref Input Bias Current	PWM V_{ref} = 0.4 to 5.5V		400	800	nA
LIN V_{ref}	Reference Voltage Input	Note 2; R_S = 0.5Ω I_{motor} (PWM) = 1A I_{motor} (LIN) = 200mA		2		V
PWM V_{ref}				0.4		V
G_v	Sense Amplifier Voltage Gain	PWM V_{ref} = 2.5V, LIN V_{ref} = 0.4V, R_S = 0.5Ω; Note 2	3.8	4	4.2	V/V
G_m	LIN Error Amplifier Transconductance			0.8		mA/V
Zout	Error Amplifier Output Impedance			2		MΩ

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INH}	Logic Input Voltage BRK; INUA; INUB; INUC; INLA; INLB; INLC		2			V
V_{INL}					0.8	V
$I_{INH(leak)}$	Logic Input Current BRK; INUA; INUB; INUC; INLA; INLB; INLC	V_I = 2.7V			-1	mA
I_{INL}		V_I = 0.4V			-0.1	mA
t_{donU}	Upper/Lower Turn-on Delay	Table 1 see Fig. 3		0.7		µs
t_{donL}				0.15		µs
t_{doffU}	Upper/Lower Turn-off Delay			15		µs
t_{doffL}				0.5		µs
dV/dt	Source DMOS Slew-Rate (PWM)	see Fig. 3	10			V/µs
dV/dt	Source DMOS Slew-Rate (LIN)	see Fig. 3			1	V/µs
dV/dt	Sink DMOS Output Turn-off Slew-Rate	Note 3; R = 100KΩ		0.15		V/µs
F_C	Internal Clock Frequency			380		KHz
T_{off}	PWM Cutoff Time	R=100KΩ; C=180pF, Note 4; see Fig. 2	33	38	50	µs
T_{sd}	Shutdown Temperature			160		°C
T_{sdr}	Recovery Temperature			120		°C

Notes:

1) The Head Park time must be shorter than the Brake Delay time $t_{d(BRK)} = R_d C_d$
2) Both in PWM and in LIN mode the Ref. Voltage must agree to $V_{ref}=G_V R_S I_{motor}$
3) The resistance of the RC network defines the dv/dt value.
4) $t_{off} = 1.8RC + 6 \quad 10^{-6}$

Table 1

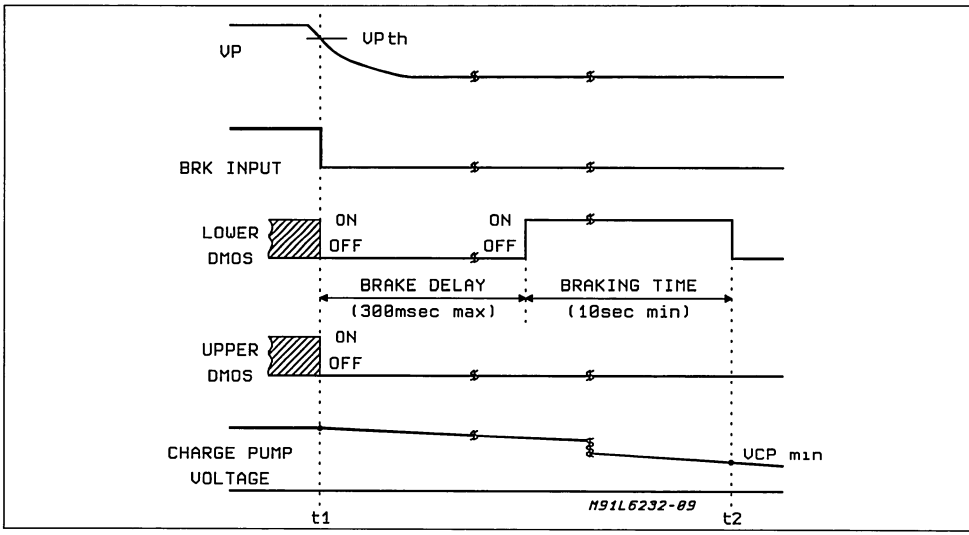
INPUT STATE						OUTPUT STATE		
INUA	INUB	INUC	INLA	INLB	INLC	A	B	C
L	L	L	H	H	H	*	*	*
L	L	L	L	L	L	H	H	H
H	H	H	L	L	L	*	*	*
H	H	H	H	H	H	L	L	L

H = The Upper DMOS is ON

L = The Lower DMOS is ON

* = Tristate condition

Figure 1: Brake Delay and Braking timing of the L6232A. At the time t1 a VP Powerdown threshold detector drives low the BRK input; at time t2 the Charge Pump voltage becomes inadequate to maintain ON the lower DMOS.



FUNCTIONAL DESCRIPTION (Refer to the Block Diagram)

The commutation sequence is provided by the user via six inputs. INUA,INUB,INUC turn on the three upper DMOS drivers when held at logic LOW, and inputs INLA,INLB,INLC turn on the three lower DMOS drivers when held at logic HIGH.

The BRK and BRK DLY inputs offer flexibility to the system designer in the implementation of the braking function. The BRK logic input, when pulled low will turn-off all upper and lower Dmos drivers. The low transition at BRK will produce a delayed negative transition at the BRK DLY input, configurable by connection of a capacitor Cd and a resistor Rd from the BRK DLY pin to ground. The negative transition at BRK DLY will initiate the braking of the motor by turning on all lower Dmos, while keeping all upper DMOS turned-off. This feature provides a time interval where the motor BEMF can be used to power the head parking function before the braking procedure is iniziated. External detection of the supply(VP) drop-off is necessary to provide the appropriate logic signal to the BRK input. (see Fig. 1)

The brake function utilizes the energy stored in the central charge pump capacitor (Cp) to turn-on or turn-off the DMOS drivers. This allows for completion of the braking procedure after the VP supply has powered down.

The L6232A is capable of driving the motor in either pulse width modulation (PWM) or linear (LIN) mode. The driving mode is determined by the smaller of two analog voltages inputs, LIN Vref and PWM Vref. The motor current is controlled by LIN Vref and PWM Vref and the current sense resistor Rs connected to the SENSE output. The SENSE output provides for connection of a resistor in series with the source of all lower DMOS drivers. The voltage at this pin provides the error signal wich is utilized internally to regulate the motor current Im. The current in both PWM and linear mode is determined by the expression :

$$I_m = \frac{V_{ref}}{G_V \cdot R_S}$$

in wich Gv is the voltage gain of the sense amplifier. In linear mode, the current is regulated by a linear control loop wich drives the lower DMOS. Compensation of the linear control loop is achieved by connection of a series network (Rc,Cc) from the transconductance amplifier output (Gm) and ground. Control is passed to each lower DMOS in succession during the commutation sequence(MPX).

The rate at which the upper and lower drivers turns-off during linear mode operation is configurable externally by the value of the resistor R used at the RC pin. This defines a current which is utilized internally to limit the voltage slew-rate at the outputs during transitions. The output slew-rate is internally adjusted for fast slewing during PWM operation to reduce losses, and a relatively slower rate during linear mode operation to minimize noise effects(EMI). LIN Vref and PWM Vref are connected to a comparator whose output is

fed to the logic . The upper and lower DMOS driver slew-rates are controlled by the internal logic.

In PWM mode, the upper driver is turned-off when the motor current reaches the intended value. An internal One-Shot pulse determines the lenght of time the upper driver stays off before turning on again. The pulse width, and thus the cutoff time (toff), is configurable by means of the external RC network connected to the RC pin. (see Fig. 2). The resistor at the RC pin, therefore determines both the driver output slew-rate during linear mode and the off-time constant during PWM. The lower driver is always on during PWM mode of operation; an on-chip 2µs mask can prevent the beginning of a new cutoff time because of transient current spikes caused by the upper drivers turn-on.

The driving mode is determined by the smaller of the two controlling input voltages. In a typical application the motor start-up would occur in PWM mode to limit power dissipation, with on-speed control then performed in linear mode.

Thermal protection circuitry will shut-off all drivers when the chip junction temperature exceeds the threshold temperature. A small amount of hysteresis is included to prevent rapid on/off cycling of the power stages.

Additional protection is provided against driver input combinations where the upper and lower drivers of a half bridge are turned on simultaneusly, resulting in a short from supply to ground. The chip logic will cause both the upper and lower drivers involved to turn-off. (see Table 1)

APPLICATION INFORMATION

A typical application configuration of the L6232A driving a three-phase brushless DC motor is shown in Fig.3. The spindle motor is a 4 ohm-2mH per phase, star connected. This load requires a suitable compensation of the linear control loop that can be achieved by Rc= 10 Kohm and Cc= 10nF (R3;C8). Changing the motor characteristics, the RcCc network would be modified for the best performances of the system. At the start-up the spindle is driven in PWM mode fixed toff time.

The off-time is calculated by the formula :

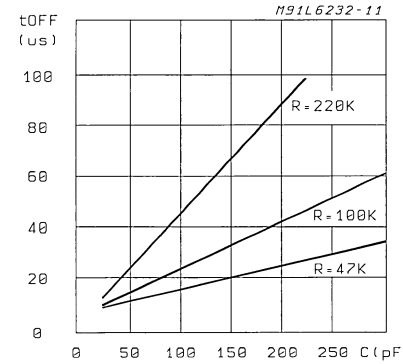
$$toff = 1.8\ R2\ C7 + 6 \cdot 10^{-6}$$

See fig.2 for a quick choice of the needed capacitor, after the resistor has been fixed. The value of the resistor defines the rate at which the upper and lower drivers turn-off during linear mode operation to avoid EMI effects. The PWM to linear mode of operation is switched by decreasing the LIN Vref level under the PWM Vref value that could be fixed and calculated by:

$$PWM\ Vref = 4\ Rs\ Ip$$

where Ip is the peak chopping current in the motor windings. Of course, when the required

Figure 2: Typical t_{off} vs. Capacity of C



RPM is reached, it become of no need a strong torque and the LIN Vref starting from a value higher than the calculated PWM Vref, decreases to the value :

$$LIN\ Vref = 4\ Rs\ Im$$

where Im, smaller than Ip, is the needed motor current to keep constant spin. This last reference voltage is generally a PLL output driven by speed transducers coupled to the spindle (like Hall effect sensors or BEMF processors). To drive the upper DMOS and during the brake function a voltage higher than the supply Vs is needed. The charge pump integrated in the L6232A keeps C3 at the correct voltage. To guarantee efficient braking of the motor , C3 must be chosen of adeguate quality (very high equivalent parallel resistance). C4 can be a ceramic disk capacitor . The typical application od the L6232A is in HDD systems on which there is the need to park the Read-Write Heads before the motor braking. This behavior is possible with the circuit of Fig.3. At Power Supply switch-off (see Fig. 1), VP falls down and drives down the BRK input (Active Low). D1 insulates the L6232A from the power suppy output while the power output stage is switched in a high impedance state. The spindle motor acting as a three-phase alternator supplies the Heads voice coil motor driven through integrated diodes that rectifie the EMF. After a delay longer than the parking time, the lower output DMOS are switched-on and the spindle motor is braked. The brake delay time is tipically 150 msec and it is defined by :

$$td(BRK) = R1\ C6$$

The sensing resistor value is generally lower than 1ohm, but a wire wounded type must be avoided. In Fig.3 the 0.33 ohm sensing resistor is shown as three parallel 1ohm metal film resistors. Care must be taken in the PC Board design particularly about ground loops and ground copper area. The typical Thermal Resistance junction to ambient versus PC Board copper area (Fig.5) is shown in Fig 6. For Transient Thermal Resistance see Fig. 7.

Figure 3: Typical Application Circuit

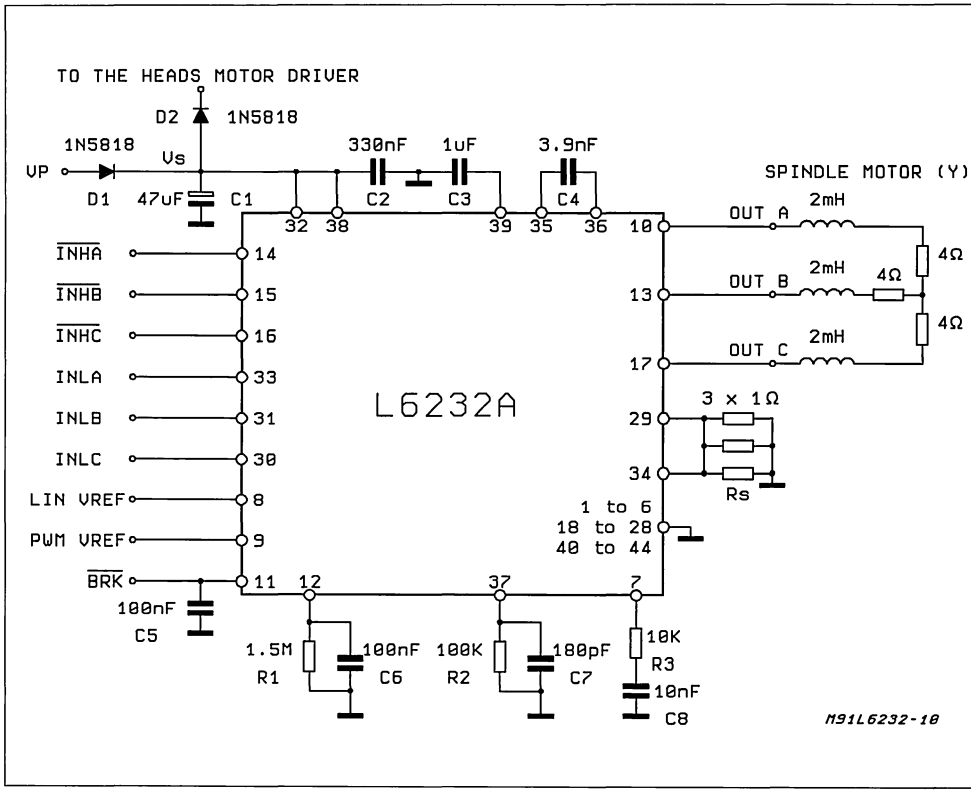


Figure 4: Typical Normalized $R_{DS\,(on)}$ vs. Junction Temperature

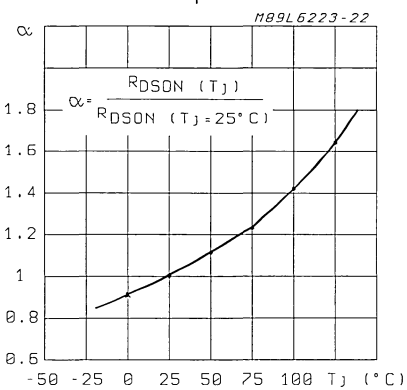


Figure 5: On Board Dissipation Copper Area Size

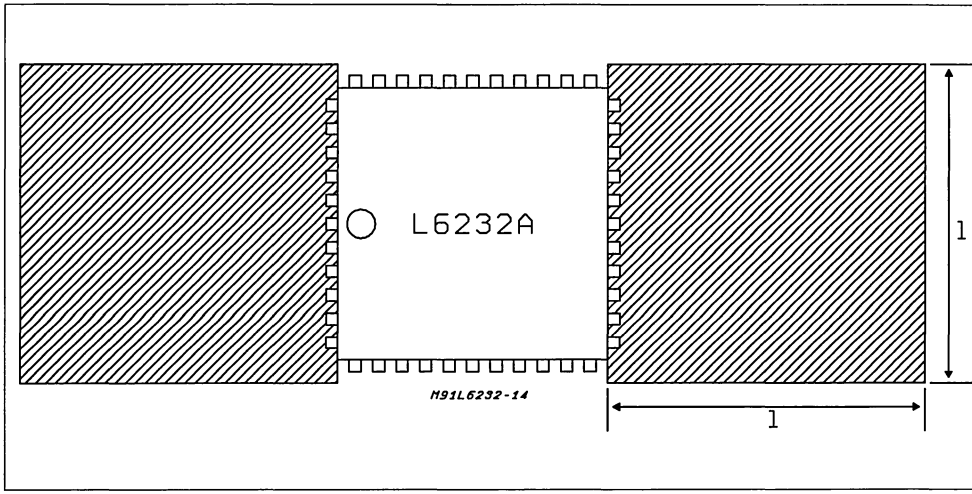


Figure 6: Typical $R_{th\ j\text{-}amb}$ vs. On-Board Heatsink Side l.

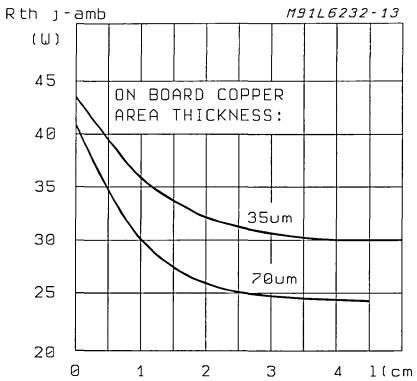
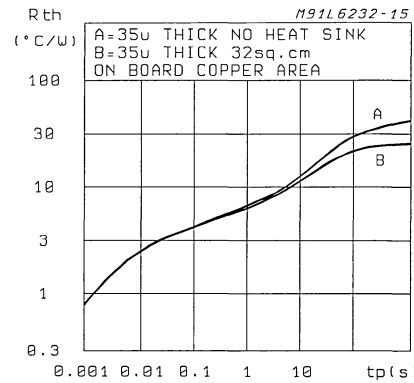


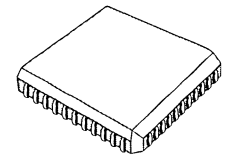
Figure 7: Typical Transient R_{th} in Single Pulse Condition.



VOICE COIL MOTOR DRIVER

PRODUCT PREVIEW

- 12V/5V OPERATION
- PARKING FUNCTION FOR HARD DISK HEAD ACTUATOR
- OUTPUT CURRENT UP TO 2A DC, 2.5A PEAK
- LOW SATURATION VOLTAGE
- LOGIC AND POWER SUPPLY MONITOR
- LINEAR CONTROL
- THERMAL PROTECTION
- ENABLE FUNCTION
- CURRENT SENSE RESISTOR CONNECTIONS



PLCC44 **SO(24+2+2)**

ORDERING NUMBERS:

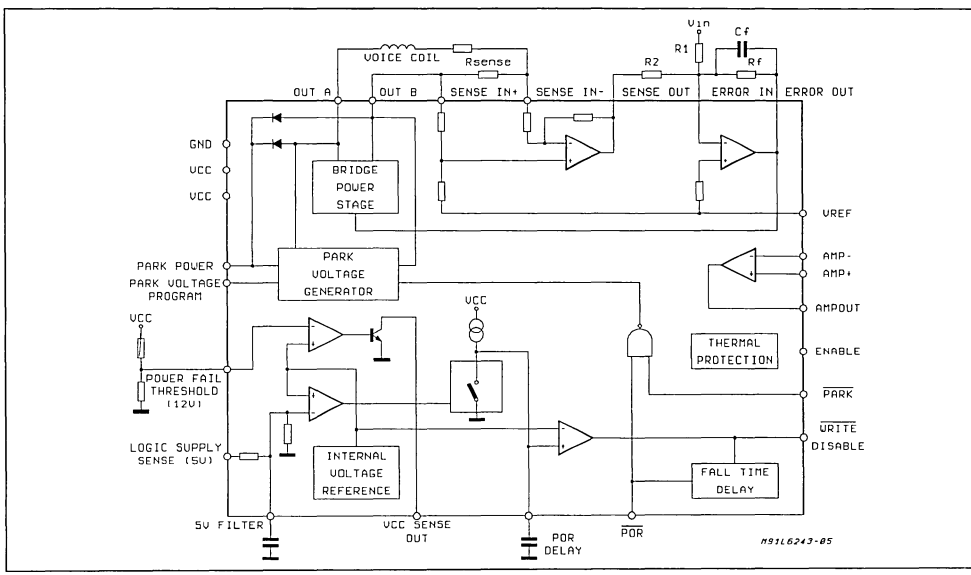
L6243 L6243D

DESCRIPTION

The L6243/D is a Bipolar IC developed for use in Hard Disk Head Actuator positioning applications. The Power Op-Amp Output Bridge, Differential Amplifier, and Error Amplifier, are controlled by TTL/CMOS, input compatible, Digital Logic, and an Analog Current Control Voltage. A simple RC compensation network, tied to the output of the Error Amp, will configure the system to work as a Transconductance Amplifier to drive a Voice Coil Motor in Linear Mode.

Additional features include Power On Reset Delay, Enable and Park, as well as a general purpose Operational Amplifier. A logic low at the Park input activates the parking function. Holding the Enable input low will disable the device by forcing the outputs into a tristate mode. Power Fail Monitors for the logic and power supplies initiate an automatic parking sequence during a power failure. A resistor programmed parking voltage enables a constant velocity head retract.

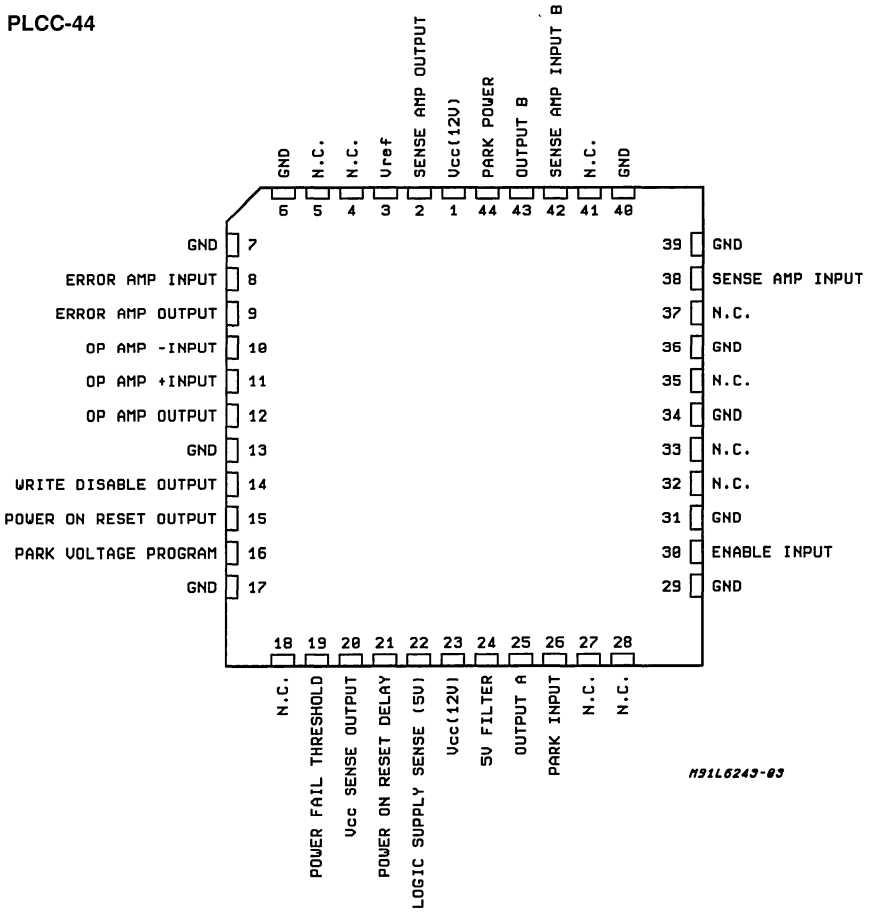
BLOCK DIAGRAM



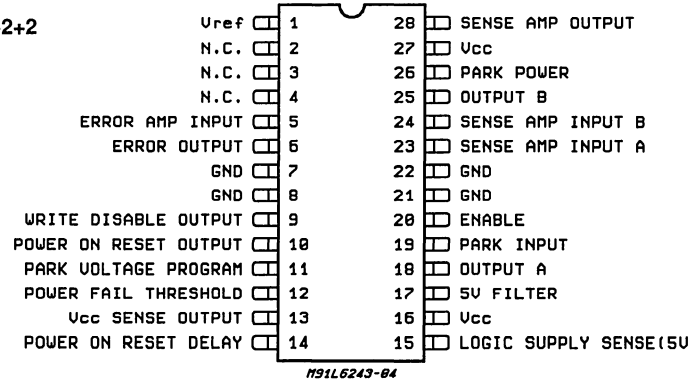
This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

PIN CONNECTION (Top view)

PLCC-44



SO 24+2+2



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	18	V
V_{IN}	Input Voltage	0.3V to V_S	
V_{ID}	Differential Input Voltage	$\pm V_S$	
I_O	DC Output Current	2	A
I_p	Peak Output Current (non repetitive)	2.5	A
P_{tot}	Total Power Dissipation (T_{amb} = 70°C) for L6243 for L6243D	2 1.2	W W
T_{stg}	Storage and Junction Temperature	-55 to +150	°C

THERMAL DATA

Symbol	Description	L6243	L6243D	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction to pin	12	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to pin floating in air	62		°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to pin 16 cm^2 copper area on board heat sink	36	50	°C/W

PIN FUNCTIONS

Name	Function
V_{CC}	Power supply.
GND	Common Ground.
V_{ref}	Voltage Reference.
ENABLE	Input. Logic low will disable IC.
PARK POWER	Input Power supply for the parking circuit.
CURRENT SENSE OUT	Current sense operational amplifier output.
ERROR AMP IN	Error amplifier inverting input.
ERROR AMP OUT	Error amplifier output.
SENSE IN ±	Input for external sense resistors.
OUT A, B	Outputs of the two Power Operational Amplifiers Connections for Voice coil Motor.
PARK	External input for parking. Low will activate the park procedure.
PARK VOLTAGE PROGRAM	Input to set the park voltage.
POWER FAIL THRESHOLD	Supply monitor threshold setting.
LOGIC SUPPLY SENSE	Logic Supply Sense.
5V FILTER	Capacitor connection to filter the logic supply ripple.
V_{CC} SENSE OUT	Power supply failure monitor output.
POR	Power on reset output. Low will signal to the controller the failure of the logic supply.
POR DELAY	Capacitor connection to set the power on reset delay.
WRITE DISABLE	Output for write disable. Low will disable the writing mode.
AMP–	Inverting input of the additional op amp.
AMP+	Non-inverting input of the additional op amp.
AMPOUT	Output of the additional op amp.

ELECTRICAL CHARACTERISTICS (V_S = 12V, T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Range		4.5		13.2	V
I_d	Quiescent Drain Current			20		mA
T_j	Thermal Shutdown Junction Temperature			160		°C

ERROR AMPLIFIER

I_b	Input Bias Current				1	µA
I_{OS}	Input Offset Current				300	nA
V_{OS}	Input Offset Voltage				5	mV
Gv	Large Signal Open Loop Voltage Gain		70			dB
GBW	Gain Bandwidth			3		MHz
G_{min}	Minimum Voltage Gain		5			
I_{O+}	Output Source Current			6		mA
I_{O-}	Output Sink Current			6		mA
SR	Slew-rate			2		V/µs

SENSE AMPLIFIER

R_{IN}, V_{ref}	V_{ref} Input Impedance		9			KΩ
A_d	Differential Gain			8		V/V
SR	Slew-rate			1		V/µs
GBW	Gain Bandwidth Product			3		MHz
R_{in}	Sense Input Impedance		1.5			KΩ
CMRR	Common Mode Rejection Ratio		60			dB

POWER OP. AMP.

G_V	Voltage Gain			26		dB
V_d	Total Output Voltage Drop	I_O = 1A I_O = 2A			1.8 2.5	V V
V_{off}	Offset Voltage on Sense Resistor			5		mV
BW	Bandwidth on Resistive Load			100		KHz

GENERAL PURPOSE OP-AMP

I_b	Input Bias Current				1	µA
I_{OS}	Input Offset Current				300	nA
V_{OS}	Input Offset Voltage				5	mV
G_V	Large Signal Open Loop Voltage Gain		70			dB
GBW	Gain Bandwidth Product			1		MHz
I_{O+}	Output Source Current			6		mA
I_{O-}	Output Sink Current			6		mA
SR	Slew Rate			1		V/µs

ELECTRICAL CHARACTERISTICS (continued)
MONITORS AND CONTROL CIRCUIT

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{t1}	Threshold Voltage at Logic Supply Sense		4.45	4.60	4.75	V
V_{t2}	Threshold Voltage at Power Fail Threshold Input		1.375	1.4	1.425	V
HV_{t1}	Hysteresis on V_{t1}			50		mV
HV_{t2}	Hysteresis on Vt2			15		mV
V_{ll}	Low Level Voltage	Write Disable = 2mA		250	500	mV
		Power on Reset = 2mA		250	500	mV
I_e	Enable Input Current	V_i = 2.4V			100	µA
		V_i = 0.4V			–200	µA
I_p	Input Current at Park	V_i = 2.4V			100	µA
		V_i = 0.4V			–200	µA
R_f	Equivalent Input Resistance at 5V Filter Input			6.9		KΩ
V_{enl}	Enable Low Input Voltage				0.8	V
V_{enh}	Enable High Input Voltage		2			V
V_{ph}	Parking Input High Voltage		2			V
V_{pl}	Parking Input Low Voltage				0.8	V
V_{pfl}	Power Fail Low Output Voltage	I_l = 2mA			0.5	V
V_{pfh}	Power Fail High Output Voltage	I_l = –440µA	2.4			V
I_{prog}	Parking Voltage Program Current			100		µA
I_{ch}	Power On Reset Delay Capacitor Charging			10		µA
T_d	Delay Between Write Disable and Power on Reset Falling Edges			4	10	µs

FUNCTIONAL DESCRIPTION

The VCM Driver is controlled via three control signals, ENABLE, POWER ON RESET, and WRITE DISABLE. An analog input voltage, ERROR AMP IN, controls the polarity and amplitude of the VCM driving current.

Refer to figure two. This diagram is a representation of the function of the VCM System. Note that the signals with the bars represent the "not true", or "non asserted" condition. From initial power up, the system is held in the Park Mode. Upon completion of the POWER UP RESET DELAY the machine moves to Tristate Mode or Run Mode, depending upon the condition of the ENABLE input. If ENABLE is asserted, the machine moves directly to Run Mode. If ENABLE is not asserted, the machine moves to Tristate Mode.

POWER ON RESET is an asynchronous output. Additionally it affects the internal logic as a hard wired reset and therefore if a supply failure occurs during Tristate or Run state, the machine moves directly back to a few the Park Mode. A WRITE DISABLE occurs five to ten microseconds prior to the POWER ON RESET in order for the system to halt any read/write activity before a head retract begins.

While in Tristate Mode, the assertion of ENABLE will move the machine to the Run Mode. Run Mode will typically be the steady running state. The deassertion of the ENABLE signal causes the machine to move into Tristate. If it is desired to perform an active Parking function, the PARK input must be driven low by the external hardware, or the the VCM can be driven to the Park position via the ERROR AMP IN control voltage

FUNCTIONAL DESCRIPTION (continued)

Function	Description
V_{CC} input	This is the Power Supply input. An internal sense is done monitor this supply. A POWER ON RESET is asserted if the Vcc supply drops below the programmed threshold.
POWER FAIL THRESH	Input for the V_{CC} supply monitor. The Threshold can be externally set via a voltage divider.
V_{CC} SENSE OUT Output	TTL compatible signal indicating the V_{CC} supply has dropped below the POWER FAIL THRESHOLD.
LOGIC SUPPLY SENSE input	This input is used to monitor the Five Volt LOGIC SUPPLY SENSE Logic Supply for the external control and other support IC's. The LOGIC SUPPLY SENSE operates independently of the 12V Power Supply. When a 5V supply failure is detected a POWER ON RESET is generated.
5V FILTER input	This pin allows for the application of filter circuitry in order to avoid false triggering.
PARK POWER input	This input is used during the Power Down/Power Fail Parking operation. When the supply goes down, a typical Spindle Driver Circuit automatically tristates its output stages. During this time the spindle motor spins freely and the stored energy is used to drive the VCM to the park position. The generated BEMF is rectified and filtered across an external PARKING CAPACITOR.
PROGRAMMABLE PARK VOLTAGE input	Used to set the voltage applied to the VCM during an Automatic Parking Operation.
PARK input	Logic signal asserted low, activates parking.
POWER ON RESET output	Indicates an error condition to the external control and support circuitry. A Logic Supply Fail condition automatically initiates a POWER ON RESET.
POWER ON RESET DELAY input	The intent of this input is to provide a time delay at power up. During this time, the POWER ON RESET line will be asserted (low). A POWER ON RESET, will hold the system in the PARK mode. Once the delay has timed out, the POWER ON RESET will be removed to allow the external system to assume control. When applied in a Disk Drive Application, the POWER ON RESET DELAY will be required to have a minimum duration which will ensure that the Read/Write Heads can be fully parked.
WRITE DISABLE output	Becomes asserted five to ten microseconds prior to the assertion of POWER ON RESET.
ENABLE input	This signal originates at the external controller and, when asserted, allows the VCM Drivers to operate. When deasserted the VCM Driver is forced into Tristate mode. During a POWER ON RESET condition however, the parking operation is automatic and takes priority over the ENABLE function. Only at the end of the POWER ON RESET DELAY will the ENABLE input become active. If active parking is desired, it will be accomplished under control of the V_{IN} signal, otherwise it is an automatic function at power down.
V_{REF} input	The reference voltage input is basically that voltage, at which the output current is zero.
ERROR AMP IN input	Inverting input of error amplifier. The non inverting one is internally tied to V_{ref}.
ERROR AMP OUT output	Error amplifier output pin.
OUTPUT A power output	Voice Coil power output.
OUTPUT B power output	Voice Coil power output.
SENSE AMP IN A/B signal input	Sense amplifier input pins. The sense resistor is connected across these pins.
SENSE AMP OUT signal output	Output pin of sense amplifier.
AMPOUT output	Output of an internal op-amp for general application.
AMP+ input	Non inverting general purpose op-amp input.
AMP- input	Inverting input general purpose op-amp input.

BLOCK DESCRIPTION

OUTPUT STAGE

It consists of two Power Op Amps connected in bridge configuration.

CURRENT SENSE AMPLIFIER

Differential amplifier whose inputs are connected to the sense lines and whose output is accessible externally. Closing the loop will transform the differential voltage signal from the sense lines into a current signal for the Error Amplifier.

ERROR AMPLIFIER

Error amplifier which drives the output stage. The input and the output pins are accessible externally.

POWER SUPPLY MONITOR OPERATION

The circuit monitors the logic supply voltage input (typ 5V) and activates Power on Reset and Write Disable output when such a supply drops below the safe operating limit. After the logic supply voltage reaches its nominal value a delay capacitor has to be charged [Tdelay=3x10e5 x C sec] before Power on Reset and Write Disable outputs change from low to high level. Falling edges of Write Disable and Power on Reset are delayed (typ 4µs) in order to disable the writing on the disk before the Power on Reset is activated. An additional supervisor circuit is present in the IC with a programmable threshold, which is set by an external resistive divider. The TTL compatible output can be used separately or connected to Park input in order to park the head.

The V_{CC} sense output pin can also be connected to 5V filter input in order to implement a POWER ON RESET function sensitive both to 5V and V_{CC}.

PARKING CIRCUIT OPERATIONT

The voice coil driver is switched into the parking condition when Power on Reset output or Park input are low. In such a condition a fixed voltage is superimposed on the load and the value of such a voltage is set by connecting an external resistor between Park Voltage Program input and ground: (Vpark=Rext x Iref, Iref=100µA typ). Connecting ENABLE input to GND the driver will be disabled (outputs in high impedance mode).

THERMAL SHUTDOWN

It will disable the IC when the junction temperature exceeds the threshold value above which the device could be damaged.

Figure 1: Application Circuit

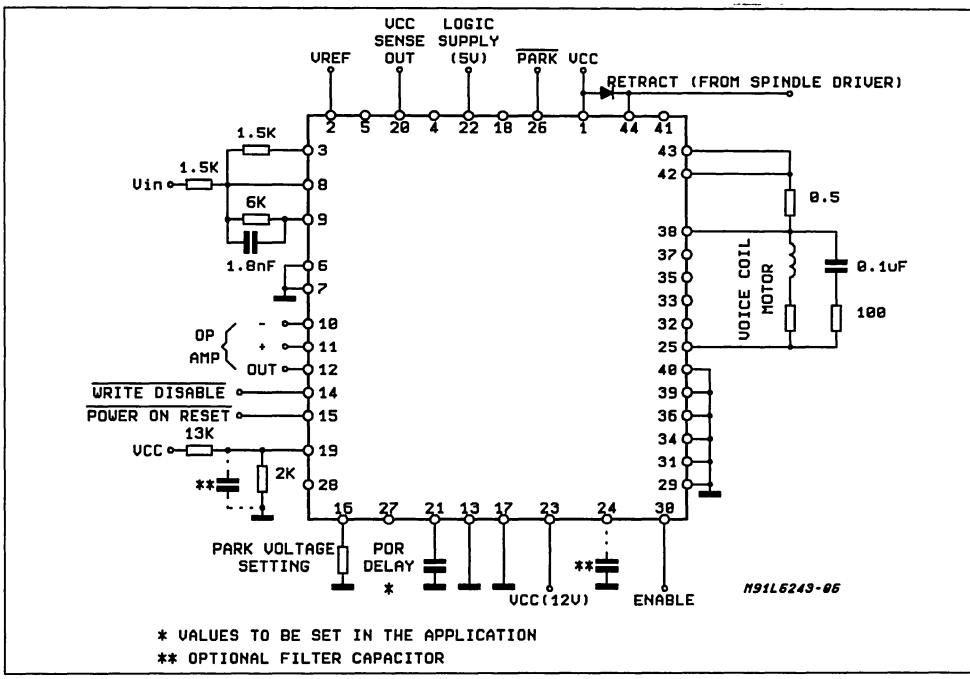
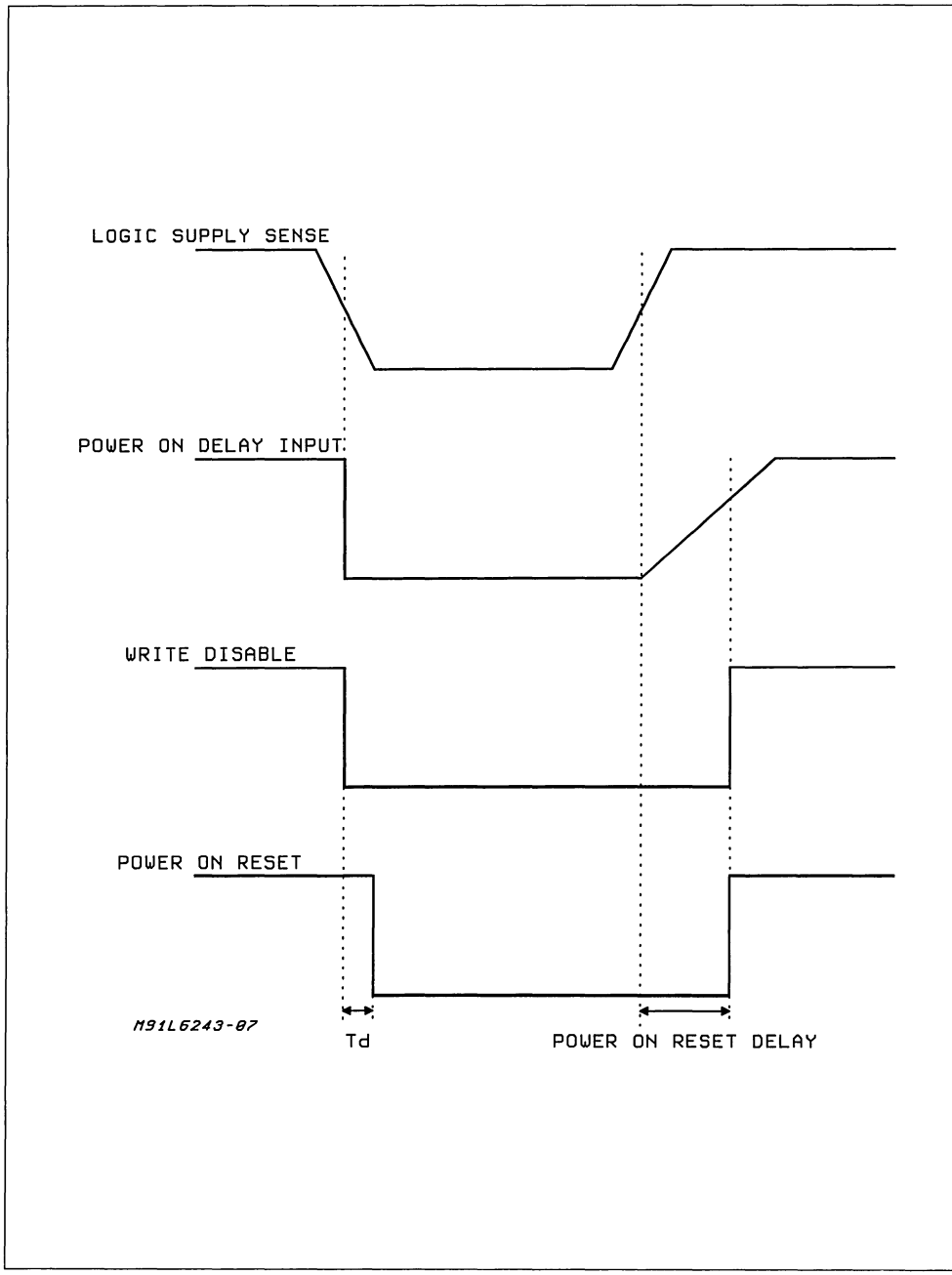


Figure 2: Waveforms



THERMAL CHARACTERISTICS

Figure 3: $R_{th\ (j\text{-}amb)}$ vs. Dissipated Power

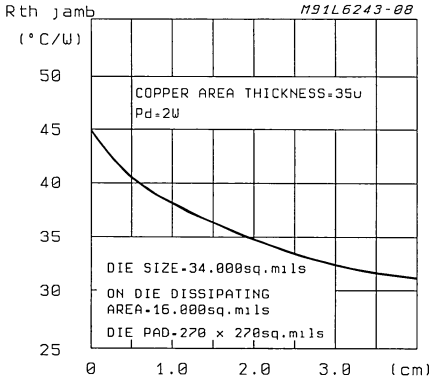
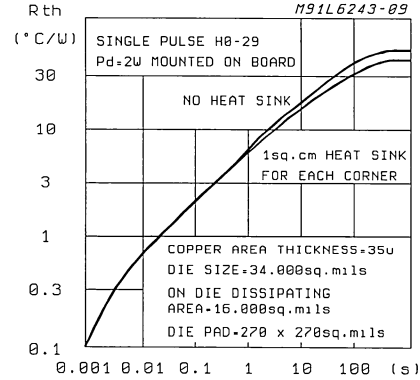


Figure 4: $R_{th\ (j\text{-}amb)}$ vs. Dissipated Power



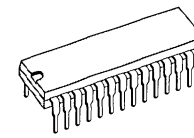
SGS-THOMSON MICROELECTRONICS

L6603
L6604

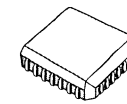
MEMORY CARD INTERFACE

ADVANCE DATA

- Single Power Supply operation
- Internal Clock Generator or External Clock Input
- Adjustable Precision of PVS Output Voltage (2%)
- 100mV/step of the Writing Output Voltage
- I/O, Reset and Clock Outputs Protection Against Short Circuit to GND and to V_{pvs}.



DIP28
ORDERING NUMBER: L6603

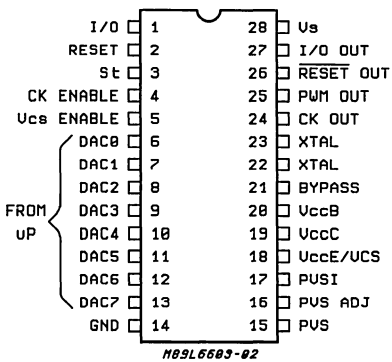


PLCC-28
ORDERING NUMBER: L6604

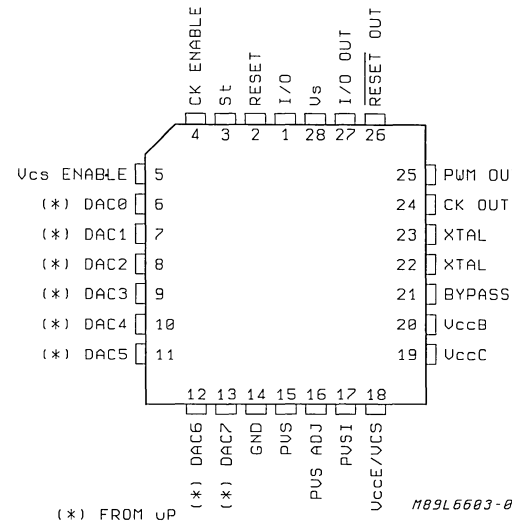
DESCRIPTION

The L6603 and L6604 are integrated circuits for applications as interface between different types of memory card and a microprocessor which exchanges data with cards. It operates with a single power supply.

PIN CONNECTIONS



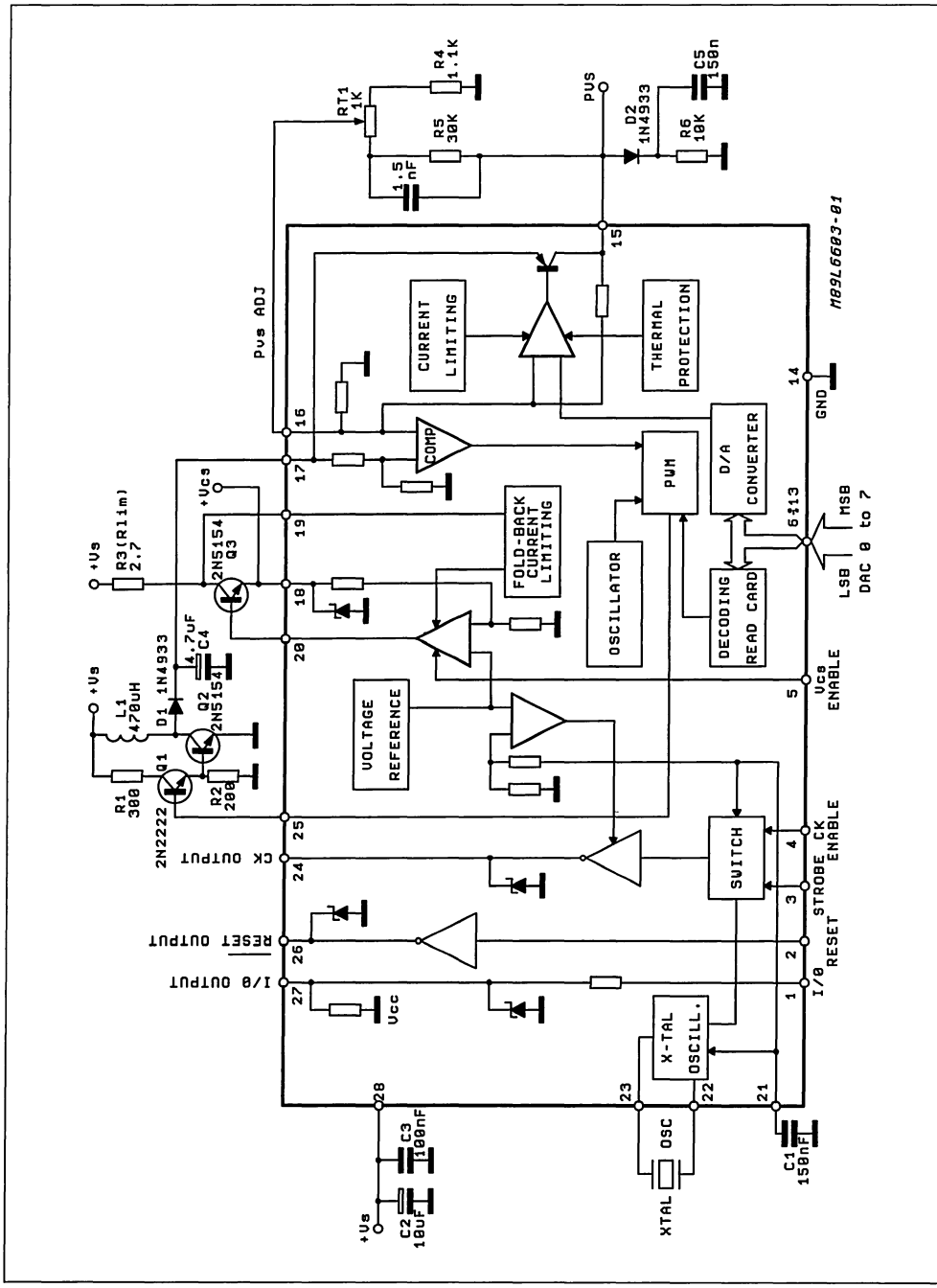
DIP-28



PLCC-28

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice.

BLOCK DIAGRAM AND FUNCTIONAL TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Supply Voltage	11	V
T_{op}	Operating Temperature Range	-20 to 70	°C
T_{stg}	Storage Temperature Range	-40 to 150	°C

THERMAL DATA (*)

			DIP 28	PLCC 28	
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	100	°C/W

(*) With all the pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

Pin	Name	Function
1	I/O	Input of the Bidirectional Data Line
2	Reset	Control Input for Reset for Cards with µP and Memory
3	St	Strobe for Cards with Memory (TTL compatible)
4	CK ENABLE	Commutation for µP Cards CK ENABLE = 1 (internal clock)
5	VCS ENABLE	Control Input for VCS Supply Voltage for the Card
6 to 13	DAC0 to DAC7	Control Inputs for Programmation of V_{PVS} Supply (see Application Information)
14	GND	Ground
15	V_{PVS}	Programmable Supply for Memory Card (no use with decoupling capacitor) Note 7 (to the card)
16	V_{PVS} Adj	Adjustment Input for 2% Precision V_{PVS} Output
17	PVS I	Input for V_{PVS} Voltage Regulator
18 19 20	V_{CS} V_{CC} E C B	Inputs for Connection of Power Transistor (V_{CS} regulator) (decoupling capacitor on pin 18 <100nF if necessary) Note 8 (pin 18 to the card supply)
21	BYPASS	Reference Output Voltage (decoupling capacitor > 150nF). Note 9
22, 23	XTAL	Inputs for X-tal Connection. Note 10
24	CK OUT	Output for Clock Signal (TTL levels). Note 11 (to the card)
25	PWM OUT	Output for DC/DC Step-up Converter
26	$\overline{\text{RESET}}$/OUT	Reset Output. Note 11 (to the credit card)
27	I/O Out	Output I/O. Note 11 (to the card)
28	V_S	Power Supply (Note 12)

ELECTRICAL CHARACTERISTICS (V_S = 8.5V; Tj = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
V_{IH}	Input High Voltage		2			V	1
V_{IL}	Input Low Voltage				0.8	V	1
$\lvert I_{IH} \rvert$	Input High Current				250	µA	2
					500	µA	3
					100	µA	4
					400	µA	5
					200	µA	6

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
$\lvert I_{IL} \rvert$	Input Low Current				150	µA	2
					300	µA	3
					10	µA	4
					200	µA	5
					300	µA	6
I_{SW}	Supply Current Writing Mode (pin 28)	$V_{PVS} = V_{PVSW\ max}$		40	50	mA	13
I_{SR}	Supply Current Reading Mode (pin 28)	$V_{PVS} = V_{PVSR}$		40	50	mA	13
I_{stby}	Stand by current (pin 28)	All functions inhibited		35	50	mA	13
V_{CS}	Output Voltage Range	V_S = 7 to 10V; I_{CS} = 0 to -150mA; T_{amb} = -20 to 70 °C	4.8	5	5.2	V	8; 13
$\frac{\Delta V_{CS}}{V_{CS}}$	Load Regulation	I_{CS} = 0 to -150mA		0.18		%	13
$\frac{\Delta V_{CS}}{V_{CS}}$	Line Regulation	V_S = 7 to 10V		-50		dB	13
$\frac{\Delta V_{CS}}{\Delta T}$	Temperature Coeff. of Output Voltage V_{CS}	T_{amb} = -20 to 70 °C		65		dB	
t_{off1}	Fall Time of V_{CS}	Fig. 1; C_L = 30pF; I_{CS} = -30mA			200	µs	13
t_{off2}	Fall Time of V_{PVS}	Fig. 1 C_L = 30pF Write to Read	$\frac{V_{PVS}\ (V)}{2V/\mu s}$		200	µs	13
$\lvert I_{CS\ max} \rvert$	Maximum Operating Current	V_{CS} -4% V_{CS}	180			mA	8; 13
$\lvert I_{CSL} \rvert$	Short Circuit Current limit			70	100	mA	8; 13
$V_{PVSW\ max}$	Maximum Programming Voltage (writing mode memory)	V_S = 8 to 10V; I_{PVS} = 0 to -30mA	24.5	25.5	26.5	V	13
V_{PVSW} max	Maximum Programming Voltage (writing mode memory)	V_S = 7 to 10V; I_{PVS} = 0 to -40mA	20.15	21	21.85	V	13
V_{PVSW} min	Minimum Programming Voltage (writing mode memory)	V_S = 7 to 10V; I_{PVS} = 0 to -50mA	4.9	5.1	5.3	V	13
V_{PVSR}	Output Voltage Range of PVS (reading mode memory)	V_S = 7 to 10V; I_{PVS} = 0 to -20mA	4.8	5	5.2	V	13
$\frac{\Delta V_{PVS}}{V_{PVS}}$	Load Regulation	I_{PVS} = 0 to -30mA @ V_{PVS} = 25.5V; I_{PVS} = 0 to -40mA @ V_{PVS} = 21V; I_{PVS} = 0 to -50mA @ V_{PVS} = 5.1V; Writing Conditions		0.8		%	13
$\frac{\Delta V_S}{\Delta V_{PVS}}$	Line Regulation	I_{PVS} = 0mA; V_S = 7 to 10V		50		dB	13
$\frac{\Delta V_{PVS}}{\Delta T}$	Temperature Coeff. of Output Voltage V_{PVS}	I_{PVS} = 0 mA, T_{amb} = -20 to 70 °C		74		dB	
$\lvert I_{PVS\ max} \rvert$	Short Circuit Current Limit		50	70	100	mA	13
V_{PVS} ADJ -V_{CS}	Differential Voltage between V_{PVS} (reading mode) & V_{CS}		-5		5	%	13
t_{pLH1}	Turn ON Time of V_{CS}	Fig. 1 C_L = 30pF			1	ms	
t_{pLH2}	Turn ON Time of VPVS	Fig. 1 CL = 30pF		50	200	µs	13

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
t_{on1}	Rise Time of V_{CS}	Fig. 1 C_L = 30pF			200	µs	13
t_{on2}	Rise Time of V_{PVS}	VPVS = 5 to 25.5V; Fig. 1 C_L = 30pF			200	µs	13
V_{OH1}	High Output Voltage (pin 26)	(pin 26) VCSmin I_{OH} = -200µA	4.2	4.8		V	
V_{OL1}	Low Output Voltage (pin 26)	(pin 26) VIH = 2V I_{OL} =+200µA		0.15	0.4	V	
V_{SC1}	Max Output Voltage during Short-circuit between V_{PVS} and pin 26				V_{CS} +0.3	V	
$\mid I_{SC2} \mid$	Short-circuit Current Limit (pin 26)				0.5	mA	
V_{OH2}	High Output Voltage (pin 27)	VCSmin I_{OH} = -500µA V_{IHmax} = 2V	1.9			V	
V_{OL2}	Low Output Voltage (pin 27)	V_{CSmax} I_{OL} = 200µA V_{IHmin} = 0.8V			1	V	
V_{SC2}	Max Output Voltage during Short-circuit between VPVS and Pin 27				V_{CS} +0.3	V	
$\mid I_{SC3} \mid$	Short-circuit Current limit (pin 27)	I/O = 4.2V			30	mA	
V_{OH3}	High Output Voltage (pin 24)	I_{OH} = -200µA	3.5	4.1		V	
V_{OH4}	High Output Voltage (pin 24)	I_{OH} = -10µA	4.1	4.2		V	
V_{OL3}	Low Output Voltage (pin 24)	I_{OL} = 200µA		0.1	0.4	V	
V_{SC3}	Max Output Voltage during Short-circuit between Pin24 & V_{PVS} Output				V_{CS} +0.3	V	
$\mid I_{SC4} \mid$	Short-circuit Current Limit (pin 24)				35	mA	
t_{on}	Rise Time of Clock Output (pin 24)	Fig. 2 f_{XTAL} = 4.91MHz C_L = 30pF		15		ns	
t_{off}	Fall Time of Clock Output (pin 24)	Fig. 2 fXTAL = 4.91MHz C_L = 30pF		18		ns	
	Duty Cycle (T1/T)	f_{XTAL} = 4.91MHz C_L = 30pF		50		%	

Note 1: For inputs V_{CS} enable, Reset, I/O, St, CK enable DAC (0-7)
Note 2: For inputs DAC (0-7), I_{IH} is forward; I_{IL} is coming out.
Note 3: For input CK enable; I_{IH} is forward; I_{IL} is coming out.
Note 4: For input Reset; I_{IH} and I_{IL} are both forward
Note 5: For input V_{CS} enable, I_{IH} is forward; I_{IL} is coming out.
Note 6: For Input I/O; I_{IH} and I_{IL} are both coming out.
Note 7: Internal thermal protection & current limiting system (see Block Diagram)
Note 8: Current limiting with "fold back system" (fig. 4)
Note 9: Internal current limiting system
Note 10: Input for external clock (fig. 3)
Note 11: Output protected against short-circuit to ground and to V_{PVS}
Note 12: The V_{CS} Voltage Regulator and the DC/DC step-up converter must be supplied with the same voltage.
Note 13: See functional Test Circuit

APPLICATION INFORMATION

Operation of Programming Supply V_{PVS}

The output voltage VPVS can be programmed from 5V to 25.5V by steps of 0.1 V and can be expressed as follows:

$$V_{VPS} = \frac{\text{Decimal value of code DAC0–7}}{10}$$

Writing mode (Decimal value of code 51 to 255):
V_{PVS} = 5.1 to 25.5V
In the latter case, the voltage drop between output of converter DC/DC (PVSI) and V_{PVS} is constant and typically of 3V.

The Decimal Value of an 8bit word is computed as it follws:

X	X	X	X	X	X	X	X	Word (DAC0-7)
7	6	5	4	3	2	1	0	Bit (n)

0	0	0	0	0	0	0	0	If X = L (*)
128	64	32	16	8	4	2	1	2^n if X = H (*)

(*) Corresponding Decimal Value

When V_{PVS} is requested to be of 21V the Decimal Value of Code DAC 0to7 is 210, that is obtained by:

128+ 64+ 0+ 16+ 0+ 0+ 2+ 0

Then the word is the following:

H	H	L	H	L	L	H	L	From µP

The throuth table of C_{Kout} is the following:

Strobe (pin 3)	$C_{Kenable}$ (pin 4)	C_{Kout} (pin 24)
H	L	L
L	L	H
X	H	Clock

Figure1: V_{CS} (V_{CC}) and V_{PVS} (V_{PP}) Times test sequence

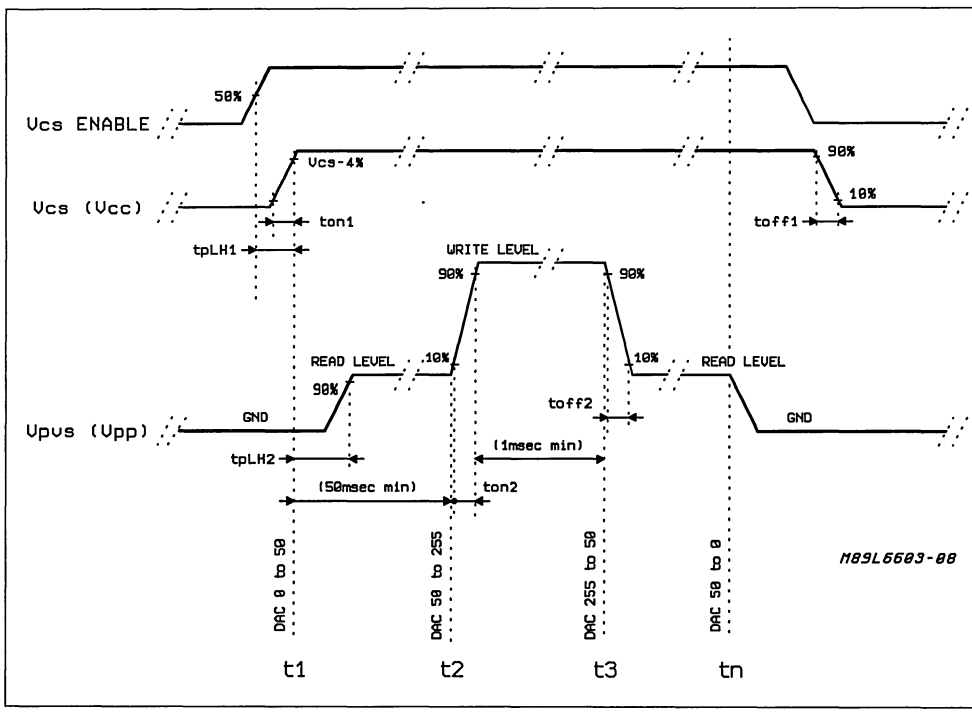


Figure 2: Clock Output Waveform and Times

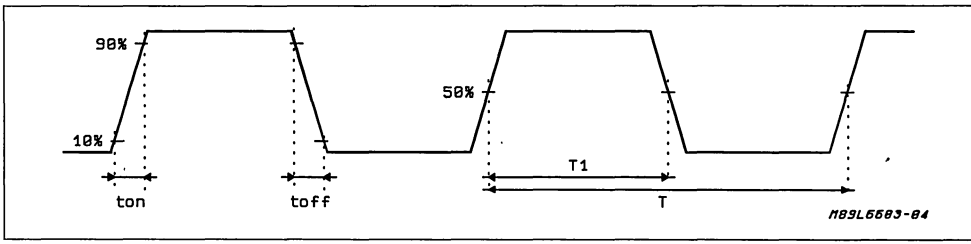


Figure 3: Input for External Clock

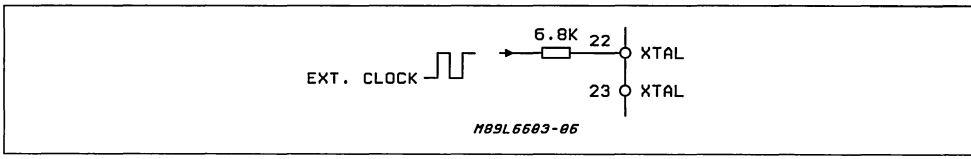
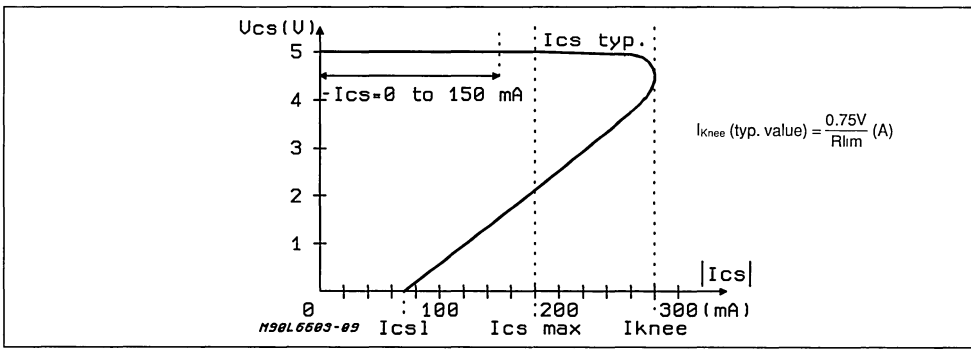


Figure 4

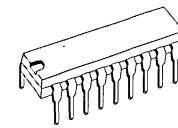


SMART CARD INTERFACE

PRODUCT PREVIEW

- 8 DIFFERENT V_{PP} OUTPUT VOLTAGE LEVELS
- V_{PP}, V_{CS} RISE AND FALL TIME FULL SPEC WITH ISO/IEC 7816-3
- POWER SUPPLY OUTPUT FOR MEMORY CARD (5V/80mA)
- POWER ON/OFF RESET
- V_{PP}, V_{CS} SHORT CIRCUIT PROTECTIONS
- INTERNAL STATUS FAILURE CODING
  - SHORT CIRCUIT CODE
  - INSERTION FAILURE CODE
  - OVERTEMPERATURE FAILURE
- ANTI-BOUNCING SYSTEM
- INPUT/OUTPUT LOGIC TTL COMPATIBLE
- THERMAL PROTECTION

Multipower BCD Technology



Powerdip 12+3+3

DESCRIPTION

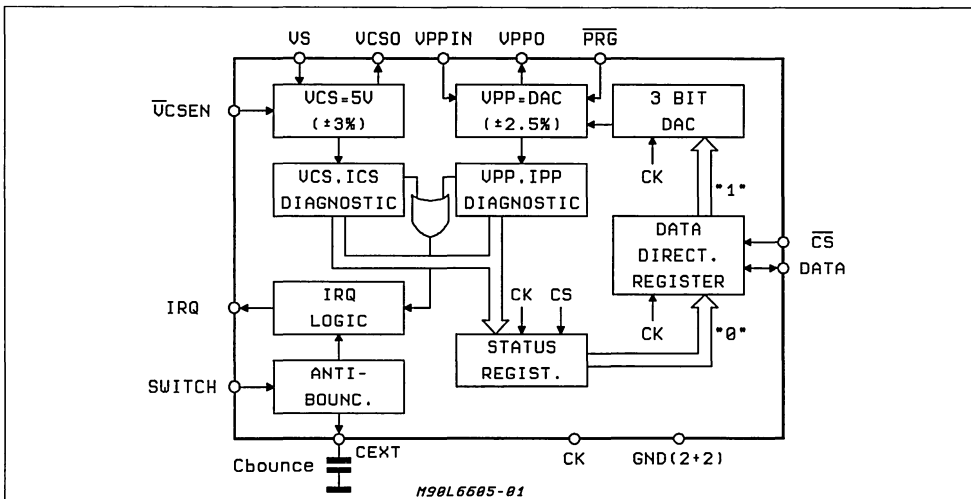
The L6605 is an IC dedicated as intelligent interface between different types of smart cards and microprocessors. The internal architecture can be shared in a power supply section and in a diagnostic parts.

The power supply section can deliver in output 5V/80mA to supply the card and V_{PP}/50mA to write the memory inside the card; the V_{PP} voltage can be programmed by means of the 3 serial input bit (see TAB, 1).

Table 1: 3 bit DAC CODE

CODE	V_{PP}
0 0 0	5V
0 0 1	10V
0 1 0	12.5V
0 1 1	13.5V
1 0 0	15V
1 0 1	18V
1 1 0	21V
1 1 1	25V

BLOCK DIAGRAM



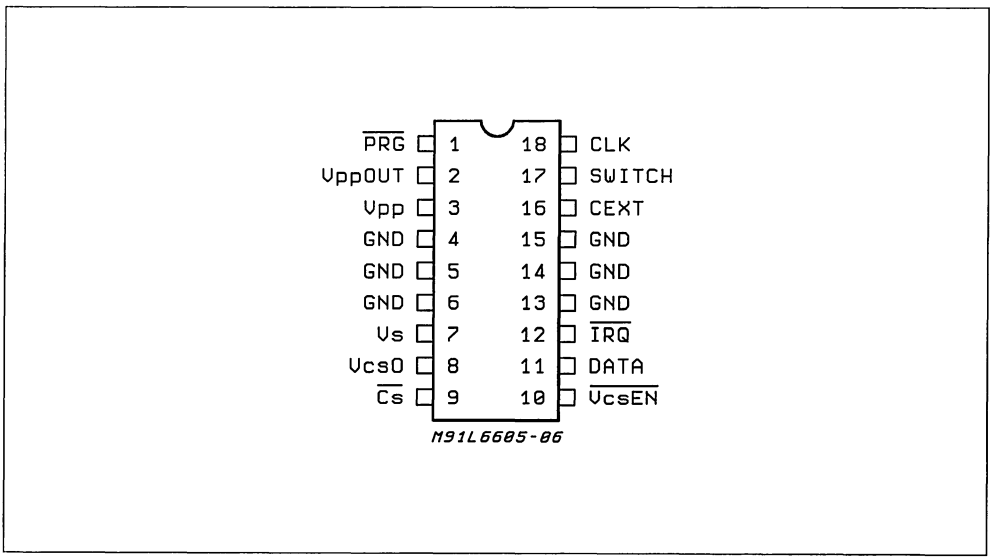
This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

DESCRIPTION (continued)
The diagnostic part allows to monitor failures due to overcurrent, overtemperature or wrong card positioning. The failures are internally coded and readable inside the STATUS REGISTER through the bidirectional pin DATA configurated in output. The antibouncing circuitry, active during card insertion only, rejects ripetitive switching-on of the power supply sections.

PIN FUNCTION

Pin	Description
V_S	Input Power Supply voltage for V_{CS} regulated output and for device supply
V_{CSO}	Output regulated voltage for card supply; I_{CSmax} = 80mA; overload protected (81 to 200mA)
V_{PPIN}	Input power supply for V_{PP} regulated voltage
V_{PPOUT}	Programmable output regulated voltage for memory card writing; 8 voltage levels are allowed by means of 3 bit DAC. I_{PPmax} = 50mA
$\overline{V_{CSEN}}$	Active Low) VCS supply input enable; Its value is fixed from the µP allowing or not the normal R/W operations on the card
SWITCH	Input signal produced by the reader system indicating that a card has been inserted. Internally, an antibounding system is provided to avoid multiple switching.
$\overline{CS}$	Chip select (active low) $\overline{CS}$ low level indicates an I/O operation request from µP
IRQ	Interrupt Request (Active low). An IRQ low level indicates that a card insertion extraction or Failure has occured.
$\overline{PRG}$	Program Active low). PRG low level enables L6605 to deliver in output the V_{PPO} level set by 3 bit DAC.
DATA	I/O pin for data exchange between µP and the device. Through this pin flow 3 bit input DAC or 2 bit STATUS REGISTER code.
CK	External clock
C_{EXT}	Pin to connect an external capacitor for antibouncing delay time.
GND	4 pins to ground

PIN CONNECTION (Top view)



ELECTRICAL CHARACTERISTICS (V_S = 12V; T_j = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		10	12	15	V
V_{CS}	Card Supply Voltage (Logic Inputs onset)	I_{CS} = 80mA, V_S = 12V	4.85	5	5.15	V
		I_{CS} = 1mA to 80mA V_S = 10V to 15V	4.75	5	5.25	V
I_{CS}	Current Supply Card				80	mA
I_{CSS}	I_{CS} Short Circuit	VS = 12V	81		200	mA
V_{PPI}	V_{PP} Supply Voltage		V_{PPO} + 2.5V		33	V
V_{PPO}	Programming Voltage	I_{PP} = 50mA; V_{PPI} = 30V; $T_{on} \leq$ 5ms	-2.5%	V_{DAC}	+2.5%	V
		I_{PP} = 1mA to 50mA V_{PPI} = max. 33V (see note 1)	-5%	V_{DAC}	+5%	V
I_{PP}	Output Program. Current	V_{PPI} = 30V			50	mA
I_{PPS}	I_{PP} Short Circuit		51		150	mA
t_{on}	V_{PP}, Rise Time	C_L = 100pF; I_L = 50mA (see note 1)			200	µs
t_{off}	V_{PP}, Fall Time				200	µs
t_{shadow}	Shadow Timing	C_{Source} = 0.1µF (see note 2)		1		ms
t_{CKON}	Clock ON Time	C_{LOAD} = 50pF, I_{SINK} = 4mA, V_L = 0.4V	1			µs
t_{CKOFF}	Clock OFF Time		1			µs
t_D	Delay Time		250			ns
$t_{SET-UP1}$	1st bit Set-up Time		500			ns
t_{HOLD1}	1st bit Hold Time		500		t_{CKON}	ns
$t_{SET-UP2}$	Data Set-up Time		500			ns
t_{HOLD2}	Data Hold Time		500			ns
f	Clock Frequency				500	KHz
SR	V_{PP} Slew Rate	From rest state to programming state and viceversa			2	V/µs
V_{STH}	Power ON/OFF Threshold	Logic inputs onset	8.5		9.5	V
V_{SHY}	V_{STH} Hysteresis		0.6			V
T_S	Thermal Shutdown			180		°C
T_H	Thermal Hysteresis			20		°C

Note 1: True for values in Tab. 1 only
Note 2: Antibouncing circuitry active during card insertion only.

CIRCUIT OPERATION

CARD POWER SUPPLY
Regulated voltage to supply the card (5V/80mA). During nominal condition (V_S = 12V, I_{CS} = 80mA) the V_{CS} range variation is equal to ± 3%.
While during line/load variation (V_S = 10V to 15V; I_{CS} = 1mA to 80mA) the VCS range is ± 5%.
An internal circuitry checks the I_{CS} level; the protection block activates an IRQ with the proper failure code when the output current is in 81mA to 200mA range.

PROGRAMMING POWER SUPPLY
L6605 works in step-down mode by means of the programmed output voltage V_{PP}.
8V_{PP} levels can be selected programming the 3 bit DAC as per Table 1. During nominal conditions (I_{PP} = 50mA; V_{PPI} = 30V) the V_{PP} range variation is equal to ±2.5%; while during line/load variation (I_{PP} = 1mA to 50mA; V_{PPI} = max. 33V) the V_{PP} range is ±5%. An internal circuitry checks the I_{PP} level; the protection block activates an IRQ with the proper failure code when the output current is in 51mA to 150mA range. Under the power ON/OFF threshold value the logic section and the power supply regulators are disabled.

LOGIC SECTION
L6605 includes a logic circuitry in order to protect,

both card and itself.
If a failure occours an asynchronous IRQ is sent to the µP; consequently the µP forces low CS signal as I/O request.
After CS variation the µP sends also one "data direction bit" into DATA DIRECTION REGISTER.

- Direction bit = "0"
  Pin DATA is configurated in output and the µP reads the 2 bit STATUS REGISTER content

Code	1st bit	2nd bit
0	No insertion	No Failure
1	Card Inserted	Failure

Failure could be overtemperature or short circuit over the 2 regulators (VPP, VCS).

- Direction bit = "1"
  Pin DATA is configurated in input to allow the 3 bit DAC loading and than the programming of V_{PPo} output level voltage. (see Table 1).

During card insertion only resing edge of switch signal is detected , while during card extraction switch level is detected

Figure 1: Card Insertion

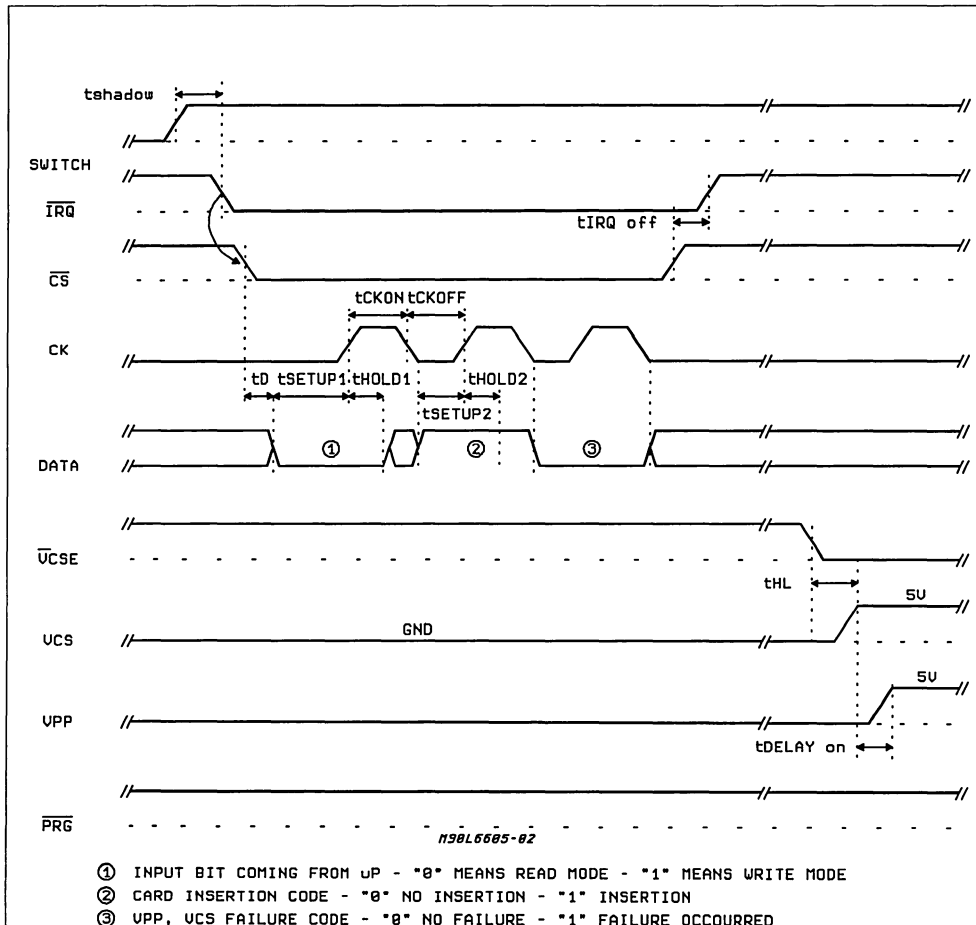
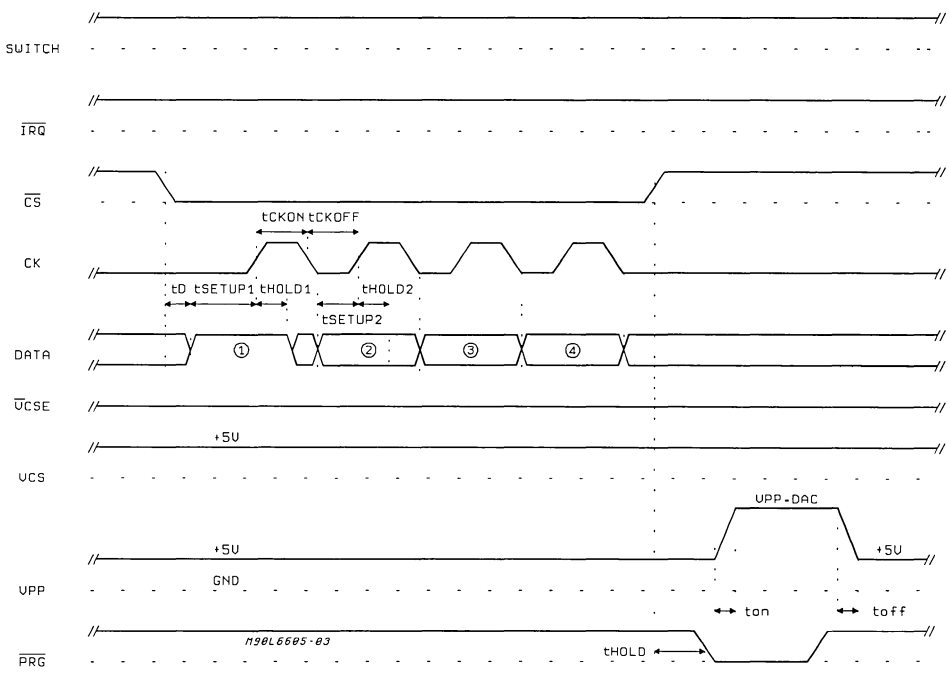
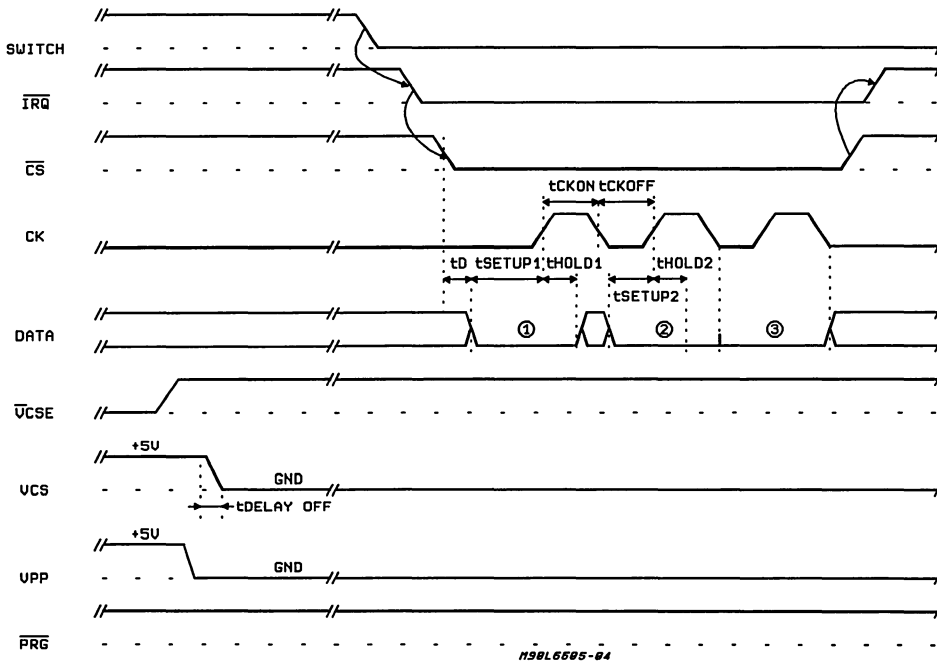


Figure 2: DAC Loading and Programmed Voltage on Set



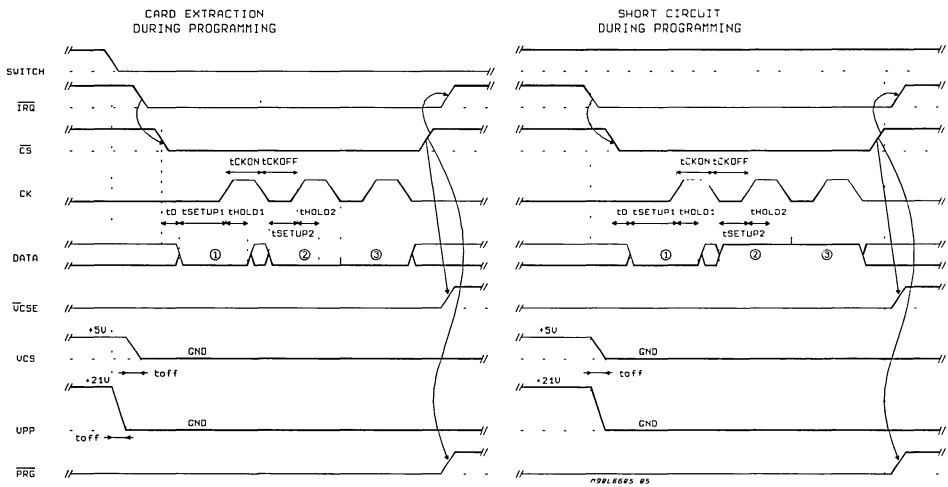
① INPUT BIT COMING FROM uP - "0" MEANS READ MODE - "1" MEANS WRITE MODE
② 1st BIT DAC
③ 2nd BIT DAC
④ 3th BIT DAC

Figure 3: End Normal Operation



① INPUT BIT COMING FROM uP - "0" MEANS READ MODE - "1" MEANS WRITE MODE
② CARD INSERTION CODE - "0" NO INSERTION - "1" INSERTION
③ VPP, VCS FAILURE CODE - "0" NO FAILURE - "1" FAILURE

Figure 4


CARD EXTRACTION
DURING PROGRAMMING
SHORT CIRCUIT
DURING PROGRAMMING
SWITCH
IRQ
CS
CK
DATA
VCSE
VCS
VPP
PRG
tCKON tCKOFF
tD tSETUP1 tHOLD1
tHOLD2
tSETUP2
+5V
GND
+21V
toff
① INPUT BIT COMING FROM uP - "0" MEANS READ MODE - "1" MEANS WRITE MODE
② CARD INSERTION CODE - "0" NO INSERTION - "1" INSERTION
③ VPP, VCS FAILURE CODE - "0" NO FAILURE - "1" FAILURE

SGS-THOMSON MICROELECTRONICS

M206

PLL TV MICROCOMPUTER INTERFACE

- HIGHLY INTEGRATED SOLUTION INCLUDING PLL SYNTHESIZER, NV MEMORY, D/A CONVERTERS, BAND SELECT OUTPUTS, CLOCK OSCILLATOR, IR SIGNAL PRE-PROCESSOR AND SERIAL BUS INTERFACE
- 32 x 16 BITS OF NV MEMORY WITH LIFETIMES OF 10^4 CYCLES/WORD AND MINIMUM 10 YEARS RETENTION STORES TUNING DATA FOR 30 CHANNELS PLUS PRESET VALUES FOR THE SIX ANALOG OUTPUTS
- PRE-PROCESSOR FOR INFRARED REMOTE CONTROL SIGNALS REDUCES COMPONENT COUNT
- SIX PWM D/A CONVERTERS WITH 64-STEP RESOLUTION
- FOUR OPEN-DRAIN BAND SELECT OUTPUTS RATED TO 13.2 V
- ON-CHIP 4 MHz CLOCK OSCILLATOR WITH BUFFERED OUTPUT
- INTEGRATED DIGITAL POWER-ON RESET
- 3-WIRE SERIAL BUS TO LOAD/READ INTERNAL REGISTERS

DESCRIPTION

The M206 is a highly integrated, programmable LSI integrated circuit for microcomputer controlled TV applications, realized using an advanced N-channel double polysilicon gate technology (NVMOS) that allows the integration of non-volatile memory and standard logic on the same chip.

It contains a phase-locked loop (PLL) synthesizer, six pulse-width modulation (PWM) digital/analog converters, a four-bit parallel output buffer, clock oscillator with buffered output, pre-processor for infrared remote control signals and a 3-wire serial bus interface.

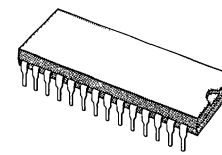
The M206 interfaces with a microcomputer through the three-wire serial bus and is programmed by loading thirteen internal registers - twelve of which are readable to simplify programming.

The PLL synthesizer requires an external 64 + 15/16 prescaler and divider and works with a phase comparator reference frequency of 0.9765 kHz. Outputs are provided to control the division ratio of the prescaler and to signal the out-of-lock condition to the microcomputer.

The infrared remote control signal pre-processor consists of a preamplifier, a squarer and a digital filter to separate noise from signals transmitted by the M708, M709 and M710 remote control transmitters. The output of this pre-processor is connected to the interrupt input of a microcomputer programmed to receive and decode the signal.

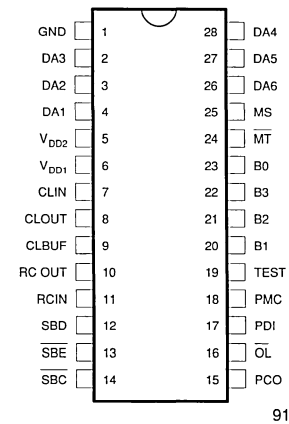
The M206 is supplied with two separate 5 V supply inputs, each provided with internal power-on reset circuits. The first, V_{DD1}, supplies the remote control and clock circuits in both standby and TV set operation. The second, V_{DD2}, supplies the rest of the circuits and is only active during TV operation.

The M206 is packaged in a 28-pin dual in-line plastic package.



DIP28
(Plastic Package)
ORDER CODE : M206B1

PIN CONNECTIONS



91DSM206-01

PIN DESCRIPTION

DA1-DA6 - *Digital/Analog converter outputs (open-drain outputs)*
Output from the six pulse-width modulation D/A converters.

B0-B3 - *Band drive outputs (open-drain outputs)*
Outputs from the four-bit buffer used for band selection.

SBD - *Serial Bus Data (bidirectional)*
Data line for serial communication with a microcomputer.

$\overline{\text{SBE}}$ - *Serial Bus Enable (bidirectional. active low)*
Enables serial bus transmissions.

$\overline{\text{SBC}}$ - *Serial Bus Clock (input. active low)*
Clock for serial bus transmissions.

RCIN - *Remote Control signal Input (analog input)*
Input to the infrared remote control signal preprocessor. Connected to the output of the IR preamplifier. Minimum input level 0.5 V peak-to-peak.

RCOUT - *Remote Control signal Output*
Output from the infrared remote control signal preprocessor. To be connected to the interrupt input of a microcomputer.

PDI - *Programmable Divider Input (input)*
This pin is the input of the programmable divider and is connected to the output of the prescaler.

PCM - *Prescaler Modulo Control (output)*
Control signal to set the prescaler division ratio (15 if high, 16 if low).

$\overline{\text{OL}}$ - *Out of Lock (output. active low)*
Signals an out of lock condition. This output is also active during the power on reset sequence.

PCO - *Phase Comparator Output*
The output of the phase comparator. Connected to the input of a low pass filter used to generate the tuning voltage.

TEST - *Test pin (input)*
The test pin is used only to test the device and is not specified for customer use. It must be connected to ground.

CLIN, CLOUT - *Clock oscillator connections*
A 4 MHz quartz crystal is connected between these pins.

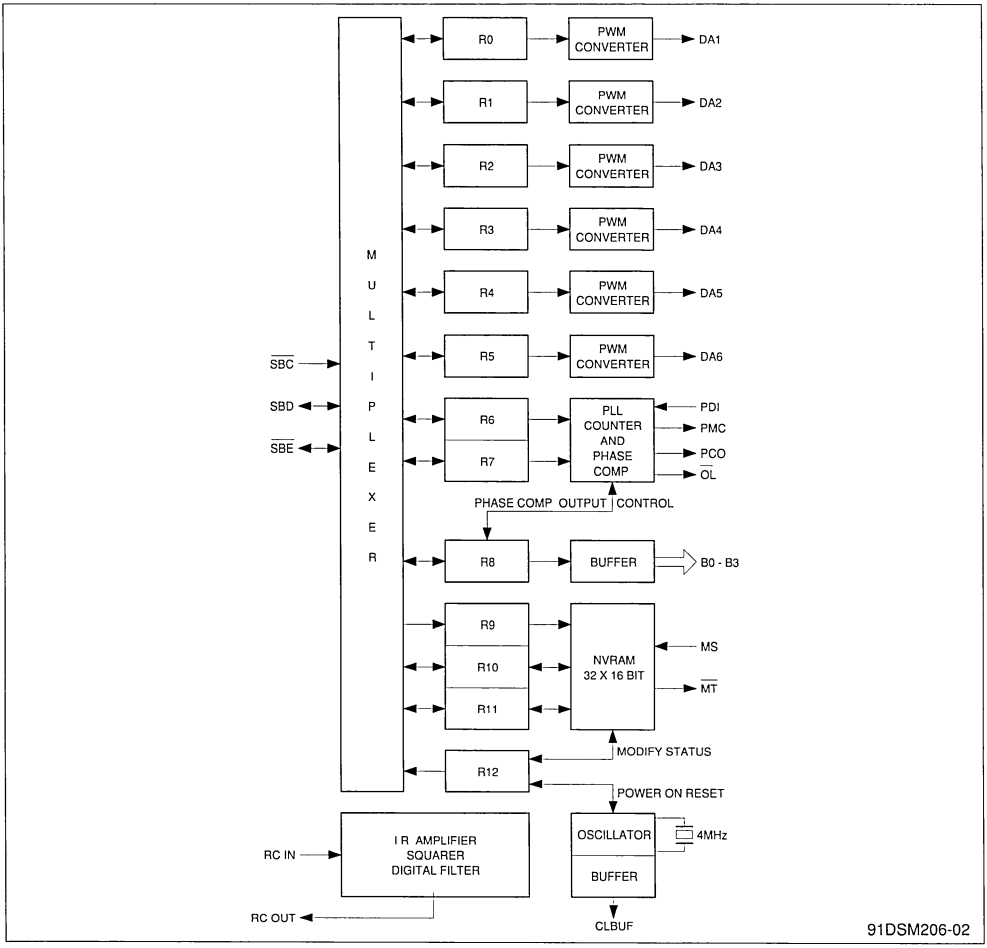
V_{DD1}, V_{DD2}, GND - *Power Supply Connections*
V_{DD1} is the + 5 V standby supply input ; V_{DD2} is the main + 5 V supply input.

MS - *Memory Supply Input (input)*
Programming pulses for the NV memory are supplied to this pin during store cycles.

$\overline{\text{MT}}$ - *Memory Timing (output. active low)*
This output supplies the timing for the memory write pulses supplied to the MS input during store cycles.

CLBUF - *Clock Buffer (output)*
This is a buffered output from the on-chip clock oscillator and can be used to drive other components (for example the microcomputer).

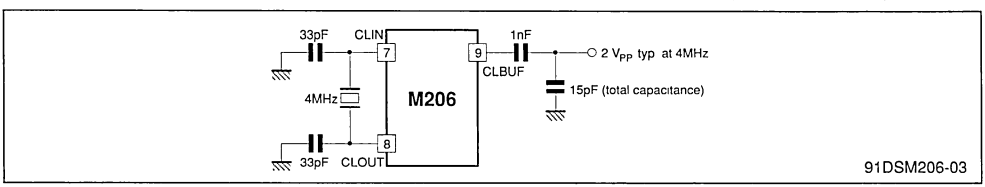
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

CLOCK

To use the internal oscillator a 4 MHz quartz crystal is connected between the pins CLIN and CLOUT. If an external clock is used this must be connected to CLIN and CLOUT left unconnected or, if required as a clock output, loaded by a capacitor up to 15 pF. The minimum external clock amplitude is 2 V peak-to-peak. A buffered clock output, CLBUF, is provided which can drive up to three ± 100 µA loads.



LOADING AND READING INTERNAL REGISTERS

The M206 is programmed by loading a set of internal registers through a 3-wire serial bus. The functions of these registers are summarised in table 1.

TABLE 1 : Summary of Internal Registers

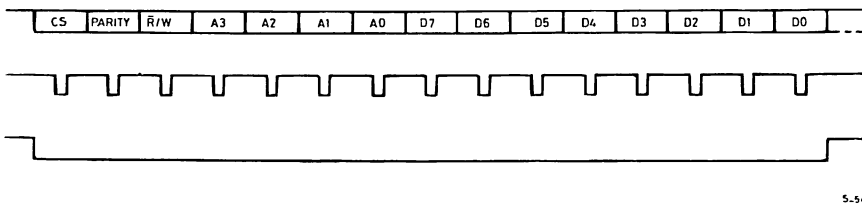
Register Number	Address				Number of Bits	Function
	A3	A2	A1	A0		
0	L	L	L	L	6	D/A Converter n° 1
1	L	L	L	H	6	D/A Converter n° 2
2	L	L	H	L	6	D/A Converter n° 3
3	L	L	H	H	6	D/A Converter n° 4
4	L	H	L	L	6	D/A Converter n° 5
5	L	H	L	H	6	D/A Converter n° 6
6	L	H	H	L	7	PLL Counter (MSB)
7	L	H	H	H	8	PLL Counter (LSB)
8	H	L	L	L	7	Buffer Outputs/Phase Comp. Output Control
9	H	L	L	H	5	NV Memory Address
10	H	L	H	H	8	NV Memory DATA
11	H	L	H	H	8	NV Memory DATA
12	H	H	L	L	2	NV Memory Modify Control/Reset Control

TAB-01

The 3-wire serial bus consists of the signals SBD (Serial Bus Data), SBE (Serial Bus Enable) and SBC (Serial Bus Clock). The enable and data pins, SBD and SBE, are bidirectional.

Data is accepted when the clock is low (active) and latched into the M206 on the low-high transition of the clock. All bus transfers are controlled by SBE.

REGISTER LOADING. Serial data transferred from the microprocessor to the M206 has the following format :

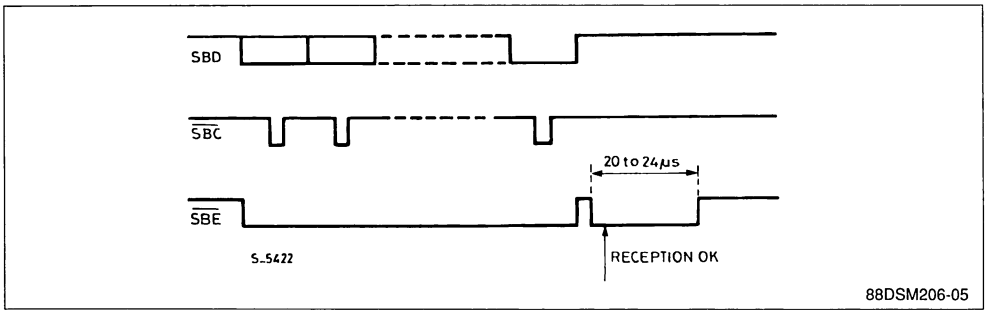


88DSM206-04

Bit	+Description
CS	Chip Select (always low)
PARITY	Parity bit (the number of " H " bits transmitted is odd)
R/W	Read/Write. High for Register Load ; Low for Register Read
A0-A3	Register Address (see table 1)
D0-D7	Data to be loaded into register (load operation only)

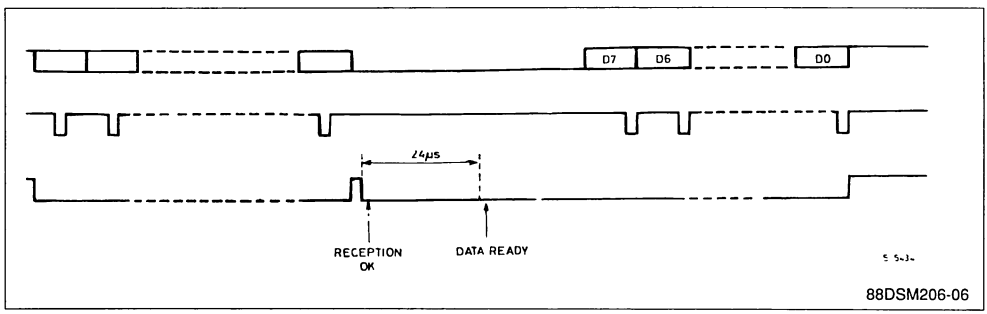
TAB-02

The received data word is checked - length, CS and parity - immediately after the low-high transition of SBE. If the received word is valid this is signalled to the microprocessor by forcing the SBE line low for 20-24µs.



REGISTER READING. M206 registers are read by transmitting a 15 bit word as shown in fig. 4 with R/W low and the address of the register to be read in A0, A1, A2, A3. Bits D0-D7 can be high or low except when register 9 is addressed.

If this word is received correctly the SBE line is immediately pulled low by the M206 and after 24 µs the contents of the addressed register will be available to be read. The microprocessor reads this data by sending eight clock pulses. Data is output on the low-high transition of SBC and the first data bit is available before the first clock pulse.



LOADING THE NON-VOLATILE MEMORY. Data is stored in the 32 x 16-bit NV memory by loading the new contents into registers 10 and 11 then the address into register 9. The memory modify cycle begins when the address has been loaded and successful completion is indicated by a logic "1" in bit zero of register 12.

The time for a modify cycle varies from a few milliseconds to several hundred milliseconds during the device lifetime and is not internally limited. The storage operation should be aborted after one second if it proves unsuccessful. This is done by setting bit zero of register 12.

READING THE NON-VOLATILE MEMORY. The NV memory is read by loading the address into register 9. The contents of the addressed word are automatically loaded into registers 10 and 11 and can be read by two register read operations. The data is ready 200 µs after the address load.

PLL COUNTER

The PLL counter consists of a single counter that acts as the program counter (11 bit) and is swallow counter (4 bit) alternately. Data for the PLL counter is loaded into registers 6 and 7. Register 6 must be loaded first because the register 7 load operation initiates the data transfer to the PLL counter.

The reference frequency is produced by dividing the clock frequency by 4096. With a 4 MHz clock this gives a reference frequency of 976.5 Hz.

An out-of-lock signal is generated (output OL) when the phase error between the reference frequency and the input frequency exceeds 0.72 (2 µs).

The phase comparator output, PCO, has a three-state push pull configuration with a high level of 5 V and a low level of 0 V (with zero current sink or pump). The output impedance (both states) is typically 200 Ω (400 Ω maximum). The phase comparator output can be set to a high impedance state (both

sink and pump transistors off) by setting bit 4 of register 8. The output is held in the high impedance state until this bit is reset. The phase comparator output should be set to high impedance when changing band.

RECOVERING LOCK. The phase comparator output can also be set to high and low levels to restore normal operation when the oscillator stops or the prescaler functions incorrectly at high frequency.

In the first condition (oscillator off) the prescaler sometimes oscillates, at high frequency. The loop reacts by reducing the varicap voltage in an attempt to reduce the frequency, thus worsening the situation. This out-of-lock condition is signalled to the microprocessor (by the $\overline{OL}$ output) which can set the phase comparator output to low level, forcing the varicap voltage up and restarting the oscillator. The phase comparator output is forced low by setting bit 5 of register 8. After about 1 ms this bit is automatically reset and the loop should lock again.

When the out-of-lock condition is caused by a failure of the prescaler to operate correctly at high frequencies the loop reacts by increasing the voltage, hence the frequency, again worsening the situation. To recover from this condition the phase comparator output is set high. This is done by setting bit 6 of register 8 which, as in the previous case, resets itself after 1 ms.

The out-of-lock condition could also be caused by unwanted changes in band or PLL counter contents provoked by external interference (spikes on supply etc.). For this reason it is always advisable to reload the band and PLL counter registers before attempting to recover lock as described above. If the phase comparator output is in the high impedance state, the $\overline{OL}$ output signals the reset condition but not the out-of-lock condition.

CALCULATING PLL COUNTER VALUES

a) F = video carrier

b) IF = 38.9 MHz

c) The frequency to be synthesized is Fs = F + IF

d) The Ref. frequency of the phase comparator is

$$F_{ref} = \frac{4.000MHz}{4096} = 0.97656kHz$$

e) Using the prescaler 64 + 15/16 the minimum frequency steps is

$$F_{ref} \times 64 = 62.5\ kHz$$

f) The modulo of division N is given by the ratio between the frequency to be synthesized and the reference frequency multiplied by 64. The result has to be rounded.

$$NS = \text{Integer rounded} \left[\frac{F_S}{F_{ref} \cdot 64} \right]$$

g) With the 64 + 15/16 prescaler and the particular counter of the M206 the division by N is given by

$$N_S = (I_S + 1) \cdot 15 + (R_S + 1) \cdot 16$$

where I (integer part) controls the division by 15 (program counter) and R (rest) controls the division by 16 (swallow counter). For ease of calculation we decrement N_S by one getting $N_C = N_S - 1$.

The numbers I_C and R_C are given by :

$$N_C = (I_C + 1) \cdot 15 + (R_C + 1) \cdot 16$$

$$N_C - 31 = I_C \cdot 15 + R_C \cdot 16$$

using the formulas :

$$R_C = N_C - 31 - 15 \cdot \text{Integer} \left[\frac{N_C - 31}{15} \right]$$

$$IC = \frac{N_C - 31 - R_C \cdot 16}{15}$$

$$R_S = R_C + 1$$

$$I_S = I_C\ 1$$

Example :

Channel 21, F = 471.25 MHz

$F_S = F + IF$, $F_S = 471.25 + 38.9 = 510.15$ MHz

$$N_S = \text{Integer rounded} \left[\frac{510.15 \cdot 10^6}{62.5 \cdot 10^3} \right]$$

$$= \text{Integer rounded } [8162.4] = 8162$$

$$N_C = N_S - 1 = 8161$$

$$R_C = N_C - 31 - 15 \cdot \text{Integer} \left[\frac{N_C - 31}{15} \right]$$

$$= 8161 - 31 - 15 \cdot \text{Integer} \left[\frac{8161 - 31}{15} \right]$$

$$= 8130 - 15 \cdot \text{Integer } [542]$$

$$= 8130 - 15 \cdot 542 = 8130 - 8130 = 0$$

$$I_C = \frac{N_C - 31 - R_C \cdot 16}{15} = \frac{8161 - 31}{15} = 542$$

$$R_S = R_C + 1 = 0 + 1 = 1$$

$$I_S = I_C - 1 = 542 - 1 = 541$$

R and I have to be translated into binary code.

DIGITAL/ANALOG CONVERTERS

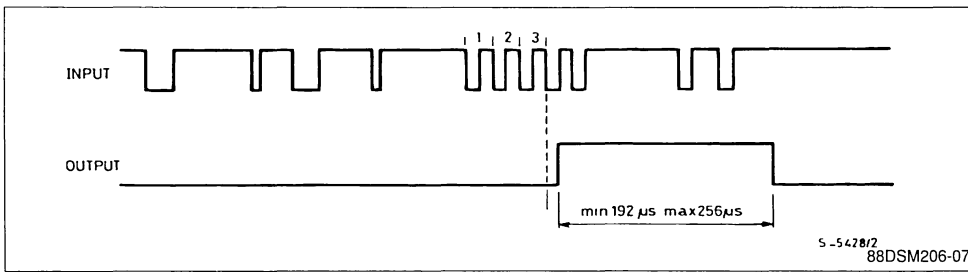
The six pulse-width modulation (PWM) D/A converters have a resolution of 64 steps and an output frequency of 16 kHz (with 4 MHz clock). At power on reset they are set to a duty cycle of zero.

POWER ON RESET

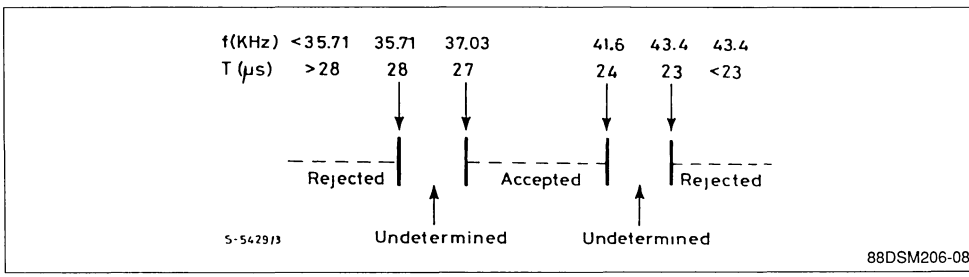
The V_{DD1} and V_{DD2} supplies have an integrated digital power on reset with a duration of 250 ms.
The reset condition is signalled by a low level on the out-of-lock output, $\overline{OL}$. The microprocessor can test this condition by reading bit 1 of register 12. This bit is zero during power on reset and the $\overline{OL}$ output remains active until it is read. Reading this bit automatically restores it to a high state.
During power on reset time commands from the micoprocessor are not acknowledged. Power on reset also sets the phase comparator output to a high impedance, state. It is restored by resetting bit 4 of register 8.

REMOTE CONTROL SIGNAL PRE-PROCESSOR

This section contains a preamplifier, squarer, digital filter and a pulse generator. The digital filter enables the pulse generator only if three successive negative going pulses (4 edges) are detected. The distance between these pulses must be in the range 24-27 µs (about 37-41 kHz with a 4 MHz clock). The input is not tested for the duration of the output pulse (192-256 µs).
If this pre-processor is used in conjunction with M709 or M710 remote control transmitters valid signals can be recognized in the presence of extreme noise conditions. Separating the signals from the noise externally in this way reduces the number of interrupts that the microcomputer has to handle thus allowing it to concentrate on other takes. To take advantage of this section the M708, 709, 710 transmitters must operate with a clock frequency in the range 492-508 kHz.
The input can be DC or AC compled to the I.R. preamplifier.
In case of DC coupling the quiescent input level is suggested to be 1.5 V.

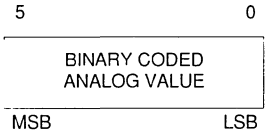


Response of the Digital Filter as a Function of the Input Frequency (in kHz).



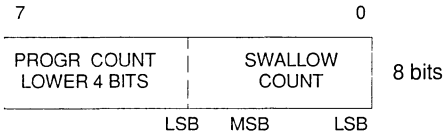
M206 PROGRAMMING SUMMARY

Registers 0-5 – D/A Convertors 1-6

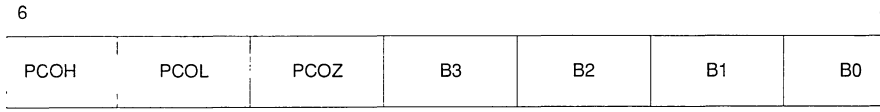


Register 6 – PLL Program Counter.

Register 7 – PLL Program/Swallow Counter.



Register 8 – Band Drive Outputs/Phase Comparator Output Control.



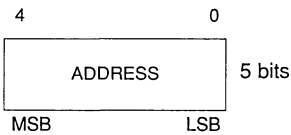
B0-B3 Band Drive outputs B0-B3
PCOZ Phase Comparator Output High Impedance
PCOL Phase Comparator Output Low Level
PCOH Phase Comparator Output High Level

PCOH	+PCOL	+PCOZ	+Phase Comparator Output
L	L	L	Normal PLL Operation
L	L	H	High Impedance State
L	H	L	Low for 1 ms then returns automatically to normal PLL operation.
L	H	H	Low for 1 ms then returns to high impedance state.
H	L	L	High for 1 ms then returns to normal PLL operation.
H	L	H	High for 1 ms then returns to high impedance.
H	H	L	Normal Operation *
H	H	H	High Impedance *

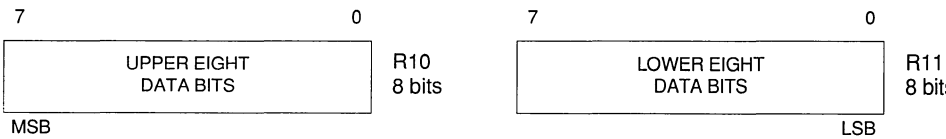
TAB-03

* These combinations are not accepted and PCOL, PCOH are automatically reset low after 1 ms

Register 9 – NV Memory Address.



Registers 10 & 11 – NV Memory Data.



M206 PROGRAMMING SUMMARY (continued)

Register 12 – NV Modify Status/Reset Status.

1	0	
RESET STATUS	MODIFY STATUS	2 bits

Flag	L	H
MODIFY STATUS RESET STATUS	Modify in progress. Reset actived.	Modify over Reset not actived.

TAB-04

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD1}, V_{DD2}	Supply Voltage	– 0.3 to 7	V
V_{PP}	Memory Supply Voltage	– 0.3 to 28	V
V_I	Input Voltage (except Pin 11) Pin 11	– 0.3 to 7 – 0 3 to 15	V V
$V_{O\ (off)}$	Off State Output Voltage (except Pins 2–3–4–26–27–28–20–21–22–23–24) Pins 2–3–4–20 to 23–26 to 28 Pin 24	7 15 28	 V V
I_{OL}	Output Current (except Pins 2–3–4–26–27–28) Pins 2–3–4–26–27–28	5 10	mA mA
I_{OH}	Output Current (Pins 15, 9)	– 5	mA
P_{tot}	Total Package Power Dissipation	1	W
T_{stg}	Storage Temperature Range	– 25 to 125	°C
T_{oper}	Operating Temperature Range	0 to 70	°C

TAB-05

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C ; typical values are at T_{amb} = 25°C)

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD1}, V_{DD2}	Supply Voltage	5–6		4.75	5	5.25	V
V_{PP}	Memory Supply Voltage	25		24	25	26	V
V_{IL}	Input Low Voltage	12–13–14–17		0		0.8	V
V_{IH}	Input High Voltage	12–13–14–17		2.4		5.25	V
V_{IPP}	Peak to Peak Signal	11	AC COUPLING	0.5		13.2	V
V_{TH}	Threshold Voltage	11	DC COUPLING		1.25		V
V_{OL}	Output Low Voltage	10–12–13 16–18–20 21–22–23	V_{DD} = 4.75 V I_{OL} = 1.6 mA			0.4	V
		9	V_{DD} = 4.75 V I_{OL} = 0.2 mA			0.4	V
		15	V_{DD} = 4.75 V I_{OL} = 1 mA		0.2	0.4	V
		2–3–4–26 27–28	V_{DD} = 4.75 V I_{OL} = 5 mA			1	V
		24	V_{DD} = 4.75 V I_{OL} = 2.5 mA			8	V

TAB-06

STATIC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output High Voltage	9–18	V_{DD} = 4.75 V I_{OH} = – 0.2 mA			2.4	V
		15	I_{OH} = – 1 mA		V_{DD2} – 0.2	V_{DD2} – 0.4	V
$I_{O\ (off)}$	Output Leakage Current	2–3–4–10–16 20–21–22–23 26–27–28	V_{DD} = 4 75 V $V_{O\ (off)}$ = 5.25 V			10	µA
		24	V_{DD} = 4.75 V $V_{O\ (off)}$ = 26 V			100	µA
I_{IL}	Input Low Current	12-13	V_{DD} = 5.25 V V_{OL} = 0.4 V		50	200	µA
I_{OZ}	High Impedance output Current	15	V_O = 0 to V_{DD2}		± 20		nA
I_{DD1}	Supply Current	6	V_{DD1} = 5.25 V			8	mA
I_{DD2}	Supply Current	5	V_{DD2} = 5.25 V			30	mA
I_{PP}	Memory Supply current	25	V_{PP} = 26 V • Write Peak Average • Erase Peak Average • Read Peak Average			 40 11 7 4.5 6 2	mA

TAB-07

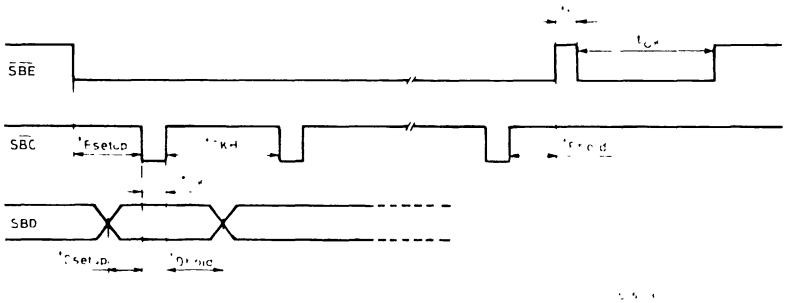
DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{CKL}	$\overline{SBC}$ LOW Time		2		50	µs
t_{CKH}	$\overline{SBC}$ HIGH Time		4			
$t_{E\ setup}$	$\overline{SBE}$ Set-up to $\overline{SBC}$ falling edge time		0.5			
$t_{E\ hold}$	$\overline{SBE}$ Hold Time from $\overline{SBC}$ rising edge		3			
$t_{D\ setup}$	Data Setup Time		1			
$t_{D\ hold}$	Data Hold time		1			
t_1	Time between $\overline{SBE}$ Rising Edge and OK of Reception				3	
t_{OK}	OK of Reception Time			22	26	
t_2	Minimum $\overline{SBC}$ Delay Time from OK of Reception		26			
t_3	Data Valid Time from OK of Reception			20	25	
t_4	Data Valid Time from $\overline{SBC}$ Pulse				4	
t_5	Propagation Delay of PMC				0.9	

TAB-08

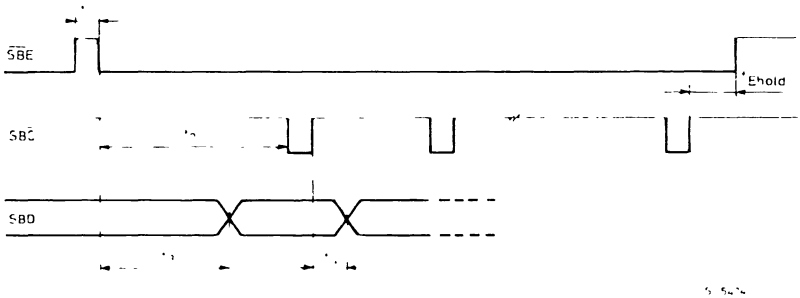
TIMING WAVEFORMS

REGISTER LOAD



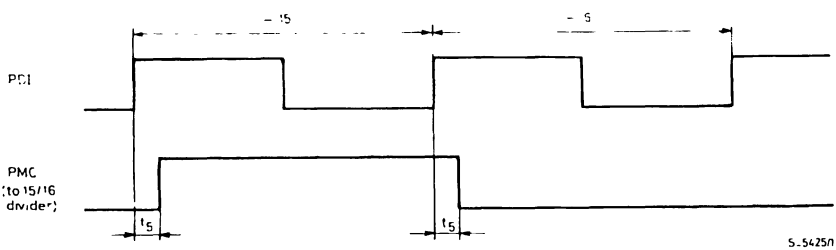
88DSM206-09

REGISTER READ



88DSM206-10

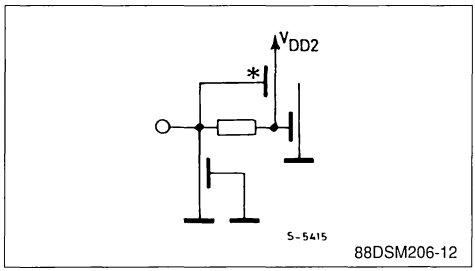
PRESCALER MODULO CONTROL TIMING



88DSM206-11

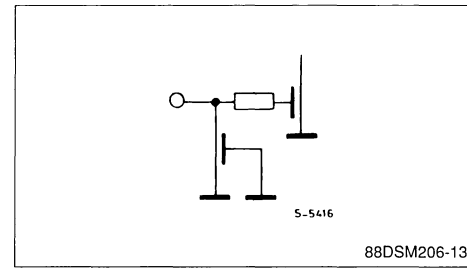
INPUT AND OUTPUT CONFIGURATIONS

$\overline{SBC}$



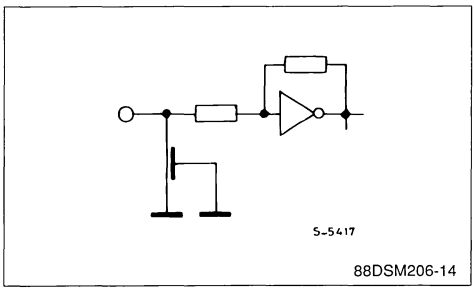
88DSM206-12

PDI



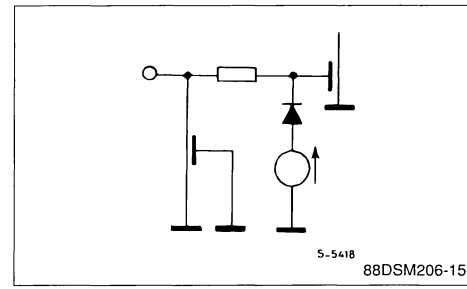
88DSM206-13

CLIN



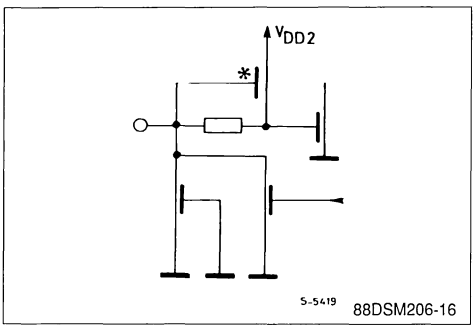
88DSM206-14

RCIN



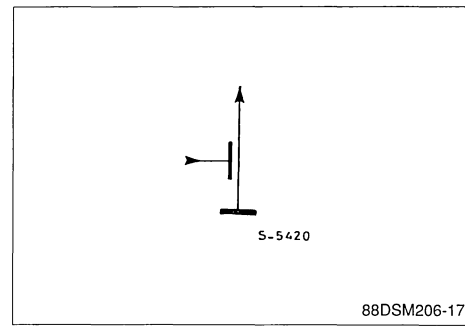
88DSM206-15

SBD, $\overline{SBE}$



88DSM206-16

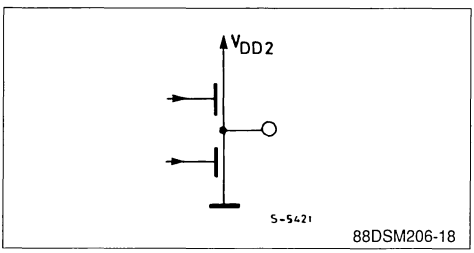
DA1-DA6, B0-B3, $\overline{OL}$, RCOUT



88DSM206-17

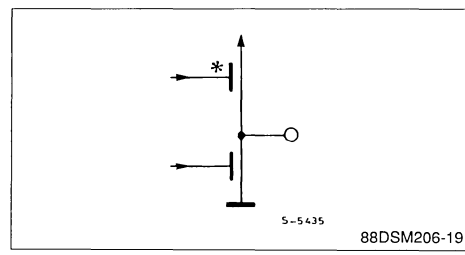
* Depletion transistors

PCO



88DSM206-18

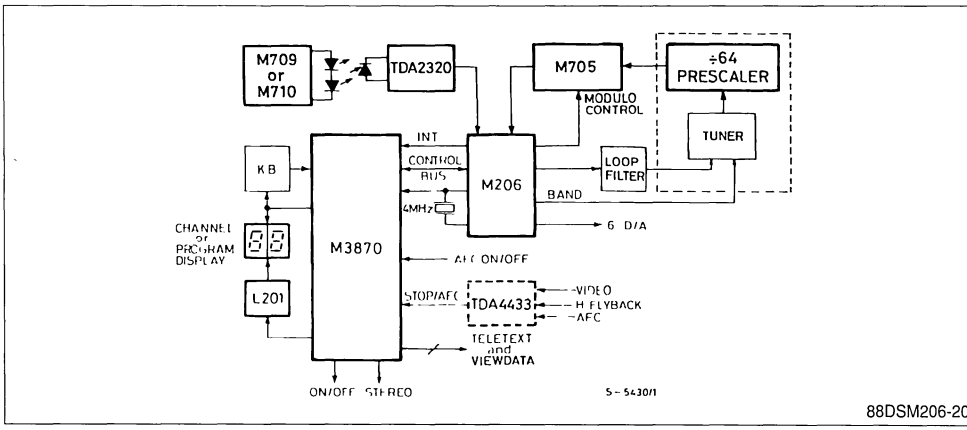
PMC, CLOUT, CLBUF



88DSM206-19

TYPICAL APPLICATIONS

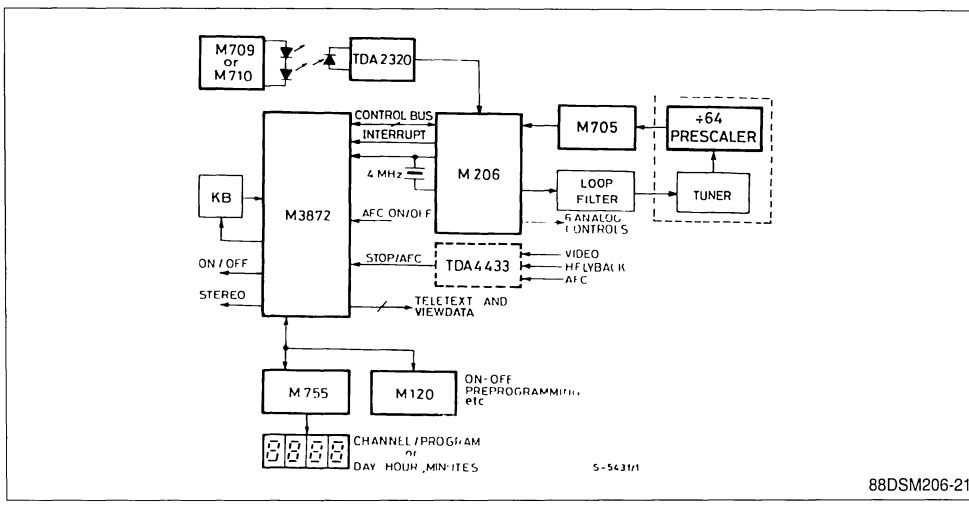
Remote Controlled TV Frequency Synthetizer.



88DSM206-20

- Remote Control Decoding by Microprocessor.
- 32 Station Non-Volatile Memory or 30 Station
- Memory + Normalized D/A Positions
- Flexible System Operation
- Frequency Synthesis of all Standard and CATV Channels
- Direct Channel Selection
- ± 4 MHz Fine Tuning (62.5 kHz per Step)
- Automatic Search within Channel (using TDA4433)
- AFC Operation (using TDA4433)
- 6 D/A Converters
- Teletext and Viewdata Data Bus Conversion

Remote Controlled TV Frequency Synthetizer and Clock Timer.



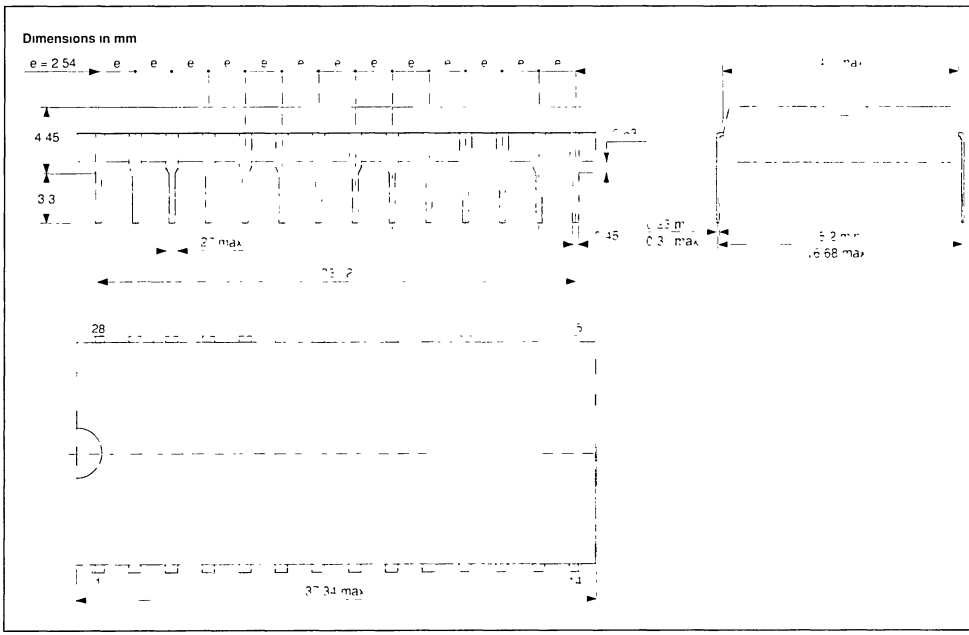
88DSM206-21

Frequency Synthesis as described in the Basic Configuration with the addition of :

- Further Station Memory, using M120, 1 K NV MEMORY
- Clock and programmable timer for automatic switch ON/OFF, using M755.

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

M491B

SINGLE-CHIP VOLTAGE SYNTHESIS TUNING SYSTEM WITH 1 ANALOG CONTROL

- 16-STATION MEMORY - 7-SEGMENT LED DISPLAY
- VOLTAGE SYNTHESIZER : 13 BITS
- 4-BAND PRESET CAPABILITY
- NON-VOLATILE MEMORY : 304 BITS
  - 16 WORDS OF 19 BITS FOR TUNING VOLTAGE (13 bits) - BAND (2 bits) - FINE DETUNING (4 bits)
  - 10^4 MODIFY CYCLES PER WORD
  - MIN 10 YEARS DATA RETENTION
- PCM REMOTE CONTROL RECEIVER : DECODES SIGNAL TRANSMITTED BY M708
- VOLUME D/A : 6-BIT RESOLUTION / 8kHz
- MEMORY SKIP FUNCTION
- AUTOMATIC SEARCH WITH DIGITAL AFT CONTROL
- FINE DETUNING D/A ACTING ON AFT DISCRIMINATOR (16 steps) WITH SEPARATE STORAGE FOR EACH MEMORY POSITION. ALTERNATIVELY IT CAN BE USED TO CONTROL BRIGHTNESS OR COLOUR SATURATION
- MANUAL SEARCH WITH DIGITAL AFT CONTROL
- MANUAL SEARCH WITH LINEAR AFT
- SWEEP SEARCH DISPLAY OUTPUT
- SUPPLY VOLTAGES : V_{DD} = + 5V, V_{PP} = + 25V FOR THE MEMORY
- CLOCK OSCILLATOR : 445 TO 510kHz
- INTEGRATED DIGITAL POWER ON RESET (no external initialization circuitry required)

DESCRIPTION

The M491B is a monolithic N-MOS LSI circuit including a Floating-gate Non-Volatile Memory for storage of up to 16 stations. Tuning of the station is performed with a 8192 step D/A converter, using the principle of voltage synthesis.

It is designed for 7-segment LED displays. Direct memory selection is possible only from remote control while Up/Down memory scanning is possible on the set and also from remote control. An option input for 8 or 16 stations is available.

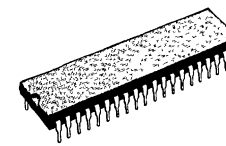
The circuit also includes a PCM remote control receiver operating in conjunction with the transmitter M708. The highly reliable transmission code ensures error-free signal detection even in presence of high noise conditions.

Search of the station is possible in automatic or manual modes. The circuit can operate with a Digital or Linear AFT control.

The Digital AFT mode is necessary for automatic search and requires an external circuit (TDA4433 or equivalent, e.g. dual comparator plus TV station detector) to convert the AFC-S-curve into an Up/Down command.

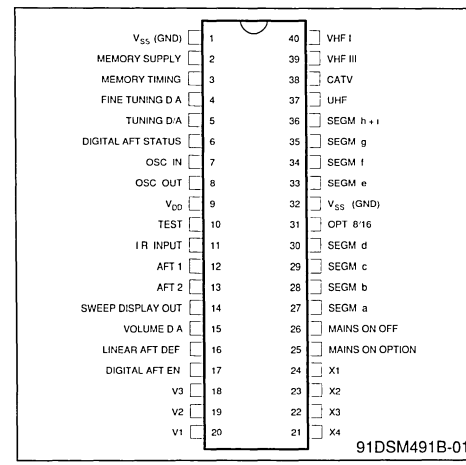
Fine tuning (detuning) is also possible with different modes of operation.

The circuit is assembled in 40-pin dual in-line plastic package.

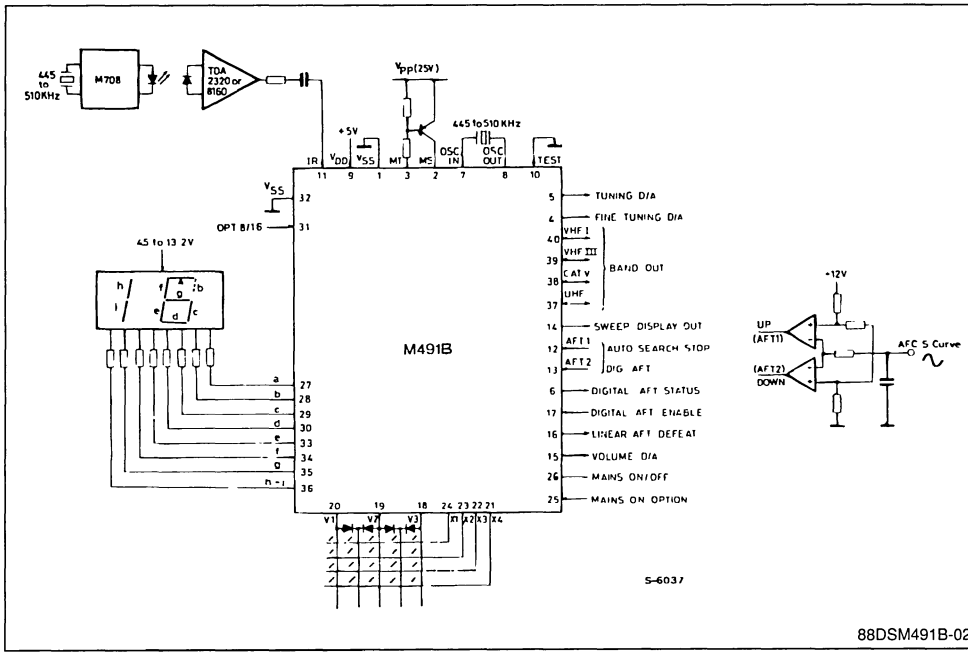


DIP40
(Plastic Package)
ORDER CODE : M491B1

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3, + 7	V
V_{PP}	Memory Supply Voltage	– 0.3, + 26	V
V_I	Input Voltage	– 0.3, + 15	V
$V_{O\ (off)}$	Off State Input Voltage (except pin 3) Pin 3	15 28	V V
I_{OL}	Output Low Current Led Driver Outputs Pins 6 – 14 Pins 4 – 5 All Other Outputs	 20 20 7.5 5	mA
t_{pd}	Max. Delay between Memory Timing and Memory Supply Pulses	5	µs
P_{tot}	Total Package Power Dissipation	1	W
T_{stg}	Storage Teperature	– 25, + 125	°C
T_{op}	Operating Temperature	0, + 70	°C

TAB-01

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(T_{amb} = 0 to + 70°C, V_{DD} = +5V unless otherwise specified)

Pin	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
2-Memory Supply	I_{PP}	Memory Supply Current	V_{PP} = 25V Write Peak Average Erase Peak Average Read Peak Average			 42 12 9 5 8 2.5	mA
	R	Pull Down Resistor				25	kΩ
3–Write Timing Out	V_{OL}	Output Low Voltage	V_{DD} = 4.75 V, I_{OL} = 2.5 mA			8	V
	$I_{O\ (off)}$	Output Leakage Current	V_{DD} = 4.75 V, V_{OUT} = 26 V			100	µA
4–Fine Tuning D/A 5–Tuning D/A	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			50	µA
	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 5 mA			1	V
6–Digital AFT Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 20 mA			1.5	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			100	µA
9–Power Supply	I_{DD}	Supply Current	V_{DD} = 5.25 V			100	mA
11–I.R. Input	V_{IPP}	Peak-to-Peak Voltage		0.5		13.2	V
12–AFT1 13–AFT2	V_{IL}	Input low Voltage	V_{DD} = 5.25 V			1.5	V
	V_{IH}	Input High Voltage	V_{DD} = 5.25 V	3.5			V
	I_{IL}	Input Low Current	V_{DD} = 5.25 V, V_{IL} = 1.5 V			–0.4	mA
	R	Pull-up Resistor			30		kΩ
14—Display Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 20 mA			1.5	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			100	µA
15–Volume D/A	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 4 mA			1	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			50	µA
16–Linear AFT Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 1 mA			0.4	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V, $V_{O\ (off)}$ = 13.2 V			50	µA
17–Digital AFT Enable	V_{IL}					0.8	V
	V_{IH}			2.0			V
	I_{IL}		V_{DD} = 5.25 V, V_{IL} = 0.8 V			–0.4	mA
	R	Pull-up Resistor			30		kΩ
18–19–20 V3, V2, V1 } Keyboard In	V_{IL}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25 V, V_{IL} = 0.8 V			–0.4	mA
	R	Pull-up Resistor			30		kΩ
21–22–23–24 X4, X3, X2, X1 } Keyboard Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 1 mA			0.4	V
	$I_{O\ (off)}$		$V_{O\ (off)}$ = 5.5 V			25	µA

TAB-02

DC ELECTRICAL CHARACTERISTICS (continued)

Pin	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
25–Mains On Enable	V_{IL}					0.8	V
	V_{IH}			2.4			V
	I_{IL}		V_{DD} = 5.25 V			–0.4	mA
	R	Pull-up Resistor	V_{IL} = 0.8 V		30		kΩ
26–Mains On/Off	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 100 µA			0.4	V
	I_O		V_{DD} = 4.75 V, V_O = 0.7 V	–1.6			mA
31–Z2 32–Z1 MPX for Display Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 1 mA			0.4	V
	$I_{O\,(off)}$		V_{DD} = 5.25 V, $V_{O\,(off)}$ = 13.2 V			50	µA
37–UHF, 38–CATV, 39–VHFIII, 40–VHFI (B A N D)	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 1 mA			3	V
	V_{OH}		V_{DD} = 4.75 V, I_{OH} = – 150 µA	2.4			V
	V_{IL}					0.3	V
	V_{IH}			3			V
	$I_{O\,(off)}$		V_{DD} = 5.25 V, $V_{O\,(off)}$ = 13.2 V			50	µA
27-28-29-30-33-34-35 Display Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 20 mA			1.5	V
36-Display Out	V_{OL}		V_{DD} = 4.75 V, I_{OL} = 30 mA			1.5	V
31-Memory 8/16	V_{IH}			2.0			V
	V_{IL}					0.8	V

TAB-03

DESCRIPTION (All timings at f_{clock} = 500kHz)

PIN 1 : V_{SS}

The substrate of the IC is connected to this pin. This is the reference pin for all parameters of the IC.

PIN 2 : MEMORY SUPPLY VOLTAGE

A supply voltage of 25 ± 1 V has to be applied to this pin during the modify and read cycles.

MODIFY CYCLE

A modify cycle consists of three steps :

1. All "1"s are written in the bits of the selected word.
2. All bits of the selected word are erased (all "0"s)
3. The new content is written.

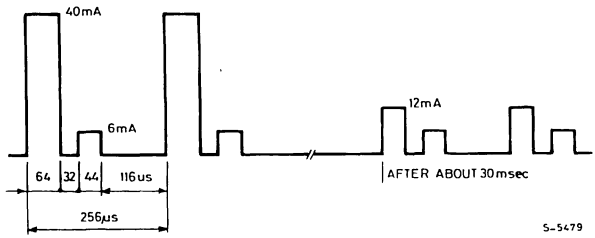
Thus a constant aging of all the bits of the word is obtained.

During both write and erase cycles the memory status is checked continuously ; therefore after each write or erase pulse a read operation is carried out. The write or the erase operations are stopped as soon as the result of the read operation is valid.

WRITE CYCLE. The peak of the current flowing through pin 2 during a write operation is shown in fig. 1, while fig. 2 shows the envelope of the same current.

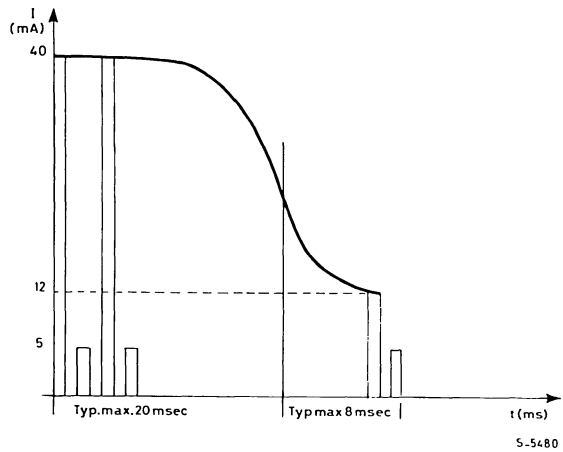
The typical write time is 3-4 ms for the first cycles and increases to about 30 ms after 1000 cycles.

Figure 1



88DSM491B-03

Figure 2



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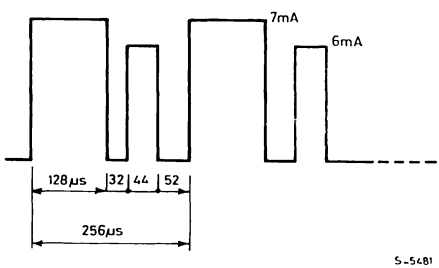
ERASE CYCLE. Fig. 3 shows the timing and the waveform of the current flowing through pin 2 during the erase operation. The peak current is 7 mA (max) during the erase cycle and 6 mA (max) during the read cycle. The typical erase time is 10 ms for a new device and increases with the number of modify operations up to 200 ms after 1000 cycles.

Figure 3



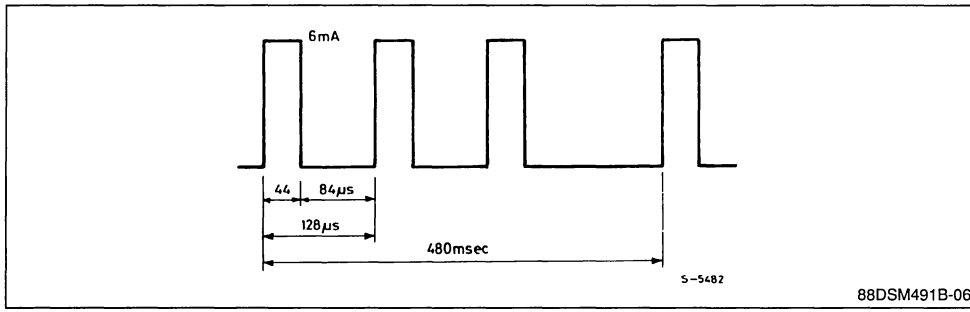
88DSM491B-05

In order to protect the memory in case of failure of some bits the modify operation is stopped after 1 sec.

READ CYCLE

Fig. 4 shows the waveform of the current during a read operation.

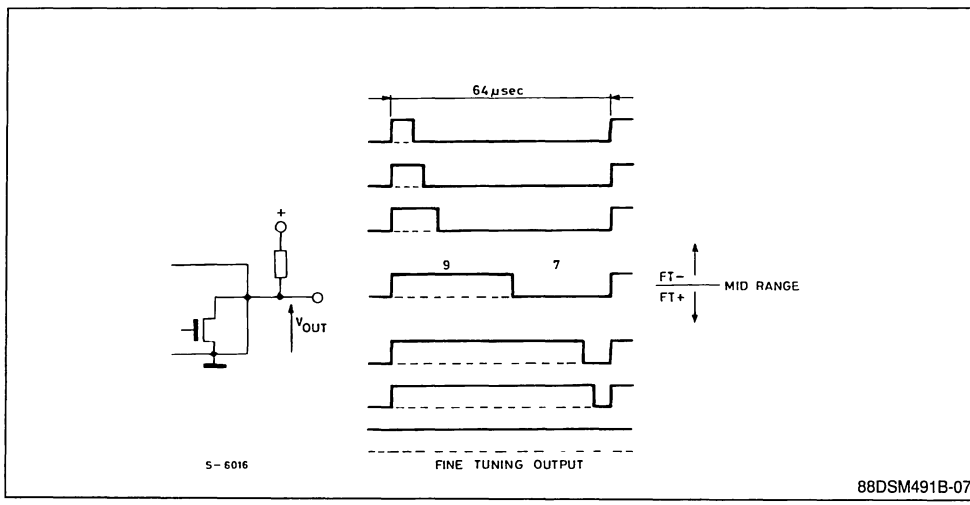
Figure 4



PIN 3 : MEMORY TIMING OUTPUT
This output gives the timing for the pulses to be applied at pin 2 during the modify and read cycles. The output consists of an open drain transistor.

PIN 4 : FINE TUNING D/A
A D/A converter with 16-step resolution and a frequency of 15kHz can be used to generate a voltage which, if fed to a varicap diode in parallel to the AFC discriminator, will detune the receiver by a small Δf while maintaining the action of the Digital AFT. This output can be used in conjunction with both Linear and Digital AFT modes of operations.

Figure 5



The Fine tuning function operates as follows :

- At the start of any automatic or manual search, the output is set at the mid range.
- When the search has been completed it is possible to operate on FT ± commands.
  The store command memorizes this information together with the 13 tuning voltage bits and 2 information bits.
- Modification time of FT D/A is of 1 step every 200 ms if issued locally or every 2 received signals from Remote control transmitter.

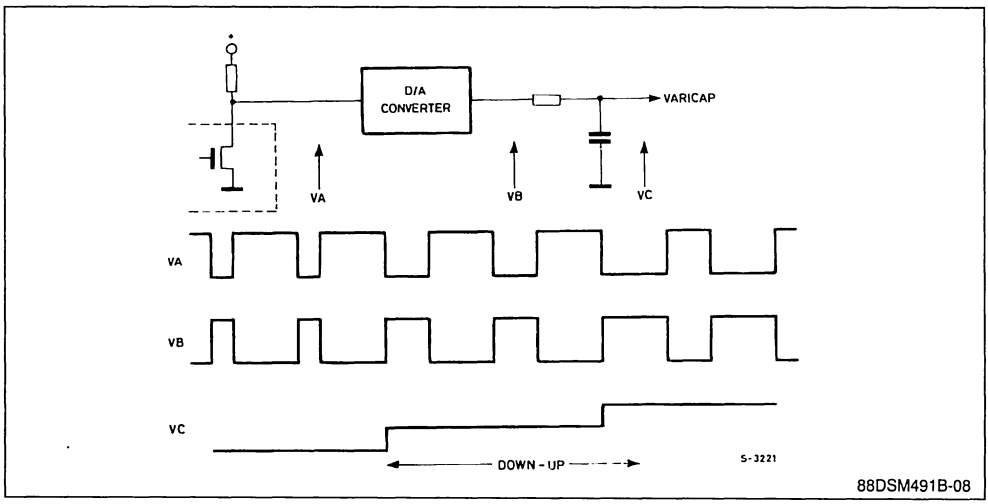
PIN 5 : TUNING D/A

A 2^{13} = 8192 step pulse modulated signal for the tuning voltage is available on this pin.

Pulse modulation is implemented by combination of a rate multiplier and pulse width principle.

With a tuning voltage increasing from zero, the number of pulses increases continuously up to 2^8 = 256 ; starting from this point the number of pulses remains the same but the pulses get larger until they reach the maximum content of the internal counter. The output consists of an open drain transistor which offers a low impedance to ground when in the ON state.

Figure 6

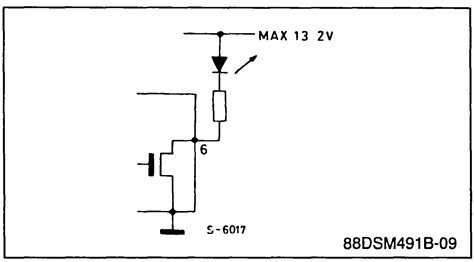


PIN 6 : DIGITAL AFT STATUS OUTPUT

This output shows the status of the digital AFT. It is low when the digital AFT is enabled and it can directly drive a LED.

The output consists of an open drain transistor.

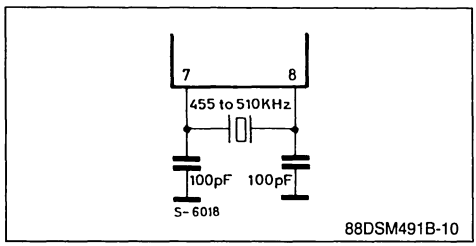
Figure 7



PINS 7 & 8 : OSCILLATOR INPUT/OUTPUT

The frequency of the clock oscillator should be between 445 and 510kHz using a low-cost ceramic resonator. In these conditions the value of the reference frequency of the transmitter can be in the same range. In other words the transmitter and the receiver can operate with different reference frequencies.

Figure 8



PIN 9 : V_{DD}

The supply voltage has to be comprised in the range 4.75 to 5.25 V. When it is applied an internal power on reset of 0.5 s is generated.

The memory position 1 is automatically read if the mains on option input (pin 25) is grounded.

PIN 10 : TEST

This pin is used for testing and has to be connected to V_{SS}.

PIN 11 : I.R. SIGNAL INPUT

The integrated receiver decodes signals transmitted by M708, address 9.

The minimum signal to be applied is 0.5 V peak-to-peak. (AC-coupled).

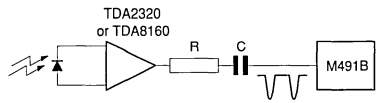
The receiver input section performs the following tests on the incoming signal to achieve the necessary noise immunity :

- measurement of the pulse distance (time base synchronization)
- check of the position of the received bits opening window at the time bases
- check of the parity bit
- check of the absence of pulses between the parity bit and the stop pulse
- check of noise level ; the receiver checks parasitic transients inside and outside the time windows.

If the above test conditions are not fulfilled, the received word is rejected and not decoded. If the received signal is acknowledged as a valid word it is stored an decoded.

The end of transmission will be acknowledged by receiving the end of transmission code or by means of an internal timer if the transmission remains interrupted for more than about 550ms.

Figure 9



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Supply Voltage of TDA2320	R	C
5	2.2kΩ	4.7nF
12	10kΩ	4.7nF

M491B REMOTE CONTROL RECEIVER TRUTH TABLE. Transmitter M708 ; Address Code 9

Command Number	I.R. Code						Function
	C1	C2	C3	C4	C5	C6	
0	0	0	0	0	0	0	End to Transmission
1	1	0	0	0	0	0	Power On/Off
2	1	1	0	0	0	0	Mute On/Off
3	0	0	1	0	0	0	Memory 1
4	1	0	1	0	0	0	Memory 2
5	0	1	1	0	0	0	Memory 3
6	1	1	1	0	0	0	Memory 4
7	1	0	0	0	1	0	Fine Detuning Up
8	1	1	0	0	1	0	Fine Detuning Down
9	0	0	1	0	1	0	Memory 5
10	1	0	1	0	1	0	Memory 6
11	0	1	1	0	1	0	Memory 7
12	1	1	1	0	1	0	Memory 8
13	1	0	0	0	0	1	Memory Up
14	1	1	0	0	0	1	Memory Down
15	0	0	1	0	0	1	Memory 9
16	1	0	1	0	0	1	Memory 10
17	0	1	1	0	0	1	Memory 11
18	1	1	1	0	0	1	Memory 12
19	1	0	0	0	1	1	Manual Search Up
20	1	1	0	0	1	1	Manual Search Down
21	0	0	1	0	1	1	Memory 13
22	1	0	1	0	1	1	Memory 14
23	0	1	1	0	1	1	Memory 15
24	1	1	1	0	1	1	Memory 16
25	1	0	0	1	1	1	Volume Up } Mute
26	1	1	0	1	1	1	Volume Down } Off
27	0	0	1	1	1	1	Memory Addressing
28	1	0	1	1	1	1	Digital AFT On
29	0	1	1	1	1	1	Band Sequential
30	1	1	1	1	1	1	Automatic Search

TAB-04

PINS 12 & 13 : AFT1-AFT2 (STOP AFT INPUTS)

These pins are enabled during the automatic search and during normal operation. when the digital AFT is enabled (see description of pin 17).

The STOP/AFT inputs are also disabled internally during any program or band change for the duration of the Mute signal.

These pins work according to the truth table given below :

M491B Pin 12 TDA4433 Pin 2	M491 B Pin 13 TDA4433 Pin 6	Function (referred to the tuning voltage)
H	L	Up
L	H	Down
L	L	Middle
H	H	No Operation

TAB-05

These inputs have two different functions depending on whether the system is in the search or in normal operation (AFT control).

The inputs have internal pull-up resistors of 30kΩ typ.

A) **Search mode :** after depressing the Automatic search or preset keys, the levels of the signals coming from the TDA4433. applied to these pins, control the search function and determine when the search must stop. i.e. a TV station has been recognized.

The circuit operates in the following sequence (see fig. 10 for reference) :

1 - after pressing the search start key the search occurs in the FAST UP mode.

2 - eventual transitions available on these inputs are ignored during the first 15 search steps if the system is in the UHF or CATV bands.

If the system operates in VHF I and III bands, the first 60 search steps are ignored. The acceptance delay of 15 (60) search steps has been introduced to prevent the system from stopping at the previous station.

After this time the FAST UP speed is automatically reduced to half during each UP signal (MEDIUM UP = FAST UP/2).

A DOWN signal preceded by at least an UP signal will set the search to MEDIUM DOWN mode (FAST UP/4).

3 - the next UP signal will switch the search to SLOW UP speed (61Hz).

At this point the systems is in normal AFT operation.

B) **Digital AFT operation :** when a station is perfectly tuned. the input signals coming from TDA4433 are at middle condition.

If the tuning moves lower than the threshold below 38.9 MHz, the pin 12 is put H and pin 13 is put L ; the 13 bit internal counter is moved SLOW UP speed to increase the varicap voltage.

When a detuning occurs in the opposite direction the input 12 goes Low and 13 goes High and the tuning voltage falls at VERY SLOW DOWN speed (7.6Hz).

The increase or decrease of the tuning voltage is stopped as soon as the input returns to middle conditions.

Therefore during normal operation pins 12 and 13 act as digital AFT control commands.

C) **Recall from memory :** when the digital AFT is enabled and data is recalled from Memory, a fixed value of 8 steps (≈ 31.2mV) is subtracted from the tuning voltage.

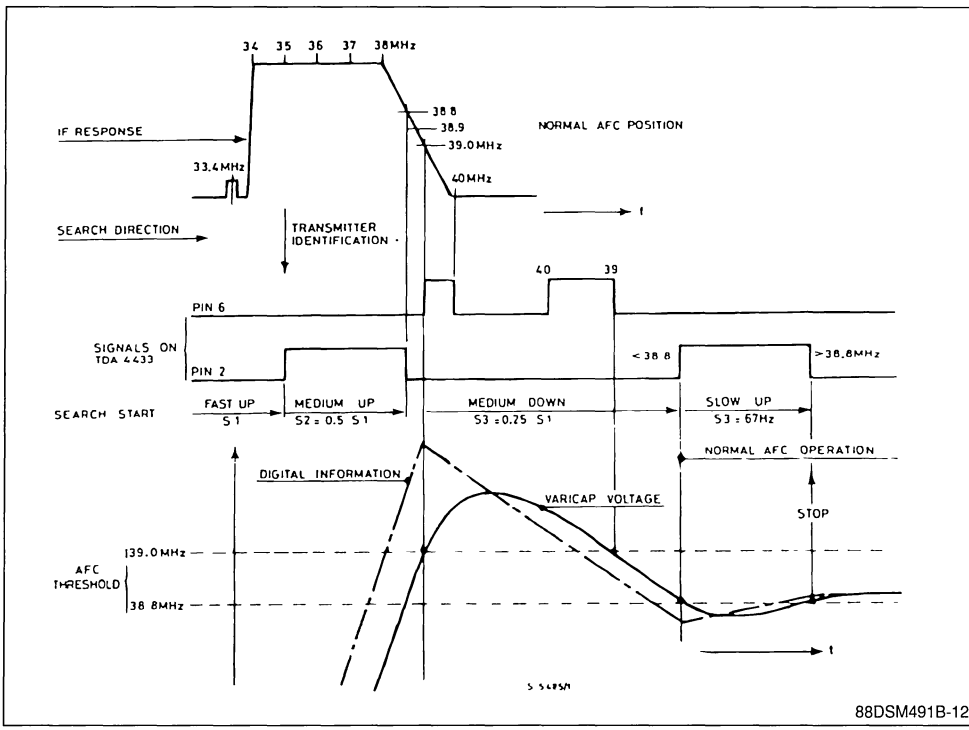
This corresponds to a detuning of 0.6MHz (UHF) and of 0.3MHz in VHF III into that part of the IF response curve which corresponds to the fully transmitted sideband.

At this point the AFT operation takes over as described in point B above and the exact tuning is achieved in about 0.2 sec.

This feature increases the AFT capture range and fullfills the stability requirements of the tuner, voltage references and the D/A converter.

If the Digital AFT is disabled (pin 17 at V_{SS}). the memory content is read without any change.

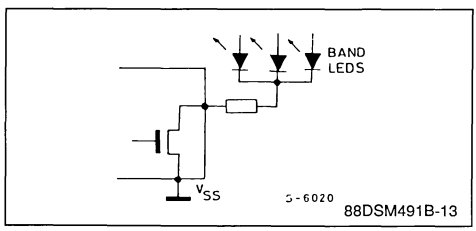
Figure 10



PIN 14 : SWEEP SEARCH DISPLAY OUTPUT

This output, which is normally Low, goes High during automatic search automatic preset et intervals of 160ms for about 40ms to blank the LED of band display.

Figure 11



PIN 15 : VOLUME D/A OUTPUT

This output delivers a square wave signal of 7.8 kHz and duty cycle variable in 63 steps. In case of a continuous command for varying the volume, the duty cycle is changed at the rate of the transmitted signal (approximately every 102ms with f_{ref} = 500kHz) or every 112ms if issued locally.

Overflow and underflow protection are provided.

The volume output can be switched to V_{SS} and reset to the previous level by means of the Mute On/Off command. It is also reset by the Volume Up/Down and the Mains On/Off commands.

The volume is muted for about 1s at each mains on and off command during the power on reset time and program change (0.5s).

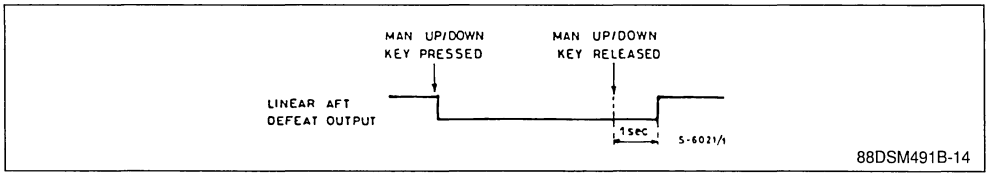
At the first power on reset of V_{DD} the volume D/A is set at the level 21/64. The last level is preserved until V_{DD} is not removed.

PIN 16 : LINEAR AFT DEFEAT OUTPUT

This output is normally High and goes Low when a Manual Up/Down command is issued.

It returns High with a 1 second delay from the release of the key, in order to give the user the possibility of the tuning adjustment without the AFT intervention. It goes Low for 0.5s during program change.

Figure 12



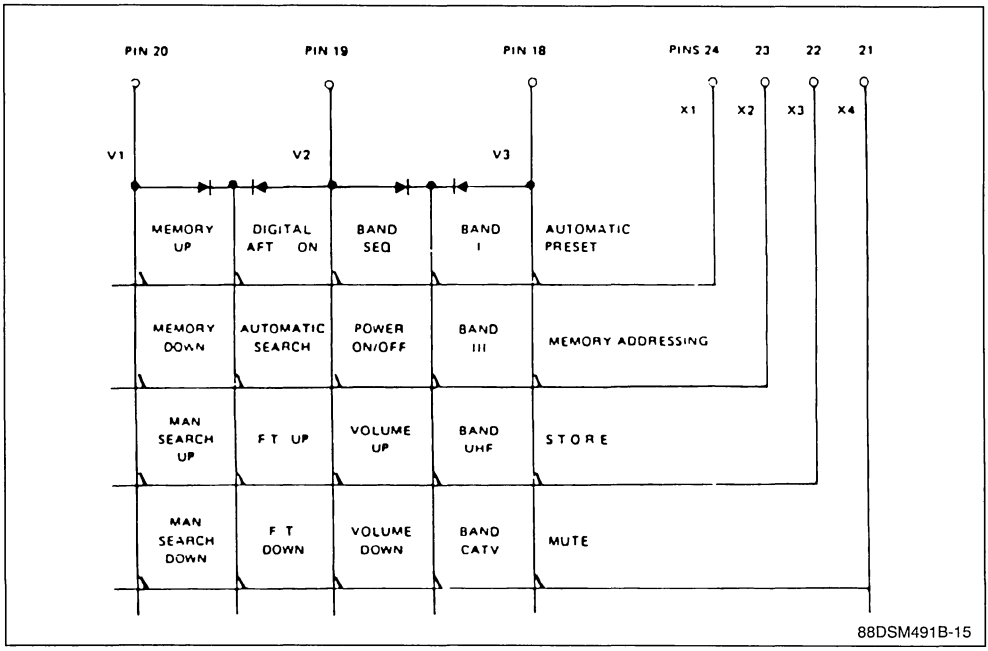
PIN 17 : DIGITAL AFT ENABLE INPUT

If this input is connected to V_{SS} (GND), the digital AFT loop is always disabled. If pin 17 is left open or is connected to V_{DD}, the digital AFT is automatically enabled at power on. When a manual up/down search command is issued, the digital AFT loop is disabled and the digital AFT status output is inhibited.

The digital AFT loop is restored by the commands: Digital AFT on/Automatic search/Automatic preset.

PINS 18-19-20-21-22-23-24 : KEYBOARD MATRIX

Figure 13



A command is accepted if the corresponding contact has been closed for a minimum time of 30ms.

Local input commands and I.R. commands have the same priority.

If a complete I.R. command has been received, the local inputs are blocked until the command has been executed and the "end of transmission code" generated.

Viceversa an I.R. signal cannot be decoded until an issued local command has been executed.

MEMORY UP/DOWN

Depressing one of these two commands, the memory position is stepped in the UP or DOWN direction.

If the key is kept closed, the channels are stepped UP/DOWN every 0.5 second or every 5 commands from the transmitter.

The memory locations 9 to 16 are jumped if pin 31 is at GND level.

BAND SELECTION

The bands can be selected either directly or with a step-by-step command in the following sequence :

VHF I
CATV
VHF III
UHF
VHF I and so on

Only one band change is performed at each accepted command.

Disabled bands are automatically skipped. A band can be disabled connecting the corresponding output to V_{SS}.

SEARCH MODES

4 modes are available :

a) Automatic search } (digital AFT)
b) Automatic preset }
c) Manual up/down (digital and linear AFT)
d) Manual up/down (linear AFT)

a) AUTOMATIC SEARCH. The search starts from the actual tuning and band position. During the search the tuning voltage is always changing from lower to higher voltage levels. When the end of the band is reached the search restarts from the beginning of the next band after a 480 ms interruption with the sequence of step-by-step band selection. Disabled bands are automatically skipped.

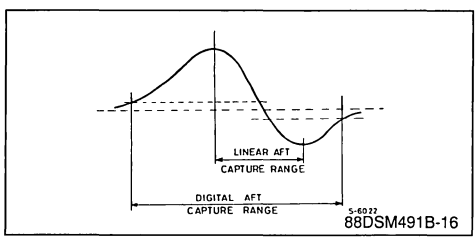
The search is stopped when the first station is found or if a channel selection command is given.

Stop of the automatic search is determined by the STOP/AFT inputs controlled by the TDA4433 which converts the AFC-S-curve into an up/down command.

At the end of the search the up/down command controls the correct tuning acting on the counter of the voltage synthesizer (Digital AFT).

It is important to call the attention to the Digital AFT capture range which is larger than the normal linear AFT as shown in fig. 14.

Figure 14



Additionally the use of the Digital AFT allows storage of the tuning information corresponding to the zero point of the AFC-S-curve. This cannot be guaranteed using the Linear AFT method only. The latter is a cheaper system, because it does not require the use of the TDA4433 but it cannot guarantee what described above.

As a result of the use of the Digital AFT, the requirements for stability of the tuner, of the reference voltage source and of stability of the D/A converter are less critical.

Tuning speed in automatic search, if no station is found is :

VHF I	8 second
VHF III	8 second
UHF	32 second
CATV	32 second

The tuning and band information can be stored using the store/memory addressing command.
The search can be stopped by a memory selection command.

b) AUTOMATIC PRESET. The search starts from the lowest memory address, tuning voltage and VHF I band as described in automatic search mode.

When an active station is encountered, the corresponding tuning and band information is automatically stored in the Non-Volatile Memory.

Afterwards the system starts to search for the next station. The cycle is repeated until all bands have been scanned or the tuning information has been stored into all address locations. After completing this cycle the system reads out the tuning information of the lowest address.

c) MANUAL UP/DOWN WITH DIGITAL AND LINEAR AFT (pin 17 at V_{DD}). Holding one of these commands pressed, the tuning voltage is increased or decreased.

During this operation, the Digital AFT is automatically defeated and can only be reconnected with the "AFT on" command or by an Automatic search or preset command.

The search speed is kept at minimum (there is no increment with the time)

Band	Sweep Time for the Complete Band	Number of Tuning Steps/Second
VHF I	128 seconds	64
VHF III	128 seconds	64
UHF	512 seconds	16
CATV	512 seconds	16

In case of command received from remote control, the counter is increased/decreased every two received commands.

No band switching is provided at the upper or lower tuning positions.

The volume is automatically muted 3 second after the key pressure is immediately restored at the release of the key.

d) MANUAL UP/DOWN WITH LINEAR AFT (pin 17 at V_{SS}). When this control is used the Digital AFT is disabled.

The Linear AFT output goes low after an up or down command is issued and remains Low for 1 second after the release of the key.

The volume is automatically muted for 3 seconds after the key pressure and is immediately restored at the release of the key.

Tuning speeds are as follows :

FINE TUNING UP/DOWN
See description of pin 4.

DIGITAL AFT ON
See description of pin 17.

VOLUME UP/DOWN
See description of pin 15.

MAINS ON/OFF
See description of pins 25 and 26.

Band	Number of Tuning Steps Second			
	Time 0	After 1 s	After 2 s	After 3 s
VHF I	64	128	256	512
VHF III	64	128	256	512
UHF	16	32	64	128
CATV	16	32	64	128

TAB-06

STORE COMMANDS

2 modes of operations are available.

a) store

b) memory addressing

In order to protect the memory, the store function is internally disabled after one store cycle.

It is enabled after a program change or a tuning operation (it is not disabled by the Digital AFT control).

a) STORE. The tuning information (Tuning D/A, Fine tuning D/A and band) is stored in a previously selected memory address when this command is issued.

b) MEMORY ADDRESSING. The tuning information can also be stored with this command followed by the memory position selection.

When this command is accepted all the memory LEDs are blanked.

Selection of the memory position initiates the store operations and restores the display.

MUTE ON/OFF

See description of pin 15.

PIN 25 : MAINS ON OPTION INPUT

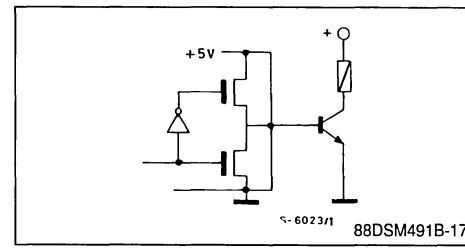
If connected to V_{SS} (GND) the Mains output is automatically switched on when V_{DD} is applied and memory 1 is read.

If it is connected to V_{DD} the circuit goes in stand by condition.

PIN 26 : MAINS ON/OFF OUTPUT

Switch on of the set is controlled by the Mains on command issued for more than 0.3 s. The output transistor is set in the off condition to drive through an integrated pull-up resistor, an external NPN transistor.

Figure 15



At each Mains on command a memory read out occurs. A V_{PP} (+ 25 V) is required for this operation, a 1 second delay starts when the mains output is switched off. For a correct reading of the memory the V_{PP} supply voltage must reach the value of 25 V within 1 second after a Mains on command.

In case of automatic switch on at power on caused by pin 25 at GND, the total delay is of 1.13 second (0.13s for V_{DD} power on reset plus 1 second for mains on).

The Mains on/off command, if repeated, will switch the output on (set off).

The last address information is preserved until V_{DD} is present.

Next Mains on command will switch the set at the previously selected memory address and a read operation will be performed.

PINS 27-28-29-30-33-34-35-36 : MEMORY ADDRESS OUTPUT

These pins operate as output only for display of the selected memory location. Max drive capability is of

15 mA/1.2 V with the exception of pin 36 that is of 30 mA/1.5 V.

Direct memory selection is only possible by remote control. A local memory up/down command is available in case of emergency.

Pin 32 must be grounded.

If pin 31 is grounded, the memory position 9 to 16 are skipped in case of memory up/down commands.

For normal operation pin 31 can be left open or, better, connected to V_{DD}.

PINS 31-32

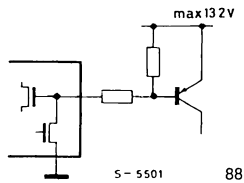
See description of pins 27 to 30 and 33 to 36.

PINS 37-38-39-40 : BAND INPUT/OUTPUT

These outputs are provided to select up to 4 bands via external PNPs.

If one or more bands have to be skipped, the corresponding outputs have to be short-circuited to V_{SS}.

Figure 16

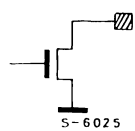


88DSM491B-18

The relation between pins and bands are as follows :
pin 37 = UHF
pin 38 = CATV
pin 39 = VHF III
pin 40 = VHF I

INPUT/OUTPUT CONFIGURATION

Output Open Drain.

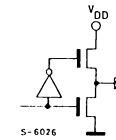


88DSM491B-19

Pins 3, 4, 5, 6, 14, 15, 16, 31, 32 (M490B)

Pins 3, 4, 5, 6, 14, 15, 16, 27, 28, 29, 30, 33, 34, 35, 36 (M491B)

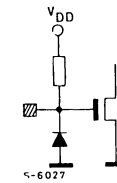
Output Push-pull.



Pin 26.

88DSM491B-20

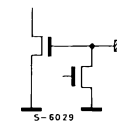
Inputs with Pull-up Load.



88DSM491B-21

Pins 12, 13, 17, 18, 19, 20, 25, 31

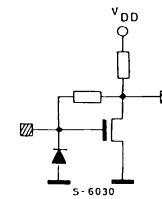
Inputs/Outputs (std)



88DSM491B-22

Pins 37, 38, 39, 40, 21, 22, 23, 24 (21, 22, 23, 24 are used only for testing purposes).

Oscillator.

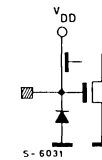


Pin 8

Pin 7

88DSM491B-23

IR Input.

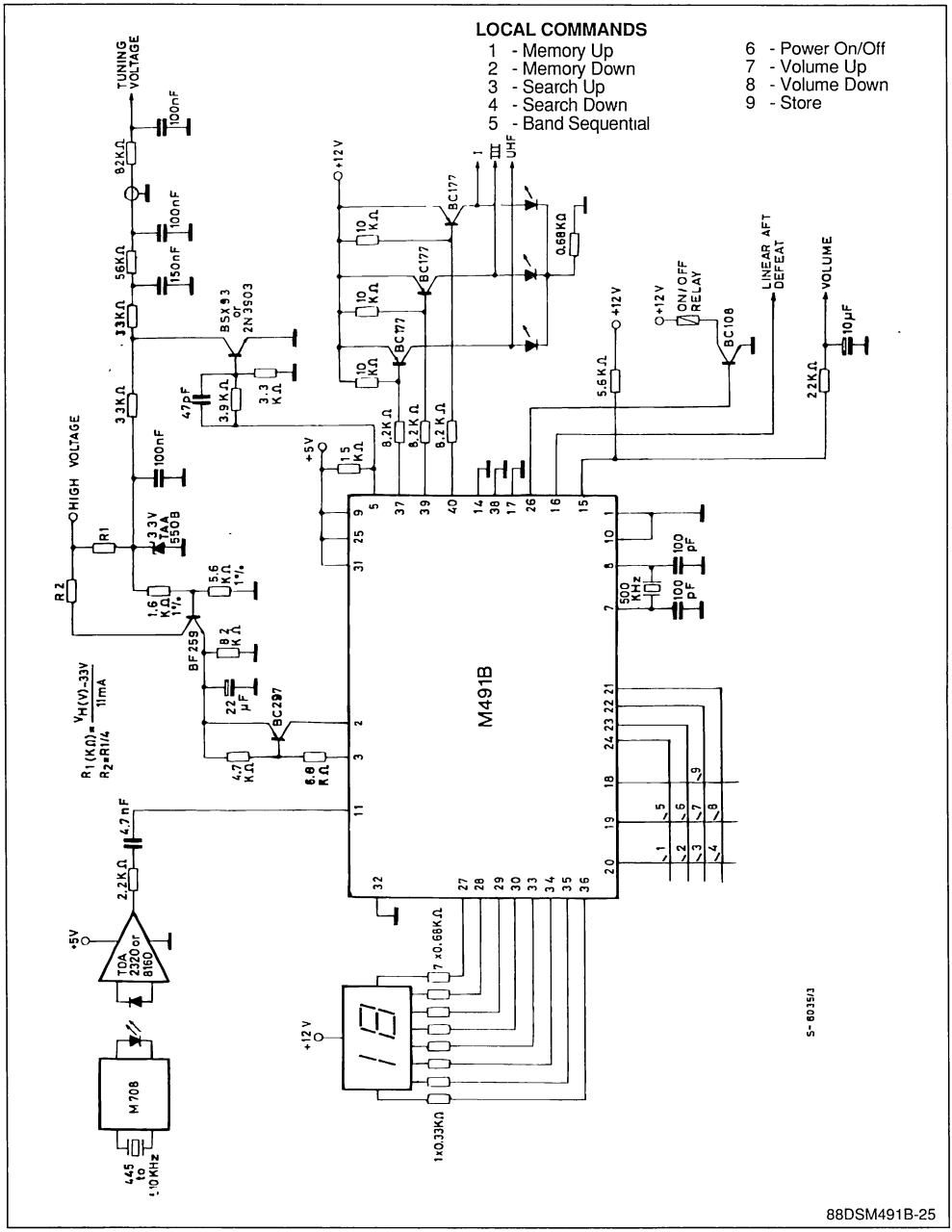


Pin 11

88DSM491B-24

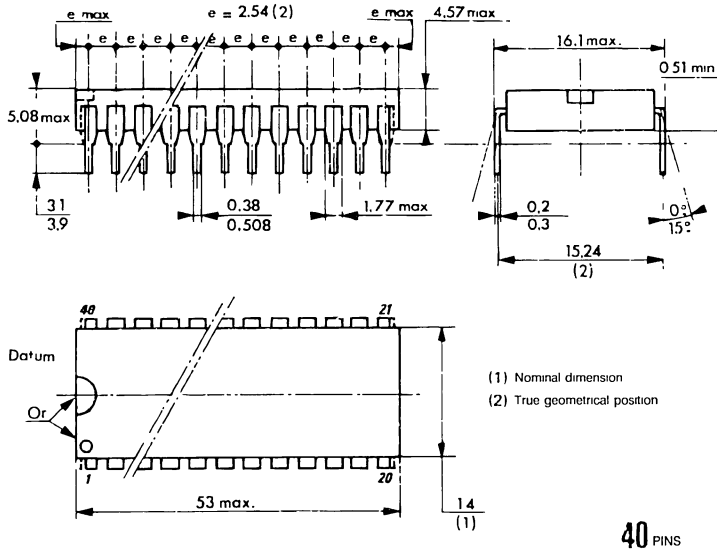
TYPICAL APPLICATION

Manual Search with Linear AFT (16 memory option)



PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

M494

SINGLE-CHIP VOLTAGE TUNING SYSTEM WITH 4 ANALOG CONTROLS AND μP INTERFACE

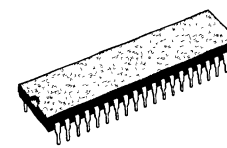
- NON-VOLATILE MEMORY FOR 20 PROGRAM WORDS (17 BIT x 20)
  - TUNING VOLTAGE 12 BITS
  - BAND 2 BITS
  - MULTI STANDARD 2 BITS
  - PROGRAM SKIP BIT 1 BIT
  - 10,000 MODIFY CYCLES PER WORD
  - MIN. 10 YEARS DATA RETENTION
- 13 BIT VOLTAGE SYNTHESIZER (BRM + PWM)
- NV MEMORY FOR 4 ANALOG CONTROLS (6 BIT x 4)
- 4 BAND SWITCH OUTPUTS (VHF I & III, UHF, CATV)
- 5 x 7 KEYBOARD
- 2 AUDIO VISUAL OUTPUTS (VCR & PC)
- 2 CODED MULTI STANDARD OUTPUTS (e.g. PAL, SECAM, NTSC etc.)
- DIRECT 1 1/2 DIGIT 7 SEGMENT COMMON ANODE LED DISPLAY DRIVING
- PCM REMOTE CONTROL RECEIVER (M708 transmitter)
- 5-BIT DATA INPUT + CONTROL LINE FOR P INTERFACE
- LINEAR AFC DEFEAT OUTPUT
- FLYBACK/SYNC. COINCIDENCE INPUT FOR SEMIAUTOMATIC SEARCH
- STANDBY OUTPUT
- OPTION SELECT :
- 16 OR 20 PROGRAMS
- POWER UP MODE
- PROGRAM SKIP DEFEAT
- AV OPTIONS
- 1 * OR DECADE MODE OPTION IN 20 PROGRAM OPTION
- TEMPORARY ANALOG UP/DOWN INDICATOR ON LED DISPLAY
- BAND SKIP OPTION
- 455 TO 510KHz CHEAP CERAMIC RESONATOR
- V_{DD} = 5V ± 5%. V_{PP} = 25V ± 1V

DESCRIPTION

The M494 is a monolithic LSI integrated circuit fabricated in SGS-THOMSON's EPM2 process ; an N-channel, Planox, double poly MOS process capable of including a floating gate NV memory cell (EEPROM).

The i.c. has been designed as a complete digital TV tuning system based on the voltage synthesis principle and as a replacement for all the conventional potentiometers and band switches particularly in low cost TV sets. It also provides some functions normally only associated with higher cost sets. NV memory is integrated on the chip together with all the necessary control circuitry to provide the program memory. Separate NV memory is also integrated to provide the memory for four analog controls. A seven segment LED display can be directly driven by the chip to display the program selected, and the direction of movement of the analog controls. Provision is made for a remote control receiver both on and off chip, the latter is interfaced via a data input and single control line. (This enables control by a microprocessor). A local keyboard can be used with the device in a variety of configurations. An option select pin provides for different program number options, power up options and skip associated functions. This device is another significant step towards the complete integration of TV control circuitry.

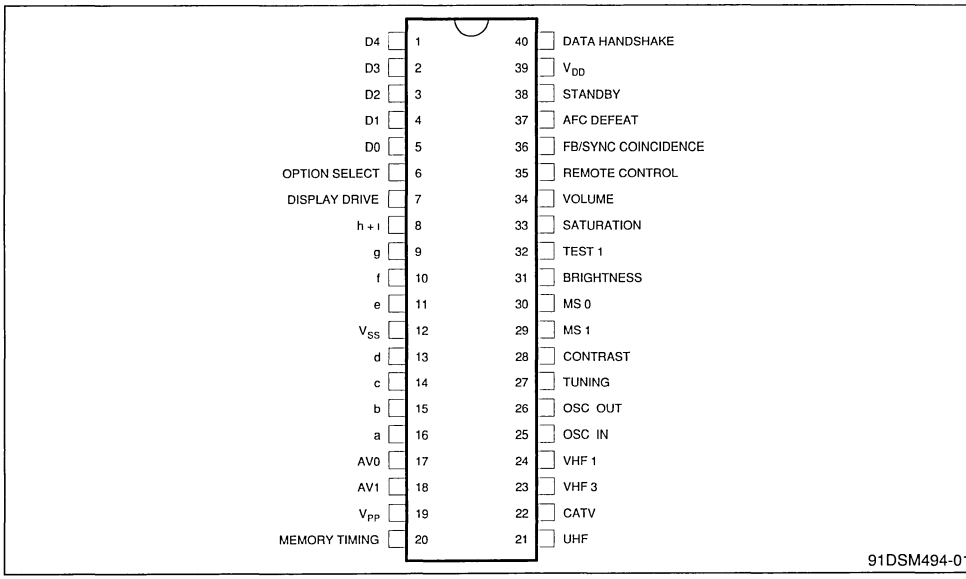
The device is packaged in a 40 pin DIL plastic package.



DIP40
(Plastic Package)

ORDER CODE : M494B1

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7	V
V_{PP}	Memory Supply Voltage	– 0.3 to 26	V
V_I	Input Voltage	– 0.3 to 15	V
$V_{O(off)}$	Off State Input Voltage	15	V
I_{OL}	Output Low Current LED Driver Outputs : pin a-g pin h + i All other Outputs	 20 35 5	 mA mA mA
t_{PD}	Max. Delay between Memory Timing & Memory Supply Pulses	5	µs
P_{tot}	Total Package Power Dissipation	1	W
T_{stg}	Storage Temperature	– 25 to + 125	°C
T_{op}	Operating Temperature	0 to + 70	°C
C_{os}	Capacitance on Option Select Pin	100	pF
R_{os}	Resistance on Option Select Pin	1	kΩ
C_{dk}	Capacitance on data outputs & keyboard inputs when lines are connected by a keyboard switch closure	150	pF
R_k	Series Resistance of Single Keyboard Switch	10	kΩ
C_{rts}	Capacitance on Data Handshake Pin	50	pF

TAB-01

Stresses above those under "Absolute Maximum Ratings" may causes permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DEFINITION OF TERMS

The M494 has four conditions or states that it can be in which are defined below. Logic LO 0V and logic HI ≡ 5V.

POWERED DOWN

V_{DD} = 0V. V_{PP} = 0V

ON

V_{DD} = 5V. V_{PP} = 25V. Device driving display normally. Data Handshake pin configured as RTS i/p. Standby o/p = HI. All other functions operating normally.

STANBDBY

V_{DD} = 5V. V_{PP} = 0V. Device driving display to show a single static bar (g segment). Data Handshake pin configured as RTS i/p. Standby o/p = LO. All keyboard commands are disabled except any program command On/Off. On/Standby. Memory sequence up or down, 1 * and ±10 (decade) commands. All RC and Data commands are disabled except any program command, On/Standby, Memory sequence up or down, 1 * and ±10 (decade) commands. Analog controls. Tuning, AV, MS and AFC defeat o/p's = LO. Band o/p's = HI (externally pulled up). See Standby section for more detail.

OFF

V_{DD} = 5V. V_{PP} = 0V. Device not driving display. Data Handshake pin configured as OFF o/p. Standby o/p = LO. Display disabled and Display drive o/p = HI (externally pulled up). All keyboard commands disabled except ON/OFF. Remote and data command sources disabled. Analog controls, Tuning, AV, MS and AFC defeat o/p's = HI (externally pulled up).

STATIC ELECTRICAL CHARACTERISTICS

(T_{amb} = 0 to 70°C, V_{DD} = 5V unless otherwise specified)

Pins	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Memory Supply	I_{PP}	Memory Supply Current	V_{PP} = 25V Write Peak Average Erase Peak Average Read Peak Average			 35 10 9 5 8 2.5	 mA mA mA mA mA mA
	R	Pull Down				25	kΩ
Memory Timing	V_{OL}		V_{DD} = 4.75V, I_{OL} = 2.5mA			8	V
	$I_{O(off)}$	Leakage	V_{DD} = 4.75V, V_O = 26V			100	µA
Tuning	V_{OL}		V_{DD} = 4.75V, I_{OL} = 5mA			1	V
V_{DD}	I_{DD}	Supply Current	V_{DD} = 5.25V			100	mA
RC	V_I	pk to pk		0.5		13.2	V
FB/sync. Coin. Input	V_{IL}					0.8	V
	V_{IH}			2.0			V
	I_{IL}		V_{DD} = 5.25V, V_{IL} = 0.8V			– 0.4	mA
	R	Pull up			30		kΩ
Vol. Brigh. Sat. Contr. DACs	V_{OL}		V_{DD} = 4.75V, I_{OL} = 4mA			1	V
	$I_{O(off)}$		V_{DD} = 5.25V, V_O = 13.2V			50	µA
h + i	V_{IL}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25V, V_{IL} = 1.5V			– 50	µA
	R	Pull up			200		kΩ
	V_{OH}		V_{DD} = 4.75V, I_{OL} = 30mA			1.5	V

TAB-02

STATIC ELECTRICAL CHARACTERISTICS (continued)

Pins	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
D0, D1 D2, D3 D4	V_{IL}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25V, V_{IL} = 1.5V			– 0.4	mA
	V_{OL}		V_{DD} = 4.75V, I_{OL} = 1mA			0.4	V
	$I_{O(off)}$		$V_{O(off)}$ = 5.5V			25	µA
	R	Pull up			30		KΩ
MS0, MS1 AFC def. AV0, AV1	V_{OL}		V_{DD} = 4.75V, I_{OL} = 1mA			0.4	V
	$I_{O(off)}$		V_{DD} = 5.25V, V_O 13.2V			50	µA
Option Select	V_{IL}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25V, V_{IL} = 1.5V			– 0.4	mA
	R	Pull up			30		kΩ
Standby	V_{OL}		V_{DD} = 4.75V, I_{OL} = 100µA			0.4	V
	I_O		V_{DD} = 4.75V, V_O = 0.7V			1.6	mA
a, b, c, d, e, f, g	V_{IL}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25V, V_{IL} = 1.5V			– 50	µA
	R	Pull up			200		kΩ
	V_{OL}		V_{DD} = 4.75V, I_{OL} = 15mA			1.5	V
Display Drive	V_{OL}		V_{DD} = 4.75V, I_{OL} = 5mA			0.4	V
	$I_{O(off)}$		V_{DD} = 5.25V, V_O = 13.2V			50	µA
UHF, III I, CATV	V_{OL}		V_{DD} = 4.75V, I_{OL} = 1mA			3	V
	V_{OH}		V_{DD} = 4.75V, I_{OH} = – 150µA	2.4			V
	V_{IL}					1.5	V
	V_{IH}			3.5			V
	$I_{O(off)}$		V_{DD} = 5.25V, V_O = 13.2V			50	µA
Data Handshake	V_{OL}		V_{DD} = 4.75V, I_{OL} = 1mA			3	V
	V_{OH}		V_{DD} = 4.75V, I_{OH} = 150µA	2.4			V
	V_{IH}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25V, V_{IL} = 1.5V			– 0.4	mA
	R	Pull up			30		kΩ
	$I_{O(off)}$		V_{DD} = 5.25V, V_O = 13.2V			50	µA

TAB-03

FUNCTIONAL DESCRIPTION
(clock frequency = 500kHz)

V_{DD} & V_{SS}

V_{DD} = + 5V ± 5%. When applied, an internal power on reset of 110ms is generated. The voltage threshold for the reset is in the range 3 to 3.5V but is in fact the point at which the internal clock phases start.

V_{SS} = 0V. This pin is connected to the substrate of the i.c. and is the reference for all parameters of the device.

OSCILLATOR I/O

The frequency of the oscillator should be between 445 and 510kHz using a cheap ceramic resonator. The reference frequency of the remote control transmitter must also be in the same range i.e. if the oscillator frequency is 455kHz then the transmitter frequency could be 510kHz or vice versa.

TEST

This pin is normally used for post fabrication testing purposes only and should be tied to V_{SS}. However this pin can be used by SGS-THOMSON Microelectronics or the OEM to enable external loading of the memory. Details of how to achieve this can be furnished by SGS-THOMSON.

REMOTE CONTROL INPUT

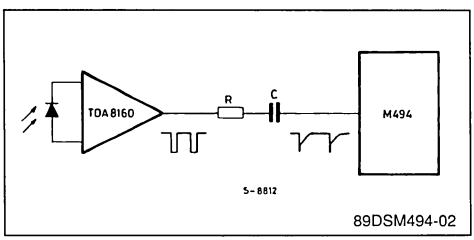
The integrated RC receiver decodes signals transmitted by the M708 (address 10). The minimum signal amplitude should be 0.5V peak to peak at the input pin. The minimum pulse width should be 8µs.

The signal from the preamplifier (TDA8160) is brought to the RC signal input via an AC coupling network (see fig. 1).

V_{DD} (TDA8160)	R	C
5V	2.2kΩ	4.7nF
12V	10kΩ	4.7nF

TAB-04

Figure 1.



The input is self biased to approx. 1.5V. When a large signal is applied to the input a level shift will take place predominantly due to the coupling network. However another time constant is also visible due to the coupling C and the internal resistor R_i. (see figs. 2 & 3).

Figure 2 .

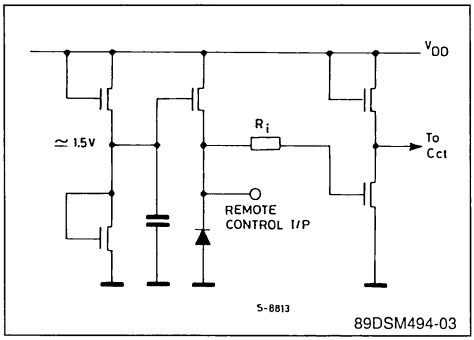
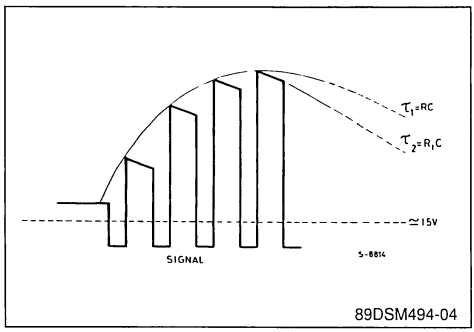


Figure 3 .



Several tests are performed on the signal :

a) Measurement of the pulse distance T (time base synchronization).

b) Check of the bit positions relative to the time base windows.

c) Check of the parity bit.

d) Check of the absence of pulses between parity and stop pulses.

e) Check of the noise level. The receiver checks the noise level for a time T after each pulse detected.

If all these tests are successful the received word is stored and decoded. If not it is rejected. The transmission is terminated on reception of the end of

transmission (EOT) code or if the internal timer measures a transmission interruption of more than 550ms. For more detail concerning the operation of the RC receiver refer to SGS-THOMSON Technical Note No. 155 pp11-12.

The RC receiver and the local keyboard have the same command source priority i.e. a local command is not accepted until a previously accepted RC command has been completely executed and the EOT code transmitted. Similarly if a local command is under execution then an RC command will not be accepted. The RC truth table and commands are shown on the next page.

ANALOG CONTROL OUTPUTS

Four analog control outputs are implemented to provide for Volume, Brightness, Saturation and Contrast from four 6 bit D/A's. These D/A's use the Pulse Width Modulation technique to synthesize a pulse train of constant frequency but variable pulse width (PWM). Each output delivers a 7.8kHz square wave whose duty cycle is variable in 63 steps. External RC filtering and level shifting is required to realise a static DC voltage from the pulse train. If the analog outputs are continuously varied by command from the keyboard or data command sources the outputs will change approx. every 112ms (fck = 500kHz) or approx. every 102ms if the command is issued from the RC command source. One analog control is specifically designed as a volume control as mute circuitry is built in.

On start up reset the analog control outputs except volume are enabled after a period of approx. 1.1 seconds. In the Standby and Off states all the analog control outputs are pulled to logic LO.

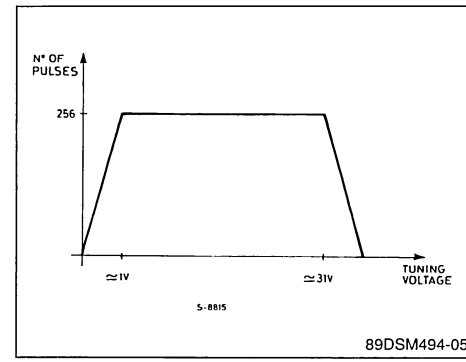
The normalise command reads the contents of each analog memory sequentially to its corresponding counter and D/A output.

TUNING OUTPUT

The tuning voltage is generated from a 13 bit counter. The program memory stores the 12 MSB's of the tuning word. The range of the AFC circuitry is at least 3 bits so the LSB of the tuning counter does not affect the resolution of tuning.

The contents of the counter are converted using a PWM and a Bit Rate Multiplier (BRM) technique. 13 bits gives 8192 steps which yields a resolution of approximately 3.9mV with a max. tuning voltage of 32V. This corresponds to a resolution of about 75kHz in the UHF band. The 5 MSB's of the tuning word are converted using PWM and the remaining 8 bits using BRM. Thus as the tuning word increases from all zeroes the number of pulses in one period increases to 256 with all the pulses being the same length (t_o = 2µs). For values larger then 256 PWM conversion takes place where the number of pulses in one period stays constant at 256 but the width changes. When the pulse width reaches $15t_o$ two successive pulses "link" together and the number of pulses decreases. (see fig. 4).

Figure 4 .



The pulse train is fed to an external low pass filter to realise a DC voltage. The temperature dependence of this system is predominantly the switching times of the output pulses and as there are only a maximum of 256 pulses in one period the temperature stability is very good.

In Standby and Off states the tuning output is pulled to logic LO.

M494 REMOTE CONTROL COMMANDS (address 10, code = 1010)

M708 Command Number	Function		Code					
	16 Programs	20 Programs	C1	C2	C3	C4	C5	C6
0	EOT	EOT	0	0	0	0	0	0
1	Standby	Standby	1	0	0	0	0	0
2	Mute (toggle)	Mute (toggle)	1	1	0	0	0	0
3	Program 1	Program 1	0	0	1	0	0	0
4	Program 2	Program 2	1	0	1	0	0	0
5	Program 3	Program 3	0	1	1	0	0	0
6	Program 4	Program 4	1	1	1	0	0	0
7	Contrast up	Contrast up	1	0	0	0	1	0
8	Contrast down	Contrast down	1	1	0	0	1	0
9	Program 5	Program 5	0	0	1	0	1	0
10	Program 6	Program 6	1	0	1	0	1	0
11	Program 7	Program 7	0	1	1	0	1	0
12	Program 8	Program 8	1	1	1	0	1	0
13	Memory Seq. up	Memory Seq. up	1	0	0	0	0	1
14	Memory Seq. down	Memory Seq. down	1	1	0	0	0	1
15	Program 9	Program 9	0	0	1	0	0	1
16	Program 10	Program 0	1	0	1	0	0	1
17	Program 11	– 10 (decade)	0	1	1	0	0	1
18	Program 12	+ 10 (decade)	1	1	1	0	0	1
19	Normalise	Normalise	1	0	0	0	1	1
20	On/stby (tog.)	On/stby (tog.)	1	1	0	0	1	1
21	Program 13	1*	0	0	1	0	1	1
22	Program 14	NOP	1	0	1	0	1	1
23	Program 15	NOP	0	1	1	0	1	1
24	Program 16	NOP	1	1	1	0	1	1
25	Volume up	Volume up	1	0	0	1	1	1
26	Volume down	Volume down	1	1	0	1	1	1
27	Brightness up	Brightness up	0	0	1	1	1	1
29	Brightness down	Brightness down	0	1	1	1	1	1
28	Saturation up	Saturation up	1	0	1	1	1	1
30	Saturation down	Saturation down	1	1	1	1	1	1

TAB-05

The above table showns the difference between the 16 and 20 program options with respect to the remote control commands. Commands 16, 17, 18 &21 change function between the two options. Commands 22, 23 & 24 should not be used in the 20 program option, as they have no function.
NOP = No operation

PROGRAM MEMORY

NV memory (EEPROM) is integrated on the chip to provide storage for up to 20 stations. Each memory location is 17 bits in length providing 12 bits for tuning voltage, 2 bits for band, 2 bits for two coded multistandard outputs and 1 bit program skip flag. Individual program words can be read on command from the keyboard, remote or data command sources but can only be written on command from the keyboard. There are two methods for storing a program (writing the memory) : pre and post tuning selection of the program number. See Commands, section 7. Reading each memory location in sequence (up or down) can also be achieved from all the command sources.

All memory timing functions are provided on chip and only one external transistor is required to switch the external memory supply (25V). There are essentially two operations carried out on the memory : Write/Modify and Read. The Write/Modify cycle consists of 3 steps :

a) All "1s" are written to the bits of the addressed word.

b) All bits of the word are erased.

c) The new contents are written.

Using this method all the bits of the addressed word are aged the same. For more detail concerning the write, erase and read current waveforms at the Memory Supply pin see M491 datasheet.

MEMORY FOR ANALOG CONTROLS

The memory for the analog controls is electrically identical to the main program memory but is organised as four 6 bit words located in two sequentially addressed words at the memory. Each word
corresponds to the Volume, Brightness, Saturation and Contrast outputs. At power on reset and normalise command each memory word is read out to its corresponding counter and D/A in sequence.

DISPLAY, KEYBOARD AND DATA MULTIPLEXING

Logic is integrated on the chip to provide the multiplexing between the display, keyboard and data inputs. In the On state and with the Data Handshake pin at logic HI as an input the display and keyboard are muxed together. See fig. 5. Each column output goes to logic LO in sequence and the row inputs are scanned for a key closure. In chronological order across the total mux. period there is : initialisation, scan, decision and display periods.

The Data Handshake pin has a complex logical function. It has two modes of operation : as a hand shake I/O line to a µP and as an output line to the P to signal that the M494 is in the Off state. In order to achieve this function careful signal timing is required both internally and externally to the chip. See fig. 6. When the device is in the OFF state the Data Handshake pin is used to signal this condition to the µP by being pulled LO.

Figure 5 .

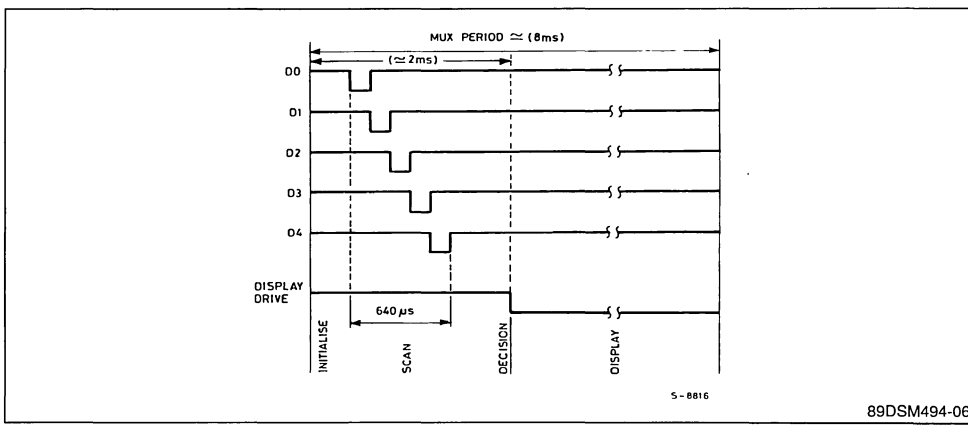
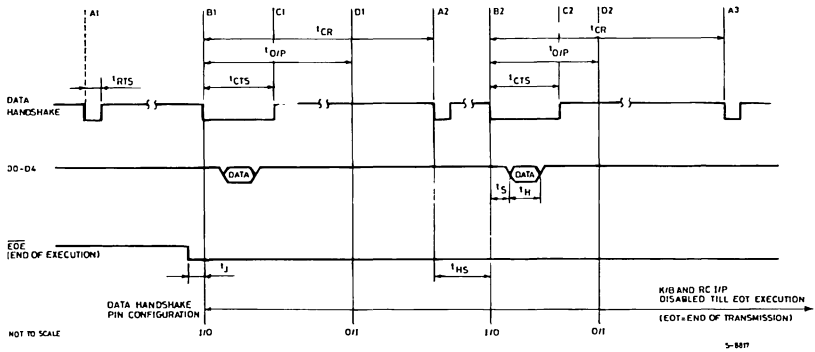


Figure 6 : Data-input-timing.



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N°	Symbol	Parameter	Min	Typ	Max	Unit
1	t_{RTS}	Request to Send Pulse (RTS)	5		10	µs
2	t_{CTS}	Clear to Send (CTS)		512		µs
3	$t_{O/P}$	Pin Output Configuration		8		ms
4	t_{HS}	Handshake Time	12			µs
5	t_S	Data Set up Time	10		128	µs
6	t_H	Data Hold Time	128		256	µs
7	t_J	Synchronization Jitter			8	ms
8	t_{CR}	CTS to next RTS Pulse		98		ms

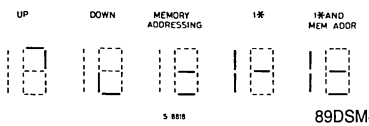
TAB-06

Note : Oscillator Clock = 500kHz.

DISPLAY

The M494 is capable of directly driving a 1 digit common anode LED display at the max. sink current of 15mA per segment. The h+i pin is capable of sinking a max. current of 30mA so that these two segments can be driven from the same pin and be the same brightness as the other segments.

On instruction from the internal command decoder the display shows programme number, direction of analog control movement, decade change or Memory Addressing function active. Analog controls in this context are defined as Tuning, Volume, Contrast, Saturation & Brightness. The formats of the display for analog control direction, decade change and Memory Addressing are shown below respectively :



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For the analog controls the above condition is displayed with an "overrun" time of 300ms. i.e. the display will show the "arrows" for a period of 300ms after the release of any analog control up or down key. The Memory Addressing function display flashes at 5Hz after the Memory Addressing function is commanded and continues to flash until a programme is selected or any other command is given. In 1 * the g segment only flashes at 5Hz and continues to flash until a programme number is selected or any other command is given. If in Memory Addressing and 1 * is pressed then the display above is shown with segments g & d only flashing at 5Hz until a programme number is selected or any other commands is given. When Store or Set Skip Flag commands are executed the whole display is flashed at 5Hz for 1 second.

KEYBOARD

It is possible to implement a keyboard with a max. size of 35 keys as a 5 x 7 array. Fig. 8 shows the arrangement of the key matrix. Each key connects a row (a-g) with a column (D0-D4) with a max. resistance of 10KΩ. De-bounce logic is integrated on the chip that only allows acceptance of a command if the key is closed for longer than 40ms except for the On/Standby and On/Off commands where the relevant keys must be closed for approximately 100ms. This is equivalent to 2 received RC commands).

For the main keyboard matrix (a-g x D0-D4), if the logic detects two keys closed simultaneously the display is blanked to indicate this condition to the user and no command is executed. When the logic detects only one key pressed the display will re-illuminate and the command be executed.

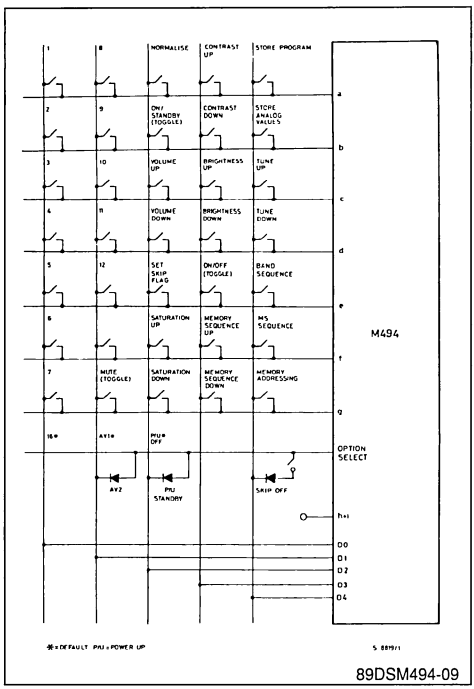
This avoids confusion as to which command should be executed and provides feed back to the user. For the Option select line all options/commands can be active simultaneously.

1 * mode or decade mode can be selected on the option select line by the presence of a diode or not respectively. These two modes are only active for the 20 program option and are described below :

In 1 * mode the display will toggle in & out of the condition shown in the Display Section. Access to programs in the first decade is made by simply pressing any 0-9 program key and access to programs in the second decade, whatever the current program is made by pressing 1 * followed by any 0-9 program key.

In decade mode on pressing either ±10 (decade) keys the display will light or extinguish the half digit respectively and simultaneously effect the tuning information. e.g. if the device is in program 3 pressing + 10 (decade) key will give program 13 and then pressing - 10 (decade) key will give program 3. Pressing - 10 (decade) again will have no effect.

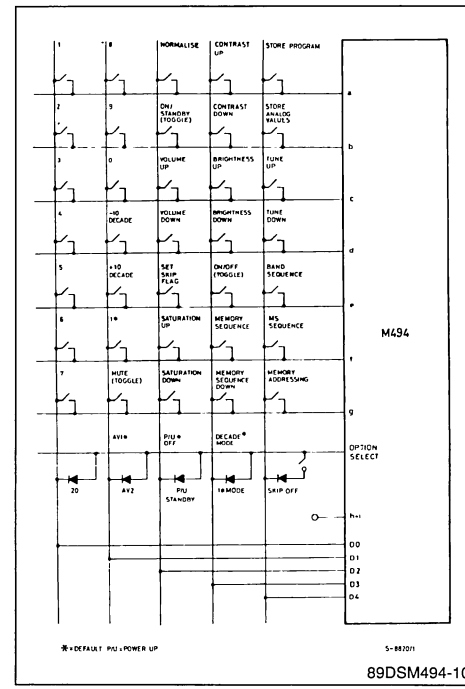
Figure 7 : Keyboard 16 Programs.



The 20 program option select acts like an enable for the 1 * or decade modes. i.e. the 1 * or decade modes are only selectable in the 20 program option. In 16 program option the function of the 1* key, program key 0, -10 (decade) & + 10 (decade) are changed to no function, programme 10, 11 & 12 respectively. i.e. The difference between fig. 7 & 8 for those keys that change function.

If the 1 * key is pressed followed by brightness up for example the device will increase the brightness only and reset the 1 * command **i.e. the last command from any command source will always be executed if it is a single keystroke command and the 1 * command will be reset by it.** It is possible to press the 1 * key on the keyboard and then a program 0-9 command from RC or Data command sources or vice versa. Thus there are 2 methods of selecting a program from the keyboard for the 16 program option : direct access (only up to 12 programs) or Memory sequence up/down. And there are 3 methods of selecting a program from the keyboard for the 20 program option : 1 * mode, decade mode and Memory sequence up/down.

Figure 8 : Keyboard 20 Programs.



DATA INPUT
Shown below are the codes for the commands :

M494 DATA COMMANDS

Command Number	Function		Code				
	16 Programs	20 Porgrams	D0	D1	D2	D3	D4
0	EOT	EOT	0	0	0	0	0
1	Program 1	Program 1	1	0	0	0	0
2	Program 2	Program 2	1	0	0	0	0
3	Program 3	Program 3	1	1	0	0	0
4	Program 4	Program 4	0	0	1	0	0
5	Program 5	Program 5	1	0	1	0	0
6	Program 6	Program 6	0	1	1	0	0
7	Program 7	Program 7	1	1	1	0	0
8	Program 8	Program 8	0	0	0	1	0
9	Program 9	Program 9	1	0	0	1	0
10	Program 10	Program 0	0	1	0	1	0
11	Program 11	– 10 (decade)	1	1	0	1	0
12	Program 12	+ 10 (decade)	0	0	1	1	0
13	Program 13	1*	1	0	1	1	0
14	Program 14	NOP	0	1	1	1	0
15	Program 15	NOP	1	1	1	1	0
16	Program 16	NOP	0	0	0	0	1
17	Normalise	Normalise	1	0	0	0	1
18	Volume up	Volume up	0	1	0	0	1
19	Volume down	Volume down	1	1	0	0	1
20	Contrast up	Contrast up	0	0	1	0	1
21	Contrast down	Contrast down	1	0	1	0	1
22	Brightness up	Brightness up	0	1	1	0	1
23	Brightness down	Brightness down	1	1	1	0	1
24	Saturation up	Saturation up	0	0	0	1	1
25	Saturation down	Saturation down	1	0	0	1	0
26	Memory Seq. up.	Memory Seq. up.	0	1	0	1	1
27	Memory Seq. down	Memory Seq. down	1	1	0	1	1
28	On/standby (toggle)	On/standby (toggle)	0	0	1	1	1
29	Standby	Standby	1	0	1	1	1
30	Mute (toggle)	Mute (toggle)	0	1	1	1	1
	NO TRANSMISSION (pulled up)		1	1	1	1	1

TAB-07

The above table shown the difference between the 16 and 20 program options with respect to the Data input commands. Commands 10, 11, 12 & 13 change function between the two options. Commands 14, 15 & 16 should not be used in the 20 program option, as they have no function.
NOP = No Operation

The Data input will accept signals whose timing is defined in fig. 6 and electrical characteristics defined in the table of static electrical characteristics. The EOT code must be transmitted after each command after a min. period of 112ms.

BAND OUTPUTS

Four band outputs are provided for selection of the signal band : VHF I & III, UHF and CATV. Band skip logic is implemented so that by tieing the relevant pin to V_{SS} a band can be skipped in regions of no transmission in that band. The bands can be selected only in a rolling sequence by the band sequence keyboard command. The sequence is as follows :

VHF III, UHF, VHF I, CATV

MULTI STANDARD OUTPUTS

Two coded multi standard outputs (or general purpose TV system flags) are provided so that the TV set can be designed for use in areas of more than one transmission standard. This function requires an external decoder to realise 4 different standards e.g. PAL 1, PAL 2, NTSC, SECAM etc. The multi standard sequence command available from the keyboard gives a simple binary count at the two outputs : 00, 01, 10, 11, 00 etc. In Standby and Off states the multistandard outputs are pulled to logic LO.

AUDIO VISUAL OUTPUTS

Two audio visual outputs are provided for automatic selection of a VCR and/or personal computer. The logic state of the pins depends on the AV option selected, the program option and the program number selected according to the truth tables below

AV Option 1		
16/20 Programs		
Program	AV0	AV1
16/0	1	0
15/19	0	1
Others	0	0

TAB-08

AV Option 2		
16/20 Programs		
Program	AV0	AV1
8/8	1	0
7/7	0	1
6/6	1	1
Others	0	0

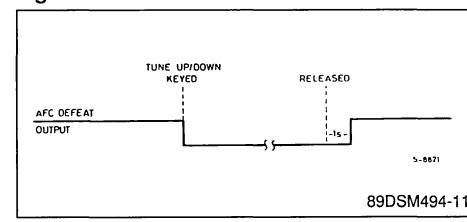
TAB-09

External pull up resistors must be used to realise a logic HI as the outputs are open drain transistors. See I/O Configuration.

AFC DEFEAT OUTPUT

The AFC defeat output is a TTL compatible signal that is capable of switching the AFC circuitry in and out. The AFC defeat output is pulled LO on any program change including memory sequence up and down and is held LO for 500ms after execution of the command. When tune up or down are commanded the AFC defeat output is taken to logic LO. After the tuning operation the AFC defeat is held LO for 1 second after the key is released. See fig. 8. On power on & start up resets it is taken to logic LO for approx. 1.1 seconds.

Figure 9 .



STANDBY

The standby output is a push pull output capable of directly driving an NPN transistor for switching a relay. The states of this pin are defined in the definition of terms. When standby is commanded, available from all command sources as Standby or On/Standby commands, the standby output is enabled.

If the device goes into Standby from On then any program command will bring the device On with that program selected. On/Off command from keyboard only will execute the Off function. On/Standby, Memory sequence up or down, 1 * and ± 10 (decade) commands from any command source will bring the device On in the program selected before Standby with the display showing that program only, i.e. the device executes an On command only.

If the device goes into Standby from Powered down then the On/Off command from keyboard only and any program command, On/Standby, Memory sequence up or down, 1 * and ± 10 (decade) commands from any command source will bring the device On in program 1. i.e. the device executes an On command only.

OPTION SELECT

The Option select pin provides an extra line that performs a "hard wired keyboard function" in conjunction with the keyboard scanning lines D0-D4. This line has integrated logic associated with it that enables one or many of the functions to be active simultaneously. In contrast, the keyboard inputs a-g will allow one key active at any given time. See keyboard section.

Various options can be selected by the connection or not of a diode as shown in figs. 7 & 8. From left to right along the Option select line column 1 selects the number of programs. A diode connected here selects 20 programs (full complement) and no diode (default) selects 16 programs only that can be accessed. The 20 program option only enables selection of 1 * or decade modes in column 4. In column 2 the AV option defines the state of the AV outputs for two protocols. These are described in section Audio visual output. Column 3 defines the state the M494 powers up in. If no connection of a diode (default) is made here the device powers up in the Off state. If a diode is present then the device powers up in the Standby state. In column 4, activated by the 20 program option only, the presence of a diode places the device in 1 * mode and the absence of a diode selects decade mode. The diode and switch in column 5 defeats the skip condition and enables program memory words to be read with the skip flag set. This allows programming (or reprogramming) of previously skipped words.

SKIP FUNCTION

Program skip is implemented in the M494 by a single memory bit associated with each program word. The bit acts as a flag to the device to indicate that the program word should be skipped and the next program word read from the memory in ascending or descending order if the skip flag is set. Programs are skipped only when accessed using the memory sequence up/down commands. Direct access to a program from the keyboard, RC or data command sources will always override the skip function. e.g. if skip is set on prog. 7 and prog. 7 is commanded from RC then prog. 7 will be tuned even if there is nc prog. stored in that memory location.

In order to program the skip bit and to defeat its function when required two commands are available : set skip flag and skip defeat. The skip defeat switch is designed to be activated by a facia panel on the TV set under which are infrequently used controls.

On the set skip flag command the M494 stores the current contents of the tuning, band and MS counters and sets the skip bit. After the set skip flag operation the contents of the tuning, band and MS counters will not change and the device continues to output these values. The operation is transparent to the user in terms of function but is indicated on the display by the program number flashing at 5Hz for 1 second. In order to reset the skip bit for any program word the desired program should be selected with skip defeated. A station should then be tuned, if required, and then the store command issued. The store command automatically resets the skip flag.

The skip defeat command enables the reading and writing (plus resetting of skip flag) of memory words whose skip flag is set. If skip is defeated the device will only access the number of programs selected by the option select i.e. If 16 programs only are selected then skip defeat will NOT enable access to all 20 programs.

RESET

There are two conditions under which the M494 is reset : power on and start up (On command). Power on reset is triggered whenever V_{DD} falls below about 3V. The duration of this reset is 110ms after V_{DD} has been restored.

POWER ON RESET (Powered down to Off or Standby states)

After the reset period of 110ms :

a) The program counter is set to program 1.

b) The outputs are disabled as defined in the Off and Standby states. See Standby & Off definitions.

c) The option selection, keyboard, momentary on switch and, when in standby, the display, RC and data inputs become active. For the "activity level" of the keyboard in Off and standby states. See Standby & Off definitions.

d) An internal register is set to indicate that the device has powered up from the powered down state.

Start up reset (Standby or Off states to On state)

A start up reset is instigated by the reception of the commands given in the definition of terms or the Standby section. The following then occurs :

a) The internal register indicating that the device has powered up from the powered down state is read:

I) If the register is set than the memory word addres sed by the program counter is loaded into the tu ning counter and then the analog values are read rom the memory.

II) If the register is reset then the previously selec ted tuning and analog values are left unchanged.

b) The AFC is defeated and the volume muted for a period of approx 1.7 seconds or 0.6 seconds lon ger than the other analog outputs.

c) The tuning and analogue outputs, except volume, are enabled after approx. 1.1 seconds.

d) The volume output is enabled after 1.7 seconds

e) The standby output is pulled up internally to logic HI

f) The internal register is reset.

If the device has either of the power up options (power up in Off or standby states) selected then it will perform a power up reset but all the outputs and command sources will remain disabled, then on the On command, a start up reset will be performed. If the device is required to power up in the On state using the momentary mechanical switch connected to the h+i pin then it will perform an ordinary power on reset followed immediately by a start up reset. The outputs and command sources will be enabled after the periods defined above.

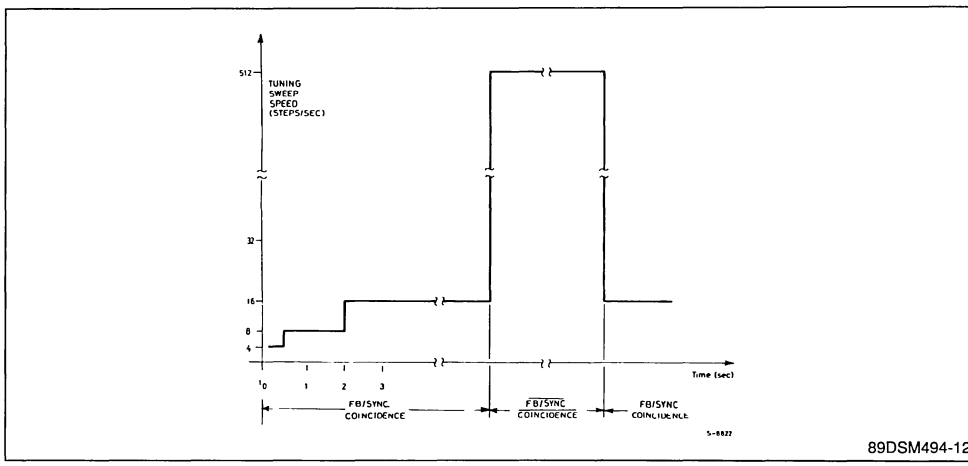
MANUAL TUNING

Manual tuning commands tune up or down, are available from keyboard only and are provided to allow both manual station search and tuning adjustments. If a continuous tuning up or down command is made from the keyboard the speed of movement of the tuning counter is as shown in fig. 10 for the UHF and CATV bands. Time t_o is the start time for the key being pressed. When the FB/sync. coincidence input is a logic HI the tuning speed is reduced to 16 steps/sec. If, at time t_o the FB/sync. coincidence input is at logic LO than the tuning.sweep speed jumps immediately to 512 steps/sec.

For VHF III & I all these levels are shifted up by a factor of 2 & 4 respectively giving slowest speeds of 8 steps/sec. and 16 steps/sec. and highest speeds of 1024 steps/sec and 2048 steps/sec. If the continuity of command is broken by releasing the keyboard for example then the tuning speed returns to its slowest speed when the FB/sync. coincidence input is at logic HI. If the upper or lower limit of a band is reached during manual tuning then tuning will continue in the same direction from the opposite limit after a 480ms delay to allow for the discharge of the external network.

The tuning counter is 13 bits in length giving a range of 8192 steps. The UHF band has a bandwidth of approx. 400MHz. Thus in the UHF band the slowest speed of 4 steps/sec. gives a tuning speed of about 200KHz/sec. The fastest speed of 512 step/sec. corresponds to a total band sweep time of 16 seconds.

Figure 10 : Tuning Sweep Speed (UHF & CATV BANDS).



PROGRAM MEMORY SEQUENCE

A continuous up/down program memory command from keyboard produces a program change every 500ms. From remote control and data command sources a continuous program memory sequence command produces a program change approx. every 500ms or every 5 received commands. A memory sequence up or down command issued from any source will bring the device out of standby to the program selected before standby was commanded. The memory sequence up or down will not then commence until the command is stopped and reissued from any source (until an EOT has been received or internally generated).

MUTE

The sound mute function is available as a toggle command from all command sources. There are other commands and functions during which the sound is muted :

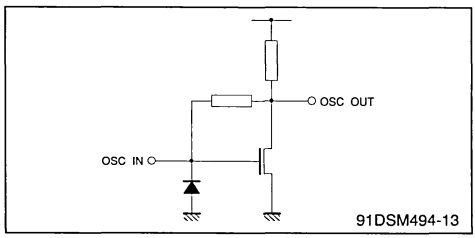
- FB/sync. coincidence - If there is no FB/sync. coincidence under any conditions the sound is muted.
- Start up reset - the sound is muted for approx. 1.7 seconds.
- Program change - the sound is muted for 0.6 seconds on any program change ; direct, 1 * + 0-9 program (only after the second keystroke), ±10 (decade) & Memory sequence up/down continuous or single keystrokes.
- Standby & Off states - the sound is muted.
- Band sequence - same as program change.
- The sound is demuted under the following conditions :
- When the mute command is received from any source.
- When the device is commanded On from standby of Off, i.e. if the device was muted when the standby command was issued then when On is commanded it will always start up with the sound demuted after the reset and settling period of approx. 17 seconds.
- Volume up - if volume up is commanded whilst the sound is muted then the volume will increase from zero.
- Volume down - if volume down is commanded whilst the sound is muted then there is no effect.
- Any program change - the sound is NOT demuted.

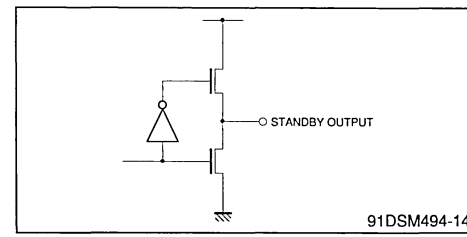
MOMENTARY ON SWITCH

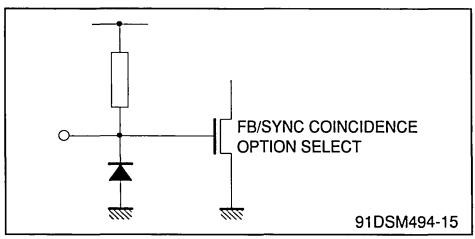
Provision is made for a momentary switch connected between the h+i pin and ground to force the M494 to make Power on and Start up resets automatically so that the device attains the On state immediately.

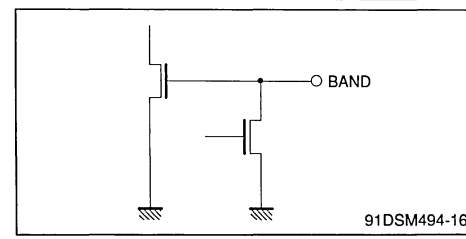
The condition of the h+i pin is latched after the reset period of 110ms. Therefore the period of switch contact closure should be a min. of 120ms.

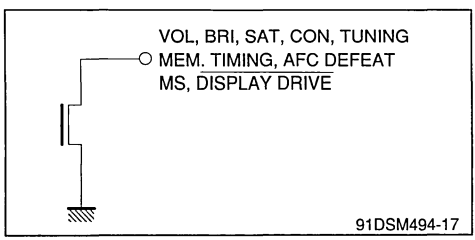
INPUT/OUTPUT PINS

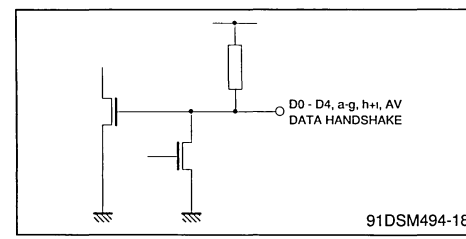












COMMANDS

Command	Source	Function
Programs 1-12	KB, D,RC (16 opt.)	Reads the contents of the memory location : 2MSB's to the MS counter, next 2 MSB's to the band counter next 12 MSB's to the tuning counter and D/A and LSB to skip flag register. Initiates an on command only after standby.
Programs 0-9	KB, D, RC (20 opt.)	Reads the contents of the memory location : 2MSB's to the MS counter, next 2 MSB's to the band counter next 12 MSB's to the tuning counter and D/A and LSB to skip flag register. Initiates an on command only after standby.
Programs 13-16	D, RC (16 opt.)	Reads the contents of the memory location : 2 MSB's to the MS counter, next 2 MSB's to the band counter next 12 MSB's to the tuning counter and D/A and LSB to skip flag register. Initiates an on command only after standby.
– 10 (decade)	KB, D, RC (20 opt.)	Sustracts 10 from the current program (if possible). Initiates an on command only after standby.
+ 10 (decade)	KB, D, RC (20 opt.)	Adds 10 to the current program (if possible). Initiates an on command only after standby.
1*	KB, D, RC (20 opt.)	Commands the M494 to wait for a 0-9 program command or to reset on any other command. Display shows static half digit and g segment flashing at 5Hz. Initiates an on command only after standby.
Vol. up/down Bri. up/down Sat. up/down Con. up/down	KB, D, RC	Increments up or down the relevant analog control counter every keystroke or continuously every 112ms from KB and every 102ms from the RC and data inputs. The display shows an up/down arrow for 300ms min.
Tune up/down	KB	Increments up or down the tuning counter. The speed or increment/decrement is defined by Fig. 10. The display shows an up/down arrow for 300ms min.
Mem. up/down	KB, D, RC	The program number (memory location) is incremented/decremented.
Mute (toggle)	KB, D, RC	Volume Mute. See mute section.
Standby	D, RC	Commands the standby state.
On/standby (toggle)	KB, D, RC	Commands the standby state from the on state and the on state from the standby state.
ON/OFF	KB	Commands the on state when in the off state and commands the off state when in the on state. See standby section.
Store Program	KB	The currently addressed memory location is written from the tuning, band and MS counters and the skip flag is reset. See fig. 11. Execution of this command is indicated by the display flashing at 5Hz for 1 second.
Store analog Controls	KB	The analog control memories are written in sequence from the analog control counters. Execution of this command is indicated by the display flashing at 5Hz for 1 second.
Band Sequence	KB	Command the next band in the sequence as defined in bands outputs section. One step for each key stroke.
MS Sequence	KB	Increments the MS counter by binary one. One step for each key stroke.
Normalise Analog	KB, D, RC	Reads the analog memories in sequence to their corresponding D/A's. The analog control outputs are disabled during the read sequence.
Memory addressing	KB	Strokes the program selected immediately after the memory addressing command (post tuning program selection). See fig. 12.
Set Skip Flag	KB	Sets the skip flag on the currently selected program. Execution of this command is indicated by the display flashing at 5Hz for 1 second.
Skip Defeat	OS	Defeats the function of the skip bit to allow reading and writing of the currently selected program.

TAB-10

KB = Keyboard; D = Data; RC = Remove Control; OS = Option Select.

Figs. 11 & 12 respectively show in flow diagram form the two methods for storing a station : pretuning program selection and post tuning program selection. Figs. 13, 14 & 15 show the select programme subroutine for figs. 11 & 12 for either 16 program option or 20 program option with 1 * or ±10 (decade modes).

Figure 11 : Normal Methods for Storing a Station (preselection of program number).

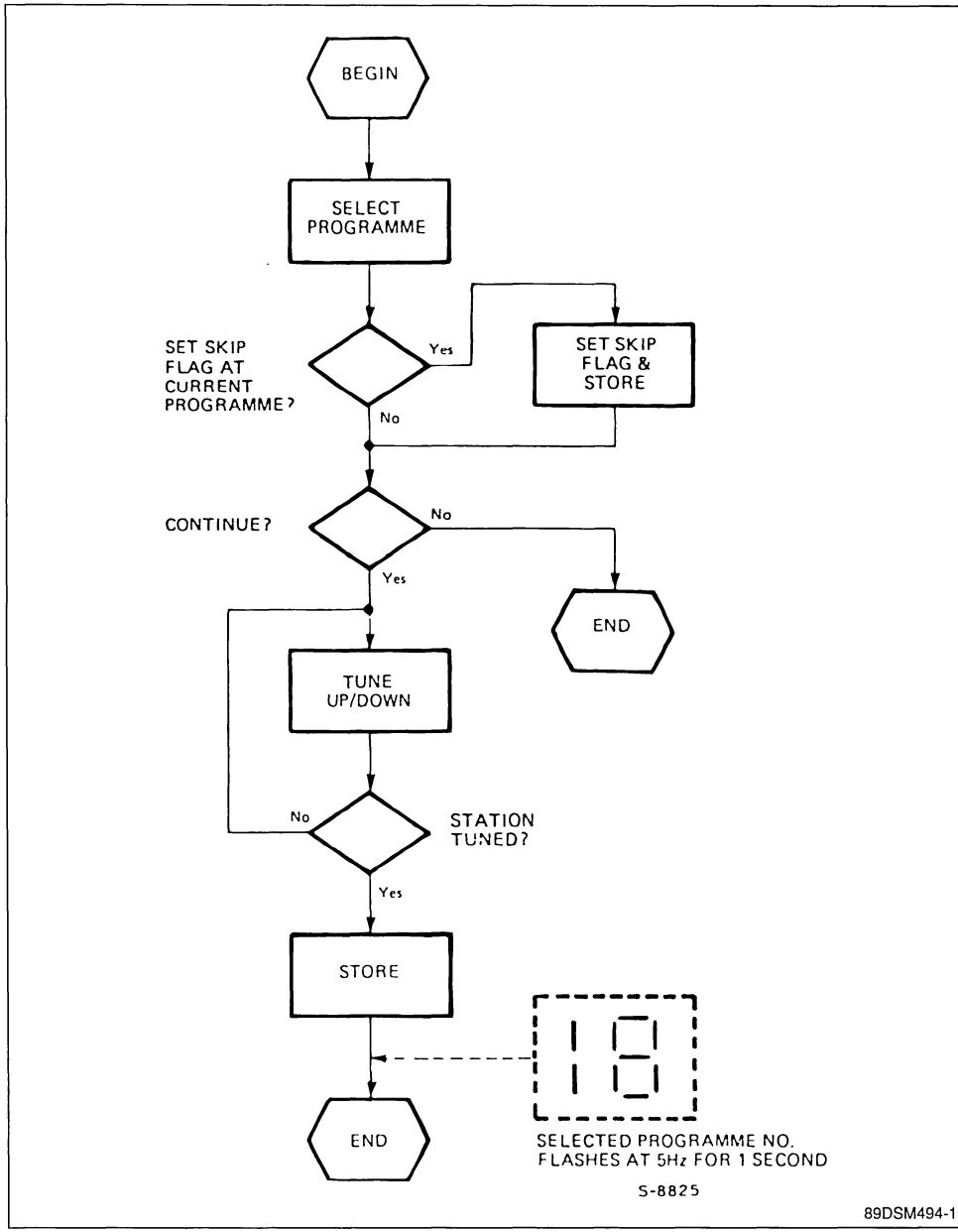


Figure 12 : Secondary Method for Storing a Station (postselection of program number).

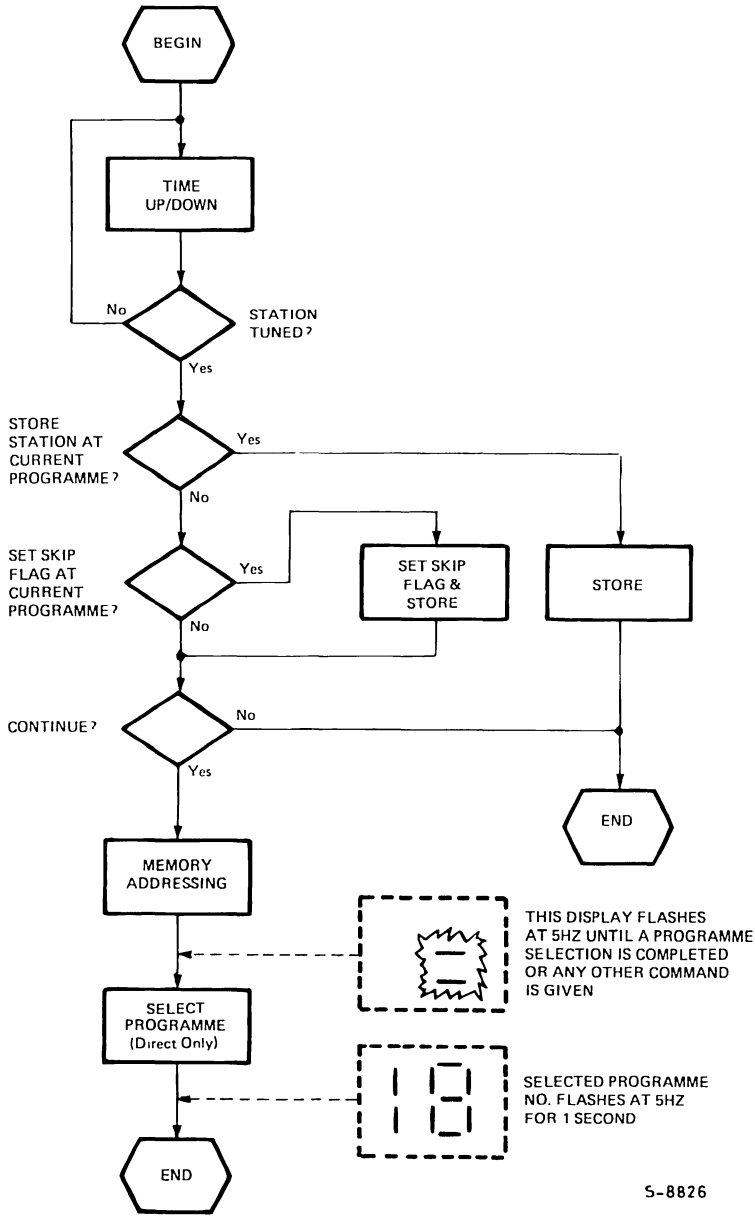


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Figure 13 : Program Selection Routine (16 program).

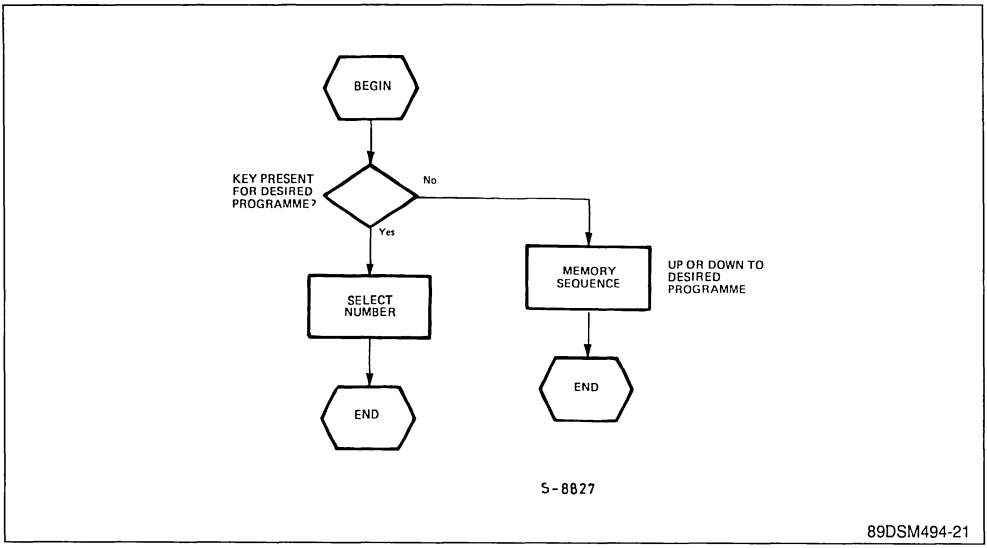


Figure 14 : Program Selection Routine (20 program, 1 * mode).

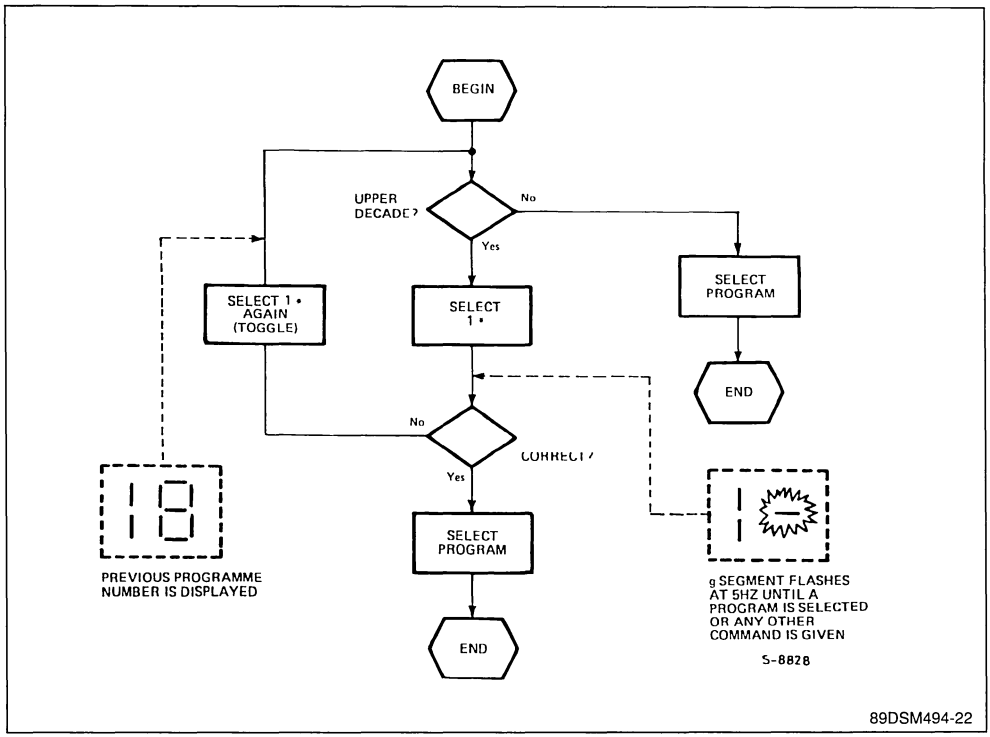
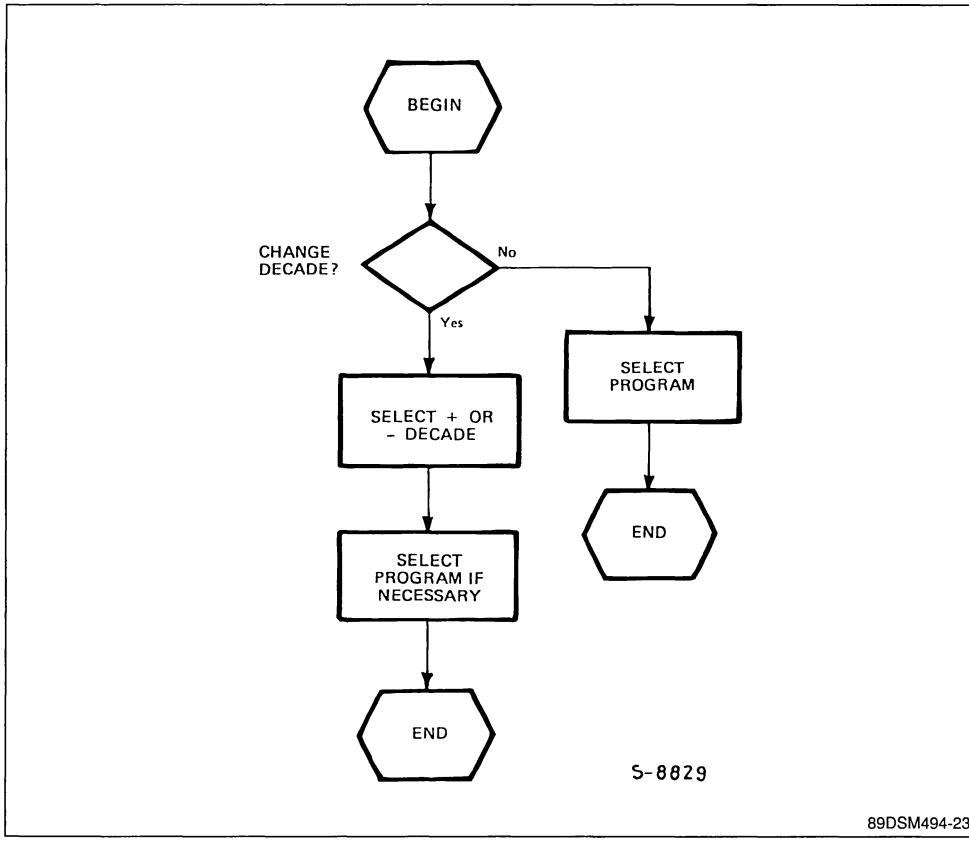
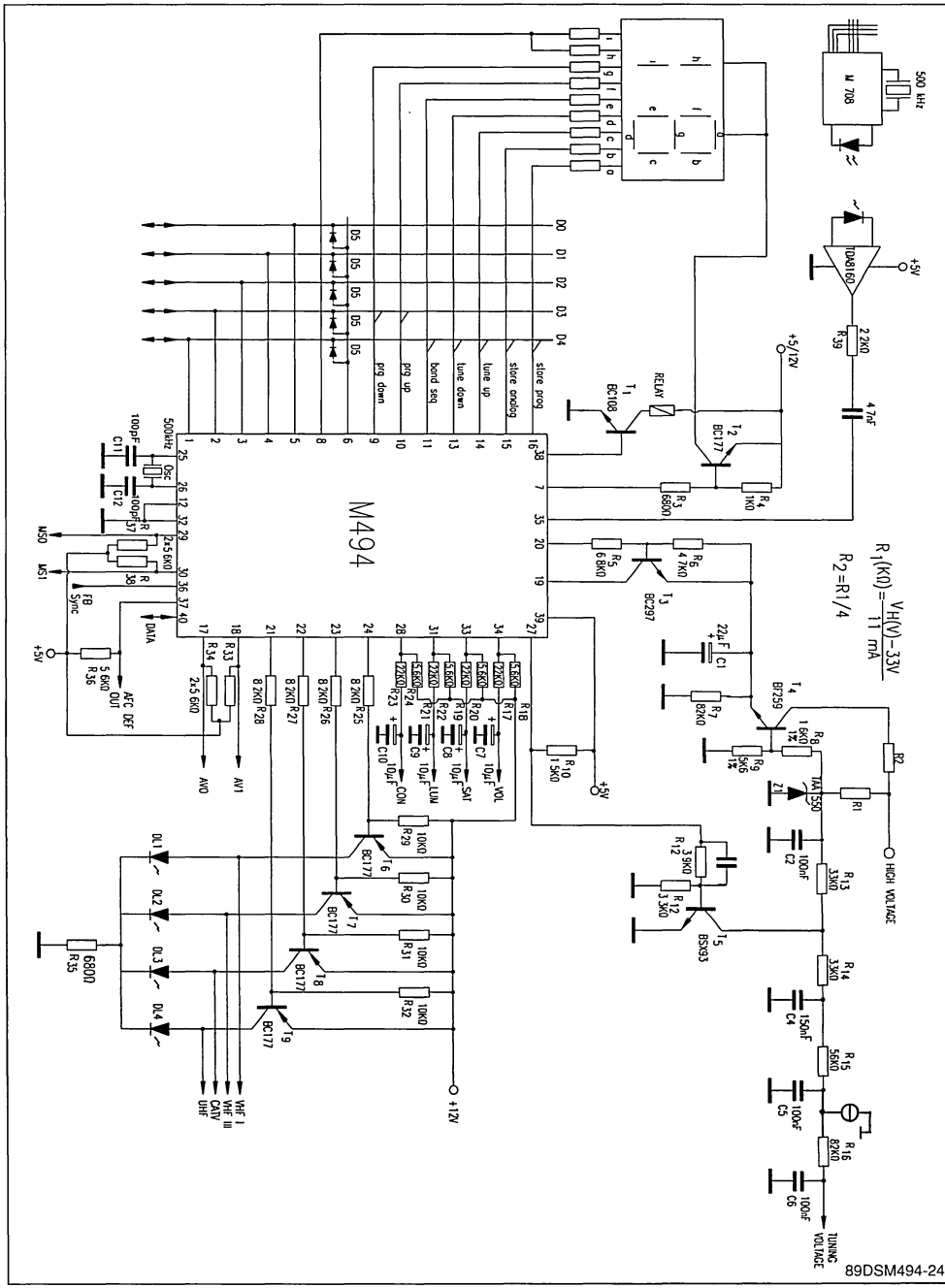


Figure 15 : Program Selection Routine (20 program, decade mode).

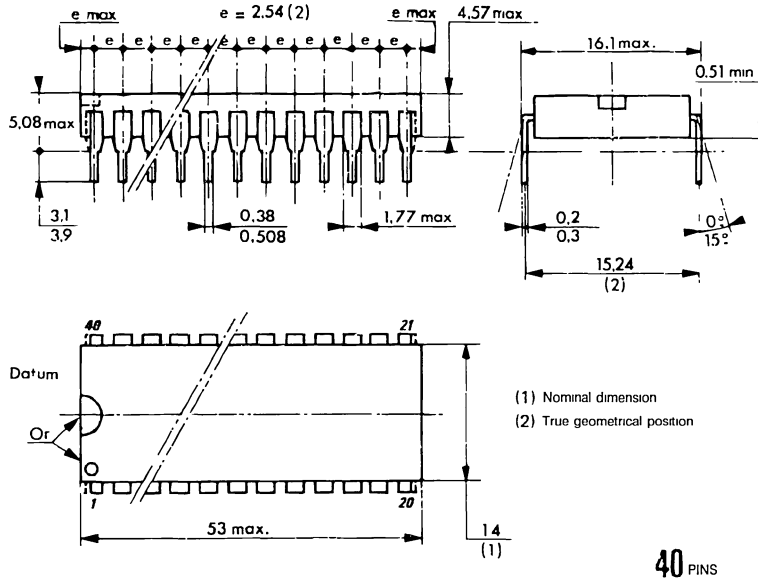


TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

40 PINS - PLASTIC PACKAGE



PCM REMOTE CONTROL TRANSMITTER

- 30 CHANNELS/4 ADDRESSES
- SELECTABLE FLASH/CARRIER TRANSMISSION MODE
- END OF TRANSMISSION CODE
- VERY LOW POWER DISSIPATION DURING TRANSMISSION : DUTY CYCLE 0.15 % (flash mode), 0.7 % (carrier mode)
- SINGLE CONTACT MATRIX KEYBOARD
- INTEGRATED ANTIBOUNCE AND INTERLOCK
- WIDE SUPPLY RANGE (M708 4.5 to 10.5 V)/(M708A 3 to 10.5 V)
- WIDE REFERENCE FREQUENCY RANGE (445 to 510 kHz ceramic resonator)
- 20 PIN PLASTIC PACKAGE
- TO BE USED IN CONJUNCTION WITH M491/M494 SINGLE CHIP STATION MEMORY AND R.C. RECEIVER (flash mode) OR WITH MICROPROCESSOR CONTROLLED SYSTEM (carrier mode)

DESCRIPTION

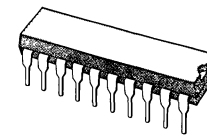
This IC has been developed for remote control in consumer applications. It uses a highly reliable transmission code which has the capacity of 1024 channels. Each transmitted word is structured into 4 bits which constitute the address and 6 bits which constitute the command. However only 2 address bits and 30 commands are available in this IC. An additional command (000000) is used to transmit the "end of transmission code" when the key is released.

Additional bits are transmitted for synchronization of transmitter and receiver clocks and for security checks. The address organization provides simultaneous applications without interference among each system.

The receiver accepts the decoded command only if the transmitted address matches the address selected at the receiver. Four addresses are available for this purpose. The reference oscillator is controlled by a cheap ceramic resonator.

When the M708 works in conjunction with M491/M494 single chip Station Memory and R.C. receiver the oscillator frequency can be in the range 445 to 510 kHz and no synchronization is required with the receiver clock.

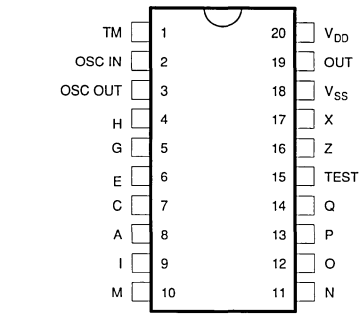
The M708 is produced with CMOS Si-gate technology and is available in a 20 pin dual in-line plastic package.



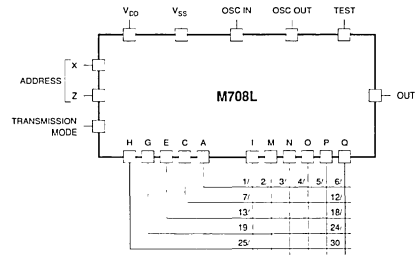
DIP20
(Plastic Package)

ORDER CODES : M708 B1
M708A B1

PIN CONNECTIONS



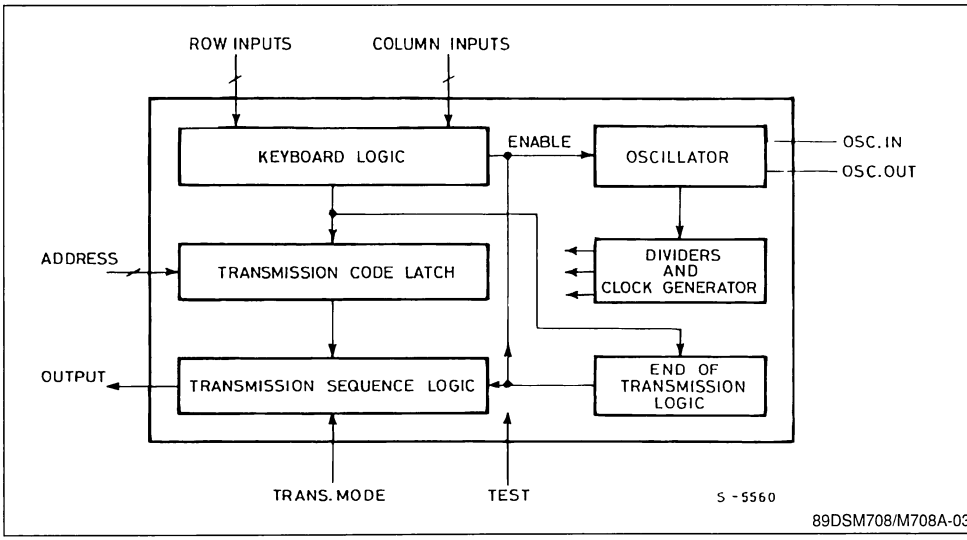
91DSM708/M708A-01



91DSM708/M708A-02

Note : The test pin must be connected to V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 12	V
V_I	Input Voltage	– 0 3 to V_{DD} + 0.3	V
$\|I_{OY}$	IR Output Current (t < 50 µs)	10	mA
T_{op}	Operating Temperature	0 to 70	°C
P_{tot}	Total Package Power Dissipation	200	mW
T_{stg}	Storage Temperature	– 55 to 125	°C

TAB-01

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : M708 M708A	4.5 to 10.5 3 to 10.5	V V
V_I	Input Voltage	0 to V_{DD}	
$\|I_O\|$	IR Output Current (t < 50 µs)	max. 2.5	mA
f_{ref}	Reference Frequency	445 to 510	kHz
T_{op}	Operating Temperature	0 to 70	°C
r_s	Serial Resistance of a Closed Key Contact	max. 2.5	KΩ
r_p	Parallel Resistance of Open Key Contact	min. 2.2	MΩ
R_s	Serial Resistance of the Ceramic Resonator	max. 20	Ω

TAB-02

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)
Typical values are at 9V and T_{amb} = 25 °C

Symbol	Parameter	Pins	Test Conditions		Min.	Typ.	Max.	Unit
I_{DD}	Supply Voltage		V_{DD} = 9 V IR Output Open	Stand–by		5	15	µA
				Operating (one key closed)		4	7	mA
I_{OH}	H State IR Output Current		V_{DD} = 9 V	V_{OH} = 8 V	– 1.5	– 2.5		mA
			V_{DD} = 4.5 V	V_{OH} = 3.5 V	– 0.3	– 0.5		
I_{OL}	L State IR Output Current		V_{DD} = 9 V	V_{OL} = 1 V	1.5	– 2.5		mA
			V_{DD} = 4.5 V	V_{OL} = 1 V	0.3	0.5		
V_{TH}	Input Threshold High	Selection Inputs A to H	V_{DD} = 9 V				6	V
			V_{DD} = 4.5 V				3	
V_{TL}	Input Threshold Low	Selection Inputs K to Q	V_{DD} = 9 V		3			V
			V_{DD} = 4.5 V		1.5			
I_{IL}	Input Low Current	Pull–up Inputs A to H	V_{DD} = 9 V V_{IL} = 4.5 V		– 60		– 300	µA
I_{IH}	Input High Current	Pull–down Inputs K to Q	V_{DD} = 9 V V_{IH} = 4.5 V		60		300	µA
I_{IH}	Input High Current	Address Selection Inputs	V_{DD} = 9 V V_{IL} = 8.25 V (oscillator running)				150	µA
I_L	Input Leakage Current	Trans. Mode Test Pin	V_{DD} = 9 V V_{IN} = 0 to 9 V				1	µA
I_{OS}	Output Current	Osc. Out.	V_{DD} = 9 V Osc. In. = V_{SS}		– 2		– 8	µA

TAB-03

TRUTH TABLE

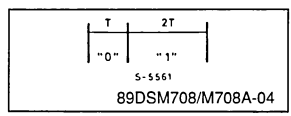
Command N°	Input Code											Command Bits					
	A	C	E	G	H	I	M	N	O	P	Q	C1	C2	C3	C4	C5	C6
0	END OF TRANSMISSION											0	0	0	0	0	0
1	X					X						1	0	0	0	0	0
2	X						X					1	1	0	0	0	0
3	X							X				0	0	1	0	0	0
4	X								X			1	0	1	0	0	0
5	X									X		0	1	1	0	0	0
6	X										X	1	1	1	0	0	0
7		X				X						1	0	0	0	1	0
8		X					X					1	1	0	0	1	0
9		X						X				0	0	1	0	1	0
10		X							X			1	0	1	0	1	0
11		X								X		0	1	1	0	1	0
12		X									X	1	1	1	0	1	0
13			X			X						1	0	0	0	0	1
14			X				X					1	1	0	0	0	1
15			X					X				0	0	1	0	0	1
16			X						X			1	0	1	0	0	1
17			X							X		0	1	1	0	0	1
18			X								X	1	1	1	0	0	1
19				X		X						1	0	0	0	1	1
20				X			X					1	1	0	0	1	1
21				X				X				0	0	1	0	1	1
22				X					X			1	0	1	0	1	1
23				X						X		0	1	1	0	1	1
24				X							X	1	1	1	0	1	1
25					X	X						1	0	0	1	1	1
26					X		X					1	1	0	1	1	1
27					X			X				0	0	1	1	1	1
28					X				X			1	0	1	1	1	1
29					X					X		0	1	1	1	1	1
30					X						X	1	1	1	1	1	1

TAB-04

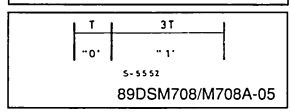
DESCRIPTION

The signals are transmitted with infrared light using a Pulse Code Modulation. Each word consists of 12 bits. The binary information of a bit is determined by the time interval between two pulses. If "T" is the time base, the bits are coded as follows :

Odd bits (1, 3, etc)
0 = T
1 = 2T

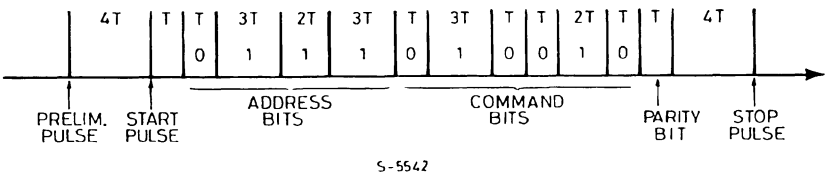


Even bits (2, 4, etc.)
0 = T
1 = 3T



The different code introduced for the even and odd "1s" improves the capability to recognize false codes at the receiver end. For example the double error which can cause the exchange "10" with "01" is easily detected. A Parity bit is also added in order to further increase the reliability of the transmission. This bit is "1" if the number of transmitted "1" is even while it is "0" if the number of transmitted "1" is odd. In addition, every word contains a preliminary pulse, a start pulse and a stop pulse. The spacing between the preliminary and the start pulse is 4T. This is followed after 1T by 11 data pulses (one parity bit), and terminated after a 4T interval by a stop pulse. Consequently, a word in which the binary digit 0 occurs ten times has a total duration of 21T. A word containing ten "1s" has a duration of 36T.

Example :



89DSM708/M708A-06

SYNCHRONIZATION BETWEEN TRANSMITTER AND RECEIVER

The transmitter and the receiver can operate with different reference frequencies. Typical values suitable for correct operation of the system should be comprised between 445 and 510 kHz, using a cheap ceramic resonator.

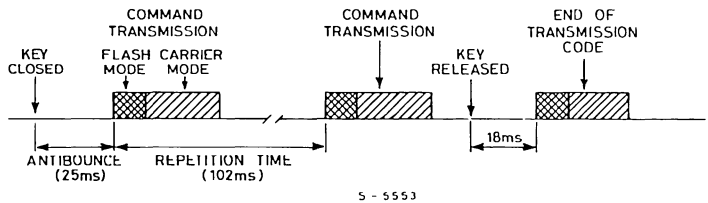
Synchronization between the transmitter and the receiver, necessary to obtain the above described wide range of frequency tolerance is achieved by measuring in the receiver the interval between the start pulse and the first data pulse, storing this value and using it as time base T.

KEYBOARD/CODE REPETITION

One column, input (pins IMNOPQ) has to be connected to one row (pins ACEGH) input to activate the transmitter. The contact must be continuously closed for a minimum of 25 ms.

Double and multiple contact operations are not accepted. The command information is repeatedly transmitted at intervals of 102 ms (f_{ref} = 500 kHz) as long as the push button remains operated. When the contact is interrupted the circuit transmits, after a pause of 18 ms, the "end of transmission code" and returns to stand-by mode. If the contact is interrupted while a command is being transmitted the circuit carries on with the transmission to the end. After a pause of about 18 ms it transmits the end of transmission code.

No command is accepted until the "end of transmission code" is over.

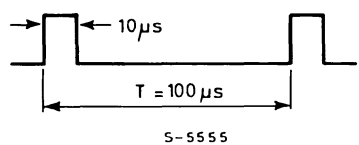


89DSM708/M708A-07

TRANSMISSION MODE (pin T)

The M708 can operate in Flash (pin T = V_{DD}) or Carrier (pin T = V_{SS}) transmission modes. Using a referance frequency of 500 kHz the output signal has these formats respectively :

Flash Mode



Transmission time

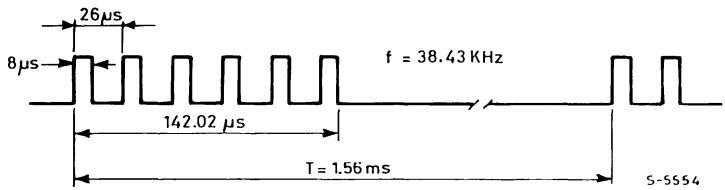
min. = 2.1 ms

max. = 3.6 ms

duty cycle = 0.15 %

89DSM708/M708A-08

Carrier Mode

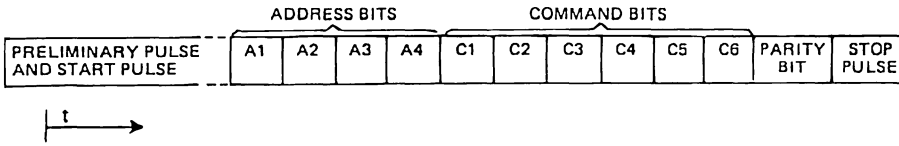


Transmission time
min. = 32.76 ms
max = 56.16 ms
duty cycle = 0.7 %

89DSM708/M708A-09

ADDRESS (pins X, Z)

The address information is coded and transmitted as follows.

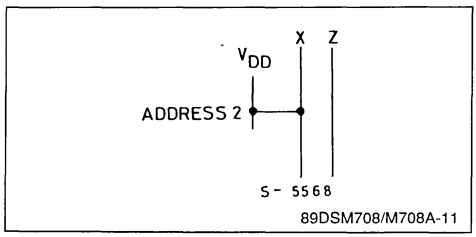


89DSM708/M708A-10

Address Number	Transmitted Code				Address Input Code	
	A1	A2	A3	A4	X	Z
1	0	0	0	0	L	L
2	1	0	0	0	H	L
9	0	0	0	1	L	H
10	1	0	0	1	H	H

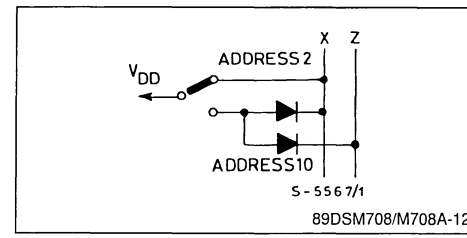
The Address inputs have internal pull-downs which are disabled during stand-by.

Single address selection



89DSM708/M708A-11

Multiple address selection

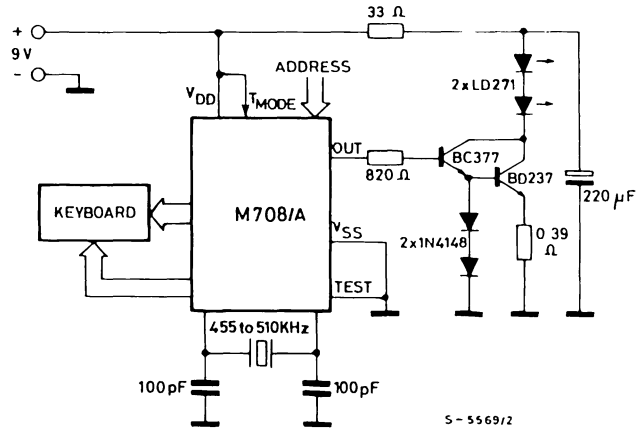


89DSM708/M708A-12

Note : Unused inputs can be left open or connected to V_{SS}

TYPICAL APPLICATIONS

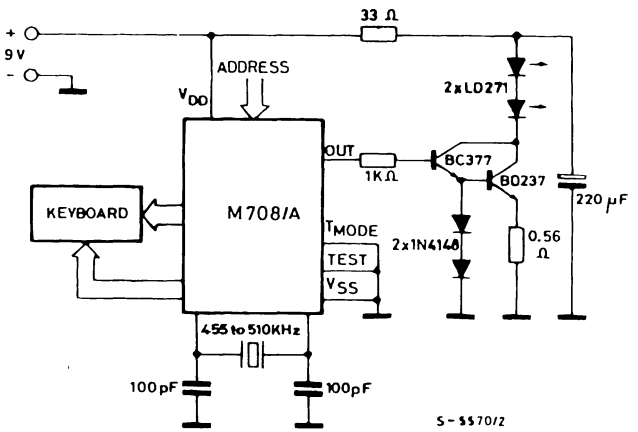
FLASH MODE



Infrared Diode Peak Current = 1.8 A
Total Average Consumption = 6.5 mA

89DSM708/M708A-13

CARRIER MODE

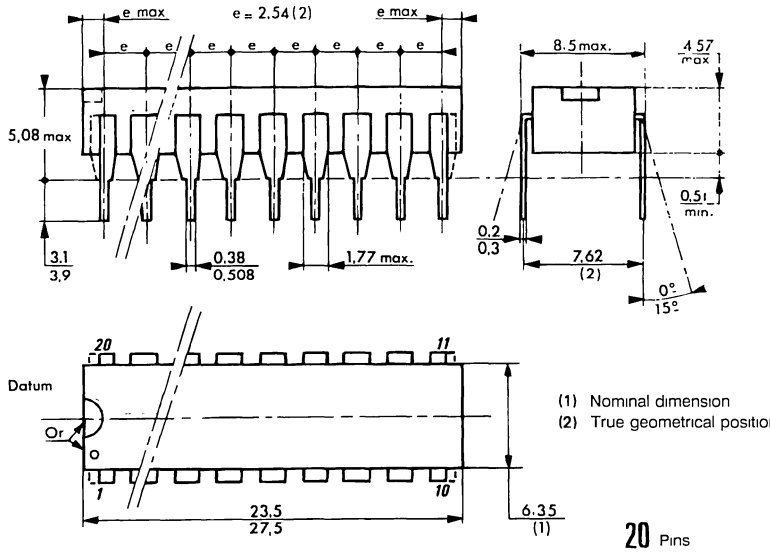


Infrared Diode Peak Current = 1.25 A
Total Average Consumption = 13 mA

89DSM708/M708A-14

PACKAGE MECHANICAL DATA

20 PINS - PLASTIC DIP



PCM REMOTE CONTROL TRANSMITTER (LOW VOLTAGE)

- 2.2 TO 5 V OPERATING SYPPLY VOLTAGE RANGE
- 30 CHANNELS/4 ADDRESSES
- SELECTABLE FLASH/CARRIER TRANSMISSION MODE
- END OF TRANSMISSIONE CODE
- VERY LOW POWER DISSIPATION DURING TRANSMISSION. DUTY CYCLE : 0.15 % (flash mode), 0.7 % (carrier mode)
- SINGLE CONTACT MATRIX KEYBOARD
- INTEGRATED ANTIBOUNCE AND INTERLOCK
- WIDE REFERENCE FREQUENCY RANGE (455 to 510 KHz ceramic or LC resonator)
- 20 PIN PLASTIC PACKAGE
- TO BE USED IN CONJUNCTION WITH M491/M494 SINGLE CHIP STATION MEMORY AND R.C. RECEIVER (flash mode)

DESCRIPTION

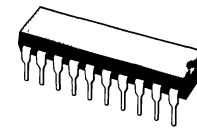
This IC has been developed for remote control in consumer applications. It uses a highly reliable transmission code wich has the capacity of 1024 channels. Each transmitted word is structured into 4 bits which constitute the address and 6 bits which constitute the command. However only 2 bits of addresses and 30 commands are available in this IC. An additional command (000000) is used to transmit the "end of transmission code" when the key is released.

Additional bits are transmitted for synchronization of transmitter and receiver clock and for security checks. The address organization provides simultaneous applications without interference among each system.

The receiver accepts the decoded command only if the transmitted address matches the address selected at the receiver. Two address are available for this purpose. The reference oscillator is controlled by a cheap ceramic resonator.

When the M708L works in conjunction with M491/M494 single chip Station Memory and R.C. receiver the oscillator frequency can be in the range 445 to 510 KHz and no synchronization is required with the receiver clock.

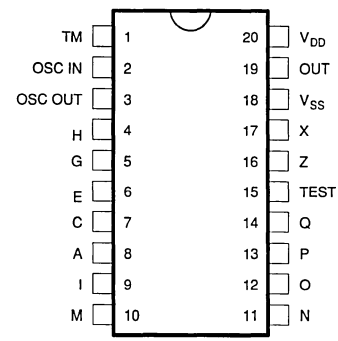
The M708L is produced with CMOS Si-gate technology and is available in a 20 pin dual in-line plastic package.



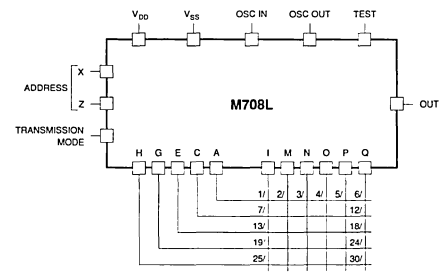
DIP20
(Plastic Package)

ORDER CODE : M708LB1

PIN CONNECTIONS (top view)



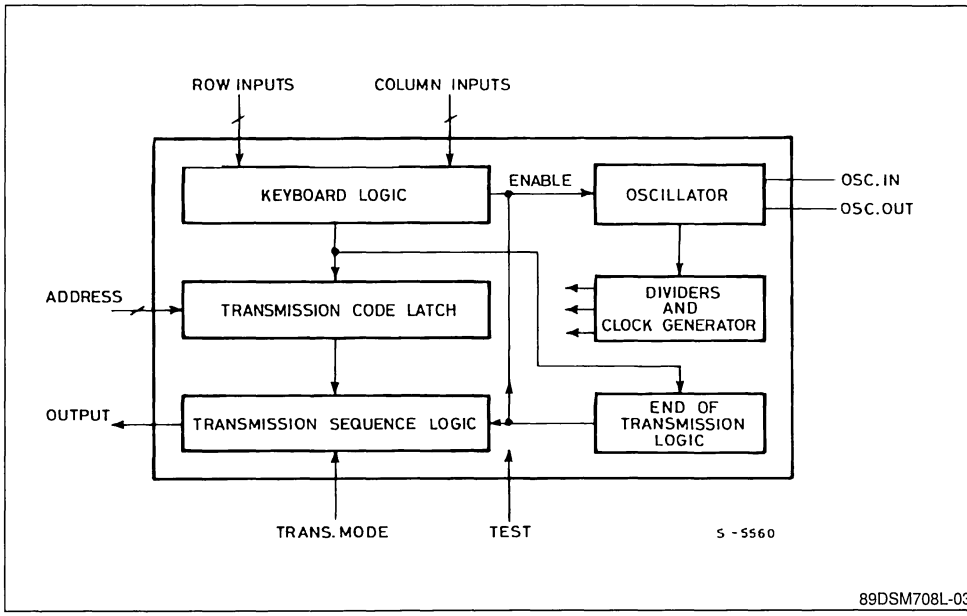
91DSM708L-01



91DSM708L-02

Note : The test pin must be connected to V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 5.5	V
V_I	Input Voltage	– 0.3 to V_{DD} + 0.3	V
$\|I_O\|$	IR Output Current (t < 50 µs)	10	mA
T_{op}	Operating Temperature	0 to 70	°C
P_{tot}	Total Package Power Dissipation	200	mW
T_{stg}	Storage Temperature	– 55 to 125	°C

TAB-01

Stresses above those listed under " Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	2.2 to 5	V
V_I	Input Voltage	0 to V_{DD}	
$\|I_O\|$	IR Output Current (t < 50 µs)	max 2.5	mA
f_{ref}	Reference Frequency	445 to 510	kHz
T_{op}	Operating Temperature	0 to 70	°C
r_s	Serial Resistance of a Closed Key Contact	max 2.5	kΩ
r_p	Parallel Resistance of Open Key Contact	min 2.2	MΩ
R_s	Serial Resistance of the Ceramic Resonator	max 20	Ω

TAB-02

TRUTH TABLE

Command N°	Input Code											Command Bits					
	A	C	E	G	H	I	M	N	O	P	Q	C1	C2	C3	C4	C5	C6
0	End of Transmission											0	0	0	0	0	0
1	X					X						1	0	0	0	0	0
2	X						X					1	1	0	0	0	0
3	X							X				0	0	1	0	0	0
4	X								X			1	0	1	0	0	0
5	X									X		0	1	1	0	0	0
6	X										X	1	1	1	0	0	0
7		X				X						1	0	0	0	1	0
8		X					X					1	1	0	0	1	0
9		X						X				0	0	1	0	1	0
10		X							X			1	0	1	0	1	0
11		X								X		0	1	1	0	1	0
12		X									X	1	1	1	0	1	0
13			X			X						1	0	0	0	0	1
14			X				X					1	1	0	0	0	1
15			X					X				0	0	1	0	0	1
16			X						X			1	0	1	0	0	1
17			X							X		0	1	1	0	0	1
18			X								X	1	1	1	0	0	1
19				X		X						1	0	0	0	1	1
20				X			X					1	1	0	0	1	1
21				X				X				0	0	1	0	1	1
22				X					X			1	0	1	0	1	1
23				X						X		0	1	1	0	1	1
24				X							X	1	1	1	0	1	1
25					X	X						1	0	0	1	1	1
26					X		X					1	1	0	1	1	1
27					X			X				0	0	1	1	1	1
28					X				X			1	0	1	1	1	1
29					X					X		0	1	1	1	1	1
30					X						X	1	1	1	1	1	1

TAB-03

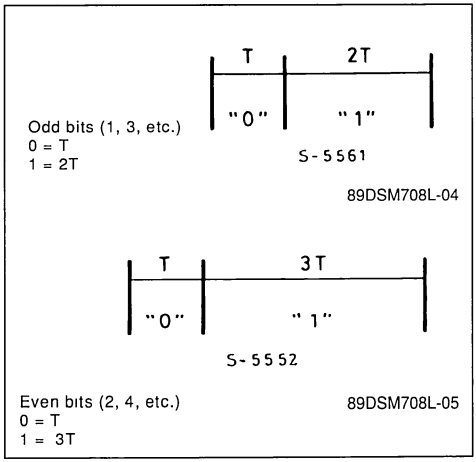
STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter	Pins	Test Conditions		Value			Unit
					Min.	Typ.	Max.	
I_{DD}	Supply Voltage		V_{DD} = 5 V IR Output Open	Stand-by		3	10	µA
				Operating (one key closed)		4	7	mA
I_{OH}	H State IR Output Current		V_{DD} = 3 V	V_{OH} = 2 V	− 1	− 2		mA
			V_{DD} = 2.2 V	V_{OH} = 1 V	− 0.3	− 0.5		
I_{OL}	L State IR Output Current		V_{DD} = 3 V	V_{OL} = 1 V	1	2		mA
			V_{DD} = 2.2 V	V_{OL} = 1 V	0.3	0.5		
I_{IH}	Input High Current	Address Selection Inputs	V_{DD} = 3 V V_{IL} = 3 V (oscillator running)				150	µA
I_L	Input Leakage Current	Trans. Mode Test Pin	V_{DD} = 3 V V_{IN} = 0 to 3 V				1	µA

TAB-04

DESCRIPTION

The signals are transmitted with infrared light using a Pulse Code Modulation. Each word consists of 12 bits. The binary information of a bit is determined by the time interval between two pulses. If "T" is the time base, the bits are coded as follows :



The different code introduced for the even and odd "1s" improves the capability to recognize false codes at the receiver end. For example the double error which can cause the exchange "10" with "01" is easily detected. A Parity bit is also added in order to further increase the reliability of the transmission. This bit is "1" if the number of transmitted "1" is even while it is "0" if the number of transmitted "1" is odd. In addition, every word contains a preliminary pulse, a start pulse and a stop pulse. The spacing between the preliminary and the start pulse is 4T. This is followed after 1T by 11 data pulses (one parity bit), and terminated after a 4T interval by a stop pulse. Consequently, a word in which the ninary digit 0 occurs ten times has a total duration of 21T. A word containing ten "1s" has a duration of 36T.(see Example)

SYNCHRONIZATION BETWEEN TRANSMITTER AND RECEIVER.

The transmitter and the receiver can operate with different reference frequencies. Typical values suitable for correct operation of the system should be comprised between 445 and 510 KHz, using a cheap ceramic resonator.

Synchronization between the transmitter and the receiver necessary to obtain the above described wide range of frequency tolerance is achieved by measuring in the receiver the interval between the start pulse and the first data pulse, storing this value and using it as time base T.

KEYBOARD/CODE RECEPTION.

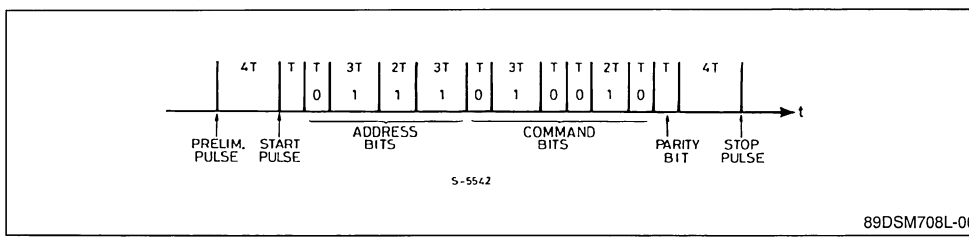
One column input (pins IMNOPQ) has to be connected to one row (pins ACEGH) input to activate the transmitter. The contact must be continuously closed for a minimum of 25 ms.

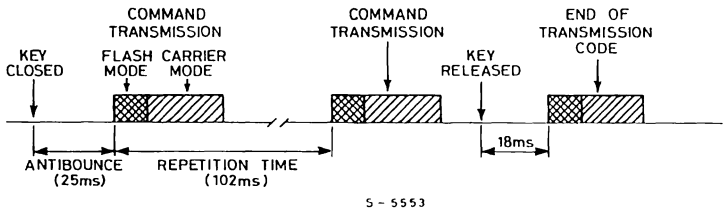
Double and multiple contact operations are not accepted. The command information is repatedly transmitted at intervals of 102 ms (f_{ref} = 500 KHz) as long as the push button remains operated.

When the contact is interrupted the circuit transmits, after a pause of 18 ms, the "end of transmission code" and returns to stand-by mode. If the contact is interrupted while a command is being transmitted the circuit carries on with the transmission to the end. After a pause of about 18 ms it transmits the end of transmission code.

No command is accepted until the "end of transmission code" is over.

Example



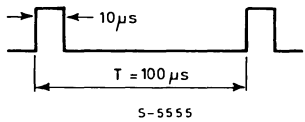


89DSM708L-07

TRANSMISSION MODE (Pin T).

The M708 can operate in Flash (pin T = V_{DD}) or Carrier (pin T = V_{SS}) transmission modes. Using a reference frequency of 500 KHz the output signal has these formats respectively :

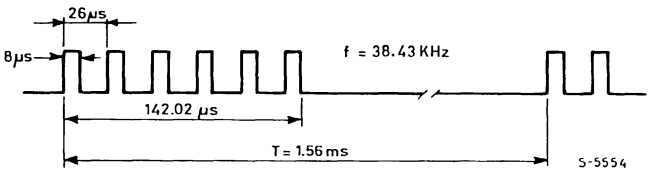
Flash mode



Transmission time
min. = 2.1 ms
max = 3.6 ms
duty cycle = 0.15%

89DSM708L-08

Carrier mode

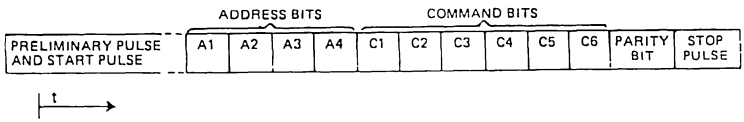


Transmission time
min = 32.76 ms
max. = 56 16 ms
duty cycle = 0.7%

89DSM708L-09

ADDRESS (Pin X, Z).

The address information is coded and transmitted as follows :



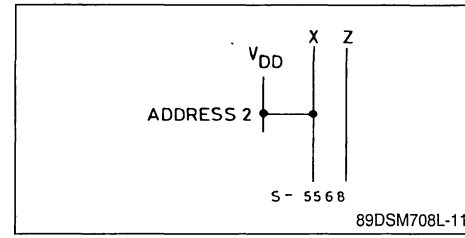
89DSM708L-10

Address Number	Transmitted Code				Address Input Code	
	A1	A2	A3	A4	X	Z
1	0	0	0	0	L	L
2	1	0	0	0	H	L
9	0	0	0	1	L	H
10	1	0	0	1	H	H

TAB-05

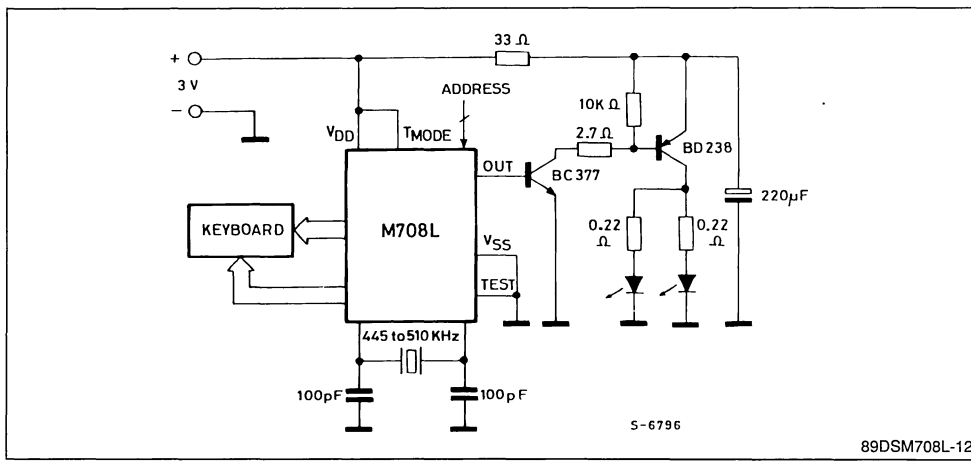
The Address inputs have internal pull-downs which are disabled during stand-by.

Note : Unused inputs can be left open or connected to V_{SS}

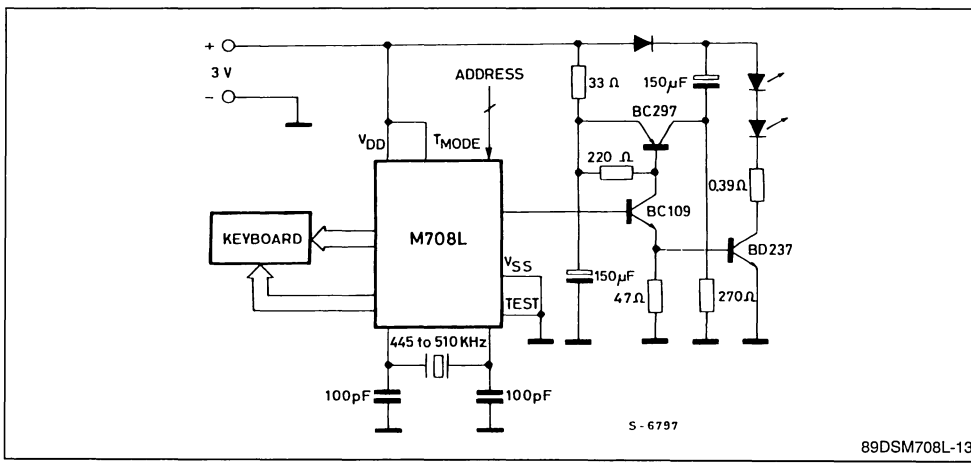


TYPICAL APPLICATION (flash mode)

STANDARD

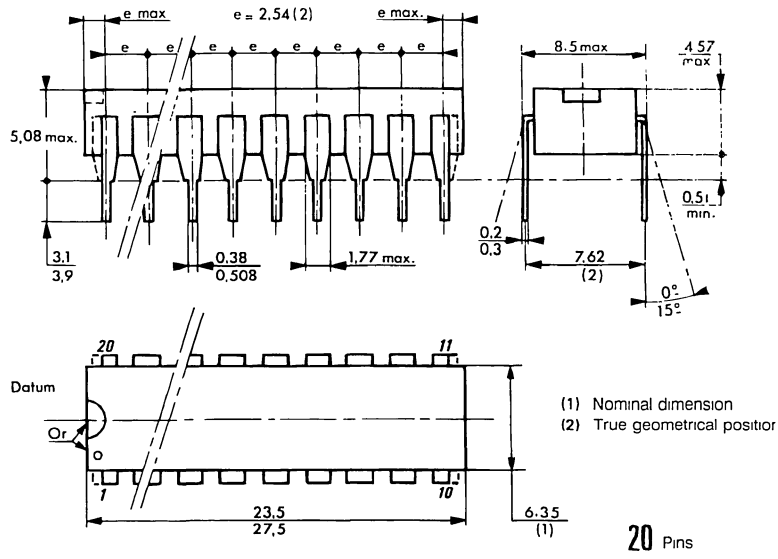


VOLTAGE DUPLICATOR



PACKAGE MECHANICAL DATA

20 PINS - PLASTIC DIP



PCM REMOTE CONTROL TRANSMITTERS

- M 709 : 40 COMMANDS x 16 ADDRESSES
- M 710 : 64 COMMANDS x 16 ADDRESSES
- ADDRESS ORGANIZATION PROVIDES WIDE RANGE OF SIMULTANEOUS APPLICATIONS WITHOUT INTERFERENCE BETWEEN SYSTEMS
- IMPROVED PCM TRANSMISSION CODE PROVIDES EASY RECOGNITION OF FALSE SIGNALS
- "FLASH" OR "CARRIER" PIN SELECTABLE TRANSMISSION MODES
- END OF TRANSMISSION CODE
- SINGLE CONTACT MATRIX KEYBOARD
- INTEGRATED ANTIBOUNCE AND INTERLOCK
- WIDE SUPPLY RANGE (M709 - M710 4.5 to 10.5V) / (M709A - M710A 3 to 10.5V)
- WIDE REFERENCE FREQUENCY RANGE (445 to 510kHz ceramic resonator)
- VERY LOW POWER CONSUMPTION DURING TRANSMISSION. OUTPUT DUTY CYCLE 0.15% (flash mode), 0.7% (carrier mode)
- FULLY COMPATIBLE WITH M491 AND M494 (In flash mode)

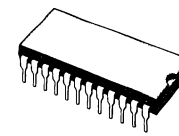
DESCRIPTION

These ICs have been developed for remote control in consumer applications (TV, radio, videorecorders) or in the industrial field and use a highly reliable transmission code which has a capacity of 1024 channels. Each transmitted word is structured into 4 bits which constitute the address and 6 bits which constitute the command (64 commands available). One command (1 st = 000000) is used to transmit the "end of transmission code " when the key is released. Additional bits are transmitted for synchronization of transmitter and receiver clocks and for security checks. The address organization provides a wide range of simultaneous applications without interference between systems. The receiver accepts the decoded command only if the transmitted address matches the address selected at the receiver. 16 addresses are available for this purpose.

The reference oscillator is controlled by a cheap ceramic or LC resonator. Two types of transmission mode are available : "Flash" or "Carrier" mode.

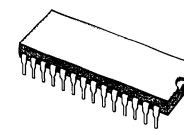
The M709 is a simplified version of the M710 which can only transmit 40 commands with 16 possible addresses. The M710 on the other hand has the full system capacity : it can transmit 64 commands with 16 addresses.

The M709 and M710 are produced with CMOS Si-gate technology and are available in 24 and 28-pin dual in-line plastic packages respectively.



DIP24
(Plastic Package)

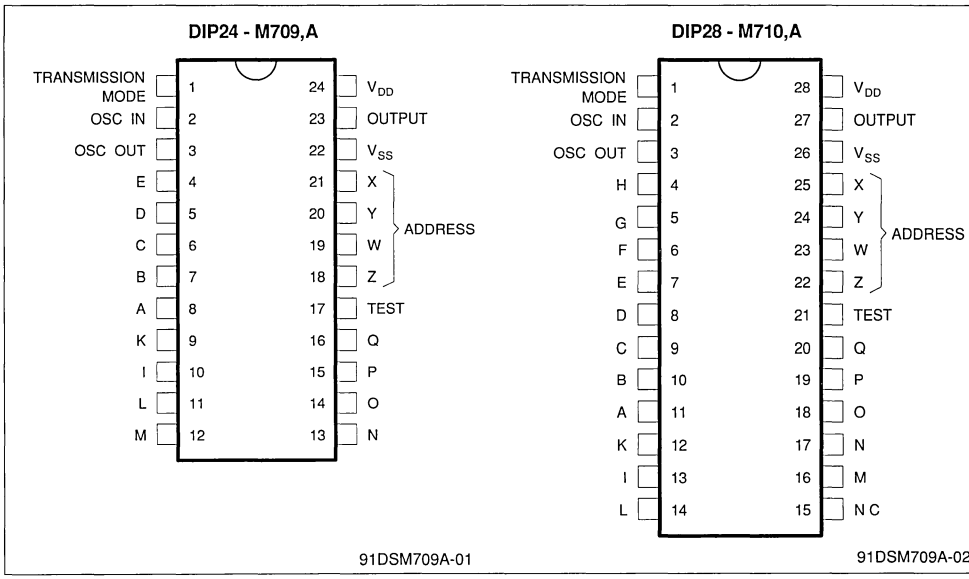
ORDER CODES : M709B1/M709AB1



DIP28
(Plastic Package)

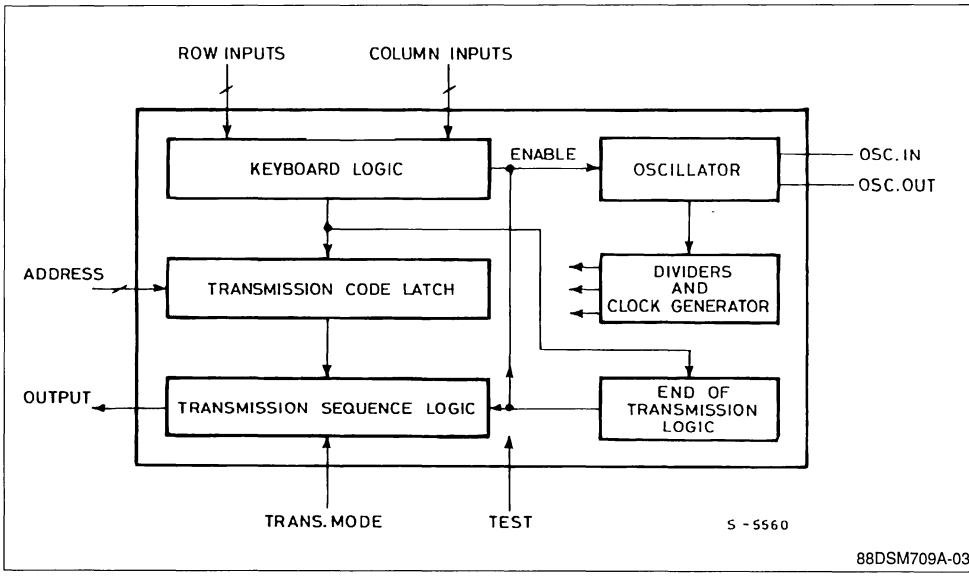
ORDER CODES : M710B1/M710AB1

PIN CONNECTIONS



Note : The test pin must be connected to V_{ss}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	-0.3 to 12	V
V_I	Input Voltage Range	-0.3 to V_{DD} + 0.3	V
$\|I_O\|$	IR Output Current (t< 50µs)	10	mA
P_{tot}	Total Package Power Dissipation	200	mW
T_{oper}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to +125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS

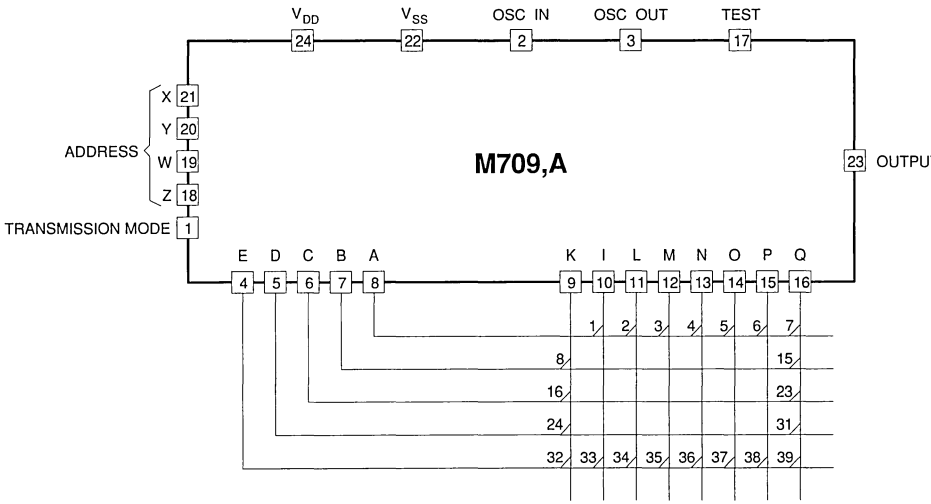
Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range : M709/M710 M709A/M710A	4.5 to 10.5 3 to 10.5	V V
V_I	Input Voltage Range	0 to V_{DD}	V
$\|I_O\|$	IR Output Current (t< 50µs)	max. 2.5	mA
f_{ref}	Reference Frequency Range	445 to 510	kHz
T_{oper}	Operating Temperature Range	0 to 70	°C
r_s	Serial Resistance of a Closed Key Contact	max. 2.5	kΩ
r_p	Parallel Resistance of Open Key Contact	min. 2.2	MΩ
R_S	Serial Resistance of the Ceramic Resonator	max. 20	Ω

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

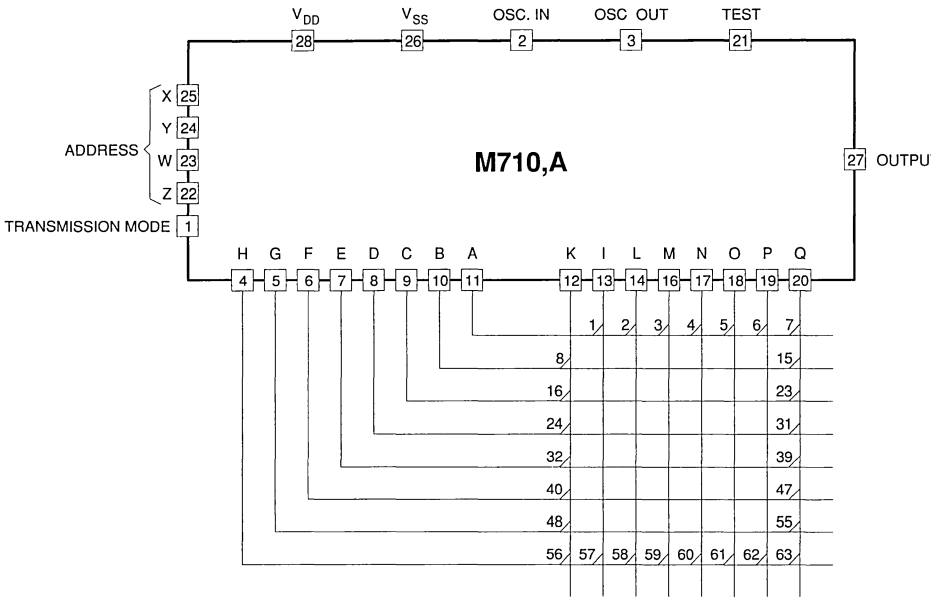
Typical values are at 9V and T_{AMB} = 25°C

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current	M709 Pin 24 M710 Pin 28	V_{DD} = 9V, IR Output open Stand-by Operating (one key closed)		 5 4	 15 7	 µA mA
I_{OH}	High State IR Output Current	M709 Pin 23 M710 Pin 27	V_{DD} = 9V, V_{OH} = 8V V_{DD} = 4.5V, V_{OH} = 3.5V	-1.5 -0.3	-2.5 -0.5		mA mA
I_{OL}	Low State IR Output Current	M709 Pin 23 M710 Pin 27	V_{DD} = 9V, V_{OL} = 1V V_{DD} = 4.5V, V_{OL} = 1V	1.5 0.3	2.5 0.5		mA mA
V_{TH}	Input Threshold High	Selection Inputs A to H	V_{DD} = 9V V_{DD} = 4.5V			6 3	V V
V_{TL}	Input Threshold Low	Selection Inputs K to Q	V_{DD} = 9V V_{DD} = 4.5V	3 1.5			V V
I_{IL}	Input Low Current	Pull-up Inputs A to H	V_{DD} = 9V, V_{IL} = 4.5V	-60		-300	µA
I_{IH}	Input High Current	Pull-down Inputs K to Q	V_{DD} = 9V, V_{IH} = 4.5V	60		300	µA
I_{IH}	Input High Current	Address Selection Inputs	V_{DD} = 9V, V_{IL} = 8.25V (oscillator running)			150	µA
I_L	Input Leakage Current	Trans. Mode Test Pin	V_{DD} = 9V, V_{IN} = 0 to 9V			1	µA
I_{OS}	Output Current	Osc. Out	V_{DD} = 9V, Osc. In. = V_{SS}	-2		-8	µA

FUNCTIONAL DESCRIPTION



91DSM709A-04



91DSM709A-05

TRUTH TABLE

Command N°	Input Code																Command Bits					
	A	B	C	D	E	F	G	H	K	I	L	M	N	O	P	Q	C1	C2	C3	C4	C5	C6
0	END OF TRANSMISSION																0	0	0	0	0	0
1	X									X							1	0	0	0	0	0
2	X										X						0	1	0	0	0	0
3	X											X					1	1	0	0	0	0
4	X												X				0	0	1	0	0	0
5	X													X			1	0	1	0	0	0
6	X														X		0	1	1	0	0	0
7	X															X	1	1	1	0	0	0
8		X							X								0	0	0	1	0	0
9		X								X							1	0	0	1	0	0
10		X									X						0	1	0	1	0	0
11		X										X					1	1	0	1	0	0
12		X											X				0	0	1	1	0	0
13		X												X			1	0	1	1	0	0
14		X													X		0	1	1	1	0	0
15		X														X	1	1	1	1	0	0
16			X						X								0	0	0	1	0	0
17			X							X							1	0	0	1	0	0
18			X								X						0	1	0	1	0	0
19			X									X					1	1	0	1	0	0
20			X										X				0	0	1	1	0	0
21			X											X			1	0	1	1	0	0
22			X												X		0	1	1	1	0	0
23			X													X	1	1	1	1	0	0
24				X					X								0	0	0	1	0	0
25				X						X							1	0	0	1	0	0
26				X							X						0	1	0	1	0	0
27				X								X					1	1	0	1	0	0
28				X									X				0	0	1	1	0	0
29				X										X			1	0	1	1	0	0
30				X											X		0	1	1	1	0	0
31				X												X	1	1	1	1	0	0
32					X				X								0	0	0	1	0	0
33					X					X							1	0	0	1	0	0
34					X						X						0	1	0	1	0	0
35					X							X					1	1	0	1	0	0
36					X								X				0	0	1	1	0	0
37					X									X			1	0	1	1	0	0
38					X										X		0	1	1	1	0	0
39					X											X	1	1	1	1	0	0
40						X			X								0	0	0	1	0	1
41						X				X							1	0	0	1	0	1
42						X					X						0	1	0	1	0	1
43						X						X					1	1	0	1	0	1
44						X							X				0	0	1	1	0	1
45						X								X			1	0	1	1	0	1
46						X									X		0	1	1	1	0	1
47						X										X	1	1	1	1	0	1

TAB-01

TRUTH TABLE (continued)

Command N°	Input Code															Command Bits					
	A	B	C	D	E	F	G	H	K	I	L	M	N	O	P	Q	C1	C2	C3	C4	C5	C6
48							X		X								0	0	0	0	1	1
49							X			X							1	0	0	0	1	1
50							X				X						0	1	0	0	1	1
51							X					X					1	1	0	0	1	1
52							X						X				0	0	1	0	1	1
53							X							X			1	0	1	0	1	1
54							X								X		0	1	1	0	1	1
55							X									X	1	1	1	0	1	1
56								X	X								0	0	0	1	1	1
57								X		X							1	0	0	1	1	1
58								X			X						0	1	0	1	1	1
59								X				X					1	1	0	1	1	1
60								X					X				0	0	1	1	1	1
61								X						X			1	0	1	1	1	1
62								X							X		0	1	1	1	1	1
63								X								X	1	1	1	1	1	1

TAB-02

DESCRIPTION

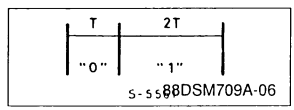
The signals are transmitted with infrared light using pulse code modulation. Each word consists of 12 bits. The binary information of a bit is determined by the time interval between two pulses.

If "T" is the time base, the bits are coded as follows :

Odd bits (1, 3, etc)

0 = T

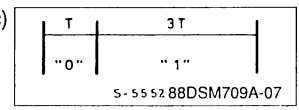
1 = 2T



Even bits (2, 4, etc)

0 = T

1 = 3T



The different code introduced for the even and odd "1s" improves the capability to recognize false codes at the receiver end. For example the double error which can cause the exchange "10" with "01" is easily detected.

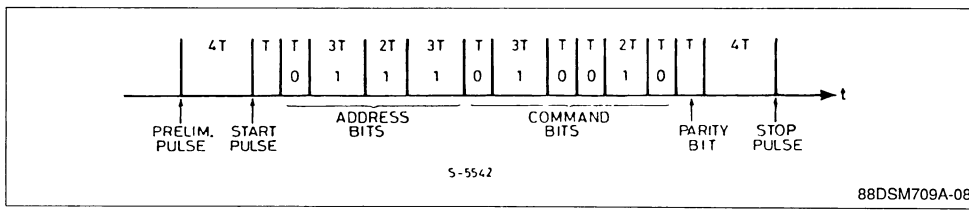
A parity bit is also added in order to further increase the reliability of the transmission. This bits is "1" if the number of transmitted "1s" is even while it is "0" if the number of transmitted "1s" is odd.

In addition, every word contains a preliminary pulse, a start pulse and a stop pulse. The spacing between the preliminary and the start pulse is 4T. This is followed after 1T by 11 data pulses (one parity bit), and terminated after 4T interval by a stop pulse.

Consequently, a word in which the binary digit 0 occurs ten times has a total duration of 21T.

A word containing ten "1s" has a duration of 36T.

Example :



SYNCHRONIZATION BETWEEN TRANSMITTER AND RECEIVER

The transmitter and the receiver can operate with different reference frequencies.

Typical values suitable for correct operation of the system should be between 445 and 510kHz, using a cheap ceramic resonator.

Synchronization between the transmitter and the receiver, necessary to obtain the wide range of frequency tolerance described above is achieved by measuring in the receiver the interval between the start pulse and the first data pulse, storing this value and using it as time base T.

KEYBOARD (pins A to Q) / CODE REPETITION

One column input (K to Q) has to be connected to one row (A to H) input to activate the transmitter. The contact must be continuously closed for a minimum of 25ms.

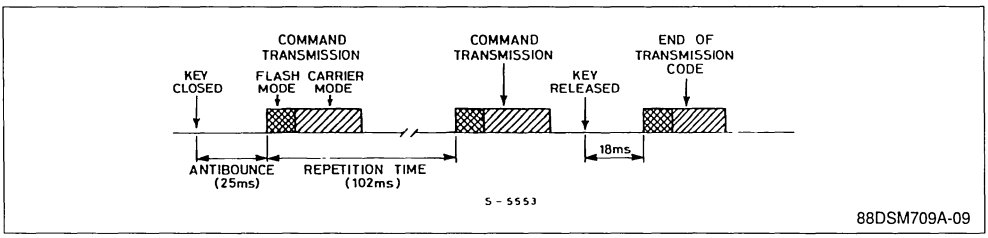
Double and multiple contact operations are not accepted.

The command information is repeatedly transmitted at intervals of 102ms (f_{ref} = 500kHz) as long as the push button remains operated.

When the contact is interrupted the circuit transmits, after a pause of about 18 ms, the "end of transmission code" and returns to stand-by mode.

If the contact is interrupted while a command is being transmitted the circuit carries on with the transmission to the end. After a pause of about 18 ms it transmits the end of transmission code.

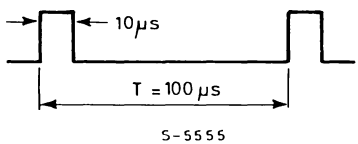
No command is accepted until the "end of transmission code" is over.



TRANSMISSION MODE (pin 1)

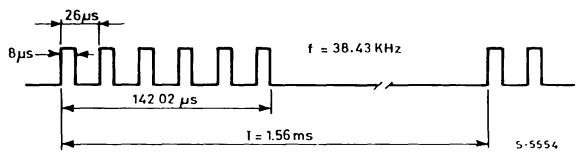
The M709/M710 can operate in Flash (pin 1 = V_{DD}) or Carrier (pin 1 = V_{SS}) transmission modes. Using a reference frequency of 500kHz the output signal has these formats :

Flash mode



Transmission time
min. = 2.1 ms
max. = 3.6 ms
duty cycle = 0.15 %

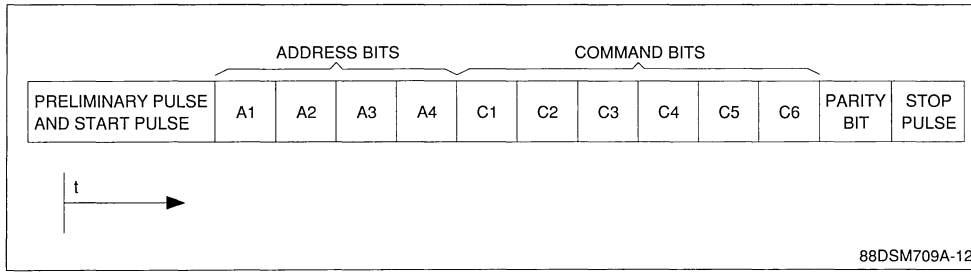
Carrier mode



Transmission time
min. = 32.76 ms
max. = 56.16 ms
duty cycle = 0.7 %

ADDRESS (pins X, Y, W, Z)

The Address information is coded and transmitted as follows :

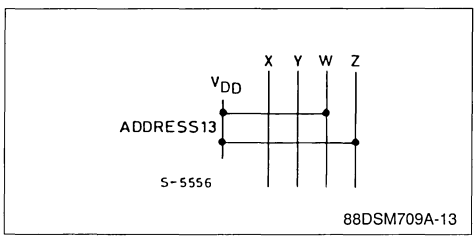


Address Number	Transmitted Code				Address Input Code			
	A1	A2	A3	A4	X	Y	W	Z
1	0	0	0	0	L	L	L	L
2	1	0	0	0	H	L	L	L
3	0	1	0	0	L	H	L	L
4	1	1	0	0	H	H	L	L
5	0	0	1	0	L	L	H	L
6	1	0	1	0	H	L	H	L
7	0	1	1	0	L	H	H	L
8	1	1	1	0	H	H	H	L
9	0	0	0	1	L	L	L	H
10	1	0	0	1	H	L	L	H
11	0	1	0	1	L	H	L	H
12	1	1	0	1	H	H	L	H
13	0	0	1	1	L	L	H	H
14	1	0	1	1	H	L	H	H
15	0	1	1	1	L	H	H	H
16	1	1	1	1	H	H	H	H

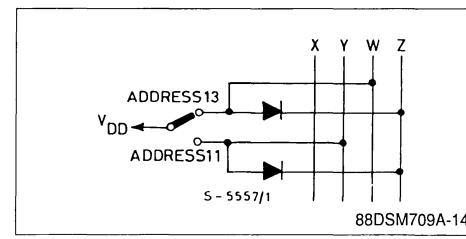
TAB-03

The address inputs have internal pull-downs which are disabled during stand-by.

Single address selection



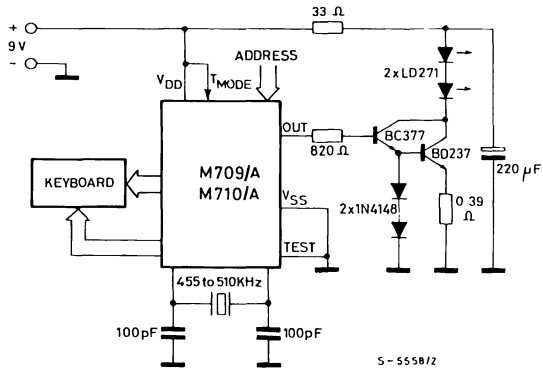
Multiple address selection



Note : unused inputs can be left open or connected to V_{SS}

TYPICAL APPLICATIONS

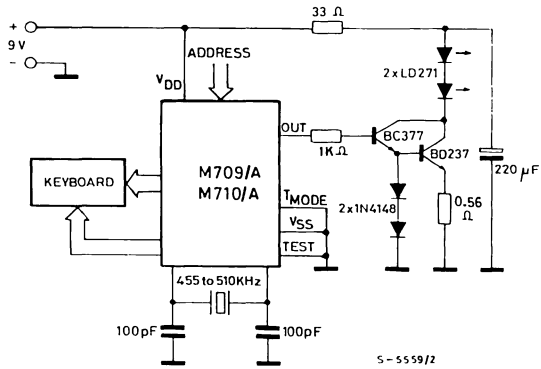
FLASH MODE



88DSM709A-15

INFRARED DIODE PEAK CURRENT = 1.8 A
TOTAL AVERAGE CONSUMPTION = 6.5 mA

CARRIER MODE

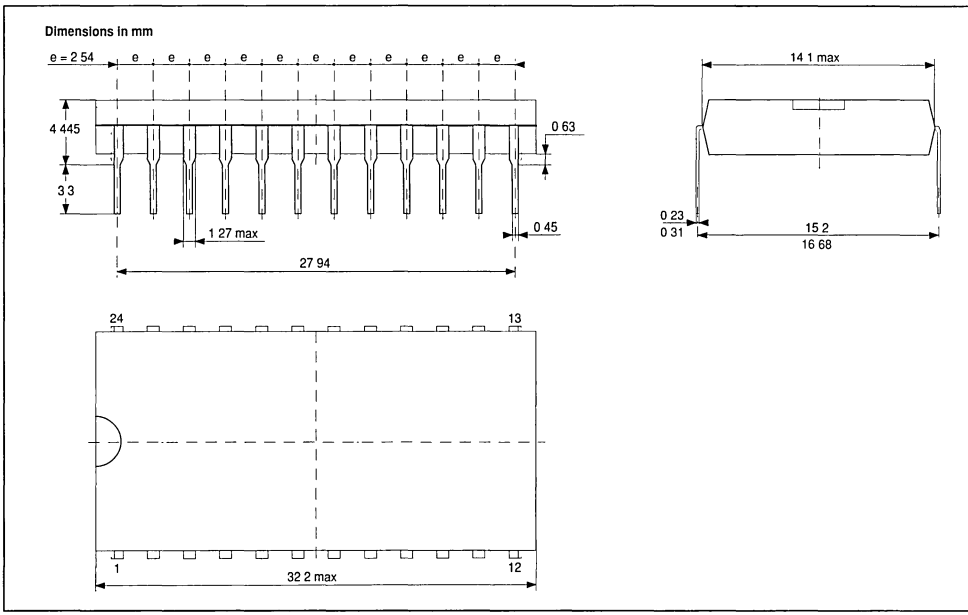


88DSM709A-16

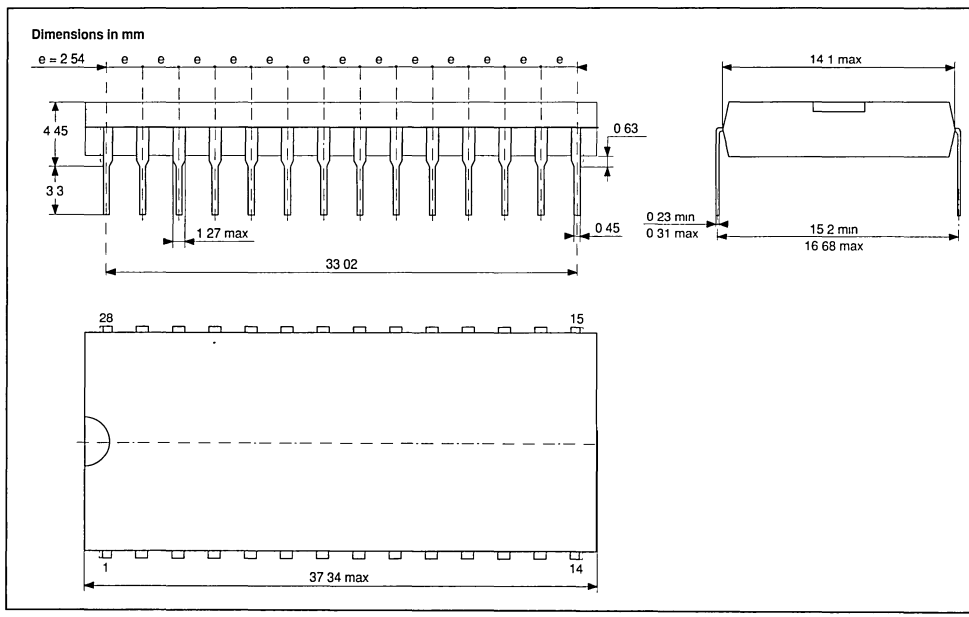
INFRARED DIODE PEAK CURRENT = 1.25 A
TOTAL AVERAGE CONSUMPTION = 13 mA

PACKAGE MECHANICAL DATA

24 PINS - PLASTIC DIP



28 PINS - PLASTIC DIP



PCM REMOTE CONTROL TRANSMITTERS (LOW VOLTAGE)

- 2.2V TO 5V OPERATING SUPPLY VOLTAGE RANGE
- M 709L : 40 COMMANDS x 16 ADDRESSES
- M 710L : 64 COMMANDS x 16 ADDRESSES
- ADDRESS ORGANIZATION PROVIDES WIDE RANGE OF SIMULTANEOUS APPLICATIONS WITHOUT INTERFERENCE BETWEEN SYSTEMS
- IMPROVED PCM TRANSMISSION CODE PROVIDES EASY RECOGNITION OF FALSE SIGNALS
- "FLASH" OR "CARRIER" PIN SELECTABLE TRANSMISSION MODES
- END OF TRANSMISSION CODE
- SINGLE CONTACT MATRIX KEYBOARD
- INTEGRATED ANTIBOUNCE AND INTERLOCK
- WIDE REFERENCE FREQUENCY RANGE (445 to 510 kHz ceramic resonator)
- VERY LOW POWER CONSUMPTION DURING TRANSMISSION. OUTPUT DUTY CYCLE 0.15 % (flash mode), 0.7 % (carrier mode)
- FULLY COMPATIBLE WITH M491 AND M494 (In flash mode)

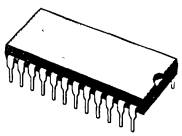
DESCRIPTION

These ICs have been developed for remote control in consumer applications (TV, radio, videorecorders) or in the industrial field and use a highly reliable transmission code which has a capacity of 1024 channels. Each transmitted word is structured into 4 bits which constitute the address and 6 bits which constitute the command (64 commands available). One command (1 st = 000000) is used to transmit the "end of transmission code" when the key is released. Additional bits are transmitted for synchronization of transmitter and receiver clocks and for security checks. The address organization provides a wide range of simultaneous applications without interference between systems. The receiver accepts the decoded command only if the transmitted address matches the address selected at the receiver. 16 addresses are available for this purpose.

The reference oscillator is controlled by a cheap ceramic or LC resonator. Two types of transmission mode are available : "Flash" or "Carrier" mode.

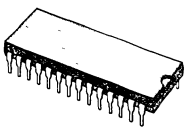
The M709L is a simplified version of the M710L which can only transmit 40 commands with 16 possible addresses. The M710L on the other hand has the full system capacity : it can transmit 64 commands with 16 addresses.

The M709L and M710L are produced with CMOS Si-gate technology and are available in 24 and 28-pin dual in-line plastic packages respectively.



DIP24
(Plastic Package)

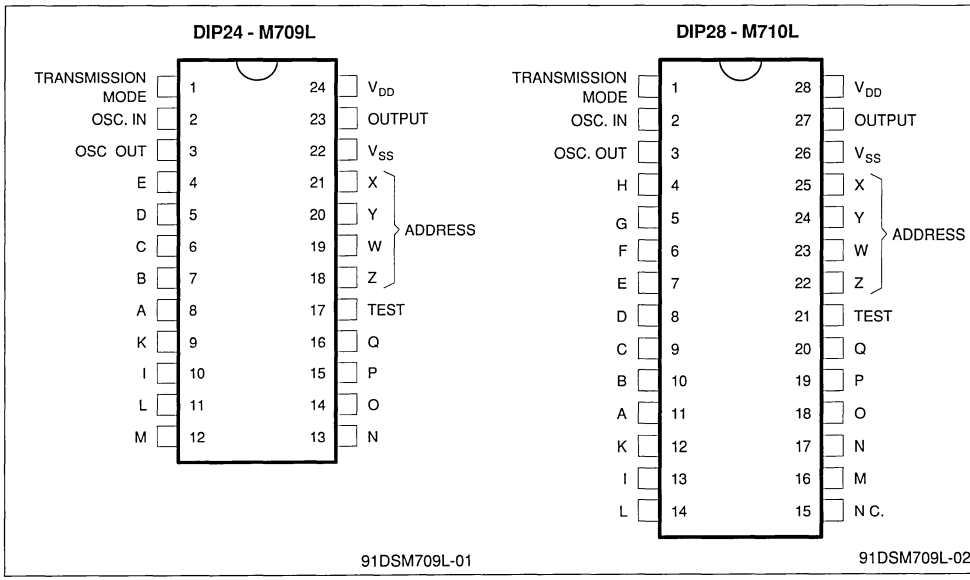
ORDER CODE : M709LB1



DIP28
(Plastic Package)

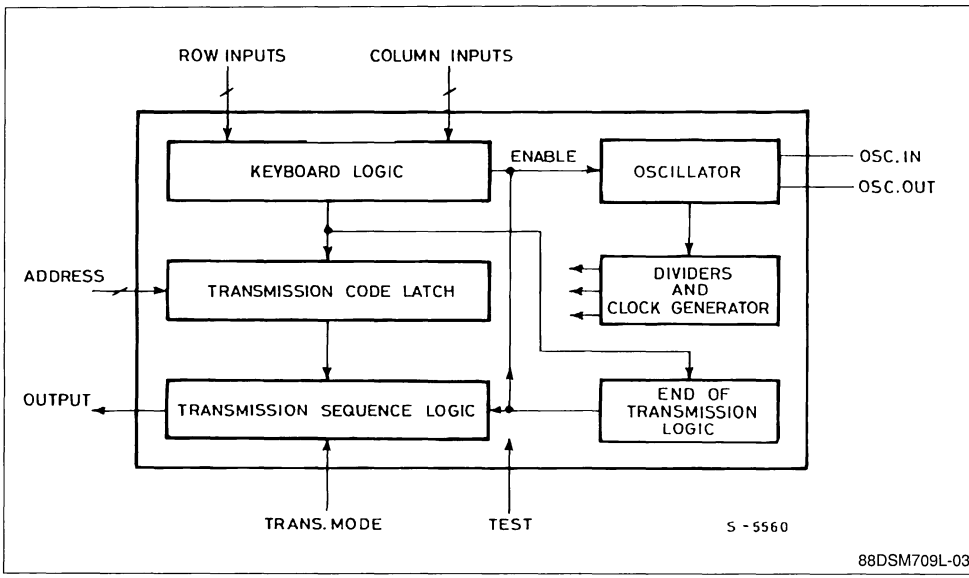
ORDER CODE : M710LB1

PIN CONNECTIONS



Note : The test pin must be connected to V_{SS}.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	-0.3 to 5.5	V
V_I	Input Voltage Range	-0.3 to V_{DD} + 0.3	V
$\|I_O\|$	IR Output Current (t< 50µs)	10	mA
P_{tot}	Total Package Power Dissipation	200	mW
T_{oper}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to +125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS

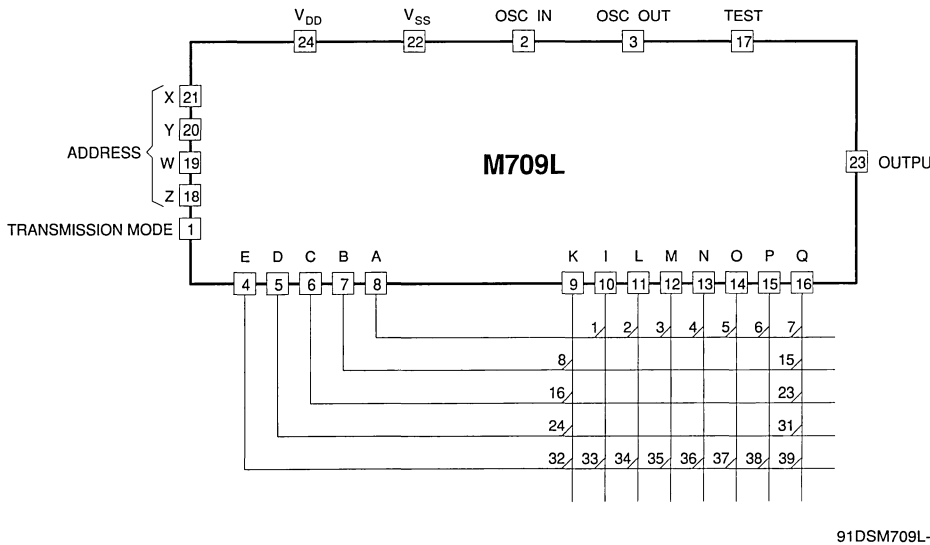
Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	2.2 to 5	V
V_I	Input Voltage Range	0 to V_{DD}	V
$\|I_O\|$	IR Output Current (t< 50µs)	max. 2.5	mA
f_{ref}	Reference Frequency Range	445 to 510	kHz
T_{oper}	Operating Temperature Range	0 to 70	°C
r_s	Serial Resistance of a Closed Key Contact	max. 2.5	kΩ
r_p	Parallel Resistance of Open Key Contact	min. 2.2	MΩ
R_S	Serial Resistance of the Ceramic Resonator	max. 20	Ω

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

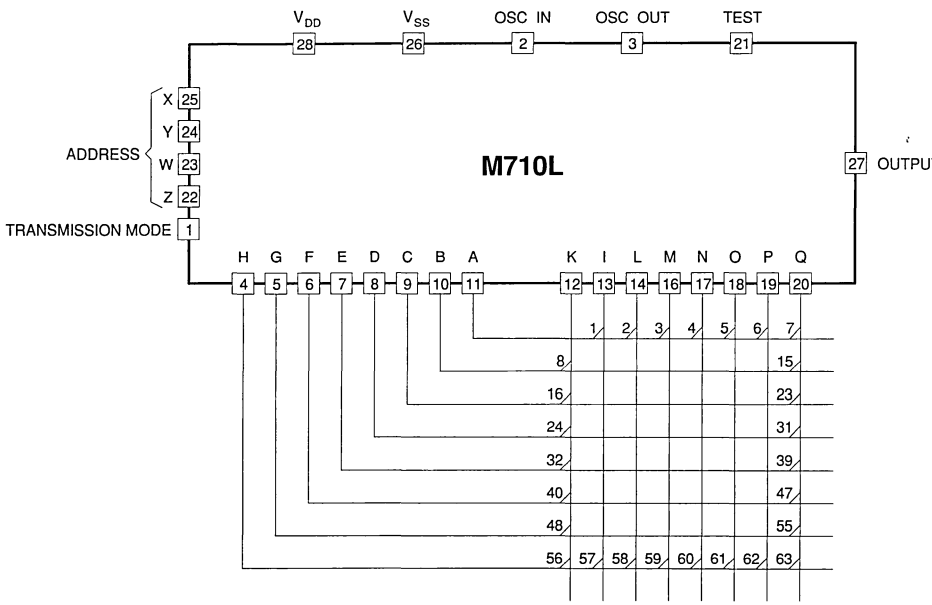
Typical values are at 9V and T_{AMB} = 25°C

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current		V_{DD} = 5V, IR Output Stand-by Operating (one key closed)		 3 4	 10 7	 µA mA
I_{OH}	High State IR Output Current		V_{DD} = 3V, V_{OH} = 2V V_{DD} = 2.2V, V_{OH} = 1V	-1 -0.3	-2 -0.5		mA mA
I_{OL}	Low State IR Output Current		V_{DD} = 3V, V_{OL} = 1V V_{DD} = 2.2V, V_{OL} = 1V	1 0.3	2 0.5		mA mA
I_{IH}	Input High Current	Address Selection Inputs	V_{DD} = 3V, V_{IL} = 3V (oscillator running)			150	µA
I_L	Input Leakage Current	Trans. Mode Test Pin	V_{DD} = 3V, V_{IN} = 0 to 3V			1	µA

FUNCTIONAL DESCRIPTION



91DSM709L-04



91DSM709L-05

TRUTH TABLE

Command N°	Input Code																Command Bits					
	A	B	C	D	E	F	G	H	K	I	L	M	N	O	P	Q	C1	C2	C3	C4	C5	C6
0	END OF TRANSMISSION																0	0	0	0	0	0
1	X									X							1	0	0	0	0	0
2	X										X						0	1	0	0	0	0
3	X											X					1	1	0	0	0	0
4	X												X				0	0	1	0	0	0
5	X													X			1	0	1	0	0	0
6	X														X		0	1	1	0	0	0
7	X															X	1	1	1	0	0	0
8		X							X								0	0	0	1	0	0
9		X								X							1	0	0	1	0	0
10		X									X						0	1	0	1	0	0
11		X										X					1	1	0	1	0	0
12		X											X				0	0	1	1	0	0
13		X												X			1	0	1	1	0	0
14		X													X		0	1	1	1	0	0
15		X														X	1	1	1	1	0	0
16			X						X								0	0	0	1	0	0
17			X							X							1	0	0	1	0	0
18			X								X						0	1	0	1	0	0
19			X									X					1	1	0	1	0	0
20			X										X				0	0	1	1	0	0
21			X											X			1	0	1	1	0	0
22			X												X		0	1	1	1	0	0
23			X													X	1	1	1	1	0	0
24				X					X								0	0	0	1	0	0
25				X						X							1	0	0	1	0	0
26				X							X						0	1	0	1	0	0
27				X								X					1	1	0	1	0	0
28				X									X				0	0	1	1	0	0
29				X										X			1	0	1	1	0	0
30				X											X		0	1	1	1	0	0
31				X												X	1	1	1	1	0	0
32					X				X								0	0	0	1	0	0
33					X					X							1	0	0	1	0	0
34					X						X						0	1	0	1	0	0
35					X							X					1	1	0	1	0	0
36					X								X				0	0	1	1	0	0
37					X									X			1	0	1	1	0	0
38					X										X		0	1	1	1	0	0
39					X											X	1	1	1	1	0	0
40						X			X								0	0	0	1	0	1
41						X				X							1	0	0	1	0	1
42						X					X						0	1	0	1	0	1
43						X						X					1	1	0	1	0	1
44						X							X				0	0	1	1	0	1
45						X								X			1	0	1	1	0	1
46						X									X		0	1	1	1	0	1
47						X										X	1	1	1	1	0	1

TAB-01

TRUTH TABLE (continued)

Command N°	Input Code															Command Bits					
	A	B	C	D	E	F	G	H	K	I	L	M	N	O	P	Q	C1	C2	C3	C4	C5	C6
48							X		X								0	0	0	0	1	1
49							X			X							1	0	0	0	1	1
50							X				X						0	1	0	0	1	1
51							X					X					1	1	0	0	1	1
52							X						X				0	0	1	0	1	1
53							X							X			1	0	1	0	1	1
54							X								X		0	1	1	0	1	1
55							X									X	1	1	1	0	1	1
56								X	X								0	0	0	1	1	1
57								X		X							1	0	0	1	1	1
58								X			X						0	1	0	1	1	1
59								X				X					1	1	0	1	1	1
60								X					X				0	0	1	1	1	1
61								X						X			1	0	1	1	1	1
62								X							X		0	1	1	1	1	1
63								X								X	1	1	1	1	1	1

TAB-02

DESCRIPTION

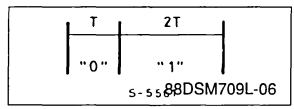
The signals are transmitted with infrared light using pulse code modulation. Each word consists of 12 bits. The binary information of a bit is determined by the time interval between two pulses.

If "T" is the time base, the bits are coded as follows :

Odd bits (1, 3, etc)

0 = T

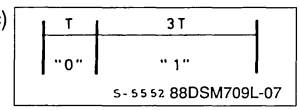
1 = 2T



Even bits (2, 4, etc)

0 = T

1 = 3T



The different code introduced for the even and odd "1s" improves the capability to recognize false codes at the receiver end. For example the double error which can cause the exchange "10" with "01" is easily detected.

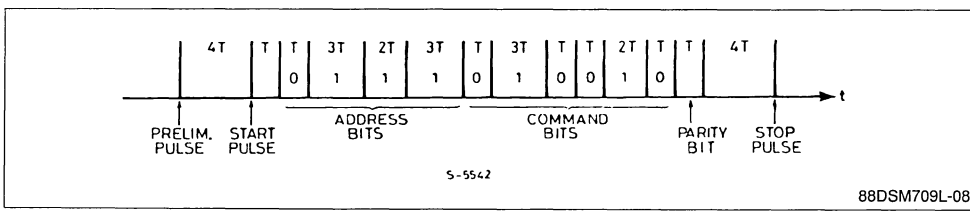
A parity bit is also added in order to further increase the reliability of the transmission. This bits is "1" if the number of transmitted "1s" is even while it is "0" if the number of transmitted "1s" is odd.

In addition, every word contains a preliminary pulse, a start pulse and a stop pulse. The spacing between the preliminary and the start pulse is 4T. This is followed after 1T by 11 data pulses (one parity bit), and terminated after 4T interval by a stop pulse.

Consequently, a word in which the binary digit 0 occurs ten times has a total duration of 21T.

A word containing ten "1s" has a duration of 36T.

Example :



SYNCHRONIZATION BETWEEN TRANSMITTER AND RECEIVER

The transmitter and the receiver can operate with different reference frequencies.

Typical values suitable for correct operation of the system should be between 445 and 510 kHz, using a cheap ceramic resonator.

Synchronization between the transmitter and the receiver, necessary to obtain the wide range of frequency tolerance described above is achieved by measuring in the receiver the interval between the start pulse and the first data pulse, storing this value and using it as time base T.

KEYBOARD (pins A to Q) / CODE REPETITION

One column input (K to Q) has to be connected to one row (A to H) input to activate the transmitter. The contact must be continuously closed for a minimum of 25 ms.

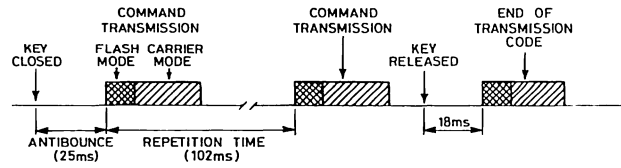
Double and multiple contact operations are not accepted.

The command information is repeatedly transmitted at intervals of 102 ms (f_{ref} = 500 kHz) as long as the push button remains operated.

When the contact is interrupted the circuit transmits, after a pause of about 18 ms, the "end of transmission code" and returns to stand-by mode.

If the contact is interrupted while a command is being transmitted the circuit carries on with the transmission to the end. After a pause of about 18 ms it transmits the end of transmission code.

No command is accepted until the "end of transmission code" is over.



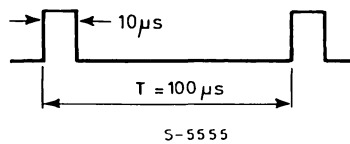
88DSM709L-09

TRANSMISSION MODE (pin 7)

The M709L/M710L can operate in Flash (pin T = V_{DD}) or Carrier (pin T = V_{SS}) transmission modes.

Using a reference frequency of 500 kHz the output signal has these formats :

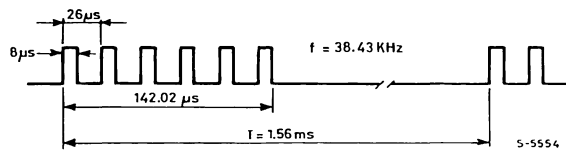
Flash mode



Transmission time
min. = 2.1 ms
max. = 3.6 ms
duty cycle = 0.15 %

88DSM709L-10

Carrier mode

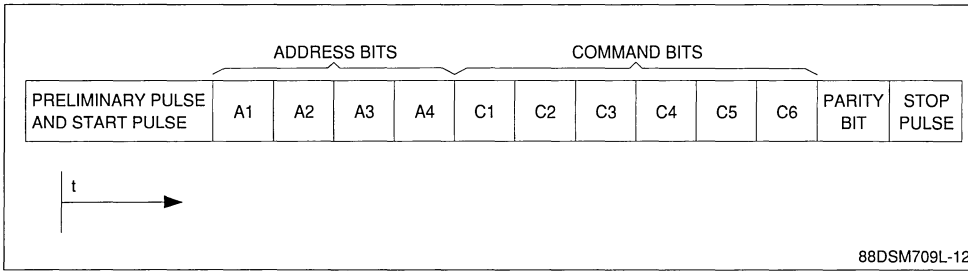


Transmission time
min. = 32.76 ms
max. = 56.16 ms
duty cycle = 0.7 %

88DSM709L-11

ADDRESS (pins X, Y, W, Z)

The Address information is coded and transmitted as follows :

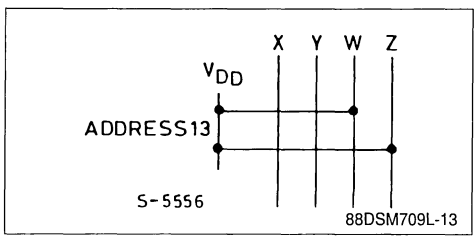


Address Number	Transmitted Code				Address Input Code			
	A1	A2	A3	A4	X	Y	W	Z
1	0	0	0	0	L	L	L	L
2	1	0	0	0	H	L	L	L
3	0	1	0	0	L	H	L	L
4	1	1	0	0	H	H	L	L
5	0	0	1	0	L	L	H	L
6	1	0	1	0	H	L	H	L
7	0	1	1	0	L	H	H	L
8	1	1	1	0	H	H	H	L
9	0	0	0	1	L	L	L	H
10	1	0	0	1	H	L	L	H
11	0	1	0	1	L	H	L	H
12	1	1	0	1	H	H	L	H
13	0	0	1	1	L	L	H	H
14	1	0	1	1	H	L	H	H
15	0	1	1	1	L	H	H	H
16	1	1	1	1	H	H	H	H

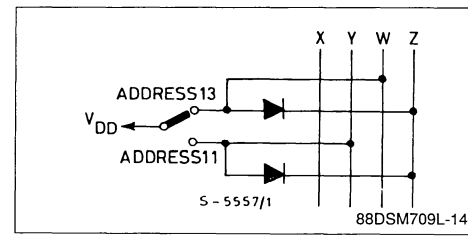
TAB-03

The address inputs have internal pull-downs which are disabled during stand-by.

Single address selection



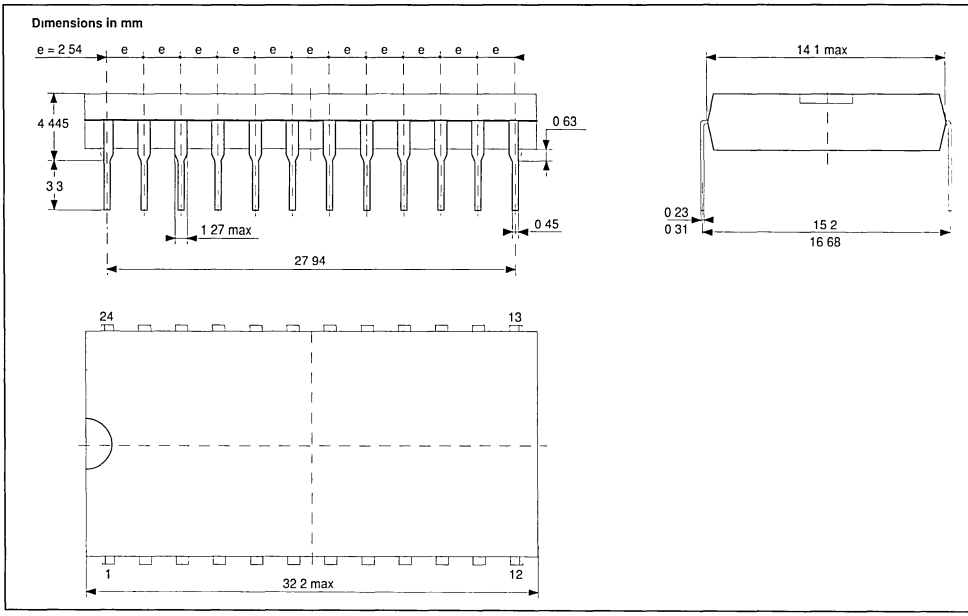
Multiple address selection



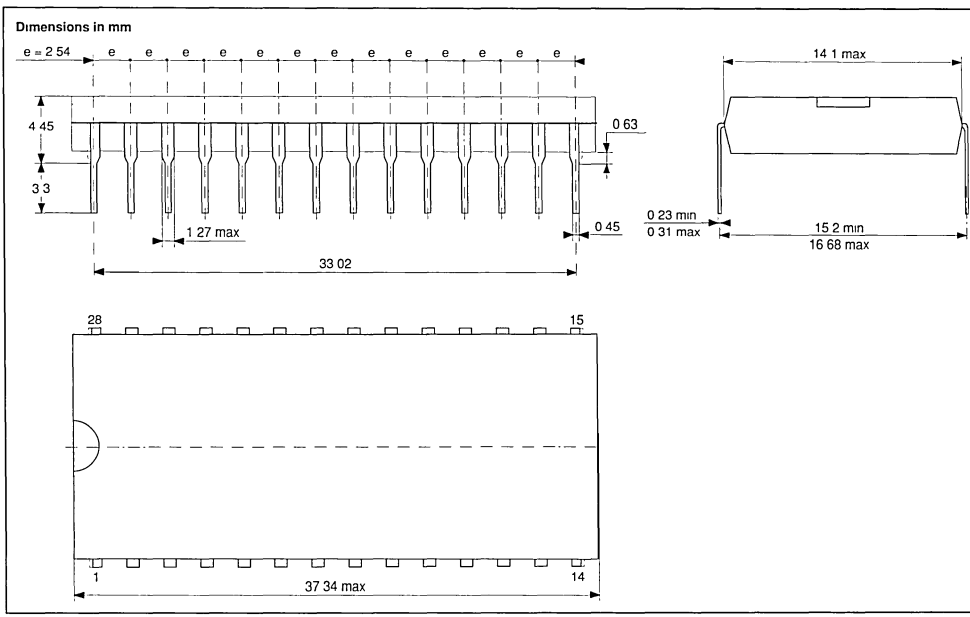
Note : unused inputs can be left open or connected to V_{SS}

PACKAGE MECHANICAL DATA

24 PINS - PLASTIC DIP



28 PINS - PLASTIC DIP

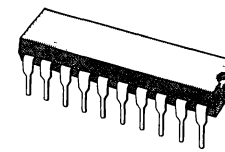


SGS-THOMSON MICROELECTRONICS

M3004AB1

REMOTE CONTROL TRANSMITTER

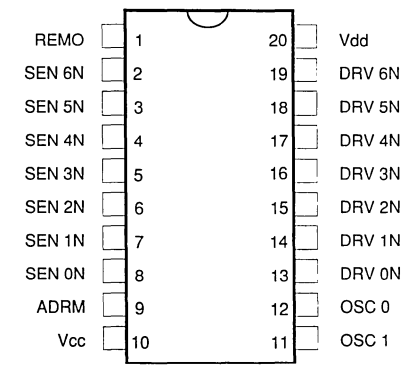
- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (– I_{OH} = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 4 TO 11V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

ORDER CODE : M3004AB1

PIN CONNECTIONS



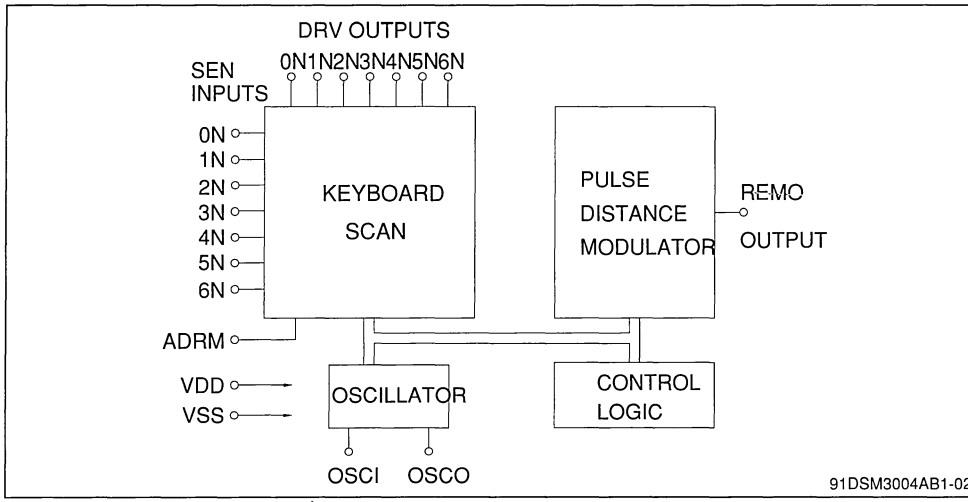
91DSM3004AB1-01

DESCRIPTION

The M3004AB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3004AB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmision.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.
In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function is an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.
The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1ms, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT / OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively.
Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.
In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.
In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.
There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.
The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing.

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_{ML} (µs)	t_{MH} (µs)	t_W (ms)
Flashed	2.53	8.8	-	-	-	121
Modulated	2.53	-	26.4	17.6	8.8	121

f_{OSC}	455kHz	t_{OSC} = 2.2µs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period LOW
t_{MH}	4 x t_{OSC}	Modulation Period HIGH
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	Word Distance

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O
Reference Time	3 x T_O

Table 3 : Transmission Mode and Sub-system Adress Selection.
The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	O						
A	2	0	0	1	X	O					
S	3	0	1	0	X	X	O				
H	4	0	1	1	X	X	X	O			
E	5	1	0	0	X	X	X	X	O		
D	6	1	0	1	X	X	X	X	X	O	
M											
O	0	1	1	1							O
D	1	0	0	0	O						O
U	2	0	0	1	X	O					O
L	3	0	1	0	X	X	O				O
A	4	0	1	1	X	X	X	O			O
T	5	1	0	0	X	X	X	X	O		O
E	6	1	0	1	X	X	X	X	X	O	O
D											

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
V_{SS}	SEN1N	0	0	1	1	1	1	8 to 15
V_{SS}	SEN2N	0	1	0	1	1	1	16 to 23
V_{SS}	SEN3N	0	1	1	1	1	1	24 to 31
V_{SS}	SEN4N	1	0	0	1	1	1	32 to 39
V_{SS}	SEN5N	1	0	1	1	1	1	40 to 47
V_{SS}	SEN6N	1	1	0	1	1	1	48 to 55
V_{SS}	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 12	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 150	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C		4		12	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz	V_{DD} = 6V		0.8	1.5	mA
		REMO,Output unload	V_{DD} = 9V		1.5	3	mA
		• Inactive (stand-by mode)	V_{DD} = 6V			2	µA
			V_{DD} = 9V			2	µA
f_{OSC}	Oscill. Frequency	V_{DD} = 4 to 11V (cer resonator)		350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N							
V_{IL}	Input Voltage Low	V_{DD} = 4 to 11V				0.2 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 4 to 11V		0.8 x V_{DD}			V
- I_I	Input Current	V_{DD} = 4V, V_I = 0V		25		250	µA
		V_{DD} = 11V, V_I = 0V		75		750	µA
I_I	Input Leakage Current	V_{DD} = 11V, V_I = VDD				1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N							
V_{OL}	Output Voltage "ON"	V_{DD} = 4V, I_O = 0.1mA				0.3	V
		V_{DD} = 11V, I_O = 1mA				0.5	V
I_O	Output Current "OFF"	V_{DD} = 11V, V_O = 11V				10	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.2 x V_{DD}	V
V_{IH}	Input Voltage High		0.8 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 6V, V_{OH} = 3V V_{DD} = 9V, V_{OH} = 6V	80 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 6V, V_{OL} = 0.2V V_{DD} = 9V, V_{OL} = 0.1V			0.6 0.6	mA mA
t_{OH}	Pulse Length	V_{DD} = 6V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 6V, OSC1 at V_{DD}	0.8		2.7	µA
V_{OH}	Output Voltage high	V_{DD} = 6V, - I_{OL} = 0.1mA			V_{DD} - 0.6	V
V_{OL}	Output Voltage Low	V_{DD} = 6V, I_{OH} = 0.1mA			0.6	V

Figure 1 : Typical Application.

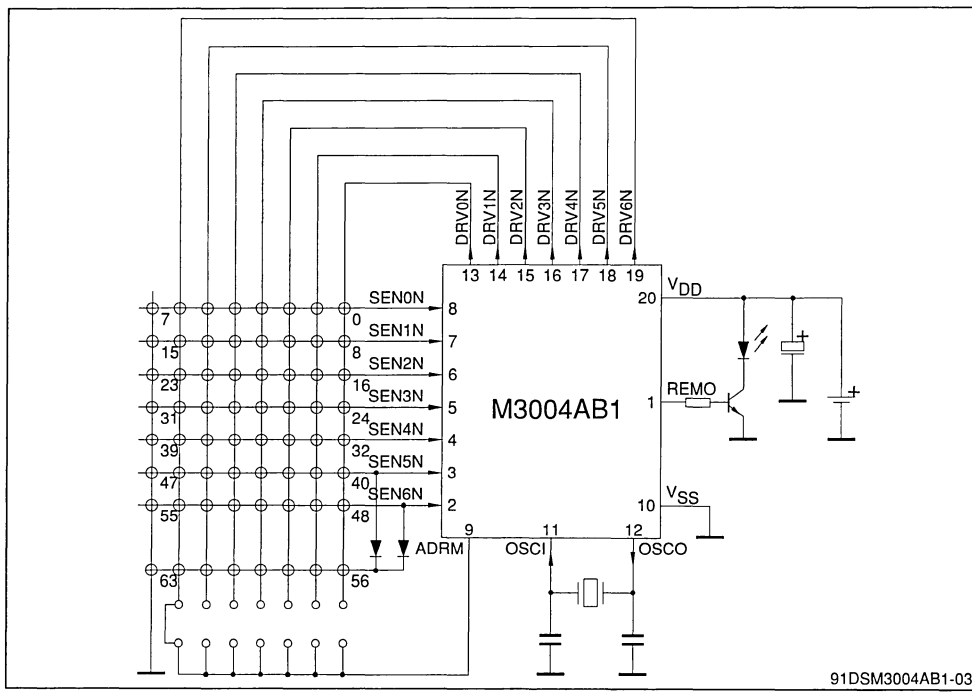


Figure 2 : Data Format of REMO Output; REF = Reference Time; T0 and T1 = Toggle bits; S0, S1 and S2 = System address; A, B, C, D, E and F = Command bits.
(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed)
(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

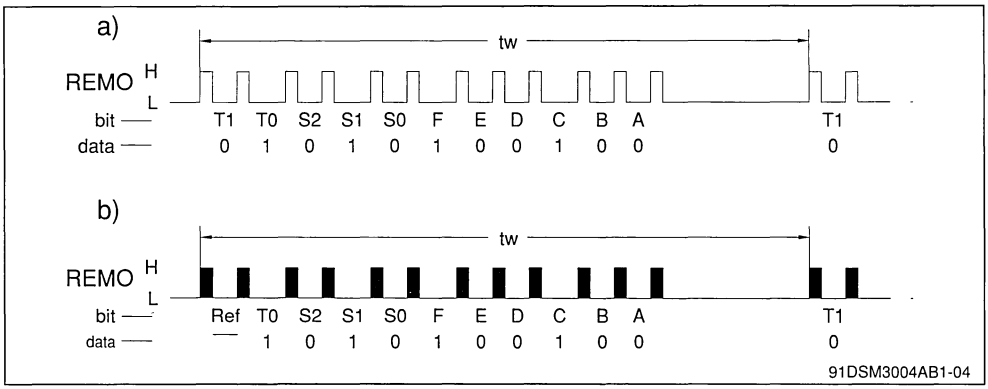


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse { $t_{PW} = (5 \times t_M) + t_{MH}$)}.

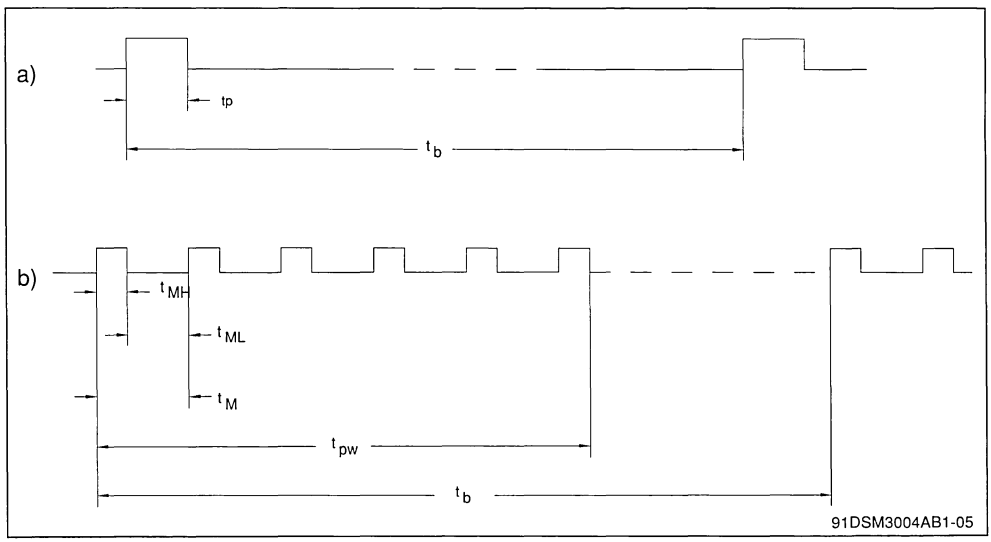


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

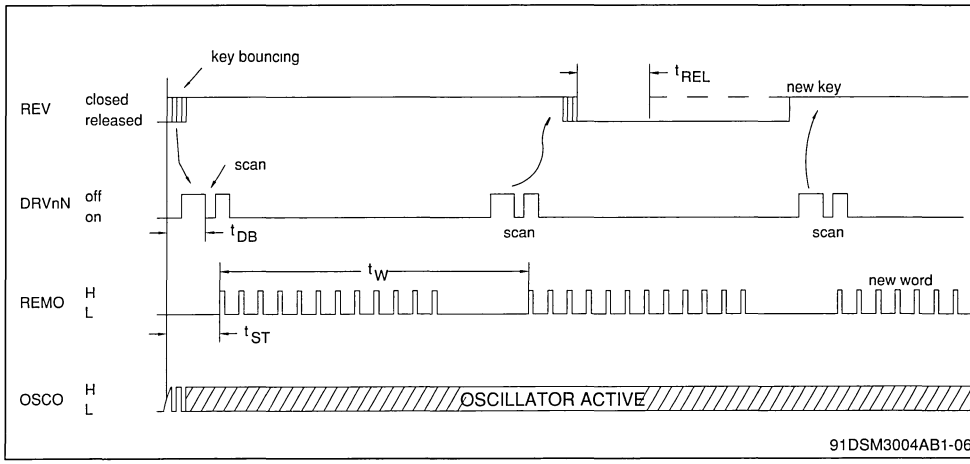
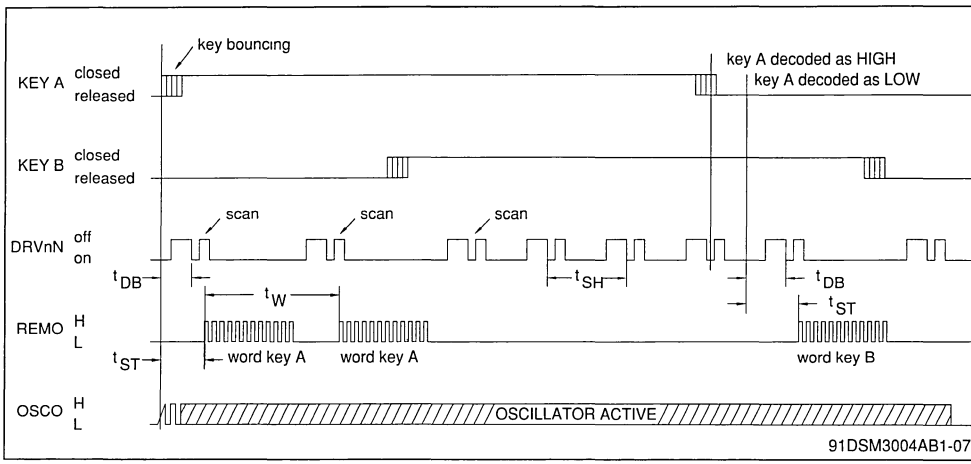


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.

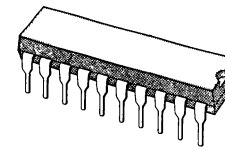


SGS-THOMSON MICROELECTRONICS

M3004LAB1

REMOTE CONTROL TRANSMITTER

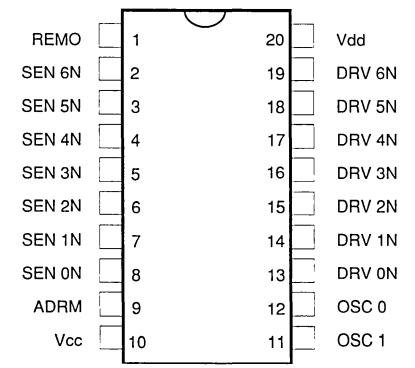
- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (– I_{OH} = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

ORDER CODE : M3004LAB1

PIN CONNECTIONS

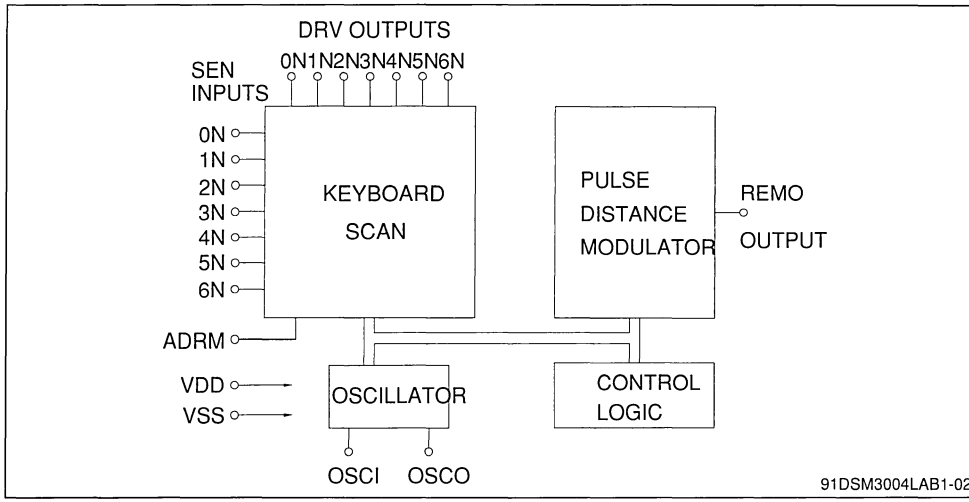


91DSM3004LAB1-01

DESCRIPTION

The M3004LAB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.
The M3004LAB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmision.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.
In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function is an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.
The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1ms, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT / OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively.
Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.
In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.
In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.
There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.
The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing.

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_{ML} (µs)	t_{MH} (µs)	t_W (ms)
Flashed	2.53	8.8	-	-	-	121
Modulated	2.53	-	26.4	17.6	8.8	121

f_{OSC}	455kHz	t_{OSC} = 2.2µs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period LOW
t_{MH}	4 x t_{OSC}	Modulation Period HIGH
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	Word Distance

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O
Reference Time	3 x T_O

Table 3 : Transmission Mode and Sub-system Adress Selection.
The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
FLASHED	0	1	1	1							
	1	0	0	0	O						
	2	0	0	1	X	O					
	3	0	1	0	X	X	O				
	4	0	1	1	X	X	X	O			
	5	1	0	0	X	X	X	X	O		
	6	1	0	1	X	X	X	X	X	O	
MODULATED	0	1	1	1							O
	1	0	0	0	O						O
	2	0	0	1	X	O					O
	3	0	1	0	X	X	O				O
	4	0	1	1	X	X	X	O			O
	5	1	0	0	X	X	X	X	O		O
	6	1	0	1	X	X	X	X	X	O	O

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
V_{SS}	SEN1N	0	0	1	1	1	1	8 to 15
V_{SS}	SEN2N	0	1	0	1	1	1	16 to 23
V_{SS}	SEN3N	0	1	1	1	1	1	24 to 31
V_{SS}	SEN4N	1	0	0	1	1	1	32 to 39
V_{SS}	SEN5N	1	0	1	1	1	1	40 to 47
V_{SS}	SEN6N	1	1	0	1	1	1	48 to 55
V_{SS}	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 7	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 125	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C	2		6.5	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz V_{DD} = 3V REMO,Output unload V_{DD} = 6V • Inactive (stand-by mode) V_{DD} = 6V		0.25 1.0	0.5 2 2	mA mA µA
f_{OSC}	Oscill. Frequency	V_{DD} = 2 to 6.5V (cer resonator)	350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N						
V_{IL}	Input Voltage Low	V_{DD} = 2 to 6.5V			0.3 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 2 to 6.5V	0.7 x V_{DD}			V
- I_I	Input Current	V_{DD} = 2V, V_I = 0V V_{DD} = 6.5V, V_I = 0V	10 100		100 600	µA µA
I_I	Input Leakage Current	V_{DD} = 6.5V, V_I = V_{DD}			1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N						
V_{OL}	Output Voltage "ON"	V_{DD} = 2V, I_O = 0.1mA V_{DD} = 6.5V, I_O = 1mA			0.3 0.6	V V
I_O	Output Current "OFF"	V_{DD} = 6.5V, V_O = 11V			10	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Input Voltage High		0.7 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 2V, V_{OH} = 0.8V V_{DD} = 6.5V, V_{OH} = 5V	60 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 2V, V_{OL} = 0.4V V_{DD} = 6.5V, V_{OL} = 0.4V			0.6 0.6	mA mA
t_{OH}	Pulse Length	V_{DD} = 6.5V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 2V V_{DD} = 6.5V, OSC1 at V_{DD}	 5		5 7	µA µA
V_{OH}	Output Voltage high	V_{DD} = 6.5V, - I_{OL} = 0.1mA	V_{DD} - 0.8			V
V_{OL}	Output Voltage Low	V_{DD} = 6.5V, I_{OH} = 0.1mA			0.7	V

Figure 1 : Typical Application.

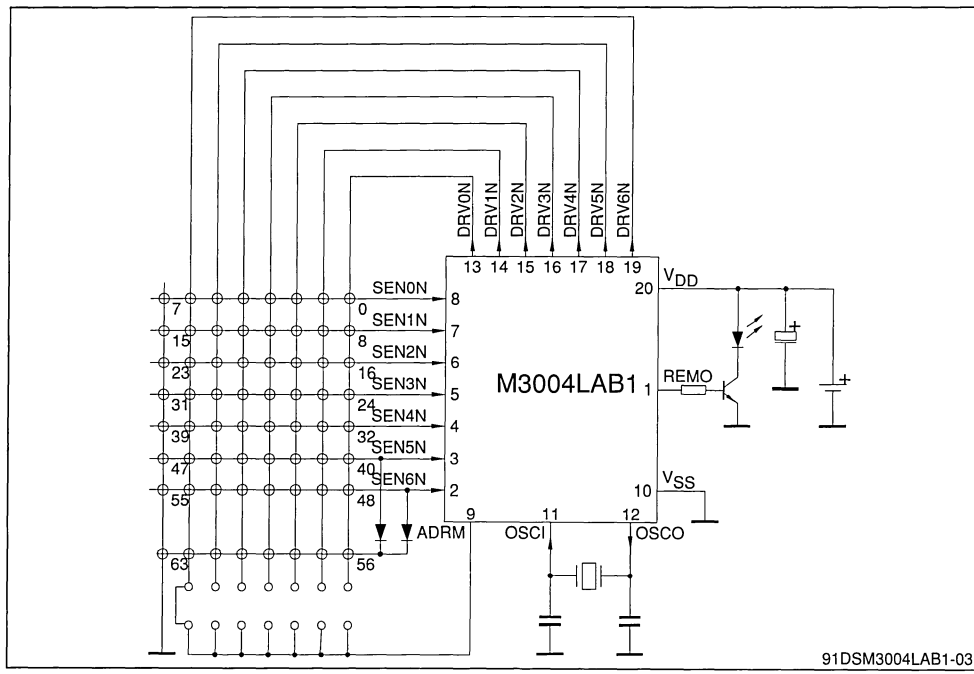


Figure 2 : Data Format of REMO Output; REF = Reference Time; T0 and T1 = Toggle bits; S0, S1 and S2 = System address; A, B, C, D, E and F = Command bits.
(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed)
(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

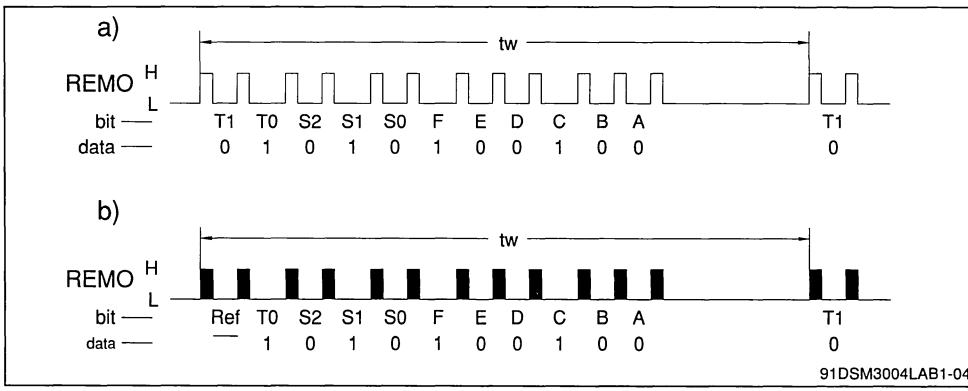


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse { $t_{PW} = (5 \times t_M) + t_{MH}$)}.

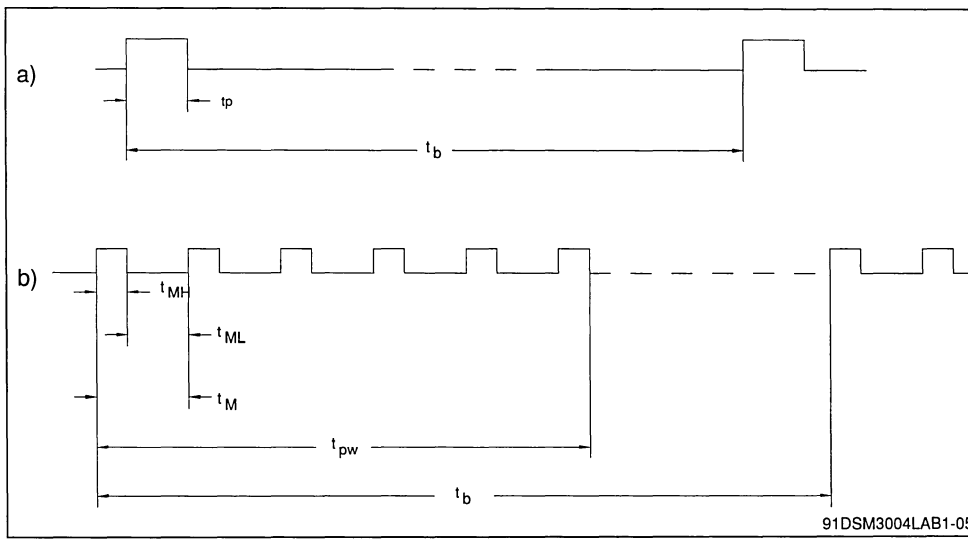


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
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Minimum release time : t_{REL} = T_O.

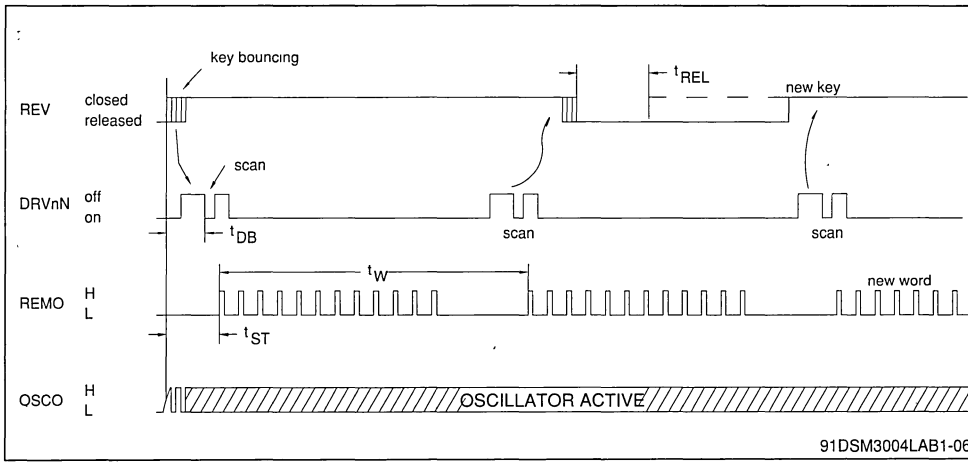
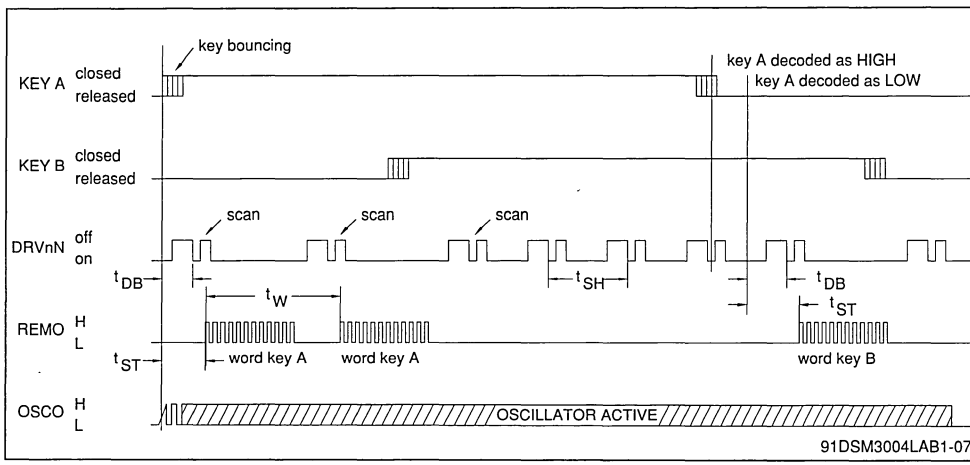
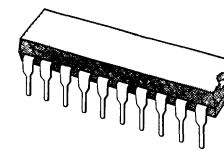


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.



REMOTE CONTROL TRANSMITTER

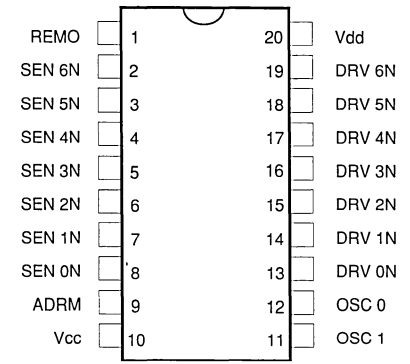
- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (– I_{OH} = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 4 TO 11V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

ORDER CODE : M3005AB1

PIN CONNECTIONS



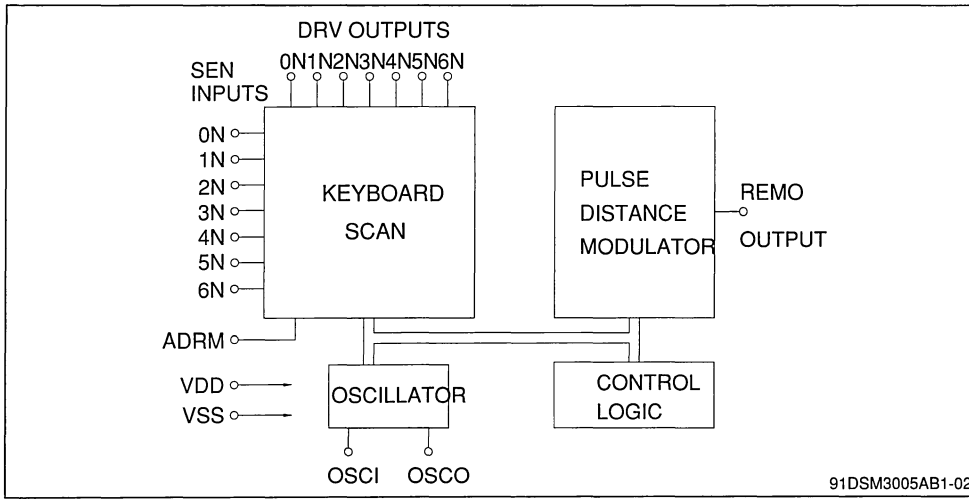
91DSM3005AB1-01

DESCRIPTION

The M3005AB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3005AB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmision.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.
In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function is an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.
The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1ms, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT / OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively.
Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.
In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.
In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.
There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.
The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing.

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_W (ms)
Flashed	2.53	8.8	-	121
Modulated	2.53	-	tosc	121

	Flash Mode	Carrier Mode	
fosc	455kHz	600kHz	
t_P	4 x tosc		Flashed Pulse Width
t_M		tosc	Modulation Period
N		8*	Number of Modulation Pulses
T_O	1152 x tosc	1536 x tOSC	Basic Unit of Pulse Distance
t_W	55296 x tosc	73728 x tOSC	Word Distance

The following number of pulses may be selected by Metal option : N = 8, 12, 16

Note : The different dividing ratio for T_O and t_W between flash mode and carrier mode is obtained by changing the modulo of a particular divider from divide by 3 during flash mode to divide by 4 during carrier mode This allows the use of a 600kHz ceramic resonator during carrier mode to obtain a better noise immunity for the receiver without a significant change in T_O and t_W. For first samples, the correct divider ration is obtained by a metal mask option For final parts, this is automatically done together with the selection of flash-/carrier mode.

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O

Table 3 : Transmission Mode and Sub-system Adress Selection.

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	O						
A	2	0	0	1	X	O					
S	3	0	1	0	X	X	O				
H	4	0	1	1	X	X	X	O			
E	5	1	0	0	X	X	X	X	O		
D	6	1	0	1	X	X	X	X	X	O	
M											
O	0	1	1	1							O
D	1	0	0	0	O						O
U	2	0	0	1	X	O					O
L	3	0	1	0	X	X	O				O
A	4	0	1	1	X	X	X	O			O
T	5	1	0	0	X	X	X	X	O		O
E	6	1	0	1	X	X	X	X	X	O	O
D											

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
V_{SS}	SEN1N	0	0	1	1	1	1	8 to 15
V_{SS}	SEN2N	0	1	0	1	1	1	16 to 23
V_{SS}	SEN3N	0	1	1	1	1	1	24 to 31
V_{SS}	SEN4N	1	0	0	1	1	1	32 to 39
V_{SS}	SEN5N	1	0	1	1	1	1	40 to 47
V_{SS}	SEN6N	1	1	0	1	1	1	48 to 55
V_{SS}	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 12	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 150	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C		4		11	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz	V_{DD} = 6V		0.8	1.5	mA
		REMO,Output unload	V_{DD} = 9V		1.5	3	mA
		• Inactive (stand-by mode)	V_{DD} = 6V			2	µA
			V_{DD} = 9V			2	µA
f_{OSC}	Oscill. Frequency	V_{DD} = 4 to 11V (cer resonator)		350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N							
V_{IL}	Input Voltage Low	V_{DD} = 4 to 11V				0.2 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 4 to 11V		0.8 x V_{DD}			V
- I_I	Input Current	V_{DD} = 4V, V_I = 0V		25		250	µA
		V_{DD} = 11V, V_I = 0V		75		750	µA
I_I	Input Leakage Current	V_{DD} = 11V, V_I = VDD				1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N							
V_{OL}	Output Voltage "ON"	V_{DD} = 4V, I_O = 0.1mA				0.3	V
		V_{DD} = 11V, I_O = 1mA				0.5	V
I_O	Output Current "OFF"	V_{DD} = 11V, V_O = 11V				10	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.2 x V_{DD}	V
V_{IH}	Input Voltage High		0.8 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 6V, V_{OH} = 3V V_{DD} = 9V, V_{OH} = 6V	80 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 6V, V_{OL} = 0.2V V_{DD} = 9V, V_{OL} = 0.1V			0.6 0.6	mA mA
t_{MH}/t_{OSC}	Pulse Duty Cycle	During Carrier Mode	0.4	0.5	0.6	
t_{OH}	Pulse Length	V_{DD} = 6V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 6V, OSC1 at V_{DD}	0.8		2.7	µA
V_{OH}	Output Voltage high	V_{DD} = 6V, - I_{OL} = 0.1mA			V_{DD} - 0.6	V
V_{OL}	Output Voltage Low	V_{DD} = 6V, I_{OH} = 0.1mA			0.6	V

Figure 1 : Typical Application.

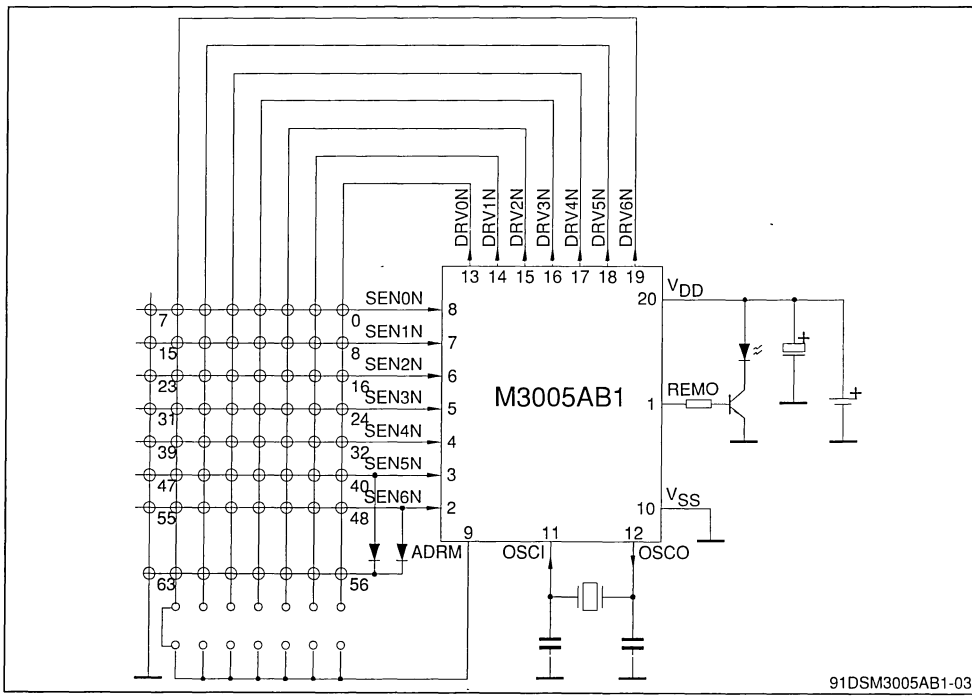


Figure 2 : Data Format of REMO Output

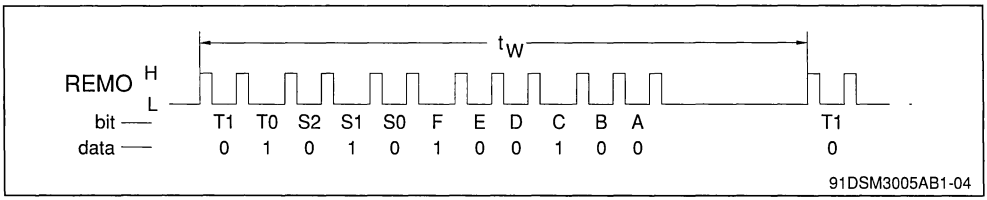


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse

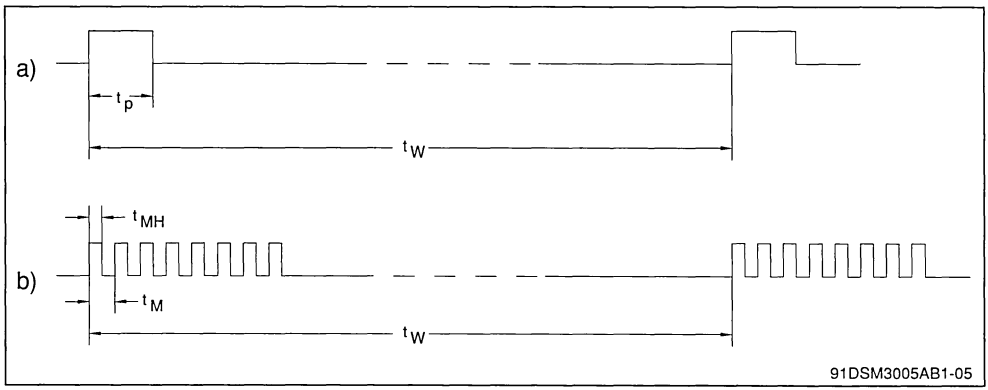


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

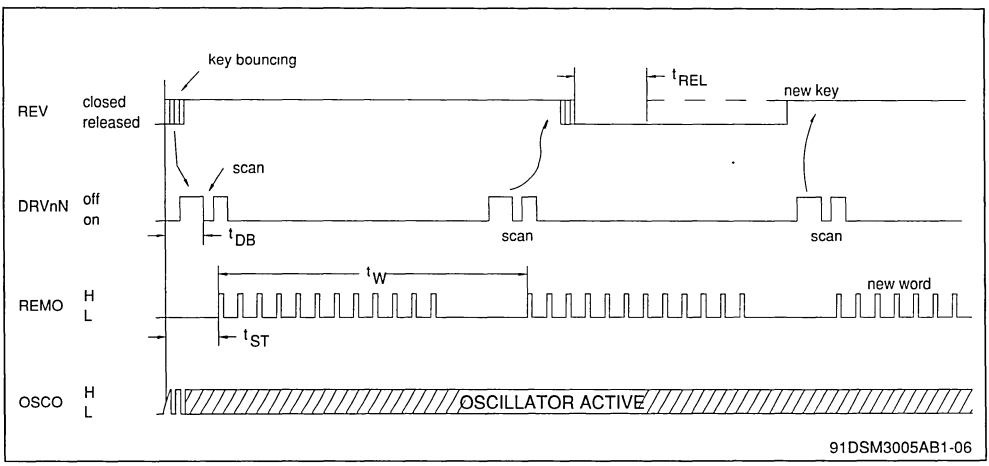
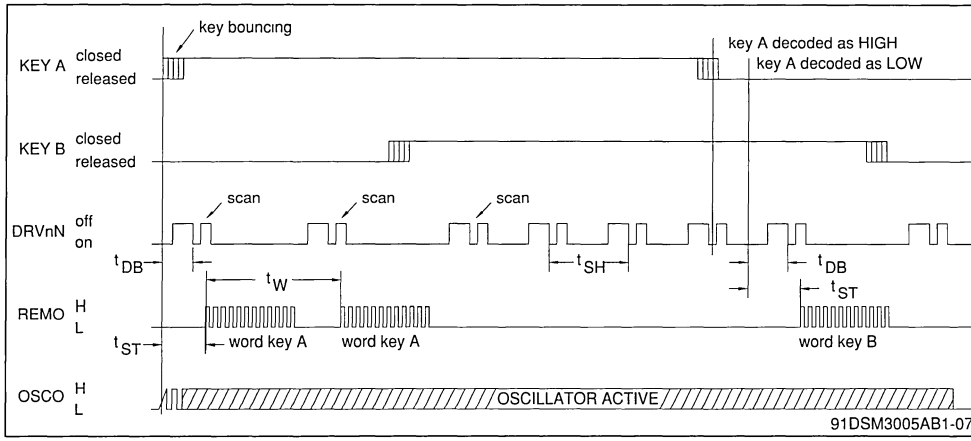


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.

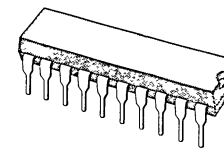


SGS-THOMSON MICROELECTRONICS

M3005LAB1

REMOTE CONTROL TRANSMITTER

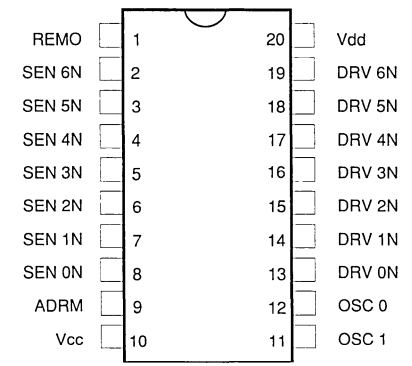
- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (– I_{OH} = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

ORDER CODE : M3005LAB1

PIN CONNECTIONS

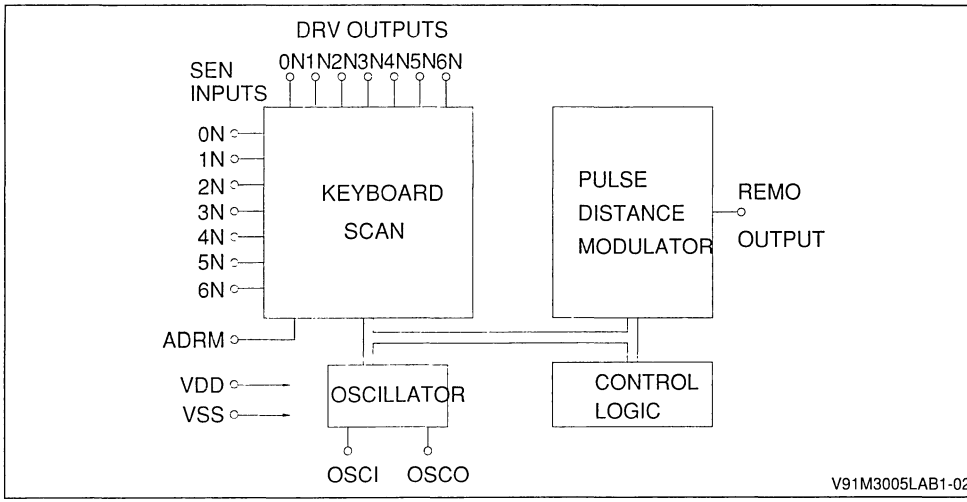


91DS3005LAB1-01

DESCRIPTION

The M3005LAB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.
The M3005LAB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



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F	0	1	1	1							
L	1	0	0	0	O						
A	2	0	0	1	X	O					
S	3	0	1	0	X	X	O				
H	4	0	1	1	X	X	X	O			
E	5	1	0	0	X	X	X	X	O		
D	6	1	0	1	X	X	X	X	X	O	
M											
O	0	1	1	1							O
D	1	0	0	0	O						O
U	2	0	0	1	X	O					O
L	3	0	1	0	X	X	O				O
A	4	0	1	1	X	X	X	O			O
T	5	1	0	0	X	X	X	X	O		O
E	6	1	0	1	X	X	X	X	X	O	O
D											

O = connected to ADRM
blank = not connected to ADRM
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Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
V_{SS}	SEN1N	0	0	1	1	1	1	8 to 15
V_{SS}	SEN2N	0	1	0	1	1	1	16 to 23
V_{SS}	SEN3N	0	1	1	1	1	1	24 to 31
V_{SS}	SEN4N	1	0	0	1	1	1	32 to 39
V_{SS}	SEN5N	1	0	1	1	1	1	40 to 47
V_{SS}	SEN6N	1	1	0	1	1	1	48 to 55
V_{SS}	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 7	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 150	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C	2		6.5	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz V_{DD} = 3V REMO,Output unload V_{DD} = 6V • Inactive (stand-by mode) V_{DD} = 6V		0.25 1.0	0.5 2 2	mA mA µA
f_{OSC}	Oscill. Frequency	V_{DD} = 2 to 6.5V (cer resonator)	350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N						
V_{IL}	Input Voltage Low	V_{DD} = 2 to 6.5V			0.3 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 2 to 6.5V	0.7 x V_{DD}			V
- I_I	Input Current	V_{DD} = 2V, V_I = 0V V_{DD} = 6.5V, V_I = 0V	10 100		100 600	µA µA
I_I	Input Leakage Current	V_{DD} = 6.5V, V_I = V_{DD}			1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N						
V_{OL}	Output Voltage "ON"	V_{DD} = 2V, I_O = 0.25mA V_{DD} = 6.5V, I_O = 2.5mA			0.3 0.6	V V
I_O	Output Current "OFF"	V_{DD} = 6.5V, V_O = 11V			10	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Input Voltage High		0.7 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 2V, V_{OH} = 0.8V V_{DD} = 6.5V, V_{OH} = 5V	60 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 2V, V_{OL} = 0.4V V_{DD} = 6.5V, V_{OL} = 0.4V			0.6 0.6	mA mA
t_{MH}/t_{OSC}	Pulse Duty Cycle	During Carrier Mode	0.4	0.5	0.6	
t_{OH}	Pulse Length	V_{DD} = 6.5V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 2V V_{DD} = 6.5V, OSC1 at V_{DD}	 5		5 7	µA µA
V_{OH}	Output Voltage high	V_{DD} = 6.5V, - I_{OL} = 0.1mA	V_{DD} - 0.8			V
V_{OL}	Output Voltage Low	V_{DD} = 6.5V, I_{OH} = 0.1mA			0.7	V

Figure 1 : Typical Application.

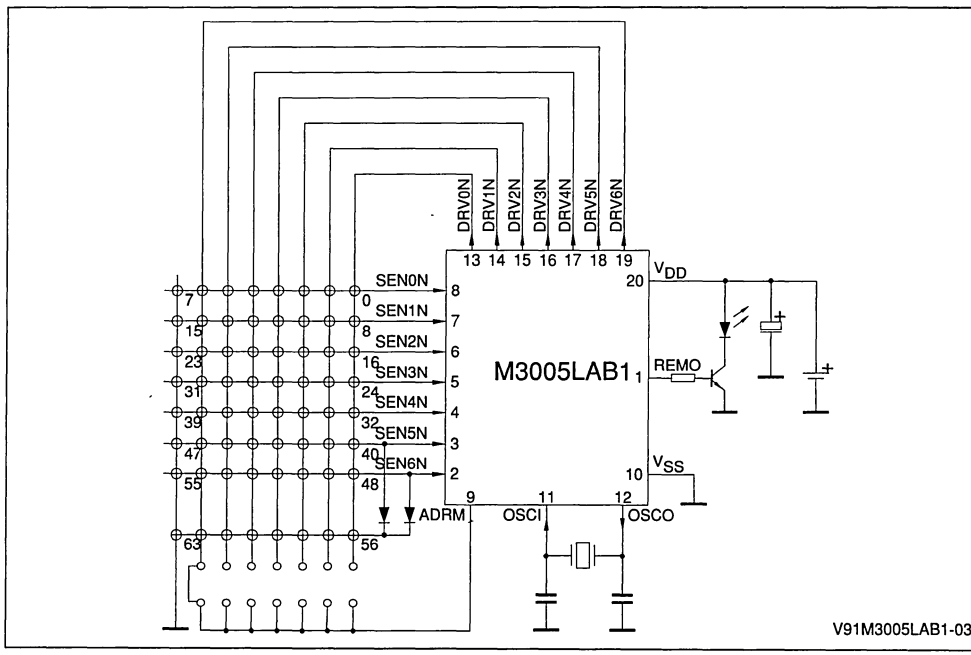


Figure 2 : Data Format of REMO Output

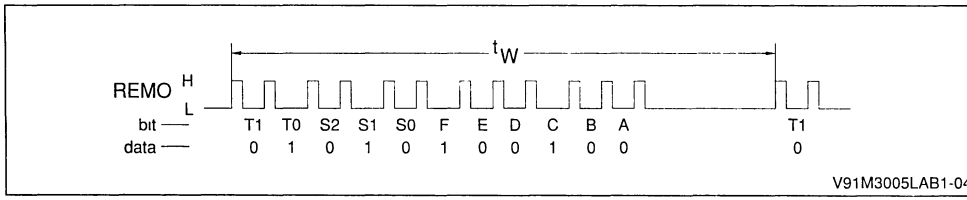


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse

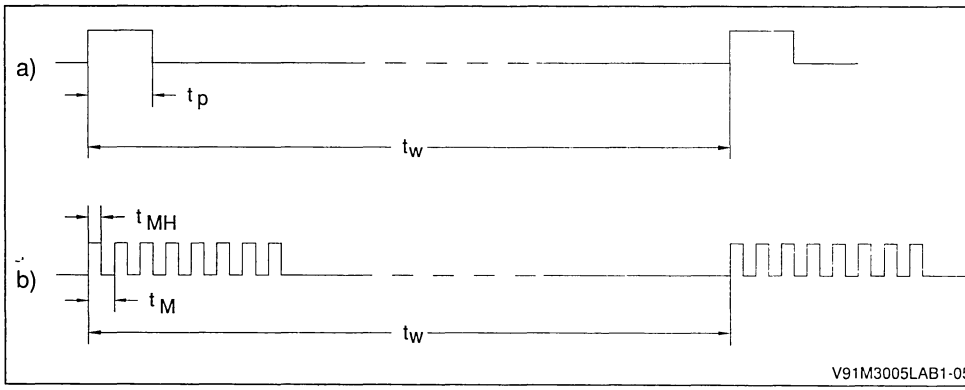


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

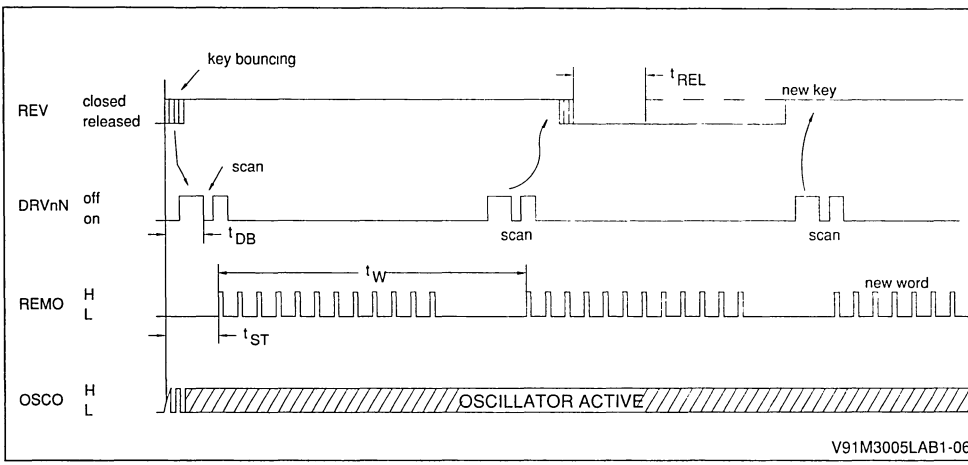
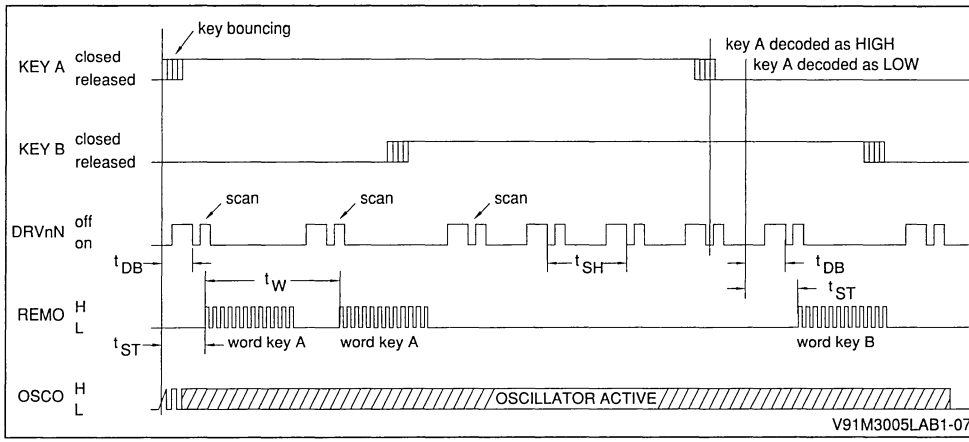


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.



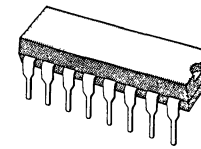
SGS-THOMSON MICROELECTRONICS

M3006LAB1

REMOTE CONTROL TRANSMITTER

ADVANCE DATA

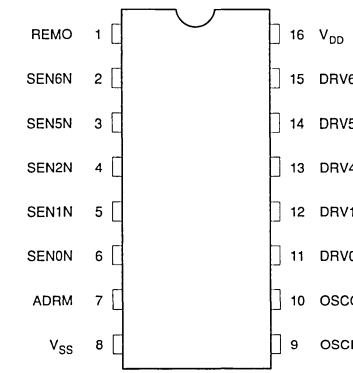
- FLASHED OR MODULATED TRANSMISSION
- 5 SUB-SYSTEM ADDRESSES
- UP TO 36 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V ($-I_{OH}$ = 120mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)
- ENCAPSULATION : 16-LEAD PLASTIC DIL



DIP16
(Plastic Package)

ORDER CODE : M3006LAB1

PIN CONNECTIONS



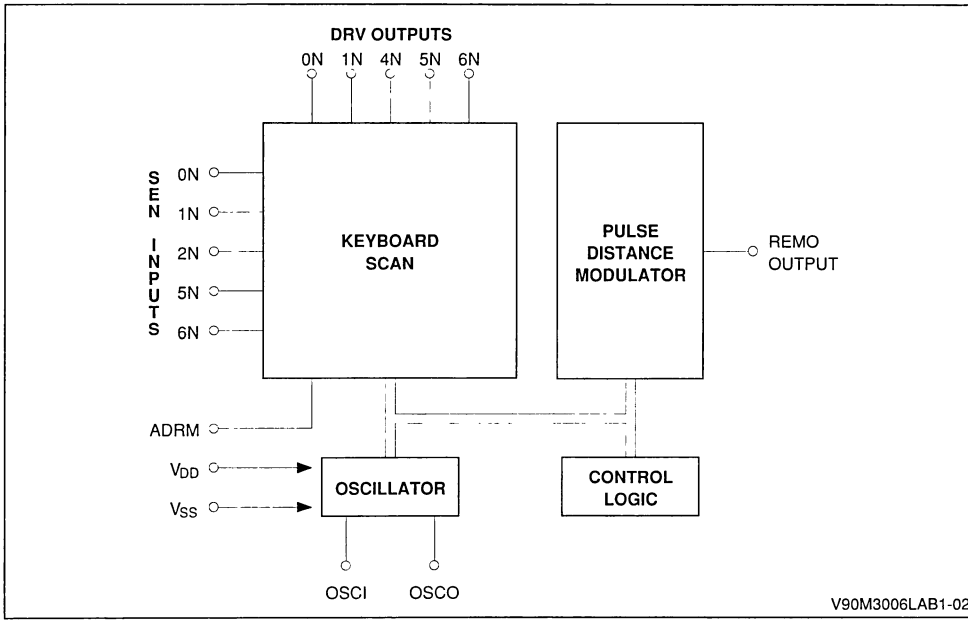
V90M3006LAB1-01

DESCRIPTION

The M3006LAB1 transmitter IC is designed for infrared remote control systems. It has a total of 180 commands which are divided into 5 sub-system groups with 36 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.
The M3006LAB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).
The transmitter keyboard is arranged as a scanned matrix. Tne matrix consists of 5 driver outputs and 5 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 5 sense inputs (SEN0N to SEN6N) enable the generation of 30 command codes. With 2 external diodes all 36 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRVON to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of five sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.
The ADRM input has switched pull-up and pull-down loads. In the stand-by mode, only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.
The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if drivers DRV1N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV4N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 5. A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1msec, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT/OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively).

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 5, 11, 17, 23, 29 and 35) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 30 to 35).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing.

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_{ML} (µs)	t_{MH} (µs)	t_W (ms)
Flashed	2.53	8.8	-	-	-	121
Modulated	2.53	-	26.4	17.6	8.8	121

f_{OSC}	455kHz	t_{OSC} = 2.2µs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period LOW
t_{MH}	4 x t_{OSC}	Modulation Period HIGH
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	Word Distance

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O
Reference Time	3 x T_O

Table 3 : Transmission Mode and Sub-system Adress Selection.
The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =				
	#	S2	S1	S0	0	1	4	5	6
FLASHED	0	1	1	1					
	1	0	0	0	O				
	2	0	0	1	X	O			
	5	1	0	0	X	X	O		
	6	1	0	1	X	X	X	O	
MODULATED	0	1	1	1					O
	1	0	0	0	O				O
	2	0	0	1	X	O			O
	5	1	0	0	X	X	O		O
	6	1	0	1	X	X	X	O	O

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV4N	SEN0N	0	0	0	1	0	0	2
DRV5N	SEN0N	0	0	0	1	0	1	3
DRV6N	SEN0N	0	0	0	1	1	0	4
V_{SS}	SEN0N	0	0	0	1	1	1	5
V_{SS}	SEN1N	0	0	1	1	1	1	6 to 11
V_{SS}	SEN2N	0	1	0	1	1	1	12 to 17
V_{SS}	SEN5N	1	0	1	1	1	1	18 to 23
V_{SS}	SEN6N	1	1	0	1	1	1	24 to 29
V_{SS}	SEN5N and SEN6N	1	1	1	1	1	1	30 to 35

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 7	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 125	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C	2		6.5	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz V_{DD} = 3V REMO,Output unload V_{DD} = 6V • Inactive (stand-by mode) V_{DD} = 6V		0.25 1.0	 4	mA mA µA
f_{OSC}	Oscill. Frequency	V_{DD} = 2 to 6.5V (cer resonator)	350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N						
V_{IL}	Input Voltage Low	V_{DD} = 2 to 6.5V			0.3 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 2 to 6.5V	0.7 x V_{DD}			V
- I_I	Input Current	V_{DD} = 2V, V_I = 0V V_{DD} = 6.5V, V_I = 0V	10 100		100 600	µA µA
I_I	Input Leakage Current	V_{DD} = 6.5V, V_I = VDD			1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N						
V_{OL}	Output Voltage "ON"	V_{DD} = 2V, I_O = 0.1mA V_{DD} = 6.5V, I_O = 1mA			0.3 0.6	V V
I_O	Output Current "OFF"	V_{DD} = 6.5V, V_O = 6.5V			10	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
KEYBOARD MATRIX - Control Input ADRM						
V_{IL}	Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Input Voltage High		0.7 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
KEYBOARD MATRIX - Data Output REMO						
V_{OH}	Output Voltage High	V_{DD} = 2V, $-I_{OH}$ = 60mA V_{DD} = 6.5V, $-I_{OH}$ = 60mA	0.8 5.0		 	V V
V_{OL}	Output Voltage Low	V_{DD} = 2V, I_{OL} = 0.3mA V_{DD} = 6.5V, I_{OL} = 0.3mA			0.4 0.4	V V
t_{OH}	Pulse Length	V_{DD} = 6.5V, Oscill. Stopped			1	ms
KEYBOARD MATRIX -Oscillator						
I_I	Input Current	V_{DD} = 2V, OSC1 at V_{DD} V_{DD} = 6.5V, OSC1 at V_{DD}	 5.0		5.0 7.0	µA µA
V_{OH}	Output Voltage high	V_{DD} = 6.5V, - I_{OL} = 0.1mA	V_{DD} - 0.8			V
V_{OL}	Output Voltage Low	V_{DD} = 6.5V, I_{OH} = 0.1mA			0.7	V

Figure 1 : Typical Application.

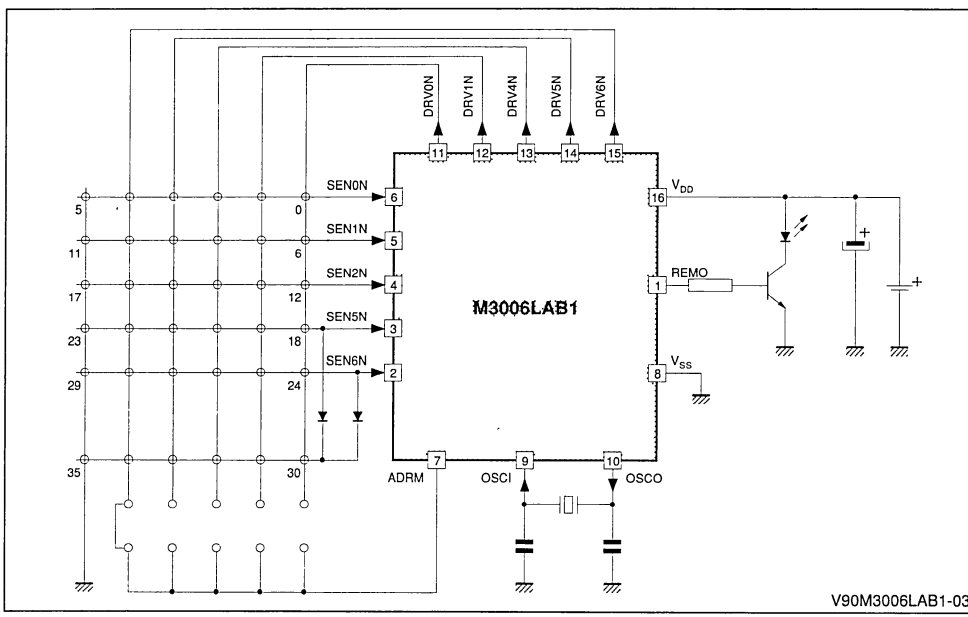


Figure 2 : Data Format of REMO Output; REF = Reference Time; T0 and T1 = Toggle bits; S0, S1 and S2 = System address; A, B, C, D, E and F = Command bits.
(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed)
(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

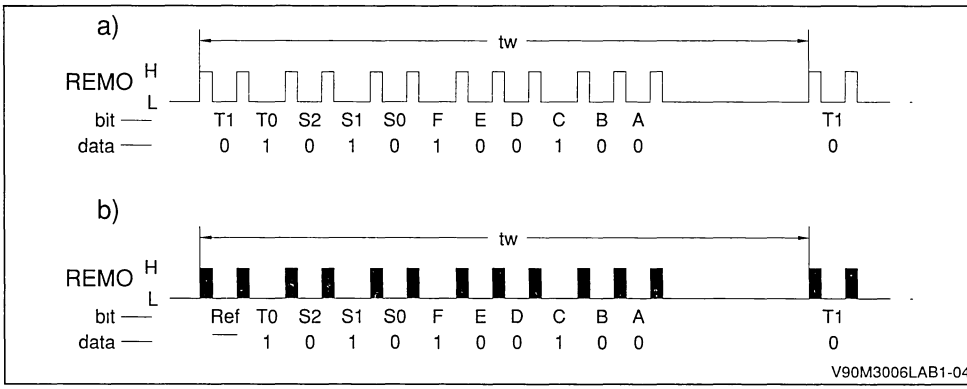


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse { $t_{PW} = (5 \times t_M) + t_{MH}$)}.

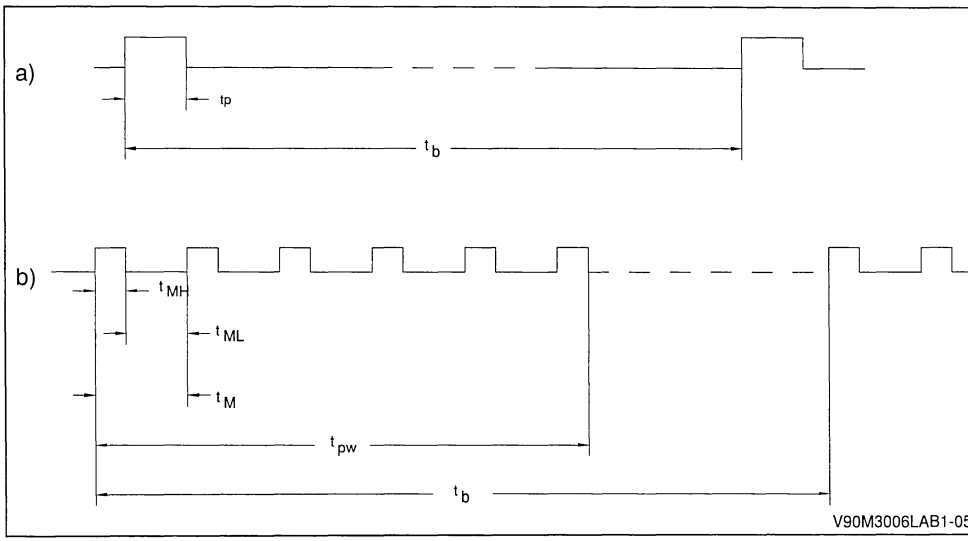


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

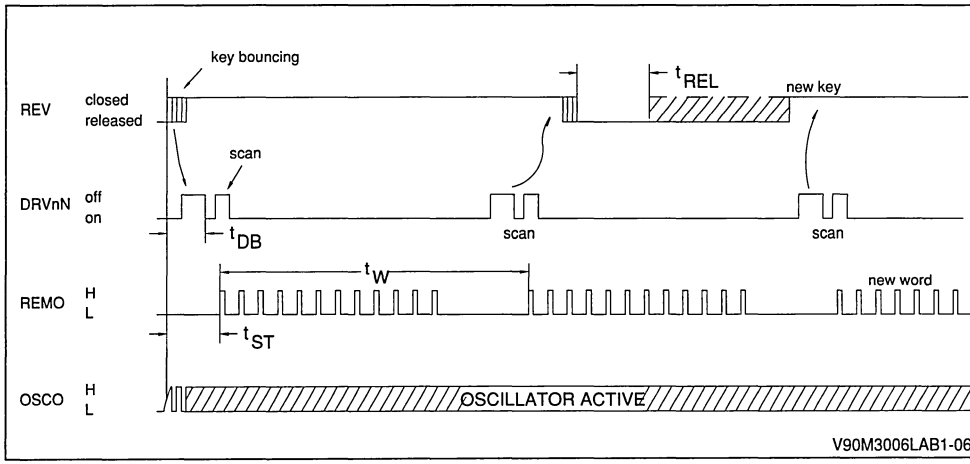
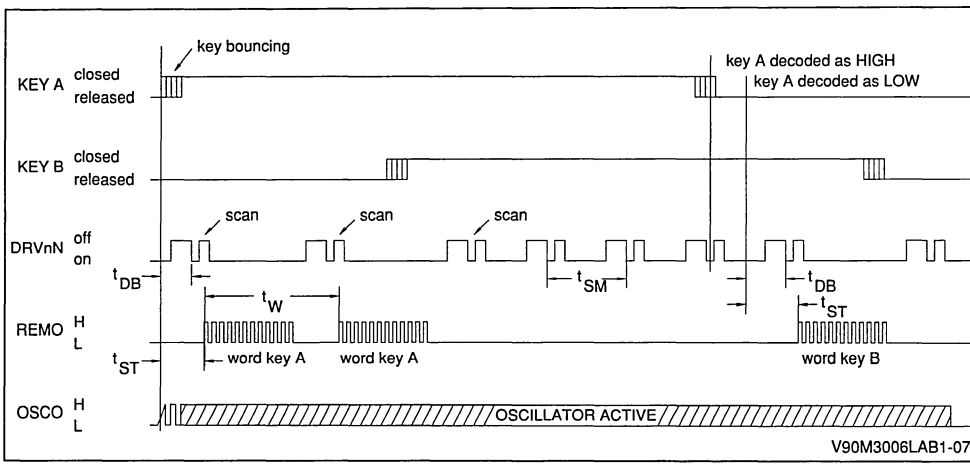
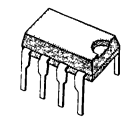


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.



CLOCK/CALENDAR WITH SERIAL I^2C BUS

- CLOCK/CALENDAR WITH SERIAL I^2C BUS
- 32kHZ QUARTZ TIMEBASE
- COUNTERS FOR SEC ; MIN ; HRS ; DAY ; MONTH OR SEC ; MIN ; HRS ; DAY OF WEEK
- EXTREMELY LOW POWER CONSUMPTION IN STANDBY OPERATION (TYP. 5µA)
- 8 PIN DIP PACKAGE
- INTEGRATED POWER FAIL DETECTION AND POWER-ON RESET
- PULSE OUTPUT FOR SECONDS
- CMOS PROCESS



DIP8
(Plastic Package)

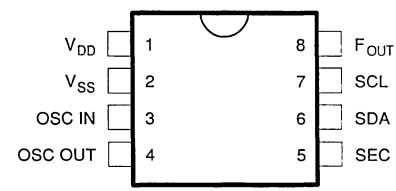
ORDER CODE : M8716A B1

DESCRIPTION

The integrated circuit M8716B contains a digital clock with a 32kHz quartz oscillator and a serial bus interface (I^2C Bus). The circuit is programmable to count seconds, minutes, hours, days and month or seconds, minutes, hours and day of the week.
This circuit is intended for use within a microcomputer system.

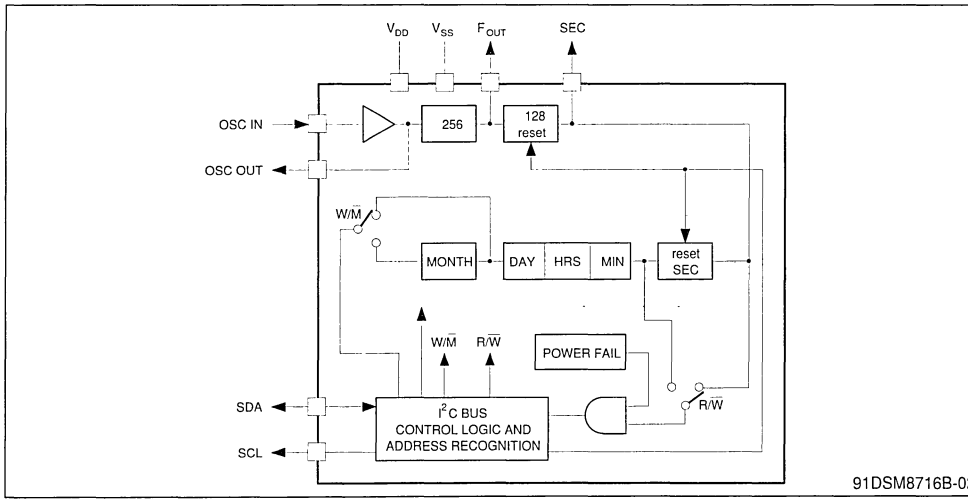
The M8716B is available in a 8 lead dual in-line plastic package.

PIN CONNECTION (top view)



91DSM8716B-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}-V_{SS}	Supply Voltage	– 0.3 to + 10	V
V_I/V_O	Input Voltage, Output Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
P_D	Total Package Power Dissipation	300	mW
T_{stg}	Storage Temperature	– 55 to + 125	°C
T_A	Operating Temperature	0 to + 70	°C

TAB-01

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS

(T_A = 25°C : V_{DD} = 5V ; F_{OSC} = 32.768kHz if not otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_{DD}	Supply Current				1	mA
V_{BAT}	Supply Voltage (standby operation)	No Data Transfer	2.0	2.4		V
I_{BAT}	Supply Current (standby operation)	Test Circuit V_{BAT} = 2.4V		5	15	µA
I_{IN}	Input Current SDA ; SCL	V_{IN} = V_{DD}			5	µA
		V_{IN} = V_{SS}			– 5	µA
I_{OUT}	Output Current SDA	V_{OL} = 0.4V	4			mA
I_{OUT}	Output Current F_{OUT}, SEC	V_{OUT} = 1V	0.1			mA
		V_{OUT} = 4V	– 0.1			mA
C_{OUT}	Oscillator Output-capacitance		16	20	24	pF

TAB-02

GENERAL DESCRIPTION

The integrated circuit M8716B contains a digital clock counting seconds, minutes, hours, days and months or seconds, minutes, hours and days of the week as an option. A 32.768kHz quartz oscillator serves as time-base. This circuit is intended for use within a microcomputer system.

Writing (time setting) and reading of the counters is done via a serial interface (I^2C Bus). The micro-computer is used for controlling the data transfer and for generating the signals to drive a (7 segment) display. If a data transfer takes place between the M8716B and the microprocessor, a 5V supply voltage has to be provided. During standby the circuit is supplied by two NiCd-cells at a very low power consumption.

FUNCTIONAL DESCRIPTION

DIVIDERS AND COUNTERS

The oscillator frequency of 32.768kHz is first divided by 256 and then again by 128. The resulting output frequency of 1Hz then serves as clock pulse for the time counters.

The content of the counters for sec, min, hr, day and month of sec, min, hr, and day of week can be read or modified (written) via the I^2C Bus interface. During a "write" cycle only the content of the counters starting from the minutes counter is modified : the seconds counter and the seconds divider block are reset to zero.

Selection between "calendar" operation (display of day and month) and "day of week" operation (display of day of week 1 to 7) is done as follows :

If the second bit in the first data byte is "1" during a "write" operation, the counters are set for the mode "day of week".

If this bit remains at "0" during a "write" operation the calendar mode is selected. In this case, carry of the "day" counter is performed automatically at positions 28, 30 or 31, depending on the month. In case of a leap year the day 29 (of February) can be set by a "write" operation.

In this case, carry takes place on 3-1 (March 1st).

I^2C BUS INTERFACE GENERAL DESCRIPTION

Data transfer from the circuit M8716B to the microcomputer (reading) and vice versa (writing) takes place via the two lines SDA and SCL. Address and data are transmitted on SDA while at the same time clock pulses have to be provided on SCL for synchronization by the microcomputer.

I^2C BUS INTERFACE ADDRESSING

(see fig. 1...3)

A data transfer (reading or writing) is initiated by a start condition ("1" – > "0" transition on SDA while SCL remains at "1") and a subsequent address byte. By assigning a unique address to each circuit, several circuits may be connected to the I^2C Bus without interfering each other.

If the M8716B recognizes an address transmitted on the bus as its own address, the data transfer starts. The least significant bit of the address word controls the direction of data transfer (R/$\overline{W}$-control). If it is set to "0", data is transferred from the microcomputer to the circuit, i.e. the content of the time counters is modified. If it is set to "1" the time information is read out by the microcomputer. A data transmission between the microprocessor and M8716B must always be completed otherwise the clock content may be lost. This means that the "master" can't use the possibility to stop the transmission after a certain byte by not sending the acknowledge bit.

Even 2f M8716B can work at the frequency four DC UP to 100kHz, it is tested at a frequency of 30kHz. If a carry of the time counter should take place during a data transfer, the carry will be stored and made after the data transfer. As only one carry can be stored, the whole data transfer must not take a time longer than one second.

SYNCHRONIZATION

For easy of synchronization with an external time reference in case of small deviations ($< \pm$ 30sec), only the address (with R/$\overline{W}$ = "0") has to be transmitted, followed immediately by a stop condition. No data is transmitted (see fig. 4). The second divider block (128Hz to 1Hz) and the seconds counter are reset. If the seconds counter was at position 30 ... 59, a carry to the minutes counter takes place in addition to the reset.

POWER FAIL

In case of total power fail an internal register is set to "0". This register disables the data of the watch. So in a read cycle the µP recognizes "0" of the watch content. This is a unique situation appearing only in case of a power fail. The power fail register is automatically reset by the first "write" command.

PULSE OUTPUTS F_{OUT}, SEC

The output frequency of the first divider block (128Hz) is provided on the pin F_{OUT} and facilitates adjustment of the oscillator frequency without loading (and detuning) the oscillator.

The output SEC (1Hz) may be utilized for a blinking second indication.
Both pins F_{OUT} and SEC can also be used as input during the functional test. A Low impedance (50 to 100Ω) external signal source which overrides the internal output buffer can drive the circuit at a frequency higher than the normal rate. This allows to reduce test time.

Figure 1 : Complete Timing for an Address/-read ; Resp. Address/-write Cycle.

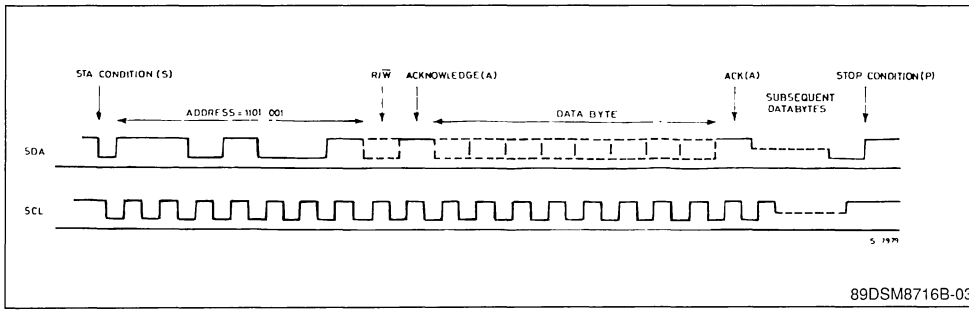


Figure 2a : Data Format for One Cycle Address/-read (with calendar).

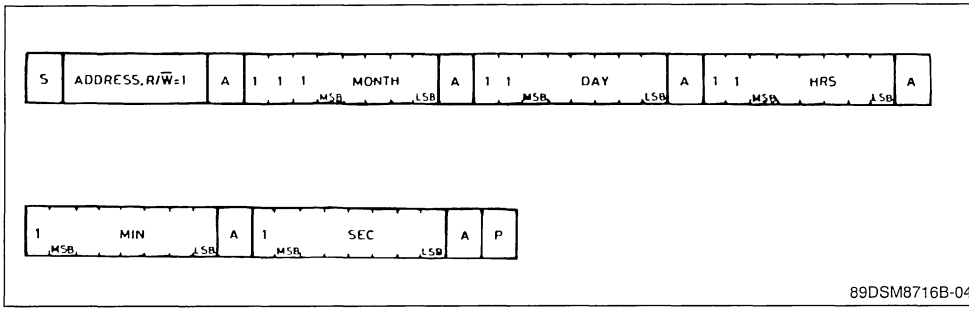


Figure 2b : Data Format for One Cycle Address/-write (with calendar).

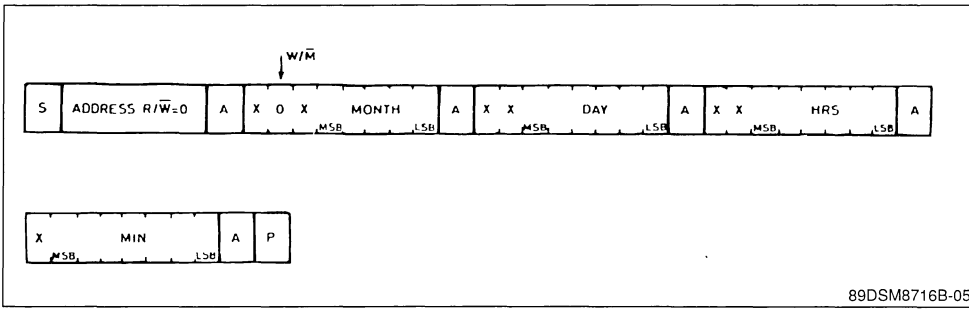


Figure 3a : Data Format for One Cycle Address/-read (with day of week indication).

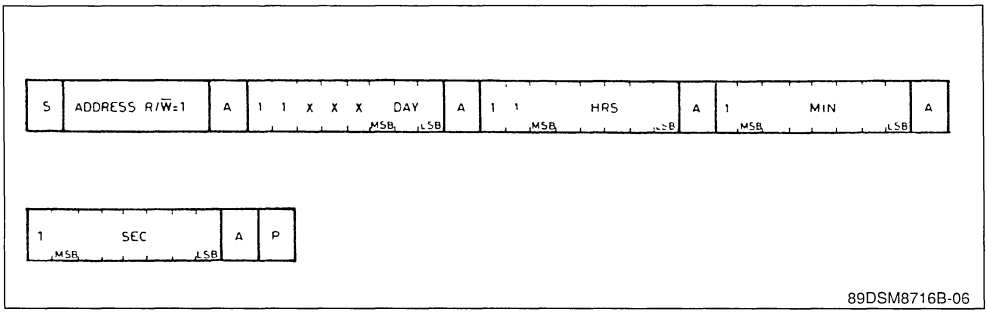


Figure 3b : Data Format for One Cycle Address/-write (with day of week indication).

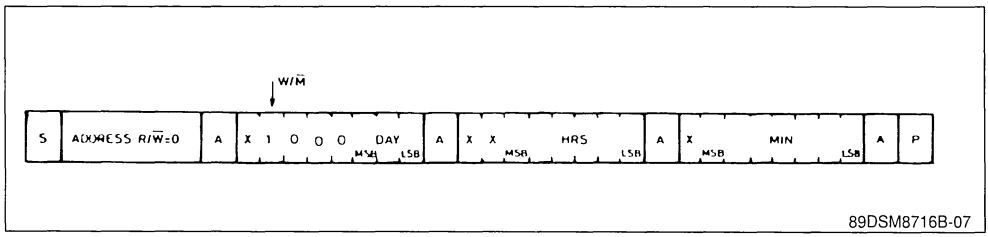


Figure 4 : Data Format for Synchronization (deviation < 30sec).

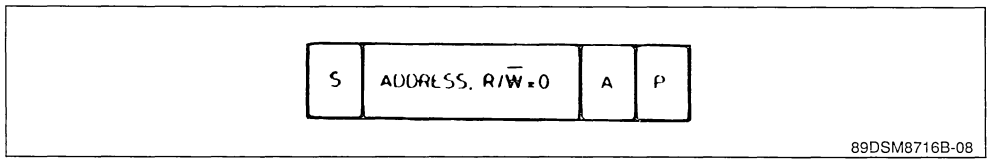


Figure 5 : Test Circuit.

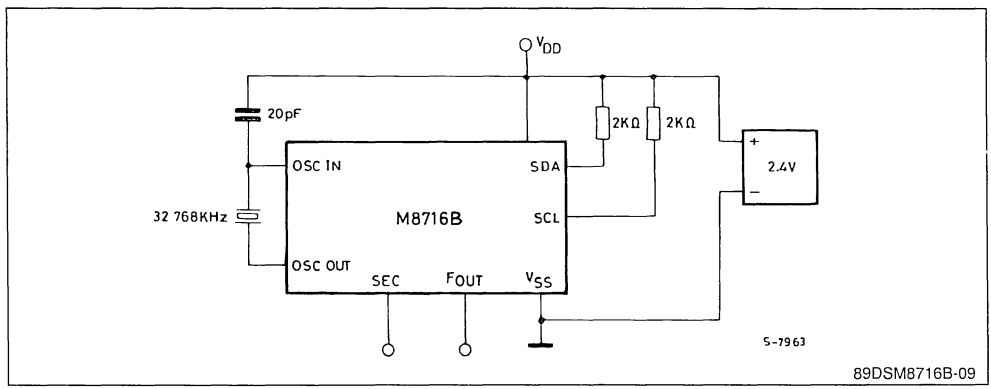
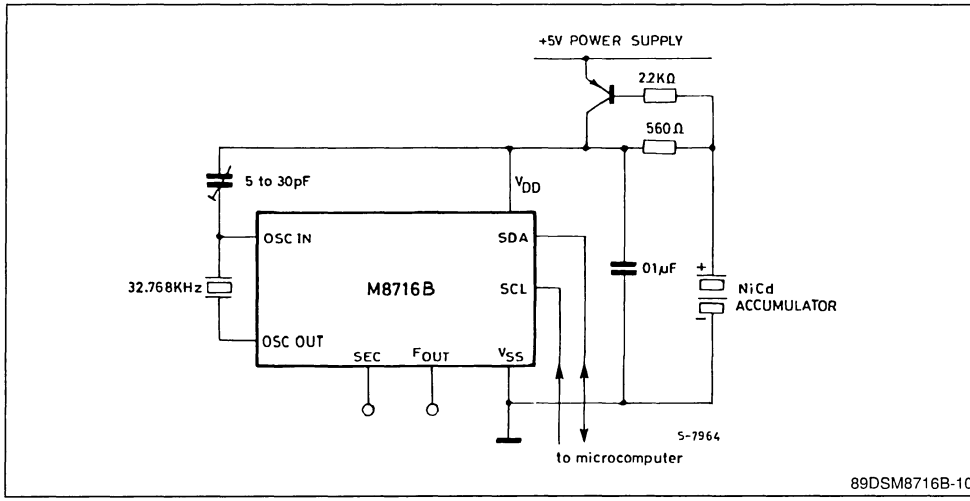
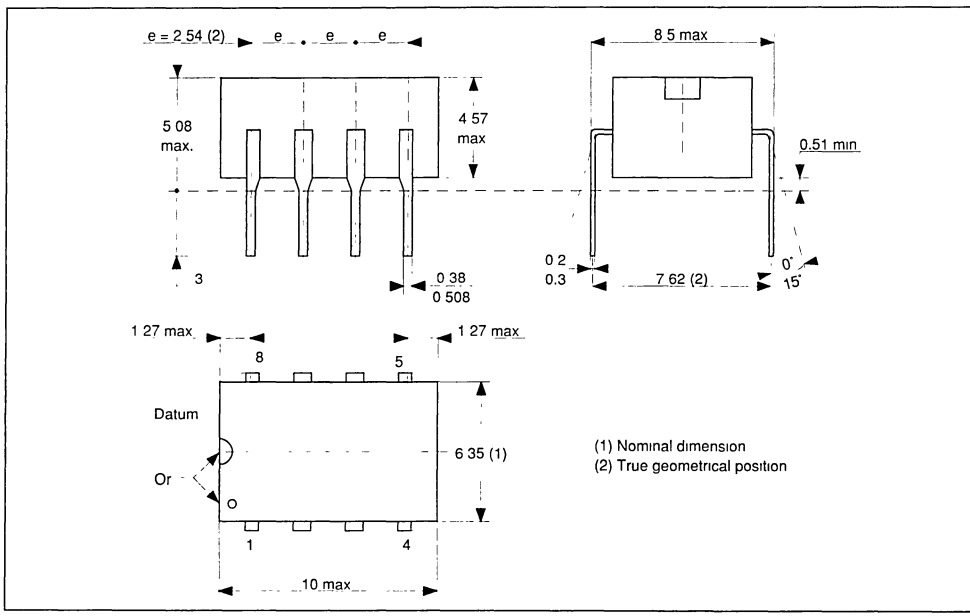


Figure 6 : Typical Application.



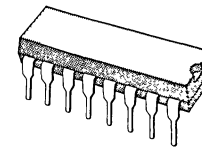
PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



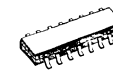
REMOTE CONTROL ENCODER/DECODER CIRCUITS

- M145026 ENCODER
- M145027/M145028 DECODERS
- MAY BE ADDRESSED IN EITHER BINARY OR TRINARY
- TRINARY ADDRESSING MAXIMIZES NUMBER OF CODES
- INTERFACES WITH RF, ULTRASONIC, OR INFRARED TRANSMISSION MEDIAS
- DOUBLE TRANSMISSIONS FOR ERROR CHECKING
- 4.5V TO 18V OPERATION
- ON-CHIP R/C OSCILLATOR, NO CRYSTAL REQUIRED
- HIGH EXTERNAL COMPONENT TOLERANCE, CAN USE 5% COMPONENTS
- STANDARD CMOS B-SERIES INPUT AND OUTPUT CHARACTERISTICS
- APPLICATIONS INCLUDE GARAGE DOOR OPENERS, REMOTE CONTROLLED TOYS, SECURITY MONITORING, ANTITHEFT SYSTEMS, LOW END DATA TRANSMISSIONS WIRE LESS TELEPHONES



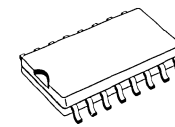
DIP16 (0.25")
(Plastic package)

ORDER CODES :
M145026B1
M145027B1
M145028 B1



SO16 Narrow (0.15")
(Plastic package)

ORDER CODE : M145026D



SO16 Large (0.3")
(Plastic package)

ORDER CODE : M145028D

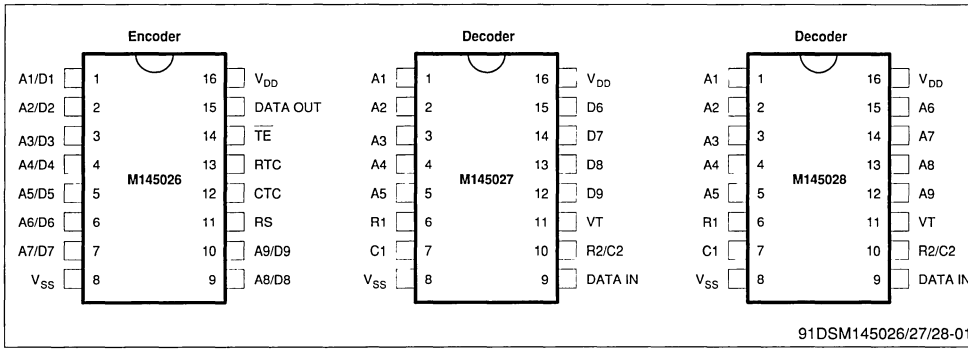
DESCRIPTION

The M145026 encodes nine bits of information and serially transmits this information upon receipt of a transmit enable, $\overline{TE}$, (active low) signal. Nine inputs may be encoded with trinary data (0,1, open) to allow 3^9 (19.683) different codes.

Two decoders are presently available. Both use the same transmitter - the M145026. The decoders will receive the 9-bit word and will interpret some of the bits as address codes and some as data. The M145027 interprets the first five transmitted bits as address and the last four bits as data. The M145028 treats all nine bits as address. If no errors are received, the M145027 outputs the four data bits when the transmitter sends address codes that match that of the receiver. A valid transmission output goes high on both decoders when they recognize an address that matches that of the decoder. Other receivers can be produced with different address/data ratios.

All the devices are available in 16 lead plastic package. The M145026 is available in SO16 plastic package (narrow) and the M145028 is available in SO16 plastic package (large).

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18	V
V_I	Input Voltage, All Inputs	– 0.5 to V_{DD} + 0.5	V
I_I	DC Current Drain Per Pin	10	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_{op}	Operating Temperature Range	– 40 to + 85	°C

TAB-01

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at thses or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_{amb} = 25 °C)

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit
t_{TLH} t_{THL}	Output Rise and Fall Time	5 10 15	– – –	100 50 40	200 100 80	ns
t_{TLH} t_{THL}	Data in Rise and Fall Time (M145027, M145028)	5 10 15	– – –	– – –	15 15 15	µs
f_{CL}	Encoder Clock Frequency	5 10 15	0 0 0	– – –	2 5 5	MHz
f_{CL}	Maximum Decoder Frequency (referenced to encoder clock) (see figure 9)	5 10 15	– – –	– – –	240 410 450	kHz
t_{WL}	$\overline{TE}$ Pulse Width	5 10 15	65 30 20	– – –	– – –	ns
	System Propagation Delay (TE to valid transmission)	–	–	182	–	Clock Cycles
	Tolerance on Timing Components (ΔRTC + ΔCTC + ΔR1 + ΔC1) (ΔR2 + ΔC2)	– –	– –	– –	± 25 ± 25	%

TAB-02

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{DD} V	– 40 °C		25 °C			+ 85 °C		Unit
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OL}	Output Voltage $V_I = V_{DD}$ or 0 "0" Level	5	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
V_{OH}	$V_I = 0$ or V_{DD} "1" Level	5	4.95	–	4.95	5	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
V_{IL}	Input Voltage (V_O = 4.5 or 0.5 V)	5	–	1.5	–	2.25	1.5	–	1.5	V
	(V_O = 0.9 or 1 V) "0" Level	10	–	3	–	4.50	3	–	3	
	(V_O = 13.5 or 1.5 V)	15	–	4	–	6.25	4	–	4	
V_{IH}	(V_O = 0.5 or 4.5 V)	5	3.5	–	3.5	2.75	–	3.5	–	V
	(V_O = 1.0 or 9 V) "1" Level	10	7	–	7	5.50	–	7	–	
	(V_O = 1.5 or 13.5 V)	15	11	–	11	8.25	–	11	–	
I_{OH}	Output Drive Current (V_{OH} = 2.5 V)	5	– 2.5	–	– 2.1	– 4.2	–	– 1.7	–	mA
	(V_{OH} = 4.6 V)	5	– 0.52	–	– 0.44	– 0.88	–	– 0.36	–	
	(V_{OH} = 9.5 V) Source	10	– 1.3	–	– 1.1	– 2.25	–	– 0.9	–	
	(V_{OH} = 13.5 V)	15	– 3.6	–	– 3	– 8.8	–	– 2.4	–	
I_{OL}	(V_{OL} = 0.4 V)	5	0.52	–	0.44	0.88	–	0.36	–	mA
	(V_{OL} = 0.5 V) Sink	10	1.3	–	1.1	2.25	–	0.9	–	
	(V_{OL} = 1.5 V)	15	3.6	–	3	8.8	–	2.4	–	
I_I	Input Current $\overline{TE}$ (M145026, pull up device)	5	–	–	3	4	7	–	–	µA
		10	–	–	16	20	26	–	–	
		15	–	–	35	45	55	–	–	
I_I	Input Current RS (M145026) Data In (M145027, M145028)	15	–	± 0.3	–	± 0.00001	± 0.3	–	± 1.0	µA
I_I	Input Current A1/D1-A9/D9 (M145026)	5	–	–	–	± 55	± 80	–	–	µA
	A1-A5 (M145027)	10	–	–	–	± 300	± 340	–	–	
	A1-A9 (M145028)	15	–	–	–	± 650	± 725	–	–	
C_I	Input Capacitance (V_I = 0)	–	–	–	–	5	7.5	–	–	pF
I_{DD}	Quiescent Current- M145026	5	–	–	–	0.0050	0.10	–	–	µA
		10	–	–	–	0.0100	0.20	–	–	
		15	–	–	–	0.0150	0.30	–	–	
I_{DD}	Quiescent Current M145027, M145028	5	–	–	–	30	50	–	–	µA
		10	–	–	–	60	100	–	–	
		15	–	–	–	90	150	–	–	
I_T	Total Supply Current M145026 (f_{CL} = 20 kHz)	5	–	–	–	100	200	–	–	µA
		10	–	–	–	200	400	–	–	
		15	–	–	–	300	600	–	–	
I_T	Total Supply Current M145027,M145028 (f_{CL} = 20 kHz)	5	–	–	–	200	400	–	–	µA
		10	–	–	–	400	800	–	–	
		15	–	–	–	600	1200	–	–	

TAB-03

OPERATING CHARACTERISTICS

M145026

The encoder will serially transmit nine bits of trinary data as defined by the state of the A1/D1-A9/D9 input pins. These pins can be in either of three states (0,1, open) allowing 3^9 = 19683 possible codes.The transmit sequence will be initiated by a low level of the $\overline{TE}$ input pin. Each time the $\overline{TE}$ input is forced low the encoder will output two identical data words. This redundant information is used by the receiver to reduce errors. If the $\overline{TE}$ input is kept low, the encoder will continuously transmit the data words. The transmitted words are self-completing (two words will be transmitted for each $\overline{TE}$ pulse).

Each transmitted data bit is encoded into two data pulses. A logic zero will be encoded as two consecutive short pulses, a logic one by two consecutive long pulses, and an open as a long pulse followed by a short pulse. The input state is determined by using a weak output device to try to force each input first low, then high. If only a high state results from the two tests, the input is assumed to be hard wired to V_{DD}. If only a low state is obtained, the input is assumed to be hard wired to V_{SS}. If both a high and a low can be forced at an input, it is assumed to be open and is encoded as such.

The transmit sequence is enabled by a logic zero on the $\overline{TE}$ input. This input has an internal pullup device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high the encoder is completely disabled, the oscillator is inhibited and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started, and an internal reset is generated to initialize the transmit sequence. Each input is then sequentially selected and a determination is made as to input logic state. This information is serially transmitted via the Data Out output pin.

M145027

The decoder will receive the serial data from the encoder, check it for errors and output data if valid. The transmitted data consisting of two identical data words is examined bit by bit as it is received. The first five bits are assumed to be address bits and must be encoded to match the address inputs at the receiver. If the address bits match, the next four (data) bits are stored and compared to the last valid data stored. if this data matches, the VT pin will go high on the 2nd rising edge of the 9th bit of the first word. Between the two data words no signal is sent for three data bit times. As the second encoded word is received, the address must again match, and if it does, the data bits are checked against the previously stored data bits. If the two words of data (four bits each) match, the data is transferred to the output data latches and will remain until new data replaces it. At the same time, the Valid Transmission output pin is brought high and will remain high until an error is received or until no input signal is received for four data bit times.

Although the address information is encoded in trinary fashion, the data information must be either a one or a zero. A trinary (open) will be decoded as a logic one.

M145028

This receiver operates in the same manner as the M145027 except that nine address bits are used and no data output is available. The Valid Transmission output is used to indicate that a valid signal has been received.

Although address information normally is encoded in trinary, the designer should be aware that, for the M145028, the ninth address bit (A9) must be either a one or a zero. This part, therefore, can accept only 2×3^8 = 13.122 different codes. A trinary (open) A9 will be interpreted as a logic 1. However if the transmitter sends a trinary (or logic 1) and the receiver address is a logic 1 (or trinary) respectively, the valid transmission output will be shortened to the R1 x C1 time constant.

DOUBLE TRANSMISSION DECODING

Although the encoder sends two words fo error checking, a decoder does not necessarily wait for two transmitted words to be received before issuing a valid transmission output. Refer to the flowcharts in Figure 7 and 8.

Figure 1 : Encoder Block Diagram M145026.

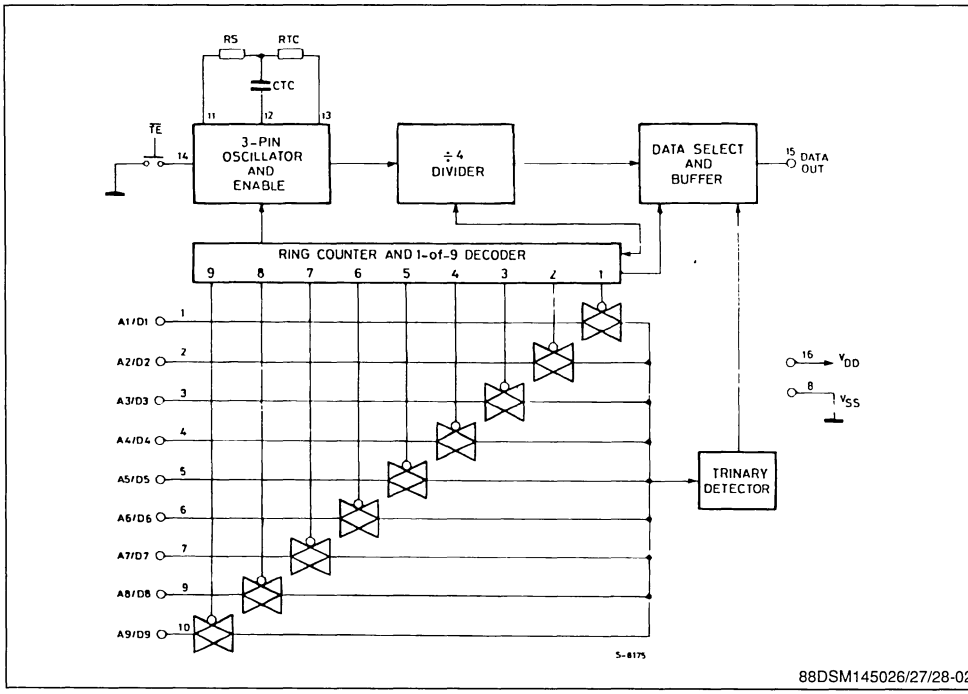


Figure 2 : Decoder Block Diagram M145027.

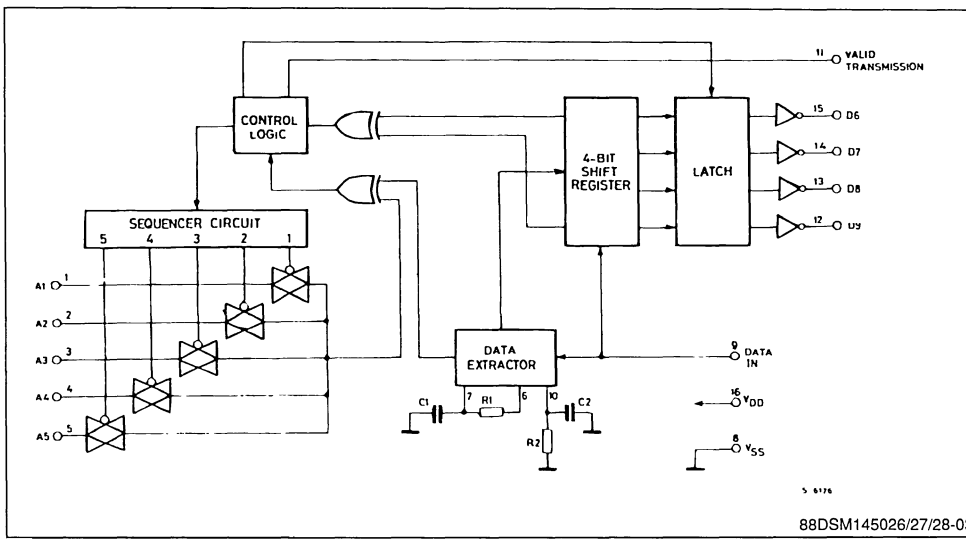
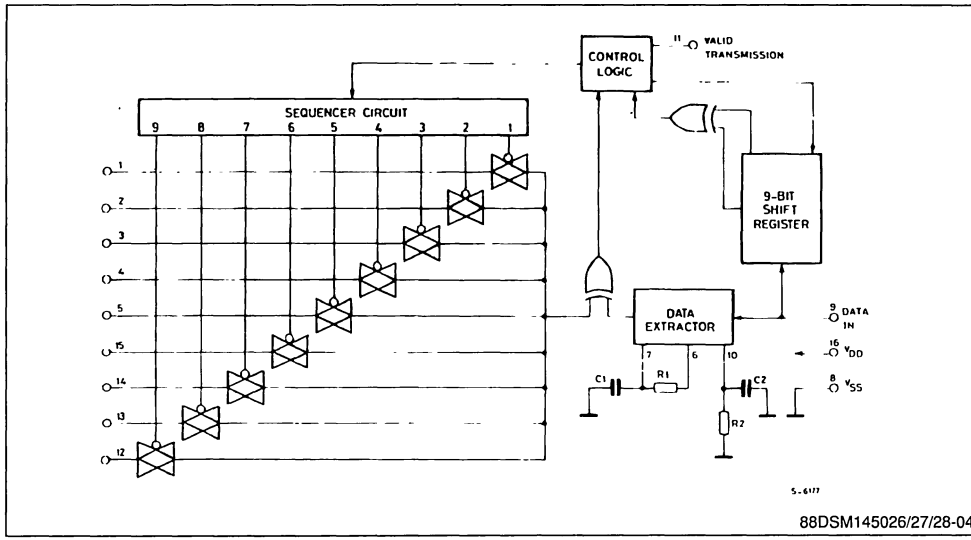


Figure 3 : Decoder Block Diagram M145028.



PIN DESCRIPTION

M145026 ENCODER

A1/D1-A9/D9. These inputs will be encoded and the data serially output form the encoder.

V_{SS}. The most negative supply (usually ground).

RS, CTC, RTC. These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator it should be connected to the RS input and the RTC and CTC pins should be left open.

$\overline{TE}$. This Transmit-Enable (active low) input will initiate transmission when forced low. A pullup device will keep this input high normally.

DATA OUT. This is the output of the encoder that will present the serially encoded signals.

V_{DD}. The most positive supply.

M145027/M145028 DECODERS

A1-A5 (M145027) / A1-A9 (M145028). These are the address inputs that must match the encoder inputs A1/D1-A5/D5 in the case of M145027 or A1/D1-A0/D9 in the case of M145028, in order for the decoder to output data.

D6-D9 (M145027). These outputs will give the information that is presented to the encoder inputs A6/D6-A9/D9.

Note: Only binary data will be acknowledged, a trinary open will be decoded as logic one.

R1, C1. These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant R1 x C1 should be set to 1.72 transmit clock periods. R1C1 = 3.95 RTC x CTC.

R2/C2. This pin accepts a resistor to V_{SS} and a capacitor to V_{SS} that are used to detect both the end of an encoded word and the end of transmission. The time constant R2 x C2 should be 33.5 transmit clock periods (four data bit periods). This time constant is used to determine that the Data In input has remained low for four data bit times (end of transmission). A separate comparator looks at a voltage equivalent two data bit times (0.4 R2C2) to detect the dead time between transmitted words. R2C2 = 77 x RTC x CTC.

VALID TRANSMISSION, VT. This output will go high when the following conditions are satisfied:

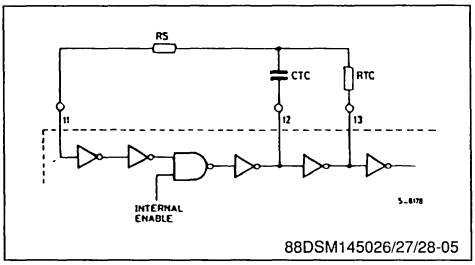
1. the transmitted address matches the receiver address, and
2. the transmitted data matches the last valid data received (M145028 only).

VT will remain high until either a mismatch is received, or no input signal is received for four data data bit times.

V_{DD}. The most positive supply.

V_{SS}. The most negative supply (usually ground).

Figure 4 : Encoder Oscillator Information.



The value for RS should be chosen to be about 2 times RTC. This range will ensure that current through RS is insignificant compared to current through RTC. The upper limit for RS must ensure that RS x 5 pF (input capacitance) is small compared to RTC x CTC. For frequencies outside the indicated range, the formula will be less accurate. The actual oscillation range of this circuit is from less than 1 Hz to over 1 MHz.

This oscillator will operate at a frequency determined by the external RC network; i.e..

$$f \approx \frac{1}{2.3 \cdot RTC \cdot CTC} (Hz)$$

for 1 kHz ≤ f ≤ 400 kHz

where: CTC = CTC + C layout + 12 pF

RS ≈ 2 RTC
RS ≥ 20 k
RTC ≥ 10 k
400 pF < CTC < µF

Figure 5 : Encoder/Decoder Timing Diagram.

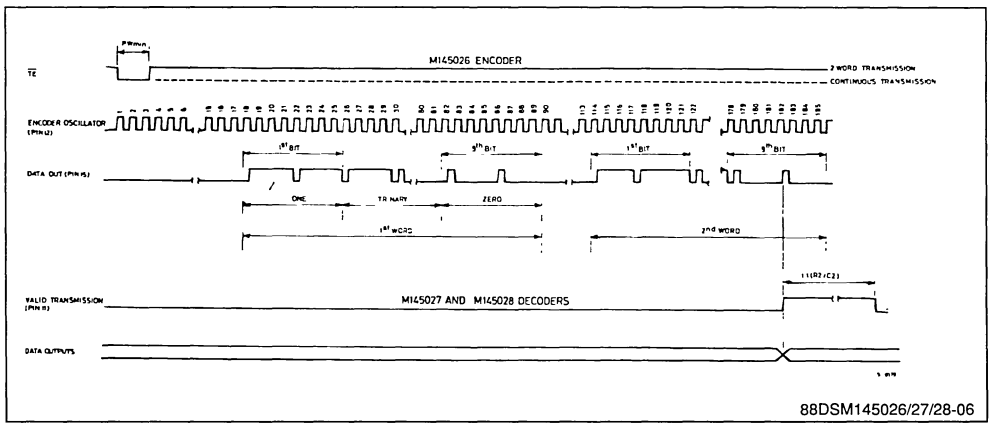
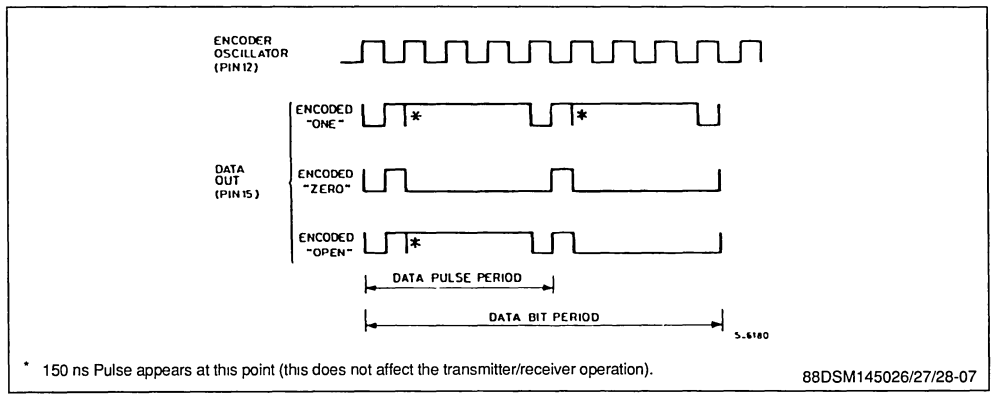


Figure 6 : Encoder Data Waveforms (M145026).



* 150 ns Pulse appears at this point (this does not affect the transmitter/receiver operation).

Figure 7 : M145027 Flowchart.

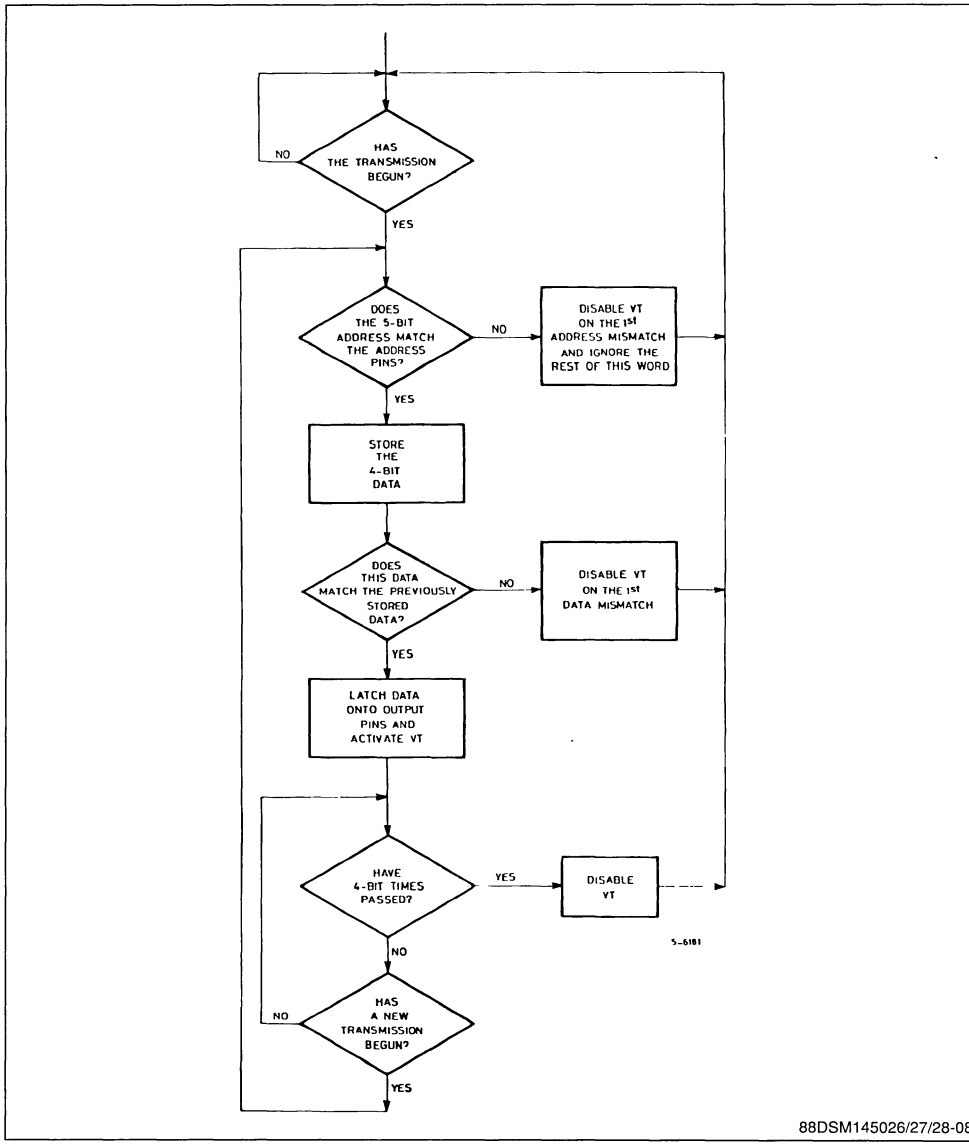


Figure 8 : M145028 Flowchart.

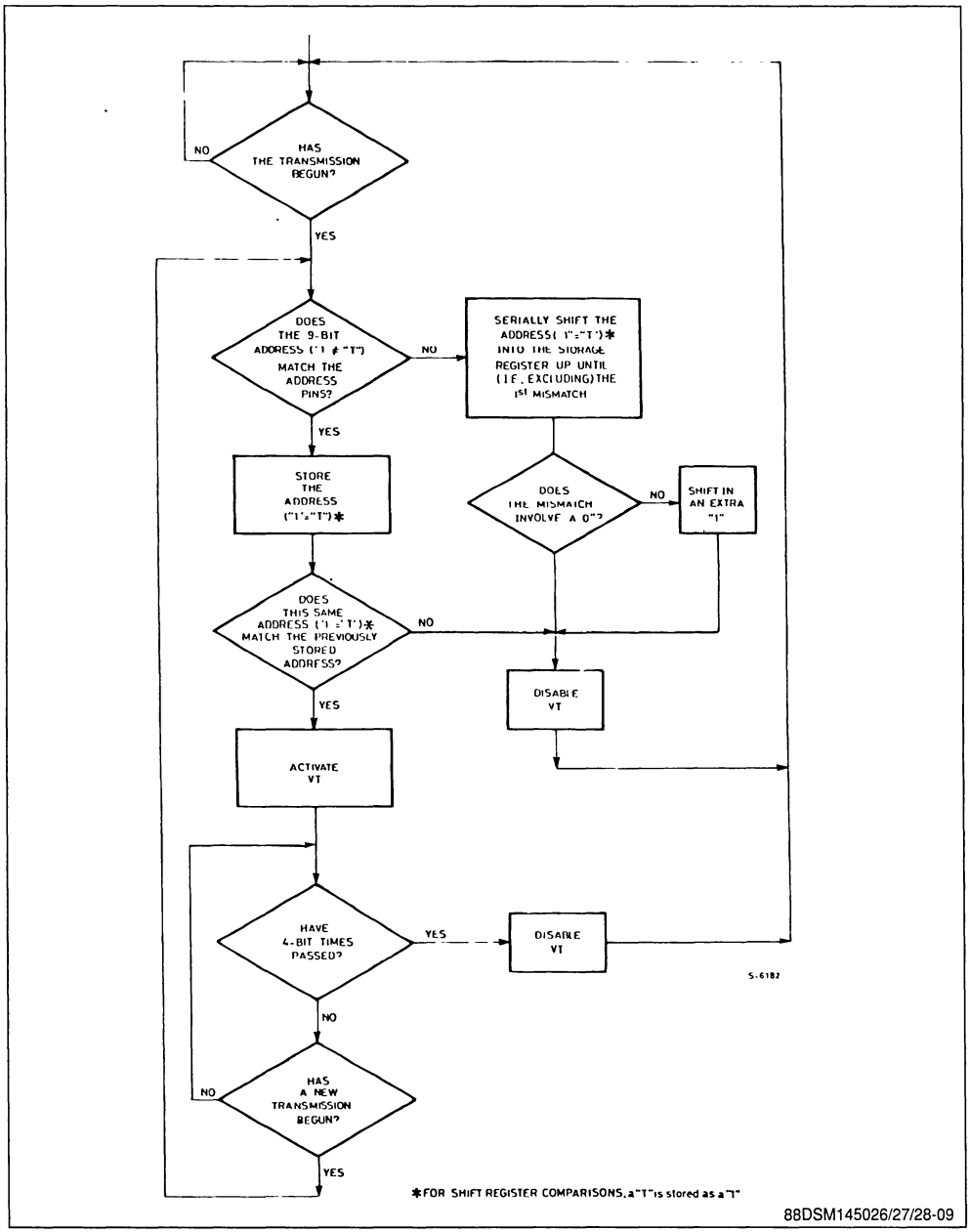
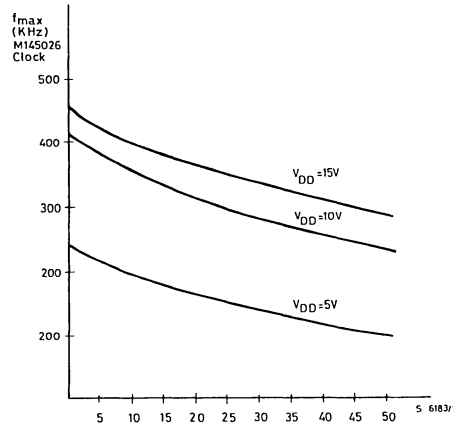
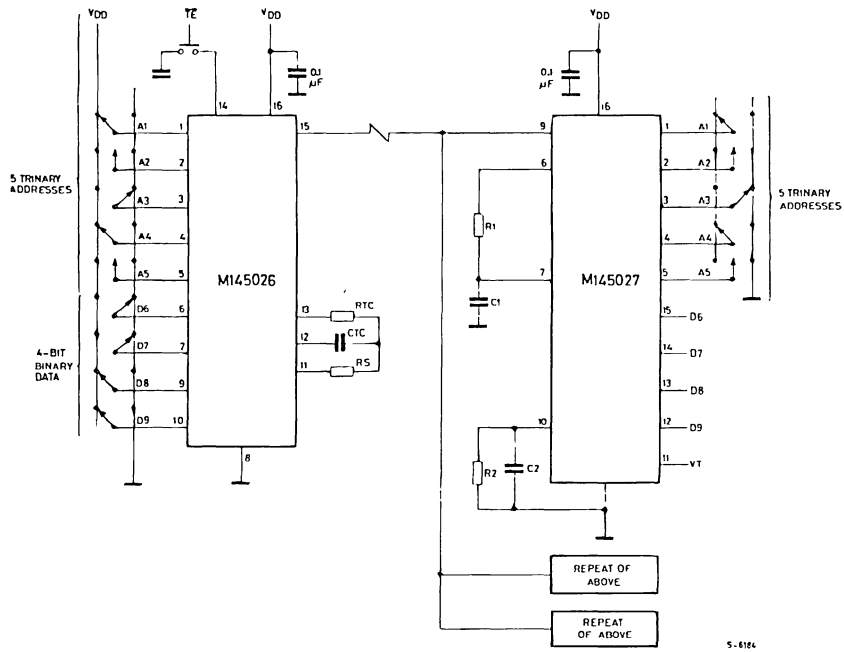


Figure 9 : M145027/M145028 (f_{max} vs. C_{layout}).



88DSM145026/27/28-010

Figure 10 : Typical Application.



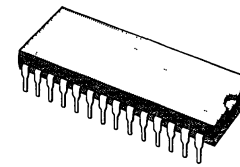
88DSM145026/27/28-11

EXAMPLE R/C VALUES (all resistors and capacitors are ± 5 %)
(CTC' = CTC + 20 pF)

f_{OSC} (kHz)	RTC	CTC'	RS	R1	C1	R2	C2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

DATA SLICER FOR TELETEXT PROCESSOR

- SEPARATION OF TELETEXT DATA FROM THE COMPOSITE VIDEO SIGNAL
- SEPARATION OF HORIZONTAL AND VERTICAL SYNCHRONIZATION SIGNALS FROM THE COMPOSITE VIDEO SIGNAL
- EXTERNAL OSCILLATOR GENERATING 6MHz SIGNAL SYNCHRONIZED TO A MULTIPLE OF THE LINE FREQUENCY BY PLL
- A 6.9375MHz CLOCK GENERATED FROM AN EXTERNAL QUARTZ CRYSTAL
- "AFTER-HOURS" SYNCHRONIZATION OPTION
- PROGRAMMABLE LEVELS FOR THE INPUT COMPOSITE VIDEO SIGNAL (1V OR 2.5V)
- PROCESSING OF EXTERNAL TELETEXT DATA
- OUTPUT OF POSITIVE OR NEGATIVE SYNCHRONIZING SIGNALS
- 28 PIN DIP PACKAGE
- HDS2P2 TECHNOLOGY



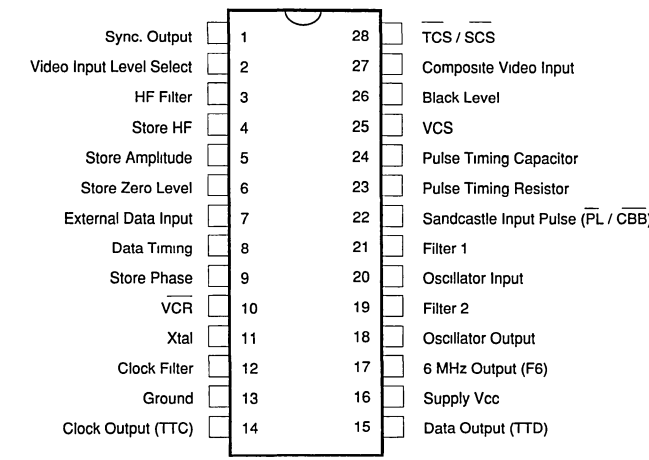
DIP28
(Plastic Package)

ORDER CODE : SAA5231

DESCRIPTION

The SAA5231 is a monolithic integrated circuit in 28 Pin DIP package designed to separate Teletext signals from TV signal.

PIN CONNECTIONS

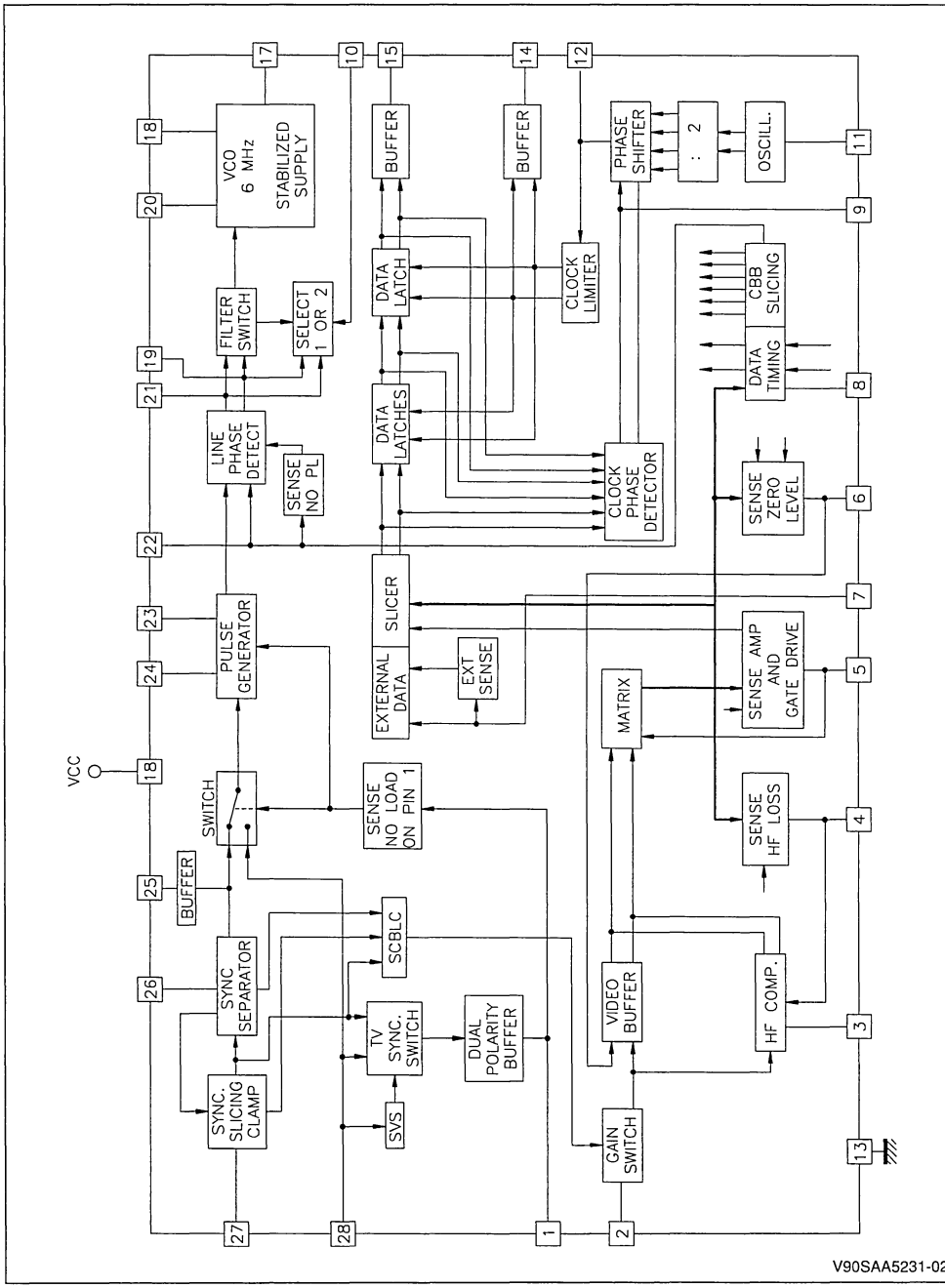


V90SAA5231-01

PIN DESCRIPTION

Pin	Function	Description
1	Display Synchronization Output	Synchronization signal output available as positive or negative
2	Input Video Signal Level	Input level selected as 1V (pin 2 low) or 2.5V (pin 2 not connected)
3	H.F. Filter	Video signal filtering using an external capacitor of 15pF
4-5-6	"HF STORE" "Amplitude STORE" "Zero Level STORE"	Three external capacitors used to store : 1/ HF amplitude 2/ Amplitude of adaptive data slicer 3/ Zero level
7	External Data Input	"Teletext data slice" input from external source
8	Data Timing	Connection of an external 270pF capacitor for the timing of the adaptive data slicer
9	Store Phase	Storage on an external capacitor of the output signal "Clock phase detector"
10	"Video Tape Recorder" Mode ($\overline{VCR}$)	Control signal for the PLL in the low-time constant mode
11	Crystal	External connection for a 13.875MHz crystal. This frequency, divided by 2, yields the 6.9375MHz clock
12	Clock Filter	Filter for 6.9375MHz clock
13	Ground	
14	Teletext Clock Output	Clock output for the SDA5243
15	Teletext Data Output	Output of Teletext data for the SDA5243
16	Supply V_{CC}	
17	6MHz Clock Output	6 MHz clock output for the SDA5243
18/20	Oscillator Output/Input	An external resonant circuit between pins 18 and 20 is connected to the 6MHz internal VCO
19	Filter 2	Low time constant filter for phase detection of the horizontal signal
21	Filter 1	High time constant filter for phase detection of the horizontal signal
22	"Sandcastle" Input Pulse	Input of the sandcastle signal produced by the SDA5243 from the PL and CBB signals
23	Pulse Timing Resistor	External resistor of 68kΩ used to define the current for the pulse generator
24	Pulse Timing Capacitor	External capacitor of 270pF to define the timing of the pulse generator
25	Composite Video Synchronizing Output (V_{CS})	Synchronizing output for the SDA5243
26	Black level	Storage of the black level for the adaptive sync. separator on an external 68nF capacitor
27	Composite Video Input	Composite video signal input for the adaptive sync. separator via an external capacitor of 2.2µF
28	Teletext Composite Sync. Input ($\overline{TCS}$) or Scan Composite Sync. Input ($\overline{SCS}$)	$\overline{TCS}$ input from the SDA5243 or $\overline{SCS}$ input from an alternative synchronizing circuit.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{16}	Supply Voltage	13.2	V
$-I_{25}$	Output Current V_{CS}	5	mA
$-I_{15}$	Output Current TTD	10	mA
$-I_{14}$	Output Current TTC	10	mA
$-I_{17}$	Output Current F6	10	mA
I_1	Output Current Sync.	5	mA
T_{stg}	Storage Temperature	- 40 to + 150	°C
T_J	Junction Temperature	0 to + 150	°C
T_A	Ambient Temperature	0 to + 70	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th(j-a)}$	Junction-Ambient Thermal Resistance	Max.	70	°C/W

ELECTRICAL CHARACTERISTICS

V_S = 12 V , T_A = 25 °C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
POWER SUPPLY (pin 16)					
V_S	Supply Voltage	10.8	12	13.2	V
I_S	Supply Current	-	70	-	mA
CVBS INPUT (pin 27)					
V_{27}	Input Signal Level : Pin 2 to ground Pin 2 open	 0.7 1.75	 1 2.5	 1.4 3.5	V
$V_{27(p-p)}$	Synchronous Signal Amplitude	0.1	-	1	V
$V_{27(txt)}$	Teletext Data Level : Pin 2 to ground Pin 2 open	 0.3 0.75	 0.46 1.15	 0.7 1.75	V
R_{G27}	Generator Resistance	-	-	250	Ω
VIDEO INPUT LEVEL SELECT (pin 2)					
 V_{2L} V_{2H}	Voltage : Low (V_{27} = 1 V) High (V_{27} = 2.5 V)	 0 2	 - -	 0.8 5.5	 V V
 - I_{2L} I_{2H}	Current : Low High	 0 0	 - -	 150 1.3	 µA mA
TELETEXT DATA (pin 15)					
$V_{15(p-p)}$	Signal TTD Output	2.5	3.5	4.5	V
t_r , t_f	Transition Times	20	30	45	ns
C_{15}	Load Capacitance	-	-	40	pF
V_{15DC}	DC Voltage at Output	-	4	-	V
DATA CLOCK (pin 15)					
$V_{14(p-p)}$	Signal TTC Output	2.5	3.5	4.5	V
t_r , t_f	Transition Times	20	30	45	ns
C_{14}	Load Capacitance	-	-	40	pF
t_d	Time Deviation with Respect to TTD	-20	0	+20	ns
V_{14DC}	DC Voltage at Output	-	4	-	V
SYNC. PULSE SEPARATION VCS (to SDA5243) (pin 25)					
 V_{25L} V_{25H}	Output Voltage : Low High	 0 2.1	 - -	 0.4 5.5	 V
 I_{25L} - I_{25H}	Output Current : Low High	 - -	 - -	 0.5 1.5	 mA
t_d	Delay with Respect to CVBS Sync.	-	0.5	-	µs

ELECTRICAL CHARACTERISTICS (continued)

V_S = 12 V , T_A = 25 °C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
SYNC. OUTPUT DRIVER (to TV set) (pin 1)					
$V_{1(p-p)}$	Output Voltage : $\overline{TCS}$ Operation CVBS Operation	 - -	 0.45 	 1	V
V_{1DC}	DC Voltage with Load Resistor to Ground (positive synchronous signal)	-	1.4	-	V
$-I_1$	Output Current	-	-	3	mA
V_{1DC}	DC Voltage with Load Resistor to V_S (negative synchronous signal)		10.1		V
I_1	Output Current	-	-	3	mA
6MHz CLOCK F6 (pin 17)					
$V_{17(p-p)}$	F6 Output Signal (negligible harmonic content)	1	2	3	V
t_r , t_f	Transition Times	20	-	40	ns
C_{17}	Load Capacitance	-	-	40	pF
V_{17DC}	DC Voltage	4	-	8.5	V
SYNCHRONIZATION SELECTION (pin 28)					
 $-I_{28}$ I_{28}	Input Current : $\overline{TCS}$ Operation (V_{28} = 0 to 7 V) CVBS Operation (V_{28} = 10 V to V_S)	 40 -5	 70 0	 100 5	µA
  V_{28L} V_{28H}	$\overline{TCS}$ Operation : Input Voltage (load resistor at pin 1) Low High	 0 2	 - -	 0.8 6.1	V
  V_{28L} V_{28H}	$\overline{SCS}$ Operation : Input Voltage (pin 1 open) Low High	 0 3.5	 - -	 1.5 6.1	V
t_p	Line Synchronous Pulse Width : $\overline{TCS}$ Operation $\overline{SCS}$ Operation	 - -	 2 3		µs
VCR OPERATION (pin 10)					
 V_{10L} V_{10H}	Input Voltage : VCR Operation Standard Operation	 0 2	 - -	 0.8 Vs	V
I_{10}	Input Current	-10	0	10	µA

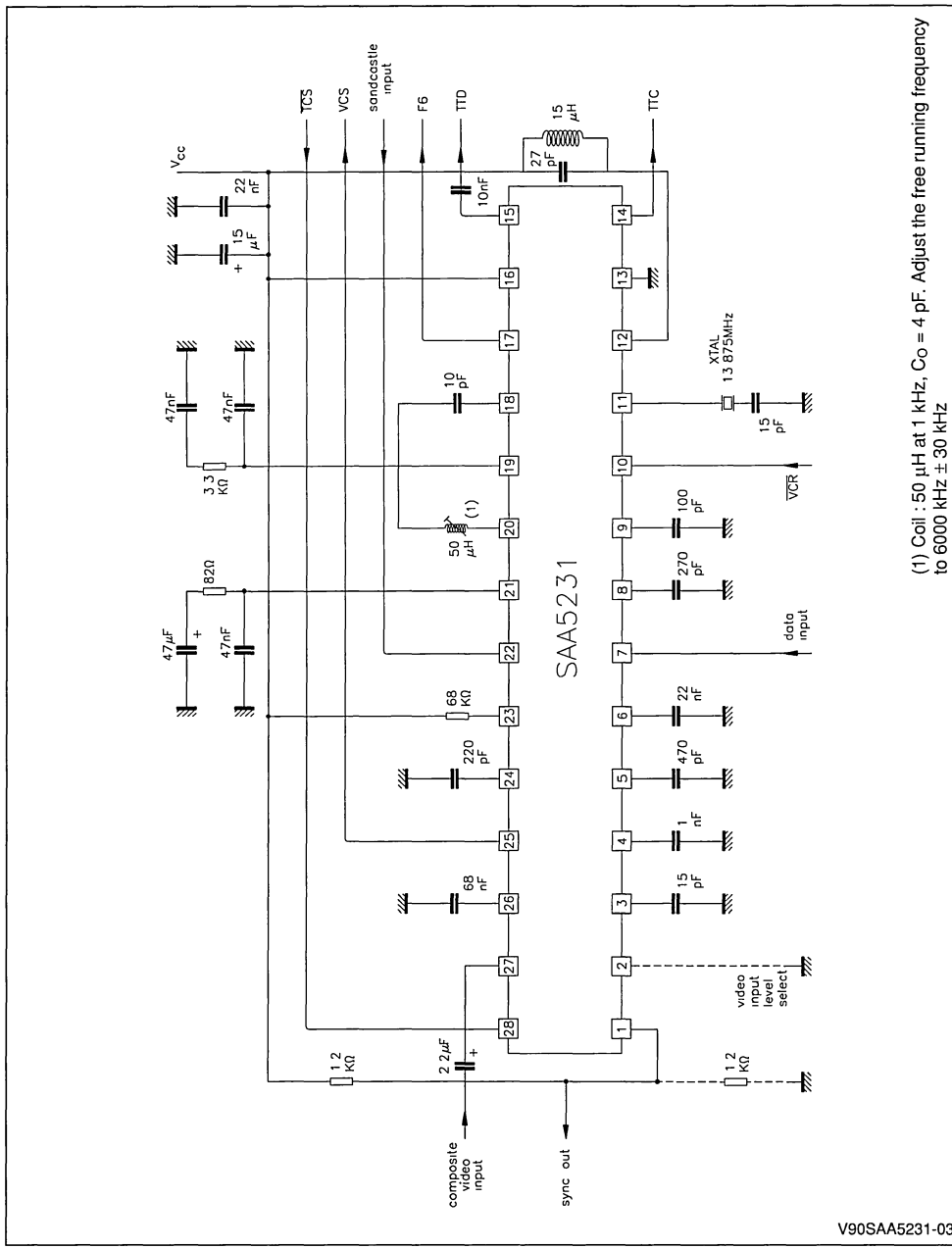
ELECTRICAL CHARACTERISTICS (continued)

V_S = 12 V , T_A = 25 °C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
SANDCASTLE PULSE INPUT (pin 22)					
	Phase Locked Mode Input Voltage PL :				V
V_{22L}	Low	0	-	3	
V_{22H}	High	3.9	-	5.5	
t_{pl}	PL - Low Time For Free-Wheeling Oscillator	100	-	-	ms
	Reset Pulse for Data Separation Input Voltage CBB :				V
V_{22L}	Low	0	-	0.5	
V_{22H}	High	1	-	5.5	
I_{22}	Input Current	-10	-	10	µA
EXTERNAL DATA INPUT (CURRENT SOURCE DRIVING) (pin 7)					
	Internal Data Processing Input :				
I_7	Current	-10	0	100	µA
V_7	Voltage (I_7 = -10 to 100 µA)	-	10	-	V
	External data processing input :				
I_{7L}	Current for Low Level	-175	-40	-25	µA
I_{7H}	Current for High Level	-1000	-500	-325	µA
V_7	Voltage (I_7 = -1000 to -25 µA)	7	8	-	V

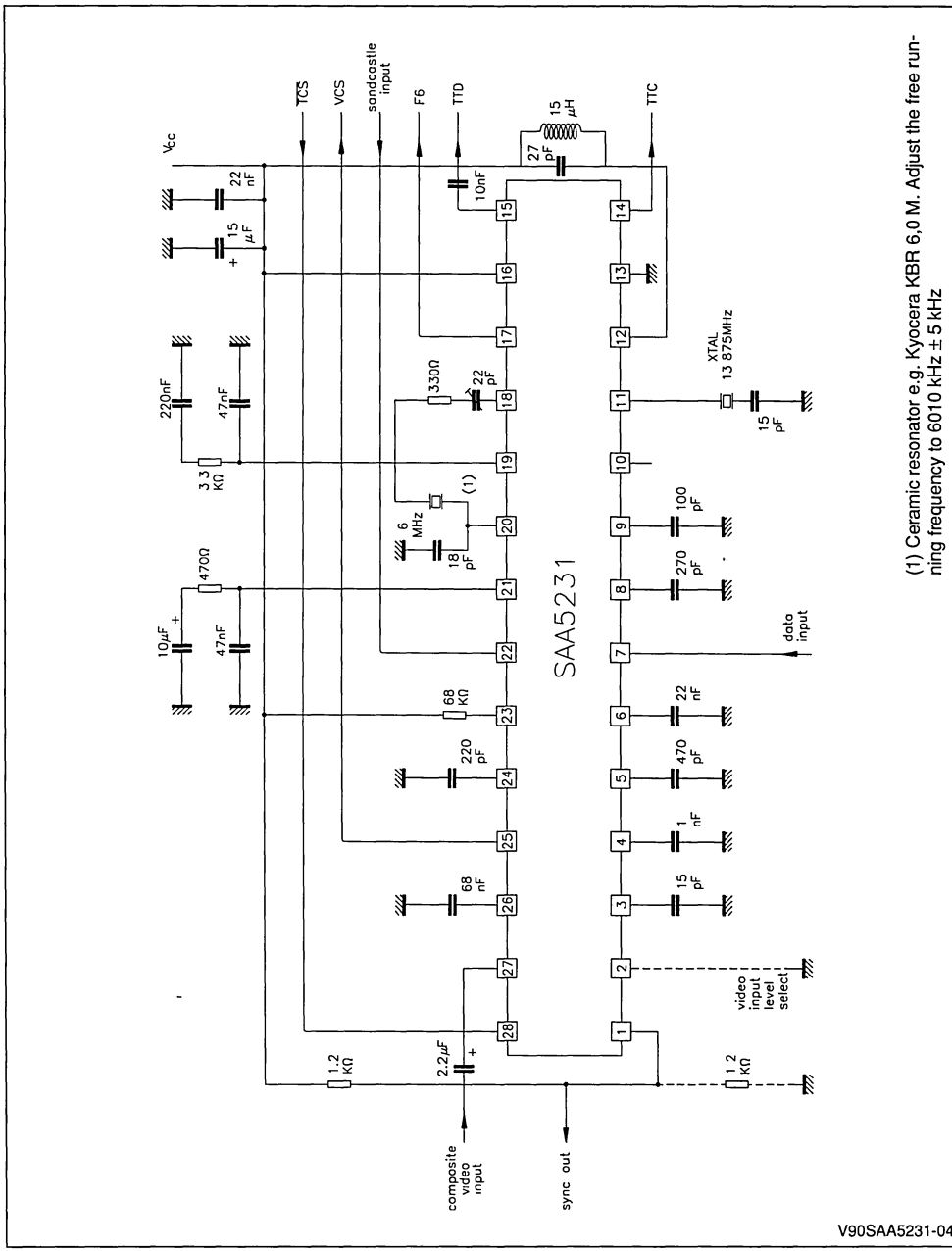
APPLICATION DIAGRAMS

Figure 1a : Application diagram with LC circuit in 6MHz PLL.



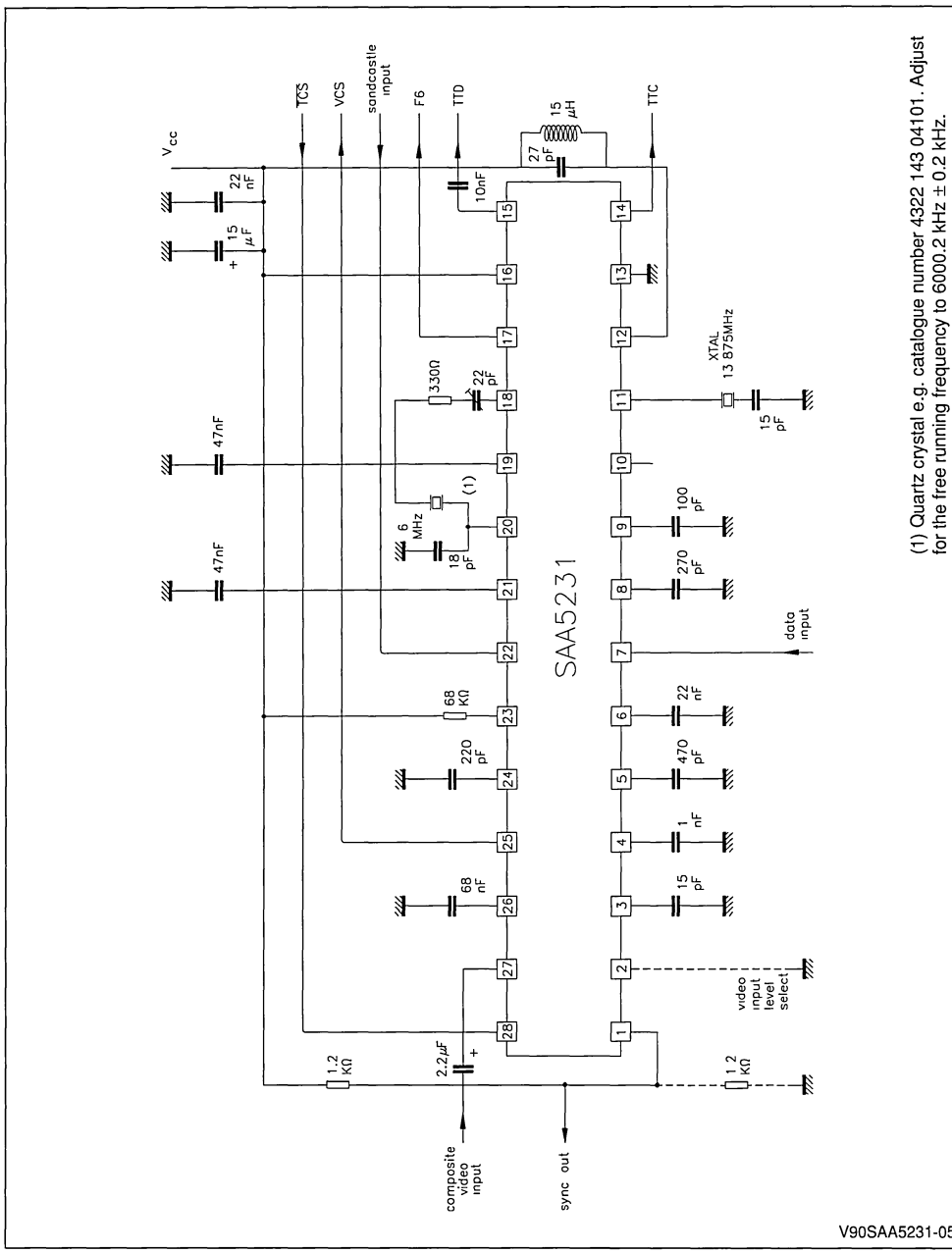
APPLICATION DIAGRAMS (continued)

Figure 1b : Application diagram with ceramic resonator in 6MHz PLL.



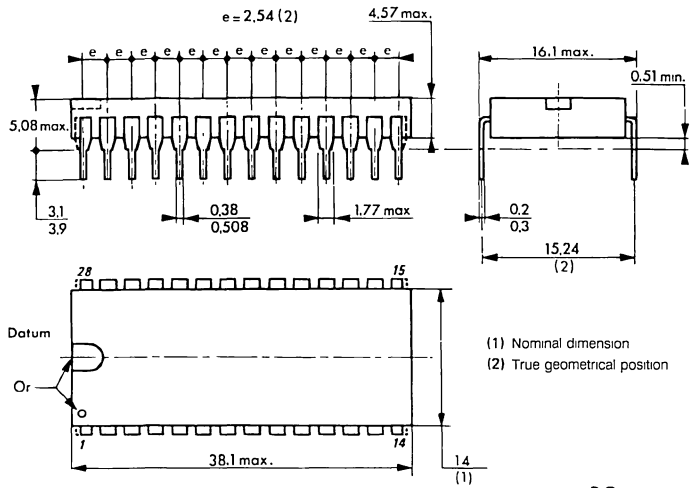
APPLICATION DIAGRAMS (continued)

Figure 1c : Application diagram with quartz crystal in 6MHz PLL.



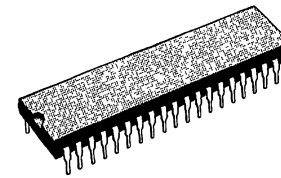
PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



COMPUTER-CONTROLLED TELETEXT DECODER

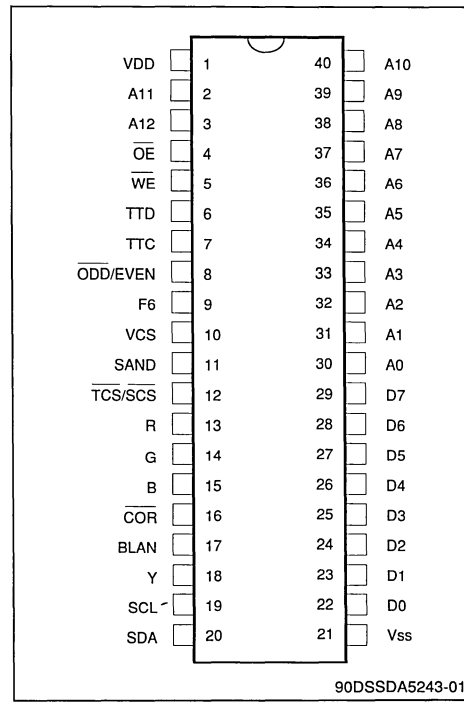
- AUTOMATIC SELECTION OF UP TO SEVEN NATIONAL LANGUAGES
- FOUR SIMULTANEOUS PAGE REQUESTS
- DISPLAY OF THE 25TH STATUS ROW
- MICROPROCESSOR CONTROL VIA AN I2C BUS (SLAVE ADDRESS 0010001 R/$\overline{W}$)
- DATA ACQUISITION AVAILABLE FROM LINES 2 TO 22 OR FROM A COMPLETE FIELD.
- DIRECT INTERFACE TO A STATIC RAM OF UP TO 8kBYTES
- HIGH QUALITY DISPLAY USING A CHARACTER MATRIX OF 12 x 10 DOTS.
- SINGLE + 5V SUPPLY VOLTAGE
- ON-CHIP MASK PROGRAMMABLE ROM CHARACTER GENERATORS
- NMOSH2 PROCESS



DIP40
(Plastic Package)

ORDER CODE :
SDA5243 West European Languages
SDA5243/H East European Languages

PIN CONNECTIONS



90DSSDA5243-01

DESCRIPTION

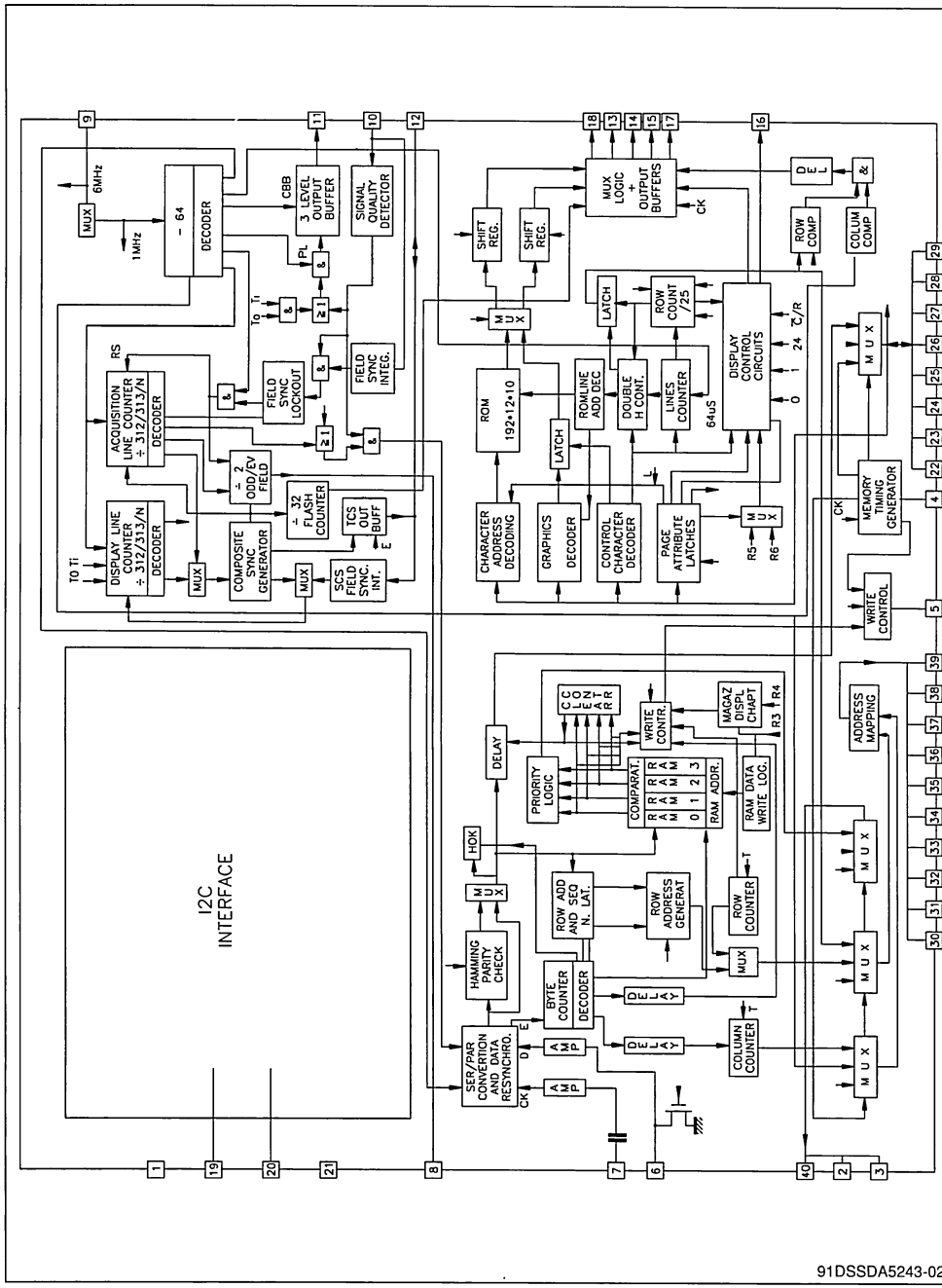
The SDA5243 is a NMOSH2 integrated circuit which performs all the processing of logical data within a 625 line system teletext decoder. It is designed to operate in conjunction with at least two chips : the SAA5231 integrated chip which extracts Teletext information embedded in a composite video signal and up to eight kilobytes of static RAM memory which can be used to store a maximum of 8 pages of display data. A complete system also comprises a microprocessor controling the SDA5243 via a 2-wire serial bus. An on-chip ROM memory contains the character sets. The SDA5243 performs automatic selection of one of up to seven natural languages. Data bytes may be decoded in either 7-Bit plus parity or in full 8-Bit formats. The chip set also supports facilities for reception and display of higher-level protocol data.

PIN DESCRIPTION

Pin	Symbol	Function	Description
1	V_{DD}	+5V	Positive supply voltage
2,3,40	A11, A12, A10	Chapter address	Address selection outputs for 1 of 8 static RAM chapters each of 1 kBytes.
4	$\overline{OE}$	Output enable	Active-low RAM output enable control signal.
5	$\overline{WE}$	Write enable	Active-low RAM write enable control signal. It supports write-cycles interleaved with read-cycles.
6	TTD	Teletext data input	An A.C. coupled teletext data input supplied by the SAA5231 chip is latched to V_{SS} between 4 and 8µs after each TV line.
7	TTC	Teletext clock input	A 6.9375MHz clock signal, supplied by the SAA5231 chip, is internally A.C. coupled, clamped and buffered.
8	$\overline{ODD}$/EVEN	Interlaced mode state output	High for even numbered and low for odd-numbered frames. The value is valid 2µs before the end of lines 311 and 624.
9	F6	Character display clock signal	The 6MHz clock signal, supplied by the SAA5231 chip is internally A.C. coupled, clamped and buffered.
10	VCS	Video composite synchronization input signal	Active high VCS input.
11	SAND	Sandcastle	Three level output pulse to the SAA5231 device. Phase lock, blanking signal, and color burst components are contained in this signal.
12	$\overline{TCS}/\overline{SCS}$	Input / output composite synchronization signal	Scan composite input signal ($\overline{SCS}$) for the display synchronization or Text composite sync. ($\overline{TCS}$) output signal to the SAA5231. Both signals are active low.
13,14,15	R G B	Red, green, blue	Character and background colors active-high open-drain outputs.
16	$\overline{COR}$	Contrast reduction	Open-drain active-low output supporting optimal display of characters in "mixed mode" operation.
17	BLAN	Blanking signal output	Open-drain active high output for TV-image blanking in normal and mixed-mode operation.
18	Y	Foreground output	Open-drain active-high output with foreground information. Can be used for printer command.
19	SCL	Serial clock	Microprocessor clock input via serial bus.
20	SDA	Serial data input / output	Open-drain microprocessor serial data input/output via serial bus.
21	V_{SS}	0 Volt	Ground.
22-29	D0-D7	Parallel data input / output	Eight tri-state input/output for data read/write from/to an external RAM.
30-39	A0-A9	Address signals	Ten addresses output pins for accessing to individual Bytes of a 1 kByte chapter stored in an external Static RAM.

TAB-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Range	-0.3 to +7.5	V

INPUT VOLTAGE RANGE :

V_I	VCS,SDA,SCL,D0-D7 TTD,F6,TCS/SCS,TTC	-0.3 to +7.5 -0.3 to +10	V V

OUTPUT VOLTAGE RANGE :

V_O	SAND,A0-A12,OE,WE,D0-D7,SDA,ODD/EVEN,R,G,B ,BLAN,COR, Y TCS/SCS	-0.3 to +7.5 -0.3 to +10	V V
T_{stg}	Storage Temperature Range	-20 to +125	°C
T_A	Operating Ambient Temperature Range	-20 to +70	°C

TAB-02

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage (pin 1)	4.5	5	5.5	V
I_{DD}	Supply Current	-	140	200	mA

INPUTS

	TTD (pin 6)				
C_{EXT}	Ext. Coupling Capacitor	-	-	50	nF
$V_{I(p-p)}$	Input Voltage p-p	2	-	7	V
t_r , t_f	Input Rise / Fall Times	10	-	80	ns
t_{DS}	Input Set-up Time	40	-	-	ns
t_{DH}	Input Hold Time	40	-	-	ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to 10V)	-	-	20	µA
C_I	Input capacitance	-	-	7	pF
	TTC, F6 (pins 7,9)				
V_I	DC Input Voltage	- 0.3	-	+10	V
$V_{I(p-p)}$	AC Input Voltage F6 AC Input Voltage TTC	1 1.5	- -	7 7	V V
± V_P	Input Peak Rel. 50 % Duty	0.2	-	3.5	V
f_{TTC}	TTC Clock Frequency	4	6.9375	8	MHz
f_{F6}	F6 Clock Frequency	4	6	8	MHz
t_r , t_f	Clock Rise / Fall Times	10	-	80	ns
$I_{I(L)}$	Input Leakage Current (VI = 0 to10 V)	-	-	20	µA
C_I	Input Capacitance	-	-	7	pF

TAB-03

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min	Typ	Max	Unit
INPUTS					
	VCS (pin 10)				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 2	 - -	 0.8 V_{DD}	V
t_r , t_f	Input Rise / Fall Times	-	-	500	ns
$I_{I(L)}$	Input Leakage Current (VI = 5.5V)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
	SCL (pin 19)				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 3	 - -	 1.5 VDD	V
f_{SCL}	SCL Clock Frequency	-	-	100	KHz
t_r , t_f	Input Rise / Fall Times	-	-	2	µs
$I_{I(L)}$	Input Leakage Current (VI = 5.5V)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
INPUT/OUTPUTS					
	$\overline{TCS}$(output), $\overline{SCS}$(input) (pin12)				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 3	 - -	 1.5 8	V
t_r , t_f	Input Rise / Fall Times	-	-	500	ns
± $I_{I(L)}$	Input Leakage Current (Vi = 0 to10V and output in high impedance state)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
V_{OL} V_{OH}	Output Voltage : ● Low Level I_{OL} = 0.4mA ● High Level -I_{OH} = 0.2mA I_{OH} = 0.1mA	 0 2.4 2.4	 - - -	 0.4 V_{DD} 5 5	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	100	ns
C_I	Load Capacitance	-	-	50	pF
	SDA (pin 20) (see fig. 8)				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 3	 - -	 1.5 V_{DD}	V
t_r , t_f	Input Rise / Fall Times	-	-	2	µs
$I_{I(L)}$	Input Leakage Current (VI = 5.5V with output off)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF

TAB-03

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min	Typ	Max	Unit
INPUT/OUTPUTS					
	SDA (continued)				
V_{OL}	Low Output Voltage (I_{OL} = 3mA)	0	-	0.5	V
t_f	Output Fall Time between 3.0V and 1.0V	-	-	200	ns
C_I	Load Capacitance	-	-	400	pF
	D0-D7 (pin 22-29), (see fig.9)				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 2	 - -	 0.8 V_{DD}	V
$\pm I_{I(L)}$	Input Leakage Current (VI = 0 to 5.5V and output in high impedance state)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
V_{OL} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 1.6mA) ● High Level ($-I_{OH}$ = 0.2mA)	 0 2.4	 - -	 0.4 V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	50	ns
C_I	Load Capacitance	-	-	120	pF
OUTPUTS					
	A0-A12, $\overline{OE}$, $\overline{WE}$ (pins 30-40,2,3,4,5,)				
V_{OL} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 1.6mA) ● High Level ($-I_{OH}$ = 0.2mA)	 0 2.4	 - -	 0.4 V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	50	ns
C_L	Load Capacitance	-	-	120	pF
	$\overline{ODD}$/EVEN (pin 8)				
V_{OL} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 0.4mA) ● High Level ($-I_{OH}$ = 0.2mA)	 0 2.4	 - -	 0.4 V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	100	ns
C_L	Load Capacitance	-	-	50	pF
	SAND (pin 11)(see fig.5)				
V_{OL} V_{OI} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 0.2mA) ● Middle Level (I_{OL} = ± 10 µA) ● High Level (I_{OH} = 0/- 10µA)	 0 1.1 4	 - - -	 0.25 2.9 V_{DD}	V
t_{r1} t_{r2}	Output Rise Time : ● V_{OL} to V_{OI} from 0.4 to 1.1V ● V_{OI} to V_{OH} from 2.9 to 4.0V	 - -	 - -	 400 200	ns
t_f	Output Fall Time V_{OH} to V_{OI} from 4.0 to 0.4V	-	-	50	ns

TAB-03

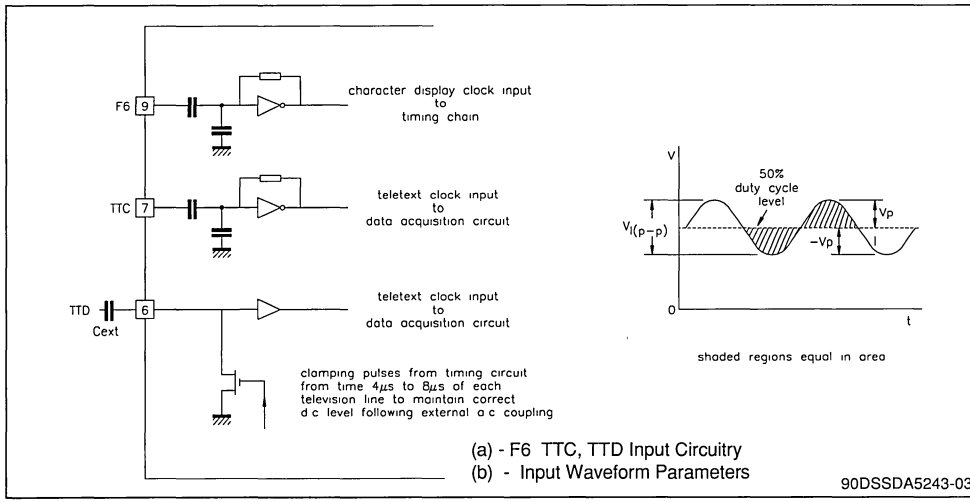
ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min	Typ	Max	Unit
OUTPUTS					
	SAND (continued)				
C_I	Load Capacitance	-	-	30	pF
	R, G, B, $\overline{COR}$, BLAN, Y (pins 13-18), (see fig.8)				
V_{OL}	Low Level Output Voltage : • I_{OL} = 2mA • I_{OL} = 5mA	 0 0	 - -	 0.4 1	V
V_{PU}	Pull-up Voltage (with R = 1kΩ to 5V)	-	-	5	V
t_f	Output Fall Time from 4.5 to 1.5V (with R = 1kΩ to 5V)	-	-	20	ns
t_{SK}	Skew Delay on Falling Edges (at 3V with R = 1kΩ connected to 5V)	-	-	20	ns
C_L	Load Capacitance	-	-	25	pF
I_{LO}	Output Leakage Current (V_{PU} = 0 to 6V output off)	-	-	20	µA
TIMING					
	SERIAL BUS (referred to V_{IH} = 3V, V_{IL} = 1.5V)				
t_{LOW} t_{HIGH}	Clock : • Low Period • High Period	 4 4	 - -	 - -	µs
t_{SU} , d_{AT} t_{HD} , d_{AT}	Data Set-up Time Data Hold Time	250 170	- -	- -	ns ns
t_{SU} , $_{STO}$	Stop Set-up Time from Clock High	4	-	-	µs
t_{BUF}	Start Set-up Time Following a Stop	4	-	-	µs
t_{HD} , $_{STA}$ t_{SU} , $_{STA}$	Start Hold Time Start Set-up Time Following Clock Low to High Transition	4 4	- -	- -	µs µs
	MEMORY INTERFACE referred to V_{IL} = 1.5V				
t_{CY}	Cycle Time	-	500	-	ns
t_{OE}	Adress Change to $\overline{OE}$ Low	60	-	-	ns
t_{ADDR}	Address Active Time	450	500	-	ns
t_{OEW}	$\overline{OE}$ Pulse Duration	320	-	-	ns
t_{ACC}	Access Time from $\overline{OE}$ to Data Valid	-	-	200	ns
t_{DH}	Data Hold Time from $\overline{OE}$ High or Address Change	0	-	-	ns
t_{WE}	Address Change to $\overline{WE}$ Low	40	-	-	ns
t_{WEW}	$\overline{WE}$ Pulse Duration	200	-	-	ns
t_{DS}	Data Set-up Time to $\overline{WE}$ High	100	-	-	ns
t_{DHWE}	Data Hold Time from $\overline{WE}$ High	20	-	-	ns
t_{WR}	Write Recovery Time	25	-	-	ns

TAB-03

F6, TTC, TTD INPUT INTERNAL CONNECTIONS



(a) - F6 TTC, TTD Input Circuitry
(b) - Input Waveform Parameters

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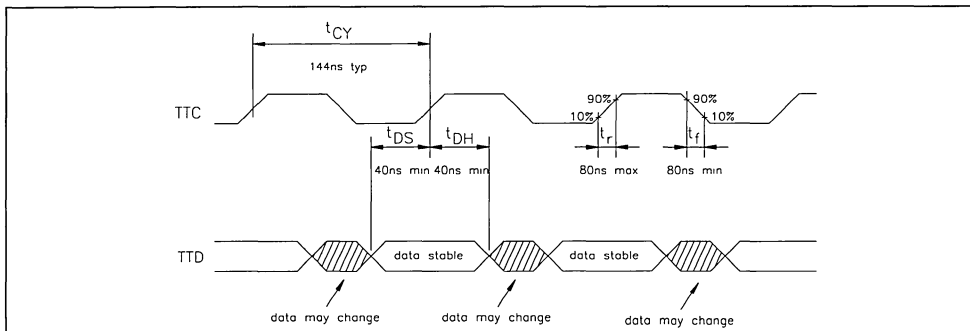
TELETEXT DATA INPUT TIMING

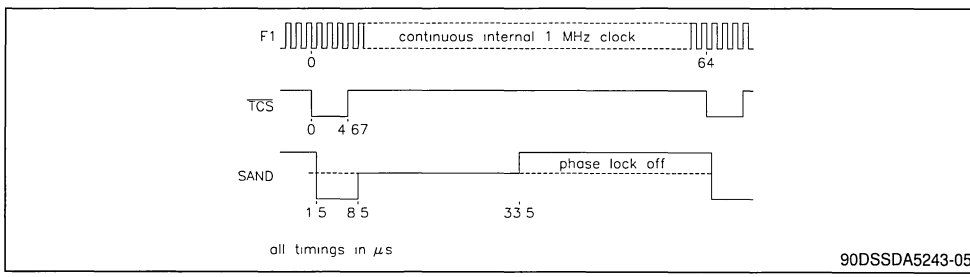


Data Stable : 1 if ≥ 2V , 0 if ≤ 0.8V

90DSSDA5243-04

SYNCHRONIZATION TIMING

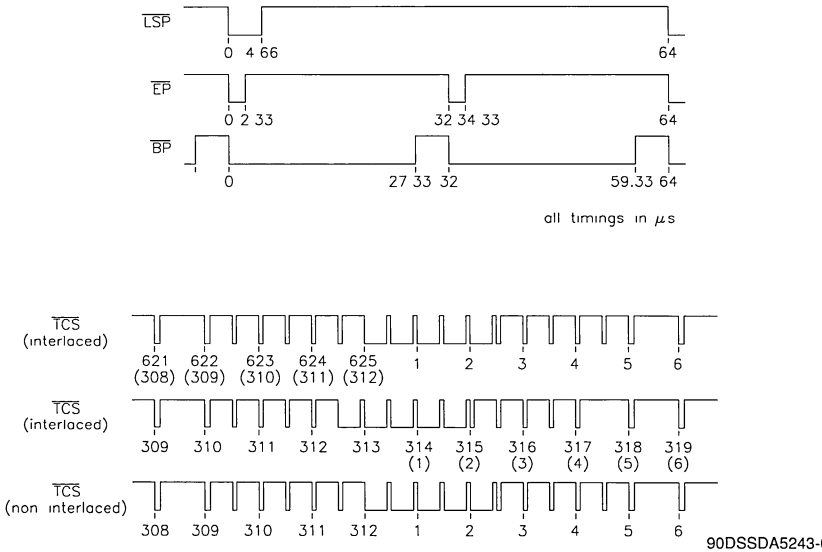
Figure 5



90DSSDA5243-05

COMPOSITE SYNC. WAVEFORMS

Figure 6

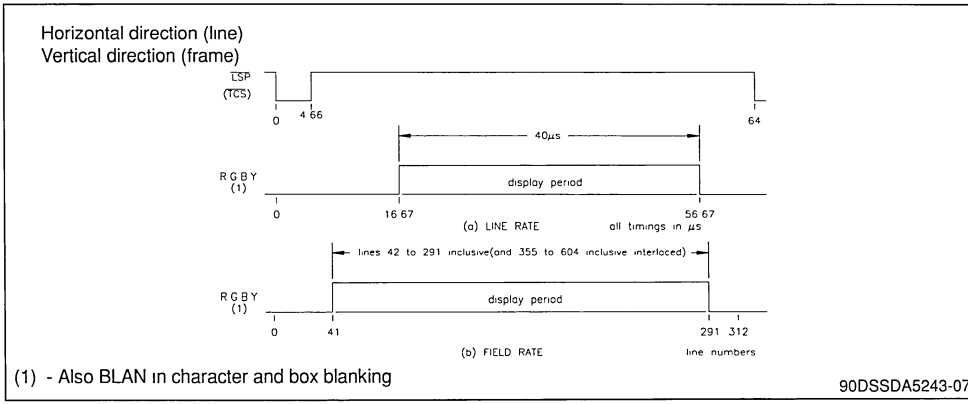


The number positions indicate the end of lines.
The Teletext composite synchronization signal ($\overline{TCS}$), whether interlacing is present or not, comprises three components.
a) The line-synchronization pulses (LSP).
b) the equalisation pulses (EP)
c) the frame-synchronization pulses (BP).

The timing reference is specified by the descending edge of the signal LSP, with a tolerance spread of ± 100 ns.

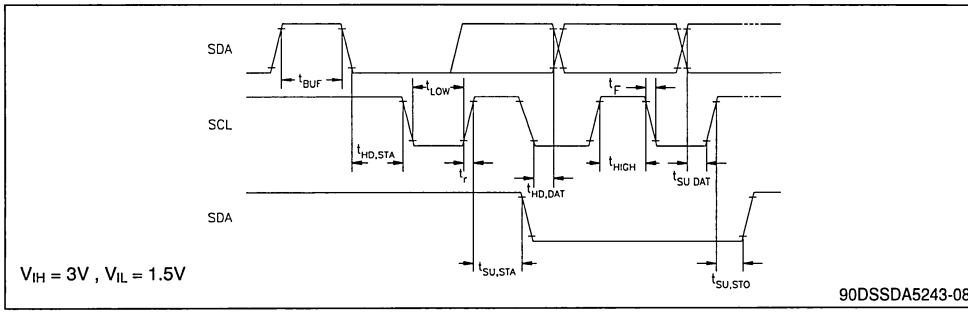
DISPLAY OUTPUT TIMING

Figure 7



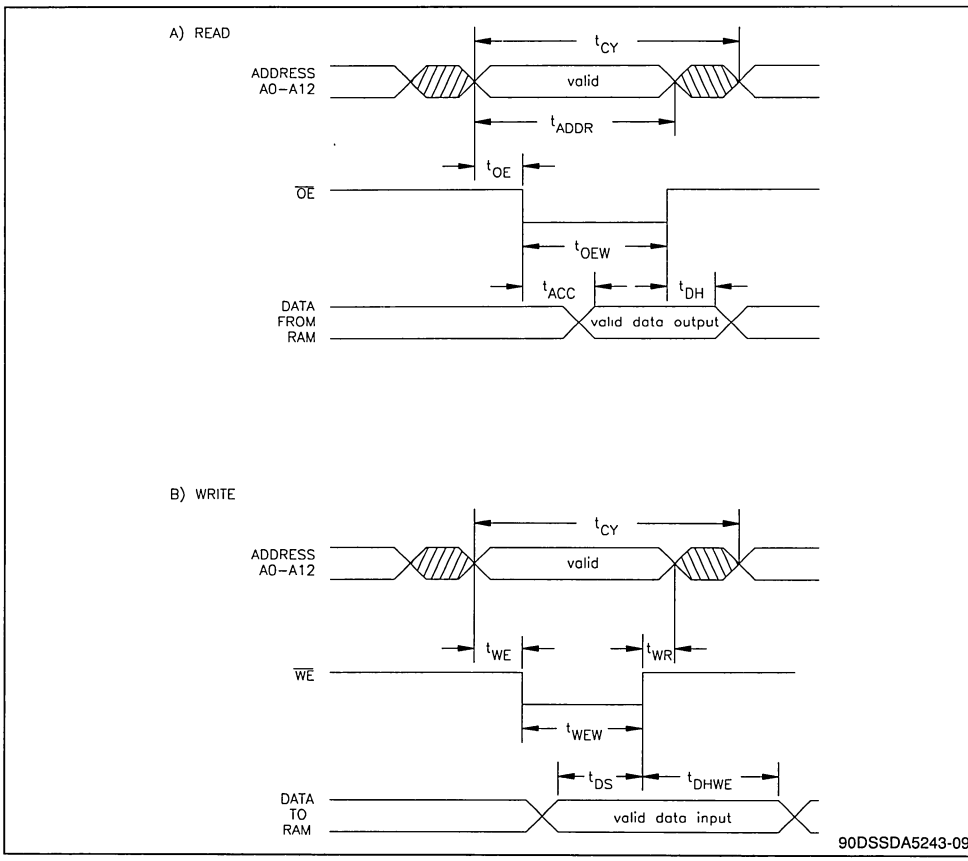
SERIAL BUS TIMING

Figure 8

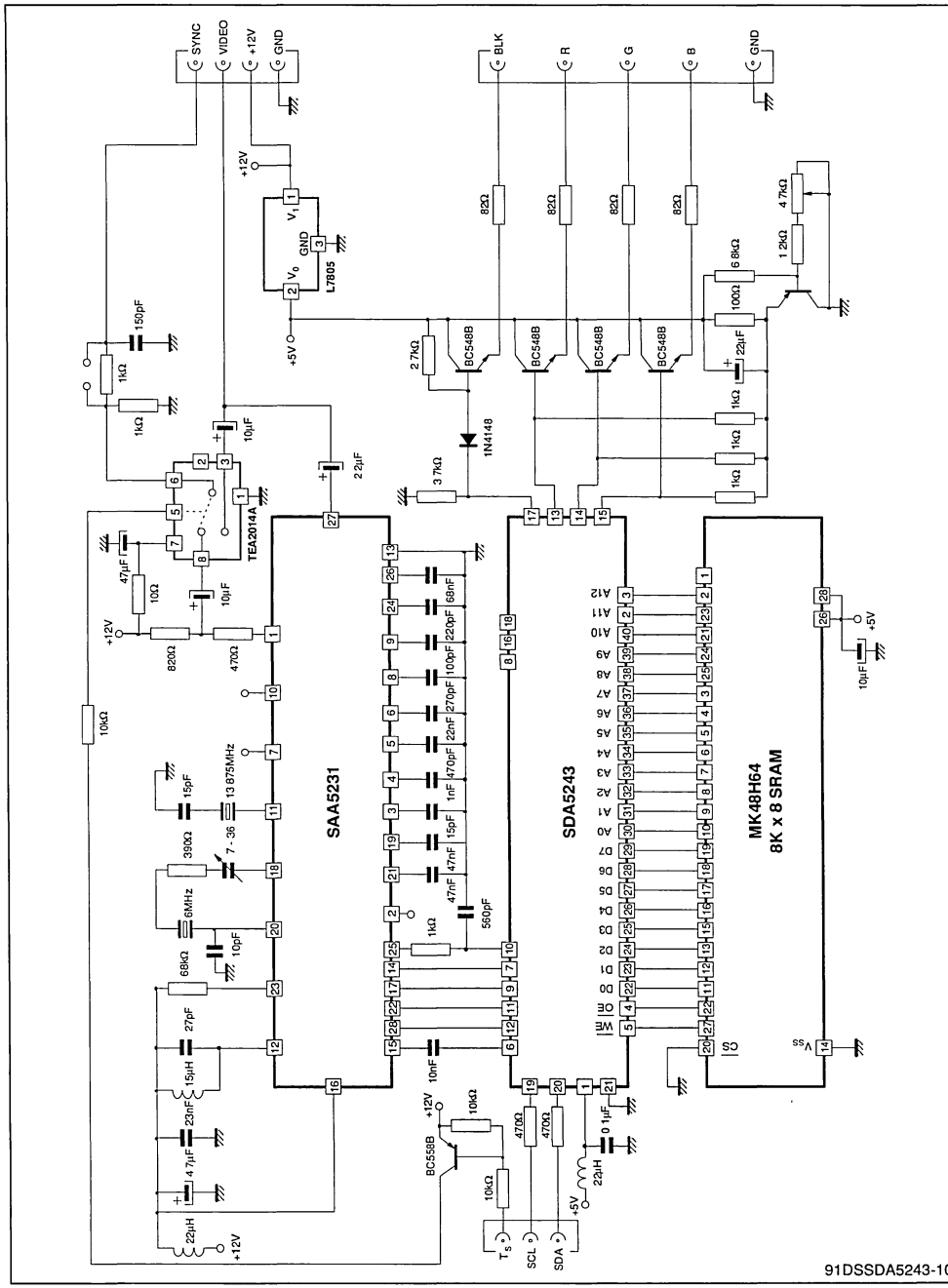


MEMORY INTERFACE TIMING

Figure 9



APPLICATION DIAGRAM



APPLICATION NOTES

ORGANIZATION OF A PAGE-MEMORY

The organization of a page-memory is shown in Figure 11. In contrast with the first generation of Teletext Decoders the new CCT (Computer Controlled Teletext) chip provides a display format of 25 rows of 40 characters per row.
Row number twenty-four is used by the microprocessor for the display of information.
Row zero contains the page header.
The organization is as follows :
The first seven characters (0 - 6) are used for messages regarding the operational status.
The eighth character is an alphanumeric control character either "white" or "green" defining the "search" status of the page. When it is "white" the operational state is normal and the header appears white ; when it is "green" the operational state corresponds to "search mode" and the header appears green. The following twenty-four characters give the header of the requested page when the system is in search mode. The last eight characters display the time of day.
Row twenty-five comprises ten bytes of control data concerning the received page (see Table 1) and fourteen free bytes which can be used by the microprocessor.

PAGE MEMORY ORGANISATION

Figure 11

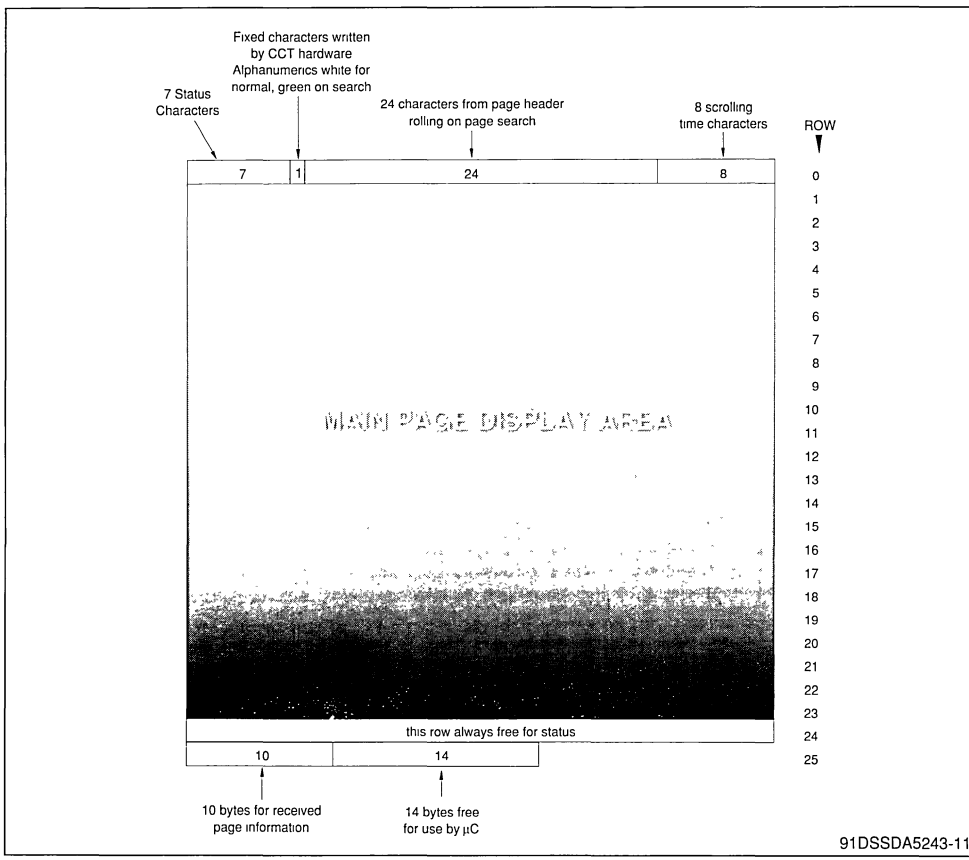


Table 1 : Row 25 received control data format.

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM	HAM	HAM	HAM	HAM	HAM	HAM	HAM	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
COLUMN	0	1	2	3	4	5	6	7	8	9

Page number : - MAG = magazine, PU = page units, PT = page tens.
Page sub-code : - MU = minutes units, MT = minutes tens, HU = hours units, HT = hours tens.
PBLF = page being looked for, FOUND = low for page found, HAM = hamming error in byte, C4-14 = control bits.

TAB-04

REGISTER MAP (see Table 2)

Registers R1 to R10 are write only whilst R11 is a read/write register respect to the microprocessor. The automatic succession on a byte basis is indicated by the arrows in Table 2.
In the normal operating mode TA and TB should be set to logic level 0.
After power-up the contents of the registers are as follows : all bits in registers R1 to R10 are cleared to zero with the exception of bits D0 an D1 in registers R5 and R6 which are set to logical one. After power-up all the memory bytes are preset to hexadecimal value 20 H (space) with the exception of the byte corresponding to row 0 of column 7 of chapter 0 which is set to the value corresponding to "alpha white" hexadecimal value 07 H.

Table 2 : Register specification.

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P/8\ \text{BIT}}$	$\underline{\text{ACQ}}$ $\overline{\text{ON/OFF}}$	GHOST ROW ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
-	BANK SELECT A2	ACQ CCT A1	ACQ CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request adress
-	-	-	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
-	-	-	-	-	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash / subtitle)
STATUS $\underline{\text{ROW}}$ BTM/TOP	CURSOR ON	$\overline{\text{CONCEAL}}$/ REVEAL	$\overline{\text{TOP}}$/ BOTTOM	$\overline{\text{SINGLE}}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
-	-	-	-	CLEAR MEM	A2	A1	A0	R8	Active chapter
-	-	-	R4	R3	R2	R1	R0	R9	Active row
-	-	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

- bit does not exist

REGISTER FUNCTIONS

Register	Function	Bit(s)	Description
R1	Mode controls	T0,T1 (D0,D1)	These bits control the frame display format. Interlaced or non-interlaced,312/313 or 312/312.
		TCS ON (D2)	This bit determines the character display synchronization mode. Teletext composite synchronism (TCS ON = 1) or direct broadcast synchronism (TCS ON = 0).
		$\overline{\text{DEW}}$/FULLFIELD (D3)	Selection of field flyback mode or full channel mode (D3 = 1) for recovering of Teletext data.
		GHOST ROW ENABLE (D4)	Selection of ghost row mode (D4 = 1)
		ACQUISITION $\overline{\text{ON/OFF}}$ (D5)	Control of acquisition operation (D5 = 0 enables acquisition)
		7 bits + parity or 8 bits without parity (D6)	Selection of received data format either 7 bits with parity (D6 = 0) or 8 bits without parity (D6 = 1).
		TA (D7)	Test bit equal to "0" in the normal operating mode.
R2	Addressing information for a page request	SC0,SC1,SC2 (D0,D1,D2)	Address the first column of the on chip page request RAM to be written.
		TB (D3)	Test bit equal to "0" in the normal working mode.
		A0,A1 (D4,D5)	Address a group of four consecutive pages currently used for data acquisition;
		A2 (D6)	Address of one of the two groups of four pages for acquisition in normal mode.
R3	Data relative to the requested page (see Table 3).	PRD0-PRD4 (D0-D4)	Written data in the page request RAM, starting with the columns addressed by SC0,SC1,SC2.
R4	Selection of one of eight pages to display.	A0,A1,A2 (D0,D1,D2)	These three bits correspond to the logical states of the three address lines (A12,A11,A10) during memory read cycles.
R5	Display control for normal operation.	PON (D0,D1)	Picture on (IN. D0, OUT: D1)
		TEXT (D2,D3)	Text on (IN: D2, OUT: D3)
		COR (D4,D5)	Contrast reduction on (IN· D4, OUT: D5)
		BKGND (D6,D7)	Background colour on (IN: D6, OUT: D7)
		IN/OUT	Enable inside/outside the box
R6	Display control for news-flash subtitle generation.	See R5	See R5
R7	Display mode	BOX ON 0,1-23,24 (D0,D1,D2)	The "boxing" function is enabled on row 0,1-23 and 24 by D0, D1 and D2 set to one.
		STATUS ROW $\overline{\text{BTM/TOP}}$ (D7)	The 25th row is displayed before the "Main text Area" (lines 0-23) or after (D7 = 0).
R8 to R11	Active chapter address (R8), active row address (R9), active column address (R10). Data contained in R11 read (written) from (to) memory by microprocessor via I^2C bus.		

TAB-05

Table 3 : Register R3.

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care page tens	PT3	PT2	PT1	PT0
2	Do care page units	PU3	PU2	PU1	PU0
3	Do care hours tens	X	X	HT1	HT0
4	Do care hours units	HU3	HU2	HU1	HU0
5	Do care minutes tens	X	MT2	MT1	MT0
6	Do care minutes units	MU3	MU2	MU1	MU0

TAB-06

The abbreviations have the same significance as in Table 1 with the exception of the "DO CARE" entries. It is only when this bit is "1" that the corresponding digit is taken into consideration on page request. For example, a page defined as "normal" or one difined as "timed" may be selected.

If "HOLD" is low the page is held. The addressing of successive bytes via the I^2C bus is automatic.

CHARACTER SETS

The selection of the character sets for a particular language is effected by the three control bits (C12-C14) located in the page header. These three bits are decoded as shown in Table 4.

Table 4a : National character sets control bits for SDA5243

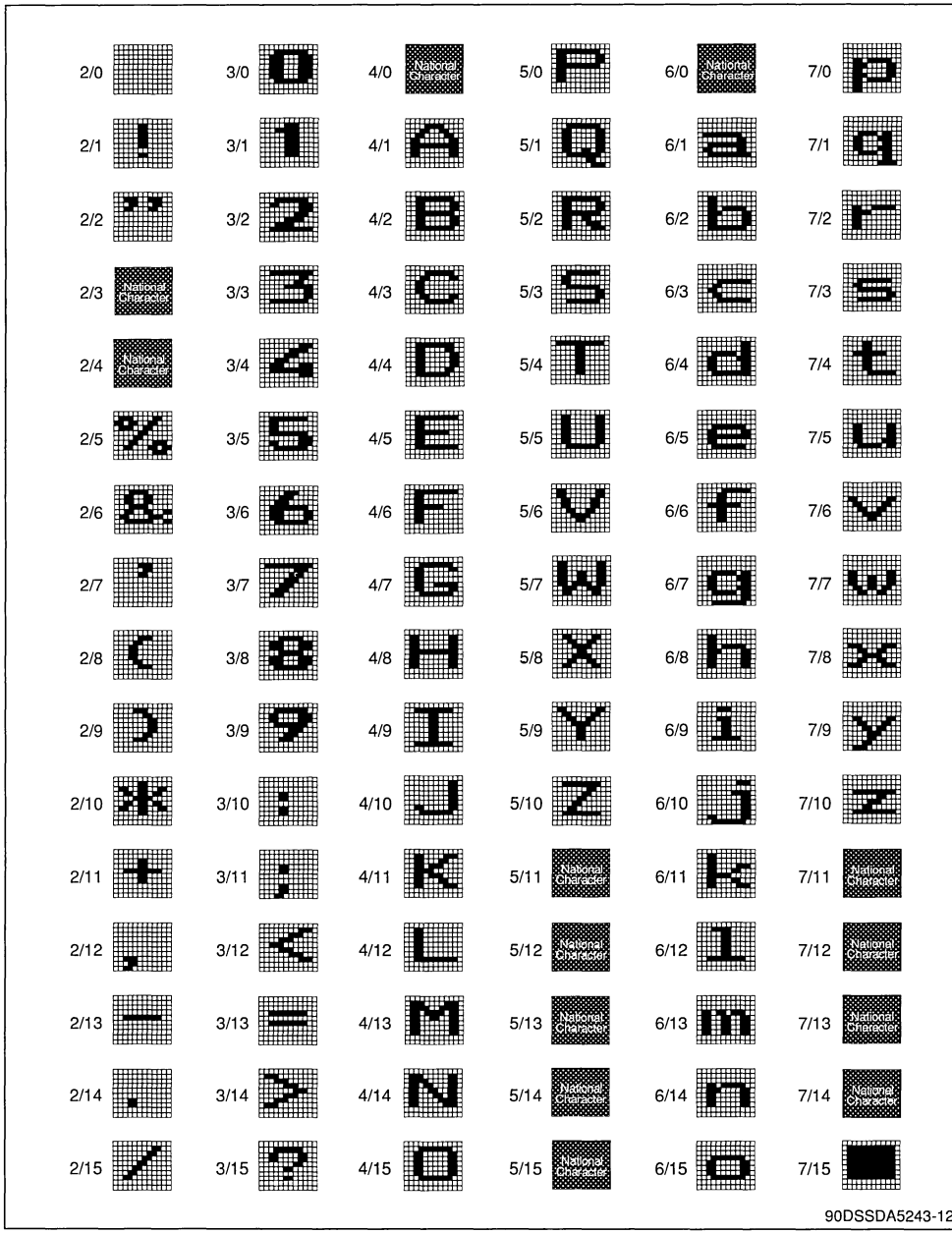
PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH	SPANISH
C12	0 (1) (1)	0	0	0	1	1
C13	0 (1) (1)	0	1	1	0	0
C14	0 (0) (1)	1	0	1	0	1

Table 4b : National character sets control bits for SDA5243/H

PHCB	POLISH	GERMAN	SWEDISH	SERBO-CROAT	CZECHOSLOVAK	RUMANIAN
C12	0	0 (0) (1)	0	1	1	1
C13	0	0 (1) (0)	1	0	1	1
C14	0	1 (1) (0)	0	1	0	1

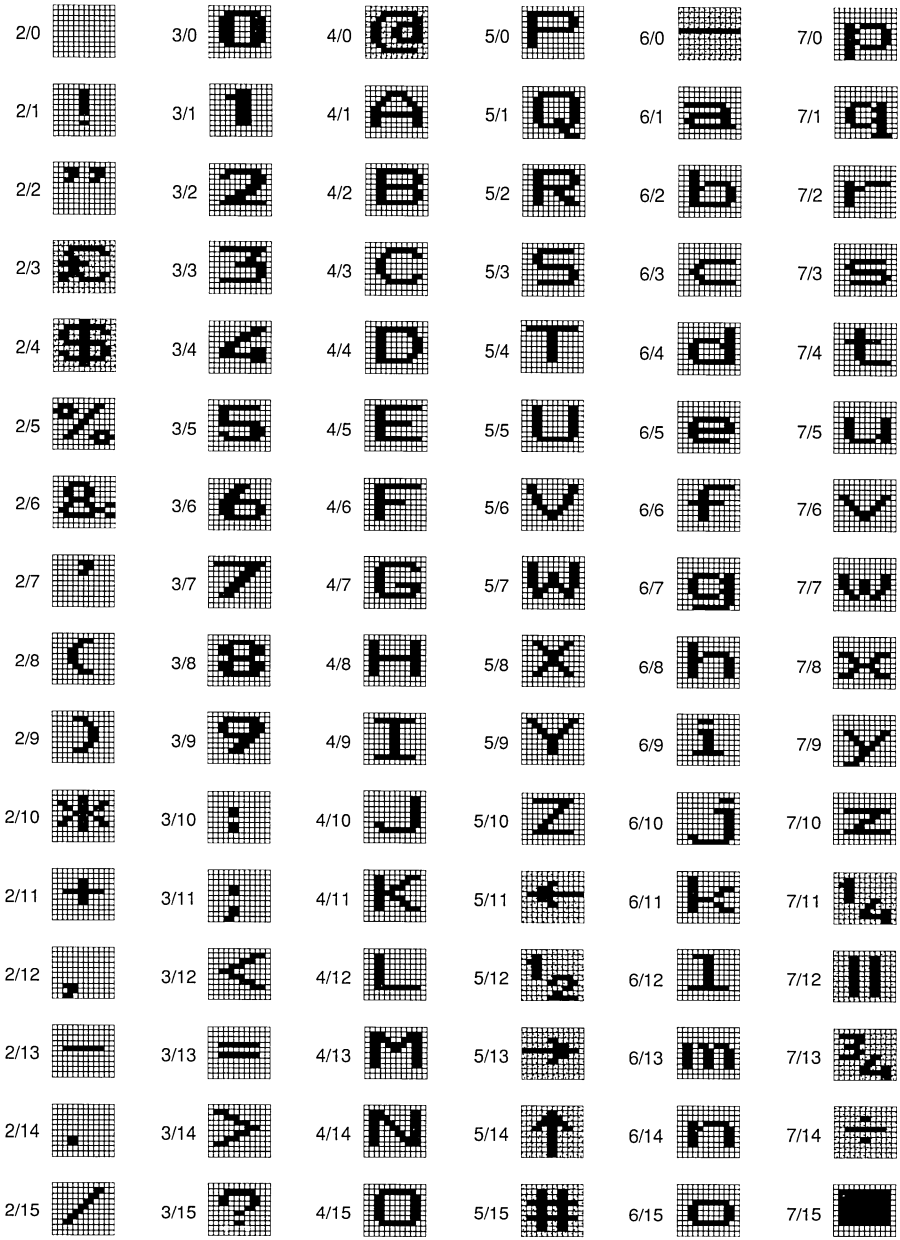
The basic set of the 96 characters is shown in Table 5.The location of the 13 national characters are shown in Table 5 whilst full national character sets are depicted in Tables 6 and 7.

Table 5 : Basic character set.



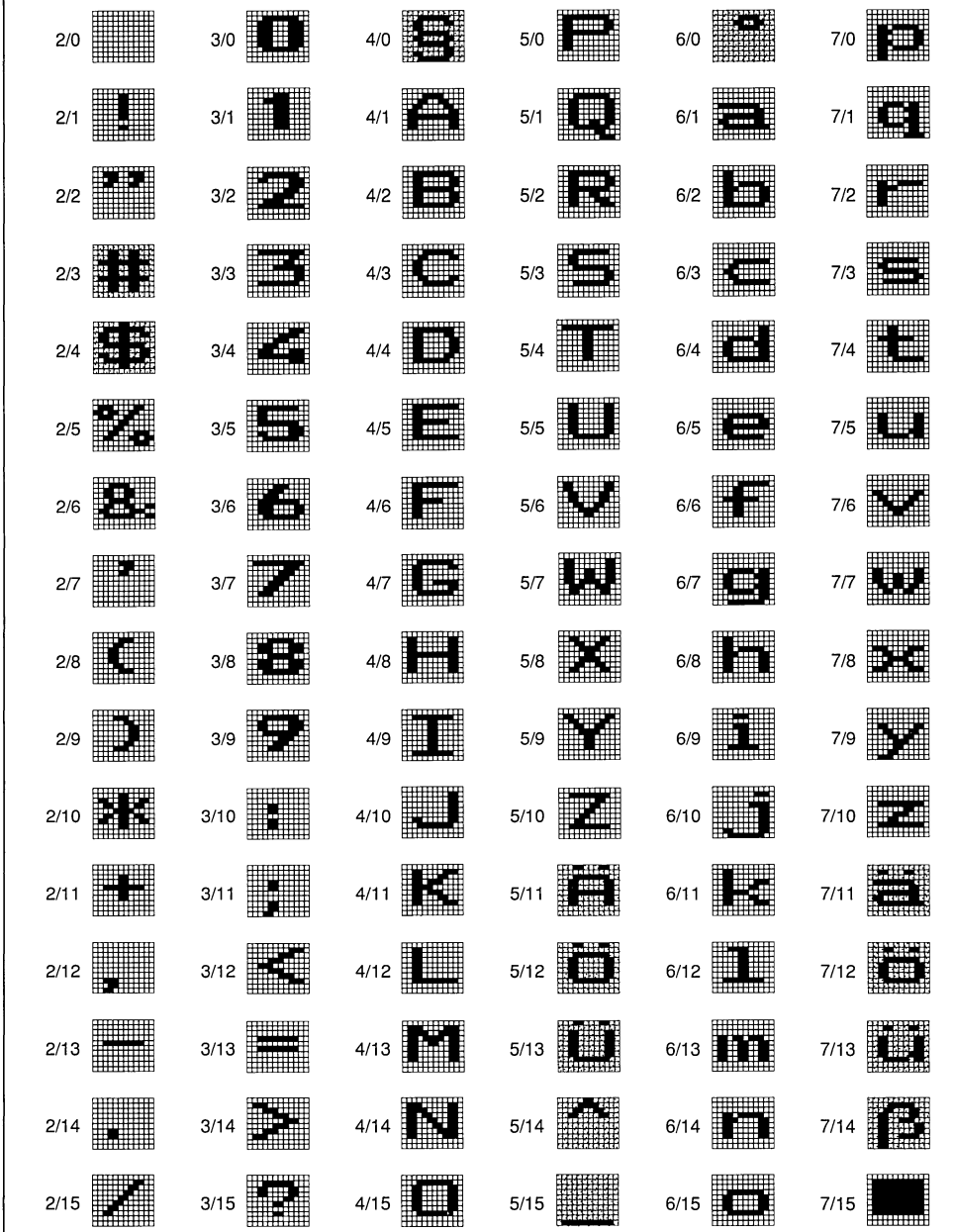
90DSSDA5243-12

Table 6a : English Basic Character Set for SDA5243 West European Languages



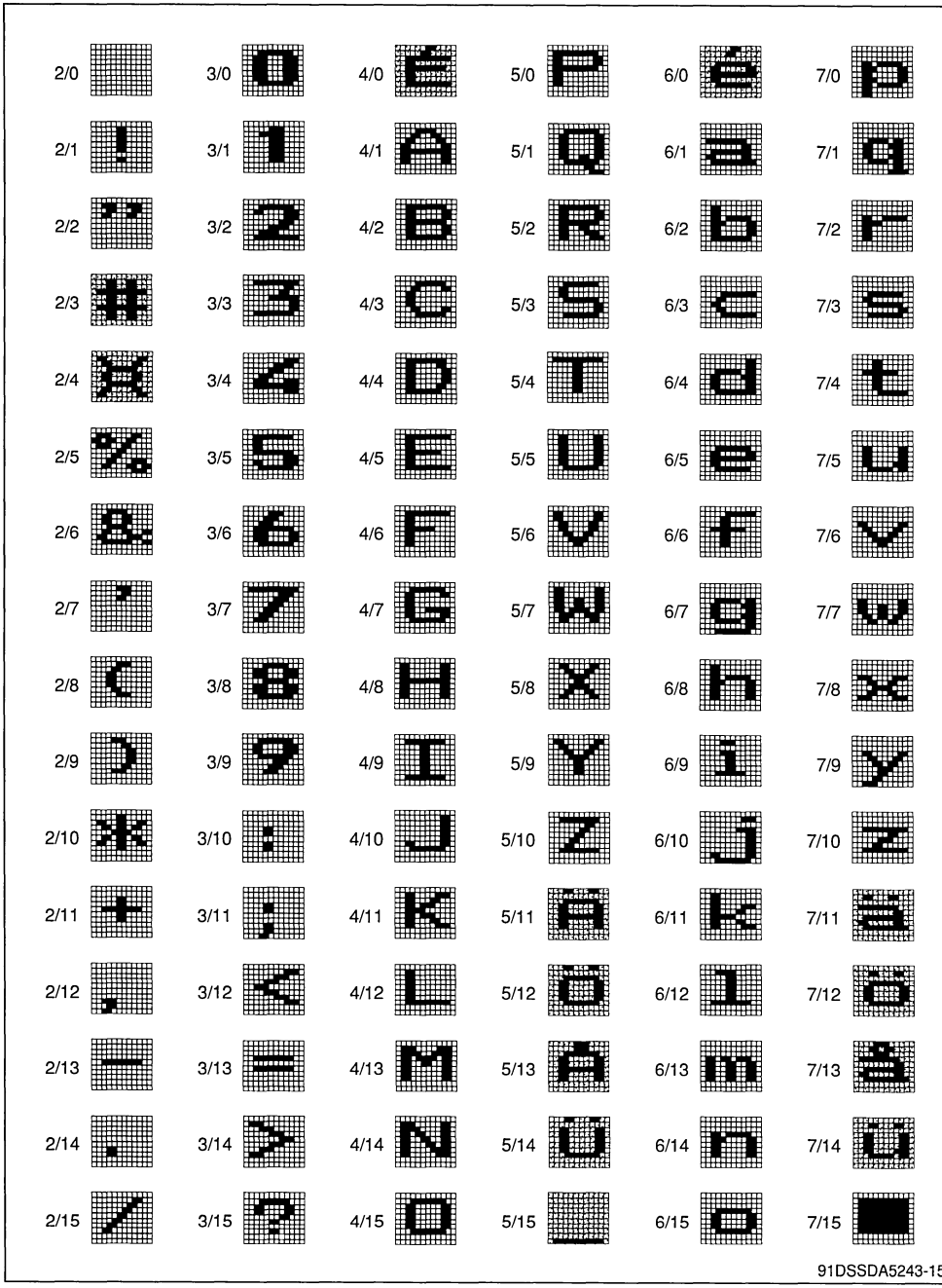
90DSSDA5243-13

Table 6b : German Basic Character Set for SDA5243 West European Languages



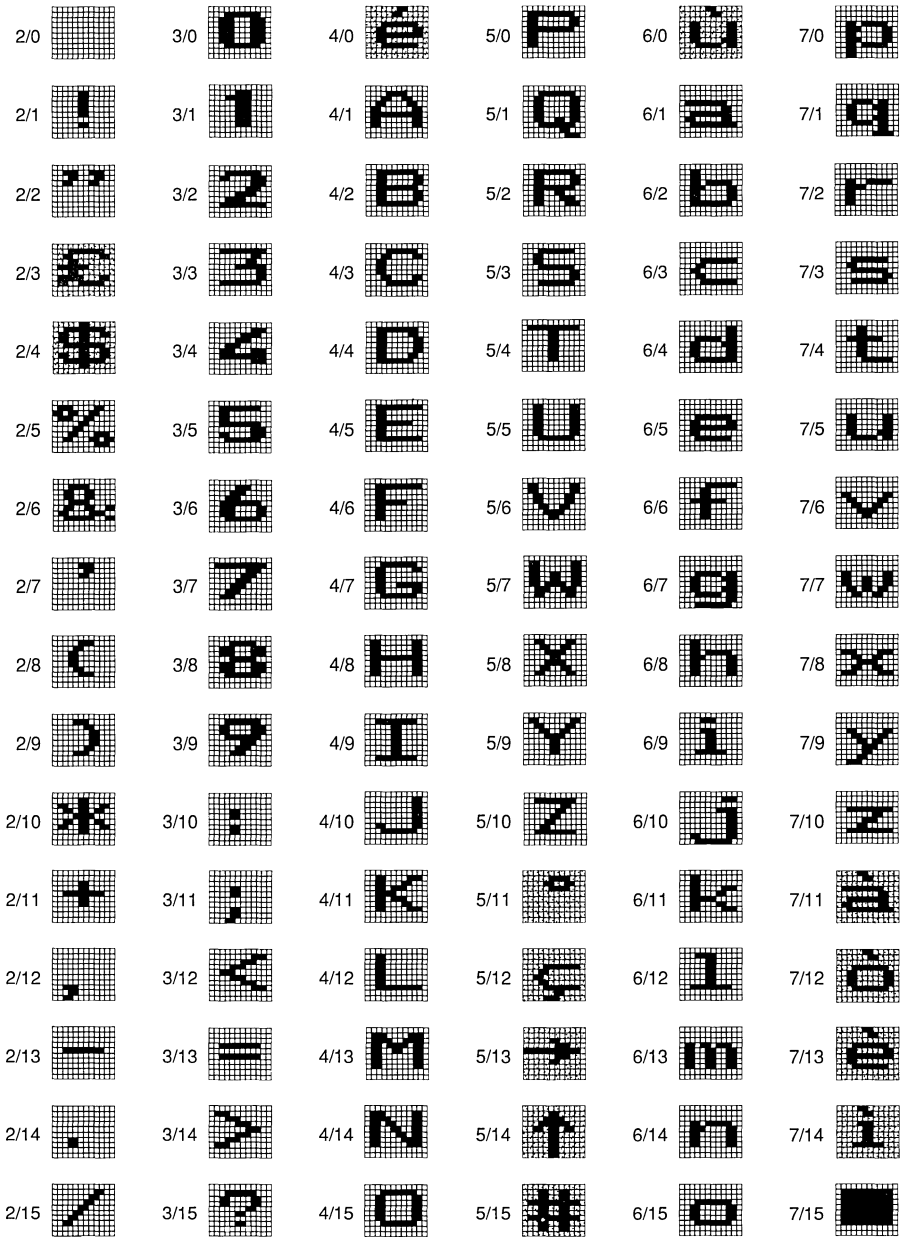
90DSSDA5243-14

Table 6c : Swedish Basic Character Set for SDA5243 West European Languages



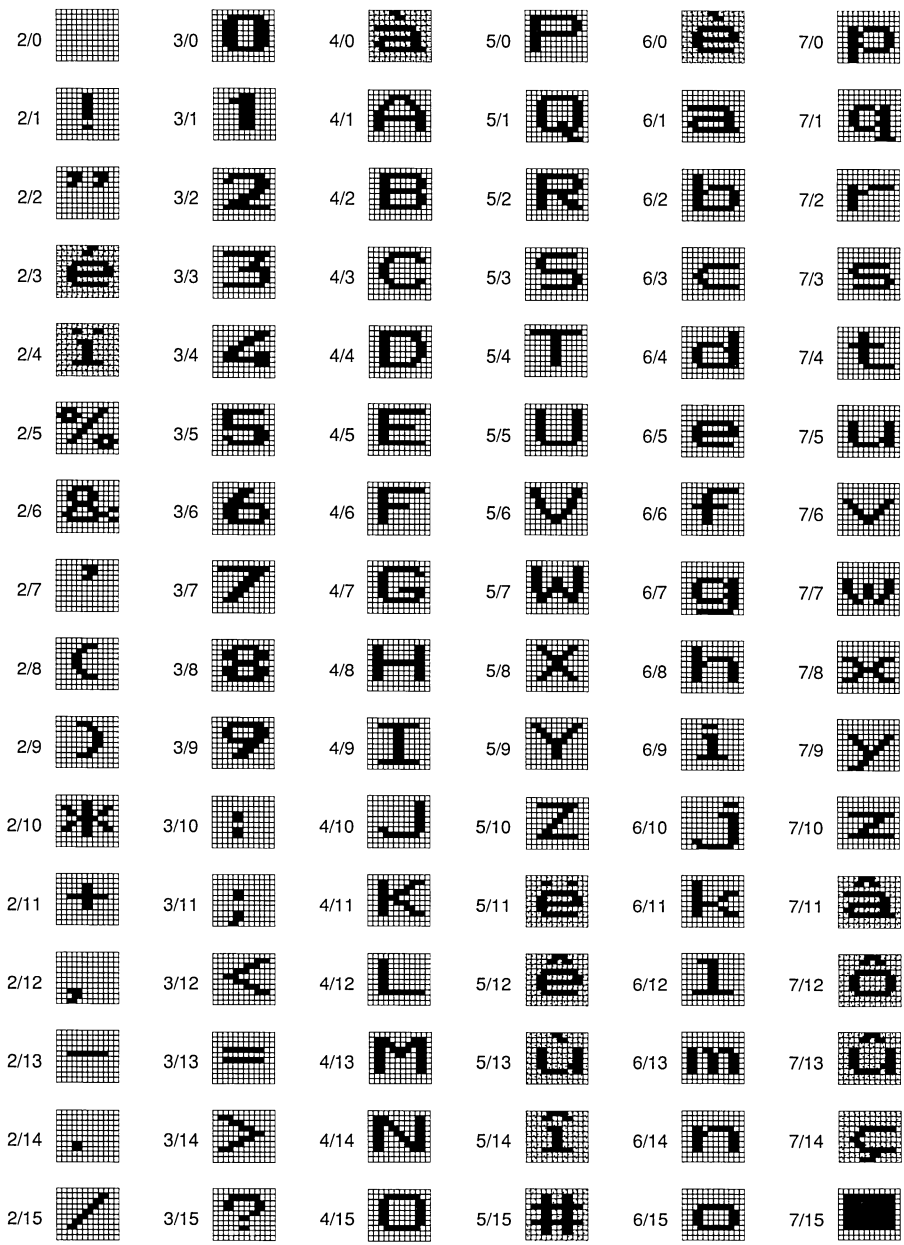
91DSSDA5243-15

Table 6d : Italian Basic Character Set for SDA5243 West European Languages



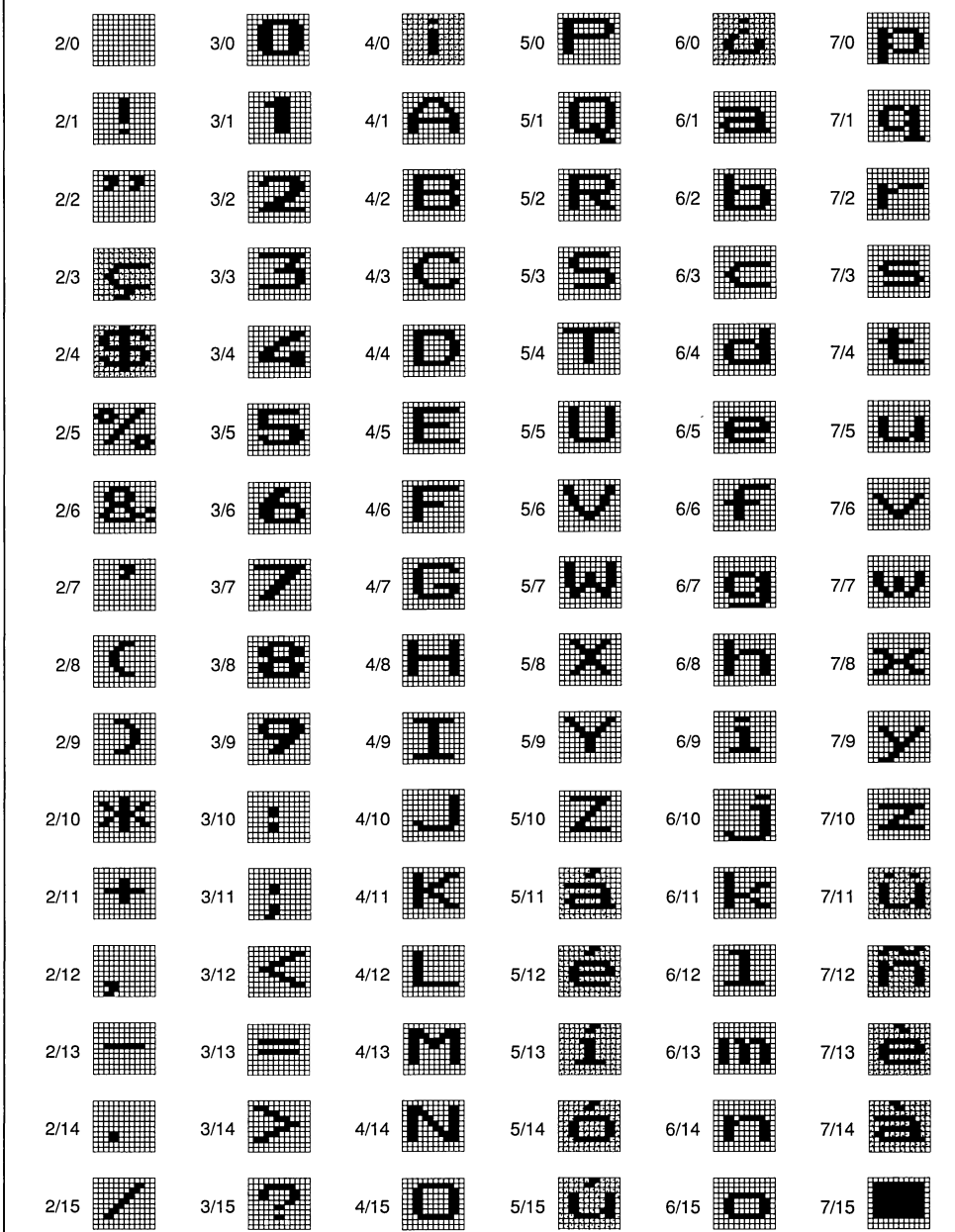
90DSSDA5243-16

Table 6e : French Basic Character Set for SDA5243 West European Languages



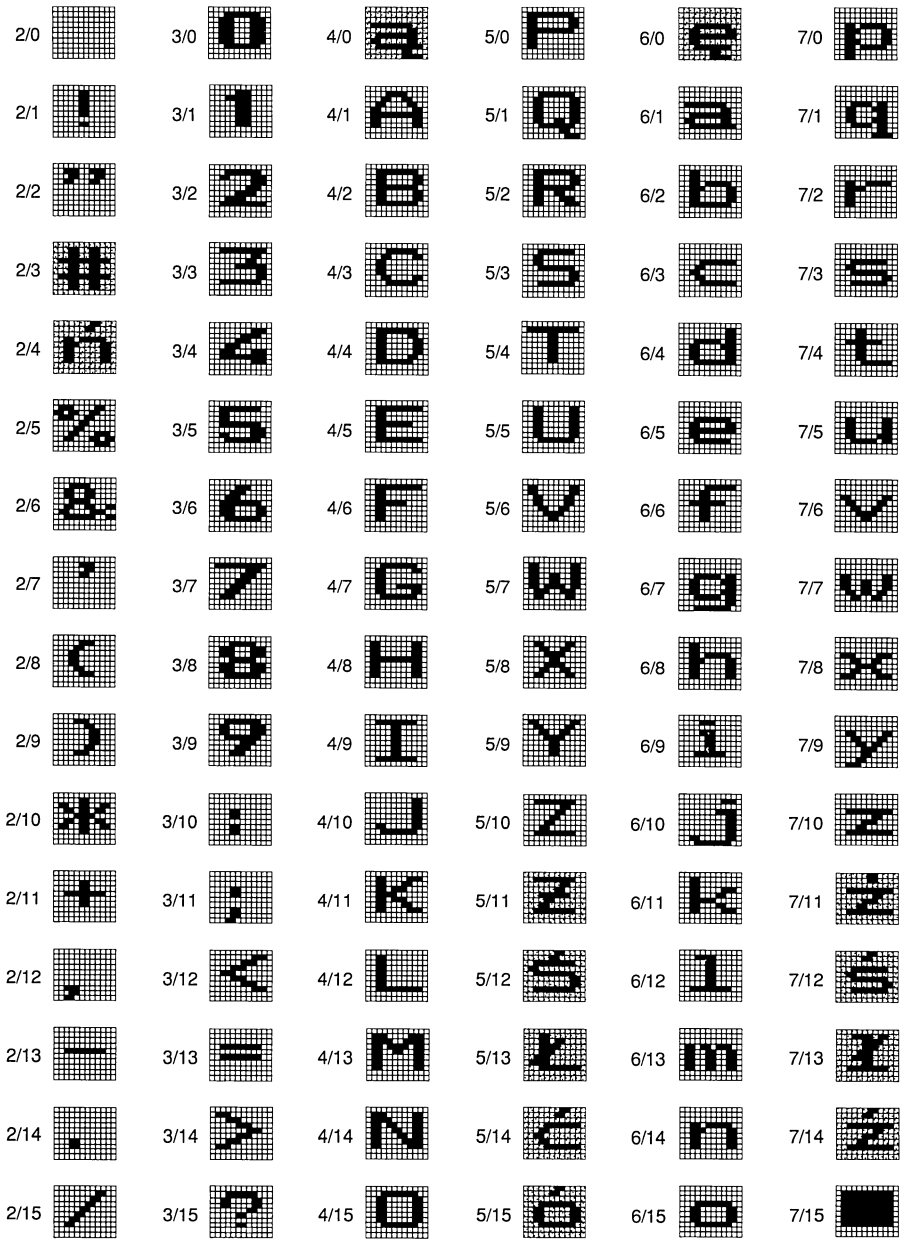
90DSSDA5243-17

Table 6f : Spanish Basic Character Set for SDA5243 West European Languages



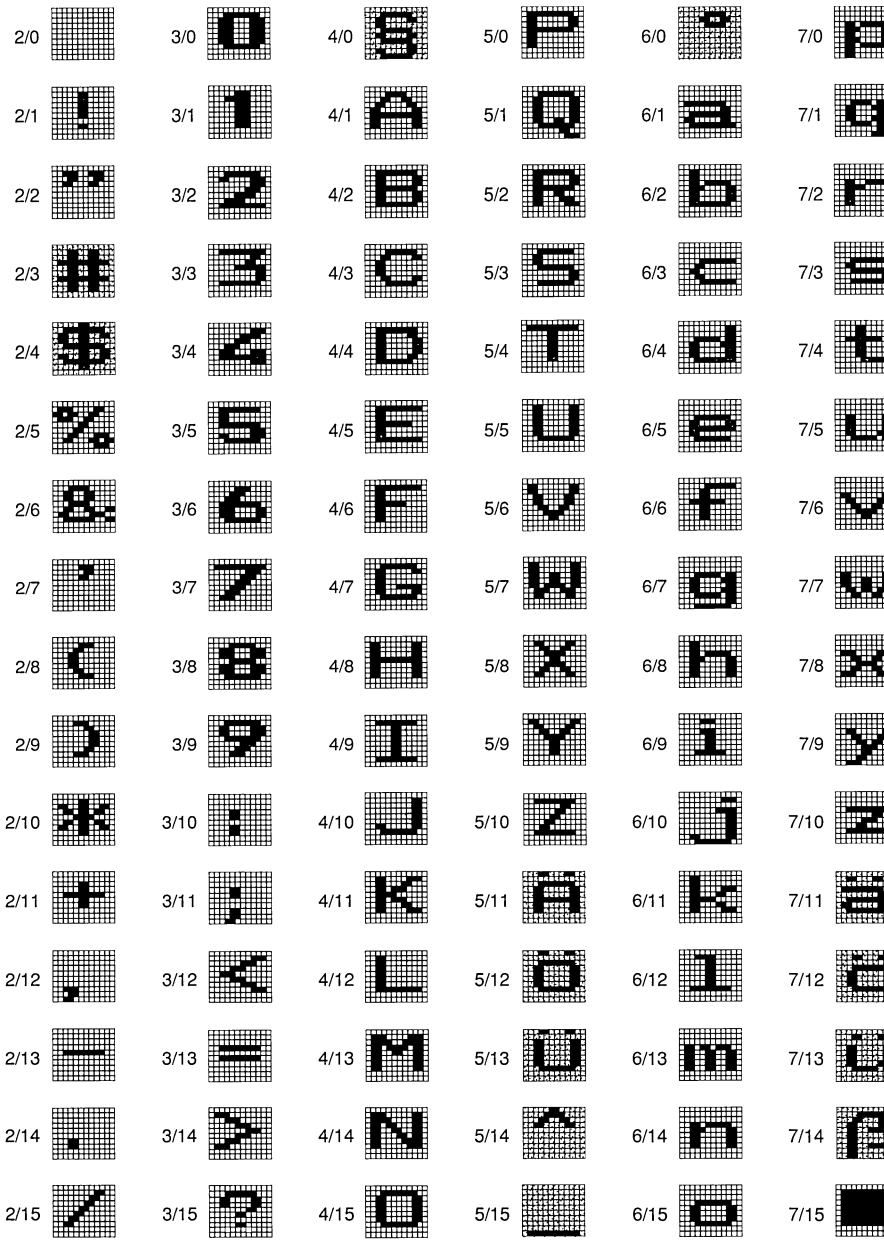
90DSSDA5243-18

Table 7a : Polish Basic Character Set for SDA5243/H East European Languages



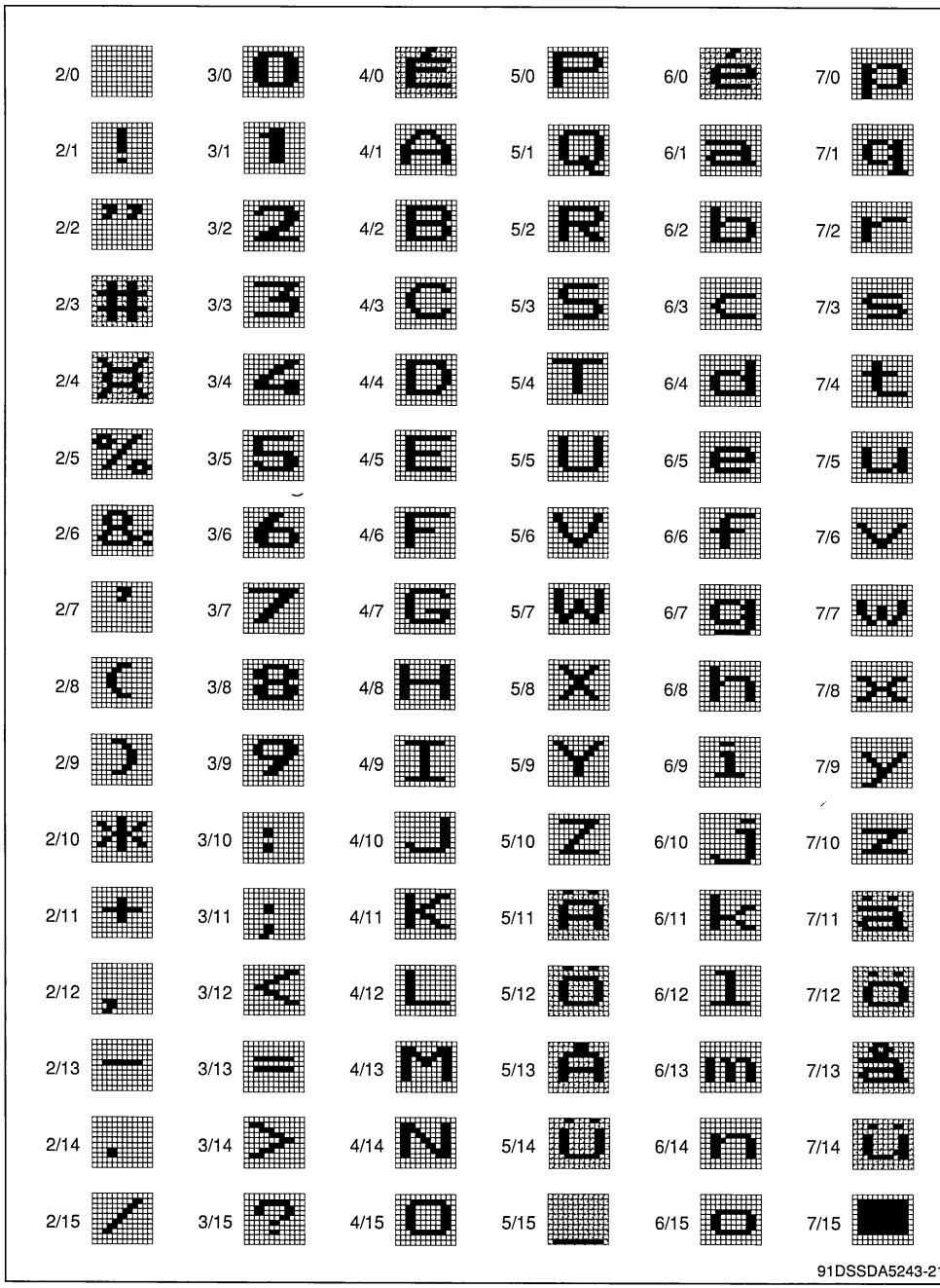
91DSSDA5243-19

Table 7b : German Basic Character Set for SDA5243/H East European Languages



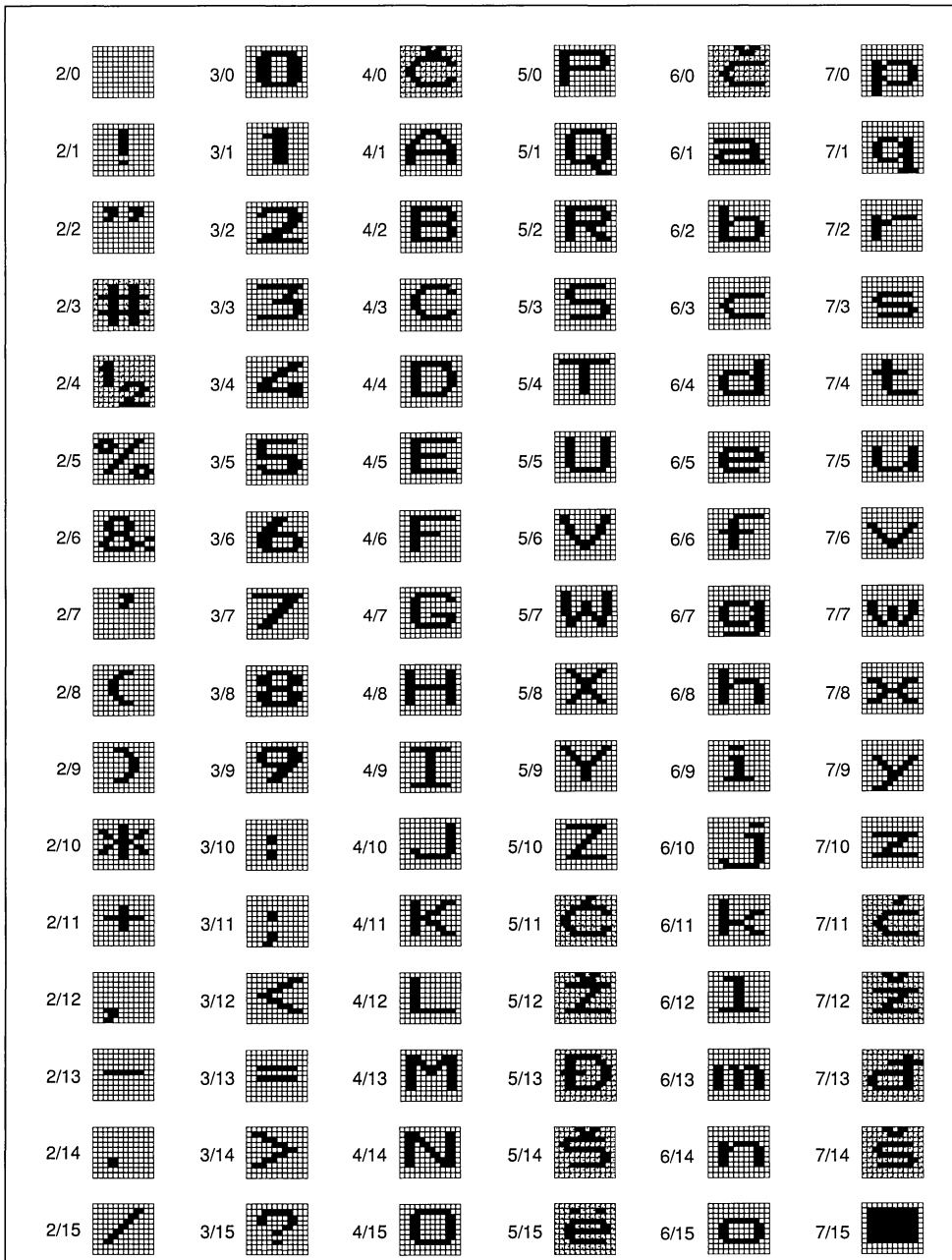
91DSSDA5243-20

Table 7c : Swedish Basic Character Set for SDA5243/H East European Languages



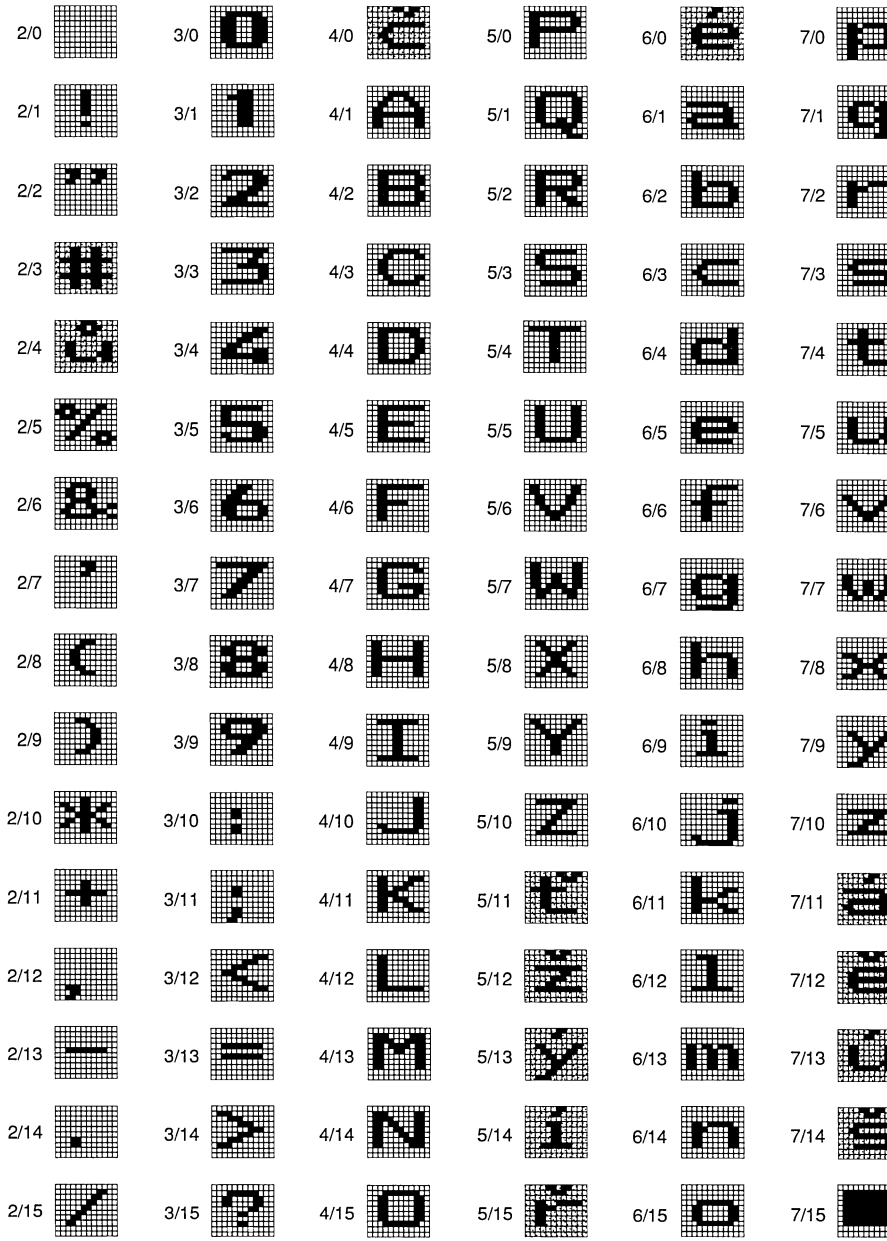
91DSSDA5243-21

Table 7d : Serbo-croat Basic Character Set for SDA5243/H East European Languages



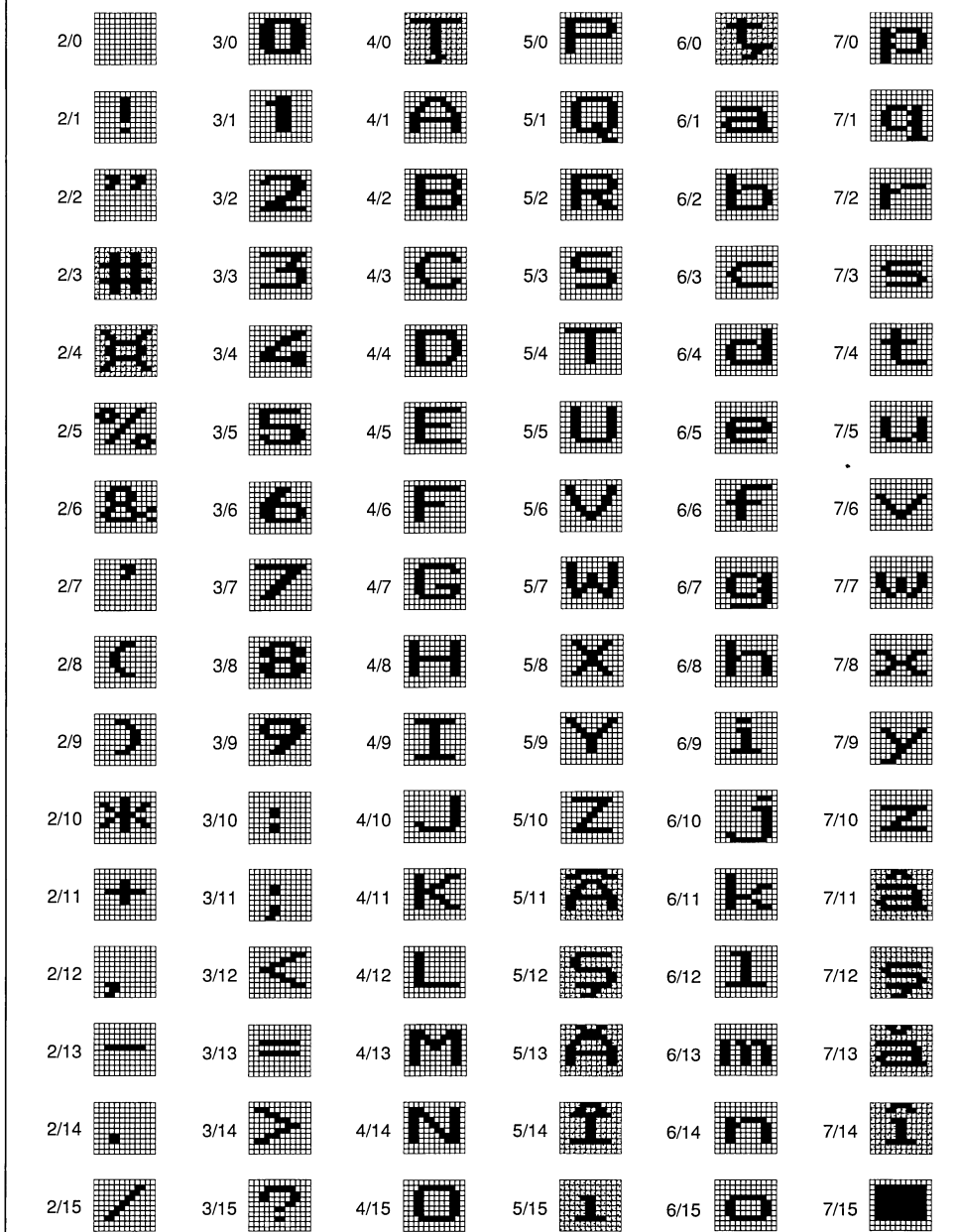
91DSSDA5243-22

Table 7e : Czechoslovak Basic Character Set for SDA5243/H East European Languages



91DSSDA5243-23

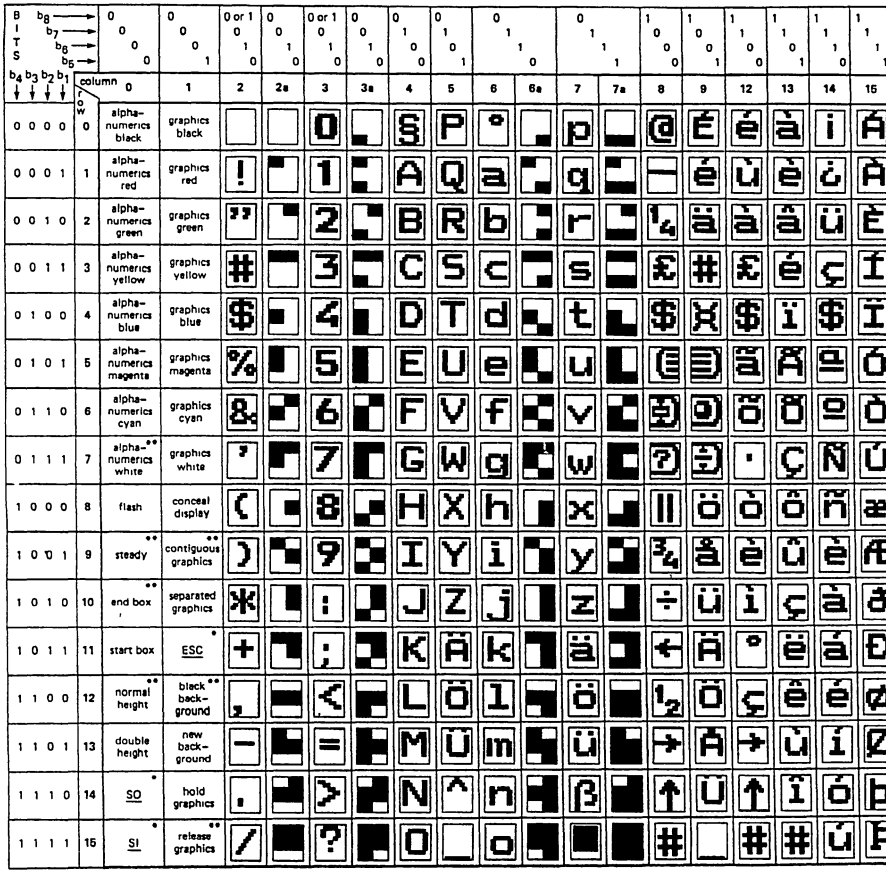
Table 7f : Rumanian Basic Character Set for SDA5243/H East European Languages



91DSSDA5243-24

The complete character set with 8-bit decoding is given in Table 8.
Characters in columns 0 and 1 are normally displayed as blanks. Black dots represent the character shape whereas white dots represent the background.
Each character can be identified by a pair of corresponding row and column integers : for example the character "3" may be indicated by 3/3.
A rectangle may be represented as follows : ▭
The characters 8/6, 8/7, 9/5, 9/7 are used as special characters, always in conjunction with 8/5.
The 13 national characters are placed in columns with bit 8 = 0.

Table 8a: Complete character set (with 8 bit codes) - West European Languages

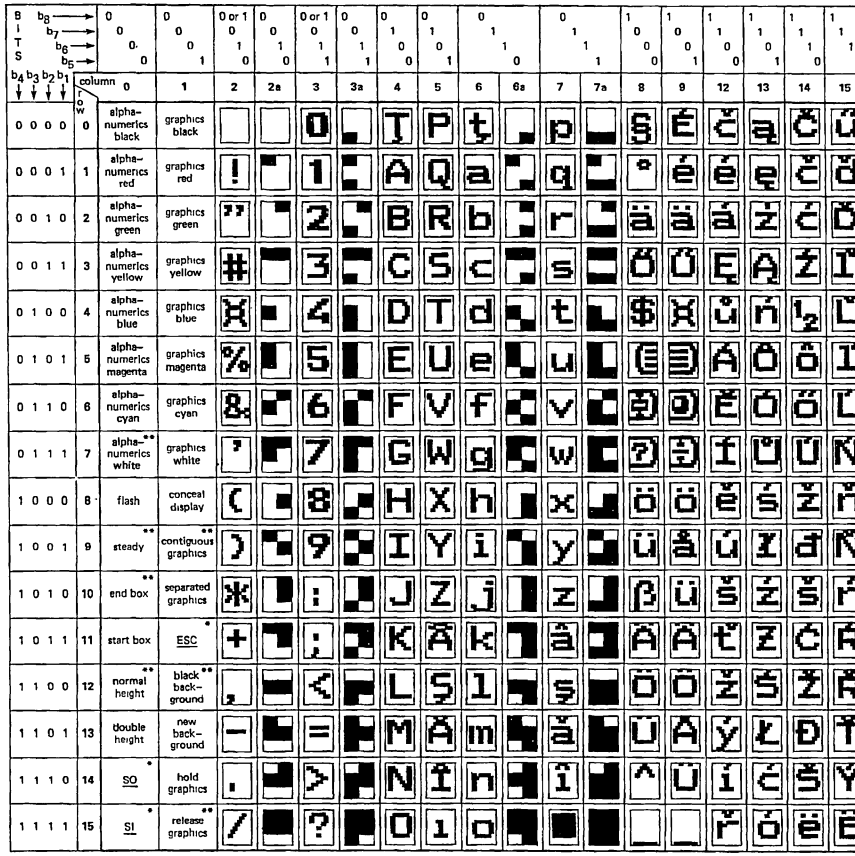


Case using C12 C13 C14 = 001 (German Set)

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins

89DSSDA5243-25

Table 8b: Complete character set (with 8 bit codes) - East European Languages

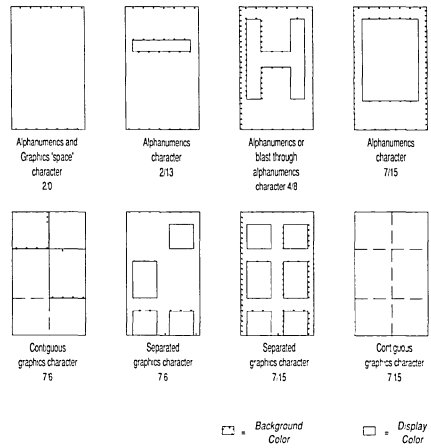


Case using C12 C13 C14 = 111 (Rumanian Set)

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins

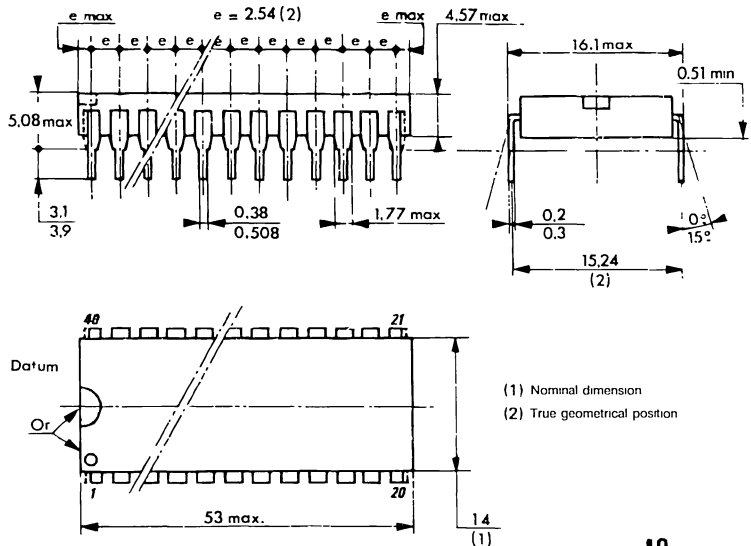
91DSSDA5243-26

Figure 12: Character Format



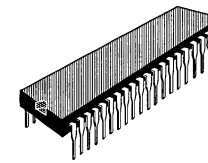
91DSSDA5243-27

PACKAGE MECHANICAL DATA : 40 PINS - PLASTIC DIP



COMPUTER-CONTROLLED TELETEXT DECODER

- AUTOMATIC SELECTION OF UP TO SEVEN NATIONAL LANGUAGES
- FOUR SIMULTANEOUS PAGE REQUESTS
- DISPLAY OF THE 25th STATUS ROW
- MICROPROCESSOR CONTROL VIA AN I^2C BUS INTERFACE (SLAVE ADDRESS 0010001 R/$\overline{W}$)
- DATA ACQUISITION AVAILABLE FROM ROWS 2 TO 22 OR FROM A COMPLETE FIELD
- HIGH QUALITY DISPLAY USING A CHARACTER MATRIX OF 12 x 10 DOTS
- DIRECT INTERFACE TO ONE 8-BIT x 8K STATIC MEMORY A TWO 4-BIT x 16K DYNAMIC MEMORIES
- 60Hz RECOGNITION AND INSERTION WITHOUT ADDITIONAL HARDWARE
- FIELD RECOGNITION FOR NOT-INTERLACED MODE AND 25Hz OUTPUT
- VIDEO SIGNAL QUALITY STATUS BIT
- EXTERNAL SYNCHRONIZATION BY H/V TV SIGNALS
- SINGLE +5V SUPPLY VOLTAGE
- NMOSH2 PROCESS



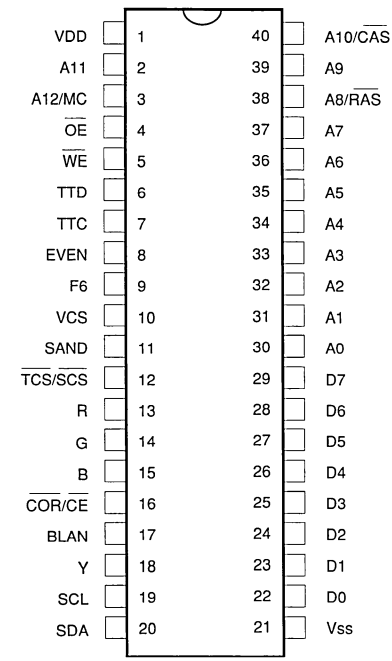
DIP40
(Plastic Package)

ORDER CODE : SDA5343

DESCRIPTION

The SDA5343 is a NMOSH2 integrated circuit which performs all the processing of logical data within a 625 line system teletext decoder. It is designed to operate in conjunction with at less two chips : the SAA5231 integrated chip which extracts Teletext information embedded in a composite video signal and with up to eight kilobytes of static or dynamic RAM memory which can be used to store a maximum of 8 pages of display data. A complete system also comprises a microprocessor controlling the SDA5343 via a 2-wire serial bus. An on-chip ROM memory contains the character sets. The SDA5343 performs automatic selection of one of up to seven natural languages making the system suitable for the display of text in English, German, Swedish, French, Italian and Spanish. Data bytes may be decoded in either 7-Bit plus parity or in full 8-Bit formats. The chip set also supports facilities for reception and display of higher-level protocol data.

PIN CONNECTIONS

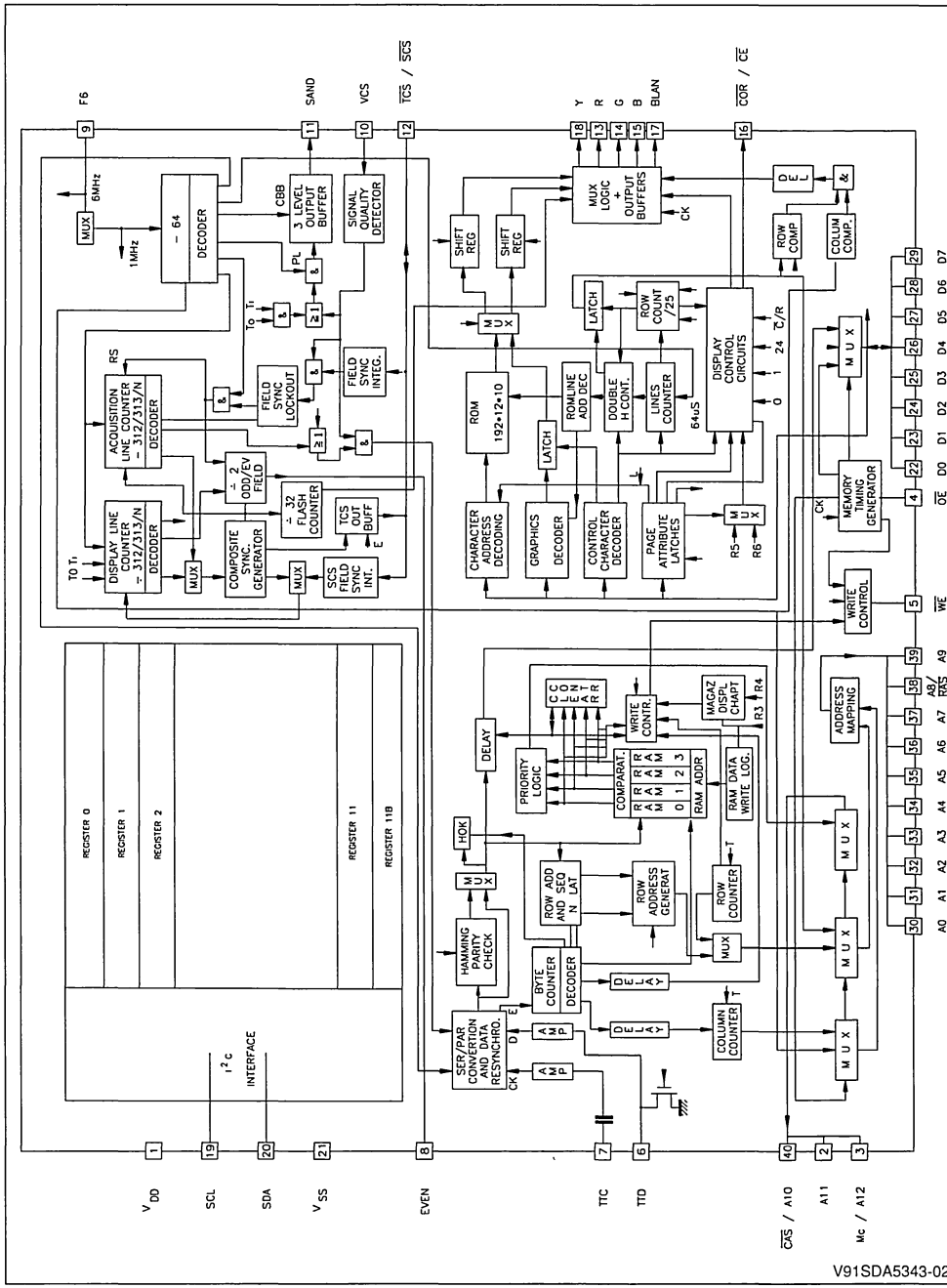


V91SDA5343-01

PIN DESCRIPTION

Symbol	Function	Description
V_{DD}	+ 5V	Positive supply voltage.
A11, A12, A10	Chapter address	Address selection outputs for 1 of 8 chapters each of 1 kBytes.
$\overline{OE}$	Output enable	Active-low RAM output enable control signal.
$\overline{WE}$	Write enable	Active-low RAM write enable control signal. It supports write-cycles interleaved with read-cycles.
TTD	Teletext data input	An A.C. coupled teletext data input supplied by the SAA5231 chip is latched to V_{SS} between 4 and 8µs after each TV line.
TTC	Teletext clock input	A 6.9375MHz clock signal, supplied by the SAA5231 chip, is internally A.C. coupled, clamped and buffered.
EVEN	Interlaced mode state output	High for even numbered and low for odd-numbered frames.
F6	Character display clock signal	The 6MHz clock signal, supplied by the SAA5231 chip is internally A.C. coupled, clamped and buffered.
VCS	Video composite synchronization input signal	Active high VCS input.
SAND	Sandcastle	Three level output pulse to the SAA5231 device. Phase lock, blanking signal, and color burst components are contained in this signal.
$\overline{TCS}$ / $\overline{SCS}$	Input composite synchronization signal	Scan composite input signal ($\overline{SCS}$) for the display synchronization.
RGB	Red, green, blue	Character and background colors active-high open-drain outputs.
$\overline{COR}/\overline{CE}$	Contrast reduction	Open-drain active-low output supporting optimal display of characters in "mixed mode" operation. Chip enable for dynamic memory with 8-Bit configuration I^2C bus programmable.
BLAN	Blanking signal output	Open-drain active high output for TV-image blanking in normal and mixed-mode operation.
Y	Foreground output	Open-drain active-high output with foreground information. Can be used for printer command.
SCL	Serial clock	Microprocessor clock input via serial bus.
SDA	Serial data input / output	Open-drain microprocessor serial data input/output via serial bus.
V_{SS}	0 Volt	Ground.
D0 - D7	Parallel data input / output	Eight tri-state input/output for data read/write
A0 - A9	Address signals	Ten addresses output pins for accessing to individual Bytes of a 1 kByte chapter stored in an external SRAM / PSRAM and DRAM (only A0 - A7)
MC	Address multiplying control	If MC (Pin 3) is grounded, addresses are multiplexed for dynamic RAM's use.
$\overline{RAS}$, $\overline{CAS}$	Address control	Address control for dynamic RAM's - Active low.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Range	- 0.3 to + 7.5	V
INPUT VOLTAGE RANGE			
V_I	VCS, SDA, SCL, D0 - D7 TTD, F6, $\overline{TCS}$ / SCS, TTC	- 0.3 to + 7.5 - 0.3 to + 10	V V
OUTPUT VOLTAGE RANGE			
V_O	SAND, A0 - A12, $\overline{OE}$, $\overline{WE}$, D0 - D7, $\overline{ODD}$ / EVEN, R, G, B, BLAN, $\overline{COR}$ / $\overline{CE}$, Y $\overline{TCS}$ / SCS	- 0.3 to + 7.5 - 0.3 to + 10	V V
T_{stg}	Storage Temperature Range	- 20 to + 125	°C
T_{oper}	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage (pin 1)	4.5	5	5.5	V
I_{DD}	Supply Current		130	190	mA
INPUTS					
	TTD				
C_{EXT}	Ext. Coupling Capacitor			50	nF
$V_{I(p-p)}$	Input Voltage p-p	2		7	V
t_r , t_f	Input Rise / Fall Times	10		80	ns
t_{DS}	Input Set-up Time	40			ns
t_{DH}	Input Hold Time	40			ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to 10V)			20	µA
C_I	Input capacitance			7	pF
	TTC, F6				
V_I	Input Voltage Range	- 0.3		+10	V
$V_{I(p-p)}$	AC Input Voltage F6 AC Input Voltage TTC	1 1.5		7 7	V V
± V_P	Input Peak Rel. 50 % Duty	0.2		3.5	V
f_{TTC}	TTC Clock Frequency	4	6.9375	8	MHz
f_{F6}	F6 Clock Frequency	4	6	8	MHz
t_r , t_f	Clock Rise / Fall Times	10		80	ns
$I_{I(L)}$	Input Leakage Current (VI = 0 to 10V)			20	µA
C_I	Input Capacitance			7	pF
	VCS				
V_{IL} V_{IH}	Input Voltage : • Low Level • High Level	 0 2		 0.8 V_{DD}	V
t_r , t_f	Input Rise / Fall Times			500	ns
$I_{I(L)}$	Input Leakage Current (VI = 5.5V)			10	µA
C_I	Input Capacitance			7	pF

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
INPUTS (continued)					
	SCL				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 3		 1.5 V_{DD}	V
f_{SCL}	SCL Clock Frequency			100	kHz
t_r , t_f	Input Rise / Fall Times			2	µs
$I_{I(L)}$	Input Leakage Current (VI = 5.5V)			10	µA
C_I	Input Capacitance			7	pF
	$\overline{TCS}$, $\overline{SCS}$				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 3.5		 1.5 8	V
t_r , t_f	Input Rise / Fall Times			500	ns
± $I_{I(L)}$	Input Leakage Current (VI = 0 to10V and output in high impedance state)			10	µA
C_I	Input Capacitance			7	pF
INPUT/OUTPUTS					
	SDA				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 3		 1.5 V_{DD}	V
t_r , t_f	Input Rise / Fall Times			2	µs
$I_{I(L)}$	Input Leakage Current (VI = 5.5V with output off)			10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Output Voltage (IOL = 3mA)	0		0.5	V
t_f	Output Fall Time between 3.0V and 1.0V			200	ns
C_I	Load Capacitance			400	pF
	D0-D7				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 2		 0.8 V_{DD}	V
± $I_{I(L)}$	Input Leakage Current (VI = 0 to 5.5V and output in high impedance state)			10	µA
C_I	Input Capacitance			7	pF
V_{OL} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 1.6mA) ● High Level (-I_{OH} = 0.2mA)	 0 2.4		 0.4 V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V			50	ns
C_I	Load Capacitance			120	pF

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
OUTPUTS					
	A0-A12, $\overline{OE}$, $\overline{WE}$, ($\overline{RAS}$), ($\overline{CAS}$), $\overline{CE}$*				
V_{OL} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 1.6mA) ● High Level (-I_{OH} = 0.2mA)	 0 2.4		 0.4 V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V			50	ns
C_L	Load Capacitance			120	pF
	EVEN				
V_{OL} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 0.4mA) ● High Level (-I_{OH} = 0.2mA)	 0 2.4		 0.4 V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V			100	ns
C_L	Load Capacitance			50	pF
	SAND				
V_{OL} V_{OI} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 0.2mA) ● Middle Level (I_{OL} = ± 10 µA) ● High Level (I_{OH} = 0/- 10µA)	 0 1.1 4		 0.25 2.9 V_{DD}	V
t_{r1} t_{r2}	Output Rise Time : ● V_{OL} to V_{OI} from 0.4 to 1.1V ● V_{OI} to V_{OH} from 2.9 to 4.0V			 400 200	ns
t_f	Output Fall Time VOH to V_{OI} from 4.0 to 0.4V			50	ns
C_I	Load Capacitance			30	pF
	R, G, B, $\overline{COR}$, BLAN, Y - (Open drain outputs)				
V_{OL}	Low Level Output Voltage : ● I_{OL} = 2mA ● I_{OL} = 5mA	 0 0		 0.4 1	V
V_{PU}	Pull-up Voltage (with R = 1kΩ to 5V)			5	V
t_f	Output Fall Time from 4.5 to 1.5V (with R = 1kΩ to 5V)			20	ns
t_{SK}	Skew Delay on Falling Edges (at 3V with R = 1kΩ connected to 5V)			20	ns
C_L	Load Capacitance			25	pF
I_{LO}	Output Leakage Current (VPU = 0 to 6V output off)			20	µA
TIMING					
	SERIAL BUS (referred to V_{IH} = 3V, V_{IL} = 1.5V)				
t_{LOW} t_{HIGH}	Clock : ● Low Period ● High Period	 4 4			µs
t_{SU} , d_{AT} t_{HD} , d_{AT}	Data Set-up Time Data Hold Time	250 170			ns ns
t_{SU} , s_{TO}	Stop Set-up Time from Clock High	4			µs
t_{BUF}	Start Set-up Time Following a Stop	4			µs
t_{HD} , s_{TA} t_{SU} , s_{TA}	Start Hold Time Start Set-up Time Following Clock Low to High Transition	4 4			µs µs

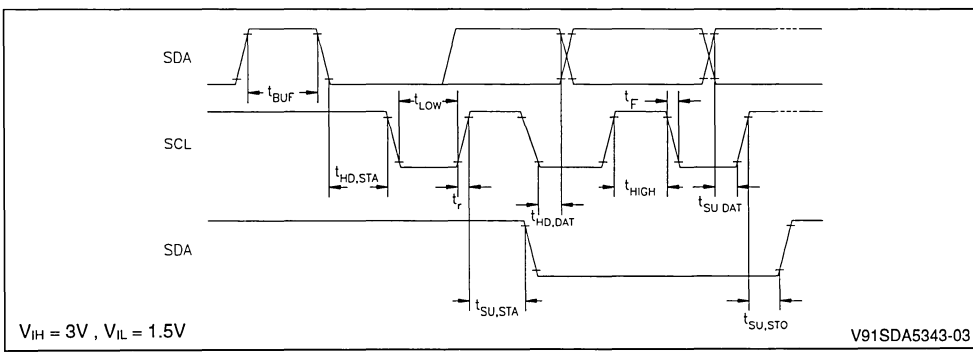
* ($\overline{RAS}$) ($\overline{CAS}$) valid if Pin 3 is grounded.

ELECTRICAL CHARACTERISTICS (continued)

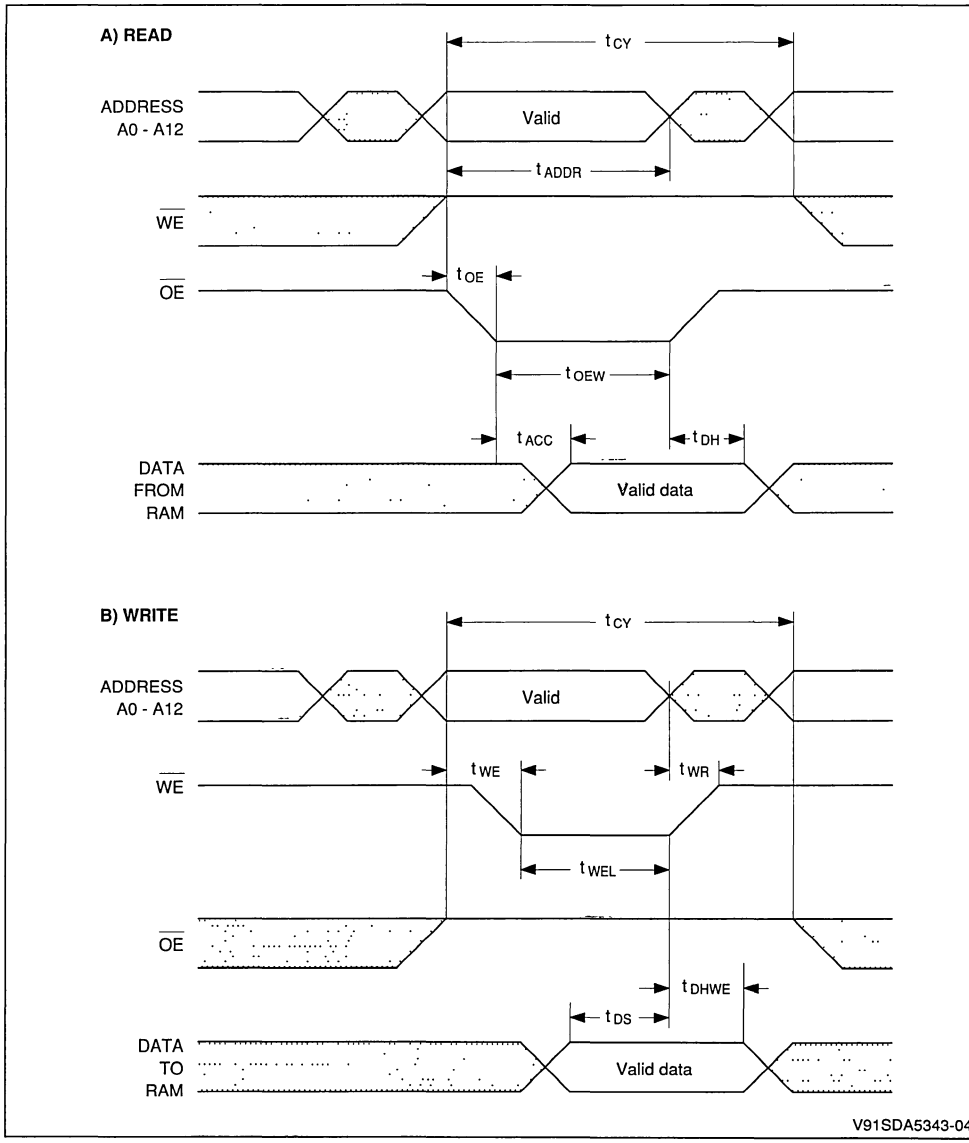
V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
TIMING (continued)					
	STATIC MEMORY INTERFACE (referred to V_{IL} = 1.5V)				
t_{CY}	Cycle Time		500		ns
t_{OE}	Adress Change to $\overline{OE}$ Low	60			ns
t_{ADDR}	Address Active Time	450	500		ns
t_{OEW}	$\overline{OE}$ Pulse Duration	320			ns
t_{ACC}	Access Time from $\overline{OE}$ to Data Valid			200	ns
t_{DH}	Data Hold Time from $\overline{OE}$ High or Address Change	0			ns
t_{WE}	Address Change to $\overline{WE}$ Low	40			ns
t_{WEL}	$\overline{WE}$ Pulse Duration	200			ns
t_{DS}	Data Set-up Time to $\overline{WE}$ High	100			ns
t_{DHWE}	Data Hold Time from $\overline{WE}$ High	20			ns
t_{WR}	Write Recovery Time	25			ns
	DYNAMIC RAM MEMORY INTERFACE - Read				
t_{RC}	Read Cycle Time	450			ns
t_{RAS}	$\overline{RAS}$ Pulse Width	320			ns
t_{ASR}	Row Address Set up Time (A0 - A6)	40			ns
t_{ASC}	Column Address Set up Time (A0 - A7)	40			ns
t_{RDC}	Delay Time, $\overline{RAS}$ low to $\overline{CS}$ low		160		ns
t_{CAC}	Access Time from $\overline{CAS}$			100	ns
t_{OEW}	$\overline{OE}$ Pulse Width	320			ns
	DYNAMIC RAM MEMORY INTERFACE - Write				
t_{RC}	Write Cycle Time	450			ns
t_{RAS}	$\overline{RAS}$ Pulse Width	320			ns
t_{ASR}	Row Address Set up Time	40			ns
t_{ASC}	Column Address Set up Time	40			ns
t_{RDC}	Delay Time, $\overline{RAS}$ low to $\overline{CS}$ low		160		ns
t_{WCS}	Write Set up Time		160		ns
t_{DS}	Data Set up Time		160		ns

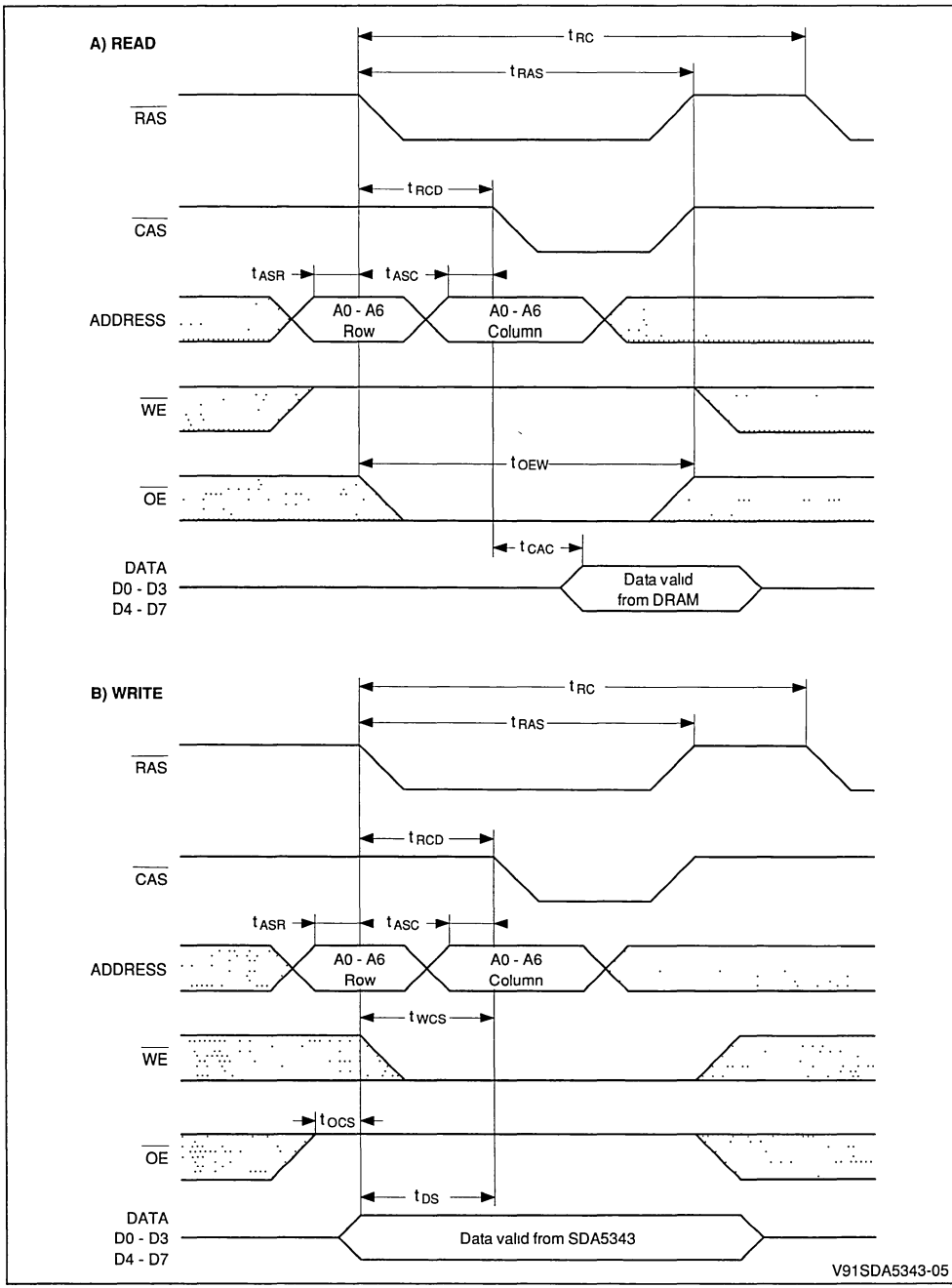
SERIAL BUS TIMING



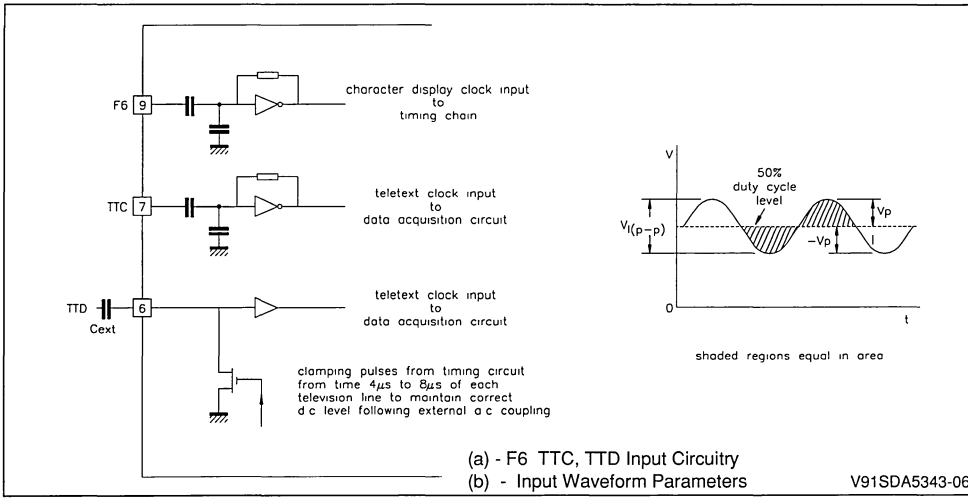
STATIC RAM MEMORY INTERFACE TIMING



DYNAMIC RAM MEMORY INTERFACE TIMING



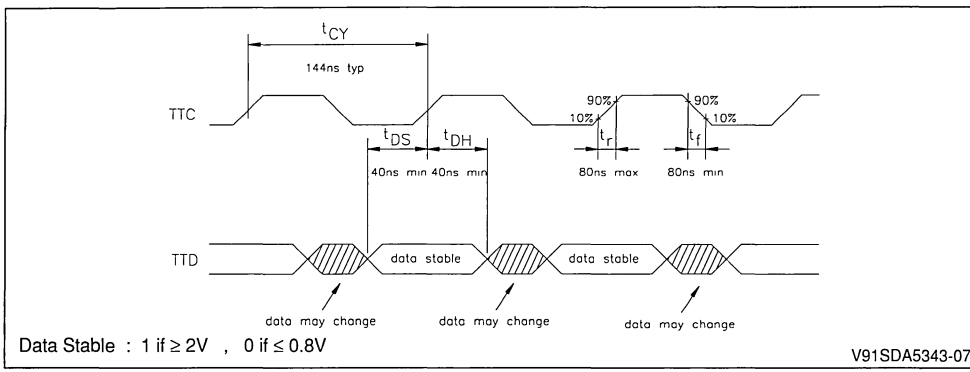
F6, TTC, TTD INPUT INTERNAL CONNECTIONS



(a) - F6 TTC, TTD Input Circuitry
(b) - Input Waveform Parameters

V91SDA5343-06

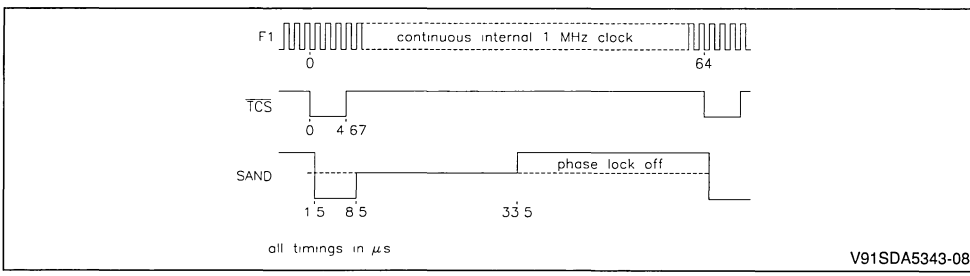
TELETEXT DATA INPUT TIMING



Data Stable : 1 if ≥ 2V , 0 if ≤ 0.8V

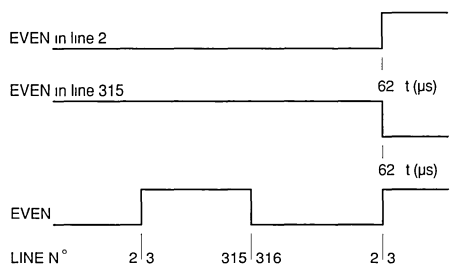
V91SDA5343-07

SYNCHRONIZATION TIMING



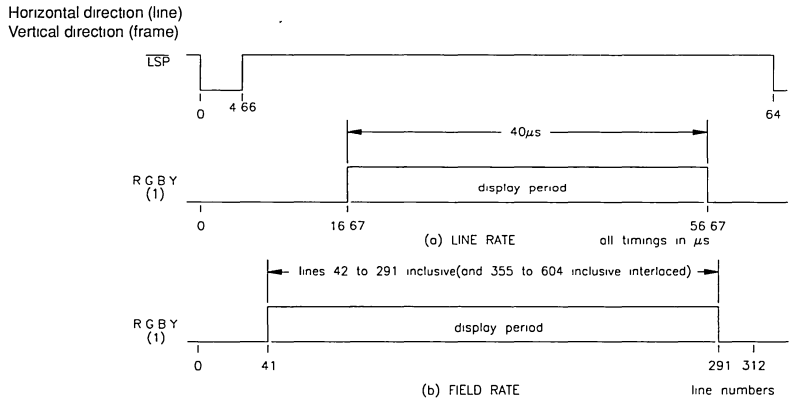
V91SDA5343-08

EVEN - OUTPUT TIMING



V91SDA5343-09

DISPLAY OUTPUT TIMING



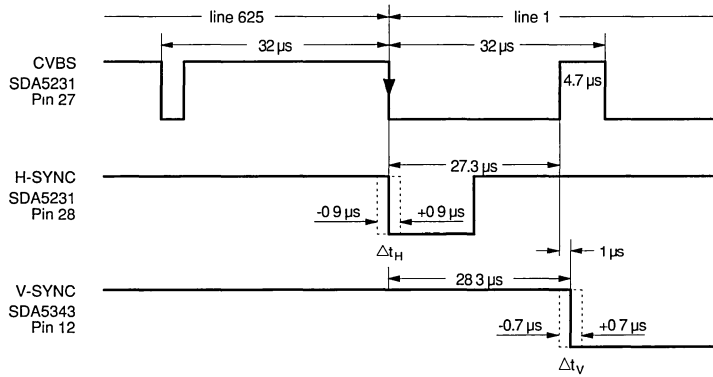
(1) - Also BLAN in character and box blanking

V91SDA5343-10

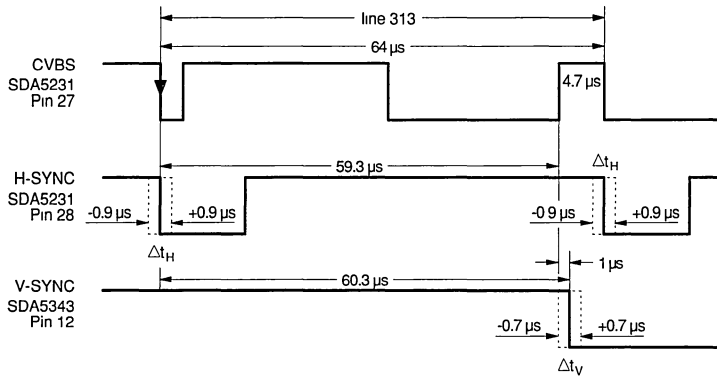
SYNCHRONIZATION TIMING

External Synchronization TV Mode

1st FRAME



2nd FRAME

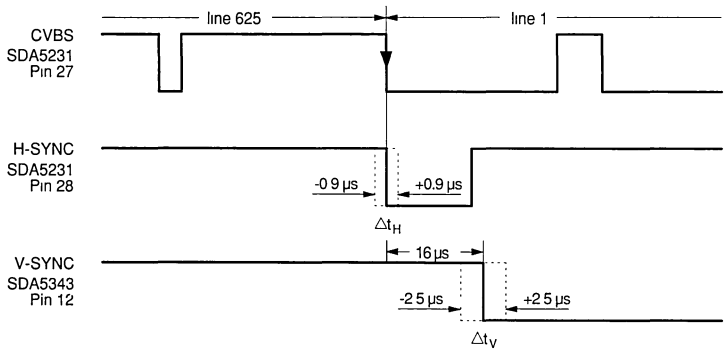


V91SDA5343-11

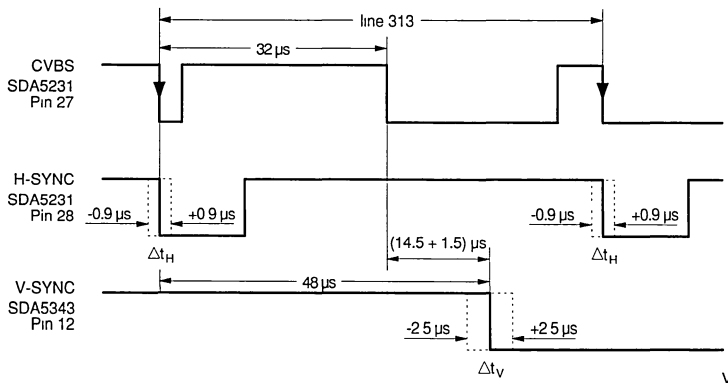
SYNCHRONIZATION TIMING (continued)

External Synchronization VCR Mode

1st FRAME

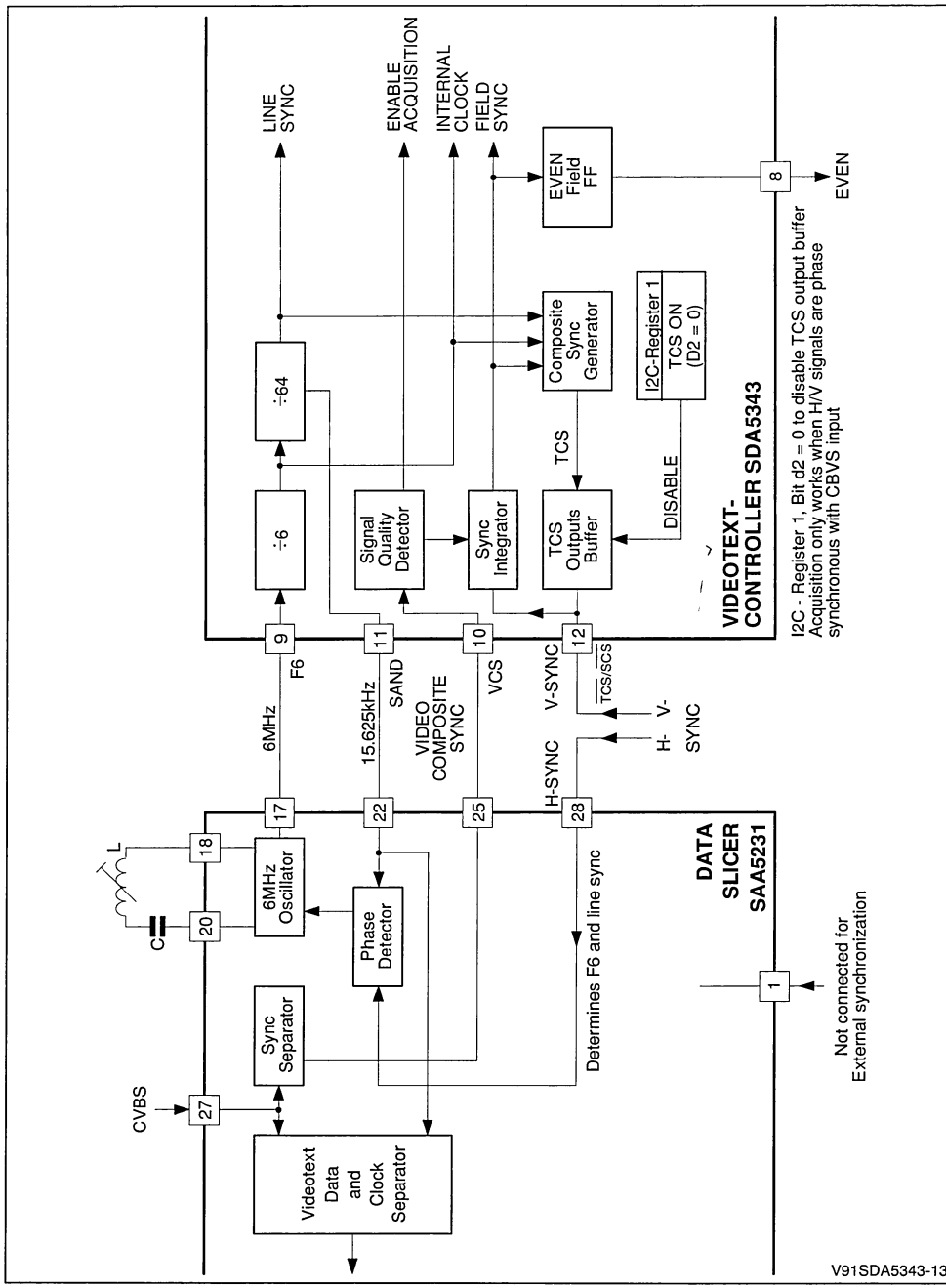


2nd FRAME



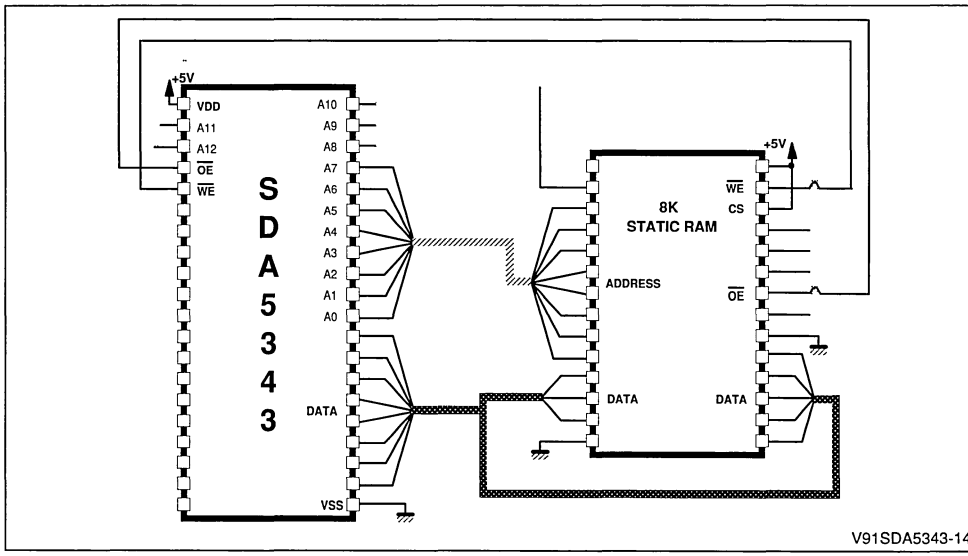
V91SDA5343-12

EXTERNAL SYNCHRONIZATION BY H/V SIGNALS



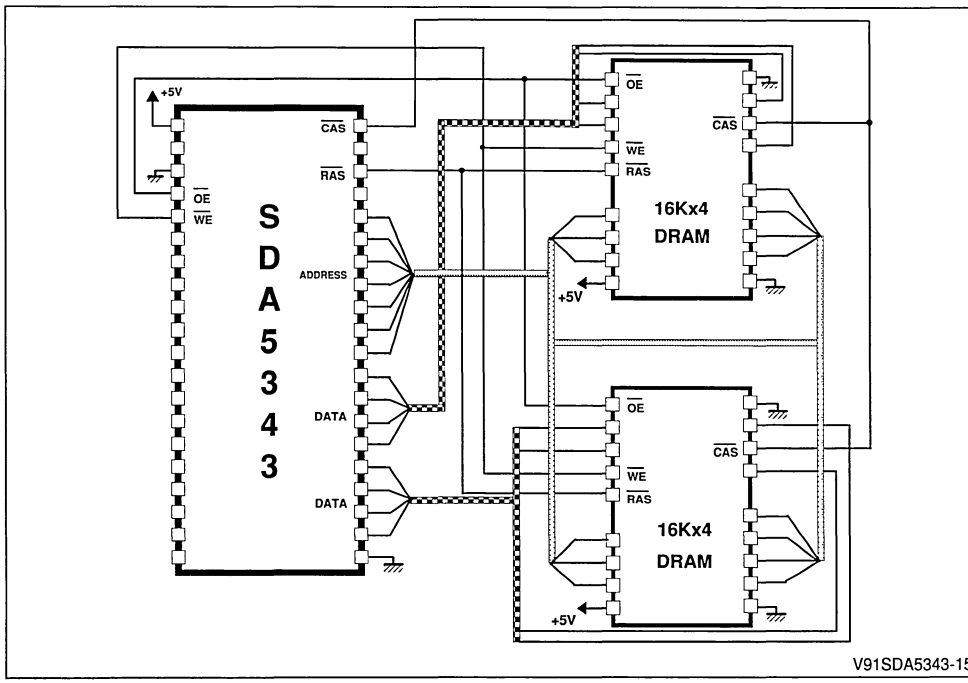
MEMORY INTERFACE DIAGRAM WITH SDA5343 (40-pin DIP package)

Figure 1a : 8-page Application with SRAM



V91SDA5343-14

Figure 1b : 8-page Application with DRAM



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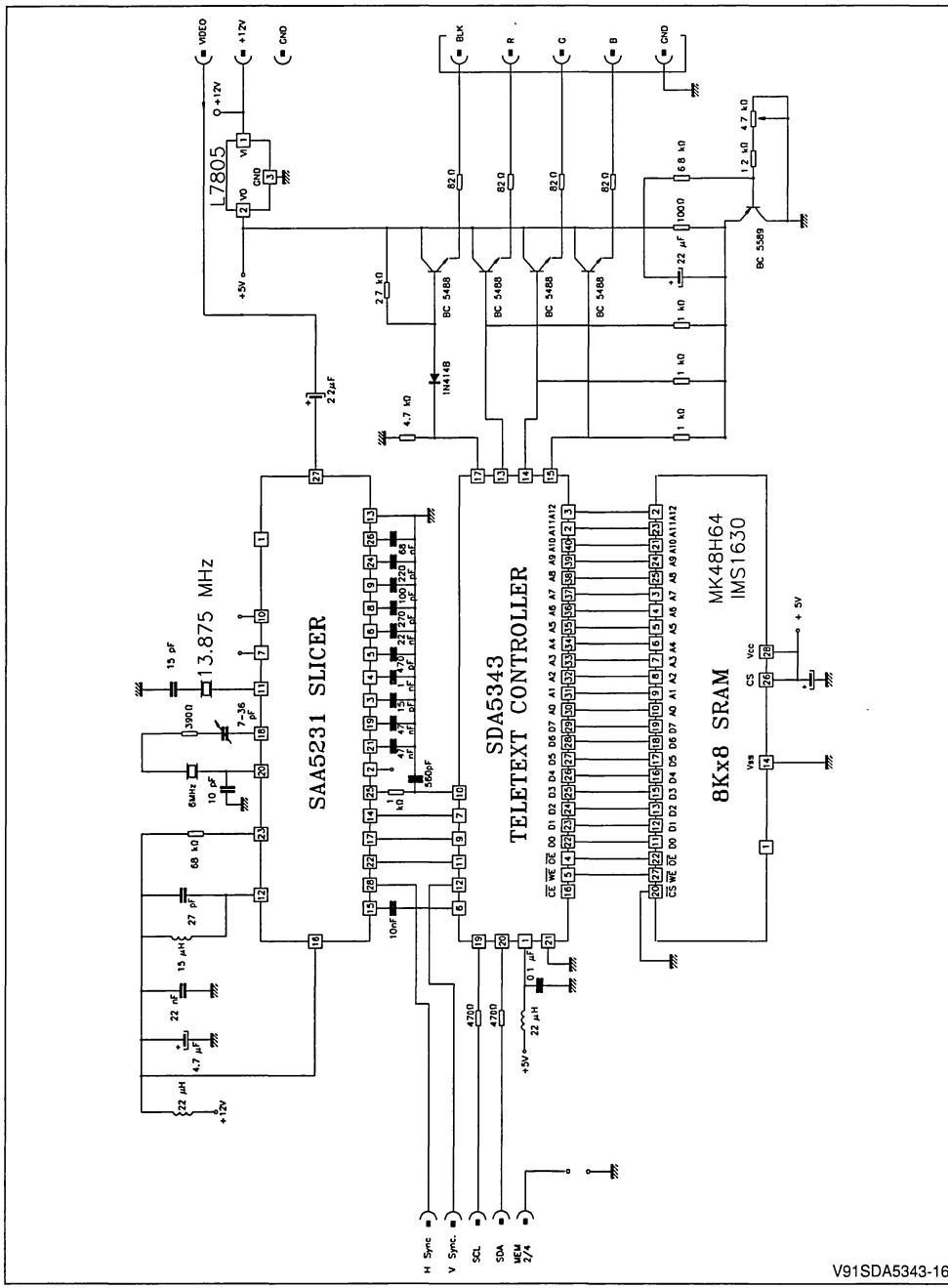
APPLICATION DIAGRAM

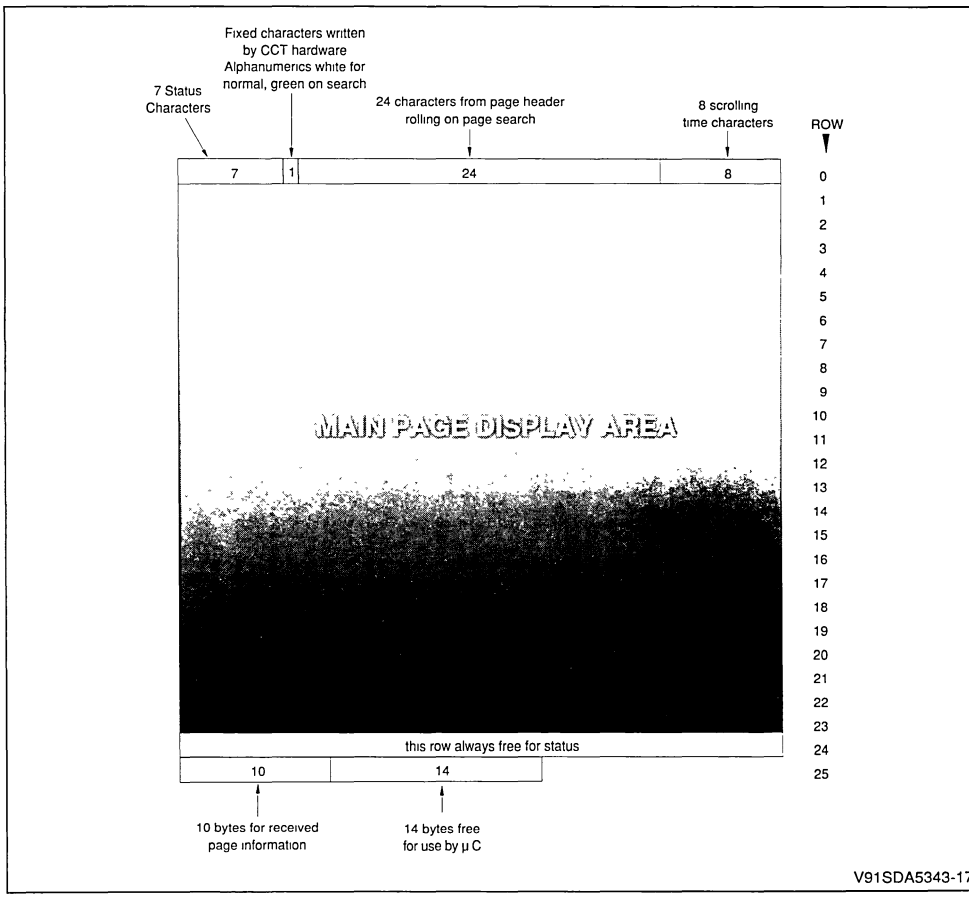


APPLICATION NOTES

ORGANIZATION OF A PAGE-MEMORY

The organization of a page-memory is shown below. In contrast with the first generation of Teletext Decoders the new CCT (Computer Controlled Teletext) chip provides a display format of 25 rows of 40 characters per row.
Row number twenty-four is used by the microprocessor for the display of information.
Row zero contains the page header.
The organization is as follows :
The first seven characters (0 - 6) are used for messages regarding the operational status.
The eighth character is an alphanumeric control character either "white" or "green" defining the "search" status of the page. When it is "white" the operational state is normal and the header appears white ; when it is "green" the operational state corresponds to "search mode" and the header appears green. The following twenty-four characters give the header of the requested page when the system is in search mode. The last eight characters display the time of day.
Row twenty-five comprises ten bytes of control data concerning the received page (see Table 1) and fourteen free bytes which can be used by the microprocessor.

PAGE MEMORY ORGANISATION



REGISTER FUNCTIONS

Register	Function	Bit(s)	Description
R0 Address 00H	R11 adressing and pin functions control	SEL 11B (D0)	Selection of register 11B (D0 = 1) or 11A (D0 = 0)
		CE ON (D1)	Selection of signal output on pin 16 : $\overline{CE}$ (D1 = 1) or $\overline{COR}$ (D1 = 0)
		EVEN OFF (D2)	Control of EVEN pin : EVEN signal output (D2 = 0) or grounded (D2 = 1)
R1 Address 01H	Operating mode controls	TCS (D2)	0 = TCS OFF, V_{SYNCH} input 1 = Not allowed
		$\overline{DEW}$ / FULLFIELD (D3)	Selection of field flyback mode or full channel mode (D3 = 1) for recovering of Teletext data.
		GHOST ROW ENABLE (D4)	Selection of ghost row mode (D4 = 1)
		$\overline{ACQUISITION}$ ON / OFF (D5)	Control of acquisition operation (D5 = 0 enables acquisition)
		7 bits + parity or 8 bits without parity (D6)	Selection of received data format either 7 bits with parity (D6 = 0) or 8 bits without parity (D6 = 1).
R2 Address 02H	Addressing information for a page request	SC0, SC1, SC3 (D0, D1, D2)	Address the first column of the on chip page request RAM to be written.
		TB (D3)	Test bit equal to "0" in the normal working mode.
		A0, A1 (D4, D5)	Address a group of four consecutive pages currently used for data acquisition;
		A2 (D6)	Address of one of the two groups of four pages for acquisition in normal mode.
R3 Address 03H	Data relative to the requested page (see Table 3)	PRD0 - PRD4 (D0 - D4)	Written data in the page request RAM, starting with the columns addressed by SC0,SC1,SC2.
R4 Address 04H	Selection of one of eight pages to display	A0, ... A2 (D0, ... D2)	These three bits correspond to the logical states of the three address lines (A10, A11, A12) during access read cycles.
R5 Address 05H	Display control for normal operation	PON (D0, D1)	Picture on (IN: D0, OUT: D1) (1 = ON, 0 = OFF)
		TEXT (D2, D3)	Text on (IN: D2, OUT: D3) (1 = ON, 0 = OFF)
		$\overline{COR}$ (D4, D5)	Contrast reduction on (IN: D4, OUT: D5) (1 = ON, 0 = Normal)
		BKGND (D6, D7)	Background colour on (IN: D6, OUT: D7) (1 = ON, 0 = OFF)
R6 Address 06H	Display control for news-flash subtitle generation	See R5	Activated by broadcasted bit C5, C6 of Teletext control bit
R7 Address 07H	Display mode	BOX ON 0, 1-23,24 (D0, D1, D2)	The "boxing" function is enabled on row 0,1-23 and 24 by D0, D1 and D2 set to one.
		$\overline{Single}$/Double height (D4/D3)	X0 = Normal 01 = double height Rows 0 to 11 11 = double height Rows 12 to 23
		$\overline{Conceal}$/Reveal (D5)	Conceal Reveal Function
		Cursor ON/$\overline{OFF}$ (D6)	Cursor poisition given by row/column value of R9/R10
		$\overline{STATUS}$ ROW $\overline{BTM}$ / TOP (D7)	The 25th row is displayed before the "Main text Area" (lines 0-23) (D7 = 1) or after (D7 = 0).

REGISTER FUNCTIONS (continued)

Register	Function	Bit(s)	Description
R8 to R11A Address 08H to 0BH*	Active chapter address (R8), active row address (R9), active column address (R10). Data contained in R11A read (written) from (to) memory by microprocessor via I^2C Bus.		
R11B Address 0BH*	Status	VCS ON (D0)	Good VCS quality signal detected (D0 = 1) or disturbance (D0 = 0)
		60Hz (D7)	VCS received with 60Hz frequency (D7 = 1) or 50Hz (D7 = 0). Valid only when D0 = 1 (D7 grounded if D0 = 0)

* Reading of R11A and R11B is determined by register 0, bit D0. Nevertheless, write operation is always performed on R11A register.

Table 1 : Row 25 received control data format.

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM	HAM	HAM	HAM	HAM	HAM	HAM	HAM	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
COLUMN	0	1	2	3	4	5	6	7	8	9

Page number : - MAG = magazine, PU = page units, PT = page tens
Page sub-code . - MU = minutes units, MT = minutes tens, HU = hours units, HT = hours tens.
PBLF = page being looked for, FOUND = low for page found, HAM = hamming error in byte, C4-14 = control bits

REGISTER MAP (see Table 2)

Registers R1 to R10 are write only whilst R11A is a read/write and R11B is a read only register respect to the microprocessor.
The automatic succession on a byte basis is indicated by the arrows in Table 2.
In the normal operating mode TB should be set to logic level 0.
After power-up the contents of the registers are as follows : all bits in registers R1 to R11 are cleared to zero with the exception of bits D0 an D1 in registers R5 and R6 which are set to logical one.
After power-up all the memory bytes are preset to hexadecimal value 20 H (space) with the exception of the byte corresponding to row 0 of column 7 of chapter 0 which is set to the value corresponding to "alpha white" hexadecimal value 07 H.

Table 2 : Register specification.

D7	D6	D5	D4	D3	D2	D1	D0		
*	*	*	*	*	EVEN OFF	CE ON	SEL 11B	R0	Mode 0
*	$\overline{7+P}$/ 8 BIT	ACQ $\overline{ON}$/OFF	GHOST ROW ENABLE	$\overline{DEW}$/ FULL FIELD	TCS	*	*	R1	Mode 1
*	BANK SELECT A2	ACQ CCT A1	ACQ CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request adress
*	*	*	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
*	*				A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash / subtitle)
STATUS ROW $\overline{BTM}$/TOP	CURSOR $\overline{ON}$/OFF	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
*				CLEAR MEM	A2	A1	A0	R8	Active chapter
*	*	*	R4	R3	R2	R1	R0	R9	Active row
*	*	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11A	Active data
60Hz	0	0	0	0	0	0	V_{CS} ON	R11B	Status

* Reserved register bits : must be set to 0

Table 3 : Register R3.

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care magazine	$\overline{HOLD}$	MAG2	MAG1	MAG0
1	Do care page tens	PT3	PT2	PT1	PT0
2	Do care page units	PU3	PU2	PU1	PU0
3	Do care hours tens	X	X	HT1	HT0
4	Do care hours units	HU3	HU2	HU1	HU0
5	Do care minutes tens	X	MT2	MT1	MT0
6	Do care minutes units	MU3	MU2	MU1	MU0

The abbreviations have the same significance as in Table 1 with the exception of the "DO CARE" entries. It is only when this bit is "1" that the corresponding digit is taken into consideration on page request. For example, a page defined as "normal" or one difined as "timed" may be selected

If "HOLD" is low the page is held. The addressing of successive bytes via the S-bus is automatic.

CHARACTER SETS

The selection of the character sets for a particular language is effected by the three control bits (C12-C14) located in the page header. These three bits are decoded as shown in Table 4.

Table 4 : National character sets control bits.

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH	SPANISH
C12	0 (1) (1)	0	0	0	1	1
C13	0 (1) (1)	0	1	1	0	0
C14	0 (0) (1)	1	0	1	0	1

The basic set of the 96 characters is shown in Table 5.The location of the 13 national characters are shown in Table 5 whilst full national character sets are depicted in Tables 6 thru 11.

Table 5 : Basic character set.

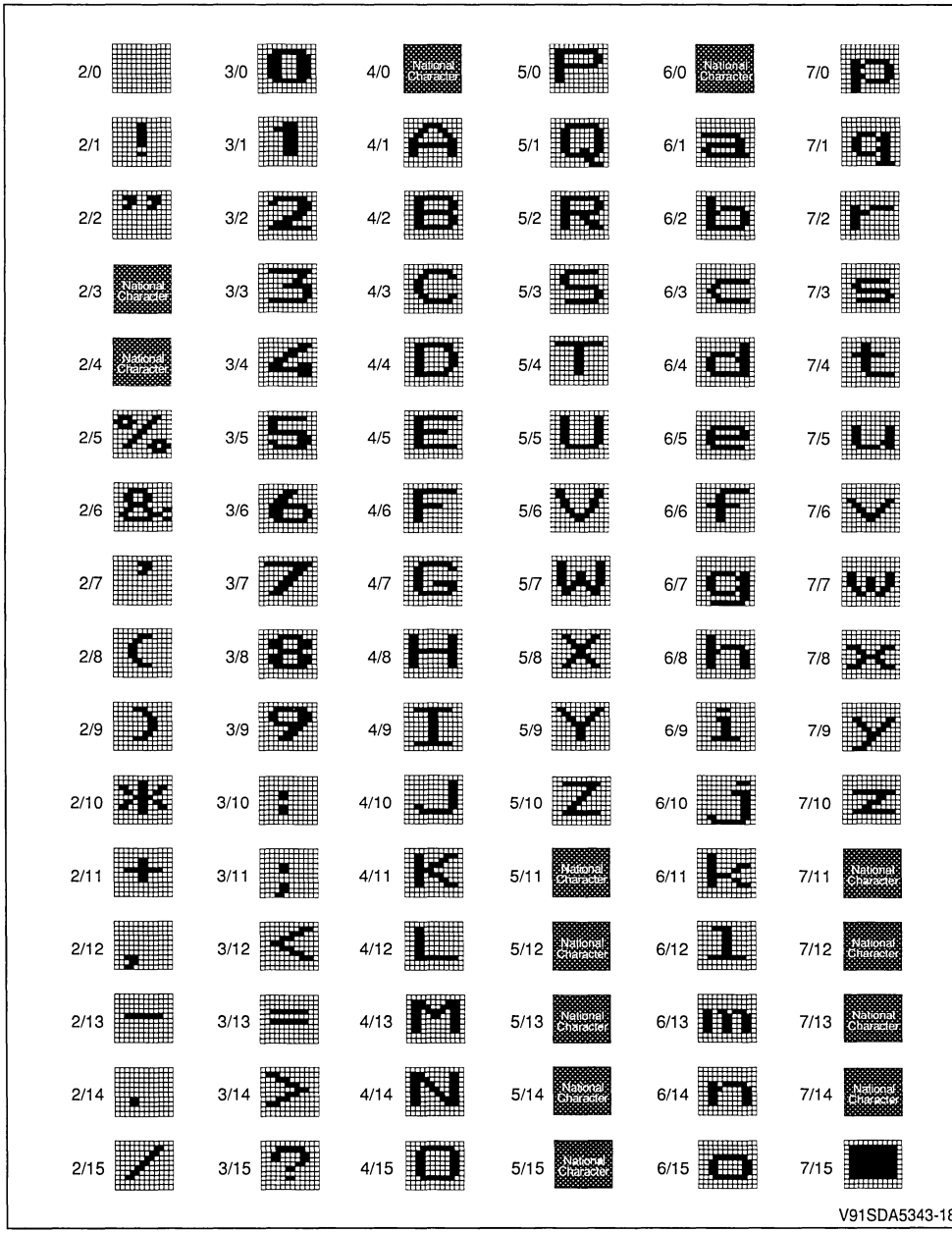


Table 6 : English Basic Character Set

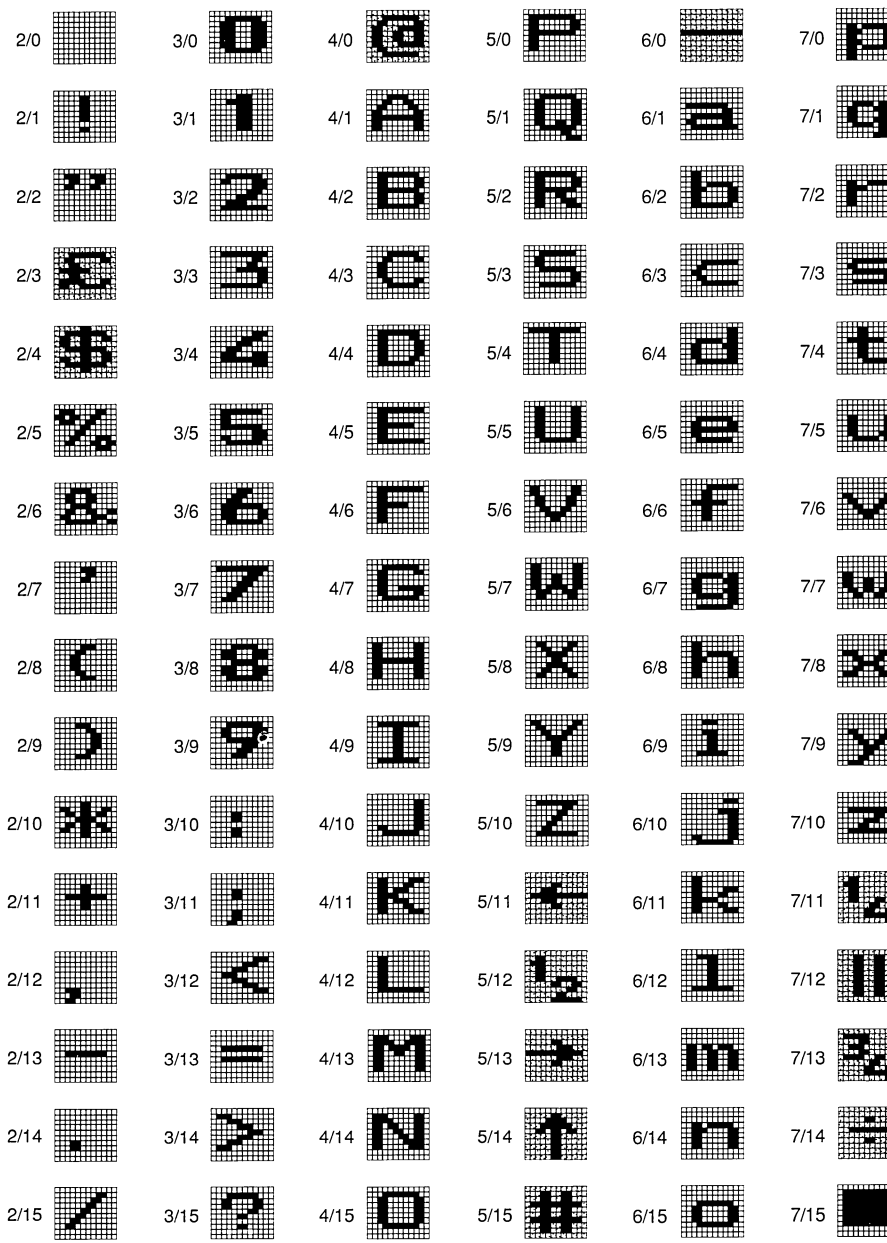


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Table 7 : German Basic Character Set

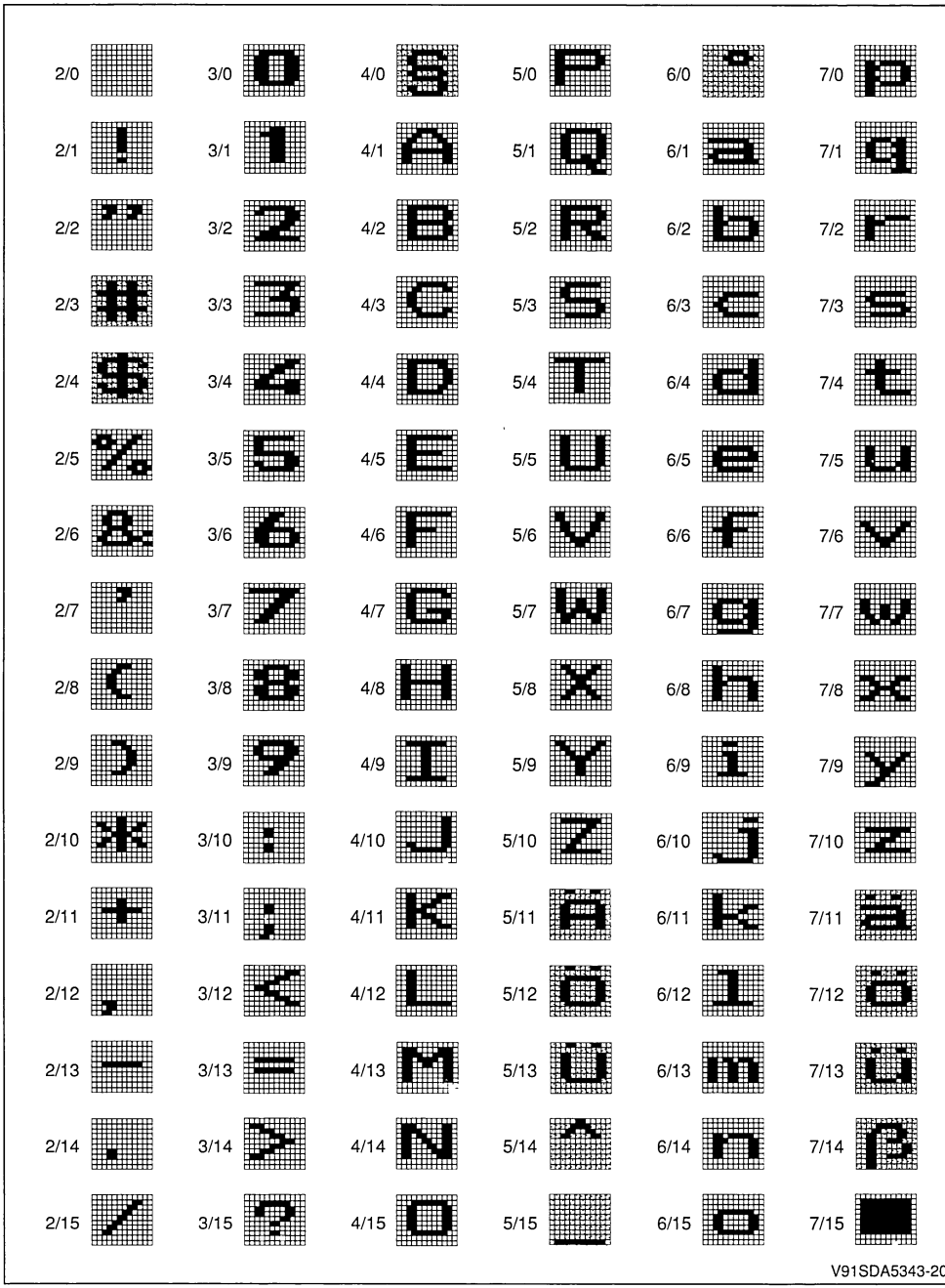
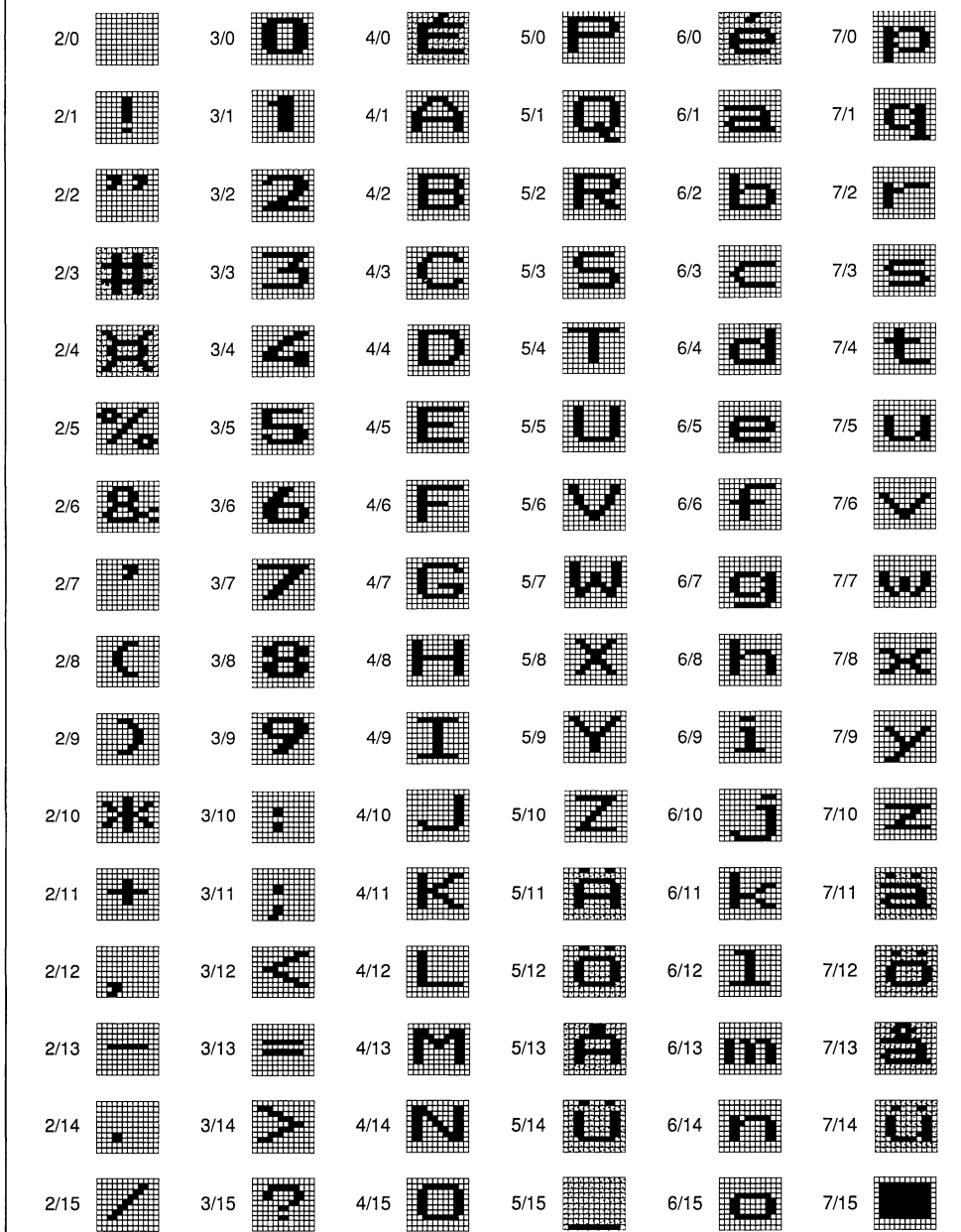
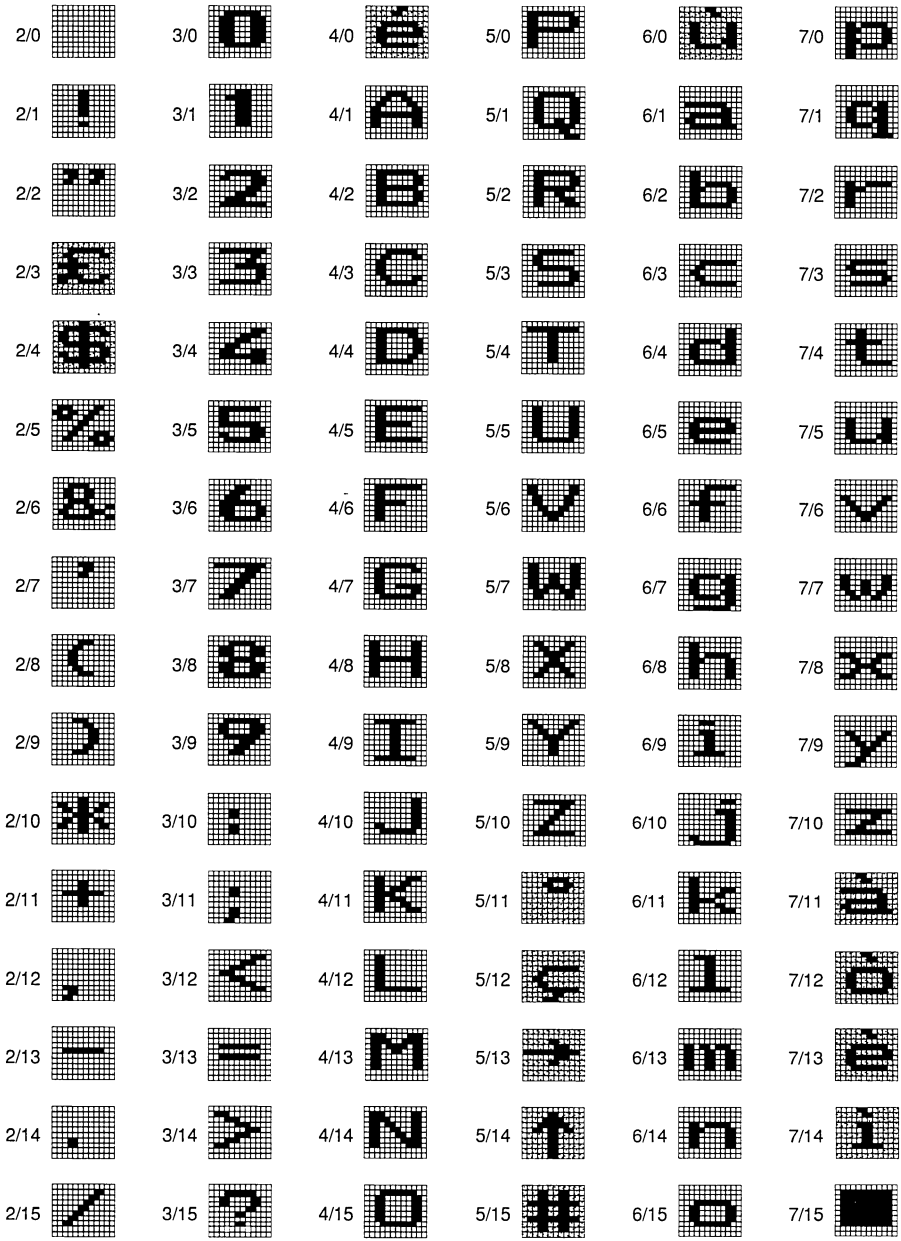


Table 8 : Swedish Basic Character Set



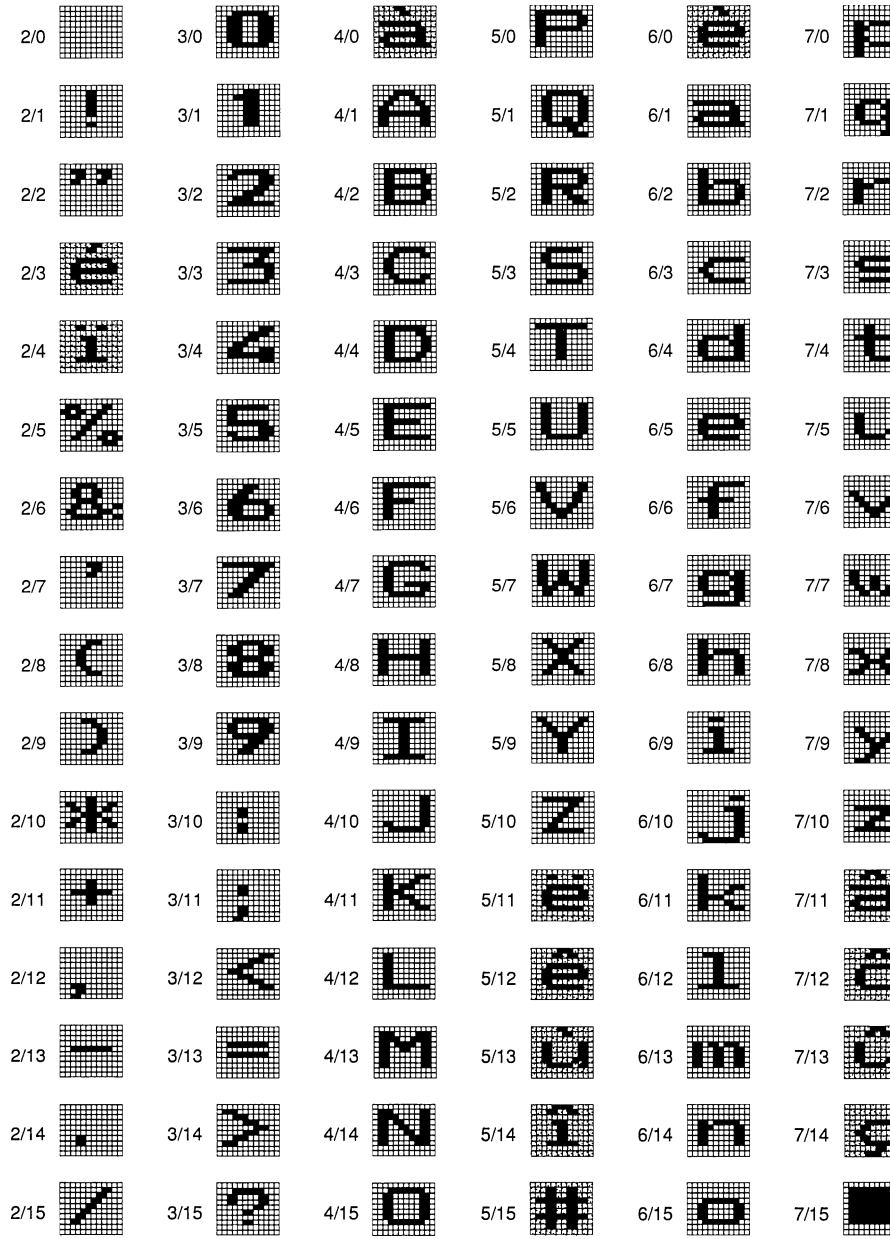
V91SDA5343-21

Table 9 : Italian Basic Character Set



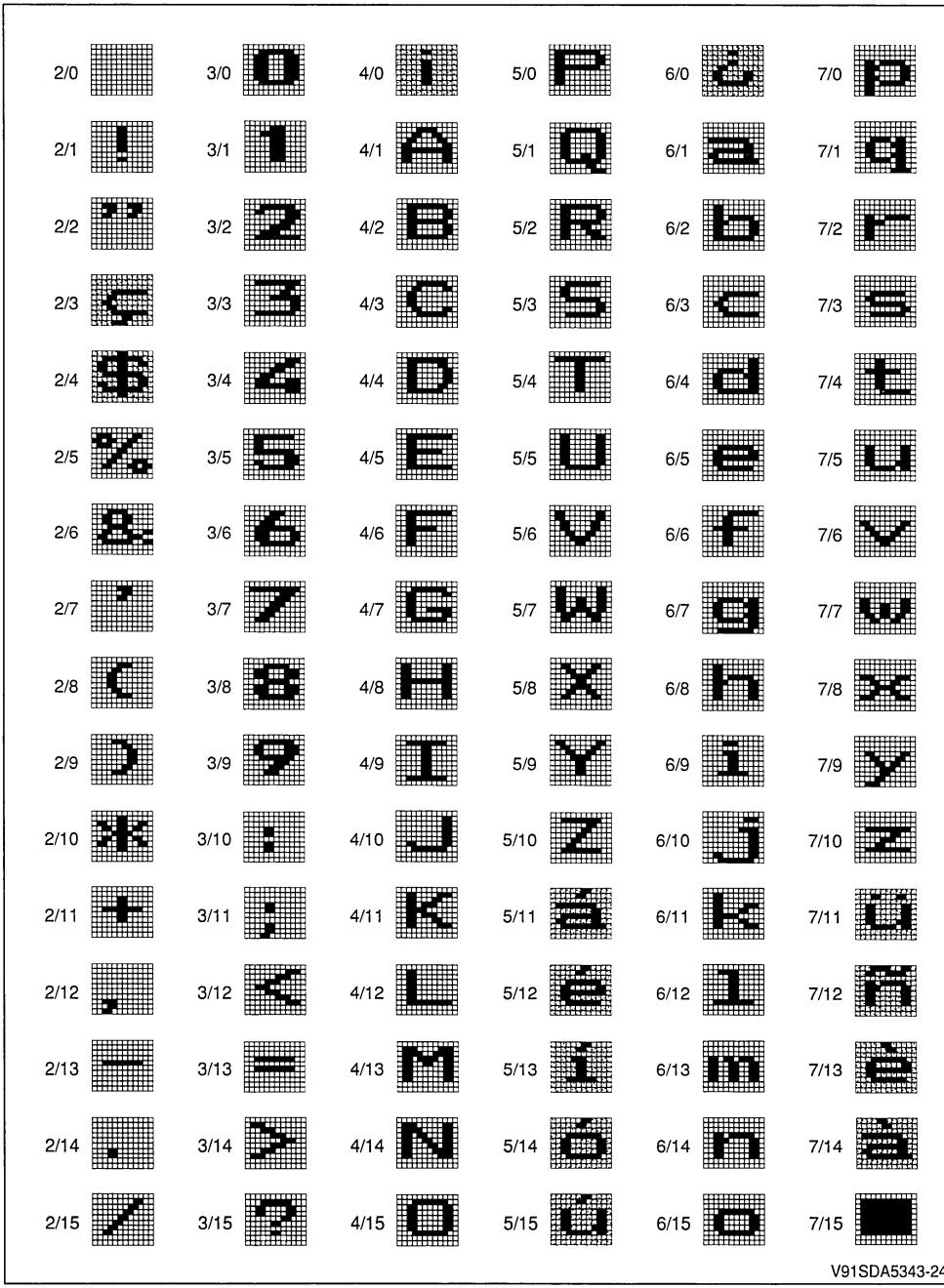
V91SDA5343-22

Table 10 : French Basic Character Set



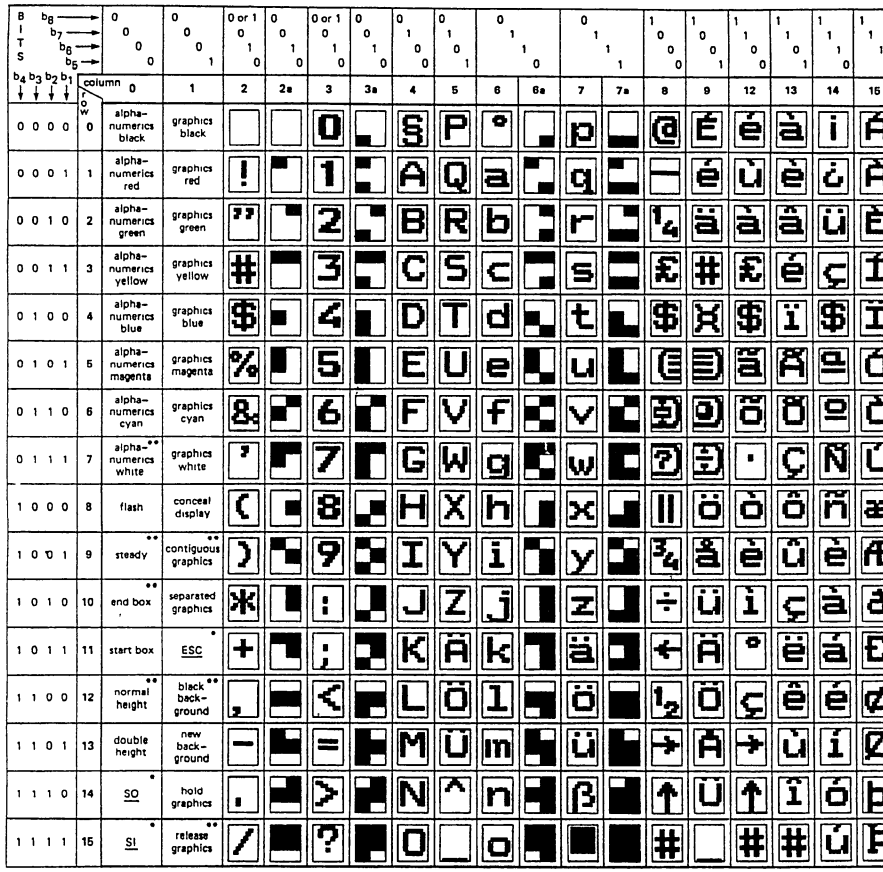
V91SDA5343-23

Table 11 : Spanish Basic Character Set



The complete character set with 8-bit decoding and using the German national character is given in Table 7.
Characters in columns 0 and 1 are normally displayed as blanks. Black dots represent the character shape whereas white dots represent the background.
Each character can be identified by a pair of corresponding row and column integers : for example the character "3" may be indicated by 3/3.
A rectangle may be represented as follows : ▭
The characters 8/6, 8/7, 9/5, 9/7 are used as special characters, always in conjunction with 8/5.
The 13 national characters are placed in columns with bit 8 = 0.

Table 7: Complete character set (with 8 bit codes).



* These control charcters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins

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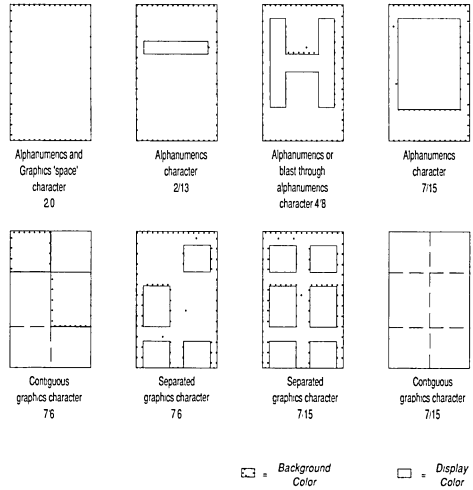
Figure 12: Character Format



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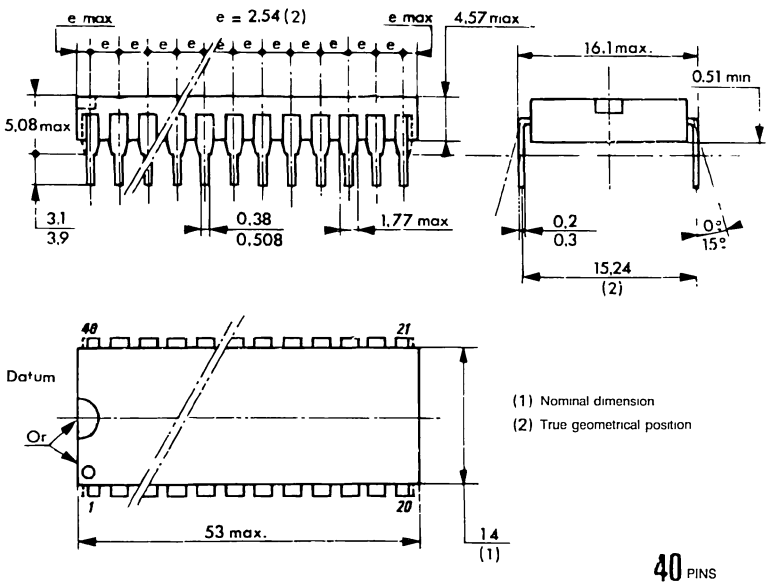
PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

STV1389AQ

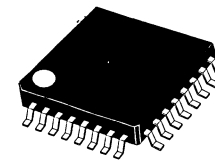
CABLE DRIVER FOR DIGITAL TRANSFER

ADVANCE DATA

- 1 DIFFERENTIAL INPUT, 3 DIFFERENTIAL OUTPUTS
- SUFFICIENT DRIVE CAPABILITY FOR A 300m LENGTH COAXIAL CABLE
- STABILITY DUE TO MINIMAL WAVEFORM DISTORTION
- BIPOLAR SILICON MONOLITHIC IC

APPLICATIONS

- DATA TRANSFER BETWEEN DIGITAL SIGNAL PROCESSING EQUIPMENT



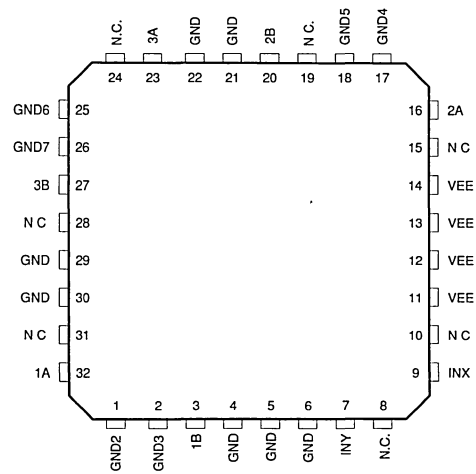
QFP32
(Plastic Package)

ORDER CODE : STV1389AQ

DESCRIPTION

The STV1389AQ offers in a single-chip a complete IC driver for digital data transfer.

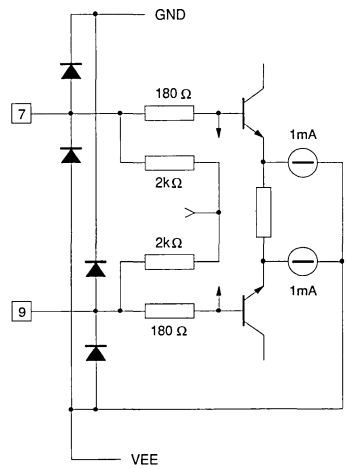
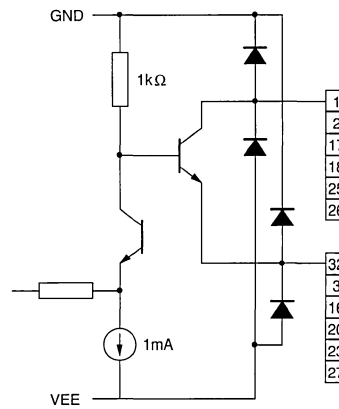
PIN CONNECTIONS



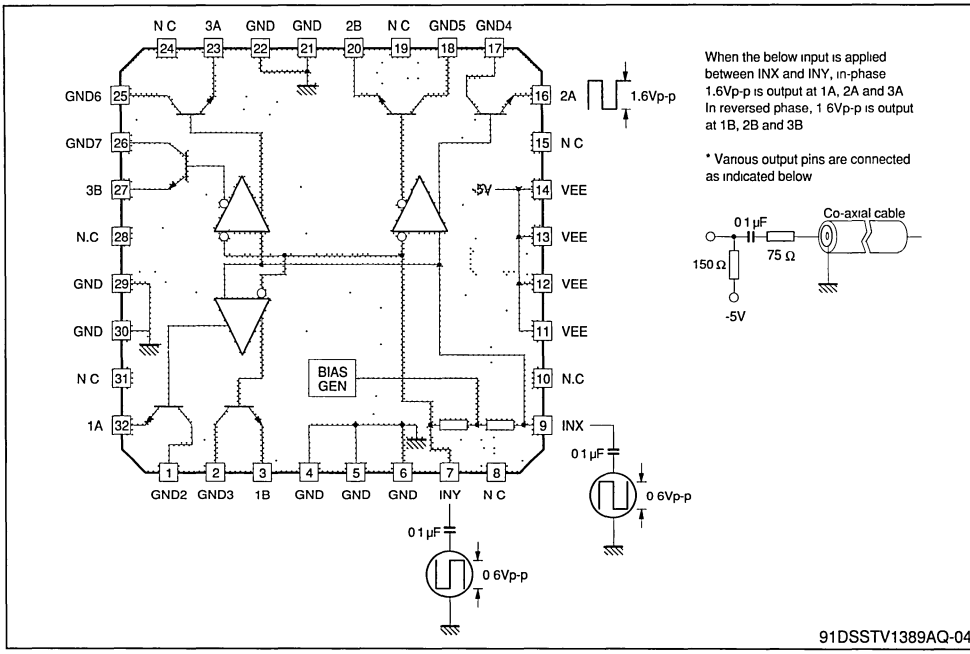
91DSSTV1389AQ-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION

Pin Number	Symbol	Standard DC Voltage	Equivalent Circuit	Description
7 9	INY INX	- 2.7V	 91DSSTV1389AQ-02	Input pin of the differential amplifier. Input executed after DC portion is cut off.
1 2 17 18 25 26	GND2 GND3 GND4 GND5 GND6 GND7	-	 91DSSTV1389AQ-03	Collector of the emitter follower output Tr. Connect to GND.
32 3 16 20 23 27	1A 1B 2A 2B 3A 3B	- 2.7V		Emitter of emitter follower output Tr. To use, connect pull-down resistor. (Even when only 1 side is used pull-down is executed In pairs.) Pairs 32 16 23 3 20 27

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7.0	V
T_{stg}	Storage Temperature	-65 to + 150	°C
P_D	Allowable Power Dissipation	500	mW

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.8 to 5.2	V
T_{opr}	Operating Temperature	- 20 to + 75	°C

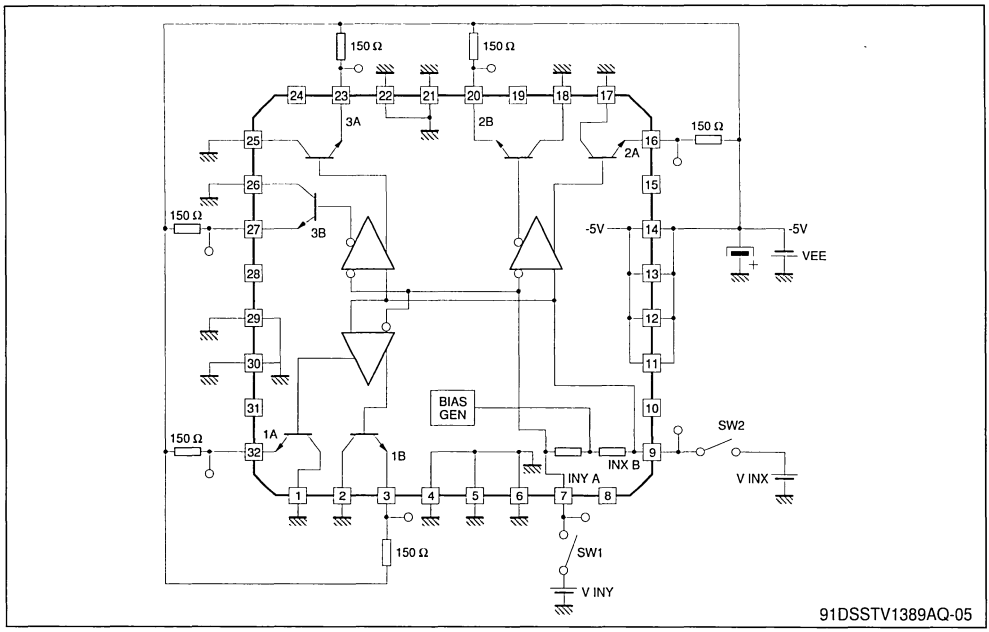
ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Bias Conditions		SW ON	Test Point	Test	Min.	Typ.	Max.	Unit
		V INY	V INX							
V1	Pin Voltage INY	-	-	-	Pin 7	Test of pin voltage	- 2.9	- 2.7	- 2.5	V
V2	Pin Voltage INX	-	-	-	Pln 9		- 2.9	- 2.7	- 2.5	V
A1-1	Pln Voltage 1A	-	-	-	Pin 32		- 3.1	- 2.7	- 2.5	V
B1-1	Pin Voltage 1B	-	-	-	Pin 3		- 3.1	- 2.7	- 2.5	V
A2-1	Pln Voltage 2A	-	-	-	Pin 16		- 3.1	- 2.7	- 2.5	V
B2-1	Pin Voltage 2B	-	-	-	Pin 3		- 3.1	- 2.7	- 2.5	V

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Bias Conditions		SW ON	Test Point	Test	Min.	Typ.	Max.	Unit
		V INY	V INX							
A3-1	PIn Voltage 3A	-	-	-	Pin 23	Test of pin voltage	- 3.1	- 2.7	- 2.5	V
B3-1	Pin Voltage 3B	-	-	-	Pin 27		- 3.1	- 2.7	- 2.5	V
IEE	Current Power Supply	-	-	-	VEE	Current power supply at VEE	- 143		- 77	mA
A1-2	DC applied 1A	V1 + 0.2	V2 - 0.2	SW1 SW2	Pin 32	Output DC voltage is tested when +0.2V is applied to INY and - 0.2V to INX. (A1-2) = Test value - (A1-1) (B1-2) = Test value - (B1-1) The difference with the previous pin voltage is recorded. Same for A2-2, B2-2, A3-2, B3-2	0.31	0.39	0.47	V
B1-2	DC applied 1B	↓	↓		Pin 3		- 0.47	- 0.39	- 0.31	V
A2-2	DC applied 2A	↓	↓		Pin 16		0.31	0.39	0.47	V
B2-2	DC applied 2B	↓	↓		Pin 20		- 0.47	- 0.39	- 0.31	V
A3-2	DC applied 3A	↓	↓		Pin 23		0.31	0.39	0.47	V
B3-2	DC applied 3B	↓	↓		Pin 27		- 0.47	- 0.39	- 0.31	V
V1-1	Amplitude 1A + 1B	Calculation				(V1-1) = (A1-2) - (B1-2) Amplitude calculated from T10 with T15 as base, same for V2-1, V3-1.	0.65	0.75	0.85	V
V2-1	Amplitude 2A + 2B	Calculation					0.65	0.75	0.85	V
V3-1	Amplitude 3A + 3B	Calculation					0.65	0.75	0.85	V
-	Amplitude 1A/1B	Calculation				(A1-2) / (B1-2)	0.85	1.0	1.15	-
-	Amplitude 2A/2B	Calculation					0.85	1.0	1.15	-
-	Amplitude 3A/3B	Calculation					0.85	1.0	1.15	-
A1-3	DC applied 1A'	V1 - 0.4	V1 + 0.4	SW1 SW2	Pin 32	Output DC voltage is tested when - 0.4V is applied to INY and + 0.4V to INX. (A1-3) = Test value - (A1-1) (B1-3) = Test value - (B1-1) The difference with the previous pin voltage is recorded. Same for A2-3, B2-3, A3-3, B3-3	- 0.9	- 0.75	- 0.6	V
B1-3	DC applied 1B'	↓	↓		Pin 3		0.6	0.75	0.9	V
A2-3	DC applied 2A'	↓	↓		Pin 16		- 0.9	- 0.75	- 0.6	V
B2-3	DC applied 2B'	↓	↓		Pin 20		0.6	0.75	0.9	V
A3-3	DC applied 3A'	↓	↓		Pin 23		- 0.9	- 0.75	- 0.6	V
B3-3	DC applied 3B'	↓	↓		Pin 27		0.6	0.75	0.9	V
V1-2	Amplitud'e 1A' + 1B	Calculation				(V1-2) = (A1-3) + (B1-3) Amplitude calculated from T22 with T27 as base, same for V2-2, V3-2.	1.3	1.5	1.7	V
V2-2	Amplitude 2A' + 2B'	Calculation					1.3	1.5	1.7	V
V3-2	Amplitude 3A' + 3B'	Calculation					1.3	1.5	1.7	V
-	Amplitude 1A' + 1B'	Calculation				(A1-3) / (B1-3)	0.85	1.0	1.15	V
-	Amplitude 2A' + 2B'	Calculation				(A2-3) / (B2-3)	0.85	1.0	1.15	V
-	Amplitude 3A' + 3B'	Calculation				(A3-3) / (B3-3)	0.85	1.0	1.15	V
V1-3	Linearity 1	Calculation				(V1-2) / (V1-1)	1.7	1.9	2.1	V
V2-3	Linearity 2	Calculation				(V2-2) / (V1-1)	1.7	1.9	2.1	V
V3-3	Linearity 3	Calculation				(V3-2) / (V1-1)	1.7	1.9	2.1	V

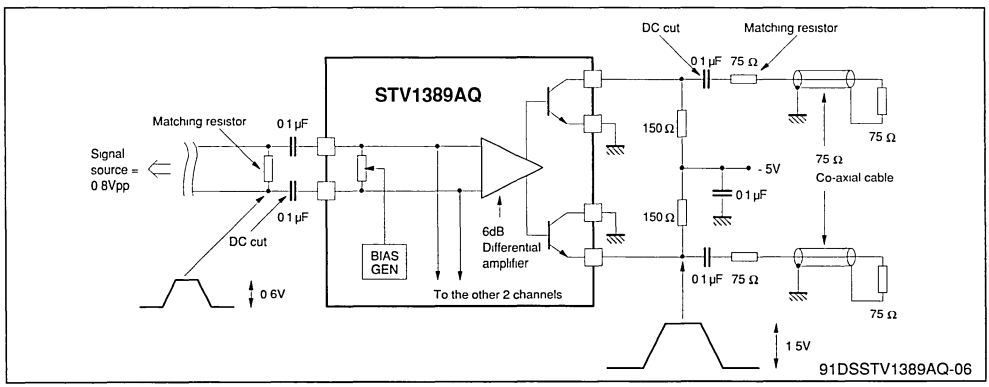
TEST CIRCUIT



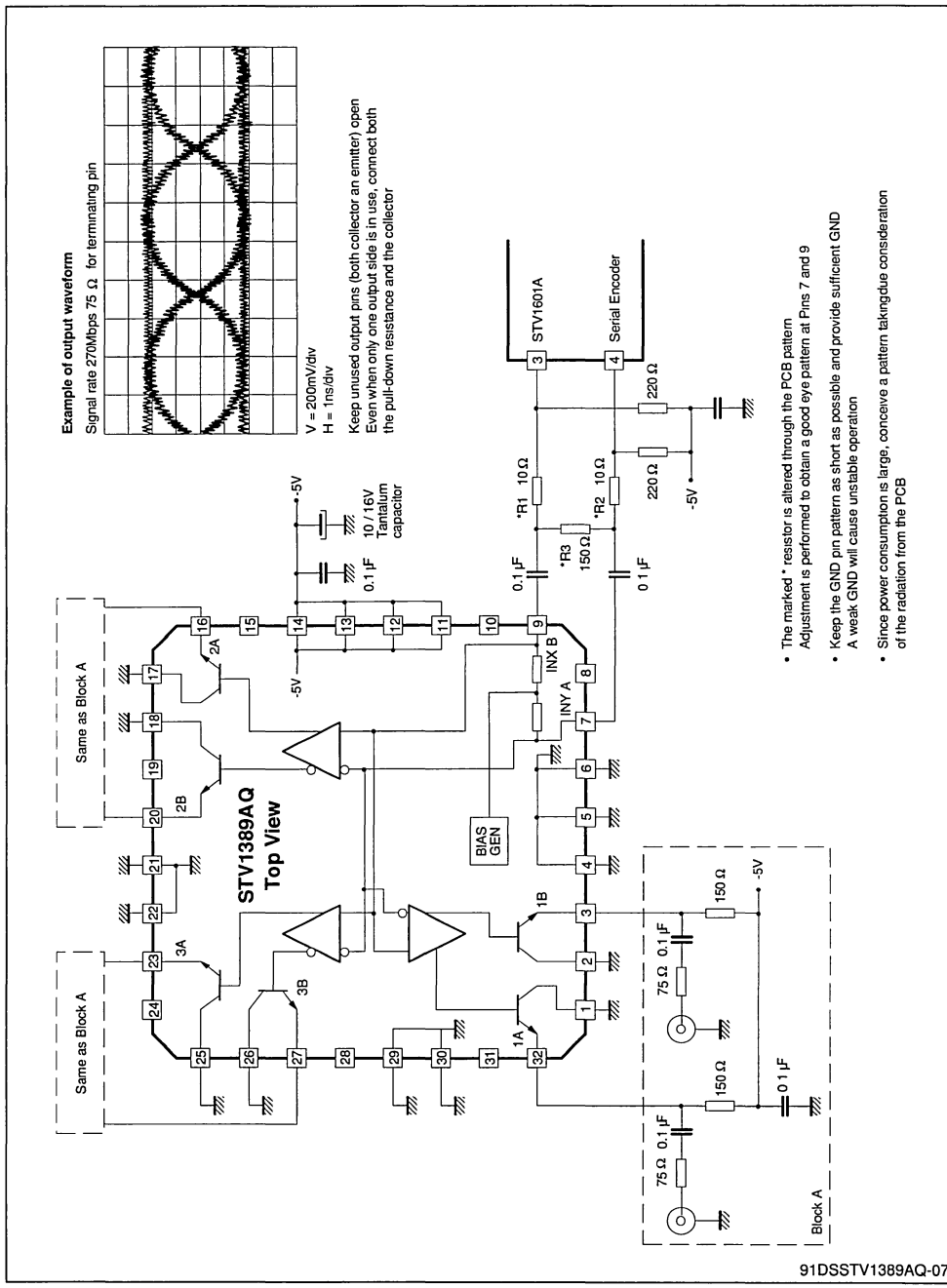
DESCRIPTION OF OPERATION

The STV1389AQ consists of 3 differential amplifier with a common input and a bias generator, and three differential outputs. Each amplifiers provides a 6dB gain and is configured as a differential output feeding the bases of a pair of current boosting on-chip emitter follower transistors. The differential input pins are internally biased and the input signal is ac-coupled to remove the D.C. component.
Between the output pins of each differential amplifier and the coaxial cable, an R-C network is connected to remove D.C. component from the output and for impedance matching. The series resistor has a value of 68 to 75Ω to match a 75Ω coaxial cable. In this manner a signal almost identitical in level to the input signal is transferred to the coaxial cable.

Optimum PCB layout and matching resistor value are chosen to obtain good eye pattern design at the input pins. This is necessary because the waveform distortion at the input pins is directly transferred to the output waveform.



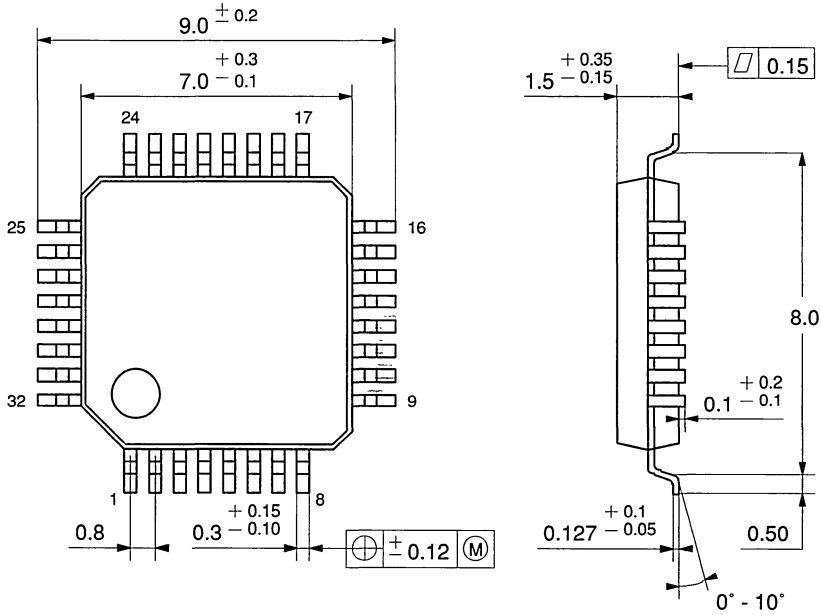
TEST CIRCUIT



PACKAGE MECHANICAL DATA

32 PINS - PLASTIC QFP

Dimensions in mm



SERIAL INTERFACE TRANSMISSION ENCODER

PRELIMINARY DATA

THIS IC CONTAINS ALL THE CIRCUITS NEEDED FOR CONVERSION FROM PARALLEL DATA, AND PARALLEL CLOCK, INTO SERIAL DATA. APPLICATIONS ARE STRAIGHTFORWARD AS ONLY A FEW EXTERNAL COMPONENTS ARE NEEDED.

OTHER RELATED IC's INCLUDE :

- STV1602A, A SERIAL TRANSMISSION DECODER (WITH A BUILT-IN CABLE EQUALIZER AND PARALLEL-TO-SERIAL CONVERSION)
- STV1389AQ COAXIAL CABLE DRIVER

STRUCTURE

- Hybrid IC

APPLICATIONS

SERIAL DATA TRANSMISSION ENCODER

- 100 to 270 Mb/s

APPLICATIONS EXAMPLES

- Serial data transmission of digital television signal 525-625 lines
- 4:2:2 component 270Mb/s (10-BIT)
- 4*FSC PAL composite 177Mb/s (10-BIT)
- 4*FSC NTSC composite 143Mb/s (10-BIT)

FUNCTIONS

- Parallel-to-serial conversion
- Scrambler : Modulo - 2 division by $G(x) = (x^9 + x^4 + 1)(x + 1)$
- PLL for serial clock generation
- PLL lock detection
- Sync word required with the parallel data stream

	8 bit	10 bit
1st word	FFH	3FFH
2nd word	00H	000H
3rd word	00H	000H

Note : The words composing the Sync word given above will not appear during datawords
This limitation includes 00 and FF in 8-bit use and 000 through 003 and 3FC through 3FF in 10-bit use.

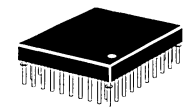
SYNC WORD CONVERSION (8-BIT OR 9-BIT TIMING REFERENCE SIGNAL IS INTERNALLY CONVERTED TO 10-BIT).

CODE LIMITATION

The word composing the Sync word listed above shall not appear during data words.

DESCRIPTION

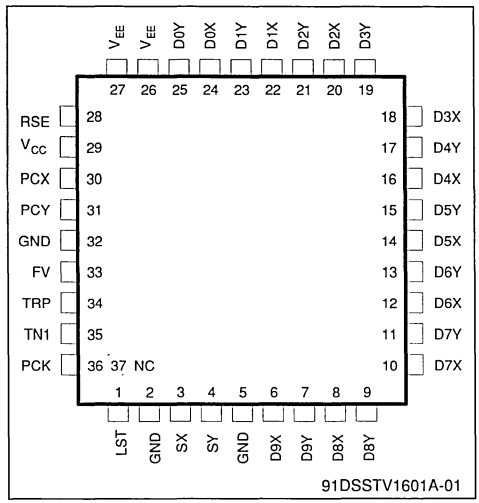
The STV1601A is a Hybrid IC encoder that converts parallel data into serial data for a serial transmission line.



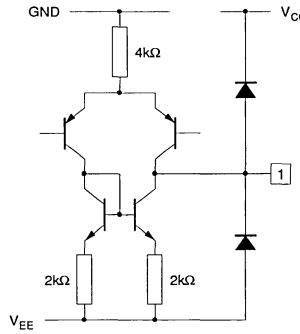
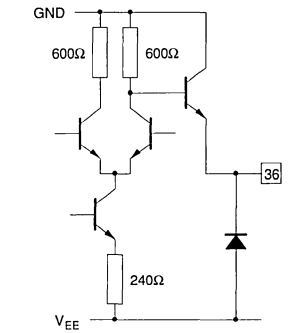
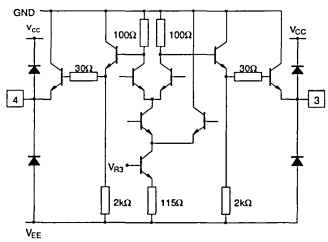
PGA37
(Ceramic Package)

ORDER CODE : STV1601A

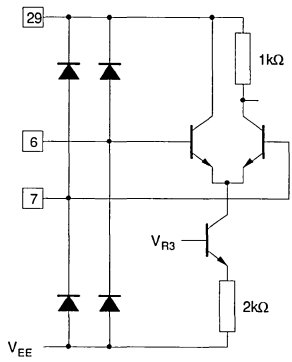
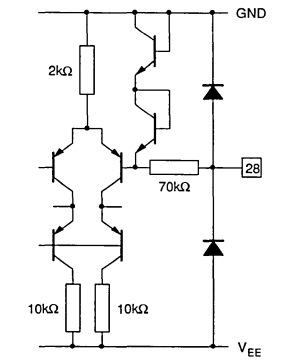
PIN CONNECTIONS



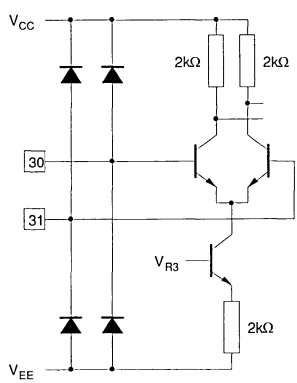
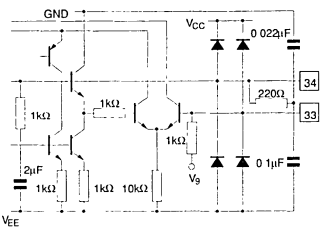
PIN DESCRIPTION

Pin N	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
1	LST	 91DSSTV1601A-02	PLL lock detection. Is High while PLL locked. If unlocked, becomes irregular. At free running (TN1 H) turns Low H L	O	 -1.0	 	 -4.0	 V V
36	PCK	 91DSSTV1601A-03	Clock output frequency divided to 1/10 VCO output. Used to check VCO free running frequency H L	O	 	 -0.8 -1.6	 	 V V
3	SX	 91DSSTV1601A-04	Differential Serial Output Input parallel data is converted to serial, then from scrambled NRZ to NRZI data H L	O	 	 -1.6 -2.4	 	 V V
4	SY							

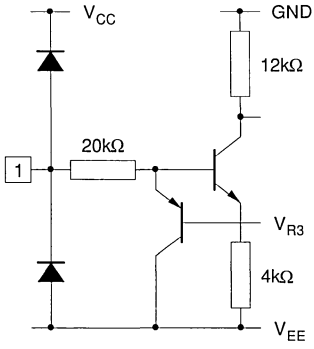
PIN DESCRIPTION (continued)

Pin N	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
29	V_{CC}	 91DSSTV1601A-05	Parallel data and clock input buffers power supply. When this pin is connected to +5V, parallel data clock turns to TTL mode. When this pin is connected to GND, parallel data clock turns to ECL mode.	-				
6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25	D9X D9Y D8X D8Y D7X D7Y D6X D6Y D5X D5Y D4X D4Y D3X D3Y D2X D2Y D1X D1Y D0X D0Y		Parallel input ports: LSB : D0X or Y MSB : D9X or Y Signal : DnX Return : DnY For ECL mode, V_{CC} shalll be 0V H L ForTTL mode, VCC shall be +5V H L		 -1.0 2.0	 -1.6 0.8	 V V V V
28	RSE	 91DSSTV1601A-06	VCO range selection H : high range 140 to 270MHz L : low range 100 to 143MHz H L	I	 -0.4		 -4.0	 V V

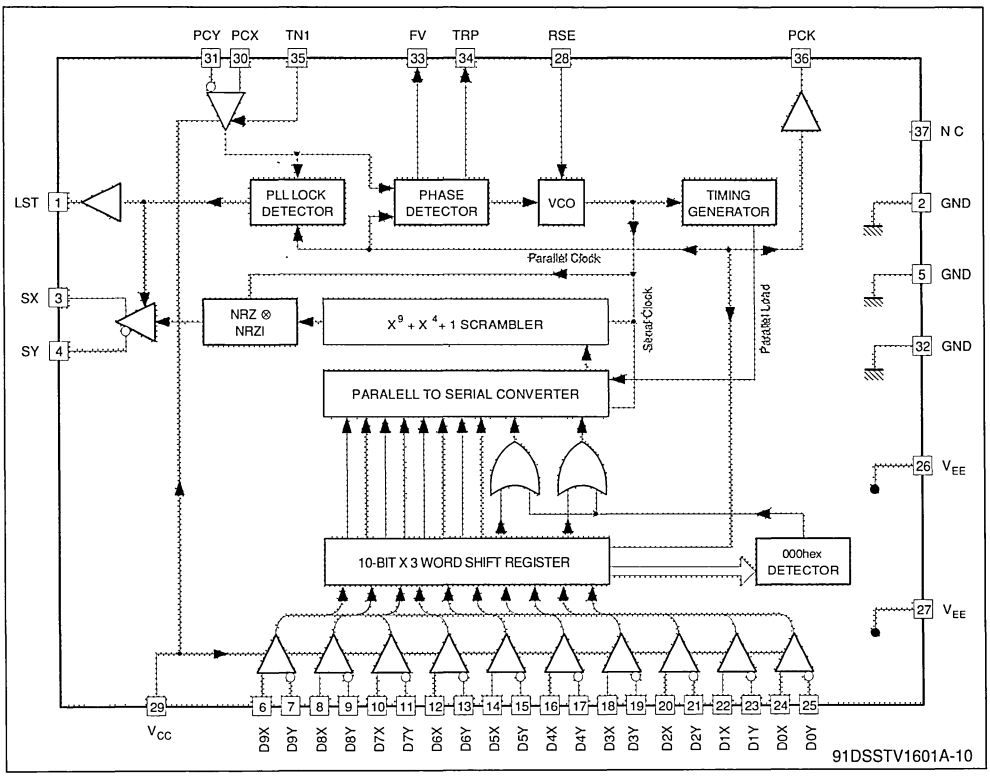
PIN DESCRIPTION (continued)

Pin N	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
30	PCX	 91DSSTV1601A-07	Parallel clock (PCX) and its return (PCY) For ECL mode, V_{CC} = 0 H L For TTL mode, V_{CC} = +5V H L	I	 -1.0 2.0	 	 -1.6 0.8	 V V V V
31	PCY							
2 5 32	GND		GND					
26	V_{EE}		-5V power supply I/O buffer PLL		-5.2	-5.0	-4.8	V
27	V_{EE}		-5V power supply Logic part		-5.2	-5.0	-4.8	V
33	FV	 91DSSTV1601A-08	VCO free running frequency adjustment : V_{EE} level gives the lowest frequency. To adjust set TN1 high.	I		-3.9		V
34	TRP		VCO input and phase comparator output should be connected to a parallel clock frequency trap filter to minimize jitter	O		-3.2		V

PIN DESCRIPTION (continued)

Pin N	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
35	TN1	 91DSSTV1601A-09	Test mode : High : VCO free running condition (input disabled) Low : Normal mode (input enabled)	I	-1.0		-4.5	V V

BLOCK DIAGRAM



91DSSTV1601A-10

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-6	V
V_{CC}	Supply Voltage	+6	V
V_{IN}	Input Voltage	V_{EE} to V_{CC}	V
I_{OUT}	Output Current	-30	mA
T_{oper}	Operating Temperature	0 to 65	°C
T_{stg}	Storage Temperature	-50 to 125	°C
P_D	Allowable Power Dissipation	2.0	W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-4.8 to -5.2	V
V_{CC}	Supply Voltage *	4.8 to 5.2	V
T_{oper}	Operating Temperature	0 to 65	°C

* For TTL input. Voltages are given with respect to GND

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5V, V_{CC} = GND/+5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
DC characteristics							
I_{EE}	Supply Current 1		Figure 4		140		mA
I_{CC}	Supply Current 2				7		mA
V_{IH}	Input Voltage	V_{CC} = GND PCX, PCY, DnX, DnY		-1.0			V
V_{IL}						-1.6	V
V_{IH}		V_{CC} = +5V PCX, PCY, DnX, DnY		2.0			V
V_{IL}						0.8	V
I_{IH}	Input Current	PCX, PCY, DnX, DnY	Figure 5			5	µA
I_{IL}				-1		+1	µA
V_{IH}	Input Voltage	RSE	Figure 9	-0.4			V
V_{IL}						-4.0	V
V_{IH}		TN1	Figure 8	-1			V
V_{IL}						-4.5	V
V_{OH}	Output Voltage	PCK R_P = 1kΩ			-0.8		V
V_{OL}					-1.6		V
V_{OH}		LST I_{OH} = -10µA, I_{OL} = +10µA	Figure 7	-1.0			V
V_{OL}						-4.0	V
V_{OH}		SX, SY R_P = 220Ω			-1.6		V
V_{OL}					-2.4		V

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5V, V_{CC} = GND/+5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
AC characteristics							
f_{MAX1}	VCO Max. Oscillation Frequency 1	RSE = "H"	Figure 6	30.0			MHz
f_{MIN1}	VCO Min. Oscillation Frequency 1					14.0	MHz
f_{MAX2}	VCO Max. Oscillation Frequency 2	RSE = "L"		15.0			MHz
f_{MIN2}	VCO Min. Oscillation Frequency 2					10.0	MHz
f_{HP1}	PLL Pull in Range	f signal = 270MHz RSE = "H"	Figure 3	27.7			MHz
f_{LP1}						25.5	MHz
f_{HP2}		f signal = 177MHz RSE = "H"		18.8			MHz
f_{LP2}						16.5	MHz
f_{HP3}		f signal = 143MHz RSE = "H"		15.0			MHz
f_{LP3}						13.0	MHz
f_{OP1}	PLL Generator Frequency	RSE = "H"		14.0		27.0	MHz
f_{OP2}		RSE = "L"		10.0		14.5	MHz
tjit	Jitter	f signal = 270MHz RSE = "H"	Figure 10			±0.25	nsec

Tested through PCK : 1/10 of serial clock

SWITCHING CHARACTERISTICS

(V_{EE} = -5V, V_{CC} = GND/+5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
t_r	Rise Time	PCX R_P = 1kΩ	Figure 1		0.8		nsec
t_f	Fall Time				1.4		nsec
t_r	Rise Time	SX, SY R_P = 220Ω			0.7		nsec
t_f	Fall Time				0.7		nsec

TIMING RELATION OF INPUT CLOCK AND DATA

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
t_w	Pulse Width	PCX, PCY	Figure2	-5 + t_c/2	t_c/2	+5 + t_c/2	nsec
t_d	Delay Time	PCX - Dn		-5		+5	nsec

Figure 1 : t_r, t_f Definition

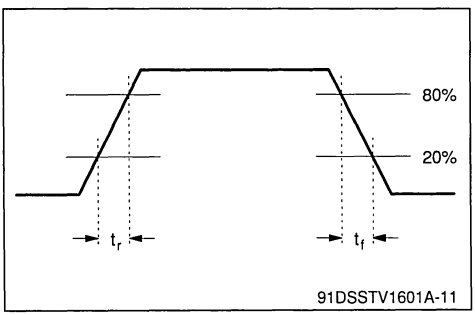


Figure 2 : t_d, t_w Definition

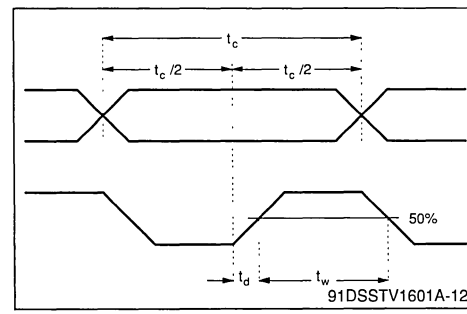
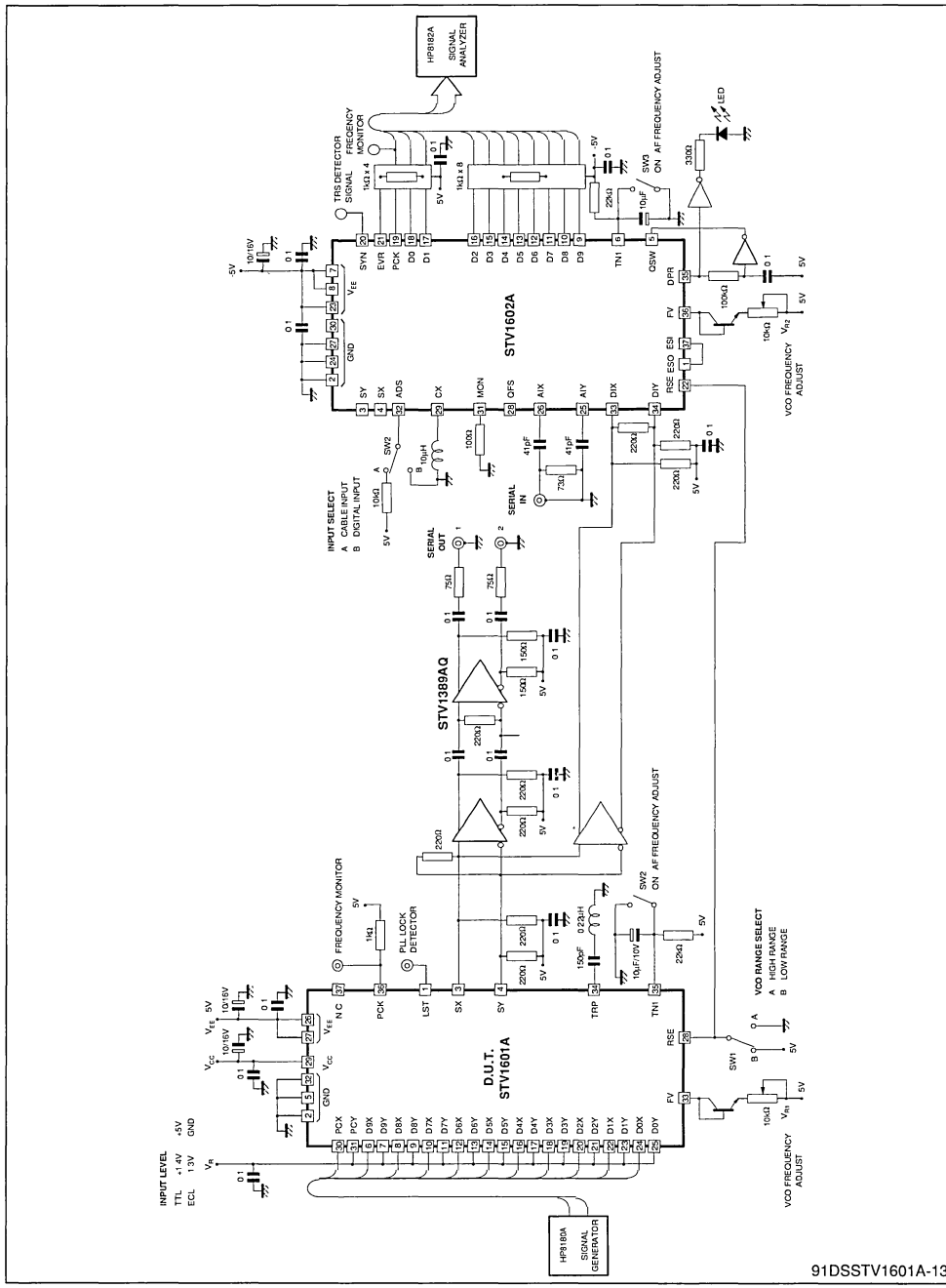


Figure 3 : Test Circuit Diagram Example



SGS-THOMSON MICROELECTRONICS

Figure 4

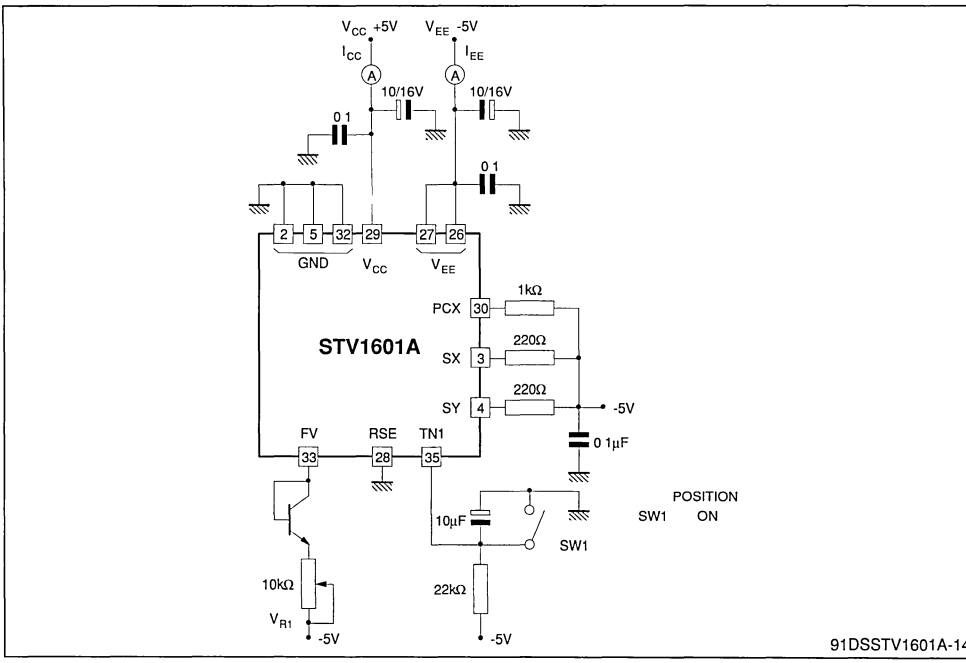


Figure 5

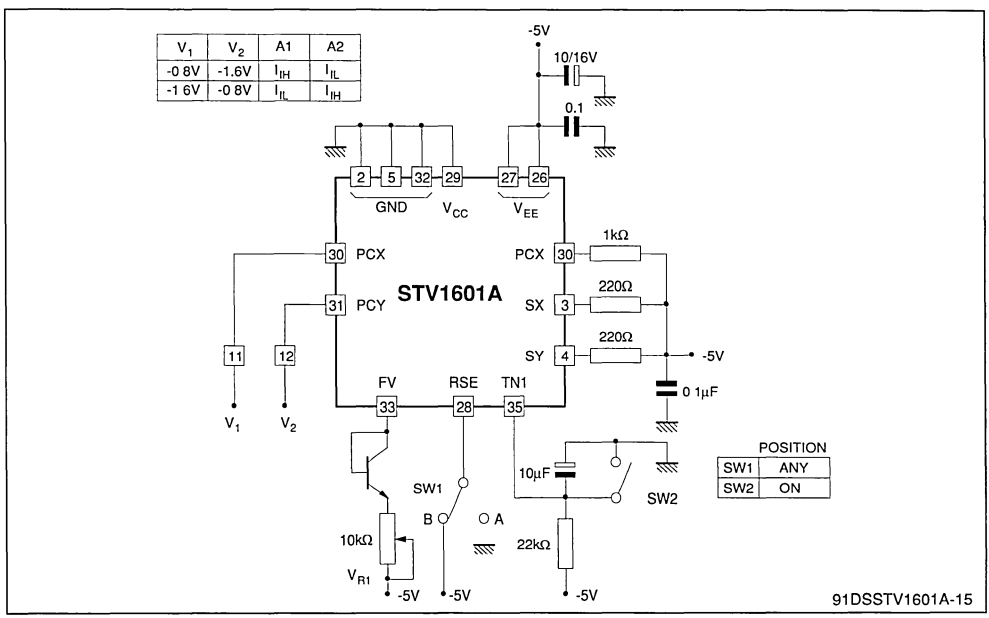


Figure 6

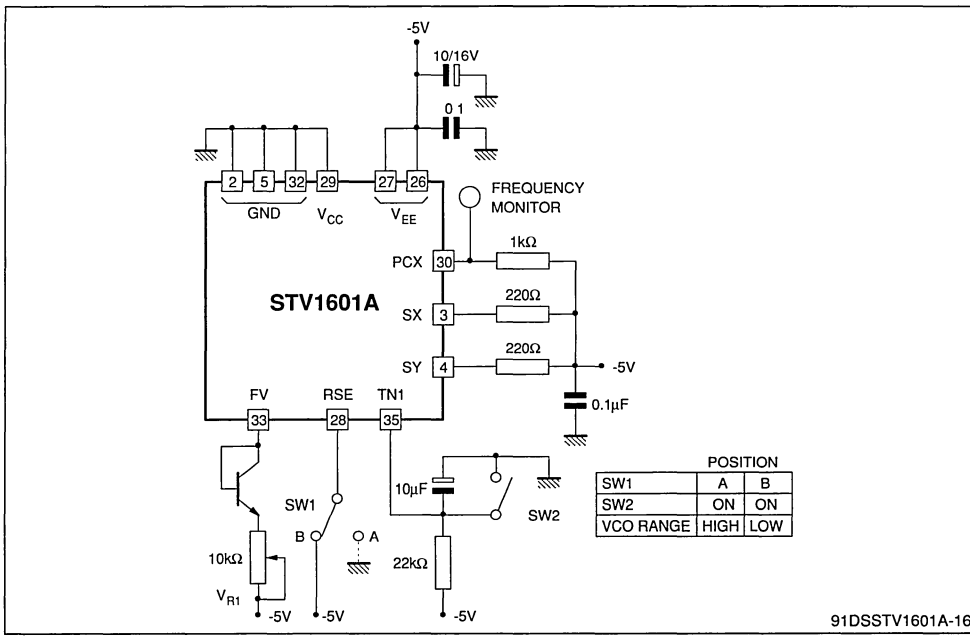


Figure 7

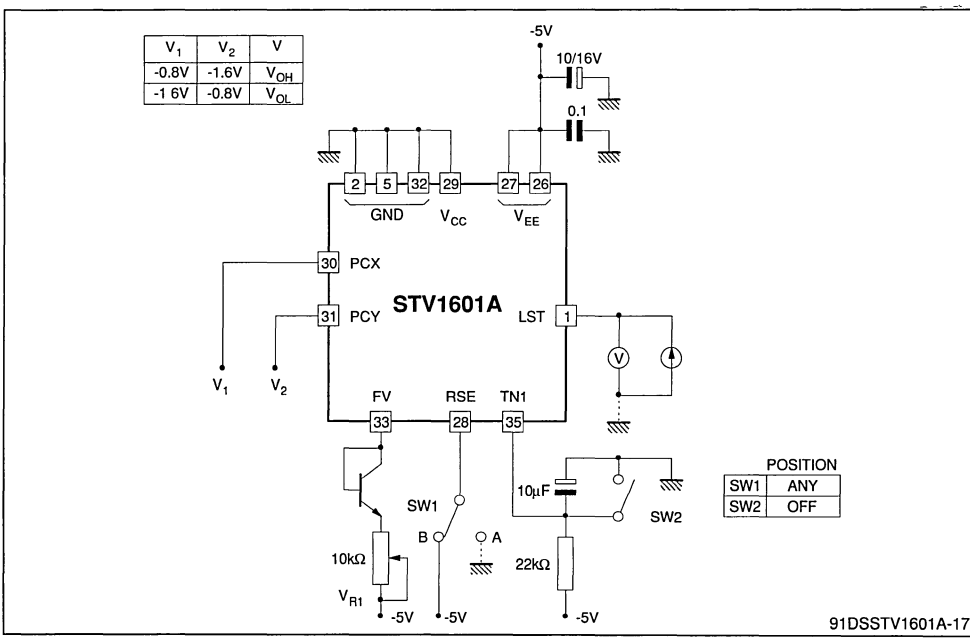


Figure 8

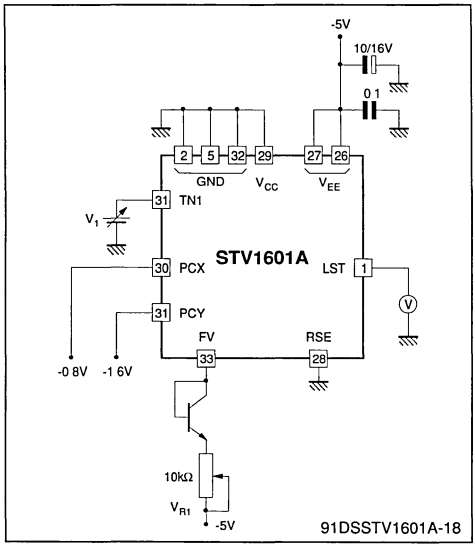


Figure 9

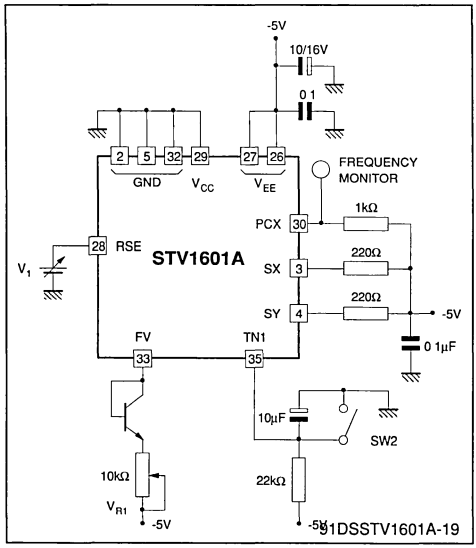
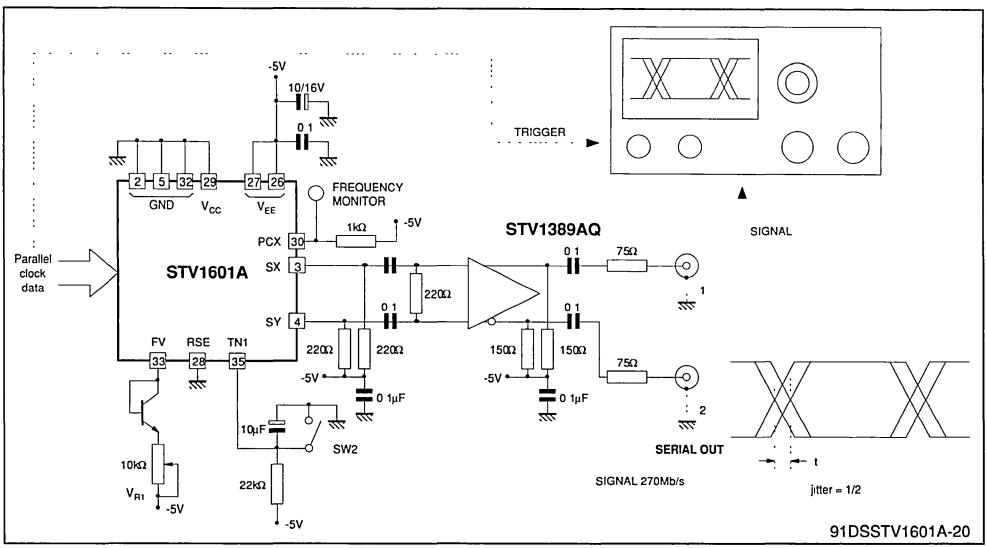


Figure 9



DESCRIPTION

STV1601A internally generates a 10 times clock frequency locked to the parallel input clock thanks to a built-in PLL and converts input parallel data into serial data.

To ease clock extraction at the receiving end, serial data is scrambled. To minimize polarity effect, serial data is then converted to NRZI and output in differential mode.

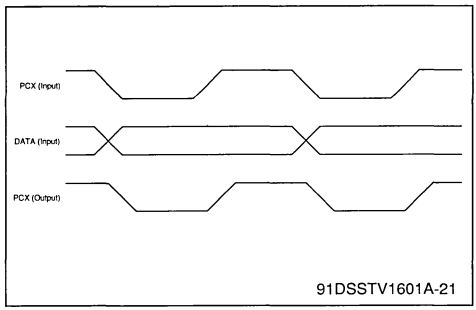
A PLL lock detection circuit only enables the serial output when locked.

1. Phase relation between input parallel clock and data

The phase relation between the parallel clock and the data is shown in Figure 11. Both clock and data are differential inputs

Parallel clock and data are such that the rising edge of PCX should be at the middle of the data. A clock having the same phase as PCX is internally generated in order to latch the data.

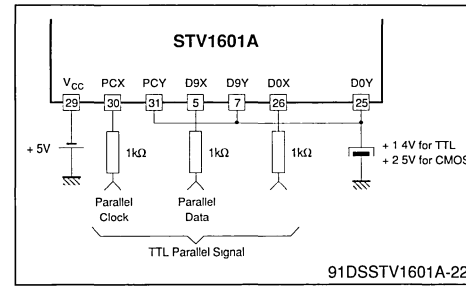
Figure 11 : Phase Relation between Clock and Data



2. TTL input operation

Parallel clock and data can be either TTL or ECL inputs. To use as TTL inputs VCC (Pin 29) shall be connected to +5V. A fixed bias of +1.4V shall be applied to PCY and DnY (n = 0 to 9). TTL signals and their parallel clock will be provided through 1kΩ resistors to each "X" input. These 1kΩ resistors are effective to minimize the influence of the TTL input signals to the jitter characteristics of the serial output signal. For 8-bit data, unused LSB(s) must be fixed Low. Fixed bias value can be higher, for example, 2.5V in case of CMOS inputs.

Figure 12 : TTL input operation



3. PLL block

Parallel clock input control

PLL, PLL lock detection and the various blocks of the serial output control are shown in Figure 13.

When TN1 is connected to GND (set High), the parallel clock input is disabled.

The VCO turns to free running conditions and its frequency can be adjusted through FV.

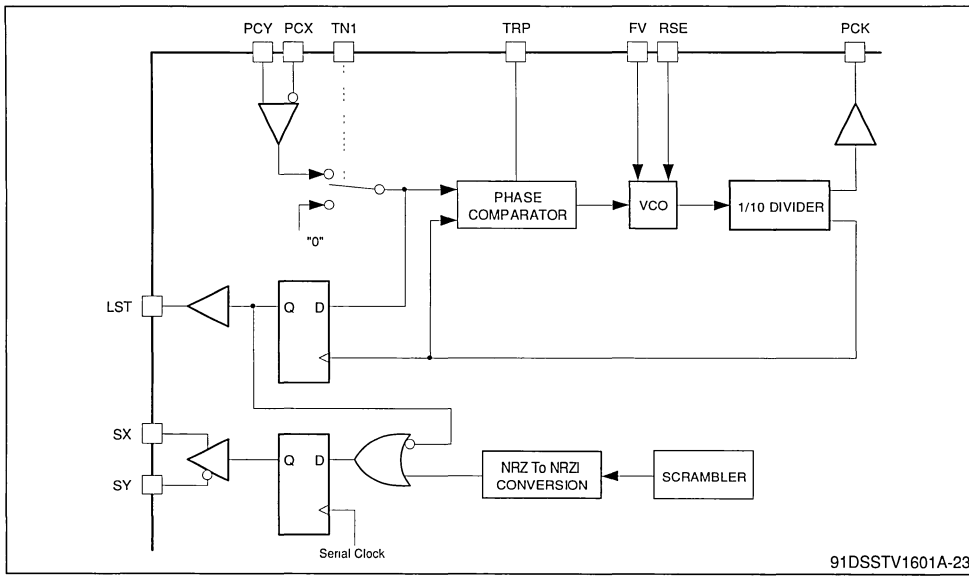
This frequency decreases when the resistor value between FV and V_{EE} is reduced. Oscillation frequency monotoring is performed through PCK which delivers a frequency divided by ten.

When PLL is locked, PLL and PCX input signal phases are nearly matched. The RC network connected to TN1, temporarily, disables the parallel clock in order to avoid mislocking problems.

VCO oscillation frequency range selection is available through RSE ; High : from 140 to 270MHz ; Low : from 100 to 145MHz.

TRP (Pin 34) is the phase comparator output. To minimize jitter, a trap circuit, consisting in a serial tuned circuit at parallel clock frequency can be used.

Figure 13 : PLL and Serial Output Control BLock



PLL lock detection

The LST signal is generated by latching the incoming parallel clock by the internal one (which is 1/10 of the VCO frequency). LST is used as a PLL lock detection signal and also controls the serial output. If the parallel clock input is disabled (by means of TN1), LST turns Low and the serial output is disabled as described in the previous section (SX (Pin 3) = High, SY (Pin 4) = Low).

If the serial output has to be disabled while no parallel clock input is provided, PCX must be set Low and PCY must be set High.

4. Sync word

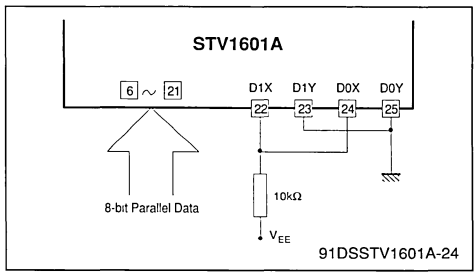
To convert serial data back to parallel, insertion of some timing reference data indicating the parallel data word boundary in the serial data is needed. This, called TRS (Timing Reference Signal) in the digital interface format, consists of the three consecutive words 3FFH, 000H, 000H.

Conversion to 10-bit TRS from 8-bit, 9-bit data (TRS)

8-bit parallel data

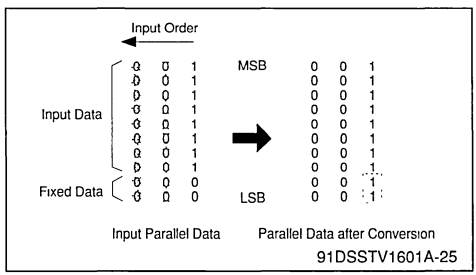
8-bit parallel data can be converted into 10-bit data by using the 8th bit as the MSB and by setting the 2 LSBs at logical states as shown in Figure 14.

Figure 14 : 8-bit Parallel Input Data (ECL level)



The conversion algorithm detects 2 successive 000H words and sets the two LSBs of the previous word, which is supposed to be FF, according to the standard.

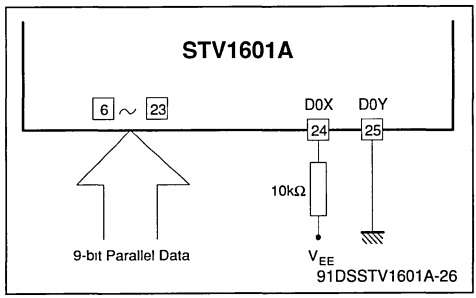
Figure 15 : Conversion from 8-bit TRS to 10-bit TRS



9-bit parallel data

Similary, 9-bit parallel input data can be accepted as shown in Figure 16.

Figure 16 : 9-bit Parallel Input Data (ECL level)



Conversion in the case of more than three successive "000H" words.

If more than 3 consecutive words of 000 in D1 standard, or 4 consecutive words of 000 in D2 standard occur at the parallel input it does not meet the SHPTE T14.224 proposed standard thus no proper operation is possible.

With TRS, the word before two successive "000H" is all "1". Internally, this word is checked and the two LSBs are set to "1".

5. Scrambling and NRZI conversion

Figure 20 shows the scrambling circuit, the scrambling polynomial is as follows : $x^9 + x^4 + 1$.

Figure 17 : $(x^9 + x^4 + 1)$ Basic Scrambling Circuit

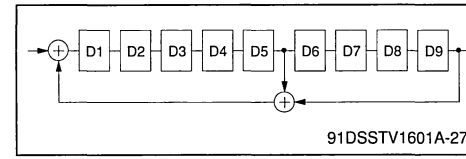
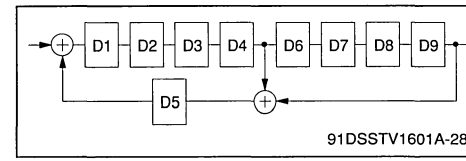


Figure 18 : $(x^9 + x^4 + 1)$ Actual Scrambling Circuit



To eliminate signal polarity of scrambled data, conversion from NRZ to NRZI is performed (Figures 11 and 12).

Therefore, the polarity for output distribution or receiving is not needed. This allows easy system design. The NRZ to NRZI polynominal is x + 1.

Figure 19 : NRZ To NRZI Conversion and NRZI to NRZ Conversion

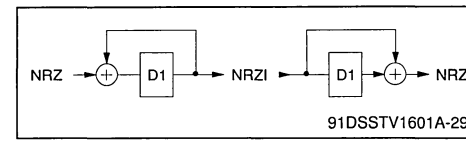
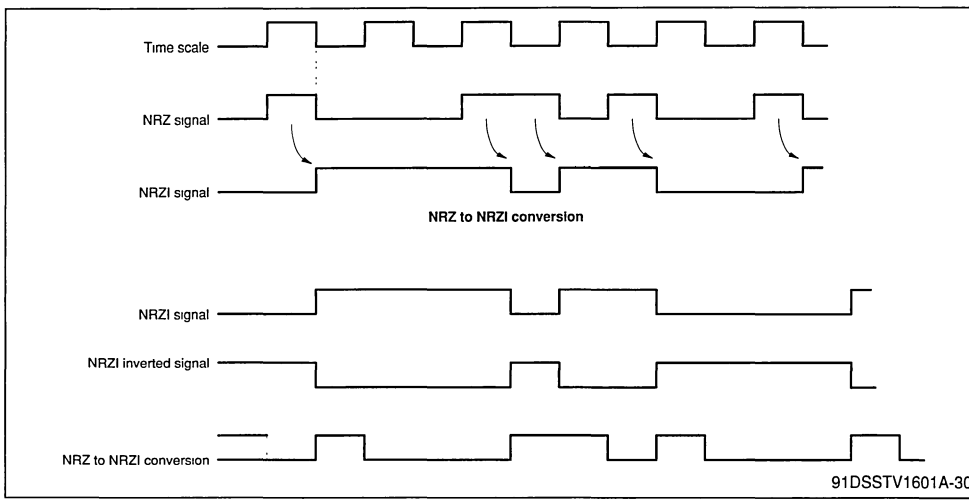


Figure 20 : Relation between NRZ and NRZI Signals



VCO temperature compensation and oscillation frequency adjustment

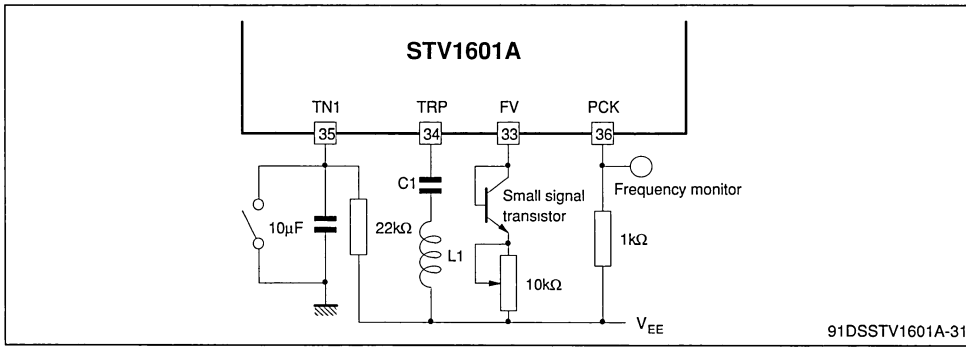
VCO oscillation frequency depends on the temperature as shown inFigures 23 and 24 "Representative characteristics examples". Within the normal range of operation, frequency increases with temperature. FV voltage remains almost constant regardless of temperature. Figure 21 shows an example of a temperature compensation circuit using a diode (transistor with C-B diode short-circuited) and a resistor connected between FV and V_{EE}. Examples of representative characteristics for various temperatures are shown in Figures 23 and 24 concerning oscillation frequency and PLL pull-in range (signal frequency 270, 177 and 143MHz).

VCO free running frequency adjustment

VCO free running frequency adjustment is performed at room temperature.

If TN1 is set High, VCO free runs. Wait for 5 to 10 minutes after turning power supply ON (warm up time). While monitoring PCK output (Pin 36) adjust the signal frequency (within ± 1%) with the variable resistor connected between FV and V_{EE}.

Figure 21 : VCO Temperature Compensation and Free Running Adjustment



Jitter trap

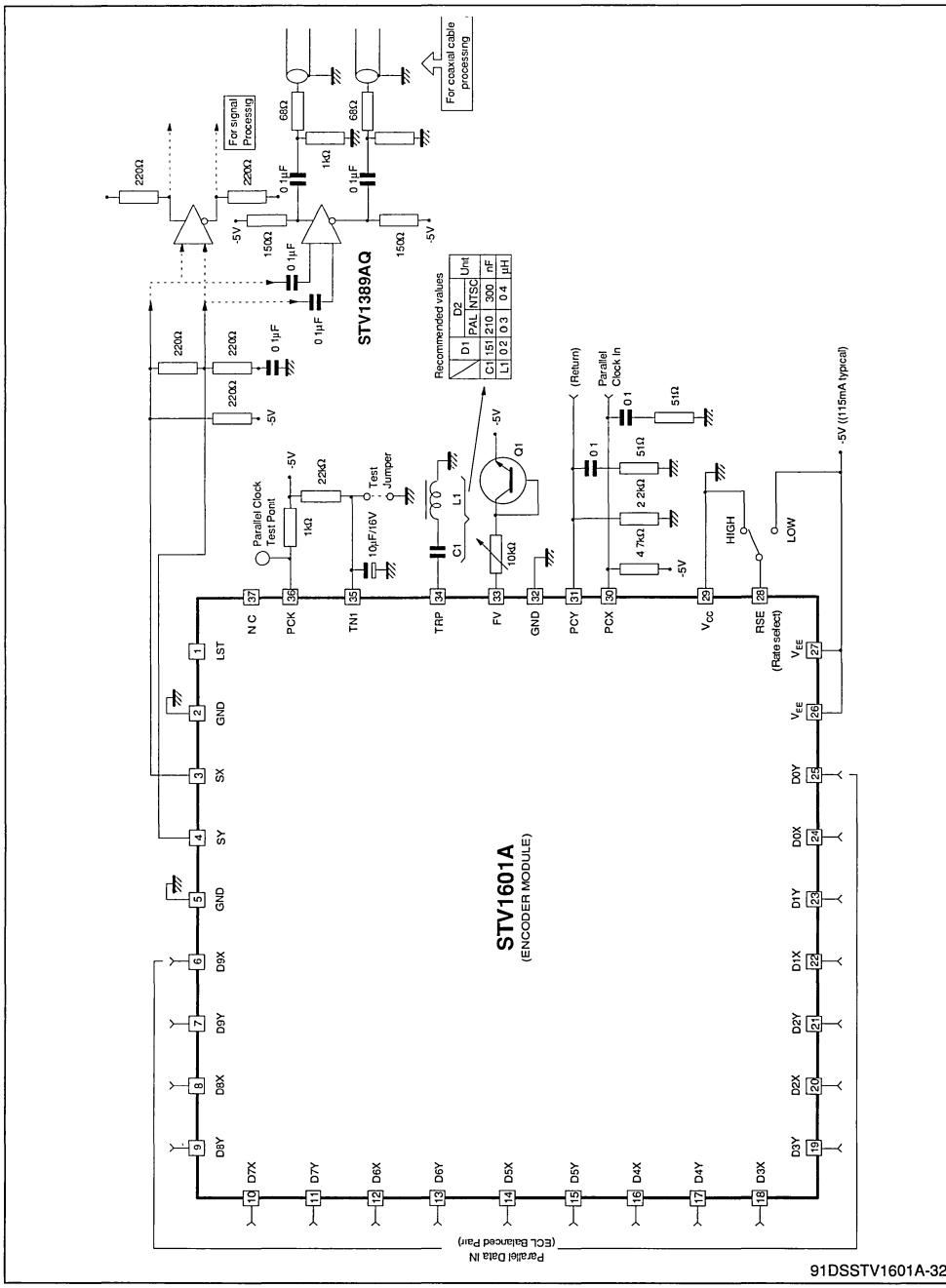
Since the internally generated serial clock is locked to the incoming parallel clock, there exists periodic jitter components which are generated from the phase comparison process of the PLL. A serial resonant circuit (trap) connected between TRP (Pin 34) and V_{EE} tuned at the parallel clock frequency reduces effectively the fundamental component of the jitter well below the specification (±0.25ns). Recommended values of C1 and L1 are given in the following table.

RECOMMENDED VALUES OF THE TRAP CIRCUIT

COMPONENT	STANDARD		
	D1	D2	
		PAL	NTSC
C1 (pF)	150	240	300
L1 (µH)	0.2	0.3	0.4

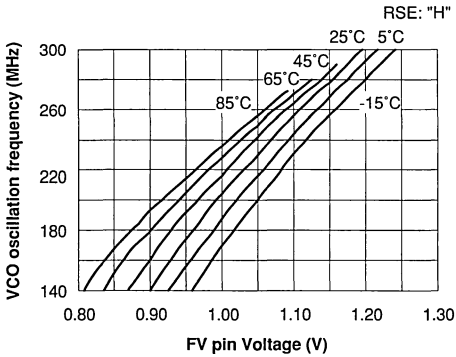
An important remark in a practical implementation is that TRP node is an input of a very sensitive voltage-frequency converter (VCO) which can be easily disturbed by any pick-up noise. Hence, the trap circuit should be carefully located and be kept as short as possible from the Pin 34 in order to avoid noise problems.

Figure 22 : Application Circuit Example



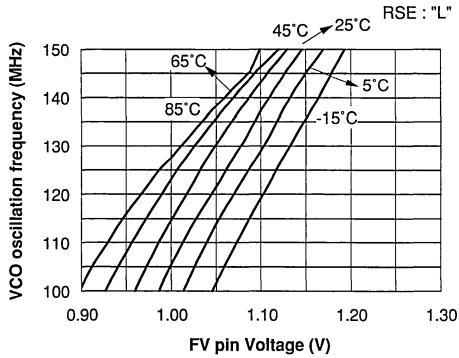
EXAMPLE OF REPRESENTATIVE CHARACTERISTICS

Figure 23 : VCO Oscillation Frequency versus FV Pin Voltage



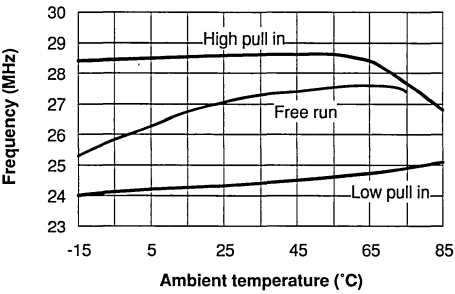
91DSSTV1601A-33

Figure 24 : VCO Oscillation Frequency versus FV Pin Voltage



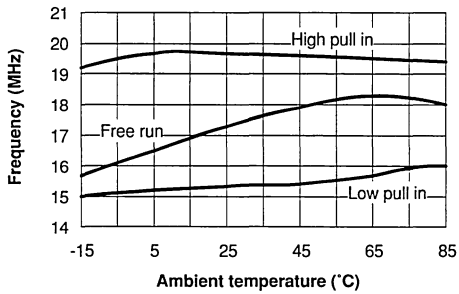
91DSSTV1601A-34

Figure 25 : Pull in Range and Free Run Frequency (270Mb/s)



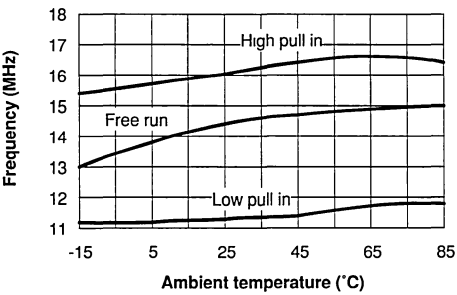
91DSSTV1601A-35

Figure 26 : Pull in Range and Free Run Frequency (177Mb/s)



91DSSTV1601A-36

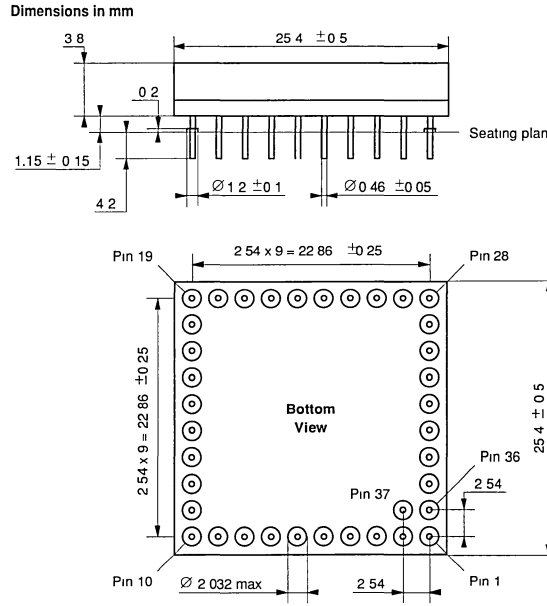
Figure 27 : Pull in Range and Free Run Frequency (143Mb/s)



91DSSTV1601A-37

PACKAGE MECHANICAL DATA

37 PINS - CERAMIC PGA

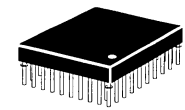


SERIAL INTERFACE TRANSMISSION DECODER

PRELIMINARY DATA

BUILT-IN AUTOMATIC EQUALIZER FOR UP TO 30dB ATTENUATION AT 135MHz (TYPICALLY 300m OF HIGH-GRADE COAXIAL CABLE), PLL CIRCUIT FOR RECLOCKING, AND SERIAL-PARALLEL CONVERSION CIRCUIT.
THIS SERIAL TRANSMISSION DECODER REQUIRES ONLY FEW EXTERNAL COMPONENTS.
OTHER RELATED IC's INCLUDE :

- STV1601A, A SERIAL TRANSMISSION ENCODER (PARALLEL-TO-SERIAL CONVERSION)
- STV1389AQ COAXIAL CABLE DRIVER



PGA37
(Ceramic Package)

ORDER CODE : STV1602A

STRUCTURE

- Hybrid IC

APPLICATIONS

SERIAL DATA TRANSMISSION DECODER
- 100 to 270 Mb/s

APPLICATIONS EXAMPLES
- Serial data transmission of digital television signals 525-625 lines
- 4:2:2 component 270Mb/s (10-bit)
- 4*fsc PAL composite 177Mb/s (10-bit)
- 4*fsc NTSC Composite 143Mb/s (10-bit)

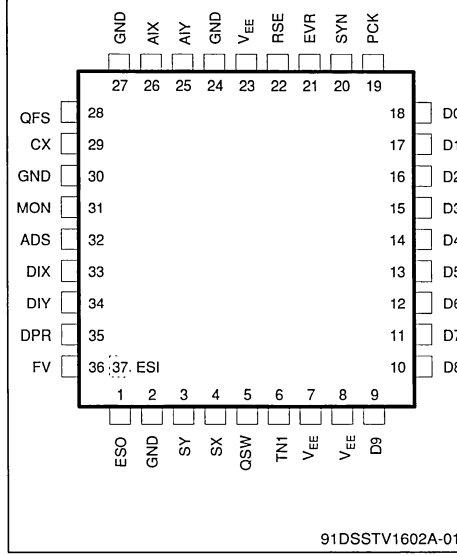
FUNCTIONS

- Cable equalizer
  (maximum gain : 30dB at 135MHz)
- PLL for serial clock generation
- Reclocked repeater output (active loop through)
- Descrambler : modulo-2 multiplication by
  $G(x) = (x^9 + x^4 + 1)(x + 1)$
- Parallel-to-serial conversion
- Sync monitor output
- Eye pattern monitoring
- Input signal detector

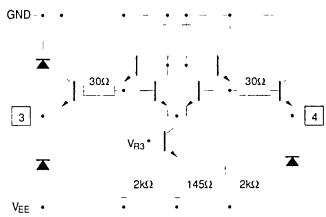
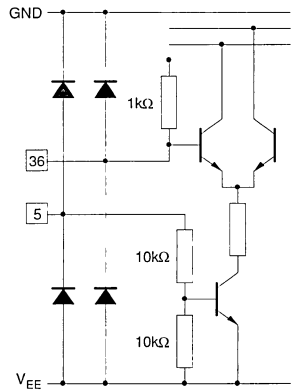
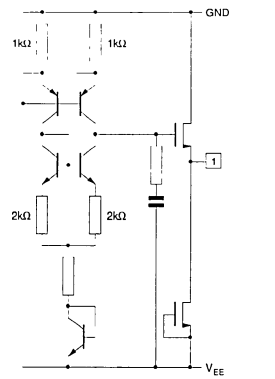
DESCRIPTION

The STV1602A is a Hybrid IC decoder which converts serial data coming from a serial transmission line into parallel data.

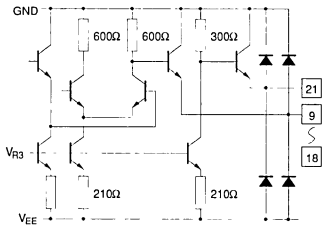
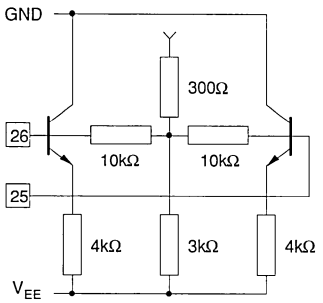
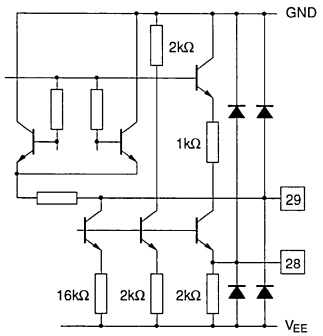
PIN CONNECTIONS



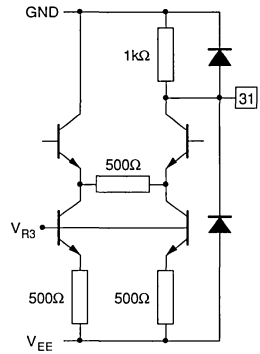
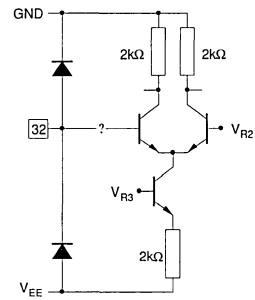
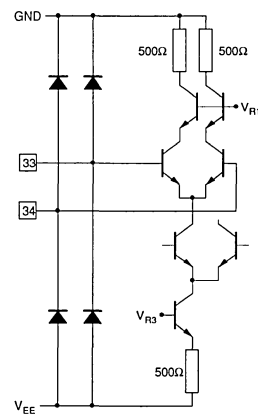
PIN DESCRIPTION

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
3	SY	 91DSSTV1602A-02	Reclocked serial data output in differential mode. SX and SY are disabled when TN1 is set High. In this case, SX is set High and SY is set Low H L	O		 -1.6 -2.4		 V V
4	SX							
5	QSW (GND)	 91DSSTV1602A-03	To be connected to GND	I				
36	FV		Adjustment of VCO Free running frequency : V_{EE} level gives the lowest frequency. To adjust it, set TN1 High.	I				
1	ESO	 91DSSTV1602A-04	Output of phase comparator must be connected to ESI with shortest distance	O		-3.2		V

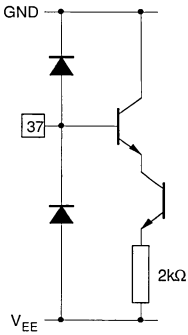
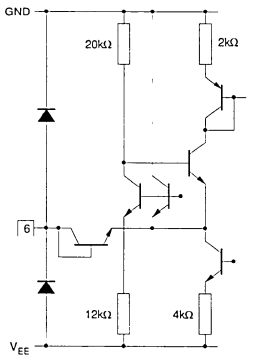
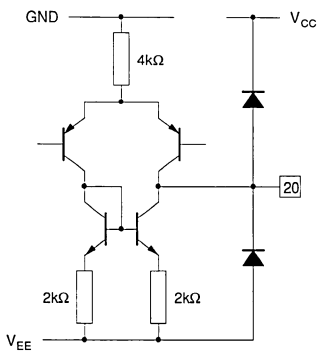
PIN DESCRIPTION (continued)

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
9 to 18	D9 to D0	 91DSSTV1602A-05	Parallel data output H L	O		 -0.8 -1.6		 V V
19	PCK		Parallel clock output (rising edge at data center) H L	O		 -0.8 -1.6		 V V
21	EVR		Data output reference potential	O		-1.2		V
26	AIX	 91DSSTV1602A-06	Equalizer differential input	I		-2.0		V
25	AIY							
28	NC	 91DSSTV1602A-07	To be left open	I		-4.6		V
29	CX		Equalizer detector output; Input signal : absent present	O		 -2.4 -2.0		 V V

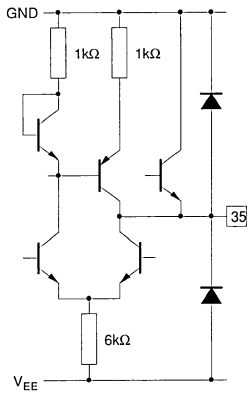
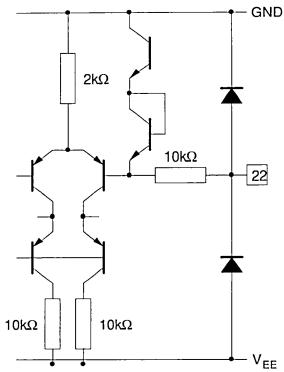
PIN DESCRIPTION (continued)

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
31	MON	 91DSSTV1602A-08	Equalizer monitor output. Connect 75Ω resistor between MON-GND. Observe using a 50Ω input oscilloscope at the 75Ω coaxial cable.	O		15		mV (pp)
32	ADS	 91DSSTV1602A-09	Serial data input selection High : Digital input DIX/DIY Low : Equalizer input AIX/AIY H L	I	 -0.5		 -1.5	 V V
33	DIX	 91DSSTV1602A-10	Serial data digital differential input	I				
34	DIY		Selected when ADS is High. H L		 -1.0		 -1.6	 V V

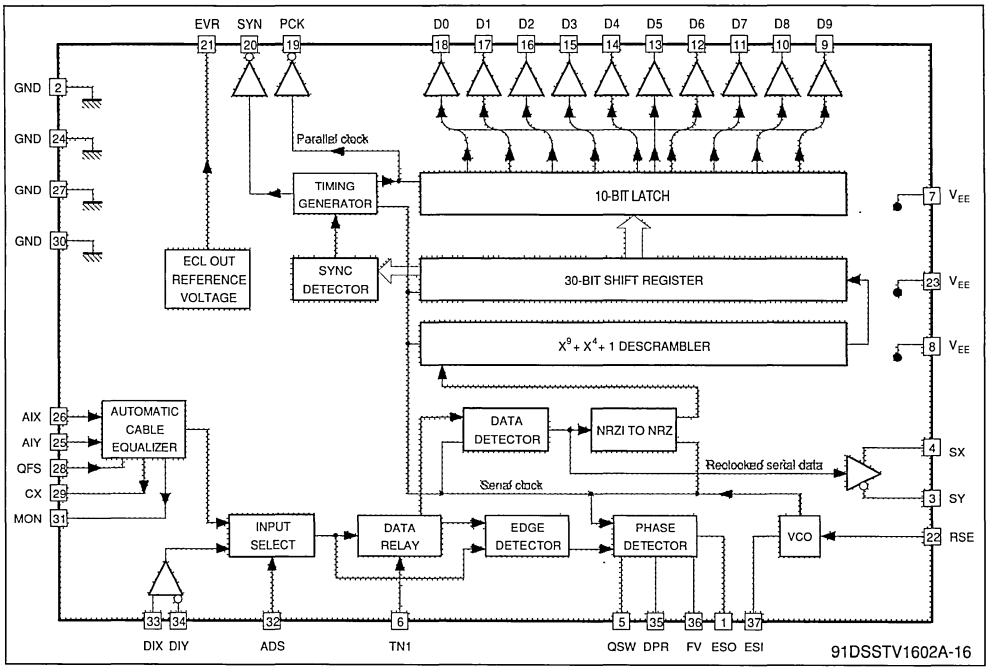
PIN DESCRIPTION (continued)

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
37	ESI	 91DSSTV1602A-11	PLL error signal input : must be connected to ESO with the shortest distance	i		-3.2		V
6	TN1	 91DSSTV1602A-12	Serial data input activation High : Input disabled (VCO free running condition). Low : Input enabled. During switch-on phase, by temporarily hold High for quick start-up	I	-1.0		-4.0	V V
20	SYN	 91DSSTV1602A-13	State changes at each TRS Sync word 3FFH 000H 000H H L	O	-1.0		-4.0	V V

PIN DESCRIPTION (continued)

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
35	DPR	 91DSSTV1602A-14	Serial data detection output. When there is an input signal at the input side selected through ADS, this pin goes High. At no signal, it goes Low. H L i.e. - present : High - absent : Low	O	 -1.0		 -4.0	 V V
22	RSE	 91DSSTV1602A-15	Selects VCO frequency range H : High range 140 to 270MHz L : Low range 100 to 145MHz H L	I	 -4.0		 -4.0	 V V
7 23	V_{EE}		-5V supply I/O buffer, PLL equalizer		-5.2	-5.0	-4.8	V
8	V_{EE}		-5V Supply Logic part		-5.2	-5.0	-4.8	V
2 24 27 30	GND		GND					

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-6	V
V_{IN}	Input Voltage	V_{EE} to 0	V
I_{OUT}	Output Current	-30	mA
T_{oper}	Operating Temperature	0 to 65	°C
T_{stg}	Storage Temperature	-50 to 125	°C
P_D	Allowable Power Dissipation	2.0	W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-4.8 to -5.2	V
T_{oper}	Operating Temperature	0 To 65	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	TYp.	Max.	Unit
DC CHARACTERISTICS							
I_{EE}	Supply Current	V_{EE} = 5V	Figure 4		185		mA
V_{IH}	Input Voltage	Pin ADS		-0.4			V
V_{IL}						-1.5	V
V_{IH}		Pin RSE	Figure 10	-0.4			V
V_{IL}						-4.0	V
V_{IH}		Pin DIX, DIY		-1.0			V
V_{IL}						-1.6	V
I_{IH}	Input Current	Pin DIX, DIY	Figure 5			5.0	µA
I_{IL}				-1.0		+1.0	µA
V_{IH}	Input Voltage	Pin QSW		-0.5			V
V_{IL}						-4.6	V
V_{IH}		Pin TN1	Figure 9	-1.0			V
V_{IL}						-4.6	V
V_{OH}	Output Voltage	Pin PCX, Dn R_P = 1kΩ			-0.8		V
V_{OL}					-1.6		V
V_M		Pin EVR, R_P = 1kΩ			-1.2		V
V_{OH}		Pin DPR, SYN I_{OH} = -10µA, I_{OL} = +10µA	Figure 7	-1.0			V
V_{OL}			Figure 8			-4.0	V
V_{OH}		Pin SX, SY R_P = 220Ω			-1.6		V
V_{OL}					-2.4		V
AC CHARACTERISTICS							
f_{MAX1}	VCO Max. Oscillation Frequency 1	RSE = "H"	Figure 6	30.0			MHz
f_{MIN1}	VCO Min. Oscillation Frequency 1	RSE = "H"				14.0	MHz
f_{MAX2}	VCO Max. Oscillation Frequency 2	RSE = "L"		15.0			MHz
f_{MIN2}	VCO Min. Oscillation Frequency 2	RSE = "L"				10.0	MHz
f_{HP1}	PLL Pull in Range	f signal = 270MHz RSE = "H"	Figure 3	27.7			MHz
f_{LP1}						25.5	MHz
f_{HP2}		f signal = 177MHz RSE = "H"		18.5			MHz
f_{LP2}						16.8	MHz
f_{HP3}		f signal = 143MHz RSE = "H"		15.0			MHz
f_{LP3}						13.3	MHz
f_{OP1}	PLL Generator Frequency	RSE = "H"		14.0		27.0	MHz
f_{OP2}		RSE = "L"		10.0		14.5	MHz

Frequency at 1/10 the value of signal frequency (Tested through Pin PCK).

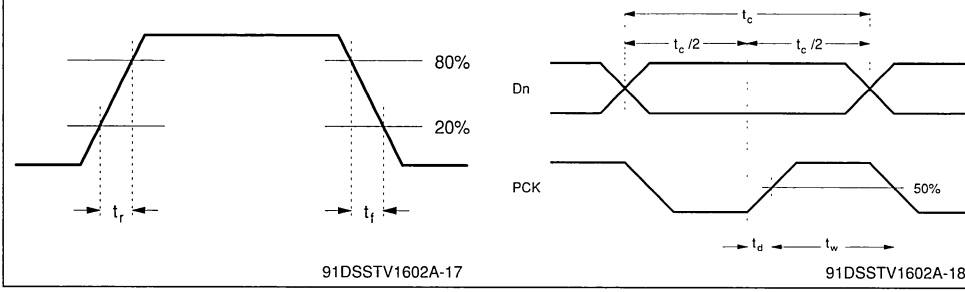
SWITCHING CHARACTERISTICS (V_{EE} = -5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
t_r	Rise Time	Pins PCK, Dn R_P = 1kΩ	Figure 3		0.8		nsec
t_f	Fall Time				1.4		nsec
t_r	Rise Time	Pins SX, SY R_P = 220Ω			0.7		nsec
t_f	Fall Time				0.7		nsec
t_d	Delay Time	Pins PCK, Dn		-5		+5	nsec

EQUALIZER (V_{EE} = -5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
V_{MAX}	Equalizer Max. Input Voltage	Pins AIX, AIY	Figure 3	0.88			Vp-p
G_{MAX}	Equalizer Max. Gain				30		dB
C_{IN}	Input Capacity	Pins AIX, freq = 100MHz					pF
R_{IN}	Input Resistance	Pins AIX, freq = 100MHz					Ω

Figure 1 : t_r, t_f, t_c, t_d Definition



SYN pin guaranteed operation range.

SYNC pin and serial to parallel conversion operate normally within the frequency and ambient temperature ranges according to Figure 2.

Serial output pin use.

Normal use of the STV1602A is to convert serial data into parallel data. Output serial data is also available. However, when this output is used, the PLL is affected and in some instances, bit slip errors will be generated during long runs of 0 or 1.

Serial output operation is checked (TRS can be detected from the output) but characteristics cannot be guaranteed. Moreover, simultaneous use of parallel and serial outputs is not advised due to higher power consumption.

When both parallel and serial outputs are needed, use STV1601A to convert the parallel output to serial.

Power saving in repeater mode

Since the parallell output is not always required for a reclocked repeater, the chip has been designed such that the uncessary parallel logic circuit can be disabled by disconnecting Pin 8, one of V_{EE}s, from the power supply. With this arrangement the power dissipation is reducible to about 45 percent of that of the fully functional mode.

In practice, a test switch should be provided so that some parallel signals may be available during adjustment procedures as shown in Figure 2.

Figure 2 : A Suggested Parallel Clock / Data Output Circuit

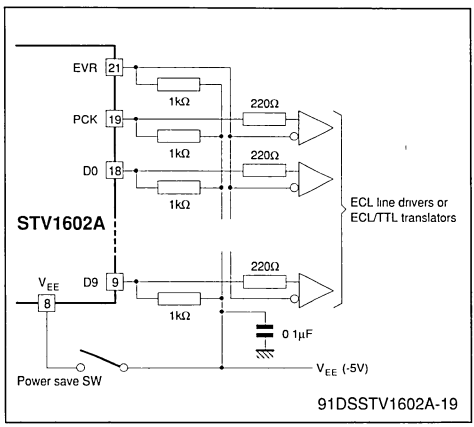


Figure 3 : Test Circuit Diagram Example

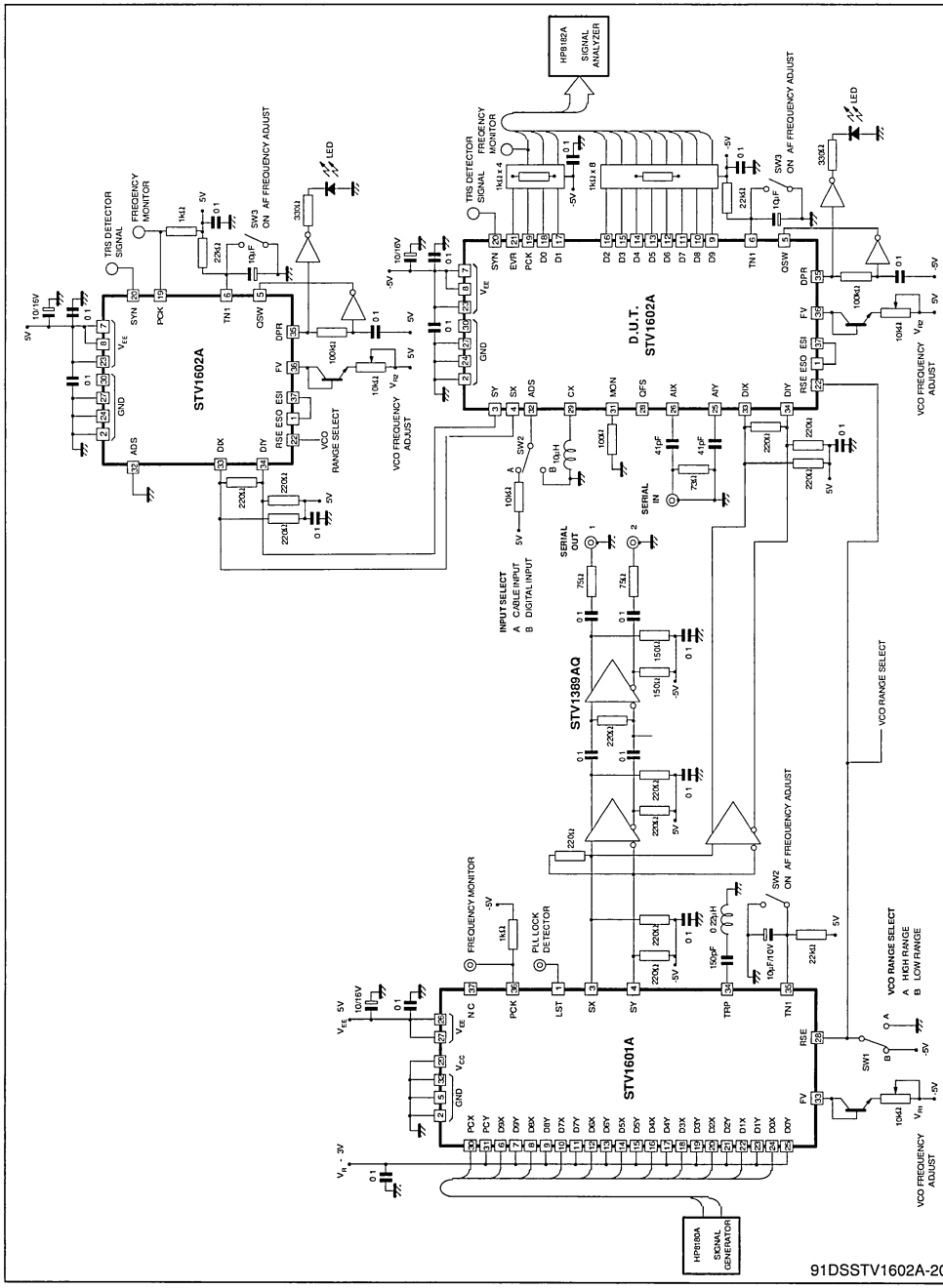


Figure 4

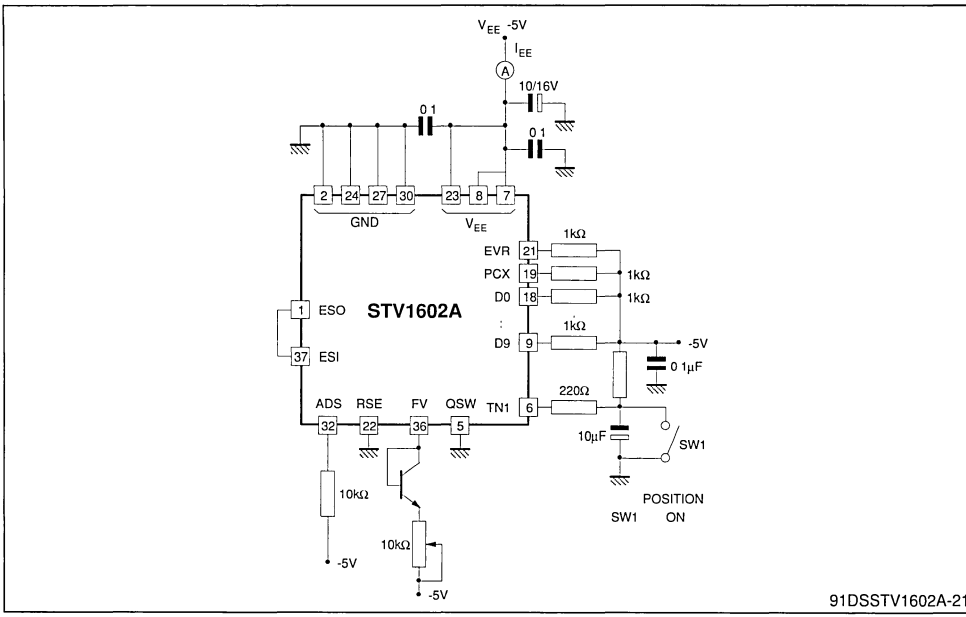


Figure 5

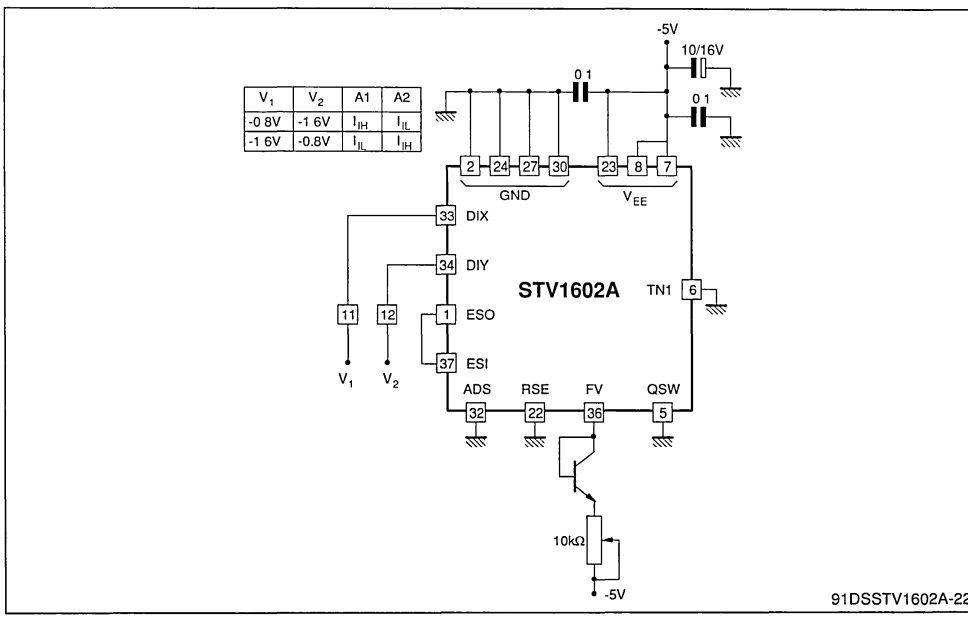


Figure 6

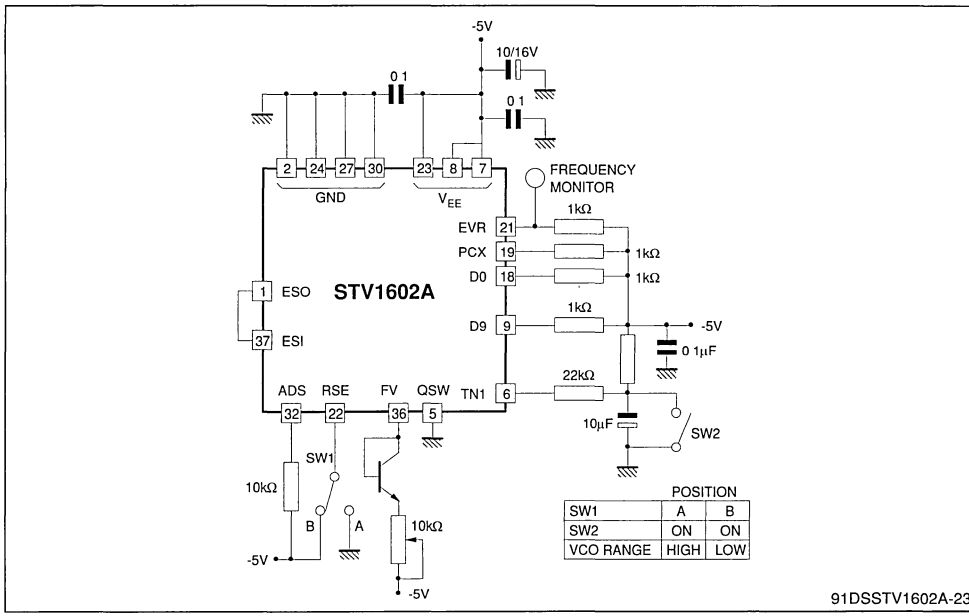


Figure 7

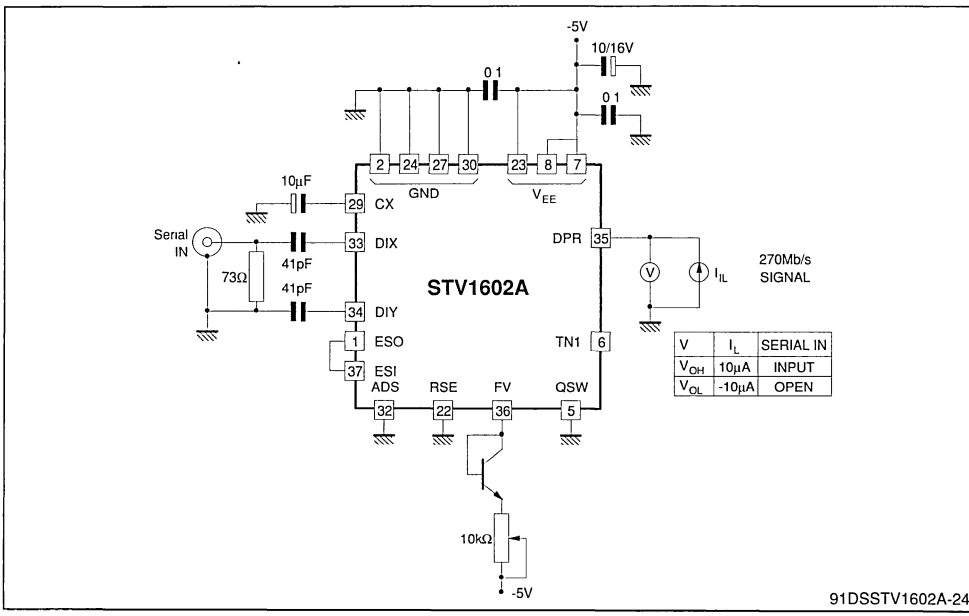


Figure 8

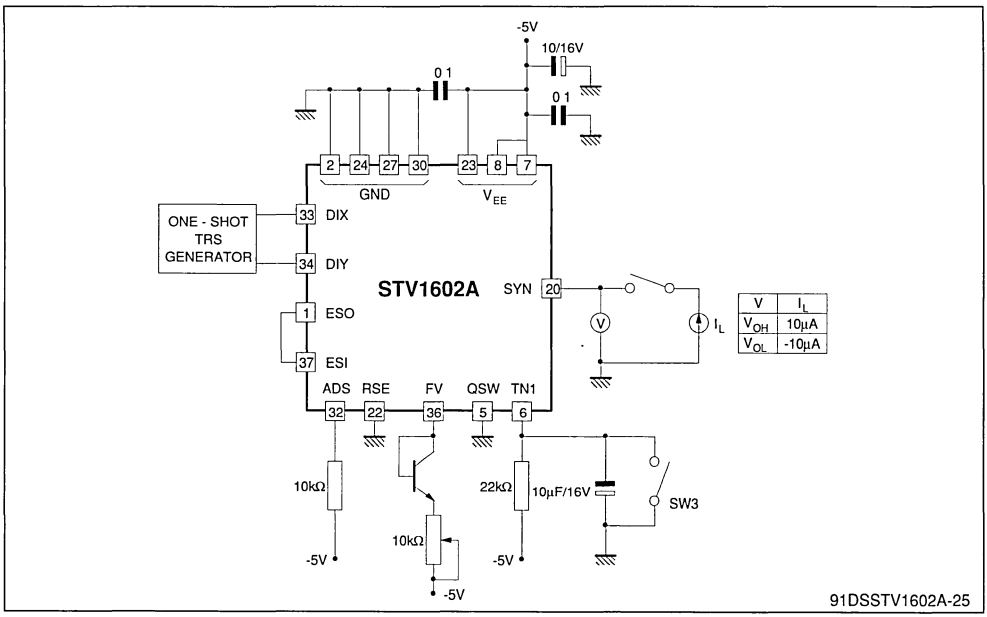


Figure 9

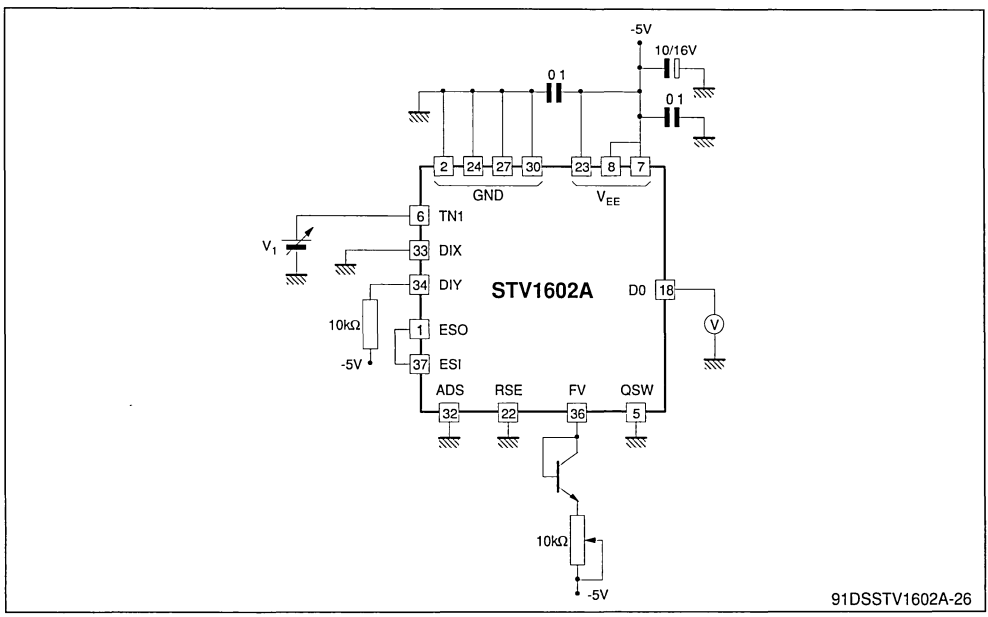
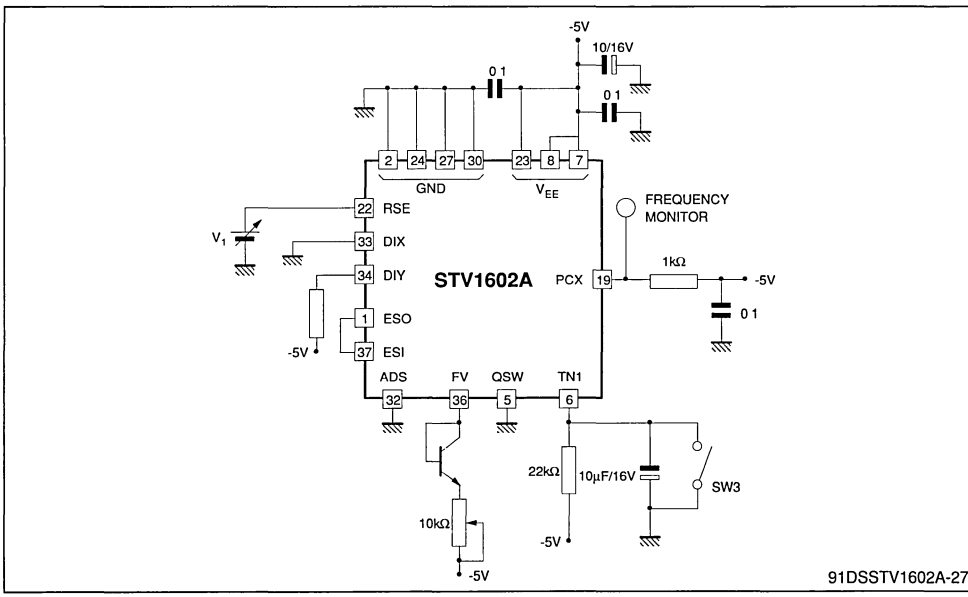


Figure 10



STV1602A GENERAL

As shown in the overall block diagram on page 7, STV1602A is composed of the following functions :

(1) Analog input as a primary input with automatic equalizer to meet the loss characteristics of coaxial cable
(2) Digital input as a secondary input to receive the encoded signal from short distances within the same printed circuit board or the same equipment
(3) Phase locked loop (PLL) variable oscillator
(4) Reclocked serial output
(5) Serial descrambler
(6) SYNC detector
(7) Deserializer
(8) Parallel output buffer amplifiers
(9) Three diagnostic signals : eye monitor, SYNC monitor and input data presence monitor

A briaf explanation of each function is given in the following sections.

1. Cable equalizer

Transmission of high speed digital data by means of coaxial cable can greatly attenuate high frequency components. According to the cable length, received signals can widely differ from those sent; in such conditions, clock extraction and data identification could be difficult.
The cable equalizer overcomes this problem.
The IC performs up to 30dB (typical) equalization at 135MHz, typically 300m of high-grade coaxial cable. The equalization is automatically performed according to the coaxial cable length.
The input signal can be delivered either through a transformer or through a capacitor.
When the digital input is selected, the equalizer is disabled.

Figure 11 : Equalizer Capacitor Coupling Input Circuit

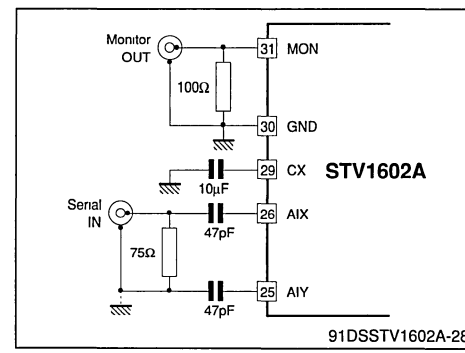
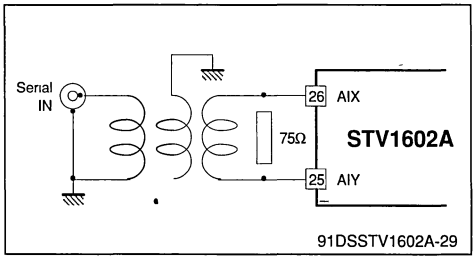
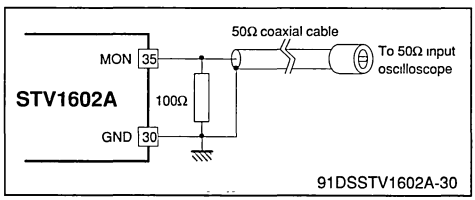


Figure 12 : Equalizer Transformer Input Circuit



MON Pin (31)
Equalized signals can be observed at this pin by connecting an oscilloscope input (50Ω).

Figure 13 : Equalized Waveforms Monitoring



CX Pin (29) Equalizer detection output
Connect a 10µF capacitor between this pin and GND. According to input signals, voltage changes from -2V to -2.4V can occur.

Figure 14 : An example of technique to improve the return-loss figure for the capacitor coupling input case

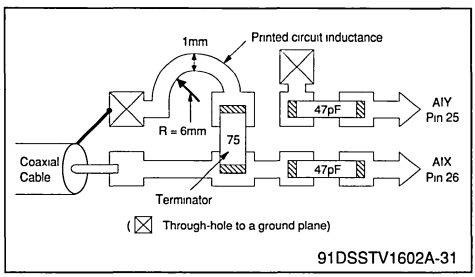
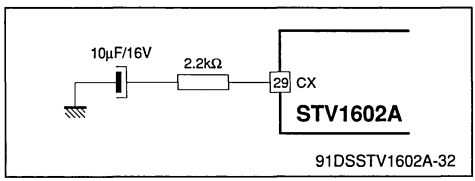


Figure 15 : AGC Time Constant

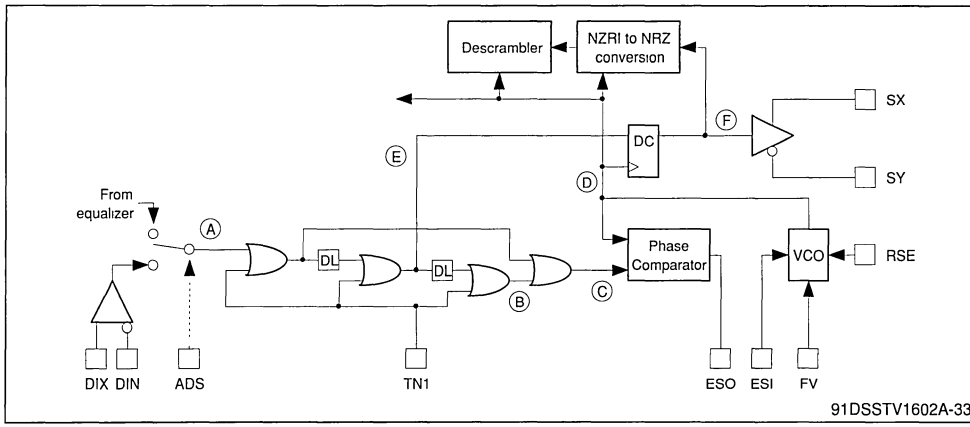


2. Digital input
The serial data input can be used without the equalizer.
DIX (Pin 33) and DIY (Pin 34) are differential inputs for ECL signals.
From these pins, input signals are differentially amplified, therefore with no input signals, the data detection signals could go High and erroneous data would be transferred to the parallel output.
To avoid this, a voltage level conforming to ECL specifications must be applied between DIX and DIY pins.
Also, while the analog input is in use, digital input must be kept "quiet" in order to avoid possible errors caused by cross-talk. This cross-talk problem naturally gets most severe when the analog input cable length is close to the limit of the transmission capability.

3. Serial input selection
Selection of the serial input is performed by ADS (Pin 32); when High the digital input is enabled; this input can be used for very short transmission lines. When Low, the equalizer input is enabled; this input must be used for long transmission lines.

4. PLL
In order to extract clock signals from the equalized serial data, it is processed to generate edge signals which are sent to the phase comparator.
When the PLL is locked, the identifier clock (D - flipflop) will be in phase with the incoming clock. The identifier clock rises at the center of the data period for easy identification.
The PLL detailed block diagram is shown in Figure 16.
ESI is the VCO control input (Pin 37). Normally, the phase comparator output ESO (Pin 1) is connected to ESI.
Through FV (Pin 35) one can adjust the free running frequency; when the FV Voltage is equal to V_{EE}, the free running frequency is the lowest; the voltage adjustment can be performed by using a variable resistor connected between FV and VEE.
RSE (Pin 22) selects the VCO frequency range; High : 140 to 270MHz, Low : 100 to 145MHz.
When TN1 (Pin 6) is set High, input signals are disabled and the VCO free runs. The capacitor connected between TN1 and GND avoids mislocking problem when the power supply is switched on.

Figure 16 : Serial Data Input and PLL



Data detection

Serial data edges are detected and go through low pass filter. The processed signal is available at DPR (Pin 35).DPR goes High when an input signal is detected, otherwise it stays Low.

The driving capability of this pin is weak. It is recommended to load it with a high impedance CMOS or equivalent.

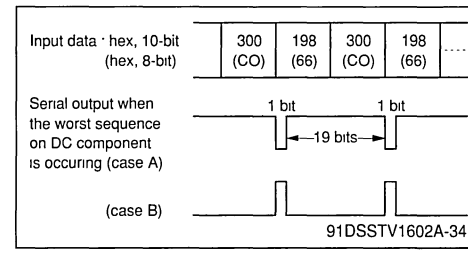
Using particular codes to check overall performance

Althrough the scrambling method employed in the proposed SMPTE standard effectively randomizes the incoming data and puts out a signal with a nearly uniform spectrum, there still exist some combinations of codes that give somewhat unfriendly conditions to the transmission path in terms of low frequency component or of a long run without any transitions.

As shown in Figure 17, it is known that if the code words 300, 198 (hex, 10-bit) are given alternately to the parallel input of the encoder, the largest amount of DC component (nearly one TV line period) can be produced at some place with a certain probability (such a sequence is, however, destroyed when different data is input to the encoder).

Even with such signals, error-free reception is possible with the STV1602A if a proper implementation is made (refer to section 12 for a recommended circuit).

Figure 17



5. NRZI To NRZ conversion, descrambler

Serial data delivered by the identifier is available in differential mode, SX (Pin 4) and SY (Pin 3). At the same time, to recover the original data, NRZI to NRZ conversion and descrambling are performed.

Figure 18 : $x^9 + x^4 + 1$ Descrambler

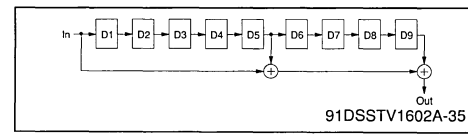
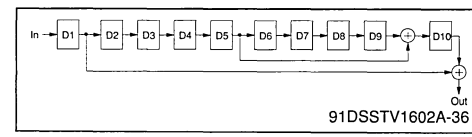


Figure 19 : Actual $x^9 + x^4 + 1$ Descrambler



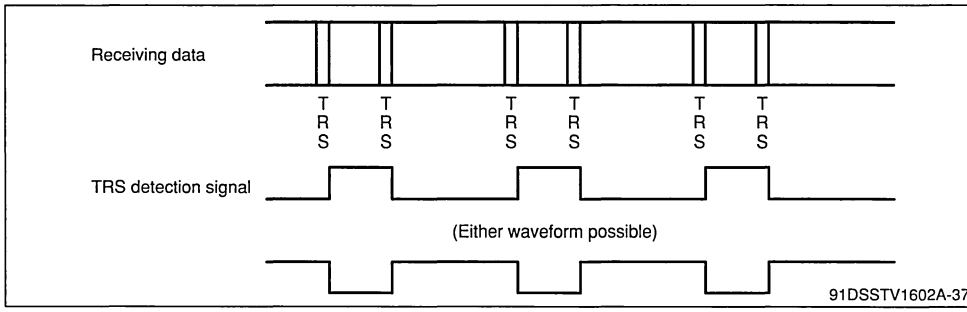
6. Serial to parallel conversion

After descrambling, serial data is sent to a 30-bit register to detect the sync word (TRS). When the sequence 11111111110000000000000000000000 is detected, sync word detection signal is output, the counter which divides the clock frequency by 10 is initialized and data is converted to parallel (10-bit word) to be output.

Each time the sync word is detected, SYN (Pin 20) changes state as shown in Figure 20.

As SYN driving capability is weak, the time relation with the parallel data is not constant. Parallel data processing using this signal is not possible.

Figure 20 : TRS Insertion Example and the Indicated Condition Resulting from TRS Detection



7. Phase relation ship between parallel data and parallel clock

Parallel data and clock are output so that the rising edge of the parallel clock is located at the center of the parallel data. Both parallel data and clock (ECL single output) have DC levels depending on the temperature. In order to simplify the driving amplifier, a reference level (EVR) is available at Pin 21. PCX, Dn and EVR use pull down resistors (identical values). A peripheral circuit example is shown in Figure 22. Figure 23 shows a circuit to disable the parallel clock output.

Figure 21 : Phase Relation of Parallel Clock, Data and EVR Voltage Level

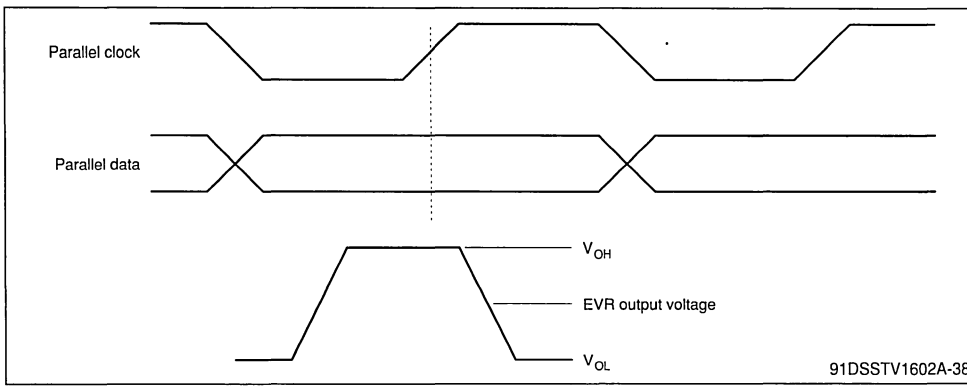


Figure 22 : Parallel Clock Data Output Circuit

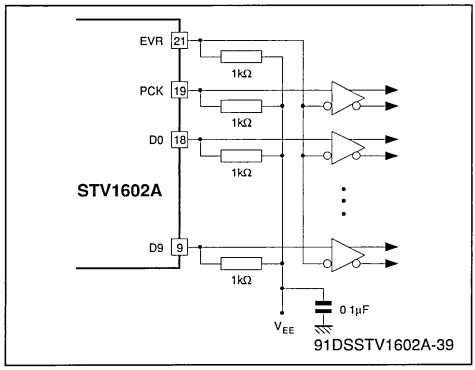
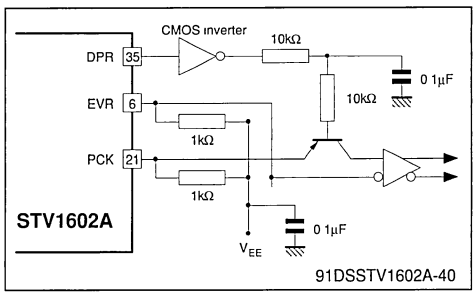


Figure 23 : A Circuit Example to Disable Parallel Clock



8. VCO temperature compensation and oscillation frequency adjustment.

VCO oscillation frequency depends on the temperature as shown in Figures 26 and 27 "Representative characteristics example". Within the normal range of operation, frequency increases with temperature.

FV pin voltage remains almost constant regardless of temperature.

Figure 24 shows an example of a temperature compensation circuit using a diode (transistor with C-B diode short-circuited) and a resistor between FV and V_{EE}.

PLL pull-in range (signal frequency 270, 177 and 143MHz) are given by Figures 29, 30 and 31.

9. VCO free running frequency adjustment

VCO free running frequency adjustment is performed at room temperature.

If TN1 is set High, VCO is free running. Wait for 5 to 10 minutes after turning power supply ON (warm up time).

While monitoring PCK (Pin 19) output, adjust the signal frequency (within ±1%) with the variable resistor connected between FV and V_{EE}.

Figure 24 : VCO Temperature Compensation and Free Running Frequency Adjustment

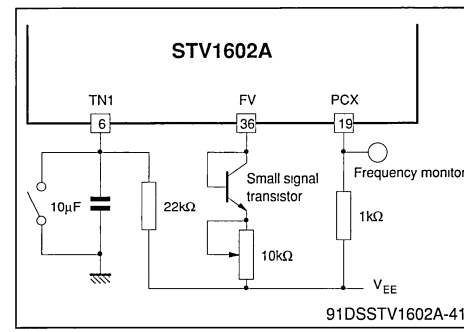
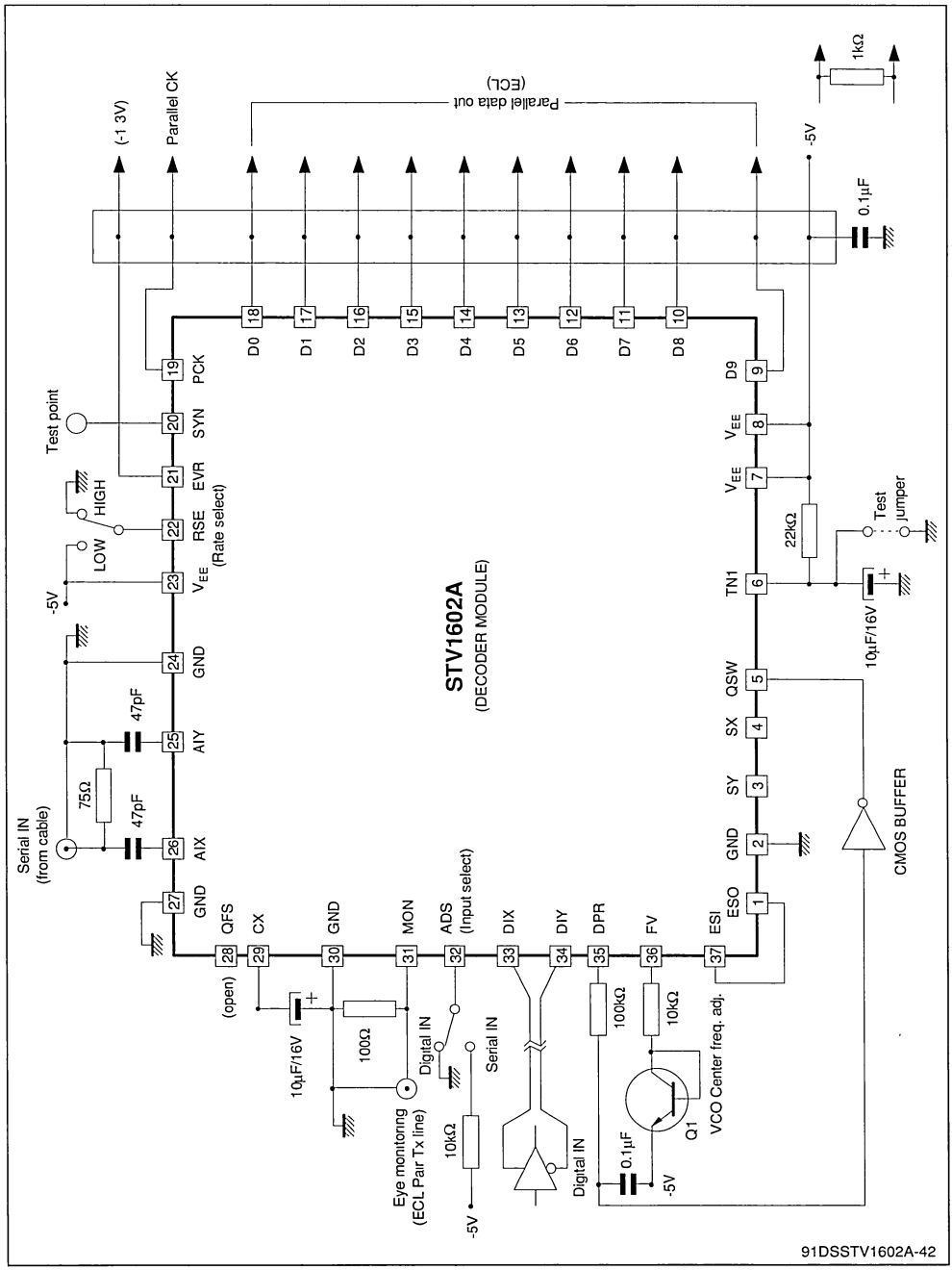
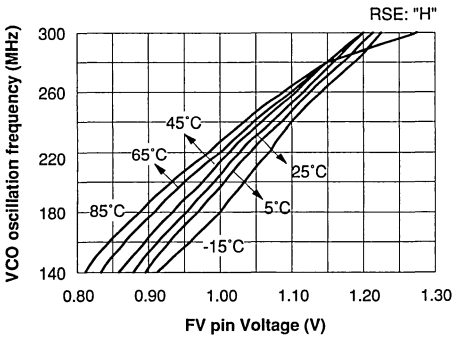


Figure 25 : Application Circuit Example



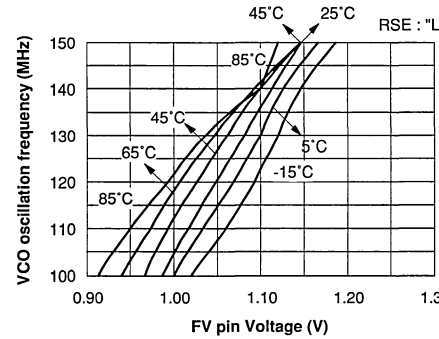
REPRESENTATIVE CHARACTERISTICS EXAMPLE

Figure 26 : VCO Oscillation Frequency versus FV Pin Voltage



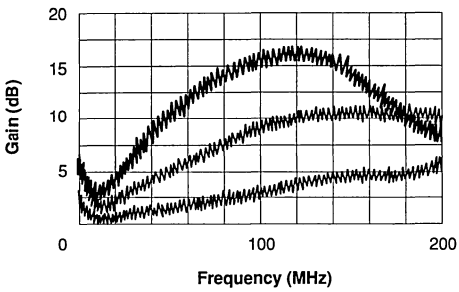
91DSSTV1602A-43

Figure 27 : VCO Oscillation Frequency versus FV Pin Voltage



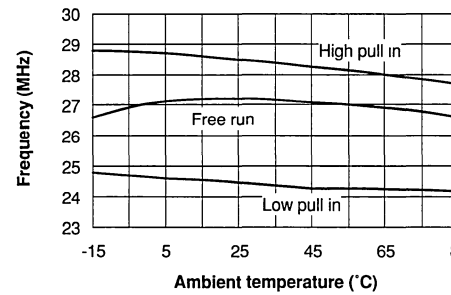
91DSSTV1602A-44

Figure 28 : An example of equalizer characteristics using 5C - 2V coaxial cable with respect to the gain for 0.5meter



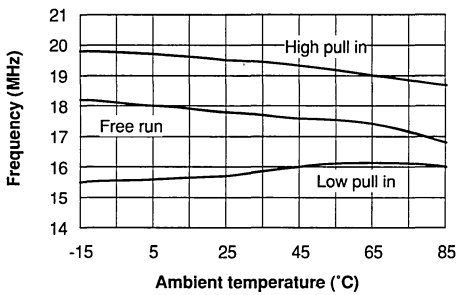
91DSSTV1602A-45

Figure 29 : Pull-in Range and Free Run Frequency (270Mb/s)



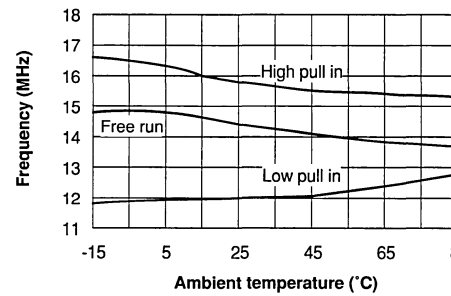
91DSSTV1602A-46

Figure 30 : Pull-in Range and Free Run Frequency (177Mb/s)



91DSSTV1602A-47

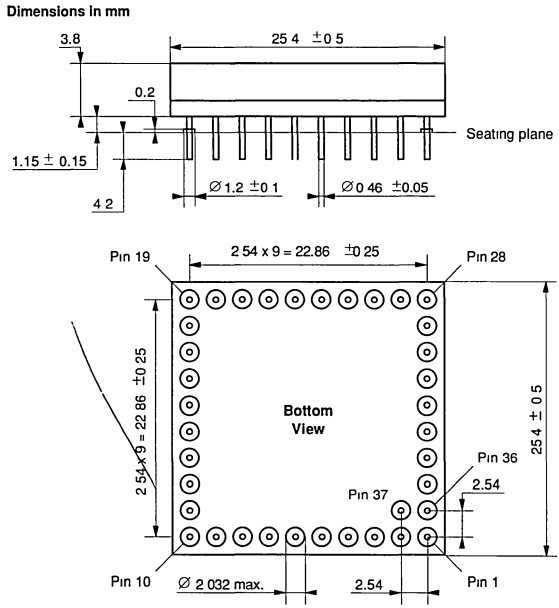
Figure 31 : Pull-in Range and Free Run Frequency (143Mb/s)



91DSSTV1602A-48

PACKAGE MECHANICAL DATA

37 PINS - CERAMIC PGA



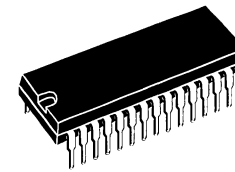
SGS-THOMSON MICROELECTRONICS

STV2100

PAL LUMA-CHROMA & DEFLECTION PROCESSOR

ADVANCE DATA

- ONE RGB AND FB INPUT
- DC-CONTROLLED BRIGHTNESS, CONTRAST AND SATURATION
- CERAMIC 500kHz VCO FOR LINE DEFLECTION
- PHASE-LOCKED REFERENCE OSCILLATOR USING A STANDARD 4.43MHz QUARTZ
- NO LINE AND FRAME OSCILLATOR ADJUSTMENTS REQUIRED
- OSD CAPABILITY ON OUTPUTS
- VIDEO IDENTIFICATION GENERATOR
- FEW EXTERNAL COMPONENTS



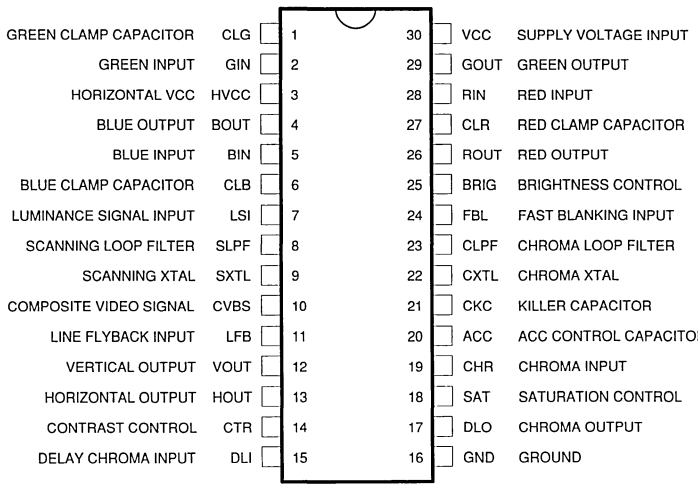
SKRINK DIP30
(plastic package)

ORDER CODE : STV2100

DESCRIPTION

The STV2100 is a PAL chroma decoder, video and H/V deflection processor for CTV.
Used with the TDA8213, this IC permits a complete low cost solution with external output stages.

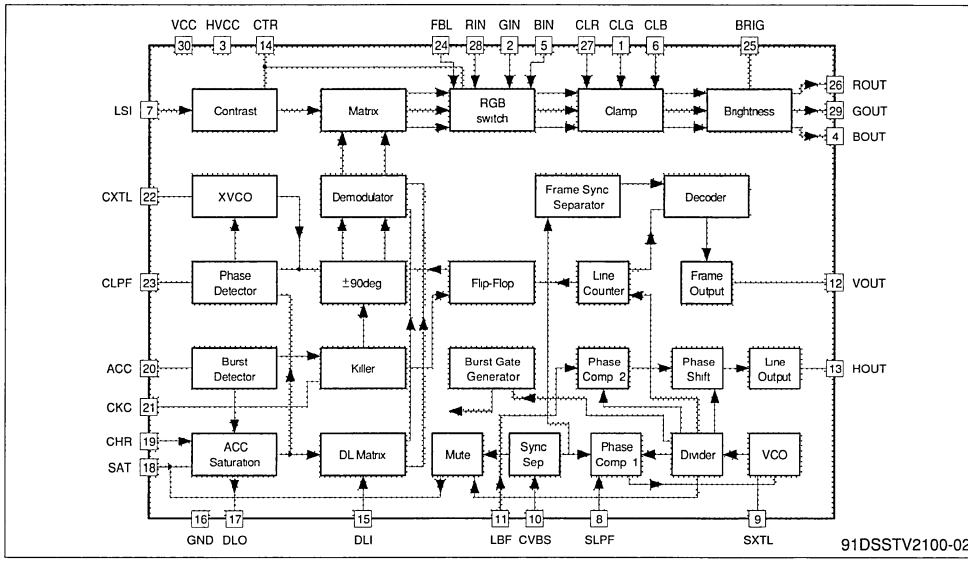
PIN CONNECTIONS



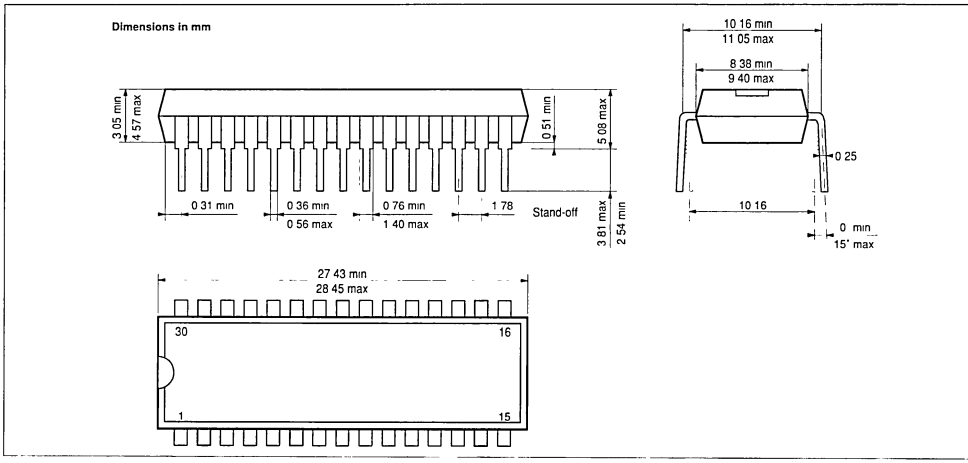
91DSSTV2100-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

BLOCK DIAGRAM



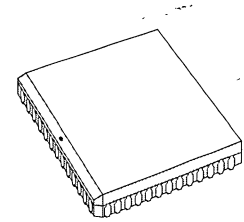
PACKAGE MECHANICAL DATA : 30 PINS - PLASTIC SHRINK



DIGITAL VIDEO FILTERING AND DEMATRIXING

PRELIMINARY DATA

- DIGITAL RESTITUTION OF R,G,B PRIMARY COMPONENTS FROM DIGITAL INPUTS Y (LUMINANCE) AND CR, CB (CHROMINANCE) THROUGH FILTERING AND DEMATRIXING.
- TWO 8-BIT INPUT CHANNELS:
  - Y signal at 13.5 Msamples/sec
  - multiplexed CR, CB signal at 13.5 Msamples/sec
- OVERSAMPLING DIGITAL FILTERING TECHNIQUE WITH A FIXED RESPONSE CURVE FOR Y, AND FOUR SELECTABLE RESPONSE CURVES FOR CR, CB.
- DIGITAL DEMATRIXING OPERATOR
- THREE-STATE BUFFERS ON R,G,B OUPUTS
- CMOS TECHNOLOGY
- SINGLE 5 VOLTS POWER SUPPLY



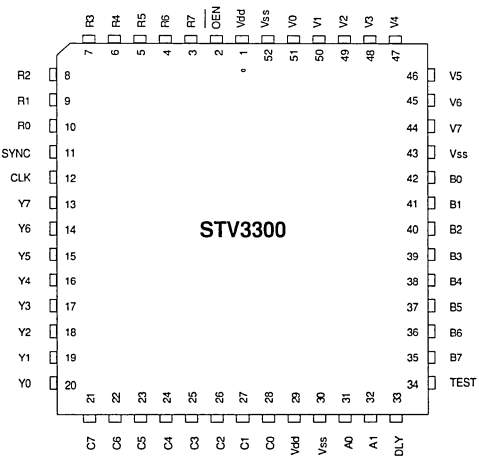
PACKAGE
PLCC52

DESCRIPTION

This circuit associated with a triple Digital-to-Analog converter is dedicated to the restitution of primary components R,G,B of a digital video processing system according to 601 CCIR recommandations.

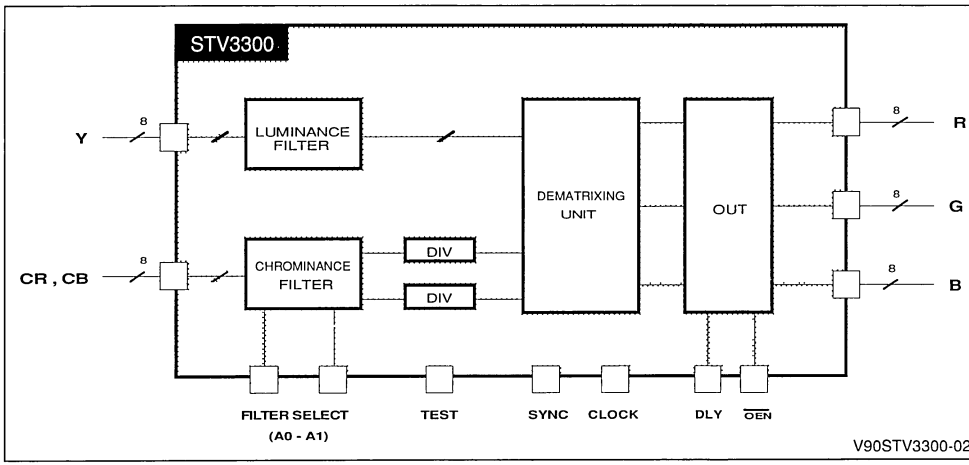
The STV3300 is also suitable for other TV standards and for still picture applications. Due to the implementation of oversampling technique, complex analog filters are eliminated and the restitution module is greatly simplified.

PIN CONNECTIONS



V90STV3300-01

BLOCK DIAGRAM



PIN DESCRIPTION

Pin number	Symbol	Description
1 - 29	V_{DD}	Power supply
2	$\overline{OEN}$	Output Enable: This TTL input controls the output buffers; $\overline{OEN}$ = 1, ouput are in three state: $\overline{OEN}$ = 0, ouputs are valid
3 : 10	R7:R0	8-bit TTL outputs for R channel. R7 is the MSB, R0 is the LSB
11	SYNC	This TTL input synchronizes the multiplexing of the CR,CB signals on the C inputs. SYNC must be low when CB is active, every four CLK periods.
12	CLK	Clock TTL input. Data inputs on Y and C channels are sampled on the falling edge of CLK signal
13 : 20	Y7 : Y0	8-bit inputs for Y channel. Y7 is the MSB, Y0 is the LSB
21 : 28	C7 : C0	8-bit inputs for C channel. C7 is the MSB, C0 is the LSB
30 - 43 - 52	V_{SS}	Ground
31 - 32	A0-A1	TTL inputs for chrominance filter response curve selection
33	DLY	This TTL input activates a delay of one clock period on the output path: active at level 1
34	TEST	This signal must be connected to 0
35 : 42	B0 : B7	8-bit TTL outputs for B channel. B7 is the MSB, B0 is the LSB
44 : 51	G0 : G7	8-bit TTL outputs for G channel. G7 is the MSB, G0 is the LSB

DEVICE DESCRIPTION

The STV3300 is basicaly constituted of two different parts; a filtering stage and a dematrixing stage.

Luminance filter

The luminance filter oversamples the Y input signal by a factor of 2, (filter output frequency is 27 Msamples/sec.), and reduces duplicated spectrum introduced by digitization. It is a 19th order finite response filter which includes the compensation of the Sinx/x attenuation of the digital to analog conversion. Figure 1 shows the luminance filter response curve.

Chrominance filter

The chrominance filter oversamples CR, CB input signals by a factor of 4,
(filter output frequency is 27 Msamples/sec). Two filters are implemented in series, each of them oversamples by a factor of 2. The first filter stage allows four different filter selections via two dedicated pins.

Those filters provide different cutoff frequencies (from 1 MHz to 1.8 MHz). Figure 2 shows the chrominance filter response curves and the following table the mode selection on the two external pins, A0 and A1.

A0	A1	Filter selected
0	0	1
0	1	2
1	0	3
1	1	4

Dematrixing unit

The dematrixing unit operates at 27 Msamples/sec using the following equations according to the 601 CCIR recommandations:

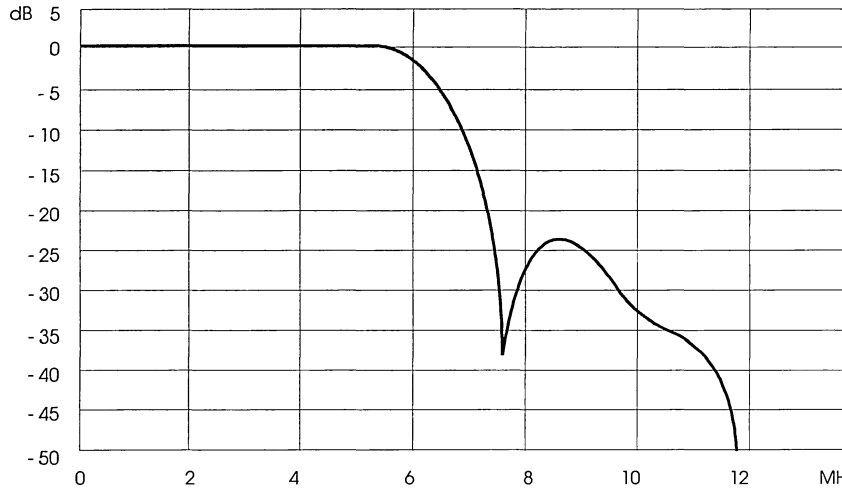
$R = Y + 1.370 \cdot (CR-0.5)$
$G = Y - 0.698 \cdot (CR-0.5) - 0.336 \cdot (CB-05)$
$B = Y + 1.730 \cdot (CB-0.5)$

In addition to the filtering and dematrixing functions two other features are provided :
- An additionnal 27 MHz period can be inserted in the ouput path in order to reproduce the quincunx acquisation principle. This consists in delaying a frame of one 27 MHz period. The external signal DLY controls this operation.
- Output three-state buffers are implemented to provide multiplexing with external signal without external switches. The $\overline{OEN}$ signal controls this function.

SUMMARY OF CONTROL SIGNALS

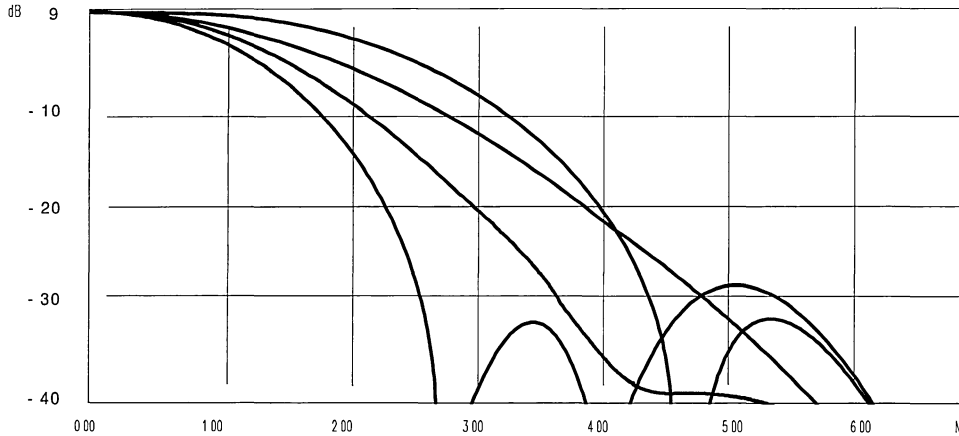
Symbol	Function		Description
A0-A1	Chrominance filter selection	A0-A1=0,0	filter # 1: cutoff frequency = 1.1 MHz
		A0-A1=0,1	filter # 2: cutoff frequency = 1.3 MHz
		A0-A1=1,0	filter # 3: cutoff frequency = 1.5 MHz
		A0-A1=1,1	filter # 4: cutoff frequency = 1.8 MHz
DLY	Frame delay selection	0	Inactive
		1	The output signal is delayed of one clock period versus the input signal
$\overline{OEN}$	Output enable	1	Output buffers are in three-state
		0	Output buffers are active

Figure 1 : Luminance response curve (f_{CLK} = 27MHz)



V90STV3300-03

Figure 2 : Chrominance response curves (f_{CLK} = 27MHz)



V90STV3300-04

ELECTRICAL CHARACTERISTICS

Parameter	Value
Supply Voltage	6V
Voltage on any pin relative to V_{SS}	-0.3V to V_{DD} + 0.3 V
Operating Temperature Range	0 to + 70°C
Storage Temperature Range	-65 °Cto + 150°C

DC ELECTRICAL CHARACTERISTICSS

V_{SS} = 0V, V_{DD} = +5V +/- 10 %, Temperature = +70°C

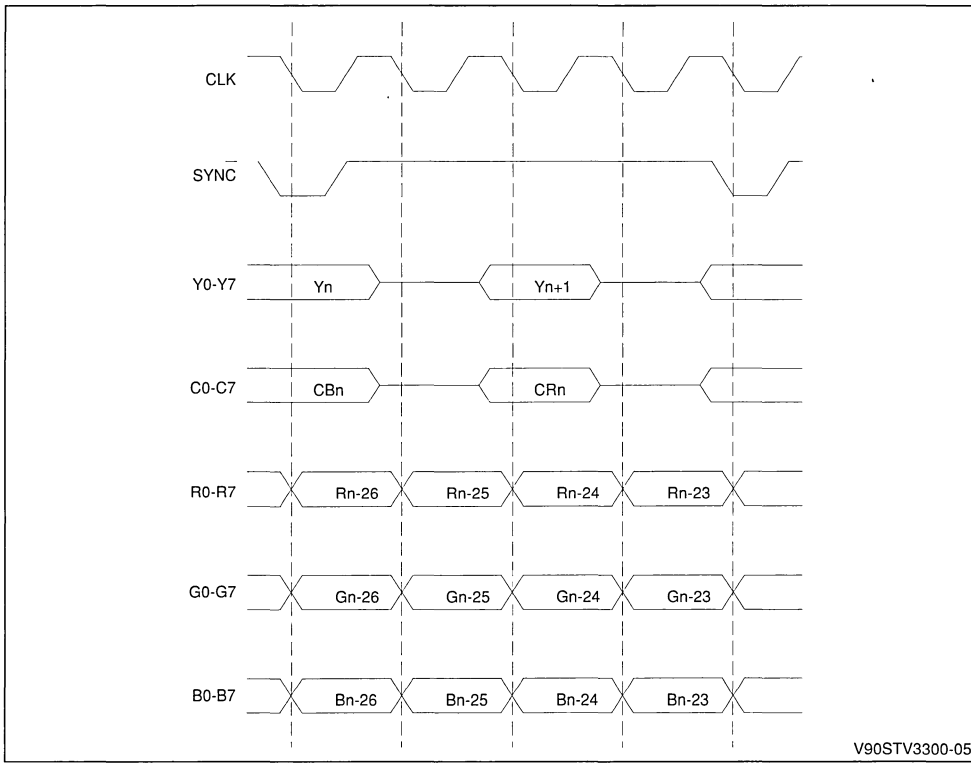
Parameter		Min	Typ	Max	Unit
Supply Voltage		4.5	5	5.5	V
Supply Current (C_{LOAD} = 50pF)			45	100	mA
Power Dissipation (@27 MHz)			300	500	mW
Input Voltage	High level	2			V
	Low level			0.8	V
Output Current	Source(V_{OUT} = 0V)	45			mA
	Sink(V_{OUT} = 5V)	45			mA
Output Voltage	Low level(I_{LOAD} = 6.4mA)			0.4	V
	High level(I_{LOAD} = -400µA)	2.7			V
Input Capacitance		6			pF

AC ELECTRICAL CHARACTERISTICS

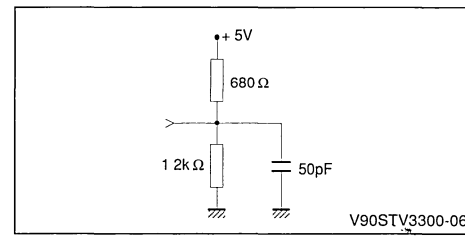
V_{SS} = 0V, V_{DD} = +5V ± 10%, Temperature = +70°C, C_{LOAD} = 50pF

Symbol	Parameter	Min	Typ	Max	Unit
tpf	Output Propagation Delay from CLK Falling Edge		12	18	ns
tpr			12	18	ns
tr	Ouput Rise Time from 0.4 to 4.5V		6.5	10	ns
tf	Output Fall Time from 4.5 to 0.5V		5	10	ns
thzh	Output Enable Time from $\overline{OEN}$		7	12	ns
thzl			7	12	ns
thhz	Output Disable Time from $\overline{OEN}$		6	12	ns
tlhz			6	12	ns
tsuzy	SYNC Setup Time	2	2		ns
thdsy	SYNC Hold Time	5			ns
tclk	Clock Cycle Time	24	37		ns
tch	Clock High Pulse Width	12			ns
tcl	Clock Low Pulse Width	12			ns
tsuda	Input Data Setup Time	0			ns
thdda	Input Data Hold Time	7.5			ns

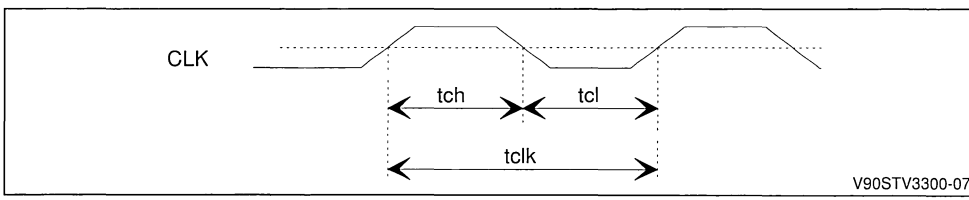
TIMING WAVEFORMS



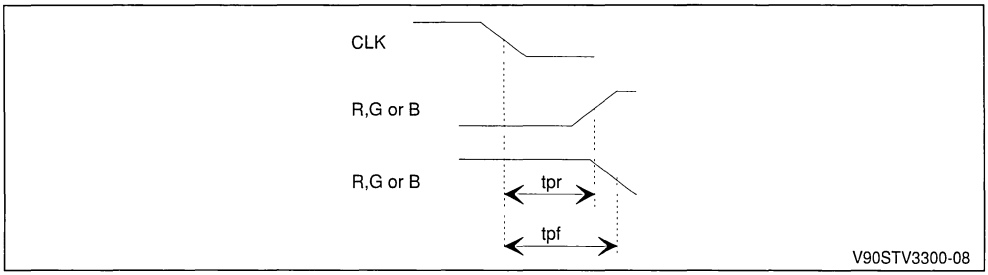
Note : AC load on each output.

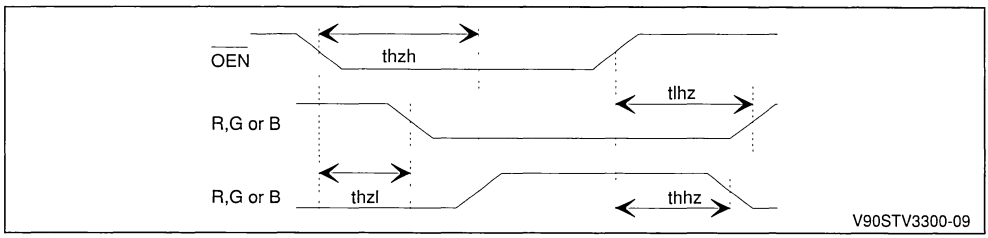


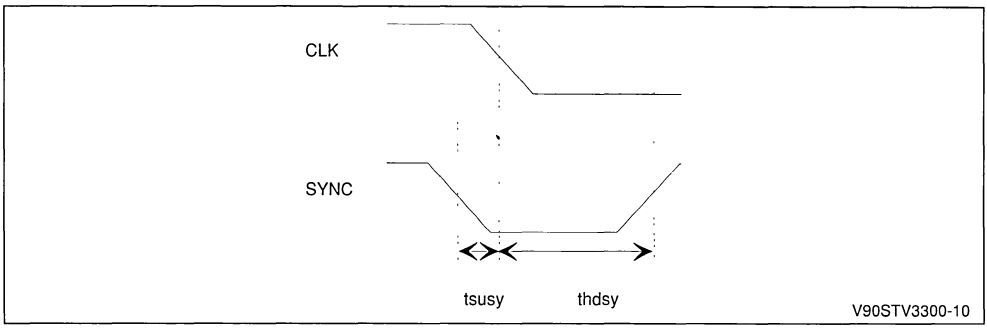
TIMING DIAGRAMS

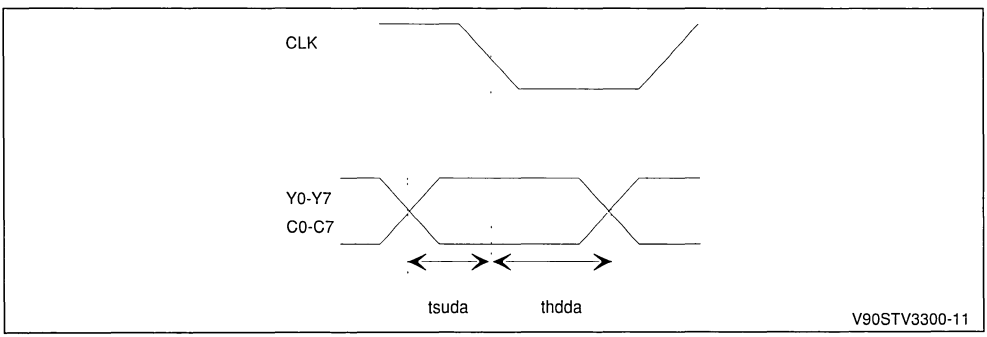


TIMING DIAGRAMS (continued)



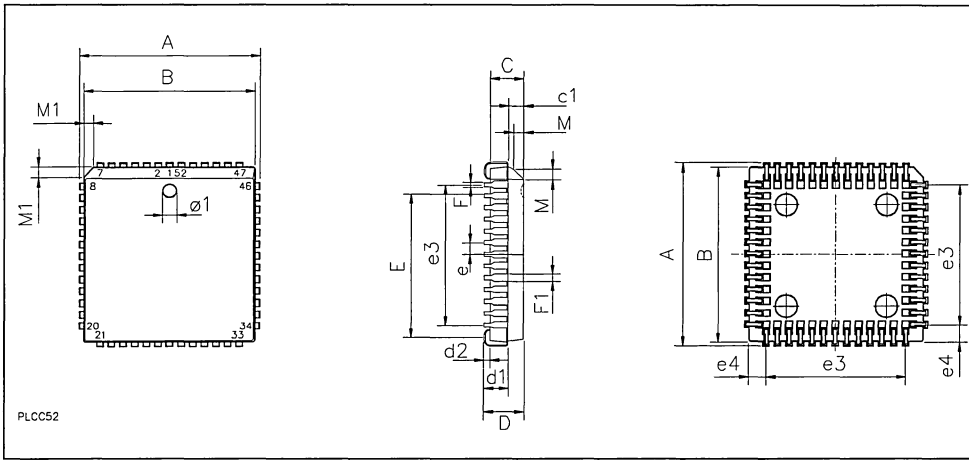






PACKAGE MECHANICAL DATA

52 PINS - PLASTIC PLCC



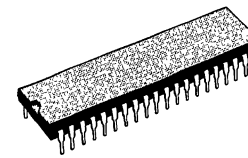
REF.	DIMENSIONS (mm)			REF.	DIMENSIONS (mm)		
	Min.	TYp.	Max.		Min.	Typ.	Max.
A	19.94		20.19	e		1.27	
B	19.050		19.202	e3		15.24	
C				e4			
c1				F	0.331		0.533
D	4.20		5.08	F1	0.661		0.812
d1				M	1.07		1.42
d2				M1	1.067		1.219
E	17.53		18.54				

SGS-THOMSON MICROELECTRONICS

STV5343

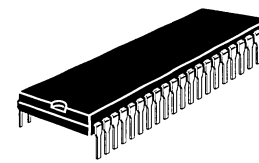
COMPUTER-CONTROLLED TELETEXT DECODER WITH UP TO 64 KBYTES RAM ADDRESSING CAPABILITY

- FULLY COMPATIBLE WITH SDA5243 TELETEXT CONTROLLER
- UP TO 32K x 8 BIT STATIC / PSEUDO-STATIC RAM OR 2 x (64K x 4) DRAM DIRECT INTERFACE
- 60Hz RECOGNITION AND INSERTION WITHOUT ADDITIONAL HARDWARE
- MASTER OR SLAVE MODE FOR HORIZONTAL AND VERTICAL SYNCHRONIZATION
- VIDEO SIGNAL QUALITY STATUS BIT
- PROGRAMMABLE RAM CONTROL SIGNAL ($\overline{CE}$, $\overline{WE}$)
- FLEXIBLE CAPABILITIES FOR MANAGEMENT AND REFRESH OF ACQUISITION AND DISPLAY MEMORY
- ON-CHIP MASK PROGRAMMABLE ROM CHARACTER GENERATOR
- AUTOMATIC SELECTION OF UP TO SEVEN NATIONAL LANGUAGES
- MICROPROCESSOR CONTROL VIA AN I^2C BUS
- SINGLE + 5V SUPPLY VOLTAGE



DIP40
(Plastic Package)

ORDER CODE : STV5343



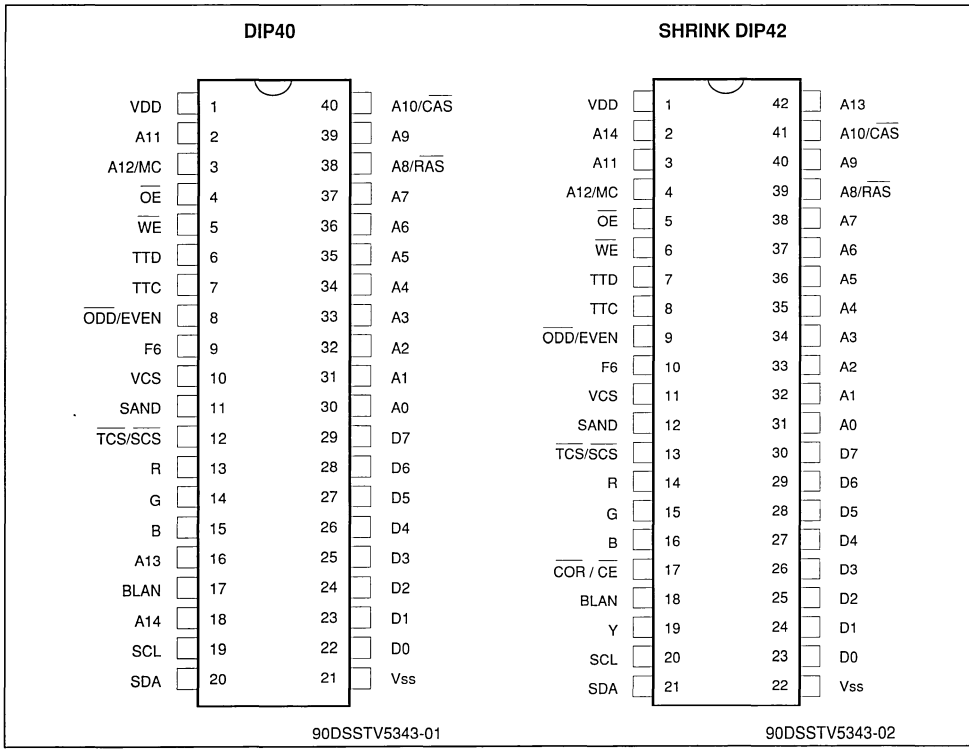
SHRINK DIP42
(Plastic Package)

ORDER CODE : STV5343S

DESCRIPTION

The STV5343 integrated circuit is a computer-controlled teletext decoder with high RAM addressing capability (up to 64Kbytes) upward software compatible with the SDA5243 device.
It is designed to operate in conjunction with the SAA5231 integrated circuit which extracts the teletext information embedded in a composite video signal.
A complete system also comprises a microprocessor controlling the STV5343 via a 2-wire serial bus. An on-chip ROM memory contains the character sets. The STV5343 performs automatic selection of one of up to seven natural languages making the system suitable for the display of text in English, German, Swedish, French, Italian and Spanish. Data bytes may be decoded in either 7-Bit plus parity or in full 8-Bit formats. The chip set also supports facilities for reception and display of higher-level protocol data.

PIN CONNECTIONS



PIN DESCRIPTION

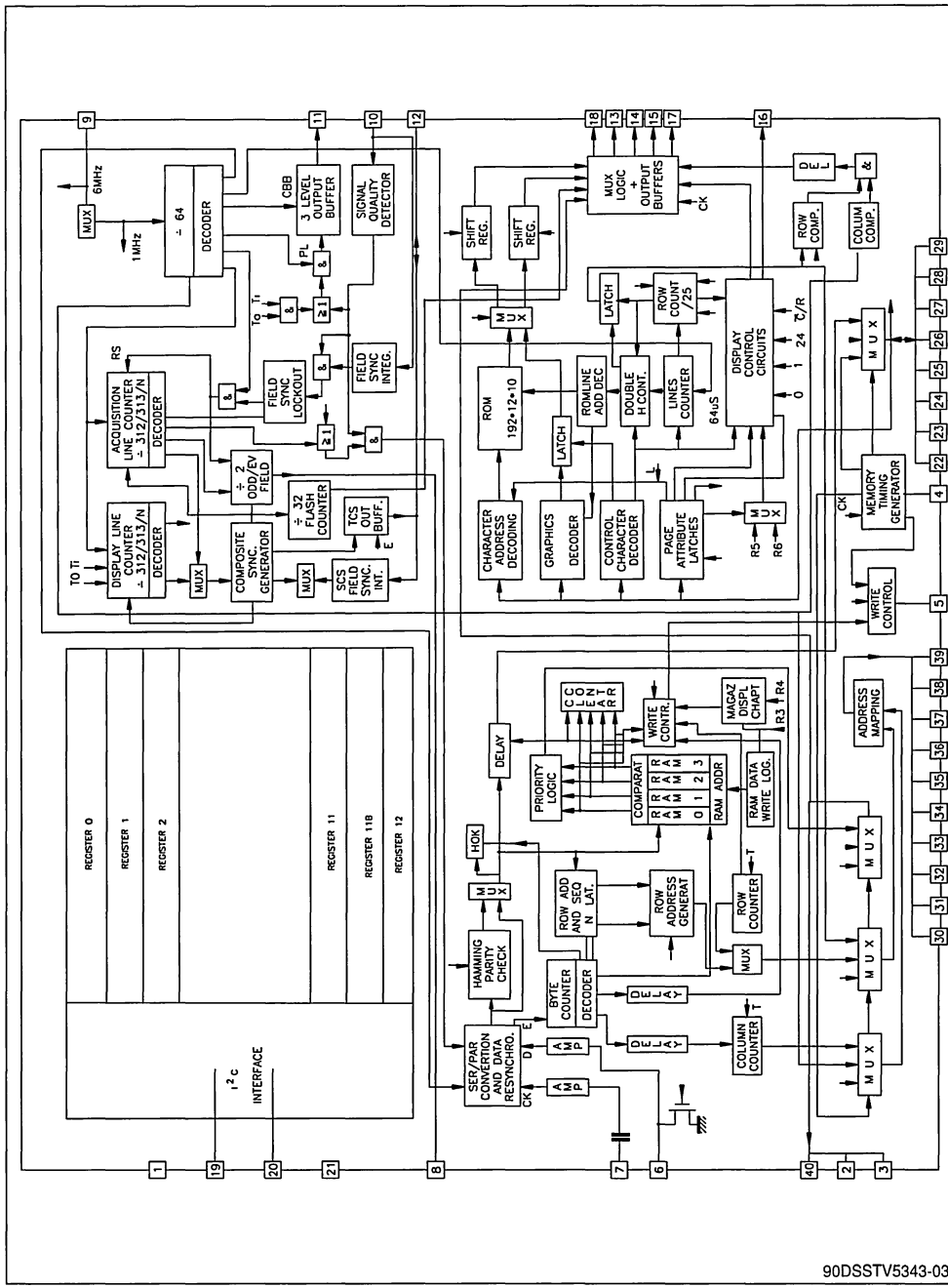
Symbol	Function	Description
V_{DD}	+ 5V	Positive supply voltage.
A10, A11, A12	Chapter address	Address selection outputs for 1 of 8 chapters each of 1 kBytes for SRAM / PSRAM.
A13, A14	Group address	Address selection outputs for 1 of 4 groups each of 8 chapters for SRAM / PSRAM.
$\overline{OE}$	Output enable	Active-low RAM output enable control signal.
$\overline{WE}$	Write enable	Active-low RAM write enable control signal. It supports write-cycles interleaved with read-cycles.
TTD	Teletext data input	An A.C. coupled teletext data input supplied by the SAA5231 chip is latched to V_{SS} between 4 and 8µs after each TV line.
TTC	Teletext clock input	A 6.9375MHz clock signal, supplied by the SAA5231 chip, is internally A.C. coupled, clamped and buffered.
$\overline{ODD}$ / EVEN	Interlaced mode state output	High for even numbered and low for odd-numbered frames. The value is valid 2µs before the end of lines 311 and 624.
F6	Character display clock signal	The 6MHz clock signal, supplied by the SAA5231 chip is internally A.C. coupled, clamped and buffered.

PIN DESCRIPTION (continued)

Symbol	Function	Description
VCS	Video composite synchronization input signal	Active high VCS input.
SAND	Sandcastle	Three level output pulse to the SAA5231 device. Phase lock, blanking signal, and color burst components are contained in this signal.
$\overline{TCS}$ / $\overline{SCS}$	Input / output composite synchronization signal	Scan composite input signal ($\overline{SCS}$) for the display synchronization or Text composite sync. ($\overline{TCS}$) output signal to the SAA5231. Both signals are active low.
RGB	Red, green, blue	Character and background color active-high open-drain outputs.
$\overline{COR}$*	Contrast reduction	Open-drain active-low output supporting optimal display of characters in "mixed mode" operation.
BLAN	Blanking signal output	Open-drain active high output for TV-image blanking in normal and mixed-mode operation.
Y *	Foreground output	Open-drain active-high output with foreground information. Can be used for printer command.
SCL	Serial clock	Microprocessor clock input via serial bus.
SDA	Serial data input / output	Open-drain microprocessor serial data input/output via serial bus.
V_{SS}	0 Volt	Ground.
D0 - D7	Parallel data input / output	Eight tri-state input/output for data read/write from/to external RAM
A0 - A9	Address signals	Ten addresses output pins for accessing to individual Bytes of a 1 kByte chapter stored in an external SRAM / PSRAM and DRAM (only A0 - A7)
MC	Address multiplying control	Address multiplexing control for dynamic RAM - Active low.
$\overline{CE}$	Chip enable	Chip enable for 32K x 8 pseudostatic RAM - Active low.
$\overline{RAS}$, $\overline{CAS}$	Address control	Address control for 64K dynamic RAM - Active low.

* 42SDIP only.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Range	- 0.3 to + 7.5	V
INPUT VOLTAGE RANGE			
V_I	VCS, SDA, SCL, D0 - D7 TTD, F6, TCS / SCS, TTC	- 0.3 to + 7.5 - 0.3 to + 10	V V
OUTPUT VOLTAGE RANGE			
V_O	SAND, A0 - A14, OE, WE, D0 - D7, ODD / EVEN, R, G, B, BLAN, COR / CE, Y TCS / SCS	- 0.3 to + 7.5 - 0.3 to + 10	V V
T_{stg}	Storage Temperature Range	- 20 to + 125	°C
T_{oper}	Operating Ambient Temperature Range	- 20 to + 70	°C

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage (pin 1)	4.5	5	5.5	V
I_{DD}	Supply Current	-	140	200	mA
INPUTS					
	TTD				
C_{EXT}	Ext. Coupling Capacitor	-	-	50	nF
$V_{I(p-p)}$	Input Voltage p-p	2	-	7	V
t_r , t_f	Input Rise / Fall Times	10	-	80	ns
t_{DS}	Input Set-up Time	40	-	-	ns
t_{DH}	Input Hold Time	40	-	-	ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to 10V)	-	-	20	µA
C_I	Input capacitance	-	-	7	pF
	TTC, F6				
V_I	Input Voltage Range	- 0.3	-	+10	V
$V_{I(p-p)}$	AC Input Voltage F6 AC Input Voltage TTC	1 1.5	- -	7 7	V V
$\pm V_P$	Input Peak Rel. 50 % Duty	0.2	-	3.5	V
f_{TTC}	TTC Clock Frequency	4	6.9375	8	MHz
f_{F6}	F6 Clock Frequency	4	6	8	MHz
t_r , t_f	Clock Rise / Fall Times	10	-	80	ns
$I_{I(L)}$	Input Leakage Current (VI = 0 to10 V)	-	-	20	µA
C_I	Input Capacitance	-	-	7	pF

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min	Typ	Max	Unit
INPUTS					
	VCS				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 2	 - -	 0.8 V_{DD}	V
t_r , t_f	Input Rise / Fall Times	-	-	500	ns
$I_{I(L)}$	Input Leakage Current (VI = 5.5V)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
	SCL				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 3	 - -	 1.5 V_{DD}	V
f_{SCL}	SCL Clock Frequency	-	-	100	kHz
t_r , t_f	Input Rise / Fall Times	-	-	2	µs
$I_{I(L)}$	Input Leakage Current (VI = 5.5V)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
INPUT/OUTPUTS					
	$\overline{TCS}$(output), $\overline{SCS}$(input)				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 3	 - -	 1.5 8	V
t_r , t_f	Input Rise / Fall Times	-	-	500	ns
± $I_{I(L)}$	Input Leakage Current (Vi = 0 to10V and output in high impedance state)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
V_{OL} V_{OH}	Output Voltage : ● Low Level I_{OL} = 0.4mA ● High Level -I_{OH} = 0.2mA I_{OH} = 0.1mA	 0 2.4 2.4	 - - -	 0.4 V_{DD} 5 5	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	100	ns
C_I	Load Capacitance	-	-	50	pF
	SDA				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 3	 - -	 1.5 V_{DD}	V
t_r , t_f	Input Rise / Fall Times	-	-	2	µs
$I_{I(L)}$	Input Leakage Current (VI = 5.5V with output off)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min	Typ	Max	Unit
INPUT/OUTPUTS					
	SDA (continued)				
V_{OL}	Low Output Voltage (I_{OL} = 3mA)	0	-	0.5	V
t_f	Output Fall Time between 3.0V and 1.0V	-	-	200	ns
C_I	Load Capacitance	-	-	400	pF
	D0-D7				
V_{IL} V_{IH}	Input Voltage : ● Low Level ● High Level	 0 2	 - -	 0.8 V_{DD}	V
$\pm I_{I(L)}$	Input Leakage Current (VI = 0 to 5.5V and output in high impedance state)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
V_{OL} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 1.6mA) ● High Level (-I_{OH} = 0.2mA)	 0 2.4	 - -	 0.4 V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	50	ns
C_I	Load Capacitance	-	-	120	pF
OUTPUTS					
	A0-A14, $\overline{OE}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{CE}$				
V_{OL} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 1.6mA) ● High Level (-I_{OH} = 0.2mA)	 0 2.4	 - -	 0.4 V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	50	ns
C_L	Load Capacitance	-	-	120	pF
	$\overline{ODD}$/EVEN				
V_{OL} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 0.4mA) ● High Level (-I_{OH} = 0.2mA)	 0 2.4	 - -	 0.4 V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	100	ns
C_L	Load Capacitance	-	-	50	pF
	SAND				
V_{OL} V_{OI} V_{OH}	Output Voltage : ● Low Level (I_{OL} = 0.2mA) ● Middle Level (I_{OL} = ± 10 µA) ● High Level (I_{OH} = 0/- 10µA)	 0 1.1 4	 - - -	 0.25 2.9 V_{DD}	V
t_{r1} t_{r2}	Output Rise Time : ● V_{OL} to V_{OI} from 0.4 to 1.1V ● V_{OI} to V_{OH} from 2.9 to 4.0V	 - -	 - -	 400 200	ns
t_f	Output Fall Time V_{OH} to V_{OI} from 4.0 to 0.4V	-	-	50	ns

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

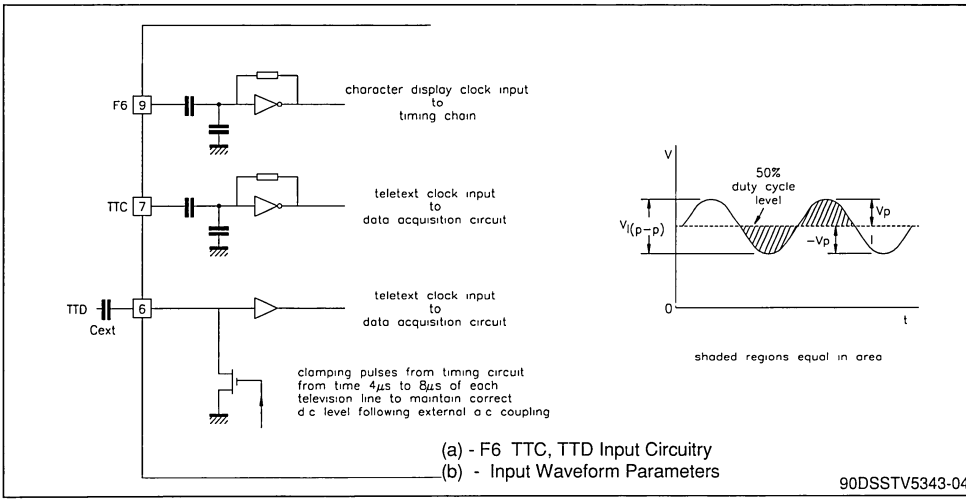
Symbol	Parameter	Min	Typ	Max	Unit
OUTPUTS					
	SAND (continued)				
C_I	Load Capacitance	-	-	30	pF
	R, G, B, $\overline{COR}$, BLAN, Y - (Open drain outputs)				
V_{OL}	Low Level Output Voltage : • I_{OL} = 2mA • I_{OL} = 5mA	 0 0	 - -	 0.4 1	V
V_{PU}	Pull-up Voltage (with R = 1kΩ to 5V)	-	-	5	V
t_f	Output Fall Time from 4.5 to 1.5V (with R = 1kΩ to 5V)	-	-	20	ns
t_{SK}	Skew Delay on Falling Edges (at 3V with R = 1kΩ connected to 5V)	-	-	20	ns
C_L	Load Capacitance	-	-	25	pF
I_{LO}	Output Leakage Current (V_{PU} = 0 to 6V output off)	-	-	20	µA
TIMING					
	SERIAL BUS (referred to V_{IH} = 3V, V_{IL} = 1.5V)				
t_{LOW} t_{HIGH}	Clock : • Low Period • High Period	 4 4	 - -	 - -	µs
t_{SU} , d_{AT} t_{HD} , d_{AT}	Data Set-up Time Data Hold Time	250 170	- -	- -	ns ns
t_{SU} , s_{TO}	Stop Set-up Time from Clock High	4	-	-	µs
t_{BUF}	Start Set-up Time Following a Stop	4	-	-	µs
t_{HD} , s_{TA} t_{SU} , s_{TA}	Start Hold Time Start Set-up Time Following Clock Low to High Transition	4 4	- -	- -	µs µs
	STATIC MEMORY INTERFACE (referred to V_{IL} = 1.5V)				
t_{CY}	Cycle Time	-	500	-	ns
t_{OE}	Adress Change to $\overline{OE}$ Low	60	-	-	ns
t_{ADDR}	Address Active Time	450	500	-	ns
t_{OEW}	$\overline{OE}$ Pulse Duration	320	-	-	ns
t_{ACC}	Access Time from $\overline{OE}$ to Data Valid	-	-	200	ns
t_{DH}	Data Hold Time from $\overline{OE}$ High or Address Change	0	-	-	ns
t_{WE}	Address Change to $\overline{WE}$ Low	40	-	-	ns
t_{WEW}	$\overline{WE}$ Pulse Duration	200	-	-	ns
t_{DS}	Data Set-up Time to $\overline{WE}$ High	100	-	-	ns
t_{DHWE}	Data Hold Time from $\overline{WE}$ High	20	-	-	ns
t_{WR}	Write Recovery Time	25	-	-	ns

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
TIMING (continued)					
	PSEUDOSTATIC RAM MEMORY INTERFACE - Read				
t_{RC}	Read Cycle Time	450	-	-	ns
t_{CE}	$\overline{CE}$ Pulse Width	320	-	-	ns
t_{ASC}	Address Set up Time	60	-	-	ns
t_{AHC}	Address Hold Time	300	-	-	ns
t_{RCS}	$\overline{WE}$ Set up Time	60	-	-	ns
t_{CEA}	Acces Time from $\overline{CE}$	-	-	200	ns
t_{OD}	Data Hold Time	0	-	-	ns
	PSEUDOSTATIC RAM MEMORY INTERFACE - Write				
t_{RC}	Write Cycle Time	450	-	-	ns
t_{CE}	$\overline{CE}$ Pulse Width	320	-	-	ns
t_{ASC}	Address Set up Time	60	-	-	ns
t_{AHC}	Address Hold Time	300	-	-	ns
t_{OSC}	$\overline{OE}$ Set up Time	60	-	-	ns
t_{DSC}	Data Set up Time	0	-	100	ns
t_{DHW}	Data Hold Time to $\overline{WE}$ High	60	-	-	ns
t_{WCH}	$\overline{WE}$ Pulse Width	200	-	-	ns
	DYNAMIC RAM MEMORY INTERFACE - Read				
t_{RC}	Read Cycle Time	450	-	-	ns
t_{RAS}	$\overline{RAS}$ Pulse Width	320	-	-	ns
t_{ASR}	Row Address Set up Time (A0 - A7)	40	-	-	ns
t_{ASC}	Column Address Set up Time (A1 - A7)	40	-	-	ns
t_{RCD}	Delay Time, $\overline{RAS}$ low to $\overline{CS}$ low	-	160	-	ns
t_{CAC}	Acces Time from $\overline{CAS}$	-	-	100	ns
t_{OEW}	$\overline{OE}$ Pulse Width	320	-	-	ns
	DYNAMIC RAM MEMORY INTERFACE - Write				
t_{RC}	Write Cycle Time	450	-	-	ns
t_{RAS}	$\overline{RAS}$ Pulse Width	320	-	-	ns
t_{ASR}	Row Address Set up Time	40	-	-	ns
t_{ASC}	Column Address Set up Time	40	-	-	ns
t_{RCD}	Delay Time, $\overline{RAS}$ low to $\overline{CAS}$ low	-	160	-	ns
t_{WCS}	Write Set up Time	-	160	-	ns
t_{DS}	Data Set up Time	-	160	-	ns

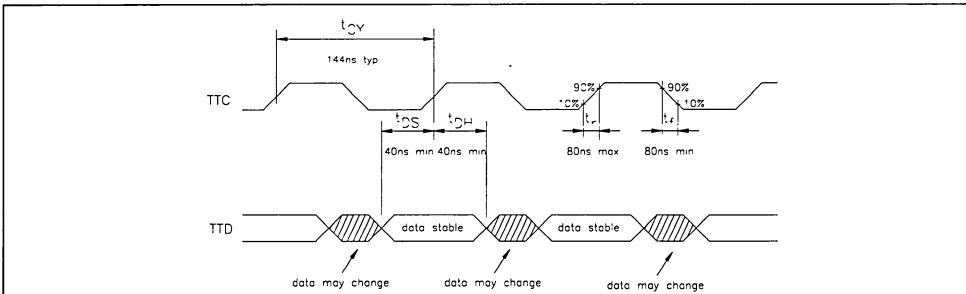
F6, TTC, TTD INPUT INTERNAL CONNECTIONS



(a) - F6 TTC, TTD Input Circuitry
(b) - Input Waveform Parameters

90DSSTV5343-04

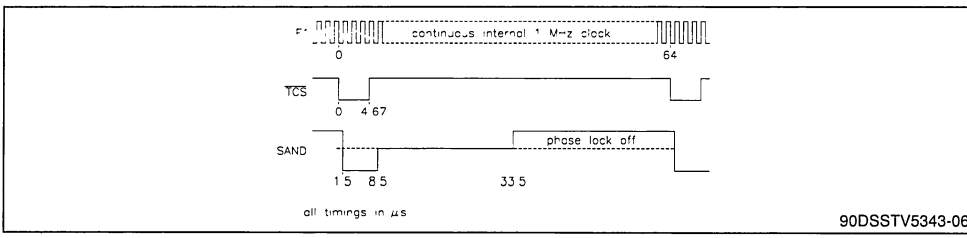
TELETEXT DATA INPUT TIMING



Data Stable : 1 if ≥ 2V , 0 if ≤ 0.8V

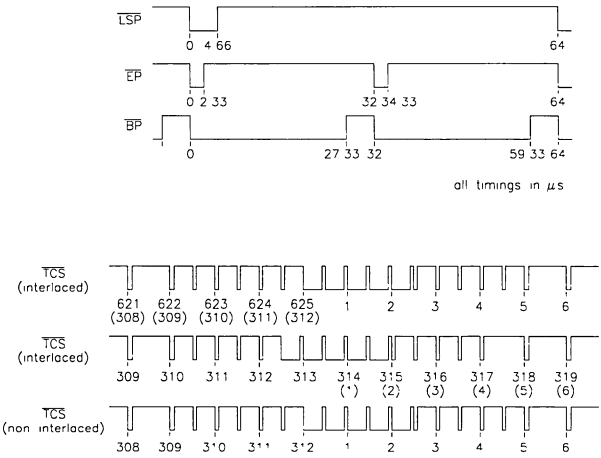
90DSSTV5343-05

SYNCHRONIZATION TIMING



90DSSTV5343-06

COMPOSITE SYNC. WAVEFORMS



90DSSTV5343-07

The number positions indicate the end of lines

The Teletext composite synchronization signal ($\overline{TCS}$), whether interlacing is present or not, comprises three components.

a) The line-synchronization pulses (LSP)

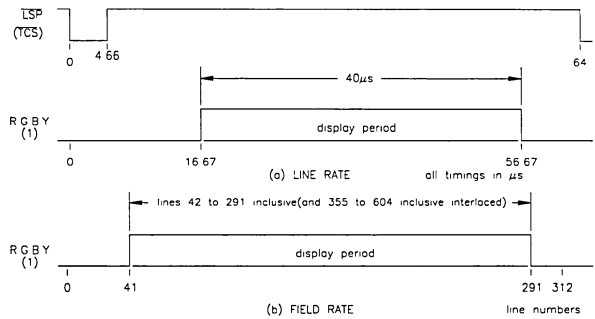
b) the equalisation pulses (EP)

c) the frame-synchronization pulses (BP).

The timing reference is specified by the descending edge of the signal LSP, with a tolerance spread of ± 100 ns.

DISPLAY OUTPUT TIMING

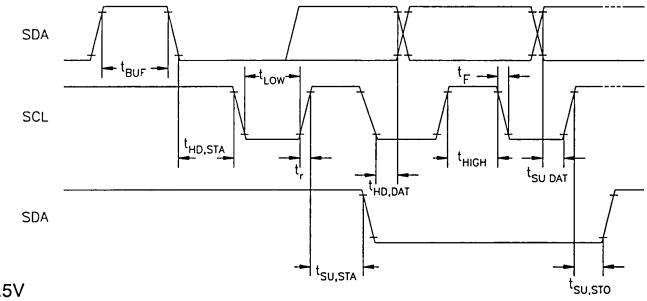
Horizontal direction (line)
Vertical direction (frame)



(1) - Also BLAN in character and box blanking

90DSSTV5343-08

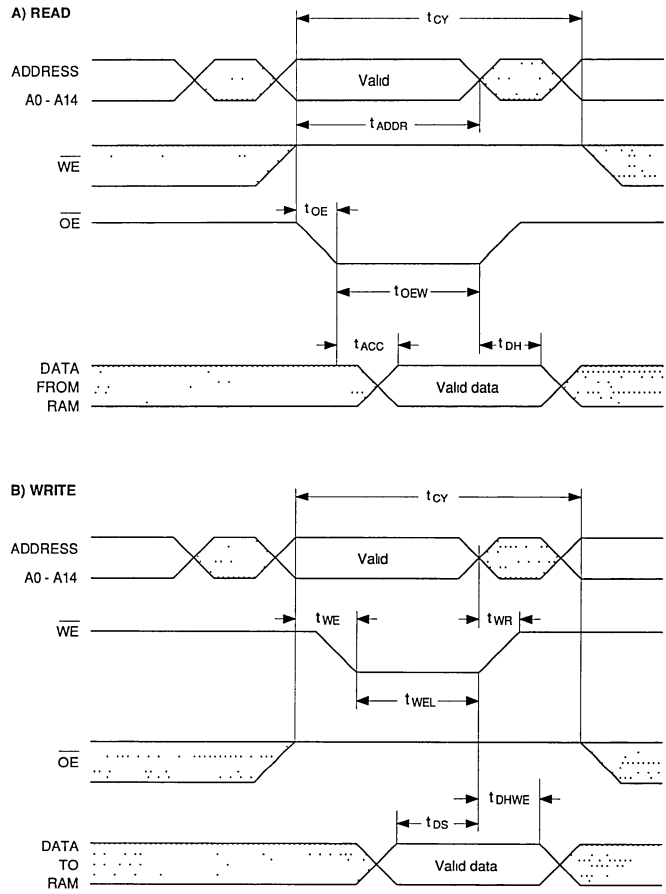
SERIAL BUS TIMING



V_{IH} = 3V , V_{IL} = 1.5V

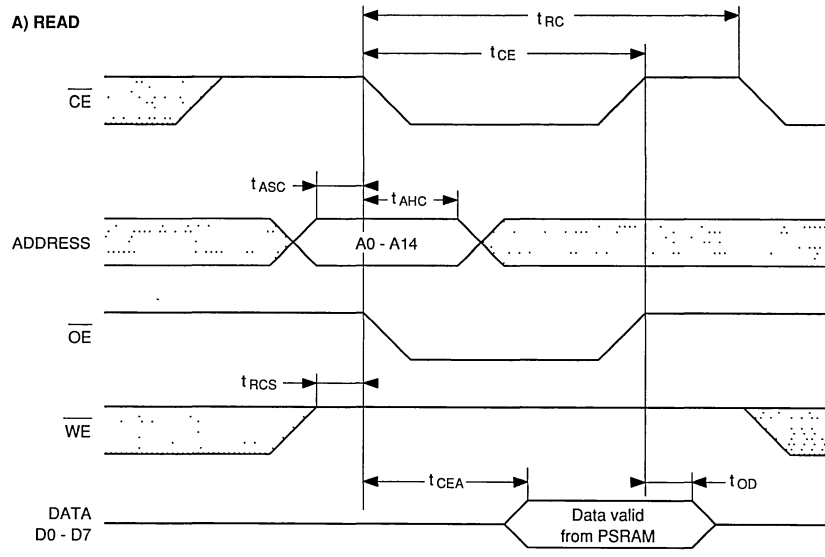
90DSSTV5343-09

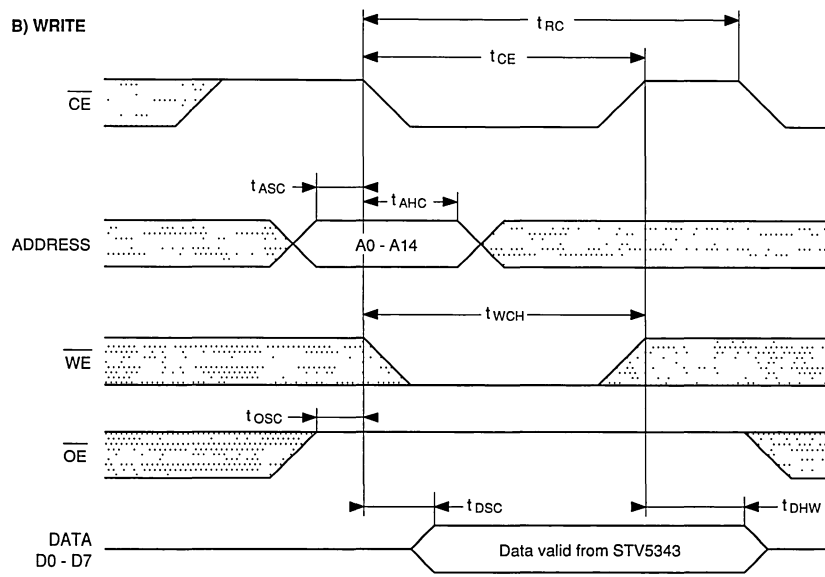
STATIC RAM MEMORY INTERFACE TIMING



91DSSTV5343-10

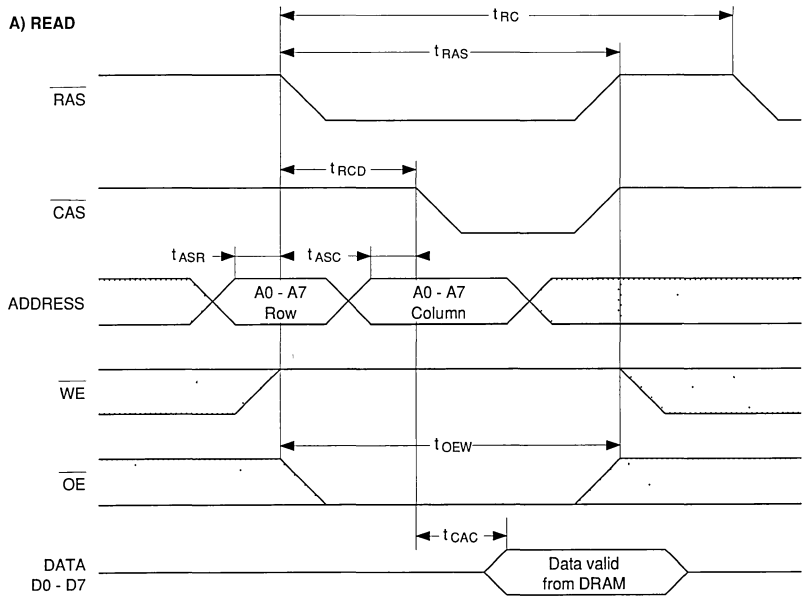
PSEUDO SRAM MEMORY INTERFACE TIMING

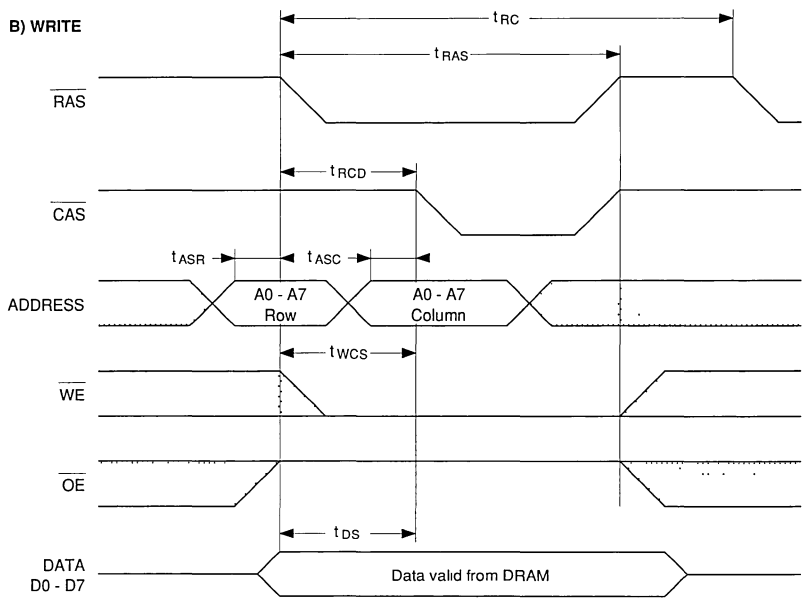




91DSSTV5343-11

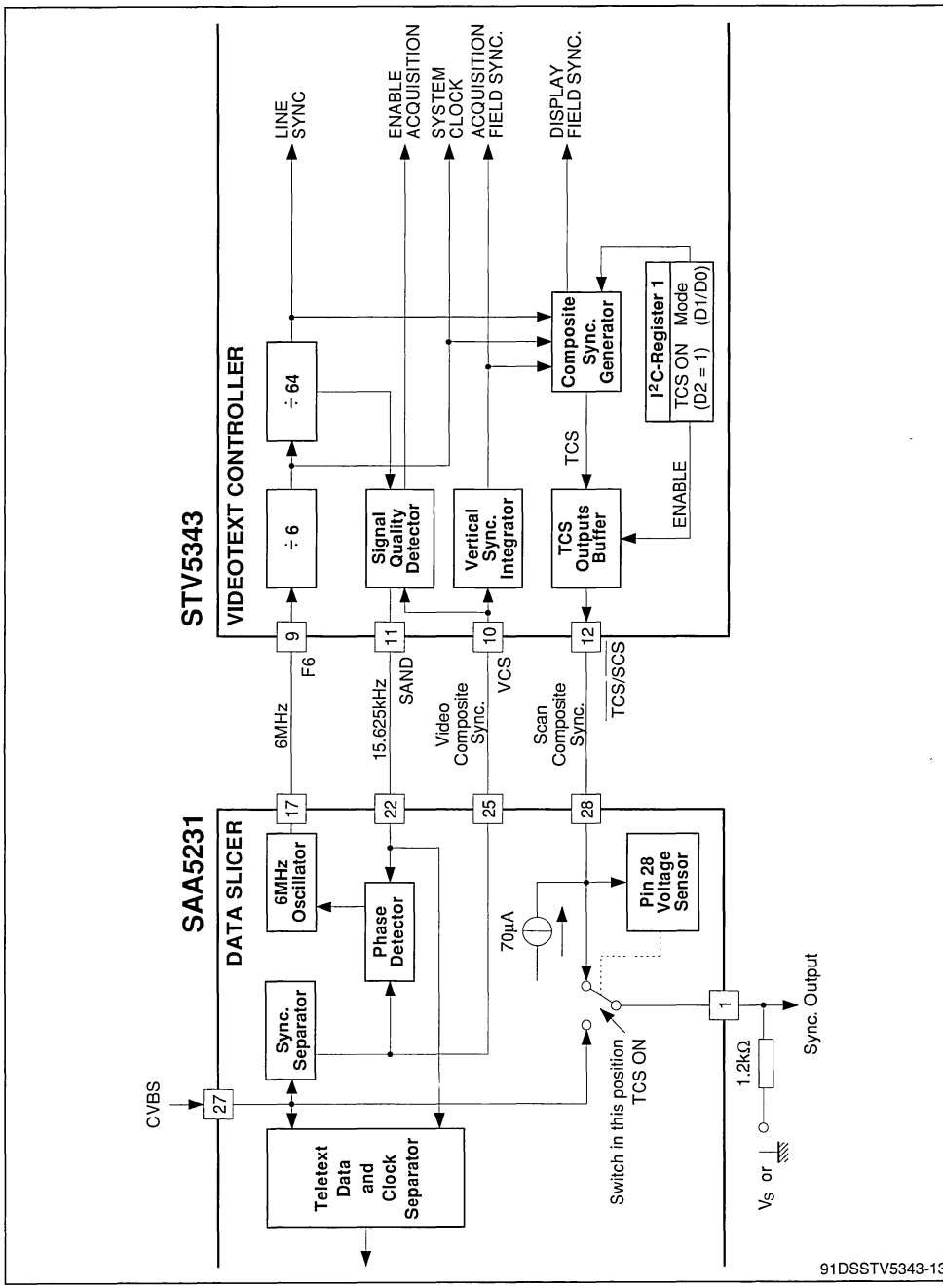
DYNAMIC RAM MEMORY INTERFACE TIMING



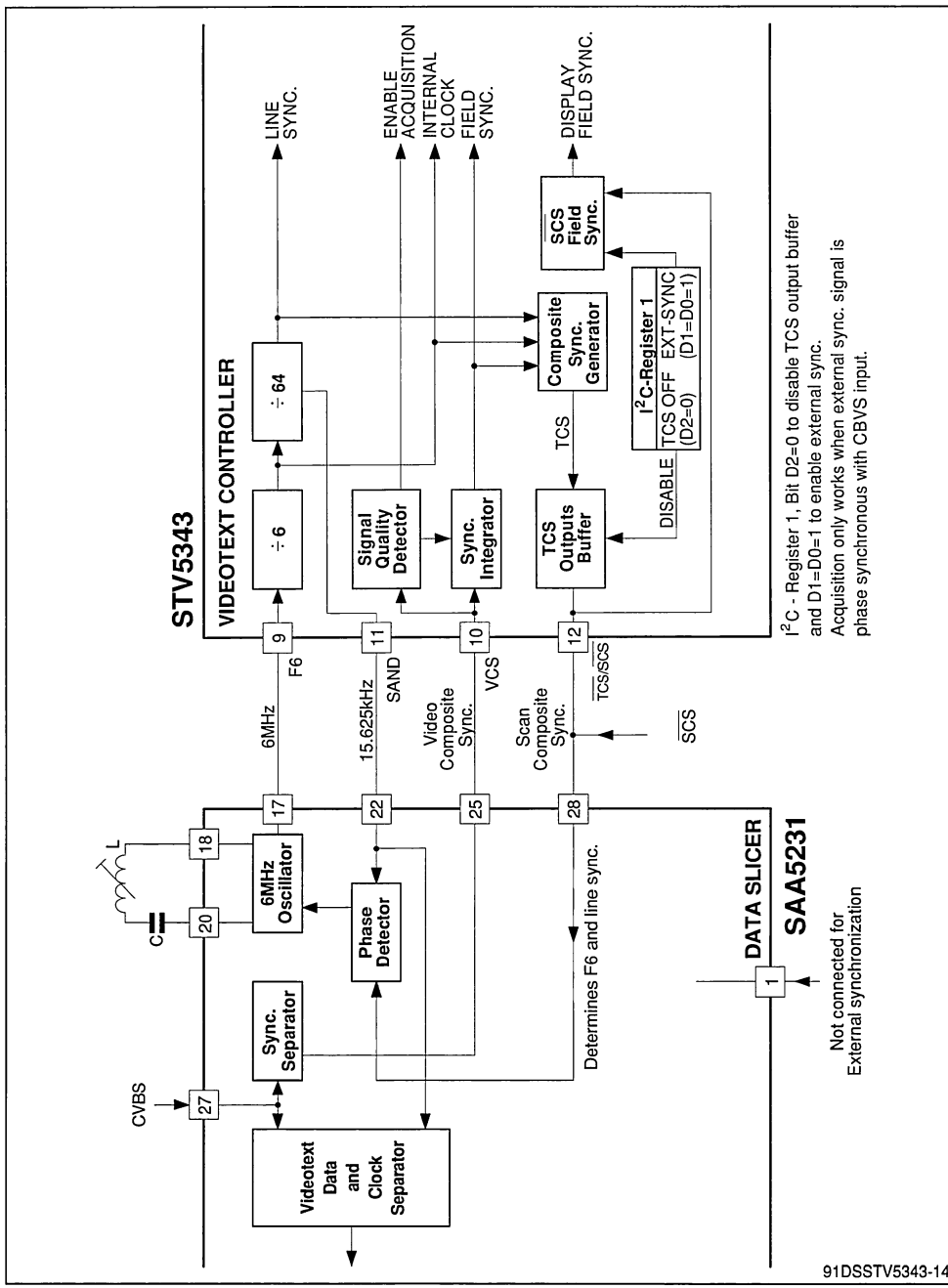


91DSSTV5343-12

MASTER SYNCHRONIZATION MODE



SLAVE SYNCHRONIZATION MODE



MEMORY INTERFACE DIAGRAM WITH STV5343 (40-pin DIP package)

Figure 1a : 32-page Application with SRAM or PSRAM

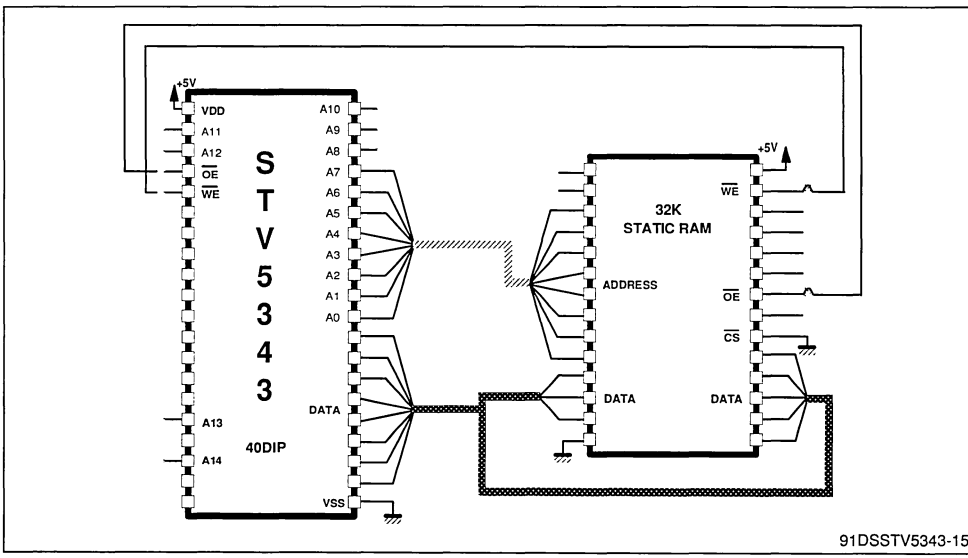
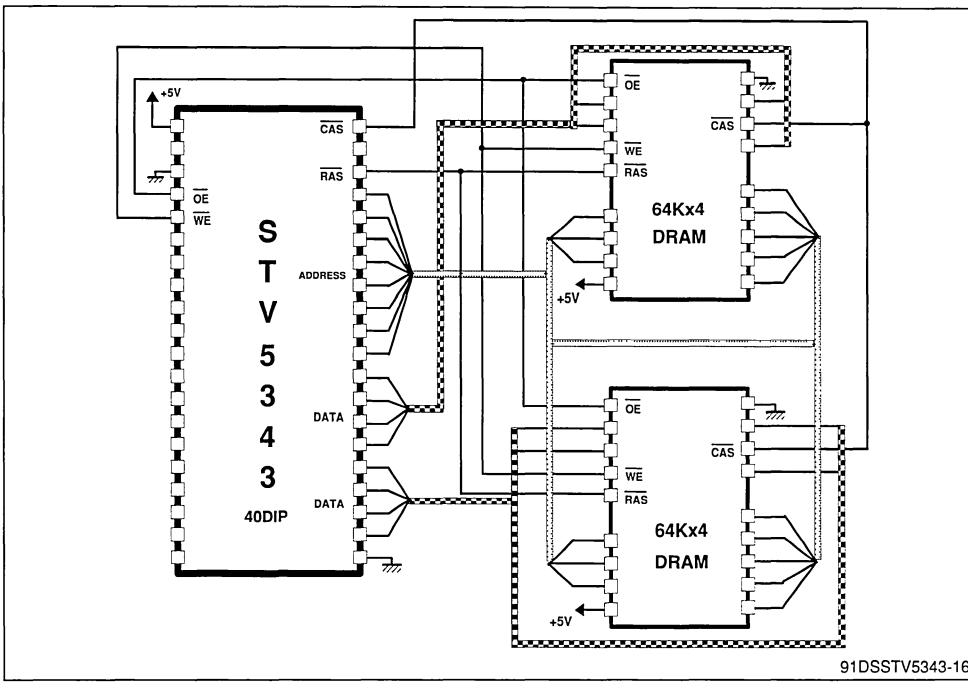


Figure 1b : 64-page Application with DRAM



MEMORY INTERFACE DIAGRAM WITH STV5343 (42-pin SDIP package)

Figure 2a : 32-page Application with SRAM or PSRAM

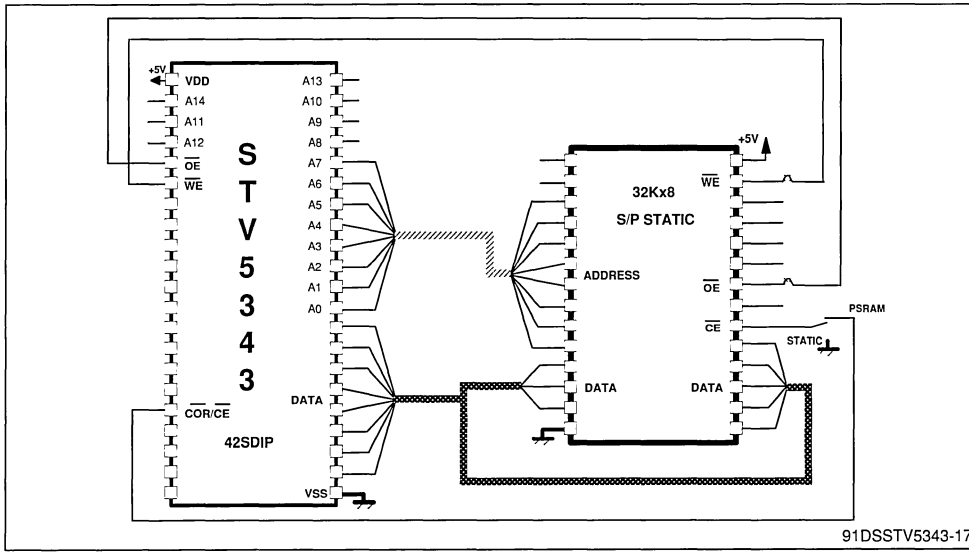
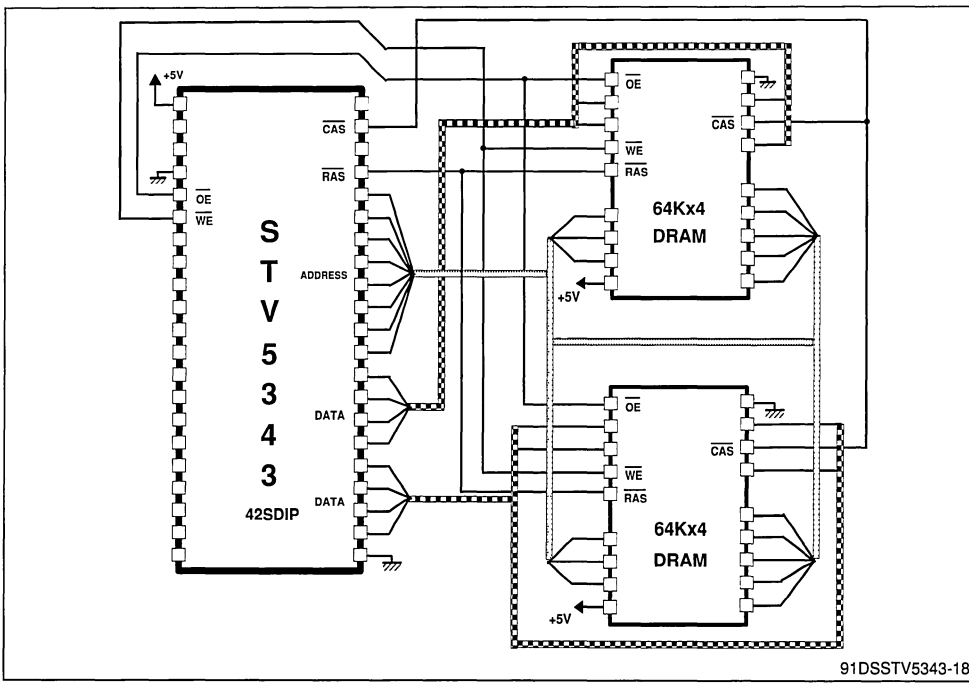
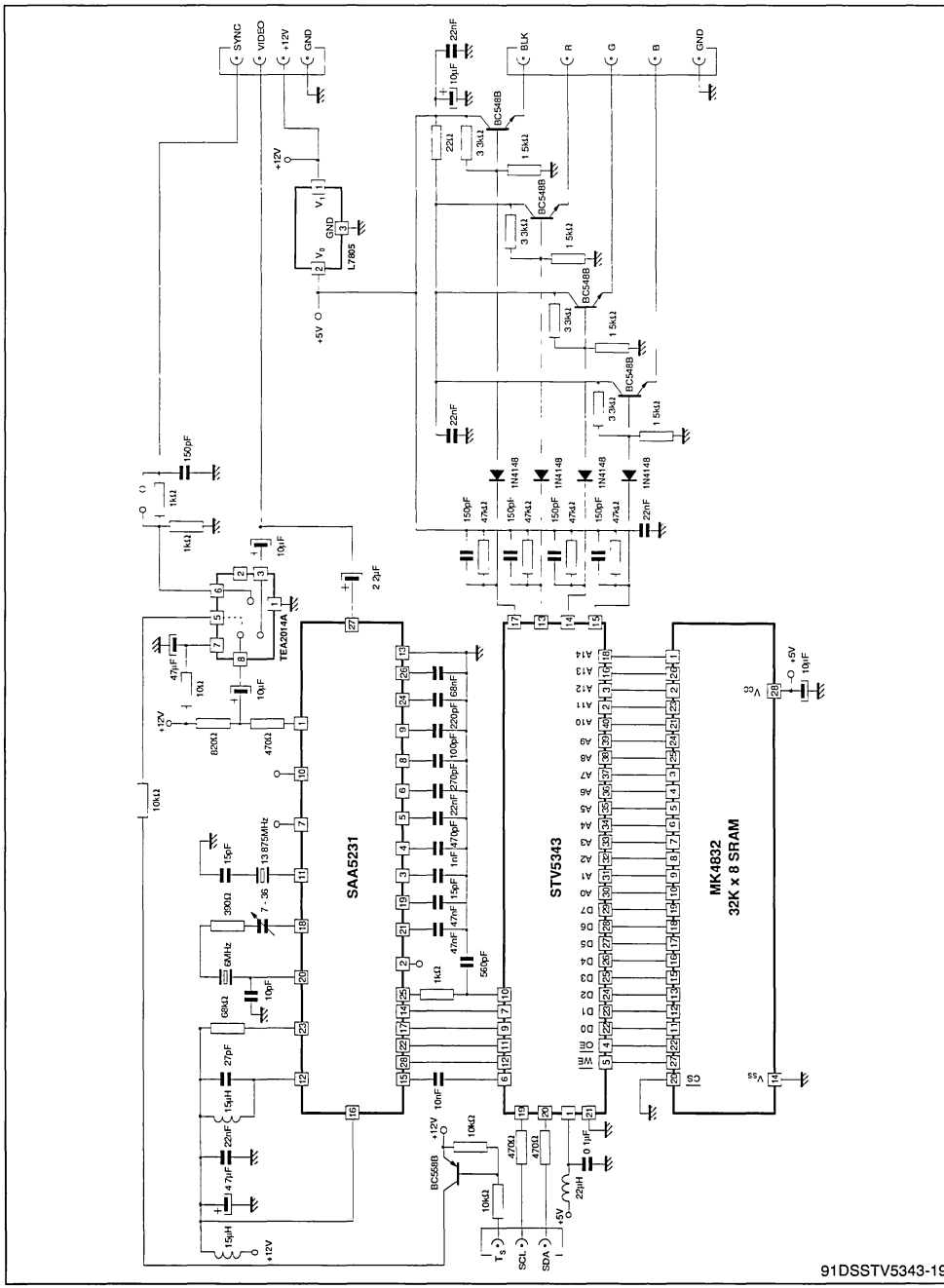


Figure 2b : 64-page Application with DRAM



APPLICATION DIAGRAM (STV5343 in DIP40 with 32K x 8 SRAM)

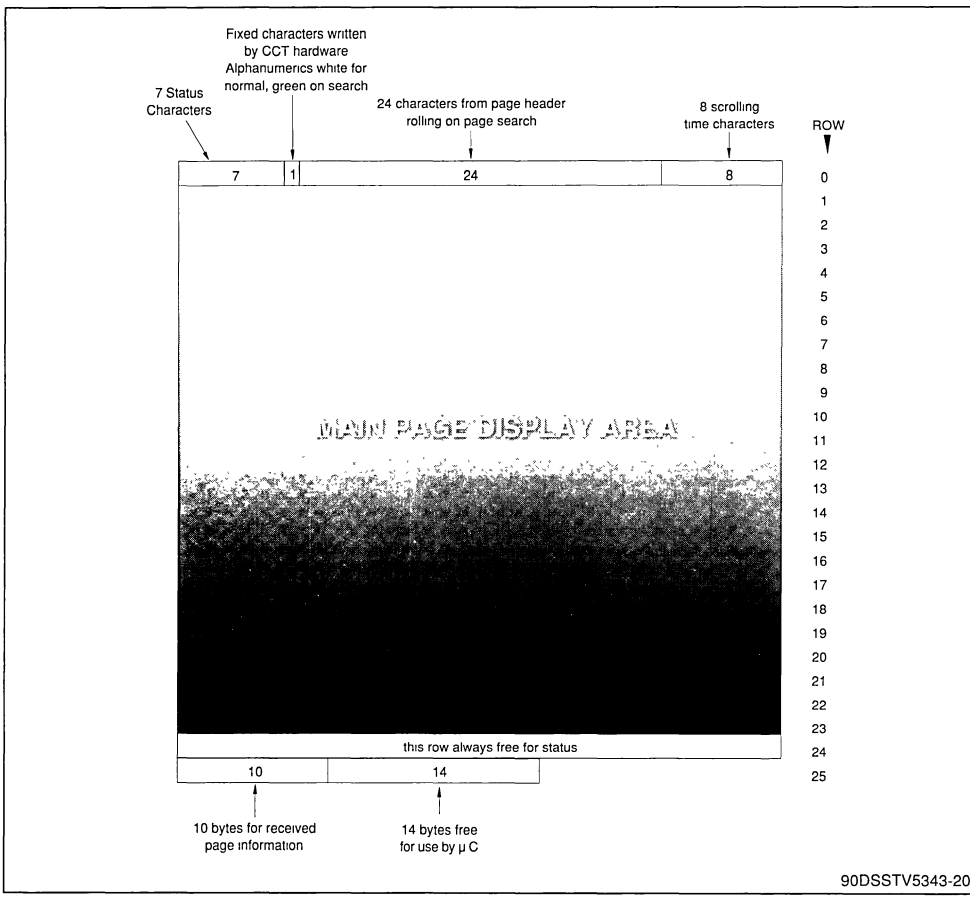


APPLICATION NOTES

ORGANIZATION OF A PAGE-MEMORY

The organization of a page-memory is shown below. In contrast with the first generation of Teletext Decoders the new CCT (Computer Controlled Teletext) chip provides a display format of 25 rows of 40 characters per row.
Row number twenty-four is used by the microprocessor for the display of information.
Row zero contains the page header.
The organization is as follows :
The first seven characters (0 - 6) are used for messages regarding the operational status.
The eighth character is an alphanumeric control character either "white" or "green" defining the "search" status of the page. When it is "white" the operational state is normal and the header appears white ; when it is "green" the operational state corresponds to "search mode" and the header appears green. The following twenty-four characters give the header of the requested page when the system is in search mode. The last eight characters display the time of day.
Row twenty-five comprises ten bytes of control data concerning the received page (see Table 1) and fourteen free bytes which can be used by the microprocessor.

PAGE MEMORY ORGANISATION



REGISTER FUNCTIONS

Register	Function	Bit(s)	Description
R0 Address 00H	R11 adressing and pin functions control	SEL 11B (D0)	Selection of register 11B (D0 = 1) or 11A (D0 = 0)
		CE ON (D1)	Selection of signal output on pin 16 (17 in 42SDIP) : CE (D1 = 1) or COR (D1 = 0)
		EVEN OFF (D2)	Control of ODD/EVEN pin : EVEN signal output (D2 = 0) or grounded (D2 = 1)
		EOE (D3)	D3 = 1 OE = 1, D3 = 0 OE active
		EWE (D4)	D4 = 1 WE = 1, D4 = 0 WE active
R1 Address 01H	Operating mode controls	T0 T1 0 0 0 1 1 0 1 1	312/313 line MIX - mode with interlace 312/313 line TEXT - mode without interlace 312/313 line Terminal mode without interlace External synchronization TCS/SCS is an input
		TCS ON (D2)	This bit determines the character display synchronization mode. Teletext composite synchronism (TCS ON = 1) or direct broadcast synchronism (TCS ON = 0).
		DEW / FULLFIELD (D3)	Selection of field flyback mode or full channel mode (D3 = 1) for recovering of Teletext data.
		GHOST ROW ENABLE (D4)	Selection of ghost row mode (D4 = 1)
		ACQUISITION ON / OFF (D5)	Control of acquisition operation (D5 = 0 enables acquisition)
		7 bits + parity or 8 bits without parity (D6)	Selection of received data format either 7 bits with parity (D6 = 0) or 8 bits without parity (D6 = 1).
R2 Address 02H	Addressing information for a page request	SC0, SC1, SC2 (D0, D1, D2)	Address the first column of the on chip page request RAM to be written.
		TB (D3)	Test bit equal to "0" in the normal working mode.
		A0, A1 (D4, D5)	Address a group of four consecutive pages currently used for data acquisition;
		A2 (D6)	Address of one of the two groups of four pages for acquisition in normal mode.
R3 Address 03H	Data relative to the requested page (see Table 3)	PRD0 - PRD4 (D0 - D4)	Written data in the page request RAM, starting with the columns addressed by SC0,SC1,SC2.
R4 Address 04H	Selection of one of eight pages to display	A0, ... A5 (D0, ... D5)	These 6 bits correspond to the logical states of the 6 address lines (A10, ... A15) during memory read cycles.
R5 Address 05H	Display control for normal operation	PON (D0, D1)	Picture on (IN: D0, OUT: D1)
		TEXT (D2, D3)	Text on (IN: D2, OUT: D3)
		COR (D4, D5)	Contrast reduction on (IN: D4, OUT: D5)
		BKGND (D6, D7)	Background colour on (IN: D6, OUT: D7)
		IN / OUT	Enable inside/outside the box
R6 Address 06H	Display control for news-flash subtitle generation	See R5	See R5

REGISTER FUNCTIONS (continued)

Register	Function	Bit(s)	Description
R7 Address 07H	Display mode	BOX ON 0, 1-23,24 (D0, D1, D2)	The "boxing" function is enabled on row 0,1-23 and 24 by D0, D1 and D2 set to one.
		STATUS ROW BTM / TOP (D7)	The 25th row is displayed before the "Main text Area" (lines 0-23) or after (D7 = 0).
R8 to R11A Address 08H to 0BH*	Active chapter address (R8), active row address (R9), active column address (R10). Data contained in R11A read (written) from (to) memory by microprocessor via I^2C.		
R11B Address 0BH*	Status	VCS ON (D0)	Good VCS quality signal detected (D0 = 1) or disturbance (D0 = 0)
		60Hz (D7)	VCS received with 60Hz frequency (D7 = 1) or 50Hz (D7 = 0). Valid only when if good V_{CS} (D0 = 1)
R12 Address 0CH	Page request address	A3, A4, A5 (D0, D1, D2)	Address one of up to 8 groups of 8 pages currently used for acquisition
		A0, A1 (D3, D4)	A0, A1 addresses of displayed page to refresh when using refresh on display function
		EROD (D5)	Enable refresh on displayed page function when = 1 normal acquisition storage if EROD = 0

* Reading of R11A or R11B is determined by register 0, bit D0. Nevertheless, write operation is always performed on R11A register.

Table 1 : Row 25 received control data format.

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM	HAM	HAM	HAM	HAM	HAM	HAM	HAM	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
COLUMN	0	1	2	3	4	5	6	7	8	9

Page number · - MAG = magazine, PU = page units, PT = page tens.
Page sub-code · - MU = minutes units, MT = minutes tens, HU = hours units, HT = hours tens.
PBLF = page being looked for, FOUND = low for page found, HAM = hamming error in byte, C4-14 = control bits.

REGISTER MAP (see Table 2)

Registers R0 to R10 and R12 are write only whilst R11A is a read/write and R11B is a read only register respect to the microprocessor.
The automatic succession on a byte basis is indicated by the arrows in Table 2.
In the normal operating mode TB should be set to logic level 0.
After power-up the contents of the registers are as follows : all bits in registers R0 to R12 are cleared to zero with the exception of bits D0 an D1 in registers R5 and R6 which are set to logical one.
After power-up all the memory bytes are preset to hexadecimal value 20 H (space) with the exception of the byte corresponding to row 0 of column 7 of chapter 0 which is set to the value corresponding to "alpha white" hexadecimal value 07 H.

Table 2 : Register specification.

D7	D6	D5	D4	D3	D2	D1	D0		
*	*	*	EWE	EGE	EVEN OFF	CE ON	SEL 11B	R0	Mode 0
*	$\overline{7+P/}$ 8 BIT	$\underline{ACQ}$ $\overline{ON/OFF}$	GHOST ROW ENABLE	$\overline{DEW/}$ FULL FIELD	TCS ON	T1	T0	R1	Mode 1
*	BANK SELECT A2	ACQ CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request adress
*	*	*	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
*	*	A5	A4	A3	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash / subtitle)
STATUS $\underline{ROW}$ BTM/TOP	CURSOR $\underline{ON/OFF}$	$\overline{CONCEAL/}$ REVEAL	TOP/ BOTTOM	$\overline{SINGLE/}$ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
*	A5	A4	A3	CLEAR MEM	A2	A1	A0	R8	Active chapter
*	*	*	R4	R3	R2	R1	R0	R9	Active row
*	*	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11A	Active data
60Hz	0	0	0	0	0	0	V_{CS} ON	R11B	Status
*	*	EROD	A1	A0	A5	A4	A3	R12	Page request address

* Reserved register bits : must be set to 0

REFRESH ON DISPLAY FUNCTION

This function allows independently to fill the memory using 3 acquisition circuits when the 4th one refreshes the displayed page.

- When EROD (Bit 5 of Reg. 12) is 0, refresh on display function is not active. Four teletext pages are filled into memory corresponding to addresses of acquisition registers.
  8 pages bank number, among 0 to 7, is selected with A5/A4/A3 (b2/b1/b0 of Reg. 12)
  Upper or lower bank of 4 pages is selected with A2 (b6 of Reg. 2).
  Acquisition circuits are selected with A1/A0 (b5/b4 of Reg. 2). This 2 bits also determine the 1KByte of RAM (the chapter) allocated to each acquisition circuit.
- When EROD = 1, refresh on display function is active.
  3 acquisition circuits store pages as described above. The 4th one stores data into the current displayed chapter. The chapter is selected with addresses A5/A4/A3/A2/A1/A0 (b5/b4/b3/b2/b1/b0 of Reg. 4). Notice that A1/A0 (b1/b0 of Reg. 4) give the circuit number to be used to refresh this displayed chapter. That means A1/A0 of refresh on display function (b4/b3 of Reg. 12) have to be written identical to A1/A0 (b1/b0 of Reg. 4), as A2 of acquisition circuit (b6 of Reg. 2) has to be identical to A2 of displayed chapter (b2 of Reg. 4).

Table 3 : Register R3.

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care page tens	PT3	PT2	PT1	PT0
2	Do care page units	PU3	PU2	PU1	PU0
3	Do care hours tens	X	X	HT1	HT0
4	Do care hours units	HU3	HU2	HU1	HU0
5	Do care minutes tens	X	MT2	MT1	MT0
6	Do care minutes units	MU3	MU2	MU1	MU0

The abbreviations have the same significance as in Table 1 with the exception of the "DO CARE" entries. It is only when this bit is "1" that the corresponding digit is taken into consideration on page request. For example, a page defined as "normal" or one defined as "timed" may be selected.

If "HOLD" is low the page is held. The addressing of successive bytes via the I^2C is automatic.

CHARACTER SETS

The selection of the character sets for a particular language is effected by the three control bits (C12-C14) located in the page header. These three bits are decoded as shown in Table 4.

Table 4 : National character sets control bits.

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH	SPANISH
C12	0 (1) (1)	0	0	0	1	1
C13	0 (1) (1)	0	1	1	0	0
C14	0 (0) (1)	1	0	1	0	1

The basic set of the 96 characters is shown in Table 5.The location of the 13 national characters are shown in Table 5 whilst full national character sets are depicted in Tables 6 thru 11.

Table 5 : Basic character set.

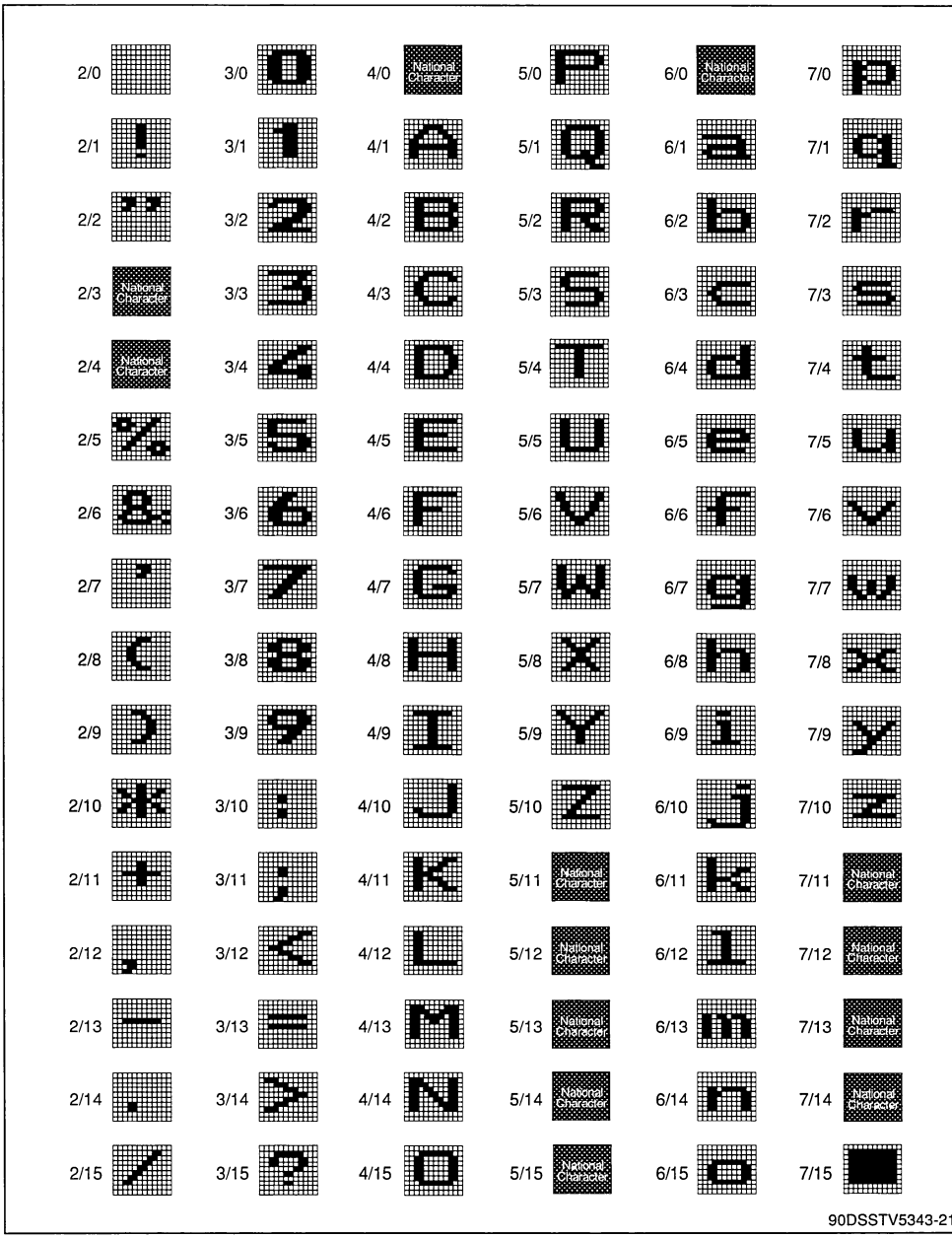


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Table 6 : English Basic Character Set

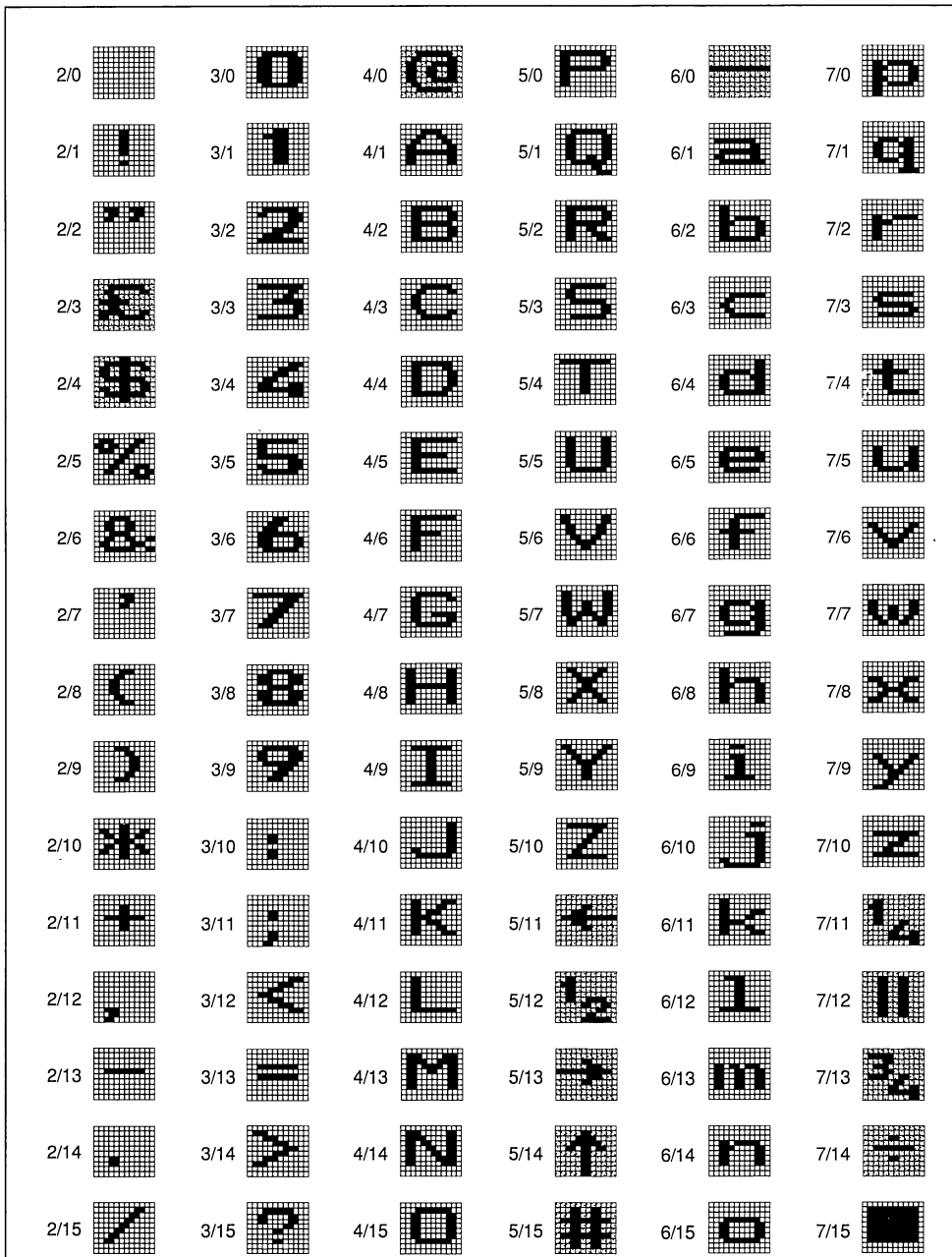

Table 7 : German Basic Character Set

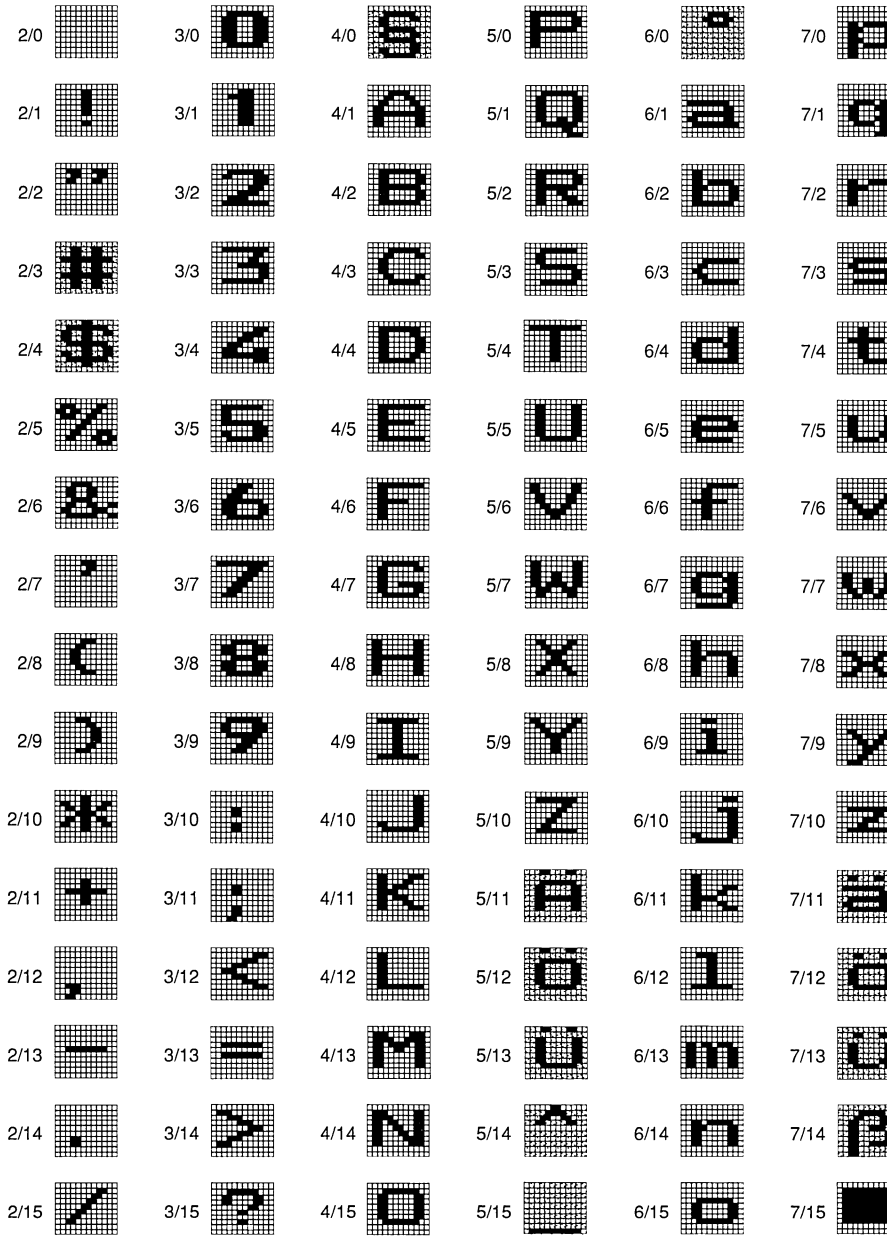

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Table 8 : Swedish Basic Character Set

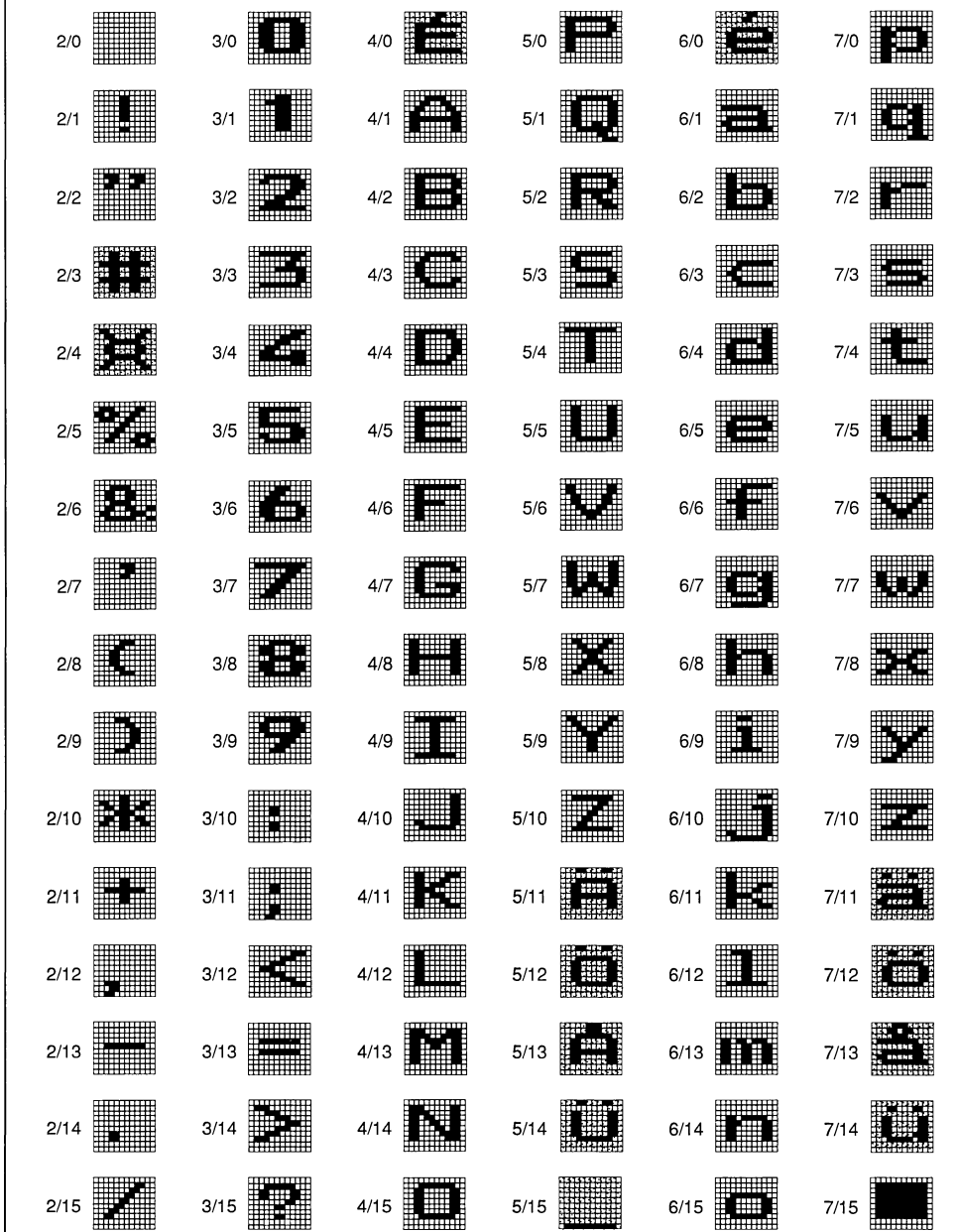

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Table 9 : Italian Basic Character Set

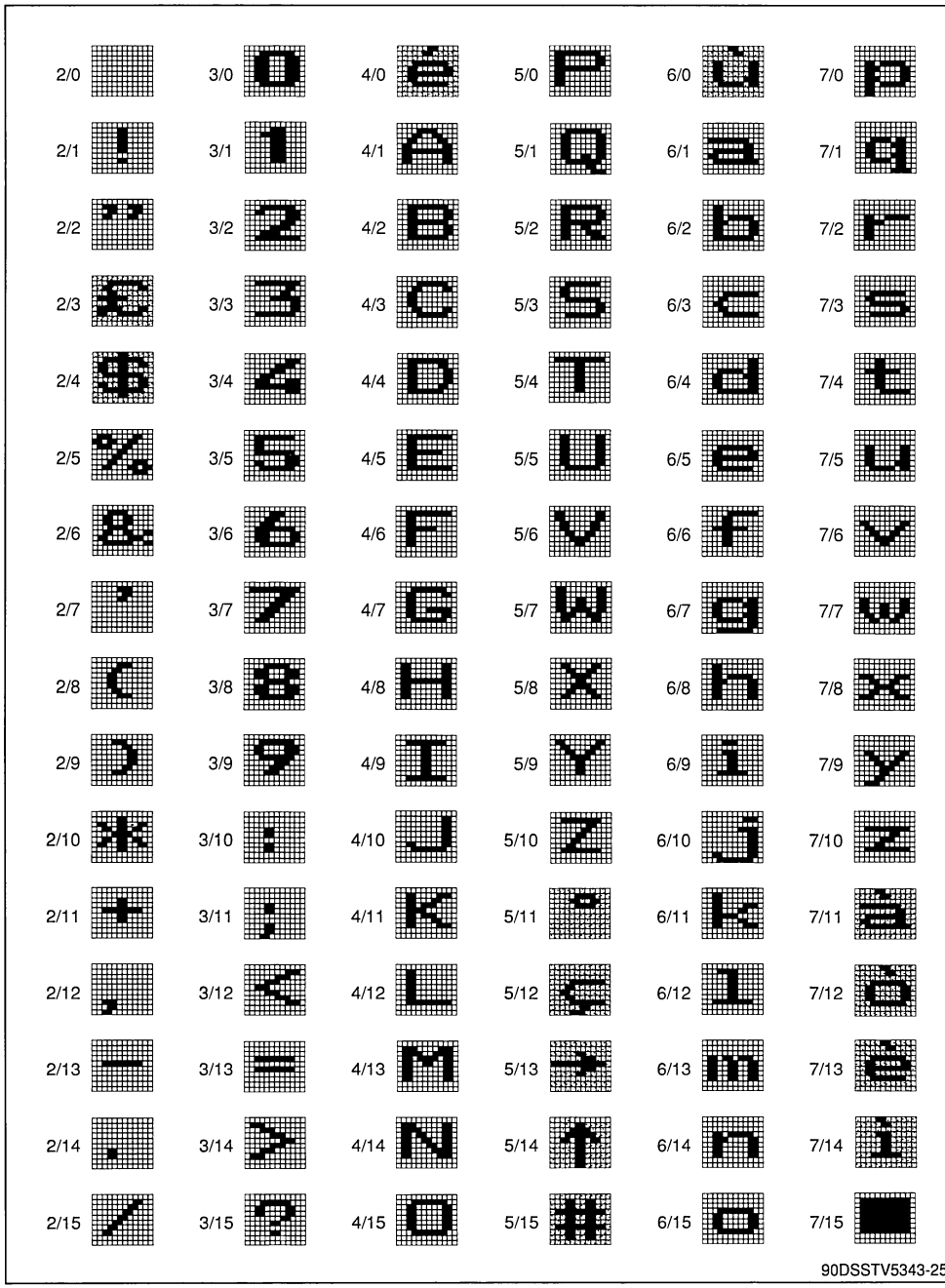

Table 10 : French Basic Character Set

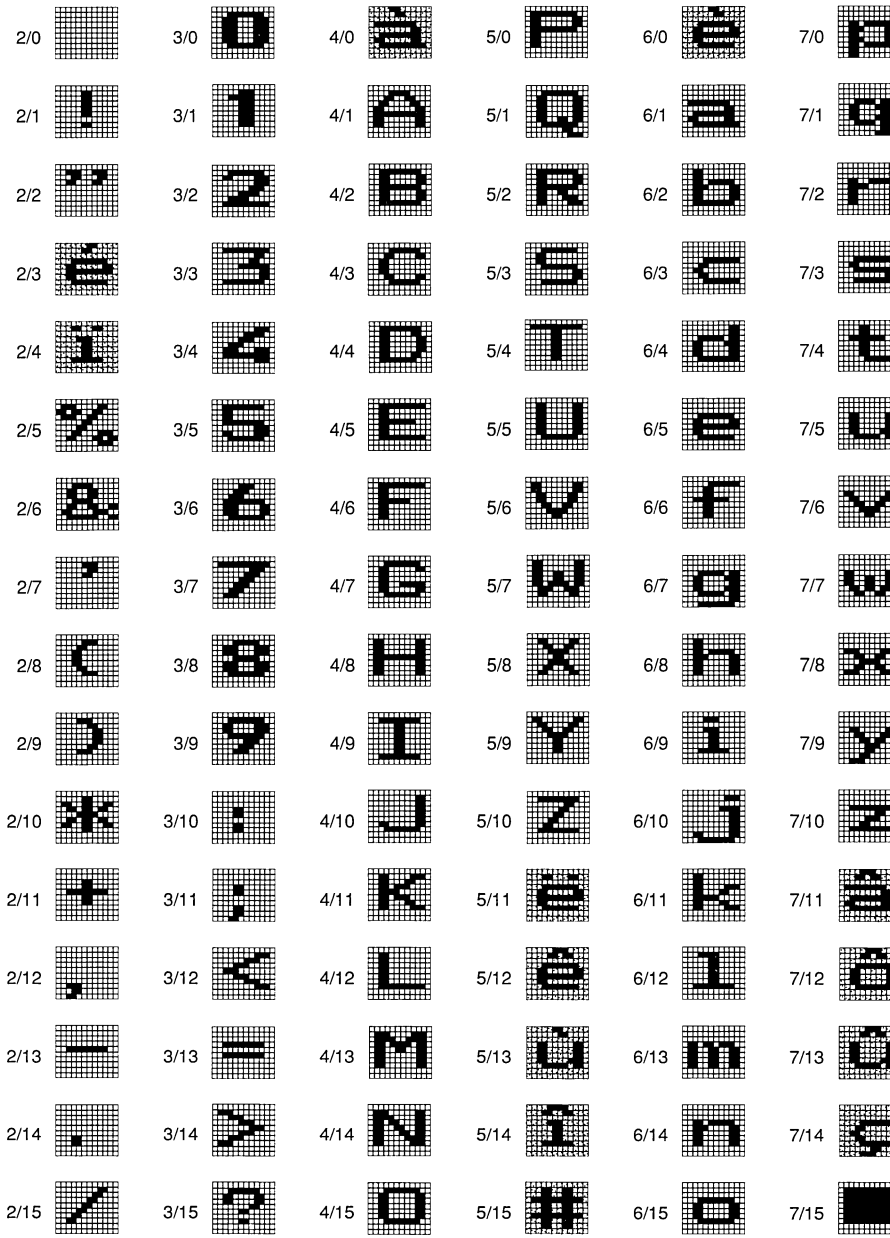

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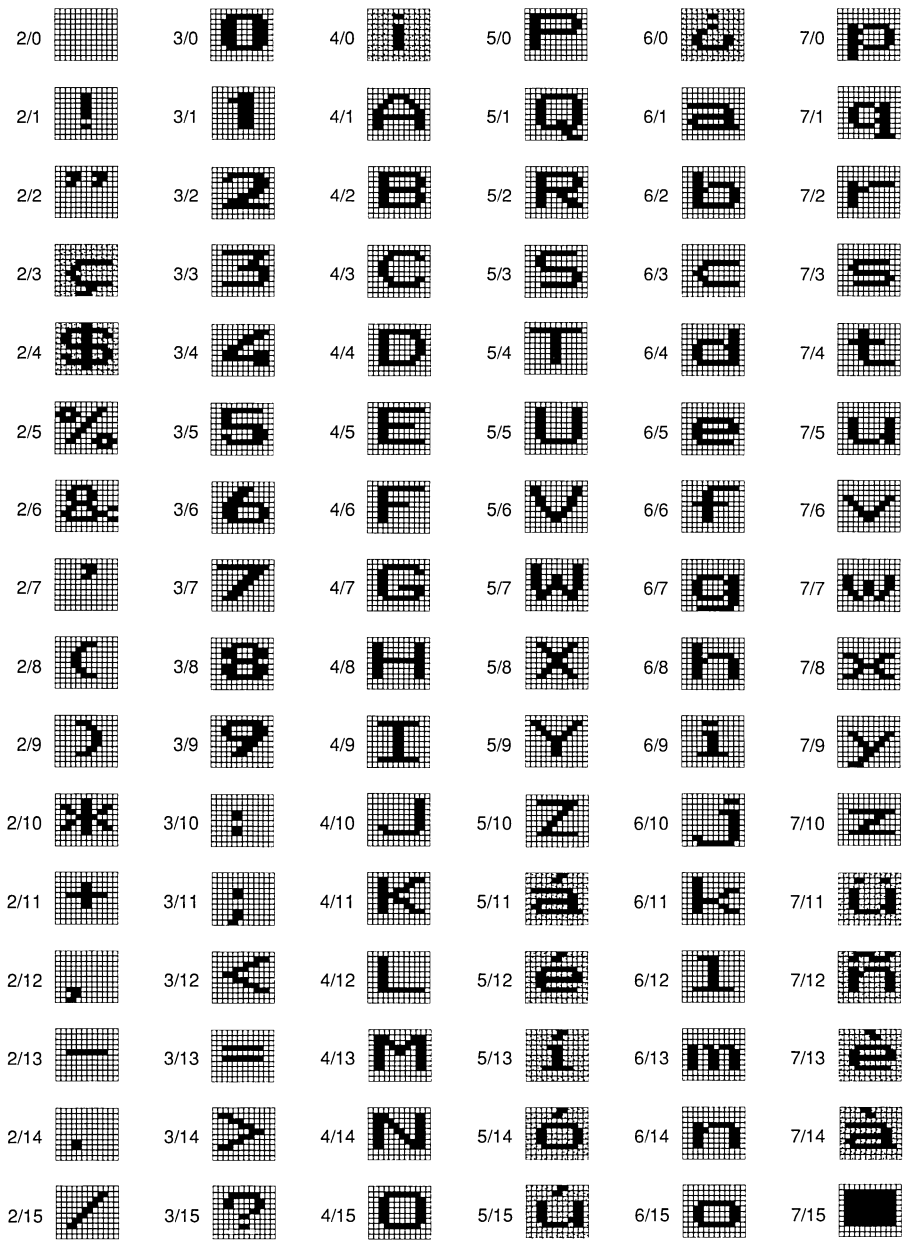
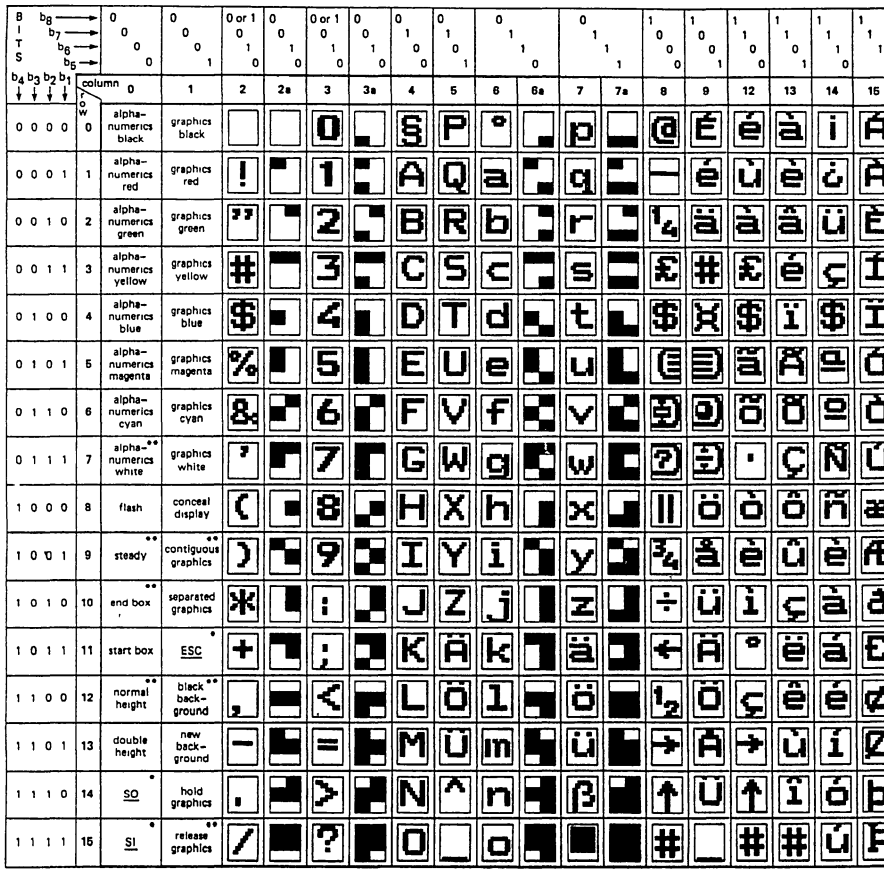
Table 11 : Spanish Basic Character Set



The complete character set with 8-bit decoding and using the German national character is given in Table 7.
Characters in columns 0 and 1 are normally displayed as blanks. Black dots represent the character shape whereas white dots represent the background.
Each character can be identified by a pair of corresponding row and column integers : for example the character "3" may be indicated by 3/3.
A rectangle may be represented as follows : ▭
The characters 8/6, 8/7, 9/5, 9/7 are used as special characters, always in conjunction with 8/5.
The 13 national characters are placed in columns with bit 8 = 0.

Table 7: Complete character set (with 8 bit codes).



* These control charcters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins

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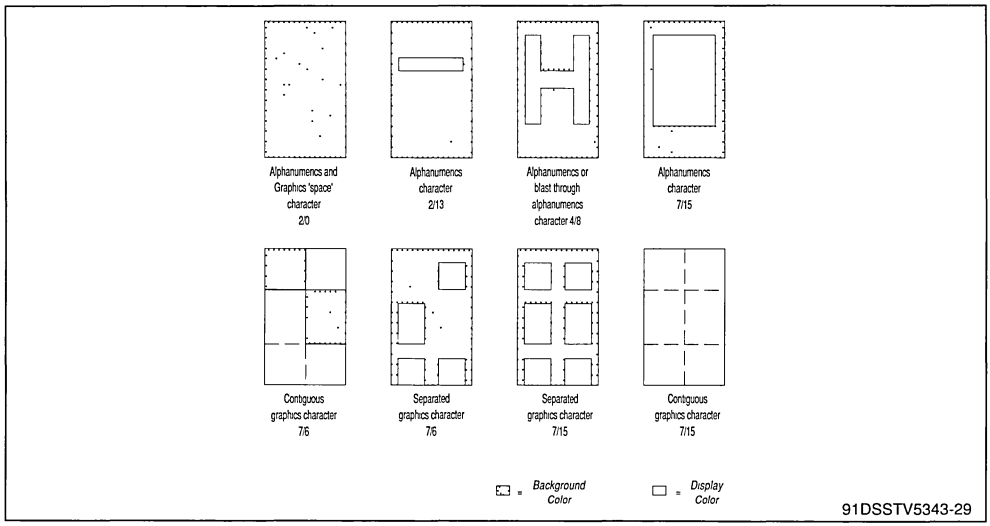
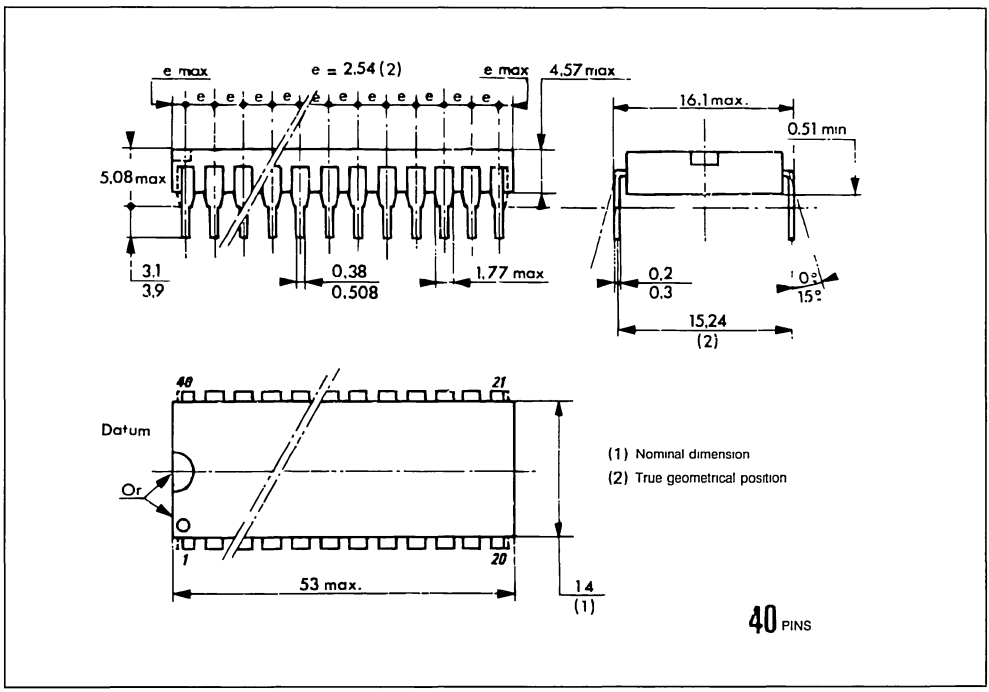
Figure 12: Character Format



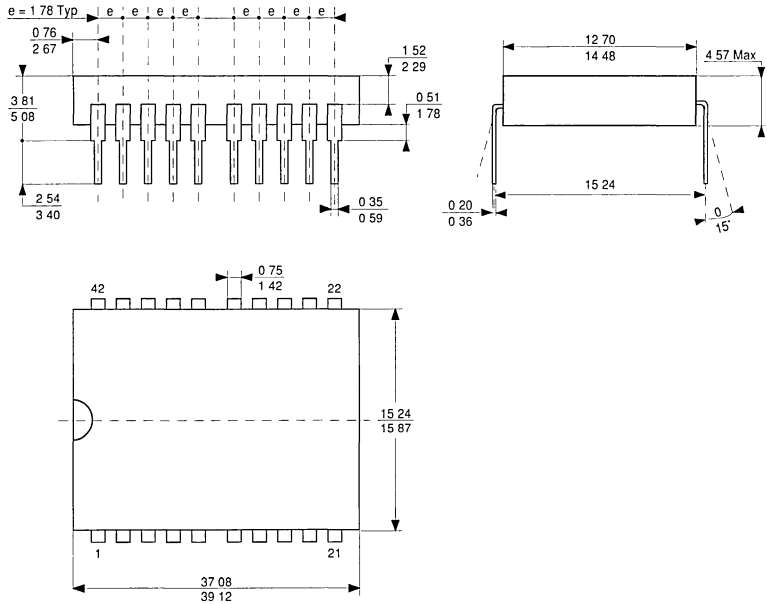
PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



PACKAGE MECHANICAL DATA

42 PINS - PLASTIC SHRINK DIP



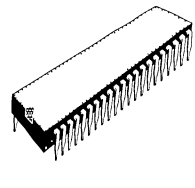
SGS-THOMSON MICROELECTRONICS

STV8438

TRIPLE 8-BIT D/A CONVERTER

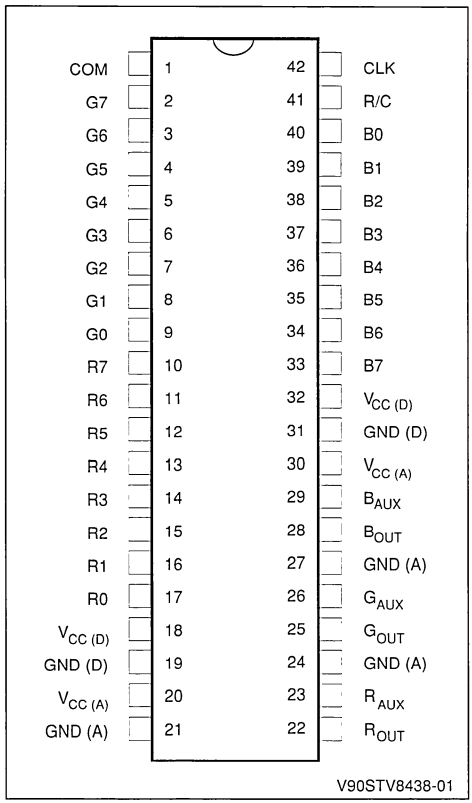
ADVANCE DATA

- 3 CHANNEL D/A CONVERTER
- 8-BIT RESOLUTION
- 70 MEGASAMPLES PER SECOND CONVERSION RATE
- AUXILIARY ANALOG R, G, B, SWITCHING CAPABILITIES
- SINGLE VOLTAGE +5V OPERATION
- ON-CHIP VOLTAGE REFERENCE
- VOLTAGE OUTPUT BUFFER AMPLIFIER
- TTL COMPATIBLE DIGITAL INPUTS
- BINARY INPUT ON ALL CHANNELS
- 2'S COMPLEMENT INPUT CAPABILITY ON TWO CHANNELS
- MONOLITHIC BIPOLAR
- 850 mW POWER DISSIPATION
- OPERATING TEMPERATURE RANGE $0^{o}C$ to + $70^{o}C$
- SHRINK DIP 42-PIN PACKAGE



SHRINK 42
(Plastic Package)

PIN CONNECTIONS



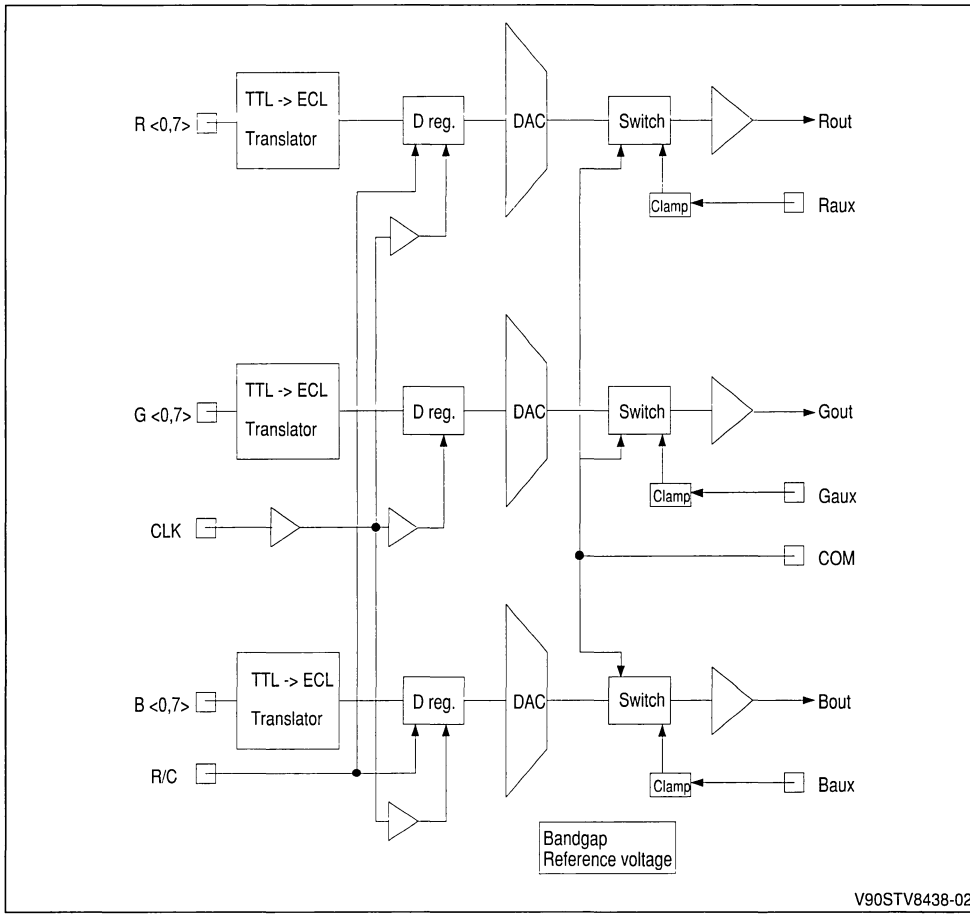
V90STV8438-01

DESCRIPTION

This Digital-to-Analog converter is a monolithic voltage output converter which can accept TTL-level digital input voltages.
The STV8438 contains three 8-bit D/A converters with a high performance on-chip voltage reference. Internal analog multiplexing between the signals from the internal D/A converter and from auxiliary analog R, G, B signals is provided. Either binary or 2's Complement inputs are available for two of the three channels.
This device is particularly recommended for use in video processing applications with the capability of 70Msps data conversion rate with excellent linearity.

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

BLOCK DIAGRAM



PIN ASSIGNMENT

N° Pin Number	Symbol	Type	Function
1	COM	I	Analog switch selection
2 to 9	G < 0:7>	I	Digital input channel G
10 to 17	R < 0:7>	I	Digital input channel R
18 to 32	V_{CC} (D)	I	Digital power supply
19 to 31	GND (D)	I	Digital ground
20 to 30	V_{CC} (A)	I	Analog power supply
21	GND (A)	I	Analog R channel ground
22	R_{OUT}	O	Analog output, R channel
23	R_{AUX}	I	Auxiliary analog input, R channel
24	GND (A)	I	Analog G channel ground
25	G_{OUT}	O	Analog output, G channel
26	G_{AUX}	I	Auxiliary analog input, G channel
27	GND (A)	I	Analog B channel ground
28	B_{OUT}	O	Analog output, B channel
29	B_{AUX}	I	Auxiliary analog input, B channel
33 to 40	B < 0:7>	I	Digital input channel B
41	R/C	I	Binary or 2's complement selection
42	CLK	I	Clock input

PIN DESCRIPTION

COM : Digital or analog inputs selection
This TTL input selects on the output stage the signal from the D/A converter or the signal from the external analog input. The three internal analog switches are activated by the COM signal.

COM = 0 connects auxiliary analog inputs to output amplifier
COM = 1 connects internal digital channel to output amplifier

G <0:7> : Digital input channel G
These TTL 8-Bit input data are sampled on the rising edge of the clock CLK. G_0 is the LSB and G_7 the MSB, coding is binary.

R <0:7>: Digital input channel R
These TTL 8-Bit input data are sampled on the rising edge of the clock CLK. R_0 is the LSB and R_7 the MSB. Coding is binary if the R/C input is high, coding is 2's complement if the R/C input is low.

B <0:7> : Digital input channel B
These TTL 8-Bit input data are sampled on the rising edge of the clock CLK. B_0 is the LSB and B_7 the MSB. Coding is binary if the R/C input is high, coding is 2's complement if the R/C input is low.

R/C : Binary/2's complement coding selection
This TTL input selects the coding type on R and B channels.

R/C = 0 selects 2's complement coding on R and B channels
R/C = 1 selects Binary coding on R and B channels

R_{AUX} : Auxiliary analog input, R channel
This analog input is connected to the output Rout through the output amplifier if the COM signal is low.

G_{AUX} : Auxiliary analog input, G channel
This analog input is connected to the output G_{OUT} through the output amplfier if the COM signal is low.

B_{AUX} : Auxiliary analog input, B channel
This analog input is connected to the output B_{OUT} through the output amplifier if the COM signal is low.

R_{OUT} : Analog output, R channel
This voltage analog output corresponds to the digital channel R if the COM signal is high or to the auxiliary analog input R_{AUX} it the COM signal is low.

G_{OUT} : Analog output, G channel
This voltage analog output corresponds to the digital channel G if the COM signal is high or to the auxiliary analog input G_{AUX} if the COM signal is low.

B_{OUT} : Analog output, B channel
This voltage analog output corresponds to the digital channel B if the COM signal is high or to the auxiliary analog input B_{AUX} if the COM signal is low.

CLK : Clock signal
The digital inputs are sampled on the rising edge of this TTL input signal.

V_{CC} (A) / GND (A) : Analog power supply
V_{CC} (D) / GND (D) : Digital power supply.

CIRCUIT DESCRIPTION

The STV8438 is designed with 3 identical D/A converters. Each D/A converter is constituted of two 4-bit DACs separated by a current divider the elementary DAC is composed of multiple identical current switches supplied with the same current allowing high speed conversion rate.

DIGITAL INPUT CHANNELS

The STV8438 supports binary coding on the 3 R, G, B, input channels when R/C pin is high. When R/C pin is low, a 2's complement coding is applied to the R and B channels this provides the capability to use the STV8438 with luminance and chrominance coded signal ; the luminance signal (usually called Y) being applied to the G channel, the chrominance signals (called U, V) being applied respectively to the R and B channels.
The input range on Y signal is 0/255 and the input range on both U, V signals is -127/+128. Whatever binary coding or 2's complement coding the output voltage is in the range of 1,685V for the lowest code to 3,315V for the highest code.

ANALOG INPUT CHANNELS

The STV8438 provides the capability to switch the output voltage from signals coming from the digital channels or from signal coming from auxiliary analog inputs. When COM signal is low, the auxiliary analog signals are connected to the output amplifier internaly clamped to the 16th digital step. When COM signal is high, the digital inputs after D/A conversion are connected to the output amplifier.

ANALOG OUTPUTS

The output voltage amplifiers have an output range of 1,685V to 3,315V. The 1,685V corresponds to the binary code Ø (R/C = 1) or to the 2's complement code -127 (R/C = 0). The 3,315V corresponds to the maximum value on the digital code 255 if R/C = 0, +128 if R/C = 1.
The STV8438 provides a step if 6,39mV per LSB. Using the analog input signal (COM = 0), the output amplifier has a gain of 2.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	8	V
P_{tot}	Power Dissipation	1.8	W
T_{oper}	Operating Temperature	- 40 to 85	°C
T_{stg}	Storage Temperature	- 55 to 150	°C

DC ELECTRICAL CHARACTERISTICS (Temperature 0 to 70°C, V_{CC} ± 5%)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
I_{CC}	Supply Current		170		mA
	Resolution			8	Bit
V_{OUTF}	Full Scale Output Voltage		3.315		V
V_{OUTZ}	Zero Scale Output Voltage		1.685		V
DL	Differential Linearity Error			± 0.5	LSB
IL	Integral Linearity Error			1	LSB
	Gain Conversion Error between RGB			± 2	%
P_D	Power Dissipation		850		mW

AC ELECTRICAL CHARACTERISTICS (Temperature 0 to 70°C, V_{CC} ± 5%)

ANALOG OUTPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Maximum Data Conversion Rate	70			Msps
t_S	Settling Time Figure 1 Figure 2			 14 28.5	ns
	Monotonicity		Guaranteed		
	Glitch Energy			80	pVs
t_{PD}	Propagation Delay (Figures 1 and 2)			4	ns
	Crosstalk between Any Outputs (f_{CLK} = 25MHz-input voltage.7V_{pp})	50			dB
	Crosstalk between any outputs when auxiliary analog inputs are selected (f_{CLK} = 25MHz .7V_{pp})	50			dB
R_{LOAD}	Output Load (AC coupled - see typical application diagram)	100	150		Ω
V_{OUT}	Output Voltage Range (on 150Ω AC coupled)		1.63		Vpp

AC ELECTRICAL CHARACTERISTICS (continued)

AUXILIARY ANALOG RGB INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SW}	Switching-time DAC/Analog Input (Figure 3)			5	ns
	Black Level Clamp Error			± 2.5	%
	Crosstalk between Any Outputs (f = 5MHz-input voltage.7V_{pp})	50			dB
	Crosstalk between RGB Analog Inputs and D/A Outputs (f = 5MHz-input voltage.7Vpp)	50			dB

ANALOG OUTPUTS FROM ANALOG INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
G	Voltage gain at f=1MHz (input voltage .7Vpp)		2.0		
BNa	Band-width (-3dB)	100			MHz
	Slew-rate (inp. pulse 0.7Vpp)	120	150		V/us
	Harmonic distortion rate at 1MHz			0.2	%

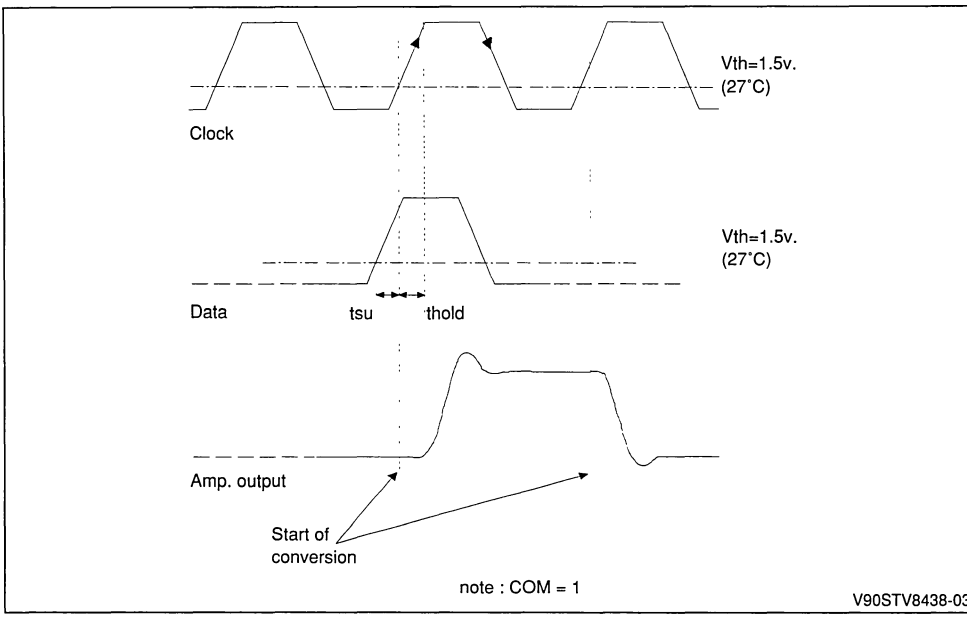
DIGITAL INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage High Level	2			V
V_{IL}	Input Voltage Low Level			0 8	V
I_{IH}	Input Current High Level			10	µA
I_{IL}	Inpur Current Low Level	-500			µA

SWITCHING CHARACTERISTICS

Symbol	Ac-parameter	Min.	Typ.	Max.	Unit
FCK	Clock Rate		100		MHz
	Clock Duty-cycle Rate		50		%
t_{CKR}	Clock Rise-time (10% - 90%)			3.5	ns
t_{CKF}	Clock Fall-time (90% - 10%)			3.5	ns
t_{SU}	Data Set-up Time to CLK	2.5			ns
t_{HOLD}	Data Hold-time from CLK	2.5			ns
t_D	Data Conversion Delay		1		cycle

INPUT TIMING DIAGRAM



SETTLING TIME MEASUREMENTS

Figure 1.

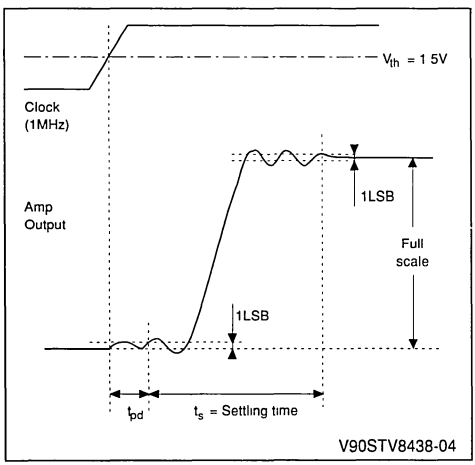
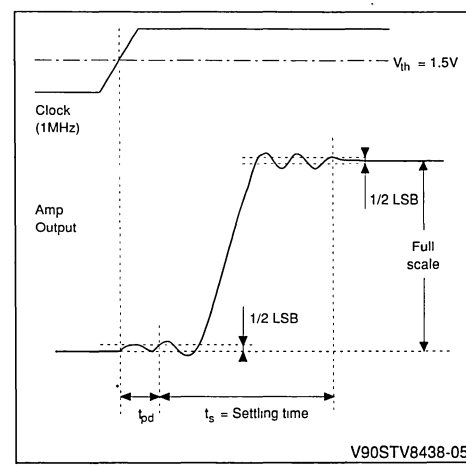
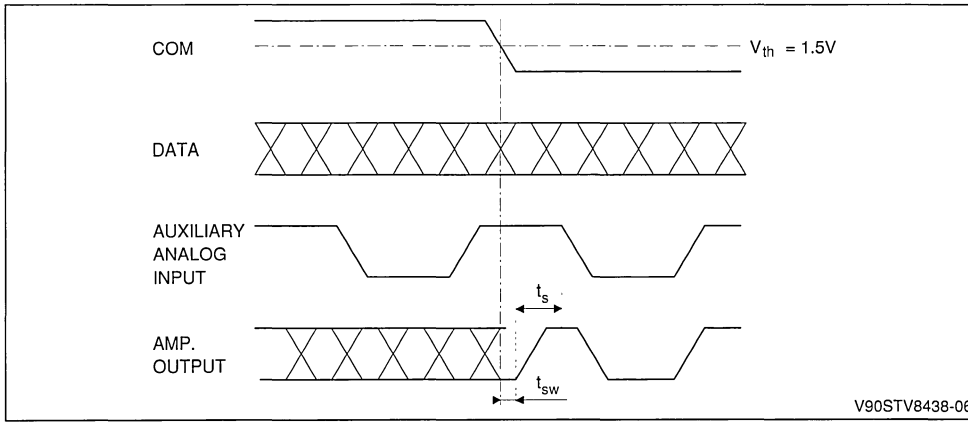


Figure 2.

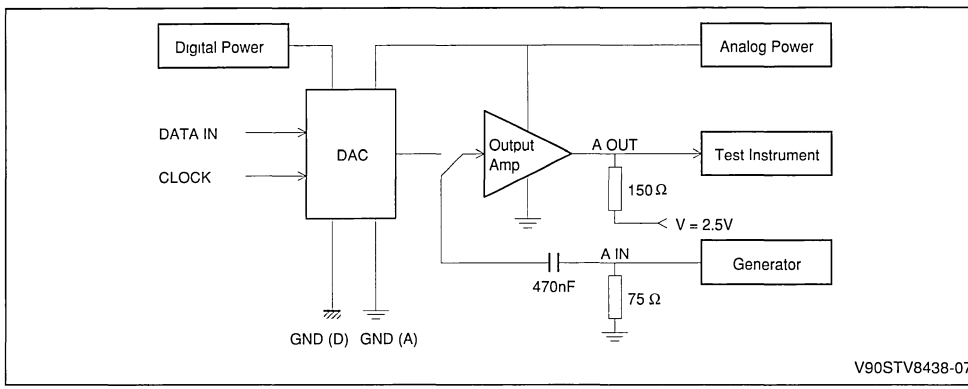


SWITCHING TIME DAC/AUXILIARY ANALOG INPUT MEASUREMENT

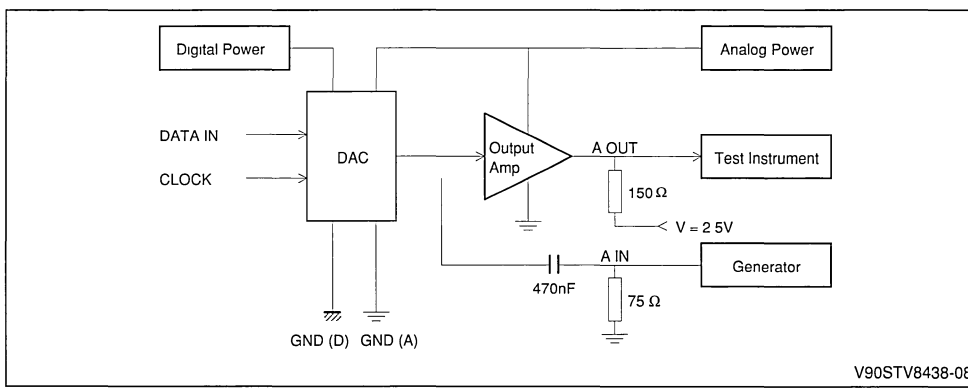
Figure 3.



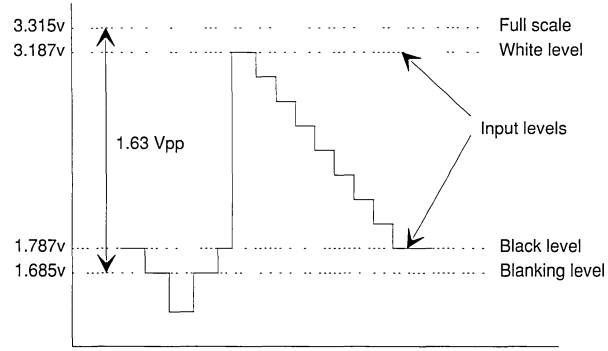
ANALOG-TEST SCHEMATICS



DAC-TEST SCHEMATICS



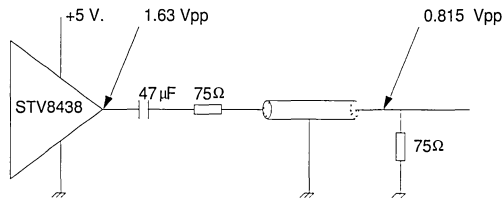
VOLTAGE AT BUFFER OUTPUT



note : Analog external RGB signals clamped to black level

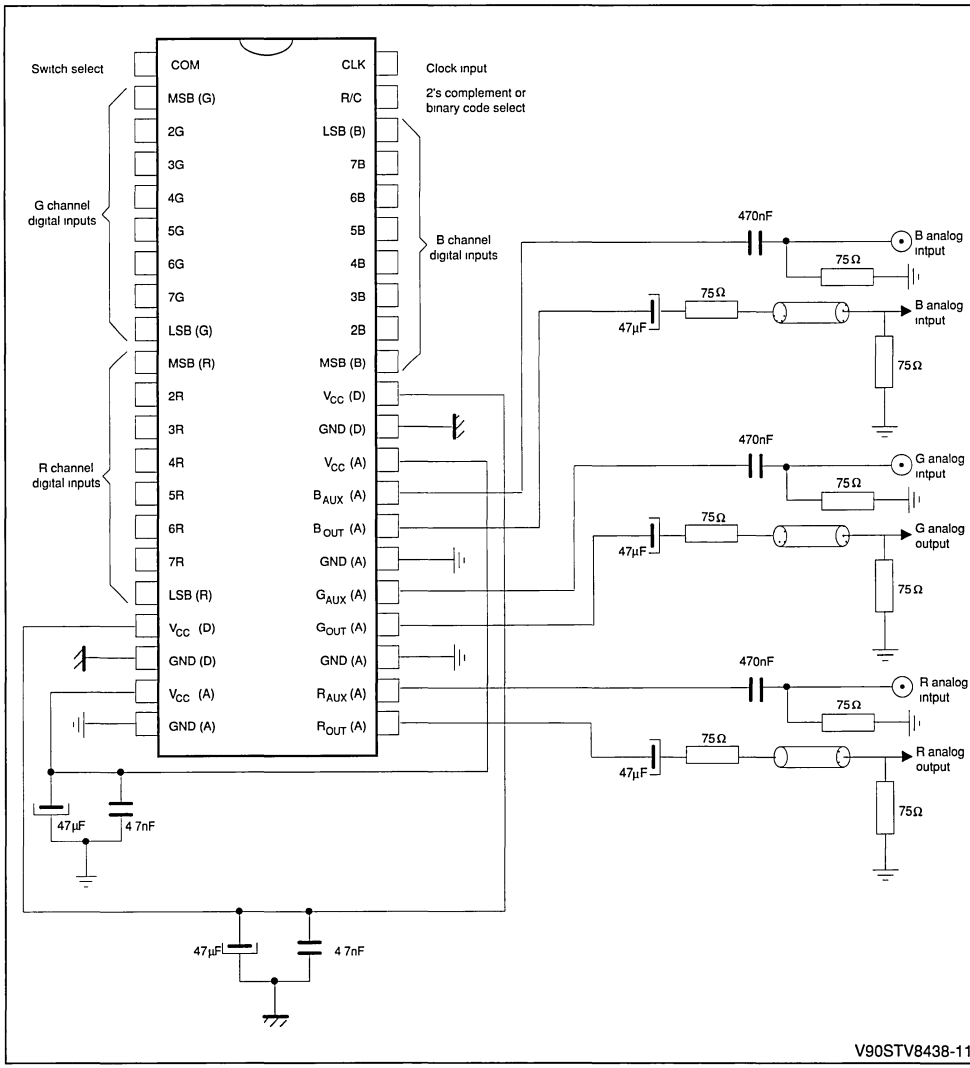
V90STV8438-09

OUTPUT 75 ΩMATCHING



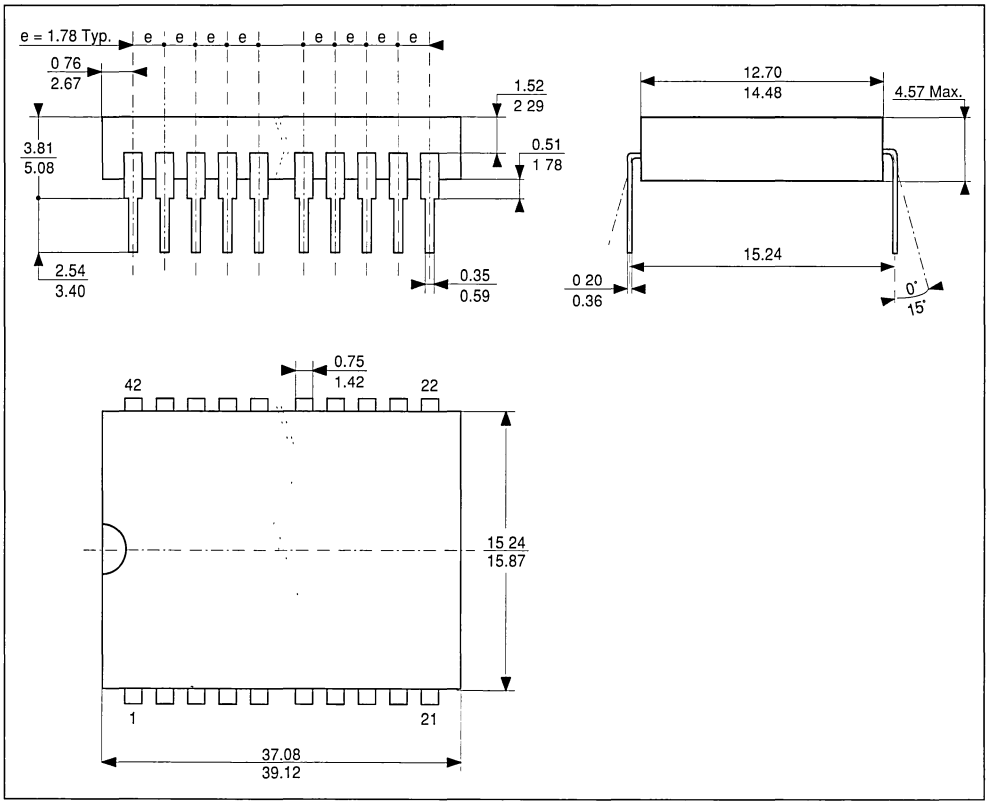
V90STV8438-10

TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

42 PINS - PLASTIC SHRINK DIP



PROGRAMMING MANUAL

INTRODUCTION

This manual deals with the description of instruction set and addressing modes of ST62,63 microcontroller series. The manual is divided in two main sections. The first one includes, after a general family description, the addressing modes description. The second one includes the detailed description of ST62,63 instruction set. Here following each instruction is deeply described and are underlined the differences among each ST6 series. ST6 software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short to provide byte efficient programming capability.

PROGRAMMING MODEL

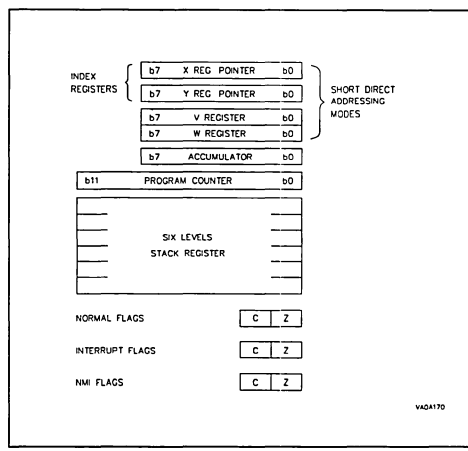
It is useful at this stage to outline the programming model of the ST62,63 series, by which we mean the available memory spaces, their relation to one another, the interrupt philosophy and so on.

Memory Spaces. The ST6 devices have three different memory spaces: data, program and stack. All addressing modes are memory space specific so there is no need for the user to specify which space is being used as in more complex systems. The stack space, which is used automatically with subroutine and interrupt management for program counter storage, is not accessible to the user.

Table 1. ST62,63 Series Core Characteristics

	ST62,63 Series
Stack Levels	6
Interrupt Vectors	5
NMI	YES
Flags Sets	3
Program ROM	2K + 2K• n 20K Max
Data RAM	64 byte • m
Data ROM	64 byte pages in ROM
Carry Flag SUB Instruction	Reset if A > Source
Carry Flag CP Instruction	Set if A < Source

Figure 1. ST6 Family Programming Model



PROGRAMMING MODEL (Continued)

Figure 2. ST62 Data Space Example

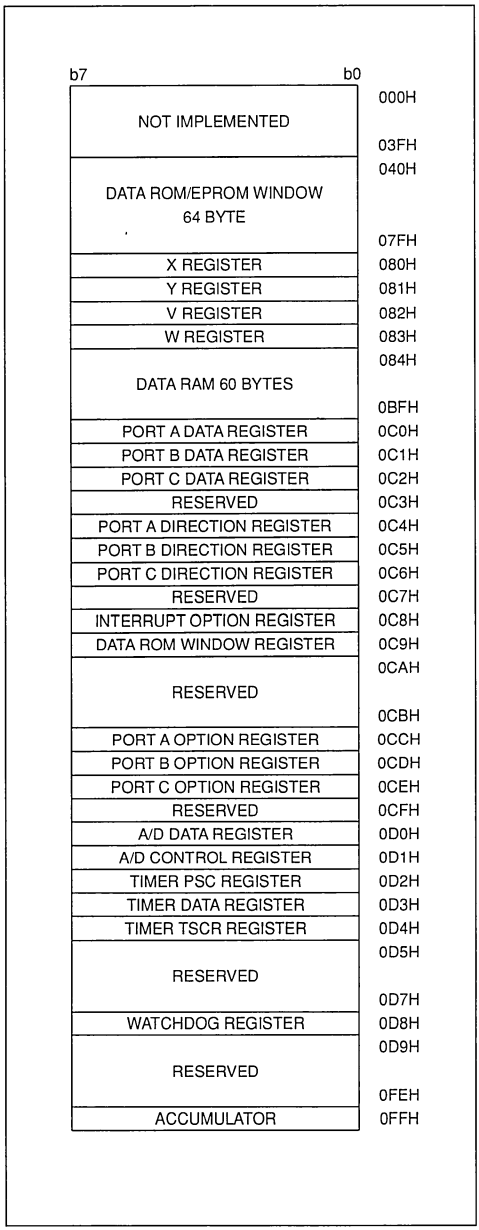
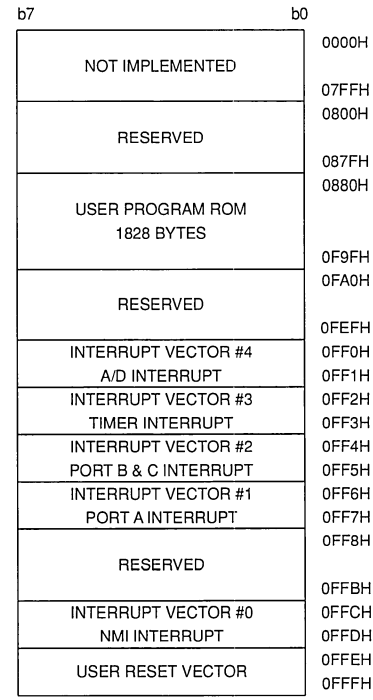


Figure 3. ST62 Program Memory Example



On EPROM versions there are no reserved areas. These reserved bytes are present on ROM/OTP versions.

Data Memory Space. The following registers in the data space have fixed addresses which are hardware selected so as to decrease access times and reduce addressing requirements and hence program length. The Accumulator is an 8 bit register in location 0FFH. The X, Y, V & W registers have the addresses 80H-83H respectively. These are used for short direct addressing, reducing byte requirements in the program while the first two, X & Y, can also be used as index registers in the indirect addressing mode. These registers are part of the data RAM space. In the ST62 and ST63 for data space ROM a 6 bit (64 bytes addressing) window multiplexing in program ROM is available through a dedicated data ROM banking register.

PROGRAMMING MODEL (Continued)

For data RAM and I/O expansion the lowest 64 bytes of data space (00H-03FH) are paged through a data RAM banking register.

Self-check Interrupt Vector FF8H & FF9H:
jp (self-check interrupt routine)

A jump instruction to the reset and interrupt routines must be written into these locations.

ST62 & ST63 Program Memory Space. The ST62 and ST63 devices can directly address up to 4K bytes (program counter is 12-bit wide). A greater ROM size is obtained by paging the lower 2K of the program ROM through a dedicated banking register located in the data space. The higher 2K of the program ROM can be seen as static and contains the reset, NMI and interrupt vectors at the following fixed locations:

Reset Vector FFEH & FFFH:
jp (reset routine)

NMI Interrupt Vector FFCH & FFDH:
jp (NMI routine)

Non user Vector FFAH & FFBH

Non user Vector FF8H & FF9H

Interrupt #1 Vector FF6H & FF7H jp (Int 1 routine)

Interrupt #2 Vector FF4H & FF5H jp (Int 2 routine)

Interrupt #3 Vector FF2H & FF3H jp (Int 3 routine)

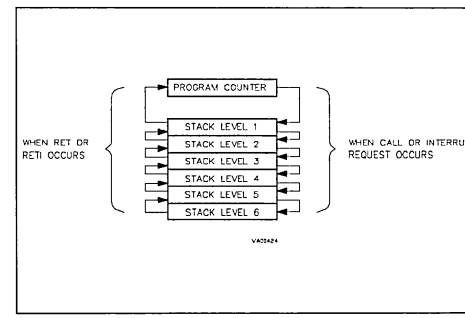
Interrupt #4 Vector FF0H & FF1H jp (Int 4 routine)

Program Counter & Stack Area. The program counter is a twelve bit counter register since it has to cover a direct addressing of 4K byte program memory space. When an interrupt or a subroutine occurs the current PC value is forward "pushed" into a deep LIFO stacking area. On the return from the routine the top (last in) PC value is "popped" out and becomes the current PC value. The ST60/61 series offer a 4-word deep stack for program counter storage during interrupt and sub-routines calls. In the ST62 and ST63 series the stack is 6-word deep.

Status Flags. Three pairs of status flags, each pair consisting of a Zero flag and a Carry flag, are available. In the ST62 and ST63 an additional third set is available. One pair monitors the normal status while the se-cond monitors the state during interrupts; the third flags set monitors the status during Non Maskable interrupt servicing. The switching from one set to another one is automatic as the interrupt requests (or NMI request for ST62,ST63 only) are acknowledged and when the program returns after an interrupt service routine. After reset, NMI set is active, until the first RETI instruction is executed.

ST62 & ST63 Interrupt Description. The ST62 and ST63 devices have 5 user interrupt vectors (plus one vector for testing purposes). Interrupt vector #0 is connected to the not maskable interrupt input of the core. Interrupts from #1 to #4 can be connected to different on-chip and external sources (see individual datasheets for detailed information). All interrupts can be globally disabled through the interrupt option register. After the reset ST62 and ST63 devices are in NMI mode, so no other interrupts can be accepted and the NMI flags set is in use, until the RETI instruction is performed. If an interrupt is detected, a special cycle will be executed, during this cycle the program counter is loaded with the related interrupt vector address. NMI can interrupt other interrupt routines at any time while normal interrupt can't interrupt each other. If more then one interrupt is waiting service, they will be accepted according to their priority. Interrupt #1 has the highest priority while interrupt #4 the lowest. This priority relationship is fixed.

Figure 2. ST62 & ST63 Stack Area

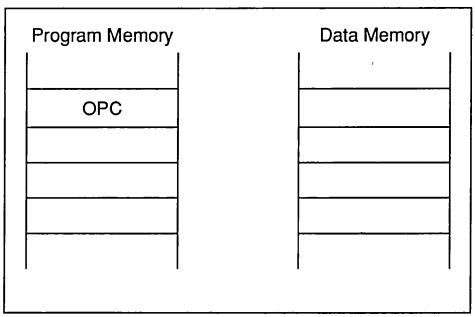


ADDRESSING MODES

The ST6 family gives the user nine addressing modes for access to data locations. Some of these are specifically tailored to particular instruction types or groups while others are designed to reduce program length and operating time by using the hardware facilities such as the X, Y, V & W registers. The data locations can be in either the program memory space or the data memory space when the ST6 is operating due to user software. In addition the ST6 has a stack space for the 12 bit program counter but this is controlled by internal programming and is not accessible by the user. This section will describe all the addressing modes which are provided to the user. The following is the complete list of the ST6 available addressing modes:

- Inherent
- Direct
- Short Direct
- Indirect
- Immediate
- Program Counter Relative
- Extended
- Bit Direct
- Bit Test & Branch

Inherent. For instructions using the inherent addressing mode the opcode contains all the information necessary for execution. All instructions using this mode are **One Byte** instructions.

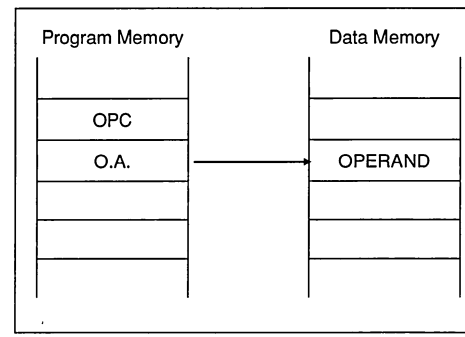


OPC = Opcode

Example:

Instruction	Comments
WAIT	Puts ST6 into the low power WAIT mode
STOP	Puts the ST6 into the lowest power mode
RETI	Returns from interrupt. Pops the PC from the PC stack.Sets the normal set of flags

Direct. In the direct addressing mode the address of the data is given by the program memory byte immediately following the opcode. This data location is in the data memory space. All instructions using this mode are **Two Bytes** instructions, lasting **Four Cycles**.



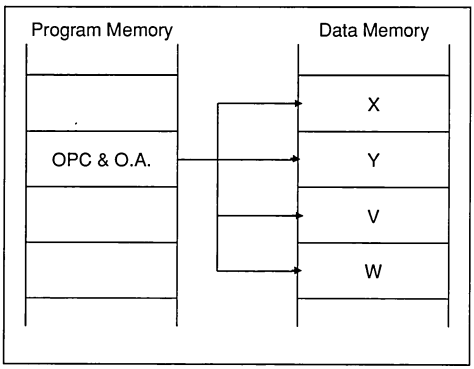
OPC = Opcode
O.A = Operand Address

Example:

Instruction	Comments
LD A,0A3H	Loads the accumulator with the value found in location A3H in the data space.
SUB A,11H	The value found in locations 11H in the data memory is subtracted from the value in the accumulator.

ADDRESSING MODES (Continued)

Short Direct. ST6 core has four fixed location registers in the data space which may be addressed in a short direct manner. The addresses and names of these registers are 80H (X), 81H (Y), 82H (V) and 83H (W). When using this addressing mode the data is in one of these registers and the address is a part of the opcode. All instructions using this mode are **One Byte** instructions, lasting **Four Cycles.**

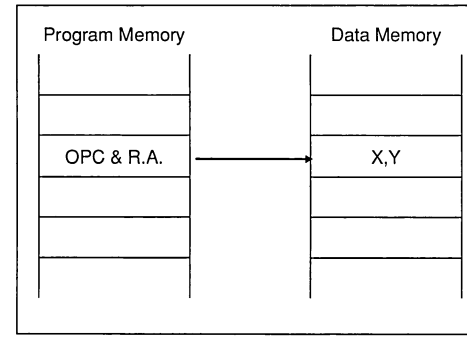


OPC = Opcode
O.A .= Operand Address

Example:

Instruction	Comments
LD A,X	The value of the X register (80H) is loaded into the accumulator.
INC X	The X register is incremented.

Indirect. The indirect mode must use either the X (80H) or Y (81H) register. This register contains the address of the data. The operand is at the data space address pointed to by the content of X or Y registers. All instructions using this mode are **One Byte** instructions, lasting **Four Cycles**.

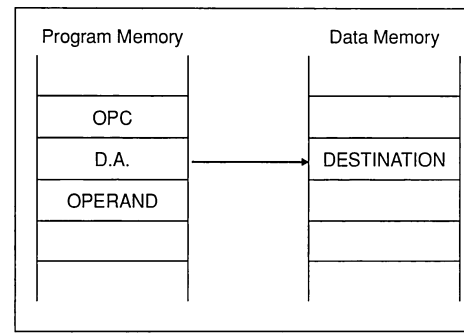


OPC = Opcode
R.A = Register Address

Example:

Instruction	Comments
LD A,(X)	The value in the registers pointed to by the X register is loaded into the accumulator.
ADD A,(Y)	The value in the register pointed to by the Y register is added to the accumulator value.
INC (Y)	The value in the register pointed to by the Y register is incremented.

Immediate. In the immediate addressing mode the operand is found in the program ROM in a byte which is the last byte of the instruction. This addressing mode can be used for initializing data space registers and supplying constants. Instructions using this mode can be **Two** or **Three Bytes** instructions, lasting **Four Cycles**.



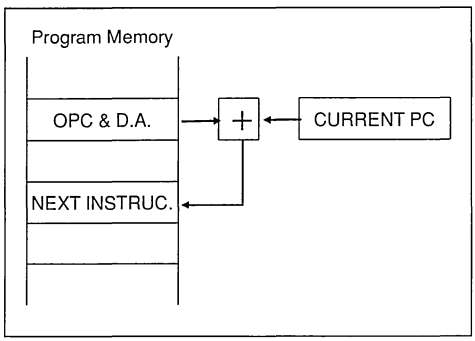
OPC = Opcode
D.A = Destination Address

ADDRESSING MODES (Continued)

Example:

Instruction	Comments
LDI 34H,DFH	Loads immediate value DFH into data space location 34H.
SUBI A,22H	The immediate value 22H is subtracted from the acc.

Program Counter Relative. This addressing mode is used only with conditional branches within the program. The opcode byte contains the data which is a fixed offset value. This offset is added to the program counter to give the address of the next instruction. The offset can have any value in the range -15 to +16. It is determined by the last five bits of the opcode. All instructions using this mode are **One Byte** Instructions, lasting **Two Cycles**.



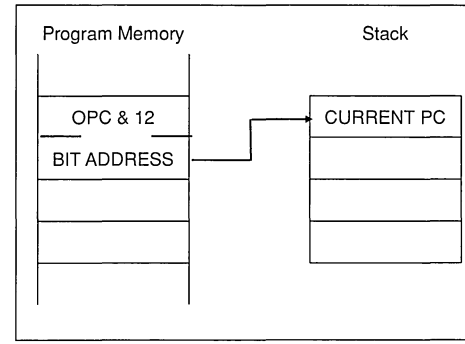
OPC = Opcode
D.A. = Destination Address

Example:

Instruction	Comments
JRC 3	If the carry flag is set then PC = PC+3
JRNZ -7	If the zero flag is not set (i.e the result of a previous instruction is not zero) then PC = PC-7

The relative jump address can be also a label that is automatically handled by the assembler.

Extended. The extended addressing mode is used to make long jumps within the program memory space (4K). The data requires 12 bits and is provided by half of the opcode byte and all of the second byte. All instructions using this mode are **Two Bytes** instructions, lasting **Four Cycles**.



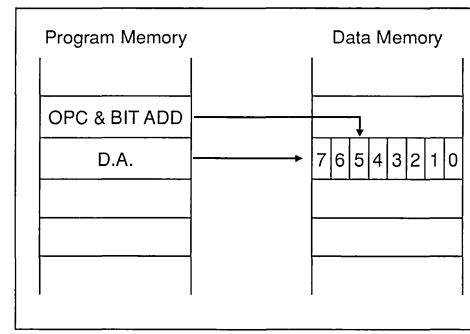
OPC = Opcode

Example:

Instruction	Comments
JP 3FAH	Loads 3FAH into program counter and continues with the instruction at 3FAH.
CALL ROU1	The current PC is pushed onto the stack and PC loaded with the value associated to the ROU1 label

The absolute jump address can be also a label that is automatically handled by the assembler.

Bit Direct. This addressing mode allows the user to set or clear any specified bit in a data memory register. The address of the bit is given in the form: "b,R" where b is the number of the bit and R is the address of the register. The bit is determined by three bits in the opcode and the register address is given by the second byte. All instructions using this mode are **Two Byte** instructions, lasting **Four Cycles**.



OPC = Opcode
D.A = Destination Address

ADDRESSING MODES (Continued)

Example:

Instruction	Comments
SET 4,A	Sets bit 4 of the accumulator to 1.
RES 0,PORT	Clears bit 0 of PORT register

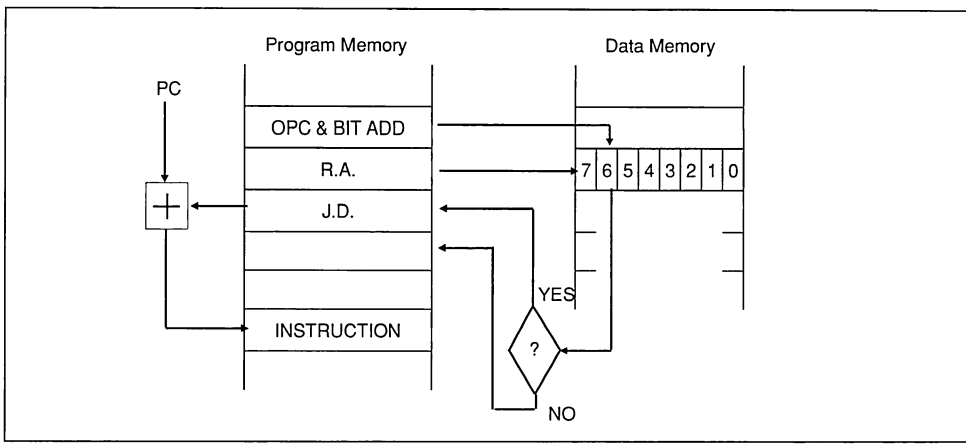
The register address can be associated to a label that is automatically handled by the assembler.

Bit Test & Branch. The bit test addressing mode is used in conditional jump instructions in which the jump depends on the result of a bit test. The opcode specifies the bit to be tested, the byte following the opcode in the register address in data space, and the third byte is the jump displacement, which is in the range -126 to +129. This displacement can be determined using a label, which is converted by the assembler. The state of the tested bit is also copied into the carry flag. All instructions using this mode are **Three Byte** instructions, lasting **Five Cycles**.

Example:

Instruction	Comments
JRS 3,PORT,LAB1	If bit three of data memory register associated to PORT label is set then PC=PC+LAB1 (where LAB1 is the jump displacement associated to a label
JRR 0,0AH,-72	If bit 0 of data memory register OAH is reset to 0 then PC=PC-72.

The register address and the jump displacement can be associated to labels that are automatically handled by the assembler.



OPC = Opcode
R.A. = Relative Address
J.D. = Jump Displacement

ST62 & ST63 INSTRUCTION SET

The ST62,63 instructions can be divided functionally into the following seven groups.

- LOAD AND STORE
- ARITHMETIC AND LOGIC
- CONDITIONAL BRANCH
- JUMP AND CALL
- BIT MANIPULATION
- CONTROL
- IMPLIED

The following summary shows the instructions belonging to each group, the number of operands required for each instructions and the number of machine cycles. The flag behaviour is usually the same for both ST62 and ST63. The only difference is present for CP and SUB instructions as specified in the detailed description.

Table 2. Load & Store Instructions

Instruction	Bytes	Cycles	Flags	
			Z	C
LD	1	4	Δ	*
LD rr	2	4	Δ	*
LDI A	2	4	Δ	*
LDI	3	4	*	*

Notes Δ Affected
*. Not Affected

Table 3. Arithmetic & Logic Instructions

Instruction	Bytes	Cycles	Flags	
			Z	C
ADD	2	4	Δ	Δ
ADD (X,Y)	1	4	Δ	D
ADDI	2	4	Δ	D
AND	2	4	Δ	*
AND (X,Y)	1	4	Δ	*
ANDI	2	4	Δ	*
CLR A	2	4	Δ	D
CLR	3	4	*	*
COM	1	4	Δ	D
CP	2	4	Δ	D
CP (X,Y)	1	4	Δ	D
CPI	2	4	Δ	D
DEC	1	4	Δ	*
DEC A/rr	2	4	Δ	*
INC	1	4	Δ	*
INC A/rr	2	4	Δ	*
RLC	1	4	Δ	D
SLA	2	4	Δ	D
SUB	2	4	Δ	D
SUB (X,Y)	1	4	Δ	D
SUBI	2	4	Δ	D

Notes. Δ. Affected
*: Not Affected

Table 4. Conditional Branch Insructions

Instruction	Bytes	Cycles	Flags	
			Z	C
JRC	1	2	*	*
JRNC	1	2	*	*
JRR	3	5	*	Δ
JRS	3	5	*	Δ
JRZ	1	2	*	*
JRNZ	1	2	*	*

Notes Δ Affected
* Not Affected

Table 5. Jump & Call Instructions

Instruction	Bytes	Cycles	Flags	
			Z	C
CALL	2	4	*	*
JP	2	4	*	*

Notes Δ· Affected
* Not Affected

ST62 & ST63 INSTRUCTION SET (Continued)

Table 6. Bit Manipulation Instructions

Instruction	Bytes	Cycles	Flags	
			Z	C
RES	2	4	*	*
SET	2	4	*	*

Notes Δ Affected
*. Not Affected

Table 7. Control Instructions

Instruction	Bytes	Cycles	Flags	
			Z	C
NOP	1	2	*	*
RET	1	2	*	*
RETI	1	2	Δ	Δ
STOP	1	2	*	*
WAIT	1	2	*	*

Notes Δ Affected
* Not Affected

Table 8. Addressing Modes/Instruction Table

Instruction	Inh	Dir	Sh Dir	Ind	Imm	PCR	Ext	Bit Dir	Bit Test	Flags	
										Z	C
ADD		X	X	X						Δ	Δ
AND		X	X	X						Δ	*
CALL							X			*	*
CLR A		X								Δ	D
CLR		X								*	*
COM	X									Δ	Δ
CP		X		X	X					Δ	Δ
DEC		X	X	X						Δ	*
INC		X	X	X						Δ	*
JP							X			*	*
JRC, JRNC						X				*	*
JRZ, JRNZ						X				*	*
JRR, JRS									X	*	Δ
LD, LDI					X					Δ	*
NOP						X				*	*
RES, SET								X		*	*
RET	X									*	*
RETI	X									Δ	Δ
RLC	X									Δ	Δ
SLA	X									Δ	Δ
STOP, WAIT	X									*	*
SUB		X		X	X					Δ	Δ

Notes:
INH. Inherent, DIR· Direct, SH.DIR. Short Direct,
IND. Indirect, IMM Immediate, PCR. Program Counter Relative
EXT Extended, BIT DIR Bit Direct, BIT TEST.· Bit Test
Δ Affected
* . Not Affected

ST62 & ST63 INSTRUCTION SET (Continued)

Table 9. ST62,63 Opcode Map

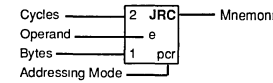
Low / Hi	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Low / Hi
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 pcr	4 LD a,(y) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 pcr	4 LD a,rr 2 dir	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b d	2 JRZ e 1 pcr	4 COM a 1 inh	2 JRC e 1 pcr	4 CP a,(y) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b d	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 pcr	4 CP a,rr 2 dir	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 ADD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 pcr	4 ADD a,(y) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 pcr	4 ADD a,rr 2 dir	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 INC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 pcr	4 INC (y) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 pcr	4 INC rr 2 dir	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD (x),a 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b d	2 JRZ e 1 pcr	# 	2 JRC e 1 pcr	4 LD (y),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 pcr	4 LD rr,a 2 dir	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 AND a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b d	2 JRZ e 1 pcr	4 RLC a 1 inh	2 JRC e 1 pcr	4 AND a,(y) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 pcr	4 AND a,rr 2 dir	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 SUB a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 pcr	4 SUB a,(y) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 pcr	4 SUB a,rr 2 dir	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 DEC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 pcr	4 DEC (y) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 pcr	4 DEC rr 2 dir	F 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement



ST62 & ST63 INSTRUCTION SET (Continued)

Table 10. Instruction Set Cycle-by-Cycle Summary

Instruction	Cycles	Cycles(#)	Address Bus	Data Bus	CPU Activity	Notes
Indirect Addressing Mode						
ADD, AND, CP, DEC, INC, LD, SUB	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Opcode Address +1	Opcode (*) Next Instruction Next Instruction Next Instruction	Decode Opcode Read Operand Address Read Operand Execute Instruction	ROM Data Space not Addressed
ADD, AND, CP, DEC, INC, LD, SUB	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Data Space Rom Add	Opcode (*) Next Instruction Next Instruction Rom Data (#)	Decode Opcode Read Operand Address Read Operand Execute Instruction	ROM Data Space Addressed
Direct Addressing Mode						
ADD, AND, CP, DEC, INC, LD, RES, SET, LSA, SUB, CLR	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 (*) Opcode Address +2	Opcode (*) Operand Address Operand Address(*) Next Instruction	Decode Opcode Address Data Space Read Operand Execute Instruction	ROM Data Space not Addressed
ADD, AND, CP, DEC, INC, LD, RES, SET, LSA, SUB, CLR	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 (*) Data Space Rom Add (*)	Opcode (*) Operand Address Operand Address(#) Rom Data (#)	Decode Opcode Address Data Space Read Operand Execute Instruction	ROM Data Space Addressed
Immediate Addressing Mode						
ADDI, ANDI, CPI, LDI, SUBI	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1(*) Opcode Address +2(*)	Opcode (*) Immediate Operand Immediate Operand Next Instruction	Decode Opcode Idle Read Operand Execute Instruction	
LDI rr	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +2 Opcode AdDress +3	Opcode (*) Register Address Immediate Operand Next Opcode	Decode Opcode Read Register Address Read Immediate Operand Write Operand To Reg	ROM Data Space not Addressed
LDI rr	4	1 2 3 4	Opcode Address(*) Opcode Address +1 (*) Opcode Address +2 (#) Data Space Rom Add	Opcode (*) Register Address Immediate Operand Rom Operand (#)	Decode Opcode Read Register Address Read Immediate Operand Write Operand To Reg.	ROM Data Space Addressed
Short Direct Addressing Mode						
DEC, INC, LD	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Opcode Address +1	Opcode (*) Next Opcode Next Opcode Next Opcode	Decode Opcode Define Data Space Add. Read Operand Execute Instruction	

Notes: *. Valid only at the beginning of the cycle

#. Valid only until 18 of the cycle

ST62 & ST63 INSTRUCTION SET (Continued)

Table 10. Instruction Set Cycle-by-Cycle Summary (Continued)

Instruction	Cycles	Cycles(#)	Address Bus	Data Bus	CPU Activity	Notes
Other Instructions						
CALL	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Opcode Address +2(*)	Opcode (*) Subroutine Address Subroutine Address Next Instruction	Decode Opcode Increment Stack Pointer Push Return Address Calculate Subroutine Add	
COM	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Opcode Address +1	Opcode (*) Next Opcode Next Opcode Next Opcode	Decode Opcode Calculate Acc Address Read Accumulator Complement Accumulator	
INTERRUPT .	1	1	Next opcode address	Next Opcode (*)	Calculate Interrupt Add. Push Return Address Switch Flag Set	Note 1
JP	4	1 2 3 4	Opcode Address(*) opcode Address +1 opcode Address +1 opcode Address +2	Opcode (*) Jump Address Following Instr. Following Instr (*)	Decode Opcode Idle Read Jump Address Calculate Jump Address	
JRC, JRNC, JRZ, JRNZ	2	1 2	Opcode Address(*) Opcode Address +1	Opcode (*) Following Instr.	Decode Opcode Calculate Offset	
JRR, JRS	5	1 2 3 4 5	Opcode Address(*) Opcode Address +1(*) Opcode Address +2(*) Opcode Address +2(*) Opcode Address +3(*)	Opcode (*) Operand Address (*) Branch Value Branch Value (*) Following Instr.	Decode Opcode Read Operand Test Operand Fetch Branch Value Calculate New Address	ROM Data Space not Addressed
JRR, JRS	5	1 2 3 4 5	Opcode Address(*) Opcode Address +1(*) Data Space Rom Add (#) Opcode Address +2(*) Data Space Rom Add.(#)	Opcode (*) Operand Address (*) Rom Data (#) Branch Value (*) Rom Data (#)	Decode Opcode Read Operand Test Operand Fetch Branch Value Calculate New Address	ROM Data Space Addressed
RET	2	1 2	Opcode Address(*) Return Address	Opcode (*) Next Opcode	Decode Opcode Pop Return Address	
RETI	2	1 2	Opcode Address(*) Return Address	Opcode (*) Next Opcode	Decode Opcode Pop Return Address Switch Flag Set	
RLC	4	1 2 3 4	Opcode Address(*) Opcode Address +1 Opcode Address +1 Opcode Address +1	Opcode (*) Next Opcode Next Opcode Next Opcode	Decode Opcode Calculate Acc. Address Read Accumulator Shifted	
STOP, WAIT	2	1 2	Opcode Address(*) Opcode Address +1	Opcode (*) Next Opcode	Decode Opcode Stop/Wait the Oscillator	

Notes: *. Valid only at the beginning of the cycle
#. Valid only until t18 of the cycle

1. Add oscillator build up time plus 16 oscillator clocks if a stop instruction has been executed before the interrupt occured

ADD

Addition

Mnemonic: ADD

Function: Addition

Description: The contents of the source byte is added to the accumulator leaving the result in the accumulator. The source register remains unaltered.

Operation: dst ← dst + src

The destination must be the accumulator.

Instruction Format	Opcode (Hex)	Bytes	Cycles	Flags	
ADD dst,src				Z	C
ADD A,A	5F FF	2	4	Δ	Δ
ADD A,X	5F 80	2	4	Δ	D
ADD A,Y	5F 81	2	4	Δ	D
ADD A,V	5F 82	2	4	Δ	D
ADD A,W	5F 83	2	4	Δ	D
ADD A,(X)	47	1	4	Δ	D
ADD A,(Y)	4F	1	4	Δ	D
ADD A,rr	5F rr	2	4	Δ	D

Notes:
rr. 1 Byte dataspace address.
Δ: Z is set if the result is zero. Cleared otherwise.
C is cleared before the operation and than set if there is an overflow from the 8-bit result.

Example: If data space register 22H contains the value 33H and the accumulator holds the value 20H then the instruction,

ADD A,22H

will cause the accumulator to hold 53H (i.e. 33+20).

Addressing Modes: Source: Direct, Indirect

Destination: Accumulator

ADDI

Addition Immediate

Mnemonic: ADDI

Function: Addition Immediate

Description: The immediately addressed data (source) is added to the accumulator leaving the result in the accumulator.

Operation: dst ← dst + src

The destination must be the accumulator.

Instruction Format	Opcode (Hex)	Bytes	Cycles	Flags	
ADDI dst,src				Z	C
ADDI A,nn	57 nn	2	4	Δ	Δ

Notes:
nn 1 Byte immediate data
Δ· Z is set if result is zero Cleared otherwise
C is cleared before the operation and than set if there is an overflow from the 8-bit result

Example: If the accumulator holds the value 20H then the instruction,

ADDI A,22H

will cause the accumulator to hold 42H (i.e. 22+20).

Addressing Modes: Source: Immediate
Destination: Accumulator

AND

Logical AND

Mnemonic: AND

Function: Logical AND

Description: This instruction logically ANDs the source register and the accumulator. The result is left in the destination register and the source is unaltered.

Operation: dst ←src AND dst

The destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
AND dst,src				Z	C
AND A,A	BF FF	2	4	Δ	*
AND A,X	BF 80	2	4	Δ	*
AND A,Y	BF 81	2	4	Δ	*
AND A,V	BF 82	2	4	Δ	*
AND A,W	BF 83	2	4	Δ	*
AND A,(X)	A7	1	4	Δ	*
AND A,(Y)	AF	1	4	Δ	*
AND A,rr	BF rr	2	4	Δ	*

Notes:
rr. 1 Byte dataspace address
*. C is unaffected
Δ Z is set if the result is zero. Cleared otherwise.

Example: If data space register 54H contains the binary value 11110000 and the accumulator contains the binary value 11001100 then the instruction,

AND A,54H

will cause the accumulator to be altered to 11000000.

Addressing Modes: Source: Direct, Indirect.
Destination: Accumulator

ANDI

Logical AND Immediate

Mnemonic: ANDI

Function: Logical AND Immediate

Description: This instruction logically ANDs the immediate data byte and the accumulator. The result is left in the accumulator.

Operation: dst ← src AND dst

The source is immediate data and the destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
ANDI dst,src				Z	C
ANDI A,nn	B7 nn	2	4	Δ	*

Notes:
nn. 1 Byte immediate data
*. C is unaffected
Δ. Z is set if the result is zero Cleared otherwise.

Example: If the accumulator contains the binary value 00001111 then the instruction,

ANDI A,33H

will cause the accumulator to hold the value 00000011.

Addressing Modes: Source: Immediate
Destination: Accumulator

CALL

Call Subroutine

Mnemonic: CALL

Function: Call Subroutine

Description: The CALL instruction is used to call a subroutine. It "pushes" the current contents of the program counter (PC) onto the top of the stack. The specified destination address is then loaded into the PC and points to the first instruction of a procedure. At the end of the procedure a RETurn instruction can be used to return to the original program flow. RET pops the top of the stack back into the PC. Because the ST6 stack is 4 levels deep (ST60) and 6 levels deep (ST62,ST63), a maximum of four/six calls or interrupts may be nested. If more calls are nested, the PC values stacked latest will be lost. In this case returns will return to the PC values stacked first.

Operation: PC ← dst; Top of stack ← PC

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
CALL dst					
CALL abc	c0001 ab	2	4	*	*

Notes:
abc. the three half bytes of a twelve bit address, the start location of the subroutine.
*. C,Z not affected

Example: If the current PC is 345H then the instruction,

CALL 8DCH

The current PC 345H is pushed onto the top of the stack and the PC will be loaded with the value 8DCH. The next instruction to be executed will be the instruction at 8DCH, the first instruction of the called subroutine.

Addressing Modes: Extended

CLR

Clear

Mnemonic: CLR

Function: Clear

Description: The destination register is cleared to 00H.

Operation: dst ← 0

Inst. Format	OPCDE (Hex)	Bytes	Cycles	Flags	
CLR dst				Z	C
CLR A	DF FF	2	4	Δ	Δ
CLR X	0D 80 00	3	4	*	*
CLR Y	0D 81 00	3	4	*	*
CLR V	0D 82 00	3	4	*	*
CLR W	0D 83 00	3	4	*	*
CLR rr	0D rr 00	3	4	*	*

Notes:
rr. 1 Byte dataspace address
Δ. C,Z set
*. C,Z unaffected

Example: If data space register 22H contains the value 33H,
CLR 22H
will cause register 22H to hold 00H.

Addressing Modes: Direct

COM

Complement

Mnemonic: COM

Function: Complement

Description: This instruction complements each bit of the accumulator; all bits which are set to 1 are cleared to 0 and vice-versa.

Operation: dst ← NOT dst

The destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
COM dst				Z	C
COM A	2D	1	4	Δ	Δ

Note :
Δ: Z is set if the result is zero. Cleared otherwise.
C will contain the value of the MSB before the operation.

Example: If the accumulator contains the binary value 10111001 then the instruction

COM A

will cause the accumulator to be changed to 01000110 and the carry flag to be set (since the original MSB was 1).

Addressing Modes: Inherent

CP

Compare

Mnemonic: CP

Function: Compare

Description: This instruction compares the source byte (subtracted from) with the destination byte, which must be the accumulator. The carry and zero flags record the result of this comparison.

Operation: dst - src

The destination must be the accumulator, but it will not be changed.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
CP dst,src				Z	C
CP A,A	3F FF	2	4	Δ	Δ
CP A,X	3F 80	2	4	Δ	Δ
CP A,Y	3F 81	2	4	Δ	Δ
CP A,V	3F 82	2	4	Δ	Δ
CP A,W	3F 83	2	4	Δ	Δ
CP A,(X)	27	1	4	Δ	Δ
CP A,(Y)	2F	1	4	Δ	Δ
CP A,rr	3F rr	2	4	Δ	Δ

Note: rr. 1 Byte dataspace address

ST60 Δ: Z is set if the result is zero. Cleared otherwise.

C is set if Acc ≥ src, cleared if Acc < src.

ST62/63 Δ: Z is set if the result is zero. Cleared otehrwise.

C is set if Acc < src, cleared if Acc ≥ src.

Example: If the accumulator contains the value 11111000 and the register 34H contains the value 00011100 then the instruction,

CP A,34H

will clear the Zero flag Z and set the Carry flag C, indicating that Acc ≥ src (on ST60)

Addressing Modes: Source: Direct, Indirect

Destination: Accumulator

CPI

Compare Immediate

Mnemonic: CPI

Function: Compare Immediate

Description: This instruction compares the immediately addressed source byte (subtracted from) with the destination byte, which must be the accumulator. The carry and zero flags record the result of this comparison.

Operation: dst-src

The source must be the immediately addressed data and the destination must be the accumulator, that will not be changed.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
CPI dst,src				Z	C
CPI A,nn	37 nn	2	4	Δ	Δ

Note: nn.1 Byte immediate data

ST60 Δ: Z is set if the result is zero. Cleared otherwise.
C is set if Acc ≥ src, cleared if Acc < src.

ST62/63 Δ: Z is set if the result is zero. Cleared otherwise.
C is set if Acc < src, cleared if Acc ≥ src.

Example: If the accumulator contains the value 11111000 then the instruction,
CPI A,00011100B
will clear the Zero flag Z and set the Carry flag C indicating that Acc ≥ src (on ST60).

Addressing Modes: Source: Immediate
Destination: Accumulator

DEC

Decrement

Mnemonica: DEC

Function: Decrement

Description: The destination register's contents are decremented by one.

Operation: dst ← dst-1

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
DEC dst				Z	C
DEC A	FF FF	2	4	Δ	*
DEC X	1D	1	4	Δ	*
DEC Y	5D	1	4	Δ	*
DEC V	9D	1	4	Δ	*
DEC W	DD	1	4	Δ	*
DEC (X)	E7	1	4	Δ	*
DEC (Y)	EF	1	4	Δ	*
DEC rr	FF rr	2	4	Δ	*

Notes:
rr. 1 Byte dataspace address
*. C is unaffected
Δ. Z is set if the result is zero. Cleared otherwise.

Example: If the X register contains the value 45H and the data space register 45H contains the value 16H then the instruction,

DEC (X)

will cause data space register 45H to contain the value 15H.

Addressing Modes: Short direct, Direct, Indirect.

INC

Increment

Mnemonic: INC

Function: Increment

Description: The destination register's contents are incremented by one.

Operation: dst ← dst+1

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
INC dst				Z	C
INC A	7F FF	2	4	Δ	*
INC X	15	1	4	Δ	*
INC Y	55	1	4	Δ	*
INC V	95	1	4	Δ	*
INC W	D5	1	4	Δ	*
INC (X)	67	1	4	Δ	*
INC (Y)	6F	1	4	Δ	*
INC rr	7F rr	2	4	Δ	*

Notes:
rr. 1 Byte dataspace address
*. C is unaffected
Δ. Z is set if the result is zero. Cleared otherwise.

Example: If the X register contains the value 45H and the data space register 45H contains the value 16H then the instruction

INC (X)

will cause data space register 45H to contain the value 17H.

Addressing Modes: Short direct, Direct, Indirect.

JP

Jump

Mnemonic: JP

Function: Jump (Unconditional)

Description: The JP instruction replaces the PC value with a twelve bit value thus causing a simple jump to another location in the program memory. The previous PC value is lost, not stacked.

Operation: PC ← dst

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JP dst					
JP abc	c1001 ab	2	4	*	*

Notes:
abc. the three half bytes of a twelve bit address.
*. C,Z not affected

Example: The instruction,

JP 5CDH

will cause the PC to be loaded with 5CDH and the program will continue from that location.

Addressing Modes: Extended

JRC

Jump Relative on Carry Flag

Mnemonic: JRC

Function: Jump Relative on Carry Flag

Description: This instruction causes the carry (C) flag to be tested and if this flag is set then a jump is performed within the program memory. This jump is in the range -15 to +16 and is relative to the PC value. The displacemente is of five bits. If C=0 than the next instruction is executed.

Operation: If C=1, PC ← PC + e
where e= 5 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRC e	e110	1	2	*	*

Notes:
e 5 bit displacement in the range –15 to + 16
* C,Z not affected

Example: If the carry flag is set then the instruction,

JRC + 8

will cause a branch forward to PC+8. The user can use labels as indentifiers and the assembler will automatically allow the jump if it is in the range -15 to +16.

Addressing Modes: Program Counter Relative

JRNC

Jump Relative on Non Carry Flag

Mnemonic: JRNC

Function: Jump Relative on Non Carry Flag

Description: This instruction causes the carry (C) flag to be tested and if this flag is cleared to zero then a jump is performed within the program memory. This jump is in the range -15 to +16 and is relative to the PC value. The dispacement is of five bits. If C=1 then the next instruction is executed.

Operation: If C=0, PC ← PC + e
where e= 5 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRNC e	e010	1	2	*	*

Notes:
e: 5 bit displacement in the range -15 to +16
*: C,Z not affected

Example: If the carry flag is cleared then the instruction,
JRNC -5
will cause a branch backward to PC-5. The user can use labels as identifiers and the assembler will automatically allow the jump if it is in the range -15 to +16.

Addressing Modes: Program Counter Relative

JRNZ

Jump Relative on Non Zero Flag

Mnemonic: JRNZ

Function: Jump Relative on Non Zero Flag

Description: This instruction causes the zero (Z) flag to be tested and if this flag is cleared to zero then a jump is performed within the program memory. This jump is in the range -15 to +16 and is relative to the PC value. The displacement is of five bits. If Z=1 then the next instruction is executed.

Operation: If Z=0, PC ← PC + e

where e= 5 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRNZ e	e000	1	2	*	*

Notes:
e. 5 bit displacement in the range -15 to +16.
* C,Z not affected

Example: If the zero flag is cleared then the instruction,

JRNZ -5

will cause a branch backward to PC-5. The user can use labels as identifiers and the assembler will automatically allow the jump if it is in the range -15 to +16.

Addressing Modes: Program Counter Relative

JRR

Jump Relative if Reset

Mnemonic: JRR

Function: Jump Relative if RESET

Description: This instruction causes a specified bit in a given dataspace register to be tested. If this bit is reset (=0) then the PC value will be changed and a relative jump will be performed within the program. The relative jump range is -126 to +129. If the tested bit is not reset then the next instruction is executed.

Operation: If bit=0, PC ← PC + ee

where ee= 8 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRR b,rr,ee	b00011 rr ee	3	5	*	Δ

Notes:
b 3 bit-address
rr 1 Byte dataspace address
ee 8 bit displacement in the range -126 to +129

* Z is not affected
Δ The tested bit is shifted into carry

Example: If bit 4 of dataspace register 70H is reset and the PC=110 then the instruction,

JRR 4, 70H, -20

will cause the PC to be changed to 90 (110-20) and the instruction starting at that address in the program memory to be the next instruction executed.

The user is advised to use labels for conditional jumps. The relative jump will be calculated by the assembler. The jump must be in the range -126 to +129.

Addressing Modes: Bit Test

JRS

Jump Relative if Set

Mnemonic: JRS

Function: Jump Relative if set

Description: This instruction causes a specified bit in a given dataspace register to be tested. If this bit is set (=1) then the PC value will be changed and a relative jump will be performed within the program. The relative jump range is -126 to +129. If the tested bit is not set then the next instruction is executed.

Operation: If bit=1, PC ← PC + ee

where ee= 8 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRS b,rr,ee	b10011 rr ee	3	5	*	Δ

Notes:
b 3 bit-address
rr. 1 Byte dataspace address
ee 8 bit displacement in the range -126 to +129

* Z is not affected
Δ The tested bit is shifted into carry.

Example: If bit 7 of dataspace register AFH is set and the PC=123 then the instruction,

JRS 7,AFH,+25

will cause the PC to be changed to 148 (123+25) and the instruction starting at that address in the program memory to be the next instruction executed.

The user is advised to use labels for conditional jumps. The relative jump will be calculated by the assembler. The jump must be in the range -126 to +129.

Addressing Modes: Bit Test

JRZ

Jump Relative on Zero Flag

Mnemonic: JRZ

Function: Jump Relative on Zero Flag

Description: This instruction causes the zero (Z) flag to be tested and if this flag is set to one then a jump is performed within the program memory. This jump is in the range -15 to +16 and is relative to the PC value. The displacement is of five bits. If Z=0 then next instruction is executed.

Operation: If Z=1, PC ← PC + e

where e= 5 bit displacement

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
JRZ e	e100	1	2	*	*

Notes:
e. 5 bit displacement in the range -15 to +16.
*. C,Z not affected

Example: If the zero flag is set then the instruction,

JRZ +8

will cause a branch forward to PC+8. The user can use labels as identifiers and the assembler will automatically allow the jump if it is in the range -15 to +16.

Addressing Modes: Program Counter Relative

LD

Load

Mnemonic: LD

Function: Load

Description: The contents of the source register are loaded into the destination register. The source register remains unaltered and the previous contents of the destination register are lost.

Operation: dst ← src

Either the source or the destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
LD dst,src				Z	C
LD A,X	35	1	4	Δ	*
LD A,Y	75	1	4	Δ	*
LD A,V	B5	1	4	Δ	*
LD A,W	F5	1	4	Δ	*
LD X,A	3D	1	4	Δ	*
LD Y,A	7D	1	4	Δ	*
LD V,A	BD	1	4	Δ	*
LD W,A	FD	1	4	Δ	*
LD A,(X)	07	1	4	Δ	*
LD (X), A	87	1	4	Δ	*
LD A,(Y)	0F	1	4	Δ	*
LD (Y),A	8F	1	4	Δ	*
LD A,rr	1F rr	2	4	Δ	*
LD rr,A	9F rr	2	4	Δ	*

Notes:
rr. 1 Byte dataspace address
*. C not affected
Δ. Z is set if the result is zero. Cleared otherwise.

Example: If data space register 34H contains the value 45H then the instruction;

LD A,34H

will cause the accumulator to be loaded with the value 45H. Register 34H will keep the value 45H.

Addressing Modes: Source: Direct, Short Direct, Indirect

Destination: Direct, Short Direct, Indirect

LDI

Load Immediate

Mnemonic: LDI

Function: Load Immediate

Description: The immediately addressed data (source) is loaded into the destination data space register.

Operation: dst ← src

The source is always an immediate data while the destination can be the accumulator, one of the X,Y,V,W registers or one of the available data space registers.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
LDI dst,src				Z	C
LDI A,nn	17 nn	2	4	Δ	*
LDI X,nn	0D 80 nn	3	4	*	*
LDI Y,nn	0D 81 nn	3	4	*	*
LDI V,nn	0D 82 nn	3	4	*	*
LDI W,nn	0D 83 nn	3	4	*	*
LDI rr,nn	0D rr nn	3	4	*	*

Notes:
rr. 1 Byte dataspace address
nn. 1 Byte immediate value

*. Z, C not affected
Δ. Z is set if the result is zero. Cleared otherwise.

Example: The instruction

LDI 34H,45H

will cause the value 45H to be loaded into data register at location 34H.

Addressing Modes: Source: Immediate
Destination: Direct

NOP

No Operation

Mnemonic: NOP

Function: No Operation

Description: No action is performed by this instruction. It is typically used for timing delay.

Operation: No Operation

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
NOP	04	1	2	*	*

Note: *. C,Z not affected

Addressing Modes: Program Counter Relative

RES

Reset Bit

Mnemonic: RES

Function: Reset Bit

Description: The RESET instruction is used to reset a specified bit in a given register in the data space.

Operation: dst (n) ← 0, 0 ≤ n ≤ 7

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
RES bit,dst				Z	C
RES b,A	b01011 FF	2	4	*	*
RES b,rr	b01011 rr	2	4	*	*

Notes:
b. 3 bit-address
rr. 1 Byte dataspace address
*. C,Z not affected

Example: If register 23H of the dataspace contains 11111111 then the instruction,
RES 4,23H
will cause register 23H to hold 11101111.

Addressing Modes: Bit Direct

RET

Return from Subroutine

Mnemonic: RET

Function: Return From Subroutine

Description: This instruction is normally used at the end of a subroutine to return to the previously executed procedure. The previously stacked program counter (stacked during CALL) is popped back from the stack. The next statement executed is that addressed by the new contents of the PC. If the stack had already reached its highest level (no more PC stacked) before the RET is executed, program execution will be continued at the next instruction after the RET.

Operation: PC ← Stacked PC

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
RET	CD	1	2	*	*

Note: *. C,Z not affected

Example: If the current PC value is 456H and the PC value at the top of the stack is 3DFH then the instruction,

RET

will cause the PC value 456H to be lost and the current PC value to be 3DFH.

Addressing Modes: Inherent

RETI

Return from Interrupt

Mnemonic: RETI

Function: Return from Interrupt

Description: This instruction marks the end of the interrupt service routine and returns the ST60/62/63 to the state it was in before the interrupt. It "pops" the top (last in) PC value from the stack into the current PC. This instruction also causes the ST60/62/63 to switch from the interrupt flags to the normal flags. The RETI instruction also applies to the end of NMI routine for ST62/63 devices; in this case the instruction causes the switch from NMI flags to normal flags (if NMI was acknowledged inside a normal routine) or to standard interrupt flags (if NMI was acknowledged inside a standard interrupt service routine).

In addition the RETI instruction also clears the interrupt mask (also NMI mask for ST62/63) which was set when the interrupt occurred. If the stack had already reached its highest level (no more PC stacked) before the RETI is executed, program execution will be continued with the next instruction after the RETI. Because the ST60 is in interrupt mode after reset (NMI mode for ST62/63), RETI has to be executed to switch to normal flags and enable interrupts at the end of the starting routine. If no call was executed during the starting routine, program execution will continue with the instruction after the RETI (supposed no interrupt is active).

Operation: Actual Flags ← Normal Flags (1)

PC ← Stacked PC

IM ← 0

(1) Standard Interrupt flags if NMI was acknowledged inside a standard interrupt service (ST62/63 only).

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
RETI	4D	1	2	Δ	Δ

Note: Δ C,Z normal flag will be used from now on.

Example: If the current PC value is 456H and the PC value at the top of the stack is 3DFH then the instruction

RETI

will cause the value 456H to be lost and the current PC value to be 3DFH. The ST6 will switch from interrupt flags to normal flags and the interrupt mask is cleared.

Addressing Modes: Inherent

RLC

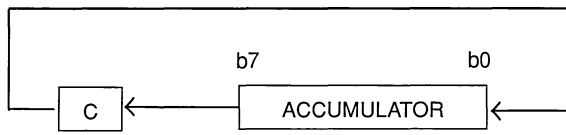
Rotate Left Through Carry

Mnemonic: RLC

Function: Rotate Left through Carry

Description: This instruction moves each bit in the accumulator one place to the left (i.e. towards the MSBit. The MSBit (bit 7) is moved into the carry flag and the carry flag is moved into the LSBit (bit0) of the accumulator.

Operation:



dst(0) ← C

C ←dst(7)

dst(n+1) ← dst(n), 0 ≤ n ≤ 6

This instruction can only be performed on the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
RLC A	AD	1	4	Δ	Δ

Note : Δ: Z is set if the result is zero. Cleared otherwise.
C will contain the value of the MSB before the operation.

Example: If the accumulator contains the binary value 10001001 and the carry flag is set to 0 then the instruction,

RLC A

will cause the accumulator to have the binary value 00010010 and the carry flag to be set to 1.

Addressing Modes: Inherent

SET

Set Bit

Mnemonic: SET

Function: Set Bit

Description: The SET instruction is used to set a specified bit in a given register in the data space.

Operation: dst (n) ← 1, $0 \leq n \leq 7$

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
SET bit,dst				Z	C
SET b,A	b11011 FF	2	4	*	*
SET b,rr	b11011 rr	2	4	*	*

Notes:
b. 3 bit-address
rr. 1 Byte dataspace address
*. C,Z not affected

Example: If register 23H of the dataspace contains 00000000 then the instruction,
SET 4,23H
will cause register 23H to hold 00010000.

Addressing Modes: Bit Direct

SLA

Shift Left Accumulator

Mnemonic: SLA

Function: Shift Left Accumulator

Description: This instruction implements an addition of the accumulator to itself (i.e a doubling of the accumulator) causing an arithmetic left shift of the value in the register.

Operation: ADD A,FFH

This instruction can only be performed on the accumulator.

Inst. Format	OPCPDE (Hex)	Bytes	Cycles	Flags	
				Z	C
SLA A	5F FF	2	4	Δ	Δ

Note: Δ· Z is set if the result is zero Cleared otherwise
C will contain the value of the MSB before the operation

Example: If the accumulator contains the binary value 11001101 then the instruction,

SLA A

will cause the accumulator to have the binary value 10011010 and the carry flag to be set to 1.

Addressing Modes: Inherent

STOP

Stop Operation

Mnemonic: STOP

Function: Stop operation

Description: This instruction is used for putting the ST60/62/63 into a stand-by mode in which the power consumption is reduced to a minimum. All the on-chip peripherals and oscillator are stopped (for some peripherals,A/D for example, it is necessary to individually turn-off the macrocell before entering the STOP instruction). To restart the processor an external interrupt or a reset is needed.

Operation: Stop Processor

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
STOP	6D	1	2	*	*

Note : *: C,Z not affected

Addressing Mode: Inherent

SUB

Subtraction

Mnemonic: SUB

Function: Subtraction

Description: This instruction subtracts the source value from the destination value.

Operation: dst ←dst-src

The destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
SUB dst,src				Z	C
SUB A,A	DF FF	2	4	Δ	Δ
SUB A,X	DF 80	2	4	Δ	Δ
SUB A,Y	DF 81	2	4	Δ	Δ
SUB A,V	DF 82	2	4	Δ	Δ
SUB A,W	DF 83	2	4	Δ	Δ
SUB A,(X)	C7	1	4	Δ	Δ
SUB A,(Y)	CF	1	4	Δ	Δ
SUB A,rr	DF rr	2	4	Δ	Δ

Note: rr.1 Byte dataspace address

ST60 Δ: Z is set if the result is zero. Cleared otherwise.

C is set if Acc ≥ src, cleared if Acc < src.

ST62/63 Δ: Z is set if the result is zero. Cleared otherwise.

C is set if Acc < src, cleared if Acc ≥ src.

Example: If the Y register contains the value 23H, dataspace register 23H contains the value 53H and the accumulator contains the value 78H then the instruction,

SUB A,(Y)

will cause the accumulator to hold the value 25H (i.e. 78-53). The zero flag is cleared and the carry flag is set (on ST60), indicating that result is > 0.

Addressing Modes: Source: Indirect,Direct

Destination: Accumulator

SUBI

Subtraction Immediate

Mnemonic: SUBI

Function: Subtraction Immediate

Description: This instruction causes the immediately addressed source data to be subtracted from the accumulator.

Operation: dst ← dst - src

The destination must be the accumulator.

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
SUBI dst,src				Z	C
SUBI A,nn	D7 nn	2	4	Δ	Δ

Note: nn 1 Byte of immediate data

ST60 Δ: Z is set if the result is zero. Cleared otherwise.
C is set if Acc ≥ src, cleared if Acc < src.

ST62/63 Δ: Z is set if the result is zero. Cleared otherwise.
C is set if Acc < src, cleared if Acc ≥ src.

Example: If the accumulator contains the value 56H then the instruction,

SUBI A,25

will cause the accumulator to contain the value 31H. The zero flag is cleared and the carry flag is set (on ST60), indicating that the result is > 0.

Addressing Modes: Source: Immediate
Destination: Accumulator

WAIT

Wait Processor

Mnemonic: WAIT

Function: Wait Processor

Description: This instruction is used for putting the ST60/62/63 into a stand-by mode in which the power consumption is reduced to a minimum. Instruction execution is stopped, but the oscillator and some on-chip peripherals continue to work. To restart the processor an interrupt from an active on-chip peripheral (eg. timer), an external interrupt or reset is needed. For on-chip peripherals active during wait, see ST60/62/63 data sheets.

Operation: Put ST6 in stand-by mode

Inst. Format	OPCODE (Hex)	Bytes	Cycles	Flags	
				Z	C
WAIT	ED	1	2	*	*

Note : *. C,Z not affected

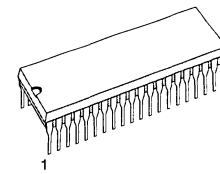
Addressing Modes: Inherent

SGS-THOMSON MICROELECTRONICS

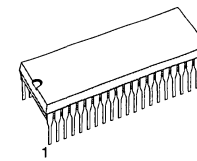
ST6326,ST6327,ST6328 ST6356,ST6357,ST6358

8 BIT HCMOS MCUs FOR TV FREQUENCY & VOLTAGE SYNTHESIS WITH OSD

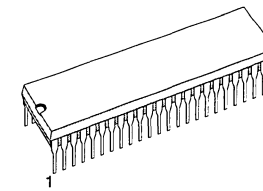
- 8-bit Architecture
- HCMOS Technology
- 8MHz Clock
- User Program ROM: 7948 byte
- Reserved Test ROM: 244 bytes
- Data ROM: User selectable size
- Data RAM: 256 bytes
- Data EEPROM: 128 bytes
- 40-Pin Dual in Line Plastic Package for the ST6326,56
- 42-Pin Shrink Dual in Line Plastic Package for the ST6327,57
- 48-Pin Dual in Line Plastic Package for the ST6328,58
- Up to 18, software programmable general purpose Inputs/Outputs, including up to 8 direct LED driving Outputs
- 3 Inputs for keyboard scan (KBYO-2)
- 4 High voltage outputs (BSWO-3)
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I^2C BUS and standard serial protocols
- 4 6-Bit PWM D/A Converters
- 62.5KHz Output Pin
- AFC A/D converter with 0.5V resolution
- 4 interrupt vectors (IRIN/NMI, Timer 1 & 2, VSYNC)
- 14-bit counter for Voltage Synthesis Tuning (ST6356,57,58)
- On-chip clock oscillator
- 5 Lines by 15 Characters On-Screen Display Generator with 64 Characters
- Byte efficient instruction set
- Bit test and jump instructions
- Wait and Bit Manipulation instructions
- True LIFO 6-level stack
- All ROM types are supported by pin-to-pin piggyback versions.
- The development tool of the ST63 microcontrollers consists of the ST63TVS-EMU emulation and development system to be connected via a standard RS232 serial line to an MS-DOS Personal Computer.



PDIP40



PSDIP42



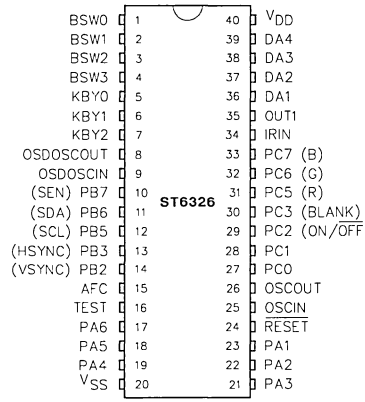
PDIP48

(Ordering Information at the end of the datasheet)

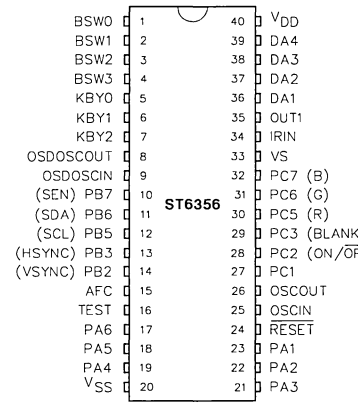
DEVICE SUMMARY

DEVICE	ROM (Bytes)	I/O pins	Package
ST6326	8K	12	PDIP40
ST6327	8K	14	PSDIP42
ST6328	8K	18	PDIP48
ST6356	8K	11	PDIP40
ST6357	8K	13	PSDIP42
ST6358	8K	18	PDIP48

Figures 1, 2. ST6326,56 Pin Configuration

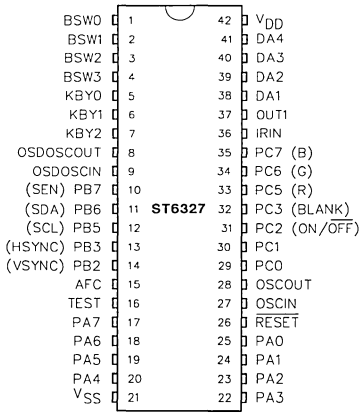


VA00282

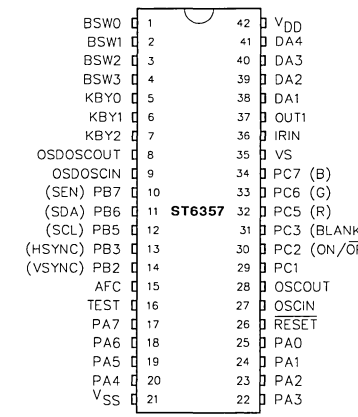


VA00288

Figures 3, 4. ST6327,57 Pin Configuration

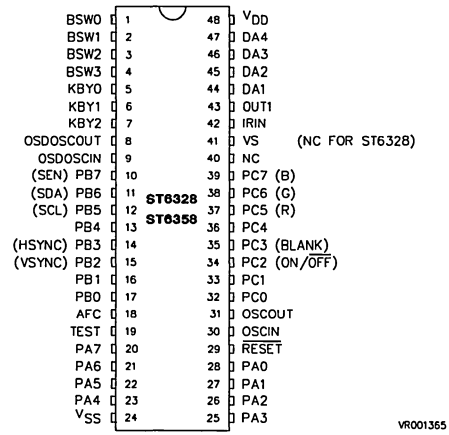


VA00283



VA00289

Figures 5, 6. ST6328,58 Pin Configuration



GENERAL DESCRIPTION

The ST632X,5X microcontrollers are members of the 8-bit HCMOS ST63XX family, a series of devices specially oriented to TV applications. Different pin-out configurations are available to give the maximum application and cost flexibility. All ST63XX members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility and short design time. Many of these macrocells are specially dedicated to TV applications. The macrocells of the ST632X,5X family: two Timer peripherals each including an 8-bit counter with a 7-bit software programmable prescaler (Timer), a digital hardware activated watchdog function (DHWD), a serial peripheral interface (SPI), four 6-bit PWM D/A converters, an AFC A/D converter with 0.5V resolution, a 14-bit Voltage Synthesis tuning peripheral (ST635X only), an on-screen display (OSD) with 15 characters per line, 64 characters. In addition all these devices have 8K of ROM, 256 bytes of data RAM and 128 bytes of EEPROM. Refer to pin configurations figures and to ST632X,5X device summary (Table 1) for the definition of family members and a summary of differences among the different types.

Figure 7. ST632X,5X Block Diagram

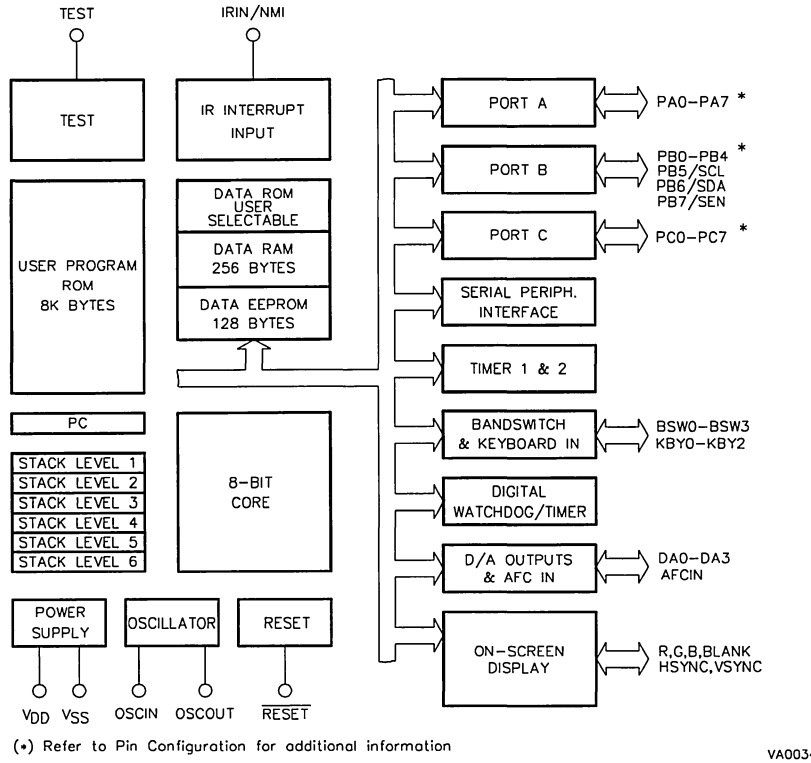


Table 1. ST632X,5X Device Summary

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	I/O	KBY I/O	BSW OUT	AFC	D/A	OSD	PACK-AGE	EMUL. DEVICE
ST6326	8K	256	128	12	3	4	YES	4	YES	PDIP40	ST63P26
ST6327	8K	256	128	14	3	4	YES	4	YES	PSDIP42	ST63P27
ST6328	8K	256	128	18	3	4	YES	4	YES	PDIP48	ST63P28
ST6356	8K	256	128	11	3	4	YES	4	YES	PDIP40	ST63P56
ST6357	8K	256	128	13	3	4	YES	4	YES	PSDIP42	ST63P57
ST6358	8K	256	128	18	3	4	YES	4	YES	PDIP48	ST63P58

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN, OSCOUT. These pins are internally connected to the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The OSCIN pin is the input pin, the OSCOUT pin is the output pin. Refer to ON-CHIP CLOCK OSCILLATOR description for additional information.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to start the microcontroller to the beginning of its program. Refer to RESET description for additional information.

TEST. The TEST (mode select) pin is used to place the MCU into special operating mode. If TEST is held at V_{SS} the MCU enters the normal operating mode. If TEST is held at V_{DD} when $\overline{\text{RESET}}$ is active the test operating mode is automatically selected (the user should connect this pin to V_{SS} for normal operation). Refer to TEST mode description for additional information.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or as an output under software control of the data direction register. Port A has an open-drain (12V drive) output configuration with direct led driving capability (30mA, 1V). Refer to I/O PORT description for additional information.

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register. PB0-PB4 have a push-pull configuration in output mode while PB5-PB7 are open-drain (5V drive). PB2 and PB3 lines are connected to the VSYNC and HSYNC control signals of the OSD cell ; to provide the right signals to the OSD these I/O lines should be programmed in input mode and the user can read "on the fly" the state of VSYNC and HSYNC signals. PB2 is connected with the vertical synchronization signal VSYNC input. The active polarity of this signal is software controlled. PB3 is connected with the horizontal synchronization signal input HSYNC. Oscillator is synchronous with the change to low state. Oscillation stops while signal is in the high state. A ROM mask option is available to change the polarity of this signal. PB5, PB6 and PB7 lines when in output modes are "ANDed" with the SPI control signals. PB5 is connected with the SPI clock signal (SCL), PB6 with the SPI data signal (SDA) while PB7 is connected with SPI enable signal (SEN). Refer to I/O port and pin configuration description for additional information.

PC0-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register. PC0-PC2, PC4 have a push-pull configuration in output mode while PC3, PC5-PC7 (OSD signals) are open-drain (5V drive). PC3, PC5, PC6 and PC7 lines when in output modes are "ANDed" with the character and blank signals of the OSD cell. PC3 is connected with the OSD BLANK signal, PC5, PC6 and PC7 with the OSD R,G and B signals. These signals are active high. PC2 is also used as TV set On-Off switch (5V drive). Refer to I/O port and pin configuration description for additional information.

DA0-DA3. These pins are the four PWM D/A outputs (with 32KHz repetition) of the 6-bit on-chip D/A converters. The PWM function can be disabled by software and these lines can be used as general purpose open-drain outputs (12V drive). Refer to D/A converter description for additional information.

IRIN. This pin is the external NMI of the MCU

OUT1. This pin is the 62.5KHz output specially suited to drive multi-standard chroma processors. This function can be disabled by software and the pin can be used as general purpose open-drain output (12V drive). Refer to D/A converter description for additional information.

PIN DESCRIPTION (Continued)

BSW0-BSW3. These output pins can be used to select up to 4 tuning bands. These lines are configured as open-drain outputs (12V drive). Refer to AFC description for additional information.

KBY0-KBY2. These pins are input only and can be used for keyboard scan. They have CMOS threshold levels with schmitt trigger and on-chip 100 KΩ pull-up resistors. Refer to AFC description for additional information.

AFC. This is the input of the on-chip 10 levels comparator that can be used to implement the AFC function. This pin is an high impedance input able to withstand signals with a peak amplitude up to 12V. Refer to AFC description for additional information.

OSDOSCIN, OSDOSCOUT. These are the On Screen display oscillator terminals. An oscillation capacitor and coil network have to be connected to provide the right signal to the OSD.

HSYNC, VSYNC. These are the horizontal and vertical synchronization pins. The active polarity of these pins to the OSD macrocell can be selected by the user as ROM mask option. If the device is specified to have negative logic inputs, then when these signals are low the OSD oscillator stops. If the device is specified to have positive logic inputs, then when these signals are high the OSD oscillator stops. Refer to OSD description for additional information.

R, G, B, BLANK. Outputs from the OSD. R, G and B are the color outputs while BLANK is the blanking output. All outputs are open-drain. The active polarity of these pins to can be selected by the user as ROM mask option. Refer to the pin configurations for additional information.

VS. This is the output pin of the on-chip 14-bit voltage synthesis tuning cell (VS). The tuning signal present at this pin gives an approximate resolution of 40KHz per step over the UHF band. This line is a push-pull output with standard drive (ST6356,57,58 only).

Table 2. ST639X Pin Summary

Pin Function	Description
DA0 to DA3	Output, Open-Drain, 12V
BSW0 to BSW3	Output, Open-Drain, 12V
IRIN	Input, Resistive Bias, Schmitt Trigger
AFC	Input, High Impedance, 12V
OUT1	Output, Open-Drain, 12V
KBY0 to KBY2	Input, Pull-up, Schmitt Trigger
PA0 to PA7	I/O, Open-Drain, 12V, No Input Pull-up, Schmitt Trigger, High Drive
PB0-PB4	I/O, Push-Pull, 5V, Input Pull-up, Schmitt Trigger
PB5-PB7	I/O, Open-Drain, 5V, Input Pull-up, Schmitt Trigger
PC0-PC2, PC4	I/O, Push-Pull, 5V, Input Pull-up, Schmitt Trigger
PC3, PC5-PC7	I/O, Open-Drain, 5V, Input Pull-up, Schmitt Trigger
VS	Output, Push-Pull
R,G,B, BLANK	Output, Open-Drain, 5V
HSYNC, VSYNC	Input, Pull-up, Schmitt Trigger
OSDOSCIN	Input, High Impedance
OSDOSCOUT	Output, Push-Pull
TEST	Input, Pull-Down
OSCIN	Input, Resistive Bias, Schmitt Trigger to Reset Logic Only
OSCOUT	Output, Push-Pull
RESET	Input, Pull-up, Schmitt Trigger Input
V_{DD}, V_{SS}	Power Supply Pins

ST63XX CORE

The Core of the ST63XX Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control busses. The in-core communication is arranged as shown in the following block diagram figure; the controller being externally linked to both the reset and the oscillator, while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes through the control registers.

Registers

The ST63XX Family Core has five registers and three pairs of flags available to the programmer. They are shown in Figure 9 and are explained in the following paragraphs together with the program and data memory page registers.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is addressed in the data space as RAM location at the FFH address.

Figure 9. ST63XX Core Programming Model

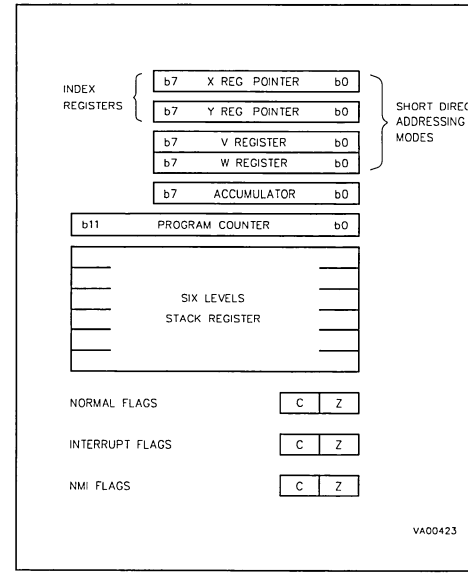
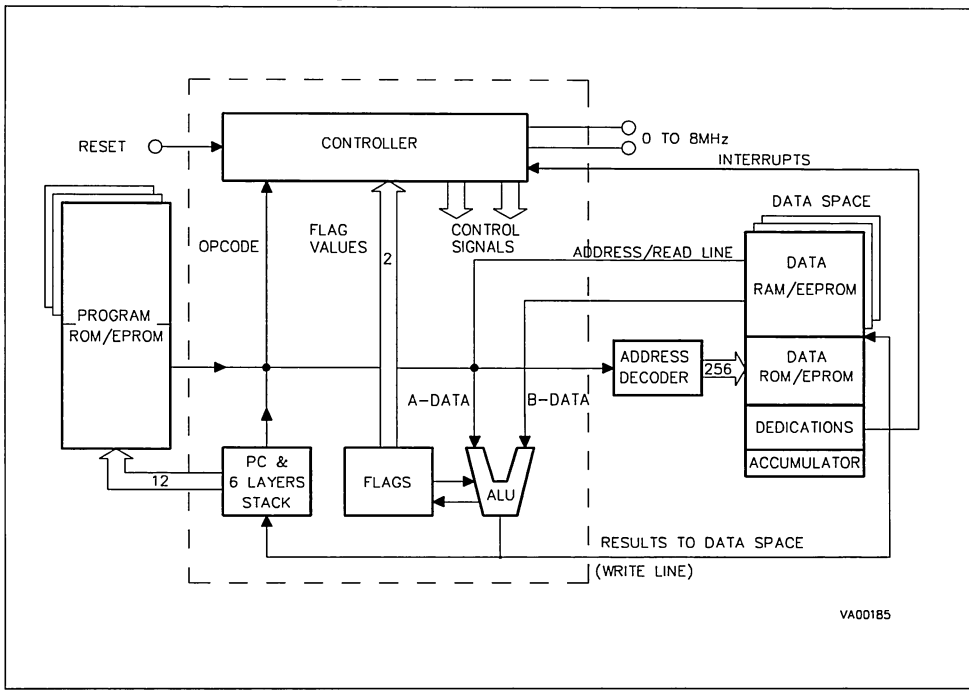


Figure 8. ST63XX Core Block Diagram



ST63XX CORE (Continued)

Accordingly, the ST63XX instruction set can use the accumulator as any other register of the data space.

Indirect Registers (X, Y). These two indirect registers are used as pointers to the memory locations in the data space. They are used in the register-indirect addressing mode.These registers can be addressed in the data space as RAM locations at the 80H (X) and 81H (Y) addresses. They can also be accessed with the direct, short direct, or bit direct addressing modes. Accordingly, the ST63XX instruction set can use the indirect registers as any other register of the data space.

Short Direct Registers (V, W). These two registers are used to save one byte in short direct addressing mode. These registers can be addressed in the data space as RAM locations at the 82H (V) and 83H (W) addresses. They can also be accessed with the direct and bit direct addressing modes. Accordingly, the ST63XX instruction set can use the short direct registers as any other register of the data space.

Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM location to be processed by the core. This ROM location may be an opcode, an operand, or an address of operand. The 12-bit length allows the direct addressing of 4096 bytes in the program space. Nevertheless, if the program space contains more than 4096 locations, the further program space can be addressed by using the Program Bank Switch register. The PC value is incremented, after it is read for the address of the current instruction, by sending it through the ALU, so giving the address of the next byte in the program. To execute relative jumps the PC and the offset values are shifted through the ALU, where they will be added, and the result is shifted back into the PC. The program counter can be changed in the following ways:

JP (Jump) instruction . . . . PC= Jump address

CALL instruction . . . . . PC= Call address

Relative Branch instructions . . . . . PC= PC+offset

Interrupt . . . . . PC= Interrupt vector

Reset . . . . . PC= Reset vector

Test mode . . . . . PC=Test mode vector (1)

RET & RETI instructions . . . PC= Pop (stack)

Normal instruction . . . . . PC= PC+1

Note: 1. Not available to the user.

Flags (C, Z)

The ST63XX Core includes three pairs of flags that correspond to 3 different modes: normal mode, interrupt mode and Non-Maskable-Interrupt-Mode. Each pair consists of a CARRY flag and a ZERO flag. One pair (CN, ZN) is used during normal operation, one pair is used during the interrupt mode (CI,ZI) and one is used during the not-maskable interrupt mode (CNMI, ZNMI).

The ST63XX Core uses the pair of flags that corresponds to the actual mode: as soon as an interrupt (resp. a Non-Maskable-Interrupt) is generated, the ST63XX Core uses the interrupt flags (resp. the NMI flags) instead of the normal flags. When the RETI instruction is executed, the normal flags (resp. the interrupt flags) are restored if the MCU was in the normal mode (resp. in the interrupt mode) before the interrupt. Should be observed that each flag set can only be addressed in its own routine (Not-maskable interrupt, normal interrupt or main routine). The interrupt flags are not cleared during the context switching and so, they remain in the state they were at the exit of the last routine switching.

The Carry flag is set when a carry or a borrow occurs during arithmetic operations, otherwise it is cleared. The Carry flag is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

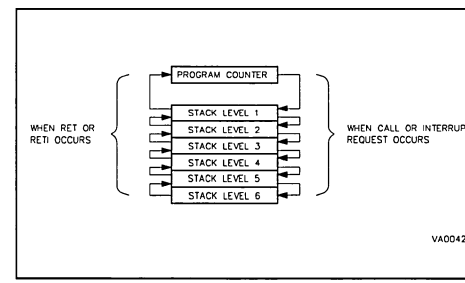
The Zero flag is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

The switching between these three sets is automatically performed when an NMI, an interrupt and a RETI instructions occur. As the NMI mode is automatically selected after the reset of the MCU, the ST63XX Core uses at first the NMI flags. Refer to INTERRUPT description for additional information.

Stack

The ST63XX Core includes true LIFO hardware stack that eliminates the need for a stack pointer.

Figure 10. Stack Operation

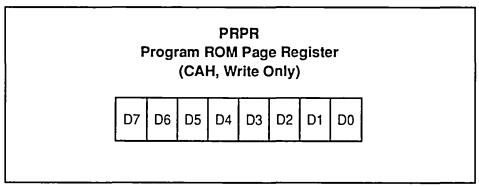


ST63XX CORE (Continued)

The stack consists of six separate 12-bit RAM locations that do not belong to the data space RAM area. When a subroutine call (or interrupt request) occurs, the contents of each level is shifted into the next level while the content of the PC is shifted into the first level (the value of the sixth level will be lost). When subroutine or interrupt return occurs (RET or RETI instructions), the first level register is shifted back into the PC and the value of each level is shifted back into the previous level. These two operating modes are described in Figure 10. Since the accumulator, as all other data space registers, is not stored in this stack the handling of this registers shall be performed inside the subroutine. The stack pointer will remain in its deepest position, if more than 6 calls or interrupts are executed, so that the last return address will be lost. It will also remain in its highest position if the stack is empty and a RET or RETI is executed. In this case the next instruction will be executed.

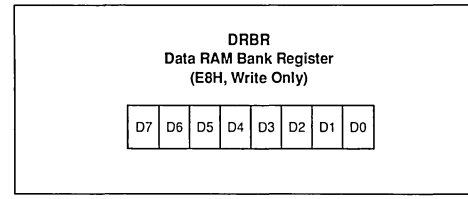
Memory Registers

Figure 11. Program ROM Page Register



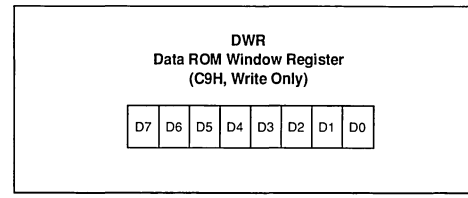
The PRPR register can be addressed like a RAM location in the Data Space at the CAH address; nevertheless it is a write-only register that can not be accessed with single-bit operations. This register is used to select the 2-Kbyte ROM bank of the Program Space that will be addressed. The number of the page has to be loaded in the PRPR register. The PRPR register is not cleared during the MCU initialization and should therefore be defined before jumping out of the static page. Refer to the Program Space description for additional information concerning the use of this registers. The PRPR register is not modified when an interrupt or a subroutine occurs.

Figure 12. Data RAM Bank Register



The DRBR register can be addressed like a RAM location in the Data Space at the E8H address, nevertheless it is write-only register that can not be accessed with single-bit operations. This register is used to select the desired 64-byte RAM/EEPROM bank of the Data Space. The number of the bank has to be loaded in the DRBR register and the instruction has to point to the selected location as it was in the 0 bank (from 00H address to 3FH address). This register is cleared during the MCU initialization (the Data space 0 bank is automatically addressed after the Reset). Refer to the Data Space description for additional information. The DRBR register is not modified when a interrupt or a subroutine occurs.

Figure 13. Data ROM Window Register



The DWR register can be addressed like a RAM location in the Data Space at the C9H address, nevertheless it is write-only register that can not be accessed with single-bit operations. This register is used to move up and down the 64-byte read-only data window (from the 40H address to 7FH address of the Data Space) along the ROM memory of the MCU by step of 64 bytes. The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 less significant bits of the address given in the instruction (as less significant bits) and the content of the DWR register (as most significant bits). Refer to the Data Space description for additional information.

MEMORY SPACES

The MCUs operate in three different memory spaces: Program Space, Data Space, and Stack Space. A description of these spaces is shown in Figure 14 and Figure 15.

Figure 14. ST632X,5X Data Space

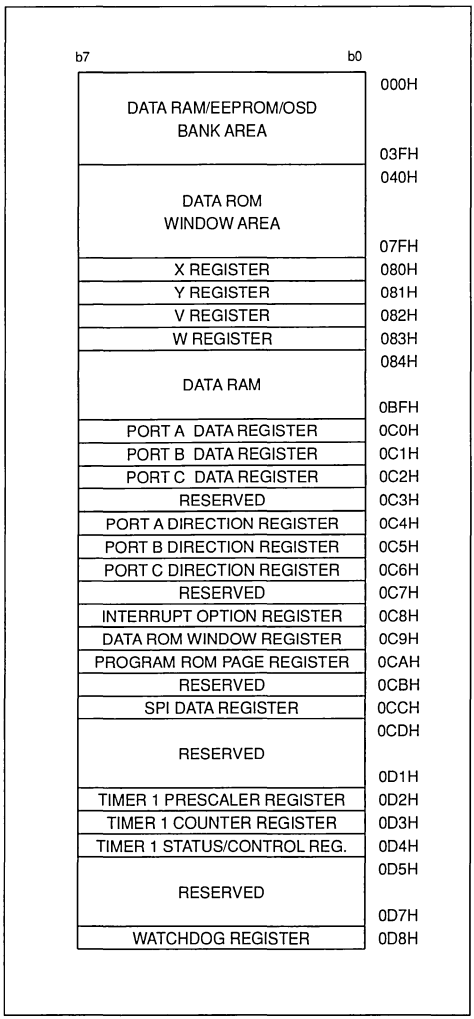
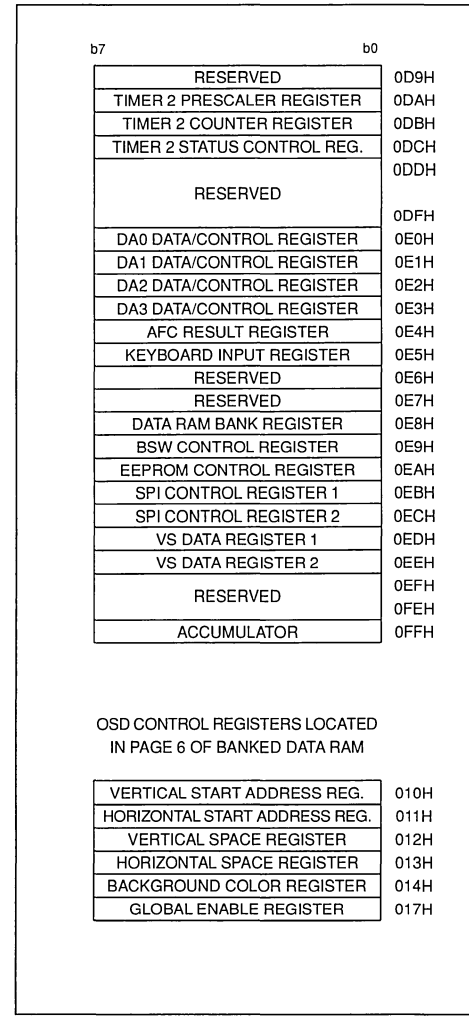


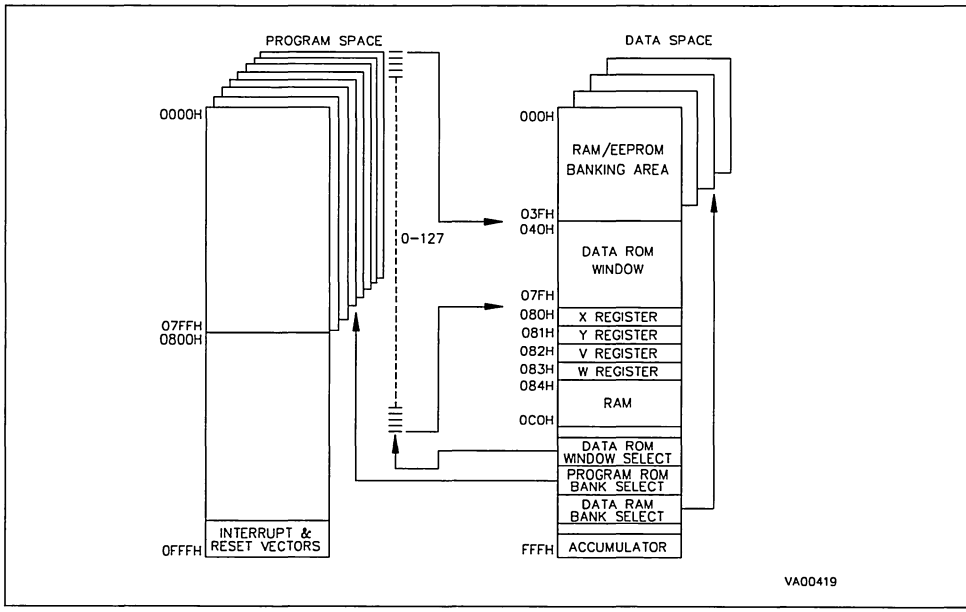
Figure 15. ST632X,5X Data Space (Continued)



Note 1. VS data registers are available only on ST6356,57,58

MEMORY SPACES (Continued)

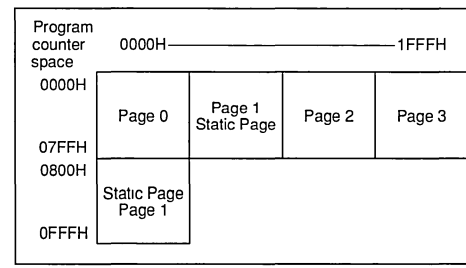
Figure 16. ST632X,5X Memory Addressing Description Diagram



Program Space

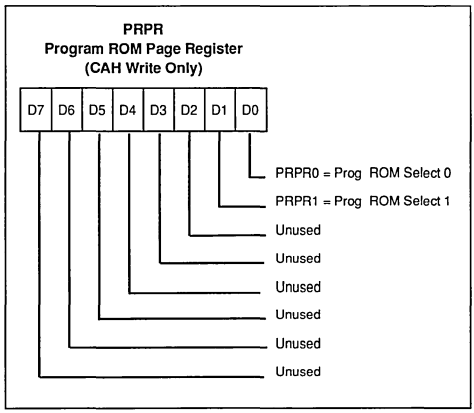
The program space is physically implemented in the ROM memory and includes all the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, the reserved test area and user vectors. It is addressed thanks to the 12-bit Program Counter register (PC register) and so, the ST63XX Core can directly address up to 4K bytes of Program Space. Nevertheless, the Program Space can be extended by the addition of 2-Kbyte ROM banks as it is shown in figure 16 in which an 8 Kbyte memory is described. These banks are addressed by pointing to the 000H-7FFH locations of the Program Space thanks to the Program Counter, and by writing the appropriate code in the Program ROM Page Register (PRPR register) located at the CAH address of the Data Space. Because interrupts and common subroutines should be available all the time only the lower 2K byte of the 4K program space are bank switched while the upper 2K byte can be seen as static space. Table 3 gives the different codes that allows the selection of the corresponding banks. Note that, from the memory point of view, the Page 1 and the Static Page represent the same physical memory: it is only a different way of addressing the same location. On ST632X,5X a total of 8192 bytes of ROM have been implemented; 7948 are available as user ROM while 244 are reserved for testing.

Figure 17. 8K Bytes Program Space Addressing Description



MEMORY SPACES (Continued)

Figure 18. Program ROM Page Register



D7-D2. These bits are not used.

PRPR1-PRPR0. These are the program ROM banking bits and the value loaded selects the corresponding page to be addressed in the lower part of 4K program address space as specified in Table 3. This register is undefined on reset.

Table 3. ST632X,5X Program ROM Page Register Coding

PRPR1	PRPR0	PC11	Memory Page
X	X	1	Static Page (Page 1)
0	0	0	Page 0
0	1	0	Page 1 (Static Page)
1	0	0	Page 2
1	1	0	Page 3

Note. The number of bits implemented depends on the size of the ROM of the device. Only the lower part of address space has been bankswitched because interrupt vectors and common subroutines should be available all the time. The reason of this structure is due to the fact that it is not possible to jump from a dynamic page to another, unless jumping back to the static page, changing contents of PRPR, and, than, jumping to a different dynamic page.

Care is required when handling the PRPR register as it is write only. For this reason, it is not allowed to change the PRPR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. Anyway, this operation may be necessary if the sum of common routines and interrupt drivers will take more than 2K bytes; in this case could be necessary to divide the interrupt driver in a (minor) part in the static page (start and end), and in the second (major) part in one dynamic page. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the PRPR it writes also the image register. The image register must be written first, so if an interrupt occurs between the two instructions the PRPR register is not affected.

MEMORY SPACE (Continued)

Table 4. ST632X,5X Program ROM Memory Map

ROM Page	Device Address	EPROM Address (1)	Description
PAGE 0	0000H-007FH 0080H-07FFH	0000H-007FH 0080H-07FFH	Reserved User ROM
PAGE 1 "STATIC"	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	User ROM Reserved Interrupt Vectors Reserved NMI Vector Reset Vector
PAGE 2	0000H-000FH 0010H-07FFH	1000H-100FH 1010H-17FFH	Reserved User ROM
PAGE 3	0000H-000FH 0010H-07FFH	1800H-180FH 1810H-1FFFH	Reserved User ROM

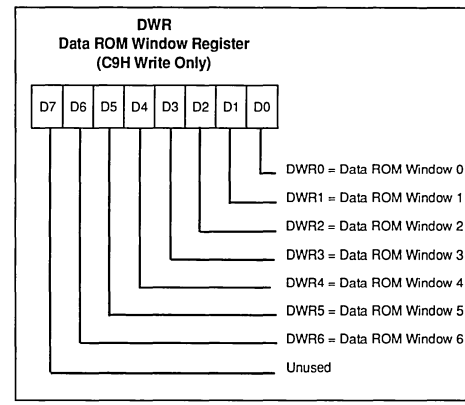
Note 1. EPROM addresses are related to the use of ST63PXX piggyback emulation devices.

Data Space

The instruction set of the ST63XX Core operates on a specific space, named Data Space that contains all the data necessary for the processing of the program. The Data Space allows the addressing of RAM memory, EEPROM memory, ST63XX Core/peripheral registers, and read-only data such as constants and the look-up tables.

Data ROM Addressing. All the read-only data are physically implemented in the ROM memory in which the Program Space is also implemented. The ROM memory therefore contains the program to be executed and also the constants and the look-up tables needed for the program. The locations of Data Space in which the different constants and look-up tables are addressed by the ST63XX Core can be considered as being a 64-byte window through which it is possible to access to the read-only data stored in the ROM memory. This window is located from the 40H address to the 7FH address in the Data space and allows the direct reading of the bytes from the 000H address to the 03FH address in the ROM memory. All the bytes of the ROM memory can be used to store either instructions or read-only data. Indeed, the window can be moved by step of 64 bytes along the ROM memory in writing the appropriate code in the Write-only Data ROM Window register (DWR register, location C9H). The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 less significant bits of the address in the Data Space (as less significant bits) and the content of the DWR register (as most significant bits). So when addressing location 40H of data space, and 0 is loaded in the DWR register, the physical addressed location in ROM is 00H.

Figure 19. Data ROM Window Register



D7. This bit is not used.

DWR6-DWR0. These are the Data Rom Window bits that correspond to the upper bits of data ROM program space. This register is undefined after reset.

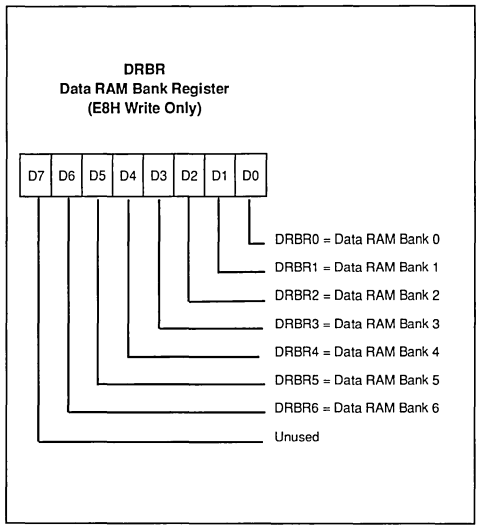
Notes Care is required when handling the DWR register as it is write only. For this reason, it is not allowed to change the DWR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the DWR it writes also the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DWR register is not affected.

MEMORY SPACE (Continued)

Data RAM/EEPROM/OSD RAM Addressing

In all members of the ST63XX family 64 bytes of data RAM are directly addressable in the data space from 80H to BFH addresses. The additional 192 bytes of RAM the 128 bytes of EEPROM memory and the OSD RAM can be addressed using the banks of 64 bytes located between addresses 00H and 3FH. The selection of the bank is done by programming the Data RAM Bank Switching register (DRBR register) located at the E8H address of the Data Space. In this way each bank of RAM, EEPROM or OSD RAM can be selected 64 bytes at a time. No more than one bank should be set at a time.

Figure 20. Data RAM Bank Register



D7. This bit is not used.

DRBR6, DRBR5. Each of these bits, when set, will select one OSD RAM register page.

DRBR4,DRBR3,DRBR2. Each of these bits, when set, will select one RAM page.

DRBR1,DRBR0. These bits select the EEPROM pages. Table 5 summarizes how to set the Data RAM Bank Register in order to select the various banks or pages.

This register is undefined after reset.

Table 5. Data RAM Bank Register Set-up

DRBR Value	Selection
01H	EEPROM Page 0
02H	EEPROM Page 1
04H	RAM Page 2
08H	RAM Page 3
10H	RAM Page 4
20H	OSD Page 5
40H	OSD Page 6

Notes :

Care is required when handling the DRBR register as it is write only. For this reason, it is not allowed to change the DRBR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the DRBR it writes also the image register.
The image register must be written first, so if an interrupt occurs between the two instructions the DRBR register is not affected.

EEPROM Description

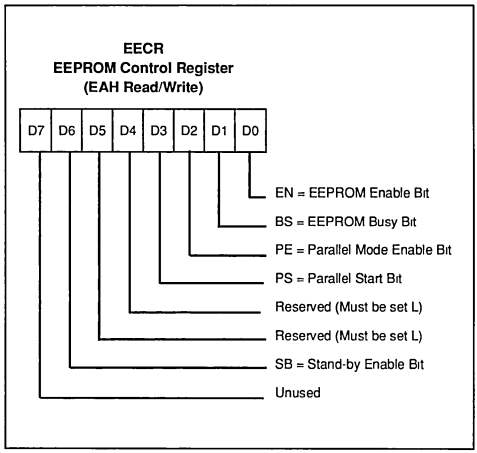
Through the programming of the Data RAM Bank Register (DRBR= E8H) the user can select the bank or page leaving unaffected the way to address the static registers. The way to address the "dynamic" page is to set the DRBR as described in Table 5 (e.g. to select EEPROM page 0, the DRBR has to be loaded with content 01H, see Data RAM/EEPROM/OSD RAM addressing for additional information). Bits 0, 1 of the DRBR are dedicated to the EEPROM.

The EEPROM module is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. The EEPROM is controlled by the EEPROM Control Register (EECR=EAH). Any EEPROM location can be read just like any other data location, also in terms of access time.

To write an EEPROM location takes about 5 mSec (10mSec max) and during this time the EEPROM is not accessible by the Core. A busy flag can be read by the Core to know the EEPROM status before trying any access. In writing the EEPROM can work in two modes: Byte Mode (BMODE) and Parallel Mode (PMODE). The BMODE is the normal way to use the EEPROM and consists in accessing one byte at a time. The PMODE consists in accessing 8 bytes per time.

MEMORY SPACE (Continued)

Figure 21. EEPROM Control Register



D7. Not used

SB. *WRITE ONLY.* If this bit is set the EEPROM is disabled (any access will be meaningless) and the power consumption of the EEPROM is reduced to the leakage values.

D5, D4. Reserved for testing purposes, they must be set to zero.

PS. *SET ONLY.* Once in Parallel Mode, as soon as the user software sets the PS bit the parallel writing of the 8 adjacent registers will start. PS is internally reset at the end of the programming procedure. Note that less than 8 bytes can be written; after parallel programming the remaining undefined bytes will have no particular content.

PE. *WRITE ONLY.* This bit must be set by the user program in order to perform parallel programming (more bytes per time). If PE is set and the "parallel start bit" (PS) is low, up to 8 adjacent bytes can be written at the maximum speed, the content being stored in volatile registers. These 8 adjacent bytes can be considered as row, whose A7, A6, A5, A4, A3 are fixed while A2, A1 and A0 are the changing bytes. PE is automatically reset at the end of any parallel programming procedure. PE can be reset by the user software before starting the programming procedure, leaving unchanged the EEPROM registers.

BS. *READ ONLY.* This bit will be automatically set by the CORE when the user program modifies an EEPROM register. The user program has to test it before any read or write EEPROM operation; any attempt to access the EEPROM while "busy bit" is set will be aborted and the writing procedure in progress completed.

EN. *WRITE ONLY.* This bit MUST be set to one in order to write any EEPROM register. If the user program will attempt to write the EEPROM when EN= 0 the involved registers will be unaffected and the "busy bit" will not be set.

After RESET the content of EECR register will be 00H.

Notes :

When the EEPROM is busy (BS= 1) the EECR can not be accessed in write mode, it is only possible to read BS status. This implies that as long as the EEPROM is busy it is not possible to change the status of the EEPROM control register. EECR bits 4 and 5 are reserved for testing purposes, and the user must never set them to 1.

Additional Notes on Parallel Mode. If the user wants to perform a parallel programming the first action should be the set to one the PE bit; from this moment the first time the EEPROM will be addressed in writing, the ROW address will be latched and it will be possible to change it only at the end of the programming procedure or by resetting PE without programming the EEPROM. After the ROW address latching the Core can "see" just one EEPROM row (the selected one) and any attempt to write or read other rows will produce errors. Do not read the EEPROM while PR is set.

As soon as PE bit is set, the 8 volatile ROW latches are cleared. From this moment the user can load data in the whole ROW or just in a subset. PS setting will modify the EEPROM registers corresponding to the ROW latches accessed after PE. For example, if the software sets PE and accesses EEPROM in writing at addresses 18H,1AH,1BH and then sets PS, these three registers will be modified at the same time; the remaining bytes will have no particular content. Note that PE is internally reset at the end of the programming procedure. This implies that the user must set PE bit between two parallel programming procedures. Anyway the user can set and then reset PE without performing any EEPROM programming. PS is a set only bit and is internally reset at the end of the programming procedure. Note that if the user tries to set PS while PE is not set there will not be any programming procedure and the PS bit will be unaffected. Consequently PS bit can not be set if EN is low. PS can be affected by the user set if, and only if, EN and PE bits are also set to one.

MEMORY SPACE (Continued)

Warning : *Parallel programming of the EEPROM with less than eight bytes may corrupt other bytes and should therefore be used with care, as here after underlined.*

a. *Reason for limitation:*
betweeen PE (Parallel Enable) and PS (Parallel Start) of the EEPROM, the user writes up to eight bytes into the volatile data registers, a latch is also set to indicate which bytes have been accessed; the accessed bytes will be programmed when PS arrives. The logic is such that it is possible to set the latches of bytes which have NOT been accessed. The latches are set whenever ANY register in the banked dataspace (00h-3FH) is accessed for READ or WRITE between a PE and PS. The latch which is set will be determined by the three least significant bits of the register address. Only the latch is set, so finaal data of a corrupted byte after the parallel programming is always FFH.

Note: *read operations also occur internally to the micro for most instructions. Even if bytes are not seen to be corrupted within the parallel programming routine, care should be taken, since they could become corrupted by an interrupt routine being serviced during loading of parallel bytes.*
This is logic related and is not a marginality or race condition; piggyback devices perform in the same way as ROM devices. Parallel programming is tested with only LDI rr,nn instructions which do not corrupt other bytes.

b. *To Avoid Corrupted Bytes:*
- *use Single Byte Mode, or*
- *always define all eight bytes in Parallel Programming Mode, or*
- *when programming less than eight bytes, the remaining EEPROM bytes should do not used by the program.*

Additional Notes Regarding Differences Between ST63XX Devices and Corresponding Emulators. While PE is set, all the EEPROM page currently selected is accessible in reading and the writing of the bytes happens at the row to which belongs the last byte written before setting PS. The sequence: set PE, write in 10H the value X, write in 21H the value Y, set PS, will result in: 10H unchanged, 20H loaded with value X, 21H loaded with value Y. In the emulator bits 4 and 5 of the EECR are implemented.If the user set to 1 one or both of these bits the contents of the EEPROM will be destroyed. The user should use care in using EEPROM emulation as in general the emulator does not emulate the behaviour of the EEPROM when it is misused.

STACK SPACE

The stack space consists of six 12 bit registers that are used for stacking subroutine and interrupt return addresses plus the current program counter register.

TEST MODE

The test mode can be entered by connecting the TEST pin to an high logic level when reset is active; this action enables the factory test mode. The user is recommended to avoid this situation for normal operation. (TEST pin should be tied to ground).

INTERRUPT

The ST63XX Core can manage 4 different maskable interrupt sources, plus one non-maskable interrupt source (top priority level interrupt). Each source is associated with a particular interrupt vector that contains a Jump instruction to the related interrupt service routine. Each vector is located in the Program Space at a particular address (see Table 6). When a source provides an interrupt request, and the request processing is also enabled by the ST63XX Core, then the PC register is loaded with the address of the interrupt vector (i.e. of the Jump instruction). Finally, the PC is loaded with the address of the Jump instruction and the interrupt routine is processed.

The relationship between vector and source and the associated priority is hardware fixed for the different ST63XX devices. For some interrupt sources it is also possible to select by software the kind of event that will generate the interrupt.

All interrupts can be disabled by writing to the GEN bit (global interrupt enable) of the interrupt option register (address C8H). After a reset, ST63XX is in non maskable interrupt mode, so no interrupts will be accepted and NMI flags will be used, until a RETI instruction is executed. If an interrupt is executed, one special cycle is made by the core, during that the PC is set to the related interrupt vector address. A jump instruction at this address has to redirect program execution to the beginning of the related interrupt routine. The interrupt detecting cycle, also resets the related interrupt flag (not available to the user), so that another interrupt can be stored for this current vector, while its driver is under execution.

If additional interrupts arrive from the same source, they will be lost. NMI can interrupt other interrupt routines at any time, while other interrupts cannot interrupt each other. If more than one interrupt is waiting for service, they are executed according to their priority. The lower the number, the higher the priority. Priority is, therefore, fixed. Interrupts are checked during the last cycle of an instruction

INTERRUPT (Continued)

(RETI included). Level sensitive interrupts have to be valid during this period.

Table 6 details the different interrupt vectors/sources relationships.

Table 6. Interrupt Vectors/Sources Relationships

Interrupt Source	Associated Vector	Vector Address
IRIN/NMI Pin (1)	Interrupt Vector # 0 (NMI)	0FFCH-0FFDH
None (2)	Interrupt Vector # 1	0FF6H-0FF7H
Vsync	Interrupt Vector # 2	0FF4H-0FF5H
Timer 1	Interrupt Vector # 3	0FF2H-0FF3H
Timer 2	Interrupt Vector # 4	0FF0H-0FF1H

Notes:
1. This pin is associated with the NMI Interrupt Vector.
2. This vector is not used in ST632X,5X

Interrupt Vectors/Sources

The ST63XX Core includes 5 different interrupt vectors in order to branch to 5 different interrupt routines. The interrupt vectors are located in the fixed (or static) page of the Program Space.

The interrupt vector associated with the non-maskable interrupt source is named interrupt vector #0. It is located at the (FFCH,FFDH) addresses in the Program Space. On ST632X,5X this vector is associated to the rising edge sensitive external interrupt pin.

The interrupt vectors located at addresses (FF6H,FF7H), (FF4H,FF5H), (FF2H,FF3H), (FF0H,FF1H) are named interrupt vectors #1, #2, #3 and #4 respectively. These vectors are associated with VSYNC (#2), TIMER 1 (#3) and TIMER 2 (#4); Interrupt vector (#1) is not used on ST6356,57,58. Refer to the Interrupt Details description for more information.

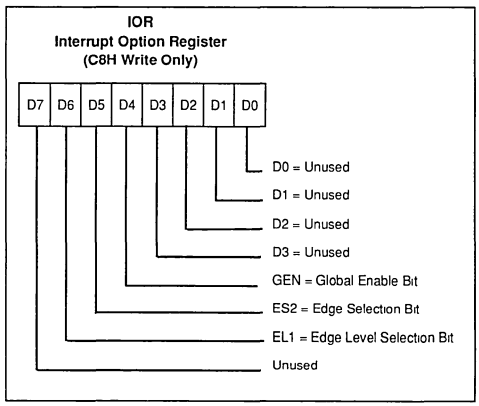
Interrupt Priority

The non-maskable interrupt request has the highest priority and can interrupt any other interrupt routines at any time, nevertheless the other interrupts cannot interrupt each other. If more than one interrupt request is pending, they are processed by the ST63XX Core according to their priority level: vector #1 has the higher priority while vector #4 the lower. The priority of each interrupt source is hardware fixed.

Interrupt Option Register

The Interrupt Option Register (IOR register, location C8H) is used to enable/disable the individual interrupt sources and to select the operating mode of the external interrupt inputs. This register can be addressed in the Data Space as RAM location at the C8H address, nevertheless it is write-only register that can not be accessed with single-bit operations. The operating modes of the external interrupt inputs associated to interrupt vectors #1 and #2 are selected through bits 4 and 5 of the IOR register.

Figure 22. Interrupt Option Register



D7. Not used.

EL1. This is the Edge/Level selection bit of interrupt #1. When set to one, the interrupt is generated on low level of the related signal; when cleared to zero, the interrupt is generated on falling edge. The bit is cleared to zero after reset and as no interrupt source is associated to vector #1 on ST63XX, the user must keep this bit to zero to avoid ghost interrupts from this source.

ES2. This is the edge selection bit on interrupt #2. This bit is used on the ST63XX devices with on-chip OSD generator for VSYNC detection.

GEN. This is the global enable bit. When set to one all interrupts are globally enabled ; when this bit is cleared to zero all interrupts are disabled (including NMI).

D3 - D0. These bits are not used.

INTERRUPT (Continued)

Interrupt Procedure

The interrupt procedure is very similar to a call procedure; the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event the user does not know about the context and the time at which it occurred. As a result the user should save all the data space registers which will be used inside the interrupt routines. There are separate sets of processor flags for normal, interrupt and non-maskable interrupt modes which are automatically switched and so these do not need to be saved.

The following list summarizes the interrupt procedure (refer also to Figure 23. Interrupt Processing Flow Chart):

- Interrupt detection
- The flags C and Z of the main routine are exchanged with the flags C and Z of the interrupt routine (resp. the NMI flags)
- The value of the PC is stored in the first level of the stack - The normal interrupt lines are inhibited (NMI still active)
- The edge flip-flop is reset
- The related interrupt vector is loaded in the PC.
- User selected registers are saved inside the interrupt service routine (normally on a software stack)
- The source of the interrupt is found by polling (if more than one source is associated to the same vector)
- Interrupt servicing
- Return from interrupt (RETI)
- Automatically the ST63XX core switches back to the normal flags (resp the interrupt flags) and pops the previous PC value from the stack

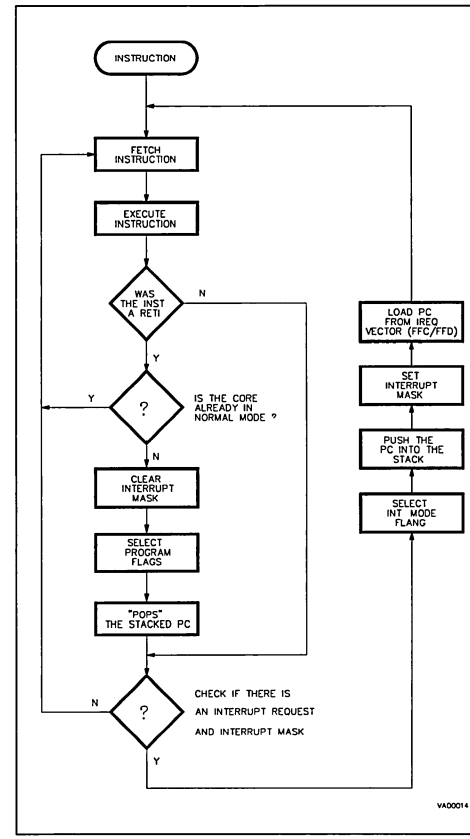
The interrupt routine begins usually by the identification of the device that has generated the interrupt request. The user should save the registers which are used inside the interrupt routine (that holds relevant data) into a software stack.
After the RETI instruction execution, the Core carries out the previous actions and the main routine can continue.

ST632X/5X Interrupt Details

IR Interrupt (#0). The IRIN Interrupt is associated with the first interrupt #0 (NMI, 0FFCH). If enabled, then an interrupt will be generated on a rising edge at the pin.

Interrupt (#1). On ST632X/5X no sources are associated to vector (#1). To avoid any ghost interrupt due to interrupt (#1) the user must keep to zero the EL1 bit of IOR register.

Figure 23. Interrupt Processing Flow-Chart



VSYNC Interrupt (#2). The VSYNC Interrupt is connected to the interrupt #2. When disabled the VSYNCINT signal is low. Bit 5 of the interrupt option register C8H is used to select the negative edge (B2=0) or the positive edge (B2=1); the edge will depend on the application. Note that once an edge has been latched, then the only way to remove the latched signal is to service the interrupt. Care must be taken not to generate spurious interrupts. This interrupt may be used for synchronize to the VSYNC signal in order to change characters in the OSD only when the screen is on vertical blanking (if desired). This method may also be used to blink characters.

INTERRUPT (Continued)

TIMER 1 Interrupt (#3). The TIMER 1 Interrupt is connected to the fourth interrupt #3 (0FF2H) which detects a high to low level (latched in the timer). For more information on the timer interrupt refer to the timer section.

Timer 2 Interrupt (#4). The TIMER 2 Interrupt is connected to the fifth interrupt #4 (0FF0H) which detecty a high to low level (latched in the timer). For more information on the timer interrupt refer to the timer section.

Notes Global disable does not reset edge sensitive interrupt flags. These edge sensitive interrupts become pending again when global disabling is released. Moreover, edge sensitive interrupts are stored in the related flags also when interrupts are globally disabled, unless each edge sensitive interrupt is also individually disabled before the interrupting event happens. Global disable is done by clearing the GEN bit of Interrupt option register, while any individual disable is done in the control register of the peripheral. The on-chip Timer peripherals have an interrupt request flag bit (TMZ), this bit is set to one when the device wants to generate an interrupt request and a mask bit (ETI) that must be set to one to allow the transfer of the flag bit to the Core.

RESET

The ST63XX devices can be reset in two ways: by the external reset input (RESET) tied low and by the hardware activated digital watchdog peripheral.

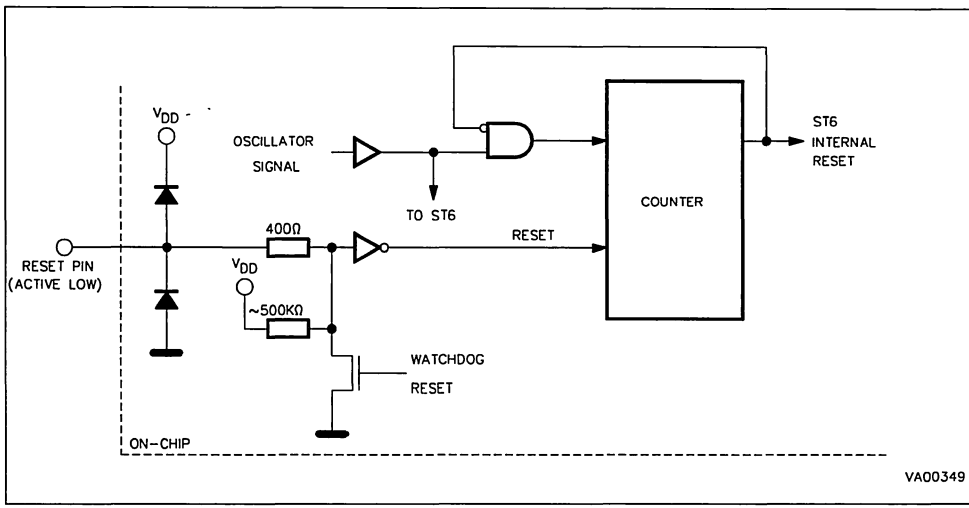
RESET Input

The external active low reset pin is used to reset the ST63XX devices and provide an orderly software startup procedure. The activation of the Reset pin may occur at any time in the RUN or WAIT mode. Even short pulses at the reset pin will be accepted since the reset signal is latched internally and is only cleared after 2048 clocks at the oscillator pin. The clocks from the oscillator pin to the reset circuitry are buffered by a schmit trigger so that an oscillator in start-up conditions will not give spurious clocks. The MCU is configured in the Reset mode as long as the signal of the RESET pin is low. The processing of the program is stopped and the standard Input/Output ports (port A, port B and port C) are in the input state (except PC2). As soon as the level on the reset pin becomes high, the initialization sequence is executed. Refer to the MCU initialization sequence for additional information.

Watchdog Reset

The ST63XX devices are provided with an on-chip hardware activated digital watchdog function in order to provide a graceful recovery from a software upset. If the watchdog register is not refreshed and the end-of-count is reached, then the reset state will be latched into the MCU and an internal circuit pulls down the reset pin. This also

Figure 24. Internal Reset Circuit



RESET (Continued)

Figure 25. Reset & Interrupt Processing Flow-chart

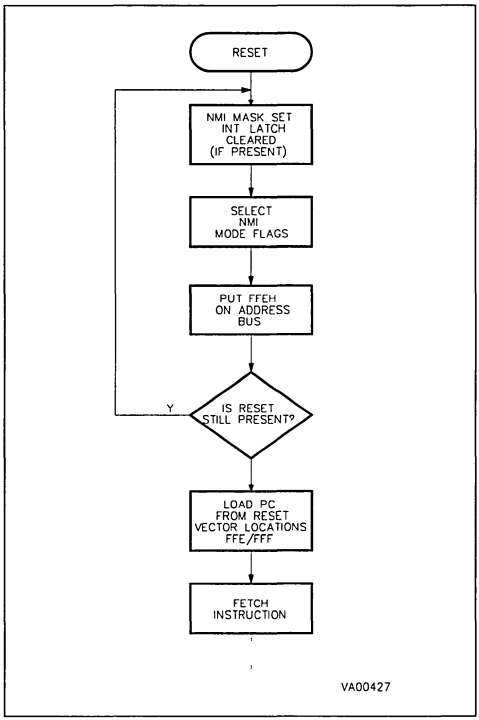
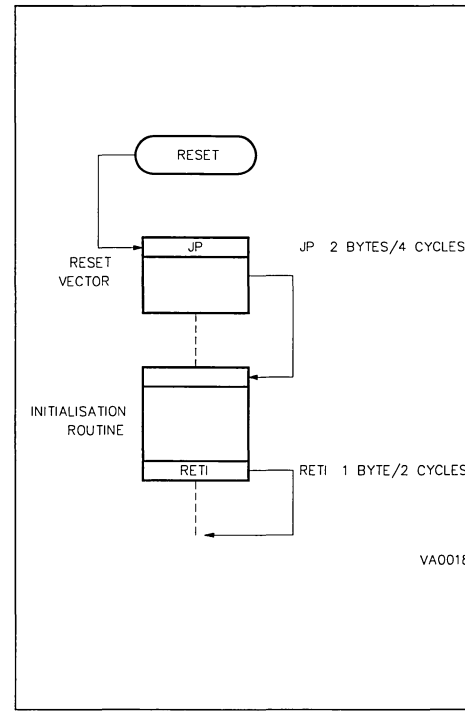


Figure 26. Restart Initialization Program Flow-chart



resets the watchdog which subsequently turns off the pull-down and activates the pull-up device at the reset pin. This causes the positive transition at the reset pin. The MCU will then exit the reset state after 2048 clocks on the oscillator pin.

Application Notes

An external resistor between V_{DD} and the reset pin is not required because an internal pull-up device is provided. The user may prefer to add an external pull-up resistor.

An internal Power-on device does not guarantee that the MCU will exit the reset state when V_{DD} is above 4.5V and therefore the RESET pin should be externally controlled.

MCU Initialization Sequence

When a reset occurs the stack is reset to program counter, the PC is loaded with the address of the reset vector (located in the program ROM at addresses FFEH & FFFH). A jump instruction to the beginning of the program has to be written into these locations. After a reset the interrupt mask is automatically activated so that the Core is in non-maskable interrupt mode to prevent false or ghost interrupts during the restart phase. Therefore the restart routine should be terminated by a RETI instruction to switch to normal mode and enable interrupts. If no pending interrupt is present at the end of the reset routine, the ST63XX will continue with the instruction after the RETI; otherwise the pending interrupt will be serviced.

WAIT & STOP MODES

The STOP and WAIT modes have been implemented in the ST63XX Core in order to reduce the consumption of the device when the latter has no instruction to execute. These two modes are described in the following paragraphs. On ST63XX as the hardware activated digital watchdog function is present the STOP instruction is de-activated and any attempt to execute it will cause the automatic execution of a WAIT instruction.

WAIT Mode

The configuration of the MCU in the WAIT mode occurs as soon as the WAIT instruction is executed. The microcontroller can also be considered as being in a "software frozen" state where the Core stops processing the instructions of the routine, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage but where the peripherals are still working.

The WAIT mode is used when the user wants to reduce the consumption of the MCU when it is in idle, while not loosing count of time or monitoring of external events. The oscillator is not stopped in order to provide clock signal to the peripherals. The timers counting may be enabled (writing the PSI bit in TSCR register) and the timer interrupt may be also enabled before entering the WAIT mode; this allows the WAIT mode to be left when timer interrupt occurs. If the exit from the WAIT mode is performed with a general RESET (either from the activation of the external pin or by watchdog reset) the MCU will enter a normal reset procedure as described in the RESET chapter. If an interrupt is generated during WAIT mode the MCU behaviour depends on the state of the ST63XX Core before the initialization of the WAIT sequence, but also of the kind of the interrupt request that is generated. This case will be described in the following paragraphs. In any case, the ST63XX Core does not generate any delay after the occurrence of the interrupt because the oscillator clock is still available.

STOP Mode

On ST63XX the hardware watchdog is present and the STOP instruction has been de-activated. Any attempt to execute a STOP will cause the automatic execution of a WAIT instruction.

Exit from WAIT Mode

The following paragraphs describe the output procedure of the ST63XX Core from WAIT mode when an interrupt occurs. It must be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non-maskable interrupt mode) before the start of the WAIT sequence, but also of the type of the interrupt request that is generated.

Normal Mode. If the ST63XX Core was in the main routine when the WAIT instruction has been executed, the ST63XX Core outputs from the wait mode as soon as any interrupt occurs; the related interrupt routine is executed and at the end of the interrupt service routine the instruction that follows the WAIT instruction is executed if no other interrupts are pending.

Non-maskable Interrupt Mode. If the WAIT instruction has been executed during the execution of the non-maskable interrupt routine, the ST63XX Core outputs from the wait mode as soon as any interrupt occurs: the instruction that follows the WAIT instruction is executed and the ST63XX Core is still in the non-maskable interrupt mode even if an other interrupt has been generated.

Normal Interrupt Mode. If the ST63XX Core was in the interrupt mode before the initialization of the WAIT sequence, it outputs from the wait mode as soon as any interrupt occurs. Nevertheless, two cases have to be considered:

- If the interrupt is a normal interrupt, the interrupt routine in which the WAIT was entered will be completed with the execution of the instruction that follows the WAIT and the ST63XX Core is still in the interrupt mode. At the end of this routine pending interrupts will be serviced in accordance to their priority.
- If the interrupt is a non-maskable interrupt, the non-maskable routine is processed at first. Then, the routine in which the WAIT was entered will be completed with the execution of the instruction that follows the WAIT and the ST63XX Core is still in the normal interrupt mode.

Notes :

If all the interrupt sources are disabled, the restart of the MCU can only be done by a Reset activation. The Wait instruction is not executed if an enabled interrupt request is pending. In the ST63XX the hardware activated digital watchdog function is present. As the watchdog is always activated the STOP instruction is de-activated and any attempt to execute the STOP instruction will cause an execution of a WAIT instruction.

ON-CHIP CLOCK OSCILLATOR

The internal oscillator circuit is designed to require a minimum of external components. A crystal quartz, a ceramic resonator, or an external signal (provided to the OSCIN pin) may be used to generate a system clock with various stability/cost tradeoffs. The typical clock frequency is 8MHz. Please note that different frequencies will affect the operation of those peripherals (D/As, SPI, 62.5 KHz OUT) whose reference frequencies are derived from the system clock.

The different clock generator options connection methods are shown in Figure 27, crystal specifications and suggested PC board layouts are given in Figure 28 and Figure 29. One machine cycle takes 13 oscillator pulses; 12 clock pulses are needed to increment the PC while and additional 13th pulse is needed to stabilize the internal latches during memory addressing. This means that with a clock frequency of 8MHz the machine cycle is 1.625µSec.

The crystal oscillator start-up time is a function of many variables: crystal parameters (especially RS), oscillator load capacitance (CL), IC parameters, ambient temperature, and supply voltage.It must be observed that the crystal or ceramic leads and circuit connections must be as short as possible. Typical values for CL1 and CL2 are in the range of 15pF to 22pF but these should be chosen based on the crystal manufacturers specification. Typical input capacitance for OSCIN and OSCOUT pins is 5pF.

The oscillator output frequency is internally divided by 13 to produce the machine cycle and by 12 to produce the Timer and the Watchdog clock. A byte cycle is the smallest unit needed to execute any operation (i.e., increment the program counter). An instruction may need two, four, or five byte cycles to be executed (See Table 7).

Figure 27. Clock Generator Options

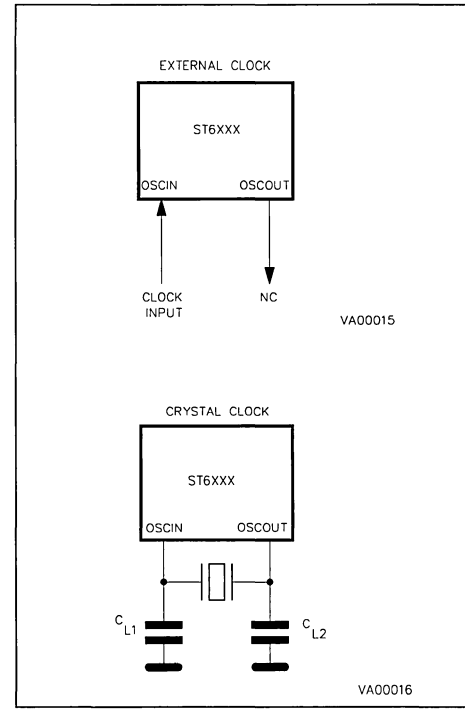
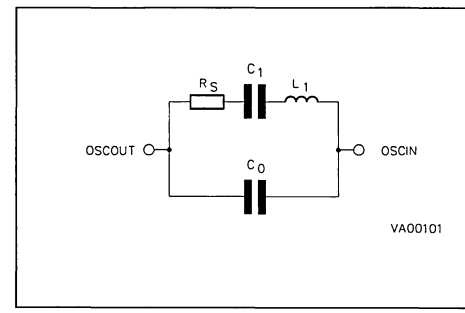


Table 7. Instructions Timing with 8MHz Clock

Instruction Type	Cycles	Execution Time
Branch if set/reset	5 Cycles	8.125µs
Branch & Subroutine Branch	4 Cycles	6.50µs
Bit Manipulation	4 Cycles	6.50µs
Load Instruction	4 Cycles	6.50µs
Arithmetic & Logic	4 Cycles	6.50µs
Conditional Branch	2 Cycles	3.25µs
Program Control	2 Cycles	3.25µs

Figure 28. Crystal Parameters



ON-CHIP CLOCK OSCILLATOR (Continued)

Figure 29. PC Board Layouts Examples

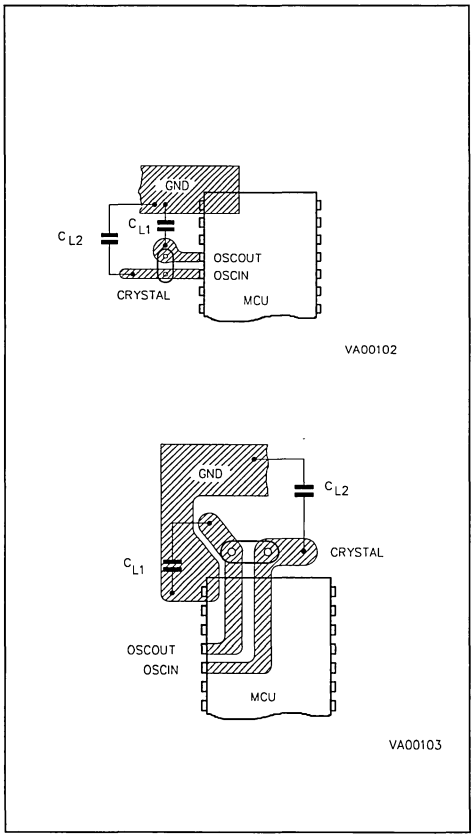
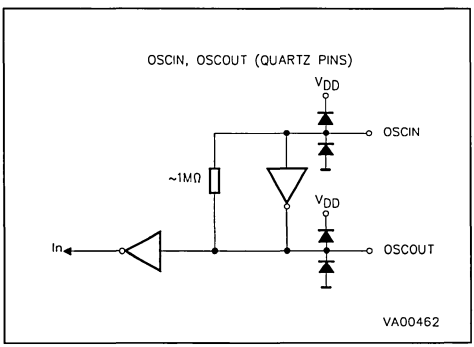


Figure 30. OSCIN, OSCOUT Configuration Diagram



INPUT/OUTPUT PORTS

The ST63XX microcontrollers use three standard I/O ports (A,B,C) with up to eight pins on each port; refer to the device pin configurations to see which pins are available.

Each line can be individually programmed either in the input mode or the output mode as follows by software.

- Output
- Input with on-chip pull-up resistor (selected by software)
- Input without on-chip pull-up resistor (selected by software)

Note: pins with 12V open-drain capability do not have pull-up resistors.

In output mode the following hardware configurations are available:

- Open-drain output 12V (PA0-PA7)
- Open-drain output 5V (PB5-PB7, PC3, PC5-PC7)
- Push-pull output (PB0-PB4, PC0-PC2,PC4)

The lines are organized in three ports (port A,B,C). The ports occupies 6 registers in the data space. Each bit of these registers is associated with a particular line (for instance, the bits 0 of the Port A Data and Direction registers are associated with the PA0 line of Port A).

There are three Data registers (DRA, DRB, DRC), that are used to read the voltage level values of the lines programmed in the input mode, or to write the logic value of the signal to be output on the lines configured in the output mode. The port Data Registers can be read to get the effective logic levels of the pins, but they can be also written by the user software, in conjunction with the related Data Direction Register, to select the different input mode options. Single-bit operations on I/O registers (bit set/reset instructions) are possible but care is necessary because reading in input mode is done from I/O pins and therefore they might be influenced by the external load, while writing will directly affect the Port data register causing an undesired changes of the input configuration. The three Data Direction registers (DDRA, DDRB,DDRB) allow the selection of the direction of each pin (input or output).

All the I/O registers can be read or written as any other RAM location of the data space, so no extra RAM cell is needed for port data storing and manipulation. During the initialization of the MCU, all the I/O registers are cleared and the input mode with pull-up is selected on all the pins thus avoiding pin conflicts (with the exception of PC2 that is set in output mode and is set low).

INPUT/OUTPUT PORTS (Continued)

Details of I/O Ports

When programmed as an input a pull-up resistor (if available) can be switched active under program control. When programmed as an output the I/O port will operate either in the push-pull mode or the open-drain mode according to the hardware fixed configuration as specified below.

Port A is available as an open-drain only (no push-pull programmability and no resistive pull-up in input mode) capable of withstanding 12V while the normal open drain has standard ratings of V_{DD} + 0.3V. This I/O port has been specially designed for direct led driving and is able to sink up to 30mA with a maximum V_{OL} of 1V.

Some Port B and C lines are also used as I/O buffers for signals coming from the on-chip SPI and OSD. In this case the final signal on the output pin is equivalent to a wired AND with the programmed data output. If the user needs to use the SPI or the OSD, then the I/O line should be set in output mode while the open-drain configuration is harware fixed ; the corresponding data bit must set to one.

PB2 and PB3 must be programmed in input mode to provide the HSYNC and VSYNC signal to the OSD.

On ST632X,5X the I/O pins with double or special functions are:

- PB2/VSYNC (connected to the OSD VSYNC signal)
- PB3/HSYNC (connected to the OSD HSYNC signal)
- PB5/SCL (connected to the SPI clock signal)
- PB6/SDA (connected to the SPI data signal)
- PB7/SEN (connected to the SPI enable signal)
- PC2/ON-OFF, this I/O is specially suited for TV SET ON-OFF and for this reason at reset the related Data Direction bit will be automatically set to one (I/O line is in output mode), while the rest of the port is in input mode.
- PC3/BLANK (connected to the OSD Blank signal)
- PC5/R, PC6/G, PC7/B (connected to the OSD R-G-B signals)

All the Port A, B and C I/O lines have Schmitt-trigger input configuration with a typical hysteresis of 1V.

I/O Pin Programming

Each pin can be individually programmed as input or output with different input and output configurations.

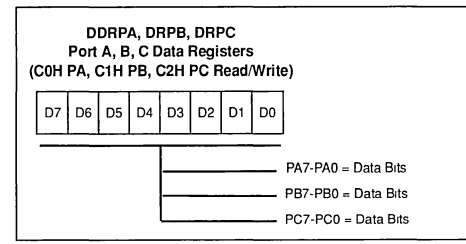
This is achieved by writing to the relevant bit in the data (DR) and data direction register (DDR). Table 8 shows all the port configurations that can be selected by the user software.

Table 8. I/O Port Options Selection

DDR	DR	Mode	Option
0	0	Input	With on-chip pull-up resistor
0	1	Input	Without on-chip pull-up resistor
1	X	Output	Open-drain or Push-Pull

Note. X. Means don't care

Figure 31. I/O Port Data Registers



PA7-PA0. These are the I/O port A data bits with open-drain configuration and high-drive capability. Reset at power on.

PB7/SEN. This is a general purpose open-drain I/O line. The output is the AND between this data bit and the SEN (Enable) signal coming from the SPI peripherals. Reset at power on.

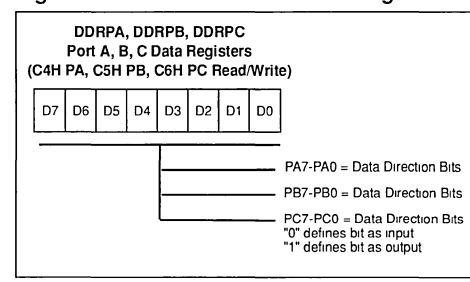
PB6/SDA. This is a general purpose open-drain I/O line. The output is the AND between this data bit and the SDA (Data) signal coming from the SPI peripheral. Reset at power on.

PB5/SCL. This is a general purpose open-drain I/O line. The output is the AND between this data bit and the SCL (Clock) signal coming from the SPI peripheral. Reset at power on.

PC7-PC3,PC1-PC0. These are the I/O port C data bits. Reset at power on.

PC2/ON-OFF. This is a general purpose I/O line suitable for TV set ON-OFF. Reset at power on.

Figure 32. I/O Port Data Direction Registers



INPUT/OUTPUT PORTS (Continued)

PA7-PA0. These are the I/O port A data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Reset at power-on.

PB7-PB0. These are the I/O port B data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Reset at power-on.

PC7-PC0. These are the I/O port C data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Set to 04H at power-on. Bit 2 (PC2 pin) is set to one (output mode selected) as this line is intended for TV ON-OFF switching.

Input/Output Configurations

The following schematics show the I/O lines hardware configuration for the different options. Figure 34 shows the I/O configuration for an I/O pin with open-drain 12V capability (standard drive and high drive). Figure 33 shows the I/O configuration for an I/O pin with push-pull and with open drain 5V capability.

Notes :

The WAIT instruction allows the ST63XX to be used in situations where low power consumption is needed. This can only be achieved however if the I/O pins either are programmed as inputs with well defined logic levels or have no power consuming resistive loads in output mode. As the same die is used for the different ST63XX versions the unavailable I/O lines of ST63XX should be programmed in output mode.

Single-bit operations on I/O registers are possible but **care is necessary** because reading in input mode is done from I/O pins while writing will directly affect the Port data register causing an undesired changes of the input configuration.

Figure 34. Port A I/O Configuration Diagram

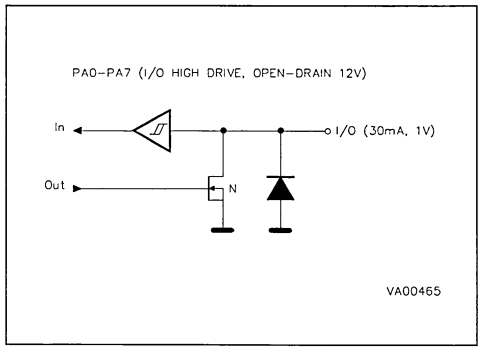
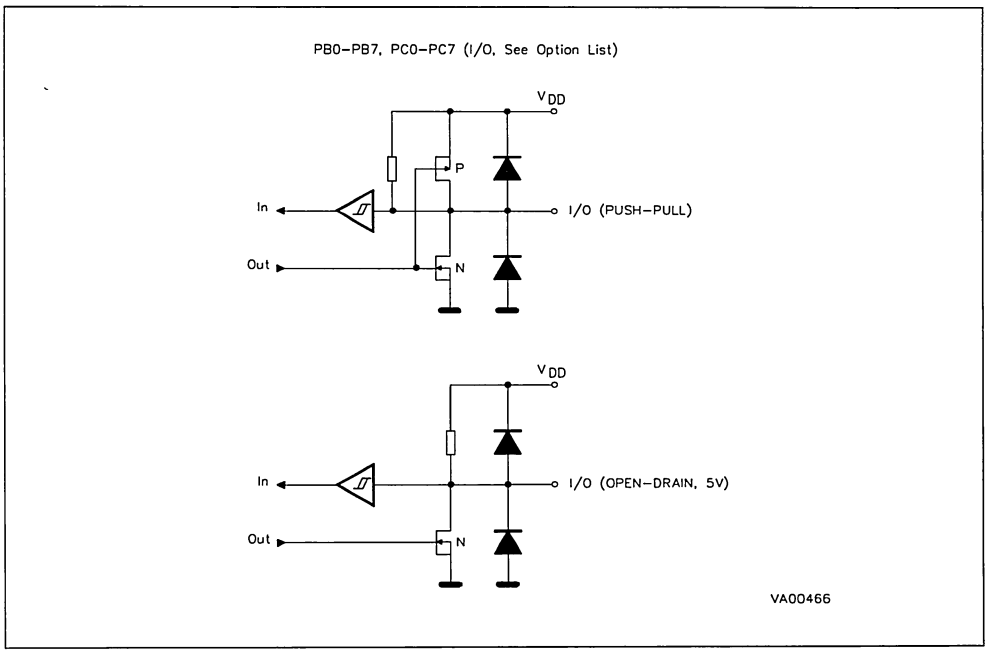


Figure 33. Port B & C I/O Configuration Diagram



TIMERS

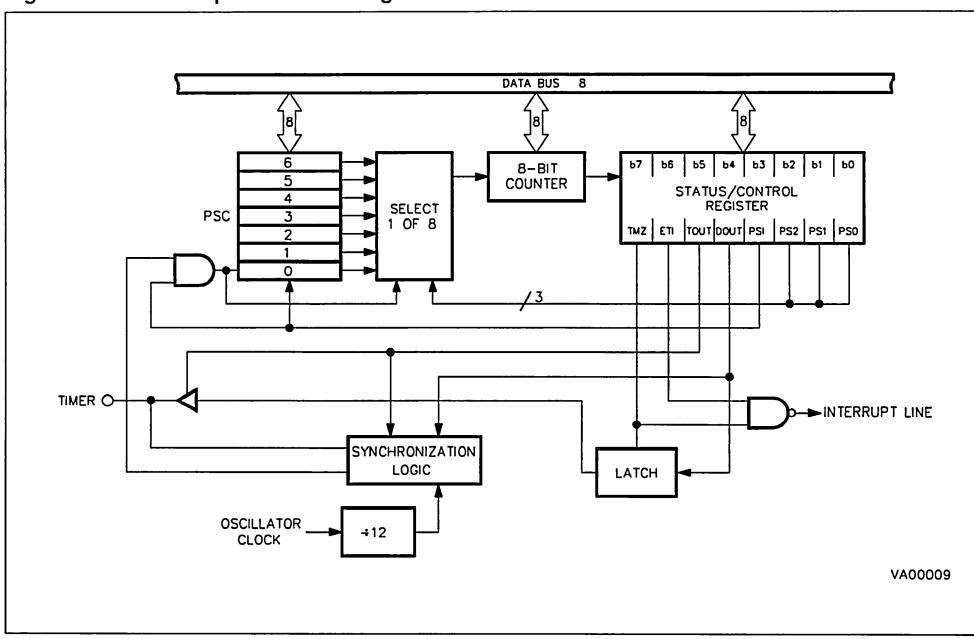
The ST63XX devices offer two on-chip Timer peripherals consisting of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes. Figure 35 shows the timer block diagram. These timers do not have the external TIMER pin available for the user. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR that can be addressed in the data space as RAM location at the D3H (Timer 1) and DBH (Timer 2) addresses. The state of the 7-bit prescaler can be read in the PSC register at the D2H (Timer 1) and DAH (Timer 2) addresses. The control logic device can be managed thanks to the TSCR register D4H (Timer 1) and DCH (Timer 2) addresses as it is described in the following paragraphs.

The following description applies to both Timer 1 and Timer 2. The 8-bit counter is decrement by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (timer zero) bit in the TSCR is set to one. If the ETI (enable timer interrupt) bit in the TSCR is also set to one an interrupt request, associated to interrupt vector #3 (for Timer 1) and #4 for (Timer 2), is generated. The interrupt of the timer can be used to exit the MCU from the WAIT mode.

The prescaler decrements on rising edge. The prescaler input can be the oscillator frequency divided by 12 or an external clock at TIMER pin (this is not available in ST63XX).
Depending on the division factor programmed by PS2/PS1/PS0 (see table 9) bits in the TSCR, the clock input of the timer/counter register is multiplexed to different sources.
On division factor 1, the clock input of the prescaler is also that of timer/counter; on factor 2, bit 0 of prescaler register is connected to the clock input of TCR.

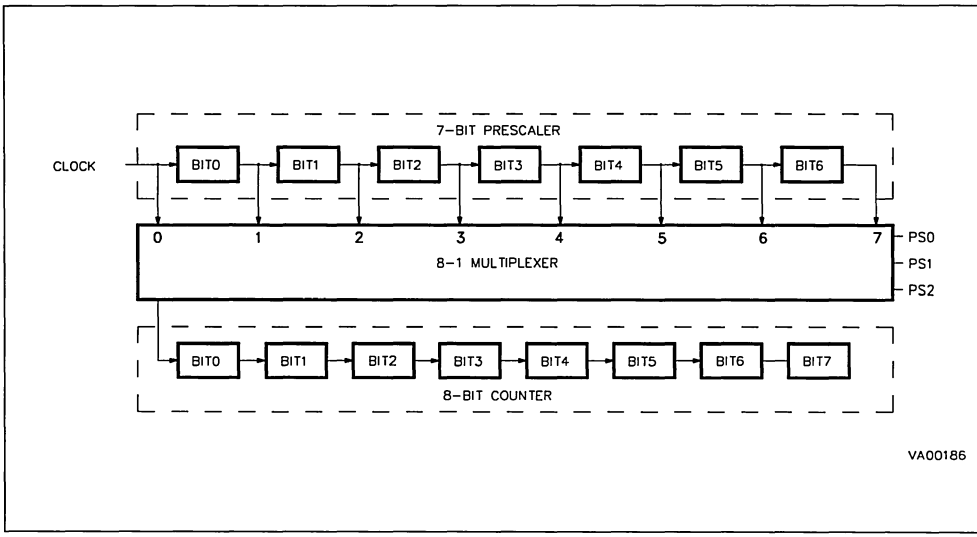
This bit changes its state with the half frequency of prescaler clock input. On factor 4, bit 1 of PSC is connected to clock input of TCR, and so on. On division factor 128, the MSB bit 6 of PSC is connected to clock input of TCR. The prescaler initialize bit (PSI) in the TSCR register must be set to one to allow the prescaler (and hence the counter) to start. If it is cleared to zero then all of the prescaler bits are set to one and the counter is inhibited from counting.

Figure 35. Timer Peripheral Block Diagram



TIMERS (Continued)

Figure 36. Timer Working Principle



The prescaler can be given any value between 0 and 7FH by writing to the related register address, if bit PSI in the TSCR register is set to one. The tap of the prescaler is selected using the PS2/PS1/PS0 bits in the control register. Figure 36 shows the timer working principle.

Timer Operating Modes

As on ST63XX devices the external TIMER pin is not available the only allowed operating mode is the output mode that have to be selected by setting to 1 bit 4 and by clearing to 0 bit 5 in the TSCR1 register. This procedure will enable both Timer 1 and Timer 2. Any other combination written into these two bits will disable any Timer 1 and Timer 2 operation.

Output Mode (TSCR1 D4 = 1, TSCR1 D5 = 0). On this mode the timer prescaler is clocked by the prescaler clock input (OSC/12). The user can select the desired prescaler division ratio through the PS2/PS1/PS0 bits. When TCR count reaches 0, it sets the TMZ bit in the TSCR.

The TMZ bit can be tested under program control to perform a timer function whenever it goes high. Bit D4 and D5 on TSCR2 (Timer 2) register are not implemented.

Timer Interrupt

When the counter register decrements to zero and the software controlled ETI (enable timer interrupt) bit is set to one then an interrupt request associated to interrupt vector #3 (for Timer 1) and to interrupt vector #4 (for Timer 2) is generated. When the counter decrements to zero also the TMZ bit in the TSCR register is set to one.

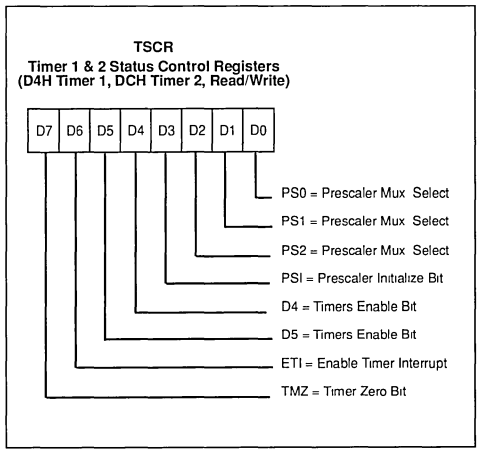
Notes :
TMZ is set when the counter reaches 00H ; however, it may be set by writing 00H in the TCR register or setting the bit 7 of the TSCR register. TMZ bit must be cleared by user software when servicing the timer interrupt to avoid undesired interrupts when leaving the interrupt service routine. After reset, the 8-bit counter register is loaded to FFH while the 7-bit prescaler is loaded to 7FH , and the TSCR register is cleared which means that timer is stopped (PSI=0) and timer interrupt disabled.

A write to the TCR register will predominate over the 8-bit counter decrement to 00H function, i.e. if a write and a TCR register decrement to 00H occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter reaches 00H again. The values of the TCR and the PSC registers can be read accurately at any time.

TIMERS (Continued)

Timer Registers

Figure 37. Timer Status Control Registers



TMZ. Low-to-high transition indicates that the timer count register has decrement to zero. This bit must be cleared by user software before to start with a new count.

ETI. This bit, when set, enables the timer interrupt (vector #3 for Timer 1, vector #4 for Timer 2) request. If ETI=0 the timer interrupt is disabled. If ETI= 1 and TMZ= 1 an interrupt request is generated.

D5. This is the timers enable bit D5. It must be cleared to 0 together with a set to 1 of bit D4 to enable both Timer 1 and Timer 2 functions. It is not implemented on TSCR2 register. Any other combination of TSCR1 D4 and D5 bits will disable any operation of both Timer 1 and Timer 2.

D4. This is the timers enable bit D4. It must be set to 1 together with a clear to 0 of bit D5 to enable both Timer 1 and Timer 2 functions. It is not implemented on TSCR2 register. Any other combination of TSCR1 D4 and D5 bits will disable any operation of both Timer 1 and Timer 2.

PSI. Used to initialize the prescaler and inhibit its counting while PSI = 0 the prescaler is set to 7FH and the counter is inhibited. When PSI = 1 the prescaler is enabled to count downwards. As long as PSI= 0 both counter and prescaler are not running.

PS2-PS0. These bits select the division ratio of the prescaler register. (see table 9)

The TSCR1 and TSCR2 registers are cleared on reset. The correct D4-D5 combination must be written in TSCR1 by user's software to enable the operation of Timer 1 and Timer 2.

Table 9. Prescaler Division Factors

PS2	PS1	PS0	Divided By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Figure 38. Timer Counter Registers

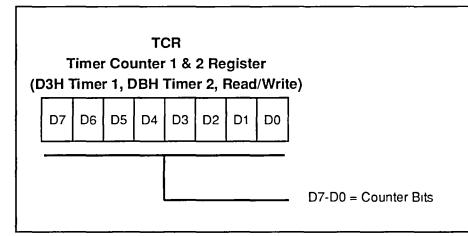
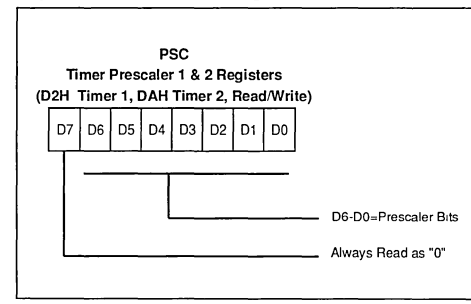


Figure 39. Prescaler Registers



HARDWARE ACTIVATED DIGITAL WATCHDOG FUNCTION

The hardware activated digital watchdog function consists of a down counter that is automatically initialized after reset so that this function does not need to be activated by the user program. As the watchdog function is always activated this down counter can't be used as a timer. The watchdog is using one data space register (HWDR location D8H). The watchdog register is set to FEH on reset and immediately starts to count down, requiring no software start. Similarly the hardware activated watchdog can not be stopped or delayed by software.

The watchdog time can be programmed using the 6 MSbits in the watchdog register, this gives the possibility to generate a reset in a time between 3072 to 196608 oscillator cycles in 64 possible steps. (With a clock frequency of 8MHz this means from 384µs to 24.576ms). The reset is prevented if the register is reloaded with the desired value before bits 2-7 decrement from all zeros to all ones.

The presence of the hardware watchdog deactivates the STOP instruction and a WAIT instruction is automatically executed instead of a STOP. Bit 1 of the watchdog register (set to one at reset) can be used to generate a software reset if cleared to zero). Figure 40 shows the watchdog block diagram while Figure 41 shows its working principle.

Figure 41. Hardware Activated Watchdog Working Principle

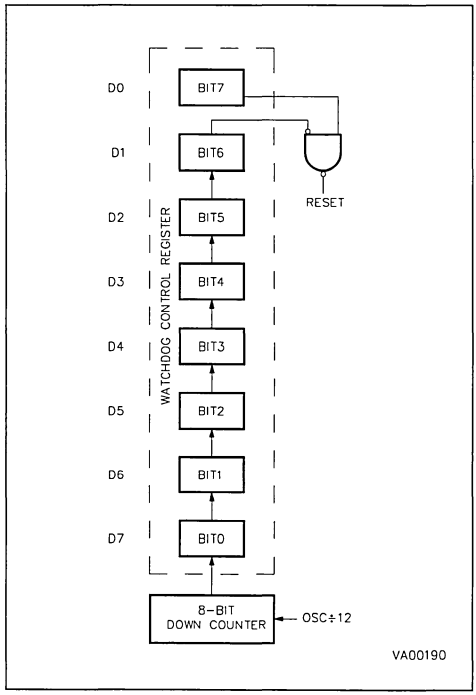
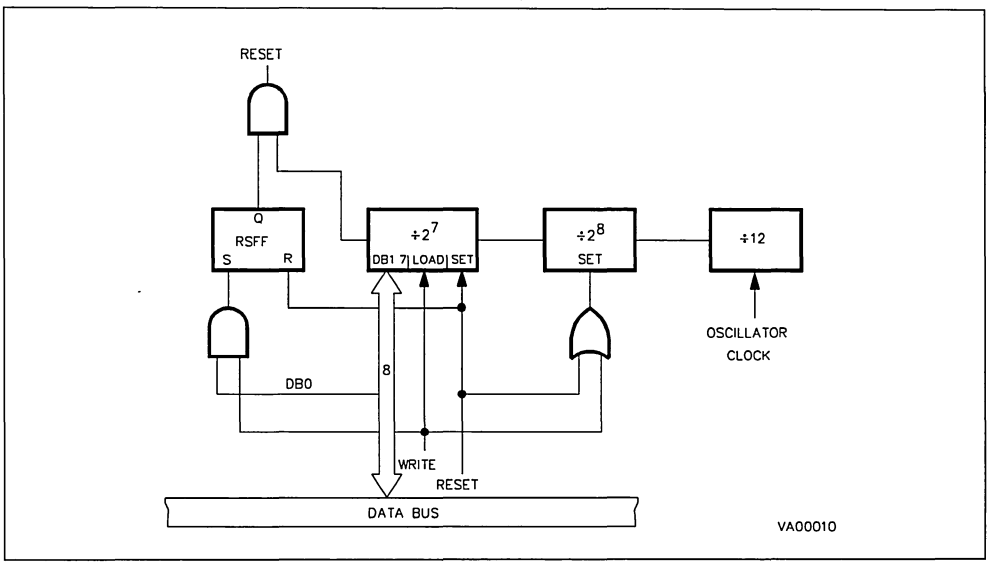
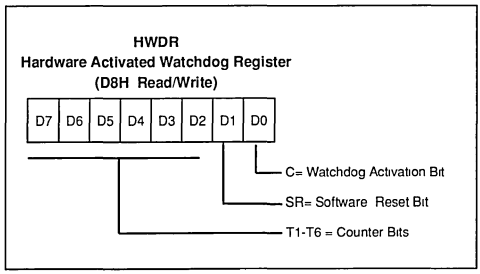


Figure 40. Hardware Activated Watchdog Block Diagram



HARDWARE ACTIVATED DIGITAL WATCHDOG FUNCTION (Continued)

Figure 42. Watchdog Register



T1-T6. These are the watchdog counter bits. It should be noted that D7 (T1) is the LSB of the counter and D2 (T6) is the MSB of the counter, these bits are in the opposite order to normal.

SR. This bit is set to one during the reset phase and will generate a software reset if cleared to zero.

C. This is the watchdog activation bit that is hardware set to one; the user can't change the value of this bit (the watchdog is always active).

The register reset value is FEH (Bit 1-7 set to one, Bit 0 cleared).

SERIAL PERIPHERAL INTERFACE

The ST63XX Serial Peripheral Interface macrocell (SPI) has been designed to be cost effective and flexible in interfacing the various peripherals in TV applications.

It maintains the software flexibility but adds hardware configurations suitable to drive devices which require a fast exchange of data. The three pins dedicated for serial data transfer (single master only) can operate in the following ways:

- as standard I/O lines (software configuration)
- as S-BUS or as I^2CBUS (two pins)
- as standard (shift register) SPI

When using the hardware SPI, a fixed clock rate of 62.5kHz is provided.

It has to be noted that the first bit that is output on the data line by the 8-bit shift register is the MSB.

SPI Data/Control Registers

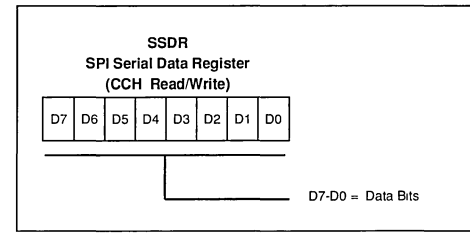
For I/O details on SCL (Serial Clock), SDA (Serial Data) and SEN (Serial Enable) please refer to I/O Ports description with reference to the following registers:

Port B data register, Address C1H (Read/Write).

- BIT D5 "SCL"
- BIT D6 "SDA"
- BIT D7 "SEN"

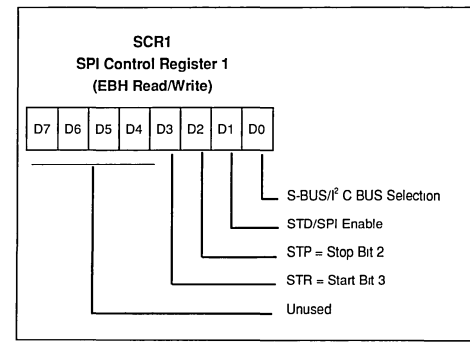
Port B data direction register, Address C5H (Read/Write).

Figure 43. SPI Serial Data Register



D7-D0. These are the SPI data bits. They can be neither read nor written when SPI is operating (BUSY bit set). They are undefined after reset.

Figure 44. SPI Control Register 1



D7-D4. These bits are not used.

STR. This is Start bit for $I^2CBUS/S\text{-}BUS$. This bit is meaningless when STD/SPI enable bit is cleared to zero. If this bit is set to one STD/SPI bit is also set to "1" and SPI Start generation, before beginning of transmission, is enabled. Set to zero after reset.

STP. This is Stop bit for $I^2CBUS/S\text{-}BUS$. This bit is meaningless when STD/SPI enable bit is cleared to zero. If this bit is set to one STD/SPI bit is also set to "1" and SPI Stop condition generation is enabled. STP bit must be reset when standard protocol is used (this is also the default reset conditions). Set to zero after reset.

SERIAL PERIPHERAL INTERFACE (Continued)

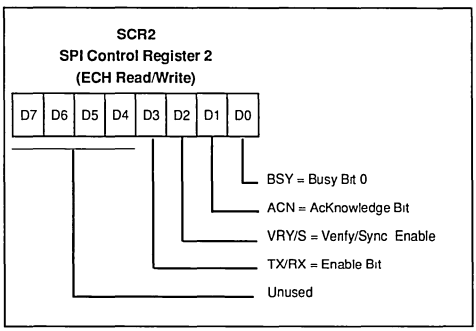
S-BUS/I²CBUS Selection. This bit, in conjunction with STD/SPI bit, allows the SPI disable and will select between I²CBUS and S-BUS protocols. If this bit is cleared to "0" when STD bit is also "0", the SPI interface is disabled. If this bit is cleared to zero when STD bit is set to "1", the I²CBUS protocol will be selected. If this bit is set to one when STD bit is set to "1", the S-BUS protocol will be selected. Cleared to zero after reset.

STD, SPI Enable. This bit, in conjunction with S-BUS/I²CBUS bit, allows the SPI disable and will select between I²CBUS/S-BUS and Standard shift register protocols. If this bit is set to one, it selects both I²CBUS and S-BUS protocols; final selection between them is made by S-BUS/I²CBUS bit. If this bit is cleared to zero when S-BUS/I²CBUS is set to "1" the Standard shift register protocol is selected. If this bit is cleared to "0" when S-BUS/I²CBUS is cleared to 0 the SPI is disabled. Set to zero after reset.

Table 10. SPI Modes Selection

D0 S-Bus/I²CBUS	D1 STD/SPI	SPI Function
0	0	Disabled
1	0	STD Shift Register
0	1	I²CBUS
1	1	S-BUS

Figure 45. SPI Control Register 2



D7-D4. These bits are not used.

TX/RX. *Write Only.* When this bit is set, current byte operation is a transmission. When it is reset, current operation is a reception. Set to zero after reset.

VRY/S. *Read Only/Write Only.* This bit has two different functions in relation to read or write operation. *Reading Operation:* when STD and/or TRX bits are cleared to 0, this bit is meaningless. When bits STD and TX are set to 1, this bit is set each time BSY bit is set. This bit is reset during byte operation if real data on SDA line are different from the ones output from the shift register. Set to zero after reset. *Writing Operation* : it enables (if set to one) or disables (if cleared to zero) the interrupt coming from VSYNC pin. Undefined after reset. Refer to OSD description for additional information.

ACN. *Read Only.* If STD bit (D1 of SCR1 register) is cleared to zero this bit is meaningless. When STD is set to one, this bit is set to one if no Acknowledge has been received. In this case it is automatically reset when BSY is set again. Set to zero after reset.

BSY. *Read/Set Only.* This is the busy bit zero. When a one is loaded into this bit the SPI interface start the transmission of the data byte loaded into SSDR data register or receiving and building the receive data into the SSDR data register. This is done in accordance with protocol, direction and start/stop condition(s). This bit is automatically cleared at the end of the current byte operation. Cleared to zero after reset.

Note :
The SPI shift register is also the data transmission register and the data received register; this new feature is made possible by using the serial structure of the ST63XX and thus reducing size and complexity.

During transmission or reception of data, all access to serial data register is therefore disabled. The reception or transmission of data is started by setting the BUSY bit to "1"; this will be automatically reset at the end of the operation. After reset, the busy bit is cleared to "0", and the hardware SPI disabled by clearing bit 0 and bit 1 of SPI control register 1 to "0". The outputs from the harware SPI are "ANDed" to the standard I/O software controlled outputs. If the hardware SPI is in operation then Port B ouputs related to the SPI should be set high or the pins should pin configured as inpus using the data direction register. When the SPI is configured as the S-BUS, the three pins PB5, PB6 and PB7 become the pins SCL, SDA and SEN respectively. When configured as the I²CBUS the pins PB5 and PB6 are configured as the pins SCL and SDA; PB7 is not driven and can be used as general purpose I/O pin. In the case of the STDSPI the pins PB5 and PB6 become the signals CLOCK and DATA, PB7 is not driven and can be used as general purpose I/O pin. The VERIFY bit is available when the SPI is configured as either S-BUS or I²CBUS. At the start of a byte transmission, the verify bit is set to one. If at any time during the transmission of the

SERIAL PERIPHERAL INTERFACE (Continued)

following eight bits, the data on the SDA line does not match the data forced by the SPI (while SCL is high), then the VERIFY bit is reset. The verify is available only during transmission for the S-BUS and I²CBUS; for other protocol it is not definfited. The SDA and SCL signal entering the SPI are buffered in order to remove any minor glitches. When STD bit is set to one (S-BUS or I²CBUS selected), and TRX bit is reset (receiving data), and STOP bit is set (last byte of current communication), the SPI interface does not generate the Acknowledge, according to S-BUS/I²CBUS specifications. PB5-SCL, PB6-SDA and PB7-SEN lines are standard drive I/O port pins with open-drain output configuration (maximum voltage that can be applied to these pins is V_{DD}+ 0.3V).

S-BUS/I²CBUS Protocol Information

The S-BUS is a three-wire bidirectional data-bus with functional features similar to the I²CBUS. In fact the S-BUS includes decoding of Start/Stop conditions and the arbitration procedure in case of multimaster system configuration (the ST63XX SPI allows a single-master only operation). The SDA line, in the I²CBUS represents the AND combination of SDA and SEN lines in the S-BUS. If the SDA and the SEN lines are short-circuit connected, they appear as the SDA line of the I²CBUS. The Start/Stop conditions are detected (by the external peripherals suited to work with S-BUS/I²CBUS) in the following way:

- On S-BUS by a transition of the SEN line (1 to 0 Start, 0 to 1 Stop) while the SCL line is at high level.
- On I²CBUS by a transition of the SDA line (10 Start, 01Stop) while the SCL line is at high level.

Start and Stop condition are always generated by the master (ST63XX SPI can only work as single master). The bus is busy after the start condition and can be considered again free only when a certain time delay is left after the stop condition. In the S-BUS configuration the SDA line is only allowed to change during the time SCL line is low. After the start information the SEN line returns to high level and remains unchanged for all the data transmission time. When the transmission is completed the SDA line is set to high level and, at the same time, the SEN line returns to the low level in order to supply the stop information with a low to high transition, while the SCL line is at high level. On the S-BUS, as on the I²CBUS, each eight bit information (byte) is followed by one acknowledged bit which is a high level put on the SDA line by the transmitter. A peripheral that acknowledges has to pull down the SDA line during the acknowledge clock pulse. An addressed receiver has to generate an acknowledge after the reception of each byte; otherwise the SDA line remains at the high level during the ninth clock pulse time. In this case the master transmitter can generate the Stop condition, via the SEN (or SDA in I²CBUS) line, in order to abort the transfer.

Start/Stop Acknowledge. The timing specs of the S-BUS protocol require that data on the SDA (only on this line for I²CBUS) and SEN lines be stable during the "high" time of SCL. Two exceptions to this rule are foreseen and they are used to signal the start and stop condition of data transfer.

- On S-BUS by a transition of the SEN line (10 Start, 01 Stop) while the SCL line is at high level.
- On I²CBUS by a transition of the SDA line (10 Start, 01 Stop) while the SCL line is at high level.

Data are transmitted in 8-bit groups; after each group, a ninth bit is interposed, with the purpose of acknowledging the transmitting sequence (the transmit device place a "1" on the bus, the acknowledging receiver a "0").

Interface Protocol. This paragraph deals with the description of data protocol structure. The interface protocol includes:

- A start condition

- A "slave chip address" byte, transmitted by the master, containing two different information:

a. the code identifying the device the master wants to address (this information is present in the first seven bits)

b. the direction of transmission on the bus (this information is given in the 8th bit of the byte); "0" means "Write", that is from the master to the slave, while "1" means "Read". The addressed slave must always acknowledge.

The sequence from, now on, is different according to the value of R/$\overline{W}$ bit.

1. R/$\overline{W}$ = "0" ($\overline{\text{Write}}$)

In all the following bytes the master acts as transmitter; the sequence follows with:

a. an optional data byte to address (if needed) the slave location to be written (it can be a word address in a memory or a register address, etc.).

b. a "data" byte which will be written at the address given in the previous byte.

c. further data bytes.

d. a STOP condition

A data transfer is always terminated by a stop condition generated from the master. The ST63XX peripheral must finish with a stop condition before another start is given. Figure 46 shows an example of write operation.

2. R/$\overline{W}$ = "1" (Read)

In this case the slave acts as transmitter and, therefore, the transmission direction is changed. In read mode two different conditions can be considered:

SERIAL PERIPHERAL INTERFACE (Continued)

a. The master reads slave immediately after first byte. In this case after the slave address sent from the master with read condition enabled the master transmitter becomes master receiver and the slave receiver becomes slave transmitter.

b. The master reads a specified register or location of the slave. In this case the first sent byte will contain the slave address with write condition enabled, then the second byte will specify the address of the register to be read. At this moment a new start is given together with the slave address in read mode and the procedure will proceed as described in previous point "a".

Figure 46. Master Transmit to Slave Receiver (Write Mode)

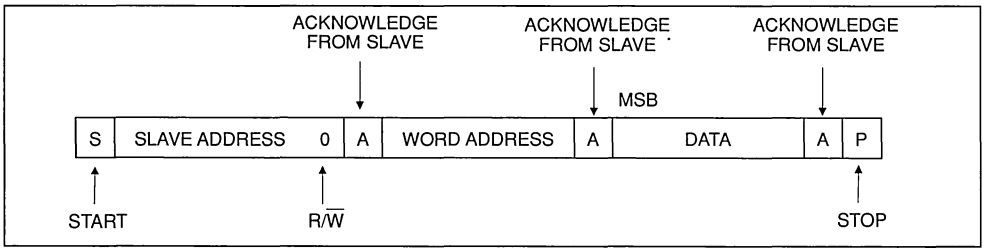


Figure 47. Master Reads Slave Immediately After First Byte (read Mode)

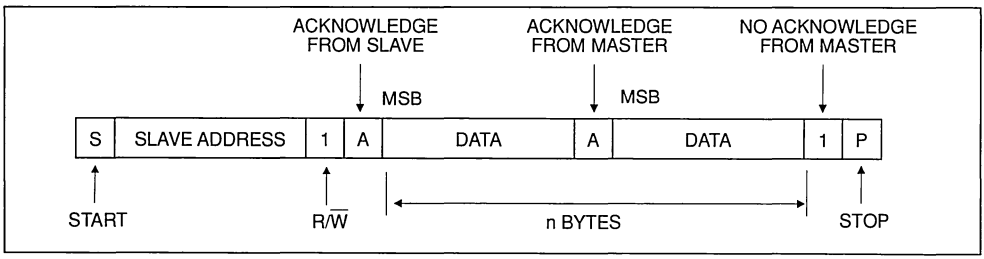
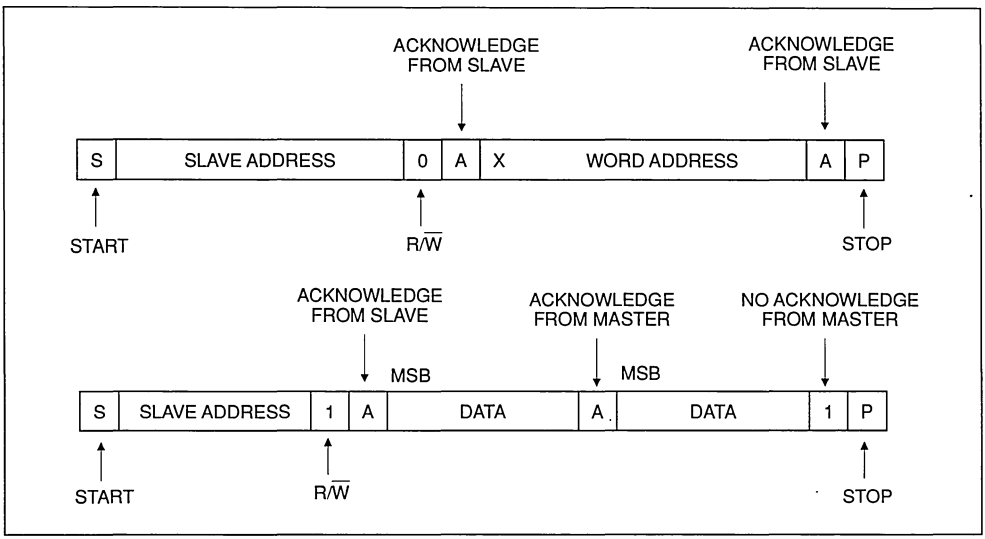


Figure 48. Master Reads After Setting Slave Register Address (Write Address, Read Data)

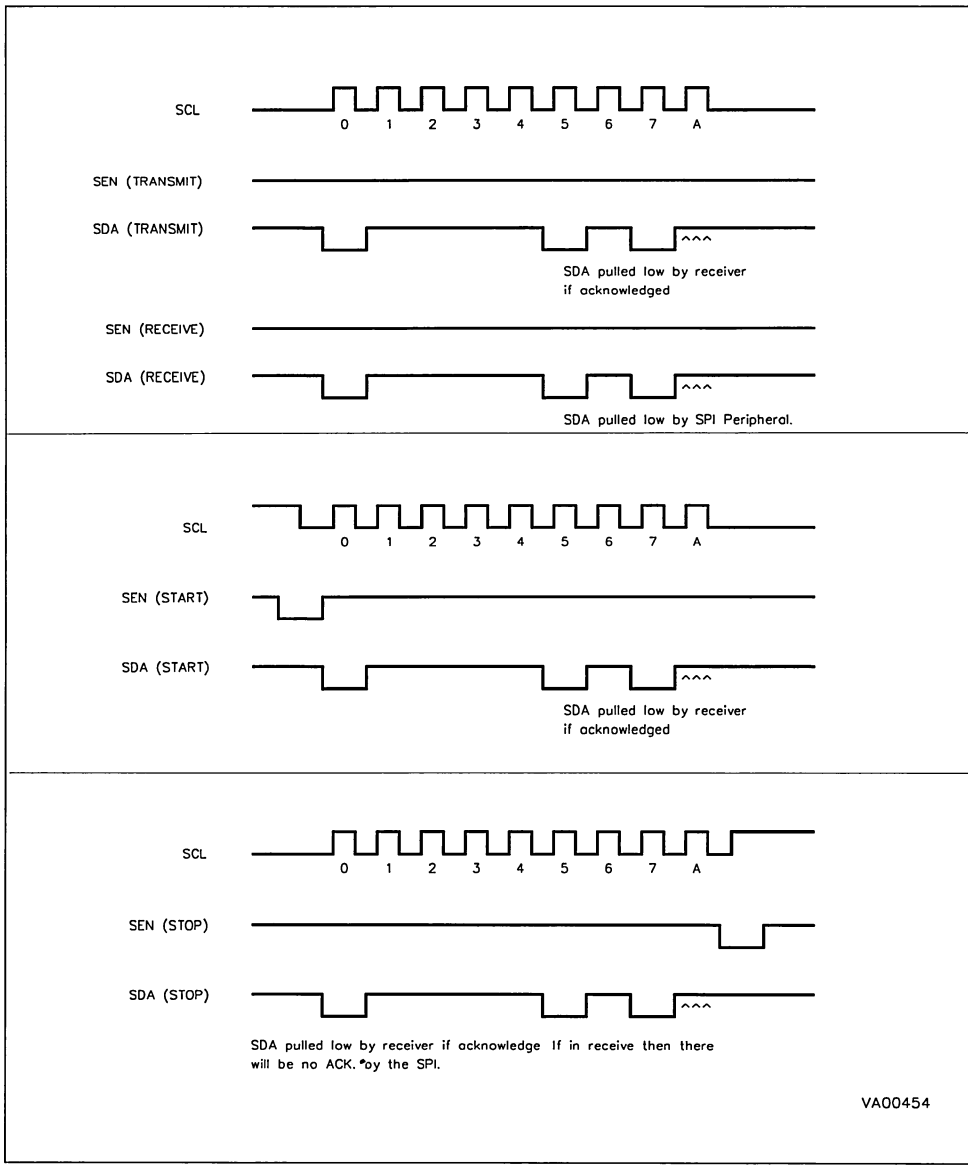


SERIAL PERIPHERAL INTERFACE (Continued)

S-BUS/I²CBUS Timing Diagrams

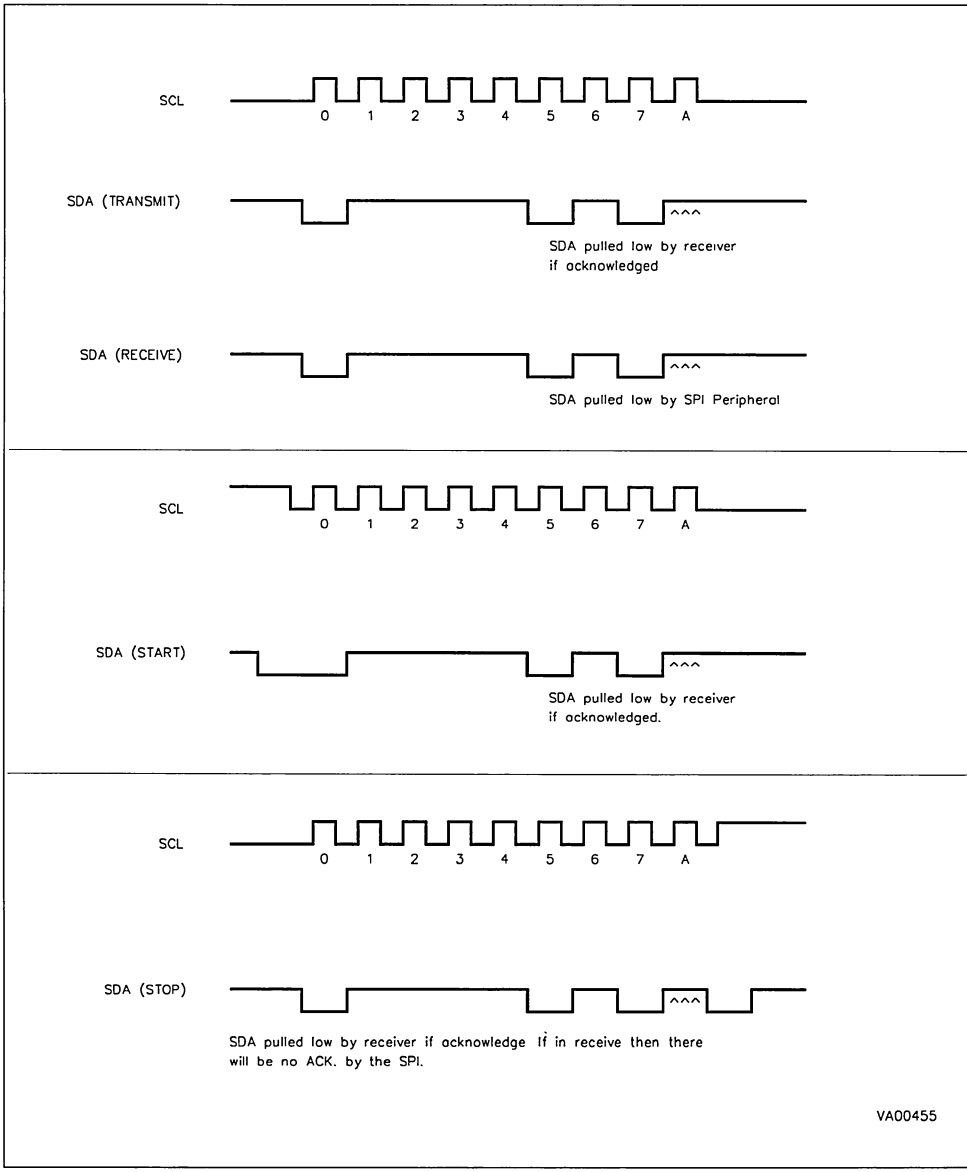
The clock of the S-BUS/I²CBUS of the ST63XX SPI (single master only) has a fixed bus clock frequency of 62.5KHz. All the devices connected to the bus must be able to follow transfers with frequencies up to 62.5KHz, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure which will force the master into a wait state and stretch low periods.

Figure 49. S-BUS Timing Diagrams



SERIAL PERIPHERAL INTERFACE (Continued)

Figure 50. I²C BUS Timing Diagrams



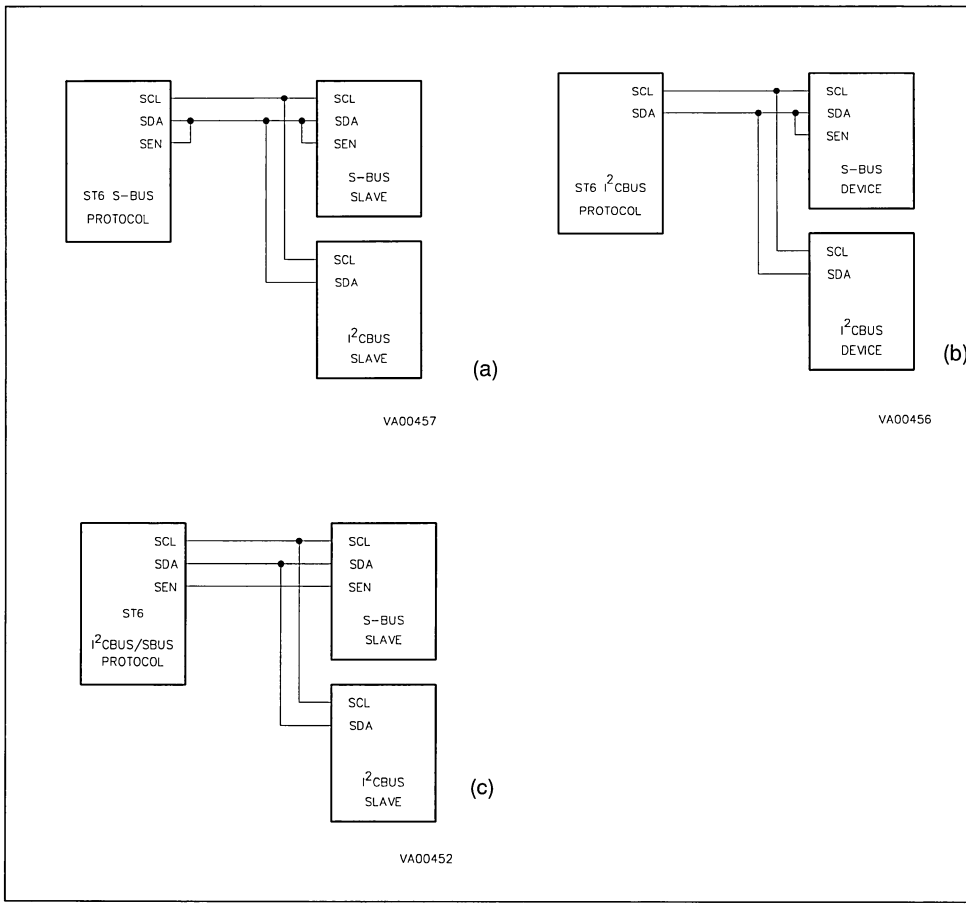
Note: The third pin, SEN, should be high; it's not used in the I²CBUS. Logically SDA is the AND of the S-BUS SDA and SEN.

SERIAL PERIPHERAL INTERFACE (Continued)

Compatibility S-BUS/I²CBUS

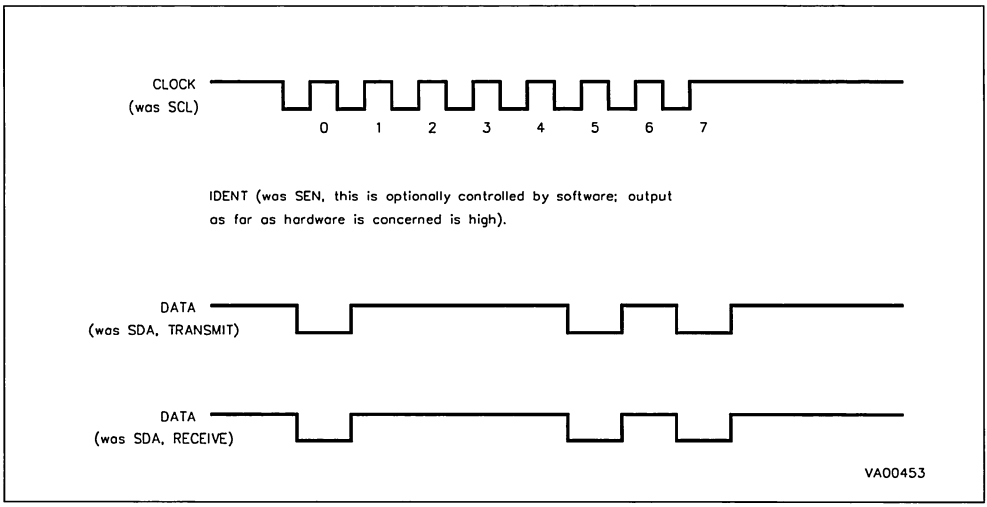
Using S-BUS protocol it is possible to implement mixed system including S-BUS/I²CBUS bus peripherals. In order to have the compatibility with the I²CBUS peripherals, the devices including the S-BUS interface must have their SDA and SEN pins connected together as shown in the following Figure 51 (a and b). It is also possible to use mixed S-BUS/I²CBUS protocols as showed in figure 51 (c). S-BUS peripherals will only react to S-BUS protocol signals, while I²CBUS peripherals will only react to I²CBUS signals. Multimaster configuration is not possible with ST63XX SPI (single master only).

Figure 51. S-BUS/I²C BUS Mixed Configurations



SERIAL PERIPHERAL INTERFACE (Continued)

Figure 52. STD Bus (hardware bus disabled) Timing Diagram



STD SPI Protocol (Shift Register)

This protocol is similar to the I^2CBUS with the exception that there is no acknowledge pulse and there are no stop or start bits. The clock cannot be slowed down by the external peripherals.

The I/O ports associated with the SPI should be programmed as outputs with data high in order not to inhibit the functionality of the hardware SPI.

SPI APPLICATION NOTES

Stop Clock Slowdown: In the ST63XX family of devices when operating in the I^2C or SBUS modes, there is no internal clock slowdown for the final STOP clock. Slowdown means that if an external peripheral requires extra time it will hold the ST63XX SCL clock low. To be fully I^2C and SBUS compatible in this respect, the SW should check that the SCL line is indeed high before proceeding with the START of another I^2C or SBUS transmission. In all other cases the SCL clock slowdown feature is operational.

SPI Standard Bus Protocol: The standard bus protocol is selected by loading the SPI Control Register 1 (SCR1 Add. EBH). Bit 0 named I^2C must be set at one and bit 1 named STD must be reset. When the standard bus protocol is selected bit 2 of the SCR1 is meaningless.
This bit named STOP bit is used only in I^2CBUS or SBUS. However take care that the *STOP BIT MUST BE RESET WHEN THE STANDARD PROTOCOL IS USED.* This bit is set to ZERO after RESET.

6-BIT PWM D/A CONVERTERS AND 62.5 KHz OUTPUT FUNCTION

The D/A macrocell contains four PWM D/A outputs (32Khz repetition, DA0-DA3) with six bit resolution plus a 62.5KHz open-drain output pin (OUT1) specially suited for multistandard chroma processors driving. Both the D/A and OUT1 functions can be disabled by software allowing the DA0-DA3 and OUT1 pins to be used as general purpose open-drain output pins able to withstand signals with up to 12V amplitude.

6-Bit D/A Converters

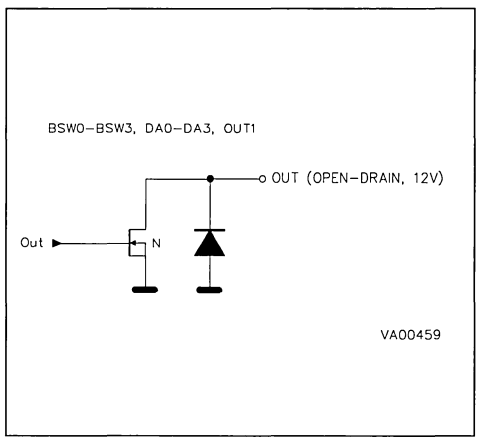
Each D/A converter of ST63XX is composed by the following main blocks:

- pre-divider
- 6-bit counter
- data latches and compare circuits

The pre-divider uses the clock input frequency (8MHz) and its output clocks the 6-bit free-running counter. The data latched in the four registers (E0H, E1H, E2H and E3H) control the four D/A outputs (DA0,1,2 and 3). When all zeros are loaded the relevant output is an high logic level; all 1's correspond to a pulse with a 1/64 duty cycle and almost 100% zero level. A 7th bit (bit D6) is used to enable the relevant D/A output; when zero, the D/A is no longer enabled and it forces the output to zero. If the other six bits are all zero then the output is controlled only by the enable bit.

he repetition frequency is 32.5KHz and is related to the 8MHz clock frequency. All D/A outputs are open-drain with standard current drive capability and able to withstand up to 12V.

Figure 53. 6-BIT PWM D/A & 62.5KHz Output Configuration



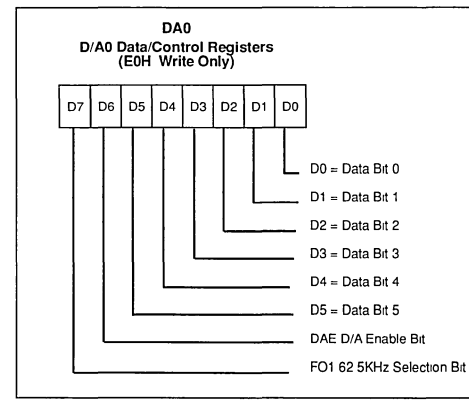
62.5 KHZ Output

This pin provides a 62.5 KHz signal with a 50% duty cycle; the output is enabled by a dedicated enable bit (E0H register bit 7). When the 62.5KHz frequency is disabled then the output is controlled by the OUT1 bit and the line can be used as general purpose open-drain output (E1H bit 7). The OUT1 output is open-drain with standard current drive capability and able to withstand signals with up to 12V amplitude. The pin can be used to drive the SGS-THOMSON TEA5640 chroma processor. Refer to the TEA5640 data sheet for more information on the use of this pin. Care must be taken to respect the frequency tolerances required by the TEA5640 by chosing a quartz with PPM variations within the limits required by the chroma processor.

D/A and OUT1 Data/Control Registers

This paragraph deals with the description of D/A and OUT1 data/control registers. Some bits of DA2 and DA3 data/control registers are used for external interrupt enable and A/D reference voltage shift, please refer to A/D and IR descriptions for additional information.

Figure 54. D/A0 Data/Enable Register



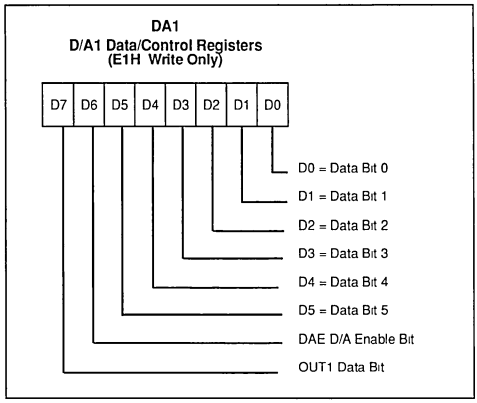
DA0-DA5. These are the 6 bits of the PWM digital to analog converter . Undefined after reset.

DAE. This is the D/A 0 enable bit. If zero, the output of the D/A is forced to zero; if one, the output of the D/A depends on bits DA0..DA5. Undefined after reset.

FO1. This is the 62.5KHz frequency output/ OUT1 selection bit. If one, the OUT1 pin will give a 62.5KHz frequency; if zero the OUT1 pin can be used as general purpose open-drain output and the value present on the pin depends on the value of OUT1 bit programmed in the DA1 data/control register. Undefined after reset.

6-BIT PWM D/A CONVERTERS AND 62.5 KHz OUTPUT FUNCTION (Continued)

Figure 55. D/A1 Data/Enable Register

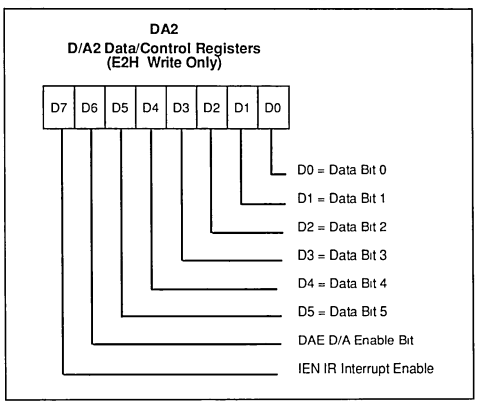


DA0-DA5. These are the 6 bits of the PWM digital to analog converter. Undefined after reset.

DAE. This is the D/A 1 enable bit. If zero, the output of the D/A is forced to zero; if one, the output of the D/A depends on bits DA0..DA5. Undefined after reset.

OUT1. This is the OUT1 data bit. The content of this bit is output on the OUT1 pin when the 62.5KHz frequency function is disabled (FO1 bit in DA0 register is cleared to zero). Undefined after reset.

Figure 56. D/A2 Data/Enable Register

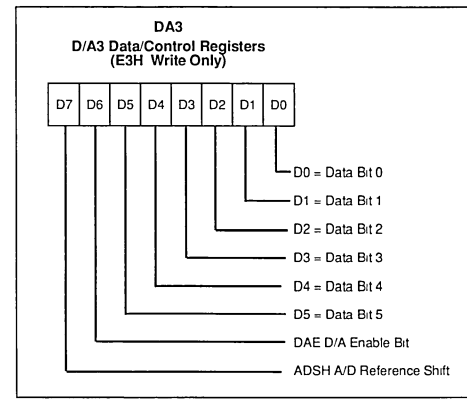


DA0-DA5. These are the 6 bits of the PWM digital to analog converter bits. Undefined after reset.

DAE. This is the D/A 2 enable bit. If zero, the output of the D/A is forced to zero; if one, the output of the D/A depends on bits DA0..DA5. Undefined after reset.

IEN. This is the external interrupt enable. If set to one, the interrupt coming from the external interrupt pin is enabled, if this bit is cleared the interrupt is disabled. Undefined after reset. This interrupt is associated to the NMI interrupt vector. Refer to IR and interrupt descriptions for additional information.

Figure 57. D/A3 Data/Enable Register



DA0-DA5. These are the 6 bits of the PWM digital to analog converter. Undefined after reset.

DAE. This is the D/A 3 enable bit. If zero, the output of the D/A is forced to zero; if one, the output of the D/A depends on bits DA0..DA5. Undefined after reset.

ADSH. This is the analog to digital converter reference voltage shift bit. If set to one, the AFC block has reference voltages on 1V border. If set to zero, on 0.5V border. Undefined after reset. Refer to AFC for additional information.

AFC A/D INPUT, KEYBOARD INPUTS AND BANDSWITCH OUTPUTS

The AFC macrocell contains an A/D comparator with five levels at intervals of 1V from 1V to 5V. The levels can all be lowered by 0.5v to effectively double the resolution. This A/D can be used to perform the AFC function. In addition this cell offers also a keyboard input register of three bits used to perform a keyboard scan and 4 open-drain outputs (able to withstand signals up to 12V) that can be used to perform band switch function.

Figure 58. AFC, KBY Inputs Configuration Diagrams

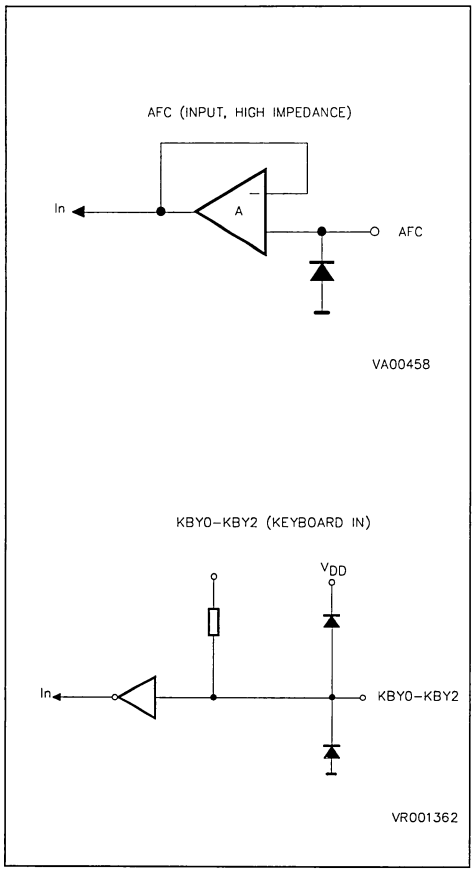
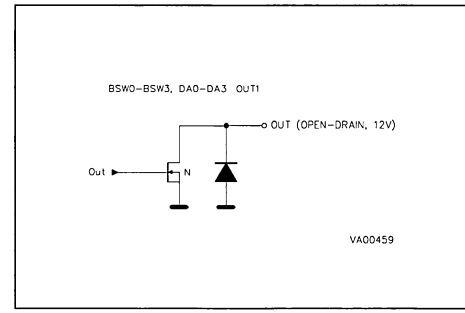


Figure 59. BSW, DA, OUT1 Output Configuration Diagram



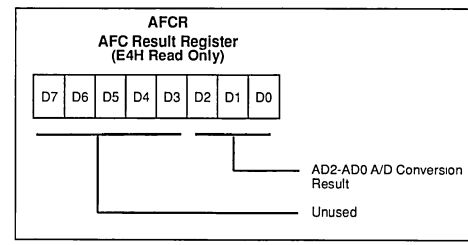
A/D Comparator

The A/D used to perform the AFC function (when high threshold is selected) has the following voltage levels: 1,2,3,4 and 5V. Bits 0-2 of AFC result register (E4H address) will provide the result in binary form (less than 1V is 000, greater than 5V is 101).

If the application requires a greater resolution, the sensitivity can be doubled by clearing to zero bit 7 of DA3 Data/Control register, address E3H (refer to D/A description for additional information). In this case all levels are shifted lower by 0.5V. If the two results are now added within a software routine then the A/D S-curve can be located within a resolution of 0.5V. The A/D input has high impedance able to withstand up to 13V signals (input level tolerances ± 200mv absolute and ± 100mv relative to 5V).

AFC, Keyboard Inputs and Bandswitch Outputs Data/Control Registers

Figure 60. AFC Result Register

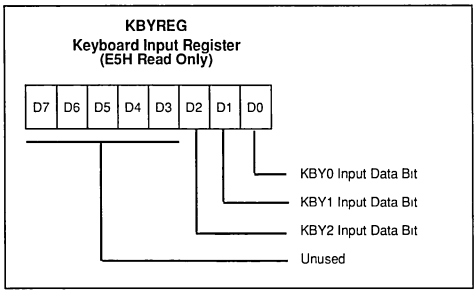


D7-D3. These bits are not used.

AD0-AD2. These bits store the real time conversion of the value present on the AFC input pin. No reset value.

AFC A/D INPUT, KEYBOARD INPUTS AND BANDSWITCH OUTPUTS (Continued)

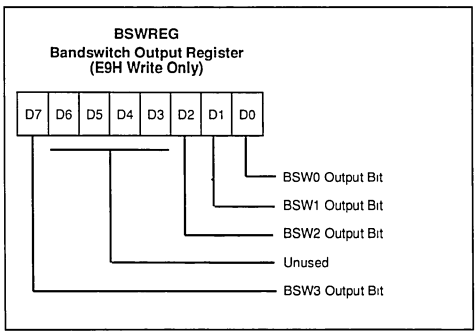
Figure 61. Keyboard Input Register



D7-D3. These bits are not used.

KBY0-KBY2. These bits store the logic level present at KBY0, KBY1 and KBY2 input pins. No reset value. This input pins have CMOS levels with on-chip pull-up resistor (100Kohm typical).

Figure 62. Bandswitch Output Register



D6-D3. These bits are not used.

BSW0-BSW2,BSW3. The writing into these bits will cause the corresponding BSW open-drain output line to switch to the programmed level. Undefined after reset.

INFRARED INPUT (IRIN)

The IRIN pin is directly connected to the NMI interrupt and acts as external interrupt pin (refer to interrupt description for additional information).

The enable/disable of this interrupt can be managed with the write only IRINTEN bit available in the D/A2 Data/Control register (Address E2H, bit D7). When this bit is set to one the interrupt is enabled otherwise it is disabled.

The IRIN pin is RISING EDGE sensitive.

Application Note

When the IR interrupt is enabled, then a rising edge on the IR pin will generate an interrupt; if the IR interrupt is disabled, no IR interrupts can occur. Care should be taked because if the IR pin is high when the IR interrupt is enabled, an interrupt will also be generated; the following method to eliminate noise can also be used if the SW engineer wishes to enable/disable the IR interrupt.

If A Low-cost infra-red receiver is used, the customer may wish to test the IR signal by software after an interrupt in order to verify that there is a good pulse and not just noise. The IRIN pin cannot be read, so in this case it should be connected in parallel with another pin so the signal can be read. Furthermore the IRIN pin is sensitive to a rising edge interrupt; this means that the input to the pin should be low in the presence of no infra-red signal, but since most infra-red receiver modules give a high signal, the signal will need to be inverted with a transistor.

ON-SCREEN DISPLAY (OSD)

The ST632X,5X OSD macrocell is a CMOS LSI character generator which enable display of characters and symbols on the TV screen. The character rounding function enhances the readability of the characters. The ST632X,5X OSD receives horizontal and vertical synchronization signal and outputs screen information via R, G, B and blanking pins. The main characteristics of the macrocell are listed below:

- Number of display characters: 5 lines by 15 columns.
- Number of character types: 64 characters in one bank.
- Character size: Four character heights (18H, 36H 54H, 72H), two available per screen programmable by line.
- Character format: 6x9 dots with character rounding function.
- Character color: Eight colors available programmable by word.
- Display position: 64 horizontal positions by 2/fos and 63 vertical positions by 4 H
- Word spacing: 64 positions programmable from 2/fosc to 128/fosc.
- Line spacing: 63 positions programmable from 4 to 252 H.
- Background: No background, square background or fringe background programmable by word.
- Background color: Two of eight colors available programmable by word.
- Display output: Three character data output terminals (R,G,B) and a blank output terminal.
- Display on/off: Display data may be programmed on or off by word or entire screen. Entire screen may be blanked.

ON-SCREEN DISPLAY (Continued)

Format Specification

The entire display can be turned on or off thru the use of global enable bit or the display may be selectively turned on or off by word. To turn off the entire display, the global enable bit (GE) should be zero. If the global enable is one, the display is controlled by the word enable bits (WE). The global enable bit is located in the global enable register and the word enable bit is located in the space character preceding the word.

Each line must begin with a format character which describes the format of that line and of the first word. This character is not displayed.

A space character defines the format of subsequent words. A space character is denoted by a one in bit 6 in the display RAM. If bit 6 of the display RAM is a zero, the other six bits define one of the 64 display characters.

The color, background and enable can be programmed by word. This information is encoded in the space character between words or in the format character at the beginning of each line. Five bits define the color and background of the following word, and determine whether it will be displayed or not.

Characters are stored in a 6 x 9 dot format. One dot is defined vertically as 2H (horizontal lines) and horizontally as 2/fosc if the smallest character size is enabled. There is no space between characters or lines if the vertical space enable (VSE) and horizontal space enable (HSE) bits are both zero. This allows the use of special graphics characters.

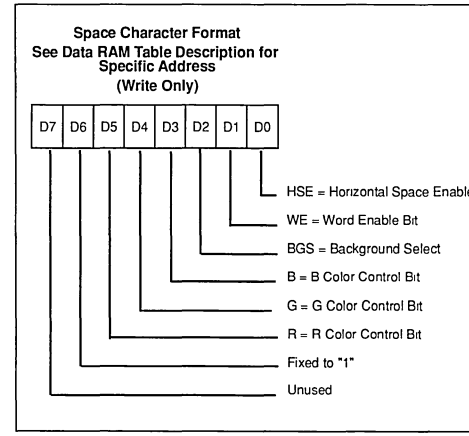
The normal alphanumeric character set is formatted to be 5 x 7 with on empty row at the top and one at the bottom and one empty column at the right. If VSE and HSE are both zero, then the spacing between alphanumeric characters is 1 dot and the spacing between lines of alphanumeric characters is 2H.

The character size is programmed by line thru the use of the size bit (S) in the format character and the global size bits (GS1 and GS2). The vertical spacing enable bit (VSE) located in the format character controls the spacing between lines. If this bit is set to one, the spacing between lines is defined by the vertical spacing register, otherwise the spacing between lines is 0.

The spacing between words is controlled by the horizontal space enable bit (HSE) located in the space character. If this bit is set to one, the spacing between words is defined by the horizontal spacing register, otherwise the space character width of 6 dots is the spacing between words.

The formats for the display character, space character and format character are described hereafter.

Figure 65. Space Character Register Explanation



D7. Not used.

D6. This pin is fixed to "1".

R, G, B. *Color.* The 3 color control bits define the color of the following word as shown in table 11.

Table 11. Space Character Register Colour Setting.

R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

BGS. *Background Select.* The background select bit selects the desired background for the following word. There are two possible backgrounds defined by the bits in the Background Control Register.

"0" - The background on the following word is enabled by BG0 and the color is set by R0, G0, and B0.

"1" - The background on the following word is enabled by BG1 and the color is set by R1, G1, and B1.

ON-SCREEN DISPLAY (Continued)

WE. *Word Enable.* The word enable bit defines whether or not the following word is displayed.

"0" - The word is not displayed.

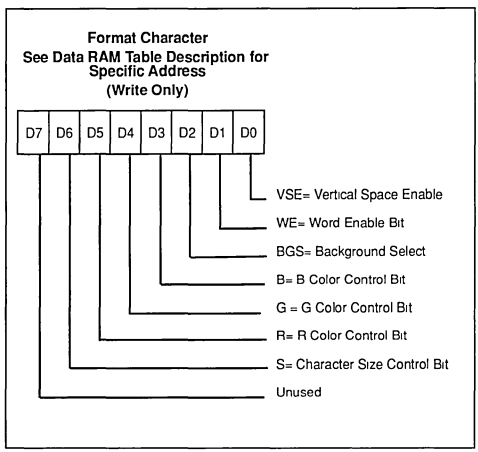
"1" - If the global enable bit is one, then the word is displayed.

HSE. *Horizontal Space Enable.* The horizontal space enable bit determines the spacing between words. The space between characters is always 0. The alphanumeric character set is implemented in a 5 x 7 format with one empty column to the right and one empty row above and below so that the space between alphanumeric characters will be one dot.

"0" - The space between words is equal to the width of the space character, which is 6 dots.

"1" - The space between words is defined by the value in the horizontal space register plus the width of the space character.

Figure 66. Format Character Register Explanation



D7. This bit is not used

S. *Character Size.* The character size bit, along with the global size bits (GS2 and GS1) located in the horizontal space register, specify the character size for each line as defined in Table 13.

BGS. *Background Select.* The background select bit selects the desired background for the following word. There are two possible backgrounds defined by the bits in the Background Control Register.

"0" - The background on the following word is enabled by BG0 and the color is set by R0, G0, and B0.

"1" - The background on the following word is enabled by BG1 and the color is set by R1, G1, and B1.

WE. *Word Enable.* The word enable bit defines whether or not the following word is displayed.

"0" - The word is not displayed.

"1" - If the global enable bit is one, then the word is displayed.

R, G, B. *Color.* The 3 color control bits define the color of the following word as shown in Table 12.

VSE. *Vertical Space Enable.* The vertical space enable bit determines the spacing between lines.

"0" - The space between lines is equal to 0H. The alphanumeric character set is implemented in a 5 x 7 format with one empty column to the right and one empty row above and one below and stored in a 6 x 9 format.

"1" - The space between lines is defined by the value in the vertical space register.

Table 12. Format Character Register Colour Setting.

R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

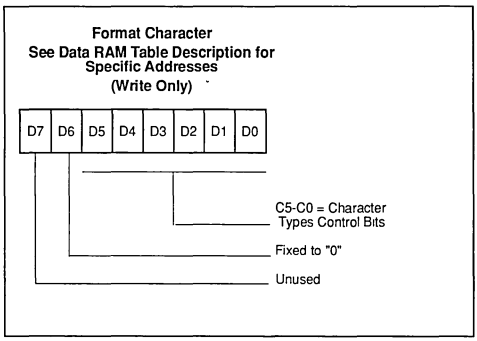
Table 13. Format Character Register Size Setting

GS2	GS1	S	Vertical Height	Horizontal lenght
0	0	0	18H	6 TDOT
0	0	1	36H	12 TDOT
0	1	0	18H	6 TDOT
0	1	1	54H	18 TDOT
1	0	0	36H	12 TDOT
1	0	1	54H	18 TDOT
1	1	0	36H	12 TDOT
1	1	1	72H	24 TDOT

TDOT= 2/fosc

ON-SCREEN DISPLAY (Continued)

Figure 67. Display Character Register Explanation



D7. This bit is not used.

D6. This bit is fixed to "0".

C5-C0. *Character type.* The 6 character type bits define one of the 64 available character types. These character types are shown on the following pages.

Character Types

The character set is user defined as ROM mask option.

Register and RAM Addressing

The OSD contains six registers and 80 RAM locations. The seven registers are the Vertical Start Address register, Horizontal Start Address register, Vertical Space register, Horizontal Space register, Background Control register and Global Enable register. The Global Enable register can be written at any time by the ST63 Core. The other five registers and the RAM can only be read or written to if the global enable is zero.

The six registers and the RAM are located on two pages of the paged memory of the ST63XX MCUs. Each page contains 64 memory locations. This paged memory is at memory locations 00H to 3FH in the ST63XX memory map. A page of memory is enabled by setting the desired page bit, located in the data RAM bank switching register, to a one. The page register is location E8H. A one in bit five selects page 5, located on the OSD and a one in bit 6 selects page 6 on the OSD. Table 14 shows the addresses of the OSD registers and RAM.

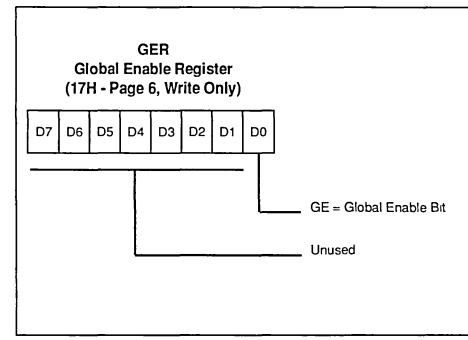
Table 14. OSD Control Registers and Data RAM Addressing

Page	Address	Register or RAM
5	00H - 3FH	RAM Locations 00H - 3FH
6	00H - 0FH	RAM Locations 00H - 0FH
6	10H	Vertical Start Register
6	11H	Horizontal Start Register
6	12H	Vertical Space Register
6	13H	Horizontal Space Register
6	14H	Background Control Register
6	17H	Global Enable Register

OSD Global Enable Register

This register contains the global enable bit (GE). It is the only register that can be written at any time regardless of the state of the GE bit. It is a write only register.

Figure 68. Global Enable register



D7-D1. These bits are not used

GE. *Global Enable.* This bit allows the entire display to be turned off.

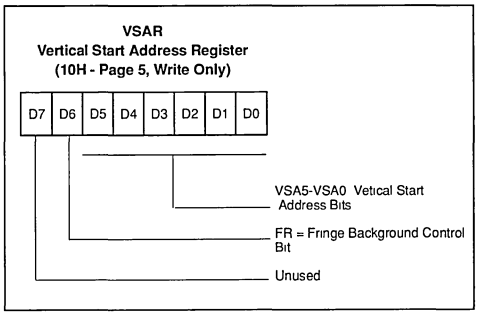
"0" - The entire display is disabled. The RAM and other registers of the OSD can be accessed by the Core.

"1" - Display of words is controlled by the word enable bits (WE) located in the format or space character.

The other registers and RAM cannot be accessed by the Core.

ON-SCREEN DISPLAY (Continued)

Figure 69. Vertical Start Address Register



D7. This bit is not used

FR. *Fringe Background.* This bit changes the background from a box background to a fringe background. The background is enabled by word as defined by either BK0 or BK1.

"0" - The background is defined to be a box which is 7 x 9 dots.

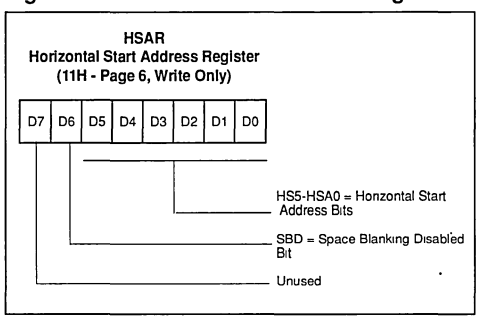
"1" - The background is defined to be a fringe.

VSA5-VSA0. *Vertical Start Address.* These bits determine the start position of the first line in the vertical direction. The 6 bits can specify 63 display start positions of interval 4H. The first start position will be the fourth line of the display. The vertical start address is defined VSA0 by the following formula.

Vertical Start Address = $4H(2^5(VSA5) + 2^4(VSA4) + 2^3(VSA3) + 2^2(VSA2) + 2^1(VSA1) + 2^0(VSA0))$

The case of all Vertical Start Address bits being zero is 111.

Figure 70. Horizontal Start Address Register



D7. This bit is not used.

SBD. *Space Blanking Disable.* This bit controls whether or not the background is displayed when outputting spaces. If two background colors are used on adjacent words, then the background should not be displayed on spaces in order to make a nice break between colors. If an even background around an area of text is desired, as in a menu, then the background should be displayed when outputting spaces.

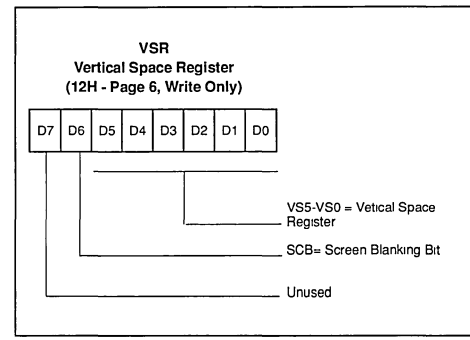
"0" - The background during spaces is controlled by the background enable bits (BK0 and BK1) located in the Background Control register.

"1" - The background is not displayed when outputting spaces.

HSA5, HSA0 - *Horizontal Start Address bits.* These bits determine the start position of the first character in the horizontal direction. The 6 bits can specify 64 display start positions of interval 2/fosc or 400ns. The first start position will be at 4.0µs because of the time needed to access RAM and ROM before the first character can be displayed. The horizontal start address is defined by the following formula.

Horizontal Start Address = $2/fosc(10.0 + 2^5(HSA5) + 2^4(HSA4) + 2^3(HSA3) + 2^2(HSA2) + 2^1(HSA1) + 2^0(HSA0))$

Figure 71. Vertical Space Register



D7. This bit is not used

SCB. *Screen Blanking.* This bit allows the entire screen to be blanked.

"0" - The blanking output signal (VBLK) is active only when displaying characters.

"1" - The blanking output signal (VBLK) is always active. Characters in the display RAM are still displayed.

When this bit is set to one, the screen is blanked also without setting the Global Enable bit to one (OSD disabled).

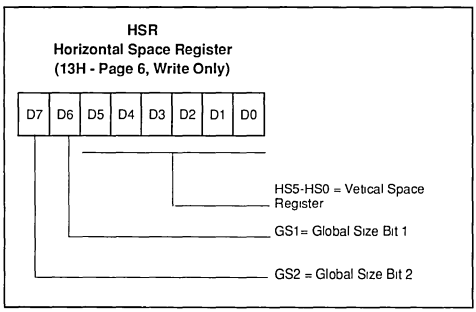
ON-SCREEN DISPLAY (Continued)

VS5 , VS0. *Vertical Space.* These bits determine the spacing between lines if the Vertical Space Enable bit (VSE) in the format character is one. If VSE is zero there will be no spaces between lines. The Vertical Space bits can specify one of 63 spacing values from 4H to 252H. The space between lines is defined by the following formula.

Space between lines = $4H(2^5(VS5) + 2^4(VS4) + 2^3(VS3) + 2^2(VS2) + 2^1(VS1) + 2^0(VS0))$

The case of all Vertical Start Address bits being zero is ill.

Figure 72. Horizontal Space Register



GS2,GS1. *Global Size.* These bits along with the size bit (S) located in the Character format word specify the character size for each line as defined in table 15.

Table 15. Horizontal Space Register Size Setting.

GS2	GS1	S	Vertical Height	Horizontal Lenght
0	0	0	18H	6 TDOT
0	0	1	36H	12 TDOT
0	1	0	18H	6 TDOT
0	1	1	54H	18 TDOT
1	0	0	36H	12 TDOT
1	0	1	54H	18 TDOT
1	1	0	36H	12 TDOT
1	1	1	72H	24 TDOT

Note: TDOT= $2/f_{OSC}$

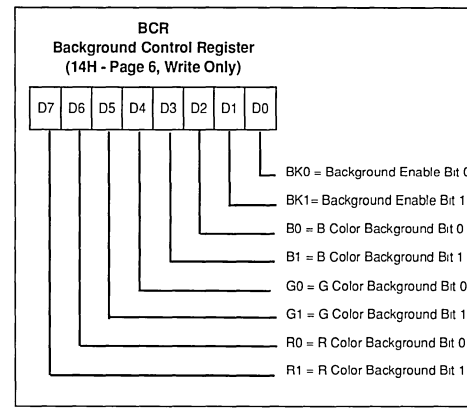
HS5, HS0 . *Horizontal Space* . These bits determine the spacing between words if the Horizontal Space Enable bit (HSE) located in the space character is a one. The space between words is then equal to the width of the space character plus the number of tdots specified by the Horizontal Space bits. The 6 bits can specify one of 64 spacing values ranging from 2/fosc to 128/fosc. The formula is shown below for the smallest size character(18H). If larger size characters are being displayed the spacing between words will increase proportionately. Multiply the value below by 2, 3 or 4 for character sizes of 36H, 54H and 72H respectively.

Space between words (not including the space character)=$2/fosc((1+2^5(HS5)+2^4(HS4)+2^3(HS3)+2^2(HS2)+2^1(HS1)+2^0(HS0))$

Background Control Register

This register sets up two possible backgrounds. The background select bit (BGS) in the format or space character will determine which background is selected for the current word.

Figure 73. Background Control Registers



R1,R0,G1,G0,B1,B0. Background Color. These bits define the color of the specified background, either background 1 or background 0 as defined in Table 16.

Table 16. Background Register Colour Setting.

RX	GX	BX	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

ON-SCREEN DISPLAY (Continued)

BK1,BK0. *Background Enable.*These bits determine if the specified background is enabled or not.

"0" - The following word does not have a background.

"1" - There is a background around the following word.

OSD Data RAM

The contents of the data RAM can be accessed by the ST63XX MCUs only when the global enable bit (GE) in the Global Enable register is a zero.

The first character in every line is the format character. This character is not displayed. It defines the size of the characters in the line and contains the vertical space enable bit. This character also defines the color, background and display enable for the first word in the line. Subsequent characters are either spaces or one of the 64 available character types.

The space character defines the color, background, display enable and horizontal space enable for the following word. Since there are 5 display lines of 15 characters each, the display RAM must contain 5 lines x (15 characters + 1 format character) or 80 locations. The RAM size is 80 locations x 7 bits. The data RAM map is shown inTable 17.

Emulator Remarks

There are a few differences between emulator and silicon. For noise reasons, the OSD oscillator pins are not available: the internal oscillator cannot be disabled and replaced by an external coil.

Application Notes

1 - The OSD character generator is composed of a dual port video ram and some circuitry. It needs two input signals VSYNC and HSYNC to syncronize its dedicated oscillator to the TV picture. It generates 4 output signals, that can be used from the TV set to generate the characters on the screen. For instance, they can be used to feed the SCART plug, providing an adequate buffer to drive the low impedance (75 Ω) of the SCART inputs.

2 - The Core sees the OSD as a number of RAM locations (80) plus a certain number of control registers (6). These 86 locations are mapped in two pages of the dynamic data ram address range (0H..3FH).
In page 5 (load 20H in the register 0E8H), there are 64 bytes of RAM, the ones of the first 4 rows (16 bytes each row, 15 characters per row maximum, plus an hidden leading format character). In page 6 (load 40H in register 0E8H), the 16 bytes of the fith row (0..0FH), and the 6 control registers (10H..14H,17H).

3 - The video RAM is a dual port ram. That means that it can be addressed either from the Core or from the OSD circuitry itself. To reduce the complexity of the circuitry, and thus its cost, some restrictions have been introduced in the use of the OSD.

Table 17. OSD RAM Map

Column				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A0				0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A3				0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A2				0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A1				0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A6	A5	A4	LINE																
0	0	0	1	FT															
0	0	1	2	FT															
0	1	0	3	FT															
0	1	1	4	FT															
1	0	0	5	FT															

AVAILABLE SCREEN SPACE

Notes: FT. The format character required for each line. Characters in columns 1 thru 15 are displayed

ON-SCREEN DISPLAY (Continued)

a. The Core can Only write to any of the 86 locations (either video RAM or control registers).

b. The Core can Only write to any of the leading 85 locations when the OSD oscillator is OFF. Only the last location (control register 17H in page 6) can be addressed at any time. This is the Global Enable Register, which contains only the GE bit. If it is set, the OSD is on, if it is reset the OSD is off.

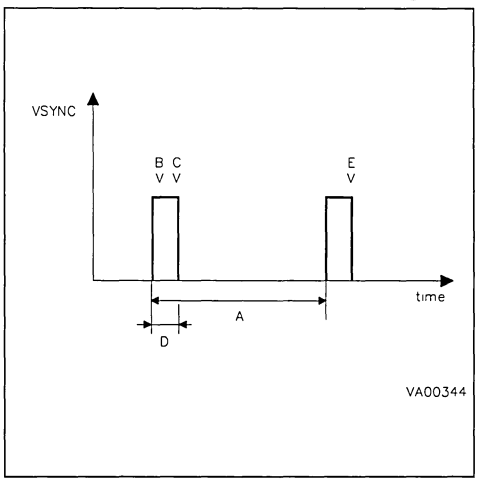
4 - The timing of the on/off switching of the OSD oscillator is the following:

a. GE bit is set. The OSD oscillator will start on the next VSYNC signal.

b. GE bit is reset. The OSD oscillator will be immediately switched off.

To avoid a bad visual impression, it is important that the GE bit is set before the end of the flyback time when changing characters. This can be done inside the VSYNC interrupt routine. The following diagram can explain better:

Figure 74. OSD Oscillator ON/OFF Timing



Notes:
A. Picture time: 20 mS in PAL/SECAM.
B. VSYNC interrupt, if enabled.
C. Starting of OSD oscillator, if GE = 1.
D. Flyback time.

When modifying the picture display (i.e.: a bar graph for an analog control), it is important that the switching on of the GE bit is done before the the end of the flyback time (D in Figure 67). If the GE bit is set after the end of the flyback time then the OSD will not start until the begining of the next frame. This results in one frame being lost and will result in a Flicker on the screen. One method to be sure to avoid the flicker is to wait for the VSYNC interrupt at the start of the flyback; once the VSYNC interrupt is detected, then the GE bit can be set to zero, the characters changed, and the the GE set to one. All this should occur before the end of the flyback time in order not to loose a frame. The correct edge of the interrupt must be chosen. The VSYNC pin may alternatively be sampled by software in order to know the status; this can be done by reading the pin PB2 (VSYNC).

6 - An OSD end of line Bar is present in the ST63PXX piggyback and ST63XX ROM devices when using the background mode. If this bar is present with software running in the piggybacks then it is also present on the ROM mask version. If the end of line bar is seen to be eliminated by software in the piggyback, then it is also be eliminated in the ROM mask version.

The bar appears at the end of the line in the background mode when the last character is a space character and the first format character is defined with S=0 (size 0). The bar is the color of the background defined by the space character. To eliminate bar:

a. If two backgrounds are used then the bar should be moved off the screen by using large word spaces instead of character spaces. If there are not enough spaces before the end of the line, then the location of the valid characters should be moved so they appear at the end of the line (and hence no bar); positioning can be compensated using the horizontal start register.

b. If only one background is used, then the other background should be transparent in order to eliminate the bar.

7 - The OSD oscillator external network should consist of a capacitor on each of the OSD oscillator pins to ground together with an inductance between the the pin. The user should select the two capacitors to be the same value (15pF to 25pF each is recommended). The inductance is chosen to give the desired OSD oscillator frequency for the application (normally 56µH).

14-BIT VOLTAGE SYNTHESIS TUNING PERIPHERAL (ST6356,57,58 only)

The ST635X on-chip voltage synthesis tuning peripheral has been integrated to allow the generation of tuning reference voltage in low/mid end TV set applications. The peripheral is composed of a 14-bit counter that allows the conversion of the digital content in a tuning voltage, available at the VS output pin, by using PWM and BRM techniques. The 14-bit counter gives 16384 steps which allows a resolution of approximately 2mV over a tuning voltage of 32V ; this corresponds to a tuning resolution of about 40KHz per step in UHF band (the actual value will depend on the characteristics of the tuner).

The tuning word consists of a 14-bit word contained in the registers VSDATA1 (location 0EDH) and VSDATA2 (location 0EEH). Course tuning (PWM) is performed using the seven MSBit, while the fine tuning (BRM) is performed using the data in the seven LSBIT. With all zeros loaded the output is zero ; as the tuning voltage increseses from all zeros, the number of pulses in one period increses to 128 with all pulses being the same width. For values larger than 18, the PWM takes over and the number of pulses in one period remains constant at 128, but the width changes. At the other end of the scale, when almost all ones are loaded, the pulses will start to link together and the number of pulses will decrease. When all ones are loaded, the output will be almost 100% high but will have a low pulse (1/16384 of the high pulse).

Output Details

Inside the on-chip Voltage Synthesis cell are included the register latches, a reference counter, PWM and BRM control circuitry ; the structure is one used in many devices currenlty in production from SGS-THOMSON (M106, M193, M293, M490/91/94). In the ST635X the clock for the 14-bit reference counter is 2MHz derived from the 8MHz system clock. From the circuit point of view, the seven most significant bits controls the course tuning, while the seven least significant bits the fine tuning. From the application and software point of view, the 14 bits can be considered as one binary number.

As already mentioned the course tuning consists of a PWM signal with 128 steps ; we can consider the fine tuning to cover 128 course tuning cycles. The addition of pulses is described in the following Table 18.

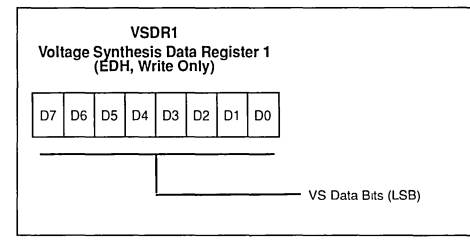
Table 18. Fine Tuning Pulse Addition

Fine Tuning (7 LSB)	N° of Pulses added at the following cycles (0...127)
0000001	64
0000010	32, 96
0000100	16, 48, 80, 112
0001000	8, 24, ...104, 120
0010000	4, 12, ...116, 124
0100000	2, 6, ...122, 126
1000000	1, 3, ...125, 127

The VS output pin has a standard drive push-pull output configuration.

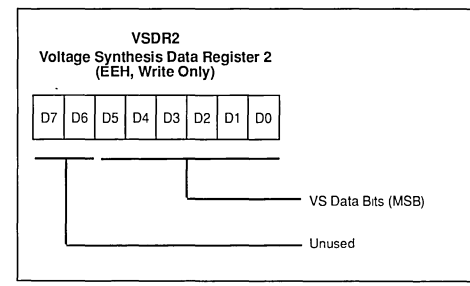
VS Tuning Cell Registers

Figure 75. VS Data Register 1



D7-D0. These are the 8 least significant VS data bits. Bit 0 is the LSB. This register is undefined on reset.

Figure 76. VS Data Register 2



D7-D6. These bits are not used.

D5-D0. These are the 6 most significant VS data bits. Bit 5 is the MSB. This register is undefined on reset.

SOFTWARE DESCRIPTION

The ST63XX software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short to provide byte efficient programming capability. The ST63XX Core has the ability to set or clear any register or RAM location bit of the Data space with a single instruction. Furthermore, the program may branch to a selected address depending on the status of any bit of the Data space. The carry bit is stored with the value of the bit when the SET or RES instruction is processed.

Addressing Modes

The ST63XX Core has nine addressing modes which are described in the following paragraphs. The ST63XX Core uses three different address spaces: Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, the data for immediate mode instructions, and in this space is physically allocated the data ROM which is addressed as data space. Data space contains the Accumulator, the X,Y,V and W registers, the Core control registers, peripheral and Input/Output registers, the RAM locations and the window to address the Data ROM (physically located into the program memory) locations (for storage of tables and constants). Stack space contains six 12-bit RAM bytes used to stack the return addresses for subroutines and interrupts.

Immediate. In the immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In the direct addressing mode, the address of the byte that is processed by the instruction is stored in the location that follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data space memory with a single two-byte instruction.

Short Direct. The Core can address the four RAM registers X,Y,V,W (locations 80H, 81H, 82H, 83H) in the short-direct addressing mode . In this case, the instruction is only one byte long and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of the direct addressing mode. (Note : 80H and 81H are also indirect registers).

Extended. In the extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four less significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) that use the extended addressing mode are able to branch any address of the directly addressable Program space. An extended addressing mode instruction is two-byte long.

Program Counter Relative. The relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to + 16 locations around the address of the relative instruction. If the condition is not true, the instruction that follows the relative instruction is executed. The relative addressing mode instruction is one-byte long. The opcode is obtained by adding the three most significant bits that characterize the kind of test, one bit that determines whether the branch is a toward (when it is 0) or backward (when it is 1) branch and the four less significant bits that give the span of the branch (0H to FH) that must be added or subtracted to the address of the relative instruction to obtain the address of the branch.

Bit Direct. In the bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 directly addressable locations of Data space memory can be set or cleared.

Bit Test & Branch. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit test and branch instruction is three-byte long. The bit identification and the tested condition are included in the opcode byte. The address of the byte to be tested follows immediately the opcode in the Program space. The third byte is the jump displacement, which is in the range from -126 to + 129. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In the indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed by the content of one of the indirect registers, X or Y (80H,81H). The indirect register is selected by the bit 4 of the opcode. A register indirect instruction is one byte long.

Inherent. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

SOFTWARE DESCRIPTION (Continued)

Instruction Set

The ST63XX Core has a set of 40 basic instructions. When these instructions are combined with nine addressing modes, 244 usable opcodes can be obtained. They can be divided into six different types : load/store, arithmetic/logic, conditional branch, control instructions, jump/call, bit manipulation. The following paragraphs describe the different types. All the instructions within a given type are presented in individual tables.

Load & Store. These instructions use one,two or three bytes in relation with the addressing mode. One operand is the Accumulator for LOAD and the other operand is obtained from data memory using one of the addressing modes. For LOAD Immediate one operand can be any of the 256 data space bytes while the other is always an immediate data. Refer to Table 19.

Table 19. Load & Store instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
LD A, X	Short Direct	1	4	Δ	*
LD A, Y	Short Direct	1	4	Δ	*
LD A, V	Short Direct	1	4	Δ	*
LD A, W	Short Direct	1	4	Δ	*
LD X, A	Short Direct	1	4	Δ	*
LD Y, A	Short Direct	1	4	Δ	*
LD V, A	Short Direct	1	4	Δ	*
LD W, A	Short Direct	1	4	Δ	*
LD A, rr	Direct	2	4	Δ	*
LD rr, A	Direct	2	4	Δ	*
LD A, (X)	Indirect	1	4	Δ	*
LD A, (Y)	Indirect	1	4	Δ	*
LD (X), A	Indirect	1	4	Δ	*
LD (Y), A	Indirect	1	4	Δ	*
LDI A, #N	Immediate	2	4	Δ	*
LDI rr, #N	Immediate	3	4	*	*

Notes:
X,Y Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr Data space register
Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Arithmetic and Logic. These instructions are used to perform the arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while the other can be either a data space memory content or an immediate value in relation with the addressing mode. In CLR,DEC,INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator. Refer to Table 20.

Table 20. Arithmetic & Logic instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	*
AND A, (Y)	Indirect	1	4	Δ	*
AND A, rr	Direct	2	4	Δ	*
ANDI A, #N	Immediate	2	4	Δ	*
CLR A	Short Direct	2	4	Δ	Δ
CLR rr	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register

Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Conditional Branch. The branch instructions achieves a branch in the program when the selected condition is met. Refer to Table 21.

Bit Manipulation Instructions. These instructions can handle (set or reset) any bit in data space memory. Refer to Table 22.

Control Instructions. The control instructions control the MCU operations during program execution. Refer to Table 23.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutines call inside the whole program space. Refer to Table 24.

Table 21. Conditional Branch instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b. 3-bit address
e. 5 bit signed displacement in the range -15 to +16
ee. 8 bit signed displacement in the range -126 to +129
rr. Data space register
Δ Affeed
*. Not Affected

Table 22. Bit Manipulation instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes:
b. 3-bit address,
rr Data space register,
* Not Affected

Table 23. Control instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:
1. This instruction is deactivated on ST639X (HW watchdog and a WAIT is automatically executed instead of a STOP.
Δ. Affected
*. Not Affected

Table 24. Jump & Call instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes:
abc. 12-bit address,
* Not Affected

SOFTWARE DESCRIPTION (Continued)

Opcode Map Summary. The following table contains an opcode map for the instructions used on the MCU.

Table 25. Opcode Map

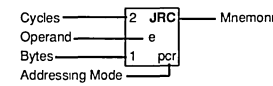
Low / Hi	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Low / Hi
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 LD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 pcr	4 LD a,(y) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 pcr	4 LD a,rr 2 dir	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b d	2 JRZ e 1 pcr	4 COM a 1 inh	2 JRC e 1 pcr	4 CP a,(y) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b d	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 pcr	4 CP a,rr 2 dir	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 ADD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 pcr	4 ADD a,(y) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 pcr	4 ADD a,rr 2 dir	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 INC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 pcr	4 INC (y) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 pcr	4 INC rr 2 dir	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 LD (x),a 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b d	2 JRZ e 1 pcr	# 	2 JRC e 1 pcr	4 LD (y),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ v 1 sd	4 INC v 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 pcr	4 LD rr,a 2 dir	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 AND a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b d	2 JRZ e 1 pcr	4 RLC a 1 inh	2 JRC e 1 pcr	4 AND a,(y) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ a,v 1 sd	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 pcr	4 AND a,rr 2 dir	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 SUB a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 pcr	4 SUB a,(y) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 pcr	4 SUB a,rr 2 dir	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 DEC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 pcr	4 DEC (y) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 pcr	4 DEC rr 2 dir	F 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement



ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that VI and VO must be higher than V_{SS} and smaller than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature. Tj, in Celsius can be obtained form.:

$$Tj = TA + PD \times RthJA$$

Where: TA = Ambient Temperature,
RthJA = Package thermal resistance (junction-to ambient),

PD = Pint + Pport,

Pint = $I_{DD} \times V_{DD}$ (chip internal power),

Pport = Port power dissipation (determined by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
V_I	Input Voltage (AFC IN)	V_{SS} – 0.3 to +13	V
V_I	Input Voltage (Other Inputs)	VSS – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage (Port A, DA0-3, BSW0-3, OUT1)	V_{SS} – 0.3 to + 13	V
V_O	Output Voltage (Other Inputs)	VSS – 0.3 to V_{DD} +0.3	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}, Port A	± 10	mA
I_O	Current Drain per Pin (Port A)	± 50	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	150	mA
T_j	Junction Temperature	150	°C
T_{STG}	Storage Temperature	– 60 to 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP40 PSDIP42 PDIP48			38 39 40	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature		0		70	°C
V_{DD}	Operating Supply Voltage		4.5		5.5	V
fOSC	Oscillator Frequency RUN & WAIT Modes			8.0	8.1	MHz
fOSDOSC	On-Screen Display Oscillator Frequency				8.0	MHz

EEPROM INFORMATION

The ST63XX EEPROM macrocell and the single poly EEPROM process have been specially developed to achieve 1.000.000 Write/Erase cycles and a 10 years data retention.

DC ELECTRICAL CHARACTERISTICS

(T_A= 0 to + 70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	All I/O Pins, KBY0-2			0.3x V_{DD}	V
V_{IH}	Input High Level Voltalge	All I/O Pins, KBY0-2	0.75xV_{DD}			V
V_{HYS}	Hysteresis Voltage(1)	All I/O Pins, KBY0-2 V_{DD} = 5V		1.0		V
V_{OL}	Low Level Output Voltage	Port B/C, DA0-3 BSW0-3, OUT1, VS, OSD Outputs V_{DD} = 4.5V I_{OL} = 1.6mA I_{OL} = 5.0mA			 0.4 1.0	 V V
V_{OL}	Low Level Output Voltage	Port A, V_{DD} = 4.5V I_{OL}= 3.2mA I_{OL}= 30mA			 0.4 1.0	 V V
V_{OL}	Low Level Output Voltage	OSDOSCOUT, OSCOUT, V_{DD} = 4.5V I_{OL}= 0.1mA			 0.4	 V
V_{OH}	High Level Output Voltage	Port B/C (2), VS V_{DD} = 4.5V I_{OH} = – 1.6mA	 4.1			 V
V_{OH}	High Level Output Voltage	OSDOSCOUT, OSCOUT, V_{DD} = 4.5V I_{OL}= – 0.1mA	 4.1			 V
I_{PU}	Input Pull Up Current Input Mode with Pull-up	Port B/C, KBY0-2 V_{IN}= V_{SS} (2)	– 100	– 50	– 25	µA
I_{IL} I_{IH}	Input Leakage Current	OSCIN V_{IN}= V_{SS} V_{IN}= V_{DD}	– 10 0.1	– 1 1	– 0.1 10	µA
I_{IL} I_{IH}	Input Leakage Current	All I/O Input Mode no Pull-up OSDOSCIN V_{IN}= V_{DD} or V_{SS}	 – 10		 10	 µA
I_{IL} I_{IH}	Input Leakage Current	Reset Pin with Pull-up V_{IN}= V_{SS}	– 50	– 30	– 10	µA
I_{IL} I_{IH}	Input Leakage Current	AFC Pin V_{IH}= V_{DD} V_{IL}= V_{SS} V_{IH}= 12.0V	 – 1		 1 40	 µA
I_{OH}	Output Leakage Current	Port A, DA0-3, BSW0-3 OUT1, OSDOUT V_{OH} = V_{DD}			10	µA
I_{OH}	Output Leakage Current High Voltage	Port A, DA0-3, BSW0-3 OUT1 V_{OH} = 12V			40	µA
I_{DD}	Supply Current RUN Mode	f_{OSC}= 8MHz, ILoad= 0mA V_{DD}= 5.5V		6	16	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{DD}	Supply Current WAIT Mode	f_{OSC}= 8MHz, ILoad= 0mA V_{DD}= 5.5V		3	10	mA
V_{ON}	Reset Trigger Level ON	RESET Pin			$0.2xV_{DD}$	V
V_{OFF}	Reset Trigger Level OFF	RESET Pin	$0.8xV_{DD}$			V
V_{TA}	Input Level Absolute Tolerance	A/D AFC Pin V_{DD} = 5V			±200	mV
V_{TR}	Input Level Relatice Tolerance (1)	A/D AFC Pin Relative to other levels V_{DD} = 5V			±100	mV

Notes:
1 Not 100% Tested
2. Input pull-up option only

AC ELECTRICAL CHARACTERISTICS

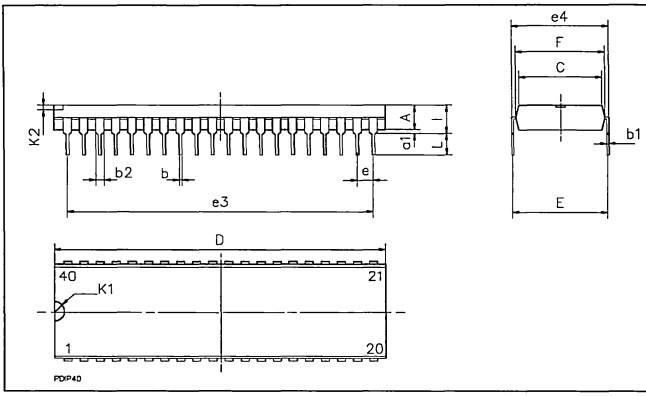
(T_A= 0 to + 70°C, f_{OSC} = 8MHz, V_{DD} = 4.5V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{WRES}	Minimum Pulse Width	RESET Pin	125			ns
t_{OHL}	High to Low Transition Time	Port A V_{DD} = 5V, CL = 1000pF (2)		100		ns
t_{OHL}	High to Low Transition Time	Port B, C, V_{DD} = 5V, CL = 100pF		20		ns
t_{OLH}	Low to High Transition Time (push-pill only)	Port B,C, V_{DD} = 5V, CL = 100pF		20		ns
t_{OH}	Data HOLD Time SPI after clock goes low I²CBUS/S-BUS Only		125			ns
f_{DA}	D/A Converter Repetition Frequency(1)			31.25		KHz
f_{OUT1}	62.5KHz Output(1)			62.50		KHz
f_{SPI}	SPI Baud Rate(1)			62.50		KHz
t_{WEE}	EEPROM Write Time	T_A = 25 °C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycles	Q_A LOT Acceptance Criteria	300.000	> 1 million		cycles
Retention	EEPROM Data Retention (4)	T_A = 25°C	10			years
C_{IN}	Input Capacitance (3)	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance (3)	All outputs Pins			10	pF
COSCIN, COSCOUT	Oscillator Pins Internal Capacitance (3)			5		pF
COSDIN, COSDOUT	OSD Oscillator External Capacitance	Recommended	15		25	pF

Notes:
1. A clock other than 8 MHz will affect the frequency response of those peripherals (D/A, 62.5KHz and SPI) whose clock is derived from the system clock.
2. The fall times of PORT A have been reduced in order to avoid current spikes while maintaining a high drive capability
3. Not 100% Tested
4. Based on extrapolated data

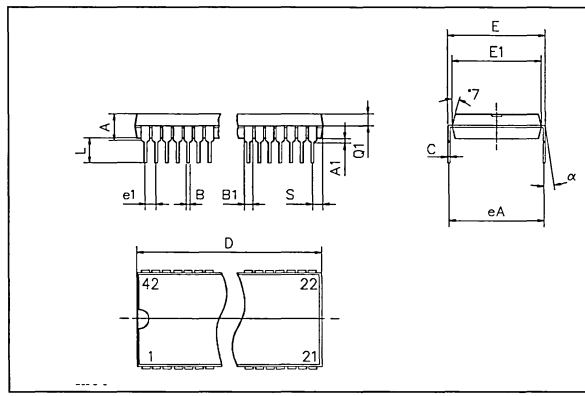
PACKAGE MECHANICAL DATA

Figure 76. 40-Pin Dual in Line Plastic



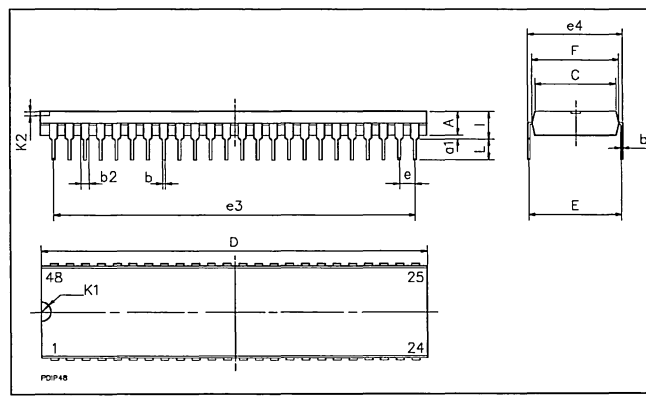
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0 63			0.025	
b		0.45			0 018	
b1	0 23		0.31	0.009		0.012
b2		1.27			0.050	
C	–	–	–	–	–	–
D			52.58			2.070
E	15.20		16.68	0.598		0.656
e		2 54			0 100	
e3		48.26			1.900	
e4	–	–	–	–	–	–
F			14.10			0 555
I		4 45			0 175	
L		3.30			0 129	

Figure 77. 42-Pin Shrink Dual in Line Plastic (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.81		5.08	0 15		0.20
A1	0.51		1.78	0.020		0.070
B	0.35		0.59	0.013		0.023
B1	0.75		1.42	0 029		0 056
C	0.20		0.36	0.008		0.014
D			39.12			1.540
E	15 24		15.87	0 60		0 62
E1	12.70		14.48	0 50		0.57
e1		1.78			0 070	
eA		15.24			0 600	
L	2 54		3.40	0.10		0.13
Q1	1.52		2.29	0.20		0.09
S	0.76		2.67	0.03		0.105
α	0		15°	0		15°

Figure 78. 48-Pin Dual in Line Plastic



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0 63			0.024	
b		0 45			0 017	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
C	–	–	–	–	–	–
D			62.74			2.470
E	15.20		16 68	0.598		0.656
e		2 54			0 100	
e3		58.42			2 300	
e4	–	–	–	–	–	–
F			14.10			0.555
I		4.45			0.175	
L		3 30			0.129	

ORDERING INFORMATION

The following chapter deals with the procedure for transfer the Program/Data ROM codes to SGS-THOMSON.

Communication of the ROM Codes. To communicate the contents of Program /Data ROM memories to SGS-THOMSON, the customer has to send:

- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the PROGRAM Memory
- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the ODD and EVEN ODD OSD Characters
- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the EEPROM initial content (this file is optional)
- a filled Option List form as described in the OPTION LIST paragraph.

The program ROM should respect the ROM Memory Map as in Table 26.

The ROM code must be generated with ST6 assembler. Before programming the EPROM, the buffer of the EPROM programmer must be filled with FFH. For shipment to SGS-THOMSON the EPROMs should be placed in a conductive IC carrier and packaging carefully.

Table 26. ROM Memory Map

ROM Page	Device Address	EPROM Address (1)	Description
Page 0	0000H-007FH 0080H-07FFH	0000H-007FH 0080H-07FFH	Reserved User ROM
Page 1 "STATIC"	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	User ROM Reserved Interrupt Vectors Reserved NMI Vector Reset Vector
Page 2	0000H-000FH 0010H-07FFH	1000H-100FH 1010H-17FFH	Reserved User ROM
PAGE 3	0000H-000FH 0010H-07FFH	1800H-180FH 1810H-1FFFH	Reserved user ROM

Note: 1. EPROM addresses are related to the use of ST63P2X/P5X piggyback emulation devices.

ORDERING INFORMATION (Continued)

Customer EEPROM Initial Contents: Format

a. The content should be written into an INTEL INTELLEC format file.

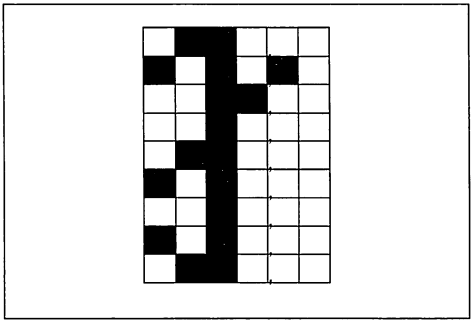
b. The starting address in 000h and the end in 7Fh.

c. Undefined or don't care bytes should have the content FFH.

OSD Test Character. In order to allow the testing of the on-chip OSD macrocell the following character must be provided at the fixed 3FH (63).

Listing Generation & Verification. When SGS-THOMSON receives the Codes, they are compared and a computer listing is generated from them. This listing refers extractly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed list constitutes a part of the contractual agreement for the creation of the customer mask. SGS-THOMSON sales organization will provide detailed information on contractual points.

Figure 79. OSD Test Character



Ordering Information Table

Sales Type	ROM/EEPROM Size	Temperature Range	Package
ST6326B1/XX	8K/128 Bytes	0 to + 70 ° C	PDIP40
ST6327B1/XX	8K/128 Bytes	0 to + 70 ° C	PSDIP42
ST6328B1/XX	8K/128 Bytes	0 to + 70 ° C	PDIP48
ST6356B1/XX	8K/128 Bytes	0 to + 70 ° C	PDIP40
ST6357B1/XX	8K/128 Bytes	0 to + 70 ° C	PSDIP42
ST6358B1/XX	8K/128 Bytes	0 to + 70 ° C	PDIP48

Note: "XX" Is the ROM code identifier that is allocated by SGS-THOMSON after receipt of all required options and the related ROM file.

ST632X,5X MICROCONTROLLER OPTION LIST

Customer: . . . . . .

Address: . . . . . .

Contact: . . . . . .

Phone No: . . . . . .

Reference: . . . . . .

Device [ ] (d) Package [ ] (p) Temperature Range [ ] (t)

For marking one line with 10 characters maximum is possible

Special Marking [ ] (y/n) Line1 " _ _ _ _ _ _ _ _ _ _ " (N)

Notes:

(d) 1= ST6326, 2 = ST6327, 3 = ST6328, 4 = ST6356, 5 = ST6357, 6 = ST6358

(p) B= Dual in Line Plastic

(t) 1= 0 to 70°C

(N) Letters, digits, ' . ', ' - ', ' / ' and spaces only

Marking: the default marking is equivalent to the sales type only (part number).

OSD POLARITY OPTIONS (Put a cross on selected item) :

	POSITIVE	NEGATIVE
VSYNC,HSYNC	[ ]	[ ]
R,G,B	[ ]	[ ]
BLANK	[ ]	[ ]

CHECK LIST:

	YES	NO
ROM CODE	[ ]	[ ]
OSD Code: ODD & EVEN	[ ]	[ ]
EEPROM Code (if Desired)	[ ]	[ ]

Signature .....

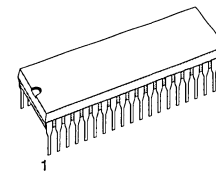
Date .....

SGS-THOMSON MICROELECTRONICS

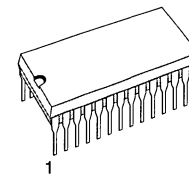
ST6340,ST6342 ST6344,ST6346

8 BIT HCMOS LOW COST MCUs FOR TV FREQUENCY & VOLTAGE SYNTHESIS WITH OSD

- 8-bit Architecture
- HCMOS Technology
- 8MHz Clock
- User Program ROM: 3884 byte
- Reserved Test ROM: 212 bytes
- Data ROM: User selectable size
- Data RAM: 64 bytes
- Data EEPROM: 48 bytes
- 28-Pin Dual in Line Plastic Package for the ST6340,42,44
- 40-Pin Dual in Line Plastic Package for the ST6346
- Up to 12, software programmable general purpose Inputs/Outputs
- 3 Inputs for keyboard scan (KBYO-2)
- Up to 4 High voltage outputs (BSWO-2)
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Up to 4 6-Bit PWM D/A Converters
- 62.5KHz Output Pin
- AFC A/D converter with 0.5V resolution
- 4 interrupt vectors (IRIN/NMI, Timer 1 & 2, VSYNC)
- 14-bit counter for Voltage Synthesis Tuning (Not available on ST6342)
- On-chip clock oscillator
- 2 Lines by 15 Characters On-Screen Display Generator with 64 Characters
- Byte efficient instruction set
- Bit test and jump instructions
- Wait and Bit Manipulation instructions
- True LIFO 6-level stack
- The development tool of the ST63 microcontrollers consists of the ST63TVS-EMU emulation and development system to be connected via a standard RS232 serial line to an MS-DOS Personal Computer.



PDIP40



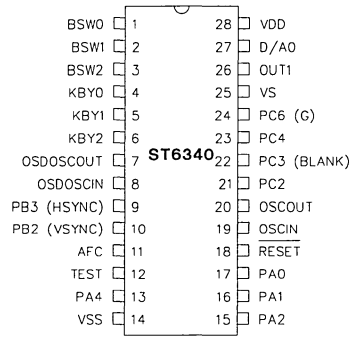
PDIP28

(Ordering Information at the end of the datasheet)

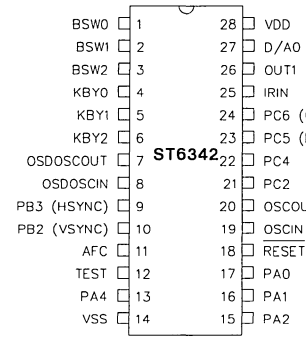
DEVICE SUMMARY

DEVICE	ROM (Bytes)	I/O pins	Package
ST6340	4K	6	PDIP28
ST6342	4K	6	PDIP28
ST6344	4K	5	PDIP28
ST6346	4K	12	PDIP40

Figures 1, 2. ST6340,42 Pin Configuration

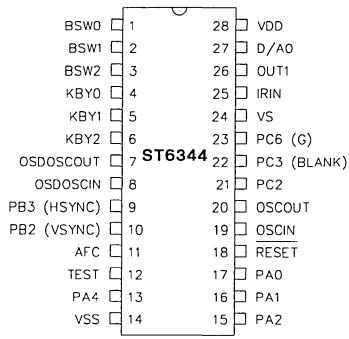


VR001389

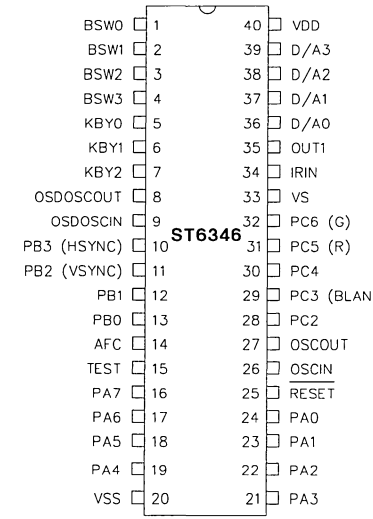


VR001390

Figures 3, 4. ST6344,46 Pin Configuration



VR001391



VR001392

Figure 5. ST634X Block Diagram

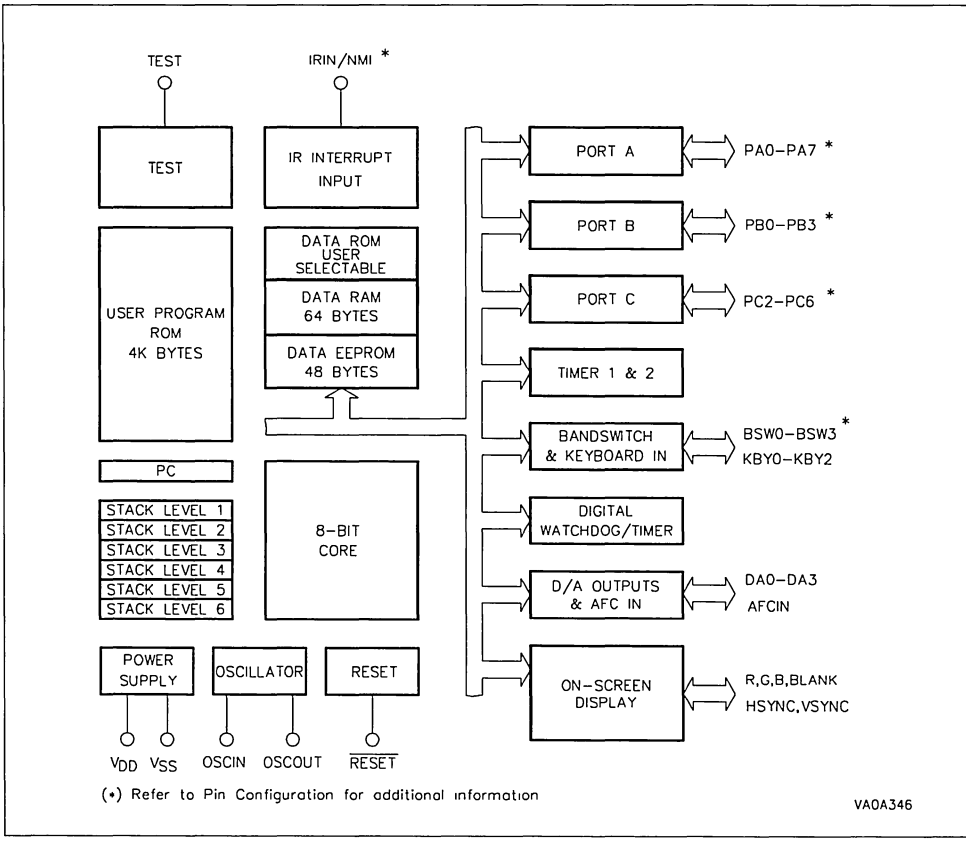


Table 1. ST634X Device Summary

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	I/O	KBY I/O	BSW OUT	AFC	D/A	OSD	PACK-AGE	EMUL. DEVICE
ST6340	4K	64	48	6	3	3	YES	1	YES	PDIP28	ST63P40
ST6342	4K	64	48	6	3	3	YES	1	YES	PDIP28	ST63P42
ST6344	4K	64	48	5	3	3	YES	1	YES	PDIP28	ST63P44
ST6346	4K	64	48	12	3	4	YES	4	YES	PDIP40	ST63P46

GENERAL DESCRIPTION

The ST634X microcontrollers are members of the 8-bit HCMOS ST63XX family, a series of devices specially oriented to TV applications. Different pin-out configurations are available to give the maximum application and cost flexibility. All ST63XX members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility and short design time. Many of these macrocells are specially dedicated to TV applications. The macrocells of the ST634X family: two Timer peripherals each including an 8-bit counter with a 7-bit software programmable prescaler (Timer), a digital hardware activated watchdog function (DHWD), four 6-bit PWM D/A converters, an AFC A/D converter with 0.5V resolution, a 14-bit Voltage Synthesis tuning peripheral, an on-screen display (OSD) with 15 characters per line, 64 characters. In addition all these devices have 4K of ROM, 64 bytes of data RAM and 48 bytes of EEPROM. Refer to pin configurations figures and to ST634X device summary (Table 1) for the definition of family members and a summary of differences among the different types.

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN, OSCOUT. These pins are internally connected to the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The OSCIN pin is the input pin, the OSCOUT pin is the output pin. Refer to ON-CHIP CLOCK OSCILLATOR description for additional information.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to start the microcontroller to the beginning of its program. Refer to RESET description for additional information.

TEST. The TEST (mode select) pin is used to place the MCU into special operating mode. If TEST is held at V_{SS} the MCU enters the normal operating mode. If TEST is held at V_{DD} when $\overline{\text{RESET}}$ is active the test operating mode is automatically selected (the user should connect this pin to V_{SS} for normal operation). Refer to TEST mode description for additional information.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or as an output under software control of the data direction register. Port A has an open-drain (5V drive) output configuration. Refer to I/O PORT description for additional information.

PB0-PB3. These 4 lines are organized as one I/O port (B). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register. PB0-PB4 have a push-pull configuration in output mode. PB2 and PB3 lines are connected to the VSYNC and HSYNC control signals of the OSD cell ; to provide the right signals to the OSD these I/O lines should be programmed in input mode and the user can read "on the fly" the state of VSYNC and HSYNC signals. PB2 is connected with the vertical synchronization signal VSYNC input. The active polarity of this signal is software controlled. PB3 is connected with the horizontal synchronization signal input HSYNC. Oscillator is synchronous with the change to low state. Oscillation stops while signal is in the high state. A ROM mask option is available to change the polarity of this signal. Refer to I/O port and pin configuration description for additional information.

PC2-PC6. These 5 lines are organized as one I/O port (C). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register. PC2 and PC4 have a push-pull configuration in output mode while PC3, PC5-PC6 (OSD signals) are open-drain (5V drive). PC3, PC5 and PC6 lines when in output modes are "ANDed" with the character and blank signals of the OSD cell. PC3 is connected with the OSD BLANK signal, PC5 and PC6 with the OSD R and G signals. These signals are active high. PC2 is also used as TV set On-Off switch (5V drive). Refer to I/O port and pin configuration description for additional information.

DA0-DA3. These pins are the four PWM D/A outputs (with 32KHz repetition) of the 6-bit on-chip D/A converters. The PWM function can be disabled by software and these lines can be used as general purpose open-drain outputs (12V drive). Refer to D/A converter description for additional information.

IRIN. This pin is the external NMI of the MCU . This pin is not available on ST634X.

OUT1. This pin is the 62.5KHz output specially suited to drive multi-standard chroma processors. This function can be disabled by software and the pin can be used as general purpose open-drain output (12V drive). Refer to D/A converter description for additional information.

BSW0-BSW3. These output pins can be used to select up to 4 tuning bands. These lines are configured as open-drain outputs (12V drive). Refer to AFC description for additional information.

PIN DESCRIPTION (Continued)

KBY0-KBY2. These pins are input only and can be used for keyboard scan. They have CMOS threshold levels with schmitt trigger and on-chip 100 KΩ pull-up resistors. Refer to AFC description for additional information.

AFC. This is the input of the on-chip 10 levels comparator that can be used to implement the AFC function. This pin is an high impedance input able to withstand signals with a peak amplitude up to 12V. Refer to AFC description for additional information.

OSDOSCIN, OSDOSCOUT. These are the On Screen display oscillator terminals. An oscillation capacitor and coil network have to be connected to provide the right signal to the OSD.

HSYNC, VSYNC. These are the horizontal and vertical synchronization pins. The active polarity of these pins to the OSD macrocell can be selected by the user as ROM mask option. If the device is specified to have negative logic inputs, then when these signals are low the OSD oscillator stops. If the device is specified to have positive logic inputs, then when these signals are high the OSD oscillator stops. Refer to OSD description for additiona information,

R, G, BLANK. Outputs from the OSD. R, and G are the color outputs while BLANK is the blanking output. All outputs are open-drain. The active polarity of these pins can be selected by the user as ROM mask option. Refer to the pin configurations for additional information.

VS. This is the output pin of the on-chip 14-bit voltage synthesis tuning cell (VS). The tuning signal present at this pin gives an approximate resolution of 40KHz per step over the UHF band. This line is a push-pull output with standard drive (Not available on ST6342).

Table 2. ST634X Pin Summary

Pin Function	Description
DA0 to DA3	Output, Open-Drain, 12V
BSW0 to BSW3	Output, Open-Drain, 12V
IRIN	Input, Resistive Bias, Schmitt Trigger
AFC	Input, High Impedance, 12V
OUT1	Output, Open-Drain, 12V
KBY0 to KBY2	Input, Pull-up, Schmitt Trigger
PA0 to PA7	I/O, Open-Drain, 5V, No Input Pull-up, Schmitt Trigger
PB0-PB3	I/O, Push-Pull, 5V, Input Pull-up, Schmitt Trigger
PC2, PC4	I/O, Push-Pull, 5V, Input Pull-up, Schmitt Trigger
PC3, PC5, PC6	I/O, Open-Drain, 5V, Input Pull-up, Schmitt Trigger
VS	Output, Push-Pull
R,G, BLANK	Output, Open-Drain, 5V
HSYNC, VSYNC	Input, Pull-up, Schmitt Trigger
OSDOSCIN	Input, High Impedance
OSDOSCOUT	Output, Push-Pull
TEST	Input, Pull-Down
OSCIN	Input, Resistive Bias, Schmitt Trigger to Reset Logic Only
OSCOUT	Output, Push-Pull
RESET	Input, Pull-up, Schmitt Trigger Input
V_{DD}, V_{SS}	Power Supply Pins

ST63XX CORE

The Core of the ST63XX Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control busses. The in-core communication is arranged as shown in the following block diagram figure; the controller being externally linked to both the reset and the oscillator, while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes through the control registers.

Registers

The ST63XX Family Core has five registers and three pairs of flags available to the programmer. They are shown in Figure 7 and are explained in the following paragraphs together with the program and data memory page registers.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is addressed in the data space as RAM location at the FFH address.

Figure 7. ST63XX Core Programming Model

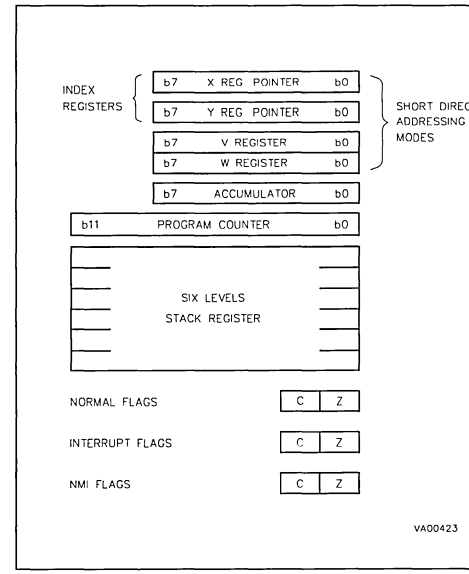
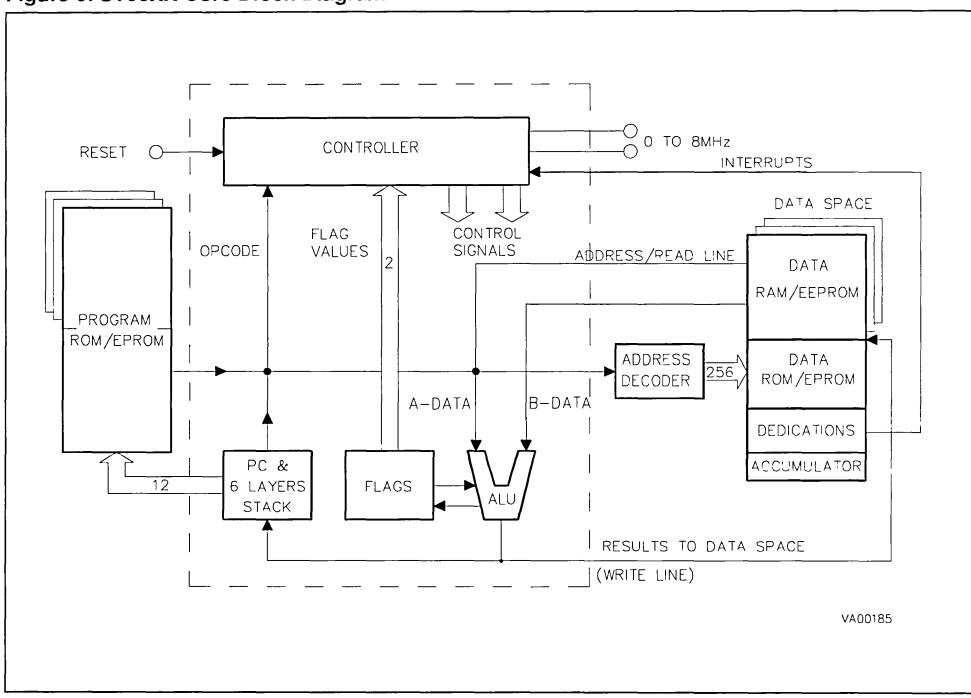


Figure 6. ST63XX Core Block Diagram



ST63XX CORE (Continued)

Accordingly, the ST63XX instruction set can use the accumulator as any other register of the data space.

Indirect Registers (X, Y). These two indirect registers are used as pointers to the memory locations in the data space. They are used in the register-indirect addressing mode.These registers can be addressed in the data space as RAM locations at the 80H (X) and 81H (Y) addresses. They can also be accessed with the direct, short direct, or bit direct addressing modes. Accordingly, the ST63XX instruction set can use the indirect registers as any other register of the data space.

Short Direct Registers (V, W). These two registers are used to save one byte in short direct addressing mode. These registers can be addressed in the data space as RAM locations at the 82H (V) and 83H (W) addresses. They can also be accessed with the direct and bit direct addressing modes. Accordingly, the ST63XX instruction set can use the short direct registers as any other register of the data space.

Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM location to be processed by the core. This ROM location may be an opcode, an operand, or an address of operand. The 12-bit length allows the direct addressing of 4096 bytes in the program space. The PC value is incremented, after it is read for the address of the current instruction, by sending it through the ALU, so giving the address of the next byte in the program. To execute relative jumps the PC and the offset values are shifted through the ALU, where they will be added, and the result is shifted back into the PC. The program counter can be changed in the following ways:

JP (Jump) instruction . . . . PC= Jump address

CALL instruction . . . . . PC= Call address

Relative Branch instructions . . . . . PC= PC+offset

Interrupt . . . . . PC= Interrupt vector

Reset . . . . . PC= Reset vector

Test mode . . . . . PC=Test mode vector (1)

RET & RETI instructions . . . PC= Pop (stack)

Normal instruction . . . . . PC= PC+1

Note: 1. Not available to the user.

Flags (C, Z)

The ST63XX Core includes three pairs of flags that correspond to 3 different modes: normal mode, interrupt mode and Non-Maskable-Interrupt-Mode. Each pair consists of a CARRY flag and a ZERO flag. One pair (CN, ZN) is used during normal operation, one pair is used during the interrupt mode (CI,ZI) and one is used during the not-maskable interrupt mode (CNMI, ZNMI).

The ST63XX Core uses the pair of flags that corresponds to the actual mode: as soon as an interrupt (resp. a Non-Maskable-Interrupt) is generated, the ST63XX Core uses the interrupt flags (resp. the NMI flags) instead of the normal flags. When the RETI instruction is executed, the normal flags (resp. the interrupt flags) are restored if the MCU was in the normal mode (resp. in the interrupt mode) before the interrupt. Should be observed that each flag set can only be addressed in its own routine (Not-maskable interrupt, normal interrupt or main routine). The interrupt flags are not cleared during the context switching and so, they remain in the state they were at the exit of the last routine switching.

The Carry flag is set when a carry or a borrow occurs during arithmetic operations, otherwise it is cleared. The Carry flag is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

The Zero flag is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

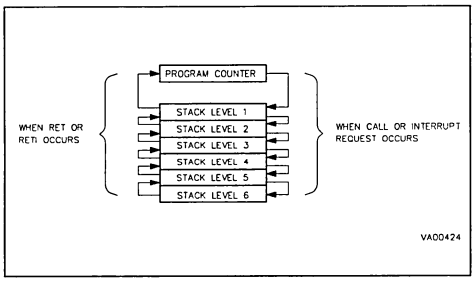
The switching between these three sets is automatically performed when an NMI, an interrupt and a RETI instructions occur. As the NMI mode is automatically selected after the reset of the MCU, the ST63XX Core uses at first the NMI flags. Refer to INTERRUPT description for additional information.

ST63XX CORE (Continued)

Stack

The ST63XX Core includes true LIFO hardware stack that eliminates the need for a stack pointer. The stack consists of six separate 12-bit RAM locations that do not belong to the data space RAM area. When a subroutine call (or interrupt request) occurs, the contents of each level is shifted into the next level while the content of the PC is shifted into the first level (the value of the sixth level will be lost). When subroutine or interrupt return occurs (RET or RETI instructions), the first level register is shifted back into the PC and the value of each level is shifted back into the previous level. These two operating modes are described in Figure 8. Since the accumulator, as all other data space registers, is not stored in this stack the handling of this registers shall be performed inside the subroutine.

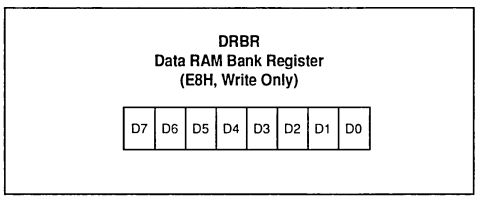
Figure 8. Stack Operation



The stack pointer will remain in its deepest position, if more than 6 calls or interrupts are executed, so that the last return address will be lost. It will also remain in its highest position if the stack is empty and a RET or RETI is executed. In this case the next instruction will be executed.

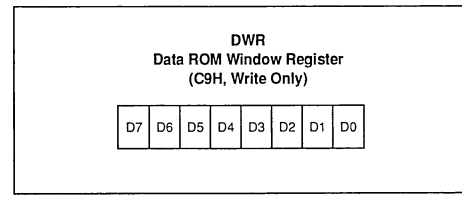
Memory Registers

Figure 9. Data RAM Bank Register



The DRBR register can be addressed like a RAM location in the Data Space at the E8H address, nevertheless it is write-only register that can not be accessed with single-bit operations. This register is used to select the desired 64-byte RAM/EEPROM bank of the Data Space. The number of the bank has to be loaded in the DRBR register and the instruction has to point to the selected location as it was in the 0 bank (from 00H address to 3FH address). This register is cleared during the MCU initialization (the Data space 0 bank is automatically addressed after the Reset). Refer to the Data Space description for additional information. The DRBR register is not modified when a interrupt or a subroutine occurs.

Figure 10. Data ROM Window Register

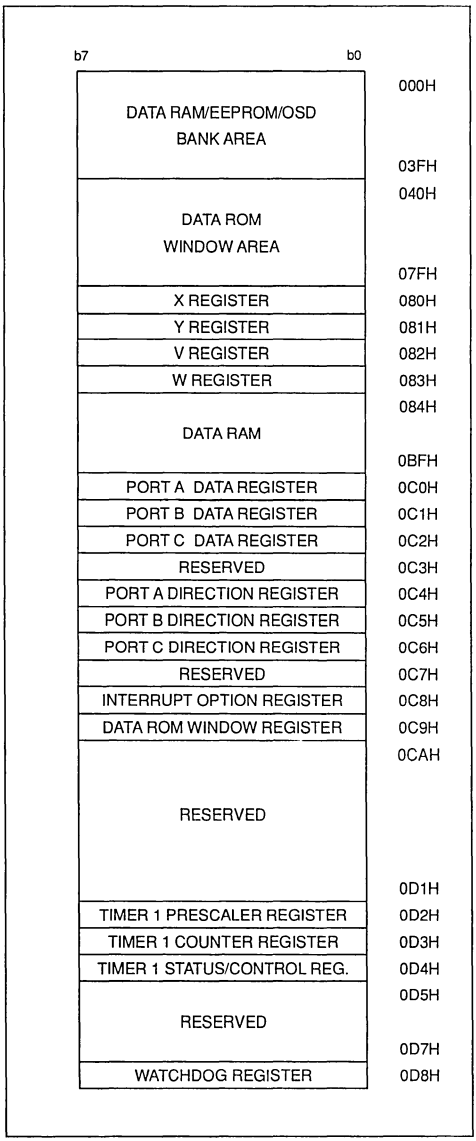


The DWR register can be addressed like a RAM location in the Data Space at the C9H address, nevertheless it is write-only register that can not be accessed with single-bit operations. This register is used to move up and down the 64-byte read-only data window (from the 40H address to 7FH address of the Data Space) along the ROM memory of the MCU by step of 64 bytes. The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 less significant bits of the address given in the instruction (as less significant bits) and the content of the DWR register (as most significant bits). Refer to the Data Space description for additional information.

MEMORY SPACES

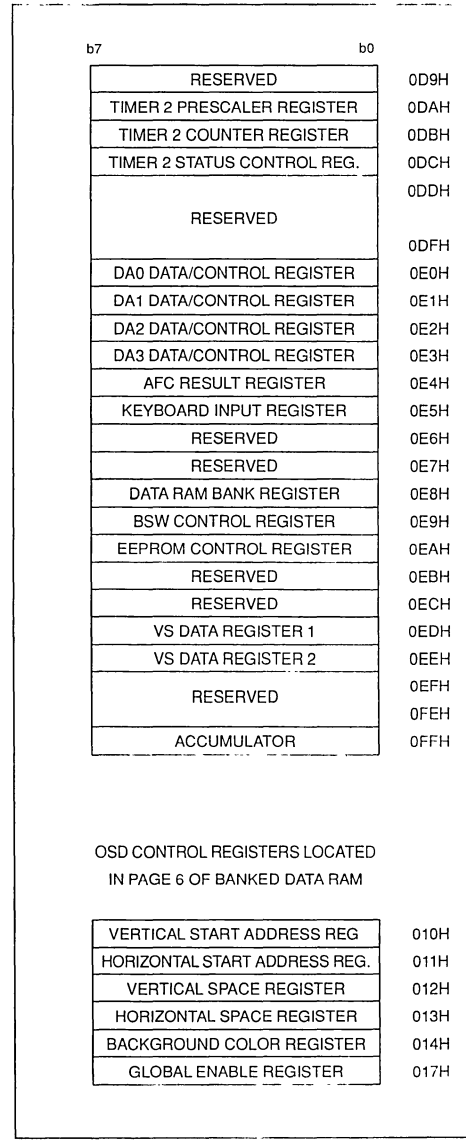
The MCUs operate in three different memory spaces: Program Space, Data Space, and Stack Space. A description of these spaces is shown in Figure 11 and Figure 12.

Figure 11. ST634X Data Space



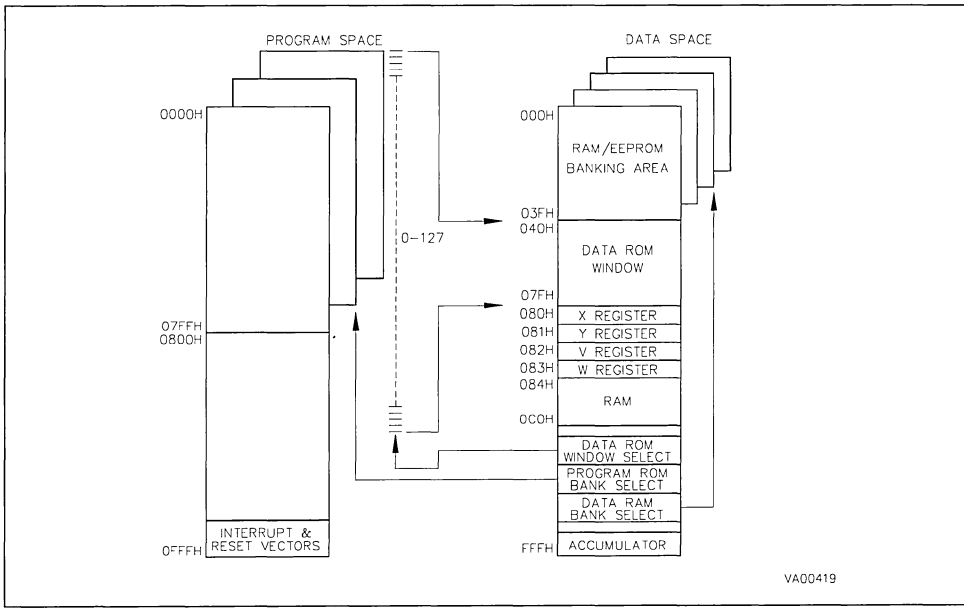
Note : The register CAh must be reset to zero in order to ensure compatibility with the emulator and pggybacks.

Figure 12. ST634X Data Space (Continued)



MEMORY SPACES (Continued)

Figure 13. ST63XX Memory Addressing Description Example



Program Space

The program space is physically implemented in the ROM memory and includes all the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, the reserved test area and user vectors. It is addressed thanks to the 12-bit Program Counter register (PC register) and so, the ST63XX Core can directly address up to 4K bytes of Program Space. On ST634X a total of 4096 bytes of ROM have been implemented; 3884 are available as user ROM while 214 are reserved for testing.

Data Space

The instruction set of the ST63XX Core operates on a specific space, named Data Space that contains all the data necessary for the processing of the program. The Data Space allows the addressing of RAM memory, EEPROM memory, ST63XX Core/peripheral registers, and read-only data such as constants and the look-up tables.

Data ROM Addressing. All the read-only data are physically implemented in the ROM memory in which the Program Space is also implemented. The ROM memory therefore contains the program to be executed and also the constants and the look-up tables needed for the program. The locations of Data Space in which the different constants and look-up tables are addressed by the ST63XX Core can be considered as being a 64-byte window through which it is possible to access to the read-only data stored in the ROM memory. This window is located from the 40H address to the 7FH address in the Data space and allows the direct reading of the bytes from the 000H address to the 03FH address in the ROM memory. All the bytes of the ROM memory can be used to store either instructions or read-only data. Indeed, the window can be moved by step of 64 bytes along the ROM memory in writing the appropriate code in the Write-only Data ROM Window register (DWR register, location C9H). The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 less significant bits of the address in the Data Space (as less significant bits) and the content of the DWR register (as most significant bits). So when addressing location 40H of data space, and 0 is loaded in the DWR register, the physical addressed location in ROM is 00H.

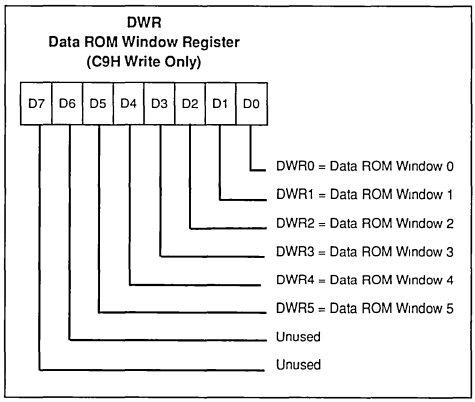
MEMORY SPACE (Continued)

Table 3. ST634X Program ROM Memory Map

ROM Page	Device Address	EPROM Address (1)	Description
PAGE 0	0000H-007FH 0080H-07FFH	0000H-007FH 0080H-07FFH	Reserved User ROM
PAGE 1 "STATIC"	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	User ROM Reserved Interrupt Vectors Reserved NMI Vector Reset Vector

Note 1. EPROM addresses are related to the use of ST63PXX piggyback emulation devices.

Figure 14. Data ROM Window Register



D6,D7. This bit is not used however care should be taken to reset these bits to ensure compatibility with the emulator and piggybacks.

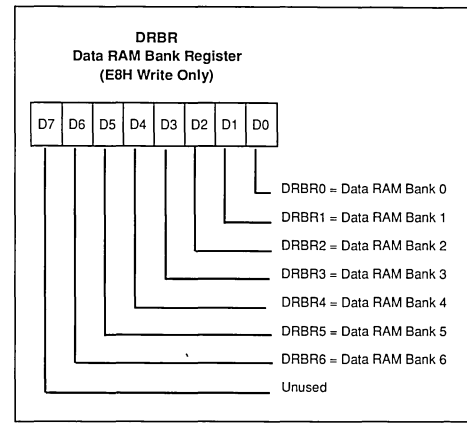
DWR6-DWR0. These are the Data Rom Window bits that correspond to the upper bits of data ROM program space. This register is undefined after reset.

Notes Care is required when handling the DWR register as it is write only. For this reason, it is not allowed to change the DWR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the DWR it writes also the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DWR register is not affected.

Data RAM/EEPROM/OSD RAM Addressing

In ST634X 64 bytes of data RAM are directly addressable in the data space from 80H to BFH addresses. The 48 bytes of EEPROM memory and the OSD RAM can be addressed using the banks of 64 bytes located between addresses 00H and 3FH. The selection of the bank is done by programming the Data RAM Bank Switching register (DRBR register) located at the E8H address of the Data Space. In this way each bank of EEPROM or OSD RAM can be selected 64 bytes at a time. No more than one bank should be set at a time.

Figure 15. Data RAM Bank Register



D7. This bit is not used.

DRBR6, DRBR5. Each of these bits, when set, will select one OSD RAM register page.

MEMORY SPACE (Continued)

DRBR4,DRBR3,DRBR2. Each of these bits, when set, will select one RAM page.

DRBR1,DRBR0. These bits select the EEPROM pages. Table 5 summarizes how to set the Data RAM Bank Register in order to select the various banks or pages.

This register is undefined after reset.

Notes :
Care is required when handling the DRBR register as it is write only. For this reason, it is not allowed to change the DRBR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the DRBR it writes also the image register.
The image register must be written first, so if an interrupt occurs between the two instructions the DRBR register is not affected.

Table 4. Data RAM Bank Register Set-up

DRBR Value	Selection
01H	EEPROM Page 0
20H	OSD Page 5
40H	OSD Page 6

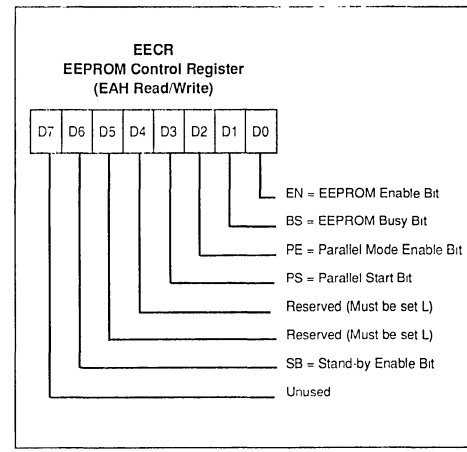
EEPROM Description

Through the programming of the Data RAM Bank Register (DRBR= E8H) the user can select the bank or page leaving unaffected the way to address the static registers. The way to address the "dynamic" page is to set the DRBR as described in Table 4 (e.g. to select EEPROM page 0, the DRBR has to be loaded with content 01H, see Data RAM/EEPROM/OSD RAM addressing for additional information). Bit 0 of the DRBR is dedicated to the EEPROM.

The EEPROM module is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. The EEPROM is controlled by the EEPROM Control Register (EECR=EAH). Any EEPROM location can be read just like any other data location, also in terms of access time.

To write an EEPROM location takes about 5 mSec (10mSec max) and during this time the EEPROM is not accessible by the Core. A busy flag can be read by the Core to know the EEPROM status before trying any access. In writing the EEPROM can work in two modes: Byte Mode (BMODE) and Parallel Mode (PMODE). The BMODE is the normal way to use the EEPROM and consists in accessing one byte at a time. The PMODE consists in accessing 8 bytes per time.

Figure 16. EEPROM Control Register



D7. Not used

SB. *WRITE ONLY.* If this bit is set the EEPROM is disabled (any access will be meaningless) and the power consumption of the EEPROM is reduced to the leakage values.

D5, D4. Reserved for testing purposes, they must be set to zero.

PS. *SET ONLY.* Once in Parallel Mode, as soon as the user software sets the PS bit the parallel writing of the 8 adjacent registers will start. PS is internally reset at the end of the programming procedure. Note that less than 8 bytes can be written; after parallel programming the remaining undefined bytes will have no particular content.

PE. *WRITE ONLY.* This bit must be set by the user program in order to perform parallel programming (more bytes per time). If PE is set and the "parallel start bit" (PS) is low, up to 8 adjacent bytes can be written at the maximum speed, the content being stored in volatile registers. These 8 adjacent bytes can be considered as row, whose A7, A6, A5, A4, A3 are fixed while A2, A1 and A0 are the changing bytes. PE is automatically reset at the end of any parallel programming procedure. PE can be reset by the user software before starting the programming procedure, leaving unchanged the EEPROM registers.

MEMORY SPACE (Continued)

BS. *READ ONLY.* This bit will be automatically set by the CORE when the user program modifies an EEPROM register. The user program has to test it before any read or write EEPROM operation; any attempt to access the EEPROM while "busy bit" is set will be aborted and the writing procedure in progress completed.

EN. *WRITE ONLY.* This bit MUST be set to one in order to write any EEPROM register. If the user program will attempt to write the EEPROM when EN= 0 the involved registers will be unaffected and the "busy bit" will not be set.

After RESET the content of EECR register will be 00H.

Notes :
When the EEPROM is busy (BS= 1) the EECR can not be accessed in write mode, it is only possible to read BS status. This implies that as long as the EEPROM is busy it is not possible to change the status of the EEPROM control register. EECR bits 4 and 5 are reserved for testing purposes, and the user must never set them to 1.

Additional Notes on Parallel Mode. If the user wants to perform a parallel programming the first action should be the set to one the PE bit; from this moment the first time the EEPROM will be addressed in writing, the ROW address will be latched and it will be possible to change it only at the end of the programming procedure or by resetting PE without programming the EEPROM. After the ROW address latching the Core can "see" just one EEPROM row (the selected one) and any attempt to write or read other rows will produce errors. Do not read the EEPROM while PR is set.

As soon as PE bit is set, the 8 volatile ROW latches are cleared. From this moment the user can load data in the whole ROW or just in a subset. PS setting will modify the EEPROM registers corresponding to the ROW latches accessed after PE. For example, if the software sets PE and accesses EEPROM in writing at addresses 18H,1AH,1BH and then sets PS, these three registers will be modified at the same time; the remaining bytes will have no particular content. Note that PE is internally reset at the end of the programming procedure. This implies that the user must set PE bit between two parallel programming procedures. Anyway the user can set and then reset PE without performing any EEPROM programming. PS is a set only bit and is internally reset at the end of the programming procedure. Note that if the user tries to set PS while PE is not set there will not be any programming procedure and the PS bit will be unaffected. Consequently PS bit can not be set if EN is low. PS can be affected by the user set if, and only if, EN and PE bits are also set to one.

Warning : *Parallel programming of the EEPROM with less than eight bytes may corrupt other bytes and should therefore be used with care, as here after underlined.*

a. *Reason for limitation:*
betweeen PE (Parallel Enable) and PS (Parallel Start) of the EEPROM, the user writes up to eight bytes into the volatile data registers, a latch is also set to indicate which bytes have been accessed; the accessed bytes will be programmed when PS arrives. The logic is such that it is possible to set the latches of bytes which have NOT been accessed. The latches are set whenever ANY register in the banked dataspace (00h-3FH) is accessed for READ or WRITE between a PE and PS. The latch which is set will be determined by the three least significant bits of the register address. Only the latch is set, so finaal data of a corrupted byte after the parallel programming is always FFH.

Note: *read operations also occur internally to the micro for most instructions. Even if bytes are not seen to be corrupted within the parallel programming routine, care should be taken, since they could become corrupted by an interrupt routine being serviced during loading of parallel bytes.*
This is logic related and is not a marginality or race condition; piggyback devices perform in the same way as ROM devices. Parallel programming is tested with only LDI rr,nn instructions which do not corrupt other bytes.

b. *To Avoid Corrupted Bytes:*
- *use Single Byte Mode, or*
- *always define all eight bytes in Parallel Programming Mode, or*
- *when programming less than eight bytes, the remaining EEPROM bytes should do not used by the program.*

Additional Notes Regarding Differences Between ST63XX Devices and Corresponding Emulators. While PE is set, all the EEPROM page currently selected is accessible in reading and the writing of the bytes happens at the row to which belongs the last byte written before setting PS. The sequence: set PE, write in 10H the value X, write in 21H the value Y, set PS, will result in: 10H unchanged, 20H loaded with value X, 21H loaded with value Y. In the emulator bits 4 and 5 of the EECR are implemented.If the user set to 1 one or both of these bits the contents of the EEPROM will be destroyed. The user should use care in using EEPROM emulation as in general the emulator does not emulate the behaviour of the EEPROM when it is misused.

STACK SPACE

The stack space consists of six 12 bit registers that are used for stacking subroutine and interrupt return addresses plus the current program counter register.

TEST MODE

The test mode can be entered by connecting the TEST pin to an high logic level when reset is active: this action enables the factory test mode. The user is recommended to avoid this situation for normal operation. (TEST pin should be tied to ground).

INTERRUPT

The ST63XX Core can manage 4 different maskable interrupt sources, plus one non-maskable interrupt source (top priority level interrupt). Each source is associated with a particular interrupt vector that contains a Jump instruction to the related interrupt service routine. Each vector is located in the Program Space at a particular address (see Table 5). When a source provides an interrupt request, and the request processing is also enabled by the ST63XX Core, then the PC register is loaded with the address of the interrupt vector (i.e. of the Jump instruction). Finally, the PC is loaded with the address of the Jump instruction and the interrupt routine is processed.

The relationship between vector and source and the associated priority is hardware fixed for the different ST63XX devices. For some interrupt sources it is also possible to select by software the kind of event that will generate the interrupt.

All interrupts can be disabled by writing to the GEN bit (global interrupt enable) of the interrupt option register (address C8H). After a reset, ST63XX is in non maskable interrupt mode, so no interrupts will be accepted and NMI flags will be used, until a RETI instruction is executed. If an interrupt is executed, one special cycle is made by the core, during that the PC is set to the related interrupt vector address. A jump instruction at this address has to redirect program execution to the beginning of the related interrupt routine. The interrupt detecting cycle, also resets the related interrupt flag (not available to the user), so that another interrupt can be stored for this current vector, while its driver is under execution.

If additional interrupts arrive from the same source, they will be lost. NMI can interrupt other interrupt routines at any time, while other interrupts cannot interrupt each other. If more than one interrupt is waiting for service, they are executed according to their priority. The lower the number, the higher the priority. Priority is, therefore, fixed. Interrupts are checked during the last cycle of an instruction (RETI included). Level sensitive interrupts have to be valid during this period.

Table 5 details the different interrupt vectors/sources relationships.

Table 5. Interrupt Vectors/Sources Relationships

Interrupt Source	Associated Vector	Vector Address
IRIN/NMI Pin (1)	Interrupt Vector # 0 (NMI)	0FFCH-0FFDH
None (2)	Interrupt Vector # 1	0FF6H-0FF7H
Vsync	Interrupt Vector # 2	0FF4H-0FF5H
Timer 1	Interrupt Vector # 3	0FF2H 0FF3H
Timer 2	Interrupt Vector # 4	0FF0H-0FF1H

Notes
1 This pin is associated with the NMI Interrupt Vector. Not available on ST6340
2 This vector is not used in ST634X

Interrupt Vectors/Sources

The ST63XX Core includes 5 different interrupt vectors in order to branch to 5 different interrupt routines. The interrupt vectors are located in the fixed (or static) page of the Program Space.

The interrupt vector associated with the non-maskable interrupt source is named interrupt vector #0. It is located at the (FFCH,FFDH) addresses in the Program Space. On ST634X this vector is associated to the rising edge sensitive external interrupt pin.

The interrupt vectors located at addresses (FF6H,FF7H), (FF4H,FF5H), (FF2H,FF3H), (FF0H,FF1H) are named interrupt vectors #1, #2, #3 and #4 respectively. These vectors are associated with VSYNC (#2), TIMER 1 (#3) and TIMER 2 (#4); Interrupt vector (#1) is not used on ST6356,57,58. Refer to the Interrupt Details description for more information.

INTERRUPT (Continued)

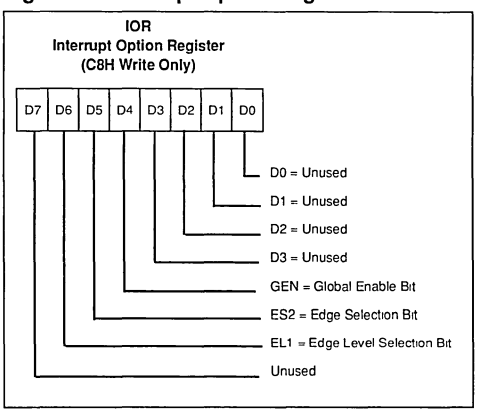
Interrupt Priority

The non-maskable interrupt request has the highest priority and can interrupt any other interrupt routines at any time, nevertheless the other interrupts cannot interrupt each other. If more than one interrupt request is pending, they are processed by the ST63XX Core according to their priority level: vector #1 has the higher priority while vector #4 the lower. The priority of each interrupt source is hardware fixed.

Interrupt Option Register

The Interrupt Option Register (IOR register, location C8H) is used to enable/disable the individual interrupt sources and to select the operating mode of the external interrupt inputs. This register can be addressed in the Data Space as RAM location at the C8H address, nevertheless it is write-only register that can not be accessed with single-bit operations. The operating modes of the external interrupt inputs associated to interrupt vectors #1 and #2 are selected through bits 4 and 5 of the IOR register.

Figure 17. Interrupt Option Register



D7. Not used.

EL1. This is the Edge/Level selection bit of interrupt #1. When set to one, the interrupt is generated on low level of the related signal; when cleared to zero, the interrupt is generated on falling edge. The bit is cleared to zero after reset and as no interrupt source is associated to vector #1 on ST63XX, the user must keep this bit to zero to avoid ghost interrupts from this source.

ES2. This is the edge selection bit on interrupt #2. This bit is used on the ST63XX devices with on-chip OSD generator for VSYNC detection.

GEN. This is the global enable bit. When set to one all interrupts are globally enabled ; when this bit is cleared to zero all interrupts are disabled (including NMI).

D3 - D0. These bits are not used.

Interrupt Procedure

The interrupt procedure is very similar to a call procedure; the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event the user does not know about the context and the time at which it occurred. As a result the user should save all the data space registers which will be used inside the interrupt routines. There are separate sets of processor flags for normal, interrupt and non-maskable interrupt modes which are automatically switched and so these do not need to be saved.

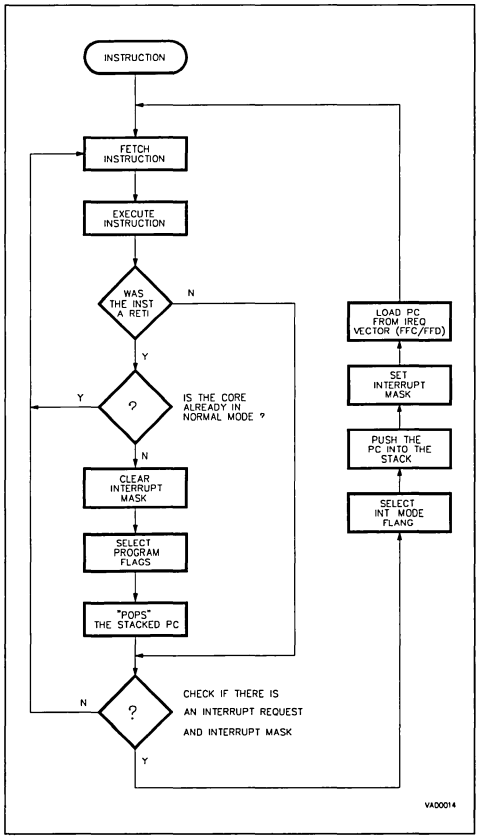
The following list summarizes the interrupt procedure (refer also to Figure 18. Interrupt Processing Flow Chart):

- Interrupt detection
- The flags C and Z of the main routine are exchanged with the flags C and Z of the interrupt routine (resp. the NMI flags)
- The value of the PC is stored in the first level of the stack - The normal interrupt lines are inhibited (NMI still active)
- The edge flip-flop is reset
- The related interrupt vector is loaded in the PC.
- User selected registers are saved inside the interrupt service routine (normally on a software stack)
- The source of the interrupt is found by polling (if more than one source is associated to the same vector)
- Interrupt servicing
- Return from interrupt (RETI)
- Automatically the ST63XX core switches back to the normal flags (resp the interrupt flags) and pops the previous PC value from the stack

The interrupt routine begins usually by the identification of the device that has generated the interrupt request. The user should save the registers which are used inside the interrupt routine (that holds relevant data) into a software stack.
After the RETI instruction execution, the Core carries out the previous actions and the main routine can continue.

INTERRUPT (Continued)

Figure 18. Interrupt Processing Flow-Chart



ST634X Interrupt Details

IR Interrupt (#0). The IRIN Interrupt is associated with the first interrupt #0 (NMI, 0FFCH). If enabled, then an interrupt will be generated on a rising edge at the pin. The IRIN pin is nt available on ST6340.

Interrupt (#1). On ST634X no sources are associated to vector (#1). To avoid any ghost interrupt due to interrupt (#1) the user must keep to zero the EL1 bit of IOR register.

VSYNC Interrupt (#2). The VSYNC Interrupt is connected to the interrupt #2. When disabled the VSYNCINT signal is low. Bit 5 of the interrupt option register C8H is used to select the negative edge (B2=0) or the positive edge (B2=1); the edge will depend on the application. Note that once an edge has been latched, then the only way to remove the latched signal is to service the interrupt. Care must be taken not to generate spurious interrupts. This interrupt may be used for synchronize to the VSYNC signal in order to change characters in the OSD only when the screen is on vertical blanking (if desired). This method may also be used to blink characters.

TIMER 1 Interrupt (#3). The TIMER 1 Interrupt is connected to the fourth interrupt #3 (0FF2H) which detects a high to low level (latched in the timer). For more information on the timer interrupt refer to the timer section.

Timer 2 Interrupt (#4). The TIMER 2 Interrupt is connected to the fifth interrupt #4 (0FF0H) which detecty a high to low level (latched in the timer). For more information on the timer interrupt refer to the timer section.

Notes Global disable does not reset edge sensitive interrupt flags. These edge sensitive interrupts become pending again when global disabling is released. Moreover, edge sensitive interrupts are stored in the related flags also when interrupts are globally disabled, unless each edge sensitive interrupt is also individually disabled before the interrupting event happens. Global disable is done by clearing the GEN bit of Interrupt option register, while any individual disable is done in the control register of the peripheral. The on-chip Timer peripherals have an interrupt request flag bit (TMZ), this bit is set to one when the device wants to generate an interrupt request and a mask bit (ETI) that must be set to one to allow the transfer of the flag bit to the Core.

RESET

The ST63XX devices can be reset in two ways: by the external reset input (RESET) tied low and by the hardware activated digital watchdog peripheral.

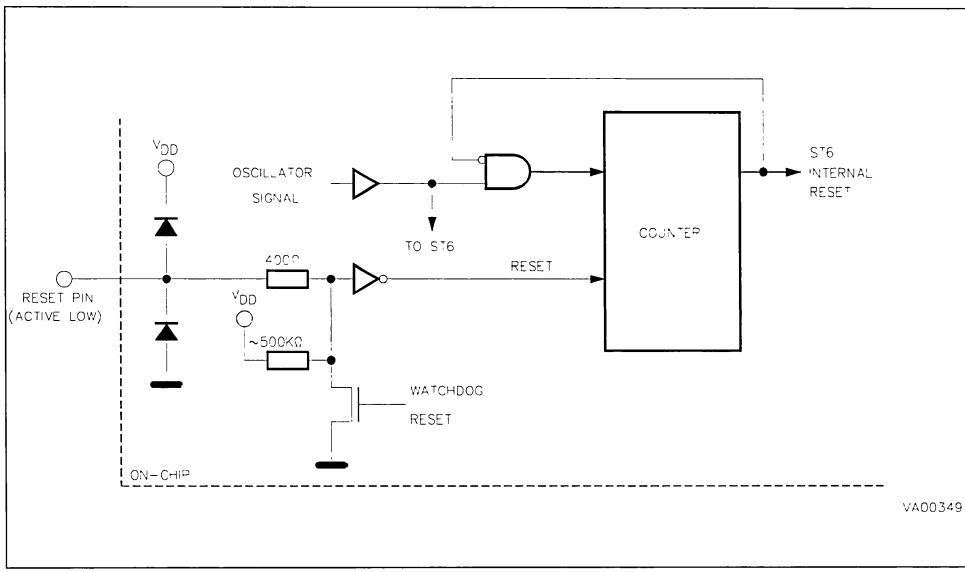
RESET Input

The external active low reset pin is used to reset the ST63XX devices and provide an orderly software startup procedure. The activation of the Reset pin may occur at any time in the RUN or WAIT mode. Even short pulses at the reset pin will be accepted since the reset signal is latched internally and is only cleared after 2048 clocks at the oscillator pin. The clocks from the oscillator pin to the reset circuitry are buffered by a schmit trigger so that an oscillator in start-up conditions will not give spurious clocks. The MCU is configured in the Reset mode as long as the signal of the RESET pin is low. The processing of the program is stopped and the standard Input/Output ports (port A, port B and port C) are in the input state (except PC2). As soon as the level on the reset pin becomes high, the initialization sequence is executed. Refer to the MCU initialization sequence for additional information.

Watchdog Reset

The ST63XX devices are provided with an on-chip hardware activated digital watchdog function in order to provide a graceful recovery from a software upset. If the watchdog register is not refreshed and the end-of-count is reached, then the reset state will be latched into the MCU and an internal circuit pulls down the reset pin. This also resets the watchdog which subsequently turns off the pull-down and activates the pull-up device at the reset pin. This causes the positive transition at the reset pin. The MCU will then exit the reset state after 2048 clocks on the oscillator pin.

Figure 19. Internal Reset Circuit



RESET (Continued)

Figure 20. Reset & Interrupt Processing Flow-chart

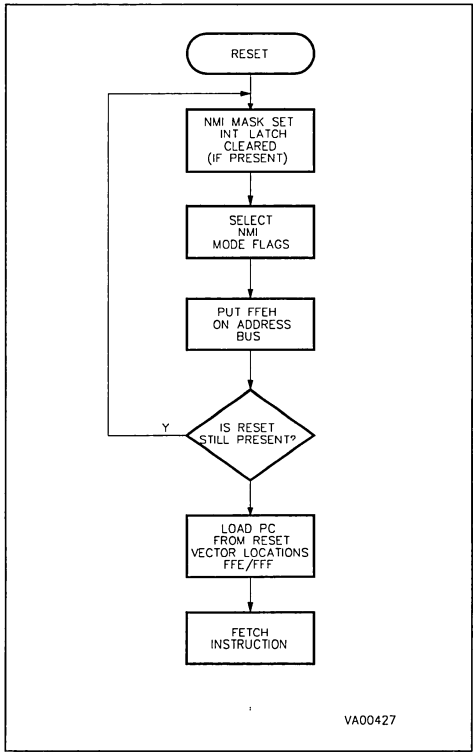
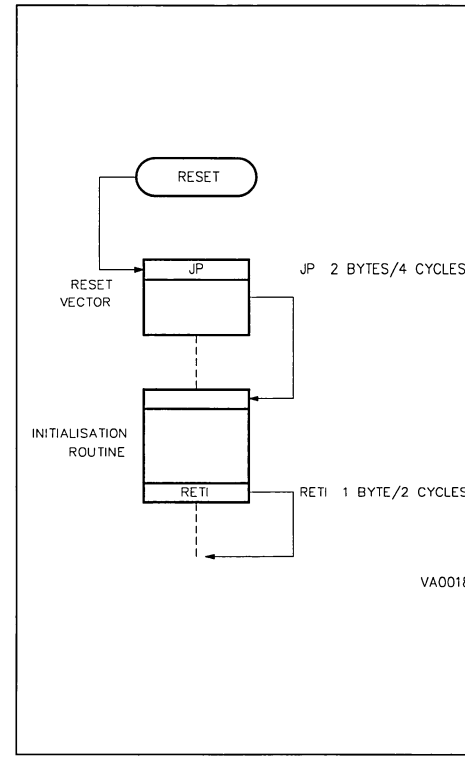


Figure 21. Restart Initialization Program Flow-chart



Application Notes

An external resistor between V_{DD} and the reset pin is not required because an internal pull-up device is provided. The user may prefer to add an external pull-up resistor.

An internal Power-on device does not guarantee that the MCU will exit the reset state when V_{DD} is above 4.5V and therefore the RESET pin should be externally controlled.

MCU Initialization Sequence

When a reset occurs the stack is reset to program counter, the PC is loaded with the address of the reset vector (located in the program ROM at addresses FFEH & FFFH). A jump instruction to the beginning of the program has to be written into these locations. After a reset the interrupt mask is automatically activated so that the Core is in non-maskable interrupt mode to prevent false or ghost interrupts during the restart phase. Therefore the restart routine should be terminated by a RETI instruction to switch to normal mode and enable interrupts. If no pending interrupt is present at the end of the reset routine, the ST63XX will continue with the instruction after the RETI; otherwise the pending interrupt will be serviced.

WAIT & STOP MODES

The STOP and WAIT modes have been implemented in the ST63XX Core in order to reduce the consumption of the device when the latter has no instruction to execute. These two modes are described in the following paragraphs. On ST63XX as the hardware activated digital watchdog function is present the STOP instruction is de-activated and any attempt to execute it will cause the automatic execution of a WAIT instruction.

WAIT Mode

The configuration of the MCU in the WAIT mode occurs as soon as the WAIT instruction is executed. The microcontroller can also be considered as being in a "software frozen" state where the Core stops processing the instructions of the routine, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage but where the peripherals are still working.

The WAIT mode is used when the user wants to reduce the consumption of the MCU when it is in idle, while not loosing count of time or monitoring of external events. The oscillator is not stopped in order to provide clock signal to the peripherals. The timers counting may be enabled (writing the PSI bit in TSCR register) and the timer interrupt may be also enabled before entering the WAIT mode: this allows the WAIT mode to be left when timer interrupt occurs. If the exit from the WAIT mode is performed with a general RESET (either from the activation of the external pin or by watchdog reset) the MCU will enter a normal reset procedure as described in the RESET chapter. If an interrupt is generated during WAIT mode the MCU behaviour depends on the state of the ST63XX Core before the initialization of the WAIT sequence, but also of the kind of the interrupt request that is generated. This case will be described in the following paragraphs. In any case, the ST63XX Core does not generate any delay after the occurrence of the interrupt because the oscillator clock is still available.

STOP Mode

On ST63XX the hardware watchdog is present and the STOP instruction has been de-activated Any attempt to execute a STOP will cause the automatic execution of a WAIT instruction.

Exit from WAIT Mode

The following paragraphs describe the output procedure of the ST63XX Core from WAIT mode when an interrupt occurs. It must be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non maskable interrupt mode) before the start of the WAIT sequence, but also of the type of the interrupt request that is generated

Normal Mode. If the ST63XX Core was in the main routine when the WAIT instruction has been executed the ST63XX Core outputs from the wait mode as soon as any interrupt occurs; the related interrupt routine is executed and at the end of the interrupt service routine the instruction that follows the WAIT instruction is executed if no other interrupts are pending.

Non-maskable Interrupt Mode. If the WAIT instruction has been executed during the execution of the non-maskable interrupt routine, the ST63XX Core outputs from the wait mode as soon as any interrupt occurs: the instruction that follows the WAIT instruction is executed and the ST63XX Core is still in the non-maskable interrupt mode even if an other interrupt has been generated.

Normal Interrupt Mode. If the ST63XX Core was in the interrupt mode before the initialization of the WAIT sequence, it outputs from the wait mode as soon as any interrupt occurs. Nevertheless, two cases have to be considered:

- If the interrupt is a normal interrupt, the interrupt routine in which the WAIT was entered will be completed with the execution of the instruction that follows the WAIT and the ST63XX Core is still in the interrupt mode. At the end of this routine pending interrupts will be serviced in accordance to their priority.
- If the interrupt is a non maskable interrupt, the non-maskable routine is processed at first Then the routine in which the WAIT was entered will be completed with the execution of the instruction that follows the WAIT and the ST63XX Core is still in the normal interrupt mode

Notes :

If all the interrupt sources are disabled, the restart of the MCU can only be done by a Reset activation The Wait instruction is not executed if an enabled interrupt request is pending. In the ST63XX the hardware activated digital watchdog function is present As the watchdog is always activated the STOP instruction is de-activated and any attempt to execute the STOP instruction will cause an execution of a WAIT instruction.

ON-CHIP CLOCK OSCILLATOR

The internal oscillator circuit is designed to require a minimum of external components. A crystal quartz, a ceramic resonator, or an external signal (provided to the OSCIN pin) may be used to generate a system clock with various stability/cost tradeoffs. The typical clock frequency is 8MHz. Please note that different frequencies will affect the operation of those peripherals (D/As, SPI, 62.5 KHz OUT) whose reference frequencies are derived from the system clock.

The different clock generator options connection methods are shown in Figure 22, crystal specifications and suggested PC board layouts are given in Figure 23 and Figure 24. One machine cycle takes 13 oscillator pulses; 12 clock pulses are needed to increment the PC while and additional 13th pulse is needed to stabilize the internal latches during memory addressing. This means that with a clock frequency of 8MHz the machine cycle is 1.625µSec.

The crystal oscillator start-up time is a function of many variables: crystal parameters (especially RS), oscillator load capacitance (CL), IC parameters, ambient temperature, and supply voltage.It must be observed that the crystal or ceramic leads and circuit connections must be as short as possible. Typical values for CL1 and CL2 are in the range of 15pF to 22pF but these should be chosen based on the crystal manufacturers specification. Typical input capacitance for OSCIN and OSCOUT pins is 5pF.

The oscillator output frequency is internally divided by 13 to produce the machine cycle and by 12 to produce the Timer and the Watchdog clock. A byte cycle is the smallest unit needed to execute any operation (i.e., increment the program counter). An instruction may need two, four, or five byte cycles to be executed (See Table 6).

Figure 22. Clock Generator Options

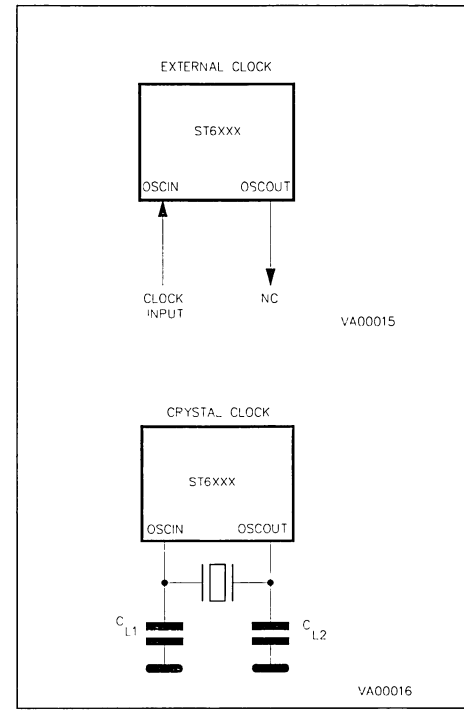
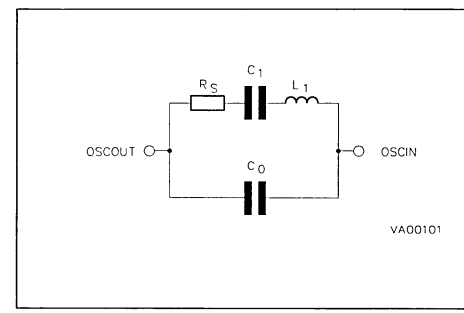


Table 6. Instructions Timing with 8MHz Clock

Instruction Type	Cycles	Execution Time
Branch if set/reset	5 Cycles	8.125µs
Branch & Subroutine Branch	4 Cycles	6.50µs
Bit Manipulation	4 Cycles	6.50µs
Load Instruction	4 Cycles	6.50µs
Arithmetic & Logic	4 Cycles	6.50µs
Conditional Branch	2 Cycles	3.25µs
Program Control	2 Cycles	3.25µs

Figure 23. Crystal Parameters



ON-CHIP CLOCK OSCILLATOR (Continued)

Figure 24. PC Board Layouts Examples

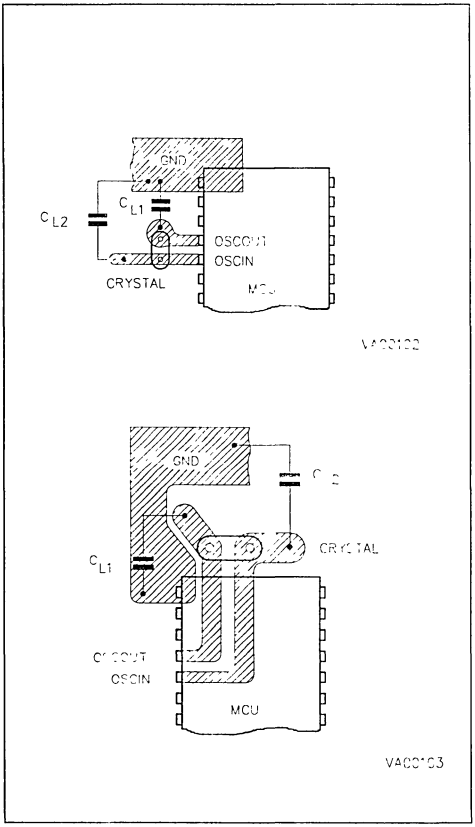
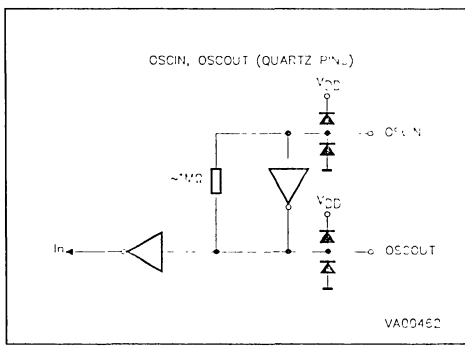


Figure 25. OSCIN, OSCOUT Configuration Diagram



INPUT/OUTPUT PORTS

The ST63XX microcontrollers use three standard I/O ports (A,B,C) with up to eight pins on each port; refer to the device pin configurations to see which pins are available.

Each line can be individually programmed either in the input mode or the output mode as follows by software.

- Output
- Input with on-chip pull-up resistor (selected by software)
- Input without on-chip pull-up resistor (selected by software)

In output mode the following hardware configurations are available:

- Open-drain output 5V (PA0-PA7)
- Open-drain output 5V (PC3, PC5, PC6)
- Push-pull output (PB0-PB3, PC2,PC4)

The lines are organized in three ports (port A,B.C). The ports occupies 6 registers in the data space. Each bit of these registers is associated with a particular line (for instance, the bits 0 of the Port A Data and Direction registers are associated with the PA0 line of Port A).

There are three Data registers (DRA, DRB, DRC), that are used to read the voltage level values of the lines programmed in the input mode, or to write the logic value of the signal to be output on the lines configured in the output mode. The port Data Registers can be read to get the effective logic levels of the pins, but they can be also written by the user software, in conjunction with the related Data Direction Register, to select the different input mode options. Single-bit operations on I/O registers (bit set/reset instructions) are possible but care is necessary because reading in input mode is done from I/O pins and therefore they might be influenced by the external load, while writing will directly affect the Port data register causing an undesired changes of the input configuration. The three Data Direction registers (DDRA, DDRB,DDRB) allow the selection of the direction of each pin (input or output).

All the I/O registers can be read or written as any other RAM location of the data space, so no extra RAM cell is needed for port data storing and manipulation. During the initialization of the MCU, all the I/O registers are cleared and the input mode with pull-up is selected on all the pins thus avoiding pin conflicts (with the exception of PC2 that is set in output mode and is set low).

INPUT/OUTPUT PORTS (Continued)

Details of I/O Ports

When programmed as an input a pull-up resistor (if available) can be switched active under program control. When programmed as an output the I/O port will operate either in the push-pull mode or the open-drain mode according to the hardware fixed configuration as specified below.

Port A is available as an open-drain only (no push-pull programmability and no resistive pull-up in input mode) capable of withstanding 5V.

Some Port B and C lines are also used as I/O buffers for signals coming from the on-chip OSD. In this case the final signal on the output pin is equivalent to a wired AND with the programmed data output. If the user needs to use the OSD, then the I/O line should be set in output mode while the open-drain configuration is harware fixed ; the corresponding data bit must set to one.

PB2 and PB3 must be programmed in input mode to provide the HSYNC and VSYNC signal to the OSD.

On ST634X the I/O pins with double or special functions are:

- PB2/VSYNC (connected to the OSD VSYNC signal)
- PB3/HSYNC (connected to the OSD HSYNC signal)
- PC2/ON-OFF, this I/O is specially suited for TV SET ON-OFF and for this reason at reset the related Data Direction bit will be automatically set to one (I/O line is in output mode), while the rest of the port is in input mode.
- PC3/BLANK (connected to the OSD Blank signal)
- PC5/R, PC6/G (connected to the OSD R-G signals)

All the Port A, B and C I/O lines have Schmitt-trigger input configuration with a typical hysteresis of 1V.

I/O Pin Programming

Each pin can be individually programmed as input or output with different input and output configurations.

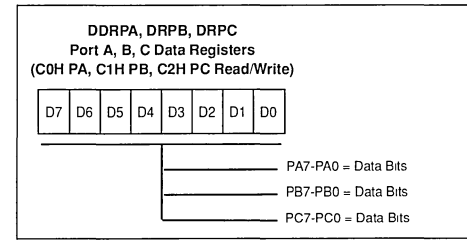
This is achieved by writing to the relevant bit in the data (DR) and data direction register (DDR). Table 8 shows all the port configurations that can be selected by the user software.

Table 7. I/O Port Options Selection

DDR	DR	Mode	Option
0	0	Input	With on-chip pull-up resistor
0	1	Input	Without on-chip pull-up resistor
1	X	Output	Open-drain or Push-Pull

Note: X· Means don't care

Figure 26. I/O Port Data Registers



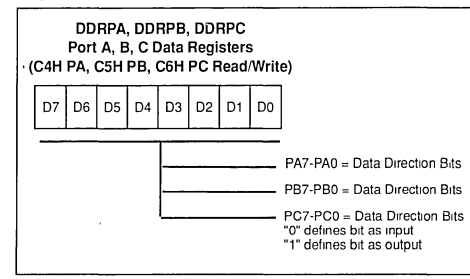
PA7-PA0. These are the I/O port A data bits with open-drain configuration.
Reset at power on.

PB3-PB0. These are the I/O Port B data bits. Reset at power on.

PC3-PC6. These are the I/O port C data bits. Reset at power on.

PC2/ON-OFF. This is a general purpose I/O line suitable for TV set ON-OFF. Reset at power on.

Figure 27. I/O Port Data Direction Registers



PA7-PA0. These are the I/O port A data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Reset at power-on.

INPUT/OUTPUT PORTS (Continued)

PB3-PB0. These are the I/O port B data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Reset at power-on.

PC6-PC2. These are the I/O port C data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Set to 04H at power-on. Bit 2 (PC2 pin) is set to one (output mode selected) as this line is intended for TV ON-OFF switching.

Input/Output Configurations

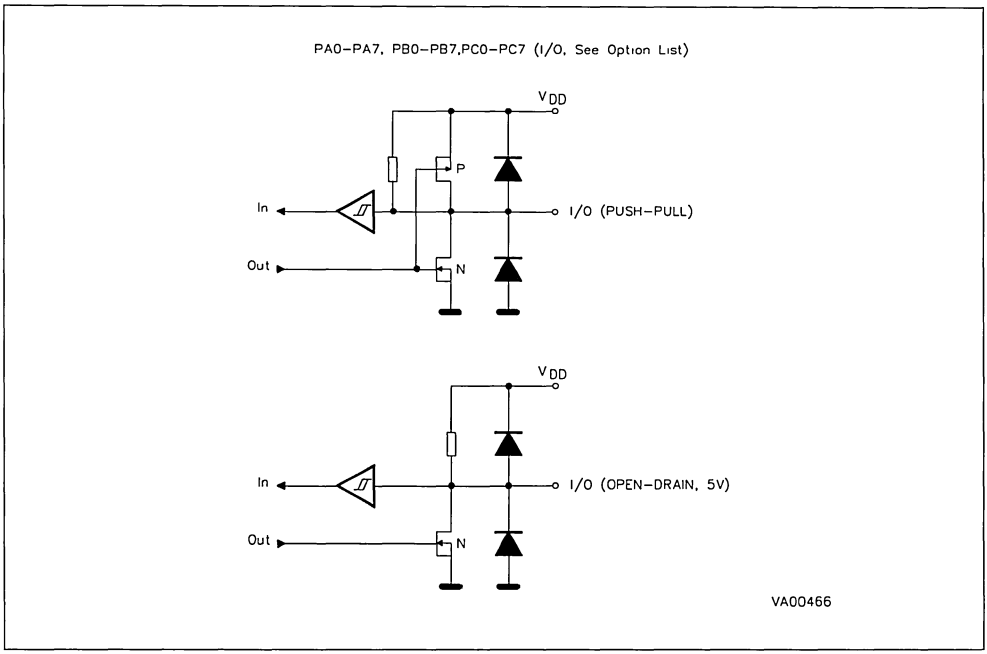
The following schematics show the I/O lines hardware configuration for the different options. Figure 29 shows the I/O configuration for an I/O pin with open-drain capability. Figure 28 shows the I/O configuration for an I/O pin with push-pull and with open drain 5V capability.

Notes :

The WAIT instruction allows the ST63XX to be used in situations where low power consumption is needed. This can only be achieved however if the I/O pins either are programmed as inputs with well defined logic levels or have no power consuming resistive loads in output mode. As the same die is used for the different ST63XX versions the unavailable I/O lines of ST63XX should be programmed in output mode.

Single-bit operations on I/O registers are possible but **care is necessary** because reading in input mode is done from I/O pins while writing will directly affect the Port data register causing an undesired changes of the input configuration.

Figure 28. Port A,B & C I/O Configuration Diagram



TIMERS

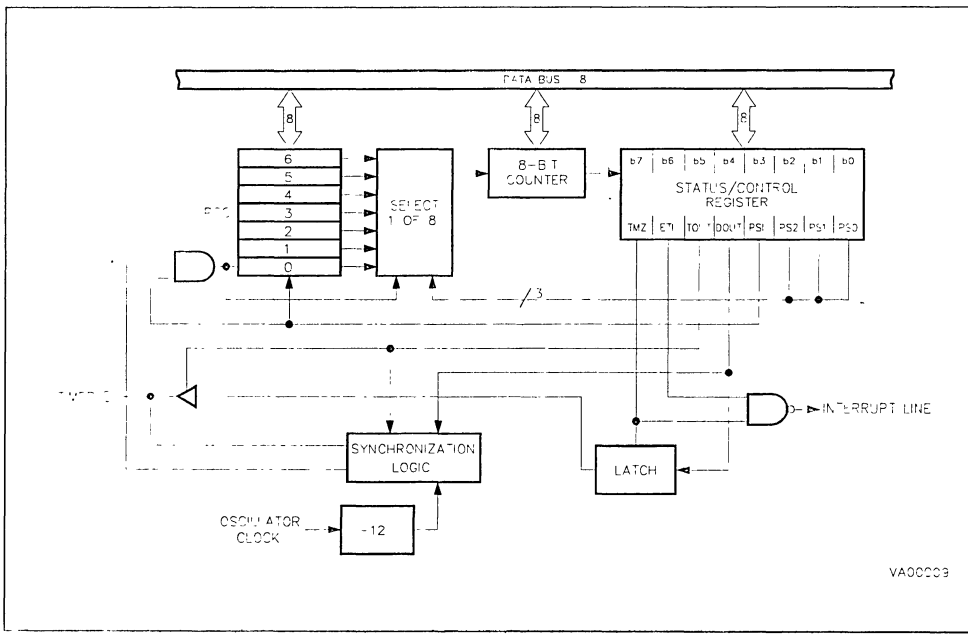
The ST63XX devices offer two on-chip Timer peripherals consisting of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes. Figure 30 shows the timer block diagram. These timers do not have the external TIMER pin available for the user. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR that can be addressed in the data space as RAM location at the D3H (Timer 1) and DBH (Timer 2) addresses. The state of the 7-bit prescaler can be read in the PSC register at the D2H (Timer 1) and DAH (Timer 2) addresses. The control logic device can be managed thanks to the TSCR register D4H (Timer 1) and DCH (Timer 2) addresses as it is described in the following paragraphs.

The following description applies to both Timer 1 and Timer 2. The 8-bit counter is decrement by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (timer zero) bit in the TSCR is set to one. If the ETI (enable timer interrupt) bit in the TSCR is also set to one an interrupt request, associated to interrupt vector #3 (for Timer 1) and #4 for (Timer 2), is generated. The interrupt of the timer can be used to exit the MCU from the WAIT mode.

The prescaler decrements on rising edge. The prescaler input can be the oscillator frequency divided by 12 or an external clock at TIMER pin (this is not available in ST63XX).
Depending on the division factor programmed by PS2/PS1/PS0 (see table 9) bits in the TSCR, the clock input of the timer/counter register is multiplexed to different sources.
On division factor 1, the clock input of the prescaler is also that of timer/counter; on factor 2, bit 0 of prescaler register is connected to the clock input of TCR.

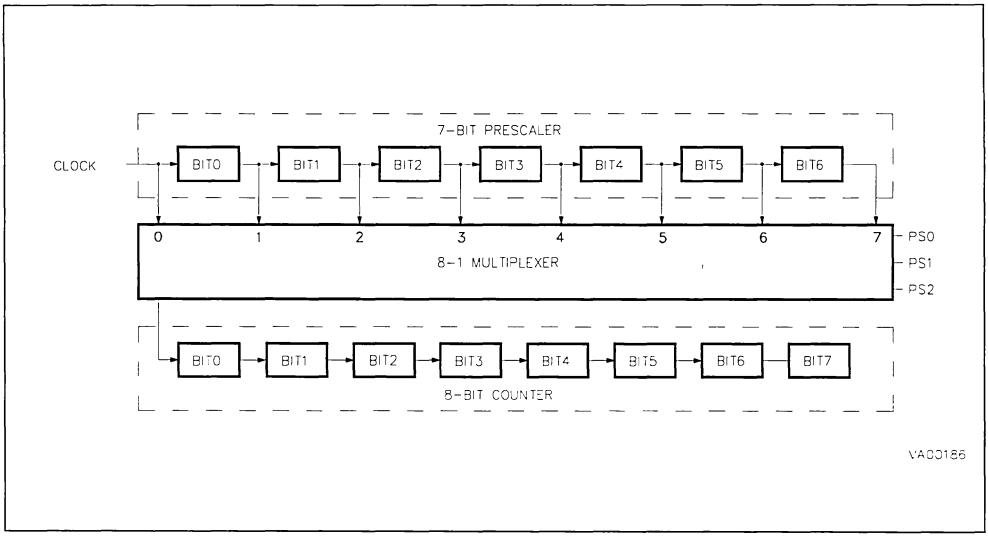
This bit changes its state with the half frequency of prescaler clock input. On factor 4, bit 1 of PSC is connected to clock input of TCR, and so on. On division factor 128, the MSB bit 6 of PSC is connected to, clock input of TCR. The prescaler initialize bit (PSI) in the TSCR register must be set to one to allow the prescaler (and hence the counter) to start. If it is cleared to zero then all of the prescaler bits are set to one and the counter is inhibited from counting.

Figure 30. Timer Peripheral Block Diagram



TIMERS (Continued)

Figure 31. Timer Working Principle



The prescaler can be given any value between 0 and 7FH by writing to the related register address, if bit PSI in the TSCR register is set to one. The tap of the prescaler is selected using the PS2/PS1/PS0 bits in the control register. Figure 36 shows the timer working principle.

Timer Operating Modes

As on ST63XX devices the external TIMER pin is not available the only allowed operating mode is the output mode that have to be selected by setting to 1 bit 4 and by clearing to 0 bit 5 in the TSCR1 register. This procedure will enable both Timer 1 and Timer 2. Any other combination written into these two bits will disable any Timer 1 and Timer 2 operation.

Output Mode (TSCR1 D4 = 1, TSCR1 D5 = 0). On this mode the timer prescaler is clocked by the prescaler clock input (OSC/12). The user can select the desired prescaler division ratio through the PS2/PS1/PS0 bits. When TCR count reaches 0, it sets the TMZ bit in the TSCR.

The TMZ bit can be tested under program control to perform a timer function whenever it goes high. Bit D4 and D5 on TSCR2 (Timer 2) register are not implemented.

Timer Interrupt

When the counter register decrements to zero and the software controlled ETI (enable timer interrupt) bit is set to one then an interrupt request associated to interrupt vector #3 (for Timer 1) and to interrupt vector #4 (for Timer 2) is generated. When the counter decrements to zero also the TMZ bit in the TSCR register is set to one.

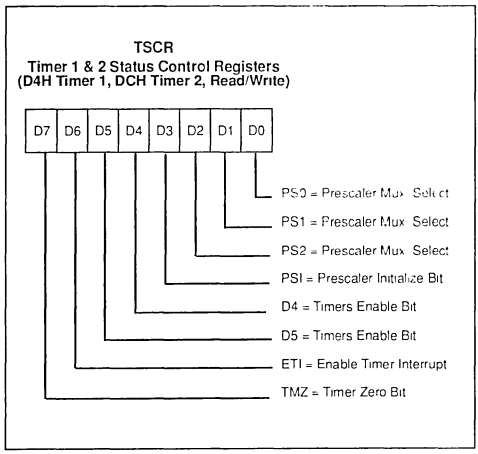
Notes :
TMZ is set when the counter reaches 00H ; however, it may be set by writing 00H in the TCR register or setting the bit 7 of the TSCR register. TMZ bit must be cleared by user software when servicing the timer interrupt to avoid undesired interrupts when leaving the interrupt service routine. After reset, the 8-bit counter register is loaded to FFH while the 7-bit prescaler is loaded to 7FH , and the TSCR register is cleared which means that timer is stopped (PSI=0) and timer interrupt disabled.

A write to the TCR register will predominate over the 8-bit counter decrement to 00H function, i.e. if a write and a TCR register decrement to 00H occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter reaches 00H again. The values of the TCR and the PSC registers can be read accurately at any time.

TIMERS (Continued)

Timer Registers

Figure 32. Timer Status Control Registers



TMZ. Low-to-high transition indicates that the timer count register has decrement to zero. This bit must be cleared by user software before to start with a new count.

ETI. This bit, when set, enables the timer interrupt (vector #3 for Timer 1, vector #4 for Timer 2) request. If ETI=0 the timer interrupt is disabled. If ETI= 1 and TMZ= 1 an interrupt request is generated.

D5. This is the timers enable bit D5. It must be cleared to 0 together with a set to 1 of bit D4 to enable both Timer 1 and Timer 2 functions. It is not implemented on TSCR2 register. Any other combination of TSCR1 D4 and D5 bits will disable any operation of both Timer 1 and Timer 2.

D4. This is the timers enable bit D4. It must be set to 1 together with a clear to 0 of bit D5 to enable both Timer 1 and Timer 2 functions. It is not implemented on TSCR2 register. Any other combination of TSCR1 D4 and D5 bits will disable any operation of both Timer 1 and Timer 2.

PSI. Used to initialize the prescaler and inhibit its counting while PSI = 0 the prescaler is set to 7FH and the counter is inhibited. When PSI = 1 the prescaler is enabled to count downwards. As long as PSI= 0 both counter and prescaler are not running.

PS2-PS0. These bits select the division ratio of the prescaler register. (see table 8)

The TSCR1 and TSCR2 registers are cleared on reset. The correct D4-D5 combination must be written in TSCR1 by user's software to enable the operation of Timer 1 and Timer 2.

Table 8. Prescaler Division Factors

PS2	PS1	PS0	Divided By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Figure 33. Timer Counter Registers

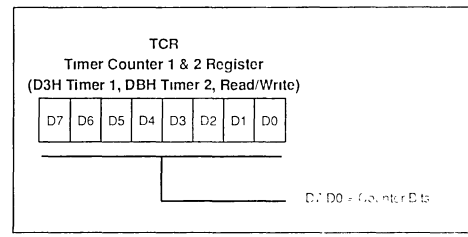
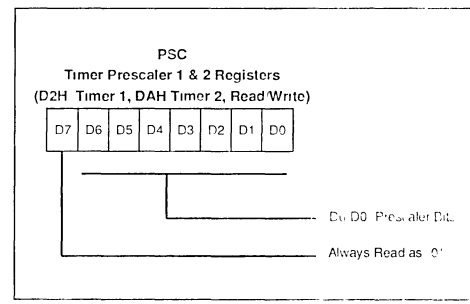


Figure 34. Prescaler Registers



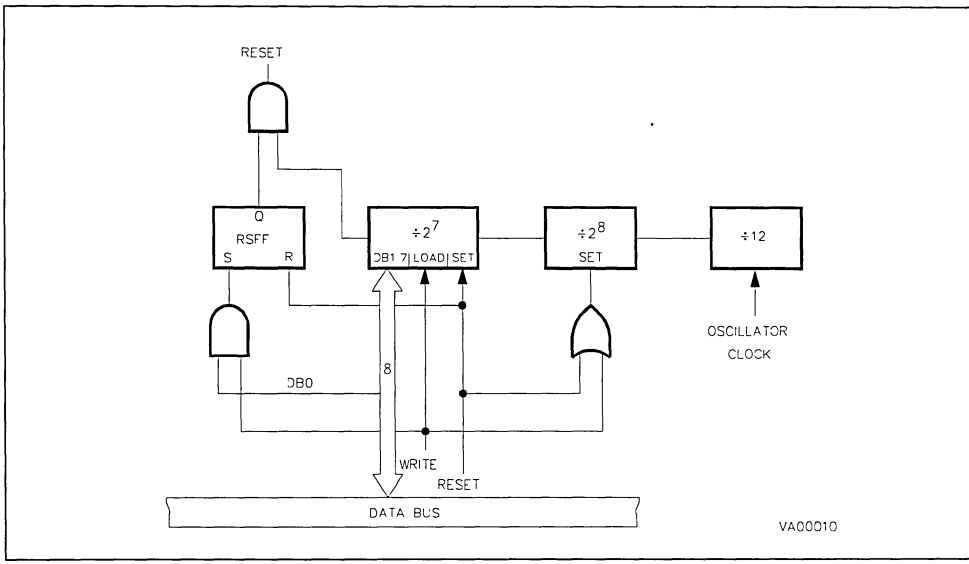
HARDWARE ACTIVATED DIGITAL WATCHDOG FUNCTION

The hardware activated digital watchdog function consists of a down counter that is automatically initialized after reset so that this function does not need to be activated by the user program. As the watchdog function is always activated this down counter can't be used as a timer. The watchdog is using one data space register (HWDR location D8H). The watchdog register is set to FEH on reset and immediately starts to count down, requiring no software start. Similarly the hardware activated watchdog can not be stopped or delayed by software.

The watchdog time can be programmed using the 6 MSbits in the watchdog register, this gives the possibility to generate a reset in a time between 3072 to 196608 oscillator cycles in 64 possible steps. (With a clock frequency of 8MHz this means from 384µs to 24.576ms). The reset is prevented if the register is reloaded with the desired value before bits 2-7 decrement from all zeros to all ones.

The presence of the hardware watchdog deactivates the STOP instruction and a WAIT instruction is automatically executed instead of a STOP. Bit 1 of the watchdog register (set to one at reset) can be used to generate a software reset if cleared to zero). Figure 35 shows the watchdog block diagram while Figure 36 shows its working principle.

Figure 35. Hardware Activated Watchdog Block Diagram



HARDWARE ACTIVATED DIGITAL WATCHDOG FUNCTION (Continued)

Figure 36. Hardware Activated Watchdog Working Principle

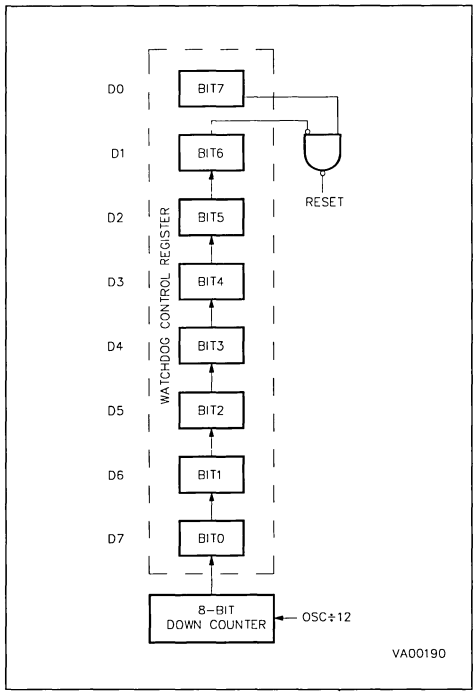
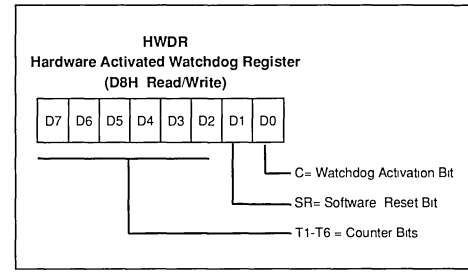


Figure 37. Watchdog Register



T1-T6. These are the watchdog counter bits. It should be noted that D7 (T1) is the LSB of the counter and D2 (T6) is the MSB of the counter, these bits are in the opposite order to normal.

SR. This bit is set to one during the reset phase and will generate a software reset if cleared to zero.

C. This is the watchdog activation bit that is hardware set to one; the user can't change the value of this bit (the watchdog is always active).

The register reset value is FEH (Bit 1-7 set to one, Bit 0 cleared).

6-BIT PWM D/A CONVERTERS AND 62.5 KHz OUTPUT FUNCTION

The D/A macrocell contains four PWM D/A outputs (32Khz repetition, DA0-DA3) with six bit resolution plus a 62.5KHz open-drain output pin (OUT1) specially suited for multistandard chroma processors driving. Both the D/A and OUT1 functions can be disabled by software allowing the DA0-DA3 and OUT1 pins to be used as general purpose open-drain output pins able to withstand signals with up to 12V amplitude.

6-Bit D/A Converters

Each D/A converter of ST63XX is composed by the following main blocks:

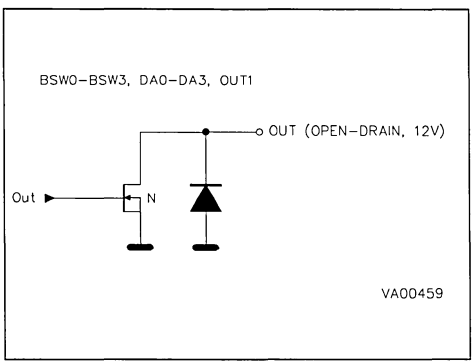
- pre-divider
- 6-bit counter
- data latches and compare circuits

The pre-divider uses the clock input frequency (8MHz) and its output clocks the 6-bit free-running counter. The data latched in the four registers (E0H, E1H, E2H and E3H) control the four D/A outputs (DA0,1,2 and 3). When all zeros are loaded the relevant output is an high logic level; all 1's correspond to a pulse with a 1/64 duty cycle and almost 100% zero level. A 7th bit (bit D6) is used to enable the relevant D/A output; when zero, the D/A is no longer enabled and it forces the output to zero. If the other six bits are all zero then the output is controlled only by the enable bit.

The repetition frequency is 32.5KHz and is related to the 8MHz clock frequency. All D/A outputs are open-drain with standard current drive capability and able to withstand up to 12V.

Only DAO is available on ST6340,42,44.

Figure 38. 6-BIT PWM D/A & 62.5KHz Output Configuration



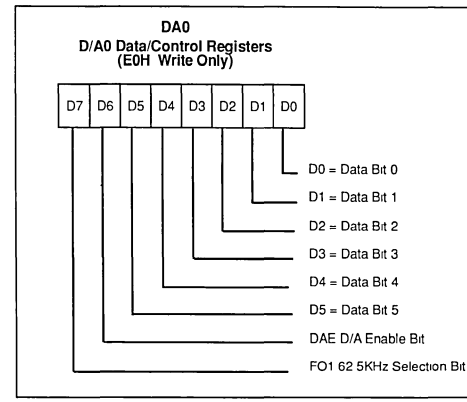
62.5 KHZ Output

This pin provides a 62.5 KHz signal with a 50% duty cycle; the output is enabled by a dedicated enable bit (E0H register bit 7). When the 62.5KHz frequency is disabled then the output is controlled by the OUT1 bit and the line can be used as general purpose open-drain output (E1H bit 7). The OUT1 output is open-drain with standard current drive capability and able to withstand signals with up to 12V amplitude. The pin can be used to drive the SGS-THOMSON TEA5640 chroma processor. Refer to the TEA5640 data sheet for more information on the use of this pin. Care must be taken to respect the frequency tolerances required by the TEA5640 by chosing a quartz with PPM variations within the limits required by the chroma processor.

D/A and OUT1 Data/Control Registers

This paragraph deals with the description of D/A and OUT1 data/control registers. Some bits of DA2 and DA3 data/control registers are used for external interrupt enable and A/D reference voltage shift, please refer to A/D and IR descriptions for additional information.

Figure 39. D/A0 Data/Enable Register



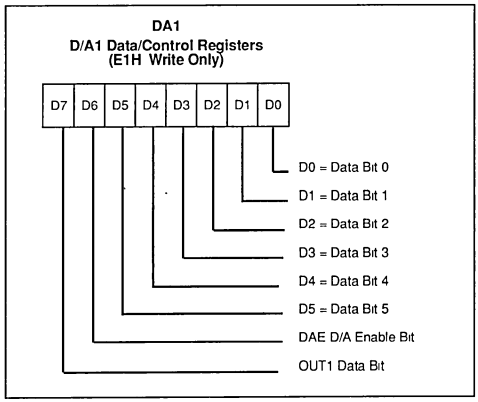
DA0-DA5. These are the 6 bits of the PWM digital to analog converter . Undefined after reset.

DAE. This is the D/A 0 enable bit. If zero, the output of the D/A is forced to zero; if one, the output of the D/A depends on bits DA0..DA5. Undefined after reset.

FO1. This is the 62.5KHz frequency output/ OUT1 selection bit. If one, the OUT1 pin will give a 62.5KHz frequency; if zero the OUT1 pin can be used as general purpose open-drain output and the value present on the pin depends on the value of OUT1 bit programmed in the DA1 data/control register. Undefined after reset.

6-BIT PWM D/A CONVERTERS AND 62.5 KHz OUTPUT FUNCTION (Continued)

Figure 40. D/A1 Data/Enable Register

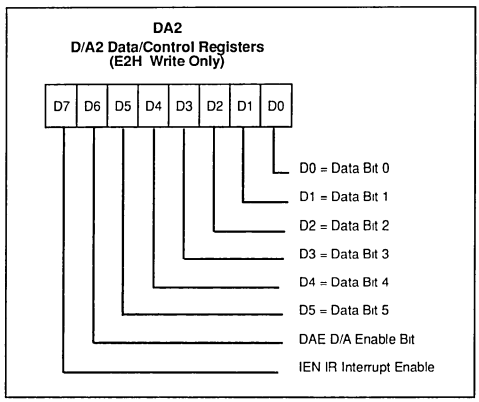


DA0-DA5. These are the 6 bits of the PWM digital to analog converter. Undefined after reset.

DAE. This is the D/A 1 enable bit. If zero, the output of the D/A is forced to zero; if one, the output of the D/A depends on bits DA0..DA5. Undefined after reset.

OUT1. This is the OUT1 data bit. The content of this bit is output on the OUT1 pin when the 62.5KHz frequency function is disabled (FO1 bit in DA0 register is cleared to zero). Undefined after reset.

Figure 41. D/A2 Data/Enable Register

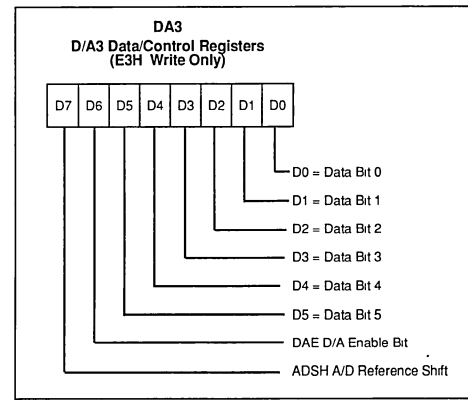


DA0-DA5. These are the 6 bits of the PWM digital to analog converter bits. Undefined after reset.

DAE. This is the D/A 2 enable bit. If zero, the output of the D/A is forced to zero; if one, the output of the D/A depends on bits DA0..DA5. Undefined after reset.

IEN. This is the external interrupt enable. If set to one, the interrupt coming from the external interrupt pin is enabled, if this bit is cleared the interrupt is disabled. Undefined after reset. This interrupt is associated to the NMI interrupt vector. This bit must be cleared to zero on ST6340 (IRIN pin not available). Refer to IR and interrupt descriptions for additional information.

Figure 42. D/A3 Data/Enable Register



DA0-DA5. These are the 6 bits of the PWM digital to analog converter. Undefined after reset.

DAE. This is the D/A 3 enable bit. If zero, the output of the D/A is forced to zero; if one, the output of the D/A depends on bits DA0..DA5. Undefined after reset.

ADSH. This is the analog to digital converter reference voltage shift bit. If set to one, the AFC block has reference voltages on 1V border. If set to zero, on 0.5V border. Undefined after reset. Refer to AFC for additional information.

AFC A/D INPUT, KEYBOARD INPUTS AND BANDSWITCH OUTPUTS

The AFC macrocell contains an A/D comparator with five levels at intervals of 1V from 1V to 5V. The levels can all be lowered by 0.5v to effectively double the resolution. This A/D can be used to perform the AFC function. In addition this cell offers also a keyboard input register of three bits used to perform a keyboard scan and 4 open-drain outputs (able to withstand signals up to 12V) that can be used to perform band switch function.

Figure 43. AFC, KBY Inputs Configuration Diagrams

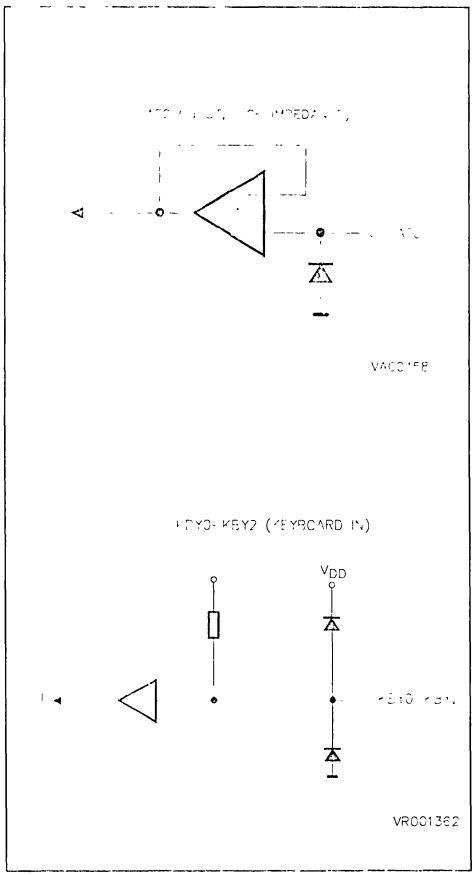
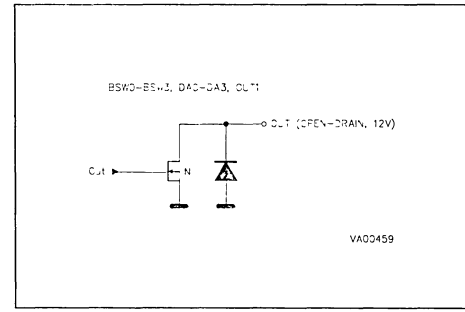


Figure 44. BSW, DA, OUT1 Output Configuration Diagram



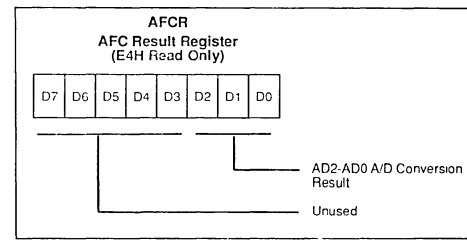
A/D Comparator

The A/D used to perform the AFC function (when high threshold is selected) has the following voltage levels: 1,2,3,4 and 5V. Bits 0-2 of AFC result register (E4H address) will provide the result in binary form (less than 1V is 000, greater than 5V is 101).

If the application requires a greater resolution, the sensitivity can be doubled by clearing to zero bit 7 of DA3 Data/Control register, address E3H (refer to D/A description for additional information). In this case all levels are shifted lower by 0.5V. If the two results are now added within a software routine then the A/D S-curve can be located within a resolution of 0.5V. The A/D input has high impedance able to withstand up to 13V signals (input level tolerances ± 200mv absolute and ± 100mv relative to 5V).

AFC, Keyboard Inputs and Bandswitch Outputs Data/Control Registers

Figure 45. AFC Result Register

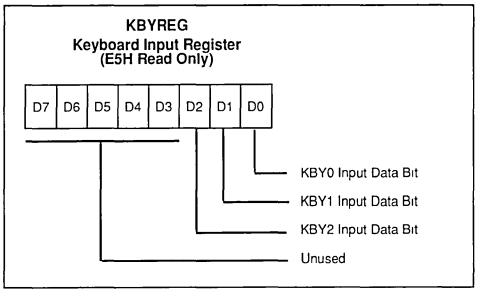


D7-D3. These bits are not used.

AD0-AD2. These bits store the real time conversion of the value present on the AFC input pin. No reset value.

AFC A/D INPUT, KEYBOARD INPUTS AND BANDSWITCH OUTPUTS (Continued)

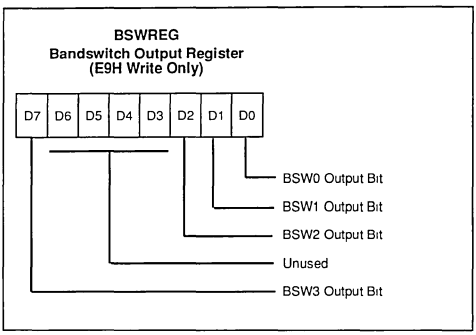
Figure 46. Keyboard Input Register



D7-D3. These bits are not used.

KBY0-KBY2. These bits store the logic level present at KBY0, KBY1 and KBY2 input pins. No reset value. This input pins have CMOS levels with on-chip pull-up resistor (100Kohm typical).

Figure 47. Bandswitch Output Register



D6-D3. These bits are not used.

BSW0-BSW2,BSW3. The writing into these bits will cause the corresponding BSW open-drain output line to switch to the programmed level. Undefined after reset.

INFRARED INPUT (IRIN)

The IRIN pin is directly connected to the NMI interrupt and acts as external interrupt pin (refer to interrupt description for additional information).

IRIN pin is not available on ST6340.

The enable/disable of this interrupt can be managed with the write only IRINTEN bit available in the D/A2 Data/Control register (Address E2H, bit D7). When this bit is set to one the interrupt is enabled otherwise it is disabled.

The IRIN pin is RISING EDGE sensitive.

Application Note

When the IR interrupt is enabled, then a rising edge on the IR pin will generate an interrupt; if the IR interrupt is disabled, no IR interrupts can be latched. Care should be taked because if the IR pin is high when the IR interrupt is enabled, an interrupt will also be generated; the following method to eliminate noise can also be used if the SW engineer wishes to enable/disable the IR interrupt.

If A Low-cost infra-red receiver is used, the customer may wish to test the IR signal by software after an interrupt in order to verify that there is a good pulse and not just noise. The IRIN pin cannot be read, so in this case it should be connected in parallel with another pin so the signal can be read. Furthermore the IRIN pin is sensitive to a rising edge interrupt; this means that the input to the pin should be low in the presence of no infra-red signal, but since most infra-red receiver modules give a high signal, the signal will need to be inverted with a transistor.

The IR interrupt must be disabled on ST6340 to prevent false interrupts as the IRIN pin is not available.

ON-SCREEN DISPLAY (OSD)

The ST634X OSD macrocell is a CMOS LSI character generator which enable display of characters and symbols on the TV screen. The character rounding function enhances the readability of the characters. The ST634X OSD receives horizontal and vertical synchronization signal and outputs screen information via R, G and blanking pins. The main characteristics of the macrocell are listed below:

- Number of display characters: 2 lines by 15 columns.
- Number of character types: 64 characters in one bank.
- Character size: Four character heights (18H, 36H 54H, 72H), two available per screen programmable by line.
- Character format: 6x9 dots with character rounding function.
- Character color: Up to four colors available programmable by word; refer to the specific pin configuration.
- Display position: 64 horizontal positions by 2/fos and 63 vertical positions by 4 H
- Word spacing: 64 positions programmable from 2/fosc to 128/fosc.
- Line spacing: 63 positions programmable from 4 to 252 H.
- Background: No background, square background or fringe background programmable by word.
- Background or fringe color: Can be enabled or disabled on a word by word basis.
  The color is selectable from any of the available colors (refer to pin configurations) on screen by basis.
- Display output: Character data output terminals (R,G) and a blank output terminal; refer to the specific pin configuration.
- Display on/off: Display data may be programmed on or off by word or entire screen. Entire screen may be blanked.

Special OSD Notes for Emulation and Piggyback

The ST634X devices feature two lines of OSD while the emulator and the piggyback devices always five lines of OSD. The OSD of the ST634X devices is in fact a direct subset of the emulator and piggyback OSD.

Special care must be taken to make sure that the user uses only the features of the ST634X devices. The registers must be loaded such that the correct two lines are used and such that only one background is used. The ST634X uses only the second and fourth lines of the emulator and piggyback OSD; the first, third and fifth lines are not available. Registers in these unused lines MUST BE LOADED WITH THE VALUE 3CH; i.e. no vertical space enable, background 1 selected. This also implies that BACKGROUND 1 MUST BE DEFINED AS TRANSPARENT.

Format Specification

The entire display can be turned on or off thru the use of global enable bit or the display may be selectively turned on or off by word. To turn off the entire display, the global enable bit (GE) should be zero. If the global enable is one, the display is controlled by the word enable bits (WE). The global enable bit is located in the global enable register and the word enable bit is located in the space character preceding the word.

Each line must begin with a format character which describes the format of that line and of the first word. This character is not displayed.

A space character defines the format of subsequent words. A space character is denoted by a one in bit 6 in the display RAM. If bit 6 of the display RAM is a zero, the other six bits define one of the 64 display characters.

The color, background and enable can be programmed by word. This information is encoded in the space character between words or in the format character at the beginning of each line. Five bits define the color and background of the following word, and determine whether it will be displayed or not.

Characters are stored in a 6 x 9 dot format. One dot is defined vertically as 2H (horizontal lines) and horizontally as 2/fosc if the smallest character size is enabled. There is no space between characters or lines if the vertical space enable (VSE) and

ON-SCREEN DISPLAY (Continued)

horizontal space enable (HSE) bits are both zero. This allows the use of special graphics characters.

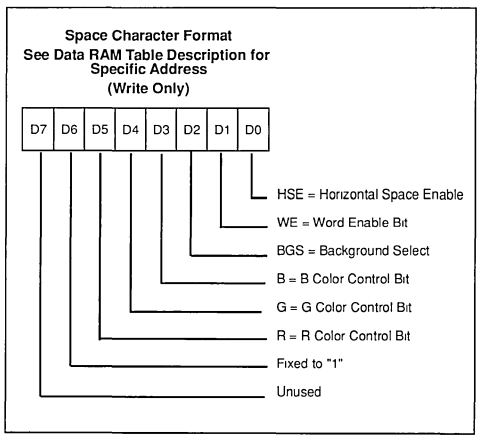
The normal alphanumeric character set is formatted to be 5 x 7 with on empty row at the top and one at the bottom and one empty column at the right. If VSE and HSE are both zero, then the spacing between alphanumeric characters is 1 dot and the spacing between lines of alphanumeric characters is 2H.

The character size is programmed by line thru the use of the size bit (S) in the format character and the global size bits (GS1 and GS2). The vertical spacing enable bit (VSE) located in the format character controls the spacing between lines. If this bit is set to one, the spacing between lines is defined by the vertical spacing register, otherwise the spacing between lines is 0.

The spacing between words is controlled by the horizontal space enable bit (HSE) located in the space character. If this bit is set to one, the spacing between words is defined by the horizontal spacing register, otherwise the space character width of 6 dots is the spacing between words.

The formats for the display character, space character and format character are described hereafter.

Figure 49. Space Character Register Explanation



D7. Not used.

D6. This pin is fixed to "1".

R, G, B. *Color.* The 3 color control bits define the color of the following word as shown in table 9. Refer to the specific pin configuration to see which colors are available.

Table 9. Space Character Register Colour Setting.

R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

BGS. *Background Select.* The background select bit selects the desired background for the following word. There are two possible backgrounds defined by the bits in the Background Control Register.

"0" - The background on the following word is enabled by BG0 and the color is set by R0, G0, and B0.

"1" - The background on the following word is enabled by BG1 and the color is set by R1, G1, and B1.

WE. *Word Enable.* The word enable bit defines whether or not the following word is displayed.

"0" - The word is not displayed.

"1" - If the global enable bit is one, then the word is displayed.

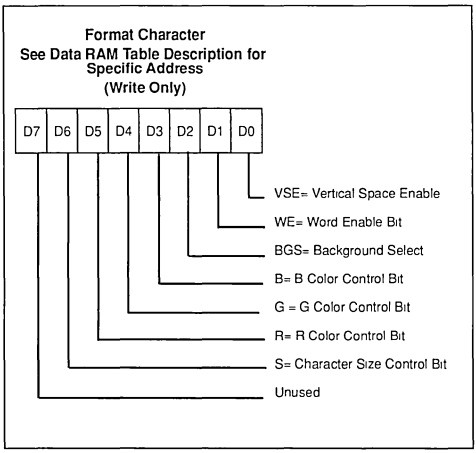
HSE. *Horizontal Space Enable.* The horizontal space enable bit determines the spacing between words. The space between characters is always 0. The alphanumeric character set is implemented in a 5 x 7 format with one empty column to the right and one empty row above and below so that the space between alphanumeric characters will be one dot.

"0" - The space between words is equal to the width of the space character, which is 6 dots.

"1" - The space between words is defined by the value in the horizontal space register plus the width of the space character.

ON-SCREEN DISPLAY (Continued)

Figure 50. Format Character Register Explanation



D7. This bit is not used

S. *Character Size.* The character size bit, along with the global size bits (GS2 and GS1) located in the horizontal space register, specify the character size for each line as defined in Table 11.

BGS. *Background Select.* The background select bit selects the desired background for the following word. There are two possible backgrounds defined by the bits in the Background Control Register.

"0" - The background on the following word is enabled by BG0 and the color is set by R0, G0, and B0.

"1" - The background on the following word is enabled by BG1 and the color is set by R1, G1, and B1.

WE. *Word Enable.* The word enable bit defines whether or not the following word is displayed.

"0" - The word is not displayed.

"1" - If the global enable bit is one, then the word is displayed.

R, G, B. *Color.* The 3 color control bits define the color of the following word as shown in Table 10. Refer to the specific pin configuration to see which colors are available.

VSE. *Vertical Space Enable.* The vertical space enable bit determines the spacing between lines.

"0" - The space between lines is equal to 0H. The alphanumeric character set is implemented in a 5 x 7 format with one empty column to the right and one empty row above and one below and stored in a 6 x 9 format.

"1" - The space between lines is defined by the value in the vertical space register.

Table 10. Format Character Register Colour Setting.

R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

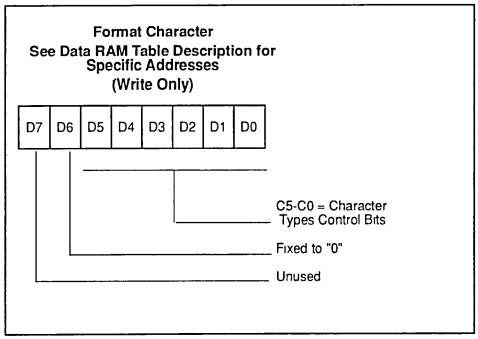
Table 11. Format Character Register Size Setting

GS2	GS1	S	Vertical Height	Horizontal lenght
0	0	0	18H	6 TDOT
0	0	1	36H	12 TDOT
0	1	0	18H	6 TDOT
0	1	1	54H	18 TDOT
1	0	0	36H	12 TDOT
1	0	1	54H	18 TDOT
1	1	0	36H	12 TDOT
1	1	1	72H	24 TDOT

TDOT= 2/fosc

ON-SCREEN DISPLAY (Continued)

Figure 51. Display Character Register Explanation



D7. This bit is not used.

D6. This bit is fixed to "0".

C5-C0. *Character type.* The 6 character type bits define one of the 64 available character types. These character types are shown on the following pages.

Character Types

The character set is user defined as ROM mask option.

Register and RAM Addressing

The OSD contains six registers and 80 RAM locations. The seven registers are the Vertical Start Address register, Horizontal Start Address register, Vertical Space register, Horizontal Space register, Background Control register and Global Enable register. The Global Enable register can be written at any time by the ST63 Core. The other five registers and the RAM can only be read or written to if the global enable is zero.

The six registers and the RAM are located on two pages of the paged memory of the ST63XX MCUs. Each page contains 64 memory locations. This paged memory is at memory locations 00H to 3FH in the ST63XX memory map. A page of memory is enabled by setting the desired page bit, located in the data RAM bank switching register, to a one. The page register is location E8H. A one in bit five selects page 5, located on the OSD and a one in bit 6 selects page 6 on the OSD. Table 12 shows the addresses of the OSD registers and RAM. Some bytes of the RAM must be set-up as described in the section "Special OSD Notes for Emulation and Piggybacks".

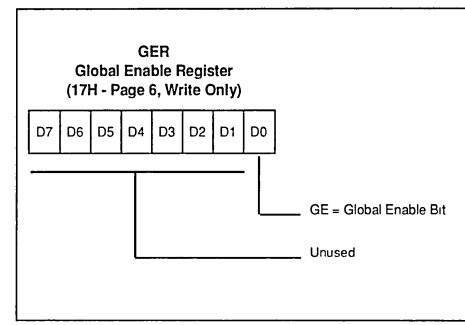
Table 12. OSD Control Registers and Data RAM Addressing

Page	Address	Register or RAM
5	00H - 3FH	RAM Locations 00H - 3FH
6	00H - 0FH	RAM Locations 00H - 0FH
6	10H	Vertical Start Register
6	11H	Horizontal Start Register
6	12H	Vertical Space Register
6	13H	Horizontal Space Register
6	14H	Background Control Register
6	17H	Global Enable Register

OSD Global Enable Register

This register contains the global enable bit (GE). It is the only register that can be written at any time regardless of the state of the GE bit. It is a write only register.

Figure 52. Global Enable Register



D7-D1. These bits are not used

GE. *Global Enable.* This bit allows the entire display to be turned off.

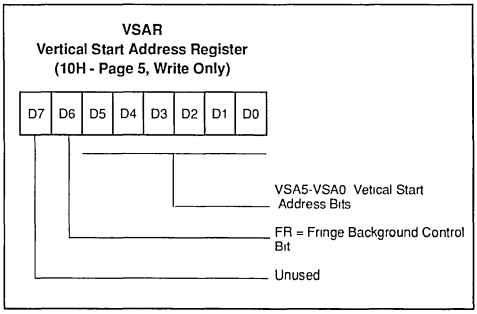
"0" - The entire display is disabled. The RAM and other registers of the OSD can be accessed by the Core.

"1" - Display of words is controlled by the word enable bits (WE) located in the format or space character.

The other registers and RAM cannot be accessed by the Core.

ON-SCREEN DISPLAY (Continued)

Figure 53. Vertical Start Address Register



D7. This bit is not used

FR. *Fringe Background.* This bit changes the background from a box background to a fringe background. The background is enabled by word as defined by either BK0 or BK1.

"0" - The background is defined to be a box which is 7 x 9 dots.

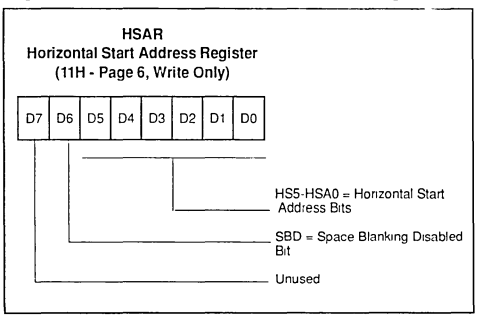
"1" - The background is defined to be a fringe.

VSA5-VSA0. *Vertical Start Address.* These bits determine the start position of the first line in the vertical direction. The 6 bits can specify 63 display start positions of interval 4H. The first start position will be the fourth line of the display. The vertical start address is defined VSA0 by the following formula.

Vertical Start Address = $4H(2^5(VSA5) + 2^4(VSA4) + 2^3(VSA3) + 2^2(VSA2) + 2^1(VSA1) + 2^0(VSA0))$

The case of all Vertical Start Address bits being zero is 111.

Figure 54. Horizontal Start Address Register



D7. This bit is not used.

SBD. *Space Blanking Disable.* This bit controls whether or not the background is displayed when outputting spaces. If two background colors are used on adjacent words, then the background should not be displayed on spaces in order to make a nice break between colors. If an even background around an area of text is desired, as in a menu, then the background should be displayed when outputting spaces.

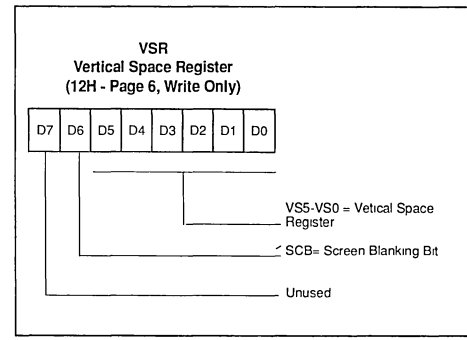
"0" - The background during spaces is controlled by the background enable bits (BK0 and BK1) located in the Background Control register.

"1" - The background is not displayed when outputting spaces.

HSA5, HSA0 - *Horizontal Start Address bits.* These bits determine the start position of the first character in the horizontal direction. The 6 bits can specify 64 display start positions of interval 2/fosc or 400ns. The first start position will be at 4.0µs because of the time needed to access RAM and ROM before the first character can be displayed. The horizontal start address is defined by the following formula.

Horizontal Start Address = $2/fosc(10.0 + 2^5(HSA5) + 2^4(HSA4) + 2^3(HSA3) + 2^2(HSA2) + 2^1(HSA1) + 2^0(HSA0))$

Figure 55. Vertical Space Register



D7. This bit is not used

SCB. *Screen Blanking.* This bit allows the entire screen to be blanked.

"0" - The blanking output signal (VBLK) is active only when displaying characters.

"1" - The blanking output signal (VBLK) is always active. Characters in the display RAM are still displayed.

When this bit is set to one, the screen is blanked also without setting the Global Enable bit to one (OSD disabled).

VS5 , VS0. *Vertical Space.* These bits determine the spacing between lines if the Vertical Space Enable bit (VSE) in the format character is one. If VSE is zero there will be no spaces between lines.

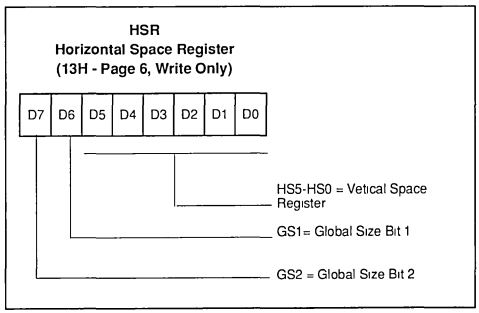
ON-SCREEN DISPLAY (Continued)

The Vertical Space bits can specify one of 63 spacing values from 4H to 252H. The space between lines is defined by the following formula.

Space between lines = $4H(2^5(VS5) + 2^4(VS4) + 2^3(VS3) + 2^2(VS2) + 2^1(VS1) + 2^0(VS0))$

The case of all Vertical Start Address bits being zero is ill.

Figure 56. Horizontal Space Register



GS2,GS1. *Global Size.* These bits along with the size bit (S) located in the Character format word specify the character size for each line as defined in table 13.

Table 13. Horizontal Space Register Size Setting.

GS2	GS1	S	Vertical Height	Horizontal Lenght
0	0	0	18H	6 TDOT
0	0	1	36H	12 TDOT
0	1	0	18H	6 TDOT
0	1	1	54H	18 TDOT
1	0	0	36H	12 TDOT
1	0	1	54H	18 TDOT
1	1	0	36H	12 TDOT
1	1	1	72H	24 TDOT

Note: TDOT= $2/f_{OSC}$

HS5, HS0 . *Horizontal Space* . These bits determine the spacing between words if the Horizontal Space Enable bit (HSE) located in the space character is a one. The space between words is then equal to the width of the space character plus the number of tdots specified by the Horizontal Space bits. The 6 bits can specify one of 64 spacing values ranging from 2/fosc to 128/fosc. The formula is shown below for the smallest size character(18H).

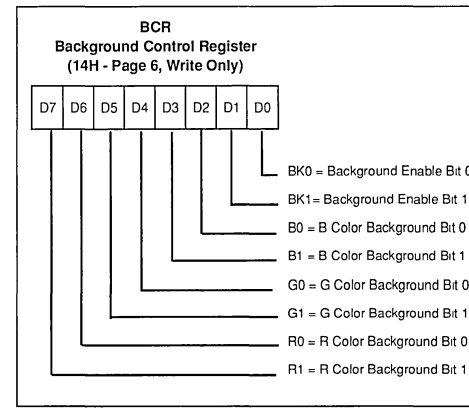
If larger size characters are being displayed the spacing between words will increase proportionately. Multiply the value below by 2, 3 or 4 for character sizes of 36H, 54H and 72H respectively.

Space between words (not including the space character)=$2/fosc((1+2^5(HS5)+2^4(HS4)+2^3(HS3)+2^2(HS2)+2^1(HS1)+2^0(HS0))$

Background Control Register

This register sets up two possible backgrounds. The background select bit (BGS) in the format or space character will determine which background is selected for the current word. The background control register must be set-up as described in the section "Special OSD Notes for Emulation and Piggybacks".

Figure 57. Background Control Registers



R1,R0,G1,G0,B1,B0. Background Color. These bits define the color of the specified background, either background 1 or background 0 as defined in Table 14.

Table 14. Background Register Colour Setting.

RX	GX	BX	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

ON-SCREEN DISPLAY (Continued)

BK1,BK0. *Background Enable.*These bits determine if the specified background is enabled or not.

"0" - The following word does not have a background.

"1" - There is a background around the following word.

OSD Data RAM

The contents of the data RAM can be accessed by the ST63XX MCUs only when the global enable bit (GE) in the Global Enable register is a zero.

The first character in every line is the format character. This character is not displayed. It defines the size of the characters in the line and contains the vertical space enable bit. This character also defines the color, background and display enable for the first word in the line. Subsequent characters are either spaces or one of the 64 available character types.

The space character defines the color, background, display enable and horizontal space enable for the following word. Since there are 5 display lines of 15 characters each, the display RAM must contain 5 lines x (15 characters + 1 format character) or 80 locations. The RAM size is 80 locations x 7 bits. The data RAM map is shown in Table 15.

Emulator Remarks

There are several differences between emulator and silicon. For noise reasons, the OSD oscillator pins are not available: the internal oscillator cannot be disabled and replaced by an external coil. Also refer to the section "Special OSD Notes for Emulation and Piggybacks".

Application Notes

1 - The OSD character generator is composed of a dual port video ram and some circuitry. It needs two input signals VSYNC and HSYNC to syncronize its dedicated oscillator to the TV picture. It generates 4 output signals, that can be used from the TV set to generate the characters on the screen. For istance, they can be used to feed the SCART plug, providing an adequate buffer to drive the low impedance (75 Ω) of the SCART inputs.

2 - The Core sees the OSD as a number of RAM locations (80) plus a certain number of control registers (6). These 86 locations are mapped in two pages of the dynamic data ram address range (0H..3FH).
In page 5 (load 20H in the register 0E8H), there are 64 bytes of RAM, the ones of the first 4 rows (16 bytes each row, 15 characters per row maximum, plus an hidden leading format character). In page 6 (load 40H in register 0E8H), the 16 bytes of the fith row (0..0FH), and the 6 control registers (10H..14H,17H).

Table 15. OSD RAM Map

Column				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A0				0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A3				0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A2				0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A1				0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A6	A5	A4	LINE																
0	0	0	1	FT															
0	0	1	2	FT															
0	1	0	3	FT															
0	1	1	4	FT															
1	0	0	5	FT															

AVAILABLE SCREEN SPACE

Notes: FT The format character required for each line. Characters in columns 1 thru 15 are displayed.

ON-SCREEN DISPLAY (Continued)

3 - The video RAM is a dual port ram. That means that it can be addressed either from the Core or from the OSD circuitry itself. To reduce the complexity of the circuitry, and thus its cost, some restrictions have been introduced in the use of the OSD.

a. The Core can Only write to any of the 86 locations (either video RAM or control registers).

b. The Core can Only write to any of the leading 85 locations when the OSD oscillator is OFF. Only the last location (control register 17H in page 6) can be addressed at any time. This is the Global Enable Register, which contains only the GE bit. If it is set, the OSD is on, if it is reset the OSD is off.

4 - The timing of the on/off switching of the OSD oscillator is the following:

a. GE bit is set. The OSD oscillator will start on the next VSYNC signal.

b. GE bit is reset. The OSD oscillator will be immediately switched off.

To avoid a bad visual impression, it is important that the GE bit is set before the end of the flyback time when charging character. This can be done inside the VSYNC interrupt routine. The following diagram can explain better:

When modifying the picture display (i.e.: a bar graph for an analog control), it is important that the switching on of the GE bit is done before the the end of the flyback time (D in Figure 67). If the GE bit is set after the end of the flyback time then the OSD will not start until the begining of the next frame. This results in one frame being lost and will result in a Flicker on the screen. One method to be sure to avoid the flicker is to wait for the VSYNC interrupt at the start of the flyback; once the VSYNC interrupt is detected, then the GE bit can be set to zero, the characters changed, and the the GE set to one. All this should occur before the end of the flyback time in order not to loose a frame. The correct edge of the interrupt must be chosen. The VSYNC pin may alternatively be sampled by software in order to know the status; this can be done by reading the pin PB2 (VSYNC).

6 - An OSD end of line Bar is present in the ST63PXX piggyback and ST63XX ROM devices when using the background mode. If this bar is present with software running in the piggybacks then it is also present on the ROM mask version. If the end of line bar is seen to be eliminated by software in the piggyback, then it is also be eliminated in the ROM mask version.

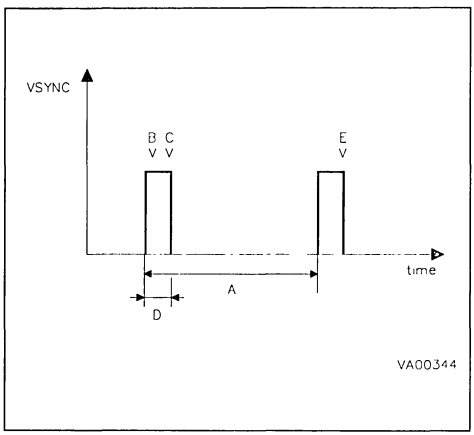
The bar appears at the end of the line in the background mode when the last character is a space character and the first format character is defined with S=0 (size 0). The bar is the color of the background defined by the space character. To eliminate bar:

a. If two backgrounds are used then the bar should be moved off the screen by using large word spaces instead of character spaces. If there are not enough spaces before the end of the line, then the location of the valid characters should be moved so they appear at the end of the line (and hence no bar); positioning can be compensated using the horizontal start register.

b. If only one background is used, then the other background should be transparent in order to eliminate the bar.

7 - The OSD oscillator external network should consist of a capacitor on each of the OSD oscillator pins to ground together with an inductance between the the pin. The user should select the two capacitors to be the same value (15pF to 25pF each is recommended). The inductance is chosen to give the desired OSD oscillator frequency for the application (normally 56µH).

Figure 58. OSD Oscillator ON/OFF Timing



Notes:
A Picture time 20 mS in PAL/SECAM
B VSYNC interrupt, if enabled.
C. Starting of OSD oscillator, if GE = 1
D. Flyback time.

14-BIT VOLTAGE SYNTHESIS TUNING PERIPHERAL (Not available on ST6342)

The ST634X on-chip voltage synthesis tuning peripheral has been integrated to allow the generation of tuning reference voltage in low/mid end TV set applications. The peripheral is composed of a 14-bit counter that allows the conversion of the digital content in a tuning voltage, available at the VS output pin, by using PWM and BRM techniques. The 14-bit counter gives 16384 steps which allows a resolution of approximately 2mV over a tuning voltage of 32V ; this corresponds to a tuning resolution of about 40KHz per step in UHF band (the actual value will depend on the characteristics of the tuner).

The tuning word consists of a 14-bit word contained in the registers VSDATA1 (location 0EDH) and VSDATA2 (location 0EEH). Course tuning (PWM) is performed using the seven MSBit, while the fine tuning (BRM) is performed using the data in the seven LSBIT. With all zeros loaded the output is zero ; as the tuning voltage increseses from all zeros, the number of pulses in one period increses to 128 with all pulses being the same width. For values larger than 18, the PWM takes over and the number of pulses in one period remains constant at 128, but the width changes. At the other end of the scale, when almost all ones are loaded, the pulses will start to link together and the number of pulses will decrease. When all ones are loaded, the output will be almost 100% high but will have a low pulse (1/16384 of the high pulse).

Output Details

Inside the on-chip Voltage Synthesis cell are included the register latches, a reference counter, PWM and BRM control circuitry ; the structure is one used in many devices currenlty in production from SGS-THOMSON (M106, M193, M293, M490/91/94). In the ST635X the clock for the 14-bit reference counter is 2MHz derived from the 8MHz system clock. From the circuit point of view, the seven most significant bits controls the course tuning, while the seven least significant bits the fine tuning. From the application and software point of view, the 14 bits can be considered as one binary number.

As already mentioned the course tuning consists of a PWM signal with 128 steps ; we can consider the fine tuning to cover 128 course tuning cycles. The addition of pulses is described in the following Table 16.

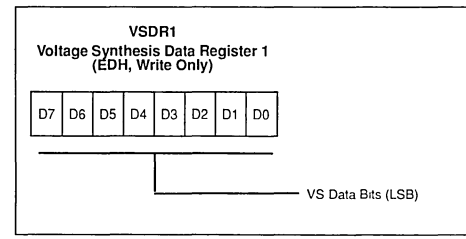
Table 16. Fine Tuning Pulse Addition

FIne Tuning (7 LSB)	N° of Pulses added at the following cycles (0...127)
0000001	64
0000010	32, 96
0000100	16, 48, 80, 112
0001000	8, 24, ...104, 120
0010000	4, 12, ...116, 124
0100000	2, 6, ...122, 126
1000000	1, 3, ...125, 127

The VS output pin has a standard drive push-pull output configuration.

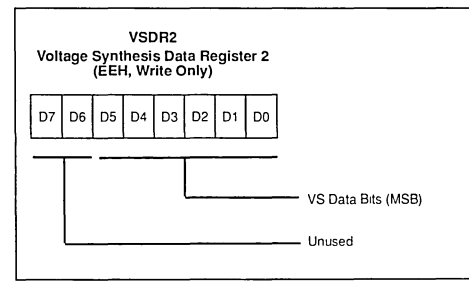
VS Tuning Cell Registers

Figure 59. VS Data Register 1



D7-D0. These are the 8 least significant VS data bits. Bit 0 is the LSB. This register is undefined on reset.

Figure 60. VS Data Register 2



D7-D6. These bits are not used.

D5-D0. These are the 6 most significant VS data bits. Bit 5 is the MSB. This register is undefined on reset.

SOFTWARE DESCRIPTION

The ST63XX software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short to provide byte efficient programming capability. The ST63XX Core has the ability to set or clear any register or RAM location bit of the Data space with a single instruction. Furthermore, the program may branch to a selected address depending on the status of any bit of the Data space. The carry bit is stored with the value of the bit when the SET or RES instruction is processed.

Addressing Modes

The ST63XX Core has nine addressing modes which are described in the following paragraphs. The ST63XX Core uses three different address spaces: Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, the data for immediate mode instructions, and in this space is physically allocated the data ROM which is addressed as data space. Data space contains the Accumulator, the X,Y,V and W registers, the Core control registers, peripheral and Input/Output registers, the RAM locations and the window to address the Data ROM (physically located into the program memory) locations (for storage of tables and constants). Stack space contains six 12-bit RAM bytes used to stack the return addresses for subroutines and interrupts.

Immediate. In the immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In the direct addressing mode, the address of the byte that is processed by the instruction is stored in the location that follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data space memory with a single two-byte instruction.

Short Direct. The Core can address the four RAM registers X,Y,V,W (locations 80H, 81H, 82H, 83H) in the short-direct addressing mode . In this case, the instruction is only one byte long and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of the direct addressing mode. (Note : 80H and 81H are also indirect registers).

Extended. In the extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four less significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) that use the extended addressing mode are able to branch any address of the directly addressable Program space. An extended addressing mode instruction is two-byte long.

Program Counter Relative. The relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to + 16 locations around the address of the relative instruction. If the condition is not true, the instruction that follows the relative instruction is executed. The relative addressing mode instruction is one-byte long. The opcode is obtained by adding the three most significant bits that characterize the kind of test, one bit that determines whether the branch is a toward (when it is 0) or backward (when it is 1) branch and the four less significant bits that give the span of the branch (0H to FH) that must be added or subtracted to the address of the relative instruction to obtain the address of the branch.

Bit Direct. In the bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 directly addressable locations of Data space memory can be set or cleared.

Bit Test & Branch. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit test and branch instruction is three-byte long. The bit identification and the tested condition are included in the opcode byte. The address of the byte to be tested follows immediately the opcode in the Program space. The third byte is the jump displacement, which is in the range from -126 to + 129. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In the indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed by the content of one of the indirect registers, X or Y (80H,81H). The indirect register is selected by the bit 4 of the opcode. A register indirect instruction is one byte long.

Inherent. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

SOFTWARE DESCRIPTION (Continued)

Instruction Set

The ST63XX Core has a set of 40 basic instructions. When these instructions are combined with nine addressing modes, 244 usable opcodes can be obtained. They can be divided into six different types : load/store, arithmetic/logic, conditional branch, control instructions, jump/call, bit manipulation. The following paragraphs describe the different types. All the instructions within a given type are presented in individual tables.

Load & Store. These instructions use one,two or three bytes in relation with the addressing mode. One operand is the Accumulator for LOAD and the other operand is obtained from data memory using one of the addressing modes. For LOAD Immediate one operand can be any of the 256 data space bytes while the other is always an immediate data. Refer to Table 17.

Table 17. Load & Store instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
LD A, X	Short Direct	1	4	Δ	*
LD A, Y	Short Direct	1	4	Δ	*
LD A, V	Short Direct	1	4	Δ	*
LD A, W	Short Direct	1	4	Δ	*
LD X, A	Short Direct	1	4	Δ	*
LD Y, A	Short Direct	1	4	Δ	*
LD V, A	Short Direct	1	4	Δ	*
LD W, A	Short Direct	1	4	Δ	*
LD A, rr	Direct	2	4	Δ	*
LD rr, A	Direct	2	4	Δ	*
LD A, (X)	Indirect	1	4	Δ	*
LD A, (Y)	Indirect	1	4	Δ	*
LD (X), A	Indirect	1	4	Δ	*
LD (Y), A	Indirect	1	4	Δ	*
LDI A, #N	Immediate	2	4	Δ	*
LDI rr, #N	Immediate	3	4	*	*

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register
Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Arithmetic and Logic. These instructions are used to perform the arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while the other can be either a data space memory content or an immediate value in relation with the addressing mode. In CLR,DEC,INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator. Refer to Table 18.

Table 18. Arithmetic & Logic instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	*
AND A, (Y)	Indirect	1	4	Δ	*
AND A, rr	Direct	2	4	Δ	*
ANDI A, #N	Immediate	2	4	Δ	*
CLR A	Short Direct	2	4	Δ	Δ
CLR rr	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register

Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Conditional Branch. The branch instructions achieves a branch in the program when the selected condition is met. Refer to Table 19.

Bit Manipulation Instructions. These instructions can handle (set or reset) any bit in data space memory. Refer to Table 20.

Control Instructions. The control instructions control the MCU operations during program execution. Refer to Table 21.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutines call inside the whole program space. Refer to Table 22.

Table 19. Conditional Branch instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b. 3-bit address
e. 5 bit signed displacement in the range -15 to +16
ee 8 bit signed displacement in the range -126 to +129
rr. Data space register
Δ. Affeed
*. Not Affected

Table 20. Bit Manipulation instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes:
b. 3-bit address;
rr. Data space register;
*. Not Affected

Table 21. Control instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:
1. This instruction is deactivated on ST639X (HW watchdog and a WAIT is automatically executed instead of a STOP.
Δ. Affected
*. Not Affected

Table 22. Jump & Call instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes:
abc. 12-bit address;
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Opcode Map Summary. The following table contains an opcode map for the instructions used on the MCU.

Table 23. Opcode Map

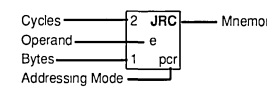
Low / Hi	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Low / Hi
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 pcr	4 LD a,(y) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 pcr	4 LD a,rr 2 dir	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b d	2 JRZ e 1 pcr	4 COM a 1 inh	2 JRC e 1 pcr	4 CP a,(y) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b d	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 pcr	4 CP a,rr 2 dir	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 ADD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 pcr	4 ADD a,(y) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 pcr	4 ADD a,rr 2 dir	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 INC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 pcr	4 INC (y) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 pcr	4 INC rr 2 dir	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD (x),a 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b d	2 JRZ e 1 pcr	#	2 JRC e 1 pcr	4 LD (y),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 pcr	4 LD rr,a 2 dir	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 AND a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b d	2 JRZ e 1 pcr	4 RLC a 1 inh	2 JRC e 1 pcr	4 AND a,(y) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 pcr	4 AND a,rr 2 dir	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 SUB a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 pcr	4 SUB a,(y) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 pcr	4 SUB a,rr 2 dir	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 DEC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 pcr	4 DEC (y) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 pcr	4 DEC rr 2 dir	F 1111

Abbreviations for Addressing Modes.

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend.

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement



ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature. Tj, in Celsius can be obtained form.:

$$Tj = TA + PD \times RthJA$$

Where: TA = Ambient Temperature,
RthJA = Package thermal resistance (junction-to ambient),

PD = Pint + Pport,

Pint = $I_{DD} \times V_{DD}$ (chip internal power),

Pport = Port power dissipation (determined by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
V_I	Input Voltage (AFC IN)	V_{SS} – 0.3 to +13	V
V_I	Input Voltage (Other Inputs)	VSS – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage (Port A, DA0-3, BSW0-3, OUT1)	V_{SS} – 0.3 to + 13	V
V_O	Output Voltage (Other Inputs)	VSS – 0.3 to V_{DD} +0.3	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS},	± 10	mA
IV_{SS}	Total Current out of V_{SS} (sink)	150	mA
T_j	Junction Temperature	150	°C
T_{STG}	Storage Temperature	– 60 to 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these conditions is not implied Exposure to maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP40 PDIP28			40 55	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature		0		70	°C
V_{DD}	Operating Supply Voltage		4.5		5.5	V
f_{OSC}	Oscillator Frequency RUN & WAIT Modes			8.0	8.1	MHz
f_{OSDOSC}	On-Screen Display Oscillator Frequency				8.0	MHz

EEPROM INFORMATION

The ST63XX EEPROM macrocell and the single poly EEPROM process have been specially developed to achieve 1.000.000 Write/Erase cycles and a 10 years data retention.

DC ELECTRICAL CHARACTERISTICS

(T_A= 0 to + 70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	All I/O Pins, KBY0-2			0.2x V_{DD}	V
V_{IH}	Input High Level Voltalge	All I/O Pins, KBY0-2	0.8x V_{DD}			V
V_{HYS}	Hysteresis Voltage(1)	All I/O Pins, KBY0-2 V_{DD} = 5V		1.0		V
V_{OL}	Low Level Output Voltage	Port A/B/C, DA0-3 BSW0-3, OUT1, VS, OSD Outputs V_{DD} = 4.5V I_{OL} = 1.6mA I_{OL} = 5.0mA			 0.4 1.0	 V V
V_{OL}	Low Level Output Voltage	OSDOSCOUT, OSCOUT, V_{DD} = 4.5V I_{OL}= -0.1mA			0.4	V
V_{OH}	High Level Output Voltage	Port B/C (2), VS V_{DD} = 4.5V I_{OH} = – 1.6mA	4.1			V
V_{OH}	High Level Output Voltage	OSDOSCOUT, OSCOUT, V_{DD} = 4.5V I_{OL}= – 0.1mA	4.1			V
I_{PU}	Input Pull Up Current Input Mode with Pull-up	Port A/B/C, KBY0-2 V_{IN}= V_{SS}	– 100	– 50	– 25	µA
I_{IL} I_{IH}	Input Leakage Current	OSCIN V_{IN}= V_{SS} V_{IN}= V_{DD}	– 10 0.1	– 1 1	– 0.1 10	µA
I_{IL} I_{IH}	Input Leakage Current	All I/O Input Mode no Pull-up OSDOSCIN V_{IN}= V_{DD} or V_{SS}	– 10		10	µA
I_{IL} I_{IH}	Input Leakage Current	Reset Pin with Pull-up V_{IN}= V_{SS}	– 50	– 30	– 10	µA
I_{IL} I_{IH}	Input Leakage Current	AFC Pin V_{IH}= V_{DD} V_{IL}= V_{SS} V_{IH}= 12.0V	– 1		1 40	µA
I_{OH}	Output Leakage Current	DA0-3, BSW0-3 OUT1, OSDOUT V_{OH} = V_{DD}			10	µA
I_{OH}	Output Leakage Current High Voltage	DA0-3, BSW0-3 OUT1 V_{OH} = 12V			40	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{DD}	Supply Current RUN Mode	f_{OSC}= 8MHz, ILoad= 0mA V_{DD}= 6.0V		6	16	mA
I_{DD}	Supply Current WAIT Mode	f_{OSC}= 8MHz, ILoad= 0mA V_{DD}= 6V		3	10	mA
V_{ON}	Reset Trigger Level ON	RESET Pin			0.3x V_{DD}	V
V_{OFF}	Reset Trigger Level OFF	RESET Pin	0.8x V_{DD}			V
V_{TA}	Input Level Absolute Tolerance	A/D AFC Pin V_{DD} = 5V			±200	mV
V_{TR}	Input Level Relative Tolerance (1)	A/D AFC Pin Relative to other levels V_{DD} = 5V			±100	mV

Notes:
1 Not 100% Tested
2. push-pull option only

AC ELECTRICAL CHARACTERISTICS

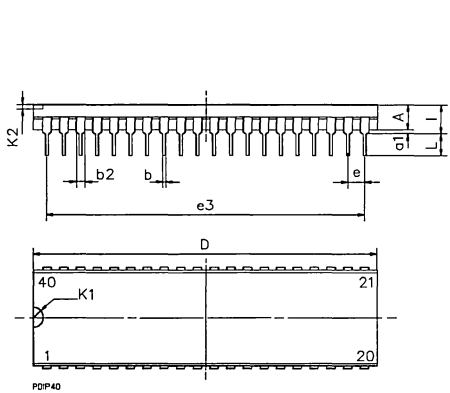
(T_A= 0 to + 70°C, f_{OSC} = 8MHz, V_{DD} = 4.5V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
tWRES	Minimum Pulse Width	RESET Pin	125			ns
t_{OHL}	High to Low Transition Time	Port A, B, C, V_{DD} = 5V, CL = 100pF		20		ns
t_{OHL}	Low to HighTransition Time (push-pull only)	Port B, C,		20		ns
f_{DA}	D/A Converter Repetition Frequency(1)			31.25		KHz
f_{OUT1}	62.5KHz Output(1)			62.50		KHz
tWEE	EEPROM Write Time	T_A = 25 °C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycles	Q_A LOT Acceptance Criteria	300.000	> 1 million		cycles
Retention	EEPROM Data Retention (3)	T_A = 25°C	10			years
C_{IN}	Input Capacitance (2)	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance (2)	All outputs Pins			10	pF
COSCIN, COSCOUT	Oscillator Pins Internal Capacitance (2)			5		pF
COSDIN, COSDOUT	OSD Oscillator External Capacitance	Recommended	15		25	pF

Notes:
1. A clock other than 8 MHz will affect the frequency response of those peripherals (D/A, 62 5KHz and SPI) whose clock is derived from the system clock.

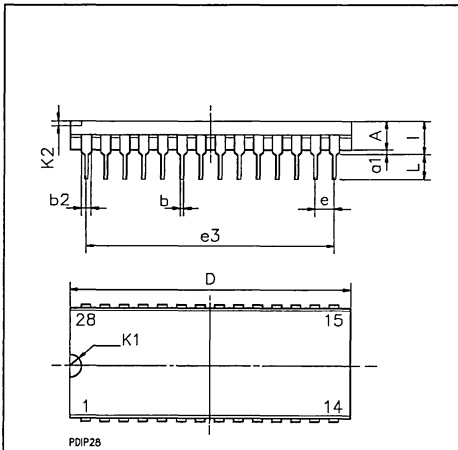
PACKAGE MECHANICAL DATA

Figure 61. 40-Pin Dual in Line Plastic



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0.63			0.025	
b		0 45			0.018	
b1	0.23		0 31	0.009		0.012
b2		1.27			0.050	
C	–	–	–	–	–	–
D			52.58			2.070
E	15.20		16 68	0.598		0.656
e		2.54			0.100	
e3		48 26			1.900	
e4	–	–	–	–	–	–
F			14.10			0.555
I		4 45			0.175	
L		3.30			0.129	

Figure 62. 28-Pin Dual in Line Plastic



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1		0 63			0.025	
b		0.45			0 018	
b1	0.23		0 31	0.009		0.012
b2		1.27			0 050	
C	–	–	–	–	–	–
D			37.34			1.470
E	15.20		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
e4	–	–	–	–	–	–
F			14.10			0.555
I		4 45			0.175	
L		3.30			0.130	

ORDERING INFORMATION

The following chapter deals with the procedure for transfer the Program/Data ROM codes to SGS-THOMSON.

Communication of the ROM Codes. To communicate the contents of Program /Data ROM memories to SGS-THOMSON, the customer has to send:

- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the PROGRAM Memory
- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the ODD and EVEN ODD OSD Characters
- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the EEPROM initial content (this file is optional)
- a filled Option List form as described in the OPTION LIST paragraph.

The program ROM should respect the ROM Memory Map as in Table 24.

The ROM code must be generated with ST6 assembler. Before programming the EPROM, the buffer of the EPROM programmer must be filled with FFH. For shipment to SGS-THOMSON the EPROMs should be placed in a consecutive IC carrier and packaging carefully.

Table 24. ROM Memory Map

ROM Page	Device Address	EPROM Address (1)	Description
Page 0	0000H-007FH 0080H-07FFH	0000H-007FH 0080H-07FFH	Reserved User ROM
Page 1 "STATIC"	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	User ROM Reserved Interrupt Vectors Reserved NMI Vector Reset Vector

Note: 1. EPROM addresses are related to the use of ST63P4X piggyback emulation devices.

ORDERING INFORMATION (Continued)

Customer EEPROM Initial Contents: Format

a. The content should be written into an INTEL INTELLEC format file.

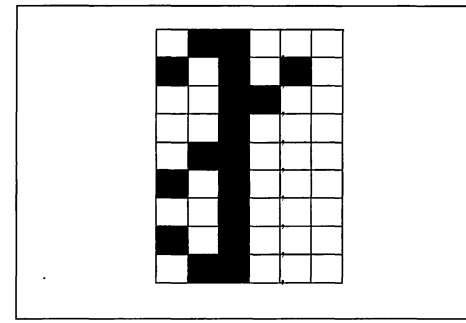
b. The starting address in 000h and the end in 7Fh.

c. Undefined or don't care bytes should have the content FFH.

OSD Test Character. In order to allow the testing of the on-chip OSD macrocell the following character must be provided at the fixed 3FH (63).

Listing Generation & Verification. When SGS-THOMSON receives the Codes, they are compared and a computer listing is generated from them. This listing refers extractly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed list constitutes a part of the contractual agreement for the creation of the customer mask. SGS-THOMSON sales organization will provide detailed information on contractual points.

Figure 63. OSD Test Character



Ordering Information Table

Sales Type	ROM/EEPROM Size	Temperature Range	Package
ST6340B1/XX	4K/48 Bytes	0 to + 70 ° C	PDIP28
ST6342B1/XX	4K/48 Bytes	0 to + 70 ° C	PDIP28
ST6344B1/XX	4K/48 Bytes	0 to + 70 ° C	PDIP28
ST6346B1/XX	4K/48 Bytes	0 to + 70 ° C	PDIP40

Note: "XX" Is the ROM code identifier that is allocated by SGS-THOMSON after receipt of all required options and the related ROM file.

ST634X MICROCONTROLLER OPTION LIST

Customer: . . . . . .

Address: . . . . . .

Contact: . . . . . .

Phone No: . . . . . .

Reference: . . . . . .

Device [ ] (d) Package [ ] (p) Temperature Range [ ] (t)

For marking one line with 10 characters maximum is possible

Special Marking [ ] (y/n) Line1 " _ _ _ _ _ _ _ _ _ _ " (N)

Notes:

(d) 1= ST6340, 2 = ST6342, 3 = ST6344, 4 = ST6346

(p) B= Dual in Line Plastic

(t) 1= 0 to 70°C

(N) Letters, digits, ' . ', ' - ', ' / ' and spaces only

Marking: the default marking is equivalent to the sales type only (part number).

OSD POLARITY OPTIONS (Put a cross on selected item) :

	POSITIVE	NEGATIVE
VSYNC,HSYNC	[ ]	[ ]
R,G	[ ]	[ ]
BLANK	[ ]	[ ]

CHECK LIST:

	YES	NO
ROM CODE	[ ]	[ ]
OSD Code: ODD & EVEN	[ ]	[ ]
EEPROM Code (if Desired)	[ ]	[ ]

Signature .....

Date .....

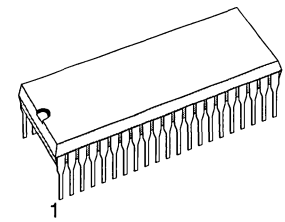
SGS-THOMSON MICROELECTRONICS

ST6385,6386 ST6387,6388

8 BIT HCMOS MCUs FOR TV VOLTAGE SYNTHESIS WITH OSD

ADVANCE DATA

- 8-bit Architecture
- HCMOS Technology
- 8MHz Clock
- User Program ROM: 20140 bytes
- Reserved Test ROM: 336 bytes
- Data ROM: User selectable size
- Data RAM: 256 bytes
- Data EEPROM: 384 bytes
- 42-Pin Shrink Dual in Line Plastic Package
- Up to 22 software programmable general purpose Inputs/Outputs, including 2 direct LED driving Outputs
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I^2C BUS and standard serial protocols
- Up to Six 6-Bit PWM D/A Converters
- 62.5KHz Output Pin (ST6386,88 Only)
- AFC A/D converter with 0.5V resolution
- Five interrupt vectors (IRIN/NMI, Timer 1 & 2, VSYNC, PWR INT.)
- 14 bit counter for voltage synthesis tuning
- On-chip clock oscillator
- 5 Lines by 15 Characters On-Screen Display Generator with 128 Characters
- Byte efficient instruction set
- Bit test and jump instructions
- Wait and Bit Manipulation instructions
- True LIFO 6-level stack
- All ROM types are supported by pin-to-pin piggyback versions.
- The development tool of the ST638X microcontrollers consists of the ST638X-EMU emulation and development system to be connected via a standard RS232 serial line to an MS-DOS Personal Computer.



PSDIP42

(Ordering Information at the end of the datasheet)

DEVICE SUMMARY

DEVICE	D/A Converter	62.5 KHz PIN	EEPROM (Bytes)
ST6385	4	NO	384
ST6386	4	YES	384
ST6387	6	NO	384
ST6388	6	YES	384

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 1. ST6385 Pin Configuration

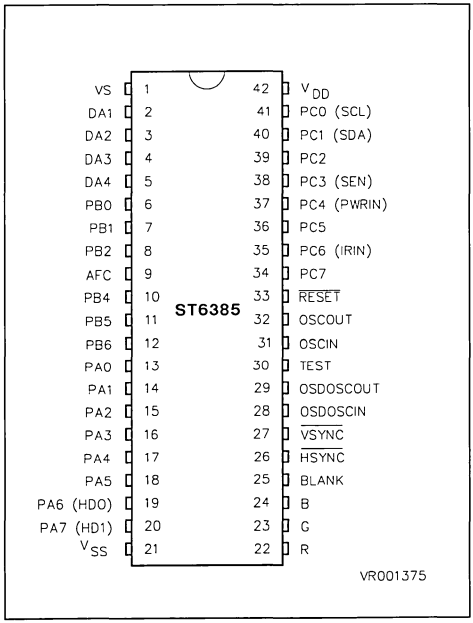
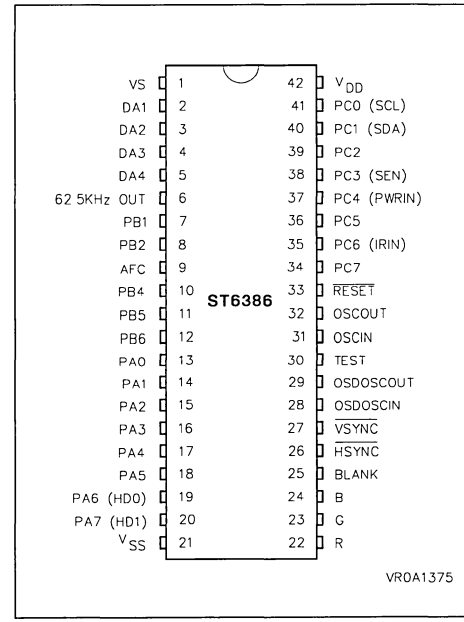


Figure 2. ST6386 Pin Configuration



Figre 3. ST6387 Pin Configuration

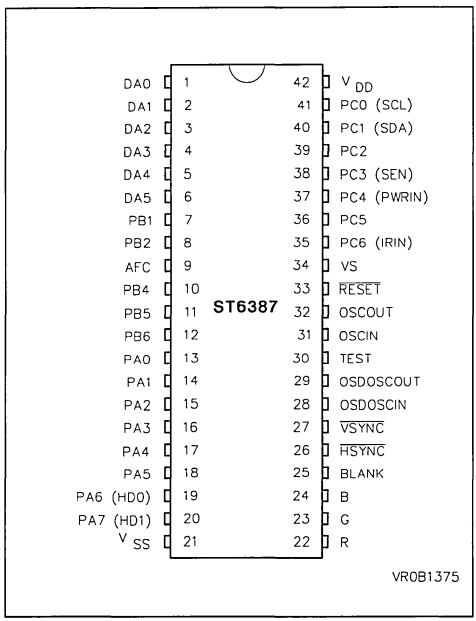
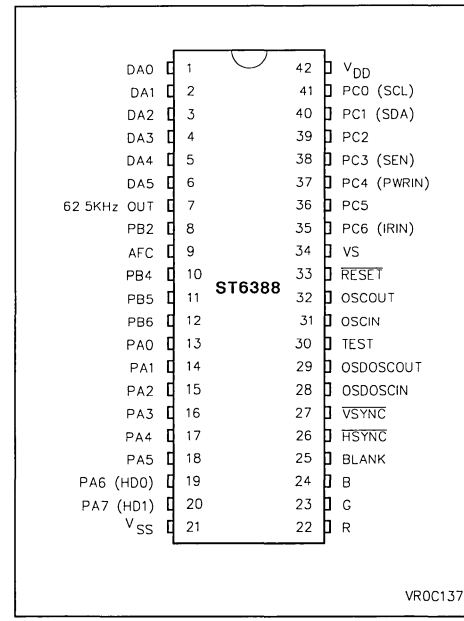


Figure 4. ST6388 Pin Configuration



GENERAL DESCRIPTION

The ST6385,86,87,88 microcontrollers are members of the 8-bit HCMOS ST638X family, a series of devices specially oriented to TV applications. Different pin-out and peripheral configurations are available to give the maximum application and cost flexibility. All ST638X members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility and short design time. Many of these macrocells are specially dedicated to TV applications. The macrocells of the ST638X family are : two Timer peripherals each including an 8-bit counter with a 7-bit software programmable prescaler (Timer), a digital hardware activated watchdog function (DHWD), a 14-bit voltage synthesis tuning pripheral, a serial peripheral interface (SPI), up to six 6-bit PWM D/A converters, an AFC A/D converter with 0.5V resolution, an on-screen display (OSD) with 15 characters per line, 128 characters (in two banks each of 64 characters). In addition the following memory resources are available: program ROM (20K), data RAM (256 bytes), EEPROM (384 bytes). Refer to pin configurations figures and to ST638X device summary (Table 1) for the definition of ST638X family members and a summary of differences among the different types.

Figure 5. ST6385,86,87,88 Block Diagram

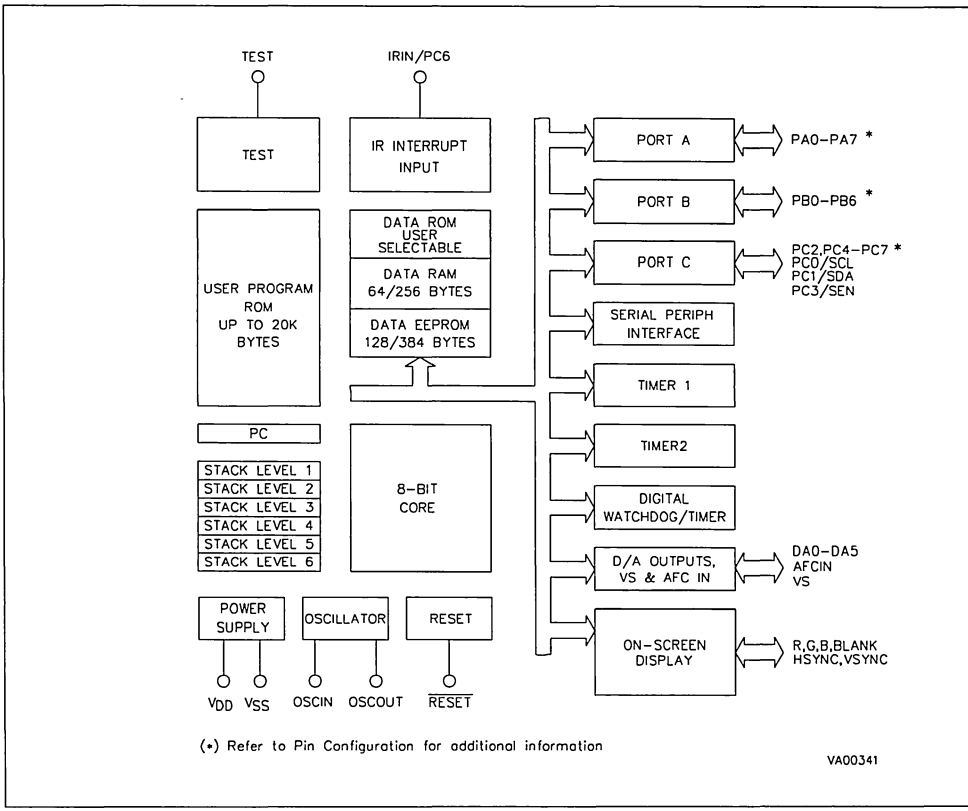


Table 1. ST638X Device Summary

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	AFC	VS	D/A	LOW PWR IN RESET	PWR IN PIN	COLOR PINS	SPI CLOCK FREQ. (KHz)	62.5KHz PIN	EMUL. DEVICE
ST6385	20K	256	384	YES	YES	4	YES	YES	3	62.5	NO	ST63P85
ST6386	20K	256	384	YES	YES	4	YES	YES	3	62.5	YES	ST63P86
ST6387	20K	256	384	YES	YES	6	YES	YES	3	62.5	NO	ST63P87
ST6388	20K	256	384	YES	YES	6	YES	YES	3	62.5	YES	ST63P88

Note: 1. Low power in RESET function disables the oscillator when RESET pin is active (LOW).

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN, OSCOUT. These pins are internally connected to the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The OSCIN pin is the input pin, the OSCOUT pin is the output pin. Refer to ON-CHIP CLOCK OSCILLATOR description for additional information.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to start the microcontroller to the beginning of its program. Additionally the quartz oscillator will be disabled when the $\overline{\text{RESET}}$ pin is low to reduce power consumption during reset phase. Refer to RESET description for additional information.

TEST. The TEST (mode select) pin is used to place the MCU into special operating mode. If TEST is held at V_{SS} the MCU enters the normal operating mode. If TEST is held at V_{DD} when $\overline{\text{RESET}}$ is active the test operating mode is automatically selected (the user should connect this pin to V_{SS} for normal operation). Refer to TEST mode description for additional information.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input with or without pull-up resistor or as an output under software control of the data direction register. Pins PA4 to PA7 are configured as open-drain outputs (12V drive). On PA4-PA7 pins the input pull-up option is not available while PA6 and PA7 have additional current driving capability (25mA, 1V). PA0 to PA3 pins are configured as push-pull. Refer to I/O PORT description for additional information.

PB0-PB2, PB4-PB6. These 6 lines are organized as one I/O port (B). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register. Refer to I/O PORT description and Pin configurations (Figures 1 to 4) for additional information.

PC0-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register. Pins PC0 to PC3 are configured as open-drain (5V drive) in output mode while PC4 to PC7 are open-drain with 12V drive and the input pull-up options does not exist on these four pins. PC0, PC1 and PC3 lines when in output mode are "ANDed" with the SPI control signals and are all open-drain. PC0 is connected to the SPI clock signal (SCL), PC1 with the SPI data signal (SDA) while PC3 is connected with SPI enable signal (SEN, used in S-BUS protocol). Pin PC4 and PC6 can also be inputs to software programmable edge sensitive latches which can generate interrupts; PC4 can be connected to Power Interrupt while PC6 can be connected to the IRIN/NMI interrupt line. Refer to I/O PORT description, Pin Configurations (Figures 1 to 4), INTERRUPT description for additional information.

DA0-DA5. These pins are the six PWM D/A outputs of the 6-bit on-chip D/A converters. These lines have open-drain outputs with 12V drive. The output repetition rate is 31.25KHz (with 8MHz clock). Refer to Pin Configurations (Figures 1 to 4) and D/A description for additional information.

PIN DESCRIPTION (Continued)

AFC. This is the input of the on-chip 10 levels comparator that can be used to implement the AFC function. This pin is an high impedance input able to withstand signals with a peak amplitude up to 12V. Refer to Pin Configurations (Figures 1 to 4) and AFC description for additional information.

OSDOSCIN, OSDOSCOUT. These are the On Screen display oscillator terminals. An oscillation capacitor and coil network have to be connected to provide the right signal to the OSD.

HSYNC, VSYNC. These are the horizontal and vertical synchronization pins. The active polarity of these pins to the OSD macrocell can be selected by the user as ROM mask option. If the device is specified to have negative logic inputs, then when these signals are low the OSD oscillator stops. If the device is specified to have positive logic inputs, then when these signals are high the OSD oscillator stops. Refer to OSD description for additional information.

R, G, B, BLANK. Outputs from the OSD. R, G and B are the color outputs while BLANK is the blanking output. All outputs are push-pull. The active polarity of these pins can be selected by the user as ROM mask option. Refer to the pin configurations for additional information.

62.5kHz OUT. This pin is an open drain (12V) output at a frequency of 62.5kHz (with an 8MHz clock). The pin can be used to drive the SGS-THOMSON TEA5640 chroma processor. Refer to the TEA5640 data sheet for more information.

VS. This is the output pin of the on-chip 14-bit voltage synthesis tuning cell (VS). The tuning signal present at this pin gives an approximate resolution of 40KHz per step ovre the UHF band. This line is a push-pull output with standard drive .

Table 2. ST638X Pin Summary

Pin Function	Description
DA0 to DA5	Output, Open-Drain, 12V
62.5KHz OUT	Output, Open-Drain, 12V
AFC	Input, High Impedance, 12V
VS	Output, Push-Pull
R,G,B, BLANK	Output, Push-Pull
HSYNC, VSYNC	Input, Pull-up, Schmitt Trigger
OSDOSCIN	Input, High Impedance
OSDOSCOUT	Output, Push-Pull
TEST	Input, Pull-Down
OSCIN	Input, Resistive Bias, Schmitt Trigger to Reset Logic Only
OSCOUT	Output, Push-Pull
RESET	Input, Pull-up, Schmitt Trigger Input
PA0-PA3	I/O, Push-Pull, Software Input Pull-up, Schmitt Trigger Input
PA4-PA5	I/O, Open-Drain, 12V, No Input Pull-up, Schmitt Trigger Input
PA6-PA7	I/O, Open-Drain, 12V, No Input Pull-up, Schmitt Trigger Input, High Drive
PB0-PB2	I/O, Push-Pull, Software Input Pull-up, Schmitt Trigger Input
PB4-PB6	I/O, Push-Pull, Software Input Pull-up, Schmitt Trigger Input
PC0-PC3	I/O, Open-Drain, 5V , Software Input Pull-up, Schmitt Trigger Input
PC4-PC7	I/O, Open-Drain, 12V, No Input Pull-up, Schmitt Trigger Input
V_{DD}, V_{SS}	Power Supply Pins

ST638X CORE

The Core of the ST638X Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control busses. The in-core communication is arranged as shown in the following block diagram figure; the controller being externally linked to both the reset and the oscillator, while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes through the control registers.

Registers

The ST638X Family Core has five registers and three pairs of flags available to the programmer. They are shown in Figure 7 and are explained in the following paragraphs together with the program and data memory page registers.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is addressed in the data space as RAM location at the FFH address.

Figure 7. ST638X Core Programming Model

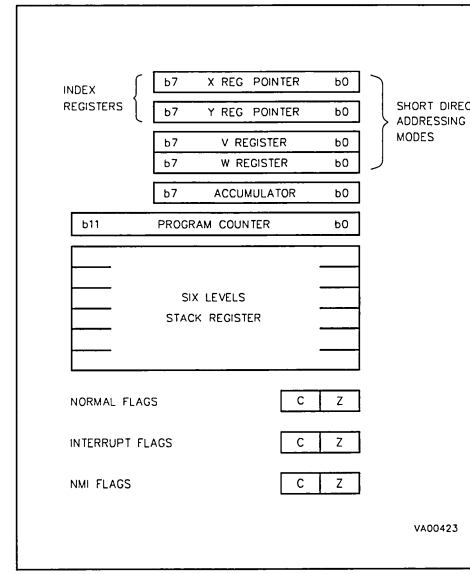
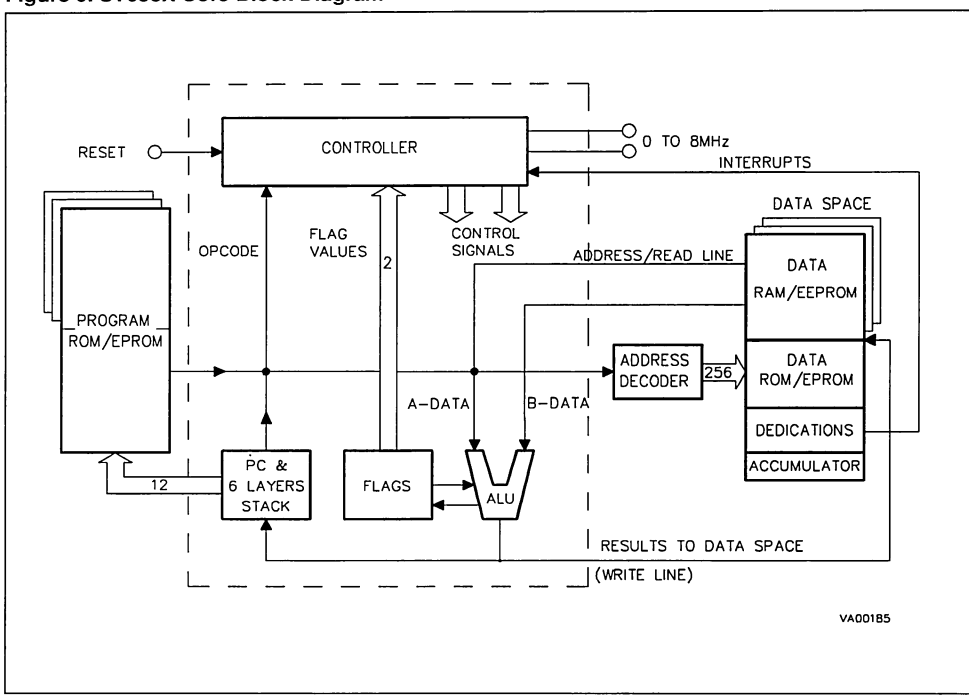


Figure 6. ST638X Core Block Diagram



ST638X CORE (Continued)

Accordingly, the ST638X instruction set can use the accumulator as any other register of the data space.

Indirect Registers (X, Y). These two indirect registers are used as pointers to the memory locations in the data space. They are used in the register-indirect addressing mode.These registers can be addressed in the data space as RAM locations at the 80H (X) and 81H (Y) addresses. They can also be accessed with the direct, short direct, or bit direct addressing modes. Accordingly, the ST638X instruction set can use the indirect registers as any other register of the data space.

Short Direct Registers (V, W). These two registers are used to save one byte in short direct addressing mode. These registers can be addressed in the data space as RAM locations at the 82H (V) and 83H (W) addresses. They can also be accessed with the direct and bit direct addressing modes. Accordingly, the ST638X instruction set can use the short direct registers as any other register of the data space.

Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM location to be processed by the core. This ROM location may be an opcode, an operand, or an address of operand. The 12-bit length allows the direct addressing of 4096 bytes in the program space. Nevertheless, if the program space contains more than 4096 locations, the further program space can be addressed by using the Program Bank Switch register. The PC value is incremented, after it is read for the address of the current instruction, by sending it through the ALU, so giving the address of the next byte in the program. To execute relative jumps the PC and the offset values are shifted through the ALU, where they will be added, and the result is shifted back into the PC. The program counter can be changed in the following ways:

JP (Jump) instruction	PC= Jump address
CALL instruction	PC= Call address
Relative Branch instructions	PC= PC+offset
Interrupt	PC= Interrupt vector
Reset	PC= Reset vector
Test mode	PC=Test mode vector (1)
RET & RETI instructions	PC= Pop (stack)
Normal instruction	PC= PC+1

Note: 1. Not available to the user.

Flags (C, Z)

The ST63 Core includes three pairs of flags that correspond to 3 different modes: normal mode, interrupt mode and Non-Maskable-Interrupt-Mode. Each pair consists of a CARRY flag and a ZERO flag. One pair (CN, ZN) is used during normal operation, one pair is used during the interrupt mode (CI,ZI) and one is used during the not-maskable interrupt mode (CNMI, ZNMI).

The ST63 Core uses the pair of flags that corresponds to the actual mode: as soon as an interrupt (resp. a Non-Maskable-Interrupt) is generated, the ST638X Core uses the interrupt flags (resp. the NMI flags) instead of the normal flags. When the RETI instruction is executed, the normal flags (resp. the interrupt flags) are restored if the MCU was in the normal mode (resp. in the interrupt mode) before the interrupt. Should be observed that each flag set can only be addressed in its own routine (Not-maskable interrupt, normal interrupt or main routine). The interrupt flags are not cleared during the context switching and so, they remain in the state they were at the exit of the last routine switching.

The Carry flag is set when a carry or a borrow occurs during arithmetic operations, otherwise it is cleared. The Carry flag is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

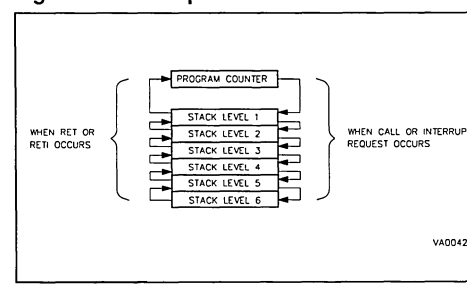
The Zero flag is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

The switching between these three sets is automatically performed when an NMI, an interrupt and a RETI instructions occur. As the NMI mode is automatically selected after the reset of the MCU, the ST638X Core uses at first the NMI flags. Refer to INTERRUPT description for additional information.

Stack

The ST638X Core includes true LIFO hardware stack that eliminates the need for a stack pointer.

Figure 8. Stack Operation

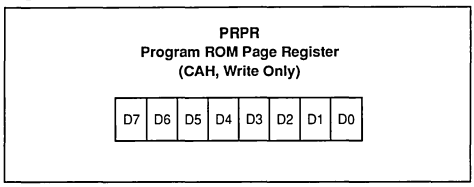


ST638X CORE (Continued)

The stack consists of six separate 12-bit RAM locations that do not belong to the data space RAM area. When a subroutine call (or interrupt request) occurs, the contents of each level is shifted into the next level while the content of the PC is shifted into the first level (the value of the sixth level will be lost). When subroutine or interrupt return occurs (RET or RETI instructions), the first level register is shifted back into the PC and the value of each level is shifted back into the previous level. These two operating modes are described in Figure 8. Since the accumulator, as all other data space registers, is not stored in this stack the handling of this registers shall be performed inside the subroutine. The stack pointer will remain in its deepest position, if more than 6 calls or interrupts are executed, so that the last return address will be lost. It will also remain in its highest position if the stack is empty and a RET or RETI is executed. In this case the next instruction will be executed.

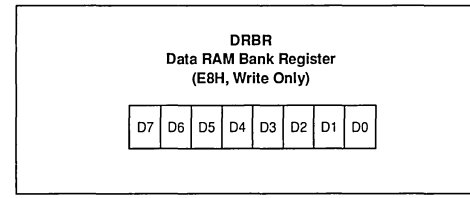
Memory Registers

Figure 9. Program ROM Page Register



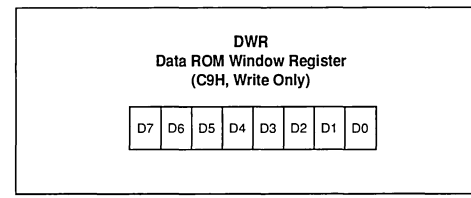
The PRPR register can be addressed like a RAM location in the Data Space at the CAH address; nevertheless it is a write-only register that can not be accessed with single-bit operations. This register is used to select the 2-Kbyte ROM bank of the Program Space that will be addressed. The number of the page has to be loaded in the PRPR register. The PRPR register is not cleared during the MCU initialization and should therefore be defined before jumping out of the static page. Refer to the Program Space description for additional information concerning the use of this registers. The PRPR register is not modified when an interrupt or a subroutine occurs.

Figure 10. Data RAM Bank Manager



The DRBR register can be addressed like a RAM location in the Data Space at the E8H address, nevertheless it is write-only register that can not be accessed with single-bit operations. This register is used to select the desired 64-byte RAM/EEPROM bank of the Data Space. The number of the bank has to be loaded in the DRBR register and the instruction has to point to the selected location as it was in the 0 bank (from 00H address to 3FH address). This register is cleared during the MCU initialization (the Data space 0 bank is automatically addressed after the Reset). Refer to the Data Space description for additional information. The DRBR register is not modified when a interrupt or a subroutine occurs.

Figure 11. Data ROM Window Register



The DWR register can be addressed like a RAM location in the Data Space at the C9H address, nevertheless it is write-only register that can not be accessed with single-bit operations. This register is used to move up and down the 64-byte read-only data window (from the 40H address to 7FH address of the Data Space) along the ROM memory of the MCU by step of 64 bytes. The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 less significant bits of the address given in the instruction (as less significant bits) and the content of the DWR register (as most significant bits). Refer to the Data Space description for additional information.

MEMORY SPACES

The MCUs operate in three different memory spaces: Program Space, Data Space, and Stack Space. A description of these spaces is shown in Figure 12 and Figure 13. (Figure 14 refers to the ST638X which has a total of 20K bytes of ROM).

Figure 12. ST638X Data Space

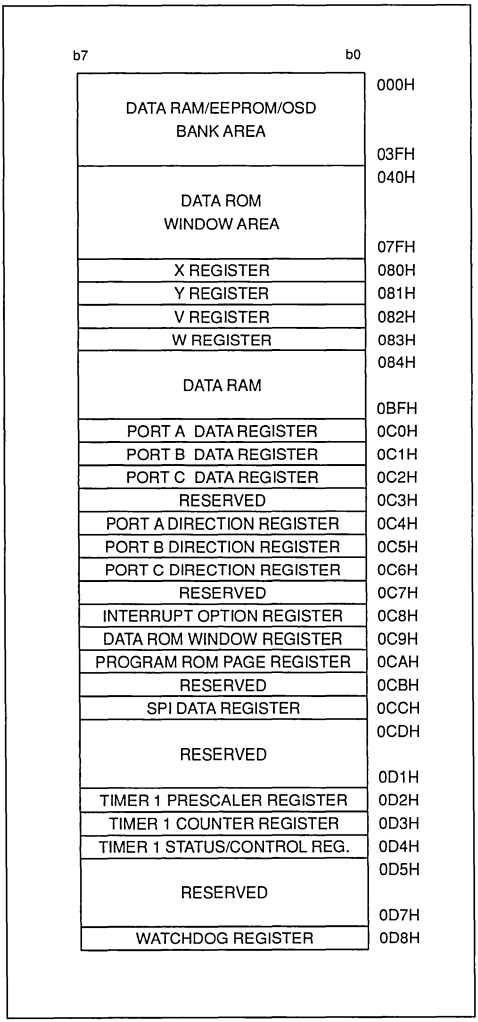
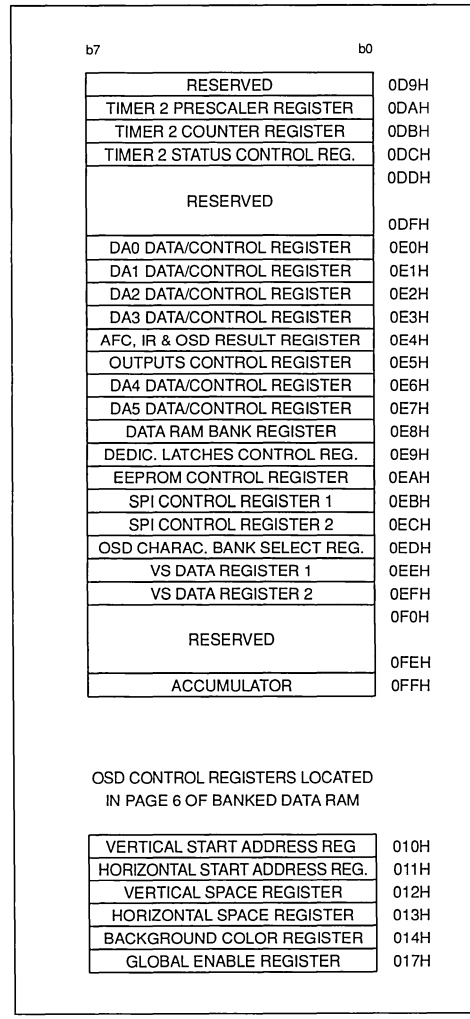
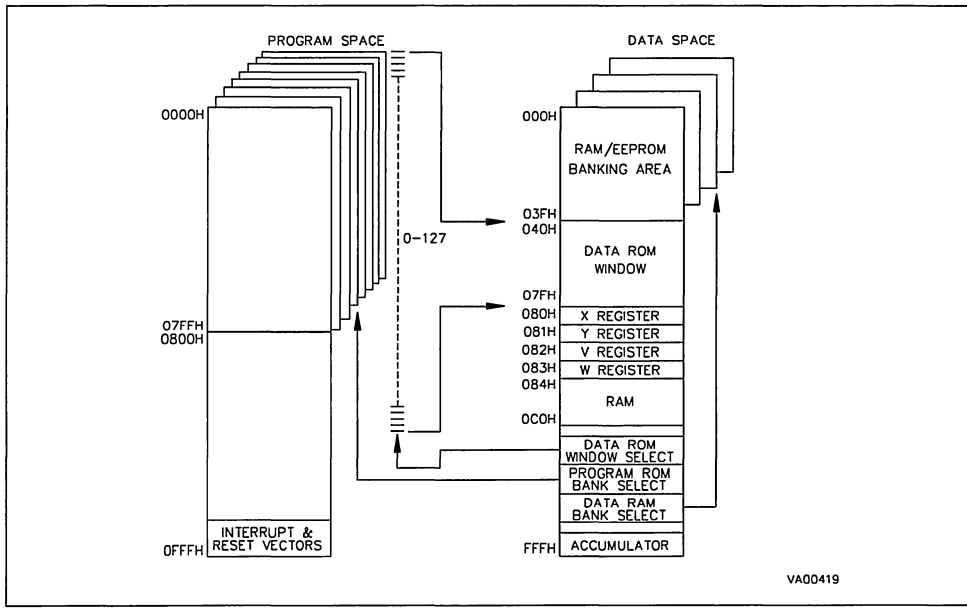


Figure 13. ST638X Data Space (Continued)



MEMORY SPACES (Continued)

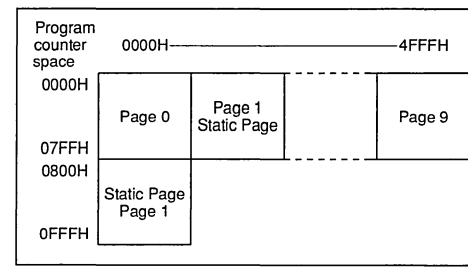
Figure 14. ST638X Memory Addressing Description Diagram



Program Space

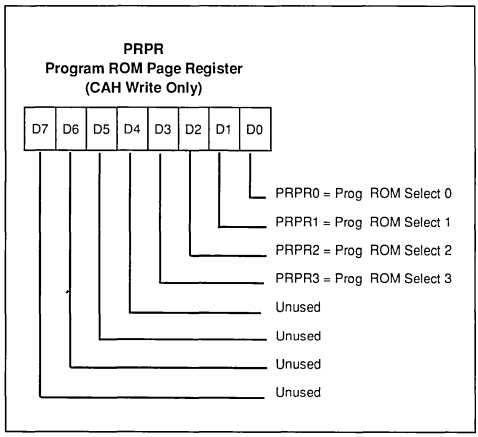
The program space is physically implemented in the ROM memory and includes all the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, the reserved test area and user vectors. It is addressed thanks to the 12-bit Program Counter register (PC register) and so, the ST638X Core can directly address up to 4K bytes of Program Space. Nevertheless, the Program Space can be extended by the addition of 2-Kbyte ROM banks as it is shown in figure 14 in which a 20K bytes memory is described. These banks are addressed by pointing to the 000H-7FFH locations of the Program Space thanks to the Program Counter, and by writing the appropriate code in the Program ROM Page Register (PRPR register) located at the CAH address of the Data Space. Because interrupts and common subroutines should be available all the time only the lower 2K byte of the 4K program space are bank switched while the upper 2K byte can be seen as static space. Table 3 gives the different codes that allows the selection of the corresponding banks. Note that, from the memory point of view, the Page 1 and the Static Page represent the same physical memory: it is only a different way of addressing the same location. On the ST638X a total of 20480 bytes of ROM have been implemented; 20140 are available as user ROM while 340 are reserved for testing.

Figure 15. ST638X 20K Bytes Program Space Addressing Description



MEMORY SPACES (Continued)

Figure 16. Program ROM Page Register



D7-D5. These bits are not used.

PRPR4-PRPR0. These are the program ROM banking bits and the value loaded selects the corresponding page to be addressed in the lower part of 4K program address space as specified in Table 3. This register is undefined on reset.

Table 3. ST638X Program ROM Page Register Coding

PRPR3	PRPR2	PRPR1	PRPR0	PC11	Memory Page
X	X	X	X	1	Static Page (Page 1)
0	0	0	0	0	Page 0
0	0	0	1	0	Page 1 (Static Page)
0	0	1	0	0	Page 2
0	0	1	1	0	Page 3
0	1	0	0	0	Page 4
0	1	0	1	0	Page 5
0	1	1	0	0	Page 6
0	1	1	1	0	Page 7
1	0	0	0	0	Page 8
1	0	0	1	0	Page 9

Note. The number of bits implemented depends on the size of the ROM of the device. Only the lower part of address space has been bankswitched because interrupt vectors and common subroutines should be available all the time. The reason of this structure is due to the fact that it is not possible to jump from a dynamic page to another, unless jumping back to the static page, changing contents of PRPR, and, than, jumping to a different dynamic page.

Care is required when handling the PRPR register as it is write only. For this reason, it is not allowed to change the PRPR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. Anyway, this operation may be necessary if the sum of common routines and interrupt drivers will take more than 2K bytes; in this case could be necessary to divide the interrupt driver in a (minor) part in the static page (start and end), and in the second (major) part in one dynamic page. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the PRPR it writes also the image register. The image register must be written first, so if an interrupt occurs between the two instructions the PRPR register is not affected.

MEMORY SPACE (Continued)

Table 4. ST638X Program ROM Memory Map (up to 20K Bytes)

ROM Page	Device Address	EPROM Address (1)	Description
PAGE 0	0000H-007FH 0080H-07FFH	0000H-007FH 0080H-07FFH	Reserved User ROM
PAGE 1 "STATIC"	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	User ROM Reserved Interrupt Vectors Reserved NMI Vector Reset Vector
PAGE 2	0000H-000FH 0010H-07FFH	1000H-100FH 1010H-17FFH	Reserved User ROM
PAGE 3	0000H-000FH 0010H-07FFH	1800H-180FH 1810H-1FFFH	Reserved User ROM
PAGE 4	0000H-000FH 0010H-07FFH	2000H-200FH 2010H-27FFH	Reserved User ROM
PAGE 5	0000H-000FH 0010H-07FFH	2800H-280FH 2810H-2FFFH	Reserved User ROM
PAGE 6	0000H-000FH 0010H-07FFH	3000H-300FH 3010H-37FFH	Reserved User ROM
PAGE 7	0000H-000FH 0010H-07FFH	3800H-380FH 3810H-3FFFH	Reserved User ROM
PAGE 8	0000H-000FH 0010H-07FFH	4000H-400FH 4010H-47FFH	Reserved User ROM
PAGE 9	0000H-000FH 0010H-07FFH	4800H-480FH 4810H-4FFFH	Reserved User ROM

Notes:
1. EPROM addresses are related to the use of ST63P8X piggyback emulation devices.

MEMORY SPACE (Continued)

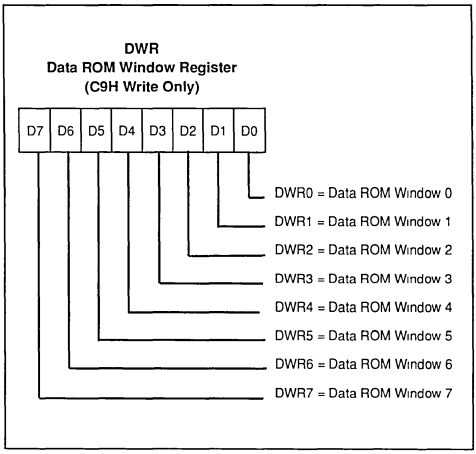
Data Space

The instruction set of the ST638X Core operates on a specific space, named Data Space that contains all the data necessary for the processing of the program. The Data Space allows the addressing of RAM memory (up to 256 bytes for the ST638X family), EEPROM memory (up to 384 bytes for the ST638X family), ST638X Core/peripheral registers, and read-only data such as constants and the look-up tables.

Data ROM Addressing. All the read-only data are physically implemented in the ROM memory in which the Program Space is also implemented. The ROM memory therefore contains the program to be executed and also the constants and the look-up tables needed for the program. The locations of Data Space in which the different constants and look-up tables are addressed by the ST638X Core can be considered as being a 64-byte window through which it is possible to access to the read-only data stored in the ROM memory. This window is located from the 40H address to the 7FH address in the Data space and allows the direct reading of the bytes from the 000H address to the 03FH address in the ROM memory. All the bytes of the ROM memory can be used to store either instructions or read-only data. Indeed, the window can be moved by step of 64 bytes along the ROM memory in writing the appropriate code in the Write-only Data ROM Window register (DWR register, location C9H). The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 less significant bits of the address in the Data Space (as less significant bits) and the content of the DWR register (as most significant bits). So when addressing location 40H of data space, and 0 is loaded in the DWR register, the physical addressed location in ROM is 00H.

Note. The data ROM window cannot address windows above the 16k byte range.

Figure 17. Data ROM Window Register



DWR7-DWR0. These are the Data Rom Window bits that correspond to the upper bits of data ROM program space. This register is undefined after reset.

Notes Care is required when handling the DWR register as it is write only. For this reason, it is not allowed to change the DWR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the DWR it writes also the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DWR register is not affected.

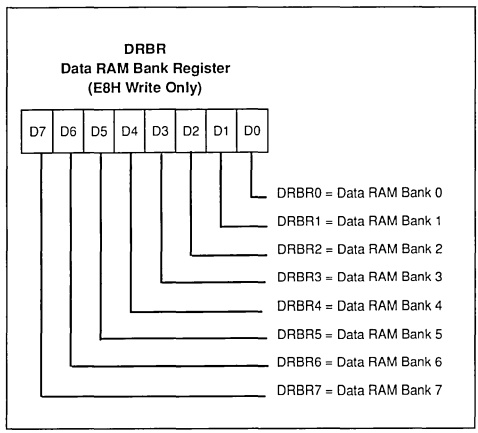
Data RAM/EEPROM/OSD RAM Addressing

In all members of the ST638X family 64 bytes of data RAM are directly addressable in the data space from 80H to BFH addresses. The additional 192 bytes of RAM, the 384 bytes of EEPROM memory , and the

MEMORY SPACE (Continued)

OSD RAM can be addressed using the banks of 64 bytes located between addresses 00H and 3FH. The selection of the bank is done by programming the Data RAM Bank Switching register (DRBR register) located at the E8H address of the Data Space. In this way each bank of RAM, EEPROM or OSD RAM can select 64 bytes at a time. No more than one bank should be set at a time.

Figure 18. Data RAM Bank Register



DRBR7,DRBR1,DRBR0. These bits select the EEPROM pages.

DRBR6, DRBR5. Each of these bits, when set, will select one OSD RAM register page.

DRBR4,DRBR3,DRBR2. Each of these bits, when set, will select one RAM page.

This register is undefined after reset.

Table 5 summarizes how to set the Data RAM Bank Register in order to select the various banks or pages.

Notes :
Care is required when handling the DRBR register as it is write only. For this reason, it is not allowed to change the DWR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the DRBR it writes also the image register.
The image register must be written first, so if an interrupt occurs between the two instructions the DRBR register is not affected.

EEPROM Description

The data space of ST638X family from 00H to 3FH is paged as described in Table 5. 384 bytes of EEPROM located in six pages of 64 bytes (pages 0,1,2,3,4,5 and 6, see Table 5).

Through the programming of the Data RAM Bank Register (DRBR= E8H) the user can select the bank or page leaving unaffected the way to address the static registers. The way to address the "dy-

Table 5. Data RAM Bank Register Set-up

DRBR Value	Selection	Applicable Devices
01H	EEPROM Page 0	All Devices
02H	EEPROM Page 1	All Devices
03H	EEPROM Page 2	All Devices
81H	EEPROM Page 3	All Devices
82H	EEPROM Page 4	All Devices
83H	EEPROM Page 5	All Devices
04H	RAM Page 2	All Devices
08H	RAM Page 3	All Devices
10H	RAM Page 4	All Devices
20H	OSD Page 5	All Devices
40H	OSD Page 6	All Devices

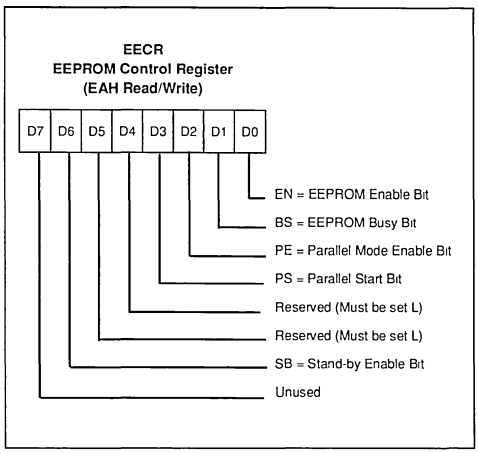
MEMORY SPACE (Continued)

namic" page is to set the DRBR as described in Table 5 (e.g. to select EEPROM page 0, the DRBR has to be loaded with content 01H, see Data RAM/EEPROM/OSD RAM addressing for additional information). Bits 0, 1 and 7 of the DRBR are dedicated to the EEPROM.

The EEPROM module is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. The EEPROM is controlled by the EEPROM Control Register (EECR=EAH). Any EEPROM location can be read just like any other data location, also in terms of access time.

To write an EEPROM location takes about 5 mSec (10mSec max) and during this time the EEPROM is not accessible by the Core. A busy flag can be read by the Core to know the EEPROM status before trying any access. In writing the EEPROM can work in two modes: Byte Mode (BMODE) and Parallel Mode (PMODE). The BMODE is the normal way to use the EEPROM and consists in accessing one byte at a time. The PMODE consists in accessing 8 bytes per time.

Figure 19. EEPROM Control Register



D7. Not used

SB. *WRITE ONLY.* If this bit is set the EEPROM is disabled (any access will be meaningless) and the power consumption of the EEPROM is reduced to the leakage values.

D5, D4. Reserved for testing purposes, they must be set to zero.

PS. *SET ONLY.* Once in Parallel Mode, as soon as the user software sets the PS bit the parallel writing of the 8 adjacent registers will start. PS is internally reset at the end of the programming procedure. Note that less than 8 bytes can be written; after parallel programming the remaining undefined bytes will have no particular content.

PE. *WRITE ONLY.* This bit must be set by the user program in order to perform parallel programming (more bytes per time). If PE is set and the "parallel start bit" (PS) is low, up to 8 adjacent bytes can be written at the maximum speed, the content being stored in volatile registers. These 8 adjacent bytes can be considered as row, whose A7, A6, A5, A4, A3 are fixed while A2, A1 and A0 are the changing bytes. PE is automatically reset at the end of any parallel programming procedure. PE can be reset by the user software before starting the programming procedure, leaving unchanged the EEPROM registers.

BS. *READ ONLY.* This bit will be automatically set by the CORE when the user program modifies an EEPROM register. The user program has to test it before any read or write EEPROM operation; any attempt to access the EEPROM while "busy bit" is set will be aborted and the writing procedure in progress completed.

EN. *WRITE ONLY.* This bit MUST be set to one in order to write any EEPROM register. If the user program will attempt to write the EEPROM when EN= 0 the involved registers will be unaffected and the "busy bit" will not be set.

After RESET the content of EECR register will be 00H.

Notes :
When the EEPROM is busy (BS= 1) the EECR can not be accessed in write mode, it is only possible to read BS status. This implies that as long as the EEPROM is busy it is not possible to change the status of the EEPROM control register. EECR bits 4 and 5 are reserved for testing purposes, and the user must never set them to 1.

Additional Notes on Parallel Mode. If the user wants to perform a parallel programming the first action should be the set to one the PE bit; from this moment the first time the EEPROM will be addressed in writing, the ROW address will be latched and it will be possible to change it only at the end of the programming procedure or by resetting PE without programming the EEPROM. After the ROW address latching the Core can "see" just one EEPROM row (the selected one) and any attempt to write or read other rows will produce errors. Do not read the EEPROM while PR is set.

As soon as PE bit is set, the 8 volatile ROW latches are cleared. From this moment the user can load

MEMORY SPACE (Continued)

data in the whole ROW or just in a subset. PS setting will modify the EEPROM registers corresponding to the ROW latches accessed after PE. For example, if the software sets PE and accesses EEPROM in writing at addresses 18H,1AH,1BH and then sets PS, these three registers will be modified at the same time; the remaining bytes will have no particular content. Note that PE is internally reset at the end of the programming procedure. This implies that the user must set PE bit between two parallel programming procedures. Anyway the user can set and then reset PE without performing any EEPROM programming. PS is a set only bit and is internally reset at the end of the programming procedure. Note that if the user tries to set PS while PE is not set there will not be any programming procedure and the PS bit will be unaffected. Consequently PS bit can not be set if EN is low. PS can be affected by the user set if, and only if, EN and PE bits are also set to one.

Warning : *Parallel programming of the EEPROM with less than eight bytes may corrupt other bytes and should therefore be used with care, as here after underlined.*

a. *Reason for limitation:*
betweeen PE (Parallel Enable) and PS (Parallel Start) of the EEPROM, the user writes up to eight bytes into the volatile data registers, a latch is also set to indicate which bytes have been accessed; the accessed bytes will be programmed when PS arrives. The logic is such that it is possible to set the latches of bytes which have NOT been accessed. The latches are set whenever ANY register in the banked dataspace (00h-3FH) is accessed for READ or WRITE between a PE and PS. The latch which is set will be determined by the three least significant bits of the register address. Only the latch is set, so final data of a corrupted byte after the parallel programming is always FFH.

Note: *read operations also occur internally to the micro for most instructions. Even if bytes are not seen to be corrupted within the parallel programming routine, care should be taken, since they could become corrupted by an interrupt routine being serviced during loading of parallel bytes.*
This is logic related and is not a marginality or race condition; piggyback devices perform in the same way as ROM devices. Parallel programming is tested with only LDI rr,nn instructions which do not corrupt other bytes.

b. *To Avoid Corrupted Bytes:*
   - *use Single Byte Mode, or*
   - *always define all eight bytes in Parallel Programming Mode, or*
   - *when programming less than eight bytes, the remaining EEPROM bytes should do not used by the program.*

Additional Notes Regarding Differences Between ST638X Devices and Corresponding Emulators. While PE is set, all the EEPROM page currently selected is accessible in reading and the writing of the bytes happens at the row to which belongs the last byte written before setting PS. The sequence: set PE, write in 10H the value X, write in 21H the value Y, set PS, will result in: 10H unchanged, 20H loaded with value X, 21H loaded with value Y. In the emulator bits 4 and 5 of the EECR are implemented.If the user set to 1 one or both of these bits the contents of the EEPROM will be destroyed. The user should use care in using EEPROM emulation as in general the emulator does not emulate the behaviour of the EEPROM when it is misused.

STACK SPACE

The stack space consists of six 12 bit registers that are used for stacking subroutine and interrupt return addresses plus the current program counter register.

TEST MODE

The test mode can be entered by connecting the TEST pin to an high logic level when reset is active; this action enables the factory test mode. The user is recommended to avoid this situation for normal operation. (TEST pin should be tied to ground).

INTERRUPT

The ST638X Core can manage 4 different maskable interrupt sources, plus one non-maskable interrupt source (top priority level interrupt). Each source is associated with a particular interrupt vector that contains a Jump instruction to the related interrupt service routine. Each vector is located in the Program Space at a particular address (see Table 6). When a source provides an interrupt request, and the request processing is also enabled by the ST638X Core, then the PC register is loaded with the address of the interrupt vector (i.e. of the Jump instruction). Finally, the PC is loaded with the address of the Jump instruction and the interrupt routine is processed.

The relationship between vector and source and the associated priority is hardware fixed for the different ST638X devices. For some interrupt sources it is also possible to select by software the kind of event that will generate the interrupt.

All interrupts can be disabled by writing to the GEN bit (global interrupt enable) of the interrupt option register (address C8H). After a reset, ST638X is in non maskable interrupt mode, so no interrupts will be accepted and NMI flags will be used, until a RETI

INTERRUPT (Continued)

RETI instruction is executed. If an interrupt is executed, one special cycle is made by the core, during that the PC is set to the related interrupt vector address. A jump instruction at this address has to redirect program execution to the beginning of the related interrupt routine. The interrupt detecting cycle, also resets the related interrupt flag (not available to the user), so that another interrupt can be stored for this current vector, while its driver is under execution.

If additional interrupts arrive from the same source, they will be lost. NMI can interrupt other interrupt routines at any time, while other interrupts cannot interrupt each other. If more than one interrupt is waiting for service, they are executed according to their priority. The lower the number, the higher the priority. Priority is, therefore, fixed. Interrupts are checked during the last cycle of an instruction (RETI included). Level sensitive interrupts have to be valid during this period.

Table 6. Interrupt Vectors/Sources Relationships

Interrupt Source	Associated Vector	Vector Address
PC6/IRIN Pin (1)	Interrupt Vector # 0 (NMI)	0FFCH-0FFDH
Timer 2	Interrupt Vector # 1	0FF6H-0FF7H
Vsync	Interrupt Vector # 2	0FF4H-0FF5H
Timer 1	Interrupt Vector # 3	0FF2H-0FF3H
PC4/PWRIN	Interrupt Vector # 4	0FF0H-0FF1H

Note: 1. This pin is associated with the NMI Interrupt Vector

Table 6 details the different interrupt vectors/sources relationships.

Interrupt Vectors/Sources

The ST638X Core includes 5 different interrupt vectors in order to branch to 5 different interrupt routines. The interrupt vectors are located in the fixed (or static) page of the Program Space.

The interrupt vector associated with the non-maskable interrupt source is named interrupt vector #0. It is located at the (FFCH,FFDH) addresses in the Program Space. This vector is associated with the PC6/IRIN pin; refer to the ST638X Interrupt Details section for more information.

The interrupt vectors located at addresses (FF6H,FF7H), (FF4H,FF5H), (FF2H,FF3H), (FF0H,FF1H) are named interrupt vectors #1, #2, #3 and #4 respectively. These vectors are associated with TIMER 2 (#1), VSYNC (#2), TIMER 1 (#3) and PC4(PWRIN) (#4); refer to the ST638X Interrupt Details description for more information.

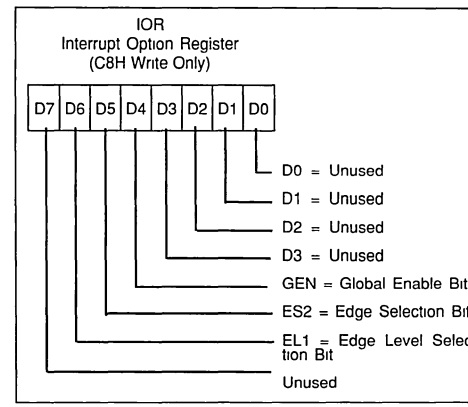
Interrupt Priority

The non-maskable interrupt request has the highest priority and can interrupt any other interrupt routines at any time, nevertheless the other interrupts cannot interrupt each other. If more than one interrupt request is pending, they are processed by the ST638X Core according to their priority level: vector #1 has the higher priority while vector #4 the lower. The priority of each interrupt source is hardware fixed.

Interrupt Option Register

The Interrupt Option Register (IOR register, location C8H) is used to enable/disable the individual interrupt sources and to select the operating mode of the external interrupt inputs. This register can be addressed in the Data Space as RAM location at the C8H address, nevertheless it is write-only register that can not be accessed with single-bit operations. The operating modes of the external

Figure 20. Interrupt Option Register



interrupt inputs associated to interrupt vectors #1 and #2 are selected through bits 4 and 5 of the IOR register.

D7. Not used.

EL1. This is the Edge/Level selection bit of interrupt #1. When set to one, the interrupt is generated on low level of the related signal; when cleared to zero, the interrupt is generated on falling edge. The bit is cleared to zero after reset.

INTERRUPT (Continued)

ES2. This is the edge selection bit on interrupt #2. This bit is used on the ST638X devices with on-chip OSD generator for VSYNC detection.

GEN. This is the global enable bit. When set to one all interrupts are globally enabled; when this bit is cleared to zero all interrupts are disabled (including NMI).

D3 - D0. These bits are not used.

Interrupt Procedure

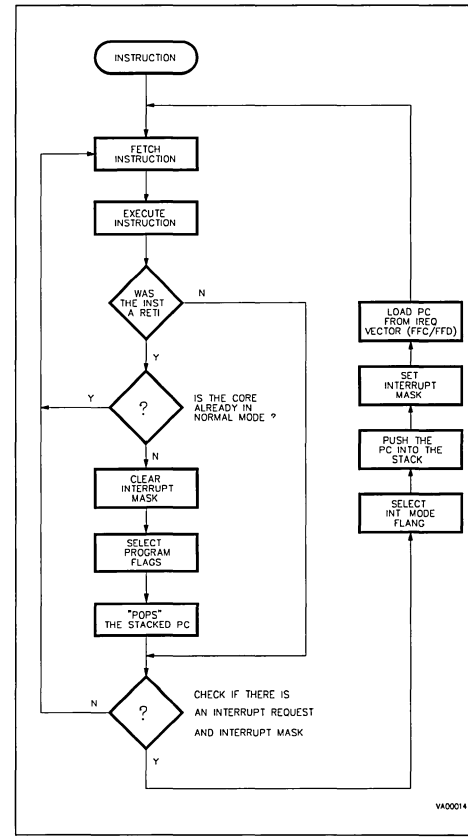
The interrupt procedure is very similar to a call procedure; the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event the user does not know about the context and the time at which it occurred. As a result the user should save all the data space registers which will be used inside the interrupt routines. There are separate sets of processor flags for normal, interrupt and non-maskable interrupt modes which are automatically switched and so these do not need to be saved.

The following list summarizes the interrupt procedure (refer also to Figure 21. Interrupt Processing Flow Chart):

- Interrupt detection
- The flags C and Z of the main routine are exchanged with the flags C and Z of the interrupt routine (resp. the NMI flags)
- The value of the PC is stored in the first level of the stack - The normal interrupt lines are inhibited (NMI still active)
- The edge flip-flop is reset
- The related interrupt vector is loaded in the PC.
- User selected registers are saved inside the interrupt service routine (normally on a software stack)
- The source of the interrupt is found by polling (if more than one source is associated to the same vector)
- Interrupt servicing
- Return from interrupt (RETI)
- Automatically the ST638X core switches back to the normal flags (resp the interrupt flags) and pops the previous PC value from the stack

The interrupt routine begins usually by the identification of the device that has generated the interrupt request. The user should save the registers which are used inside the interrupt routine (that holds relevant data) into a software stack.
After the RETI instruction execution, the Core carries out the previous actions and the main routine can continue.

Figure 20. Interrupt Processing Flow-Chart



ST638X Interrupt Details

IR Interrupt (#0). The IRIN/PC6 Interrupt is connected to the first interrupt #0 (NMI, 0FFCH). If the $\overline{\text{IRINT}}$ interrupt is disabled at the Latch circuitry, then it will be high. The #0 interrupt input detects a high to low level. Note that once # 0 has been latched, then the only way to remove the latched # 0 signal is to service the interrupt. # 0 can interrupt the other interrupts. A simple latch is provided from the PC6(IRIN) pin in order to generate the $\overline{\text{IRINT}}$ signal. This latch can be triggered by either the positive or negative edge of IRIN signal. $\overline{\text{IRINT}}$ is inverted with respect to the latch. The latch can be read by software and reset by software.

TIMER 2 Interrupt (# 1). The TIMER 2 Interrupt is connected to the interrupt # 1 (0FF6H). The TIMER 2 interrupt generates a low level (which is latched in the timer). For more information on the timer interrupt

INTERRUPT (Continued)

to remove the latched signal is to service the interrupt.

VSYNC Interrupt (#2). The VSYNC Interrupt is connected to the interrupt #2. When disabled the VSYNCINT signal is low. The VSYNCINT signal is inverted with respect to the signal applied to the VSYNCN pin. Bit 5 of the interrupt option register C8H is used to select the negative edge (B2=0) or the positive edge (B2=1); the edge will depend on the application. Note that once an edge has been latched, then the only way to remove the latched signal is to service the interrupt. Care must be taken not to generate spurious interrupts. This interrupt may be used for synchronize to the VSYNC signal in order to change characters in the OSD only when the screen is on vertical blanking (if desired). This method may also be used to blink characters.

TIMER 1 Interrupt (#3). The TIMER 1 Interrupt is connected to the fourth interrupt #3 (0FF2H) which detects a high to low level (latched in the timer). For more information on the timer interrupt refer to the timer section.

PWR Interrupt (#4). The PWR Interrupt is connected to the fifth interrupt #4 (0FF0H). If the PWRINTN is disabled at the PWR circuitry, then it will be high. The #4 interrupt input detects a low level. A simple latch is provided from the PC4 (PWRIN)pin in order to generate the PWRINTN signal. This latch can be triggered by either the positive or negative edge of the PWRIN signal. PWRINTN is inverted with respect to the latch. The latch can be reset by software.

Notes Global disable does not reset edge sensitive interrupt flags. These edge sensitive interrupts become pending again when global disabling is released. Moreover, edge sensitive interrupts are stored in the related flags also when interrupts are globally disabled, unless each edge sensitive interrupt is also individually disabled before the interrupting event happens. Global disable is done by clearing the GEN bit of Interrupt option register, while any individual disable is done in the control register of the peripheral. The on-chip Timer peripherals have an interrupt request flag bit (TMZ), this bit is set to one when the device wants to generate an

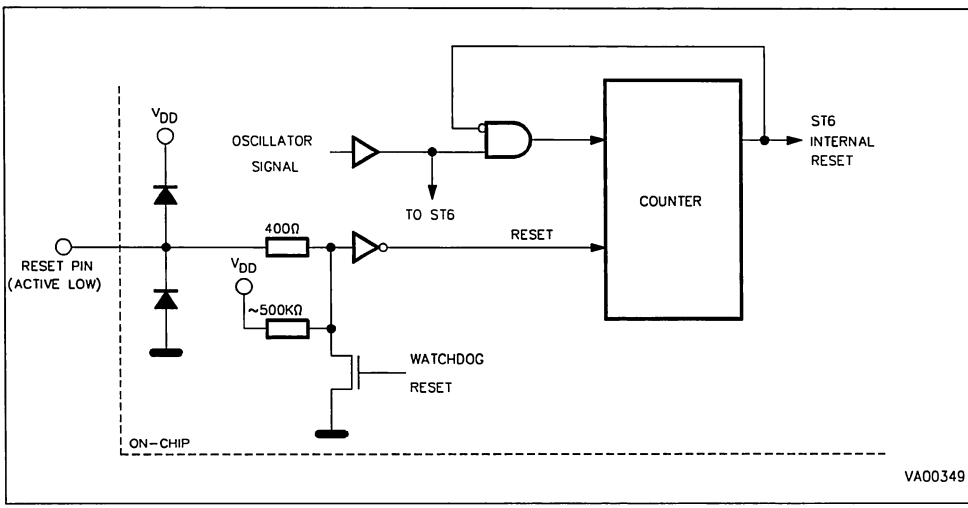
RESET

The ST638X devices can be reset in two ways: by the external reset input (RESET) tied low and by the hardware activated digital watchdog peripheral.

RESET Input

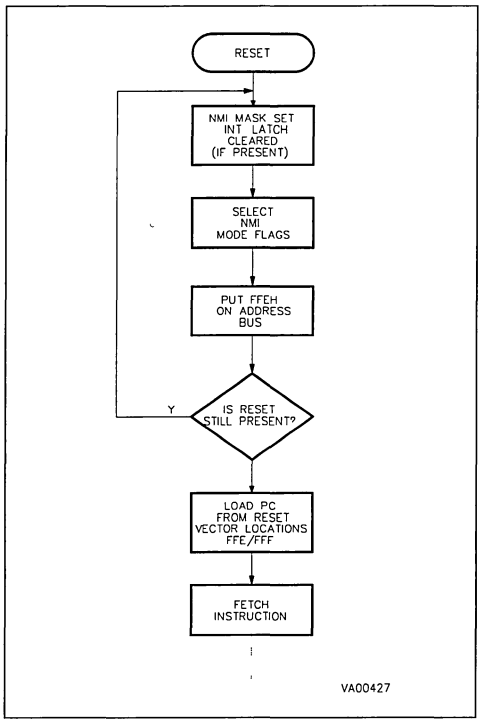
The external active low reset pin is used to reset the ST638X devices and provide an orderly software startup procedure. The activation of the Reset pin may occur at any time in the RUN or WAIT mode. Even short pulses at the reset pin will be accepted since the reset signal is latched internally and is only cleared after 2048 clocks at the oscillator pin. The clocks from the oscillator pin to the reset circuitry are buffered by a schmit trigger so that an oscillator in start-up conditions will not give spurious clocks. When the reset pin is held low, the external quartz oscillator is

Figure 22. Internal Reset Circuit



RESET (Continued)

Figure 23. Reset & Interrupt Processing Flow-chart

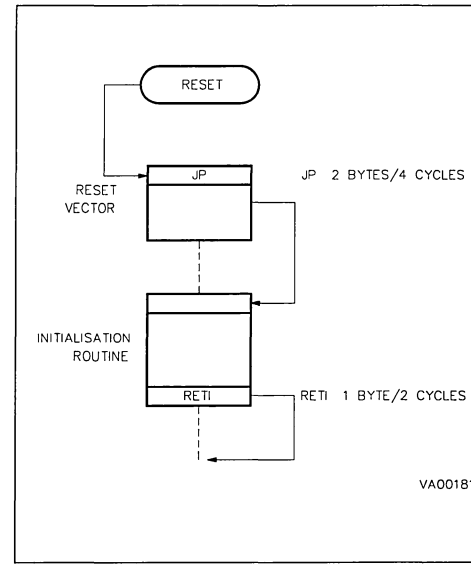


When the reset pin is held low, the external quartz oscillator is also disabled in order to reduce current consumption. The MCU is configured in the Reset mode as long as the signal of the RESET pin is low. The processing of the program is stopped and the standard Input/Output ports (port A, port B and port C) are in the input state. As soon as the level on the reset pin becomes high, the initialization sequence is executed. Refer to the MCU initialization sequence for additional information.

Watchdog Reset

The ST638X devices are provided with an on-chip hardware activated digital watchdog function in order to provide a graceful recovery from a software upset. If the watchdog register is not refreshed and the end-of-count is reached, then the reset state will be latched into the MCU and an internal circuit pulls down the reset pin. This also resets the watchdog which subsequently turns off the pull-down and activates the pull-up device at the reset pin. This causes the positive transition at

Figure 24. Restart Initialization Program Flow-chart



the reset pin. The MCU will then exit the reset state after 2048 clocks on the oscillator pin.

Application Notes

An external resistor between V_{DD} and the reset pin is not required because an internal pull-up device is provided. The user may prefer to add an external pull-up resistor.

An internal Power-on device does not guarantee that the MCU will exit the reset state when V_{DD} is above 4.5V and therefore the RESET pin should be externally controlled.

MCU Initialization Sequence

When a reset occurs the stack is reset to program counter, the PC is loaded with the address of the reset vector (located in the program ROM at addresses FFEH & FFFH). A jump instruction to the beginning of the program has to be written into these locations.After a reset the interrupt mask is automatically activated so that the Core is in non-maskable interrupt mode to prevent false or ghost interrupts during the restart phase. Therefore the restart routine should be terminated by a RETI instruction to switch to normal mode and enable interrupts. If no pending interrupt is present at the end of the reset routine, the ST638X will continue with the instruction after the RETI; otherwise the pending interrupt will be serviced.

RESET (Continued)

RESET Low Power Mode

When the reset pin is low, the quartz oscillator is Disabled allowing reduced current consumption. When the reset pin is raised the quartz oscillator is enabled and oscillations will start to build up.The internal reset circuitry will count 2048 clocks on the oscillator pin before allowing the MCU to go out of the reset state;the clocks are after a schmtit trigger so that false or multiple counts are not possible.

The stack space consists of six 12 bit registers that are used for stacking subroutine and interrupt return addresses plus the current program counter register.

TEST MODE

The test mode can be entered by connecting the TEST pin to an high logic level when reset is active; this action enables the factory test mode. The user is recommended to avoid this situation for normal operation. (TEST pin should be tied to ground).

WAIT & STOP MODES

The STOP and WAIT modes have been implemented in the ST638X Core in order to reduce the consumption of the device when the latter has no instruction to execute. These two modes are described in the following paragraphs. On ST638X as the hardware activated digital watchdog function is present the STOP instruction is de-activated and any attempt to execute it will cause the automatic execution of a WAIT instruction.

WAIT Mode

The configuration of the MCU in the WAIT mode occurs as soon as the WAIT instruction is executed. The microcontroller can also be considered as being in a "software frozen" state where the Core stops processing the instructions of the routine, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage but where the peripherals are still working.
The WAIT mode is used when the user wants to reduce the consumption of the MCU when it is in idle, while not loosing count of time or monitoring of external events. The oscillator is not stopped in order to provide clock signal to the peripherals. The timers counting may be enabled (writing the PSI bit in TSCR register) and the timer interrupt may be also enabled before entering the WAIT mode; this allows the WAIT mode to be left when timer interrupt occurs. If the exit from the WAIT mode is performed with a general RESET (either from the activation of the external pin or by watchdog reset) the MCU will enter a normal reset procedure as described in the RESET chapter. If an interrupt is generated during WAIT mode the MCU behaviour depends on the state of the ST638X Core before the initialization of the WAIT sequence, but also of the kind of the interrupt request that is generated. This case will be described in the following paragraphs. In any case, the ST638X Core does not generate any delay after the occurrence of the interrupt because the oscillator clock is still available.

STOP Mode

On ST638X the hardware watchdog is present and the STOP instruction has been de-activated. Any attempt to execute a STOP will cause the automatic execution of a WAIT instruction.

Exit from WAIT Mode

The following paragraphs describe the output procedure of the ST638X Core from WAIT mode when an interrupt occurs. It must be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non-maskable interrupt mode) before the start of the WAIT sequence, but also of the type of the interrupt request that is generated.

Normal Mode. If the ST638X Core was in the main routine when the WAIT instruction has been executed, the ST638X Core outputs from the wait mode as soon as any interrupt occurs; the related interrupt routine is executed and at the end of the interrupt service routine the instruction that follows the WAIT instruction is executed if no other interrupts are pending.

Non-maskable Interrupt Mode. If the WAIT instruction has been executed during the execution of the non-maskable interrupt routine, the ST638X Core outputs from the wait mode as soon as any interrupt occurs: the instruction that follows the WAIT instruction is executed and the ST638X Core is still in the non-maskable interrupt mode even if an other interrupt has been generated.

Normal Interrupt Mode. If the ST638X Core was in the interrupt mode before the initialization of the WAIT sequence, it outputs from the wait mode as soon as any interrupt occurs. Nevertheless, two cases have to be considered:

- If the interrupt is a normal interrupt, the interrupt routine in which the WAIT was entered will be completed with the execution of the instruction that follows the WAIT and the ST638X Core is still in the interrupt mode. At the end of this routine pending interrupts will be serviced in accordance to their priority.
- If the interrupt is a non-maskable interrupt, the non-maskable routine is processed at first. Then, the routine in which the WAIT was entered

tered will be completed with the execution of the instruction that follows the WAIT and the ST638X Core is still in the normal interrupt mode.

Notes :
If all the interrupt sources are disabled, the restart of the MCU can only be done by a Reset activation. The Wait instruction is not executed if an enabled interrupt request is pending. In the ST638X the hardware activated digital watchdog function is present. As the watchdog is always activated the STOP instruction is de-activated and any attempt to execute the STOP instruction will cause an execution of a WAIT instruction.

ON-CHIP CLOCK OSCILLATOR

The internal oscillator circuit is designed to require a minimum of external components. A crystal quartz, a ceramic resonator, or an external signal (provided to the OSCIN pin) may be used to generate a system clock with various stability/cost tradeoffs. The typical clock frequency is 8MHz. Please note that different frequencies will affect the operation of those peripherals (D/As, SPI, 62.5 KHz OUT) whose reference frequencies are derived from the system clock.

The different clock generator options connection methods are shown in Figure 25, crystal specifications and suggested PC board layouts are given in Figure 26 and Figure 27. One machine cycle takes 13 oscillator pulses; 12 clock pulses are needed to increment the PC while and additional 13th pulse is needed to stabilize the internal latches during memory addressing. This means that with a clock frequency of 8MHz the machine cycle is 1.625µSec.

The crystal oscillator start-up time is a function of many variables: crystal parameters (especially RS), oscillator load capacitance (CL), IC parameters, ambient temperature, and supply voltage.It must be

Table 7. Instructions Timing with 8MHz Clock

Instruction Type	Cycles	Execution Time
Branch if set/reset	5 Cycles	8.125µs
Branch & Subroutine Branch	4 Cycles	6.50µs
Bit Manipulation	4 Cycles	6.50µs
Load Instruction	4 Cycles	6.50µs
Arithmetic & Logic	4 Cycles	6.50µs
Conditional Branch	2 Cycles	3.25µs
Program Control	2 Cycles	3.25µs

Figure 25. Clock Generator Options

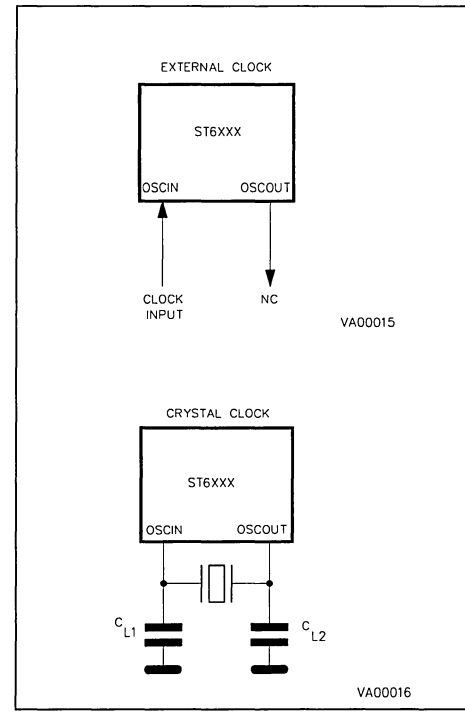
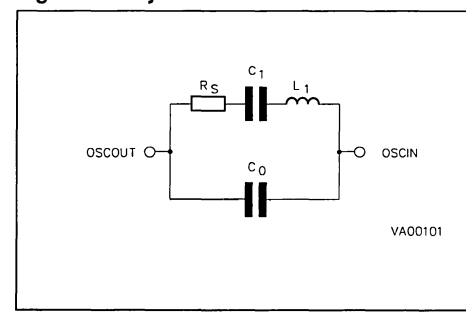


Figure 26. Crystal Parameters



ON-CHIP CLOCK OSCILLATOR (Continued)

Figure 27. PC Board Layouts Examples

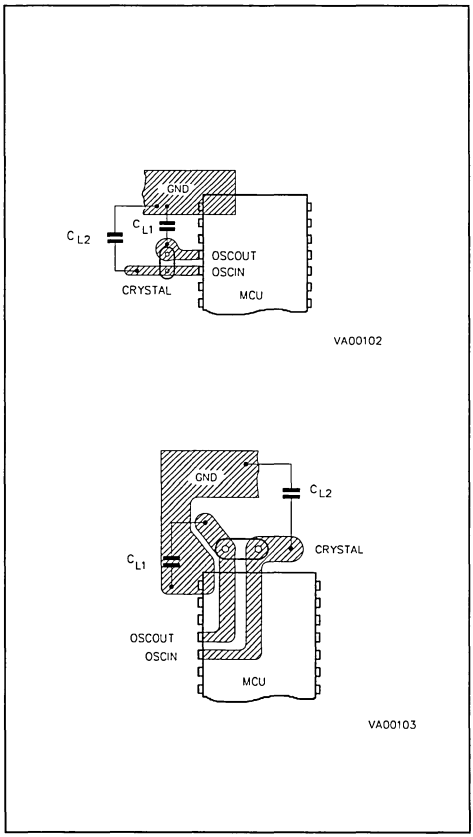
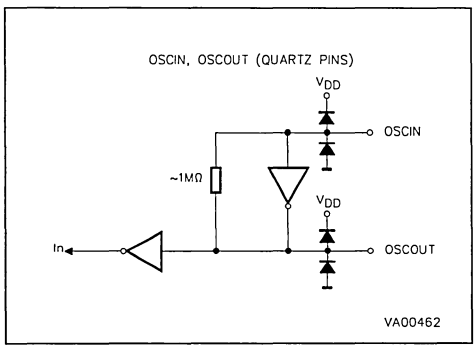


Figure 28. OSCIN, OSCOUT Configuration Diagram



INPUT/OUTPUT PORTS

The ST638X microcontrollers use three standard I/O ports (A,B,C) with up to eight pins on each port; refer to the device pin configurations to see which pins are available.

Each line can be individually programmed either in the input mode or the output mode as follows by software.

- Output
- Input with on-chip pull-up resistor (selected by software)
- Input without on-chip pull-up resistor (selected by software)

Note: pins with 12V open-drain capability do not have pull-up resistors.

In output mode the following hardware configurations are available:

- Open-drain output 12V (PA4-PA7, PC4-PC7)
- Open-drain output 5V (PC0-PC3)
- Push-pull output (PA0-PA3, PB0-PB6)

The lines are organized in three ports (port A,B,C). The ports occupie 6 registers in the data space. Each bit of these registers is associated with a particular line (for instance, the bits 0 of the Port A Data and Direction registers are associated with the PA0 line of Port A).

There are three Data registers (DRA, DRB, DRC), that are used to read the voltage level values of the lines programmed in the input mode, or to write the logic value of the signal to be output on the lines configured in the output mode. The port Data Registers can be read to get the effective logic levels of the pins, but they can be also written by the user software, in conjunction with the related Data Direction Register, to select the different input mode options. Single-bit operations on I/O registers (bit set/reset instructions) are possible but care is necessary because reading in input mode is done from I/O pins and therefore they might be influenced by the external load, while writing will directly affect the Port data register causing an undesired changes of the input configuration. The three Data Direction registers (DDRA, DDRB,DDRB) allow the selection of the direction of each pin (input or output).

All the I/O registers can be read or written as any other RAM location of the data space, so no extra RAM cell is needed for port data storing and manipulation. During the initialization of the MCU, all the I/O registers are cleared and the input mode with pull-up is selected on all the pins thus avoiding pin conflicts (with the exception of PC2 that is set in output mode and is set high ie. high impedence).

INPUT/OUTPUT PORTS (Continued)

Details of I/O Ports

When programmed as an input a pull-up resistor (if available) can be switched active under program control. When programmed as an output the I/O port will operate either in the push-pull mode or the open-drain mode according to the hardware fixed configuration as specified below.

Port A. PA0-PA3 are available as push-pull when outputs. PA4-PA7 are available as open-drain (no push-pull programmability) capable of withstanding 12V (no resistive pull-up in input mode). PA6-PA7 has been specially designed for higher driving capability and are able to sink 25mA with a maximum VOL of 1V.

Port B. All lines are configured as push-pull when outputs.

Port C. PC0-PC3 are available as open-drain capable of withstanding a maximum V_{DD}+ 0.3V. PC4-PC7 are available as open-drain capable of withstanding 12V (no resistive pull-up in input mode). Some lines are also used as I/O buffers for signals coming from the on-chip SPI.

In this case the final signal on the output pin is equivalent to a wired AND with the programmed data output.

If the user needs to use the serial peripheral, the I/O line should be set in output mode while the open-drain configuration is hardware fixed; the corresponding data bit must set to one. If the latched interrupt functions are used (IRIN, PWRIN) then the corresponding pins should be set to input mode.

On ST638X the I/O pins with double or special functions are:

- PC0/SCL (connected to the SPI clock signal)
- PC1/SDA (connected to the SPI data signal)
- PC3/SEN (connected to the SPI enable signal)
- PC4/PWRIN (connected to the PWRIN interrupt latch)
- PC6/IRIN (connected to the IRIN interrupt latch)

All the Port A,B and C I/O lines have Schmitt-trigger input configuration with a typical hysteresis of 1V.

I/O Pin Programming

Each pin can be individually programmed as input or output with different input and output configurations.

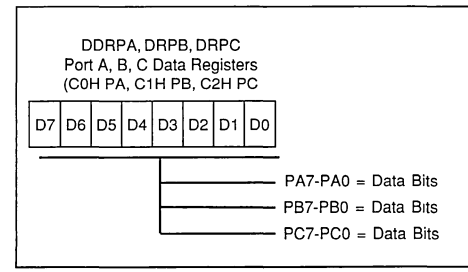
This is achieved by writing to the relevant bit in the data (DR) and data direction register (DDR). Table 8 shows all the port configurations that can be selected by the user software.

Table 8. I/O Port Options Selection

DDR	DR	Mode	Option
0	0	Input	With on-chip pull-up resistor
0	1	Input	Without on-chip pull-up resistor
1	X	Output	Open-drain or Push-Pull

Note: X. Means don't care

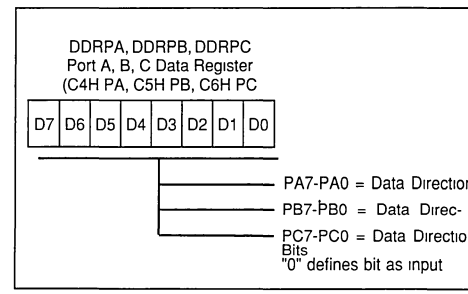
Figure 29. I/O Port Data Registers



PA7-PA0. These are the I/O port A data bits. Reset at power-on.

PB7-PB0. These are the I/O port B data bits. Reset at power-on.

Figure 30. I/O Port Data Direction Registers



PC7-PC0. Set to 04H at power-on. Bit 2 (PC2 pin) is set to one (open drain therefore high impedence).

PA7-PA0. These are the I/O port A data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Reset at power-on.

INPUT/OUTPUT PORTS (Continued)

PB7-PB0. These are the I/O port B data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Reset at power-on.

PC7-PC0. These are the I/O port C data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Set to 04H at power-on. Bit 2 (PC2 pin) is set to one (output mode selected).

Input/Output Configurations

The following schematics show the I/O lines hardware configuration for the different options. Figure 31 shows the I/O configuration for an I/O pin with open-drain 12V capability (standard drive and high drive). Figure 31 shows the I/O configuration for an I/O pin with push-pull and with open drain 5V capability.

Notes :
The WAIT instruction allows the ST638X to be used in situations where low power consumption is needed. This can only be achieved however if the I/O pins either are programmed as inputs with well defined logic levels or have no power consuming resistive loads in output mode. As the same die is used for the different ST638X versions the unavailable I/O lines of ST638X should be programmed in output mode.

Figure 32. I/O Configuration Diagram (Open Drain 12V)

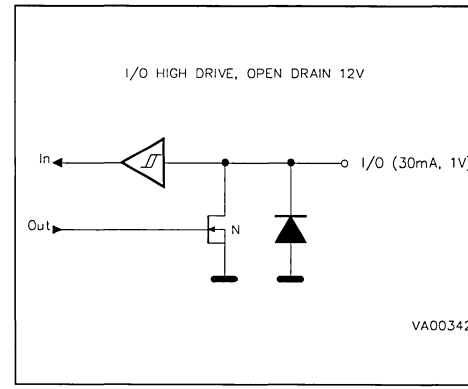
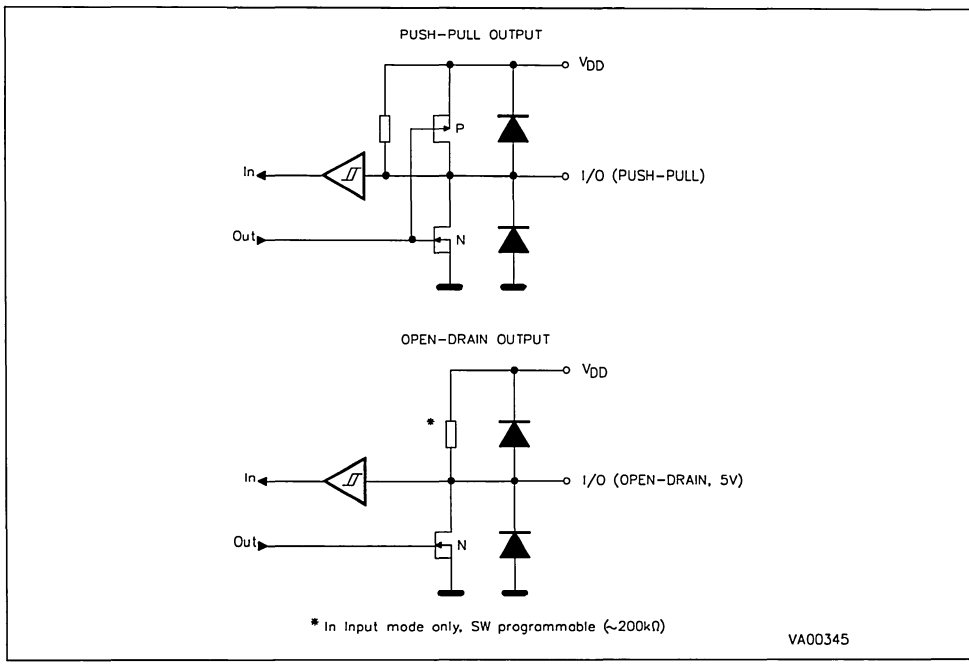


Figure 31. I/O Configuration Diagram (Open Drain 5V, Push-pull)



TIMERS

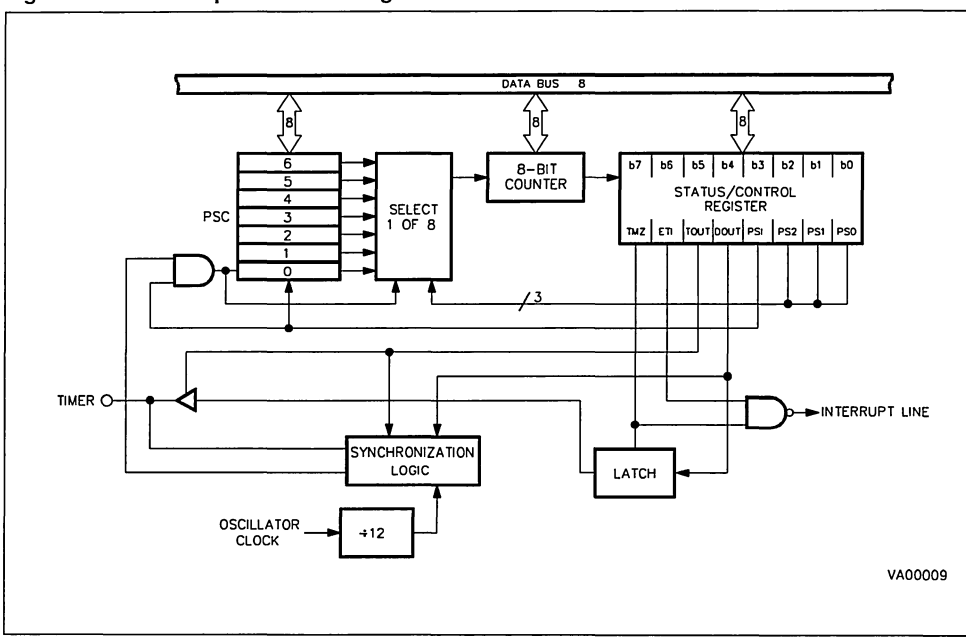
The ST638X devices offer two on-chip Timer peripherals consisting of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes. Figure 33 shows the timer block diagram. This timers do not have the external TIMER pin available for the user. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR that can be addressed in the data space as RAM location at the D3H (Timer 1) and DBH (Timer 2) addresses. The state of the 7-bit prescaler can be read in the PSC register at the D2H (Timer 1) and DAH (Timer 2) addresses. The control logic device can be managed thanks to the TSCR register D4H (Timer 1) and DCH (Timer 2) addresses as it is described in the following paragraphs.

The following description applies to both Timer 1 and Timer 2. The 8-bit counter is decrement by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (timer zero) bit in the TSCR is set to one. If the ETI (enable timer interrupt) bit in the TSCR is also set to one an interrupt request, associated to interrupt vector #3 (for Timer 1) and #1 for Timer 2, is generated. The interrupt of the timer can be used to exit the MCU from the WAIT mode.

The prescaler decrements on rising edge. The prescaler input can be the oscillator frequency divided by 12 or an external clock at TIMER pin (this is not available in ST638X).
Depending on the division factor programmed by PS2/PS1/PS0 (see table 9) bits in the TSCR, the clock input of the timer/counter register is multiplexed to different sources.
On division factor 1, the clock input of the prescaler is also that of timer/counter; on factor 2, bit 0 of prescaler register is connected to the clock input of TCR.

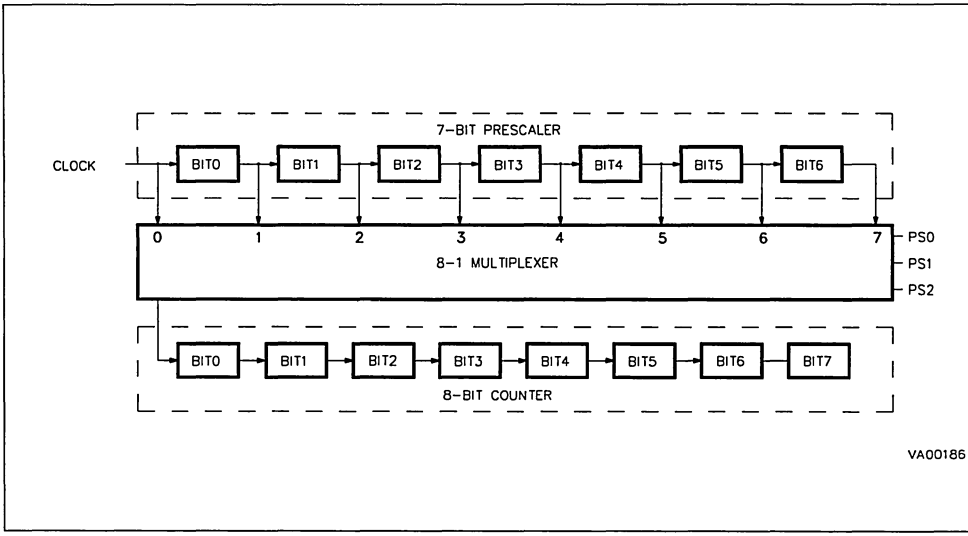
This bit changes its state with the half frequency of prescaler clock input. On factor 4, bit 1 of PSC is connected to clock input of TCR, and so on. On division factor 128, the MSB bit 6 of PSC is connected to clock input of TCR. The prescaler initialize bit (PSI) in the TSCR register must be set to one to allow the prescaler (and hence the counter) to start. If it is cleared to zero then all of the prescaler bits are set to one and the counter is inhibited from counting.

Figure 33. Timer Peripheral Block Diagram



TIMERS (Continued)

Figure 34. Timer Working Principle



The prescaler can be given any value between 0 and 7FH by writing to the related register address, if bit PSI in the TSCR register is set to one. The tap of the prescaler is selected using the PS2/PS1/PS0 bits in the control register. Figure 34 shows the timer working principle.

Timer Operating Modes

As on ST638X devices the external TIMER pin is not available the only allowed operating mode is the output mode that have to be selected by setting to 1 bit 4 and by clearing to 0 bit 5 in the TSCR1 register. This procedure will enable both Timer 1 and Timer 2. Any other combination written into these two bits will disable any Timer 1 and Timer 2 operation.

Output Mode (TSCR1 D4 = 1, TSCR1 D5 = 0). On this mode the timer prescaler is clocked by the prescaler clock input (OSC/12). The user can select the desired prescaler division ratio through the PS2/PS1/PS0 bits. When TCR count reaches 0, it sets the TMZ bit in the TSCR.

The TMZ bit can be tested under program control to perform a timer function whenever it goes high. Bit D4 and D5 on TSCR2 (Timer 2) register are not implemented.

Timer Interrupt

When the counter register decrements to zero and the software controlled ETI (enable timer interrupt) bit is set to one then an interrupt request associated to interrupt vector #3 (for Timer 1) and to interrupt vector #1 (for Timer 2) is generated. When the counter decrements to zero also the TMZ bit in the TSCR register is set to one.

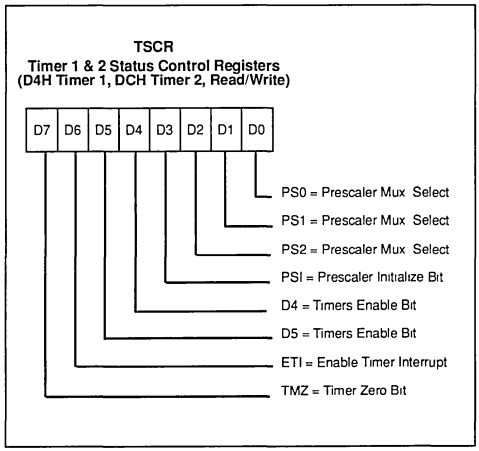
Notes :
TMZ is set when the counter reaches 00H ; however, it may be set by writing 00H in the TCR register or setting the bit 7 of the TSCR register. TMZ bit must be cleared by user software when servicing the timer interrupt to avoid undesired interrupts when leaving the interrupt service routine. After reset, the 8-bit counter register is loaded to FFH while the 7-bit prescaler is loaded to 7FH , and the TSCR register is cleared which means that timer is stopped (PSI=0) and timer interrupt disabled.

A write to the TCR register will predominate over the 8-bit counter decrement to 00H function, i.e. if a write and a TCR register decrement to 00H occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter reaches 00H again. The values of the TCR and the PSC registers can be read accurately at any time.

TIMERS (Continued)

Timer Registers

Figure 35. Timer Status Control Registers



TMZ. Low-to-high transition indicates that the timer count register has decrement to zero. This bit must be cleared by user software before to start with a new count.

ETI. This bit, when set, enables the timer interrupt (vector #3 for Timer 1, vector #1 for Timer 2) request. If ETI=0 the timer interrupt is disabled. If ETI= 1 and TMZ= 1 an interrupt request is generated.

D5. This is the timers enable bit D5. It must be cleared to 0 together with a set to 1 of bit D4 to enable both Timer 1 and Timer 2 functions. It is not implemented on TSCR2 register. Any other combination of TSCR1 D4 and D5 bits will disable any operation of both Timer 1 and Timer 2.

D4. This is the timers enable bit D4. It must be set to 1 together with a clear to 0 of bit D5 to enable both Timer 1 and Timer 2 functions. It is not implemented on TSCR2 register. Any other combination of TSCR1 D4 and D5 bits will disable any operation of both Timer 1 and Timer 2.

PSI. Used to initialize the prescaler and inhibit its counting while PSI = 0 the prescaler is set to 7FH and the counter is inhibited. When PSI = 1 the prescaler is enabled to count downwards. As long as PSI= 0 both counter and prescaler are not running.

PS2-PS0. These bits select the division ratio of the prescaler register. (see table 9)

The TSCR1 and TSCR2 registers are cleared on reset. The correct D4-D5 combination must be written in TSCR1 by user's software to enable the operation of Timer 1 and Timer 2.

Table 9. Prescaler Division Factors

PS2	PS1	PS0	Divided By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Figure 36. Timer Counter Registers

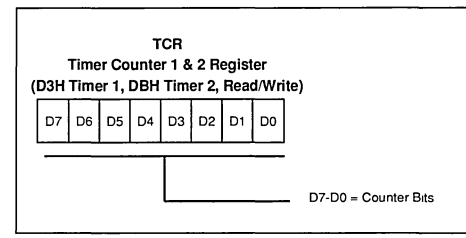
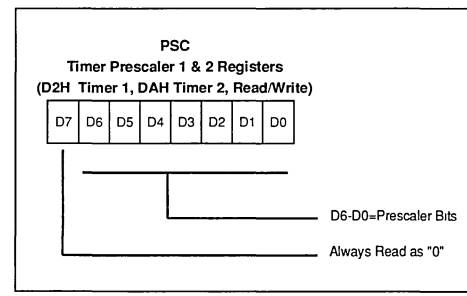


Figure 37. Prescaler Registers



HARDWARE ACTIVATED DIGITAL WATCHDOG FUNCTION

The hardware activated digital watchdog function consists of a down counter that is automatically initialized after reset so that this function does not need to be activated by the user program. As the watchdog function is always activated this down counter can't be used as a timer. The watchdog is using one data space register (HWDR location D8H). The watchdog register is set to FEH on reset and immediately starts to count down, requiring no software start. Similarly the hardware activated watchdog can not be stopped or delayed by software.

The watchdog time can be programmed using the 6 MSbits in the watchdog register, this gives the possibility to generate a reset in a time between 3072 to 196608 oscillator cycles in 64 possible steps. (With a clock frequency of 8MHz this means from 384µs to 24.576ms). The reset is prevented if the register is reloaded with the desired value before bits 2-7 decrement from all zeros to all ones.

The presence of the hardware watchdog deactivates the STOP instruction and a WAIT instruction is automatically executed instead of a STOP. Bit 1 of the watchdog register (set to one at reset) can be used to generate a software reset if cleared to zero). Figure 38 shows the watchdog block diagram while Figure 39 shows its working principle.

Figure 39. Hardware Activated Watchdog Working Principle

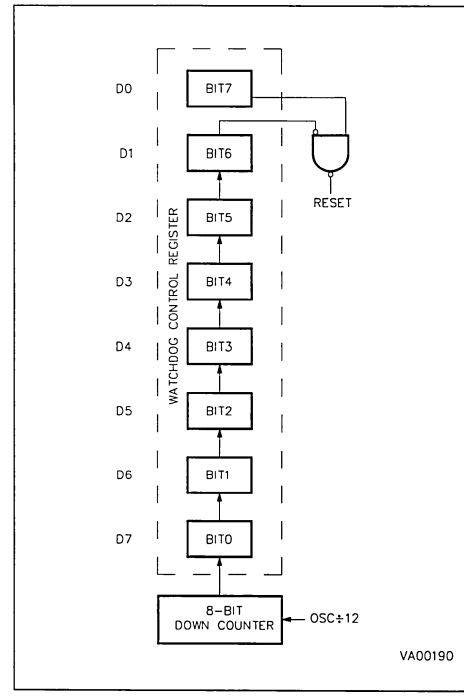
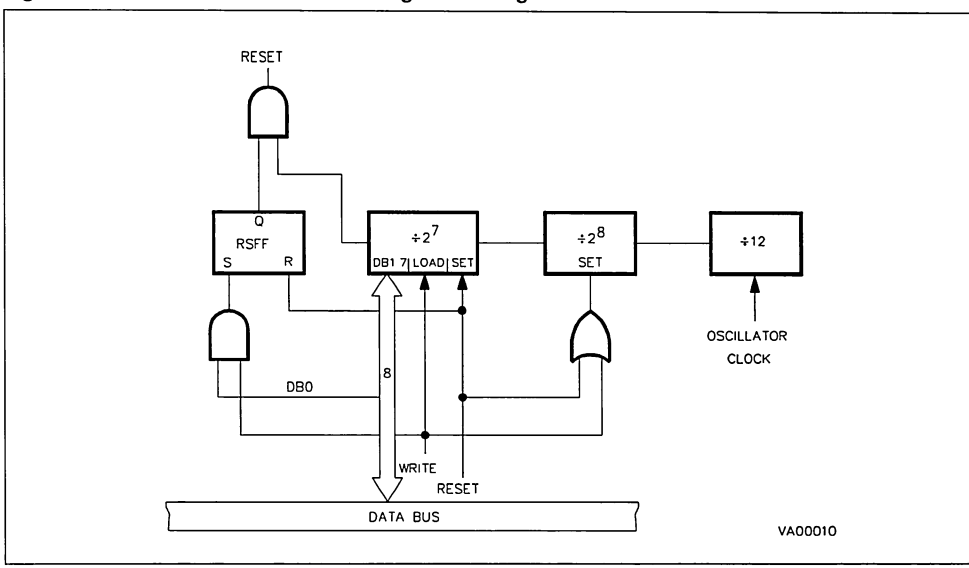
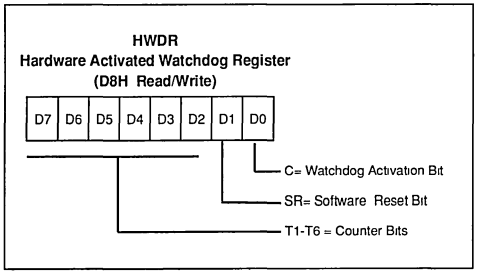


Figure 38. Hardware Activated Watchdog Block Diagram



HARDWARE ACTIVATED DIGITAL WATCHDOG FUNCTION (Continued)

Figure 40. Watchdog Register



T1-T6. These are the watchdog counter bits. It should be noted that D7 (T1) is the LSB of the counter and D2 (T6) is the MSB of the counter, these bits are in the opposite order to normal.

SR. This bit is set to one during the reset phase and will generate a software reset if cleared to zero.

C. This is the watchdog activation bit that is hardware set to one; the user can't change the value of this bit (the watchdog is always active).

The register reset value is FEH (Bit 1-7 set to one, Bit 0 cleared).

SERIAL PERIPHERAL INTERFACE

The ST638X Serial Peripheral Interface macrocell (SPI) has been designed to be cost effective and flexible in interfacing the various peripherals in TV applications.

It maintains the software flexibility but adds hardware configurations suitable to drive devices which require a fast exchange of data. The three pins dedicated for serial data transfer (single master only) can operate in the following ways:

- as standard I/O lines (software configuration)
- as S-BUS or as I^2CBUS (two pins)
- as standard (shift register) SPI

When using the hardware SPI, a fixed clock rate of 62.5kHz is provided.

It has to be noted that the first bit that is output on the data line by the 8-bit shift register is the MSB.

SPI Data/Control Registers

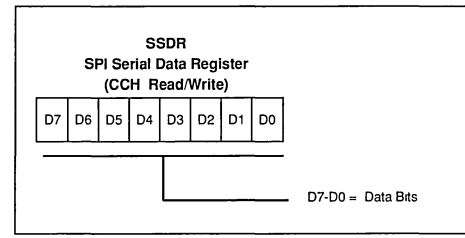
For I/O details on SCL (Serial Clock), SDA (Serial Data) and SEN (Serial Enable) please refer to I/O Ports description with reference to the following registers:

Port C data register, Address C2H (Read/Write).

- BIT D0 "SCL"
- BIT D1 "SDA"
- BIT D3 "SEN"

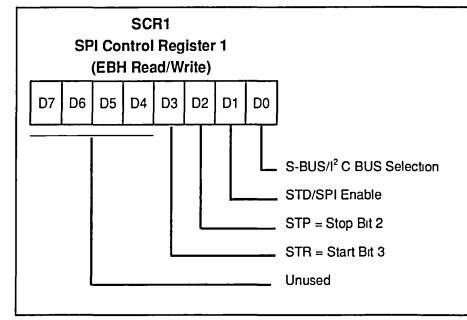
Port C data direction register, Address C6H (Read/Write).

Figure 41. SPI Serial Data Register



D7-D0. These are the SPI data bits. They can be neither read nor written when SPI is operating (BUSY bit set). They are undefined after reset.

Figure 42. SPI Control Register 1



D7-D4. These bits are not used.

STR. This is Start bit for $I^2CBUS/S-BUS$. This bit is meaningless when STD/SPI enable bit is cleared to zero. If this bit is set to one STD/SPI bit is also set to "1" and SPI Start generation, before beginning of transmission, is enabled. Set to zero after reset.

STP. This is Stop bit for $I^2CBUS/S-BUS$. This bit is meaningless when STD/SPI enable bit is cleared to zero. If this bit is set to one STD/SPI bit is also set to "1" and SPI Stop condition generation is enabled. STP bit must be reset when standard protocol is used (this is also the default reset conditions). Set to zero after reset.

STD, SPI Enable. This bit, in conjunction with S-BUS/I^2CBUS bit, allows the SPI disable and will select between $I^2CBUS/S-BUS$ and Standard

SERIAL PERIPHERAL INTERFACE (Continued)

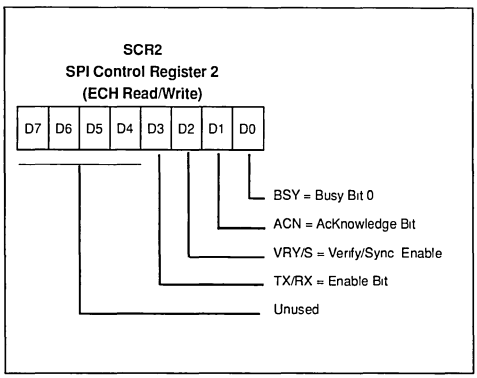
shift register protocols. If this bit is set to one, it selects both I²CBUS and S-BUS protocols; final selection between them is made by S-BUS/I²CBUS bit. If this bit is cleared to zero when S-BUS/I²CBUS is set to "1" the Standard shift register protocol is selected. If this bit is cleared to "0" when S-BUS/I²CBUS is cleared to 0 the SPI is disabled. Set to zero after reset.

S-BUS/I²CBUS Selection. This bit, in conjunction with STD/SPI bit, allows the SPI disable and will select between I²CBUS and S-BUS protocols. If this bit is cleared to "0" when STD bit is also "0", the SPI interface is disabled. If this bit is cleared to zero when STD bit is set to "1", the I²CBUS protocol will be selected. If this bit is set to one when STD bit is set to "1", the S-BUS protocol will be selected. Cleared to zero after reset.

Table 10. SPI Modes Selection

D0 S-BUS/I²CBUS	D1 STD/SPI	SPI Function
0	0	Disabled
1	0	STD Shift Register
0	1	I²CBUS
1	1	S-BUS

Figure 43. SPI Control Register 2



D7-D4. These bits are not used.

TX/RX. *Write Only.* When this bit is set, current byte operation is a transmission. When it is reset, current operation is a reception. Set to zero after reset.

VRY/S. *Read Only/Write Only.* This bit has two different functions in relation to read or write operation. *Reading Operation:* when STD and/or TRX bits are cleared to 0, this bit is meaningless. When bits STD and TX are set to 1, this bit is set each time BSY bit is set. This bit is reset during byte operation if real data on SDA line are different from the ones output from the shift register. Set to zero after reset. *Writing Operation* : it enables (if set to one) or disables (if cleared to zero) the interrupt coming from VSYNC pin. Undefined after reset. Refer to OSD description for additional information.

ACN. *Read Only.* If STD bit (D1 of SCR1 register) is cleared to zero this bit is meaningless. When STD is set to one, this bit is set to one if no Acknowledge has been received. In this case it is automatically reset when BSY is set again. Set to zero after reset.

BSY. *Read/Set Only.* This is the busy bit zero. When a one is loaded into this bit the SPI interface start the transmission of the data byte loaded into SSDR data register or receiving and building the receive data into the SSDR data register. This is done in accordance with protocol, direction and start/stop condition(s). This bit is automatically cleared at the end of the current byte operation. Cleared to zero after reset.

Note :
The SPI shift register is also the data transmission register and the data received register; this new feature is made possible by using the serial structure of the ST638X and thus reducing size and complexity.

During transmission or reception of data, all access to serial data register is therefore disabled. The reception or transmission of data is started by setting the BUSY bit to "1"; this will be automatically reset at the end of the operation. After reset, the busy bit is cleared to "0", and the hardware SPI disabled by clearing bit 0 and bit 1 of SPI control register 1 to "0". The outputs from the harware SPI are "ANDed" to the standard I/O software controlled outputs. If the hardware SPI is in operation then Port C ouputs related to the SPI should be set high or the pins should pin configured as inpus using the data direction register. When the SPI is configured as the S-BUS, the three pins PC0, PC1 and PC3 become the pins SCL, SDA and SEN respectively. When configured as the I²CBUS the pins PC0 and PC1 are configured as the pins SCL and SDA; PC3 is not driven and can be used as general purpose I/O pin. In the case of the STDSPI the pins PC0 and PC1 become the signals CLOCK and DATA, PC3 is not driven and can be used as general purpose I/O pin. The VERIFY bit is available when the SPI is configured as either S-BUS or I²CBUS. At the start of a byte transmission, the verify bit is set to one. If at any time during the transmission of the following eight bits, the data on the SDA line does not match the data forced by the SPI (while SCL is

SERIAL PERIPHERAL INTERFACE (Continued)

high), then the VERIFY bit is reset. The verify is available only during transmission for the S-BUS and I²CBUS; for other protocol it is not definfited. The SDA and SCL signal entering the SPI are buffered in order to remove any minor glitches. When STD bit is set to one (S-BUS or I²CBUS selected), and TRX bit is reset (receiving data), and STOP bit is set (last byte of current communication), the SPI interface does not generate the Acknowledge, according to S-BUS/I²CBUS specifications. PCO-SCL, PC1-SDA and PC3-SEN lines are standard drive I/O port pins with open-drain output configuration (maximum voltage that can be applied to these pins is V_{DD}+ 0.3V).

S-BUS/I²CBUS Protocol Information

The S-BUS is a three-wire bidirectional data-bus with functional features similar to the I²CBUS. In fact the S-BUS includes decoding of Start/Stop conditions and the arbitration procedure in case of multimaster system configuration (the ST638X SPI allows a single-master only operation). The SDA line, in the I²CBUS represents the AND combination of SDA and SEN lines in the S-BUS. If the SDA and the SEN lines are short-circuit connected, they appear as the SDA line of the I²CBUS. The Start/Stop conditions are detected (by the external peripherals suited to work with S-BUS/I²CBUS) in the following way:

- On S-BUS by a transition of the SEN line (1 to 0 Start, 0 to 1 Stop) while the SCL line is at high level.
- On I²CBUS by a transition of the SDA line (10 Start, 01Stop) while the SCL line is at high level.

Start and Stop condition are always generated by the master (ST638X SPI can only work as single master). The bus is busy after the start condition and can be considered again free only when a certain time delay is left after the stop condition. In the S-BUS configuration the SDA line is only allowed to change during the time SCL line is low. After the start information the SEN line returns to high level and remains unchanged for all the data transmission time. When the transmission is completed the SDA line is set to high level and, at the same time, the SEN line returns to the low level in order to supply the stop information with a low to high transition, while the SCL line is at high level. On the S-BUS, as on the I²CBUS, each eight bit information (byte) is followed by one acknowledged bit which is a high level put on the SDA line by the transmitter. A peripheral that acknowledges has to pull down the SDA line during the acknowledge clock pulse. An addressed receiver has to generate an acknowledge after the reception of each byte; otherwise the SDA line remains at the high level during the ninth clock pulse time. In this case the master transmitter can generate the Stop condition, via the SEN (or SDA in I²CBUS) line, in order to abort the transfer.

Start/Stop Acknowledge. The timing specs of the S-BUS protocol require that data on the SDA (only on this line for I²CBUS) and SEN lines be stable during the "high" time of SCL. Two exceptions to this rule are foreseen and they are used to signal the start and stop condition of data transfer.

- On S-BUS by a transition of the SEN line (10 Start, 01 Stop) while the SCL line is at high level.
- On I²CBUS by a transition of the SDA line (10 Start, 01 Stop) while the SCL line is at high level.

Data are transmitted in 8-bit groups; after each group, a ninth bit is interposed, with the purpose of acknowledging the transmitting sequence (the transmit device place a "1" on the bus, the acknowledging receiver a "0").

Interface Protocol. This paragraph deals with the description of data protocol structure. The interface protocol includes:

- A start condition
- A "slave chip address" byte, transmitted by the master, containing two different information:

a. the code identifying the device the master wants to address (this information is present in the first seven bits)

b. the direction of transmission on the bus (this information is given in the 8th bit of the byte); "0" means "Write", that is from the master to the slave, while "1" means "Read". The addressed slave must always acknowledge.

The sequence from, now on, is different according to the value of R/$\overline{W}$ bit.

1. R/$\overline{W}$ = "0" ($\overline{\text{Write}}$)

In all the following bytes the master acts as transmitter; the sequence follows with:

a. an optional data byte to address (if needed) the slave location to be written (it can be a word address in a memory or a register address, etc.).

b. a "data" byte which will be written at the address given in the previous byte.

c. further data bytes.

d. a STOP condition

A data transfer is always terminated by a stop condition generated from the master. The ST638X peripheral must finish with a stop condition before another start is given. Figure 44 shows an example of write operation.

2. R/$\overline{W}$ = "1" (Read)

In this case the slave acts as transmitter and, therefore, the transmission direction is changed. In read mode two different conditions can be considered:

SERIAL PERIPHERAL INTERFACE (Continued)

a. The master reads slave immediately after first byte. In this case after the slave address sent from the master with read condition enabled the master transmitter becomes master receiver and the slave receiver becomes slave transmitter.

b. The master reads a specified register or location of the slave. In this case the first sent byte will contain the slave address with write condition enabled, then the second byte will specify the address of the register to be read. At this moment a new start is given together with the slave address in read mode and the procedure will proceed as described in previous point "a".

Figure 44. Master Transmit to Slave Receiver (Write Mode)

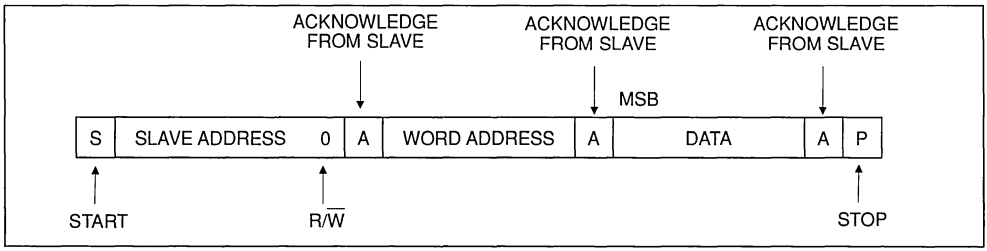


Figure 45. Master Reads Slave Immediately After First Byte (read Mode)

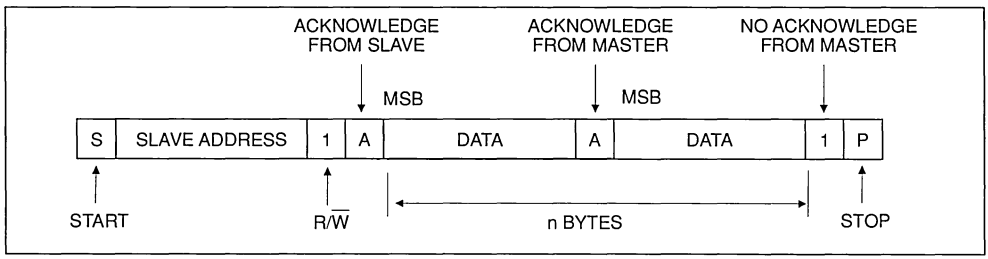
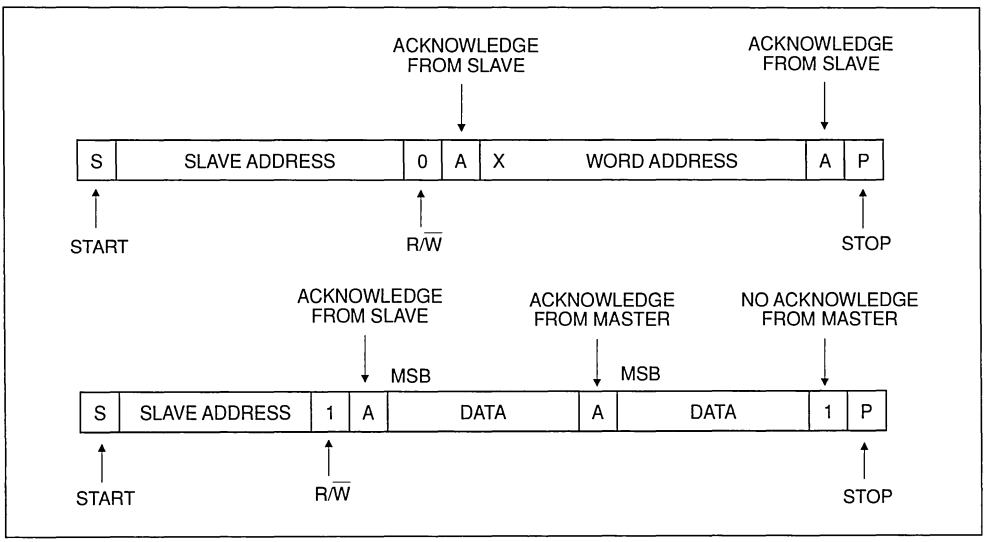


Figure 46. Master Reads After Setting Slave Register Address (Write Address, Read Data)

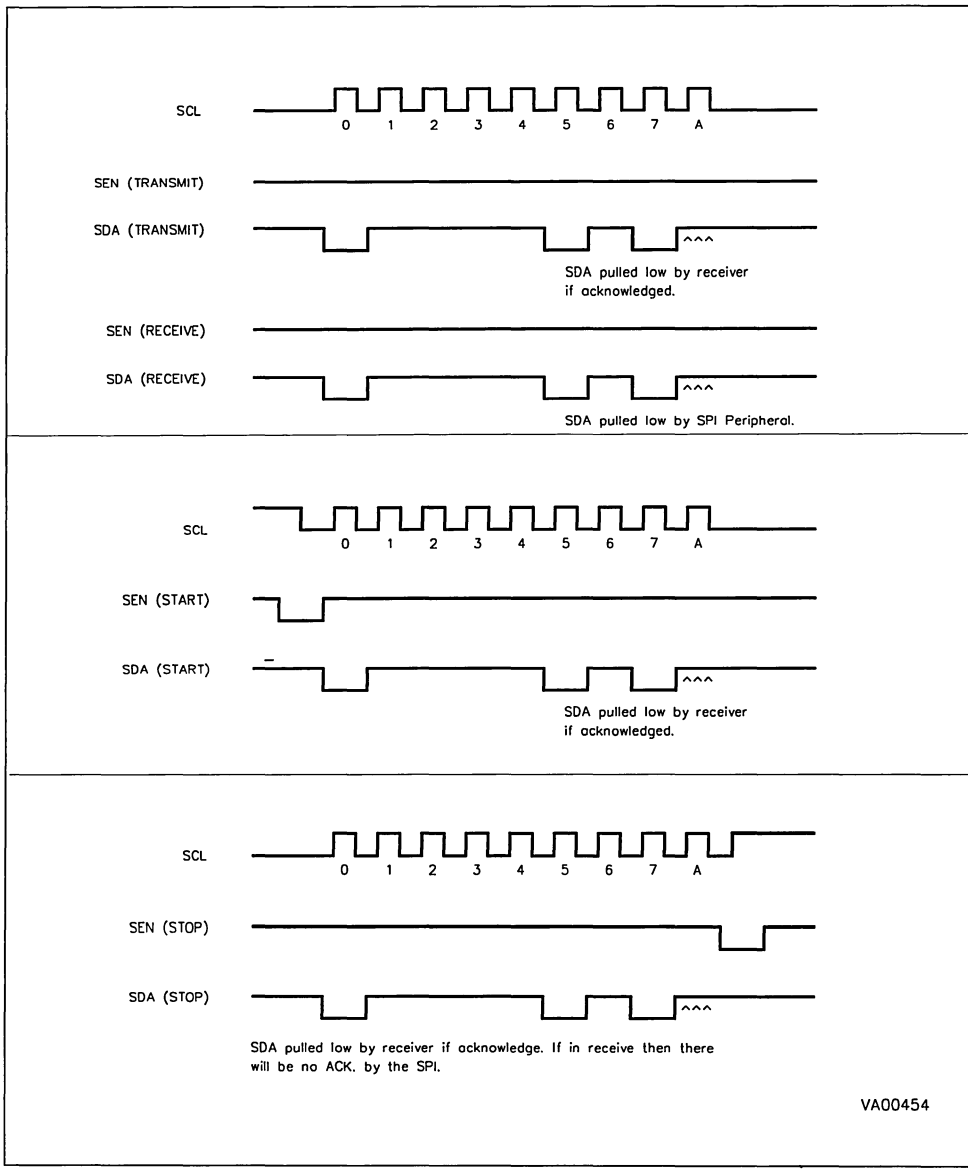


SERIAL PERIPHERAL INTERFACE (Continued)

S-BUS/I²CBUS Timing Diagrams

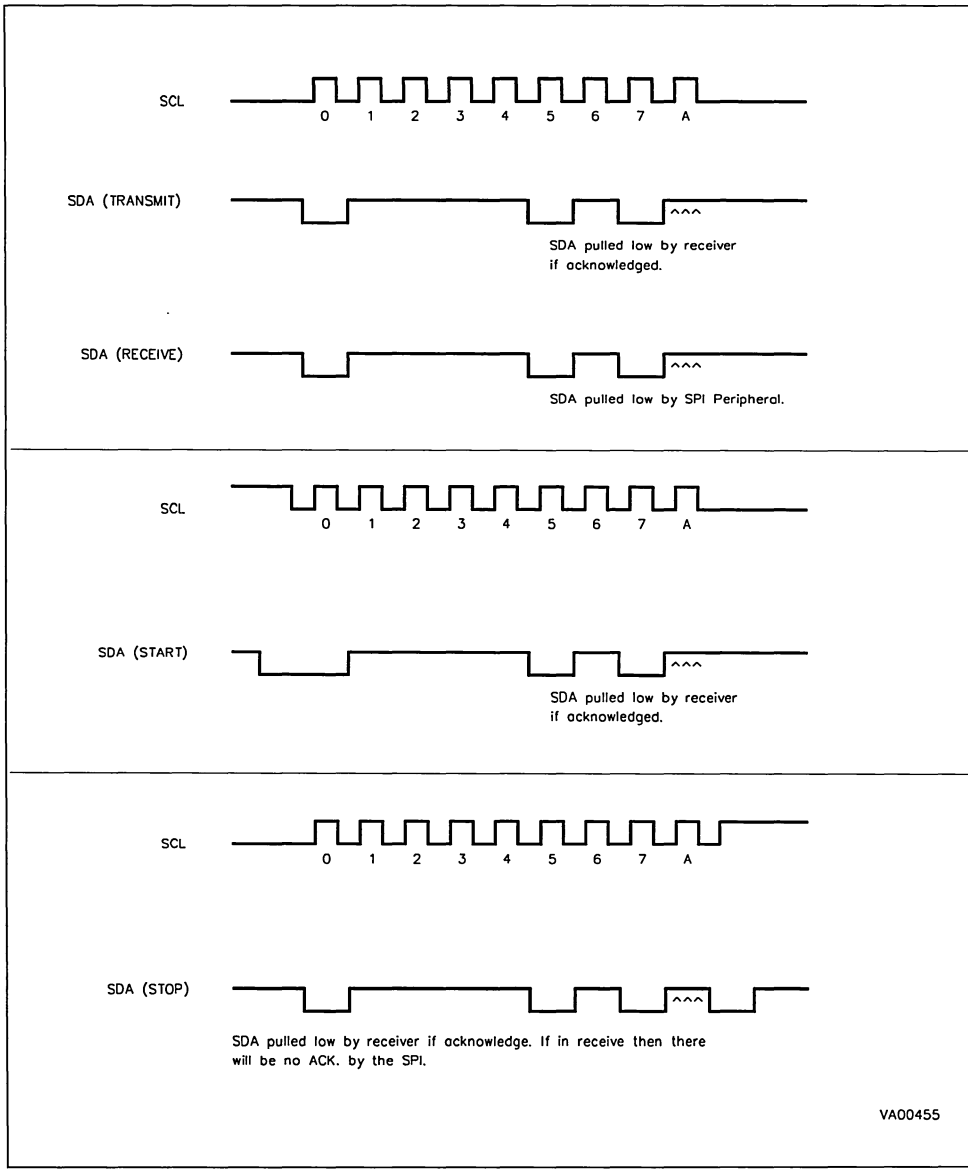
The clock of the S-BUS/I²CBUS of the ST638X SPI (single master only) has a fixed bus clock frequency of 62.5KHz. All the devices connected to the bus must be able to follow transfers with frequencies up to 62.5KHz, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure which will force the master into a wait state and stretch low periods.

Figure 47. S-BUS Timing Diagrams



SERIAL PERIPHERAL INTERFACE (Continued)

Figure 48. I²C BUS Timing Diagrams



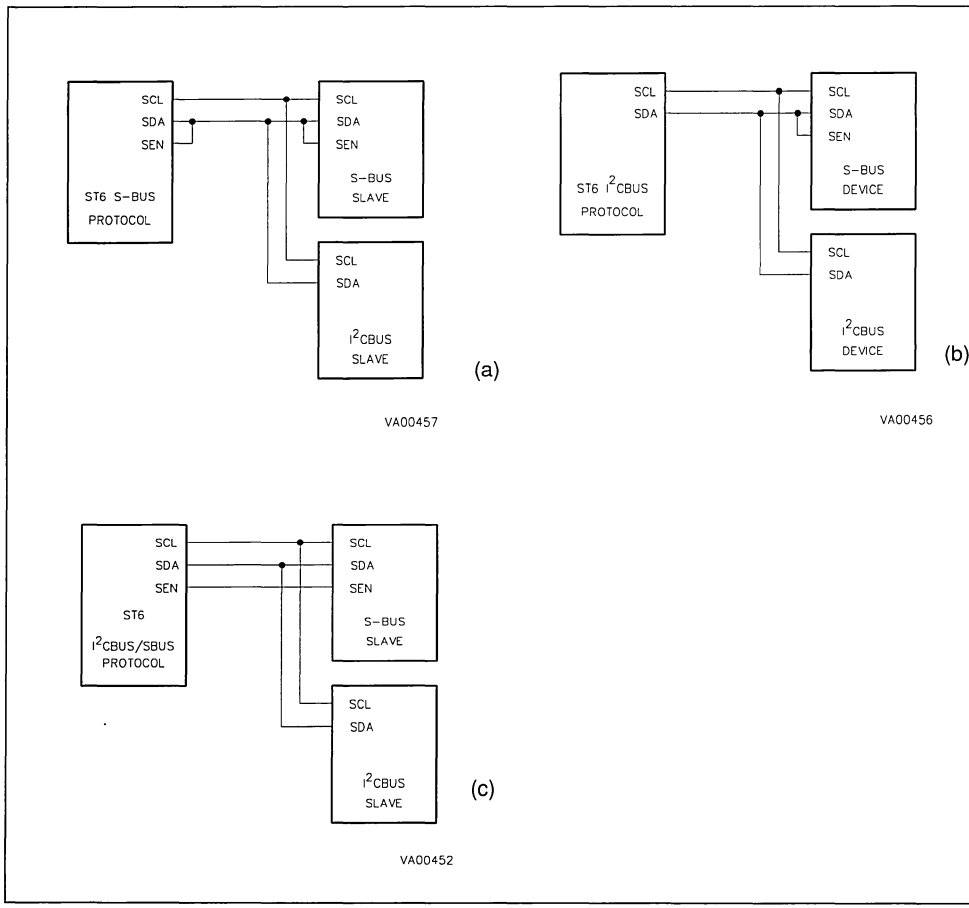
Note: The third pin, SEN, should be high; it's not used in the I²CBUS. Logically SDA is the AND of the S-BUS SDA and SEN.)

SERIAL PERIPHERAL INTERFACE (Continued)

Compatibility S-BUS/I²CBUS

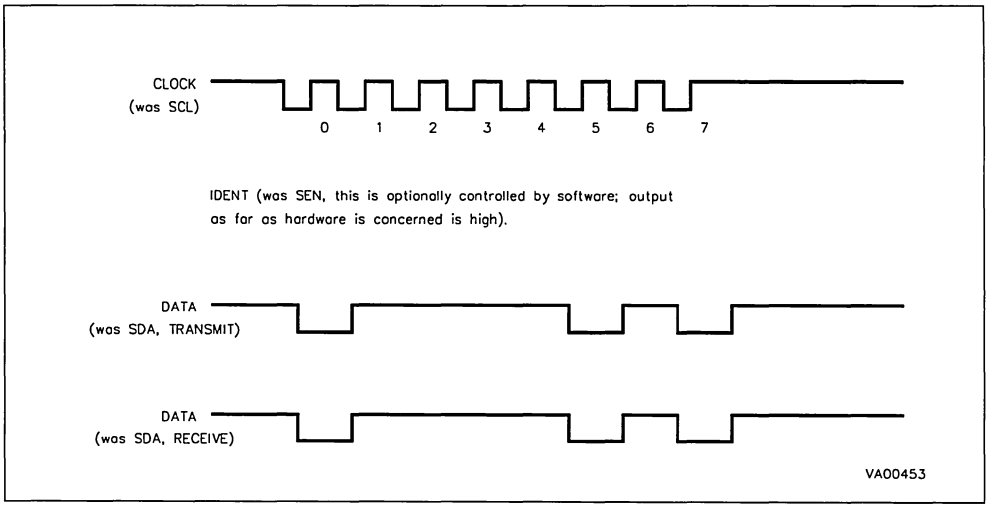
Using S-BUS protocol it is possible to implement mixed system including S-BUS/I²CBUS bus peripherals. In order to have the compatibility with the I²CBUS peripherals, the devices including the S-BUS interface must have their SDA and SEN pins connected together as shown in the following Figure 49 (a and b). It is also possible to use mixed S-BUS/I²CBUS protocols as showed in figure 49 (c). S-BUS peripherals will only react to S-BUS protocol signals, while I²CBUS peripherals will only react to I²CBUS signals. Multimaster configuration is not possible with ST63XX SPI (single master only).

Figure 49. S-BUS/I²C BUS Mixed Configurations



SERIAL PERIPHERAL INTERFACE (Continued)

Figure 50. Software Bus (hardware bus disabled) Timing Diagram



STD SPI Protocol (Shift Register)

This protocol is similar to the I²CBUS with the exception that there is no acknowledge pulse and there are no stop or start bits. The clock cannot be slowed down by the external peripherals.

In this case all three outputs should be high in order not to lock the software I/Os from functioning.

SPI APPLICATION NOTES

Stop Clock Slowdown: In the ST638X family of devices when operating in the I²C or SBUS modes, there is no internal clock slowdown for the final STOP clock. Slowdown means that if an external peripheral requires extra time it will hold the ST638X SCL clock low. To be fully I²C and SBUS compatible in this respect, the SW should check that the SCL line is indeed high before proceeding with the START of another I²C or SBUS transmission. In all other cases the SCL clock slowdown feature is operational.

SPI Standard Bus Protocol: The standard bus protocol is selected by loading the SPI Control Register 1 (SCR1 Add. EBH). Bit 0 named I²C must be set at one and bit 1 named STD must be reset. When the standard bus protocol is selected bit 2 of the SCR1 is meaningless.
This bit named STOP bit is used only in I²CBUS or SBUS. However take care that the *STOP BIT MUST BE RESET WHEN THE STANDARD PROTOCOL IS USED.* This bit is set to ZERO after RESET.

14-BIT VOLTAGE SYNTHESIS TUNING PERIPHERAL

The ST638X on-chip voltage synthesis tuning peripheral has been integrated to allow the generation of tuning reference voltage in low/mid end TV set applications. The peripheral is composed of a 14-bit counter that allows the conversion of the digital content in a tuning voltage, available at the VS output pin, by using PWM and BRM techniques. The 14-bit counter gives 16384 steps which allows a resolution of approximately 2mV over a tuning voltage of 32V ; this corresponds to a tuning resolution of about 40KHz per step in UHF band (the actual value will depend on the characteristics of the tuner).

The tuning word consists of a 14-bit word contained in the registers VSDATA1 (location 0EEH) and VSDATA2 (location 0EFH). Course tuning (PWM) is performed using the seven MSBit, while the fine tuning (BRM) is performed using the data in the seven LSBIT. With all zeros loaded the output is zero ; as the tuning voltage increseses from all zeros, the number of pulses in one period increses to 128 with all pulses being the same width. For values larger than 18, the PWM takes over and the number of pulses in one period remains constant at 128, but the width changes. At the other end of the scale, when almost all ones are loaded, the pulses will start to link together and the number of pulses will decrease. When all ones are loaded, the output will be almost 100% high but will have a low pulse (1/16384 of the high pulse).

Output Details

Inside the on-chip Voltage Synthesis cell are included the register latches, a reference counter, PWM and BRM control circuitry ; the structure is one used in many devices currenlty in production from SGS-THOMSON (M106, M193, M293, M490/91/94). In the ST638X the clock for the 14-bit reference counter is 2MHz derived from the 8MHz system clock. From the circuit point of view, the seven most significant bits controls the course tuning, while the seven least significant bits the fine tuning. From the application and software point of view, the 14 bits can be considered as one binary number.

As already mentioned the course tuning consists of a PWM signal with 128 steps ; we can consider the dine tuning to cover 128 course tuning cycles. The addition of pulses is described in the following Table 11.

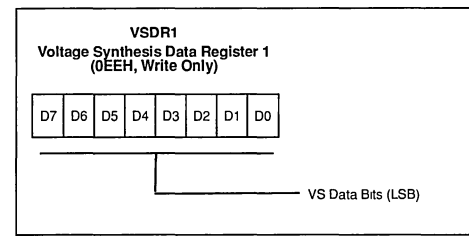
Table 11. Fine Tuning Pulse Addition

Fine Tuning (7 LSB)	N° of Pulses added at the following cycles (0...127)
0000001	64
0000010	32, 96
0000100	16, 48, 80, 112
0001000	8, 24, ...104, 120
0010000	4, 12, ...116, 124
0100000	2, 6, ...122, 126
1000000	1, 3, ...125, 127

The VS output pin has a standard drive push-pull output configuration.

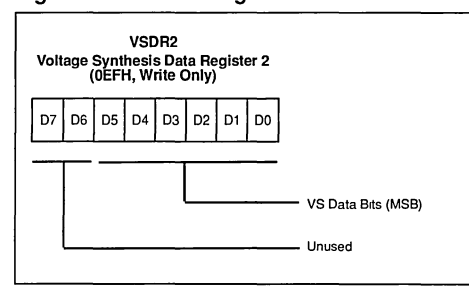
VS Tuning Cell Registers

Figure 51. VS Data Register 1



D7-D0. These are the 8 least significant VS data bits. Bit 0 is the LSB. This register is undefined on reset.

Figure 52. VS Data Register 2



D7-D6. These bits are not used.

D5-D0. These are the 6 most significant VS data bits. Bit 5 is the MSB. This register is undefined on reset.

6-BIT PWM D/A CONVERTERS

The D/A macrocell contains up to six PWM D/A outputs (32Khz repetition, DA0-DA5) with six bit resolution .

Each D/A converter of ST638X is composed by the following main blocks:

- pre-divider
- 6-bit counter
- data latches and compare circuits

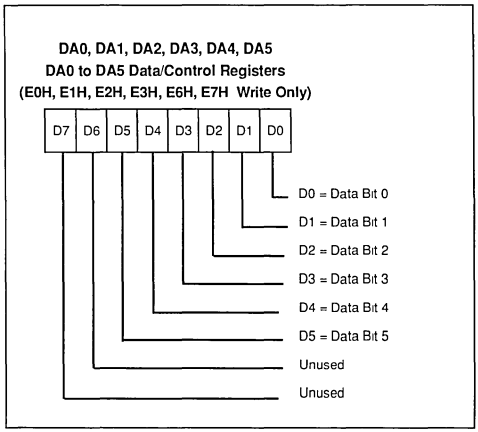
The pre-divider uses the clock input frequency (8MHz typical) and its output clocks the 6-bit free-running counter. The data latched in the six registers (E0H, E1H, E2H, E3H, E6H and E7H) control the six D/A outputs (DA0,1,2, 3, 4 and 5). When all zeros are loaded the relevant output is an high logic level; all 1's correspond to a pulse with a 1/64 duty cycle and almost 100% zero level.

The repetition frequency is 31.25KHz and is related to the 8MHz clock frequency. Use of a different oscillator frequency will result in wrong repetition frequency. All D/A outputs are open-drain with standard current drive capability and able to withstand up to 12V.

D/A Data/Control Registers

This paragraph deals with the description of D/A data/control registers.

Figure 54. DA0-DA5 Data Control Registers



D7, D6. These bits are not used.

DA0-DA5. These are the 6 bits of the PWM digital to analog converter . Undefined after reset.

AFC A/D INPUT, IR/PC6 RESULT, VSYNC RESULT AND 62.5KHz OUTPUTS

The AFC macrocell contains an A/D comparator with five levels at intervals of 1V from 1V to 5V. The levels can all be lowered by 0.5V to effectively double the resolution. This A/D can be used to perform the AFC function. In addition this cell offers also a keyboard input register of three bits used to perform a keyboard scan and 4 open-drain outputs (able to withstand signals up to 12V) that can be used to perform band switch function.

Figure 53. 6-BIT PWM D/A Output Configuration

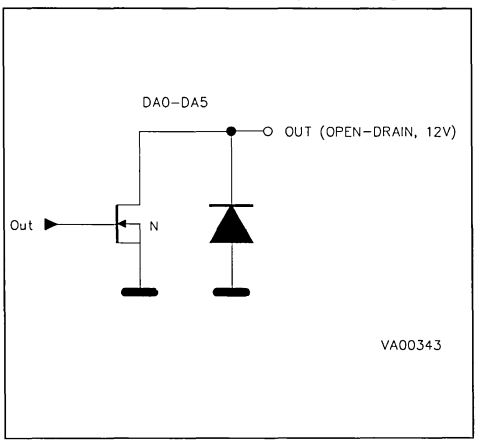
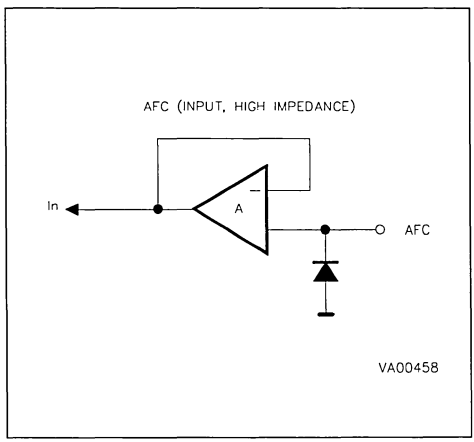


Figure 55. AFC Inputs Configuration Diagram



AFC A/D INPUT, IR/PC6 RESULT, VSYNC RESULT, AND 62.5KHz OUTPUT (Continued)

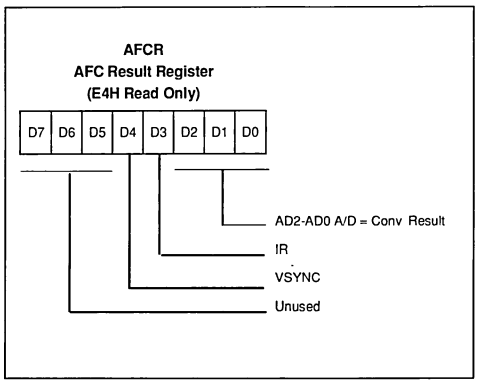
A/D Comparator

The A/D used to perform the AFC function (when high threshold is selected) has the following voltage levels: 1,2,3,4 and 5V. Bits 0-2 of AFC result register (E4H address) will provide the result in binary form (less than 1V is 000, greater than 5V is 101).

If the application requires a greater resolution, the sensitivity can be doubled by clearing to zero bit 2 of the OUTPUTS control register, address E5H. In this case all levels are shifted lower by 0.5V. If the two results are now added within a software routine then the A/D S-curve can be located within a resolution of 0.5V.

The A/D input has high impedance able to withstand up to 13V signals (input level tolerances ± 200mV absolute and ± 100mv relative to 5V).

Figure 56. AFC, IR and OSD Result Register



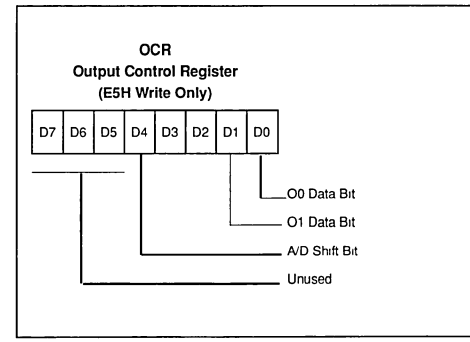
D7-D5. These bits are not used.

VSYNC. This bit reads the status of the VSYNC pin. It is inverted with respect to the pin. Refer to the OSD description for additional information.

IR. This bit reads the status of the IR latch. If a signal has been latched this bit will be high. Refer to the DEDICATED LATCHES description for additional information.

AD2-AD0. These bits store the real time conversion of the value present on the AFC input pin. No reset value.

Figure 57. Outputs Control Register



D7, D6, D5, D3, D2. These bits are not used.

A/D Shift. This bit determines the voltage range of the AFC input. Writing a zero will select the 0.5V to 4.5V range. Writing a one will select the 1.0V to 5.0V range. Undefined after reset.

62.5 KHz Output

This bit is available only on ST6386,88. The pin is push-pull output at a frequency of 62.5KHz (with an 8MHz clock). The pin can used to drive the SGS-THOMSON TEA5640 chroma processor. Refer to the TEA5640 data sheet for more information. Care must be taken to respect the frequency tolerances required by the TEA5640 by chosing a quartz with PPM variations within the limits required by the chroma processor.

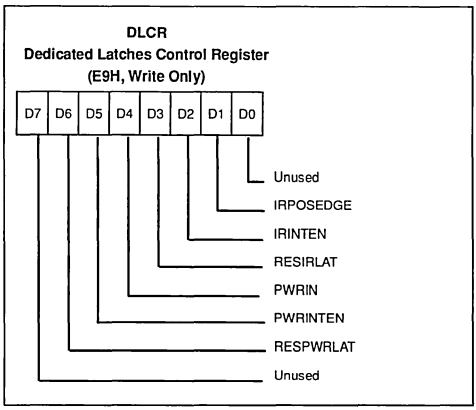
DEDICATED LATCHES

Two latches are available which may generate interrupts to the ST638X core. The IR latch is set either by the falling or rising edge of the signal on pin PC6(IRIN). If bit 1 (IRPOSEDGE) of the latches register (E9H) is high, then the latch will be triggered on the rising edge of the signal at PC6(IRIN). If bit 1 (IRPOSEDGE) is low, then the latch will be triggered on the rising edge of the signal at PC6(IRIN). The IR latch can be reset by setting bit 3 (RESIRLAT) of the latches register; the bit is set only and a high should be written every time the IR latch needs to be reset. If bit 2 (IRINTEN) of the latches register (E9H) is high, then the output of the IR latch, IRINTN, may generate an interrupt (#0). IRINTN is inverted with respect to the state of the

DEDICATED LATCHES (Continued)

IR latch. If bit 2 (IRINTEN) is low, then the output of the IR latch, IRINTN, is forced high. For more information see the interrupts section. The state of the IR latch may be read from bit 3 (IRLATCH) of register E4H; if the IR latch is set, then bit 3 will be high. The PWR latch is set either by the falling or rising edge of the signal on pin PC4(PWRIN). If bit 4 (PWREDGE) of the latches register (E9H) is high, then the latch will be triggered on the rising edge of the signal at PC4(PWRIN). If bit 4 (PWREDGE) is low, then the latch will be triggered on the falling edge of the signal at PC4(PWRIN). The PWR latch can be reset by setting bit 6 (RESPWRLAT) of the latches register; the bit is set only and a high should be written every time the PWR latch needs to be reset. If bit 5 (PWRINTEN) of the latches register (E9H) is high, then the output of the PWR latch, PWRINTN, may generate an interrupt (#4). PWRINTN is inverted with respect to the state of the PWR latch. If bit 5 (PWRINTEN) is low, then the output of the PWR latch, PWRINTN, is forced high. For more information see the interrupts section.

Figure 58. Dedicated Latched Control Register



D7. This bit is not used

RESPWRLAT. Resets the PWR latch; this bit is set only.

PWRINTEN. This bit enables the PWRINTN signal (#4) from the latch to the ST638X core. Undefined after reset.

PWRIN. The bit determines the edge which will cause the PWRIN latch to be set. If this bit is high, than the PWRIN latch will be set on the rising edge of the PWRIN signal. Undefined after reset.

RESIRLAT. Resets the IR latch; this bit is set only.

IRINTEN. This bit enables the IRINTN signal (#0) from the latch to the ST638X core. Undefined after reset.

IRPOSEDGE. The bit determines the edge which will cause the IR latch to be set. If this bit is high, than the IR latch will be set on the rising edge of the IR signal. Undefined after reset.

D0. This bit is not used

ON-SCREEN DISPLAY (OSD)

The ST638X OSD macrocell is a CMOS LSI character generator which enable display of characters and symbols on the TV screen. The character rounding function enhances the readability of the characters. The ST638X OSD receives horizontal and vertical synchronization signal and outputs screen information via R, G, B and blanking pins. The main characteristics of the macrocell are listed below:

- Number of display characters: 5 lines by 15 columns.
- Number of character types: 128 characters in two banks of 64 characters. Only one bank per screen can be used.
- Character size: Four character heights (18H, 36H 54H, 72H), two available per screen programmable by line.
- Character format: 6x9 dots with character rounding function.
- Character color: Eight colors available programmable by word.
- Display position: 64 horizontal positions by 2/fos and 63 vertical positions by 4 H
- Word spacing: 64 positions programmable from 2/fosc to 128/fosc.
- Line spacing: 63 positions programmable from 4 to 252 H.
- Background: No background, square background or fringe background programmable by word.
- Background color: Two of eight colors available programmable by word.
- Display output: Three character data output terminals (R,G,B) and a blank output terminal.
- Display on/off: Display data may be programmed on or off by word or entire screen. Entire screen may be blanked.

Format Specification

The entire display can be turned on or off thru the use of global enable bit or the display may be selectively turned on or off by word. To turn off the entire display, the global enable bit (GE) should be

ON-SCREEN DISPLAY (Continued)

zero. If the global enable is one, the display is controlled by the word enable bits (WE). The global enable bit is located in the global enable register and the word enable bit is located in the space character preceding the word.

Each line must begin with a format character which describes the format of that line and of the first word. This character is not displayed.

A space character defines the format of subsequent words. A space character is denoted by a one in bit 6 in the display RAM. If bit 6 of the display RAM is a zero, the other six bits define one of the 64 display characters.

The color, background and enable can be programmed by word. This information is encoded in the space character between words or in the format character at the beginning of each line. Five bits define the color and background of the following word, and determine whether it will be displayed or not.

Characters are stored in a 6 x 9 dot format. One dot is defined vertically as 2H (horizontal lines) and horizontally as 2/fosc if the smallest character size is enabled. There is no space between characters or lines if the vertical space enable (VSE) and horizontal space enable (HSE) bits are both zero. This allows the use of special graphics characters.

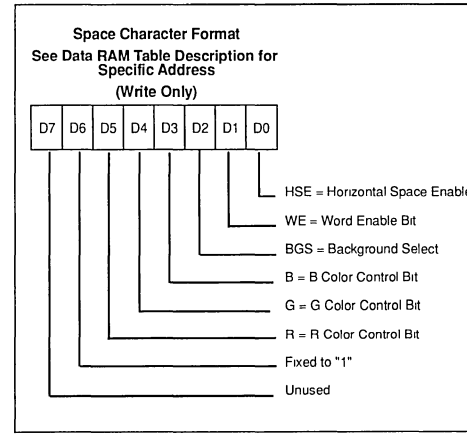
The normal alphanumeric character set is formatted to be 5 x 7 with on empty row at the top and one at the bottom and one empty column at the right. If VSE and HSE are both zero, then the spacing between alphanumeric characters is 1 dot and the spacing between lines of alphanumeric characters is 2H.

The character size is programmed by line thru the use of the size bit (S) in the format character and the global size bits (GS1 and GS2). The vertical spacing enable bit (VSE) located in the format character controls the spacing between lines. If this bit is set to one, the spacing between lines is defined by the vertical spacing register, otherwise the spacing between lines is 0.

The spacing between words is controlled by the horizontal space enable bit (HSE) located in the space character. If this bit is set to one, the spacing between words is defined by the horizontal spacing register, otherwise the space character width of 6 dots is the spacing between words.

The formats for the display character, space character and format character are described hereafter.

Figure 59. Space Character Register Explanation



D7. Not used.

D6. This pin is fixed to "1".

R, G, B. *Color.* The 3 color control bits define the color of the following word as shown in table 12.

Table 12. Space Character Register Colour Setting.

R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

BGS. *Background Select.* The background select bit selects the desired background for the following word. There are two possible backgrounds defined by the bits in the Background Control Register.

"0" - The background on the following word is enabled by BG0 and the color is set by R0, G0, and B0.

"1" - The background on the following word is enabled by BG1 and the color is set by R1, G1, and B1.

WE. *Word Enable.* The word enable bit defines whether or not the following word is displayed.

"0" - The word is not displayed.

ON-SCREEN DISPLAY (Continued)

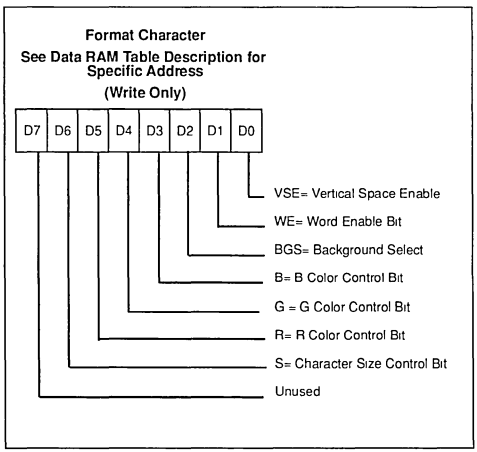
"1" - If the global enable bit is one, then the word is displayed.

HSE. *Horizontal Space Enable.* The horizontal space enable bit determines the spacing between words. The space between characters is always 0. The alphanumeric character set is implemented in a 5 x 7 format with one empty column to the right and one empty row above and below so that the space between alphanumeric characters will be one dot.

"0" - The space between words is equal to the width of the space character, which is 6 dots.

"1" - The space between words is defined by the value in the horizontal space register plus the width of the space character.

Figure 60. Format Character Register Explanation



D7. This bit is not used

S. *Character Size.* The character size bit, along with the global size bits (GS2 and GS1) located in the horizontal space register, specify the character size for each line as defined in Table 14.

R, G, B. *Color.* The 3 color control bits define the color of the following word as shown in Table 13.

BGS. *Background Select.* The background select bit selects the desired background for the following word. There are two possible backgrounds defined by the bits in the Background Control Register.

"0" - The background on the following word is enabled by BG0 and the color is set by R0, G0, and B0.

"1" - The background on the following word is enabled by BG1 and the color is set by R1, G1, and B1.

WE. *Word Enable.* The word enable bit defines whether or not the following word is displayed.

"0" - The word is not displayed.

"1" - If the global enable bit is one, then the word is displayed.

VSE. *Vertical Space Enable.* The vertical space enable bit determines the spacing between lines.

"0" - The space between lines is equal to 0H. The alphanumeric character set is implemented in a 5 x 7 format with one empty column to the right and one empty row above and one below and stored in a 6 x 9 format.

"1" - The space between lines is defined by the value in the vertical space register.

Table 13. Format Character Register Colour Setting.

R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

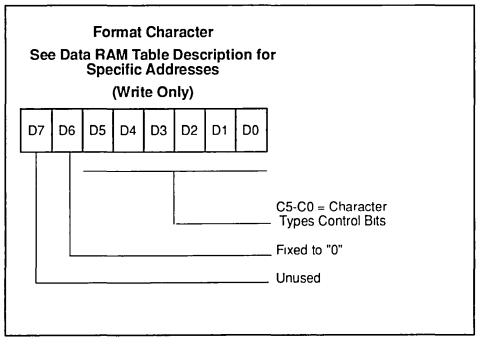
Table 14. Format Character Register Size Setting

GS2	GS1	S	Vertical Height	Horizontal lenght
0	0	0	18H	6 TDOT
0	0	1	36H	12 TDOT
0	1	0	18H	6 TDOT
0	1	1	54H	18 TDOT
1	0	0	36H	12 TDOT
1	0	1	54H	18 TDOT
1	1	0	36H	12 TDOT
1	1	1	72H	24 TDOT

TDOT= 2/fosc

ON-SCREEN DISPLAY (Continued)

Figure 61. Display Character Register Explanation



D7. This bit is not used.

D6. This bit is fixed to "0".

C5-C0. *Character type.* The 6 character type bits define one of the 64 available character types. These character types are shown on the following pages.

Character Types

The character set is user defined as ROM mask option.

Register and RAM Addressing

The OSD contains seven registers and 80 RAM locations. The seven registers are the Vertical Start Address register, Horizontal Start Address register, Vertical Space register, Horizontal Space register, Background Control register, Global Enable register and Character Bank Select register. The Global Enable register can be written at any time by the ST638X Core. The other six registers and the RAM can only be read or written to if the global enable is zero.

The six registers and the RAM are located on two pages of the paged memory of the ST638X MCUs; the Character Bank Select register is located outside the paged memory at address EDH. Each page contains 64 memory locations. This paged memory is at memory locations 00H to 3FH in the ST638X memory map. A page of memory is enabled by setting the desired page bit, located in the data RAM bank switching register, to a one. The page register is location E8H. A one in bit five selects page 5, located on the OSD and a one in bit 6 selects page 6 on the OSD. Table 15 shows the addresses of the OSD registers and RAM.

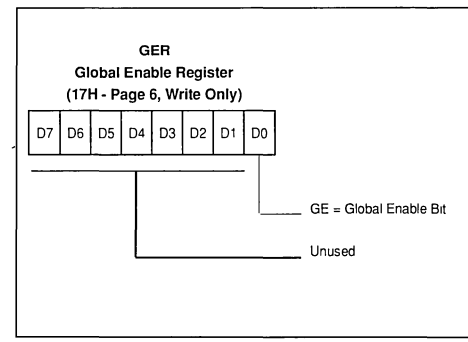
Table 15. OSD Control Registers and Data RAM Addressing

Page	Address	Register or RAM
5	00H - 3FH	RAM Locations 00H - 3FH
6	00H - 0FH	RAM Locations 00H - 0FH
6	10H	Vertical Start Register
6	11H	Horizontal Start Register
6	12H	Vertical Space Register
6	13H	Horizontal Space Register
6	14H	Background Control Register
6	17H	Global Enable Register
No Page	EDH	Character Bank Select Register

OSD Global Enable Register

This register contains the global enable bit (GE). It is the only register that can be written at any time regardless of the state of the GE bit. It is a write only register.

Figure 62. Global Enable register



D7-D1. These bits are not used

GE. *Global Enable.* This bit allows the entire display to be turned off.

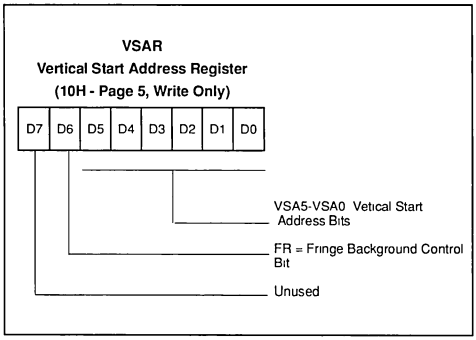
"0" - The entire display is disabled. The RAM and other registers of the OSD can be accessed by the Core.

"1" - Display of words is controlled by the word enable bits (WE) located in the format or space character.

The other registers and RAM cannot be accessed by the Core.

ON-SCREEN DISPLAY (Continued)

Figure 63. Vertical Start Address Register



D7. This bit is not used

FR. *Fringe Background.* This bit changes the background from a box background to a fringe background. The background is enabled by word as defined by either BK0 or BK1.

"0" - The background is defined to be a box which is 7 x 9 dots.

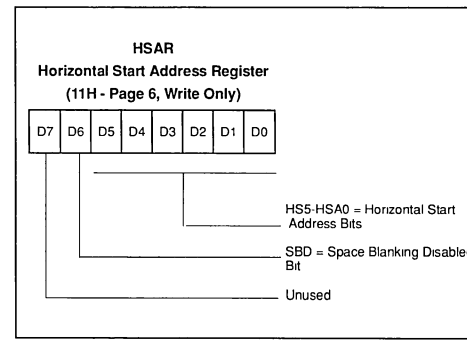
"1" - The background is defined to be a fringe.

VSA5-VSA0. *Vertical Start Address.* These bits determine the start position of the first line in the vertical direction. The 6 bits can specify 63 display start positions of interval 4H. The first start position will be the fourth line of the display. The vertical start address is defined VSA0 by the following formula.

Vertical Start Address = $4H(2^5(VSA5) + 2^4(VSA4) + 2^3(VSA3) + 2^2(VSA2) + 2^1(VSA1) + 2^0(VSA0))$

The case of all Vertical Start Address bits being zero is 111.

Figure 64. Horizontal Start Address Register



D7. This bit is not used.

SBD. *Space Blanking Disable.* This bit controls whether or not the background is displayed when outputting spaces. If two background colors are used on adjacent words, then the background should not be displayed on spaces in order to make a nice break between colors. If an even background around an area of text is desired, as in a menu, then the background should be displayed when outputting spaces.

"0" - The background during spaces is controlled by the background enable bits (BK0 and BK1) located in the Background Control register.

"1" - The background is not displayed when outputting spaces.

HSA5, HSA0 - *Horizontal Start Address bits.* These bits determine the start position of the first character in the horizontal direction. The 6 bits can specify 64 display start positions of interval 2/fosc or 400ns. The first start position will be at 4.0µs because of the time needed to access RAM and ROM before the first character can be displayed. The horizontal start address is defined by the following formula.

Horizontal Start Address = $2/fosc(10.0 + 2^5(HSA5) + 2^4(HSA4) + 2^3(HSA3) + 2^2(HSA2) + 2^1(HSA1) + 2^0(HSA0))$

ON-SCREEN DISPLAY (Continued)

Figure 65. Vertical Space Register

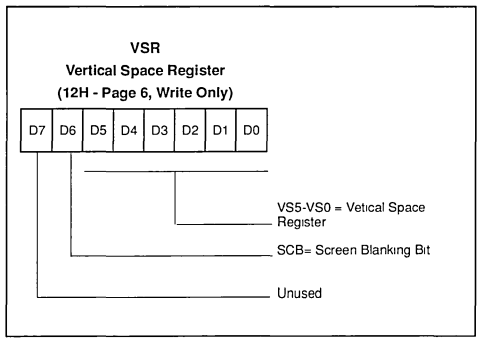
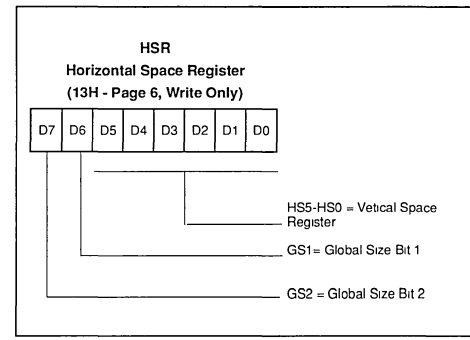


Figure 66. Horizontal Space Register



D7. This bit is not used

SCB. *Screen Blanking.* This bit allows the entire screen to be blanked.

"0" - The blanking output signal (VBLK) is active only when displaying characters.

"1" - The blanking output signal (VBLK) is always active. Characters in the display RAM are still displayed.

When this bit is set to one, the screen is blanked also without setting the Global Enable bit to one (OSD disabled).

VS5 , VS0. *Vertical Space.* These bits determine the spacing between lines if the Vertical Space Enable bit (VSE) in the format character is one. If VSE is zero there will be no spaces between lines. The Vertical Space bits can specify one of 63 spacing values from 4H to 252H. The space between lines is defined by the following formula.

Space between lines = $4H(2^5(VS5) + 2^4(VS4) + 2^3(VS3) + 2^2(VS2) + 2^1(VS1) + 2^0(VS0))$

The case of all Vertical Start Address bits being zero is ill.

GS2,GS1. *Global Size.* These bits along with the size bit (S) located in the Character format word specify the character size for each line as defined in table 16.

Table 16. Horizontal Space Register Size Setting.

GS2	GS1	S	Vertical Height	Horizontal Lenght
0	0	0	18H	6 TDOT
0	0	1	36H	12 TDOT
0	1	0	18H	6 TDOT
0	1	1	54H	18 TDOT
1	0	0	36H	12 TDOT
1	0	1	54H	18 TDOT
1	1	0	36H	12 TDOT
1	1	1	72H	24 TDOT

Note: TDOT= $2/f_{OSC}$

HS5, HS0 . *Horizontal Space* . These bits determine the spacing between words if the Horizontal Space Enable bit (HSE) located in the space character is a one. The space between words is then equal to the width of the space character plus the number of tdots specified by the Horizontal Space bits. The 6 bits can specify one of 64 spacing values ranging from 2/fosc to 128/fosc. The formula is shown below for the smallest size character(18H). If larger size characters are being displayed the spacing between words will increase proportionately. Multiply the value below by 2, 3 or 4 for character sizes of 36H, 54H and 72H respectively.

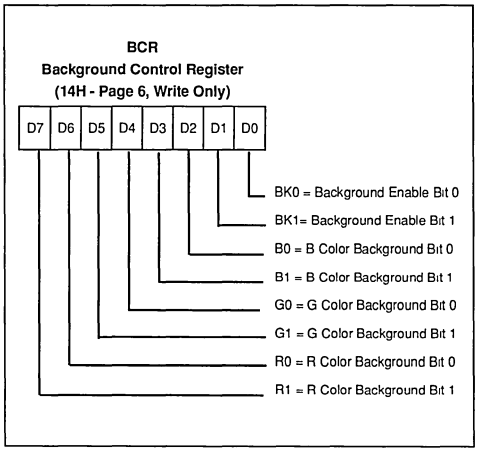
Space between words (not including the space character)$=2/fosc((1+2^5(HS5)+2^4(HS4)+2^3(HS3)+2^2(HS2)+ 2^1(HS1)+2^0(HS0))$

ON-SCREEN DISPLAY (Continued)

Background Control Register

This register sets up two possible backgrounds. The background select bit (BGS) in the format or space character will determine which background is selected for the current word.

Figure 67. Background Control Registers



R1,R0,G1,G0,B1,B0. Background Color. These bits define the color of the specified background, either background 1 or background 0 as defined in Table 17.

Table 17. Background Register Colour Setting.

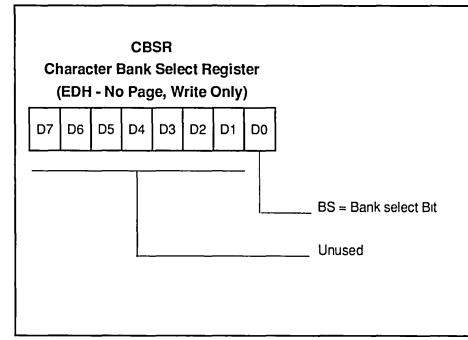
RX	GX	BX	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

BK1,BK0. *Background Enable.*These bits determine if the specified background is enabled or not.

"0" - The following word does not have a background.

"1" - There is a background around the following word.

Figure 68. Character Bank Select Register



D7-D1. These bits are not used

BS. *Bank Select.* This bit select the character bank to be used. The lower bank is selected with 0. The value can be modified only when the OSD is OFF (GE=0). No reset value.

OSD Data RAM

The contents of the data RAM can be accessed by the ST638X MCUs only when the global enable bit (GE) in the Global Enable register is a zero.

The first character in every line is the format character. This character is not displayed. It defines the size of the characters in the line and contains the vertical space enable bit. This character also defines the color, background and display enable for the first word in the line. Subsequent characters are either spaces or one of the 64 available character types.

The space character defines the color, background, display enable and horizontal space enable for the following word. Since there are 5 display lines of 15 characters each, the display RAM must contain 5 lines x (15 characters + 1 format character) or 80 locations. The RAM size is 80 locations x 7 bits. The data RAM map is shown inTable 18.

ON-SCREEN DISPLAY (Continued)

Table 18. OSD RAM Map

Column				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A0				0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A3				0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A2				0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A1				0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A6	A5	A4	LINE																
0	0	0	1	FT															
0	0	1	2	FT															
0	1	0	3	FT															
0	1	1	4	FT															
1	0	0	5	FT															
					AVAILABLE SCREEN SPACE														

Notes: FT. The format character required for each line. Characters in columns 1 thru 15 are displayed.

Emulator Remarks

There are a few differences between emulator and silicon. For noise reasons, the OSD oscillator pins are not available: the internal oscillator cannot be disabled and replaced by an external coil. In the emulator, the Character Bank Select register can be written also with Global Enable bit set, while this is not allowed in the device.

Application Notes

1 - The OSD character generator is composed of a dual port video ram and some circuitry. It needs two input signals VSYNC and HSYNC to syncronize its dedicated oscillator to the TV picture. It generates 4 output signals, that can be used from the TV set to generate the characters on the screen. For istance, they can be used to feed the SCART plug, providing an adequate buffer to drive the low impedance (75 Ω) of the SCART inputs.

2 - The Core sees the OSD as a number of RAM locations (80) plus a certain number of control registers (6). These 86 locations are mapped in two pages of the dynamic data ram address range (0H..3FH).
In page 5 (load 20H in the register 0E8H), there are 64 bytes of RAM, the ones of the first 4 rows (16 bytes each row, 15 characters per row maximum, plus an hidden leading format character). In page 6 (load 40H in register 0E8H), the 16 bytes of the fith row (0..0FH), and the 6 control registers (10H..14H,17H).

3 - The video RAM is a dual port ram. That means that it can be addressed either from the Core or from the OSD circuitry itself. To reduce the complexity of the circuitry, and thus its cost, some restrictions have been introduced in the use of the OSD.

a. The Core can Only write to any of the 86 locations (either video RAM or control registers).

b. The Core can Only write to any of the leading 85 locations when the OSD oscillator is OFF. Only the last location (control register 17H in page 6) can be addressed at any time. This is the Global Enable Register, which contains only the GE bit. If it is set, the OSD is on, if it is reset the OSD is off.

4 - The timing of the on/off switching of the OSD oscillator is the following:

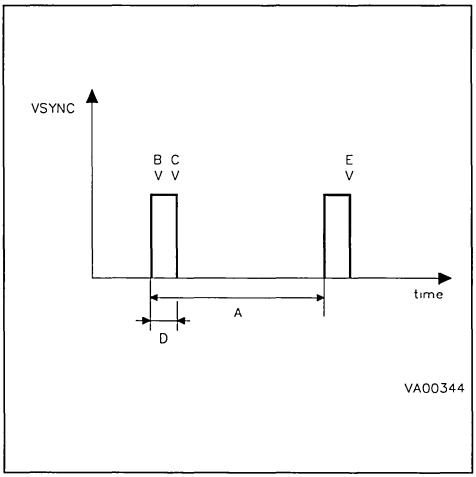
a. GE bit is set. The OSD oscillator will start on the next VSYNC signal.

b. GE bit is reset. The OSD oscillator will be immediately switched off.

ON-SCREEN DISPLAY (Continued)

To avoid a bad visual impression, it is important that the GE bit is set before the end of the flyback time when charging character. This can be done inside the VSYNC interrupt routine. The following diagram can explain better:

Figure 69. OSD Oscillator ON/OFF Timing



Notes: A - Picture time· 20 mS in PAL/SECAM.
B - VSYNC interrupt, if enabled.
C - Starting of OSD oscillator, if GE = 1.
D - Flyback time.

When modifying the picture display (i.e.: a bar graph for an analog control), it is important that the switching on of the GE bit is done before the the end of the flyback time (D in Figure 69). If the GE bit is set after the end of the flyback time then the OSD will not start until the begining of the next frame. This results in one frame being lost and will result in a Flicker on the screen. One method to be sure to avoid the flicker is to wait for the VSYNC interrupt at the start of the flyback; once the VSYNC interrupt is detected, then the GE bit can be set to zero, the characters changed, and the GE set to one. All this should occur before the end of the flyback time in order not to loose a frame. The correct edge of the interrupt must be chosen. The VSYNC pin may alternatively be sampled by software in order to know the status; this can be done by reading bit 4 of register E4H; this bit is inverted with respect to the VSYNC pin.

6 - An OSD end of line Bar is present in the ST63P8X piggyback and ST638X ROM devices when using the background mode. If this bar is present with software running in the piggybacks then it is also present on the ROM mask version. If the end of line bar is seen to be eliminated by software in the piggyback, then it is also be eliminated in the ROM mask version.

The bar appears at the end of the line in the background mode when the last character is a space character and the first format character is defined with S=0 (size 0). The bar is the color of the background defined by the space character. To eliminate bar:

a. If two backgrounds are used then the bar should be moved off the screen by using large word spaces instead of character spaces. If there are not enough spaces before the end of the line, then the location of the valid characters should be moved so they appear at the end of the line (and hence no bar); positioning can be compensated using the horizontal start register.

b. If only one background is used, then the other background should be transparent in order to eliminate the bar.

7 - The OSD oscillator external network should consist of a capacitor on each of the OSD oscillator pins to ground together with an inductance between pins. The user should select the two capacitors to be the same value (15pF to 25pF each is recommended). The inductance is chosen to give the desired OSD oscillator frequency for the application (normally 56µH).

SOFTWARE DESCRIPTION

The ST638X software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short to provide byte efficient programming capability. The ST638X Core has the ability to set or clear any register or RAM location bit of the Data space with a single instruction. Furthermore, the program may branch to a selected address depending on the status of any bit of the Data space. The carry bit is stored with the value of the bit when the SET or RES instruction is processed.

Addressing Modes

The ST638X Core has nine addressing modes which are described in the following paragraphs. The ST638X Core uses three different address spaces: Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, the data for immediate mode instructions, and in this space is physically allocated the data ROM which is addressed as data space. Data space contains the Accumulator, the X,Y,V and W registers, the Core control registers, peripheral and Input/Output registers, the RAM locations and the window to address the Data ROM (physically located into the program memory) locations (for storage of tables and constants). Stack space contains six 12-bit RAM bytes used to stack the return addresses for subroutines and interrupts.

Immediate. In the immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In the direct addressing mode, the address of the byte that is processed by the instruction is stored in the location that follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data space memory with a single two-byte instruction.

Short Direct. The Core can address the four RAM registers X,Y,V,W (locations 80H, 81H, 82H, 83H) in the short-direct addressing mode . In this case, the instruction is only one byte long and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of the direct addressing mode. (Note : 80H and 81H are also indirect registers).

Extended. In the extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four less significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) that use the extended addressing mode are able to branch any address of the directly addressable Program space. An extended addressing mode instruction is two-byte long.

Program Counter Relative. The relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to + 16 locations around the address of the relative instruction. If the condition is not true, the instruction that follows the relative instruction is executed. The relative addressing mode instruction is one-byte long. The opcode is obtained by adding the three most significant bits that characterize the kind of test, one bit that determines whether the branch is a toward (when it is 0) or backward (when it is 1) branch and the four less significant bits that give the span of the branch (0H to FH) that must be added or subtracted to the address of the relative instruction to obtain the address of the branch.

Bit Direct. In the bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 directly addressable locations of Data space memory can be set or cleared.

Bit Test & Branch. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit test and branch instruction is three-byte long. The bit identification and the tested condition are included in the opcode byte. The address of the byte to be tested follows immediately the opcode in the Program space. The third byte is the jump displacement, which is in the range from -126 to + 129. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In the indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed by the content of one of the indirect registers, X or Y (80H,81H). The indirect register is selected by the bit 4 of the opcode. A register indirect instruction is one byte long.

Inherent. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

SOFTWARE DESCRIPTION (Continued)

Instruction Set

The ST638X Core has a set of 40 basic instructions. When these instructions are combined with nine addressing modes, 244 usable opcodes can be obtained. They can be divided into six different types : load/store, arithmetic/logic, conditional branch, control instructions, jump/call, bit manipulation. The following paragraphs describe the different types. All the instructions within a given type are presented in individual tables.

Load & Store. These instructions use one,two or three bytes in relation with the addressing mode. One operand is the Accumulator for LOAD and the other operand is obtained from data memory using one of the addressing modes. For LOAD Immediate one operand can be any of the 256 data space bytes while the other is always an immediate data. Refer to Table 19.

Table 19. Load & Store instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
LD A, X	Short Direct	1	4	Δ	*
LD A, Y	Short Direct	1	4	Δ	*
LD A, V	Short Direct	1	4	Δ	*
LD A, W	Short Direct	1	4	Δ	*
LD X, A	Short Direct	1	4	Δ	*
LD Y, A	Short Direct	1	4	Δ	*
LD V, A	Short Direct	1	4	Δ	*
LD W, A	Short Direct	1	4	Δ	*
LD A, rr	Direct	2	4	Δ	*
LD rr, A	Direct	2	4	Δ	*
LD A, (X)	Indirect	1	4	Δ	*
LD A, (Y)	Indirect	1	4	Δ	*
LD (X), A	Indirect	1	4	Δ	*
LD (Y), A	Indirect	1	4	Δ	*
LDI A, #N	Immediate	2	4	Δ	*
LDI rr, #N	Immediate	3	4	*	*

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr Data space register
Δ Affected
* Not Affected

SOFTWARE DESCRIPTION (Continued)

Arithmetic and Logic. These instructions are used to perform the arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while the other can be either a data space memory content or an immediate value in relation with the addressing mode. In CLR,DEC,INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator. Refer to Table 20.

Table 20. Arithmetic & Logic instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	*
AND A, (Y)	Indirect	1	4	Δ	*
AND A, rr	Direct	2	4	Δ	*
ANDI A, #N	Immediate	2	4	Δ	*
CLR A	Short Direct	2	4	Δ	Δ
CLR rr	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register

Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Conditional Branch. The branch instructions achieves a branch in the program when the selected condition is met. Refer to Table 21.

Bit Manipulation Instructions. These instructions can handle (set or reset) any bit in data space memory. Refer to Table 22.

Control Instructions. The control instructions control the MCU operations during program execution. Refer to Table 23.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutines call inside the whole program space. Refer to Table 24.

Table 21. Conditional Branch instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b 3-bit address
e 5 bit signed displacement in the range -15 to +16
ee 8 bit signed displacement in the range -126 to +129
rr. Data space register
Δ. Affected
*. Not Affected

Table 22. Bit Manipulation instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes:
b 3-bit address;
rr Data space register,
*. Not Affected

Table 23. Control instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:
1 This instruction is deactivated on ST638X (HW watchdog and a WAIT is automatically executed instead of a STOP)
Δ. Affected
*. Not Affected

Table 24. Jump & Call instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes:
abc. 12-bit address;
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Opcode Map Summary. The following table contains an opcode map for the instructions used on the MCU.

Table 25. Opcode Map

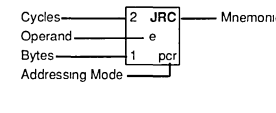
Low / Hi	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Low / Hi
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 dir	2 JRC e 1 prc	4 LD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 pcr	4 LD a,(y) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 pcr	4 LD a,rr 2 dir	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 dir	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b d	2 JRZ e 1 pcr	4 COM a 1 inh	2 JRC e 1 pcr	4 CP a,(y) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b d	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 pcr	4 CP a,rr 2 dir	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 dir	2 JRC e 1 prc	4 ADD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 pcr	4 ADD a,(y) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 pcr	4 ADD a,rr 2 dir	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 dir	2 JRC e 1 prc	4 INC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 pcr	4 INC (y) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	# 1 dir	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 pcr	4 INC rr 2 dir	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 dir	2 JRC e 1 prc	4 LD (x),a 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b d	2 JRZ e 1 pcr	# 1 dir	2 JRC e 1 pcr	4 LD (y),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	# 1 dir	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 pcr	4 LD rr,a 2 dir	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 dir	2 JRC e 1 prc	4 AND a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b d	2 JRZ e 1 pcr	4 RLC a 1 inh	2 JRC e 1 pcr	4 AND a,(y) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 pcr	4 AND a,rr 2 dir	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 dir	2 JRC e 1 prc	4 SUB a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 pcr	4 SUB a,(y) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 pcr	4 SUB a,rr 2 dir	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 dir	2 JRC e 1 prc	4 DEC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 pcr	4 DEC (y) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	# 1 dir	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 pcr	4 DEC rr 2 dir	F 1111

Abbreviations for Addressing Modes

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement



ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature. Tj, in Celsius can be obtained form.:

$$Tj = TA + PD \times RthJA$$

Where: TA = Ambient Temperature,
RthJA = Package thermal resistance (junction-to ambient),

PD = Pint + Pport,

Pint = $I_{DD} \times V_{DD}$ (chip internal power),

Pport = Port power dissipation (determined by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
V_I	Input Voltage (AFC IN)	V_{SS} – 0.3 to +13	V
V_I	Input Voltage (Other Inputs)	VSS – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage (PA4-PA7, PC4-PC7, DA0-DA5)	V_{SS} – 0.3 to + 13	V
V_O	Output Voltage (Other Inputs)	VSS – 0.3 to V_{DD} +0.3	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}, PA6, PA7	± 10	mA
I_O	Current Drain per Pin (PA6, PA7)	± 50	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	150	mA
T_j	Junction Temperature	150	°C
T_{STG}	Storage Temperature	– 60 to 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PSDIP42			67	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature		0		70	°C
V_{DD}	Operating Supply Voltage		4.5		6.0	V
f_{OSC}	Oscillator Frequency RUN & WAIT Modes			8.0	8.1	MHz
f_{OSDOSC}	On-Screen Display Oscillator Frequency				8.0	MHz

EEPROM INFORMATION

The ST638X EEPROM macrocell and the single poly EEPROM process have been specially developed to achieve 1.000.000 Write/Erase cycles and a 10 years data retention.

DC ELECTRICAL CHARACTERISTICS

(T_A= 0 to + 70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	All I/O Pins			0.2xV_{DD}	V
V_{IH}	Input High Level Voltalge	All I/O Pins	0.8xV_{DD}			V
V_{HYS}	Hysteresis Voltage(1)	All I/O Pins V_{DD} = 5V		1.0		V
V_{OL}	Low Level Output Voltage	DA0-DA5, PB0-PB6, OSD Outputs, PC0-PC7, O0, O1, PA0-PA5, 62.5KHz OUT V_{DD} = 4.5V I_{OL} = 1.6mA I_{OL} = 5.0mA			 0.4 1.0	 V V
V_{OL}	Low Level Output Voltage	PA0-PA7, V_{DD} = 4.5V I_{OL}= 1.6mA I_{OL}= 25mA			 0.4 1.0	 V V
V_{OL}	Low Level Output Voltage	OSDOSCOUT, OSCOUT, V_{DD} = 4.5V I_{OL}= 0.4mA			 0.4	 V
V_{OH}	High Level Output Voltage	PB0-PB7, PA0-PA3, OSD Outputs, PC0-PC3, 62.5KHz OUT, V_{DD} = 4.5V I_{OH} = – 1.6mA	 4.1			 V
V_{OH}	High Level Output Voltage	OSDOSCOUT, OSCOUT, V_{DD} = 4.5V I_{OL}= – 0.4mA	 4.1			 V
I_{PU}	Input Pull Up Current Input Mode with Pull-up	PB0-PB6, PA0-PA3, PC0-PC3 V_{IN}= V_{SS}	– 100	– 50	– 25	µA
I_{IL} I_{IH}	Input Leakage Current	OSCIN V_{IN}= V_{SS} V_{IN}= V_{DD}	 – 10 0.1	 – 1 1	 – 0.1 10	 µA
I_{IL}	Input Pull-down current in Reset	OSCIN	 100			 µA
I_{IL} I_{IH}	Input Leakage Current	All I/O Input Mode no Pull-up OSDOSCIN V_{IN}= V_{DD} or V_{SS}	 – 10		 10	 µA
V_{DD}RAM	RAM Retention Voltage in RESET		1.5			V
I_{IL} I_{IH}	Input Leakage Current	Reset Pin with Pull-up V_{IN}= V_{SS}	 – 50	 – 30	 – 10	 µA
I_{IL} I_{IH}	Input Leakage Current	AFC Pin V_{IH}= V_{DD} V_{IL}= V_{SS} V_{IH}= 12.0V	 – 1		 1 40	 µA
I_{OH}	Output Leakage Current	DA0-DA5, PA4-PA5, PC0-PC7, O0, O1 V_{OH} = V_{DD}			 10	 µA
I_{OH}	Output Leakage Current High Voltage	DA0-DA5, PA4-PA7, PC4-PC7, O0, O1 V_{OH} = 12V			 40	 µA

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{DD}	Supply Current RUN Mode	f_{OSC}= 8MHz, ILoad= 0mA V_{DD}= 6.0V		6	16	mA
I_{DD}	Supply Current WAIT Mode	f_{OSC}= 8MHz, ILoad= 0mA V_{DD}= 6V		3	10	mA
I_{DD}	Supply Current at transition to RESET	f_{OSC}= Not App, ILoad= 0mA V_{DD}= 6V		0.1	1	mA
V_{ON}	Reset Trigger Level ON	RESET Pin			0.3xV_{DD}	V
V_{OFF}	Reset Trigger Level OFF	RESET Pin	0.8xV_{DD}			V
V_{TA}	Input Level Absolute Tolerance	A/D AFC Pin V_{DD} = 5V			±200	mV
V_{TR}	Input Level Relatice Tolerance (1)	A/D AFC Pin Relative to other levels V_{DD} = 5V			±100	mV

Note: 1. Not 100% Tested

AC ELECTRICAL CHARACTERISTICS

(T_A= 0 to + 70°C, f_{OSC} = 8MHz, V_{DD} = 4.5V to 6.0V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
tWRES	Minimum Pulse Width	RESET Pin	125			ns
t_{OHL}	High to Low Transition Time	PA6, PA7 V_{DD} = 5V,CL = 1000pF (2)		100		ns
t_{OHL}	High to Low Transition Time	DA0-DA5, PB0-PB6, OSD Outputs, PC0-PC7, V_{DD} = 5V, CL = 100pF		20		ns
t_{OLH}	Low to High Transition Time	PB0-PB6, PA0-PA3, OSD Outputs, PC0-PC3, V_{DD} = 5V, CL = 100pF		20		ns
t_{OH}	Data HOLD Time SPI after clock goes low I^2CBUS/S-BUS Only		125			ns
f_{DA}	D/A Converter Repetition Frequency(1)			31.25		KHz
f_{SIO}	SIO Baud Rate(1)			62.50		KHz
f_{OUT1}	62.5KHz Output(1)	ST6386,87		62.50		KHz
tWEE	EEPROM Write Time	T_A = 25 °C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycles	Q_A LOT Acceptance Criteria	300.000	> 1 million		cycles
Retention	EEPROM Data Retention (4)	T_A = 25°C	10			years
C_{IN}	Input Capacitance (3)	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance (3)	All outputs Pins			10	pF
COSCIN, COSCOUT	Oscillator Pins Internal Capacitance(3)			5		pF
COSDIN, COSDOUT	OSD Oscillator External Capacitance	Recommended	15		25	pF

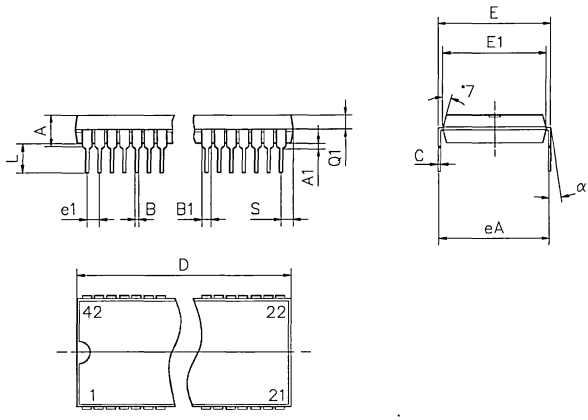
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
COSDIN, COSDOUT	OSD Oscillator External Capacitance	Recommended	15		25	pF

Notes:
1. A clock other than 8 MHz will affect the frequency response of those peripherals (D/A, 62.5KHz and SPI) whose clock is derived from the system clock.
2 The rise and fall times of PORT A have been reduced in order to avoid current spikes while maintaining a high drive capability
3 Not 100% Tested
4 Based on extrapolated data

PACKAGE MECHANICAL DATA

Figure 70. 42-Pin Shrink Dual in Line Plastic (JEDEC MO-015 BB)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.81		5.08	0 15		0 20
A1	0 51		1.78	0 020		0 070
B	0 35		0.59	0 013		0 023
B1	0.75		1 42	0 029		0.056
C	0 20		0 36	0 008		0 014
D			39.12			1.540
E	15.24		15 87	0 60		0 62
E1	12 70		14 48	0 50		0 57
e1		1 78			0 070	
eA		15 24			0 600	
L	2.54		3.40	0 10		0.13
Q1	1 52		2.29	0.20		0.09
S	0.76		2.67	0 03		0 105
α	0		15°	0		15°

ORDERING INFORMATION

The following chapter deals with the procedure for transfer the Program/Data ROM codes to SGS-THOMSON.

Communication of the ROM Codes. To communicate the contents of Program /Data ROM memories to SGS-THOMSON, the customer has to send:

- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the PROGRAM Memory
- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the ODD and EVEN ODD OSD Characters
- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the EEPROM initial content (this file is optional)
- a filled Option List form as described in the OPTION LIST paragraph.

The program ROM should respect the ROM Memory Map as in Table 26.

The ROM code must be generated with ST6 assembler. Before programming the EPROM, the buffer of the EPROM programmer must be filled with FFH. For shipment to SGS-THOMSON the EPROMs should be placed in a consecutive IC carrier and packaging carefully.

ORDERING INFORMATION (Continued)

Table 26. ROM Memory Map

ROM Page	Device Address	EPROM Address (1)	Description
Page 0	0000H-007FH 0080H-07FFH	0000H-007FH 0080H-07FFH	Reserved User ROM
Page 1 "STATIC"	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	User ROM Reserved Interrupt Vectors Reserved NMI Vector Reset Vector
Page 2	0000H-000FH 0010H-07FFH	1000H-100FH 1010H-17FFH	Reserved User ROM
PAGE 3	0000H-000FH 0010H-07FFH	1800H-180FH 1810H-1FFFH	Reserved user ROM
Page 4	0000H-000FH 0010H-07FFH	2000H-200FH 2010H-27FFH	Reserved User ROM
Page 5	0000H-000FH 0010H-07FFH	2800H-280FH 2810H-2FFFH	Reserved User ROM
Page 6	0000H-000FH 0010H-07FFH	3000H-300FH 3010H-37FFH	Reserved User ROM
Page 7	0000H-000FH 0010H-07FFH	3800H-380FH 3810H-3FFFH	Reserved User ROM
Page 8	0000H-000FH 0010H-07FFH	4000H-400FH 4010H-47FFH	Reserved User ROM
Page 9	0000H-000FH 0010H-07FFH	4800H-480FH 4810H-4FFFH	Reserved User ROM

Notes:
1. EPROM addresses are related to the use of ST63P8X piggyback emulation devices.

ORDERING INFORMATION (Continued)

Customer EEPROM Initial Contents: Format

a. The content should be written into an INTEL INTELLEC format file.

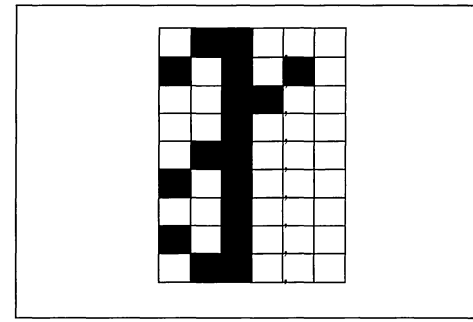
b. In the case of 384 bytes of EEPROM, the starting address is 000H and the end address is 7FH. The order of the pages (64 bytes each) is an in the specification (ie. b7, b1 b0: 001, 010, 011, 101, 110. 111).

c. Undefined or don't care bytes should have the content FFH.

OSD Test Character. In order to allow the testing of the on-chip OSD macrocell the following character must be provided at the fixed 3FH (63) position of the second OSD bank.

Listing Generation & Verification. When SGS-THOMSON receives the Codes, they are compared and a computer listing is generated from them. This listing refers extractly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed list constitutes a part of the contractual agreement for the creation of the customer mask. SGS-THOMSON sales organization will provide detailed information on contractual points.

Figure 71. OSD Test Character



ST638X MICROCONTROLLER OPTION LIST

Customer: . . . . . .

Ordering Information Table

Sales Type	ROM/EEPROM Size	Temperature Range	Package
ST6385B1/XX	20K/384 Bytes	0 to + 70 ° C	PSDIP42
ST6386B1/XX	20K/384 Bytes	0 to + 70 ° C	PSDIP42
ST6387B1/XX	20K/384 Bytes	0 to + 70 ° C	PSDIP42
ST6388B1/XX	20K/384 Bytes	0 to + 70 ° C	PSDIP42

Note: "XX" Is the ROM code identifier that is allocated by SGS-THOMSON after receipt of all required options and the related ROM file.

Address: . . . . . .
Contact: . . . . . .
Phone No: . . . . . .
Reference: . . . . . .

Device [ ] (d) Package [ ] (p) Temperature Range [ ] (t)
For marking one line with 10 characters maximum is possible
Special Marking [ ] (y/n) Line1 " _ _ _ _ _ _ _ _ _ _ " (N)

Notes:
(d) 1= ST6385, 2 = ST6386, 3 = ST6387, 4 = ST6388
(p) B= Dual in Line Plastic
(t) 1= 0 to 70°C

(N) Letters, digits, ' . ', ' - ', ' / ' and spaces only

Marking: the default marking is equivalent to the sales type only (part number).

OSD POLARITY OPTIONS (Put a cross on selected item) :

	POSITIVE	NEGATIVE
VSYNC,HSYNC	[ ]	[ ]
R,G,B	[ ]	[ ]
BLANK	[ ]	[ ]

CHECK LIST:

	YES	NO
ROM CODE	[ ]	[ ]
OSD Code: ODD & EVEN	[ ]	[ ]
EEPROM Code (if Desired)	[ ]	[ ]

Signature .....

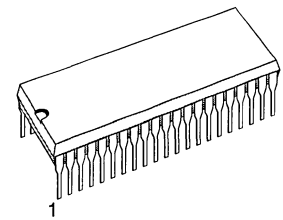
Date .....

SGS-THOMSON MICROELECTRONICS

ST6391,6393,6394 ST6395,6396,6399

8 BIT HCMOS MCUs FOR TV FREQUENCY SYNTHESIS WITH OSD

- 8-bit Architecture
- HCMOS Technology
- 8MHz Clock
- User Program ROM: 7948 bytes (ST6394)
  16076 bytes (ST6391,93,99)
  20140 bytes(ST6395,96)
- Reserved Test ROM: 244 bytes (ST6394)
  308 bytes (ST6391,93,99)
  336 bytes (ST6395,96)
- Data ROM: User selectable size
- Data RAM: 64 bytes (ST6394)
  256 bytes
  (ST6391,93,95,96,99)
- Data EEPROM: 128 bytes (ST6391,93,99)
  384 bytes (ST6394,95,96)
- 42-Pin Shrink Dual in Line Plastic Package
- 23 software programmable general purpose Inputs/Outputs, including 2 direct LED driving Outputs (On ST6391,95,99)
  two pins are output only(On ST6394,96)
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I^2C BUS and standard serial protocols
- Up to Six 6-Bit PWM D/A Converters
- 62.5KHz Output Pin (ST6399 Only)
- AFC A/D converter with 0.5V resolution (ST6393,94,96)
- Five interrupt vectors (IRIN/NMI, Timer 1 & 2, VSYNC, PWR INT.)
- On-chip clock oscillator
- 5 Lines by 15 Characters On-Screen Display Generator with 128 Characters
- Byte efficient instruction set
- Bit test and jump instructions
- Wait and Bit Manipulation instructions
- True LIFO 6-level stack
- All ROM types are supported by pin-to-pin piggyback versions.
- The development tool of the ST63XX microcontrollers consists of the emulation and development system to be connected via a standard RS232 serial line to an MS-DOS Personal Computer.



PSDIP42

(Ordering Information at the end of the datasheet)

DEVICE SUMMARY

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)
ST6391	16K	256	128
ST6393	16K	256	128
ST6394	8K	64	384
ST6395	20K	256	384
ST6396	20K	256	384
ST6399	16K	256	128

Figure 1. ST6394,96 Pin Configuration

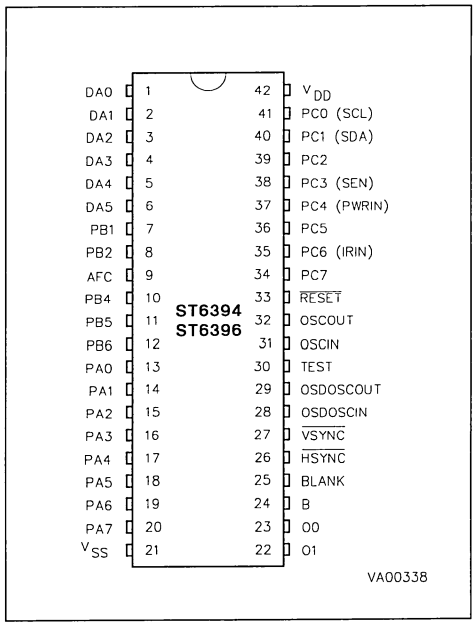
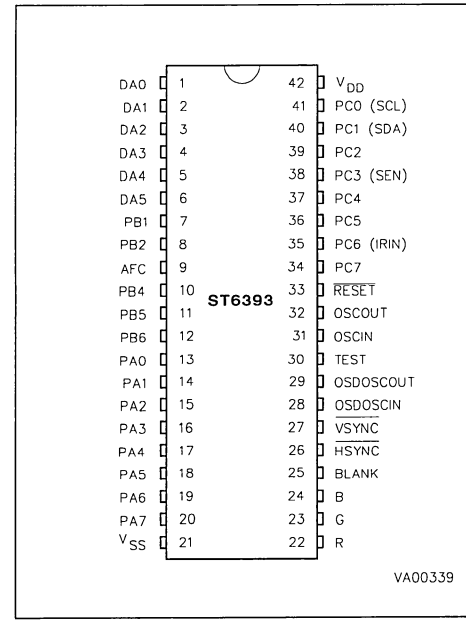


Figure 2. ST6393 Pin Configuration



Figre 3. ST6399 Pin Configuration

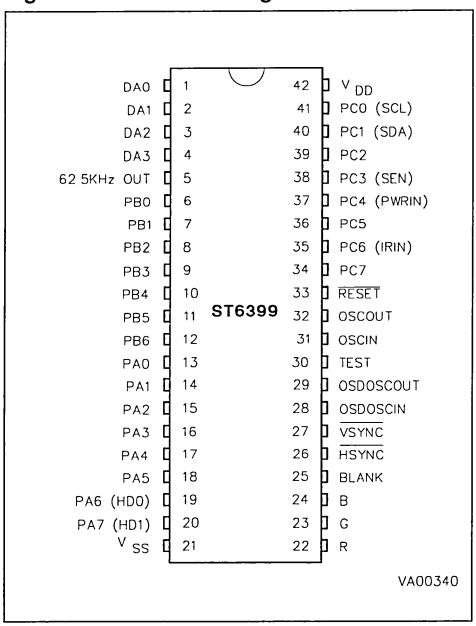
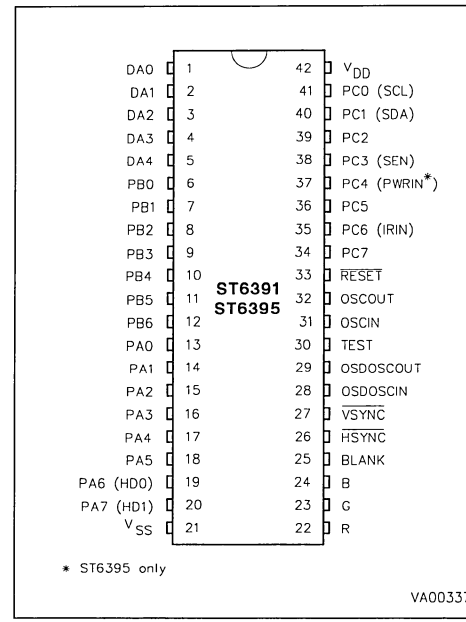


Figure 4. ST6391,95 Pin Configuration



GENERAL DESCRIPTION

The ST6391,93,94,95,96,99 microcontrollers are members of the 8-bit HCMOS ST639X family, a series of devices specially oriented to TV applications. Different pin-out and peripheral configurations are available to give the maximum application and cost flexibility. All ST639X members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility and short design time. Many of these macrocells are specially dedicated to TV applications. The macrocells of the ST639X family are : two Timer peripherals each including an 8-bit counter with a 7-bit software programmable prescaler (Timer), a digital hardware activated watchdog function (DHWD), a serial peripheral interface (SPI), up to six 6-bit PWM D/A converters, an AFC A/D converter with 0.5V resolution, an on-screen display (OSD) with 15 characters per line, 128 characters (in two banks each of 64 characters). In addition the following memory resources are available: program ROM (up to 20K), data RAM (up to 256 bytes), EEPROM (up to 384 bytes). Refer to pin configurations figures and to ST639X device summary (Table 1) for the definition of ST639X family members and a summary of differences among the different types.

Figure 5. ST6391,93,94,95,96,99 Block Diagram

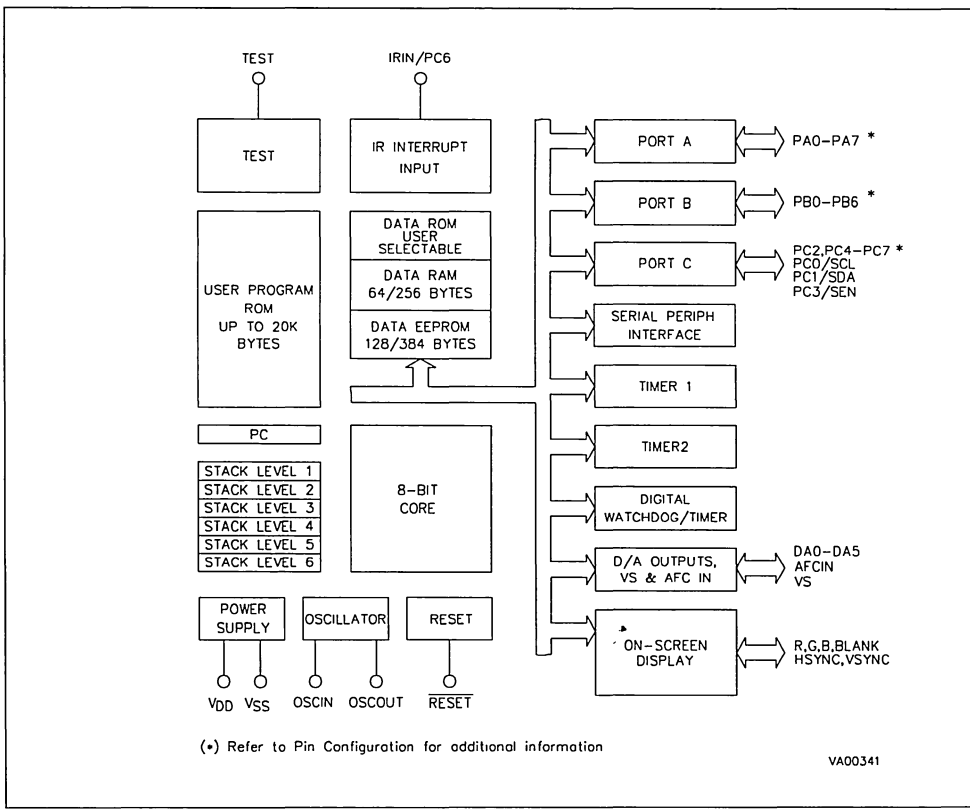


Table 1. ST639X Device Summary

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	AFC	D/A	LOW PWR IN RESET	PWRIN PIN	COLOR PINS	SPI CLOCK FREQ. (KHz)	62.5KHz PIN	EMUL. DEVICE
ST6391	16K	256	128	NO	5	NO	NO	3	62.5	NO	ST63P91
ST6393	16K	256	128	YES	6	NO	NO	3	62.5	NO	ST63P93
ST6394	8K	64	384	YES	6	YES	YES	1	62.5	NO	ST63P94
ST6395	20K	256	384	NO	5	NO	YES	3	100	NO	ST63P95
ST6396	20K	256	384	YES	6	YES	YES	1	62.5	NO	ST63P96
ST6399	16K	256	128	NO	4	YES	YES	3	62.5	YES	ST63P99

Note: 1. Low power in RESET function disables the oscillator when RESET pin is active (LOW)

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN, OSCOUT. These pins are internally connected to the on-chip oscillator circuit. A quartz crystal or a ceramic resonator can be connected between these two pins in order to allow the correct operation of the MCU with various stability/cost trade-offs. The OSCIN pin is the input pin, the OSCOUT pin is the output pin. Refer to ON-CHIP CLOCK OSCILLATOR description for additional information.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to start the microcontroller to the beginning of its program. Additionally in the ST6394/96/99 the quartz oscillator will be disabled when the $\overline{\text{RESET}}$ pin is low to reduce power consumption during reset phase. Refer to RESET description for additional information.

TEST. The TEST (mode select) pin is used to place the MCU into special operating mode. If TEST is held at V_{SS} the MCU enters the normal operating mode. If TEST is held at V_{DD} when $\overline{\text{RESET}}$ is active the test operating mode is automatically selected (the user should connect this pin to V_{SS} for normal operation). Refer to TEST mode description for additional information.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input with or without pull-up resistor or as an output under software control of the data direction register. Pins PA4 to PA7 are configured as open-drain outputs (12V drive). On PA4-PA7 pins the input pull-up option is not available while PA6 and PA7 have additional current driving capability (25mA, 1V). PA0 to PA3 pins are configured as push-pull. Refer to I/O PORT description for additional information.

PB0-PB6. These 7 lines are organized as one I/O port (B). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register. Refer to I/O PORT description and Pin configurations (Figures 1 to 4) for additional information.

PC0-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured as either an input with or without internal pull-up resistor or as an output under software control of the data direction register. Pins PC0 to PC3 are configured as open-drain (5V drive) in output mode while PC4 to PC7 are open-drain with 12V drive and the input pull-up options does not exist on these four pins. PC0, PC1 and PC3 lines when in output mode are "ANDed" with the SPI control signals and are all open-drain. PC0 is connected to the SPI clock signal (SCL), PC1 with the SPI data signal (SDA) while PC3 is connected with SPI enable signal (SEN, used in S-BUS protocol). Pin PC4 and PC6 can also be inputs to software programmable edge sensitive latches which can generate interrupts; PC4 can be connected to Power Interrupt (not available on ST6391 and ST6393) while PC6 can be connected to the IRIN/NMI interrupt line. Refer to I/O PORT description, Pin Configurations (Figures 1 to 4), INTERRUPT description for additional information.

O0, O1. These two lines are available only on ST6394 and ST6396. They are output open-drain pins with 12V drive.

PIN DESCRIPTION (Continued)

DA0-DA5. These pins are the six PWM D/A outputs of the 6-bit on-chip D/A converters. These lines have open-drain outputs with 12V drive. The output repetition rate is 31.25KHz (with 8MHz clock) with the exception of ST6395 which has a repetition rate of 25KHz (with 8MHz clock). Refer to Pin Configurations (Figures 1 to 4) and D/A description for additional information.

AFC. This is the input of the on-chip 10 levels comparator that can be used to implement the AFC function. This pin is an high impedance input able to withstand signals with a peak amplitude up to 12V. Refer to Pin Configurations (Figures 1 to 4) and AFC description for additional information.

OSDOSCIN, OSDOSCOUT. These are the On Screen display oscillator terminals. An oscillation capacitor and coil network have to be connected to provide the right signal to the OSD.

HSYNC, VSYNC. These are the horizontal and vertical synchronization pins. The active polarity of these pins to the OSD macrocell can be selected by the user as ROM mask option. If the device is specified to have negative logic inputs, then when these signals are low the OSD oscillator stops. If the device is specified to have positive logic inputs, then when these signals are high the OSD oscillator stops. Refer to OSD description for additiona information,

R, G, B, BLANK. Outputs from the OSD. R, G and B are the color outputs while BLANK is the blanking output. All outputs are push-pull. The active polarity of these pins to can be selected by the user as ROM mask option. Refer to the pin configurations for additional information.

62.5kHz OUT. This pin is available only on the ST6399. The pin is an open-drain (12V) output at a frequency of 62.5kHz (with an 8MHz clock). The pin can be used to drive the SGS-THOMSON TEA5640 chroma processor. Refer to the TEA5640 data sheet for more information.

Table 2. ST639X Pin Summary

Pin Function	Description
DA0 to DA5	Output, Open-Drain, 12V
62.5KHz OUT	Output, Open-Drain, 12V
PB0-PB6	I/O, Push-Pull, Software Input Pull-up, Schmitt Trigger Input
AFC	Input, High Impedance, 12V
PA0-PA3	I/O, Push-Pull, Software Input Pull-up, Schmitt Trigger Input
PA4-PA5	I/O, Open-Drain, 12V, No Input Pull-up, Schmitt Trigger Input
PA6-PA7	I/O, Open-Drain, 12V, No Input Pull-up, Schmitt Trigger Input, High Drive
O0, 01	Output, Open-Drain, 12V
R,G,B, BLANK	Output, Push-Pull
HSYNC, VSYNC	Input, Pull-up, Schmitt Trigger
OSDOSCIN	Input, High Impedance
OSDOSCOUT	Output, Push-Pull
TEST	Input, Pull-Down
OSCIN	Input, Resistive Bias, Schmitt Trigger to Reset Logic Only
OSCOUT	Output, Push-Pull
RESET	Input, Pull-up, Schmitt Trigger Input
PC4-PC7	I/O, Open-Drain, 12V, No Input Pull-up, Schmitt Trigger Input
PC0-PC3	I/O, Open-Drain, 5V , Software Input Pull-up, Schmitt Trigger Input
V_{DD}, V_{SS}	Power Supply Pins

ST639X CORE

The Core of the ST639X Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control busses. The in-core communication is arranged as shown in the following block diagram figure; the controller being externally linked to both the reset and the oscillator, while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes through the control registers.

Registers

The ST639X Family Core has five registers and three pairs of flags available to the programmer. They are shown in Figure 7 and are explained in the following paragraphs together with the program and data memory page registers.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is addressed in the data space as RAM location at the FFH address.

Figure 7. ST639X Core Programming Model

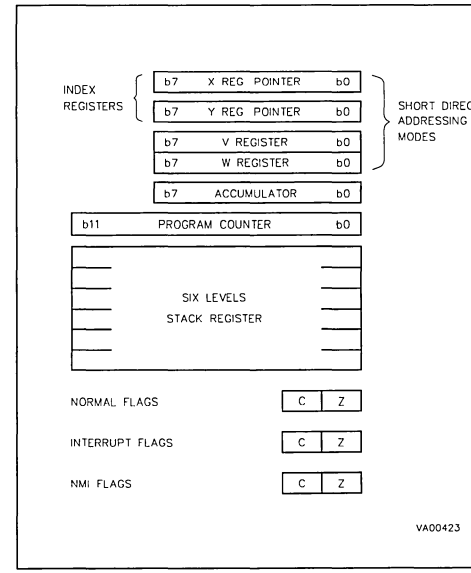
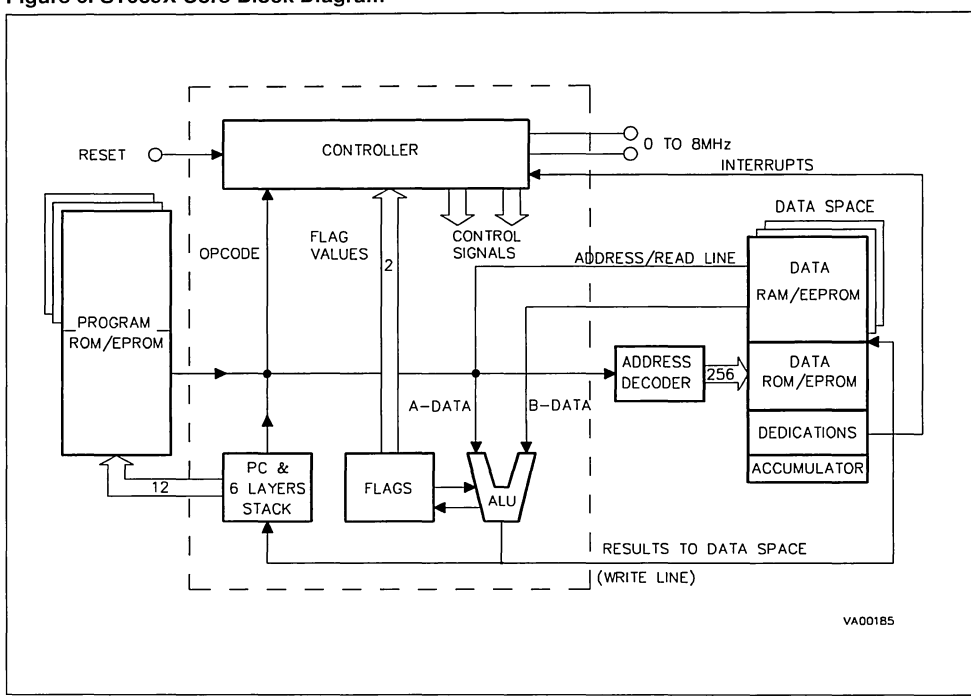


Figure 6. ST639X Core Block Diagram



ST639X CORE (Continued)

Accordingly, the ST639X instruction set can use the accumulator as any other register of the data space.

Indirect Registers (X, Y). These two indirect registers are used as pointers to the memory locations in the data space. They are used in the register-indirect addressing mode.These registers can be addressed in the data space as RAM locations at the 80H (X) and 81H (Y) addresses. They can also be accessed with the direct, short direct, or bit direct addressing modes. Accordingly, the ST639X instruction set can use the indirect registers as any other register of the data space.

Short Direct Registers (V, W). These two registers are used to save one byte in short direct addressing mode. These registers can be addressed in the data space as RAM locations at the 82H (V) and 83H (W) addresses. They can also be accessed with the direct and bit direct addressing modes. Accordingly, the ST639X instruction set can use the short direct registers as any other register of the data space.

Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM location to be processed by the core. This ROM location may be an opcode, an operand, or an address of operand. The 12-bit length allows the direct addressing of 4096 bytes in the program space. Nevertheless, if the program space contains more than 4096 locations, the further program space can be addressed by using the Program Bank Switch register. The PC value is incremented, after it is read for the address of the current instruction, by sending it through the ALU, so giving the address of the next byte in the program. To execute relative jumps the PC and the offset values are shifted through the ALU, where they will be added, and the result is shifted back into the PC. The program counter can be changed in the following ways:

JP (Jump) instruction	PC= Jump address
CALL instruction	PC= Call address
Relative Branch instructions	PC= PC+offset
Interrupt	PC= Interrupt vector
Reset	PC= Reset vector
Test mode	PC=Test mode vector (1)
RET & RETI instructions	PC= Pop (stack)
Normal instruction	PC= PC+1

Note: 1. Not available to the user.

Flags (C, Z)

The ST63 Core includes three pairs of flags that correspond to 3 different modes: normal mode, interrupt mode and Non-Maskable-Interrupt-Mode. Each pair consists of a CARRY flag and a ZERO flag. One pair (CN, ZN) is used during normal operation, one pair is used during the interrupt mode (CI,ZI) and one is used during the not-maskable interrupt mode (CNMI, ZNMI).

The ST63 Core uses the pair of flags that corresponds to the actual mode: as soon as an interrupt (resp. a Non-Maskable-Interrupt) is generated, the ST639X Core uses the interrupt flags (resp. the NMI flags) instead of the normal flags. When the RETI instruction is executed, the normal flags (resp. the interrupt flags) are restored if the MCU was in the normal mode (resp. in the interrupt mode) before the interrupt. Should be observed that each flag set can only be addressed in its own routine (Not-maskable interrupt, normal interrupt or main routine). The interrupt flags are not cleared during the context switching and so, they remain in the state they were at the exit of the last routine switching.

The Carry flag is set when a carry or a borrow occurs during arithmetic operations, otherwise it is cleared. The Carry flag is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

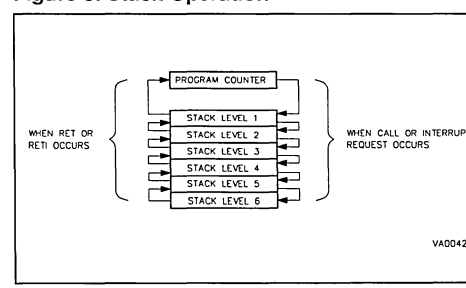
The Zero flag is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

The switching between these three sets is automatically performed when an NMI, an interrupt and a RETI instructions occur. As the NMI mode is automatically selected after the reset of the MCU, the ST639X Core uses at first the NMI flags. Refer to INTERRUPT description for additional information.

Stack

The ST639X Core includes true LIFO hardware stack that eliminates the need for a stack pointer.

Figure 8. Stack Operation

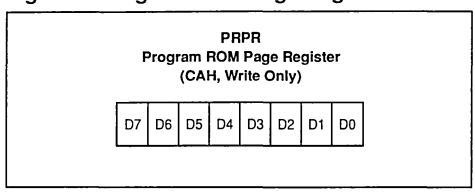


ST639X CORE (Continued)

The stack consists of six separate 12-bit RAM locations that do not belong to the data space RAM area. When a subroutine call (or interrupt request) occurs, the contents of each level is shifted into the next level while the content of the PC is shifted into the first level (the value of the sixth level will be lost). When subroutine or interrupt return occurs (RET or RETI instructions), the first level register is shifted back into the PC and the value of each level is shifted back into the previous level. These two operating modes are described in Figure 8. Since the accumulator, as all other data space registers, is not stored in this stack the handling of this registers shall be performed inside the subroutine. The stack pointer will remain in its deepest position, if more than 6 calls or interrupts are executed, so that the last return address will be lost. It will also remain in its highest position if the stack is empty and a RET or RETI is executed. In this case the next instruction will be executed.

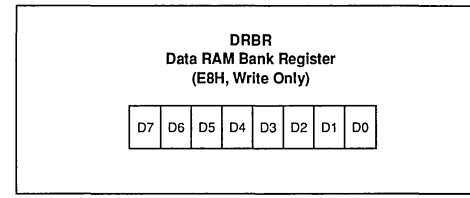
Memory Registers

Figure 9. Program ROM Page Register



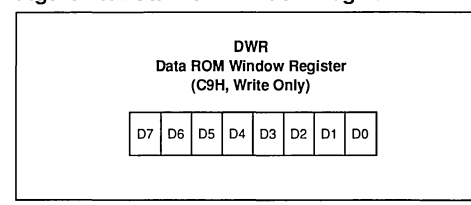
The PRPR register can be addressed like a RAM location in the Data Space at the CAH address; nevertheless it is a write-only register that can not be accessed with single-bit operations. This register is used to select the 2-Kbyte ROM bank of the Program Space that will be addressed. The number of the page has to be loaded in the PRPR register. The PRPR register is not cleared during the MCU initialization and should therefore be defined before jumping out of the static page. Refer to the Program Space description for additional information concerning the use of this registers. The PRPR register is not modified when an interrupt or a subroutine occurs.

Figure 10. Data RAM Bank Register



The DRBR register can be addressed like a RAM location in the Data Space at the E8H address, nevertheless it is write-only register that can not be accessed with single-bit operations. This register is used to select the desired 64-byte RAM/EEPROM bank of the Data Space. The number of the bank has to be loaded in the DRBR register and the instruction has to point to the selected location as it was in the 0 bank (from 00H address to 3FH address). This register is cleared during the MCU initialization (the Data space 0 bank is automatically addressed after the Reset). Refer to the Data Space description for additional information. The DRBR register is not modified when a interrupt or a subroutine occurs.

Figure 11. Data ROM Window Register



The DWR register can be addressed like a RAM location in the Data Space at the C9H address, nevertheless it is write-only register that can not be accessed with single-bit operations. This register is used to move up and down the 64-byte read-only data window (from the 40H address to 7FH address of the Data Space) along the ROM memory of the MCU by step of 64 bytes. The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 less significant bits of the address given in the instruction (as less significant bits) and the content of the DWR register (as most significant bits). Refer to the Data Space description for additional information.

MEMORY SPACES

The MCUs operate in three different memory spaces: Program Space, Data Space, and Stack Space. A description of these spaces is shown in Figure 12 and Figure 13. (Figure 14 refers to the ST6394 which has a total of 8K bytes of ROM).

Figure 12. ST639X Data Space

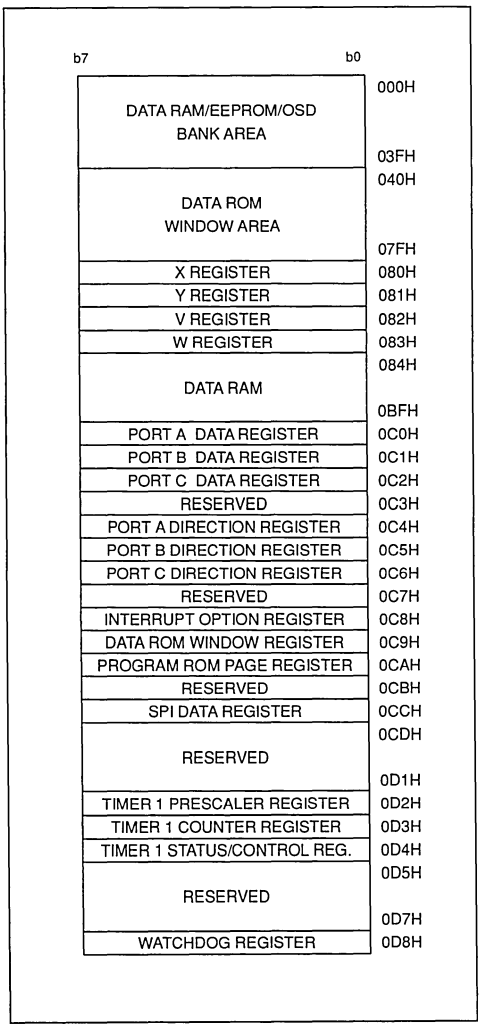
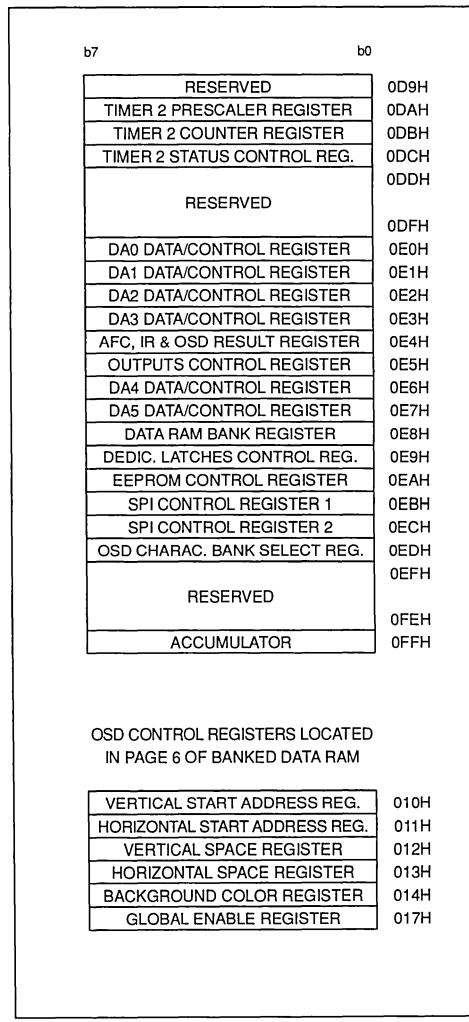
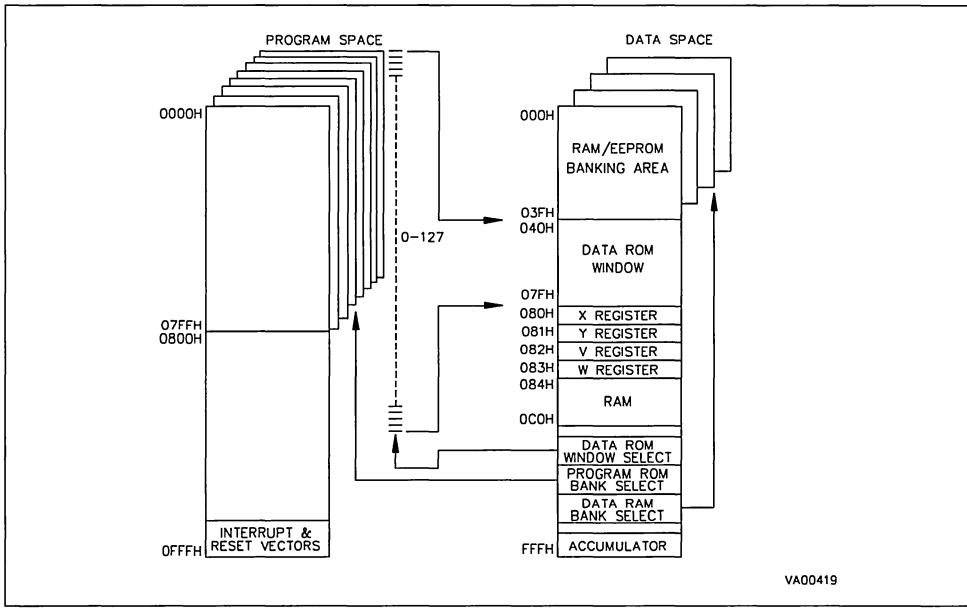


Figure 13. ST639X data Space (Continued)



MEMORY SPACES (Continued)

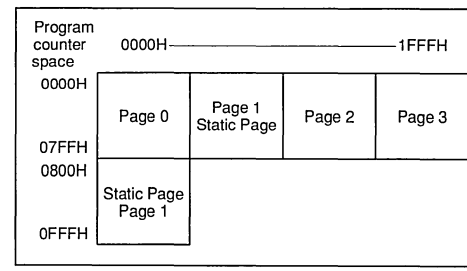
Figure 14. ST6394 Memory Addressing Description Diagram



Program Space

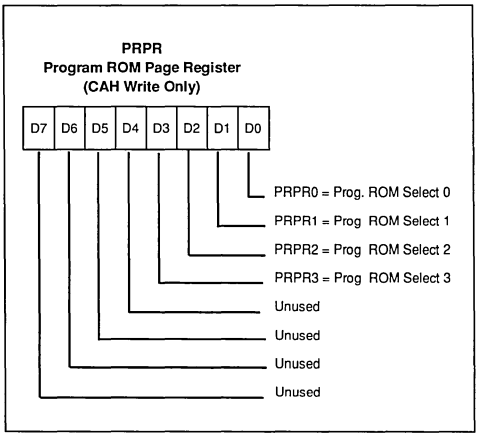
The program space is physically implemented in the ROM memory and includes all the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, the reserved test area and user vectors. It is addressed thanks to the 12-bit Program Counter register (PC register) and so, the ST639X Core can directly address up to 4K bytes of Program Space. Nevertheless, the Program Space can be extended by the addition of 2-Kbyte ROM banks as it is shown in figure 14 in which an 8 Kbyte (as it is in ST6394) memory is described. These banks are addressed by pointing to the 000H-7FFH locations of the Program Space thanks to the Program Counter, and by writing the appropriate code in the Program ROM Page Register (PRPR register) located at the CAH address of the Data Space. Because interrupts and common subroutines should be available all the time only the lower 2K byte of the 4K program space are bank switched while the upper 2K byte can be seen as static space. Table 3 gives the different codes that allows the selection of the corresponding banks. Note that, from the memory point of view, the Page 1 and the Static Page represent the same physical memory: it is only a different way of addressing the same location. On ST6394 a total of 8192 bytes of ROM have been implemented; 7948 are available as user ROM while 244 are reserved for testing. On the ST6391, ST6393 and ST6399 a total of 16384 bytes of ROM have been implemented; 16076 are available as user ROM while 308 are reserved for testing. On the ST6395, ST6396 a total of 20480 bytes of ROM have been implemented; 20140 are available as user ROM while 340 are reserved for testing.

Figure 15. ST6394 8K Bytes Program Space Addressing Description



MEMORY SPACES (Continued)

Figure 16. Program ROM Page Register



D7-D5. These bits are not used.

PRPR4-PRPR0. These are the program ROM banking bits and the value loaded selects the corresponding page to be addressed in the lower part of 4K program address space as specified in Table 3. This register is undefined on reset.

Table 3. ST639X Program ROM Page Register Coding

PRPR3	PRPR2	PRPR1	PRPR0	PC11	Memory Page
X	X	X	X	1	Static Page (Page 1)
0	0	0	0	0	Page 0
0	0	0	1	0	Page 1 (Static Page)
0	0	1	0	0	Page 2
0	0	1	1	0	Page 3
0	1	0	0	0	Page 4
0	1	0	1	0	Page 5
0	1	1	0	0	Page 6
0	1	1	1	0	Page 7
1	0	0	0	0	Page 8
1	0	0	1	0	Page 9

Note. The number of bits implemented depends on the size of the ROM of the device. Only the lower part of address space has been bankswitched because interrupt vectors and common subroutines should be available all the time. The reason of this structure is due to the fact that it is not possible to jump from a dynamic page to another, unless jumping back to the static page, changing contents of PRPR, and, than, jumping to a different dynamic page.

Care is required when handling the PRPR register as it is write only. For this reason, it is not allowed to change the PRPR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. Anyway, this operation may be necessary if the sum of common routines and interrupt drivers will take more than 2K bytes; in this case could be necessary to divide the interrupt driver in a (minor) part in the static page (start and end), and in the second (major) part in one dynamic page. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the PRPR it writes also the image register. The image register must be written first, so if an interrupt occurs between the two instructions the PRPR register is not affected.

MEMORY SPACE (Continued)

Table 4. ST639X Program ROM Memory Map (up to 20K Bytes)

ROM Page	Device Address	EPROM Address (1)	Description
PAGE 0	0000H-007FH 0080H-07FFH	0000H-007FH 0080H-07FFH	Reserved User ROM
PAGE 1 "STATIC"	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	User ROM Reserved Interrupt Vectors Reserved NMI Vector Reset Vector
PAGE 2	0000H-000FH 0010H-07FFH	1000H-100FH 1010H-17FFH	Reserved User ROM
PAGE 3	0000H-000FH 0010H-07FFH	1800H-180FH 1810H-1FFFH	Reserved User ROM (2)
PAGE 4	0000H-000FH 0010H-07FFH	2000H-200FH 2010H-27FFH	Reserved User ROM
PAGE 5	0000H-000FH 0010H-07FFH	2800H-280FH 2810H-2FFFH	Reserved User ROM
PAGE 6	0000H-000FH 0010H-07FFH	3000H-300FH 3010H-37FFH	Reserved User ROM
PAGE 7	0000H-000FH 0010H-07FFH	3800H-380FH 3810H-3FFFH	Reserved User ROM (3)
PAGE 8	0000H-000FH 0010H-07FFH	4000H-400FH 4010H-47FFH	Reserved User ROM
PAGE 9	0000H-000FH 0010H-07FFH	4800H-480FH 4810H-4FFFH	Reserved User ROM (4)

Notes:
1. EPROM addresses are related to the use of ST63P9X piggyback emulation devices.
2. End address for ST6394
3. End address for ST6391,93,99
4. End address for ST6395,96

MEMORY SPACE (Continued)

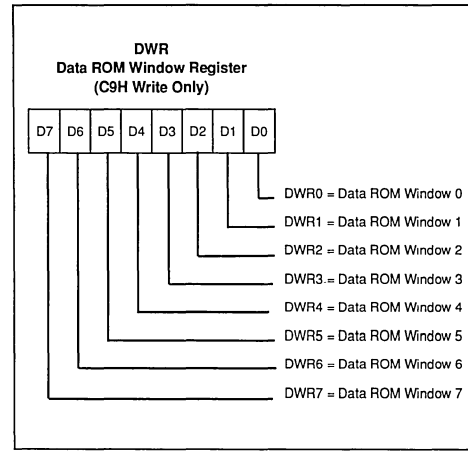
Data Space

The instruction set of the ST639X Core operates on a specific space, named Data Space that contains all the data necessary for the processing of the program. The Data Space allows the addressing of RAM memory (up to 256 bytes for the ST639X family), EEPROM memory (up to 384 bytes for the ST639X family), ST639X Core/peripheral registers, and read-only data such as constants and the look-up tables.

Data ROM Addressing. All the read-only data are physically implemented in the ROM memory in which the Program Space is also implemented. The ROM memory therefore contains the program to be executed and also the constants and the look-up tables needed for the program. The locations of Data Space in which the different constants and look-up tables are addressed by the ST639X Core can be considered as being a 64-byte window through which it is possible to access to the read-only data stored in the ROM memory. This window is located from the 40H address to the 7FH address in the Data space and allows the direct reading of the bytes from the 000H address to the 03FH address in the ROM memory. All the bytes of the ROM memory can be used to store either instructions or read-only data. Indeed, the window can be moved by step of 64 bytes along the ROM memory in writing the appropriate code in the Write-only Data ROM Window register (DWR register, location C9H). The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 less significant bits of the address in the Data Space (as less significant bits) and the content of the DWR register (as most significant bits). So when addressing location 40H of data space, and 0 is loaded in the DWR register, the physical addressed location in ROM is 00H.

Note. The data ROM window cannot address windows above the 16k byte range.

Figure 17. Data ROM Window Register



DWR7-DWR0. These are the Data Rom Window bits that correspond to the upper bits of data ROM program space. The ST6394 is an 8k byte device and as such DWR7 is not used. This register is undefined after reset.

Notes Care is required when handling the DWR register as it is write only. For this reason, it is not allowed to change the DWR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the DWR it writes also the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DWR register is not affected.

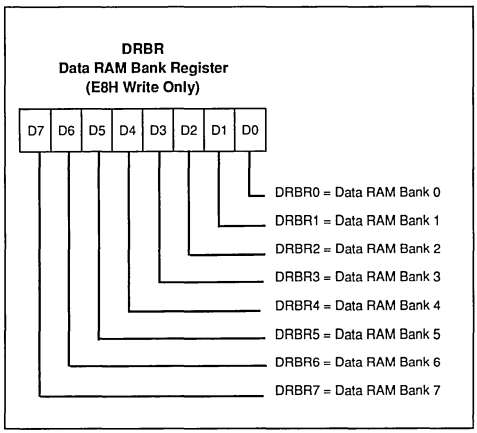
Data RAM/EEPROM/OSD RAM Addressing

In all members of the ST639X family 64 bytes of data RAM are directly addressable in the data space from 80H to BFH addresses. The additional 192 bytes of

MEMORY SPACE (Continued)

RAM (depending on the device), the 384 bytes of EEPROM memory (depending on the device), and the OSD RAM can be addressed using the banks of 64 bytes located between addresses 00H and 3FH. The selection of the bank is done by programming the Data RAM Bank Switching register (DRBR register) located at the E8H address of the Data Space. In this way each bank of RAM, EEPROM or OSD RAM can select 64 bytes at a time. No more than one bank should be set at a time.

Figure 18. Data RAM Bank Register



DRBR7,DRBR1,DRBR0. These bits select the EEPROM pages.

DRBR6, DRBR5. Each of these bits, when set, will select one OSD RAM register page.

DRBR4,DRBR3,DRBR2. Each of these bits, when set, will select one RAM page.

This register is undefined after reset.

Table 5 summarizes how to set the Data RAM Bank Register in order to select the various banks or pages.

Notes :

Care is required when handling the DRBR register as it is write only. For this reason, it is not allowed to change the DWR contents while executing interrupts drivers, as the driver cannot save and than restore its previous content. If it is impossible to avoid the writing of this register in interrupts drivers, an image of this register must be saved in a RAM location, and each time the program writes the DRBR it writes also the image register.

The image register must be written first, so if an interrupt occurs between the two instructions the DRBR register is not affected.

EEPROM Description

The data space of ST639X family from 00H to 3FH is paged as described in Table 5. The ST6391, ST6393 and ST6399 have 128 bytes of EEPROM located in two pages of 64 bytes (pages 0 and 1). The ST6394,ST6395 and ST6396 have 384 bytes of EEPROM located in six pages of 64 bytes (pages 0,1,2,3,4,5 and 6, see Table 5).

Through the programming of the Data RAM Bank Register (DRBR= E8H) the user can select the bank or page leaving unaffected the way to address the

Table 5. Data RAM Bank Register Set-up

DRBR Value	Selection	Applicable Devices
01H	EEPROM Page 0	All Devices
02H	EEPROM Page 1	All Devices
03H	EEPROM Page 2	ST6394, ST6395, ST6396
81H	EEPROM Page 3	ST6394, ST6395, ST6396
82H	EEPROM Page 4	ST6394, ST6395, ST6396
83H	EEPROM Page 5	ST6394, ST6395, ST6396
04H	RAM Page 2	ST6391, ST6393, ST6395, ST6396, ST6399
08H	RAM Page 3	ST6391, ST6393, ST6395, ST6396, ST6399
10H	RAM Page 4	ST6391, ST6393, ST6395, ST6396, ST6399
20H	OSD Page 5	All Devices
40H	OSD Page 6	All Devices

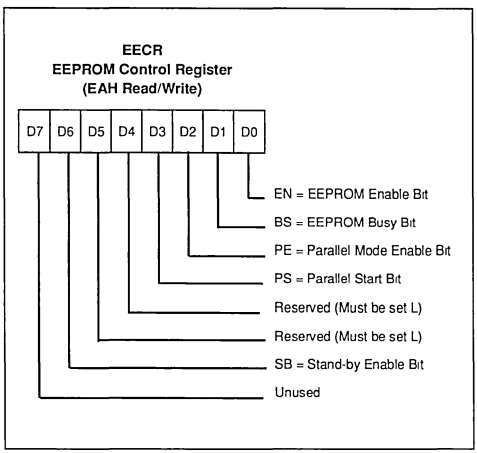
MEMORY SPACE (Continued)

static registers. The way to address the "dynamic" page is to set the DRBR as described in Table 5 (e.g. to select EEPROM page 0, the DRBR has to be loaded with content 01H, see Data RAM/EEPROM/OSD RAM addressing for additional information). Bits 0, 1 and 7 of the DRBR are dedicated to the EEPROM.

The EEPROM module is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. The EEPROM is controlled by the EEPROM Control Register (EECR=EAH). Any EEPROM location can be read just like any other data location, also in terms of access time.

To write an EEPROM location takes about 5 mSec (10mSec max) and during this time the EEPROM is not accessible by the Core. A busy flag can be read by the Core to know the EEPROM status before trying any access. In writing the EEPROM can work in two modes: Byte Mode (BMODE) and Parallel Mode (PMODE). The BMODE is the normal way to use the EEPROM and consists in accessing one byte at a time. The PMODE consists in accessing 8 bytes per time.

Figure 19. EEPROM Control Register



D7. Not used

SB. *WRITE ONLY.* If this bit is set the EEPROM is disabled (any access will be meaningless) and the power consumption of the EEPROM is reduced to the leakage values.

D5, D4. Reserved for testing purposes, they must be set to zero.

PS. *SET ONLY.* Once in Parallel Mode, as soon as the user software sets the PS bit the parallel writing of the 8 adjacent registers will start. PS is internally reset at the end of the programming procedure. Note that less than 8 bytes can be written; after parallel programming the remaining undefined bytes will have no particular content.

PE. *WRITE ONLY.* This bit must be set by the user program in order to perform parallel programming (more bytes per time). If PE is set and the "parallel start bit" (PS) is low, up to 8 adjacent bytes can be written at the maximum speed, the content being stored in volatile registers. These 8 adjacent bytes can be considered as row, whose A7, A6, A5, A4, A3 are fixed while A2, A1 and A0 are the changing bytes. PE is automatically reset at the end of any parallel programming procedure. PE can be reset by the user software before starting the programming procedure, leaving unchanged the EEPROM registers.

BS. *READ ONLY.* This bit will be automatically set by the CORE when the user program modifies an EEPROM register. The user program has to test it before any read or write EEPROM operation; any attempt to access the EEPROM while "busy bit" is set will be aborted and the writing procedure in progress completed.

EN. *WRITE ONLY.* This bit MUST be set to one in order to write any EEPROM register. If the user program will attempt to write the EEPROM when EN= 0 the involved registers will be unaffected and the "busy bit" will not be set.

After RESET the content of EECR register will be 00H.

Notes :
When the EEPROM is busy (BS= 1) the EECR can not be accessed in write mode, it is only possible to read BS status. This implies that as long as the EEPROM is busy it is not possible to change the status of the EEPROM control register. EECR bits 4 and 5 are reserved for testing purposes, and the user must never set them to 1.

Additional Notes on Parallel Mode. If the user wants to perform a parallel programming the first action should be the set to one the PE bit; from this moment the first time the EEPROM will be addressed in writing, the ROW address will be latched and it will be possible to change it only at the end of the programming procedure or by resetting PE without programming the EEPROM. After the ROW address latching the Core can "see" just one EEPROM row (the selected one) and any attempt to write or read other rows will produce errors. Do not read the EEPROM while PR is set.

As soon as PE bit is set, the 8 volatile ROW latches are cleared. From this moment the user can load

MEMORY SPACE (Continued)

data in the whole ROW or just in a subset. PS setting will modify the EEPROM registers corresponding to the ROW latches accessed after PE. For example, if the software sets PE and accesses EEPROM in writing at addresses 18H,1AH,1BH and then sets PS, these three registers will be modified at the same time; the remaining bytes will have no particular content. Note that PE is internally reset at the end of the programming procedure. This implies that the user must set PE bit between two parallel programming procedures. Anyway the user can set and then reset PE without performing any EEPROM programming. PS is a set only bit and is internally reset at the end of the programming procedure. Note that if the user tries to set PS while PE is not set there will not be any programming procedure and the PS bit will be unaffected. Consequently PS bit can not be set if EN is low. PS can be affected by the user set if, and only if, EN and PE bits are also set to one.

Warning : *Parallel programming of the EEPROM with less than eight bytes may corrupt other bytes and should therefore be used with care, as here after underlined.*

a. *Reason for limitation:*
betweeen PE (Parallel Enable) and PS (Parallel Start) of the EEPROM, the user writes up to eight bytes into the volatile data registers, a latch is also set to indicate which bytes have been accessed; the accessed bytes will be programmed when PS arrives. The logic is such that it is possible to set the latches of bytes which have NOT been accessed. The latches are set whenever ANY register in the banked dataspace (00h-3FH) is accessed for READ or WRITE between a PE and PS. The latch which is set will be determined by the three least significant bits of the register address. Only the latch is set, so final data of a corrupted byte after the parallel programming is always FFH.

Note: *read operations also occur internally to the micro for most instructions. Even if bytes are not seen to be corrupted within the parallel programming routine, care should be taken, since they could become corrupted by an interrupt routine being serviced during loading of parallel bytes.*
This is logic related and is not a marginality or race condition; piggyback devices perform in the same way as ROM devices. Parallel programming is tested with only LDI rr,nn instructions which do not corrupt other bytes.

b. *To Avoid Corrupted Bytes:*
- *use Single Byte Mode, or*
- *always define all eight bytes in Parallel Programming Mode, or*
- *when programming less than eight bytes, the remaining EEPROM bytes should do not used by the program.*

Additional Notes Regarding Differences Between ST639X Devices and Corresponding Emulators. While PE is set, all the EEPROM page currently selected is accessible in reading and the writing of the bytes happens at the row to which belongs the last byte written before setting PS. The sequence: set PE, write in 10H the value X, write in 21H the value Y, set PS, will result in: 10H unchanged, 20H loaded with value X, 21H loaded with value Y. In the emulator bits 4 and 5 of the EECR are implemented.If the user set to 1 one or both of these bits the contents of the EEPROM will be destroyed. The user should use care in using EEPROM emulation as in general the emulator does not emulate the behaviour of the EEPROM when it is misused.

STACK SPACE

The stack space consists of six 12 bit registers that are used for stacking subroutine and interrupt return addresses plus the current program counter register.

TEST MODE

The test mode can be entered by connecting the TEST pin to an high logic level when reset is active; this action enables the factory test mode. The user is recommended to avoid this situation for normal operation. (TEST pin should be tied to ground).

INTERRUPT

The ST639X Core can manage 4 different maskable interrupt sources, plus one non-maskable interrupt source (top priority level interrupt). Each source is associated with a particular interrupt vector that contains a Jump instruction to the related interrupt service routine. Each vector is located in the Program Space at a particular address (see Table 6). When a source provides an interrupt request, and the request processing is also enabled by the ST639X Core, then the PC register is loaded with the address of the interrupt vector (i.e. of the Jump instruction). Finally, the PC is loaded with the address of the Jump instruction and the interrupt routine is processed.

The relationship between vector and source and the associated priority is hardware fixed for the different ST639X devices. For some interrupt sources it is also possible to select by software the kind of event that will generate the interrupt.

All interrupts can be disabled by writing to the GEN bit (global interrupt enable) of the interrupt option register (address C8H). After a reset, ST639X is in non maskable interrupt mode, so no interrupts will be accepted and NMI flags will be used, until a RETI

INTERRUPT (Continued)

instruction is executed. If an interrupt is executed, one special cycle is made by the core, during that the PC is set to the related interrupt vector address. A jump instruction at this address has to redirect program execution to the beginning of the related interrupt routine. The interrupt detecting cycle, also resets the related interrupt flag (not available to the user), so that another interrupt can be stored for this current vector, while its driver is under execution.

If additional interrupts arrive from the same source, they will be lost. NMI can interrupt other interrupt routines at any time, while other interrupts cannot interrupt each other. If more than one interrupt is waiting for service, they are executed according to their priority. The lower the number, the higher the priority. Priority is, therefore, fixed. Interrupts are checked during the last cycle of an instruction (RETI included). Level sensitive interrupts have to be valid during this period.

Table 6 details the different interrupt vectors/sources relationships.

Table 6. Interrupt Vectors/Sources Relationships

Interrupt Source	Associated Vector	Vector Address
PC6/IRIN Pin (1)	Interrupt Vector # 0 (NMI)	0FFCH-0FFDH
Timer 2	Interrupt Vector # 1	0FF6H-0FF7H
Vsync	Interrupt Vector # 2	0FF4H-0FF5H
Timer 1	Interrupt Vector # 3	0FF2H-0FF3H
PC4/PWRIN	Interrupt Vector # 4	0FF0H-0FF1H

Note: 1. This pin is associated with the NMI Interrupt Vector

Interrupt Vectors/Sources

The ST639X Core includes 5 different interrupt vectors in order to branch to 5 different interrupt routines. The interrupt vectors are located in the fixed (or static) page of the Program Space.

The interrupt vector associated with the non-maskable interrupt source is named interrupt vector #0. It is located at the (FFCH,FFDH) addresses in the Program Space. This vector is associated with the PC6/IRIN pin; refer to the ST639X Interrupt Details section for more information.

The interrupt vectors located at addresses (FF6H,FF7H), (FF4H,FF5H), (FF2H,FF3H), (FF0H,FF1H) are named interrupt vectors #1, #2, #3 and #4 respectively. These vectors are associated with TIMER 2 (#1), VSYNC (#2), TIMER 1 (#3) and PC4(PWRIN) (#4); refer to the ST639X Interrupt Details description for more information.

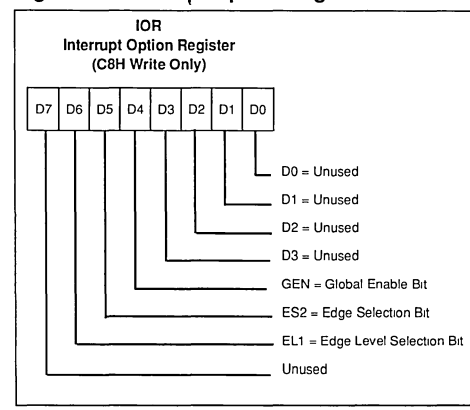
Interrupt Priority

The non-maskable interrupt request has the highest priority and can interrupt any other interrupt routines at any time, nevertheless the other interrupts cannot interrupt each other. If more than one interrupt request is pending, they are processed by the ST639X Core according to their priority level: vector #1 has the higher priority while vector #4 the lower. The priority of each interrupt source is hardware fixed.

Interrupt Option Register

The Interrupt Option Register (IOR register, location C8H) is used to enable/disable the individual interrupt sources and to select the operating mode of the external interrupt inputs. This register can be addressed in the Data Space as RAM location at the C8H address, nevertheless it is write-only register that can not be accessed with single-bit operations. The operating modes of the external interrupt inputs associated to interrupt vectors #1 and #2 are selected through bits 4 and 5 of the IOR register.

Figure 20. Interrupt Option Register



D7. Not used.

EL1. This is the Edge/Level selection bit of interrupt #1. When set to one, the interrupt is generated on low level of the related signal; when cleared to zero, the interrupt is generated on falling edge. The bit is cleared to zero after reset.

ES2. This is the edge selection bit on interrupt #2. This bit is used on the ST639X devices with on-chip OSD generator for VSYNC detection.

INTERRUPT (Continued)

GEN. This is the global enable bit. When set to one all interrupts are globally enabled; when this bit is cleared to zero all interrupts are disabled (including NMI).

D3 - D0. These bits are not used.

Interrupt Procedure

The interrupt procedure is very similar to a call procedure; the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event the user does not know about the context and the time at which it occurred. As a result the user should save all the data space registers which will be used inside the interrupt routines. There are separate sets of processor flags for normal, interrupt and non-maskable interrupt modes which are automatically switched and so these do not need to be saved.

The following list summarizes the interrupt procedure (refer also to Figure 21. Interrupt Processing Flow Chart):

- Interrupt detection
- The flags C and Z of the main routine are exchanged with the flags C and Z of the interrupt routine (resp. the NMI flags)
- The value of the PC is stored in the first level of the stack - The normal interrupt lines are inhibited (NMI still active)
- The edge flip-flop is reset
- The related interrupt vector is loaded in the PC.
- User selected registers are saved inside the interrupt service routine (normally on a software stack)
- The source of the interrupt is found by polling (if more than one source is associated to the same vector)
- Interrupt servicing
- Return from interrupt (RETI)
- Automatically the ST639X core switches back to the normal flags (resp the interrupt flags) and pops the previous PC value from the stack

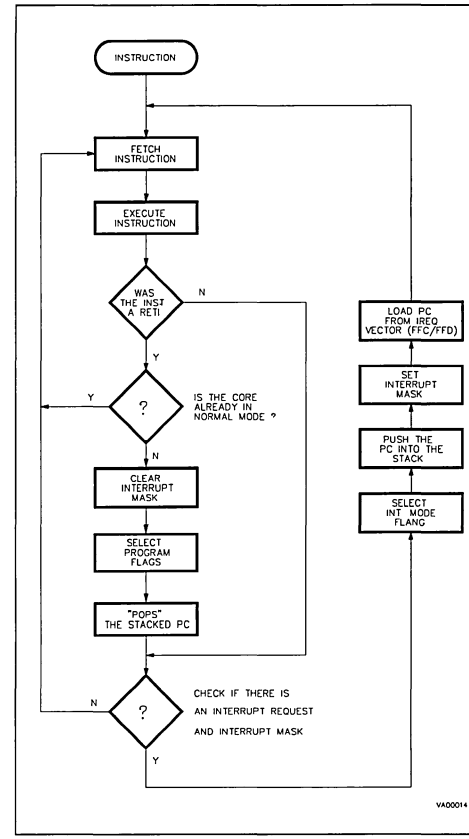
The interrupt routine begins usually by the identification of the device that has generated the interrupt request. The user should save the registers which are used inside the interrupt routine (that holds relevant data) into a software stack.
After the RETI instruction execution, the Core carries out the previous actions and the main routine can continue.

ST639X Interrupt Details

IR Interrupt (#0). The IRIN/PC6 Interrupt is connected to the first interrupt #0 (NMI, 0FFCH). If the $\overline{\text{IRINT}}$ interrupt is disabled at the Latch circuitry, then it will be high. The #0 interrupt input detects a high to low level. Note that once #0 has been latched, then the only way to remove the latched #0 signal is to service the interrupt. #0 can interrupt the other interrupts. A simple latch is provided from the PC6(IRIN) pin in order to generate the $\overline{\text{IRINT}}$ signal. This latch can be triggered by either the positive or negative edge of IRIN signal. $\overline{\text{IRINT}}$ is inverted with respect to the latch. The latch can be read by software and reset by software.

TIMER 2 Interrupt (#1). The TIMER 2 Interrupt is connected to the interrupt #1 (0FF6H). The TIMER 2 interrupt generates a low level (which is latched in the timer). For more information on the timer interrupt refer to the timer section. Either the low level or negative edge selection for #1 can be used. Bit 6 of the interrupt option register C8H is used to select negative edge (B1=0) or low level (B1=1) interrupts. Note that once a negative edge has been latched, then the only way to remove the latched signal is to service the interrupt.

Figure 20. Interrupt Processing Flow-Chart



INTERRUPT (Continued)

VSYNC Interrupt (#2). The VSYNC Interrupt is connected to the interrupt #2. When disabled the VSYNCINT signal is low. The VSYNCINT signal is inverted with respect to the signal applied to the VSYNCN pin. Bit 5 of the interrupt option register C8H is used to select the negative edge (B2=0) or the positive edge (B2=1); the edge will depend on the application. Note that once an edge has been latched, then the only way to remove the latched signal is to service the interrupt. Care must be taken not to generate spurious interrupts. This interrupt may be used for synchronize to the VSYNC signal in order to change characters in the OSD only when the screen is on vertical blanking (if desired). This method may also be used to blink characters.

TIMER 1 Interrupt (#3). The TIMER 1 Interrupt is connected to the fourth interrupt #3 (0FF2H) which detects a high to low level (latched in the timer). For more information on the timer interrupt refer to the timer section.

PWR Interrupt (#4). The PWR Interrupt is connected to the fifth interrupt #4 (0FF0H). If the PWRINTN is disabled at the PWR circuitry, then it will be high. The #4 interrupt input detects a low level. This interrupt is not available on the ST6391 and ST6393. A simple latch is provided from the PC4 (PWRIN)pin in order to generate the PWRINTN signal. This latch can be triggered by either the positive or negative edge of the PWRIN signal. PWRINTN is inverted with respect to the latch. The latch can be reset by software.

Notes Global disable does not reset edge sensitive interrupt flags. These edge sensitive interrupts become pending again when global disabling is released. Moreover, edge sensitive interrupts are stored in the related flags also when interrupts are globally disabled, unless each edge sensitive interrupt is also individually disabled before the interrupting event happens. Global disable is done by clearing the GEN bit of Interrupt option register, while any individual disable is done in the control register of the peripheral. The on-chip Timer peripherals have an interrupt request flag bit (TMZ), this bit is set to one when the device wants to generate an interrupt request and a mask bit (ETI) that must be set to one to allow the transfer of the flag bit to the Core.

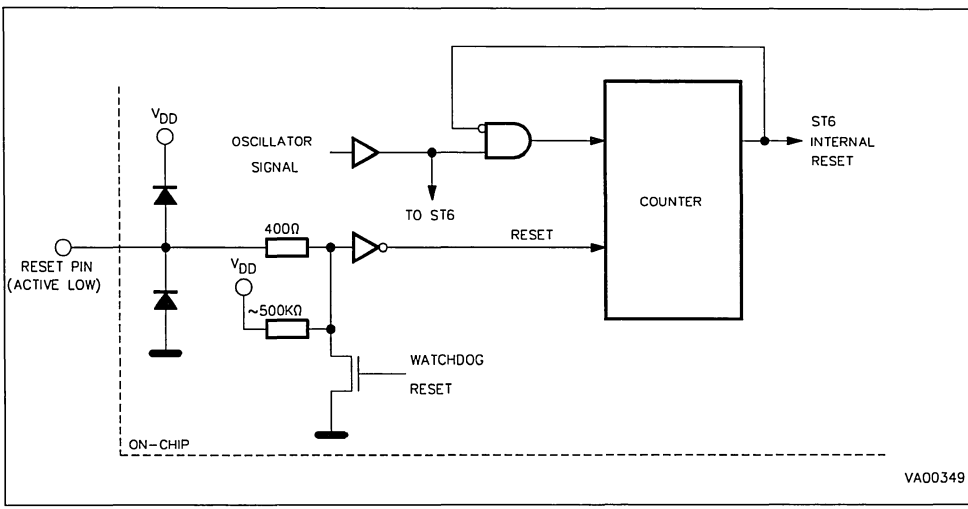
RESET

The ST639X devices can be reset in two ways: by the external reset input (RESET) tied low and by the hardware activated digital watchdog peripheral.

RESET Input

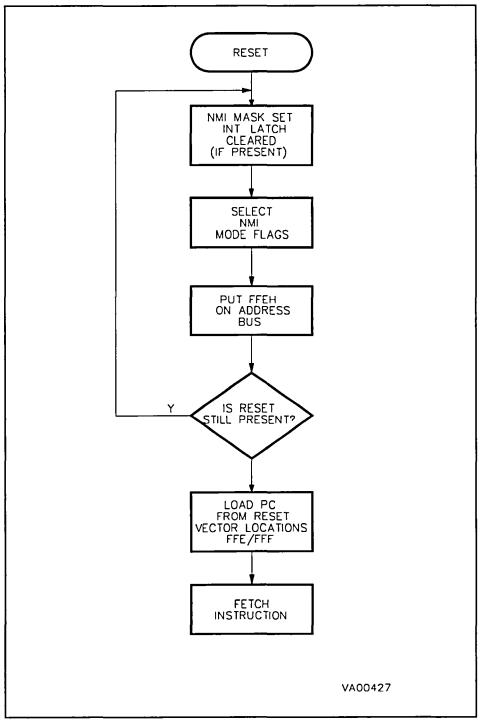
The external active low reset pin is used to reset the ST639X devices and provide an orderly software startup procedure. The activation of the Reset pin may occur at any time in the RUN or WAIT mode. Even short pulses at the reset pin will be accepted since the reset signal is latched internally and is only cleared after 2048 clocks at the oscillator pin. The clocks from the oscillator pin to the reset circuitry are buffered by a schmit trigger so that an oscillator in start-up conditions will not give spurious clocks. When the reset pin of the ST6394, ST6396 and ST6399 is

Figure 22. Internal Reset Circuit



RESET (Continued)

Figure 23. Reset & Interrupt Processing Flow-chart

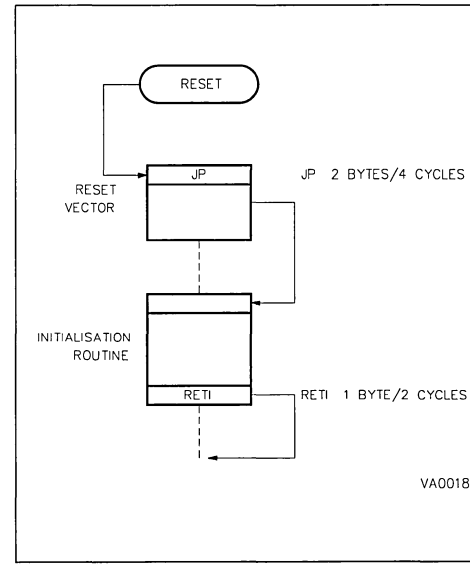


held low, the external quartz oscillator is also disabled in order to reduce current consumption. The MCU is configured in the Reset mode as long as the signal of the RESET pin is low. The processing of the program is stopped and the standard Input/Output ports (port A, port B and port C) are in the input state. As soon as the level on the reset pin becomes high, the initialization sequence is executed. Refer to the MCU initialization sequence for additional information.

Watchdog Reset

The ST639X devices are provided with an on-chip hardware activated digital watchdog function in order to provide a graceful recovery from a software upset. If the watchdog register is not refreshed and the end-of-count is reached, then the reset state will be latched into the MCU and an internal circuit pulls down the reset pin. This also resets the watchdog which subsequently turns off the pull-down and activates the pull-up device at the reset pin. This causes the positive transition at

Figure 24. Restart Initialization Program Flow-chart



the reset pin. The MCU will then exit the reset state after 2048 clocks on the oscillator pin.

Application Notes

An external resistor between V_{DD} and the reset pin is not required because an internal pull-up device is provided. The user may prefer to add an external pull-up resistor.

An internal Power-on device does not guarantee that the MCU will exit the reset state when V_{DD} is above 4.5V and therefore the RESET pin should be externally controlled.

MCU Initialization Sequence

When a reset occurs the stack is reset to program counter, the PC is loaded with the address of the reset vector (located in the program ROM at addresses FFEH & FFFH). A jump instruction to the beginning of the program has to be written into these locations.After a reset the interrupt mask is automatically activated so that the Core is in non-maskable interrupt mode to prevent false or ghost interrupts during the restart phase. Therefore the restart routine should be terminated by a RETI instruction to switch to normal mode and enable interrupts. If no pending interrupt is present at the end of the reset routine, the ST639X will continue with the instruction after the RETI; otherwise the pending interrupt will be serviced.

RESET (Continued)

RESET Low Power Mode

The ST6394/96 and ST6399 have a special low power mode when the reset pin is held low. When the reset pin is low, the quartz oscillator is Disabled allowing reduced current consumption. When the reset pin is raised the quartz oscillator is enabled and oscillations will start to build up.The internal reset circuitry will count 2048 clocks on the oscillator pin before allowing the MCU to go out of the reset state;the clocks are after a schmtit trigger so that false or multiple counts are not possible.

WAIT & STOP MODES

The STOP and WAIT modes have been implemented in the ST639X Core in order to reduce the consumption of the device when the latter has no instruction to execute. These two modes are described in the following paragraphs. On ST639X as the hardware activated digital watchdog function is present the STOP instruction is de-activated and any attempt to execute it will cause the automatic execution of a WAIT instruction.

WAIT Mode

The configuration of the MCU in the WAIT mode occurs as soon as the WAIT instruction is executed. The microcontroller can also be considered as being in a "software frozen" state where the Core stops processing the instructions of the routine, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage but where the peripherals are still working.
The WAIT mode is used when the user wants to reduce the consumption of the MCU when it is in idle, while not loosing count of time or monitoring of external events. The oscillator is not stopped in order to provide clock signal to the peripherals. The timers counting may be enabled (writing the PSI bit in TSCR register) and the timer interrupt may be also enabled before entering the WAIT mode; this allows the WAIT mode to be left when timer interrupt occurs. If the exit from the WAIT mode is performed with a general RESET (either from the activation of the external pin or by watchdog reset) the MCU will enter a normal reset procedure as described in the RESET chapter. If an interrupt is generated during WAIT mode the MCU behaviour depends on the state of the ST639X Core before the initialization of the WAIT sequence, but also of the kind of the interrupt request that is generated. This case will be described in the following paragraphs. In any case, the ST639X Core does not generate any delay after the occurrence of the interrupt because the oscillator clock is still available.

STOP Mode

On ST639X the hardware watchdog is present and the STOP instruction has been de-activated. Any attempt to execute a STOP will cause the automatic execution of a WAIT instruction.

Exit from WAIT Mode

The following paragraphs describe the output procedure of the ST639X Core from WAIT mode when an interrupt occurs. It must be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non-maskable interrupt mode) before the start of the WAIT sequence, but also of the type of the interrupt request that is generated:

Normal Mode. If the ST639X Core was in the main routine when the WAIT instruction has been executed, the ST639X Core outputs from the wait mode as soon as any interrupt occurs; the related interrupt routine is executed and at the end of the interrupt service routine the instruction that follows the WAIT instruction is executed if no other interrupts are pending.

Non-maskable Interrupt Mode. If the WAIT instruction has been executed during the execution of the non-maskable interrupt routine, the ST639X Core outputs from the wait mode as soon as any interrupt occurs: the instruction that follows the WAIT instruction is executed and the ST639X Core is still in the non-maskable interrupt mode even if an other interrupt has been generated.

Normal Interrupt Mode. If the ST639X Core was in the interrupt mode before the initialization of the WAIT sequence, it outputs from the wait mode as soon as any interrupt occurs. Nevertheless, two cases have to be considered:

- If the interrupt is a normal interrupt, the interrupt routine in which the WAIT was entered will be completed with the execution of the instruction that follows the WAIT and the ST639X Core is still in the interrupt mode. At the end of this routine pending interrupts will be serviced in accordance to their priority.
- If the interrupt is a non-maskable interrupt, the non-maskable routine is processed at first. Then, the routine in which the WAIT was entered will be completed with the execution of the instruction that follows the WAIT and the ST639X Core is still in the normal interrupt mode.

Notes :
If all the interrupt sources are disabled, the restart of the MCU can only be done by a Reset activation. The Wait instruction is not executed if an enabled interrupt request is pending. In the ST639X the hardware activated digital watchdog function is present. As the watchdog is always activated the STOP instruction is de-activated and any attempt to execute the STOP instruction will cause an execution of a WAIT instruction.

ON-CHIP CLOCK OSCILLATOR

The internal oscillator circuit is designed to require a minimum of external components. A crystal quartz, a ceramic resonator, or an external signal (provided to the OSCIN pin) may be used to generate a system clock with various stability/cost tradeoffs. The typical clock frequency is 8MHz. Please note that different frequencies will affect the operation of those peripherals (D/As, SPI, 62.5 KHz OUT) whose reference frequencies are derived from the system clock.

The different clock generator options connection methods are shown in Figure 25, crystal specifications and suggested PC board layouts are given in Figure 26 and Figure 27. One machine cycle takes 13 oscillator pulses; 12 clock pulses are needed to increment the PC while and additional 13th pulse is needed to stabilize the internal latches during memory addressing. This means that with a clock frequency of 8MHz the machine cycle is 1.625µSec.

The crystal oscillator start-up time is a function of many variables: crystal parameters (especially RS), oscillator load capacitance (CL), IC parameters, ambient temperature, and supply voltage.It must be observed that the crystal or ceramic leads and circuit connections must be as short as possible. Typical values for CL1 and CL2 are in the range of 15pF to 22pF but these should be chosen based on the crystal manufacturers specification. Typical input capacitance for OSCIN and OSCOUT pins is 5pF.

The oscillator output frequency is internally divided by 13 to produce the machine cycle and by 12 to produce the Timer and the Watchdog clock. A byte cycle is the smallest unit needed to execute any operation (i.e., increment the program counter). An instruction may need two, four, or five byte cycles to be executed (See Table 7).

Table 7. Instructions Timing with 8MHz Clock

Instruction Type	Cycles	Execution Time
Branch if set/reset	5 Cycles	8.125µs
Branch & Subroutine Branch	4 Cycles	6.50µs
Bit Manipulation	4 Cycles	6.50µs
Load Instruction	4 Cycles	6.50µs
Arithmetic & Logic	4 Cycles	6.50µs
Conditional Branch	2 Cycles	3.25µs
Program Control	2 Cycles	3.25µs

Figure 25. Clock Generator Options

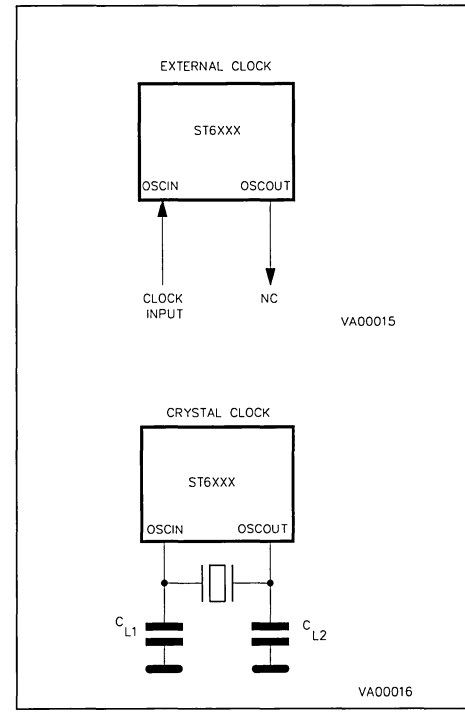
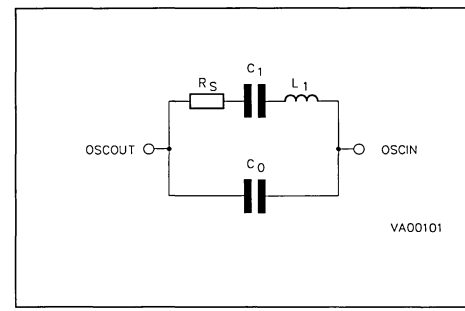


Figure 26. Crystal Parameters



ON-CHIP CLOCK OSCILLATOR (Continued)

Figure 27. PC Board Layouts Examples

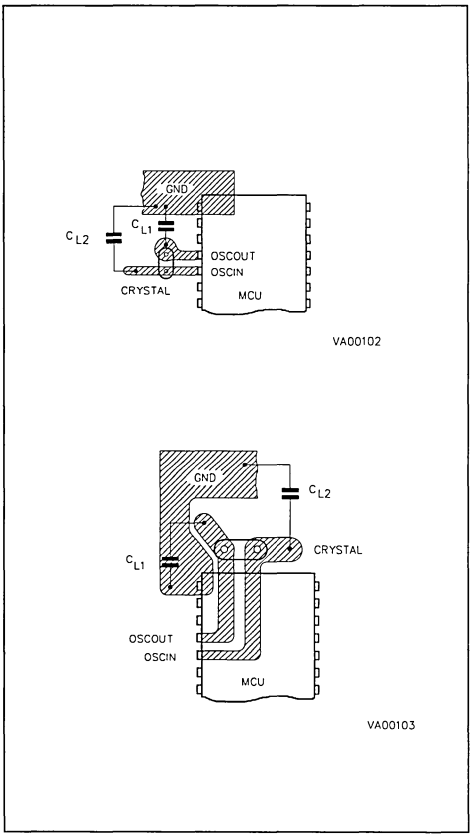
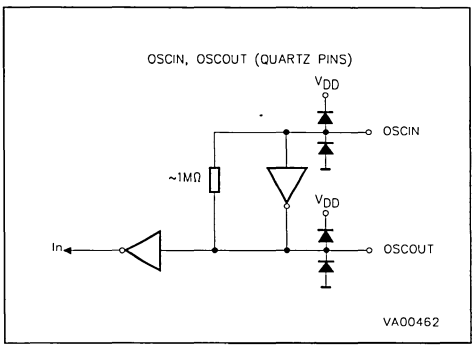


Figure 28. OSCIN, OSCOUT Configuration Diagram



INPUT/OUTPUT PORTS

The ST639X microcontrollers use three standard I/O ports (A,B,C) with up to eight pins on each port; refer to the device pin configurations to see which pins are available.

Each line can be individually programmed either in the input mode or the output mode as follows by software.

- Output
- Input with on-chip pull-up resistor (selected by software)
- Input without on-chip pull-up resistor (selected by software)

Note: pins with 12V open-drain capability do not have pull-up resistors.

In output mode the following hardware configurations are available:

- Open-drain output 12V (PA4-PA7, PC4-PC7)
- Open-drain output 5V (PC0-PC3)
- Push-pull output (PA0-PA3, PB0-PB6)

The lines are organized in three ports (port A,B,C). The ports occupies 6 registers in the data space. Each bit of these registers is associated with a particular line (for instance, the bits 0 of the Port A Data and Direction registers are associated with the PA0 line of Port A).

There are three Data registers (DRA, DRB, DRC), that are used to read the voltage level values of the lines programmed in the input mode, or to write the logic value of the signal to be output on the lines configured in the output mode. The port Data Registers can be read to get the effective logic levels of the pins, but they can be also written by the user software, in conjunction with the related Data Direction Register, to select the different input mode options. Single-bit operations on I/O registers (bit set/reset instructions) are possible but care is necessary because reading in input mode is done from I/O pins and therefore they might be influenced by the external load, while writing will directly affect the Port data register causing an undesired changes of the input configuration. The three Data Direction registers (DDRA, DDRB,DDRB) allow the selection of the direction of each pin (input or output).

All the I/O registers can be read or written as any other RAM location of the data space, so no extra RAM cell is needed for port data storing and manipulation. During the initialization of the MCU, all the I/O registers are cleared and the input mode with pull-up is selected on all the pins thus avoiding pin conflicts (with the exception of PC2 that is set in output mode and is set high ie. high impedence).

INPUT/OUTPUT PORTS (Continued)

Details of I/O Ports

When programmed as an input a pull-up resistor (if available) can be switched active under program control. When programmed as an output the I/O port will operate either in the push-pull mode or the open-drain mode according to the hardware fixed configuration as specified below.

Port A. PA0-PA3 are available as push-pull when outputs. PA4-PA7 are available as open-drain (no push-pull programmability) capable of withstanding 12V (no resistive pull-up in input mode). PA6-PA7 has been specially designed for higher driving capability and are able to sink 25mA with a maximum VOL of 1V.

Port B. All lines are configured as push-pull when outputs.

Port C. PC0-PC3 are available as open-drain capable of withstanding a maximum V_{DD}+0.3V. PC4-PC7 are available as open-drain capable of withstanding 12V (no resistive pull-up in input mode). Some lines are also used as I/O buffers for signals coming from the on-chip SPI.

In this case the final signal on the output pin is equivalent to a wired AND with the programmed data output.

If the user needs to use the serial peripheral, the I/O line should be set in output mode while the open-drain configuration is hardware fixed; the corresponding data bit must set to one. If the latched interrupt functions are used (IRIN, PWRIN) then the corresponding pins should be set to input mode.

On ST639X the I/O pins with double or special functions are:

- PC0/SCL (connected to the SPI clock signal)
- PC1/SDA (connected to the SPI data signal)
- PC3/SEN (connected to the SPI enable signal)
- PC4/PWRIN (connected to the PWRIN interrupt latch)
- PC6/IRIN (connected to the IRIN interrupt latch)

All the Port A,B and C I/O lines have Schmitt-trigger input configuration with a typical hysteresis of 1V.

I/O Pin Programming

Each pin can be individually programmed as input or output with different input and output configurations.

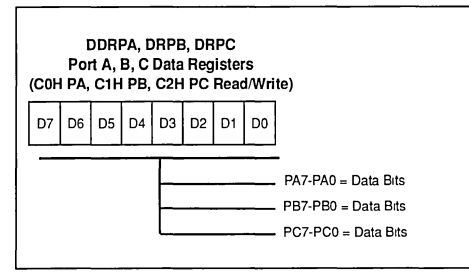
This is achieved by writing to the relevant bit in the data (DR) and data direction register (DDR). Table 8 shows all the port configurations that can be selected by the user software.

Table 8. I/O Port Options Selection

DDR	DR	Mode	Option
0	0	Input	With on-chip pull-up resistor
0	1	Input	Without on-chip pull-up resistor
1	X	Output	Open-drain or Push-Pull

Note. X: Means don't care

Figure 29. I/O Port Data Registers

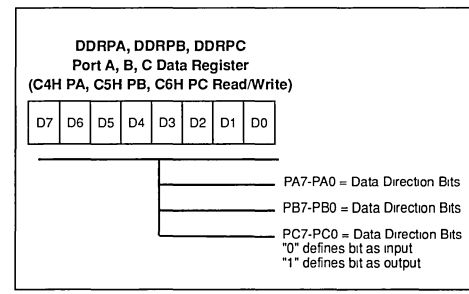


PA7-PA0. These are the I/O port A data bits. Reset at power-on.

PB7-PB0. These are the I/O port B data bits. Reset at power-on.

PC7-PC0. Set to 04H at power-on. Bit 2 (PC2 pin) is set to one (open drain therefore high impedence).

Figure 30. I/O Port Data Direction Registers



PA7-PA0. These are the I/O port A data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Reset at power-on.

PB7-PB0. These are the I/O port B data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Reset at power-on.

INPUT/OUTPUT PORTS (Continued)

PC7-PC0. These are the I/O port C data direction bits. When a bit is cleared to zero the related I/O line is in input mode, if bit is set to one the related I/O line is in output mode. Set to 04H at power-on. Bit 2 (PC2 pin) is set to one (output mode selected).

Input/Output Configurations

The following schematics show the I/O lines hardware configuration for the different options. Figure 31 shows the I/O configuration for an I/O pin with open-drain 12V capability (standard drive and high drive). Figure 31 shows the I/O configuration for an I/O pin with push-pull and with open drain 5V capability.

Notes :
The WAIT instruction allows the ST639X to be used in situations where low power consumption is needed. This can only be achieved however if the I/O pins either are programmed as inputs with well defined logic levels or have no power consuming resistive loads in output mode. As the same die is used for the different ST639X versions the unavailable I/O lines of ST639X should be programmed in output mode.

Single-bit operations on I/O registers are possible but **care is necessary** because reading in input mode is done from I/O pins while writing will directly affect the Port data register causing an undesired changes of the input configuration.

Figure 32. I/O Configuration Diagram (Open Drain 12V)

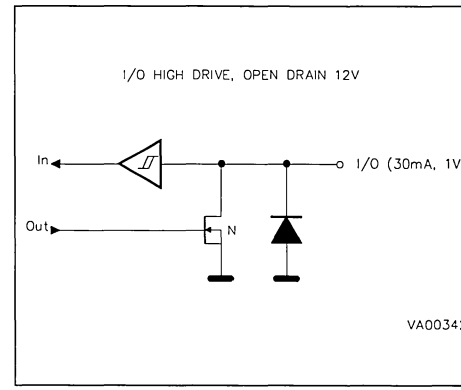
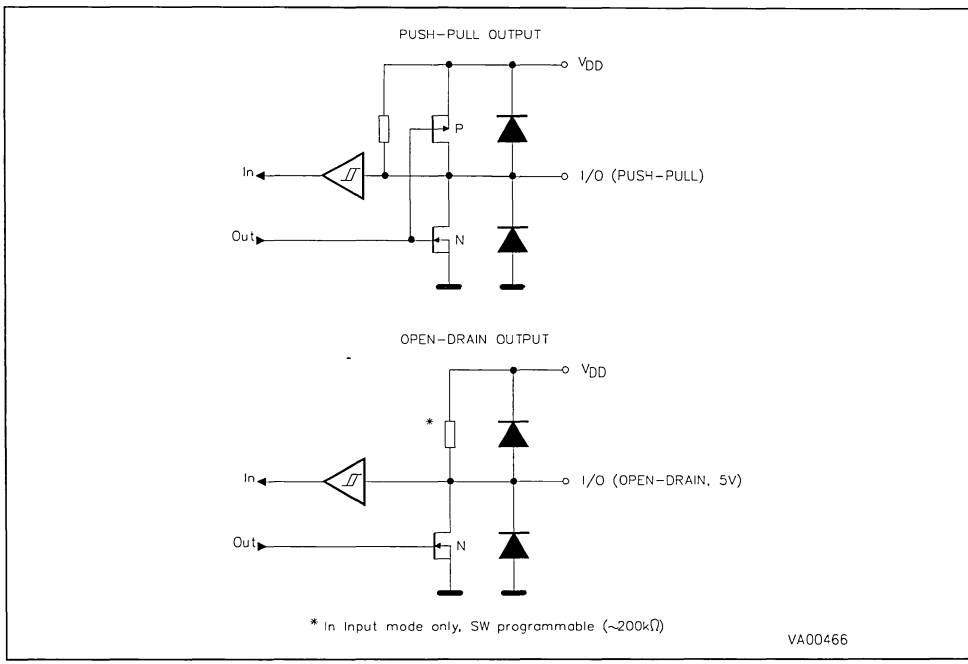


Figure 31. I/O Configuration Diagram (Open Drain 5V, Push-pull)



TIMERS

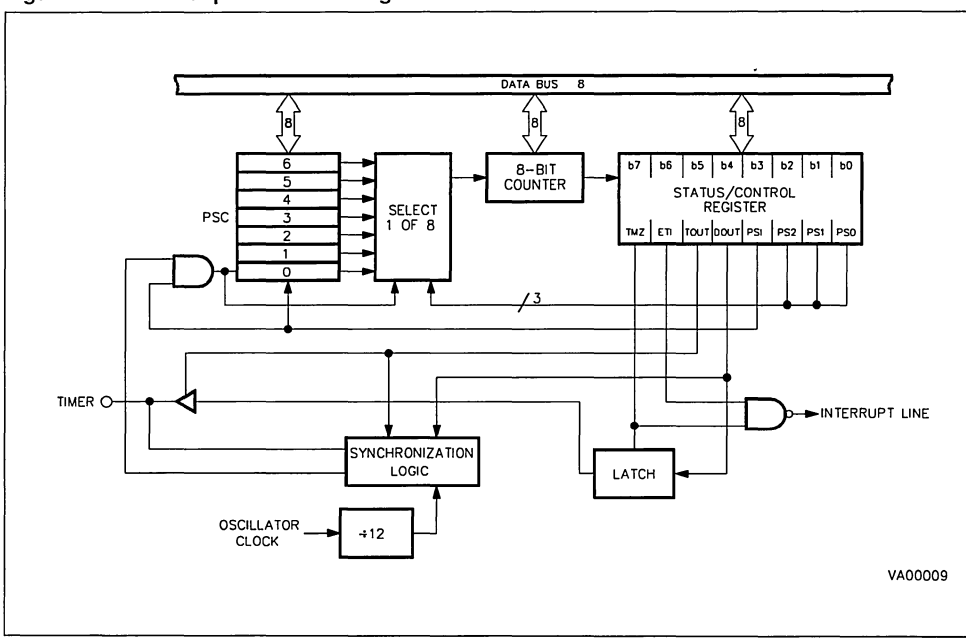
The ST639X devices offer two on-chip Timer peripherals consisting of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes. Figure 33 shows the timer block diagram. This timers do not have the external TIMER pin available for the user. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR that can be addressed in the data space as RAM location at the D3H (Timer 1) and DBH (Timer 2) addresses. The state of the 7-bit prescaler can be read in the PSC register at the D2H (Timer 1) and DAH (Timer 2) addresses. The control logic device can be managed thanks to the TSCR register D4H (Timer 1) and DCH (Timer 2) addresses as it is described in the following paragraphs.

The following description applies to both Timer 1 and Timer 2. The 8-bit counter is decrement by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (timer zero) bit in the TSCR is set to one. If the ETI (enable timer interrupt) bit in the TSCR is also set to one an interrupt request, associated to interrupt vector #3 (for Timer 1) and #1 for Timer 2, is generated. The interrupt of the timer can be used to exit the MCU from the WAIT mode.

The prescaler decrements on rising edge. The prescaler input can be the oscillator frequency divided by 12 or an external clock at TIMER pin (this is not available in ST639X).
Depending on the division factor programmed by PS2/PS1/PS0 (see table 9) bits in the TSCR, the clock input of the timer/counter register is multiplexed to different sources.
On division factor 1, the clock input of the prescaler is also that of timer/counter; on factor 2, bit 0 of prescaler register is connected to the clock input of TCR.

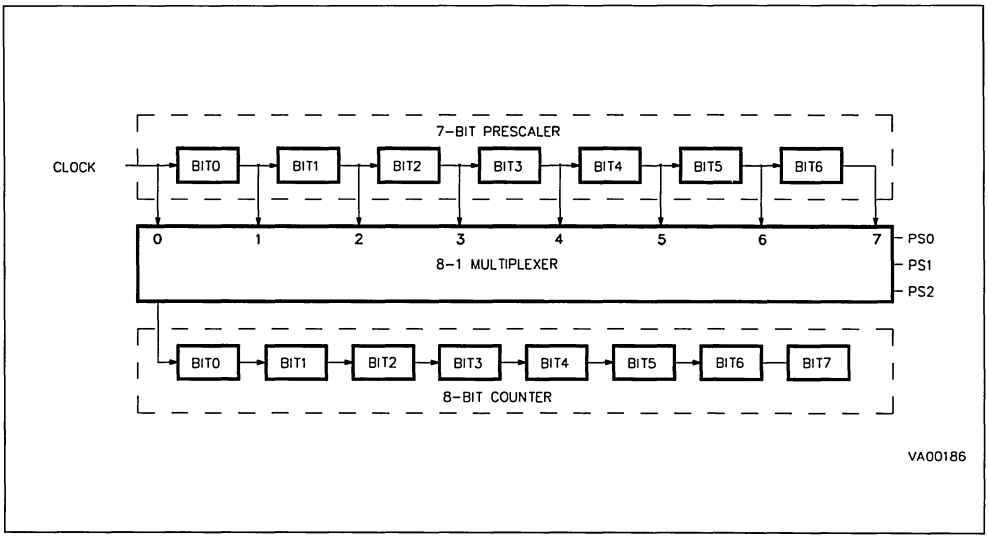
This bit changes its state with the half frequency of prescaler clock input. On factor 4, bit 1 of PSC is connected to clock input of TCR, and so on. On division factor 128, the MSB bit 6 of PSC is connected to clock input of TCR. The prescaler initialize bit (PSI) in the TSCR register must be set to one to allow the prescaler (and hence the counter) to start. If it is cleared to zero then all of the prescaler bits are set to one and the counter is inhibited from counting.

Figure 33. Timer Peripheral Block Diagram



TIMERS (Continued)

Figure 34. Timer Working Principle



The prescaler can be given any value between 0 and 7FH by writing to the related register address, if bit PSI in the TSCR register is set to one. The tap of the prescaler is selected using the PS2/PS1/PS0 bits in the control register. Figure 34 shows the timer working principle.

Timer Operating Modes

As on ST639X devices the external TIMER pin is not available the only allowed operating mode is the output mode that have to be selected by setting to 1 bit 4 and by clearing to 0 bit 5 in the TSCR1 register. This procedure will enable both Timer 1 and Timer 2. Any other combination written into these two bits will disable any Timer 1 and Timer 2 operation.

Output Mode (TSCR1 D4 = 1, TSCR1 D5 = 0). On this mode the timer prescaler is clocked by the prescaler clock input (OSC/12). The user can select the desired prescaler division ratio through the PS2/PS1/PS0 bits. When TCR count reaches 0, it sets the TMZ bit in the TSCR.

The TMZ bit can be tested under program control to perform a timer function whenever it goes high. Bit D4 and D5 on TSCR2 (Timer 2) register are not implemented.

Timer Interrupt

When the counter register decrements to zero and the software controlled ETI (enable timer interrupt) bit is set to one then an interrupt request associated to interrupt vector #3 (for Timer 1) and to interrupt vector #1 (for Timer 2) is generated. When the counter decrements to zero also the TMZ bit in the TSCR register is set to one.

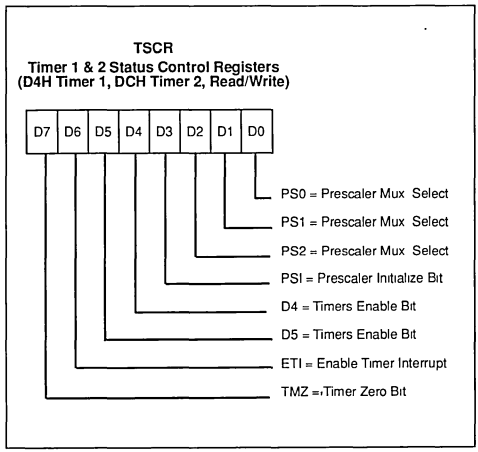
Notes :
TMZ is set when the counter reaches 00H ; however, it may be set by writing 00H in the TCR register or setting the bit 7 of the TSCR register. TMZ bit must be cleared by user software when servicing the timer interrupt to avoid undesired interrupts when leaving the interrupt service routine. After reset, the 8-bit counter register is loaded to FFH while the 7-bit prescaler is loaded to 7FH , and the TSCR register is cleared which means that timer is stopped (PSI=0) and timer interrupt disabled.

A write to the TCR register will predominate over the 8-bit counter decrement to 00H function, i.e. if a write and a TCR register decrement to 00H occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter reaches 00H again. The values of the TCR and the PSC registers can be read accurately at any time.

TIMERS (Continued)

Timer Registers

Figure 35. Timer Status Control Registers



TMZ. Low-to-high transition indicates that the timer count register has decrement to zero. This bit must be cleared by user software before to start with a new count.

ETI. This bit, when set, enables the timer interrupt (vector #3 for Timer 1, vector #1 for Timer 2) request. If ETI=0 the timer interrupt is disabled. If ETI= 1 and TMZ= 1 an interrupt request is generated.

D5. This is the timers enable bit D5. It must be cleared to 0 together with a set to 1 of bit D4 to enable both Timer 1 and Timer 2 functions. It is not implemented on TSCR2 register. Any other combination of TSCR1 D4 and D5 bits will disable any operation of both Timer 1 and Timer 2.

D4. This is the timers enable bit D4. It must be set to 1 together with a clear to 0 of bit D5 to enable both Timer 1 and Timer 2 functions. It is not implemented on TSCR2 register. Any other combination of TSCR1 D4 and D5 bits will disable any operation of both Timer 1 and Timer 2.

PSI. Used to initialize the prescaler and inhibit its counting while PSI = 0 the prescaler is set to 7FH and the counter is inhibited. When PSI = 1 the prescaler is enabled to count downwards. As long as PSI= 0 both counter and prescaler are not running.

PS2-PS0. These bits select the division ratio of the prescaler register. (see table 9)

The TSCR1 and TSCR2 registers are cleared on reset. The correct D4-D5 combination must be written in TSCR1 by user's software to enable the operation of Timer 1 and Timer 2.

Table 9. Prescaler Division Factors

PS2	PS1	PS0	Divided By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Figure 36. Timer Counter Registers

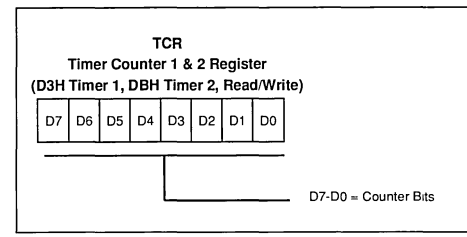
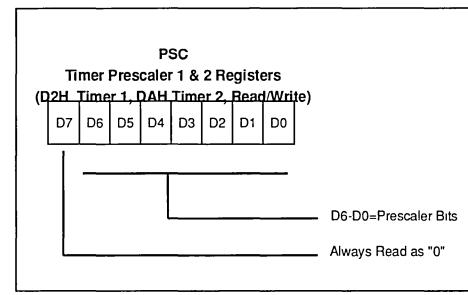


Figure 37. Prescaler Registers



HARDWARE ACTIVATED DIGITAL WATCHDOG FUNCTION

The hardware activated digital watchdog function consists of a down counter that is automatically initialized after reset so that this function does not need to be activated by the user program. As the watchdog function is always activated this down counter can't be used as a timer. The watchdog is using one data space register (HWDR location D8H). The watchdog register is set to FEH on reset and immediately starts to count down, requiring no software start. Similarly the hardware activated watchdog can not be stopped or delayed by software.

The watchdog time can be programmed using the 6 MSbits in the watchdog register, this gives the possibility to generate a reset in a time between 3072 to 196608 oscillator cycles in 64 possible steps. (With a clock frequency of 8MHz this means from 384µs to 24.576ms). The reset is prevented if the register is reloaded with the desired value before bits 2-7 decrement from all zeros to all ones.

The presence of the hardware watchdog deactivates the STOP instruction and a WAIT instruction is automatically executed instead of a STOP. Bit 1 of the watchdog register (set to one at reset) can be used to generate a software reset if cleared to zero). Figure 38 shows the watchdog block diagram while Figure 39 shows its working principle.

Figure 39. Hardware Activated Watchdog Working Principle

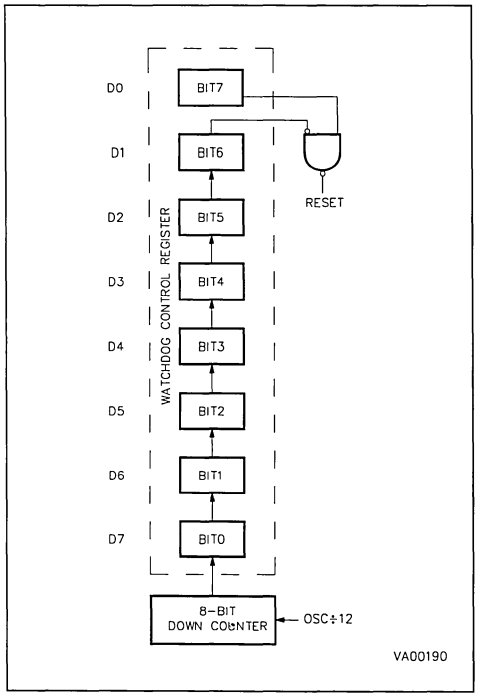
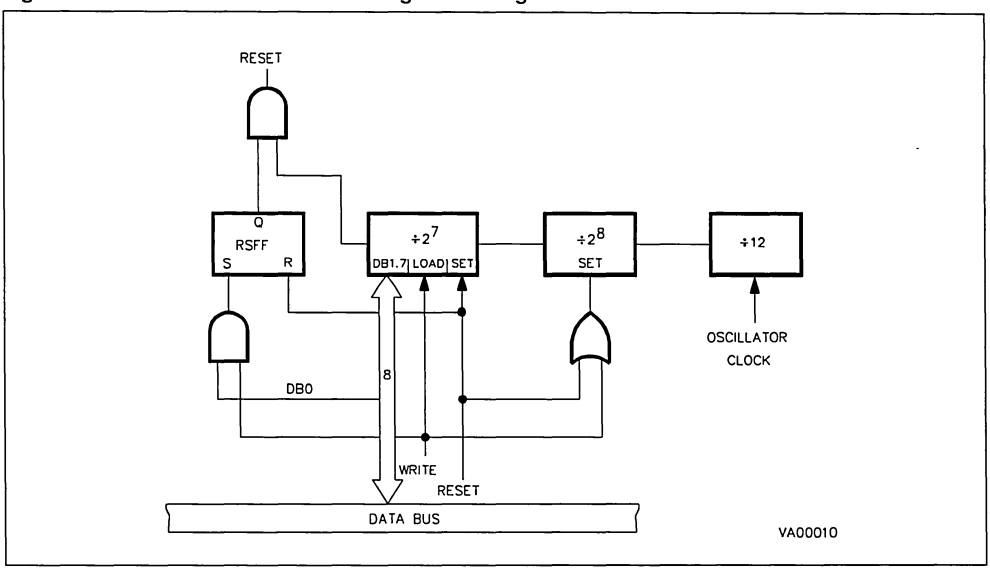
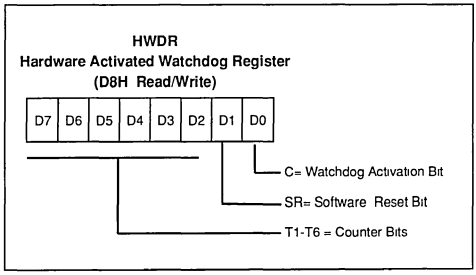


Figure 38. Hardware Activated Watchdog Block Diagram



HARDWARE ACTIVATED DIGITAL WATCHDOG FUNCTION (Continued)

Figure 40. Watchdog Register



T1-T6. These are the watchdog counter bits. It should be noted that D7 (T1) is the LSB of the counter and D2 (T6) is the MSB of the counter, these bits are in the opposite order to normal.

SR. This bit is set to one during the reset phase and will generate a software reset if cleared to zero.

C. This is the watchdog activation bit that is hardware set to one; the user can't change the value of this bit (the watchdog is always active).

The register reset value is FEH (Bit 1-7 set to one, Bit 0 cleared).

SERIAL PERIPHERAL INTERFACE

The ST639X Serial Peripheral Interface macrocell (SPI) has been designed to be cost effective and flexible in interfacing the various peripherals in TV applications.

It maintains the software flexibility but adds hardware configurations suitable to drive devices which require a fast exchange of data. The three pins dedicated for serial data transfer (single master only) can operate in the following ways:

- as standard I/O lines (software configuration)
- as S-BUS or as I^2CBUS (two pins)
- as standard (shift register) SPI

When using the hardware SPI, a fixed clock rate of 62.5kHz is provided. The ST6395 uses a fixed clock rate at 100KHz.

It has to be noted that the first bit that is output on the data line by the 8-bit shift register is the MSB.

SPI Data/Control Registers

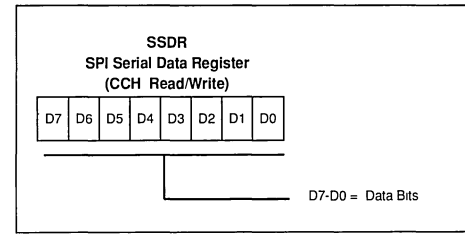
For I/O details on SCL (Serial Clock), SDA (Serial Data) and SEN (Serial Enable) please refer to I/O Ports description with reference to the following registers:

Port C data register, Address C2H (Read/Write).

- BIT D0 "SCL"
- BIT D1 "SDA"
- BIT D3 "SEN"

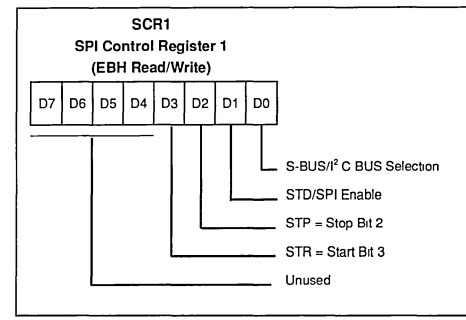
Port C data direction register, Address C6H (Read/Write).

Figure 41. SPI Serial Data Register



D7-D0. These are the SPI data bits. They can be neither read nor written when SPI is operating (BUSY bit set). They are undefined after reset.

Figure 42. SPI Control Register 1



D7-D4. These bits are not used.

STR. This is Start bit for I^2CBUS/S-BUS. This bit is meaningless when STD/SPI enable bit is cleared to zero. If this bit is set to one STD/SPI bit is also set to "1" and SPI Start generation, before beginning of transmission, is enabled. Set to zero after reset.

STP. This is Stop bit for I^2CBUS/S-BUS. This bit is meaningless when STD/SPI enable bit is cleared to zero. If this bit is set to one STD/SPI bit is also set to "1" and SPI Stop condition generation is enabled. STP bit must be reset when standard protocol is used (this is also the default reset conditions). Set to zero after reset.

STD, SPI Enable. This bit, in conjunction with S-BUS/I^2CBUS bit, allows the SPI disable and will select between I^2CBUS/S-BUS and Standard

SERIAL PERIPHERAL INTERFACE (Continued)

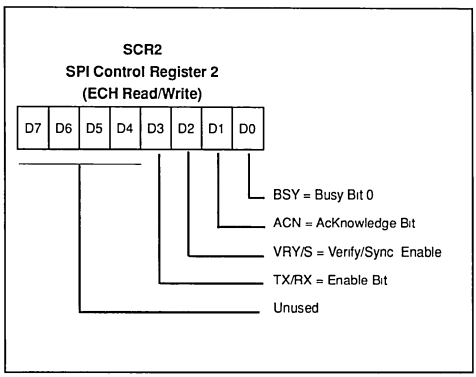
shift register protocols. If this bit is set to one, it selects both I²CBUS and S-BUS protocols; final selection between them is made by S-BUS/I²CBUS bit. If this bit is cleared to zero when S-BUS/I²CBUS is set to "1" the Standard shift register protocol is selected. If this bit is cleared to "0" when S-BUS/I²CBUS is cleared to 0 the SPI is disabled. Set to zero after reset.

S-BUS/I²CBUS Selection. This bit, in conjunction with STD/SPI bit, allows the SPI disable and will select between I²CBUS and S-BUS protocols. If this bit is cleared to "0" when STD bit is also "0", the SPI interface is disabled. If this bit is cleared to zero when STD bit is set to "1", the I²CBUS protocol will be selected. If this bit is set to one when STD bit is set to "1", the S-BUS protocol will be selected. Cleared to zero after reset.

Table 10. SPI Modes Selection

D0 S-BUS/I²CBUS	D1 STD/SPI	SPI Function
0	0	Disabled
1	0	STD Shift Register
0	1	I²CBUS
1	1	S-BUS

Figure 43. SPI Control Register 2



D7-D4. These bits are not used.

TX/RX. *Write Only.* When this bit is set, current byte operation is a transmission. When it is reset, current operation is a reception. Set to zero after reset.

VRY/S. *Read Only/Write Only.* This bit has two different functions in relation to read or write operation. *Reading Operation:* when STD and/or TRX bits are cleared to 0, this bit is meaningless. When bits STD and TX are set to 1, this bit is set each time BSY bit is set. This bit is reset during byte operation if real data on SDA line are different from the ones output from the shift register. Set to zero after reset. *Writing Operation* : it enables (if set to one) or disables (if cleared to zero) the interrupt coming from VSYNC pin. Undefined after reset. Refer to OSD description for additional information.

ACN. *Read Only.* If STD bit (D1 of SCR1 register) is cleared to zero this bit is meaningless. When STD is set to one, this bit is set to one if no Acknowledge has been received. In this case it is automatically reset when BSY is set again. Set to zero after reset.

BSY. *Read/Set Only.* This is the busy bit zero. When a one is loaded into this bit the SPI interface start the transmission of the data byte loaded into SSDR data register or receiving and building the receive data into the SSDR data register. This is done in accordance with protocol, direction and start/stop condition(s). This bit is automatically cleared at the end of the current byte operation. Cleared to zero after reset.

Note :
The SPI shift register is also the data transmission register and the data received register; this new feature is made possible by using the serial structure of the ST639X and thus reducing size and complexity.

During transmission or reception of data, all access to serial data register is therefore disabled. The reception or transmission of data is started by setting the BUSY bit to "1"; this will be automatically reset at the end of the operation. After reset, the busy bit is cleared to "0", and the hardware SPI disabled by clearing bit 0 and bit 1 of SPI control register 1 to "0". The outputs from the harware SPI are "ANDed" to the standard I/O software controlled outputs. If the hardware SPI is in operation then Port C ouputs related to the SPI should be set high or the pins should pin configured as inpus using the data direction register. When the SPI is configured as the S-BUS, the three pins PC0, PC1 and PC3 become the pins SCL, SDA and SEN respectively. When configured as the I²CBUS the pins PC0 and PC1 are configured as the pins SCL and SDA; PC3 is not driven and can be used as general purpose I/O pin. In the case of the STDSPI the pins PC0 and PC1 become the signals CLOCK and DATA, PC3 is not driven and can be used as general purpose I/O pin. The VERIFY bit is available when the SPI is configured as either S-BUS or I²CBUS. At the start of a byte transmission, the verify bit is set to one. If at any time during the transmission of the following eight bits, the data on the SDA line does not match the data forced by the SPI (while SCL is

SERIAL PERIPHERAL INTERFACE (Continued)

high), then the VERIFY bit is reset. The verify is available only during transmission for the S-BUS and I²CBUS; for other protocol it is not definfited. The SDA and SCL signal entering the SPI are buffered in order to remove any minor glitches. When STD bit is set to one (S-BUS or I²CBUS selected), and TRX bit is reset (receiving data), and STOP bit is set (last byte of current communication), the SPI interface does not generate the Acknowledge, according to S-BUS/I²CBUS specifications. PCO-SCL, PC1-SDA and PC3-SEN lines are standard drive I/O port pins with open-drain output configuration (maximum voltage that can be applied to these pins is V_{DD}+ 0.3V).

S-BUS/I²CBUS Protocol Information

The S-BUS is a three-wire bidirectional data-bus with functional features similar to the I²CBUS. In fact the S-BUS includes decoding of Start/Stop conditions and the arbitration procedure in case of multimaster system configuration (the ST639X SPI allows a single-master only operation). The SDA line, in the I²CBUS represents the AND combination of SDA and SEN lines in the S-BUS. If the SDA and the SEN lines are short-circuit connected, they appear as the SDA line of the I²CBUS. The Start/Stop conditions are detected (by the external peripherals suited to work with S-BUS/I²CBUS) in the following way:

- On S-BUS by a transition of the SEN line (1 to 0 Start, 0 to 1 Stop) while the SCL line is at high level.
- On I²CBUS by a transition of the SDA line (10 Start, 01Stop) while the SCL line is at high level.

Start and Stop condition are always generated by the master (ST639X SPI can only work as single master). The bus is busy after the start condition and can be considered again free only when a certain time delay is left after the stop condition. In the S-BUS configuration the SDA line is only allowed to change during the time SCL line is low. After the start information the SEN line returns to high level and remains unchanged for all the data transmission time. When the transmission is completed the SDA line is set to high level and, at the same time, the SEN line returns to the low level in order to supply the stop information with a low to high transition, while the SCL line is at high level. On the S-BUS, as on the I²CBUS, each eight bit information (byte) is followed by one acknowledged bit which is a high level put on the SDA line by the transmitter. A peripheral that acknowledges has to pull down the SDA line during the acknowledge clock pulse. An addressed receiver has to generate an acknowledge after the reception of each byte; otherwise the SDA line remains at the high level during the ninth clock pulse time. In this case the master transmitter can generate the Stop condition, via the SEN (or SDA in I²CBUS) line, in order to abort the transfer.

Start/Stop Acknowledge. The timing specs of the S-BUS protocol require that data on the SDA (only on this line for I²CBUS) and SEN lines be stable during the "high" time of SCL. Two exceptions to this rule are foreseen and they are used to signal the start and stop condition of data transfer.

- On S-BUS by a transition of the SEN line (10 Start, 01 Stop) while the SCL line is at high level.
- On I²CBUS by a transition of the SDA line (10 Start, 01 Stop) while the SCL line is at high level.

Data are transmitted in 8-bit groups; after each group, a ninth bit is interposed, with the purpose of acknowledging the transmitting sequence (the transmit device place a "1" on the bus, the acknowledging receiver a "0").

Interface Protocol. This paragraph deals with the description of data protocol structure. The interface protocol includes:

- A start condition
- A "slave chip address" byte, transmitted by the master, containing two different information:

a. the code identifying the device the master wants to address (this information is present in the first seven bits)

b. the direction of transmission on the bus (this information is given in the 8th bit of the byte); "0" means "Write", that is from the master to the slave, while "1" means "Read". The addressed slave must always acknowledge.

The sequence from, now on, is different according to the value of R/$\overline{W}$ bit.

1. R/$\overline{W}$ = "0" ($\overline{Write}$)

In all the following bytes the master acts as transmitter; the sequence follows with:

a. an optional data byte to address (if needed) the slave location to be written (it can be a word address in a memory or a register address, etc.).

b. a "data" byte which will be written at the address given in the previous byte.

c. further data bytes.

d. a STOP condition

A data transfer is always terminated by a stop condition generated from the master. The ST639X peripheral must finish with a stop condition before another start is given. Figure 44 shows an example of write operation.

2. R/$\overline{W}$ = "1" (Read)

In this case the slave acts as transmitter and, therefore, the transmission direction is changed. In read mode two different conditions can be considered:

SERIAL PERIPHERAL INTERFACE (Continued)

a. The master reads slave immediately after first byte. In this case after the slave address sent from the master with read condition enabled the master transmitter becomes master receiver and the slave receiver becomes slave transmitter.

b. The master reads a specified register or location of the slave. In this case the first sent byte will contain the slave address with write condition enabled, then the second byte will specify the address of the register to be read. At this moment a new start is given together with the slave address in read mode and the procedure will proceed as described in previous point "a".

Figure 44. Master Transmit to Slave Receiver (Write Mode)

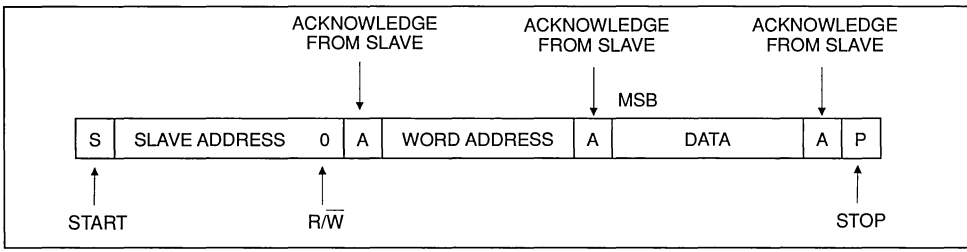


Figure 45. Master Reads Slave Immediately After First Byte (read Mode)

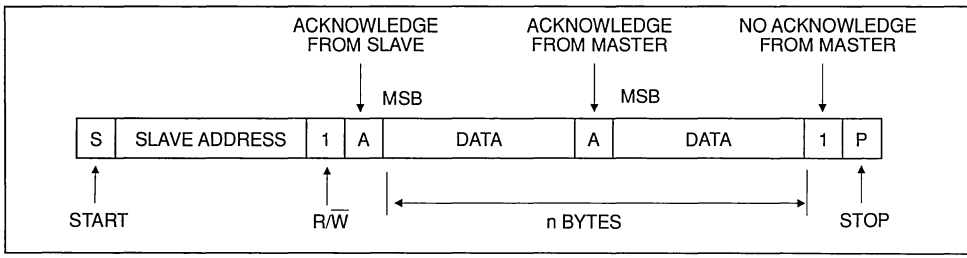
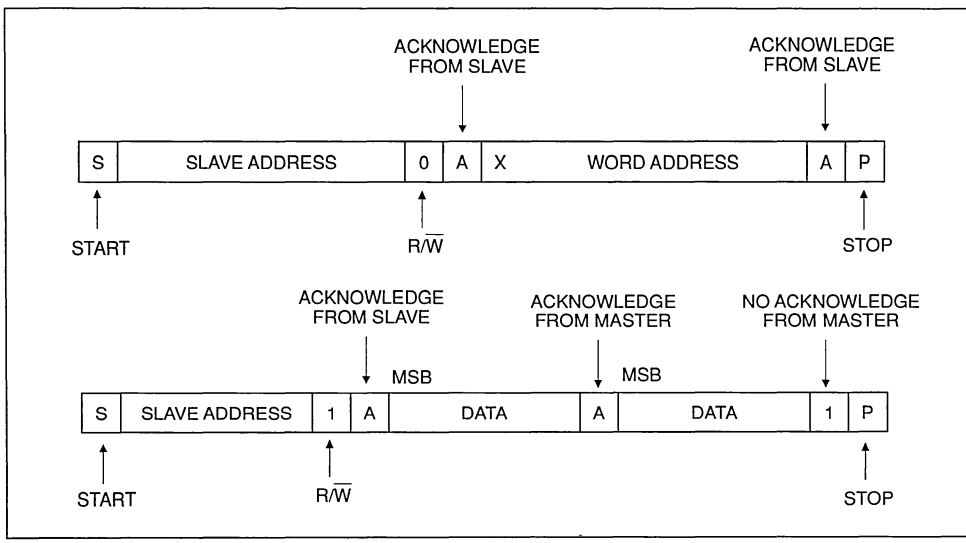


Figure 46. Master Reads After Setting Slave Register Address (Write Address, Read Data)

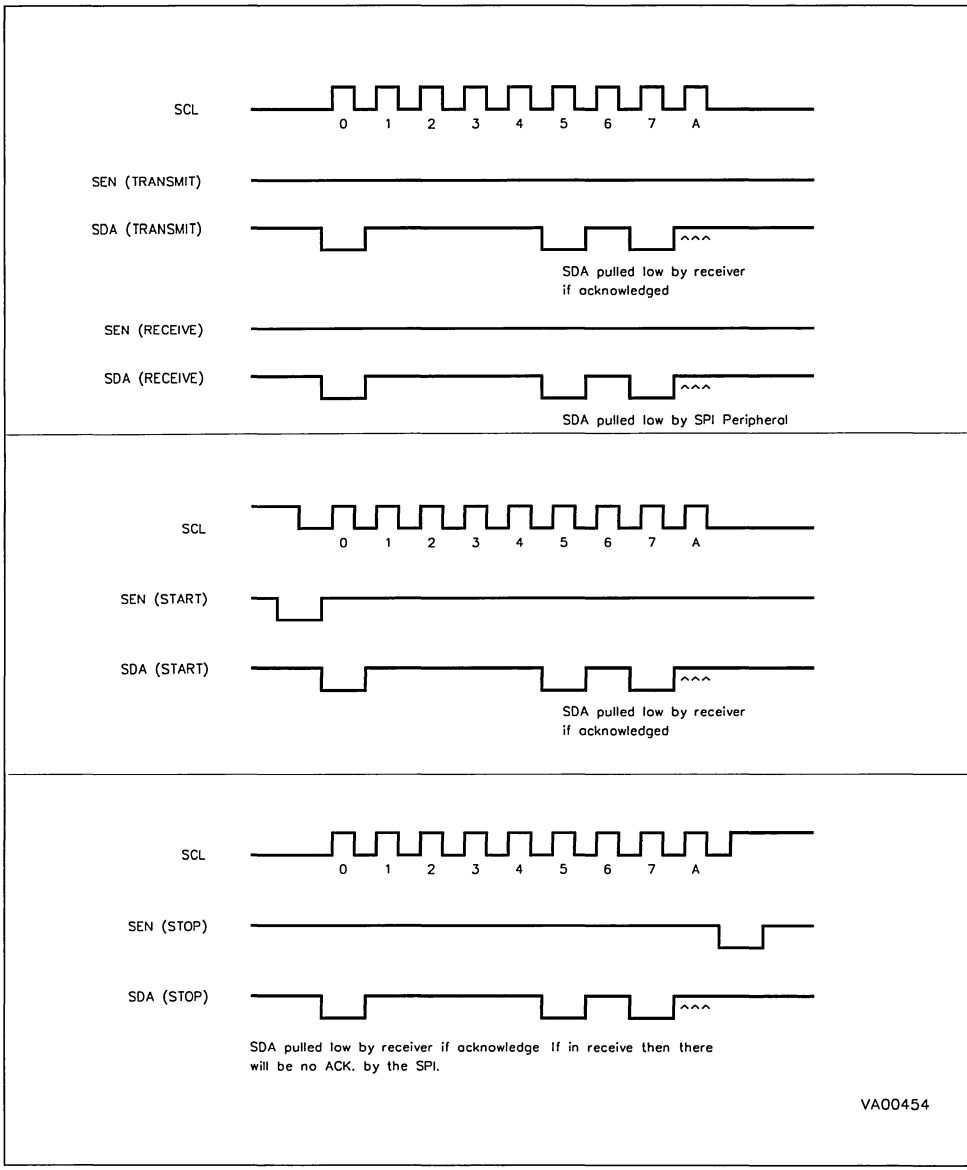


SERIAL PERIPHERAL INTERFACE (Continued)

S-BUS/I²CBUS Timing Diagrams

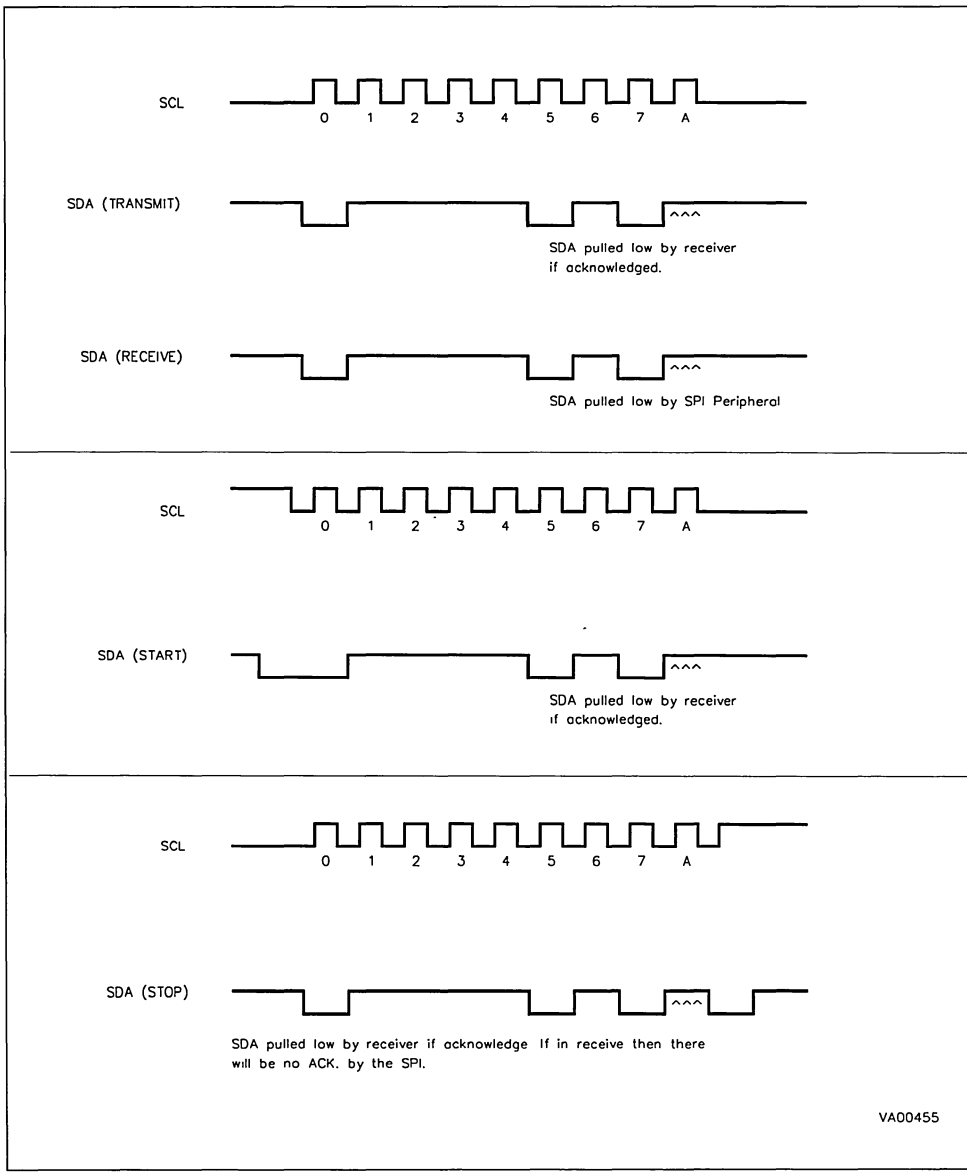
The clock of the S-BUS/I²CBUS of the ST639X SPI (single master only) has a fixed bus clock frequency of 62.5KHz (100KHz for ST6395). All the devices connected to the bus must be able to follow transfers with frequencies up to 62.5KHz (100KHz for ST6395), either by being able to transmit or receive at that speed or by applying the clock synchronization procedure which will force the master into a wait state and stretch low periods.

Figure 47. S-BUS Timing Diagrams



SERIAL PERIPHERAL INTERFACE (Continued)

Figure 48. I²C BUS Timing Diagrams



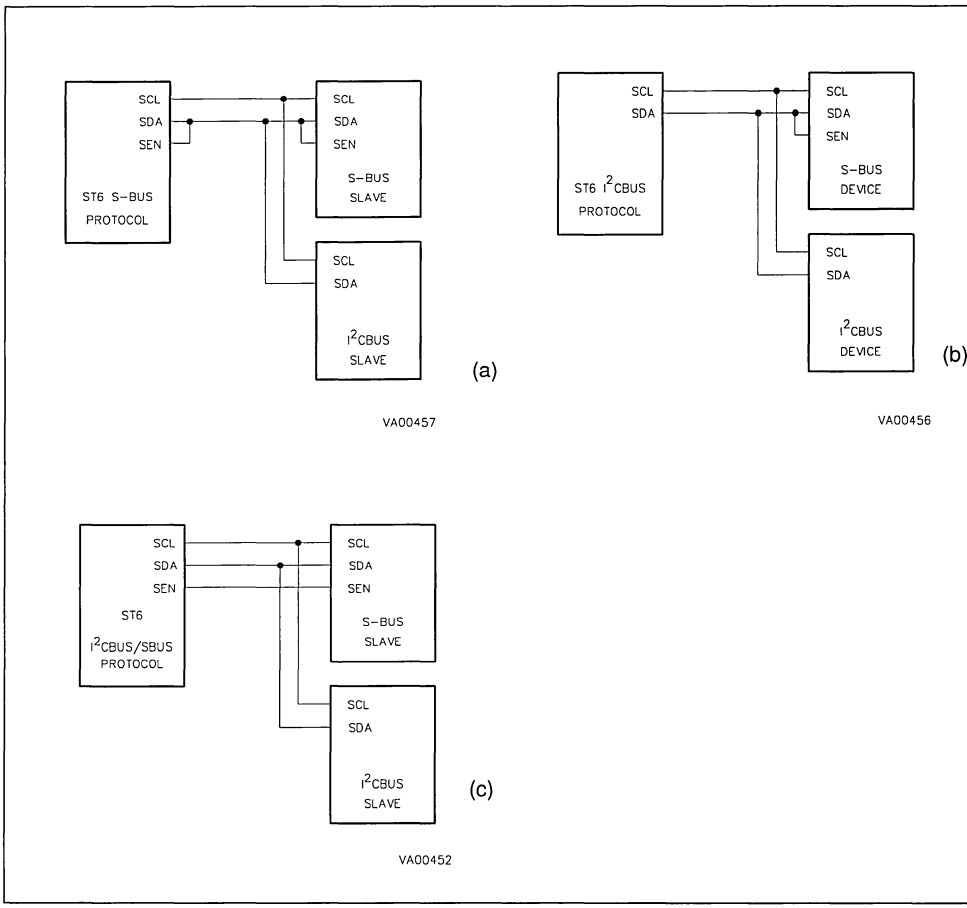
Note: The third pin, SEN, should be high; it's not used in the I²CBUS. Logically SDA is the AND of the S-BUS SDA and SEN.)

SERIAL PERIPHERAL INTERFACE (Continued)

Compatibility S-BUS/I²CBUS

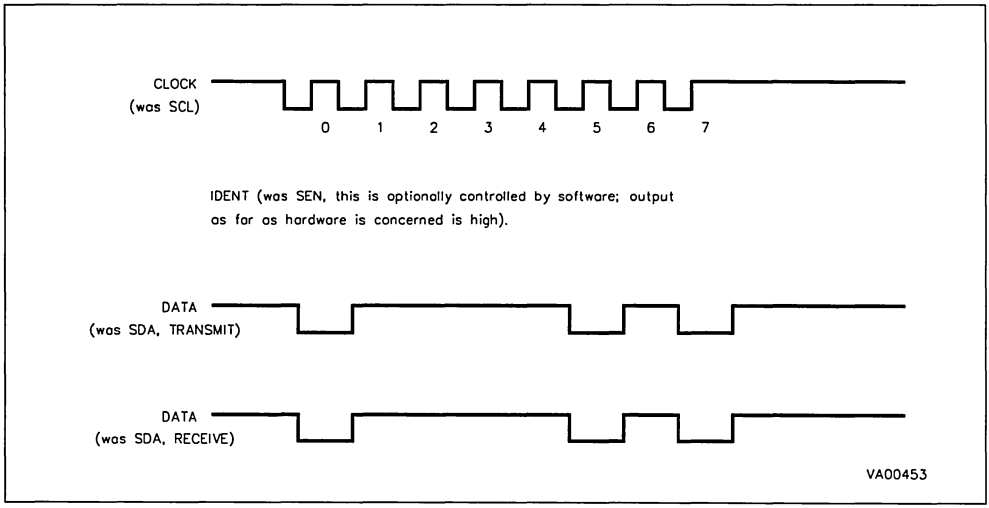
Using S-BUS protocol it is possible to implement mixed system including S-BUS/I²CBUS bus peripherals. In order to have the compatibility with the I²CBUS peripherals, the devices including the S-BUS interface must have their SDA and SEN pins connected together as shown in the following Figure 49 (a and b). It is also possible to use mixed S-BUS/I²CBUS protocols as showed in figure 49 (c). S-BUS peripherals will only react to S-BUS protocol signals, while I²CBUS peripherals will only react to I²CBUS signals. Multimaster configuration is not possible with ST63XX SPI (single master only).

Figure 49. S-BUS/I²C BUS Mixed Configurations



SERIAL PERIPHERAL INTERFACE (Continued)

Figure 50. Software Bus (hardware bus disabled) Timing Diagram



STD SPI Protocol (Shift Register)

This protocol is similar to the I²CBUS with the exception that there is no acknowledge pulse and there are no stop or start bits. The clock cannot be slowed down by the external peripherals.

In this case all three outputs should be high in order not to lock the software I/Os from functioning.

SPI APPLICATION NOTES

Stop Clock Slowdown: In the ST639X family of devices when operating in the I²C or SBUS modes, there is no internal clock slowdown for the final STOP clock. Slowdown means that if an external peripheral requires extra time it will hold the ST639X SCL clock low. To be fully I²C and SBUS compatible in this respect, the SW should check that the SCL line is indeed high before proceeding with the START of another I²C or SBUS transmission. In all other cases the SCL clock slowdown feature is operational.

SPI Standard Bus Protocol: The standard bus protocol is selected by loading the SPI Control Register 1 (SCR1 Add. EBH). Bit 0 named I²C must be set at one and bit 1 named STD must be reset. When the standard bus protocol is selected bit 2 of the SCR1 is meaningless.
This bit named STOP bit is used only in I²CBUS or SBUS. However take care that the *STOP BIT MUST BE RESET WHEN THE STANDARD PROTOCOL IS USED.* This bit is set to ZERO after RESET.

6-BIT PWM D/A CONVERTERS

The D/A macrocell contains up to six PWM D/A outputs (32Khz repetition, DA0-DA5) with six bit resolution .

Each D/A converter of ST639X is composed by the following main blocks:

- pre-divider
- 6-bit counter
- data latches and compare circuits

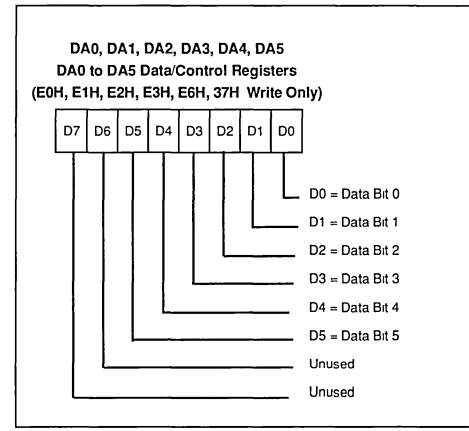
The pre-divider uses the clock input frequency (8MHz typical) and its output clocks the 6-bit free-running counter. The data latched in the six registers (E0H, E1H, E2H, E3H, E6H and E7H) control the six D/A outputs (DA0,1,2, 3, 4 and 5). When all zeros are loaded the relevant output is an high logic level; all 1's correspond to a pulse with a 1/64 duty cycle and almost 100% zero level.

The repetition frequency is 31.25KHz (except the ST6395 which is 25KHz) and is related to the 8MHz clock frequency. Use of a different oscillator frequency will result in wrong repetition frequency. All D/A outputs are open-drain with standard current drive capability and able to withstand up to 12V.

D/A Data/Control Registers

This paragraph deals with the description of D/A data/control registers.

Figure 52. DA0-DA5 Data Control Registers



D7, D6. These bits are not used.

DA0-DA5. These are the 6 bits of the PWM digital to analog converter . Undefined after reset.

AFC A/D INPUT, IR/PC6 RESULT, VSYNC RESULT, O0, O1 AND 62.5KHz OUTPUTS

The AFC macrocell contains an A/D comparator with five levels at intervals of 1V from 1V to 5V. The levels can all be lowered by 0.5V to effectively double the resolution. This A/D can be used to perform the AFC function. In addition this cell offers also a keyboard input register of three bits used to perform a keyboard scan and 4 open-drain outputs (able to withstand signals up to 12V) that can be used to perform band switch function. This pin is not available on ST6391 and ST6395

Figure 51. 6-BIT PWM D/A Output Configuration

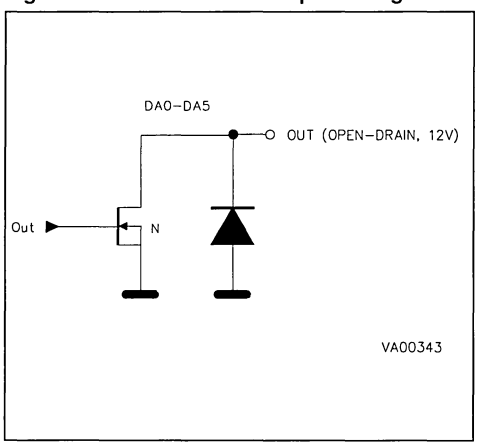
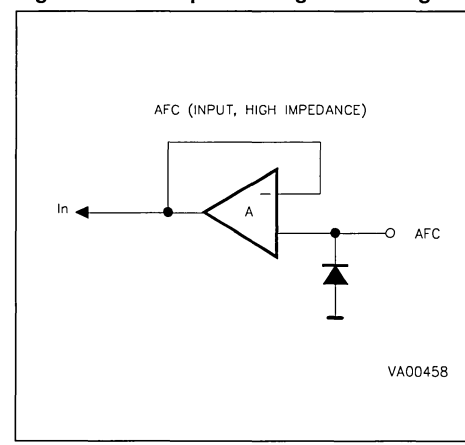


Figure 53. AFC Inputs Configuration Diagram



AFC A/D INPUT, IR/PC6 RESULT, VSYNC RESULT, O0, O1 AND 62.5KHz OUTPUT (Continued)

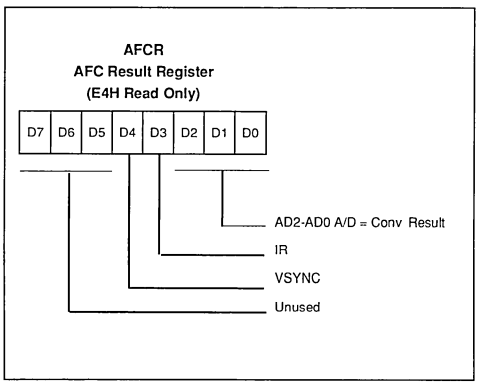
A/D Comparator

The A/D used to perform the AFC function (when high threshold is selected) has the following voltage levels: 1,2,3,4 and 5V. Bits 0-2 of AFC result register (E4H address) will provide the result in binary form (less than 1V is 000, greater than 5V is 101).

If the application requires a greater resolution, the sensitivity can be doubled by clearing to zero bit 2 of the OUTPUTS control register, address E5H. In this case all levels are shifted lower by 0.5V. If the two results are now added within a software routine then the A/D S-curve can be located within a resolution of 0.5V.

The A/D input has high impedance able to withstand up to 13V signals (input level tolerances ± 200mV absolute and ± 100mv relative to 5V).

Figure 54. AFC, IR and OSD Result Register



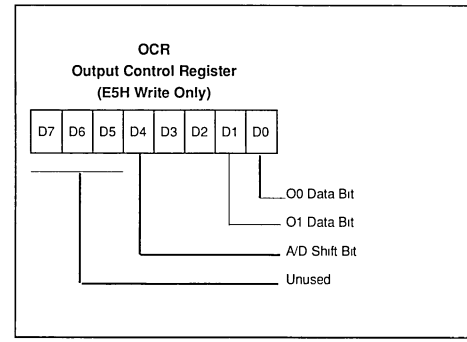
D7-D5. These bits are not used.

VSYNC. This bit reads the status of the VSYNC pin. It is inverted with respect to the pin. Refer to the OSD description for additional information.

IR. This bit reads the status of the IR latch. If a signal has been latched this bit will be high. Refer to the DEDICATED LATCHES description for additional information.

AD2-AD0. These bits store the real time conversion of the value present on the AFC input pin. No reset value.

Figure 55. Outputs Control Register



D7, D6, D5, D3, D2. These bits are not used.

A/D Shift. This bit determines the voltage range of the AFC input. Writing a zero will select the 0.5V to 4.5V range. Writing a one will select the 1.0V to 5.0V range. Undefined after reset.

O1, O0. These bit control the output pins O1, O0 (ST6394, ST6396 only). They are undefined after reset.

62.5 KHz Output

This bit is available only on ST6399. The pin is an open-drain (12V) output at a frequency of 62.5KHz (with an 8MHz clock). The pin can used to drive the SGS-THOMSON TEA5640 chroma processor. Refer to the TEA5640 data sheet for more information. Care must be taken to respect the frequency tolerances required by the TEA5640 by chosing a quartz with PPM variations within the limits required by the chroma processor.

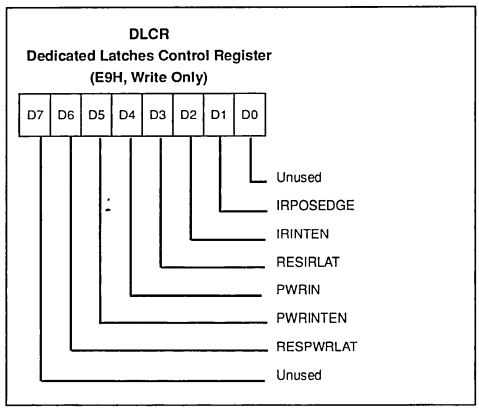
DEDICATED LATCHES

Two latches are available which may generate interrupts to the ST639X core. The IR latch is set either by the falling or rising edge of the signal on pin PC6(IRIN). If bit 1 (IRPOSEDGE) of the latches register (E9H) is high, then the latch will be triggered on the rising edge of the signal at PC6(IRIN). If bit 1 (IRPOSEDGE) is low, then the latch will be triggered on the rising edge of the signal at PC6(IRIN). The IR latch can be reset by setting bit 3 (RESIRLAT) of the latches register; the bit is set only and a high should be written every time the IR latch needs to be reset. If bit 2 (IRINTEN) of the latches register (E9H) is high, then the output of the IR latch, IRINTN, may generate an interrupt (#0). IRINTN is inverted with respect to the state of the

DEDICATED LATCHES(Continued)

IR latch. If bit 2 (IRINTEN) is low, then the output of the IR latch, IRINTN, is forced high. For more information see the interrupts section. The state of the IR latch may be read from bit 3 (IRLATCH) of register E4H; if the IR latch is set, then bit 3 will be high. The PWR latch is set either by the falling or rising edge of the signal on pin PC4(PWRIN). If bit 4 (PWREDGE) of the latches register (E9H) is high, then the latch will be triggered on the rising edge of the signal at PC4(PWRIN). If bit 4 (PWREDGE) is low, then the latch will be triggered on the falling edge of the signal at PC4(PWRIN). The PWR latch can be reset by setting bit 6 (RESPWRLAT) of the latches register; the bit is set only and a high should be written every time the PWR latch needs to be reset. If bit 5 (PWRINTEN) of the latches register (E9H) is high, then the output of the PWR latch, PWRINTN, may generate an interrupt (#4). PWRINTN is inverted with respect to the state of the PWR latch. If bit 5 (PWRINTEN) is low, then the output of the PWR latch, PWRINTN, is forced high. For more information see the interrupts section. The PWR latch is not available on the ST6391 and the ST6393.

Figure 56. Dedicated Latched Control Register



D7. This bit is not used

RESPWRLAT. Resets the PWR latch; this bit is set only.

PWRINTEN. This bit enables the PWRINTN signal (#4) from the latch to the ST639X core. Undefined after reset.

PWRIN. The bit determines the edge which will cause the PWRIN latch to be set. If this bit is high, than the PWRIN latch will be set on the rising edge of the PWRIN signal. Undefined after reset.

RESIRLAT. Resets the IR latch; this bit is set only.

IRINTEN. This bit enables the IRINTN signal (#0) from the latch to the ST639X core. Undefined after reset.

IRPOSEDGE. The bit determines the edge which will cause the IR latch to be set. If this bit is high, than the IR latch will be set on the rising edge of the IR signal. Undefined after reset.

D0. This bit is not used

ON-SCREEN DISPLAY (OSD)

The ST639X OSD macrocell is a CMOS LSI character generator which enable display of characters and symbols on the TV screen. The character rounding function enhances the readability of the characters. The ST639X OSD receives horizontal and vertical synchronization signal and outputs screen information via R, G, B and blanking pins. The main characteristics of the macrocell are listed below:

- Number of display characters: 5 lines by 15 columns.
- Number of character types: 128 characters in two banks of 64 characters. Only one bank per screen can be used.
- Character size: Four character heights (18H, 36H 54H, 72H), two available per screen programmable by line.
- Character format: 6x9 dots with character rounding function.
- Character color: Eight colors available programmable by word. The ST6394 and ST6396 have only one color available
- Display position: 64 horizontal positions by 2/fos and 63 vertical positions by 4 H
- Word spacing: 64 positions programmable from 2/fosc to 128/fosc.
- Line spacing: 63 positions programmable from 4 to 252 H.
- Background: No background, square background or fringe background programmable by word.
- Background color: Two of eight colors available programmable by word.
- Display output: Three character data output terminals (R,G,B) and a blank output terminal. The ST6394 and ST6396 have only the B and Blank output terminals.
- Display on/off: Display data may be programmed on or off by word or entire screen. Entire screen may be blanked.

Format Specification

The entire display can be turned on or off thru the use of global enable bit or the display may be

ON-SCREEN DISPLAY (Continued)

selectively turned on or off by word. To turn off the entire display, the global enable bit (GE) should be zero. If the global enable is one, the display is controlled by the word enable bits (WE). The global enable bit is located in the global enable register and the word enable bit is located in the space character preceding the word.

Each line must begin with a format character which describes the format of that line and of the first word. This character is not displayed.

A space character defines the format of subsequent words. A space character is denoted by a one in bit 6 in the display RAM. If bit 6 of the display RAM is a zero, the other six bits define one of the 64 display characters.

The color, background and enable can be programmed by word. This information is encoded in the space character between words or in the format character at the beginning of each line. Five bits define the color and background of the following word, and determine whether it will be displayed or not.

Characters are stored in a 6 x 9 dot format. One dot is defined vertically as 2H (horizontal lines) and horizontally as 2/fosc if the smallest character size is enabled. There is no space between characters or lines if the vertical space enable (VSE) and horizontal space enable (HSE) bits are both zero. This allows the use of special graphics characters.

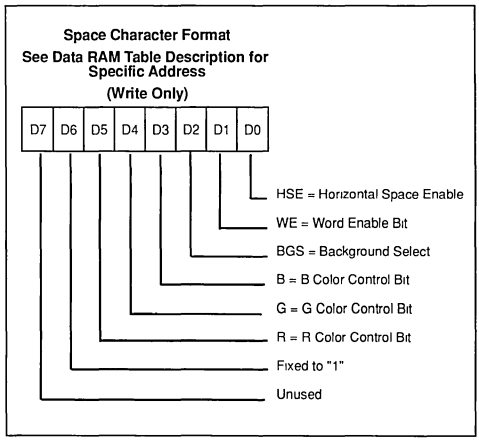
The normal alphanumeric character set is formatted to be 5 x 7 with on empty row at the top and one at the bottom and one empty column at the right. If VSE and HSE are both zero, then the spacing between alphanumeric characters is 1 dot and the spacing between lines of alphanumeric characters is 2H.

The character size is programmed by line thru the use of the size bit (S) in the format character and the global size bits (GS1 and GS2). The vertical spacing enable bit (VSE) located in the format character controls the spacing between lines. If this bit is set to one, the spacing between lines is defined by the vertical spacing register, otherwise the spacing between lines is 0.

The spacing between words is controlled by the horizontal space enable bit (HSE) located in the space character. If this bit is set to one, the spacing between words is defined by the horizontal spacing register, otherwise the space character width of 6 dots is the spacing between words.

The formats for the display character, space character and format character are described hereafter.

Figure 57. Space Character Register Explanation



D7. Not used.

D6. This pin is fixed to "1".

R, G, B. *Color.* The 3 color control bits define the color of the following word as shown in table 11.

Table 11. Space Character Register Colour Setting.

R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

BGS. *Background Select.* The background select bit selects the desired background for the following word. There are two possible backgrounds defined by the bits in the Background Control Register.

"0" - The background on the following word is enabled by BG0 and the color is set by R0, G0, and B0.

"1" - The background on the following word is enabled by BG1 and the color is set by R1, G1, and B1.

WE. *Word Enable.* The word enable bit defines whether or not the following word is displayed.

"0" - The word is not displayed.

ON-SCREEN DISPLAY (Continued)

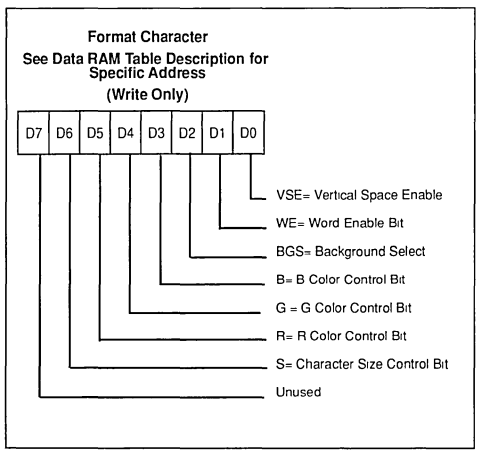
"1" - If the global enable bit is one, then the word is displayed.

HSE. *Horizontal Space Enable.* The horizontal space enable bit determines the spacing between words. The space between characters is always 0. The alphanumeric character set is implemented in a 5 x 7 format with one empty column to the right and one empty row above and below so that the space between alphanumeric characters will be one dot.

"0" - The space between words is equal to the width of the space character, which is 6 dots.

"1" - The space between words is defined by the value in the horizontal space register plus the width of the space character.

Figure 58. Format Character Register Explanation



D7. This bit is not used

S. *Character Size.* The character size bit, along with the global size bits (GS2 and GS1) located in the horizontal space register, specify the character size for each line as defined in Table 13.

R, G, B. *Color.* The 3 color control bits define the color of the following word as shown in Table 12.

BGS. *Background Select.* The background select bit selects the desired background for the following word. There are two possible backgrounds defined by the bits in the Background Control Register.

"0" - The background on the following word is enabled by BG0 and the color is set by R0, G0, and B0.

"1" - The background on the following word is enabled by BG1 and the color is set by R1, G1, and B1.

WE. *Word Enable.* The word enable bit defines whether or not the following word is displayed.

"0" - The word is not displayed.

"1" - If the global enable bit is one, then the word is displayed.

VSE. *Vertical Space Enable.* The vertical space enable bit determines the spacing between lines.

"0" - The space between lines is equal to 0H. The alphanumeric character set is implemented in a 5 x 7 format with one empty column to the right and one empty row above and one below and stored in a 6 x 9 format.

"1" - The space between lines is defined by the value in the vertical space register.

Table 12. Format Character Register Colour Setting.

R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

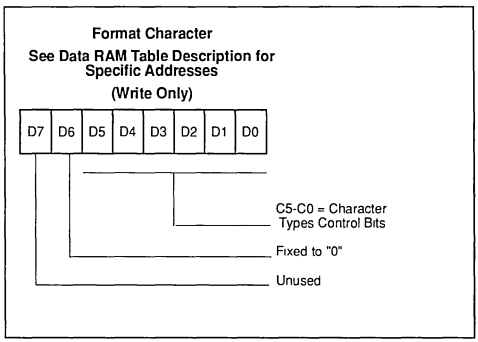
Table 13. Format Character Register Size Setting

GS2	GS1	S	Vertical Height	Horizontal lenght
0	0	0	18H	6 TDOT
0	0	1	36H	12 TDOT
0	1	0	18H	6 TDOT
0	1	1	54H	18 TDOT
1	0	0	36H	12 TDOT
1	0	1	54H	18 TDOT
1	1	0	36H	12 TDOT
1	1	1	72H	24 TDOT

TDOT= 2/fosc

ON-SCREEN DISPLAY (Continued)

Figure 59. Display Character Register Explanation



D7. This bit is not used.

D6. This bit is fixed to "0".

C5-C0. *Character type.* The 6 character type bits define one of the 64 available character types. These character types are shown on the following pages.

Character Types

The character set is user defined as ROM mask option.

Register and RAM Addressing

The OSD contains seven registers and 80 RAM locations. The seven registers are the Vertical Start Address register, Horizontal Start Address register, Vertical Space register, Horizontal Space register, Background Control register, Global Enable register and Character Bank Select register. The Global Enable register can be written at any time by the ST639X Core. The other six registers and the RAM can only be read or written to if the global enable is zero.

The six registers and the RAM are located on two pages of the paged memory of the ST639X MCUs; the Character Bank Select register is located outside the paged memory at address EDH. Each page contains 64 memory locations. This paged memory is at memory locations 00H to 3FH in the ST639X memory map. A page of memory is enabled by setting the desired page bit, located in the data RAM bank switching register, to a one. The page register is location E8H. A one in bit five selects page 5, located on the OSD and a one in bit 6 selects page 6 on the OSD. Table 14 shows the addresses of the OSD registers and RAM.

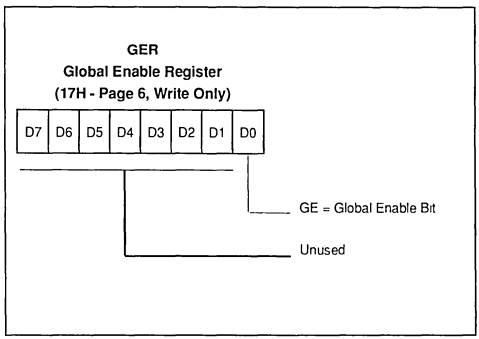
Table 14. OSD Control Registers and Data RAM Addressing

Page	Address	Register or RAM
5	00H - 3FH	RAM Locations 00H - 3FH
6	00H - 0FH	RAM Locations 00H - 0FH
6	10H	Vertical Start Register
6	11H	Horizontal Start Register
6	12H	Vertical Space Register
6	13H	Horizontal Space Register
6	14H	Background Control Register
6	17H	Global Enable Register
No Page	EDH	Character Bank Select Register

OSD Global Enable Register

This register contains the global enable bit (GE). It is the only register that can be written at any time regardless of the state of the GE bit. It is a write only register.

Figure 60. Global Enable register



D7-D1. These bits are not used

GE. *Global Enable.* This bit allows the entire display to be turned off.

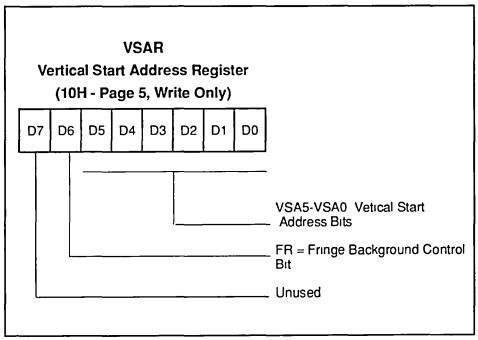
"0" - The entire display is disabled. The RAM and other registers of the OSD can be accessed by the Core.

"1" - Display of words is controlled by the word enable bits (WE) located in the format or space character.

The other registers and RAM cannot be accessed by the Core.

ON-SCREEN DISPLAY (Continued)

Figure 61. Vertical Start Address Register



D7. This bit is not used

FR. *Fringe Background.* This bit changes the background from a box background to a fringe background. The background is enabled by word as defined by either BK0 or BK1.

"0" - The background is defined to be a box which is 7 x 9 dots.

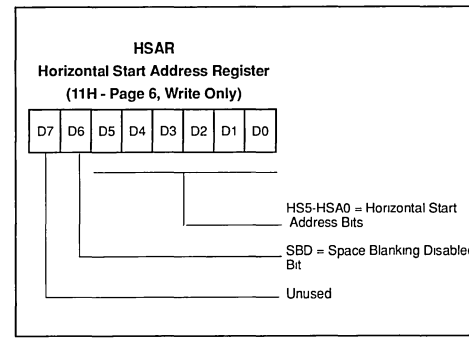
"1" - The background is defined to be a fringe.

VSA5-VSA0. *Vertical Start Address.* These bits determine the start position of the first line in the vertical direction. The 6 bits can specify 63 display start positions of interval 4H. The first start position will be the fourth line of the display. The vertical start address is defined VSA0 by the following formula.

Vertical Start Address = $4H(2^5(VSA5) + 2^4(VSA4) + 2^3(VSA3) + 2^2(VSA2) + 2^1(VSA1) + 2^0(VSA0))$

The case of all Vertical Start Address bits being zero is 111.

Figure 62. Horizontal Start Address Register



D7. This bit is not used.

SBD. *Space Blanking Disable.* This bit controls whether or not the background is displayed when outputting spaces. If two background colors are used on adjacent words, then the background should not be displayed on spaces in order to make a nice break between colors. If an even background around an area of text is desired, as in a menu, then the background should be displayed when outputting spaces.

"0" - The background during spaces is controlled by the background enable bits (BK0 and BK1) located in the Background Control register.

"1" - The background is not displayed when outputting spaces.

HSA5, HSA0 - *Horizontal Start Address bits.* These bits determine the start position of the first character in the horizontal direction. The 6 bits can specify 64 display start positions of interval 2/fosc or 400ns. The first start position will be at 4.0µs because of the time needed to access RAM and ROM before the first character can be displayed. The horizontal start address is defined by the following formula.

Horizontal Start Address = $2/fosc(10.0 + 2^5(HSA5) + 2^4(HSA4) + 2^3(HSA3) + 2^2(HSA2) + 2^1(HSA1) + 2^0(HSA0))$

ON-SCREEN DISPLAY (Continued)

Figure 63. Vertical Space Register

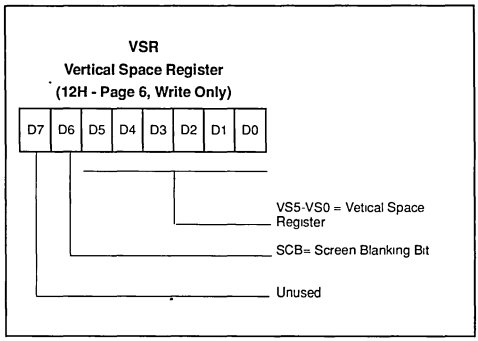
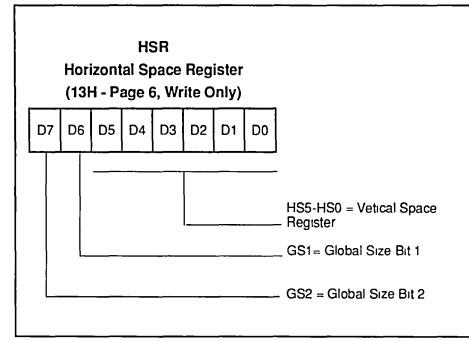


Figure 64. Horizontal Space Register



D7. This bit is not used

SCB. *Screen Blanking.* This bit allows the entire screen to be blanked.

"0" - The blanking output signal (VBLK) is active only when displaying characters.

"1" - The blanking output signal (VBLK) is always active. Characters in the display RAM are still displayed.

When this bit is set to one, the screen is blanked also without setting the Global Enable bit to one (OSD disabled).

VS5 , VS0. *Vertical Space.* These bits determine the spacing between lines if the Vertical Space Enable bit (VSE) in the format character is one. If VSE is zero there will be no spaces between lines. The Vertical Space bits can specify one of 63 spacing values from 4H to 252H. The space between lines is defined by the following formula.

Space between lines = $4H(2^5(VS5) + 2^4(VS4) + 2^3(VS3) + 2^2(VS2) + 2^1(VS1) + 2^0(VS0))$

The case of all Vertical Start Address bits being zero is ill.

GS2,GS1. *Global Size.* These bits along with the size bit (S) located in the Character format word specify the character size for each line as defined in table 15.

Table 15. Horizontal Space Register Size Setting.

GS2	GS1	S	Vertical Height	Horizontal Lenght
0	0	0	18H	6 TDOT
0	0	1	36H	12 TDOT
0	1	0	18H	6 TDOT
0	1	1	54H	18 TDOT
1	0	0	36H	12 TDOT
1	0	1	54H	18 TDOT
1	1	0	36H	12 TDOT
1	1	1	72H	24 TDOT

Note: TDOT= $2/f_{OSC}$

HS5, HS0 . *Horizontal Space* . These bits determine the spacing between words if the Horizontal Space Enable bit (HSE) located in the space character is a one. The space between words is then equal to the width of the space character plus the number of tdots specified by the Horizontal Space bits. The 6 bits can specify one of 64 spacing values ranging from 2/fosc to 128/fosc. The formula is shown below for the smallest size character(18H). If larger size characters are being displayed the spacing between words will increase proportionately. Multiply the value below by 2, 3 or 4 for character sizes of 36H, 54H and 72H respectively.

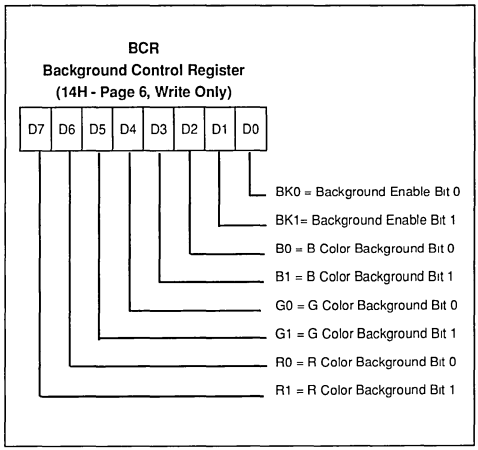
Space between words (not including the space character)=$2/fosc((1+2^5(HS5)+2^4(HS4)+2^3(HS3)+2^2(HS2)+ 2^1(HS1)+2^0(HS0))$

ON-SCREEN DISPLAY (Continued)

Background Control Register

This register sets up two possible backgrounds. The background select bit (BGS) in the format or space character will determine which background is selected for the current word.

Figure 65. Background Control Registers



R1,R0,G1,G0,B1,B0. Background Color. These bits define the color of the specified background, either background 1 or background 0 as defined in Table 16.

Table 16. Background Register Colour Setting.

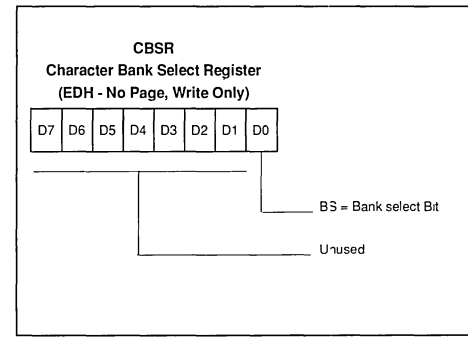
RX	GX	BX	Color
0	ó	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

BK1,BK0. *Background Enable.*These bits determine if the specified background is enabled or not.

"0" - The following word does not have a background.

"1" - There is a background around the following word.

Figure 66. Character Bank Select Register



D7-D1. These bits are not used

BS. *Bank Select.* This bit select the character bank to be used. The lower bank is selected with 0. The value can be modified only when the OSD is OFF (GE=0). No reset value.

OSD Data RAM

The contents of the data RAM can be accessed by the ST639X MCUs only when the global enable bit (GE) in the Global Enable register is a zero.

The first character in every line is the format character. This character is not displayed. It defines the size of the characters in the line and contains the vertical space enable bit. This character also defines the color, background and display enable for the first word in the line. Subsequent characters are either spaces or one of the 64 available character types.

The space character defines the color, background, display enable and horizontal space enable for the following word. Since there are 5 display lines of 15 characters each, the display RAM must contain 5 lines x (15 characters + 1 format character) or 80 locations. The RAM size is 80 locations x 7 bits. The data RAM map is shown inTable 17.

ON-SCREEN DISPLAY (Continued)

Table 17. OSD RAM Map

Column				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A0				0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A3				0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A2				0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A1				0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A6	A5	A4	LINE																
0	0	0	1	FT															
0	0	1	2	FT															
0	1	0	3	FT															
0	1	1	4	FT															
1	0	0	5	FT															
					AVAILABLE SCREEN SPACE														

Notes: FT. The format character required for each line. Characters in columns 1 thru 15 are displayed.

Emulator Remarks

There are a few differences between emulator and silicon. For noise reasons, the OSD oscillator pins are not available: the internal oscillator cannot be disabled and replaced by an external coil. In the emulator, the Character Bank Select register can be written also with Global Enable bit set, while this is not allowed in the device.

Application Notes

1 - The OSD character generator is composed of a dual port video ram and some circuitry. It needs two input signals VSYNC and HSYNC to syncronize its dedicated oscillator to the TV picture. It generates 4 output signals, that can be used from the TV set to generate the characters on the screen. For istance, they can be used to feed the SCART plug, providing an adequate buffer to drive the low impedance (75 Ω) of the SCART inputs.

2 - The Core sees the OSD as a number of RAM locations (80) plus a certain number of control registers (6). These 86 locations are mapped in two pages of the dynamic data ram address range (0H..3FH).
In page 5 (load 20H in the register 0E8H), there are 64 bytes of RAM, the ones of the first 4 rows (16 bytes each row, 15 characters per row maximum, plus an hidden leading format character). In page 6 (load 40H in register 0E8H), the 16 bytes of the fith row (0..0FH), and the 6 control registers (10H..14H,17H).

3 - The video RAM is a dual port ram. That means that it can be addressed either from the Core or from the OSD circuitry itself. To reduce the complexity of the circuitry, and thus its cost, some restrictions have been introduced in the use of the OSD.

a. The Core can Only write to any of the 86 locations (either video RAM or control registers).

b. The Core can Only write to any of the leading 85 locations when the OSD oscillator is OFF. Only the last location (control register 17H in page 6) can be addressed at any time. This is the Global Enable Register, which contains only the GE bit. If it is set, the OSD is on, if it is reset the OSD is off.

4 - The timing of the on/off switching of the OSD oscillator is the following:

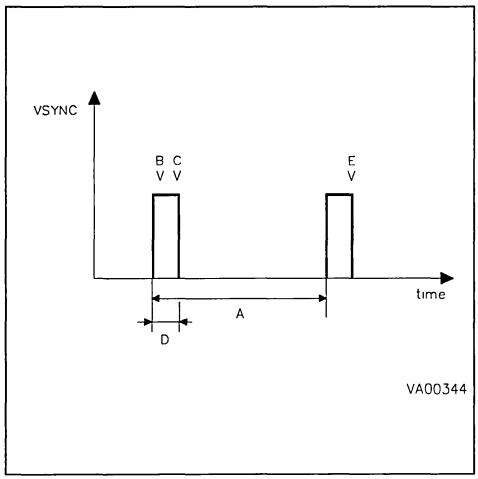
a. GE bit is set. The OSD oscillator will start on the next VSYNC signal.

b. GE bit is reset. The OSD oscillator will be immediately switched off.

ON-SCREEN DISPLAY (Continued)

To avoid a bad visual impression, it is important that the GE bit is set before the end of the flyback time when charging character. This can be done inside the VSYNC interrupt routine. The following diagram can explain better:

Figure 67. OSD Oscillator ON/OFF Timing



Notes: A - Picture time. 20 mS in PAL/SECAM.
B - VSYNC interrupt, if enabled.
C - Starting of OSD oscillator, if GE = 1
D - Flyback time.

When modifying the picture display (i.e.: a bar graph for an analog control), it is important that the switching on of the GE bit is done before the the end of the flyback time (D in Figure 67). If the GE bit is set after the end of the flyback time then the OSD will not start until the begining of the next frame. This results in one frame being lost and will result in a Flicker on the screen. One method to be sure to avoid the flicker is to wait for the VSYNC interrupt at the start of the flyback; once the VSYNC interrupt is detected, then the GE bit can be set to zero, the characters changed, and the GE set to one. All this should occur before the end of the flyback time in order not to loose a frame. The correct edge of the interrupt must be chosen. The VSYNC pin may alternatively be sampled by software in order to know the status; this can be done by reading bit 4 of register E4H; this bit is inverted with respect to the VSYNC pin.

6 - An OSD end of line Bar is present in the ST63P9X piggyback and ST639X ROM devices when using the background mode. If this bar is present with software running in the piggybacks then it is also present on the ROM mask version. If the end of line bar is seen to be eliminated by software in the piggyback, then it is also be eliminated in the ROM mask version.

The bar appears at the end of the line in the background mode when the last character is a space character and the first format character is defined with S=0 (size 0). The bar is the color of the background defined by the space character. To eliminate bar:

a. If two backgrounds are used then the bar should be moved off the screen by using large word spaces instead of character spaces. If there are not enough spaces before the end of the line, then the location of the valid characters should be moved so they appear at the end of the line (and hence no bar); positioning can be compensated using the horizontal start register.

b. If only one background is used, then the other background should be transparent in order to eliminate the bar.

7 - The OSD oscillator external network should consist of a capacitor on each of the OSD oscillator pins to ground together with an inductance between pins. The user should select the two capacitors to be the same value (15pF to 25pF each is recommended). The inductance is chosen to give the desired OSD oscillator frequency for the application (normally 56µH).

SOFTWARE DESCRIPTION

The ST639X software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short to provide byte efficient programming capability. The ST639X Core has the ability to set or clear any register or RAM location bit of the Data space with a single instruction. Furthermore, the program may branch to a selected address depending on the status of any bit of the Data space. The carry bit is stored with the value of the bit when the SET or RES instruction is processed.

Addressing Modes

The ST639X Core has nine addressing modes which are described in the following paragraphs. The ST639X Core uses three different address spaces: Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, the data for immediate mode instructions, and in this space is physically allocated the data ROM which is addressed as data space. Data space contains the Accumulator, the X,Y,V and W registers, the Core control registers, peripheral and Input/Output registers, the RAM locations and the window to address the Data ROM (physically located into the program memory) locations (for storage of tables and constants). Stack space contains six 12-bit RAM bytes used to stack the return addresses for subroutines and interrupts.

Immediate. In the immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In the direct addressing mode, the address of the byte that is processed by the instruction is stored in the location that follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data space memory with a single two-byte instruction.

Short Direct. The Core can address the four RAM registers X,Y,V,W (locations 80H, 81H, 82H, 83H) in the short-direct addressing mode . In this case, the instruction is only one byte long and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of the direct addressing mode. (Note : 80H and 81H are also indirect registers).

Extended. In the extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four less significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) that use the extended addressing mode are able to branch any address of the directly addressable Program space. An extended addressing mode instruction is two-byte long.

Program Counter Relative. The relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to + 16 locations around the address of the relative instruction. If the condition is not true, the instruction that follows the relative instruction is executed. The relative addressing mode instruction is one-byte long. The opcode is obtained by adding the three most significant bits that characterize the kind of test, one bit that determines whether the branch is a toward (when it is 0) or backward (when it is 1) branch and the four less significant bits that give the span of the branch (0H to FH) that must be added or subtracted to the address of the relative instruction to obtain the address of the branch.

Bit Direct. In the bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 directly addressable locations of Data space memory can be set or cleared.

Bit Test & Branch. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit test and branch instruction is three-byte long. The bit identification and the tested condition are included in the opcode byte. The address of the byte to be tested follows immediately the opcode in the Program space. The third byte is the jump displacement, which is in the range from -126 to + 129. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In the indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed by the content of one of the indirect registers, X or Y (80H,81H). The indirect register is selected by the bit 4 of the opcode. A register indirect instruction is one byte long.

Inherent. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

SOFTWARE DESCRIPTION (Continued)

Instruction Set

The ST639X Core has a set of 40 basic instructions. When these instructions are combined with nine addressing modes, 244 usable opcodes can be obtained. They can be divided into six different types : load/store, arithmetic/logic, conditional branch, control instructions, jump/call, bit manipulation. The following paragraphs describe the different types. All the instructions within a given type are presented in individual tables.

Load & Store. These instructions use one,two or three bytes in relation with the addressing mode. One operand is the Accumulator for LOAD and the other operand is obtained from data memory using one of the addressing modes. For LOAD Immediate one operand can be any of the 256 data space bytes while the other is always an immediate data. Refer to Table 18.

Table 18. Load & Store instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
LD A, X	Short Direct	1	4	Δ	*
LD A, Y	Short Direct	1	4	Δ	*
LD A, V	Short Direct	1	4	Δ	*
LD A, W	Short Direct	1	4	Δ	*
LD X, A	Short Direct	1	4	Δ	*
LD Y, A	Short Direct	1	4	Δ	*
LD V, A	Short Direct	1	4	Δ	*
LD W, A	Short Direct	1	4	Δ	*
LD A, rr	Direct	2	4	Δ	*
LD rr, A	Direct	2	4	Δ	*
LD A, (X)	Indirect	1	4	Δ	*
LD A, (Y)	Indirect	1	4	Δ	*
LD (X), A	Indirect	1	4	Δ	*
LD (Y), A	Indirect	1	4	Δ	*
LDI A, #N	Immediate	2	4	Δ	*
LDI rr, #N	Immediate	3	4	*	*

Notes:

X,Y Indirect Register Pointers, V & W Short Direct Registers

. Immediate data (stored in ROM memory)

rr. Data space register

Δ . Affected

* Not Affected

SOFTWARE DESCRIPTION (Continued)

Arithmetic and Logic. These instructions are used to perform the arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while the other can be either a data space memory content or an immediate value in relation with the addressing mode. In CLR,DEC,INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator. Refer to Table 19.

Table 19. Arithmetic & Logic instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	*
AND A, (Y)	Indirect	1	4	Δ	*
AND A, rr	Direct	2	4	Δ	*
ANDI A, #N	Immediate	2	4	Δ	*
CLR A	Short Direct	2	4	Δ	Δ
CLR rr	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
. Immediate data (stored in ROM memory)
rr. Data space register

Δ . Affected
* . Not Affected

SOFTWARE DESCRIPTION (Continued)

Conditional Branch. The branch instructions achieves a branch in the program when the selected condition is met. Refer to Table 20.

Bit Manipulation Instructions. These instructions can handle (set or reset) any bit in data space memory. Refer to Table 21.

Control Instructions. The control instructions control the MCU operations during program execution. Refer to Table 22.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutines call inside the whole program space. Refer to Table 23.

Table 20. Conditional Branch instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b 3-bit address
e 5 bit signed displacement in the range -15 to +16
ee 8 bit signed displacement in the range -126 to +129
rr. Data space register
Δ. Affected
*. Not Affected

Table 21. Bit Manipulation instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes: b 3-bit address; rr. Data space register, * Not Affected

Table 22. Control instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:

1. This instruction is deactivated on ST639X (HW watchdog and a WAIT is automatically executed instead of a STOP)

Δ Affected
*. Not Affected

Table 23. Jump & Call instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes: abc 12-bit address; *. Not Affected

SOFTWARE DESCRIPTION (Continued)

Opcode Map Summary. The following table contains an opcode map for the instructions used on the MCU.

Table 24. Opcode Map

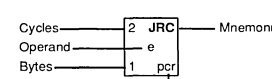
Low / Hi	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Low / Hi
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 prc	2 JRC e 1 prc	4 LD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 pcr	4 LD a,(y) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 pcr	4 LD a,rr 2 dir	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 pcr	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b d	2 JRZ e 1 pcr	4 COM a 1 inh	2 JRC e 1 pcr	4 CP a,(y) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b d	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 pcr	4 CP a,rr 2 dir	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 pcr	2 JRC e 1 prc	4 ADD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 pcr	4 ADD a,(y) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 pcr	4 ADD a,rr 2 dir	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 pcr	2 JRC e 1 prc	4 INC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 pcr	4 INC (y) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 pcr	4 INC rr 2 dir	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	# 1 pcr	2 JRC e 1 prc	4 LD (x),a 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b d	2 JRZ e 1 pcr	# 	2 JRC e 1 pcr	4 LD (y),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 pcr	4 LD rr,a 2 dir	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 AND a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b d	2 JRZ e 1 pcr	4 RLC a 1 inh	2 JRC e 1 pcr	4 AND a,(y) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 pcr	4 AND a,rr 2 dir	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 SUB a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 pcr	4 SUB a,(y) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 pcr	4 SUB a,rr 2 dir	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	# 	2 JRC e 1 prc	4 DEC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 pcr	4 DEC (y) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	# 	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 pcr	4 DEC rr 2 dir	F 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement



ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that VI and VO must be higher than V_{SS} and smaller than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature. Tj, in Celsius can be obtained form.:

$$Tj = TA + PD \times RthJA$$

Where: TA = Ambient Temperature,
RthJA = Package thermal resistance (junction-to ambient),

PD = Pint + Pport,

Pint = $I_{DD} \times V_{DD}$ (chip internal power),

Pport = Port power dissipation (determined by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
V_I	Input Voltage (AFC IN)	V_{SS} – 0.3 to +13	V
V_I	Input Voltage (Other Inputs)	VSS – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage (PA4-PA7, PC4-PC7, DA0-DA5, O0, O1)	V_{SS} – 0.3 to + 13	V
V_O	Output Voltage (Other Inputs)	VSS – 0.3 to V_{DD} +0.3	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}, PA6, PA7	± 10	mA
I_O	Current Drain per Pin (PA6, PA7)	± 50	mA
IV_{DD}	Total Current into V_{DD} (source)	50	mA
IV_{SS}	Total Current out of V_{SS} (sink)	150	mA
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	– 60 to 150	°C

Note Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these conditions is not implied Exposure to maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PSDIP42			67	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature		0		70	°C
V_{DD}	Operating Supply Voltage		4.5		6.0	V
f_{OSC}	Oscillator Frequency RUN & WAIT Modes			8.0	8.1	MHz
f_{OSDOSC}	On-Screen Display Oscillator Frequency				8.0	MHz

EEPROM INFORMATION

The ST639X EEPROM macrocell and the single poly EEPROM process have been specially developed to achieve 1.000.000 Write/Erase cycles and a 10 years data retention.

DC ELECTRICAL CHARACTERISTICS

(T_A= 0 to + 70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	All I/O Pins			0.2 x V_{DD}	V
V_{IH}	Input High Level Voltalge	All I/O Pins	0.8 x V_{DD}			V
V_{HYS}	Hysteresis Voltage(1)	All I/O Pins V_{DD} = 5V		1.0		V
V_{OL}	Low Level Output Voltage	DA0-DA5, PB0-PB6, OSD Outputs, PC0-PC7, O0, O1, PA0-PA5, 62.5KHz OUT V_{DD} = 4.5V I_{OL} = 1.6mA I_{OL} = 5.0mA			 0.4 1.0	 V V
V_{OL}	Low Level Output Voltage	PA0-PA7, V_{DD} = 4.5V I_{OL}= 1.6mA I_{OL}= 25mA			 0.4 1.0	 V V
V_{OL}	Low Level Output Voltage	OSDOSCOUT, OSCOUT, V_{DD} = 4.5V I_{OL}= 0.4mA			 0.4	 V
V_{OH}	High Level Output Voltage	PB0-PB7, PA0-PA3, OSD Outputs, PC0-PC3, 62.5KHz OUT, V_{DD} = 4.5V I_{OH} = – 1.6mA	 4.1			 V
V_{OH}	High Level Output Voltage	OSDOSCOUT, OSCOUT, V_{DD} = 4.5V I_{OL}= – 0.4mA	 4.1			 V
I_{PU}	Input Pull Up Current Input Mode with Pull-up	PB0-PB6, PA0-PA3, PC0-PC3 V_{IN}= V_{SS}	– 100	– 50	– 25	µA
I_{IL} I_{IH}	Input Leakage Current	OSCIN V_{IN}= V_{SS} V_{IN}= V_{DD}	 – 10 0.1	 – 1 1	 – 0.1 10	 µA
I_{IL}	Input Pull-down current in Reset	OSCIN ST6394,96,99 Only	 100			 µA
I_{IL} I_{IH}	Input Leakage Current	All I/O Input Mode no Pull-up OSDOSCIN V_{IN}= V_{DD} or V_{SS}	 – 10		 10	 µA
V_{DD}RAM	RAM Retention Voltage in RESET	ST6394,95,96	1.5			V
I_{IL} I_{IH}	Input Leakage Current	Reset Pin with Pull-up V_{IN}= V_{SS}	– 50	– 30	– 10	µA
I_{IL} I_{IH}	Input Leakage Current	AFC Pin V_{IH}= V_{DD} V_{IL}= V_{SS} V_{IH}= 12.0V	 – 1		 1 40	 µA
I_{OH}	Output Leakage Current	DA0-DA5, PA4-PA5, PC0-PC7, O0, O1 V_{OH} = V_{DD}			 10	 µA
I_{OH}	Output Leakage Current High Voltage	DA0-DA5, PA4-PA7, PC4-PC7, O0, O1 V_{OH} = 12V			 40	 µA

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{DD}	Supply Current RUN Mode	f_{OSC}= 8MHz, ILoad= 0mA V_{DD}= 6.0V		6	16	mA
I_{DD}	Supply Current WAIT Mode	f_{OSC}= 8MHz, ILoad= 0mA V_{DD}= 6V		3	10	mA
I_{DD}	Supply Current at transition to RESET (ST6394,95,96)	f_{OSC}= Not App, ILoad= 0mA V_{DD}= 6V		0.1	1	mA
V_{ON}	Reset Trigger Level ON	RESET Pin			0.3 x V_{DD}	V
V_{OFF}	Reset Trigger Level OFF	RESET Pin	0.8 x V_{DD}			V
V_{TA}	Input Level Absolute Tolerance	A/D AFC Pin V_{DD} = 5V			±200	mV
V_{TR}	Input Level Relatice Tolerance (1)	A/D AFC Pin Relative to other levels V_{DD} = 5V			±100	mV

Note 1 Not 100% Tested

AC ELECTRICAL CHARACTERISTICS

(T_A= 0 to + 70°C, f_{OSC} = 8MHz, V_{DD} = 4.5V to 6.0V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{WRES}	Minimum Pulse Widht	RESET Pin	125			ns
t_{OHL}	High to Low Transition Time (2)	PA6, PA7 V_{DD} = 5V,CL = 1000pF (2)		100		ns
t_{OHL}	Low to High Transition Time	DA0-DA5, PB0-PB6, OSD Outputs, PC0-PC7 V_{DD} = 5V, CL = 100pF		20		ns
t_{OLH}	High to Low Transition Time	PB0-PB6, PA0-PA3, OSD Outputs, PC0-PC3 V_{DD} = 5V, CL = 100pF		20		ns
t_{OH}	Data HOLD Time SPI after clock goes low I^2CBUS/S-BUS Only	ST6391,93 ST6396,99	750			ns
		ST6394 Only	125			ns
f_{DA}	D/A Converter Repetition Frequency (1)	ST6391, 93, 94, 96, 99		31.25		KHz
		ST6395		25		KHz
f_{SIO}	SIO Baud Rate (1)	ST6391, 93, 94, 96, 99 ST6395 Only		62.50 100		KHz
f_{OUT1}	62.5KHz Output (1)	ST6399 Only		62.50		KHz
t_{WEE}	EEPROM Write Time	T_A = 25 °C One Byte		5	10	ms
Endurance	EEPROM WRITE/ERASE Cycles	Q_A LOT Acceptance Criteria	300.000	> 1 million		cycles
Retention	EEPROM Data Retention (4)	T_A = 25°C	10			years
C_{IN}	Input Capacitance (3)	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance (3)	All outputs Pins			10	pF

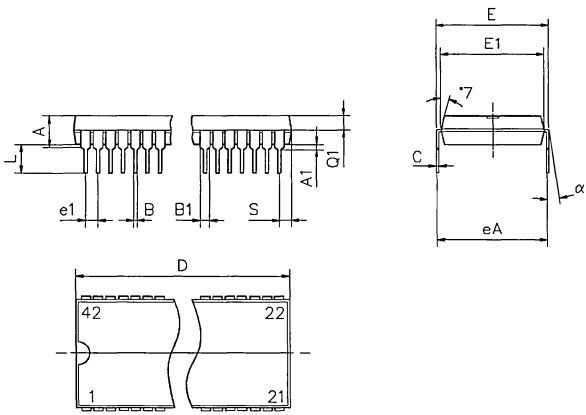
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
COSCIN, COSCOUT	Oscillator Pins Internal Capacitance (3)			5		pF
COSDIN, COSDOUT	OSD Oscillator External Capacitance	Recommended	15		25	pF

Notes: 1. A clock other than 8 MHz will affect the frequency response of those peripherals (D/A, 62.5KHz and SPI) whose clock is derived from the system clock.
2 The rise and fall times of PORT A have been reduced in order to avoid current spikes while maintaining a high drive capability
3. Not 100% Tested
4. Based on extrapolated data

PACKAGE MECHANICAL DATA

Figure 68. 42-Pin Shrink Dual in Line Plastic (JEDEC MO-015 BB)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3 81		5.08	0 15		0.20
A1	0.51		1.78	0.020		0 070
B	0.35		0 59	0.013		0.023
B1	0.75		1.42	0.029		0.056
C	0 20		0.36	0 008		0.014
D			39 12			1.540
E	15 24		15.87	0 60		0.62
E1	12.70		14.48	0.50		0.57
e1		1.78			0.070	
eA		15 24			0.600	
L	2 54		3 40	0.10		0 13
Q1	1 52		2 29	0 20		0.09
S	0.76		2.67	0.03		0 105
α	0		15°	0		15°

ORDERING INFORMATION

The following chapter deals with the procedure for transfer the Program/Data ROM codes to SGS-THOMSON.

Communication of the ROM Codes. To communicate the contents of Program /Data ROM memories to SGS-THOMSON, the customer has to send:

- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the PROGRAM Memory
- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the ODD and EVEN ODD OSD Characters
- one file in INTEL INTELLEC 8/MDS FORMAT (either as an EPROM or in a MS-DOS 5" diskette) for the EEPROM initial content (this file is optional)
- a filled Option List form as described in the OPTION LIST paragraph.

The program ROM should respect the ROM Memory Map as in Table 25.

The ROM code must be generated with ST6 assembler. Before programming the EPROM, the buffer of the EPROM programmer must be filled with FFH. For shipment to SGS-THOMSON the EPROMs should be placed in a consecutive IC carrier and packaging carefully.

ORDERING INFORMATION (Continued)

Table 25. ROM Memory Map

ROM Page	Device Address	EPROM Address (1)	Description
Page 0	0000H-007FH 0080H-07FFH	0000H-007FH 0080H-07FFH	Reserved User ROM
Page 1 "STATIC"	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	0800H-0F9FH 0FA0H-0FEFH 0FF0H-0FF7H 0FF8H-0FFBH 0FFCH-0FFDH 0FFEH-0FFFH	User ROM Reserved Interrupt Vectors Reserved NMI Vector Reset Vector
Page 2	0000H-000FH 0010H-07FFH	1000H-100FH 1010H-17FFH	Reserved User ROM
PAGE 3	0000H-000FH 0010H-07FFH	1800H-180FH 1810H-1FFFH	Reserved user ROM (2)
Page 4	0000H-000FH 0010H-07FFH	2000H-200FH 2010H-27FFH	Reserved User ROM
Page 5	0000H-000FH 0010H-07FFH	2800H-280FH 2810H-2FFFH	Reserved User ROM
Page 6	0000H-000FH 0010H-07FFH	3000H-300FH 3010H-37FFH	Reserved User ROM
Page 7	0000H-000FH 0010H-07FFH	3800H-380FH 3810H-3FFFH	Reserved User ROM (3)
Page 8	0000H-000FH 0010H-07FFH	4000H-400FH 4010H-47FFH	Reserved User ROM
Page 9	0000H-000FH 0010H-07FFH	4800H-480FH 4810H-4FFFH	Reserved User ROM (4)

Notes:
1. EPROM addresses are related to the use of ST63P9X piggyback emulation devices.
2. End address for ST6394
3. End address for ST6391,93,99
4. End address for ST6395,96

ORDERING INFORMATION (Continued)

Customer EEPROM Initial Contents: Format

a. The content should be written into an INTEL INTELLEC format file.

b. In the case of 128 bytes of EEPROM, the starting address in 000h and the end in 7Fh.

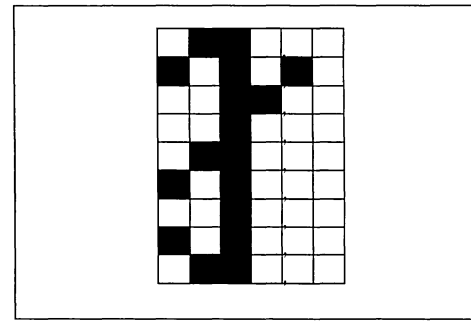
c. In the case of 384 bytes of EEPROM, the starting address is 000H and the end address is 7FH. The order of the pages (64 bytes each) is an in the specification (ie. b7, b1 b0: 001, 010, 011, 101, 110. 111).

d. Undefined or don't care bytes should have the content FFH.

OSD Test Character. In order to allow the testing of the on-chip OSD macrocell the following character must be provided at the fixed 3FH (63) position of the second OSD bank.

Listing Generation & Verification. When SGS-THOMSON receives the Codes, they are compared and a computer listing is generated from them. This listing refers extractly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed list constitutes a part of the contractual agreement for the creation of the customer mask. SGS-THOMSON sales organization will provide detailed information on contractual points.

Figure 69. OSD Test Character



Ordering Information Table

Sales Type	ROM/EEPROM Size	Temperature Range	Package
ST6391B1/XX	16K/128 Bytes	0 to + 70 ° C	PSDIP42
ST6393B1/XX	16K/128 Bytes	0 to + 70 ° C	PSDIP42
ST6394B1/XX	8K/384 Bytes	0 to + 70 ° C	PSDIP42
ST6395B1/XX	20K/384 Bytes	0 to + 70 ° C	PSDIP42
ST6396B1/XX	20K/384 Bytes	0 to + 70 ° C	PSDIP42
ST6399B1/XX	16K/128 Bytes	0 to + 70 ° C	PSDIP42

Note: "XX" Is the ROM code identifier that is allocated by SGS-THOMSON after receipt of all required options and the related ROM file.

ST639X MICROCONTROLLER OPTION LIST

Customer: . . . . . .

Address: . . . . . .

Contact: . . . . . .

Phone No: . . . . . .

Reference: . . . . . .

Device [ ] (d) Package [ ] (p) Temperature Range [ ] (t)

For marking one line with 10 characters maximum is possible

Special Marking [ ] (y/n) Line1 " _ _ _ _ _ _ _ _ _ _ " (N)

Notes:

(d) 1= ST6391, 2 = ST6393, 3 = ST6394, 4 = ST6395, 5 = ST6396, 6 = ST6399

(p) B= Dual in Line Plastic

(t) 1= 0 to 70°C

(N) Letters, digits, ' . ', ' - ', ' / ' and spaces only

Marking: the default marking is equivalent to the sales type only (part number).

OSD POLARITY OPTIONS (Put a cross on selected item) :

	POSITIVE	NEGATIVE
VSYNC,HSYNC	[ ]	[ ]
R,G,B	[ ]	[ ]
BLANK	[ ]	[ ]

CHECK LIST:

	YES	NO
ROM CODE	[ ]	[ ]
OSD Code: ODD & EVEN	[ ]	[ ]
EEPROM Code (if Desired)	[ ]	[ ]

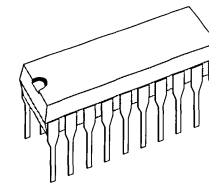
Signature .....

Date .....

ON-SCREEN DISPLAY

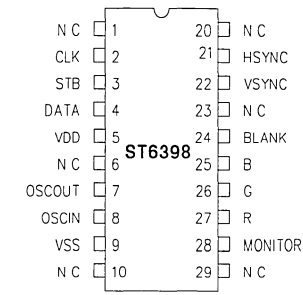
ADVANCE DATA

- Display format of 26 characters x 11 rows
- Character Matrix of 12 x 18 pixels
- Character color selectable on a character by character basis. (up to four different colors per screen).
- Character fonts: 128 ROM and 4 RAM based characters.
- Character background selectable on a character by character basis (no background, background 1 or background 2 ; one backround color set per screen).
- Character border (fringe) enable/disable for each row (one border color per screen).
- Programmable vertical and horizontal start position for the display.
- Programmable horizontal offset position for each row.
- Row enable/disable feature.
- Raster Control: The whole screen can be displayed in a color (display off, screen background enabled) or together with the characters (display on, screen background enabled); or transparent (display on/off,screen backround disabled).
- Vertical row spacing: Rows can be spaced or squeezed by up to 17 lines; a squeezed row will have its height reduced by skipping the required number of lines.
- An extra pin MONITOR (enable / disable) is available to indicate the presence of a character pixel or border (fringe).
- Microcontroller interface with a 3 line serial bus
- Oscillator enable/disable.
- Package: 20 pins DIP (300 mils).
- Power Supply: 4.5 to 5.5 volts.



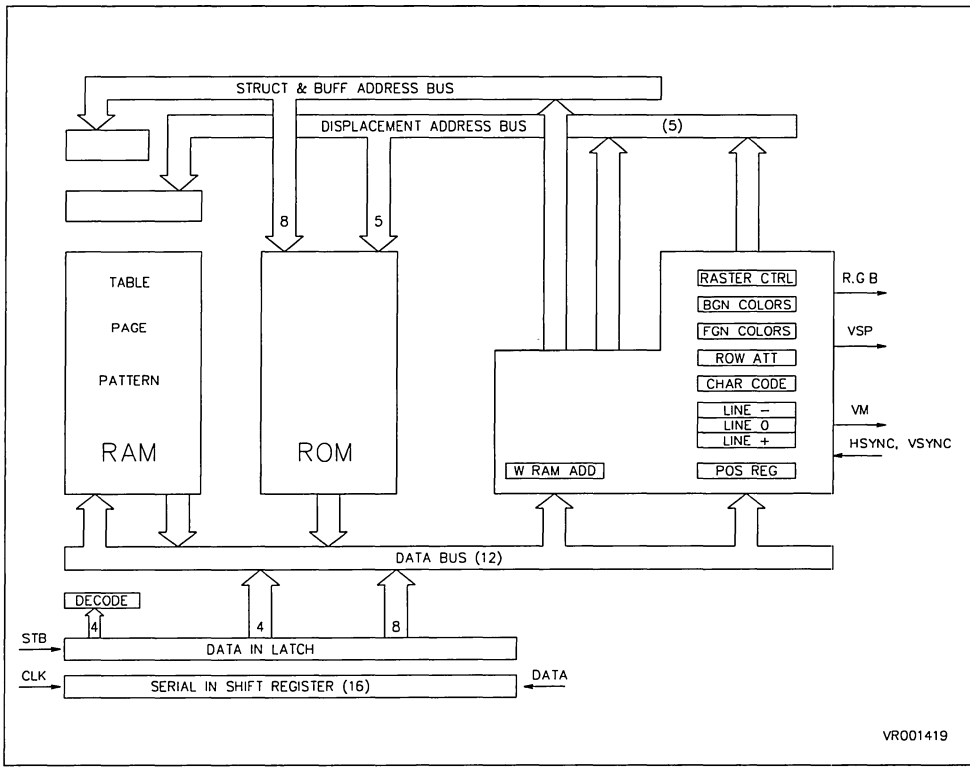
PDIP20

Figure 1. ST6398 Pin Configuration



This is an advance information from SGS-THOMSON Details are subject to change without notice

Figure 2. ST6398 Block Diagram



GENERAL DESCRIPTION

The ST6398 is a stand alone on-screen-display peripheral with advanced features.

The device is controlled by an external microcontroller via the serial bus interface. Four characters which can be defined in RAM give great flexibility since characters can be defined and redefined via the serial bus without limit and without changing the character ROM mask. Updating of control registers and characters via the serial bus is not limited to the flyback intervals but can also be performed during the display of characters. Most information is stored in on-chip RAM organized in three main structures: page, attribute and pattern store. The data for the 12-bit words is entered via the serial bus however it is not necessary to redefine all twelve bits via the serial bus when writing similar data to successive addresses.

The device (sales type ST6398B1/B) is delivered with a standard set of ROM based characters; extra characters particular to the application are defined via the RAM characters. If a customized set of ROM based characters is required then contact your SGS-THOMSON sales office.

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied via these two pins. V_{DD} is power and V_{SS} is the ground connection.

DATA. Serial bus data input; high impedance.

CLK. Serial bus clock input; high impedance.

STB. Serial bus strobe input; high impedance.

OSCIN and OSCOUT. These are the oscillator terminals for the on screen display. A capacitor and coil network should be connected across these pins in order to provide the desired oscillation frequency.

HSYNC. Horizontal synchronization input; high impedance. When the signal goes high the OSD oscillator is started and characters can be displayed. A different polarity can be defined with a customized ROM mask.

VSYNC. Vertical synchronization input, high impedance. When the signal goes high, this indicates the start of the TV display. The OSD oscillator is not affected by this signal. A different polarity can be defined with a customized ROM mask.

R, G, B, BLANK. Color and blanking outputs; push-pull. These outputs are all active high. A different polarity can be defined with a customized ROM mask.

MONITOR. Output pin which indicates the presence of a character pixel or border; push-pull. This output is active LOW. A different polarity can be defined with a customized ROM mask.

NC. The pins are not used in the application and should be left unconnected.

ST6398 ARCHITECTURE OVERVIEW

The ST6398 consists of the following blocks:

- SERIAL MICROPROCESSOR INTERFACE. Most data received through this interface is stored in the on-chip RAM.
- RAM. The RAM holds 12-bit words. It is logically organized in three structures: PAGE, ATTRIBUTE TABLE, PATTERN STORE.
- ROM. This is where the 128 ROM based characters are stored.
- TIMING GENERATOR: This is synchronized by the VSYNC and HSYNC inputs. Its timing is derived from the oscillator (7.5MHz nomimal).
- MEMORY ADDRESS MODULE. Controls the addressing of the RAM and ROM.
- PIXEL LOGIC. Used to determine when to output the color, blanking or monitor information including the backgrounds and border.

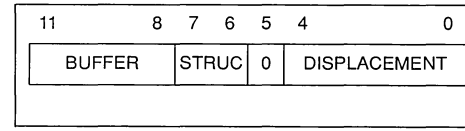
RAM STRUCTURE

RAM Addressing

Random access to any word is performed by a logical 11 bit address, comprised of three fields (see Ram Memory Map):

- A Structure Identifier: 2 bits.
- A Buffer Index: 4 bits.
- A Displacement from the buffer origin: 5 bits.

Figure 3. RAM Addressing



RAM Structure Description

The three structures PAGE, ATTRIBUTE TABLE and PATTERN STORE are divided as follows:

PAGE:

- 11 row buffers, numbered from 0 to 10. Each row buffer holds 26 character words. Inside a buffer, characters words are numbered from 0 to 25; Sequential addressing: Character first, then row buffer.

ATTRIBUTE TABLE:

- 11 row attribute words (0 to 10). Each of the row attribute words (0 to 10) controls the display of the corresponding row buffer.
- The foreground colors (word number 12) which holds the 4 color foreground set (FC0 to FC3).
- The background colors (word number 13) which holds the 2 color character background set (BC0 and BC1), the foreground border color (FBC) and the screen background color (SBC).
- The raster control (word number 14).
- The position register (word number 15) which has been mapped into the RAM for convenience.

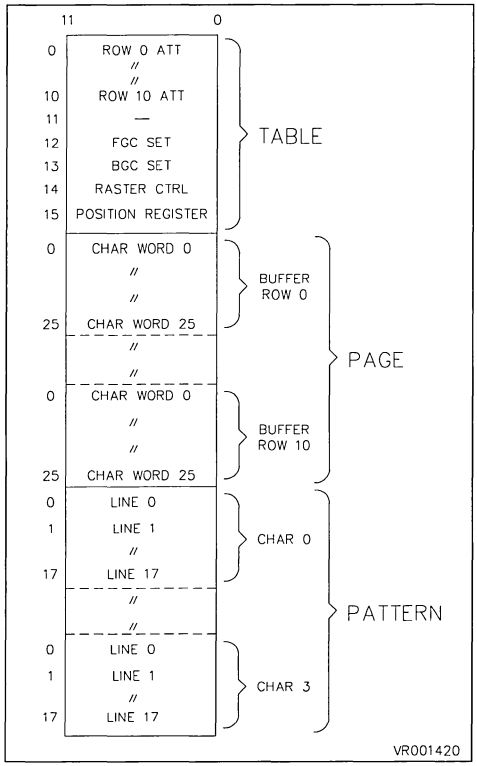
The raster control word, foreground color word, background color word and the current row attribute word are retrieved at the begining of each tv line.

PATTERN STORE:

- Sufficient RAM to describe four character patterns (0 to 3).
  Each character pattern is comprised of 18 pattern lines (0 to 17; one word each). Line 0 is displayed topmost; the msb is displayed leftmost. Sequential addressing: Line first, then character index.

RAM STRUCTURE (Continued)

Figure 4. RAM Memory Map



SERIAL INTERFACE

Microprocessor Interface

The OSD RAM is down loaded from the microcontroller through the three input pins DATA, CLK and STB.

At the rising edge of CLK the DATA input is sampled and shifted in; either 0 bit, 8 bit or 16 bit messages can be received. The MSB is transmitted first.

At the rising edge of STB the number of clock periods counted from last falling edge of STB is sampled; the clock is ignored when STB is high.

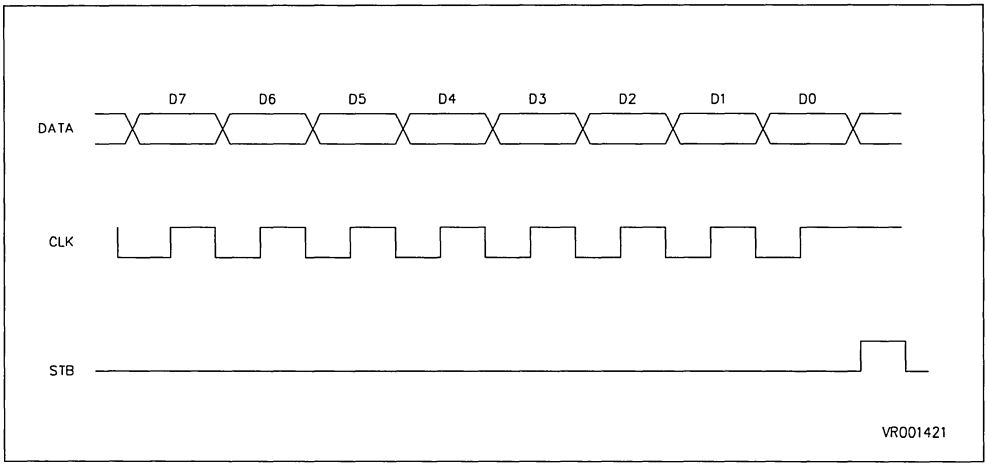
According to this count 0, 8 or 16 bits from the shift register are latched into the 16 bit DATA IN register. Short messages do not modify the most significant bits of DATA IN. The twelve least significant bits of DATA IN can be transfered either to the RAM as DATA or as the WRITE RAM ADDRESS depending on the four most significant bits (4 bit tag).

Transfer to the RAM is done into the location currently pointed to by the WRITE RAM ADDRESS register; this register is automatically post-incremented.

The STB raising edge requests a transfer which is quickly granted providing that the oscillator is running. As the oscillator is blocked during HSYNC, the STB worse case minimum period is related to the maximum HSYNC duration and the oscillator period.

SERIAL INTERFACE (Continued)

Figure 6. Serial Bus Waveforms



Writing To RAM

Writing into RAM consists of two steps:

a. Sending a RAM address.
This selects a starting address in a given structure, together with an auto-incrementation scheme (see auto-incrementation).

b. Sending a string of DATA TO RAM messages. These will be stored sequentially in the selected structure from the starting address.

Long Messages

The 16 bit message consists of:

– A 12 bit word.

– A 4 bit tag (most significant bits).

Figure 5. Summary of 16-Bit Messages

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	BUF				STRUC		0	DISPLACEMENT					RAM ADDRESS
0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	LONG DATA TO RAM
0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	DISABLE OSCILLATOR
0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	RESET

Auto-incrementation

Sequential addressing is performed by an automatic incrementation of the address after every command that loads data into the RAM; it is therefore not necessary to redefine the address when addressing sequentially.

The auto-incrementation is valid for the TABLE (a single buffer structure which contains the attributes and general control registers) and the PATTERN STORE (a four buffer structure which contains the definition of the RAM based characters).

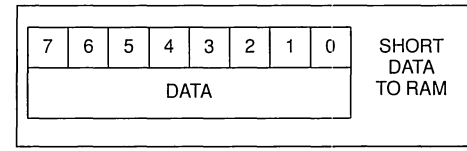
When in PAGE (an 11 buffer structure which defines the characters used on each line), the auto-incrementation can be programmed to wrap-around from the last character of a row either to the begining of the same row or to the begining of next row depending on the value of the two bits that define the structure (as defined the the table below). Refer also to RAM ADDRESSING section.

The TABLE holds a single buffer so auto-incrementation to the next buffer is not applicable. Note that auto-incrementation never allows you to go from one structure to the next one: after the last address of any structure, an illegal address is reached (some are reserved for testing) so AFTER WRITING THE LAST WORD OF ANY STRUCTURE, THE ADDRESS MUST BE REINITIALIZED

Short Data To Ram Messages

In order to minimize the transmission time of character words (or row attributes) differing only by the eight least significant bits, the common four most significant bits may be transmitted only once. This is done by transmitting these MSBs, together with the first word, in a full size 16 bit message (long data to RAM). The subsequent strings may then be compressed by using the short DATA TO RAM message (8 bits).

Figure 7. Short Data to RAM Format



A more radical compression can be achieved when a string of identical words is down loaded into RAM at successive addresses. This is done, as already suggested, by sending the common value once, and then by toggling STB without toggling CLK. This 0 bit message writes the full current content of the DATA IN register into RAM.

Reset And Disable Oscillator Messages

In order to initialize the circuit after power on, it is mandatory to send TWO SUCCESSIVE RESET MESSAGES; this procedure resets the clock count and starts the oscillator.

The oscillator starts regardless of the SYNC input terminals. The RESET messages clear the raster control word (screen background transparent, display disabled). After these two RESET messages the OSD is ready to store subsequent messages. After a DISABLE OSCILLATOR message, the oscillator stops immediately. As long as the oscillator is stopped, the video output terminals remain in their retrace state: RGB, BLANK and MONITOR are all inactive. The RAM contents remain unmodified. When OSD is not in use it is best to disable the oscillator. The oscillator can be restarted by a single RESET message.

Table 1. Auto-Incrementation to Next Buffer Summary

Structure	Buffer Index	Displacement	To Next Buffer by Auto-Incrementation
Page 00	0 to 10	0 to 25	YES
Page 01	0 to 10	0 to 25	NO
Pattern 10	0 to 3	0 to 17	YES
Table 11	0	0 to 15	N/A

RAM DATA FORMAT

Page: Character Word Format

Figure 8. Character Words

11	10	9	8	7	6	5	4	3	2	1	0
FS1	FS0	BE	BS	CHAR INDEX							

CHAR INDEX

0xxxxxxx Addresses one character pattern out of 128 in ROM.

100000xx Addresses one character out of 4 in RAM pattern store.

BE	BS	Character background color selection
1	0	Selects BC0 (in background color word)
1	1	Selects BC1 (in background color word)
0	-	Disables character background; the screen background is therefore displayed if enabled (SBC Screen Background Color in background color word). If SBE = 0 in the raster control word then there is no screen background; if SBE = 1 screen background color is displayed.

FS1	FS0	Character foreground color selection.
0	0	Selects FC0 (in foreground color word).
0	1	Selects FC1 (in foreground color word).
1	0	Selects FC2 (in foreground color word).
1	1	Selects FC3 (in foreground color word).

Note on Blanking:

Whenever a background, border or character is outputed, the BLANK signal will also go high This is used to externally switch off the normal screen display so that the RGB signals from the OSD can be displayed.

Table

ROW ATTRIBUTE WORDS (numbered 0 to 10).

Figure 9. Row Attribute Word

11	10	9	8	7	6	5	4	3	2	1	0
HPOS OFFSET				RE	FBE	VPOS OFFSET					

HPOS OFFSET: Adds a horizontal offset (0 to 15 Tosc) to the basic horizontal position for any line belonging to the row (bit 8 is lsb).

VPOS OFFSET:

0xxxxx Adds n (0 to 17) tv lines at the top of the plain 18 line row. These lines are displayed in the character background color (as defined by the current BE, BS) during character period. During the horizontal front and back porch period these lines are displayed in the screen background if enabled or transparent if disabled (bit 0 is lsb).

1xxxxx Jumps directly to line n (0 to 17) in the display of that particular row. This means that the row height is reduced by n lines (bit 0 is lsb).

FBE:	Foreground border (fringe) enable.
0	Border (fringe) effect disabled.
1	Border (fringe) effect enabled; any background pixel in the vicinity of a foreground pixel is diplayed in foreground border color (fetched from the background color word).

RE:	Row Enable
0	The row is disabled; nothing is displayed except the screen background color if enable; VPOS OFFSET is still interpreted.
1	Row enable

RAM DATA FORMAT (Continued)

FOREGROUND COLOR WORD (number 12)

Figure 10. Foreground Color Word

11	10	9	8	7	6	5	4	3	2	1	0
FC3			FC2			FC1			FC0		

FC0 to FC3: The foreground color word holds the character foreground color set.

Each of the above defines an RGB triplet (B is the LSB):

RGB	COLOR
000	Black
001	Blue
010	Green
011	Cyan
100	Red
101	Magenta
110	Yellow
111	White

BACKGROUND COLOR WORD (number 13)

Figure 11. Background Color Word

11	10	9	8	7	6	5	4	3	2	1	0
SBC			FBC			BC1			BC0		

BC0, BC1: Defines the background color set definitions.

FBC: Defines the character border (fringe) color.

SBC: Defines the screen background color.

Each of the above defines an RGB triplet (B is the LSB):

RGB	COLOR
000	Black
001	Blue
010	Green
011	Cyan
100	Red
101	Magenta
110	Yellow
111	White

RASTER CONTROL WORD (number 14).

Figure 12. Raster Control Word

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	DON	FME	SBE

SBE: Screen Background Enable.
0 Screen background is off; the normal video image is enabled.
1 The screen background is enabled; the video image is disabled by the BLANK signal (raster blanking) and the screen is forced to the color defined by SBC (screen background color).

FME: Foreground Monitoring Enable.
0 Disabled. MONITOR output terminal stays active.
1 Enabled. MONITOR output terminal is activated only at the time when a character pixel or border (fringe) is being displayed; it is inactive in all other cases (eg. background display).

DON:
0 The display is OFF; all the characters are disabled; the full screen displayed as either "transparent" or "blanked" depending on the state of SBE.
1 The OSD character display is ON.

POSITION REGISTER (number 15).

Figure 13. Raster Control Word

11	10	9	8	7	6	5	4	3	2	1	0
VPOS						HPOS					

VPOS: Vertical start position; counts 1 to 63 lines from the top of the screen.
HPOS: Horizontal start position; counts 5 to 63 oscillator periods from the left of the screen.

NOTE: Correct operation is not guaranteed if these parameters are programmed under the minimum values given above

RAM DATA FORMAT (Continued)

PATTERN WORDS

Figure 14. Pattern Words

11	10	9	8	7	6	5	4	3	2	1	0
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11

Word 0 in the pattern buffer is displayed topmost on the screen.

Most significant bit is displayed on the left of the screen.

The foreground pixels are set to 1.

The background pixels (ie. no pixel) are 0.

This set of rules also applies to the ROM pattern store.

VIDEO TIMING

Introduction

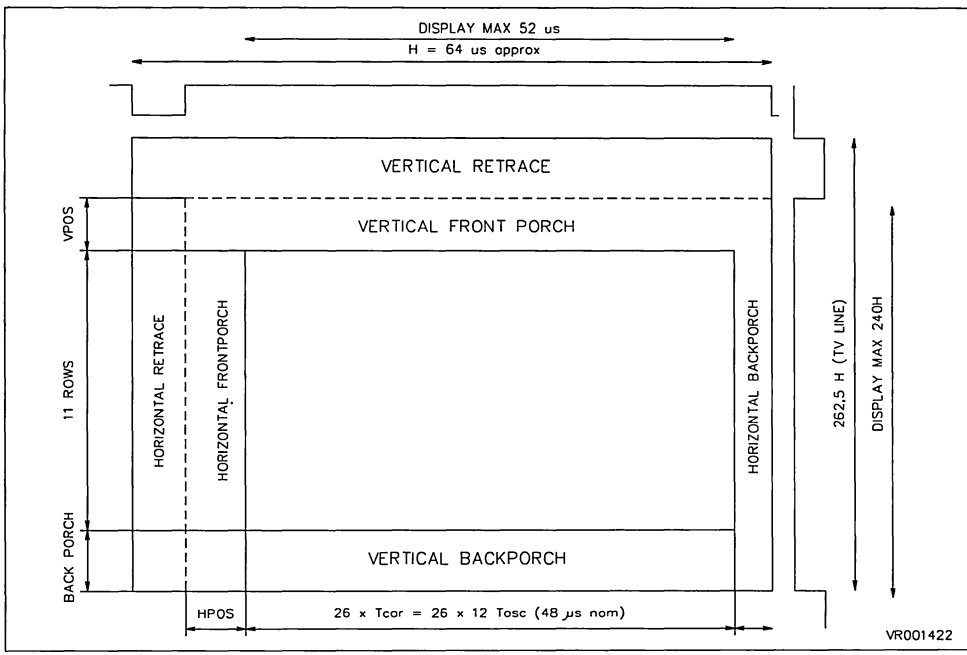
The OSD cycles through three main states: RETRACE, PORCH and CHARACTER.

The vertical and horizontal RETRACE are determined by the VSYNC and HSYNC signals.

The vertical and horizontal FRONT PORCH are determined by the POSITION REGISTER. For the vertical front porch, VPOS horizontal lines are counted down from the VSYNC trailing edge. For the vertical front porch HPOS + HPOS OFFSET clock periods are counted down from the HSYNC trailing edge.

The CHARACTER state is when the 11 rows of 26 CHARACTERS are interpreted. The horizontal and vertical BACK PORCH occur after the last character or row respectively.

Figure 15. Typical OSD Display



VIDEO TIMING (Continued)

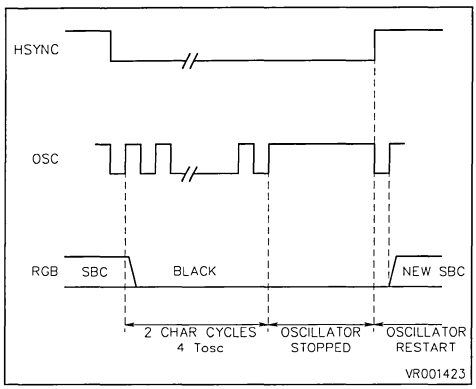
Horizontal Timing

The leading edge of HSYNC is resynchronized at TOSC and the 24 subsequent oscillator periods (2 character cycles) are used to fetch the current row attribute word, the foreground color word, the background color word and the raster control word. The oscillator is then is stopped.

HSYNC lasts nominally for 10us depending on the application. When enabled, the oscillator is restarted at the trailing edge of HSYNC. HPOS + HPOS ROW OFFSET oscillator periods are counted during this HORIZONTAL FRONT PORCH period. After this the 26 CHARACTER periods (12 Tosc each) are counted. The HORIZONTAL BACK-PORCH period occurs after the last character while waiting for the next HSYNC.

If HSYNC arrives before the end of the 26th character, then there will be no backporch; HSYNC will restart full line process.

Figure 16. Horizontal Timing During Retrace



Vertical Timing

VSYNC marks the vertical retrace. It lasts nominally for 0.9 ms (14 TV lines) but will depend on the application. The VSYNC signal has no influence on the oscillator and does not start or stop it.

VPOS lines (leading HSYNC edges) are counted down during VERTICAL FRONT PORCH PERIOD. VPOS is a 6 bit binary parameter.

During the display of the eleven rows, the number of lines per row depends on the VPOS OFFSET row attribute. The VERTICAL BACKPORCH period occurs after the last row while waiting for the next VSYNC.

Ram Time Sharing

The RAM is cycled in 2 tosc (300 ns approximately) so that six access time slots can be provided along any character display period (12 tosc):

Four slots are reserved for character interpretation: one slot for fetching the character word and three slots for fetching three successive character lines in the pattern store (this is required for deriving the foreground border when the character pattern is stored in RAM).

The two remaining slots are available to store a serially received word.

VIDEO OUTPUT

Retrace And Porch

The video terminal outputs RGB, BLANK and MONITOR are driven according to:

- The video timing state: RETRACE, PORCH or CHARACTER;
- The programmed context retrieved from RAM.

DURING RETRACE

- RGB are inactive.
- BLANK and MONITOR are inactive. These values prevail also during the full field when the oscillator has been disabled.

DURING PORCH

- RGB are inactive unless the screen background is enabled (SBE=1) in which case RGB will set to the screen background color (SBC).
- BLANK is inactive unless the screen background is enabled (SBE=1) in which case it will be active.
- MONITOR is inactive. These values prevail also during the character period when the display is disabled (DON =0) or when the current row is disabled (RE=0 in the current row attribute word).

Character State

CHARACTER DISPLAY

During a character display, the video terminal outputs are driven according to the pixel type, the current row attribute word, the foreground and background color words , the raster control word and the oscillator status. In this section the following is assumed: oscillator enabled, display enabled, row enabled.

The pattern indexed by the character word is mapped onto the screen and determines the pixel type:

- Foreground. Active when the bit in the pattern store is set to 1.
- Background: When the bit in the pattern store is reset to 0 and when not in the vicinity of a foreground pixel, then the background will be displayed. When VPOS adds n tv lines to the row, these extra lines will be implicitly displayed as background pixels.
- Border (or fringe): The border occurs when the bit in the pattern store is reset to 0, when in the vicinity of at least one foreground pixel and when FBE=1 in the row attribute word. If FBE=0 then there is no border. The border will outline the shape of the character.

VICINITY

Each pixel has four neighbours (two vertical, two horizontal). The vicinity is horizontally continuous from character to character so that the first column of a charactacter neighbours the last column of the previous character. Vicinity is not vertically cointinuous between different lines. Refer to the following diagram for examples on vicinity in order to see how the border is formed.

Figure 17. Examples of Borders

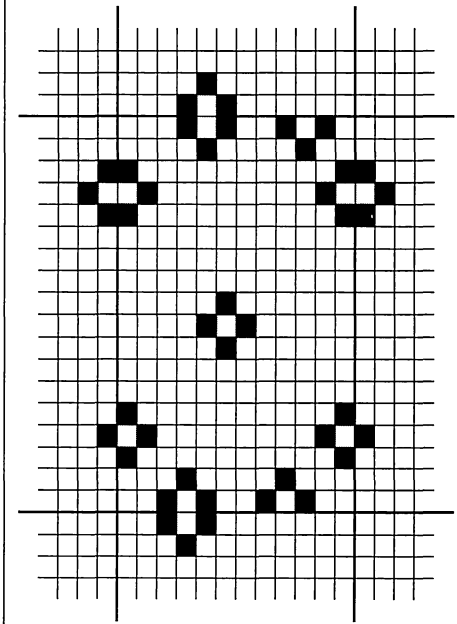


Table 2. The Different Character States

Type of Pixel Condition	Outputs		
	RGB	Blank	Monitor *
Background BE = 1 BE = 0, SBE = 1 BE = 1, SBE = 0	 Background color Screen background Inactive (Black)	 Active Active Inactive	 Inactive Inactive Inactive
Foreground	Character color	Active	Active
Border FBE = 1	Border color (FBC)	Active	Active

Note : * Assumes VME = 1; when VME = 0, MONITOR remains active.

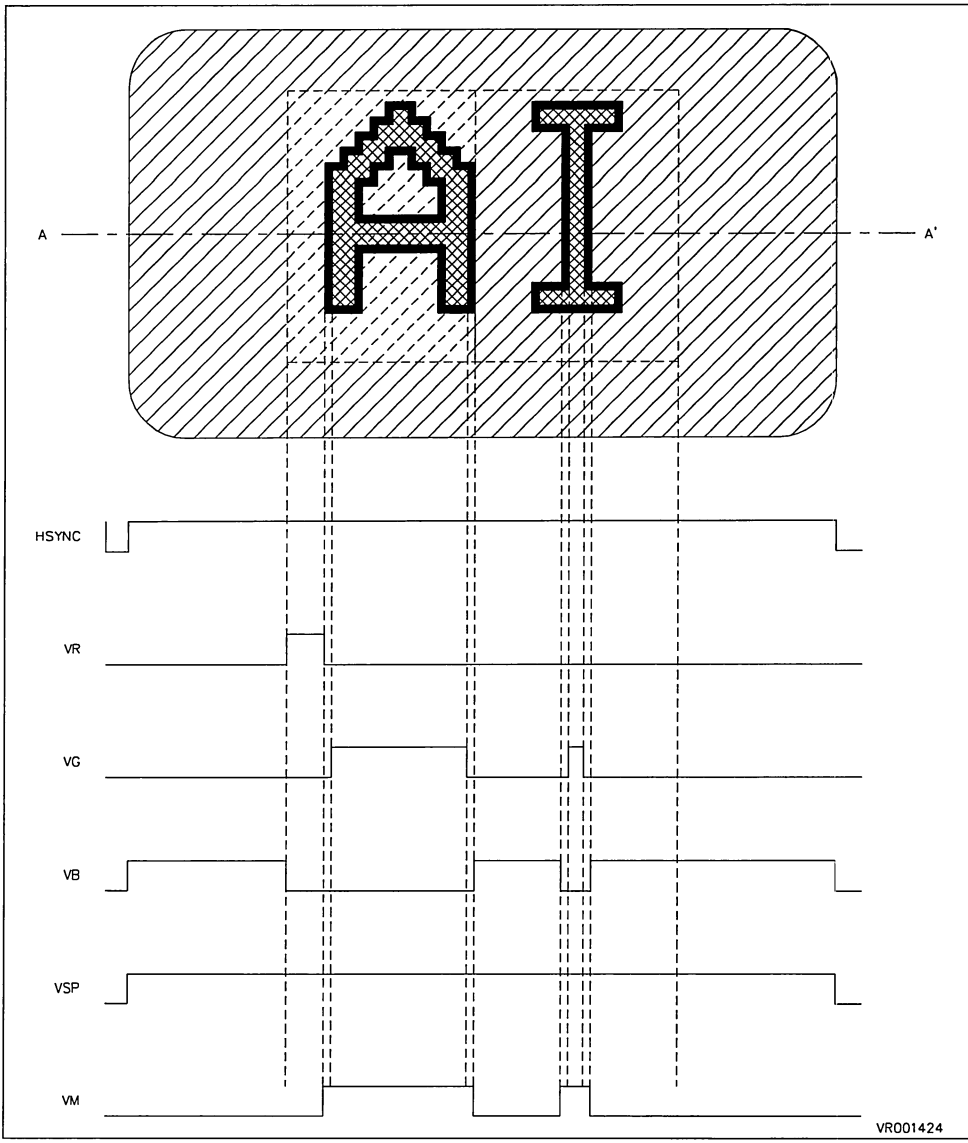
OSD WAVEFORM EXAMPLES

Note: for the following examples, the following polarities have been assumed:

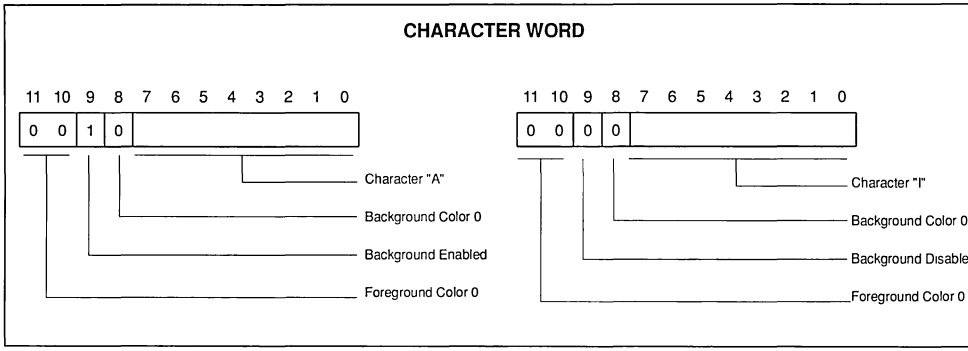
HSYNC,VSYNC . . . . . negative

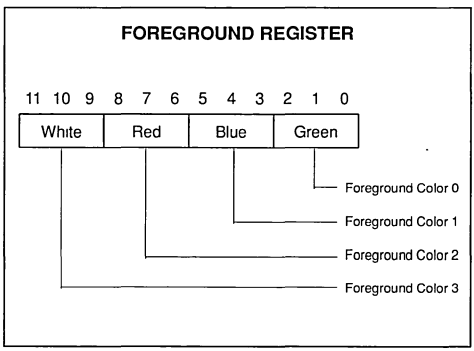
R,G,B,BLANK,MONITOR . . . . . positive

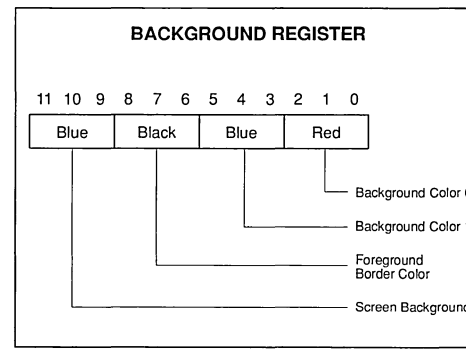
Figure 18.

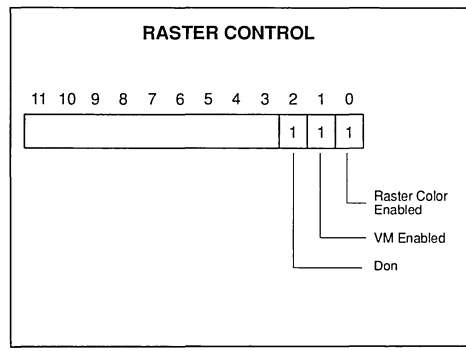


OSD WAVEFORMS EXAMPLES (Continued)



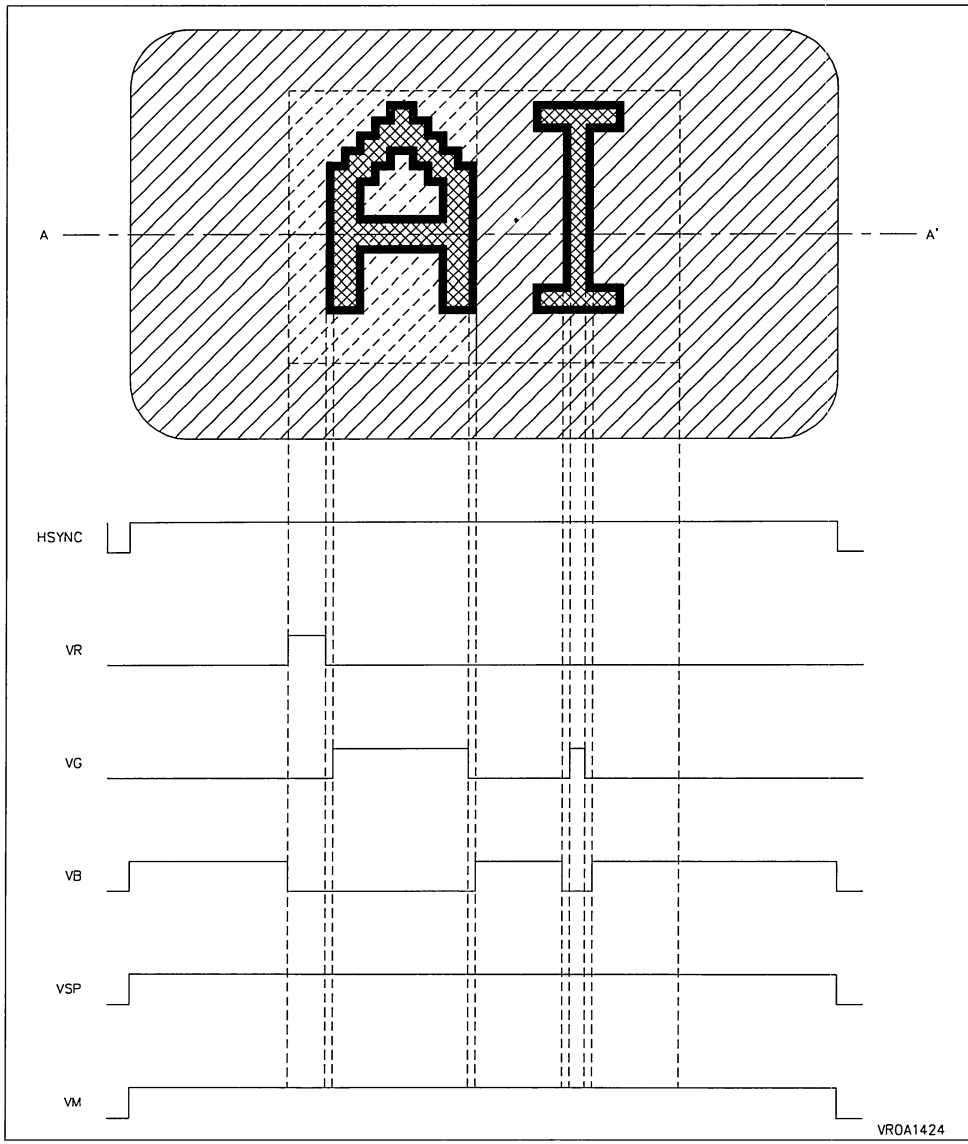






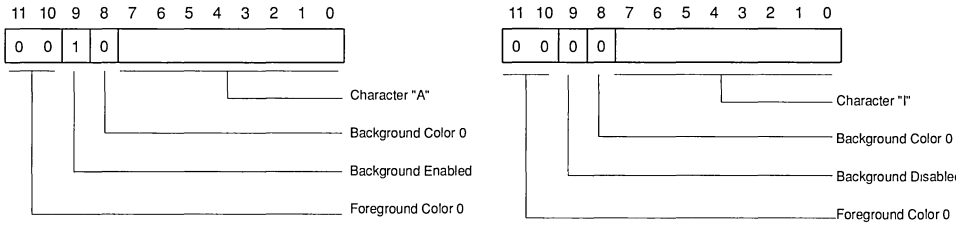
OSD WAVEFORM EXAMPLES (Continued)

Figure 19.

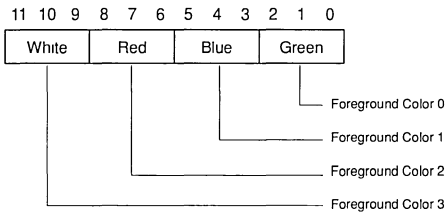


OSD WAVEFORMS EXAMPLES (Continued)

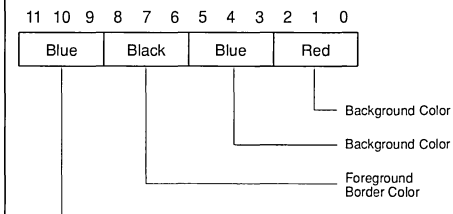
CHARACTER WORD



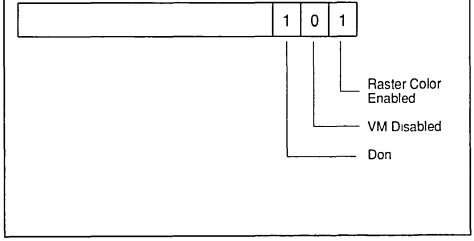
FOREGROUND REGISTER



BACKGROUND REGISTER

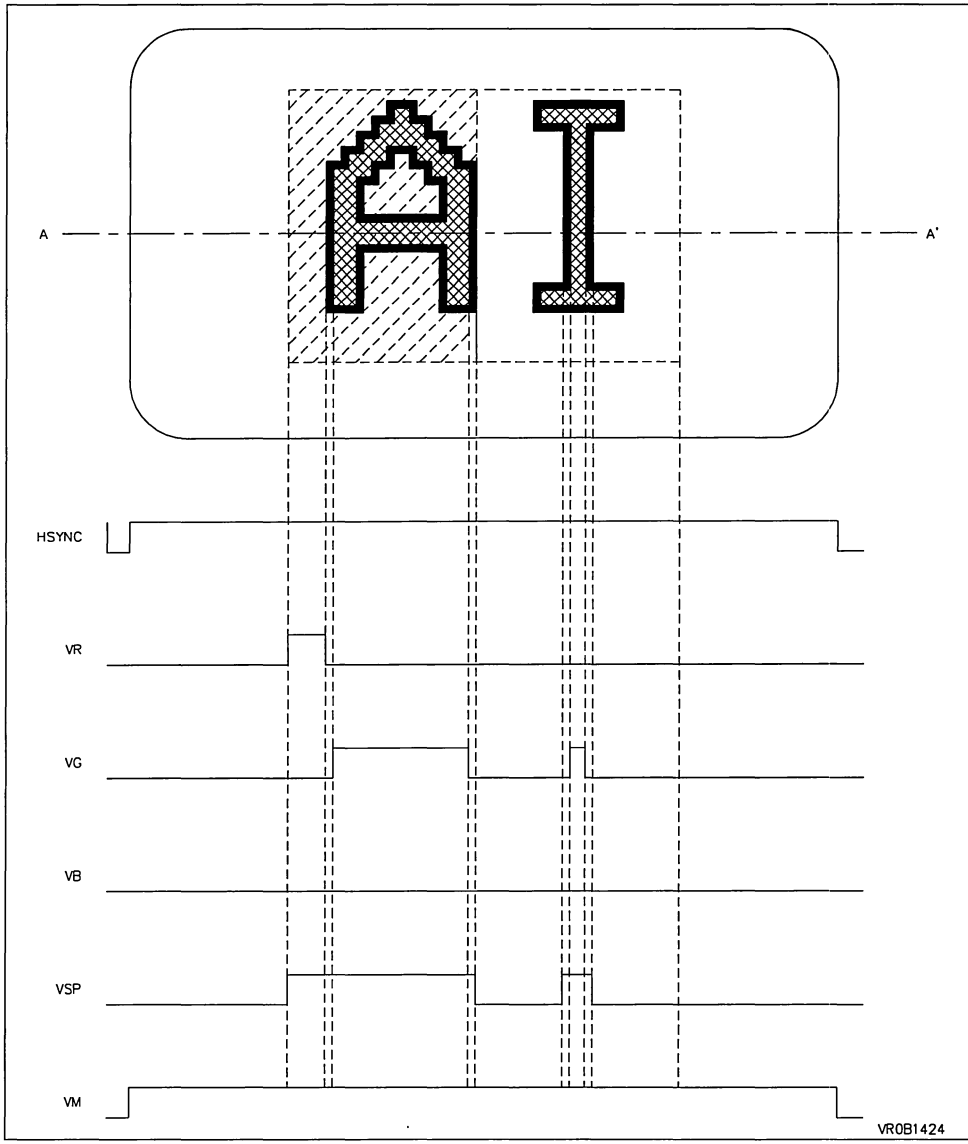


RASTER CONTROL

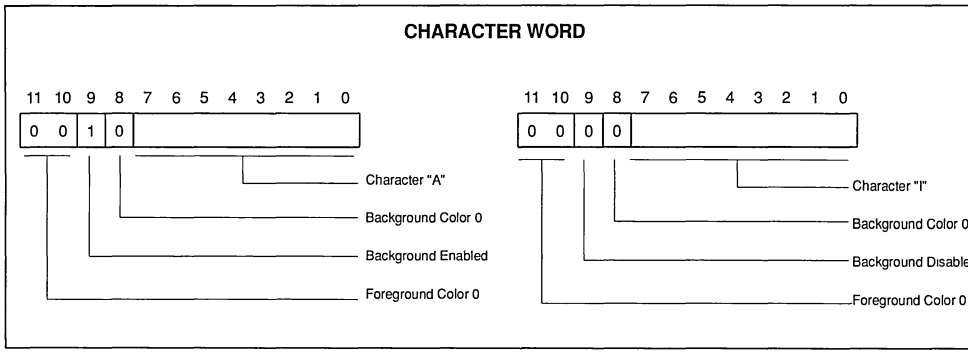


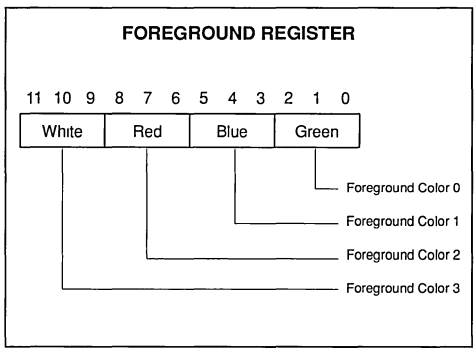
OSD WAVEFORM EXAMPLES (Continued)

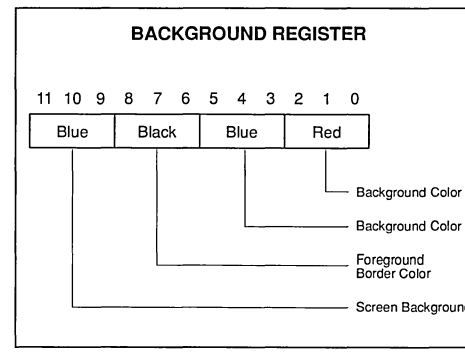
Figure 20.

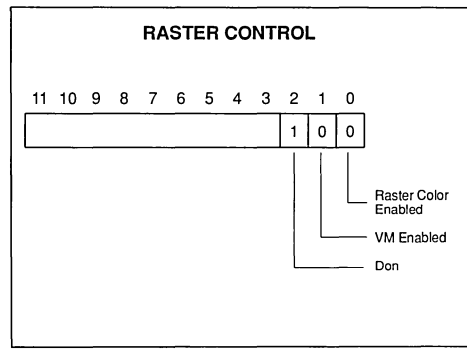


OSD WAVEFORMS EXAMPLES (Continued)









STANDARD CHARACTERS

The default device (sales type ST6398B1/B) is delivered with a standard set of ROM based characters and masked pin polarities; extra characters particular to the application are defined via the RAM characters.

The pin polarities have been fixed as follows:

HSYNC,VSYNC . . . . . negative (input low during retrace)

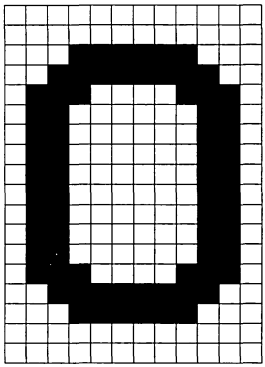
R,G,B,BLANK . . . . . positive

MONITOR . . . . . negative

Forty standard alphanumeric characters has been defined in character locations 00 to 27h; the remaining characters up to address 7Fh are not defined. Should these characters (together with the user definable and variable RAM characters) not be sufficient for the customer's application, then a customized set can be defined (see the section on customized characters). The standard set of ROM based characters is fixed as shown below.

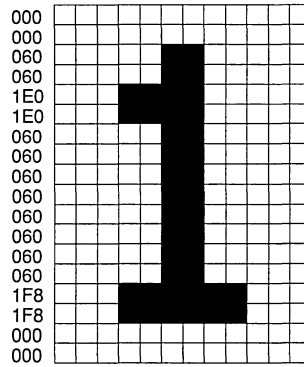
CHARACTER DEFINITION

000
000
1F8
3FC
70E
606
606
606
606
606
606
606
606
70E
3FC
1F8
000
000



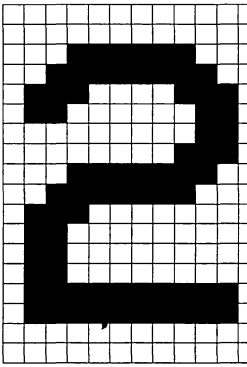
00

000
000
060
060
1E0
1E0
060
060
060
060
060
060
060
060
1F8
1F8
000
000



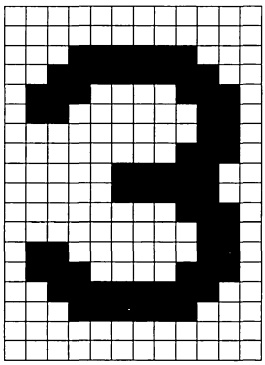
01

000
000
1F8
3FC
70E
606
006
00E
1FC
3F8
700
600
600
600
7FE
7FE
000
000



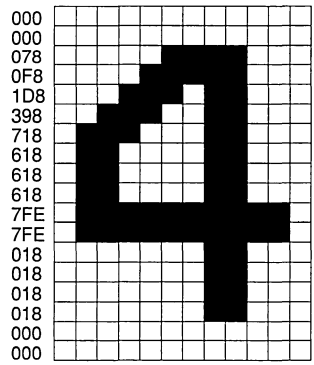
02

000
000
1F8
3FC
70E
606
006
00E
07C
07C
00E
006
606
70E
3FC
1F8
000
000



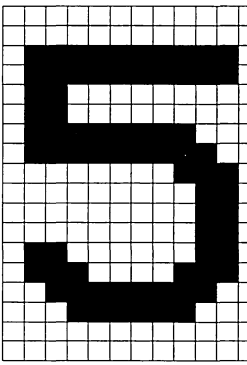
03

000
000
078
0F8
1D8
398
718
618
618
618
7FE
7FE
018
018
018
018
000
000



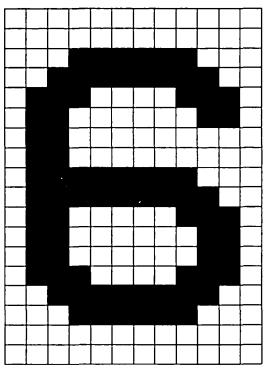
04

000
000
7FE
7FE
600
600
7F8
7FC
00E
006
006
006
606
70E
3FC
1F8
000
000



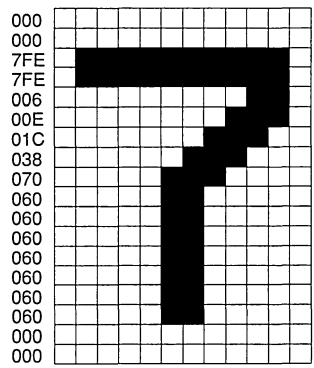
05

000
000
1F8
3FC
70C
606
600
600
7F8
7FC
60E
606
606
70E
3FC
1F8
000
000



06

000
000
7FE
7FE
006
00E
01C
038
070
060
060
060
060
060
060
000
000



07

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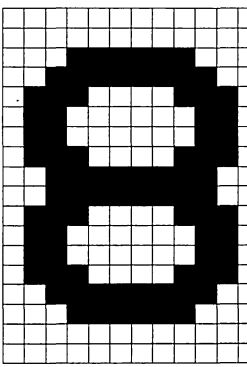
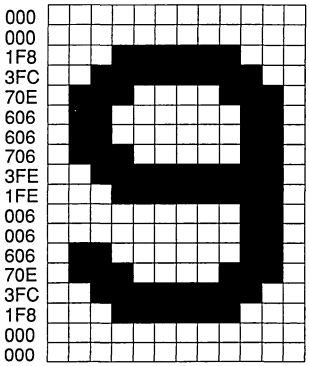
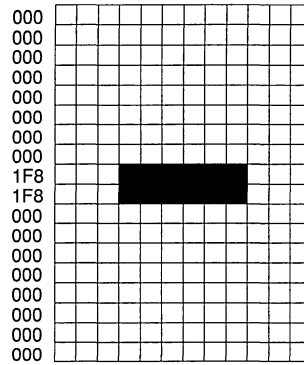


08

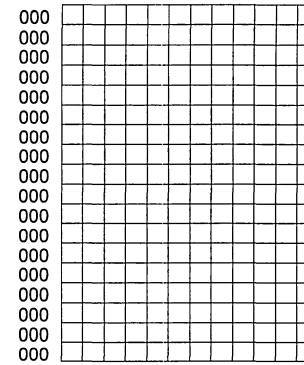
CHARACTER DEFINITION (Continued)



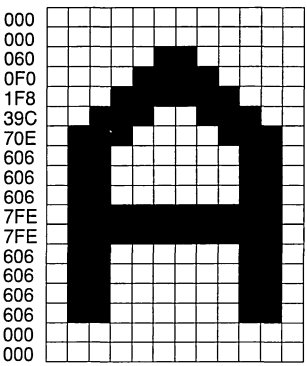
09



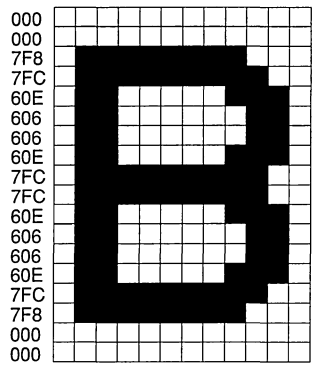
0A



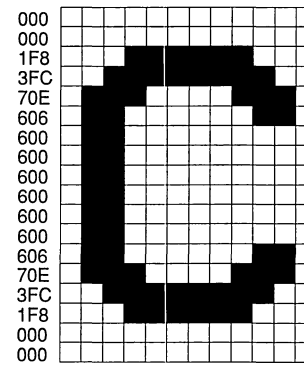
0B



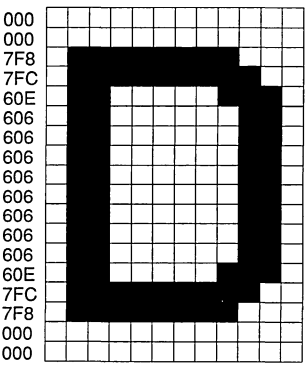
0C



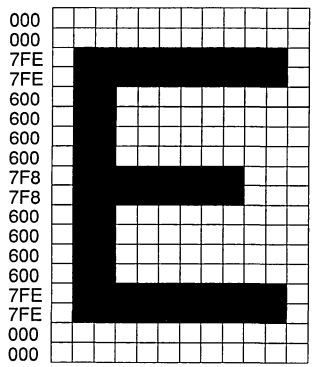
0D



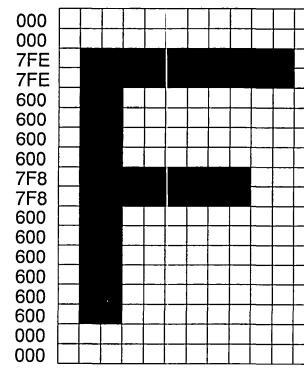
0E



0F

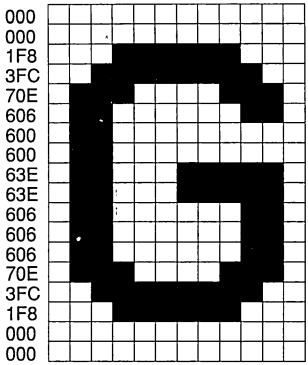


10

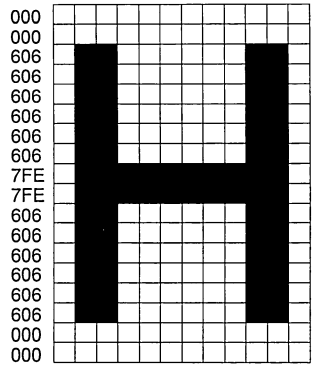


11

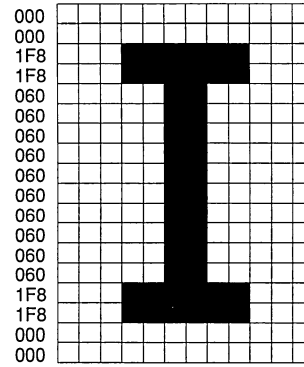
CHARACTER DEFINITION (Continued)



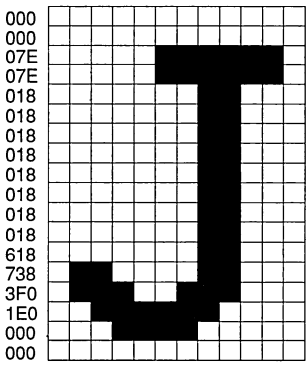
12



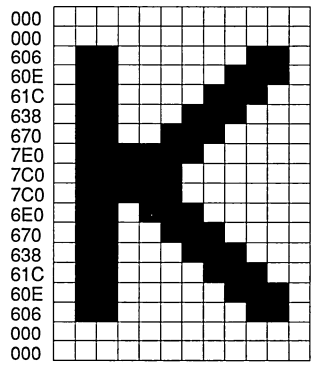
13



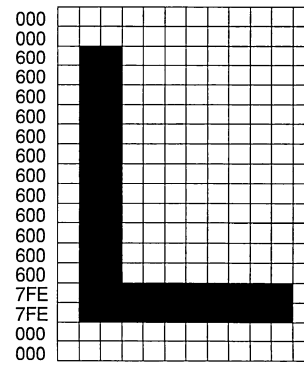
14



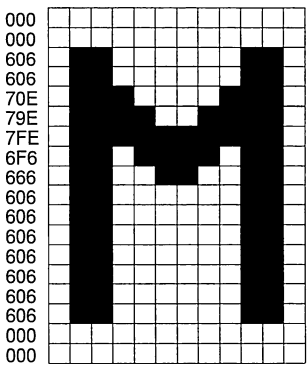
15



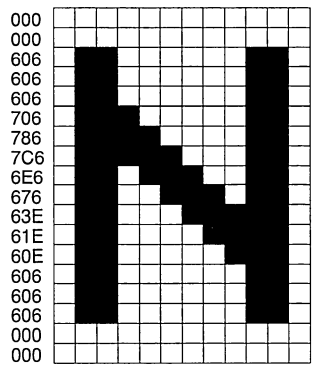
16



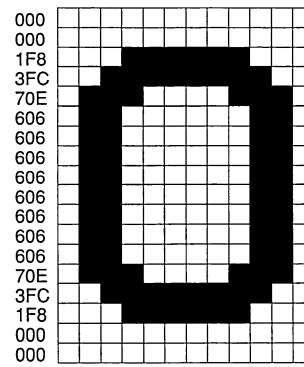
17



18

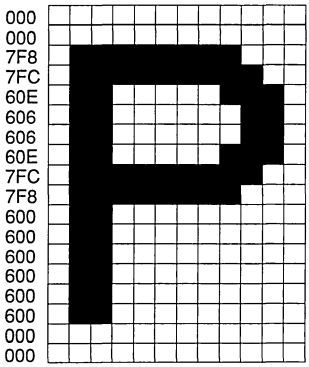


19

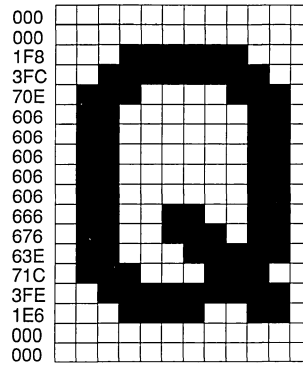


1A

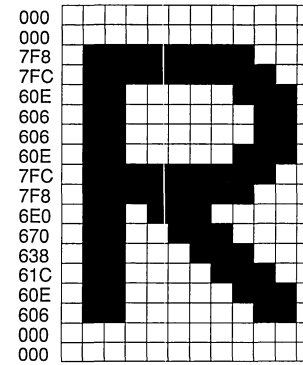
CHARACTER DEFINITION (Continued)



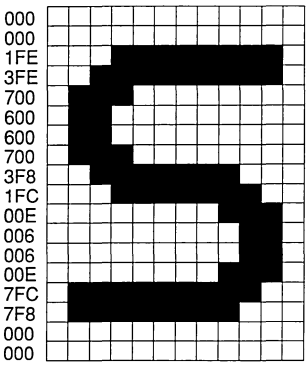
1B



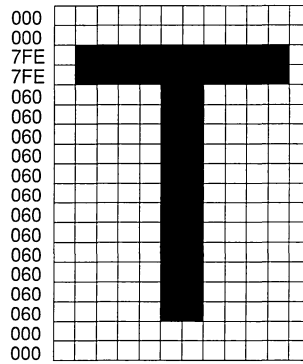
1C



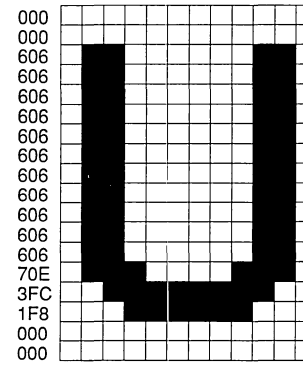
1D



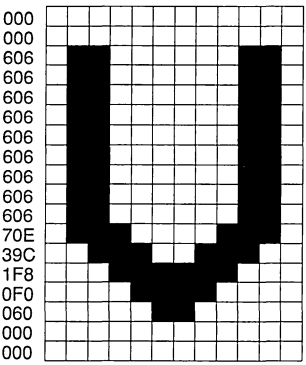
1E



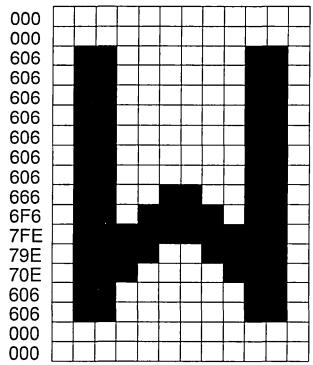
1F



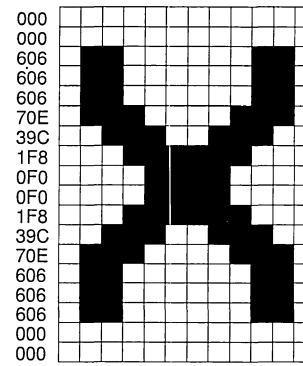
20



21

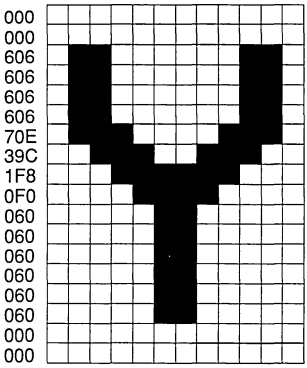


22

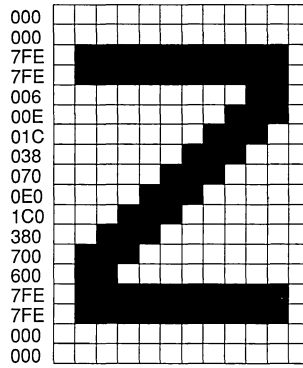


23

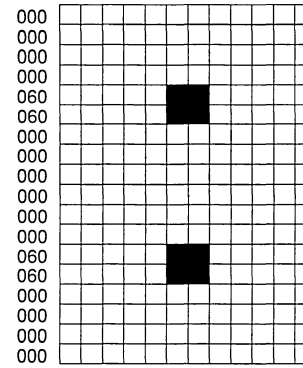
CHARACTER DEFINITION (Continued)



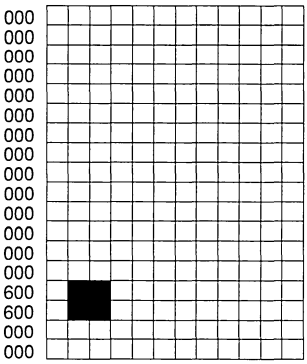
24



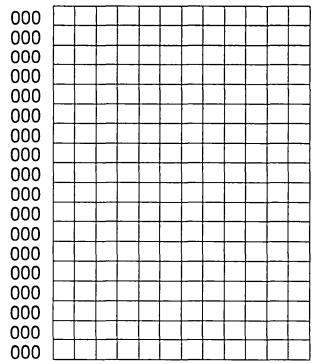
25

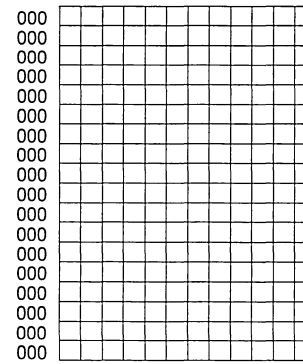


26



27





ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages. For proper operation it is recommended that V_I and V_O must be high than V_{SS} and smaller than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{DD}	Supply Voltage	-0.3	7	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
V_{OUT}	Output Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-60	150	°C
I_O	Current per pin	-5	+5	mA

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{DD} - V_{SS}	Supply Voltage	4.5	5.0	5.5	V
f_{OSC}	Oscillation Frequency	4.0	7.5	8.0	MHz
f_{CLK}	Clock Frequency	0		2	MHz
T_{OPT}	Operating Temperature	0		70	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Value			Unit
			Min.	Typ.	Max.	
Rth_{JA}	Thermal Resistance	DIP20			60	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, Tj, in Celsius can be obtained from:

$T_J = T_A + P_D \times Rth_{JA}$

Where: T_A = Ambient Temperature,
Rth_{JA} = Package thermal resistance (junction-to ambient),
P_D = Pint + Pport,
Pint = $I_{DD} \times V_{DD}$ (chip internal power),
Pport = Port power dissipation (determined by the user).

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70°C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Condition	Value		Unit
			Min.	Max.	
I_{DD}	Current Consumption			15	mA
V_{IH}	Input High Level		$0.75 \times V_{DD}$		V
V_{IL}	Input Low Level			$0.15 \times V_{DD}$	V
V_{OH}	Output High Level	I_{OH} = -1.0mA	V_{DD} - 0.5		V
V_{OL}	Output Low Level	I_{OL} = 1.0mA		0.5	V
I_{IL}	Input Low Leakage Current	V_{IL} = 0V	-10		µA
I_{IH}	Input High Leakage Current	$V_{IH} = V_{DD}$		10	µA

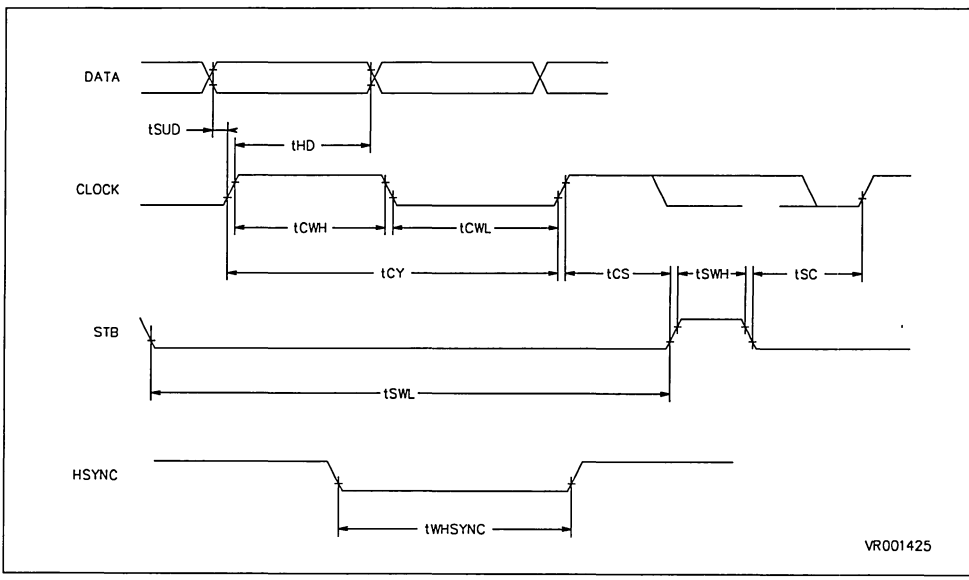
AC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70°C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Value		Unit
		Min.	Max.	
t_{CY}	Clock Cycle	500		ns
t_{CWH}	Clock High	200		ns
t_{CWL}	Clock Low	200		ns
t_{SUD}	Data Set Up	100		ns
t_{HD}	Data Hold	100		ns
t_{CS}	Clock to Strobe	200		ns
t_{SWH}	Strobe High	t_{WHSYNC}		t_{OSC}
t_{SWL}	Strobe Low (1)	t_{WHSYNC}		t_{OSC}
t_{SC}	Strobe to Clock	200		ns
t_{WHSYNC}	HSYNC Width	50		t_{OSC}

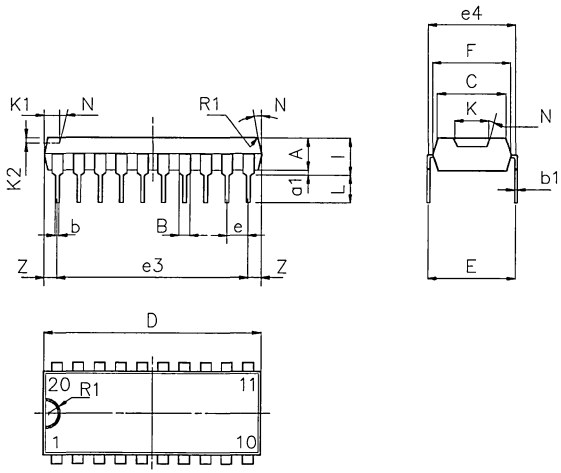
Note 1. For a 0 bit message.

Figure 21. AC Electrical Characteristics



PACKAGE MECHANICAL DATA

Figure 22. 20 Lead Plastic Dual In Line Package (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	–	–	–	–	–	–
a1	0.254			0.010		
B	1.39		1.65	0.054		0 064
b		0 45			0 017	
b1		0.25			0 009	
C	–	–	–	–	–	–
D			25.4			1.000
E		8 5			0.334	
e		2 54			0.100	
e3		22.86			0.900	
e4	–	–	–	–	–	–
F			7.1			0.279
I			3.93			0.154
L		3 3			0 129	
Z			1.34			0 052

CUSTOMED CHARACTERS AND ORDERING INFORMATION

Character Definition

If necessary Customized characters can be developed using the ST6398 CHARACTER DEVELOPMENT BOARD (emulator board). The board is inserted into a PC and is used to develop and simulate the OSD characters and functions. The graphics system is built around the alphanumeric and graphics contoller TS68483 which contains a separate dedicated display memory.

For ST6398 CHARACTER DEVELOPMENT BOARD (emulator board) ordering information contact your SGS-THOMSON sales representative.

Code Procedure

Upon completion of character development, the file created by the SAVE command should be given to SGS-THOMSON (on a MS-DOS 5" diskette) together with the option list.

When SGS-THOMSON receives the file, a character listing is generated and returned to the customer together with a copy of the option list for approval. The signed list constitutes a part of the contractual agreement for the creation of the customer mask. A mask charge together with a minimum quantity of parts will be charged to the customer. The SGS-THOMSON sales organization will provide detailed information on contractual points.

ORDERING INFORMATION

Type	Description	Frequency	Range	Package
ST6398B1	On Screen Display	2MHz	0 to +70°C	DIP20

ST6398 MICROCONTROLLER OPTION LIST

Customer : . . . . . .

Address: . . . . . .

Contact: . . . . . .

Phone No: . . . . . .

Reference: . . . . . .

Package [ ] (p) Temperature Range [ ] (t)

For marking one line with 10 characters maximum is possible

Special Marking [ ] (y/n) Line1 " _ _ _ _ _ _ _ _ _ _ " (N)

Notes:

(p) B= Dual in Line Plastic

(t) 1= 0 to 70°C

(N) Letters, digits, ' . ', ' - ', ' / ' and spaces only

Marking: the default marking is equivalent to the sales type only (part number).

OSD POLARITY OPTIONS (Put a cross on selected item) :

		POSITIVE	NEGATIVE
VSYNC		[ ]	[ ]
HSYNC		[ ]	[ ]
R	(VR)	[ ]	[ ]
G	(VG)	[ ]	[ ]
B	(VB)	[ ]	[ ]
BLANK	(VSP)	[ ]	[ ]
MONITOR	(VM)	[ ]	[ ]

Signature .....

Date .....

Note: A negative SYNC means the input is low during retrace.

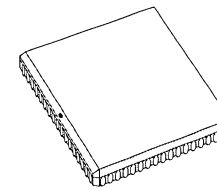
SGS-THOMSON MICROELECTRONICS

ST90R40

ROMLESS HCMOS MCU WITH EEPROM, RAM AND A/D

ADVANCE DATA

- Single chip microcontroller with 256 bytes of RAM and 256 bytes of Register File with 224 general purpose registers available as RAM, accumulators or index pointers.
- Romless to allow maximum external memory flexibility in development and production phases.
- 512 bytes of high-reliability EEPROM on-chip, with 300,000 erase/write cycle capability and 10 year data retention.
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-BUS, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Two 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Full function Serial Communications Interface with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to six 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Compatible with ST9040, 16k ROM devices (also available in windowed and One Time Programmable EPROM packages).
- 68-lead Plastic Leaded Chip Carrier package for ST90R40.



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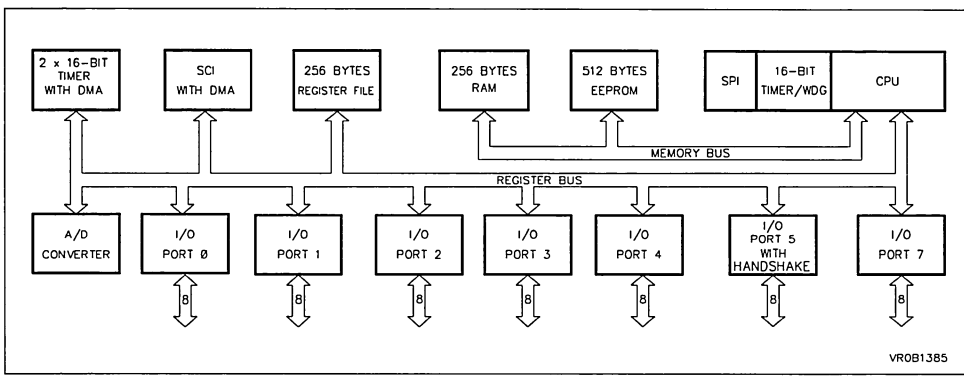
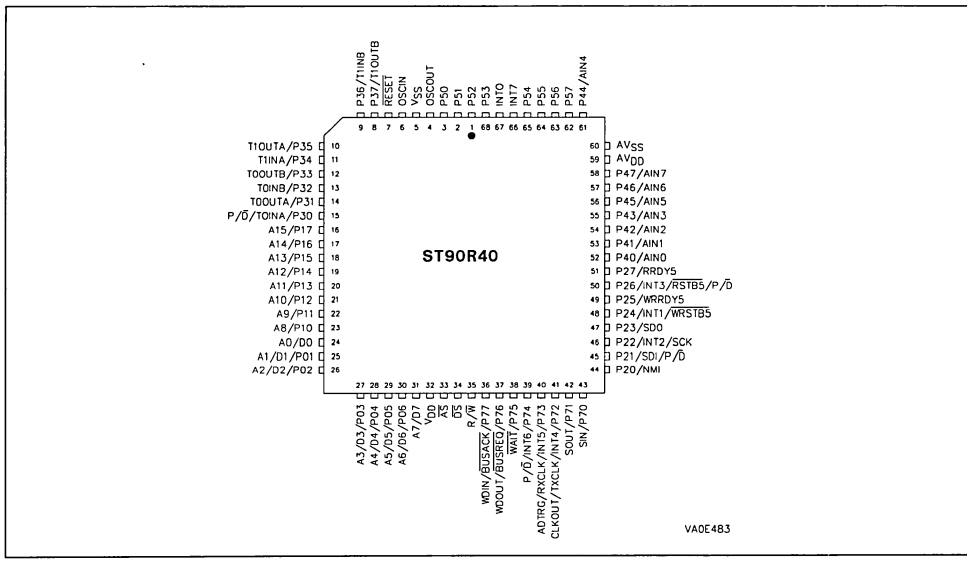
(Ordering Information at the end of the datasheet)

Figure 1. ST90R40 Block Diagram



This is advance information on a new product now in development or undergoing evaluation Details are subject to change without notice

Figure 2. ST90R40 Pin Configuration



GENERAL DESCRIPTION

The ST90R40 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems.

The ST90R40 is fully compatible with the ST9040 ROM version and this datasheet will thus provide only information specific to the ROMLESS device.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9040 ROM-BASED DEVICE, OR ST90R50 FOR FURTHER DETAILS.

The ROMLESS ST90R40 can be configured as a microcontroller able to manage up to 128K bytes of external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

A key point of the ST90R40 architecture is related to its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90R40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R40 with up to 48 I/O lines dedicated to digital Input/Output. These lines are grouped into up to six 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing and status signals, address lines, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

GENERAL DESCRIPTION (Continued)

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90R40 accesses on-chip Data memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for memory transactions. R/$\overline{W}$ is low when writing to program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

AD0-AD7, (P0.0-P0.7) *Address/Data Lines (Input/Output, TTL or CMOS compatible).* 8 lines providing a multiplexed address and data bus, under control of the $\overline{AS}$ and $\overline{DS}$ timing signals.

P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 48 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90R40 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Figure 1.2 shows the Functions allocated to each I/O Port pins.

PIN DESCRIPTION (Continued)

Table 1. ST90R40 I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31
P1.0	A8	O	Address bit 8	23
P1.1	A9	O	Address bit 9	22
P1.2	A10	O	Address bit 10	21
P1.3	A11	O	Address bit 11	20
P1.4	A12	O	Address bit 12	19
P1.5	A13	O	Address bit 13	18
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	16
P2.0	NMI	I	Non-Maskable Interrupt	44
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45
P2.1	SDI	I	SPI Serial Data Out	45
P2.2	INT2	I	External Interrupt 2	46
P2.2	SCK	O	SPI Serial Clock	46
P2.3	SDO	O	SPI Serial Data In	47
P2.4	INT1	I	External Interrupt 1	48
P2.4	$\overline{\text{WRSTB5}}$	O	Handshake Write Strobe P5	48
P2 5	WRRDY5	I	Handshake Write Ready P5	49
P2.6	INT3	I	External Interrupt 3	50
P2.6	$\overline{\text{RDSTB5}}$	I	Handshake Read Strobe P5	50
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50
P2.7	RDRDY5	O	Handshake Read Ready P5	51

PIN DESCRIPTION (Continued)

Table 1. ST90R40 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P3.0	T0INA	I	MF Timer 0 Input A	15
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15
P3.1	T0OUTA	O	MF Timer 0 Output A	14
P3 2	T0INB	I	MF Timer 0 Input B	13
P3.3	T0OUTB	O	MF Timer 0 Output B	12
P3.4	T1INA	I	MF Timer 1 Input A	11
P3.5	T1OUTA	O	MF Timer 1 Output A	10
P3.6	T1INB	I	MF Timer 1 Input B	9
P3.7	T1OUTB	O	MF Timer 1 Output B	8
P4.0	AIN0	I	A/D Analog Input 0	52
P4.1	AIN1	I	A/D Analog Input 1	53
P4.2	AIN2	I	A/D Analog Input 2	54
P4.3	AIN3	I	A/D Analog Input 3	55
P4.4	AIN4	I	A/D Analog Input 4	61
P4.5	AIN5	I	A/D Analog Input 5	56
P4.6	AIN6	I	A/D Analog Input 6	57
P4.7	AIN7	I	A/D Analog Input 7	58
P5.0		I/O	I/O Handshake Port 5	3
P5.1		I/O	I/O Handshake Port 5	2
P5.2		I/O	I/O Handshake Port 5	1
P5.3		I/O	I/O Handshake Port 5	68
P5.4		I/O	I/O Handshake Port 5	65
P5.5		I/O	I/O Handshake Port 5	64
P5.6		I/O	I/O Handshake Port 5	63
P5.7		I/O	I/O Handshake Port 5	62
P7.0	SIN	I	SCI Serial Input	43
P7.1	SOUT	O	SCI Serial Output	42
P7.2	INT4	I	External Interrupt 4	41
P7.2	TXCLK	I	SCI Transmit Clock Input	41

PIN DESCRIPTION (Continued)

Table 1. ST90R40 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41
P7.3	INT5	I	External Interrupt 5	40
P7.3	RXCLK	I	SCI Receive Clock Input	40
P7.3	ADTRG	I	A/D Conversion Trigger	40
P7.4	INT6	I	External Interrupt 6	39
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39
P7.5	$\overline{WAIT}$	I	External Wait Input	38
P7.6	WDOUT	O	T/WD Output	37
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37
P7.7	WDIN	I	T/WD Input	36
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36

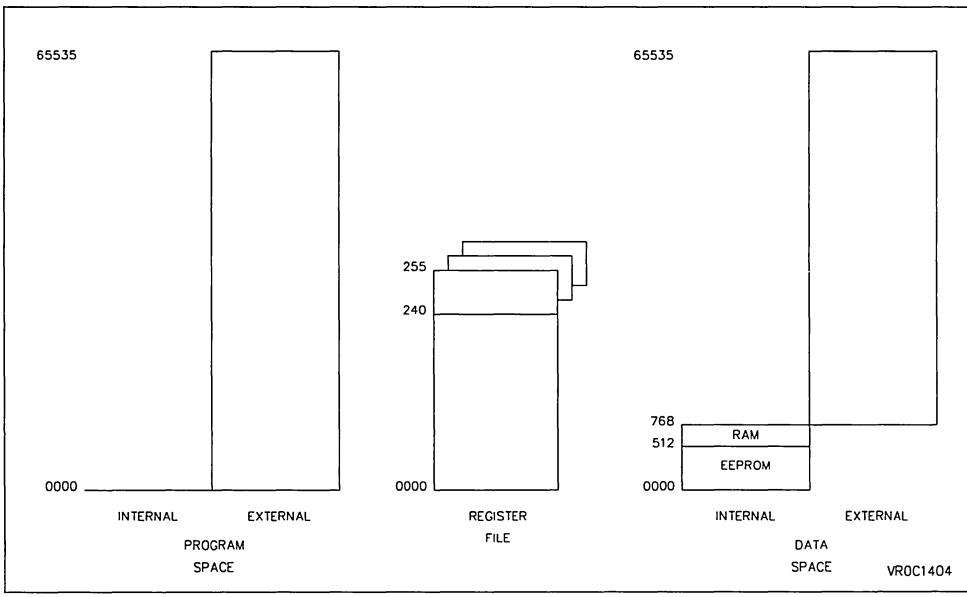
MEMORY

The memory of the ST90R40 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90R40 addresses all program memory in the external PROGRAM space. The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of on-chip RAM memory at memory addresses 200h through 2FFh.

The External Memory spaces are addressed using the multiplexed address and data buses on Ports 0 and 1. Additional Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may be used as RAM memory.

MEMORY (Continued)

Figure 3. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \leq AV_{SS} < AV_{DD} \leq V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied Exposure to maximum rating conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

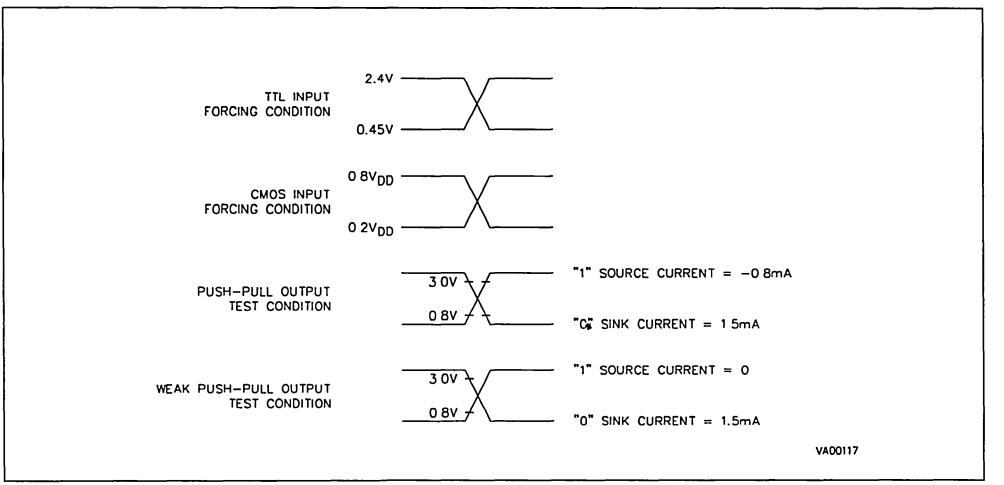
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0 7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, 0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	0V < V_{IN} < V_{DD}	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, 0V < V_{IN} < V_{DD}	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	0V < V_{IN} < 0.8V	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution)

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

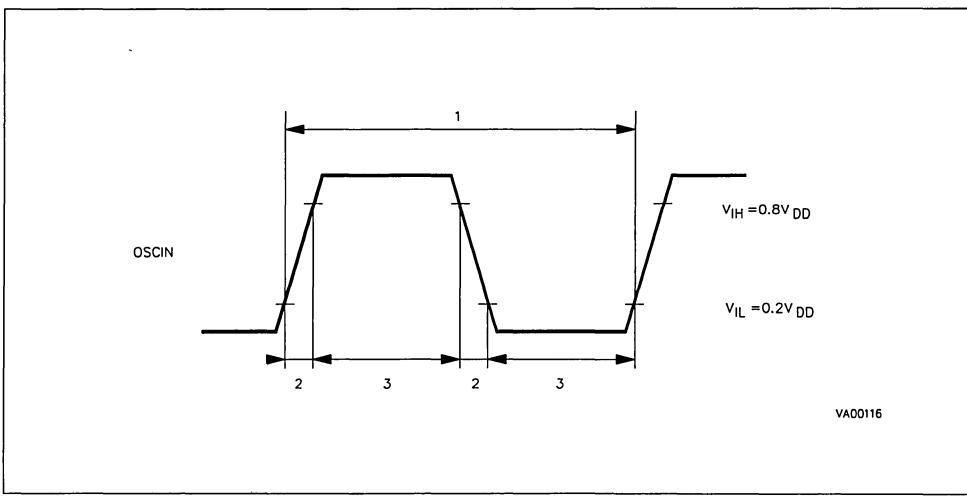
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Notes:
1. Clock divided by 2 internally (MODER.DIV2=1)
2 Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status

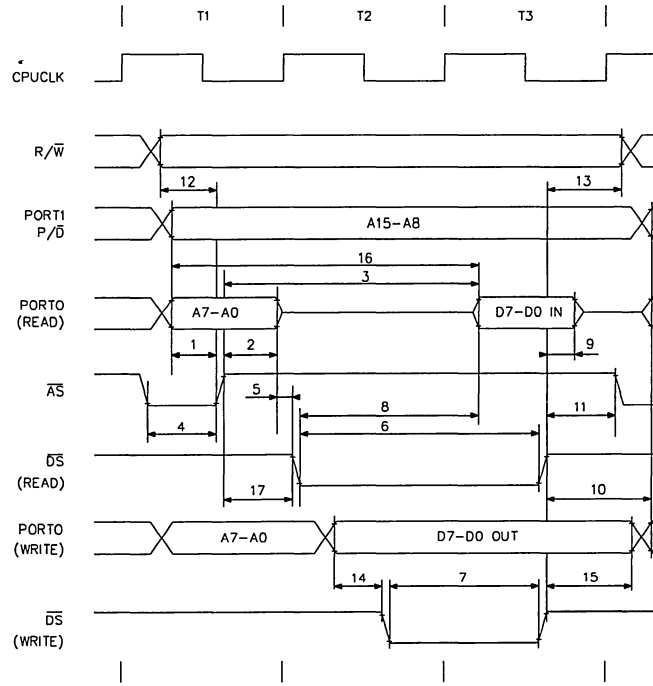
Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

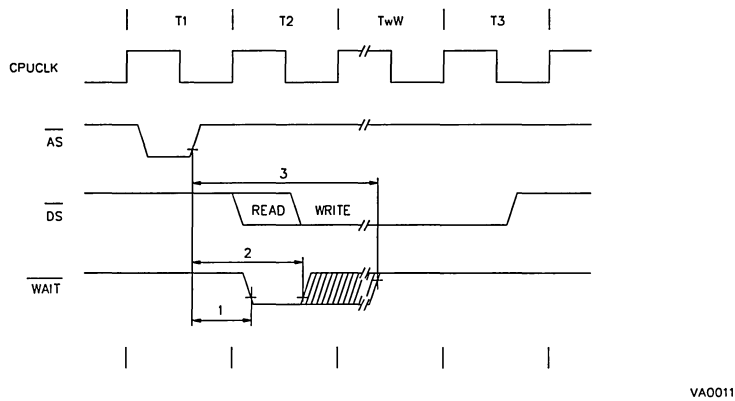
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC – 29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING

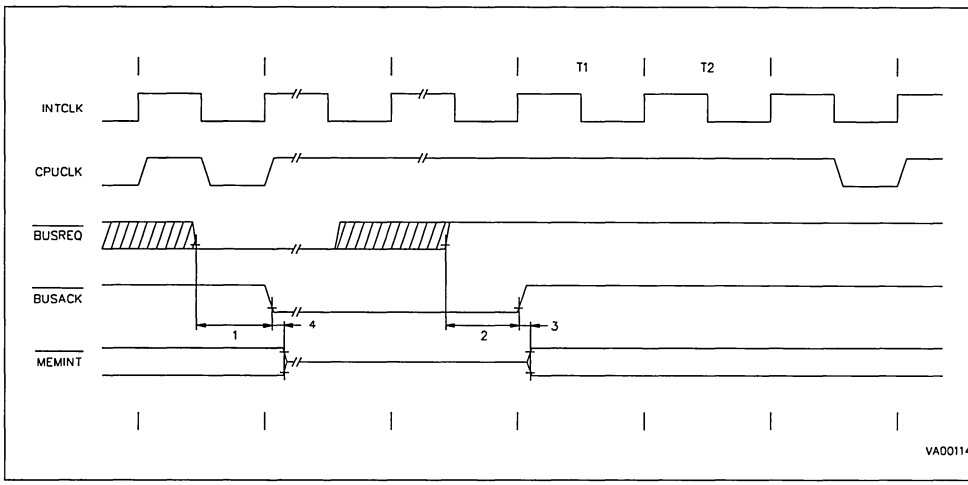


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

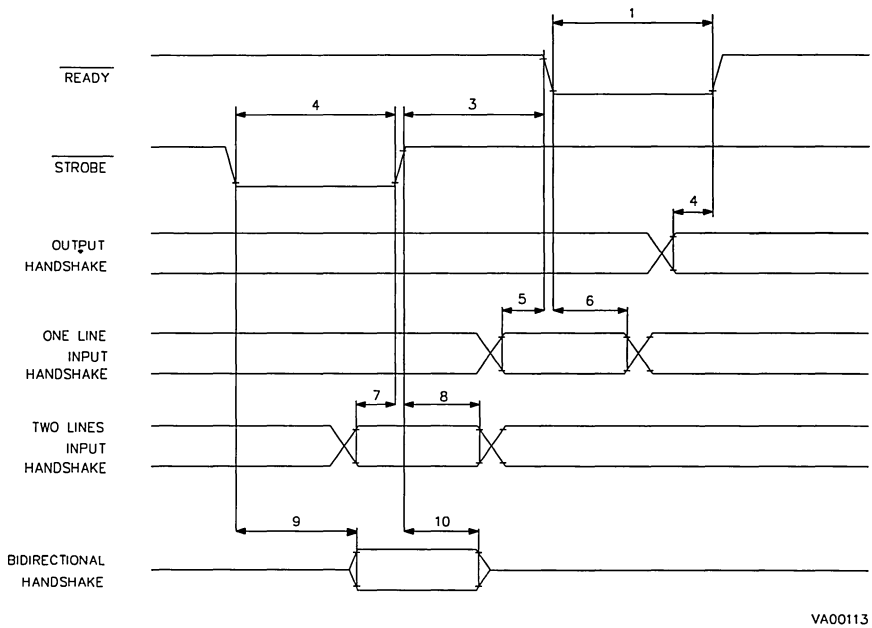
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		Tp (P+W+1) – 18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

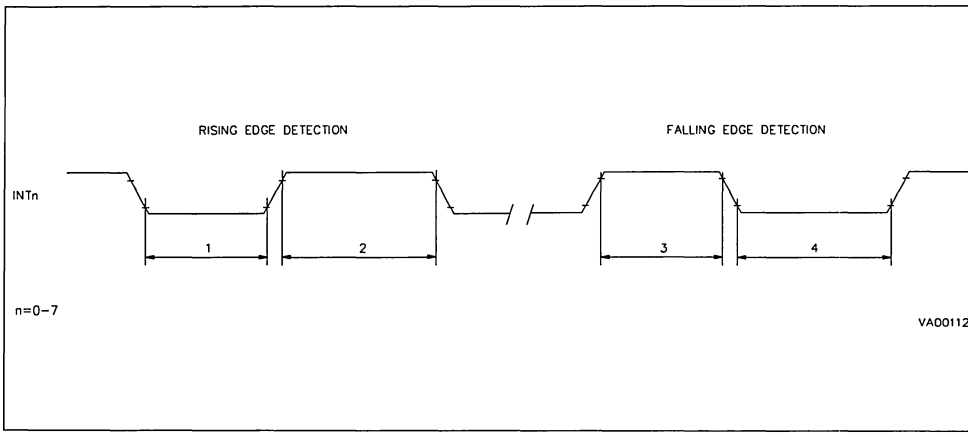


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

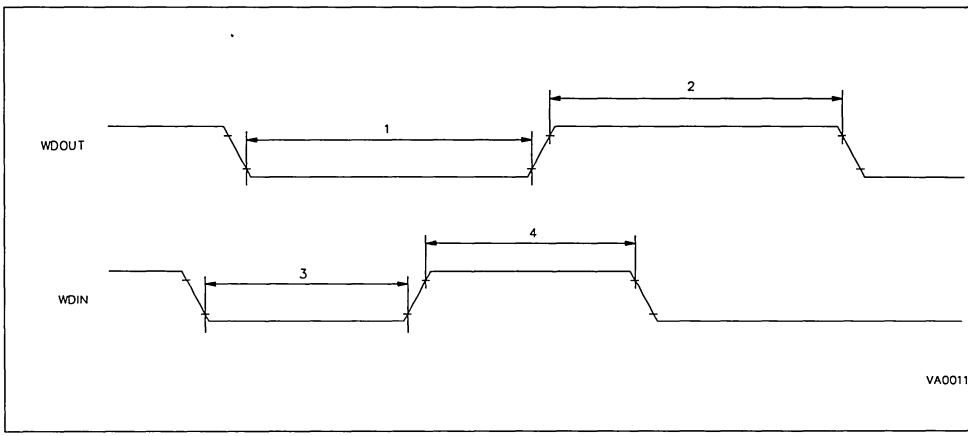
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

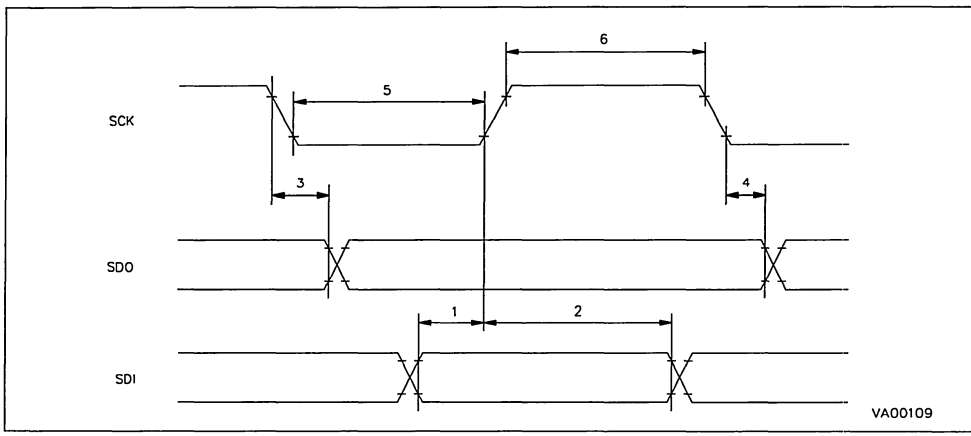


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

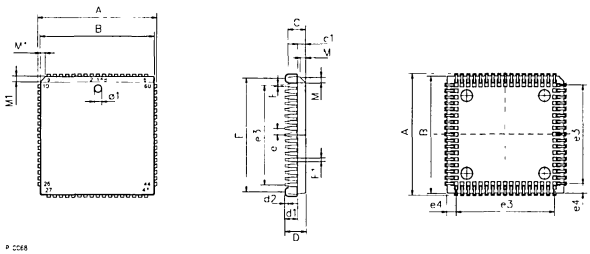
Note: 1. TpC is the Clock period.

SPI TIMING



PACKAGE MECHANICAL DATA

Figure 57. 68-Lead Plastic Leaded Chip Carrier



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	25.02		25.27	0.985		0.995
B	24 13		24.33	0 950		0.958
D	4.20		5.08	0.165		0 200
d1		2.54			0.100	
d2		0.56			0 022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0 10			0 004
M		1.27			0.050	
M1		1.14			0.044	
Ø1		7.36			0.289	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90R40C6	24MHz	-40°C to +85°C	PLCC68
ST90R40C1	24MHz	0°C to +70°C	PLCC68

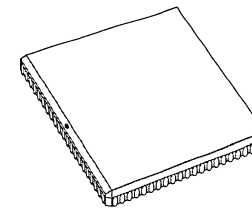
SGS-THOMSON MICROELECTRONICS

ST90R50

ROMLESS HCMOS MCU WITH BANKSWITCH AND A/D CONVERTER

ADVANCE DATA

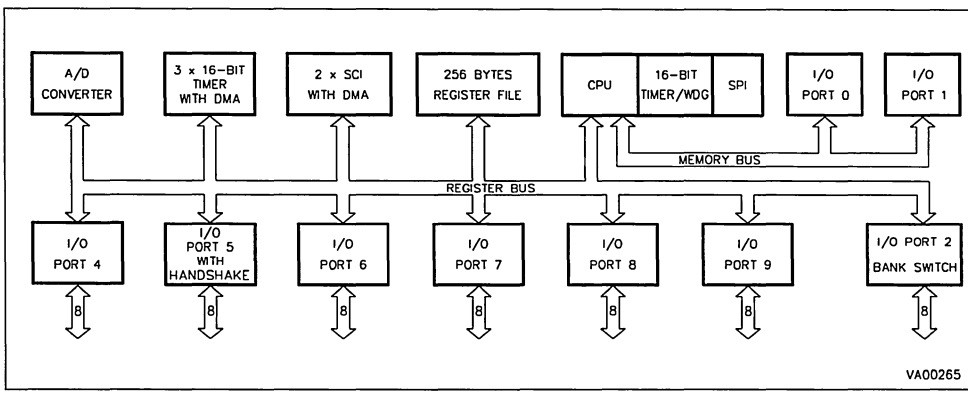
- Single chip microcontroller with 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- Romless to allow maximum external memory flexibility in development and production phases.
- BankSwitch logic allowing a maximum addressing capability of 8M bytes for program and data spaces (16M byte total).
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I^2C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Three 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Two full function Serial Communications Interfaces with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to nine 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Compatible with ST9054, 32k ROM devices (also available in windowed and One Time Programmable EPROM packages).



PLCC84

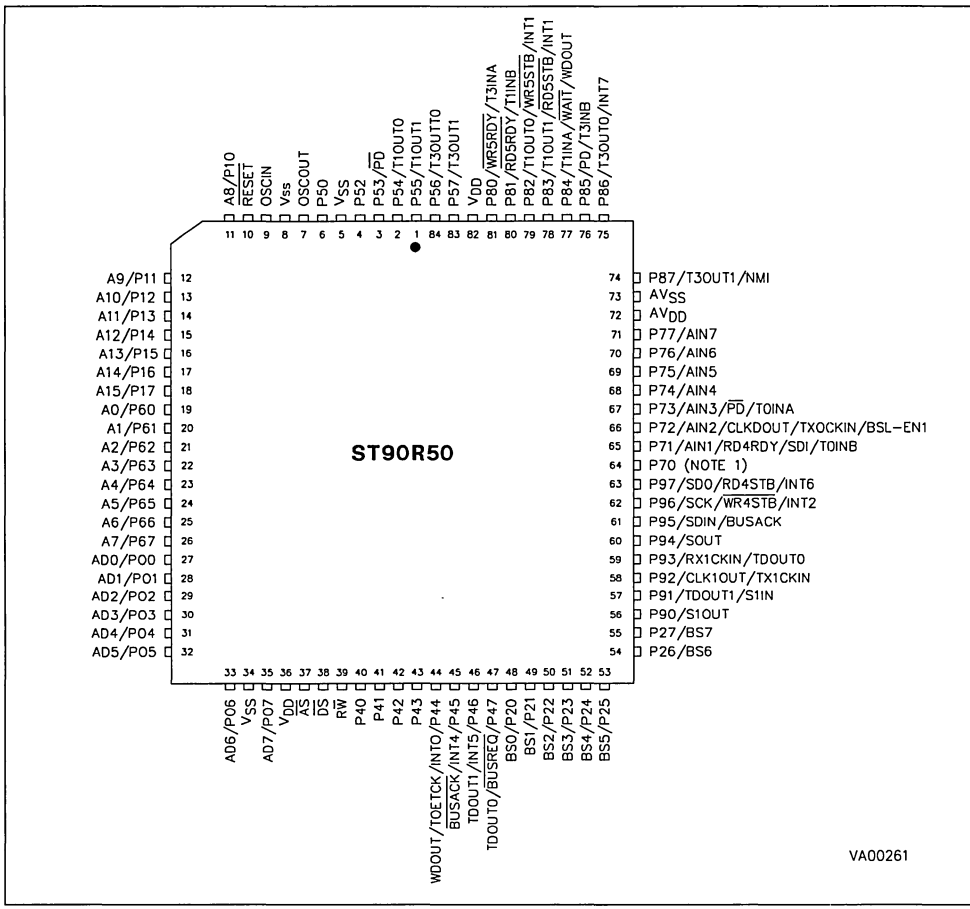
(Ordering Information at the end of the datasheet)

Figure 1. ST90R50 Block Diagram



This is advanced information on a new product now in development or undergoing evalution. Details are subject to change without notice.

Figure 2. ST90R50 Pin Configuration



Note 1 : P70/AIN0/ADTRG/WR4DRDY/RX0CKIN/WDIN/BSH_EN1.

GENERAL DESCRIPTION

The ST90R50 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems with its 16M byte addressing space when using the Bankswitch memory expansion.

A key point of the ST90R50 architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90R50 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

GENERAL DESCRIPTION (Continued)

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R50 with up to 72 I/O lines dedicated to digital Input/Output. These lines are grouped into up to nine 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, address and data buses for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device are two full duplex Serial Communications Interfaces, each with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0, Port 1, Port 6, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90R50 accesses on-chip RAM memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, Port 6, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. The timing of R/$\overline{W}$ may be modified when using the Bank Switch Logic memory expansion to prevent external timing conflicts. R/$\overline{W}$ can be placed in a high impedance state along with Port 0, Port 1, Port 6, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P6.0-P6.7 *(Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits providing the external memory interface to address the external program memory.

P2.0-P2.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7, P8.0-P8.7, P9.0-P9.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90R50 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1 shows the Functions allocated to each I/O Port pins

PIN DESCRIPTION (Continued)

Table 1. ST90R50 I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P0.0	A0/D0	I/O	Address/Data bit 0 mux	27
P0.1	A1/D1	I/O	Address/Data bit 1 mux	28
P0.2	A2/D2	I/O	Address/Data bit 2 mux	29
P0.3	A3/D3	I/O	Address/Data bit 3 mux	30
P0.4	A4/D4	I/O	Address/Data bit 4 mux	31
P0.5	A5/D5	I/O	Address/Data bit 5 mux	32
P0.6	A6/D6	I/O	Address/Data bit 6 mux	33
P0.7	A7/D7	I/O	Address/Data bit 7 mux	35
P1.0	A8	O	Address bit 8	11
P1.1	A9	O	Address bit 9	12
P1.2	A10	O	Address bit 10	13
P1.3	A11	O	Address bit 11	14
P1.4	A12	O	Address bit 12	15
P1.5	A13	O	Address bit 13	16
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	18
P2.0	BS0	O	Bank Switch Address 0 (A16)	48
P2.1	BS1	O	Bank Switch Address 1 (A17)	49
P2.2	BS2	O	Bank Switch Address 2 (A18)	50
P2.3	BS3	O	Bank Switch Address 3 (A19)	51
P2.4	BS4	O	Bank Switch Address 4 (A20)	52
P2.5	BS5	O	Bank Switch Address 5 (A21)	53
P2.6	BS6	O	Bank Switch Address 6 (A22)	54
P2.7	BS7	O	Bank Switch Address 7 (A23)	55
P4.0		I/O	I/O Handshake Port 4	40
P4.1		I/O	I/O Handshake Port 4	41
P4.2		I/O	I/O Handshake Port 4	42
P4.3		I/O	I/O Handshake Port 4	43
P4.4	INT0	I	External interrupt 0	44
P4.4	WDOUT	O	T/WD output	44
P4.4		I/O	I/O Handshake Port 4	44
P4.5	INT4	I	External interrupt 4	45
P4.5	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	45
P4.5		I/O	I/O Handshake Port 4	45

PIN DESCRIPTION (Continued)

Table 1. ST90R50 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P4.6	INT5	I	External interrupt 5	46
P4.6	T0OUTB	O	MF Timer 0 output B	46
P4.6		I/O	I/O Handshake Port 4	46
P4.7	T0OUTA	O	MF Timer 0 output A	47
P4.7	$\overline{\text{BUSREQ}}$	I	External Bus Request	47
P4.7		I/O	I/O Handshake Port 4	47
P5.0		I/O	I/O Handshake Port 5	6
P5.1		I/O	I/O Handshake Port 5	5
P5.2		I/O	I/O Handshake Port 5	4
P5.3		I/O	I/O Handshake Port 5	3
P5.3	P/$\overline{\text{D}}$	O	Program/Data space select	3
P5.4	T1OUTA	O	MF Timer 1 output A	2
P5.4		I/O	I/O Handshake Port 5	2
P5.5	T1OUTB	O	MF Timer 1 output B	1
P5.5		I/O	I/O Handshake Port 5	1
P5.6	T3OUTA	O	MF Timer 3 output A	84
P5.6		I/O	I/O Handshake Port 5	84
P5.7	T3OUTB	O	MF Timer 3 output B	83
P5.7		I/O	I/O Handshake Port 5	83
P6.0	A0	O	Address bit 0 (non mux)	19
P6.1	A1	O	Address bit 1 (non mux)	20
P6.2	A2	O	Address bit 2 (non mux)	21
P6.3	A3	O	Address bit 3 (non mux)	22
P6.4	A4	O	Address bit 4 (non mux)	23
P6.5	A5	O	Address bit 5 (non mux)	24
P6.6	A6	O	Address bit 6 (non mux)	25
P6.7	A7	O	Address bit 7 (non mux)	26
P7.0	AIN0	I	A/D Analog input 0	64
P7.0	ADTRG	I	A/D conversion trigger	64
P7.0	WRRDY4	I	Handshake Write Ready P4	64
P7.0	RX0CKIN	I	SCI0 Receive Clock input	64
P7.0	WDIN	I	T/WD input	64
P7.0	BSH_EN1	I	Bank Switch High Nibble Enable	64
P7.1	AIN1	I	A/D Analog input 1	65

PIN DESCRIPTION (Continued)

Table 1. ST90R50 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P7.1	RDRDY4	O	Handshake Read Ready P4	65
P7.1	SDI	I	SPI Serial Data In	65
P7.1	T0INB	I	MF Timer 0 input B	65
P7.2	AIN2	I	A/D Analog input 2	66
P7.2	CLK0OUT	O	SCI0 Byte Sync Clock output	66
P7.2	TX0CKIN	I	SCI0 Transmit Clock input	66
P7.2	BSL_EN1	I	Bank Switch Low Nibble Enable	66
P7.3	AIN3	I	A/D Analog input 3	67
P7.3	P/$\overline{D}$	O	Program/data space select	67
P7.3	T0INA	I	MF Timer 0 input A	67
P7.4	AIN4	I	A/D Analog input 4	68
P7.5	AIN5	I	A/D Analog input 5	69
P7.6	AIN6	I	A/D Analog input 6	70
P7.7	AIN7	I	A/D Analog input 7	71
P8.0	WRRDY5	I	Handshake Write Ready P5	61
P8.0	T3INA	I	MF Timer 3 input A	61
P8.1	RDRDY5	O	Handshake Read Ready P5	60
P8.1	T1INB	I	MF Timer 1 input B	60
P8.2	INT1	I	External interrupt 1	79
P8.2	T1OUTA	O	MF Timer 1 output A	79
P8.2	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	79
P8.3	INT3	I	External interrupt 3	78
P8.3	T1OUTB	O	MF Timer 1 output B	78
P8.3	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	78
P8.4	T1INA	I	MF Timer 1 input A	77
P8.4	$\overline{WAIT}$	I	External Wait input	77
P8.4	WDOUT	O	T/WD output	77
P8.5	P/$\overline{D}$	O	Program/Data space select	76
P8.5	T3INB	I	MF Timer 3 input B	76
P8.6	INT7	I	External interrupt 7	75
P8.6	T3OUTA	O	MF Timer 3 output A	75
P8.7	NMI	I	Non-Maskable Interrupt	74
P8.7	T3OUTB	O	MF Timer 3 output B	74
P9.0	S1OUT	O	SCI1 Serial Output	56

PIN DESCRIPTION (Continued)

Table 1. ST90R50 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P9.1	T0OUTB	O	MF Timer 0 output B	57
P9.1	S1IN	I	SCI1 Serial Input	57
P9.2	CLK1OUT	O	SCI1 Byte Sync Clock output	58
P9.2	TX1CKIN	I	SCI1 Transmit Clock input	58
P9.3	RX1CKIN	I	SCI1 Receive Clock input	59
P9.3	T0OUTA	O	MF Timer 0 output A	59
P9.4	S0OUT	O	SCI0 Serial Output	60
P9.5	S0IN	I	SCI0 Serial Input	61
P9.5	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	61
P9.6	INT2	I	External interrupt 2	62
P9.6	SCK	O	SPI Serial Clock	62
P9.6	WRSTB4	O	Handshake Write Strobe P4	62
P9.7	INT6	I	External interrupt 6	63
P9.7	SDO	O	SPI Serial Data Out	63
P9.7	$\overline{\text{RDSTB4}}$	I	Handshake Read Strobe P4	63

ST90R50 CORE

The Core or Central Processing Unit (CPU) of the ST90R50 includes the 8 bit Arithmetic Logic Unit and the 16 bit Program Counter, System and User Stack Pointers. The microcoded Instruction Set is highly optimised for both byte (8 bit) and word (16 bit) data, BCD and Boolean data types, with 14 addressing modes. Two 8 bit I/O ports are connected to the Core module for external memory interfacing, while a 16 bit Timer/Watchdog gives system security and timing functions, and a Serial Peripheral Interface allows for synchronous communication. Three independent buses are controlled by the Core, a 16 bit Memory bus, an 8 bit Register addressing bus and a 6 bit Interrupt/DMA bus connected to the interrupt and DMA controllers in the on-chip peripherals and the Core. This multiple bus architecture allows a high degree of pipelining and parallel operation within the ST90R50, giving it its efficiency in both numerical calculations and communication with the on-chip peripherals.

MEMORY

The memory of the ST90R50 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The Memory may be expanded with the Bankswitch logic to give paging of the top 32K bytes of each space to expand the ST90R50 addressing capability to 8M bytes in each space. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90R50 addresses all program memory in the external PROGRAM space.

Off-chip memory, addressed using the address and data buses (Port 0, Port 1 and Port 6) and may be divided into the Program and Data spaces by the external decoding of the Program/Data select pin ($P/\overline{D}$) available as an Alternate function. The memory spaces are selected by the execution of the SDM and SPM instructions (Set Data Memory and Set Program Memory, respectively).

MEMORY (Continued)

Figure 3. Memory Spaces, Bankswitch Disabled

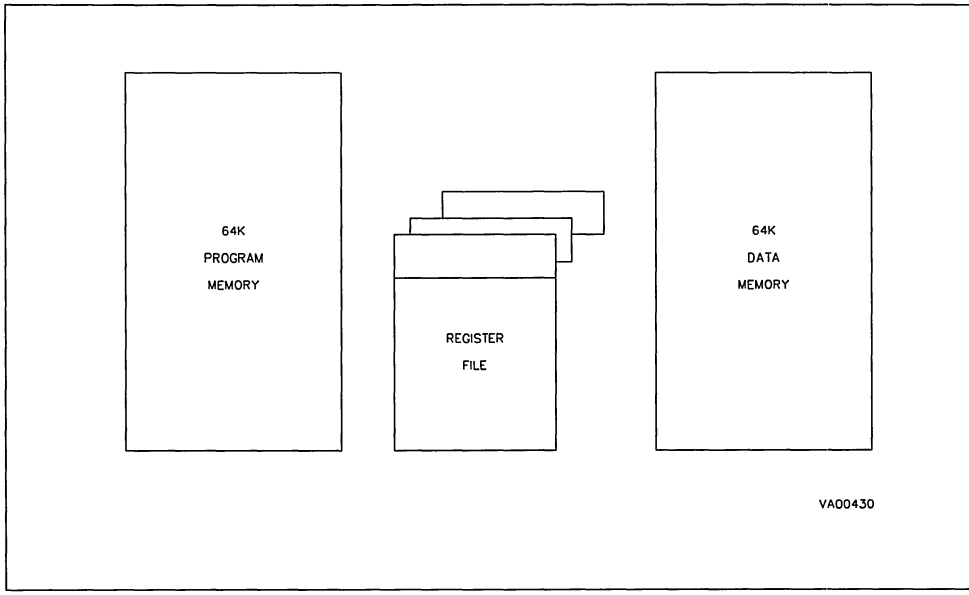
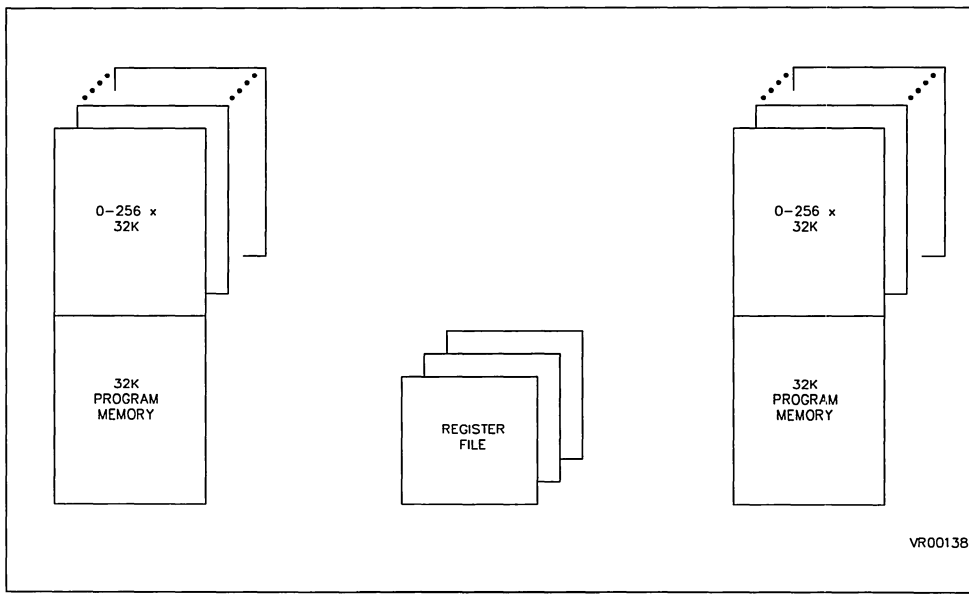


Figure 4. Memory Spaces, Bankswitch Enabled



MEMORY (Continued)

There is no need to use either of these instructions again until the memory area required is to be changed. This requirement is not necessary in two cases: first, when operating with external stacks (the Data memory is automatically selected) and, secondly, when using the memory indirect to memory indirect post-increment addressing mode (the memory types are specified in the instructions: LDPP, LDPD, LDDP, LDDD).

Either the Data Memory or the Program Memory can be addressed using any of the memory addressing modes.

Program Space

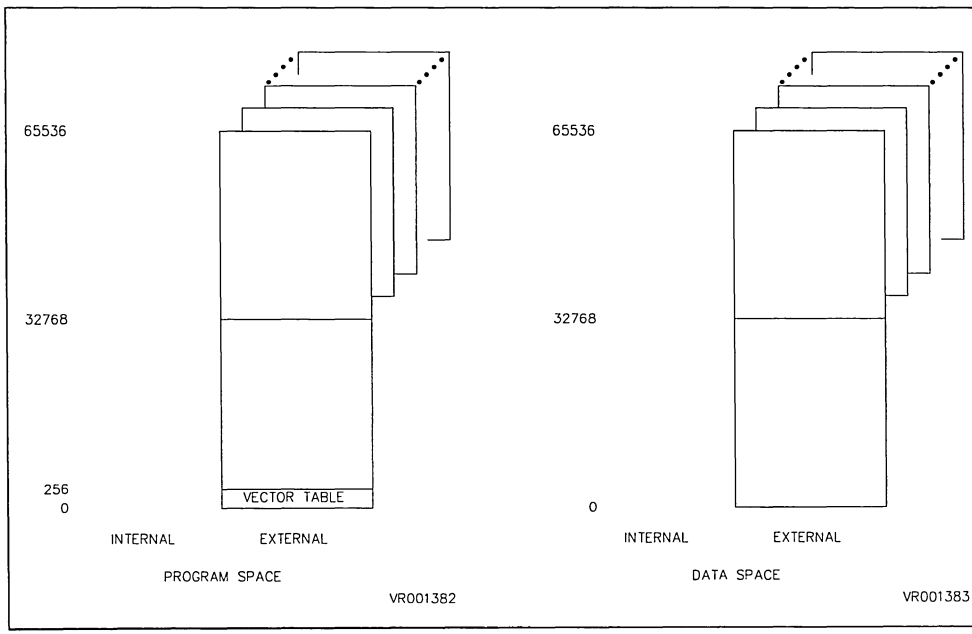
The Program memory space of the ST90R50, 64K bytes of off-chip memory is fully available to the User. The ST90R50 executes external memory cycles for instruction fetches. The first 256 memory locations from address 0 to 0FFh (hexadecimal) hold the Reset Vector, the Top-Level (Pseudo Non-Maskable) interrupt, the Divide by Zero Trap vector and, optionally, the interrupt vector table for use with the on-chip peripherals and the external interrupt sources. Each vector is contained in two consecutive byte locations, the high order address held in the lower (even) byte, the low order address held in the upper (odd) byte, forming the address which is loaded into the Program Counter when selected by the interrupt vector provided by the interrupt source. This should point to the relevant Interrupt Service routine provided by the User for immediate response to the interrupt.

Data Space

The ST90R50 addresses External Data through the External Memory Interface when decoded with the P/$\overline{D}$ pin. On-chip general purpose Registers may be used as additional RAM memory for minimum chip count systems.

The Data Space is selected by the execution of the SDM instruction. All subsequent memory references will access the Data Space. When a separate Data Space is not required, data may stored in external RAM or ROM memory within the Program Space.

Figure 5. Program and Data Spaces



REGISTERS

The ST90R50 register file consists of 240 registers (224 general purpose) plus pages of 16 registers supporting the configuration and control registers for the on-chip peripherals. The 224 general purpose registers all have 8 and 16 bit arithmetic capability and may be used as accumulators, on-chip RAM, internal Stack areas (for system and/or user stacks), or, with the appropriate addressing modes, as index, offset or stack pointers.

The register file is arranged into 16 groups of 16 registers, where the general purpose registers occupy the first 14 groups. The 15th group, E, contains the system registers and Group F contains the pages of the on-chip peripheral control registers.

Group F is paged in this manner due to the modularity of the ST9 family of microcontrollers. Each member of the family retains all general purpose and system registers, only the paged register groups changing owing to the different on-chip peripheral organizations of each device. The User can therefore generate code libraries which use the general purpose registers knowing that they will not be lost on future ST9 devices. To address a paged register, the Page Pointer (PPR, R234) within the system register group must be loaded with the relevant page number using the SPP instruction. Subsequently any access to registers in the top group (R240-R255) will refer to the selected page. This remains set until the next change to the Page Pointer register (by the SPP instruction).

The System group (Group E, registers RE0 to REF) includes the system and user stack pointers, the Mode register, the ALU FLAG register and the Page pointer register. In addition the data registers for the first 6 I/O ports are present, the configuration registers for the ports being in the paged area. This allows the immediate access to these I/O ports at all times.

Figure 6. Register Grouping

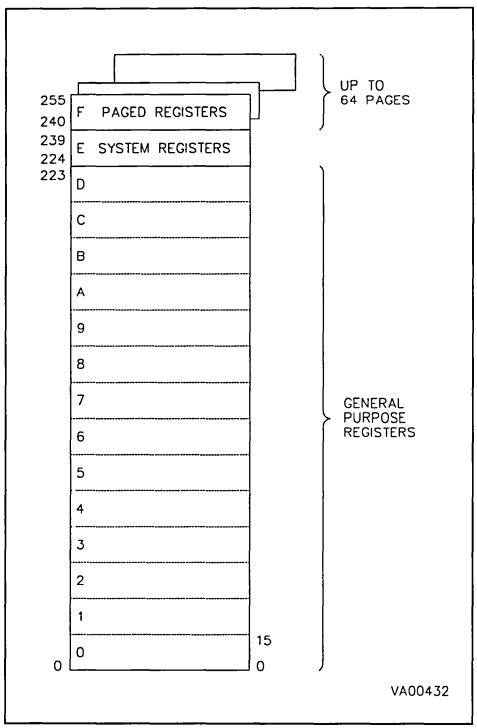
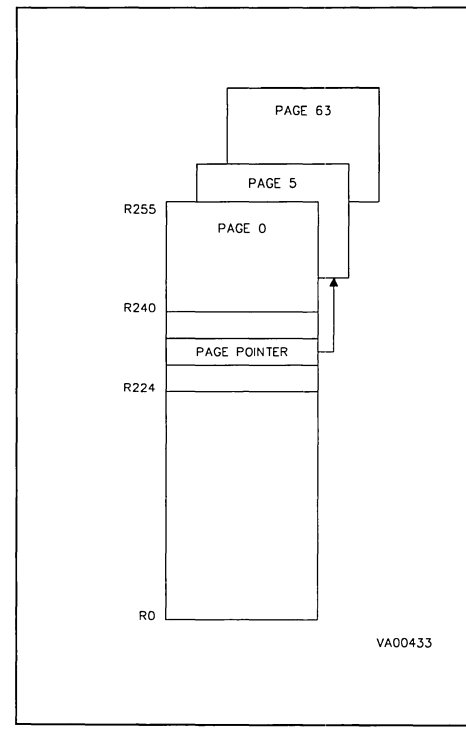
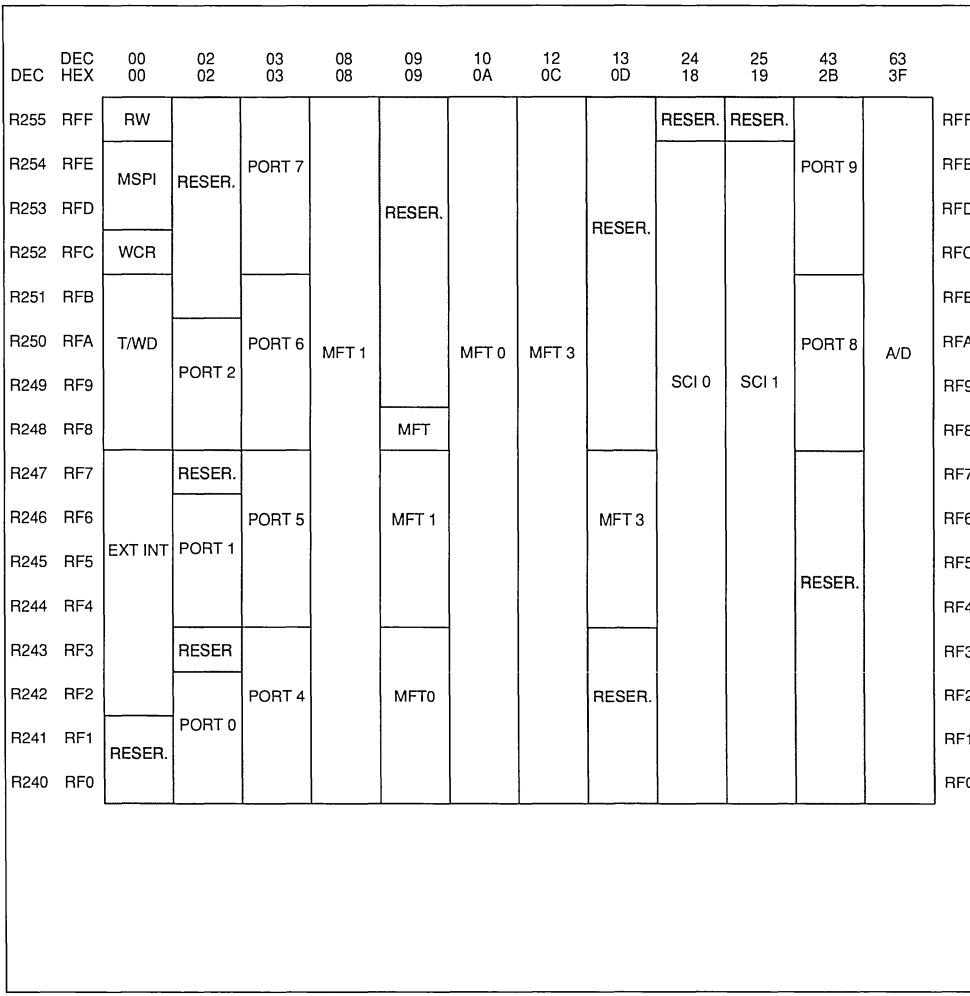


Figure 7. Page Pointer Mechanism



REGISTERS (Continued)

Figure 8. ST90R50 Group F Peripheral Organisation



The Register Pointers, present in the system register group, select groups of registers as "Working Registers", which have faster addressing modes than direct Register addressing and allows smaller code size. The Register Pointers may either be used singly, creating a register group of 16 working registers, or as two independent groups of 8 working registers which may be placed at any 8 register boundary within the register file. The single and twin working register modes are automatically set by hardware when the respective SRP and either SRP0 or SRP1 instructions are executed. If working registers are used as accumulators and RAM locations for particular tasks, fast context switching on interrupts may be achieved by setting the register pointer to another group for the Interrupt Service

REGISTERS (Continued)

Routine, ISR, (e.g. saving the Register pointer on the stack), using the new group in the ISR and subsequently restoring the original group before the Return from Interrupt instruction. Working registers also allow the use of the ABAR - Any Bit-Any Register Boolean operations (including directly on the I/O port data registers).

In the ST9 syntax, directly addressed Registers are indicated with a capital R e.g. R0, R224, RBF, with Register Pairs (16 bit accumulators or memory pointers) as RR0, RR24. When using Working Registers, groups of 16 registers (`SRP` instruction) are denoted as r0 to r15 (rr0 to rr14), while the dual working register group are addressed as r0 to r7 (rr0 to rr6), for the first group of 8 registers (`SRP0`), with r8 to r15 (rr8 to rr14) for the second set (`SRP1`).

Working register addressing requires a 4 bit field within the instruction. When packed into a byte, the upper nibble is set to Dh (1101b), this being the escape code to indicate the use of the working registers. As a result, group D CANNOT be selected with direct register addressing, it is recommended that this group be used as internal stacking area when using register file based system or user stack pointers.

Figure 9. Groupe E Register Map

R239	System Stack Pointer Low (SSPLR)
R238	System Stack Pointer High (SSPHR)
R237	User Stack Pointer Low (USPLR)
R236	User Stack Pointer High (USPHR)
R235	Mode Register (MODER)
R234	Page Pointer (PPR)
R233	Register Pointer 1 (RP1R)
R232	Register Pointer 0 (RP0R)
R231	ALU Flags (FLAGR)
R230	Central Interrupts Control (CICR)
R229	Port 5 Data (P5DR)
R228	Port 4 Data (P4DR)
R227	Port 3 Data (P3DR)
R226	Port 2 Data (P2DR)
R225	Port 1 Data (P1DR)
R224	Port 0 Data (P0DR)

Figure 10. Single Working Register Bank

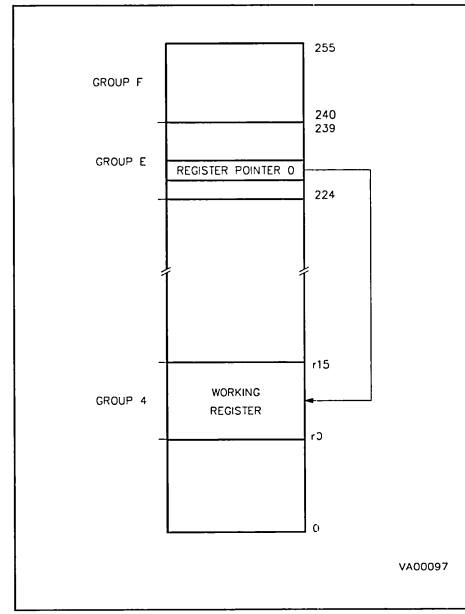
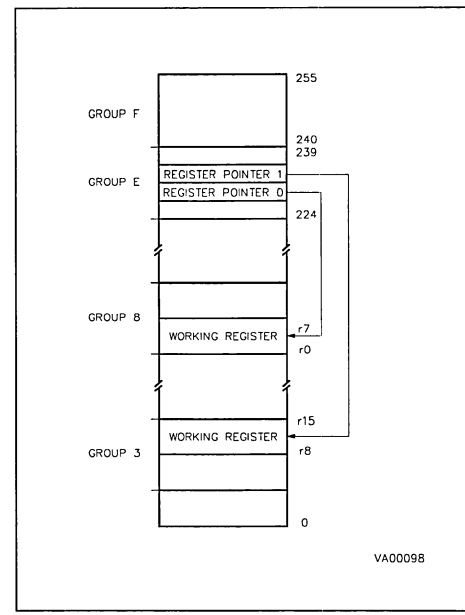


Figure 11. Dual Working Register Banks



STACK POINTERS

There are two separate, double register stack pointers available (System and User), both of which can operate in register or Data memory address spaces. These operate in a Pre-Decrement mode when data is PUSHed onto the Stack and in a Post-Increment mode when data is POPed from the stack.

The SYSTEM Stack Pointer (SSPR, R238:R239) is used for the storage of temporarily suspended system and/or control registers (ie the the Program Counter and FLAG register) while interrupts are being serviced, and is used for the storage of the Program Counter following the CALLing of a subroutine.

The USER Stack Pointer (USPR, R236:R237) is completely free from all interference from automatic operations and so provides for a totally User controlled stack area.

Both Stack pointers may operate with both byte (PUSH,POP) and word (PUSHW,POPW) data, and are differentiated by appending a "U" to the instruction mnemonic for the User Stack (PUSHU/PUSHUW, POPU/POPUW).

When the Stack Pointers are using RAM Memory as the stack areas, a full word register is used as the pointer, while when operating with the stack area within the Register File (Groups 0 to 14 only, but not the within the system and paged groups) only an 8 bit register is required for addressing and consequently only the low byte of the word registers are used (R239 for the System Stack and R237 for the User Stack). In this latter case the upper byte of the stack pointer registers (R238 and R236) must be considered as reserved. The Stack Pointers may be selected to point to RAM or Register file by the setting of the SSP (MODER.7) and USP (MODER.6) of the ST90R50 configuration register (MODER, R235) where a "1" denotes Register file operation (Default at Reset) and "0" causes external Data space operation.

Figure 12. Internal Stack Pointers

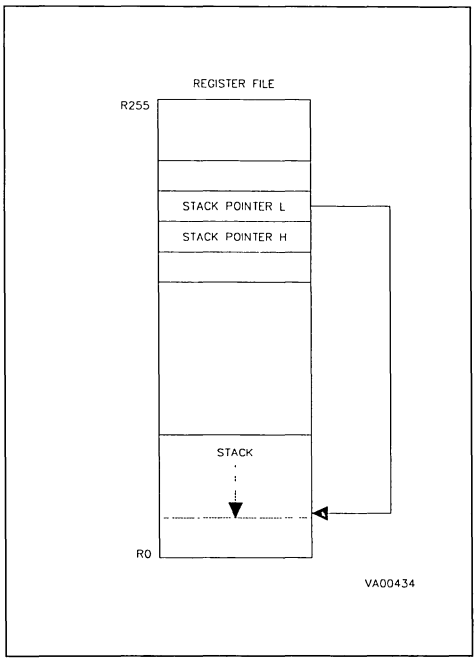
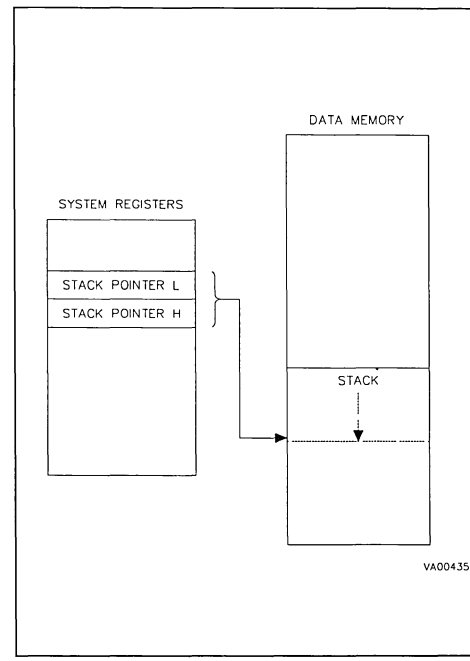


Figure 13. External Stack Pointers



INTERRUPTS

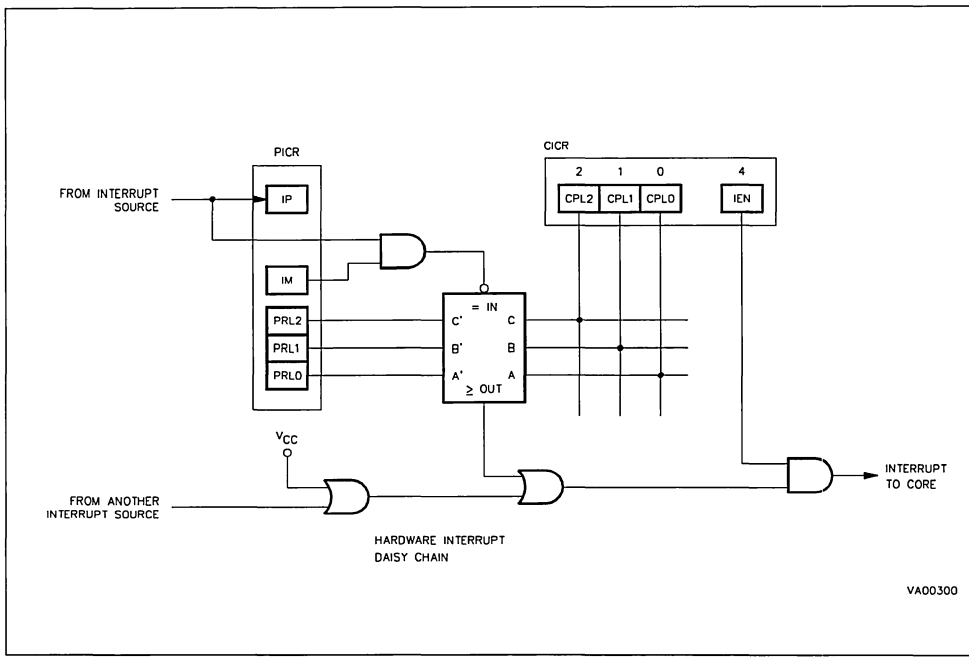
The ST90R50 offers a powerful solution to the response requirements of real-time systems with its advanced interrupt structure. Interrupt trigger sources can be prioritized within 8 levels to match the priorities assigned to the application. In addition a top-level or non-maskable interrupt is available.

The ST90R50 interrupts follow the logical flow of Figure 14.

Interrupt events (selectable with each function) cause the setting of the Interrupt Pending (IP) bit within the status register of the peripheral. This bit may also be set by software in order to generate a software interrupt, and should normally be reset by software within the interrupt service routine. If the interrupt is not Masked with the corresponding Interrupt Mask bit, the interrupt is passed to the central interrupt control logic where the priority level assigned by the User to the interrupt source is compared with the priority level of the core (User programmed dynamically in the 3 bits of the Central Priority register (CPL, CICR.0-2, Level 7 is the lowest priority and level 0 the highest). If the incoming priority level is higher than the CPL, and Global Interrupts are enabled (by the `EI` instruction, interrupts are disabled by the execution of the `DI` instruction), the interrupt is acknowledged. If interrupts are globally disabled, the priority level of the source is lower than or equal to the CPL or the Interrupt is masked, then the IP bit remains set and the interrupt is held pending until the `EI` instruction is executed, the CPL is set to a lower level AND the interrupt is un-masked. Alternatively the IP bit of a masked interrupt source may be used in a polled interrupt environment, with the IP bit being reset by software within the service routine.

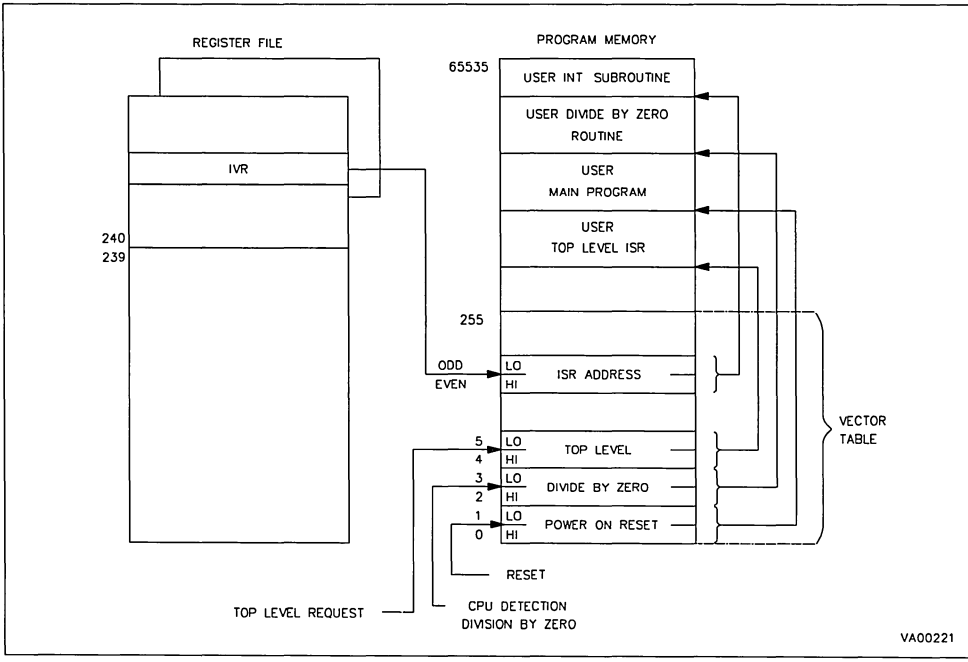
The interrupt acknowledge cycle causes the Program Counter and FLAGS register to be pushed onto the System Stack (PC low byte first, PC high byte, then FLAGS Register) and all maskable interrupts to be disabled by resetting the IEN bit (CICR.4). The peripheral Interrupt Vector, IVR, a User programmable feature of the peripheral interrupt control registers, is used as an offset into the vector table, pointing to the high byte (even address) of the 16 bit address which should contain the starting address of the interrupt service routine. Addresses 0 through 255 of the program space comprise the interrupt vector table. Where multiple

Figure 14. Interrupt Logic



INTERRUPTS (Continued)

Figure 15. Interrupt Vector Table Usage



interrupt sources may occur within a peripheral, the peripheral interrupt vector source may be encoded by hardware set bits within the IVR register. This means that the vector address defined in the peripheral IVR is the base address for a block of vectors servicing that peripheral. The address pointed to by the vector is loaded into the Program Counter and execution restarts from this point.

The interrupt service routine should clear the interrupt pending flag of the interrupt source and take the appropriate action. The last instruction of the interrupt service routine should be the IRET instruction, the action of this is to restore the Program Counter and Flags register to their value prior to the interrupt acknowledgment, and to re-enable interrupts. Within the interrupt service routine, use may be made of the working register pointer mechanism to reduce the context switching time.

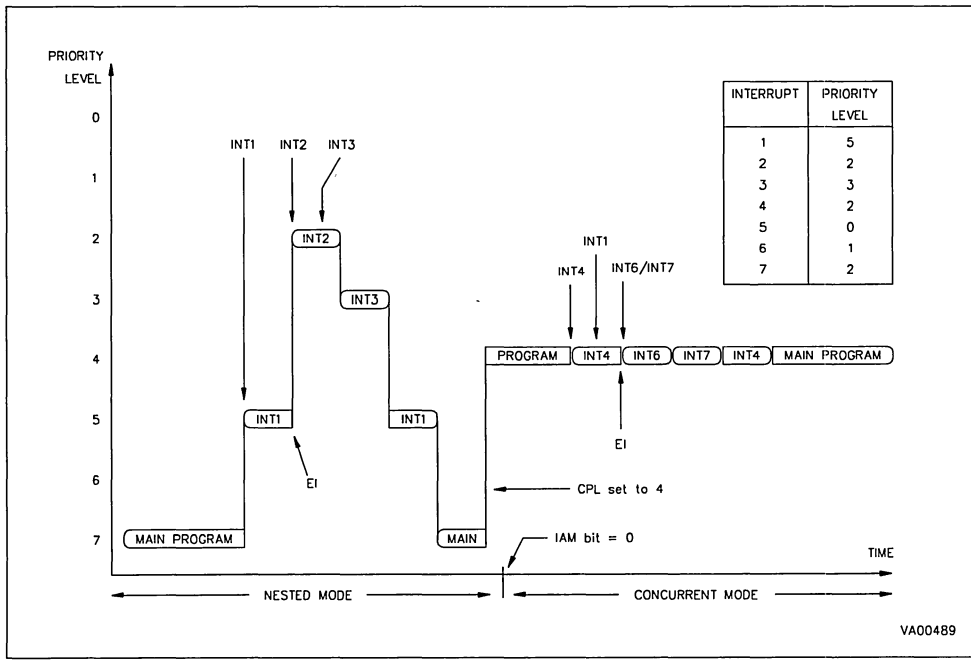
Two interrupt arbitration modes are available for use with the 8 level priority scheme, Nested and Concurrent modes. These are selected by the status of the IAM bit (CICR.3).

Concurrent mode, selected when IAM = "0" (the reset condition) is the standard interrupt arbitration mode, where the arbitration phase of every instruction acknowledges interrupts according to their priority level (if higher than the CPL) and follows the sequence shown. All pending interrupts existing or having eventually occurred during interrupt service routine execution, remain pending until the Enable Interrupt instruction (EI) (even if it is executed during the interrupt service routine). EI within the interrupt service routine is not recommended for use with the Concurrent arbitration mode as this can trigger a Last In, First Out condition where high priority interrupts are masked by lower priority interrupts which are all higher than the CPL value.

Nested mode, selected when IAM = "1", uses the same arbitration phase as concurrent mode, the difference being that the CPL is modified during the interrupt processing cycle to that of the acknowledged interrupt level. The CPL value is pushed by hardware into the Nested Interrupt Control register (NICR, R247 page 0) by setting the NICR bit corresponding to the CPL value. The interrupt service

INTERRUPTS (Continued)

Figure 16. Interrupt Modes Example of Usage



routine is entered in the normal manner. The revised CPL level is used for arbitration of further interrupts, each higher level being saved on the NICR stack, and being restored automatically by hardware with the `IRET` instruction. This allows the execution of the `EI` instruction within the interrupt service routine to operate the correct nesting of interrupts. The two modes are shown graphically in Figure 16, where the Y axis shows the CPL value. It should be noted that in the example INT1 will not be acknowledged until the CPL level is programmed to a lower level.

Interrupts coming from on-chip sources at the same instant, and at the same priority level, are resolved during the arbitration phase according to a hardware daisy-chain. This follows the priorities of the table shown in Table 2.

Table 2. ST90R50 Interrupt Hardware Daisy Chain

INTA	High Priority
INTB	
INTC	
INTD	
MFTIMER0	
SCI 0	
SCI 1	
A/D	
MFTIMER3	
MFTIMER1	Lowest Priority

INTERRUPTS (Continued)

External Interrupts. Up to 8 external interrupts are available on the ST90R50 as alternate function inputs of I/O pins. These may be selected to be triggered on rising or falling edges and can be independently masked. The eight external interrupt sources are grouped into four pairs or channels which can be assigned to independent interrupt priority levels. Within each channel the even interrupt number takes the even priority level and the odd channel the odd priority level (even+1).

Table 3. External Interrupt Channel Grouping

External Interrupt	Channel
INT7 INT6	INTD1 INTD0
INT5 INT4	INTC1 INTC0
INT3 INT2	INTB1 INTB0
INT1 INT0	INTA1 INTA0

Several of the External Interrupt channels have their inputs selectable between the external interrupt source and on-chip peripheral sources.

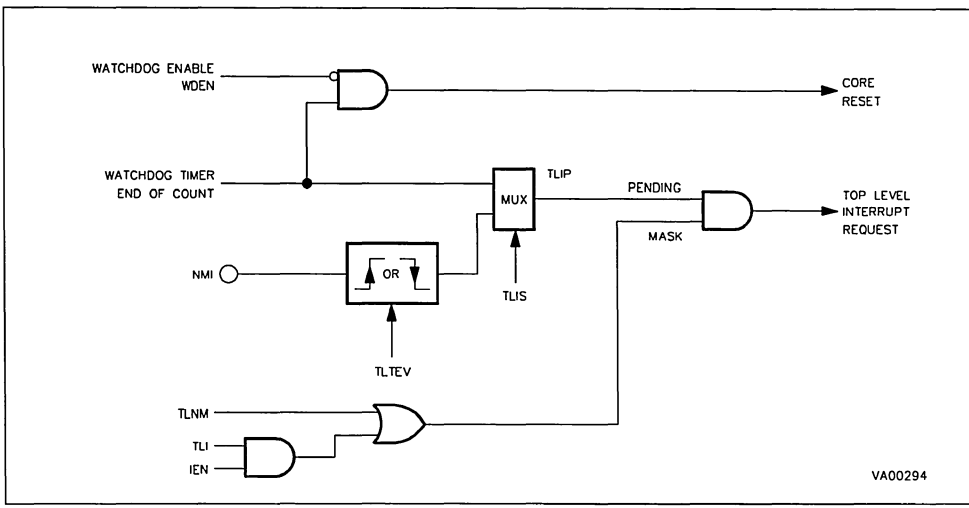
Table 4. ST90R50 External Interrupt Souce Selection

INT0	INTA0
Timer/Watchdog End of Count	
INT2	INTB0
SPI Interrupt	

Top Level Interrupt. The Top Level Interrupt channel can be assigned either to the external NMI pin or to the Timer/Watchdog output. When selected as the external NMI pin, the active edge may be programmed to be rising or falling. The TLI event will cause the setting of the TLIP bit (CICR.6) and according to the mask situation, a Top Level Interrupt request may be generated. Two masking conditions are available, a Maskable Mask and a Not-Maskable Mask.

The Maskable Top Level Interrupt may be enabled or disabled by software and follows the state of the Global Interrupt Enable bit IEN (CICR.4), while the Not-Maskable Mask bit (TLI, CICR.5) is a set-only mask. Once set, the Top Level Interrupt is active independently of IEN and cannot be disabled until the next Reset cycle.

Figure 17. Top-Level Interrupt Structure



DMA

The ST90R50 has on-chip DMA channels to provide high-speed data transaction between peripherals and Memory or Register File. Multi-channel DMA is fully supported because each peripheral can have its own DMA channel(s). Each DMA channel transfers data to/from contiguous locations of the Register File, Program Memory or Data Memory. The maximum number of transactions that each DMA channel can perform is 222 if the Register File is selected and 65536 if Program or Data Memory are selected.

DMA transfer to (or from) the Register File takes 8 INTCLK cycles, DMA transfer to (or from) Memory takes 16 INTCLK cycles. If the ST90R50 is in the idle mode (following the execution of the WFI instruction), DMA requests are acknowledged according to their priority and control is returned to the idle mode pending an interrupt, this operation increases the number of INTCLK cycles by 2 for both Register File and Memory DMA transactions.

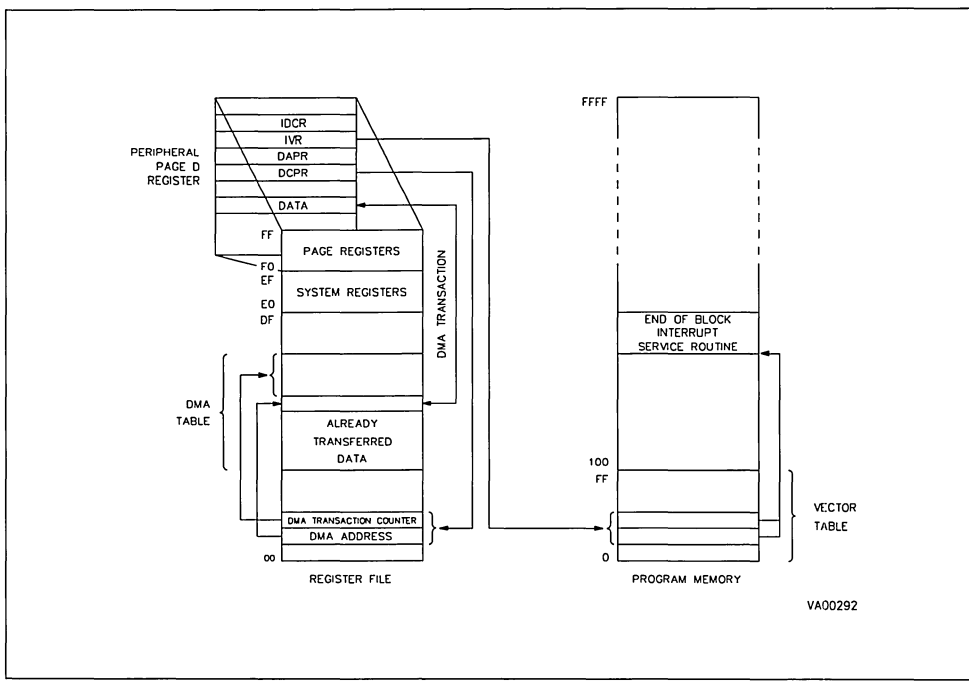
Each DMA channel has its own control registers located in the page(s) related to the peripheral.

There are two pointer registers, DAPR which points to a register or register pair containing the current DMA address to/from which data will be transferred, and DCPR, which points to a register or register pair which contain the transaction counter for the DMA operations. Each DMA transfer consists of three operations:

- A load from/to the peripheral data register to/from a location of Register File (or Memory) addressed through the DMA Address Register (or Register Pair)
- A post-increment of the DMA Address Register (or Register Pair)
- A post-decrement of the DMA transaction counter, which contains the number of transactions that have still to be performed.

When the transaction counter reaches 0 (all data has been transferred) an End of Block Interrupt event is generated to allow the processing of the DMA data block, or, by reloading the Address and counter registers and retriggering, a repeated DMA cycle.

Figure 18. DMA Between Registers and Peripheral

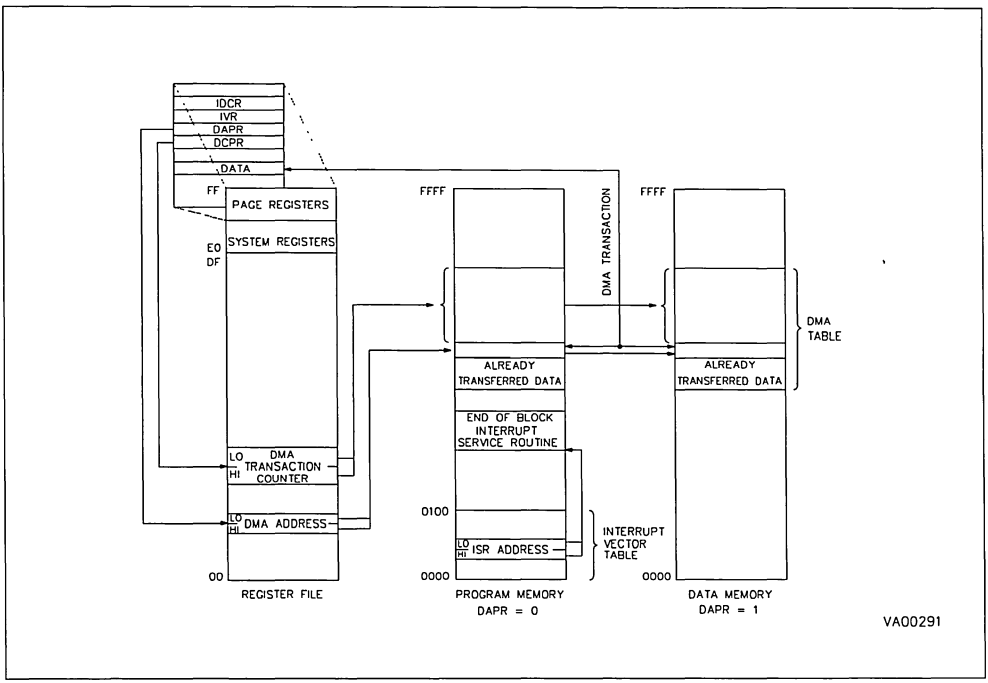


DMA (Continued)

A SWAP mode, allowing continuous DMA operation, is available for the Multifunction Timer and is described in the section relating to the Multifunction Timer.

The ST90R50 has DMA channels associated with the Serial Communications Interface Input and Output Serial data channels; the 16 bit Load/Capture Register 0, CAPT0R, of each Multifunction Timer allowing the timing of external signals to be captured into a table for off-line analysis or for the automatic output of PWM signals of variable width and timing; and the 16 bit Comparison Register 0, COMP0R, of each Multifunction Timer which can be programmed to cause output or input of parallel data through the handshake ports under DMA.

Figure 19. DMA Between Memory and Peripheral



CLOCK GENERATION, WAIT, HALT AND RESET

Clock Generation

The ST90R50 Clock Generator module generates the internal clock for the ST9 core and the on-chip peripherals, it may be driven by an external quartz crystal circuit, connected to the OSCIN and OSCOUT pins, or by an external pulse generator connected to OSCIN (Figures 20, 21).

The conceptual schematic of the ST9 internal clock circuit is shown in Figure 22.

The maximum external frequency of the ST9 is 24 MHz, while the maximum internal operating frequency is 12 MHz, thus a programmable divide by two circuit is present, this allows the use of high frequency crystals for economy, or low frequency crystals for reduction in radiated noise. This divider is active upon exit from the reset condition, the User may bypass the divide by two circuit by setting the DIV2 bit (MODER.5). The resulting clock from this section is named INTCLK, the internal clock which drives the timebases of the on-chip clock for the ST90R50 peripherals (eg the Multifunction Timer,

Figure 20. Crystal Oscillator

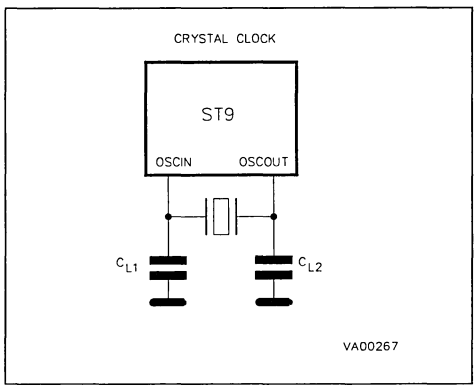


Figure 21. External Oscillator

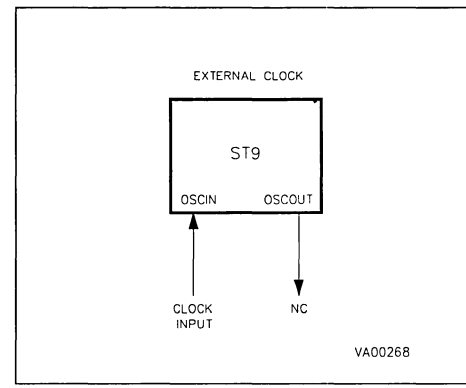
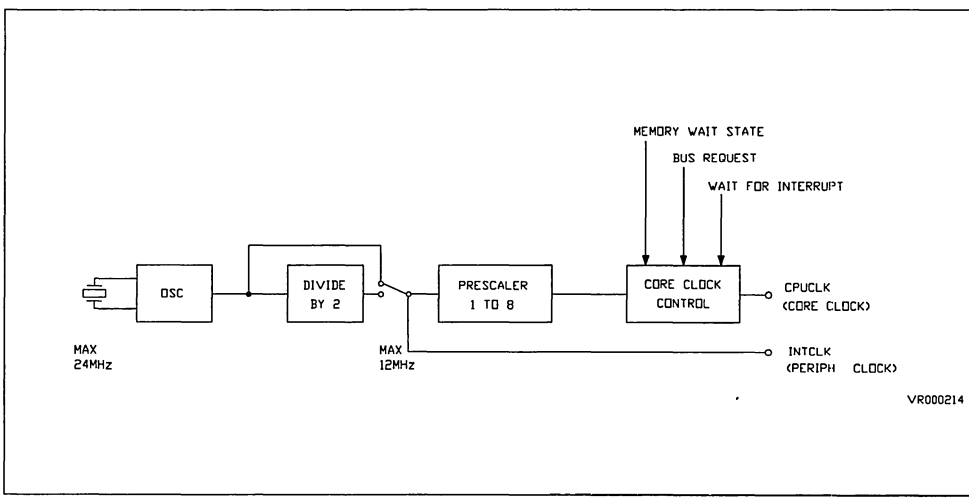


Figure 22. Internal Clock Circuit



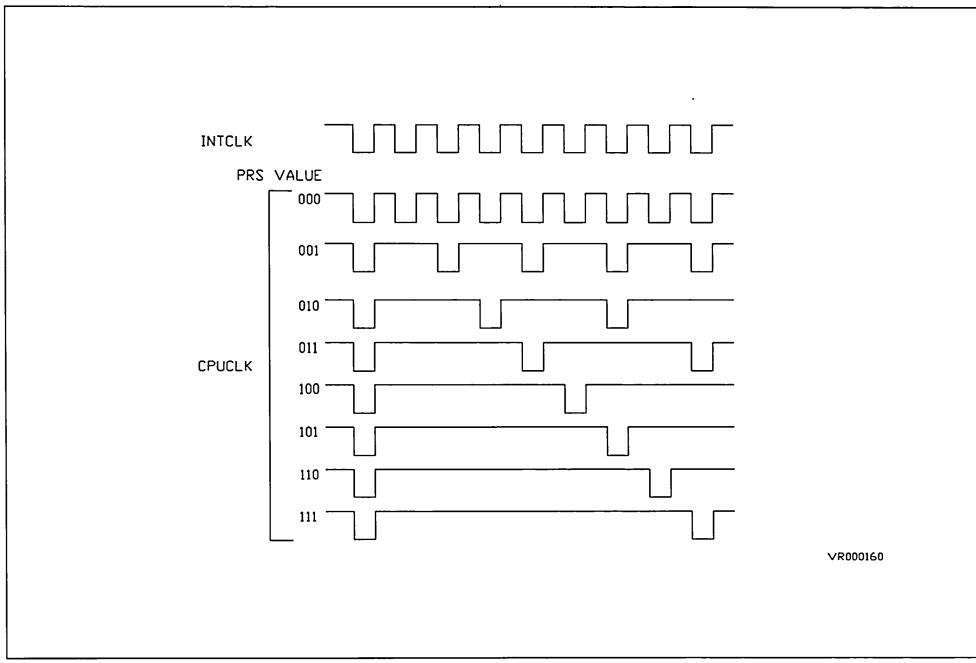
CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Timer/Watchdog, Serial Communications Interface) and also the input of the CPU prescaler section. The CPU of the ST9 includes the instruction execution logic and may run at different rates according to the setting of the PRS2,PRS1 and PRS0 bits (MODER.4-2) (figure 23). The resulting clock is named CPUCLK and it should be noted that this does not maintain a 50% duty cycle, but stretches the high level of the clock until completion. The CPUCLK prescaler allows the User to slow down the program execution time (eg for lower power consumption), while time-critical sections of the program may tune the CPUCLK execution speed to high speed and then restore it to its original speed.

Wait States

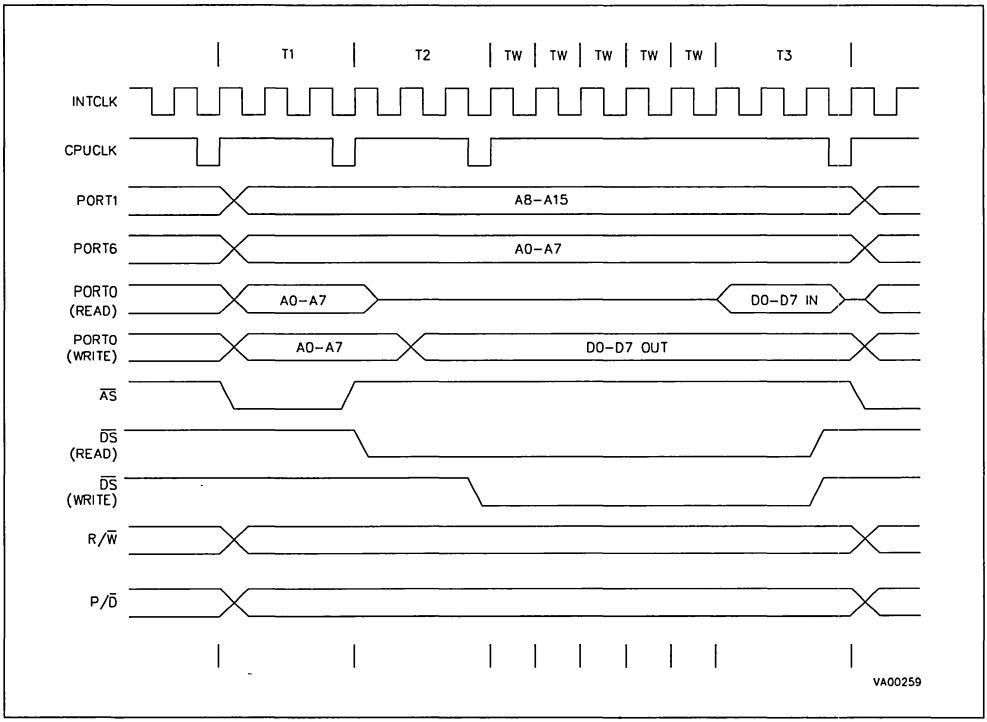
The output from the prescaler can also be affected by wait states. Wait states from two sources allow the User to tailor timing for slow external memories or peripherals. The internal Wait State generator will insert from 0 to 7 wait states, independently programmable for both Program and Data Spaces, via the Wait Control Register WCR (R252, page 0). The second source of wait states is the external Wait input pin when enabled as the Alternate Function. Fig 24 shows the External Memory Interface timing as it relates to CPUCLK prescaling of 2 and 5 added wait states. The added wait states are derived from the INTCLK clock cycle, not CPUCLK. Internal memory is always accessed with no Wait states.

Figure 23. CPUCLK Prescaler



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Figure 24. External Memory Interface Timing with CPUCLK Prescaling and 5 Added Wait States

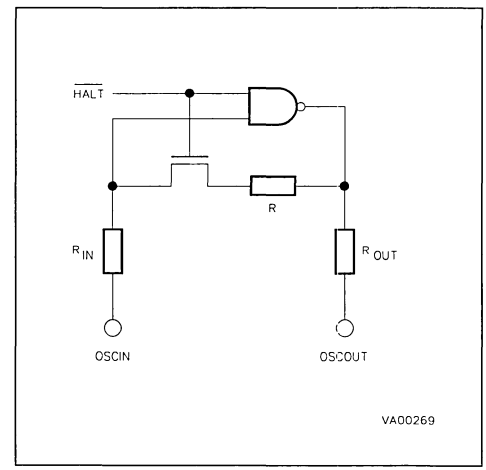


Halt and Wait for Interrupt (WFI) States

The schematic of the on-chip oscillator circuit is shown in figure 25. The HALT condition, caused by the execution of the HALT instruction, disables the oscillator, forcing OSCOUT high. This places the ST90R50 into the lowest power mode. The exit of the HALT condition and the restarting of the oscillator requires a RESET pulse with a minimum duration of 10ms (figure 26). It must be noted that if the TIMER/WATCHDOG has the WATCHDOG mode enabled, a HALT instruction will not disable the oscillator; this is to avoid stopping the Watchdog if, by an error, a HALT instruction is executed. If this occurs, the ST90R50 runs in an endless loop terminated only by the Watchdog reset (or hardware reset).

The WFI (Wait for Interrupt) instruction suspends program execution until an interrupt request is acknowledged. During this period, DMA transactions are allowed if their priority is higher than or equal to the CPL level; the ST90R50 returns to WFI

Figure 25. Oscillator Schematic



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

mode after completion of the DMA transfer. The CPUCLK is halted during Wait For Interrupt while INTCLK continues to run, thus the power consumption of the processor is lowered by the CORE power consumption value.

The External Memory Interface lines status during HALT and WFI modes is shown in Table 5.

Table 5. External Memory Interface Line Status During WFI and Halt

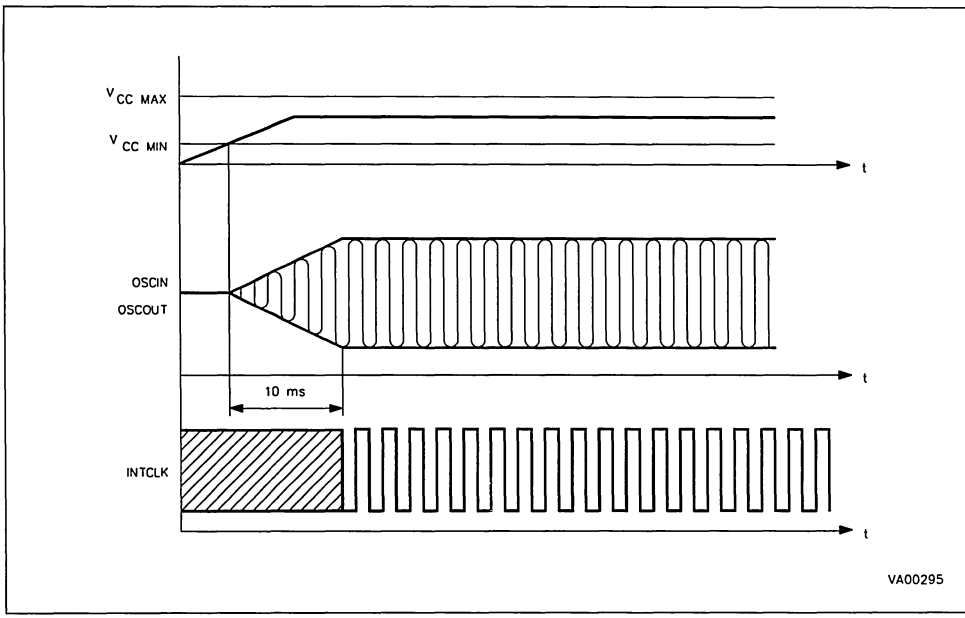
P0 (AD0-AD7)	High Impedance
P1 (A8-A15)	Forced to Address of Next Opcode
$\overline{AS}$	Forced High
$\overline{DS}$	Forced High
R/$\overline{W}$	Forced High

Reset

The processor Reset overrides all other conditions and forces the ST90R50 to the reset state. During Reset, the internal registers are set to their Reset values, as shown in Table 6 for the system and Page 0 Registers. The I/O Ports pins are set to the Bidirectional Weak Pull-up mode. The User must then initialize the ST90R50 registers to give the required functions.

The Reset condition can be generated from the external $\overline{RESET}$ pin or by the on-chip TIMER/WATCHDOG operating in Watchdog mode. To guarantee the complete reset of the ST90R50, the $\overline{RESET}$ input pin must be held low for at minimum of 53 crystal periods in addition to the crystal start-up period. The Watchdog $\overline{RESET}$ will occur if the Watchdog mode is enabled (WDEN, WCR.6, is reset) and if the programmed period has elapsed without the code 0AAh,55h written to the appropriate register. The input pin $\overline{RESET}$ is not driven low by the on-chip reset generated by the TIMER/WATCHDOG.

Figure 26. Reset Timing Requirements from Halt State



CLOCK GENERATION, WAIT, HALT AND RESET (Continued)

Table 6. System and Page 0 Reset Values

Register Number	System Register Reset Value	Page 0 Register Reset Value
F	(SSPLR) = undefined	Reserved
E	(SSPHR) = undefined	(SPICR) = 00h
D	(USPLR) = undefined	(SPIDR) = undefined
C	(USPHR) = undefined	(WCR) = 7Fh
B	(MODER) = E0h	(WDTCR) = 12h
A	(Page Ptr) = undefined	(WDTPR) = undefined
9	(Reg Ptr 1) = undefined	(WDTLR) = undefined
8	(Reg Ptr 0) = undefined	(WDTHR) = undefined
7	(FLAGR) = undefined	(NICR) = 00h
6	(CICR) = 87h	(EIVR) = x2h
5	(PORT5) = FFh	(EIPLR) = FFh
4	(PORT4) = FFh	(EIMR) = 00h
3	(PORT3) = FFh	(EIPR) = 00h
2	(PORT2) = FFh	(EITR) = 00h
1	(PORT1) = FFh	Reserved
0	(PORT 0) = FFh	Reserved

During the $\overline{\text{RESET}}$ state, $\overline{\text{DS}}$ is held low and $\overline{\text{AS}}$ is toggled with the frequency of the crystal (OSCIN) divided by 32. This condition may be recognized by external peripherals as a Reset condition. It may also be used to enable the synchronization of multiple ST90R50 running from the same clock in a multi-processing or high security majority voting system.

Once the Reset pin reaches a logical high, the ST90R50 fetches the starting address from locations 0 and 1 of the program space and begins program execution from this address after 67 crystal cycles.

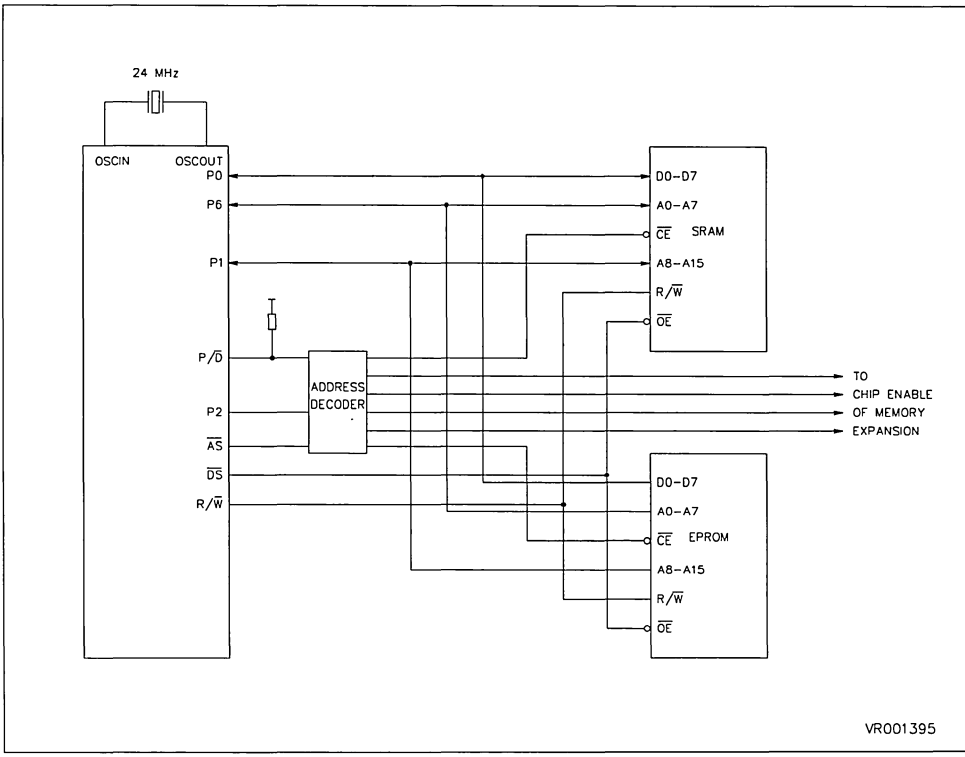
INTERFACING TO EXTERNAL MEMORY

External Memory and/or peripherals may be connected to the ST90R50 through its External Memory Interface. This provides the multiplexed Address bits A0 to A7 and Data bits D0 to D7 on Port 0, and the higher order address bits A8 to A15 on Port 1, giving the full 64K bytes addressing capability. Port 6 is available to be programmed as non-multiplexed address outputs A0 to A7 to reduce the requirement for an external latch to demultiplex the low order addresses. Port 0, in this case, becomes solely the Data I/O port. The Program/Data (P/$\overline{D}$) output, when selected as an Alternate function, allows external decoding to provide for the two independent pages for Program and Data.

Data transfer timing is generated by the Address strobe $\overline{AS}$ and the data strobe $\overline{DS}$. Address strobe low indicates that the data present on AD0 to AD7 is the low order address and is guaranteed valid on the rising edge of $\overline{AS}$ allowing for latching of the address bits by an external latch (if Port 6 is not used). Data transfer direction is indicated by the status of the Read/Write (R/$\overline{W}$) pin; for write cycles (R/$\overline{W}$ low), data out is valid at the falling edge of $\overline{DS}$; for read cycles (R/$\overline{W}$ high), data in must be valid prior to the rising edge of $\overline{DS}$. The timing of the R/$\overline{W}$ signal may be modified by the setting of the RW bit (bit 0 Register 0FFh, page 0) in order to accomodate different types of external memories. In addition, when the Bank Switch logic is enabled, the timing of the Bank Switch outputs may be modified by software to prevent potential conflicts on the data bus. Please refer to following sections for further details.

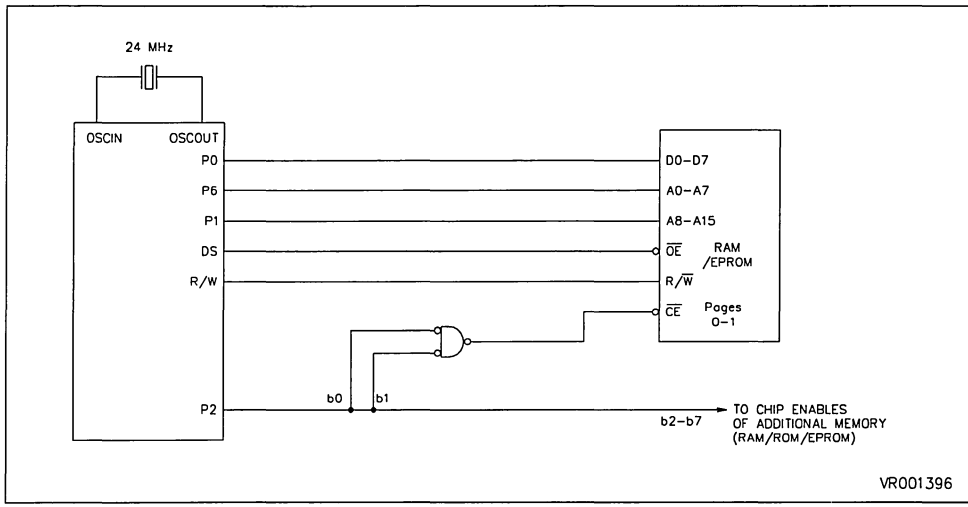
The Data Strobe low period may be extended to accomodate slow external devices by the adding of internally generated wait cycles (0 to 7 cycles for both program and data memory maps) or by an external input on the WAIT input pin also available as an Alternative Function of an I/O bit. Suggested interface circuits are shown in figures 27 and 28.

Figure 27. External Memory Addressing Circuit



INTERFACING TO EXTERNAL MEMORY (Continued)

Figure 28. External Memory Addressing Circuit



BANKSWITCH LOGIC

Port 2 of the ST90R50 may be programmed by the User to become extended address lines allowing expansion of the memory to a maximum of 8M bytes in both program and data pages. This is achieved by paging of the top 32K bytes of memory (A15 high, addresses 8000h to FFFFh), with the lower 32K bytes (A15 low addresses 0000h to 7FFFh) remaining static. The static area, segment 0, allows for the direct access to interrupt service and page change routines, and other common sub-routines, while the paged segments (1 to 256) of 32K bytes may contain additional program code, database entries, printer fonts, buffer space, or any other function requiring a large amount of memory.

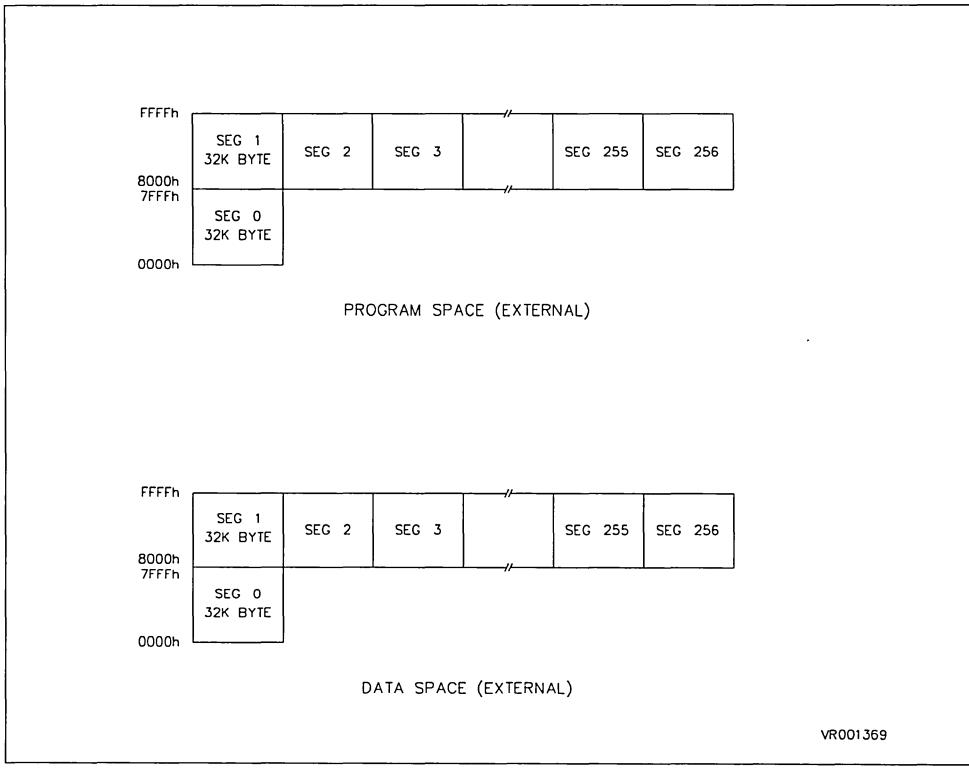
The setting of Port 2 is made during the Reset cycle, by the latched status of the signals BSH_EN1 and BSL_EN1. These control the high and low nibbles of Port 2 between Address Expansion lines and normal I/O lines as shown in Table 7.

Table 7. Port 2 Nibble Programming For Bank Switch and I/O

BSH_EN1	BSL_EN1	BS Port Nibble		BS Port Reset Value	
		High	Low	High	Value
O	O	I/O	I/O	- -	- -
O	I	I/O	BS	- -	0FEh
I	O	I/O	BS	- -	0FEh
I	I	BS	BS	0FEh	0FEh

In order to program the functions, weak pull-up/down resistors (100k ohm) on the BSH_EN1 and BSL_EN1 designated lines are used to generate the logic level latched on the rising edge of the Reset input. After this event, these lines may be used as I/O and be programmed in the normal way.

Figure 29. Bank Switch Memory Maps

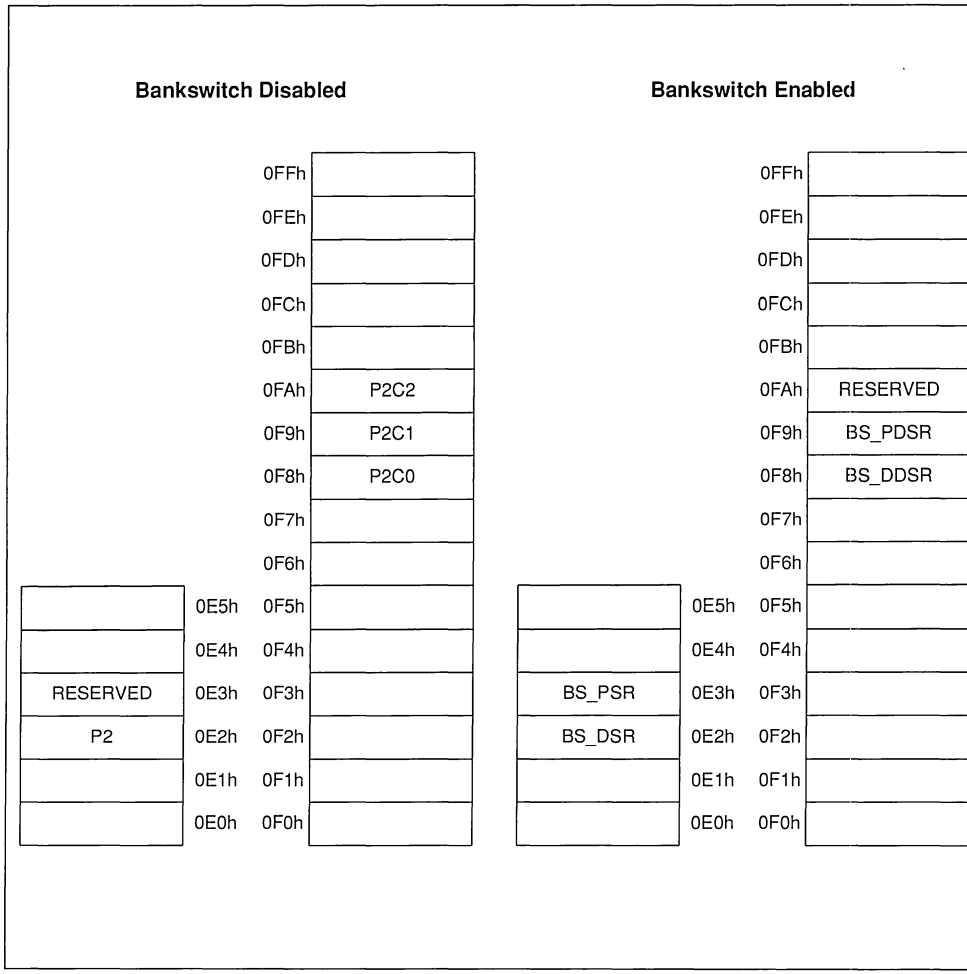


When the Address Expansion is selected, several I/O port configuration registers take an alternative function. The Port Data Registers for I/O ports 2 and 3 (Registers E2h and E3h) become the Bank Switch Data Segment Register and Bank Switch Program Segment Register respectively. The values held in these registers are output on Port 2 whenever a memory access is made to either data or program spaces with A15 high. This allows Port 2 bits to represent either extended address lines A16 to A23 or to output chip-selects to external memories. For this second option the reset value for these registers, and the value output whenever A15 is low, is 0FEh, generating the selection of a standard "startup" page automatically. Port 2 Configuration registers P2C0 and P2C1 contained in I/O Page 2 hold the User programmed values output on Port 2 for DMA cycles with addresses in the the high 32K byte of the memory for data and program spaces respectively.

Warning: The Bankswitch Program DMA register occupies the same register as Port 2 Control Register 2 (P2CR), so caution must be taken in writing to BS_PDSR when the high nibble is used as I/O and the low nibble is used for the Bankswitch output as P2C2 is used for the port configuration. The Program and Data Segment Registers are located in the direct Register file within the System Register group in order to be immediately accessible, while the DMA Segment Registers are held within an I/O page as, once programmed, they do not need constant service.

BANKSWITCH LOGIC (Continued)

Figure 30. Bank Switch Register Mapping



BANKSWITCH LOGIC (Continued)

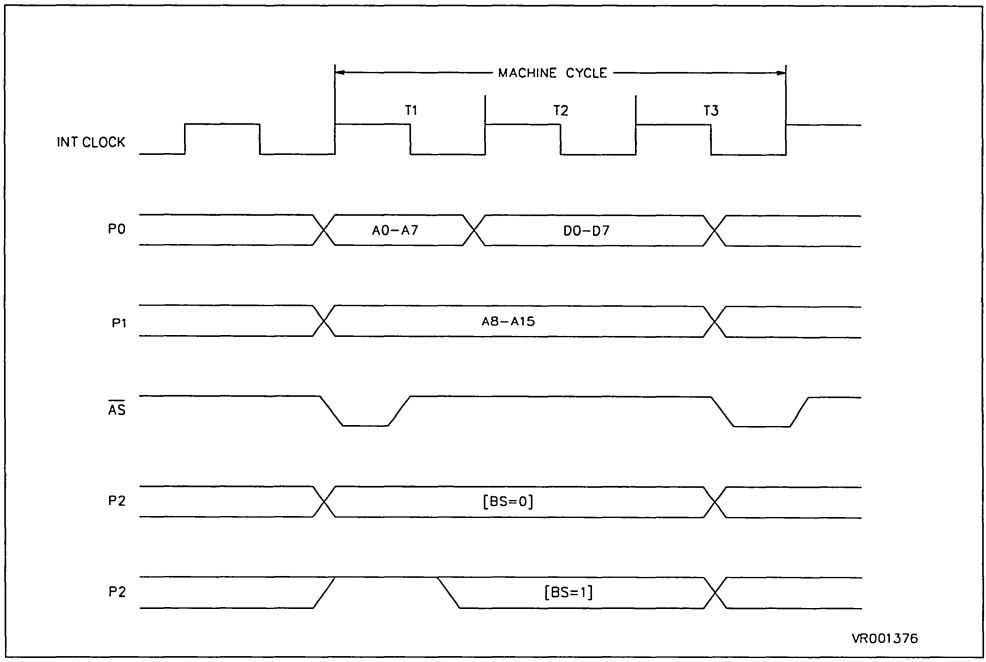
Output Timing

In order to prevent potential bus conflicts on Port 0 (Address/Data multiplexed) during the address strobe time when using the Bankswitch logic, the timing of the Bankswitch outputs may be modified by software. This is achieved by setting to "1" bit 1 of Register 0FFh in I/O page 0. This causes the Bankswitch outputs to be all high during the address strobe period. The reset condition provides normal timing and status.

The timing of the Read/Write signal may be modified as shown in the next figure by setting to "1" bit 0 of Register 0FFh in I/O page 0. This allows the use of different types of external memories. When this bit is "0" (the reset state) normal timing is generated.

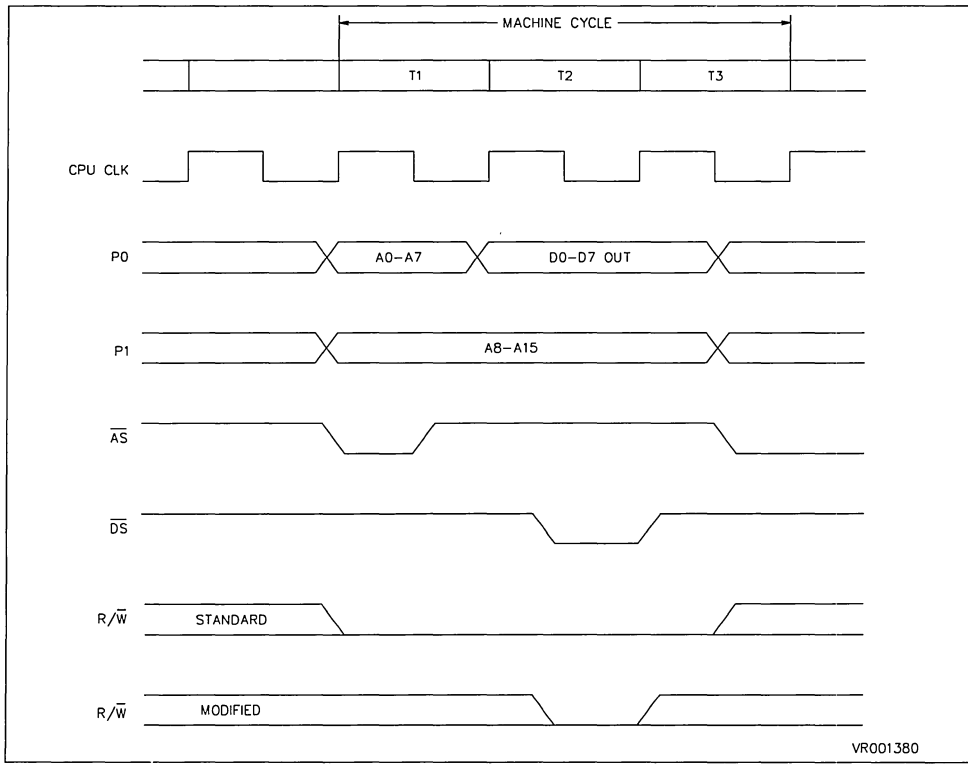
Note : The LST9 ST9 Incremental Linker supports the paging mechanism of the ST90R50 and is able to allocate program and data code into specific segments if required.

Figure 31. Bankswitch Output Timing Modification



BANKSWITCH LOGIC (Continued)

Figure 32. R/$\overline{W}$ Output Timing Modification



BUS CONTROL

Multi-processing or external program testing may be accomplished by disabling the I/O ports used for external memory addressing and the associated timing signals.

High Impedance Mode

The User may place the External Memory Interface (I/O Port 0, Port 1 and Port 6, Address Strobe, Data Strobe and Read/Write) into the high impedance state by setting the HIMP bit (MODER.0). External test equipment may then drive the memory lines for automatic test, external memory validation or programming. The ST9 will continue to execute internal programs, providing no external memory is addressed, allowing the execution of security routines without showing externally the addresses used.

Bus Request/Acknowledge

The External Memory Interface address ports and timing signals may be forced to their high impedance state by utilizing the $\overline{BUSREQ}$, Bus Request, and $\overline{BUSACK}$, Bus Acknowledge, signals available as Alternate Functions of two I/O pins. The signals, $\overline{BUSREQ}$ and $\overline{BUSACK}$, must be enabled by setting the BRQEN bit (MODER.1). Once enabled, a low level detected on the $\overline{BUSREQ}$ pin at the start of an internal machine cycle will cause the stretching of the CPUCLK, and $\overline{BUSACK}$ to go low indicating that the External Memory Interface is disabled. The $\overline{BUSREQ}$ pin is then continuously monitored, and when sampled high, the External Memory Interface pins are driven by the ST9 within two INTCLK cycles.

I/O PORTS

Summary of Function

For the ST90R50 84 pin package, only twelve pins have a Reserved function: V_{DD}(x2), V_{SS}(x2), $\overline{RESET}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, OSCIN, OSCOUT, the Analog to Digital Converter Voltage references. All other pins are available as Input/Output (I/O) for the User, grouped into Ports of 8 bits. These may be programmed to be Input, Output, Bidirectional or Alternate Function (Peripheral or Memory Interface), on a bit by bit basis, at any time. When programmed as an Input the pin may be set to TTL or CMOS input threshold levels, while, when programmed as Output, Push-Pull or Open Drain configuration may be selected. The Bidirectional mode sets the pin with a weak pull-up resistor to V_{DD} or to Open Drain, allowing bidirectional communication with external logic. The Alternate Function setting is predetermined for each pin as shown in the Pin Configuration Table.

The circuitry of the I/O port allows for several ST90R50 peripheral functions to address, as Alternate Functions, the same pin, for both input and output, the User selects which peripheral function is to be active by enabling its individual Input or Output function. This multi-function I/O capability of the ST90R50 allows for easy adaptation to external circuits. The options available for each bit are summarized in Table 8.

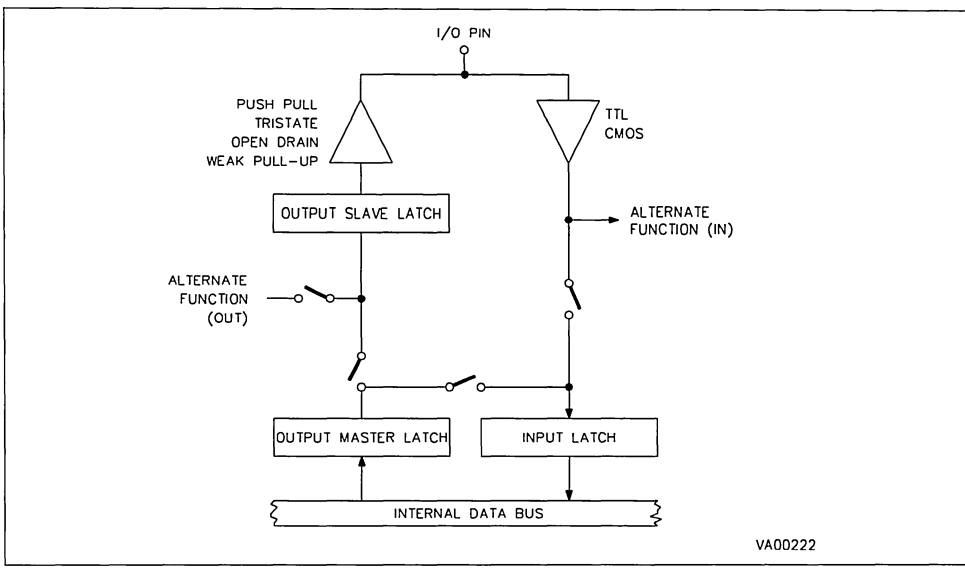
Table 8. I/O Setting Options

Input	TTL Thresholds
	CMOS Thresholds
Output	Open Drain
	Push Pull
Bidirectional	Open Drain
	Weak Pull-up
Alternate Function	Open Drain
	Push Pull

I/O Port Configuration

The configuration of each general I/O bit of the ST90R50 is set by the corresponding bits in three I/O Port control registers. These affect the status of the input and output buffers of the pin, and enable the Alternate function Outputs. Alternate Function inputs are always connected, and are used by enabling the function from within the configuration registers of the relevant peripheral function. The configuration of an I/O bit is shown in figure 33. Outputs follow a Master/Slave buffer, data is tran-

Figure 33. I/O Port Schematic



I/O PORTS (Continued)

ferred from the ST9 internal data bus at the beginning of the machine cycle, and, if enabled as output, is passed to the output latch at the end of the cycle. This synchronization allows for the Bidirectional use of the pin without potential conflicts.

Configuration Registers.

Three registers are used to allow the setting of each pin, generically PxC2R, PxC1R, PxC0R, where x relates to the 8 bit I/O port in which the bit is present. The setting of the corresponding bit in each register to achieve the desired functionality of the I/O pin is shown in Table 9.

The effect of the configuration settings of Table 9 on the I/O ports structure is shown in Figures 34 to 37.

I/O Register Map

The Data Registers which correspond to the pin status (after configuration) of I/O port 0 to 5, are found in Group E of the Register File, for immediate access at all times, while the configuration registers and the Data Registers for Additional Ports are found within I/O pages (Group F) 2, 3 and 43 (2Bh).

Table 9. Port Configuration Status Bits

PxC2n	0	1	0	1	0	1	0	1
PxC1n	0	0	1	1	0	0	1	1
PxC0n	0	0	0	0	1	1	1	1
Pxn Configuration	BID	BID	OUT	OUT	IN	IN	AF	AF
Pxn Output	WP	OD	PP	OD	HI	HI	PP	OD
Pxn Input	TTL	TTL	TTL	TTL	CMOS	TTL	TTL	TTL

Legend :
x = Port
n = Bit
BID = Bidirectional
OUT = Output
IN = Input
AF = Alternate Function
WP = Weak Pull-up
OD = Open Drain
PP = Push Pull
HI = High Impedance

Figure 34. I/O Port Input Configuration

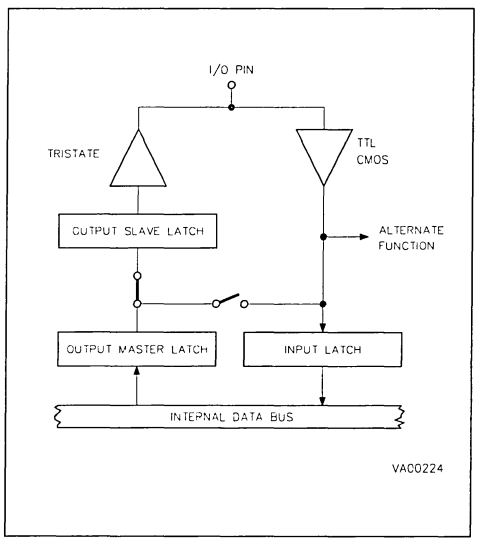
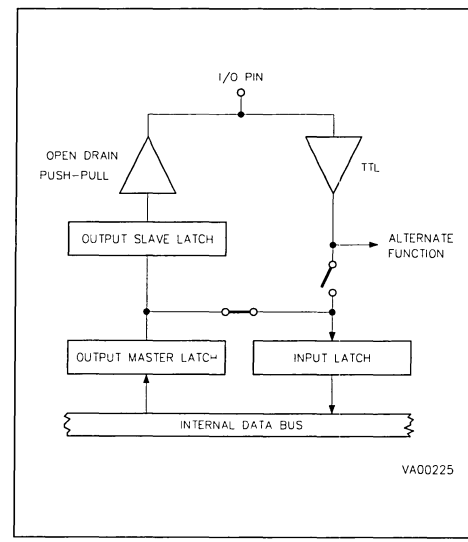


Figure 35. I/O Port Output Configuration



I/O PORTS (Continued)

Figure 36. I/O Port Bidirectional Configuration

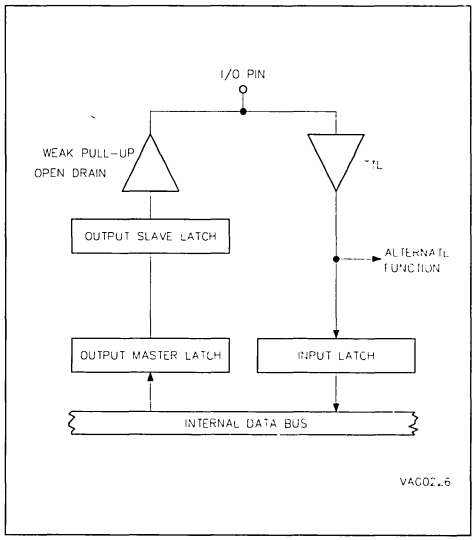


Figure 37. I/O Port Alternate Function Config.

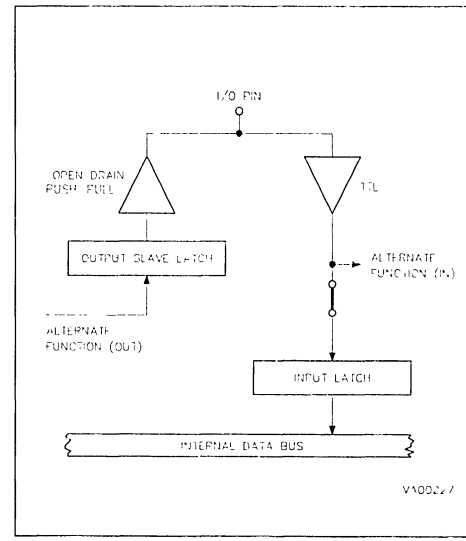


Figure 38. I/O Register Maps

GROUP E			GROUP F		PAGE		
DEC	HEX		DEC	HEX	02	03	43
			R255	RFF	RESERVED	P7D	P9D
			R254	RFE	P3C2	P7C2	P9C2
			R253	RFD	P3C1	P7C1	P9C1
			R252	RFC	P3C0	P7C0	P9C0
			R251	RFB	RESERVED	RESERVED	P8D
			R250	RFA	P2C2	RESERVED	P8C2
			R249	RF9	P2C1	RESERVED	P8C1
			R248	RF8	P2C0	RESERVED	P8C0
			R247	RF7	RESERVED	HDC5	RESERVED
			R246	RF6	P1C2	P5C2	RESERVED
R229	RE5	P5D	R245	RF5	P1C1	P5C1	RESERVED
R228	RE4	P4D	R244	RF4	P1C0	P5C0	RESERVED
R227	RE3	P3D	R243	RF3	RESERVED	RESERVED	RESERVED
R226	RE2	P2D	R242	RF2	P0C2	P4C2	RESERVED
R225	RE1	P1D	R241	RF1	P0C1	P4C1	RESERVED
R224	RE0	P0D	R240	RF0	P0C0	P4C0	RESERVED

I/O PORTS (Continued)

Handshake and DMA

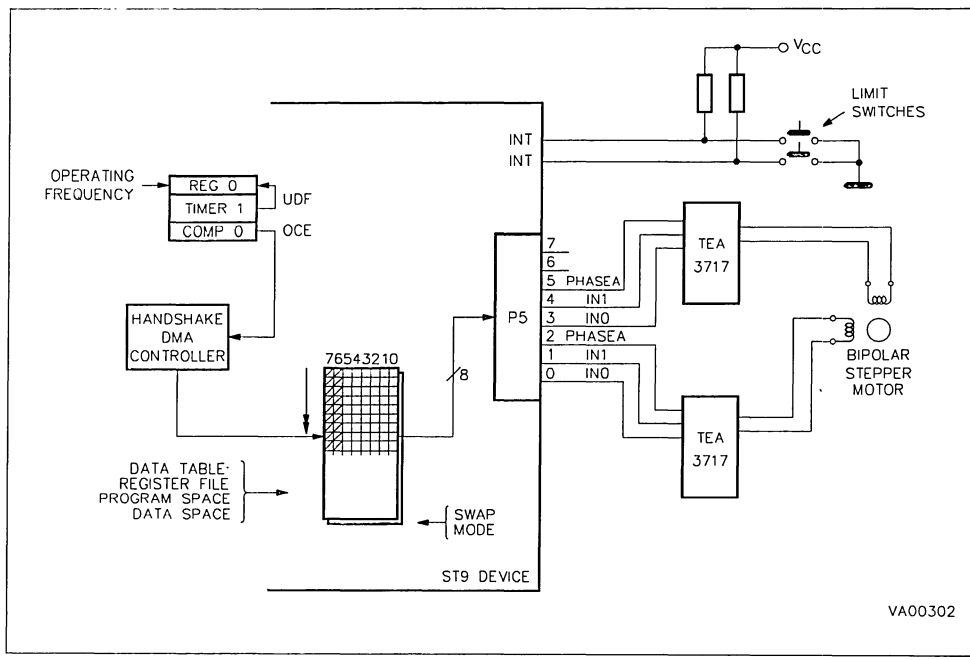
I/O Ports 4 and 5 of the ST90R50 are able to support a parallel interface with handshake capability. This allows one, two or four wire interconnecting handshake signals and facilitates very fast parallel transfer of data for input and output, or for the interconnection of peripheral devices requiring strobe signals for synchronization. Table 10 shows the available options for input and output status and strobe signals available as Alternate Functions of I/O port bits (see Pin Configuration). The Handshake configuration is set within the Handshake Control Register (HDC*n*R) for the relevant I/O port *n*.

Data transfer through a parallel I/O port with handshake can also be triggered through a DMA channel. Timing is generated by the ST90R50 TIMER ON-CHIP EVENT strobe signal (see the TIMER section for information on generating these signals), which causes the programmed transfer of data to or from the memory source which can be Register File, Program space memory or Data space memory. An example of application of this technique is shown in figure 39, a complex stepper motor timing sequence automatically being transferred from a table in the Register File (or memory spaces) to the stepper motor drivers. After initialization, this operation is transparent until the task (complex microstepping) is completed.

Table 10. Handshake Control Signal Options

Mode	Handshake Lines	Names
Input to Port	1	WRRDY
	2	$\overline{\text{WRSTB}}$ WRRDY
Output from Port	1	RDRDY
	2	$\overline{\text{RDSTB}}$ RDRDY
Bidirectional	4	$\overline{\text{WRSTB}}$ WRRDY $\overline{\text{RDSTB}}$ RDRDY

Figure 39. Handshake + DMA Used for Stepper Motor Driving



TIMER/WATCHDOG

A 16 bit down-counter, complete with 8 bit prescaler, is integrated into the ST90R50 core. This is able to operate both as a general purpose timer with associated input and output pins for timing functions, and also as a Watchdog Timer offering a security against possible processor malfunctions due to external events.

Timer Modes

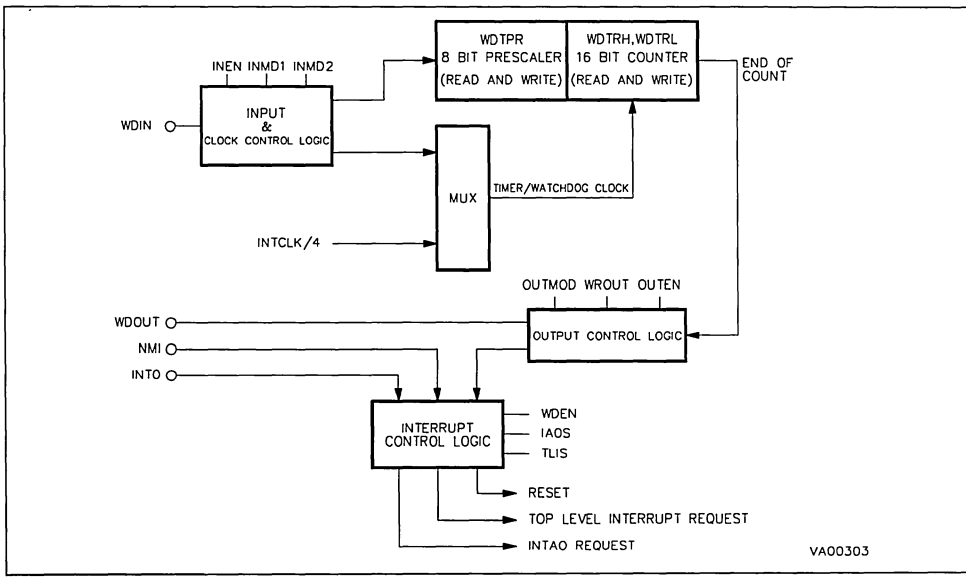
When operating as a Timer, with a timing resolution from 333ns to 5.59s (INTCLK = 12MHz), an input pin (WDIN) and output pin (WDOUT) may be selected as the Alternate Functions of two I/O pins. When WDIN is enabled by the User by setting INEN high (WDTCR.3) and the Alternate Function is set, 4 operating modes are available: The WDIN input may be programmed to act as an event counter input, with high to low transitions causing the counter to decrement (the time duration between the falling edges of the input clock must be at least 333ns, allowing a maximum input frequency of 3MHz). It may also be used for pulse width measurement by being selected as a counter clock gate signal (prescaler to the counter being driven by INTCLK/4), counting being enabled when WDIN is at a high level. Trigger and Re-trigger modes cause a reload of the timer User preset values (providing STSP, WDTCR.7 is active) for a high to low transition on WDIN at any time (Re-trigger mode) or when the counter is at the end of count (Trigger mode). The counter decrements at a rate driven by INTCLK/4.

The WDOUT pin, when set as the Alternate Function, is enabled by OUTEN high (WDTCR.0), and may either toggle the state of the I/O bit (frequency generation, OUTMD = "0", WDTCR.2) or pass the state of the WROUT bit to the output allowing PWM generation (OUTMD = "1") at the end of count (timer value = 0) condition.

Watchdog Mode

The timer functions may be disabled, and the Timer configured for a Watchdog operation by re-setting WDEN (WCR.6) to zero. Once the Watchdog has been selected it CANNOT be set back into the standard timer mode until the next Hardware Reset cycle. The User should set the watchdog timer prescaler and timer reload value before enabling the Watchdog mode. The Watchdog Timer must then be retriggered, causing the reloading of the timer value, by the operation of writing of the byte sequence 0AAh, 055h to the WDTLR register. If this is not done before the Watchdog counts to zero, the Watchdog Timeout condition occurs. This causes a Hardware Reset of the ST90R50. The Watchdog reset signal is not output on the external Reset pin.

Figure 40. Timer/Watchdog Block Diagram



TIMER/WATCHDOG (Continued)

Timer/Watchdog Interrupts

The Timer/Watchdog may provide several levels of interrupts selectable by the User. The Timer mode offers two interrupt sources, triggered on the timer value reaching 0, either a prioritized level (by taking the Interrupt priority channel from the External Interrupt INTA0) or by a top level, non-maskable interrupt (taking the external NMI input channel). The interrupt channels are multiplexed from the alternative source according to the status of the IAOS (EIVR.1) and TLIS (EIVR.2) bits as shown in figure 42. Please refer to the ST9 Technical Manual for further details on changing the interrupt sources of the Timer/Watchdog. When the Watchdog mode is set (WDEN = "0"), the timer value equal to 0 event generates a Hardware reset of the ST90R50. The Timer/Watchdog control registers are located within Page 0 of the Paged I/O register group.

Figure 42. Timer/Watchdog Interrupt Sources

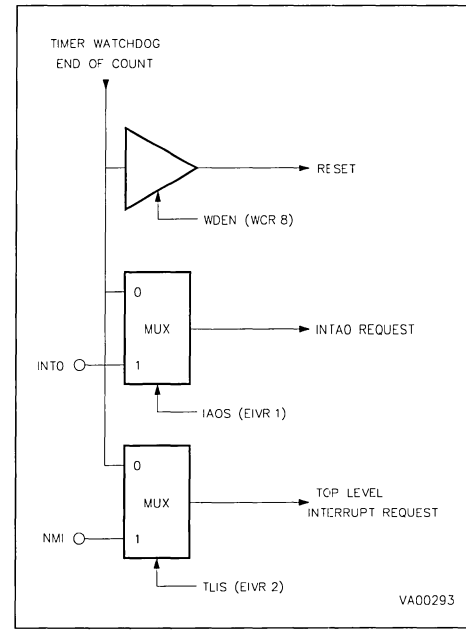
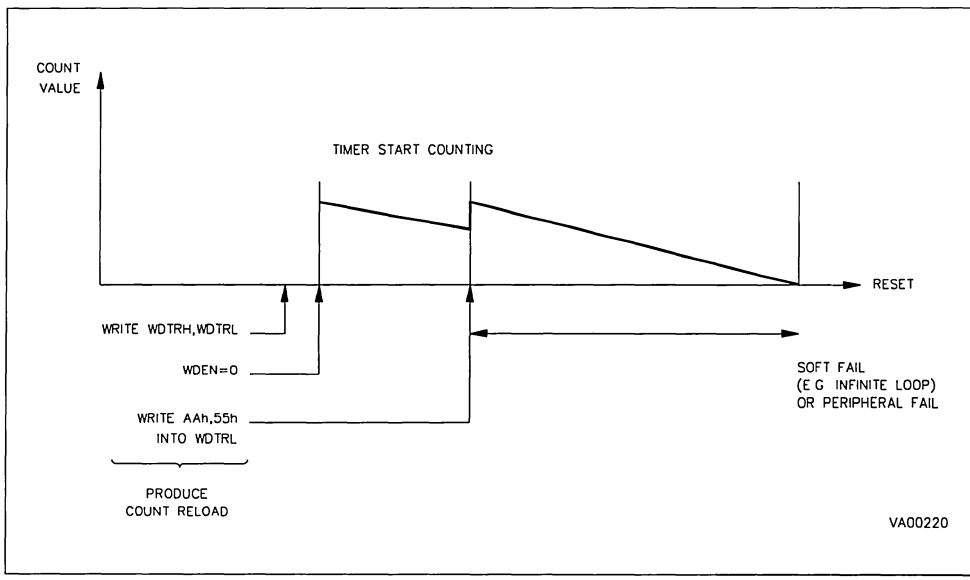


Figure 41. Timer/Watchdog in Watchdog Mode



MULTIFUNCTION TIMER

The ST90R50 includes three identical 16 bit Multifunction Timers (MFT) in addition to the TIMER/WATCHDOG. The following description applies to Timer 0, Timer 1 and Timer 3.

Each timer is a 16 bit Up/Down counter, driven by the output of an 8 bit prescaler which may be driven by INTCLK/3 (giving a minimum timing resolution of 250ns at INTCLK = 12 MHz) or by an external source. This timer is supported by two 16 bit Comparison Registers for generating timed functions and two 16 bit Capture/Load Registers for timing and variable timebase functions. These features coupled with 2 input pins (TxINA and TxINB) and 2 output pins (TxOUTA and TxOUTB, where x = 0 or 1), available as Alternate Functions, giving the timer 13 operating modes for virtually all required timing functions.

MFT Operating Modes

The operating modes are selected by the programming of the Timer Control Register (TCR Timer x) and the Timer Mode Register (TMR) as follows:

One-Shot Mode. The counter stops at the End Of Count Condition (up or down count).

Continuous Mode. At End Of Count the timer is reloaded from a Load Register.

Trigger Mode. A Trigger causes reload from a load register only if the Timer is at End of Count.

RETrigger Mode. A Trigger causes reload from a load register at any time.

Gate Mode. Counting is performed only when the external gate input (TxINA or TxINB) is active (logical 0).

Capture Mode. A Trigger causes the timer value to be latched into the selected Capture register.

Up/Down Mode. A Trigger causes a count up or down, or a change in counting direction.

Free-Running Mode. Up or Down counting is performed to the full range with no action at End of Count. This is used in Bicapture and Capture Modes.

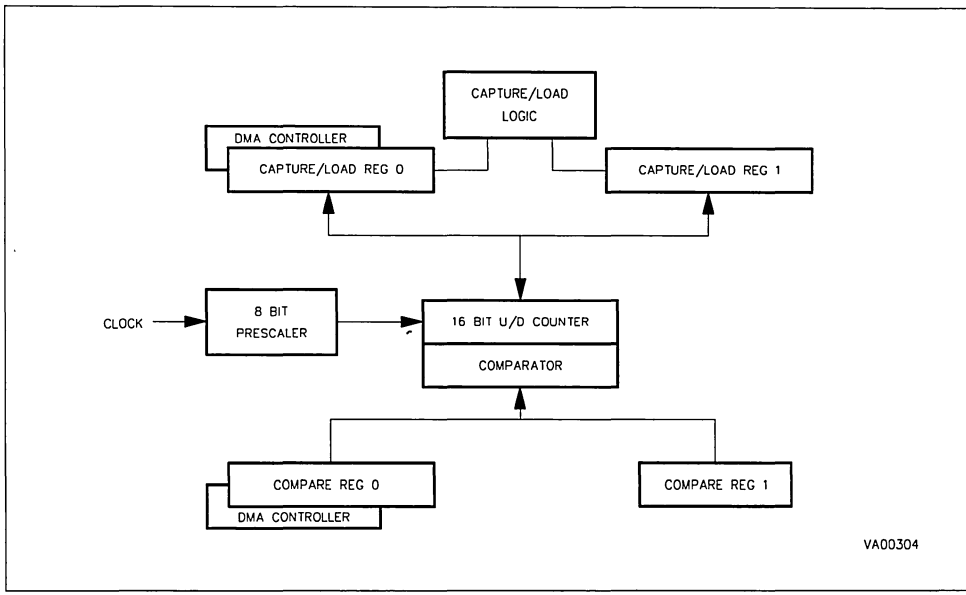
Monitor Mode. One Capture register follows the contents of the timer.

Autoclear Mode. The timer is reset to 0000h or FFFFh (up or down count respectively) on a trigger. This gives delta time measurement or free running with a modulo of less than 2^{16}.

Biload Mode. The counter is reloaded on an End Of Count condition alternately from the two Load Registers. (PWM output).

BICapture Mode. A Trigger causes the current timer value to be transferred alternately to the two Capture registers. (Pulse width measurement).

Figure 43. Multifunction Timer Block Diagram



MULTIFUNCTION TIMER (Continued)

Parallel Mode. The prescaler output of Timer 0 is internally connected to the input of the prescaler of Timer 1, if this is then set to 00h (= divide by 1), then the two timers may be run in parallel.

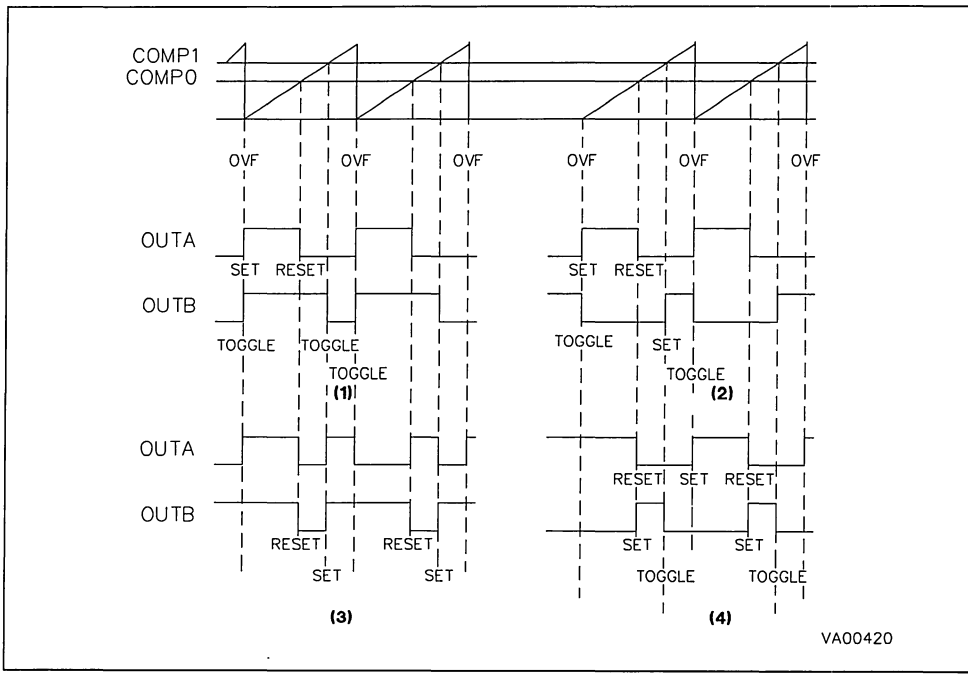
The trigger events may be either caused by software, or an action on the two input pins which may be programmed to respond to rising, falling or both edges of the input. The input modes are selected in the Input Control Register (ICR) as shown in Table 11. This includes the Autodiscriminator mode, which causes the timer to count up or down depending on the phase between the two input edges, such as the signals generated by optical encoders.

The two output pins (available as Alternate Functions) may be programmed through the Output Control Registers OACR and OBCR to be modified (Set, Reset, Toggle or No Operation) on each of Overflow/Underflow (OVF/UNF), Compare on CMP0 valid (CM0), or Compare on CMP1 (COMP1) valid events. This allows repetitive signals such as PWM drive to be output with minimum CPU overhead. Fig 44 shows some typical waveforms available from these signals.

Table 11. Input Pin Function Settings

Input Control Register IN3-IN0 bits	TxINA Input Function	TxINB Input Function
0000	I/O	I/O
0001	I/O	Trigger
0010	Gate	I/O
0011	Gate	Trigger
0100	I/O	Ext.clock
0101	Trigger	I/O
0110	Gate	Ext.clock
0111	Trigger	Trigger
1000	Clock Up	Clock Down
1001	Up/Down	Ext.clock
1010	Trigger Up	Trigger Down
1011	Up/Down	I/O
1100	Autodiscr.	Autodiscr.
1101	Trigger	Ext.clock
1110	Ext.clock	Trigger
1111	Trigger	Gate

Figure 44. Example Output Waveforms



MULTIFUNCTION TIMER (Continued)

The Overflow/Underflow event and the Compare 0 event may also be programmed to give On-chip Event timing signals to trigger other peripheral operations on the ST90R50. These are as shown in Table 12.

Table 12. ST90R50 On-Chip Event Settings

MFT0	Handshake Trigger Port 4
MFT1	Handshake Trigger Port 5
MFT3	A/D Conversion Trigger

The TxOUTA and TxINA lines for each timer may be connected internally, by setting of the SCx bits of the I/O Connection Register (IOCR).

The Multifunction Timers are enabled for counting by the Counter Enable bit (CEN, TCR.7) of the respective timer unit. When CEN is low, both prescaler and timer are halted. CEN is logically ANDed with the Global Counter Enable bit (GCEN, CICR.7), so that all timers may be started in synchronism, i.e. when the timers are set into Parallel mode, this allows initialization of the Timers before triggering at the same instant.

MFT Interrupts

Each Multifunction Timer can generate interrupt requests from 5 different interrupt sources which are grouped into 3 independent groups. The Interrupt Vector has the source of the interrupt group encoded by hardware into the least significant 3 bits of the vector. This allows the programming of the base address to an 8 byte block within the interrupt vector area of the Program Space. The groups and respective addresses are shown in Table 13.

Table 13. MFT Interrupt Vectors

Interrupt Source	Vector Address
COMP0 COMP1	xxxx x110
CAPT0 CAPT1	xxxx x100
Overflow/Underflow	xxxx x000

Each source may be independently masked, in addition all Timer interrupts may be disabled by the Global Timer Interrupt enable (GTIEN, IDMR.7) control bit. If a Timer interrupt on Compare 0 or Capture 0 does not have its corresponding pending bit reset before the next interrupt, then an overrun condition occurs. This condition is flagged in two dedicated overrun bits in the Timer FLAGS register.

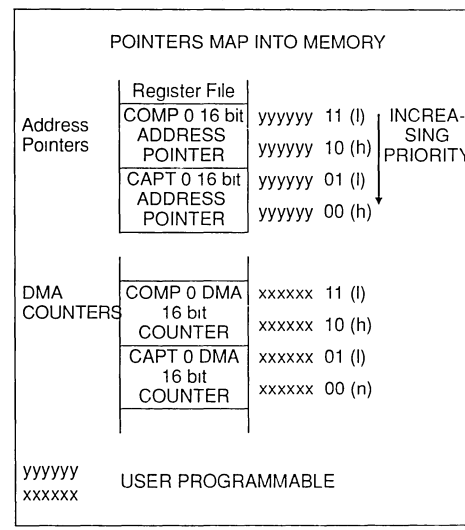
MFT DMA Channels

Two independent DMA channels are present within each MFT, associated to the Compare 0 and Capture 0 sources. This allows 16 bit DMA transactions from Register File/Memory to COMP0 registers, and from CAPT0 registers to Register File/Memory. The DMA channels allow the capture of external event timings in memory allowing off-line analysis, and creating of variable pulse width signal trains, as required by the drive of Triacs in certain modes.

The two interrupt mask sources are independently masked by two DMA mask bits, mapped in the IDMR register. The End of Block (EOB) procedures are as described in the INTERRUPT/DMA section.

The DMA counter and address pointer registers share the most significant User-programmable 6 bits for both DMA channels (COMP 0 and CAPT 0), thus the mapping of the counter and address registers use automatic offsets from the base address. The actual mapping changes dependent on whether the Register File or Memory is addressed for the transfer. The offsets are shown in Table 14.

Table 14-1. MFT DMA Address and Counter Registers for Memory DMA Transfers



MULTIFUNCTION TIMER (Continued)

Table 14-2. MFT DMA Address and Counter Registers for Register File DMA Transfers

POINTERS FOR REGISTER FILE DMA			
8 Bit COUNTER	xxxxxx	11	COMPARE 0
8 bit ADDR POINTER	xxxxxx	10	
8 bit COUNTER	xxxxxx	01	CAPTURE 0
8 bit ADDR. POINTER	xxxxxx	00	
xxxxxx	USER PROGRAMMABLE		

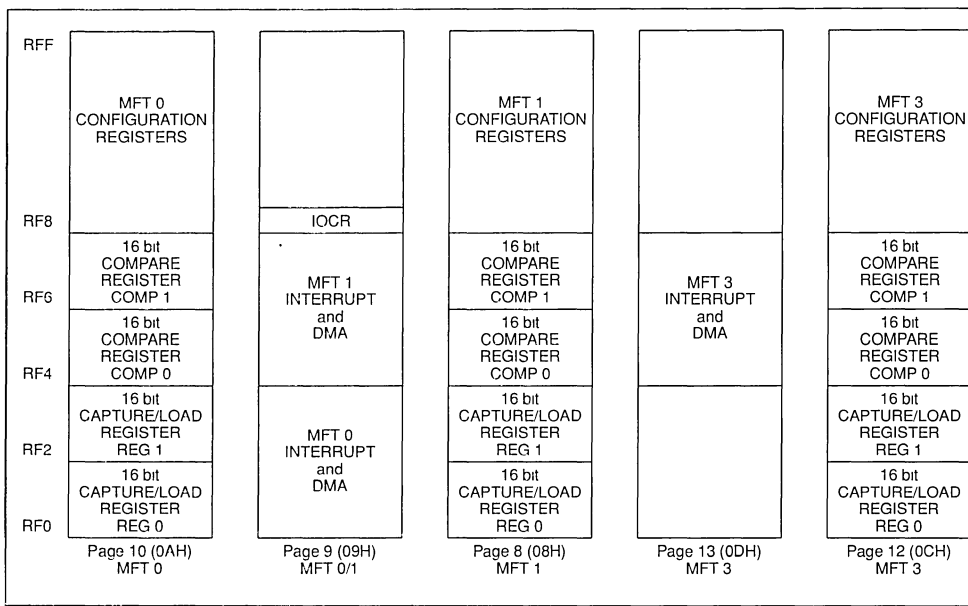
After the transfer of the complete block of data to/from the MFT, the count registers reach the zero value and an end of block interrupt occurs so that the ST9 may process the new data. In many cases, the time taken to reload the data tables and to re-trigger the DMA action causes speed limitations, especially in those applications requiring a continuous high speed data flow, because of the time consumed by the restore routine. An additional DMA function, the SWAP mode, overcomes this limitation. This is enabled by the setting of the SWEN (IDCR.3) bit. This causes hardware generated signals to replace the User address bit 2 of both the address and counter pointers. The address and counter registers are thus duplicated at an offset of 4 registers. At the End Of Block condition, the EOB interrupt is generated to signal the end of DMA, and the state of pointer address bit 2 toggles state automatically and the new address and count values are used. Thus the ST9 can safely process the previous block of data while the new block is being transferred. This will continue until the SWAP mode is disabled.

A software protection scheme is implemented to prevent non-updated pointer registers from being used if a second EOB interrupt arrives during the servicing of the first. This mechanism locks the state of the DMA mask bit to prevent further transfers from taking place. The User should check for this condition in the EOB routine to ensure that all the DMA transfers are properly serviced.

The control Registers of each MFT occupy 20 registers within the I/O paged area. These are mapped as shown in Figure 45.

In addition the MFT is able to trigger byte DMA transfers in both directions through an I/O port with Handshake (see I/O Handshake and DMA).

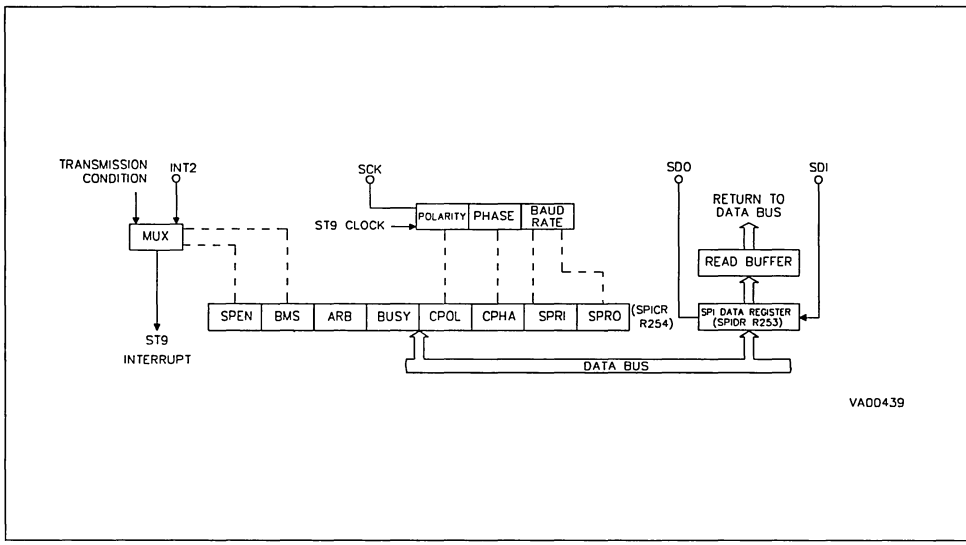
Figure 45. Multifunction Timer Page Maps



SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) is integrated into the Core module of the ST9 and provides a general purpose shift register based peripheral allowing synchronous serial I/O, with special modes allowing compatibility with I^2C-bus and IM-bus Communication standards in addition to the standard serial bus protocol. The SPI uses 3 lines comprising Serial Data Out (SDO), Serial Data In (SDI) and the Synchronous Serial Clock (SCK) which are available as Alternate Functions of I/O pins. Additional I/O pins may act as device selects or IM-bus address ident signals. The functional diagram of the SPI is shown in figure 46.

Figure 46. SPI Functional Diagram



The SPI, when enabled (SPEN, SPICR.7, high), receives input data from the ST9 internal data bus into the SPIDR, and originates the SCK to shift the data serially through SDO (Most Significant bit first) to the slave device which responds by sending data to the master device via the SDI pin. This implies full duplex transmission with both data-out and data-in synchronized with the same clock signal. Thus the byte transmitted is replaced by the byte received, eliminating the need to separate "Tx Empty" and "Rx full" status bits. After the 8 clock cycles have been concluded, the received data in SPIDR is parallel transferred to the read buffer and data becomes available for the ST90R50 during the next read cycle of SPIDR. The BUSY bit (SPICR.4) is set when transmission is in progress, this allows the User to monitor the status of the SPI by polling of this bit.

The SPI can operate only in master mode, i.e. the clock is always generated by the ST90R50, however the SCK polarity and phase can be programmed to suit all peripheral requirements (figure 47). This, together with the 4 programmable bit rates (divided from the INTCLK, Table 15), provide the large flexibility in handling different protocols.

SERIAL PERIPHERAL INTERFACE (Continued)

Figure 47. SPI Data and Clock Timing

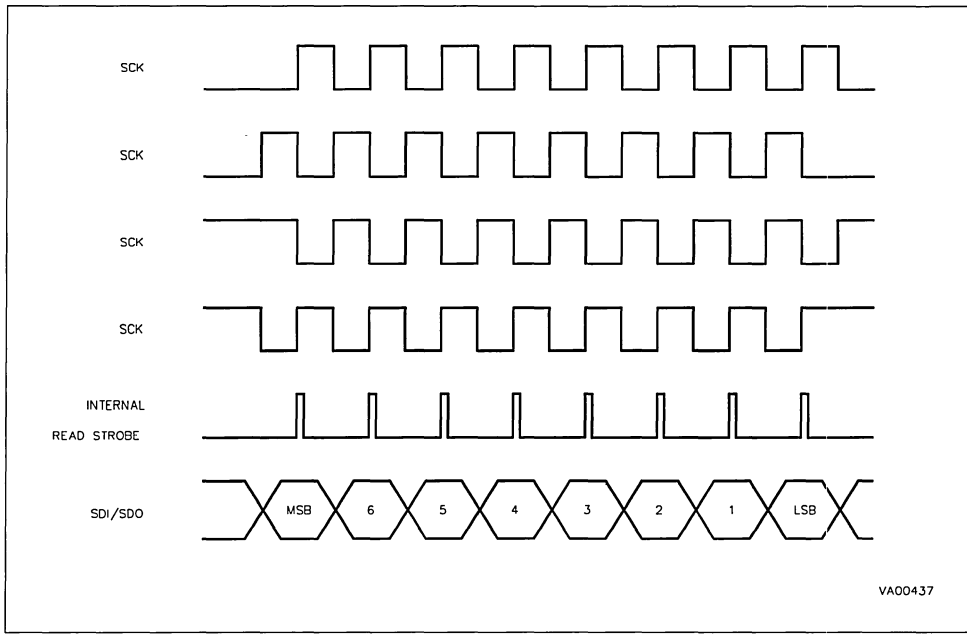


Table 15. SPI Rate Selection

SPR1	SPR0	Clock Divider	SCK Frequency (INTCLK = 12MHz)
0	0	8	1500KHz (T = 0.67µs)
0	1	16	750KHz (T = 1.33µs)
1	0	12	93.50KHz (T = 10.66µs)
1	1	256	46.87KHz (T = 21.33µs)

I^2C-bus COMPATIBILITY

The SPI includes additional circuitry to enable the use of external I^2C-bus peripherals. The I^2C-bus mode is a 2 wire bus while the SPI operates with 3 wires, however wire-ANDing SDO and SDI gives the required signalling, while setting the BMS bit causes the enabling of the special I^2C-bus features: Clock Slowdown by external devices and Arbitration Lost detection. This mode also affects the Interrupt sources as shown in the next section.

SPI Interrupts

The SPI, when enabled, uses the INT2 external interrupt channel source, using the priority selected for INT2 within the External Interrupt Priority registers. The INT2 mask bit should be set and INT2 pending bit reset before enabling the SPI through SPEN. The BMS (SPICR.6) and SPEN bits select the SPI internal interrupt source as shown in Table 6.

Table 16. SPI Interrupt Sources

SPEN	BMS	Interrupt Source
0	0	External channel INT2
0	1	S-BUS/I^2C start or stop condition
1	X	End of one byte transmission

SPI Registers

The two registers controlling the SPI are located in I/O page 0, the Data Register, SPIDR, at R253 and the control register, SPICR, at R254.

SERIAL COMMUNICATIONS INTERFACE

Function

The two Serial Communications Interfaces (SCIs) of the ST90R50 offers a means of full-duplex serial data transfer to a wide range of external equipment. Each has a fully programmable character format control for asynchronous and byte synchronous serial I/O, an integral Baud Rate Generator, giving a maximum baud rate of 375K Baud in Asynchronous mode (Internal Clock), and two DMA channels for transparent transmission and reception of characters. Support is also present in hardware for Line Break Detection and generation, character search, network interfacing with 9th bit Address logic, and Local Loop Back and Auto echo modes for Self- Test. The control registers for an SCI exist within one I/O page within the I/O page group.

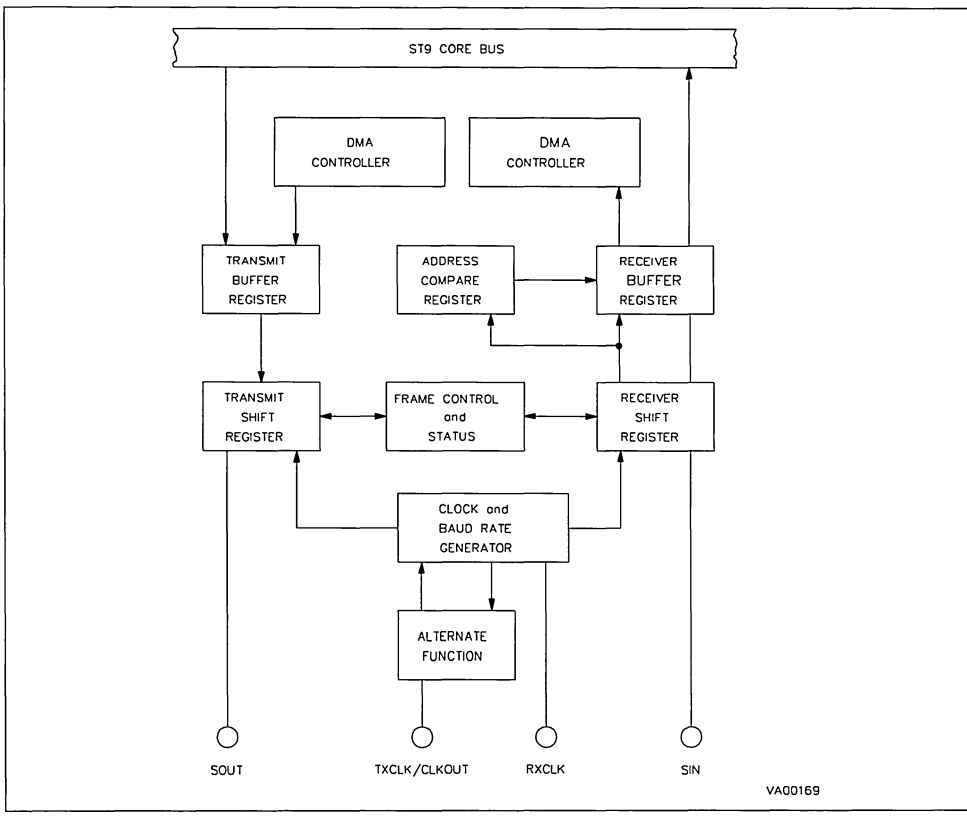
Character Formats

When used for asynchronous character transmission and reception, the character format may be changed (through the Character Control Register CHCR) to suit external equipment requirements. This is summarized in figure 49.

The baud rate clock for asynchronous mode should be set to the ÷16 Mode and the frequency of the clock input (from an external source or the internal baud-rate generator output) set to suit this.

This format control is also available for the byte synchronous mode (Clock divider set to ÷1), when the data and clock are output in synchronism, the data being sampled once per clock period (figure

Figure 48. SCI Functional Block Diagram



SERIAL COMMUNICATION INTERFACE
(Continued)

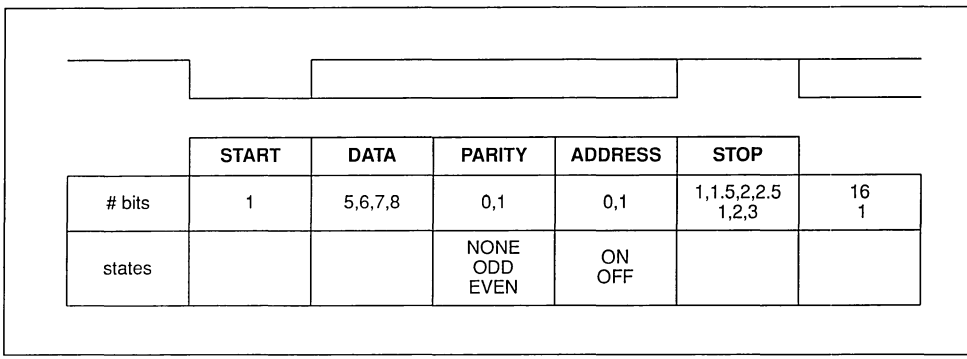
50). For a second synchronous mode, CLKOUT is activated only for the data section of the word (figure 51) on serial data output, and input data is latched on the rising edge of the external synchronised clock input on the RXCLK pin. This mode may be used to access external synchronous peripherals.

The Address bit/D9 is optional and may be added to any word format, it is commonly used in network or machine control applications. When enabled (AB, CHCR.4 = "1"), an address or ninth data bit can be added to a transmitted word by setting the Set Address bit (SA, IDPR.5). This is then appended to the next word entered into the (empty) Transmitter Buffer Register and then cleared by hardware. On character input an Address Bit set can indicate that the data preceding the bit is an address which may be compared in hardware with the value in the Address Compare Register (ACR) to generate an Address Match interrupt when equal.

The Address bit and Address Comparison Register can also be combined to generate an Address Interrupt in 4 modes to suit different protocols, based upon the status of the Address Mode Enable bit (AMEN, IDPR.7) and the Address Mode bit (AM, CHCR.7) as shown in Table 17.

The character match Address Interrupt mode may be used as a powerful character search mode, giving an interrupt on reception of a predetermined

Figure 49. SCI Character Format



	START	DATA	PARITY	ADDRESS	STOP	
# bits	1	5,6,7,8	0,1	0,1	1,1.5,2,2.5 1,2,3	16 1
states			NONE ODD EVEN	ON OFF		

Figure 50. Byte Synchronous Output

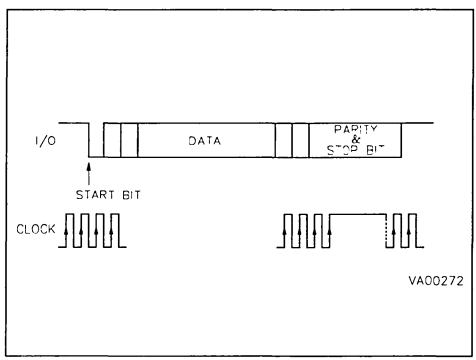
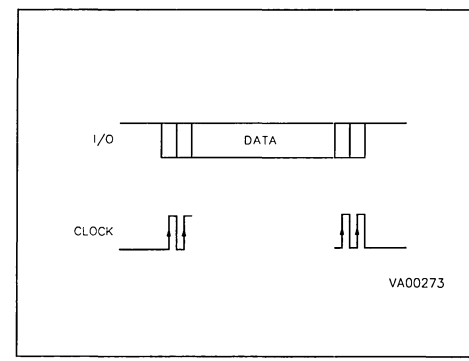


Figure 51. Serial Expansion Mode



SERIAL COMMUNICATION INTERFACE (Continued)

Table 17. Address Interrupt Modes

If 9th Data Bit = 1
If Character Match
If Character Match and 9th Data Bit = 1
If Character Match on Word Immediately Following Break

character e.g. Carriage Return or End of Block codes.

The Line Break condition is fully supported for both transmission and detection. Line Break is sent by setting the SET_BREAK bit (SB, IDPR.6). This causes the transmitter output to be held low (after all buffered data has been transmitted) for a minimum of one complete word length and until the SB bit is Reset.

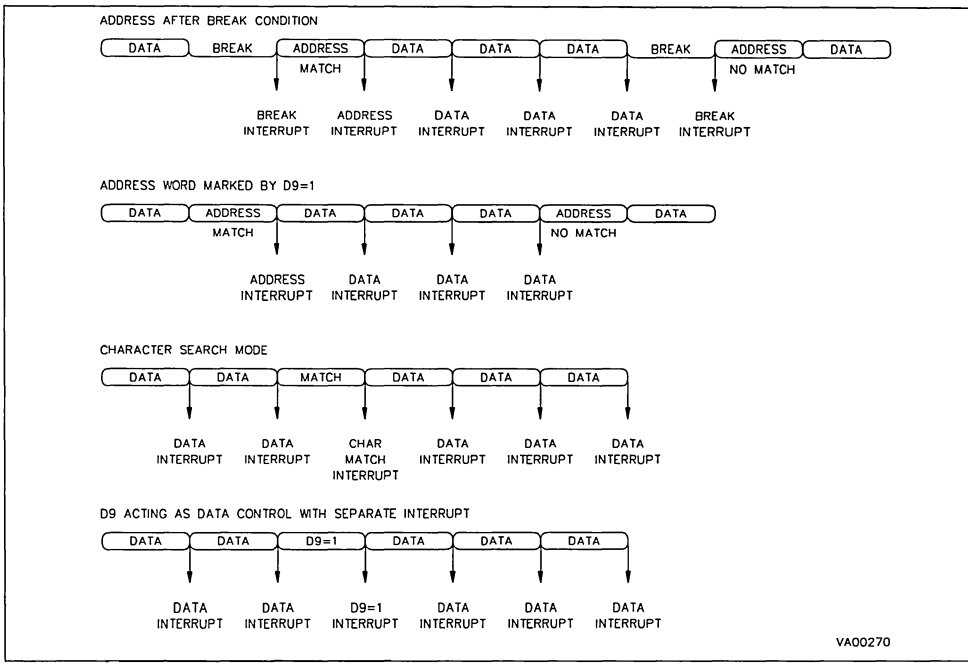
SCI Interrupts

Each SCI is able to generate interrupts from multiple sources. Receive interrupts include data pending, receive errors (overrun, framing and parity), address or break pending and transmit interrupts are software selectable for either the Transmit Holding Register Empty (HSN, IMR.7 = "1") or for the Transmit Shift Register Empty (HSN = "0"). Interrupt sources are indicated by the Interrupt pending bits, shown in Table 18. These bits

Table 18. SCI Interrupt Vector

Interrupt Source	Vector Address
Transmitter Buffer or Shift Register Empty/Transmit DMA end of Block	xxx x110
Received Read/ Receive DMA end of Block	xxxx x100
Break Detector Address Word Match	xxxx x001
Receiver Error	xxxx x000

Figure 52. SCI Interrupt Typical Usage



SERIAL COMMUNICATION INTERFACE (Continued)

should be reset by the User during the Interrupt Service routine.

When DMA is active the Receive Data Pending bit (RXDP, ISR.2), and the Transmit status bit interrupt sources are replaced by the DMA End Of Block Interrupt sources for transmit and receive, respectively.

Typical Usage of the Interrupts provided by the SCI are show in figure 52.

Table 19. SCI Interrupt Internal Priority

Receive DMA Request	Highest Priority
Transmit DMA Request	
Receive Interrupt	
Transmit Interrupt	Lowest Priority

The SCI interrupts have an internal priority structure (Table 19) in order to resolve simultaneous events.

The four major levels of interrupt are encoded in hardware to provide two bits of the interrupt vector register, allowing the position of the block of pointer vectors to be resolved to a block size of 8 bytes.

SCI DMA

Two DMA channels are associated with each SCI, for transmit and for receive. These follow the register scheme as described in the DMA Section. It should be noted that, after initializing the DMA counter and pointer registers and enabling DMA, data transmission is triggered by a character written into the Transmit Holding register. The DMA End Of Block Interrupts generated on completion of the DMA transfer take the place of the normal transmit and receive character interrupt vectors.

SCI Clock Generation

The communication bit frequency of the SCI transmitter and receiver sections can be provided from the integral Baud Rate Generator (allowing a maximum asynchronous bit rate of 350k Baud) or from external sources (maximum bit rate 175k Baud). This clock is divided by 16 for asynchronous mode (CD, CCR.3, = "0"), or divided by 1 for synchronous modes (CD = "1").

External Clock Sources.

The External Clock input pin TXCLK may be programmed in Alternate function by bits TXCLK (CCR.7) and OCLK (CCR.6) to be: the transmit clock input (respecting the ÷16 and ÷1 timing requirements), to act as the output of the Baud Rate Generator (allowing an external divider circuit to provide the receive clock for split rate transmit and receive e.g. 1200/75 baud), or to be CLKOUT, the clock output for the synchronous mode. Receive clock input via RXCLK Alternate function is enabled by the XRX bit CCR.5, this input should be set according to the setting of the CD bit.

Baud Rate Generator.

The integral Baud Rate Generator is a 16 bit divide by n circuit of the Internal Clock INTCLK. Thus INTCLK should be chosen to provide a suitable frequency for division by the Baud Rate Generator to give the required transmit and receive bit rates. Suitable INTCLK frequencies and the divider values for standard Baud rates are shown in Table 20.

The act of writing to either of the two registers comprising the 16 bit divider causes a reset of the SCI, allowing initialization of the SCI settings before the writing of the other Baud Rate Generator register.

Self Test

Testing of the communications channel may be performed using the facilities of the SCI. Auto Echo mode (SCI SOUT disconnected, SIN pin internally connected to SOUT pin) and Loopback mode (SCI transmitter and receiver sections disconnected

SERIAL COMMUNICATION INTERFACE (Continued)

Table 20. SCI Baud Rate Generator Divider Values

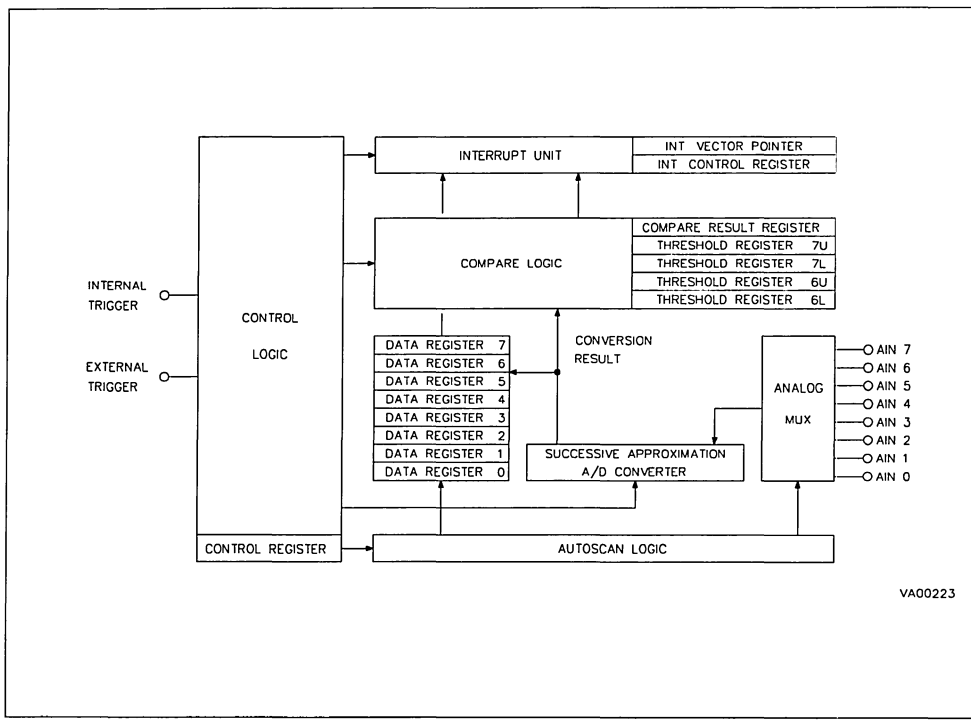
INTCLK: 7680.000 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	9600	2580	50.00	0.80000	0.0000%
75.00	16 X	1.20000	6400	1900	75.00	1.20000	0.0000%
110.00	16 X	1.76000	4364	110C	109.99	1.75985	0.0083%
300.00	16 X	4.80000	1600	0640	300.00	4.80000	0.0000%
600.00	16 X	9.60000	800	0320	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	400	0190	1200.00	19.20000	0.0000%
2400.00	16 X	38.40000	200	00C8	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	100	0064	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	50	0032	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	25	0019	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	13	000D	36923.08	590.76923	3.8462%
76800.00	16 X	1228.80000	6	0006	80000.00	1280.00000	4.1667%
INTCLK: 11059.20 KHz							
Baud Rate	Clock Factor	Desired Freq (kHz)	Divisor		Actual Baud Rate	Actual Freq (kHz)	Deviation
			Dec	Hex			
50.00	16 X	0.80000	13824	3600	50.00	0.80000	0.0000%
75.00	16 X	1.20000	9216	2400	75.00	1.20000	0.0000%
110.00	16 X	1.76000	6284	188C	109.99	1.75990	0.0058%
300.00	16 X	4.80000	2304	0900	300.00	4.80000	0.0000%
600 00	16 X	9.60000	1152	0480	600.00	9.60000	0.0000%
1200.00	16 X	19.20000	576	0240	1200.00	19.20000	0.0000%
2400.00	16 X	38 40000	288	0120	2400.00	38.40000	0.0000%
4800.00	16 X	76.80000	144	0090	4800.00	76.80000	0.0000%
9600.00	16 X	153.60000	72	0048	9600.00	153.60000	0.0000%
19200.00	16 X	307.20000	36	0024	19200.00	307.20000	0.0000%
38400.00	16 X	614.40000	18	0012	38400.00	614.40000	0.0000%
76800.00	16 X	1228.80000	9	0009	76800.00	1228.80000	0.0000%

from SOUT and SIN pins and directly connected internally) may be used individually or together.

ANALOG TO DIGITAL CONVERTER

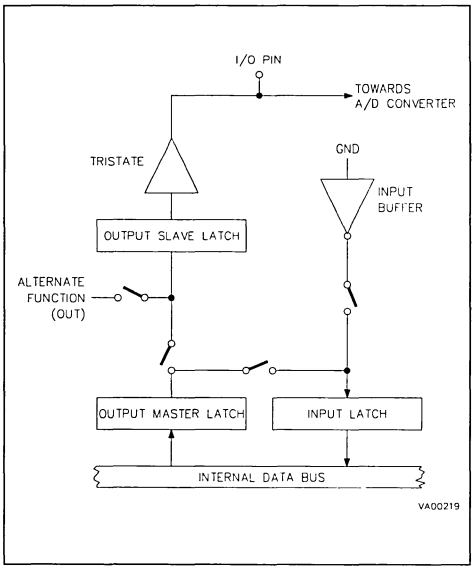
The ST90R50 Analog to Digital Converter (A/D) is comprised of an 8 channel multiplexed input selector and a Successive Approximation converter. The conversion time is a function of the INTCLK frequency; for the maximum 12MHz clock rate, conversion of the selected channel requires 11µs. This time also includes the 3µs of the integral Sample and Hold circuitry, which minimizes need for external components. The resolution of the converted channel is 8 bits ±1/2 LSB between the Analog V_{SS} and V_{DD} references which occupy two pins of the ST90R50 (AV_{SS} and AV_{DD} respectively). This allows the full 256 bit resolution to apply over a reduced input range such as provided by various sensors and allows the best supply noise rejection. The input Analog channel is selected by using the Alternate Function setting as shown in the I/O ports section. The I/O bit structure of the port connected to the A/D converter (Port 4) is modified as shown in figure 55 to prevent the Analog voltage present at the I/O pin from causing high power dissipation across the input buffer. Un-selected analog channels should also be maintained in the Alternate function mode for this reason. A Power Down mode is available for applications which require low power dissipation, this is selected by setting to zero

Figure 53. A/D Block Diagram



ANALOG TO DIGITAL CONVERTER (Continued)

Figure 54. A/D Input Configuration Status

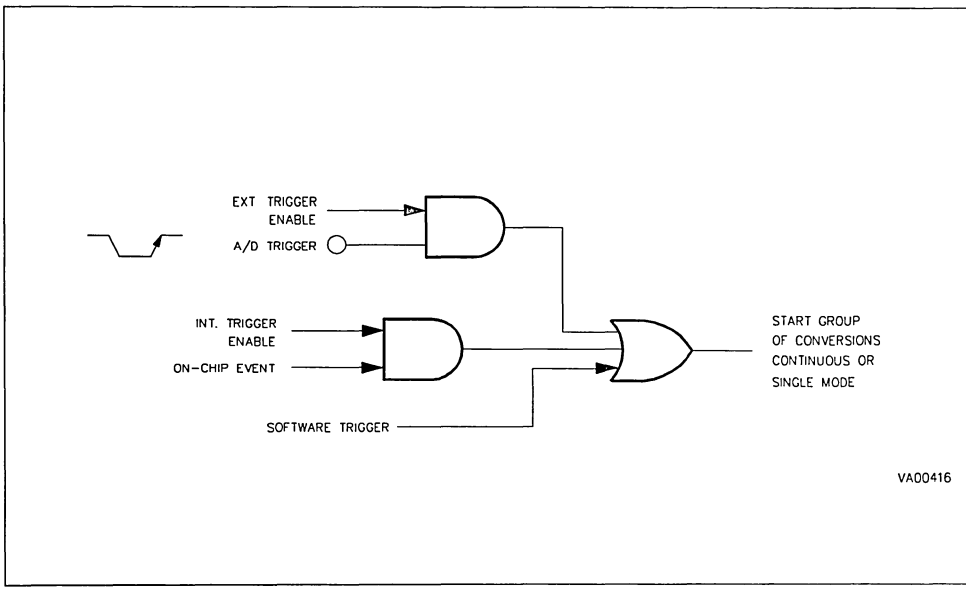


the POW bit (CLR.2) which turns off all Analog functions within the A/D converter.

Conversion

Each of the input Analog channels (AIN0-7) can be converted singly or continuously. In single mode (CONT, CLR.1, = "0") conversions are triggered by setting the Start/Stop bit ST (CLR.0), this is reset by hardware at the end of a group of conversions and conversion stops. The Autoscan mode (CONT = "1") converts each input channel in sequence, starting from the channel number selected in the Start Conversion Address (SC1-3) bits and increasing to channel 7 (AIN7), repeating so that the data registers will be maintained with the latest converted result. Conversion start is triggered by internal or external events. An external trigger (enabled by EXTG, CLR.4, = "1") is caused by a pulse on the ADTRG pin available as an Input Alternate Function. This should have a minimum length of 80 nS and of a period greater than the conversion time. The Internal trigger is enabled by setting INTG, CLR.3, to "1" (this is ORed with EXTG to prevent hardware conflicts, but the correct procedure is to enable only one source at a time), in this case

Figure 55. A/D Trigger Sources



ANALOG DIGITAL CONVERTER (Continued)

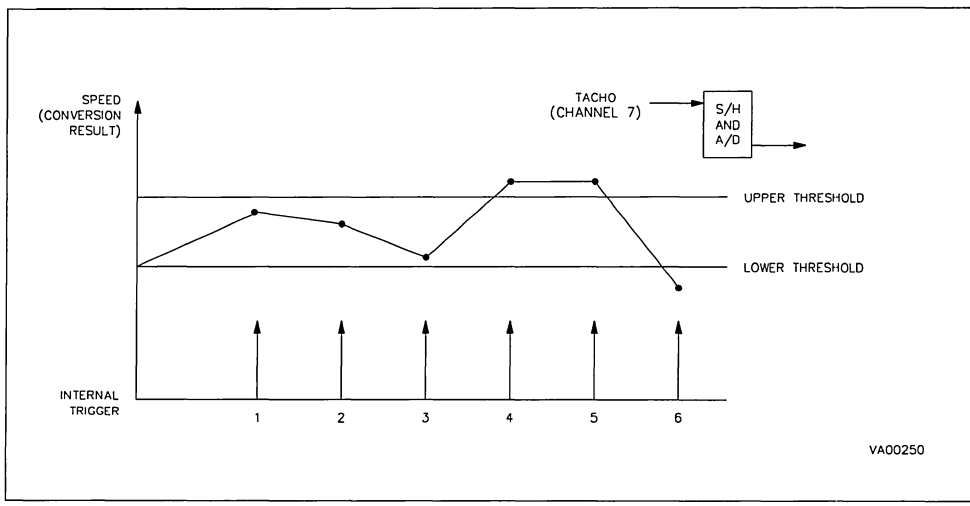
triggering is either by setting the ST bit by software or by enabling the ON-CHIP EVENT signal from the TIMER module.

The resulting data from the converted Analog channel AINx is stored in the appropriate Data Register DxR. Two channels AIN6 and AIN7 have a special feature known as the Analog Watchdog, by the use of two Threshold Registers for each channel. The Upper, (UT6R, UT7R), and lower, (LT6R, LT7R), registers contain User preset values. These values are automatically compared to the value in the Data Registers D6R and D7R following each new conversion. If the resulting data is less than the corresponding Lower Threshold Register, or higher than the contents of the corresponding Upper Threshold Register, then an interrupt may be generated. This hardware feature minimizes analog monitoring overhead and is particularly useful in motor control applications as shown in figure 56.

A/D Interrupts

The ST90R50 A/D converter provides two interrupt sources, End of Conversion and an Analog Watchdog Request. The interrupt vector register (IVR) provides 1 bit automatically generated in hardware to follow the interrupt source, allowing the User to select the base address of a four byte area of the interrupt vector table in which to store the A/D Interrupt Service Routines. The Analog Watchdog Request requires the User to poll within the Compare Result Register (CRR) to determine which of the four thresholds has been exceeded, the threshold status bits should be reset by software in the service routine. The interrupt pending flags, ECV (End of Conversion, ICR.7) and AWD (Analog

Figure 56. Analog Watchdog Used in Motor Speed Control



Watchdog, ICR.6) should also be reset by the User in the Interrupt service routine before the return.

The ST90R50 Analog to Digital converter occupies I/O page 63 (Group F).

SOFTWARE DESCRIPTION

Addressing Modes

The ST90R50 offers a wide variety of addressing modes and combinations to facilitate full and rapid access to the address spaces while reducing program length. Register addressing (using the working register group mechanism or directly addressed) can be used as 8 or 16 bit values for data or indirect addressing into the memory spaces or the Register File. The selection between Program Memory and Data Memory is performed through the DP bit in the FLAG Register, all subsequent actions on the memory space will affect the selected map only, apart from the memory map to memory map post-increment addressing mode which allows the map to be specified as part of the instruction for both destination and source operands. Apart from the immediate data and condition codes all operands are expressed as register file or memory addresses.

The available addressing modes, with the ST9 macro-assembler notation, are in Table 21.

Combinations of Available Addressing Modes

Table 21. Addressing Mode

Addressing Mode	Notation
Immediate Data	#N #NN
Register Direct	R;r RR;rr
Register Indirect	(R) (r)
Register Indexed	N(r) N(rr)
Memory Direct	NN
Memory Indirect	(RR) (rr)
Memory Indirect with Post-Increment	(rr)+
Memory Indirect with Pre-Decrement	-(rr)
Memory Indexed with Immediate Short Offset	N(rr)
Memory Indexed with Immediate Long Offset	NN(rr)
Memory Indexed with Register Offset	rr(rr)
Memory Indirect Post-Increment to Indirect Register Post-Increment	(rr)+ (r)+
Memory Map to Memory Map both with Post-Increment	(rr)+ (r)+
Bit Address	r.b, (rr).b

Legend:
N = 8 bit Value
NN = 16 bit Value or Address
r = Working Register
R = Directly Addressed Register
( ) = Indirect Addressing
( )+ = Indirect with Post-Increment
-( ) = Indirect with Pre-Decrement
b = Bit Number (0 to 7)

Table 22. Addressing Mode Permutation for Instructions

Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct

SOFTWARE DESCRIPTION (Continued)

Table 22. Addressing Mode Permutation for Instructions (Continued)

Two Operand Load Instructions	
Destination	**Source**
Register Direct	Register Direct
Register Direct	Register Indirect
Register Direct	Register Indexed
Register Direct	Memory Indirect
Register Direct	Memory Indexed
Register Direct	Memory Indirect with Post- Increment
Register Direct	Memory Indirect with Pre- Decrement
Register Direct	Memory Direct
Register Indirect	Register Direct
Register Indexed	Register Direct
Memory Indirect	Register Direct
Memory Indexed	Register Direct
Memory Indirect with Post- Increment	Register Direct
Memory Indirect with Pre- Decrement	Register Direct
Memory Direct	Register Direct
Two Operand Arithmetic and Logic Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Two Operand Load Instructions	
Destination	**Source**
Register Direct	Immediate
Memory Direct	Immediate
Memory Indirect	Immediate
Long Indexed Memory (1)	Immediate

Table 22. Addressing Mode Permutation for Instructions (Continued)

Two Operand Arithmetic, Logic & Load Instructions	
Destination	**Source**
Memory Indirect	Memory Indirect
Two Operand Load Instructions (2)	
Destination	**Source**
Register Indirect with Post- Increment	Memory Indirect with Post- Increment
Memory Indirect with Post- Increment	Register Indirect with Post- Increment
Memory Indirect with Post- Increment	Memory Indirect with Post- Increment

Notes:
1 Load Word only
2. Load Byte only

Table 22 describes the addressing modes available for the register file and the memory (both as a destination and as a source) for the two operand arithmetic, logic or load instructions.

Instruction Set

The ST90R50 instruction set consists of 87 instruction types functionally divided into eight groups as in Table 23, they are:

- Load (two operands)
- Arithmetic & Logic (two operands)
- Arithmetic Logic and Shift (one operand)
- Stack (one operand)
- Multiply & Divide (two operands)
- Boolean (one or two operands)
- Program Control (zero to three operands)
- Miscellaneous (zero to two operands)

The wide range of instructions facilitates the full use of the register file and address spaces, reducing execution times, while the register pointers mechanism allows an unmatched code efficiency and ultrafast context switching. A particularly notable feature is the comprehensive "Any Bit, Any Register" (ABAR) addressing capability of the Boolean instructions.

The ST90R50 can operate with a wide range of data lengths from single bit, 4-bit nibbles which can be in the form of Binary Coded Decimal (BCD) digits, 8-bit bytes and 16-bit words. The summary on Table 22 shows the instructions belonging to

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary

Load Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
LD LDW	dst, src dst, src	Load Load Word	– –	– –	– –	– –	– –	– –
Arithmetic and Logic (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
ADD ADDW	dst, src dst, src	Add Add Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
ADC ADCW	dst, src dst, src	Add with Carry Add Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	0 ?	Δ ?
SUB SUBW	dst, src dst, src	Subtract Subtract Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
SBC SBCW	dst, src dst, src	Subtract with Carry Subtract Word with Carry	Δ Δ	Δ Δ	Δ Δ	Δ Δ	1 ?	Δ ?
AND ANDW	dst, src dst, src	Logical AND Logical Word AND	– –	Δ Δ	Δ Δ	0 0	– ?	– ?
OR ORW	dst, src dst, src	Logical OR Logical Word OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
XOR XORW	dst, src dst, src	Logical Exclusive OR Logical Word Exclusive OR	– –	Δ Δ	Δ Δ	0 0	– –	– –
CP CPW	dst, src dst, src	Compare Compare Word	Δ Δ	Δ Δ	Δ Δ	Δ Δ	– –	– –
TM TMW	dst, src dst, src	Test Under Mask Test Word Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –
TCM TCMW	dst, src dst, src	Test Complement Under Mask Test Word Complement Under Mask	– –	Δ Δ	Δ Δ	0 0	– –	– –

Legend :
0 = Bit set to zero
1 = Bit set to one
Δ = Bit affected
? = Bit status undefined
– = Bit not affected

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Arithmetic Logic and Shift (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
INC INCW	dst dst	Increment Increment Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –
DEC DECW	dst dst	Decrement Decrement Word	– –	Δ Δ	Δ Δ	Δ Δ	– –	– –
SLA SLAW	dst dst	Shift Left Arithmetic Shift Word Left Arithmetic	Δ Δ	Δ Δ	Δ Δ	0 0	0 ?	Δ ?
SRA SRAW	dst dst	Shift Right Arithmetic Shift Word Right Arithmetic	Δ Δ	Δ ?	Δ Δ	Δ 0	0 –	Δ –
RRC RRCW	dst dst	Rotate Right through Carry Rotate Word Right through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –
RLC RLCW	dst dst	Rotate Left through Carry Rotate Word Left through Carry	Δ Δ	Δ ?	Δ Δ	Δ Δ	– –	– –
ROR	dst	Rotate Right	Δ	Δ	Δ	Δ	–	–
ROL	dst	Rotate Left	Δ	Δ	Δ	Δ	–	–
CLR	dst	Clear	–	–	–	–	–	–
CPL	dst	Complement Register	–	Δ	Δ	0	–	–
SWAP	dst	Swap Nibbles	?	Δ	Δ	?	–	–
DA	dst	Decimal Adjust	Δ	Δ	Δ	?	–	–
Stack Instructions (One Operand)									
Mnemonic	**Operand**	**Instruction**	**Flags**						
			C	**Z**	**S**	**V**	**D**	**H**
PUSH PUSHW PEA	src src src	Push on System Stack Push Word on System Stack Push Effective Address on System Stack	– – –	– – –	– – –	– – –	– – –	– – –
POP POPW	dst dst	Pop from System Stack Pop Word from System Stack	– –	– –	– –	– –	– –	– –
PUSHU PUSHUW PEAU	src src src	Push on User Stack Push Word on User Stack Push Effective Address on User Stack	– – –	– – –	– – –	– – –	– – –	– – –
POPU POPUW	dst dst	Pop from User Stack Pop Word from User Stack	– –	– –	– –	– –	– –	– –

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Multiply and Divide Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
MUL	dst, src	Multiply 8x8	Δ	Δ	Δ	Δ	0	?
DIV DIVWS	dst, src	Divide 16/8 Divide Word Stepped 32/16	1 ?	Δ ?	Δ ?	? ?	1 ?	? ?
Boolean Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BLD	dst, src	Bit Load	–	–	–	–	–	–
BAND	dst, src	Bit AND	–	–	–	–	–	–
BOR	dst, src	Bit OR	–	–	–	–	–	–
BXOR	dst, src	Bit Exclusive OR	–	–	–	–	–	–
Boolean Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BSET	dst	Bit Set	–	–	–	–	–	–
BRES	dst	Bit Reset	–	–	–	–	–	–
BCPL	dst	Bit Complement	–	–	–	–	–	–
BTSET	dst	Bit Test and Set	–	Δ	Δ	0	–	–
Program Control Instructions (Three Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
CPJFI	dst, src	Compare and Jump on False, Otherwise Post Increment	–	–	–	–	–	–
CPJTI	dst, src	Compare and Jump on True, Otherwise Post Increment	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Program Control Instructions (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
BTJF	dst, src	Bit Test and Jump if False	–	–	–	–	–	–
BTJT	dst, src	Bit Test and Jump if True	–	–	–	–	–	–
DJNZ	dst, src	Decrement a Working Register and Jump if Not Zero	–	–	–	–	–	–
DWJNZ	dst,src	Decrement a Register Pair and Jump if Not Zero	–	–	–	–	–	–
Program Control Instructions (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
JR	cc, dst	Jump Relative if Condition is Met	–	–	–	–	–	–
JP	cc, dst	Jump if Condition is Met	–	–	–	–	–	–
JP	dst	Unconditional Jump	–	–	–	–	–	–
CALL	dst	Unconditional Call	–	–	–	–	–	–
Program Control Instructions (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
RET		Return from Subroutine	–	–	–	–	–	–
IRET		Return from Interrupt	Δ	Δ	Δ	Δ	Δ	Δ
WFI		Stop Program Execution and Wait Next Enabled Interrupt. If a DMA request is present the CPU executes the DMA service routine and returns to WFI state.	–	–	–	–	–	–
HALT		Stop Program Execution until RESET	–	–	–	–	–	–
Miscellaneous (Two Operands)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
XCH	dst, src	Exchange Registers	–	–	–	–	–	–

SOFTWARE DESCRIPTION (Continued)

Table 23. Instruction Set Summary (Continued)

Miscellaneous (One Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
SRP	src	Set Register Pointer Long (16 Working Registers)	–	–	–	–	–	–
SRP0	src	Set Register Pointer 0 (8 LSB Working Registers)	–	–	–	–	–	–
SRP1	src	Set Register Pointer 1 (8 MSB Working Registers)	–	–	–	–	–	–
SPP	src	Set Page Pointer	–	–	–	–	–	–
EXT	src	Sign Extend	–	–	–	–	–	–
Miscellaneous (No Operand)								
Mnemonic	**Operand**	**Instruction**	**Flags**					
			C	**Z**	**S**	**V**	**D**	**H**
EI		Enable Interrupts	–	–	–	–	–	–
DI		Disable Interrupts	–	–	–	–	–	–
SCF		Set Carry Flag	1	–	–	–	–	–
RCF		Reset Carry Flag	0	–	–	–	–	–
CCF		Complement Carry Flag	Δ	–	–	–	–	–
SPM		Select Program Memory	–	–	–	–	–	–
SDM		Select Data Memory	–	–	–	–	–	–
NOP		No Operation	–	–	–	–	–	–

each group and the number of operands required for each. The source operand is "src", "dst" is the destination operand, and "cc" is the condition code selection.

Processor Flags

An important aspect of any single chip microcontroller is the ability to test data and make the appropriate action based on the results. In order to provide this facility, register 231 in the Register File is used as a Flag Register. Six bits of this register are used as the following flags:

C - Carry

Z - Zero

S - Sign

V - Overflow

D - Decimal Adjust

H - Half Carry

One of the two remaining bits in the flag register is available to the user (bit 1, F1). Bit 0 is the Program/Data Memory selector bit and is operated on directly by the hardware within the ST90R50. The P/$\overline{D}$ pin will follow the status of this bit.

SOFTWARE DESCRIPTION (Continued)

Table 24. Condition Codes Summary

Mnemonic Code	Meaning	Flag Setting
F	Always False	—
T	Always True	—
C	Carry	C = 1
NC	No Carry	C = 0
Z	Zero	Z = 1
NZ	No Zero	Z = 0
PL	Plus	S = 0
MI	Minus	S = 1
OV	Overflow	V = 1
NOV	No Overflow	V = 0
EQ	Equal	Z = 1
NE	Not Equal	Z = 0
GE	Greater Then or Equal	(S xor V) = 0
LT	Less Than	(S xor V) = 1
GT	Greater Than	(Z or (S xor V)) = 0
LE	Less Than or Equal	(Z or (S xor V)) = 1
UGE	Unsigned Greater Than or Equal	C = 0
UL	Unsigned Less Than	C = 1
UGT	Unsigned Greater Than	(C = 0 and Z = 0) = 1
ULE	Unsigned Less Than or Equal	(C or Z) = 1

Condition Codes. Flags C, Z, S, and V control the operation of the "conditional" Jump instructions. Table 24 shows the condition codes and the flag settings affecting the jump.

POWERFUL DEVELOPMENT ENVIRONMENT

ST9 Software Tools

The following Software Tools are available for MS-DOS, SUN-3 and SUN-4 operating systems:

AST9 high-level macro assembler with predefinited macro instructions (IF/ELSE, WHILE, DO, LOOP, SWITCH, BREAK, PROCEDURE, RESTURN).

LST9 Incremental Linker/Loader.

CST9 Optimised C-Compiler (ANSI STANDARD).

ARST9 Library Archiver.

SIMST9 Software Simulator with realtime emulation executor

ST90R50 Hardware Emulator. Realtime emulation of the ST90R50 in all packaging options is performed by a modular emulation system, interfaced to the host computer through an RS232

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note· Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

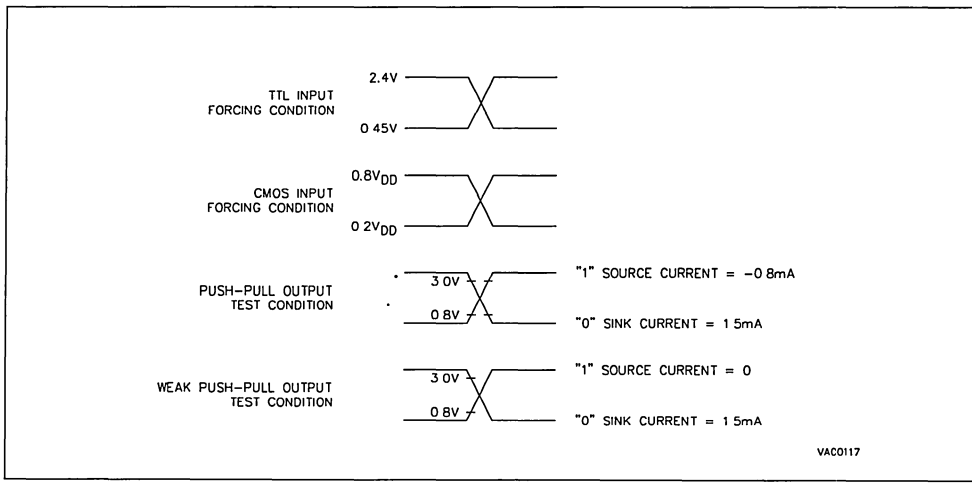
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, 0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	0V < V_{IN} < V_{DD}	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, 0V < V_{IN} < V_{DD}	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	0V < V_{IN} < 0.8V	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note:
1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

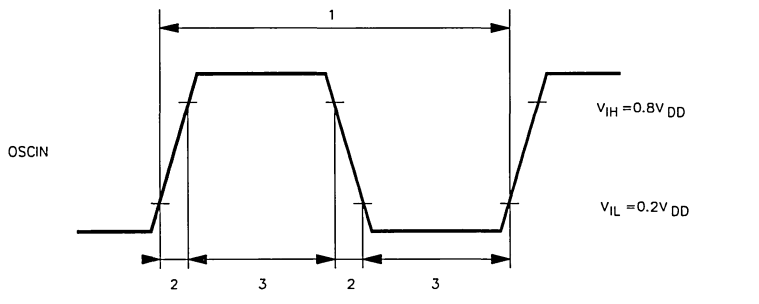
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	1
			38		ns	2

Notes:
1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

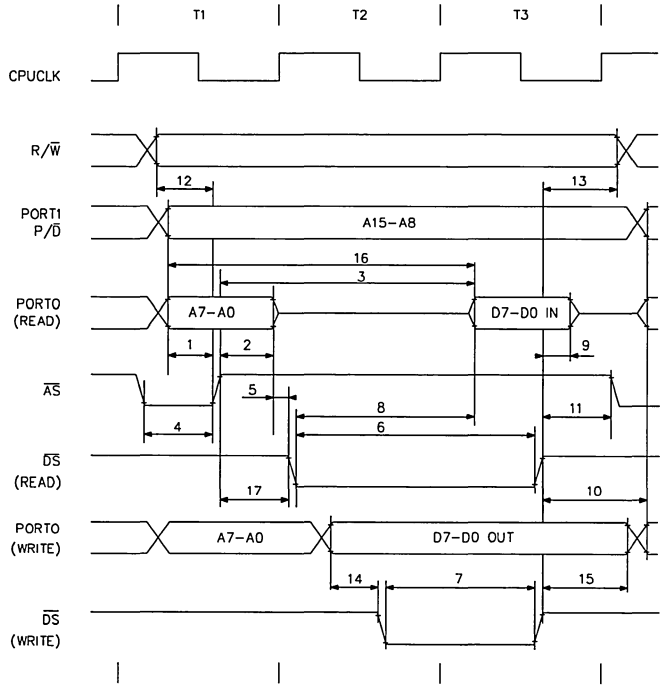
Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

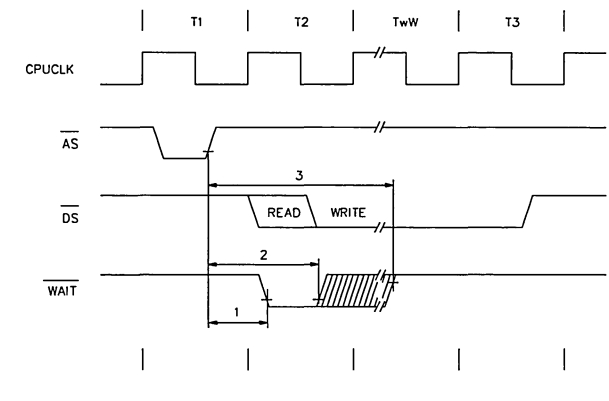
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC – 29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING

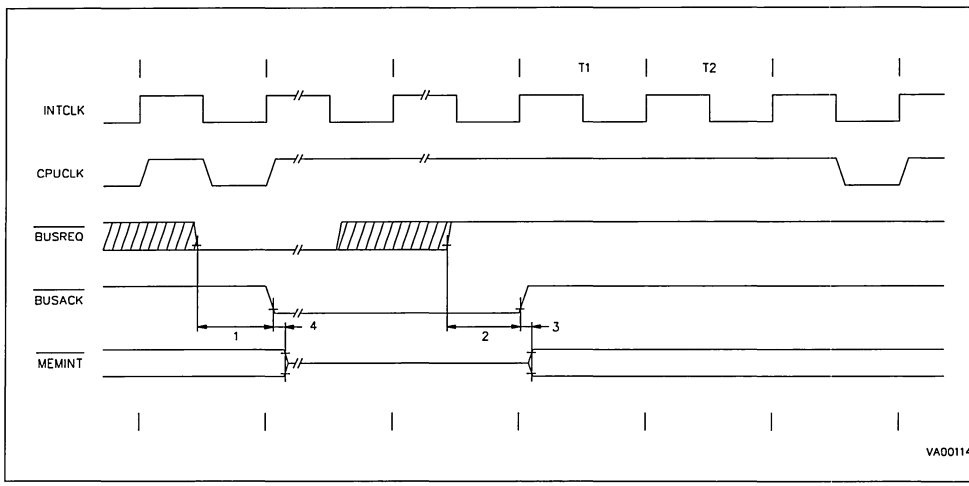


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2 prescale value of zero and zero wait status

BUS REQUEST/ACKNOWLEDGE TIMING



Note MEMINT = group of memory interface signals · $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17

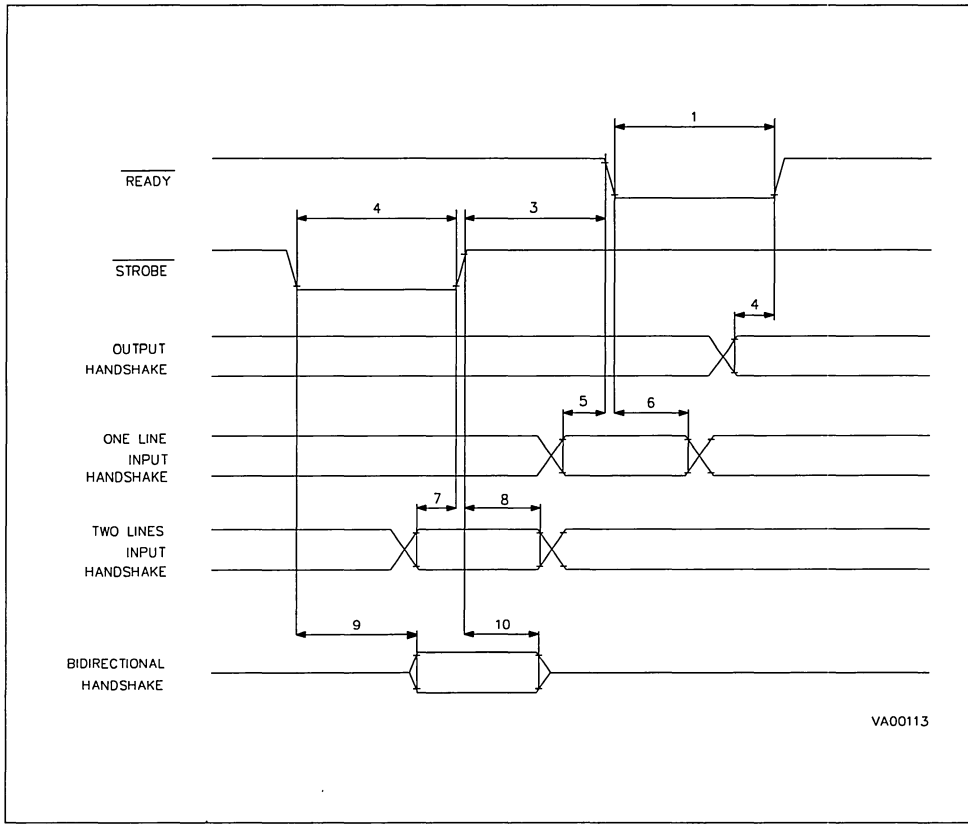
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		Tp (P+W+1) – 18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1 0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

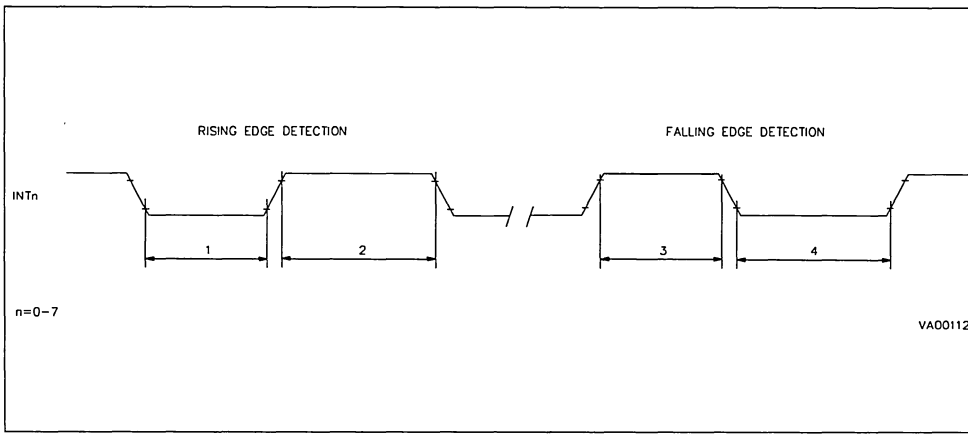


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status

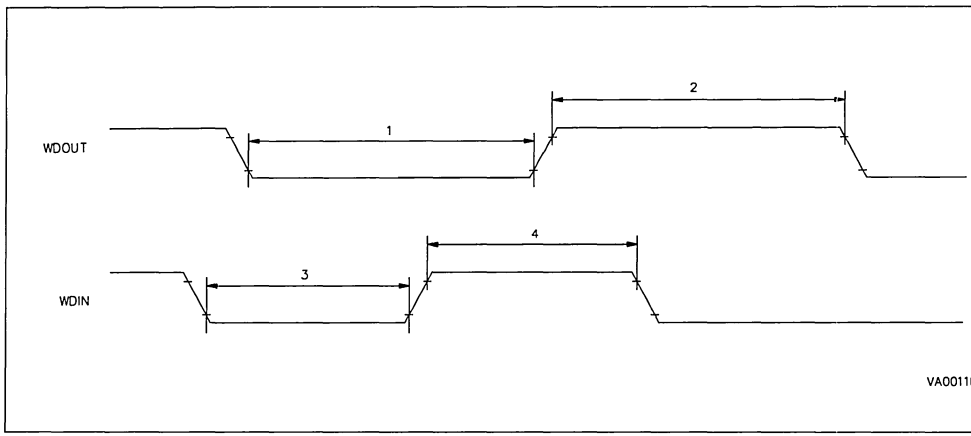
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK =12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

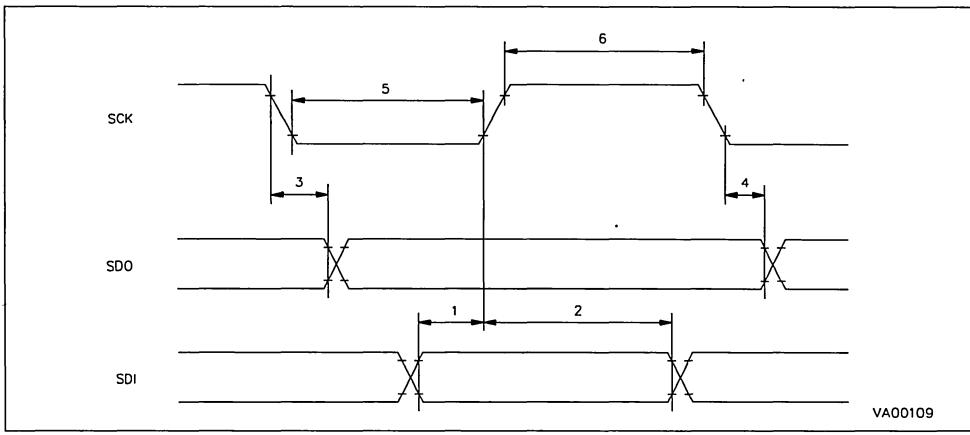


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

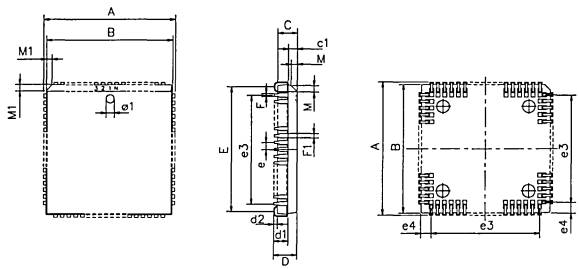
Note: 1. TpC is the Clock period.

SPI TIMING



PACKAGE MECHANICAL DATA

Figure 57. 84-Lead Plastic Leaded Chip Carrier



DIM	MM			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	30.10		30 35	1 18		1.19
B	29.20		29 41	1.14		1.15
C						
C1						
D	4 20		5 08	0 16		0.19
D1		2.54			0.02	
D2		0 56				
D3				1.09		1.12
E	27 69		28 70		0.04	
e		1.27				
e3					0 01	
F		0 38				
F1						0.003
G			0.101			
H		1.27			0 04	
H1		1.14			0 04	

ORDERING INFORMATION

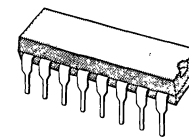
Sales Type	Frequency	Temperature Range	Package
ST90R50C6	24MHz	-40°C to +85°C	PLCC84
ST90R50C1	24MHz	0°C to +70°C	PLCC84

SGS-THOMSON MICROELECTRONICS

TDA1180P

TV HORIZONTAL PROCESSOR

- NOISE GATED HORIZONTAL SYNC SEPARATOR
- NOISE GATED VERTICAL SYNC SEPARATOR
- HORIZONTAL OSCILLATOR WITH FREQUENCY RANGE LIMITER
- PHASE COMPARATOR BETWEEN SYNC PULSES AND OSCILLATOR PULSES (PLL)
- PHASE COMPARATOR BETWEEN FLYBACK PULSES AND OSCILLATOR PULSES (PLL)
- LOOP GAIN AND TIME CONSTANT SWITCHING (VCR)
- COMPOSITE BLANKING AND KEY PULSE GENERATOR
- PROTECTION CIRCUITS
- OUTPUT STAGES WITH HIGH CURRENT CAPABILITY



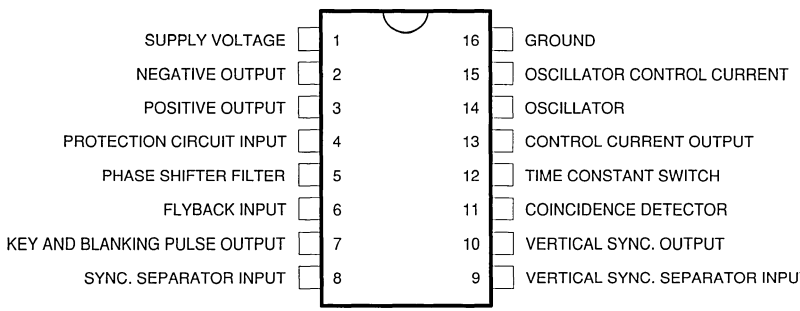
DIP16
(Plastic Package)

ORDER CODE : TDA1180P

DESCRIPTION

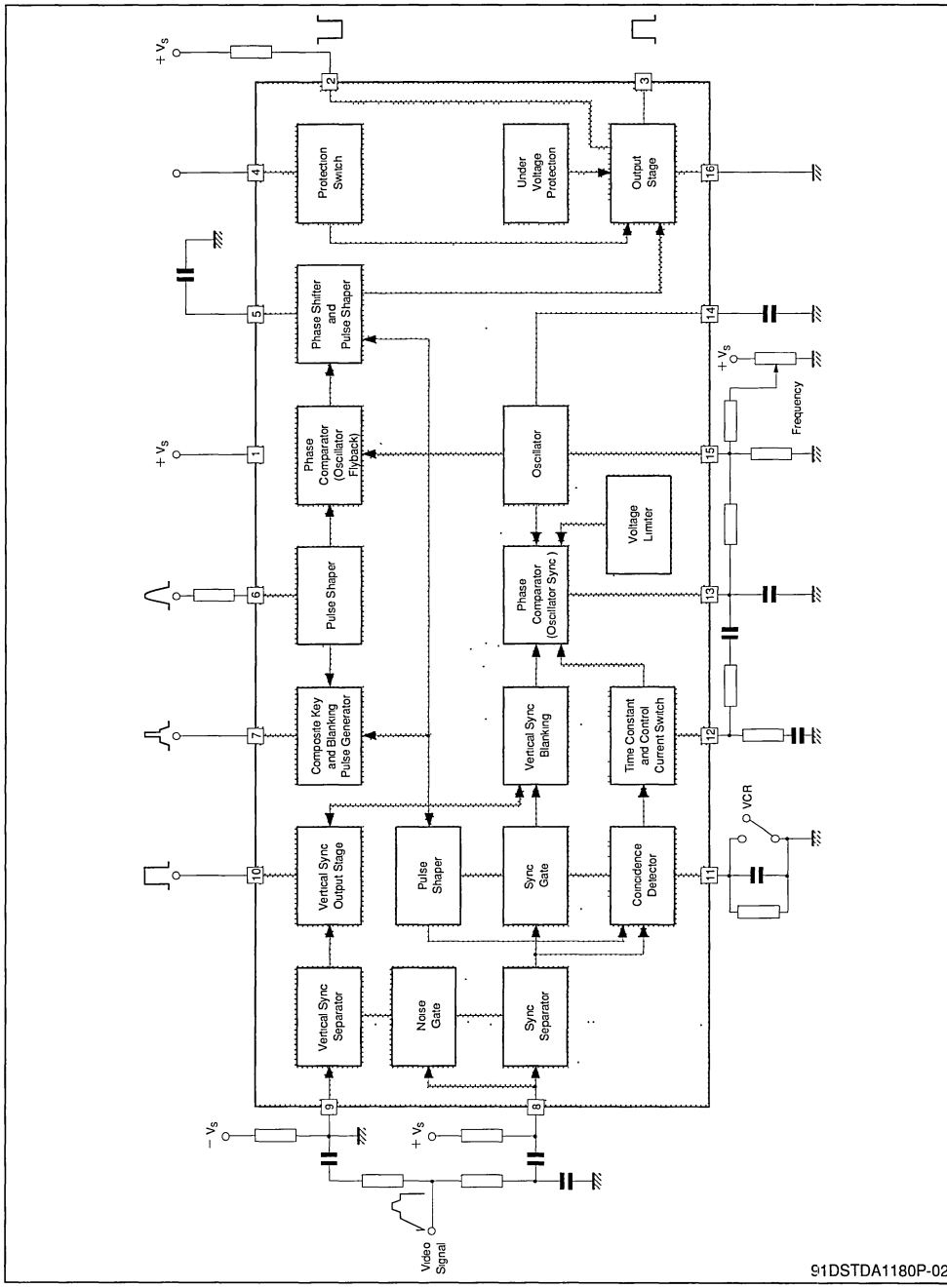
The TDA1180P is a horizontal processor circuit for b.w. and colour monitors. It is a monolithic integrated circuit encapsulated in 16-lead dual in-line plastic package.

PIN CONNECTIONS



91DSTDA1180P-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply voltage (Pin 1)	15	V
V_2	Voltage at Pin 2	18	V
V_4	Voltage at Pin 4	V_S	
V_8	Voltage at Pin 8	- 6 , V_S	V
V_9	Voltage at Pin 9	± 6	V
V_{11}	Voltage at Pin 11	V_S	
I_2	Pin 2 peak current	1	A
I_3	Pin 3 peak current	0.5	A
I_6	Pin 6 current	30	mA
I_7	Pin 7 current	20	mA
I_{10}	Pin 10 current	30	mA
P_{tot}	Total power dissipation at Tamb ≤ 70°C	1	W
T_{stg} , T_j	Storage and junction temperature	- 40 , + 150	°C

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Thermal Resistance Junction-Ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 12V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage range		9.5	12	13.2	V
I_S	Supply current	I_3 = 0		42	52	mA
V_S	Supply voltage at which the output pulses (at pin 2 and 3) are switched off				4	V
HORIZONTAL SYNC. SEPARATOR						
V_I	Peak to peak input signal		1	3	6	V
V_8	Input switching voltage	I_8 = 80 µA		1.5		V
I_8	Input switching current	V_8 = 1.4V		10		µA
I_8	Leakage current	V_8 = -5V			1	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VERTICAL SYNC. SEPARATOR						
V_I	Peak to Peak Input Signal		1	3	6	V
V_9	Input Switching Voltage	I_9= 80µA		1.5		V
I_9	Input Switching Current	V_9 = 1.4V		5		µA
I_9	Leakage Current	V_9 = -5V			1	µA
V_{10}	Vertical Sync. Pulse Output Voltage	No Load Pin10	11			V
R_{10}	Output Resistance			10		kΩ
t_{LV}	Delay between Leading Edge of Input and Output Signals			17		µs
t_{LV}	Delay between Trailing Edge of Input and Output Signals			50		µs
t_V	Vertical Sync Pulse Duration			190		µs
PROTECTION CIRCUIT						
V_4	Input Voltage for Switching off the Output Pulses	Output Pulses OFF Output Pulses ON	1		0.5	V
R_4	Input Resistance			200		kΩ
I_4	Input Current		5			µA
FLYBACK PULSE						
V_6	Input Threshold Voltage of Blanking Generator			1.8		V
V_6	Input Threshold Voltage of Phase Comparator			7.6		V
I_6	Input Switching Current	$V_6 \geq$ 1.7V		0.45		mA
OUTPUT PULSE						
V_3	Peak-to-Peak Output Voltage	I_3 = 150 mApp		10		V
I_3	Output Current	V_3 = 5V		500		mA
R_3	Output Resistance	At Leading Edge of output pulse At Training Edge of Output Pulse		3 20		Ω Ω
t_p	Output Pulse Duration		20	22	26	µs
COMPOSITE BLANKING AND KEY PULSE						
V_{7k}	Key Pulse Output Peak Voltage		9	11		V
V_{7B}	Blanking Pulse Output Voltage		4.2	4.5	4.8	V
R_7	Output Resistance			100		Ω
t_{sk}	Phase Relation Between Trailing Edge of Key Pulse and Middle of Sync. Input Pulse			2.7		µs
t_k	Key Pulse Duration		3.5	3.8		µs
t_{fb}	Delay between Flyback Pulse and Blanking Pulse	V_6 = 1.7V			0.2	µs

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INTERNAL GATING PULSE						
t_g	Gating Pulse Duration			7.5		µs
t	Phase Relation between Middle of Sync. Pulse and Trailing and Leading Edge of Gating Pulse			3.75		µs
COINCIDENCE DETECTOR						
V_{11}	Output Voltage	With Coincidence Without Coincidence		6.8	 4	V V
I_{11}	Peak Output Current			0.5		mA
VCR SWITCH						
V_{11}	Input Voltage		0 to 4 or 8.5 to 12			V
$-I_{11}$	Output Current		35			µA
I_{11}	Output Current		0.4			mA
TIME CONSTANT SWITCH						
V_{12}	Output Voltage			3		V
R_{12}	Output Resistance	$4.5V < V_{11} < 8V$ $V_{11} > 8.5V$ or $V_{11} < 4V$		100 40		Ω kΩ
OSCILLATOR						
V_{14}	Low Level Threshold Voltage			5.4		V
V_{14}	High Level Threshold Voltage			8.2		V
I_{14}	Charge Current			0.6		mA
I_{14}	Discharge Current			0.3		mA
V_{15}	Current Source Supply Voltage			3		V
I_{15}	Current Source Supply Current			0.3		mA
f_O	Free Running Frequency			15625		Hz
$\frac{\Delta f_O}{f_O}$	Adjustment Range			± 10		%
$\frac{\Delta f_O}{\Delta I_{15}}$	Frequency Control Sensitivity			52		$\frac{Hz}{\mu A}$
Δf_O	Frequency Change when V_S Drops to 4V				± 10	%
OSCILLATOR-FLYBACK PULSE PHASE COMPARATOR						
V_5	Control Voltage Range		9.4 to 8.2			V
I_5	Peak Control Current		-0.6		+0.6	mA
I_5	Input Current (blocked Phase Detector)				5	µA
t_D	Permissible Delay between Output Pulse Leading Edge and Flyback Pulse Leading Edge			$t_p - t_f$		µs
$\frac{\Delta t}{\Delta t_D}$	Static Control Error				0.2	%

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SYNC PULSE-OSCILLATOR PHASE COMPARATOR						
V_{13}	Control Voltage Range			4.6 to 1.4		V
I_{13}	Control Peak Current		+2	-2.2	-2	mA
$\frac{\Delta f}{\Delta t}$	Phase Lock Loop Gain			2		$\frac{kHz}{\mu s}$
f	Catching and Holding Range			± 700		Hz
OVERALL PHASE RELATIONSHIP						
t_O	Phase Relation between Middle of Flyback Pulse and Middle of Sync. Pulse			2.2		µs
$\frac{\Delta V_5}{\Delta t_O}$	Adjustment Sensitivity			65		$\frac{mV}{\mu s}$
$\frac{\Delta I_5}{\Delta t_O}$	Adjustment Sensitivity			16		$\frac{\mu A}{\mu s}$

TEST CIRCUIT

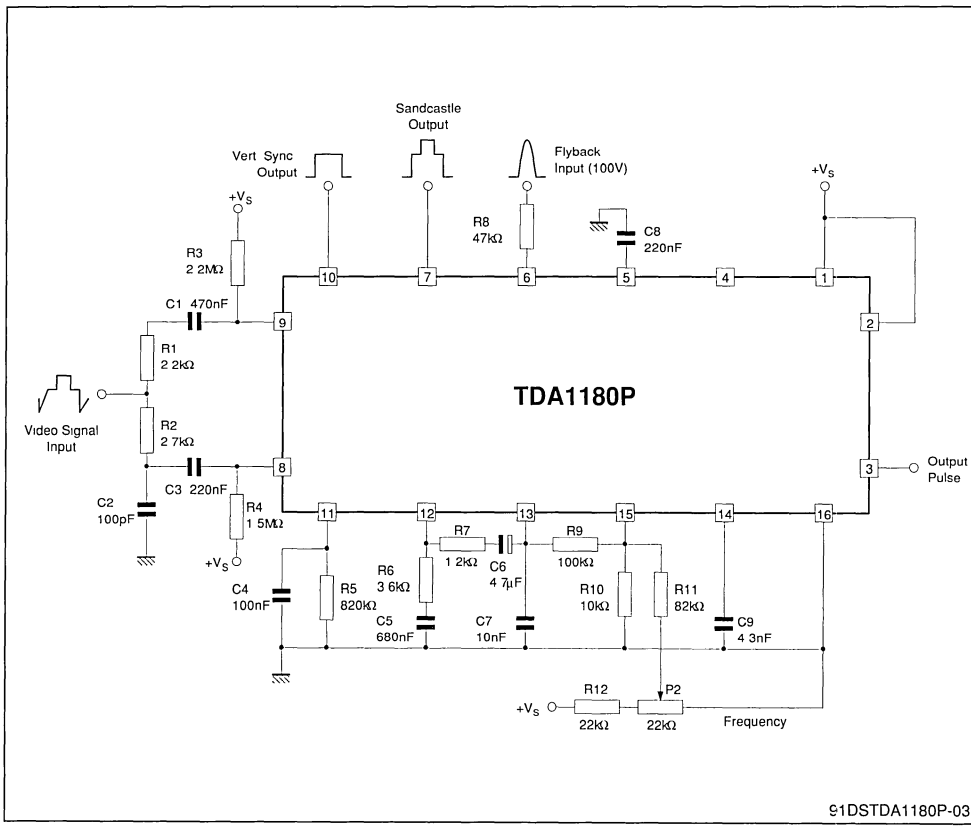


Figure 1 : Vertical Sync. Output Pulse

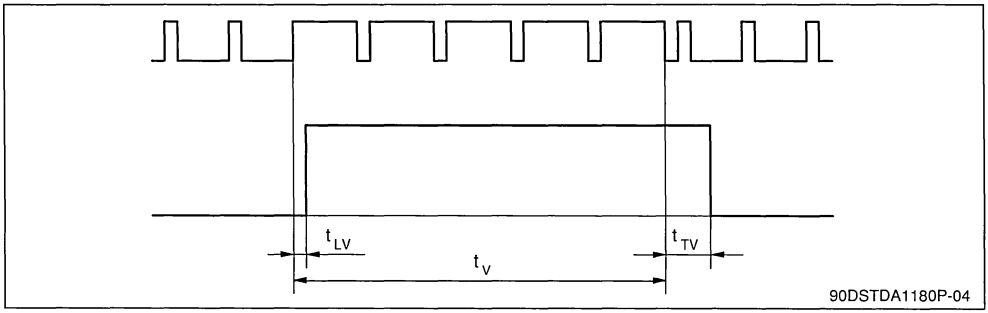


Figure 2 : Relation Ship of Main Waveform Phases

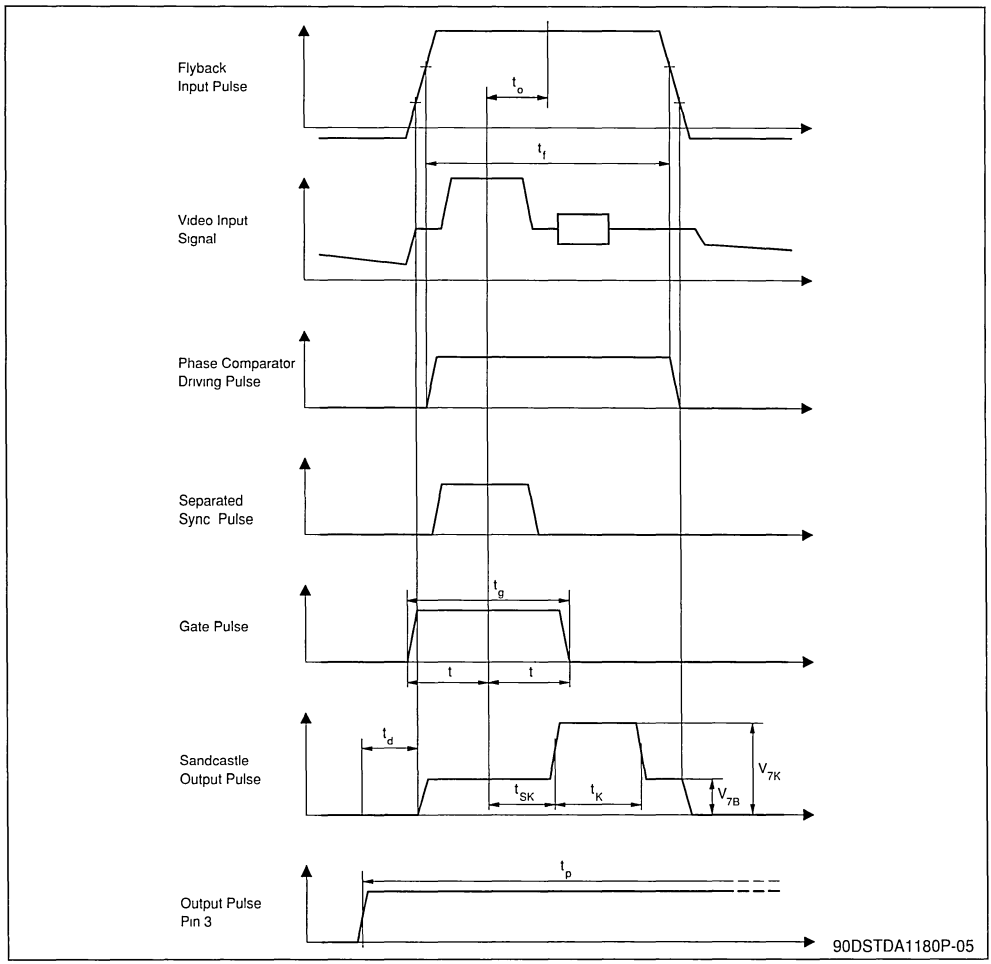


Figure 3 : Free Running Frequency versus Supply Voltage

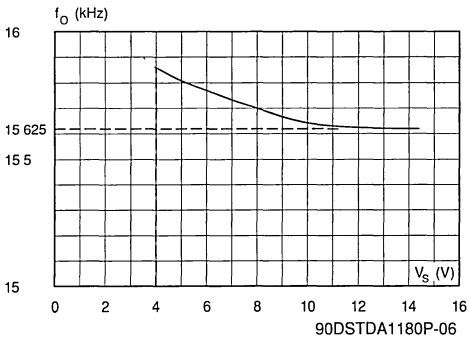
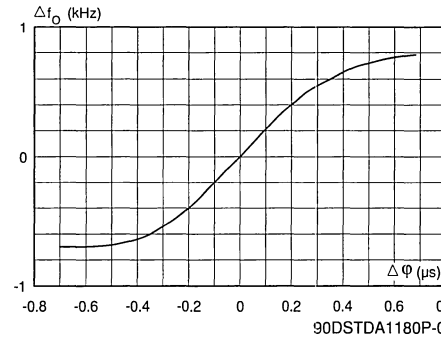


Figure 4 : Loop Gain



APPLICATION INFORMATION

Pin 1 - Positive supply

The operating supply voltage of the device ranges from 10V to 13.2V

Pin 2 and 3 - Output

The outputs of TDA1180P are suitable for driving transistor output stages, they deliver positive pulse at Pin 3 and negative pulse at Pin 2.
The negative pulse is used for direct driving of the output stage, while positive pulse is useful when a driver stage is required.
The rise and fall times of the output pulses are about 150 ns so that interference due to radiation are avoided.
Furthermore the output stages are internally protected against short circuit.

Pin 4 - Protection circuit input

By connecting Pin 4 of the IC to earth the output pulses at Pin 2 and 3 are shut off ; this function has been introduced to produced to protect the final stages from overloads.
The same pulses are also shut off when the supply voltage falls below 4V.

Pin 5 - Phase shifter filter

To compensate for the delay introduced by the line final stages, the flyback pulses to Pin 6 and the oscillator waveform are compared in the oscillator-flyback pulse phase comparator.
The result of the comparison is a control current which, after it has been filtered by the external capacitor connected to Pin 5, is sent to a phase shifter which adequately regulates the phase of the output pulses.
The maximum phase shift allowed is: $t_d = t_p - t_f$ where t_f is the flyback pulse duration.
Pin 5 has high input and output resistance (current generator).

Pin 6 - Flyback input

The flyback pulse drives the high impedance input through a resistor in order to limit the input current to suitable maximum values.
The flyback input pulses are processed by a double threshold circuit; this generates the blanking pulses by sensing low level flyback voltage and the pulses to drive the phase comparator by sensing high level flyback voltage, therefore phase jitter caused by ringing normally associated with the flyback pulse, is avoided.

Pin 7 - Key and blanking pulse output

The key pulse for taking out the burst from the chrominance signal is generated from the oscillator ramp and has therefore a fixed phase position with respect to the sync.
The key pulse is then added internally to the blanking pulse obtained by correctly forming the flyback pulse present at Pin 6.
The sum of the two signals (sandcastle pulse) is available on low impedance at output Pin 7.

Pin 8 and 9 - Sync separators inputs
The video signal is applied by means of two distinct biasing networks to pins 8 and 9 of the IC and therefore to the respective vertical and horizontal sync separators.
The latter take the sync pulses out of the video signal and make them available to the rest of the circuit for further processing.

Pin 10 - Vertical sync output
The vertical sync pulse, obtained by internal integration of the synchronizing signal, is available at this pin.
The output impedance is typically 10kΩ and the lowest amplitude without load is 11V.

Pin 11 - Coincidence detector
From the oscillator waveform a gate pulse 7 µs wide is taken whose phase position is centered on the horizontal synchronism.
The gate pulse not only controls a logic block which permits the sync to reach the oscillator-sync phase comparator only for as long as its duration, but also allows the latching and de-latching conditions of the oscillator to be established.This function is obtained by a coincidence detector which compares the phase of the gate pulses with that of the sync.
When the two signals are not accurately aligned in time it means that the oscillator is not synchronized. In this case the detector acts on the logic block to eliminate its filtering effect and on the time constant switching block to establish a high impedance on Pin 12 (small time constant of low-pass filter).
This latter block also acts on the oscillator-sync phase detector to increase its sensitivity and with it the loop gain of the synchronizing system.
In this conditions the phase lock has low noise immunity (wide equivalent noise bandwidth) and rapid pull-in time which allows fairly short synchronization times.
Once locking has taken place the coincidence detector enables the logic block, causes a low impedance on Pin 12 and reduces the sensitivity of the phase comparator.
In these conditions the phase lock has high noise immunity (narrow equivalent noise bandwidth) due to the complete elimination of interference which occurs during the scanning period and the greater inertia with which the oscillator can change its frequency.
To optimize the behaviour of the IC if a video recorder is used, the state of the detector can be forced by connecting Pin 11 to earth or to + V_S. The characteristics of the phase lock thus correspond to the lack of synchronization.

Pin 12 - Time constant switch, (see Pin 11)

Pin 13 - Control current output
The oscillator is synchronized by comparing the phase of its waveform with that of the sync pulses in the oscillator-sync phase comparator and sending its output current I13 (proportional to the phase difference between the two signals) to Pin 15 of the oscillator after it has been filtered properly with an external low-pass circuit.
The time constant of the filter can be switched between two values according to the impedance presented by Pin 12.
The voltage limiter at the output of the phase comparator limits the voltage excursion on Pin 13 and therefore the frequency range in which the oscillator remains held-in.
The output resistance of Pin 13 is:
- low when V13 > 4.3 or V13 < 1.6V
- high when 1.6V < V13 < 4.3V

To prevent the vertical sync from reaching the oscillator-sync phase comparator along with the horizontal sync,a signal which inhibits the phase detector during the vertical interval is taken from the vertical output stage; inhibition remain even if the video signal is not present.
The free running frequenc of the oscillator is determined by the values of the capacitor and of the resistor connected to Pins 14 and 15 respectively.
To generate the line frequency output pulses, two theresholds are fixed along the fall ramp of the triangular waveform of the oscillator.

Pin14 - Oscillator (see Pin 13)

Pin 15 - Oscillator control current input (see Pin 13)
Pin 16 - Ground

Figure 5 : Application Circuit for Large Screen Black & White and Colour TV

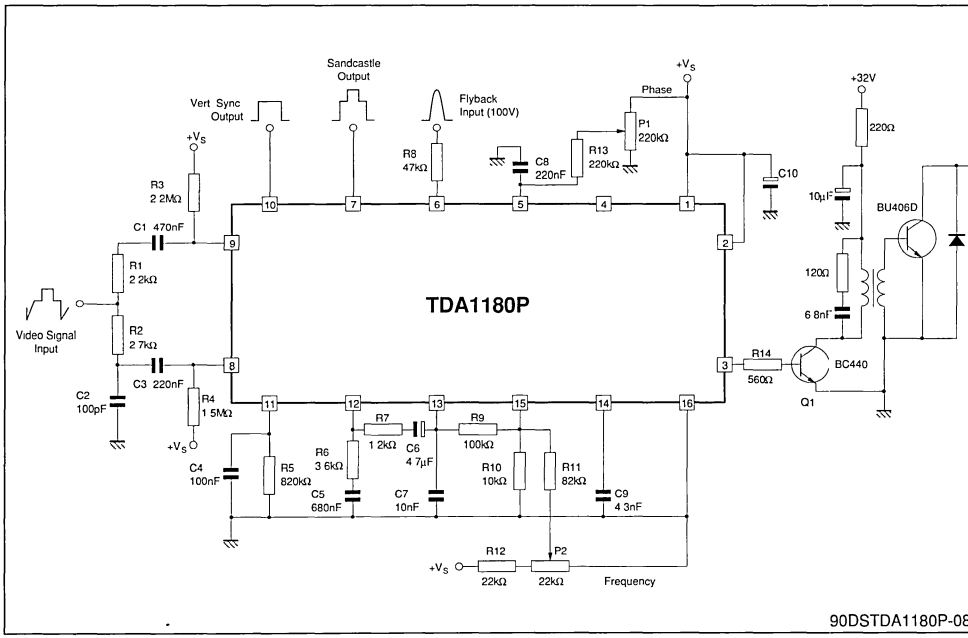


Figure 6 : P.C. Board and Component Layout for the Circuit in Figure 6 (1:1 scale)

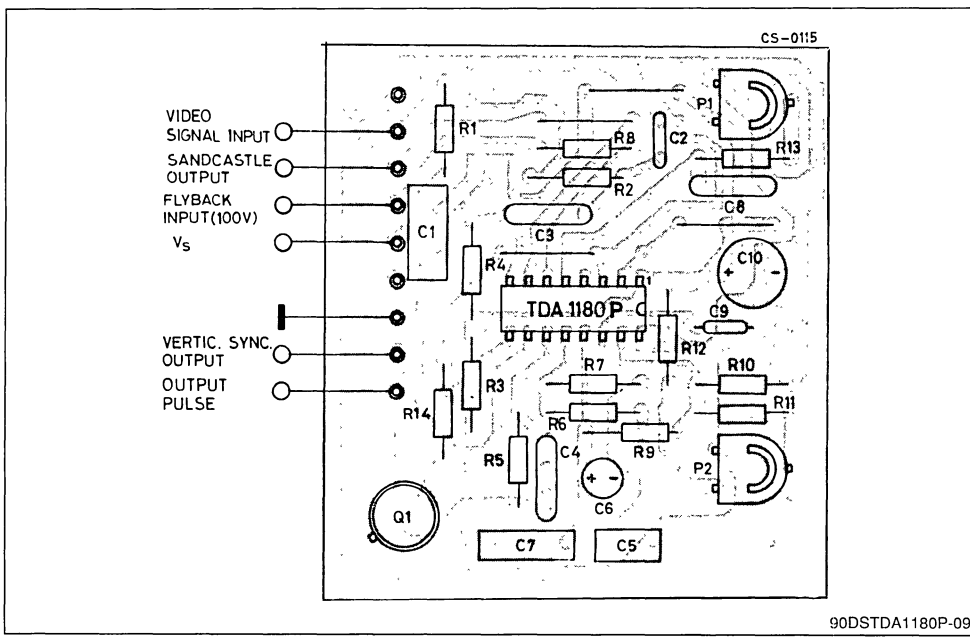


Figure 7 : Application Circuit for Small Screen b.w. TV

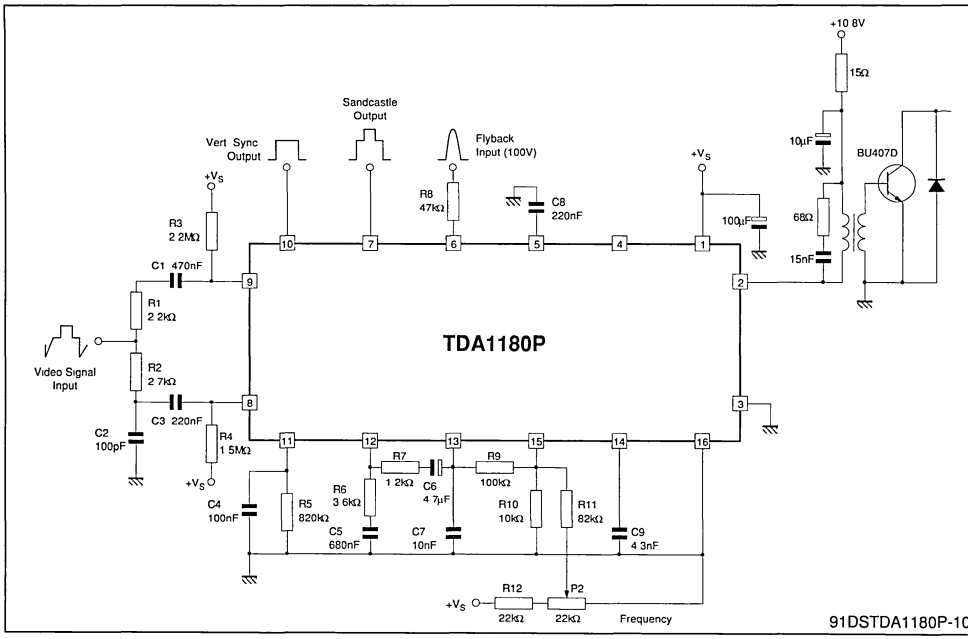
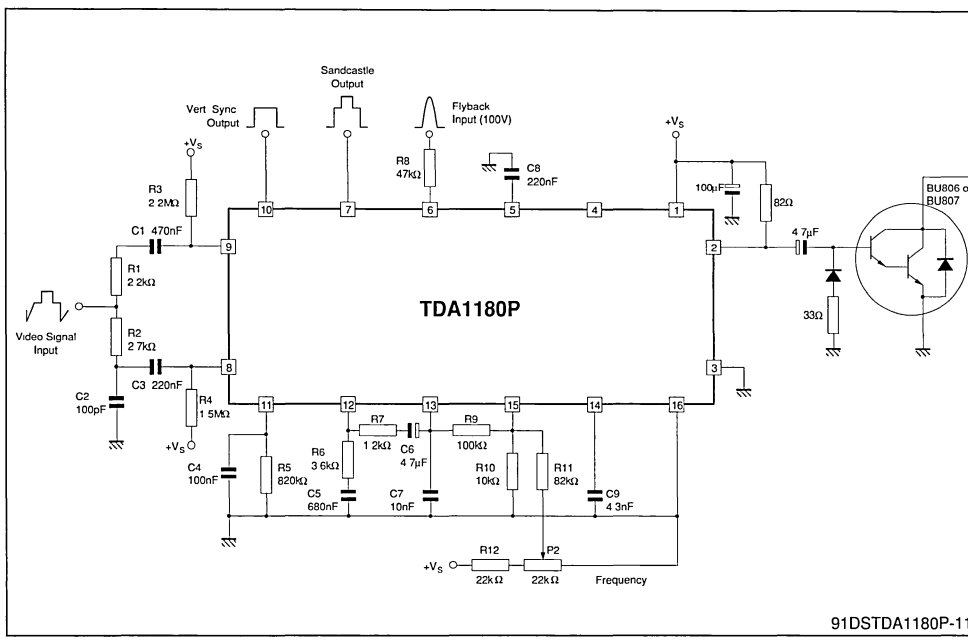
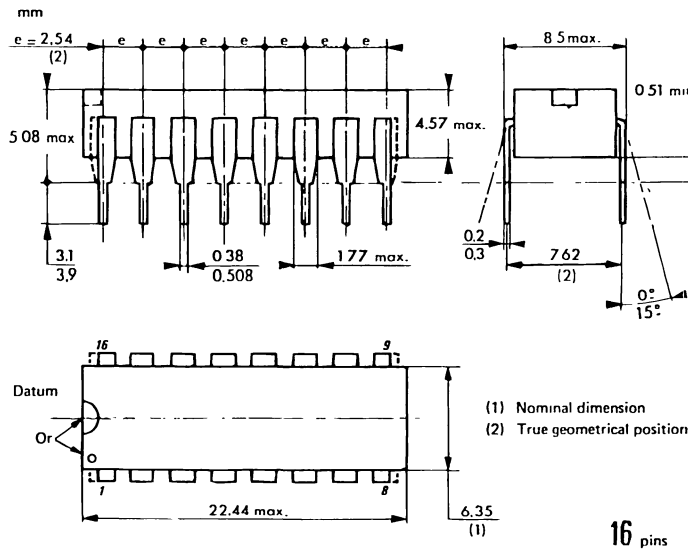


Figure 8 : Application Circuit for Darlington Output Stage



PACKAGE MECHANICAL DATA

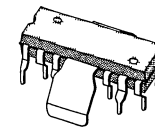
16 PINS - PLASTIC DIP



COMPLETE TV SOUND CHANNEL

The TDA 1190Z is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It performs all the functions needed for the TV sound channel :

- IF LIMITER-AMPLIFIER
- ACTIVE LOW-PASS FILTER
- FM DETECTOR
- DC VOLUME CONTROL
- AF PREAMPLIFIER
- AF OUTPUT STAGE



FINDIP 12
(Plastic Package)

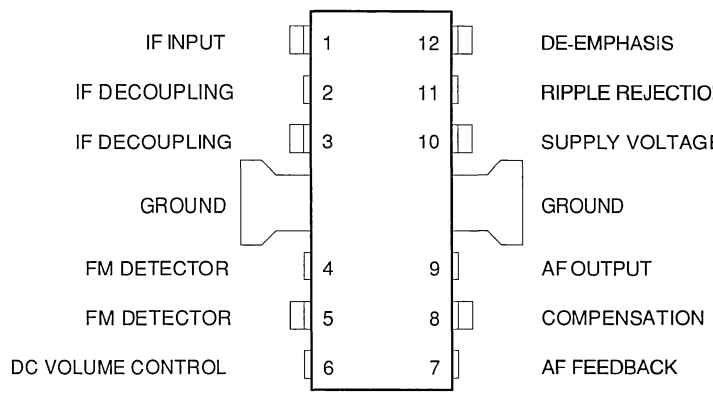
ORDER CODE : TDA1190Z

DESCRIPTION

The TDA 1190Z can give an output power of 4.2 W (d = 10 %) into a 16 Ω load at V_S = 24 V, or 1.5 W (d = 10 %) into an 8 Ω load at V_S = 12 V. This performance, together with the FM-IF section characteristics of high sensitivity, high AM rejection and low distortion, enables the device to be used in almost every type of television receivers.

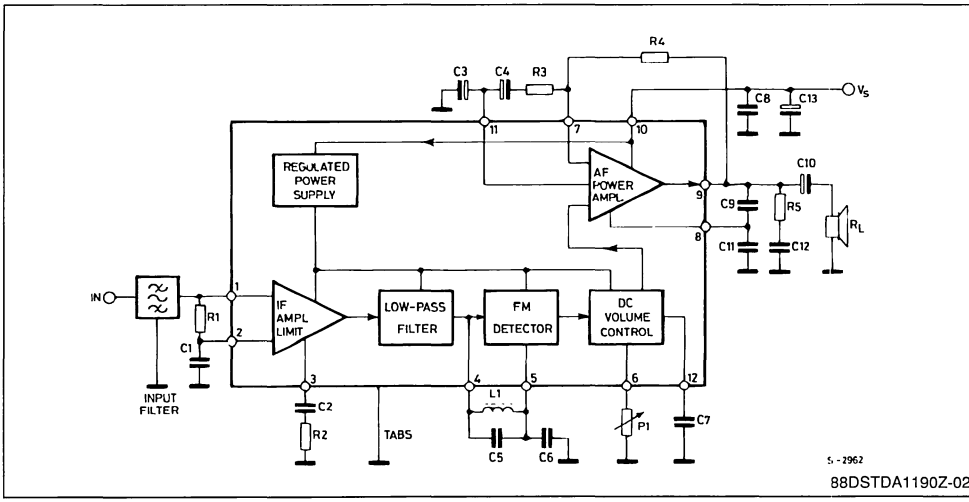
The device has no irradiation problems, hence no external screening is needed.

PUN CONNECTIONS (top view)



91DSTDA1190Z-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 10)	28	V
V_i	Input Signal Voltage (pin 1)	1	V
I_o	Output Peak current (non-repetitive)	2	A
I_o	Output Peak Current (repetitive)	1.5	A
P_{tot}	Power Dissipation : at T_{tab} = 90 °C at T_{amb} = 80 °C (free air)	5 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

TAB-01

THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal Resistance Junction-tab	Max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70*	°C/W

TAB-02

* Obtained with tabs soldered to printed circuit with minimized copper area

ELECTRICAL CHARACTERISTICS

(refer to the test circuit ; V_S = 24 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage (pin 10)		9		28	V
V_o	Quiescent Output Voltage (pin 9)	V_s = 24 V V_s = 12 V	11 5.1	12 6	13 6.9	V V
I_d	Quiescent Drain Current	P_I = 22 kΩ V_s = 24 V V_s = 12 V	11	22 19	45 40	mA mA
P_o	Output Power	d = 10 % f_o = 4.5 MHz V_s = 24 V V_s = 12 V f_m = 400 Hz Δf = ± 25 kHz R_L = 16 Ω R_L = 8 Ω		 4.2 1.5		 W W

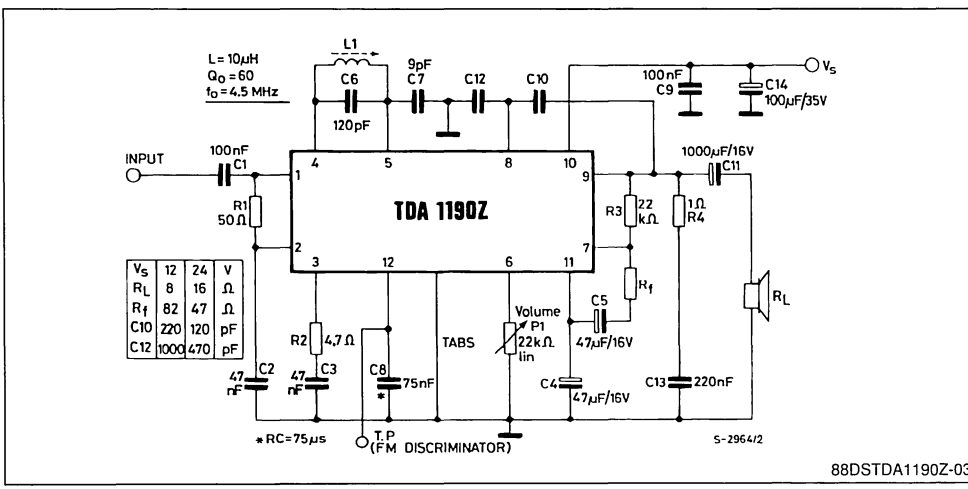
TAB-03

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
P_o	Output Power	d = 2 % f_o = 4.5 MHz V_S = 24 V V_S = 12 V	f_m = 400 Hz Δf = ± 25 kHz R_L = 16 Ω R_L = 8 Ω		 3.5 1.4		 W W
V_i	Input Limiting Voltage (– 3 dB) at Pin 1	f_o = 4.5 MHz	f_m = 400 Hz P_1 = 0 Δf = ± 7.5 kHz		 40	 100	 µV
d	Distortion	P_o = 50 mW f_o = 4.5 MHz V_S = 24 V V_S = 12 V	f_m = 400 Hz Δf = ± 7.5 kHz R_L = 16 Ω R_L = 8 Ω		 0.75 1		 % %
B	Frequency Response of Audio Amplifier (– 3 dB)	R_L = 16 Ω C_{12} = 470 pF R_f = 82 Ω R_f = 47 Ω	C_{10} = 120 pF P_1 = 22 kΩ		 70 to 12000 70 to 7000		 Hz Hz
V_o	Recovered Audio Voltage (pin. 12)	V_i ≥ 1 mV f_m = 400 Hz P_I = 0	f_o = 4.5 MHz Δf = ± 7.5 kHz		 120		 mV
AMR	Amplitude Modulation Rejection	V_i ≥ 1 mV f_m = 400 Hz m = 0.3	f_o = 4.5 MHz Δf = ± 25 kHz		 55		 dB
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i ≥ 1 mV f_o = 4.5 MHz Δf = ± 25 kHz	V_o = 4 V f_m = 400 Hz	 50	 65	 	 dB
R_f	External Feedback Resistance (between pins 7 and 9)					25	kΩ
R_i	Input Resistance (pin 1)	V_i = 1 mV f_o = 4.5 MHz			30		kΩ
C_i	Input Capacitance (pin 1)				5		pF
SVR	Supply Voltage Rejection	R_L = 16 Ω f_{ripple} = 120 Hz P_1 = 22 kΩ			 46		 dB
A	DC Volume Control Attenuation	P_1 = 12 kΩ			90		dB

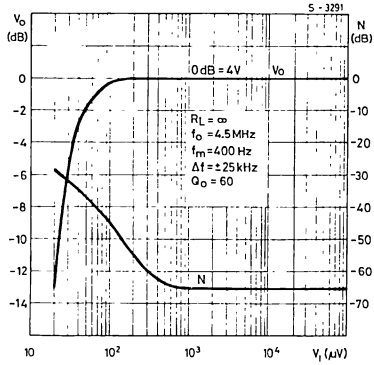
TAB-04

TEST CIRCUIT



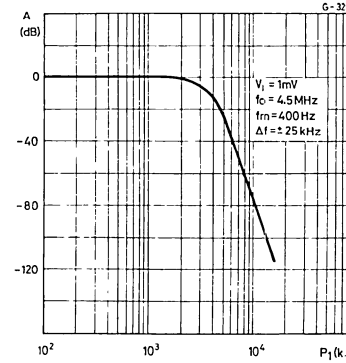
88DSTDA1190Z-03

Figure 1 : Relative Audio Output Voltage and Out-Noise versus Input Signal.



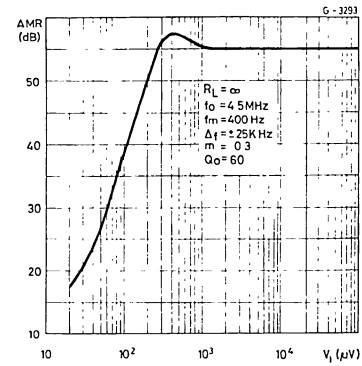
88DSTDA1190Z-04

Figure 2 : Output Voltage Attenuation versus DC Volume Control Resistance.



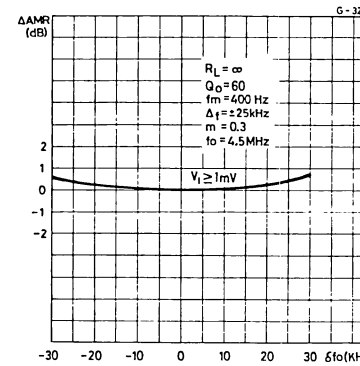
88DSTDA1190Z-05

Figure 3 : Amplitude Modulation Rejection versus Input Signal.



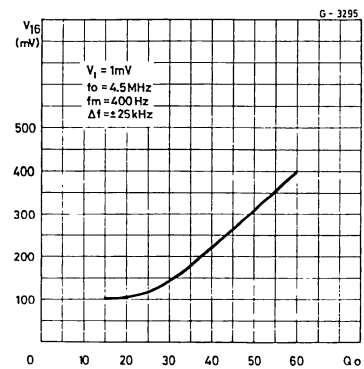
88DSTDA1190Z-06

Figure 4 : Δ AMR versus Tuning Frequency Change.



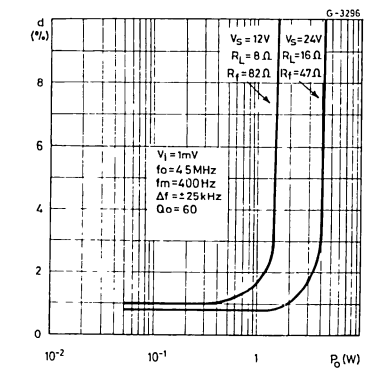
88DSTDA1190Z-07

Figure 5 : Recovered Audio Voltage versus Unloaded Q Factor of the Detector Coil.



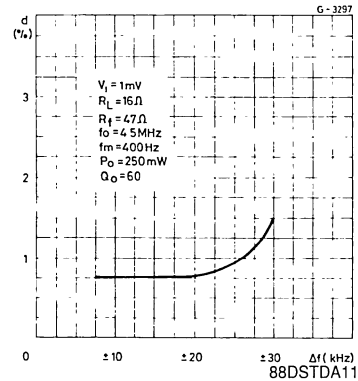
88DSTDA1190Z-08

Figure 6 : Distortion versus Output Power.



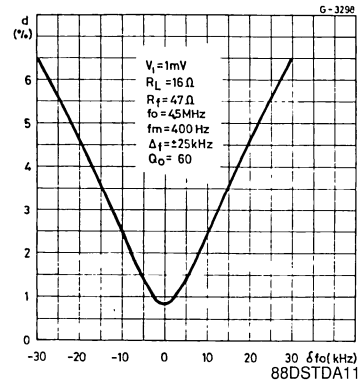
88DSTDA1190Z-09

Figure 7 : Distortion versus Frequency Deviation.



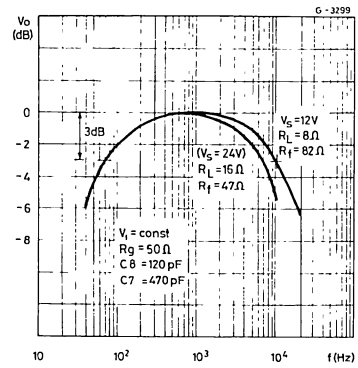
88DSTDA1190Z-10

Figure 8 : Distortion versus Tuning Frequency Change.



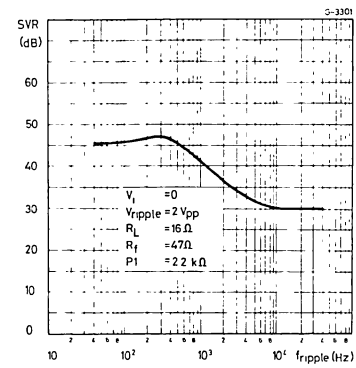
88DSTDA1190Z-11

Figure 9 : Audio Amplifier Frequency Response.



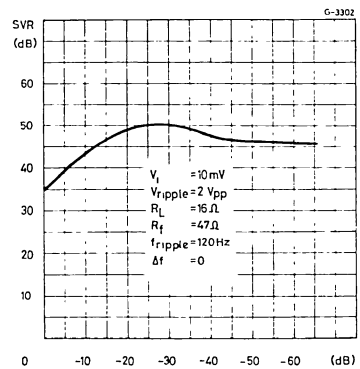
88DSTDA1190Z-12

Figure 10 : Supply Voltage Ripple Rejection versus Ripple Frequency.



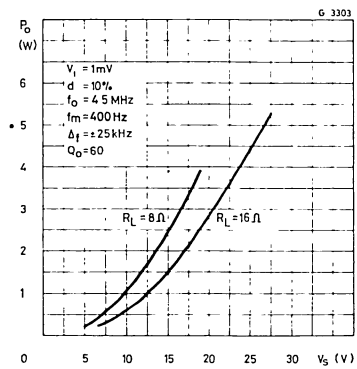
88DSTDA1190Z-13

Figure 11 : Supply Voltage Ripple Rejection versus Volume Control Attenuation.



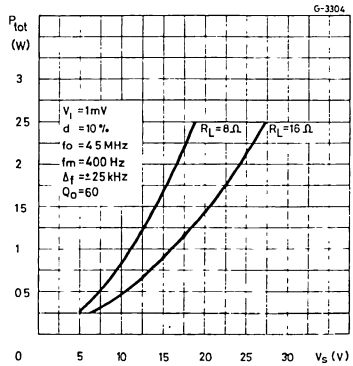
88DSTDA1190Z-145

Figure 12 : Output Power versus Supply Voltage.



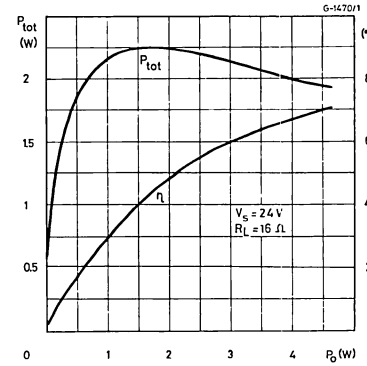
88DSTDA1190Z-15

Figure 13 : Maximum Power Dissipation versus Supply Voltage (sine wave operation).



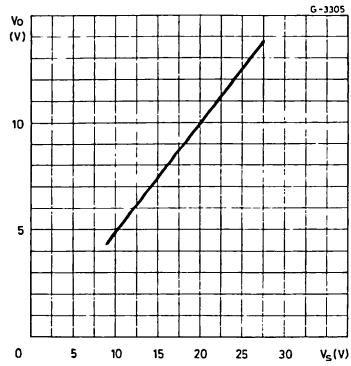
88DSTDA1190Z-16

Figure 14 : Power Dissipation and Efficiency versus Output Power.



88DSTDA1190Z-17

Figure 15 : Quiescent Output Voltage (pin 9) versus Supply Voltage.



88DSTDA1190Z-18

APPLICATION INFORMATION

The electrical characteristics of the TDA 1190Z remain almost constant over the frequency range of 4.5 to 6 MHz, therefore it can be used in all television standard (FM mod.). The TDA 1190Z has a high input impedance, so it can work with a ceramic filter or with a tuned circuit that provide the necessary input selectivity.

The value of the resistors connected to pin 7, determine the AC gain of the audio frequency amplifier. This enables the desired gain to be selected in relation to the frequency deviation at which the output stage of the AF amplifier must enter into clipping. The capacitor connected between pins 9 and 8 determines the upper cut-off frequency of the audio band. If larger bandwidth is required C_{10}, C_{12} must be reduced keeping C_{12}/C_{10} as in fig. 16.

The capacitor connected between pin 12 and ground, toghether with the internal resistor of 10 KΩ, forms the de-emphasis network. The Boucherot cell eliminates the high frequency oscillations caused by inductive load and the wires connecting the loudspeaker.

Figure 16 : Typical Application Circuit.

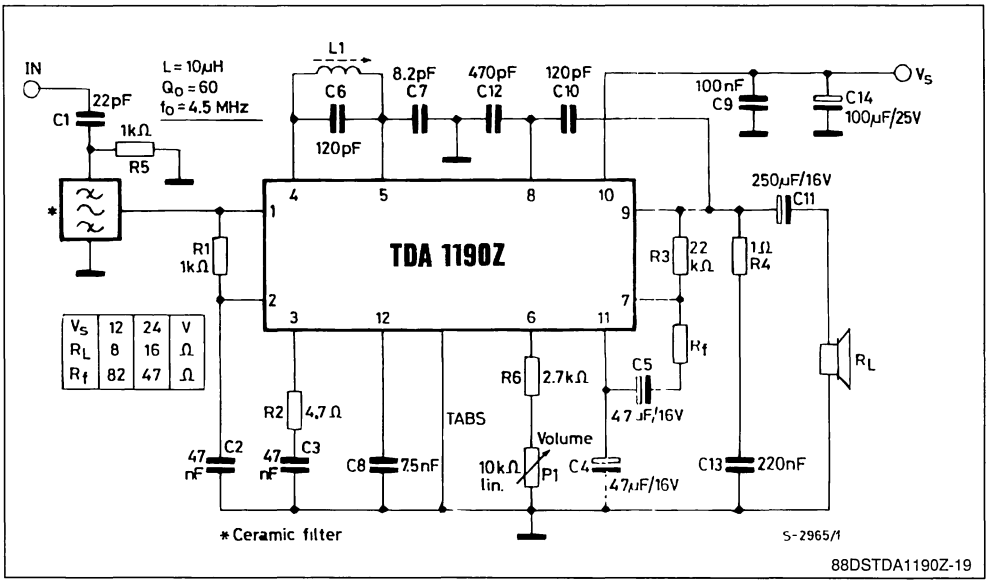
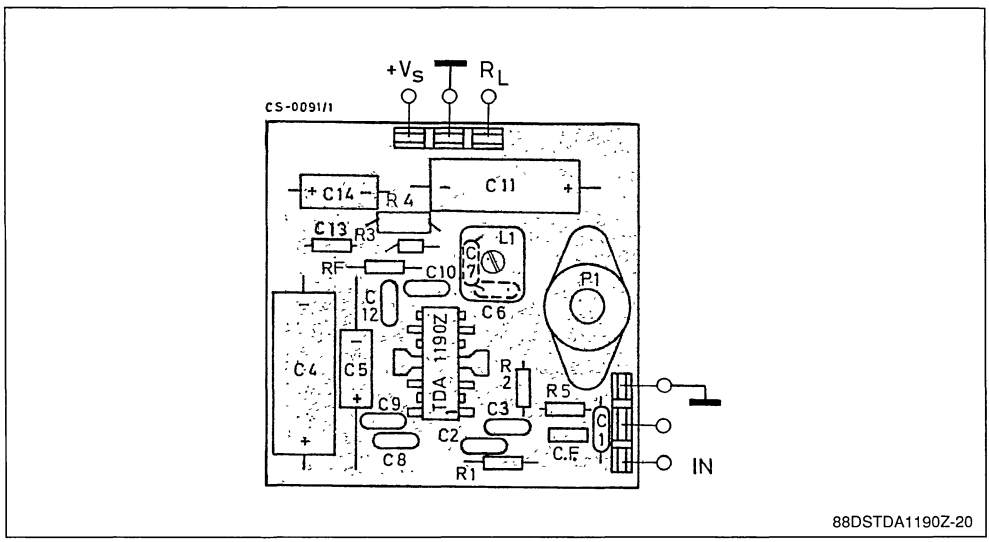


Figure 17 : P.C. Board and Component Layout of the Circuit Shown in Fig. 16.



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA1190Z can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 18) or to an external heatsink (fig. 19).

The diagram of figure 20 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "l" of two equal square copper areas having a thickness of 35 µ (1.4 mils).

During soldering the tab temperature must not exceed 260 °C and the soldering time mumst not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 18 : Example of P.C. Board Copper Area Which is Used as Heatsink.

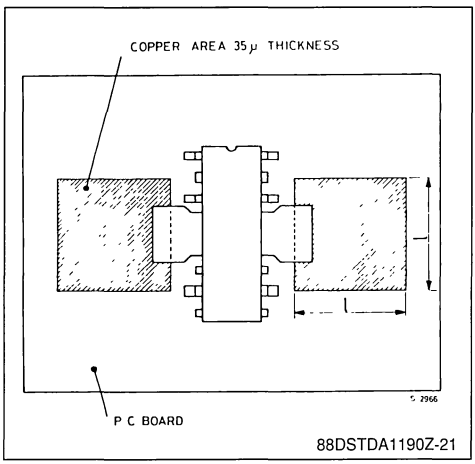


Figure 19 : External Heatsink Mounting Example.

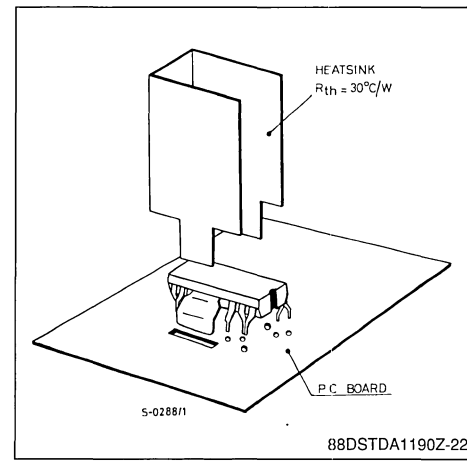


Figure 20 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance versus Side "l" .

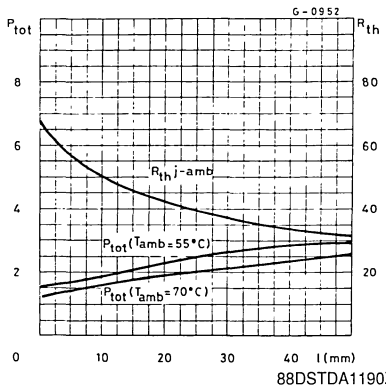
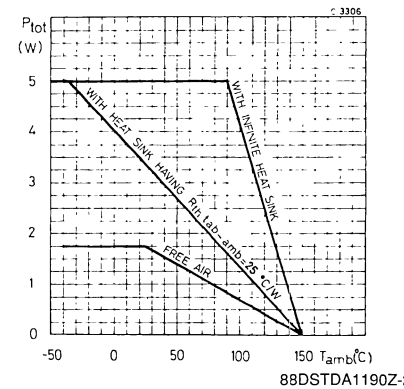
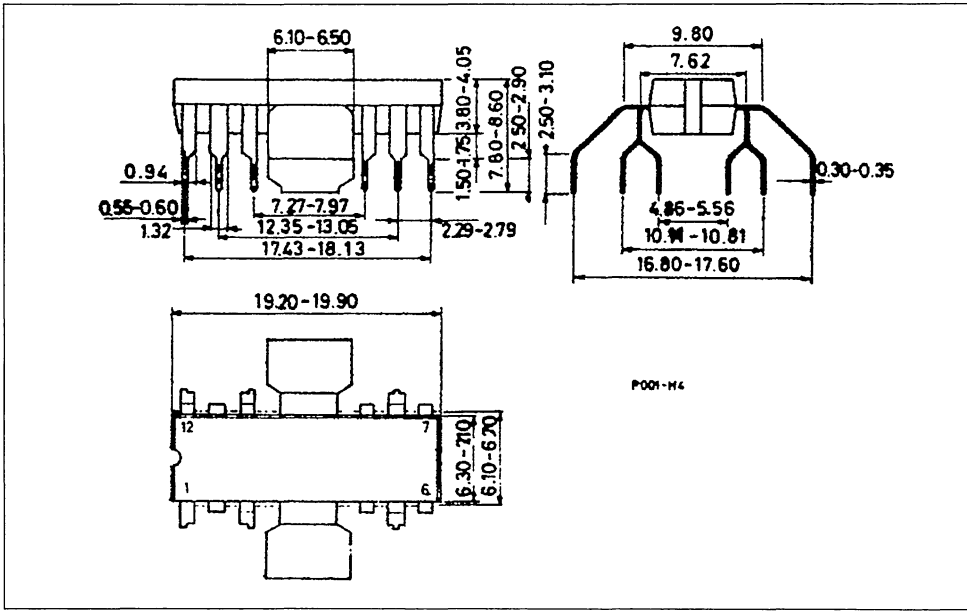


Figure 21 : Maximum Allowable Power Dissipation versus Ambient Temperature.



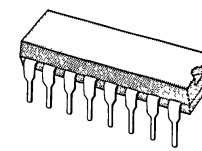
PACKAGE MECHANICAL DATA

12 PINS - PLASTIC FINDIP



IF AMPLIFIER WITH DEMODULATOR AND AFC

- SUPPLY VOLTAGE : 12 V TYP
- SUPPLY CURRENT : 50 mA TYP
- I.F. INPUT VOLTAGE SENSITIVITY AT F = 38.9 MHz : 85 μV_{RMS} TYP
- VIDEO OUTPUT VOLTAGE (white at 10 % of top synchro) : 2.7 V_{pp} TYP
- I.F. VOLTAGE GAIN CONTROL RANGE : 64 dB TYP
- SIGNAL TO NOISE RATIO AT V_I = 10 mV : 58 dB TYP
- A.F.C. OUTPUT VOLTAGE SWING FOR Δf = 100 kHz : 10 V TYP



DIP16
(Plastic Package)

ORDER CODE : TDA2540-TDA2541

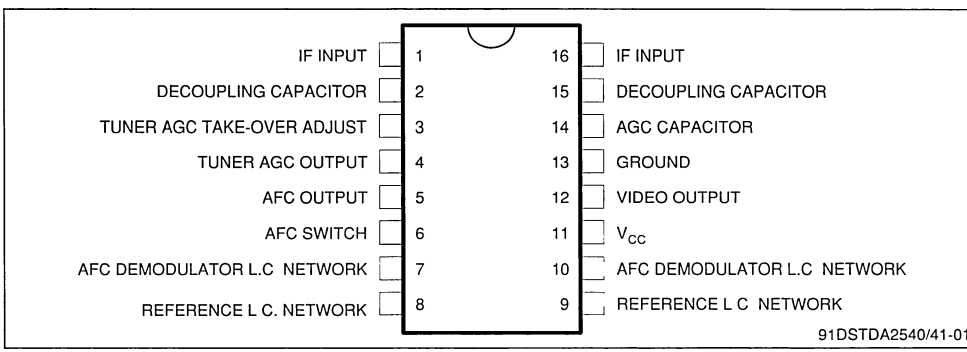
DESCRIPTION

The TDA2540 and 2541 are IF amplifier and A.M. demodulator circuits for colour and black and white television receivers using PNP or NPN tuners. They are intended for reception of negative or positive modulation CCIR standard.

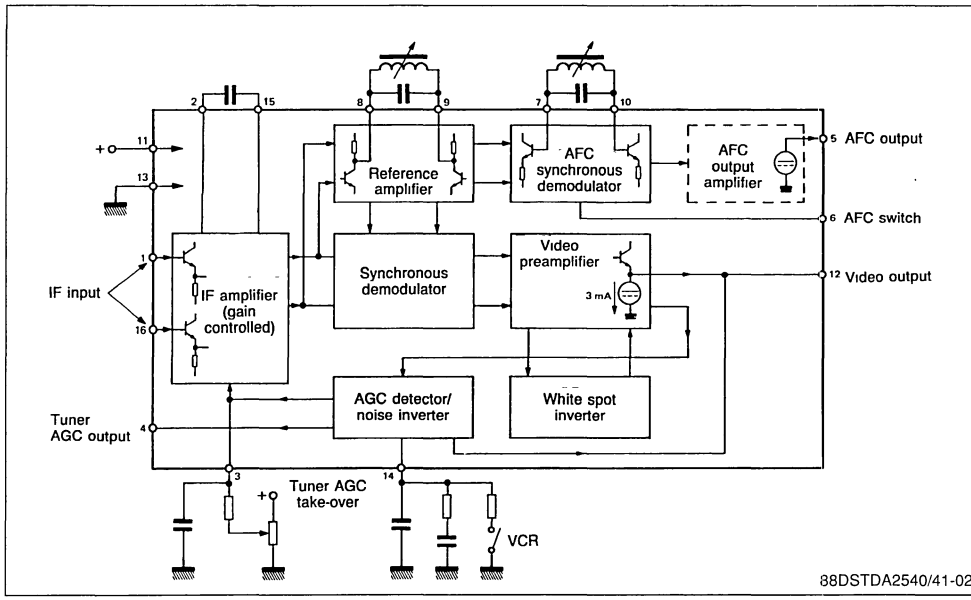
They incorporate the following functions :

- Gain controlled amplifier
- Synchronous demodulator
- White spot inverter
- Video preamplifier with noise protection
- Switchable AFC
- AGC with noise gating
- Tuner AGC output (NPN tuner for 2540)-(PNP tuner for 2541)
- VCR switch for video output inhibition (VCR play back)

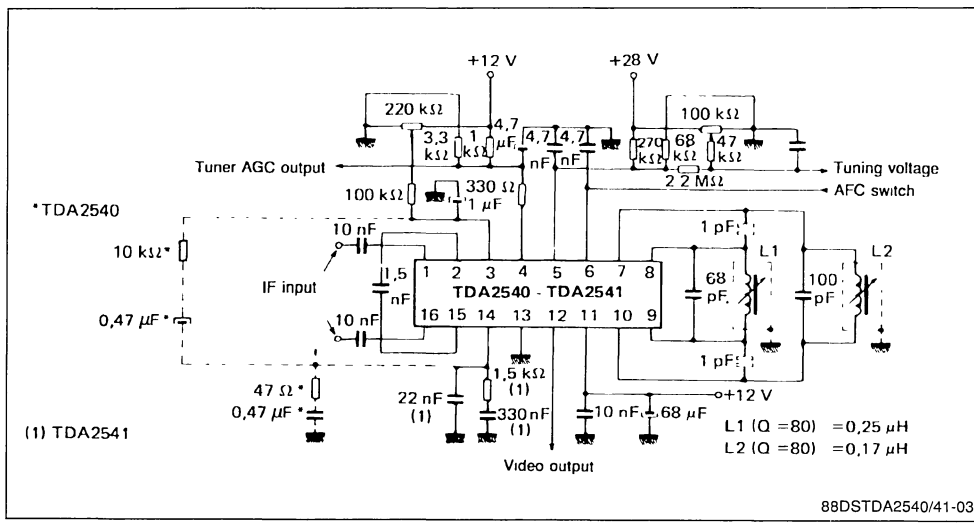
PIN CONNECTIONS



BLOCK DIAGRAM



APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V (11–13)	Supply Voltage	13.8	V
V (4–13)	Tuner A.G.C. Voltage	12	V
P_{tot}	Power Dissipation	900	mW
T_{stg}	Storage Temperature	– 55 to + 125	°C
T_{amb}	Operating Ambient Temperature	0 to + 70	°C

TAB-01

THERMAL DATA

$R_{th(j-a)}$	Junction - ambient Thermal Resistance	70	°C/W

TAB-02

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V (11 – 13) = 12 V; f = 38.9 MHz (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V (11-13)	Supply Voltage Range	10.2	12	13.8	V
I_{11}	Supply Current		50	60	mA
V (1-16)	IF Input Voltage Sensitivity	60	85	180	μVRMS
	Max Input Voltage (pins 1-16)		140		mV
V (12-13)	Video Output Voltage		2.7		V_{pp}
Z (1-16)	Differential Input Impedance (in parallel with 2 pF)		2		kΩ
V (12-13)	Zero Signal Output Level	5.7	6	6.3	V
V (12-13)	Top Synchro Output Level	2.9	3.07	3.2	V
ΔG_V	IF Voltage Gain Control Range	52	64		dB
S/N	Signal to Noise Ratio (V_I = 10 mV) (see note 1)	50	58		dB
B	Bandwidth of Video Amplifier (– 3 dB)		6		MHz
dG	Differential Gain		4	10	%
dϕ	Differential Phase		2	10	%
V (12-13)	Carrier Signal at Video Output (V_I = 10 mV)		4	30	mVRMS
V (12-13)	2nd Harmonic of Carrier at Video Output (V_I = 10 mV)		20	30	mVRMS
	Intermodulation at 1.1 MHz (blue) (see figures 2 and 3)	46	60		dB
	Intermodulation at 1.1 MHz (yellow) (see figures 2 and 3)	46	50		dB
	Intermodulation at 3.3 MHz (blue) (see figures 2 and 3)	46	54		dB
V (14-13)	VCR Switches Off Output at : (VCR = low Level)			1.1	V
	White Spot Inverter Threshold Level (see figure 1)		6.6		V
	White Spot Insertion Level (see figure 1)		4.7		V

TAB-03

Note : 1 $S/N = \frac{V_O \text{ (black to white)}}{V_N \text{ (RMS at B = 5 MHz)}}$ (dB)

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Noise Inverter Threshold Level (see figure 1)		1.8		V
	Noise Insertion Level (see figure 1)		3.8		V
I 4	Tuner AGC output Current Range		0 to 10		mA
V (14-13)	Tuner AGC Output Voltage			0.3	V
I 4	Tuner AGC Output Leakage Current TDA2541 V 14-13 = 11 V V 4-13 = 12 V TDA2540 V 14-13 = 5 V V 4-13 = 12 V			15	µA
ΔV (5-13)	AFC Output Voltage Swing (Δf = 100 kHz)	10	11		V
Δf	Change of Frequency at AFC Output (voltage swing of 10 V)		100	200	kHz
V (6-13)	AFC Switches OFF (AFC = low level) at :			2.5	V
V (6-13)	AFC Switches LOW (AFC = High level) at :	3.2			V
V (5-13)	AFC Zero = Signal Output Voltage (minimum gain)	4	6	8	V

TAB-04

Note : 1. $S/N = \frac{V_O \text{ (black to white)}}{V_N \text{ (RMS at B = 5 MHz)}}$ (dB)

Figure 1 : Video Output Waveform Showing White Spot and Noise Inverter Threshold Levels.

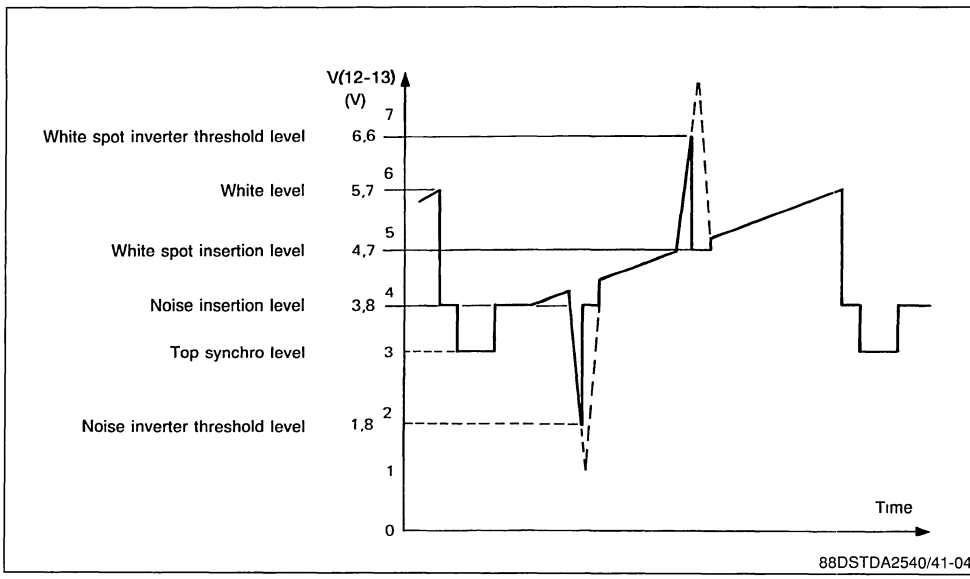


Figure 2 : Input Conditions for Intermodulation Measurements.

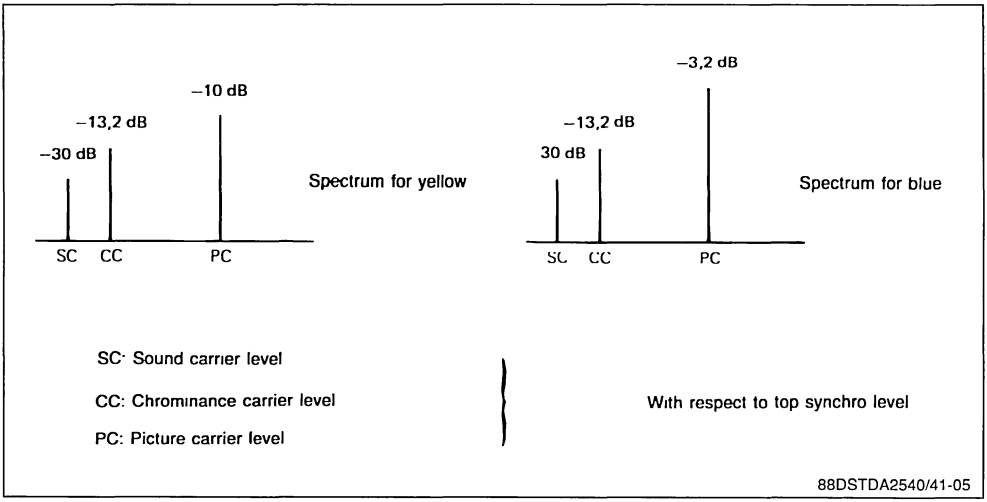


Figure 3 : Test Set-up for Intermodulation.

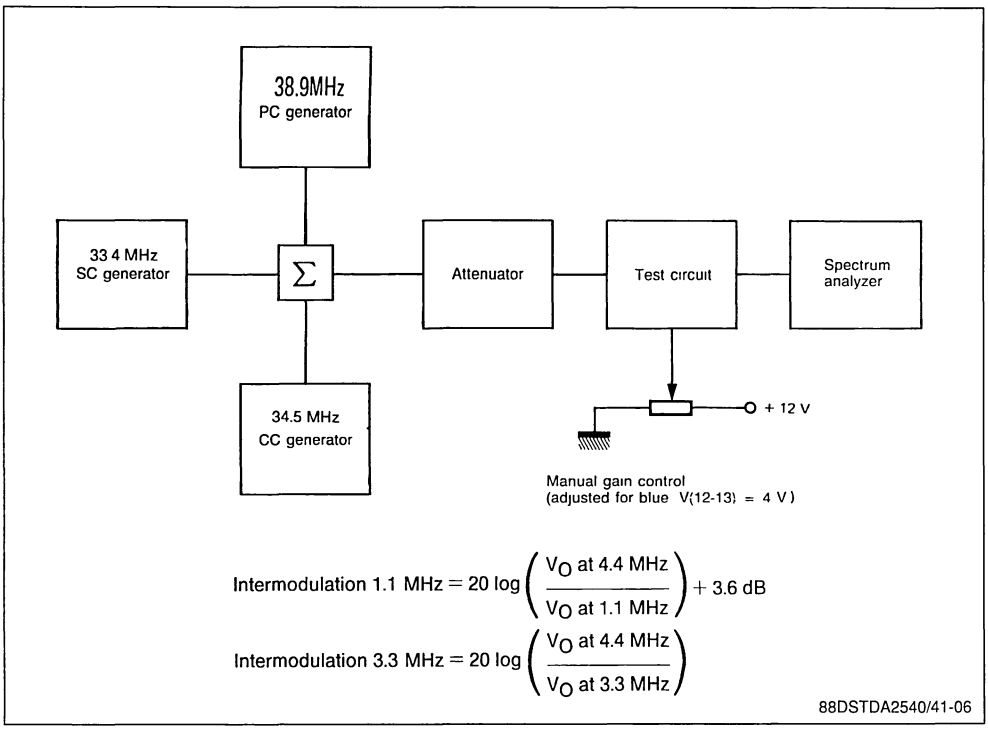


Figure 4 : AFC Voltage Versus Frequency V(5-13).

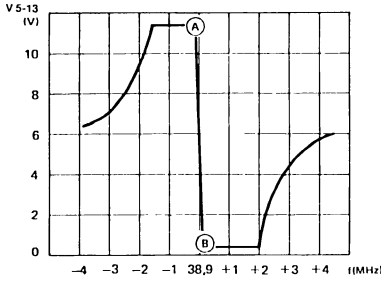


Fig. 4 — AFC VOLTAGE VERSUS FREQUENCY V 5-13

88DSTDA2540/41-07

Figure 5 : AFC Voltage Versus Frequency V(5-13).

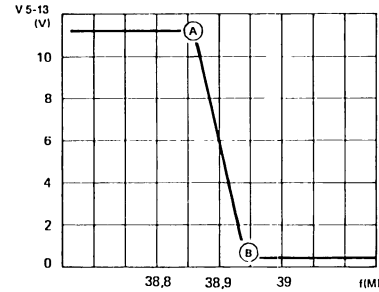


Fig. 5 — AFC VOLTAGE VERSUS FREQUENCY V 5-13

88DSTDA2540/41-08

Figure 6 : Signal/Noise Ratio Versus Input Voltage V(1-16).

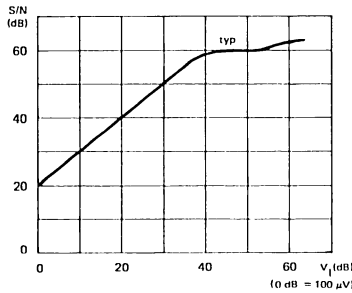
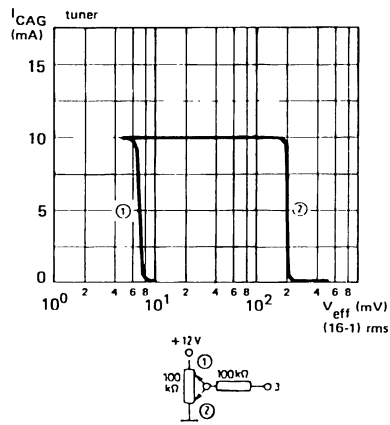


Fig 6 — SIGNAL/NOISE RATIO VERSUS INPUT VOLTAGE V 1-16

88DSTDA2540/41-09

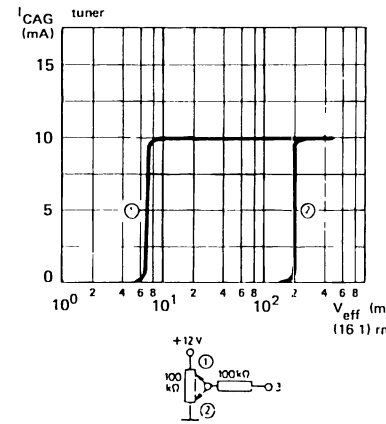
Figure 7 : AGC Tuner Current Curve.

TDA2540



88DSTDA2540/41-10

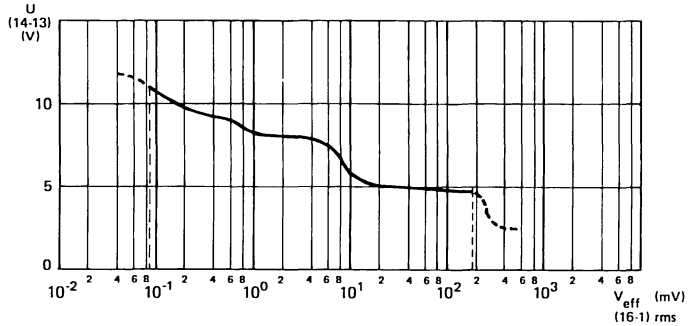
TDA2541



88DSTDA2540/41-11

Figure 7 : AGC Tuner Current Curve (continued).

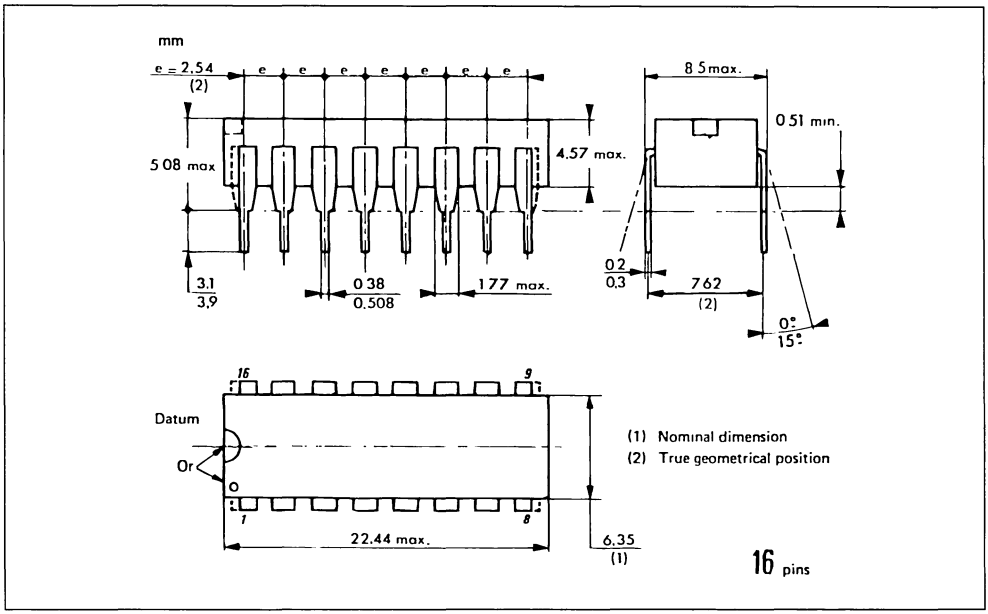
TDA2540-TDA2541



88DSTDA2540/41-12

PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

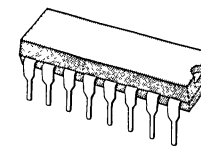
TDA2593

SYNCHRO AND HORIZONTAL DEFLECTION CONTROL FOR COLOR TV SET

- LINE OSCILLATOR (two levels switching)
- PHASE COMPARISON BETWEEN SYNCHRO-PULSE AND OSCILLATOR VOLTAGE Ø 1, ENABLED BY AN INTERNAL PULSE, (better parasitic immunity)
- PHASE COMPARISON BETWEEN THE FLY-BACK PULSES AND THE OSCILLATOR VOLTAGE Ø 2
- COINCIDENCE DETECTOR PROVIDING A LARGE HOLD-IN-RANGE
- FILTER CHARACTERISTICS AND GATE SWITCHING FOR VIDEO RECORDER APPLICATION
- NOISE GATED SYNCHRO SEPARATOR
- FRAME PULSE SEPARATOR
- BLANKING AND SAND CASTLE OUTPUT PULSES
- HORIZONTAL POWER STAGE PHASE LAGGING CIRCUIT
- SWITCHING OF CONTROL OUTPUT PULSE WIDTH
- SEPARATED SUPPLY VOLTAGE OUTPUT STAGE ALLOWING DIRECT DRIVE OF SCR'S CIRCUIT
- SECURITY CIRCUIT MAKES THE OUTPUT PULSE SUPPRESSED WHEN LOW SUPPLY VOLTAGE

DESCRIPTION

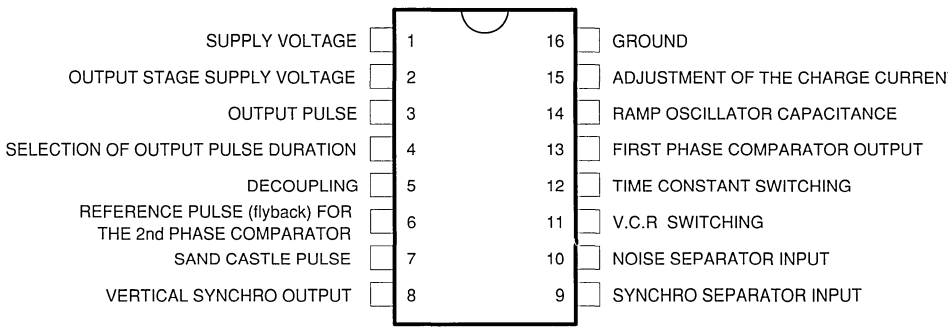
The TDA2593 is a circuit intended for the horizontal deflection of color TV sets, supplied with transistors or SCR'S.



DIP16
(Plastic Package)

ORDER CODE : TDA2593

PIN CONNECTIONS



91DSTDA2593-01

MAIN CHARACTERISTICS

Symbol	Parameter	Typ.	Unit
V(1–16)	Supply Voltage	12	V
I(1)	Supply Current	30	mA
	Input Signals		
V(9–16) (pp)	Synchro Separator Input Voltage	3 to 4	V
V(10-16) (pp)	Noise Separators Input Voltage	3 to 4	V
	Control Voltage of the Output Pulse Switching Circuit		
V(4–16)	t = 7 µs (thyristor)	9.4 to V(1–16)	V
V(4–16)	t = 14 µs + t_d (transistor)	0 to 3.5	V
V(4–16)	t = 0 (V(3–16) = 0)	5 4 to 5.6	V
	Output Signals		
V(8–16) (pp)	Frame Synchro Pulse	11	V
V(7–16) (pp)	Sandcastle Pulse	11	V
V(3–16) (pp)	Horizontal Driver Stage Control Pulse	10.5	V

TAB-01

ABSOLUTE MAXIMUM RATINGS

Maximum Ratings According to CEI 134 Data Sheet

Symbol	Parameter	Value	Unit
V(1–16)	Supply Voltage to Pin 1	13.2	V
V(2–16)	Supply Voltage to Pin 2	18	V
V(4–16)	Voltage to Pin 4	13.2	V
V(9–16)	Voltage to Pin 9	± 6	V
V(10–16)	Voltage to Pin 10	± 6	V
V(11–16)	Voltage to Pin 11	13 2	V
$I_{2M} = -I_{3M}$	Current at Pins 2 and 3 (with thyristor)	650	mA
$I_{2M} = I_{3M}$	Current at Pins 2 and 3 (with transistor)	400	mA
I(4)	Current to Pin 4	1	mA
I(6)	Current to Pin 6	± 10	mA
I(7)	Current to Pin 7	– 10	mA
I(11)	Current to Pin 11	2	mA
P_{tot}	Power Dissipation	800	mW
T_{amb}	Operating Ambient Temperature	– 20 to + 70	°C
T_{stg}	Storage Temperature	– 25 to + 125	°C

TAB-02

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C, V1–V16 = 12 V (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input Signals Synchro Separator (pin 9)				
V(9–16)	Input Threshold Voltage		0.8		V
I(9)	Input Threshold Current			5	µA
I(9)	On-state Input Current		5 to 100		µA
I(9)	Disconnect Input Current	100	150		µA
I(9)	Off-state Input Current (V(9–16) = – 5 V)			– 1	µA
V(9)	Video Input Signal (positive synchro pulses) (note 1)		3 to 4		Vpp
V(10–16)	Noise Separator (pin 10) Input Threshold Voltage		1.4		V
I(10)	Input Threshold Current	100	150		µA
I(10)	Input Current		5 to 100		µA
I(10)	Off-state Input Current (V(10–16) = – 5 V)			– 1	µA
V(10)	Video Input Signal (positive synchro pulses) (note 1)		3 to 4		Vpp
V(10)	Allowed superimposed parasitic signal			7	V
V(6–16)	Fly-back Pulse (pin 6) Input Threshold Voltage		1.4		V
V(6)	Input Limitation Level		– 0.7 and + 1.4		V
I(6)	Input Current	0.01	1	2	mA
V(4–16)	Output Pulse Width Control Switch (pin 4) Input Voltage t = 7 µs (thyristor)		9.4 to V(1–16)		V
V(4–16)	t = 14 µs + t_d (transistor)		0 to 3.5		V
V(4–16)	t = 0 (V3–16 = 0) (note 2)		5.4 to 6.6		V
I(4)	Input Current t = 7 µs (thyristor)	200			µA
I(4)	t = 14 µs + t_j (transistor)	200			µA
I(4)	t = 0 (V3–16 = 0)		0		
	Video Recorder Switch (pin 11)				
V(11–16)	Input Voltage (pin 11 low level)		0 to 2.5		V
	(pin 11 to + V_{CC})		9 to V(1–16)		V
I(11)	Input Current (pin 11 low level)			200	µA
I(11)	(pin 11 to + V_{CC})			2	mA
V(8–16)	Output Signals Frame Synchro Pulses (positive) (pin 8) Output Voltage (peak value)	10	11		V
R(8)	Output Impedance		2		kΩ
t_{on}	Delay Between Leading Edge of Input Signal and Leading Edge of Output Signal		15		µs
t_{off}	Delay Between Trailing Edge of Input Signal and Trailing Edge of Output Signal		15		µs

TAB-03

Notes : 1 Allowed range 1 to 7 V
2. Or pin 4 not connected

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

T_{amb} = 25 °C, V_1–V_{16} = 12 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V(7–16)	Sandcastle Pulse (positive) (pin7) Output Voltage (peak valve)	10	11		V
R(7)	Output Impedance		70		Ω
I(7)	Output Current During Trailing Edge		2		mA
t_7	Sandcastle Pulse Width (V7 = 7 V)	3.7		4.3	µs
Δ_t	Phase Between Middle Input Synchro Pulse and Leading Edge of Sandcastle Pulse (V7 = 7 V)	2.15		3.15	µs
V(7–16)	Fly-back Blanking Pulse (pin 7) Output Voltage (peak value)	4		5	V
R(7)	Output Impedance		70		Ω
I(7)	Output Current During Trailing Edge		2		mA
V(3–16)	Control Pulse for Horizontal Driver (positive) (pin 3) Output Voltage (peak value)		10.5		V
R(3) R(3)	Output Impedance (leading edge) (trailing edge)		2.5 20		Ω Ω
t_3 t_3	Control Pulse Width V4 = 9.4 to V(1–16) V4 = 0 to 4 V (note 3)	5.5	 14 + t_c	8.5	µs µs
V(1–16)	Control pulse is disabled for		4		V
t_z	Overall Phase Relation Ship Phrase Between Middle Synchro Pulse and Middle Fly-back Pulse t_r = 12 µs (note 4)	1.9		3.3	µs
ΔI/Δt	Sensitivity to Current Adjust		30		µA/µs
V(14–16) V(14–16)	Oscillator (pins 14 and 15) Threshold Voltage (low level) (high level)		 4.4 7.6		 V V
I(14)	Current Generator		± 0.47		mA
f	Free Running Frequency (C_{osc} = 4700 pF R_{osc} = 12 kΩ)		15625		Hz
Δf	Tolerance on Frequency (note 5)			± 5	%
Δf/15	Frequence Control Sensitivity		31		Hz/µA
Δf	Spread of Frequency		± 10		%
$\frac{\Delta f/f}{\Delta V/V \text{ nom.}}$	Influence of Supply Voltage on Frequency (note 5)			≃ 0.05	%
Δf	Frequency change when decreasing the supply down to 5 V V(1–16) = 5V (note 5)			± 10	%
T	Frequency Temperature Coefficient (note 5)			± 10^{-4}	Hz/°C
V(13–16)	Phase Comparator ø 1 (pin 13) Control Voltage Range		3.8 to 8.2		V
I(13) I(13)	Control Current (peak value) Off-state Current (V (13–16) = 4 to 8 V)		± 1.9 to ± 2.3	 – 1	mA µA

TAB-04

Notes : 3 With t_r = 12 µs

4 The adjustement of overall phase relation (and output pulse leading edge position) is automatically performed by phase comparator Ø 2 If additional adjustement is needed, a current have to be imposed at pin 5

5. Tolerance of peripheral components not included

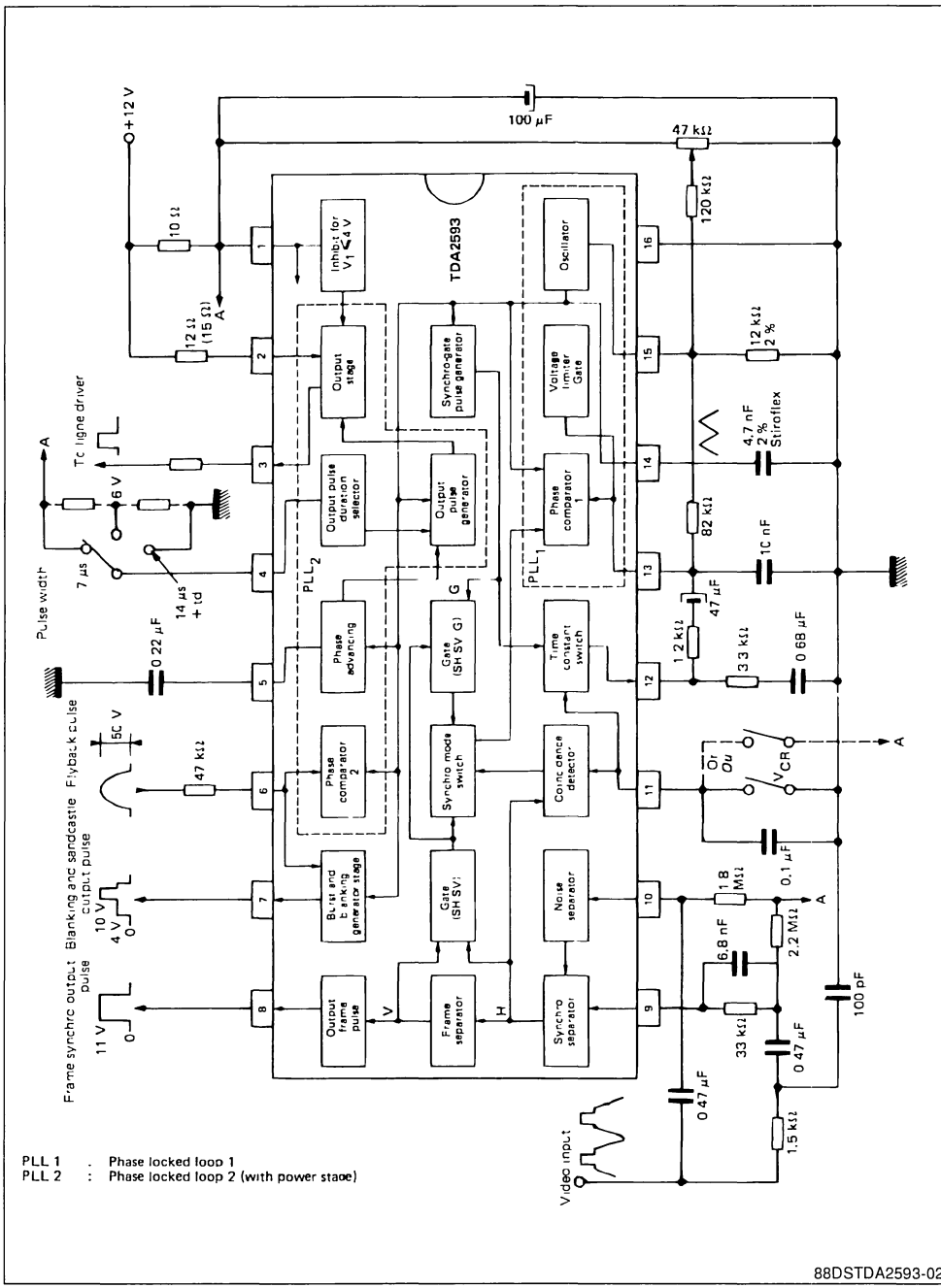
ELECTRICAL OPERATING CHARACTERISTICS (cont'd)
T_{amb} = 25 °C, V_1–V_{16} = 12 V (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit
R(13) R(13)	Output Impedance (V(13–16) = 4 to 8 V (note 6)) (V(13–16) < 3.8 V cr > 8.2 V (note 7))		High Low		
	Control Sensibility		2		kHz/µs
Δf	Catchıng and Holding Range		± 780		Hz
Δf/f	Catchıng and Holding Range Tolerance (note 5)		± 10		%
V(5–16)	Phase Comparator ϕ 2 and Phase-shift (pın 5) Control Voltage Range		5 4 to 7.6		V
I(5)	Control Current (peak value)		± 1		mA
I(5)	Off-state Output Current (V (5–16) = 5.4 to 7.6 V)			– 5	µA
R(5) R(5)	Output Impedance (V (5–16) = 5.4 to 7.6 V (note 6)) (V (5–16) < 5.4 V or > 7.6 V)		High 8		kΩ
t_d	Max. delay Between Output Pulse Leading Edge and Fly-back Pulse Trailing Edge (t_r = 12 µs)			15	µs
$\Delta_t/\Delta t_d$	Static Control Error			0.2	%
V(11–16)	Coıncıdence Detector (pin 11) Output Voltage		0.5 to 6		V
I(11) I(11)	Output Current (without coïncidence) (wıth coıncıdence)		0.1 – 0.5		mA mA
V(12–16)	Time Constant Switch (pin 12) Output Voltage		6		V
I(12)	Output Current		± 1		mA
R(12) R(12)	Output Impedance (V (11–16) = 2.5 to 7 V) (V (11–16) < 1.5 or > 9 V)		100 60		Ω kΩ
t	Pulse Generator (ınternal) Pulse Wıdth		7.5		µs

Notes : 6 Current generator
7 Emitter-follower

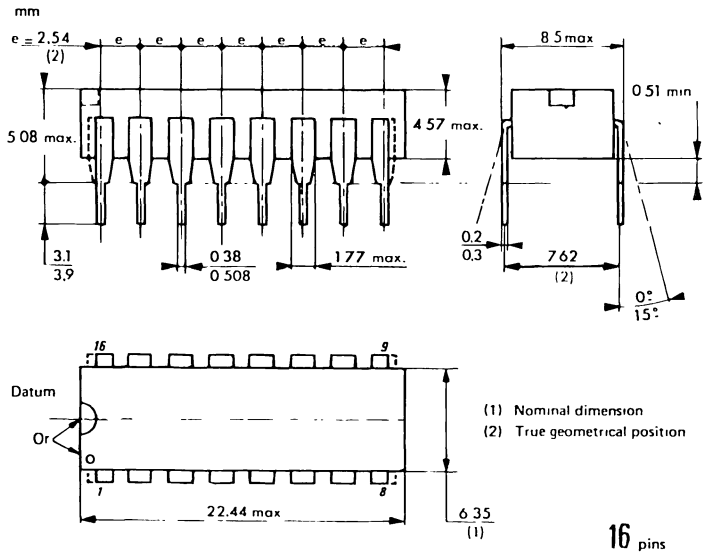
TAB-05

BLOCK DIAGRAM AND TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP



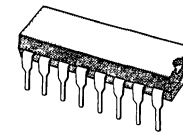
SGS-THOMSON MICROELECTRONICS

TDA3190

COMPLETE TV SOUND CHANNEL

The TDA3190 is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It performs all the functions needed for the TV sound channel :

- IF LIMITER AMPLIFIER
- ACTIVE LOW-PASS FILTER
- FM DETECTOR
- DC VOLUME CONTROL
- AF PREAMPLIFIER
- AF OUTPUT STAGE



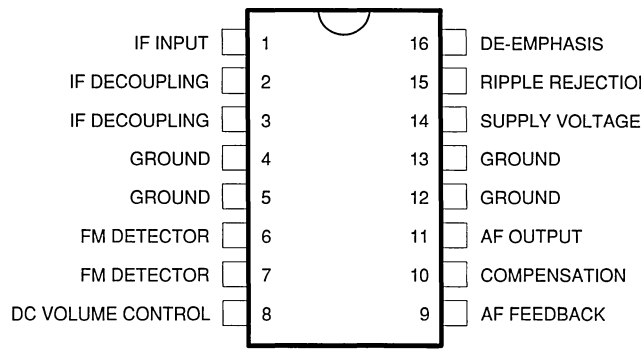
DIP16
(Plastic Package)

ORDER CODE : TDA3190

DESCRIPTION

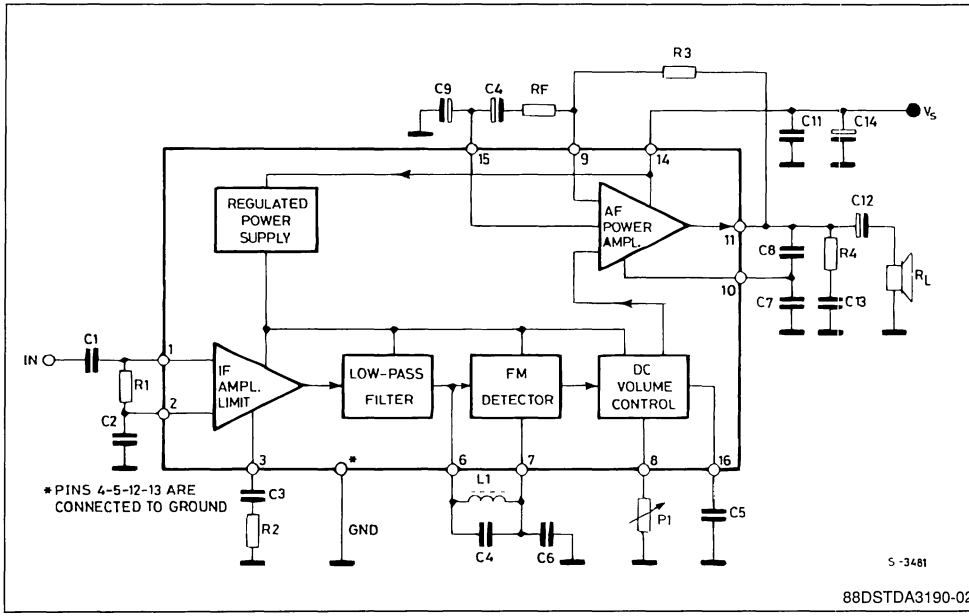
The TDA3190 can give an output power of 4.2 W (d = 10 %) into a 16 Ω load at V_S = 24 V, or 1.5 W (d = 10 %) into an 8 Ω load at V_S = 12 V. This performance, together with the FM-IF section characteristics of high sensitivity, high AM rejection and low distortion, enables the device to be used in almost every type of television receivers.
The device has no irradiation problems, hence no external screening is needed.
The TDA3190 is a pin to pin replacement of TDA1190Z.

PIN CONNECTIONS



91DSTDA3190-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 10)	28	V
V_i	Input Signal Voltage (pin 1)	1	V
I_o	Output Peak Current (non-repetitive)	2	A
I_o	Output Peak Current (repetitive)	1.5	A
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C (free air)	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

TAB-01

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80*	°C/W

TAB-02

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 24V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage (pin 14)		9		28	V
V_o	Quiescent Output Voltage (pin11)	V_s = 24 V V_s = 12 V	11 5.1	12 6	13 6.9	V V
I_d	Quiescent Drain Current	P_1 = 22 KΩ V_s = 24 V V_s = 12 V	11	22 19	45 40	mA mA
Po	Output Power	d = 10 % f_m = 400 Hz f_o = 4.5 MHz Δf = ± 25 KHz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 4.2 1.5		 W W
		d = 2 % f_m = 400 Hz f_o = 4.5 MHz Δf = ± 25 KHz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 3.5 1.4		 W W
V_i	Input Limiting Voltage (– 3dB) atPin 1	f_o = 4.5 MHz Δf = ± 7.5 KHz f_m = 400 Hz P_1 = 0		 40	 100	 µV
d	Distortion	P_o = 50 mW f_m = 400 Hz f_o = 4.5 MHz Δf = ± 7.5 KHz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 0.75 1		 % %
B	Frequency Response of audio amplifier (– 3 dB)	R_L = 16 Ω C_8 = 120 pF C_7 = 470 pF P_1 = 22 KΩ R_f = 82 Ω R_f = 47 Ω		 70 to 1200 70 to 7000		 Hz Hz
V_o	Recovered Audio Voltage (pin16)	V_i ≥ 1 mV f_o = 4.5 MHz f_m = 400 Hz Δf = ± 7.5 KHz P_1 = 0		 120		 mV
AMR	Ampliture Modulation Rejection	V_i ≥ 1 mV f_o = 4.5 MHz f_m = 400 Hz Δ_f = ± 25 KHz m = 0.3		 55		 dB
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i ≥ 1 mV V_o = 4 V f_o = 4.5 MHz f_m = 400 Hz Δf = ± 25 KHz	50	65		dB
R_3	External Feedback Resistance (betweenpins9and11)				25	KΩ
R_i	Input Resistance (pin1)	V_i = 1 mV fo = 4.5 MHz		30		KΩ
C_i	Input Capacitance (pin1)			5		pF
SVR	Supply Voltage Rejection	R_L = 16 Ω f_{ripple} = 120 Hz P_1 = 22 KΩ		 46		 dB
A_v	DC Volume Control Attenuation	P_1 = 12 KΩ		90		dB

TAB-03

TEST CIRCUIT

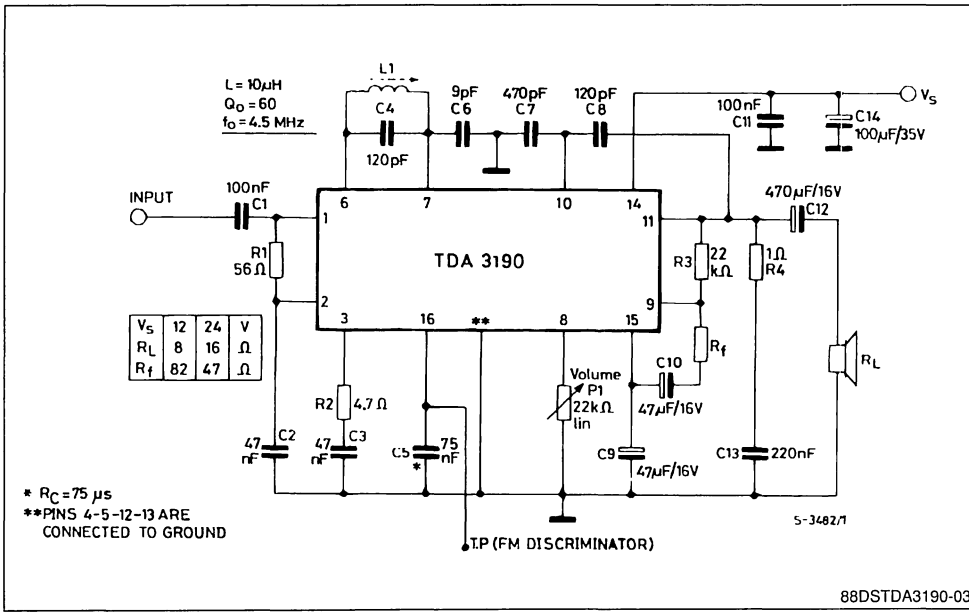
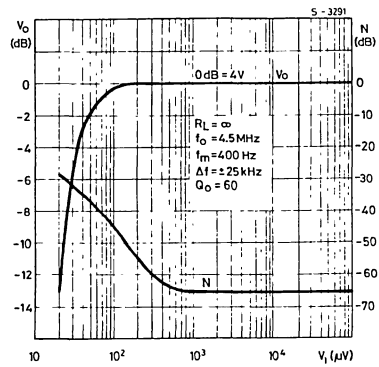
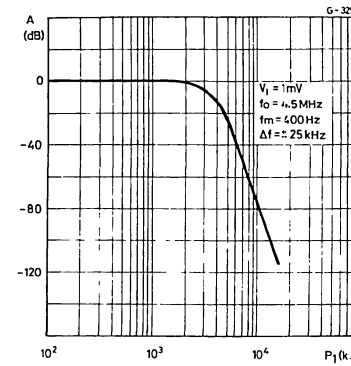


Figure 1 : Relative Audio Output Voltage and Output Noise vs. Input Signal.



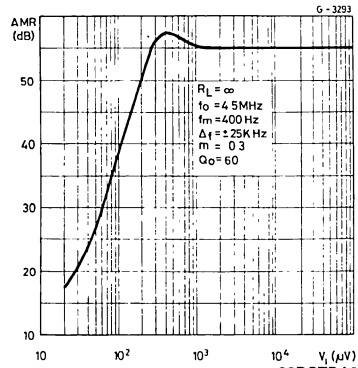
88DSTDA3190-04

Figure 2 : Output Voltage Attenuation vs. DC Volume Control Resistance.



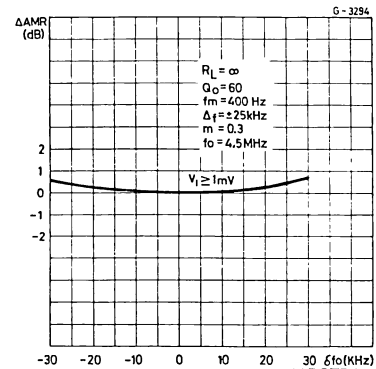
88DSTDA3190-05

Figure 3 : Amplitude Modulation Rejection vs. Input Signal.



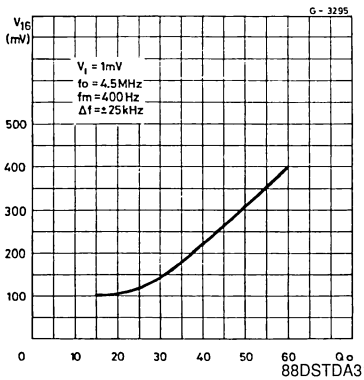
88DSTDA3190-06

Figure 4 : Δ AMR vs. Tuning Frequency Change.



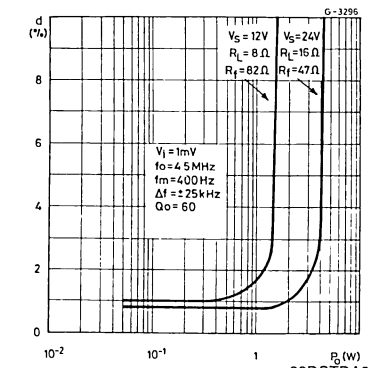
88DSTDA3190-07

Figure 5 : Recovered Audio Voltage vs. Unloaded Q Factor of the Detector Coil.



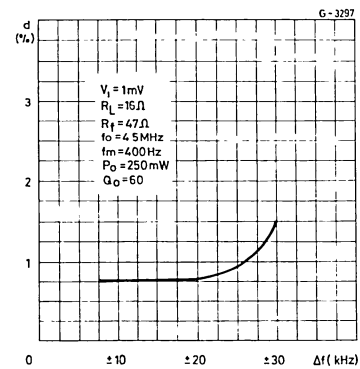
88DSTDA3190-08

Figure 6 : Distortion vs. Output Power.



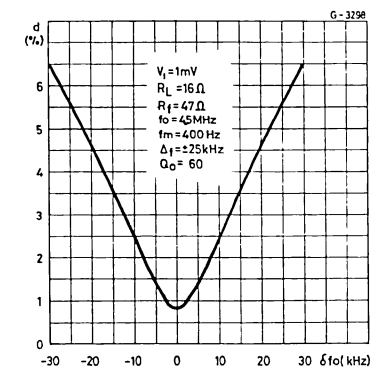
88DSTDA3190-09

Figure 7 : Distortion vs. Frequency Deviation.



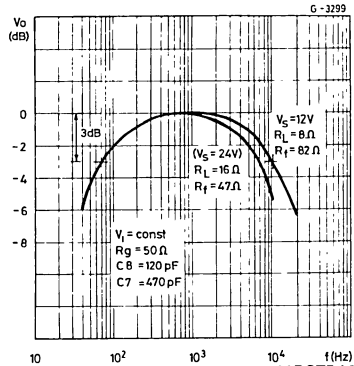
88DSTDA3190-10

Figure 8 : Distortion vs. Tunning Frequency Change.



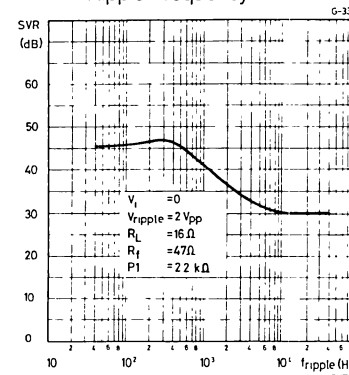
88DSTDA3190-11

Figure 9 : Audio Amplifier Frequency Response.



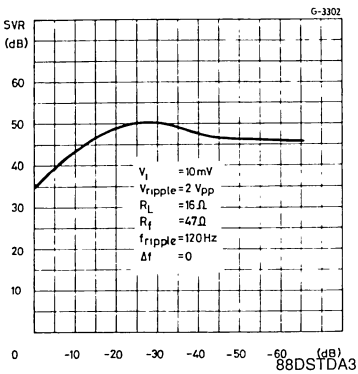
88DSTDA3190-12

Figure 10 : Supply Voltage Ripple Rejection vs. Ripple Frequency.



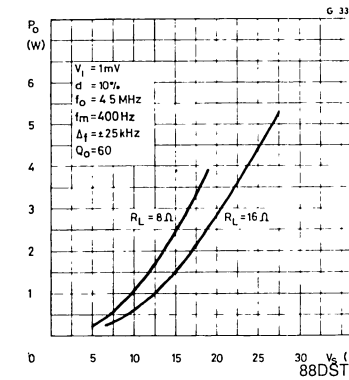
88DSTDA3190-13

Figure 11 : Supply Voltage Ripple Rejection vs; Volume Control Attenuation.



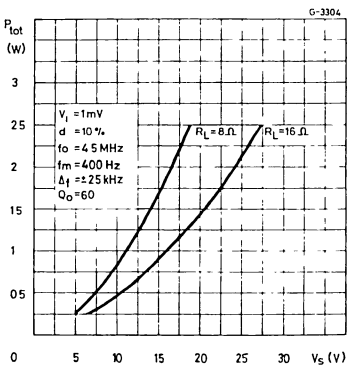
88DSTDA3190-14

Figure 12 : Output Power vs. Supply Voltage.



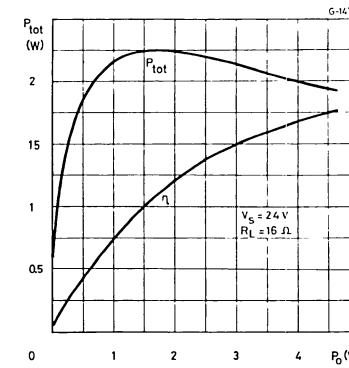
88DSTDA3190-15

Figure 13 : Maximum Power Dissipation vs. Supply Voltage (sine wave operation).



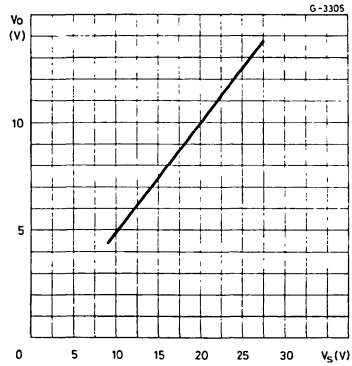
88DSTDA3190-16

Figure 14 : Power Dissipation and Efficiency vs. Output Power.



88DSTDA3190-17

Figure 15 : Quiescent Output Voltage (pin 11) vs. Supply Voltage.



88DSTDA3190-18

APPLICATION INFORMATION

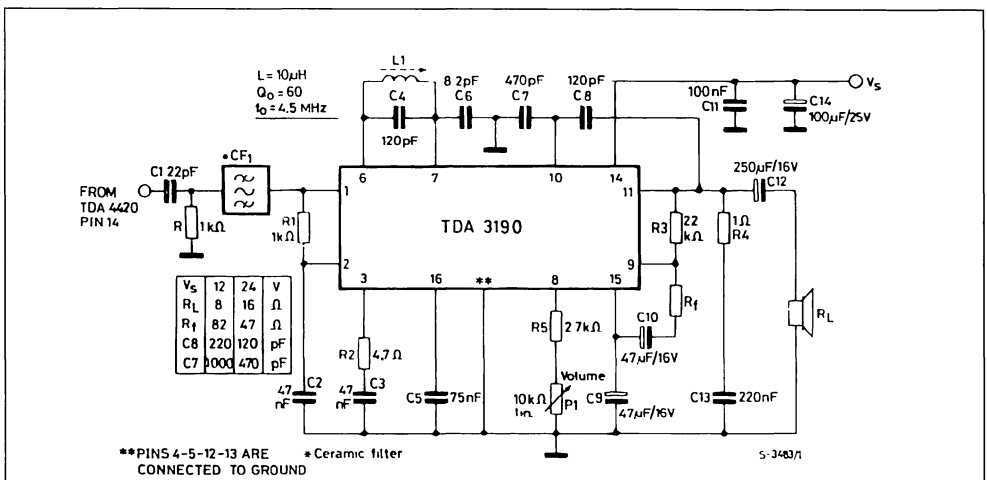
The electrical characteristics of the TDA3190 remain almost constant over the frequency range 4.5 to 6 MHz, therefore it can be used in all television standards (FM mod.). The TDA3190 has a high input impedance, so it can work with a ceramic filter or with a tuned circuit that provide the necessary input selectivity.

The value of the resistors connected to pin 9, determine the AC gain of the audio frequency amplifier. This enables the desired gain to be selected in relation to the frequency deviation at which the output stage of the AF amplifier, must enter into clipping.

Capacitor C8, connected between pins 10 and 11, determines the upper cutoff frequency of the audio bandwidth. To increase the bandwidth the values of C8 and C7 must be reduced, keeping the ratio C7/C8 as shown in the table of fig. 16.

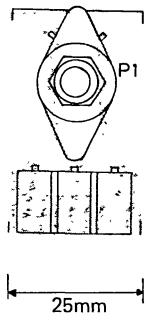
The capacitor connected between pin 16 and ground, together with the internal resistor of 10 KΩ forms the de-emphasis network. The Boucherot cell eliminates the high frequency oscillations caused by the inductive load and the wires connecting the loudspeaker.

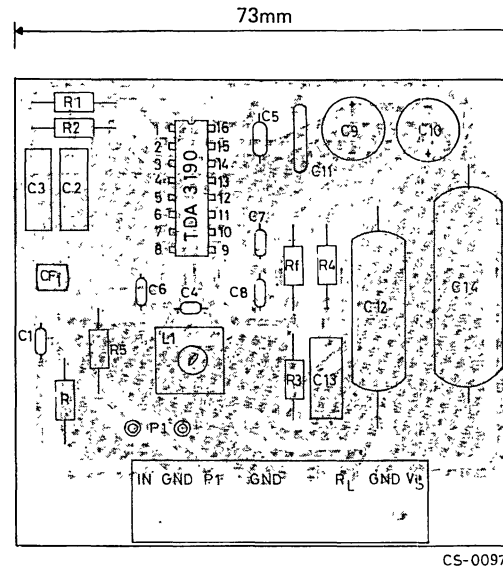
Figure 16 : Typical Application Circuit.



88DSTDA3190-19

Figure 17 : P.C. Board and Component Layout of the Circuit Shown in Fig. 16 (1 : 1 scale).





MOUNTING INSTRUCTION

The Rth j-amb of the TDA3190 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (fig. 18) or to an external heatsink (fig. 19).
The diagram of figure 20 shows the maximum dissipable power Ptot and the Rth j-amb as a function of the side "l" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 18 : Example of P.C. Board Copper Area which is used as Heatsink.

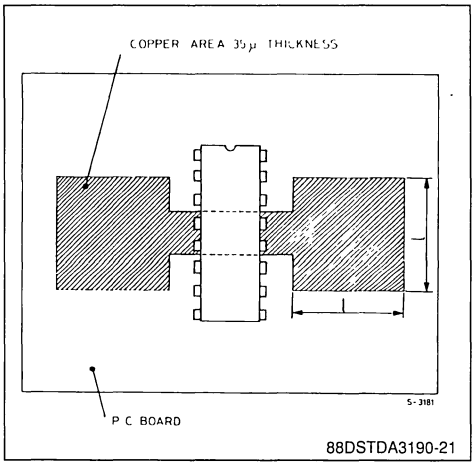


Figure 19 : External Heatsink Mounting Example.

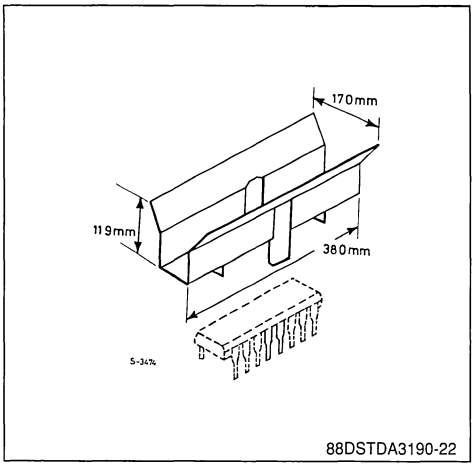


Figure 20 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l"

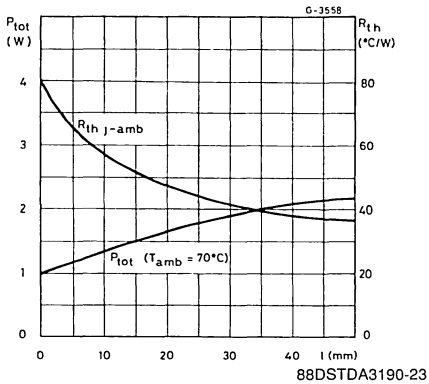
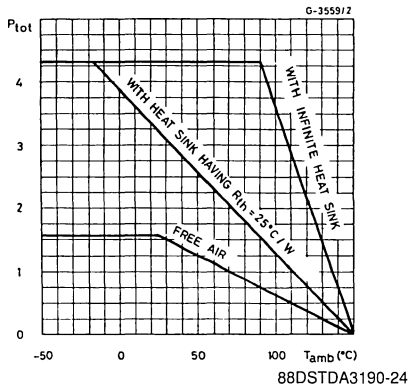


Figure 21 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

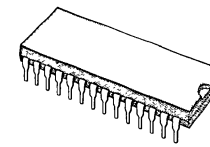


SGS-THOMSON MICROELECTRONICS

TDA3562A

PAL/NTSC ONE-CHIP DECODER

- CHROMINANCE SIGNAL PROCESSOR
- LUMINANCE SIGNAL PROCESSING WITH CLAMPING
- HORIZONTAL AND VERTICAL BLANKING
- LINEAR TRANSMISSION OF INSERTED RGB SIGNALS
- LINEAR CONTRAST AND BRIGHTNESS CONTROL ACTING ON INSERTED AND MATRIXED SIGNALS
- AUTOMATIC CUT-OFF CONTROL
- NTSC HUE CONTROL



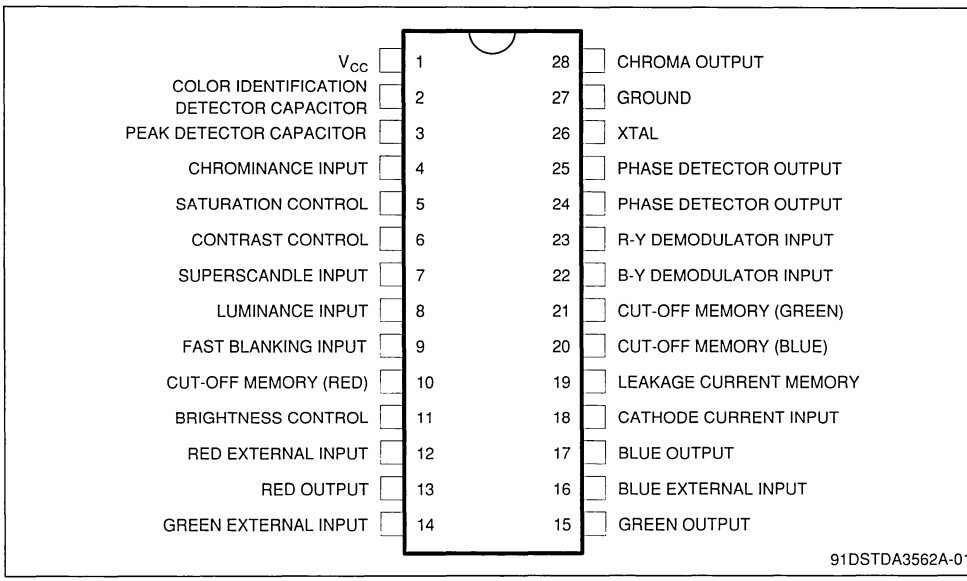
DIP28
(Plastic Package)

ORDER CODE : TDA3562A/1

DESCRIPTION

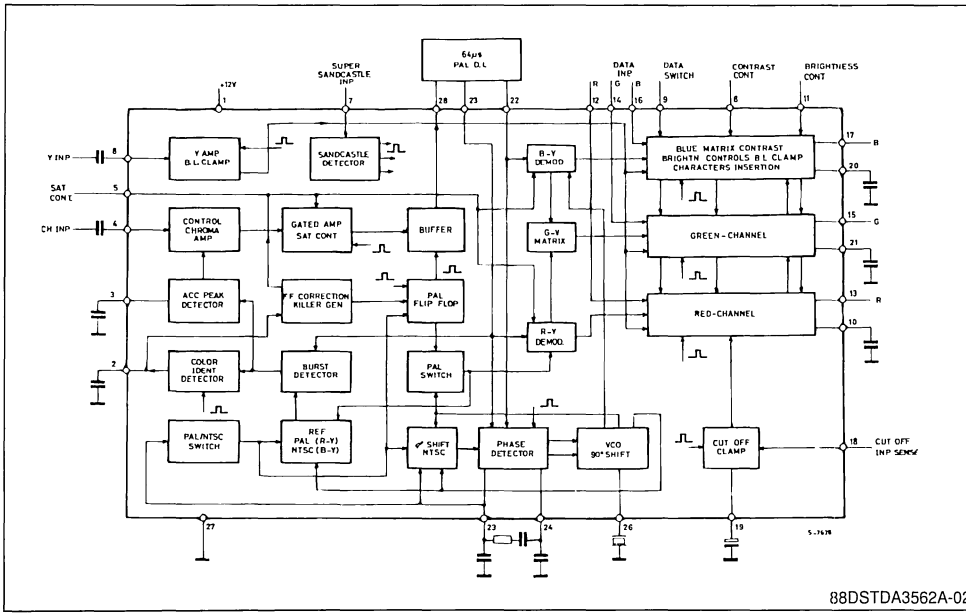
The TDA3562A is a monolithic IC designed as decode PAL and/or NTSC colour television standards and it combines all functions required for the identification and demodulation of PAL and NTSC signals.

PIN CONNECTIONS



91DSTDA3562A-01

BLOCK DIAGRAM



88DSTDA3562A-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	13.2	V
P_{tot}	Power Dissipation at T_{amb} = 65 °C	1.7	W
T_{stg}	Storage Temperature	– 25 to 150	°C
T_j	Junction Temperature	– 25 to 150	°C
T_{amb}	Ambient Temperature Range	0 to 70	°C

TAB-01

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	40	°C/W

TAB-02

ELECTRICAL CHARACTERISTICS

Test conditions unless otherwise specified :
Supply voltage : Pin 1 at 12 V
T_{amb} = 25 °C

Input signals :
Luminance input signal V8 = 0.48 Vp/p (1)
Chrominance input signal V4 = 0.39 Vpp (2)
Data input signals $V_{12, 14, 16}$ = 1.4 Vpp (3)

Control inputs at nominal value :
Pin 6 Nom. contrast = max. contrast – 5 dB
Pin 5 Nom. saturation = max. saturation – 6 dB
Pin 11 Nom. brightness = 2 V
Pin 9 at 0.4 V

(1) Composite video signal (100 % white)
(2) Colour bar signal with 75 % colour saturation and chrominance to burst ratio = 2.2 : 1.
(3) Including neg.going sync. pulse.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY INPUT (pin 1)						
	Supply Voltage Range		10.8		13.2	V
	Supply Current	V_1 = 12 V		80	110	mA
LUMINANCE INPUT (pin 8)						
	Composite Input Signal				0.8	V_{pp}
	Input Current			0.1	1	µA
CHROMINANCE INPUT (pin 4)						
	Input Signal		40		1100	mVpp
	Input Resistance			10		KΩ
	Input Capacitance				6 5	pF
SUPER SANDCASTLE INPUT (pin 7)						
	Gating & Clamping Level		7.5			V
	H-pulse Separating Level		4		5	V
	V-pulse Separating Level		2		3	V
	Forbidded Range			1 to 2		V
	Input Current	V_7 = 0 to 1 V			– 460	µA
		V_7 = 1 to 8.5 V		50		µA
		V_7 = 8.5 to 12 V			2	mA
	Delay Between Black Level Clamping Pulse and Gating Pulse			0.6		µs
DATA BLANKING INPUT (pin 9)						
	Input Voltage for no Data Insertion				0.4	V
	Input Voltage for Data Insertion		0.9		3	V
	Input Resistance		7		13	kΩ
"BLACK CURRENT" STABILIZATION INPUT (pin 18)						
	D. C. Bias Voltage		3.5	5	7	V
	Internal Limiting Threshold			9		V
	Switching Threshold for "Black Current" ON			8		V
	Difference between Input Voltage for "BlackCurrent" and Leakage Current			0.5		V
	Input Resistance during Scan			1.5		kΩ
	Input Current during "Black Current" Measurement				2	µA
	Input Current during Scan				10	mA

TAB-03

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RGB - OUTPUTS (Pins 13, 15, 17)						
	Output Resistance			50		Ω
	Current Source		2	3		mA
	Peak Output Level		10.7		11.3	V
	Residual 4.4 MHz at RGB Outputs				100	mVpp
	Residual 8.8 MHz at RGB Outputs				150	mVpp
LUMINANCE CHANNEL						
	Frequency Resp. of Total Lumin. Amplifiers	f = 0 to 5 MHz		– 1	–3	dB
	RGB Output Signal (black to white)		3.5	4	4.5	Vpp
	Relative Spread of RGB - Output Signals				1	dB
	Contrast Control Range	(see fig. 1)		– 5 to 10		dB
	Tracking Over 10 dB Contrast Control			0		dB
	Contrast Control Input Current				15	µA
	Blanking Level of RGB - Output Signals			1	1.2	V
	Difference Between Blanking Levels,		0		mV	
	Differential Drift of Blanking Levels	ΔT = 40 °C		0		mV
	Brightness Control Input Current				5	µA
	Brightness Control Range	(see fig. 3)		1 to 3		V
	Relation Ship between Black Level Variation and Brightness Control Variation	(see fig. 3)		1.3		V/V
	Black Level of RGB Output Signals	(see note 4)		3		V
	Difference between Black Levels	(see note 4)		0		mV
	Tracking Over Brightness Control				2	%
	Differential Drift of Black Levels	ΔT = 40 °C			20	mV
	Drift of Black Level Versus 10 % Variation of Supply Voltage and Contrast Control				20	mV
"CUT OFF CURRENT" REGULATION						
	RGB Output Level of the "3L Windows" after Switch-on		7.5			V
	RGB Outputs Level of the "3L Windows" after Cut off Current Stabilization	(see note 4)	1	3	5	V
	RGB Output Range		1		5	V
	Charge/Discharge Current during Measuring Time (3L windows) at Pins 10, 19, 20 and 21			1		mA
	Leakage Currents Flowing into Pins 10, 20 and 21 during Scan				50	nA

TAB-04

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RGB DATA INSERTION						
	Data RGB Output Signal	V_9 = 0.9 to 3 V		4		Vpp
	Differential Amplitude Error between RGB Output Signal and Data Output Signal				10	%
	Differential Error between Black Levels of RGB Output Signals and Black Levels of Data Output Signals				200	mV
	Rise Time of Data Output Signal			50	80	ns
	Differential Delay			0	40	ns
	Attenuation of RGB Output Signal	V_9 = 0.9 to 3 V		46		dB
	Frequency Response for f = 0 to 5 MHz			– 1	– 3	dB
CHROMINANCE CHANNEL						
Pin 4	Chrominance Input Signal		40		1100	mVpp
Pin 4	Input Resistance			10		kΩ
Pin 4	Input Capacitance				6.5	pF
	ACC Control Range		30			dB
Pin 28	Burst Change Over 30 dB ACC Range				1	dB
	Saturation Control Range	(see fig. 2)		– 44 to 6		dB
Pin 5	Sat. Control Input Current				20	µA
Pin 28	Chrominance Output Voltage	V_5 = 4.2 V	4			Vpp
	Burst Input Signal at Pins 22 and 23			100		mVpp
	Input Resist. Bet. Pins 22, 23 and Ground			1		kΩ
Pin 28	Phase Shift Bet. Burst and Chrom. Signal		– 5	0	5	°
Pin 2	Voltage at Nom. Input Signal			4.7		V
Pin 2	Voltage without Input Signal			2.6		V
Pin 2	Identificaton-on Voltage			2.1		V
Pin 2	Colour-off Voltage			3.4		V
Pin 2	Colour-on Voltage			3.6		V
Pin 3	Voltage at Nom. Input Signal			5.1		V
COLOUR DEMODULATORS AND G-Y MATRIX						
	Ratio (B-Y) / (R-Y)		1.60	1.78	1.96	
	Ratio (G-Y) / (R-Y)	(B – Y) = 0	– 0.46	– 0.51	– 0.56	
	Ratio (G-Y) / (B-Y)	(R – Y) = 0	– 0.14	– 0.19	– 0.24	
REFERENCE OSCILLATOR						
	Oscillator Frequency			2 fcs		MHz
	Temp. Coefficient of Oscillator Frequency	(see note 5)		– 2		Hz/k
Pin 26	Input Resistance			400		Ω
Pin 26	Input Capacitance				10	pF
	Pull-in Range	(see note 5)	500	700		Hz
	Phase Shift for ±400 Hz Deviation				5	°C
	Phase Shift between (R – Y) and (R – Y) Ref.Signal				5	°C
	Phase Shift between (R – Y) and (B – Y) Ref.Signal		85	90	95	°C

TAB-05

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
NTSC OPERATION						
Pins 24, 25	PAL-on Operating Range		9		11	V
Pins 24, 25	Threshold for NTSC-on			8.8		V
$J_{24} + J_{25}$	Avarage Output Current	Key Pulse = 4 µs		90		µA
	Hue Control		± 30			°C
Pins 24, 25	Hue Control Voltage		7.5		8.5	V

(4) The levels depend on the application circuit and on the spread and drift of picture tube guns.
(5) All frequency variations are referred to 4.4 MHz carrier frequency.

TAB-06

Figure 1 : Contrast Control Voltage Range.

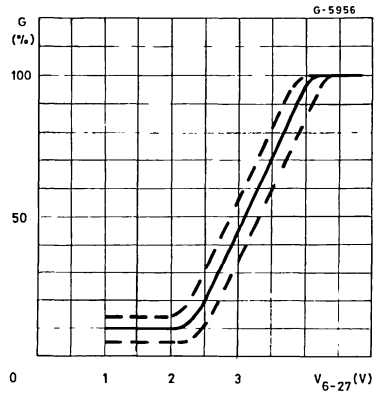


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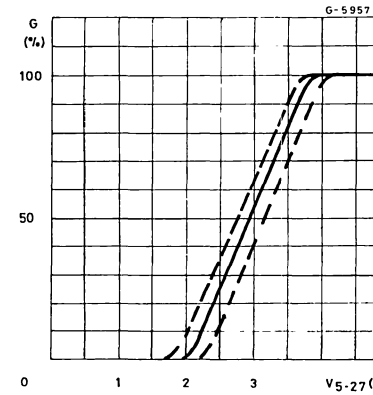
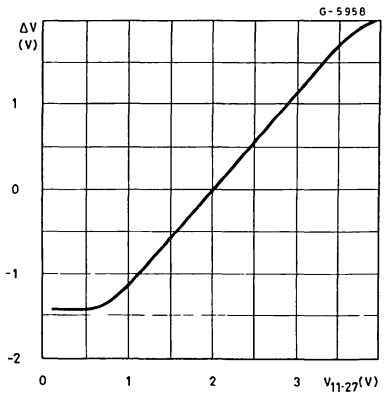
Figure 2 : Saturation Control Voltage Range.



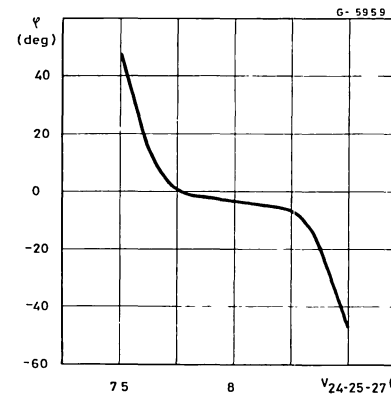
88DSTDA3562A-04

Figure 3 : Difference Between Signal Black Level and Measuring level (3L windows after cut off current stabilization) at the RGB Outputs (ΔV) vs. Control Voltage ($V_{11} - V_{12}$).



88DSTDA3562A-05

Figure 4 : Hue Control Voltage Range.



88DSTDA3562A-06

Figure 5 : Application Diagram Showing the TDA3562A for a PAL Decoder.

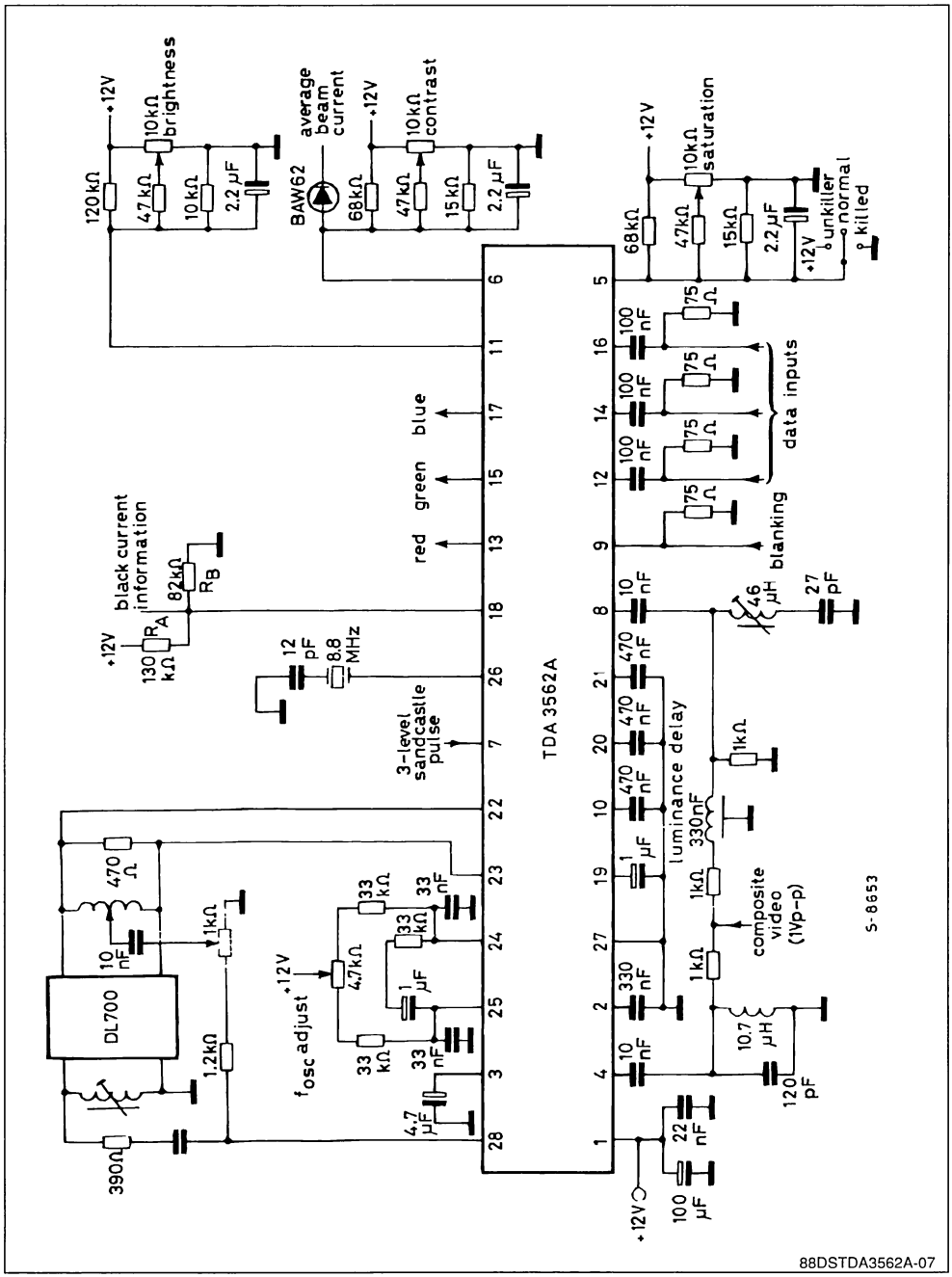
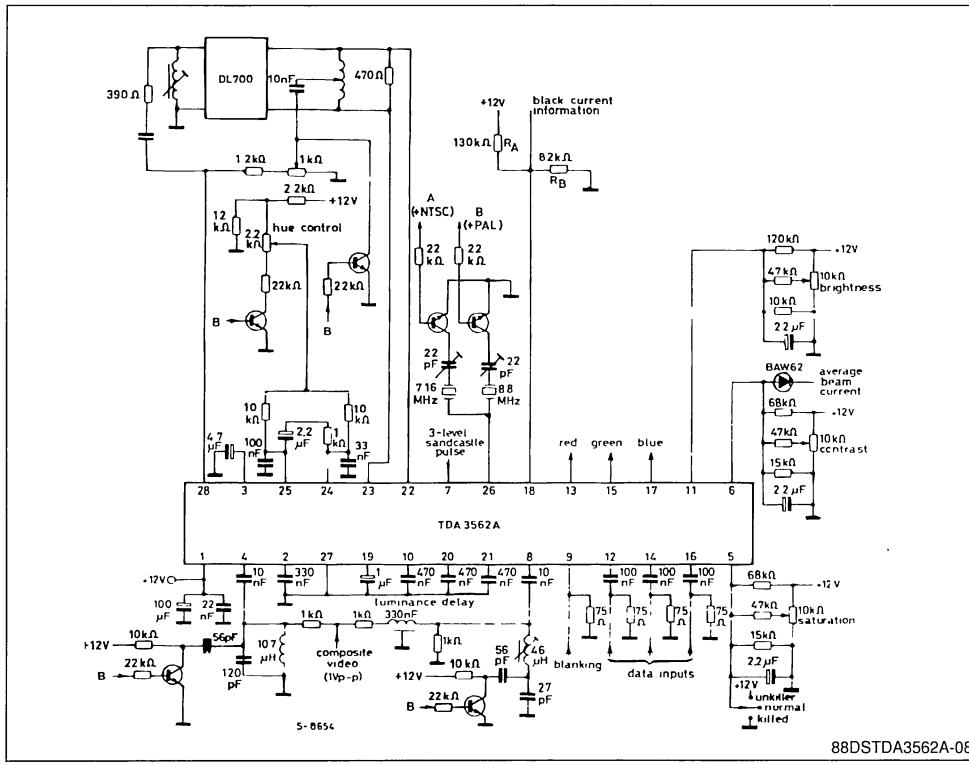
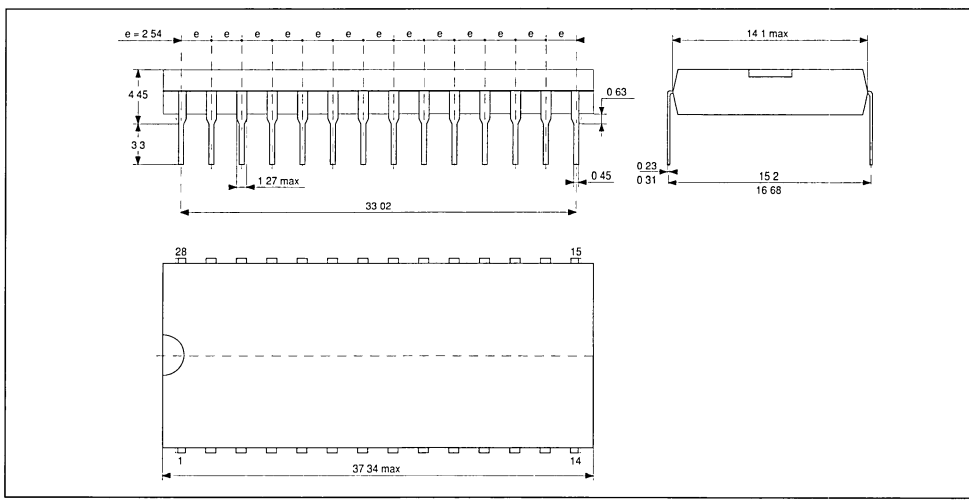


Figure 6 : Application Diagram Showing the TDA3562A for a PAL/NTSC Decoder.



PACKAGE MECHANICAL DATA : 28 PINS - PLASTIC DIP



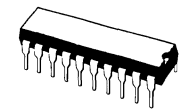
TV SOUND CHANNEL WITH DC CONTROLS

- INTERNAL VCR INPUT/OUTPUT SWITCHING
- 4W OUTPUT POWER INTO 16Ω
- NO SCREENING REQUIRED
- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- LOW DISTORTION
- DC TONE/VOLUME CONTROLS
- THERMAL PROTECTION

DESCRIPTION

The TDA4190 is a complete TV sound channel with DC tone and volume controls plus an internally switched VCR input/output. Mounted in a Powerdip 16 + 2 + 2 package, the device delivers an output power of 4 W into 16Ω (d = 10%, V_S = 24V) or 1.5W into 8Ω (d = 10%, V_S = 12V). Included in the TDA4190 are : IF amplifier limiter, active low-pass filter, AF preamplifier and power amplifier, turn-off muting, VCR switch, mute circuit and thermal protection.

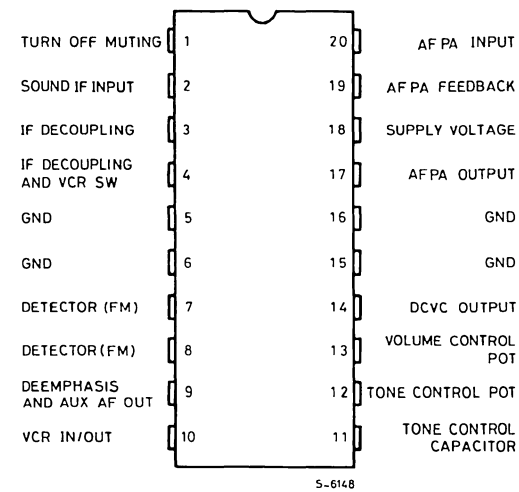
High output, high sensitivity, excellent AM rejection and low distortion make the device suitable for use in TVs of almost every type. Further, no screening is necessary because the device is free of radiation problems.



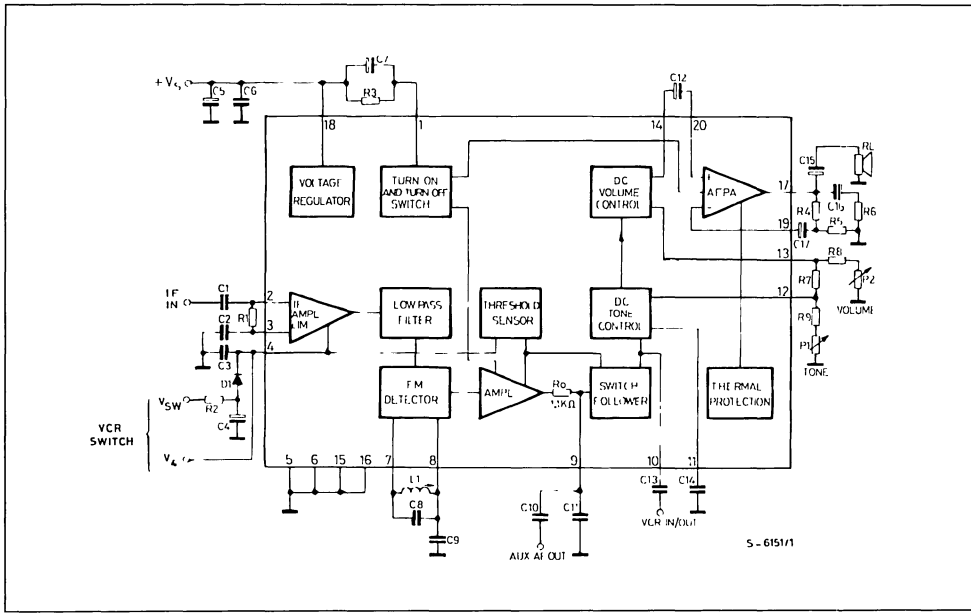
DIP-20
(plastic package)

ORDER CODE : TDA4190A

CONNECTION DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 18)	28	V
V_I	Voltage at pin 1	$\pm V_S$	
V_i	Input Voltage (pin 2)	1	V_{pp}
I_o	Output Peak Current (repetitive)	1.5	A
I_o	Output Peak Current (non repetitive)	2	A
I_4	Current (pin 4)	10	mA
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W*

(*) Obtained with GND pins soldered to printed circuit with minimized copper area

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_S = 24V, V_{sw} = 2V or no V4, $\Delta f = \pm$ 25KHz, R_L = 16Ω, V_i = 1mV, P_1 = 12KΩ, f_o = 4.5MHz, f_m = 400Hz, T_{amb} = 25°C, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 18)	P_2 = 12 KΩ	10.8		27	V
V_O	Quiescent Output Voltage (pin 18)	P_2 = 12 KΩ	11	12	13	V
V_1	Pin 1 DC Voltage	P_2 = 12 KΩ R_1 = 270 KΩ		5.3		V
V_4	Pin 4 DC Voltage	P_2 = 12 KΩ		3.2		V
I_d	Quiescent Drain Current	P_2 = 12 KΩ		32		mA

IF AMPLIFIER AND DETECTOR

$V_{i\ (threshold)}$	Input Limiting Voltage at Pin 2 (– 3 dB)	V_o = 4 V_{rms}		50	100	μV
V_9	Recovered Audio Voltage (pin 9)	$\Delta f = \pm$ 7.5 KHz P_2 = 12 KΩ	140	200	280	mV
AMR	Amplitude Modulation Rejection (*)	m = 0.3 ; V_i = 1 mV ; V_o = 4 V_{rms}		60		dB
R_i	Input Resistance (pin 2)	Δf = 0 P_2 = 12 KΩ		30		KΩ
C_i	Input Capacitance (pin 2)	Δf = 0 P_2 = 12 KΩ		6		pF
R_9	Deemphasis Resistance	C_1 = 68 to 888 nF	0 75	1 1	1 5	KΩ

DC VOLUME CONTROL

Kv	Volume Attenuation (resistance control)	P_2 = 0 KΩ P_2 = 4.3 KΩ P_2 = 12 KΩ	20	0 26 88	32	dB dB dB
Vc	Control Voltage	K = 0 dB K = 26 dB K = 88 dB		0 1.3 2.6		V V V
$\frac{\Delta K_v}{\Delta T_{pins}}$	Volume Attenuation Thermal Drift (resistance control)	T_{pins} 25 to 85 °C P_2 = 4.3 KΩ		– 0.05		$\frac{dB}{°C}$

DC TONE CONTROL

K_T	Tone Cut	V_{sw} = 8 V or V_4 = 2 V V_{10} = 200 mV P_1 = 12 KΩ to 100 Ω f = 10 KHz		14		dB

ELECTRICAL CHARACTERISTICS (continued)

AUDIO FREQUENCY AMPLIFIER

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
P_o	Output Power (d = 10 %)	V_s = 24 V V_s = 12 V	R_L = 16 Ω R_L = 8 Ω	3.5	4.1 1.5		W W
B	Frequency Response of Audio Amplifier (– 3 dB)	P_o = 1 W V_{sw} = 8 V or V_{10} = 200 mV	R_L = 16 Ω V_4 = 2 V V_o = 4 Vrms @ 400 Hz	15	50		KHz
SVR	Supply Voltage Rejection	P_2 = 12 KΩ Δf = 0	f_{ripple} = 120 Hz		26		dB

V.C.R.

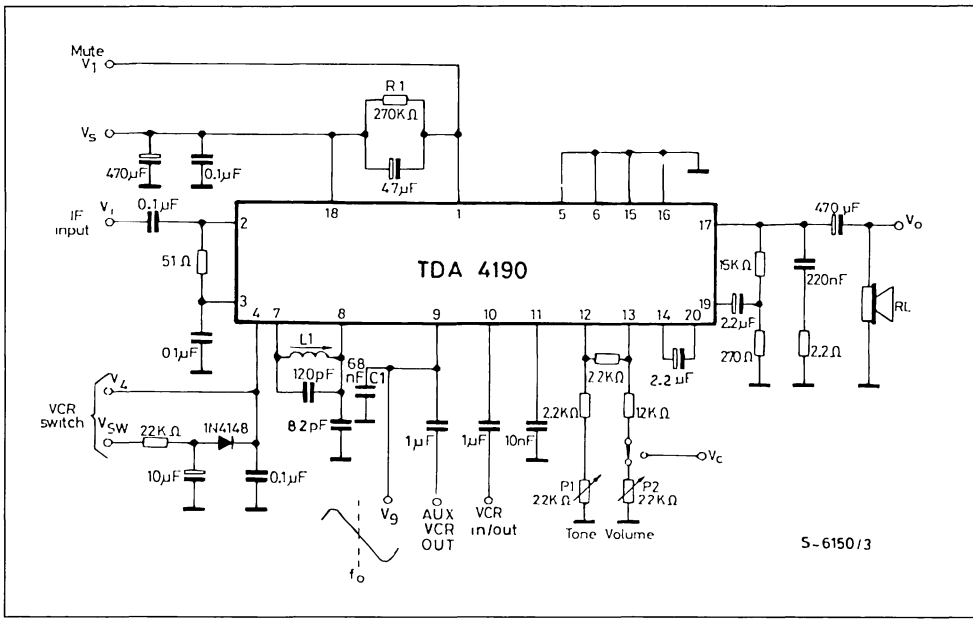
V_4	Input Switching Voltage for Recording for Playback			Floating			
						2	V
V_{sw}	Input Switching voltage for Recording for Playback					2	V
				8			V
V_{10}	Input Voltage (playback)	V_4 = 2 V or V_o = 4 V_{rms}	V_{sw} = 8 V P_2 = 0	50	70	100	mV
V_{10}	Output Voltage (recording)	P_2 = 12 KΩ	Δf = ± 7.5 KHz	140	200	280	mV
R_{10}	Input Resistance (playback)	V_4 = 2 V or	V_{sw} = 8 V	10			KΩ
R_{10}	Output Resistance (recording)	Δf = ± 7.5 KHz, no	V_4 or V_{sw} = 2 V			100	Ω
d	Total harmonic Distortion of Pin 10 Output Signal	Δf = ± 7.5 KHz	V_i = 1 mV		0 5		%
d	Total Harmonic distortion of 20 dB Over Load V_{10}	V_4 = 2 V V_{10} = 1 V_{rms}	V_{sw} = 8 V V_o = 4 V_{rms}		0.5	3	%
SVR	Supply Voltage Rejection at Output Pin 10	Δf = 0 f_{ripple} = 120 Hz	P_2 = 12 KΩ		66		dB
$\frac{S+N}{N}$	Signal and Noise Ratio at Output Pin 10	Δf = ± 25 KHz	$V_i \geq 1$ mV		70		dB

OVERALL CIRCUIT

$\frac{S+N}{N}$	Signal to Noise Ratio (*)	$V_i \geq 1$ mV Δf = 0	V_o = 4 Vrms		70		dB
d	Distortion (*)	P_o = 50 mW V_s = 24 V V_s = 12 V	Δf = ± 7.5 Hz R_L = 16 Ω R_L = 8 Ω		 0.5 0.5		 % %
M	Muting (*)	V_o = 4 V_{rms} @ no	V_1 ; V_1 = 0	100			dB
Δf		P_2 = 0	V_o = 4 Vrms		3	6	KHz

* Test bandwidth = 20 KHz

TEST CIRCUIT



TEST CONDITIONS (unless otherwise specified)

V_S = 24V ; V_{SW} = 2V or no V4 ; R_L = ∞ ;
V_{in} = 1mV ; Q_o = 60 ; f_o = 4.5MHz ;
P_1 = 12KW ; f_m = 400Hz ; Δf = ± 25KHz.

Figure 1 : Relative Audio Output Voltage and Output Noise vs. Input Signal.

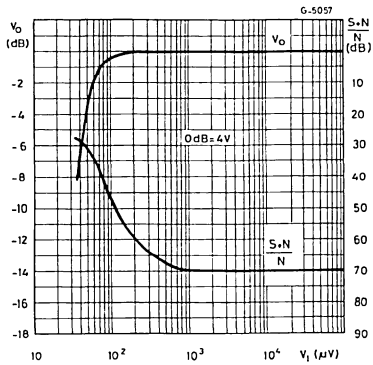


Figure 2 : Output Voltage Alternance vs. DC Volume Control Resistance (a) or Vs. DC Volume Control Voltage (b).

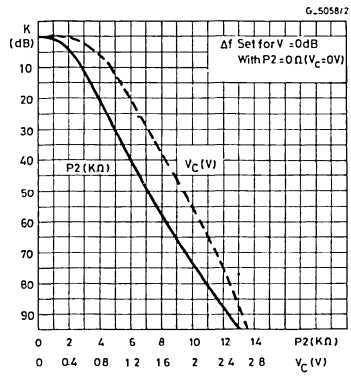


Figure 3 : DC Tone Control Cut of the High Audio Frequencies for some Values of Resistance Adjusted by P1.

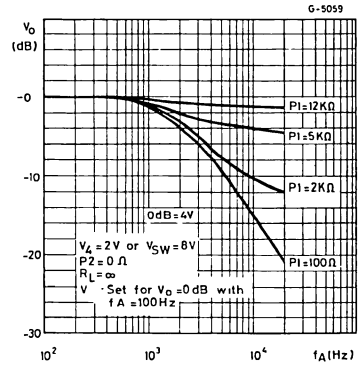


Figure 4 : Amplitude Modulation Rejection vs. Input Signal.

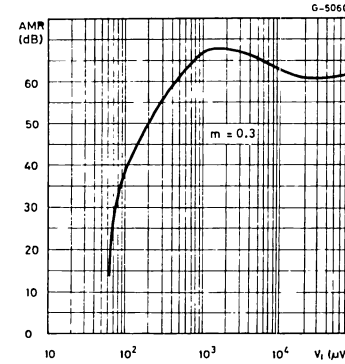


Figure 5: Δ AMR vs. Tuning Frequency Change

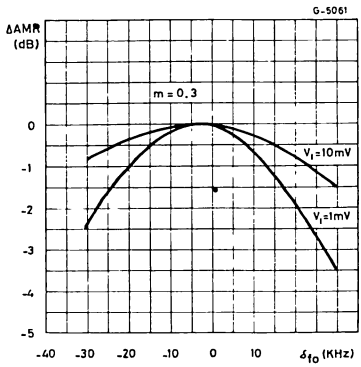


Figure 6 : Recovered Audio Voltage vs. Unloaded Q-factor of the Detector Coil.

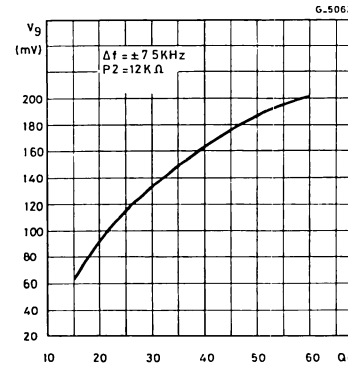


Figure 7 : Distortion vs. Unloaded Q-factor of the Detector Coil.

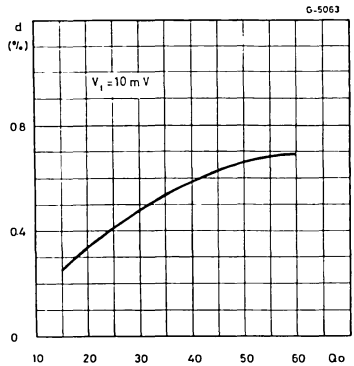


Figure 8 : Distortion vs. Frequency Variation.

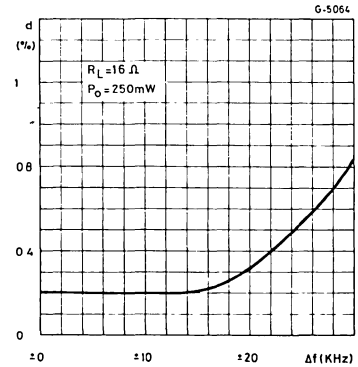


Figure 9 : Distortion vs. Tuning Frequency Change.

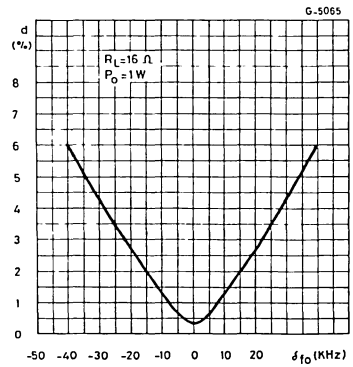


Figure 10 : Distortion vs. Output Power.

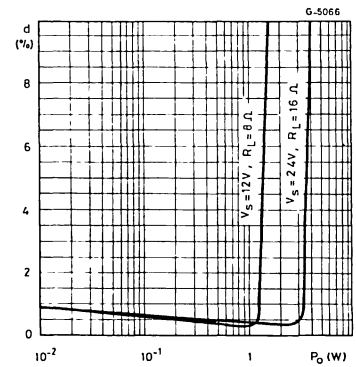


Figure 11 : Audio Amplifier Frequency Response.

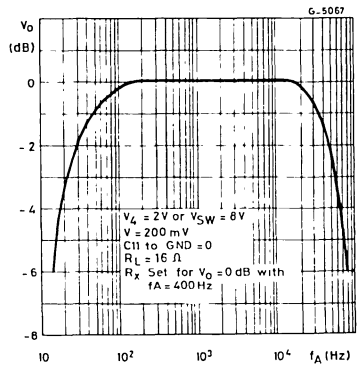


Figure 12 : Output Power vs. Supply Voltage.

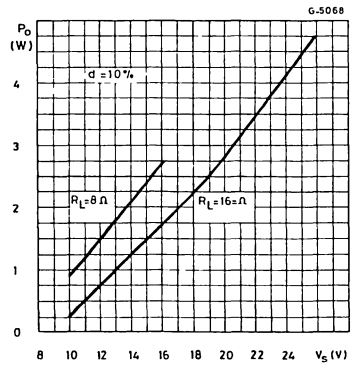


Figure 13 : Power Dissipation vs. Supply Voltage (sine Wave operation).

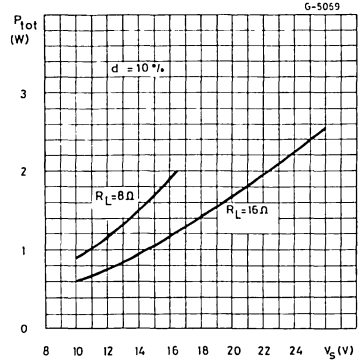


Figure 14 : Power Dissipation and Efficiency vs. Output Power.

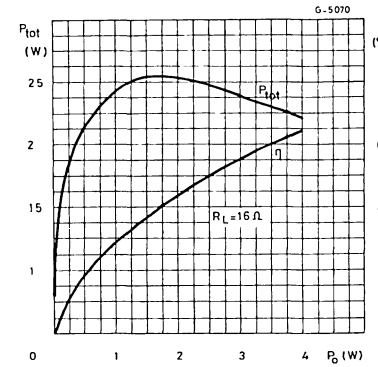
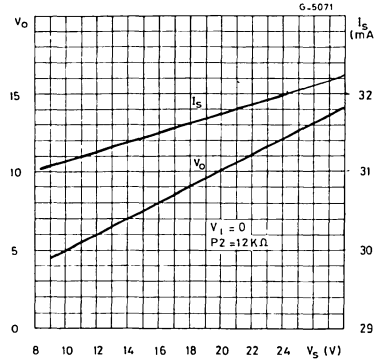


Figure 15 : Quiescent Drain and Quiescent Output Voltage vs. Supply Voltage.



APPLICATION INFORMATION (refer to the block diagram)

IF AMPLIFIER-LIMITER

It is made by six differential stages of 15dB gain each so that an open loop gain of 90 dB is obtained.

While a unity DC gain is provided, the AC closed loop gain is internally fixed at 70dB that allows a typical input sensitivity of 50μV.

The differential output signal is single ended by a 20dB gain amplifier that through a buffer stage, feeds the detector system.

Internal diodes protect the inputs against overloads.

- Pin 2 is the IF non-inverting input
- Pin 3 is decoupled by a capacitor to open the AC loop
- Pin 4 grounded by a capacitor, allows a typical sensitivity of 50μV. (see VCR facility too).

LOW-PASS FILTER, FM DETECTOR AND AMPLIFIER

The IF signal is detected by converting the frequency modulation into amplitude modulation and then detecting it.

Since the available modulated signal is a square wave, a 40dB/decade low-pass filter cuts its harmonics so that a sine wave can feed the two-resonances external network L1, C8 and C9.

This network defines the working frequency value, the amplitude of the recovered audio signal and its distortion at the highest frequency deviations.

The two resonances f1 (series resonance) and f2 (parallel resonance) can be computed respectively by :

$$X_{C9} = \frac{X_{L1} \cdot X_{C8}}{X_{L1} + X_{C8}} \quad \text{and} \quad X_{L1} = X_{C8}$$

The ratio of these frequencies defines the peak-to-peak separation of the "S" curve :

$$\frac{f2}{f1} = \sqrt{1 \frac{C_9}{C_8}}$$

A differential peak detector detects the audio frequency signal that amplified, reaches the deemphasis network R0 ; C11.

The AF amplifier can be muted (see turn-on and turn-off switch and VCR facility).

- Pin 7 is the output of the low-pass filter and one input of the differential peak detector
- Pin 8 is the other input of the differential peak detector
- Pin 9 is used to provide the required deemphasis time constant by grounding it with C11. At this pin, the internal impedance of which is typically of 1.1 KΩ, is available the recovered audio signal as auxiliary output.

VCR FACILITY

The deemphathized AF signal reaches the switch follower block can provide to change the impedance of its output depending on the VCR function required.

The switch follower is driven by the threshold sensor block. This one switches both the amplifier and the switch follower by sensing the voltage at pin 4.

When no voltage is forced at pin 4 the function of pin 10 is of VCR output with low impedance ; when the voltage at pin 4 is lower or higher than its quiescent value, the amplifier is muted and the impedance of pin 10 is switched to a high value for a proper VCR input operation.

Since pin 4 reaches also the inverting input of the IF amplifier-limiter, this one can be switched off two for best insulation of the pin 10 with the TV signal path.

So, the VCR facility followed this truth table :

Mode	Vsw	or V_4	Function of Pin 10	Impedance of Pin 10
Recording	≤ 2 V	No One	Output	≤ 100 Ω
Playback	≥ 8 V	≤ 2 V	Input	≥ 10 KΩ

The output signal available when operating during recording is not dependent from both the volume and tone controls while, during playback, the input signal can be regulated by P1 and P2.

Pin 10, as input, can accept until 1 VRMS of overload.

- Pin 4 is the VCR switch driver
- Pin 10 is the VCR input/output pin.

DC TONE CONTROL

The same signal available or applied to pin 10, after a voltage to current converter, reaches, the DC Tone Control block. It operates, inside the 10 KHz bandwidth, by cutting the high audio frequencies with a variable slope of an RC network, by means of P_1

The maximum slope of the RC network is of 20 dB per decade and its pole is defined by :

X_{C11} = 6.8KΩ, typically.
Pin 11 – At this pin is tied the tone capacitor
Pin 12 – is the DC Tone Control input.

DC VOLUME CONTROL

After tone control regulation, the AF current signal reaches the DC volume control block, that controls its intensity. The normal control, for which the block has been designed for a narrow spread, is produced by P2 ; however, without P2, a voltage control can be operated by forcing a voltage at pin 13 through R8.

- Pin 12, already seen as a DCTC input, is the reference voltage for the DCVC. Because of this, a small interface between tone and volume regulation can be expected.
- Pin 13 is the DC volume control input.
- Pin 14 after a current to voltage converter, the audio frequency signal comes out a this pin.

AUDIO FREQUENCY POWER AMPLIFIER AND THERMAL PROTECTION

Through C12 the signal reaches the amplifier non-inverting input. The closed loop gain is defined by

the feedback at pin 19 (inverting input) or by the ratio :

$$G_V = 20 \text{ Log } \frac{R5 + R4}{R5} \text{ (dB)}$$

The amplifier, thermally protected, can supply 4 W of power into a 16 Ω load with 24 V of supply voltage. The power output stage is a class B type.

- Pin 20 is the non-inverting input
- Pin 19 is the inverting input
- Pin 17 is the output of the AFPA.

TURN-ON AND TURN-OFF SWITCH

This block has been mainly designed to avoid, turning on the TV set, that transients, produced by the vision output, can reach the speaker.

Moreover this block, together an optimized rise time and full time of the supply voltage V_S, can avoid any pop generally produced during the turn-on and the turn-off transients.

Turning on, pin 1 follows the supply voltage V_S by means of C7 ; a threshold is reached and the muting of the AFPA output (pin 17) is suddenly produced.

When V_S reaches it stop, C7 charges itself through the input impedance of pin 1 and the muting is removed with a time constant depending on the C7 value.

Turning off, the V_S trend, in series to the voltage $VS - V_1$ and which C7 is charged, drives pin 1 at a low level threshold and a sudden muting is produced again.

Since the turn-off can be operated with high output power, if the muting operates when the current through the inductance of the speaker is different from zero, a flyback is generated and then a small pop can be produced.

The flyback is clipped by integrated diodes.

The threshold that produce the muting have been chosen in the way that 1 Vpp of ripple on the supply voltage does not produce any switching.

By shorting pin 1 to ground through a 10 KΩ resistor the muting can be obtained.

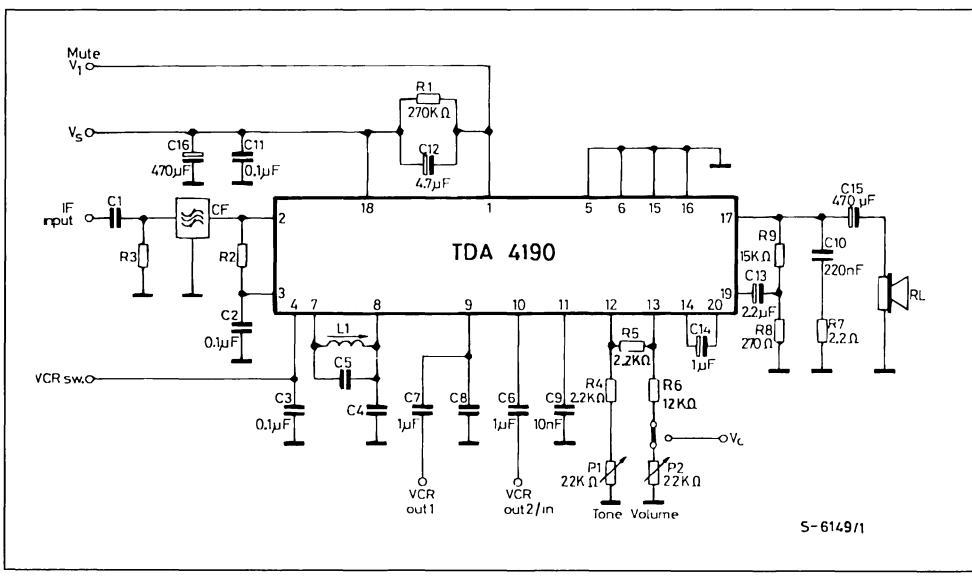
- Pin 1 is the turn-on and turn-off muting input.

SUPPLY

An integrated voltage regulator with different output levels, supplies all the blocks operating with small signal.

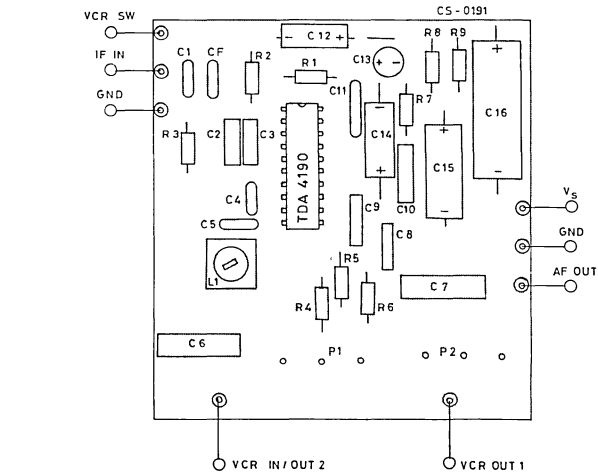
- Pin 18 is the main supply of the device.
- Pin 5 ; pin 6 ; pin 15 and pin 16 are the ground of the supply. These pins are used to drain out from the device the heat produced by the dissipated power.

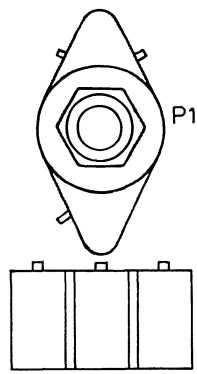
Figure 16 : Application Circuit.

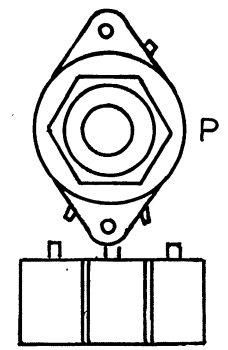


Components	Units	Appl. 4.5 MHz	Appl. 5.5 MHz	Appl. 6 MHz
L1	µH	10 $Q_0 = 60$	12 $Q_0 = 80$	10 $Q_0 = 70$
C5	pF	120	68	68
C4	pF	9	8.2	6.8
C8	nF	68	47	47
C.F.	–	Murata SFE 4.5 MA	Murata SFE 5.5 MB	Murata SFE 6.0 MB
C1	pF	22	18	18
R2	Ω	1000	560	470
R3	Ω	1000	560	470

Figure 17 : PC Board and Components Layout of the Circuit of Fig. 16 (1 : 1 scale).

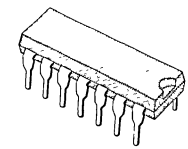






TV SIGNAL IDENTIFICATION CIRCUIT AND AFC INTERFACE

- IDENTIFICATION OF TRUE TV STATIONS ONLY
- LOW IMPEDANCE OUTPUT OF THE IDENTIFICATION SIGNAL
- DIGITAL CONTROL SIGNAL FOR AUTOMATIC SEARCH AND AFC OPERATION
- THERMAL COMPENSATION OF THE VOLTAGE REGULATOR



DIP14
(Plastic Package)

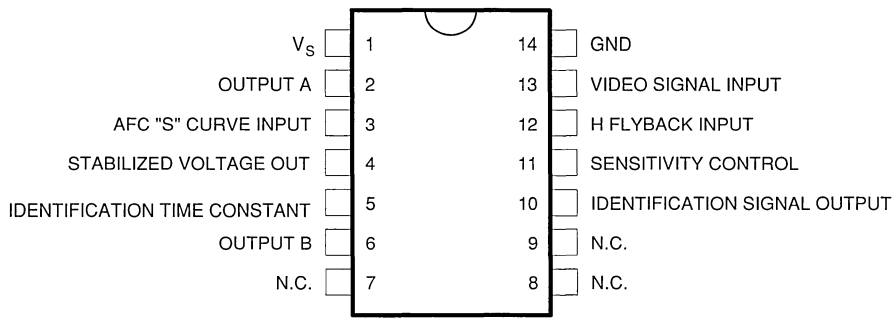
ORDER CODE : TDA4433

DESCRIPTION

The TDA4433 is a monolithic integrated circuit in a 14 lead dual-in-line plastic package. It integrates the following functions :

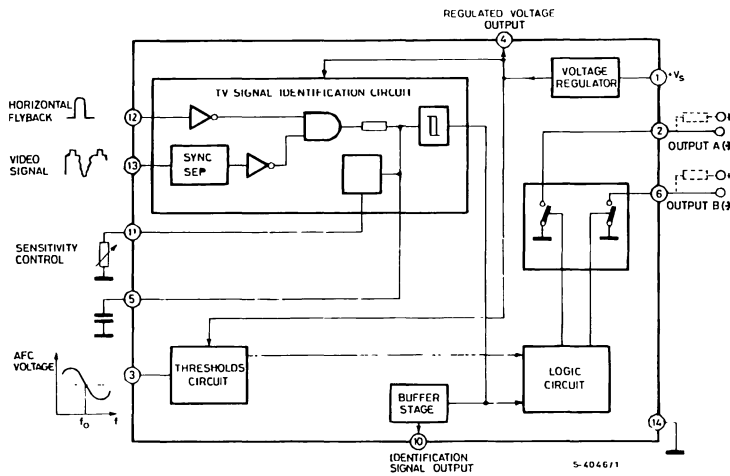
- TV signal identificator - Sync. separator - Threshold detector - Digital Interface - Voltage regulator.

PIN CONNECTION



91DSTDA4433-01

BLOCK DIAGRAM



* Open collector outputs.

88DSTDA4433-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 1)	16	V
V_3	Voltage at Pin 3	16	V
V_{13}	Voltage at Pin 13	– 5 to + 6	V
I_6 ; I_2	Pin 6 and Pin 2 Current	1	mA
I_{10}	Pin 10 Current	2	mA
I_{11}	Pin 11 Current	2	mA
I_{12}	Pin 12 Current	± 2	mA
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70$ °C	800	mW
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

TAB-01

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

TAB-02

ELECTRICAL CHARACTERISTICS

(refer to the test circuit ; V_S = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage Range (pin 1)		10.8		14.5	V
I_s	Supply Current (pin 1)	V_s = 14.5 V			30	mA
V_2	Output Voltage	$f_{tuning} < fo$ I_2 = 1 mA	V_s – 0.5			V
		$f_{tuning} = f_o$			0.8	V
		$f_{tuning} > f_o$			0.8	V

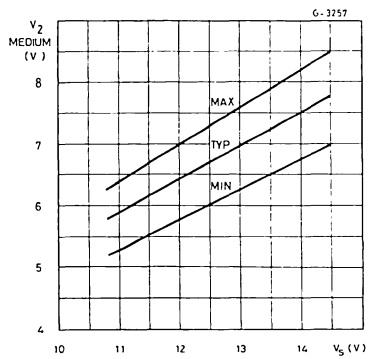
TAB-03

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_6	Output Voltage	$f_{tuning} < f_o$ I_6 = 1 mA			0.8	V
		$f_{tuning} = f_o$ I_6 = 1 mA			0.8	V
		$f_{tuning} > f_o$	V_s – 0.5			V
V_3	Input Voltage Range		4		8	V
V_{3U}	Upper Threshold Voltage (see fig. 2)		V_4 – 25	V_4	V_4 + 25	mV
V_{3L}	Lower Threshold Voltage (see fig. 2)		V_4 – 425	V_4 – 400	V_4 – 375	mV
R_3	Input Resistance	$V_3 = V_4$	1.4			MΩ
V_4	Regulated Voltage	I_4 = 1 mA		6.6		V
I_4	Output Current				1	mA
R_4	Output Differential Resistance			60		Ω
$\frac{\Delta V_4}{\Delta T_S}$	Regulated Voltage Thermal Drift				± 2	mV/°C
V_{10}	Identification Output Voltage	No Identification, I_{10} = 1 mA	V_s – 1.3			V
		Identification			20	mV
R_{10}	Output Resistance			100		Ω
V_{12}	Switch off Threshold Voltage				1	V
I_{12}	Input Flyback Current		0.5		1.5	mA
R_{12}	Input Resistance	V_{12} = 3 V		10		kΩ
t_{fly}	Flyback Pulse Duration		10		17	µsec.
t	Time Delay between Leading Edges of Flyback Pulse and Sync. Pulse.		0		3.5	µsec.
V_{13}	Video Input Signal (peak to peak)		2.5		4.5	V
V_{13}	Sync. Pulse Amplitude (above black level)		0.52			V
R_{13}	Input Resistance				1.5	kΩ

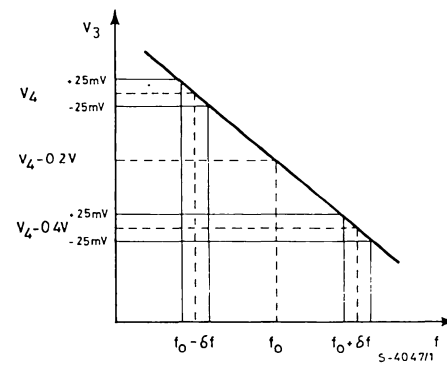
TAB-04

Figure 1 : Medium Output Voltage vs. Supply Voltage.



88DSTDA4433-03

Figure 2 : Digital AFC Threshold Voltage vs. Frequency.

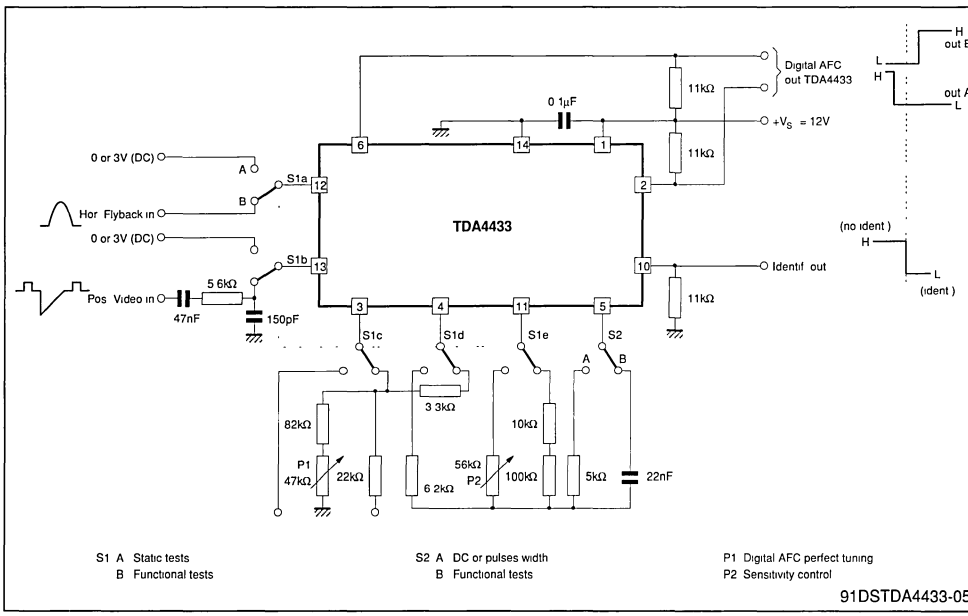


88DSTDA4433-04

Input Voltage (V_3)	TDA4433	
	Output Voltage (V_2)	Output Voltage (V_6)
$V_3 > V_4$	High level	Low Level
$V_4 - 0.4\ V < V_3 < V_4$	Low Level	Low Level
$V_2 < V_4 - 0.4\ V$	Low Level	High Level

TAB-05

TEST CIRCUIT



APPLICATION INFORMATION (refer to the block diagram)

TV SIGNAL IDENTIFICATION CIRCUIT :

The circuit recognizes only TV signals by checking logically during one line the coincidence between the horizontal flyback pulse and the pulse detected by a sync. separator.

The signal identification is carried out by charging the capacitor connected to pin 5 ; when the capacitor voltage overcomes a fixed threshold voltage, a Schmitt trigger switches and enables the AFC control. If a TV signal is recognized, the capacitor is slightly charged every line and its voltage reaches the threshold after a number of line which is defined by the value of the capacitor itself. The sensitivity of the identification circuit, hence the number of lines required to charge the capacitor, can be adjusted by means of the resistor connected between pin 11 and ground.

When the identification has been made, a signal (level L) is available at pin 10.

THRESHOLD CIRCUIT :

The circuit detects 3 ranges of AFC voltage and in combination with the TV signal identification circuit drives the electronic switches.

With a correct TV signal, the output levels corresponding to the 3 ranges are :

	TDA4433	
	(V_2)	(V_6)
$f_o - \delta f$	H	L
f_o	L	L
$f_o + \delta f$	L	H

TAB-06

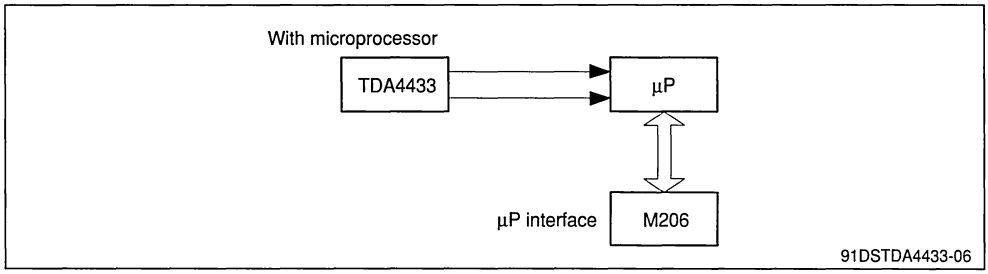
L = Low level.
H = High level.

The TDA4433 has two separate outputs which can have only two states, high (H) or low (L). The outputs at pin 2 and at pin 6 remain at a low level with no video signal input or with a video signal not identified as a true TV signal. Both pin 2 and pin 6 are open collector outputs and must be pulled-up to the positive supply voltage by external resistors.

VOLTAGE REGULATOR

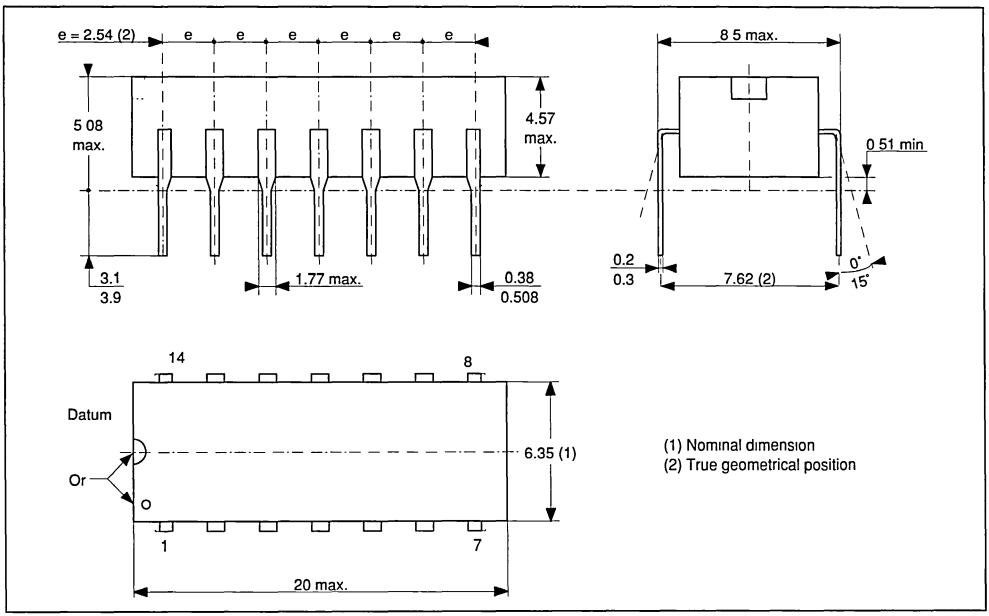
The circuit can deliver 1 mA and it can be used as D/A converter reference to supply fine tuning voltage.

EPM SYSTEM CONFIGURATIONS



PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

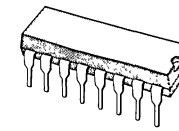
TDA4443

MULTISTANDARD VIDEO IF AMPLIFIER

- SWITCHING OFF THE IF AMPLIFIER WHEN OPERATING IN VTR MODE
- DEMODULATION OF NEGATIVE OR POSITIVE IF SIGNALS. THE OUTPUT REMAINS ON THE SAME POLARITY IN EVERY CASE
- IF AGC AUTOMATICALLY ADJUSTED TO THE ACTUAL STANDARD
- TWO AGC POSSIBILITIES FOR B/G MODE :
  1. GATED AGC
  2. UNGATED AGC ON SYNC. LEVEL AND CONTROLLED DISCHARGE DEPENDENT ON THE AVERAGE SIGNAL LEVEL FOR VTR AND PERI TV APPLICATIONS
  FOR STANDARD L : FAST AGC ON PEAK WHITE BY CONTROLLED DISCHARGE
- POSITIVE OR NEGATIVE GATING PULSE
- EXTREMELY HIGH INPUT SENSITIVITY
- LOW DIFFERENTIAL DISTORTION
- CONSTANT INPUT IMPEDANCE
- VERY HIGH SUPPLY VOLTAGE REJECTION
- FEW EXTERNAL COMPONENTS
- LOW IMPEDANCE VIDEO OUTPUT
- SMALL TOLERANCES OF THE FIXED VIDEO SIGNAL AMPLITUDE
- ADJUSTABLE, DELAYED AGC FOR PNP TUNERS

DESCRIPTION

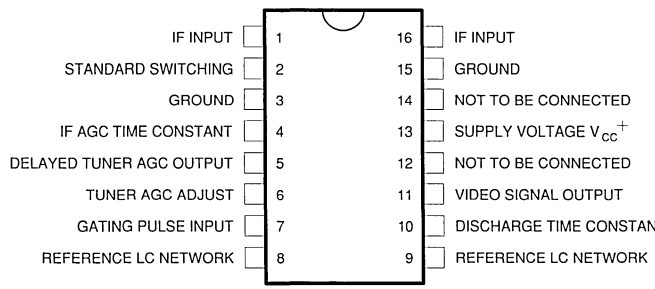
The TDA4443 is a Video IF amplifier with standard switch for multistandard colour or monochrome TV sets, and VTR's.



DIP16
(Plastic Package)

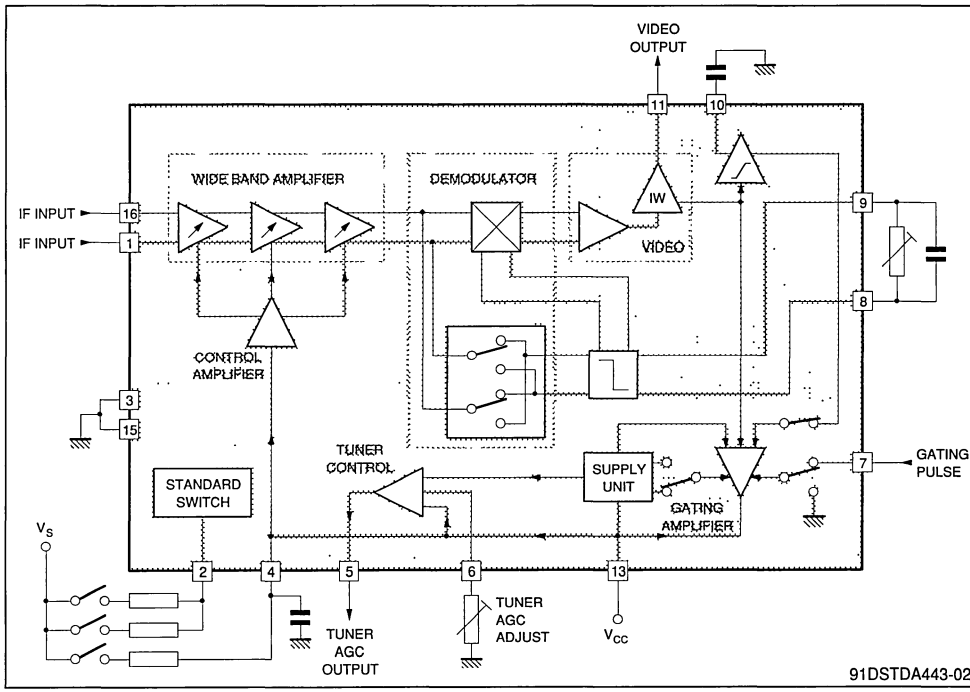
ORDER CODE : TDA4443

PIN CONNECTIONS



91DSTDA443-01

BLOCK DIAGRAM



GENERAL DESCRIPTION

This video IF processing circuit integrates the following functional blocks :

- Three symmetrical, very stable, gain controlled wideband amplifier stages - without feedback by a quasi-galvanic coupling.
- Demodulator controlled by the picture carrier
- Video output amplifier with high supply voltage rejection
- Polarity switch for the video output signal
- AGC on peak white level
- Gated AGC
- Discharge control
- Delayed tuner AGC
- At VTR Reading mode the video output signal is at ultra white level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage Range	Pin 13	15	V
V_0	Open Loop Voltage	Pin 5	max. V_{CC}	V
V_{ext}	External Voltage	Pin 4	12	V
I_4	Control Current for VTR Mode	Pin 4	0.3	mA
I_2	Control Current for Standard Mode	Pin 2	0.5	mA
I_0	Max. Video Output Current	Pin 11	5	mA
I_0	Short Circuit Current ($t \leq 1sec$)	Pin 11	30	mA
P_{tot}	Power Dissipation		1	W
T_j	Junction Temperature		125	°C
T_{AMB}	Ambient Temperature Range		0 to +70	°C
T_{stg}	Storage Temperature Range		-25 to +125	°C

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{AMB} = 25°C, V_{CC} = 12V, unless otherwise spacified. Test Circuit Page 5.

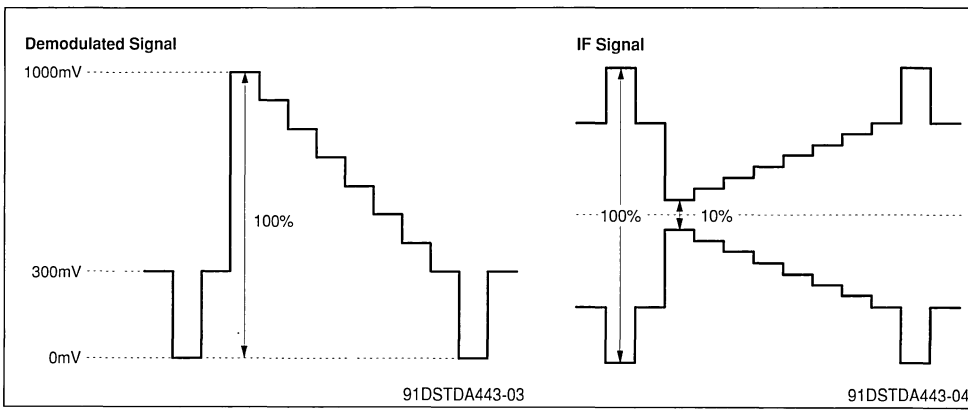
Symbol	Parameter	Pin	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	13	10	12	15	V
I_{CC}	Supply Current (V_{CC} = 12V, V_4 = 3.5V, V_{IN} = 0) Pin 6, PIn 7, PIn 2 open	13		55	75	mA
V_{11}	Ultra White Level at Standard B/G V_{CC} = 15V, V_4 = 3.5V	11	4.8	5.1	5.6	V
V_{AA}	Ultra Black Clamping Level at Standard B/G SIGNAL 1	11	1.70	1.85	2.10	V
V_O	Picture to sync. output voltage of the video signal without load in standard B/G (residual carrier 10%) SIGNAL 1	11	2.6	2.9	3.3	V_{PP}
V_O	Picture to blanking level output voltage of the video signal without load in standard L (blanking level at 28%of carrier amplitude) SIGNAL 2 (residual carrier 5%)	11	1.80	2.1	2.40	V_{PP}
$\frac{\Delta\ (V_p - V_{blank})}{V_p - V_{blank}}$	Output voltage change of the picture to blanking level from standard L to standard B/G (mode BG : signal 1, mode L : signal 2)	11			10	%
ΔVblack	Supply voltage influence on the ultra black level in standard B/G	11		0.5		%V
ΔVwhite	Supply voltage influence on the ultra white level in standard B/G	11		1		%V
ΔVvideo	Video Bandwidth Video Signal Attenuation with V_{IN} at 4.43MHz	11		1	1.5	dB
Bvideo	Video Bandwidth at -3dB	11	6			MHz
ΔVvideo	Video frequency response changes witin the AGC range	11		0.5	2.0	dB
I_O	DC Output Current (V_{11} = 10V, V_{CC} = 15V)	11		1.5	2	mA
I_7	Gating Pulse Current	7	0.30		1.0	mA
V_7	DC Voltage at Gating Input	7		1.3	1.6	V
V_1	Input Voltage Sensitivity V_{IN} (with V_{OUT} = V_O - 3dB) Standard B/G SIGNAL 1	1-16		120		μV_{RMS}
I	Control Current for Status B (see status of mode switching) V_2 = 5V	2		10	40	μA

ELECTRICAL OPERATING CHARACTERISTICS (continued)

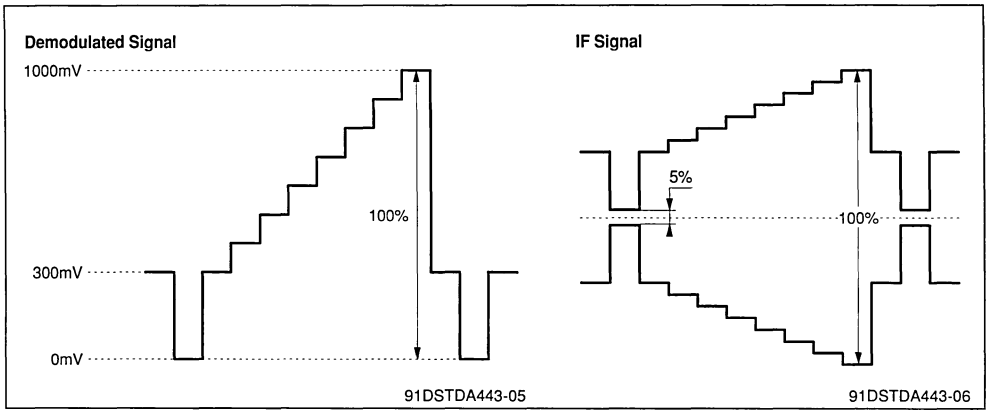
T_{AMB} = 25°C, V_{CC} = 12V, unless otherwise spacified. Test Circuit Page 5.

Symbol	Parameter	Pin	Min.	Typ.	Max.	Unit
I	Control Current Status C (see status of mode switching) V_2 = 6.3V	2		60	400	µA
ΔG_{IF}	IF AGC Range			60		dB
I_{AGC}	Available Tuner AGC Current (10dB above the AGC starting point)	5	8	12		mA
ΔAGC	Delay Between Tuner AGC and IF AGC (pin 6 not connected)	5		50		dB
VIF V2IF	IF residual carrier at the video o/p withing the AGC range 38.9MHz 77.8MHz	 11 11		 20 50		 mV_{RMS} mV_{RMS}
d	Differential Distortion on Composite VIdeo Signal Amplitude SIGNAL 3	11			5	%
aM	Attenuation of sound to color carrier intermodulation signal (1.07MHz) referred to the demodulated color carrier PIcture Carrier = 0dB Color Carrier = -6dB Sound Carrier = -24dB	11		50		dB
$\frac{\Delta Sync}{Sync}$	Sync. Pulse Compression within the IF AGC Range			3		%
RI CI	Input Impedance : Resistance Capacitance	1-16 1-16		2.5 2		kΩ pF
V	Switch off Control Voltage for VTR Mode	4	9		10	V
I	Switch off Current for VTR Mode	4			150	µA

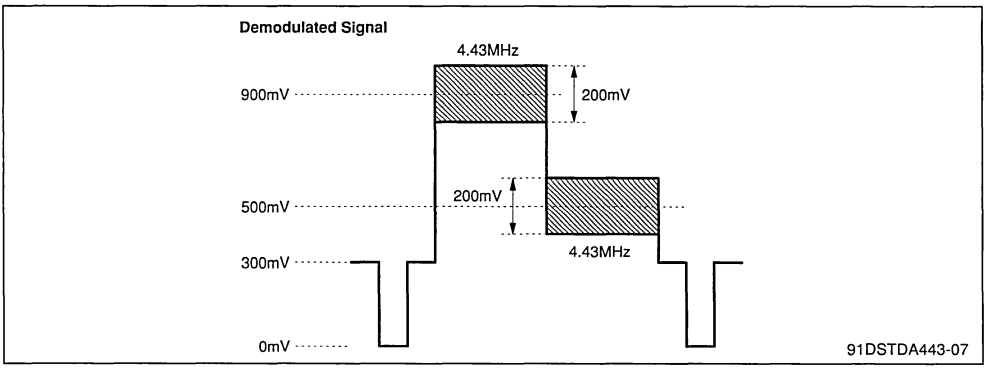
SIGNAL 1 (standard B/G)



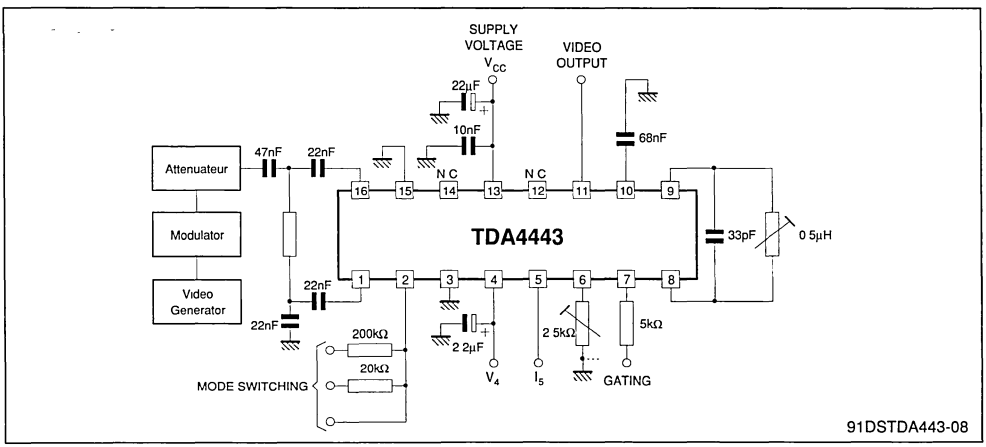
SIGNAL 2 (standard L)



SIGNAL 3



TEST CIRCUIT



DEFINITION OF MODE SWITCHING

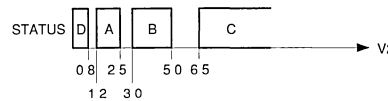
Status	Pin 2	Pin 4	Function
A	Not connected	No External Voltage	Standard B/G mode, gated charge and discharge.
B	12V HIgh Impedance	No External Voltage	Standard B/G, ungated, charging up to sync. level, discharging dependant from average signal (peri operation).
C	12V Low Impedance	No External Voltage	At standard L ungated, charging up to peak white level, discharge dependant from average signal level, inverted polarity of the video output.
D	No specifications	≥ 7.5V	In VTR reading mode the IF amplifier is blocked, turned gain controlled down : the video output signal is fixed at constant ultra white level for standard B/G mode.

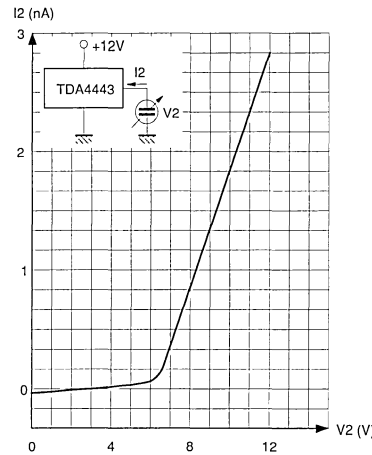
The gating pulse at Pin 7 is internally switched off.

STATUS OF MODE SWITCHING, REFERRING TO CONTROL VOLTAGE PIN 2

Control Voltage Pin 2	Connections of Pin 2	Status	Function
1.2 to 2.5V*	Open	A	Standard B/G gated sync. operation
3.0 to 5.0V	High Impedance	B	Standard B/G, no sync., operation
> 6.5V	Low Impedance	C	Standard L
0.0 to 0.8V	Ground	D	Standard L

* Voltage measured on Pin 2

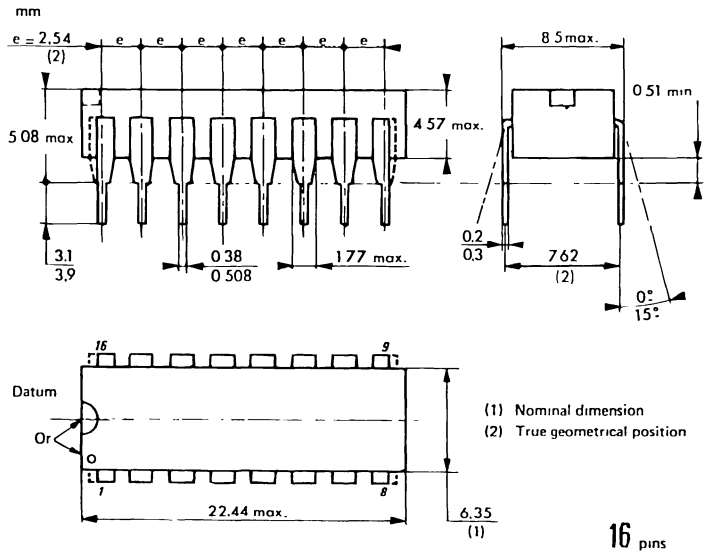




91DSTDA443-09

PACKAGE MECHANICAL DATA

16 PINS - PLASTIC DIP

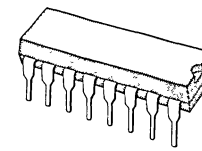


SGS-THOMSON MICROELECTRONICS

TDA4445A
TDA4445B

SOUND IF AMPLIFIER

- QUADRATURE INTERCARRIER DEMODULATOR
- VERY HIGH INPUT SENSITIVITY
- GOOD SIGNAL TO NOISE RATIO
- FAST AVERAGING AGC
- IF AMPLIFIER CAN BE SWITCHED OFF FOR VTR MODE
- GOOD AM SUPPRESSION
- OUTPUT SIGNAL STABILIZED AGAINST SUPPLY VOLTAGE VARIATIONS
- VERY FEW EXTERNAL COMPONENTS



DIP16
(Plastic Package)

ORDER CODE : TDA4445A - TDA4445B

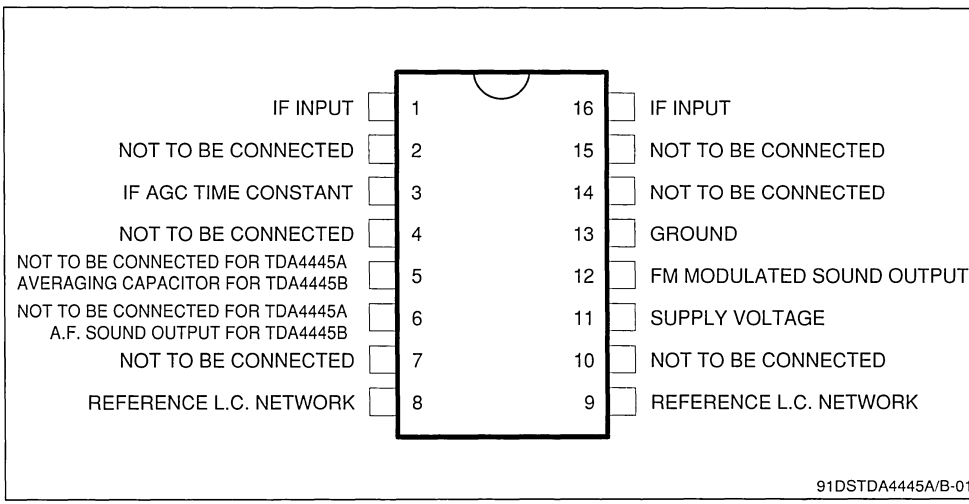
DESCRIPTION

TDA4445A :
Sound IF amplifier, with FM processing for quasi parallel sound system.

TDA4445B :
Sound IF amplifier, with FM processing and AM demodulator, for multi-standard sound TV appliances.

TDA4445B additionnal :
Bistandard applications (B/G and L)
No adjustment of the AM demodulator
Low AM distortion

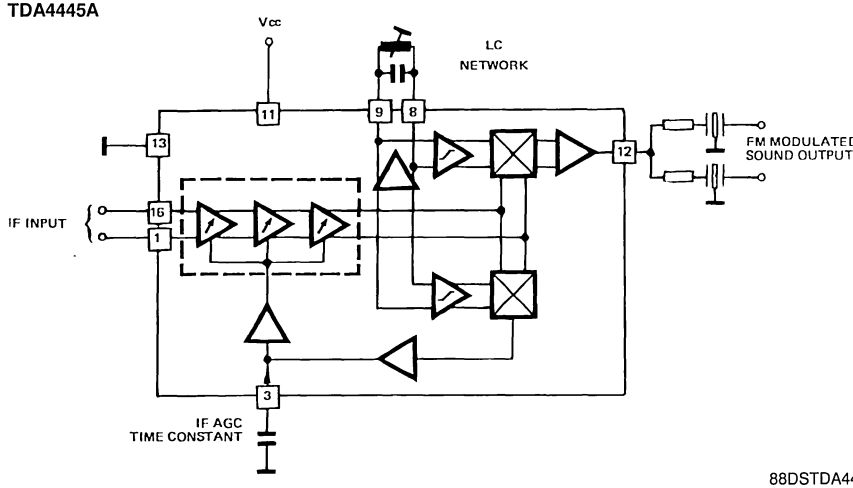
PIN CONNECTIONS



91DSTDA4445A/B-01

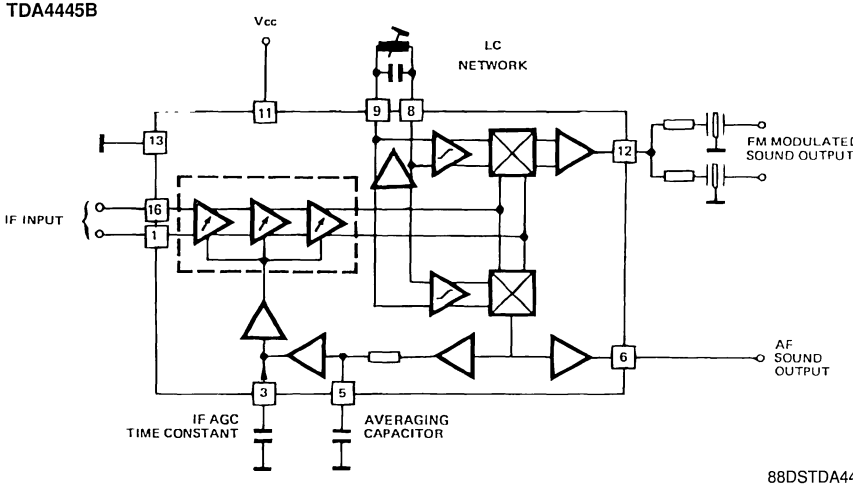
BLOCK DIAGRAMS

TDA4445A



88DSTDA4445A/B-02

TDA4445B



88DSTDA4445A/B-03

GENERAL DESCRIPTION

This circuit includes the following functions :

- Three symmetrical and gain controlled wide band amplifier stages, which are extremely stable by quasi DC coupling without feedback.
- Averaging AGC with discharge control circuit
- AGC voltage generator

Quasi parallel sound operation :

- High phase accuracy of the carrier signal processing, independent from AM
- Linear quadrature demodulator
- Sound-IF-amplifier stage with impedance converter

AM-Demodulation (only TDA4445B) :

- Carrier controlled demodulator
- Audio frequency stage with impedance converter
- Averaging low pass AGC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage Range	Pin 11	15	V
I_{CC}	Supply Current	Pin 11	70	mA
V_{ext} V_{ext}	External Voltages TDA4445A/TDA4445B	Pin 3 Pin 12	12 8	V V
V_{ext} V_{ext}	External Voltages only TDA4445B	Pin 5 Pin 6	8 8	V V
P_{tot}	Power Dissipation		1	W
T_j	Junction Temperature		125	°C
T_{amb}	Ambient Temperature Range		0 to + 70	°C
T_{stg}	Storage Temperature Range		– 25 to + 125	°C

TAB-01

THERMAL DATA

$R_{th(j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

TAB-02

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C, V_{CC} = 12V (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	DC CHARACTERISTICS					
V_{CC}	Supply Voltage	Pin 13	10	12	15	V
I_{CC}	Supply Current V_3 = 3.5V	Pin 11		45	60	mA
V_O	DC Output Voltage V_3 = 3.5V	Pin 12	4.25	5	5.75	V
I	Output DC Current V_3 = 3.5VV_{11} = 12V	Pin 12	1		2	mA
R	Input Impedance	Pins 1-16		2		kΩ
C		Pins 1-16		2		pF
V	Switch off Control Voltage for VTR Mode	Pin 3	9		10	V
I	Switch off Control Current for VTR Mode	Pin 3			150	µA
	AGC CHARACTERISTICS					
Δ_{GIF}	IF AGC Range			62		dB
	QUASI PARALLEL SOUND OPERATION (TDA4445A and TDA4445B) f_{PC} = 38.9MHz, f_{SC1} = 33.4MHz, f_{SC2} = 33.16MHz, PC/SC_1 = 13dB, PC/SC2 = 20dB, PC unmodulated Min. Input Voltage					
V_I	5.5MHz - Output Signal - 3dB	Pins 1-16		70		μV_{eff}
V_I	Max. Input Voltage 5.5MHz - Output Signal + 1dB	Pins 1-16		90		mV_{eff}
	Sound-IF-output Voltage V_{1-16} = 20mV_{eff} SC unmodulated					
V_O	5.5MHz Output Voltage	Pin 12	200		400	mV_{eff}
V_O	5.74MHz Output Voltage	Pin 12	100		300	mV_{eff}

TAB-03

ELECTRICAL OPERATING CHARACTERISTICS (continued)

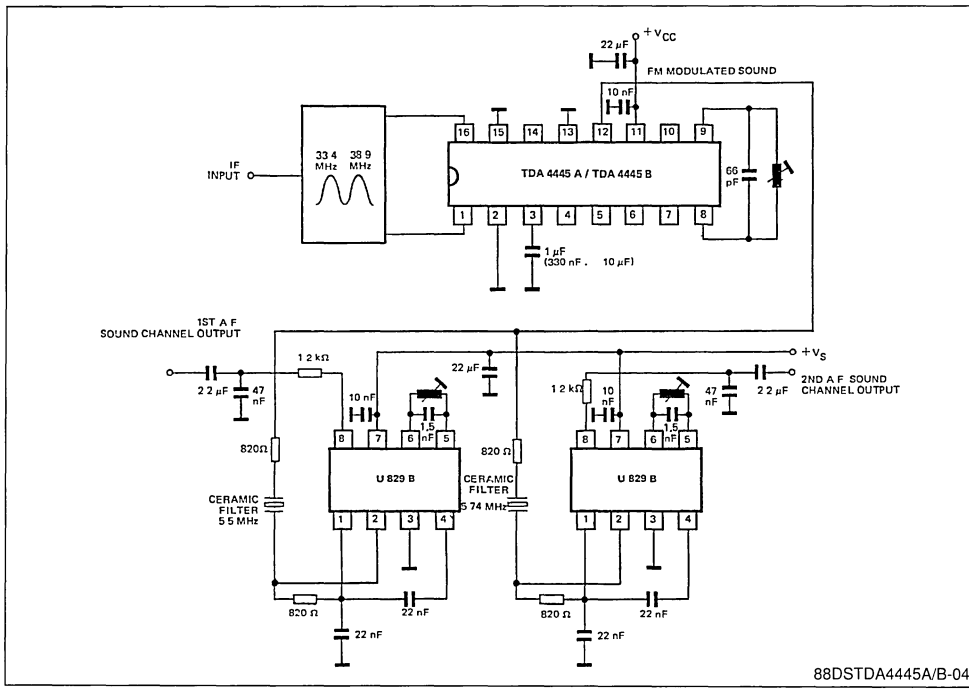
T_{amb} = + 25°C, V_{CC} = 12V (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Signal to noise ratio measured according to CCIR 468-2 Picture Modulation Ratio 90% Reference signal · V_{1-16} = 10mV, FM-frequency deviation30kHz → Out 1 350mV_{RMS} f_{mod} = 1kHz, measured at audio-output Out 2 350mV_{RMS}					
$\frac{S+N}{N}$	Black Screen 1. Channel/2. Channel					
$\frac{S+N}{N}$	Grid Screen 1. Channel/2. Channel	Pin 12 Pin 12		55/50 45/40		dB dB
V_I	AM DEMODULATION (TDA4445B only) f_{SC} = 39.2MHz, m = 80%, f_{mod} = 1kHz Min. Input Voltage Audio Output Signal - 3dB	Pins 1-16		70		μV_{eff}
V_O	Output DC Voltage V_{1-16} = 10mV_{eff} unmodulated	Pin 6	3.3		4.5	V
I	Output DC Current V_6 = 7.5V, V_3 = 3.5V	Pin 6	0.3		1.2	mA
d	Distortion V_{1-16} = 10mV, f_{mod} = 1kHz , m = 80%	Pin 6		2.5	4	%
V_O	AF Output Voltage V_{1-16} = 100mV_{eff}, m = 50% , f_{mod} = 10kHz	Pin 6	500	700	900	mV_{eff}

TAB-04

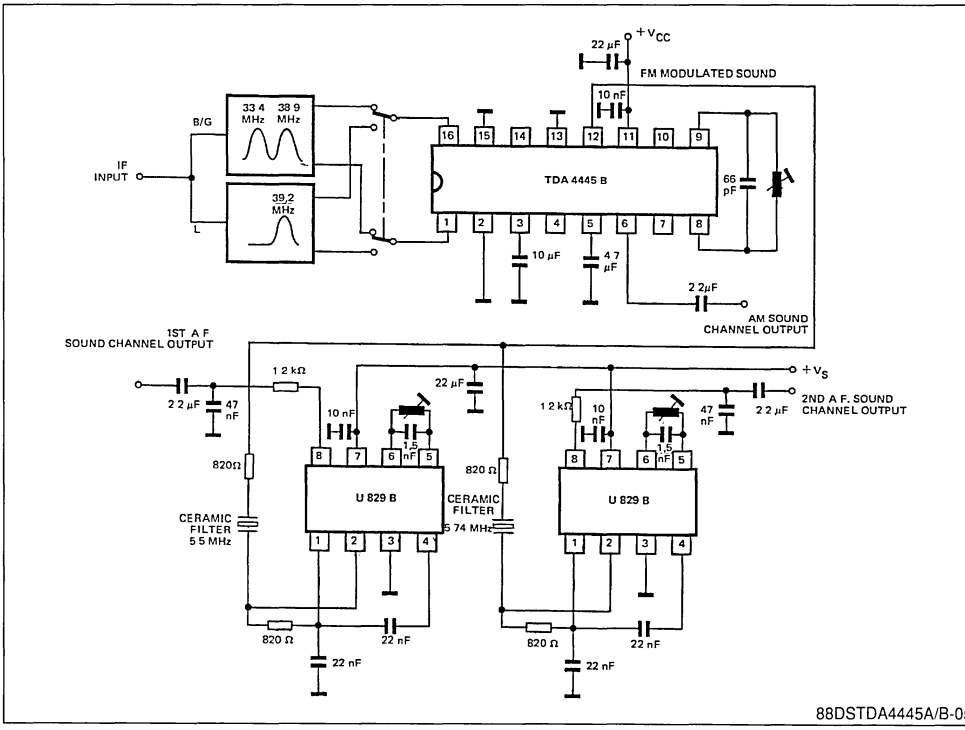
TYPICAL APPLICATION

Figure 1 : Quasi Parallel Sound Operation.

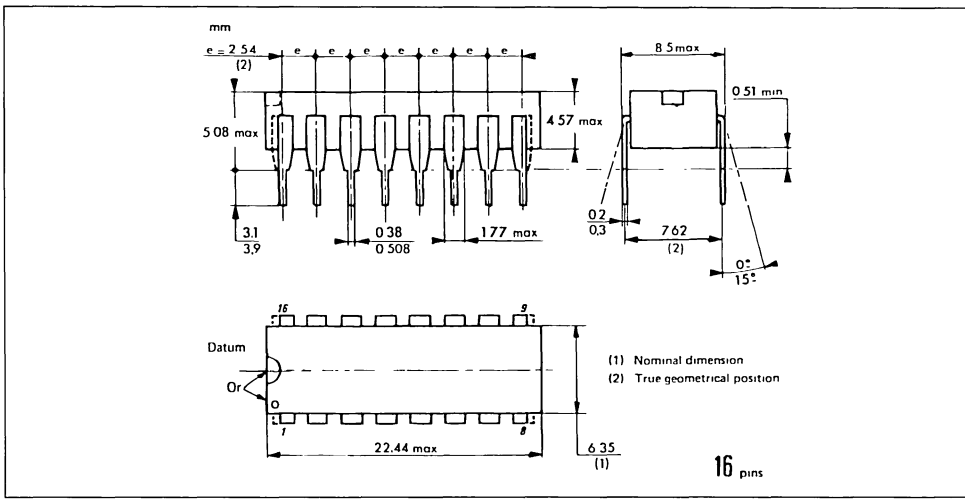


TYPICAL APPLICATION

Figure 2 : Bistandard Operation (FM stereo sound + AM sound).



PACKAGE MECHANICAL DATA : 16 PINS - PLASTIC DIP



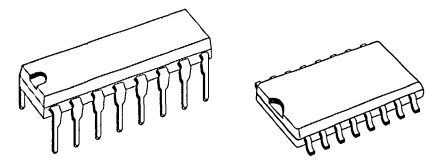
SGS-THOMSON MICROELECTRONICS

TDA7273

SINGLE CHIP STEREO CASSETTE PLAYBACK SYSTEM

ADVANCE DATA

- WIDE OPERATING SUPPLY VOLTAGE (1.8V to 7V)
- INPUT COUPLING WITHOUT CAPACITORS
- BUILT-IN DC STEREO VOLUME CONTROL
- BUILT-IN RIPPLE FILTERS
- LOW QUIESCENT CURRENT
- NO EXTERNAL BOUCHEROT CELL
- MAX OUTPUT CURRENT 70mA PEAK



DIP-16 **SO-16**

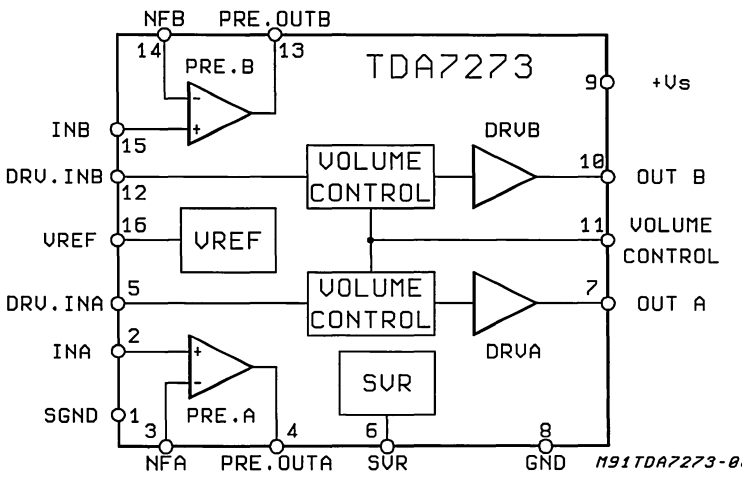
ORDERING NUMBERS:

TDA7273 TDA7273D

DESCRIPTION

The TDA7273 is a monolithic integrated circuit designed for portable cassette players market. It comprises preamplifiers, DC volume control, and headphone drivers.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Supply Voltage	9	V
I_o	Output Current (max)	70	mA
T_{op}	Operating Temperature Range	-20 to 70	°C
T_{stg}, T_j	Storage & Junction Temperature Range	-40 to +150	°C

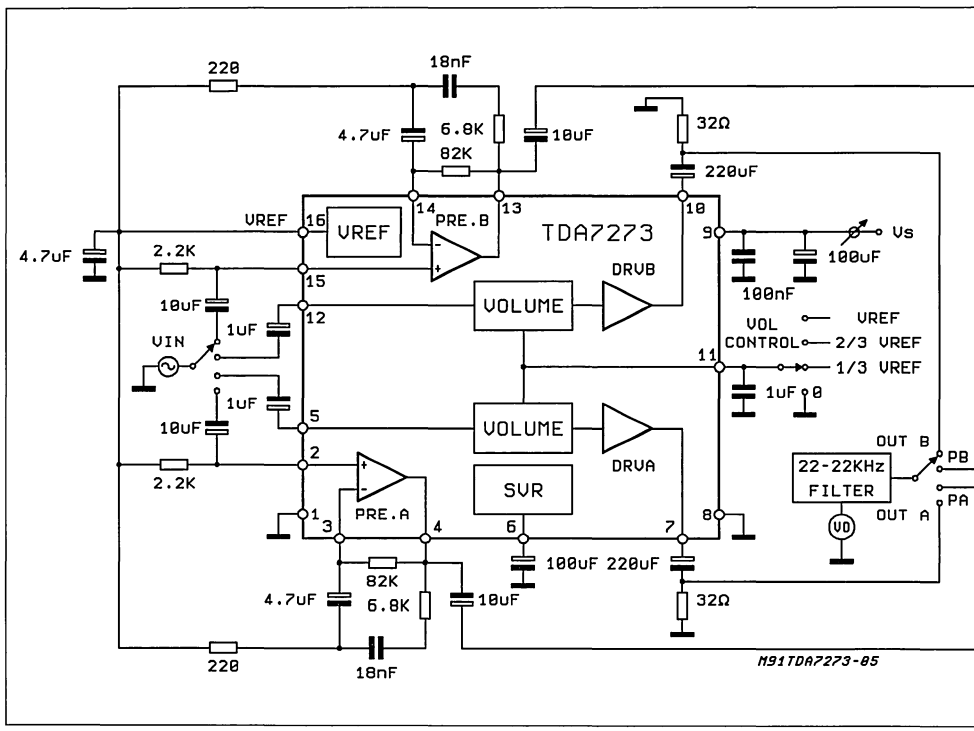
THERMAL DATA

Symbol	Description		DIP-16	SO-16	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	200	°C/W

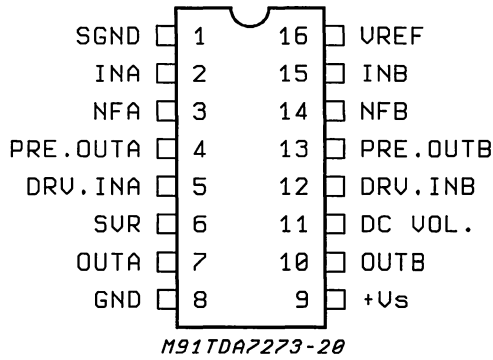
DC CHARACTERISTICS: T_{amb} = 25°C; V_S = 3V; R_L = 10KΩ (Preamplifier), R_L = 32Ω (Headphone); V_{IN} = 0; V_{OL} control = V_{ref}

Terminal No	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Terminal Voltage (V)	0	1.5	1.5	1.5	1.5	2.7	1.5	0	3	1.5	1.5	1.5	1.5	1.5	1.5	1.5

TEST CIRCUIT



PIN CONNECTION (Top view)



M91TDA7273-20

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 3V, f = 1KHz, R_L = 32Ω Vol. control = 2/3V_{ref} unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		1.8		7	V
I_d	Quiescent Current			14	20	mA
Vref	Reference Voltage		1.3	1.49	1.7	V
PREAMPLIFIER SECTION						
G_{VO}	Open Loop Gain			70		dB
G_V	Close Loop Gain		30	33	35	dB
V_o	Output Voltage	THD = 1%	600	850		mV
I_b	Bias Current			3		µA
THD	Total Harmonic Distortion	V_o = 330mVrms		0.05	0.25	%
C_t	Cross Talk	Rg = 2.2KΩ; V_o = 330mVrms		74		dB
E_N	Output Noise	Rg = 2.2KΩ; BW = 22Hz to 22KHz		100		µV
SVR	Ripple Rejection	R_g = 2.2KΩ V_R = 100mVrms f = 100Hz; C_{SVR} = 100µF	40	50		dB
HEADPHONE DRIVER						
$V_{o(DC)}$	DC Output Voltage			1.50		V
P_o	Output Power	THD = 10%;	15	30		mW
P_o	Transient Output Power	THD = 10% RL = 16Ω		50		mW
G_V	Close Loop Gain	P_o = 5mW	28	31	34	dB
THD	Total Harmonic Distortion	P_o = 5mW		0.2	1	%
C_t	Cross Talk	Rg = 10KΩ; P_o = 5mW	40	50		dB
SVR	Ripple Rejection	V_r = 100mVrms, f = 100Hz Vol. control = 1/3V_{ref} C_{SVR} = 100µF; R_g =600Ω		47		dB
	Volume Control Range		66	75		dB

Figure 1: Application Circuit

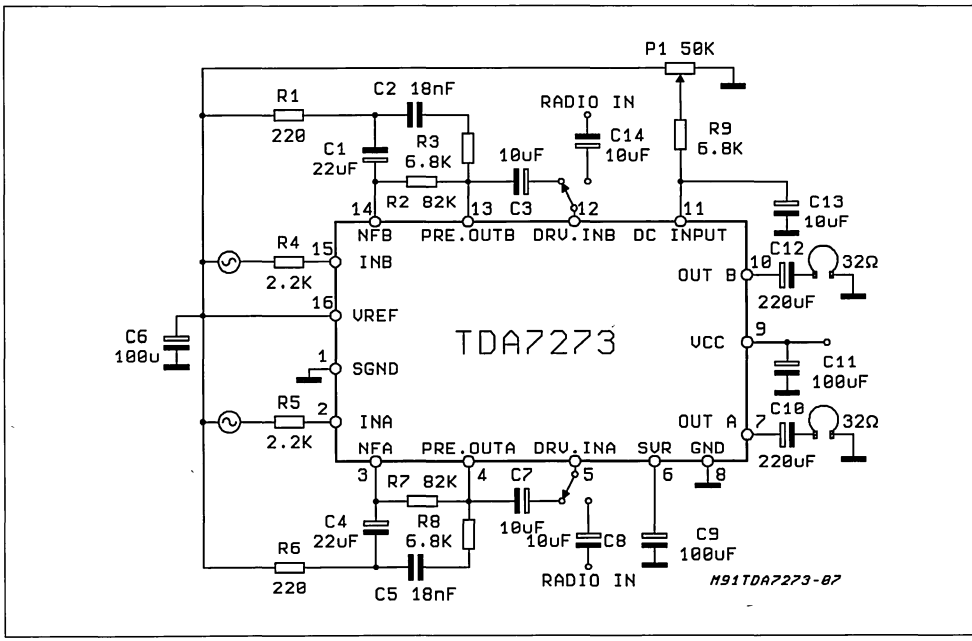


Figure 2: P.C. Board and Component Layout of the Circuit of Figure 1 (1:1 scale)

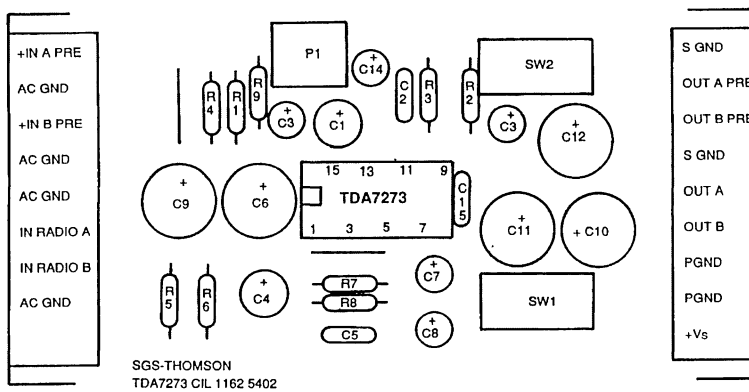


Figure 3: Supply Current vs. Supply Voltage (Preamplifier + Driver)

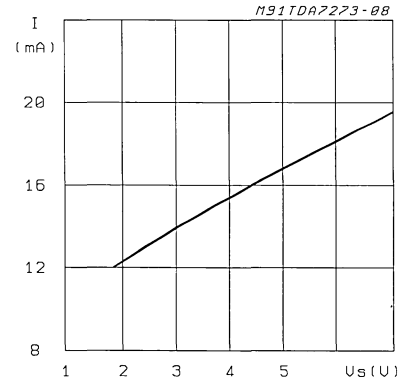


Figure 4: V_{ref}, vs. Supply Voltage (pin 16)

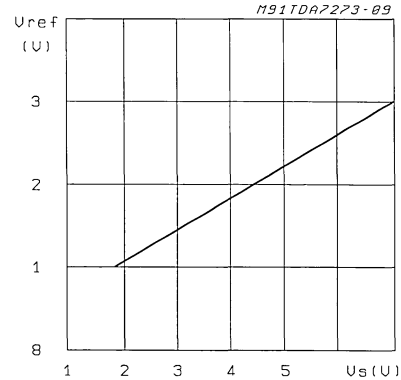


Figure 5: Closed Loop Gain vs. Frequency (V_S = 3V) (PREAMPLIFIER)

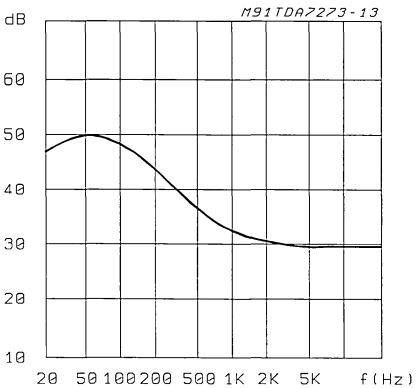


Figure 6: THD vs. Frequency (V_S = 3V, V_o =330mVrms, R_L = 10KΩ) (PREAMPLIFIER)

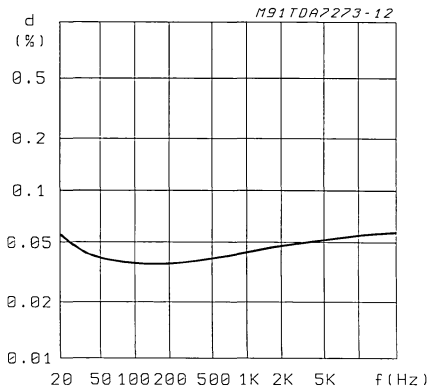


Figure 7: SVR vs. Frequency (PREAMPLIFIER)

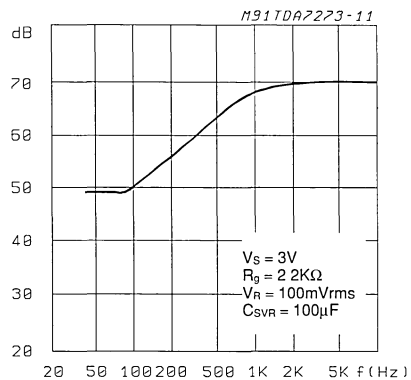


Figure 8: Quiescent Output Voltage vs. Supply Voltage (DRIVER)

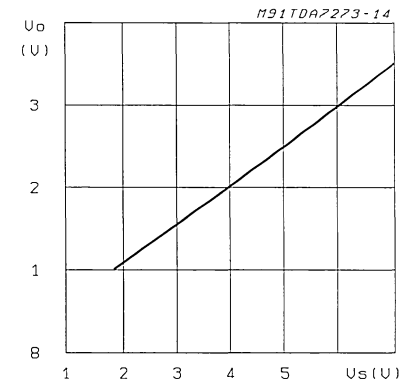


Figure 9: Closed Loop Gain vs Frequency (V_S = 3V, R_L = 32Ω) (DRIVER)

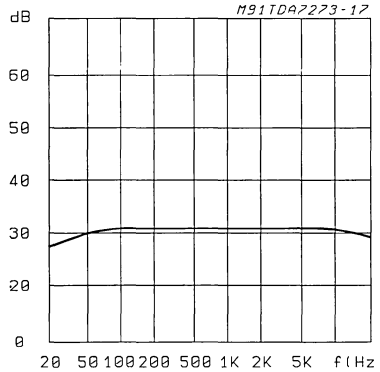


Figure 10: Output Power vs. Supply Voltage (Vol = $2/3V_{ref}$, R_L = 32Ω, THD = 10%, f = 1KHz) (DRIVER)

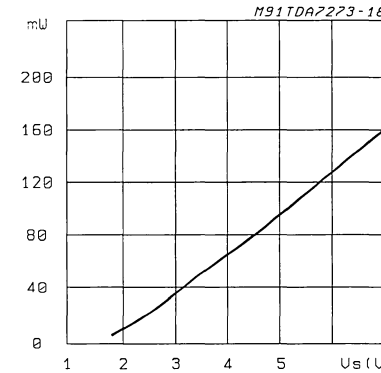


Figure 11: THD vs. Output Power (V_o = $2/3V_{ref}$, V_S = 3V, R_L = 32Ω, f = 1KHz) (DRIVER)

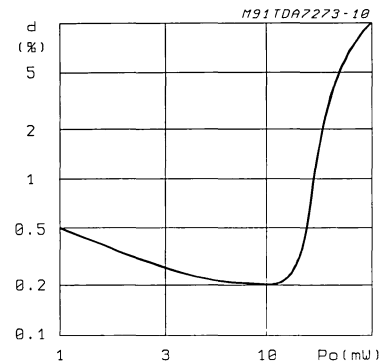


Figure 12: THD vs. Frequency (P_o = 5mW, V_S = 3V R_L = 32Ω) (DRIVER)

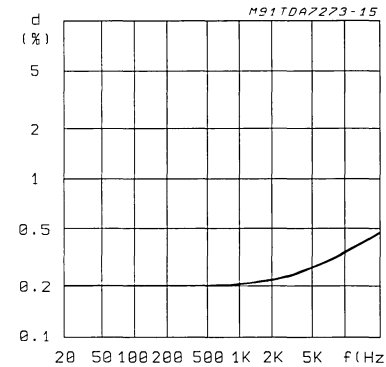


Figure 13: SVR vs. Frequency V_S = 3V (R_L = 32Ω, V_r = 100Vrms R_g = 600Ω, C_{SVR} = 100mV) (DRIVER)

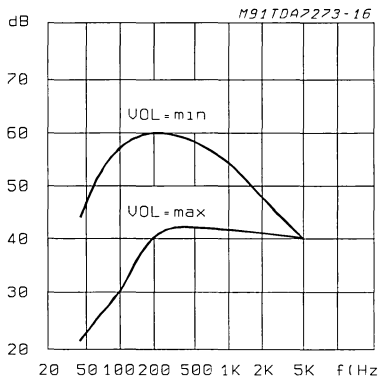
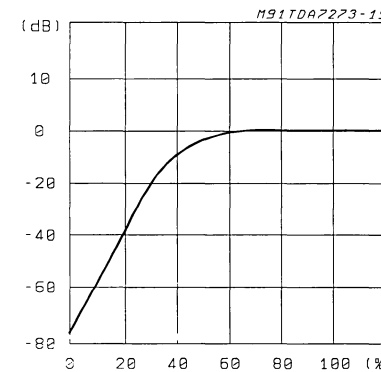
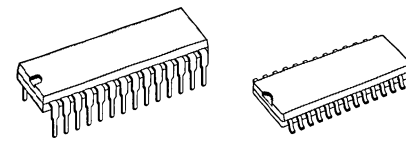


Figure 14: Volume Control (0dB = 10mW, V_S = 3V R_{vol} = 50KΩ, R_L = 32Ω, f = 1KHz) vs. Volume Setting (DRIVER)



DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

- SINGLE SUPPLY OPERATION
- FOUR STEREO INPUT SOURCE SELECTION
- MONO INPUT
- TREBLE, BASS, VOLUME, AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (FRONT/REAR)
- SINGLE SUPPLY OPERATION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING



DIP28 **SO28**

ORDERING NUMBERS:

TDA7300 TDA7300D

DESCRIPTION

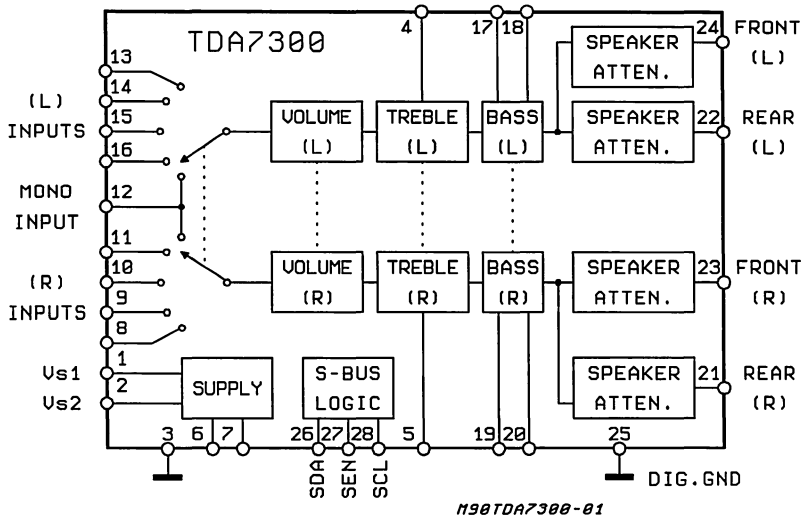
The TDA7300 is a volume, tone (bass and treble), balance (left/right) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi systems.

Control is accomplished by serial bus microprocessor interface.

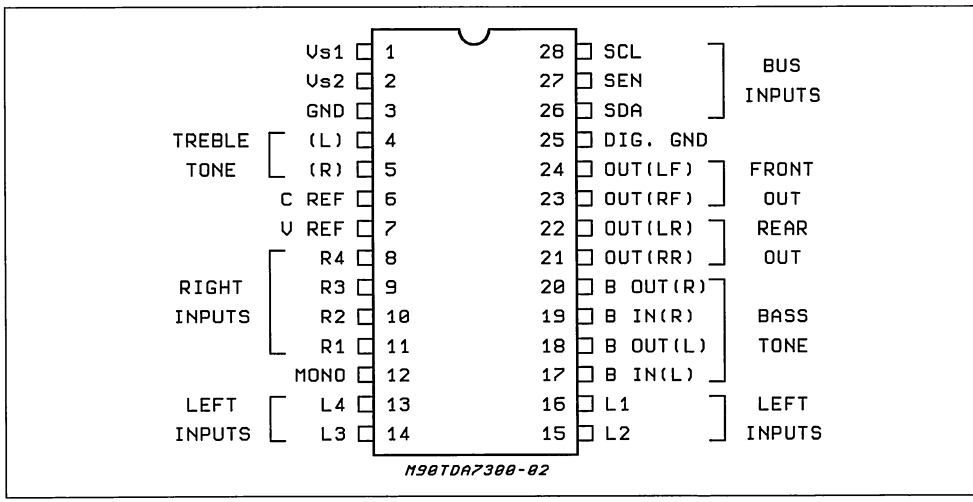
The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.

The results are: low noise, low distortion and high dynamic range.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (V_{S1})	18	V
T_{amb}	Operating Ambient Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		SO28	DIP28	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	85	65	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{S1} = 12V or V_{S2} = 8.5V , R_L = 10kΩ and R_g = 600Ω , f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY (1)						
V_{S1}	Supply Voltage VS1		10	12	16	V
V_{S2}	Supply Voltage VS2		6	8.5	10	V
I_{S2}	Supply Current		15	30	40	mA
V_{ref}	Reference Voltage (pin 7)		3.5	4.3	5	V
SVR	Ripple Rejection at V_{S1}	f = 300Hz to 10KHz	80	97		dB
SVR	Ripple Rejection at V_{S2}	f = 300Hz to 10KHz	50	58		dB
INPUT SELECTORS						
R_i	Input Resistance		30	45		KΩ
$V_{IN\ max}$	Max. Input Signal	GV = 0dB d = 0.3%	1.5	2.2		Vrms
IN_S	Input Separation	f = 1KHz (2)	90	100		dB
		f = 10KHz (2)	70	80		dB
$V_{I\ (DC)}$	Input DC Voltage		3.5	4.3	5	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOLUME CONTROLS						
	Control Range			78		dB
G_{max}	Max Gain		8	10	12	dB
	Max Attenuation		64	68		dB
	Step Resolution	G_V = -50 to 10dB		2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB
SPEAKER ATTENUATORS						
	Control Range		35	38	41	dB
	Step Resolution			2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB
BASS AND TREBLE CONTROL (3)						
	Control Range			±15		dB
	Step Resolution			2.5	3.5	dB
AUDIO OUTPUT						
V_O	Max. Output Voltage	d = 0.3%	1.5	2.2		Vrms
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				1	nF
R_O	Output Resistance			70	150	Ω
V_O(DC)	DC Voltage Level		3	3.8	4.5	V
GENERAL						
e_{NO}	Output Noise	BW = 22Hz to 22KHz, G_v = 0dB		6	15	μV
		Curve A G_v = 0dB		4		
S/N	Signal to Noise Ratio	All gain = 0dB V_O = 1Vrms BW = 22Hz to 22KHz		105		dB
d	Distortion	f = 1KHz; V_O = 1V; G_v = 0		0.01	0.1	%
	Frequency Response (-1dB)	G_v = 0 High Low	20		20	KHz Hz
S_C	Channnel Separation left/right	f = 1KHz f = 10KHz	90 70	100 80		dB dB
BUS INPUTS						
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.4			V
V_O	Output Voltage SDA Acknowledge	I = 1.6mA			0.4	V
	Digital Input Current		-5		+5	μA

Notes:

(1) The circuit can be supplied either at V_{S1} or without the use of the internal voltage regulator at V_{S2} . The circuit also operates at a supply voltage V_{S1} lower than 10V. In this case the ripple rejection of V_{S2} is valid, because the voltage regulator saturates to a saturation voltage of about 0 8V.

(2) The selected input is grounded thru the 2.2μF capacitor

(3) Bass and Treble response see attached diagram The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.

Figure 1: Application Circuit

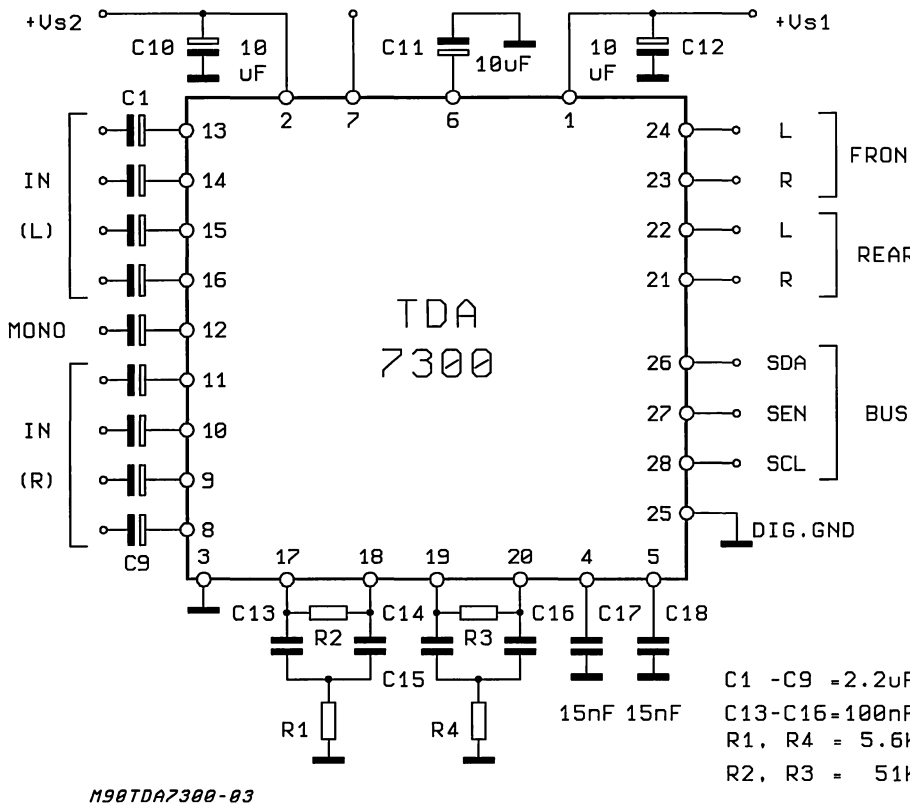


Figure 2: P.C. Board and Components Layout of the Fig.1 (1:1 scale)

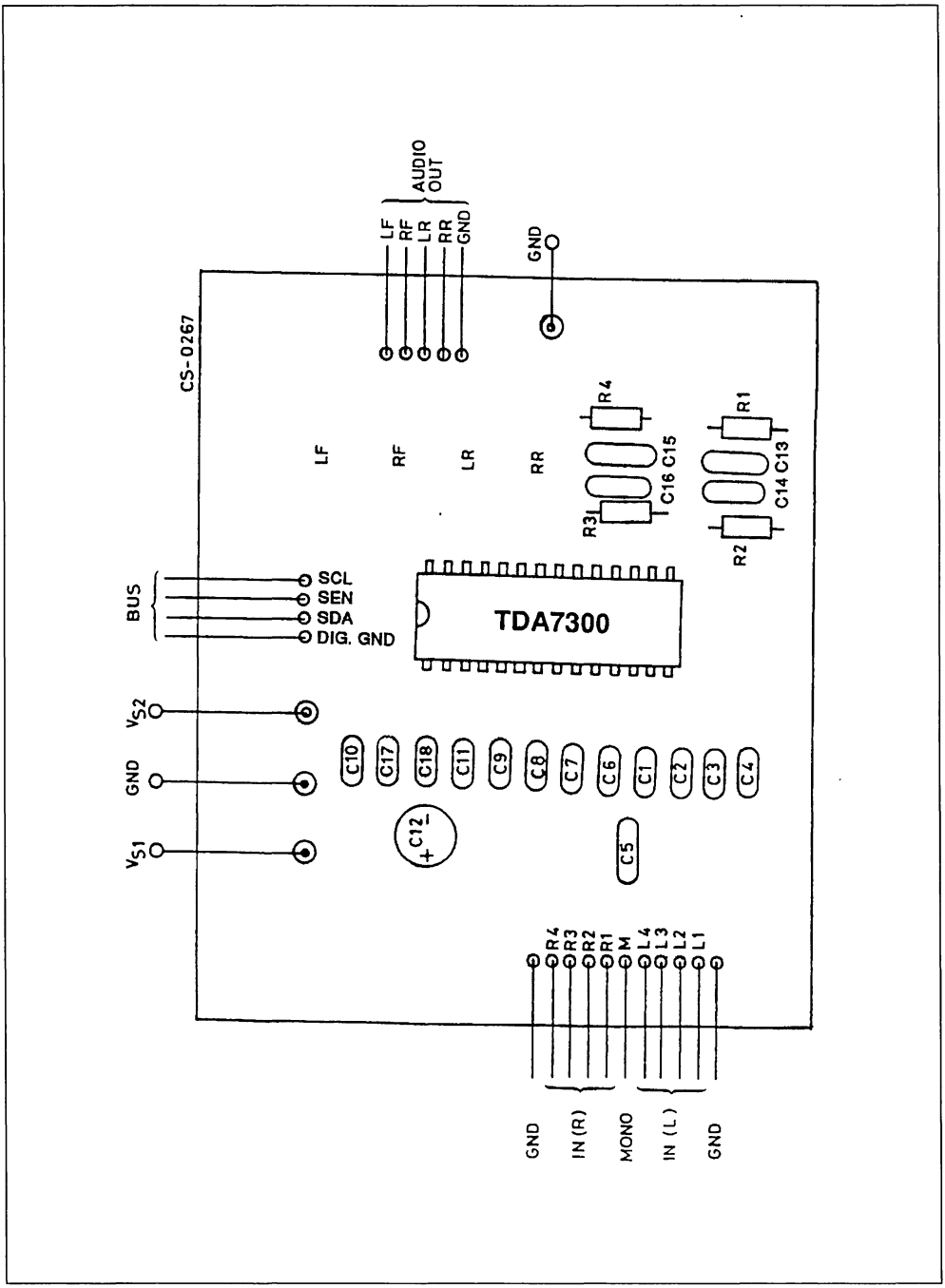


Figure 3: Total Output Noise vs. Volume Setting

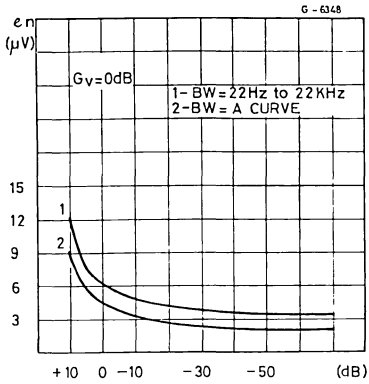


Figure 4: Signal to Noise Ratio vs. Volume Setting

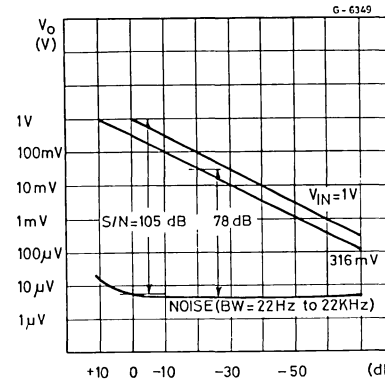


Figure 5: Distortion + Noise vs. Frequency

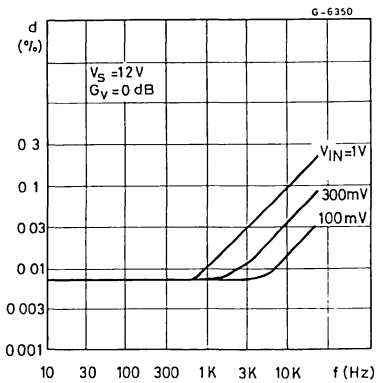


Figure 6: Distortion vs. Output Voltage

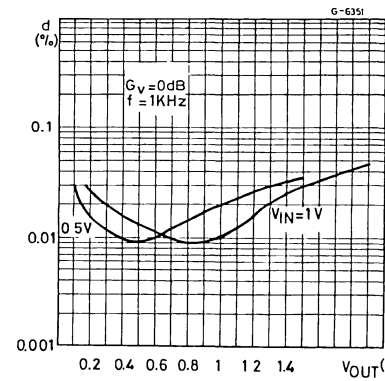


Figure 7: Distortion vs. Load Resistance

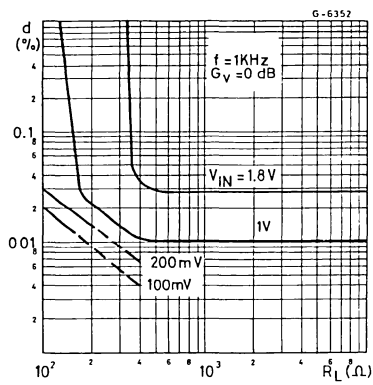


Figure 8: Channel Separation (L1 - R1) vs. Frequency

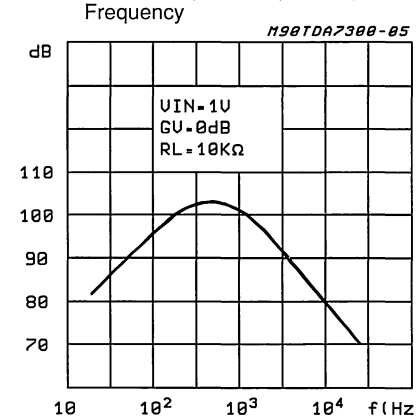


Figure 9: Input Separation (L1 - L2) vs. (V_{S1}) Frequency

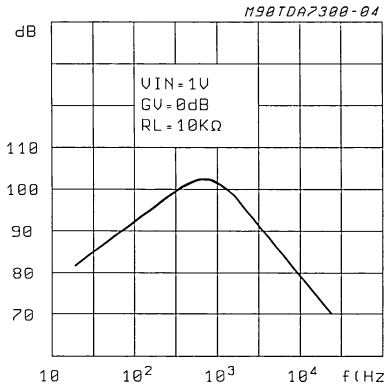


Figure 10: Supply Voltage Rejection (V_{S1}) vs. Frequency

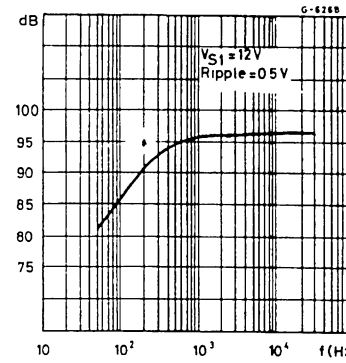


Figure 11: Supply Voltage Rejection (V_{S2}) vs. Frequency

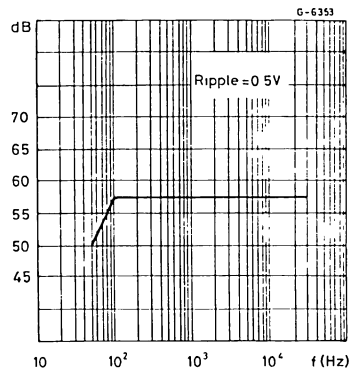


Figure 12: Supply Voltage Rejection vs. V_{S1}

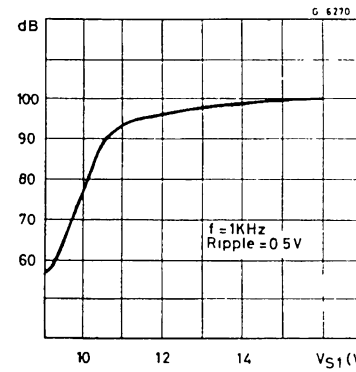


Figure 13: Supply Voltage Rejection vs. V_{S2}

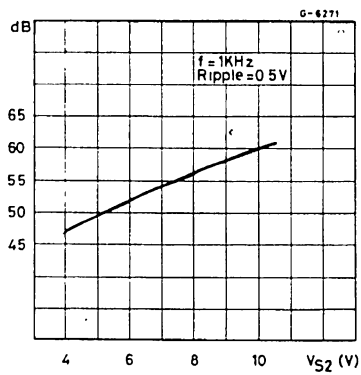
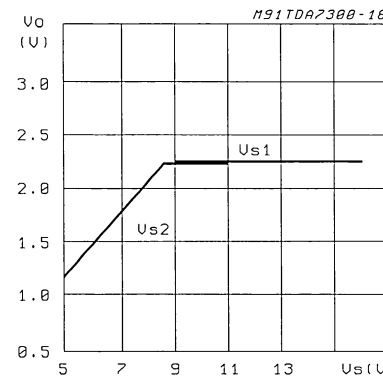


Figure 14: Clipping Level (Vrms) vs. Supply Voltage



APPLICATION INFORMATION

Volume Control Concept

Traditional electronic volume control circuits use a multiplier technique with all the disadvantages of high noise and distortion.
The used concept, as shown in Fig. 15 with digital switched resistor dividers, provides extremely low noise and distortion. The multiplexing of the resistive dividers is realized with a multiple-input operational amplifier.

Bass and Treble Control

The principle operation of the bass control is shown in Fig. 16. The external filter together with the internal buffer allows a flexible filter design according to the different requirements in car radios. The function of the treble is similar to the bass.
A typical curve is shown in Fig.19.

Outputs

A special class-A output amplifier with a modulated sink current provides low distortion and ground compatibility with low current consumption.

Figure 15: Volume Control

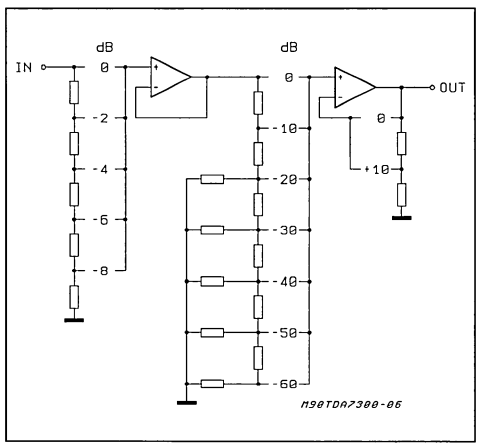


Figure 16: Bass Control

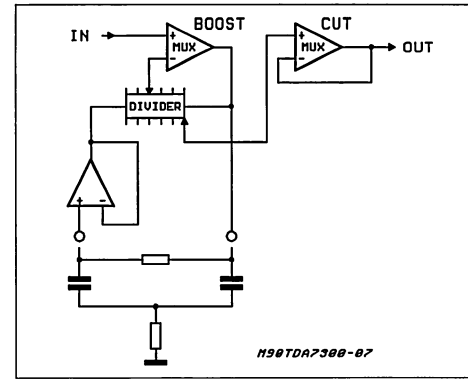


Figure 17: Quiescent Current vs. Supply Voltage

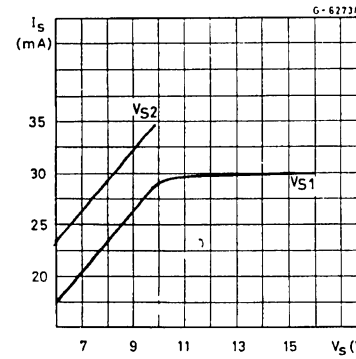
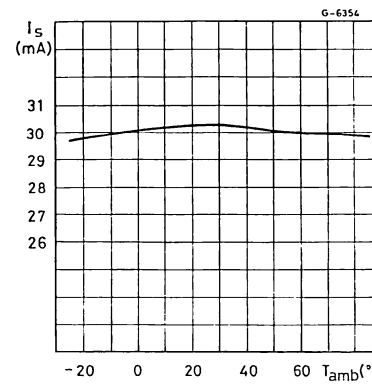


Figure 18: Quiescent Current vs. Temperature



APPLICATION INFORMATION (continued)

Figure 19: Typical Tone Response

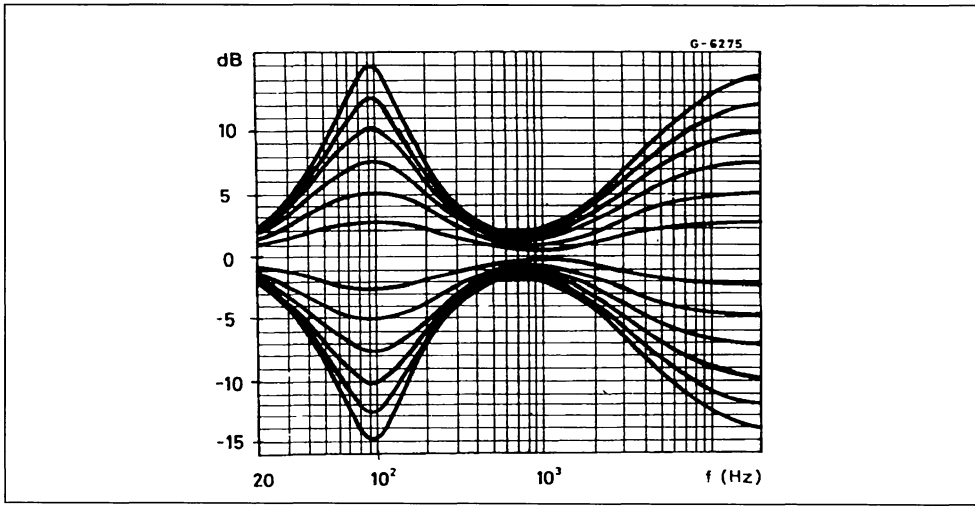
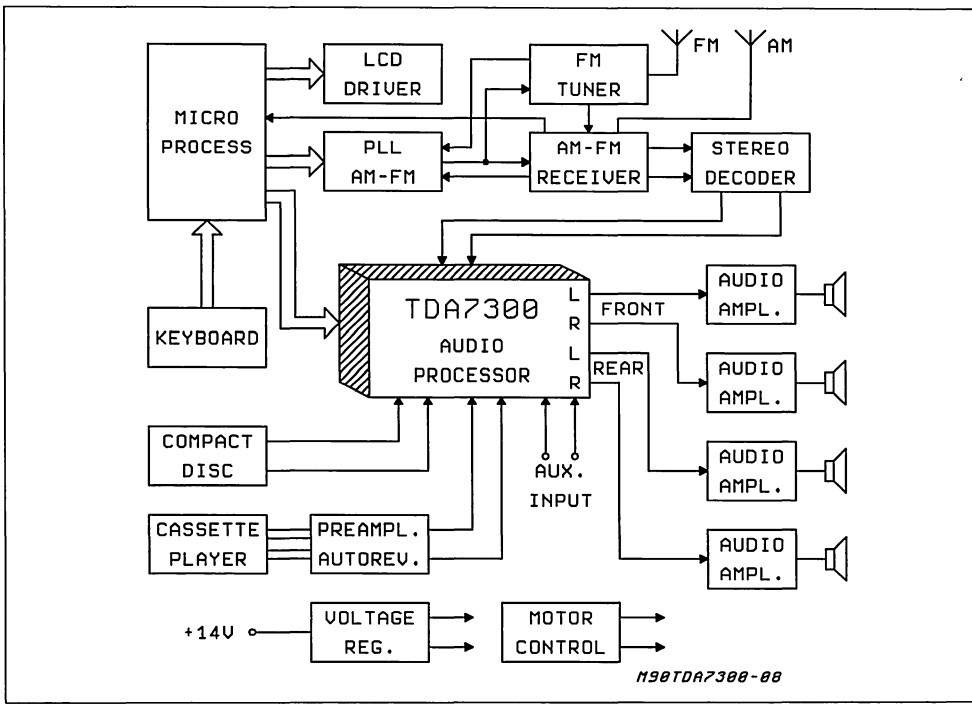


Figure 20: Complete Car-Radio System using Digital Controlled Audio Processor



APPLICATION INFORMATION (continued)

SERIAL BUS INTERFACE

S-BUS Interface and I²CBUS Compatibility

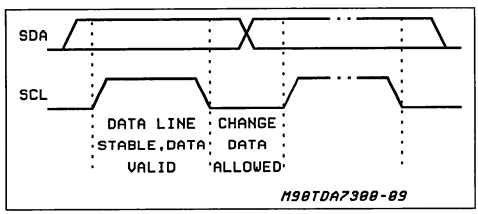
Data transmission from microprocessor to the TDA7300 and viceversa takes place thru the 3-wire S-BUS interface, consisting of the three lines SDA, SCL, SEN. If SDA and SEN inputs are short-circuited together, then the TDA7300 appears as a standard I²CBUS slave.

According to I²CBUS specification the S-BUS lines are connected to a positive supply voltage via pull-up resistors.

Data Validity

As shown in fig. 21, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Figure 21: Data Validity on the I²CBUS



Start and Stop Conditions

I²CBUS:
as shown in fig.22 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

S-bus:
the start/stop conditions (points 1 and 6) are detected exclusively by a transition of the SEN line ($1 \rightarrow 0$ / $0 \rightarrow 1$) while the SCL line is at the HIGH level.

The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). After the start information (point 1) the SEN line returns to the HIGH level and remains unchanged for all the time the transmission is performed.

Byte Format

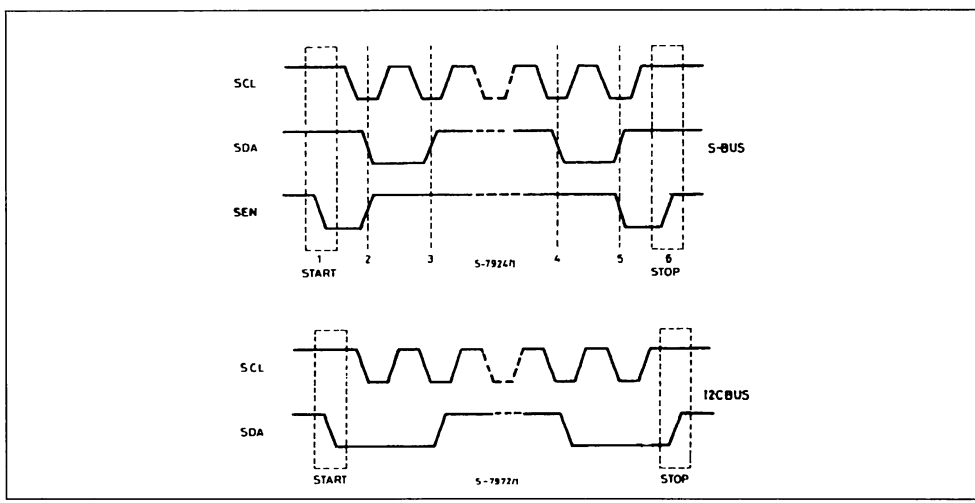
Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

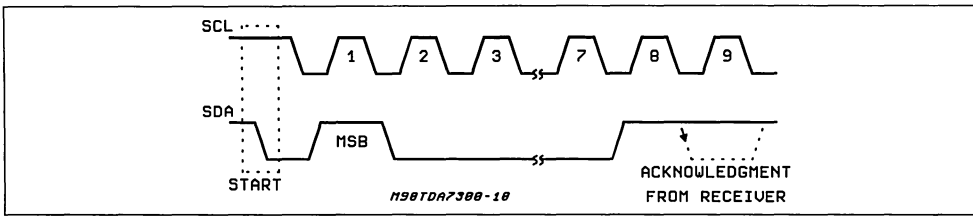
The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 23). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Figure 22: Timing Diagram of S-BUS and I²CBUS



APPLICATION INFORMATION (continued)
Figure 23: Acknowledge on the I^2CBUS



Transmission without Acknowledge

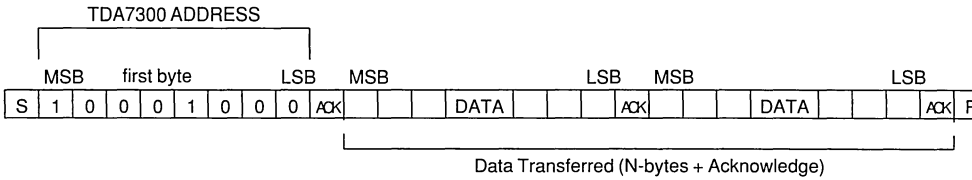
Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7300 address (the 8th bit of the byte must be 0). The TDA7300 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address (TDA7300 address)

1	0	0	0	1	0	0	0
MSB							LSB

DATA BYTES

Status after power-on reset

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	X	X	S2	S1	S0	Audio Switch
0	1	1	0	C3	C2	C1	C0	Bus Control
0	1	1	1	C3	C2	C1	C0	Treble Control

X = don't care
Ax = 2dB steps
Bx = 10dB steps
Cx = 2.5dB steps

STATUS AFTER POWER-ON-RESET

Volume	– 68 dB
Speaker	– 38 dB
Audio Switch	Mono
Bass	+ 2.5 dB
Treble	+ 2.5 dB

SOFTWARE SPECIFICATION (continued)
DATA BYTES (detailed description)

VOLUME

MSB							LSB	
0	0	B2	B1	B0	A2	A1	A0	Volume 2dB Steps
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
0	0	B2	B1	B0				Volume 10dB steps
		0	0	0				+10
		0	0	1				0
		0	1	0				-10
		0	1	1				-20
		1	0	0				-30
		1	0	1				-40
		1	1	0				-50
		1	1	1				-60

For example if you want setting the volume at -32dB the 8 bit string is: 0 0 1 0 0 0 0 1

SPEAKER ATTENUATORS

MSB							LSB	
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30

For example attenuation of 24dB on speaker RF is given by: 1 0 1 1 0 0 1 0

SOFTWARE SPECIFICATION (continued)

AUDIO SWITCH - Select the input Channel to Activate

MSB							LSB	
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Stereo 4
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care

For example to set the stereo 2 channel the 8 bit string may be: 0 1 0 0 0 0 0 1

BASS AND TREBLE - Control Range of ± 15 dB (boost and cut) Steps of 2.5 dB

0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	– 15
				0	0	0	1	– 15
				0	0	1	0	– 12.5
				0	0	1	1	– 10
				0	1	0	0	– 7.5
				0	1	0	1	– 5
				0	1	1	0	– 2.5
				0	1	1	1	– 0
				1	1	1	1	+ 0
				1	1	1	0	+ 2.5
				1	1	0	1	+ 5
				1	1	0	0	+ 7.5
				1	0	1	1	+ 10
				1	0	1	0	+ 12.5
				1	0	0	1	+ 15
				1	0	0	0	+ 15

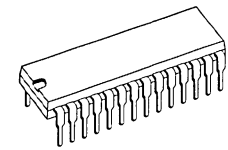
C3 = Sign

For example Bass at -12.5dB is obtained by the following 8 bit string: 0 1 1 0 0 0 1 0

Purchase of I^2C Components of SGS-THOMSON Microelectronics, conveys a licence under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specifications as defined by Philips.

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

- INPUT AND OUTPUT PINS FOR EXTERNAL EQUALIZER
- THREE STEREO INPUT SOURCE SELECTION PLUS MONO INPUT
- TREBLE, BASS, VOLUME AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (FRONT/REAR)
- SINGLE SUPPLY OPERATION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING



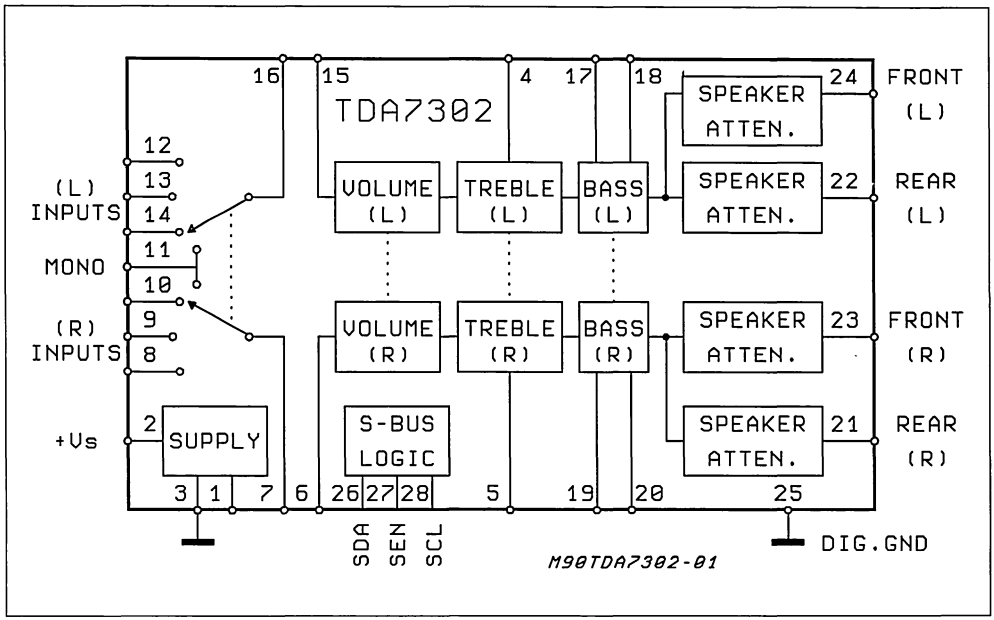
DIP28
ORDERING NUMBER: TDA7302

DESCRIPTION

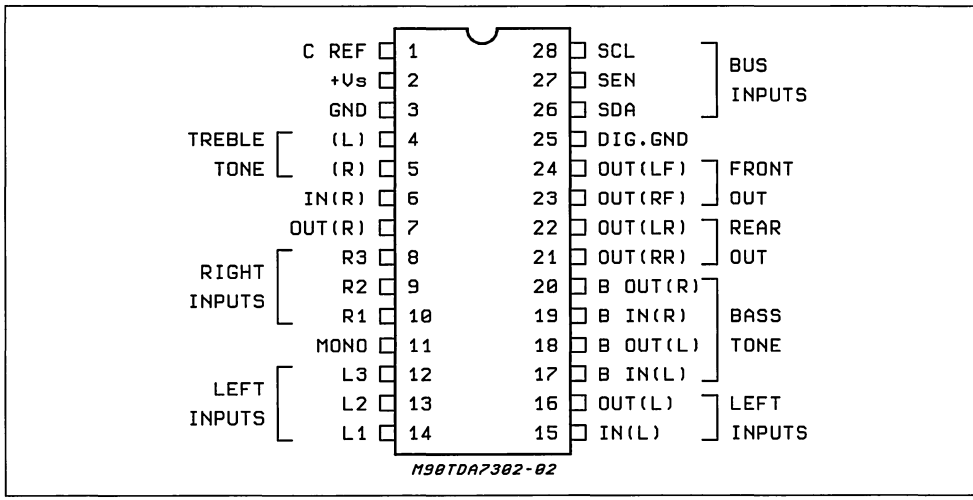
The TDA7302 is a volume, tone (bass and treble), balance (left/right) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi system.

Control is accomplished by serial bus microprocessor interface.
The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.
The results are: low noise, low distortion and high dynamic range.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	14	V
P_{tot}	Total Power Dissipation T_{amb} = 25°C	2	W
T_{amb}	Operating Ambient Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	65	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 10V, R_L = 10kΩ, R_g = 600Ω , f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	10	14	V
I_S	Supply Current		15	30	40	mA
SVR	Ripple Rejection	f = 300Hz to 10KHz	50	58		dB
INPUT SELECTORS						
R_I	Input Resistance		30	45		KΩ
$V_{IN\ max}$	Max. Input Signal	GV = 0dB d = 0.3%	1.5	2.2		Vrms
IN_S	Input Separation	f = 1KHz (2)	90	100		dB
		f = 10KHz (2)	70	80		dB
R_L	Output Load Resistance		5			KΩ
$V_{I\ (DC)}$	Input DC Voltage		3.5	4.3	5	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOLUME CONTROLS						
R_{IN}	Input Resistance		5	10	20	KΩ
	Control Range			78		mA
G_{max}	Max Gain		8	10	12	dB
	Max Attenuation		64	68		dB
	Step Resolution			2	3	dB
	Attenuator Set Error	G_V = -50 to 10dB			2	dB
	Tracking Error				2	dB
SPEAKER ATTENUATORS						
	Control Range		35	38	41	dB
	Step Resolution			2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB
BASS AND TREBLE CONTROL (1)						
	Control Range			±15		dB
	Step Resolution			2.5	3.5	dB
AUDIO OUTPUT						
V_O	Max. Output Voltage	d = 0.3%	1.5	2.2		Vrms
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				1	nF
R_O	Output Resistance			70	150	Ω
V_O(DC)	DC Voltage Level		3	3.8	4.5	V
GENERAL						
e_{NO}	Output Noise	BW = 22Hz to 22KHz, G_v = 0dB		6	15	μV
		BW = 22Hz to 22KHz, Out atten. ≥ 20dB		3.5		μV
		G_v = 0dB Curve A		4		μV
S/N	Signal to Noise Ratio	All gain = 0dB V_O = 1Vrms BW = 22Hz to 22KHz		105		dB
d	Distortion	f = 1KHz V_O = 1V G_v = 0		0.01	0.1	%
	Frequency Response (-1dB)	G_v = 0 High	20			KHz
		G_v = 0 Low			20	Hz
S_C	Channnel Separation left/right	f = 1KHz	90	100		dB
		f = 10KHz	70	80		dB
BUS INPUTS						
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.4			V
V_O	Output Voltage SDA Acknowledge	I = 1.6mA			0.4	V
	Digital Input Current		-5		+5	μA

Notes:
(1) Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.
(2) The selected input is grounded thru the 2.2μF capacitor.

Figure 1: Application Circuit

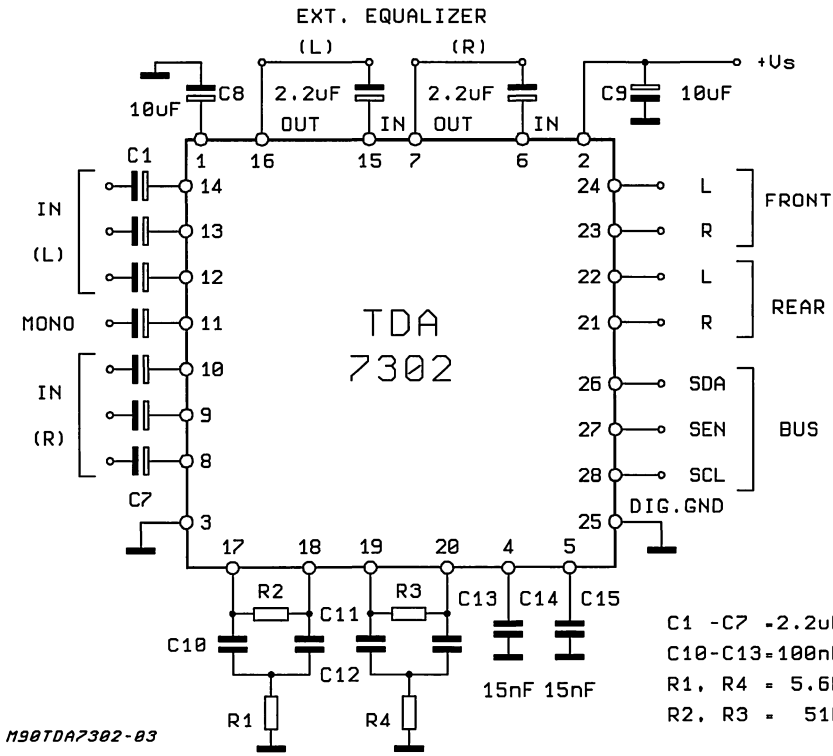


Figure 2: P.C. Board and Components Layout of the Fig.1 (1:1 scale)

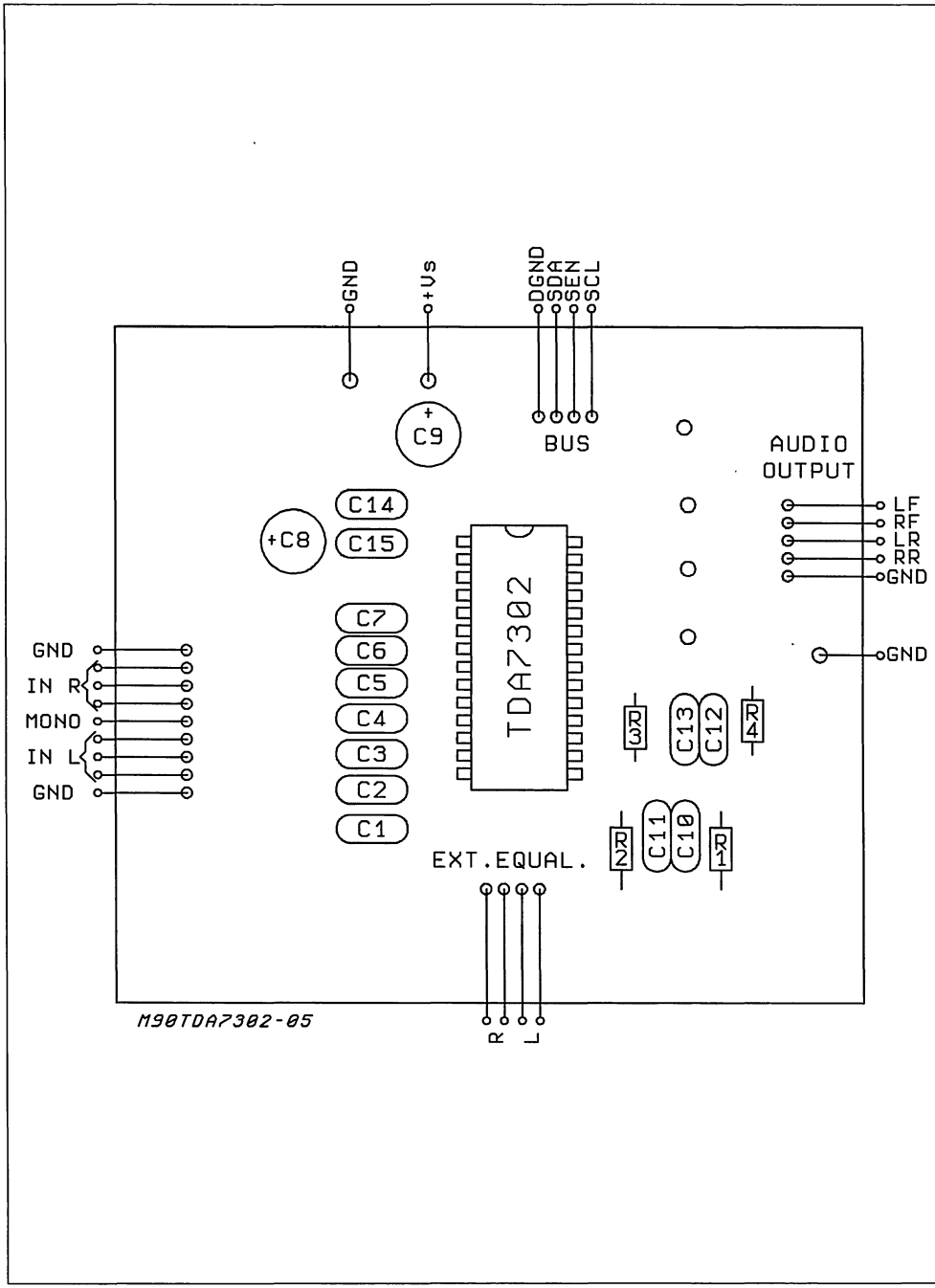


Figure 3: Total Output Noise vs. Volume Setting

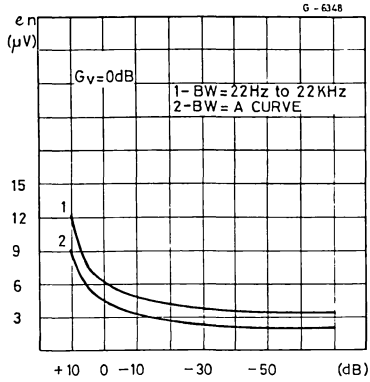


Figure 4: Signal to Noise Ratio vs. Volume Setting

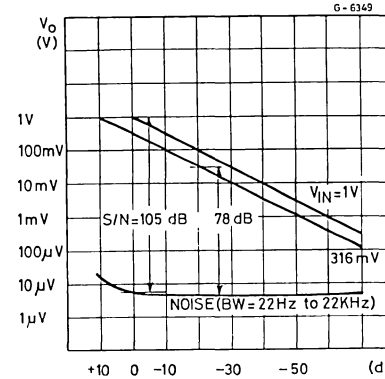


Figure 5: Distortion + Noise vs. Frequency

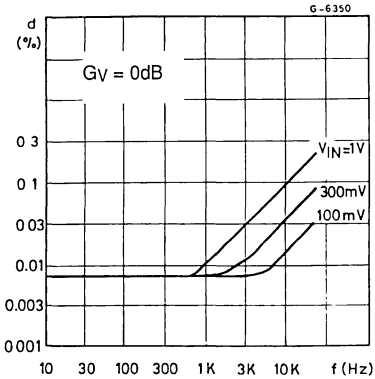


Figure 6: Distortion vs. Output Voltage

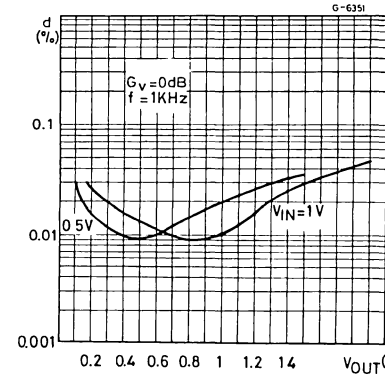


Figure 7: Distortion vs. Load Resistance

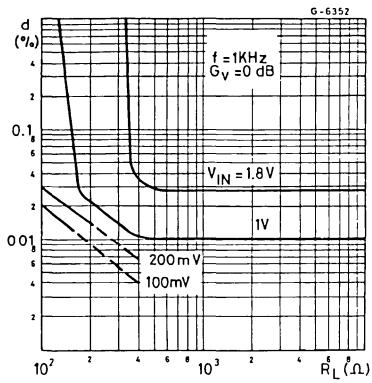


Figure 8: Channel Separation (L1 - R1) vs. Frequency

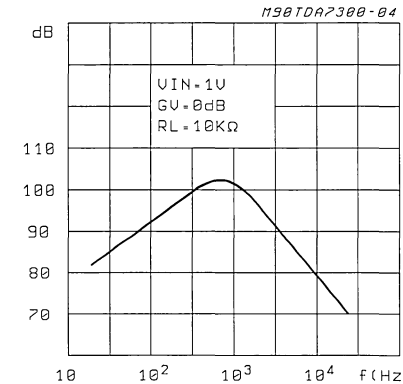


Figure 9: Input Separation (L1 - L2) vs. Frequency

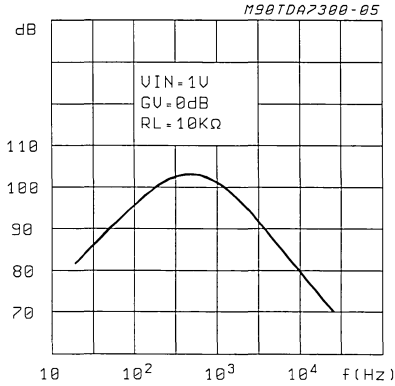


Figure 10: Supply Voltage Rejection vs. Frequency

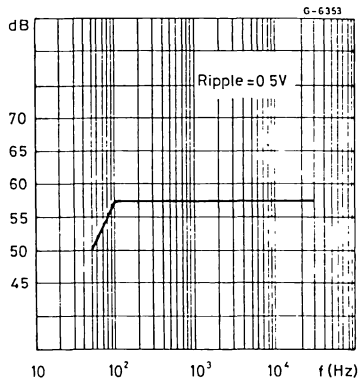
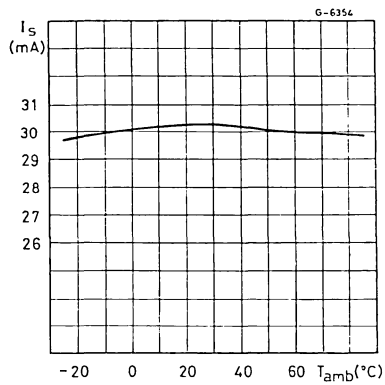


Figure 11: Quiescent Current vs. Temperature



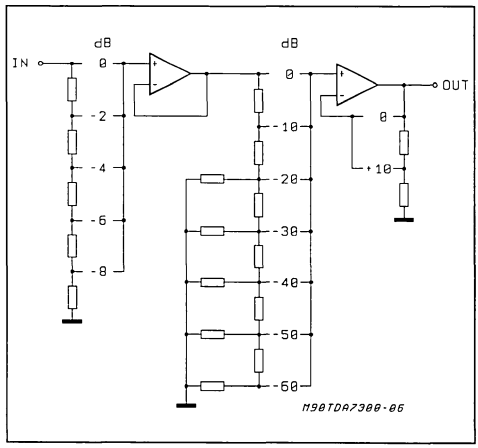
APPLICATION INFORMATION

Volume Control Concept

Traditional electronic volume control circuits use a multiplier technique with all the disadvantages of high noise and distortion.

The used concept, as shown in Fig. 12 with digital switched resistor dividers, provides extremely low noise and distortion. The multiplexing of the resistive dividers is realized with a multiple-input operational amplifier.

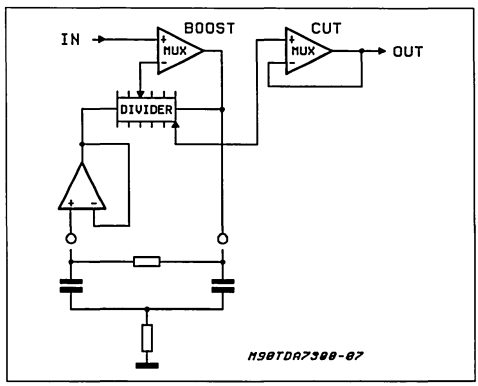
Figure 12: Volume Control



Bass and Treble Control

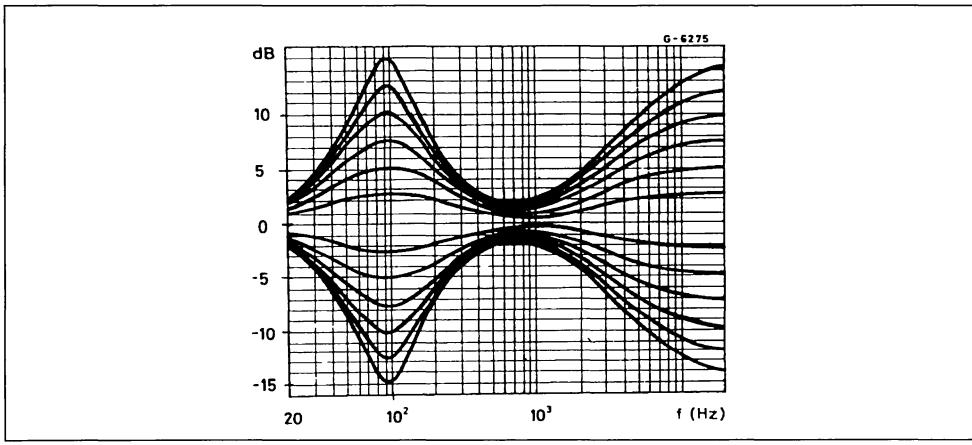
The principle operation of the bass control is shown in Fig. 12. The external filter together with the internal buffer allows a flexible filter design according to the different requirements in car radios. The function of the treble is similar to the bass. A typical curve is shown in Fig.14.

Figure 13: Bass Control



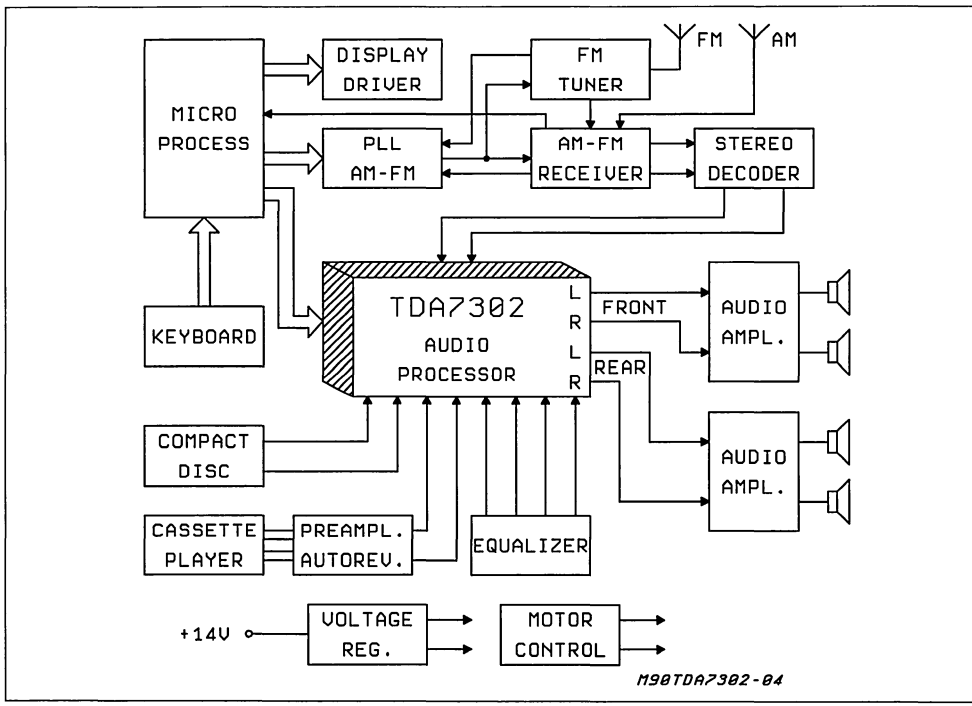
APPLICATION INFORMATION (continued)

Figure 14: Typical Tone Response



Outputs
A special class-A output amplifier with a modulated sink current provides low distortion and ground compatibility with low current consumption.

Figure 15: Complete Car-Radio System using Digital Controlled Audio Processor



APPLICATION INFORMATION (continued)

SERIAL BUS INTERFACE

S-BUS Interface and I²CBUS Compatibility

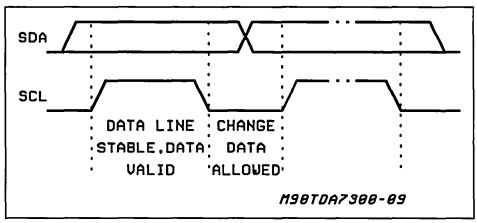
Data transmission from microprocessor to the TDA7302 and viceversa takes place thru the 3-wire S-BUS interface, consisting of the three lines SDA, SCL, SEN. If SDA and SEN inputs are short-circuited together, then the TDA7302 appears as a standard I²CBUS slave.

According to I²CBUS specification the S-BUS lines are connected to a positive supply voltage via pull-up resistors

Data Validity

As shown in fig. 16, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Figure 16: Data Validity on the I²CBUS



Start and Stop Conditions

I²CBUS:
as shown in fig.17 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

S-bus:
the start/stop conditions (points 1 and 6) are detected exclusively by a transition of the SEN line (1 → 0 / 0 →1) while the SCL line is at the HIGH level.

The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). After the start information (point 1) the SEN line returns to the HIGH level and remains unchanged for all the time the transmission is performed.

Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 18). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Figure 17: Timing Diagram of S-BUS and I²CBUS

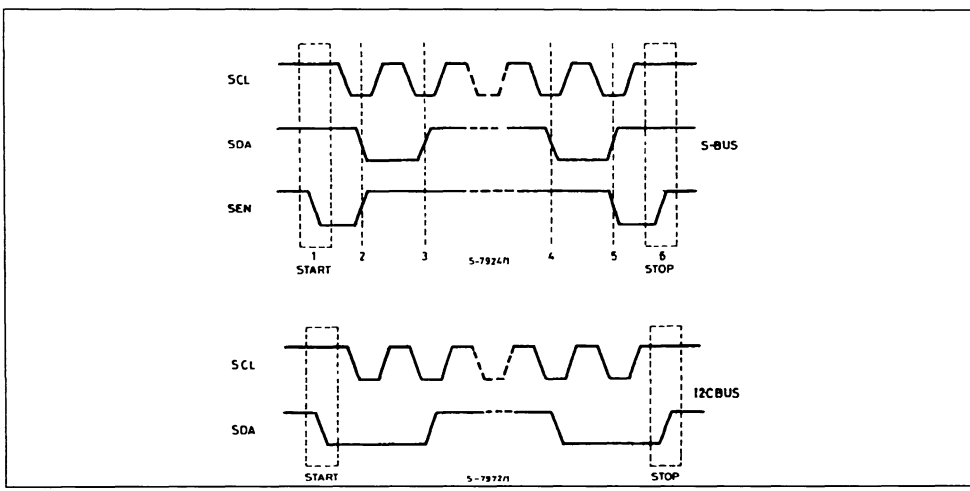
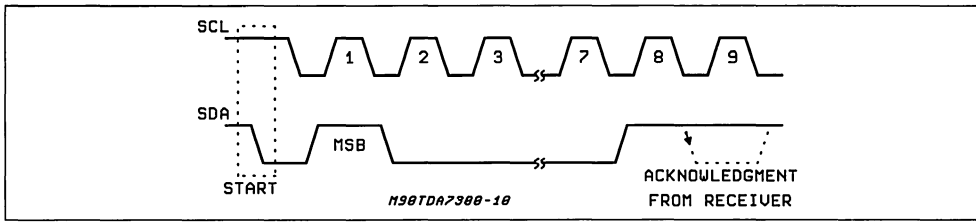


Figure 18: Acknowledge on the I^2CBUS



Transmission without Acknowledge

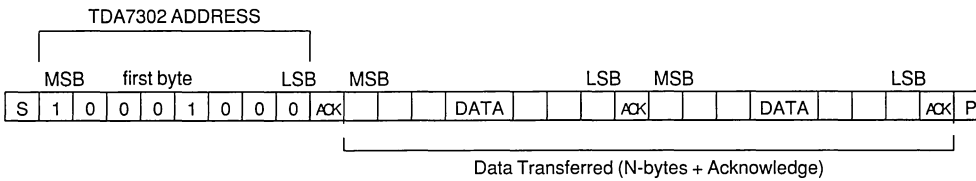
Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7302 address (the 8th bit of the byte must be 0). The TDA7302 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address (TDA7302 address)

1	0	0	0	1	0	0	0
MSB							LSB

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	X	X	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

X = don't care
Ax = 2dB steps
Bx = 10dB steps
Cx = 2.5dB steps

Status after power-on reset

STATUS AFTER POWER-ON-RESET

Volume	– 68 dB
Speaker	– 38 dB
Audio Switch	Mono
Bass	+ 2.5 dB
Treble	+ 2.5 dB

SOFTWARE SPECIFICATION (continued)
DATA BYTES (detailed description)

VOLUME

MSB							LSB	
0	0	B2	B1	B0	A2	A1	A0	Volume 2dB Steps
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
0	0	B2	B1	B0				Volume 10dB STEPS
		0	0	0				+10
		0	0	1				0
		0	1	0				-10
		0	1	1				-20
		1	0	0				-30
		1	0	1				-40
		1	1	0				-50
		1	1	1				-60

For example if you want setting the volume at -32dB the 8 bit string is: 0 0 1 0 0 0 0 1

SPEAKER ATTENUATORS

MSB							LSB	
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30

For example attenuation of 24dB on speaker RF is given by: 1 0 1 1 0 0 1 0

SOFTWARE SPECIFICATION (continued)

AUDIO SWITCH - Select the input Channel to Activate

MSB							LSB	
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Mute Input
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care

For example to set the stereo 2 channel the 8 bit string must be: 0 1 0 0 0 0 0 1

BASS AND TREBLE - Control Range of ± 15 dB (boost and cut) Steps of 2.5 dB

0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	– 15
				0	0	0	1	– 15
				0	0	1	0	– 12.5
				0	0	1	1	– 10
				0	1	0	0	– 7.5
				0	1	0	1	– 5
				0	1	1	0	– 2.5
				0	1	1	1	– 0
				1	1	1	1	+ 0
				1	1	1	0	+ 2.5
				1	1	0	1	+ 5
				1	1	0	0	+ 7.5
				1	0	1	1	+ 10
				1	0	1	0	+ 12.5
				1	0	0	1	+ 15
				1	0	0	0	+ 15

C3 = Sign

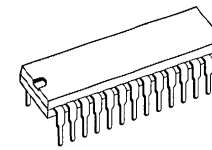
For example Bass at -12.5dB is obtained by the following 8 bit string: 0 1 1 0 0 0 1 0

Purchase of I²C Components of SGS-THOMSON Microelectronics, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

ADVANCE DATA

- CONTROL IS ACCOMPLISHED BY MICROWIRE/SPI - COMPATIBLE SERIAL BUS INTERFACE
- INPUT AND OUTPUT PINS FOR EXTERNAL EQUALIZER
- THREE STEREO INPUT SOURCE SELECTION PLUS MONO INPUT
- TREBLE, BASS, VOLUME AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (FRONT/REAR)
- SINGLE SUPPLY OPERATION
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING



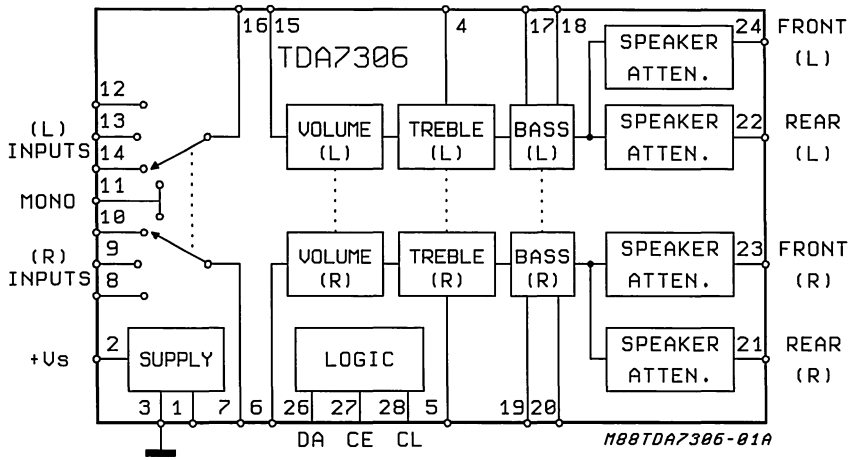
DIP28

ORDERING NUMBER: TDA7306

DESCRIPTION

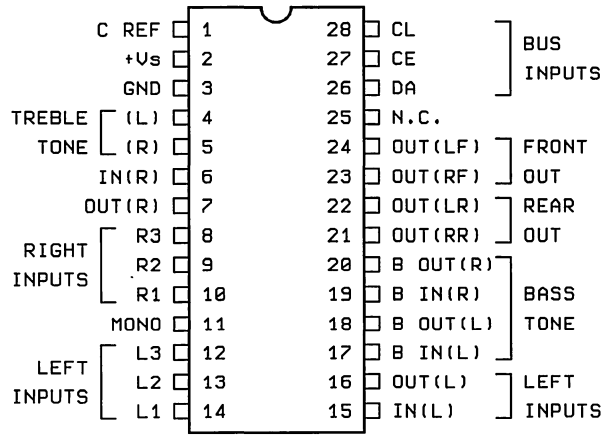
The TDA7306 is a volume, tone (bass and treble), balance (left/right) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi systems.
The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.
The results are: low noise, low distortion and high dynamic range.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice notice

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	14	V
P_{tot}	Total Power Dissipation (T_{amb} = 25°C)	2	W
T_{amb}	Operating Ambient Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	65	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 10V , R_L = 10KΩ; R_g = 600Ω , f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	10	14	V
I_S	Supply Current		15	30	40	mA
SVR	Ripple Rejection	f = 300Hz to 10KHz	50	60		dB
INPUT SELECTORS						
R_I	Input Resistance		30	45		KΩ
V_I(DC)	Input DC Voltage		3.5	4.3	5	V
$V_{IN\ MAX}$	Max. Input Signal	GV = 0dB d = 0.3%	1.5	2.0		Vrms
IN_S	Input Separation	f = 1KHz (2)	90	100		dB
		f = 10KHz (2)	70	80		dB
R_L	Output Load Resistance		5			KΩ

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOLUME CONTROLS						
R_{IN}	Input Resistance		10	18	26	KΩ
	Control Range			78		dB
G_{max}	Max Gain		8	10	12	dB
	Max Attenuation		48	52.4		dB
	Step Resolution			1.6	2.5	dB
	Attenuator Set Error	G_V = -50 to 10dB			2	dB
	Tracking Error				2	dB
SPEAKER ATTENUATORS						
	Control Range		38	41	44	dB
	Step Resolution	see Note (3)				
	Attenuator Set Error				3	dB
	Tracking Error				2	dB
BASS AND TREBLE CONTROL (1)						
	Control Range			±15		dB
	Step Resolution			2.5	3.5	dB
AUDIO OUTPUT						
V_O	Max. Output Voltage	d = 0.3%	1.5	2.2		Vrms
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				1	nF
R_O	Output Resistance			70	150	Ω
V_O(DC)	DC Voltage Level		3	3.8	4.5	V
GENERAL						
e_{NO}	Output Noise	BW = 22Hz to 22KHz, G_V = 0dB		6	15	μV
		BW = 22Hz to 22KHz, Out atten. ≥ 20dB		3.5		μV
		G_v = 0dB Curve A		4		μV
S/N	Signal to Noise Ratio	All gain = 0dB V_O = 1Vrms BW = 22Hz to 22KHz		105		dB
d	Distortion	f = 1KHz; V_O = 1V; G_v = 0		0.01	0.1	%
	Frequency Response (-1dB)	G_v = 0 High	20			KHz
		G_v = 0 Low			20	Hz
S_C	Channnel Separation left/right	f = 1KHz	90	100		dB
		f = 10KHz	70	80		dB
BUS INPUTS						
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.4			V
	Digital Input Current		-5		+5	μA

Notes:
(1) Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.
(2) The selected input is grounded thru the 2.2μF capacitor.
(3) See speaker attenuators table on "Software specification".

Figure 1: Application Circuit

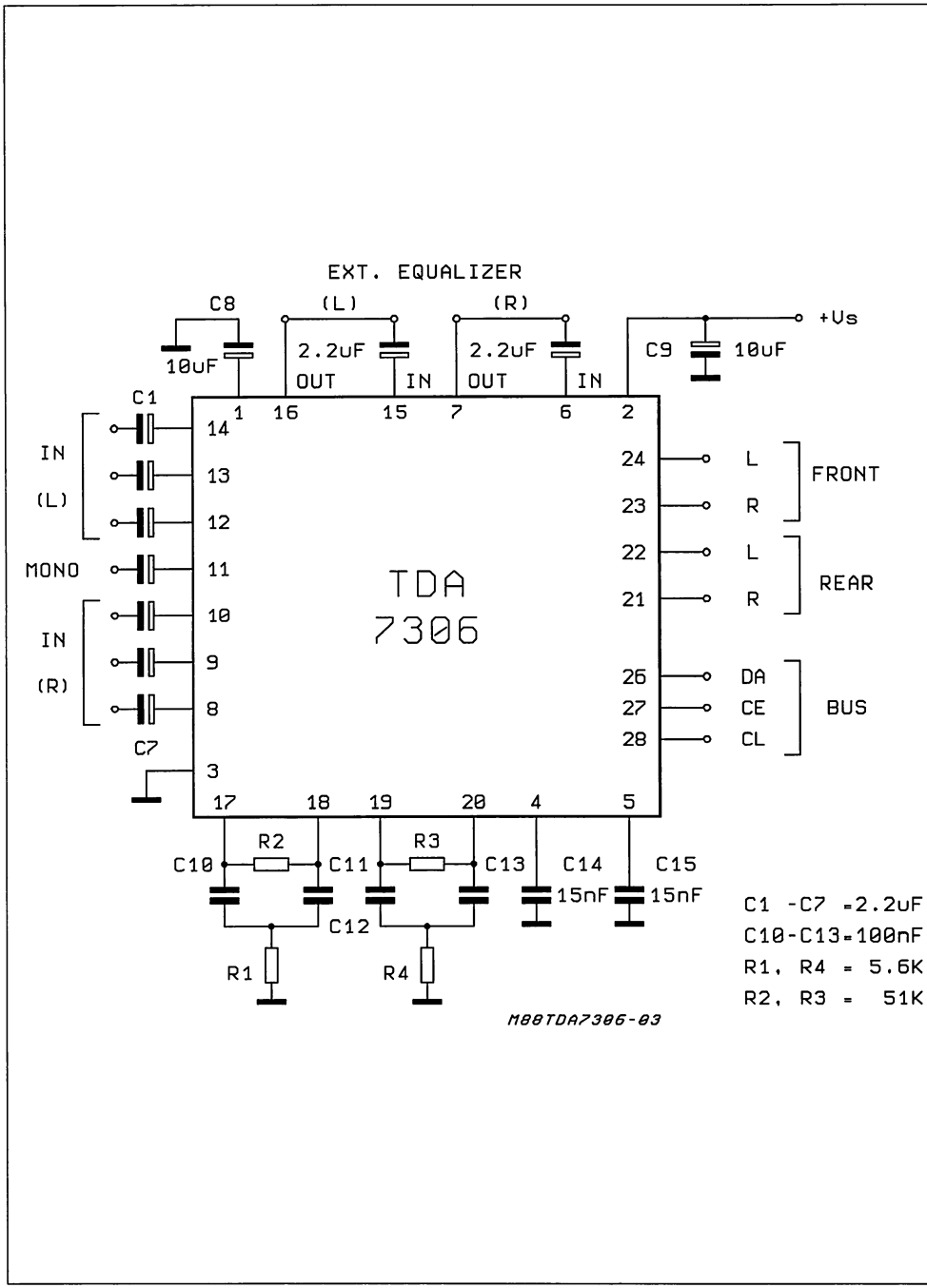


Figure 2: P.C. Board and Components Layout of the Fig.1 (1:1 scale)

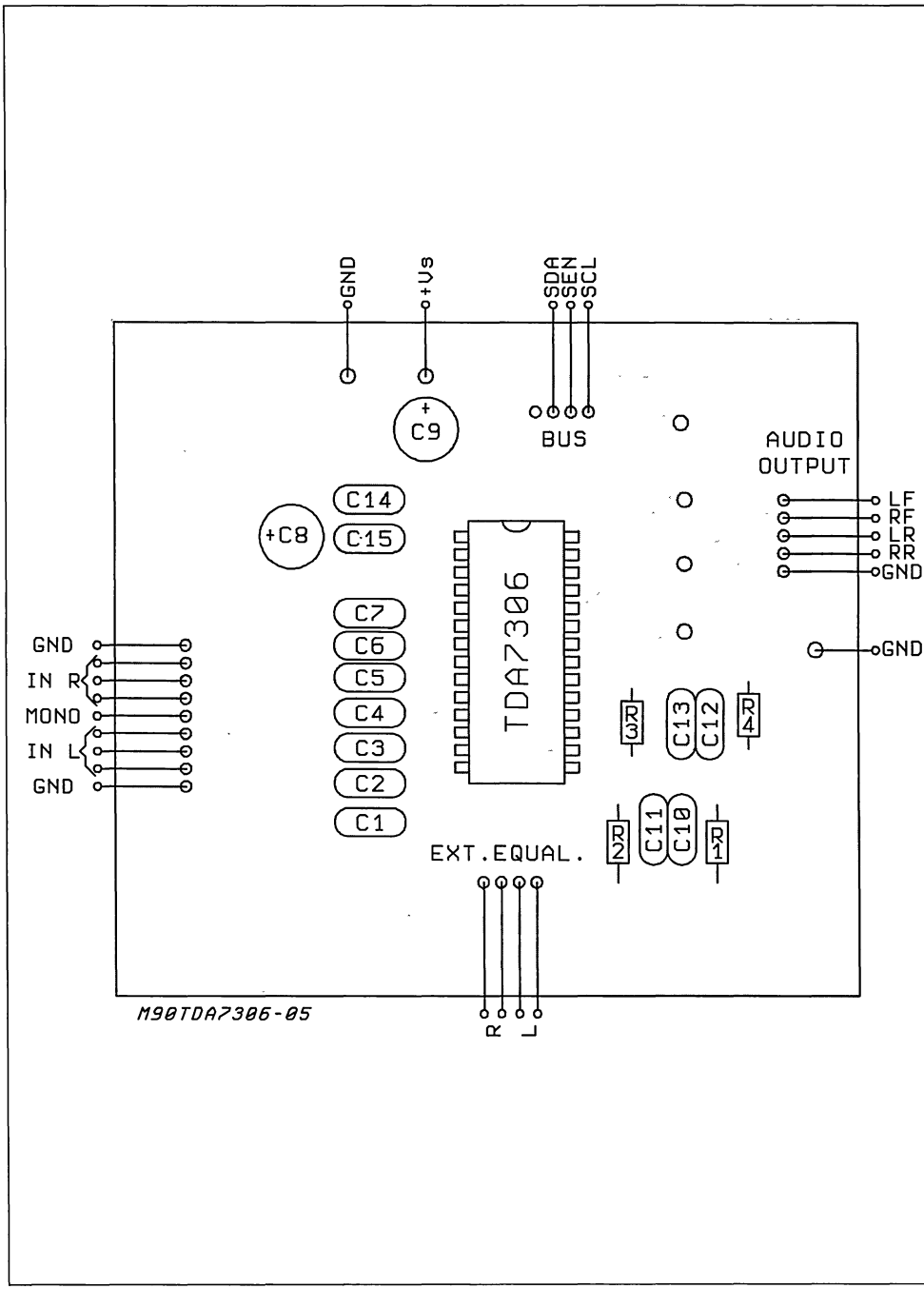


Figure 3: Total Output Noise vs. Volume Setting

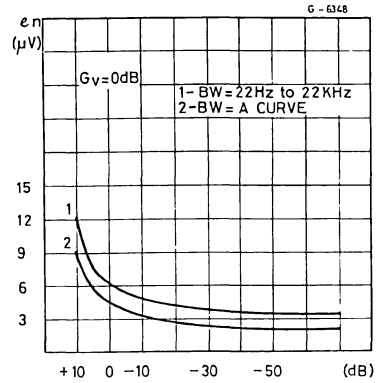


Figure 4: Signal to Noise Ratio vs. Volume Setting

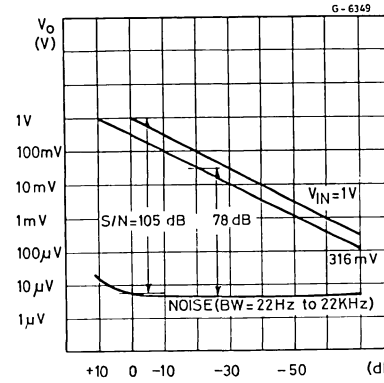


Figure 5: Distortion + Noise vs. Frequency

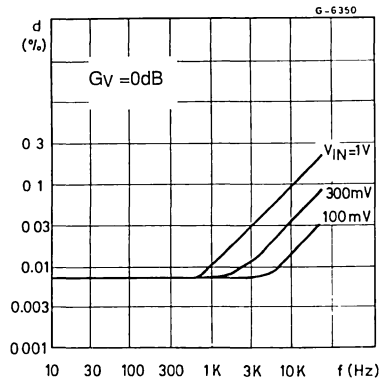


Figure 6: Distortion vs. Output Voltage

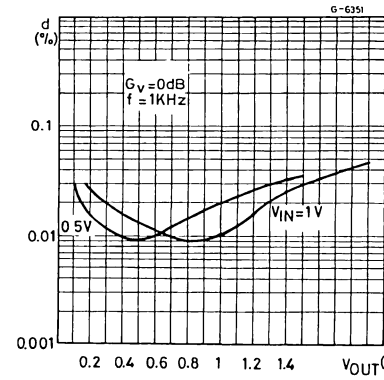


Figure 7: Distortion vs. Load Resistance

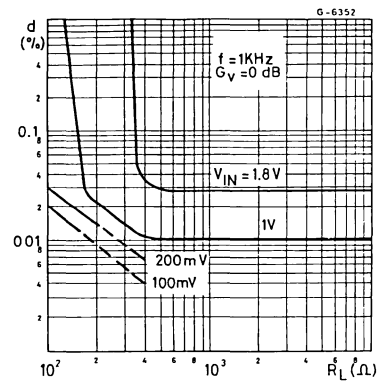


Figure 8: Channel Separation (L1 - R1) vs. Frequency

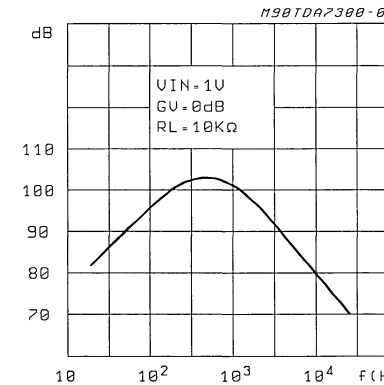


Figure 9: Input Separation (L1 - L2) vs. Frequency

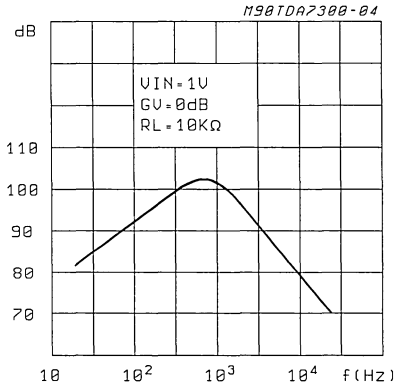


Figure 10: Supply Voltage Rejection vs. Frequency

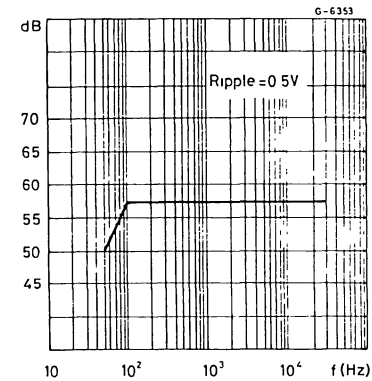
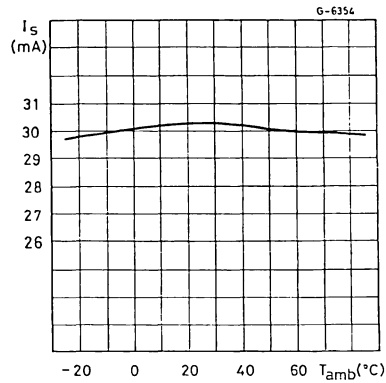


Figure 11: Quiescent Current vs. Temperature

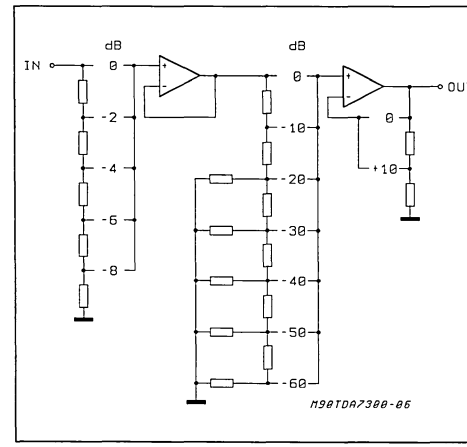


APPLICATION INFORMATION

Volume Control Concept

Traditional electronic volume control circuits use a multiplier technique with all the disadvantages of high noise and distortion.
The used concept, as shown in Fig. 12 with digital switched resistor dividers, provides extremely low noise and distortion. The multiplexing of the resistive dividers is realized with a multiple-input operational amplifier.

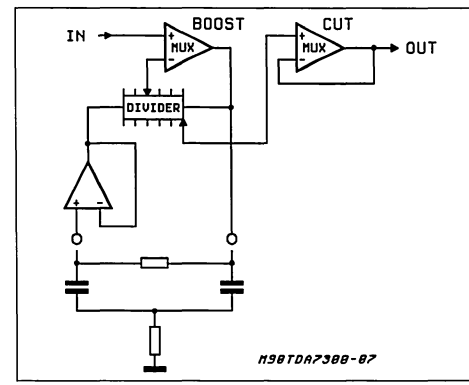
Figure 12: Volume Control



Bass and Treble Control

The principle operation of the bass control is shown in Fig. 13. The external filter together with the internal buffer allows a flexible filter design according to the different requirements in car radios. The function of the treble is similar to the bass.
A typical curve is shown in Fig.14.

Figure 13: Bass Control



APPLICATION INFORMATION (continued)

Outputs

A special class-A output amplifier with a modulated sink current provides low distortion and ground compatibility with low current consumption.

Figure 14: Typical Tone Response

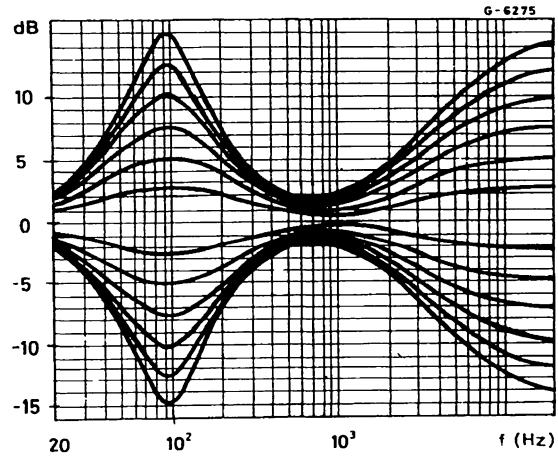
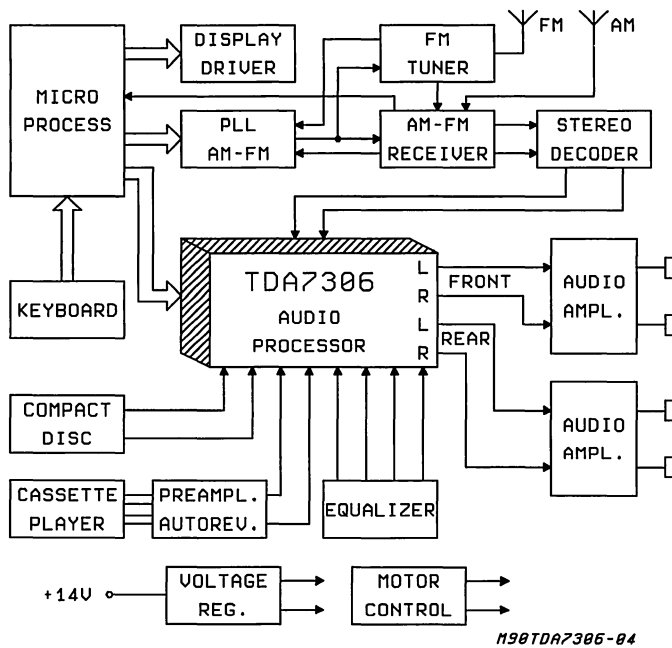


Figure 15: Complete Car-Radio System using Digital Controlled Audio Processor



APPLICATION INFORMATION (continued)

SERIAL BUS INTERFACE

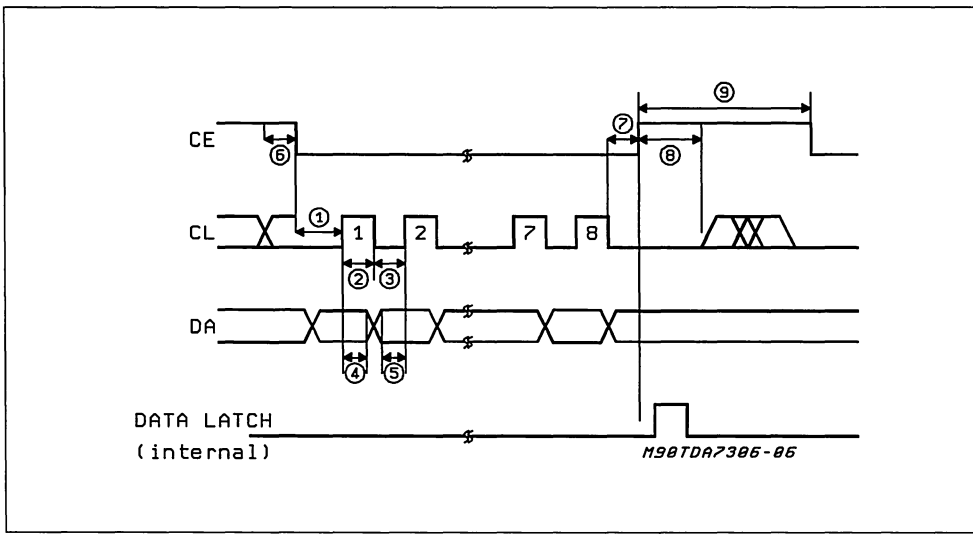
The serial bus interface is compatible to MICRO-WIRE and SPI bus systems.
During the LOW state of the chip enable signal (CE) the data on pin DA are clocked into the shift register at the LOW to HIGH transition of the clock signal CL.

At the LOW to HIGH transition of the CE signal the content of the internal shift register is stored into the addressed latches.

The transmission is separated into bytes with 8 bit according to the data specification of the audio-processor. After every byte a positive slope of the CE signal has to be generated in order to store the data byte.

A special clock counter enables the latch of the data byte only, if exactly 8 clocks were present during the LOW state of the CE signal. This results in a high immunity against spikes on the clock line and avoids a storage of wrong data-bytes.

Figure 16: BUS Timing



Nr.	Parameter	Min.	Max.	Units
	Clock Frequency		250	KHz
1	CE Lead time	4		µs
2	Clock High Time	2		µs
3	Clock Low Time	2		µs
4	Data Hold Time	1.8		µs
5	Data Setup Time	1.8		µs
6	Clock Setup Time	0		µs
7	CE lagtime	0		µs
8	Clock Hold Time	6		µs
9	CE High TIme	6		µs

SOFTWARE SPECIFICATION

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
0	1	0	X	X	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

X = don't care Ax = 2dB steps Bx = 10dB steps
Cx = 2.5dB steps

STATUS AFTER POWER-ON-RESET

Volume	– 68 dB
Speaker	– 38 dB
Audio Switch	Mono
Bass	+ 2.5 dB
Treble	+ 2.5 dB

VOLUME

MSB							LSB	
0	0	B2	B1	B0	A2	A1	A0	Volume 2dB Steps
					0	0	0	0
					0	0	1	-1.6
					0	1	0	-3.2
					0	1	1	-4.8
					1	0	0	-6.4
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
0	0	B2	B1	B0				Volume 10dB Steps
		0	0	0				+10
		0	0	1				+2
		0	1	0				-8
		0	1	1				-16
		1	0	0				-24
		1	0	1				-32
		1	1	0				-40
		1	1	1				-48

For example if you want setting the volume at -25.6dB the 8 bit string is: 0 0 1 0 0 0 0 1

SPEAKER ATTENUATORS

MSB							LSB	
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-1
					0	1	0	-2
					0	1	1	-4
					1	0	0	-5
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				0
			0	1				-6
			1	0				-18
			1	1				-36

For example attenuation of 20dB on speaker RF is given by: 1 0 1 1 0 0 1 0

SOFTWARE SPECIFICATION (continued)

AUDIO SWITCH - Select the input Channel to Activate

MSB							LSB	
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Mute Input
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care

For example to set the stereo 2 channel the 8 bit string must be: 0 1 0 0 0 0 0 1

BASS AND TREBLE - Control Range of ± 15 dB (boost and cut) Steps of 2.5 dB

0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	− 15
				0	0	0	1	− 15
				0	0	1	0	− 12.5
				0	0	1	1	− 10
				0	1	0	0	− 7.5
				0	1	0	1	− 5
				0	1	1	0	− 2.5
				0	1	1	1	− 0
				1	1	1	1	+ 0
				1	1	1	0	+ 2.5
				1	1	0	1	+ 5
				1	1	0	0	+ 7.5
				1	0	1	1	+ 10
				1	0	1	0	+ 12.5
				1	0	0	1	+ 15
				1	0	0	0	+ 15

C3 = Sign

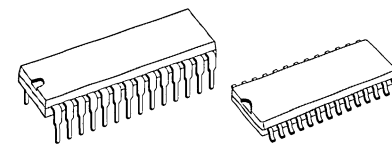
For example Bass at -12.5dB is obtained by the following 8 bit string: 0 1 1 0 0 0 1 0

Purchase of I²C Components of SGS-THOMSON Microelectronics, conveys a licence under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

ADVANCE DATA

- INPUT MULTIPLEXER:
  - 4 STEREO INPUTS
  - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTION TO DIFFERENT SOURCES
- INPUT AND OUTPUT FOR EXTERNAL EQUALIZER OR NOISE REDUCTION SYSTEM
- VOLUME CONTROL IN 1.25dB STEPS
- TREBLE AND BASS CONTROL
- FOUR SPEAKER ATTENUATORS:
  - 4 INDEPENDENT SPEAKERS CONTROL IN 1.25dB STEPS FOR BALANCE AND FADER FACILITIES
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL I^2C BUS



DIP28 **SO28**

ORDERING NUMBERS:
TDA7318 TDA7318D

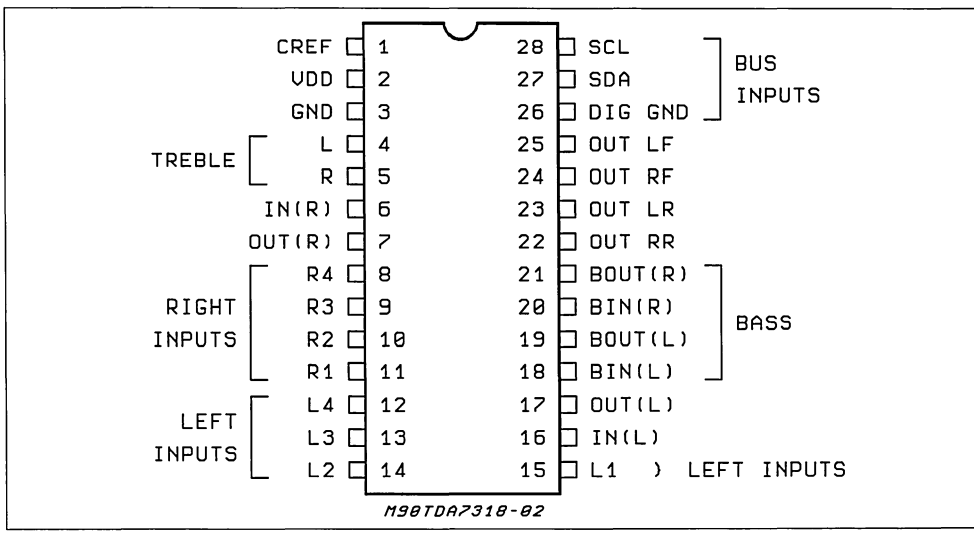
DESCRIPTION

The TDA7318 is a volume, tone (bass and treble) balance (Left/Right) and fader (front/rear) processor for quality audio applications in car radio and Hi-Fi systems.

Selectable input gain is provided. Control is accomplished by serial I^2C bus microprocessor interface. The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

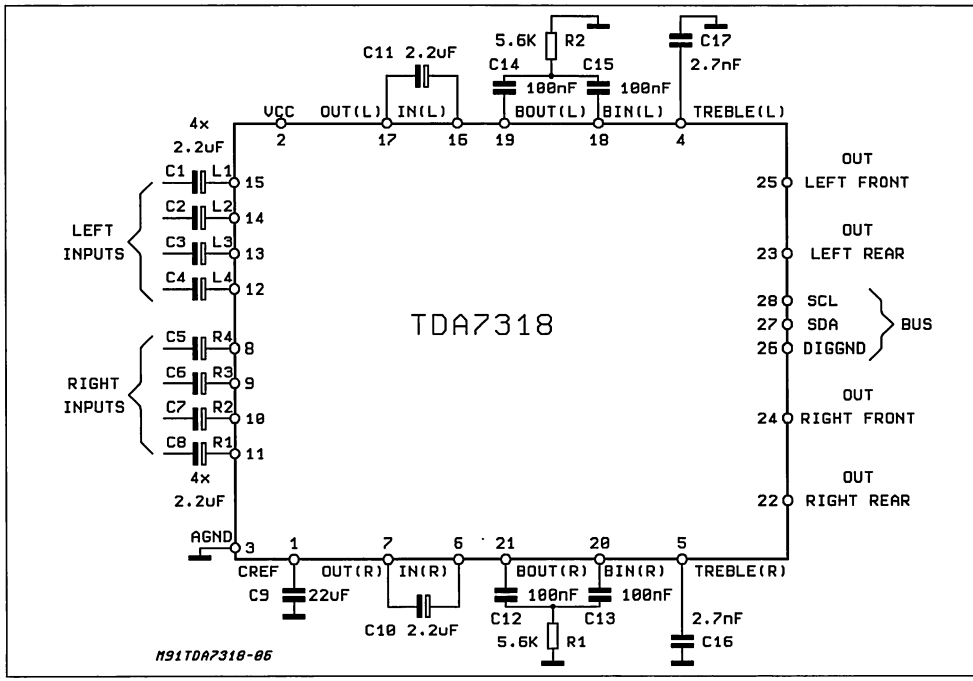
Thanks to the used BIPOLAR/CMOS Tecnology, Low Distortion, Low Noise and Low DC stepping are obtained.

PIN CONNECTION (Top view)



This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

TEST CIRCUIT



THERMAL DATA

Symbol	Description		SO28	DIP28	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	max	85	65	°C/W

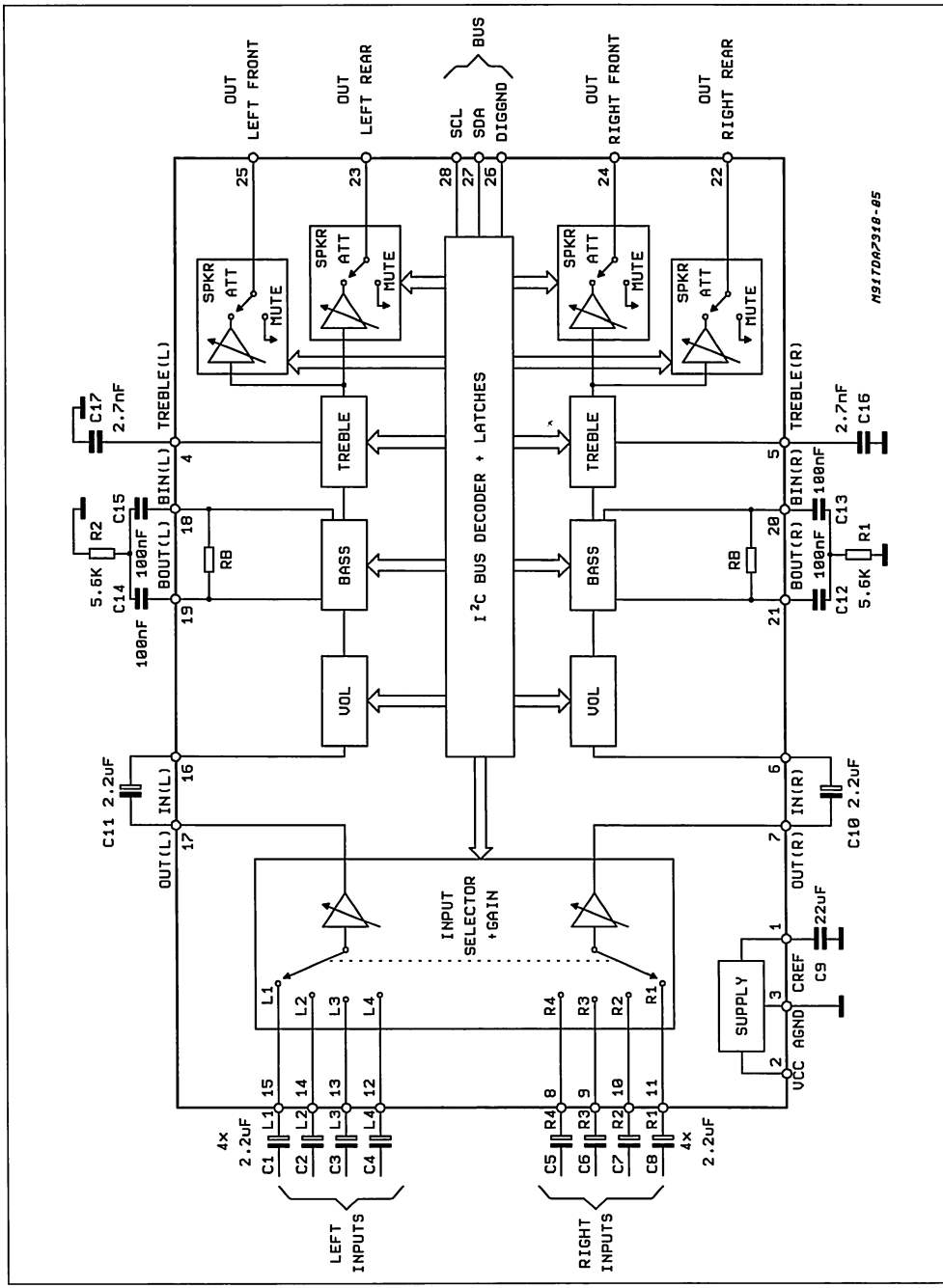
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.2	V
T_{amb}	Operating Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	6	9	10	V
V_{CL}	Max. input signal handling	2			Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio		106		dB
S_C	Channel Separation f = 1KHz		103		dB
	Volume Control 1.25dB step	-78.75		0	dB
	Bass and Treble Control 2db step	-14		+14	dB
	Fader and Balance Control 1.25dB step	-38.75		0	dB
	Input Gain 6.25dB step	0		18.75	dB
	Mute Attenuation		100		dB

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (refer to the test circuit T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, R_G = 600Ω, all controls flat (G = 0), f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	9	10	V
I_S	Supply Current		4	8	11	mA
SVR	Ripple Rejection		60	85		dB
INPUT SELECTORS						
R_{II}	Input Resistance	Input 1, 2, 3, 4	35	50	70	KΩ
V_{CL}	Clipping Level		2	2.5		Vrms
S_{IN}	Input Separation (2)		80	100		dB
R_L	Output Load resistance	pin 7, 17	2			KΩ
G_{INmin}	Min. Input Gain		-1	0	1	dB
G_{INmax}	Max. Input Gain		17	18.75	20	dB
G_{STEP}	Step Resolution		5	6.25	7.5	dB
e_{IN}	Input Noise	G = 18.75dB		2		μV
V_{DC}	DC Steps	adjacent gain steps		4	20	mV
		G = 18.75 to Mute		4		mV
VOLUME CONTROL						
R_{IV}	Input Resistance		20	33	50	kΩ
C_{RANGE}	Control Range		70	75	80	dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation		70	75	80	dB
A_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation Set Error	Av = 0 to -20dB Av = -20 to -60dB	-1.25 -3	0	1.25 2	dB dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	adjacent attenuation steps From 0dB to Av max		0 0.5	3 7.5	mV mV
SPEAKER ATTENUATORS						
C_{range}	Control Range		35	37.5	40	dB
S_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation set error				1.5	dB
A_{MUTE}	Output Mute Attenuation		80	100		dB
V_{DC}	DC Steps	adjacent att. steps from 0 to mute		0 1	3 10	mV mV
BASS CONTROL (1)						
Gb	Control Range	Max. Boost/cut	±12	±14	±16	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		34	44	58	KΩ
TREBLE CONTROL (1)						
Gt	Control Range	Max. Boost/cut	±13	±14	±15	dB
T_{STEP}	Step Resolution		1	2	3	dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
AUDIO OUTPUTS						
V_{OCL}	Clipping Level	d = 0.3%	2	2.5		Vrms
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				10	nF
R_{OUT}	Output resistance		30	75	120	Ω
V_{OUT}	DC Voltage Level		4.2	4.5	4.8	V
GENERAL						
e_{NO}	Output Noise	BW = 20-20KHz, flat output muted all gains = 0dB		 2.5 5	 15	 µV µV
		A curve all gains = 0dB		3		µV
S/N	Signal to Noise Ratio	all gains = 0dB; V_O = 1Vrms		106		dB
d	Distortion	A_V = 0, V_{IN} = 1Vrms A_V = -20dB V_{IN} = 1Vrms V_{IN} = 0.3Vrms		0.01 0.09 0.04	0.1 0.3	% % %
Sc	Channel Separation left/right		80	103		dB
	Total Tracking error	A_V = 0 to -20dB -20 to -60 dB		0 0	1 2	dB dB
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

Notes:

(1) Bass and Treble response see attached diagram (fig.19). The center frequency and quality of the resonance behaviour can be choosen by the external circuitry A standard first order bass response can be realized by a standard feedback network

(2) The selected input is grounded thru the 2 2µF capacitor

Figure 1: Noise vs. Volume/Gain Settings

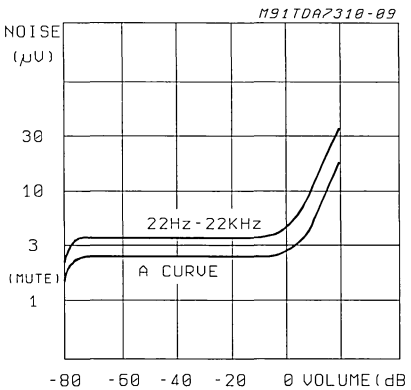


Figure 2: Signal to Noise Ratio vs. Volume Setting

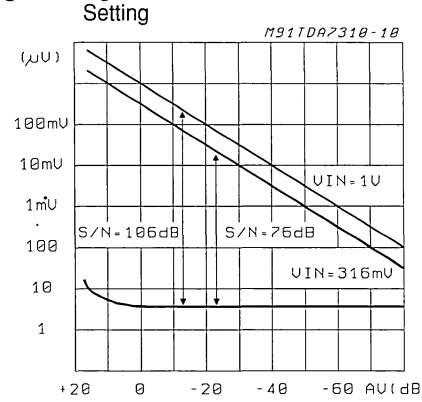


Figure 3: Distortion & Noise vs. Frequency

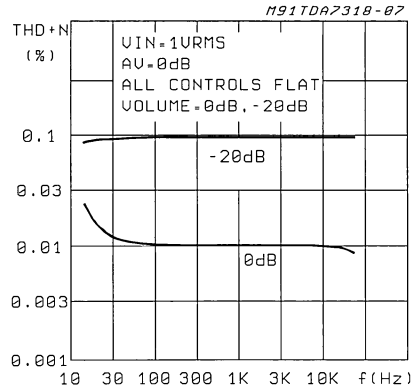


Figure 4: Distortion & Noise vs. Frequency

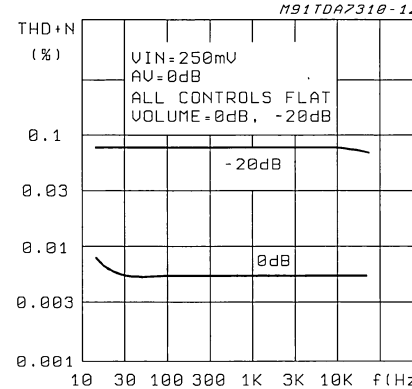


Figure 5: Distortion vs. Load Resistance

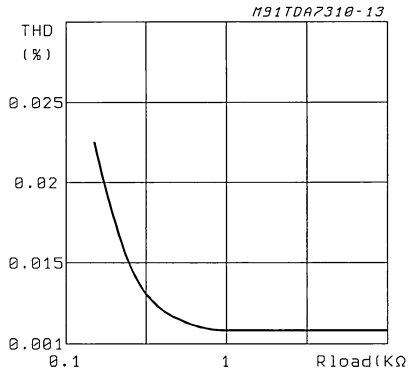


Figure 6: Channel Separation (L → R) vs. Frequency

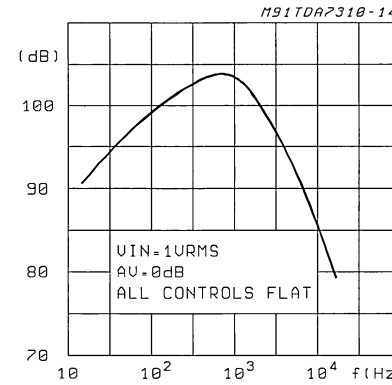


Figure 7: Input Separation (L1 → L2, L3, L4) vs. Frequency

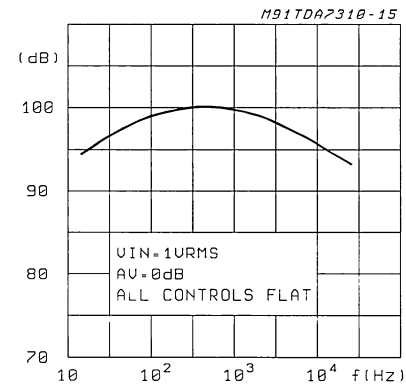


Figure 8: Supply Voltage Rejection vs. Frequency

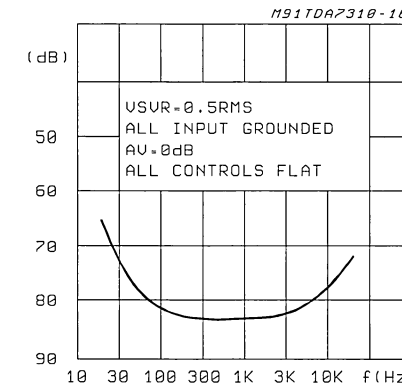


Figure 9: Output Clipping Level vs. Supply Voltage

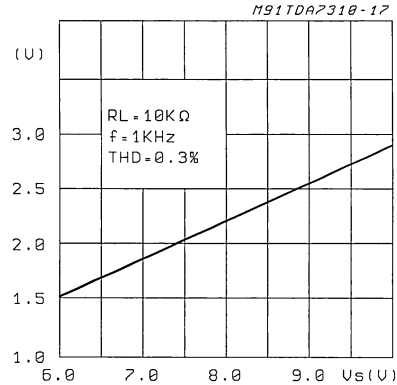


Figure 10: Quiescent Current vs. Supply Voltage

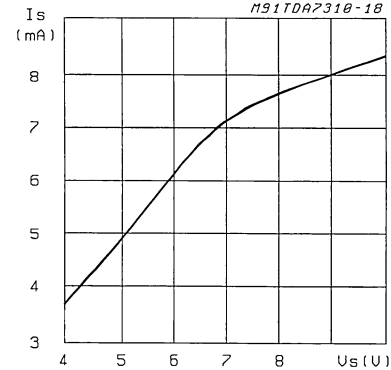


Figure 11: Supply Current vs. Temperature

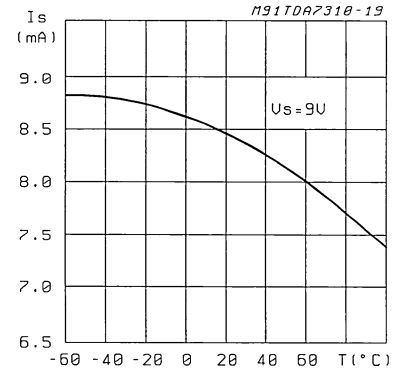


Figure 12: Bass Resistance vs. Temperature

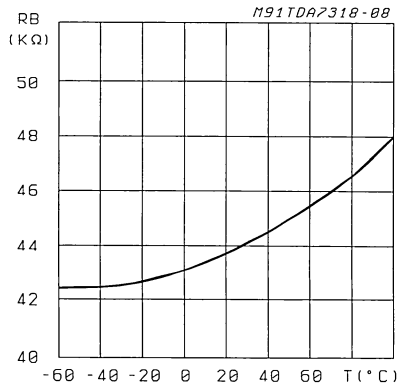
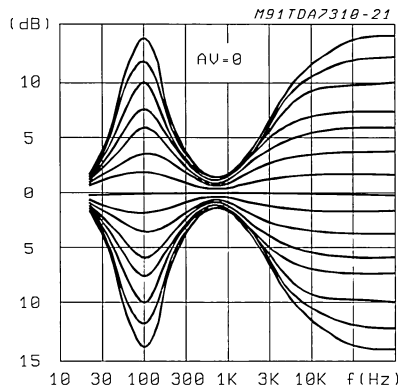


Figure 13: Typical Tone Response (with the ext. components indicated in the test circuit)



I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7318 and viceversa takes place thru the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

Data Validity

As shown in fig. 14, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.15 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 16). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Figure 14: Data Validity on the I²CBUS

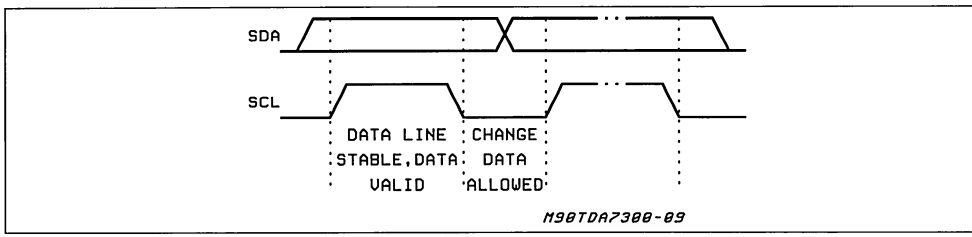


Figure 15: Timing Diagram of I²CBUS

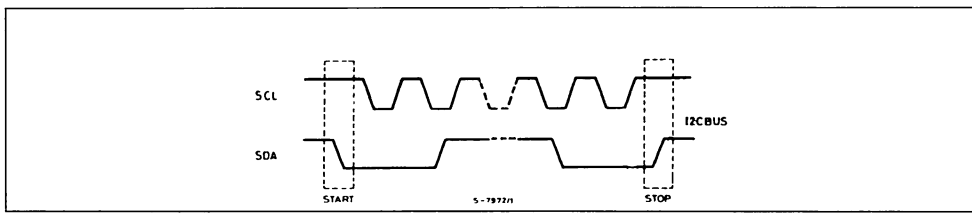
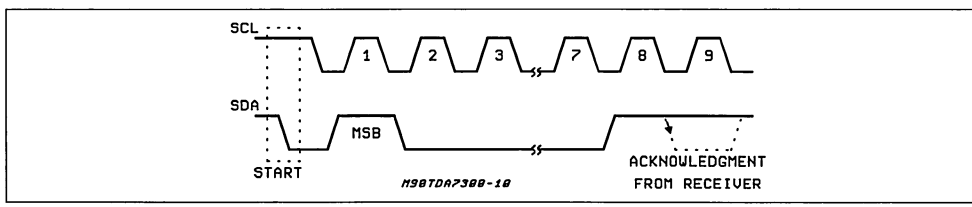


Figure 16: Acknowledge on the I²CBUS

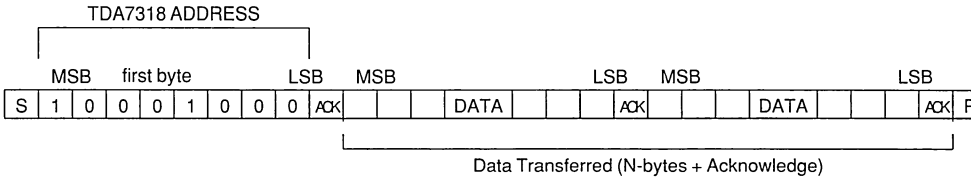


SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7318 address (the 8th bit of the byte must be 0). The TDA7318 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address

1 MSB	0	0	0	1	0	0	0 LSB

DATA BYTES

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	G1	G0	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

Ax = 1.25dB steps; Bx = 10dB steps; Cx = 2dB steps; Gx = 6.25dB steps

SOFTWARE SPECIFICATION (continued)

DATA BYTES (detailed description)

Volume

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

For example a volume of -45dB is given by:

0 0 1 0 0 1 0 0

Speaker Attenuators

MSB							LSB	FUNCTION
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

For example attenuation of 25dB on speaker RF is given by:

1 0 1 1 0 1 0 0

Audio Switch

MSB							LSB	FUNCTION
0	1	0	G1	G0	S2	S1	S0	Audio Switch
					0	0	0	Stereo 1
					0	0	1	Stereo 2
					0	1	0	Stereo 3
					0	1	1	Stereo 4
					1	0	0	Not allowed
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				+18.75dB
			0	1				+12.5dB
			1	0				+6.25dB
			1	1				0dB

For example to select the stereo 2 input with a gain of +12.5dB the 8bit string is:
0 1 0 0 1 0 0 1

Bass and Treble

0 0	1 1	1 1	0 1	C3 C3	C2 C2	C1 C1	C0 C0	Bass Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

C3 = Sign
For example Bass at -10dB is obtained by the following 8 bit string:
0 1 1 0 0 0 1 0

Purchase of I²C Components of SGS-THOMSON Microelectronics, conveys a licence under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

SGS-THOMSON MICROELECTRONICS

TDA8102B

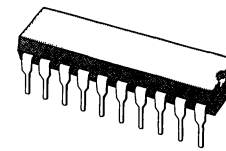
H/V PROCESSOR FOR TTL V.D.U

HORIZONTAL SECTION

- SYNCHRONIZATION INPUT : TTL COMPATIBLE, NEGATIVE EDGE TRIGGERED
- SYNCHRONIZATION INDEPENDENT FROM DUTY CYCLE TIME
- OSCILLATOR : FREQUENCY RANGE FROM 15kHz to 100kHz
- HORIZONTAL OUTPUT PULSE SHAPER AND SHIFTER
- PHASE COMPARATOR BETWEEN SYNCHRO AND OSCILLATOR (PLL1)
- PHASE COMPARATOR BETWEEN FLYBACK AND OSCILLATOR (PLL2)
- INTERNAL VOLTAGE REGULATOR
- DC COMPATIBLE CONTROLS FOR PHASE AND FREQUENCY

VERTICAL SECTION

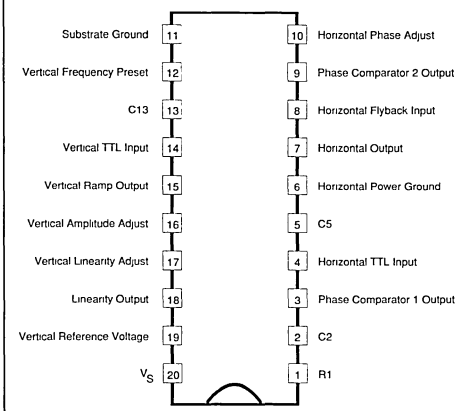
- SYNCHRONIZATION INPUT : TTL COMPATIBLE, NEGATIVE EDGE TRIGGERED
- SYNCHRONIZATION INDEPENDENT FROM DUTY CYCLE TIME
- OSCILLATOR : FREQUENCY RANGE FROM 30Hz to 120Hz
- RAMP GENERATOR WITH VARIABLE GAIN STAGE
- VERTICAL RAMP VOLTAGE REFERENCE
- INTERNAL VOLTAGE REGULATOR
- DC COMPATIBLE CONTROLS FOR FREQUENCY, AMPLITUDE AND LINEARITY



DIP20
(Plastic package)

ORDER CODE: TDA8102B

PIN CONNECTIONS



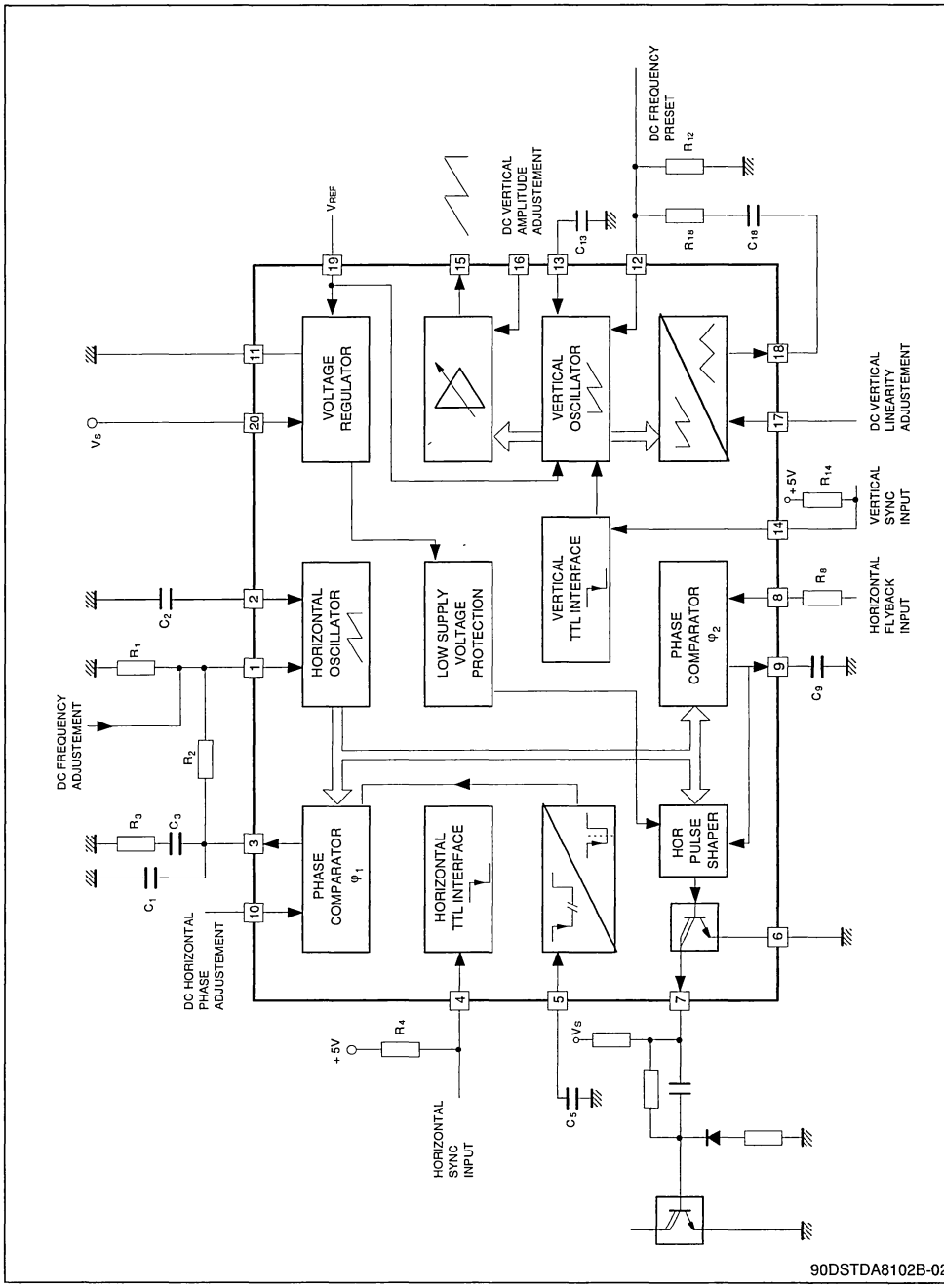
90DSTDA8102B-01

DESCRIPTION

The TDA8102B is a monolithic integrated circuit for horizontal and vertical sync processing in monochrome and color video displays driven by input TTL compatible signals.

The TDA8102B is supplied in a 20 pin dual in line package with pin 11 connected to ground and used for heatsinking.

BLOCK DIAGRAM



90DSTDA8102B-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply voltage	18	V
V_{SYNC}	Sync input peak voltage	+ V_S	V
I_{OH}	Output sinking peak current (Pin 7 ; t < 3µs)	2	A
I_{15}	Output current (Pin 15)	- 10	mA
I_{19}	Output current (Pin 19)	- 10	mA
P_{TOT}	Total power dissipation • T_{amb} < 70°C • T_{pin} < 90°C	 1.4 1.5	 W W
T_{STG} , T_J	Storage and junction temperature	- 40 to 150	°C

THERMAL DATA

$R_{TH(J-C)}$	Junction-case thermal resistance	40	°C/W
$R_{TH(J-A)}$	Junction-ambient thermal resistance	55	°C/W

ELECTRICAL CHARACTERISTICS

(T_{AMB} = 25°C, V_S = 12V, refer to the test circuits, unless otherwise specified)

HORIZONTAL SECTION

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage range		10.5	12	15.5	V
I_S	Supply current			50	70	mA
V_1	Voltage reference at Pin 1	I_1 = 0.5mA	3.2	3.5	3.8	V
I_1	Current at Pin 1		- 1			mA
V_2	Voltage swing at Pin 2			4		V_{PP}
K_0	Free running frequency constant	$f_o = 1/(K_0 \times R1 \times C2)$	2.8	3.04	3.2	
$\lvert V_3 - V_1 \rvert$	Control voltage range	(See technical note 1)		2.5		V
$\lvert I_3 \rvert$	Peak control current			3		mA
K_3	Gain phase comparator ϕ1 $K_3 = 2 \times I_3 / 360$			16.6		µA / degree
V_4	Sync threshold input (neg. edge)	• Sync high • Sync low	2		8 0.8	V V
I_4	Current at Pin 4	• Input high • Input low	 - 10		10	µA µA
T_4	Input pulse duration T = $1/f_H$		1		0.9T	µs
V_5	Monostable threshold		5.7	6	6.3	V
t_5	Internal pulse width $t_5 = C5 \times V_5 / I_5$	C5 = 220 pF (see technical note 2)		3.6		µs
t_7	Output pulse duration (low) - T = $1/f_H$	@ f_H = 27 kHz @ f_H = 100 kHz		0.33T 0.25T		µs µs
V_7 sat	Output Saturation Voltage	I_7 = 600 mA		1.2	2.5	V
t_D	Permissible delay between output pulse leading edge and flyback pulse leading edge (for keeping a constant duty cycle) ; $T = \frac{1}{f_H}$	See technical note 4	0.30 T - t_{FLY}			s
V_{FLY}	Flyback threshold voltage at Pin 8		0.6	0.7	0.9	V
I_{FLY}	Flyback input current at Pin 8	• Flyback On • Flyback Off	0.6 -1		2	mA mA
V_8	Clamp voltage at Pin 8	• I_8 = 1mA • I_8 = - 1mA	0.6		 - 0.6	V V

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, V_S = 12V, refer to the test circuits, unless otherwise specified)

HORIZONTAL SECTION (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_8	Current for switching low the output pulse		0.7		2	mA
$\lvert I_9 \rvert$	Peak control current			1		mA
K_9	Phase sensitivity at Pin 9	(See technical note 3)		67.5		$\frac{\text{degree}}{\text{V}}$
V_{10}	Control voltage range		0.5		4.5	V
K_{10}	Phase control sensitivity at Pin 10		20	22.5	30	$\frac{\text{degree}}{\text{V}}$
	Horizontal phase adjustment	Zero degree phase: flyback centered on the center of the pulse at Pin 5	- 45		+ 45	degree
K_1	Phase jitter constant (jitter = $\frac{K_1}{10^6 \cdot f_H}$)			100	150	ppm
K_2	Frequency drift versus supply voltage : $K_2 = \frac{dF \cdot 10^6}{dV \cdot f_H}$	V_S = 10.5V to 15.5V			2000	$\frac{\text{ppm}}{\text{V}}$

VERTICAL SECTION

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{12}	Voltage reference at Pin 12		3.2	3.5	3.8	V
$\frac{I_{13}}{I_{12}}$	Current gain at Pin 13			1		
V_{13}	Vertical ramp amplitude			4		V_{PP}
t_{FALL}	Discharge time at Pin 13	C_{18} = 0.22 µF V_{13} = 4V_{PP}		10	22	µs
K_{14}	Synchro window constant $t_s = \frac{K_{14}}{f_V}$	(See technical note 6)		0.333		
V_{14}	Sync input threshold (negative edge)	• Sync high • Sync Low	2		8 0.8	V V
I_{14}	Current at Pin 14	• Input high • Input Low	 - 10		10	µA µA
t_{14}	Input pulse duration $T = \frac{1}{f_V}$		10		0.5T	µs
V_{15}	Average value of voltage on Pin 15	V_{13} = 4V_{PP} V_{16} = 2.5V		4		V
$\lvert I_{15} \rvert$	Output current at Pin 15				1	mA
K_{15}	Buffer gain constant at Pin 15 $V_{15PP} = K_{15} \cdot V_{13PP}$	V_{16} = 2.5V		1		
K_{16}	Buffer variable gain constant at Pin 15 : $K_{16} = \frac{\Delta V_{15PP}}{\Delta V_{16} \cdot V_{13PP}}$	2.5V < V_{16} < 4.5V 0.5V < V_{16} < 2.5V		0.1		V^{-1}
I_{16}	Input bias current at Pin 16	V_{16} = 0.5V	- 50			µA
I_{17}	Input bias current at Pin 17	V_{17} = 4.5V			50	µA
V_{18}	Average voltage at Pin 18 : $V_{18} = 2 + \frac{V_{18PP}}{2}$	V_{17} = 3.5V R_{18} not connected		3		V
K_{18}	Linearity correction constant : $K_{18} = \frac{\Delta V_{18PP}}{\Delta V_{17}}$	V_{13PP} = 4V, 1.5V < V_{17} < 4.5V		1		

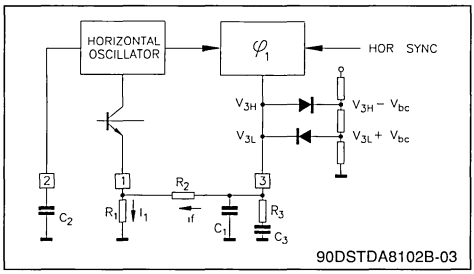
ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, V_S = 12V, refer to the test circuits, unless otherwise specified)

VERTICAL SECTION (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{19}	Voltage reference at Pin 19	(See technical note 5)	7.6	8	8.2	V
$\|I_{19}\|$	Current at Pin 19				2	mA
K_{17}	Frequency drift versus supply voltage $K_{17} = \frac{dF \cdot 10^6}{dV \cdot f_V}$	V_S = 10.5V to 15.5V			4500	$\frac{ppm}{V}$

Technical note 1:



$f_{H\,(nom)}$ = 26.8 kHz
R1 = 6.8k Ω
R2 = 56 kΩ
C2 = 1.8 nF

$$f_{pull\text{-}in} = f_{H\,(nom)} \frac{|V_3 - V_1| / R2}{V_1 / R1} = f_{H\,(nom)} \frac{I_f}{I_o} \qquad (A)$$

where: V_1 = 3.5V and $|V_3 - V_1|$ is the control voltage range.
The voltage at Pin 3 is limited by two clamping diodes at the voltage V_{3H} and V_{3L}
When the PLL1 is synchronized and perfectly tuned, $V_3 = V_1$.

Remark: The value of C2 influences the horizontal oscillator free running frequency; it doesn't effect the pull-in range. If the horizontal frequency is changed by using R1, the pull-in range changes accordingly with the formula (A).

Technical note 2

The internal pulse "t_5", is generated by the current generator "I_5" charging the external capacitor "C5", according with the formula (B):

$$t_5 = \frac{C5 \cdot V_5}{I_5} \qquad (B)$$

$$t_5 = \frac{T_H}{12} \quad \text{is recommended.}$$

Technical note 3:

K_9 = 67.5 degrees/volt represents the slope of the oscillator charging period of the waveform at Pin 2:

$$K_9 = \frac{360 \times 0.75}{4} \quad \frac{\text{degree}}{V}$$

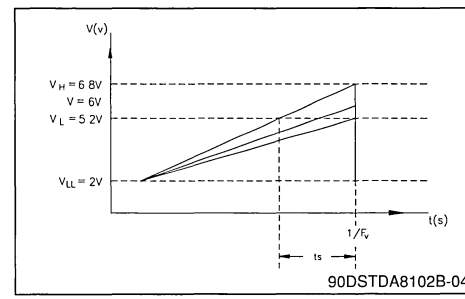
Technical note 4:

The second PLL can recover the storage of horizontal output stage maintaining a constant duty cycle till the trailing edge of the output pulse gets the trailing edge of the flyback pulse. From this point on, only the leading edge of the output pulse will be shifted covering a total phase shift of: 0.30T; overcoming this value, it will produce a notch in the output pulse (@ f_H = 27kHz).

Technical note 5:

The voltage reference at Pin 19 can be used to polarize the DC operating point of the vertical booster. This voltage corresponds to the double of the mean value voltage of the vertical sawtooth at Pin 13.

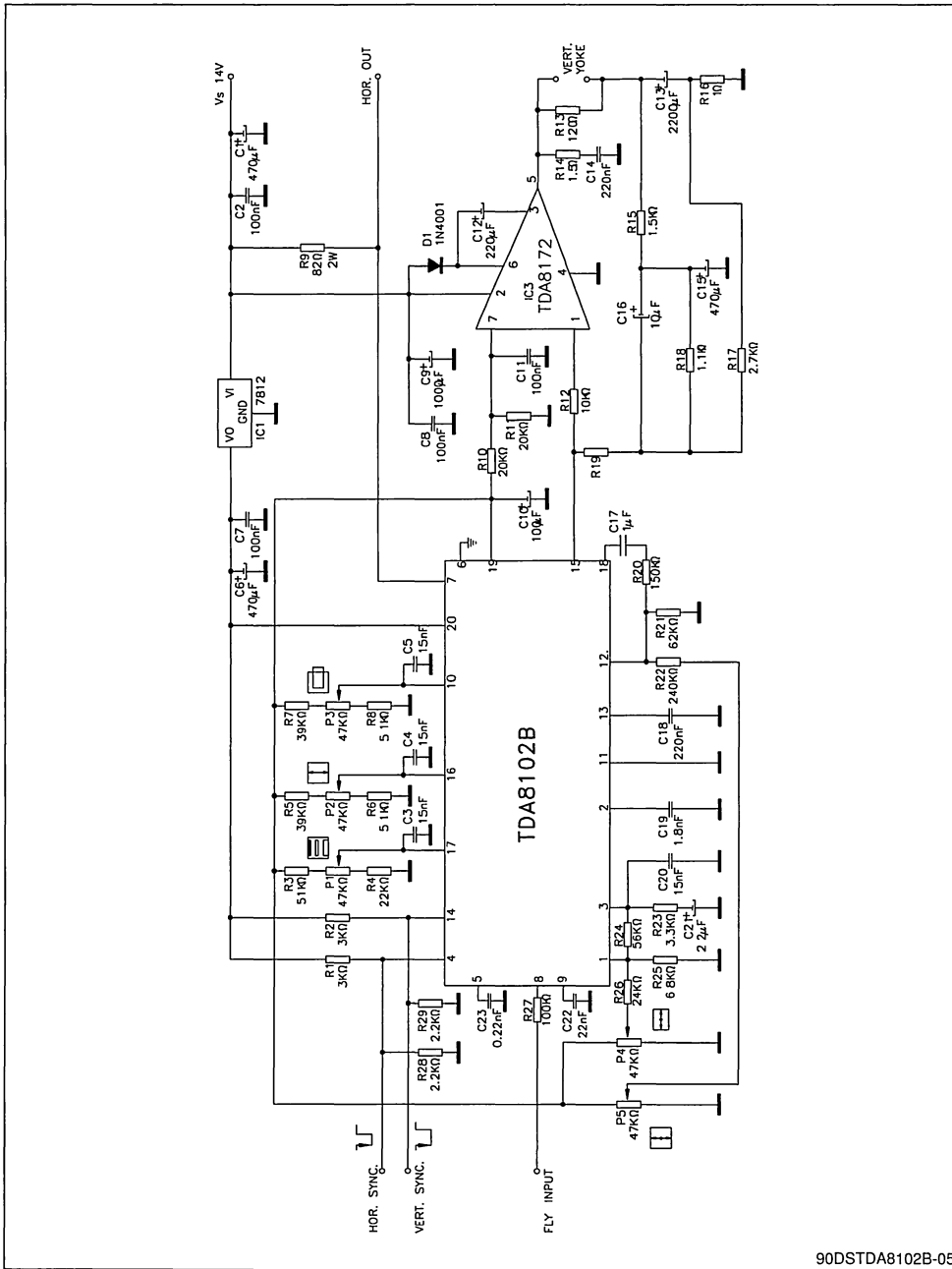
Technical note 6:



$$\frac{V_H - V_L}{t_s} = \frac{V_H - V_{LL}}{1/f_V}$$

$$t_s = \frac{(V_H - V_L)}{(V_H - V_{LL})} \frac{1}{f_V} = \frac{K_{14}}{f_V}$$

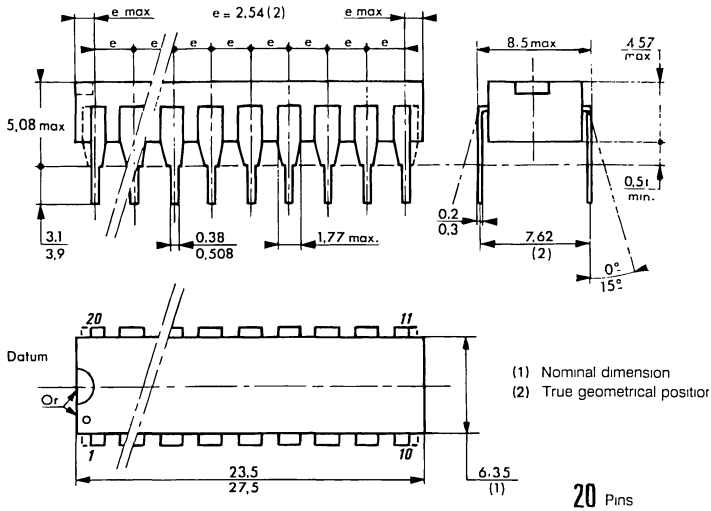
APPLICATION DIAGRAM (with TDA8172)



Note : *The value of R19 depends on CRT. On the mock-up R19 is substituted with a resistance + trimmer for generic applications.

PACKAGE MECHANICAL DATA

20 PINS - PLASTIC DIP

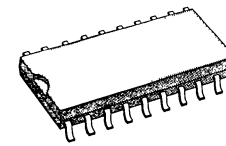


SGS-THOMSON MICROELECTRONICS

TDA8118

CONTROL HEAD PLAYBACK & RECORD AMPLIFIER AND SIGNALS INTERFACE

- CONTROL HEAD PLAYBACK AMPLIFIER WITH AGC
- CONTROL HEAD RECORD AMPLIFIER WITH SINK/SOURCE OUTPUT STAGE
- CONTROL PLAY-BACK SIGNAL INVERTER
- 4 COMPARATORS WITH INTERNAL FIXED THRESHOLD (2.5V)
- COMPARATORS WITH GROUND/V_S COMPATIBLE INPUTS AND OPEN COLLECTOR OUTPUTS



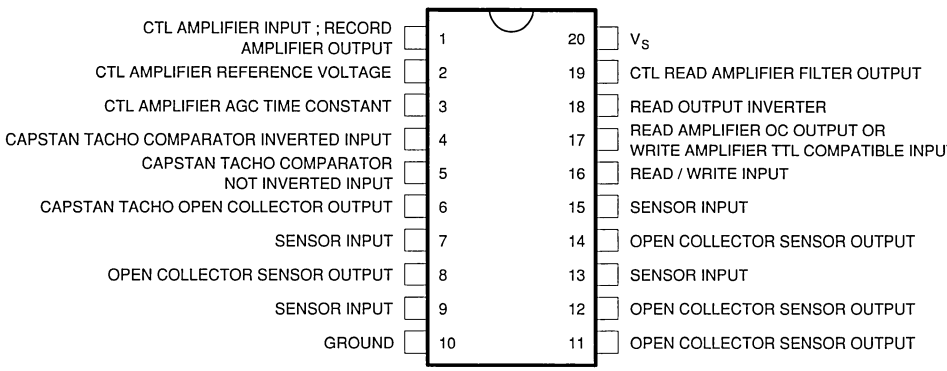
SO20 LARGE
(Plastic Micropackage)

ORDER CODE : TDA8118D

DESCRIPTION

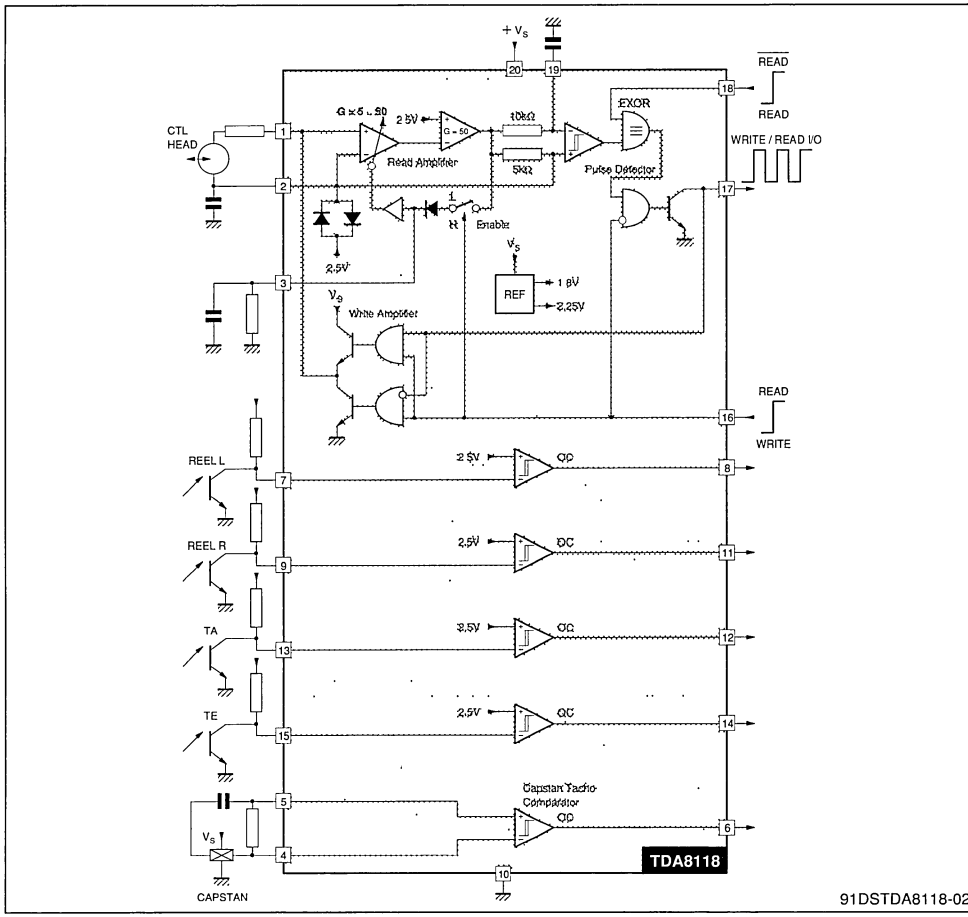
The TDA8118 is a bipolar integrated circuit for VCR application. It is intended to process the CTL-signal in record and playback mode. An internal AGC provides a wide range of input signal level. 5 further internal hysteresis comparators are intended to convert signals from optical and hall sensors to TTL-level.

PIN CONNECTIONS



91DSTDA8118-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	14	V
V_I	DC Iput Voltage	- 0.3 to V_S	V
V_O	DC Output Voltage	V_S	V
I_O	Open Collector Output Current	5	mA
T_{stg}	Storage Temperature	-55 to 125	°C
T_J	Operating Junction Temperature	0 to 85	°C

Note · The circuit is ESD protected according to MIL-STD-883C

THERMAL DATA

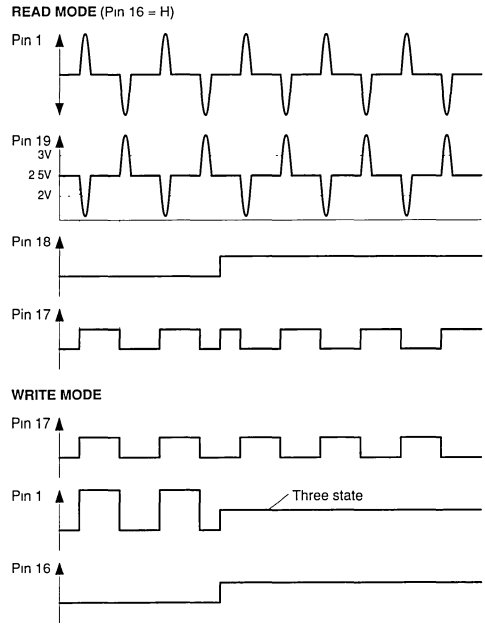
Rth(j-a)	Junction-ambient Thermal Resistance	70	°C/W

ELECTRICAL CHARACTERISTICS

V_S = 5V ±5%, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage (Pin 20)		4.5		6	V
I_S	Supply Current (Pin 20)	Pins 6, 8, 11, 12, 14, 16, 17 open			5	mA
CTL READ AMPLIFIER						
V_{REF}	CTL Reference Voltage (Pin 2)		2.1	2.25	2.4	V
R_{IN}	Input Resistance (Pin 1)		100			kΩ
G_V	Voltage Gain (Pins 1/19)	AGC not active, Pin 3 = GND, f = 1kHz	66			dB
ΔG_V	Voltage Gain range of AGC (Pins 1/19)	f = 1kHz, R_S = 220kΩ, C_3 = 33µF		18		dB
R_F	Filter Output Impedance (Pin 19)		7	10	13	kΩ
V_{IN}	Minimum Peak Input Voltage (Pin 1)		0.5			mV
CTL PULSE DETECTOR						
I_{H+}	Positive Schmitt Trigger Threshold (Pins 17/19)	See timing diagram		V_Z + 0.5		V
I_{H-}	Negative Schmitt Trigger Threshold (Pins 17/19)	See timing diagram		V_Z - 0.5		V
V_{SAT}	Output Saturation Voltage (Pin 17)	V_{17} = Low, I_{17} = 1.8mA			0.4	V
I_C	Output Leakage Current (Pin 17)	V_{17} = V_S			10	µA
V_{REL}	Read Inverter Input Low Voltage (Pin 18)		-0.3		1.5	V
V_{REH}	Read Inverter Input High Voltage (Pin 18)		2.3		V_S	V
CTL WRITE AMPLIFIER						
V_{RWL}	Read/Write Enable Input Low Voltage (Pin 16)		-0.3		1.5	V
V_{RWH}	Read/Write Enable Input High Voltage (Pin 16)		2.3		V_S	V
V_{WRL}	Write Input Low Voltage (Pin 17)	Pin 16 = Low	-0.3		1.5	V
V_{WRH}	Write Input High Voltage (Pin 17)	Pin 16 = Low	2.3		V_S	V
V_{SATL}	Output Saturation Voltage Low State (Pin 1)	I_{SINK} = 5mA, Pin 16 = Low, Pin 17 = Low			0.4	V
V_{SATH}	Output Saturation Voltage High State (Pin 1)	Pin 16 = Low, Pin 17 = High I_{SOURCE} = 5mA I_{SOURCE} = 2mA			 1.5 1.3	 V V
SENSOR INTERFACE						
I_{IN}	Input Bias Current (Pins 7/9, 13/15)	V_{IN} = 1V	-3		1	µA
I_{TH}	Input Threshold Voltage (Pins 7/9, 13/15)		2.1	2.25	2.4	V
I_{HYS}	Input Hysteresis (Pins 7/9, 13/15)		150	200	250	mV
V_{SAT}	Output Saturation Voltage (Pins 8/11/12/14)	I_{SINK} = 1.8mA			0.4	V
I_L	Output Leakage Current (Pins 8/11/12/14)	V_{OUT} = V_S			10	µA
CAPSTAN TACHO COMPARATOR						
I_{IN}	Input Bias Current (Pins 4/5)	V_{IN} = Low	-3		1	µA
V_{OFF}	Input Offset Voltage (Pins 4/5)				5	mV
I_{HYS}	Input Hysteresis (Pins 4/5)			5	10	mV
V_{SAT}	Output Saturation Voltage (Pin 6)	I_{SINK} = 1.8mA			0.4	V
I_{LEAK}	Output Leakage Current (Pin 6)	V_{OUT} = V_S			10	µA

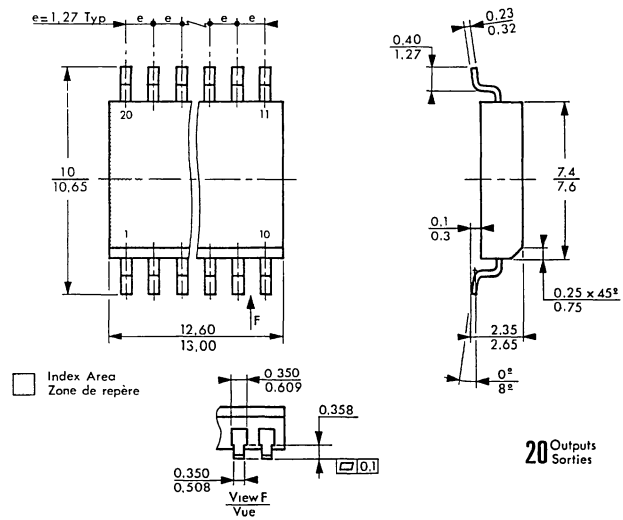
TIMING DIAGRAM



91DSTDA8118-03

PACKAGE MECHANICAL DATA

20 PINS - PLASTIC MICROPACKAGE



SGS-THOMSON MICROELECTRONICS

TDA8120B

MULTISTANDARD VIDEO AND SOUND IF SYSTEM

- GAIN CONTROLLED IF AMPLIFIER
- VIF OPERATING FREQUENCY UP TO 50 MHz
- SYNCHRONOUS DETECTOR
- WHITE SPOT INVERTER
- VERY LOW DIFFERENTIAL ERROR
- VERY LOW PHASE ERROR
- INTERNAL AGC SWITCH (B/G - L)
- AGC TOP. SYNCH. FOR STANDARD B/G
- AGC TOP WHITE FOR STANDARD L
- QUASI SPLIT SOUND FOR STANDARD B/G
- SOUND DETECTOR FOR STANDARD L
- VIDEO MUTING FACILITY
- SEPARATED SOUND OUTPUT
- OPERATES WITHOUT EXTERNAL GATING PULSE

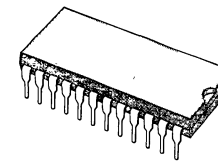
DESCRIPTION

The TDA8120B is a monolithic IC for TV video IF and Sound IF amplification and demodulation that can operate with all the TV standards.

The Video IF section can handle negative (B/G) or positive (L) modulated video signals by means of DC switching.

The Sound IF section acts as a Quasi Split Sound (QSS) subsystem in B/G transmission and allows a second Sound IF with high rejection of the video information.

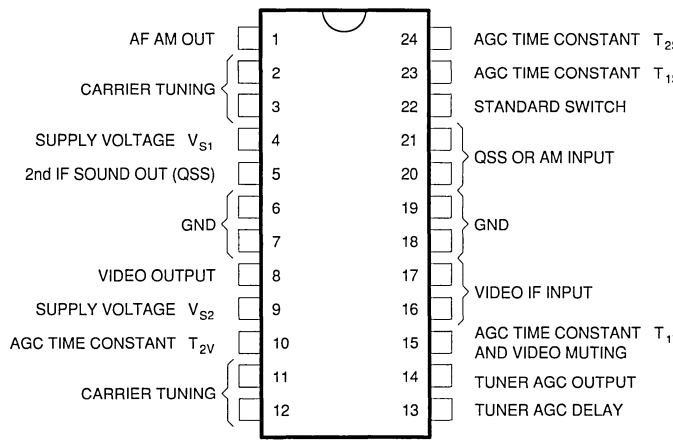
The DC switch can modify the Sound IF configuration to process AM modulated Sound signals (L). The TDA8120B is assembled in a 24 pin dual in line power package.



DIP24
(Plastic Package)

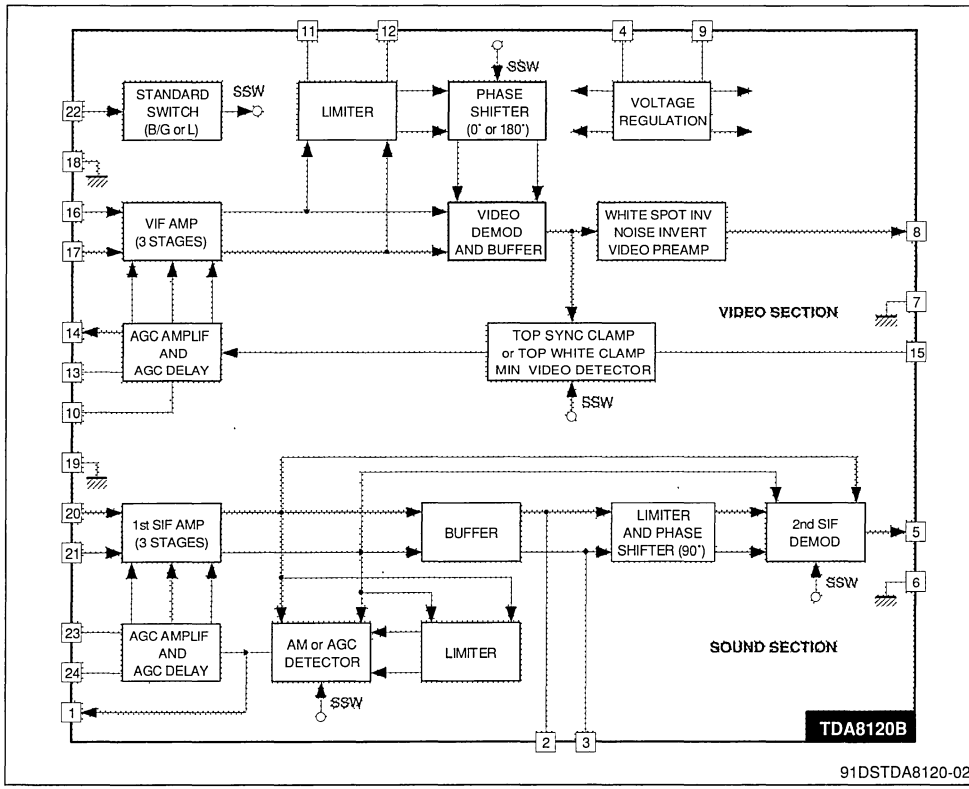
ORDER CODE : TDA8120B

PIN CONNECTIONS



91DSTDA8120-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_4, V_9	Supply Voltage V_s	15	V
I_8, I_5, I_1	Video Out, QSS_{out}, AF AM Out, DC Output Current	10	mA
I_{22}, I_{15}	Pin 22 and Pin 15 Input Current	1	mA
P_{tot}	Total Power Dissipation (T_{amb} = 70 °C)	2	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C
V_{14}	Voltage at Pin 14	V_s	

TAB-01

THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance	Max	40	°C/W

TAB-02

ELECTRICAL CHARACTERISTICS (V_S = 12 V, T_{amb} = 25 °C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VIDEO IF SECTION V_I = 10 mV_{RMS} (black field), F_O = 38.9 MHz ; unless otherwise specified						
V_S	Supply Voltage (pin 4 and pin 9)		10.8	12	13.2	V
I_S	Supply Current	V_I= 0		120		mA
$V_{8\ H}$	Top White Level	V_I = 0 R_L = 1.5kΩ		6		V
$V_{8\ L}$	Top Synchronous Level			3		V
V_8	Video Output B/G	Modulation Depth D = 90 % R_L = 1.5kΩ		3		V_{pp}
V_8	Video Output L	R_L = 1.5kΩ M = 100 %		3		V_{pp}
ΔV_8	Video Output Variat. between Standards B/G and L	M = 100 %		± 2	±10	%
$-I_8$	Output Current	R_L = 1.5kΩ		4		mA
I_8	Input Current		2			mA
I_{14}	Tuner AGC Current Capability			4.5		mA
S/N	Signal to Noise Ratio	B = 5 MHz D = 90 %	50			dB
ΔV_I	AGC Range	ΔV_8 = 1 dB D = 90 %	60			dB
B	Bandwidth	ΔV_8 = – 3 dB D = 90 %	7			MHz
V_{16-17}	Input Sensitivity for Full Output Signal	D = 90 %		50		µV
V_8	Carrier Leakages	F_o = 38.9 MHz		20		mV
		F_o = 77.8 MHz		50		mV
dG	Differential Gain	Subcarrier Modulated Staircase Video Signal D = 90 %			10	%
dϕ	Differential Phase	Subcarrier Modulated Staircase Video Signal D = 90 %			10	degree
d_{IM}	Intermodulation Product 1.07 MHz	Video Carrier Relative Level = 0 dB Chroma Subcarrier Relative Level = – 3.2 dB Sound Carrier Relative Level = – 20 dB		50		dB
R_i	Input Resistance (between pin 16 and pin 17)			1.5		kΩ
C_i	Input Capacitance (between pin 16 and pin 17)			2		pF
QUASI SPLIT SOUND CHANNEL OR FRENCH SOUND CHANNEL (see notes 1 and 2)						
V_{20-21}	Input Sensitivity for Full Output Signal (between pin 20 and 21)	R Channel Missing		50		µV
ΔV_I	AGC Range	ΔV_5 = 1 dB R Channel Missing	60			dB
V_5	Output Voltage Standard B/G	R_L = 600Ω AC Coupled F_O = 5.5MHz		100		mV_{RMS}
		R_L = 600Ω AC Coupled F_O = 5.5MHz		50		mV_{RMS}
I_5	Output Current			2.5		mA
Z_5	Small Signal Output Impedance (QSS)	F_O = 5.5MHz or F_O = 5.74MHz			50	kΩ

TAB-03

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
QUASI SPLIT SOUND CHANNEL OR FRENCH SOUND CHANNEL (see notes 1 and 2)						
R_I	Input Resistance (between Pin 21 and Pin 20)			1.5		kΩ
C_I	Input Capacitance (between Pin 21 and Pin 20)			2		pF
S/N	Noise Ratio QSS (after SIF limitation and FM demodulation) F_O = 5.50MHz F_O = 5.74MHz	Channel R or Channel L Switched off F_m = 1kHz Δf = ± 30kHz Carrier Modulated with Syncs. Pulses Only. CCIR 468-2 Recommendant	 60 58			 dB dB
V_1	Output Voltage Standard L			0.7		V_{RMS}
I_1	Output Current			2.5		mA
Z_1	AF Output Impedance (L)				50	Ω
S/N	Noise Ratio AM Standard L	B_N = 20kHz	46			dB
d	Distorsion				3	%
V_{22}	B/G Operation		2		5	V
V_{22}	L Operation		0		0.8	V
V_{15}	Video Muting		8		V_S	V

TAB-04

Notes : 1. QUASI SPLIT SOUND CHANNEL

Video carrier relative level = 0 dB f= 38 9 MHz

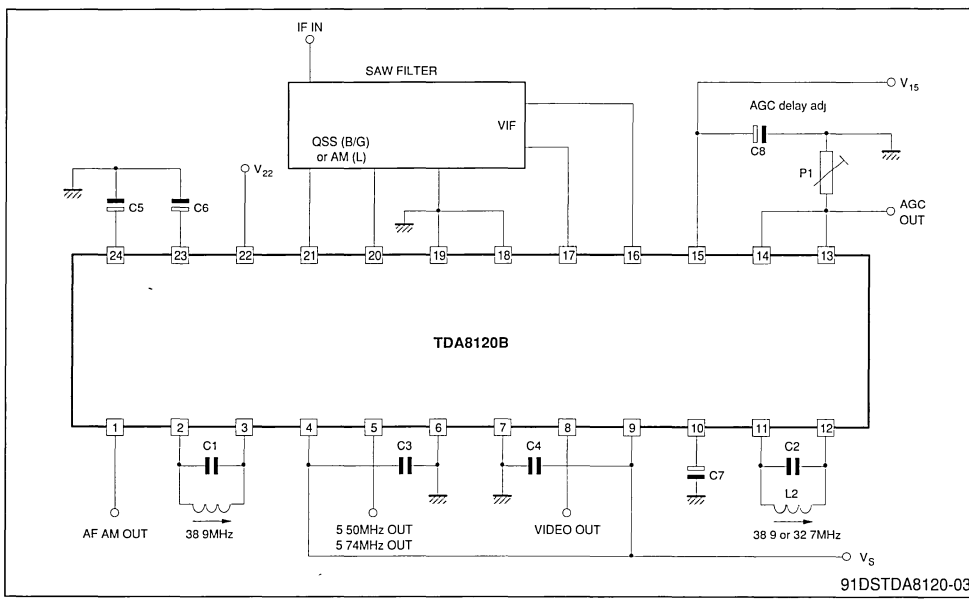
$\Delta f = 0$ { Sound carrier relative level = – 13 dB (mono or L) f = 33 4 MHz
Sound carrier relative level = – 20 dB (R) f= 33 16 MHz

V_I = 10 mV Video carrier modulated with syncs , V_{22} = 2 V, unless otherwise specified

2. FRENCH SOUND CHANNEL

V_I = 10 mV (Carrier level) ; f_o = 39.2 MHz , F_m = 1 KHz ; m = 80 % ; V_{22} = 0 8 V, unless otherwise specified.

TEST CIRCUIT



CIRCUIT OPERATION

The TDA8120B (see block diagram) consists of a video section and a sound section. The integration of both sections on the same chip requires a high isolation at IF frequencies. This is achieved by physically separating the two sections, with separate power supplies and ground pins. In addition, special care has been taken in the choice of pad positions for the IF inputs and sound/video outputs.

The video section consists of three AC-coupled IF stages with more than 60 dB AGC range, flat amplitude/frequency response from 10 to 85 MHz and linearized phase slope from 30 to 50 MHz. Video carrier regeneration is performed by a tuned limiter. The carrier is then applied to the video demodulator through a special circuit which switches the carrier phase from 0 to 180° so that the video polarity can be maintained constant when the standard switches from B/G to L. A noise inverter and a white spot inverter are included to eliminate ultra-black and white pulses.

A top sync or a top white clamping circuit and a minimum DC video component detector are implemented by two double comparators the characteristics of which may be controlled by an external control input to adapt to the modulation type for each standard. The voltage at the output of the two comparators is memorized by an external capacitor and used to drive the AGC network, which allows an input regulation of the video carrier from less than 100 µV to 100 mV. A delayed control storage with current output for the turner AGC completes the video section.

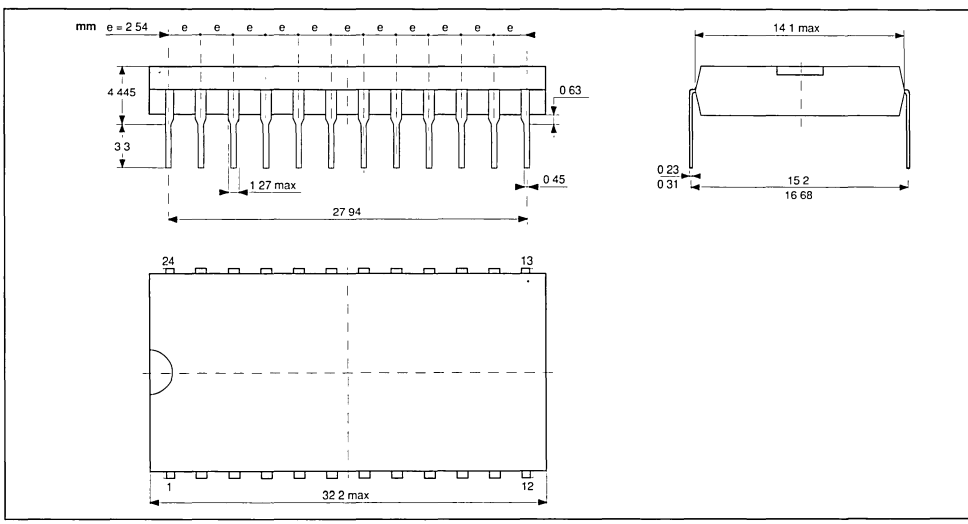
The sound section consists of three IF stages with the same characteristics as the video IF stages and an identical network to control and set the gains of the three IF amplifiers. The output of the third IF stage feeds the AM/AGC detector and the QSS section.

The AM/AGC detector consists of a wideband limiter for AM sound regeneration or video carrier regeneration used to feed the synchronous multiplier and consequently to obtain the AM demodulated audio signal. In addition, a DC voltage proportional to the peak-to-peak value of the video carrier is produced. Two comparators complete the sound AGC loop.

The subsequent QSS section consists of a reference amplifier tuned to the video IF which buffers a wideband limiter to reject completely the video AM information without introducing incidental phase modulation (IPM).
Following the limiter there are a 90° phase shifter and a linear-to-logarithmic converter which drives a linear multiplier as a demodulator for the intercarrier 2nd sound IF. This quadrature multiplier rejects all video components transmitted in DSB that is low frequency components of the video signal.

In addition to the sound and video sections, the TDA8120B includes a block for standard switching (B/G or L) controlled by a TTL-compatible input.

PACKAGE MECHANICAL DATA : 24 PINS - PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

TDA8123A

MULTISTANDARD VIDEO IF SYSTEM

ADVANCE DATA

- MULTISTANDARD VIDEO IF (POSITIVE AND NEGATIVE MODULATION)
- WHITE SPOT INVERTER AND NOISE SUPPRESSOR
- HIGH INPUT SENSITIVITY
- VERY LOW SENSITIVITY OF VISION OUTPUT AMPLITUDE VERSUS TEMPERATURE AND V_{CC}
- VERY LOW DIFFERENTIAL PHASE AND GAIN
- VERY LOW SENSITIVITY TO THE DETUNING OF THE IF VIDEO CARRIER
- HIGH STABILITY OF THE TUNER AGC CURRENT

DESCRIPTION

The TDA8123A is a multistandard B/G and L video IF demodulator consisting of three AC coupled IF stages with more than 60dB AGC range, flat amplitude/frequency response from 10 to 85 MHz and linearized phase slope from 30 to 50MHz.

Video carrier regeneration is performed by a tuned reference amplifier and a wide band limiter increasing the linearity, the differential phase and gain and reducing the sensitivity to the detuning of the 38.9MHz coil.

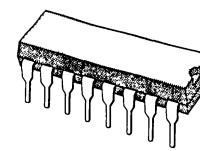
The carrier is then applied to the video demodulator through a special circuit which switches the carrier phase from 0^{o} to 180^{o} so that the video polarity can be maintained constant when the standard switches from B/G to L.

A noise inverter and a white spot inverter are included in order to eliminate ultra-black and white pulses. The last one can be disabled applying a voltage higher than 2V at Pin7.

The video output is applied also to the AGC circuit that performs a top sync or a top white clamp, implemented by two double comparators, and reconstructs the DC video components in accordance with the two different standards. The voltage at the output of the two comparators is memorized by an external capacitor and used to drive the AGC network, which allows an input regulation of the video carrier from less than 100µV to 100mV.

The integrated circuit is completed by a delayed control storage with current output for the tuner AGC. This current has a very low sensitivity to temperature variations.

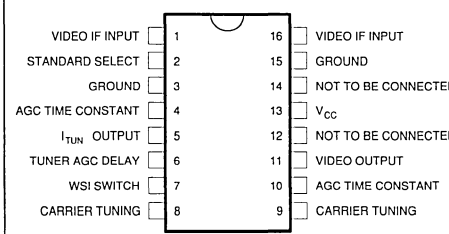
The TDA8123A includes also a block for the standard switching (standard B/G or standard L) controlled by a TTL compatible input.



DIP16
(Plastic Package)

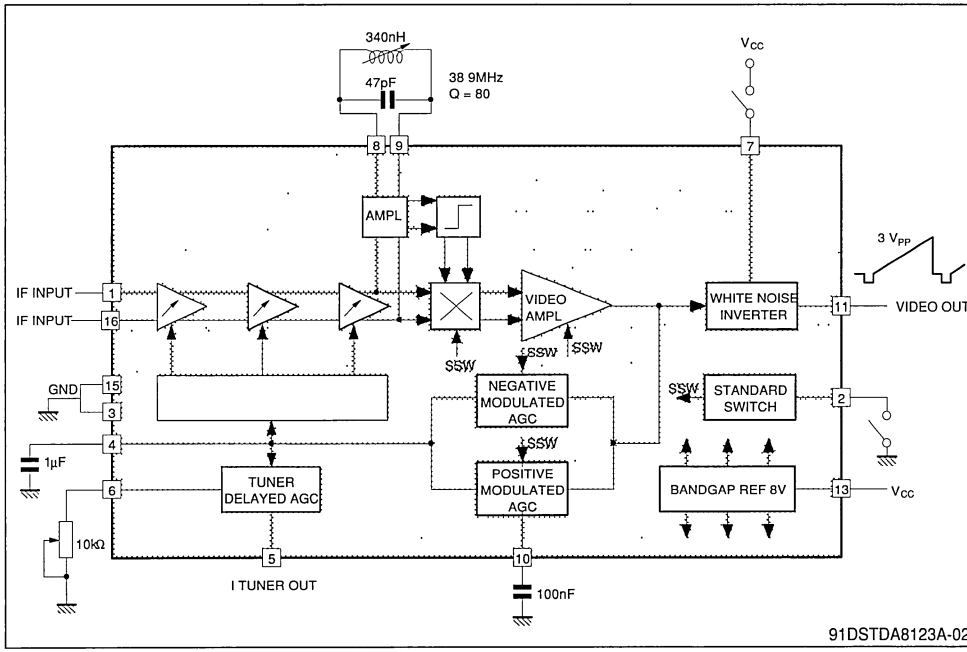
ORDER CODE : TDA8123A

PIN CONNECTIONS



91DSTDA8123A-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	15	V
V_5	Tuner AGC Voltage	V_S	V
I_{11}	Video Out DC Out Current	10	mA
I_2	Pin 2 Input Current	1	mA
P	Power Dissipation at T_{AMB} = 70°C	1	W
T_{stg}	Storage Temperature	-40 to +150	°C

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	Max.	80	°C/W

ELECTRICAL CHARACTERISTICS

V_S = 12V, f_{VC} = 38.9MHz, V_{VC} = 10mV_{RMS}
Mod. AM/DSB : T_A = 25°C, Input Video Signal = Sawtooth
Standard B/G : R = 10%, D = 90%
Standard L : M = 100%, R < 6%
(unless otherwise specified)

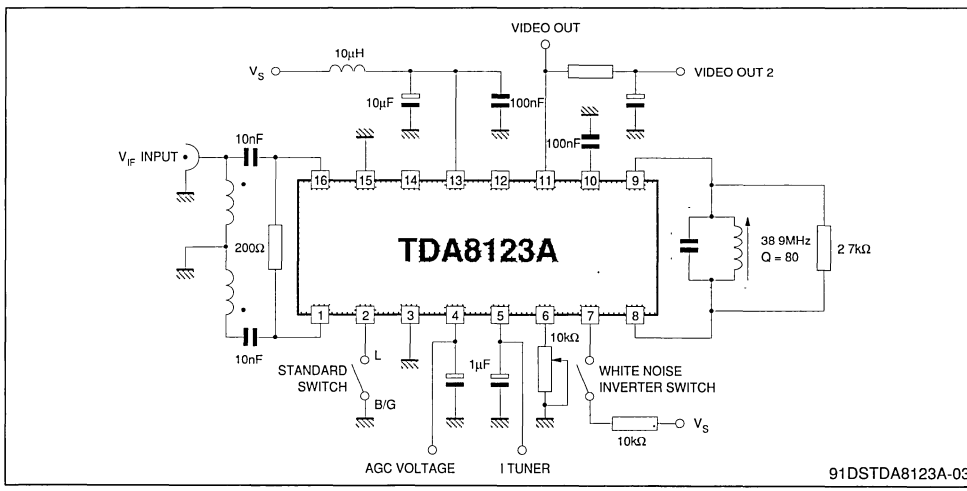
Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage Range	V_{OUT} unchanged	10.8	12	13.2	V
Supply Current		40	57	74	mA
Input Sensitivity	V_{OUT} = - 3dB		60		µV
AGC Range		60			dB
Top White Level B/G	See Fig.1		4.9		V
Top Sync. Level B/G	See Fig.1		1.9		V
DC Output Voltage for Zero Carrier B/G	See Fig.1		5.05		V
Top White Level L	See Fig.1		4.9		V
Top Sync. Level L	See Fig.1		1.9		V
DC Output Voltage for Zero Carrier L			1.9		V
Difference between V_{PP} B/G and V_{PP} L				10	%
Threshold of Negative Noise Clamp	Under the top sync. level - See Fig.1		100		mV
White Spot Inverter ON				1.2	V
		or unconnected			
White Spot Inverter OFF		2		V_S	V
White Inverter Threshold	Over the top white level - See Fig.1		900		mV
White Inverter Insertion Level	See Fig.1		3.5		V
Top White Level Relation versus Supply Voltage	V_S range		1		%
Top Black Level Relation versus Supply Voltage	V_S range		0.5		%
Video Output Peak to Peak Variation versus Supply Voltage	V_S range			1	%
Bandwidth (- 3dB)			10		MHz
Flatness of Video Response in the Whole AGC Range				2	dB
DC Output Current	Pin 11 held at 10V		2		mA
Residual Carrier at Video Output in the Whole AGC Range	38.9MHz 77.8MHz		10 20		mV mV
Differential Gain	B/G and L		3		%
Differential Phase	B/G and L		3		deg
Differential Gain Variation versus Detuning of ± 400kHz of LC at Pin 8 and 9				1	%
Differential Phase Variation versus Detuning of ± 400kHz of LC at Pin 8 and 9				2	deg
Intermodulation Products related to the Demodulated Color Carrier (1.07MHz)	• Video carrier = 0dB • Color carrier = -6dB • Sound carrier = -20dB		50		dB

ELECTRICAL CHARACTERISTICS (continued)

V_S = 12V, f_{VC} = 38.9MHz, V_{VC} = 10mV_{RMS}
Mod. AM/DSB : T_A = 25°C, Input Video Signal = Sawtooth
Standard B/G : R = 10%, D = 90%
Standard L : M = 100%, R < 6%
(unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Compression of the sync. pulse in the Whole AGC Range			3		%
Switch Voltage B/G		2		V_S	V
Switch Voltage L		0		1.2	V
I_{TYP} of Charge AGC Standard B/G	See Fig. 2		1.7		mA
I_{TYP} of Discharge AGC Standard B/G	See Fig. 2		19		µA
AGC Reacting Time Standard L				10	µs
I_{TYP} of Charge AGC Standard L	See Fig. 3		5		mA
I_{TYP} of Discharge AGC Standard L	See Fig. 3		260		µA
I_{TYP} of Discharge of the Capacitor at Pin 4 during Stationary State			100		nA
AGC Tuner Current at 10dB over the AGC Start Point	See Fig. 4	3	4	5	mA
$\frac{\Delta I_{TUNER}}{\Delta V_{IF}}$ Slope	10% to 90% See Fig. 4		250		$\frac{\mu A}{dB}$
$\frac{\Delta I}{\lvert \Delta T \rvert}$	V_{IF} = const., T_A = 100°C I_{TUNER} = I_{TUNER} Max. / 2		0.5		%
Input Resistance Symmetrical between Pin 1 and 16			1.6		kΩ
Input Capacitance Symmetrical between Pin 1 and 16			2		pF

TEST CIRCUIT



MEASUREMENTS CONFIGURATION

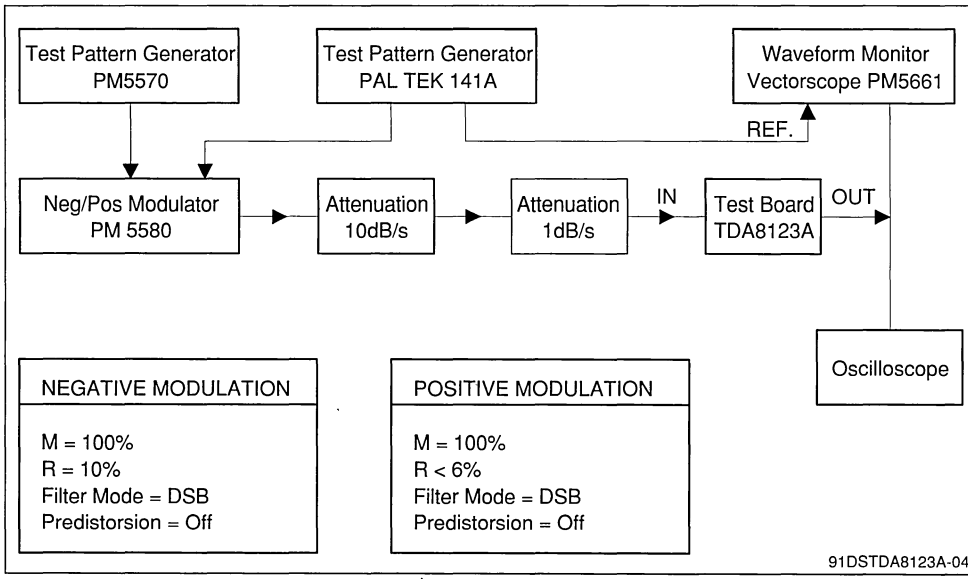


Figure 1 : Output Video Signal Levels

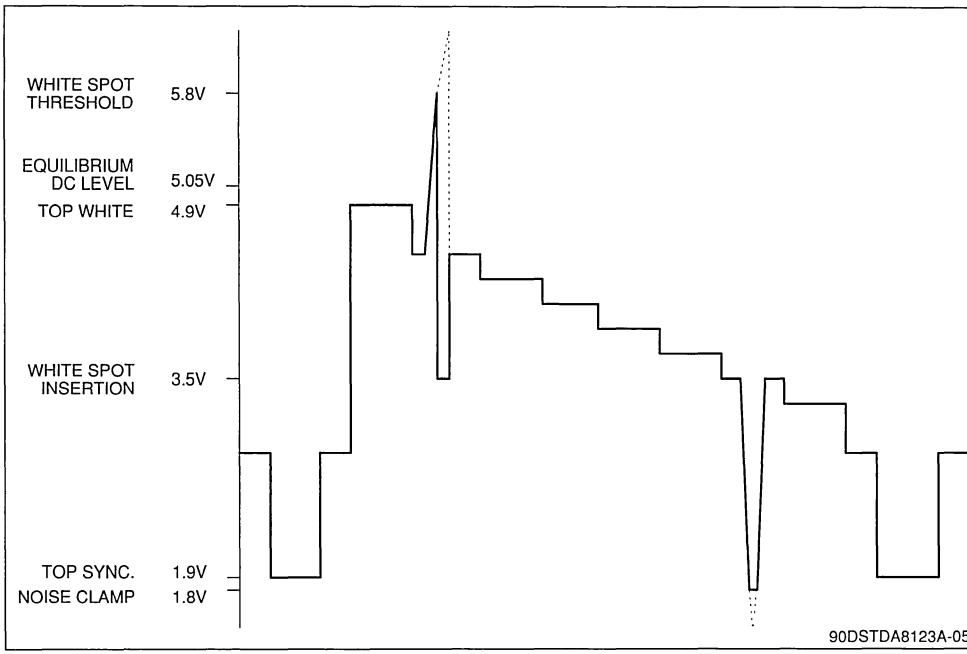
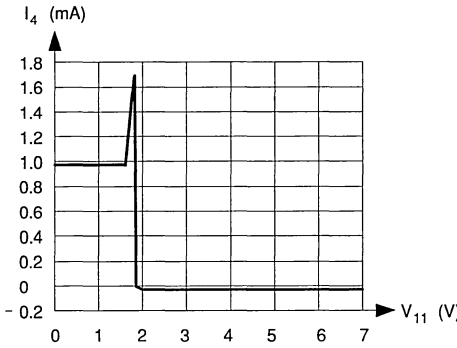
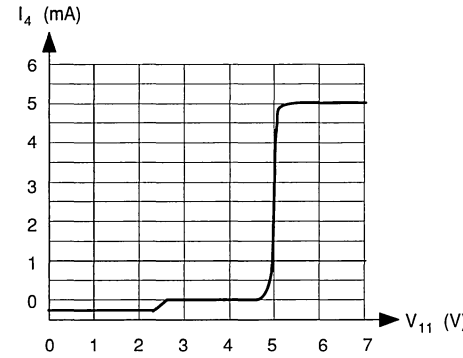


Figure 2 : AGC Current (standard B/G)



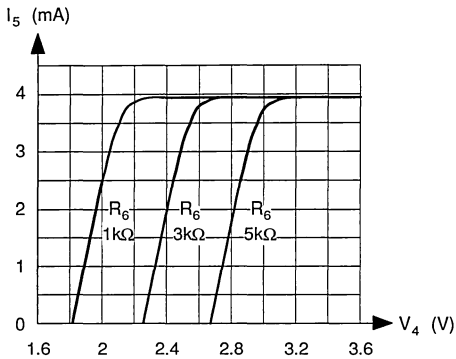
91DSTDA8123A-06

Figure 3 : AGC Current (standard L)



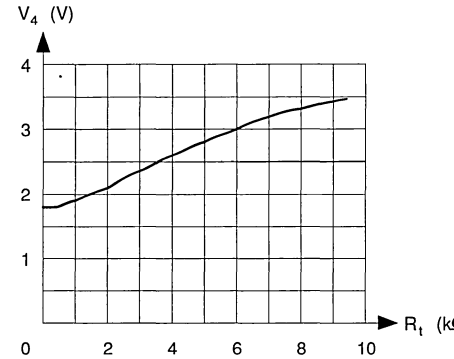
91DSTDA8123A-07

Figure 3 : Tuner AGC Output Current



91DSTDA8123A-08

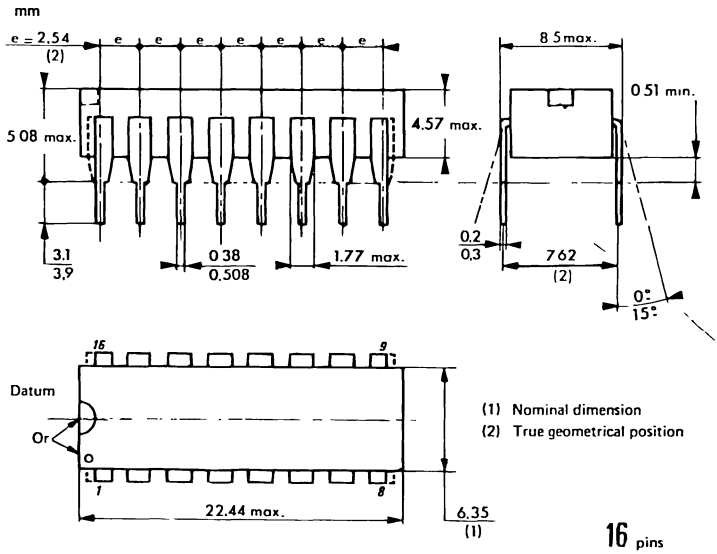
Figure 4 : Starting Point of Tuner Regulation



91DSTDA8123A-09

PACKAGE MECHANICAL DATA

16 PINS - PLASTIC DIP



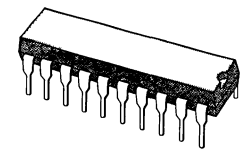
SGS-THOMSON MICROELECTRONICS

TDA8124

MULTISTANDARD VIDEO IF INTERFACE

PRELIMINARY DATA

- AUTOMATIC IDENTIFICATION OF PICTURE-CARRIER MODULATION POLARITY
- VIDEO SIGNAL IDENTIFICATION (FOR SOUND MUTING)
- ANALOG AND DIGITAL A.F.C. FOR STOP TUNING FUNCTION
- PICTURE CARRIER DETECTION IN A RANGE OF 1MHz AROUND THE IF-PICTURE CARRIER VALUE



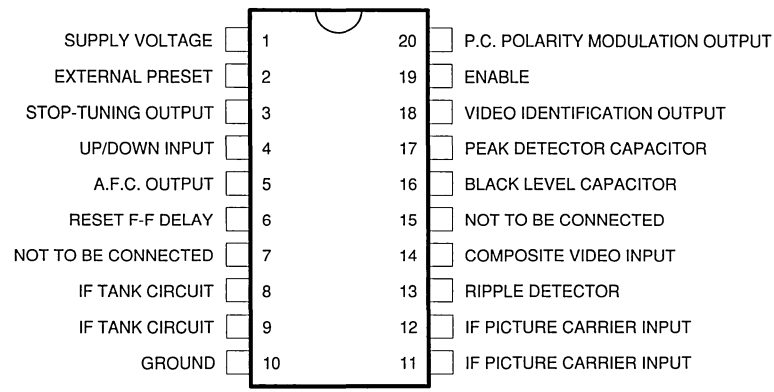
DIP20
(Plastic Package)

ORDER CODE : TDA8124

DESCRIPTION

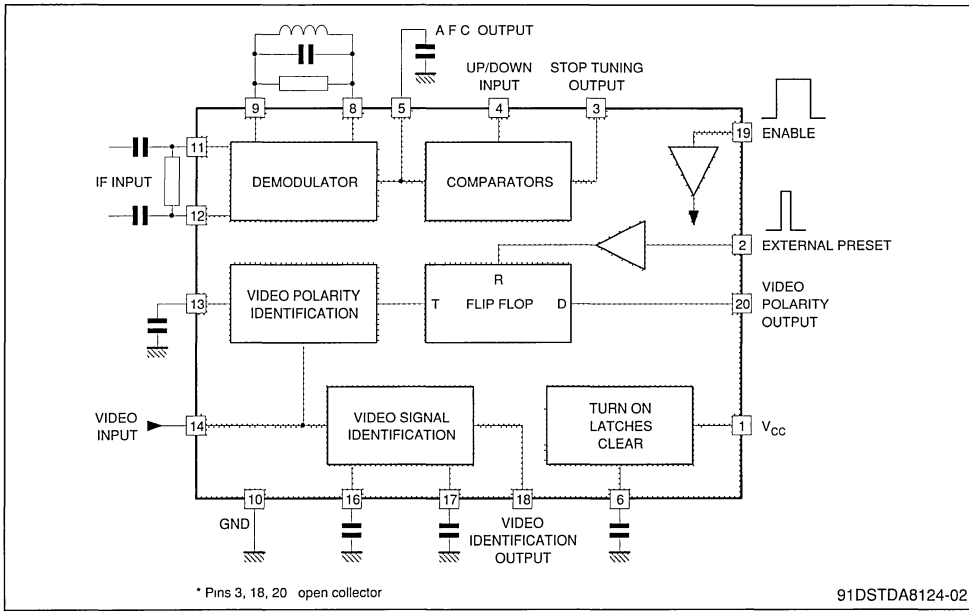
The TDA8124 has been developed in order to permit automatic standard switching and tuning when coupled with a multistandard VIDEO IF IC (for example TDA8120). It contains an A.F.C. synchronous demodulator and an A.F.C. comparator, a video polarity identification circuit with logic and a video signal identification system.

PIN CONNECTIONS



91DSTDA8124-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 1)	15	V
T_{oper}	Operating Ambient Temperature Range	0 to + 70	°C
T_{stg}	Storage Temperature Range	- 20 to + 150	°C

THERMAL DATA

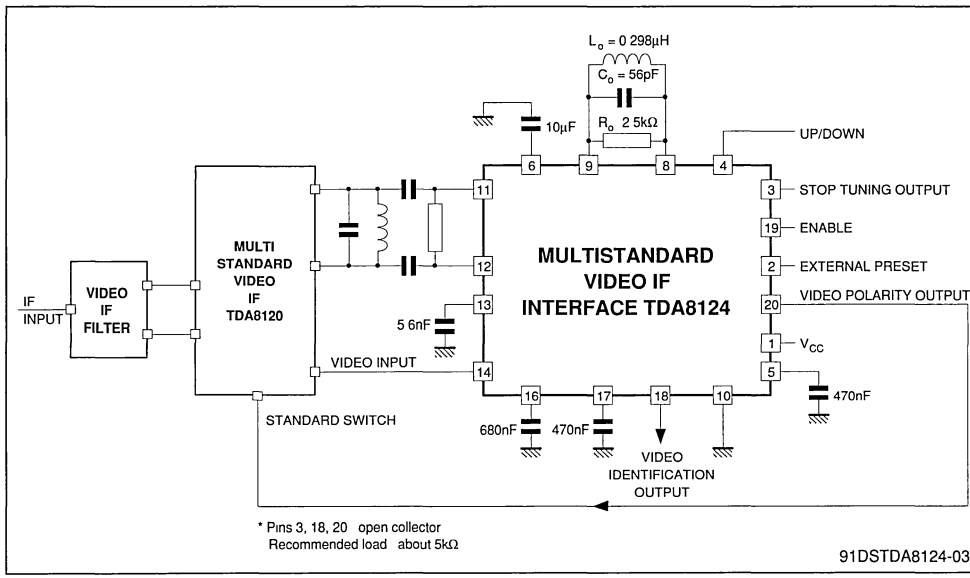
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	Max.	80	°C/W
$R_{th\ (j\text{-}c)}$	Junction-case Thermal Resistance	Max.	14	°C/W

ELECTRICAL CHARACTERISTICS

T_{AMB} = 25°C, V_{CC} = 12C (unless otherwise specified)
- Positive video input signal V_I = $3V_{PP}$ with top sync level = 3V
- Enable ≤ 0.8V or open

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	1		10.8	12	13.2	V
I_S	Supply Current	1		15	22	29	mA
	Video Input Top Sync Level	14	• B/G standard : M = 100%, D = 90% • L/E standard : M = 100%, R ≤ 6%		3		V
	Video Input Top White Level	14	• B/G standard : M = 100%, D = 90% • L/E standard : M = 100%, R ≤ 6%		6		V
	Composite Video Input Voltage	14		2.7	3	3.3	V_{PP}
	Ripple Voltage accross the 5.6nF External Capacitor	13	C13 = 5.6nF		400		mV
	Black Level Clamp Level	16			4		V
	Ripple Voltage	16	C16 = 680nF		30		mV
	Peak Detector Voltage	17			6.8		V
	Peak Detector Ripple Voltage	17				200	mV
	Video Identification Current Capability	18				10	mA
	Minimum Sync Amplitude for Video Identification	14		450			mV_{PP}
	External Preset up/down and enable switch voltages	2, 4 19		0 2		0.8 V_{CC}	V V
	External Preset, up/down, Enable Pins Input Impedance	2, 4 19		35	50		kΩ
	Video Identification Out Voltage	18	Enable ≥ 2V P.C. IF = 38.9MHz • L/E (positive modulation) • B/G (negative modulation)		 V_{CC}	 0.5	 V V
	IF Picture Carrier Input Voltage	11, 12	P.C. IF = 38.9MHz	50			mV_{PP}
	A.F.C. Output Slope	5	Q_{LC} = 80, C_O = 56pF, $L_O \cong 0.298\mu H$, R_O = 2.5kΩ	0.5		0.85	$\frac{V}{100kHz}$
	$V_{11\text{-}12}$ DC Voltage	11, 12			3.8		V
	V8-9 DC Voltage	8, 9			3.65		V
	Stop/Tuning Output Voltage	3	• No picture carrier or 39.4MHz < IF < 38.4MHz • With picture carrier IF_{PC} ≥ 38.9MHz IF_{PC} ≤ 39.4MHz		0 V_S		V V
	Stop/Tuning Output Bandwidth	3		1.1	1.3	1.5	MHz

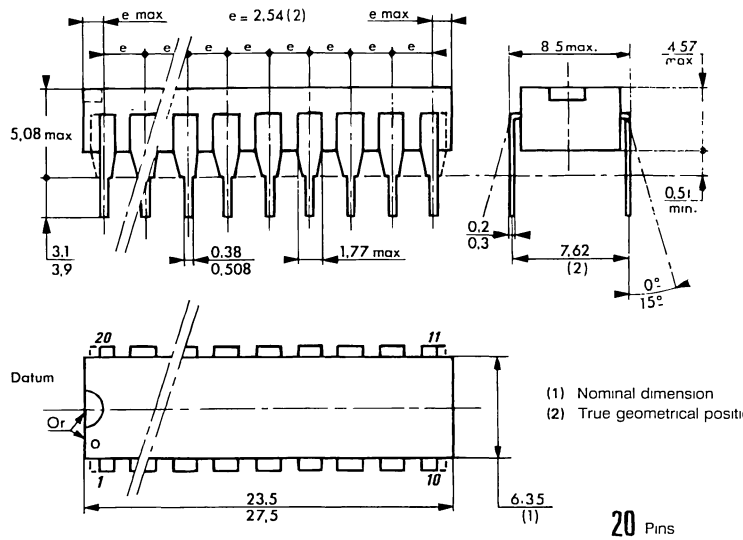
TYPICAL APPLICATION (with TDA8120)



PACKAGE MECHANICAL DATA

20 PINS - PLASTIC DIP

Dimensions in mm



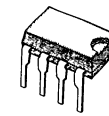
SGS-THOMSON MICROELECTRONICS

TDA8128

SYNC SEPARATOR AND VIDEO SIGNAL IDENTIFICATION

ADVANCE DATA

- AC COUPLED COMPOSITE VIDEO SIGNAL
- COMPOSITE SYNC OUTPUT
- EDGE TRIGGERED VERTICAL SYNC OUTPUT
- AUDIO MUTING OUTPUT



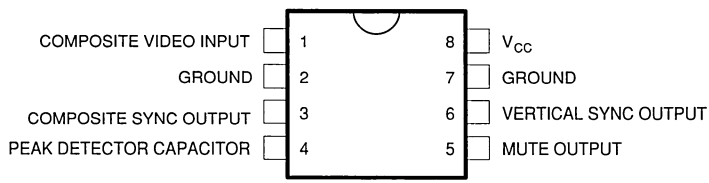
DIP8
(Plastic Package)

ORDER CODE : TDA8128

DESCRIPTION

The TDA 8128 Is a monolithic integrated circuit in DIP8 package. It provides composite sync, edge triggered vertical sync and audio muting signals.

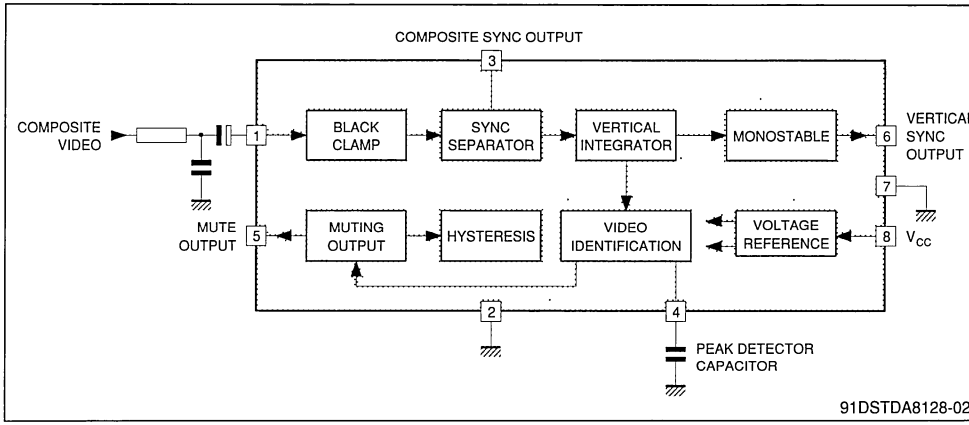
PIN CONNECTIONS



91DSTDA8128-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	15	V
	Sink Current (Pins 3, 5, 6)	20	mA
T_{oper}	Operating Ambient Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature	-40, +150	°C

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	90 Typ.	°C/W

GENERAL DESCRIPTION

The TDA8128 extracts the composite and vertical sync signals from a video input signal with a negative going horizontal sync pulse.
By means of an internal monostable, the beginning of the vertical sync is triggered by the rising edge of the first serration in the vertical sync period.

The device also provides information when the input signal is not a true video signal or if its amplitude is below a certain limit.
The output stages are supplied by an internal reference voltage so that no external pull-up resistors are needed.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_{amb} = 25°C,
Video Signal : standard PAL color bar generator (V_I = 2V_{PP}) (unless otherwise specified)

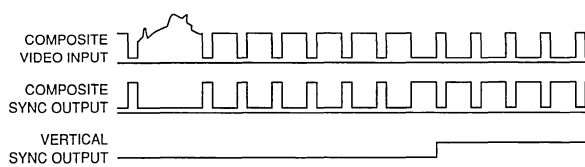
Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_8	Supply Voltage	8		10.8	12	13.2	V
I_8	Supply Current	8			7	15	mA
V_{IN}	Input Signal Range	1			2	5	V_{PP}

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 12V, T_{amb} = 25°C,
Video Signal : standard PAL color bar generator (V_I = 2V_{PP}) (unless otherwise specified)

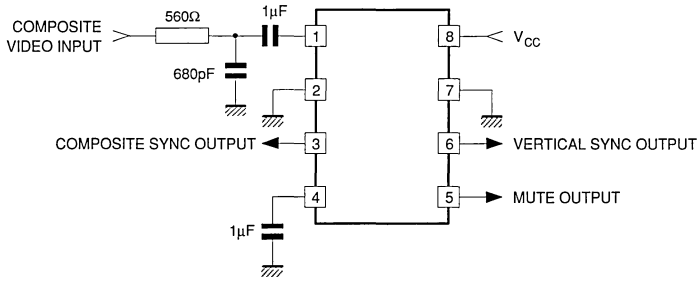
Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
COMPOSITE SYNC OUTPUT							
WH	Min. Horizontal Input Sync Width	3	For stable output signals	4	4.7	5.5	µs
$V_{1\ min}$	Min. Input Sync Pulse Amplitude	1	Stable output signal on Pin 3		330	400	mV_{PP}
V_3	Pulse Amplitude	3		4.5	5	5.3	V
$V_{3\ sat}$	Output Saturation Voltage	3	I_3 = 1mA			200	mV
R3	Input Pull-up Resistor	3		3.5	5	6.5	kΩ
T3/1	Composite Sync Extract Delay	3/1	At 50% of sync pulse amplitude		1	2	µs
IDENTIFICATION OUTPUT							
$V_{1\ ON}$	Min. Input Composite Sync Pulse Amplitude	1	Identification output going from no ident to ident		300	350	mV_{PP}
V_{1OFF}	Max. Input Composite Sync Pulse Amplitude	1	Identification output going from ident to no ident	150	210		mV_{PP}
HYS	Hysteresis	5	By attenuation of the input signal Pin 1		3		dB
V_{5H}	Identification Output Voltage	5	Video not identified	4.5	5	5.3	V
V_{5L}		5	Video identified, I_5 = 1mA			200	mV
R5	Internal Pull-up Resistor	5		3.5	5	6.5	kΩ
TI	Identification Delay	5/1	Delay between the first incoming inverted line pulse and ident output signal • C4 = 1µF • C4 = 470nF		 2 1	 3	 Frame Frame
VERTICAL PULSE OUTPUT							
$V_{1\ min}$	Min. Input Composite Sync Pulse Amplitude	1	Stable output pulse (Pin 6) Input pulse increasing		300	350	mV_{PP}
TFR	Vertical Pulse Width	6	Standard PAL color bar pattern (2V_{PP})	100	250	400	µs
V_{6H}	Vertical Pulse Amplitude	6		4.5	5	5.3	V
$V_{6\ sat}$	Output Saturation Voltage	6	I_6 = 1mA			200	mV
R6	Internal Pull-up Resistor	6		3.5	5	6.5	kΩ
TDFR	Vertical Pulse Delay	6/1	Delay between the first incoming inverted line pulse (Pin 1) and vertical pulse at 50% amplitude		1	2	µs
JIT	Vertical Rising Edge Jitter	6	Video signal pollution free		100		ns

WAVEFORMS (Pin 7 grounded)



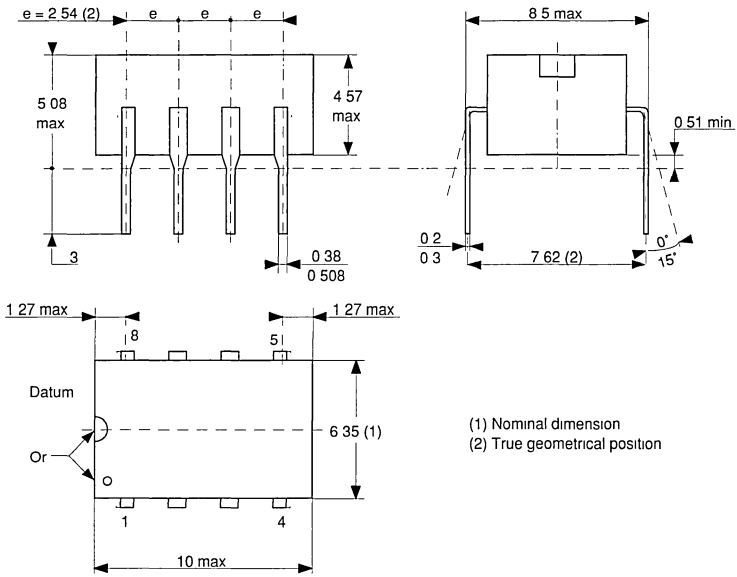
90DSTDA8128-03

TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MINIDIP

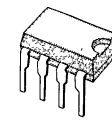


SGS-THOMSON MICROELECTRONICS

TDA8160

INFRARED REMOTE CONTROL RECEIVER

- LOW SUPPLY VOLTAGE (V_S = 5V)
- LOW CURRENT CONSUMPTION (I_S = 6mA)
- INTERNAL 5.5 V SHUNT REGULATOR
- PHOTODIODE DIRECTLY COUPLED WITH THE I.C.
- INPUT STAGE WITH GOOD REJECTION AT LOW FREQUENCY
- LARGE INPUT DYNAMIC RANGE
- FEW EXTERNAL COMPONENTS



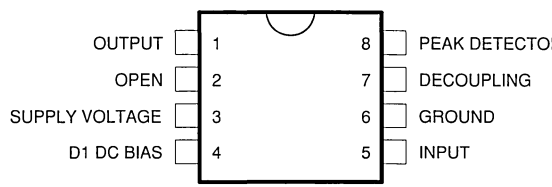
MINIDIP
(Plastic Package)

ORDER CODE : TDA 8160

DESCRIPTION

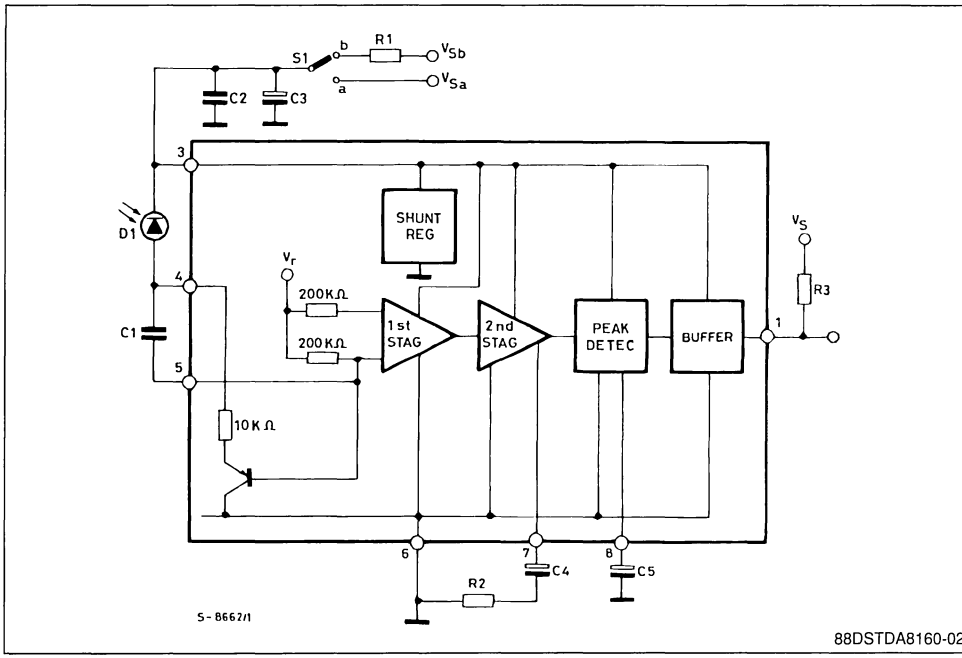
The TDA 8160 is a monolithic integrated circuit in-lead minidip plastic package specially designed to amplify the infrared signals in remote controlled TV, Radio or VCR sets. It can be used in flash transmission mode in conjunction with dedicated remote control circuits (for example : M491-494).

PIN CONNECTIONS

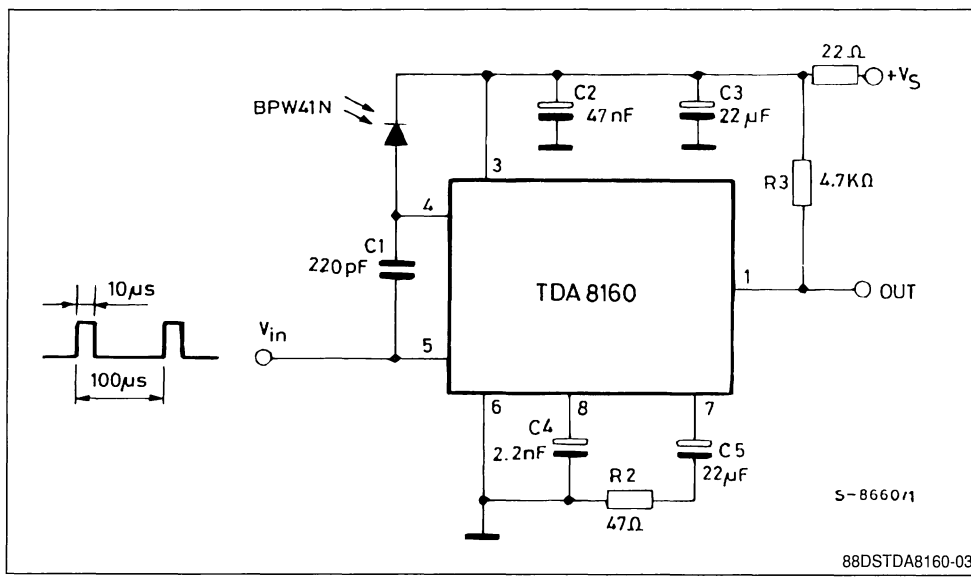


91DSTDA8160-01

BLOCK DIAGRAM



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
T_{stg-j}	Storage and Junction Temperature	– 40 to 150	°C
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	400	mW

TAB-01

THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	200	°C/W

TAB-02

ELECTRICAL CHARACTERISTICS

(refer to the test circuits ; V_S = 5 V, f_o = 10 kHz, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	Applied between Pin 3 and 6	4	5	5.25	V
I_S	Suppply Current (pin 3)			6		mA
V_3	Stabilized Voltage at Pin 3	I_3 = 8 mA		5.5		V
G_V1st	Voltage Gain (1st stage)			28		dB
g_m2nd	Transconductance (2nd stage)			15		mA/V
V_{in}	Input Voltage Sensitivity (pin 5)	For Full Swing at the Output Pin 1 R_{gen} = 600 Ω		2		mV_p
I_{in}	Input Current Sensitivity (pin 5)	For Full Swing at the Output Pin 1		10		nA_p
R_{in}	Input Impedance			200		KΩ
L_fR	Low Frequency Rejection at the Input Stage	C1 = 100 pF f = 100 Hz		30		dB
N	Noise Signal at Pin 7	C4 missing		200		mV_{pp}

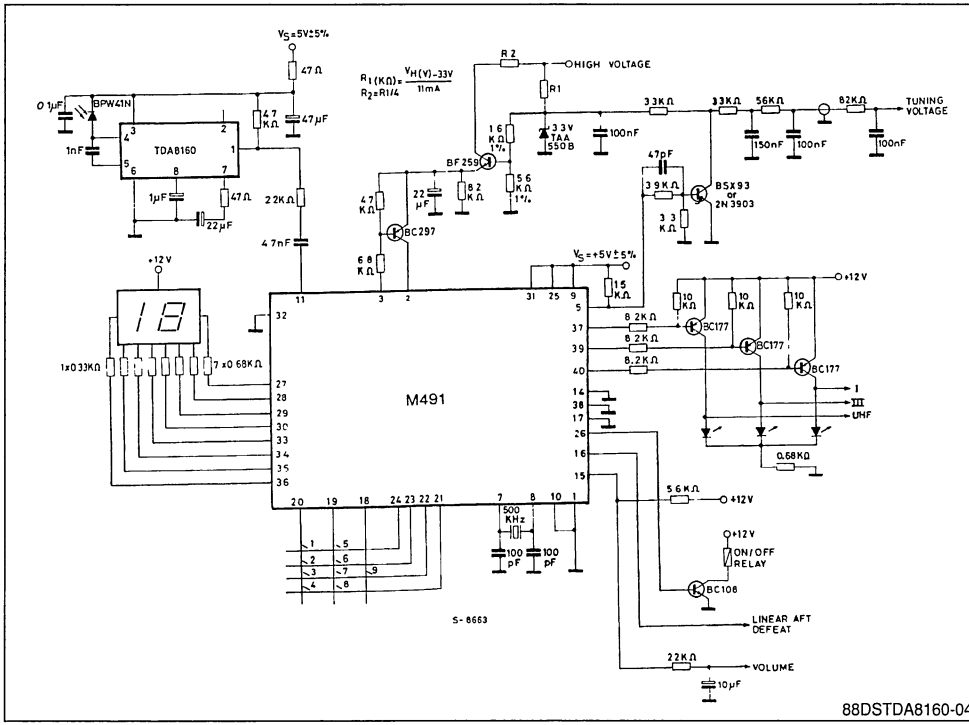
TAB-03

CIRCUIT DESCRIPTION (see the block diagram)

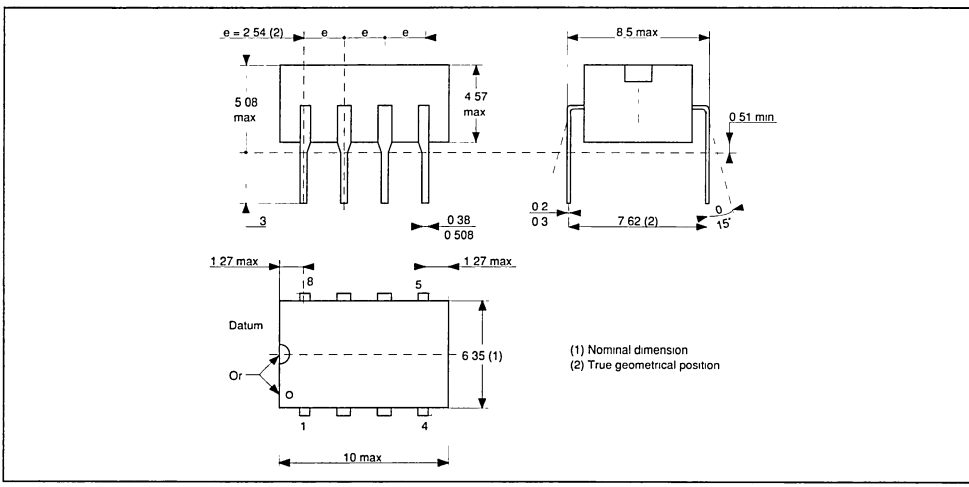
The infrared light received from D1 generates an AC signal that comes in to the device at pin 5. The capacitor C1 and the integrated 10KΩ resistor (pin 4) filter out the low frequency noise.

The first stage shows a voltage gain of about 28dB ; the second stage is a voltage to current converter of 50mA/V (R_2 = Zero). A sensitive peak detector detects the amplifier signal ; one open collector output (pin 1) gives out the recovered pulses.

Figure 1 : Recommended Application Circuit for the Drive of the IC M491 by Means of a Flash Mode IR. Transmitter only, in a TV 16 Station Memory Remote Control Subsystem. The Above Shown IR Receiver Application must be Housed Inside a Metal Can Shield.



PACKAGE MECHANICAL DATA : 8 PINS - PLASTIC DIP



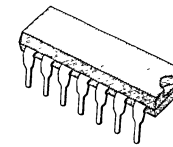
SGS-THOMSON MICROELECTRONICS

TDA8162

INFRARED REMOTE CONTROL RECEIVER

ADVANCE DATA

- LOW SUPPLY VOLTAGE (V_S = 5V)
- LOW CURRENT CONSUMPTION (I_S = 4mA)
- INTERNAL 5.5V SHUNT REGULATOR
- INPUT STAGE WITH GOOD REJECTION AT LOW FREQUENCY
- SELECTIVE AMPLIFIER
- LARGE INPUT DYNAMIC RANGE
- HIGH INPUT SENSITIVITY
- A.G.C. FACILITY



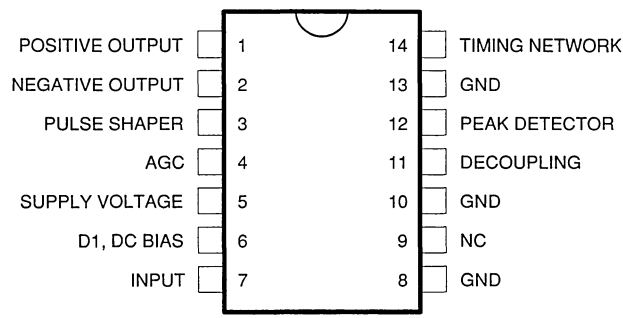
DIP14
(Plastic Package)

ORDER CODE : TDA8162

DESCRIPTION

The TDA8162 is a monolithic integrated circuit in 14-lead dual in line plastic package specially designed to amplify the infrared signals in remote controlled TV, Radio or VCR sets.
It is properly designed to work in "CARRIER" transmission mode and the open collector output allows direct operation with dedicated remote control circuit (for example M206) or microprocessor systems ST6 Family).

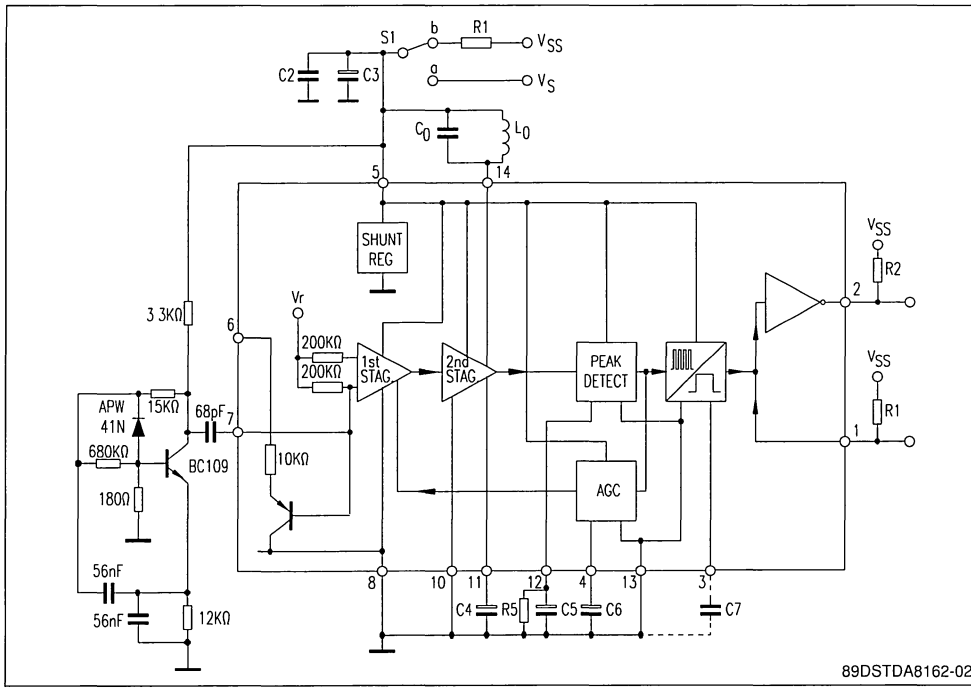
PIN CONNECTION



91DSTDA8162-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



The infrared light received from D1 generates an alternate current that, through the transistor T1, comes into the device at pin 7.

The capacitor C1 and an internal network filter out the low frequency noise.

The first stage, the gain of which is controlled by AGC, shows a maximum voltage gain of about 30dB.

The second stage is a selective amplifier (the frequency is generally included between 30kHz and 40kHz), with an voltage gain of about 50dB, loaded by Lo, Co.

A sensitive peak detector detects the amplified signal, two open collector outputs (pin 1, 2) allow positive and negative signals respectively.

The recovered signal drives the AGC block that controls the gain of the first stage when too strong signal is received.

This block (AGC) is a block at fast charge and slow discharge.

The detected information can be reshaped by connecting a suitable capacitor at pin 3 ; in such a way the carrier is integrated and the outputs become square wawes that can directly drive one microprocessor (avoiding a digital filter otherwise needed).

A voltage Regulator is also integrated, when you use a 5V of alimentation, this regulator is automatically disabled.

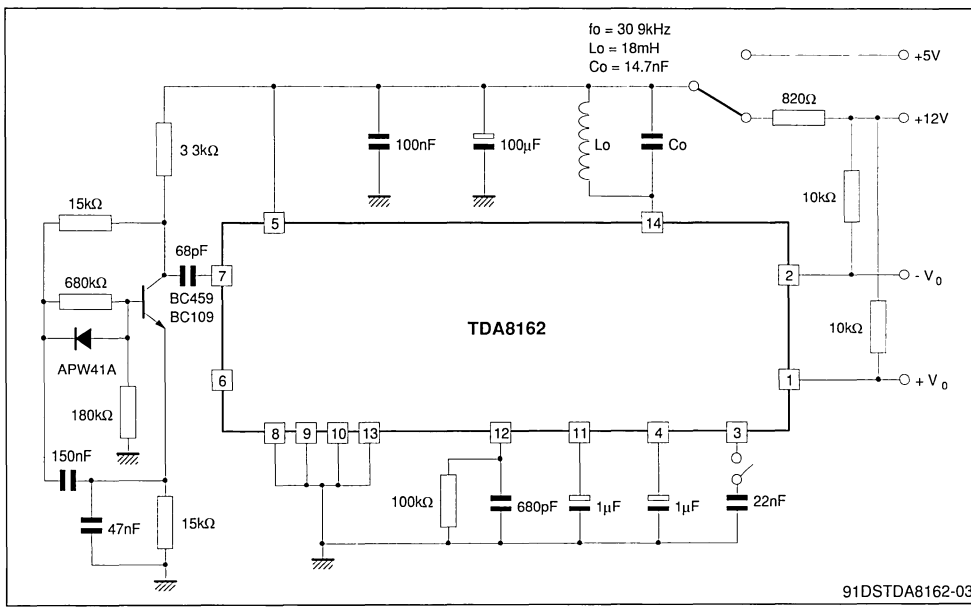
ELECTRICAL CHARACTERISTICS

Refer to the test circuit ; S1 to "a" ; V_{SS} = 12V ; V_S = 5V ; fo = 38.43kHz,
T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage	Applied between Pin 5 and 8	4	5	5.25	V
I_s	Supply Current (pin 5)	V_s = 5V V_i = 0V		4	8	mA
V_5	Stabilized Voltage at Pin 5	I_5 = 8mA S_1 to "b" ;		5.5		V
	First Stage Voltage Gain	Pin 4 to GND		30		dB
	2nd Stage Voltage Gain	V_{14} = 500mV$_{PP}$		50		dB
	2nd Stage Bandwidth	Co = 9.53nF Lo : L_S = 1.8mH ; R_S = 24.5Ω		2.2		kHz
	Input Voltage Sensitivity (pin 7)	For 500mV$_{PP}$ at Pin 14		100		μV$_{PP}$
	Input Current Sensitivity (pin 7)	For 500mV$_{PP}$ at Pin 14		1		nA$_{PP}$
	Input Impedance			100		kΩ
	AGC Range		80			dB
	Low Frequency Rejection at the Input Stage	C_1 = 2.2nF, f = 100Hz		30		dB
	Peak Detector Sensitivity (pin 12)	Full Swing at Pin 1 and at Pin 2		150		mV
	Noise Signal at Pin 14	V_{in} = 0		150		mV$_{PP}$
	Threshold Comparator			500		mV$_{PP}$

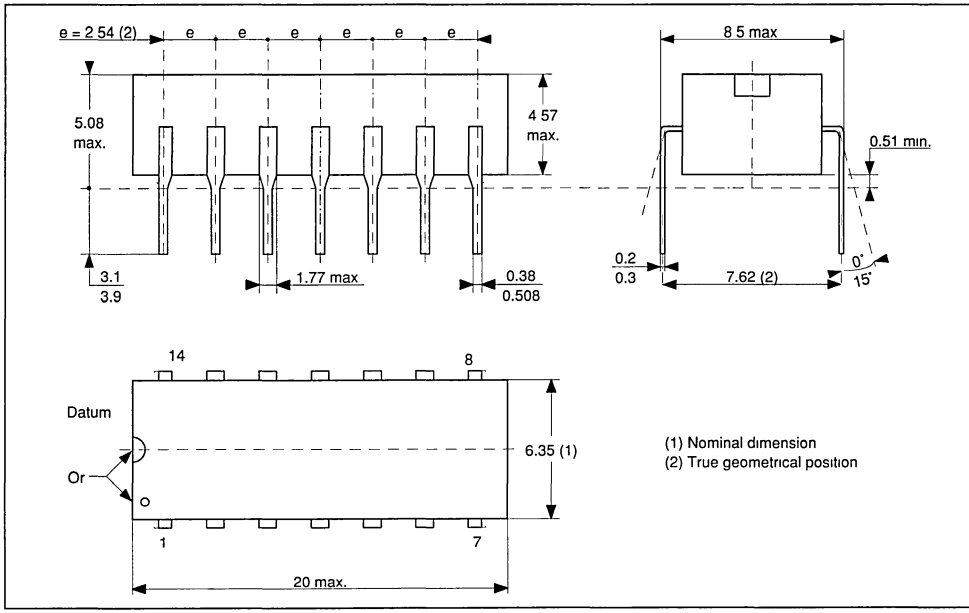
TAB-01

TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP

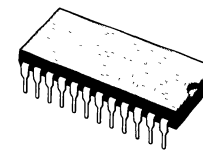


SGS-THOMSON MICROELECTRONICS

TDA8185I

HORIZONTAL AND VERTICAL PROCESSOR

- 503kHz REFERENCE OSCILLATOR
- 5.5V SUPPLY VOLTAGE INTERNALLY REGULATED
- VERY SOPHISTICATED SYNC. SEPARATOR
- COUNT DOWN TIMING LOGIC
- ADAPTS AUTOMATICALLY TO 625 LINE/50Hz AND 525 LINE/60Hz STANDARDS
- 50/60 Hz IDENTIFICATION OUTPUT
- AUTOMATIC VERTICAL AMPLITUDE CORRECTION 50/60Hz
- CRT PROTECTION CIRCUIT
- PHASE-CORRECTED HORIZONTAL OUTPUT WITH CONSTANT DUTY CYCLE



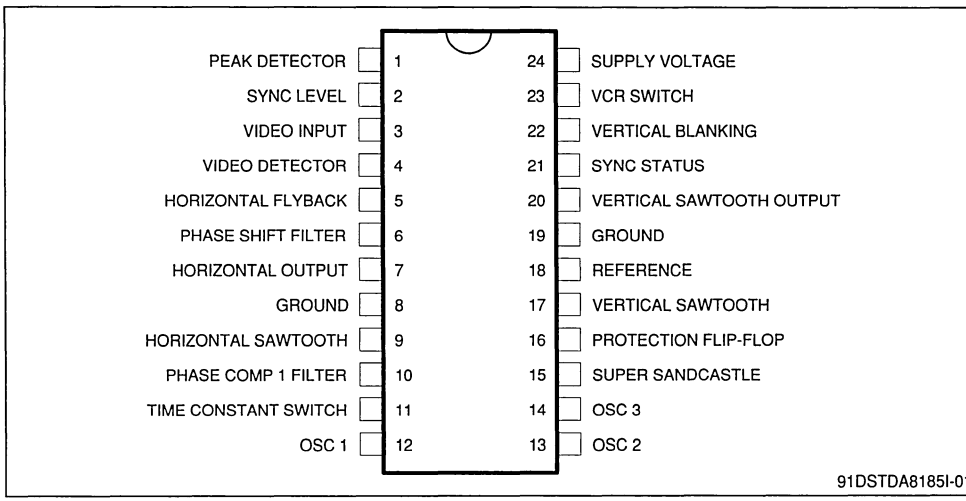
DIP24
(Plastic Package)

ORDER CODE : TDA8185I

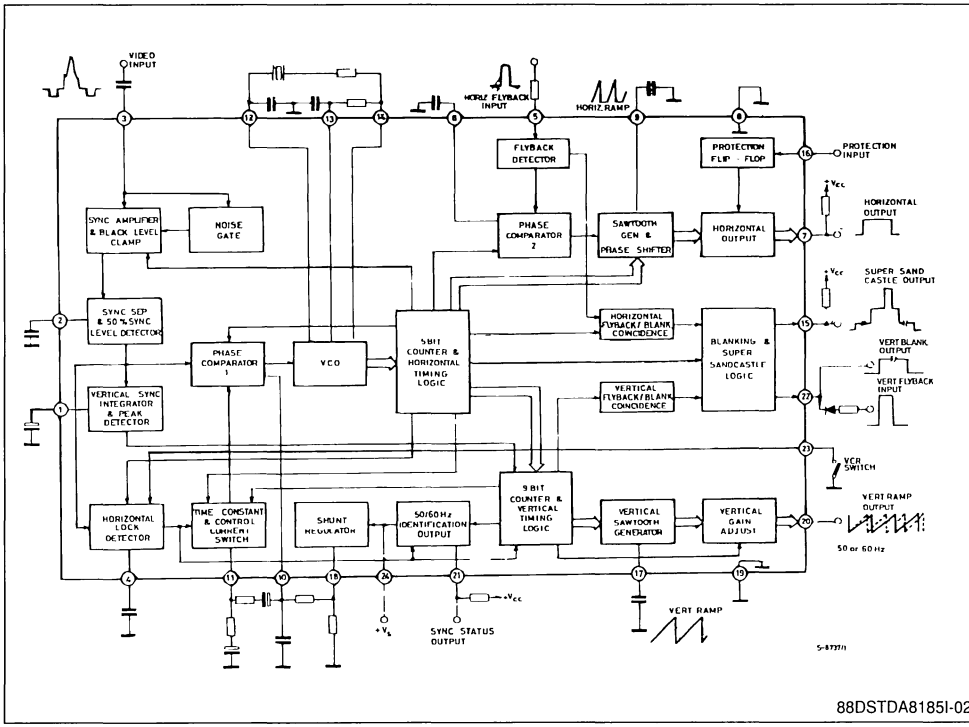
DESCRIPTION

The TDA8185I is a monolithic integrated circuit in 24 pins dual in line plastic package intended for TV signal processing and driving Horizontal and Vertical output stages. It was specially designed for VCR working conditions.

PIN CONNECTIONS (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 24 (low impedance)	5.25	V
V_{CC}	Voltage at Pins, 7, 15, 21	20	V
V_I	Input Signals	5	V
P_{tot}	Total Power Dissipation (T_{amb} = 70 °C)	1	W
T_j, T_{stg}	Storage and Junction Temperature	– 40 to 150	°C

TAB-01

THERMAL DATA

$R_{th\ j-pins}$	Thermal Resistance Junction-pins	Max	80	°C

TAB-02

ELECTRICAL CHARACTERISTICS

(V_S = 5 V, V_{CC} = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 24)		4.75	5	5.25	V
I_s	Supply Current (pin 24)		30	60	85	mA
V_{24}	Stabilized Voltage at Pin 24			5.6		V

TAB-03

ELECTRICAL CHARACTERISTICS (continued)
(V_S = 5 V, V_{CC} = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SYNC. SEPARATOR						
V_3	Peak to Peak Input Signal (negative video signal)		0.3	1	4	V
VIDEO IDENTIFICATION AND VCR SWITCH						
V_{23}	VCR Switch Voltage		1.6	2.1	2.4	V
V_4	Threshold Voltage for Time Constant Switching			2.3		V
I_4	Peak Output Current	Lock		1		mA
$-I_4$	Output Current			20		µA
OSCILLATOR						
F_O	Free Running Frequency			500		kHz
S_O	Frequency Control Sensitivity			1.0		kHz/V
V_{10}	Control Voltage Range			2.6 to 4		V
SYNC–OSCILLATOR PHASE COMPARATOR						
I_{10}	Control Peak Curent			± 0.3		mA
I_{10}	VCR Control Peak Current			± 0.6		mA
Δf	Catching and Holding Range			± 400		Hz
FLYBACK – OSCILLATOR PHASE COMPARATOR						
V_6	Control Voltage Range			2.8 to 3.7		V
I_5	Flyback Input Current		0.1			
	Flyback Input Threshold			5		mA
I_6	Peak Control Current			± 0.5		mA
	Static Control Error			1		%
t_d	Permissible Delay between Output Pulse and Flyback Pulse	$t_{flyback}$ = 12 µs		17		µs
COMPOSITE BLANKING AND KEY PULSE (supersandcastle)						
V_K	Key Pulse Output Peak Voltage			10		V
V_L	Line Blanking Voltage		4.25	4.5	4.75	V
V_F	Frame Blanking Voltage		2.38	2.5	2.63	V
t_{KS}	Phase Relationship between Leading Edge of Key Pulse and Middle of Sync. Pulse			2.5		µs
t_K	Key Pulse Duration			4		µs
t_F	Vertical Blanking Duration			1.4		ms
FRAME						
V_{20}	Output p.p. Sawtooth Voltage	50 Hz and 60 Hz		2.7		V
V_{20}	Pedestal Voltage			0.3		V
LINE						
I_7	Output Current			50		mA
V_7	Saturation Voltage	I_7 = 50 mA		0.4		V
t_L	Output Pulse Duration			29		µs
SYNC. STATUS OUTPUT						
V_{21}	Output Voltage	50 Hz 60 Hz Unlock	6.25	12 7	7.45 0.3	V V V

TAB-04

ELECTRICAL CHARACTERISTICS (continued)

(V_S = 5 V, V_{CC} = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OVERALL PHASE RELATIONSHIP						
t_O	Phase Difference between Middle of Flyback and Middle of Sync. Pulses			2		µs
VERTICAL BLANKING OUT AND FLY. INPUT						
V_{22}	Blanking Output Voltage			4		V
V_{22}	Flyback Threshold Input			5.7		V
I_{22}	Flyback Current Input		0.1			mA

Notes : 1. With t_{fly} = 12 µs and t_i = 29 µs.

2. The TDA8185 may be operated on a 5 V supply directly. A 5.5 V shunt regulator is available internally for operation on higher supply voltage ; in this case an external limiting resistor is required.
Without the external limiting resistor care must be taken to ensure that the supply voltage does not exceed 5.5 V or the regulator will intervene and the device could be damaged.

TAB-05

Figure 1 : Horizontal and Vertical Deflections for 30AX C.R.T.

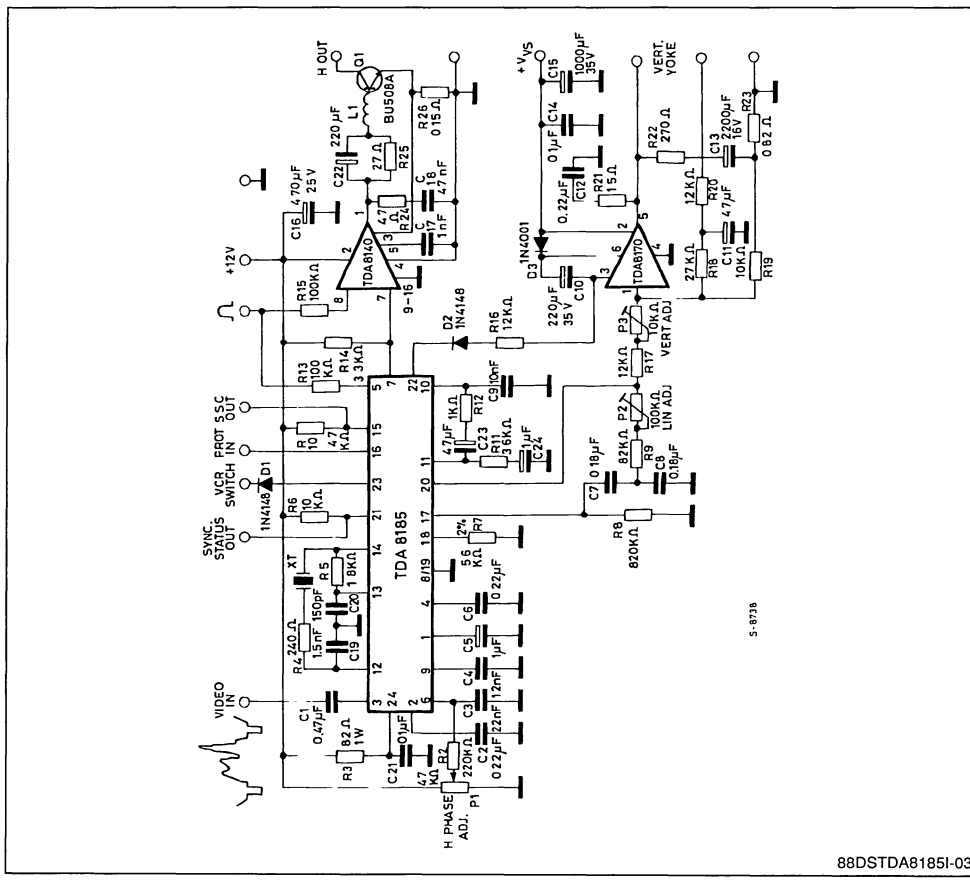


Figure 2 : Horizontal and Vertical Deflection for S4 C.R.T.

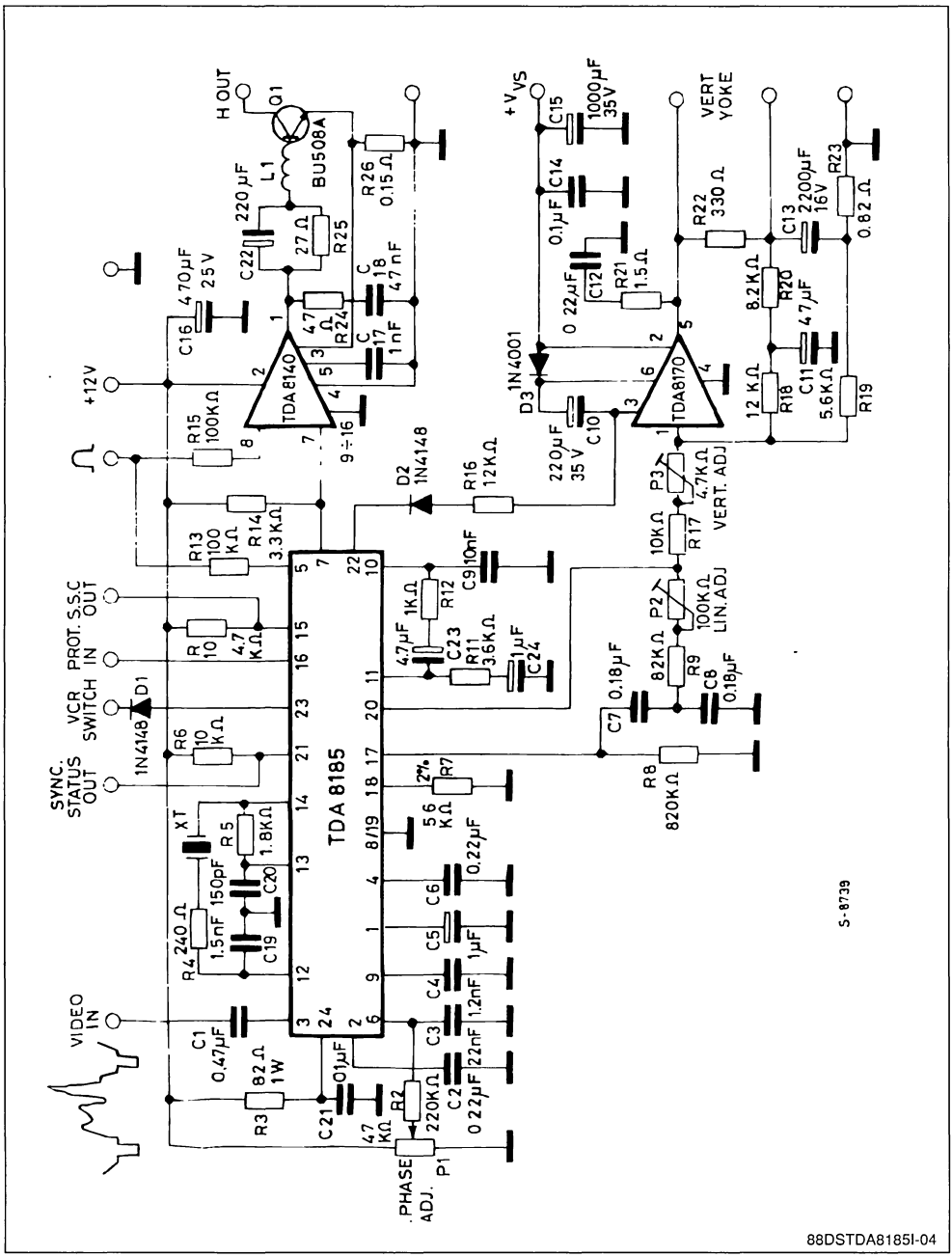
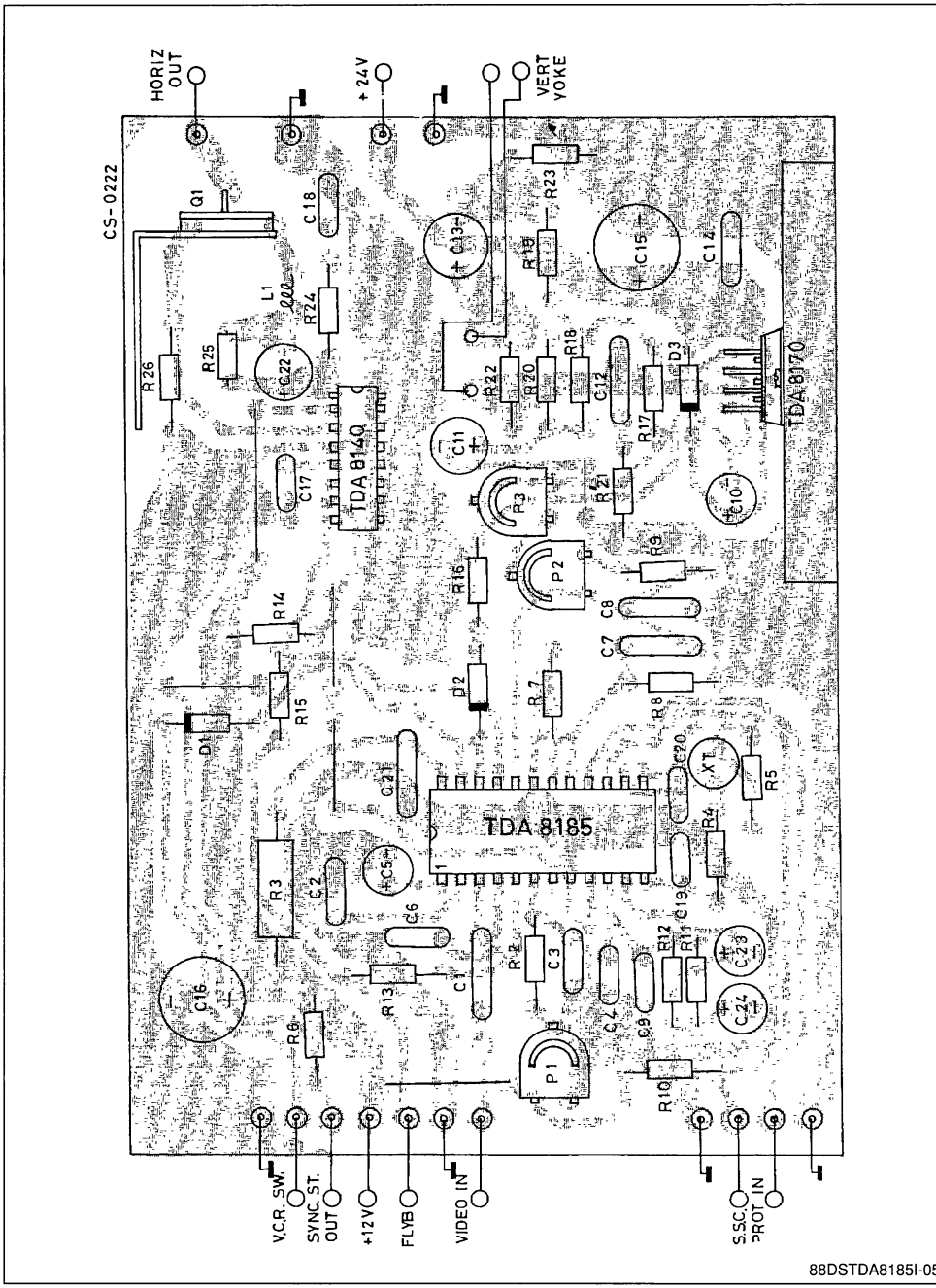
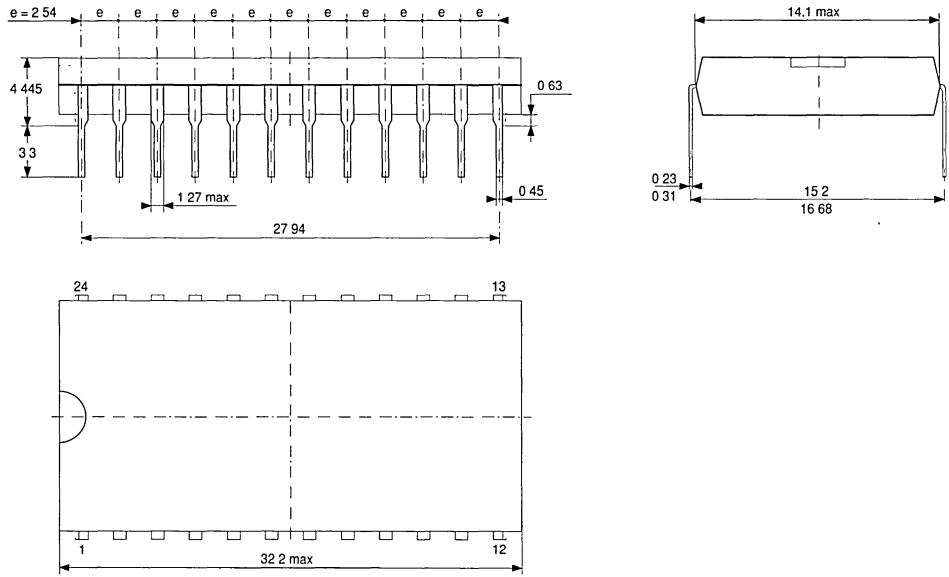


Figure 3 : P.C. Board and Components Layout of the Circuit of Fig. 2 (1:1 scale).



PACKAGE MECHANICAL DATA

24 PINS - PLATIC DIP

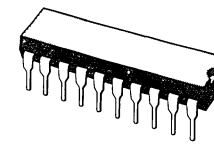


SGS-THOMSON MICROELECTRONICS

TDA8190

TV SOUND CHANNEL WITH DC CONTROLS

- SEPARATE VCR INPUT AND OUTPUT PINS
- 4W OUTPUT POWER INTO 16Ω
- NO SCREENING REQUIRED
- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- LOW DISTORTION
- DC TONE/VOLUME CONTROLS
- THERMAL PROTECTION



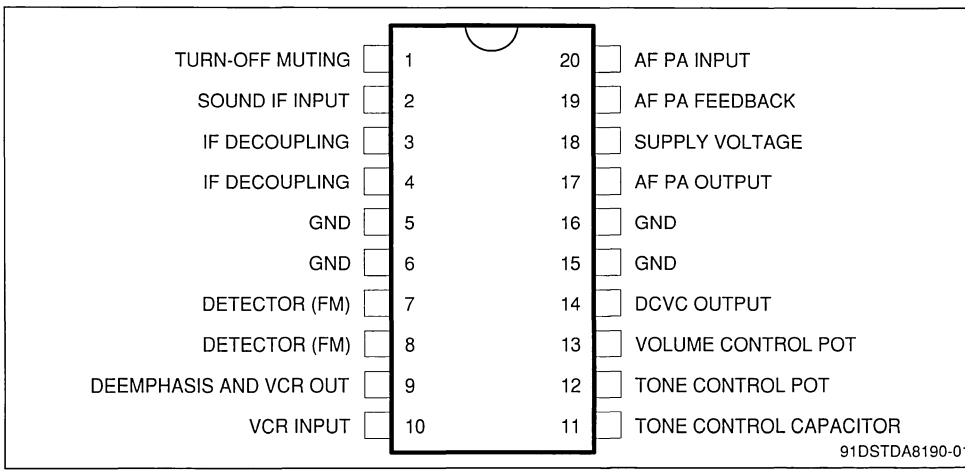
DIP20
(Plastic Package)

ORDER CODE : TDA8190

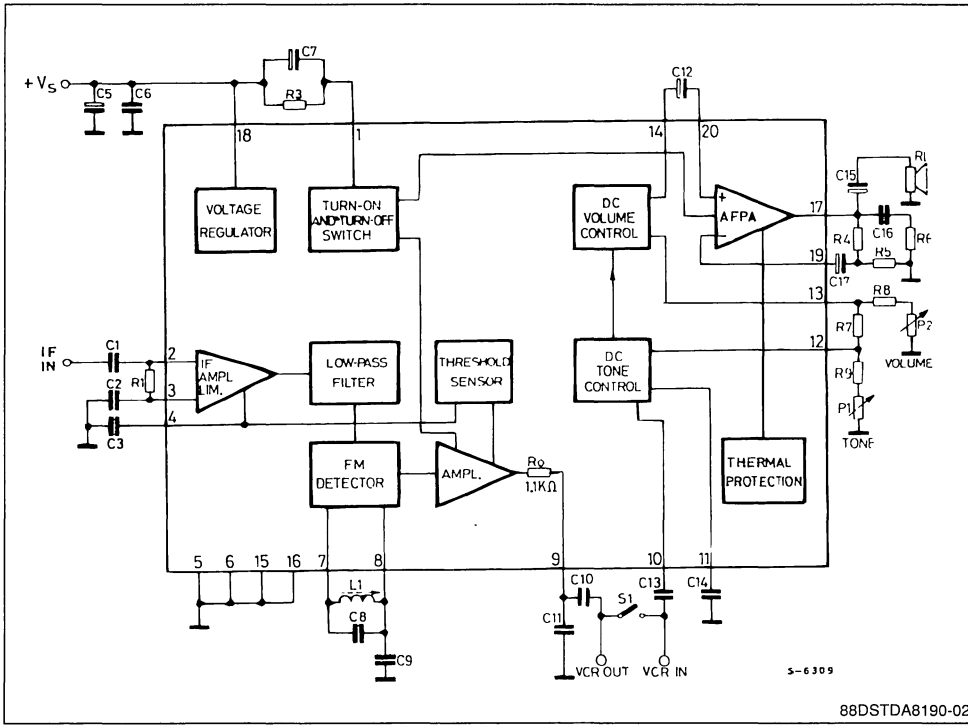
DESCRIPTION

The TDA8190 is a complete TV sound channel with DC tone and volume controls plus separate VCR input and output connections. Mounted in a Powerdip 16 + 2 + 2 package, the device delivers an output power of 4W into 16Ω (d = 10%, V_S = 24V) or 1.5W into 8Ω (d = 10%, V_S = 12V). Included in the TDA8190 are : IF amplifier limiter, active low-pass filter, AF pre-amplifier and power amplifier, turn-off muting, mute circuit and thermal protection. High output, high sensitivity, excellent AM rejection and low distortion make the device suitable for use in TVs of almost every type. Further, no screening is necessary because the device is free of radiation problems.

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 18)	28	V
V_I	Voltage at Pin 1	$\pm V_s$	
V_i	Input Voltage (pin 2)	1	V_{pp}
I_o	Output Peak Current (repetitive)	1.5	A
I_o	Output Peak Current (non repetitive)	2	A
I_4	Current (pin 4)	10	mA
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{stg} - T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j-pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W*

(*) Obtained with GND pins soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 24V, S1 : on, $\Delta f = \pm$ 25kHz, V_I = 1mV, P_1 = 12kΩ, f_o = 4.5MHz, f_m = 400Hz, T_{amb} = 25°C, unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
V_s	Supply Voltage (pin 18)	P_2 = 12kΩ	10.8		27	V
V_o	Quiescent Output Voltage (pin 17)	P_2 = 12kΩ	11	12	13	V
V_1	Pin 1 DC Voltage	P_2 = 12kΩ, R_1 = 270kΩ		5.3		V
V_4	Pin 4 DC Voltage	P_2 = 12kΩ		3.2		V
I_d	Quiescent Drain Current	P_2 = 12kΩ		32		mA
IF AMPLIFIER AND DETECTOR						
$V_{I\ (threshold)}$	Input Limiting Voltage at Pin 2 (–3dB)	V_o = 4 V_{rms}		50	100	μV
V_9	Recovered Audio Voltage (pin 9)	$\Delta f = \pm$ 7.5kHz, P_2 = 12kΩ	140	200	280	mV
AMR	Amplitude Modulation Rejection (*)	m = 0.3, V_I = 1mV, V_o = 4V_{RMS}		60		dB
R_I	Input Resistance (pin 2)	Δf = 0, P_2 = 12 kΩ		30		kΩ
C_I	Input Capacitance (pin 2)	Δf = 0, P_2 = 12 kΩ		6		pF
R_9	Deemphasis Resistance	C_1 = 68 to 888 nF	0.75	1.1	1.5	kΩ
DC VOLUME CONTROL						
K_V	Volume Attenuation (resistance control)	P_2 = 0 Ω P_2 = 4.3 kΩ P_2 = 12 kΩ	20	0 26 88	32	dB dB dB
V_C	Control Voltage	K = 0 dB K = 26 dB K = 88 dB		0 1.3 2.6		V V V
$\frac{\Delta K_V}{\Delta T_{pins}}$	Volume Attenuation Thermal Drift (resistance control)	T_{pins} = 25 to 85 °C P_2 = 4.3 kΩ		– 0.05		dB/°C
DC TONE CONTROL						
K_T	Tone Cut	S1 : Off V_{10} = 200 mV P_1 = 12 kΩ to 100 Ω f_{AF} = 10 kHz		14		dB
AUDIO FREQUENCY AMPLIFIER						
P_o	Output Power (d = 10 %)	V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω	3.5	4.1 1.5		W W
B	Frequency Response of Audio Amplifier (– 3 dB)	P_o = 1 W R_L = 16 Ω S1 : Off V_{10} = 200 mV V_o = 4 V_{RMS} @400 Hz	15	50		kHz
SVR	Supply Voltage Rejection	P_2 = 12kΩ Δf = 0 f_{ripple} = 120Hz		26		dB

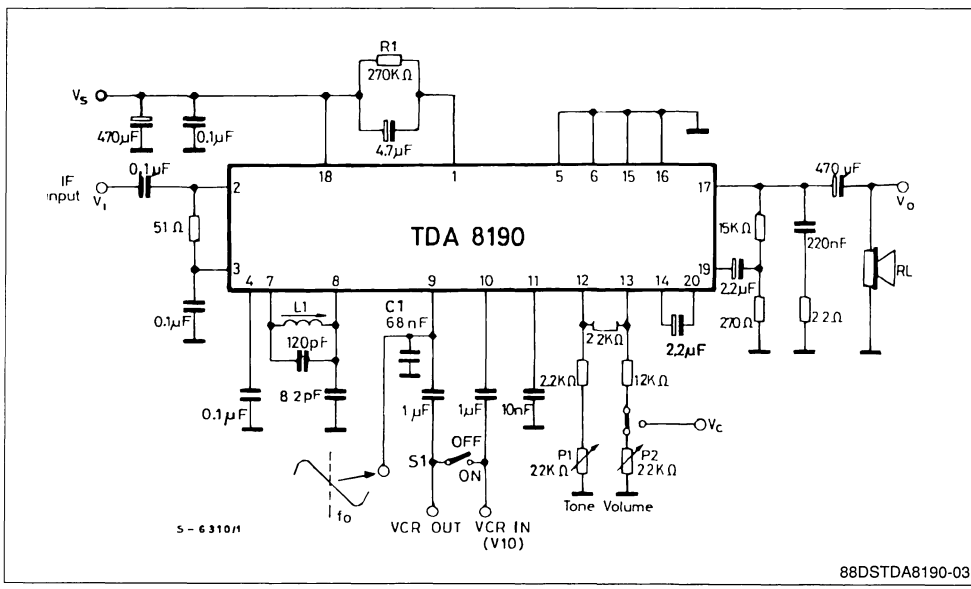
ELECTRICAL CHARACTERISTICS (continued)

(refer to the test circuit, V_S = 24V, S1 : on, $\Delta f = \pm$ 25kHz, V_I = 1mV, P_1 = 12kΩ, f_o = 4.5MHz, f_m = 400Hz, T_{amb} = 25°C, unless otherwise specified).

Symbol	Parameter	Test Conditions		Typ.	Max.	Unit	
V. C. R.							
d	Total Harmonic Distortion of pin 9 Output Signal	$\Delta f = \pm$ 7.5 kHz V_I = 1 mV			0.5		%
SVR	Supply Voltage Rejection at Output Pin 9	Δf = 0 P_2 = 12 kΩ	f_{ripple} = 120 Hz		66		dB
$\frac{S+N}{N}$	Signal to Noise Ratio at Output Pin 9	Δf = 25 kHz $V_I \geq$ 1 mV			70		dB
V_{10}	Input Voltage (playback)	V_o = 4 V_{rms}	P_2 = 0 S1 : Off	50	70	100	mV
R_{10}	Input Resistance (playback)		S1 : Off	10			kΩ
	Total Harmonic Distortion for 20 dB Overload of V_{10}	V_{10} = 1 V_{rms}	S1 : Off V_o = 4 V_{rms}		0.5	3	%
OVERALL CIRCUIT							
$\frac{S+N}{N}$	Signal to Noise Ratio (*)	$V_I \geq$ 1 mV Δf = 0	V_o = 4 V_{rms}		70		dB
d	Distortion (*)	P_o = 50 mW V_s = 24 V V_s = 12 V	$\Delta f = \pm$ 7.5 Hz R_L = 16 Ω R_L = 8 Ω		 0.5 0.5		 % %
M	Muting (*)	V_o = 4 V_{rms} @ no V_I ; V_I = 0		100			dB
Δf	Deviation Sensitivity	P_2 = 0	V_o = 4 V_{rms}		3	6	kHz

* Test Bandwidth = 20KHz.

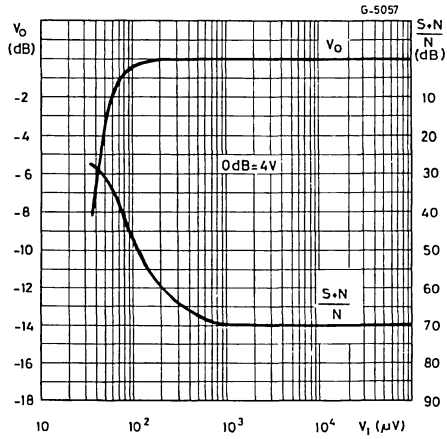
TEST CIRCUIT



TEST CONDITIONS (unless otherwise specified)

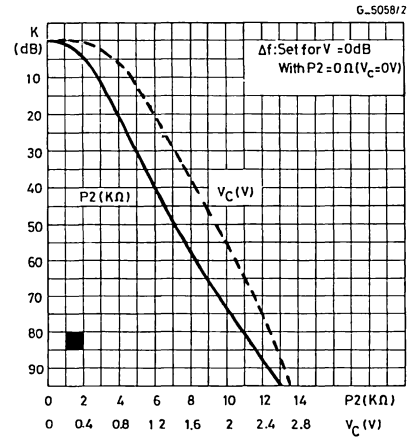
V_S = 24V ;	Q_o = 60 ;	f_o = 4.5MHz;
V_{in} = 1mV ;	f_m = 400Hz ;	$\Delta f = \pm$ 25KHz ;
P_1 = 12KΩ ;	$R_L = \infty$;	S1 = on ;

Figure 1 : Relative Audio Output Voltage and Output Noise vs. Input Signal.



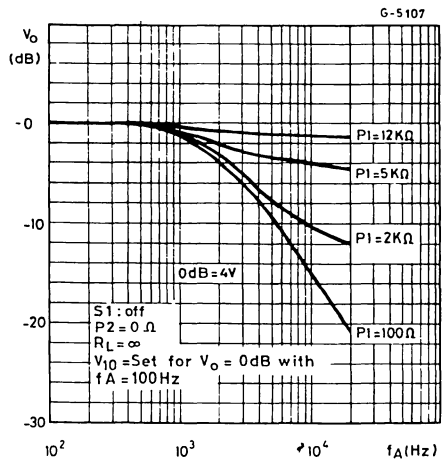
88DSTDA8190-04

Figure 2 : Output Voltage Alternation vs. DC Volume Control Resistance (a) or Vs. DC Volume Control Voltage (b).



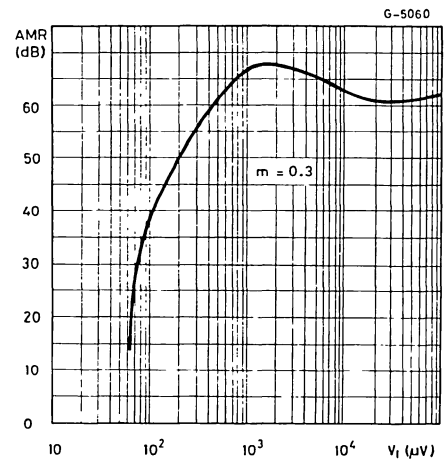
88DSTDA8190-05

Figure 3 : DC Tone Control Cut of the High Audio Frequencies for some Values of Resistance adjusted by P1.



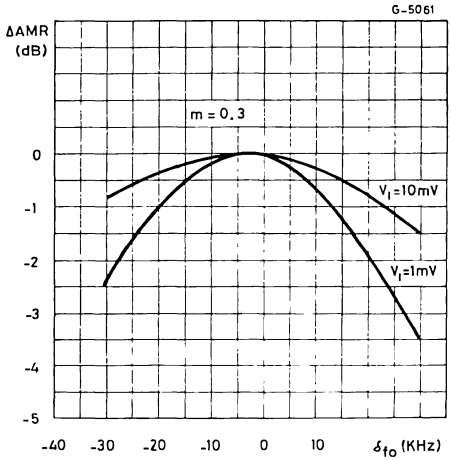
88DSTDA8190-06

Figure 4 : Amplitude Modulation Rejection vs. Input Signal.



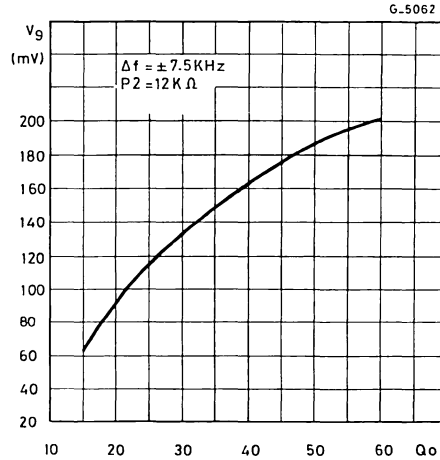
88DSTDA8190-07

Figure 5 : ΔAMR vs. Timing Frequency Change.



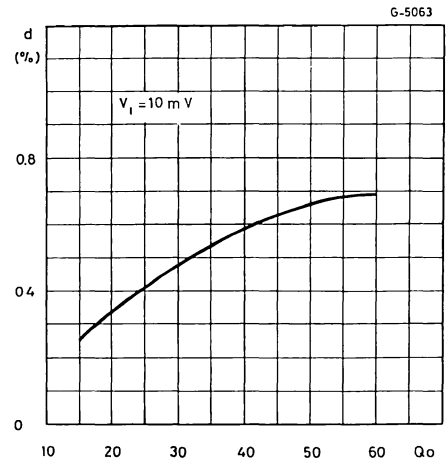
88DSTDA8190-08

Figure 6 : Recovered udio Voltage vs. Unloaded Q – factor of the Detector Coil.



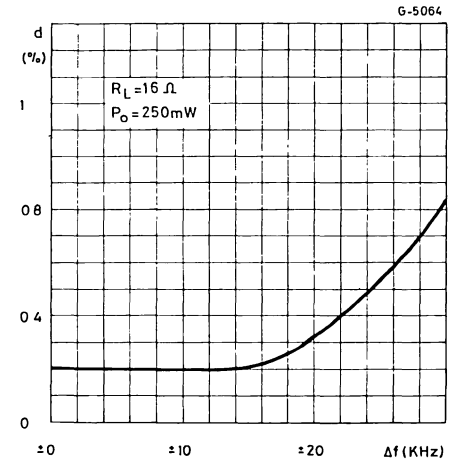
88DSTDA8190-09

Figure 7 : Distortion vs. Unloaded Q – factor of the Detector Coil.



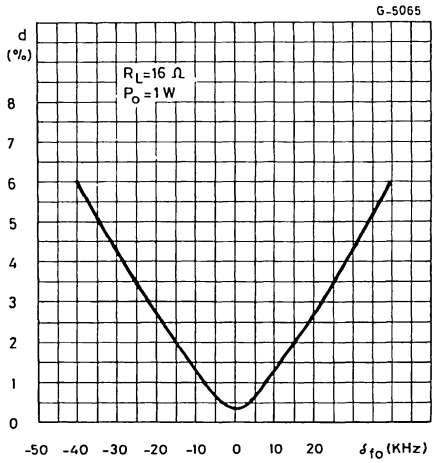
88DSTDA8190-10

Figure 8 : Distortion vs. Frequency Variation.



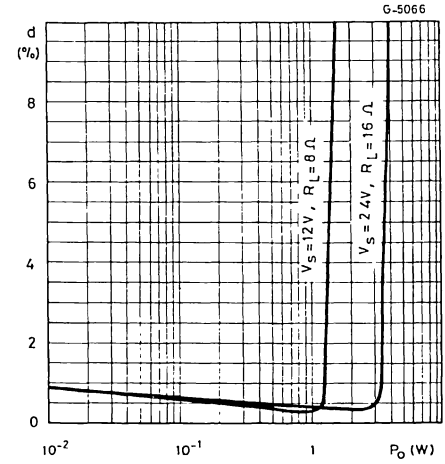
88DSTDA8190-11

Figure 9 : Distortion vs. Tuning Frequency Change.



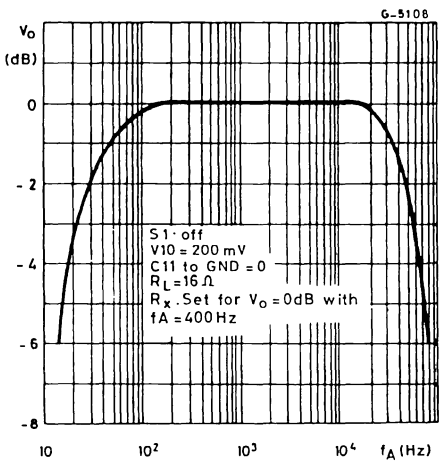
88DSTDA8190-12

Figure 10 : Distortion vs. Output Power.



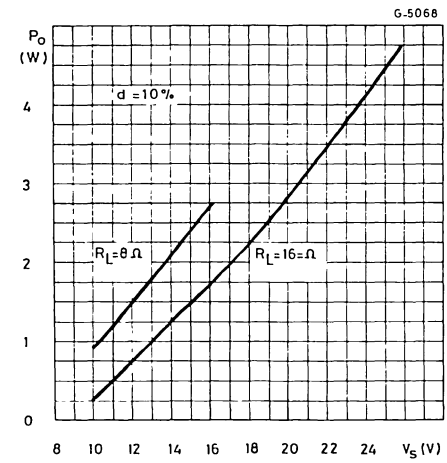
88DSTDA8190-13

Figure 11 : Audio Amplifier Frequency Response.



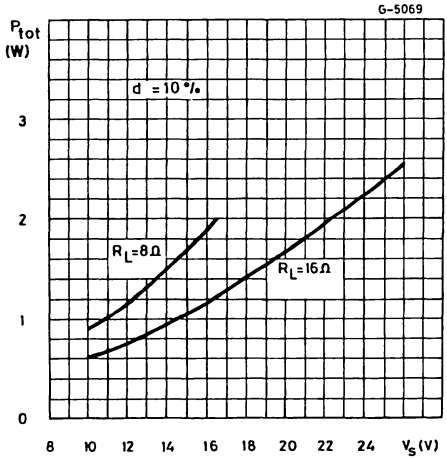
88DSTDA8190-14

Figure 12 : Output Power vs. Supply Voltage.



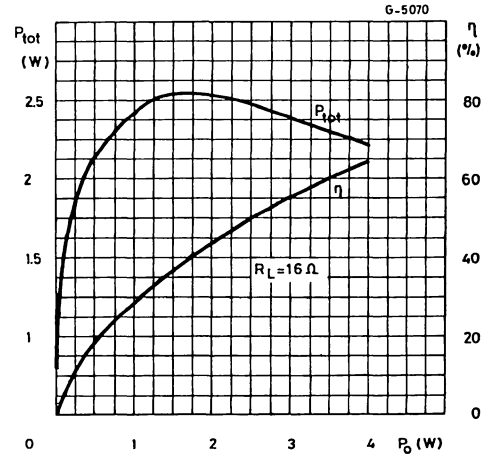
88DSTDA8190-15

Figure 13 : Power Dissipation vs. Supply Voltage(sine wave operation).



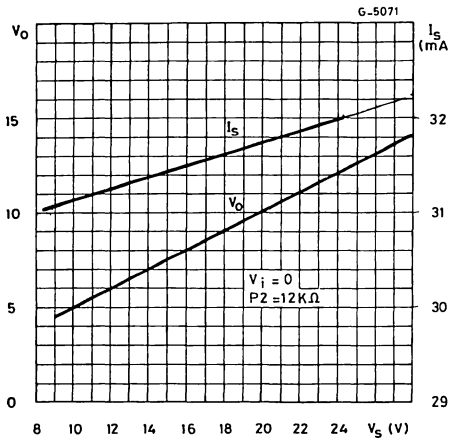
88DSTDA8190-16

Figure 14 : Power Dissipation and Efficiency vs. Output Power.



88DSTDA8190-17

Figure 15 : Quiescent Drain and Quiescent Output Voltage vs. Supply Voltage.



88DSTDA8190-18

APPLICATION INFORMATION (refer to the block diagram)

IF AMPLIFIER-LIMITER

It is made by six differential stages of 15dB gain each so that an open loop gain of 90dB is obtained.

While a unity DC gain is provided, the AC closed loop gain is internally fixed at 70dB that allows a typical input sensitivity of 50μV.

The differential output signal is single ended by a 20dB gain amplifier that through a buffer stage, feeds the detector system.

Internal diodes protect the inputs against overloads.

- Pin 2 is the IF non-inverting input
- Pin 3 is decoupled by a capacitor to open the AC loop
- Pin 4 grounded by a capacitor, allows a typical sensitivity of 50μV. (see VCR facility too).

LOW-PASS FILTER, FM DETECTOR AND AMPLIFIER

The IF signal is detected by converting the frequency modulation into amplitude modulation and then detecting it.

Since the available modulated signal is a square wave, a 40 dB/decade low-pass filter cuts its harmonics so that a sine wave can feed the two-resonances external network L1, C8 and C9.

This network defines the working frequency value, the amplitude of the recovered audio signal and its distortion at the highest frequency deviations.

The two resonances f1 (series resonance) and f2 (parallel resonance) can be computed respectively by :

$$X_{C9} = \frac{X_{L1} \cdot X_{C8}}{X_{L1} + X_{C8}} \quad \text{and } X_{L1} = X_{C8}$$

The ratio of these frequencies defines the peak-to-peak separation of the "S" curve :

$$\frac{f_2}{f_1} = \sqrt{1 + \frac{C_9}{C_8}}$$

A differential peak detector detects the audio frequency signal that amplified, reaches the deemphasis network R0 ; C11.

The AF amplifier can be muted (see turn-on and turn-off switch and VCR facility).

- Pin 7 is the output of the low-pass filter and one input of the differential peak detector
- Pin 8 is the other input of the differential peak detector
- Pin 9 is used to provide the required deemphasis time constant by grounding it with C11. At this pin, the internal impedance of which is typically of 1.1K, is available the recovered audio signal as auxiliary output.

DC TONE CONTROL

The same signal available or applied to pin 10, after a voltage to current converter, reaches, the DC Tone Control block. It operates, inside the 10KHz bandwidth, by cutting the high audio frequencies with a variable slope of an RC network, by means of P_1.

The maximum slope of the RC network is of 20dB per decade and its pole is defined by :

X_{C11} = 6.8K, typically.

Pin 11 - At this pin is tied the tone capacitor.

Pin 12 - Is the DC Tone Control input.

DC VOLUME CONTROL

After tone control regulation, the AF current signal reaches the DC volume control block that controls its intensity. The normal control, for which the block has been designed for a narrow spread, is produced by P2 ; however, without P2, a voltage control can be operated by forcing a voltage at pin 13 through R8.

- Pin 12, already seen as a DCTC input, is the reference voltage for the DCVC. Because of this, a small interface between tone and volume regulation can be expected.
- Pin 13 is the DC volume control input.
- Pin 14 after a current to voltage converter, the audio frequency signal comes out at this pin.

AUDIO FREQUENCY POWER AMPLIFIER AND THERMAL PROTECTION

Through C12 the signal reaches the amplifier non-inverting input. The closed loop gain is defined by the feedback at pin 19 (inverting input) or by the ratio :

$$G_v = 20 \text{ Log } \frac{R5 + R4}{R5} \quad \text{(dB)}$$

The amplifier, thermally protected, can supply 4W of power into a 16 load with 24V of supply voltage. The power output stage is a class B type.

- Pin 20 is the non-inverting input
- Pin 19 is the inverting input
- Pin 17 is the output of the AFPA.

TURN-ON AND TURN-OFF SWITCH

This block has been mainly designed to avoid, turning on the TV set, that transients, produced by the vision output, can reach the speaker.

Moreover this block, together an optimized rise time and full time of the supply voltage V_S, can avoid any pop generally produced during the turn-on and the turn-off transients.

Turninig on, pin 1 follows the supply voltage V_S by means of C7 ; a threshold is reached and the muting of the AFPA output (pin 17) is suddenly produced.

When V_S reaches it stop, C7 charges itself through the input impedance of pin 1 and the muting is removed with a time constant depending on the C7 value.

Turning off, the V_S trend, in series to the voltage V_S V_1 and which C7 is charged, drives pin 1 at a low level threshold and a sudden muting is produced again.

Since the turn-off can be operated with high output power, if the muting operates when the current through the inductance of the speaker is different from zero, a flyback is generated and then a small pop can be produced.

The flyback is clipped by integrated diodes.

The thresholds that produce the muting have been chosen in the way that 1 Vpp of ripple on the supply voltage does not produce any switching..

- Pin 1 is the turn-on and turn-off muting input.

SUPPLY

An integrated voltage regulator with different output levels, supplies all the blocks operating with small signal.

- Pin 18 is the main supply of the device.
- Pin 5 ; pin 6 ; pin 15 and pin 16 are the ground of the supply. These pins are used to drain out from the device the heat produced by the dissipated power.

Components	Units	Appl. 4.5 MHz	Appl. 5.5 MHz	Appl. 6 MHz
L1	µH	10 Q_o = 60	12 Q_o = 80	10 Q_o = 70
C5	pF	120	68	68
C4	pF	9	8.2	6.8
C8	nF	68	47	47
C. F		Murata SFE 4.5 MA	Murata SFE 5.5 MB	Murata SFE 6.0 MB
C1	pF	22	18	18
R2	Ω	1000	560	470
R3	Ω	1000	560	470

Figure 16 : Application Circuit.

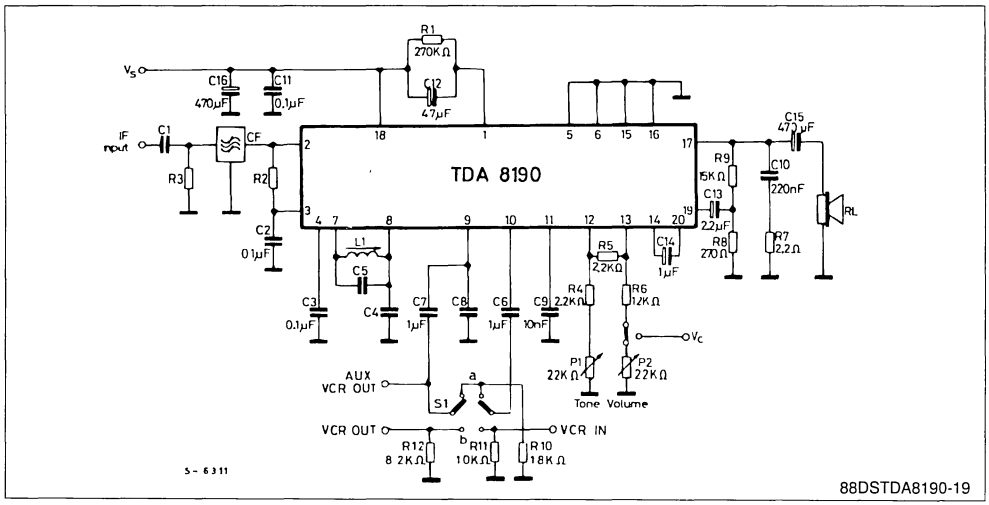
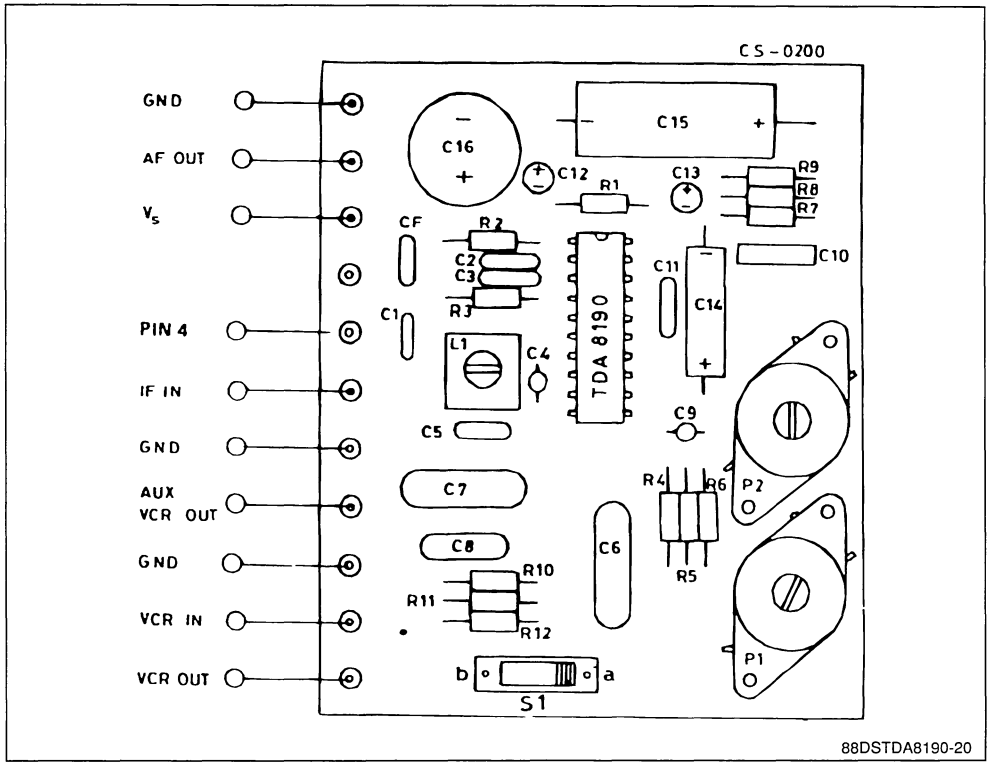


Figure 17 : PC Board and Components Layout of the Circuit of Fig. 16 (1 : 1 scale).

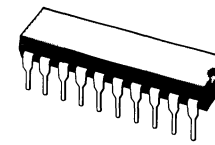


SGS-THOMSON MICROELECTRONICS

TDA8191

TV SOUND CHANNEL

- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- DC VOLUME CONTROL
- PERITELEVISION FACILITY
- 4W OUTPUT POWER
- LOW DISTORTION
- THERMAL PROTECTION
- TURN-ON AND TURN-OFF MUTING



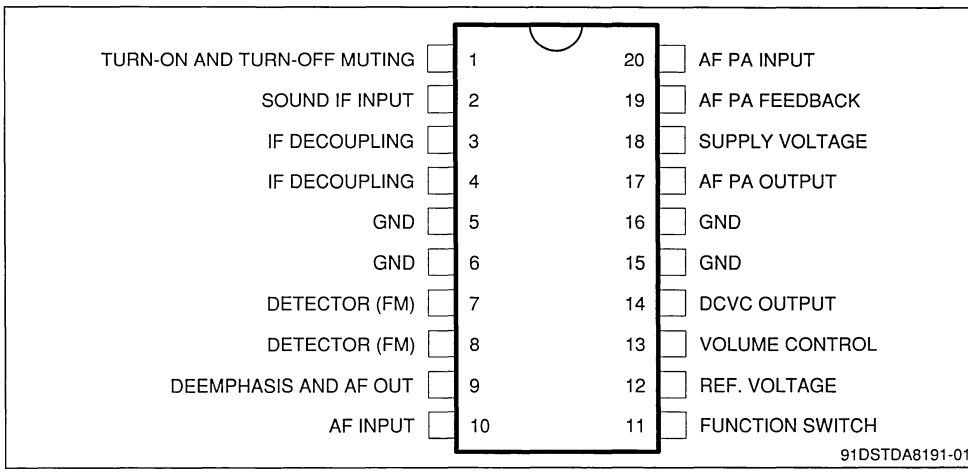
DIP20
(Plastic Package)

ORDER CODE : TDA8191

DESCRIPTION

The TDA8191 is a monolithic integrated circuit that includes all the functions needed for a complete TV sound channel. The TDA8191 is assembled in a 20 pin dual in line power package.

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	Supply Voltage (pin 18)	28	V
Vl	Voltage at Pin 1	± Vs	
Vi	Input Voltage (pin 2)	1	V_{PP}
Io	Output Peak Current (repetitive)	1.5	A
Io	Output Peak Current (non repetitive)	2	A
Ptot	Total Power Dissipation : at Tpins = 90°C at Tamb = 70°C	4.3 1	W W
Tstg, Tj	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ (j\text{-}pins)}$	Junction-pins Thermal Resistance	Max	14	°C/W
$R_{th\ (j\text{-}amb)}$	Junction-ambient Thermal Resistance	Max	80	°C/W

ELECTRICAL CHARACTERISTICS

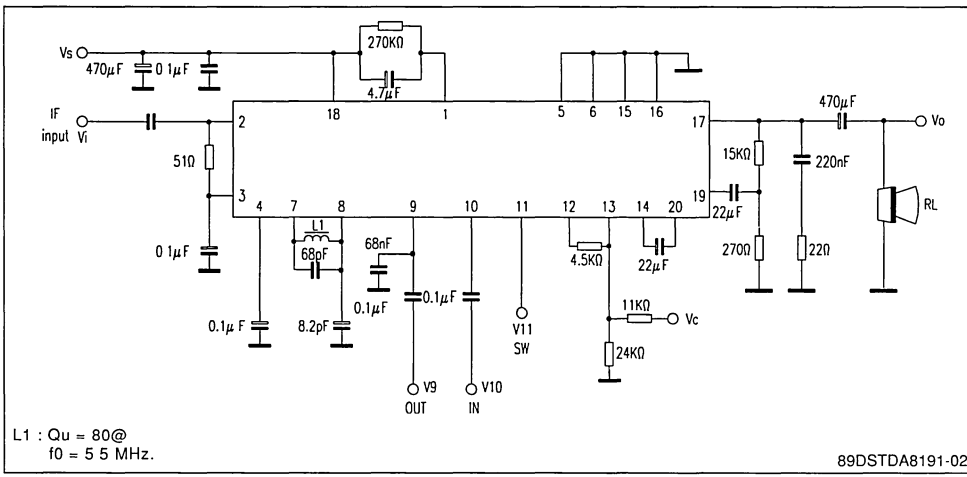
(Refer to fig. 1 ; V_S = 24V, R_L = 16Ω, pin 11 floating, Δf = ±50kHz, V_i = 1mV, f_o = 5.5MHz, f_m = 1kHz, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vs	Supply Voltage (pin 18)	Vc = 4.5V	10.8	24	27	V
Vo	Quiescent Output Voltage (pin 17)	Vc = 4.5V	11	12	13	V
V1	Pin 1 DC Voltage	Vc = 4.5V		5.3		V
Id	Quiescent Drain Current	Vc = 4.5V		35		mA
Vi	Input Limiting Voltage at Pin 2 (– 3dB)	Vo = $4V_{RMS}$		50	100	µV
V9	Recovered Audio Voltage (pin 9)	Vc = 4.5V Δf = ± 15KHz	200		400	mV_{RMS}
R9	Deemphasis Resistance	f = 20Hz to 20KHz	500	700	1000	Ω
AMR	Amplitude Modul. Rejection	m = 0.3 Vo = $4V_{RMS}$	45	60		dB
Ri	Input Resistance (pin 2)	Δf = 0		30		kΩ
Ci	Input Capacitance (pin 2)	Δf = 0 Vc =4.5V		6		pF
V12	DCVC Reference Voltage		5.6		6.2	V
Kv	Volume Attenuation	Vc = 0.5V ; Fig. 2 Vc = 4.5V ; Fig. 2	 80		1.0	dB dB
$\frac{\Delta K_V}{\Delta T_j}$	Volume Attenuation Thermal Drift	Tj = 300 to 380°K Fig. 3		– 0.05	– 0.1	dB/°C
Po	Output Power (d = 10%)		3.5	4		W
SVR	Supply Voltage Rej. (pin 17) (pin 9)	 Vc = 4.5V f_{ripple} = 100Hz	 20 50	 26 60		 dB dB
V11	Function Switch. - Television Broadc. Reproduction		 0		 2	 V
			or Pin 11 Floating			
	- Peritelevision Reproduction		8		12	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R11	Input Resistance		10			kΩ
V10	Input Voltage (d ≤ 2%)	Vo = $4V_{RMS}$; V11 = 12V		0.5	2.0	V_{RMS}
R10	Input Resistance	f = 20Hz to 20KHz	10			kΩ
CT	Crosstalk between Pins 9, 10		60			dB
$\frac{S+N}{N}$	Signal to Noise Ratio	Δf = 0 ; $V_O = 4V_{RMS}$	60	70		dB
d	Distortion (Po = 250mV)				2	%
Δf	Deviation Sens.	Vc = 0.5V ; Vo = $4V_{RMS}$		± 4	± 10	kHz

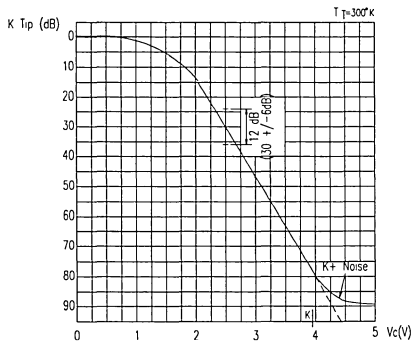
Figure 1 : Test Circuit.



L1 : Qu = 80@
f0 = 5 5 MHz.

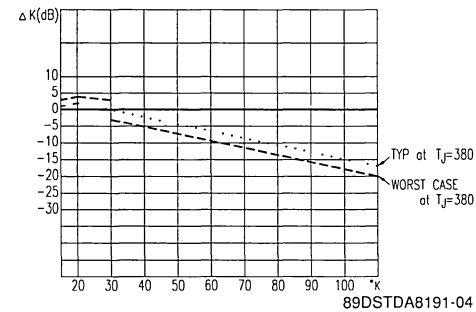
89DSTDA8191-02

Figure 2 : Volume Attenuation vs. DC Volume Control Voltage.



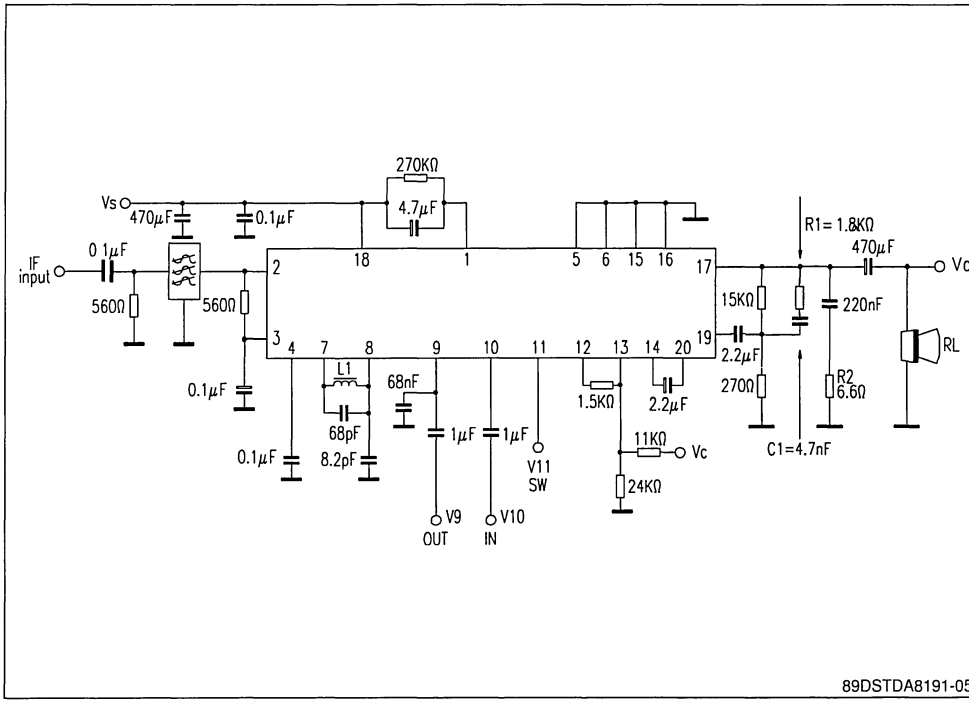
89DSTDA8191-03

Figure 3 : Volume Attenuation Thermal Drift.



89DSTDA8191-04

TYPICAL APPLICATION



L1 : Qu = 80e
fo = 5 5MHz

Figure 4 : AF Output Amplitude vs. AF Frequency by Using the Changes Shown on Fig. 4.

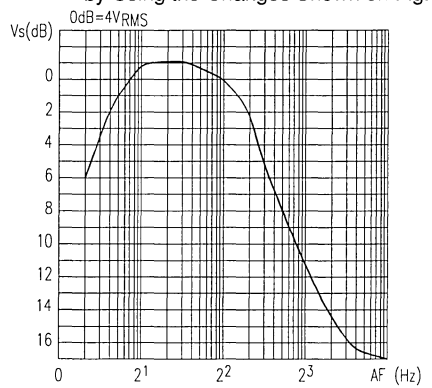


Figure 5 : Relative Audio Output Voltage and Output Noise vs. Input Signal.

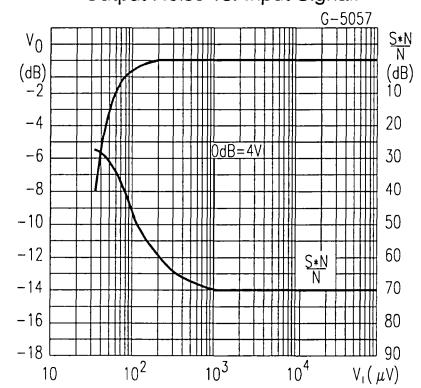
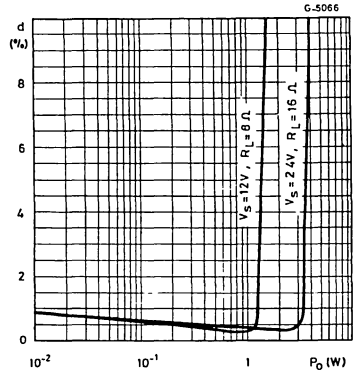
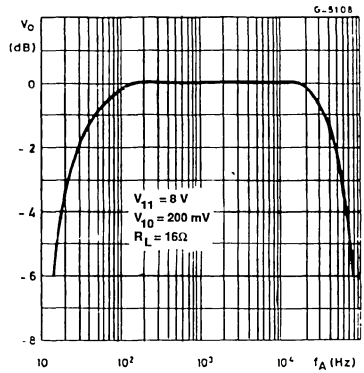


Figure 6 : Distortion vs. Output Power.



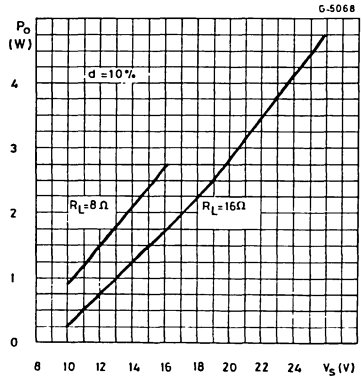
89DSTDA8191-08

Figure 7 : Audio Amplifier Frequency Response.



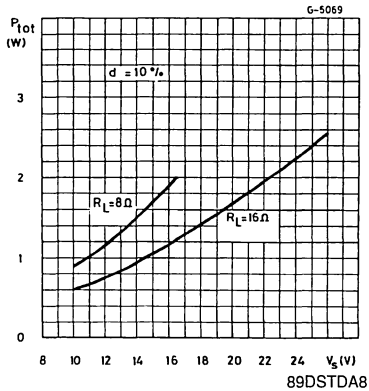
89DSTDA8191-09

Figure 8 : Output Power vs. Supply Voltage.



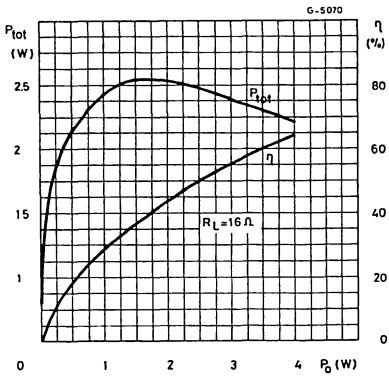
89DSTDA8191-10

Figure 9 : Power Dissipation vs. Supply Voltage (sine wave operation).



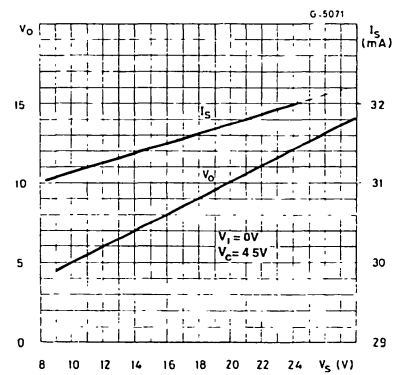
89DSTDA8191-11

Figure 10 : Power Dissipation and Efficiency vs. Output Power.



89DSTDA8191-12

Figure 11 : Quiescent Drain and Quiescent Output Voltage vs. Supply Voltage.



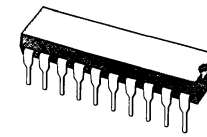
89DSTDA8191-13

MULTISTANDARD AM AND FM SOUND IF CIRCUIT FOR TV

The TDA8192 integrated circuit performs the following functions :

- A 2-STAGE GAIN CONTROLLED AMPLIFIER, PROVIDING COMPLETE IF GAIN ; (AM SECTION)
- A PEAK DETECTOR AND INTEGRATION WHICH PROVIDES AGC-VOLTAGE ; (AM SECTION)
- A 6-STAGE LIMITING AMPLIFIER FOLLOWED BY A SYNCHRONOUS DEMODULATOR AND DEEMPHASIS NETWORK ; (FM SECTION)
- AN AUDIO PREAMPLIFIER
- A CIRCUIT PROVIDING AM/FM SWITCHING AND MUTE FACILITIES
- AN EXTERNAL AUDIO INPUT CIRCUIT WITH SWITCHING FACILITIES TO DELIVER EITHER THE DEMODULATED IF, OR THE EXTERNAL AUDIO SIGNAL AT THE OUTPUT FULLY COMPATIBLE WITH THE SCART EUROPEAN NORM EN50 049
- A DC CONTROLLED VOLUME CIRCUIT

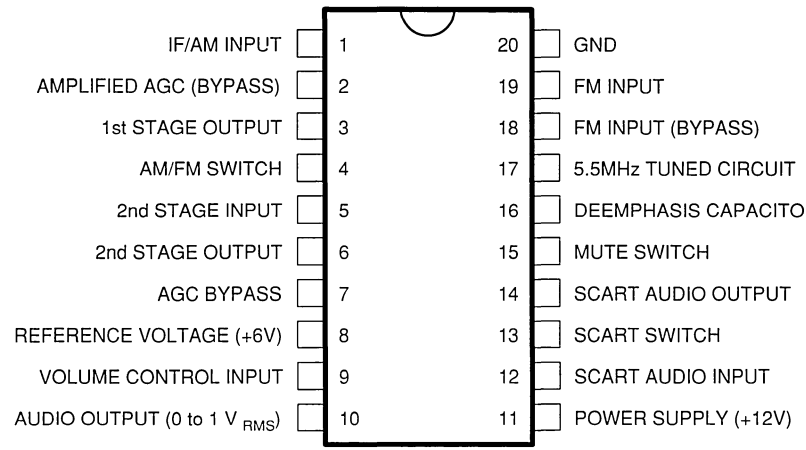
The demodulated IF signal is always available at a low impedance output.



DIP20
(Plastic Package)

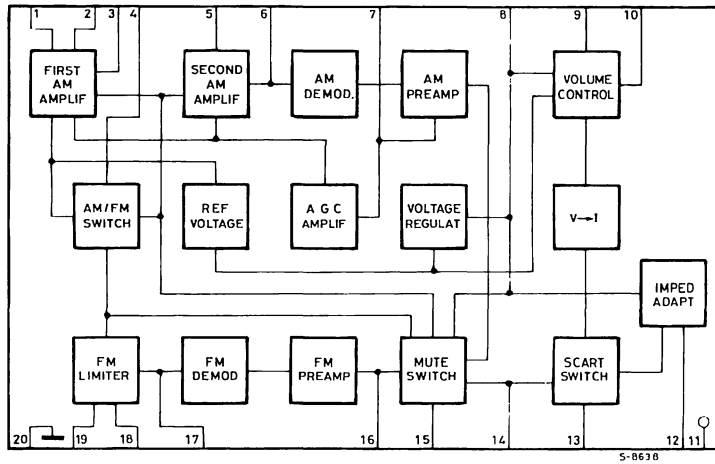
ORDER CODE : TDA8192

PIN CONNECTIONS



91DSTDA8192-01

BLOCK DIAGRAM



89DSTDA8192-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70°C$	800	mW
T_{op}	Operating Temperature	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 55 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 12V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		10.8	12	13.2	V
I_d	Current Drain	V_I = 0 AM FM		30 30		mA mA

AM SECTION (f_i = 39.2MHz, V_i = 1mV, m = 0.8, f_m = 1KHz unless otherwise specified)

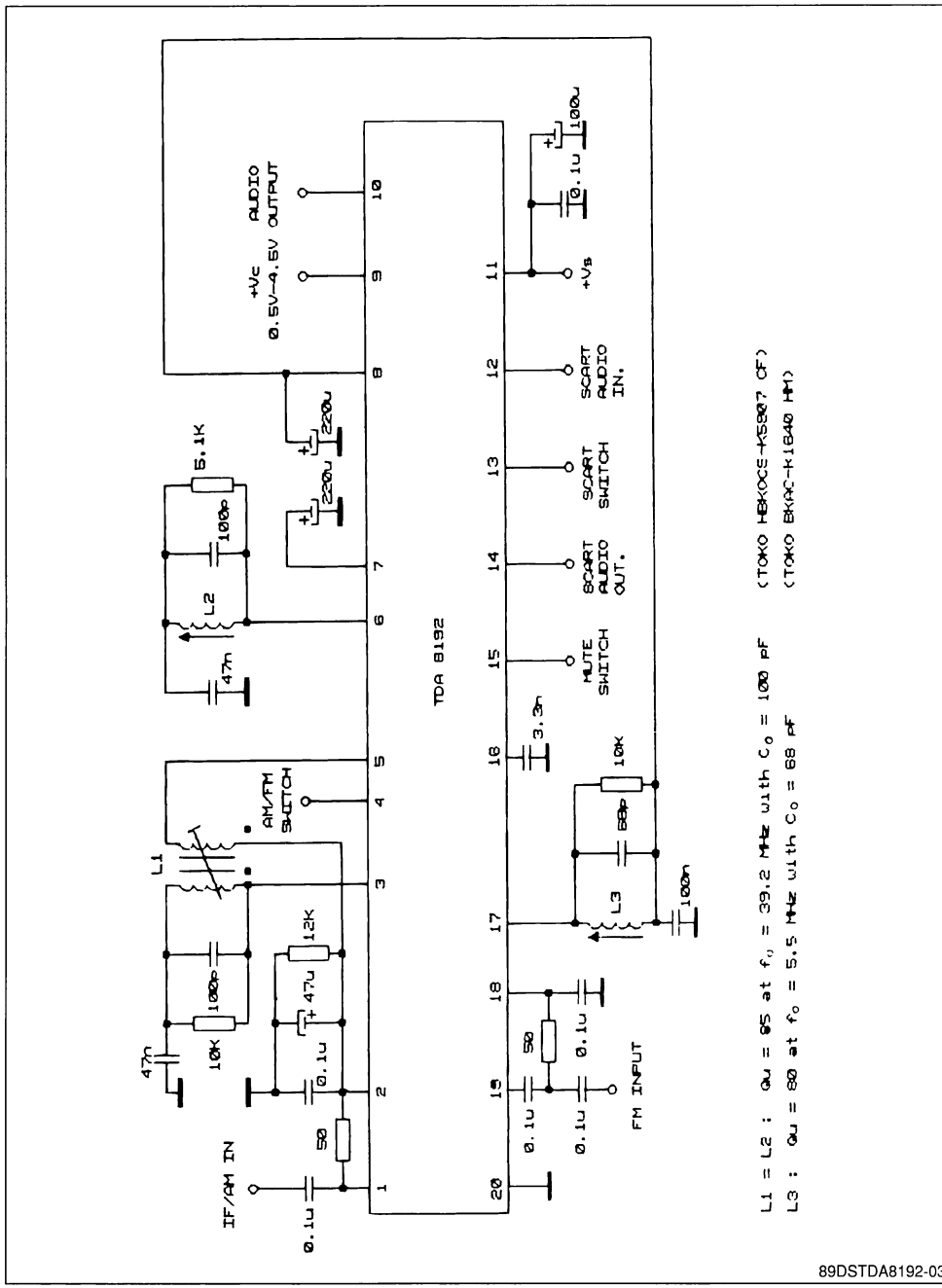
V_i	Input Sensitivity	S/N = 26dB		35		µV
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i = 0.1mV m = 0.3 V_i = 1mV V_i = 10mV	 50	36 50 56		dB
V_i	AGC Range	ΔV_{OUT} = – 1 to + 1dB		66		dB
V_o	Recovered Audio Signal			1		V
d	Distortion (1)				3	%
d	Distortion (2)				3	%

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 12V unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AM SECTION (f_i = 39.2MHz, V_i = 1mV, m = 0.8, f_m = 1KHz unless otherwise specified)						
R_i	Input Resistance between Pins 1 and 2	m = 0	2			kΩ
C_i	Input Capacitance between Pins 1 and 2	m = 0		18		pF
FM SECTION (f_i = 5.5MHz, V_i = 1mV, Δf = ± 50KHz, f_m = 1KHz, unless otherwise specified)						
V_i	Input Limiting Voltage	– 3dB Limiting Point		30		µV
AMR	Amplitude Modulation	V_i = 30mV m = 0.3		55		dB
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i = 1mV	60			dB
d	Distortion (3)				1.5	%
d	Distortion (4)			2		%
V_o	Recovered Audio Signal			1		V
R_i	Input Resistance	Δf = 0	2			kΩ
C_i	Input Capacitance	Δf = 0		14		pF
C_T	Crosstalk AM/FM			70		dB
AM/FM AND MUTE SWITCHING						
	FM "on" (pin. 4)		2.5		V_S	V
	AM "on" (pin 4)		0		0.8	V
	Mute "on" (pin 15)		0		1	V
	Mute "off" (pin 15)		5		V_S	V
	Signal Attenuation for Mute "off"		70			dB
	Mute Switch Current				50	µA
	AM/FM Switch Current		50		250	µA
SCART SWITCHING						
	Mode Selection Voltage : TV Selected (pin. 13)		0		5	V
	Mode Selection Voltage : Scart Selected (pin 13)		8		12	V
	Scart Switch Input Resistance		10			kΩ
	Scart Audio Input Amplitude (pin 12)			0.5	2	V_{rms}
	Crosstalk Between Switched Inputs (TV scart)			80		dB
DC VOLUME CONTROL						
	Audio Output Impedance (pin 10)				1	kΩ
	Control Range			90		dB
	Output/input Gain for Maximum Gain Control			0		dB
	Gain Control Voltage		0.5		4.5	V
	Noise Level (DIN 45405)			25		μV_{rms}

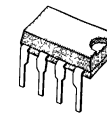
(1) 50% volume setting, V_i = 1mV
(2) 50% volume setting, V_i = 10mV
(3) V_i = 1mV, fm = 100 to 10.000Hz
(4) Vi = 1mV, ± 20KHz offset (detuning of phase shift filter).

TEST CIRCUIT



AUDIO SWITCH AND DC VOLUME CONTROL FOR TV

- TWO AUDIO INPUTS WITH SWITCHING FACILITIES FULLY COMPATIBLE WITH THE SCART EUROPEAN NORM EN 50049
- DC VOLUME CONTROL



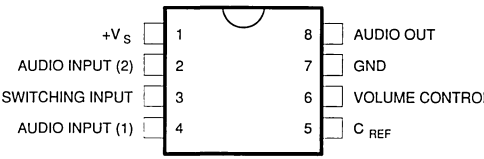
Minidip Plastic

ORDER CODE : TDA8196

DESCRIPTION

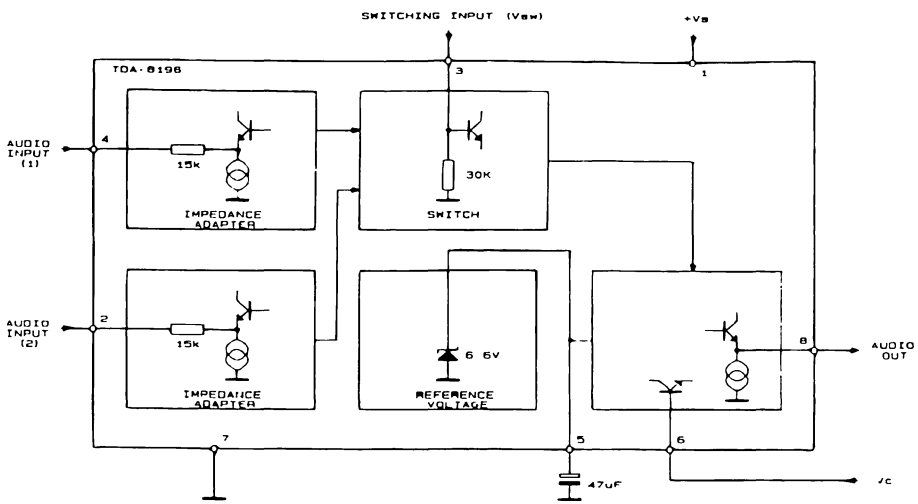
The TDA8196 is a monolithic integrated circuit in DIP8 package intended for TV applications.

PIN CONNECTION (top view)



91DSTDA8196-01

BLOCK DIAGRAM



89DSTDA8196-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 1)	16	V
T_{stg}, T_j	Storage and Junction Temperature	– 55 to 125	°C
T_{amb}	Operating Ambient Temperature	0 to 70	°C

TAB-01

THERMAL DATA

$R_{th j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200	°C/W

TAB-02

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 12V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	1		10.8	12	13.2	V
I_S	Supply Current	1	V_I = 0, V_C = 0.5V		12		mA
V_R	Reference Voltage	5			6.6		V
V_{SW}	Switching Voltage Audio Input 1 Audio Input 2	3		 0 8		 5 12	 V V
R_{SW}	Switching Input Resistance	3	V_{SW} = 12V	20	30		kΩ
C_{SW}	Switching Input Capacitance	3				10	pF
C_t	Crosstalk between Switched Inputs		Selective Volmeter (B_W = 8Hz), see Fig.1	70	90		dB
V_I	Audio Input Amplitude (1 or 2)	4 2			0.5	2	V_{RMS}
R_I	Audio Input Resistance (1 or 2)	4 2		 10	 13		 kΩ
K_{min}	Output / Input Gain for Max Vol				0		dB
R_O	Audio Output Resistance	8			0.2	1	kΩ
K_V	Attenuation Range		Selective Volmeter (B_W = 8Hz), see Fig.2	70	90		dB
V_C	Control Voltage Range $K_V = K_{MAX}$ (Vol. min) $K_V = K_{MIN}$ (Vol. max)	6			 0.5 4.5		 V V
THD	Distortion	8	V_I = 2 V_{RMS} @ V_C = 4.5V		0.4	1	%
En	Output Noise Level	8	DIN45405 V_C = 0.5V Weighted		 40		 μV_{RMS}
En	Output Noise Level	8	DIN45405 V_C = 4.5V Weighted		 120		 μV_{RMS}
$\frac{K_V}{\Delta T_a}$	Vol. Attenuation Thermal Drift		T_{amb} = 0 to 70°C K_V = 30dB, see Fig.3		 0.04		 dB/°C
SVR	Supply Voltage Rejection	8	V_C = 0.5V, f = 100Hz V_{ripple} = 1V_{PP} Selective Volmeter (B_W = 8Hz), see Fig.4 and 5		 38		 dB
V_O	Output DC Shift	8	V_C = 0.5 + 4.5V, V_I = 2 V_{RMS}		0.25		V

TEST CIRCUIT

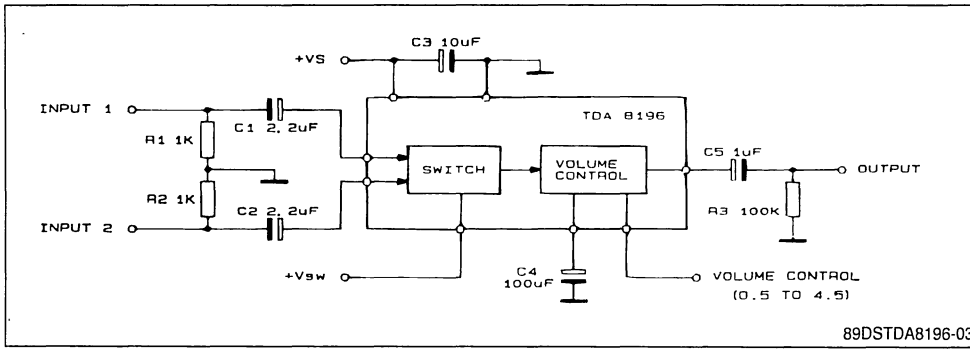
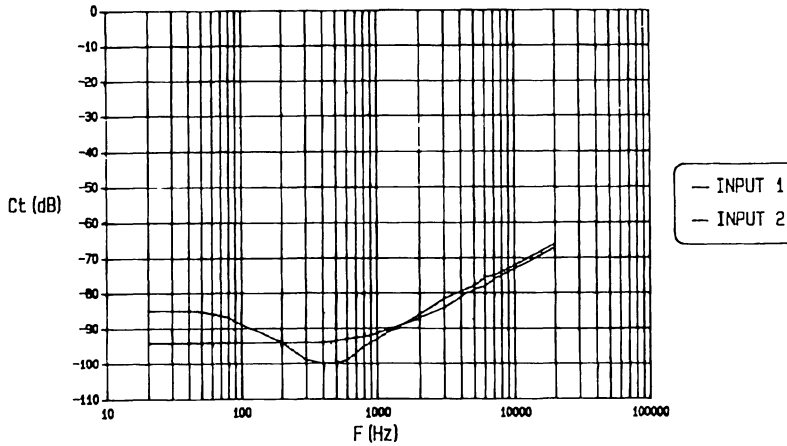
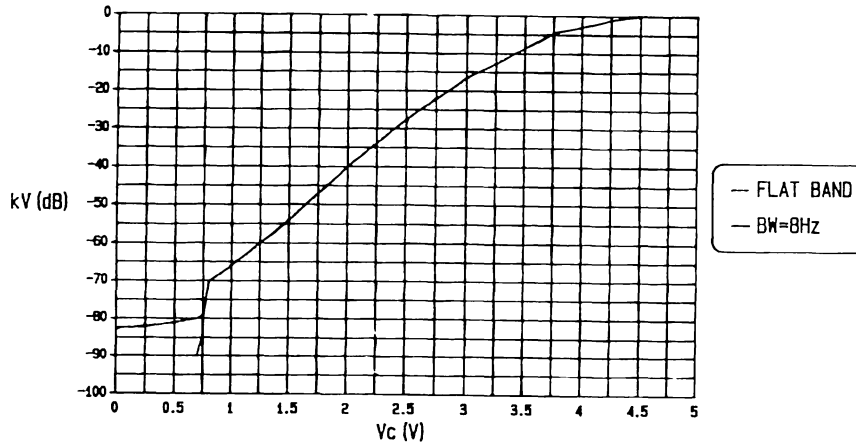


Figure 1 : TDA8196 Crosstalk.



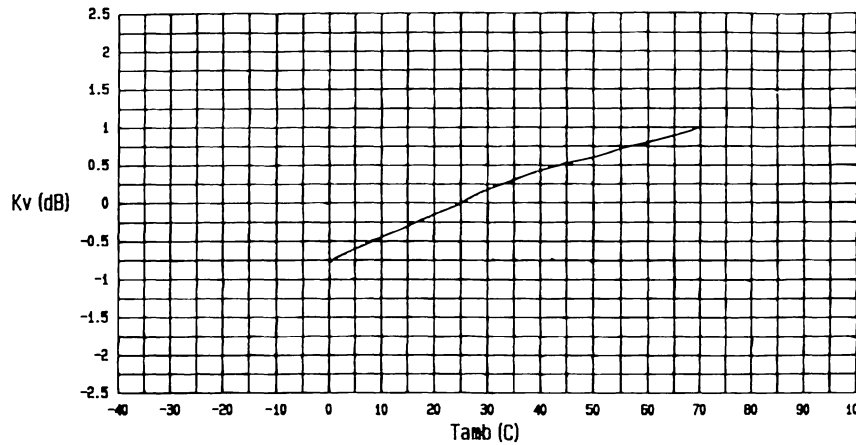
89DSTDA8196-04

Figure 2 : Output Attenuation versus DC Volume Control Voltage.



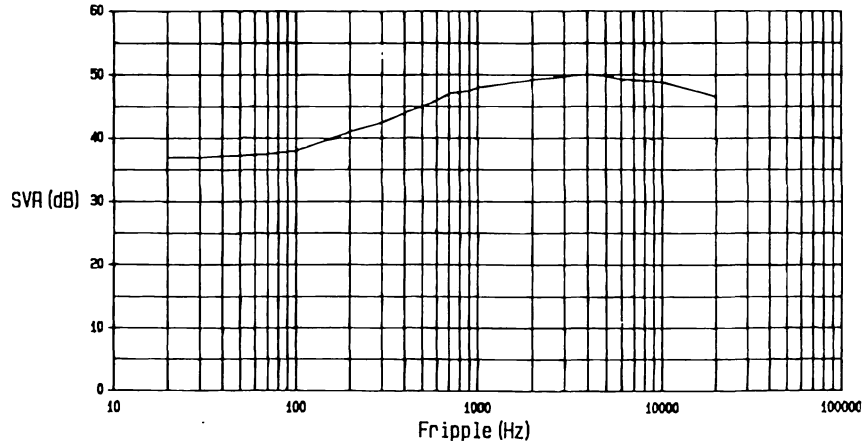
89DSTDA8196-05

Figure 3 : K_v Drift vs. T_{amb} Variation.



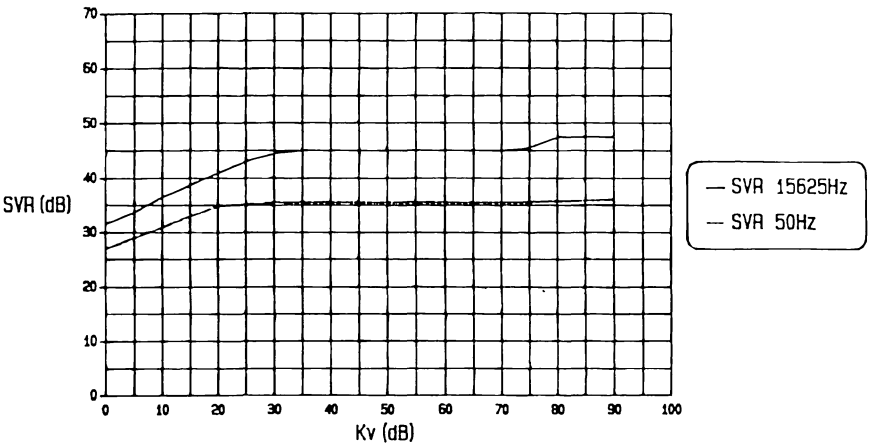
89DSTDA8196-06

Figure 4 : SVR vs. Ripple Frequency.



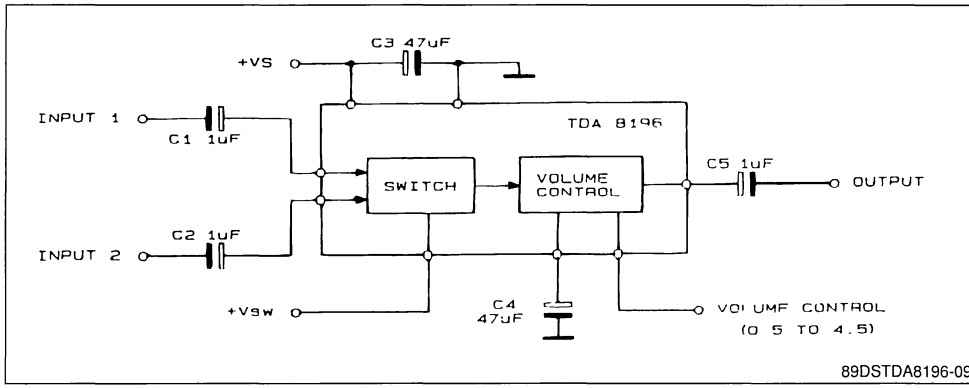
89DSTDA8196-07

Figure 5 : SVR vs. Volume Attenuation.



89DSTDA8196-08

APPLICATION CIRCUIT



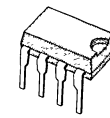
SGS-THOMSON MICROELECTRONICS

TDA8199

STEREO AMPLIFIER AND DC VOLUME CONTROL FOR TV

ADVANCE DATA

- STEREO CIRCUIT
- DC VOLUME CONTROL
- 12dB MAXIMUM GAIN



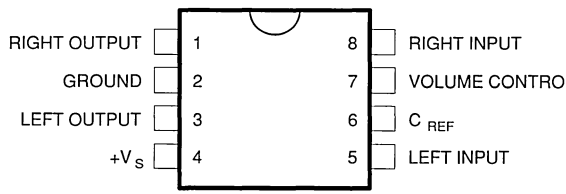
Minidip Plastic

ORDER CODE : TDA8199

DESCRIPTION

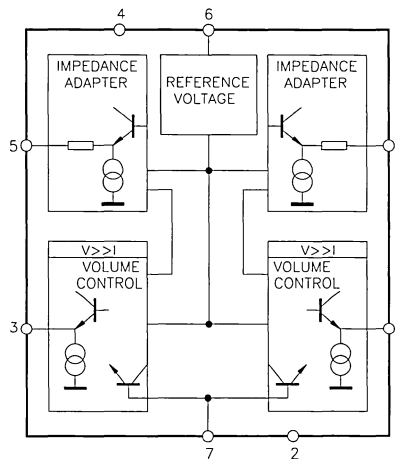
The TDA8199 is a monolithic integrated circuit in DIP8 package intented for TV applications.

PIN CONNECTIONS



91DSTDA8199-01

BLOCK DIAGRAM



91DSTDA8199-02

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

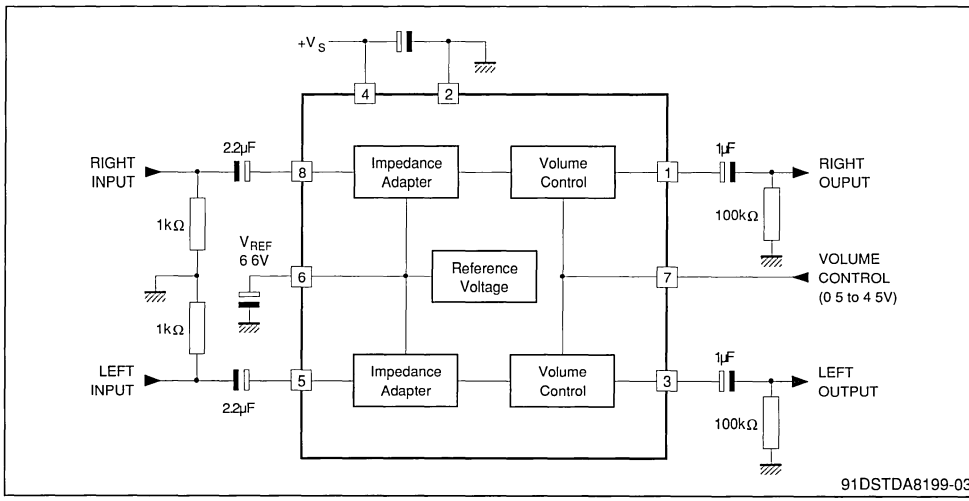
Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
T_{STG}	Storage Temperature	-55 to +125	°C
T_{OP}	Operating Ambient Temperature	0 to +70	°C

ELECTRICAL CHARACTERISTICS

Measured according to the following conditions, unless otherwise specified : T_{AMB} = 25°C, V_S = +12V.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	10.8	12	13.2	V
I_S	Supply Current (V_{IN} = 0, V_C = 0.5V)		17		mA
V_R	Reference Voltage	6.5	6.9		V
V_I	Audio Input Amplitude		0.125	0.5	V_{RMS}
THD	Distortion for V_I = 2V at Maximum Volume		0.35	1	%
C_C	Crosstalk between Channels		70		dB
R_I	Audio Input Resistance		22		kΩ
R_O	Audio Output Resistance		0.3	1	kΩ
ΔK	Attenuation Range	70	85		dB
K_{MAX}	Output/Input Gain for Maximum Volume		12		dB
V_C	Voltage Control Range volume minimum volume maximum	 4.5		 0.5	V
OUTPUT	Noise Level (DIN45 405) @ V_7 = 4.5V weighted		 300		μV_{RMS}
$\frac{\Delta K}{\Delta T}$	Volume thermal stability (K = - 30dB, 0 < T_{AMB} < 60°C)		0.04		dB/°C

APPLICATION DIAGRAM



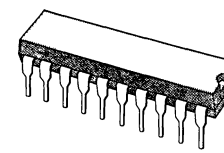
SGS-THOMSON MICROELECTRONICS

TDA8213

VIDEO & SOUND IF SYSTEM

ADVANCE DATA

- VERY LOW CURRENT ABSORPTION
- 3 STAGE IF GAIN CONTROLLED AMPLIFIER
- SYNCHRONOUS VIDEO DEMODULATOR
- WHITE SPOT AND NOISE INVERTER
- AGC CIRCUIT WITH NOISE GATING
- TUNER AGC OUTPUT FOR PNP TUNERS
- FM DETECTOR
- AF AMPLIFIER WITH DC VOLUME CONTROL
- AFC
- 2 V_{PP} ON VIDEO OUTPUT



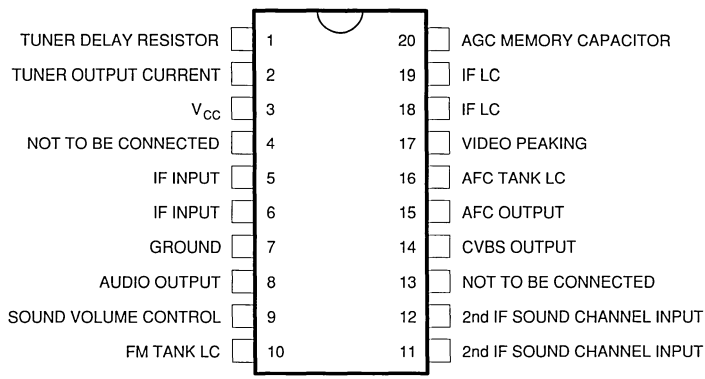
DIP20
(Plastic Package)

ORDER CODE : TDA8213

DESCRIPTION

The TDA8213 is a monolithic integrated circuit in DIP20 package for colour and black & white television receivers using PNP tuners. It is intended to operate with a negatively modulated vision carrier and frequency modulated sound carrier. Used with TDA8214/15 (H/V deflection circuit) and TDA8217 (Pal decoder and video processor), this IC permits a complete low-cost solution for PAL applications.

PIN CONNECTIONS



91DSTDA8213-01

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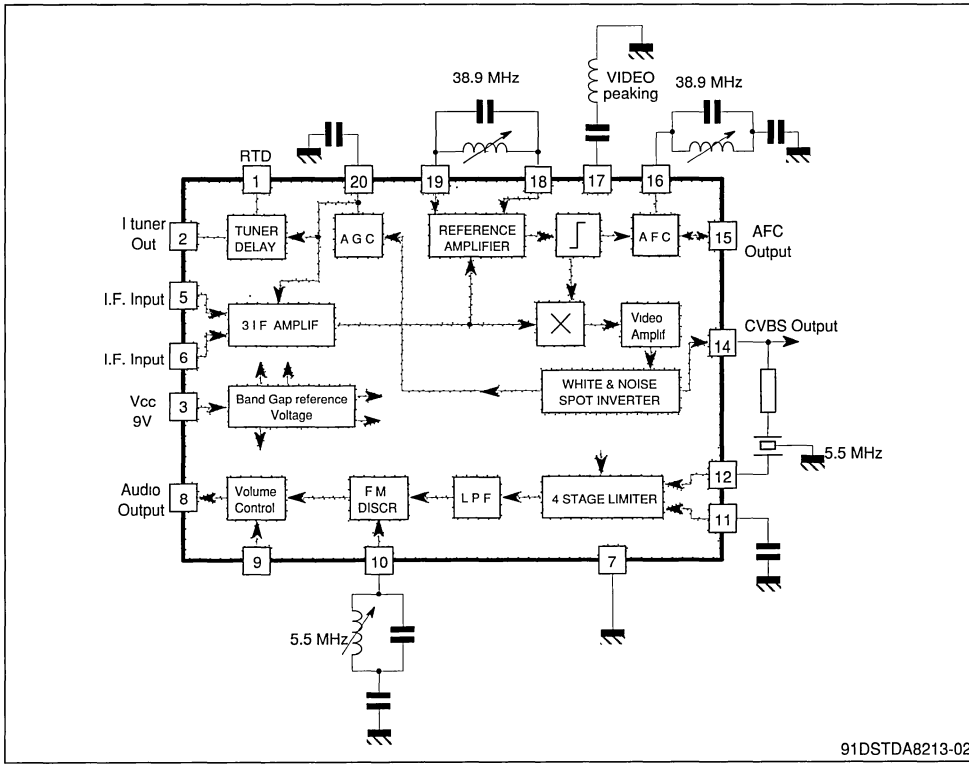
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply voltage	13.5	V
V_X	Tuner AGC voltage	V_S	V
P	Power dissipation at T_{AMB} = 70°C	880	mW
T_{STG}	Storage temperature range	-40 to 150	°C

THERMAL DATA

$R_{TH(j-a)}$	Junction-ambient thermal resistance	Max.	80	°C/W

ELECTRICAL CHARACTERISTICS

T_{AMB} = 25°C ; V_{CC} = 9V
IF input = 10 mV_{RMS} top sync
M = 100% ; R = 10% ; D = 90%
Video BW = 5MHz (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	Supply voltage		8	9	13.2	V
	Supply current		14	20	28	mA
	AGC range		58	64	67	dB
	IF - sensitivity (RMS)	Video out -3dB		70		µV
	R input differential	Guaranteed by process	1	1.5	2	kΩ
	C input Stray				2	pF
	S/N video (BW = 5MHz)	• IF inp. = 10mV_{RMS} top synchro • 20 $\log_{10} \frac{(WH - BL)}{N_{RMS}}$	49	55		dB
	Intermodulation 1.07MHz	• AGC open loop • Picture carrier = 0dB •Chrominance carrier = -3.2dB • Sound carrier = -20dB		50		dB
	Detected video output peak to peak (positive)		1.8	2	2.2	V
	Top synchro output level			1.9		V
	Video Bandwidth without output filter	-3dB			9	MHz
	Differential phase			3	7	Degree
	Differential gain			3	7	%
	White noise clamp	Referred to the video output		4.5		V
	White noise insertion			3.2		V
	Video output current capability		1.4	2	2.6	mA
	A.F.C. slope	With R_{Load} = 200kΩ	25	40	60	$\frac{mV}{kHZ}$
	Maximum I charge		630	900	1200	µA
	Maximum I discharge		14	20	26	µA
	I_{CH} / I_{DISCH} Ratio			45		-
	I max. output tuner AGC	• Suitable for Mosfet-NCH	1.3	2	2.6	mA
	Slope	• RTD = 0 ÷ 10kΩ			450	$\frac{\mu A}{dB}$
	Residual output carrier (RMS)	• At 38.9MHz • At 77.8MHz			10 20	mV mV

ELECTRICAL CHARACTERISTICS (continued)

T_{AMB} = 25°C ; V_{CC} = 9V
Sound carrier input (5.5MHz) = 10mV_{RMS}
fm = 1kHz ; Audio BW = 20kHz
$\Delta F = \pm$ 25kHz ; volume attenuation = 0dB (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	Detected output audio signal (RMS)		120	270	350	mV
	Total harmonic distorsion			0.5	2	%
	Amplitude modulation rejection	m = 30%	40	53		dB
	2nd IF sound sensitivity -3dB FM detected audio signal (RMS)			200		µV
	$\frac{S+N}{N}$	•$\Delta f = \pm$ 25kHz for signal •Δf= 0 after deemphasis (BW = 20kHz)I	50	60		dB
	Supply voltage rejection ratio	•Δf = 0 •f_{RIPPLE} on V_{CC} = 100Hz		66		dB
	Thermal drift of volume			0.05		$\frac{dB}{°C}$
	Input resistance limiter		400	560	720	Ω
	Volume control versus V_9	with selective volmeter (BW = 200Hz) V9 = 4.5V V_9 = 2.5V V_9 = 0.9V	 12 65	 0 18 74	 24	 dB dB dB

TEST CIRCUIT

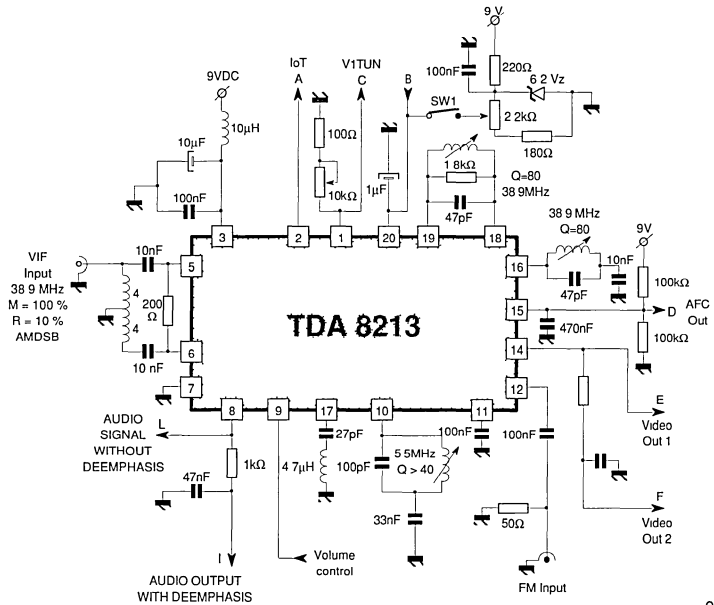


Figure 1 : Output Signal Bandwidth without Video peaking

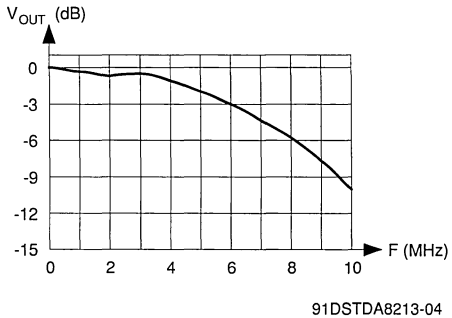


Figure 2 : Output Signal Bandwidth with Video peaking

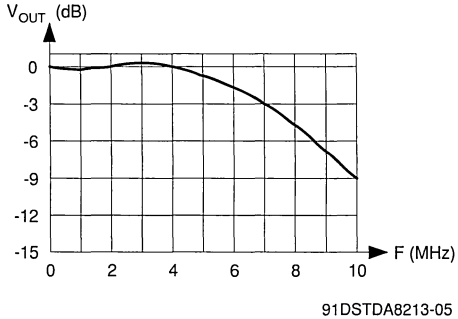


Figure 3 : AFC Voltage versus Input Frequency

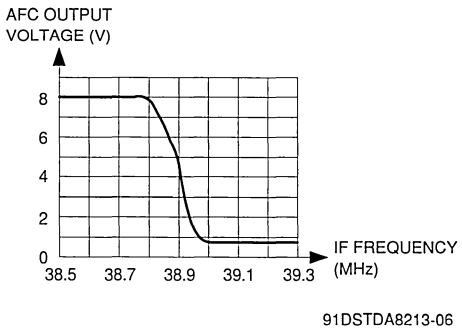


Figure 4 : Volume Control Attenuation versus Voltage in Pin 9

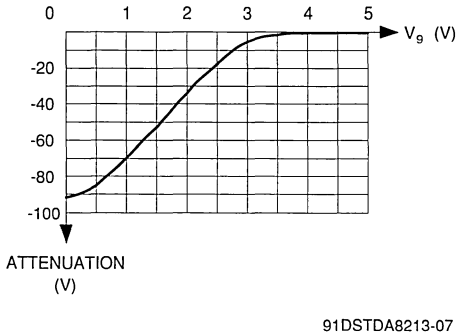


Figure 5 : Typical Connection from µP to TDA8213 for Remote Volume Control (Pin 9)

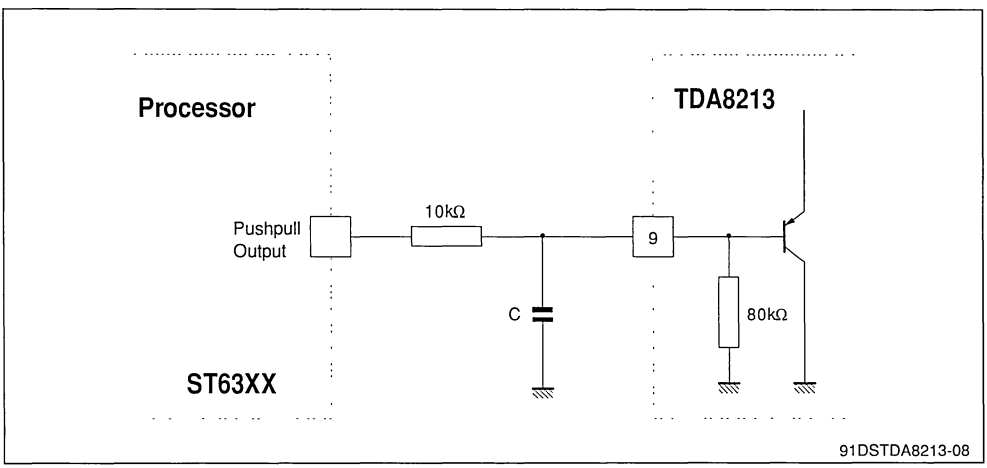
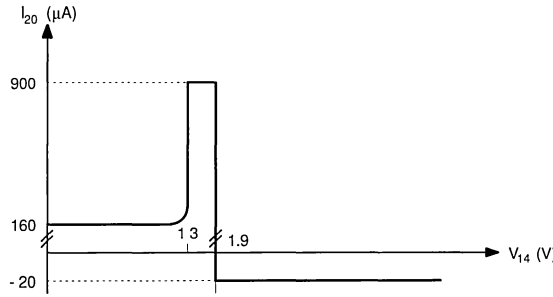
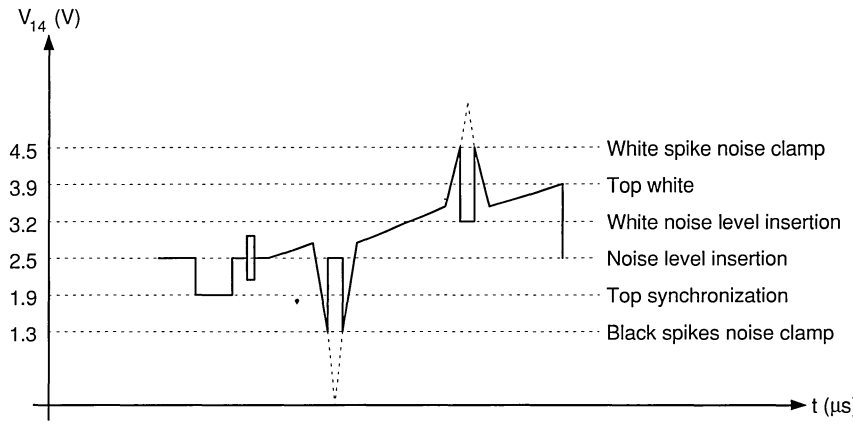


Figure 6 : IF AGC Current (Pin 20) versus Video Output Voltage



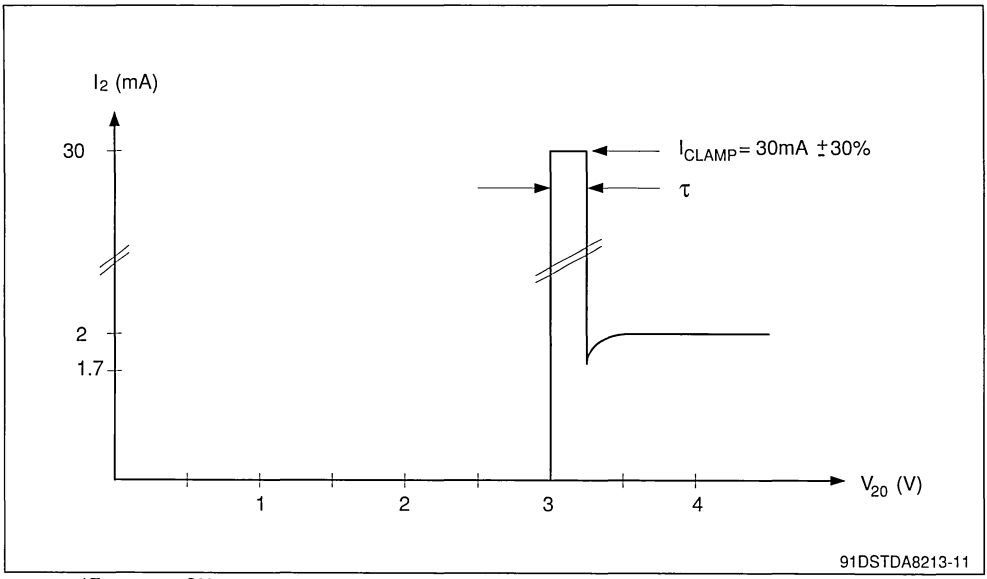
91DSTDA8213-09

Figure 7 : NSI & WSI Characteristic.



91DSTDA8213-10

Figure 8 : Tuner Output Current (Pin2) for Tuner Delay AGC behaviour @ R1 constant (take overpoint set), picture carrier IF step-up 10dB accross the take overpoint.



Note : $\tau = \frac{kT}{Q} \ln(15) \cdot \frac{C20}{160\mu A} = 440\mu s$ with C20 = 1µF

Figure 9 : Typical Application

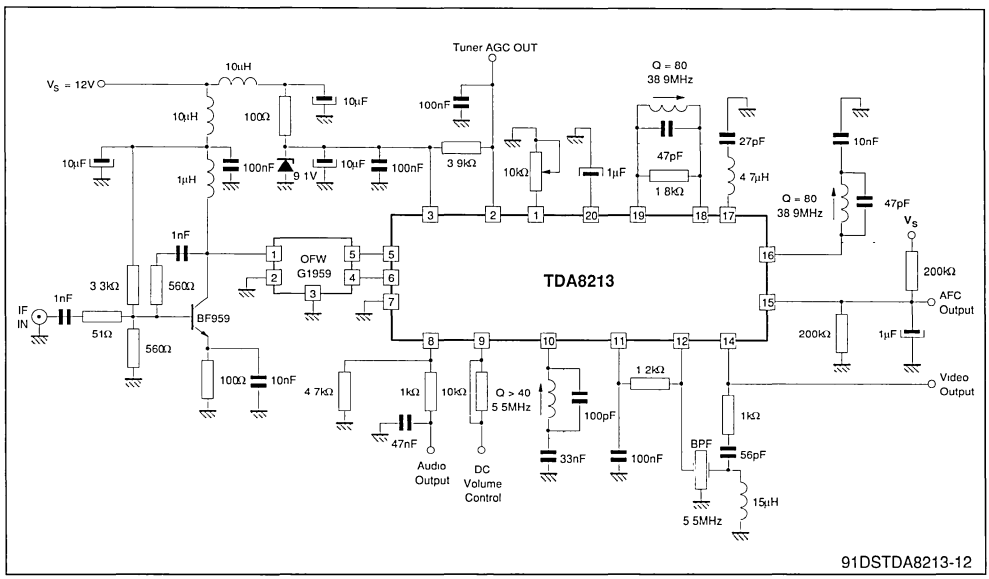
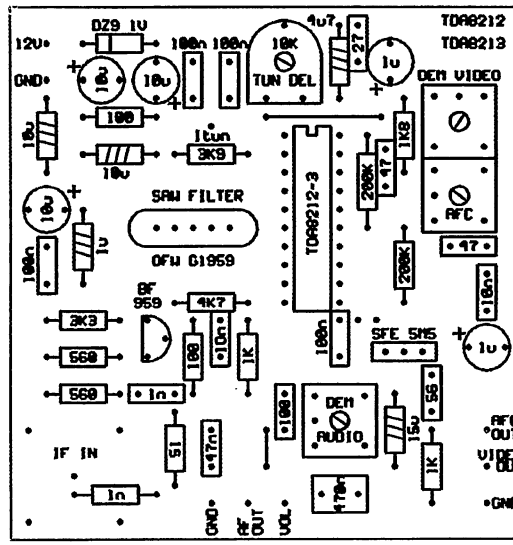


Figure 10 : PC Board and Components Lay-out of the Circuit of Figure 9 (1 : 1 scale)

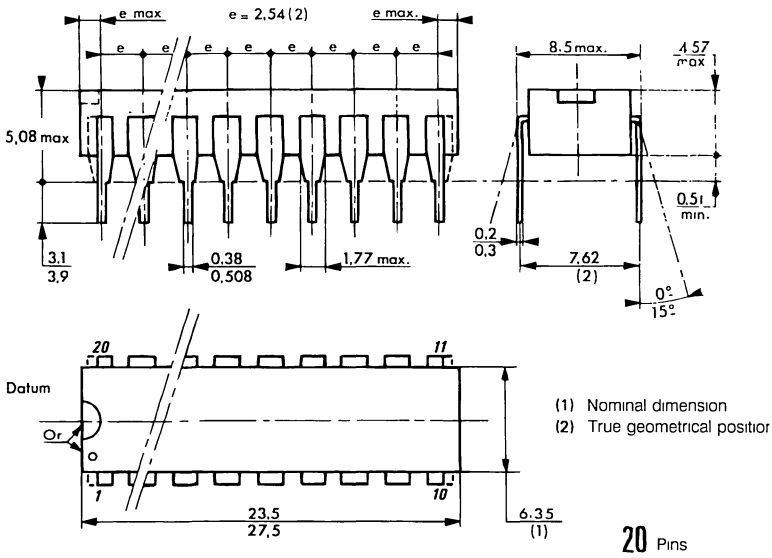


91DSTDA8213-13A

91DSTDA8213-13B

PACKAGE MECHANICAL DATA

20 PINS - PLASTIC DIP



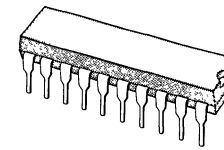
SGS-THOMSON MICROELECTRONICS

TDA8214A

HORIZONTAL AND VERTICAL DEFLECTION CIRCUIT

ADVANCE DATA

- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- VIDEO IDENTIFICATION CIRCUIT
- SUPER SANDCASTLE OUTPUT
- VERY FEW EXTERNAL COMPONENTS
- VERY LOW COST POWER PACKAGE



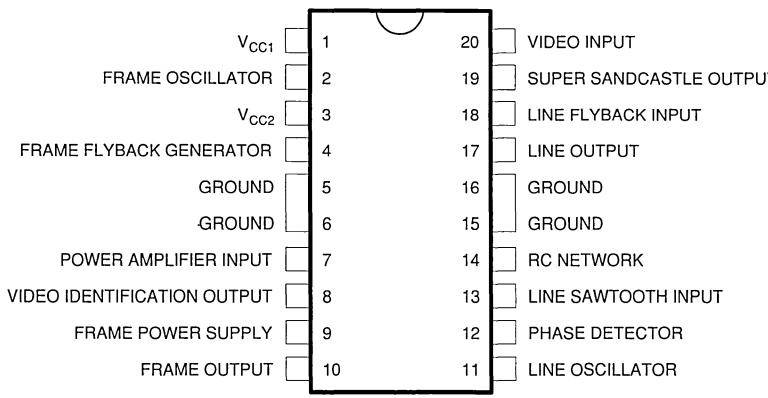
POWERDIP 16 + 2 + 2
(Plastic Package)

ORDER CODE : TDA8214A

DESCRIPTION

The TDA8214A is an horizontal and vertical deflection circuit with super sandcastle generator and video identification output. Used with TDA8213 (Video & Sound IF system) and TDA8217 (Pal decoder and video processor), this IC permits a complete low-cost solution for PAL applications.

PIN CONNECTIONS



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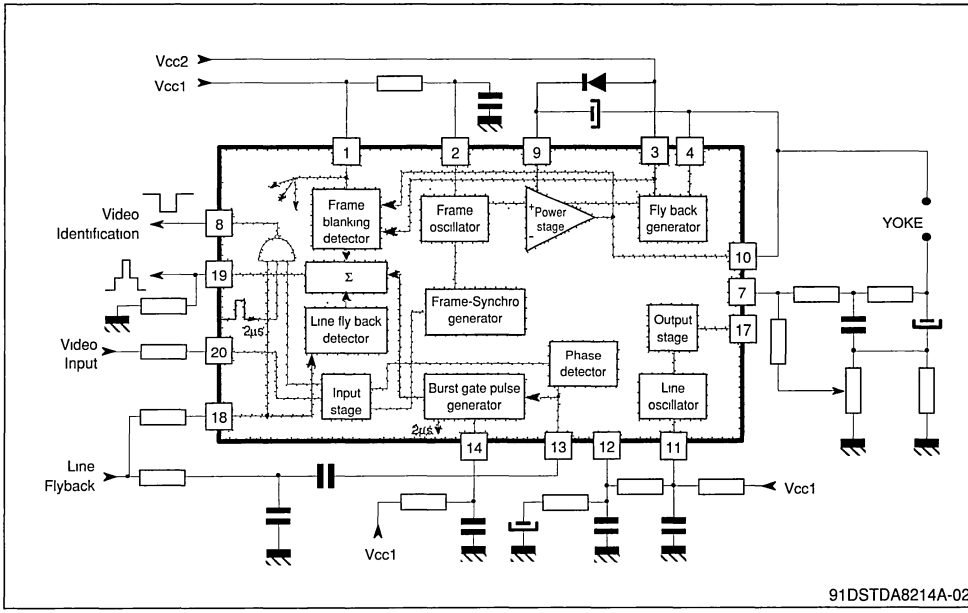
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}1$	Supply Voltage	30	V
$V_{CC}2$	Flyback Generator Supply Voltage	35	V
V9	Frame Power Supply Voltage	60	V
$I10_{NR}$	Frame Output Current (non repetitive)	± 1.5	A
I10	Frame Output Current (continuous)	± 1	A
V17	Line Output Voltage (external)	60	V
I_P17	Line Output Peak Current	0.8	A
I_C17	Line Output Continuous Current	0.4	A
T_{STG}	Storage Temperature	-40 to + 150	°C
T_J	Max Operating Junction Temperature	+ 150	°C
T_{AMB}	Operating Ambient Temperature	0 to 70	°C

THERMAL DATA

$R_{TH(j-c)}$	Max Junction-case Thermal Resistance	10	°C/W
$R_{TH(j-a)}$	Typical Junction-ambient Thermal Resistance *(Soldered on a 35µm thick 45cm^2 PC Board copper area)*	40	°C/W
T_J	Max Recommended Junction Temperature	120	°C

ELECTRICAL CHARACTERISTICS

V_{CC1} = 10 V, T_{AMB} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (Pin 1)					
I_{CC1}	Supply Current		15		mA
V_{CC1}	Supply Voltage	9	10	10.5	V
VIDEO INPUT (Pin 20)					
V20	Reference Voltage (I20 = -1µA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (When synchronized with TTL signal)	50			µs
LINE OSCILLATOR (Pin 11)					
LT11	Low Threshold Voltage	2.8	3.2	3.6	V
HT11	High Threshold Voltage	5.4	6.6	7.8	V
BI11	Bias Current		100		nA
DR11	Discharge Impedance	1.0	1.4	1.8	kΩ
FLP1	Free Running Line Period (R = 34.9kΩ Tied to V_{CC1}, C = 2.2nF Tied to Ground)	62	64	66	µs
FLP2	Free Running Line Period (R = 13.7KΩ, C = 2.2nF)		27		µs
OT11	Oscillator Threshold for Line Output, Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application)		2		Hz/°C
LINE OUTPUT (Pin 17)					
LV17	Saturation Voltage (I_{17} = 200mA)		1.1	1.6	V
OPW	Output Pulse width (line period = 64µs)	27	29	31	µs
LINE SAWTOOTH INPUT (Pin 13)					
V13	Bias Voltage	1.8	2.4	3.2	V
Z13	Input Impedance	4.5	5.8	8	kΩ
PHASE DETECTOR (Pin 12)					
I12	Output Current During Synchro Pulse	250	350	500	µA
RI12	Current Ratio (positive/negative)	0.95	1	1.05	
LI12	Leakage Current	-2		+2	µA
CV12	Control RangeVoltage	2.60		7.10	V
VIDEO IDENTIFICATION (Pin 8)					
	Low Level Output when the line syn. tip is centered in the line retrace				
V_{H8}	Without video signal (I_8 = -500µA)	4.5	6.3		V
V_{L8}	With video signal (I_8 = 50µA)		0.6	0.9	V
FRAME OSCILLATOR (Pin 2)					
LT2	Low Threshold Voltage	1.6	2.0	2.3	V
HT2	High Threshold Voltage	2.6	3.1	3.6	V
DIF2	LT2 - HT2		1.0		V
BI2	Bias Current		30		nA
DR2	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period (R = 845kΩ Tied to V_{CC1}, C = 180nF Tied to Ground	20.5	23	25	ms
MFP	Minimum Frame Period (I20 = -100µA) with the Same RC		12.8		ms
FFP2	Free Running Frame Period (R = 408kΩ, C = 220nF)		14.3		ms
FPR	Frame Period Ratio = FFP/MFP	1.7	1.8	1.9	
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		-0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Frequency Drift with Temperature (see application)		4.10^{-3}		Hz/°C

ELECTRICAL CHARACTERISTICS (continued)

V_{CC1} = 10 V, T_{AMB} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME POWER SUPPLY (Pin 9)					
V9	Operating Voltage (with flyback Generator)	10		58	V
I9	Supply Current (V9 = 30V)		11	22	mA
FLYBACK GENERATOR SUPPLY (Pin 3)					
V_{CC2}	Operating Voltage	10		30	V
FRAME OUTPUT (Pin 10)					
	Saturation Voltage to Ground (V9 = 30V)				
LV10A	I10 = 0.1A		0.06	0.6	V
LV10B	I10 = 1A		0.37	1	V
	Saturation Voltage to V9 (V9 = 30V)				
HV10A	I10 = -0.1A		1.3	1.6	V
HV10B	I10 = -1A		1.7	2.4	V
	Saturation Voltage to V9 in Flyback Mode (V10 > V9)				
FV10A	I10 = 0.1A		1.6	2.1	V
FV10B	I10 = 1A		2.5	4.5	V
FLYBACK GENERATOR (Pin 3 and Pin 4)					
	Flyback Transistor on (output = high state), V_{CC2} = 30V V4/3 with				
F2DA	$I_{4 \rightarrow 3}$ = 0.1A		1.5	2.1	V
F2DB	$I_{4 \rightarrow 3}$ = 1A		3.0	4.5	V
	Flyback Transistor on (output = high state), V_{CC2} = 30V V3/4 with				
FSVA	$I_{3 \rightarrow 4}$ = 0.1A		0.8	1.1	V
FSVB	$I_{3 \rightarrow 4}$ = 1A		2.2	4.5	V
	Flyback Transistor off (output = V9 - 8V), V9 - V_{CC2} = 30V				
FCI	Leakage Current Pin 3			170	µA
SUPER SANDCASTLE OUTPUT (Pin 19)					
	Output Voltages (R load = 2.2kΩ)				
SANDT2	Frame blanking pulse level	2	2.5	3	V
SANDL2	Line blanking pulse level	4	4.5	5	V
BG2	Burst key pulse level	8	9		V
	Pulses width and timing				
SC3	Delay between middle of sync pulse and leading edge of burst key pulse	2.3	2.7	3.1	µs
SC2	Duration of burst key pulse Vertical blanking pulse width	3.7	4 Note 1	5	µs
LINE FLYBACK INPUT (Pin 18)					
	Switching level		2		V
	Maximum imput current at V_{PEAK} = 800V		8		mA
	Limiting voltage at maximum current		4.3		V
τ	RC network time constant (Note 2)		6		µs

Notes : 1 Width of vertical blanking pulse on SSC output is proportional to the frame flyback time, the switching level is $V_{CC}2 - 2V_{BE}$ and the other input of the comparator is tied to the frame amplifier output Application circuit uses the frame flyback generator.

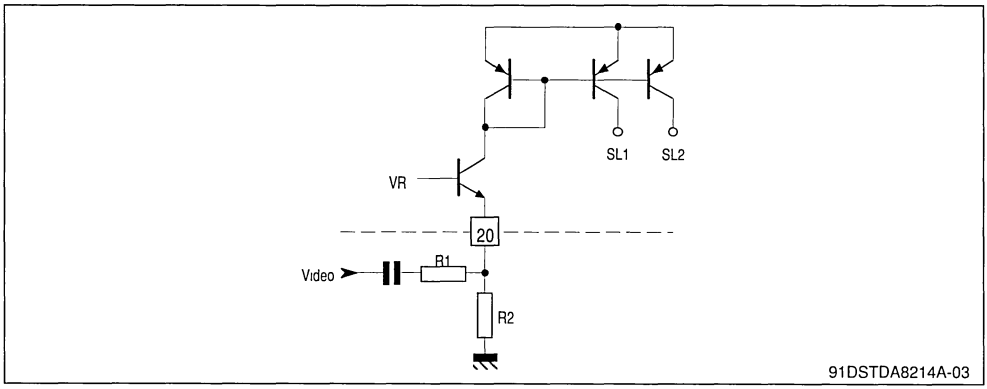
2 An RC network is connected to this input Typical value for the resistor is 27kΩ and 220pF for the capacitor A different time constant for RC changes the delay between the middle of the line synchro pulse and the leading edge of the burst key pulse but also the duration of the burst key pulse

GENERAL DESCRIPTION

The TDA8214A performs all the video and power functions required to provide signals for the line driver and frame yoke.
It contains:

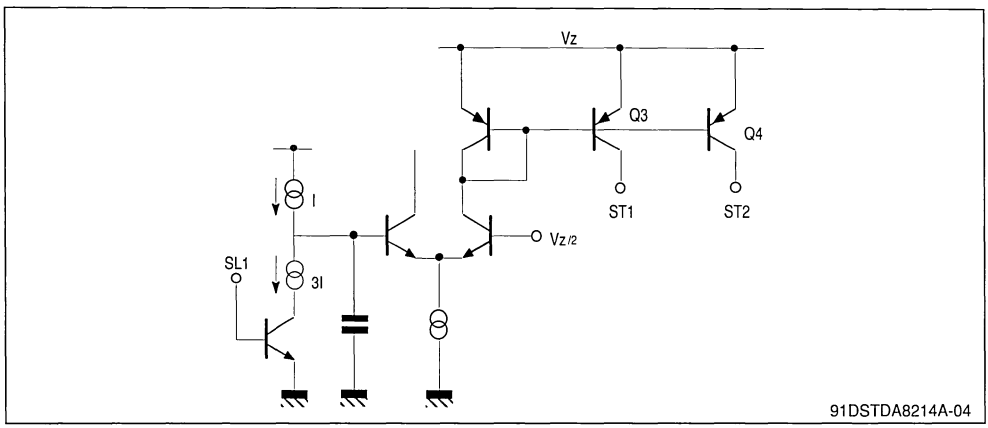
- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line driver
- A line phase detector and a voltage control oscillator
- A super sandcastle generator
- Video identification output.

Figure 1 : Synchronization Separator Circuit



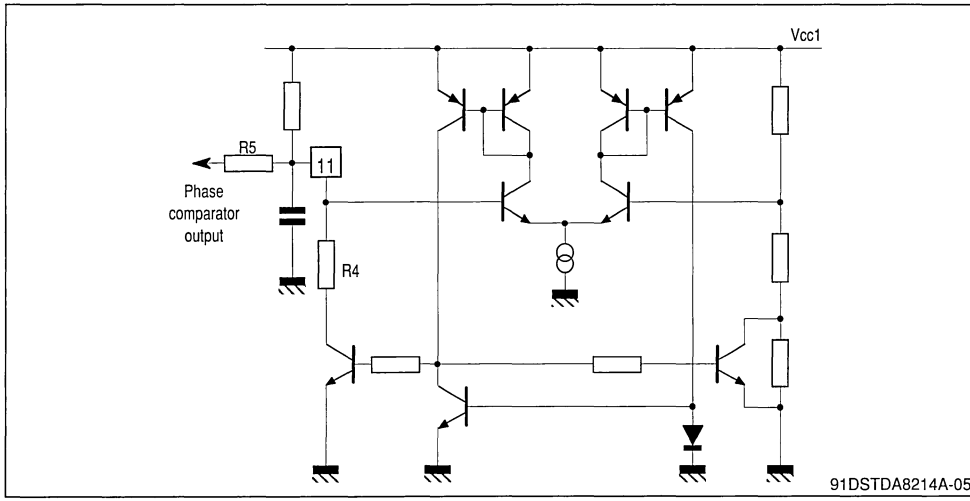
The slice level of sync-separation is fixed by value of the external resistors R1 and R2. V_R is an internally fixed voltage.

Figure 2 : Frame Separator



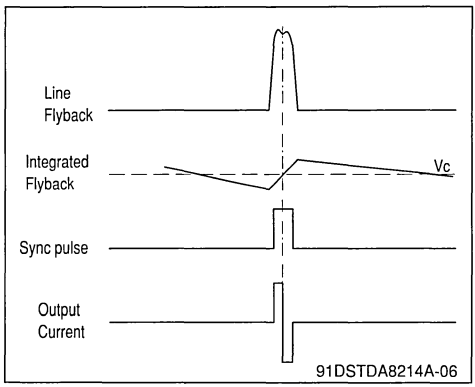
The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync-pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q_3 and Q_4 provide current for the other parts of the circuit.

Figure 3: Line Oscillator



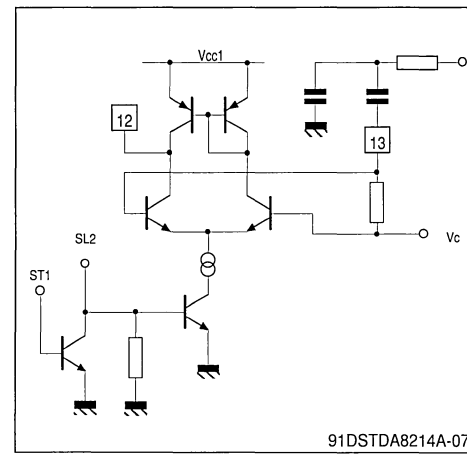
The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

Figure 4: Phase Comparator



The sync-pulse drives the current in the comparator. The line flyback integrated by the external net work gives on pin 13 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 13 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

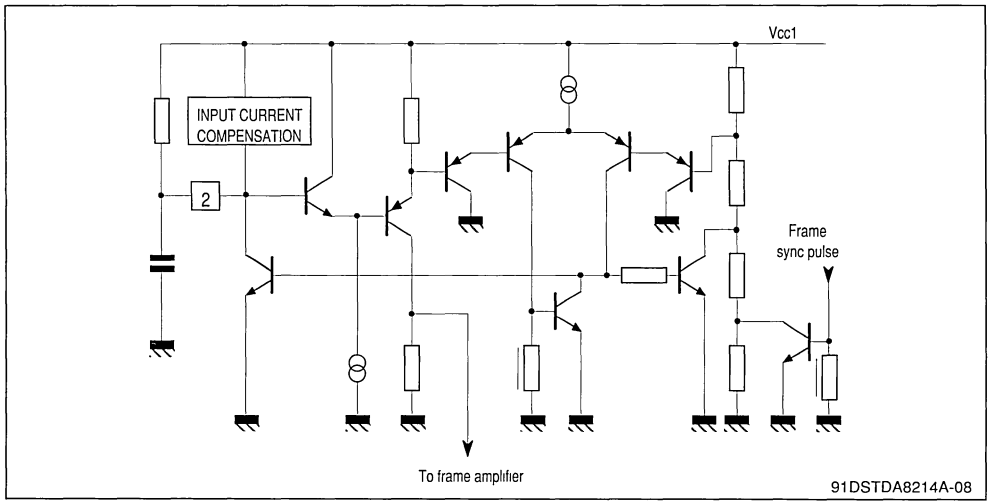
Figure 5



Line output (Pin 17)

It is an open-collector output. The output positive pulse time is 29µs for a 64µs period.

Figure 6: Frame Oscillator

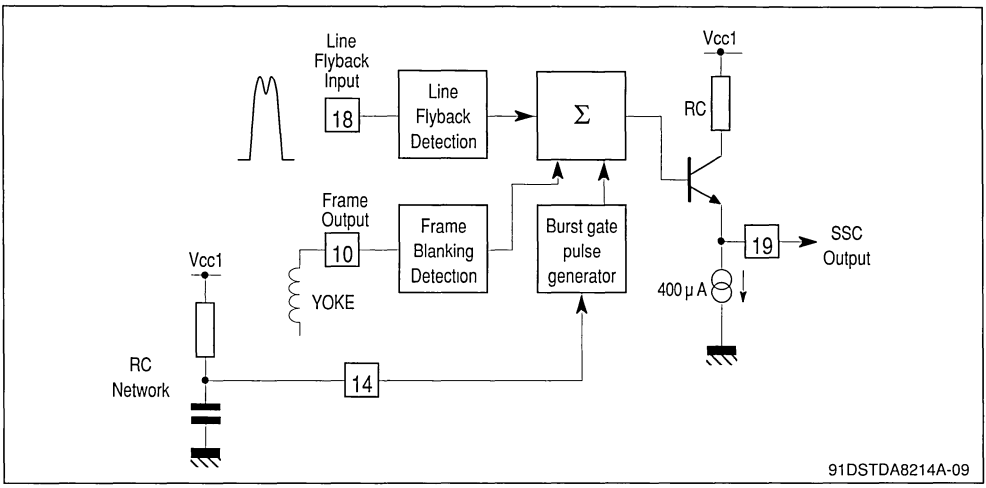


The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Frame output amplifier

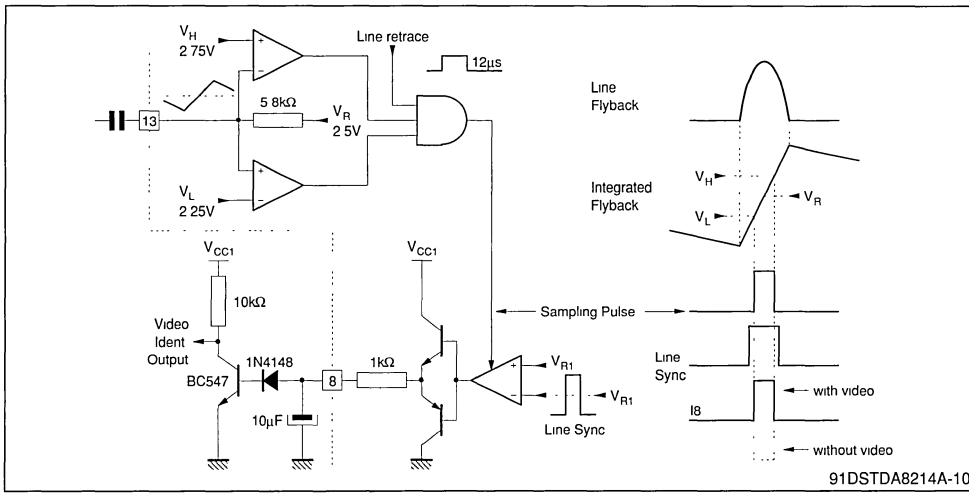
This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected; it contains also a thermal protection.

Figure 7: Super sandcastle generator



The frame blanking is detected by the frame flyback generator. When the output voltage of the frame amplifier exceeds $V_{CC}2\text{-}2V_{BE}$, the pulse is detected. The line flyback detection is provided by a comparator which compares the input line flyback pulse to an internal reference. The burst gate pulse position is fixed by the external RC network (pin 14). It is referenced to the middle of the line flyback.

Figure 8 : Video Identification Circuit (PIn 8).

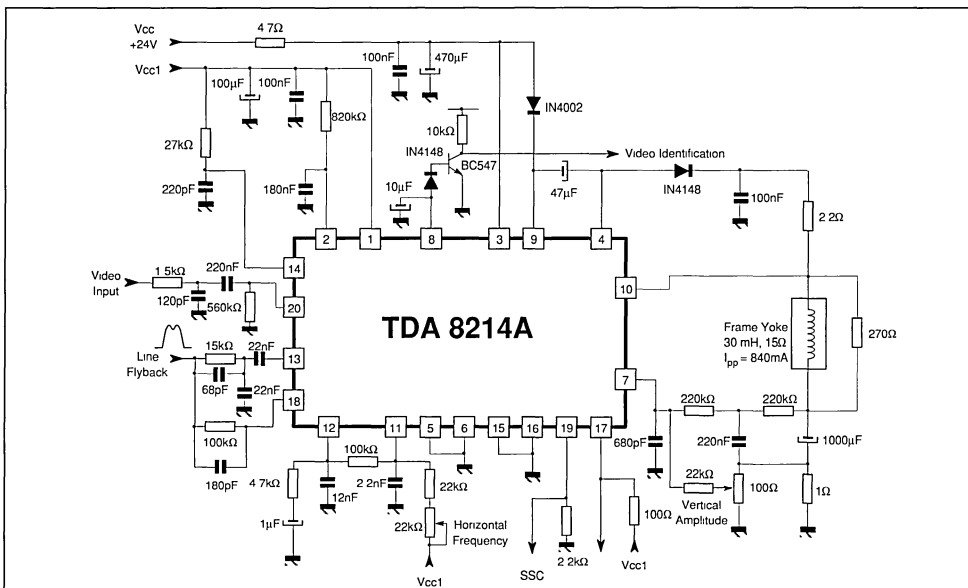


This stage will detect the coincidence between the line sync pulse (if present) and a 2µs sampling pulse. This 2µs pulse is positionned at the center of line sync pulse when the phase loop is locked. This sampled detection is stored by an external capacitor Pin 8.

The identification output level is high when video signal is present.

Important remark : minimum saw-tooth amplitude on Pin 13 has to be $2V_{PP}$ (typ. : $2.5V_{PP}$).

TYPICAL APPLICATION

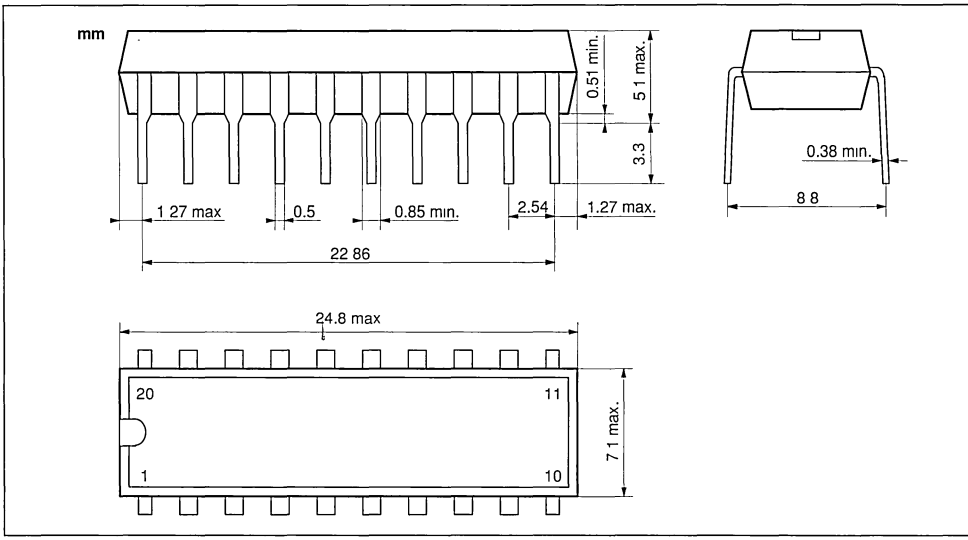


Note . Pins 5 - 6 : Frame oscillator ground
Pins 15 - 16 . Frame and line power ground

91DSTDA8214A-11

PACKAGE MECHANICAL DATA

20 PINS - POWER DIP 16 + 2+ 2



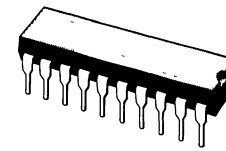
SGS-THOMSON MICROELECTRONICS

TDA8215A

HORIZONTAL AND VERTICAL DEFLECTION CIRCUIT

ADVANCE DATA

- DIRECT LINE DARLINGTON DRIVE
- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- VIDEO IDENTIFICATION CIRCUIT
- SUPER SANDCASTLE OUTPUT
- VERY FEW EXTERNAL COMPONENTS
- VERY LOW COST POWER PACKAGE



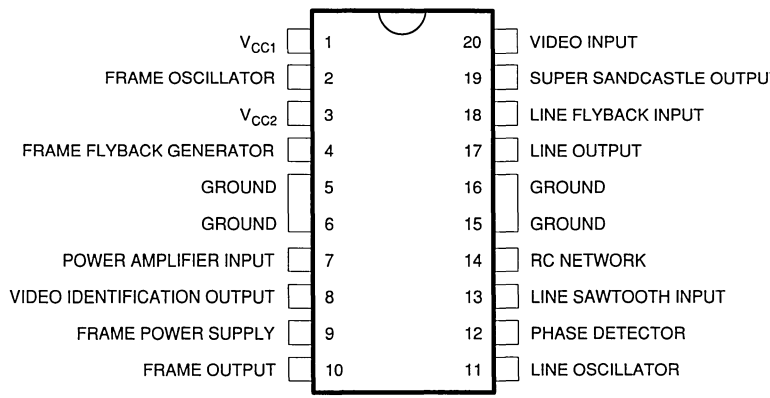
POWERDIP 16 + 2 + 2
(Plastic Package)

ORDER CODE : TDA8215A

DESCRIPTION

The TDA8215A is an horizontal and vertical deflection circuit with super sandcastle generator and video identification output. Used with TDA8213 (Video & Sound IF system) and TDA8217 (Pal decoder and video processor), this IC permits a complete low-cost solution for PAL applications. THe TDA8215A has been specially designed for direct drive of line DARLINGTON transistors.

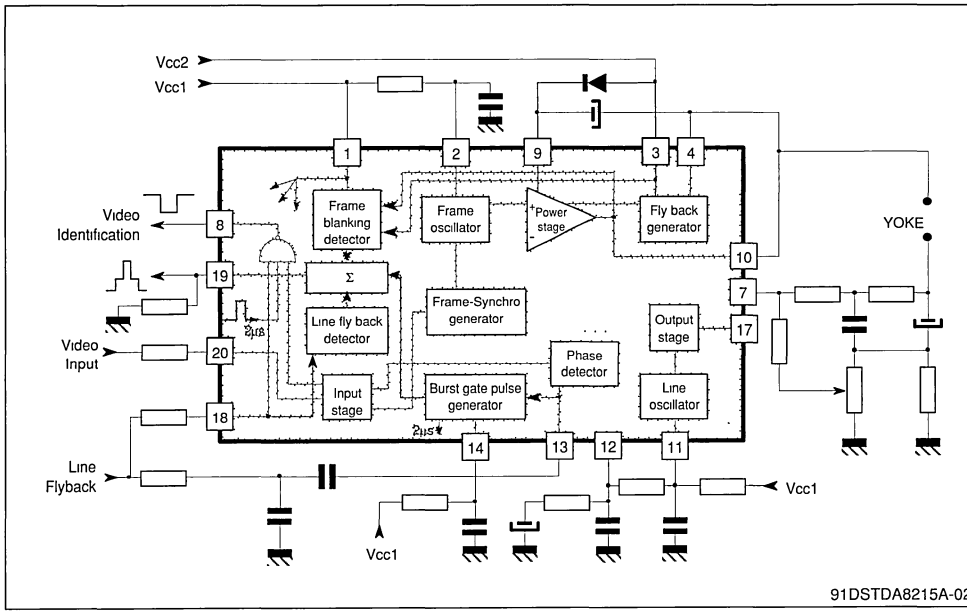
PIN CONNECTIONS



91DSTDA8215A-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}1$	Supply Voltage	30	V
$V_{CC}2$	Flyback Generator Supply Voltage	35	V
V9	Frame Power Supply Voltage	60	V
$I10_{NR}$	Frame Output Current (non repetitive)	± 1.5	A
I10	Frame Output Current (continuous)	± 1	A
V17	Line Output Voltage (external)	60	V
I_P17	Line Output Peak Current	0.8	A
I_C17	Line Output Continuous Current	0.4	A
T_{STG}	Storage Temperature	-40 to + 150	°C
T_J	Max Operating Junction Temperature	+ 150	°C
T_{AMB}	Operating Ambient Temperature	0 to 70	°C

THERMAL DATA

$R_{TH(j-c)}$	Max Junction-case Thermal Resistance	10	°C/W
$R_{TH(j-a)}$	Typical Junction-ambient Thermal Resistance *(Soldered on a 35µm thick 45cm^2 PC Board copper area)*	40	°C/W
T_J	Max Recommended Junction Temperature	120	°C

ELECTRICAL CHARACTERISTICS

V_{CC1} = 10 V, T_{AMB} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (Pin 1)					
I_{CC1}	Supply Current		15		mA
V_{CC1}	Supply Voltage	9	10	10.5	V
VIDEO INPUT (Pin 20)					
V20	Reference Voltage (I20 = -1µA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (When synchronized with TTL signal)	50			µs
LINE OSCILLATOR (Pin 11)					
LT11	Low Threshold Voltage	2.8	3.2	3.6	V
HT11	High Threshold Voltage	5.4	6.6	7.8	V
BI11	Bias Current		100		nA
DR11	Discharge Impedance	1.0	1.4	1.8	kΩ
FLP1	Free Running Line Period (R = 34.9kΩ Tied to V_{CC1}, C = 2.2nF Tied to Ground)	62	64	66	µs
FLP2	Free Running Line Period (R = 13.7KΩ, C = 2.2nF)		27		µs
OT11	Oscillator Threshold for Line Output Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application)		2		Hz/°C
LINE OUTPUT (Pin 17)					
LV17	Saturation Voltage (I_{17} = 800mA during 2µs)		2.2		V
OPW	Output Pulse width (line period = 64µs , negative pulse)	19	21	23	µs
LINE SAWTOOTH INPUT (Pin 13)					
V13	Bias Voltage	1.8	2.4	3.2	V
Z13	Input Impedance	4.5	5.8	8	kΩ
PHASE DETECTOR (Pin 12)					
I12	Output Current During Synchro Pulse	250	350	500	µA
RI12	Current Ratio (positive/negative)	0.95	1	1.05	
LI12	Leakage Current	-2		+2	µA
CV12	Control Voltage Range	2.60		7.10	V
VIDEO IDENTIFICATION (Pin 8)					
	Low Level Output when the line synchro tip is centered in the line retrace				
V_{H8}	without Video Signal (I_8 = -500µA)	4.5	6.3	0.9	V
V_{L8}	with Video Signal (I_8 = 50µA)		0.6	0.9	V
FRAME OSCILLATOR (Pin 2)					
LT2	Low Threshold Voltage	1.6	2.0	2.3	V
HT2	High Threshold Voltage	2.6	3.1	3.6	V
DIF2	LT2 - HT2		1.0		V
BI2	Bias Current		30		nA
DR2	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period (R = 845kΩ Tied to V_{CC1}, C = 180nF Tied to Ground)	20.5	23	25	ms
MFP	Minimum Frame Period (I20 = -100µA) with the Same RC		12.8		ms
FFP2	Free Running Frame Period (R = 408kΩ, C = 220nF)		14.3		ms
FPR	Frame Period Ratio = FFP/MFP	1.7	1.8	1.9	
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		-0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Frequency Drift with Temperature (see application)		4.10^{-3}		Hz/°C

ELECTRICAL CHARACTERISTICS (continued)

V_{CC1} = 10 V, T_{AMB} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME POWER SUPPLY (Pin 9)					
V9	Operating Voltage (with flyback Generator)	10		58	V
I9	Supply Current (V9 = 30V)		11	22	mA
FLYBACK GENERATOR SUPPLY (Pin 3)					
$V_{CC}2$	Operating Voltage	10		30	V
FRAME OUTPUT (Pin 10)					
	Saturation Voltage to Ground (V9 = 30V)				
LV10A	I10 = 0.1A		0.06	0.6	V
LV10B	I10 = 1A		0.37	1	V
	Saturation Voltage to V9 (V9 = 30V)				
HV10A	I10 = -0.1A		1.3	1.6	V
HV10B	I10 = -1A		1.7	2.4	V
	Saturation Votage to V9 in Flyback Mode (V10 > V9)				
FV10A	I10 = 0.1A		1.6	2.1	V
FV10B	I10 = 1A		2.5	4.5	V
FLYBACK GENERATOR (Pin 3 and Pin 4)					
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V4/3 with				
F2DA	$I_{4 \rightarrow 3}$ = 0.1A		1.5	2.1	V
F2DB	$I_{4 \rightarrow 3}$ = 1A		3.0	4.5	V
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V3/4 with				
FSVA	$I_{3 \rightarrow 4}$ = 0.1A		0.8	1.1	V
FSVB	$I_{3 \rightarrow 4}$ = 1A		2.2	4.5	V
	Flyback Transistor off (output = V9 - 8V), V9 - V_{CC2} = 30V				
FCI	Leakage Current Pin 3			170	µA
SUPER SANDCASTLE OUTPUT (Pin 19)					
	Output Voltages (R load = 2.2kΩ)				
SANDT2	Frame blanking pulse level	2	2.5	3	V
SANDL2	Line blanking pulse level	4	4.5	5	V
BG2	Burst key pulse level	8	9		V
	Pulses width and timing				
SC3	Delay between middle of sync pulse and leading edge of burst key pulse	2.3	2.7	3.1	µs
SC2	Duration of burst key pulse Vertical blanking pulse width	3.7	4 Note 1	5	µs
LINE FLYBACK INPUT (Pin 18)					
	Switching level		2		V
	Maximum imput current at V_{PEAK} = 800V		8		mA
	Limiting voltage at maximum current		4.3		V
τ	RC network time constant (Note 2)		6		µs

Notes :

1. Width of vertical blanking pulse on SSC output is proportional to the frame flyback time, the switching level is $V_{CC}2 - 2V_{BE}$ and the other input of the comparator is tied to the frame amplifier output. Application circuit uses the frame flyback generator.
2. An RC network is connected to this input. Typical value for the resistor is 27kΩ and 220pF for the capacitor. A different time constant for RC changes the delay between the middle of the line synchro pulse and the leading edge of the burst key pulse but also the duration of the burst key pulse.

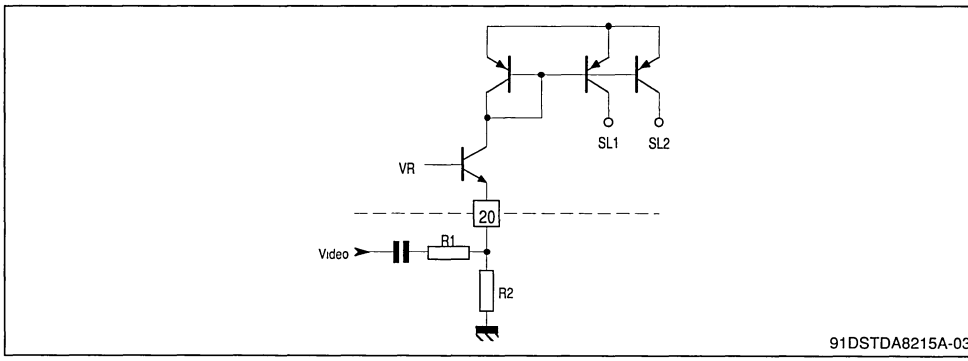
GENERAL DESCRIPTION

The TDA8215A performs all the video and power functions required to provide signals for the line driver and frame yoke.

It contains:

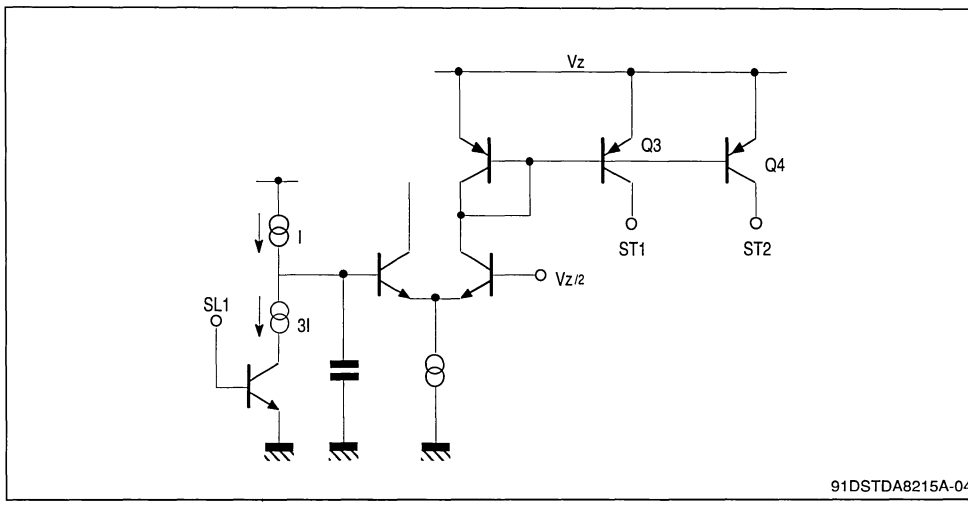
- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line darlington drive
- A line phase detector and a voltage control oscillator
- A super sandcastle generator
- Video identification output.

Figure 1 : Synchronization Separator Circuit



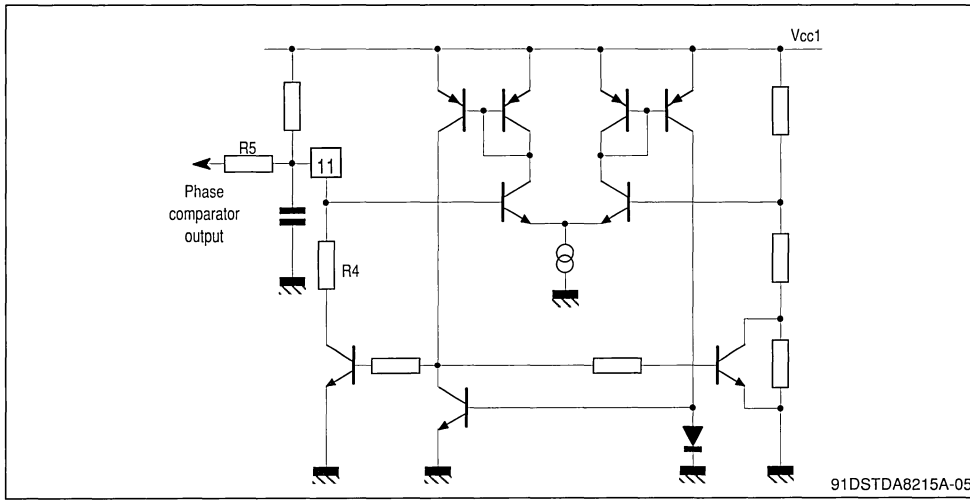
The slice level of sync-separation is fixed by value of the external resistors R1 and R2. VR is an internally fixed voltage.

Figure 2 : Frame Separator



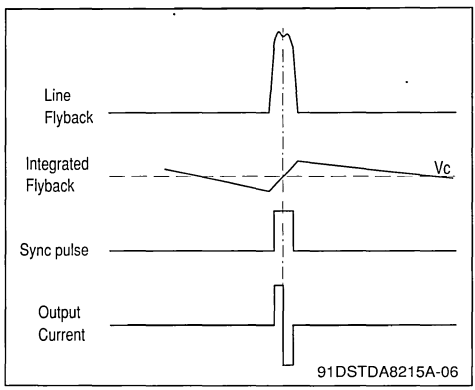
The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync-pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q_3 and Q_4 provide current for the other parts of the circuit.

Figure 3: Line Oscillator



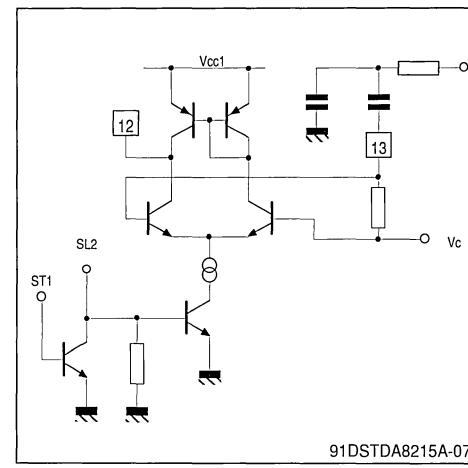
The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

Figure 4: Phase Comparator



The sync-pulse drives the current in the comparator. The line flyback integrated by the external net work gives on pin 13 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 13 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

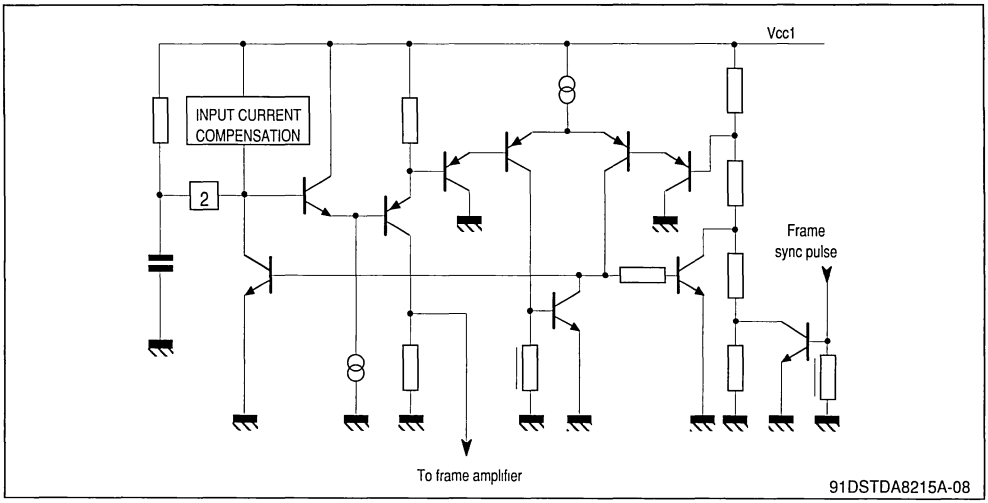
Figure 5



Line output (Pin 17)

It is an open-collector output. The output negative pulse time is 22µs for a 64µs period.

Figure 6: Frame Oscillator

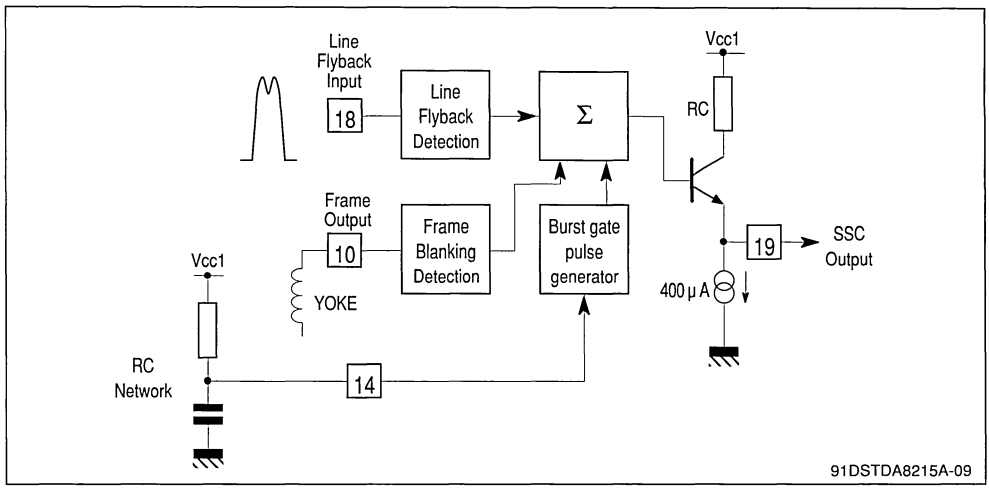


The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Frame output amplifier

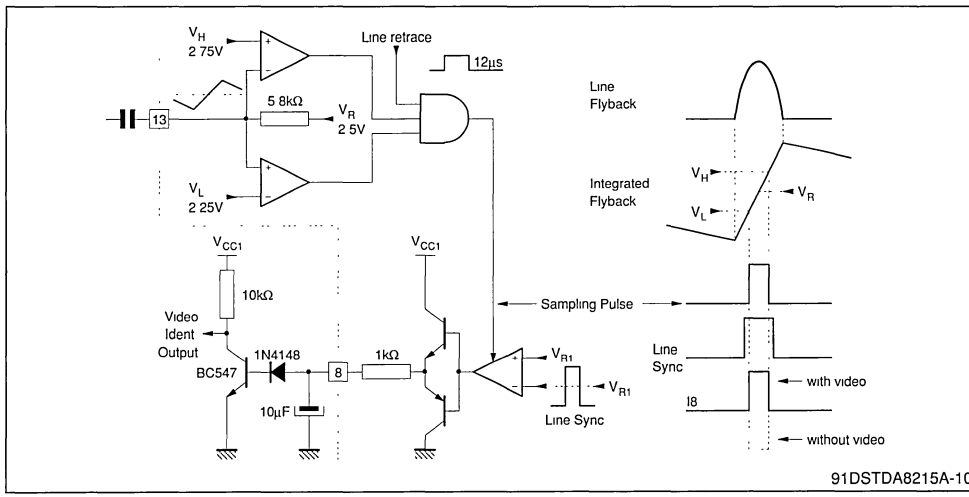
This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected; it contains also a thermal protection.

Figure 7: Super sandcastle generator



The frame blanking is detected by the frame flyback generator. When the output voltage of the frame amplifier exceeds $V_{CC}2\text{-}2V_{BE}$, the pulse is detected. The line flyback detection is provided by a comparator which compares the input line flyback pulse to an internal reference. The burst gate pulse position is fixed by the external RC network (pin 14). It is referenced to the middle of the line flyback.

Figure 8 : Video Identification Circuit (PIn 8).

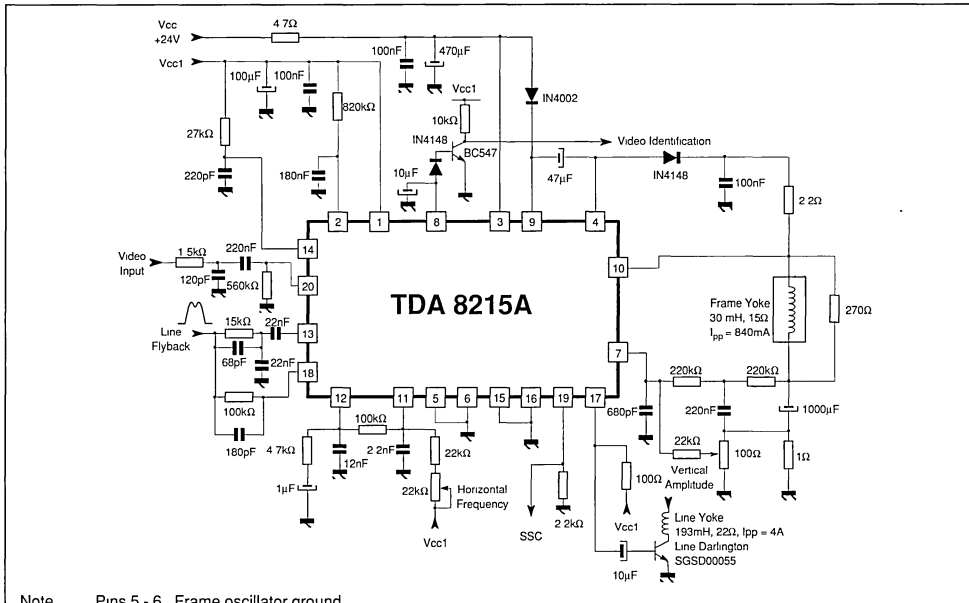


This stage will detect the coincidence between the line sync pulse (if present) and a 2µs sampling pulse. This 2µs pulse is positionned at the center of line sync pulse when the phase loop is locked. This sampled detection is stored by an external capacitor Pin 8.

The identification output level is high when video signal is present.

Important remark : minimum saw-tooth amplitude on Pin 13 has to be $2V_{PP}$ (typ. : $2.5V_{PP}$).

TYPICAL APPLICATION

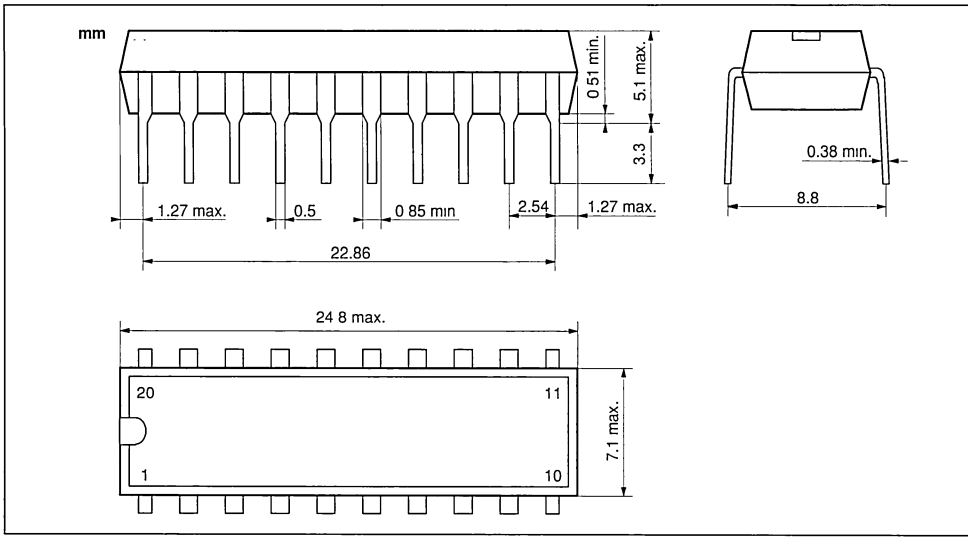


Note Pins 5 - 6 Frame oscillator ground
Pins 15 - 16 : Frame and line power ground

91DSTDA8215A-11

PACKAGE MECHANICAL DATA

20 PINS - POWER DIP 16 + 2+ 2

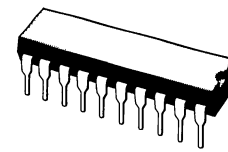


SGS-THOMSON MICROELECTRONICS

TDA8217

PAL DECODER AND VIDEO PROCESSOR

- RGB OUTPUTS
- SINGLE CHIP CHROMA AND LUMINANCE PROCESSOR
- DC CONTROL BRIGHTNESS, CONTRAST, AND SATURATION
- FEW EXTERNAL COMPONENTS
- FAST BLANKING INPUT FOR OSD INSERTION
- SUPER SANDCASTLE INPUT



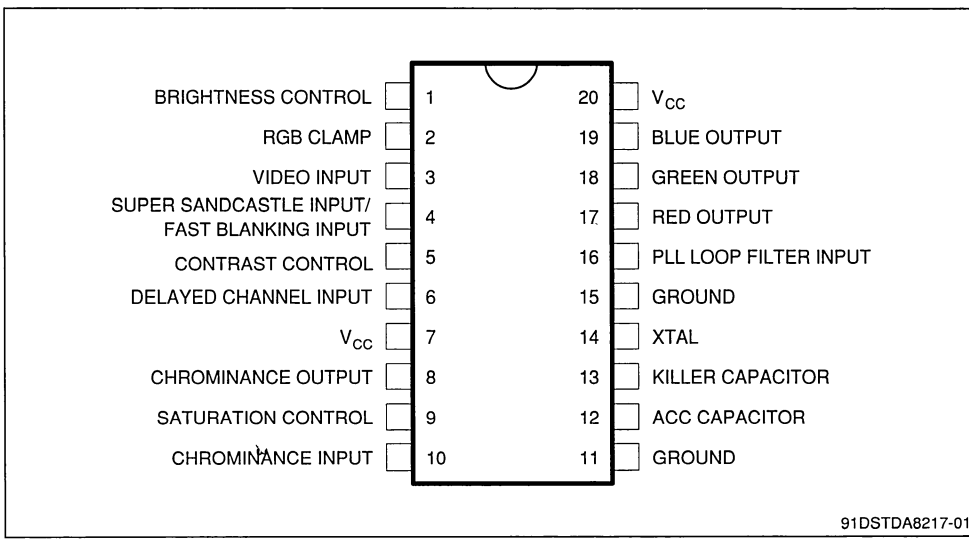
DIP20
(Plastic Package)

ORDER CODE : TDA8217

DESCRIPTION

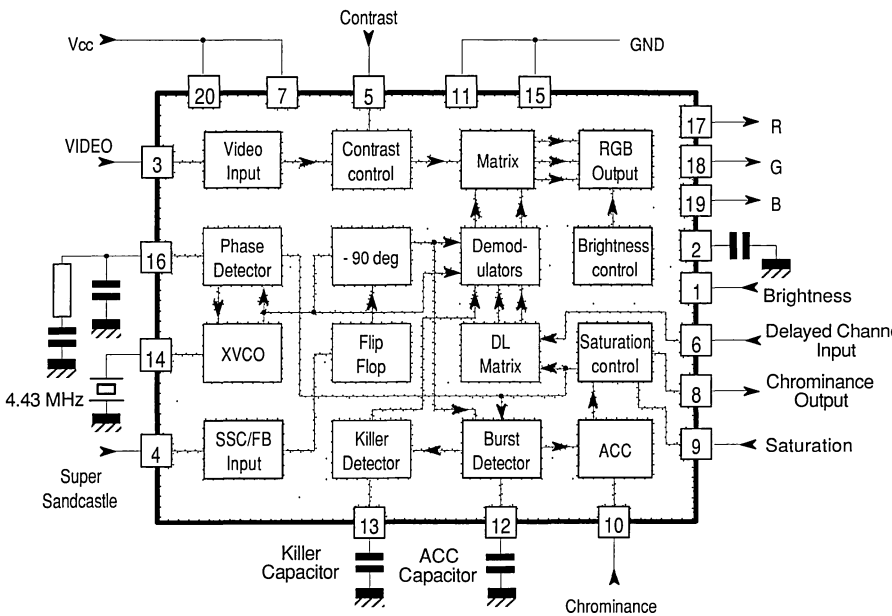
The TDA8217 is a monolithic integrated color decoder for the PAL standard. It includes in a 20 pins IC all the functions required for the identification and demodulation of PAL signals, and all the videoprocessor functions up to the drive of the video stages. Used with TDA8213 (video & sound IF system) and TDA8214A (H/V deflection circuit), this IC permits a complete low-cost solution for PAL applications.

PIN CONNECTIONS



91DSTDA8217-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	12	V
T_{OPER}	Operating temperature	0 , + 70	°C
T_{STG}	Storage temperature	-55 , + 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH\ (j-a)}$	Junction to ambient thermal resistance	Max.	80	°C/W

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 9V , T_{AMB} = 25°C (unless otherwise specified)

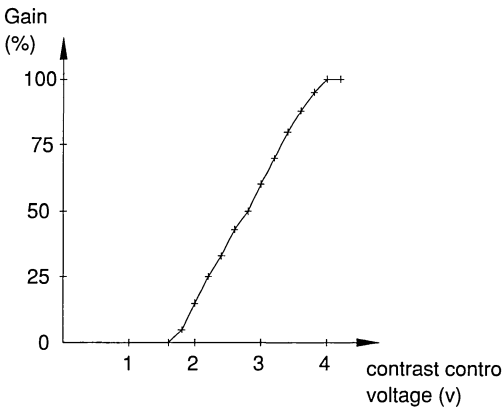
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		8	9	10	V
I_{CC}	Supply Current	No Load		30	50	mA
P_D	Total Power Dissipation	No Load		270	450	mW
LUMINANCE INPUT (Pin 3)						
	Input Level before Clipping (Black to White)				500	mV_{PP}
	DC Operating Voltage	No Input Signal	2.5	2.8	3.1	V
	Input Current	• During Burst Period • Out of Burst Period	± 50	± 100	± 150 5	µA µA
CHROMINANCE INPUT (Pin 10)						
	Input Level before Clipping				900	mV_{PP}
	Minimum Burst Signal Amplitude within the ACC Control Range		30			mV_{PP}
	ACC Control Range	Change of Burst Signal over whole ACC Control Range < 1dB	30			dB
	Input Impedance		6	8	12	kΩ
	DC Operating Voltage	No Input Signal	2.3	2 8	3.3	V
SSC INPUT (Pin 4)						
	Burst Gate Threshold		7.0	7.5	8.0	V
	Line Blanking Threshold		3.1	3.4	3.8	V
	Frame Blanking Threshold / Fast Blanking		0.5	1	1.5	V
	Input Current				60	µA
CONTRAST CONTROL INPUT (Pin 5) (See Figure 1)						
	Input Current				10	µA
	Contrast Control Range		20			dB
SATURATION CONTROL INPUT (Pin 9) (See Figure 2)						
	Input Current				10	µA
	Tracking between Luminance and Chrominance Signals over 10 dB Contrast Control				2	dB
BRIGHTNESS CONTROL INPUT (Pin 1) (See Figure 3)						
	Input Current				10	µA
ACC CAPACITOR (Pin 12)						
	Charging Current	During Burst Gate Period		100		µA
	Discharging Current	During Burst Gate Period			10	µA
	Leakage Current	Out of Burst Gate Period			5	µA
KILLER CAPACITOR (Pin 13)						
	Color off Voltage	No Chroma Signal		5.6		V
	Color on Voltage			6		V
	PAL flip-flop inhibition level			3.2		V
	Control Current			150		µA
	Leakage Current				5	µA
	Voltage with Nominal Input Signal		6.4	6.5	7.0	V
PLL LOOP FILTER (Pin 16)						
	Control Current			800		µA
	Leakage Current				5	µA
SUBCARRIER OUTPUT (Pin 8)						
	Output Burst Amplitude	Within ACC Control Range	1.6	2.4	3.0	V_{PP}

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 9V , T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DELAYED CHANNEL INPUT (Pin 6)						
	DC Operating Voltage	No Input Signal	2.0	2.2	2.4	V
	Input impedance		6	8	12	kΩ
RGB OUTPUTS (Pins 17-18-19)						
	Output Signal Amplitude (Black to White)	• 0.35V B to W, Signal @ Pin 3 • Contrast @ 4.2V • Sat. @ 1.6V • Brig. @ 3.5V	2.80	3.15	3.50	V
	Blue Channel Output Amplitude (no Y)	• 300 mV_{PP} (B-Y), Signal with 200mV_{PP} Burst Amplitude at pin 10 • Contrast @ 4.2V • Sat. @ 4.2V • Brig. @ 3.5V	3.5	3.9	4.3	V_{PP}
	Individual Output Sinking Current				2	mA
RGB OUTPUTS (Pins 17-18-19)						
	Maximum Peak White Level		7.8	8.1	8.4	V
	Blanking Level		1.0	1.2	1.4	V
	Black Level Differential Error				300	mV
	Relative Variation in Black Level with Various Saturation, Contrast and Brightness Control Level				10	mV
	Black Level Thermal Drift			0.5		mV/°C
	Differential Black Level Drift over 40°C Temperature Range			5		mV
	Frequency Response(-3dB)			5		MHz
XTAL (Pin 14)						
	Catching Range		± 500	± 700		Hz
RGB CLAMP CAPACITOR (Pin 2)						
	Control Current		50	100	150	µA
	Leakage Current				5	µA

Figure 1 : Contrast Control Voltage Range.



91DSTDA8217-03

Figure 2 : Saturation Control Voltage Range.

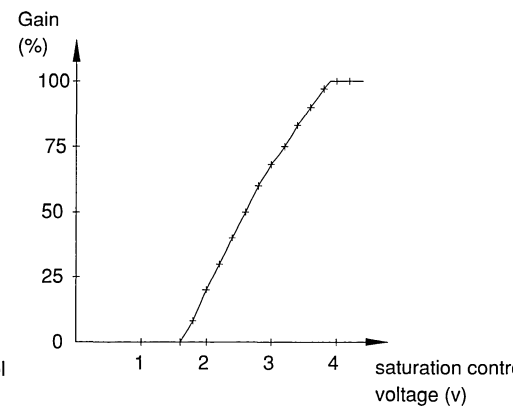


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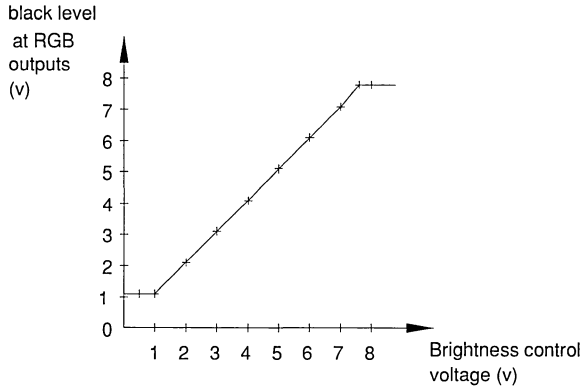
Figure 3 : Brightness Control Voltage Range.



INPUT / OUTPUT PIN CONFIGURATION

Figure 4 : Pins 1 - 2 Configuration.

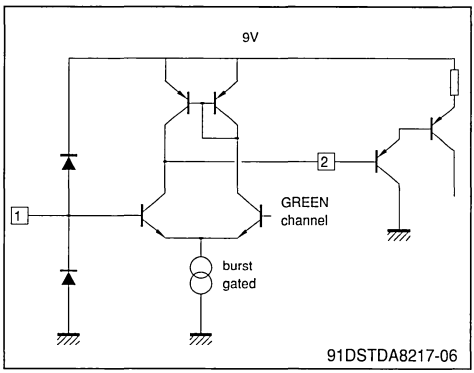


Figure 5 : Pin 3 Configuration.

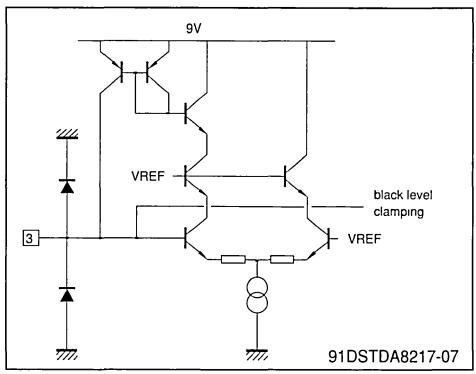
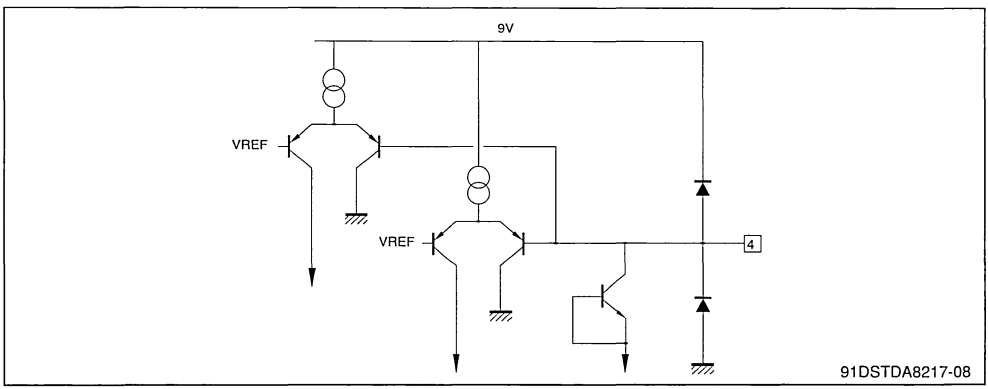


Figure 6 : Pin 4 Configuration.



INPUT / OUTPUT PIN CONFIGURATION (continued)

Figure 7 : Pin 5 Configuration.

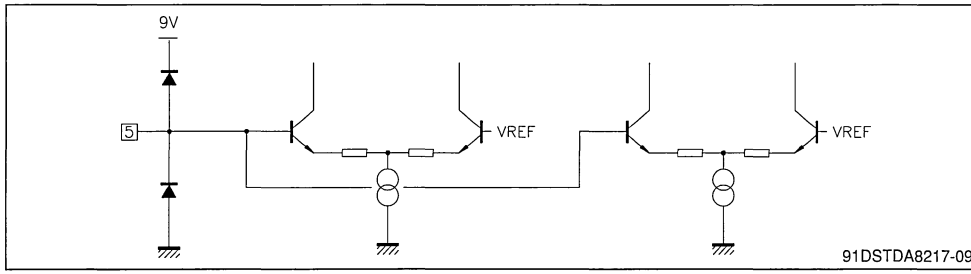


Figure 8 : Pin 6 Configuration.

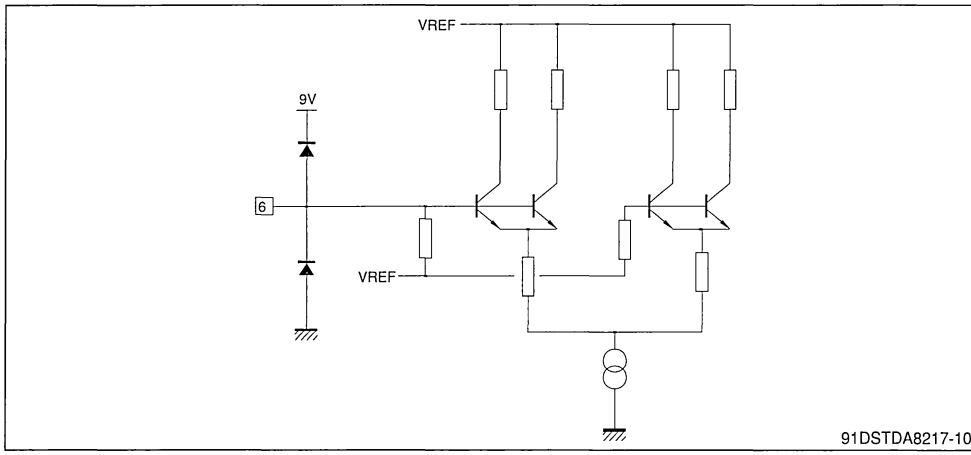


Figure 9 : Pin 8 Configuration.

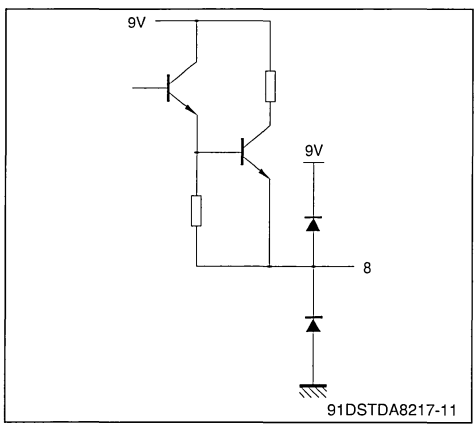
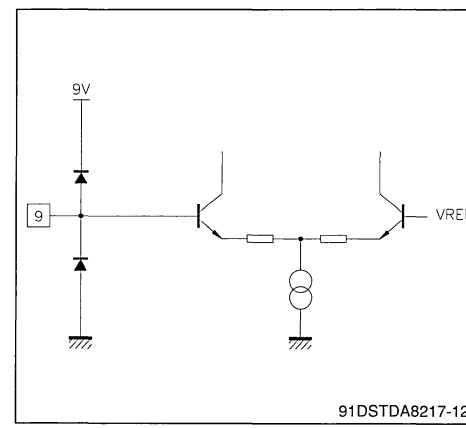


Figure 10 : Pin 9 Configuration.



INPUT / OUTPUT PIN CONFIGURATION (continued)

Figure 11 : Pin 10 Configuration.

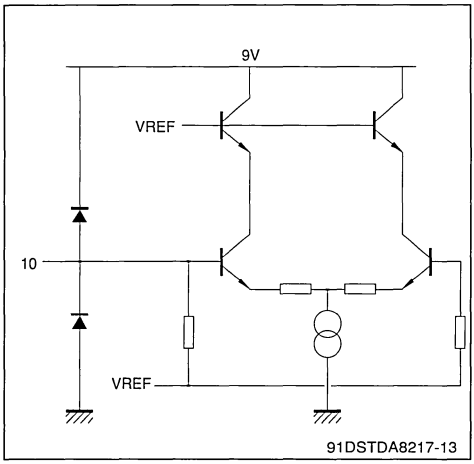


Figure 12 : Pin 12 Configuration.

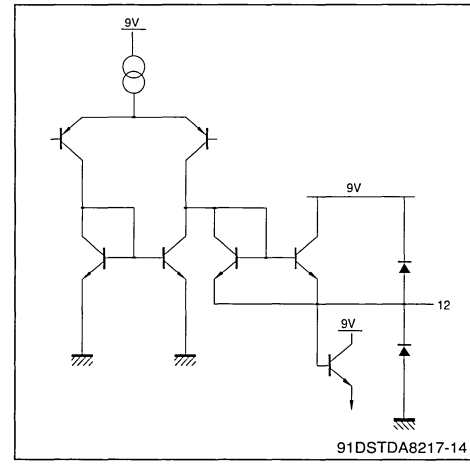


Figure 13 : Pin 13 Configuration.

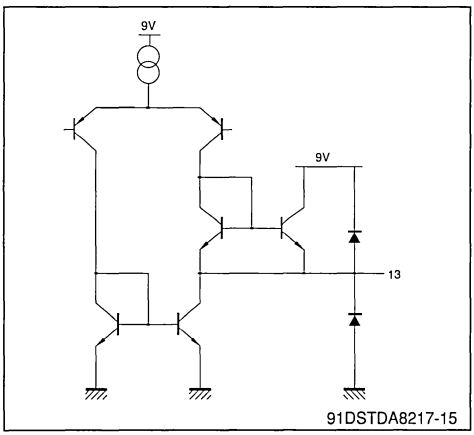


Figure 14 : Pin 14 Configuration.

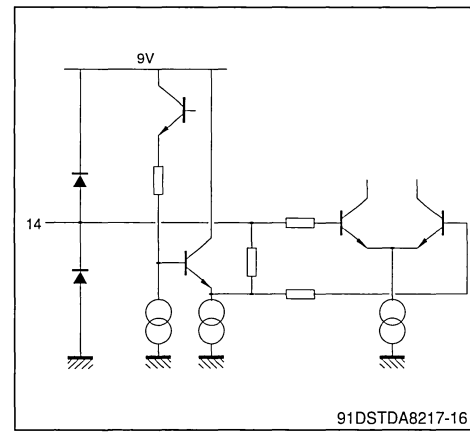


Figure 15 : Pin 16 Configuration.

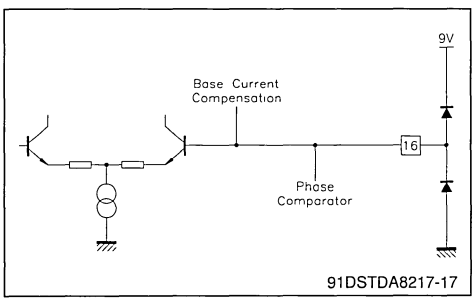
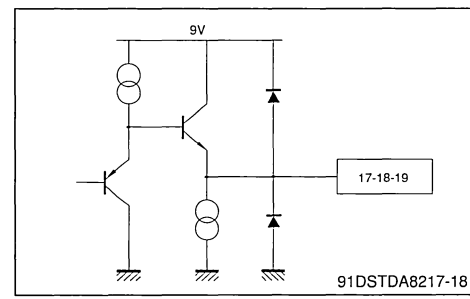
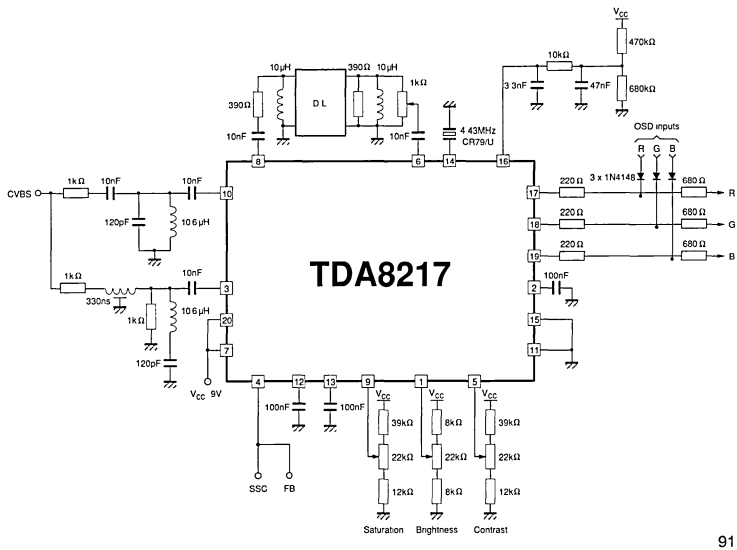


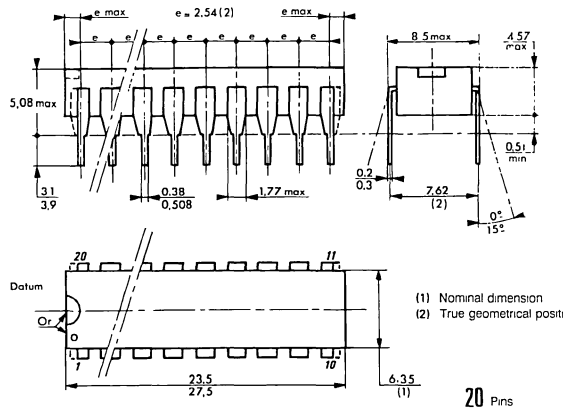
Figure 16 : Pins 17 - 18 - 19 Configuration.



APPLICATION DIAGRAM (with OSD capability)



PACKAGE MECHANICAL DATA : 20 Pins - Plastic DIP



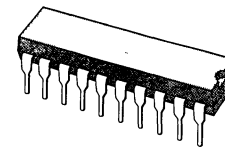
SGS-THOMSON MICROELECTRONICS

TDA8218

HORIZONTAL AND VERTICAL DEFLECTION CIRCUIT

ADVANCE DATA

- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- SUPER SANDCASTLE OUTPUT
- VERY FEW EXTERNAL COMPONENTS
- VERY LOW COST POWER PACKAGE
- STABLE FRAME BLANKING PULSE, GENERATED BY EXTERNAL RC, FOR COMPATIBILITY WITH TEA 5640



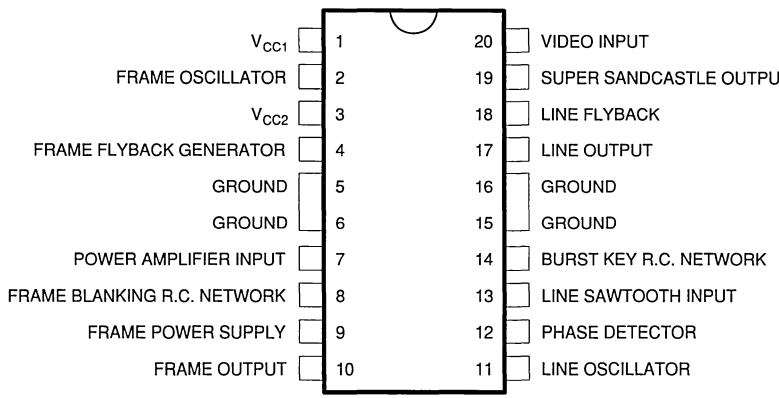
POWERDIP 16 + 2 + 2
(Plastic Package)

ORDER CODE : TDA8218

DESCRIPTION

The TDA8218 is an horizontal and vertical deflection circuit with super sandcastle generator. Used with automatic PAL/SECAM decoder TEA5640, this IC permits a complete low-cost solution for PAL/SECAM applications.

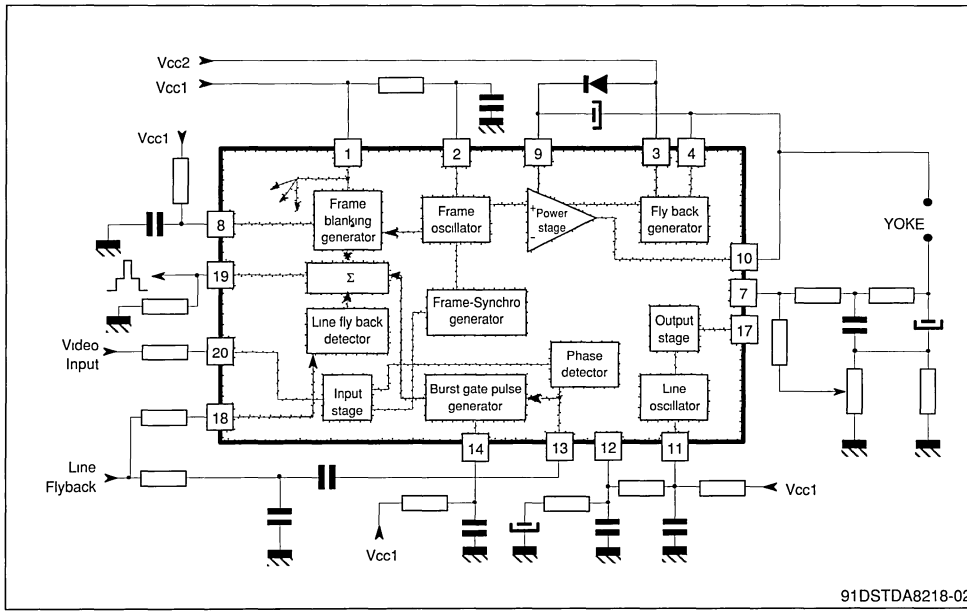
PIN CONNECTIONS



91DSTDA8218-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}1$	Supply Voltage	30	V
$V_{CC}2$	Flyback Generator Supply Voltage	35	V
V9	Frame Power Supply Voltage	60	V
$I10_{NR}$	Frame Output Current (non repetitive)	± 1.5	A
I10	Frame Output Current (continuous)	± 1	A
V17	Line Output Voltage (external)	60	V
I_P17	Line Output Peak Current	0.8	A
I_C17	Line Output Continuous Current	0.4	A
T_{STG}	Storage Temperature	-40 to + 150	°C
T_J	Max Operating Junction Temperature	+ 150	°C
T_{AMB}	Operating Ambient Temperature	0 to 70	°C

THERMAL DATA

$R_{TH(j-c)}$	Max Junction-case Thermal Resistance	10	°C/W
$R_{TH(j-a)}$	Typical Junction-ambient Thermal Resistance *(Soldered on a 35µm thick 45cm² PC Board copper area)*	40	°C/W
T_J	Max Recommended Junction Temperature	120	°C

ELECTRICAL CHARACTERISTICS

V_{CC1} = 10 V, T_{AMB} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (Pin 1)					
I_{CC1}	Supply Current		15		mA
V_{CC1}	Supply Voltage	9	10	10.5	V
VIDEO INPUT (Pin 20)					
V20	Reference Voltage (I20 = -1µA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (when synchronized with TTL signal)	50			µs
LINE OSCILLATOR (Pin 11)					
LT11	Low Threshold Voltage	2.8	3.2	3.6	V
HT11	High Threshold Voltage	5.4	6.6	7.8	V
BI11	Bias Current		100		nA
DR11	Discharge Impedance	1.0	1.4	1.8	kΩ
FLP1	Free Running Line Period (R = 34.9kΩ Tied to V_{CC1}, C = 2.2nF Tied to Ground)	62	64	66	µs
FLP2	Free Running Line Period (R = 13.7KΩ, C = 2.2nF)		27		µs
OT11	Oscillator Threshold for Line Output Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application)		2		Hz/°C
LINE OUTPUT (Pin 17)					
LV17	Saturation Voltage (I_{17} = 200mA)		1.1	1.6	V
OPW	Output Pulse width (line period = 64µs)	27	29	31	µs
LINE SAWTOOTH INPUT (Pin 13)					
V13	Bias Voltage	1.8	2.4	3.2	V
Z13	Input Impedance	4.5	5.8	8	kΩ
PHASE DETECTOR (Pin 12)					
I12	Output Current During Synchro Pulse	250	350	500	µA
RI12	Current Ratio (positive/negative)	0.95	1	1.05	
LI12	Leakage Current	-2		+2	µA
CV12	Control RangeVoltage	2.60		7.10	V
FRAME BLANKING GENERATOR (Pin 8)					
	External R.C. Network (Typical values : R = 100kΩ, C = 22nF)				
T_{fb}	Blanking Time (PIn 19, T_{fb} = K8 .R.C.)		1.35		ms
K8	Time Blanking Coefficient	0.588	0.613	0.644	
I_{O8}	Output Current during the Frame Blanking : V_8 = 2V		- 0.2	1	µA
I_{I8}	Input Current after the Frame Blanking : V_8 = 7V	300	450	600	µA
FRAME OSCILLATOR (Pin 2)					
LT2	Low Threshold Voltage	1.6	2.0	2.3	V
HT2	High Threshold Voltage	2.6	3.1	3.6	V
DIF2	LT2 - HT2		1.0		V
BI2	Bias Current		30		nA
DR2	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period (R = 866kΩ Tied to V_{CC}1, C = 220nF Tied to Ground)	20.5	23	25	ms
MFP	Minimum Frame Period (I20 = -100µA) with the Same RC		12.8		ms
FFP2	Free Running Frame Period(R = 408kΩ, C = 220nF)		14.3		ms
FPR	Frame Period Ratio = FFP/MFP	1.7	1.8	1.9	

ELECTRICAL CHARACTERISTICS (continued)

V_{CC1} = 10 V, T_{AMB} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME OSCILLATOR (Pin 2) (continued)					
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		-0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Frequency Drift with Temperature (see application)		4.10^{-3}		Hz/°C
FRAME POWER SUPPLY (Pin 9)					
V9	Operating Voltage (with flyback Generator)	10		58	V
I9	Supply Current (V9 = 30V)		11	22	mA
FLYBACK GENERATOR SUPPLY (Pin 3)					
V_{CC2}	Operating Voltage	10		30	V
FRAME OUTPUT (Pin 10)					
	Saturation Voltage to Ground (V9 = 30V)				
LV10A	I10 = 0.1A		0.06	0.6	V
LV10B	I10 = 1A		0.37	1	V
	Saturation Voltage to V9 (V9 = 30V)				
HV10A	I10 = -0.1A		1.3	1.6	V
HV10B	I10 = -1A		1.7	2.4	V
	Saturation Voltage to V9 in Flyback Mode (V10 > V9)				
FV10A	I10 = 0.1A		1.6	2.1	V
FV10B	I10 = 1A		2.5	4.5	V
FLYBACK GENERATOR (Pin 3 and Pin 4)					
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V4/3 with				
F2DA	$I_{4 \rightarrow 3}$ = 0.1A		1.5	2.1	V
F2DB	$I_{4 \rightarrow 3}$ = 1A		3.0	4.5	V
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V3/4 with				
FSVA	$I_{3 \rightarrow 4}$ = 0.1A		0.8	1.1	V
FSVB	$I_{3 \rightarrow 4}$ = 1A		2.2	4.5	V
	Flyback Transistor off (output = V9 - 8V), V9 - V_{CC2} = 30V				
FCI	Leakage Current Pin 3			170	µA
SUPER SANDCASTLE OUTPUT (Pin 19)					
	Output Voltages (R load = 2.2kΩ)				
SANDT2	Frame blanking pulse level	2	2.5	3	V
SANDL2	Line blanking pulse level	4	4.5	5	V
BG2	Burst key pulse level	8	9		V
	Pulses width and timing				
SC3	Delay between middle of sync pulse and leading edge of burst key pulse	2.3	2.7	3.1	µs
SC2	Duration of burst key pulse Vertical blanking pulse width : Defined by external R.C. Pin 8	3.7	4	5	µs
LINE FLYBACK INPUT (Pin 18)					
	Switching level		2		V
	Maximum imput current at V_{PEAK} = 800V		8		mA
	Limiting voltage at maximum current		4.3		V
τ	RC network time constant (Note 1) for the burst key pulse		6		µS

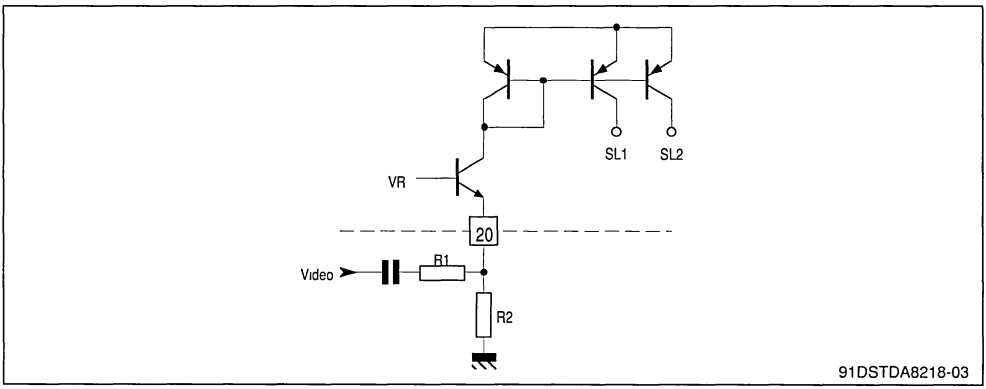
Note : 1. An RC network is connected to this input. Typical value for the resistor is 27kΩ and 220pF for the capacitor. A different time constant for RC changes the delay between the middle of the line synchro pulse and the leading edge of the burst key pulse but also the duration of the burst key pulse.

GENERAL DESCRIPTION

The TDA8218 performs all the video and power functions required to provide signals for the line driver and frame yoke.
It contains:

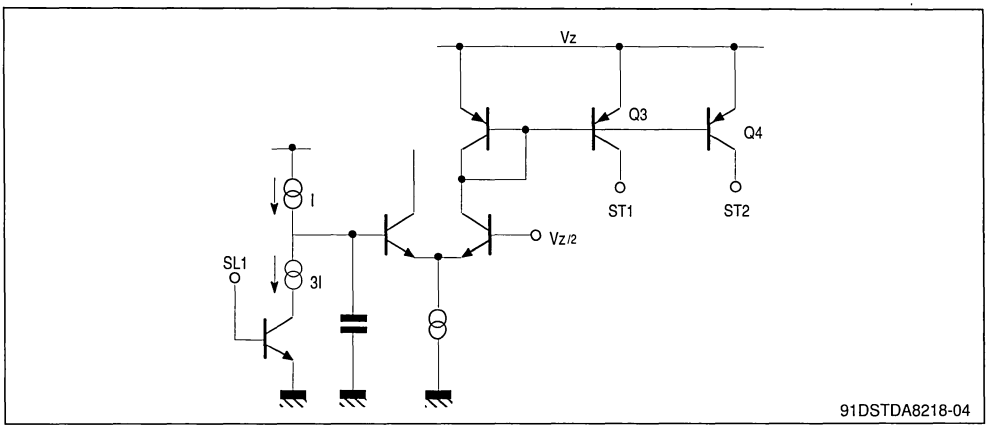
- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line driver
- A line phase detector and a voltage control oscillator
- A super sandcastle generator.

Figure 1 : Synchronization Separator Circuit



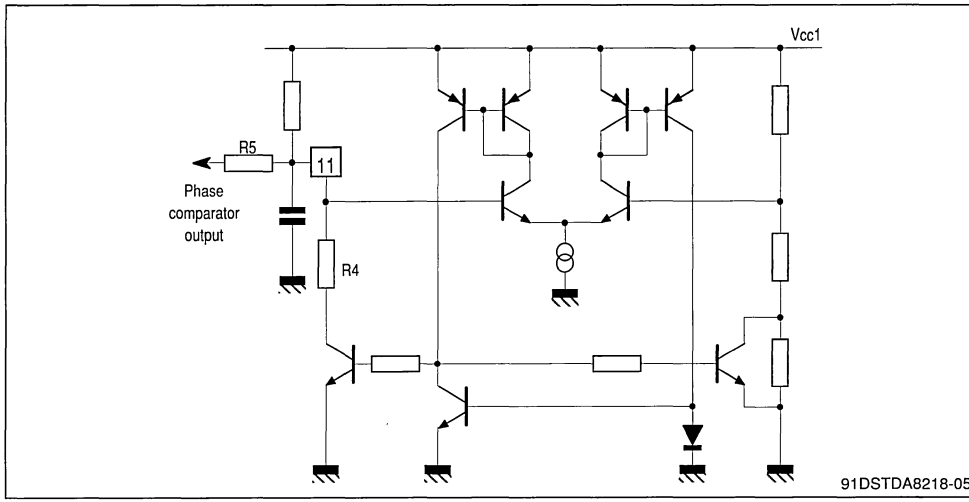
The slice level of sync-separation is fixed by value of the external resistors R1 and R2. V_R is an internally fixed voltage.

Figure 2 : Frame Separator



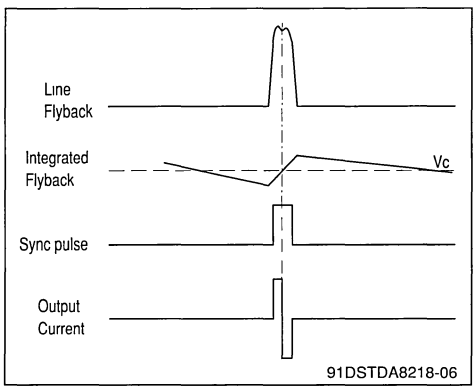
The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync-pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q_3 and Q_4 provide current for the other parts of the circuit.

Figure 3: Line Oscillator



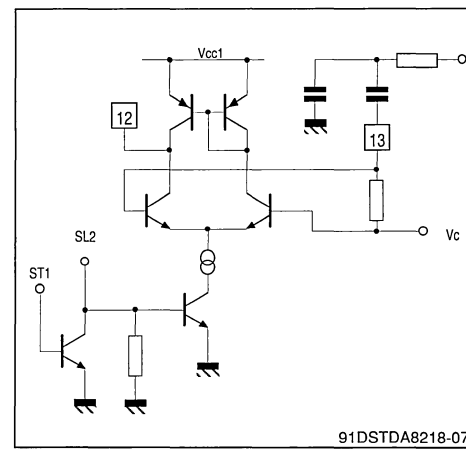
The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

Figure 4: Phase Comparator



The sync-pulse drives the current in the comparator. The line flyback integrated by the external net work gives on pin 13 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 13 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

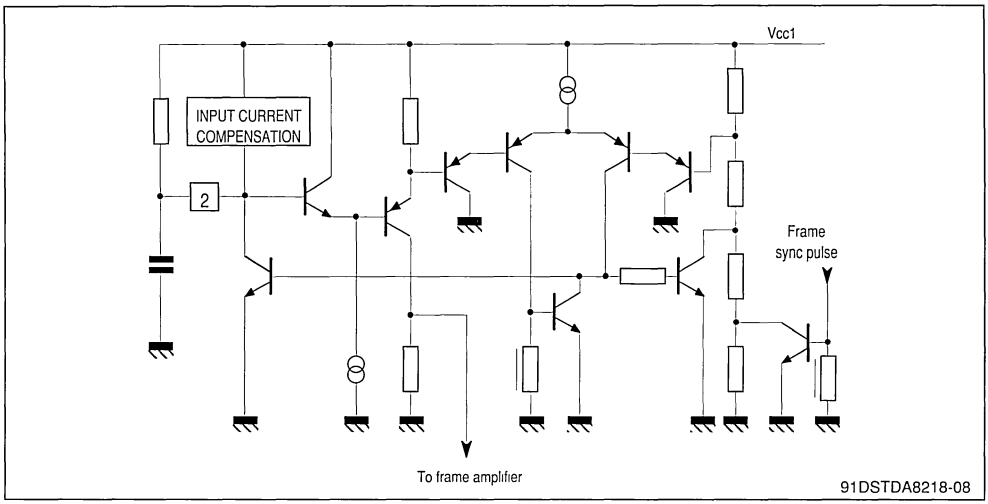
Figure 5



Line output (Pin 17)

It is an open-collector output. The output positive pulse time is 29µs for a 64µs period.

Figure 6: Frame Oscillator

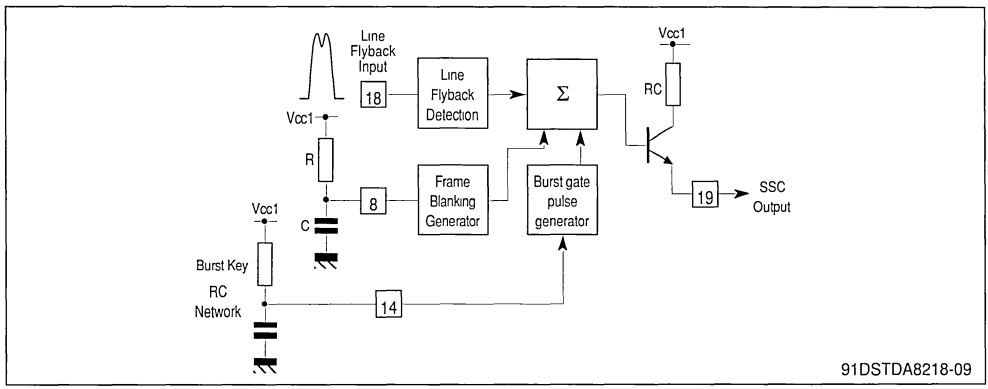


The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Frame output amplifier

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected; it contains also a thermal protection.

Figure 7: Super sandcastle generator



The line flyback detection is provided by a comparator which compares the input line flyback pulse to an internal reference. The burst gate pulse position is fixed by the external RC network (pin 14). It is referenced to the middle of the line flyback.

The frame blanking generator is a monostable with external R.C. The start blanking pulse is triggered by the falling edge of the frame saw-tooth (Pin 2). The reset is provided by a comparator which compares the capacitor voltage during its charge to an internal threshold fixed by resistors.

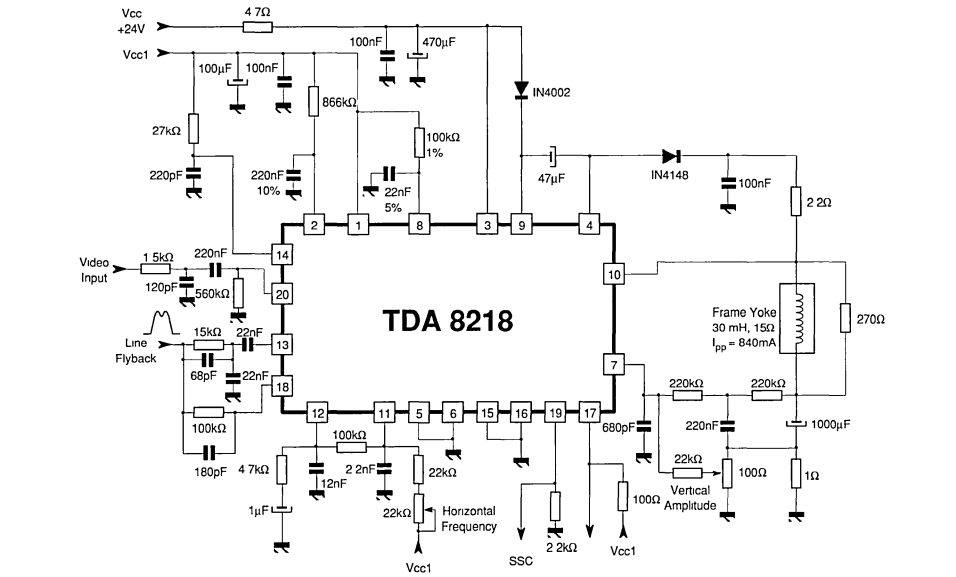
The frame blanking time is defined by :

$$T_{fb} = 0.613 \cdot R.C.$$

This pulse is available on Super Sand Castle output (Pin 19).

Remark : For compatability with TEA5640, frame blanking time must be larger than 1.15ms with centered value @ 1.35ms (R = 100kΩ ± 1%, C = 22nF ± 5%)

TYPICAL APPLICATION

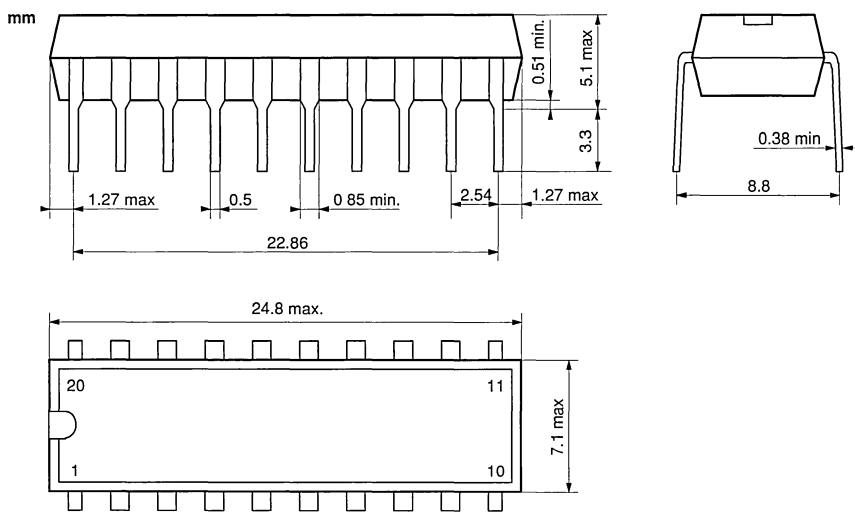


Note : Pins 5 - 6 : Frame oscillator ground
Pins 15 - 16 : Frame and line power ground

91DSTDA8218-10

PACKAGE MECHANICAL DATA

20 PINS - POWER DIP 16 + 2+ 2



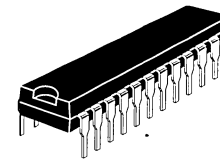
SGS-THOMSON MICROELECTRONICS

TDA8222

VIDEO & SOUND IF SYSTEM WITH VIDEO AND SOUND SWITCHES

PRELIMINARY DATA

- VERY LOW CURRENT ABSORPTION
- 3 STAGE IF GAIN CONTROLLED AMPLIFIER
- SYNCHRONOUS VIDEO DEMODULATOR
- WHITE SPOT AND NOISE INVERTER
- AGC CIRCUIT WITH NOISE GATING
- TUNER AGC OUTPUT FOR PNP TUNERS
- FM DETECTOR
- AF AMPLIFIER WITH DC VOLUME CONTROL
- AFC
- AUDIO AND VIDEO SWITCHES COMPATIBLE WITH SCART EUROPEAN NORM
- MUTE FUNCTION



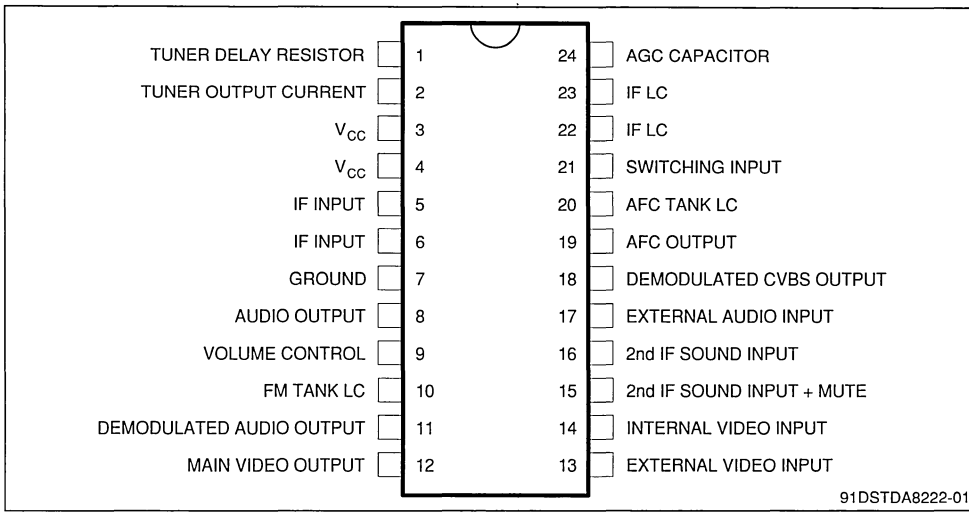
SHRINK DIP24
(Plastic Package)

ORDER CODE : TDA8222

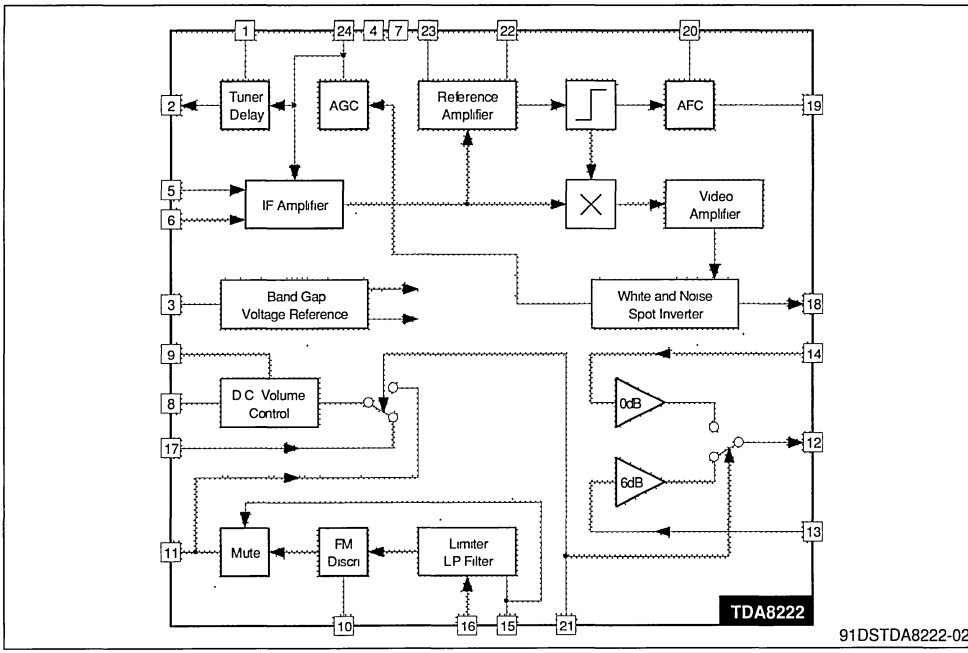
DESCRIPTION

The TDA8222 is a monolithic integrated circuit in Shrink DIP24 package for color and black & white television receivers using PNP tuners. It is intended to operate with a negatively modulated vision carrier and frequency modulated sound carrier.

PIN CONNECTIONS

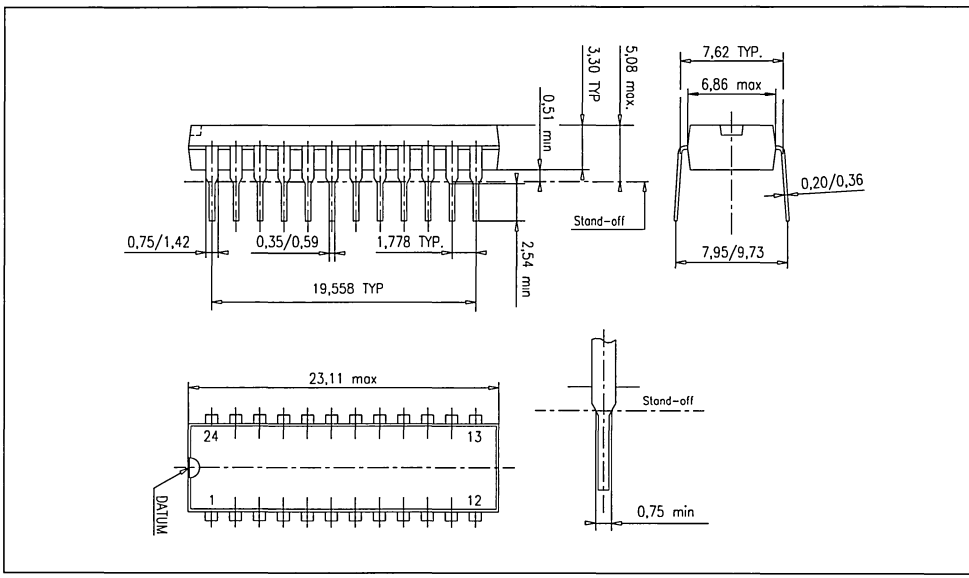


BLOCK DIAGRAM



PACKAGE MECHANICAL DATA

24 PINS - PLASTIC SHRINK



TDA9102B
TDA9102C

H/V PROCESSOR FOR TTL V.D.U

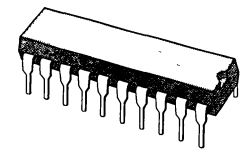
PRELIMINARY DATA

HORIZONTAL SECTION

- SYNCHRONIZATION INPUT : TTL COMPATIBLE, NEGATIVE EDGE TRIGGERED
- SYNCHRONIZATION INDEPENDENT FROM DUTY CYCLE TIME
- OSCILLATOR : FREQUENCY RANGE FROM 15kHz to 100kHz
- HORIZONTAL OUTPUT PULSE SHAPER AND SHIFTER
- PHASE COMPARATOR BETWEEN SYNCHRO AND OSCILLATOR (PLL1)
- PHASE COMPARATOR BETWEEN FLYBACK AND OSCILLATOR (PLL2)
- INTERNAL VOLTAGE REGULATOR
- DC COMPATIBLE CONTROLS FOR PHASE AND FREQUENCY
- DUTY CYCLE : 34% FOR TDA9102B
  43% FOR TDA9102C

VERTICAL SECTION

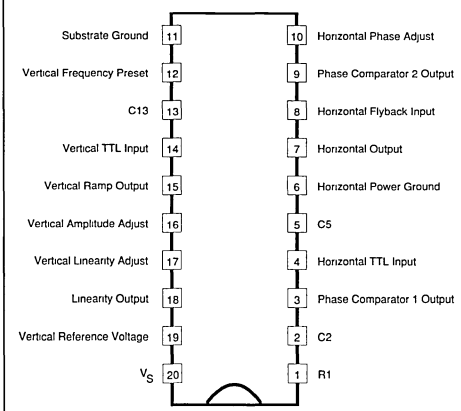
- SYNCHRONIZATION INPUT : TTL COMPATIBLE, NEGATIVE EDGE TRIGGERED
- SYNCHRONIZATION INDEPENDENT FROM DUTY CYCLE TIME
- OSCILLATOR : FREQUENCY RANGE FROM 30Hz to 120Hz
- RAMP GENERATOR WITH VARIABLE GAIN STAGE
- VERTICAL RAMP VOLTAGE REFERENCE
- INTERNAL VOLTAGE REGULATOR



DIP20
(Plastic package)

ORDER CODES : TDA9102B / TDA9102C

PIN CONNECTIONS



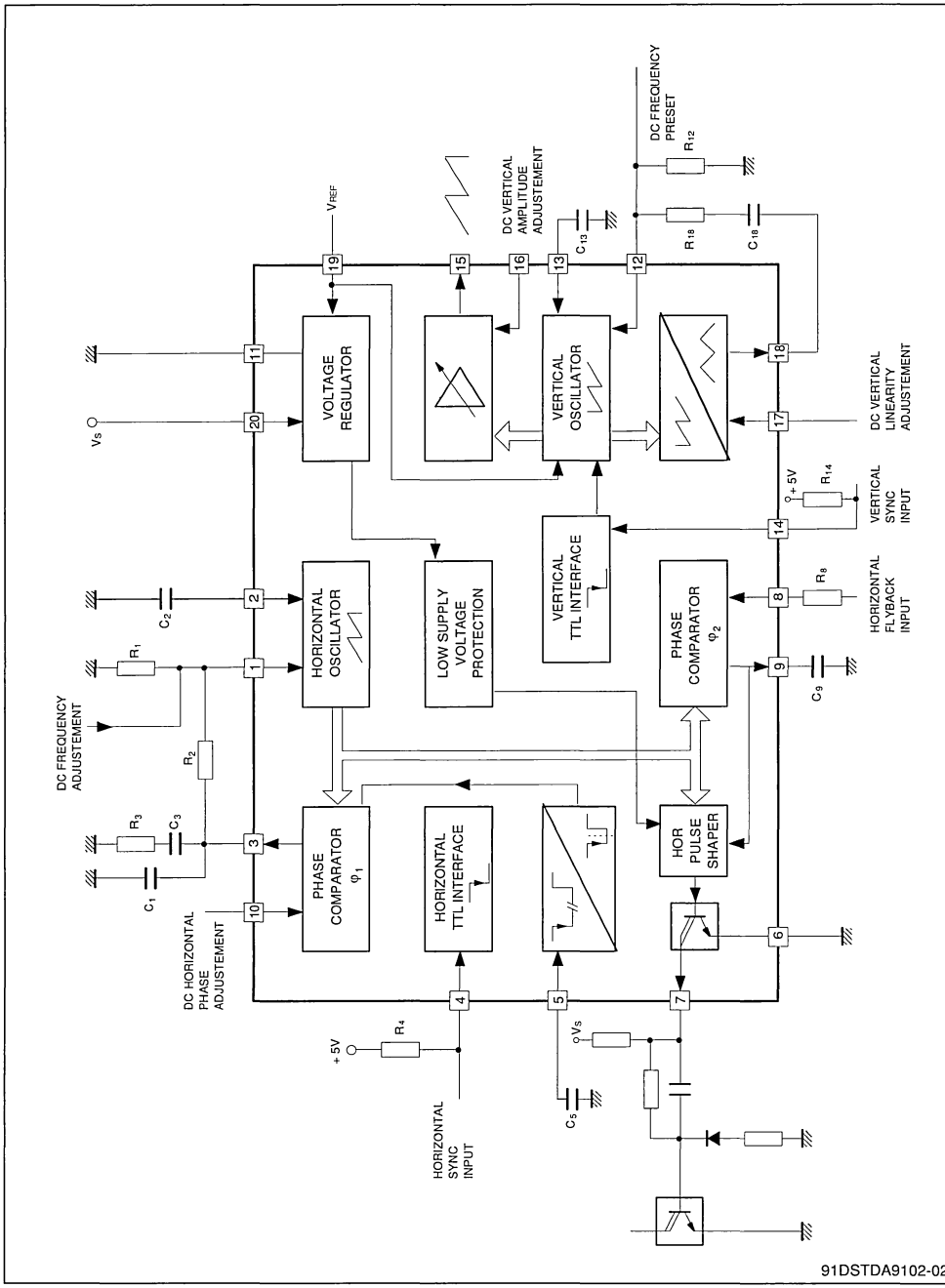
91DSTDA9102-01

DESCRIPTION

The TDA9102B, C is a monolithic integrated circuit for horizontal and vertical sync processing in monochrome and color video displays driven by input TTL compatible signals.

The TDA9102B, C is supplied in a 20 pin dual in line package with pin 11 connected to ground and used for heatsinking.

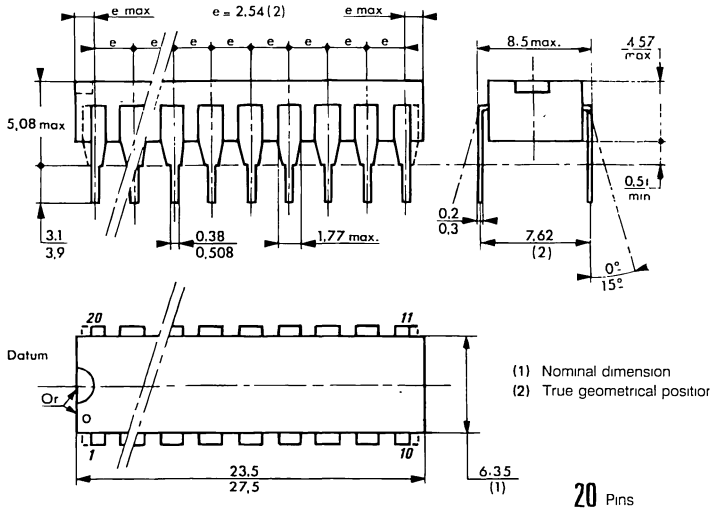
BLOCK DIAGRAM



91DSTDA9102-02

PACKAGE MECHANICAL DATA

20 PINS - PLASTIC DIP

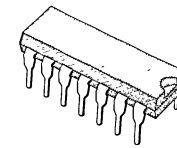


SGS-THOMSON MICROELECTRONICS

TEA1014

VIDEO AND AUDIO SIGNALS SWITCHING FOR THE PERI-TELEVISION PLUG

- VIDEO CROSSTALK : 60 dB TYPICAL
- LOW IMPEDANCE VIDEO OUTPUT 75 Ω
- SHORT-CIRCUIT PROTECTION OF INPUTS AND OUTPUTS
- INTERNAL HORIZONTAL PLL TIME CONSTANT SWITCHING IN CASE OF VIDEO RECORDER RECEPTION



DIP14
(Plastic Package)

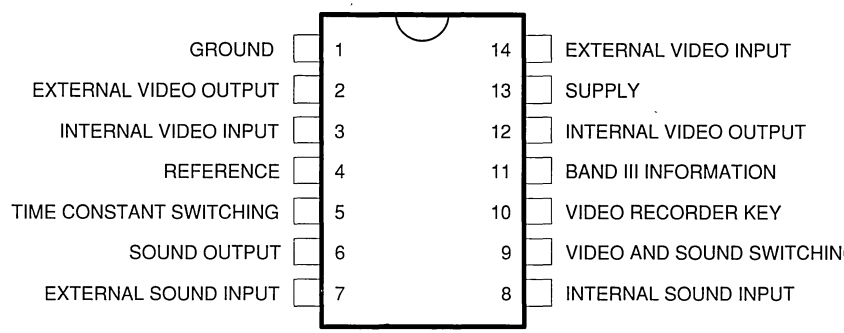
ORDER CODE : TEA1014

DESCRIPTION

This integrated circuit provides both video and sound switching allowing connections between the peri-TV plug and video, sound sections in the TV set.

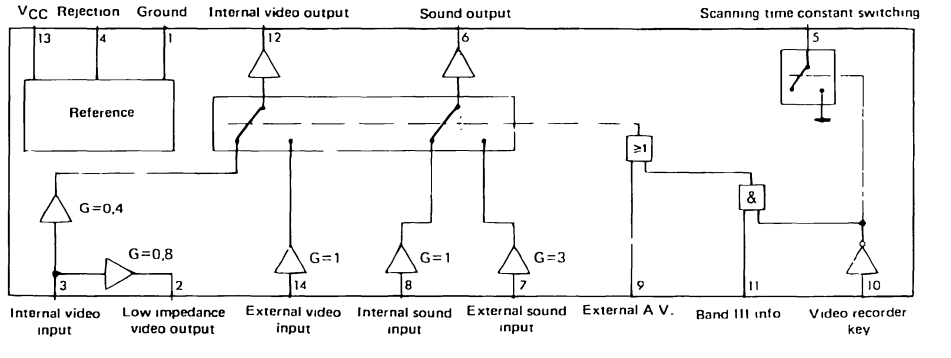
Input and output signal characteristics follow the NFC 92250/EN 50049 norms.

PIN CONNECTIONS



91DSTEA1014-01

BLOCK DIAGRAM



88DSTEA1014-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
T_{stg}	Storage Temperature Range	– 40, + 150	°C
T_j	Junction Temperature	+ 150	°C
T_{oper}	Operating Ambient Temperature Range	0 to 70	°C

TAB-01

THERMAL DATA

$R_{th(j-a)}$	Junction Ambient Thermal Resistance	90	°C/W

TAB-02

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 12 V ; T_{amb} = + 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Supply Current, with no Load		37	50	mA
	Internal Video Input (coming from picture IF) (pin 3) Video Signal Amplitude (positive video) Input Voltage Range (refered to D. C. input Voltage) Input Impedance Input Capacitance	 – 2.9 5	 2.5 	 6.8 + 3.9 5	 Vpp V kΩ pF
	External Video Input (coming from peri-TV plug) (pin 14) Video Signal Amplitude (positive video) Input Voltage Range (refered to D. C. input Voltage) Input Impedance Input Capacitance	 – 1.2 5	 1 	 2.8 + 1 6 5	 Vpp V kΩ pF
	TV Video Output (pin 12) Signal Amplitude Output Voltage Swing (refered to D. C. output Voltage) Output Dynamic Impedance D.C. Output Voltage (without input signal) Loading Resistance Video Bandwidth (– 1 dB)	 – 1.2 300 6	 1 3.5 	 2.8 + 1.6 10 	 Vpp V Ω V Ω MHz

TAB-03

ELECTRICAL OPERATING CHARACTERISTICS (continued)

V_{CC} = 12 V ; T_{amb} = + 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Gain/internal Video	− 9 5	− 8	− 6.5	dB
	Gain/external Video	− 1.5	0	+ 1.5	dB
	External Video Output (low impedance) (pin 2)				
	Signal Amplitude (on 150 Ω grounded)		2	5.5	Vpp
	Output Voltage Swing	− 2.4		+ 3.1	V
	Dynamic Output Impedance		10		Ω
	D.C. Output Voltage (without input signal)		3.5		V
	Minimum Loading Resistance (electrical performance non specified)	75			Ω
	Gain/internal Video	− 3.5	− 2	− 0.5	dB
	Output Video Signals Characteristics				
	Video Rejection between two Inputs (1 MHz)	− 55			dB
	Differential Group Delay			20	ns
	Linearity Distortion				
	Luma (test line 17)		2		%
	Chroma (test line 331)		2		%
	Intermodulation Luma–chroma (test line 331)		5		%
	Supply Voltage Rejection	45			dB
	Internal Sound Input (pin 8)				
	Input Signal		0.3	2	V_{RMS}
	Input Impedance		20		kΩ
	External Sound Input (pin 7)				
	Input Signal		0.1	0.7	V_{RMS}
	Input Impedance		20		kΩ
	Sound Output (pin 6)				
	Output Signal Amplitude		0.3		V_{RMS}
	Output Voltage Swing		2		V_{RMS}
	Distortion (V_O = 0.6 V_{eff})			0.5	%
	Bandwidth	16			kHz
	Output Impedance		40		Ω
	Load Impedance	2			kΩ
	Gain/internal Input	− 1.5	0	+ 1.5	dB
	Gain/external Input	8	9.5	11	dB
	Supply Voltage Rejection	60			dB
	Crosstalk	− 57			dB
	Video/sound Crosstalk	− 60			dB
	LOGIC				
	External A. V. Input (peri-TV plug) (pin 9)				
	Unactive Low Level or Unconnected Pin (logic state 0) – (TV receiving)	0		3	V
	Active High Level (logic state 1) (ext. receiving)	9		V_{CC}	V
	Input Impedance		10		kΩ
	"Band III" Input (pin 11)				
	Unactive Low Level or Unconnected Pin (logic state 0)	0		+ 3	V
	Active High Level (logic state 1)	9		V_{CC}	V
	Input Impedance High Level		10		kΩ
	Input Current Low Level			1	µA
	Video–recorder Key Input (pin 10)				
	Unactive High Level or Unconnected Pin (logic state 1)	9		V_{CC}	V
	Active Low Level (logic state 0)	0		3	V
	Input Impedance		10		kΩ
	Open Collector Output (time-constant switching) (pin 5)				
	Leakage Current (open collector)			1	µA
	Maximum Low Level Voltage (I(5) = 4 mA)			1.5	V

TAB-04

CIRCUIT DESCRIPTION

The main functions of the I.C. are following :

VIDEO SWITCHING

2 electronically switched inputs :

- one 2.5 Vpp input for internal video.
- one 1 Vpp input for signal coming from the peri-TV plug.

2 outputs :

- 1 Vpp output (low impedance 75 Ω) for peri-TV plug.
- 1 Vpp output low impedance for video section of the TV set.

Each input and output is protected from ground short-circuit. The 75 Ω output is protected through a 75 Ω resistor.

AUDIO SWITCHING

Two electronically switched inputs :

- 300 mV rms input coming from internal audio.
- 100 mV rms input coming from the peri-TV plug one low impedance output 300 mV rms.

Inputs and outputs are also protected against ground short-circuit.

SWITCHING LOGIC

The logic takes into account the information on 3 pins.

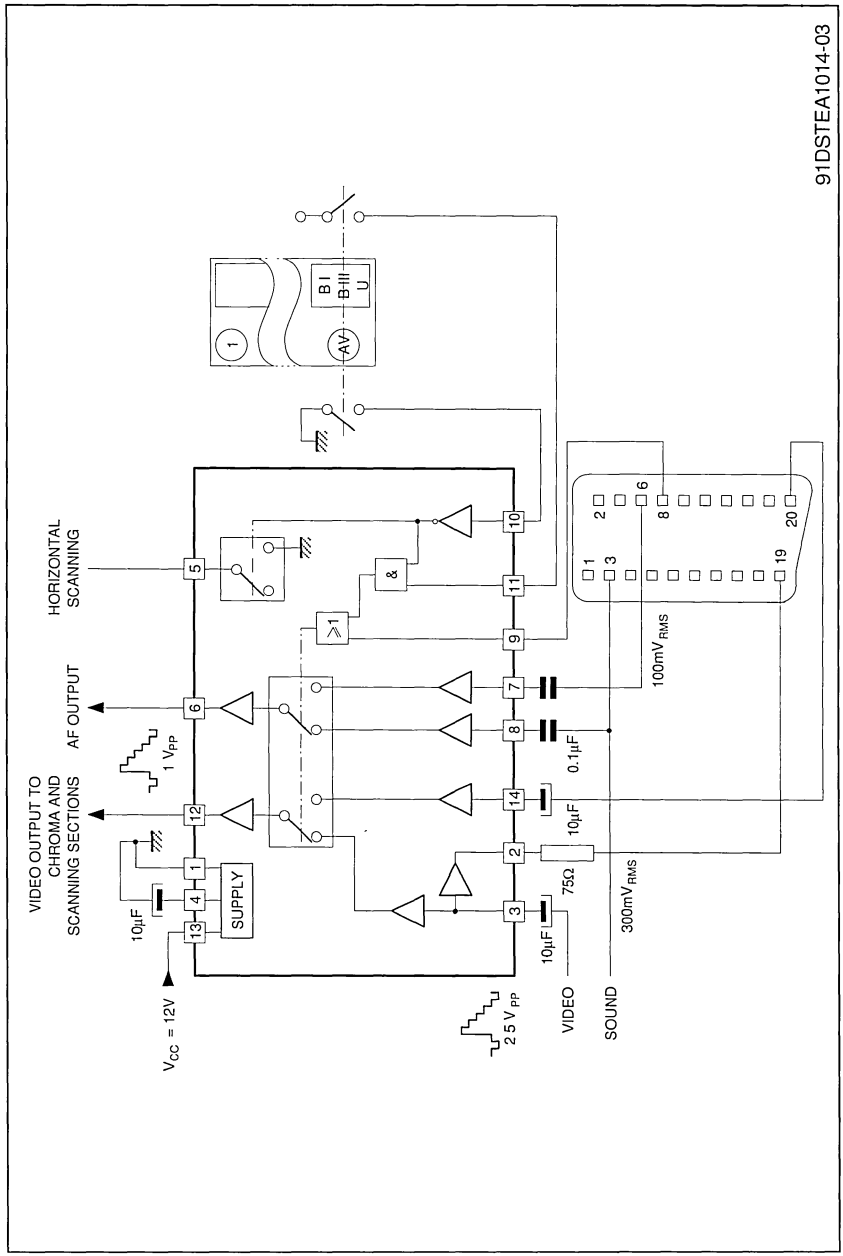
- Internal or external video and sound (pin 8 peri TV plug)
- Band III information
- Video recorder key.

External Video and Audio signals are selected in two cases.

- When there is a voltage information coming from peri-TV plug.
- When the video recorder key is selected (on TV front panel) and programmed on band III.

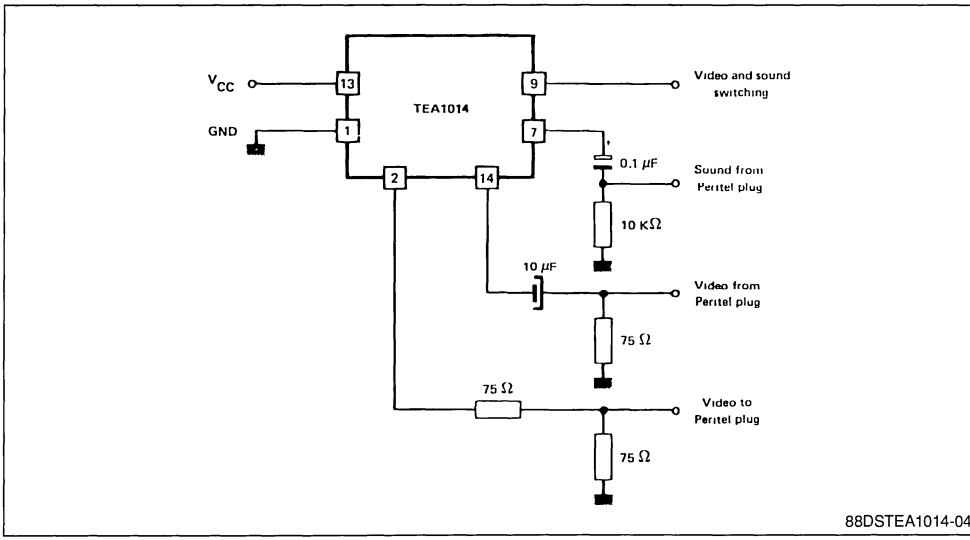
This I.C. includes an internal switch (open collector transistor) which commutes the time constant of the horizontal PLL circuit in case of video recorder reception.

APPLICATION CIRCUIT

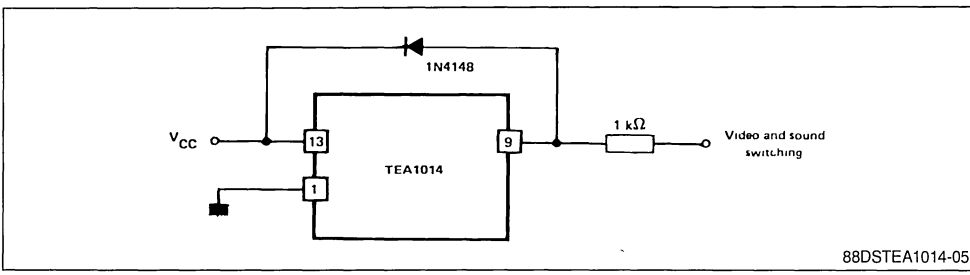


SAFETY INFORMATION FOR CRITICAL APPLICATIONS

Typical Connection Between Peritel Plug and TEA1014.

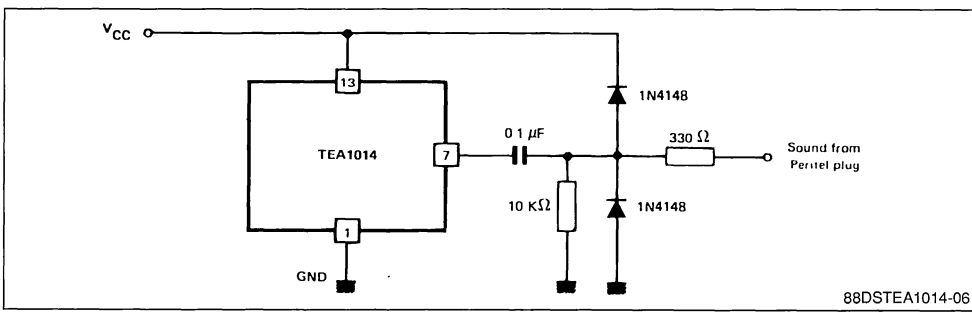


Voltage on pin 9 must not exceed the V_{CC} voltage on pin 13. In case of risk of over voltage, use the protection as described as below s :



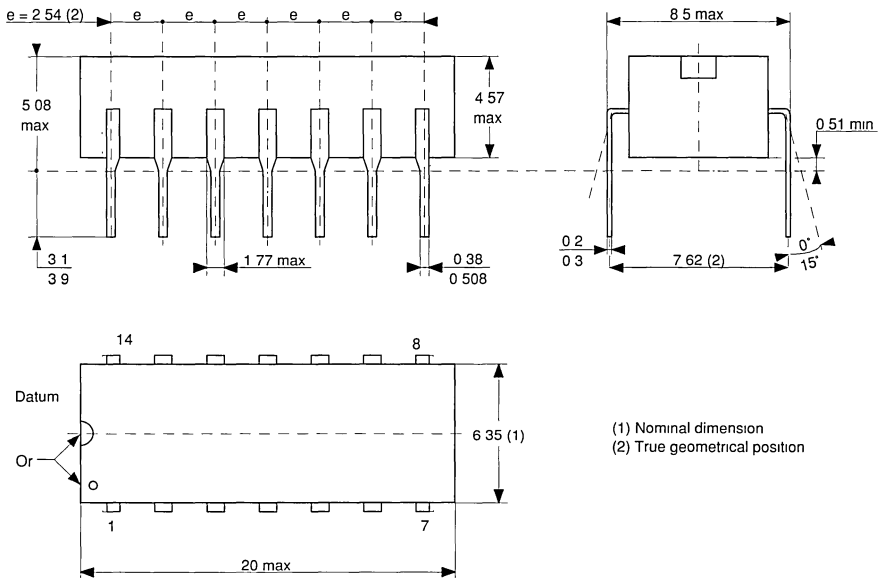
All connections to Peritel plug are terminated by low impedance loads (75 Ω), except the external sound input.

In case of risk of electrostatic discharge, use the protection as described as below.



PACKAGE MECHANICAL DATA

14 PINS – PLASTIC DIP

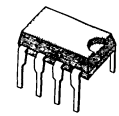


SGS-THOMSON MICROELECTRONICS

TEA2014A

VIDEO SWITCH

- 1 VIDEO OUTPUT 75 Ω- 1 V_{PP} NOT SWITCHED
- 1 SWITCHED VIDEO OUTPUT 2 V_{PP}
- VIDEO CROSSTALK : 50 dB TYPICAL
- SHORT CIRCUIT PROTECTION OF INPUTS AND OUTPUTS
- CLAMPED VIDEO INPUTS



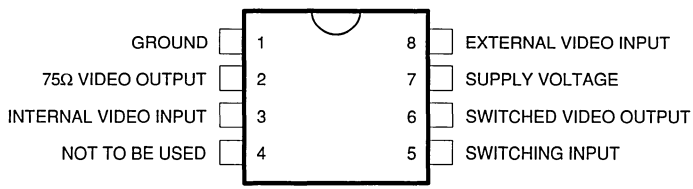
DIP8
(Plastic package)

ORDER CODE : TEA2014A

DESCRIPTION

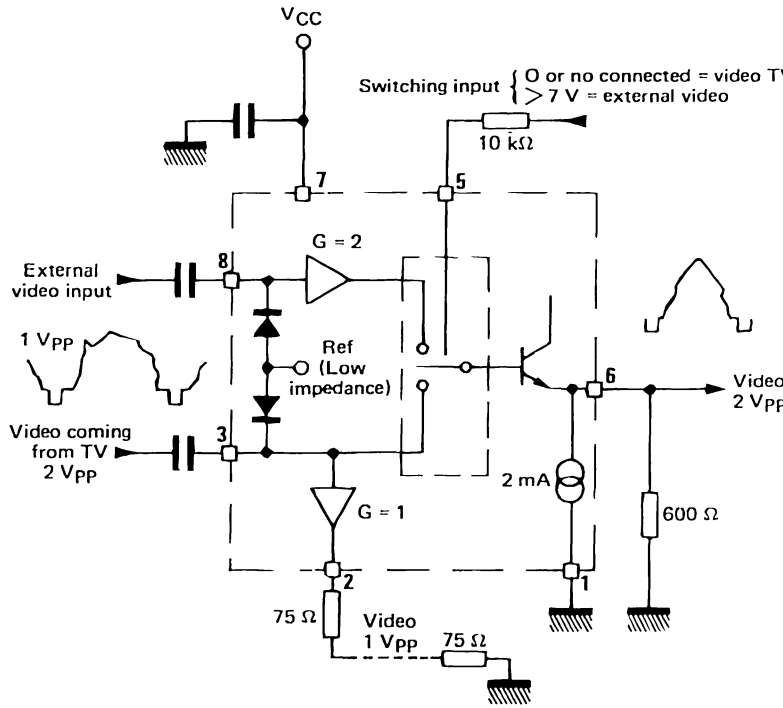
This integrated circuit provides all video switching allowing connections between the peri TV plug and video sections in the TV set. The TEA2014A is supplied in a DIL8.

PIN CONNECTIONS



91DSTEA2014A-01

TYPICAL APPLICATION AND TEST CIRCUIT



We advice to protect the 75 Ω output through a 75 Ω resistor for supply voltage higher than 9 V.

88DSTEA2014A-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
T_{oper}	Operating Temperature with Load > 150 Ω on PIN 2 with Load = 75 Ω on PIN 2	 0, + 100 0, + 70	°C
T_j	Junction Temperature	− 40, + 150	°C
T_{stg}	Storage Temperature	− 40, + 150	°C
−	Minimum DC Load Resistor PIN 6 Minimum DC Load Resistor PIN 2	600 75	Ω Ω

TAB-01

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	90 Typ	°C/W

TAB-02

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C, V_{CC} = 9 V (unless otherwise specified)

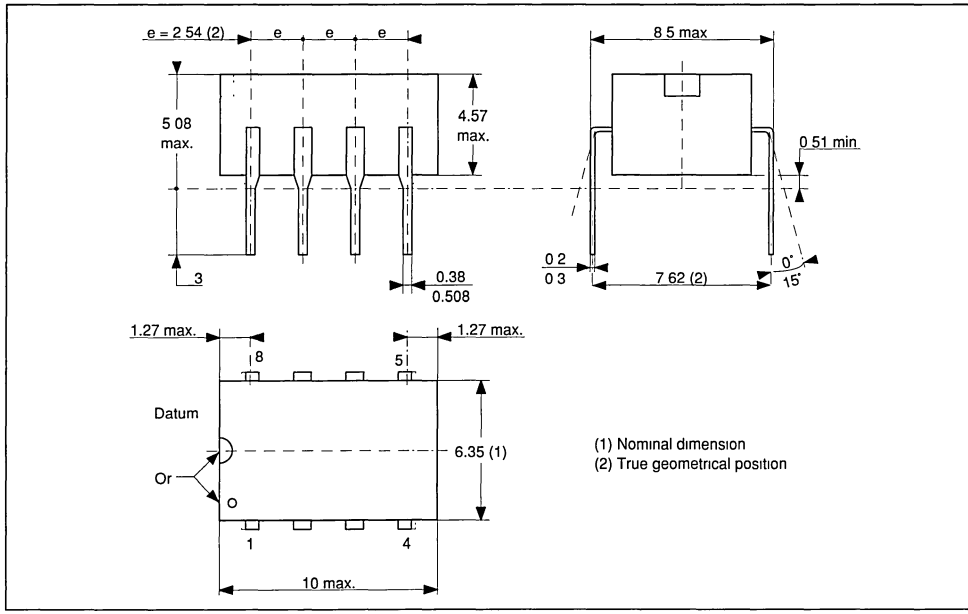
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range	8	–	14	V
I_{CC}	Supply Current (no load on pin 2 and pin 6)	–	–	20	mA
I_{CC}	Supply Current (with 75 Ω pin 2.1, with 600 Ω between pin 6.1)	–	45	–	mA
P_{tot}	Total Power Dissipation with Load	–	400	–	mW
INPUTS (pin 8 and pin 3)					
–	Internal Video Input Swing from Picture IF (positive Video)	–	–	4.5	Vpp
–	Internal Video Input Impedance (positive video)	50	–	–	kΩ
–	Internal Video Input Bias Current (positive video)	6	25	40	µA
–	External Video Input Swing (positive video)	–	–	2	Vpp
–	External Video Input Impedance (positive video)	50	–	–	kΩ
SWITCHED OUTPUT (pin 6) - R_{LOAD} = 600 Ω					
–	Video Output Swing	4	–	–	Vpp
–	Video Output Dynamic Impedance	–	–	25	Ω
–	Video DC Output Voltage (sync. pulse level note 1)	1.7	2	2.4	V
–	Video Bandwith Pin 6 – from Internal Input pin 3 (– 1 dB)	6	–	–	MHz
–	Video Bandwith Pin 6 – from External Input Pin 8 (– 3 dB)	6	–	–	MHz
–	Output Gain Pin 6 – Pin 8	+ 5	+ 6	+ 7	dB
–	Output Gain Pin 6 – Pin 3	– 1	– 0.5	0	dB
EXTERNAL OUTPUT (pin 2) - R_{LOAD} = 75 Ω					
–	Video Output Swing	2.2	–	–	Vpp
–	Video Output Dynamic Impedance	–	10	–	Ω
–	Video DC Output Voltage (sync. pulse level , note 1)	1.7	2	2.4	V
–	Video Bandwidth (– 1dB)	6	–	–	MHz
–	Video Output Gain (pin 2 – pin 3)	– 1.8	– 1	– 0.4	dB
SWITCHING INPUT (pin 5)					
–	Switching Input Unactive Low Level or Unconnected Pin (TV receiving)	0	–	3	V
–	Switching Input Active Level (ext. receiving)	7	–	V_{CC}	V
–	Switching Input Impedance	10	–	–	kΩ
OTHER DYNAMIC FEATURES					
–	Video rejection Between Two Inputs 1MHz 1kHz	 – – 50	 – 50 –	 – –	 dB dB
–	Linearity Distortion Luma (test line 17) Chroma (test line 331) Intermodulation Luma – Chroma (test line 331)	 – – –	 2 2 5	 – – –	 % % %
–	Supply Voltage Rejection (1 kHz)	40	50	–	dB

TAB-03

Note : 1. Use a video signal with a synchro pulse in order to make the clamp work in a correct way. (75 Ω to the ground and 10 µF in series)

PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

TEA2028B

COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

DEFLECTION :

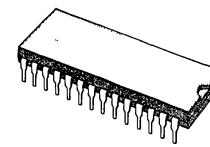
- CERAMIC 500kHz RESONATOR FREQUENCY REFERENCE
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT REFERENCE
- DUAL PLL FOR LINE DEFLECTION
- HIGH PERFORMANCE SYNCHRONIZATION
- SUPER SANDCASTLE OUTPUT
- FRAME BLANKING WITH SAFETY CIRCUIT
- VIDEO IDENTIFICATION CIRCUIT
- AUTOMATIC 50/60Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL
- SPECIAL PATENTED FRAME SYNCHRO DEVICE FOR VCR OPERATION
- FRAME SAW-TOOTH GENERATOR

SMPS CONTROL :

- ERROR AMPLIFIER AND PHASE MODULATOR
- SYNCHRONIZATION WITH HORIZONTAL DEFLECTION
- SECURITY CIRCUIT AND START-UP PROCESSOR
- OUTPUT PULSES ARE SENT TO THE PRIMARY SMPS IC (TEA2260 or TEA2164) THROUGH A LOW COST SYNCHRO PULSE TRANSFORMER

DESCRIPTION

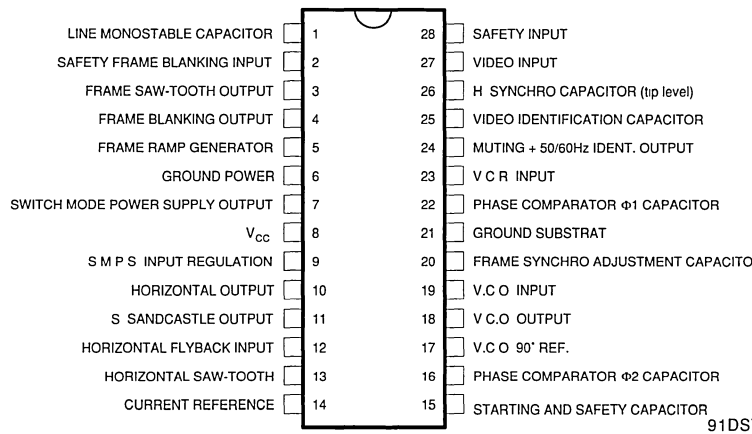
The TEA2028B is a complete (horizontal and vertical) deflection processor with secondary to primary SMPS control for color TV sets.



DIP28
(Plastic Package)

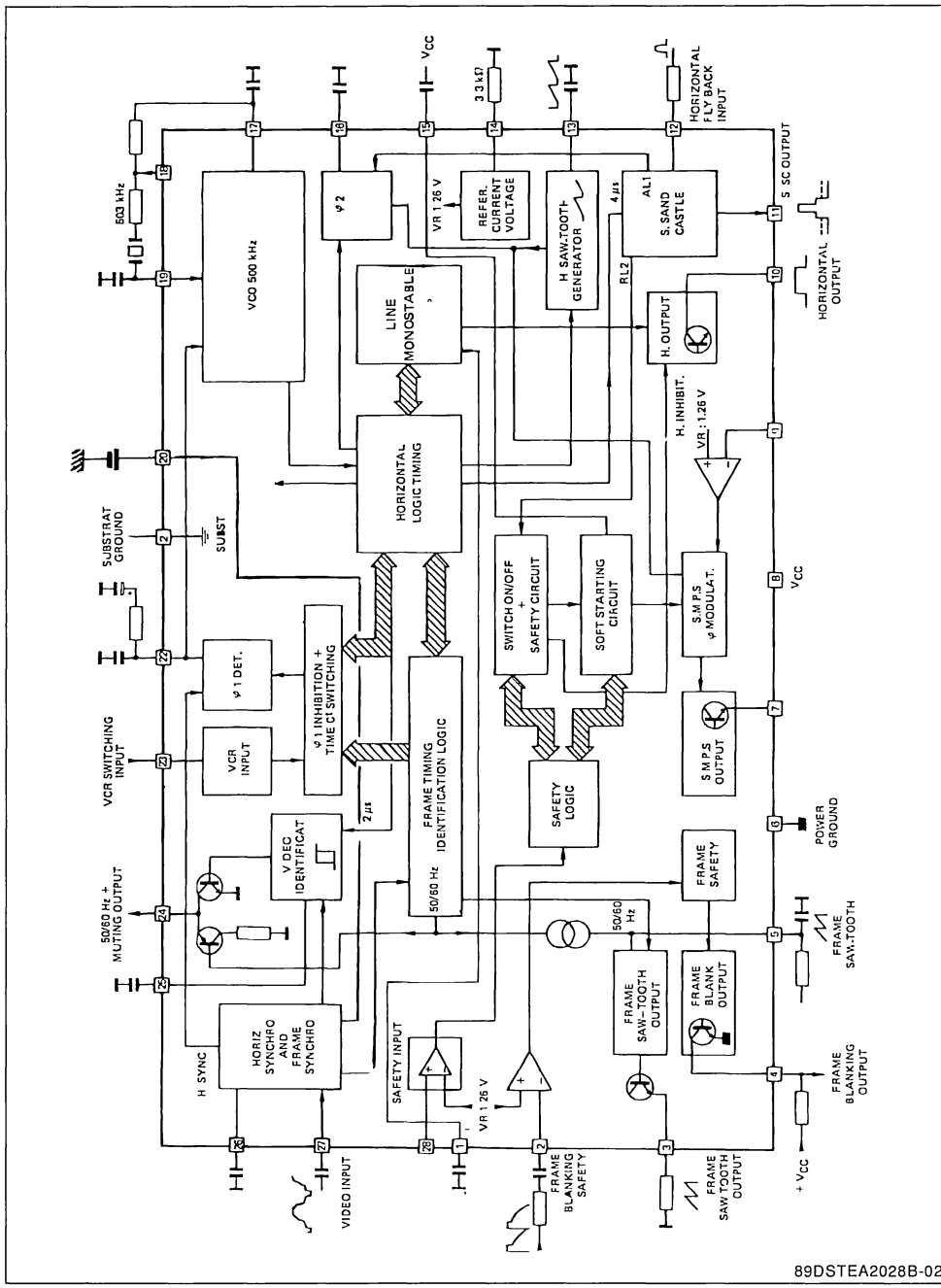
ORDER CODE : TEA2028B

PIN CONNECTIONS



91DSTEA2028B-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (limiting values)
(T_{amb} = 25°C unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit
	Supply Voltage (pin 8)		14	V
V_{CC}	Operating Supply Voltage (pin 8)	Starting threshold	13.2	V
I_{24}	Video Identification Current (pin 24)		10	mA
V_{12}	Positive voltage (pin 12)	− 5		V
I_{12}	Line retrace current (pin 12)		+ 10	mA
I_{10}	Line Output Current (pin 10)	− 10	40	mA
I_3	Frame Saw-tooth Generator (pin 3)		20	mA
I_4	Frame Blanking Input Current (pin 4)		100	mA
I_7	SMPS Output Current (pin 7)	− 40		mA
I_{28}	Safety Input Current (pin 28)		5	mA
V_{28}	Safety Input Voltage (pin 28)		V_{CC}	

TAB-01

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	55	°C/W

TAB-02

GENERAL DESCRIPTION

INTRODUCTION

This integrated circuit uses I^2L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500kHz by means of a cheap ceramic resonator. This avoids the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produce very accurately defined sampling pulses and the necessary timing signals.

The principal functions implemented are :

- Horizontal scanning processor.
- Frame scanning processor.
  - B Class Power stage using an external power amplifier with fly back generator such as the TDA8170.
- Secondary switch mode power regulation.
- The SMPS output synchronize a primary I.C. (TEA2260 or TEA2164) at the mains part.
- This concept allows ACTIVE STANDBY facilities.
- Line and frame synchronization separation.
- Dual phase-locked loop horizontal scanning.
- High performance frame and line synchronization with interlacing control.
- Video identification circuit.
- Super sandcastle.
- Automatic 50-60Hz standard identification.
- VCR input for PLL time constant and frame synchro switching.
- Frame saw-tooth generator.
- Frame blanking output.
- Switching mode regulated power supply comprising error amplifier and phase modulator.
- Security circuit and start-up processor.
- 500KHz VCO.

The circuit is supplied in a 28 pin DIP case.

V_{CC} = 12V.

SYNCHRONIZATION SEPARATOR

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.

The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signals in noise conditions.

FRAME SYNCHRONIZATION

Time constant of Frame Separator can be adjusted by adding a capacitor pin 20.

The frame timing identification logic permits automatic adaptatio to 50 - 60Hz standards or non-interlaced video.

An automatic synchronization window width system provides :

- fast frame capture (6.7ms wide window),
- good noise immunity (0.4ms narrow window).

The internal generator starts the discharge of the saw-tooth generator capacitor so that it is not disturbed by line fly-back effects.

Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line fly-back.

A 32µs timing is automatically applied on standardized transmissions, for perfect interlacing.

In VCR mode, the discharge time is controlled by an internal monostable independent of the line frequency and gives a direct frame synchronization.

HORIZONTAL SCANNING

The horizontal scanning frequency is obtained from the 500KHz VCO.

The circuit uses two phase-locked loops (PLL) :

the first one controls the frequency, the second one controls the relative phase of the synchronization and line fly-back signals.

The frequency PLL has two switched time constants to provide :

- capture with a short time constant,
- good noise immunity after capture with a long time constant.

The output pulse has a constant duration of 29µs (with C(pin 1) = 3.3nF), independent of V_{CC} and delay in switching off the scanning transistor.

VIDEO IDENTIFICATION

The horizontal synchronization signal is sampled by a 2µs pulse within the synchronization pulse. The signal is integrated by an external capacitor.

The identification function provides three different levels :

- 0V : no video identification
- 6V : 60Hz video identification
- 12V : 50Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers and for audio muting.

SUPER SANDCASTLE with 3 levels : burst, line fly-back, frame blanking.

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

Frame blanking time (start with reset of frame divider) is 21 lines.

VCR INPUT

This provides for continuous use of the short time constant of the first phase-locked loop (frequency).

In VCR mode, the frame synchronization window widens out to a search window and there is no delay of frame fly-back (direct synchronization).

FRAME SAW-TOOTH GENERATOR.

The current to charge the capacitor is automatically switched to 60Hz operation to maintain constant amplitude.

SWITCH MODE POWER SUPPLY (SMPS) SECONDARY TO PRIMARY REGULATION

This power supply uses a differential error amplifier with an internal reference voltage of 1.26V and a phase modulator operating at the line frequency. The power transistor is turned off by the falling edge of the horizontal saw-tooth.

The "soft start" device imposes a very small conduction angle on starting up, this angle progressively increases to its nominal regulation value.

The maximum conduction angle may be monitored by forcing a voltage on pin 15. This pin may also be used for current limitation.

The output pulse is sent to the primary I.C. (TEA2260 or TEA2164) via a low cost synchro transformer.

SECURITY CIRCUIT AND START UP PROCESSOR

When the security input (pin 28) is at a voltage below 1.26V the two outputs are simultaneously cut off until this voltage reaches the 1.26V threshold again. In this case the switch mode power supply is restarted by the "soft start" system.

If this cycle is repeated three times, the two outputs are cut off definitively. To reset the safety logic circuits, V_{CC} must be lower than 3.5V.

This circuit eliminates the risk to switch off the TV receiver in the event of a flash affecting the tube.

On starting up the horizontal scanning function comes into operation at V_{CC} = 6V. The power supply then comes into operation progressively.

On shutting down, the two functions are interrupted simultaneously after the first line fly back.

FRAME BLANKING SAFETY (pin 2)

The frame blanking safety checks the normal of frame scanning.

In case of any problem pin 4 and pin 11 is at a high level (frame blanking) in order to protect the tube.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 12V (unless otherwise noted) Pulse duration at 50% of the ampl.

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current (pin 8) (frame, line and SMPS output without load)		50	80	mA
	Sync Separator (pins 26-27) Positive Video Input AC Coupled (output impedance of signal source < 200Ω)	0.2	1.8	3	V_{pp}
$-I_{27}$	Negative Clamping Current (during sync pulse)	– 25	– 40	–55	µA
I_{27}	Clamping Current Pin for slicing level 0.2V < V_{27pp} < 2V (50% of sync amplitude)	3	6	9	µA
$-I_{26}$	Negative Current	0	– 750	– 1000	µA
I_{26}	Positive Current	17	25	36	µA
	Frame Synchro adjustment (pin 20) (V_{20} = 2.5V)				
I_{20H}	Output Current (V_{27} = 12V)		7.2		µA
I_{20L}	Output Current (V_{27} = 0V)		– 2.8		µA
	VCO (pins 17-18 and 19) Frequency control range after line divider (ceramic resonator : 503kHz)		15.30 to 16.10		kHz
	Phase Comparator φ 1 (pin 22)				
	Output Current Low Loop Gain	± 0.35	± 0.50	± 0.65	mA
	High Loop Gain	± 1	± 1.5	± 2	mA
	Window Pulse Width	7	10	13	µs
	VCR Switching (pin 23)				
	Threshold Voltage VCR Operating	1.7	2.2	2.7	V
I_{23}	Input Current (V_{23} = 0, V_{CC} = 12V)	– 0.030	– 0.25	– 1	mA
	Video Identification (pin 24)				
V_{24}	Output Saturation Voltage (without video signal, I_{24} = 3mA)		0.2	0.6	V
	Output Voltage (with 60Hz video signal, I_{24} = 2.5mA)	5	6.5	7.5	V
	Output Voltage (with 50Hz video signal, I_{24} = 10µA)	11.0	11.5		V
	Video Identification (pin 25)				
I_{25}	Output Current (charging the capacitor)	0.5	0.75	1	mA
t_{25}	Identification Time (charging the capacitor)	1.3	1.7	2.2	µs
V_{25}	Threshold (voltage changing from lower to higher value)	4	4.5	5	V
L_{HYS}	Hysteresis		350		mV
	H-ramp Generator (pin 13)				
I_{ch13}	Charge Current	185	200	215	µA
V_{I13}	Base Voltage of Saw-tooth			0.5	V
I_{dis13}	Discharge Current	3.5	7.0		mA
	Super Sandcastle (pin 11) Output Voltages				
V_{B11}	Burst key pulse level (I_{11} = – 5mA)	9			V
V_{L11}	Line Blanking Pulse Level (I_{11} = – 5mA)	4	4.5	5	V
V_{BT11}	Frame Blanking Pulse Level (and frame out of function) (I_{11} = – 5mA)	2	2.5	3	V
	Super Sandcastle Delay between middle of synch pulse (pin 27) and leading edge				
T_{B11}	of burst key pulse	2.3		3.0	µs
	Duration of burst key pulse	3.7	4	5	µs
T_{O11}	Delay Between SSC Cutting Level at Pin 12 and Line Blanking Pulse			0.35	µs
	Frame Blanking Time (start with reset of frame divider)		21		Line

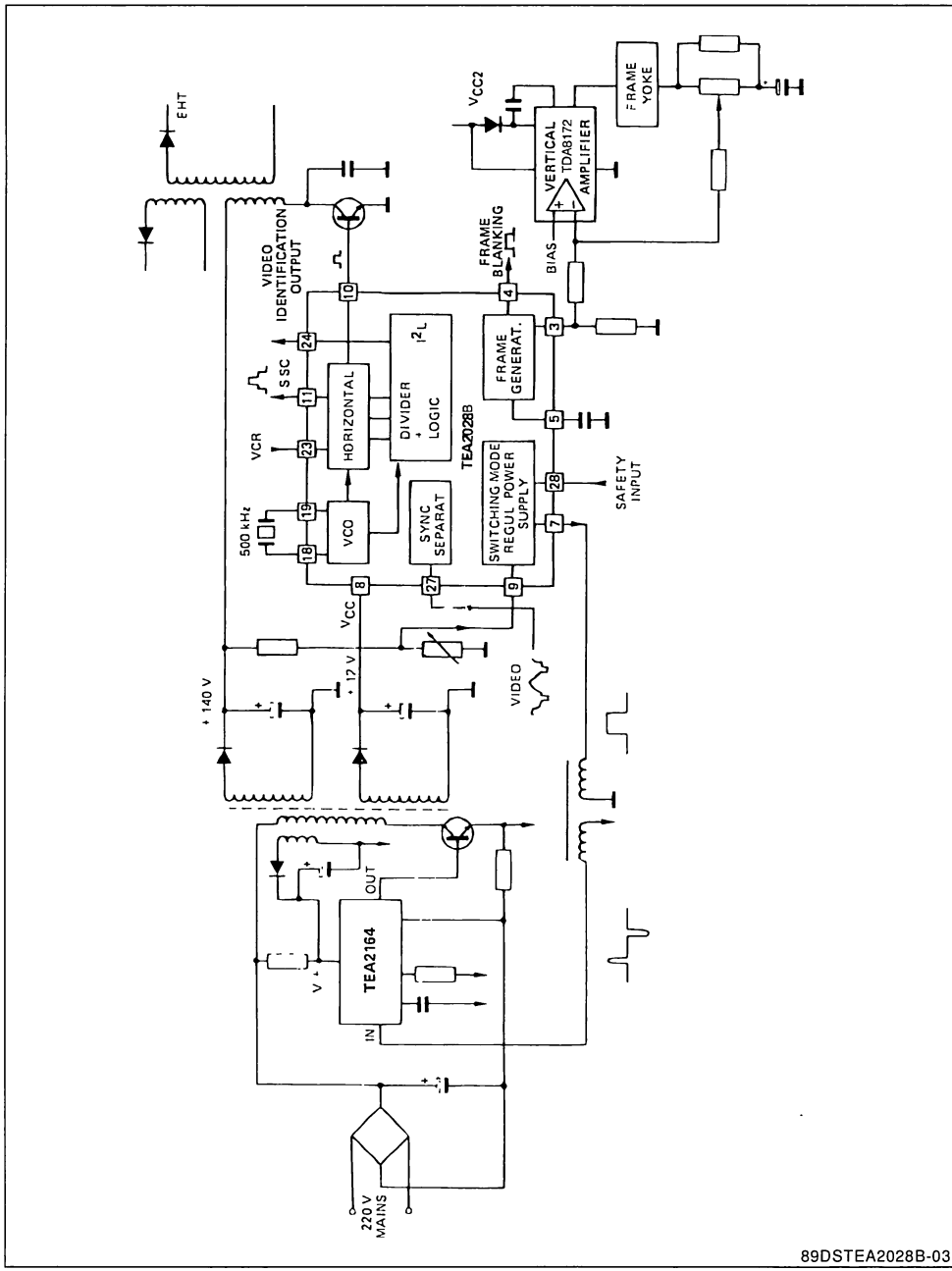
TAB-03

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Positive Line Fly Back Input (pin 12)				
	Delay between middle of synch pulse and middle of line retrace	2.1	2.6	3.1	µs
	Threshold for SMPS Safety	1.1			V
V_{bl12}	Threshold for Blanking		0.3		V
$V_{\varphi 12}$	Threshold for PLL2		3		V
I_{12}	Input Current – 0.4 V < V_{12} < V_{bl12}		– 20		µA
I_{12}	Input Current V_{bl12} < V_{12} <$V\varphi 12$		– 10		µA
I_{12}	Input Current $V_{\varphi 12}$ < V_{12} < V_{CC}	0		1	µA
	Phase Comparator φ 2 (pin 16)				
I_{16}	Charging Current	0.4	0.6	0.8	mA
	Delay Between the Edges of φ 1 and φ 2 (f_{VCO} = 500kHz)		2.3		µs
	Line Output (open collector, F_{vco} = 500KHz) (pin 10)				
	Output Voltage (I_{10max} = 20mA)		1	1.5	V
t_{10}	Output Pulse Duration (when fly-back pulse is with in time t_{10}) (with C (pin 1) = 3.3nF)	27.5	29	30.5	µs
Δt	φ 2 Phase Range	15	16	19	µs
	Frame Logic				
	Free Running Period (with mute signal)		315		Line
	Search Window	247		361	Line
	50 Hz Window	309		315	Line
	60 Hz Window	247		276	Line
	VCR Mode Window	247		361	Line
	Frame Saw-tooth generator (pins 3-5)				
$I_5(60)$	Internal Current Generator (60Hz on)	12	14	16	µA
	Discharging Current	18	55		mA
V_s	Starting Level (0 < I_s < 10mA)	1	1.26	1.4	V
	Frame Blanking Safety Input (pin 2)				
	Threshold Voltage (negative going pulse)	1.15	1.26	1.37	V
	Frame Blanking Output (open collector) - (pin 4)				
	Output Saturation Voltage (I_4 = 5mA)			0.4	V
	Output Current (low level)			10	mA
	Blanking Time		21		Line
	SMPS Control Input (pin 9)				
I_9	Input Current (V_9 = $V_{ref\ 14}$)			2	µA
	SMPS Output (pin 7)				
	No relation between end of SMPS pulse (pin 7) and leading edge of line fly back (pin 12)				
V_7	Output Voltage (0 < I_7 < 20mA)	10			V
t_7	t_{ON} max (f_{VCO} = 500kHz)	26	30	31	µs
	Output Phase Range	0		t_{ON} max	
	Safety Input (pin 28)				
V_{28}	Threshold Voltage (V_{28} = $V_{ref\ 14}$)	1.20	1.26	1.5	V
	Input Current (if V_{28} < $V_{ref\ 14}$ then SMPS and line are switched off during the next line retrace)			3	µA
	Switch-on, Switch-off Processing (pin 15)				
I_{ch15}	Charging Current (t_c = 4µs, T = 64µs)	70		130	µA
$\frac{I_{ch15}}{I_{dis15}}$	Ratio charging/discharging	0.8	1	1.2	
	Starting Supply Voltage (pin 8)				
V_{CC}	SMPS* and Line Starting (pin 7 and pin 10)	5.25		6.5	V
V_{CC}	SMPS Stopping During Line Retrace	5.25		6.5	V
V_{CC}	Frame and Line Stopping	5.25		6.5	V
V_{Hyst}	Hysteresis between Switching-on and Switching-off Level		450		mV
	* Progressive Starting by Decreasing V15				
	Current Reference (pin 14)				
$V_{ref\ 14}$	Voltage Reference (R_{14} = 3.32KΩ ± 1%)	1.2	1.26	1.35	V

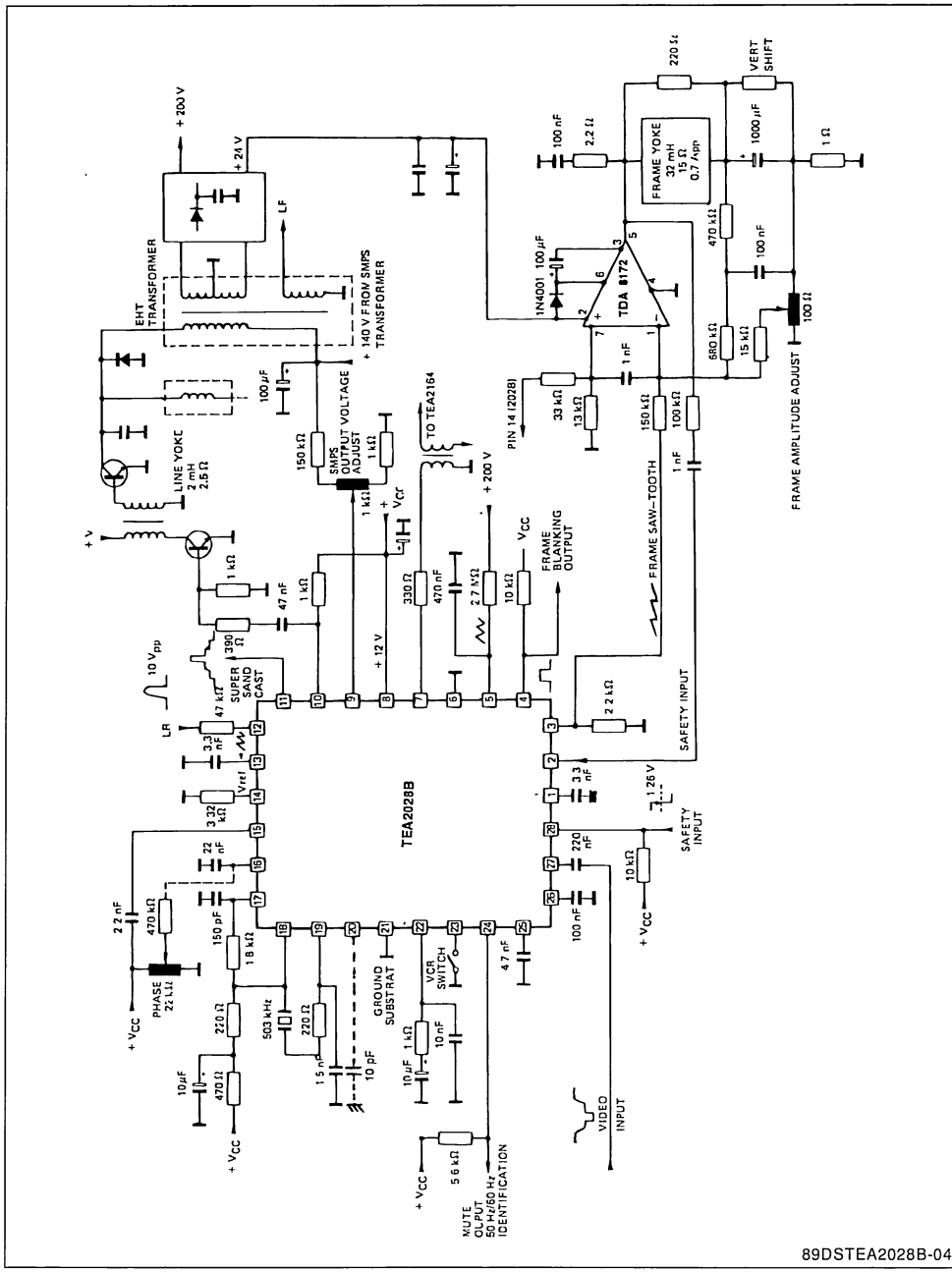
TAB-04

APPLICATION WITH TDA8172 FOR B CLASS FRAME POWER AND TEA2164 FOR SECONDARY SMPS REGULATION



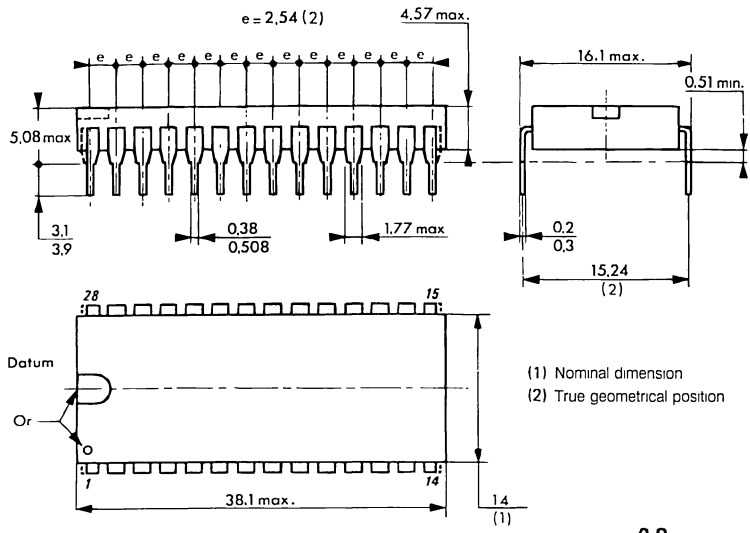
APPLICATION CIRCUIT

(with B class frame power)



PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

DEFLECTION :

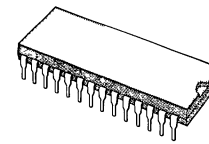
- CERAMIC 500KHz RESONATOR FREQUENCY REFERENCE
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT
- DUAL PLL FOR LINE DEFLECTION
- HIGH PERFORMANCE SYNCHRONIZATION
- SUPER SANDCASTLE OUTPUT
- VIDEO IDENTIFICATION CIRCUIT
- AUTOMATIC 50/60Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL
- SPECIAL PATENTED FRAME SYNCHRO DEVICE FOR VCR OPERATION
- FRAME SAW-TOOTH GENERATOR
- FRAME PHASE MODULATOR FOR THYRISTOR

SMPS CONTROL :

- ERROR AMPLIFIER AND PHASE MODULATOR
- SYNCHRONIZATION WITH HORIZONTAL DEFLECTION
- SECURITY CIRCUIT AND START UP PROCESSOR
- OUTPUT PULSES ARE SENT TO THE PRIMARY SMPS IC (TEA2164 OR TEA2260/61) THROUGH A LOW COST SYNCHRO PULSE TRANSFORMER

DESCRIPTION

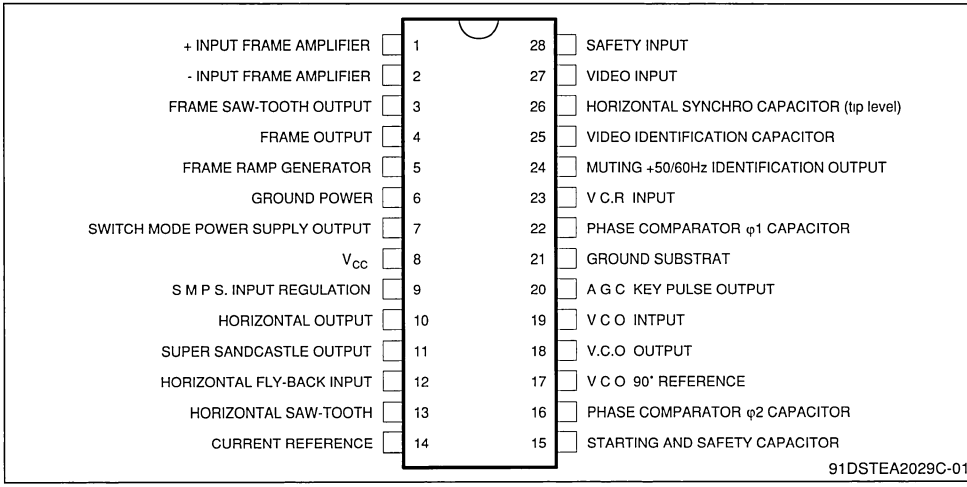
The TEA2029C is a complete (horizontal and vertical) deflection processor with secondary to primary SMPS control for color TV sets.



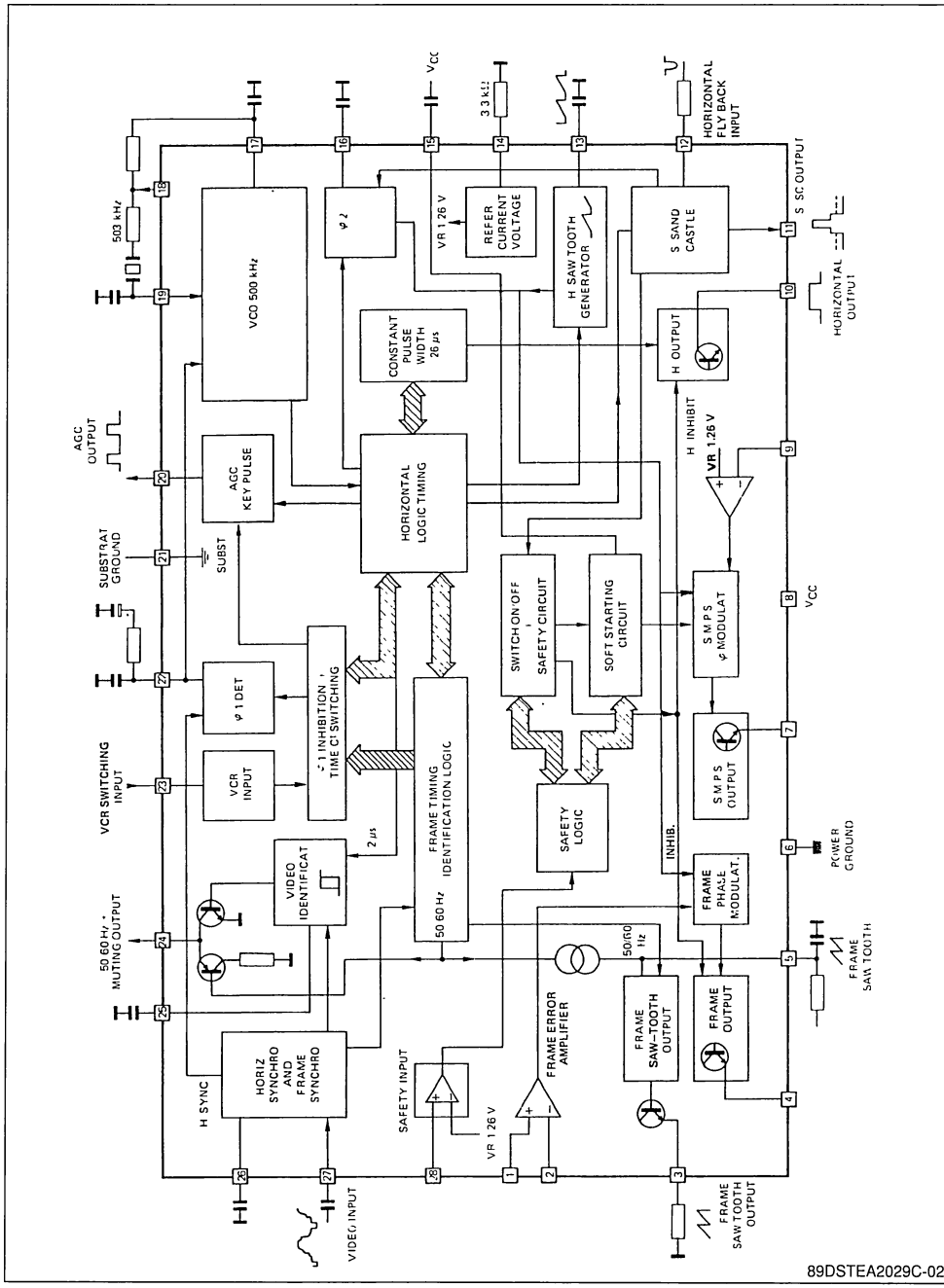
DIP28
(Plastic Package)

ORDER CODE : TEA2029C

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (limiting values) T_{amb} = 25 °C (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit
	Supply Voltage (pin 8)		14	V
VCC	Operating Supply Voltage (pin 8)	Starting threshold	13.2	V
I_{20}	AGC Current (pin 20)		5	mA
I_{24}	Video Identification Current (pin 24)		10	mA
V_{12}	Negative Line Retrace Voltage (pin 12)	– 20		V
I_{12}	Line Retrace Current (pin 12)		+ 10	mA
I_{10}	Line Output Current (pin 10)	– 10	40	mA
I_3	Frame Saw-tooth Generator (pin 3)		20	mA
I_4	Frame Output Current (pin 4)		100	mA
I_7	SMPS Output Current (pin 7)	– 40	40	mA
I_{28}	Safety Input Current (pin 28)		5	mA
V_{28}	Safety Input Voltage (pin 28)		V_{CC}	
V_1/V_2	Common Mode Range (pins 1-2)		10	V

TAB-01

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	55	°C/W

TAB-02

GENERAL DESCRIPTION

This integrated circuit uses I^2L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500KHz by means of a cheap ceramic resonator. This avoids the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produce very accurately defined sampling pulses and the necessary timing signals.

The principal functions implemented are :

- Horizontal scanning processor.
- Frame scanning processor. Two applications are possible :
  - D Class Power stage using an external thyristor.
  - B Class Power stage using an external power amplifier with fly-back generator such as the TDA8170.
- Secondary switch mode power regulation. The SMPS output synchronize a primary I.C. (TEA2164 or TEA2260/61) at the mains part. This concept allows ACTIVE STANDBY facilities.
- Dual phase-locked loop horizontal scanning.
- High performance frame and line synchronization with interlacing control.
- Video identification circuit.
- Super sandcastle.
- AGC key pulse output.
- Automatic 50-60Hz standard identification.
- VCR input for PLL time constant and frame synchro switching.
- Frame saw-tooth generator and phase modulator.
- Switching mode regulated power supply comprising error amplifier and phase modulator.
- Security circuit and start-up processor.
- 500KHz VCO

The circuit is supplied in a 28 pin DIP case.
V_{CC} = 12V.

SYNCHRONIZATION SEPARATOR

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.
The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signals in noise conditions.

FRAME SYNCHRONIZATION

Frame synchronization is fully integrated (no external capacitor required).
The frame timing identification logic permits automatic adaptation to 50 - 60Hz standards or non-interlaced video.

An automatic synchronization window width system provides :

- fast frame capture (6.7ms wide window),
- good noise immunity (0.4ms narrow window).

The internal generator starts the discharge of the saw-tooth generator capacitor so that it is not disturbed by line fly back effects.
Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line fly-back.

A 32µs timing is automatically applied on standardized transmissions, for perfect interlacing.

In VCR mode, the discharge time is controlled by an internal monostable independent of the line frequency and gives a direct frame synchronization.

HORIZONTAL SCANNING

The horizontal scanning frequency is obtained from the 500kHz VCO.

The circuit uses two phase-locked loops (PLL) :

the first one controls the frequency, the second one controls the relative phase of the synchronization and line fly-back signals.

The frequency PLL has two switched time constants to provide :

- capture with a short time constant,
- good noise immunity after capture with a long time constant.

The output pulse has a constant duration of 26µs, independent of V_{CC} and any delay in switching off the scanning transistor.

VIDEO IDENTIFICATION

The horizontal synchronization signal is sampled by a 2µs pulse within the synchronization pulse. The signal is integrated by an external capacitor.

The identification function provides three different levels :

- 0V : no video identification
- 6V : 60Hz video identification
- 12V : 50Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers, and for audio muting.

SUPER SANDCASTLE with 3 levels : burst, line fly-back, frame blanking.

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

Frame blanking time (start with reset of Frame divider) is 24 lines.

VCR INPUT

This provides for continuous use of the short time constant of the first phase-locked loop (frequency).

In VCR mode, the frame synchronization window widens out to a search window and there is no delay of frame fly-back (direct synchronization).

FRAME SCANNING

FRAME SAW-TOOTH GENERATOR. The current to charge the capacitor is automatically switched to 60Hz operation to maintain constant amplitude.

FRAME PHASE MODULATOR (WITH TWO DIFFERENTIAL INPUTS). The output signal is a pulse at the line frequency, pulse width modulated by the voltage at the differential pre-amplifier input.

This signal is used to control a thyristor which provides the scanning current to the yoke. The saw-tooth output is a low impedance, however, and can therefore be used in class B operation with a power amplifier circuit.

SWITCH MODE POWER SUPPLY (SMPS) SECONDARY TO PRIMARY REGULATION

This power supply uses a differential error amplifier with an internal reference voltage of 1.26V and a phase modulator operating at the line frequency. The power transistor is turned off by the falling edge of the horizontal saw-tooth.

The "soft start" device imposes a very small conduction angle on starting up, this angle progressively increases to its nominal regulation value.

The maximum conduction angle may be monitored by forcing a voltage on pin 15. This pin may also be used for current limitation.

The output pulse is sent to the primary S.M.P.S. I.C. (TEA2164) via a low cost synchro transformer.

SECURITY CIRCUIT AND START UP PROCESSOR

When the security input (pin 28) is at a voltage exceeding 1.26V the three outputs are simultaneously cut off until this voltage drops below the 1.26V threshold again. In this case the switch mode power supply is restarted by the "soft start" system.

If this cycle is repeated three times, the three outputs are cut off definitively. To reset the safety logic circuits, V_{CC} must be zero volt.

This circuit eliminates the risk to switch off the TV receiver in the event of a flash affecting the tube.

On starting up, the horizontal and vertical scanning functions come into operation at V_{CC} = 6V. The power supply then comes into operation progressively.

On shutting down, the three functions are interrupted simultaneously after the first line fly-back.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C V_{CC} = 12V (unless otherwise noted) Pulse duration at 50% of the ampl.

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current (pin 8, frame, line and SMPS output without load)		50	80	mA
	Synch Separator (pins 26-27)				
	Positive Video Input AC Coupled (output impedance of signal source < 200 Ω)	0.2	1.8	3	V_{pp}
$-I_{27}$	Negative Clamping Current (during synch, pulse)	− 25	− 40	− 55	µA
I_{27}	Clamping Current Pin for slicing level 0.2 V < V_{27pp} < 2 V (50 % of sync amplitude)	3	6	9	µA
$-I_{26}$	Positive Current	0	− 750	− 1000	µA
I_{26}	Negative Current	17	25	36	µA
	Pulse for keyed AGC (pin 20)				
	Positive (function : without video signal : low level, with video signal : key pulses)				
I_{20}	Output Current			5	mA
V_{20}	Output Saturation Voltage (I_{20} = 5 mA)		0.25	0.4	V
t_k	Pulse width (synchro pulse is always inside the key pulse)	6.5	8	8.5	µs
	VCO (pins 17-18 and 19)				
	Frequency control range after line divider (ceramic resonator : 503 kHz)	15.30 to 16.10			kHz
	Phase Comparator φ 1 (pin 22)				
	Output Current Low Loop Gain	± 0.35	± 0.50	± 0.65	mA
	High Loop Gain	± 1	± 1.5	± 2	mA
	Window Pulse Width	7	10	13	µs
	VCR Switching (pin 23)				
	Threshold Voltage VCR Operating	1.7	2.2	2.7	V
I_{23}	Input Current (V_{23} = 0 V_{CC} = 12V)	− 0.030	− 0.25	− 1	mA
	Video Identification (pin 24)				
V_{24}	Output Saturation Voltage (without video signal, I_{24} = 3 mA)		0.2	0.6	V
	Output Voltage (with 60 Hz video signal, I_{24} = 2.5 mA)	5	6.5	7.5	V
	Output Voltage (with 50 Hz video signal, I_{24} = 10 µA)	11	11.5		V
	Video Identification (pin 25)				
I_{25}	Output Current (charging the capacitor)	0.5	0.75	1	mA
t_{25}	Identification Time (charging the capacitor)	1.3	1.7	2.2	µs
V_{25}	Threshold (voltage changing from lower to higher value)	4	4.5	5	V
L_{HYS}	Hysteresis	150	240	400	mV

TAB-03

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 12V (unless otherwise noted) Pulse duration at 50% of the ampl.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	H-ramp Generator (pin 13)				
I_{ch13}	Charge Current	185	200	215	µA
V_{I13}	Base Voltage of Saw-tooth			0.5	V
I_{dis13}	Discharge Current	3.5	7		mA
	Super Sandcastle (pin 11)				
	Output Voltages				
V_{B11}	Burst Key Pulse Level (I_{11} = - 5mA)	9			V
V_{L11}	Line Blanking Pulse Level (I_{11} = - 5mA)	4	4.5	5	V
V_{BT11}	Frame Blanking Pulse Level (and frame out of function) (I_{11} = - 5mA)	2	2.5	3	V
	Super Sandcastle (continued)				
T_{B11}	Delay between Middle of Synch Pulse (pin 27) and Leading Edge of Burst Key Pulse	2.3		3	µs
	Duration of Burst Key Pulse	3.7	4	5	µs
T_{O11}	Delay between SSC Cutting at Pin 12 and Line Blanking Pulse			0.35	µs
	Negative Line FLy-back Input (pin 12)				
	Threshold for SMPS Safety	1.1			V
V_{bl12}	Threshold for Blanking	11	11.5	12	V
$V_{\varphi 12}$	Threshold for PLL2	- 1			V
I_{12}	Input Current 11V < V_{12}			- 200	µA
I_{12}	Input Current 1.3V < V_{12} < 11V	-3		3	µA
I_{12}	Input Current 0V < V_{12}< 1.3V	0		- 80	µA
I_{12}	Input Current - 1V < V_{12} < 0V	0	- 1	- 2	mA
	Line Blanking Trigger			80	µA
	Phase Comparator φ2 (pin 16)				
I_{16}	Charging Current	0.4	0.6	0.8	mA
	Delay between the Edges of φ1 and φ2 (f_{VCO} = 500kHz)	1.5	2	2.8	µs
	Line Output (open collector) (pin 10)				
	Output Voltage (I_{10max} = 20mA)		1	1.5	V
T_{10}	Output Pulse Duration (when fly-back pulse is with in time T_{10}) (f_{VCO} = 500kHz)	24	26	30	µs
Δt	φ2 Phase Range	15	16	19	µs
	Frame Logic				
	Free Running Period (with mute signal)		315		Line
	Search Window	247		361	Line
	50Hz Window	309		315	Line
	60Hz Window	247		276	Line
	VCR Mode Window	247		361	Line
	Frame Saw-tooth Generator (pins 3-5)				
	Saw-tooth Amplitude	2	3	4	V_{PP}
$I_5(60)$	Internal Current Generator (60Hz on)	12	14	16	µA
	Discharging Time (with C = 0.47µF, ΔV < 4V)	50		70	µs
V_S	Starting Level (0mA < I_S < 0mA)	1	1.26	1.4	V
	Saw-tooth Amplitude (I_S = 10mA)	2	3	4	V_{PP}
	Frame Feedback Inputs (pins 1-2)				
$I_{1,2}$	Positive and Negative Input Current (V_1 - V_2) > 25mA for frame blanking safety			10	µA

TAB-04

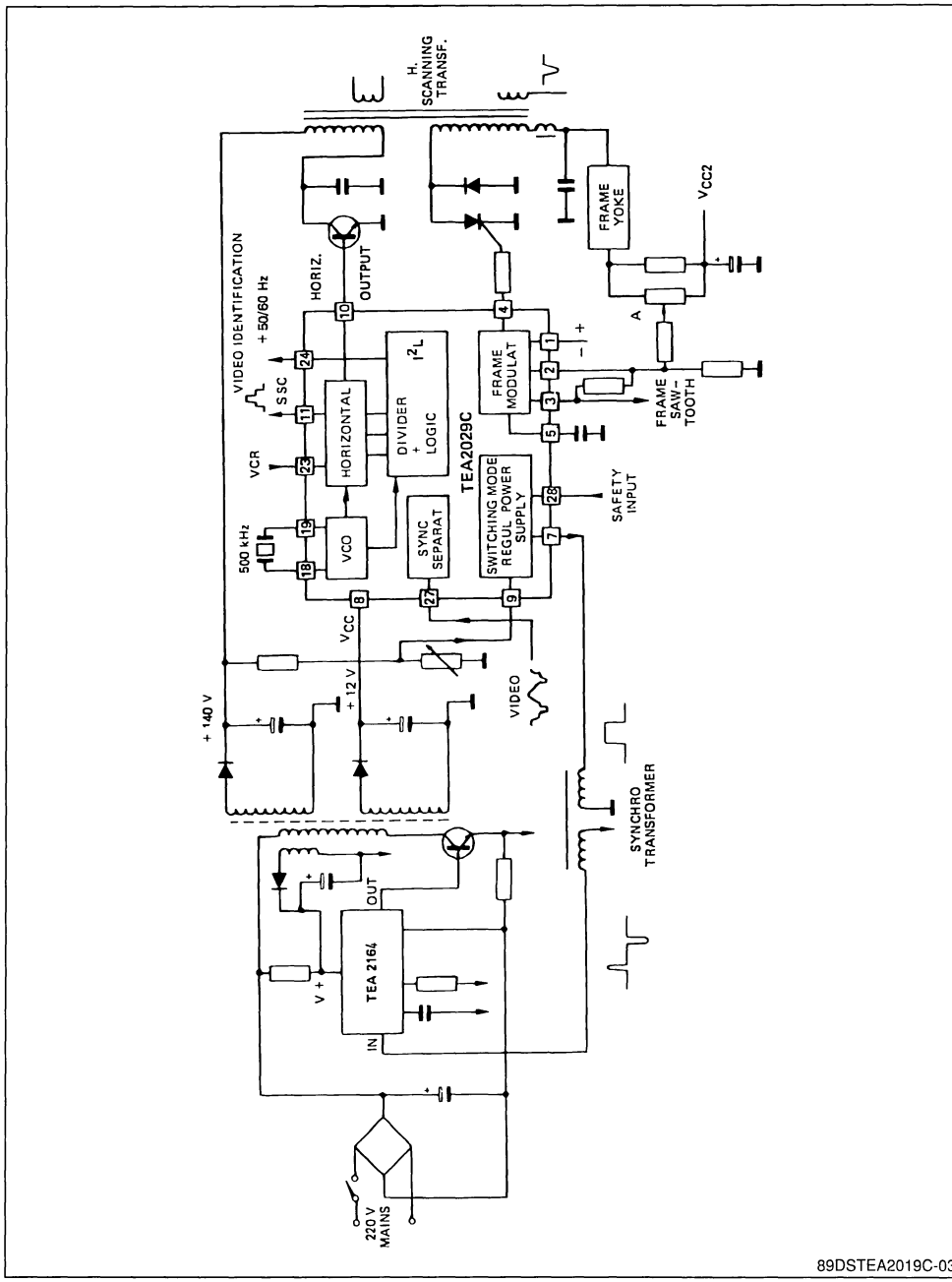
ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Frame Output (pin 4)				
	Output Voltage (0mA < $\|I_4\|$ < 80mA)	10			V
	T_{ON} max (f_{VCO} = 500kHz)	36	40	41	µs
	Output Phase Range	0		t_{ON} max	
	SMPS Control Input (pin 9)				
I_9	Input Current ($V_9 = V_{ref\,14}$)			2	µA
	SMPS Output (pin 7)				
	No Relation Between End of SMPS Pulse (pin 7) and Leading Edge of Line Fly Back (pin 12)				
V_7	Output Voltage (0 < I_7 < 20mA)	10			V
T_7	t_{ON} max (f_{VCO} = 500kHz)	30	32	34	µs
	Nominal Time ($V_9 = V_{ref\,14}$)	26		31	µs
	Output Phase Range	0		t_{ON} max	
	Safety Input (pin 28)				
V_{28}	Threshold Voltage ($V_{28} = V_{ref\,14}$)	1.15	1.26	1.37	V
	Input Current (if $V_{28} > V_{ref\,14}$ then SMPS, line and frame are switched off during the next line retrace)			3	µA
	Switch-on, Switch-off Processing (pin 15)				
$I_{ch\,15}$	Charging Current (t_c = 4µs, T = 64µs)	70		130	µA
$\frac{I_{ch\,15}}{I_{dis\,15}}$	Ratio Charging/discharging	0.8	1	1.2	
	Starting Supply Voltage (pin 8)				
V_{CC}	SMPS*, Frame and Line Starting (pins 7, 10 and 4)	5.25		6.5	V
V_{CC}	SMPS Stopping During Line Retrace	5.25		6.5	V
V_{CC}	Frame and Line Stopping	5.25		6.5	V
	Current Reference (pin 14)				
$V_{ref\,14}$	Voltage Reference	1.2	1.26	1.35	V

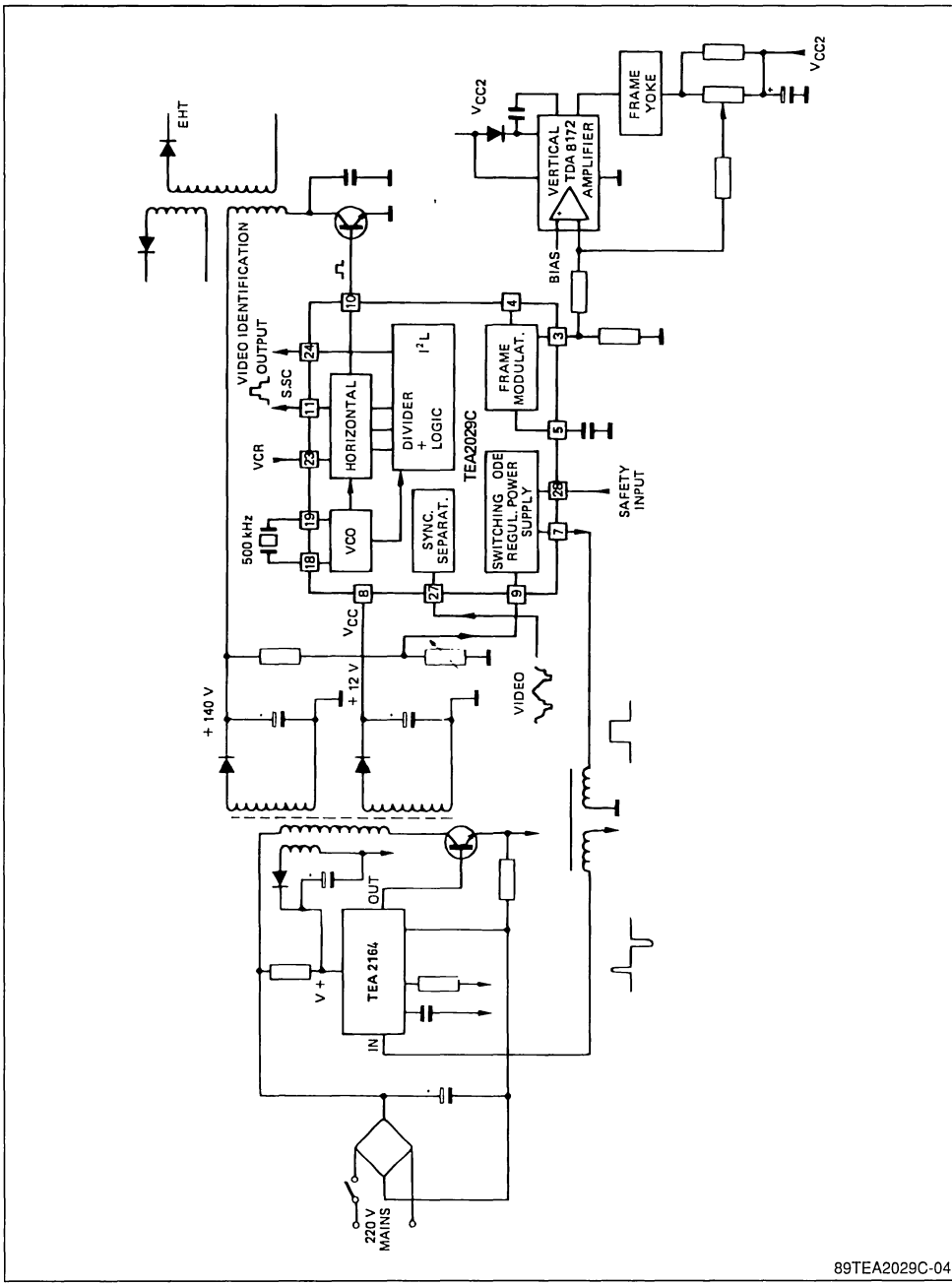
TAB-05

* Progressive starting by decreasing V_{15}

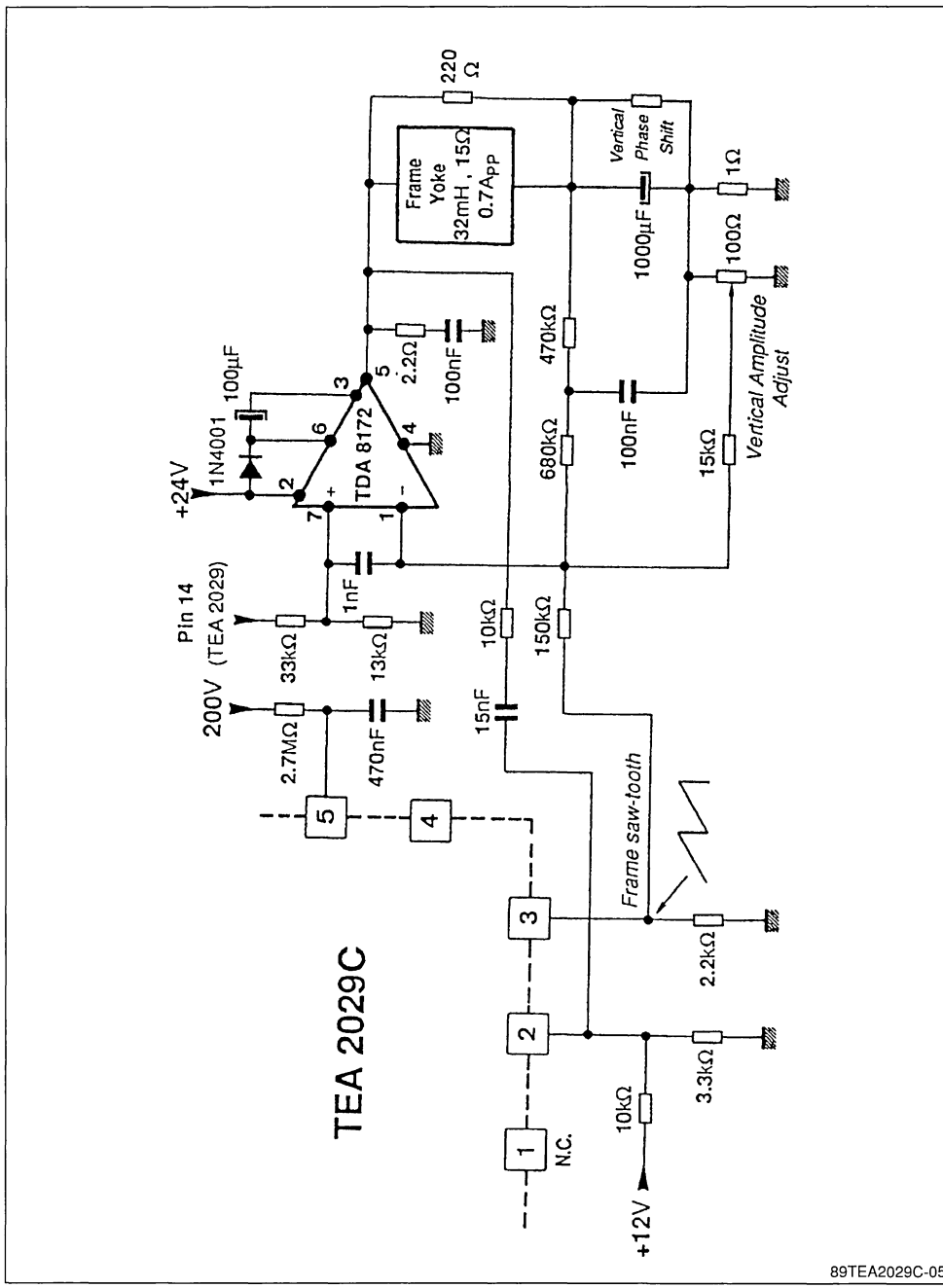
APPLICATION WITH THYRISTOR FOR FRAME POWER AND TEA2164 FOR SECONDARY SMPS REGULATION



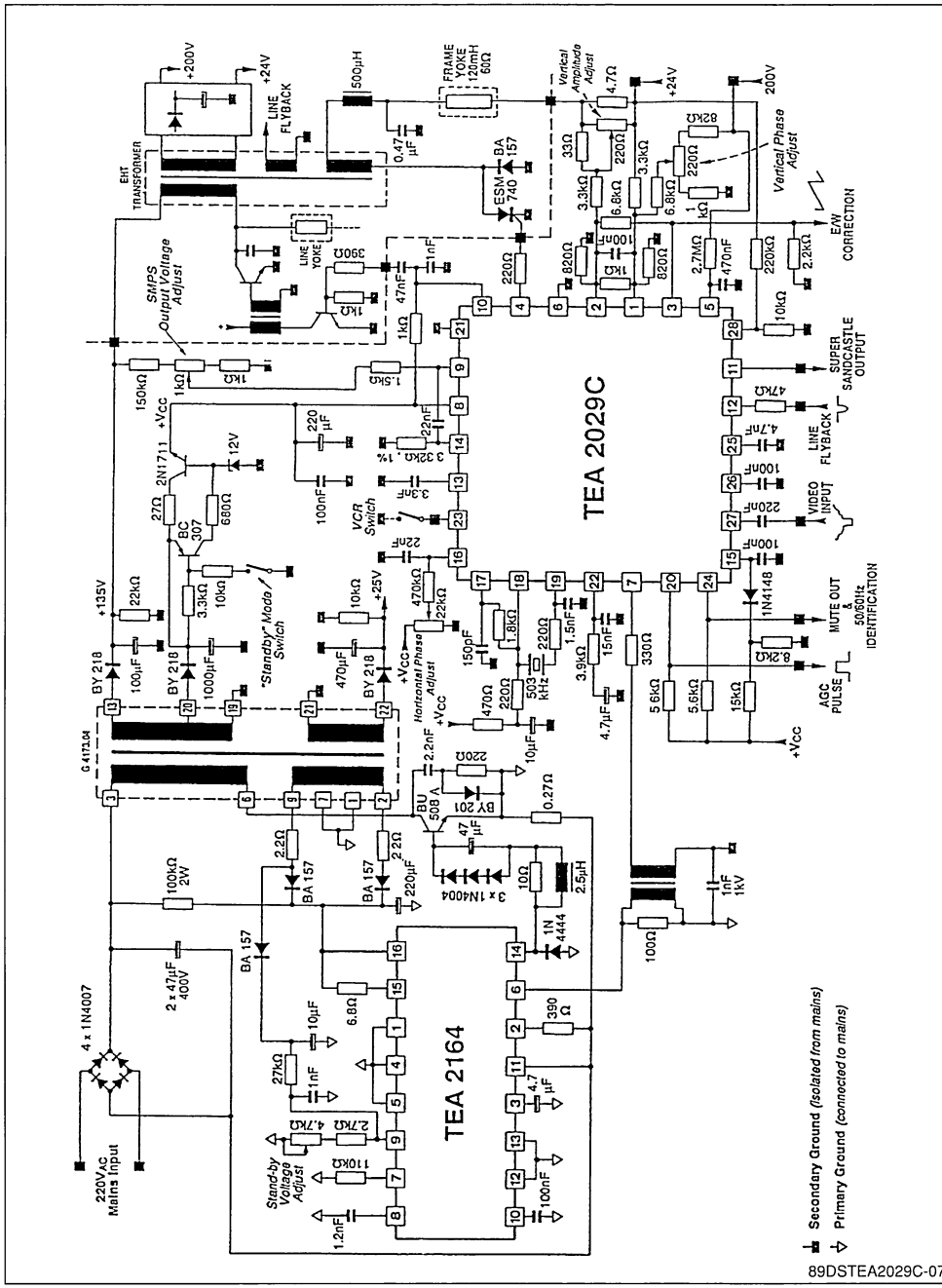
APPLICATION WITH TDA8172 FOR B CLASS FRAME POWER AND TEA2164 FOR SECONDARY SMPS REGULATION



APPLICATION CIRCUIT (WITH B CLASS FRAME POWER)

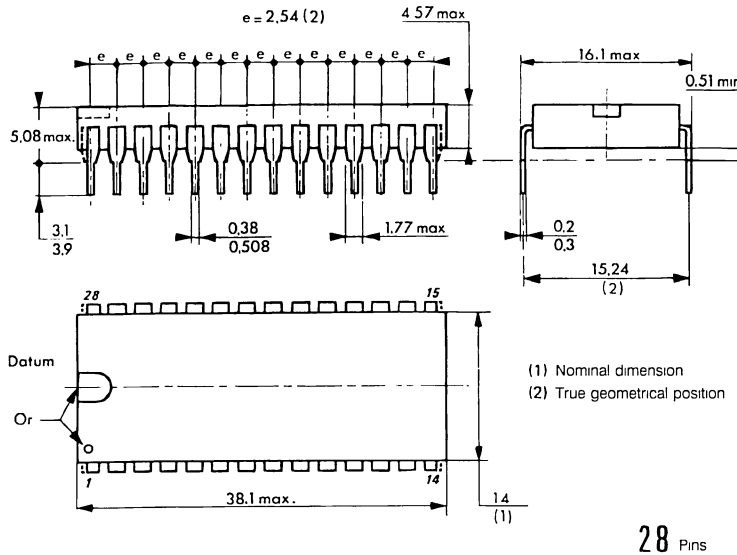


COMPLETE APPLICATION WITH TEA 2164



PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP

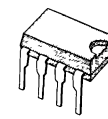


SGS-THOMSON MICROELECTRONICS

TEA2114

VIDEO SWITCH

- 2 VIDEO OUTPUTS WITH 150Ω LOAD DRIVE CAPABILITY
- DYNAMIC OUTPUT AMPLITUDE 4 V_{PP} ON EACH OUTPUT
- BANDWIDTH 18MHz TYP
- FULL PROTECTION AGAINST ESD



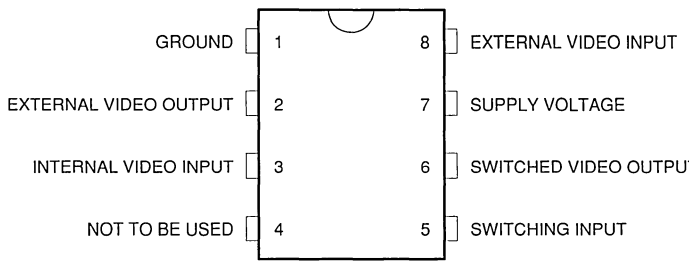
DIP8
(Plastic Package)

ORDER CODE : TEA2114

DESCRIPTION

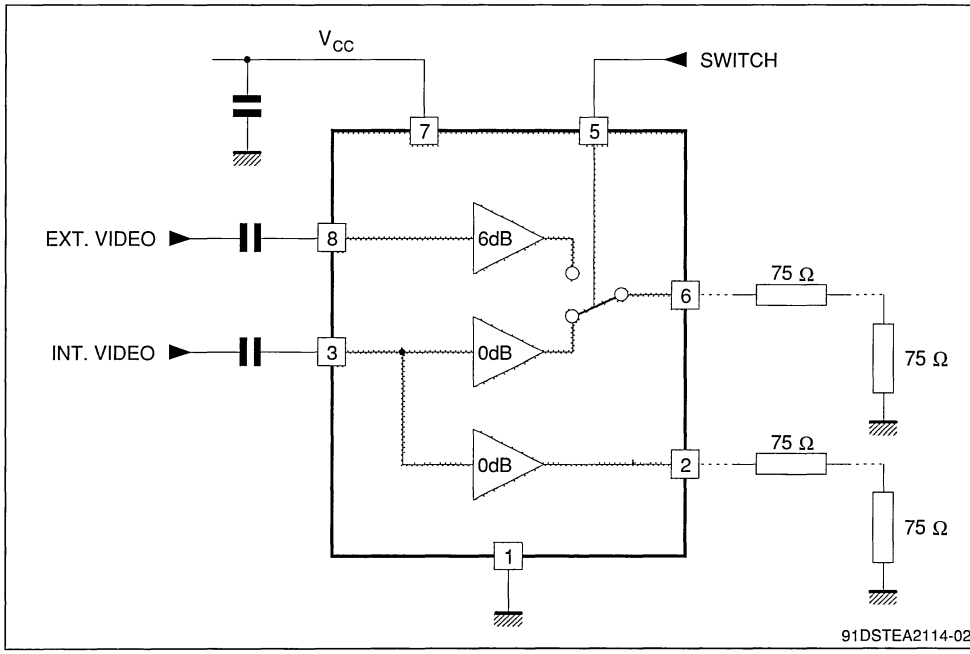
This integrated circuit provides general video switches. It is particularly intended for switching between the peri TV plug and video section of the sets. Its electrical performances make it suitable for wide bandwidth applications (Teletext, D2MAC).

PIN CONNECTIONS



91DSTEA2114-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	14	V
T_j	Junction Temperature	- 40, + 150	°C
T_{stg}	Storage Temperature	- 40, + 150	°C

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 8V$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	6.5		13.2	V
I_{CC}	Supply Current (no load Pin 2 and Pin 6)		10	15	mA
I_{CC}	Supply Current (with load 150Ω on Pin 2 and Pin 6, no video on inputs)		25		mA
INPUTS (Pin 3 and Pin 8)					
	Video Input Swing Pin3 Pin8		4 2		V_{PP} V_{PP}
V_{DCIN}	DC Level Input	1.6	1.9	2.2	V
I_{IN}	Input Bias Current ($V_{DC} = V_{DCIN} + 1.5\ V_{DC}$)		2	5	µA

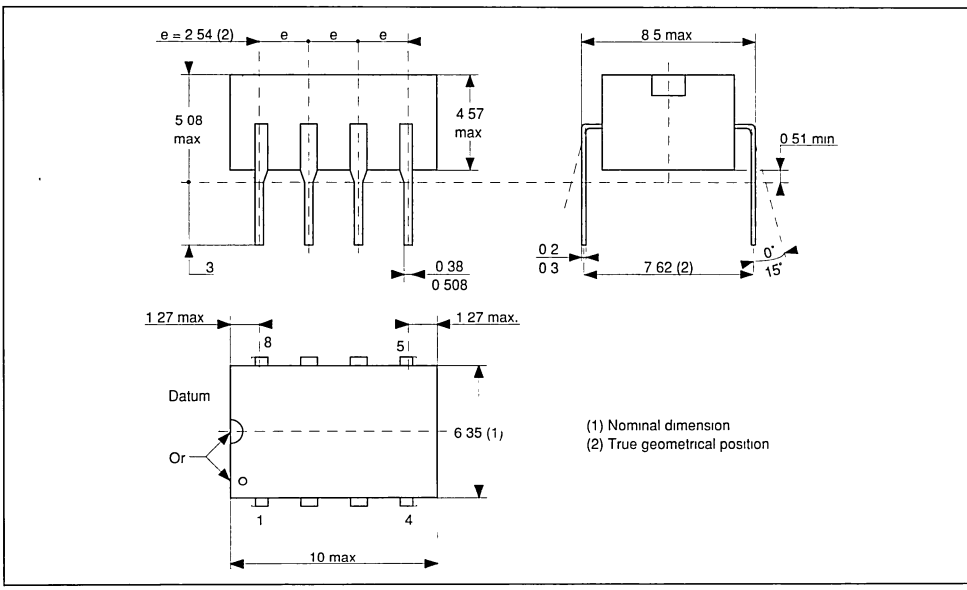
ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25^oC$, $V_{CC} = 8V$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SWITCHED OUTPUT (Pin 6) ($R_{LOAD} = 150\Omega$)					
	Video Output Swing	3	4		V_{PP}
	DC Level Output	0.7	1.1	1.4	V
	Video Gain Pin 6 versus Pin 3, measured at 100kHz, 1 V_{PP} input signal Pin 6 versus Pin 8, measured at 100kHz, 1 V_{PP} input signal	-0.8 5.5	-0.3 6	0.2 6.5	dB dB
	Video Bandwidth Pin 6 versus Pin 3, 1V_{PP} input signal Pin 6 versus Pin 8, 1V_{PP} input signal	18 12	27 18		MHz MHz
	Output Impedance (measured Pin 6)		1		Ω
EXTERNAL OUTPUT (Pin 2) ($R_{LOAD} = 150\Omega$)					
	Video Output Swing	3	4		V_{PP}
	DC Level Output	0.7	1.1	1.4	V
	Video Gain (Pin 2 versus Pin 3, measured at 100kHz, 1 V_{PP} input signal)	-0.8	-0.3	0.2	dB
	Video Bandwidth (Pin 2 versus Pin 3, 1V_{PP} input signal)	18	27		MHz
	Output Impedance (measured Pin 2)		1		Ω
SWITCHING INPUT (Pin 5)					
	Output Current Selection Pin ($V_5 = 0V$)			10	µA
	Threshold Voltage	2.5	3.7	5	V
	Max DC Level			V_{CC}	V
OTHER DYNAMIC FEATURES ($R_{LOAD} = 150\Omega$ on Pin 2 and Pin 6)					
	Crosstalk (between any input, measured at 5MHz)		- 50		dB

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP

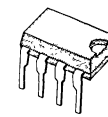


SGS-THOMSON MICROELECTRONICS

TEA2124

VIDEO SWITCH

- 2 VIDEO OUTPUTS WITH 150Ω LOAD DRIVE CAPABILITY
- DYNAMIC OUTPUT AMPLITUDE 4 V_{PP} ON EACH OUTPUT
- BANDWIDTH 18MHz TYP
- FULL PROTECTION AGAINST ESD



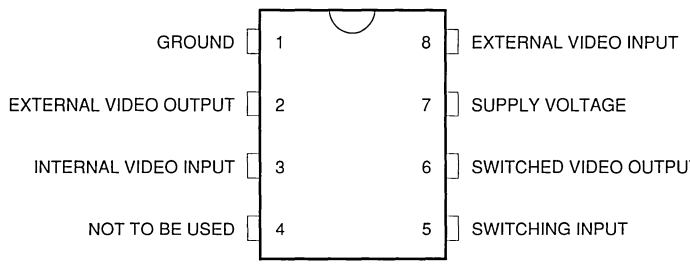
DIP8
(Plastic Package)

ORDER CODE : TEA2124

DESCRIPTION

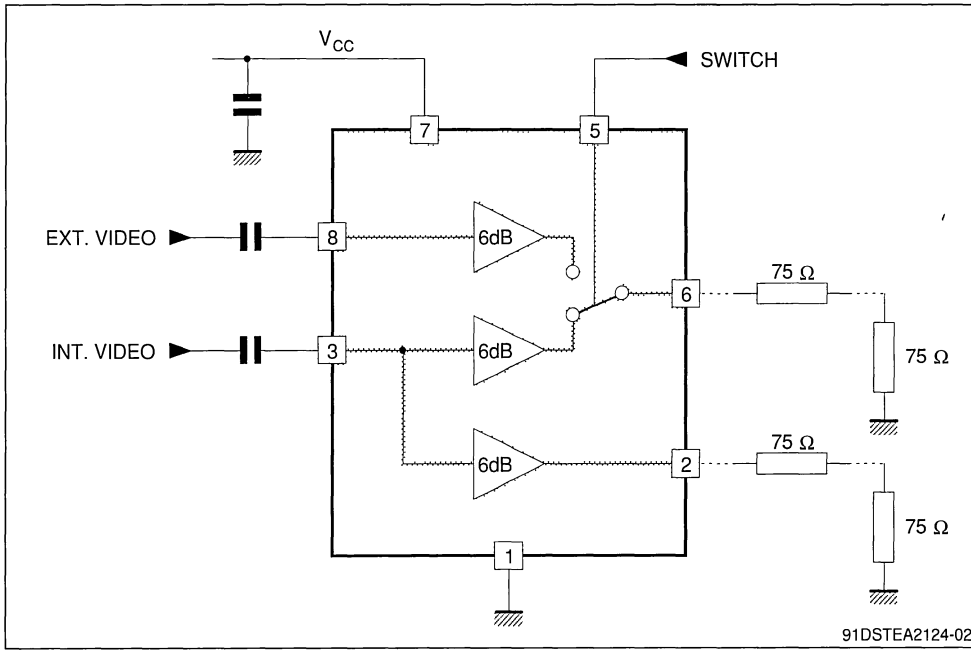
This integrated circuit provides general video switches. It is particularly intended for switching between the peri TV plug and video section of the sets. Its electrical performances make it suitable for wide bandwidth applications (Teletext, D2MAC).

PIN CONNECTIONS



91DSTEA2124-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	14	V
T_j	Junction Temperature	- 40, + 150	°C
T_{stg}	Storage Temperature	- 40, + 150	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 8V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	6.5		13.2	V
I_{CC}	Supply Current (no load Pin 2 and Pin 6)		10	15	mA
I_{CC}	Supply Current (with load 150Ω on Pin 2 and Pin 6, no video on inputs)		25		mA
INPUTS (Pin 3 and Pin 8)					
	Video Input Swing		2		V_{PP}
V_{DCIN}	DC Level Input	1.6	1.9	2.2	V
I_{IN}	Input Bias Current (V_{DC} = V_{DCIN} + 1.5 V_{DC})		1	5	µA

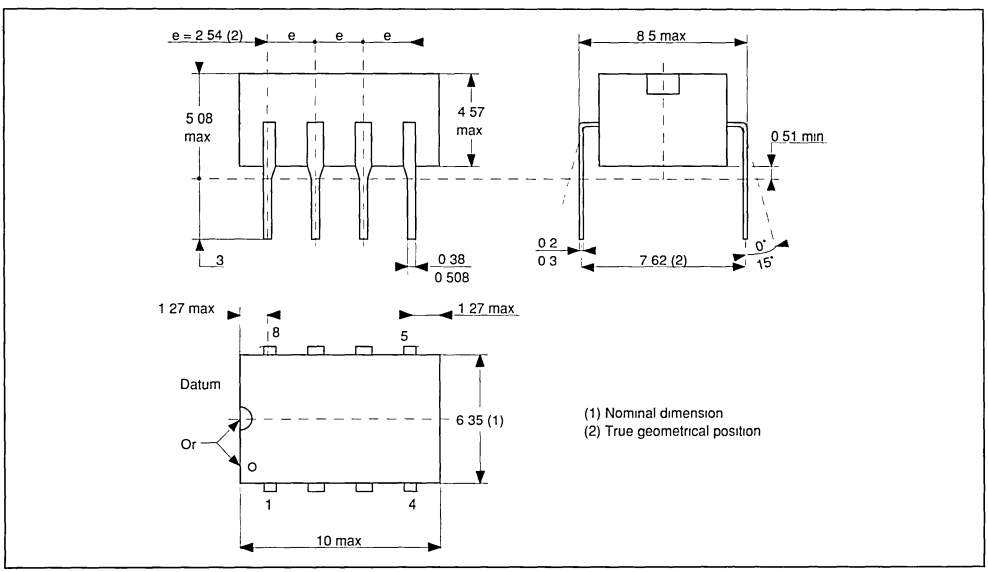
ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25^oC$, $V_{CC} = 8V$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SWITCHED OUTPUT (Pin 6) ($R_{LOAD} = 150\Omega$)					
	Video Output Swing	3	4		V_{PP}
	DC Level Output	0.7	1	1.3	V
	Video Gain (Pin 6 versus Pin 3 or Pin 8, measured at 100kHz, 1 V_{PP} input signal)	5.5	6	6.5	dB
	Video Bandwidth (Pin 6 versus Pin 3 or Pin 8, 1V_{PP} input signal	12	18		MHz
	Output Impedance (measured Pin 6)		1		Ω
EXTERNAL OUTPUT (Pin 2) ($R_{LOAD} = 150\Omega$)					
	Video Output Swing	3	4		V_{PP}
	DC Level Output	0.7	1	1.3	V
	Video Gain (Pin 2 versus Pin 3, measured at 100kHz, 1 V_{PP} input signal)	5.5	6	6.5	dB
	Video Bandwidth (Pin 2 versus Pin 3, 1V_{PP} input signal)	12	18		MHz
	Output Impedance (measured Pin 2)		1		Ω
SWITCHING INPUT (Pin 5)					
	Output Current Selection Pin ($V_5 = 0V$)			10	µA
	Threshold Voltage	2.5	3.7	5	V
	Max DC Level			V_{CC}	V
OTHER DYNAMIC FEATURES ($R_{LOAD} = 150\Omega$ on Pin 2 and Pin 6)					
	Crosstalk (between any input, measured at 5MHz) $R_{LOAD} = 150\Omega$ on Pins 2 and 6 $R_{LOAD} = 1k\Omega$ on Pins 2 and 6		 - 50 - 55		 dB dB

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

TEA2128

COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

ADVANCE DATA

DEFLECTION

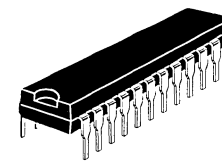
- AUTOMATIC VCR MODE RECOGNITION FOR TIME CONSTANT SWITCHING
- VIDEO IDENTIFICATION CIRCUIT
- DEFLECTION 500kHz RESONATOR OSCILLATOR
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT
- DUAL PLL FOR LINE DEFLECTION
- SUPER SANDCASTLE OUTPUT
- INTERNAL SYNCHRO INHIBITION FOR OSD MODE
- AUTOMATIC 50Hz/60Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL
- FRAME SAFETY INPUT
- FRAME SAWTOOTH GENERATOR

S.M.P.S. CONTROL

- ERROR AMPLIFIER AND PHASE MODULATOR
- SYNCHRONIZATION WITH HORIZONTAL DEFLECTION
- START UP PROCESSOR
- MASTER/SLAVE CONCEPT FACILITIES

DESCRIPTION

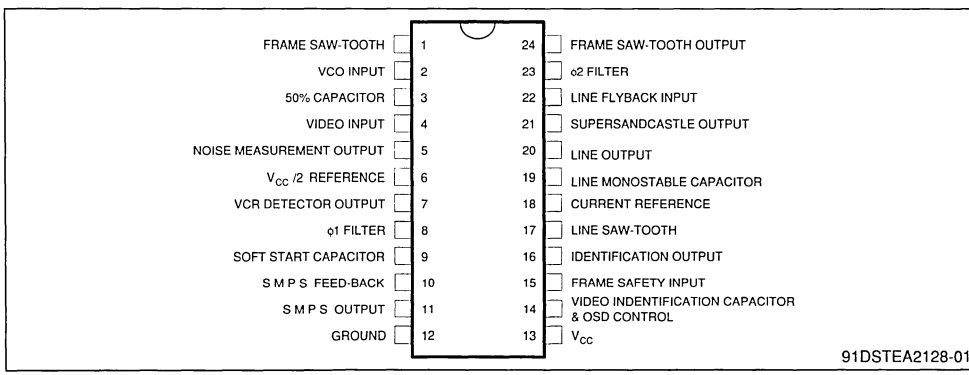
The TEA2128 is a complete (horizontal and vertical) deflection processor with secondary to primary S.M.P.S. control for color TV sets.



SHRINK24
(Plastic Package)

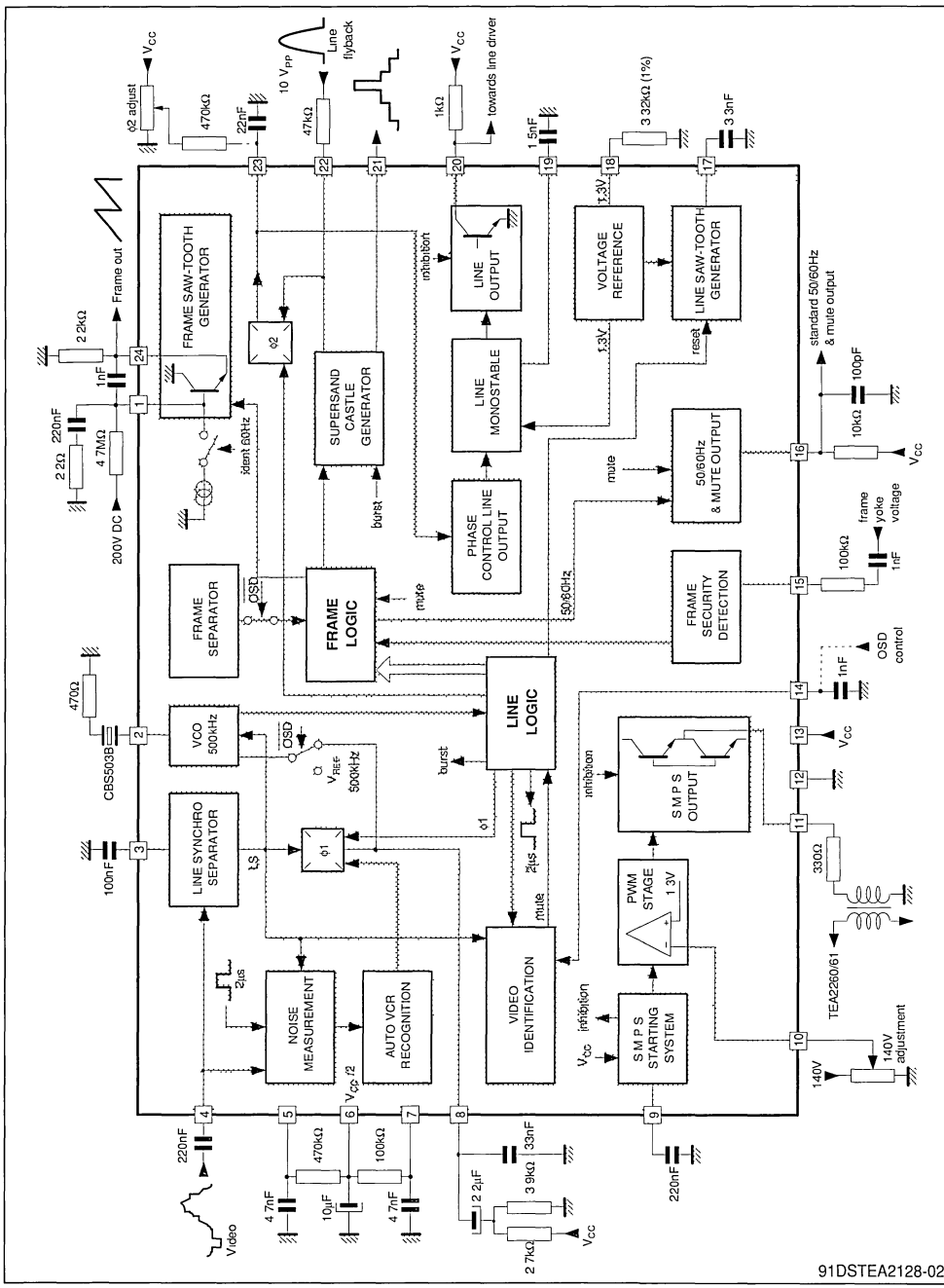
ORDER CODE : TEA2128S

PIN CONNECTIONS



This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

BLOCK DIAGRAM & TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	13.5	V
I_{11}	Output Current	80	mA
I_{20}	Input Current	40	mA
I_{22}	Input Current	± 5	mA
T_{AMB}	Operating Ambient Temperature	0 , 70	°C

THERMAL DATA

$R_{th(j-a)}$	Junction-ambient Thermal Resistance	60	°C/W

ELECTRICAL CHARACTERISTICS

T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude

Symbol	Parameter	Pins	Test conditions	Min.	Typ.	Max.	Unit
	Supply Voltage	13			12		V
	Supply Current	13	Without load in Pins 11, 16, 21, 24		30		mA
VIDEO INPUT							
	Video Signal Amplitude	4	Z source < 200Ω	0.2	1	3	V_{PP}
	Push out Current	4	During the synch. pulse		- 30		µA
	Pull in Current	4	During the line		5		µA
50% SYNCH. PULSE CLAMP							
	Push out Current	3	During the synch. pulse		- 350	-900	µA
	Pull in Current	3	During the line		25		µA
φ 1 AND φ 3 COMPARATOR							
	Short Time Output Current	7 - 8	Identification high		± 1.5		mA
	Long Time Output Current	7 - 8	Identification high		± 0.5		mA
VCO							
	Catching Range	2	Ceramic CSB 503B, R_{SERIAL} = 470Ω	15		16.3	kHz
	Transfer Characteristic		ΔF Pin 20/ΔV Pin 8		2		kHz/V
	Free Running Frequency		Without video signal		15.6		kHz
VIDEO IDENTIFICATION AND STANDARD OUTPUT							
	No video on Pin 4	16	I_{16} = 3mA		0	500	mV
	60Hz video	16	I_{16} = 3mA	5.7	6	6 3	V
	50Hz video	16	I_{16} = 10µA	10.5	11		V
VIDEO IDENTIFICATION AND O.S.D. CONTROL							
	Identification Time	14			2		µs
	Output Current		• 2µs pulse within the synchro pulse • 2µs pulse outside the synchro pulse	-135 65	-160 80	-185 95	µA µA
	Identification Threshold				4.6		V
	OSD Switching Threshold		lower than			1	V
REFERENCE VOLTAGE							
	Output voltage	6	I_6 = 0		$V_{CC}/2$		V
	Output impedance		ΔI_6 = ± 50µA		600		Ω
	Max output current					200	µA

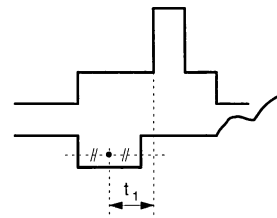
ELECTRICAL CHARACTERISTICS (continued)

T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude

Symbol	Parameter	Pins	Test conditions	Min.	Typ.	Max.	Unit
AUTO VCR SWITCH							
	Switching threshold /V_6	7	• With no noise on the video ($V_5 \leq$ 6V) • With noise on video (6V < V_5 < 7.3V) St* = 0 69 V_5 - 3.85	± 0.28	± 0.3 St*	± 0 32	V V
NOISE GATE							
	Measure sampling time	5	On the synch. pulse bottom		2		µs
	Max. push out current		Max noise		350		µA
	VCR switch inhibition threshold				7.3		V
	Measure bandwidth (-3dB)			700		2000	KHz
	Short time constant manual switching threshold		Active under threshold	4.5	5	5.5	V
	Long time constant		From lower to higher voltage	6.9	7.3	7.6	V
	Manual switching threshold		From higher to lower voltage	6.8	7.2	7.5	V
ϕ 2 COMPARATOR (Pin 14)							
	Output current		During line flyback		± 600		µA
	Delay between ϕ 2 falling edge and the middle video sync. pulse	23 -4	F_{VCO} = 500 kHz		2.8		µs
LINE MONOSTABLE							
	Charge current	19	Line output high		- 67		µA
	Discharge current	19	Line output low		120		µA
	Flip-Flop threshold	19	Falling edge on the line output		1.3		V
LINE OUTPUT							
	Low level	20	I_{20}= 20 mA			1	V
	Pulse duration		R_{18} = 3.32kΩ , C_{19} = 1.5nF	27.5	29	30.5	µs
	ϕ 2 adjustment range	20	Controlled by V_{23} compared with video signal		16		µs
LINE SAW-TOOTH							
	Charge Current	17	R_{18} = 3.32 kΩ		- 180		µA
	Discharge Current	17			7		mA
	Discharge Duration		Controlled by logic VCO 500kHz		6 5		µs
LINE FLYBACK INPUT							
	Blanking Line Threshold	22		0.38	0.4	0.42	V
	ϕ 2 Loop Threshold and Line Output Inhibition (Pin 20)			2.85	3	3 15	V
	Input Current		- 0.4V < V_{22} < 0.4V 0.4V < V_{22} < 3V 3V < V_{22}		-10 - 5	 - 1	µA µA µA
SUPER SANDCASTLE GENERATOR							
	Burst Level	21	R_L = 2.2 kΩ to ground	9			V
	Line Blanking	21		4	4 5	5	V
	Frame Blanking	21		2	2.5	3	V

ELECTRICAL CHARACTERISTICS (continued)

T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude

Symbol	Parameter	Pins	Test conditions	Min.	Typ.	Max.	Unit
SUPER SANDCASTLE GENERATOR (continued)							
	Delay between the midde of the video sync. pulse and the rising edge of the burst (t_1)	21	 91DSTEA2128-03		2.8		µs
	Burst Pulse Duration	21 21	• 50Hz • 60Hz		4.4 3.9		µs µs
	Line Blanking Duration	22	Fixed by flyback Signal pin 22				
	Frame Blanking Duration	21	Fixed by the logic		21		Line
FRAME SAW-TOOTH GENERATOR							
	Low DC Voltage	24			1.3		V
	Discharge Current	1		15		60	mA
	60Hz Internal	1			8		µA
FRAME LOGIC SYNCH.							
	Free Running Period	1-24	Without video signal		315		Line
	Synchronization Windows		Identification low Identification 50Hz high Identification 60Hz high VCR mode	247 309 247 247		361 315 277 361	Line Line Line Line
FRAME SAFETY INPUT							
	Switching Threshold	15	Actived without negative pulse during frame blanking time.		1.3		V
	Output current			40	50	67	µA
S.M.P.S.							
	Input Current	10	$V_{Pin\ 10} = V_{REF}$			2	µA
	Transfer Characteristic		$\Delta t_{Pin\ 11} / \Delta V_{Pin\ 10}$		1.9		µs/µV
$t_{ON\ (max)}$		11			28		µs
$t_{ON\ (min)}$		11			1		µs
	High Level Voltage	11	R_{load} / GND = 500Ω	9			V
SOFT-START							
	V_{CC} Starting Voltage for Line and S.M.P.S.	13	V_{CC} rising		7	7.4	V
	Switch-off Voltage For Line and S.M.P.S. Output	13	V_{CC} decreasing		6.5		V
	Discharge Current	9	• Before soft start period, V_{CC} > 7V $V_{Pin\ 9} > V_{max\ Pin\ 17}$ • During soft start period, V_{CC} > 7V $V_{Pin\ 9} < V_{max\ Pin\ 17}$		60 2.3		µA µA

ELECTRICAL CHARACTERISTICS (continued)

T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude

Symbol	Parameter	Pins	Test conditions	Min.	Typ.	Max.	Unit
CURRENT REFERENCE							
	V_{18} Voltage	18	R_{18} = 3.32 kΩ (1%)	1.21	1.3	1.39	V
	Temperature Shift	18	ΔT = 80°C			± 1	%

GENERAL DESCRIPTION

Introduction

This integrated circuit uses high density I2L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500kHz by means of a cheap ceramic resonator. This avoid the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produces very accurate defined sampling pulses and the necessary timing signals.

Internal Functions

- Horizontal scanning processor
- Frame scanning processor
- B class frame output stage using an external power amplifier with flyback generator
- Line and frame synchronization separation
- Dual phase-locked loop horizontal scanning
- High performance frame and line synchronization with interlacing control.
- Supersandcastle generator
- Automatic 50Hz / 60Hz standard identification
- Frame saw-tooth generator
- Video identification circuit
- Very steady free running mode of the line and frame oscillator in OSD mode. This allows on screen display without phase Jitter in research mode of the tuner
- Automatic VCR mode recognition for time constant switching
- Switching mode regulated supply comprising error amplifier and phase modulator. This allowed a secondary switch mode power regulation with a master slave concept and provides **active standby** facilities
- Line and S.M.P.S. start-up processor
- Frame safety input

WORKING DESCRIPTION

Synchronization Separator

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.

The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signal in noise conditions.

Frame Synchronization

Frame synchronization is fully integrated (no external capacitor required).

The frame timing identification logic permits automatic adaptation to 50-60Hz standards or non-interlaced video.

An automatic synchronization window width system provides:

- Fast frame capture (7.3ms wide window)
- Good noise immunity (0.4ms narrow window)

The internal generator starts the discharge of the sawtooth generator capacitor, so that it is not disturbed by line flyback effects.

Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line flyback. A 32µs timing is automatically applied on standardized transmissions for perfect interlacing.

In VCR mode, the discharge time is controlled by an internal monostable independent of the line frequency and gives a direct frame synchronization.

Horizontal Scanning

The horizontal scanning frequency is obtained from the 500kHz VCO.

The circuit uses two PLL:

- The first one controls the frequency
- The second one controls the relative phase of the synchronization and the line flyback signals.

The output pulse has a constant duration of 29µs, independent of V_{CC} and of any delay in switching-off the scanning transistor.

Supersandcastle Generator
This output delivers a 3 level synchronization signal:
- Burst level
- Line blanking level
- Frame blanking level

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

Frame Scanning
The current to charge the frame sawtooth generator is automatically switched to 60Hz operation to maintain constant amplitude.

Automatic VCR Mode Recognition for Time Constant Switching
- A third phase comparator is used to detect VCR signals and to switch the $\phi 1$ short time constant.
- A noise level measurement is realized on the video synchronization pulse to inhibit the short time constant if the noise level is superior to an adjustable threshold.
- VCR signals are detected if peak to peak signal on Pin 7 is superior to an internal threshold.

This threshold is depending on the noise level. So with a no noisy video signal, the auto VCR switch sensitivity is maximum, and it decreases when the noise increases.

- The sensitivity of the noise gate and the auto VCR switch is adjustable by external resistance.
- Long and short time constants can be selected manually by Pin 5.

Video Identification
The horizontal synchronization signal is sampled by a 2µs pulse within the synchronization pulse. The signal is integrated by an external capacitor.

Identification Output
The identification function provides three different levels :
- 0V : No video identification
- 6V : 60Hz video identification
- 12V : 50Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers and for audio muting.

O.S.D. Mode
The O.S.D. (On Screen Display) function is available when Pin 14 is switch to ground. This function fixes line and frame frequencies to standard deflection frequencies (f_H = 15.6kHz, f_V = 50Hz) and inhibits $\Phi 1$ PLL. This allows to have a stable text display when no signal is coming from antenna.

Switch Mode Power Supply Secondary to Primary Regulation
This power supply uses a differential error amplifier with an internal reference voltage of 1.3V and a phase modulator operating at the line frequency. The power transistor is turned-off during the line retrace by the falling edge of the horizontal sawtooth.
The maximum conduction angle may be monitored by forcing a voltage at Pin 9. This pin can also be used for current limitation.
The output pulse is sent to the primary IC (TEA2260/61 via a low cost synchro transformer).

S.M.P.S. Start-up Processor
The "soft-start" device imposes a very small conduction angle on starting-up. This angle progressively increases to its nominal regulation value.

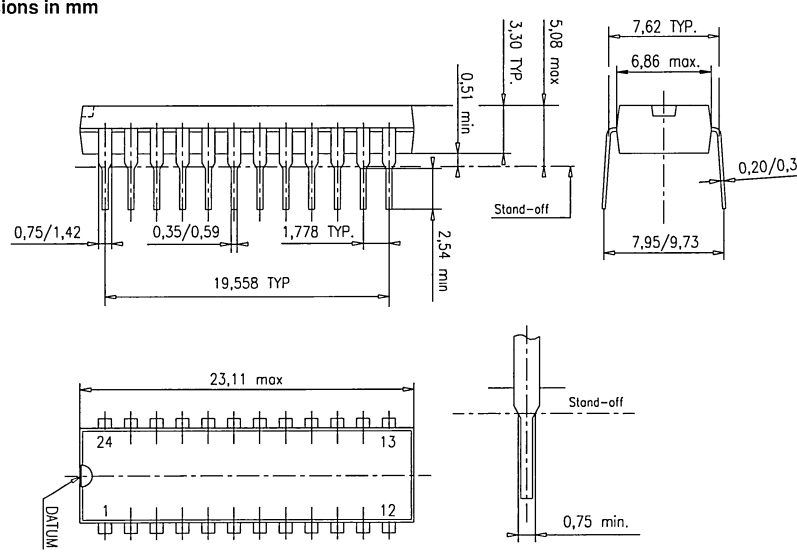
On starting-up the horizontal scanning function comes into operation at V_{CC} = 7V. The power supply then comes into operation progressively.

Frame Blanking Safety Input (Pin 15)
The frame blanking safety checks the normal frame scanning. In the event of vertical scanning failure, the frame blanking level goes high to protect the CRT.

PACKAGE MECHANICAL DATA

24 pins - PLASTIC SHRINK

Dimensions in mm



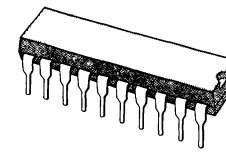
SGS-THOMSON MICROELECTRONICS

TEA2130

COLOR TV SCANNING PROCESSOR

ADVANCE DATA

- AUTOMATIC VCR MODE RECOGNITION FOR TIME CONSTANT SWITCHING
- DIGITAL VIDEO IDENTIFICATION CIRCUIT
- 500kHz RESONATOR OSCILLATOR
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT
- DUAL PLL FOR LINE DEFLECTION
- SUPER SANDCASTLE OUTPUT
- AUTOMATIC 50Hz/60Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL
- FRAME SAFETY INPUT
- FRAME SAWTOOTH GENERATOR



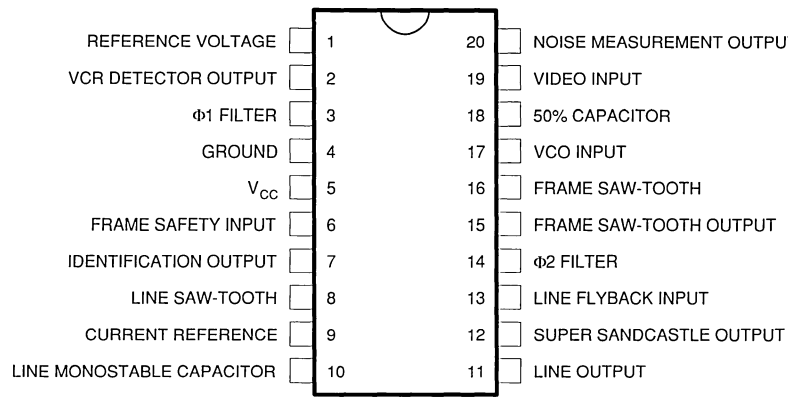
DIP20
(Plastic Package)

ORDER CODE : TEA2130

DESCRIPTION

The TEA2130 is a complete (horizontal and vertical) deflection processor.

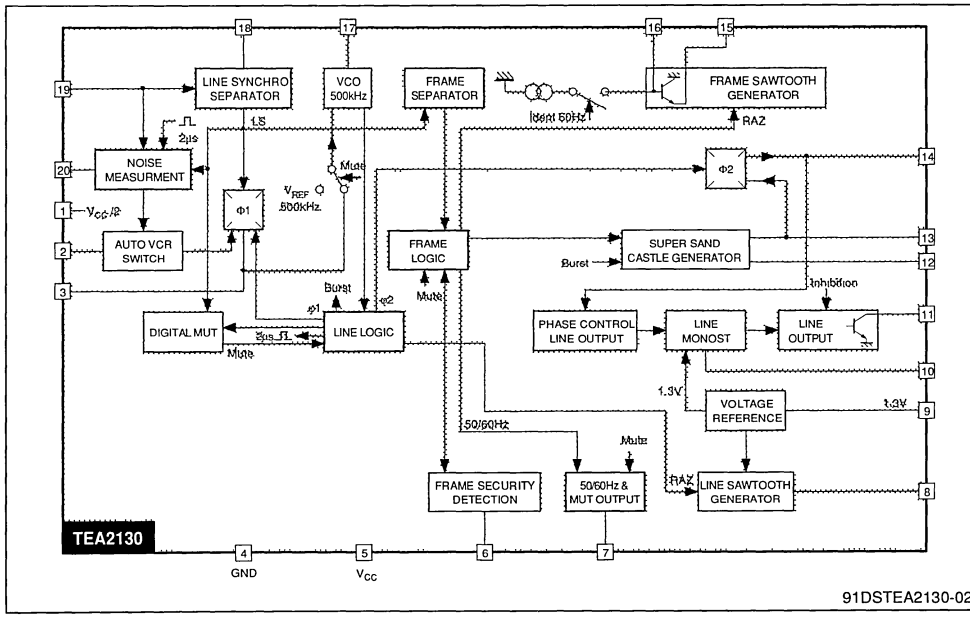
PIN CONNECTIONS



91DSTEA2130-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	13.5	V
I_{11}	Output Current	40	mA
I_{13}	Input Current	± 5	mA
T_{AMB}	Operating Ambient Temperature	0 , 70	°C

THERMAL DATA

$R_{th(j-a)}$	Junction-ambient Thermal Resistance	80	°C/W

ELECTRICAL CHARACTERISTICS

T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	Supply Voltage			12		V
	Supply Current	Without load in pins 7-12-15		26		mA
VIDEO INPUT (Pin 19)						
	Video Signal Amplitude	Z source < 220Ω	0.2	1	3	V_{PP}
	Push out Current	During the synch. pulse		- 30		µA
	Pull in Current	During the line		5		µA

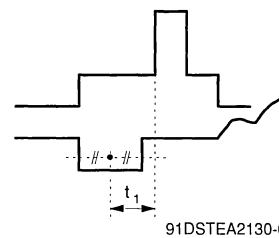
ELECTRICAL CHARACTERISTICS (continued)

T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
50% SYNCH. PULSE CLAMP (Pin 18)						
	Push out Current	During the synch. pulse		- 350	-900	µA
	Pull in Current	During the line		25		µA
φ 1 AND φ 3 COMPARATOR (Pin 2- Pin 3)						
	Short Time Output Current	Identification high		± 1.5		mA
	Long Time Output Current	Identification high		± 0.5		mA
VCO (Pin 17)						
	Catching Range	Ceramic CSB 503B R_{SERIAL} = 470Ω	15		16.3	kHz
	Transfer Characteristic	ΔF pin 11/ΔV pin 3		2		kHz/V
	Free Running Frequency	Without video signal		15.6		kHz
VIDEO IDENTIFICATION AND STANDARD OUTPUT (Pin 7)						
	No video on Pin 19	R_{LOAD}/GND = 5kΩ		0	500	mV
	60Hz video		5.7	6	6 3	V
	50Hz video		10.5	11.3		V
REFERENCE VOLTAGE (Pin 1)						
	Output voltage	I_1 = 0		$V_{CC}/2$		V
	Output impedance	ΔI_1 = ± 50µA		600		Ω
	Max output current				200	µA
AUTO VCR SWITCH (Pin 2)						
	Switching threshold /V_1	• With no noise on the video (V_{20} < 6V) • With noise on video (6V < V_{20} < 7.3V) St* = 0.69 V_{20} - 3.85	± 0 28	± 0.3 St*	± 0.32	V V
NOISE GATE (Pin 20)						
	Measure sampling time	On the synch. pulse bottom		2		µs
	Max. push out current	Max. noise		350		µA
	VCR switch inhibition threshold			7.3		V
	Measure bandwidth (-3dB)		700		2000	KHz
	Short time constant manual switching threshold	Active under threshold	4.5	5	5.5	V
	Long time constant	From lower to higher voltage	6.9	7.3	7.6	V
	Manual switching threshold	From higher to lower voltage	6.8	7.2	7.5	V
φ 2 COMPARATOR (Pin 14)						
	Output current	During line flyback		± 600		µA
	Delay between φ 2 falling edge and the middle video sync. pulse	F_{VCO} = 500 kHz		2.8		µs

ELECTRICAL CHARACTERISTICS (continued)

T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LINE MONOSTABLE (Pin 10)						
	Charge current	Line output high		- 67		µA
	Discharge current	Line output low		120		µA
	Flip-Flop threshold	Falling edge on the line output		1.3		V
LINE OUTPUT (Pin 11)						
	Low level	I_{11}= 20 mA			1	V
	Pulse duration	R_9 = 3.32kΩ , C_{10} = 1.5nF	27.5	29	30.5	µs
	ϕ 2 adjustment range	Controlled by V_{14} compared with video signal		16		µs
LINE SAW-TOOTH (Pin 8)						
	Charge Current	R_9 = 3.32 kΩ		- 180		µA
	Discharge Current			7		mA
	Discharge Duration	Controlled by logic VCO 500kHz		6.5		µs
LINE FLYBACK INPUT (Pin 13)						
	Blanking Line Threshold		0.38	0.4	0.42	V
	ϕ 2 Loop Threshold and Line Output Inhibition (Pin 11)		2.85	3	3.15	V
	Input Current	- 0.4V < V_{13} < 0.4V 0.4V < V_{13} < 3V 3V < V_{13}		-10 - 5	 - 1	µA µA µA
SUPER SANDCASTLE GENERATOR (Pin 12)						
	Burst Level	R_L = 2.2 kΩ to ground	9			V
	Line Blanking		4	4.5	5	V
	Frame Blanking		2	2.5	3	V
	Delay between the midde of the video sync. pulse and the rising edge of the burst (t_1)	 91DSTEA2130-03		2.8		µs
	Burst Pulse Duration	• 50Hz • 60Hz		4.4 3.9		µs µs
	Line Blanking Duration	Fixed by flyback Signal pin 13				
	Frame Blanking Duration	Fixed by the logic		21		Line
FRAME SAW-TOOTH GENERATOR						
	Low DC Voltage			1.3		V
	Discharge Current		15		60	mA
	60Hz Internal			8		µA

ELECTRICAL CHARACTERISTICS (continued)

T_{AMB} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FRAME LOGIC SYNCH.						
	Free Running Period	Without video signal		315		Line
	Synchronization Windows	Identification low Identification 60Hz high VCR mode	247 247 247		361 277 361	Line Line Line
CURRENT REFERENCE (Pin 9)						
	V_9 Voltage	R_9 = 3.32 kΩ (1%)	1.21	1.3	1.39	V
	Temperature Shift	ΔT = 80°C			± 1	%
FRAME SAFETY INPUT (Pin 6)						
	Switching Threshold	Actived without negative pulse during frame blanking time.		1.3		V
	Output current		40	50	67	µA

GENERAL DESCRIPTION

Introduction

This integrated circuit uses high density I2L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500kHz by means of a cheap ceramic resonator. This avoid the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produces very accurate defined sampling pulses and the necessary timing signals.

Internal Functions

- Horizontal scanning processor
- Frame scanning processor
- B class frame output stage using an external power amplifier with flyback generator
- Line and frame synchronization separation
- Dual phase-locked loop horizontal scanning
- High performance frame and line synchronization with interlacing control.
- Supersandcastle generator with reduced burst gate pulse for 60Hz
- Automatic 50Hz / 60Hz standard identification
- Frame saw-tooth generator
- Digital video identification circuit
- Very steady free running mode of the line and frame oscillator when no video is detected. This allows on screen display without phase Jitter in research mode of the tuner
- Automatic VCR mode recognition for time constant switching
- Frame safety input

WORKING DESCRIPTION

Synchronization Separator

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.

The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signal in noise conditions.

Frame Synchronization

Frame synchronization is fully integrated (no external capacitor required).

The frame timing identification logic permits automatic adaptation to 50-60Hz standards or non-interlaced video.

An automatic synchronization window width system provides:

- Fast frame capture (7.3ms wide window)
- Good noise immunity (0.4ms narrow window)

The internal generator starts the discharge of the sawtooth generator capacitor, so that it is not disturbed by line flyback effects.

Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line flyback. A 32µs timing is automatically applied on standardized transmissions for perfect interlacing.

In VCR mode, the discharge time is controlled by an internal monostable independent of the line frequency and gives a direct frame synchronization.

Horizontal Scanning

The horizontal scanning frequency is obtained from the 500kHz VCO.

The circuit uses two PLL:

- The first one controls the frequency
- The second one controls the relative phase of the output line pulse and the line flyback signals.

The output pulse has a constant duration of 29µs, independent of V_{CC} and of any delay in switching-off the scanning transistor.

Supersandcastle Generator

This output delivers a 3 level synchronization signal:

- Burst level
- Line blanking level
- Frame blanking level

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

Frame Scanning

The current to charge the frame sawtooth generator is automatically switched to 60Hz operation to maintain constant amplitude.

Automatic VCR Mode Recognition for Time Constant Switching

- A third phase comparator is used to detect VCR signals and to switch the $\phi 1$ short time constant.
- A noise level measurement is realized on the video synchronization pulse to inhibit the short time constant if the noise level is superior to an adjustable threshold.
- VCR signals are detected if peak to peak signal on pin 2 is superior to an internal threshold.

This threshold is depending on the noise level. So with a no noisy video signal, the auto VCR switch sensitivity is maximum, and it decreases when the noise increases.

- The sensitivity of the noise gate and the auto VCR switch is adjustable by external resistance.
- Long and short time constants can be selected manually by Pin 20.

Digital Video Identification

A digital circuit controls the identification signal. When identification signal is low, the line oscillator is set on a reference frequency. When identification signal is high, $\phi 1$ is locked and the catching phase can start. So that, the TEA2130 allowed on screen displays in a steady way even without video signal (during tuner research for example).

Identification Output

The identification function provides three different levels :

- 0V : No video identification
- 6V : 60Hz video identification
- 12V : 50Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers and for audio muting.

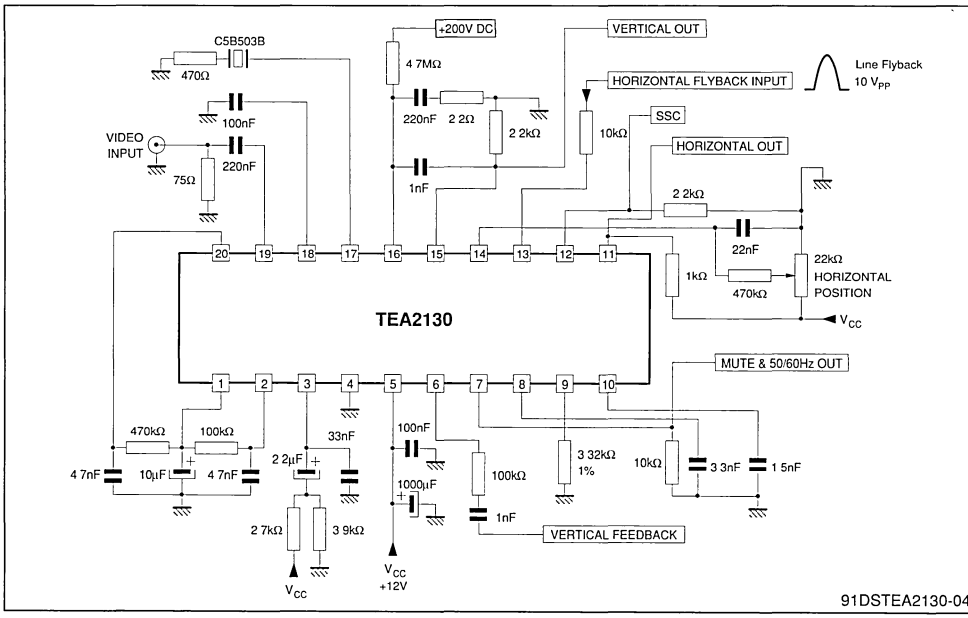
O.S.D. Mode

The O.S.D. (On Screen Display) function is available when video signal is not present on Pin 19. This function fixes line and frame frequencies to standard deflection frequencies (f_H = 15.6kHz, f_V = 50Hz) and inhibits $\Phi 1$ PLL. This allows to have a stable text display when no signal is coming from antenna.

Frame Blanking Safety Input (Pin 6)

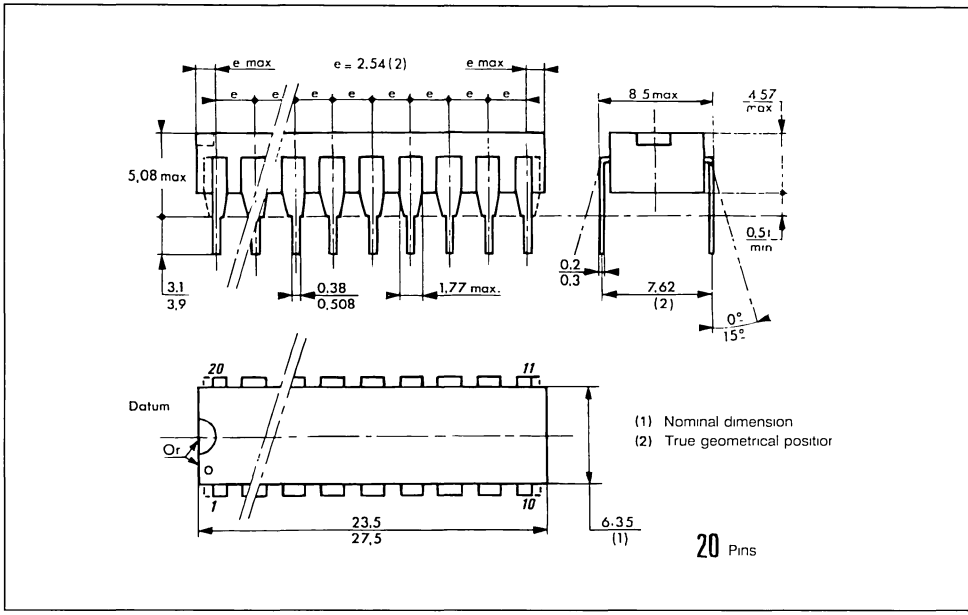
The frame blanking safety checks the normal frame scanning. In the event of vertical scanning failure, the frame blanking level goes high to protect the CRT.

TYPICAL APPLICATION



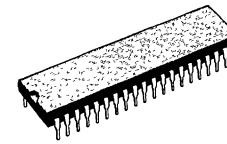
PACKAGE MECHANICAL DATA

20 pins - PLASTIC DIP

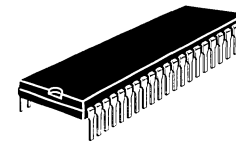


WIDE BAND VIDEO PROCESSOR

- DIGITAL CONTROL OF BRIGHTNESS, SATURATION AND CONTRAST ON TV SIGNALS AND R, G, B INTERNAL OR EXTERNAL SOURCES
- BUS DRIVE OF SWITCHING FUNCTIONS
- DEMATRIXING OF R, G, B SIGNALS FROM Y, R-Y, B-Y, TV MODE INPUTS
- MATRIXING OF R, G, B SOURCES INTO Y, R-Y, B-Y SIGNALS
- AUTOMATIC DRIVE AND CUT-OFF CONTROLS BY DIGITAL PROCESSING DURING FRAME RETRACE
- PEAK AND AVERAGE BEAM CURRENT LIMITATION
- ON-CHIP SWITCHING FOR R, G, B INPUT SELECTION
- ON-CHIP INSERTION OF INTERNAL OR EXTERNAL R, G, B SOURCES



DIP40
(Plastic Package)
ORDER CODE : TEA5040



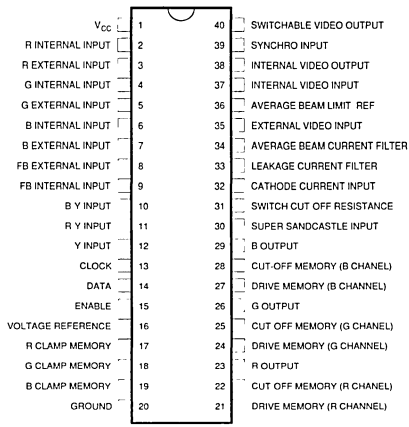
SHRINK42
(Plastic Package)
ORDER CODE : TEA5040S

DESCRIPTION

The TEA5040 is a serial bus-controlled videoprocessing device which integrates a complex architecture fulfilling multiple functions.

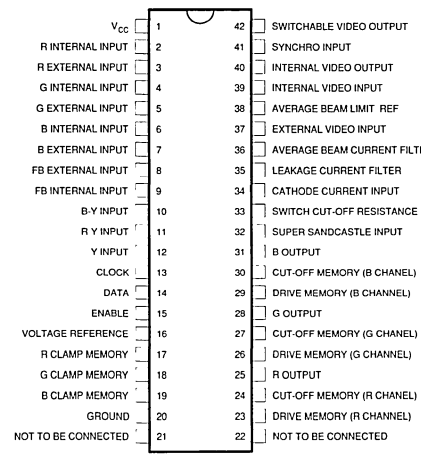
PIN CONNECTIONS

DIP40



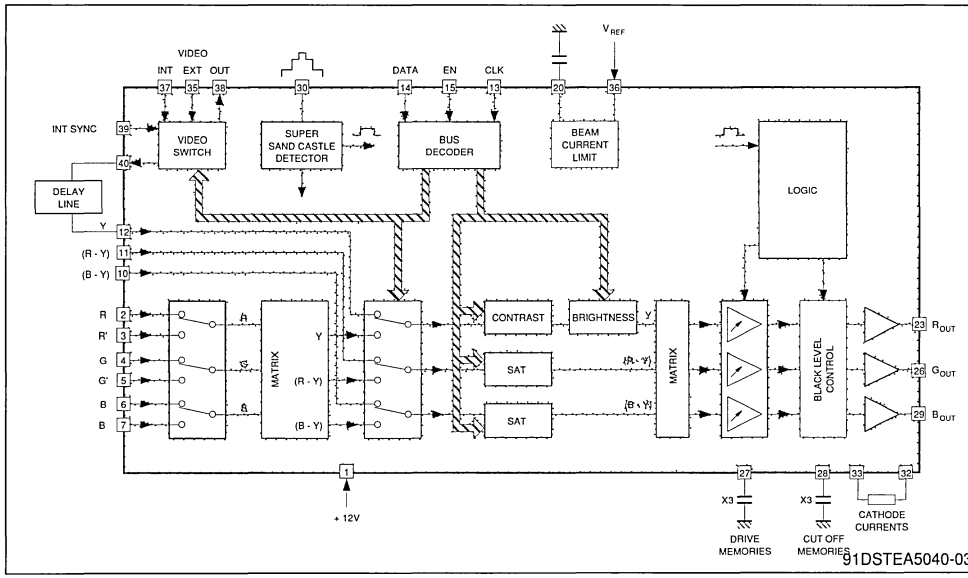
91DSTEA5040-01

SHRINK42



91DSTEA5040-02

BLOCK DIAGRAM (simplified)



GENERAL DESCRIPTION

Brief Description

This integrated circuit incorporates the following features :

- a synchro and two video inputs
- a fixed video output
- a switchable video output
- normal Y, R-Y, B-Y TV mode inputs
- double set of R, G, B inputs
- brightness, contrast and saturation controls as well on a R, G, B picture as on a normal TV picture
- digital control inputs by means of serial bus
- peak beam current limitation
- average beam current limitation
- automatic drive and cut-off controls

Block Diagram Description

BUS DECODER.

A 3 lines bus (clock, data, enable) delivered by the microcontroller of the TV-set enters the videoprocessor integrated circuit (pins 13-14-15). A control system acts in such a way that only a 9-bit word is taken into account by the videoprocessor. Six of the bits carry the data, the remaining three carry the address of the subsystem.

Function	+Address	+Number of Bits
Brightness Control	0	5
Contrast Control	1	5
Colour on/off Selection	2	1
Insertion Allowed	3	1
Sync/Async Mode	4	1
Int/Ext Video Switching	5	1
B-Y Saturation Control	6	6
R-Y Saturation Control	7	6

TAB-01

Table below depicts 9-bit words required for various functions.

Subsystem's Configuration		Data Bits LSB....MSB	Add. Bits LSB....MSB
BRIGHTNESS	Min. Max.	X00000 X11111	000
CONTRAST	Min. max.	X00000 X11111	100
COLOUR ON/OFF	Off On	XXXXX0 XXXXX1	010
INSERTION	Allowed Not Allowed	XXXXX0 XXXXX1	110
SYNC/ASYNC MODE	Sync. Async.	XXXX0X XXXX1X	001
VIDEO INT/EXT	Ext. Int.	XXXXX0 XXXXX1	101
SATURATION B-Y	Min. Max.	000000 111111	011
SATURATION R-Y	Min. Max.	000000 1111	111

TAB-02

A demultiplexer directs the data towards latches which drive the appropriate control. More detailed information about serial bus operation is given in the following chapter.

Video Switch

The video switch has three inputs :

- an internal video input (pin 37),
- an external video input (pin 35),
- a synchro input (pin 39),

and two outputs :

- an internal video output (pin 38),
- a switchable video output (pin 40)

The 1Vpp composite video signal applied to the internal video input is multiplied by two and then appears as a 2Vpp low impedance composite video signal at the output. This signal is used to deliver a 1Vpp/75Ω composite video signal to the peri-TV plug.

The switchable video output can be any of the three inputs. When the Int/Ext one active bit word is high (address number 5), the internal video input is selected. If not, either a regenerated synchro pulse or the external video signal is directed towards this output depending on the level of the Sync/Async one active bit word (address number 4). As this output is to be connected to the synchro integrated circuit, RGB information derived from an external source via the Peri-TV plug can be displayed on the screen, the synchronization of the TV-set being then made with an external video signal.

When RGB information is derived from a source integrated in the TV-set, a teletext decoder for example, the synchronization can be made either on the internal video input (in case of synchronous data) or on the synchro input (in case of asynchronous data).

R, G, B Inputs

There are two sets of R, G, B inputs : one is to be connected to the peri-TV plug (Ext R, G, B), the second one to receive the information derived from the TV-set itself (Int R, G, B).

In order to have a saturation control on a picture coming from the R, G, B inputs too, it is necessary to get R-Y, B-Y and Y signals from R, G, B information : this is performed on the first matrix that receives the three 0.9Vp (100% white) R, G, B signals and delivers the corresponding Y, R-Y, B-Y signals. These ones are multiplied by 1.4 in order to make the R-Y and B-Y signals compatible with the R-Y and B-Y TV mode inputs. The desired R, G, B inputs are selected by means of 3 switches controlled by the two fast blanking signal inputs. A high level on FB external pin selects the external RGB sources. The three selected inputs are clamped in order to give the required DC level at the output of this first matrix. The three not selected inputs are clamped on a fixed DC level.

Y, R-Y, B-Y Inputs

The 2Vpp composite video signal appearing at the switchable output of the video switch (pin 40) is driven through the subcarrier trap and the luminance delay line with a 6 dB attenuation to the Y input (1Vpp ; pin 12). In order to make this 1Vpp (synchro to white) Y signal compatible with the 1Vpp (black

to white) Y signal delivered by the first matrix, it is necessary to multiply it by a coefficient of 1.4.

R, G, B Insertion Pulse (fast blanking)

A R, G, B source has also to provide an insertion pulse. Since this integrated circuit can be directly connected to two different sources, it is necessary then to have two separate insertion pulse inputs (pin 8-9). Fast blanking can be inhibited by a one active bit word. The two fast blanking inputs carry out an OR function to insert R, G, B sources into TV picture. The external fast blanking (FB ext.) selects the appropriate R, G, B source.

Controls

The four brightness, contrast and saturation control functions are direct digitally controlled without using digital-to-analog converters.

The contrast control of the Y channel is obtained by means of a digital potentiometer which is an attenuator including several switchable cells directly controlled by a 5 active bit word (address number 1). The brightness control is also made by a digital potentiometer (5 active bit word, address number 0). Since a + 3dB contrast capability is required, the Y signal value could be up to 0.7Vpp nominal. For both functions, the control characteristics are quasi-linear.

In each R-Y and B-Y channel, a six-cell digital attenuator is directly controlled by a 6 active bit word (address number 6 and 7). The tracking needed to keep the saturation constant when changing the contrast has to be done externally by the microcontroller. Furthermore, colour can be disabled by blanking R-Y and B-Y signals using one active bit word (address number 2) to drive the one-chip colour ON/OFF switch.

Second Matrix, Clamp, Peak Clipping, Blanking

The second matrix receives the Y, R-Y and B-Y signals and delivers the corresponding R, G, B signals. As it is required to have the capability of + 6dB saturation, an internal gain of 2 is applied on both R-Y and B-Y signals.

A low clipping level is included in order to ensure a correct blanking during the line and frame retraces. A high clipping level ensures the peak beam current limitation. These limitations are correct only if the DC bias of the three R, G, B signals are precise enough. Therefore a clamp has been added in each channel in order to compensate for the inaccuracy of the matrix.

Sandcastle Detector And Counter

The three level supersandcastle is used in the circuit to deliver the burst pulse (CLP), the horizontal pulse (HP), and the composite vertical and horizontal blanking pulse (BLI). This last one is regenerated in the counter which delivers a new composite pulse (BL) in which the vertical part lasts 23 lines when the vertical part of the supersandcastle lasts more than 11 lines.

The TEA5040 cannot work properly if this minimum duration of 11 lines is not ensured.

The counter delivers different pulses needed circuit and especially the line pulses 17 to 23 used in the automatic drive and cut-off control system.

Automatic Drive And Cut-off Control System

Cut-off and drive adjustments are no longer required with this integrated circuit as it has a sample and hold feedback loop incorporating the final stages of the TV-set. This system works in a sequential mode. For this purpose, special pulses are inserted in G, R and B channels. During the lines 17, 18 and 19, a "drive pulse" is inserted respectively in the green, red and blue channels. The line 20 is blanked on the three channels. During the lines 21, 22 and 23, a "quasi cut-off pulse" is inserted respectively in the green, red and blue guns.

The resulting signal is then applied to the input of a voltage controlled amplifier. In the final stages of the TV-set, the current flowing in each green, red and blue cathode is measured and sent to the videoprocessor by a current source.

The three currents are added together in a resistor matrix which can be programmed to set the ratio between the three currents in order to get the appropriate colour temperature. The output of the matrix forms a high impedance voltage source which is connected to the integrated circuit (pin 32). Same measurement range between drive and cut-off is achieved by internally grounding an external low impedance resistor during lines 17, 18 and 19.

This is due to the fact that the drive currents are about one hundred times higher than the cut-off and leakage currents.

Each voltage appearing sequentially on the wire pin 32 is then a function of specific cathode current :

- When a current due to a drive pulse occurs, the voltage appearing on the pin 32 is compared within the IC with an internal reference, and the result of the comparison charges or discharges an external appropriate drive capacitor which stores the value during the frame. This voltage is applied to a voltage controlled amplifier and the system works in such a way that the pulse current drive derived from the cathode is kept constant.
- During the line 20, the three guns of the picture tube are blanked. The leakage current flowing out of the final stages is transformed into a voltage which is stored by an external leakage capacitor to be used later as a reference for the cut-off current measurement.
- When a current due to a cut-off pulse occurs, the voltage appearing on the pin 32 is compared within the IC to the voltage present on the leakage memory. An appropriate external capacitor is then charged or discharged in such a way that the difference between each measured current and the leakage current is kept constant, and thus the quasi cut-off current is kept constant.

Average Beam Current Limitation

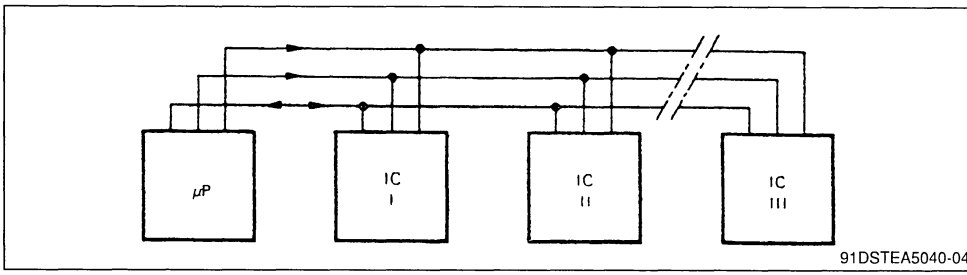
The total current of the three guns is integrated by means of an internal resistor and an external capacitor (pin 34) and then compared with a programmable voltage reference (pin 36). When 70% of the maximum permitted beam current is reached, the drive gain begins to be reduced ; to do so, the amplitude of the inserted pulse is increased.

In order to keep enough contrast, the maximum drive reduction is limited to 6dB. If it is not sufficient, the brightness is suppressed.

SPECIFICATION FOR THE THOMSON BI-DIRECTIONAL DATA BUS

This is a bi-directional 3-wire (ENABLE, CLOCK, DATA) serial bus. The DATA line transmission is bi-directional whereas ENABLE and CLOCK lines are only microprocessor controlled. The ENABLE and CLOCK lines are only driven by the microcomputer.

Figure 1 : Peripheral Connections on Bus.



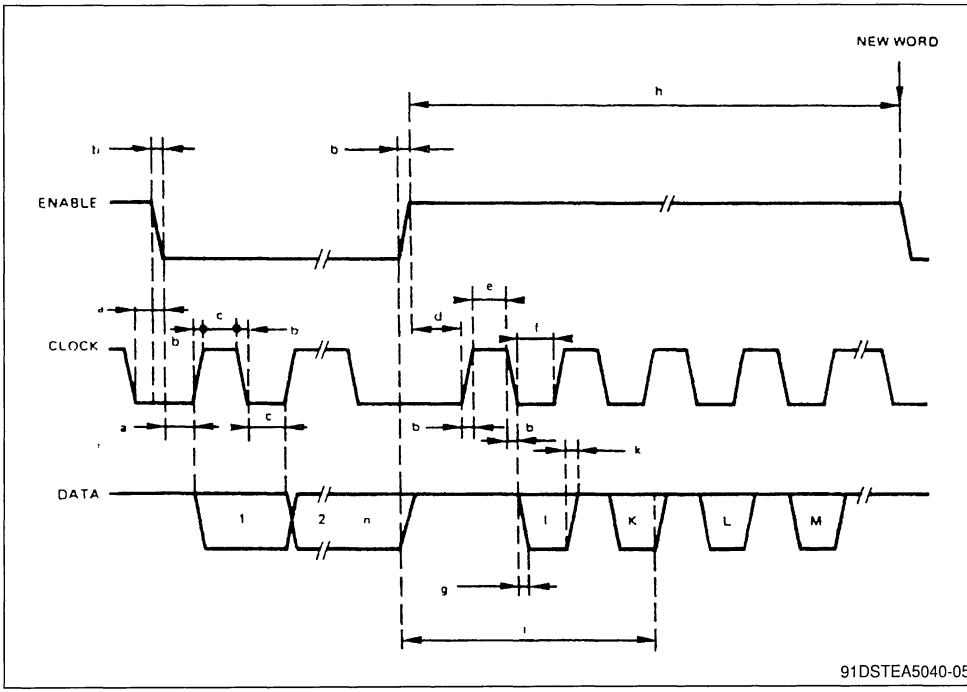
It is possible to select several IC from the microprocessor via the bus. The identification of each particular IC is achieved by the length of the word (number of data bits/clock pulses), meaning that each IC responds with its own particular word length.

The number is determined while ENABLE is low and by counting the negative clock edges. As soon as the high edge of the ENABLE signal is applied, the number is fixed (see figure 2).
The reply word lenght from any of the IC on the bi-directional line is four bits. If it is found insufficient then the reply word can be expanded to include two repetitive reply sequences one after the other.

The bi-directional transmission is enabled if :

- the IC has been previously addressed at the positive going edge of the enable pulse.
- ENABLE remains high,
  and DATA is available only during the period when the clock remains low.
- number of identification bits : n
  1...n : data from the microcomputer
- number of bi-directional clocks : 4
  1...M : data to the microcomputer

Figure 2.



The four bit reply word (synchronized with the clock coming from the microcontroller) from the addressed IC to the microcontroller is sent only once. Subsequent clock pulses present on the clock line will be ignored by the IC in question. The data sent to the microcontroller can generally be suppressed completely or partially, but in the case of the videoprocessor, a minimum reply word lenght of 1 has to be maintained (see figure 3).

This implies that a bi-directional bus that incorporates other IC's together with a videoprocessor IC is then also limited by the minimum reply word restriction of 1.

The data word from the microcompter is divided into :

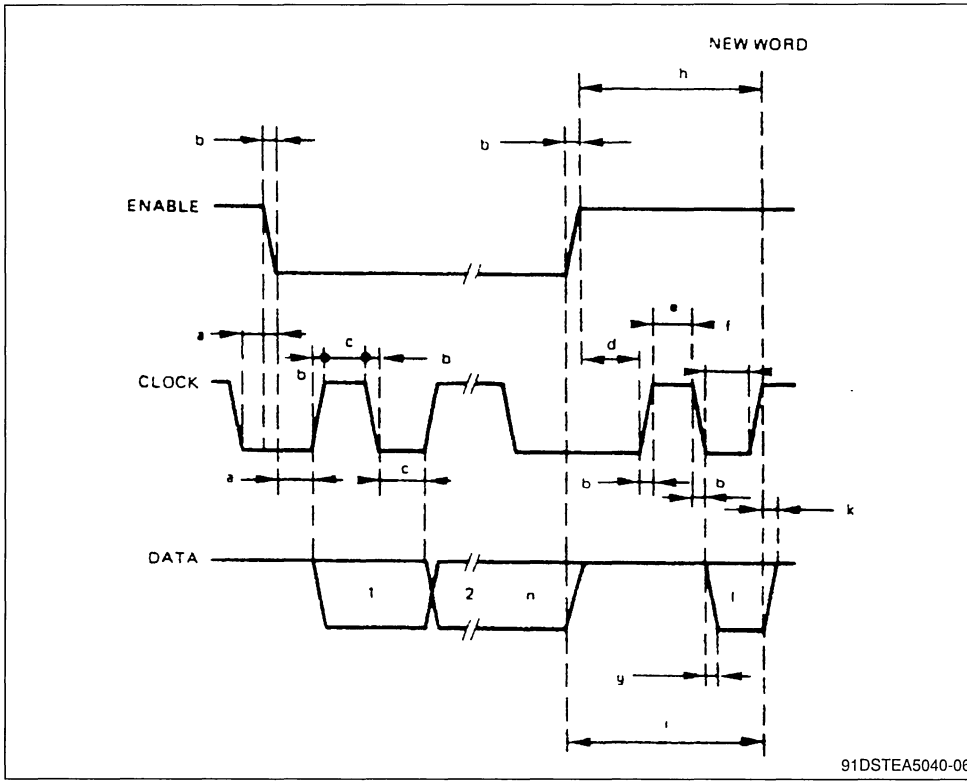
- addresses within the IC
- data

The data word to the microcomputer is divided into

- two data bits,
- two address bits

After the operating voltage is applied, the first transmission will be used as a reset command, i.e. the data word will not be detected.

Figure 3.



- number of identification bits : n
- number of bi-directional clocks : 1 (which is the minimum number for the videoprocessor)

1...n : data from the microcomputer
1 : data the microcomputer

BI-DIRECTIONAL DATA BUS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	TIMING Identification nr-9 (9 video processor address) (see figures 2-3)				
a		5			µs
b		0			µs
c		5			µs
d		70			µs
e	N/A				
f	N/A				
g	N/A				
h	(new word to same IC)	24			ms
h	(new word to other IC)	70			µs

TAB-03

ABSOLUTE MAXIMUM RATINGS

T_{AMB} = 25°C (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage Pin 1	14		V
T_{OPER}	Operating Temperature Range	0	+ 60	°C
T_{STG}	Storage Temperature Range	– 25	+ 125	°C

TAB-04

THERMAL DATA

$R_{th(j-a)}$	Junction-ambiant Thermal Resistance DIP40 SHRINK42	Max. Typ.	55 60	°C/W °C/W

TAB-05

ELECTRICAL OPERATING CHARACTERISTICS

T_{AMB} = 25°C, V_{CC} = 12V (unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Pin 1	10.8	12	12.5	V
I_{CC}	Supply Current Pin 1		80	104	mA
	Video Switch				
	External Video Input (75Ω source impedance)				
V_{35}	Signal Amplitude Pin 35		1	1.4	
I_{35}	Input Current Pin 35		10	30	Vpp µA
	Internal Video Input (300Ω source impedance)				
V_{37}	Signal Amplitude Pin 37		1	14	Vpp
I_{37}	Input Current Pin 37		10	30	µA
	Synchro Input				
	Output Signal Amplitude Pin 39 (for a 0.5V to 2.5V input signal on pin 39)	0.5	0.6		V
	Internal Video Output Pin 38				
	Dynamic	2.7			Vpp
	DC Level (bottom of synchro pulse)	1		2	V
	Gain between Pin 38 and Pin 37 (for 1Vpp on pin 37)	5	6	7	dB
	Crosstalk between Pin 35 and Pin 38			– 50	dB
	Bandwidth (– 1dB)	6			MHz
	Switchable Video Output Pin 40				
	Dynamic (pin 35 or pin 37 selected)	2.7			Vpp
	Gain between Pins 35-40 (for 1VPP on pin 35)	5		7	dB
	Gain between Pins 37-40 (for 1VPP on pin 37)	5		7	dB
	Crosstalk between Pins 35-40			– 50	dB
	Crosstalk between Pins 37-40			– 50	dB
	Bandwidth (– 1dB)	6			MHz
	TV Mode Inputs				
	Luminance Input Pin 12				
Y	Signal Amplitude (100% white)		1	1.5	V_{pp}
V_{12}	DC Level (on black level)		4		V
I_{12}	Input Current			10	µA
	R-Y Input Pin 11				
R-Y	Signal Amplitude (75% saturation)		1.05	1.47	V_{pp}
V_{11}	DC Level (on black level)		4.7		V
I_{11}	Input Current			2	µA
	B-Y Input Pin 10				
B-Y	Signal Amplitude (75% saturation)		1.33	1.86	V_{pp}
V_{10}	DC Level (on black level)		4.7		V
I_{10}	Input Current			2	µA

TAB-06

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	RGB Inputs Pins 2-3-4-5-6-7				
	Signal Amplitude (100% saturation without synchro pulse)		0.7	1	V_{pp}
	DC Level (on black level)		3.2		V
	Input Current			3	µA
	Fast Blanking Inputs Pins 8-9				
	TV/RGB Mode Threshold	0.5		0.9	V
	Switching Time		70		ns
	Switching Time Delay		70		ns
	Clamp Memory Output Pins 17-18-19				
	Voltage Range	8	10	11	V
	Input Current			2	µA
V_{REF}	**Reference Voltage Pin 16**		4		V
	Sandcastle Input Pin 30				
	Blanking Threshold	1	1.4	1.8	V
	Burst Gate Threshold	6.4	6.9	7.6	V
	Line Retrace Threshold	3.1	3.4	3.8	V
	Input Current Pin 30 Grounded			100	µA
	Drive and Cut-off Memory Output Pins 21-22-24-25-27-28				
	Drive Leakage Current Pins 21-24-27			1	µA
	Cut-off Leakage Current Pins 22-25-28			1	µA
	Minimum Active Level Pins 22-25-28		4		V
	Leakage Current Memory Output Pin 33				
	Voltage Range	3			V
	Input Current (during picture pin 33 = 5V)			0.5	µA
	Charging Output Impedance			500	Ω
	Minimum Voltage (pin 32 grounded)		3		V
	Cathode Currents Input Pin 32				
	Output Current during the Line Trace (pin 32 grounded)			10	µA
	Voltage during Lines 17, 18, 19	0.275	0.35	0.44	V
	Voltage Difference during Lines 21, 22, 23 and during Line 20		0.4		V
	Voltage Amplitude on Cathode Currents Input for Drive Decrease Threshold 10% on Drive/cut-off				
V32	1V on Pin 36		0.7		V
V32	2V on Pin 36		1.4		V
	Voltage Amplitude on Cathode Currents Input for Brightness Decrease Threshold				
V32	1V on Pin 36		1		V
V32	2V on Pin 36		2		V
	Impedance SWITCH Pin 31				
	Saturation Impedance [for 5mA] (open during lines 20, 21, 22, 23)		250		Ω
	Reference Voltage Input for the Average Beam Current Limiter Pin 36				
V36	Reference Voltage	0		5	V
I36	Input Current (V36 = 1V)			– 20	µA
	Average Beam Current FILTER Pin 34 Voltage Range				
	0 < V32 < 7V	6			V

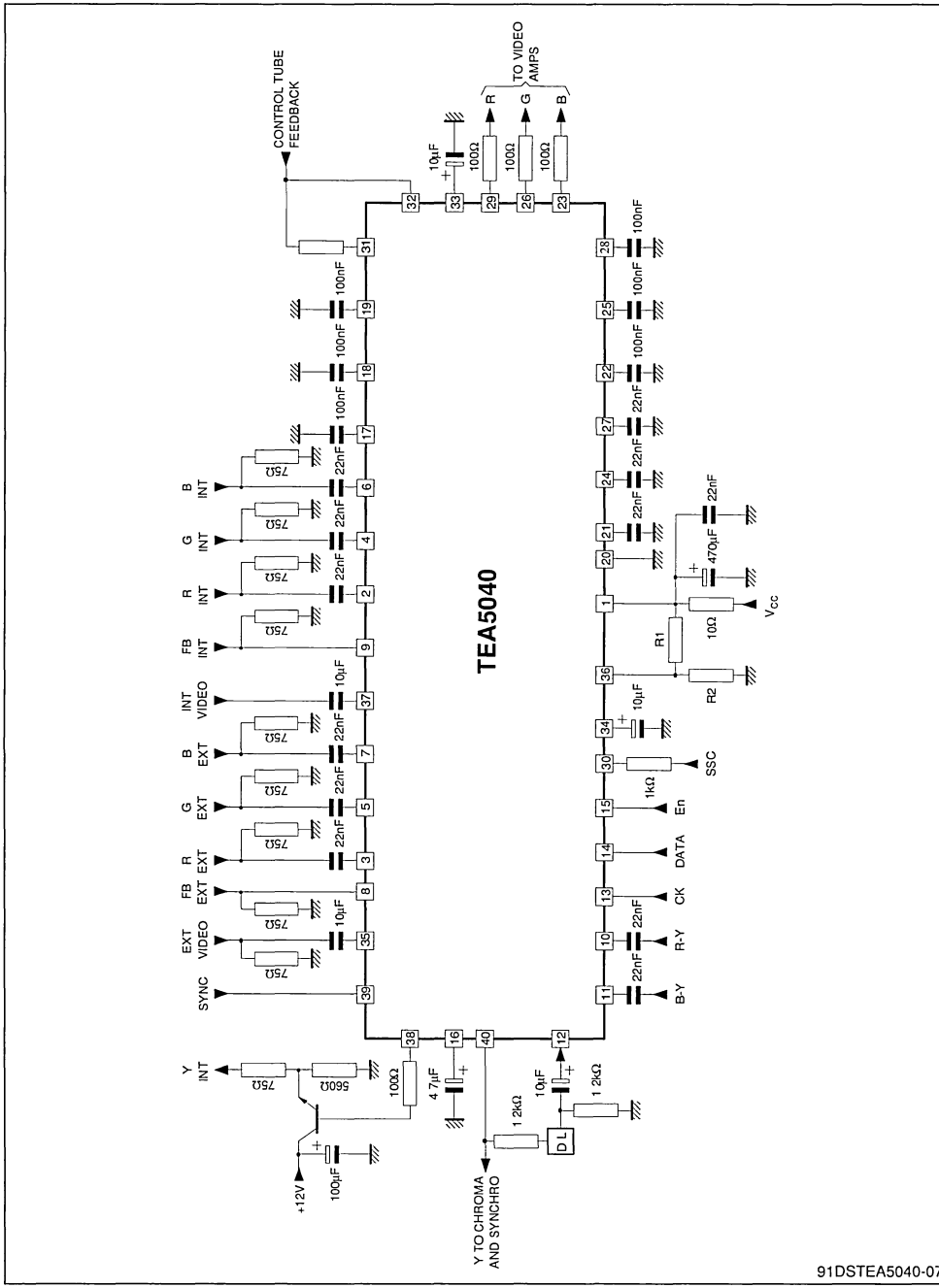
TAB-07

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	RGB Outputs R (pin 23), G (pin 26), B (pin 29)				
	Inserted Levels				
	Low Clipping Level Referred to quasi Cut-off Inserted Level (100% = B/W output signal at maximum contrast with 0.5V (B/W) input Y signal)		45		%
	High Clipping Level Referred to quasi Cut-off Inserted Level (100% = B/W output signal at maximum contrast with 0.5V (B/W) input Y signal)		115		%
	Drive Inserted Level Referred to quasi Cut-off Inserted Level (without beam limitation, V36 = 6V, V32 grounded)		35		%
	Bandwidth (– 3dB) (TV mode and R, G, B mode)		10		MHz
	Crosstalk for any of the 11 Inputs Pins 2-3-4-5-6-7-10-11-12-35-37 on any of the 5 Outputs Pins 23-26-29-38-40 (range : DC to 1MHz)			– 50	dB
	Brightness				
	Nominal Brightness Referred to quasi Cut-off Inserted Level (bit word "10000" address = 0)		– 25		%
	Total Brightness Range (100 % = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)		78		%
	Maximum Brightness (100% = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)		38		%
	Minimum Brightness (100% = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)		– 40		%
	Differential Brightness between any two Channels (TV mode, colour off, pins 10-11-12 AC grounded, 0.5 (W/B) signal on pin 12, maximum contrast = 100% on RGB outputs)		2		%
	Variation of the Differential Brightness (in the whole saturation control range (including colour off))		0.5		%
	Contrast : Max. Contrast Attenuation	11			dB
	Saturation				
	Max. Saturation		6		dB
	Max. Saturation Attenuation	20			dB
	Colour off Attenuation	40			dB
	Output Signal Amplitude Pins 23-26-29 (blanking to high clipping) • Y input : 0.7V B/W • 0dB Contrast, Bit Word = 010110, Address = 1 • Maximum Brightness • Maximum Drive Efficiency (Pins 21-24-26-27 grounded) • No Average Beam Current Limitation (Pin 36 to 6V)		6.2		V
	Black to White Output Voltage Y Input : 0.5V (B/W) Maximum Contrast (Pin 36 to 6V, Pins 21-24-27 grounded)		3.6		V
	Drive Efficiency Ratio : $\frac{V_{OUT} \text{ (Pins 21–24–27 grounded)}}{V_{OUT} \text{ (Pins 21–24–27 to } V_{CC})}$ (no average beam current limitation Pin 36 to 6V)		3.4		
	Black Level Control (variable DC voltage from 4V to V_{CC} on Pins 22-25-28)	4.3			V
	Bus Inputs Pins 13-14-15				
V_{HL}	High Level	3.5			V
V_{LL}	Low Level			1	V

TAB-08

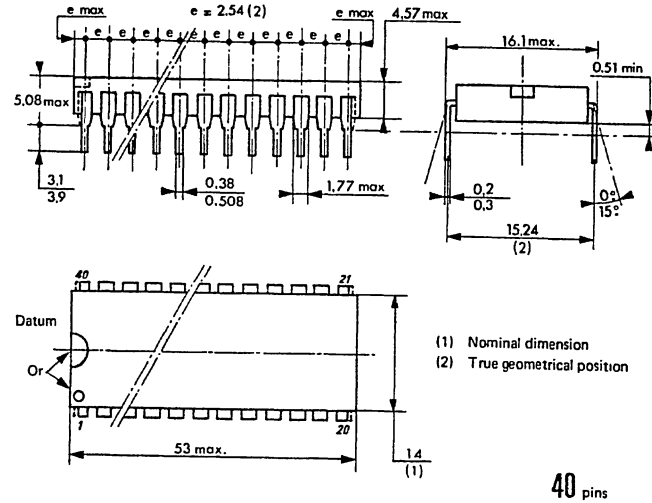
APPLICATION CIRCUIT



PACKAGE MECHANICAL DATA

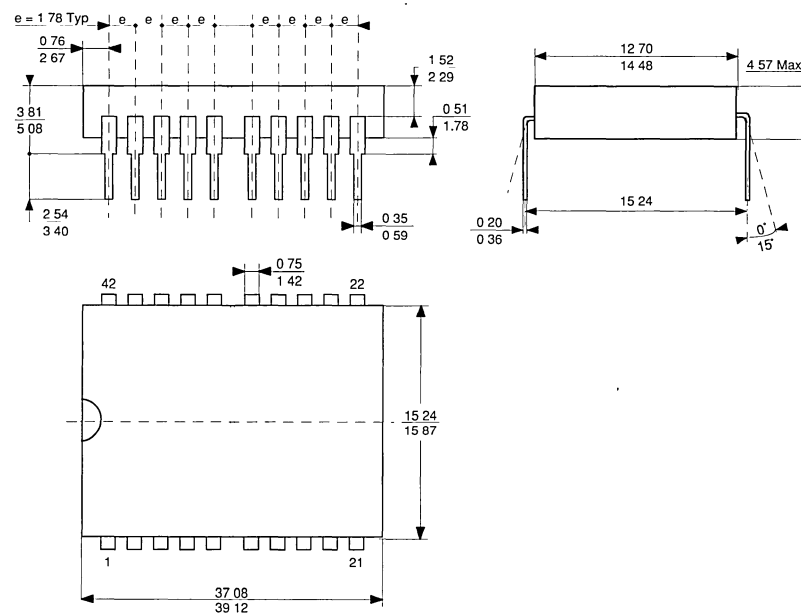
40 PINS – PLASTIC DIP

Dimensions in mm



42 PINS – PLASTIC SHRINK

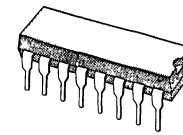
Dimensions in mm



TEA5114A

RGB SWITCHING CIRCUIT

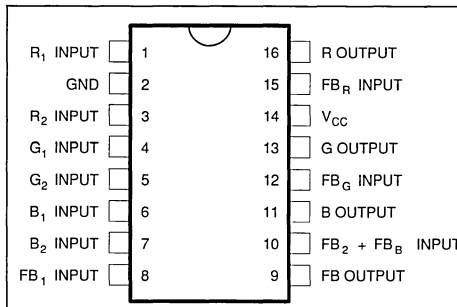
- 25 MHz BANDWIDTH
- CROSSTALK : 55 dB
- SHORT CIRCUIT TO GROUND OR V_{CC} PROTECTED
- ANTI SATURATION GAIN CHANGING
- VIDEO SWITCHING



DIP16
(Plastic package)

ORDER CODE : TEA5114A

PIN CONNECTIONS



91DSTEA5114A-01

DESCRIPTION

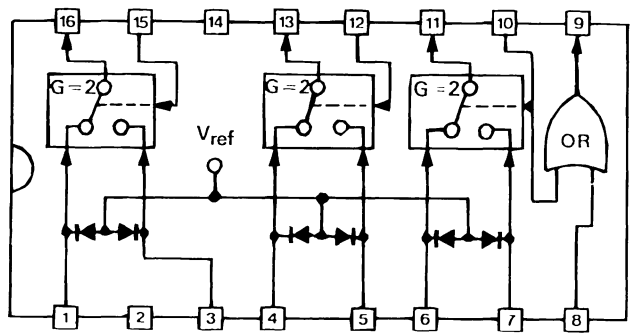
This integrated circuit provides RGB switching allowing connections between peri TV plug, internal RGB generator and video processor in a TV set.

The input signal black level is tied to the same reference voltage on each input in order to have no differential voltage when switching two RGB generators.

An AC output signal higher than 2 Vpp makes gain going slowly down to 0 dB to protect the TV set video amplifier from saturation.

Fast blanking output is a logicial OR between FB1 (Pin 8) and FB2 (Pin 10).

BLOCK DIAGRAM



88DSTEA5114A-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
T_j	Junction Temperature	– 40 to 150	°C
T_{stg}	Storage Temperature	– 40 to 150	°C
Z_L	Minimum Load Resistor on Each Output V_{CC} = 12 V V_{CC} = 10 V	300 150	Ω Ω
T_{amb}	Operating Ambient Temperature	0 to 70	°C

TAB-01

THERMAL DATA

$R_{th(j-a)}$	Junction-ambient Thermal Resistance	80	°C/W

TAB-02

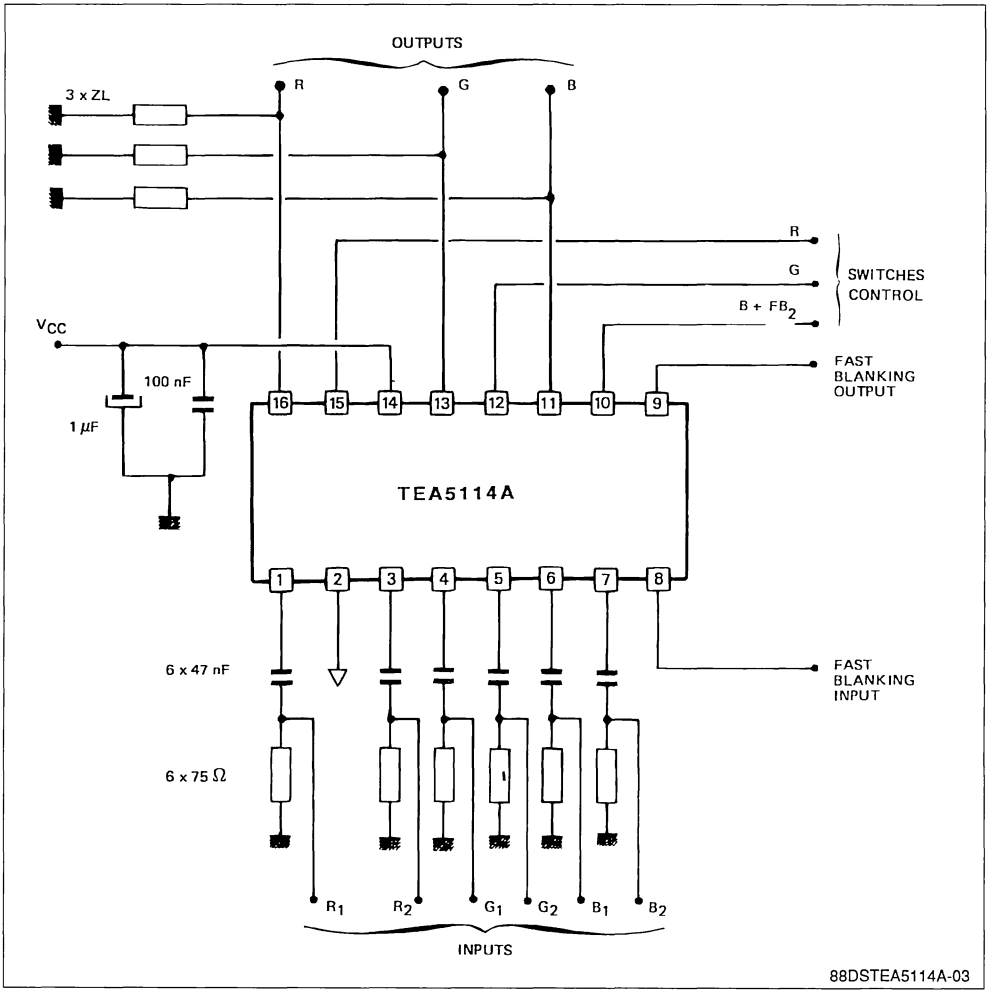
ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 12 V, Z_L (RGB) = 300 Ω
V_{CC} = 10 V, Z_L (RGB) = 150 Ω (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	9	12	13.2	V
I_{CC}	Supply Current without Load V_{CC} = 12 V	20	30	40	mA
V_{ON}	Black Level Output Voltage (on pins 11, 13, 16 square wave output signal 1 kHz - 1 Vpp) T_j = 25 °C (5mV/°C typical variation)	1.8	2.5	2.9	V
G_{RGB}	Gain of Each Channel Pins 11, 13, 16 F = 1 MHz , V_{in} = 0.5 V_{pp}	5	5.5	6	dB
B_{RGB}	Bandwidth (– 3 dB) V_O = 1 V_{pp}	18	22		MHz
V_{GC}	Threshold Output Voltage for Gain Changing (– 0.5 dB)	2			V_{pp}
V_R	Video Rejection between Two Inputs R, G or B F = 1 MHz Sinus V_O = 1 V_{pp}	50	55		dB
Z_{IRGB}	Input Impedance on Pins 1, 3, 4, 5, 6, 7 V_O = 1 V_{pp}	10			kΩ
Z_{ORGB}	R, G, B Output Impedance on Pins 11, 13, 16			15	Ω
T_{FB}	FB rising and falling time on pin 9. 1 Vpp Input Voltage Pins 8, 10		20		ns
V_{IHFB}	FB High Level Input Voltage on Pins 8, 10, 12, 15	1		4	V
V_{ILFB}	FB Low Level Input Voltage on Pins 8, 10, 12, 15	0		0.4	V
Z_{IFB}	Input Impedance on Pins 8, 10, 12, 15	0.7	1	1.3	kΩ
V_{OHFB}	High Level FB Output Voltage (pin 9) Input 1 V on Pins 8, 10	0.8	1	1.2	V
V_{OLFB}	Low Level FB Output (pin 9) Input 0 V on Pins 8, 10			0.3	V
Z_{OFB}	FB Output Impedance Pin 9 High Level			30	Ω
T_{dFBRGB}	Delay Time between FB Inputs and R, G, B Switching		20		ns

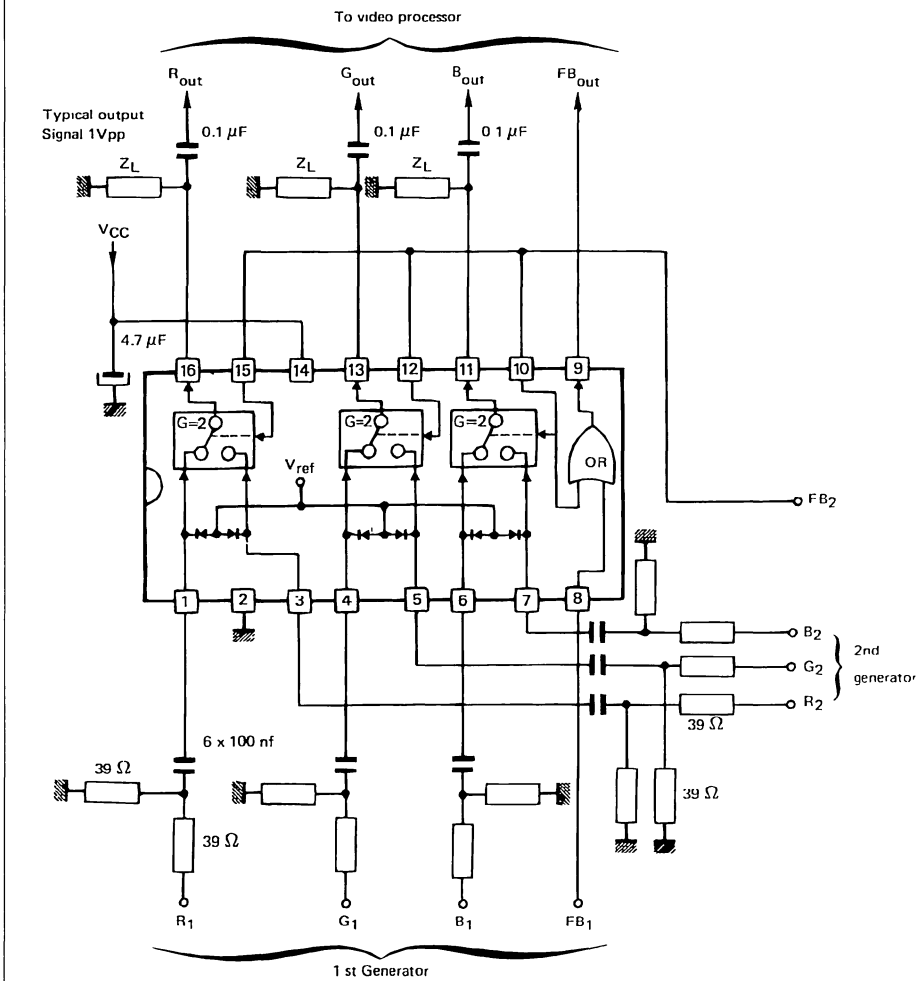
TAB-03

TEST DIAGRAM



TYPICAL R, G, B SWITCHING APPLICATION

V_{CC} = 12 V $Z_L \geq 300\ \Omega$.
V_{CC} = 10 V $Z_L \geq 150\ \Omega$.

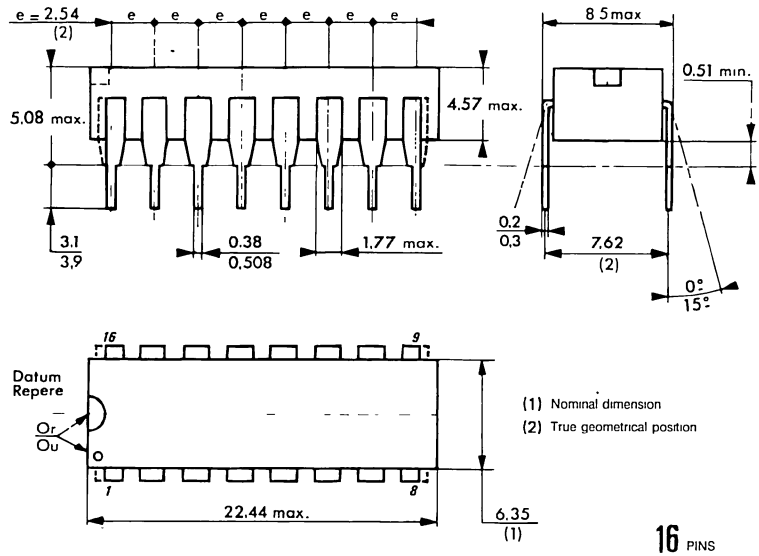


Peritelevision plug standard input value 1 Vpp

88DSTEA5114A-04

PACKAGE MECHANICAL DATA

16 Pins – Plastic DIP

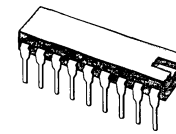


SGS-THOMSON MICROELECTRONICS

TEA5115

5 CHANNELS VIDEO SWITCH

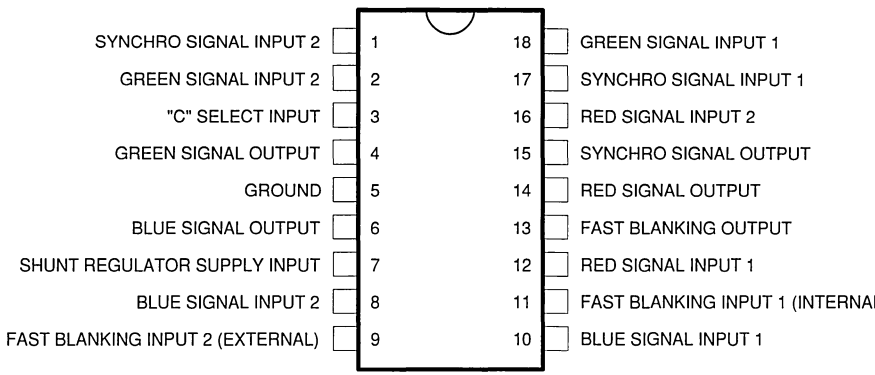
- EACH CHANNEL EXCEPT FAST BLANKING HAS 6dB GAIN
- R, G, B AND VIDEO SIGNALS ARE CLAMPED TO THE SAME REFERENCE VOLTAGE IN ORDER TO HAVE NO OUTPUT DIFFERENTIAL VOLTAGE WHEN SWITCHING
- ALL INPUT LEVELS COMPATIBLE WITH NFC 92250 AND EN 50049 NORMS
- 30MHz BAND WIDTH FOR R, G, B SIGNALS
- INTERNAL 6.7V SHUNT REGULATOR FOR :
  - LOW IMPEDANCE LOADS,
  - POWER DISSIPATION LIMITATION
- INDEPENDANT VIDEO OR SYNCHRONIZING SIGNAL SELECTION
- SIMULTANEOUS SWITCHING OF R, G, B AND FB SIGNALS BY FB1 INPUT (internal)



DIP18
(Plastic Package)

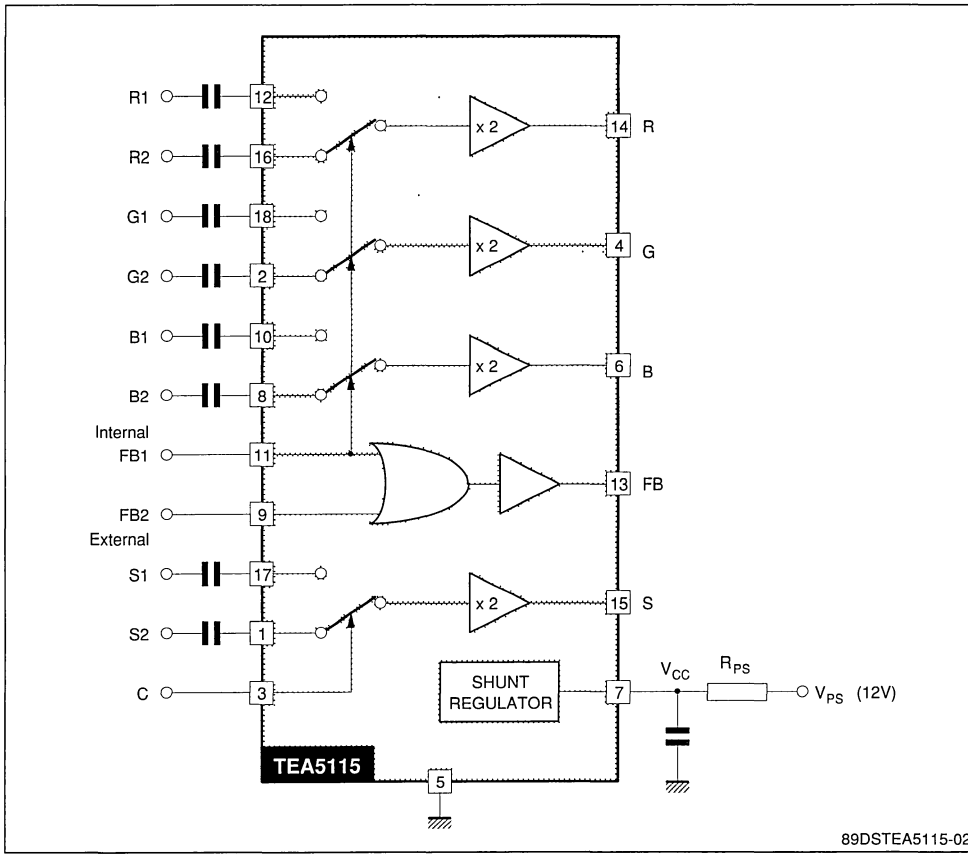
ORDER CODE : TEA5115

PIN CONNECTION



91DSTEA5115-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_{CC}	Supply Current (see note)	150	mA
V_{in}	Input Voltage (all inputs)	– 0.5 to V_{CC} + 0.5	V
T_{oper}	Operating Temperature Range	0 to 70	°C
T_j	Junction Temperature	– 40 to + 150	°C
T_{stg}	Storage Temperature	– 40 to + 150	°C

TAB-01

Note : Minimum output load is 300 Ω in case of all outputs loaded

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

TAB-02

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C, I_{CC} = 120 mA ; Load value = 150 Ω
(sequentially switched) (unless otherwise specified, refer to test circuit page 7)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Internal Shunt Regulator	I_{CC} = 120 mA I_{CC} = 90 mA I_{CC} = 150 mA	6.3 6.2 6.2	6.7	7.2 7.3 7.3	V V V

R, G, B Switches (pins 4, 6, 14) (Time Measurement Conditions : Δ inputs RGB = 0.7 V_{pp} ; FB input pulse amplitude = 2 V)

V_C	DC Output Voltage (no input voltage)	$T_{junction}$ = 25 °C $T_{junction}$ stabilized		0.9 1.2	1.25	V
V_{AC}	Max Output Swing Voltage		2	4.0		V_{pp}
B	Bandwidth (– 3 dB) (input voltage 0.7 V_{pp})		20	30		MHz
A_v	Gain of Each Channel (input voltage 0.7 V_{pp} ; F = 1MHz)		5.5	6	6.5	dB
A_{dc}	Gain Difference Between any two R, G, B Channels (input voltage 0.7 V_{pp} ; F = 1 MHz)			0.1	0.5	dB
	Input Swing			0.7 V ± 3dB		
z_{ic}	DC Input Impedance			10		kΩ
z_{oc}	Dynamic Output Impedance (input voltage 0.7 V_{pp} ; F = 1MHz) with R_{load} = 300 Ω			10		Ω
	Crosstalk between any inputs (R1 and R2 or B1 and B2 or G1 and G2) (input voltage 0.7 V_{pp} ; F = 1 MHz).		45	55		dB
	Crosstalk between any outputs (input voltage 0.7 V_{pp} ; F = 1 MHz).		40	55		dB
t_{dc}	Delay time between R, G, B inputs and RGB outputs.			10		ns
t_{sr1}	Switching rise time between FB1 input signal and R, G, B output signal.			60	110	ns
t_{sf1}	Switching fall time between FB1 input signal and R, G, B output signal.			10	40	ns
t_{sr2}	Switching rise time between FB2 input signal and R, G, B output signal.			10		ns
t_{sf2}	Switching fall time between FB2 input signal and R, G, B output signal.			10		ns
t_{d11} t_{d12}	R1, G1, B1 Decay Time			30 60		ns ns
t_{d21} t_{d22}	R2, G2, B2 Decay Time			45 40		ns ns

Fast Blanking Switch (pin 13)
(time measurement conditions : FB input pulse amplitude = 2 V)

V_{IL}	Low Level Input Voltage FB1 and FB2		- 0.5		0.45	V
V_{IH}	High Level Input Voltage FB2 External		1		V_{CC}+0.5	V
V_{IH}	High Level Input Voltage FB1 Internal		1.2		V_{CC}+0.5	V
V_{OL}	Low Level Output Voltage				0.6	V
V_{OH}	High Level Output Voltage	$T_{junction}$ = 25°C $T_{junction}$ stabilized	1.4 1.5	1.7 1.9	3.5	V V
	Input Current (without load)			1.5		µA
	Dynamic Output Impedance : with R_{load} = 300 Ω			10		Ω
t_{FB1r}	Switching rise time between FB1 input and FB output.			120	160	ns
t_{FB1f}	Switching fall time between FB1 input and FB output.			25	60	ns

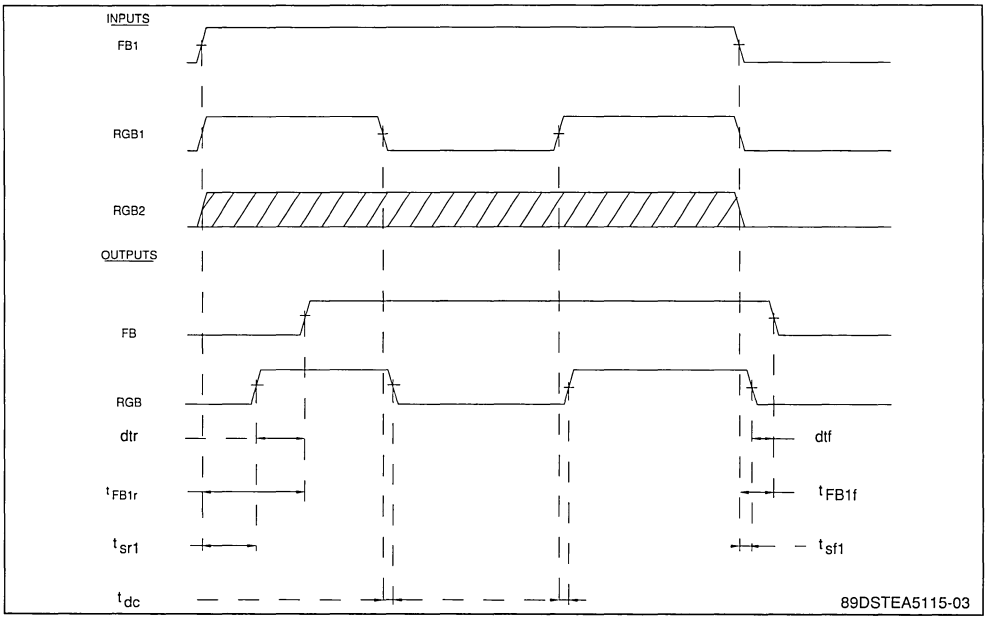
TAB-03

ELECTRICAL CHARACTERISTICS (continued)

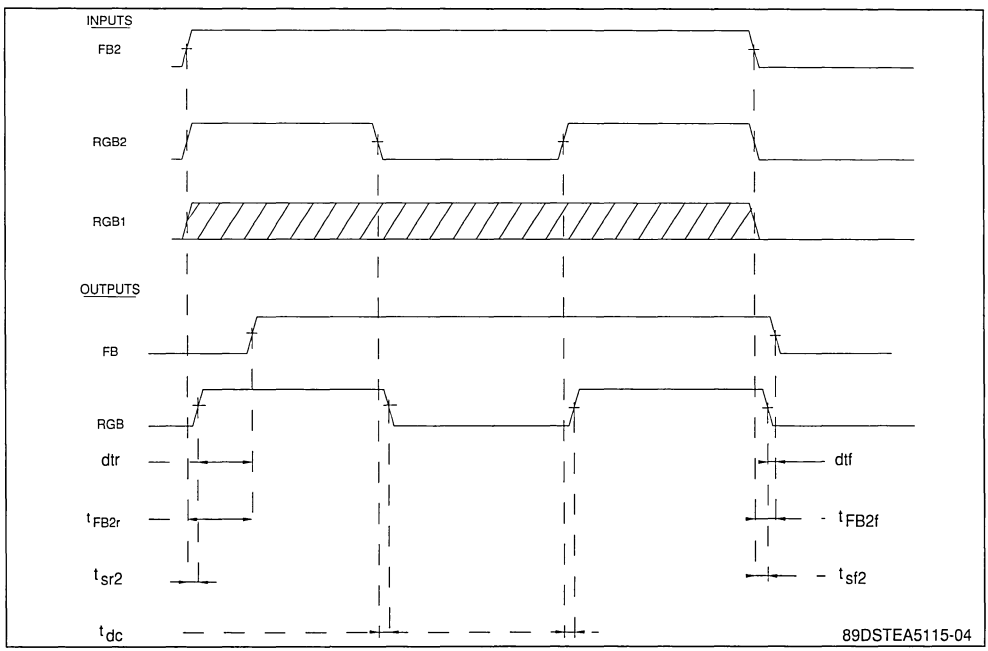
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{FB2r}	Switching rise time between FB2 input and FB output.		70		ns
t_{FB2f}	Switching fall time between FB2 input and FB output.		35		ns
d_{tr}	Delay Between RGB Output Signal and FB Output Signal (rise time)		50	100	ns
d_{tf}	Delay Between RGB Output Signal and FB Output Signal (fall time)		20	40	ns
Video (or synchro) **Signal Switch** (pin 15)					
V_S	DC Output Voltage (no input voltage) $T_{junction}$ = 25°C $T_{junction}$ stabilized Max Output Swing Voltage DC Input Impedance Dynamic Output Impedance (input voltage 1V_{pp} ; F = 1 MHz) with R_{load} = 300 Ω Gain (input voltage 1 V_{pp} ; F = 1 MHz) Bandwidth (– 3 dB) (input voltage 1 V_{pp})	 2.6 5.5 15	 0.9 1.2 10 10 6 20	 1.25 6.5 	V V V_{pp} kΩ Ω dB MHz
	Input Swing		1V ± 3 dB		
t_{cr}	Switching rise time between C input signal and S output signal (C pulse amplitude 3 V).		30		ns
t_{cf}	Switching fall time between C input signal and S output signal (C pulse amplitude 3 V).		10		ns
t_{dc}	Delay Time Between S Input and S Output (Δ input 0.7 V_{pp})		10		ns
Select Input "C" (pin 3)					
V_{IL} V_{IH} I_{IL} I_{IH}	Low Level Input Voltage High Level Input Voltage Low Level Input Current (V_{IL} = 1 V) High Level Input Current (V_{IH} = 3 V)	– 0.5 2 – 0.6 	 	1 V_{CC}+0.5 – 0.1 0.5	V V mA mA

TAB-04

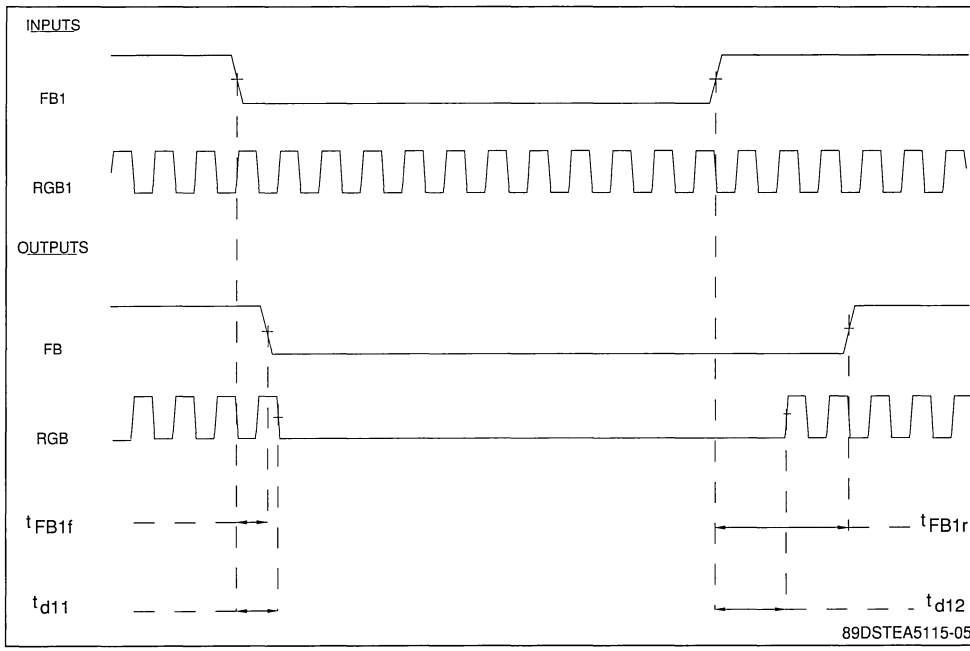
FB2 = 0


INPUTS
FB1
RGB1
RGB2
OUTPUTS
FB
RGB
dtr
dtf
tFB1r
tFB1f
tsr1
tsf1
tdc
89DSTEA5115-03

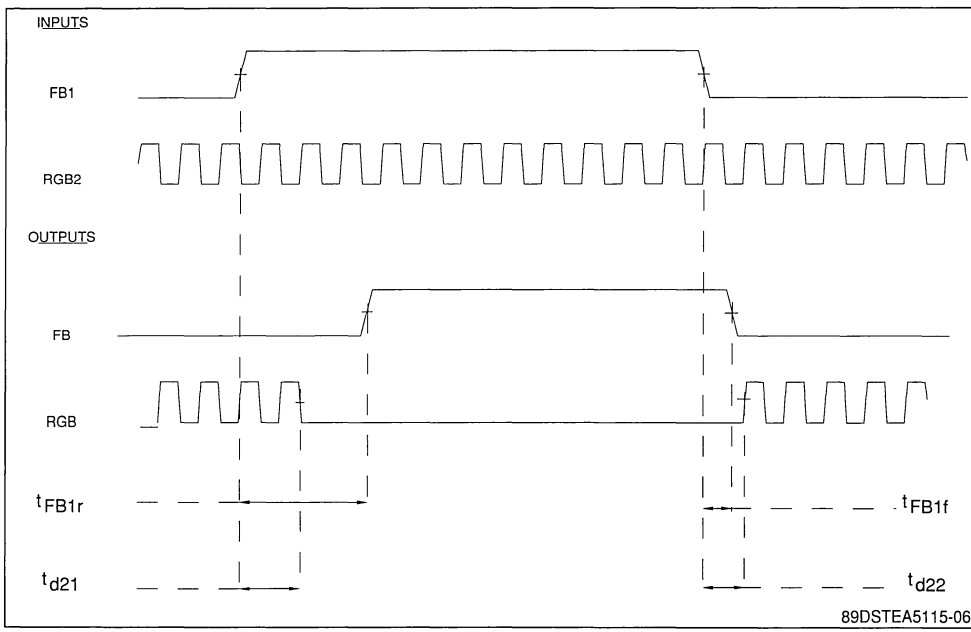
FB1 = 0

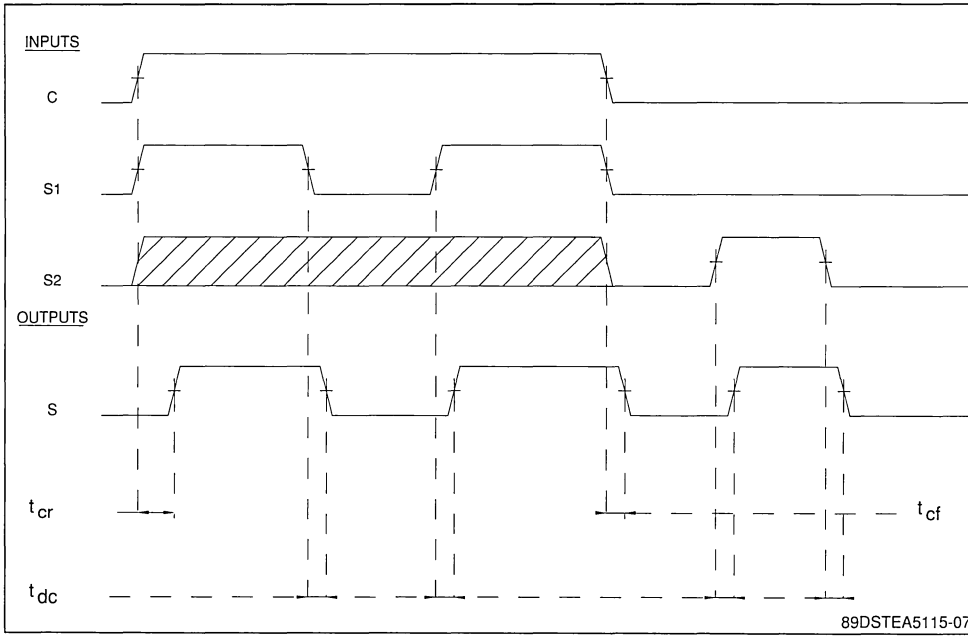

INPUTS
FB2
RGB2
RGB1
OUTPUTS
FB
RGB
dtr
dtf
tFB2r
tFB2f
tsr2
tsf2
tdc
89DSTEA5115-04

RGB2 = 0, FB2 = 0

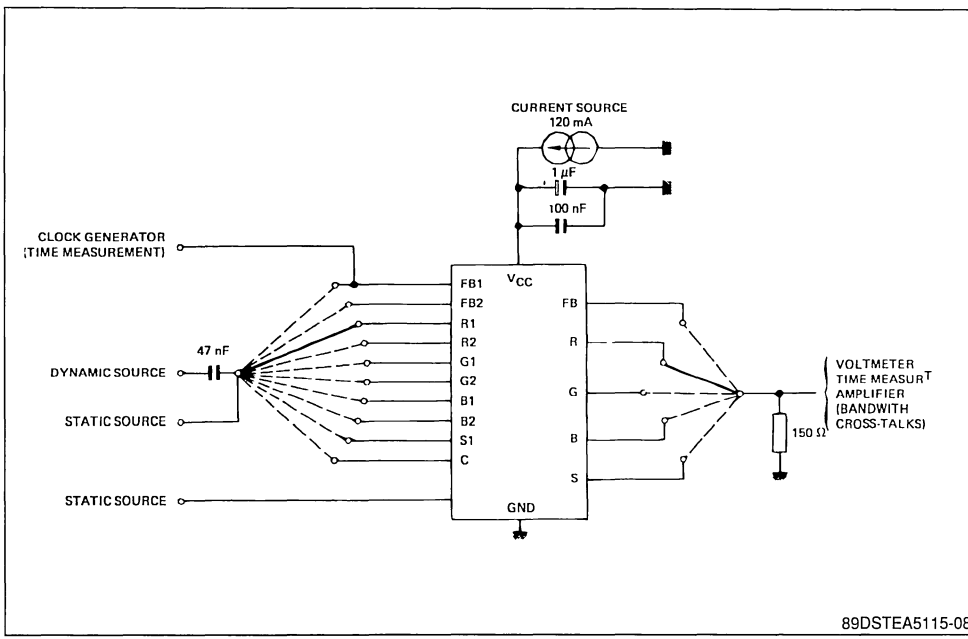


RGB1 = 0, FB2 = 0



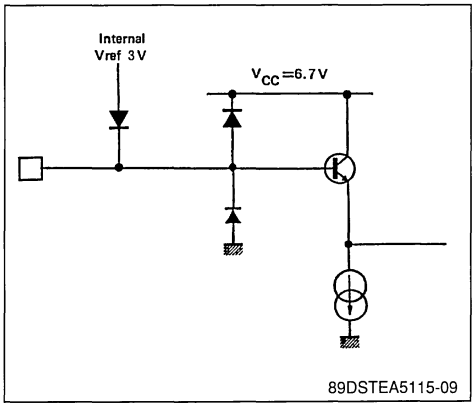


TEST CIRCUIT

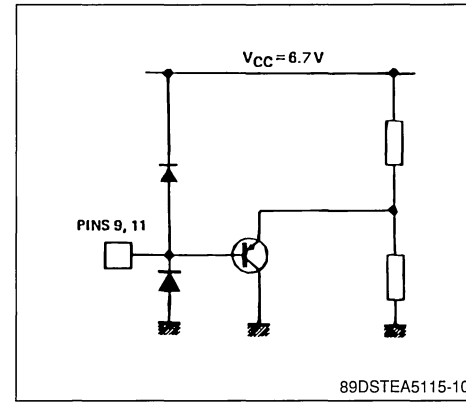


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

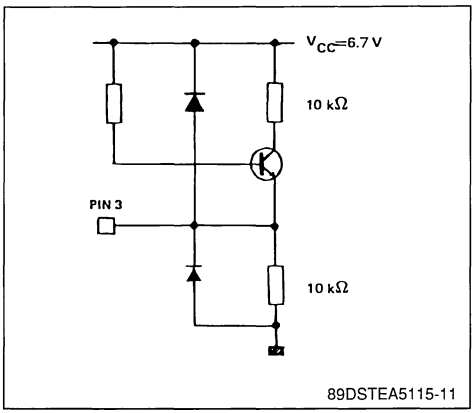
R, G, B, S inputs (pins 1, 2, 8, 10, 12, 16, 17, 18)



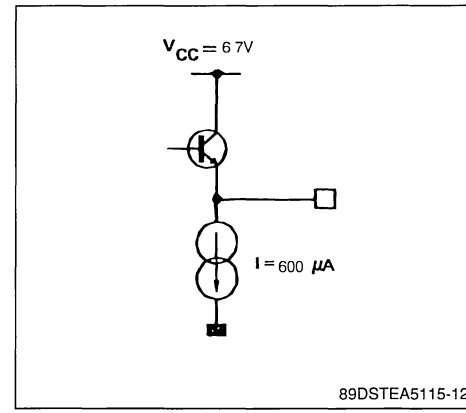
FB inputs (pins 9, 11)



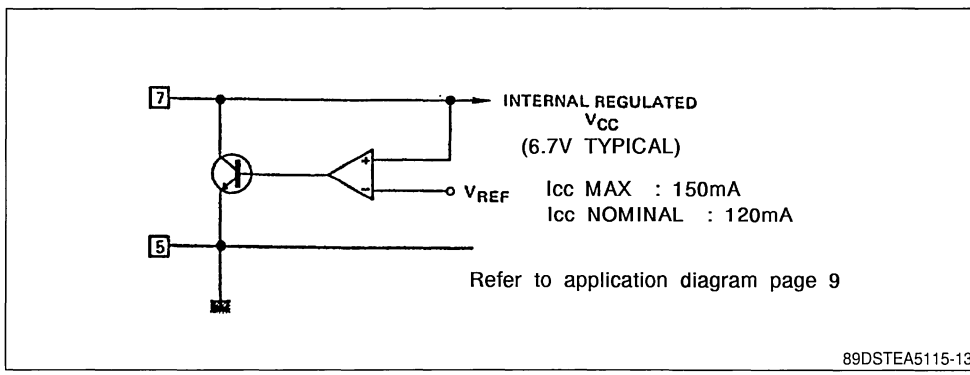
C input (pin 3)



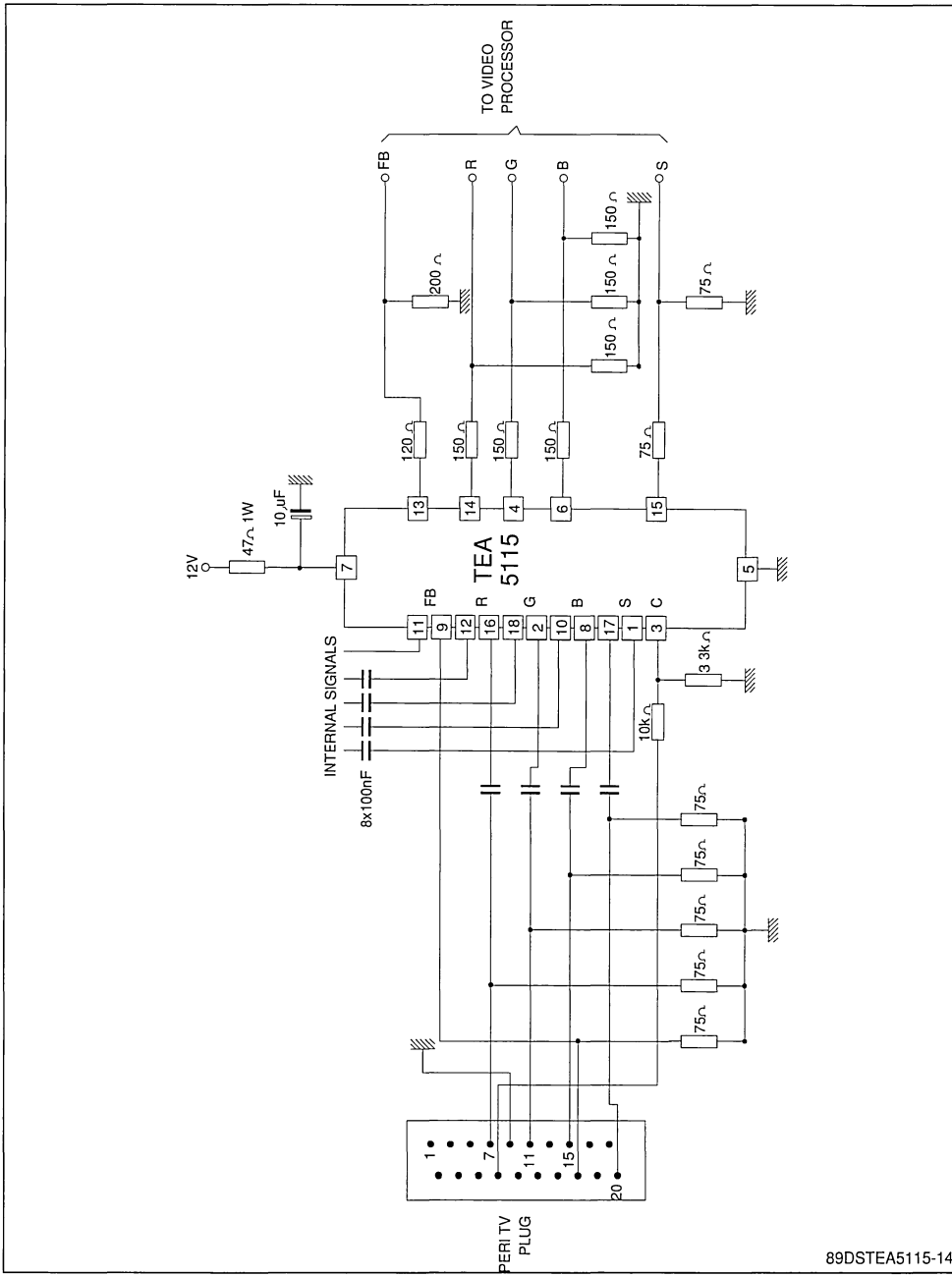
All Outputs (pins 4, 6, 13, 14, 15)



I_{CC} Supply (shunt transistor regulation system) (pin 7)

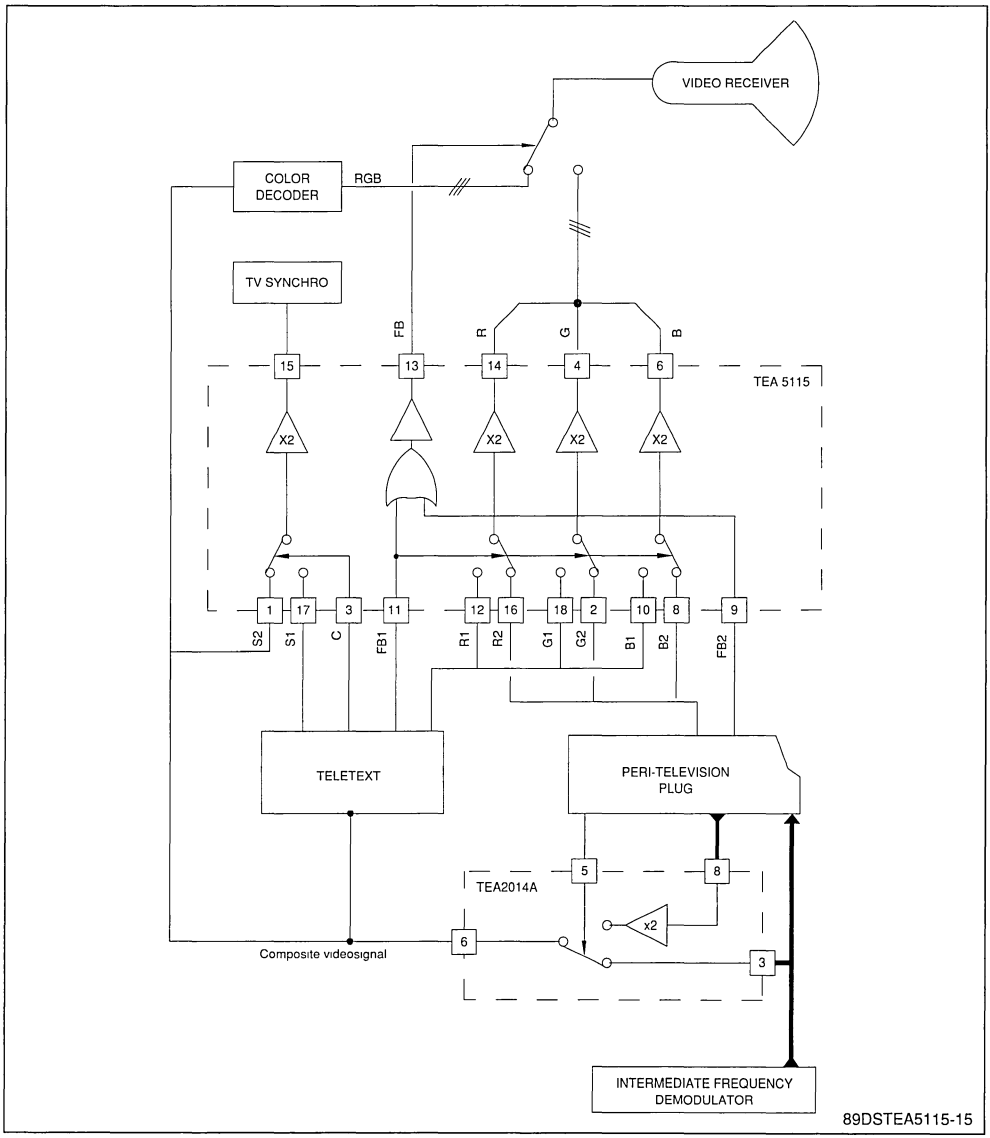


TYPICAL APPLICATION DIAGRAM



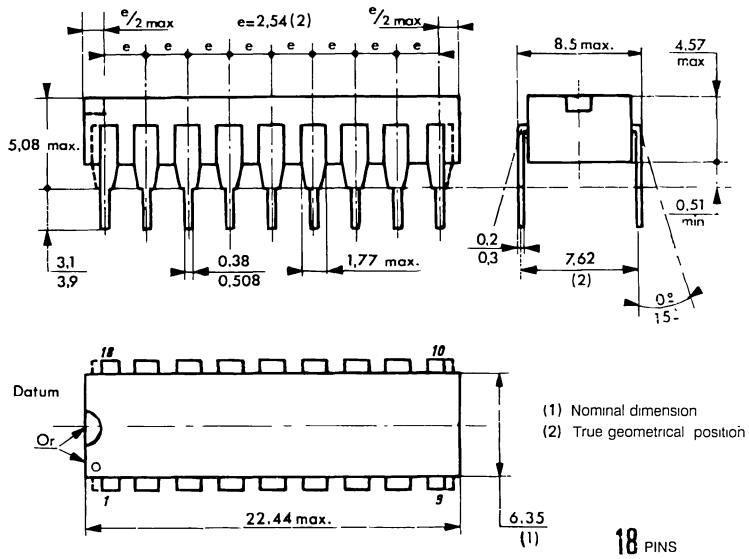
- Above given output load values are minimum values, in case of all output loading.
- Minimum output load is 150 Ω individually, provided that total supply current is less than 150 mA.

SIMAVELEC norm application with TEA5115 and TEA2014A.



PACKAGE MECHANICAL DATA

18 PINS – PLASTIC PACKAGE

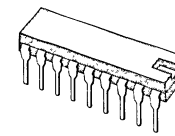


SGS-THOMSON MICROELECTRONICS

TEA5116

5 CHANNELS VIDEO SWITCH

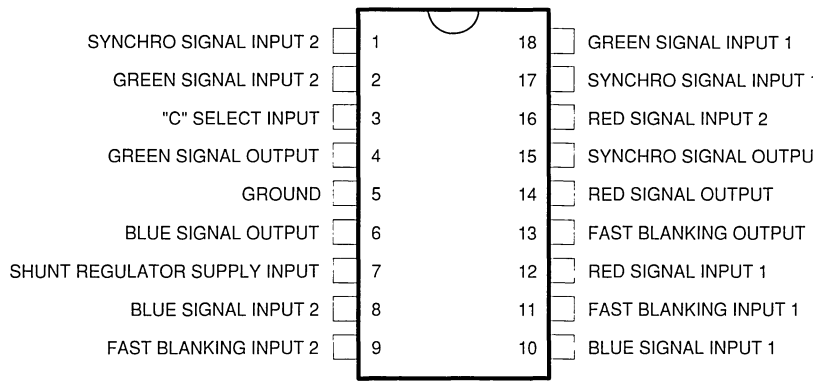
- EACH CHANNEL EXCEPT FAST BLANKING HAS 6 DB GAIN
- R, G, B AND VIDEO SIGNALS ARE CLAMPED TO THE SAME REFERENCE VOLTAGE IN ORDER TO HAVE NO OUTPUT DIFFERENTIAL VOLTAGE WHEN SWITCHING
- ALL INPUT LEVELS COMPATIBLE WITH NFC 92250 AND EN 50049 NORMS
- 30 MHZ BAND WIDTH FOR R, G, B SIGNALS
- INTERNAL 6.7 V SHUNT REGULATOR FOR
  - LOW IMPEDANCE LOADS,
  - POWER DISSIPATION LIMITATION
- THE FIVE CHANNELS ARE SIMULTANEOUSLY SWITCHED BY ONLY ONE SELECT INPUT



DIP18
(Plastic Package)

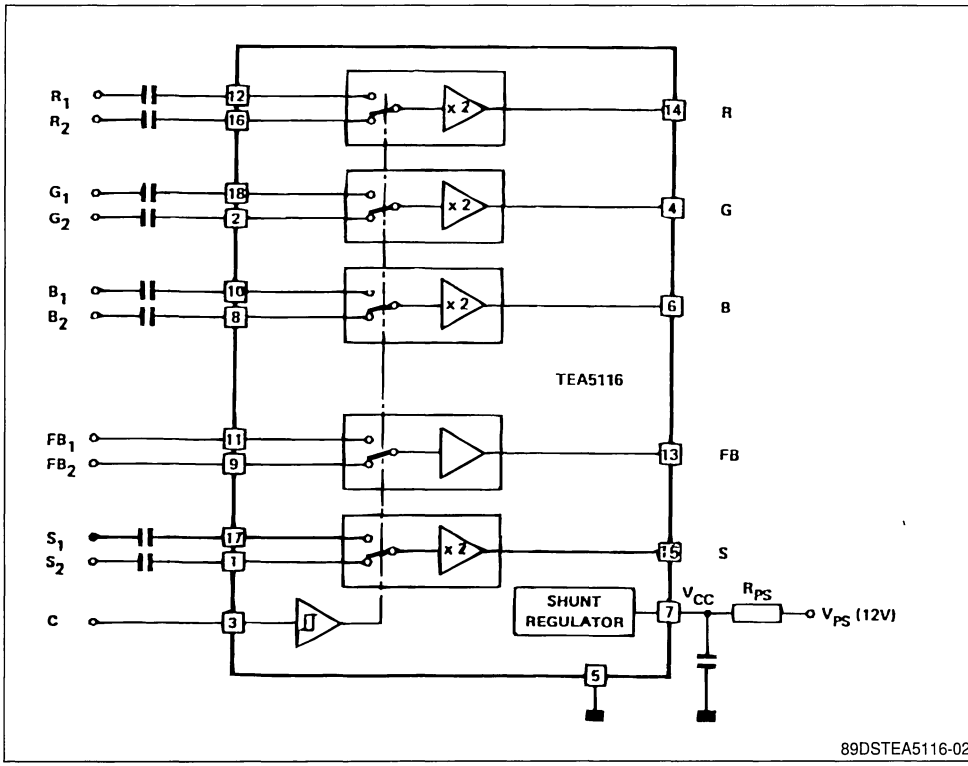
ORDER CODE : TEA5116

PIN CONNECTIONS



91DSTEA5116-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_{CC}	Supply Current (see note)	150	mA
V_{in}	Input Voltage (all inputs)	− 0.5 to V_{CC} + 0.5	V
T_{oper}	Operating Temperature Range	0 to 70	°C
T_j	Junction Temperature	− 40 to + 150	°C
T_{stg}	Storage Temperature	− 40 to + 150	°C

TAB-01

Note : Minimum output load is 300 Ω in case of all outputs loaded.

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

TAB-02

ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, I_{CC} = 120 mA ; Load value = 150 Ω (sequentially switched) (unless otherwise specified, refer to test circuit page 7)

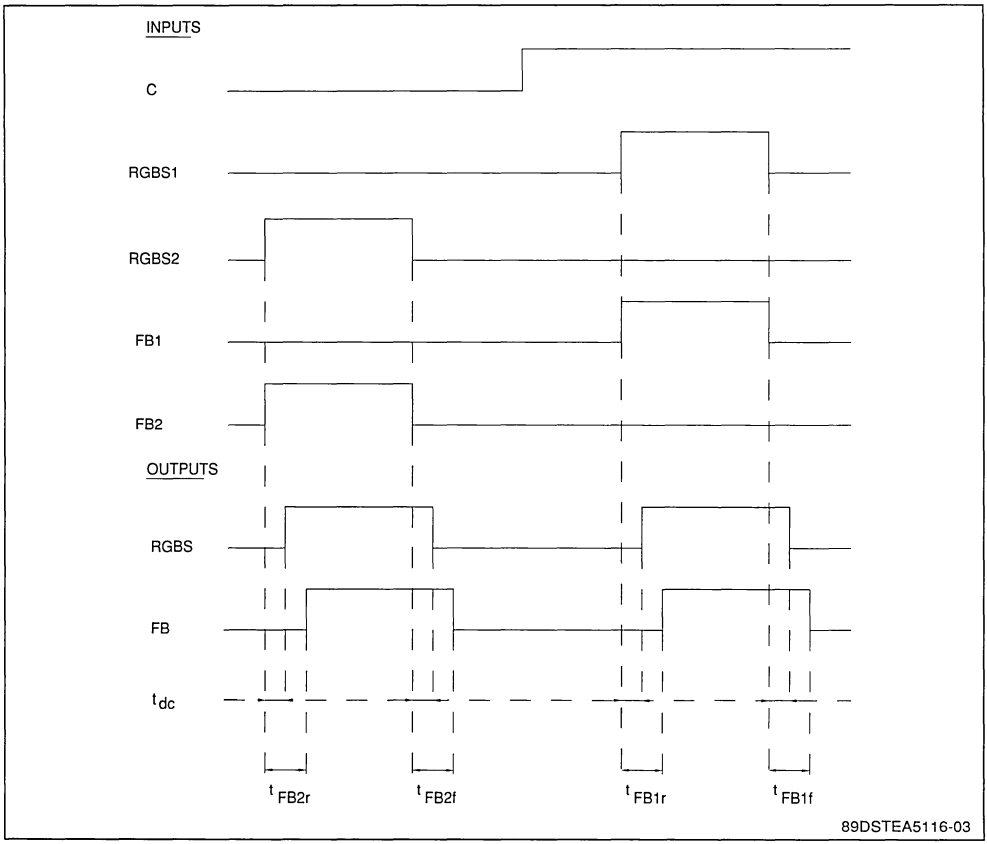
Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Internal Shunt Regulator	I_{CC} = 120 mA I_{CC} = 90 mA I_{CC} = 150 mA	6.3 6.2 6.2	6.7	7.2 7.3 7.3	V V V
R, G, B Switches (pins 4, 6, 14) - time measurement conditions : (Δ inputs RGB = 0.7 V_{pp} ; C pulse amplitude = 3 V)						
V_C	DC Output Voltage (no input voltage)	$T_{junction}$ = 25 °C $T_{junction}$ stabilized		0.9 1.2	1.25	V
V_{AC}	Max Output Swing Voltage		2	4		V_{pp}
B	Bandwidth (– 3 dB) (input voltage 0.7 V_{pp})		20	30		MHz
A_v	Gain of Each Channel (input voltage 0.7 V_{pp} ; F = 1MHz)		5.5	6	6.5	dB
A_{dc}	Gain Difference Between any two R, G, B Channels (input voltage 0.7 V_{pp} ; F = 1 MHz)			0.1	0.5	dB
	Input Swing			0.7 ± 3 dB		
z_{ic}	DC Input Impedance			10		kΩ
z_{oc}	Dynamic Output Impedance (input voltage 0.7 V_{pp} ; F = 1MHz) with R_{load} = 300 Ω			10		Ω
	Crosstalk between any inputs (R1 and R2 or B1 and B2 or G1 and G2) (input voltage 0.7 V_{pp} ; F = 1 MHz).		45	55		dB
	Crosstalk between any outputs (input voltage 0.7 V_{pp} ; F = 1 MHz).		40	55		dB
t_{dc}	Delay time between R, G, B inputs and RGB outputs.			10		nsec
t_{sr1}	Switching rise time between C input signal and R, G, B output signal (input signal on RGB1).			45		nsec
t_{sf1}	Switching fall time between C input signal and R, G, B output signal (input signal on RGB1).			25		nsec
t_{sr2}	Switching rise time between C input signal and R, G, B output signal (input signal on RGB2).			55		nsec
t_{sf2}	Switching fall time between C input signal and R, G, B output signal (input signal on RGB2).			25		nsec
Fast Blanking Switch (pin 13) (time measurement conditions : FB input pulse amplitude = 2 V ; C pulse amplitude = 3 V)						
V_{IL} V_{IH} V_{OL} V_{OH}	Low Level Input Voltage High Level Input Voltage Low Level Output Voltage High Level Output Voltage	 $T_{junction}$ = 25 °C $T_{junction}$ stabilized	– 0.5 1 1.4 1.5	 1.7 1.9	0.4 V_{CC} + 0.5 0.6 3.5	V V V V
	Dynamic Output Impedance : with R_{load} = 300 Ω			10		Ω
t_{FB1r}	Delay rise time between FB1 input and FB output.			60	110	nsec
t_{FB1f}	Delay fall time between FB1 input and FB output.			40	60	nsec
t_{FB2r}	Delay rise time between FB2 input and FB output.			60		nsec
t_{FB2f}	Delay fall time between FB2 input and FB output.			40		nsec
t_{SFB1r}	Switching rise time between C input and FB output (input signal on FB1 input).			75		nsec
t_{SFB1f}	Switching fall time between C input and FB output (input signal on FB1 input).			50		nsec
t_{SFB2r}	Switching rise time between C input and FB output (input signal on FB2 input).			85		nsec
t_{SFB2f}	Switching fall time between C input and FB output (input signal on FB2 input).			50		nsec

TAB-03

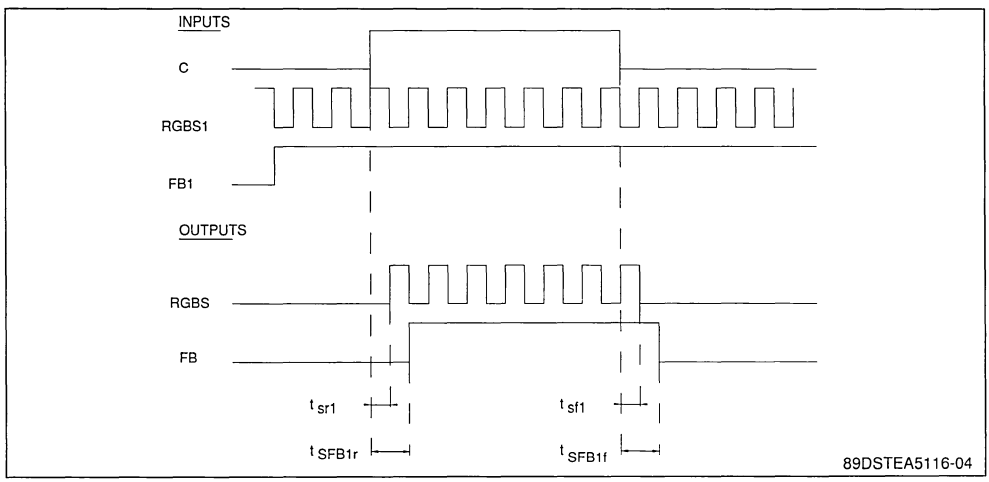
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Video (or synchro) **Signal Switch** (pin 15) - time measurement conditions : (C pulse amplitude = 3 V)					
V_S	DC Output Voltage (no input voltage) $T_{junction}$ = 25 °C $T_{junction}$ stabilized		0.9 1.2	1.25	V V
V_{as}	Max Output Swing Voltage	2.6			V_{pp}
Z_{ic}	DC Input Impedance		10		kΩ
Z_{oc}	Dynamic Output Impedance (input voltage 1 V_{pp} ; F = 1 MHz) with R_{load} = 300 Ω		10		Ω
A_v	Gain (input voltage 1 V_{pp} ; F = 1 MHz)	5.5	6	6.5	dB
B	Bandwidth (– 3 dB) (input voltage 1 V_{pp})	15	20		MHz
	Input Swing		1 V ± 3 dB		
t_{dc}	Delay Time Between S Input and S Output (Δ input : 0 7 V_{pp})		10		nsec
t_{sr1}	Switching rise time between C input signal and S output signal (input signal on S1)		45		nsec
t_{sf1}	Switching fall time between C input signal and S output signal (input signal on S1)		25		nsec
t_{sr2}	Switching rise time between C input signal and S output signal (input signal on S2)		55		nsec
t_{sf2}	Switching fall time between C input signal and S output signal (input signal on S2)		25		nsec
Select Input "C" (pin 3)					
V_{IL}	Low Level Input Voltage	– 0.5		1	V
V_{IH}	High Level Input Voltage	2		V_{CC} + 0.5	V
I_{IL}	Low Level Input Current (V_{IL} = 1 V)	– 0.6		– 0.1	mA
I_{IH}	High Level Input Current (V_{IH} = 3 V)			0.5	mA

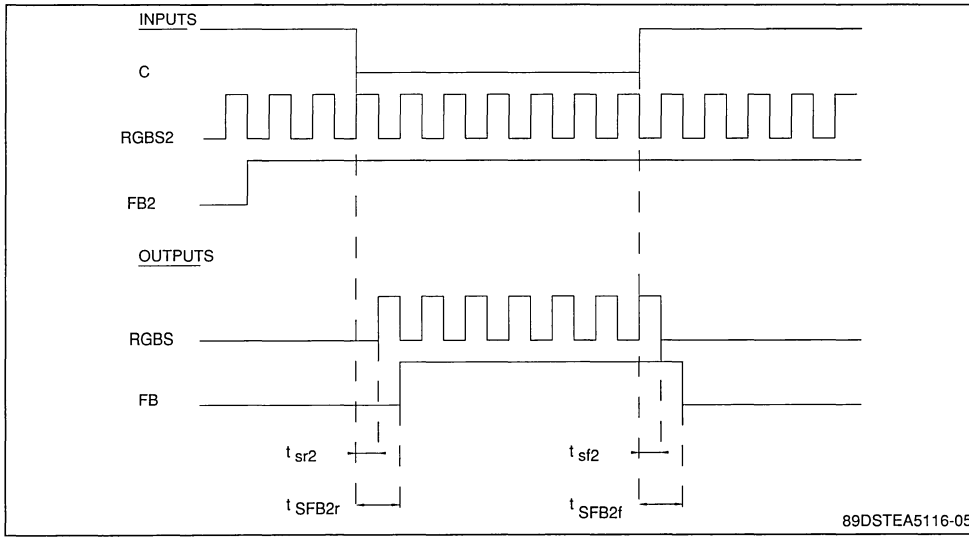
TAB-04


INPUTS
C
RGBS1
RGBS2
FB1
FB2
OUTPUTS
RGBS
FB
t_{dc}
t_{FB2r}
t_{FB2f}
t_{FB1r}
t_{FB1f}
89DSTEA5116-03

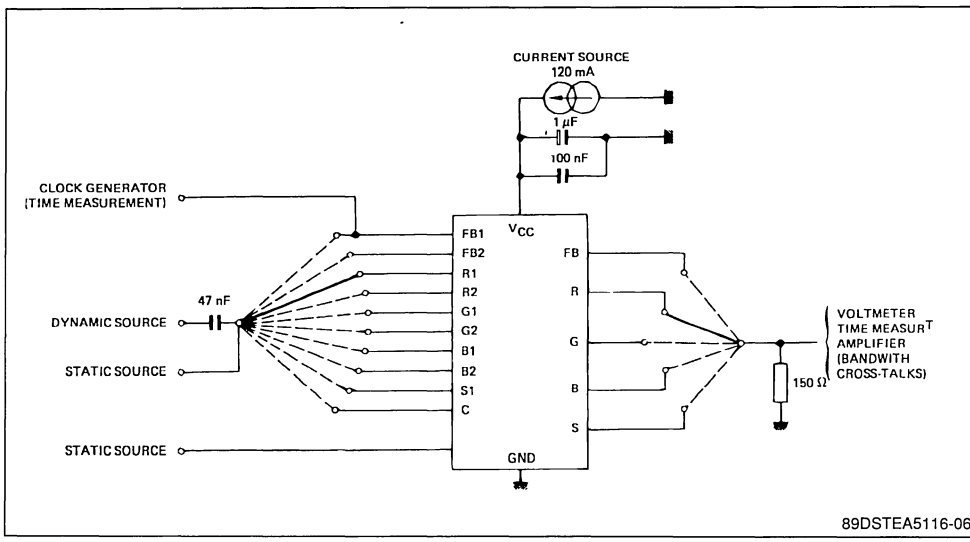
RGBS2 = 0, FB2 = 0


INPUTS
C
RGBS1
FB1
OUTPUTS
RGBS
FB
t_{sr1}
t_{SFB1r}
t_{sf1}
t_{SFB1f}
89DSTEA5116-04

RGBS1 = 0, FB1 = 0

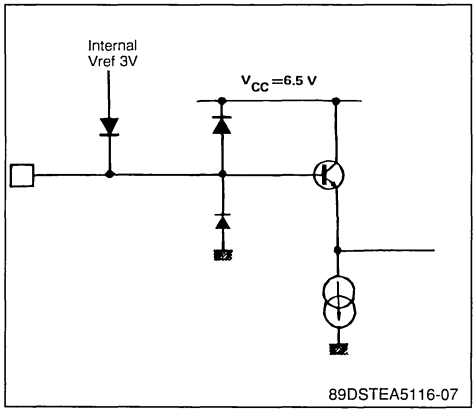


TEST CIRCUIT

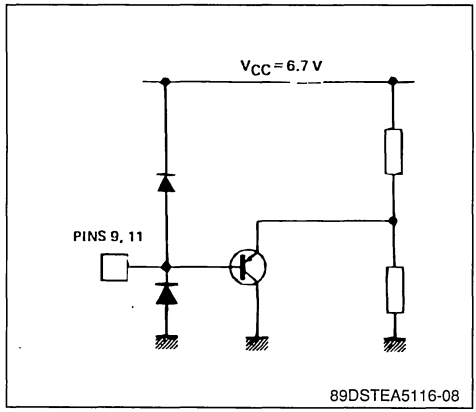


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

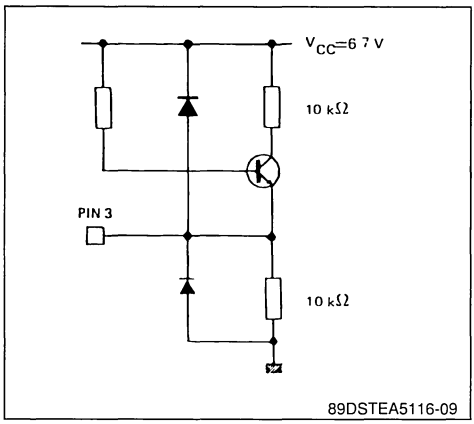
R, G, B, S INPUTS (pins 1, 2, 8, 10, 12, 16, 17, 18)



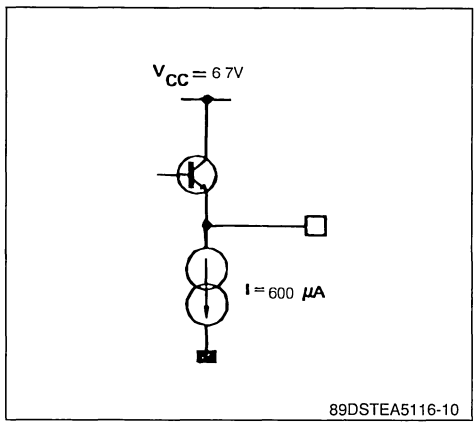
FB INPUTS (pins 9, 11)



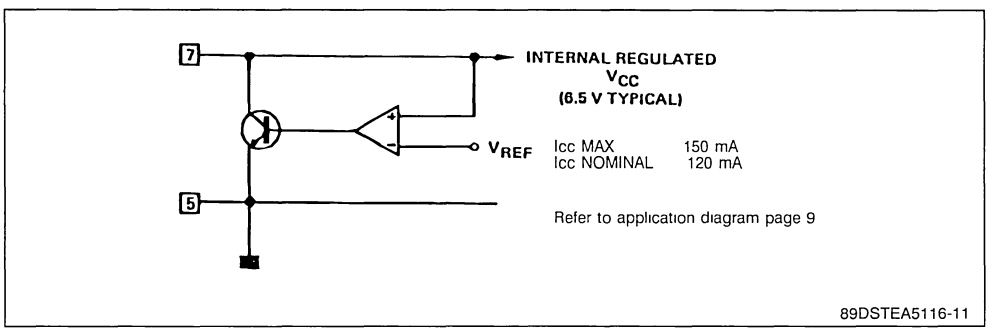
C INPUT (pin 3)



ALL OUTPUTS (pins 4, 6, 13, 14, 15)

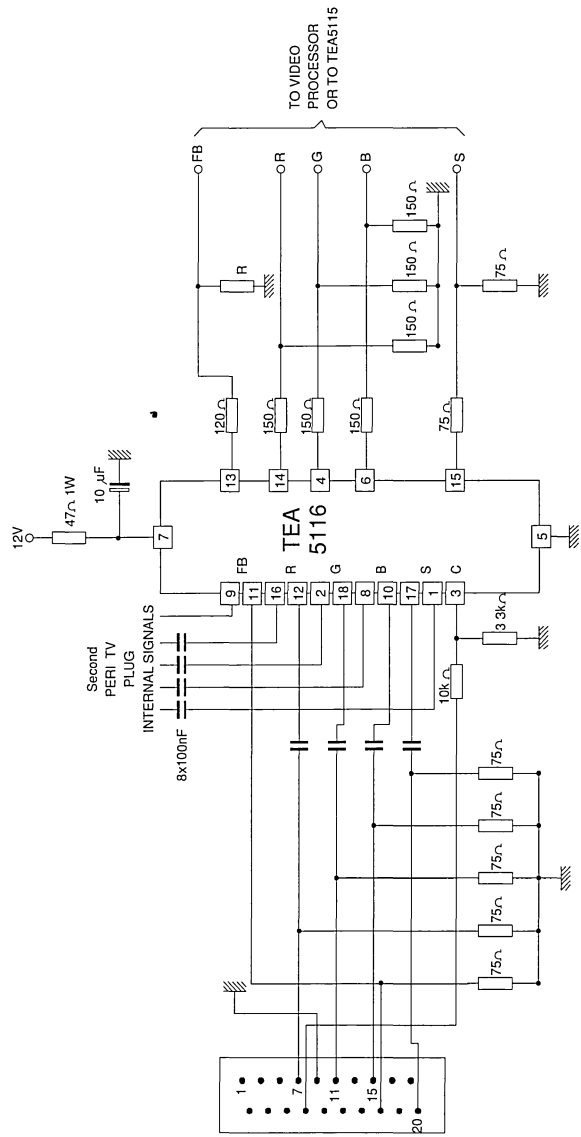


I_{CC} SUPPLY (shunt transistor regulation system) (pin 7)



TYPICAL APPLICATION DIAGRAM

- Under given output load values are minimum values, in case of all output loading.
- Minimum output load is 150 Ω individually, provided that total supply current is less than 150 mA.

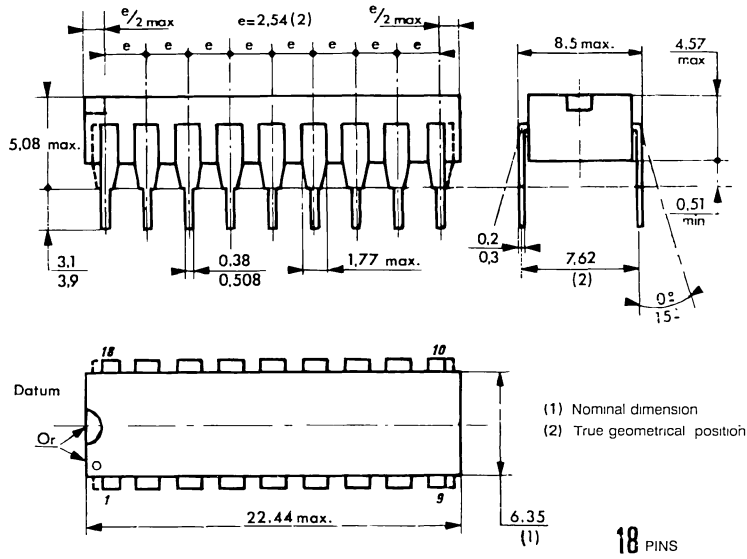


R values
1) towards TEA5115 : R = 300 Ω.
2) towards video processor : R = 200 Ω.

89DSTEA5116-12

PACKAGE MECHANICAL DATA

18 PINS – PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

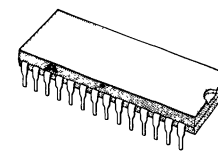
TEA5640E

MULTISTANDARD COLOR TV DECODER

- FULLY AUTOMATIC MULTISTANDARD SWITCHING : THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM USED FOR THE AUTOMATIC STANDARD RECOGNITION
- NO CRYSTALS REQUIRED : ALL THE FREQUENCIES ARE SYNTHESIZED FROM THE EXTERNAL REFERENCE FREQUENCY OF 62.5kHz, AND FROM SPECIFIED DATA STORED IN AN INTERNAL ROM
- AUTOMATIC BELL FILTER ADJUSTMENT
- ONLY ONE DELAY LINE COMPENSATION ADJUSTMENT
- AUTOMATIC INTERNAL PAL AND NTSC OSCILLATOR ADJUSTMENT
- AUTOMATIC ADJUSTMENT FOR FOB AND FOR IN SECAM
- POSITIVE R-Y AND B-Y OUTPUTS

DESCRIPTION

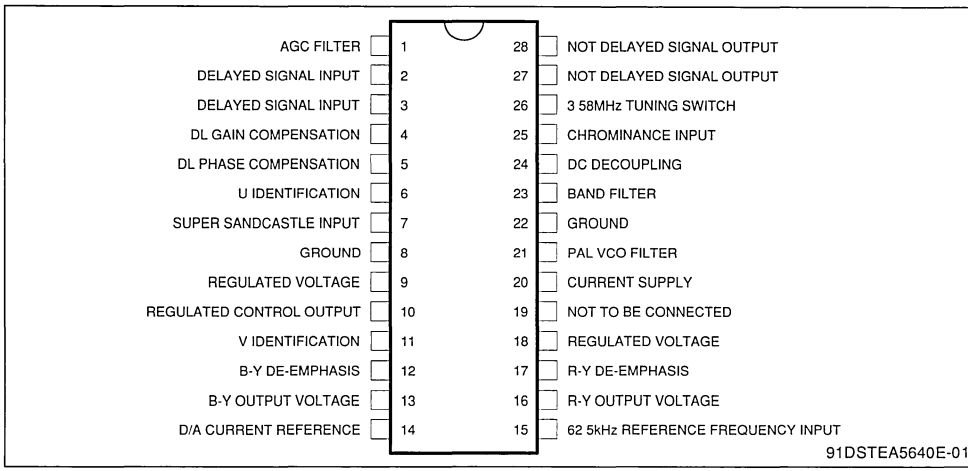
The TEA5640E is a multistandard TV decoder for PAL-SECAM NTSC1 (3.58MHz) and NTSC2 (4.43MHz). The circuit automatically selects the standard corresponding to the input signal. It produces all the reference frequencies required for decoding, which is achieved by a digital frequency synthesizer. Included on the chip are four numerical frequency locked loops that allow the elimination of PAL and NTSC crystals. The circuit uses an external reference frequency of 62.5kHz generally provided by the frequency synthesis tuner of the TV set.



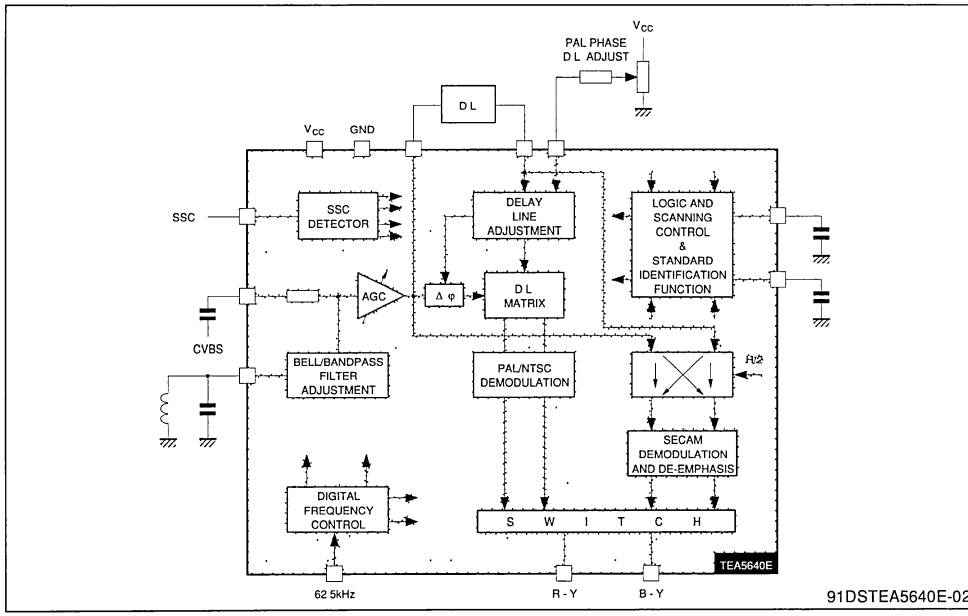
DIP28
(Plastic Package)

ORDER CODE : TEA5640E

PIN CONNECTIONS



BLOCK DIAGRAM (simplified)



FEATURES

- FULL AUTOMATIC MULTISTANDARD SWITCHING :
  THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM THAT PROVIDES ALL THE SWITCHINGS REQUIRED FOR THE AUTOMATIC STANDARD RECOGNITION. THIS SYSTEM IS SYNCHRONIZED BY THE FRAME PULSE.
- NO CRYSTAL REQUIREMENT :
  THE PAL AND NTSC FREQUENCIES ARE SYNTHESIZED ORIGINALLY BY THE EXTERNAL REFERENCE FREQUENCY OF 62.5 kHz AND DATA STORED IN THE ROM.
- AUTOMATIC ADJUSTMENT OF THE BELL FILTER : BY SWITCHING AN INTERNAL CAPACITOR NETWORK INCLUDED IN A DIGITAL LOOP.
- AUTOMATIC GAIN ADJUSTMENT OF THE DELAY LINE COMPENSATIONS :
  THIS ADJUSTMENT IS MADE ON THE BURST AND IS REFRESTED EVERY LINE RETRACE
- AUTOMATIC ADJUSTMENT FOR PAL AND NTSC OSCILLATOR :
  THIS OSCILLATOR HAS A DIGITAL AND AN ANALOGIC LOOP. THE PAL AND NTSC FREQUENCIES ARE MEMORIZED IN A ROM CONNECTED TO THE DIGITAL LOOP. THE DIGITAL LOOP GIVES THE RIGHT FREQUENCY AND THE ANALOGIC ONE HOLDS THE PHASE.
- AUTOMATIC ADJUSTMENT OF FoR AND FoB IN SECAM : THESE FREQUENCIES ARE PROGRAMMED IN THE ROM AND ARE SENT TO TWO OTHER DIGITAL LOOPS WHEN SECAM STANDARD IS SELECTED.
- AUTOMATIC DIFFERENCE PHASE ERROR COMPENSATION IN PAL MODE.
  THE PAL VCO IS LOCKED ON THE BURST AND DURING THE LINE, ON THE BLUE PICTURE CONTENT (0° axis color vector).

STANDARD SWITCHING AND INHIBITION

NTSC inhibition
NTSC 1 and 2 standards can be inhibited by connecting pin 6 to the ground.

3.58 MHz filter switching :
Pin 26 can be used to switch external filters when NTSC 1 is selected (For example luma filter).

SECAM recognition :

- When SECAM on, pin 12 and pin 17 DC voltages are lower than 5 V.
- For other standards, pin 12 and pin 17 DC voltages are regulated V_{CC} (typical 8 V).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V	Supply Voltage	Pins 9 - 18	9.5	V
I	Current	Pin 20	200	mA
T_{oper}	Operating Temperature Range		0 to 70	°C
T_{stg}	Storage Temperature		– 40 to 150	°C

TAB-01

THERMAL DATA

$R_{th\ (j-a)}$	Junction Ambient Thermal Resistance (with mini 10 % Cu on board)	55	°C/W

TAB-02

ELECTRICAL CHARACTERISTICS

Tamb = 25 °C ; V_{CC} = 12 V ; With Normalized Color Bar Pattern Input Signal (75 %) Subcarrier Level : 320 mV_{PP}

Refer to Application Diagram Page (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Supplies					
Vreg	Regulated Voltage I10 = 4 mA	Pins 9 - 18	7.5	8	8.5	V
ICC	Supply Current	Pin 9 + Pin 18		90	120	mA
I9	Supply Current	Pin 9			90	mA
I18	Supply Current	Pin 18			27	mA
VI2L	DC Voltage at I20 = 15 mA	Pin 20		0.8		V
I10	Input Current	Pin 10	2		20	mA
	Transfer Characteristic (I10 = 4.0 mA)			250		mA/V
	Current Reference	Pin 14				
V14	DC Voltage (I14 = 0.77 mA)		1.2	1.4	1.6	V
	Internal Bias	Pin 24				
V24	DC Voltage		3.7	4.2	4.7	V
	Impedance (I_{out} = 2 mA)			90	110	Ω
	Reference Clock Input					
	F = 62.5 kHz ± 6Hz	Pin 15				
I15L	Low Level Input Current (V15 = 2.1 V)		– 20	– 10	– 5	µA
I15H	High Level Input Current (V15 = 3.2 V)			5	10	µA
V15L	Low Level Input Voltage	R Source = 68 kΩ			1	V
V15H	High Level Input Voltage	R Source = 68 kΩ	4			V
	Voltage Threshold			2.8		V
	Super Sandcastle Detector	Pin 7				
VB	Blanking Threshold		0.5	0.75	0.9	V
VL	Line Threshold		1.6	1.8	1.9	V
V6	Burst Gate Threshold		3.2	3.5	3.8	V
	Minimum Frame Blanking Duration		1.15			mS
I7	Input Current (V7 = 1.75 V)		– 20		0	µA
	Max Input Voltage Pin 7				6 0	V
	Chrominance Input	Pin 25				
V25	DC Voltage			5.5		V
	Maximum AC Input Voltage				0.64	Vpp
	Impedance		0.8	1		kΩ
	Automatic Gain Control					
	SECAM MODE					
	• 0 dB Reference Voltage for Measurement on Pins 27 - 28 (chroma input voltage V25 = 320 mVpp)		50	150	250	mVpp
	• AC Voltage Variation on Pins 27 - 28 (V25 = + 6 dB)		– 3		+ 3	dB
	• AC Voltage Variation on Pins 27 -28 (V25 = – 24 dB)		– 5		+ 2	dB
	PAL/NTSC MODE WITH IDENTIFICATION					
	• 0 dB Reference Voltage for Measurement on Pins 13 -16 (chroma input voltage V25 = 320 mVpp)					
	• AC Voltage Variation on Pins 13 - 16 (V25 = + 6 dB)		– 3		+ 3	dB
	• AC Voltage Variation on Pins 13 - 16 (V25 = – 24 dB)		– 5		+ 2	dB

TAB-03

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Demodulator Part					
	GENERALITIES					
V13	B-Y Output DC Voltage	Pin 13	3	3.5	4	V
V16	R-Y Output DC Voltage	Pin 16	3.2	3.7	4.2	V
	Maximum Sink Current	Pin 13	0.4			mA
	Maximum Sink Current	Pin 16	0.4			mA
	Differential Delay Time Between PAL/SECAM				50	nS
	Delay Diff Tolerance				50	nS
	Delay Between Chroma Output and Luma Signal			450		nS
	B-Y Output AC Impedance (± 50 µA)			250		Ω
	R-Y Output AC Impedance (± 50 µA)			250		Ω
	Blanking Level Offset (% of the pp output signal)				± 2	%
	SECAM Mode					
VBYS	B-Y AC Voltage		1.0	1.34	1.6	Vpp
VRYS	R-Y AC Voltage		0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			30		mVpp
	Max overshoot on output SECAM signals (see test conditions Note 2)				5	%
	SECAM Rise Time (see test conditions Note 1)				800	ns
	PAL Mode					
VBYP	B-Y AC Voltage		1.0	1 34	1.6	Vpp
VRYP	R-Y AC Voltage		0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			30		mVpp
	PAL/SECAM Output Balance					
RYPS	R-Y Output				± 2	dB
BYPS	B-Y Output				± 2	dB
	NTSC 4.43					
VBYN2	B-Y AC Voltage		1.0	1.34	1.6	Vpp
VBYN2	R-Y AC Voltage		0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			50		mVpp
	NTSC 3.58					
VBYN1	B-Y AC Voltage		1.0		1.6	Vpp
VRYN1	R-Y AC Voltage		0 8		1.3	Vpp
	B-Y/R-Y Ratio		1 1		1.45	
	Residual Subcarrier			50		mVpp
	De-Emphasis	Pins 12 - 17				
	SECAM MODE					
	DC Voltage (blanking level)			3.5	4.0	V
	Impedance			11		kΩ
	PAL NTSC MODE					
	DC Voltage			VREG		V
	Impedance			70		kΩ
	Reference Oscillator PLL					
	Catching Range in PAL Mode		± 350			Hz
	Holding Range		± 500			Hz

TAB-04

Notes :

1. **Rise Time Test Conditions**
   - SECAM Color Bar Patterns 75%
   - Generator TEKTRONIX 143
   - Standard Application without any output load
   - Measure between 10% and 90% on the major transition (Green Violet)

2. **Overshoot Test Conditions**
   - Idem than for Rise Time
   - Ratio between the value of the overshoot and the peak-to-peak value of the transition after overshoot (on the flat level)

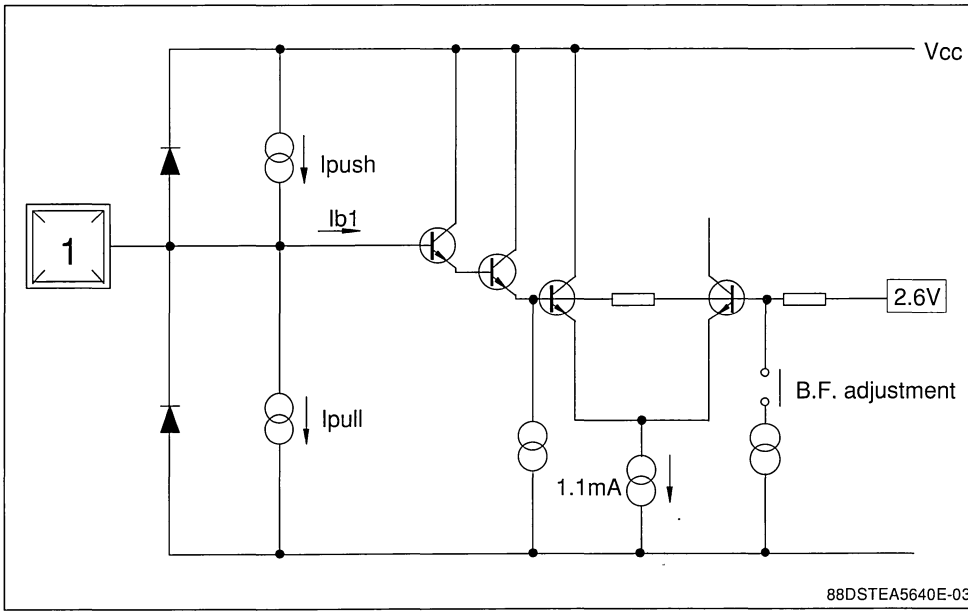
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Band Filter	Pin 23				
	Impedance SECAM Mode		3.7	4.7	5.7	kΩ
	PAL/NTSC Mode		0.85	1.1	1.35	kΩ
	Minimum Switchable Internal Capacitance (all standards)			20		pF
	Maximum Switchable Internal Capacitance (all standards)			50		pF
ΔF	Internal Oscillator Frequency Range for (L = 10 μH, C = 68 pF)		590			kHz
	Frequency Offset, After Automatic Adjustement				± 10	kHz
	3.58 MHz Switch Output	Pin 26				
	NTSC1 (3.58 MHz)					
V26N1	DC Voltage (I26 = 0 mA)		1			V
	Impedance			2		kΩ
	NTSC2 (4.43 MHz) or PAL or SECAM					
V26N2	DC Voltage				0.3	V
	Max Sink Current		0.35			mA
	Undelayed Signal Outputs	Pins 27 - 28				
V27 V28	DC Voltage			1.6		V
I27 I28	Sink Current		1			mA
	Impedance			30		Ω
	Identification					
	Burst Attenuation Range / Nominal Level					
	SECAM Mode (line identification)		30			dB
	PAL Mode		30			dB
	NTSC Modes		20			dB
V26	NTSC 3.58 Mode with $R_{pin(26)}$=100kΩ/GND		0		300	mV
V26	PAL Mode with $R_{pin(26)}$=100kΩ/GND		4		5	V
V26	SECAM Mode with $R_{pin(26)}$=100kΩ/GND		6.2		7.2	V
	TINT Control (NTSC Modes)					
	Range of Phase Change For V Pin 5 Changing from 2 to 4.5 V			± 40		degree
V5	DC Voltage for 0 Degree TINT Change	Pin 5		3.5		V
I5	Input Current	Pin 5	0.08		0.2	mA
	NTSC Detection					
	Detection Threshold	Pin 6	3	3.5	4	V
	NTSC Mode Inhibition Threshold		0.5		2.5	V
	Leakage Current				0.5	μA
	Delayed Signal Input	Pins 2 - 3				
	DC Voltage in PAL Mode			2.4		V
	Input Impedance		0.88	1.1	1.32	kΩ
	Delay Line Attenuation Compensation					
	Range of Automatic Attenuation Compensation		– 3	– 9	– 15	dB
	Delay Line Phase Shift Compensation					
	Range of Phase Shift Compensation with a 100kΩ Potentiometer (see application diagram p 13)		± 30			degree
	Alternation Line Detection PAL or SECAM	Pin 11				
VTHH	High Differential Threshold (VTHH = V11H – V24)		200		350	mV
VTHL	Low Differential Threshold (VTHL = V11L – V24)		– 350		– 200	mV
	Leakage Current Threshold (V11 = V24 + 1V)				0.5	μA

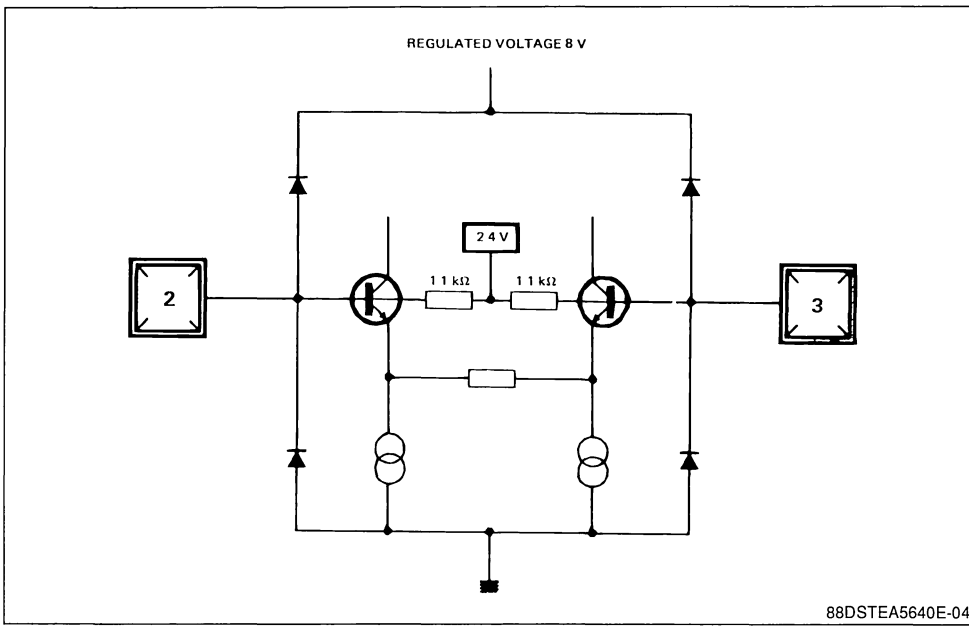
TAB-05

INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

PIN 1

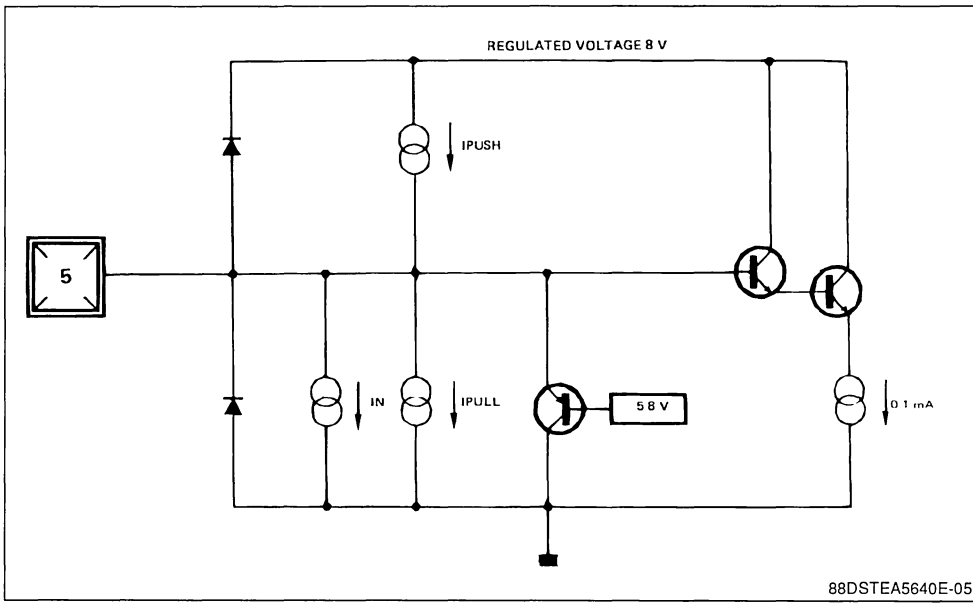


PINS 2 – 3

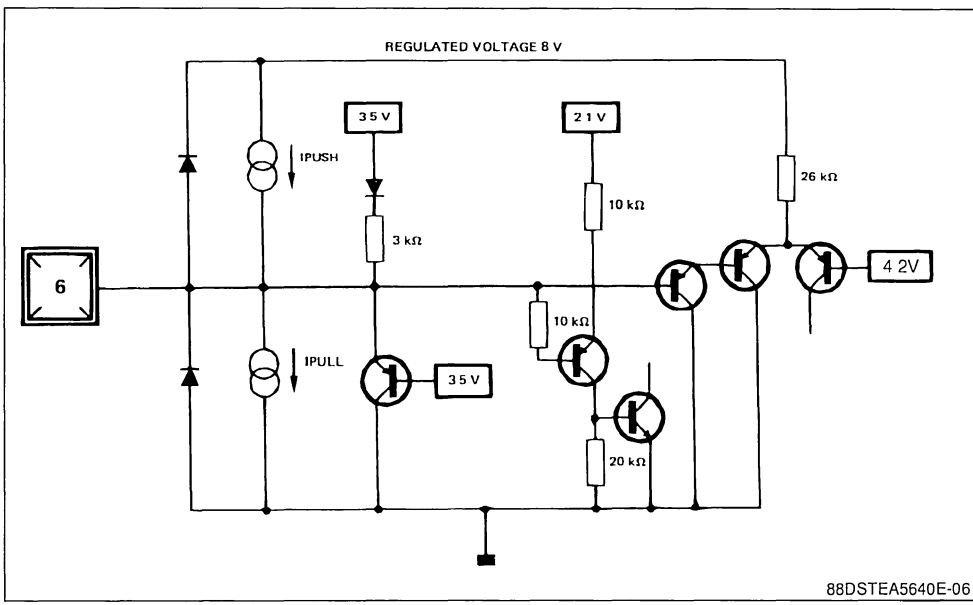


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

PIN 5

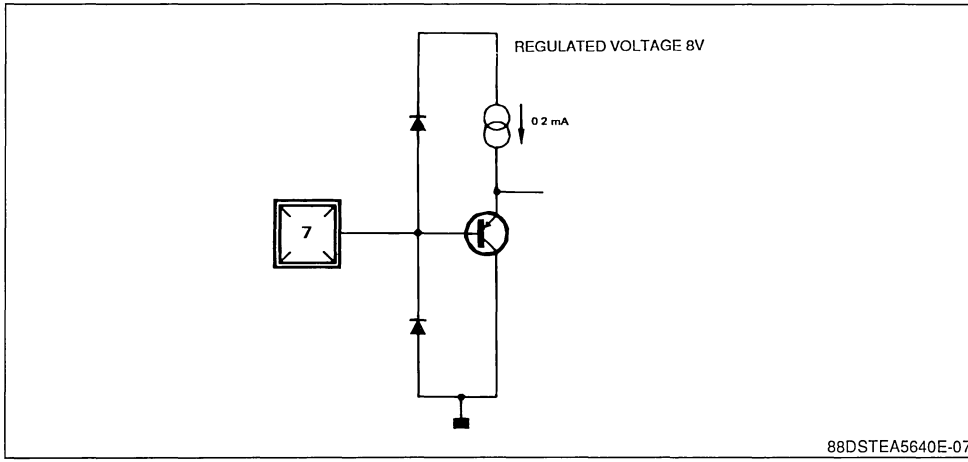


PIN 6

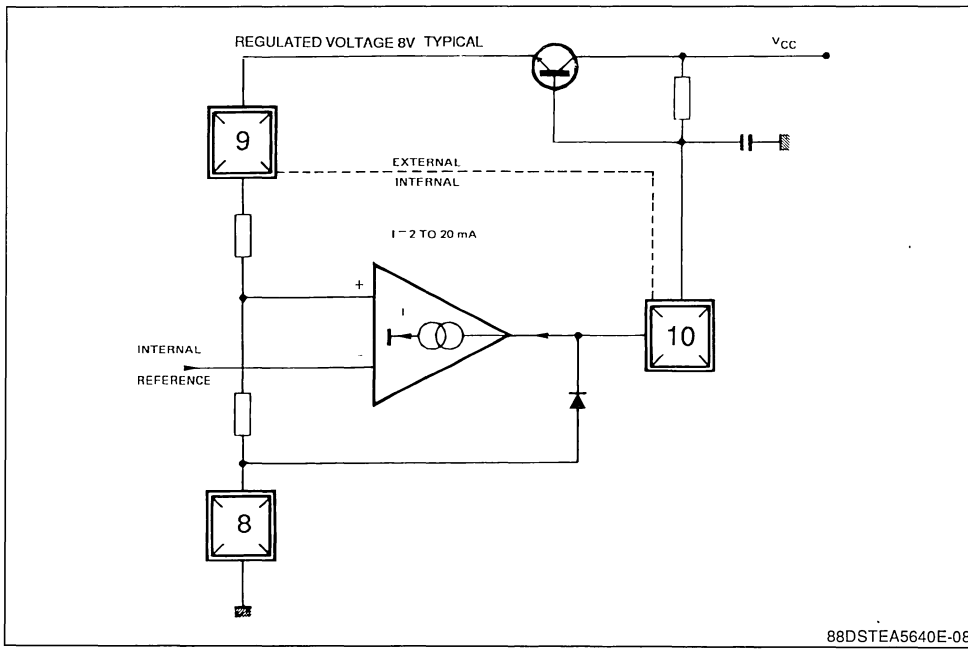


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

PIN 7

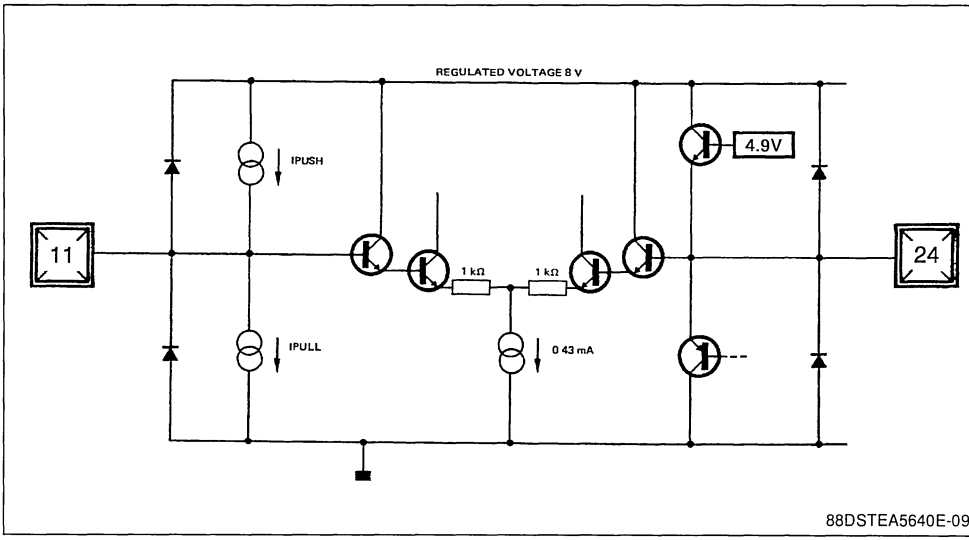


PINS 8 – 9 – 10

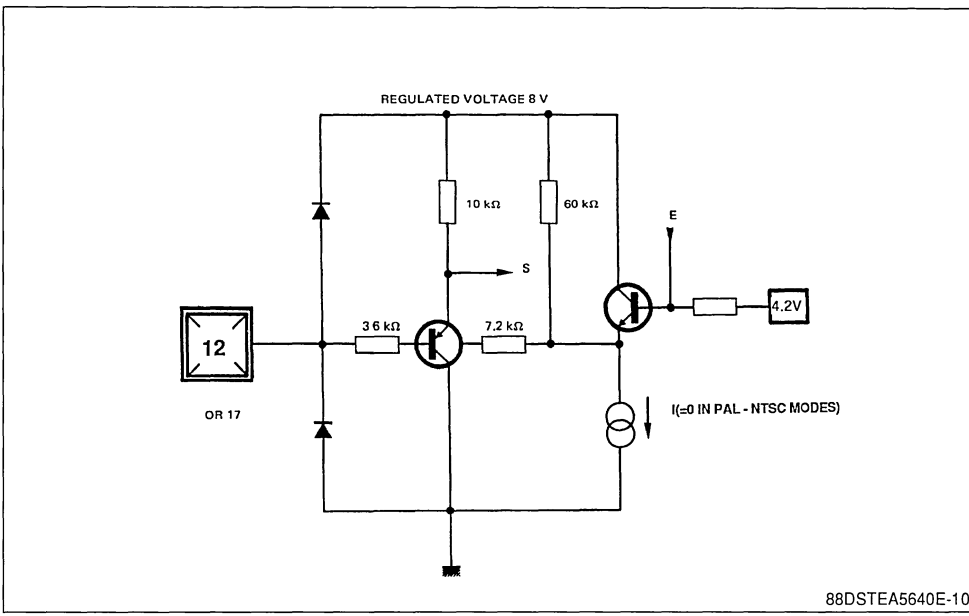


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

PINS 11 – 24

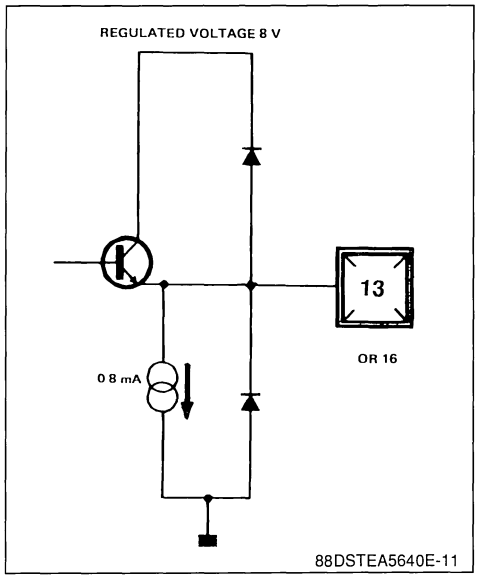


PINS 12 – 17

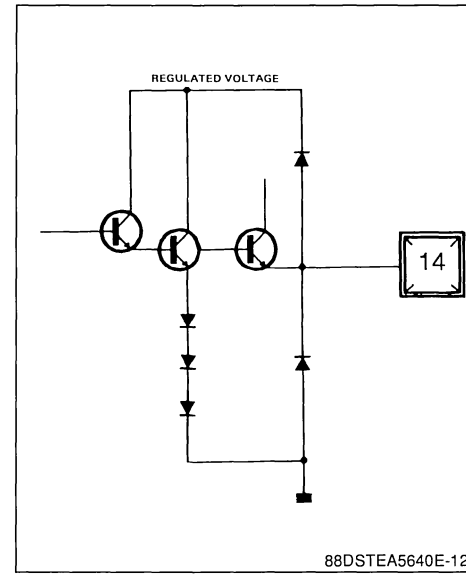


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

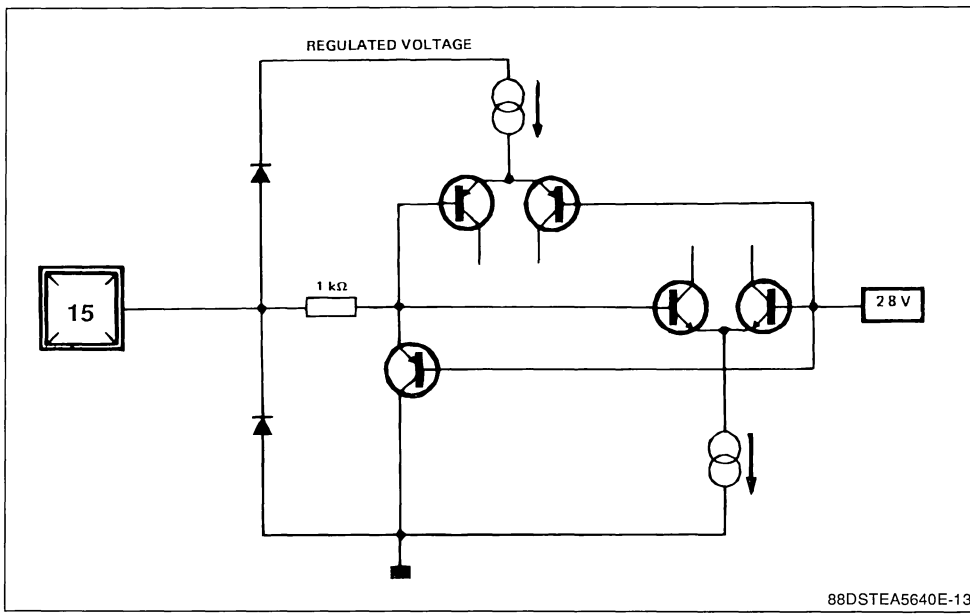
PINS 13 – 16



PIN 14

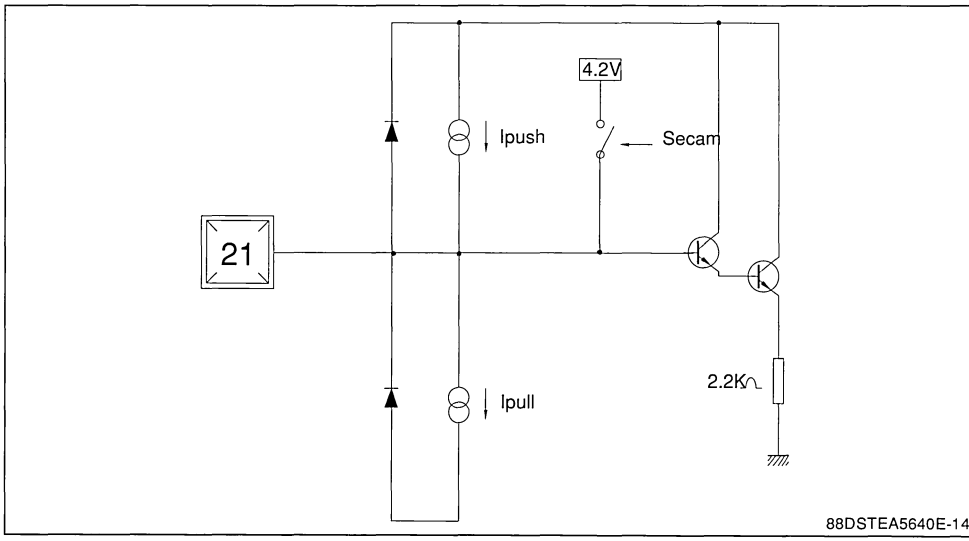


PIN 15

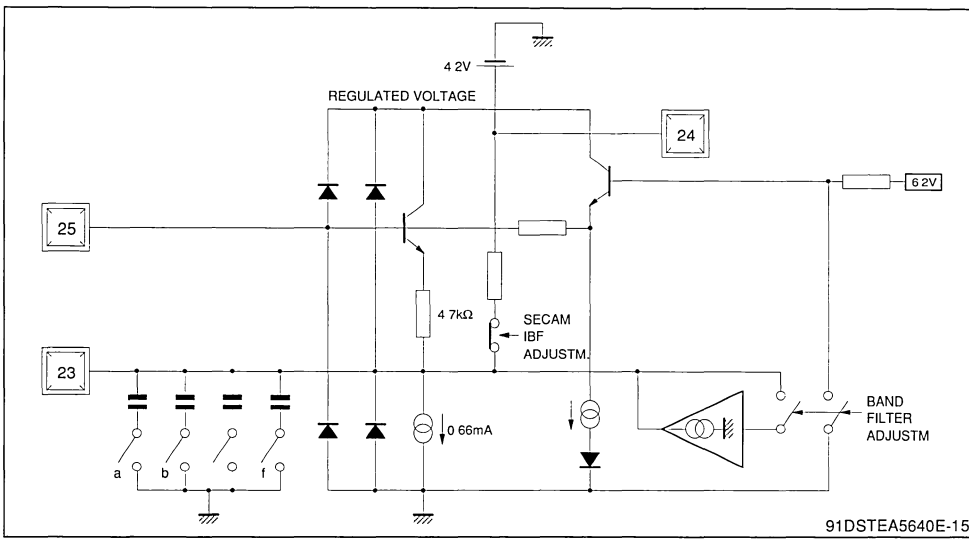


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

PIN 21

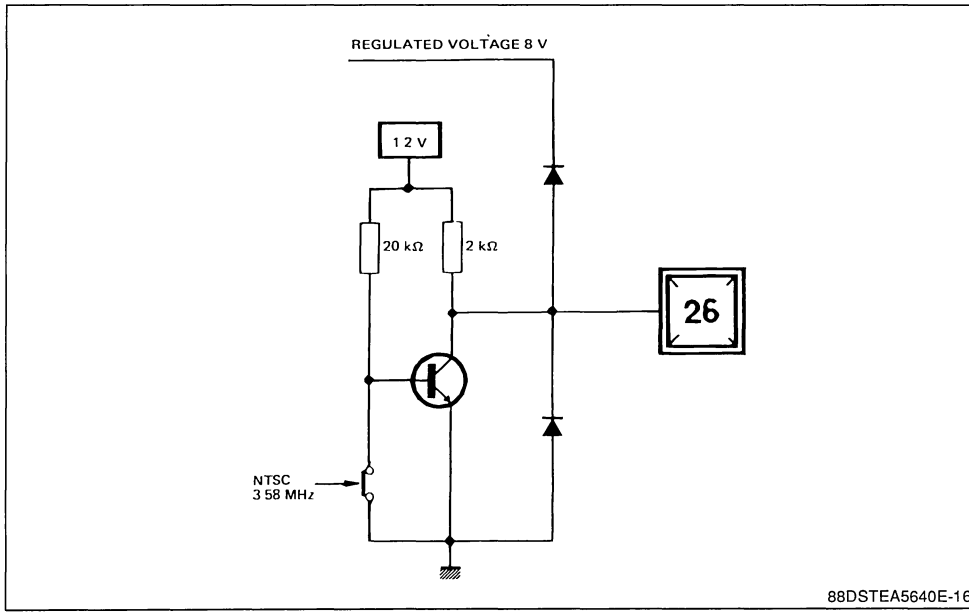


PINS 23 – 24 – 25

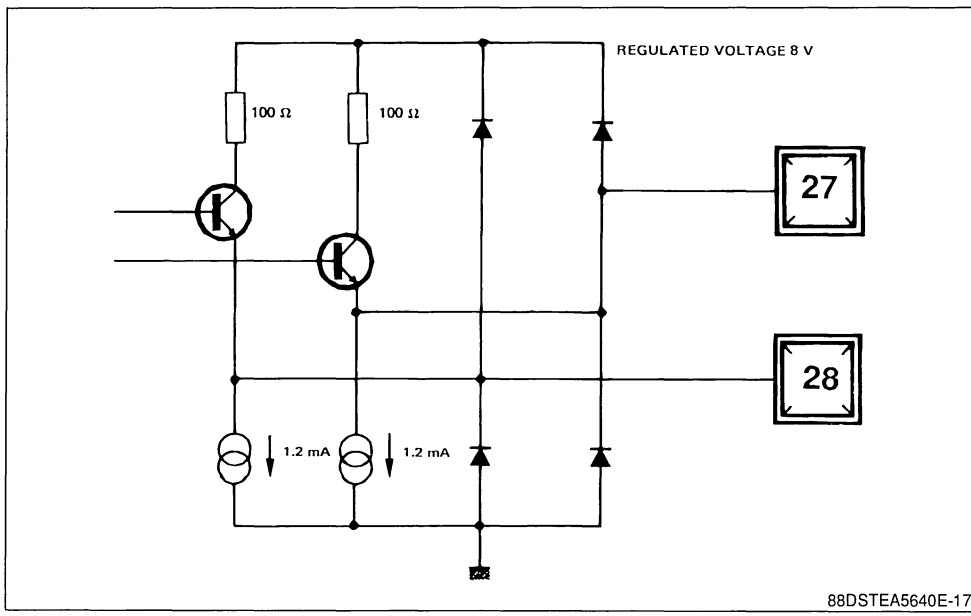


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

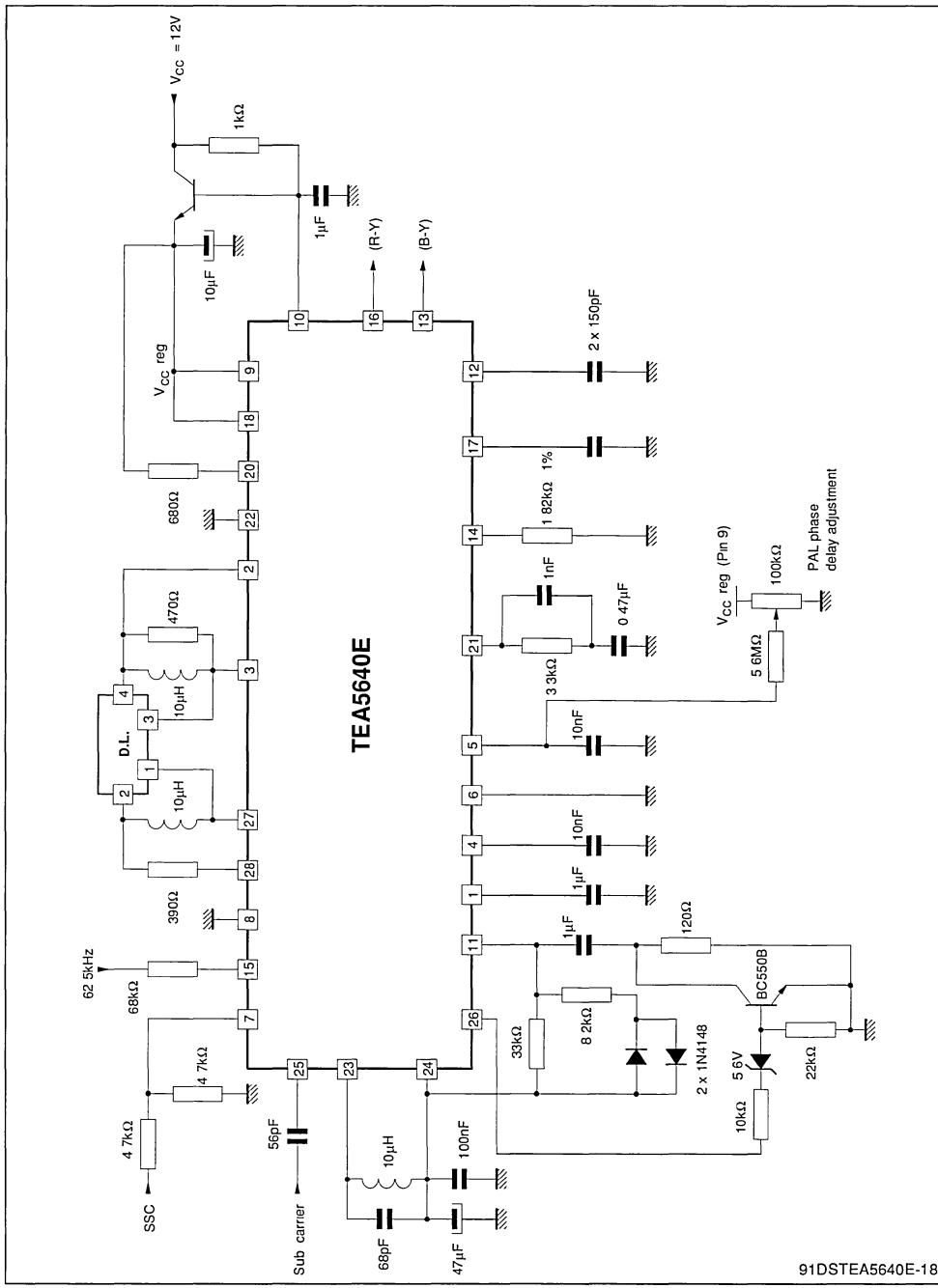
PIN 26



PINS 27 - 28

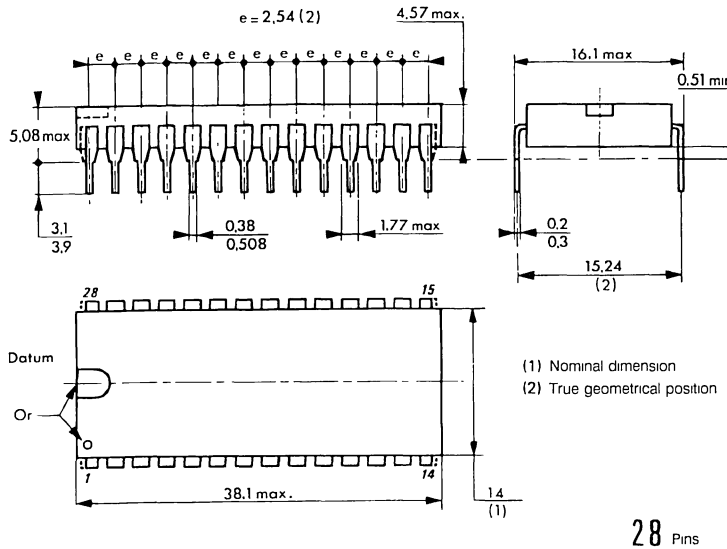


TYPICAL APPLICATION for PAL/SECAM



PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP

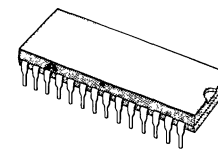


PAL/SECAM COLOR TV DECODER

- FULLY AUTOMATIC MULTISTANDARD SWITCHING : THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM USED FOR THE AUTOMATIC STANDARD RECOGNITION
- NO CRYSTALS REQUIRED : ALL THE FREQUENCIES ARE SYNTHESIZED FROM THE EXTERNAL REFERENCE FREQUENCY OF 62.5kHz, AND FROM SPECIFIED DATA STORED IN AN INTERNAL ROM
- AUTOMATIC BELL FILTER ADJUSTMENT
- ONLY ONE DELAY LINE COMPENSATION ADJUSTMENT
- AUTOMATIC INTERNAL PAL OSCILLATOR ADJUSTMENT
- AUTOMATIC ADJUSTMENT FOR FOB AND FOR IN SECAM
- POSITIVE R-Y AND B-Y OUTPUTS

DESCRIPTION

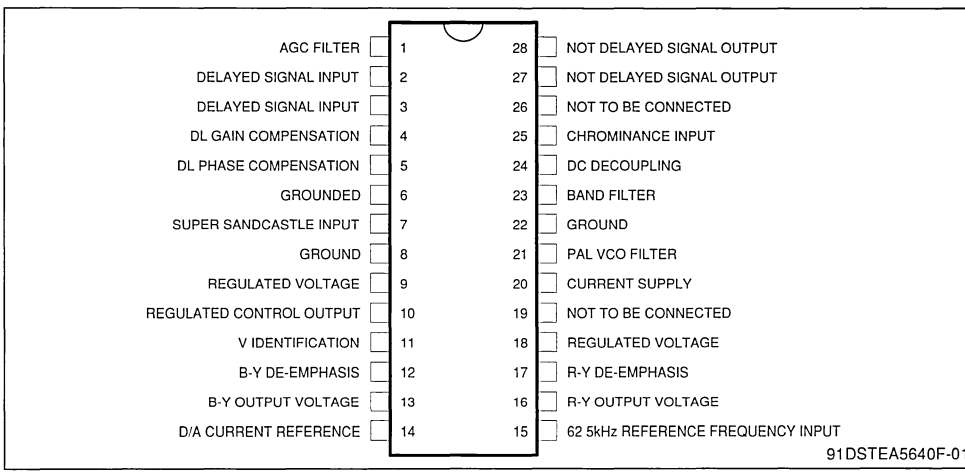
The TEA5640F is a multistandard TV decoder for PAL-SECAM. The circuit automatically selects the standard corresponding to the input signal. It produces all the reference frequencies required for decoding, which is achieved by a digital frequency synthesizer. Included on the chip are four numerical frequency locked loops that allow the elimination of PAL crystal. The circuit uses an external reference frequency of 62.5kHz generally provided by the frequency synthesis tuner of the TV set.



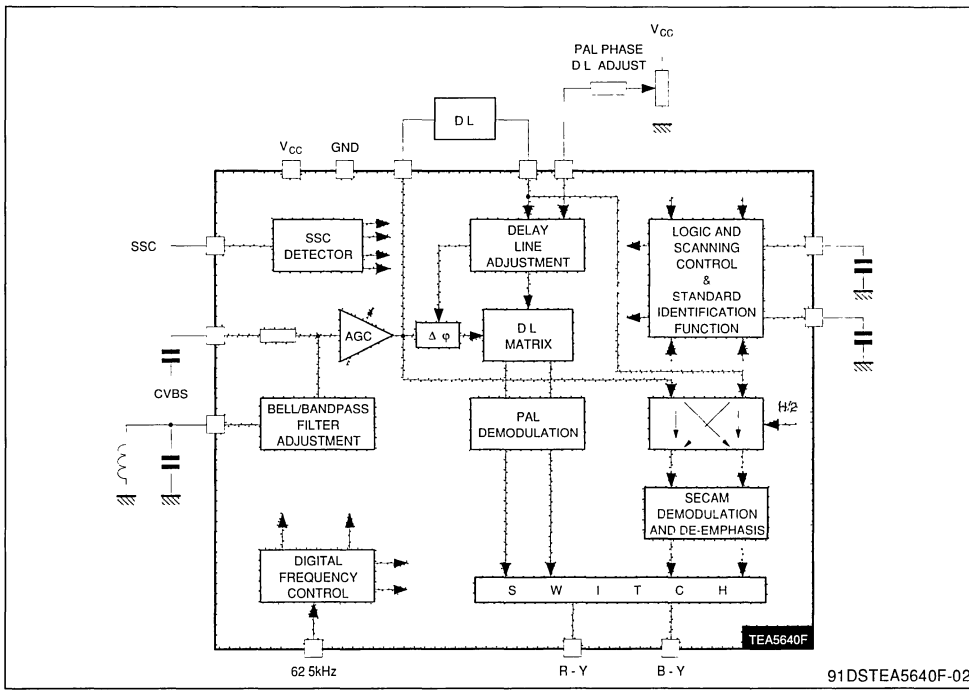
DIP28
(Plastic Package)

ORDER CODE : TEA5640F

PIN CONNECTIONS



BLOCK DIAGRAM (simplified)



FEATURES

- FULL AUTOMATIC MULTISTANDARD SWITCHING :
  THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM THAT PROVIDES ALL THE SWITCHINGS REQUIRED FOR THE AUTOMATIC STANDARD RECOGNITION. THIS SYSTEM IS SYNCHRONIZED BY THE FRAME PULSE.
- NO CRYSTAL REQUIREMENT :
  THE PAL FREQUENCIES ARE SYNTHESIZED ORIGINALLY BY THE EXTERNAL REFERENCE FREQUENCY OF 62.5 kHz AND DATA STORED IN THE ROM.
- AUTOMATIC GAIN ADJUSTMENT OF THE BELL FILTER : BY SWITCHING AN INTERNAL CAPACITOR NETWORK INCLUDED IN A DIGITAL LOOP.
- AUTOMATIC GAIN ADJUSTMENT OF THE DELAY LINE COMPENSATIONS :
  THIS ADJUSTMENT IS MADE ON THE BURST AND IS REFRESTED EVERY LINE RETRACE
- AUTOMATIC ADJUSTMENT FOR PAL OSCILLATOR :
  THIS OSCILLATOR HAS A DIGITAL AND AN ANALOGIC LOOP. THE PAL FREQUENCIES ARE MEMORIZED IN A ROM CONNECTED TO THE DIGITAL LOOP. THE DIGITAL LOOP GIVES THE RIGHT FREQUENCY AND THE ANALOGIC ONE HOLDS THE PHASE.
- AUTOMATIC ADJUSTMENT OF FoR AND FoB IN SECAM : THESE FREQUENCIES ARE PROGRAMMED IN THE ROM AND ARE SENT TO TWO OTHER DIGITAL LOOPS WHEN SECAM STANDARD IS SELECTED.
- AUTOMATIC DIFFERENCE PHASE ERROR COMPENSATION IN PAL MODE.
  THE PAL VCO IS LOCKED ON THE BURST AND DURING THE LINE, ON THE BLUE PICTURE CONTENT (0° axis color vector).

STANDARD SWITCHING AND INHIBITION

SECAM recognition :

- When SECAM on, pin 12 and pin 17 DC voltages are lower than 5 V.
- For PAL standard, pin 12 and pin 17 DC voltages are regulated V_{CC} (typical 8 V).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V	Supply Voltage	Pins 9 - 18	9.5	V
I	Current	Pin 20	200	mA
T_{oper}	Operating Temperature Range		0 to 70	°C
T_{stg}	Storage Temperature		– 40 to 150	°C

TAB-01

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction Ambient Thermal Resistance (with mini 10 % Cu on board)	55	°C/W

TAB-02

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C ; V_{CC} = 12 V ; With Normalized Color Bar Pattern Input Signal (75 %) Subcarrier Level : 320 mV_{PP}

Refer to Application Diagram Page (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Supplies					
Vreg	Regulated Voltage I10 = 4 mA	Pins 9 - 18	7.5	8	8.5	V
ICC	Supply Current	Pin 9 + Pin 18		90	120	mA
I9	Supply Current	Pin 9			90	mA
I18	Supply Current	Pin 18			27	mA
VI2L	DC Voltage at I20 = 15 mA	Pin 20		0.8		V
I10	Input Current	Pin 10	2		20	mA
	Transfer Characteristic (I10 = 4.0 mA)			250		mA/V
	Current Reference	Pin 14				
V14	DC Voltage (I14 = 0.77 mA)		1.2	1.4	1.6	V
	Internal Bias	Pin 24				
V 24	DC Voltage		3.7	4.2	4.7	V
	Impedance (I_{out} = 2 mA)			90	110	Ω
	Reference Clock Input					
	F = 62.5 kHz ± 6Hz	Pin 15				
I15L	Low Level Input Current (V15 = 2.1 V)		– 20	– 10	– 5	µA
I15H	High Level Input Current (V15 = 3.2 V)			5	10	µA
V15L	Low Level Input Voltage	R Source = 68 kΩ			1	V
V15H	High Level Input Voltage	R Source = 68 kΩ	4			V
	Voltage Threshold			2.8		V
	Super Sandcastle Detector	Pin 7				
VB	Blanking Threshold		0.5	0.75	0.9	V
VL	Line Threshold		1.6	1.8	1.9	V
V6	Burst Gate Threshold		3.2	3.5	3.8	V
	Minimum Frame Blanking Duration		1.15			mS
I7	Input Current (V7 = 1.75 V)		– 20		0	µA
	Max Input Voltage Pin 7				6.0	V
	Chrominance Input	Pin 25				
V25	DC Voltage			5.5		V
	Maximum AC Input Voltage				0.64	Vpp
	Impedance		0.8	1		kΩ
	Automatic Gain Control					
	SECAM MODE					
	• 0 dB Reference Voltage for measurement on Pins 27 - 28 (chroma input voltage V25 = 320 mVpp)		50	150	250	mVpp
	• AC Voltage Variation on Pins 27 - 28 (V25 = + 6 dB)		– 3		+ 3	dB
	• AC Voltage Variation on Pins 27 -28 (V25 = – 24 dB)		– 5		+ 2	dB
	PAL/NTSC MODE WITH IDENTIFICATION					
	• 0 dB Reference Voltage for measurement on Pins 13 -16 (chroma input voltage V25 = 320 mVpp)					
	• AC Voltage Variation on Pins 13 - 16 (V25 = + 6 dB)		– 3		+ 3	dB
	• AC Voltage Variation on Pins 13 - 16 (V25 = – 24 dB)		– 5		+ 2	dB

TAB-03

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Demodulator Part					
	GENERALITIES					
V13	B-Y Output DC Voltage	Pin 13	3	3.5	4	V
V16	R-Y Output DC Voltage	Pin 16	3.2	3.7	4.2	V
	Maximum Sink Current	Pin 13	0.4			mA
	Maximum Sink Current	Pin 16	0.4			mA
	Differential Delay Time Between PAL/SECAM				50	nS
	Delay Diff Tolerance				50	nS
	Delay Between Chroma Output and Luma Signal			450		nS
	B-Y Output AC Impedance (± 50 µA)			250		Ω
	R-Y Output AC Impedance (± 50 µA)			250		Ω
	Blanking Level Offset (% of the pp output signal)				± 2	%
	SECAM Mode					
VBYS	B-Y AC Voltage		1.0	1.34	1.6	Vpp
VRYS	R-Y AC Voltage		0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			30		mVpp
	Max overshoot on output SECAM signals (see test conditions Note 2)				5	%
	SECAM Rise Time (see test conditions Note 1)				800	ns
	PAL Mode					
VBYP	B-Y AC Voltage		1.0	1.34	1.6	Vpp
VRYP	R-Y AC Voltage		0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			30		mVpp
	PAL/SECAM Output Balance					
RYPS	R-Y Output				± 2	dB
BYPS	B-Y Output				± 2	dB
	De-Emphasis	Pins 12 - 17				
	SECAM MODE					
	DC Voltage (blanking level)			3.5	4.0	V
	Impedance			11		kΩ
	PAL MODE					
	DC Voltage			VREG		V
	Impedance			70		kΩ
	Reference Oscillator PLL					
	Catching Range in PAL Mode		± 350			Hz
	Holding Range		± 500			Hz
	Band Filter	Pin 23				
	Impedance SECAM Mode		3.7	4.7	5.7	kΩ
	PAL Mode		0.85	1.1	1.35	kΩ
	Minimum Switchable Internal Capacitance (all standards)			20		pF
	Maximum Switchable Internal Capacitance (all standards)			50		pF
ΔF	Internal Oscillator Frequency Range for (L = 10 µH, C = 68 pF)		590			kHz
	Frequency Offset, After Automatic Adjustement				± 10	kHz
	Undelayed Signal Outputs	Pins 27 - 28				
V27 V28	DC Voltage			1.6		V
I27 I28	Sink Current		1			mA
	Impedance			30		Ω

TAB-04

Notes :

1. **Rise Time Test Conditions**
   - SECAM Color Bar Patterns 75%
   - Generator TEKTRONIX 143
   - Standard Application without any output load
   - Measure between 10% and 90% on the major transition (Green Violet)

2. **Overshoot Test Conditions**
   - Same as for Rise Time
   - Ratio between the value of the overshoot and the peak-to-peak value of the transition after overshoot

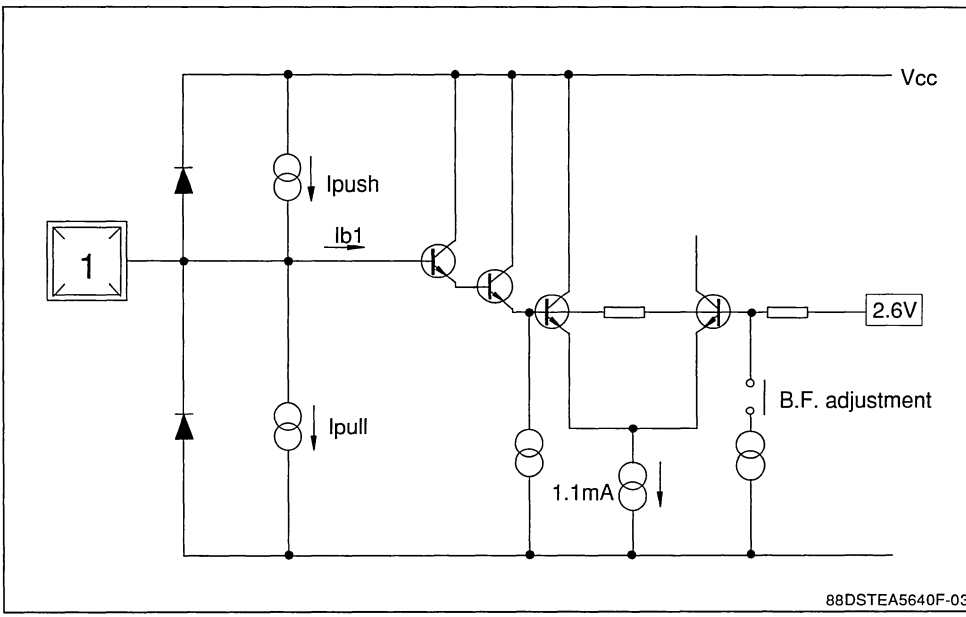
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Identification				
	Burst Attenuation Range / Nominal Level				
	SECAM Mode (line identification)	30			dB
	PAL Mode	30			dB
V26	PAL Mode (with $R_{pin(26)}$=100kΩ/GND)	4		5	V
V26	SECAM Mode (with $R_{pin(26)}$=100kΩ/GND)	6.2		7.2	V
	Delayed Signal Input Pins 2 - 3				
	DC Voltage in PAL Mode		2.4		V
	Input Impedance	0.88	1.1	1.32	kΩ
	Delay Line Attenuation Compensation				
	Range of Automatic Attenuation Compensation	– 3	– 9	– 15	dB
	Delay Line Phase Shift Compensation				
	Range of Phase Shift Compensation with a 100KΩ Potentiometer (see application diagram p. 12)	± 30			degree
	Alternation Line Detection PAL or SECAM Pin 11				
VTHH	High Differential Threshold (VTHH = V11H – V24)	200		350	mV
VTHL	Low Differential Threshold (VTHL = V11L – V24)	– 350		– 200	mV
	Leakage Current Threshold (V11 = V24 + 1V)			0.5	µA

TAB-05

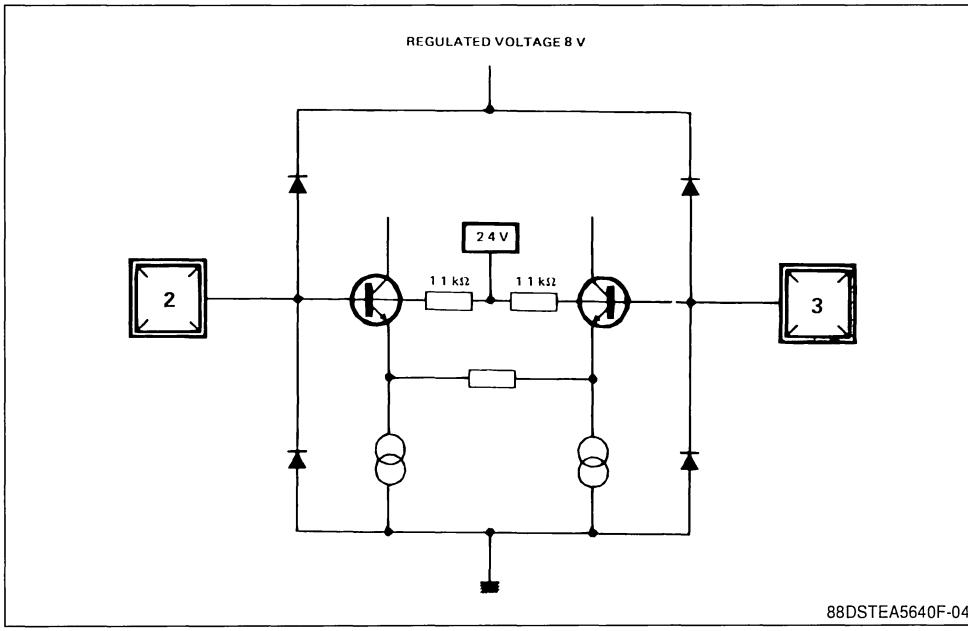
INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

PIN 1

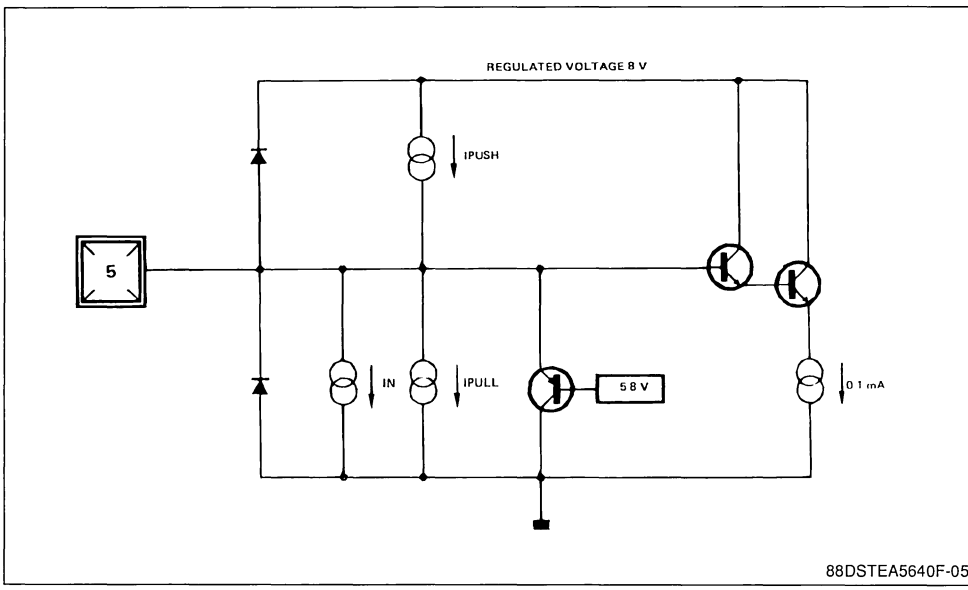


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

PINS 2 – 3

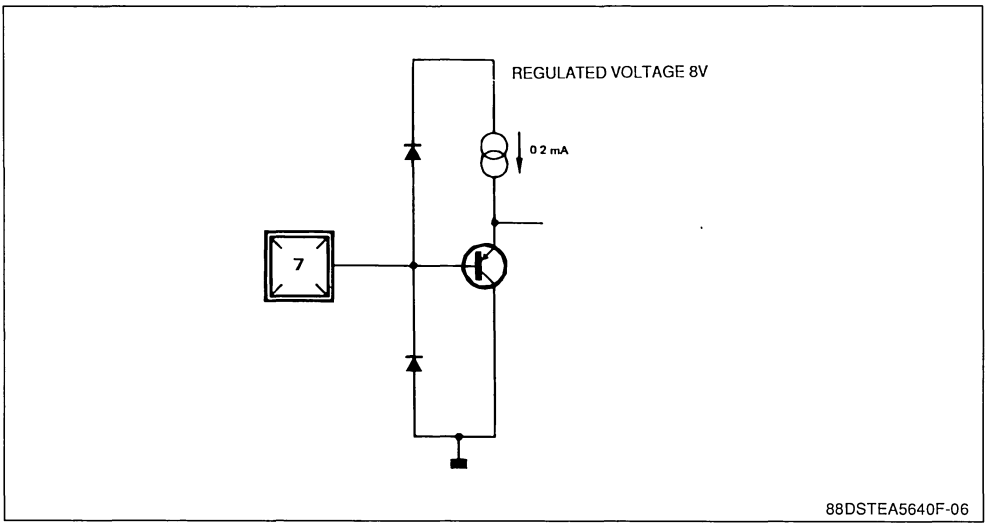


PIN 5

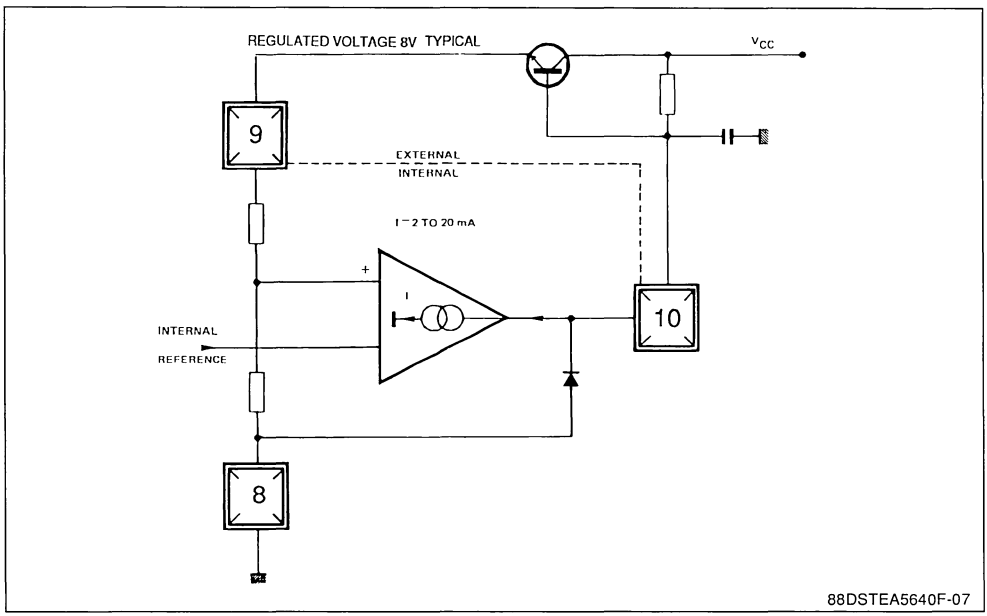


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

PIN 7

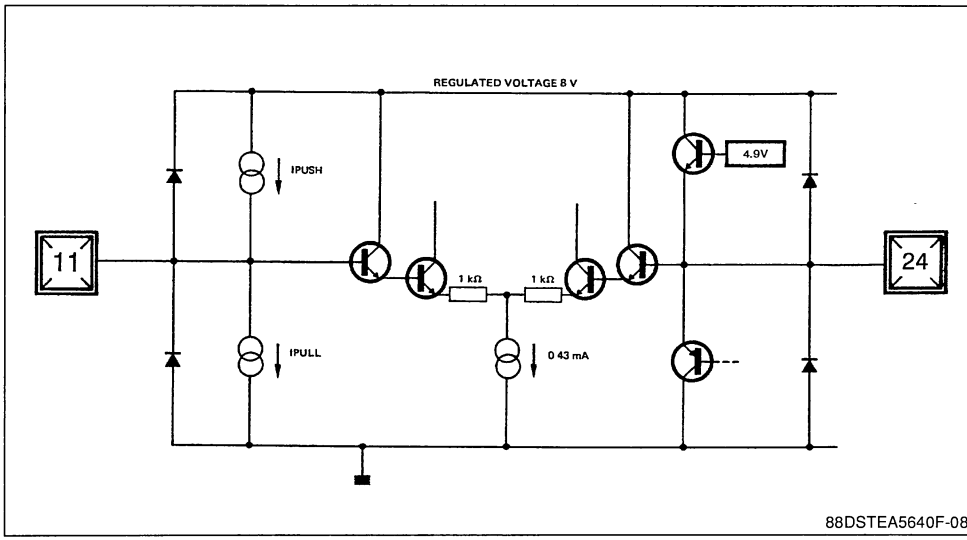


PINS 8 – 9 – 10

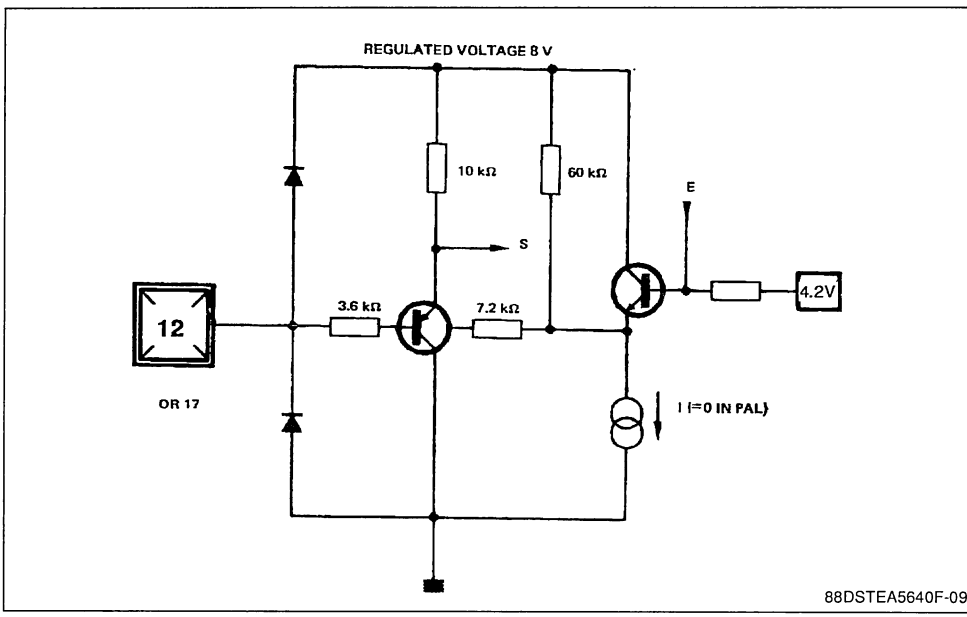


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

PINS 11 – 24

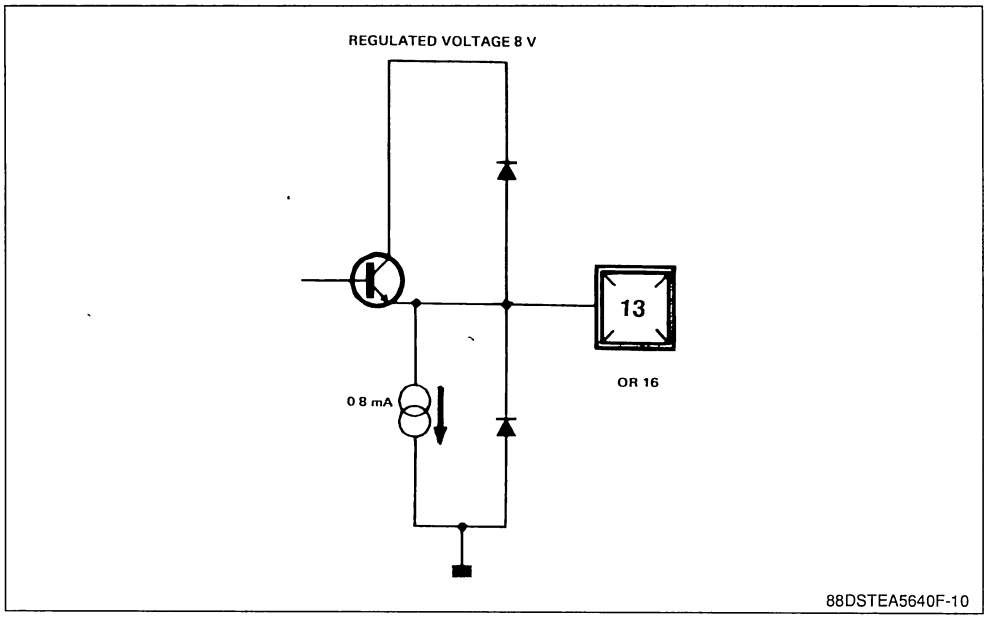


PINS 12 – 17

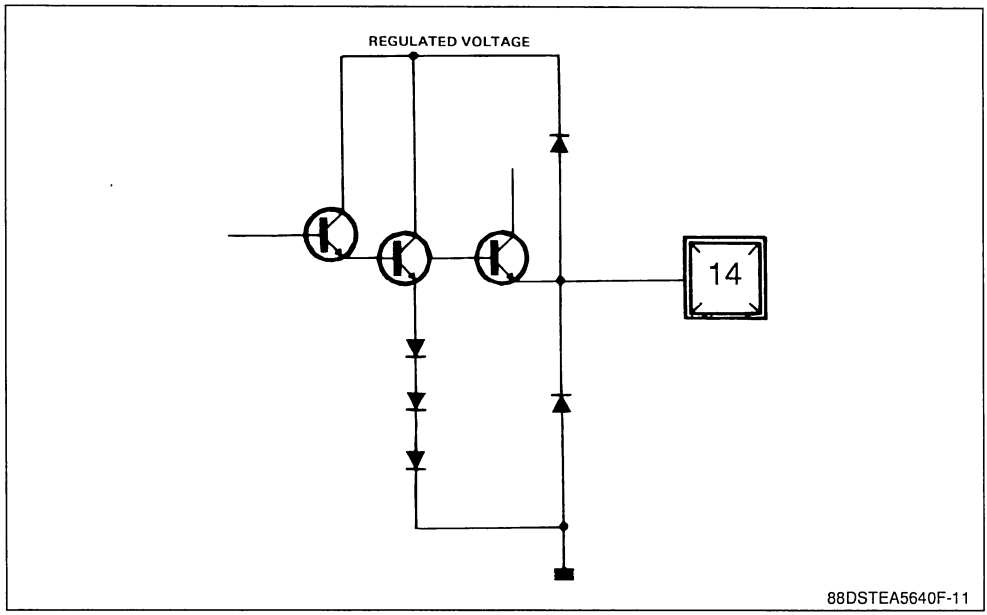


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

PINS 13 – 16

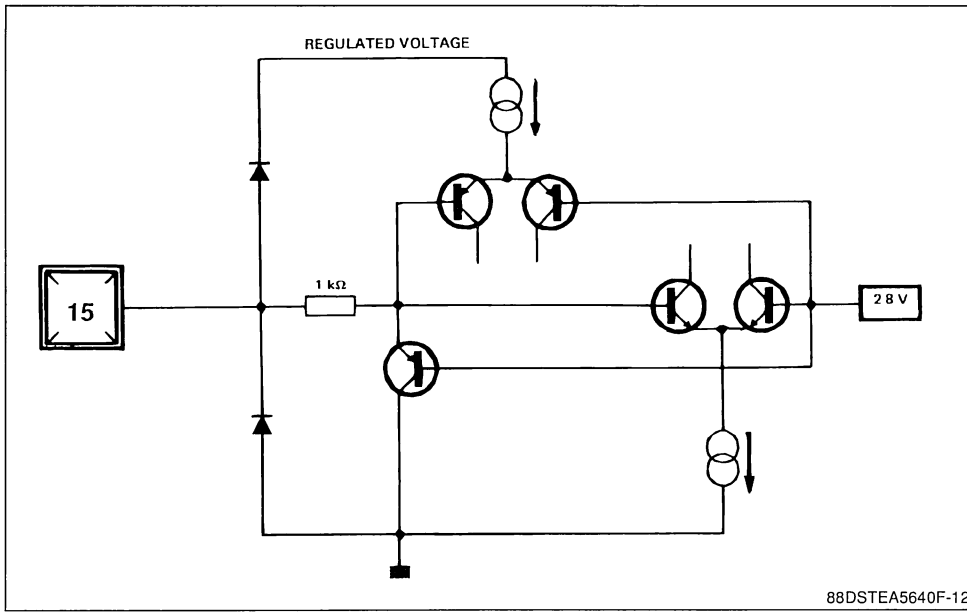


PIN 14

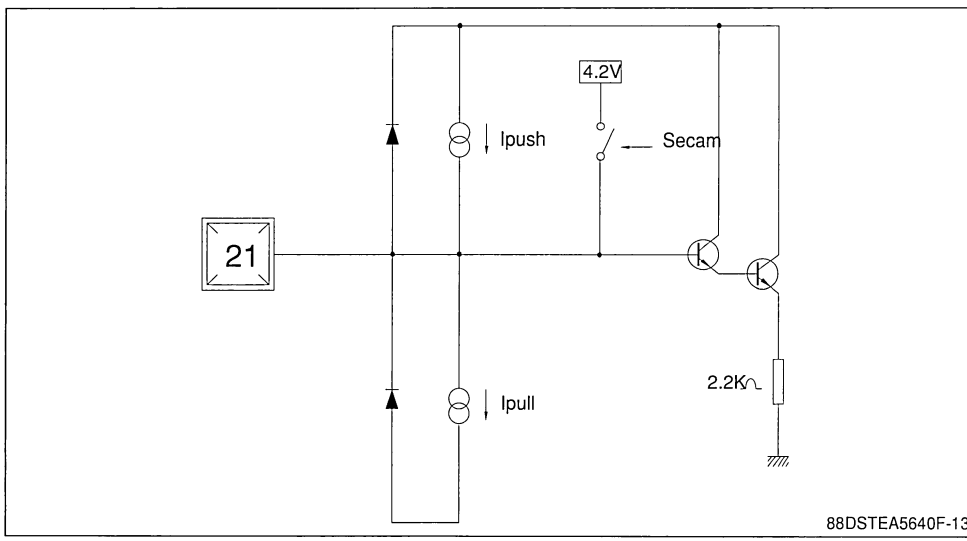


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

PIN 15

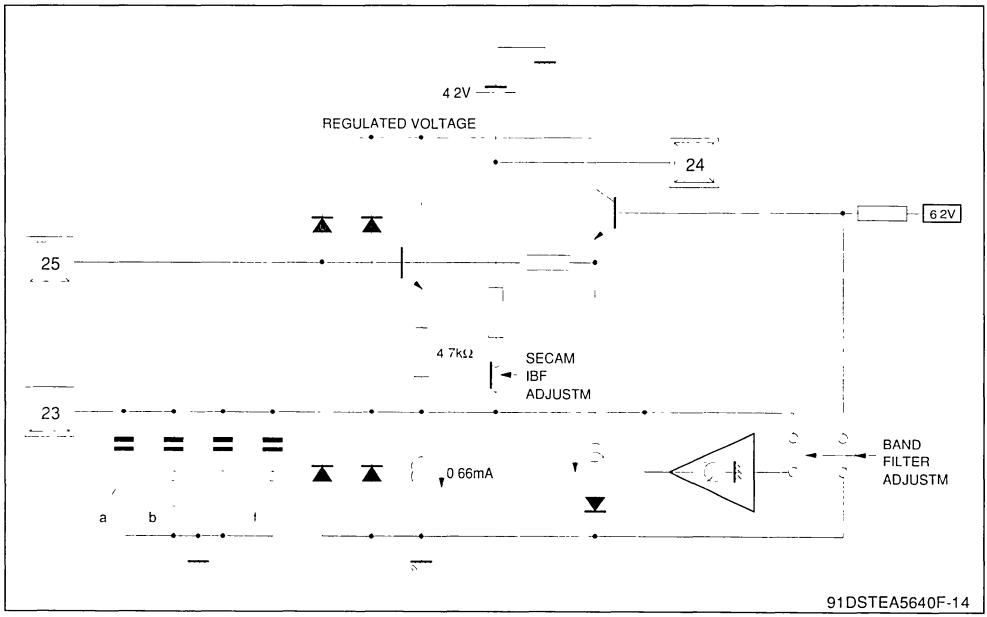


PIN 21

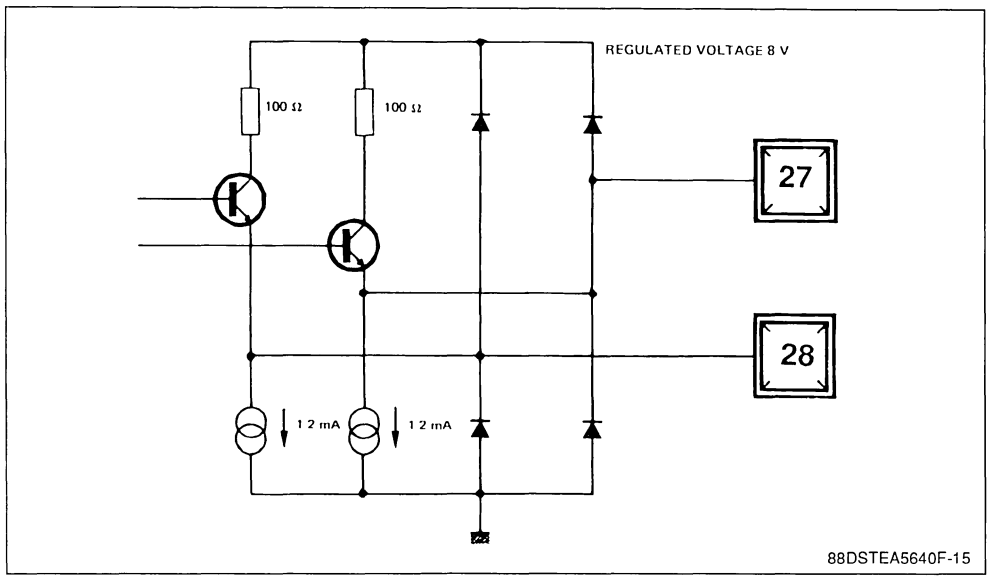


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

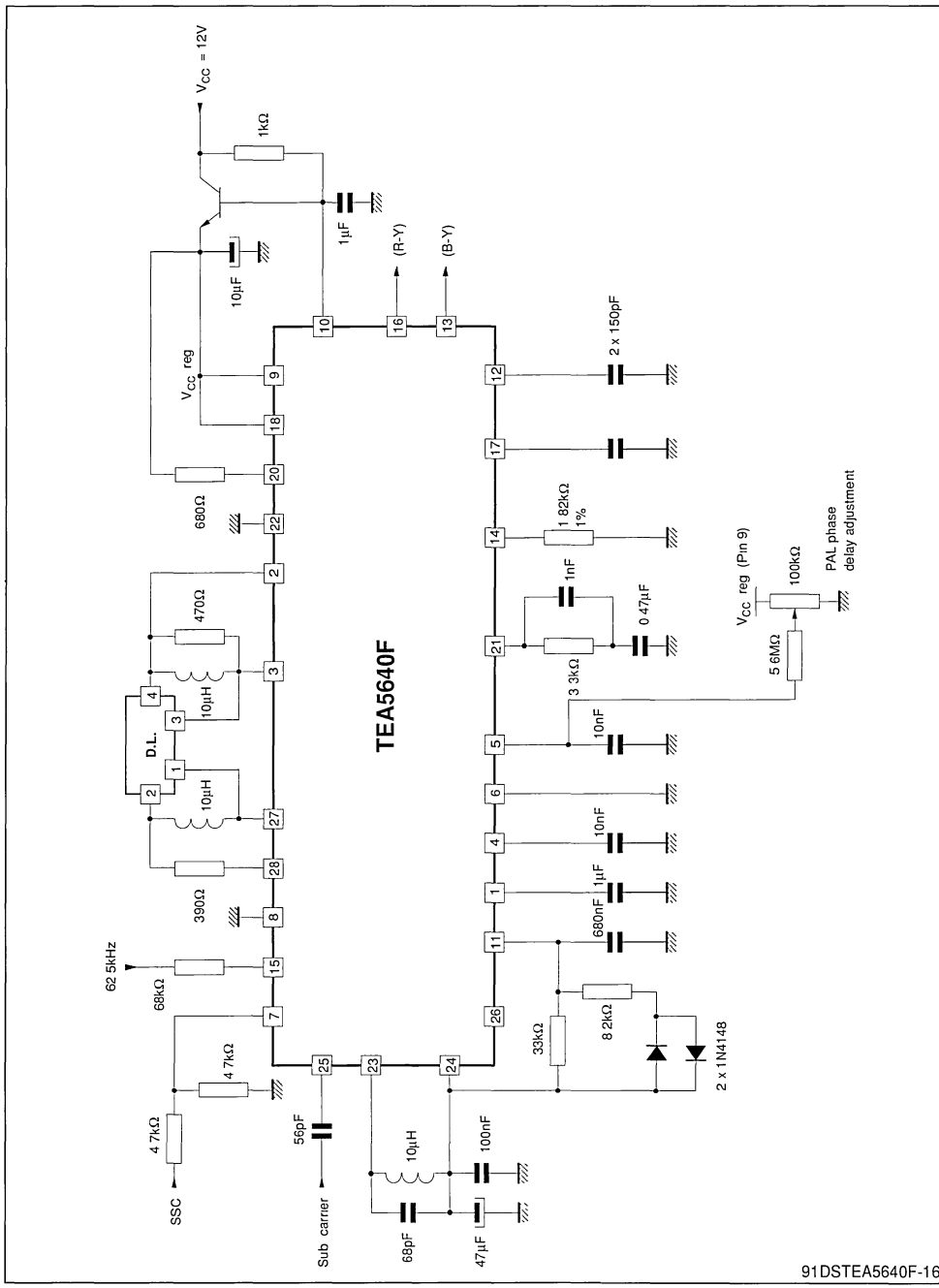
PINS 23 – 24 – 25



PINS 27 - 28

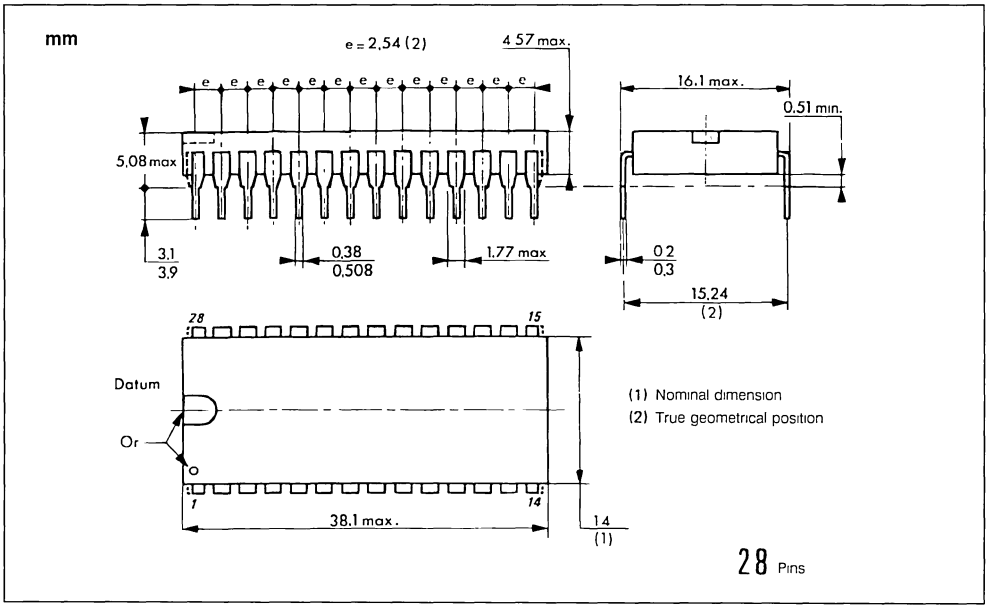


TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP



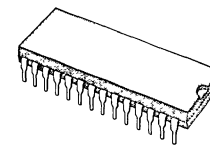
SGS-THOMSON MICROELECTRONICS

TEA5652

WIDE BAND VIDEO PROCESSOR

PRODUCT PREVIEW

- Y, R-Y, B-Y INPUTS
- 2 RGB AND FAST BLANKING
- RGB SOURCES MATRIXING
- ANALOG CUT-OFF CONTROLS
- ANALOG CONTROLS FOR : BRIGHTNESS, CONTRAST, SATURATION
- BEAM CURRENT LIMITER (START AND AVERAGE)
- 62.5kHz GENERATOR (FOR TEA5640)
- INTERNAL INDEXATION BETWEEN SATURATION AND CONTRAST



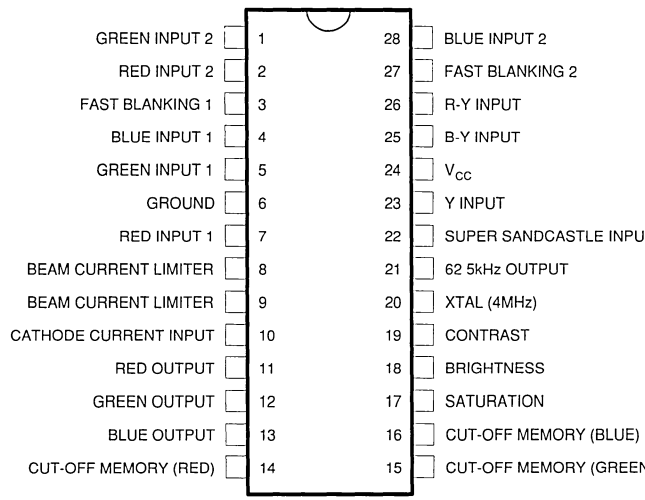
DIP28
(Plastic Package)

ORDER CODE : TEA5652

DESCRIPTION

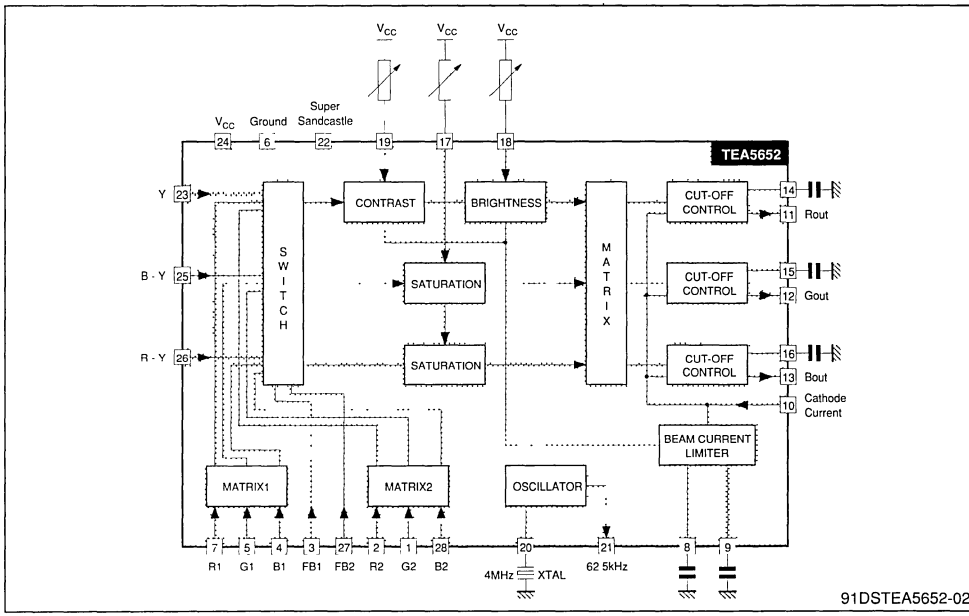
The TEA5652 is a wide band video processor intended for low-cost CTV. It integrates two RGB and fast blanking inputs, a beam current limiter and a 62.5kHz generator (for TEA5640).

PIN CONNECTIONS



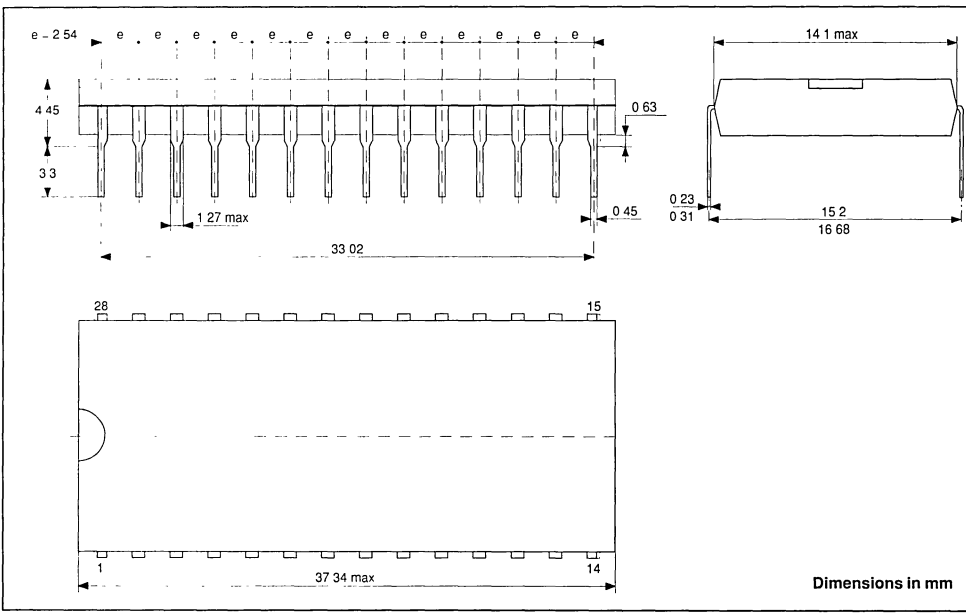
91DSTEA5652-01

BLOCK DIAGRAM



PACKAGE MECHANICAL DATA

28 PINS - PLASTIC PACKAGE



SGS-THOMSON MICROELECTRONICS

TEA5701

3 CHANNEL, LARGE BAND HEAD AMPLIFIER FOR VCR

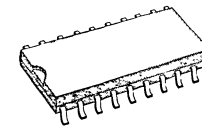
THE TEA5701 IS AN ADVANCED ONE CHIP 3 HEADS RECORD AND PLAY-BACK AMPLIFIER FOR VCR

PLAY-BACK MODE

- LOW NOISE PERFORMANCE
- LARGE BANDWIDTH (SVHS PROCESSING CAPABILITY)
- AUTOMATIC OFFSET CANCELLER BETWEEN TWO SELECTED HEADS
- RECORD AMPLIFIER INHIBITION DURING PLAY-BACK
- DIRECT DRIVE OF COAXIAL CABLE (500 Ω - 100 pF) OF PLAY-BACK OUTPUT

RECORD MODE

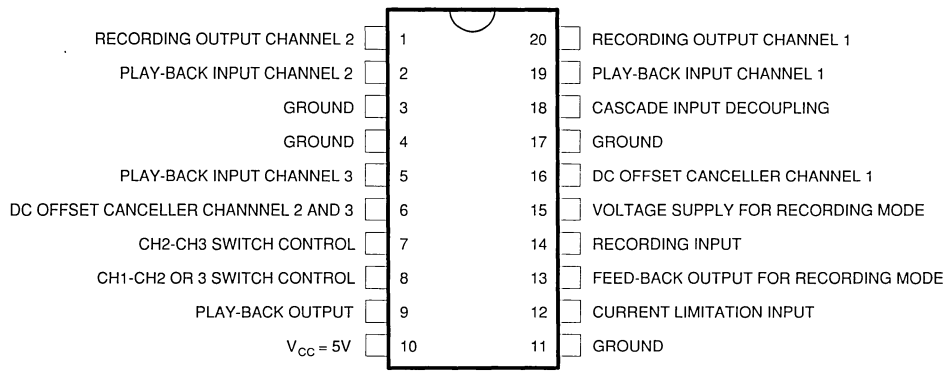
- INTEGRATED I/I CONVERTER WITH AUTOMATIC CONTROL OF TRANSCONDUCTANCE
- AUTOMATIC RECORD PLAY-BACK SWITCHING
- PLAY-BACK INHIBITION DURING RECORD MODE
- AUTOMATIC PROTECTION OF RECORD AMPLIFIER AGAINST SHORT CIRCUIT



SO20
(Plastic Micropackage)

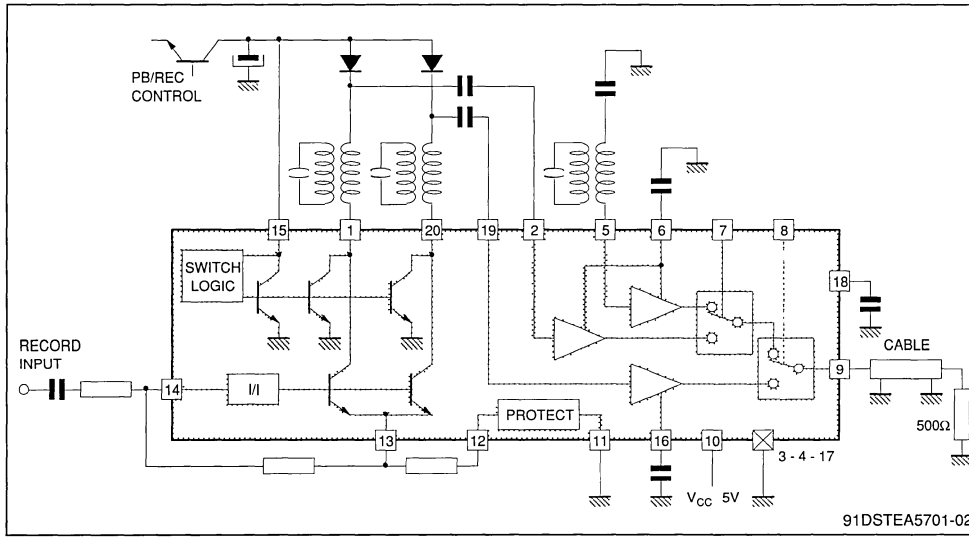
ORDER CODE : TEA5701

PIN CONNECTIONS



91DSTEA5701-01

BLOCK DIAGRAM



DESCRIPTION

TEA5701 is intended for 3 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS and SVHS applications (9 MHz).

High performance technology allows very low noise levels (current and voltage). In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5701 large capability to drive directly a coaxial cable in order to reduce number of external components.

An automatic scanning of recording supply voltage permits that TEA5701 switches automatically in play-back or in record mode. The switching threshold voltage from play-back to record and record to play-back is fixed to a value which forbids high current peaking through the heads.

The recording amplifier includes a protection system which protects the IC and the application board against overheating in case of short circuit on the recording transconductance components.

The TEA5701 is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	6	V
V_{REC}	Supply Voltage	15	V
T_{stg}	Storage Temperature Range	– 40 to + 150	°C

TAB-01

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	70	°C/W

TAB-02

ELECTRICAL OPERATING CHARACTERISTICS

All the operating characteristics are given for ambient temperature 25 °C unless otherwise specified.

PLAY-BACK MODE

General conditions for play-back : V_{CC} = 5 V, no load on play-back output.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5	5.25	V
I_{CC}	Current Supply			45	60	mA
G_{PB}	Play-back Gain	Sine Wave 400 mVpp at 600 khz on Pin 9	56	60	63	dB
ΔG_{PB}	Gain Difference Between Three Play-back Channels	Sine Wave 3.8 MHz, 0.4 mVpp on Pins 2 - 5 - 19		0.3		dB
en	Equivalent Input Voltage Noise Level	Measured at 500kHz – CH1 Via Switching Transistor Pin 20 – CH2 Via Switching Transitor Pin 1 – CH3 Grounded		0.4		$nV/\sqrt{Hz}$
in	Equivalent Input Current Noise Level	Measured at 500kHz - PB Inputs Pins 2 - 5 - 19 not Connected		3		$pA/\sqrt{Hz}$
CRT	Crosstalk	Sine Wave 3.8MHz 400 mVpp on Pin 9 For selected channel : – CH1 input, between pins 19 and 20 – CH2 input, between pins 1 and 2 – CH3 input, between pin 5 and ground.			– 40	dB
FLCPB	Play-back Bandwidth Low Cut Off Frequency	Reference Signal Level : Sine Wave 3.8MHz 400 mVpp – Play-back Input Capacitors 22 nF (pins 2 - 6 - 19) – DC Offset Canceller Capacitor (pins 6 - 16-) 47 nF		20	100	kHz

TAB-03

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
FHCPB	Play-back Bandwidth High Cut Off Frequency	Same Conditions as Above	8	9.5		MHz
C_{in}	Play-back Input Capacitance Pins 2 - 5 - 19			50		pF
R_{in}	Play-back Input Resistance Pins 2 - 5 - 19			600		Ω
VDCPB	DC Level on Play-back Output Pin 9 during Play-back	With 500 Ω Load Resistor Between Pin 9 and Ground	1.9	2.4	2.9	V
ΔVDC	Head Switch Offset Pin 9 (all switches combinations)				50	mV
SM	Second Harmonic on Play-back Output Pin 9	Sine Wave 3.8 MHz 400 mVpp with 500 Ω load Resistor		– 43	– 38	dB
V_{sat}	Maximum Voltage on Pins 1 and 20 at Play-back Mode	Input Current Pins 1 and 20 20 mADC			100	mV

TAB-04

RECORDING MODE

General conditions for recording mode : V_{REC} = 12 V
V_{CC} = 5 V
Load resistor 100 Ω on pins 1 and 20
No load on play-back output pin 9

Transconductance network defined by : R1 = 5.1 Ω 1 % pins 12-13
R2 = 1 kΩ 1 % pins 13-14
R3 = 750 Ω 1 % pin 14

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REC}	Recording Supply Voltage		9	12	12.6	V
ICCREC	Current Supply from V_{REC}			50	60	mA
ICCI	Current Supply from V_{CC}			30	37.5	mA
VDCREC	DC Level on Play-back Output Pin 9	With 500 Ω Load Resistor Between Pin 9 and Ground	3.1	3.6	4.1	V
	Maximum Recording Current on Each Channel	f = 1.6 MHz	40			mApp
	Maximum Recording Current on Each Channel	f = 3.8 MHz	35			mApp
g	Transconductance	R1 = 5.1 Ω 0 % R2 = 1000 Ω 0 % R3 = 750 Ω 0 % V_{in} = 300 mVpp Measured at 500 KHz		132		mA/V
Δ g	Recording Current Difference Between Pins 1 and 20	Sine Wave 3.8 MHz Irecording = 30 mA_{PP}			0.5	dB
REREC	Equivalent Input Resistance			660		Ω

TAB-05

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_S	Output Resistance Pins 1 and 20	R1 = 5.1 Ω		100		kΩ
SHREC	Second Harmonic Pins 1 and 20	Output Current on Each Output : 30 mApp at 3.8 MHz			– 38	dB
FLCREC	Recording Bandwidth Low Cut Off Frequency	Reference Output Current 30 mApp at 3.8 MHz for – 3 dB		20	100	kHz
FHCREC	Recording Bandwidth High Cut Off Frequency	Reference Output Current 30 mApp at 500 KHz for – 3 dB	8	9.5		MHz
	Maximum Input Current Pin 12	Pin 12 Connected to VREC = 12 V			100	mA
	Maximum Saturation Voltage on Pin12	Input Current Pin 12 : 50 mA		100	150	mV
IM	Intermodulation	I Luminance = 30 mApp 3.8 MHz I Chrominance = 7.5 mApp, 600 KHz Measured at 3.8 MHz ± 600 KHz		– 50		dB

TAB-06

SWITCHING LEVELS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{H8}	Threshold Voltage for Head 1 Selection on Pin 8		2.4		V_{CC}	V
V_{L8}	Threshold Voltage for Head 2 or 3 Selection on Pin 8		0		1.5	V
I_{H8}	Input Current Pin 8 for H1 Selected	Pin 8 Connected to V_{CC}			50	µA
I_{L8}	Output Current Pin 8 for H2 or 3 Selected	Pin 8 Connected to Ground			– 50	µA
V_{H7}	Threshold Voltage for Head 2 Selection on Pin 7		2.4		V_{CC}	V
V_{L7}	Threshold Voltage for Head 3 Selection on Pin 7		0		1.5	V
I_{H7}	Input Current Pin 7 for Head 2 Selected	Pin 7 Connected to V_{CC}			50	µA
I_{L7}	Output Current Pin 7 for Head 3 Selected	Pin 7 Connected to Ground			– 50	µA
	Switching Time from H1 Selected to H2 Selected	Switching Pulse from 5 to 0 V Applied Pin 8		250	500	ns
	Switching Time from H2 Selected to H1 Selected	Switching Pulse from 0 to 5 V Applied Pin 8		250	500	ns

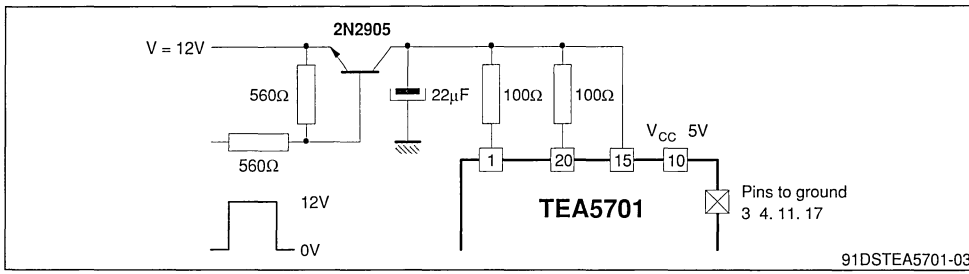
TAB-07

ELECTRICAL CHARACTERITICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VRPB	Recording Supply Voltage Threshold (pin 15) for Switching from Record to Play-back		0.15	0.3	0.5	V
VPBR	Recording Supply Voltage Threshold (pin 15) for Switching from Play-back to record		0.25	0.4	0.6	V
	Delay Time for Suppression of Play-back Output Signal on Pin 9 (play-back to record)	See Measurement Conditions End of Paragraph		30		µs
	Delay Time for Presence of Play-back Output Signal on Pin 9 (record to play-back)	See Measurements Conditions End of Paragraph		20		ms
	Delay Time for Suppression of Recording Signals Pins 1 and 20 (record to play-back)	See Measurements Conditions End of Paragraph		4		ms
	Delay Time for Suppression of Recording Signals Pin 1 and 20 (play-back to record)	See Measurements Conditions End of Paragraph		200		µs
SVR	Supply Voltage Rejection	Gain Measure Made Between Play-back Output Pin 9 and V_{CC} (0.5 mVpp on pin 10)	15	20	25	dB

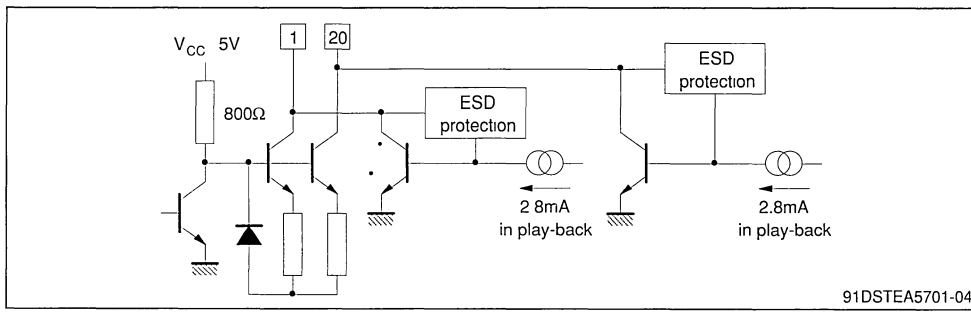
TAB-08

Test Conditions for Measuring Delay Times (play-back to record and vice versa)



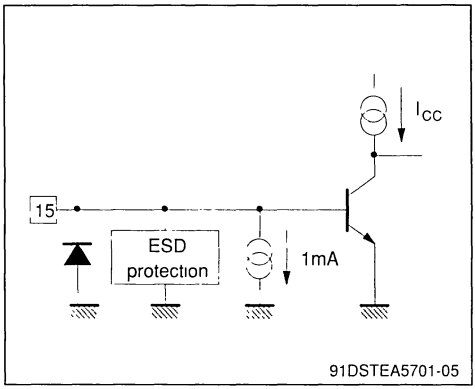
INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

PIN 1 AND 20

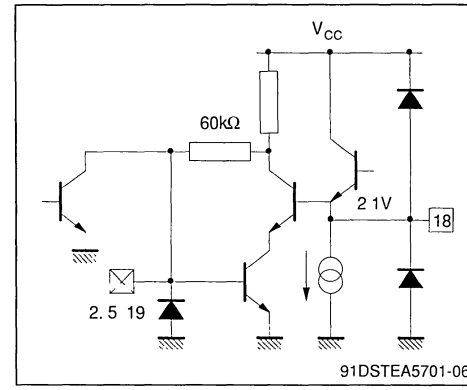


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

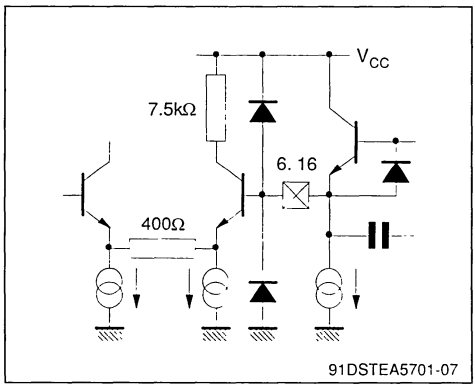
PIN 15



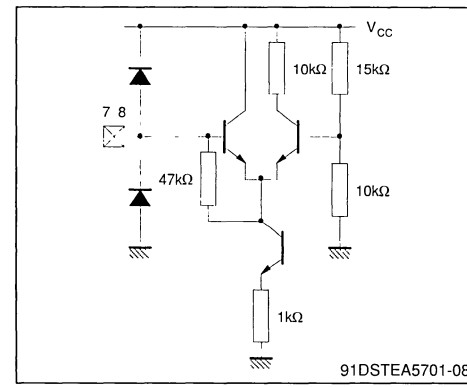
PINS 2 - 5 - 19 - 18



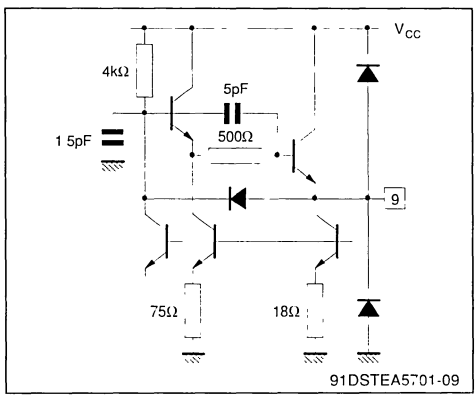
PINS 6 - 16



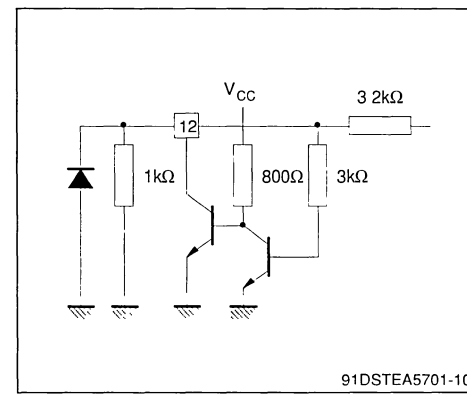
PINS 7 - 8



PIN 9

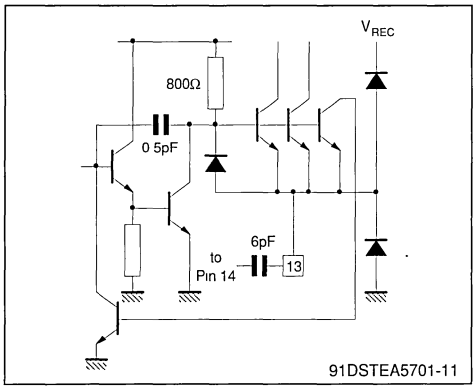


PIN 12

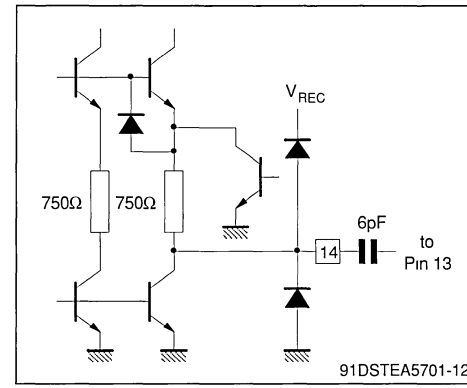


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

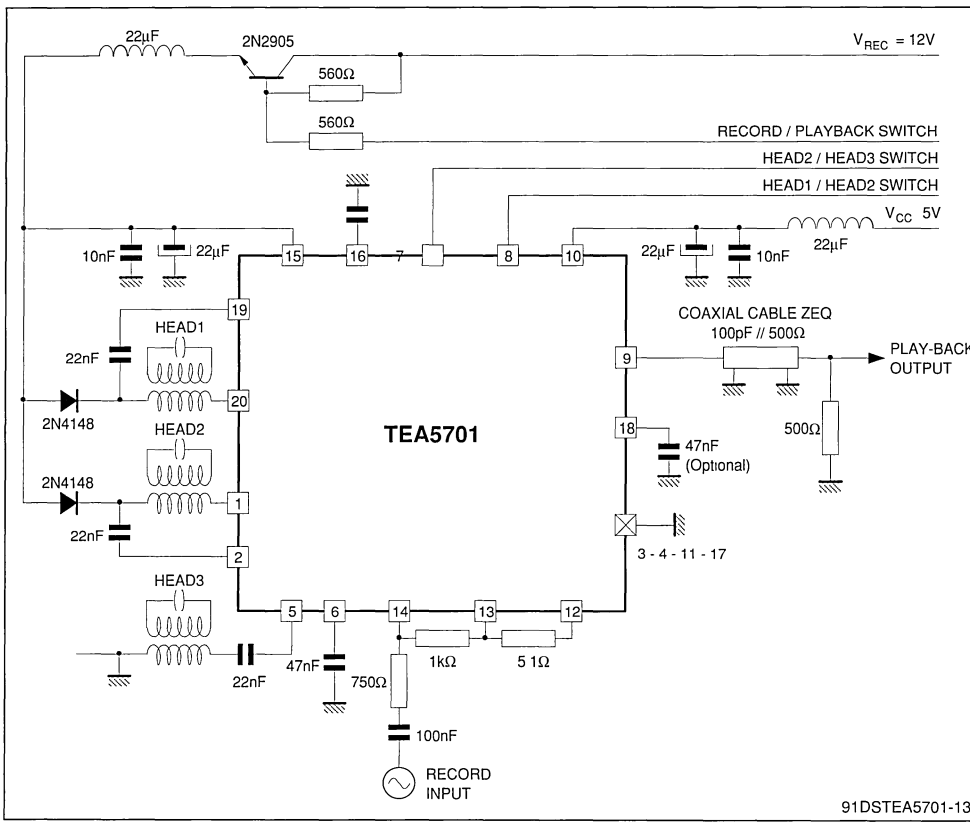
PIN 13



PIN 14

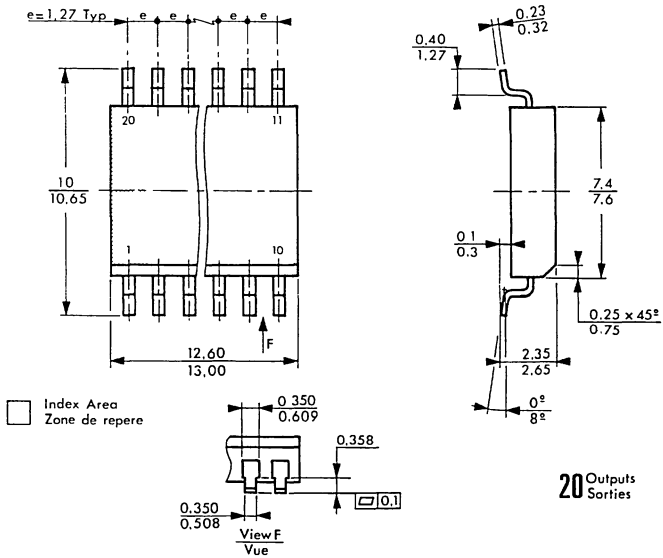


TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

SO20 LARGE – PLASTIC MICROPACKAGE



SGS-THOMSON MICROELECTRONICS

TEA5702

ADVANCED 2-HEAD PLAY-BACK AND RECORD AMPLIFIER FOR VCR

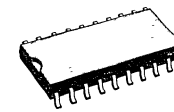
ADVANCE DATA

PLAY-BACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 2 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAY-BACK OUTPUT WITHOUT AGC
- TWO PLAY-BACK OUTPUTS INCLUDING AGC (PHASE AND OPPOSITE PHASE)
- RECORD AMPLIFIER INHIBITION AND RECORD OUTPUT GROUNDED
- OUTPUT FOR TRACKING VIDEO INFORMATION (TRIV)

RECORD MODE

- ONE INTEGRATED I/I CONVERTER WITH ACCURATE CONTROL OF TRANSCONDUCTANCE
- AUTOMATIC PLAY-BACK/RECORD SWITCHING BY SCANNING OF RECORD SUPPLY
- PLAY-BACK LOOP INHIBITION



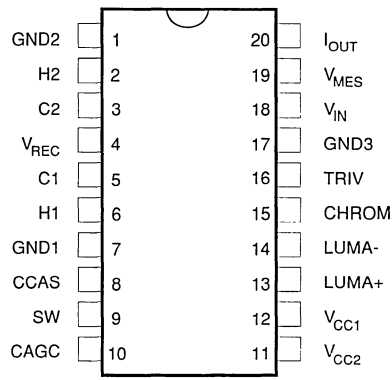
SO20
(plastic micropackage)

ORDER CODE : TEA5702

DESCRIPTION

The TEA5702 is an advanced two head record and play-back amplifier for VCR.

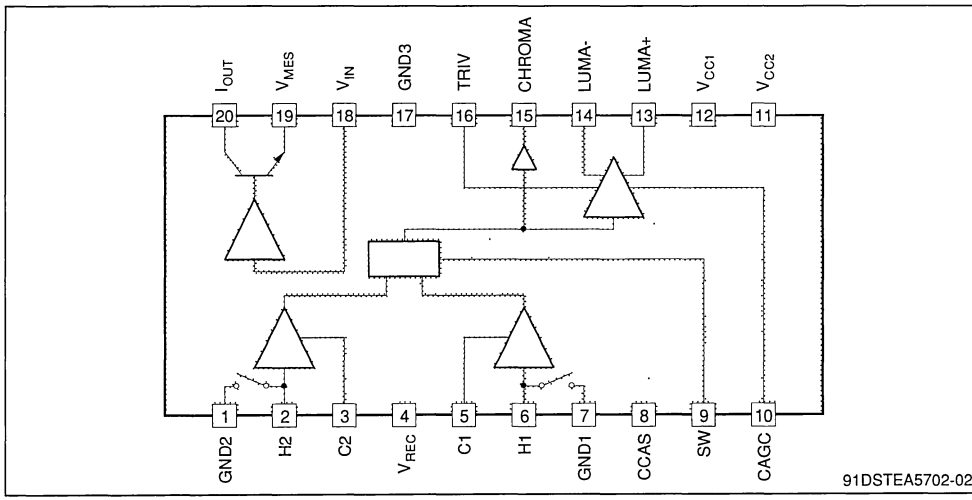
PIN DESCRIPTION



91DSTEA5702-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

TEA5702 is intended for 2 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS applications.

High performance technology allows very low noise levels (current and voltage). In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5702 large capability to drive directly a coaxial cable in order to reduce number of external components.

Three play-back outputs are availabe : one, dedicated to Chroma processing, is a 60dB voltage amplifier output, the two others, dedicated to Luma processing, are phase opposite signals with a constant AC output level of 200mV_{PP} at 3.8MHz signal.

A tracking information for video signal (TRIV) is Luma amplitude proportional and allows automatic phase correction.

An automatic scanning of record supply voltage permits TEA5702 automatically switching either in play-back or in record mode. The switching threshold voltage is fixed to a value which forbids high current peaking through the heads.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for the two heads, the DC current and the AC characteristics can be very precisely controlled with accurate external resistors. If recommended resistances are used, a ± 3% transconductance accuracy is guaranteed.

TEA5702 is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	6	V
V_{REC}	Power Supply Voltage Record	15	V
T_J	Junction Temperature	150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance (Typ.)	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Power Consumption

Parameter		Play-Back		Record (1)	
		Typ.	Max.	Typ.	Max.
V_{CC}		35mA	45mA	25mA	35mA
V_{REC}		0mA	0mA	45mA	55mA
Total Consumption (2)	V_{CC} = 5, V_{REC} = 10	175mW		530mW	
	V_{CC} = 5.25, V_{REC} = 10.5		240mW		760mW

Notes : 1. R1 = 10Ω
2. Taking in account only the consumption through the IC.
A great care should be taken to the maximum power consumption . V_{REC} can be increased to 12.6V if the DC current flowing through the head is reduced. This can be done by increasing R1 value

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA, LUMA+, LUMA-.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current		25	35	45	mA
V_{CC}	Supply Voltage		4.75	5	5.25	V
CHROMA OUTPUT (no AGC)						
G_{PB}	Pre-amplification Gain	Sinus wave 600 kHz 400mV_{PP} on output Input on Pin H1 or H2	57	60	63	dB
ΔG_{PB}	Gain Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2	Sinus wave 3.8MHz 0.4mV_{PP} on inputs H1 or H2			1.2	dB
e_N	Equivalent Input Voltage Noise Level (see note)	Input grounded via switching transistor on Pins H1, H2		0.6		$nV/\sqrt{Hz}$
i_N	Equivalent Input Current Noise	Pins H1, H2		2		$pA/\sqrt{Hz}$
CRT	Crosstalk	Sinus wave 3.8MHz 400µV_{PP}, All switches combinated			-40	dB
F_{LCPB} F_{HCPB}	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, 0dB at 600kHz Low High	 8		0.1	 MHz MHz
C_{IN}	Input Capacitance Pins H1, H2			30		pF
R_{IN}	Pre-amplifier Input Resistance Pins H1, H2		400	600	900	Ω
Z_{CPB}	Output Impedance	Sinus wave 1MHz 400µV_{PP} on input		30	50	Ω
V_{DCPB1}	DC Level			1.34		V
ΔV_{DC}	Head Switch Offset				50	mV
SH_{PB1}	Second Harmonic	Sinus wave 600kHz 400µV_{PP} on input			-40	dB
LUMA+, LUMA- OUTPUTS (with AGC)						
Z_{LPB}	Output Impedance	Sinus wave 1MHz 400µV_{PP} on input		30	50	Ω
V_{DCPB2}	DC Level			1.5		V
V_{LPB}	Output Amplitude	Input signal 200µV_{PP} at 3.8MHz on Pins H1, H2	140	200	270	mV_{PP}
ΔV_{LPB}	AGC Control Sensitivity	Input signal 200µV_{PP} at +6dB or -5dB on Pins H1, H2	-2		+1	dB

Note : These values can be adjusted to the application

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA, LUMA+, LUMA-.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LUMA+, LUMA- OUTPUTS (with AGC) (continued)						
SH_{PB2}	Second Harmonic Play-back Output	Input Signal 3.8MHz 400µV_{PP} on Pins H1, H2		-43		dB
I+	Positive Output Current on Pin CAGC	Input Signal 3.8MHz 200µV_{PP} on H1, 1V on Pin CAGC	15	30	45	µA
I-	Negative Output Current on Pin CAGC	Input Signal 3.8MHz 200µV_{PP} on H1, 3.5V on Pin CAGC	-45	-30	-15	µA
TRIV						
R_{TRIV}	Downloading Resistance		20	40	80	kΩ
V_{TRIV1} V_{TRIV2}	Output Level	V_{CHROMA} = 400mV_{PP} V_{CHROMA} = 100mV_{PP}		3.5 1 6		V V
G_{TRIV1} G_{TRIV2}	Gain	V_{CHROMA} = 300, 400mV_{PP} V_{CHROMA} = 50, 100mV_{PP}		3 12		V/V_{PP} V/V_{PP}

Record Mode

V_{REC} = 10V, V_{CC} = 5V, Load resistor 100Ω on Pin I_{OUT}

Transconductance network defined by : R1 = 10Ω 1% Pins GND3/V_{MES}

R2 = 1kΩ 1% Pins V_{MES}/V_{IN}

R3 = 750Ω 1% Pins V_{IN}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{REC} I_{CC2}	Current Supply	V_{REC} = 10V V_{CC} = 5V		45 25	55 35	mA mA
I_{OUT}						
I_{max}	Max. Record Current	3.8MHz	70			mA_{PP}
TR	Transconductance	V_{IN} = 300mV_{PP}		140		mA/V
SH_{REC}	Second Harmonic	Output Current 60mA_{PP} at 3.8MHz		-48	-40	dB
F_{LCREC} F_{HCREC}	Bandwidth Cut-off Frequency	-3dB attenuation, 0dB at 3 8MHz Output current 60mA_{PP} Low High	 8		 0 1	 MHz MHz

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SWH}	Head Selection Pin SW	Head number 1 (high level)	2.4		V_{CC}	V
V_{SWL}		Head number 2 (low level)	0		1.5	V
I_{SWH}		Input current (high level)			50	µA
I_{SWL}		Output current (low level)			50	µA
t_{ON}	Selection Pin SW Transient Response	Delay time selection ON (output signal appears on Pin CHROMA)		250	500	ns
t_{OFF}		Delay time selection OFF (output signal disappears on Pin CHROMA)		250	500	ns

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{TH1}	Inhibition Threshold for Switching from Play-back to record on Pin V_{REC}	V_{CC} = 5V	0.15	0.3	0.5	V
V_{TH2}	Inhibition Threshold Hysteresis for Switching from Record to Play-back on Pin V_{REC}	V_{CC} = 5V		80		mV
t_1	Transient Response of Record Scanning on Pin V_{REC}	Delay from play-back to record (signal disappears on Pin CHROMA)		30		µs
t_2		Delay from record to play-back (signal appears on Pin CHROMA)		2*		ms
t_3		Delay from play-back to record (signal appears on Pin I_{OUT})		0 2		ms
t_4		Delay from record to play-back (signal disappears on Pin I_{OUT})		4*		ms

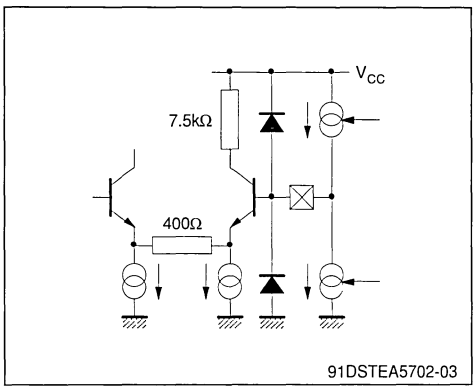
* Depending on capacitance on Pin V_{REC}

Power Supply

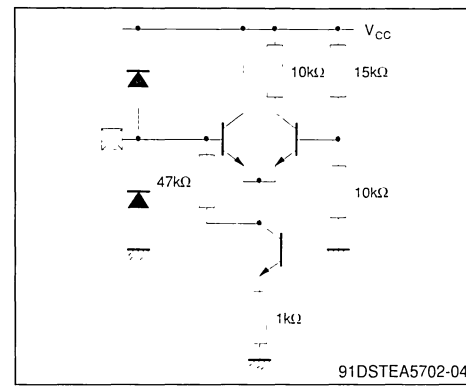
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Positive Supply Voltage Pin V_{CC}		4.75	5	5.25	V
V_{REC}	Record Voltage Pin V_{REC}		4.75	10	12.6	V
SVR	Supply Voltage Rejection	0.5mV_{PP} on Pin V_{CC} 75µV_{PP} on Pin H1, H2 Measurement on Pin Chroma	15	20		dB

INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

Pins : C1, C2

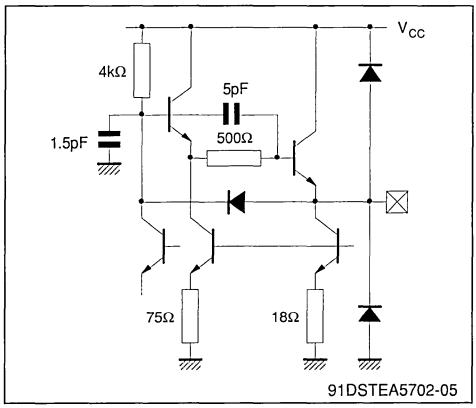


Pin : SW

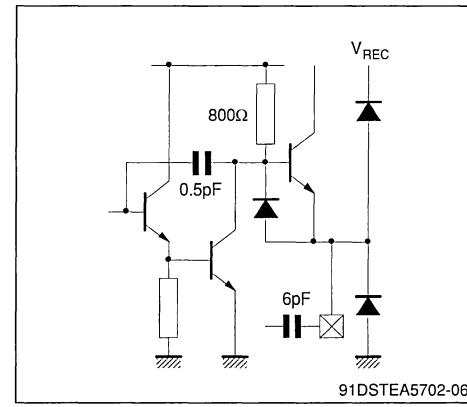


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

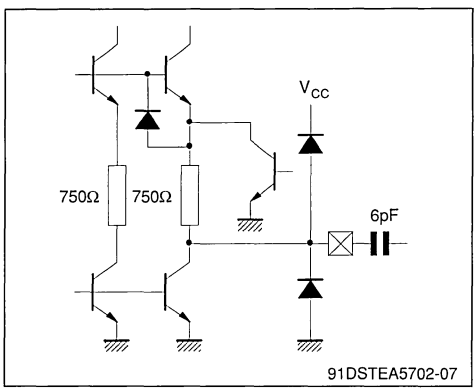
Pins : Chroma, Luma+, Luma-



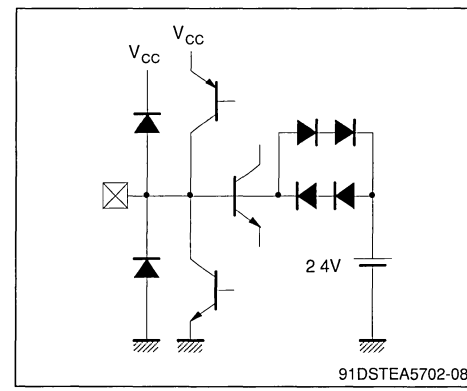
Pin : V_{MES}



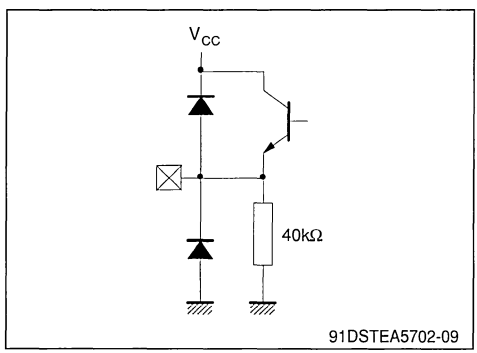
Pin : V_{IN}



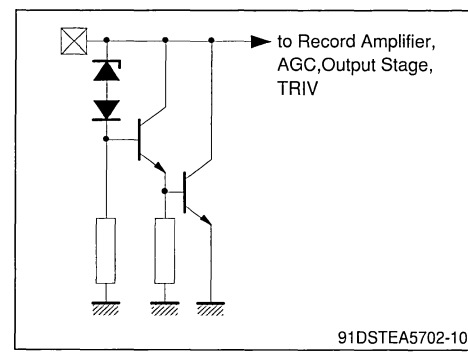
Pin : CAGC



Pin : TRIV

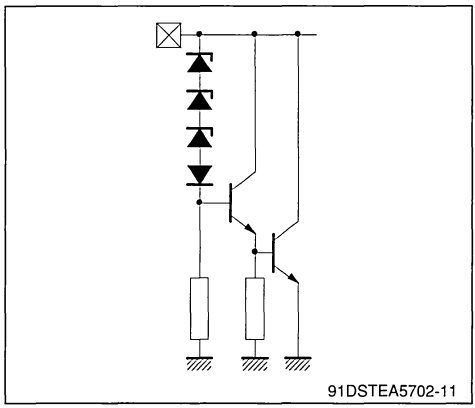


Pin : V_{CC1}

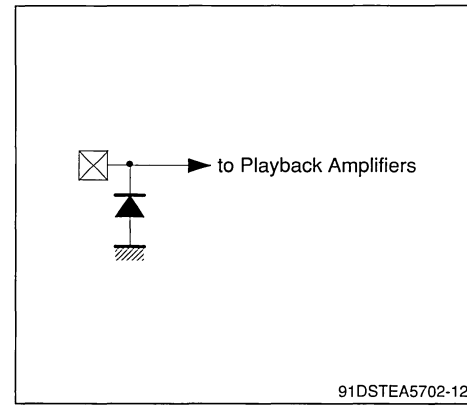


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

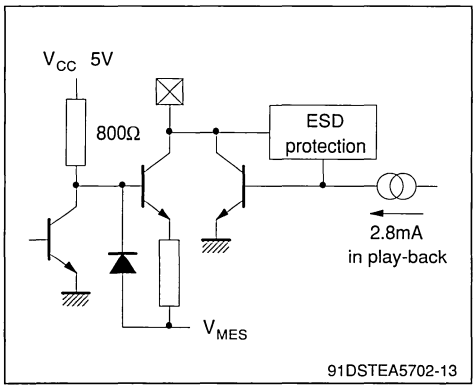
Pin : V_{REC}



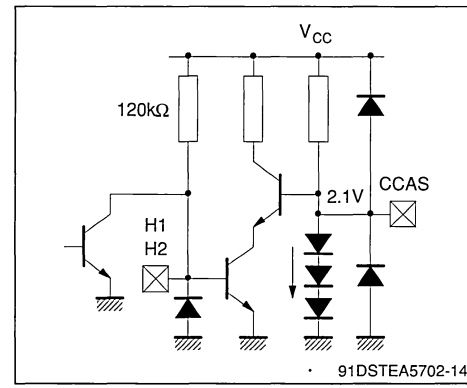
Pin : V_{CC2}



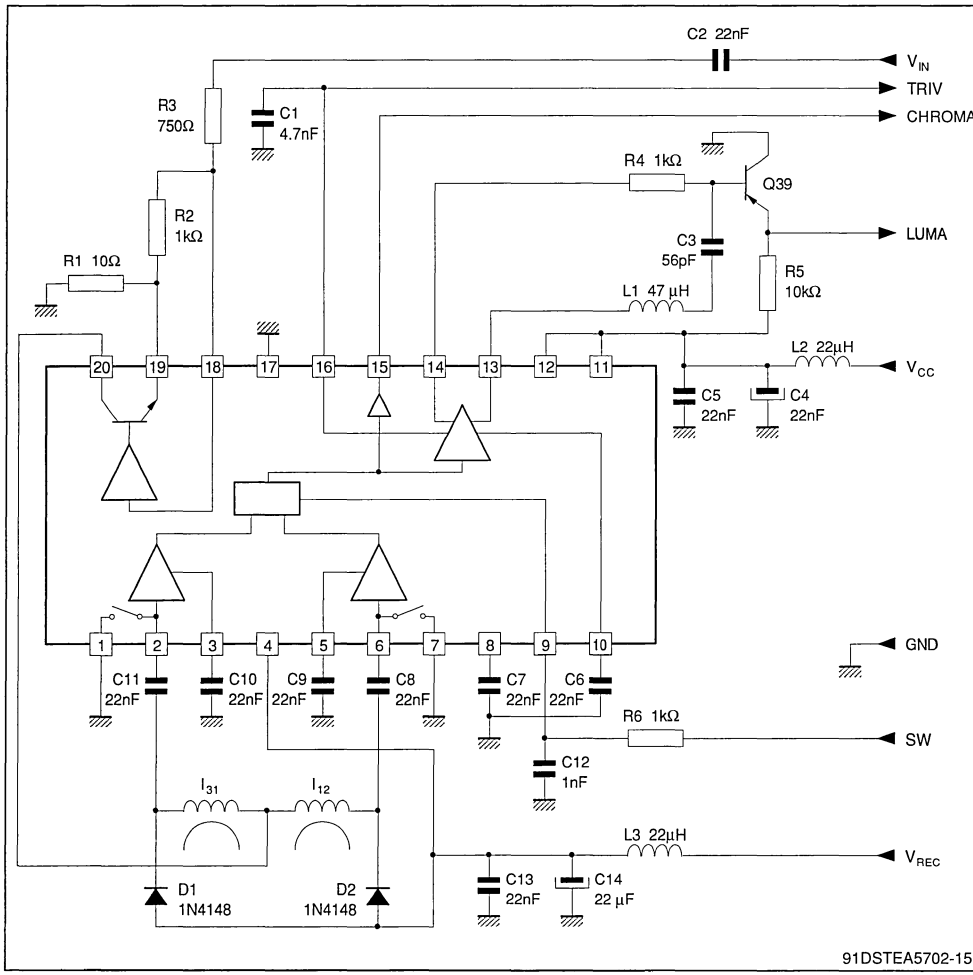
Pin : I_{OUT}



Pins : H1, H2, CCAS

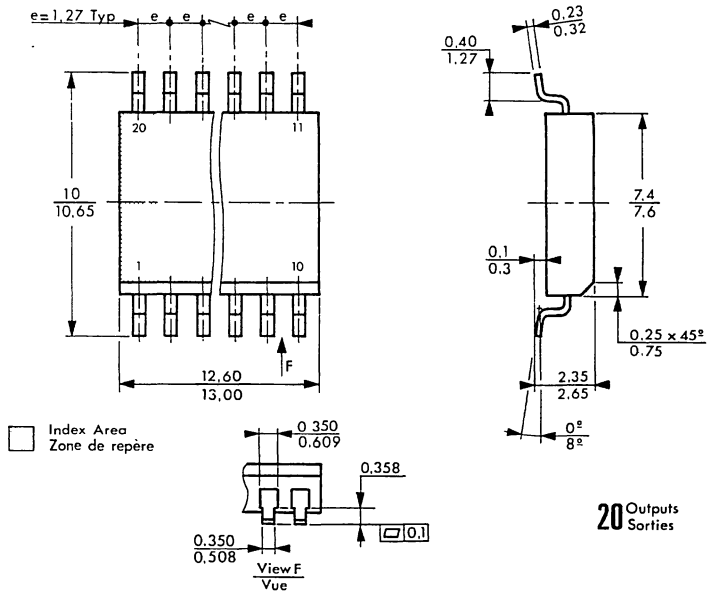


APPLICATION DIAGRAM



PACKAGE MECHANICAL DATA

20 PINS - PLASTIC MICROPACKAGE



SGS-THOMSON MICROELECTRONICS

TEA5703

ADVANCED 3-HEAD PLAY-BACK AND RECORD AMPLIFIER FOR VCR

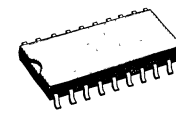
ADVANCE DATA

PLAY-BACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 3 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 3 SELECTED HEADS
- ONE PLAY-BACK OUTPUT WITHOUT AGC
- ONE PLAY-BACK OUTPUT INCLUDING AGC (OPPOSITE PHASE)
- RECORD AMPLIFIER INHIBITION AND RECORD OUTPUT GROUNDED
- OUTPUT FOR TRACKING VIDEO INFORMATION (TRIV)

RECORD MODE

- ONE INTEGRATED I/I CONVERTER WITH ACCURATE CONTROL OF TRANSCONDUCTANCE
- AUTOMATIC PLAY-BACK/RECORD SWITCHING BY SCANNING OF RECORD SUPPLY
- PLAY-BACK LOOP INHIBITION
- RECORD AMPLIFIER WITH AUTOMATIC PROTECTION AGAINST SHORT CIRCUIT



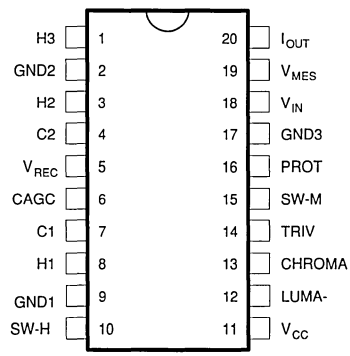
SO20 LARGE
(plastic micropackage)

ORDER CODE : TEA5703

DESCRIPTION

The TEA5703 is an advanced three head record and play-back amplifier for VCR.

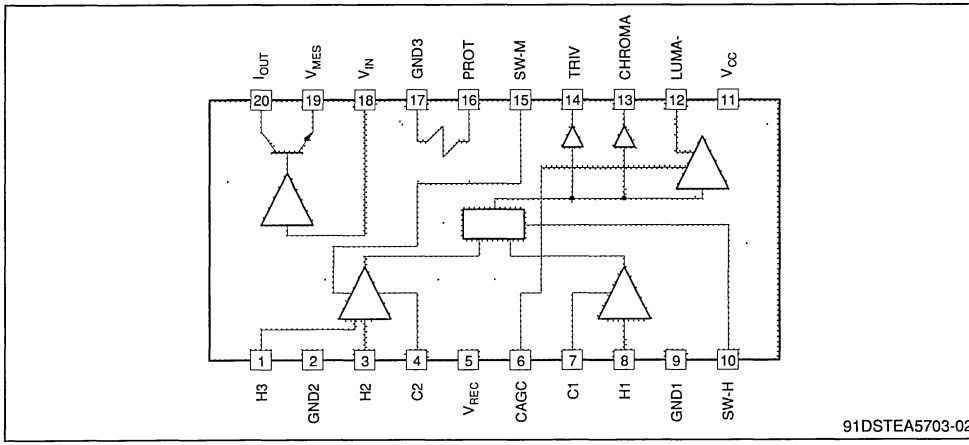
PIN DESCRIPTION



91DSTEA5703-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

TEA5703 is intended for 3 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS and S-VHS applications.

High performance technology allows very low noise levels (current and voltage). In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5703 large capability to drive directly a coaxial cable in order to reduce number of external components.

Two play-back outputs are availabe : one, dedicated to Chroma processing, is a 60dB voltage amplifier output, the other one, dedicated to Luma processing, is phase opposite signal with a constant AC output level of 200mV_{PP} at 3.8MHz signal.

A tracking information for video signal (TRIV) is Luma amplitude proportional and allows automatic phase correction.

An automatic scanning of record supply voltage permits TEA5703 automatically switching either in play-back or in record mode. The switching threshold voltage is fixed to a value which forbids high current peaking through the heads.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for the two recording heads, the DC current and the AC characteristics can be very precisely controlled with accurate external resistors. If recommended resistances are used, a ± 5% transconductance accuracy is guaranteed.

Against short circuit on the recording transconductance components, the recording amplifier includes an overheating protection system for the IC and the application board.

TEA5703 is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	6	V
V_{REC}	Power Supply Voltage Record	15	V
T_J	Junction Temperature	150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance (Typ.)	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Power Consumption

Parameter		Play-Back		Record (1)	
		Typ.	Max.	Typ.	Max.
V_{CC}		40mA	50mA	30mA	40mA
V_{REC}		0mA	0mA	30mA	40mA
Total Consumption	V_{CC} = 5, V_{REC} = 10	200mW		420mW	
	V_{CC} = 5.25, V_{REC} = 10.5		262.5mW		590mW

Notes : 1. R1 = 10Ω

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA, LUMA-.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current		30	40	50	mA
V_{CC}	Supply Voltage		4.75	5	5.25	V
CHROMA OUTPUT (no AGC)						
G_{PB}	Pre-amplification Gain	Sinus wave 600 kHz 400mV$_{PP}$ on output Input on Pin H1, H2 or H3	57	60	63	dB
ΔG_{PB}	Gain Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2	Sinus wave 3.8MHz 0.4mV$_{PP}$ on inputs H1, H2 or H3			1.2	dB
e_N	Equivalent Input Voltage Noise Level	Input grounded via switching transistor on Pins H1, H2, H3		0.45	0.55	nV/√Hz
i_N	Equivalent Input Current Noise	Pins H1, H2, H3		2.6	4	pA/√Hz
CRT	Crosstalk	Sinus wave 3.8MHz 400µV$_{PP}$, All switches combinated			-40	dB
F_{LCPB} F_{HCPB}	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, 0dB at 600kHz Low High	 8		 0.1	 MHz MHz
C_{IN}	Input Capacitance Pins H1, H2,H3			40	65	pF
R_{IN}	Pre-amplifier Input Resistance Pins H1, H2, H3		400	600	900	Ω
Z_{CPB}	Output Impedance	Sinus wave 1MHz 400µV$_{PP}$ on input		30	50	Ω
V_{DCPB1}	DC Level			1.5		V
ΔV_{DC}	Head Switch Offset				50	mV
SH_{PB1}	Second Harmonic	Sinus wave 3.8MHz 400µV$_{PP}$ on input with load resistor 500Ω/100pF			-40	dB
LUMA- OUTPUT (with AGC)						
Z_{LPB}	Output Impedance	Sinus wave 1MHz 400µV$_{PP}$ on input		30	50	Ω
V_{DCPB2}	DC Level			1.5		V
V_{LPB}	Output Amplitude	Input signal 200µV$_{PP}$ at 3.8MHz on Pins H1, H2, H3	140	200	270	mV$_{PP}$
ΔV_{LPB}	AGC Control Sensitivity	Input signal 200µV$_{PP}$ at +6dB or -5dB on Pins H1, H2, H3	-2		+1	dB
SH_{PB2}	Second Harmonic Play-back Output	Input Signal 3.8MHz 400µV$_{PP}$ on Pins H1, H2, H3		-40		dB

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA, LUMA-.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LUMA- OUTPUT (with AGC) (continued)						
I+	Positive Output Current on Pin CAGC	Input Signal 3.8MHz 200µV_{PP} on H1, 1V on Pin CAGC	15	30	45	µA
I-	Negative Output Current on Pin CAGC	Input Signal 3.8MHz 200µV_{PP} on H1, 3.5V on Pin CAGC	-45	-30	-15	µA
	Input Capacitance on Pin CAGC		4.7			nF
TRIV						
R_{TRIV}	Downloading Resistance		20	40	80	kΩ
V_{TRIV1} V_{TRIV2} V_{TRIV3} V_{TRIV4}	Output Level	V_{CHROMA} = 0mV_{PP} V_{CHROMA} = 100mV_{PP} V_{CHROMA} = 400mV_{PP} V_{CHROMA} = 600mV_{PP}	0.2	0.4 1.6 3.5	 4.5	V V V V
G_{TRIV1} G_{TRIV2}	Gain	V_{CHROMA} = 300, 400mV_{PP} V_{CHROMA} = 50, 100mV_{PP}		3 12		V/V_{PP} V/V_{PP}

Record Mode

V_{REC} = 10V, V_{CC} = 5V, Load resistor 100Ω on Pin I_{OUT}

Transconductance network defined by : R1 = 10Ω 1% Pins PROT/V_{MES}
R2 = 1kΩ 1% Pins V_{MES}/V_{IN}
R3 = 750Ω 1% Pins V_{IN}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{REC} I_{CC2}	Current Supply	V_{REC} = 10V V_{CC} = 5V		30 30	40 40	mA mA
I_{OUT}						
I_{max}	Max. Record Current	3.8MHz	35			mA_{PP}
TR	Transconductance	V_{IN} = 300mV_{PP}		90		mA/V
SH_{REC}	Second Harmonic	Output Current 30mA_{PP} at 3.8MHz		-43	-38	dB
F_{LCREC} F_{HCREC}	Bandwidth Cut-off Frequency	-3dB attenuation Output current 30mA_{PP} Low High	 8		 0.1	 MHz MHz
	Output Resistance		7			kΩ
	Maximum Input Current on Pin PROT	5V on Pin PROT	150	250	400	mA
	Maximum Saturation Voltage on Pin PROT	Input current 50mA		100	150	mV
	Input Resistance	Equivalent value of R3 resistor		700		Ω

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SWH1}	Head Selection Pin SW-H	Head number 1	2.4		V_{CC}	V
V_{SWL1}		Head number 2	0		1.5	V
V_{SWH2}	Head Selection Pin SW-M	Head number 2 or 1	2.4		V_{CC}	V
V_{SWL2}		Head number 3	0		1.5	V

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Selection Pin SW-H Transient Response	Delay time selection ON (output signal appears on Pin CHROMA)		250	500	ns
t_{OFF}		Delay time selection OFF (output signal disappears on Pin CHROMA)		250	500	ns
t_{H2}	Selection Pin SW-M Transient Response	Delay time H2 selection (output signal appears on Pin CHROMA)			10	ms
t_{H3}		Delay time H3 selection (output signal appears on Pin CHROMA)			10	ms
V_{TH1}	Inhibition Threshold for Switching from Play-back to record on Pin V_{REC}	V_{CC} = 5V	0.15	0.3	0.5	V
V_{TH2}	Inhibition Threshold Hysteresis for Switching from Record to Play-back on Pin V_{REC}	V_{CC} = 5V		80		mV
t_1	Transient Response of Record Scanning on Pin V_{REC}	Delay from play-back to record (signal disappears on Pin CHROMA)		30		µs
t_2		Delay from record to play-back (signal appears on Pin CHROMA)		2*		ms
t_3		Delay from play-back to record (signal appears on Pin I_{OUT})		0.2		ms
t_4		Delay from record to play-back (signal disappears on Pin I_{OUT})		4*		ms

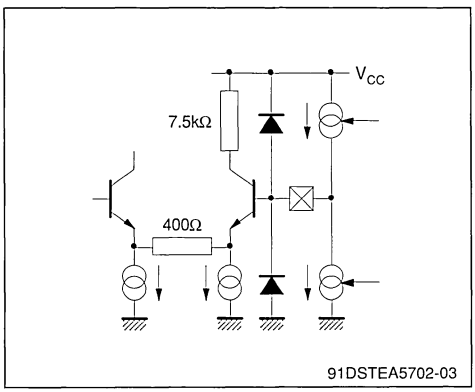
* Depending on capacitance on Pin V_{REC}

Power Supply

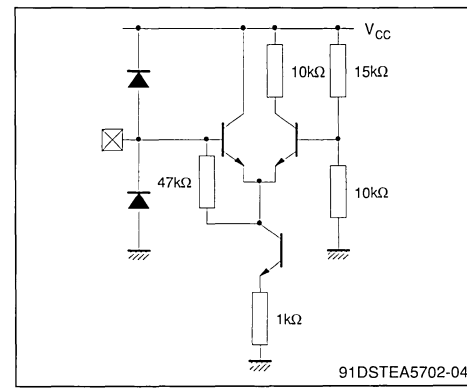
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Positive Supply Voltage Pin V_{CC}		4.75	5	5.25	V
V_{REC}	Record Voltage Pin V_{REC}		4.75	10	11	V
SVR	Supply Voltage Rejection	0.5mV$_{PP}$ on Pin V_{CC} 75µV$_{PP}$ on Pin H1, H2,H3 Measurement on Pin Chroma	15	20		dB

INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

Pins : C1, C2

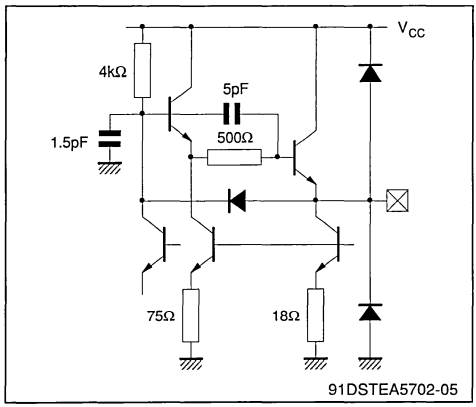


Pin : SW-H, SW-M

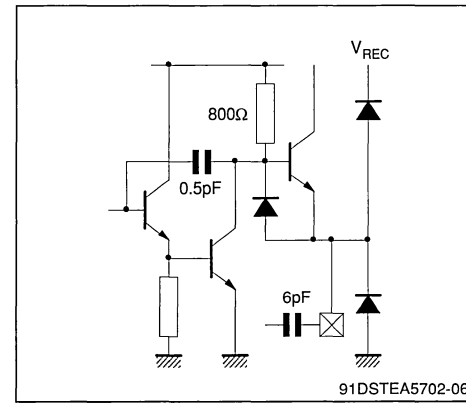


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

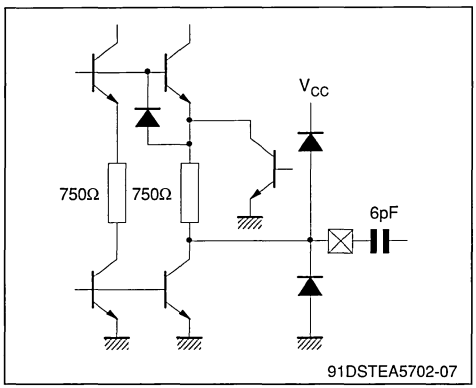
Pins : Chroma, Luma-



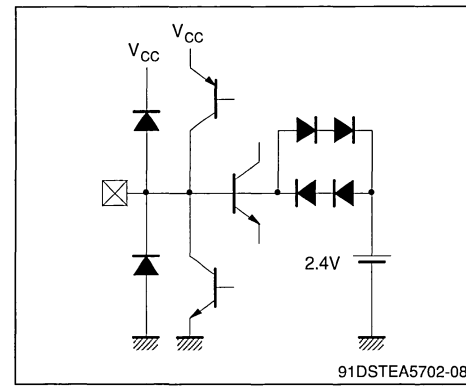
Pin : V_{MES}



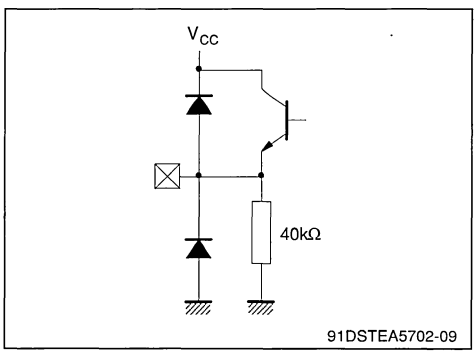
Pin : V_{IN}



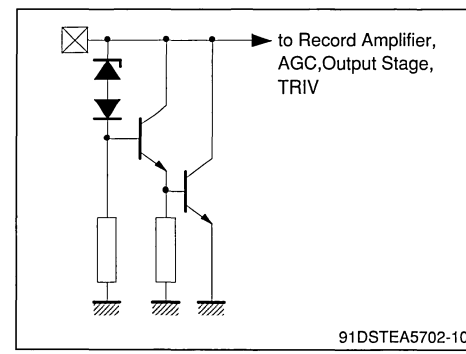
Pin : CAGC



Pin : TRIV

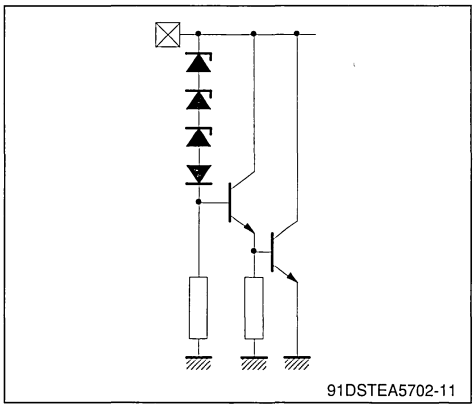


Pin : V_{CC1}

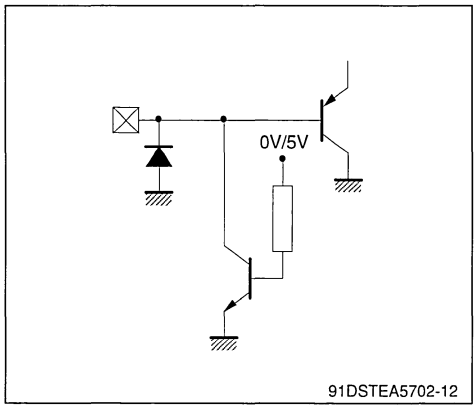


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

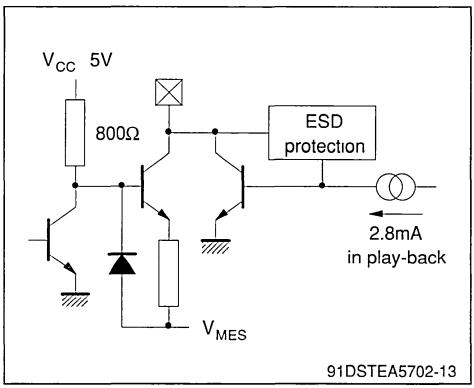
Pin : V_{REC}



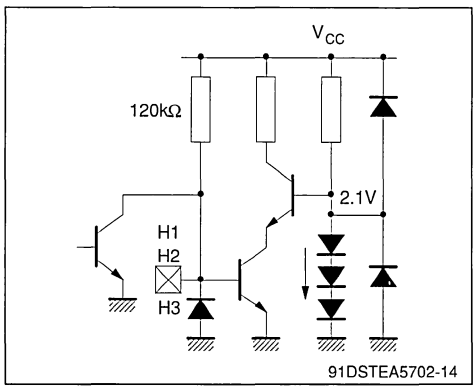
Pin : PROT



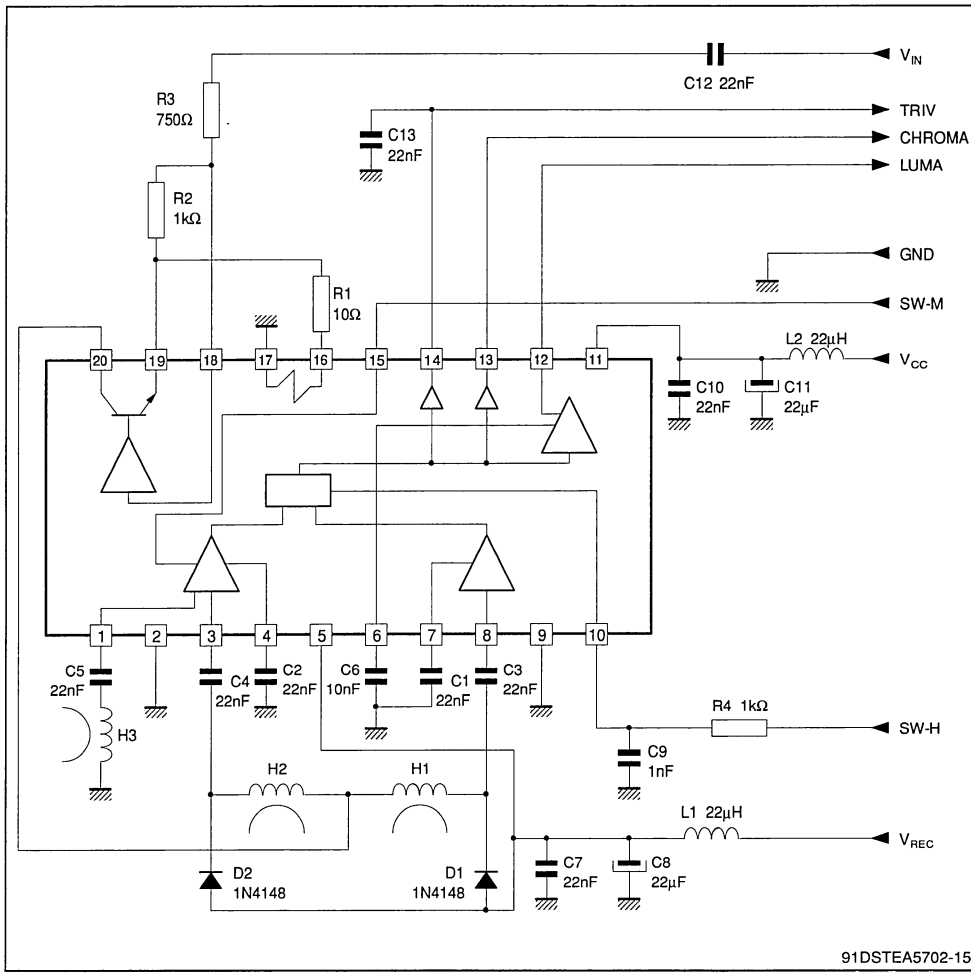
Pin : I_{OUT}



Pins : H1, H2, H3

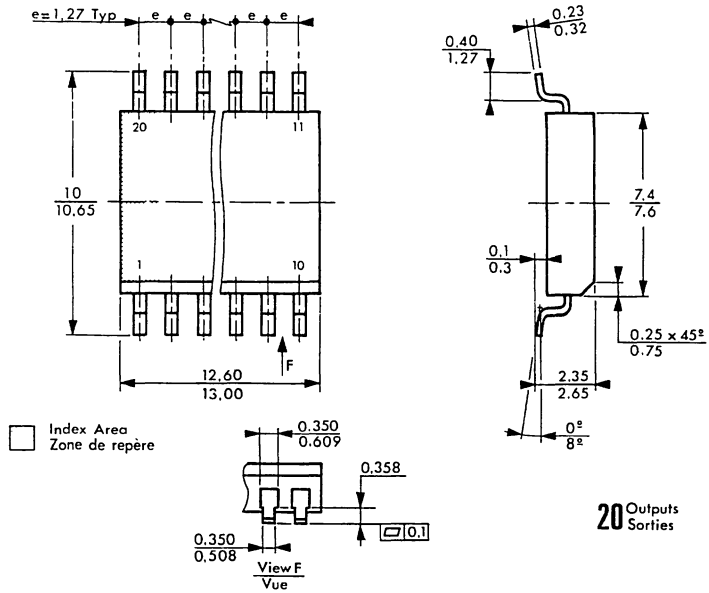


APPLICATION DIAGRAM



PACKAGE MECHANICAL DATA

20 PINS - PLASTIC MICROPACKAGE



SGS-THOMSON MICROELECTRONICS

TEA5704

ADVANCED 4-HEAD PLAY-BACK AND RECORD AMPLIFIER FOR VCR

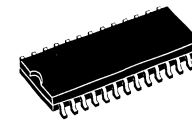
ADVANCE DATA

PLAY-BACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 4 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAY-BACK OUTPUT WITHOUT AGC
- TWO PLAY-BACK OUTPUTS INCLUDING AGC (PHASE AND OPPOSITE PHASE)
- RECORD AMPLIFIER INHIBITION AND RECORD OUTPUT GROUNDED
- OUTPUT FOR TRACKING VIDEO INFORMATION (TRIV)
- SHORT PLAY/LONG PLAY ENVELOPE COMPARATOR

RECORD MODE

- TWO INTEGRATED I/I CONVERTERS WITH ACCURATE CONTROL OF TRANSCONDUCTANCE
- AUTOMATIC PLAY-BACK/RECORD SWITCHING BY SCANNING OF RECORD SUPPLY
- PLAY-BACK LOOP INHIBITION
- RECORD AMPLIFIERS WITH AUTOMATIC PROTECTION AGAINST SHORT CIRCUIT



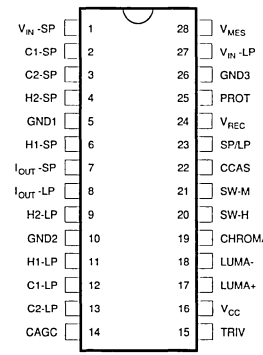
SO28
(Plastic Micropackage)

ORDER CODE : TEA5704

DESCRIPTION

The TEA5704 is an advanced four head record and play-back amplifier for VCR.

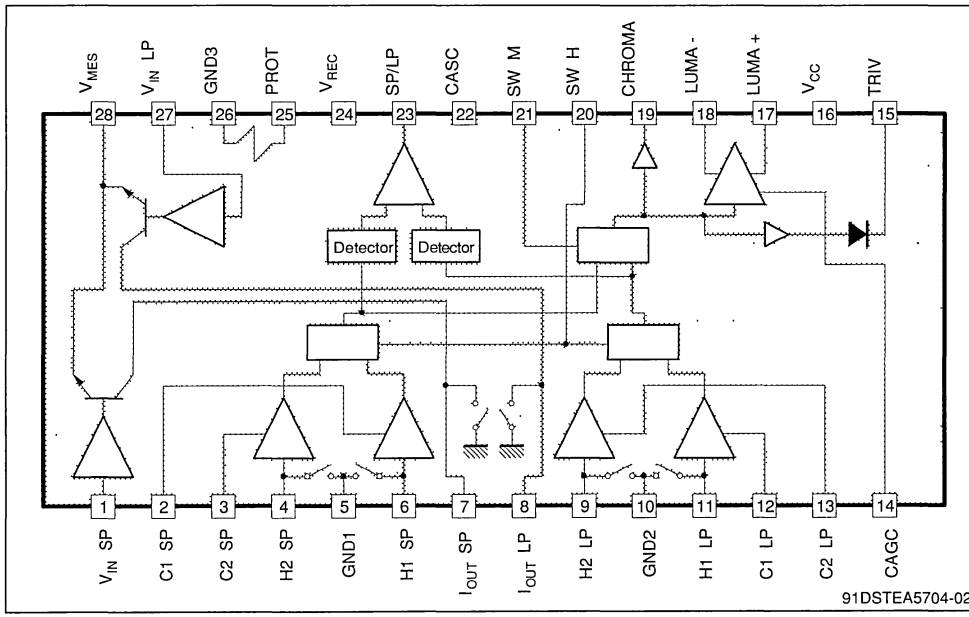
PIN DESCRIPTION



91DSTEA5704-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

TEA5704 is intended for 4 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS and S-VHS applications (10MHz bandwidth).

High performance technology allows very low noise levels (current and voltage), which are frequency dependant in all the frequency range. In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5704 large capability to drive directly a coaxial cable in order to reduce number of external components.

Three play-back outputs are availabe : one, dedicated to Chroma processing, is a 60dB voltage amplifier output, the two others, dedicated to Luma processing, are phase opposite signals with a constant AC output level of 200mV_{PP} at 3.8MHz signal.

A tracking information for video signal (TRIV) is Luma amplitude proportional and allows automatic phase correction.

An automatic scanning of record supply voltage permits TEA5704 automatically switching either in play-back or in record mode. The switching threshold voltage is fixed to a value which forbids high current peaking through the heads.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for two recording heads, the DC current and the AC characteristics can be very precisely controlled with accurate external resistors. If recommended resistances are used, a ± 5% transconductance accuracy is guaranteed.

Feedback loop gains of SP channel and LP channel can be different.

The recording amplifiers include a protection system which protexts the IC and the application board against overheating in case of short circuit on the recording transconductance components.

A particular feature is the SP/LP envelope comparator and detector. This system can be used in search mode, still mode, slow mode... The output signal is an output current feeding a capacitor. When the input signals are too low, the output is forced high (corresponding to SP Signal amplitude greater than the LP one) by an hysteresys comparator. This output is high in record mode.

TEA5704 is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	6	V
V_{REC}	Power Supply Voltage Record	15	V
T_J	Junction Temperature	+150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance (Typ.)	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Power Consumption

Parameter		Play-Back		Record (1)	
		Typ.	Max.	Typ.	Max.
V_{CC}		50mA	65mA	35mA	45mA
V_{REC}		0mA	0mA	45mA	55mA
Total Consumption (2)	V_{CC} = 5V, V_{REC} = 9V	250mW		535mW	
	V_{CC} = 5.25V, V_{REC} = 9.45V		340mW		700mW

Notes : 1. R1 = 5.6Ω
2. Taking in account only the consumption through the IC
A great care should be taken to the maximum power consumption : V_{REC} can be increased to 12.6V if the DC current flowing through the head is reduced. This can be done by increasing R1 value. V_{REC} can be reduced as long as voltage on Pins I_{OUT}-SP, I_{OUT}-LP is not going under 1V (to forbid output stage saturation).

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA, LUMA+, LUMA-.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current		40	50	65	mA
V_{CC}	Supply Voltage		4.75	5	5.25	V
CHROMA OUTPUT (no AGC)						
G_{PB}	Pre-amplification Gain	Sinus wave 600 kHz 400mV$_{PP}$ on output Input on Pin H1-SP or H2-SP, H1-LP or H2-LP	57	60	63	dB
ΔG_{PB1}	Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2 in SP Mode	Sinus wave 600kHz 0.4mV$_{PP}$ on inputs H1-SP and H2-SP			1.2	dB
ΔG_{PB2}	Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2 in LP Mode	Sinus wave 600kHz 0.4mV$_{PP}$ on inputs H1-LP and H2-LP			1.2	dB
e_N	Equivalent Input Voltage Noise Level (see note)	Input grounded via switching transistor on Pins H1-SP, H2-SP, H1-LP, H2-LP, F = 600kHz		0.6		nV/√Hz
i_N	Equivalent Input Current Noise	Pins H1-SP, H2-SP, H1-LP, H2-LP		2		pA/√Hz
CRT	Crosstalk	Sinus wave 3.8MHz 400µV$_{PP}$, All switches combinated			-40	dB
F_{LCPB1} F_{HCPB1}	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, 0dB at 600kHz Low High	 8		0.1	MHz MHz

Note : These values can be adjusted to the application.

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA, LUMA+, LUMA-.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CHROMA OUTPUT (no AGC) (continued)						
C_{IN}	Input Capacitance Pins H1-SP, H2-SP, H1-LP, H2-LP	At 5MHz		30	40	pF
R_{IN}	Pre-amplifier Input Resistance Pins H1-SP, H2-SP, H1-LP, H2-LP	At 3.8MHz	400	600	900	Ω
Z_{CPB}	Output ImpedancePin CHROMA	Sinus wave 600kHz 400µV_{PP} on input		30	50	Ω
V_{DCPB1}	DC Level at Play-back Output on Pin CHROMA			1.4		V
ΔV_{DC}	Head Switch Offset Pin CHROMA	All combinations			50	mV
SH_{PB1}	Second Harmonic Play-back Output Pin CHROMA	Sinus wave 600kHz 400µV_{PP} on input with load 500Ω/100pF			-40	dB
LUMA+, LUMA- OUTPUTS (with AGC)						
Z_{LPB}	Output Impedance	Sinus wave 1MHz 400µV_{PP} on input		30	50	Ω
V_{DCPB2}	DC Level			1.6		V
F_{LCPB2} F_{HCPB2}	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, AGC locked, 0dB at 3.8MHz Low High	 10	 12	 0.1	 MHz MHz
V_{LPB}	Output Amplitude	Input signal 200µV_{PP} at 3.8MHz on Pins H1-SP, H2-SP, H1-LP, H2-LP	140	200	270	mV_{PP}
ΔV_{LPB}	AGC Control Sensitivity	Input signal 200µV_{PP} at +6dB or -5dB on Pins H1-SP, H2-SP, H1-LP, H2-LP	-2		+1	dB
SH_{PB2}	Second Harmonic Play-back Output	Input Signal 3.8MHz 400µV_{PP} on Pins H1-SP, H2-SP, H1-LP, H2-LP without and with load 500Ω/100pF		-42	-35	dB
CAGC						
I+	Positive Output Current	Input Signal 3.8MHz 200µV_{PP} on H1-SP, 1V on Pin CAGC	15	30	45	µA
I-	Negative Output Current	Input Signal 3 8MHz 200µV_{PP} on H1-SP, 3.5V on Pin CAGC	-45	-30	-15	µA
	Capacitance		4.7			nF
TRIV						
R_{TRIV}	Downloading Resistance		20	40	80	kΩ
V_{TRIV1} V_{TRIV2}	Output Level	V_{CHROMA} = 400mV_{PP} at 3.8MHz V_{CHROMA} = 100mV_{PP} at 3.8MHz		3 5 1.6		V V
G_{TRIV1} G_{TRIV2}	Gain	V_{CHROMA} = 300, 400mV_{PP} at 3.8MHz V_{CHROMA} = 50, 100mV_{PP} at 3.8MHz		3 12		V/V_{PP} V/V_{PP}
SP/LP ENVELOPE DETECTOR						
	Capacitance on Pin SP/LP			1		nF
V_{DETH} V_{DETL}	Comparator Output Voltage, SP Selected (High Level)	High Level Low Level	4		 1	V V
I_{DET+}	Current Output on Pin SP/LP	200mVPP on Pins H1-SP or H2-SP		100	150	µA
I_{DET-}	Current Output on Pin SP/LP	200mVPP on Pins H1-LP or H2-LP	-150	-100		µA
	Sensitivity 1	15 up to 600mV_{PP} on SP, LP short circuited	4			V
	Sensitivity 2	15 up to 600mV_{PP} on LP, SP short circuited			1	V

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Record Mode

V_{REC} = 9V, V_{CC} = 5V, Load resistor 50Ω on Pin I_{OUT}-SP, I_{OUT}-LP
Transconductance network defined by : R1 = 5.6Ω, 1% Pins PROT/V_{MES}
R2-SP = 2kΩ, 1% Pins V_{MES}/V_{IN}-SP
R2-LP = 1.5kΩ, 1% Pins V_{MES}/V_{IN}-SP
R3-SP = 1.5kΩ, 1% Pin V_{IN}- SP
R3-LP = 1.5kΩ, 1% Pin V_{IN}- LP

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{REC} I_{CC2}	Current Supply	V_{REC} = 9V V_{CC} = 5V		45 35	55 45	mA mA
I_{max}	Max. Record Current on SP or LP Current Amplifier	3.8MHz	70			mA_{PP}
TR	Transconductance	V_{IN}-SP = 300mV_{PP} V_{IN}-LP = 300mV_{PP}		240 180		mA/V mA/V
SH_{REC}	Second Harmonic	Output Current, 60mA_{PP} at 3.8MHz at Pin I_{OUT}-SP at Pin I_{OUT}-LP		 -43 -43	 -38 -38	 dB dB
F_{LCREC1} F_{HCREC1}	Bandwidth Cut-off Frequency Pin I_{OUT}-SP	-3dB attenuation Output current 60mA_{PP} Low High	 10		 0.1	 MHz MHz
	DC Level at Pin SP-LP		4			V
F_{LCREC2} F_{HCREC2}	Bandwidth Cut-off Frequency Pin I_{OUT}-SP	-3dB attenuation, 0dB at 3.8MHz Output current 60mA_{PP} Low High	 10		 0.1	 MHz MHz
I_{PROT}	Maximum Input Current on Pin PROT	5V on Pin V_{MES}			400	mA
V_{SAT}	Maximum Saturation Voltage on Pin V_{MES}	Input current 80mA		100	150	mV
	Input Resistance on Pins V_{IN}-LP, V_{IN}-SP	Equivalent value of R3 resistor		700		Ω

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SWHH}	Head Selection Pin SW-H	Head number 1 in SP mode, 2 in LP mode (high level)	2.4		V_{CC}	V
V_{SWHL}		Head number 2 in SP mode, 1 in LP mode (low level)	0		1.5	V
I_{SWHH}		Input current (high level)			50	µA
I_{SWHL}		Output current (low level)			50	µA
V_{SWMH}	Mode Selection Pin SW-M (Record mode and play-back mode)	LP Mode (high level)	2.4		5	V
V_{SWML}		SP mode (low level)	0		1.5	V
I_{SWMH}		Input current (high level)			50	µA
I_{SWML}		Output current (low level)			50	µA
t_{ON}	Selection Pin SW-H or SW-M Transient Response	Delay time selection ON (output signal appears on Pin CHROMA)		250	500	ns
t_{OFF}		Delay time selection OFF (output signal disappears on Pin CHROMA)		250	500	ns

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Switching Levels (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{TH1}	Inhibition Threshold for Switching from Play-back to record on Pin V_{REC}	V_{CC} = 5V	0.15	0.3	0.5	V
V_{TH2}	Inhibition Threshold Hysteresis for Switching from Record to Play-back on Pin V_{REC}	V_{CC} = 5V		80		mV
t_1	Transient Response of Record Scanning on Pin V_{REC}	Delay from play-back to record (signal disappears on Pin CHROMA)		30		µs
t_2		Delay from record to play-back (signal appears on Pin CHROMA)		2*		ms
t_3		Delay from play-back to record (signal appears on Pin I_{OUT}-SP, I_{OUT}-LP)		0.2		ms
t_4		Delay from record to play-back (signal disappears on Pin I_{OUT}-SP, I_{OUT}-LP)		4*		ms

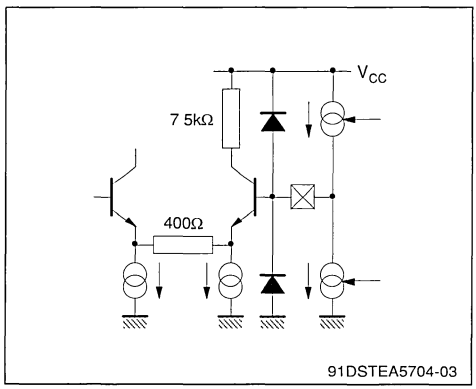
* Depending on capacitance on Pin V_{REC}.

Power Supply

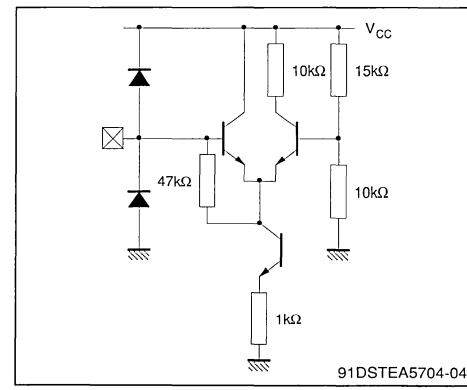
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Positive Supply Voltage Pin V_{CC}		4.75	5	5.25	V
V_{REC}	Record Voltage Pin V_{REC}		4.75	9	12.6	V
SVR	Supply Voltage Rejection	0.5mV_{PP} on Pin V_{CC} 75µV_{PP} on Pin H1-SP, H2-SP, H1-LP, H2-LP Measurement on Pin Chroma	15	20		dB

INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

Pins : C1-SP, C2-SP, C1-LP, C2-LP

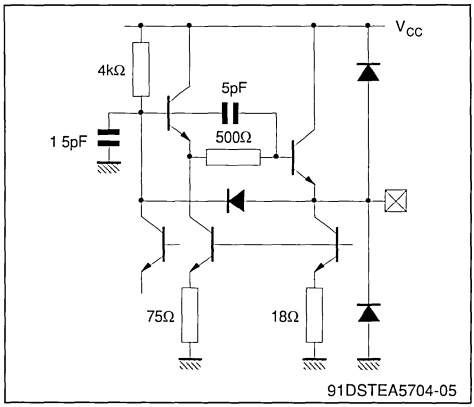


Pins : SW-H, SW-M

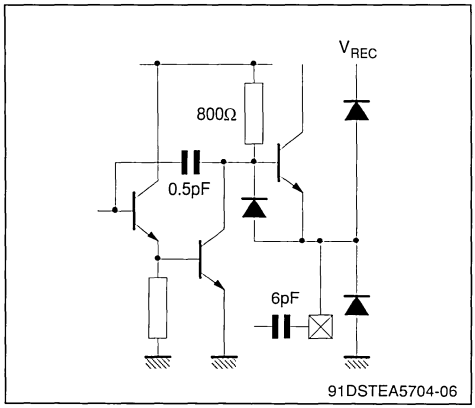


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

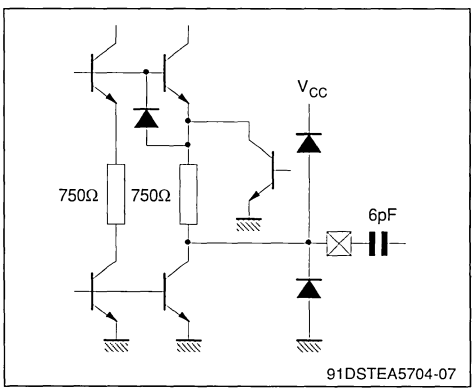
Pins : Chroma, Luma+, Luma-



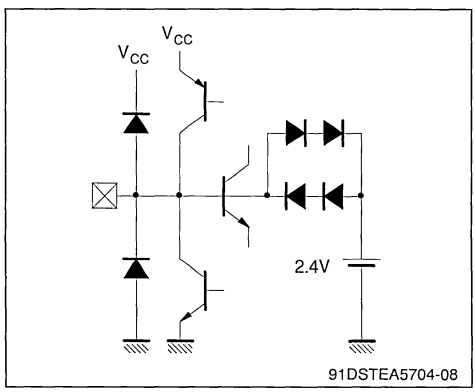
Pin : V_{MES}



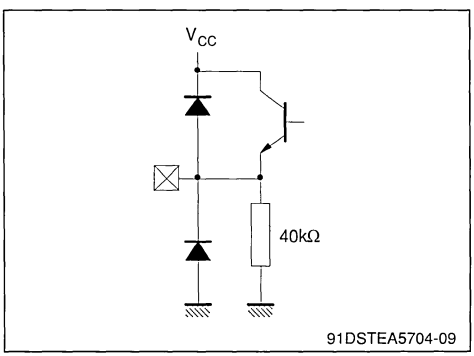
Pin : V_{IN}-SP, V_{IN}-LP



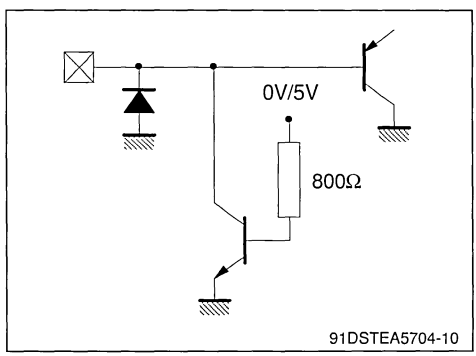
Pin : CAGC



Pin : TRIV

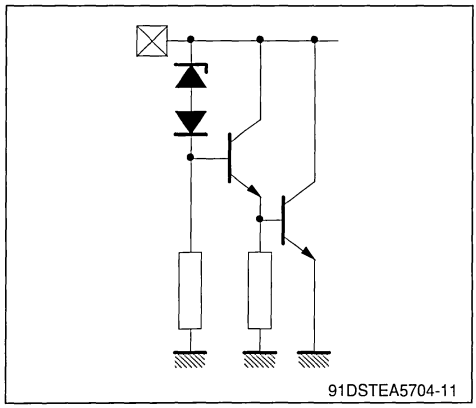


Pin : PROT

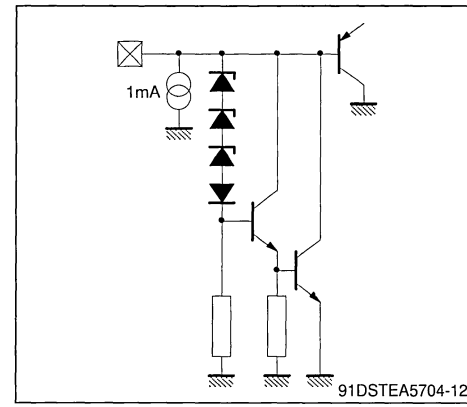


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

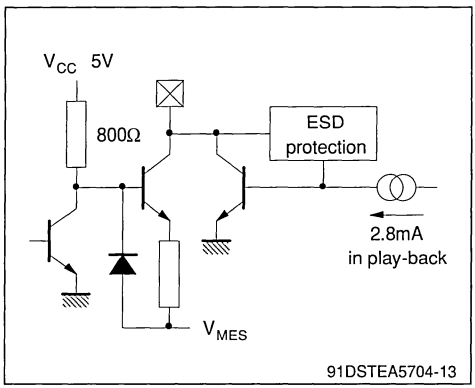
Pin : V_{CC}



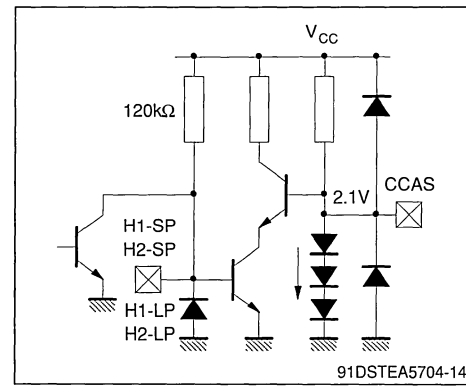
Pin : V_{REC}



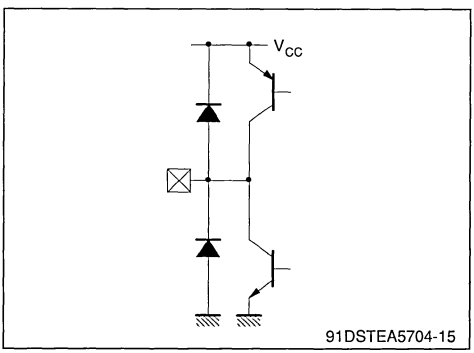
Pin : I_{OUT}-SP, I_{OUT}-LP



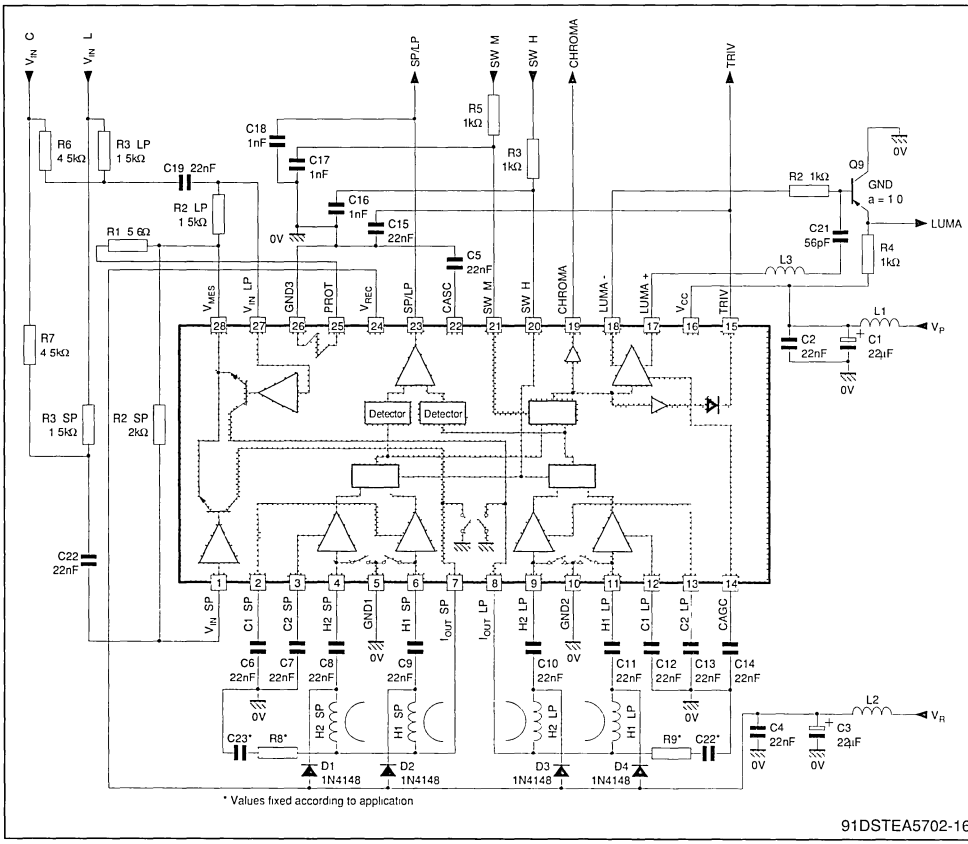
Pins : CCAS, H1-SP, H2-SP, H1-LP, H2-LP



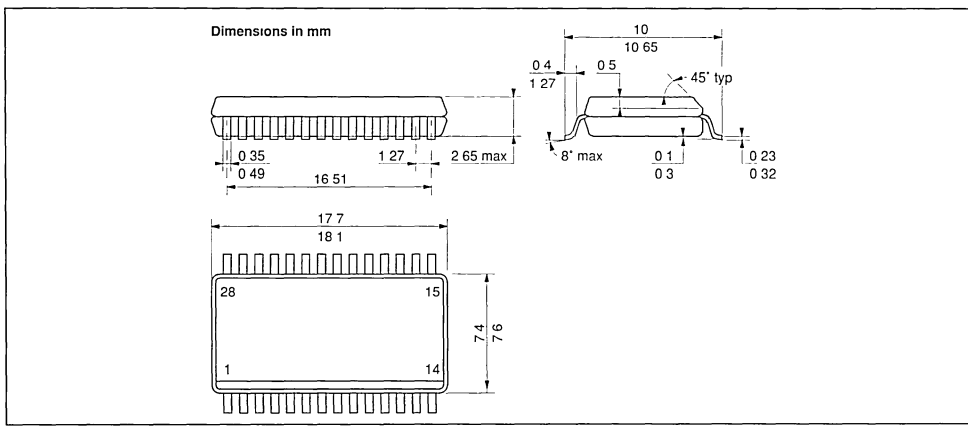
Pin : SP/LP



APPLICATION DIAGRAM



PACKAGE MECHANICAL DATA : 28 PINS - PLASTIC MICROPACKAGE



SGS-THOMSON MICROELECTRONICS

TEA5712

ADVANCED FM AUDIO PLAY-BACK AND RECORD AMPLIFIER FOR VCR

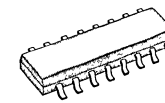
ADVANCE DATA

PLAY-BACK MODE

- LOW NOISE 70dB AMPLIFIERS FOR 2 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAY-BACK OUTPUT
- MODE SELECTION BY LOGIC INPUT

RECORD MODE

- ONE INTEGRATED I/I CONVERTER WITH ACCURATE CONTROL OF TRANSCONDUCTANCE
- RECORD AMPLIFIER WITH AUTOMATIC PROTECTION AGAINST SHORT CIRCUIT
- 5V SUPPLY VOLTAGE



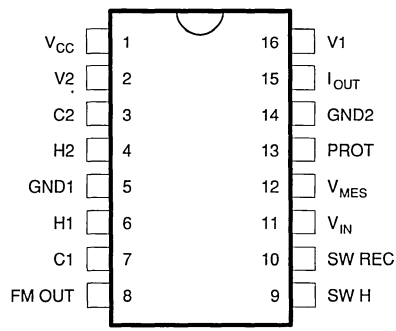
SO16J
(plastic micropackage)

ORDER CODE : TEA5712

DESCRIPTION

The TEA5712 is an advanced two head FM audio record and play-back amplifier for VCR.

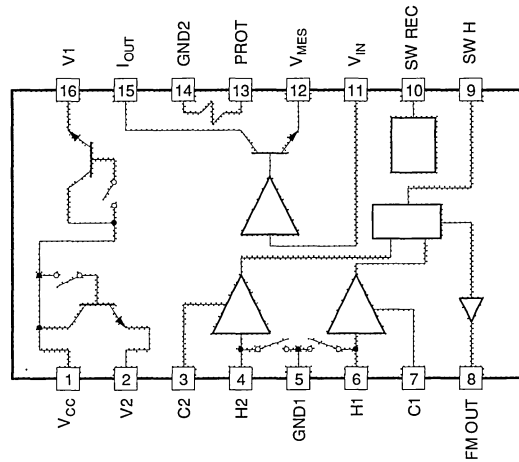
PIN DESCRIPTION



91DSTEA5712-01

This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

BLOCK DIAGRAM



91DSTEA5712-02

FUNCTIONAL DESCRIPTION

TEA5712 is intended for 2 heads FM audio VCR applications.

High performance technology allows very low noise levels (current and voltage). In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5712 large capability to directly drive a coaxial cable in order to reduce number of external components.

Only one power supply is necessary for play-back and record modes. The mode can be chosen through a logic input. A special care has been taken to avoid current peaks through the rotary transformers.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for the two heads, the DC current and the AC characteristics can be very precisely controled with accurate external resistors. If recommended resistances are used, a ±5% transconductance accuracy is guaranted.

The recording amplifier includes a protection system which protects the IC and the application board against overheating in case of short circuit on the recording transconductance components.

TEA5712 is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	6	V
T_J	Junction Temperature	+ 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance (Typ.)	100	°C/W

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Power Consumption

Parameter	Play-Back		Record (1)	
	Typ.	Max.	Typ.	Max.
V_{CC} = 5V	25mA	35mA	60mA	70mA

Note : 1. R1 = 5.6Ω

Play-back Mode

V_{CC} = 5V, no load on Pin V_{OUT}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current			25	35	mA
V_{CC}	Supply Voltage		4.75	5	5.25	V
FM OUT						
G_{PB}	Pre-amplification Gain	Sinus wave 1.6MHz 400mV$_{PP}$ on output, Input on Pin H1 or H2	65	70	75	dB
ΔG_{PB}	Gain Difference of Output Signal on Pin FM OUT between Channel 1 and Channel 2	Sinus wave 1.6MHz 0.1mV$_{PP}$ on inputs H1 or H2			1.2	dB
e_N	Equivalent Input Voltage Noise Level	Input grounded via switching transistor on Pins H1, H2		0.34		nV/√Hz
i_N	Equivalent Input Current Noise	Pins H1, H2		3.6		pA/√Hz
CRT	Crosstalk	Sinus wave 1.6MHz 100µV$_{PP}$, All switches combinated			-40	dB
F_{LCPB} F_{HCPB}	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input Low High	 5		 0.1	 MHz MHz
C_{IN}	Input Capacitance Pins H1, H2			45	60	pF
R_{IN}	Pre-amplifier Input Resistance Pins H1, H2	At 1.6MHz		600	1200	Ω
Z_{PB}	Output Impedance	Sinus wave 1.6MHz 100µV$_{PP}$ on input		30	50	Ω
V_{DCPB1}	DC Level			2.5		V
ΔV_{DC}	Head Switch Offset				150	mV
SH_{PB1}	Second Harmonic	Sinus wave 1.6MHz 100µV$_{PP}$ on input with load 500Ω/100pF			-40	dB

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Record Mode

V_{CC} = 5V, Load resistor 50Ω on Pin I_{OUT}

Transconductance network defined by : R1 = 5.6Ω 1% Pins PROT/V_{MES}
R2 = 1kΩ 1% Pins V_{MES}/V_{IN}
R3 = 750Ω 1% Pins V_{IN}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC2}	Current Supply	V_{CC} = 5V		60	70	mA
I_{OUT}						
I_{max}	Max. Record Current	1.6MHz	60			mA_{PP}
TR	Transconductance	V_{IN} = 200mV_{PP}		220		mA/V
Z_{OUT}	Output Resistance		7			kΩ
SH_{REC}	Second Harmonic	Output Current 40mA_{PP} at 1.6MHz		-43	-38	dB
F_{LCREC} F_{HCREC}	Bandwidth Cut-off Frequency	-3dB attenuation Output current 60mA_{PP} Low High	 5		 0.1	 MHz MHz
	Maximum Input Current on Pin V_{MES}	5V on Pin V_{MES}		250	400	mA
	Maximum Saturation Voltage on Pin V_{MES}	Input current 50mA		100	150	mV
	Input Resistance	Equivalent value of R3 resistor		750		Ω

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SWH1}	Head Selection Pin SW	Head number 1 (high level)	2.4		V_{CC}	V
V_{SWL1}		Head number 2 (low level)	0		1.5	V
I_{SWH1}		Input current (high level)			50	µA
I_{SWL1}		Output current (low level)			50	µA
V_{SWH2}	Mode Selection Pin SW REC	Record mode (high level)	2.4		V_{CC}	V
V_{SWL2}		Play-back mode (low level)	0		1.5	V
I_{SWH2}		Input current (high level)			50	µA
I_{SWL2}		Output current (low level)			50	µA
t_{ON1}	Selection Pin SW Transient Response	Delay time selection ON (output signal appears on Pin FM OUT)		250	500	ns
t_{OFF1}		Delay time selection OFF (output signal disappears on Pin FM OUT)		250	500	ns
t_{ON2}	Selection Pin SW REC Transient Response	Delay time selection ON (output signal appears on Pin I_{OUT})		40		µs
t_{OFF2}		Delay time selection OFF (output signal appears on Pin FM OUT)		1.3		ms

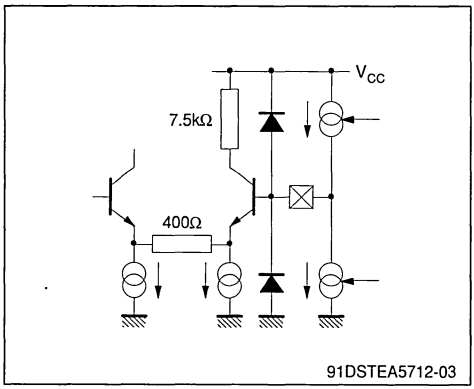
ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Power Supply

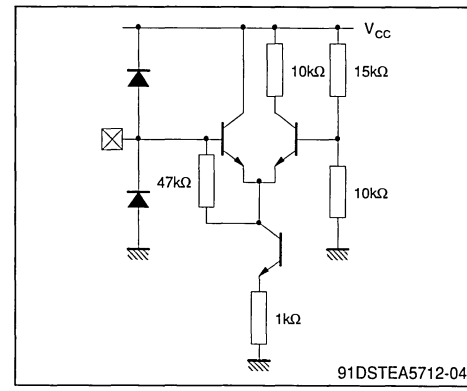
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Positive Supply Voltage Pin V_{CC}		4.75	5	5.25	V
SVR	Supply Voltage Rejection	0.5mV_{PP} on Pin V_{CC} 75µV_{PP} on Pin H1, H2 Measurement on Pin FM OUT	15	20		dB

INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

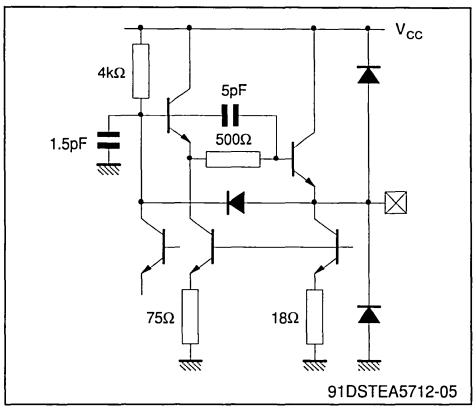
Pins : C1, C2



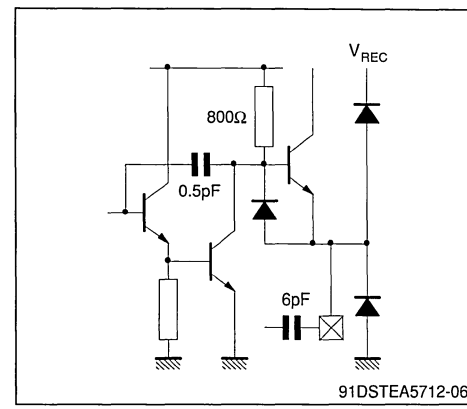
Pin : SW



Pin : FM OUT

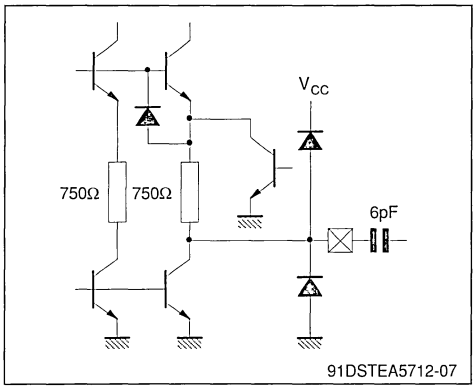


Pin : V_{MES}

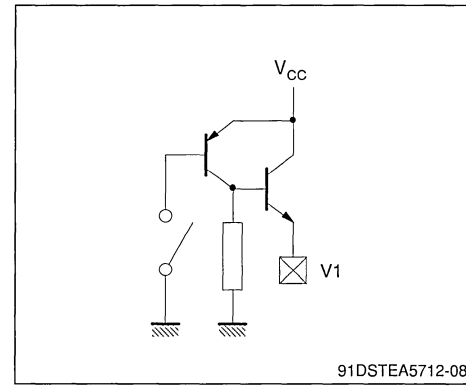


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

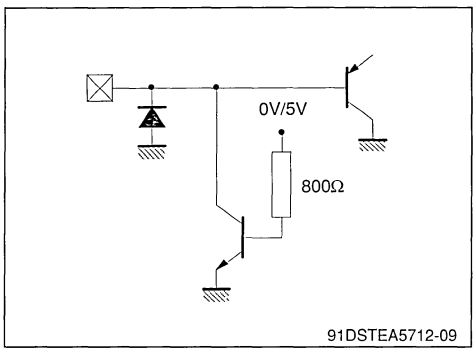
Pin : V_{IN}



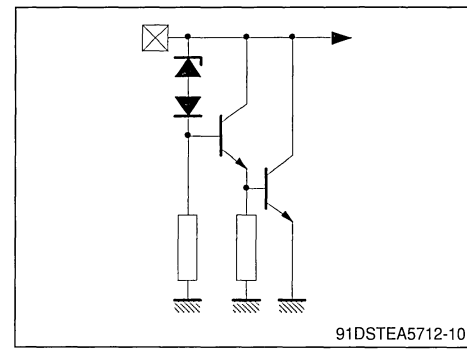
Pin s : V_1, V_2



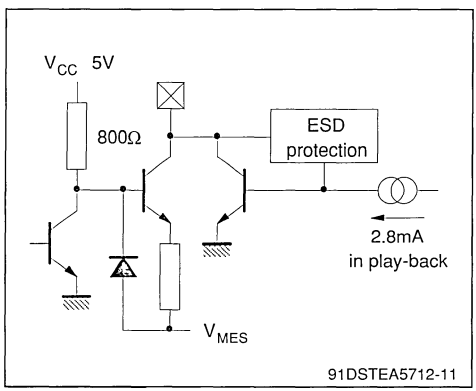
Pin : PROT



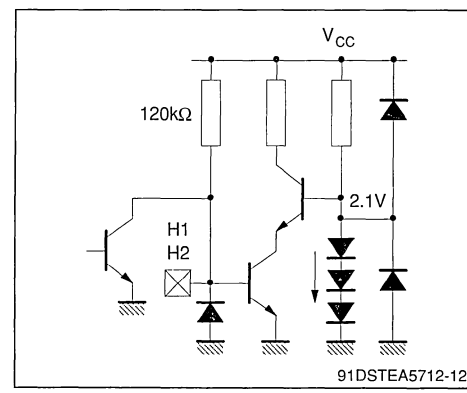
Pin : V_{CC}



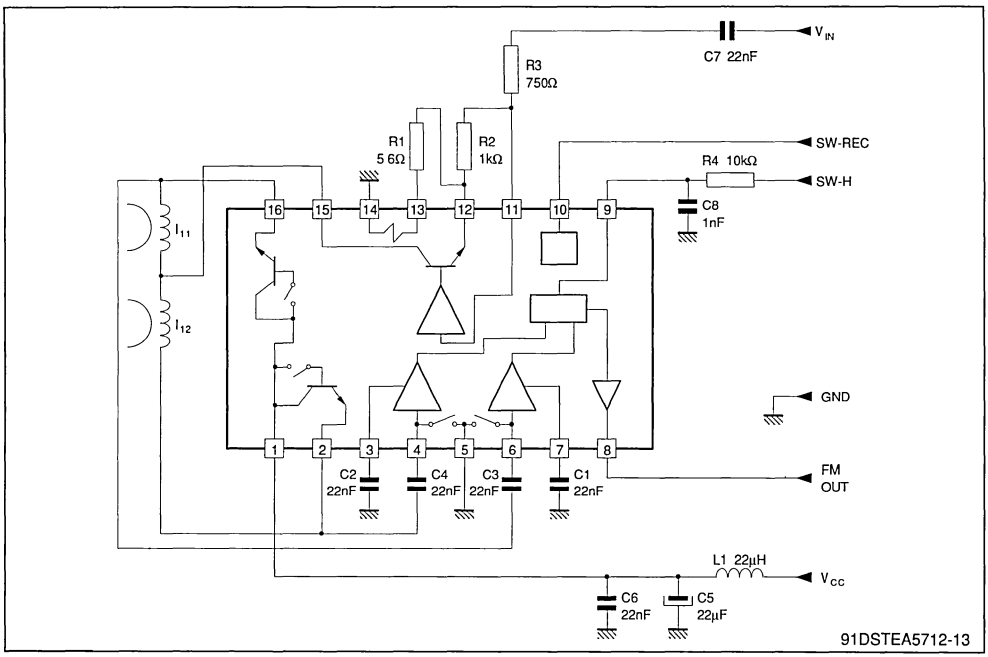
Pin : I_{OUT}



Pins : H1, H2

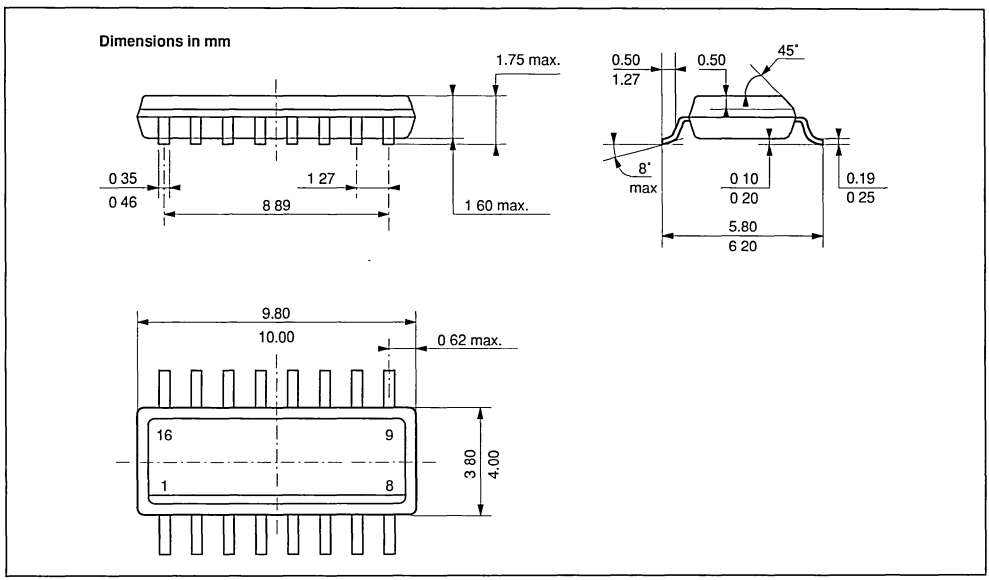


APPLICATION DIAGRAM



PACKAGE MECHANICAL DATA

16 PINS - PLASTIC MICROPACKAGE

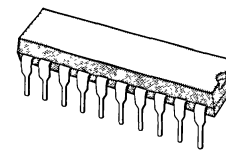


SGS-THOMSON MICROELECTRONICS

TEA6414A

BUS-CONTROLLED VIDEO MATRIX SWITCH

- 15MHz BANDWIDTH
- 8 INPUTS (CVBS, RGB, MAC, chroma...)
- 6 OUTPUTS
- POSSIBILITY OF MAC OR CHROMA SIGNAL FOR EACH INPUT BY SWITCHING-OFF THE CLAMP WITH AN EXTERNAL RESISTOR BRIDGE
- BUS CONTROLLED
- 6.5dB GAIN BETWEEN ANY INPUT AND OUTPUT
- - 50dB CROSSTALK AT 5 MHz
- FULLY PROTECTED AGAINST ESD



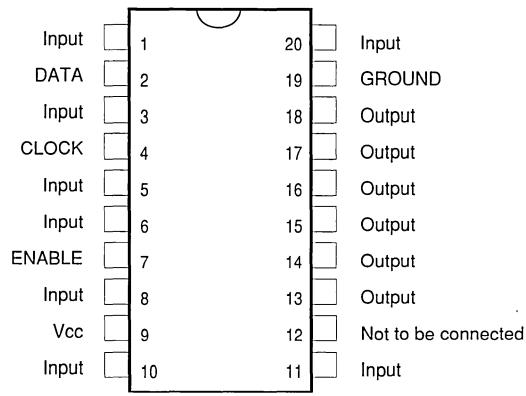
DIP20
(Plastic Package)

ORDER CODE : TEA6414A

DESCRIPTION

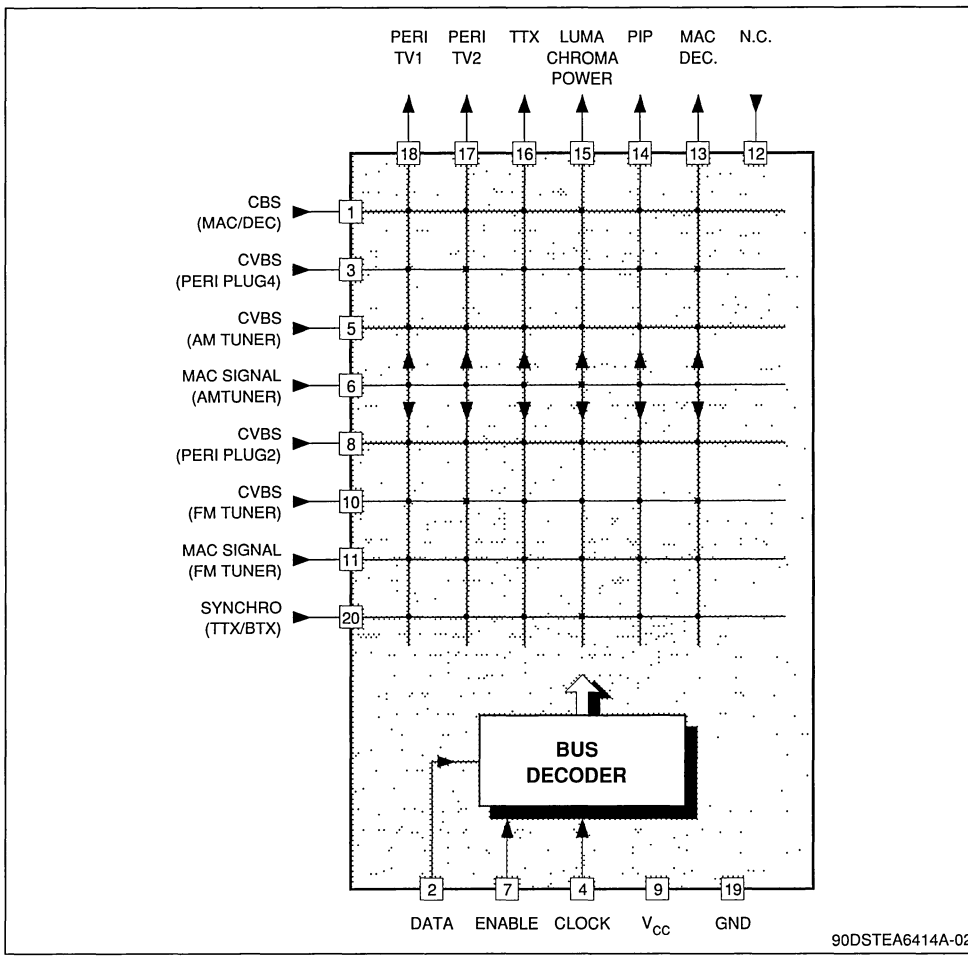
The main function of the TEA6414A is to switch 8 video input sources on the 6 outputs.
Each output can be switched to only one of the inputs whereas any same input may be connected to several outputs.
All the switching possibilities are changed through the 3-Wire Bus (THOMSON BUS).

PIN CONNECTIONS



90DSTEA6414A-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (pin 9)	13	V
T_A	Operating Ambient Temperature Range	0 to +70	°C
T_{stg}	Storage Temperature Range	-20 to +150	°C

THERMAL DATA

Symbol	Parameter	Min.	Typ.
$R_{th(j-a)}$	Junction-Ambient Thermal Resistance	80	°C/W

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 10V$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 3pF$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage (pin 9)	7	10	11	V
I_{CC}	Power Supply Current (without load on outputs ; V_{CC}=10V)	20	30	40	mA

INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Maximum Signal Amplitude (CVBS signal)	2			V_{PP}
	Input Current (per output connected, input voltage = $5V_{DC}$) (this current is X6 when all outputs are connected on the input)		1	3	µA
	DC Level	3.3	3.6	3.9	V
	DC Level Shift (temperature from 0 to 70°C)		5	100	mV

OUTPUTS (V_{IN} = $1V_{PP}$ for all dynamic tests) Pins 13-14-15-16-17-18

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Dynamic	4.5	5.5		V_{PP}
	Output Impedance		25	50	Ω
	Gain	5.5	6.5	7.5	dB
	Bandwidth (-1dB attenuation)	7	10		MHz
	Bandwidth (-3dB attenuation)		15		MHz
	Crosstalk (f = 5MHz)		-50		dB
	DC level	2.4	2.7	3	V

GENERAL DESCRIPTION

The main function of the IC is to switch 8 video input sources on 6 outputs.
Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals).
Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5 V_{DC} on the input.
Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge).
All the switching possibilities are changed through the BUS.
Driving 75Ω load needs an external transistor.
It is possible to have the same input connected to several outputs.
The starting configuration (power supply from 0 to 10V) is undetermined. In this case, 6 words of 8 bits are necessary to determine one configuration. In other case, one word of 8 bits is necessary to determine one configuration.

BUS SELECTIONS (THOMSON BUS)

ADDRESS MSB	DATA LSB	Selected Output	
00000	XXX	pin 18	Output is selected by adress bits
00100	XXX	pin 14	
00010	XXX	pin 16	
00110	- - -	Not used	
00001	XXX	pin 17	
00101	XXX	pin13	
00011	XXX	pin 15	
00111	- - -	Not used	
		Selected Input	
00XXX	000	pin 5	Input is selected by Data bits
00XXX	100	pin 8	
00XXX	010	pin 3	
00XXX	110	pin 20	
00XXX	001	pin 6	
00XXX	101	pin 10	
00XXX	011	pin 1	
00XXX	111	pin 11	

Example : 00100 101 connects pin 10 (input) to pin 14 (output).
(equals 25 hex.)

IN / OUT PIN CONFIGURATION

Figure 1 : Input Configuration.

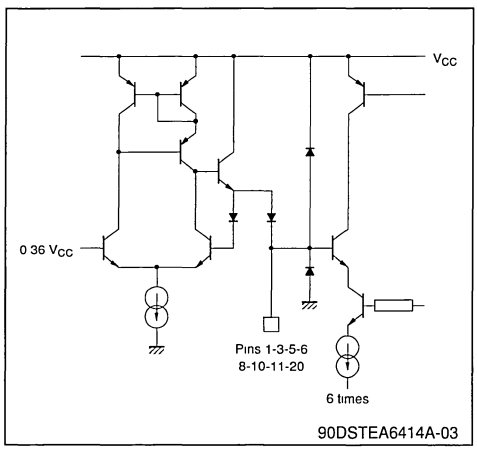
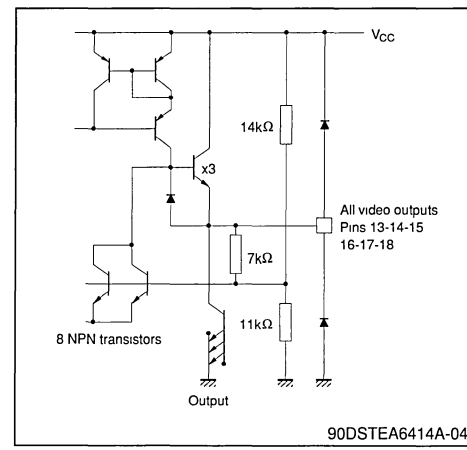


Figure 2 : Output Configuration.



IN / OUT PIN CONFIGURATION (continued)

Figure 3 : Bus I/O Configuration.

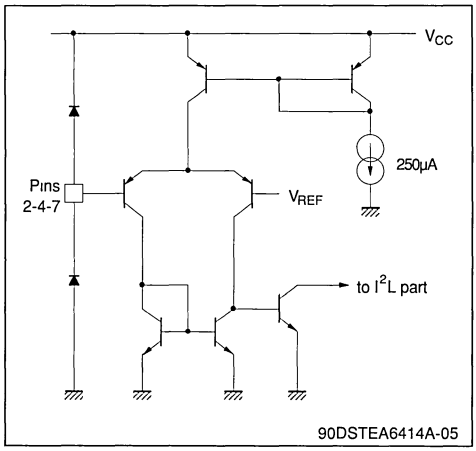
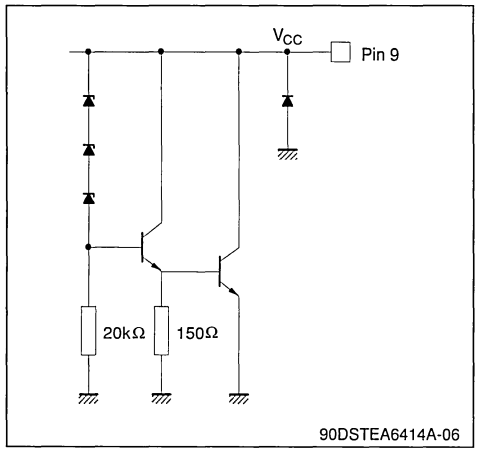
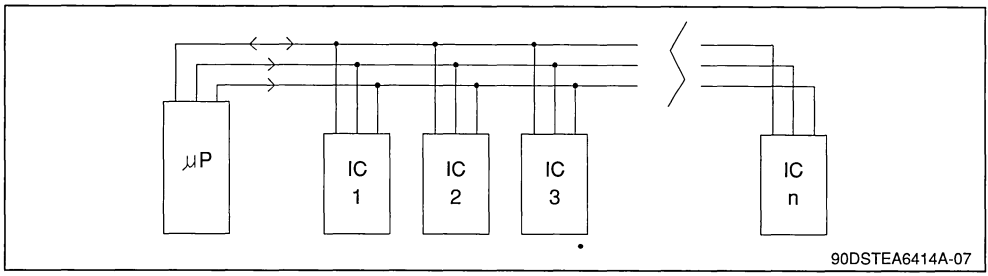


Figure 4 : V_{CC} Pin Configuration.



SPECIFICATION FOR THE THOMSON BIDIRECTIONAL DATA BUS

The bidirectional data bus has three lines (DATA, CLOCK, ENABLE) and operates serially. Transmission on the DATALINE is effected bidirectionally, whilst the ENABLE- and CLOCKLINES are driven only by the microprocessor. It is possible to select several ICs from the µP via the THOMSON BUS.



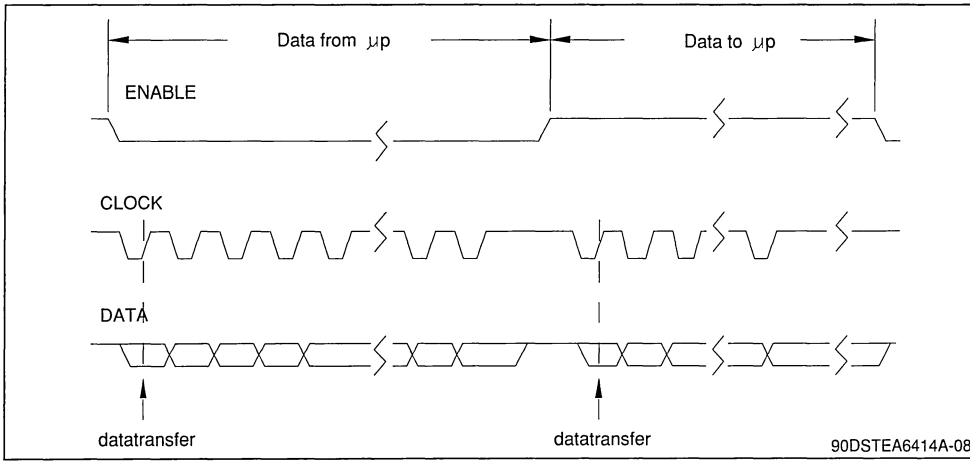
The identification or address of each particular IC is achieved by the length of the word (number of clock pulses), and each IC responds with its own particular word length. The address length is determined only while ENABLE is low, by counting the clock pulses. The rising edge of the ENABLE signal indicates the end of the address sequence.

Normally, there are several locations within the same chip, which must be selected individually, the datastream may, therefore be split into subaddress and data. In the case where an IC is not using the complete specified subaddress range it is possible to employ the unused subaddress range with a second or third IC with the same word length. The bitnumber of the subaddress is flexible.

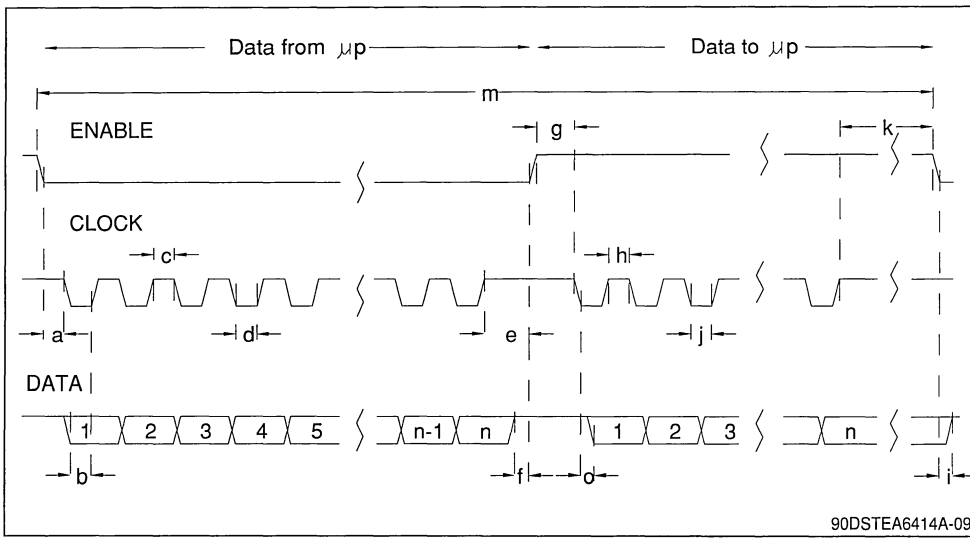
The reply word length from any of the ICs to the µP is also flexible. This bidirectional transmission is possible from the last addressed IC after the positive going edge of the ENABLE signal if the ENABLE signal remains high and the CLOCK impulses are present on the line. The µP in effect clocks out the data from the chip. When an IC is able to send information in the bidirectional way, the µP decides whether to take all information, to suppress completely the information or to stop the transfer after any bit.

This reply word, synchronized to the clock from µP, is sent only once. Should a subsequent clock impulse be present on the clock line, it will switch the IC in question to high impedance.

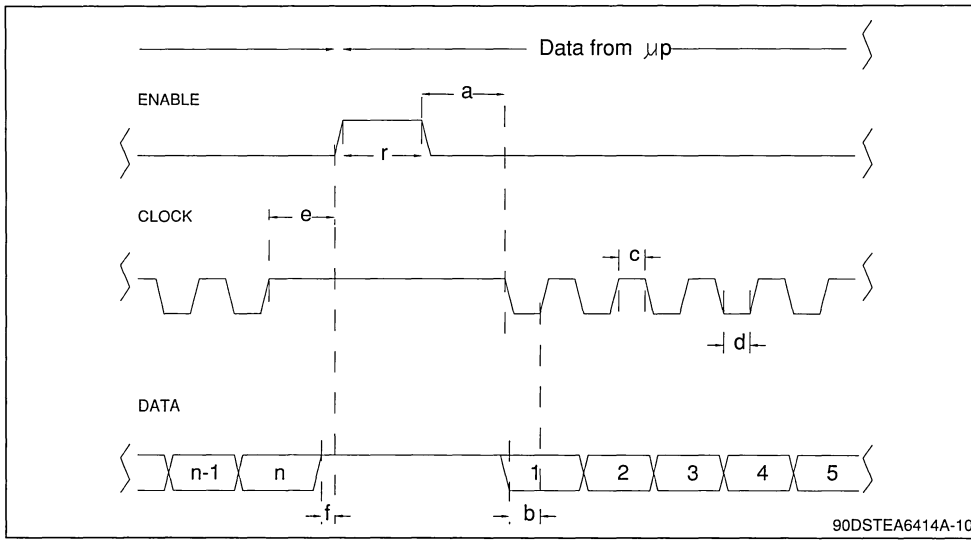
The register, from which the bidirectional information comes, is addressed with the IC address. When more than one bidirectional register exists, the selection is made by the previously selected subaddress.



TIMING DIAGRAMS



TIMING DIAGRAMS (continued)



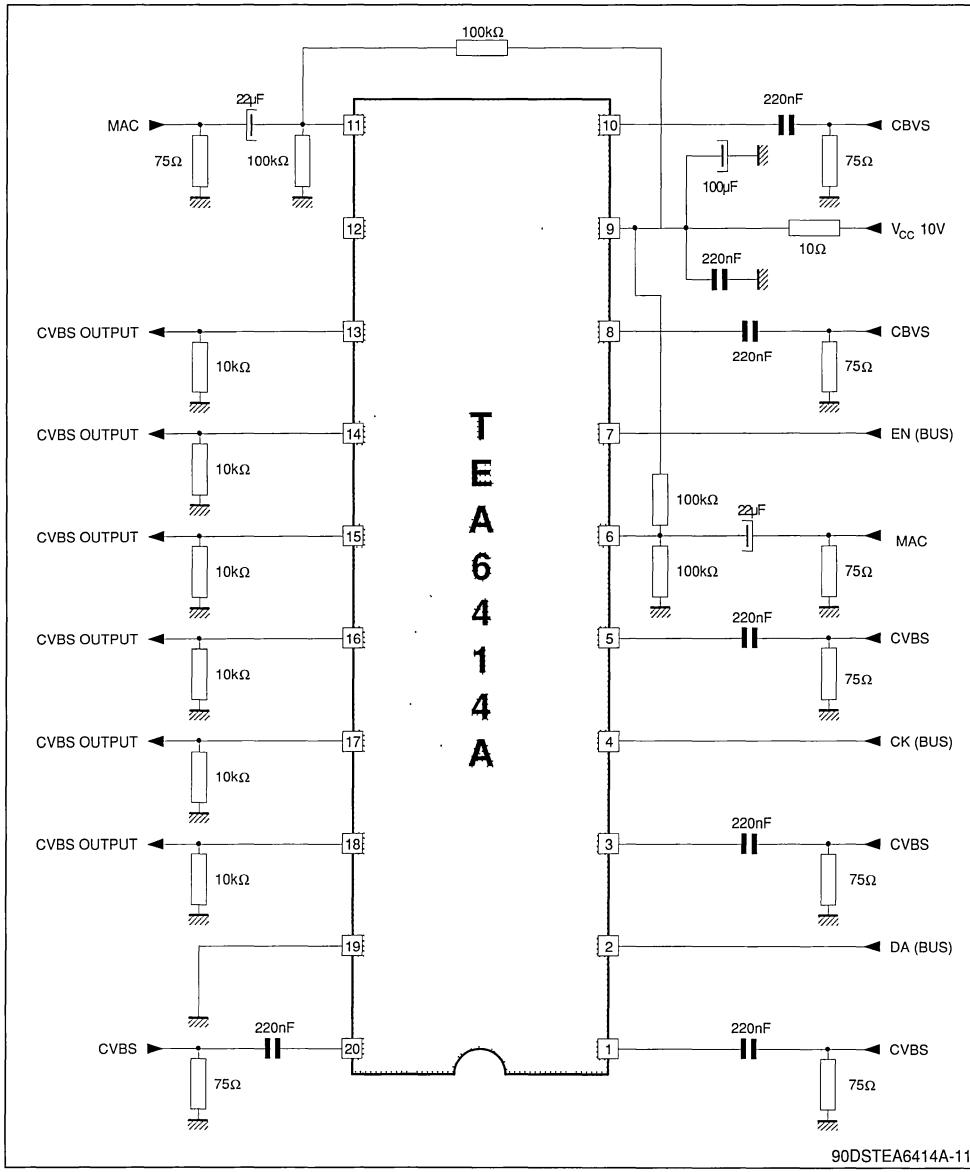
TIMING FOR THOMSON BUS

Parameter	Min.	Typ.	Max.	Unit.
a	1			µs
b	1			µs
c	1			µs
d	1			µs
e	2			µs
f	1			µs
r	2			µs

BUS INPUTS (pin 2, 4 and 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
	High Level	3.5			V
	Low Level			1	V
	Input Current ● $0.4V < V_{IN} < 1V$ ● $V_{IN} > 3.5V$	-35	-13 0	0 2	µA

TYPICAL APPLICATION



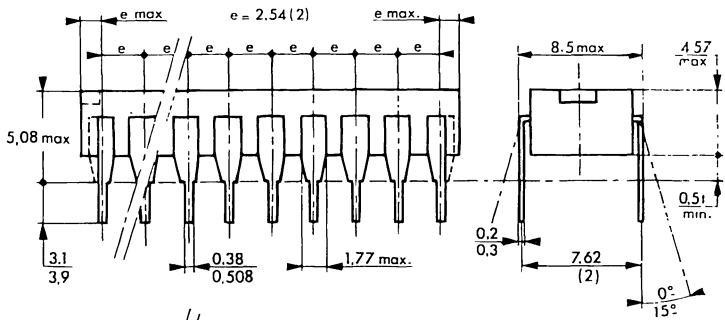
CROSSTALK IMPROVEMENT

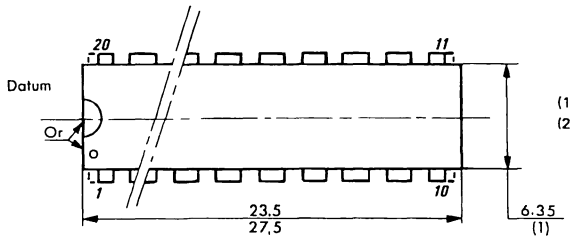
1 - When any input is not used, it must be bypassed to ground through a 220nF capacitor.

2 - An important improvement can be achieved considering the input crosstalk by means of the application (refer to technical note).

PACKAGE MECHANICAL DATA

20 PINS – PLASTIC DIP



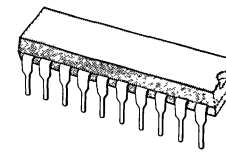


(1) Nominal dimension
(2) True geometrical position

20 Pins

BUS-CONTROLLED VIDEO MATRIX SWITCH

- 15MHz BANDWIDTH
- CASCADABLE WITH ANOTHER TEA6415B (INTERNAL ADDRESS CAN BE CHANGED BY PIN 7 VOLTAGE)
- 8 INPUTS (CVBS, RGB, MAC, CHROMA...)
- 6 OUTPUTS
- POSSIBILITY OF MAC OR CHROMA SIGNAL FOR EACH INPUT BY SWITCHING-OFF THE CLAMP WITH AN EXTERNAL RESISTOR BRIDGE
- BUS CONTROLLED
- 6.5dB GAIN BETWEEN ANY INPUT AND OUTPUT
- - 50dB CROSSTALK AT 5 MHz
- FULLY ESD PROTECTED



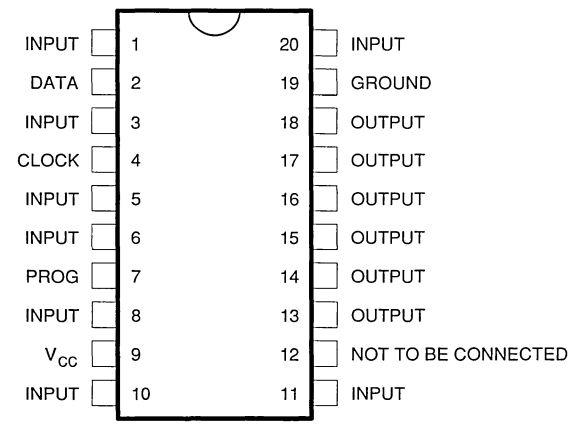
DIP20
(Plastic Package)

ORDER CODE : TEA6415B

DESCRIPTION

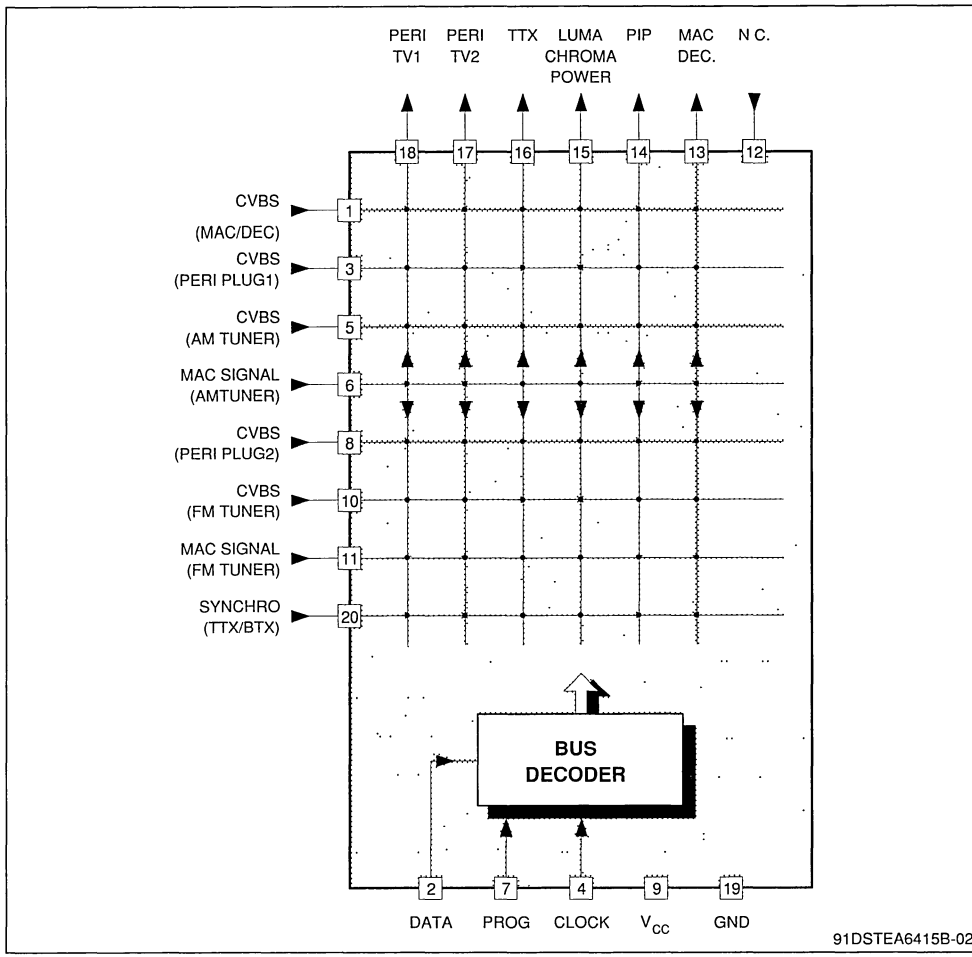
The main function of the TEA6415B is to switch 8 video input sources on the 6 outputs.
Each output can be switched to only one of the inputs whereas but any same input may be connected to several outputs.
All the switching possibilities are controlled through the I^2C Bus.

PIN CONNECTIONS



91DSTEA6415B-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (pin 9)	13	V
T_A	Operating Ambient Temperature Range	0 to +70	°C
T_{stg}	Storage Temperature Range	-20 to +150	°C

THERMAL DATA

Symbol	Parameter	Min.	Typ.
$R_{th(j-a)}$	Junction-Ambient Thermal Resistance	80	°C/W

ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_{CC} = 10V$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 3pF$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage (pin 9)	8	10	11	V
I_{CC}	Power Supply Current (without load on outputs ; V_{CC}=10V)	20	30	40	mA

INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Maximum Signal Amplitude (CVBS signal)	2			V_{PP}
	Input Current (per output connected, input voltage = $5V_{DC}$) (this current is X6 when all outputs are connected on the input)		1	3	µA
	DC Level	3.3	3.6	3.9	V
	DC Level Shift (temperature from 0 to 70^oC)		5	100	mV

OUTPUTS (V_{IN} = $1V_{PP}$ for all dynamic tests) Pins 13 - 14 - 15 - 16 - 17 - 18

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Dynamic	4.5	5.5		V_{PP}
	Output Impedance		25	50	Ω
	Gain	5.5	6.5	7.5	dB
	Bandwidth ● -1dB attenuation ● -3dB attenuation	7	 10 15		 MHz MHz
	Crosstalk (f = 5MHz)		-50		dB
	DC level	2.4	2.7	3	V

I^2C BUS INPUT : DATA, CLOCK, PROG (Pins 2 - 4 - 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Threshold Voltage	1.5	2	3	V

GENERAL DESCRIPTION

The main function of the IC is to switch 8 video input sources on 6 outputs.
Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals).
Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5 V_{DC} on the input.Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge). All the switching possibilities are changed through the BUS.
Driving 75Ω load needs an external transistor.
It is possible to have the same input connected to several outputs.
The starting configuration upon power on (power supply : 0 to 10V) is undetermined.
In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

BUS SELECTIONS (I^2C-BUS)

2 nd byte of transmission

ADDRESS MSB	DATA LSB	Selected Output	
00000	XXX	pin 18	Output is selected by address bits
00100	XXX	pin 14	
00010	XXX	pin 16	
00110	- - -	Not used	
00001	XXX	pin 17	
00101	XXX	pin13	
00011	XXX	pin 15	
00111	- - -	Not used	
		Selected Input	
00XXX	000	pin 5	Input is selected by data bits
00XXX	100	pin 8	
00XXX	010	pin 3	
00XXX	110	pin 20	
00XXX	001	pin 6	
00XXX	101	pin 10	
00XXX	011	pin 1	
00XXX	111	pin 11	

Example : 00100 101 connects pin 10 (input) to pin 14 (output).
(equals 25 in hexadecimal)

Adress byte (1st byte of transmission)

86	1000	0110	When pin PROG is connected to ground
06	0000	0110	When pin PROG is connected to V_{CC}

IN / OUT PIN CONFIGURATION

Figure 1 : Input Configuration.

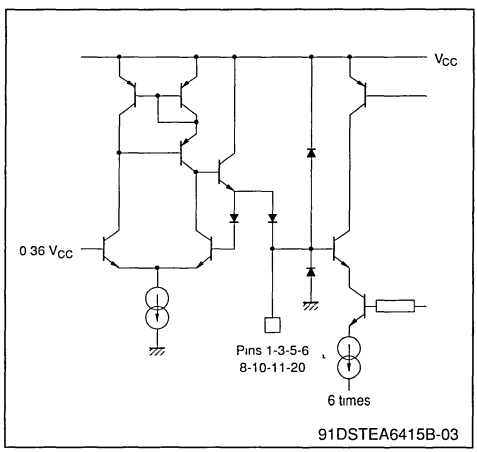
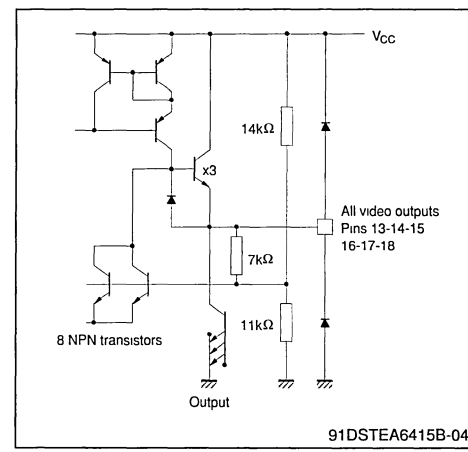


Figure 2 : Output Configuration.



IN / OUT PIN CONFIGURATION (continued)

Figure 3 : Bus I/O Configuration.

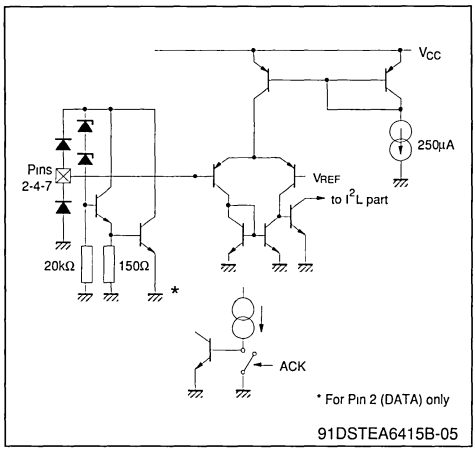
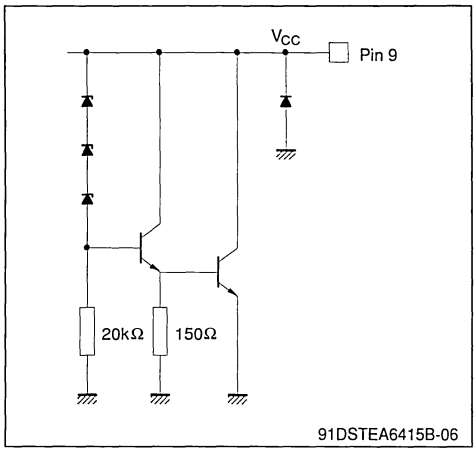
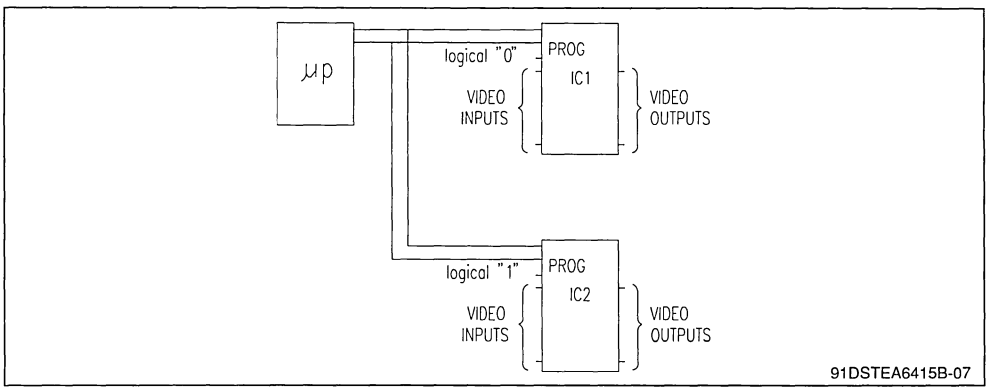


Figure 4 : V_{CC} Pin Configuration.

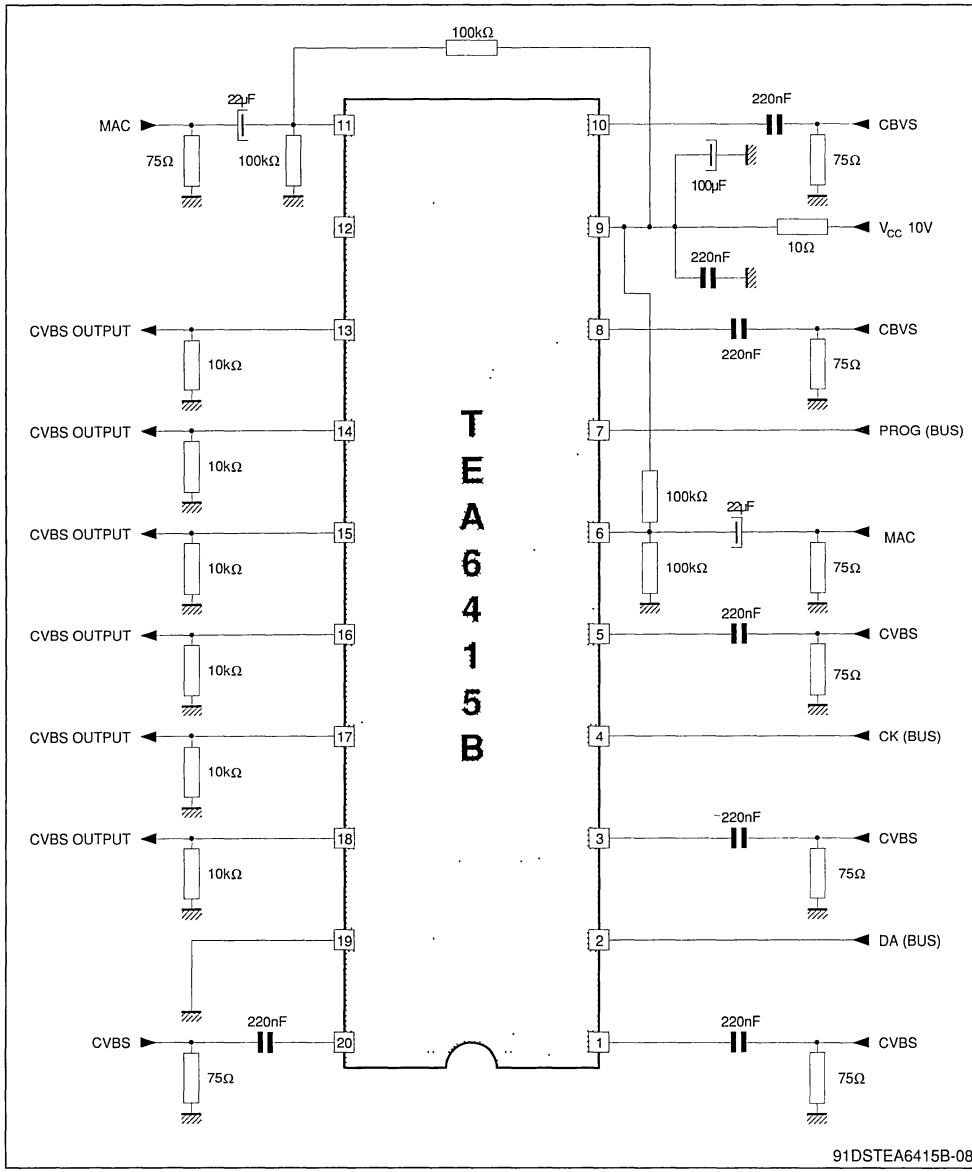


USE WITH AN OTHER TEA6415B

The programmation input (PROG) permits to operate with two TEA6415B in parallel and to select them independantly through the I^2C-BUS without modifying the adress byte. Consequently, the switch capabilities are doubled or IC1 and IC2 can be cascaded.



TYPICAL APPLICATION



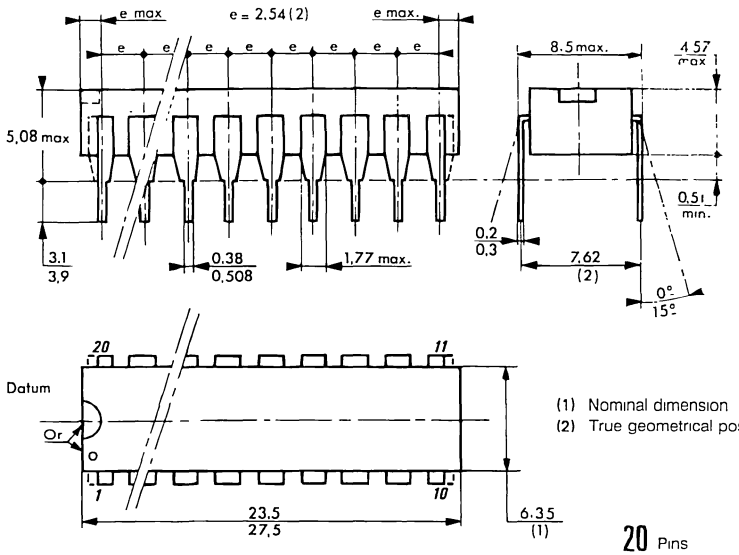
CROSSTALK IMPROVEMENT

1 - When any input is not used, it must be bypassed to ground through a 220nF capacitor.

2 - An important improvement can be achieved considering the input crosstalk by means of the application (see technical note).

PACKAGE MECHANICAL DATA

20 PINS – PLASTIC DIP



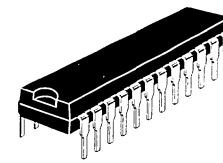
SGS-THOMSON MICROELECTRONICS

TEA6420

BUS-CONTROLLED AUDIO MATRIX

PRELIMINARY DATA

- 5 STEREO INPUTS
- 4 STEREO OUPUTS
- GAIN CONTROL 0/2/4/6DB/MUTE FOR EACH OUTPUT
- CASCADABLE (2 DIFFERRENT ADDRESSES)
- SERIAL BUS CONTROLLED
- VERY LOW NOISE



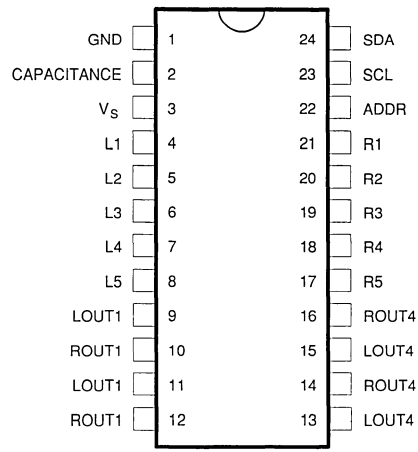
SDIP24
(plastic package)

ORDER CODE : TEA6420

DESCRIPTION

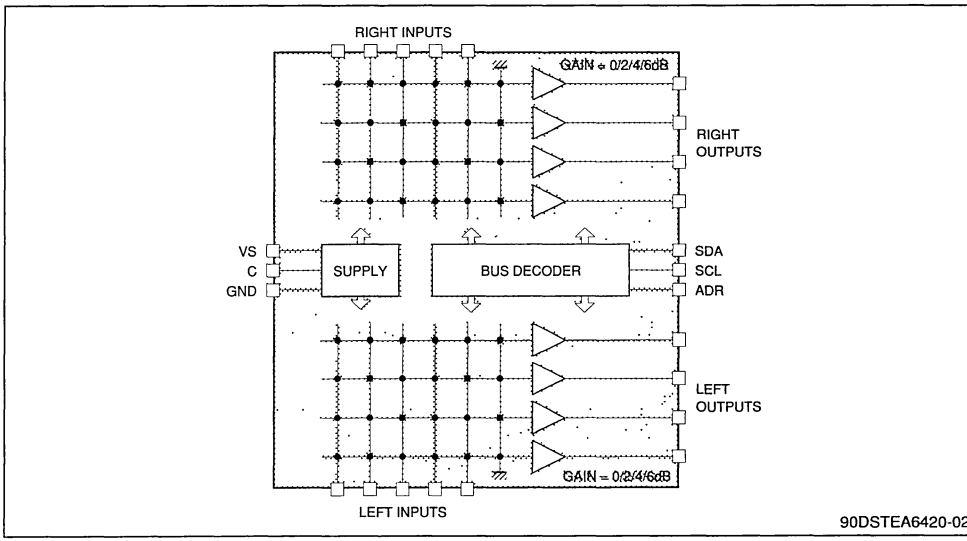
The TEA6420 switches 5 stereo audio on 4 stereo outputs.
All the switching possibities are changed through the I^2C BUS.

PIN CONNECTIONS



91DSTEA6420-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc	Supply Voltage	10.2	V
Toper	Operating ambient temperature	- 20 to + 85	°C
Tstg.	Storage Temperature	- 55 to + 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction - ambient thermal resistance	75	°C/W

ELECTICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 9V$, $R_L = 10k\Omega$, $R_G = 600\Omega$, f = 1kHz (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		8	9	10.2	V
I_S	Supply Current			5	8	mA
SVR	Ripple Rejection	$W_{IN} = 500mV_{RMS}$, BW = 20 - 20kHz		80		dB
MATRIX						
V_{IN}	Input DC Level			5		V
R_I	Input Resistance		30	50		kΩ
C_S	Channel Separation	$W_{IN} = 2V_{RMS}$, BW = 20 - 20kHz		90		dB
OUTPUT BUFFER						
V_{OUT}	Output DC Level			5		V
R_{OUT}	Output Resistance			50		Ω

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25°C$, $V_S = 9V$, $R_L = 10k\Omega$, $R_G = 600\Omega$, f = 1kHz (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OUTPUT BUFFER (continued)						
e_{NI}	Input Noise	BW = 20 - 20kHz, flat		3		µV
S/N	Signal to Noise Ratio	$V_{IN} = V_{OUT} = 1V_{RMS}$		110		dB
G_{min}	Min. Gain		-1	0	+ 1	dB
G_{max}	Max. Gain		5	6	7	dB
d	Distortion	$V_{IN} = V_{OUT} = 1V_{RMS}$		0.01		%
V_{CL}	Clipping Level	d = 0.3%	2	2.5		V_{RMS}
R_L	Output Load Resistance		2			kΩ
BUS INPUT						
V_{IL}	Input Low Voltage				1	V
V_{IN}	Input High Voltage (pin 24)		4			V
I_I	Input Current		- 10		10	µA
V_O	Output Voltage	I_O = 3mA ; SDA Acknowledge pin			0.4	V
R_{pu}	ADDR Pullup Resistor	Note 1		50		kΩ

Note : 1. R_{pu} is an internal pull-up resistor connected between the address programming pin ADDR and the internal positive supply voltage. Leaving ADDR disconnected or "floating" allows it to become logic 1. Connecting ADDR externally to the GND pin forces it to logic 0.

SOFTWARE SPECIFICATION

1. Chip address

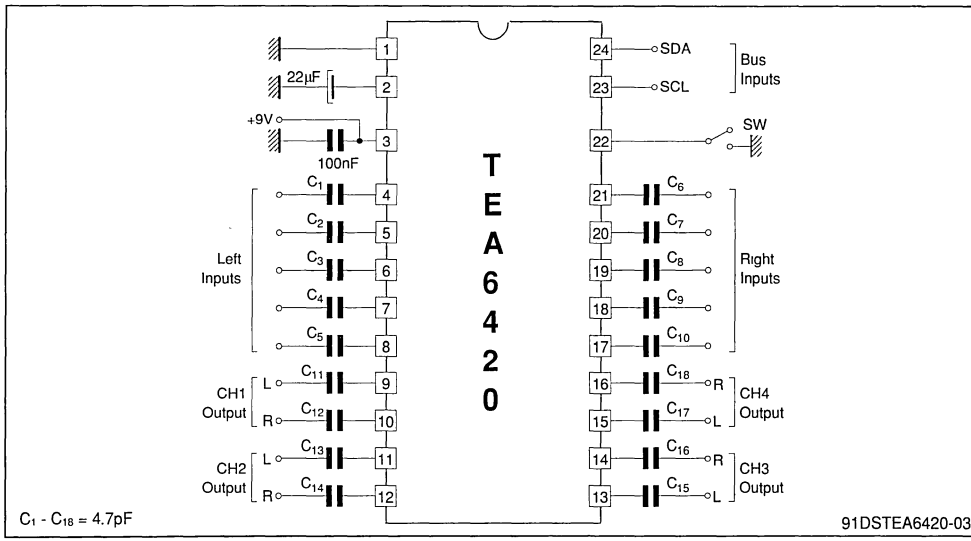
Address	HEX	ADDR
1001 1000	98	0
1001 1010	9A	1

2. Data bytes

Output select								
X	0	0	G_1	G_0	I_2	I_1	I_0	Output 1
	0	1						Output 2
	1	0						Output 3
	1	1						Output 4
Input select								
X	Q_1	Q0	G_1	G_0	0	0	0	Input 0
					0	0	1	Input 1
					0	1	0	Input 2
					0	1	1	Input 3
					1	0	0	Input 4
					1	0	1	Mute
Gain select								
X	Q_1	Q0	0	0	I_2	I_1	I_0	Gain = 6 dB
			0	1				Gain = 4 dB
			1	0				Gain = 2 dB
			1	1				Gain = 0 dB

X = don't care
MSB is transmitted first
Example : 0 10 01 100 connects outputs 3 with input 4 at a gain of 4dB
The following are selected after power-on reset . input 4 selected for all outputs ; gain = 0dB.

TYPICAL APPLICATION



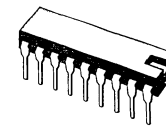
SGS-THOMSON MICROELECTRONICS

TEA8805

1.3 GHz PLL AND PRESCALER CIRCUIT

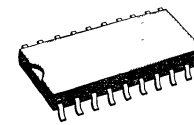
PRELIMINARY DATA

- FULLY SERIAL BUS-CONTROLLED (I^2C-BUS)
- SEVEN PROGRAMMABLE OUTPUT BAND BUFFERS (CAN DRIVE UP TO 10mA)
- PROGRAMMABLE REFERENCE COUNTER
- SELECTABLE DIVIDE-BY-8 PRESCALER (ACCEPTS INPUT FREQUENCIES > 1.3GHz)
- 15-BIT PROGRAMMABLE COUNTER (ACCEPTS INPUT FREQUENCIES > 160MHz)
- TRI-STATE PHASE/FREQUENCY COMPARATOR
- OPERATIONAL AMPLIFIER FOR DIRECT TUNING VOLTAGE OUTPUT (33V)
- 62.5kHz OUTPUT
- CHIP ADDRESS PROGRAMMABLE BY APPLICATION



DIP18
(Plastic Package)

ORDER CODE : TEA8805



SO20 LARGE
(Plastic Micropackage)

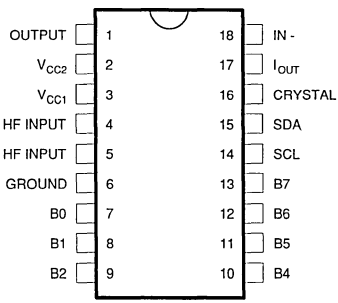
ORDER CODE : TEA8805D

DESCRIPTION

The TEA8805 is a PLL and prescaler circuit for TV applications using frequency synthesis tuning principle. It can handle frequencies up to 1.3GHz and is fully serial bus controlled (I^2C-Bus).

PIN CONNECTIONS

DIP18



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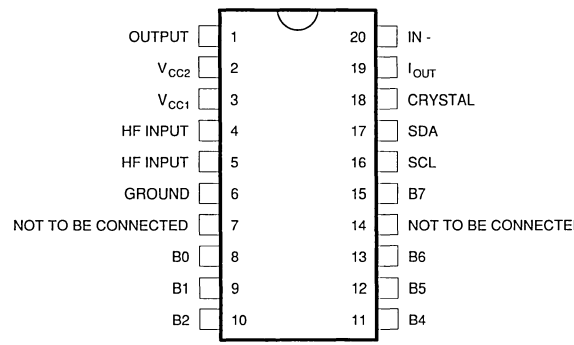
SO20 LARGE

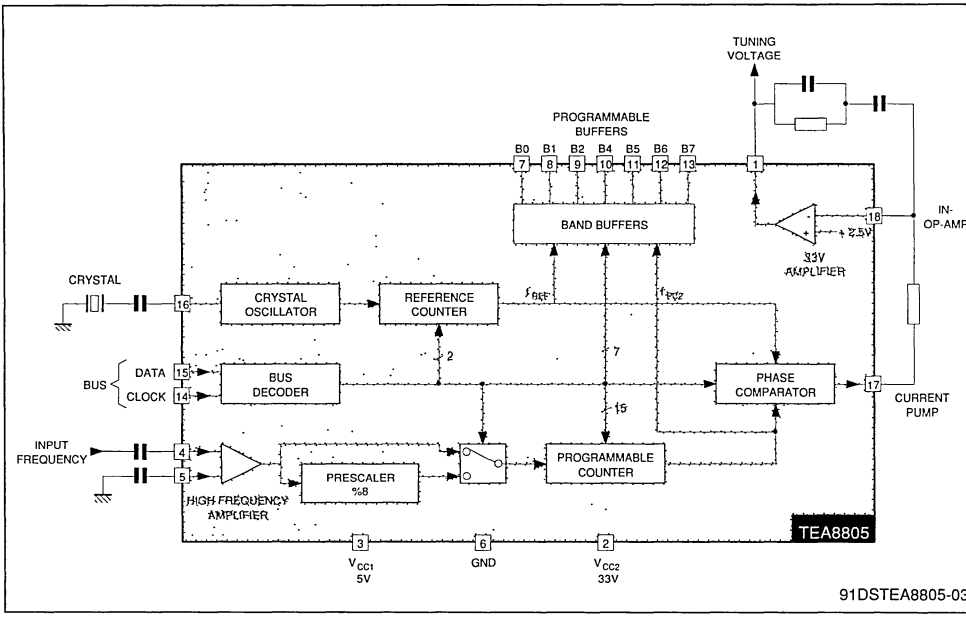


91DSTEA8805-02

PINS FUNCTIONS

Pin	Name	Function
DIP18 PACKAGE		
1	Output	Operational amplifier output which provides the tuning voltage
2	V_{CC2}	Operational amplifier positive supply
3	V_{CC1}	Positive supply of the circuit (except operational amplifier)
4, 5	HF INPUT	Either of the inputs may be used as reference
6	GND	Ground
7, 8, 9, 10, 11, 12, 13	B0, B1, ... B7	Band programmable buffer output
14	SCL	Clock input
15	SDA	Data input
16	Crystal	Crystal input (4MHz)
17	I_{OUT}	Phase comparator output
18	IN -	Negative operational amplifier input
SO20L PACKAGE		
1	Output	Operational amplifier output which provides the tuning voltage
2	V_{CC2}	Operational amplifier positive supply
3	V_{CC1}	Positive supply of the circuit (except operational amplifier)
4, 5	HF INPUT	Either of the inputs may be used as reference
6	GND	Ground
8, 9, 10, 11, 12, 13, 15	B0, B1, ... B7	Band programmable buffer output
16	SCL	Clock input
17	SDA	Data input
18	Crystal	Crystal input (4MHz)
19	I_{OUT}	Phase comparator output
20	IN -	Negative operational amplifier input
7, 14	NC	Not to be connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_{AMB} = 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{CC1}	Power Supply Voltage	6.0	V
	Band Buffer "OFF" Voltage Pins 7, 8, 9, 11, 12, 13 Pin 10	 16.5 V_{CC1}	 V V
	Band Buffer "ON" Current Pins 7, 8, 9, 11, 12, 13 Pin 10	 10 100	 mA µA
V_{CC2}	Operational Amplifier Power Supply Voltage	36	V
	Operational Amplifier Short Circuit Duration (0 to V_{CC2})	continuous	V
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_{oper}	Operating Temperature Range	0 to +70	°C

THERMAL DATA

Rth (j-a)	Junction-ambient Thermal Resistance DIP18 package SO20 LARGE package	 70 65	 °C/W °C/W

ELECTRICAL CHARACTERISTICS

V_{CC1} = 5V, V_{CC2} = 32V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC1}	Supply Voltage Range	4.5	5 0	5.5	V
I_{CC1}	Supply Current (V_{CC1} = 5.0V) (see note)		30	45	mA
V_{CC2}	Supply Voltage Range	25	30	35	V
I_{CC2}	Supply Current (output open)		0.8	2.0	mA
BAND BUFFERS					
	Band Buffer Leakage Current when "OFF"" at 5V (PIn 10) at 15V (Pins 7, 8, 9, 11, 12, 13)		0.1 0.1	1.0 1.0	µA µA
	Band Buffer Saturation Voltage when "ON" at 10mA (PIns 8, 9, 10, 11, 12, 13) at 10mA (PIn 7)		0.5 2.5	1.0	V V
BUS DECODER					
	Data/CLock Current at 0V	-1		0	µA
	Clock Current at 5.0V	0		5.0	µA
	Data CUrrent at 5.0V Acknowledge "OFF"	0		5 0	µA
	Data Saturation Voltage at 10mA Acknowledge "ON"			1.0	V
	Data/Clock Input Voltage Low			1.5	V
	Data/Clock Input Voltage High	3.0			V
	Clock Frequency Range	0		500	kHz
PHASE COMPARATOR					
	Phase Detector Tri-state Current	-15	0	15	nA
	Phase Detector High-state Source Current (@ 2.5V)		-450		µA
	Phase Detector Low-state SInk Current (@ 2.5V)		380		µA
OPERATIONAL AMPLIFIER					
	Operational Amplifier Internal Reference Voltage	2.0		3.0	V
	Operational Amplifier Input Current	-15	0	15	nA
	DC Open Loop Gain	5000			
	Gain Bandwidth Product (R_L = 10kΩ, C_L = 20pF)	0.3			MHz
	Phase Margin (R_L = 10kΩ, C_L = 20pF)		50		Deg.
	V_{OUT} Low, Sinking 50µA		0.1	0.3	V
	V_{OUT} High, Sourcing 50µA, VCC2	-4.0	-3.0		V
	V_{CC1} Supply Ripple Rejection		54	-45	dB
HF CHARACTERISTICS					
	HF in/Ref DC Bias		2		V
	HF Voltage Range Prescaler "OFF" 10-180MHz	20		300	mV_{RMS}
	HF Voltage Range Prescaler "OFF" 80-900MHz	20		300	mV_{RMS}
	HF Voltage Range Prescaler "ON" 900-1300MHz	50		300	mV_{RMS}

Note : When prescaler "OFF", typical supply current is decreased by 10mA

GENERAL DESCRITION

Bus Decoder - Data Format

The circuit receives the information for tuning and control via the Bus (I^2C-Bus).

The incomming information consisting of a chip address byte followed by two or four data bytes, is created in the bus decoder. The definition of the permissible bus protocol is shown below :

1- STA CA CO BA STO
2- STA CA FM FL STO
3- STA CA CO BA FM FL TO
4- STA CA FM FL CO BA STO

STA = Start condition
STO = Stop condition
CA = Chip address byte
CO = Data byte for control information
FM = Data byte for frequency information (MSB'S)
FL = Data byte for frequency information (LSB'S)
BA = Band Information

Frequency information is predeeded by a logic "0".

If the function bit is logic "1" the two following bytes contain control and band information where the bits have the following functions :

- Bit R0 and R1 : define the reference divider division ratio. Four ratios are available (see Table 1).
- Bit R2 and R3 : are used to switch internal signals to the buffer outputs. Pins 10 and 11 (see Table 2).
- Bit R2 and T : are used to control the phase comparator output stage (see Table 3)
- Bit P : switches the prescaler in and out. At logic "1" The prescaler is bypassed and the power supply of the prescaler is switched off.

COMPLETE DATA TRANSFER PROCESS

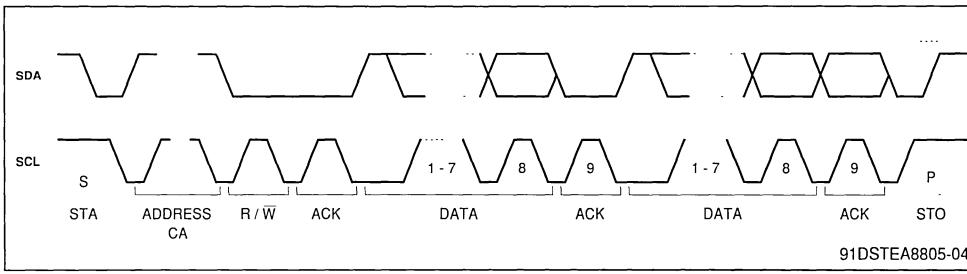


Figure 1 shows the five bytes of information that are needed for circuit operation : there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received : if three data bytes are received the third data byte is ignored.

If five or more data bytes are received the fifth and following data bytes are ignored and the last acknowledge puise is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allow the IC to distinguish between frequency information and control plus band information.

Chip address (CA) with Pin 7 to ground	1	1	0	0	0	1	1	0	ACK
Chip address (CA) with Pin 7 not grounded	1	1	0	0	0	0	1	0	ACK
Control INFO (CO)	(1)	R6	T	P	R3	R2	R1	R0	ACK
Band INFO (BA)	B7	B6	B5	B4	X	B2	B1	B0	ACK
Frequency INFO (FM)	(0)	N14	N13	N12	N11	N10	N9	N8	ACK
Frequency INFO (FL)	N7	N6	N5	N4	N3	N2	N1	N0	ACK

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Table 1

Input Data		Reference
R1	R0	Division Ratio
0	0	2048
0	1	1024
1	0	512
1	1	256

Table 2

Input Data		Test Output on Buffers	
R2	R3	PIn10	PIn11
0	0		
0	1	62.5kHz	
1	0	Fref	FpC2
1	1		

Bit B4 has to be "zero" when Pin 10 is used to output 62.5kHz frequency.
Bit B4 and B5 have to be "zero" to output internal IC signals : reference frequency (Fref) or programmable counter output frequency divided by 2 (FpC2) on PIns 10 and 11.

Table 3

Input Data			Output State of the Phase Comparator
R2	R6	T	
0	0	0	Normal operation
0	0	1	Off (high impedance)
0	1	0	High
0	1	1	Low
1	0	0	Normal operation
1	0	1	Off
1	1	0	Normal operation
1	1	1	Off

BAND BUFFERS

Band INFO (BA)	B7	B6	B5	B4	X	B2	B1	B0	ACK

The band buffers are open collector transistors and are active "low" at Bn = 1. They are designed for 10mA with a typical on-resistance of 70Ω. These buffers are designed to withstand relative high output voltage in the off-state.
B4 and B5 buffers (Pins 10 and 11 or Pins 11 and 12) may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for tests purposes. Buffer B4 may also be used to output a 62.5kHz frequency for an intermediate stage of the reference divider. The bit B4 and/or B5 have also to be zero if the buffers are used for these additional functions.

PROGRAMMABLE COUNTER
The programmable counter is a presentable down counter. When it has counted to zero it takes its required division ratio out of latches.
The division ratio definition is given by :
N = 16384 x N14 + 8132 x N13 + ... + 4 x N2 + 2 x N1 + N0
Max. Ration 32767
Min. Ratio 1024
Where N0...N14 are thedifferent bits for frequency information.
The counter may be used for any ratio between 1024 and 32767 and reloads correctly as long as its output frequency does not exceed 1/0MHz.
At power-on the whole bus receiver is reset and the programmable counter is set to a counting ratio of N = 1024 or higher.

PRESCALER
THe prescaler has a preamplifier which guarantees high input sensitivity. The prescaler may by-passed (Bip P).

PHASE COMPARATOR
The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

OPERATIONAL AMPLIFIER
The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The operational amplifier needs 33V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28V.
Block Diagram shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc).

OSCILLATOR
The oscillator uses a 4.0MHZ crystal tied to ground or V_{CC1} through a capacitor, used in the series resonance mode.
The voltage at Pin 16 or Pin 18, "crystal", has low amplitude and low harmonic distortion.

SYSTEM APPLICATION

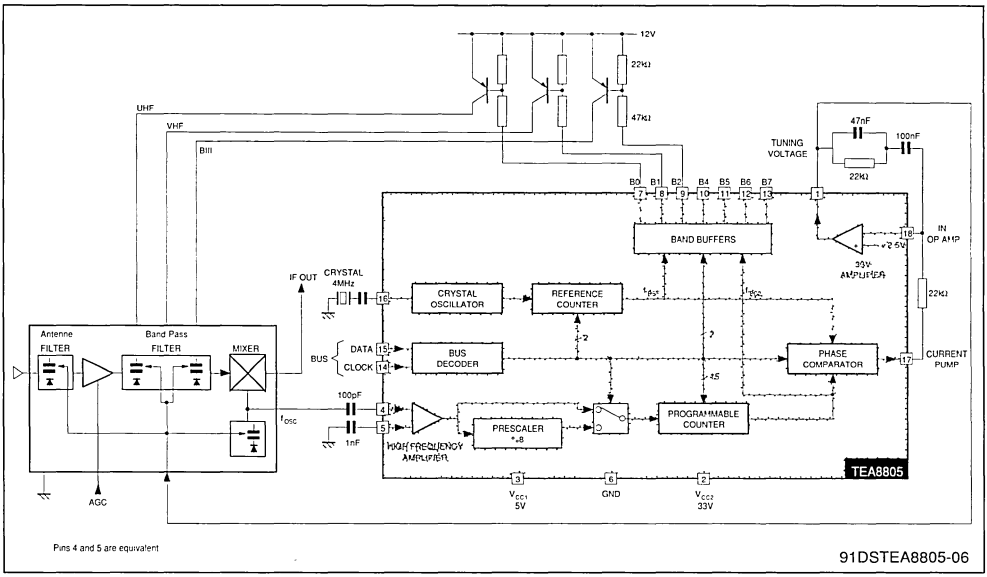
Table 4 is summary of the circuit applications using a 4.0MHz crystal.

Table 4

Input Data		Ref. Divider Div. Ratio	Reference Frequency (Hz) (1)	With int. Prescaler P = 0		With int. Prescaler P = 1	
R1	R0			Frequency Steps (kHz)	Max. Input Frequency (MHz)	Frequency Steps (kHz)	Max. Input Frequency (MHz)
0	0	2048	1953.125	15.625	512	1953125	64
0	1	1024	3906.25	31.25	1024	3.90625	128
1	0	512	7812.5	62.5	1300 (2)	7.8125	165 (3)
1	1	258	15525.0	125	1300 (2)	15.625	165 (3)

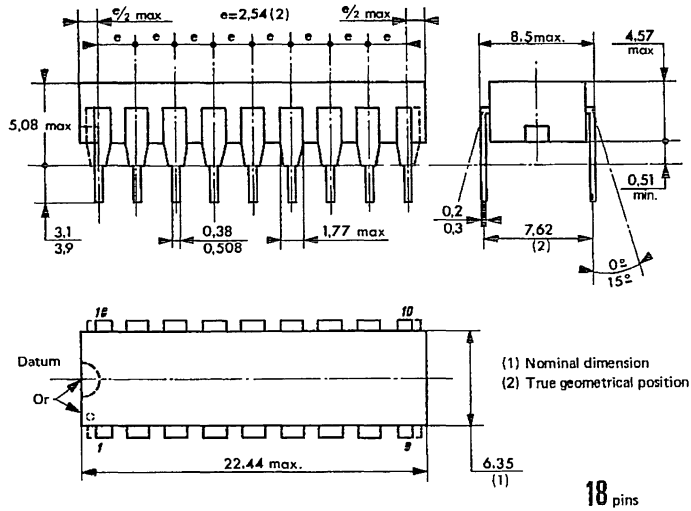
Notes : 1. With 4.0MHz crystal
2. Limit of prescaler
3 Limit of programmable divider

TYPICAL APPLICATION

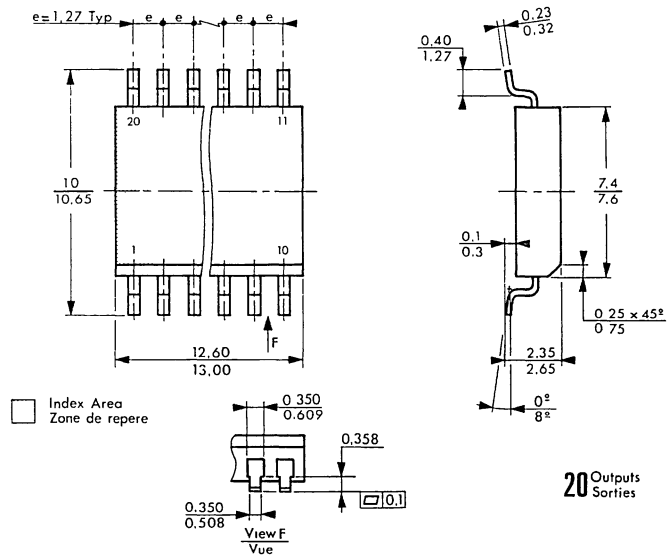


PACKAGE MECHANICAL DATA

18 PINS - PLASTIC DIP



20 PINS - PLASTIC MICROPACKAGE (SO LARGE)



REMOTE CONTROL TRANSMITTER

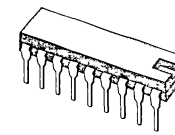
- ULTRASONIC OR INFRA-RED TRANSMISSION
- DIRECT DRIVE FOR ULTRASONIC TRANSDUCER
- DIRECT DRIVE OF VISIBLE LED WHEN USING INFRA-RED
- VERY LOW POWER REQUIREMENTS
- PULSE POSITION MODULATION GIVES EXCELLENT IMMUNITY FROM NOISE AND MULTIPATH REFLECTIONS
- SINGLE POLE KEY MATRIX
- SWITCH RESISTANCE UP TO 1 KΩ TOLERATED
- FEW EXTERNAL COMPONENTS
- ANTI-BOUNCE CIRCUITRY ON CHIP

QUICK REFERENCE DATA

- POWER SUPPLY : 9 V, STANDBY 6 µA, OPERATING 8 mA
- MODULATION : PULSE POSITION WITH OR WITHOUT CARRIER
- CODING : 5 BITS WORD GIVING A PRIMARY COMMAND SET OF 32 COMMANDS
- KEY ENTRY : 8 x 4 SINGLE POLE KEY MATRIX
- DATE RATE : SELECTABLE 1 BIT/SEC TO 10 K BIT/SEC
- CARRIER FREQUENCY : SELECTABLE 0 HZ (no carrier) TO 200 KHz

DESCRIPTION

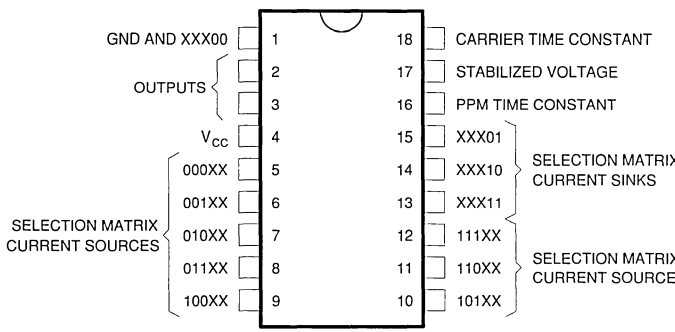
The UAA4000 is an easily expandable, 32 command, pulse position modulation transmitter drawing zero standby current.



DIP18
(Plastic Package)

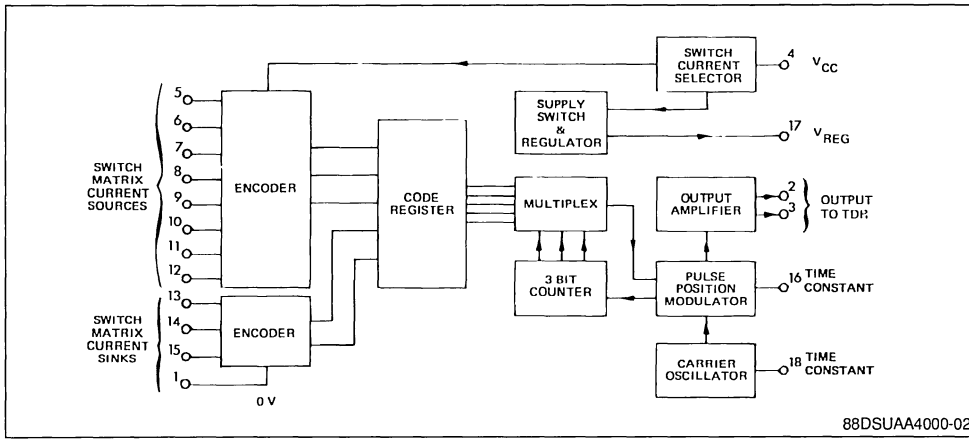
ORDER CODE : UAA4000

PIN CONNECTIONS



91DSUAA4000-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage	Pin 4	11	V
P_{tot}	Maximum Power Dissipation		600	mW
I_C	Maximum Output Current	Pin 3	5	mA
T_{oper}	Operating Temperature Range		– 10 to 65	°C
T_{stg}	Storage Temperature Range		– 55 to 125	°C

TAB-01

THERMAL DATA

$R_{th(j-a)}$	Junction–ambient Thermal Resistance	70	°C/W

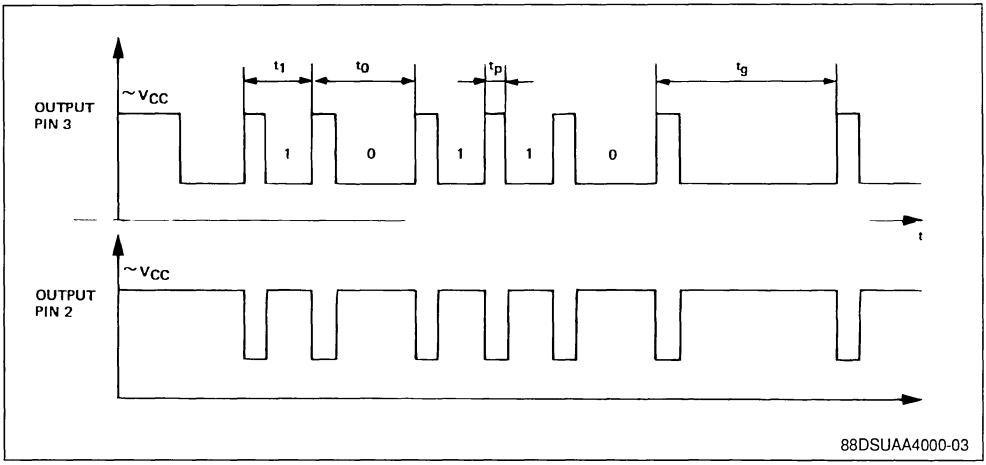
TAB-02

ELECTRICAL CHARACTERISTICS T_{amb} = 25°C, V_{CC} = 9V, f_o = 40kHz, t_1 = 18ms
4.7µF Capacitor on Pin 17 (unless otherwise specified) (see test circuit next page)

Symbol	Parameter	Pins	Min.	Typ.	Max.	Unit
V_{CC}	Operating Supply Voltage	4	7	9	11	V
	Operating Supply Current	4		8	16	mA
	Standby Supply Current	4			30	µA
	Stabilized Voltage	17	3.9	4.2	4.5	V
	Output Current Available	17			1	mA
	Output Voltage Swing (unloaded)	2, 3		8	V_{CC}	V
	Output Current (peak value)	2,3			5	mA
	External Switch Resistance				1	kΩ
	External Switch Closing Time		6			ms
	External Carrier Oscillator (R2 required, C_2 = 680 pF)	18	20	40	80	kΩ
	External PPM Resistor (R1 required, C_1 = 0.68 µF)	16	15	30	60	kΩ
	Ratio t0/t1	2, 3	1.4	1.5	1.6	
t_p	Pulse Width	2, 3	2	3	4	ms
t_g	Inter–word Gap	2, 3	50	54	58	ms

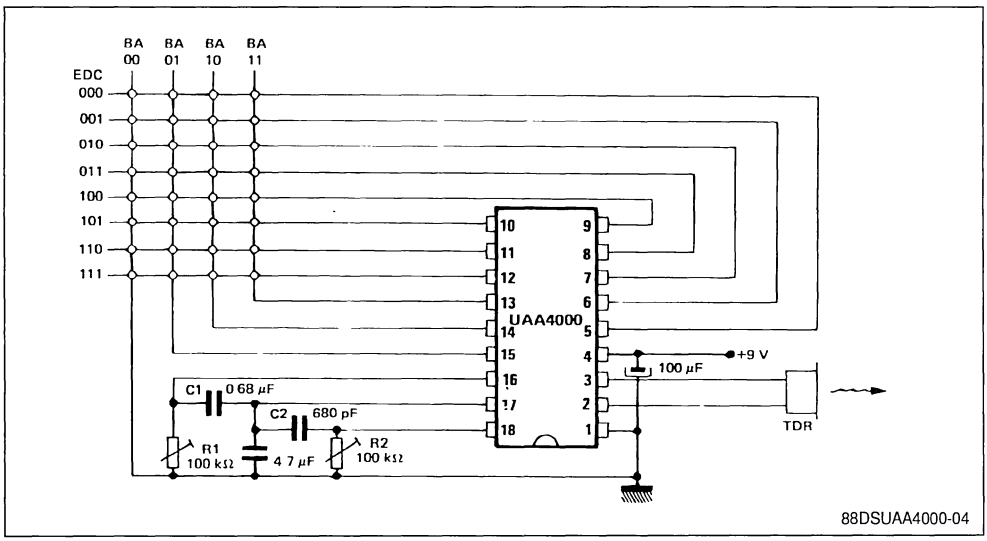
TAB-03

OUTPUT WAVEFORMS (PPM word notation)



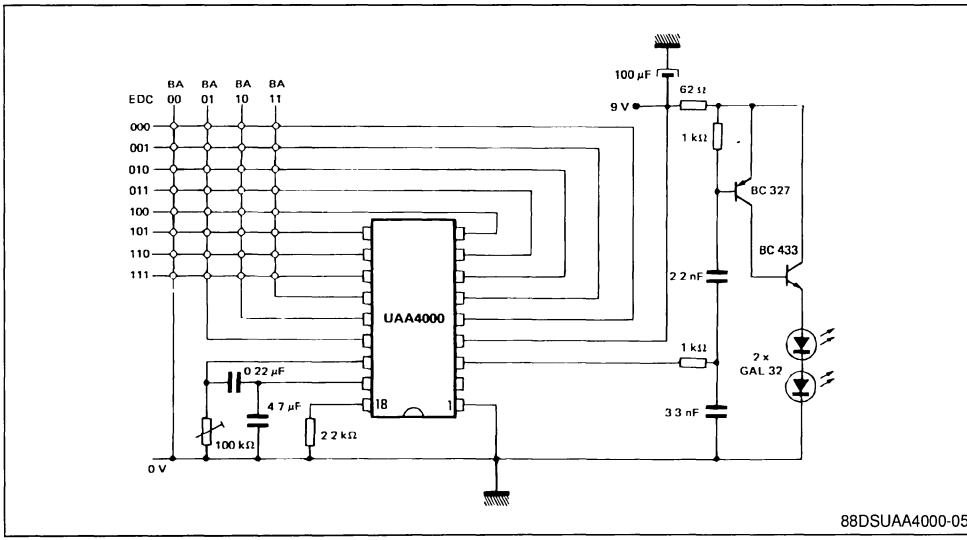
APPLICATION CIRCUITS

TEST AND ULTRASONIC APPLICATION CIRCUIT



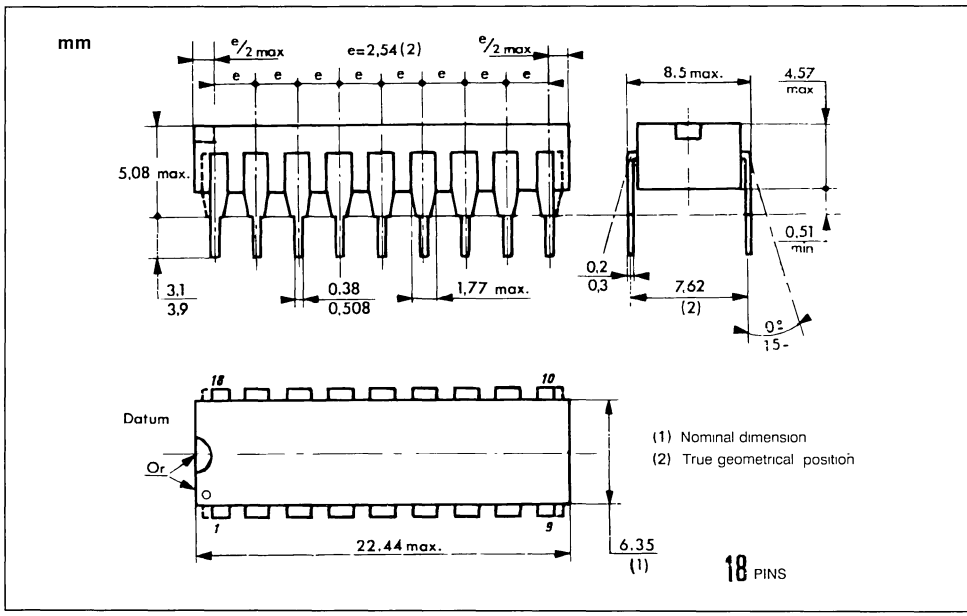
APPLICATION CIRCUITS (continued)

INFRA-RED APPLICATION CIRCUIT



PACKAGE MECHANICAL DATA

18 PINS – PLASTIC DIP

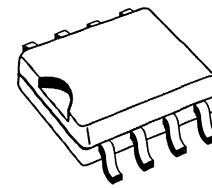


PACKAGES

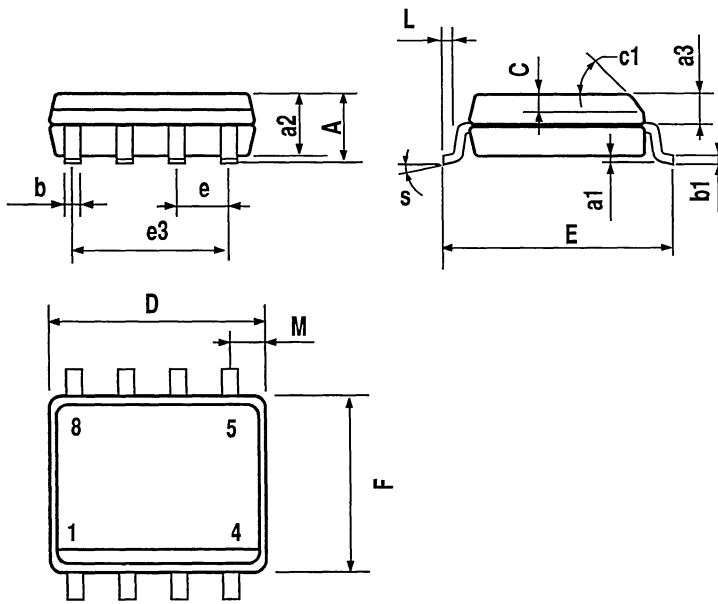
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO8

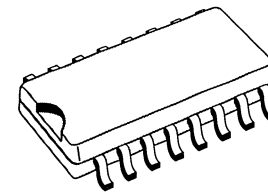


P013M

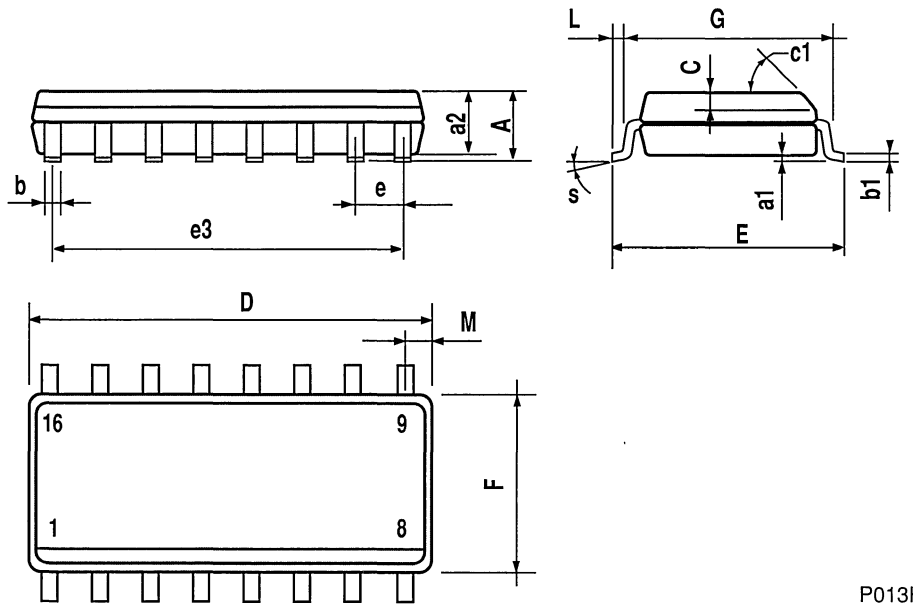
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.5		1.27	0.020		0.050
M			0.62			0.024
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16

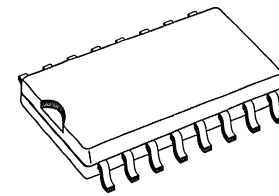


P013H

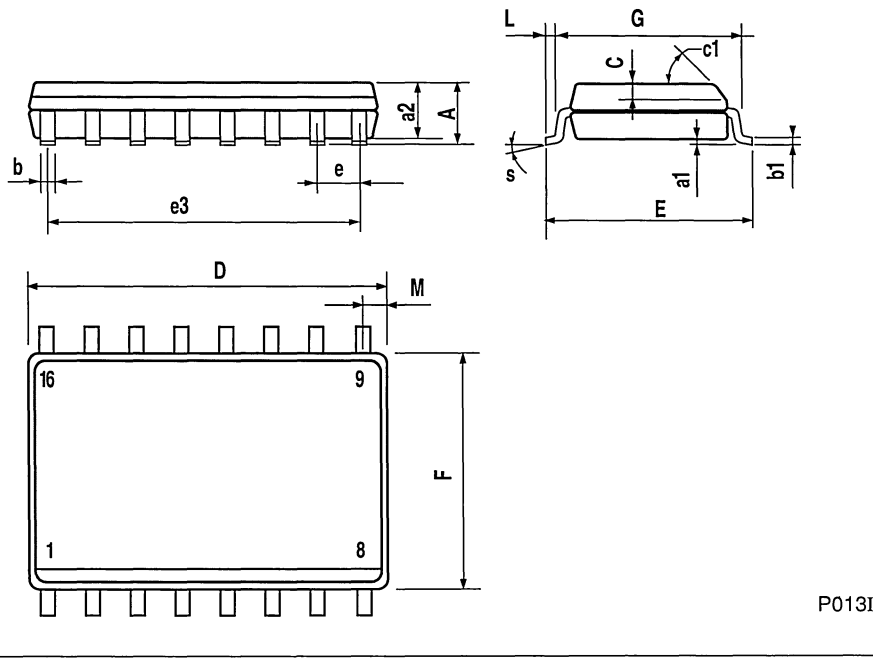
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.397		0.413
E	10.0		10.65	0.393		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.300
G	8.8		9.15	0.346		0.360
L	0.5		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16L

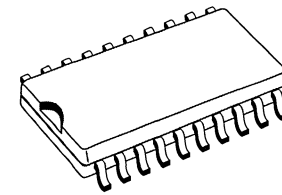


P013I

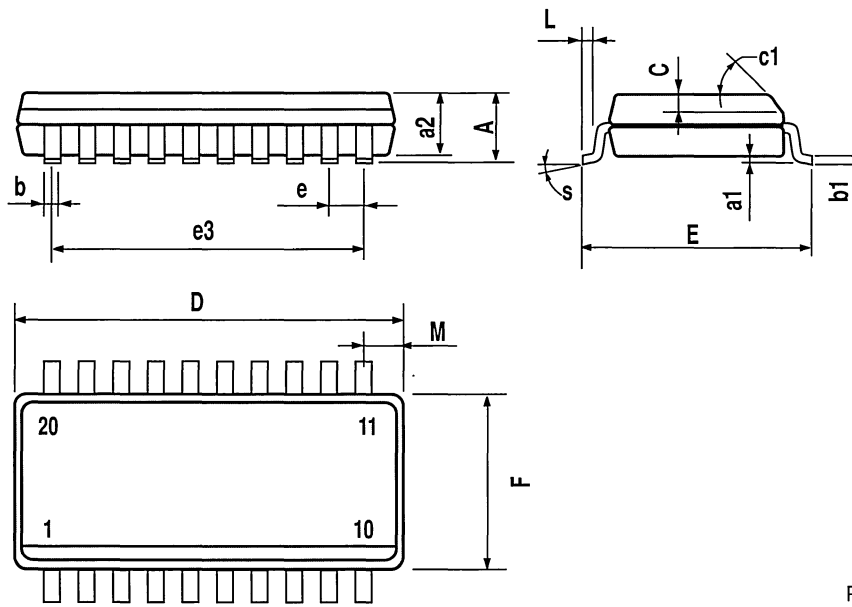
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO20

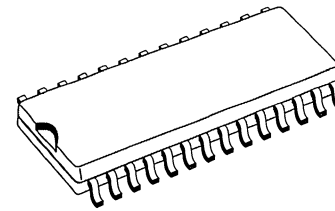


P013L

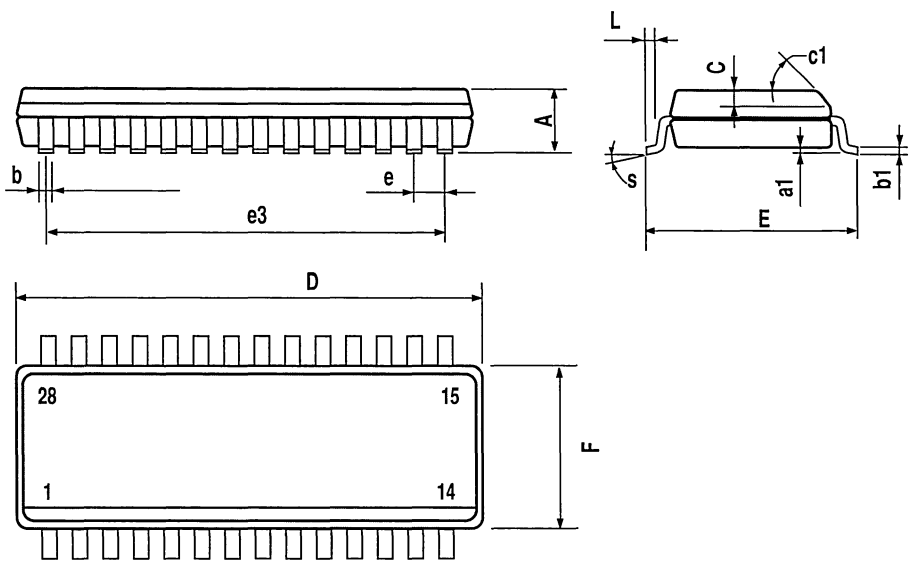
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO28

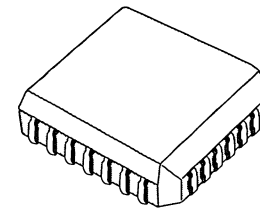


P013N

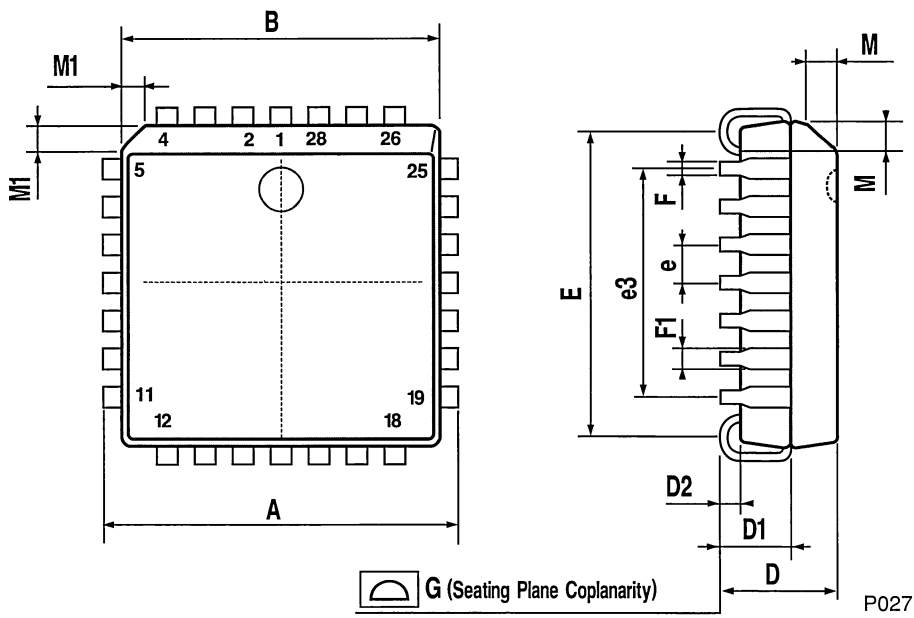
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



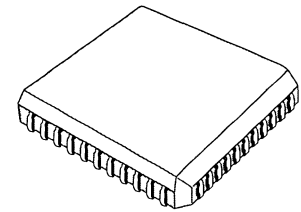
PLCC28



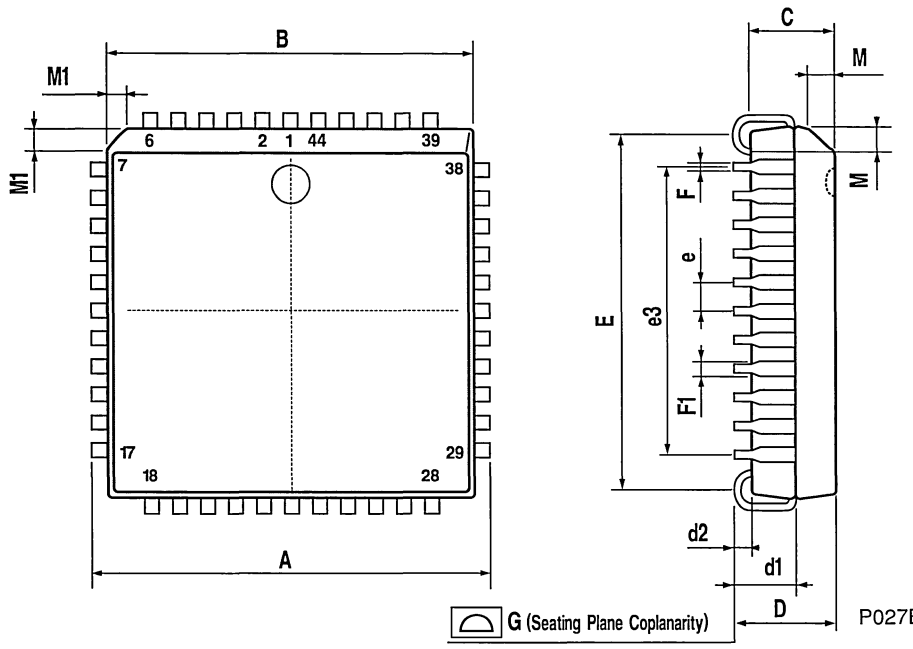
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



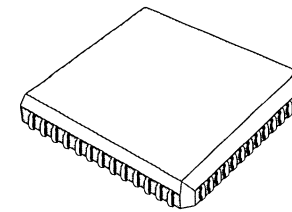
PLCC44



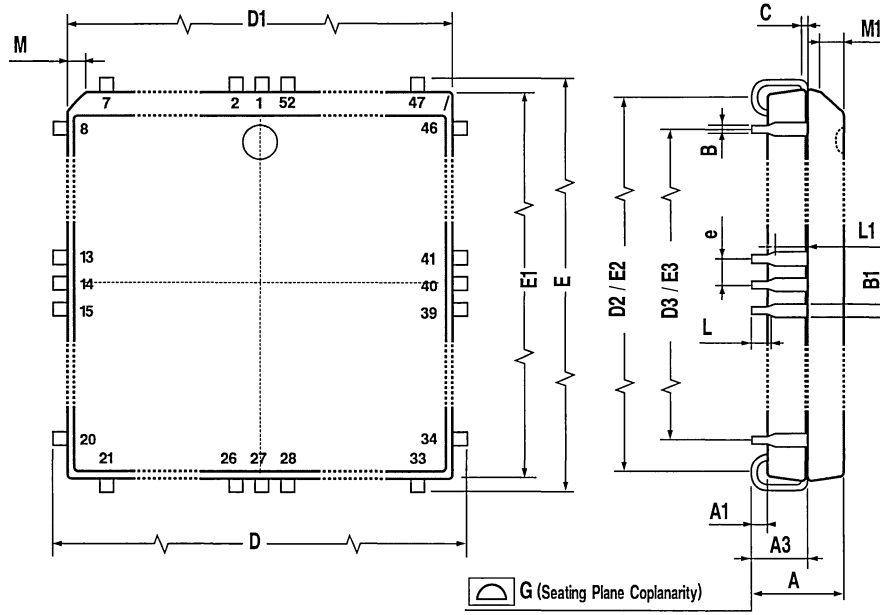
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		4.20	5.08		0.165	0.20
A1		0.51			0.020	
A3		2.29	3.30		0.090	0.13
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
C	0.25			0.01		
D		19.94	20.19		0.785	0.795
D1		19.05	19.20		0.750	0.756
D2		17.53	18.54		0.690	0.730
D3	15.24			0.60		
E		19.94	20.19		0.785	0.795
E1		19.05	19.20		0.750	0.756
E2		17.53	18.54		0.690	0.730
E3	15.24			0.60		
e	1.27			0.05		
L		0.64			0.025	
L1		1.53			0.060	
M		1.07	1.22		0.042	0.048
M1		1.07	1.42		0.042	0.056

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



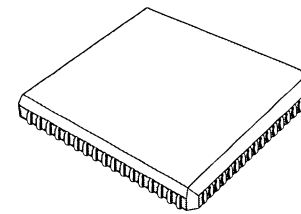
PLCC52



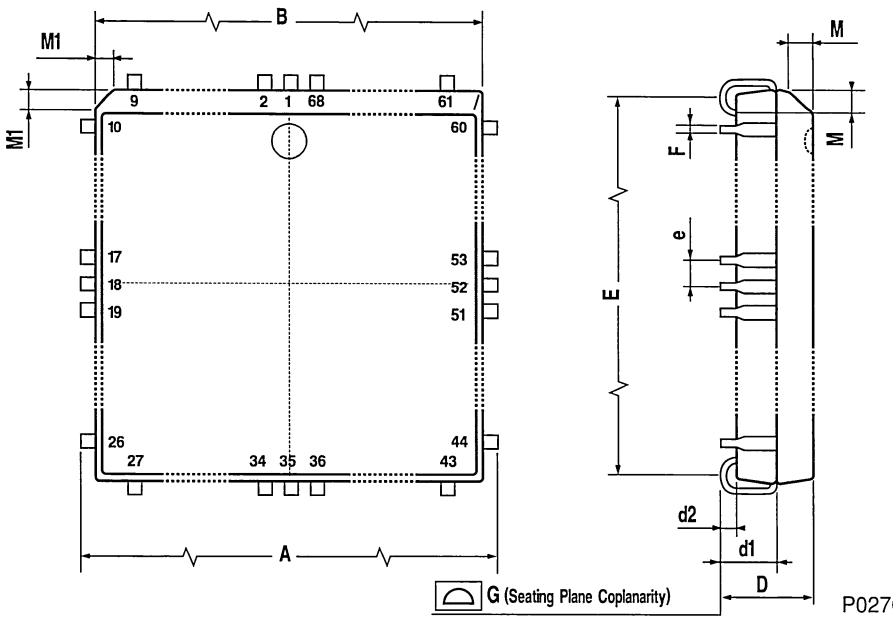
DIM.	mm			inch		
	MIN	TYP	MAX	MIN	TYP	MAX
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.2		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



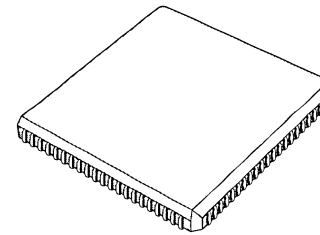
PLCC68



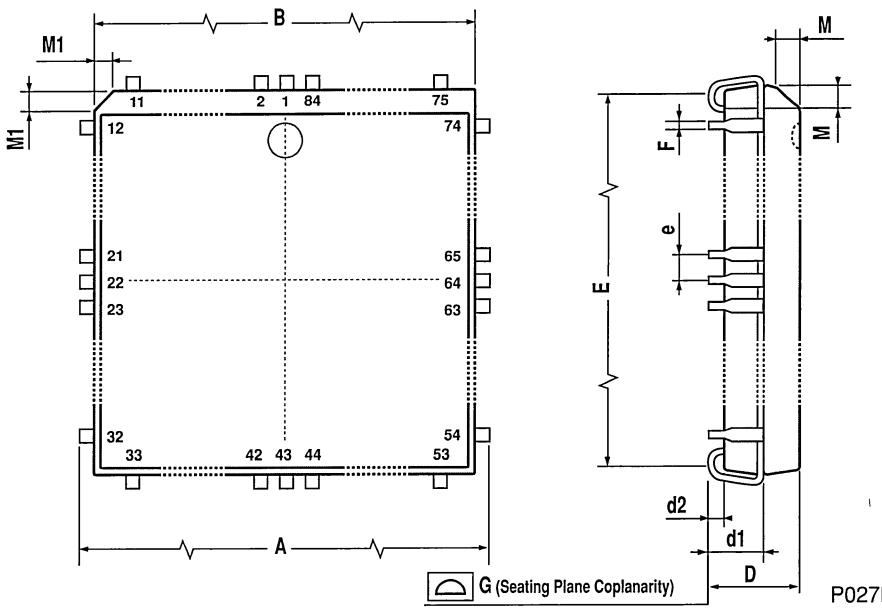
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	30.10		30.35	1.187		1.193
B	29.20		29.41	1.150		1.156
D	4.20		5.08	0.167		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	27.69		28.70	1.110		1.130
e		1.27			0.050	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



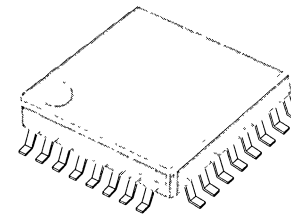
PLCC84



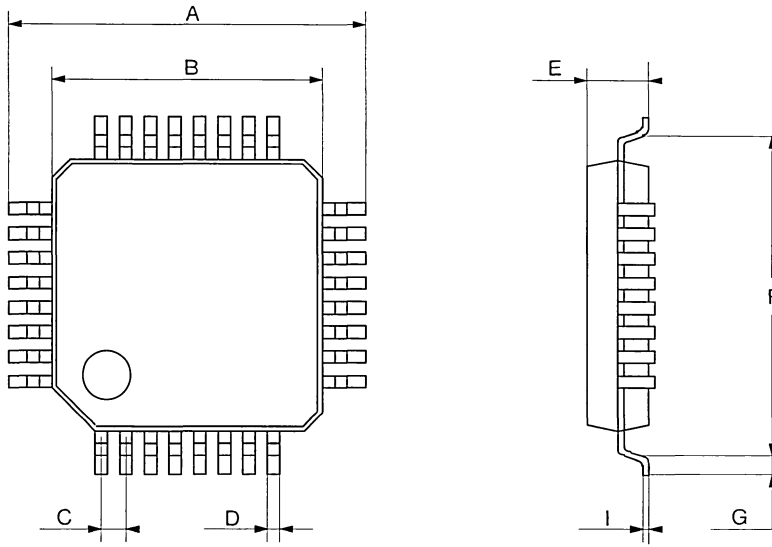
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.0		9.2	0.35		0.36
B	7.0		7.3	0.27		0.28
C	0.8			0.031		
D	0.3		0.45	0.011		0.017
E	1.5		1.85	0.060		0.072
F	8.0			0.31		
G	0.50			0.019		
I	0.127		0.227	0.005		0.008

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



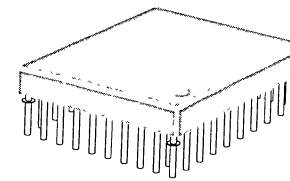
QFP32



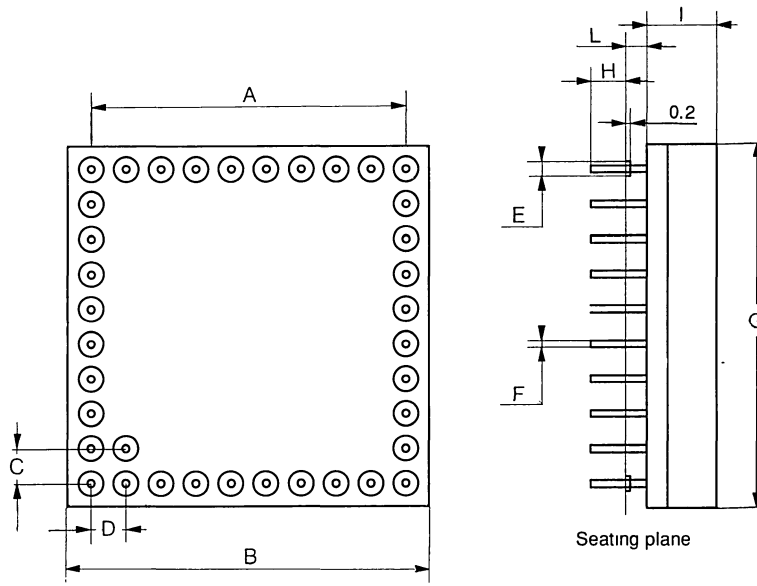
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	22.05		22.31	0.868		0.878
B	25.04		25.54	0.985		0.1000
C	2.54			0.100		
D	2.54			0.100		
E	1.2		1.3	0.047		0.051
F	0.46		0.51	0.018		0.020
G	25.40		25.90	0.996		0.1007
H	4.2			0.165		
I	3.8			0.149		

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



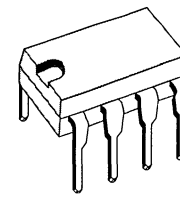
PGA37



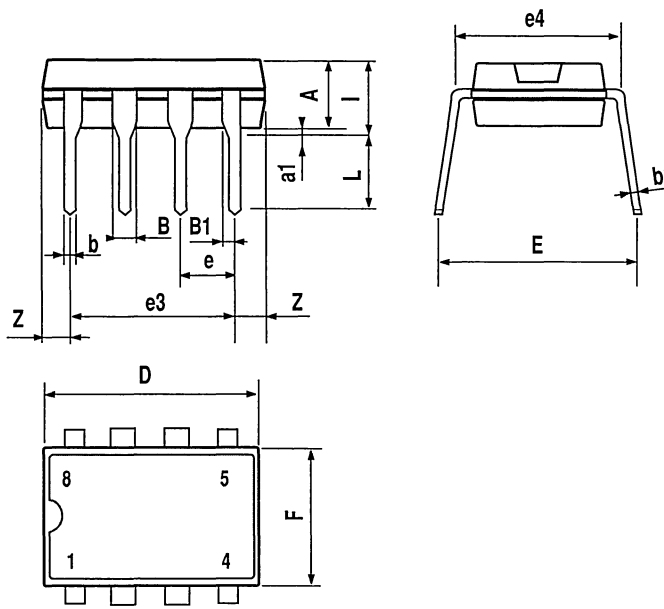
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Minidip (0.25)

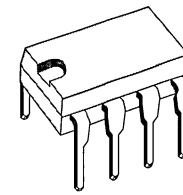


P001W

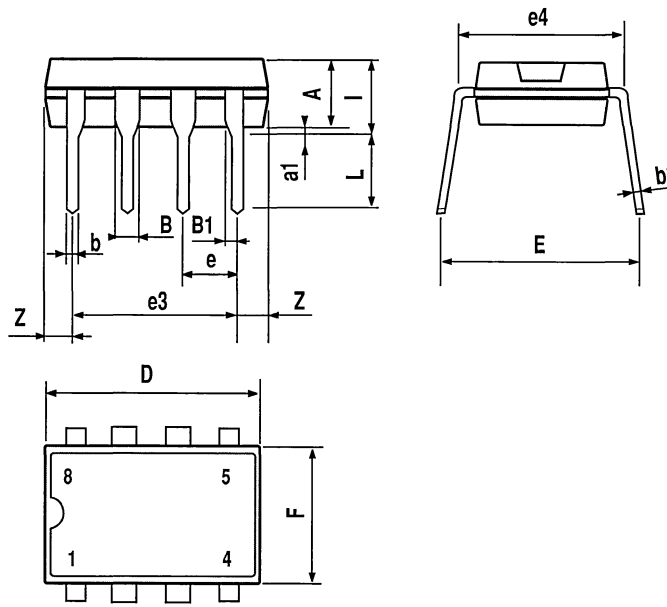
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Minidip (0.4)

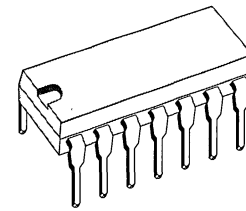


P001F

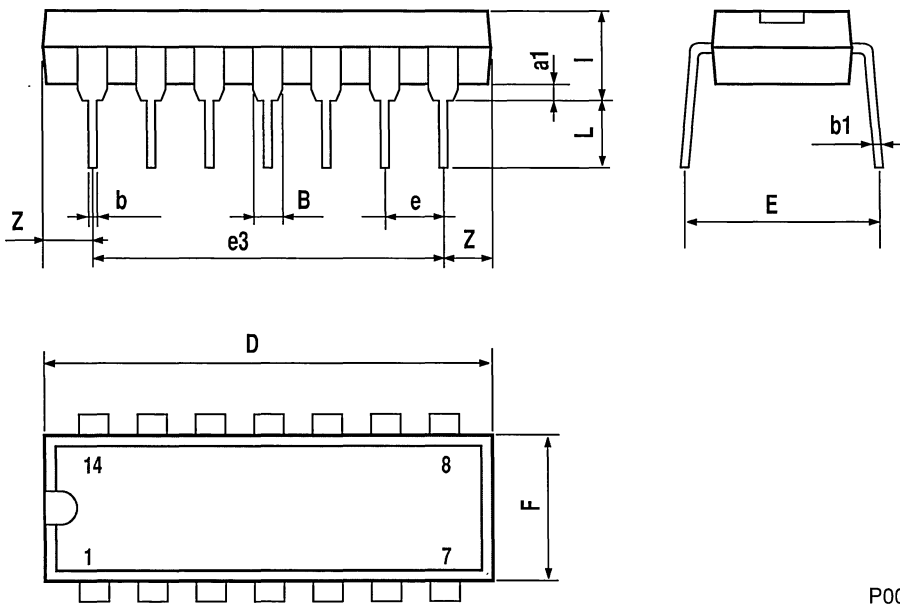
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP14

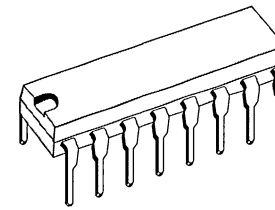


P001A

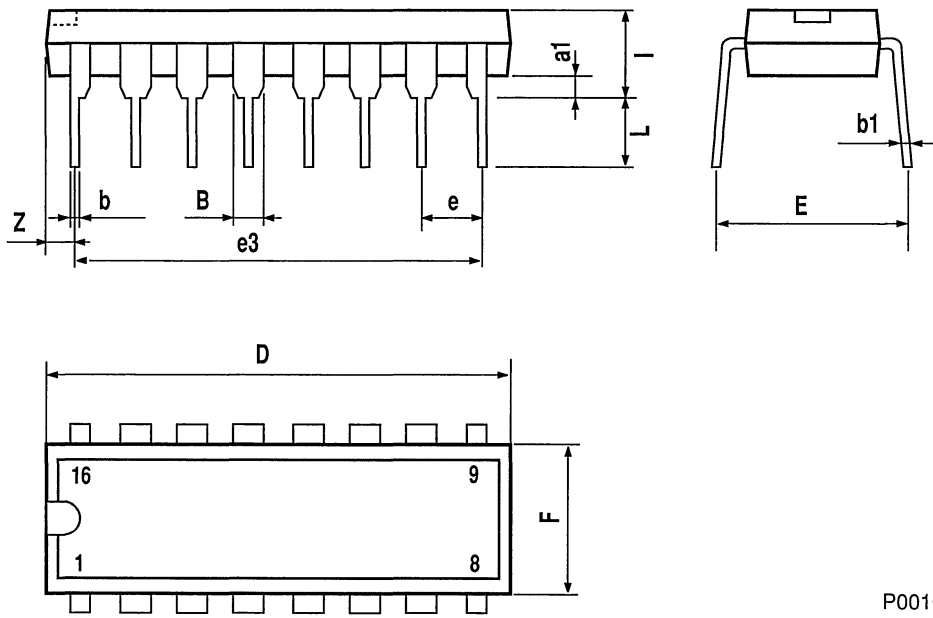
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP16 (0.25)

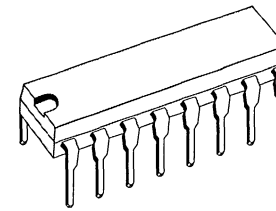


P001C

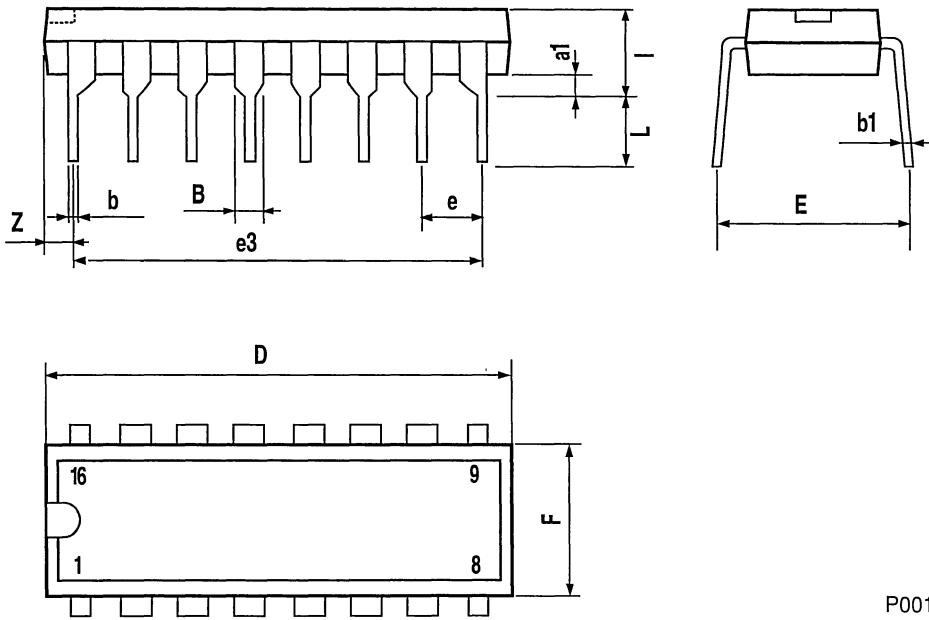
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
E		8.8			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP: (8+8), (12+2+2)

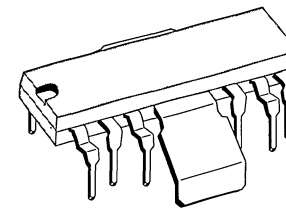


P001V

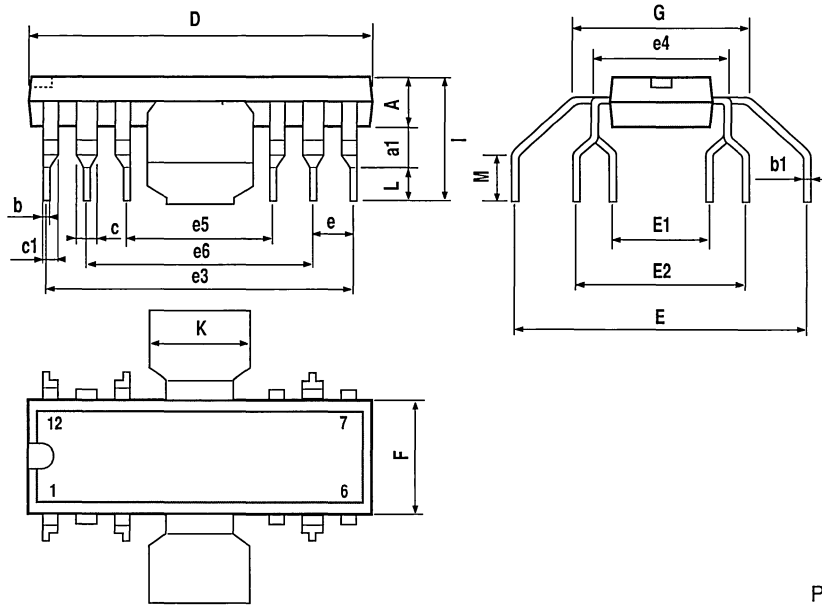
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.8		4.05	0.150		0.159
a1	1.5		1.75	0.059		0.069
b	0.55		0.6	0.022		0.024
b1	0.3		0.35	0.012		0.014
c		1.32			0.052	
c1		0.94			0.037	
D	19.2		19.9	0.756		0.783
E	16.8	17.2	17.6	0.661	0.677	0.693
E1	4.86		5.56	0.191		0.219
E2	10.11		10.81	0.398		0.426
e	2.29	2.54	2.79	0.090	0.100	0.110
e3	17.43	17.78	18.13	0.686	0.700	0.714
e4		7.62			0.300	
e5	7.27	7.62	7.97	0.286	0.300	0.314
e6	12.35	12.7	13.05	0.486	0.500	0.514
F	6.3		7.1	0.248		0.280
G		9.8			0.386	
I	7.8		8.6	0.307		0.339
K	6.1		6.5	0.240		0.256
L	2.5		2.9	0.098		0.114
M	2.5		3.1	0.098		0.122

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Findip

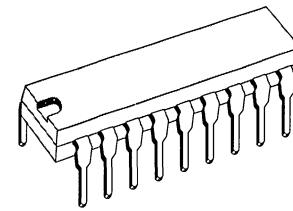


P001H

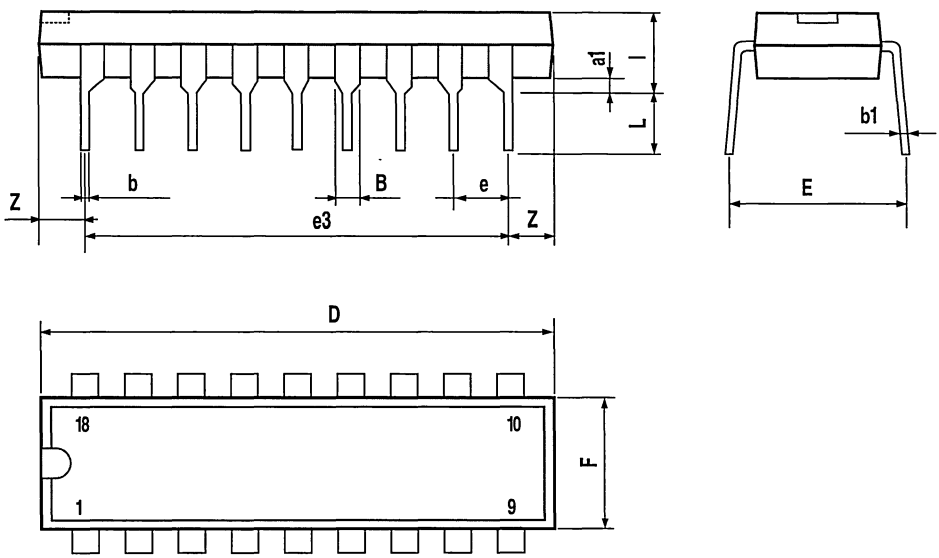
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			2.54			0.100

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP: (9+9), (12+3+3)

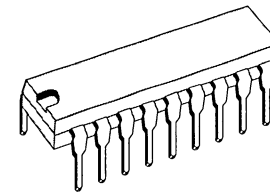


P001U

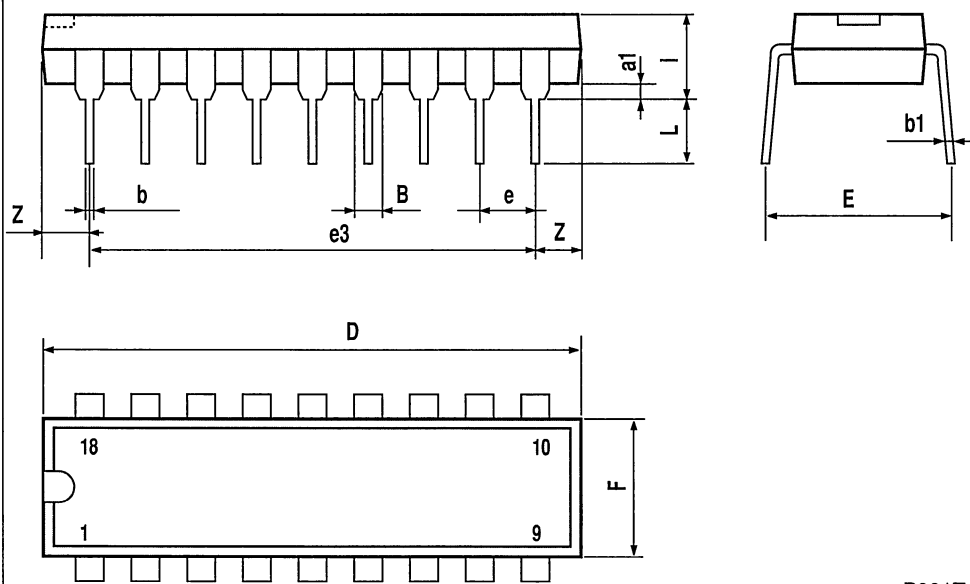
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.064
b		0.46			0.018	
b1		0.25			0.010	
D			23.24			0.914
E		8.5			0.335	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z		1.27	1.59		0.050	0.062

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP18 (0.25)

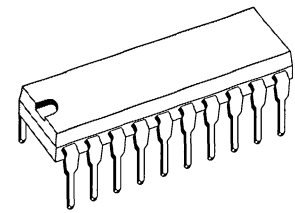


P001T

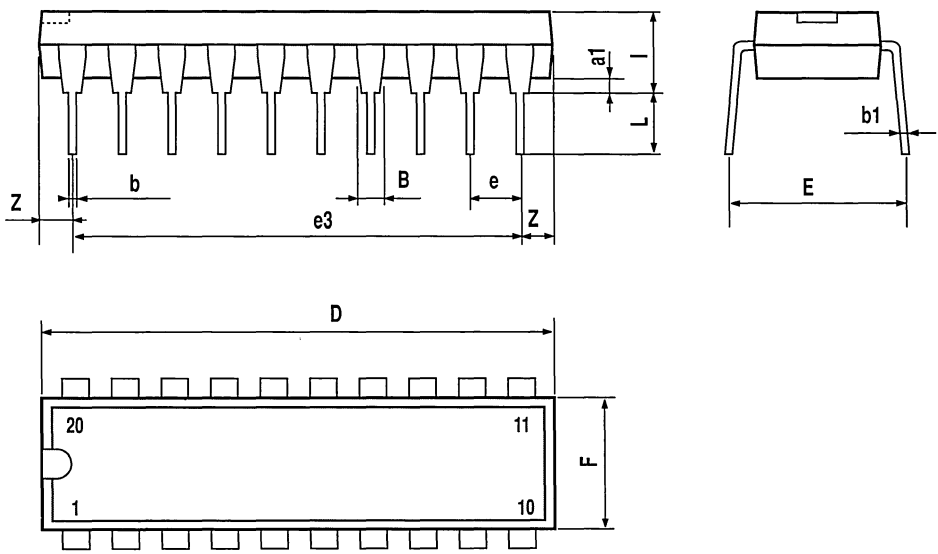
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP20 (0.25)

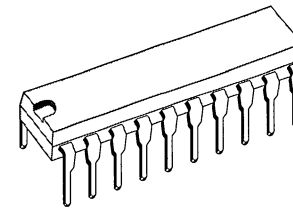


P001J

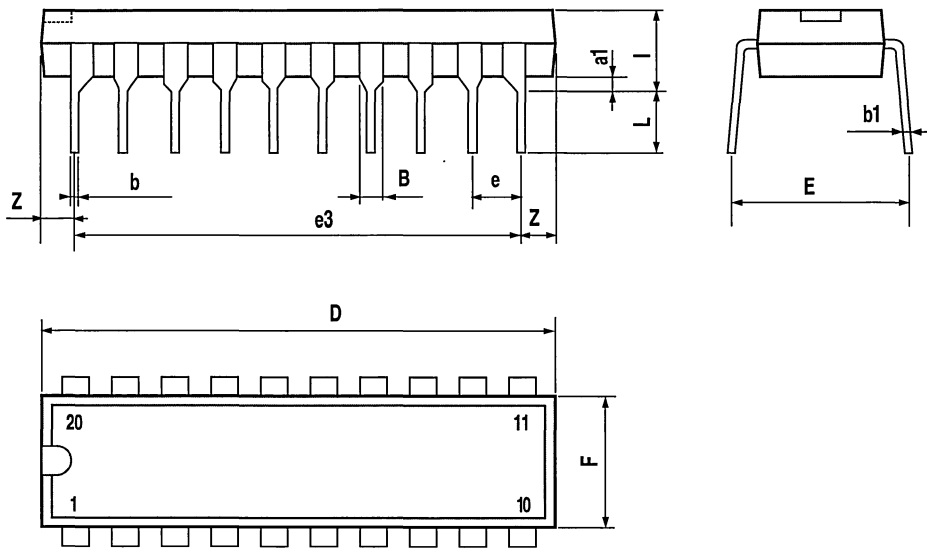
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP (16+2+2)

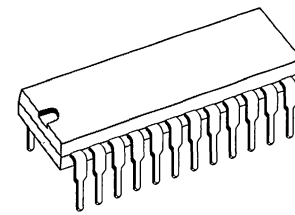


P001X

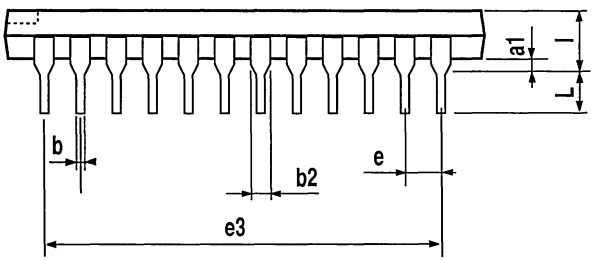
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

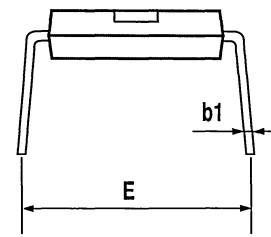
SGS-THOMSON MICROELECTRONICS

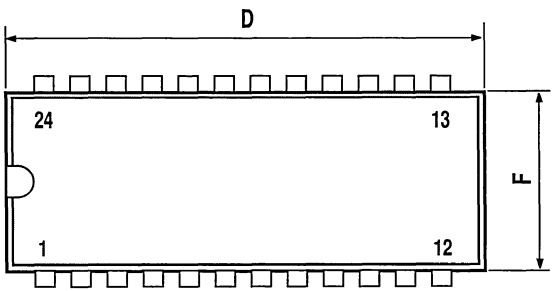
OUTLINE AND MECHANICAL DATA



DIP24 (0.25)





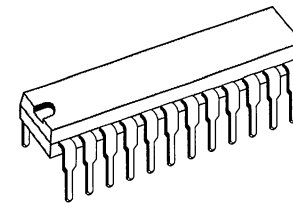


P043A

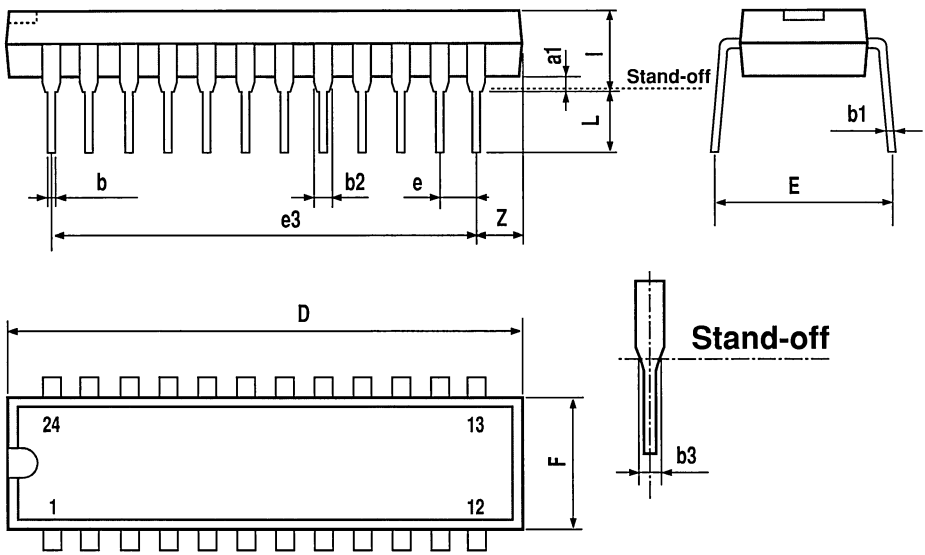
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.51			0.020		
b	0.35		0.59	0.014		0.023
b1	0.2		0.36	0.008		0.014
b2	0.75		1.42	0.030		0.056
b3	0.75			0.030		
D			23.11			0.910
E	7.95		9.73	0.313		0.383
e		1.778			0.070	
e3		19.558			0.770	
e4		7.62			0.300	
F			6.86			0.270
I			5.08			0.200
L	2.54			0.100		

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



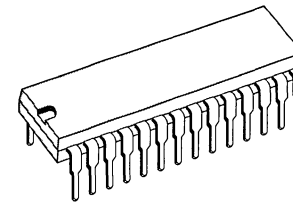
SDIP24



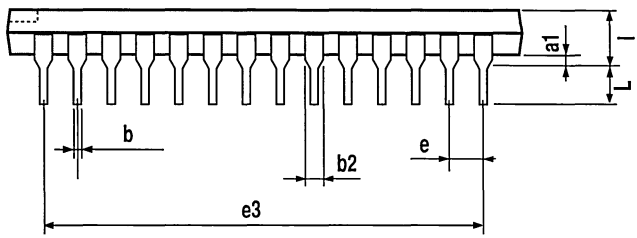
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

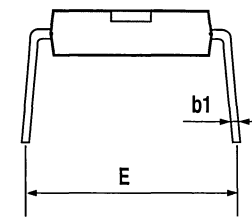
SGS-THOMSON MICROELECTRONICS

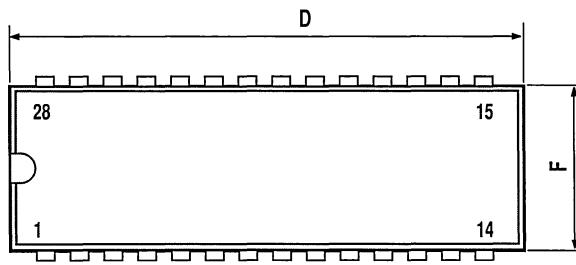
OUTLINE AND MECHANICAL DATA



DIP28





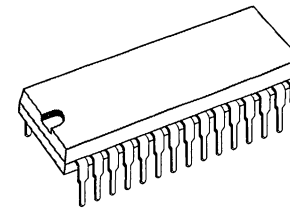


P043D

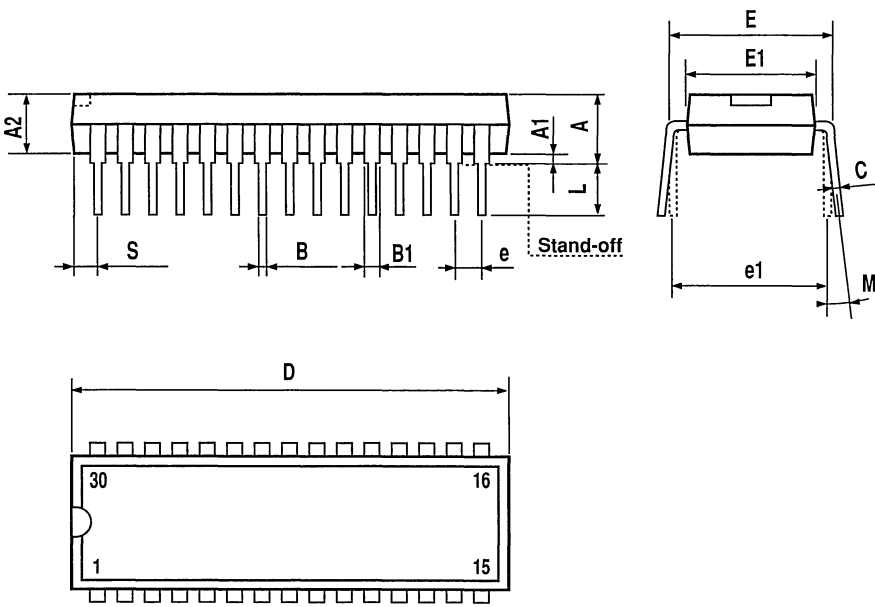
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.12	0.15	0.18
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	0.76	0.99	1.40	0.030	0.039	0.055
C	0.20	0.25	0.36	0.008	0.01	0.014
D	27.43	27.94	28.45	1.08	1.10	1.12
E	10.16	10.41	11.05	0.400	0.410	0.435
E1	8.38	8.64	9.40	0.330	0.340	0.370
e		1.78			0.070	
e1		10.16			0.400	
L	2.54	3.30	3.81	0.10	0.13	0.15
M	0°(min), 15°(max.)					
S	0.31			0.012		

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



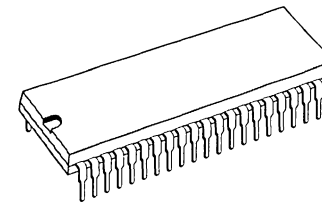
SDIP30



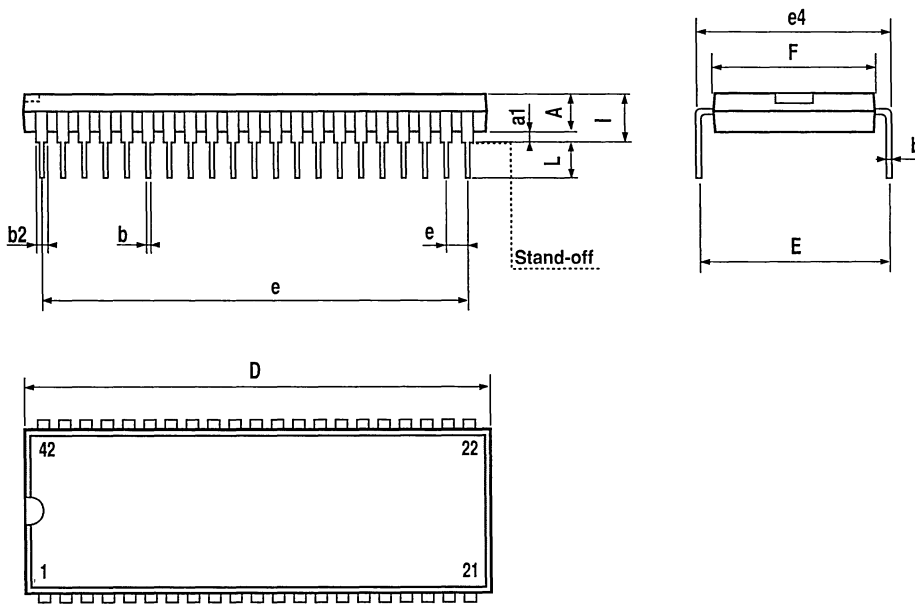
DIM.	mm			inch		
	MIN	TYP	MAX	MIN	TYP	MAX
A	3.30			0.130		
a1		0.51			0.020	
b		0.35	0.59		0.014	0.023
b1		0.20	0.36		0.008	0.014
b2		0.75	1.42		0.030	0.055
b3		0.75			0.030	
D			39.12			1.540
E		15.57	17.35		0.613	0.683
e	1.778			0.070		
e3	35.56			1.400		
e4	15.24			0.600		
F			14.48			0.570
I			5.08			0.200
L		2.54			0.100	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



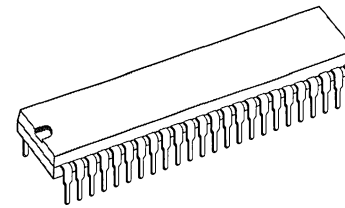
SDIP42



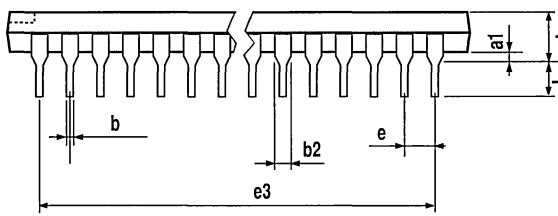
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			62.74			2.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		58.42			2.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

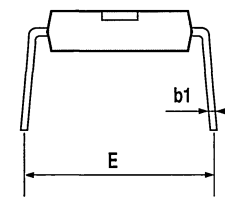
SGS-THOMSON MICROELECTRONICS

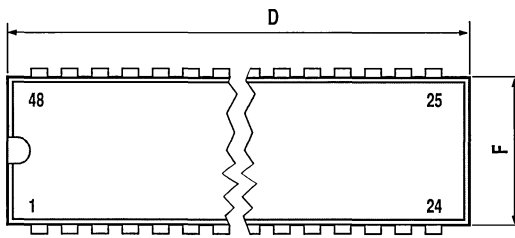
OUTLINE AND MECHANICAL DATA



DIP48





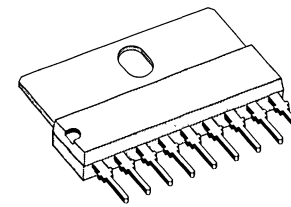


P043F

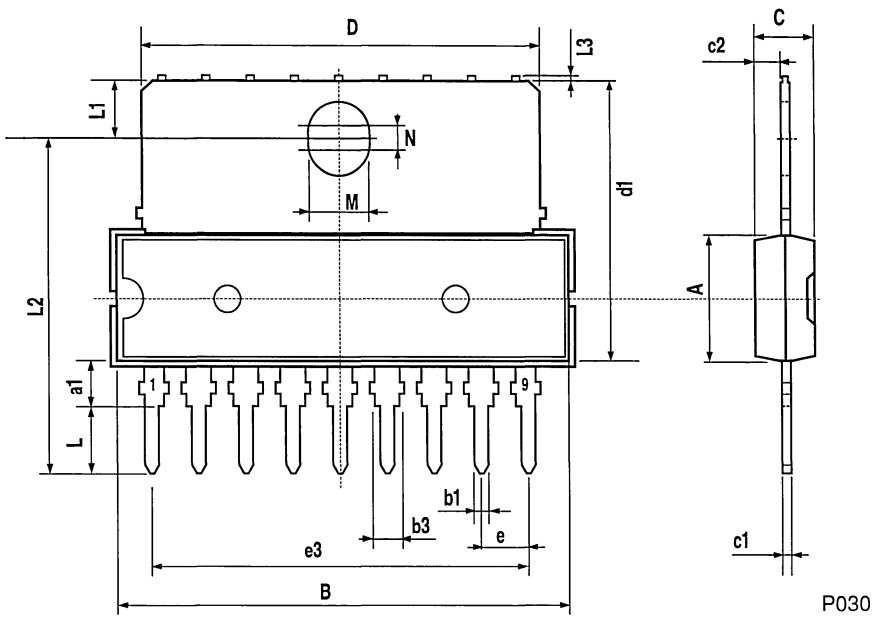
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



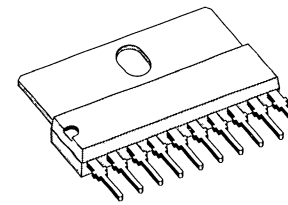
SIP9



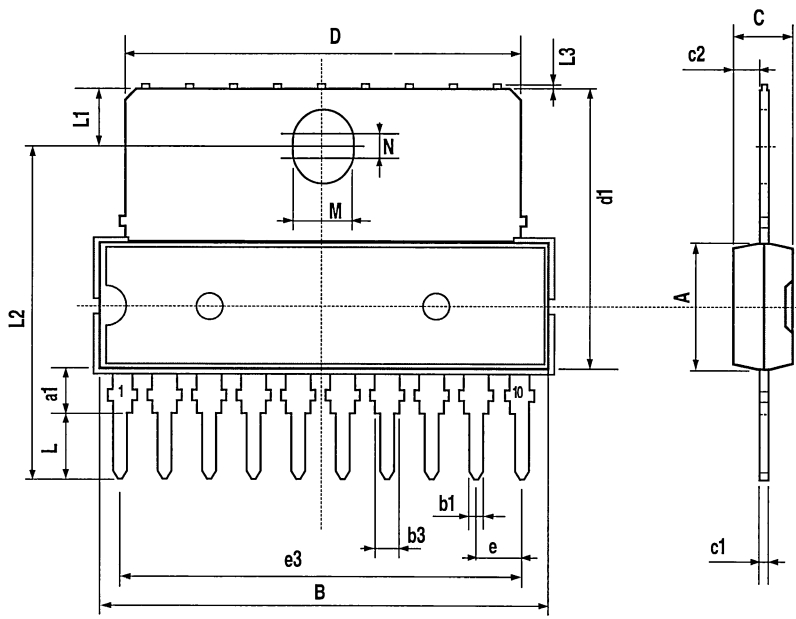
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			23.7			0.933
d1		14.5			0.571	
e		2.54			0.100	
e3		22.86			0.900	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



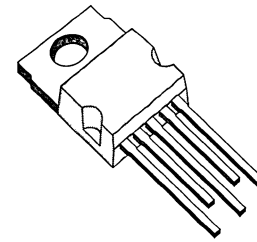
SIP10



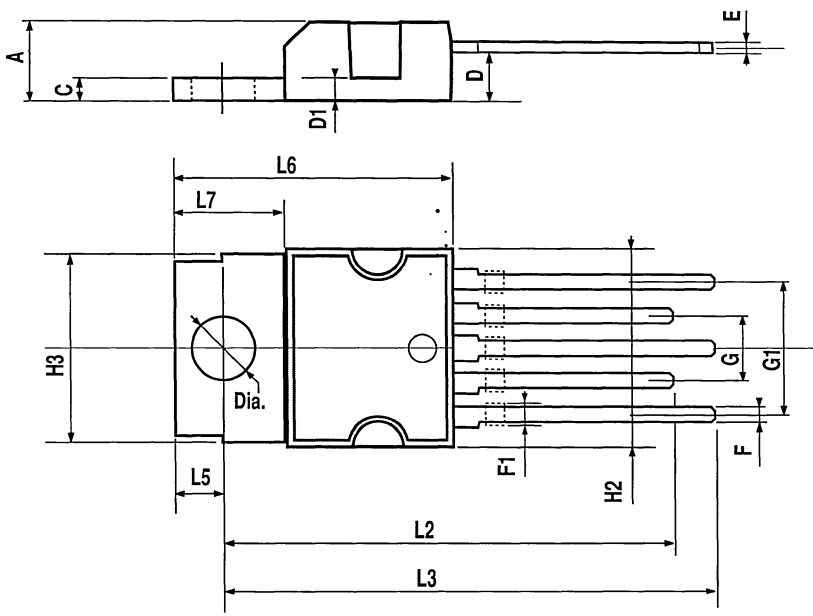
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L2	23.05	23.4	23.8	0.907	0.921	0.937
L3	25.3	25.65	26.1	0.996	1.010	1.028
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Pentawatt (In-Line)

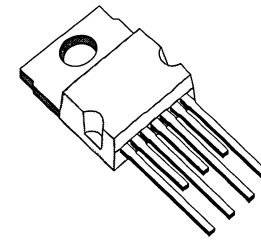


P010D

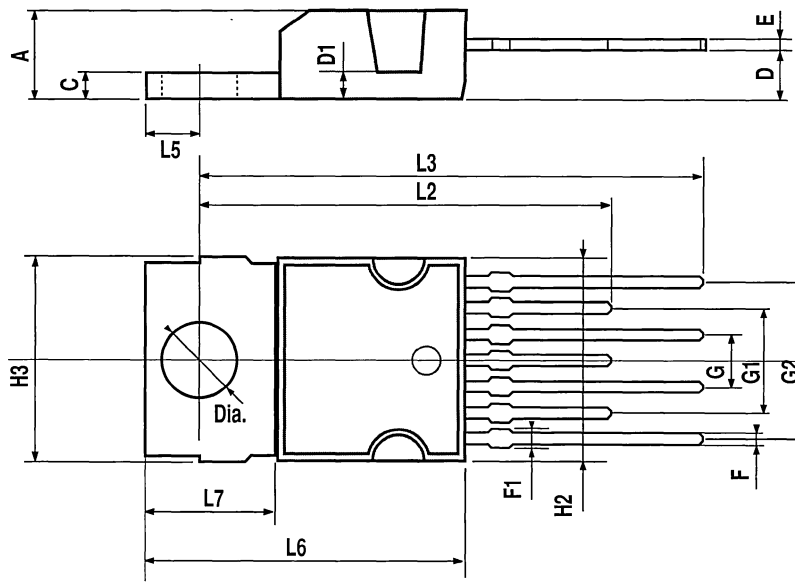
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L2	22.4		22.9	0.882		0.902
L3	25.4		26	1.000		1.024
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Heptawatt (In-Line)

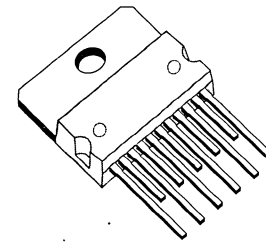


P023C

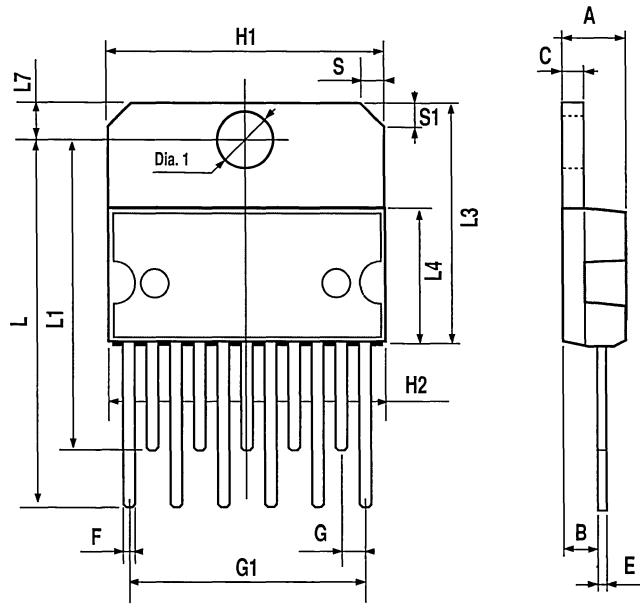
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.88		0.95	0.035		0.037
G	1.57	1.7	1.83	0.062	0.067	0.072
G1	16.87	17	17.13	0.664	0.669	0.674
H1	19.6			0.772		
H2			20.2			0.795
L	26.4		26.9	1.039		1.059
L1	22.35		22.85	0.880		0.900
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Multiwatt11 (In-Line)

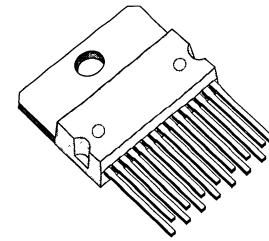


P017E

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	26.55		27.05	1.045		1.065
L1(*)	25.35		25.8	0.998		1.016
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

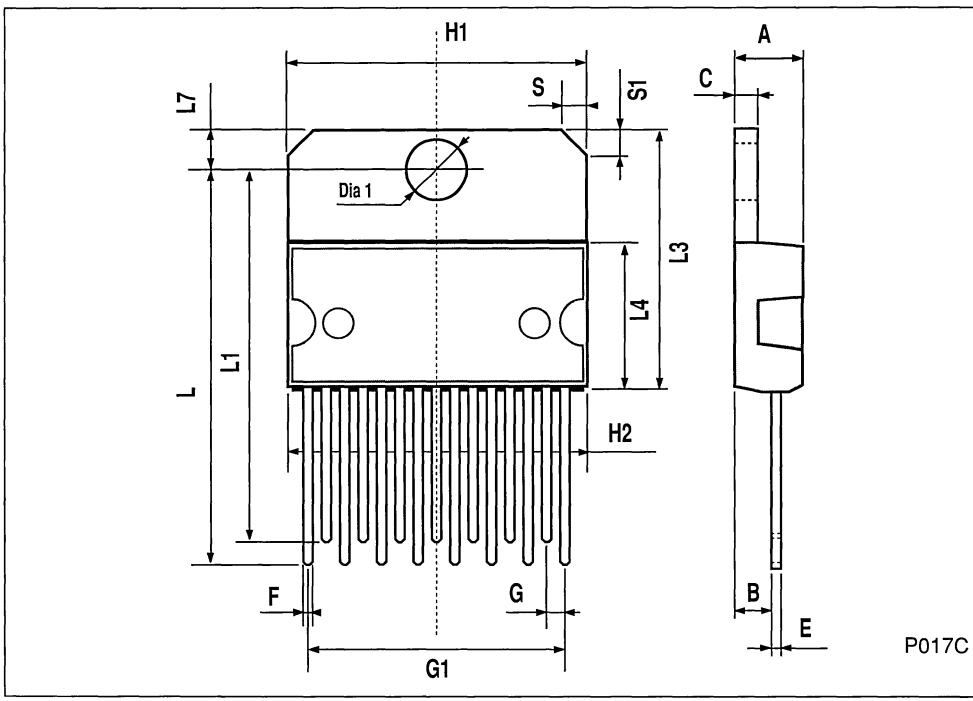
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Multiwatt15 (In-Line)

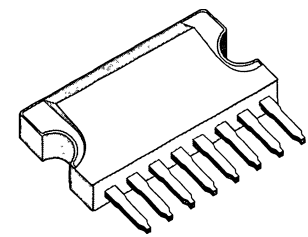
(*) For long Leads (22.35 min. and 22.8 max. for STD LEADS VERSION)



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.10			0.122
B			1.10			0.04
C		0.15			0.006	
D		3.50			0.14	
E		0.52			0.02	
F		0.80			0.03	
G		2.55			0.10	
G1		17.78			0.70	
H1		12.00			0.48	
H3		20.00			0.79	
L		15.90			0.62	
L2		11.00			0.43	

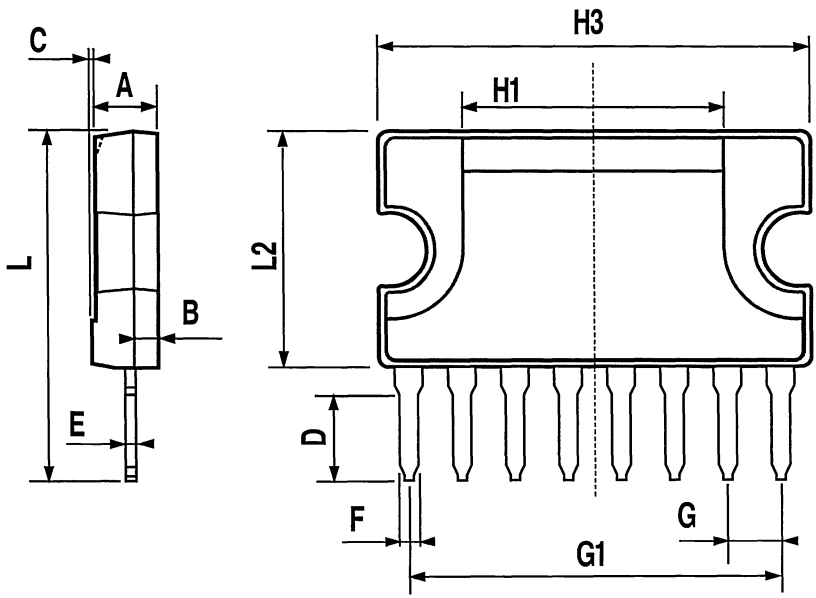
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Clipwatt8 (*)

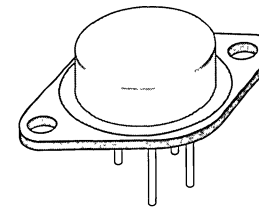
(*) Advanced information on a new package now in development or undergoing evaluation. Details are subject to change without notice.



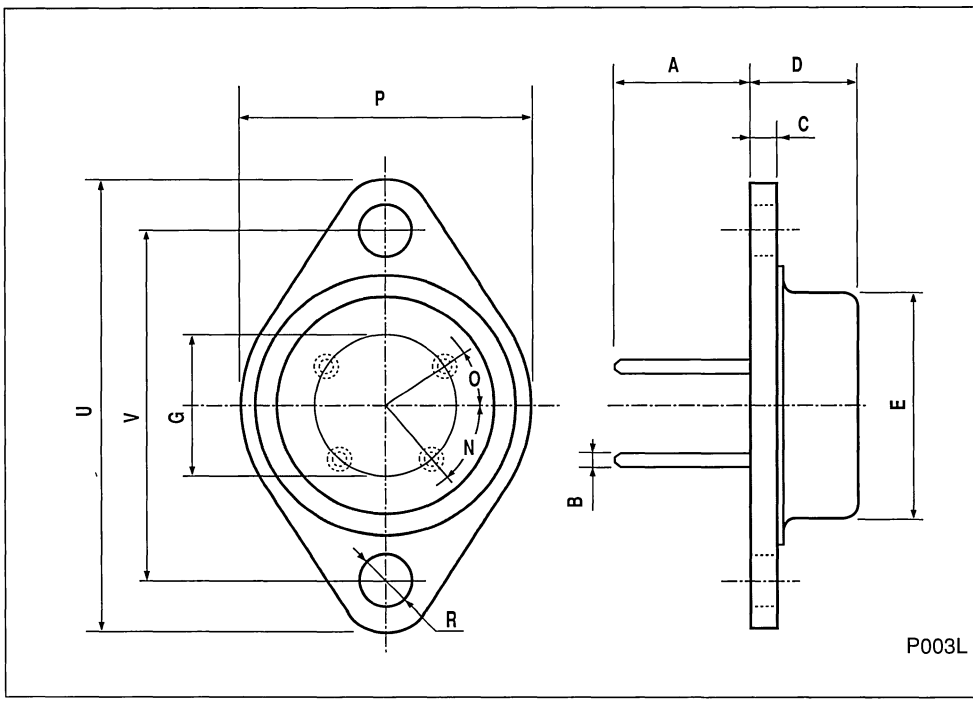
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		11.8			0.46	
B		1			0.39	
C			2.5			0.098
D			9.6			0.37
E			20			0.078
G		12.7			0.50	
N	50° (typ.)					
O	30° (typ.)					
P			26.2			1.03
R	3.88		4.20	0.15		0.16
U			39.5			1.55
V		30.1			1.18	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO3 (Four Leads)

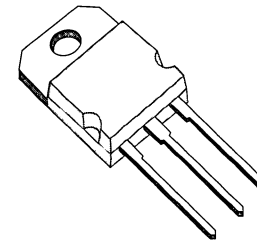


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		4.9	0.185		0.193
C	1.9		2.1	0.075		0.082
D		2.5			0.098	
E	0.5		0.78	0.019		0.030
F	1.1		1.3	0.043		0.051
G	10.8		11.1	0.425		0.437
H	14.7		15.2	0.578		0.598
L2	–		16.2	–		0.637
L3		18			0.708	
L5	3.95		4.15	0.155		0.163
L6		31			1.220	
R	–		12.2	–		0.480
Ø	4		4.1	0.157		0.161

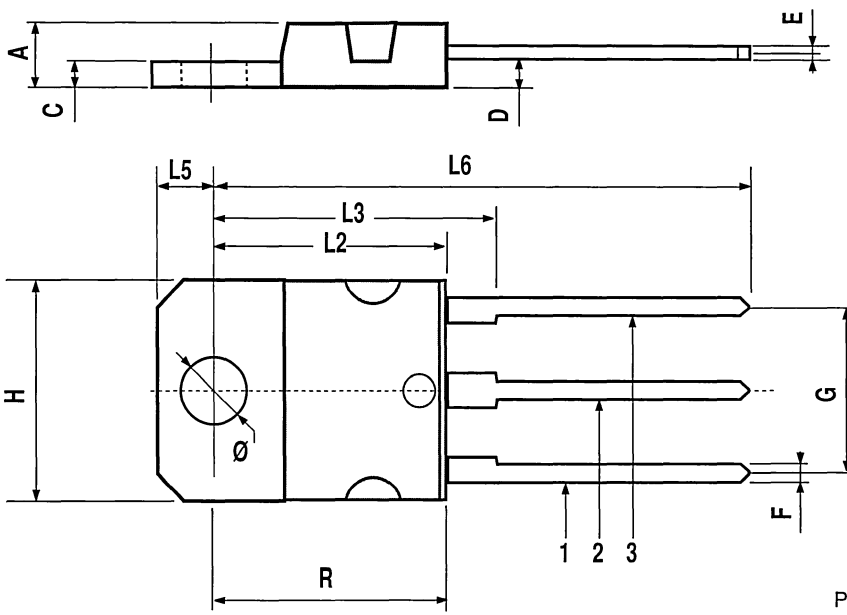
pin 1: Base - pin 2: Collector - pin 3. Emitter

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO218 (SOT-93)



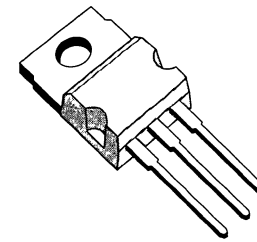
P025A

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.4		2.72	0.094		0.107
E	0.41		0.64	0.016		0.025
F	0.61		0.94	0.024		0.037
F1	1.14		1.7	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10		10.4	0.393		0.409
L2		17.6			0.692	
L4	12.7		13.7	0.500		0.539
L5	2.65		2.95	0.104		0.116
L6	15.2		15.9	0.598		0.626
L7	6.2		6.6	0.244		0260
L9	3.5		5.5	0.137		0.216
M	3.75		3.85	0.147		0.151

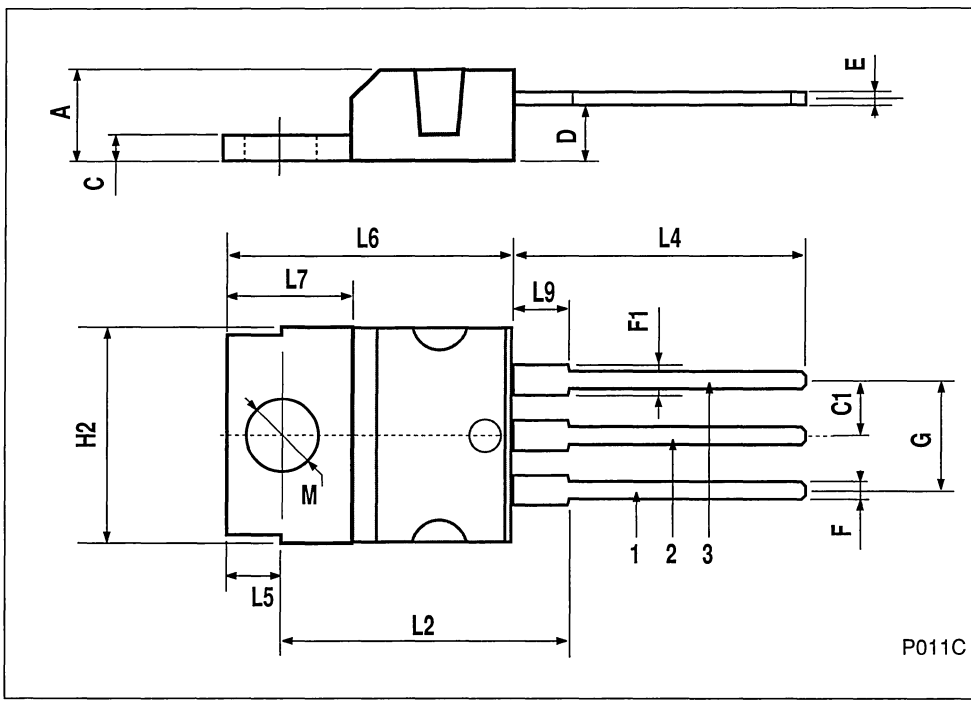
pin 1: Base - pin 2: Collector - pin 3: Emitter

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



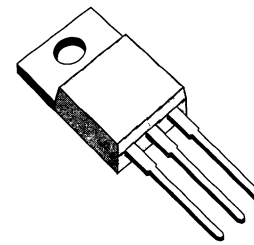
TO-220 (DSG)



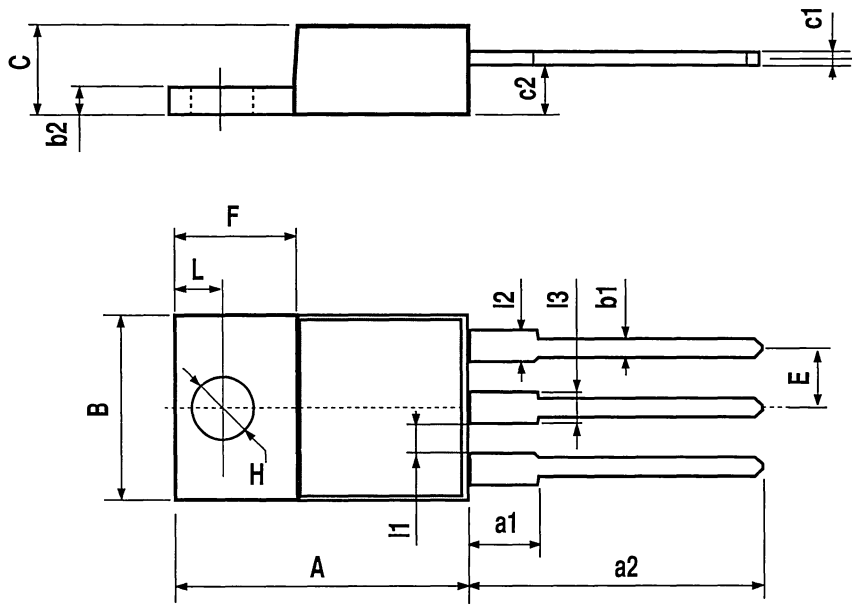
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	14.23	15.20	15.87	0.5933	0.5976	0.6031
a1			4.50			0.1311
a2	12.70		14.70	0.5522		0.5561
B	10.20	10.30	10.40	0.4028	0.4055	0.4083
b1	0.64	0.80	0.96	0.0311	0.0315	0.0327
b2	1.15	1.28	1.39	0.0494	0.0504	0.0516
C	4.48	4.65	4.82	0.1829	0.1831	0.1844
c1	0.35	0.50	0.65	0.0201	0.0209	0.0217
c2	2.10	2.40	2.70	0.0945	0.0953	0.0953
e	2.29	2.54	2.79	0.0984	0.1004	0.1024
F	5.85	6.30	6.85	0.2445	0.2480	0.2528
I	3.55	3.60	4.00	0.1413	0.1417	0.1425
L	2.54	2.80	3.00	0.1008	0.1024	0.1051
l1	1.30			0.0598		
l2	1.45	1.60	1.75	0.0575	0.0591	0.0665
l3	0.80	1.00	1.20	0.0335	0,0315	0.0394

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



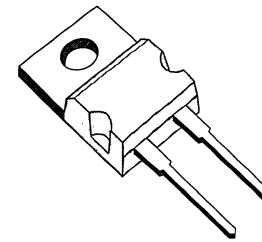
TO-220 AB



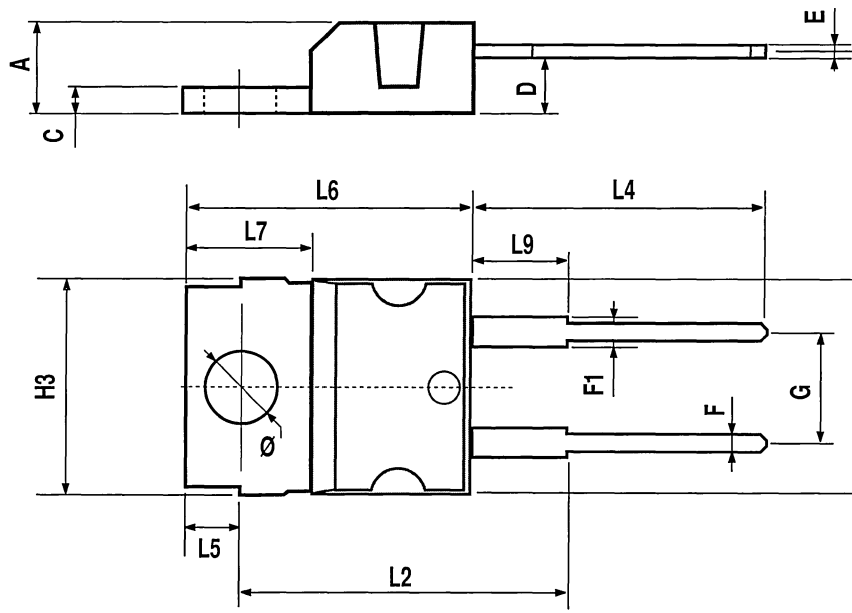
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4,40		4,60	0,1732		0,1811
B						
C	1,23		1,32	0,0484		0,0519
D	2,40		2,72	0,0944		0,1070
D1						
E	0,41		0,64	0,0161		0,0251
F	0,61		0,94	0,0240		0,0370
F1	1,14		1,70	0,0448		0,0669
G	4,95		5,15	0,1948		0,2027
H2	10,00		10,40	0,3937		0,4094
H3	9,70		10,40	0,3818		0,4094
L2		17,60			0,6929	
L4	12,70		13,70	0,5000		0,5393
L5	2,65		2,95	0,1043		0,1614
L6	15,20		15,90	0,5984		0,6259
L7	6,20		6,60	0,2440		0,2598

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO-220 AC

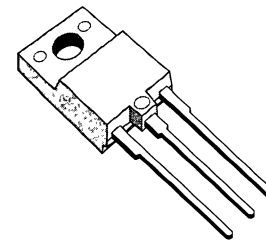


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	5.35		5.65	0.210		0.222
C	3.3		3.8	0.130		0.149
D	2.9		3.1	0.114		0.122
D1	1.88		2.08	0.074		0.081
E	0.45		1	0.017		0.039
F	1.05		1.25	0.041		0.049
G	10.8		11.2	0.425		0.441
H	15.8		16.2	0.622		0.637
L1	20.8		21.2	0.818		0.834
L2	19.1		19.9	0.752		0.783
L3	22.8		23.6	0.897		0.929
L4	40.5		42.5	1.594		1.673
L5	4.85		5.25	0.190		0.206
L6	20.25		20.75	0.797		0.817
M	3.5		3.7	0.137		0.145
N	2.1		2.3	0.082		0.090
U		4.6			0.181	

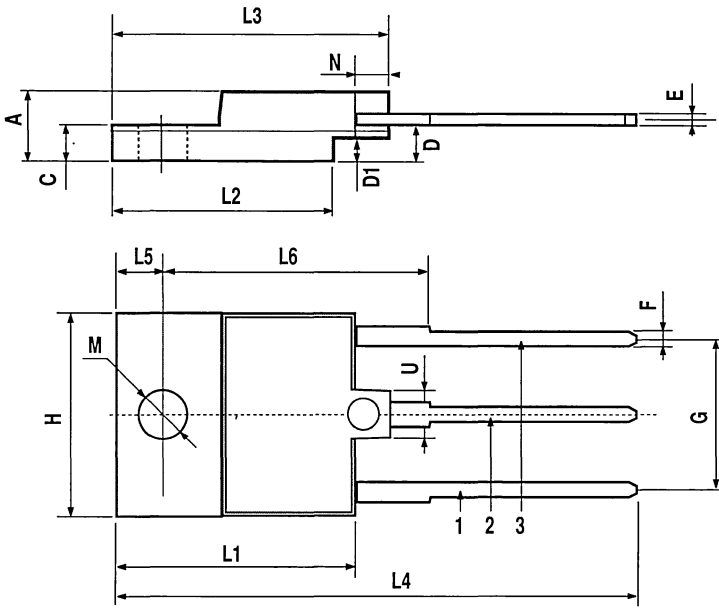
pin 1: Base - pin 2: Collector - pin 3: Emitter

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



ISOWATT 218



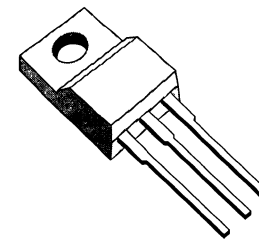
P025C

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.4		2.75	0.094		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		3.66
Ø	3		3.2	0.118		0.126

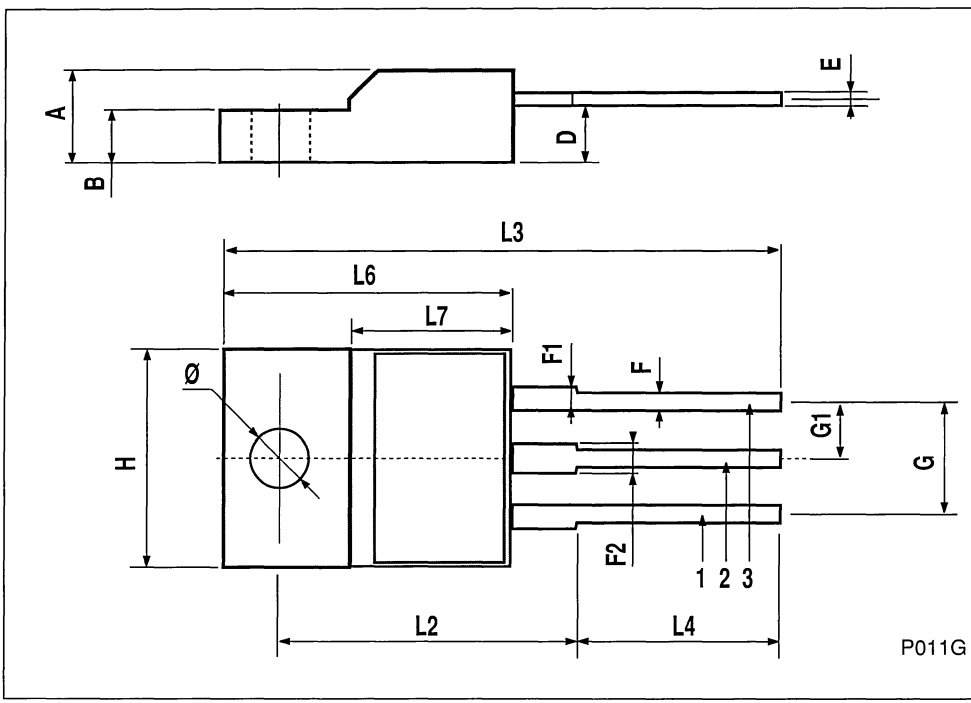
pin 1: Base - pin 2: Collector - pin 3: Emitter

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



ISOWATT220



NOTES

NOTES

NOTES

EUROPE

DENMARK

2730 HERLEV
Herlev Torv, 4
Tel (45-42) 94 85 33
Telex 35411
Telefax (45-42) 948694

FINLAND

LOHJA SF-08150
Karjalankatu, 2
Tel (358-12) 155 11
Telefax (358-12) 155.66

FRANCE

94253 GENTILLY Cedex
7 - avenue Gallieni - BP 93
Tel (33-1) 47 40 75 75
Telex 632570 STMHQ
Telefax (33-1) 47 40 79 10

67000 STRASBOURG
20, Place des Halles
Tel (33) 88 75 50 66
Telex 870001F
Telefax (33) 88 22 29 32

GERMANY

6000 FRANKFURT
Gutleutstrasse 322
Tel (49-69) 237492-3
Telex 176997 689
Telefax (49-69) 231957
Teletex 6997689=STVBP

8011 GRASBRUNN
Bretonischer Ring 4
Neukeferloh Technopark
Tel (49-89) 46006-0
Telex 528211
Telefax (49-89) 4605454
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Telefax (04) 379816

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8th floor Shinwon Building
823-14, Yuksam-Dong
Kang-Nam-Gu
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Telex SGSKOR K29998
Telefax (82-2) 552-1051

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Telex RS 55201 ESGIES
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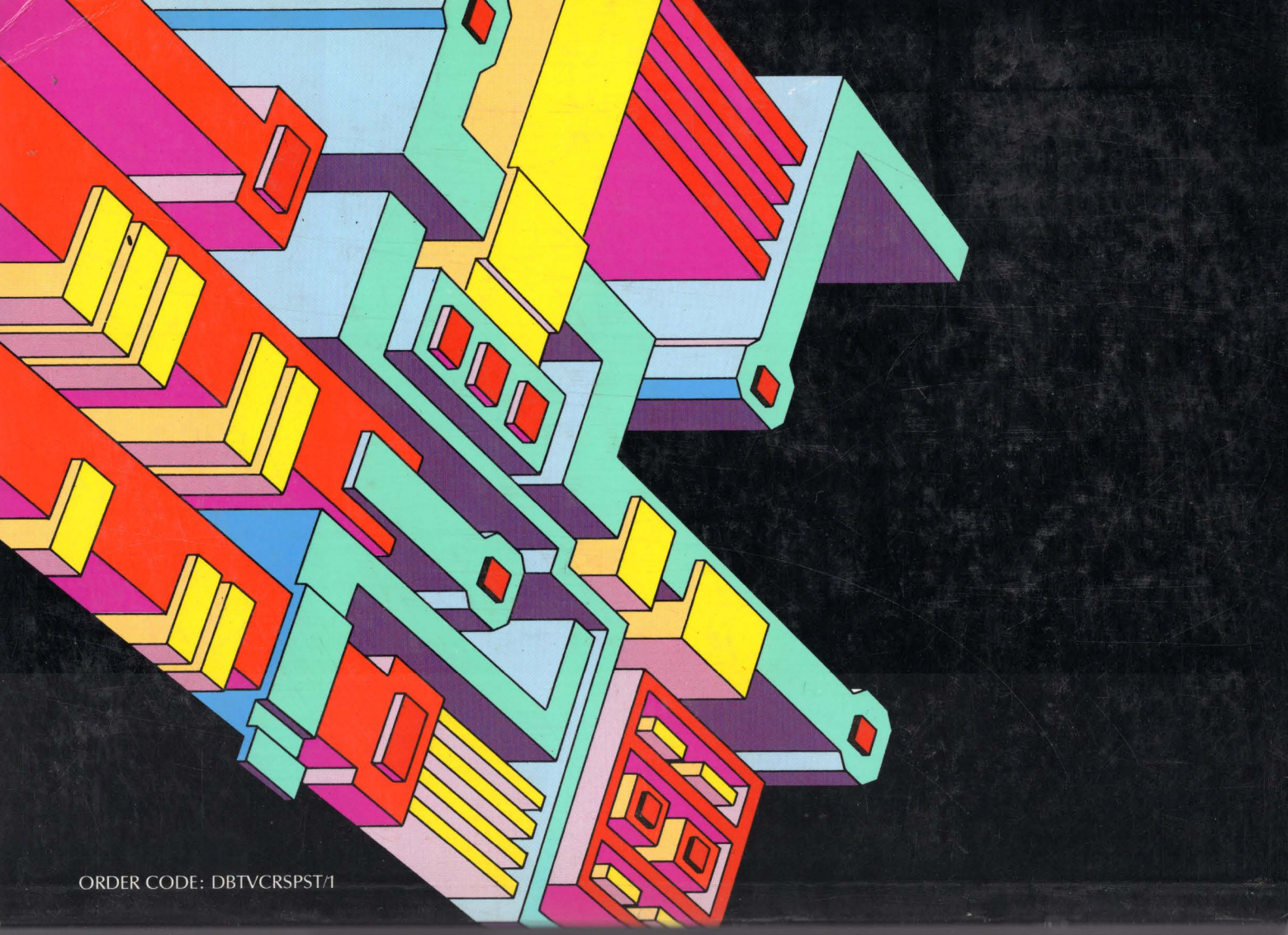

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