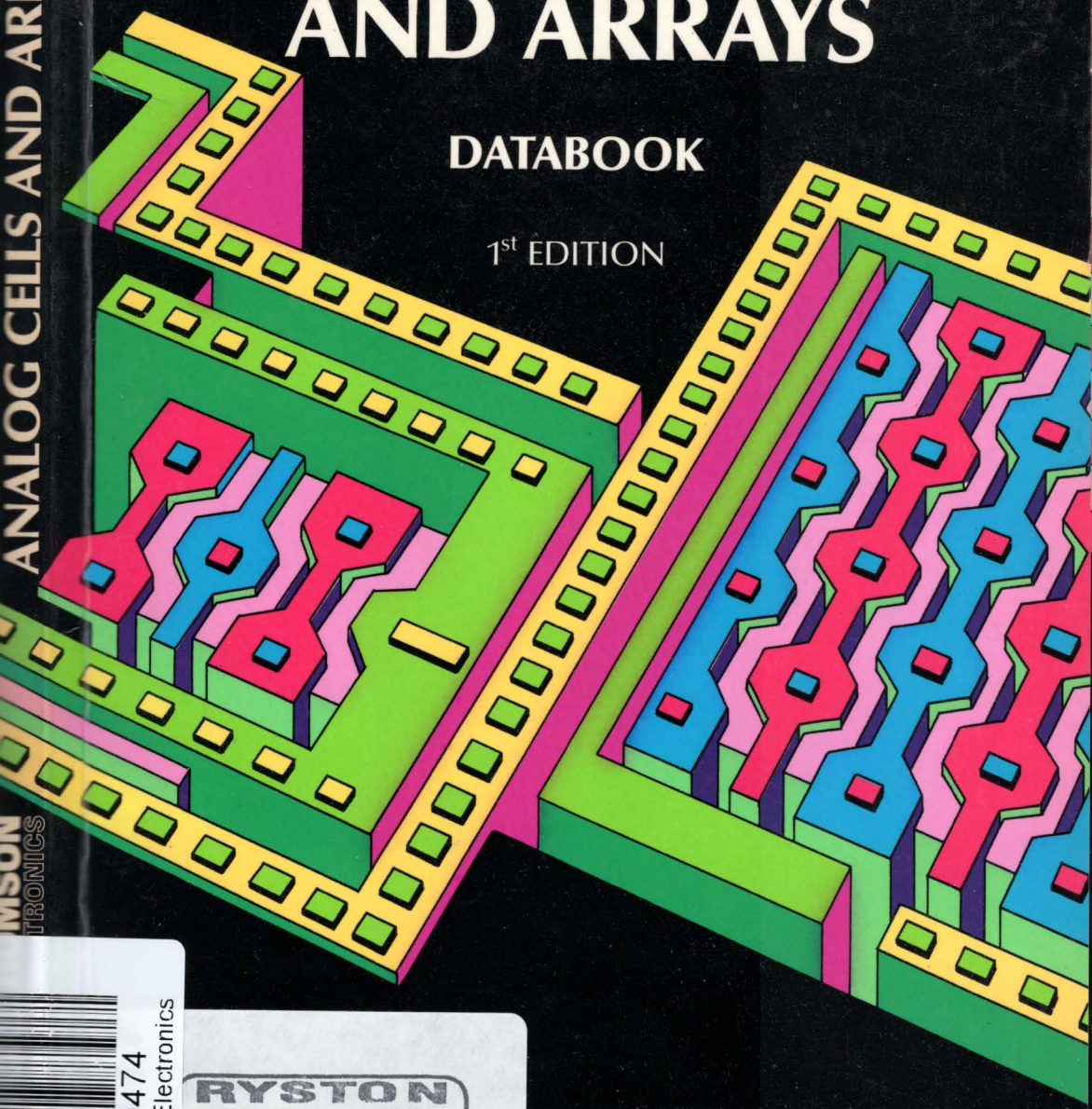
ANALOG CELLS AND ARRAYS

DATABOOK

1st EDITION



SGS-THOMSON MICROELECTRONICS

ANALOG CELLS AND ARRAYS

DATABOOK

1st EDITION

FEBRUARY 1991

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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SGS-THOMSON Microelectronics Semicustom Product Portfolio - 1991

Family	Product	Process	Complexity/ Density	Features
Sea Of Gates	ISB9000	CMOS 1.5µm, DLM	300 to 14,000 Gates	Cost Effective
Sea Of Gates	ISB12000	CMOS 1.2µm, DLM	2,000 to 50,000 Gates	Performance and Density
Sea Of Gates	ISB18000	CMOS 0.8µm, DLM	2.000 to 21,000 Gates	Bus Optimized Array
Standard Cells	CB200	CMOS 1.5µm, DLM	250 Gates/mm^2,	
Standard Cells	CB12000	CMOS 1.2µm, DLM	500 Gates/mm^2	Compilers
Analog Arrays	Polyuse K	Bipolar 3µm, SLM	906 Components	3GHz NPN
Mixed A/D Arrays	Polyuse J	Bipolar 3µm, DLM	400-23000 Components	3GHz NPN
Filter Arrays	TSGF	CMOS 3µm, SLM	4 to 12th Order	DC-30KHz
Mixed A/D Standard Cells	TSGSM	CMOS 3.5µm, SLM	1Kgates + Analog,	
Mixed A/D Standard Cells	STKM2000	BiCMOS 2µm, DP, DLM	10Kgates + Analog	6GHz NPN

THE COMPANY

SGS-THOMSON Microelectronics is a broad-range supplier of advanced semiconductor products. With extensive manufacturing capability in Europe, North-America and the Far-East, the company is dedicated to meeting customer needs with cost effective, world-class technologies and products.

The company is ranked 12th worldwide in semiconductor suppliers on a global basis with total 1990 revenues of 1.5 billion dollars* and over 18000 employees world-wide.

With 17 production locations, 24 design centers and 8 advanced research and development sites, the company continues to demonstrate its commitment to excellence in technology and products. Additionally, with 50 direct sales offices, and over 600 distributors and sales representatives, customers are never far from the service and support needed to be successful in utilizing these products.

With Research and Development expenditure as well as capital investment well above the industry average, SGS-THOMSON Microelectronics is dedicated to bring an increasing portfolio of innovative and advanced new products with the service level needed to succeed in today's and tomorrow's electronics.

The Analog Cells and Arrays Business Unit offers several families of linear and mixed analog digital arrays and standard-cells including the industry's most advanced offering in BiCMOS analog/digital standard-cells. The complete semicustom product portfolio also includes digital standard-cell continuous arrays and channelless arrays.

THE PRODUCTS

Linear and Mixed Arrays

The arrays are either purely linear (K09 array) or mixed analog-digital tile arrays (Polyuse J series).
Aimed at cost-sensitive industrial, automotive and computer peripherals application requiring a combination of analog and digital functions, the Polyuse J series is based on a high frequency bipolar process (3 GHz NPN)
The family includes 5 arrays ranging from 400 to 2300 components, each array containing functional tiles such as linear tile (op-amp or comparator functions) ECL tile (level shifter, frequency divider), I^2L tile (logic functions), PWR tile (high-current driver) and other functions such as voltage reference and resistor networks.

Filter Arrays

The TSGF family is a range of mask programmable switched capacitor filters. Filter parameters (gain, bandwidth gauge) are fully programmable and personalized by one mask layer. Three prediffused arrays allow the implementation of filters from 2nd up to 12th order. Powerful and easy to use CAD software allows any filter configuration to be implemented with very fast turn-around time.

* Source Dataquest 1/91

CMOS Analog/Digital Standard Cells

The TSGSM series of analog/digital standard-cells is based on a silicon gate, P-well, dual polysilicon layer process allowing high performance analog functions to be mixed with 10MHz digital circuitry.
The analog capability allows the integration of switched-capacitor filters. The cell library includes 94 digital cells and more than 60 analog cells. The large variety of predefined and characterized functions ranges from basic building blocks such as gates and op-amps to complex functions such as A/D and D/A converters.

BiCMOS Analog/Digital Standard Cells

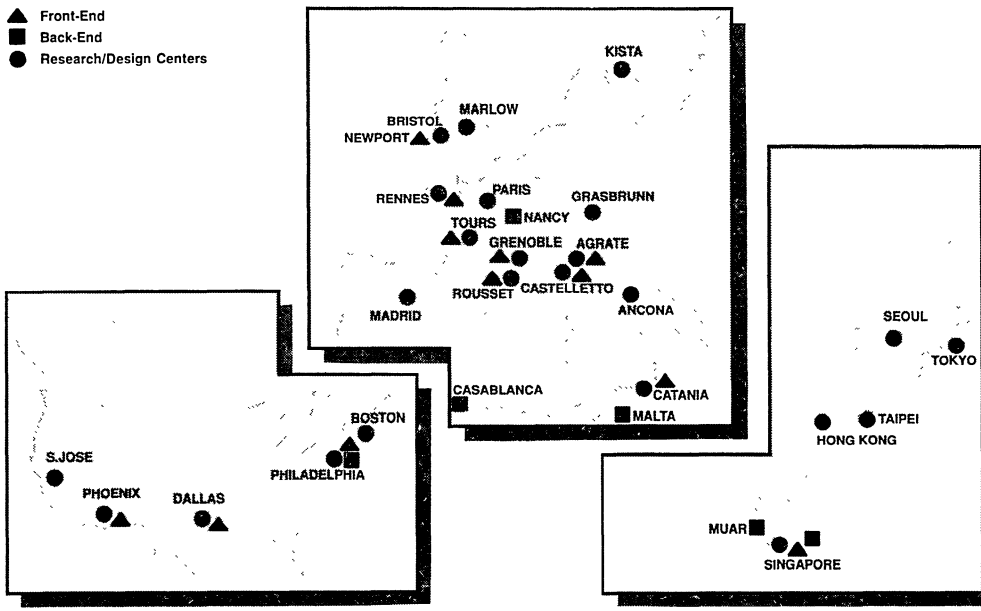
The STKM2000, the world's first true mixed signal BiCMOS standard cell family was introduced by SGS-THOMSON in 1989. Key features of this family include true mixed Bipolar-CMOS process operating at voltages from 3 to 10V, a comprehensive library of high-performance, high-accuracy analog and high-speed digital functions and state-of-the-art CAD support that offers the first practical implementation of analog compilers.
The family is based on a 2 micron, double metal, double poly process. The CMOS part allows the implementation of high-speed like digital functions as well as analog functions operating between 3 and 10V. The available Bipolar devices include 6 GHz NPN transistors, 50MHz lateral PNP transistors and 2.5 GHz vertical PNP transistors.

The library offers more than 60 CMOS digital cells and more than 100 analog cells which can be either CMOS, Bipolar or BiCMOS. All cells have power down capability. In addition to the standard Op-Amps, Comparators, Voltage Reference functions, the library includes advanced functions such as compiled filters, A/D converters (up to 12 bits) and D/A converters. Compilers for RAM, ROM and PLA are also available in the digital library.
This family is supported on the most popular CAD workstations to allow the widest range of designers to have access to this exciting new technology.

SUPPORT

With an extensive network of Design Centers, customers from all the major countries can obtain support for feasibility studies, architecture analysis and design.

These design centers are fully equipped with Design capability and their computers are interconnected with the center to allow efficient design transfer and fast response time.



ALPHANUMERICAL INDEX

APPLICATION NOTE

MIXED ANALOG-DIGITAL STANDARD CELLS

SGS-THOMSON MICROELECTRONICS

STKM2000 SERIES

2 µm/2 POLY/2 METAL BiCMOS MIXED ANALOG-DIGITAL STANDARD CELLS

FEATURES

- ADVANCED BICMOS 2 µm/2 POLY/ 2 METAL PROCESS
- TWIN TUB PROCESS
- HIGH LATCH-UP IMMUNITY
- POWER SUPPLY :
  - Maximum Rating : -0.5V to 12V
  - Operating Conditions : 3V to 10V (typ.)
- MIXED ANALOG - DIGITAL LIBRARY :
  - Analog Bipolar Library
  - Analog CMOS Library
  - Analog BiCMOS Library
  - Digital CMOS Library
- HIGH PROCESS PERFORMANCES:
  - Transition Frequency, NPN = 6 GHz
  - Vertical PNP = 2.5 GHz
  - Digital CMOS Operating Frequency Up to 30MHz
- CAD SOFTWARE SUPPORT:
  - Fully Integrated A.D.S. (Analog Design System) with Analog Block Generators, Switched Capacitor Filter Compiler; Digital Functions Generator, Ram, Rom, Pla Generators
- AVAILABILITY OF EEPROM DEVICES, ZENER DIODE.
- OPERATING TEMPERATURE RANGE:
  - Commercial: 0 to 70°C
  - Industrial: -40 to 85°C
  - Military: -55 to 125°C
- PACKAGE OPTIONS:
  - DIL: Plastic or Ceramic
  - SMD: SO, PLCC, QFP
  - Wafer or Die

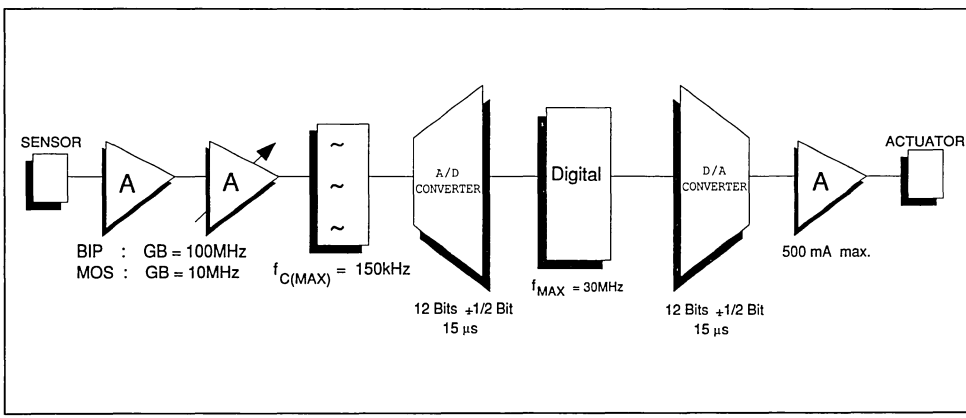
ASIC PRODUCT DESCRIPTION

With the STKM2000 series, SGS-THOMSON Microelectronics introduces the "state of the art" product for analog signal processing, from sensor to actuator.

The introduction of new concepts (cells library and CAD) opens the design of analog functions and mixed analog and digital circuits with a safe and powerful approach. This new ASIC approach is the combination of innovative :

- BiCMOS process
- Mixed libraries (ANALOG + DIGITAL)
- Generators and compilers
- "User friendly" CAD system
- Customer interface

Figure 1 : The STKM2000 Series, a complete system solution



STKM2000 ARCHITECTURE

Technology

The STKM2000 Series developed by SGS-THOMSON Microelectronics uses an advanced BICMOS silicon gate process with dual polysilicon layers and dual metal layers. This process is optimized to achieve high performance in digital CMOS applications. Depending on the operating supply voltage (10V, or 5V), the CMOS process behaves as an N-WELL technology (respectively with 3 µ gate length or 1.8 µ gate length) with operating speeds up to 30MHz. Thanks to the two metal layers, the digital part of the circuit can reach high gate density with low parasitic capacitances.

For analog functions, the STKM2000 series takes advantage of the bipolar structure:

- very high speed NPN transistor : $f_T = 6$ GHz
- very high speed vertical PNP : $f_T = 2.5$ GHz

This allows high gain - bandwith operational amplifier (80 MHz), low noise input amplifier, short propagation delay comparator, ...
With the same BICMOS process, the analog CMOS performance come from the high density CMOS structure with a double poly layer for accurate capacitors, low consumption CMOS amplifier (30 µA), CMOS switches, high accuracy switched capacitor filters (up to 100 kHz for center frequency).

STKM2000 Cell Concepts

SGS-THOMSON Microelectronics has predesigned and precharacterized cells which are selected, placed and interconnected on the chip to implement digital and analog cells having different height and supply voltages. In addition some macrocells are designed as fixed blocks, so called "hard blocks" : filters, A/D and D/A converters; some hard blocks are automatically generated and parametrized from a compiler: S.C. filters, PLA, RAM, ROM...

STKM2000 Chip Topology

The chip is optimized versus the cell complexity, in a row based structure with different heights.

Peripheral cells surround the internal active chip area to interface with its external environment.

Despite the row based architecture, "hard blocks" can be implemented with efficient floor planning organization.

STKM2000 Cell Libraries

SGS-THOMSON Microelectronics introduces the "programmable" library; instead of working with a finite number of cells of the library, the designer has now access to an infinite number of functions.

Defining only some properties, the designer is able to create himself the cells needed for his application. For example, the following electrical parameters are accessible and adjustable:

- gain-bandwith product
- phase margins, frequency compensation
- output buffer current
- biasing currents
- resistor, capacitor fields
- current, source or sink
- adjustable Ron switch resistor
- supply voltage assignment

The analog library is operating in a large voltage range: 3V to 10V (typ).

The basic analog library contains:

- 60 analog CMOS functions
- 25 analog BIPOLAR functions

From single transistor to 12 bits A to D converter , each setup becomes possible.

The digital CMOS library uses the same flexibility with a complete set of basic digital functions (NAND, NOR, Flip-Flop, ...) and some cell generators:

- register, counter, logic comparator, ...

More than 60 digital cells are available.

Figure 2: The STKM2000 Series, a complete system solution

ANALOG LIBRARY

- NPN transistor
- Lateral PNP
- Substrate PNP
- Isolated PNP
- MOS or bipolar input comparators
- N-MOS transistor
- P-MOS transistor
- NPN high-speed amplifier
- MOS or bipolar input, internal or external Op–Amp
- Crystal oscillator
- RC oscillator
- Transconductance amplifier
- Power-on reset (with adjustable threshold and hysteresis)
- Analog multiplexer
- Voltage to current converter
- Voltage references
- 8 bit A/D and D/A converters
- 12 bit A/D converters

DIGITAL LIBRARY

- AND, NAND, OR, NOR, inverter
- Exclusive OR, NOR
- D latch, D flip-flop
- Input buffer (TTL/CMOS)
- Output buffer (TTL/CMOS)
- Shift register
- Binary counter
- Decimal counter
- Magnitude comparator
- RAM, ROM, PLA, EEPROM*

* EEPROM under qualification (available Q2/91)

CAD SUPPORT: A.D.S. (Analog Design System) SGS-THOMSON Microelectronics has introduced a sophisticated CAD approach to reduce the development leadtime and to increase design flexibility and safety.

Programmable cells in the library are defined as:
- alternative cell
- adjustable cell
- telescopic cell
- parametrisable cell

Some specific parts of the design are automatically handled by an analog design manager, in order to:

- reduce capture errors
- make the unexperienced designer's task easier
- improve schematics legibility
- check electrical design rules (Analog or Digital)

The Analog Design manager takes into account:
- transconductance block generation
- automatic cell biasing
- unconnected pins and power down processing
- multipower supplies processing

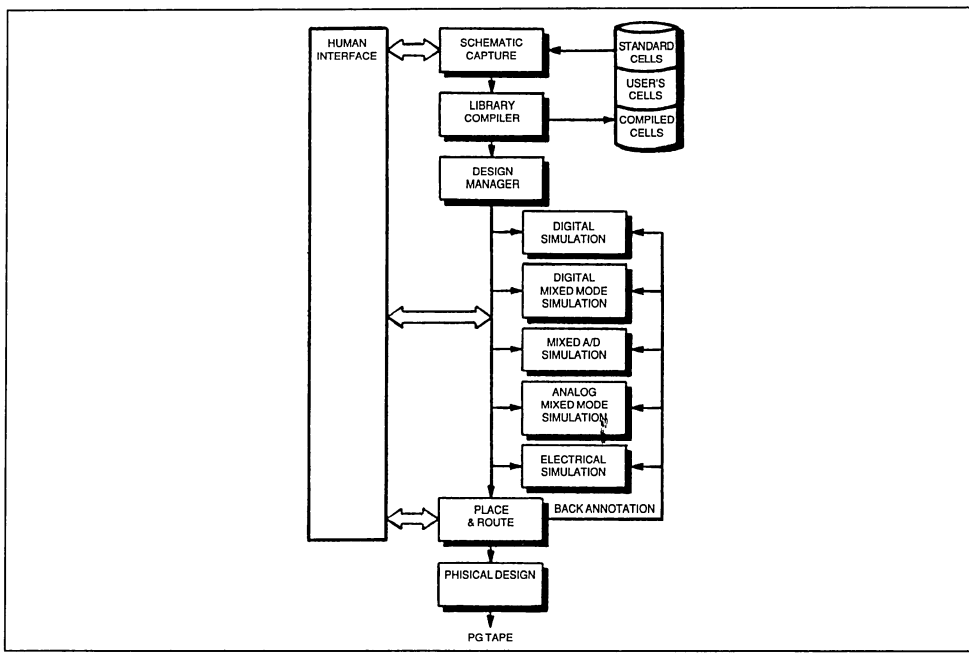
A major step has been made with the introduction of function generator and compiler approaches to improve design automation and design efficiency.

Operational Amplifier Generator
From a generic symbol and some properties, several parameters of the amplifier will be adjusted:

- Biasing current which controls major parameters of amplifier (gain-bandwidth, slew rate, power consumption).
- Frequency compensation which allows to adjust and optimize the dynamic parameters versus the capacitive and resistive load.
- Power down capabilities.
- Supply voltage of the cell.

A specific software program manages all these properties and automatically updates all libraries included in the design flow: macro models and transistor level models, footprint, GDS2 layout, LVS netlist.

Figure 3: Analog Design System (A.D.S.) flow



Filter Compiler
From the template defined at the beginning up to the complete layout, the software automatically handles the filter synthesis and the layout compilation:

- evaluation/mathematical analysis
- switched capacitor synthesis
- simulation
- Monte-Carlo analysis
- layout generation

Any kind of filters is available from 2nd up to 12th order.

Digital Cell Generator
For a set of basic digital cells, the user has access to generators which handle the netlists and interface with the layout tools.

The schematic capture uses a block which is programmable according to the required complexity.

The generator creates a " so-called" soft macrocell taking into account the complete netlist:

- counters
- shift registers
- magnitude comparators, ...

Apart from the software automation, the A.D.S. CAD tool works around standard software.

The reference CAD approach is based on industry-standard software.

Figure 4: CAD Support Availability

	Sun	Mentor HP / Apollo	Viewlogic Sun/Vaxstation
Schematic capture	EDGE	NETED	VIEWDRAW
Library compiler & design manager	CORAIL	CORAIL	CORAIL
Digital simulation	MOZART	QUICKSIM	VIEWSIM
Analog simulation	ST-SPICE	ST-SPICE	PSPICE
Mixed mode simulation	MOZART/ELDO SABER	–	VIEWSIM-AD
Place & Route	TANCELL	–	–
DRC - LVS	EDGE	–	–

Note: Please contact your local SGS-THOMSON sales representative for latest software / hardware availability.

Trademarks
EDGE & TANCELL are trademarks of Cadence Design Systems Inc.
SABER is a trademark of Analogy.
PSPICE is a trademark of Microsim
VIEWDRAW, VIEWSIM & VIEWSIM-AD are trademarks of Viewlogic Systems Inc.
NETED & QUICKSIM are trademarks of Mentor Graphics Corp.
ELDO is a trademark of ANACAD Computer Systems.

Customer Design Interface

SGS-THOMSON Micorelectronics has developed several interfaces for customers giving them easy and flexible design approaches for STKM2000.

Users can access the Analog Design System (A.D.S.):

- via SGS-THOMSON design centers
- via SGS-THOMSON associated design centers
- via CAE workstations

CAE workstation currently supported are Viewlogic and Mentor Graphics. Others will be added to meet market demands.

Contact your local representative on a regular basis to keep updated on SGS-THOMSON CAE support

In each case,direct interfaces will be offered in order to make design implementation with A.D.S. (layout and test generations).

According to these design possibilities, SGS-THOMSON defines 3 main interfaces.

Figure 5 outlines these interfaces. Each interface details the responsibilities of customer and SGS-THOMSON during circuit development flow.

Figure 5: SGS-THOMSON - CUSTOMER Interfaces

<table>
<tr><th></th><th>Interface 2</th><th>Interface 3</th><th>Interface 4</th></tr>
<tr><td>Responsibility level</td><td>Breadboard schematics</td><td>Simulated schematics</td><td>Layout tape</td></tr>
<tr><td>Circuit definition</td><td>Customer</td><td rowspan="2">Customer</td><td rowspan="3">Customer</td></tr>
<tr><td>Schematics</td><td rowspan="3">SGS-THOMSON</td></tr>
<tr><td>Simulations</td><td rowspan="2">SGS-THOMSON</td></tr>
<tr><td>Layout</td></tr>
<tr><td>Final control</td><td colspan="3">SGS-THOMSON + CUSTOMER</td></tr>
<tr><td>Prototyping phase</td><td colspan="3">SGS-THOMSON</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	− 0.5	12.0	V
V_I, V_O	I/O voltage	− 0.5	V_{DD} + 0.5	V
I_I, I_O	I/O current	− 40	+ 40	nA

Stresses above those under "maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation for the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage referred to V_{SS}

Symbol	Parameter	Min	Max	Unit
V_{DD}	Operating supply voltage	2.7	11	V
T_A	Operating ambient temperature: Military Industrial Commercial	 − 55 − 40 0	 + 125 + 85 + 70	 °C °C °C

DIGITAL LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT

Standard condition = 2 loads + 1 mm of metal interconnect

Cell Code	Description	V_{DD} = 10V ± 10%, T_A = 25°C			Unit
		T_{PHL}	T_{PLH}	Other	
IV1	Standard inverter	2.26	2.01		ns
ND2	2 - input NAND	1.74	2.44		ns
NR2	2 - input NOR	2.55	2.02		ns
FD1	D Flip - Flop				
	From C to QN	6.44	8.26		
	T_{SU}			5.00	
	T_{HL}			1.75	ns
	T_{WH}			8.25	
	T_{WL}			5.00	
OB11	CMOS inverting output buffer capacitance load = 100 pF	12.4	12.3		ns

DC GENERAL ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 10% or V_{DD} = 10V ± 10% (unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
TTL INTERFACE							
V_{IL}	Low Level Input Voltage				0.8	V	1, 2, 3, 4
V_{IH}	High Level Input Voltage		2.0			V	1, 4
			2.25			V	2, 4
			2.25			V	3, 4
V_{OL}	Low Level Output Voltage	I_{OL}= Rated buffer current			0.4	V	1, 2, 3, 4, 5
V_{OH}	High Level Output Voltage	I_{OH}= Rated buffer current	2.4			V	1, 2, 3, 4, 5
CMOS INTERFACE							
V_{IL}	Low Level Input Voltage				30% V_{DD}	V	1, 2, 3
V_{IH}	High Level Input Voltage		70% V_{DD}			V	1, 2, 3
V_{OL}	Low Level Output Voltage	I_O= ≤ ±1 µA			0.05	V	1, 2, 3
V_{OH}	High level output voltage	I_O= ≤ ±1 µA	V_{DD} –0.05			V	1, 2, 3
GENERAL							
I_{IL}	Low Level Input Current	V_I= V_{SS}	–1 –3 –5		1 3 5	µA µA µ	1 2 3
I_{IH}	High Level Input Current	V_I= V_{DD}	–1 –3 –5		1 3 5	µA µA µ	1 2 3
I_{OZ}	Tri-state Output Leakage	V_O= 0 V or V_{DD}	–2.5 –5 –10	< 1	2.5 +5 +10	µA µA µ	1 2 3
C_{IN}	Input Capacitance	Freq = 1 MHz @ 0 V		3		pF	6
C_O	Output Capacitance	Freq = 1 MHz @ 0 V		4		pF	5, 6
$C_{I/O}$	Bidi. I/O Capacitance	Freq = 1 MHz @ 0 V		5		pF	5, 6
I_{KLU}	I/O Latch-up Current	V < V_{SS}, V > V_{DD}		200		mA	
V_{ESD}	Electrostatic Protection	C = 100 pF, R = 1.5K		2000		V	
PD_G	Power Dissipation per Gate			17.5		µW/Gate/MHz	
PD_O	Power Dissipation per Output	C = 50 pF		1.5		mW/Output/MHz	

Notes: 1. Commercial 0 to 70°C
2. Industrial –40 to 85°C
3. Military –55 to 125°C
4. V_{DD} = 5 V ±/10%
5. Buffers with default programmation attribute
6. Excluding package

ANALOG LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT

Cell Code	Description	Parameters Test Conditions	Min	Typ	Max	Unit
CMP11	Static CMOS comparator	Propagation delay (overdrive = 5 mV) Offset		1 ± 3	1.4 ± 10	ms mV
CMP31	Static BICMOS comparator	Propagation delay (overdrive = 5 mV) Offset		90 ± 2	110 ± 7	ns mV
CPX11	Capacitor fields	Unit capacitance Capacitor value range Absolute accuracy Matching (capacitor ratio)	 0.1 	0.1 0.5	 50 ± 15 1.0	pF pF % %
CPP11	Monolithic Capacitor	Capacitor range Absolute accuracy	1 	 	100 ± 15	pF %
RPM/PPM	Resistor/Potentiometer P-Base	Resistor value range Absolute accuracy Matching Temperature coefficient Voltage coefficient	5.6 	 	3000 ± 20 ± 3 0.2 0.25	KΩ % % %/°C %/V
SWI1	Analog switch	Elementary switch RON value Number of switches in parallel	 1	5 	25 3	KΩ
MN11	Telescopic NMOS transistor	RON value		100		Ω
OPA31	General purpose MOS Operational amplifier	Unity gain bandwidth Current consumption Phase margin (C1 = 100 pF, R2 = 10 kΩ) Offset		3.3 700 60 ± 3	4.6 ± 10	MHz µA Degrees mV
OPA41	Internal bipolar Operational Amplifier	Unity gain-bandwidth current consumption Phase margin (CL = 15 pF, RL = 100kΩ) Offset		9 240 62 ± 1	30 ± 5	MHz µA Degrees mV
OPA71	Rail to rail external MOS operational Amplifier	Unity gain bandwidth current consumption Phase margin (CL = 100 pF, RL = 100KΩ) Offset		2.3 360 80 ± 3	 ± 10	MHz uA Degrees mV
OTA11	MOS transconductance amplifier	Unity gain - bandwidth (CL = 2 pF)		24		MHz
POR11	Programmable Power on Reset	Active Level Accuracy Hysteresis Accuracy			± 5 ± 5	% %
VRF11	Voltage bandgap reference	Output voltage accuracy Temperature coefficient Current consumption		 15	± 2 100 	% ppm µA

ANALOG LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT

Cell Code	Description	Parameters Test Conditions	Min	Typ	Max	Unit
OSC11	Programmable crystal oscillator	Frequency	0.1		20	MHz
OSC41P	RC oscillator	Frequency Stability versus temperature Stability versus voltage	1	100 0.01 0.5	800	KHz % / °C % / V
OSC31P	One pad I.C oscillator	Frequency Stability versus temperature Stability versus voltage	2	 0.01 0.5	200	KHz % / °C % / V
	Filters	Order Center frequency	2		12 100	 KHz
AD8A	8 bit analog to digital converter	Conversion time Integral non linearity Differential non linearity			10 ± 0.5 ± 0.5	µs LSB LSB
DA8A	8 bit analog to digital converter	Conversion time (C_L = 2 pF) Integral non linearity			1 ± 0.5	µs LSB

SGS-THOMSON MICROELECTRONICS

TSGSM SERIES

3.5µ/2 POLY / 1 METAL HCMOS MIXED ANALOG-DIGITAL STANDARD CELLS

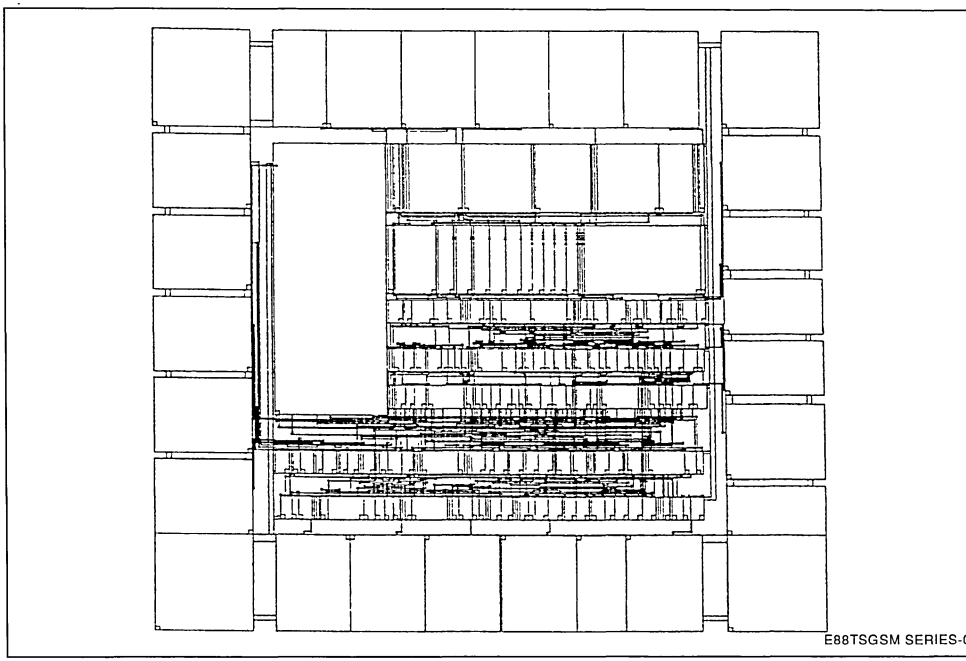
FEATURES

- ADVANCED HCMOS TECHNOLOGY :
  - 3.5µ Drawn Channel Length
  - 2 Polysilicon Layers
  - 1 Metal Layer
  - P Well Silicon Gate CMOS Process
- HIGH LATCH-UP IMMUNITY
- FULL ESD PROTECTION
- POWER SUPPLY
  Maximum Ratings : - 0.5V to + 12V
  Operating Conditions : 3 to 10V
- EXTENSIVE MACROCELL LIBRARY
  - 119 Logic Cells
  - 117 Analog Cells
    with programmable cells : soft macro cells, abuttable cells
- INPUT/OUTPUT CELLS
  Compatibility : TTL or CMOS Levels
  Configurability : Input/Output/Bidirectional I/O/Analog I/O ...
- CAD SOFTWARE SUPPORT
  - ADS (Analog Design System)
  - Fully Integrated (+ FILCAD™ for filter design)
  - Flexible Design Interfaces
- OPERATING TEMPERATURE RANGE
  - Commercial : 0 to + 70°C
  - Industrial : – 40 to + 85°C
  - Military : – 55 to + 125°C
- PACKAGE OPTIONS
  - DIL : Plastic or Ceramic
  - SMD : SO, PLCC, LCCC, QFP

DESCRIPTION

The TSGSM Series, mixed analog-digital Standard Cell products from SGS-THOMSON Microelectronics, represents a major step allowing the system designer dealing with both digital and high level analog functions to benefit of the state of the art semi-custom circuit integration capabilities.

Figure 1 : Example of TSGSM Chip Layout.



E88TSGSM SERIES-01

The large variety of predefined and precharacterized functions ranging :

- in digital from simple gates to counters, registers...
- in analog from single operational amplifier to A/D or D/A converters, switched capacitors filters ...

has been proven extremely efficient in the design of many mixed HCMOS Analog-Digital ASIC's circuits in such various applications as consumer, computer, industrial, military, telecommunications and automotive fields.

TSGSM ARCHITECTURE

TECHNOLOGY

TSGSM Series developed by SGS-THOMSON is using an advanced silicon gate P well, dual poly-silicon layer, single metal layer HCMOS technology.

The process is very well suited for the design and integration of high performance analog functions combined with digital. It achieves operating speeds up to 15MHz for the digital part of the TSGSM circuit.

Thanks to the 2 polysilicon layers, TSGSM Series can integrate high accuracy switched capacitors filters based on the same concept of TSGF Series, switched capacitor Filter Arrays (Refer to TSGF04/08/12 Data Sheet). True capacitors are realized with Poly 1 and Poly 2 layers.

CELLS

Predesigned and precharacterized Macrocells are selected, placed and interconnected on the chip to implement the mixed analog-digital function.

Digital and Analog Macrocells have different height, as shown on the chip layout of fig. 1. In addition some cells like A/D or D/A converters are designed as fixed blocks.

CHIP TOPOLOGY

The inputs and outputs of cells are interconnected by using 2 conductive layers : polysilicon and metal.

The chip layout is composed of cell rows, whose number is determined to optimize the die size, and of horizontal routing channels.

Peripheral cells surround the internal active chip area in order to interface it with its external environment.

Despite the row base architecture complex block functions can be placed and routed on the chip.

Generally for design optimization purpose, power busses of the analog and the digital parts of the chip are routed separately.

CELL LIBRARY

The TSGSM Macrocell library features around 160 different macros :

- 119 digital cells.
- 117 analog cells.

The main characteristics of TSGSM library is to offer users a high flexibility for cell definition and generation :

- The **DIGITAL LIBRARY** provides in addition of existing hard macros the capability to generate soft macros like counters, shift registers, dividers...
  These modulo N parameterized cells are generated at the layout level by lateral abutment of hard macros.
- The **ANALOG LIBRARY** presents particular features such as :
  - Biasing strategy with a current bias generator, programmable current mirrors, and current biased cells and voltage biased cells.
  - Use of programmable cells for capacitor fields (0.1 to 30pF typically), resistor fields (150 to 1.8MΩ), bipolar transistors, MOS transistors, current mirrors.
  - Grounded shield for power supply rejection improvement.

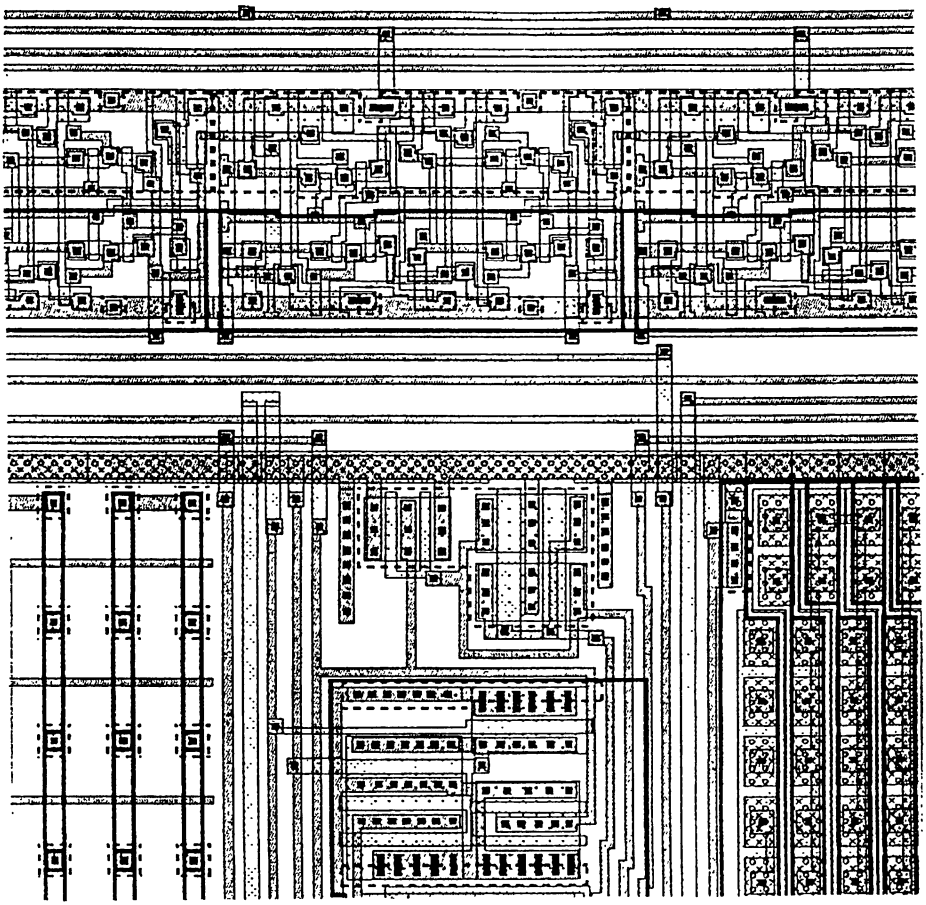
The complete TSGSM library is fully described within the TSGSM User's Manual of the SGS-THOMSON library.

Fig. 4 and Fig. 5 give an abstract of all available digital and analog cells within TSGSM' library.

For more details, users have to refer to the TSGSM User's Manual they can require to their nearest SGS-THOMSON sales office or representative.

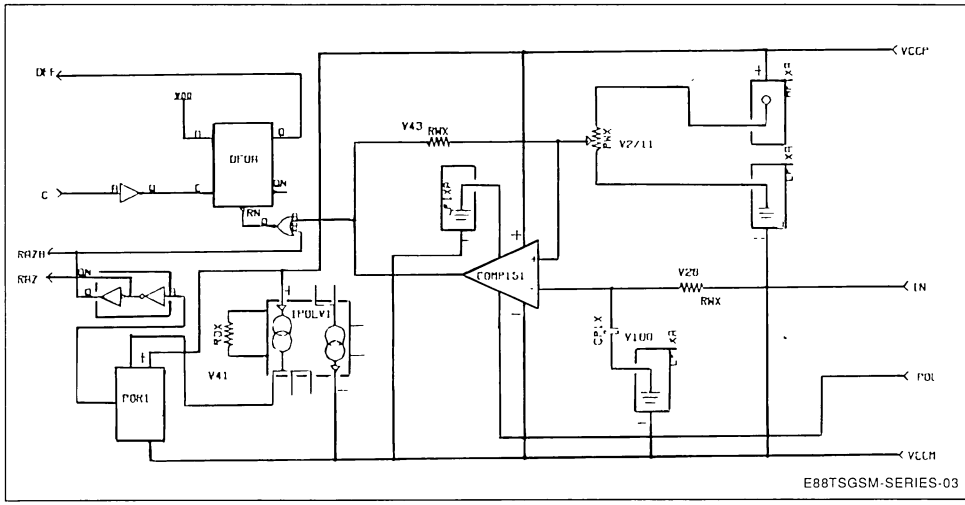
Note : SGS-THOMSON can develop on request a special cell for a specific customer circuit : new cell or existing cell with different electrical characteristics.

Figure 2 : Example of Interconnection between Analog and Digital Cells.



E88TSGSM-SERIES-02

Figure 3 : Example of a Mixed Analog-Digital Function.



CORE CELLS

Figure 4: TSGSM Series Digital Library Abstract.

Cell Type	Description	Number of Different Options (1)
AA	AND Gates	3
AN.	AND into NOR Gates	4
DF	D Flip-flops	4
DL	D Latches	5
EN	Exclusive NOR	1
EO	Exclusive OR	2
FF.	D Flip-flops (2 clocks)	4
II	Dual Buffers	2
IN	Inverters	5
IT	Tri-state Internal Buffers	3
MU	Multiplexers	3
NA	NAND Gates	4
NO.	NOR Gates	4
ON	OR into NAND Gates	2
OR	OR Gates	3
TF	Toggle Flip-flops	3
TG	Schmitt Triggers	3
TT .	Level Shifters	3
ZZ..	Supply Cells	2
CCG	Clock Generators	3
FPCG	Non-overlapping 4-phase Clock Generator	1
TPCG	Non-overlapping 2-phase Clock Generator	1
INVL	Delay Inverter	1

(1) For each type of cell, the TSGSM library provides extensive number of options as for example
- NAND type cells 2, 3, 4 or 6 input NAND's
- D flip-flop cells with low set, with low reset
- input buffers TTL, CMOS, with pull-up

Figure 4 (continued).

I/O CELLS

Cell Type	Description	Number of Different Options (1)
OB..	Output Buffers	4
PP..	Power Pads	3
OB..	Tri-state Output Buffers	4
IB..	Input Buffers	8
IO..	Bidirectional Buffers	5
OB..	Open-drain Output Buffers	4

(1) For each type of cell, the TSGSM library provides extensive number of options as for example :
- NAND type cells : 2, 3, 4 or 6 input NAND's
- D flip-flop cells : with low set, with low reset...
- input buffers : TTL, CMOS, with pull-up...

CORE CELLS

Figure 5: TSGSM Series Analog Library Abstract.

Cell Type	Description	Number of Different Options	Metal Mask Programmable
COMP...	Comparators	6	
MN...	N MOS Transistors	4	x
MP...	P MOS Transistors	4	x
OSC..	Oscillators (crystal RC)	4	
POR.	Power on Reset	2	
SW..	Switches	3	
TRIG	Schmitt Trigger	1	
CP..	Capacitor Fields	1	x
BOPA/BOTA	Bias for Op amps and Transconductance Amplifiers	3	
BIP	Bipolar Transistors	1	x
OP	Operational Amplifiers	5	
OO	Output Stage for Op Amp	1	
OT	Transconductance Amplifiers	2	
R..	Resistance Fields	3	x
P..	Potentiometer Fields	3	x
VREF	Voltage Reference Bandgap	1	
ZEN..	Zener Diodes	3	
IPNV	Current Mirror Source-sink	1	x
IPOL..	Bias Current Generator	2	x
ISN/ISP	Current Mirror Source/sink	4	x
HF/LF	Internal V^+/V^- Analog Cell	2	

BLOCKS AND SOFT MACROS

Cell Type	Description	Number of Different Options	Metal Mask Programmable
ADC8	8 Bit Analog to Digital Converters	2	
DAC8	8 Bit Digital to Analog Converter	1	
DBP/DS1	LCD Drivers	3	
SCF	Biquadratic 2nd Order Filter	1	x
VRLCD	LCD Voltage Reference	1	

ADS ANALOG DESIGN SYSTEM

The SGS-THOMSON TSGSM Series is fully supported by a complete Computer Aided Design (CAD) system. The SGS-THOMSON CAD system, ADS, is complete in that once a design is entered all the tools necessary to complete that design are available to the user in this one system.

These tools include schematic capture, logic and analog simulations, fault simulation, automatic place and route, parasitic delay extraction and test pattern generation.

ADS ANALOG DESIGN SYSTEM is available on SUN™ computer systems.

In addition, the TSGSM library is implemented on CAE workstations :
- Mentor™.

SGS-THOMSON developed direct interfaces between these CAE workstations and its ADS system.

The ADS package allows the development of analog and digital standard cell circuits so easily that each system designer can handle it.

The development of mixed analog and digital circuit is done with advanced concepts such as :
- parameterized cells (resistors, capacitors, current generators ...)
- metal mask programmable cells (switched capacitor filters ...)
- compiled cells (bit slice concept for digital functions like counters, dividers ...).

The main CAD tools available within ADS are :

■ SCHEMATIC GRAPHIC CAPTURE

EDGE/CADENCE™ provides graphic capture of schematic circuit diagram. Designer can create blocks by using the 100% hierarchy of EDGE/CADENCE™ and also can specify values of parameterized cells.

After the net list generation, the modules generated under EDGE™ are oriented automatically thru logic or analog simulation.

■ LOGIC SIMULATION

MOZART™, SGS-THOMSON's, hierarchical logic simulator, allows design verification and timing analysis of the circuit. A pre-layout timing analysis is run with calculated delays based on fanout, VDD, temperature and best, typical or worst case process conditions.

The 2 input files to MOZART™ are the net list generated from graphic capture and the input test pattern description.

MOZART™ simulator allows mixed analog and digital simulation for analog cells having an equivalent model described under MOZART™.

■ ANALOG SIMULATION

STSPICE electrical simulator allows pre-layout or post-layout timing analysis of the analog blocks of the circuit.

STSPICE input files are the net list and the input test pattern descriptions.

With the improvements brought by SGS-THOMSON to STSPICE, the analog simulator becomes a powerful CAD tool :
- special level modelling for speed improvement on digital sub-circuits,
- fast execution on full analog part of TSGSM circuit, thanks to macro modelling, allows simulation of large analog blocks.
- ELDO™ simulator can be used for large analog simulations

■ PLACEMENT AND ROUTING

TANCELL™ software is an efficient standard cell automatic place and route whose main features are
- use of different heights of cells on the chip
- interactive pre-placement of blocks, cells and I/O's for die size optimization
- capability to force priorities on nets for critical path routing
- capability to generate soft macros, blocks by cell abutment.
- multi supply routing
- routing with compaction

A check program performs at the end of the layout, design rule checking and verifies conformity of the graphic data base versus the schematics data base.

■ PARASITIC DELAY EXTRACTION

ADS is computing the exact parasitic delays brought by the placement and routing. Delays are based both on resistance and capacitance of each interconnect.

As soon as the parasitic RC delays are extracted, user can run a post layout simulation for accurate timing new analysis.

ADS software converts automatically the post layout simulation (with parasitic delays) file into test patterns directly compatible with SGS-THOMSON test equipments.

At same time static and dynamic parameters are added to the functional test pattern file : all input/output levels are tested during the functional test sequence.

Fig. 6 outlines the SGS-THOMSON approach for the design of analog or mixed analog/digital circuits.

One of the particularities of TSGSM series is to provide switched capacitor filter integration capabilities. The filter cells available within TSGSM library are identical to those used on the SGS-THOMSON Analog Filter Arrays, TSGF Series, which are mask programmable switched capacitor filters.

For filter synthesis, simulation and layout, designers are given an efficient Filter CAD design tool : FILCAD™.

For more informations about SGS-THOMSON switched capacitor filter design solutions and CAD tools, please refer to TSGF04/08/12, 4th to 12th order switched capacitor filter arrays data sheet.

Fig. 7 shows the development phases of a TSGSM Series standard cell. The design translation phase up to the prelayout simulation can be done on CAE workstations like Mentor Graphics™, with ADS Analog Design System.

Figure 6 : SGS-THOMSON CAD Tools and Product for Analog and Mixed Analog-Digital Circuits.

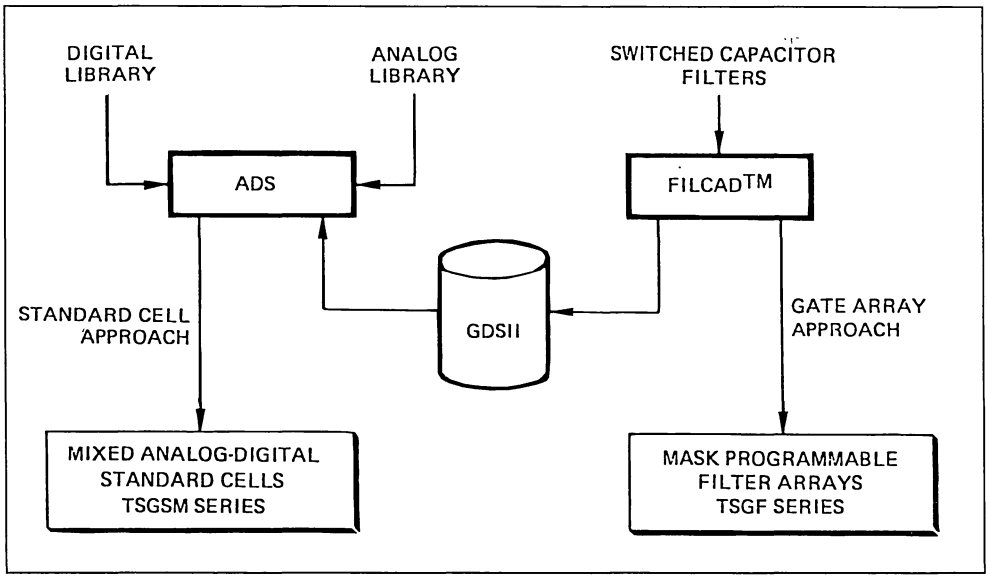
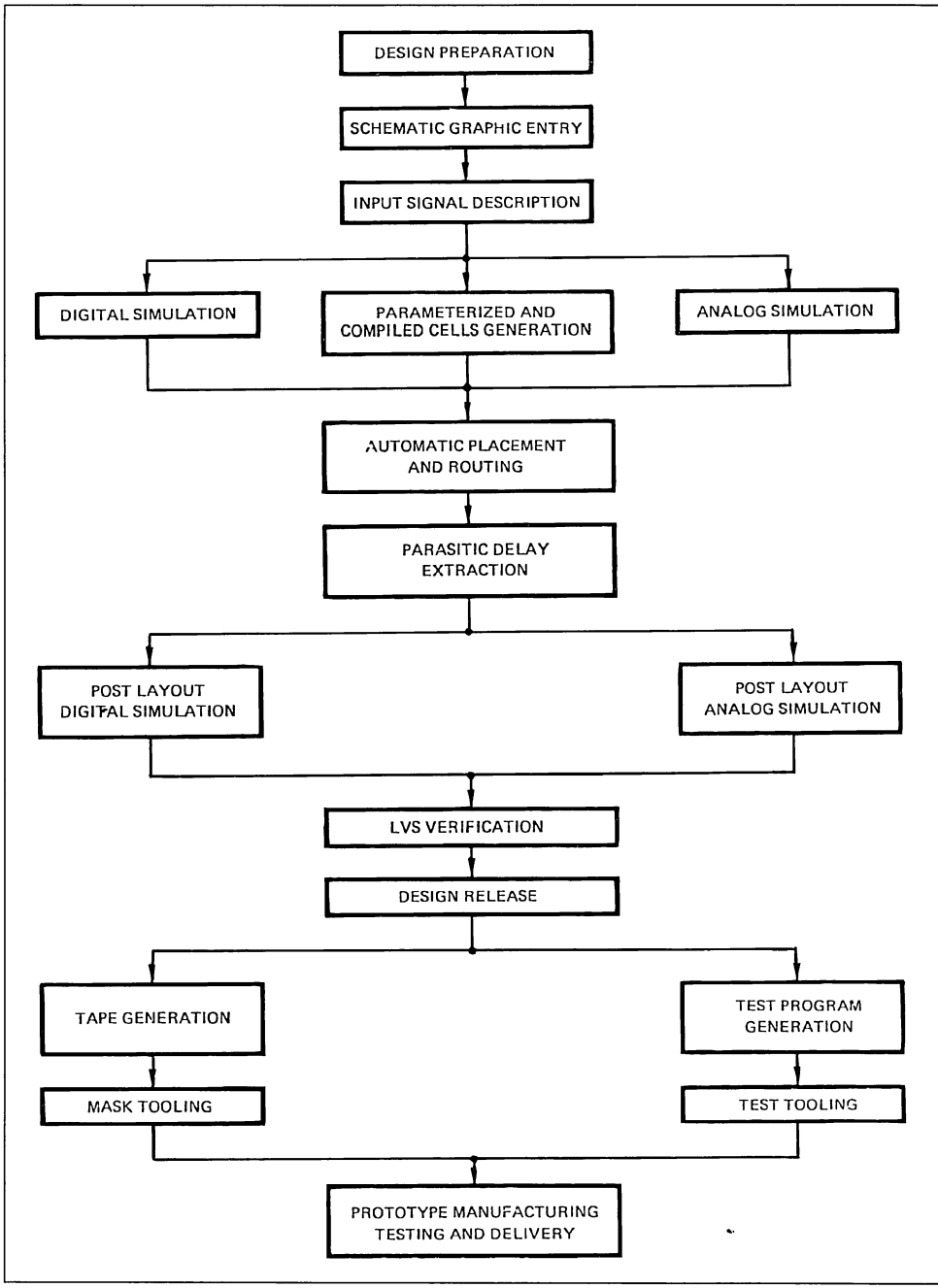


Figure 7 : TSGSM Series Development Flow.



CUSTOMER DESIGN INTERFACE

SGS-THOMSON has developed several interfaces for customers giving them easy and flexible design approaches for TSGSM 3.5µ/2 poly/1 metal HCMOS mixed Analog Digital Standard Cells series.

User can access ADS Analog Design System.
- via the SGS-THOMSON Design Centers,
- via connection to SGS-THOMSON CAD Center,
- via the SGS-THOMSON associated Design Centers.

CAE workstations capabilities are :
- CADENCE™,
- Mentor Graphics™.

In that case direct interfaces will be offered to user in order to make design implementation and test generation with ADS.

According to all of these design possibilities, SGS-THOMSON defined 3 main customer design interfaces.

Figure 8 outlines these interfaces. Each interface delineates the responsibilities of customer and SGS-THOMSON during circuit development flow shown in fig. 7.

Figure 8: Design Interface.

	Interface 2	Interface 3	Interface 4
Definition of Circuit Specification	Customer	Customer	Customer
Logic and Electrical Description	Customer	Customer	Customer
Test Pattern Definition	Customer	Customer	Customer
Graphic Capture + Input Signal Entry	SGS-THOMSON	Customer	Customer
Design Verification	SGS-THOMSON	Customer	Customer
Pre-layout Simulation	SGS-THOMSON	Customer	Customer
Approval	Customer	Customer/SGS-THOMSON	
Auto Place and Route	SGS-THOMSON	SGS-THOMSON	Customer
Post-layout Simulation	SGS-THOMSON	SGS-THOMSON	Customer
Design Release	Customer	Customer/SGS-THOMSON	Customer/SGS-THOMSON
Test Program Generation - Test Tooling	SGS-THOMSON	SGS-THOMSON	SGS-THOMSON
Mask Tooling	SGS-THOMSON	SGS-THOMSON	SGS-THOMSON
Prototype Manufacturing and Testing	SGS-THOMSON	SGS-THOMSON	SGS-THOMSON
Prototype Delivery	SGS-THOMSON	SGS-THOMSON	SGS-THOMSON

With interface 3, design can be done either at SGS-THOMSON Microelectronics Design Center facilities or at customer location.

ABSOLUTE MAXIMUM RATINGS ($T_{amb.}$ = 25°C, Voltage referenced to V_{SS}.)

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	− 0.5	12.0	V
V_I, V_O	I/O Voltage	− 0.5	V_{DD} + 0.5	V
I_I, I_O	I/O Current	− 40	+ 40	mA
T_{stg}	Storage Temperature (ceramic)	− 65	+ 150	°C
	Storage Temperature (plastic)	− 40	+ 125	°C

Stresses above those listed order "maximum rating" may cause permanent damage to the device. This is a stress rating only and functional operation to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (Voltage referred to V_{SS})

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Operating Supply Voltage	4.5 9.0	5.0 10.0	5.5 11.0	V V
V_{DD}	Extended Supply Voltage	3		12.0	V
T_{amb}	Operating Ambient Temperature Military Industrial Commercial	 −55 −40 0		 +125 +85 +70	 °C °C °C

Note : 2. For extended supply voltage please consult SGS-THOMSON Microelectronics.

DC GENERAL ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10% or V_{DD} = 10V ± 10% unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High Level TTL Input Voltage	**V_{DD} = 5V ± 10%** T° = 0°C/=70°C T° = −40°C/+85°C T° = −55°C/+125°C	 2.0 2.25 2.25			 V V V
V_{IL}	Low Level TTL Input Voltage	**V_{DD} = 5V ± 10%** All Temp. Ranges			0.8	V
V_{IH} V_{IL}	High Level CMOS Input Voltage Low Level CMOS Input Voltage		70% V_{DD}		 30% V_{DD}	V V
I_{OZH}	Tristate Output Leakage Current	**V_O = V_{DD}** T° = 0°C/+ 70°C T° = −40°C/+ 85°C T° = −55°C/+ 125°C			 2.5 5 10	 µA µA µA
I_{OZL}		**V_O = V_{SS}** T° = 0°C/+ 70° T° = −40°C/+ 85°C T° = −55°C/+ 125°C	 − 2.5 − 5.0 − 10.0			 µA µA µA
I_{IH}	High Level Input Leakage Current	**V_I = V_{DD}** T° = 0°C/+ 70° T° = −40°C/+ 85°C T° = −55°C/+ 125°C			 1.0 3.0 5.0	 µA µA µA
I_{IL}	Low Level Input Leakage Current	**V_I = V_{SS}** T° = 0°C/+ 70° T° = −40°C/+ 85°C T° = −55°C/+ 125°C	 − 1.0 − 3.0 − 5.0			 µA µA µA
I_{CC}	Max Admissable Current per Pin: Analog Digital				 ± 20 ± 40	 mA mA

DIGITAL LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT (V_{DD} = 10V ± 10%, $T_{amb.}$ = 25°C, Typical Process Standard Condition = 2 Loads + 1 mm of Metal Interconnect)

Cell Code	Description	V_{DD} = 10V ± 10%			Unit
		T_{PHL}	T_{PLH}	Other	
IN01	Standard Inverter	5.7	4.7		ns
NA02	2-input NAND	6.2	5.8		ns
NO02	2-input NOR	6.4	5.1		ns
DF08	Positive Edge D Flip-Flop from CKL to Q: T_{SH} T_H T_{WH} T_{WL}	10.6	6.1	 14.0 5.0 20.0 16.0	ns ns ns ns ns
OB2	TTL Inverting Output Buffer Capacitance Load = 50pF = 25pF = 15pF	 4.1 3.6 3.4	 5.0 4.3 4.0		 ns ns ns
T02	Tri-state TTL Output Buffer Capacitance Load = 50pF = 25pF = 15pF	 4.1 3.6 3.4	 5.0 4.3 4.0		 ns ns ns
IB021	CMOS Inverting Input Buffer	7.4	8.7		ns

Note : Refer to TSGSM User's Manual for more detailed informations.

ANALOG LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT (V_{DD} = 10V ± 10%, unless otherwise specified $T_{amb.}$ = 25°C, typical process.)

Cell Code	Description	Parameter/Conditions	Min.	Typ.	Max.	Unit
COMP	Static Comparator	Propagation Delay (overdrive = 10mV) Offset		1 ± 5	2 ± 15	µs mV
CP1X	Capacitor Fields	Unit Capacitance Capacitor Value Range Absolute Accuracy Matching (capacitor ratio)	0.08 0.1	0.1 0.5	0.12 50 ± 15 1.0	pF pF % %
RPX/PPX	Resistors . Polysilicon	Resistor Value Range Absolute Accuracy Matching Temeperature Coefficient	0.15		20 ± 20 ± 1 0.15	kΩ % % %/°C
RDX/PDX	. P^+ Diffusion	Resistor Value Range Absolute Accuracy Matching Temperature Coefficinet	0.75		100 ± 20 ± 1 0.15	kΩ % % %/°C
RWX/PWX	. P^- Well	Resistor Value Range Absolute Accurace Matching Temperature Coefficient Voltage Coefficient	5		2000 ± 20 ± 2 ± 1 5	kΩ % % %/°C %/V
SWIX MN1X/ MP1X	Switches . Analog Switch . MOS Switch	 R_{ON} Value Range R_{ON} Value Range	 50	 10 	 30 500	 kΩ Ω
IPOLXX + ISyy	Programmable Reference Current Generator	Current Current Step Supply Voltage Rejection (4V< V_{DD} < 10V)	1	 1 + 2	250	µA µA %/V
OPA2	General Purpose Operational Amplifier	Phase Margin Unit Gain Bandwidth (C_L = 100pF, R_L = 10kΩ) Offset		80 3.3 ± 5	 ± 10	Degrees MHz mV
OTA1	Transconductance Amplifier	Unit Gain Bandwidth (C_L = 3.5pF)	7	10.5		MHz
POR1	Static Power on Reset	Active Voltage (V_{DD} = 10V) (V_{DD} = 5V)		4.5 3.5		V V
VREF	Voltage Bandgap Reference	Output Voltage	1.15	1.18	1.20	V
ZENx	Zener Diode	Zener Voltage (bias current = 50µA)	5.3	5.6	5.9	V
OSC11	Crystal Oscillator	Frequency	0.1		12	MHz
OSC31	RC Timer	Frequency Stability Versus Temperature Stability Versus Supply Voltage		100 0.02 0.5	500	kHz %/°C %/V
ADC8Bx	8 Bits Analog to Digital Converter	Conversion Time Integral non Linearity			25 ± 0.5	µs LSB
SCFx	Biquadratic Filter Cell	Signal Frequency Order	 2		30 12	kHz

Note : Refer to TSGSM User's Manual for more detailed informations.

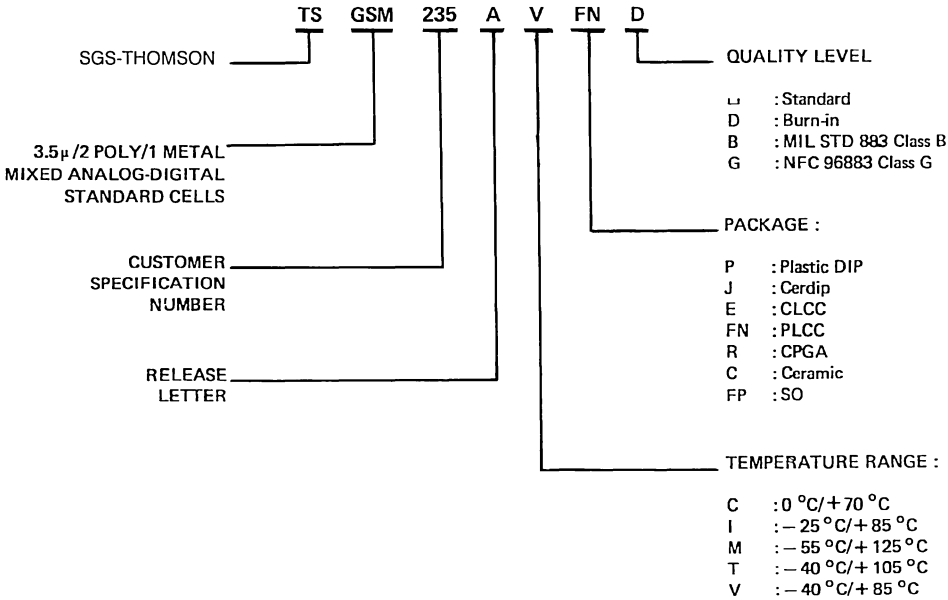
PACKAGING

SGS-THOMSON has a wide variety of package options available to the user :

- Dual in line packages (DIP)
  - Plastic
  - Cerdip
  - Side Braze
- Chip carriers
  - Plastic Leaded Chip Carriers (PLCC)
  - Ceramic Leadless Chip Carriers (CLCC)
  - Ceramic Leaded Chip Carriers (LDCC)
- Small outlines (SO)

Where different packaging requirements are needed, contact SGS-THOMSON Marketing. Standard cells products in dice form (chip tray or wafer form)can also be supplied.

ORDER INFORMATION



MIXED ANALOG-DIGITAL BIPOLAR ARRAY

MIXED ANALOG - DIGITAL BIPOLAR ARRAYS

FEATURES

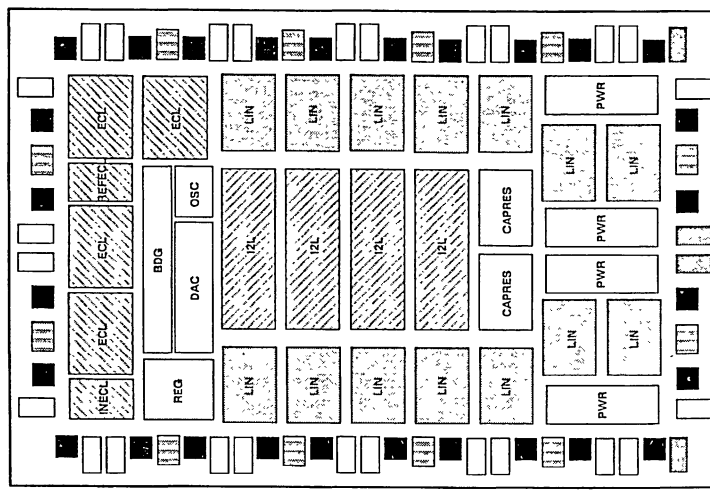
- ADVANCED BIPOLAR TECHNOLOGY :
  - NPN, F_T = 3GHz
  - 2 Metal Layers
  - 100MHz ECL Flip-Flop
- FULL ESD PROTECTION
- POWER SUPPLY :
  - Maximum Ratings = UP to 15V
  - Operating Conditions = 3 to 12V
- ANALOG - DIGITAL ARRAYS :
  - Analog Tiles
  - ECL Tile For High Speed Logic
  - I^2L Core For Low Frequency Random Logic
  - Power Tile With 200mA Capability
- 5 ARRAYS AVAILABLE :
  J4, J6, J9, J13, J23 from 600 to 3000 Components
- CAD SOFTWARE SUPPORT :
  - ADS-PC (Analog Design System - PC)
  - Fully Integrated in PC Environment
  - P-CAD* Software, for Schematic Capture, Simulation, and Layout
- OPERATING TEMPERATURE RANGE :
  Commercial : 0 to 70°C
  Industrial : - 40 to + 85°C
  Military : - 55 to + 125°C
- PACKAGE OPTIONS
  - DIL : Plastic or Ceramic
  - SMD : SO, PLCC, LCCC, QFP

USIC PRODUCTS DESCRIPTION

SGS-THOMSON Microelectronics introduce the mixed analog-digital arrays developped on a 3GHz process. Using its expertise in bipolar arrays, SGS-THOMSON has developed this new series to offer a product on leading edge of advan ced technology :

- High speed process (NPN, F_T = 3GHz)
- Architecture with tile concept to improve the efficiency of the placement and routing
- 2 customized metal layers with 4 masks to personalize (contact, M1, via, M2)
- Complete CAD system on a PC from schematic capture up to the layout.

Figure 1 : Example of TSFJ13 architecture.



E89TSFJ-01

TSFJ ARCHITECTURE

TECHNOLOGY

TSFJ series developed by SGS-THOMSON is using an advanced bipolar process with high frequency performance (NPN, F_t = 3GHz). With a double metal layer the parasitic elements are minimized to improve the layout density and to increase the performances.

The process is very well suited for accurate analog bipolar design. The other key feature is introduced with the digital capability using either ECL or I2L functions.

Thanks to protection networks on sequential input pad, the complete TSFJ series is protected against ESD parasitic effects.

TILE ARCHITECTURE

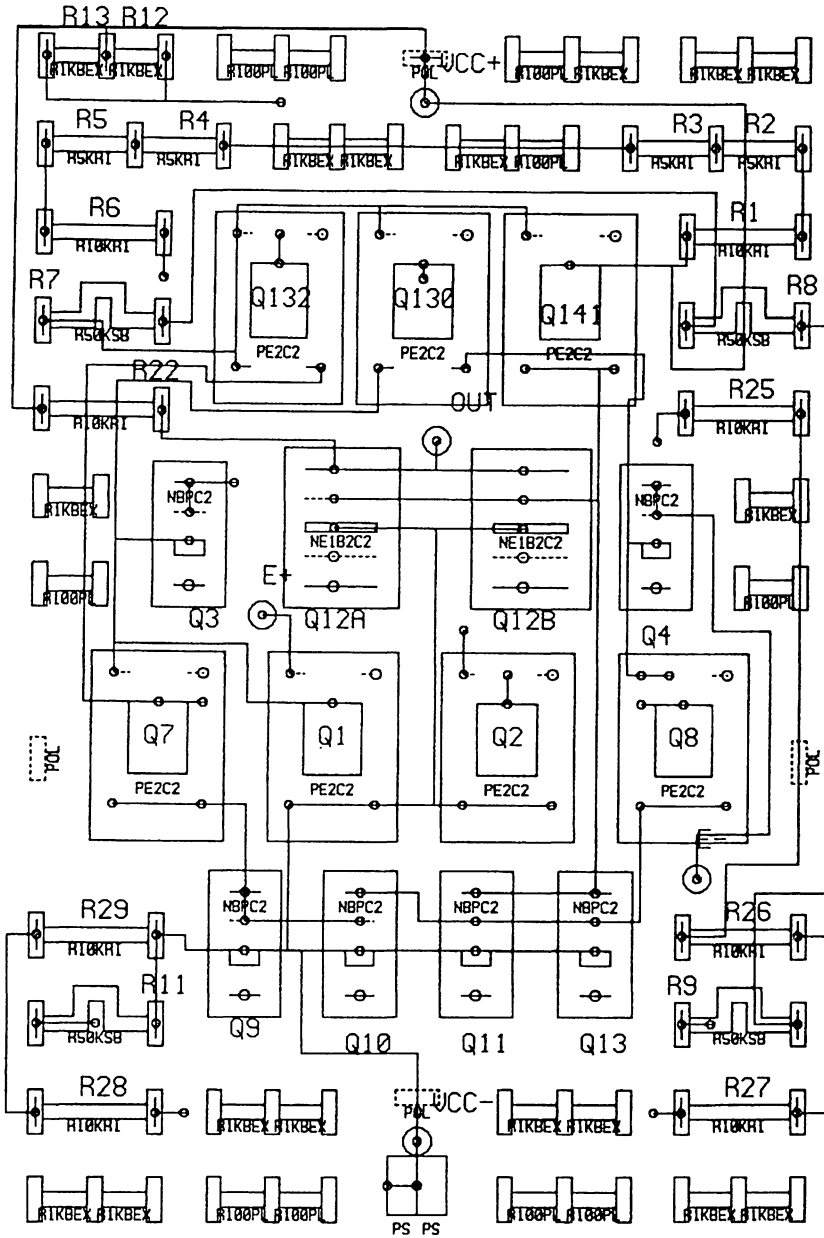
The TSFJ series has an architecture based on a tile concept in order to take advantage of efficient layout.

For SGS-THOMSON a tile is an optimized placement of basic components such as transistors, resistors, and capacitors, with no routing done in advance. When customization is prepared, the designer optimizes the routing of each tile according to needs.

6 different types of tiles have been developed :

- LINEAR TILE, optimized for analog functions (Op-amps, comparators, ...)
  - 6 standard NPN (h_{FE} = 105, and I_c = 100µA)
  - 2 low noise NPN
  - 7 lateral PNP (h_{FE} = 52, and I_c = 1µA)
  - 44 resistances from 100 Ω to 50KΩ
- POWER TILE, optimized for power interface capability ;
  - 4 standard substrate PNP
  - 1 power substrate PNP (I_{KF} = 10mA)
  - 1 power NPN (I_{KF} = 314mA)
  - 1 medium power NPN (I_{KF} = 78mA)
  - 3 standard NPN
- I^2L LOGIC TILE, optimized to implement random or logic using standard I2L functions (NAND, AND, NOR, OR, Flip-flop, ...)
  - row of I2L operators
- ECL LOGIC TILE, optimized for high speed logic up to 100MHz
  - equivalent to 1 D flip-flop
- BUILT-IN FUNCTION TILES, a certain number of predefined tile have been created to fulfill some specific analog requests such as ;
  - 1 bandgap voltage reference
  - 1 oscillator (RC or quartz)
  - 1 voltage regulator
  - 1 R-2R resistor ladder for 6 and 8 bits DAC
- RESISTOR/CAPACITOR TILE, optimized for RC network or compensation capacitor purpose
  - 2.5pF and 7pF capacitors available

Figure 2 : Example of a symbolic Linear Tile.



LINEAR TILE AFTER LAYOUT E89TSFJ-02

Figure 3 : TSFJ Series : The Available Tiles.

Tiles	Nb Components	J04	J06	J09	J13	J23
ECL	86			4	4	5
I2L	9	6	15	18	36	54
HF	46			1	1	1
CAPRES	24			2	2	
REFECL	31			1	1	1
DAC	33			1	1	
R2R	46					1
LIN	59	6	8	10	14	24
RES	21	1	1			4
PWR	34	1	2	2	2	4
PWR1	34	1	2	2	2	4
BANDGAP	37	1	1	1	1	1
OSCIL	23	1	1	1	1	1
PROTECA	2	7	8	11	13	18
PROTECB	2	7	7	11	13	18
CAP1	1	4	6	8	8	10
CAP2	2	2	4	2	4	9
CAPAS	3		1			
DIODES	2	2	4	4	4	8
PUISS	3	1				
ALIM	40		1	1	1	2
	TOTAL :	600	919	1554	1964	3067

E88TSFJ-03

Figure 4 : TSFJ Series : The Transistors.

Components	J04	J06	J09	J13	J23
NPN 5mA	54	79	201	225	331
NPN 16mA	14	18	24	32	52
NPN 50mA	2	4	4	4	8
NPN 100mA	2	2	2	2	4
NPN 200mA	2	4	4	4	8
LATERAL PNP 60µA	50	68	83	111	184
SUBSTRATE PNP	8	16	16	16	32
SUBSTRATE PNP 10mA	2	4	4	4	8

E88TSFJ-04

Figure 5: TSFJ Series: The Resistors

High values

Components	J04	J06	J09	J13	J23
3KΩ RI	0	0	10	10	10
5KΩ RI	36	56	64	80	136
8KΩ RI	0	0	18	18	18
10KΩ RI	64	80	96	128	202
40KΩ RI	0	2	2	2	2
50KΩ RI	0	4	4	4	4
50KΩ SB	24	32	40	56	88
100KΩ SB	4	4	12	12	20

Medium and low values

Components	J04	J06	J09	J13	J23
30Ω PL	9	17	17	17	33
100Ω PL	60	80	116	156	260
200Ω PL	0	0	16	16	20
300Ω PL	0	0	9	9	8
1KΩ BEX	130	182	398	470	720

E88TSFJ-05

ADS-PC : ANALOG DESIGN SYSTEM - PC

The TSFJ series is fully supported by a complete Computer Aided Design (CAD) system. The ADS-PC tool offers capabilities of schematic entry, analog and digital simulation and symbolic layout, using a standard software package from PCAD.

The ADS-PC software requires a low cost IBM PC AT3 or fully compatible with the following configuration :

- 640 KB RAM, coprocessor 80287

optional : 80386 and 80387 accelerator boards

2MB EMS board

- microsoft parallel mouse
- EGA graphic monitor
- 30 MB hard disk
- laser jet printer

Checking and mask generation are implemented on DEC™, VAX™ and SUN computer systems.

SCHEMATIC GRAPHIC CAPTURE

PC-CAPS™ software, from P-CAD™, provides capture of schematic circuit diagram, allowing the circuit description in a hierarchical way* and using either macrocell from ST library or basic array components.

A database is generated (netlist extraction) for simulation and symbolic layout.

* (symbols can be created to represent schematic designs and can be used as components in higher-level schematics)

ANALOG SIMULATION

The analog simulation is performed using PSPICE™ software and the models library for basic components and macrocells. The result analysis is performed using graphic representation or listing edition.

PSPICE input files are the net list issued from schematic capture, command file, configuration file and simulation environment (active device level description, technology worst cases...).

DIGITAL SIMULATION

PC-LOGS™, from P-CAD™, is a logic simulation program providing primitive symbols library and using commands interactively or in batch mode to set up and perform a simulation.

Simulation results can be displaid to the screen in graphic or tabular forms. PC-LOGS inputs are of two types : a verified netlist and user commands.

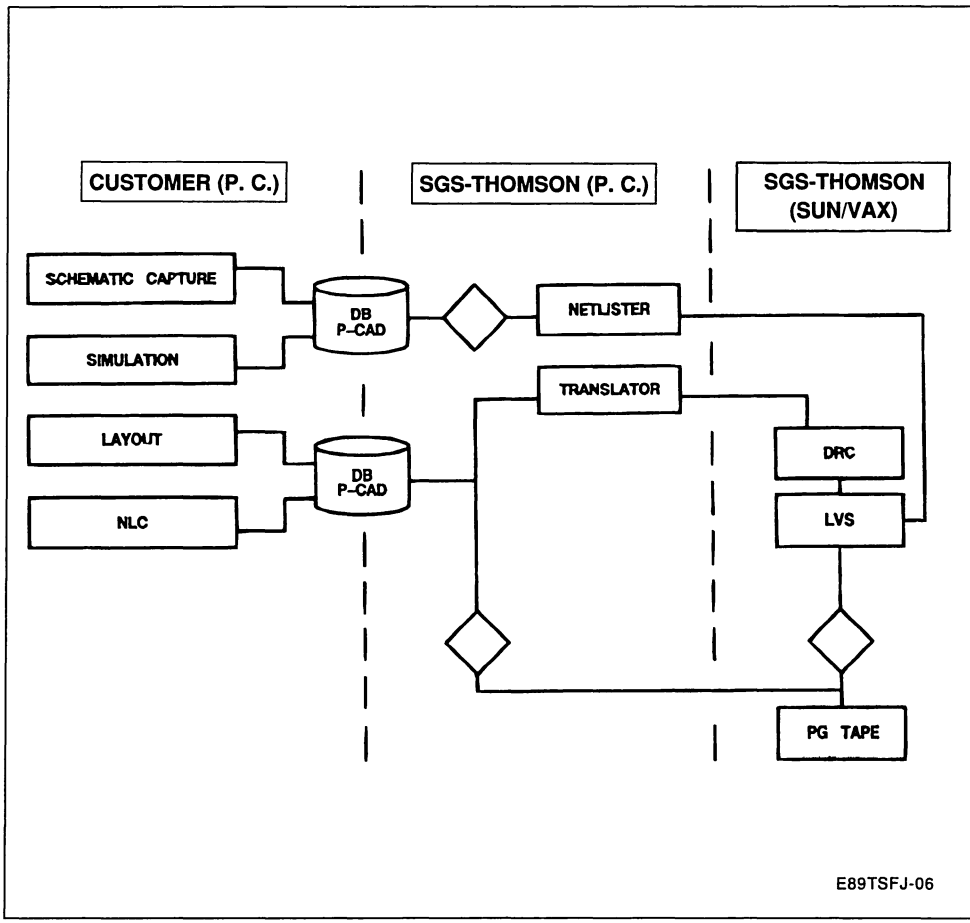
Note: PSPICE is a trademark of MICROSIM.

PLACEMENT AND ROUTING

PC-CARDS™, from P-CAD™, is built around an intelligent database that continually keeps track of components and connectivities.

The on-screen menu includes commands to draw, edit, move, delete, zoom in and out, view selected window.

Figure 6 : ADS - PC Design Flow.



CUSTOMER DESIGN INTERFACE

SGS-THOMSON has developed several interfaces for customers, giving them easy and flexible design approaches for TSFJ mixed analog/ digital bipolar arrays.

User can access ADS-PC system ;
- via the SGS-THOMSON Design centers
- via CAE workstations using a PC configuration and the P-CAD™ software package

According to all of these design possibilities, SGS-THOMSON defined 2 main customer interfaces. Next figure outlines these interfaces. Each interface delimits the responsabilities of customer and SGS-THOMSON during circuit development flow.

	Interface 2	Interface 3
Definition of Circuit Specifications	Customer	Customer
Electrical Description (analog + digital)	Customer	Customer
Test Procedure	Customer	Customer
Graphic Capture + Input Signal Entry	SGS-THOMSON	Customer
Design Verification	SGS-THOMSON	Customer
Simulation (analog + digital)	SGS-THOMSON	Customer
Approval	Customer	Customer/SGS-THOMSON
Place and Route	SGS-THOMSON	Customer
Final Design Release	Customer	Customer/SGS-THOMSON
Test Program Generation + Test Tooling	SGS-THOMSON	SGS-THOMSON
Mask Tooling	SGS-THOMSON	SGS-THOMSON
Prototype Manufacturing	SGS-THOMSON	SGS-THOMSON
Prototype Delivery	SGS-THOMSON	SGS-THOMSON

With interface 3, design can be done either at SGS-THOMSON Microelectronics design center facilities or at customer location.

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C, Voltage Referenced to V–)

Symbol	Parameter	Value		Unit
		Min.	Max.	
V+	Supply Voltage	–0.5	+ 15	V
T_{stg}	Storage Temperature (ceramic)	–60	+ 150	°C
	Storage Temperature (plastic)	–40	+ 125	°C

Stresses above those listed order "maximum rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these on any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (Voltage Referenced to V–)

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max	
V+	Operating Supply Voltage		3		12	V
T_{amb}	Operating Ambient Temperature	Military	–55		+125	°C
		Industrial	–40		+85	°C
		Commercial	0		+70	°C

DC GENERAL ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
	Resistors					
P+	P+ Diffusion	Resistor Value Range	30		420	Ω
		Absolute Accuracy			± 25	%
		Matching (note 1)			± 2	%
		Matching (note 2)			± 6	%
		Temperature Coefficient (1st order)			0.12	%/°C
B_{ext}	Extrinsic Base Region	Resistor Value Range	270		5000	Ω
		Absolute Accuracy			± 15	%
		Matching (1)			± 2	%
		Matching (2)			± 6	%
		Temperature Coefficient (1st order)			0.09	%/°C
R_I	Implanted Resistor	Resistor Value Range	5		50	KΩ
		Absolute Accuracy			± 15	%
		Matching (1)			± 2	%
		Matching (2)			± 6	%
		Temperature Coefficient (1st order)			0.21	%/°C
B_{INT}	Intrinsec Base Region	Resistor Value Range	50		100	KΩ
		Absolute Accuracy			± 25	%
		Matching (1)			± 2	%
		Matching (2)			± 6	%
	Capacitors	Capacitor Value Range	2.5		7	pF
		Absolute Accuracy			± 20	%
V+		Maximum Operating Voltage			20	V
N_{BPC1}		std NPN Transistor (note 3)				
V_{BCB0}	Breakdown Voltage	Collector-base	40			V
V_{BCE0}	Breakdown Voltage	Collector-emitter	18			V
V_{BCS0}	Breakdown Voltage	Collector-substrate	40			V
F_{FE}	Current Gain	@ I_c = 100µA		100		
I_{KF}	Knee Current			5.6		mA
NPWR		Power NPN Transistor (note 3)				
V_{BCB0}	Breakdown Voltage	Collector-base	40			V
V_{BCE0}	Breakdown Voltage	Collector-emitter	18			V
$V_{BCS0}H_{FE}$	Breakdown Voltage	Collector-substrate	40			V
I_{KF}	Current Gain	@ I_c = 10mA		140		
	Knee Current			314		mA

Notes : 1matching between 2 resistors of the same value, closed to each other and with the same orientation on the die.
2matching between 2 resistors of different values, close to each other and with the same orientation on the die.
3or more informations refer to the TSFJ user's manual.
4oltage references are provided by an "ECL reference" macrocell (REFECL) built on a specific tile.
5nput voltages could be supplied by a specific tile called HFECL.
6utput levels are not compatible with standard 10K, 100K ECL series.

DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
PNPS		Substrate PNP Transistor (note 3)				
V_{BCB0}	Breakdown Voltage	Collector-base	40			V
V_{BCE0}	Breakdown Voltage	Collector-emitter	18			V
V_{BCS0}	Breakdown Voltage	Collector-substrate	40			V
H_{FE}	Current Gain	@ I_c = 1µA		160		
I_{KF}	Knee Current			40		µA
		ECL Cells (V_+ = 5V ± 10%)				
V_R	$V_{reference}$	Voltage Reference (note 4)		.97		V
V_{T1}	$V_{reference}$	Voltage Reference (note 4)		3.92		V
V_{T2}	$V_{reference}$	Voltage Reference (note 4)		3.20		V
V_{IL}	Input Voltage	(note 5)			3.6	V
V_{IH}	Input Voltage	(note 5)	4.3			V
V_{OL}	Output Voltage	(note 6)			3.6	V
V_{OH}	Output Voltage	(note 6)	4.3			V

Notes : 1matching between 2 resistors of the same value, close to each other and with the same orientation on the die.
2matching between 2 resistors of different values, close to other and with the same orientation on the die.
3or more informations refer to the TSFJ user's manual.
4voltage references are provided by an "ECL reference" macrocell (REFECL) built on a specific tile.
5nput voltages could be supplied by a specific tile called HF.
6utput levels are not compatible with standard 10K, 100K ECL series.

DIGITAL LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT
(unless otherwise specified, T_{amb} = 25°C, typical process)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max	
		ECL CELLS				
V_S	Voltage Swing			600		mV
T_G	Toggle Frequency	D Type Flip-flop			100	MHz
t_{PLH}	Propagation Delay	NAND2, (FO=1)		1.1		ns
t_{PHL}	Propagation Delay	NAND2, (FO=1)		3.2		ns
		I^2L CELLS (note 1)				
T_G	Toggle Frequency	D Type Flip-flop @ Injection = 1µA @ Injection = 10µA			 160 600	 KHz KHz

Note : 1. I^2L cells have been characterized between 0.1µA and 100µA.

ANALOG LIBRARY, AC ELECTRICAL CHARACTERISTICS ABSTRACT

(unless otherwise specified, T_{amb} = 25°C, typical process)

JOPA1 - Programmable Operational Amplifier (V_{cc} ± 6V, I_{set} = 20µA)

Symbol	Parameter	Test Conditions	Typical Value	Unit
B	Unity Gain Bandwidth	RL = 5KΩ ; CL = 20pF	1	MHz
ϕM	Phase Margin	Av = 1 ; RL = 5KΩ ; CL = 20pF	60,	
Svo	Slew Rate	Av = 1 ; RL = 5KΩ ; CL = 20pF	0.35	V/µs
Av	Open-loop Voltage Gain	RL = 5KΩ ; CL = 20pF	90	dB

JCOMP1 - Programmable Voltage Comparator (LM139 type)

Symbol	Parameter	Test Conditions	Typical Value	Unit
tref	Large Signal Response Time	RL = 5KΩ ; CL = 2pF with Overdrive : 100mV	300	ms
tre	Small Signal Response Time	RL = 5KΩ ; CL = 2pF with Overdrive : 5mV	1	µs
AVD	Large Signal Voltage Gain		87	dB

ANALOG BIPOLAR ARRAY

HIGH FREQUENCY ANALOG BIPOLAR ARRAY

FEATURES

The TSFK09 array is manufactured using a very high frequency technology (Ft of NPN = 3GHz) which allows a 15V maximum supply operating voltage.

- TECHNOLOGY HF2C, 2 METAL LAYERS
- 1 METAL LAYER TO CUSTOMIZE
- 28 BONDING PADS (maximum)
- 188 NPN TRANSISTORS
- 28 PNP TRANSISTORS (placed in peripheral)
- 686 RESISTORS
- MAXIMUM SUPPLY VOLTAGE = 15V

DESCRIPTION

The TSFK09 array is a prediffused bipolar array of components allowing the user to design his specific applications in a short cycle time and with a minimum risk of errors.

The TSFK09 array from SGS-THOMSON Microelectronics is specially intended for use in video, telecommunication, instrumentation and other high frequency applications, but it could be used with benefit for low frequency applications.

Using kit parts for breadboard, the designer has the capability to validate the schematics in the final application environment.

ANALOG ARRAY :

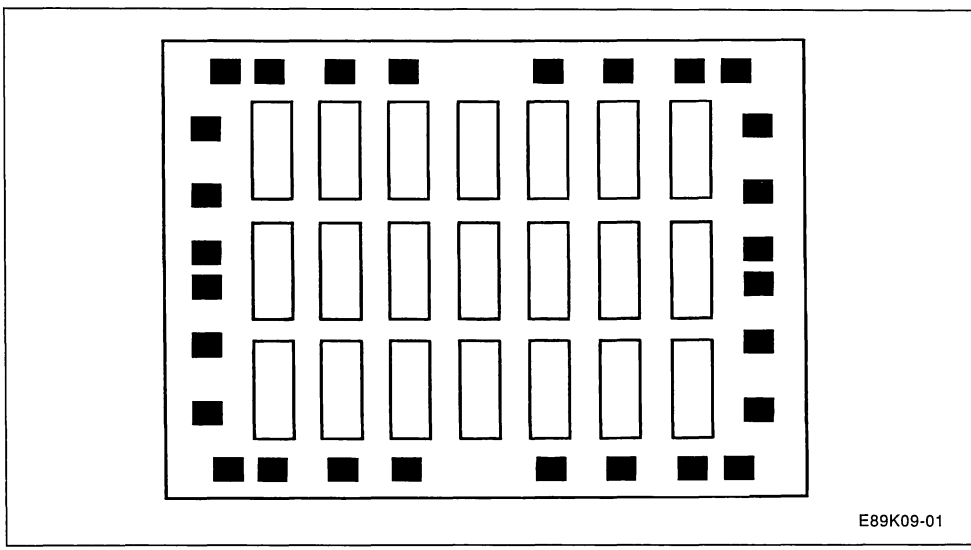
The structure of the TSFK09 based on a regular matrix of 3 x 7 tiles, improves the efficiency of the layout.

Each tile contains :

- 6 QN1 type NPN transistors
- 2 QN2 type NPN transistors
- 100, 200, 400 and 800 P+ type resistors, 1K, 2K, 4K, 8K and 16K Pextrinsic base resistors.

2 independent resistor tubs allow placing of 2 positive power supplies if required.

Figure 1 : TSFK09 Array Architecture.



MAXIMUM VOLTAGE

Volts	NPN	PNP
Collector-base	25	25
Collector-emitter	15	15
Collector-substrate	25	
Base-substrate		25
Emitter-base	5.8	
Base-emitter		25

Resistor voltage = 20V maximum.
Capacitor voltage = ± 20V maximum.

ELECTRICAL CHARACTERISTICS

Current Gain h_{FE}		Resistor Tolerances	Resistors Matching
NPN	110 (@.1mA I 1mA)	± 25%	Same Value Resistor = ± 2%
PNP	60 (@ I=10µA)		
$(F_t)_{NPN}$	3GHz (@ I=1mA)		Different Value Resistor = ± 5%
$(F_t)_{PNP}$	10MHz (@ I=10µA)		

DEVICES MODELING

All basic components are available whit SPICE models, for the 4 different kinds of transistors.
The parameters are:

Symbol	Parameter	QN1	QN2	QN4	PNP	Unit
I_S	Transport Saturation Current (10^{-16})	2.1	4.19	10.5	0.5	A
B_F	Ideal Maximum Forward Beta	136	136	136	73	
V_{AF}	Forward Early Voltage	35	35	35	41	V
I_{KF}	Knee Current	14.7	29.4	73.5	43.10^{-3}	mA
R_B	Zero Bias Resistance	292	146	58.4	190	Ω
R_{BM}	Minimum Base Resistance	56.5	28.2	11.3	61.3	Ω
R_E	Emitter Resistance	9.8	4.9	1.96	8.90	Ω
R_C	Collector Resistance	79.5	53.9	32.6	8	Ω

ANALOG SWITCHED CAPACITOR FILTER ARRAYS

SGS-THOMSON MICROELECTRONICS

TSGF SERIES

MASK PROGRAMMABLE FILTERS ANALOG SWITCHED CAPACITOR FILTER ARRAYS

FEATURES

- HCMOS MASK PROGRAMMABLE SWITCHED CAPACITOR FILTERS : Fast Design Turn-around Time (5 to 6 weeks average), Thanks To Gate Array Approach
- INTEGRATION OF ANY KING OF CLASSIC, NON-CLASSIC FILTERS : Bandpass, Lowpass, Highpass, Band Reject...
  Cauer, Chebychev, Butterworth, Legendre...
- FILTER ORDER : From 2 to 12
- CASCADABLE STRUCTURE : Higher Order Achievable
- NO EXTERNAL COMPONENTS REQUIRED TO REALIZE THE FILTERING FUNCTION
- ADDITIONAL OPTIONS AVAILABLE ON CHIP :
  - Uncommited Op-Amps (for anti-aliasing and/or smoothing filters, half or full wave rectifiers...) ;
  - Internal Divider (sampling frequency generated ; from external clock) ;
  - Output Sample-and-Hold
  - Tsgf Series Provides :
  - Leapfrog Structure For Very Low Sensitivity Filters ;
  - Cascadable Biquadratic Cells For Non-classic Filter Design
- TSGF SERIES FULLY SUPPORTED BY "FILCAD"® CAD SOFTWARE FROM FILTER SYNTHESIS AND SIMULATION UP TO LAYOUT
  - Application Notes
  - Evaluation Boards
  - Input Signal Frequency : 0 to 30KHz
  - Signal To Noise Ratio : 60 to 85dB
- POWER SUPPLY : Dual ± 5V
  Single 0 - 10V
  Single 0 - 5V
- ADJUSTABLE POWER CONSUMPTION : 0.5mW to 20mW per Filter Order
- QUALITY FACTOR : UP to 50
- PASS-BAND GAIN : UP to 40dB
- INPUT SENSITIVITY : 1mV RMS (min)

DESCRIPTION

TSGF series is a family of Mask Programmable Filters (MPFs) developed by SGS-THOMSON Microelectronics.

The TSGF product range is composed of 3 switched capacitor filter base arrays, TSGF04, TSGF08 and TSGF12 providing filter integration capability from 2nd to 12th order.

TSGF04/08/12 are using "gate array" technique : the filter customization is achieved only by the final metallization mask.

Therefore TSGF series provide users with filter integration solutions with very fast design turn-around time : 5 to 6 weeks up to delivery of full tested prototypes.

TSGF04/08/12 base arrays provide on chip all necessary functions to realize all kind of filters :

- transconductance amplifiers
- switches
- capacitor fields
- sample-and-hold
- non overlapping phase generator

Additional on-chip integration capabilities are offered by TSGF products such as :

- prefiltering and post filtering functions antialiasing and smoothing filters)
  - cosine filter
  - output sample-and-hold driving
  - power consumption adjustment
  - output DC level adjustment.

TSGF series provide users a fast and complete design solution for their specific filter circuits resulting in highly accurate and reliable products thanks to switched capacitor technique.

But SGS-THOMSON filtering approach is not only limited to the Mask Programmable Filter (MPF) products.

TSGF SERIES PRODUCT RANGE

Part Number	Number of on-chips Filters	Filter Order	Uncommitted Op-amps	Clock	Output Sample-and Hold	Packages
TSGF04	1	2 to 4	1	Internal Oscillator* TTL/CMOS Levels	External* Driving	PDIP 8-14 Pins CDIP 14 Pins SO Wide 16 Pins
TSGF08	1	4 to 8	2	1 Clock Input TTL/CMOS Levels	Internal Driving	PDIP 8-16 Pins CDIP 16 Pins SO Wide 16 Pins
TSGF12	1 or 2	8 to 12	2	2 Clock Inputs TTL/CMOS Levels	External* Driving	PDIP 16-18-20 Pins CDIP 16-18-20 Pins SO Wide 18-24 Pins

Users are given :

- Standard Device Filters which are general purpose filters designed by SGS-THOMSON from the 3 TSGF base arrays.
  - TSG 87xx developed on TSGF04 filter array (2nd to 4th order)
  - TSG 85xx developed on TSGF08 filter array (4th to 8th order)
  - TSG 86xx developed on TSGF12 filter array (8th to 12th order).

Refer to data sheets of these standard filter products.

- "Gate Array" Filters which are the TSGF04, TSGF08, TSGF12 filter arrays described in this data sheet.
- "Standard Cell" Filters

By offering TSGF-like macrocells in its library, the mixed analog/digital TSGSM Standard Cell family also provides filtering capabilities and then can extend integration possibilities offered by TSGF series.

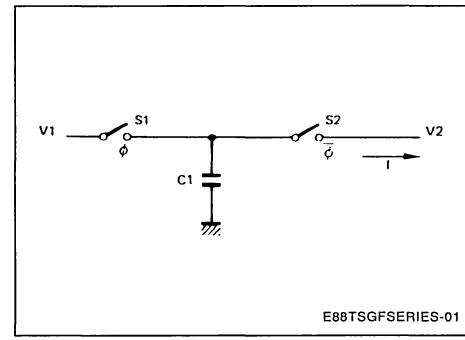
For example higher than 12th order filters or circuit combining filters with digital and analog functions on the same chip are achievable with TSGSM Standard Cells.

SWITCHED CAPACITOR TECHNIQUE

SGS-THOMSON TSGF products are active filters where resistors are replaced by capacitors which are switched at a frequency, named sampling frequency (F_i).

Figure 1 is showing the basic principle of switched capacitor technique.

Figure 1.



The 2 switches (S1 and S2) are controlled by 2 complementary and non overlapping clock phases.

During the phase $\varnothing = 1$ (S1 on, S2 off) the charge stored in C1 is :

$Q1 = C1.V1$ (1)

During the phase $\overline{\varnothing} = 1$ (S1 off, S2 on) the charge stored in C1 becomes :

$Q2 = C1.V2$ (2)

During a complete clock period $Ti = \frac{1}{Fi} = \varnothing + \overline{\varnothing}$

the transferred charge is :

$\Delta Q = Q1 - Q2 = C1\ (V1 - V2)$ (3)

During this Ti period, this charge flow is equivalent to a current, I :

$\Delta Q = C1\ (V1 - V2) = I.Ti$ (4)

$$I = C1.Fi\,(V1 - V2) = \frac{C1\,(V1 - V2)}{Ti} \quad (5)$$

Comparing (5) with Ohm's law applied to a resistance :

$$I = \frac{V1 - V2}{R} \quad (6)$$

The equivalent resistor is then :

$$Req = \frac{Ti}{C1} \quad (7)$$

Then, with (7), a RC product becomes :

$$Req.\,C = \frac{C}{C1}\,Ti \quad (8)$$

SWITCHED CAPACITOR FILTER BENEFITS

In active filters, the time constant is fixed by the RC product but the component values R and C used with the Op-amp are absolutely uncorrelated : so trimmings, tunings are very often needed to obtain an accurate template. On the other hand, with switched capacitor networks, only capacitor ratios are used. These ratios are obtained with capacitors integrated on the same chip. The available accuracy is 0.1% to 0.5% whatever the temperature condition may be.

As the time constant is fixed by capacitor ratio, fully integrated filters are achievable without trimming. In addition, as shown in (8) the time constant RC is proportional to the sampling period Ti : the filter cut-off frequency can be shifted by tuning the sampling clock frequency without any change on the shape of response curves.

SWITCHED CAPACITOR FILTER FEATURES

Key Points	Results
• Monolithic Filter. • The coefficients of the filter transfer function are completely determined by : – a single crystal controlled clock frequency – and ratioed capacitors • Fully HCMOS Integrated Filters • Switched capacitor filters are sampled-and-hold circuits.	• Board Size Reduction. • High Accuracy Template. • Stability in Temperature and Time. • High Order Filter Achievable. • No Adjustment. • Clock Tunable Cutoff Frequency. • Low Power. • No External Components. • Ease and Safety of Use. • Antialiasing prefiltering is required if the input signal is wide band. • Smoothing post filtering may be used to avoid spectral rays around the sampling frequency.

SWITCHED CAPACITOR FILTER ARRAY ARCHITECTURE

Analog switched capacitor filter arrays, TSGF series, are processed with a 3.5/2 polysilicon layer/1 metal layer HCMOS process.

SGS-THOMSON offers 3 filter base arrays, TSGF04, TSGF08 and TSGF12, providing filtering capabilities from 2nd to 12th order.

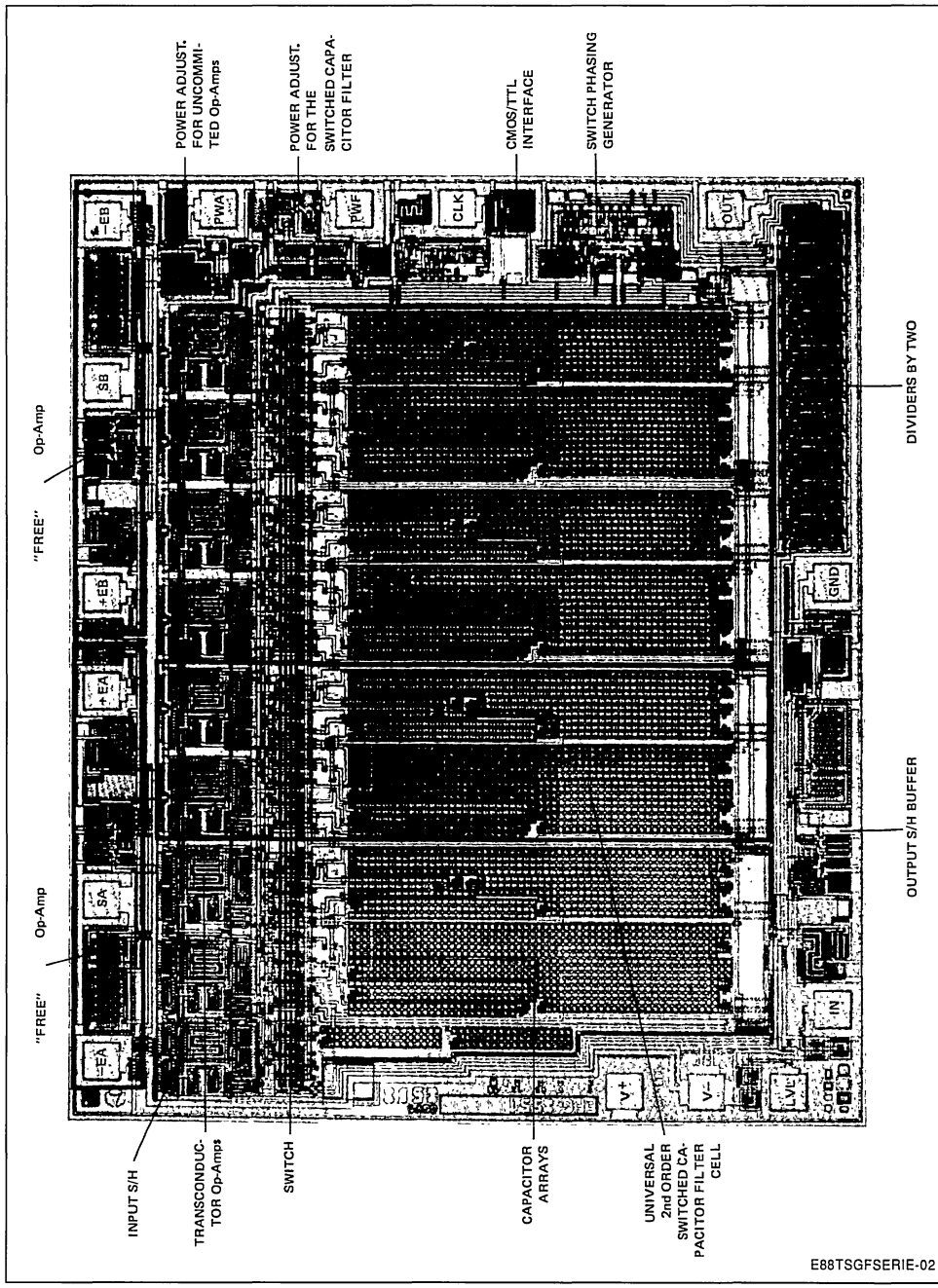
The 3 arrays are designed around a "Universal biquadratic filter cell", SGS-THOMSON patented. This cell consists of 2 adder integrators using a transconductance amplifier, switches, and capacitor fields. Fields of capacitors are composed of hundred unit capacitors (0.1pF) and then provide high and accurate capacitor values.
Figure 2 shows the TSGF08 chips, outlining all functions available on TSGF filter arrays :

- Universal 2nd order Filter Cell. Clock divider generating internal sampling frequency from external clock.
- Non overlapping phase generator.
- Input Sample-and-Hold.
- Uncommitted free Op-amps. Power consumption Adjustment cells for filter and Op-amps.
- Output Sample-and-Hold.

The internal sampling frequency Fi can be set from 500Hz to 700KHz by an external oscillator (or an internal one with TSGF04 base wafer).

When the external available clock frequency is higher than 700KHz, the set of Mask Programmable dividers by 2 is used to adapt the external clock frequency to the sampling frequency. In any case the external clock frequency must be lower than 5MHz.

Figure 2 : TSGF08 CHIP.



As the ratio Fi/Fc between sampling frequency Fi and selected filter frequency Fc is a constant, designers can move the filter characteristics (central or cut-off frequency) only by tuning the clock.

A 10V power supply, either 0V and 10V, or - 5V and + 5V, gives the best performances : maximum output swing of 8V.
The TSGF filters can also operate with a standard 0/5V power supply. In that case the maximum output swing is 2.2V.

Typical power consumption is 0.5mA per filter order. This power consumption is user adjustable between 0.1mA and 2mA with an external resistor, depending on the frequency range.

The power consumption adjustment is also provided to the uncommitted operational amplifiers : the bias current must be increased when a high gain - bandwidth product is required.

These uncommitted Op-amps give the designer the capability to create auxiliary circuits like voltage gain, prefiltering and post filtering functions half or full wave rectifier functions, or local oscillator (refer to application notes AN-061, AN-069, AN-070, AN-075).

The offset voltage of TSGF products is typically a few millivolts, with a 300mV max depending of the filter type.

Moreover, there is a possibility to adjust the filter output DC levels, thanks to an external bias voltage applied on "LVL" pin. Automatic offset compensation can be done by mean of one uncommitted on-chip operational amplifier, as indicated in Application note AN-069.

The TSGF products feature a high input impedance (typ. : 3MΩ) and a low output impedance (typ. : 10Ω) allowing then cascadable filter network in order to achieve higher than 12th order.

The output buffers are configurated as sample-and-hold amplifiers which can drive a 1KΩ load resistance and a 100pF load capacitance.

On the TSGF04 and TSGF12 an external sample-and-hold clocking allows to connect the filter output directly to an analog to digital converter (Optional ; see fig. 7).

In addition some particular switched capacitor cells have been implemented on the first 2 integrators of each chip allowing realization of special functions like :

- cosine filter
- complementary high pass filter
- exact bilinear leapfrog filter.

Figure 3a : TSG8512 : 7th Order Cauer Low 0 pass Filter.

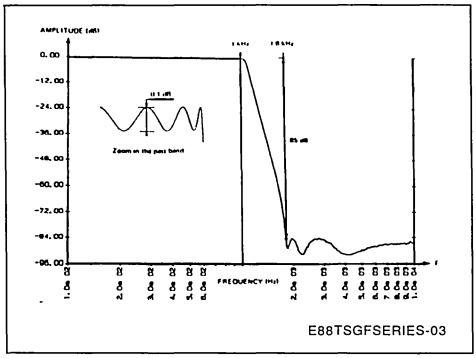
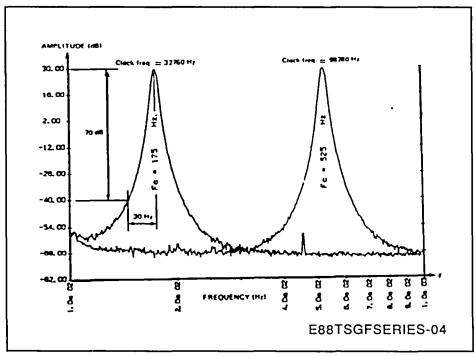


Figure 3b : TSG8551 : 8th Order High-Q Band pass Filter (Q = 35).



BENEFITS

With the TSGF series of SGS-THOMSON, designers are given unique "Gate Array" filter products for the replacement of their passive/active filters or the design of new filters.

The TSGF04/08/12 provide then with gate Array technique 3 complete arrays where all functions necessary to realize the filter function and its external circuit environment are available on chips.

The switched capacitor process permits the realization of very accurate and fully integrated filters and breaks down the equipment production costs by providing fully tested filters parts : tuning or adjustment of external components are no more necessary with TSGF series.

Figures 3A, 3B is showing 2 examples of Standard Filters designed with the TSGF08 matrix.

APPLICATIONS

TSGF products from SGS-THOMSON can integrate all filtering functions (replacement of active or passive filters...) and then can be implemented very quickly into an application/equipment requiring a filter with a maximum input signal frequency of 30KHz.

Mask Programmable Filters (MPFS) typical applications are :

- audio filtering/processing
- signal/frequency detection
- scrambling/coding
- spectrum analysis
- process control
- remote control
- harmonic analysis
- equalization
- frequency tracking
- alarm systems
- robotics
- anti-knock system
- data acquisition (before A/D and after D/A converters)
- automatic answering
- inwarding
- spreech processing
- security system (coding, recognition)
- sonar detection
- mobile radio
- modems

BLOCK DIAGRAMS

Figure 4 outlines the mean features and options offered by each of the 3 MPF arrays by showing TSGF04, TSGF08 and TSGF12 block diagrams.

Figure 4a : TSGF04 Block Diagram.

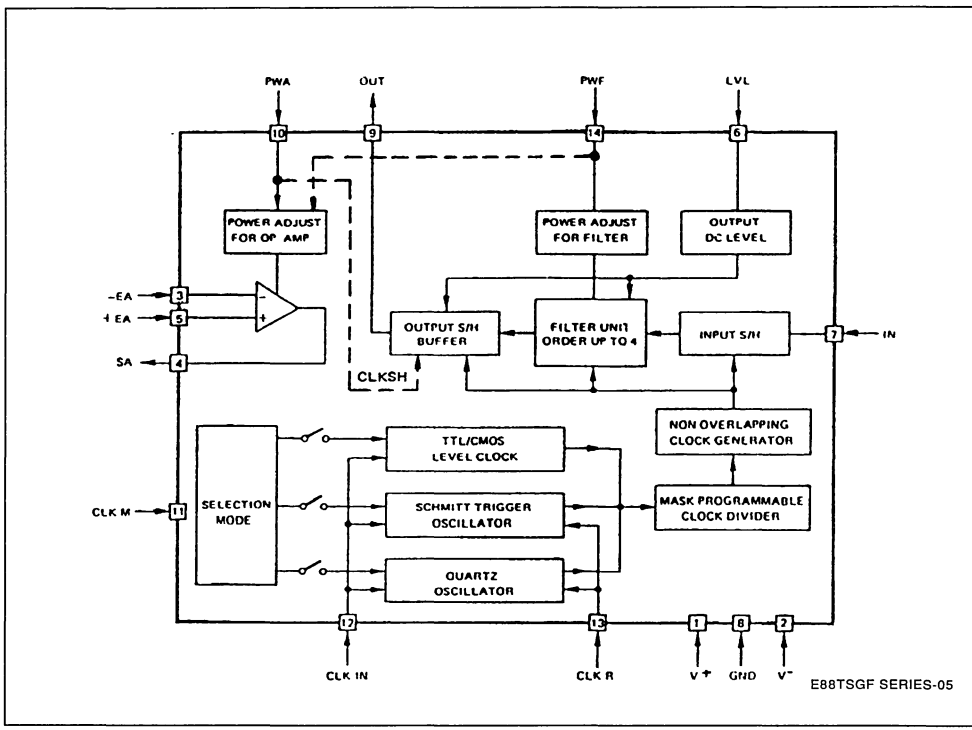
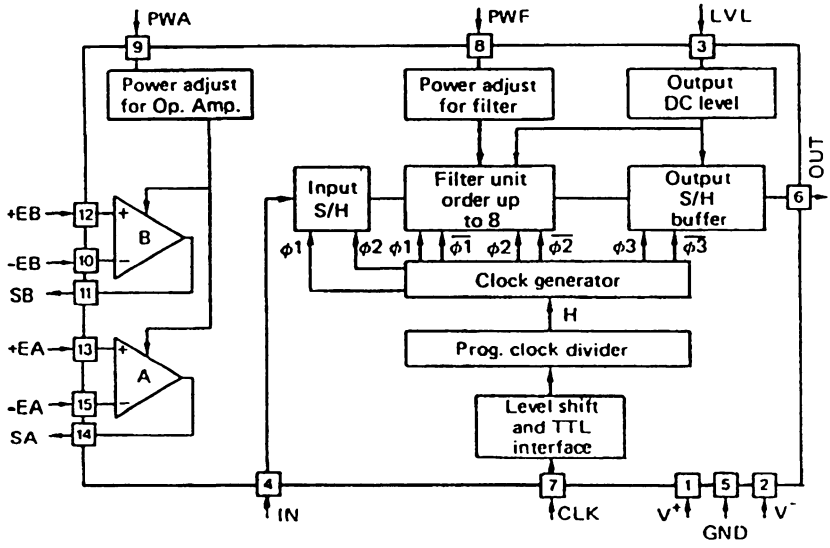


Figure 4b and 4c : TSGF08 and TSGF12 Block Diagrams.



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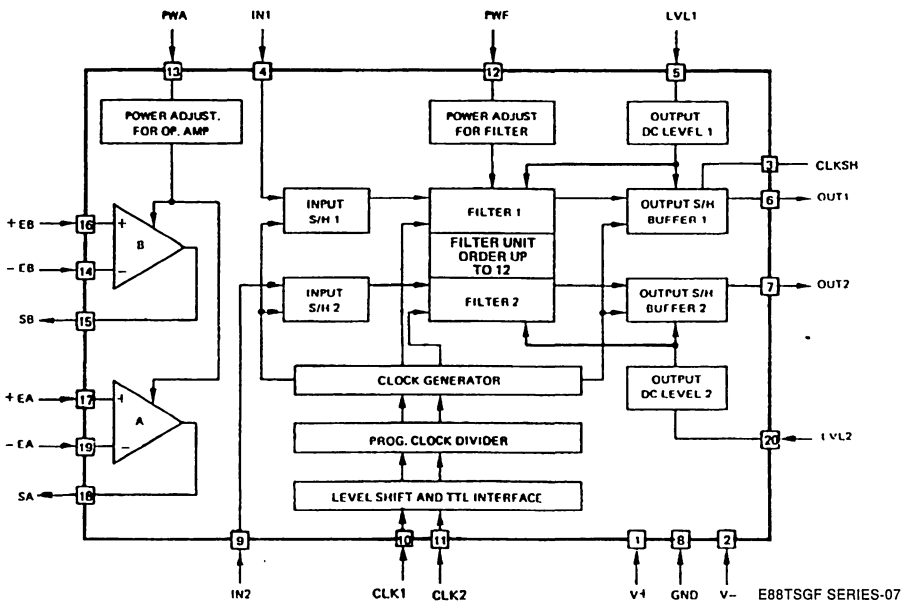


E88TSGF SERIES-07

PIN DESCRIPTION

The table below gives the pin description of the 3 MPF arrays, TSGF04 TSGF08 and TSGF12. The pin assignment is given for the extended and complete version of each array, i. e. with all the available on-chip options connected to the package.

Name	Pin Type	TSFG04 N°	TSGF08 N°	TSGF12 N°	Function	Description
V^+	Input	1	1	1	Positive Supply	
V^-	Input	2	2	2	Negative Supply	
LVL	Input	6	3	LVL1 5 LVL2 20	Output DC Level Adjustment	Filter output DC level adjustment when connecting a potentiometer between V^+ and V^- with is middle point to LVL. When no adjustment is needed, LVL pin is connected to GND.
IN	Input	7	4	IN1 4 IN2 9	Filter Input	
GND	Input	8	5	8	General Ground	GND voltage = $\frac{V^+ + V^-}{2}$
OUT	Output	9	6	OUT1 6 OUT2 7	Filter Output	
CLK	Input	See CLKIN	7	CLK1 10 CLK2 11	Clock Input	TTL/CMOS Level Compatibility
PWF	Input	14	8	12	Filter Power Adjustment	Filter power consumption can be chosen by connecting a resistor between PWF and GND (or V^+). Stand by mode is obtained by connecting PWF to V^- (or non connected)
PWA	Input	10*	9	13	Op Amp Power Adjustment	Idem PWF but for Op Amp (PWA)
–EB	Input		10	14	Inverting Input Op Amp B	
SB	Output		11	15	Output Op Amp B	
+EB	Input		12	16	Non Inverting Input Op Amp B	
+EA	Input	5	13	17	Non Inverting Input Op Amp A	
SA	Output	4	14	18	Output Op Amp A	
–EA	Input	3	15	19	Inverting Input Op Amp A	
NC			16		Non Connected	
CLKSH	Input	10*		3	S/H Clock Input	External Driving Clock of Output Sample-and-hold
CLKIN	Input	12			Clock Input	See TSGF04 Clock Oscillator Section
CLKR	Output	13			Clock Pin for External Oscillator	For TSGF04, external RC or crystal oscillator are connected to CLKIN and CLKR pins. See TSGF04 clock oscillator section
CLKM	Input	11			Clock Selection Mode	Connected to GND or V^- see TSGF04 clock oscillator section

For TSGF04 when external driving clock of output sample-and-hold (CLKSH) is used, PWF realizes the power adjustment of both uncommitted Op-amp and filter.

Note: For other packing pin-out, refer to package drawings and pin-out at the end of data sheet.

FUNCTIONAL DESCRIPTION

INTERNAL CLOCK DIVIDER (CLK)

The internal sampling frequency F_i can be fixed from 500Hz to 700KHz (F_i can be used between 700KHz and 1MHz with some limitations) by an external oscillator (or internal one with TSGF04 filter array). When the external clock frequency F_e, is higher than 700KHz, a mask programmable on-chip divider is used to adapt available clock frequency to the sampling rate.

	TSGF04	TSGF08	TSGF12
Number of Divide by 2 Available Per Chip	8	10	8
Max. F_e/Fi Ratio	256	1024	256

In any case, the external clock frequency F_e must be less than 5MHz.

Example : The TSG8510 features (TSG8510 is a standard filter based on TSGF08 array) :

F_e max = 1.5MHz and F_i max = 750KHz then

$$\frac{F_e}{F_i} = 2$$

only one divider by 2 is used for this filter (which is the case of most of SGS-THOMSON' general purpose filters).

Note : As the internal clock divider is mask programmable, the ratio Fe/Fi is fixed for each filter. The change of this ratio is possible but results into a new part number.

ADJUSTMENT OF OUTPUT DC LEVEL (LVL)

The output DC offset voltage can be removed thanks to an external bias voltage applied on "LVL" pin, as shown on figure 8.

However automatic offset compensation can be implemented by using one of the uncommitted on-chip Op-amps, as indicated in application note AN-069 (see fig. 9 in AN-069).

The offset voltage of TSGF filters is typically a few millivolts, with a 300mV max, depending on the type of the filter.

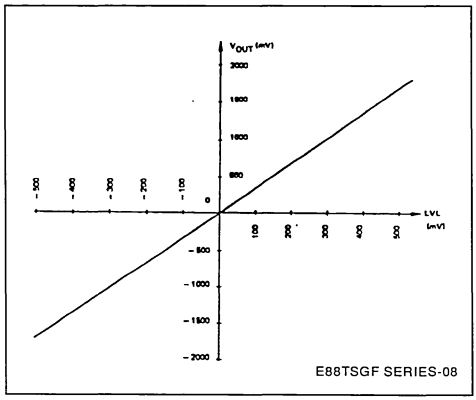
A drift of this offset voltage can be observed when user increases the power consumption of the filter with an external resistor connected to PWF pin. So when the filter operates at high frequencies, a compromise exists between the filter frequency response performance and its output DC offset voltage.

When no DC output level adjustment is required, LVL pin has to be connected to the GND voltage.

The level gain, LG, of each filter can be deduced from the curve representing V_{OUT} = f (LVL). This curve is filter dependent.

For example the TSG8510 presents following curve shown in figure 5 (measured with F_e = 256KHz, I_{PWF} = 100µA) :

Figure 5 : Output DC Voltage Adjustment from LVL Pin.



The TSG8510's level gain is :

$$LG = \frac{VOUT}{LVL} \cong \frac{1000}{300} 3.3$$

For example if one TSG8510 presents a 100mV offset voltage at its output, user must apply an external bias voltage LVL = 30mV to compensate it.

FILTER POWER ADJUSTMENT (PWF)

The filter power consumption can be chosen by connecting an external resistor, R_{PWF} between PWF and GND (or V+) pins.

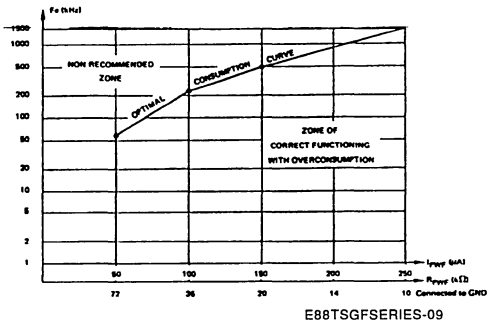
This power adjustment operates the variation of the bias current of the integrators used in the switched capacitor filter. This current, I_{PWF}, can be low when filter operates at low cut-off frequencies ($F_c \cong 1$KHz), but must be increased at high cut-off frequencies ($F_c \cong 20$KHz), in order to charge and discharge the capacitors at a higher, rate.

As a result, an optimal choice of I_{PWF} bias current can be deduced from the curve representing I_{PWF} = f (F_e), F_e being the external clock frequency applied on CLK pin.

This curve is dependent on the filter. For example, as shown in figure 6, the TSG8510 presents following characteristics :

Example : if the cutoff frequency of the low pass TSG8510 filter has to be set at 3.4KHz, user must apply the external clock frequency F_e = 75.3 x 3.4 = 256KHz.

Figure 6 : TSGF10 user's Guide for IPWFand RPWF Choise.



The User's guide for I_{PWF} choice indicates :

- optimal I_{PWF} = 100µA
  R_{PWF} = 35kΩ
- non recommanded zone for I_{PWF} 100µA
  Operation within this area can lead to increase the ripple in the pass band and to decrease the stop band attenuation.
- zone of correct functioning with over consumption for I_{PWF} > 100µA.

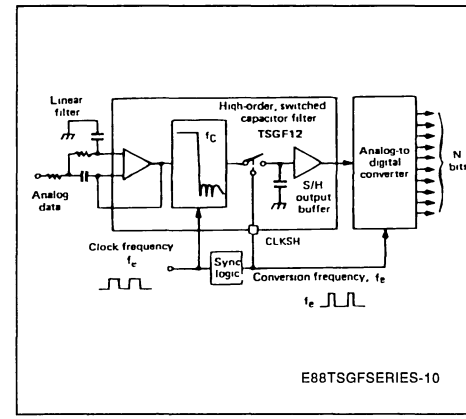
Note : Power consumption choice has to be prioritized when major concern in TSGF design is the frequency response (gain versus frequency). The output DC offset voltage comes in 2nd position in that case.

EXTERNAL DRIVING OF OUTPUT SAMPLE-AND-HOLD

This facility allows the filter output to be connected directly to an analog-to-digital converter, as illustrated in figure 7.

The clock signal which enters on the CLKSH pin must be synchronous with the sampling frequency. As a result, the external clock frequency F_e must be the sampling frequency F_i (the on-chip divider does not have to be used).

Figure 7 : External Driving of Output Sample and Hold (example).



The clock signal applied on CLKSH pin has to be optimized in order to read a settled signal issued from the switched capacitor filter.

On the example shown in figure 7, a 12th order low pass filter makes an ideal antialiasing filter to precede data conversion. The filter precludes the need for oversampling when driving the A/D converter.

CLKSH option is only available on TSGF04 and

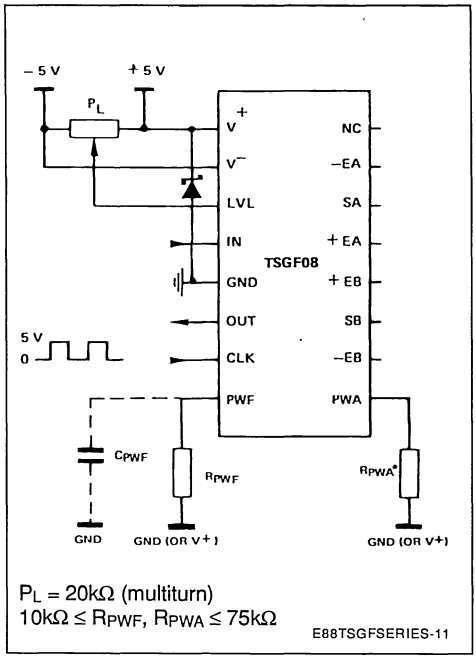
USE OF THE MPF WITH - 5V/+5V DUAL POWER SUPPLY

The adjustment of the DC output level of the M.P.F. is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F.). If no output DC adjustment is required, the LVL pin can be directly connected to GND.

The consumption of the filter can be also adjusted by means of an external resistance connected between GND (or V^+) and the PWF pin of the circuit.

The consumption can thus be chosen to match the particular application.

Figure 8 : Example of a TSGF08 Fed in Dual Supply : +5V, 0, -5V.



If the Op-Amps are not used, RPWA has not to be connected between PWA and GND.

The stand-by mode is obtained by strapping the PWF pin to V⁻ (or non connected).

The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V⁻ (or non connected).

The clock levels are TTL, but CMOS levels are accepted. With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V, between - 4.5V and + 3.5V.

A capacitor C_{PWF} can be added in parallel with R_{PWF} in order to improve the clock feedthrough rejection : (Typical value C_{PWF} = 33pF).

As for all CMOS circuits operating with dual power supply (- 5V, 0, + 5V), it is advised to use clamping diodes (Threshold voltage less than 0.6V) (Schottky is preferrable) in order to avoid transients during power up which could drive TSGF circuits over their maximum ratings. Only 1 Schottky diode between GND and V+ is sufficient for TSGF products.

USE OF THE MPF WITH 0/10V SINGLE POWER SUPPLY

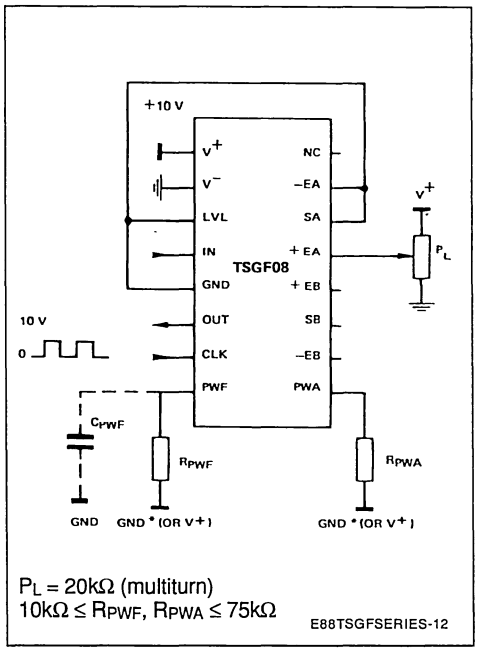
In this case, V⁻ is the reference ground of the circuit and GND must be adjusted to + 5V by means of the potentiometer P_L (V+ - V⁻)/2), or by using a simple bridge divider. But in that case small resistors values (2kΩ) have to be used in order to set GND at a low impedance value.

The adjustments of the DC output level of the M.P.F. of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4V upper the GND level.

With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V between 0.5 and 8.5V.

Figure 9 : Example of a TSGF08 FED, in Single Power Supply 0 - 10V.



* GND is used, when the user provides the 5V voltage.

USE OF THE MPF WITH 0/5V SINGLE POWER SUPPLY

In this case, V⁻ is the reference ground of the circuit

and GND must be adjusted to + 2.5V by means of the potentiometer P_L ($(V+ - V^-)/2$), and one Op-amp used as buffer in order to provide a low impedance on GND reference.

Otherwise, without Op-amp, a simple bridge divider is sufficient, but small resistor values (2kΩ) have to be used in order to set GND at a low impedance value.

The other adjustments are achieved exactly like previously except for bias resistance of the filter and of the operational amplifiers (R_{PWF} and R_{PWA}), whose must be exclusively to V+.

The clock levels must be CMOS levels. With these previous conditions, the output linear dynamic range of the M.P.F. is about 2.2V, between 1.2 and 3.4V.

ANTI-ALIASING AND SMOOTHING

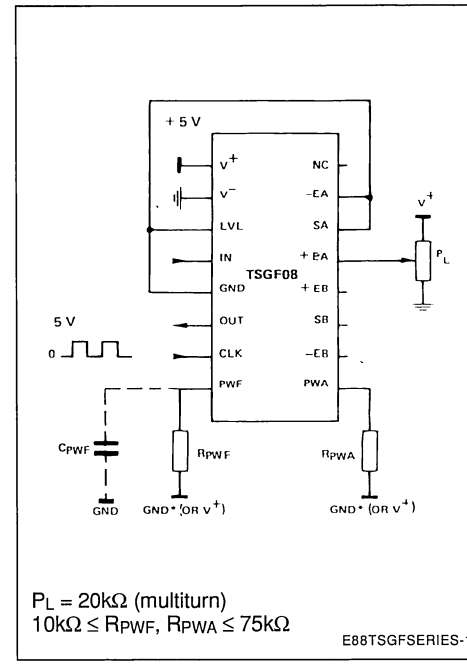
Anti-Aliasing

The switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (F_i) equal, at least, to double of the upper frequency (F_c) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 11 where the entire spectrum to transmit appears around F_i, 2 F_i, 3 F_i... and so on.

Thus, all spectrum components of the signal contained around these frequencies are transmitted by the M.P.F., oppositively to the desired result.

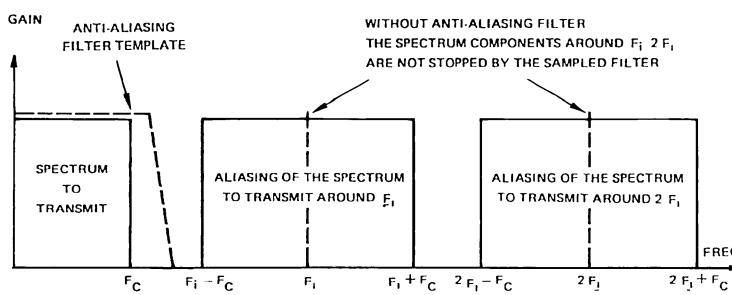
To cancel the effects of this phenomenon, it is required, before all sampled systems, to filter all the spectrum components of the intput signal upper than F_i - F_c. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.

Figure 10 : Example of a TSGF08 FED in Single Power Supply 0-5V.



*GND is used, when the user provides the 2.5V Voltage.

Figure 11.



Phenomenon of the spectrunm aliasing

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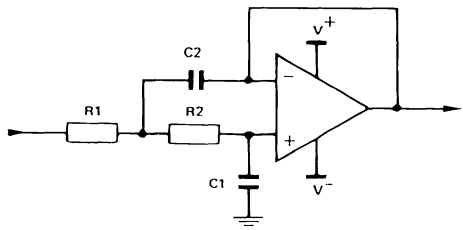
- Without anti-aliasing filter : Spectrum to transmit ≠ transmitted spectrum
- With anti-aliasing filter : Spectrum to transmit = transmitted spectrum

The selectivity of this filter depends upon the F_i/F_c ratio.

If F_i/F_c 200, a RC filter (first order low-pass) is sufficient.

If F_i/F_c 200, a SALLEN-KEY structure (second order low-pass) must be used. This structure and its relationships are described (figure 12). In there relationships, F_c is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and in order to correct the sin x/x effect, ξ must have a value around 0.7.

Figure 12.



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R1 = R2 = arbitrary value
Fc = cut-off frequency for the antialiasing filter.
An optimal choice is Fc = 2 x cut-off frequency of the main filter
x = damping coefficient ; the optimal value is 0.7

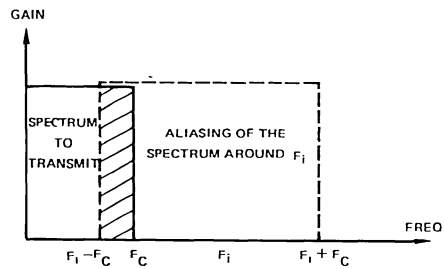
$$C1 = \frac{\xi}{2\pi R1 Fc}$$

$$(C1 = \xi 2 - C2)$$

$$C2 = \frac{1}{2\pi\xi R1 Fc}$$

SALLEN-KEY structure (second order low-pass Filter) for anti-aliasing and smoothing.
Note : If F_i/F_c 2 (figure 13), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.

Figure 13.



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When Fi/Fc<2, the spectrum component included between Fi-Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter.

Smoothing

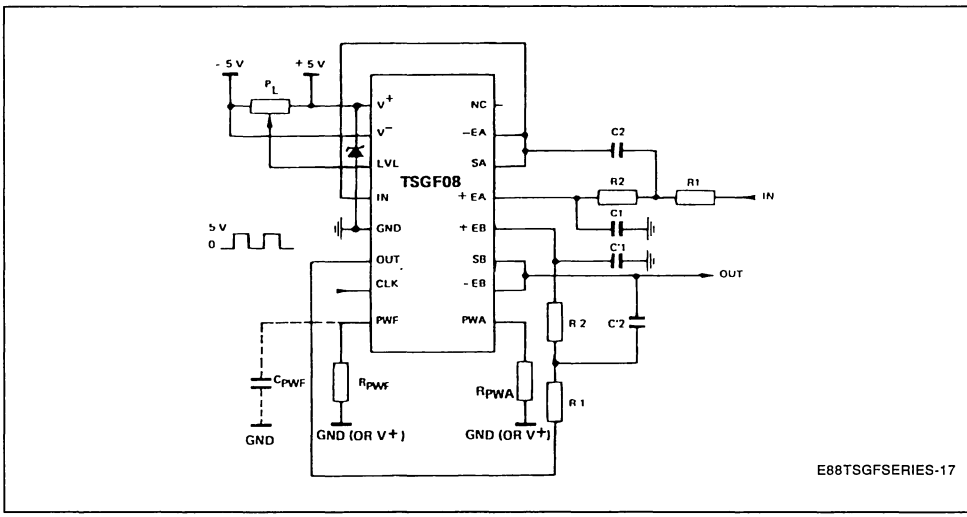
As the signal obtained at the output of the M.P.F. is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 12).

Hardware implementation

In order to make easier anti-aliasing and smoothing. SGS-THOMSON has designed, on the TSGF chip one or, two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 14).

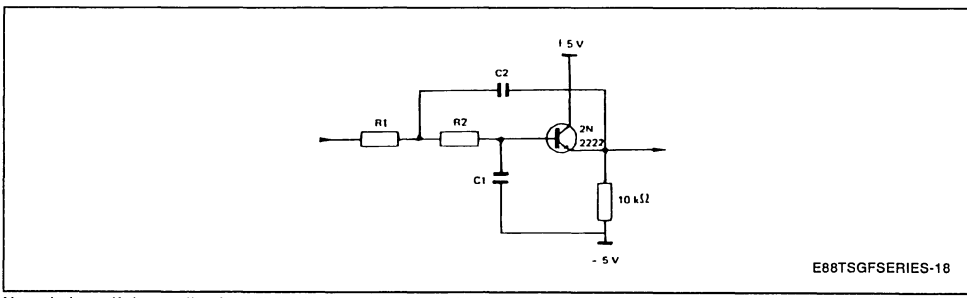
On the other hand, in the most of M.P.F.'s, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around F_i.

Figure 14. M.P.F. With anti-aliasing and smoothing filters.



P_L = 20kΩ (multiturn)
10kΩ ≤ R_{PWF}, R_{PWA} ≤ 75kΩ
R1,R2,C1,C2 } See anti-aliasing
R'1, R'2,C'1,C'2 } and smoothing considerations

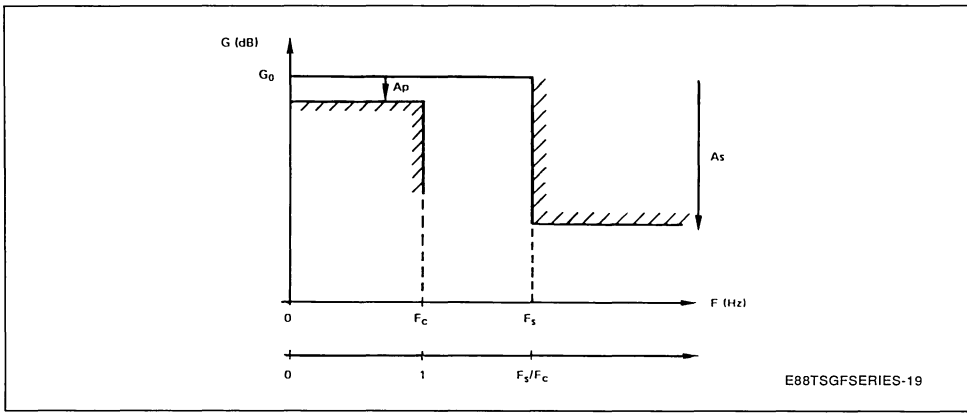
Figure 15. Second order low-pass Filter (SALLEN-KEY STRUCTURE) with a transistor replacing the operational amplifier.



Nonetheless, if the application allows it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator...).
In this case, the circuit shown Figure 15 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described in Figure 12 (second order low-pass), in the same way as the corresponding relationships.

CUT-OFF FREQUENCY DEFINITION

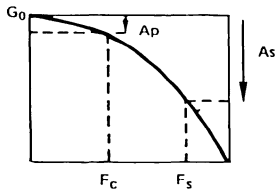
Figure 16 : Design Specifications.



The cut-off frequency Fc is the passband limit frequency as defined on the design specifications above mentioned. The maximum value of the attenuation variation in the passband : Ap is 3dB for Butterworth, Bessel and Legendre filters (figure 17a), and is called passband ripple for Chebychev (figure 17b) and Cauer filters (figure 17c).

The passband ripple is design dependent and between 0.05dB and 0.2dB with TSGF standard filters. The parameters Go called passband gain is the maximum value of the gain in the passband, and may have low variation from part to part.

Figure 17a.



E88TSGFSERIES-20

Figure 17b.

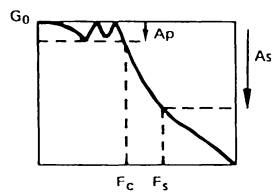


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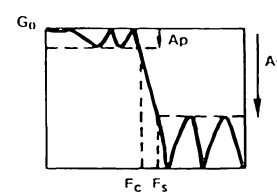
Figure 17c.



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ELECTRICAL SPECIFICATION

The following electrical characteristics are common to the 3 base filter arrays TSGF04, TSGF08 and TSGF12, because theirs structures are designed with the same basic components.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

T_{amb} = 25°C, V+ = 5V, GND = 0V, V– = – 5V, I_{PWF} = 100µA (unless otherwise specified)

Symbol	Parameter	Value	Unit
V+	Positive Supply Voltage	– 0.15 to + 7	V
V-	Negative Supply Voltage	– 7 to + 0.15	V
V	Voltage to any Pin (except for GND)	(V–) – 0.3 to (V+) + 0.3	V
T_{op}	Operating Temperature Range	T_{min} – 5°C to T_{max} + 5°C	°C
T_{stg}	Storage Temperature Range	– 60 to + 150	°C

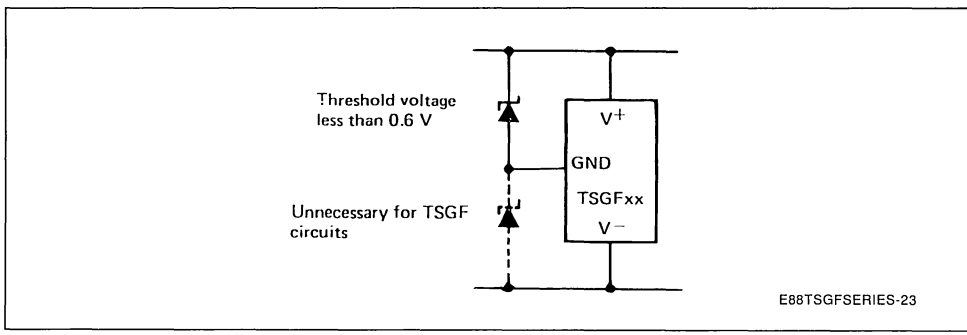
WARNING : DUAL POWER SUPPLY (- 5V, 0, + 5V)

Although TSGF circuits are internally gate protected to minimize the possibility of static damage, MOS handling and operating procedure precautions should be observed. Maximum rated supply voltages must not be exceeded. Use decoupling networks to remove power supply turn on/off transients, ripple and switching transients.

Do not apply independently powered signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken :

As for all CMOS circuits operating with three supply voltages (V+, GND, V-), it is advised to use clamping diodes (Schottky is preferable), in order to avoid transient during power up that would drive the circuit over its maximum ratings (see figure 18).

Figure 18 : Application Hint for CMOS ICs with Three Supply Voltages.



ELECTRICAL OPERATING CHARACTERISTICS

$V^+ = 5V$, GND = 0V, $V^- = -5V$, $T_{amb} = 25°C$, $I_{PWF} = 100\mu A$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	4	5	6	V
V^-	Negative Supply Voltage	−6	−5	−4	V
V_{OUT}	Output Voltage Swing (*)	$(V^-) + 0.5$		$(V^+) - 1.5$	V_{PP}
V_{IN}	Input Voltage (*) (with filter gain = 0dB)	$(V^-) + 0.5$		$(V^+) - 1.5$	V_{PP}
I_{PWF}	Bias Current on PWF (stand-by mode by connecting PWF to V^-)	50		250	µA
V_{IL}	TTL Clock Input "0" (**)			+ 0.8	V
V_{IH}	TTL Clock Input "1" (**)	2			V
T_{CP}	Ext. Clock Pulse Width	80			ns
R_{IN}	Input Resistance	1	3		MΩ
C_{IN}	Input Capacitance			20	pF
R_{OUT}	Output Resistance		10		Ω
C_L	Load Capacitance			100	pF
R_L	Load Resistance	0.1	1		kΩ

Note : with supply (0, + 10V) : same specifications
with single supply (0, + 5V) : contact SGS-THOMSON sales office or representative.
(*) Depending on I_{PWF} current
(**) TTL levels are referenced to GND voltage

Other filter's characteristics, such as noise, power supply rejection ratio, total harmonic distortion... are filter dependent. As a result, for such characteristics, SGS-THOMSON can only guarantee the lower level of performance for each parameter, as indicated below. (this lower level has been determined from measurements on a set of hundred different TSGF filters, as shown in figure 19).

PSRR + > 2dB : V+ Power supply rejection ratio.

PSRR − > 10dB : V^- Power supply rejection ratio.

V_n 1mVrms : V_n is the total output noise voltage measured in the passband of the filter.

SNR > 57dBm/600 *** : Signal to noise ratio with V_{IN} = 775mVrms.

SNR > 65dBV : signal to noise ratio with V_{IN} = 2Vrms.

THD < 0.1% : Total harmonic distortion.

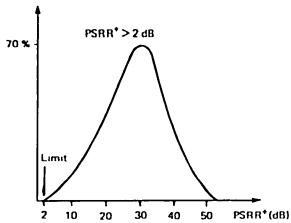
As such characteristics are not predictable from simulation results, their typical values are provided from measurements of the customized filter prototypes. (These measurements could be performed by SGS-THOMSON on special request).

These typical values, obtained with TSGF products, are better than the lowest level guaranteed, and designers can get a more accurate idea about them by two means.

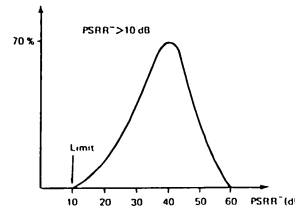
1) Such characteristics are given for general-purpose filters. Refer to TSG85xx, 86xx, 87xx data sheets.

2) Figure 19 gives histograms of the 5 parameters discussed above. These histograms indicate the distribution of the typical value of the considered parameter over a set of hundred different TSGF filters. (Note that the aim of these histograms indicate the dispersion of the considered characteristic for a given TSGF filter).

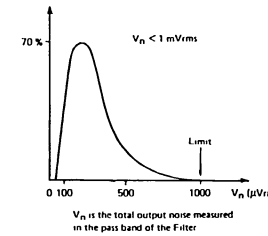
Figure 19 : Distribution of Typical Value Over a set of Hundred Different TSGF Filters.



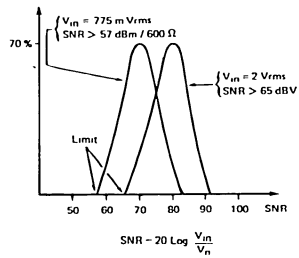
E88TSGFSERIES-24



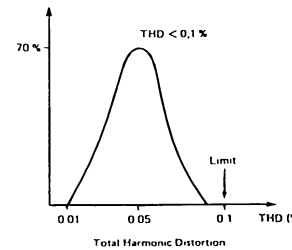
E88TSGFSERIES-25



E88TSGFSERIES-26

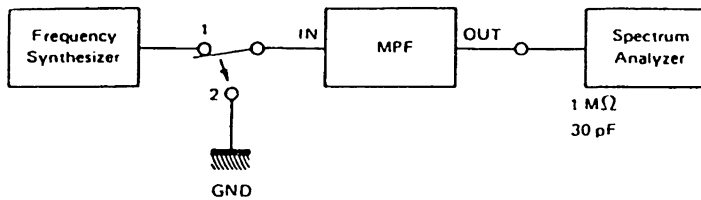


E88TSGFSERIES-27



E88TSGFSERIES-28

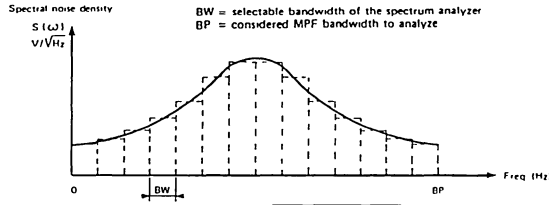
Figure 20 : Method of Noise Measurement.



E88TSGFSERIES-29

Position 1 : Calibration of the spectrum analyzer to 0dBV (1Vrms).
Position 2 : Measurement with filter input connected to GND.

Figure 20 : (continued).



We obtain theoretical noise voltage : $Vn(Vrms) = \sqrt{\int_0^{BP} S^2(\omega) \cdot d(\omega)}$

and measured noise voltage : $Vn\ (Vrms) = \sqrt{\sum_{k=1}^{BP_{BW}} S^2(k) \,.\, BW}$

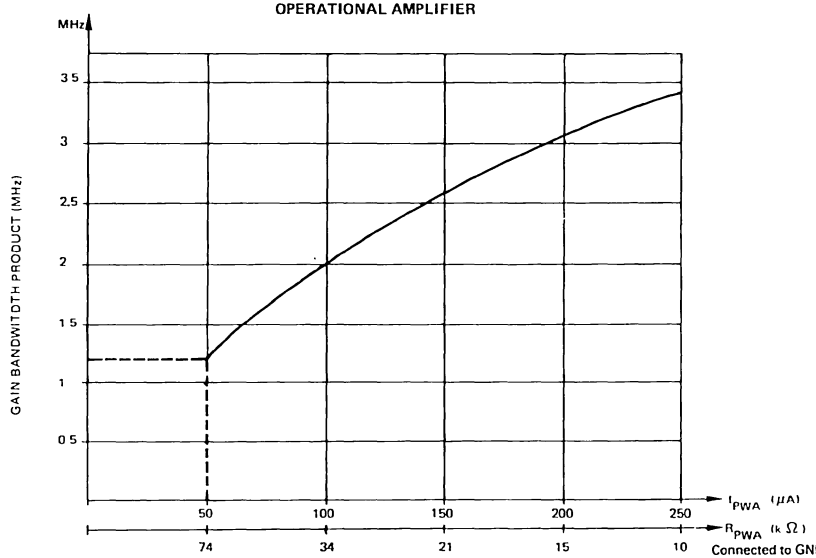
E88TSGFSERIES-30

UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIERS

$V^+ = 5V$, GND = 0V, $V^- = -5V$, $T_{amb} = 25°C$, RL = 2kΩ, $I_{PWA} = 100\mu A$ (unless otherwise specified)

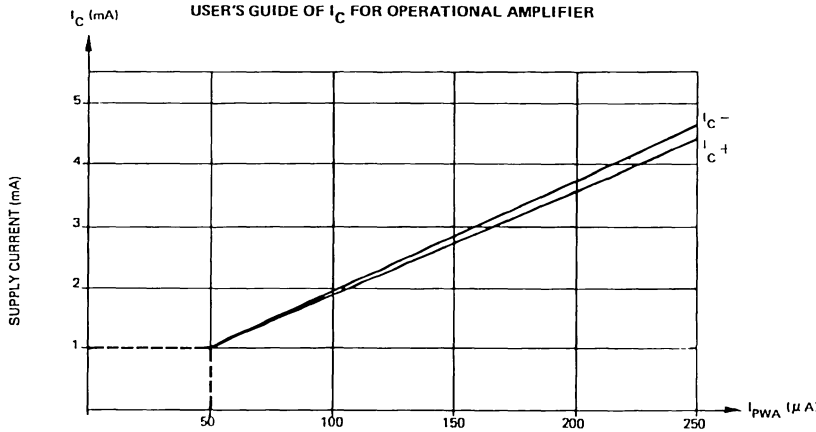
Symbol	Parameter	Min.	Typ.	Max.	Unit
G_0^+ G_0^-	DC Open Loop Gain (without load)	60 60	75 75		dB dB
G_{Bp}	Gain Bandwidth Product (without load)	1	2		MHz
V_{IO}	Input Offset Voltage (without load)		± 5	± 10	mV
$V_{OP}P$	Output Swing		− 4.5 3.5	− 4.7 3.7	V V
I_{IB}	Input Bias Current (without load)		± 5	± 10	nA
SVR	Supply Rejection (without load)	60	65		dB
CMR	Common Mode Rejection V_{CM} = 1V (without load)	60	65		dB
R_O	Output Resistance		10		Ω
Ia^+ Ia^-	Supply Current		2.6 2.6	3.2 3.2	mA mA
SR^+ SR^-	Slew Rate	2 2	5 6		V/µs V/µs

USER'S GUIDE OF I_{PWA} AND R_{PWA} FOR UNCOMMITTED ON-CHIP OPERATIONAL AMPLIFIER



E88TSGFSERIES-31

USER'S GUIDE OF I_C FOR OPERATIONAL AMPLIFIER



E88TSGFSERIES-32

CAD SOFTWARE : FILCAD

In order to take full advantage of the Mask Programmable filter TSGF approach for Semicustom applications, SGS-THOMSON has developed a comprehensive software package called FILCAD® to cover all the development steps, starting from the feasibility evaluation of the customer's specifications, up to the single-metal interconnection routing required for the MPF customization.

More specifically, the FILCAD system gives the designer strong assistance during the following steps :

- Evaluation of MPF solutions well suited to specific filter circuit requirements,
- Filter synthesis, leading to a switched capacitor electrical schematic,
- MPF filter simulation (performed with MPF capacitor capabilities),
- Schematic capture and routing of the optional connections,
- Layout file generation, and final verification performed by accurate post-routing simulation.

All FILCAD modules run on VAX® under VMS operating System, and are linked together as shown in Figure 21. All modules are fully described in the TSGF's User's manual (Vol. 5 of SGS-THOMSON ASIC User's Manuals).

The entry to FILCAD is the customer filter specification which can be provided to SGS-THOMSON in different forms :

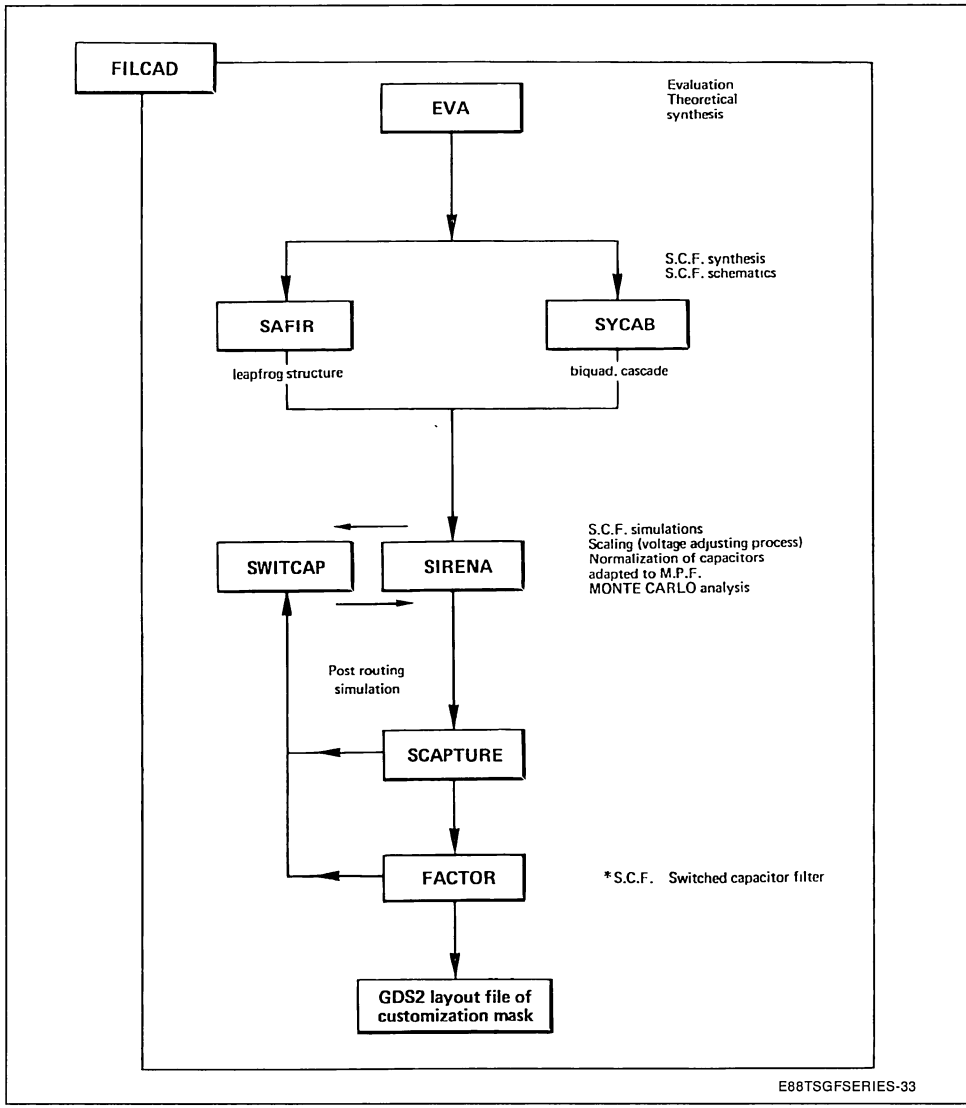
- amplitude - phase - group delay templates
- poles and zeros
- biquadratic cell coefficients
- polynomial transfer functions

In addition SGS-THOMSON can perform feasibility study of customer specific filter circuits. In a order for customers to get fast and accurate answer, SGS-THOMSON generates a feasibility analysis TSGF questionnaire that customers are kindly required to complete. This questionnaire is available on request at SGS-THOMSON Design centers or nearest sales office or representative.

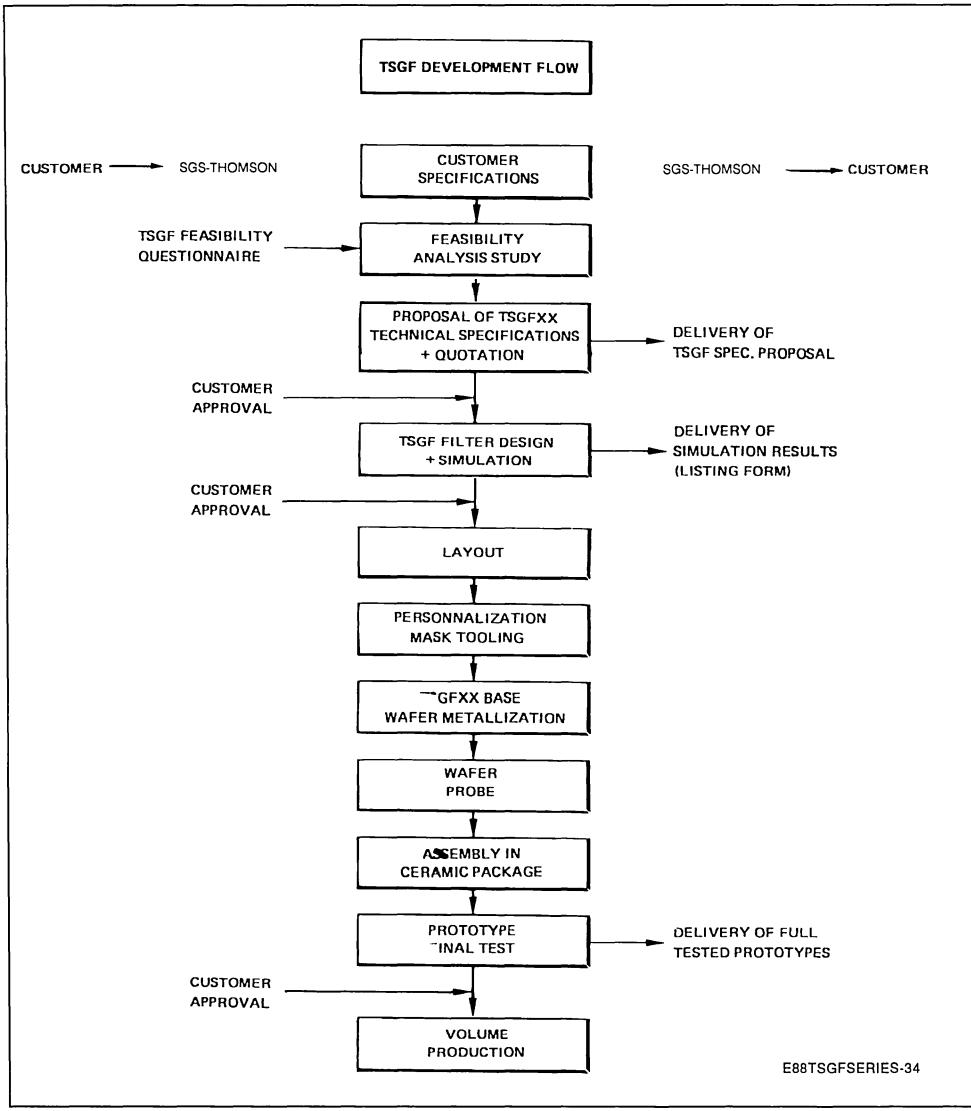
MPF® and FILCAD® are registered trademarks of SGS-THOMSON.

FILCAD, CAD software package developed by SGS-THOMSON for Switched Capacitor Filter designs, TSGF series, is also available for mixed analog-digital TSGSM Standard Cells or Full custom circuits integrating TSGF-like filtering functions.

Figure 21.



SWITCAP is a trademark of Columbia University



SGS-THOMSON proposes presently 2 design interfaces to customers for the design of their filter circuits with TSGF series :

- design entirely done by SGS-THOMSON at Design Centers ;
- design done by customer up to simulation and then completed by SGS-THOMSON.

The table following outlines customer and SGS-THOMSON respective responsibilities for these 2 design interfaces.

DESIGN INTERFACES

Design Step	FILCAD Software	Int 2	Int 3
Theoretical Syntehsis	EVA	SGS-THOMSON	Customer
Switched Capacitor Filters Schematics before Scaling	SYCAB or SAFIR	SGS-THOMSON	Customer
Final Schematics	SIRENA (SWITCAP)	SGS-THOMSON	Customer
Additional Simulation	SIRENA (SWITCAP)	SGS-THOMSON	Customer
Approval		Customer	SGS-THOMSON
Schematics Capture	SCAPTURE	SGS-THOMSON	SGS-THOMSON
Layout - Personnalization Mask Generation	FACTOR	SGS-THOMSON	SGS-THOMSON
Post Routing Simulation	SIRENA (SWITCAP)	SGS-THOMSON	SGS-THOMSON

DOCUMENTATION AND SUPPORT

In order to bring users the maximum support on switched capacitor TSGF filter arrays, SGS-THOMSON generated a complete set of documentation and tools which are available on request :

- TSGF User's Manual
- Application Notes (included)

– AN052 : How to choose a filter in a specific application

– AN061 : implementation and applications around

- Standard MPFS

– AN069 : A supplement to the utilization of switched capacitor filters.
AN070 : Band Pass and Band Stop Filters.

– AN075 : Signal detection and sinewave generation.

- MPF evaluation boards.
- TSGF feasibility/analysis questionnaire.

In addition specialists can be contacted within SGS-THOMSON Microelectronics Filter Design Centers.

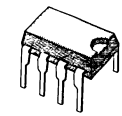
2nd TO 4th ORDER ANALOG FILTER

With the TSGF04 array, the user is given 2 different pin-out configurations :

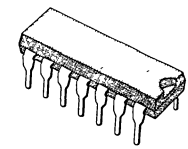
- 8 pin DIL only the filter up to 4th order is accessible.
- 14 pin DIL version where in addition, one uncommitted Op-amp and one internal oscillator capability are offered.

When the external driving of output sample-and-hold is used (CLKSH pin), PWF pin realizes the power adjustement of both uncommited Op-Amp and filter unit.

TSGF04 are also available in SO wide package version (0.3 inch) : 16 pin version only.



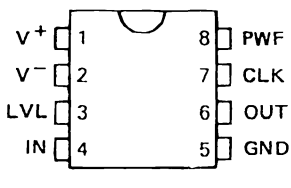
P
DIP-8
(Plastic Package)



P
DIP-14
(Plastic Package)

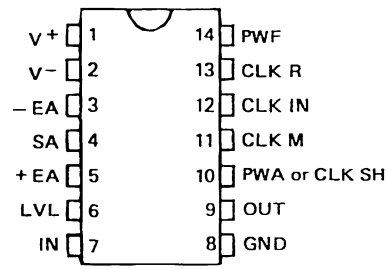
TSGF04
BLOCK DIAGRAM
See figure 4 (E88TSGFSERIES-05)

PIN CONNECTIONS



E88TSGF04-01

8 pins : FILTER ONLY
Compatible with TSGF08



E88TSGF04-02

14 pins : FILTER
: + 1 Op - Amp

CLOCK OSCILLATOR

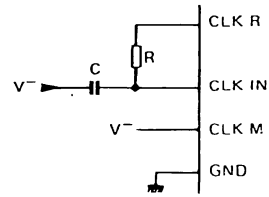
The TSGF04 base accepts external compatible TTL/CMOS clocks on CLKIN pin and provides an internal oscillator performed either by RC or crystal connected between CLKIN and CLKR pins.

The clock selection mode is provided by CLKM pad which can be connected to V- or GND voltage levels. This connection is realized by two means, depending on the package type chosen :

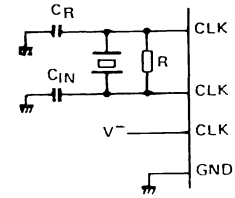
- with 14-pin package, via CLKM pin.
- with 8-pin package, by internal connection readily performed, only on custom filters.

(Note that CLKM pin connected to V+, allows the selection of the internal crystal-controlled oscillator, but the selection by CLKM connected to V- is recommended).
The different possibilities are shown below:

- two internal oscillator modes :
  - RC
  - Crystal

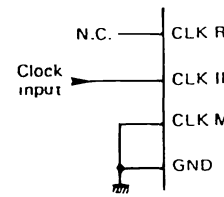


E88TSGF04-03



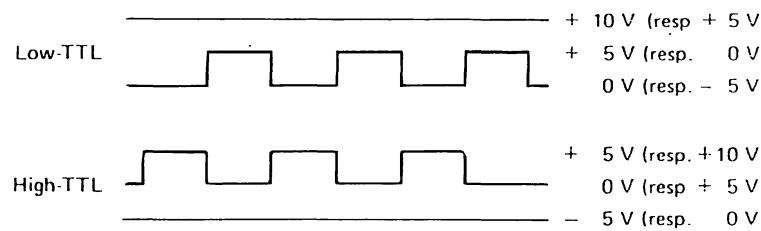
E88TSGF04-04

- three external clocks :
  - low-TTL
  - high-TTL
  - CMOS



E88TSGF04-05

The "low-TTL" and "high-TTL" clock levels are :



E88TSGF04-06

For each package version, the following tables resume, the availability of the different clocks, in terms of the power supply.

Note that in 8-pin version, the clock mode (CLKM) is internally set to GND voltage, except in the case of CMOS clock and 0-5V power supply, where CLKM is internally connected to V- voltage.

8-pin Package			
	0/5V	0/10V	– 5/+ 5V
Low-TTL	NO	C	C
High-TTL	NO	YES	YES
CMOS	C	YES	YES
RC Mode	NO	NO	NO
Crystal Mode	NO	NO	NO

C = Customization option.

14-pin Package			
	0/5V	0/10V	– 5/+ 5V
Low-TTL	NO	C	C
High-TTL	NO	CLKM=GND	CLKM=GND
CMOS	CLKM=V–	CLKM=GND	CLKM=GND
RC Mode	CLKM=V–	CLKM=V–	CLKM=V–
Crystal Mode	CLKM=V–	CLKM=V–	CLKM=V–

ELECTRICAL OPERATING CHARACTERISTICS

WITH SINGLE SUPPLY VOLTAGE

T_{amb} = 25°C, V + = 10V, V – = 0V, GND = 5V (unless otherwise specified)

CLKM	Parameter	Min.	Typ.	Max.	Unit
GND	Threshold Voltage		1.5		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	1	1.25	1.5	V
	Corresponding Voltage on CLKR		– 5		V
	Low Threshold Voltage on CLKIN	1.5	– 1.25	– 1	V
	Corresponding Voltage on CLKR		+ 5		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

ELECTRICAL OPERATING CHARACTERISTICS (continued)

WITH DUAL SUPPLY VOLTAGE
T_{amb} = 25°C, V + = 5V, V – = – 5V, GND = 0V (unless otherwise specified)

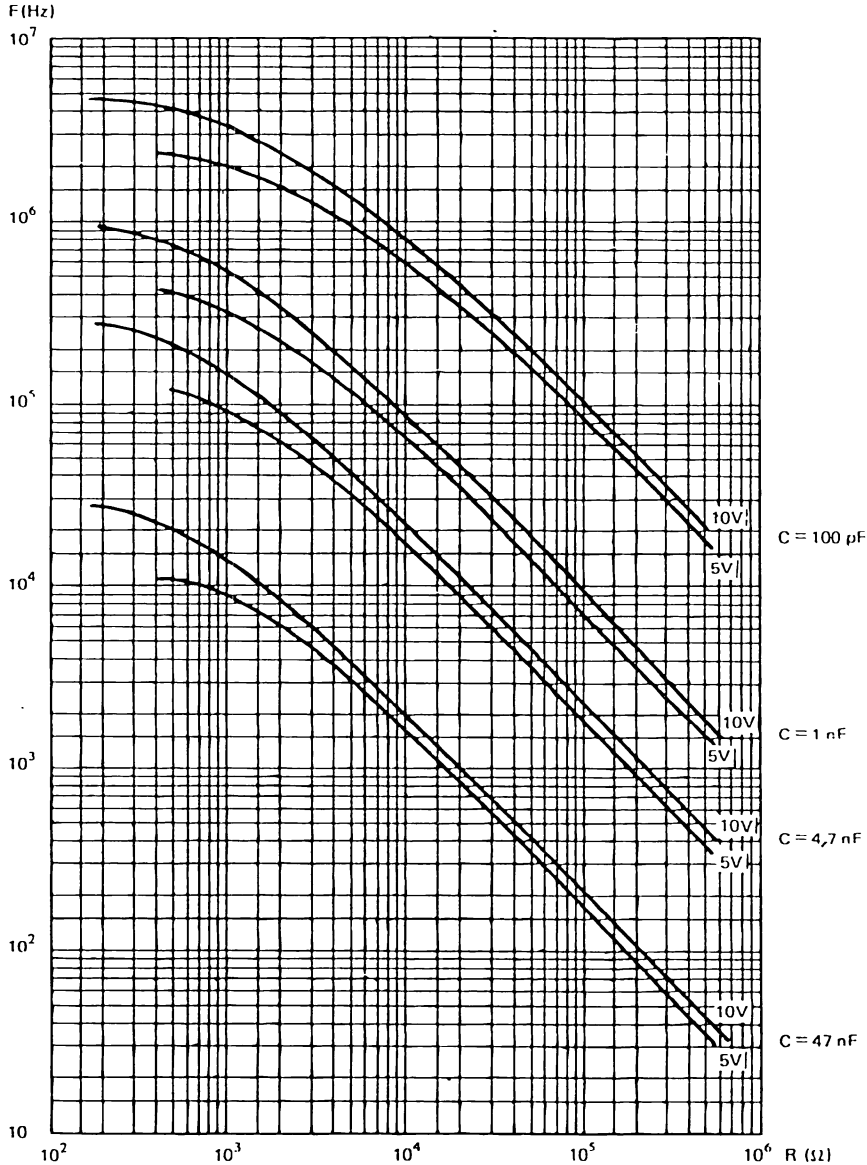
CLKM	Parameter	Min.	Typ.	Max.	Unit
GND	Threshold Voltage		6.5		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	6	6.25	6.5	V
	Corresponding Voltage on CLKR		0		V
	Low Threshold Voltage on CLKIN	3.5	3.75	4	V
	Corresponding Voltage on CLKR		+ 10		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

WITH SINGLE SUPPLY VOLTAGE
T_{amb} = 25°C, V + = 5V, V – = 0V, GND = 2.5V (unless otherwise specified)

CLKM	Parameter	Min.	Typ.	Max.	Unit
GND	Threshold Voltage		3.8		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	3	3.2	3.4	V
	Corresponding Voltage on CLKR		0		V
	Low Threshold Voltage on CLKIN	1.5	1.8	2	V
	Corresponding Voltage on CLKR		+ 5		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

INVERTING TRIGGER FUNCTIONING FREQUENCY VARIATION AS FUNCTION OF R

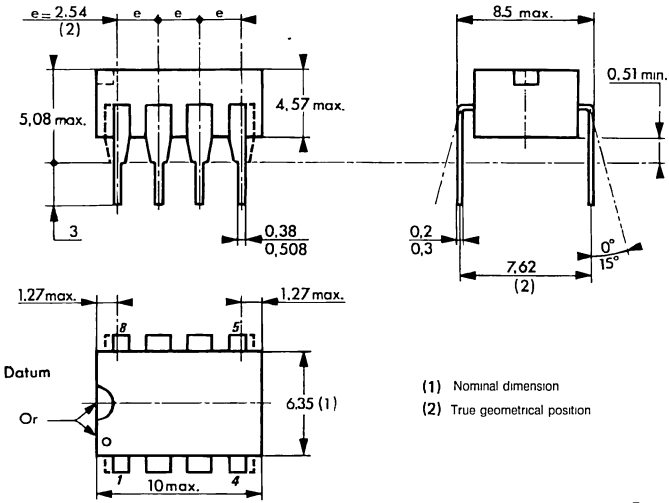
With internal RC oscillator mode, the user's guide for R and C choice is given by the following curves and for both supply voltages : 0.5V, 0.10V.



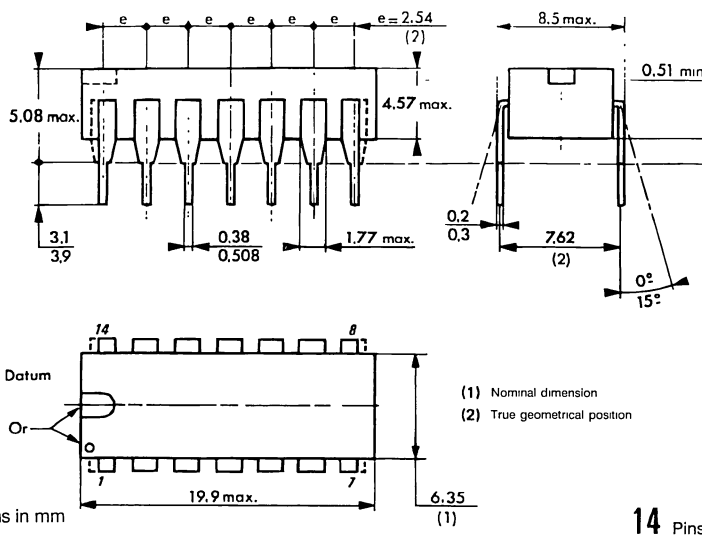
E88TSGF04-07

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



14 PINS - PLASTIC DIP

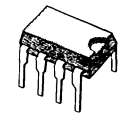


4th TO 8th ORDER ANALOG FILTER

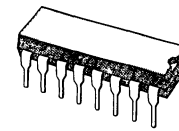
The TSGF08 array provides users with filter integration from 4th to 8th order. 2 package versions are offered to users :

- 8 pin DIL, where only the filter unit is accessible,
- 16 pin DIL, where 2 uncommitted Op-amps are added to previous version.

TSGF08 are also available in SO wide package version (0.3 inch) : 16 pin version only.



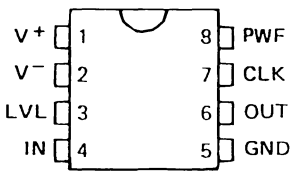
P
DIP-8
(Plastic Package)



P
DIP-16
(Plastic Package)

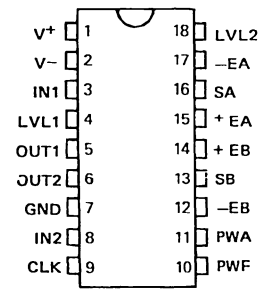
TSGF08
BLOCK DIAGRAM
See figure 4 (E88TSGFSERIES-05)

PIN CONNECTIONS



E88TSGF08-01

8 pins : FILTER ONLY
Compatible with TSGF04

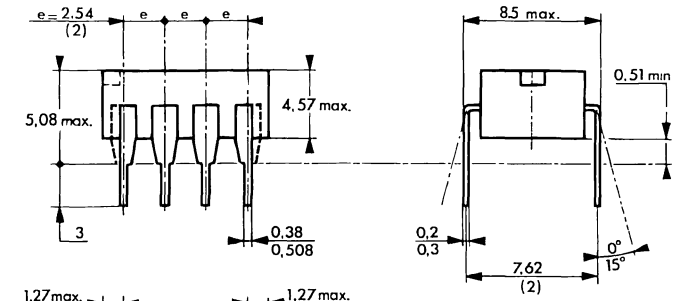


E88TSGF08-02

16 pins : FILTER
: + 2 Op - Amp
Compatible with TSGF12 (with a single filter)

PACKAGE MECHANICAL DATA

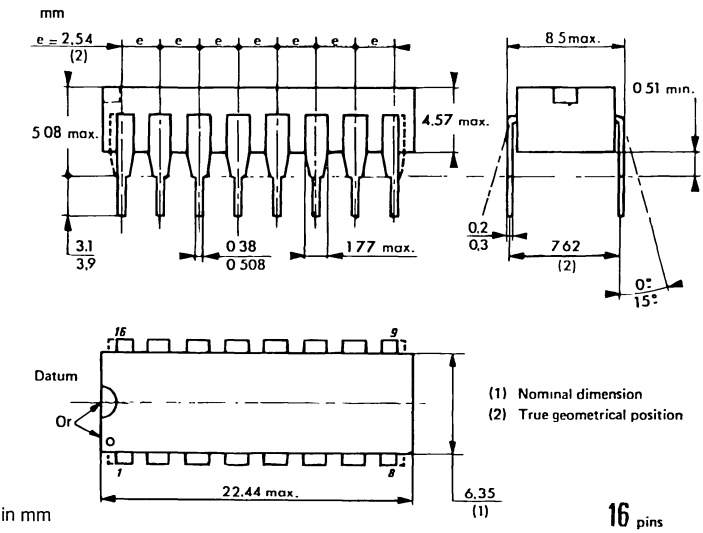
8 PINS - PLASTIC DIP



dimensions in mm

8 Pins

16 PINS - PLASTIC DIP



dimensions in mm

16 pins

8th TO 12th ORDER ANALOG FILTER

TSGF12 array offers the capability to integrate either one single from 8th to 12th order or two different filters whose sum of orders cannot exceed 12.

These 2 different filters can have either same clock or 2 different clock inputs.

The TSGF12 package versions are:

- 16 pin DIL : 1 filter + 2 Op-amps
- 16 pin DIL : 1 filter + 2 Op-amps + 2 driving of output S/H
- 16 pin DIL : 2 filters + 1 Op-amps + 2 clock inputs.
- 18 pin DIL : 2 filters + 2 Op-amps + 1 clock input.
- 20 pin DIL : 2 filters + 2 Op-amps + 2 clock inputs.
- 20 pin DIL : 2 filters + 2 Op-amps + 2 clock inputs + 2 driving of output S/H.

TSGF12 array are also available in SO wide package version (0.3 inch) : 18 and 24 pin versions.

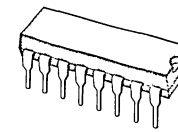
In case of dual filter integration, the CLKSH pin operates only on the output of filter n° 1 (OUTPUT 1). In the same case, for the 16 pin version, only LVL2 pin is available : therefore user can only adjust the Output DC level of filter 2.

Clock divider :

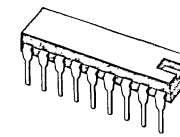
The number of dividers by 2 available on TSGF12 array is 8.

Therefore in case of dual filter on chip integration, there are 2 possibilities to use the clock divider :

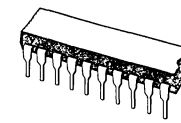
- if one filter does not require internal dividers, the 8 dividers by 2 are available for the second filter ;
- if the first filter requires n internal dividers, there remains only 7-n available for the second filter.



P
DIP-16
(Plastic Package)



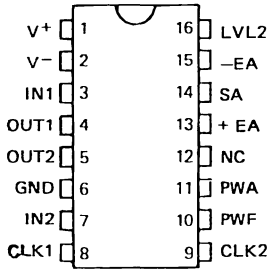
P
DIP-18
(Plastic Package)



P
DIP-20
(Plastic Package)

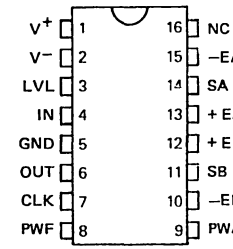
TSGF12
BLOCK DIAGRAM
See figure 4 (E88TSGFSERIES-05)

PIN CONNECTIONS



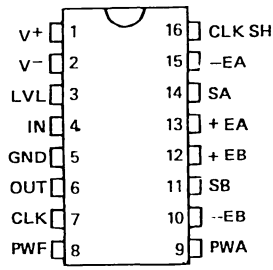
E88TSGF12-01

16 PINS : 2 filters
+ 1 OP - Amp
+ 2 Clock inputs.



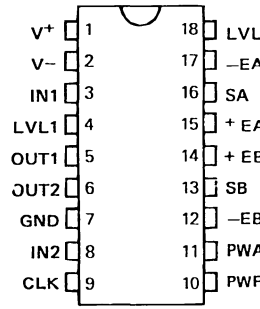
E88TSGF12-02

16 PINS : 1 filter
+ 2 OP - Amp
Compatible with TSGF08



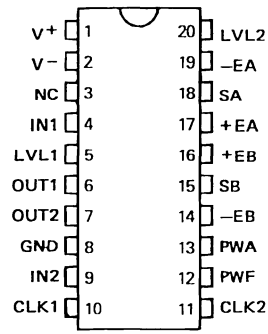
E88TSGF12-03

16 PINS : 1 filters
+ 2 OP - Amps
+ Driving of output S/H.



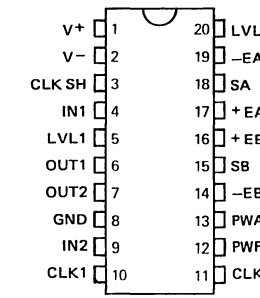
E88TSGF12-04

18 PINS : 2 filters
+ 1 OP - Amp
+ 1 Clock input.



E88TSGF12-04

20 PINS : 2 filters
+ 2 OP - Amps
+ 2 Clock inputs.

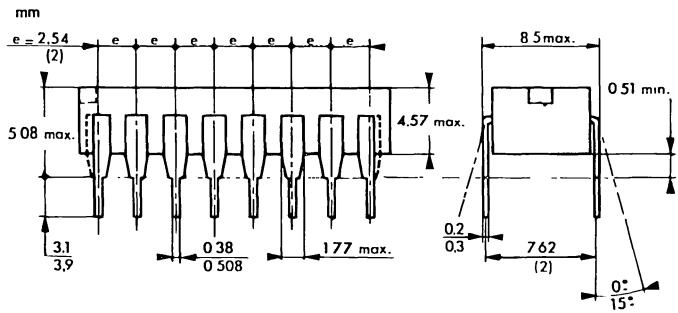


E88TSGF12-04

20 PINS : 2 filters
+ 2 OP - Amps
+ 2 Clock inputs
+ Driving of output S/H.

PACKAGE MECHANICAL DATA

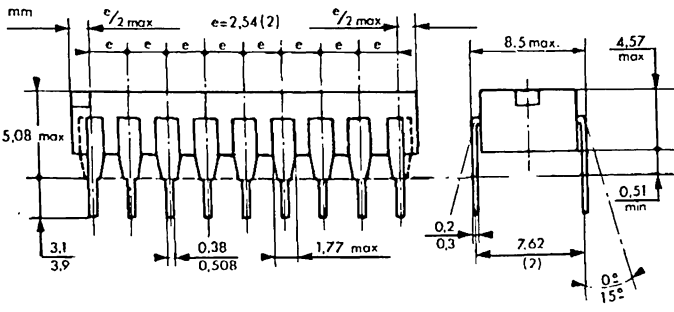
16 PINS - PLASTIC DIP



dimensions in mm

16 pins

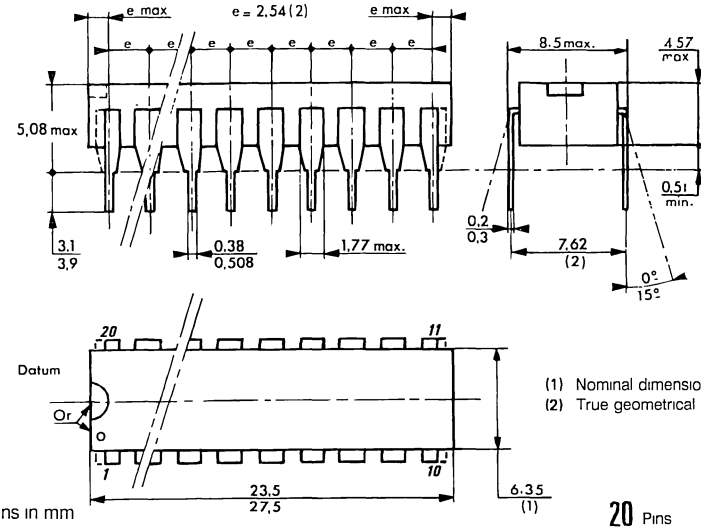
18 PINS - PLASTIC DIP



dimensions in mm

18 pins

20 PINS - PLASTIC DIP

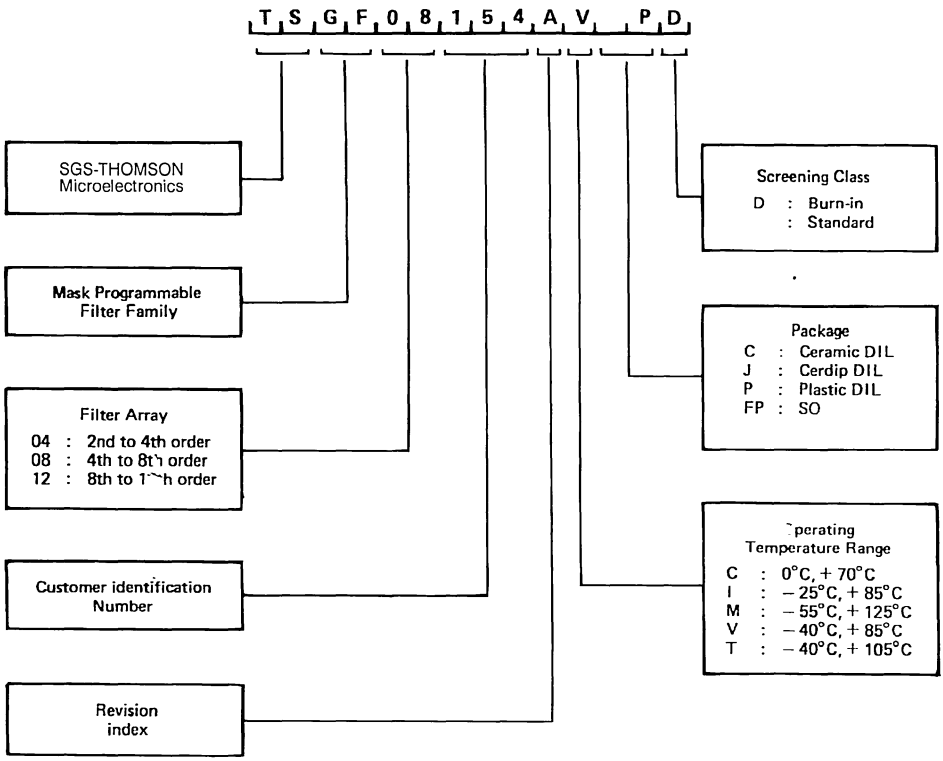


(1) Nominal dimension
(2) True geometrical position

dimensions in mm

20 Pins

ORDER INFORMATION



MASK PROGRAMMABLE FILTERS

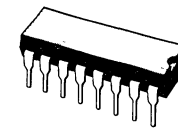
TSG8510

LOWPASS ELLIPTIC SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

FEATURES

- CAUER TYPE
- 5th ORDER
- STOPBAND ATTENUATION : 33dB (typ.)
- PASSBAND RIPPLE : 0.05dB (typ.)
- CLOCK TO CUT-OFF FREQ; RATIO : 75.3
- CLOCK FREQUENCY RANGE : 1 to 1500kHz
- CUT-OFF FREQUENCY RANGE : 13Hz to 20kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



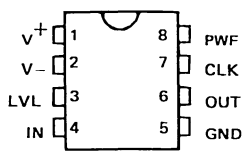
P
DIP-16
(Plastic Package)

P
DIP-8
(Plastic Package)

DESCRIPTION

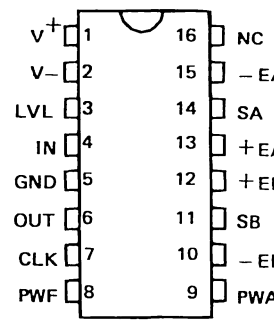
The TSG8510 is a HCMOS lowpass elliptic filter.

PIN CONNECTIONS



8 pins : FILTER ONLY

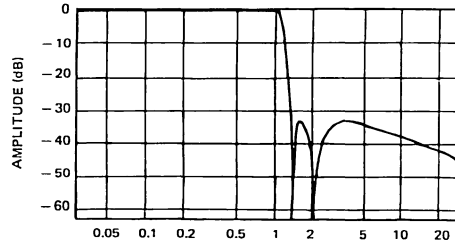
E88TSG8510-01



16 pins : FILTER + 2 OP-AMPs

E88TSG8510-02

AMPLITUDE RESPONSE CURVE



E88TSG8510-04

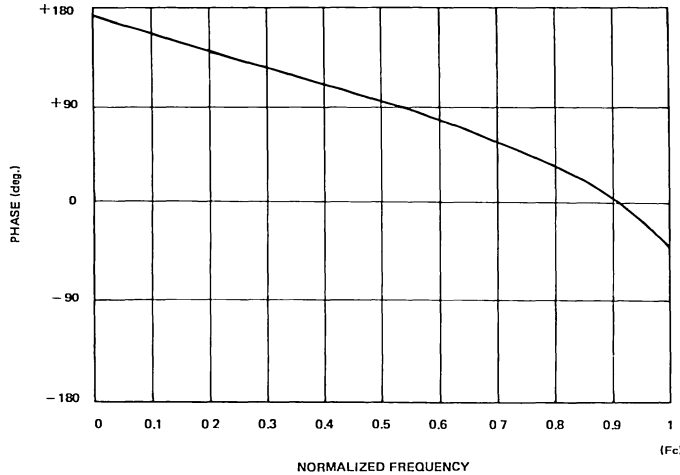
FILTER SPECIFICATIONS

Lowpass Filter : TSG8510 ; Type : Cauer ; Order : 5.
$V^+ = 5V$, $V^- = -5V$, $T = 25°C$, $RL = 5k\Omega$, $CL = 100pF$, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
F_e	External Clock Frequency		1 1500(*)		kHz (min) kHz (max)
F_i	Internal Sampling Frequency		0.5 750(*)		kHz (min) kHz (max)
F_e/F_c	Clock to Cutoff fr. Ratio		75.3 ± 1%		
F_c	Cutoff Frequency		0.013 20(*)		kHz (min) kHz (max)
G_o	Passband Gain		− 0.3 0		dB (min) dB (max)
Ap	Passband Ripple	Fe = 256kHz	0.05	0.4	dB (max)
As	Stopband Attenuation	Fe = 256kHz F > 1.37 Fc	33	32	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 200	mV (max)
LVL	DC Level Adjustment		± 60		mV
LG	Level gain		3.3		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz I_{pwa} = 0µA	3	5	mA (max)
I^-	V^- Supply Current		3	5	mA (max)
$PSRR^+$	V^+ Supply Rjection Ratio	Fe = 256kHz Fin = 1kHz	35		dB
$PSRR^-$	V^- Supply Rejection Ratio		55		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
V_o	Output Voltage Swing		+ 3.5 − 4.5		Vp - p (max)
Vn	Output Noise	BW = 3.4kHz Fe = 256kHz Vin = 2Vrms	89		µVrms
SNR	Signal to Noise Ratio		87		dB

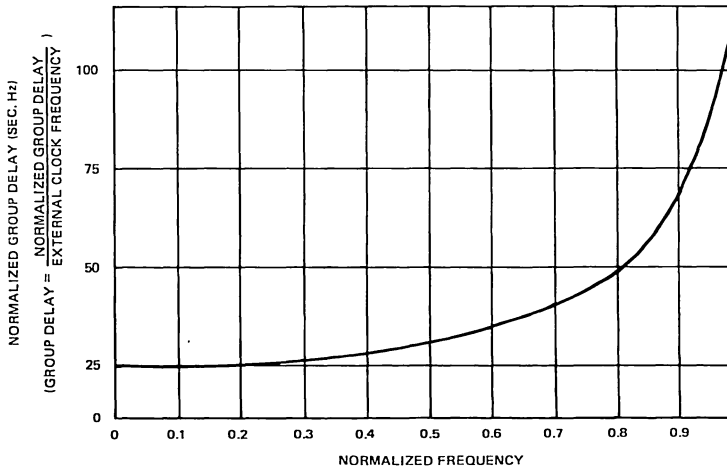
(*) At maximum Fe : - stopband attenuation As > 32dB for F > 1.37Fc
(with I_{pwf} = 250µA) - passband ripple : A_p = 0.8dB
- passband gain : G_o = − 0.4dB

PHASE RESPONSE CURVE (in passband)



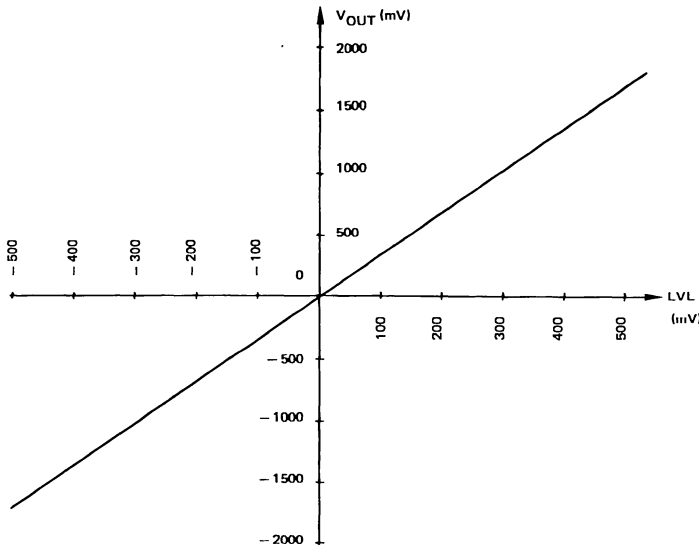
E88TSG8510-05

GROUP DELAY CURVE (in passband)



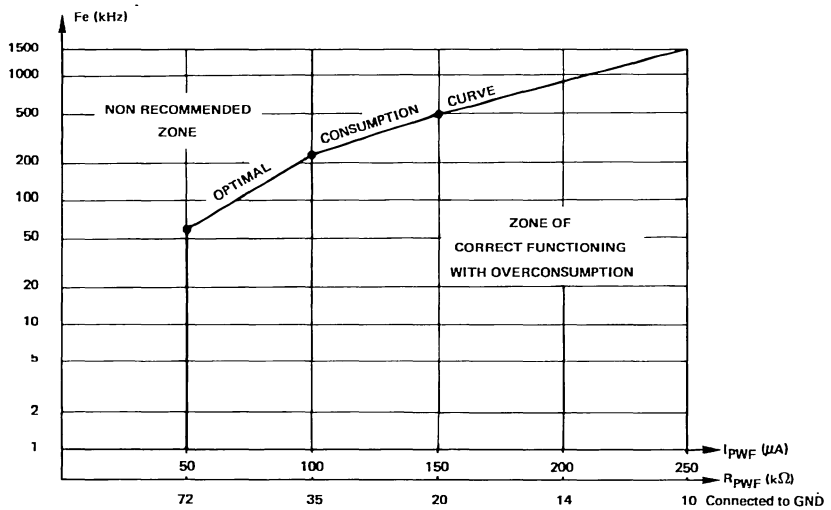
E88TSG8510-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8510-07

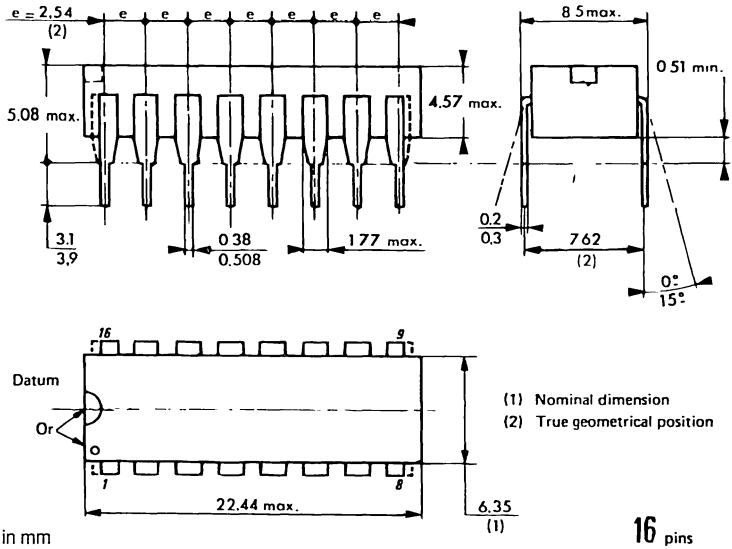
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8510-08

PACKAGE MECHANICAL DATA

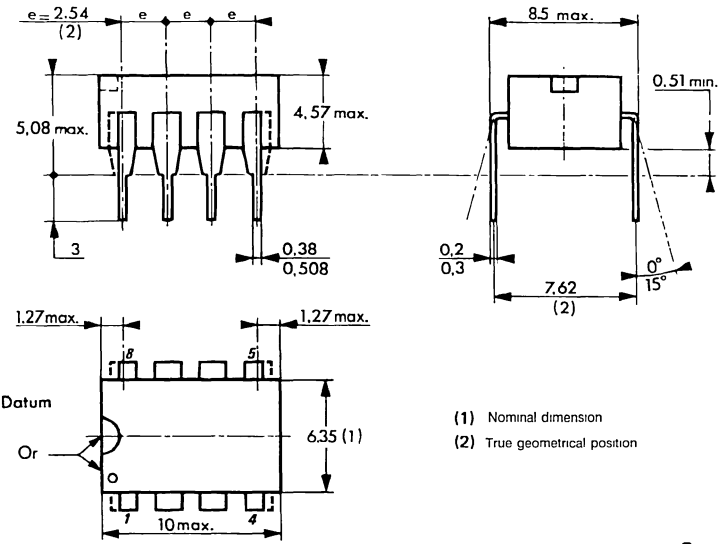
16 PINS - Plastic Dip



dimensions in mm

16 pins

8 PINS - Plastic Dip



dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8510XP
Ceramic	16 Pins Package : TSG8510XC
Cerdip	16 Pins Package : TSG8510XJ
Plastic	8 Pins Package : TSG8510101XP

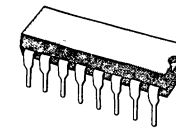
X : Temperature Range = C : 0°C, + 70°C
I : –25°C, + 85°C
V : –40°C, + 85°C
M : –55°C, + 125°C

LOWPASS ELLIPTIC SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

FEATURES

- CAUER TYPE
- 7th ORDER
- STOPBAND ATTENUATION : 55dB (typ)
- PASSBAND RIPPLE : 0.1dB (typ)
- CLOCK TO CUT-OFF FREQ. RATIO : 75.3
- CLOCK FREQUENCY RANGE : 1 to 1300kHz
- CUT-OFF FREQUENCY RANGE : 13Hz to 17.3kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



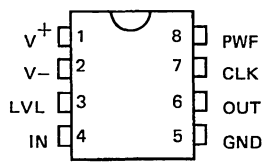
P
DIP-16
(Plastic Package)

P
DIP-8
(Plastic Package)

DESCRIPTION

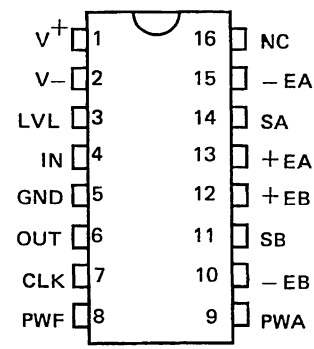
The TSG8511 is a HCMOS lowpass elliptic filter.

PIN CONNECTIONS



8 pins : FILTER ONLY

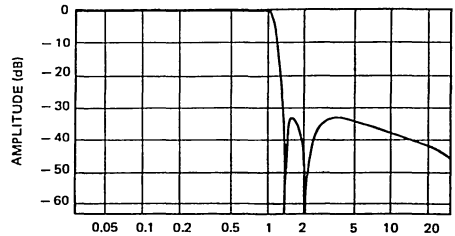
E88TSG8511-01



16 pins : FILTER + 2 OP-AMPs

E88TSG8511-02

AMPLITUDE RESPONSE CURVE



E88TSG8511-04

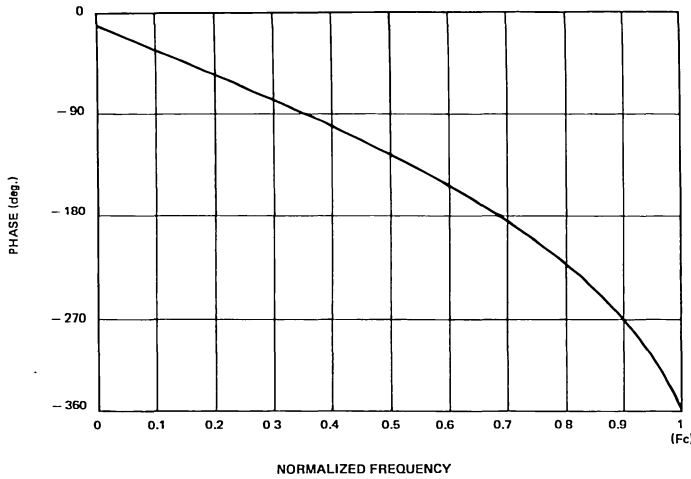
FILTER SPECIFICATIONS

Lowpass Filter : TSG8511 ; Type : Cauer ; Order : 7.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Freq.		1 1300(*)		kHz (min) kHz (max)
Fi	Internal Sampling Freq.		0.5 650(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		75.3 ± 1%		
Fc	Cutoff Frequency		0.013 17.3(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (min) dB (max)
Ap	Passband Ripple	Fe = 256kHz	0.1	0.5	dB (max)
As	Stopband Attenuation	Fe = 256kHz F > 1.3Fc;	55	50	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 150	± 300	mV (max)
LVL	DC Level Adjustment		± 64		mV
LG	Level gain		– 4.7		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	3.5	5	mA (max)
I^-	V^- Supply Current		3.5	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 256kHz Fin = 1kHz	32		dB
$PSRR^-$	V^- Supply Rejection Ratio		47		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 3.4kHz Fe = 256kHz Vin = 2Vrms	158		µVrms
SNR	Signal to Noise Ratio		82		dB

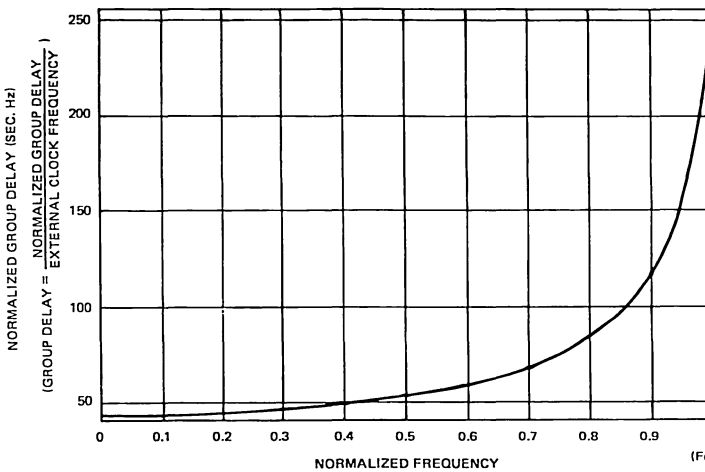
(*) At maximum Fe (with $I_{pwf} = 250\mu A$)
- stopband attenuation As > 50dB for F > 1.3Fc
- passband ripple : $A_p = 0.5dB$
- passband gain : $G_0 = -0.7dB$

PHASE RESPONSE CURVE (in passband)



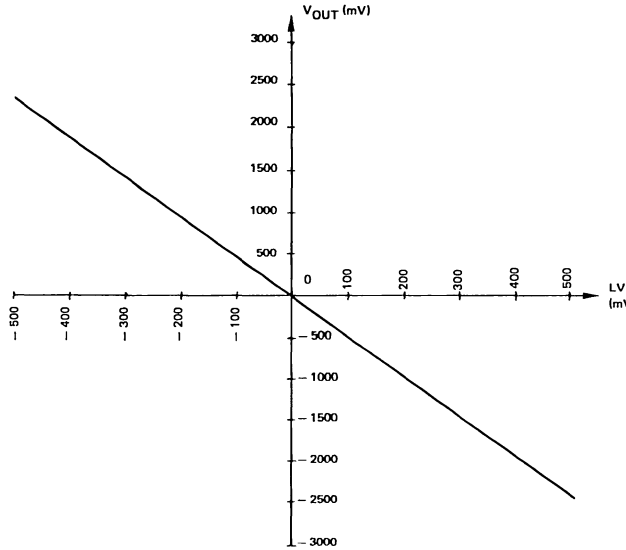
E88TSG8511-05

GROUP DELAY CURVE (in passband)



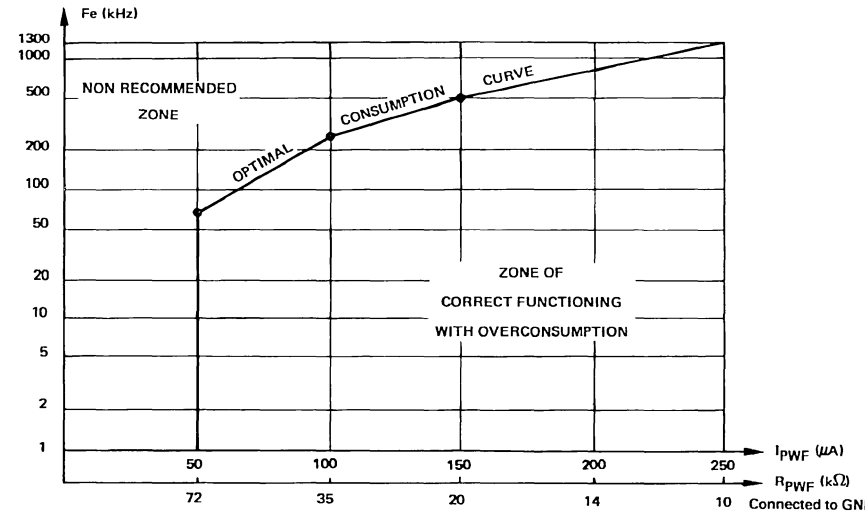
E88TSG8511-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8511-07

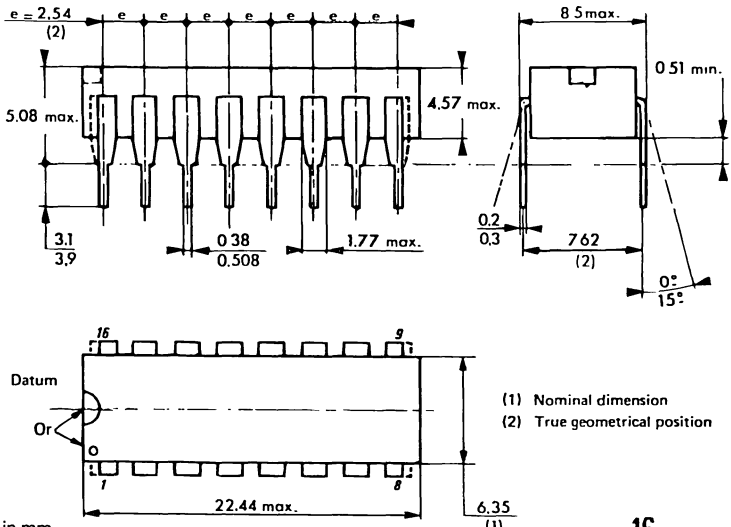
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8511-08

PACKAGE MECHANICAL DATA

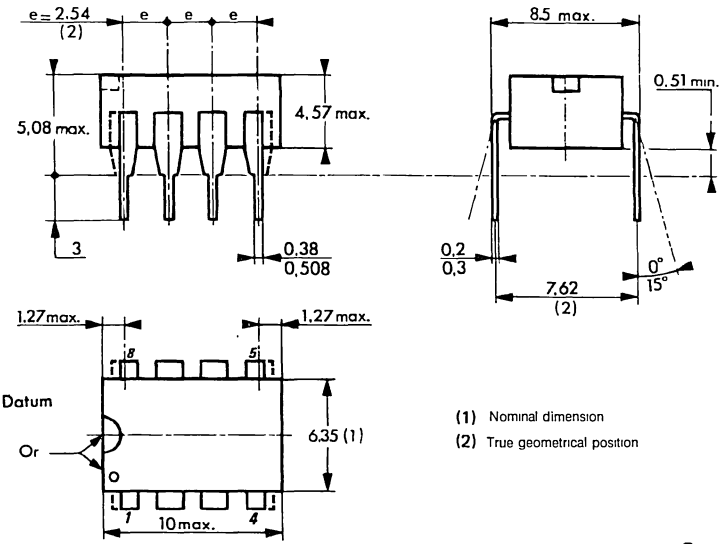
16 PINS - Plastic Dip



dimensions in mm

16 pins

8 PINS - Plastic Dip



dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8511XP
Ceramic	16 Pins Package : TSG8511XC
Cerdip	16 Pins Package : TSG8511XJ
Plastic	8 Pins Package : TSG85111XP

X : Temperature Range = C : 0°C, + 70°C
I : –25°C, + 85°C
V : –40°C, + 85°C
M : –55°C, + 125°C

SGS-THOMSON MICROELECTRONICS

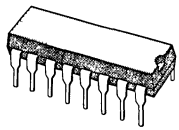
TSG8512

LOWPASS ELLIPTIC SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

FEATURES

- CAUER TYPE
- 7th ORDER
- STOPBAND ATTENUATION : 85dB (typ)
- PASSBAND RIPPLE : 0.15dB (typ)
- CLOCK TO CUT-OFF FREQ. RATIO : 100
- CLOCK FREQUENCY RANGE : 1 to 2000kHz
- CUT-OFF FREQUENCY RANGE : 10Hz to 20kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



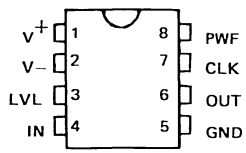
P
DIP-16
(Plastic Package)

P
DIP-8
(Plastic Package)

DESCRIPTION

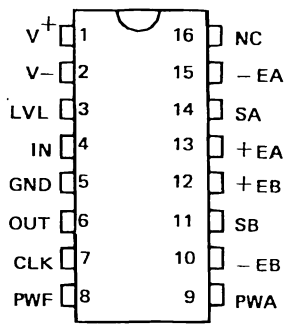
The TSG8512 is a HCMOS lowpass elliptic filter.

PIN CONNECTIONS



8 pins : FILTER ONLY

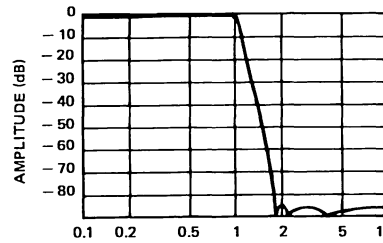
E88TSG8512-01



16 pins : FILTER + 2 OP-AMPs

E88TSG8512-02

AMPLITUDE RESPONSE CURVE



E88TSG8512-04

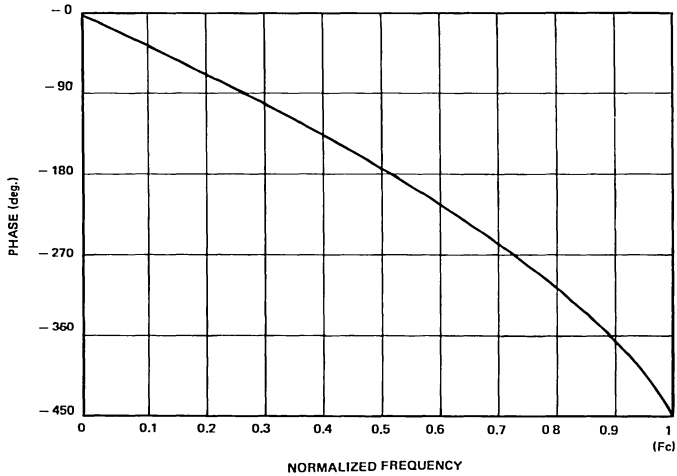
FILTER SPECIFICATIONS

Lowpass Filter : TSG8512 ; Type : Cauer ; Order : 7.
V+ = 5V, V- = –5V, T = 25°C, RL = 5kΩ, CL = 100pF, IPWF = 100µA

Symbol	Parameter		Typ.	Tested Limits	Unit
F_e	External Clock Frequency		1 2000(*)		kHz (min) kHz (max)
F_i	Internal Sampling Frequency		0.5 1000(*)		kHz (min) kHz (max)
F_e/F_c	Clock to Cutoff Frequency Ratio		100 ± 1%		
F_c	Cutoff Frequency		0.010 20(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (min) dB (max)
A_p	Passband Ripple	F_e = 100kHz	0.15	0.5	dB (max)
A_s	Stopband Attenuation	F_e = 100kHz F > 1.8F_c	85	75	dB (min)
V_{off}	Output DC Offset Voltage	LVL = 0V	± 150	300	mV (max)
LVL	DC Level Adjustment		± 22.5		mV
LG	Level gain		– 11.1		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	F_e=100kHz I_{pwa}=0µA	3.5	5	mA (max)
I^-	V^- Supply Current		3.5	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ration	F_e=200kHz F_{in}=1kHz	20		dB
$PSRR^-$	V^- Supply Rejection Ratio		35		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
V_o	Output Voltage Swing		+ 3.5 – 4.5		V_{p-p} (max)
V_n	Output Noise	BW=1kHz F_e=100kHz V_{in}=2V_{rms}	112		μV_{rms}
SNR	Signal to Noise Ratio		85		dB

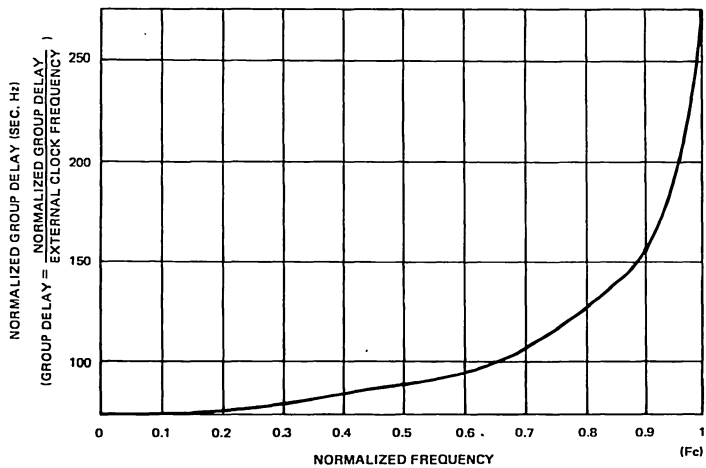
(*) At maximum Fe : - stopband attenuation As > 62dB for F > 1.8Fc
(with I_{pwf} = 250µA) - passband ripple : A_p = 0.6dB
- passband gain : G_0 = – 0.4dB

PHASE RESPONSE CURVE (in passband)



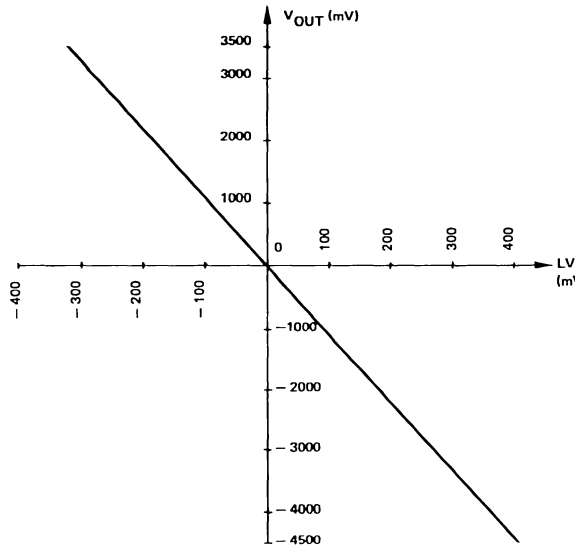
E88TSG8512-05

GROUP DELAY CURVE (in passband)



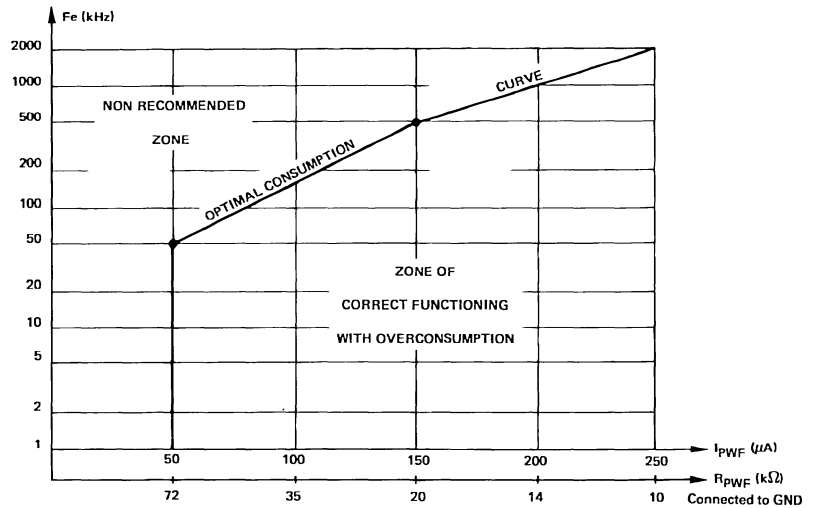
E88TSG8512-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8512-07

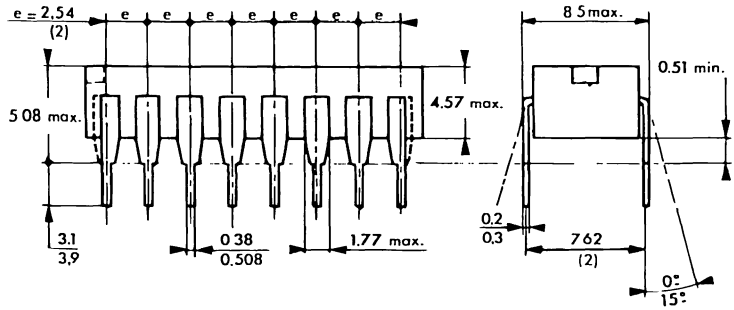
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE

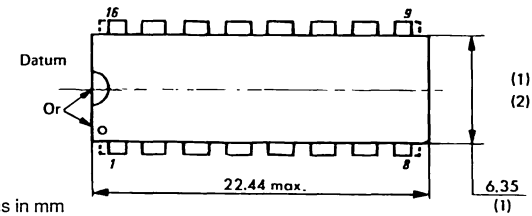


E88TSG8512-08

PACKAGE MECHANICAL DATA

16 PINS - Plastic Dip



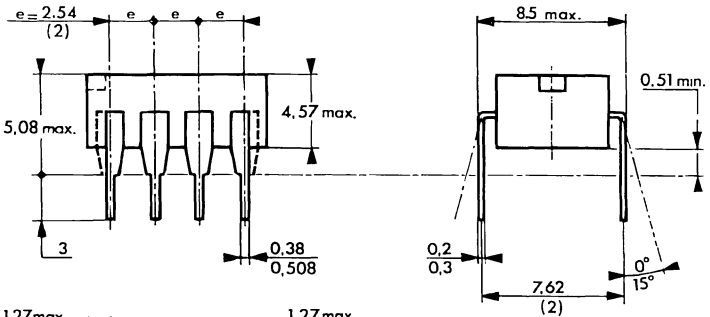


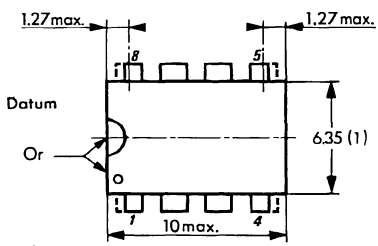
(1) Nominal dimension
(2) True geometrical position

dimensions in mm

16 pins

8 PINS - Plastic Dip





(1) Nominal dimension
(2) True geometrical position

dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8512XP
Ceramic	16 Pins Package : TSG8512XC
Cerdip	16 Pins Package : TSG8512XJ
Plastic	8 Pins Package : TSG85121XP

X : Temperature Range = C : 0°C, + 70°C
I : –25°C, + 85°C
V : –40°C, + 85°C
M : –55°C, + 125°C

SGS-THOMSON MICROELECTRONICS

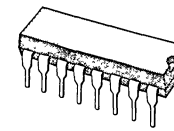
TSG8513

LOWPASS POLINOMIAL SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

FEATURES

- CHEBYCHEV TYPE
- 8th ORDER
- STOPBAND ATTENUATION : 69dB (typ) AT 2 x F_C
- PASSBAND RIPPLE : 0.15dB (typ)
- CLOCK TO CUT-OFF FREQ; RATIO : 60
- CLOCK FREQUENCY RANGE : 1 to 1500kHz
- CUT-OFF FREQUENCY RANGE : 16Hz to 25kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



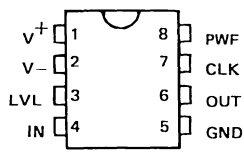
P
DIP-16
(Plastic Package)

P
DIP-8
(Plastic Package)

DESCRIPTION

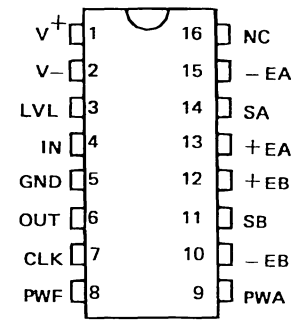
The TSG8513 is a HCMOS lowpass polynomial filter.

PIN CONNECTIONS



8 pins : FILTER ONLY

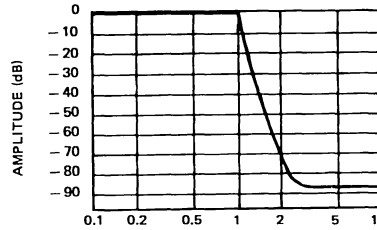
E88TSG8513-01



16 pins : FILTER + 2 OP-AMPs

E88TSG8513-02

AMPLITUDE RESPONSE CURVE



E88TSG8513-04

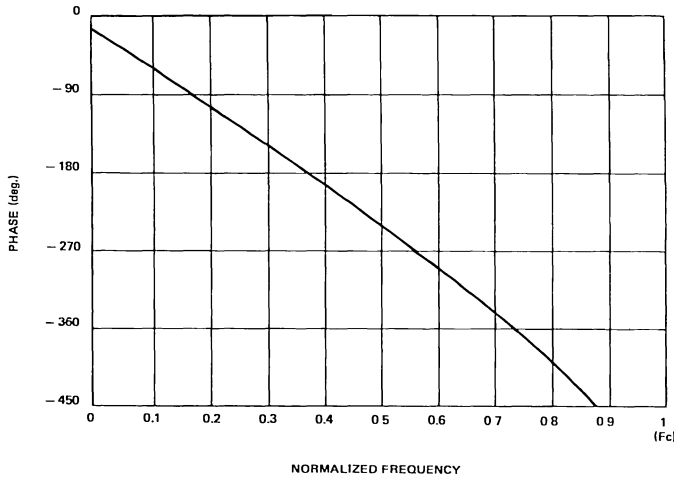
FILTER SPECIFICATIONS

Lowpass Filter : TSG8513 ; Type : Chebychev ; Order : 8.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		1 1500(*)		kHz (min) kHz (max)
Fi	Internal Sampling Freq.		0.5 750(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		60 ± 1%		
Fc	Cutoff Frequency		0.016 25(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (min) dB (max)
Ap	Passband Ripple	Fe = 60kHz	0.15	0.5	dB (max)
As	Stopband Attenuation	Fe = 60kHz F > 2Fc	69	65	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 250	mV (max)
LVL	DC Level Adjustment		± 100		mV (max)
LG	Level gain		– 2.5		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	3.8	5	mA (max)
I^-	V^- Supply Current		3.8	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 120kHz Fin = 1kHz	25		dB
$PSRR^-$	V^- Supply Rejection Ratio		40		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 1kHz Fe = 60kHz Vin = 2Vrms	107		µVrms
SNR	Signal to Noise Ratio		85		dB

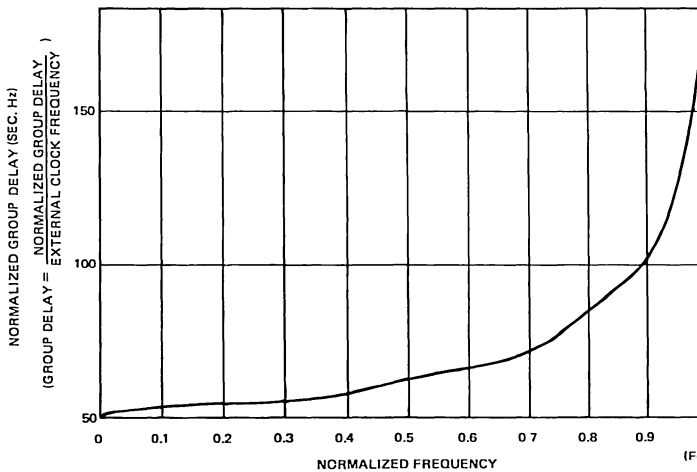
(*) At maximum Fe : - stopband attenuation As > 55dB for f > 2Fc
(with $I_{pwf} = 250\mu A$) - passband ripple : $A_p = 0.8dB$
- passband gain : $G_0 = -0.6dB$

PHASE RESPONSE CURVE (in passband)



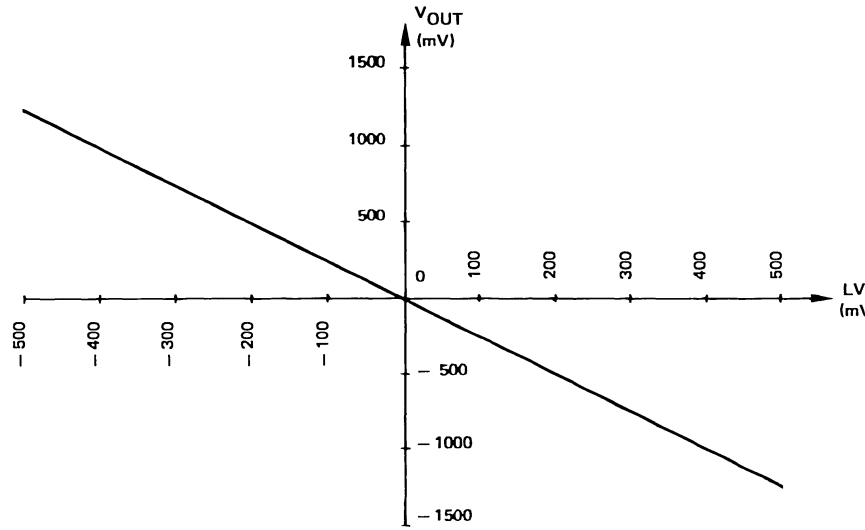
E88TSG8513-05

GROUP DELAY CURVE (in passband)



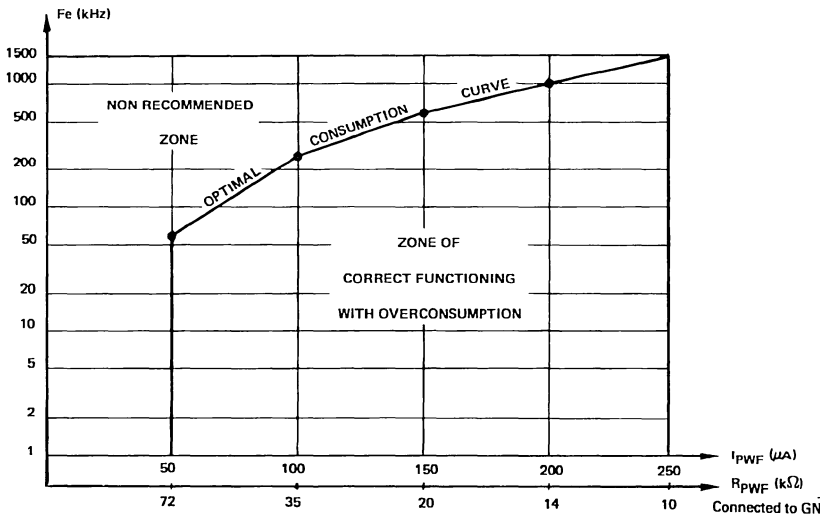
E88TSG8513-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8513-07

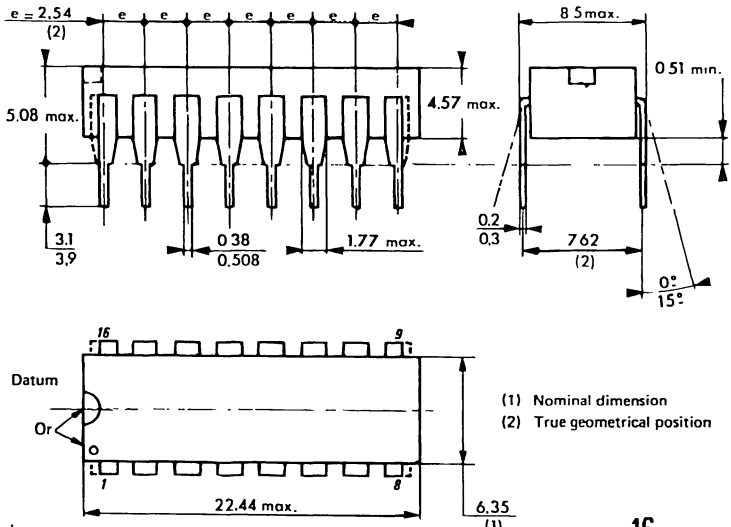
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8513-08

PACKAGE MECHANICAL DATA

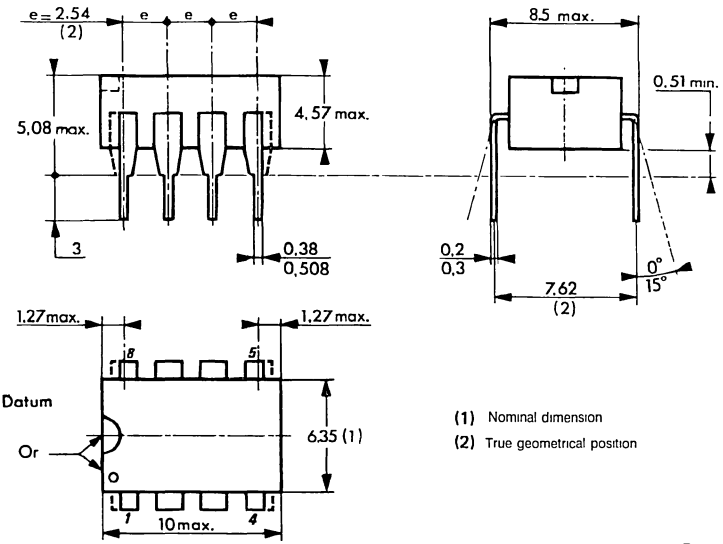
16 PINS - Plastic Dip



dimensions in mm

16 pins

8 PINS - Plastic Dip



dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8513XP
Ceramic	16 Pins Package : TSG8513XC
Cerdip	16 Pins Package : TSG8513XJ
Plastic	8 Pins Package : TSG85131XP

X : Temperature Range = C : 0°C, + 70°C
I : –25°C, + 85°C
V : –40°C, + 85°C
M : –55°C, + 125°C

SGS-THOMSON MICROELECTRONICS

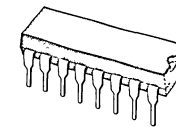
TSG8514

LOWPASS POLYNOMIAL SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

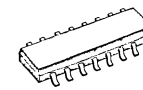
FEATURES

- BUTTERWORTH TYPE
- 8th ORDER
- STOPBAND ATTENUATION : 74dB (typ) AT 3.6 x F_c
- PASSBAND RIPPLE : MAXIMALLY FLAT
- CLOCK TO CUT-OFF FREQ. RATIO : 80
- CLOCK FREQUENCY RANGE : 1 to 1000kHz
- CUT-OFF FREQUENCY RANGE : 12.5Hz to 12.5kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



P
DIP-16
(Plastic Package)



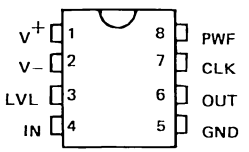
FP
SO-16
(Plastic Micropackage)

P
DIP-8
(Plastic Package)

DESCRIPTION

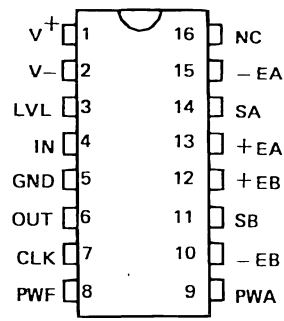
The TSG8514 is a HCMOS lowpass polynomial filter.

PIN CONNECTIONS



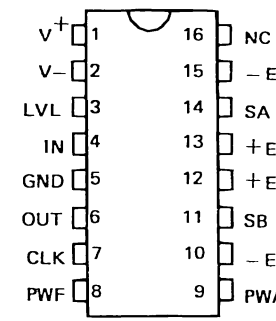
8 pins : FILTER ONLY

E88TSG8514-01



16 pins : FILTER + 2 OP-AMPs

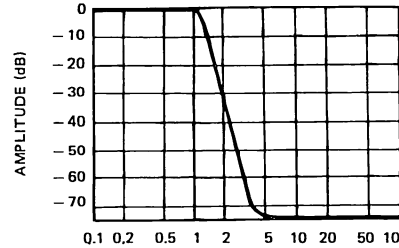
E88TSG8514-02



SO-16 Package

E88TSG8514-03

AMPLITUDE RESPONSE CURVE



E88TSG8514-04

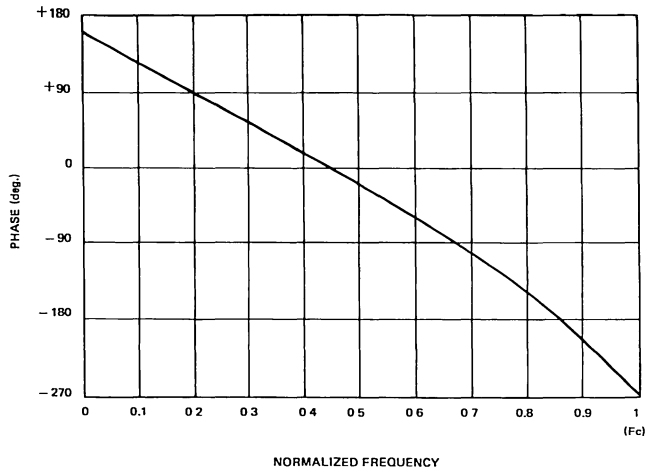
FILTER SPECIFICATIONS

Lowpass Filter : TSG8514 ; Type : Butterworth ; Order : 8.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		1 1000(*)		kHz (min) kHz (max)
Fi	Internal Sampling Freq.		0.5 500(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		80 ± 1%		
Fc	Cutoff Frequency		0.0125 12.5(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (min) dB (max)
Ap	Passband Ripple	Fe = 80kHz	maxi mally Flat		dB (max)
As	Stopband Attenuation	Fe = 80kHz F > 3.6 Fc	74	68	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 200	mV (max)
LVL	DC Level Adjustment		± 100		mV
LG	Level gain		– 2		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz I_{pwa} = 0µA	3.8	5	mA (max)
I^-	V^- Supply Current		3.8	5	mA (max)
$PSRR^+$	V^+ Supply Rjection Ratio	Fe = 160kHz Fin = 1kHz	30		dB
$PSRR^-$	V^- Supply Rejection Ratio		42		dB
R_{IN}	Input Resistance		3		. MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 3.4kHz Fe = 256kHz Vin = 2Vrms	86		µVrms
SNR	Signal to Noise Ratio		87		dB

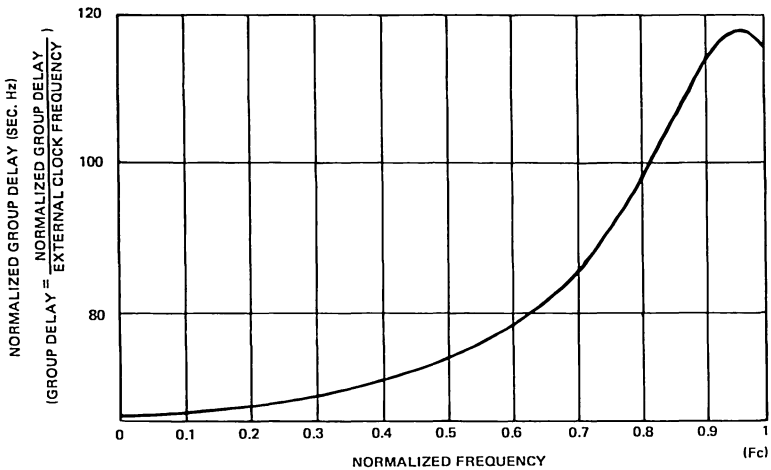
(*) At maximum Fe : - stopband attenuation As > 50dB for F > 3.6Fc
(with $I_{pwf} = 250\mu A$) - passband gain : $G_o = -0.5dB$

PHASE RESPONSE CURVE (in passband)



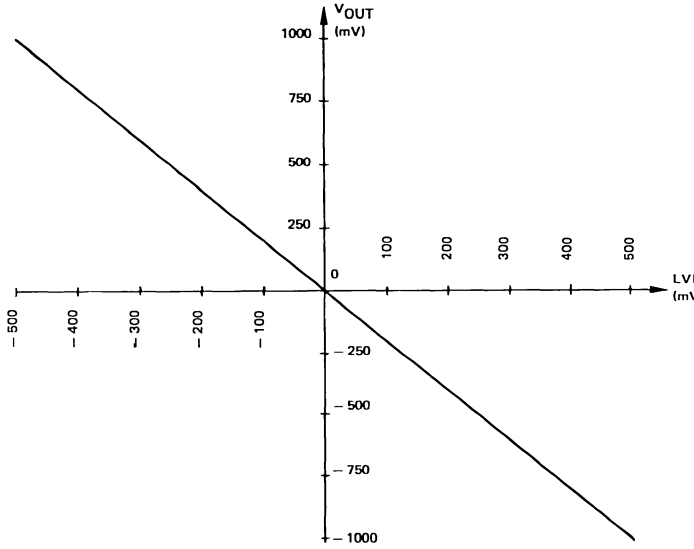
E88TSG8514-05

GROUP DELAY CURVE (in passband)



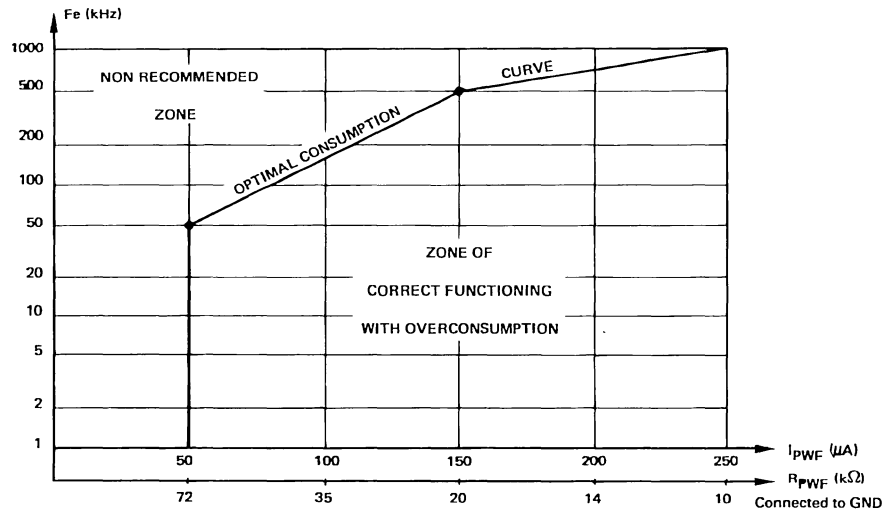
E88TSG8514-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8514-07

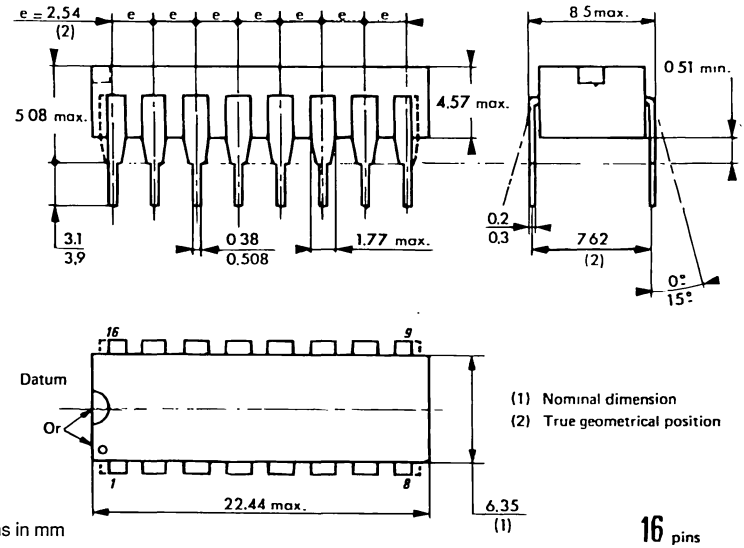
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8514-08

PACKAGE MECHANICAL DATA

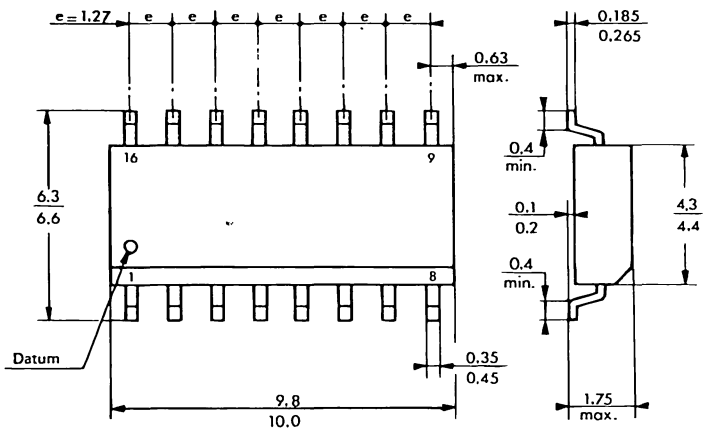
16 PINS - Plastic Dip



dimensions in mm

16 pins

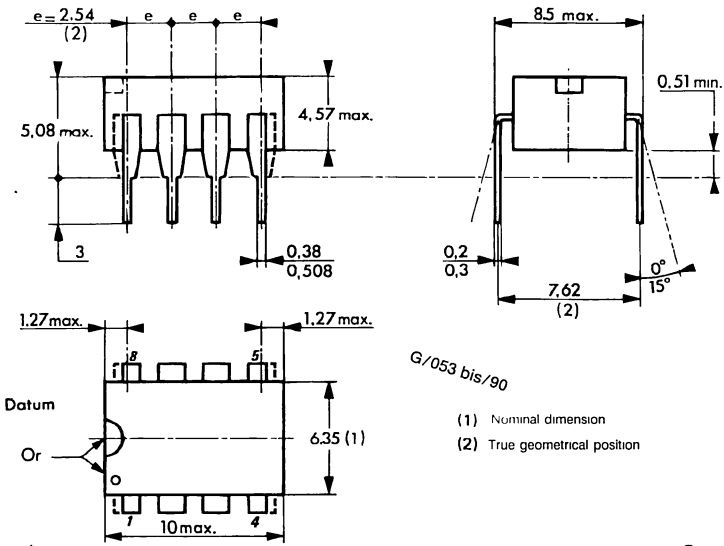
16 PINS - Plastic Micropackage



dimensions in mm

16 pins

8 PINS - Plastic Dip



dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8514XP
Ceramic	16 Pins Package : TSG8514XC
Cerdip	16 Pins Package : TSG8514XJ
Plastic	8 Pins Package : TSG85141XP

X : Temperature Range = C : 0°C, + 70°C
I : −25°C, + 85°C
V : −40°C, + 85°C
M : −55°C, + 125°C

SGS-THOMSON MICROELECTRONICS

TSG8530

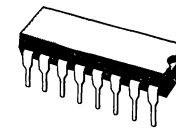
HIGHPASS ELLIPTIC SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

FEATURES

- CAUER TYPE
- 3th ORDER
- STOPBAND ATTENUATION : 15dB (typ)
- PASSBAND RIPPLE : 0.2dB (typ)
- CLOCK TO CUT-OFF FREQ. RATIO : 320
- CLOCK FREQUENCY RANGE : 4 to 2400kHz
- CUT-OFF FREQUENCY RANGE : 12Hz to 7.5kHz

* According to spectrum aliasing phenomenon, the TSG8530 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



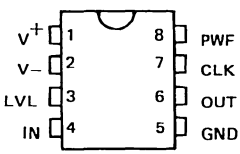
P
DIP-16
(Plastic Package)

P
DIP-8
(Plastic Package)

DESCRIPTION

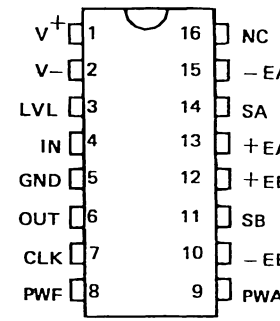
The TSG8530 is a HCMOS highpass* elliptic filter.

PIN CONNECTIONS



8 pins : FILTER ONLY

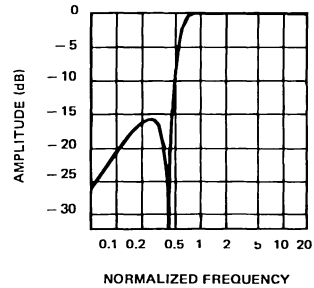
E88TSG8530-01



16 pins : FILTER + 2 OP-AMPs

E88TSG8530-02

AMPLITUDE RESPONSE CURVE



E88TSG8530-04

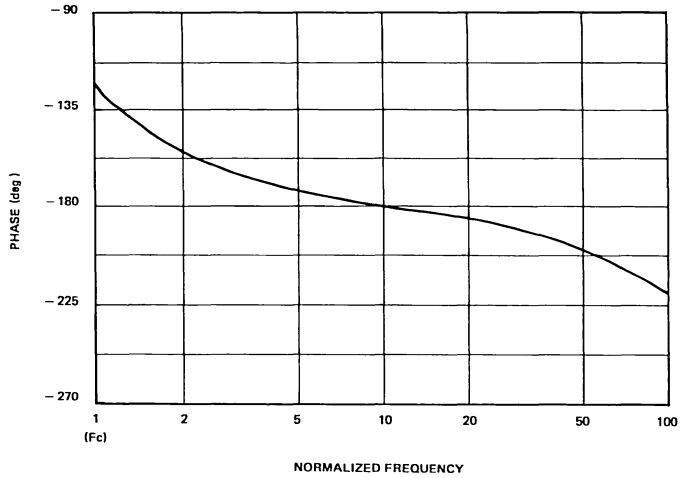
FILTER SPECIFICATIONS

Highpass Filter : TSG8530 ; Type : Cauer ; Order : 3.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		4 2400(*)		kHz (min) kHz (max)
Fi	Internal Sampling Frequency		2 1200(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		320 ± 1%		
Fc	Cutoff Frequency		0.0125 7.5(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.3 0		dB (min) dB (max)
Ap	Passband Ripple	[Fc, 30Fc] Fe = 320kHz	0.2	0.5	dB (max)
As	Stopband Attenuation	F < 0.49Fc Fe = 320kHz	15	14	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 200	mV (max)
LVL	DC Level Adjustment		± 40		mV
LG	Level gain		– 6		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	2.8	5	mA (max)
I^-	V^- Supply Current		2.8	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 32kHz Fin = 1kHz	33		dB
$PSRR^-$	V^- Supply Rejection Ratio		38		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 2kHz Fe = 32kHz Vin = 2Vrms	80		µVrms
SNR	Signal to Noise Ratio		85		dB

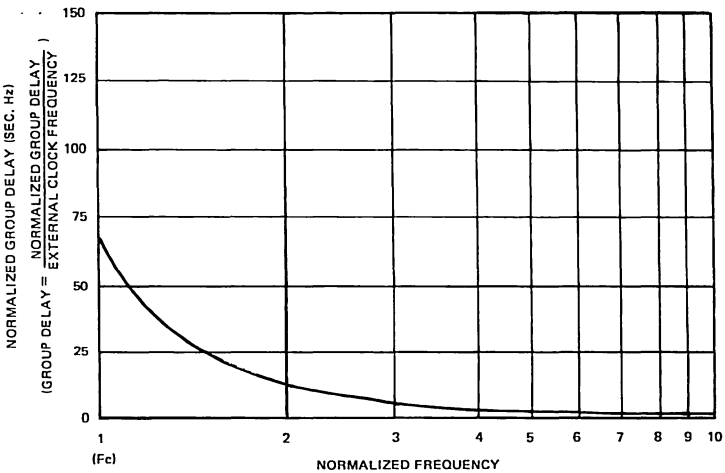
(*) At maximum Fe : - stopband attenuation As > 14dB for F < 0.49Fc
(with $I_{pwf} = 250\mu A$) - passband ripple : $A_p = 0.2dB$
- passband gain : $G_0 = -0.6dB$

PHASE RESPONSE CURVE (in passband)



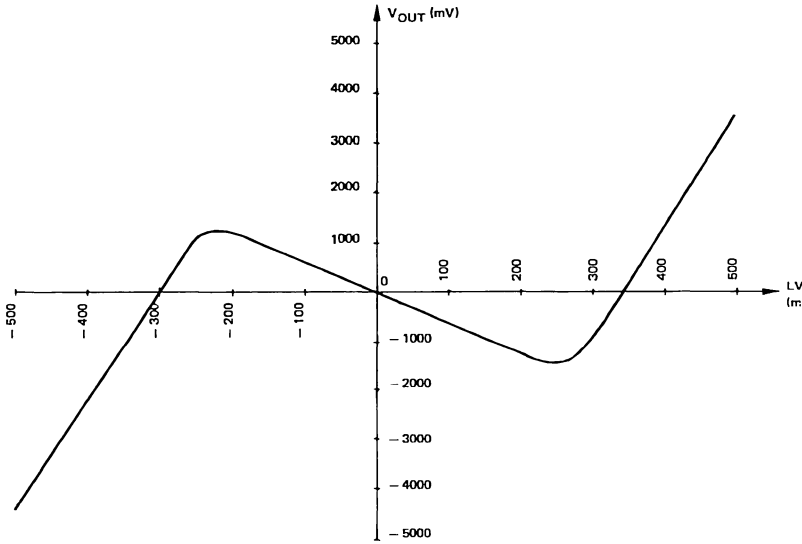
E88TSG8530-05

GROUP DELAY CURVE (in passband)



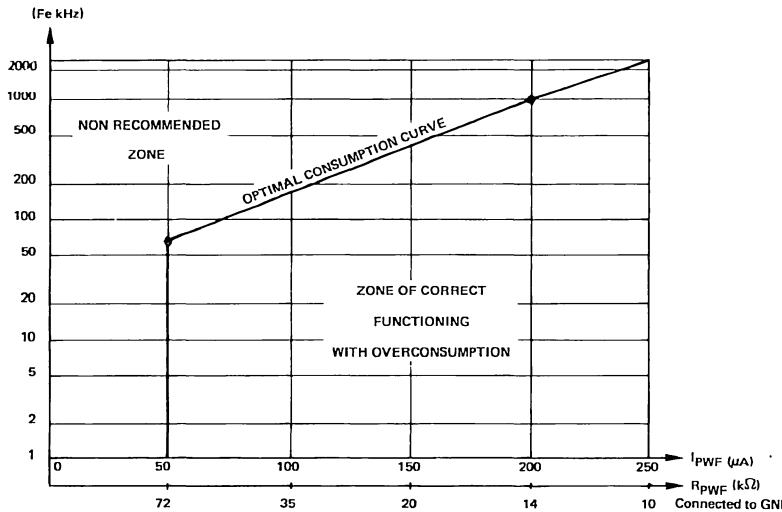
E88TSG8530-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8530-07

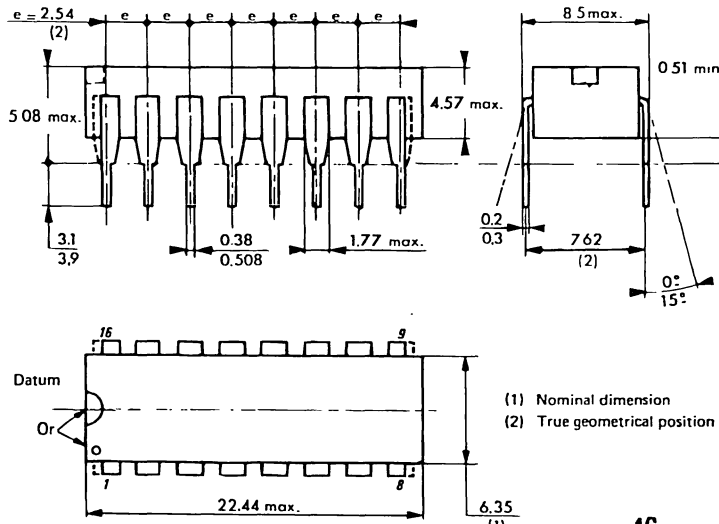
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8530-08

PACKAGE MECHANICAL DATA

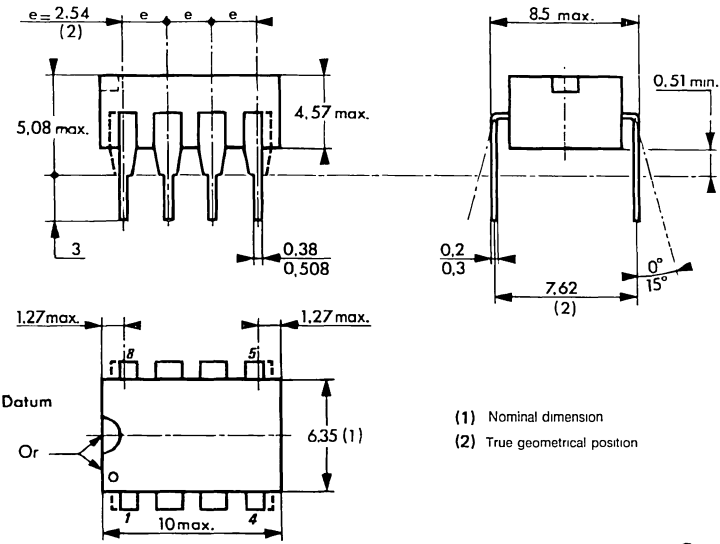
16 PINS - Plastic Dip



dimensions in mm

16 pins

8 PINS - Plastic Dip



dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8530XP
Ceramic	16 Pins Package : TSG8530XC
Cerdip	16 Pins Package : TSG8530XJ
Plastic	8 Pins Package : TSG85301XP

X : Temperature Range = C : 0°C, + 70°C
I : –25°C, + 85°C
V : –40°C, + 85°C
M : –55°C, + 125°C

SGS-THOMSON MICROELECTRONICS

TSG8531

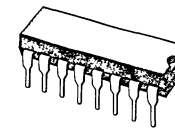
HIGHPASS ELLIPTIC SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

FEATURES

- CAUER TYPE
- 6th ORDER
- STOPBAND ATTENUATION : 32dB (typ)
- PASSBAND RIPPLE : 0.15dB (typ)
- CLOCK TO CUT-OFF FREQ. RATIO : 400
- CLOCK FREQUENCY RANGE : 4 to 1800kHz
- CUT-OFF FREQUENCY RANGE : 10Hz to 4.5kHz

* According to spectrum aliasing phenomenon, the TSG8531 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



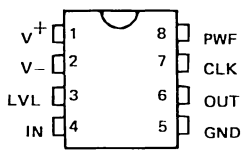
P
DIP-16
(Plastic Package)

P
DIP-8
(Plastic Package)

DESCRIPTION

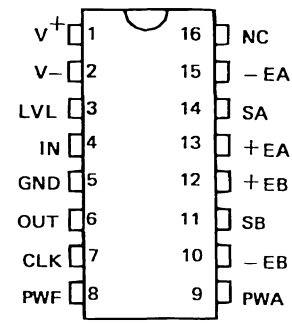
The TSG8531 is a HCMOS highpass* elliptic filter.

PIN CONNECTIONS



8 pins : FILTER ONLY

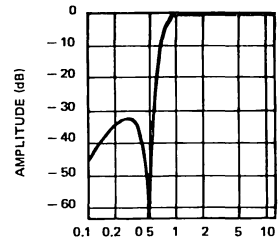
E88TSG8531-01



16 pins : FILTER + 2 OP-AMPs

E88TSG8531-02

AMPLITUDE RESPONSE CURVE



E88TSG8531-04

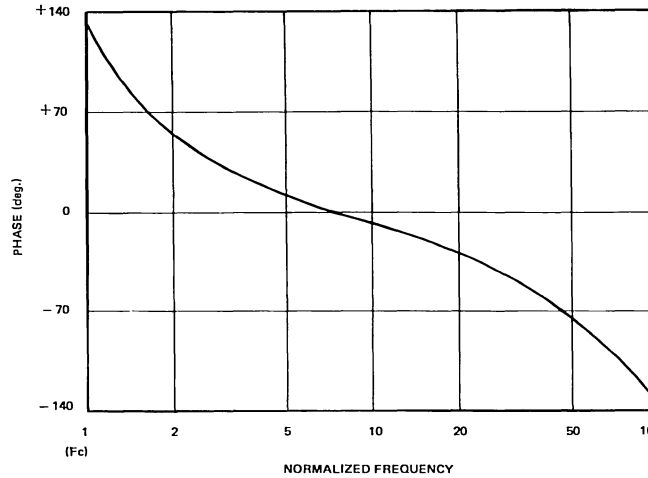
FILTER SPECIFICATIONS

Highpass Filter : TSG8531 ; Type : Cauer ; Order : 6.
$V^+ = 5V$, $V^- = -5V$, T = 25°C, RL = 5kΩ, CL = 100pF, $I_{PWF} = 100\mu A$

Symbol	Parameter		Typ.	Tested Limits	Unit
Fe	External Clock Frequency		4 1800(*)		kHz (min) kHz (max)
Fi	Internal Sampling Freq.		2 900(*)		kHz (min) kHz (max)
Fe/Fc	Clock to Cutoff fr. Ratio		400 ± 1%		
Fc	Cutoff Frequency		0.01 4.5(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.1 0.1		dB (min) dB (max)
Ap	Passband Ripple	[Fc, 30Fc] Fe = 400kHz	0.15	0.4	dB (max)
As	Stopband Attenuation	F < 0.55Fc Fe = 400kHz	32	30	dB (min)
Voff	Output DC Offset Voltage	LVL = 0V	± 100	± 200	mV (max)
LVL	DC Level Adjustment		± 300		mV
LG	Level gain		0.1		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	Fe = 100kHz Ipwa = 0µA	3.5	5	mA (max)
I^-	V^- Supply Current		3.5	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 40kHz Fin = 1kHz	36		dB
$PSRR^-$	V^- Supply Rejection Ratio		48		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 – 4.5		Vp-p (max)
Vn	Output Noise	BW = 2kHz Fe = 40kHz Vin = 2Vrms	178		µVrms
SNR	Signal to Noise Ratio		80		dB

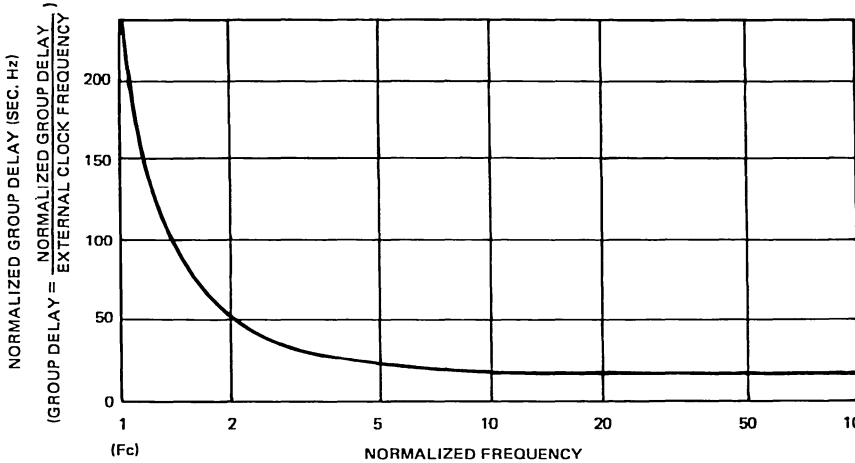
(*) At maximum Fe : - stopband attenuation As > 30dB for F > 0.55Fc
(with $I_{pwf} = 250\mu A$) - passband ripple : $A_p = 0.3dB$
- passband gain : $G_0 = -1dB$

PHASE RESPONSE CURVE (in passband)



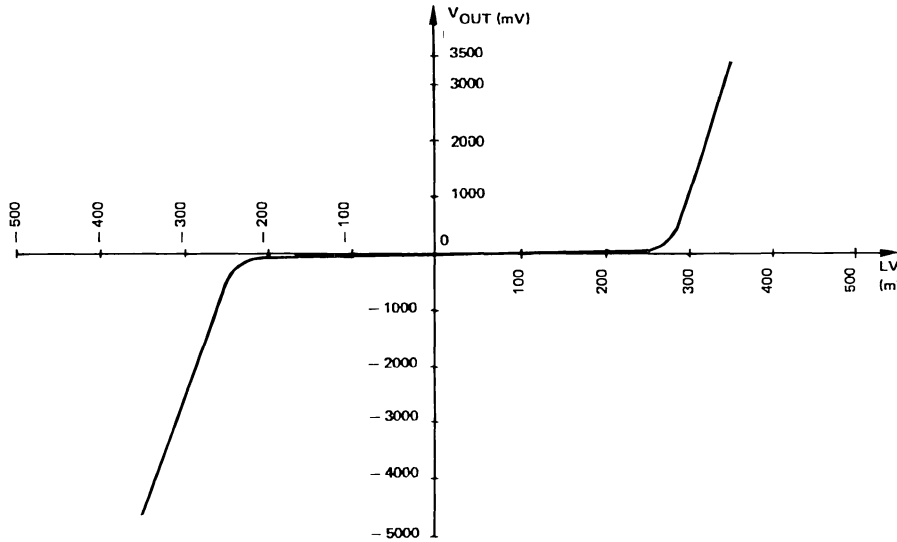
E88TSG8531-05

GROUP DELAY CURVE (in passband)



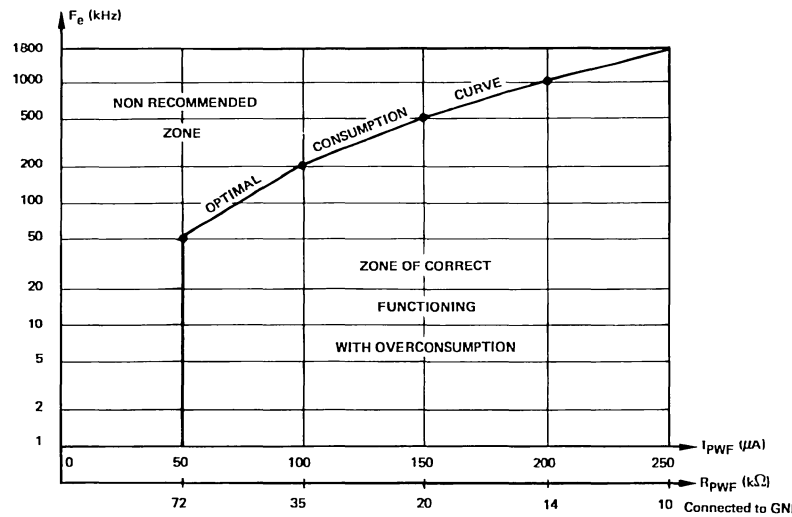
E88TSG8531-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8531-07

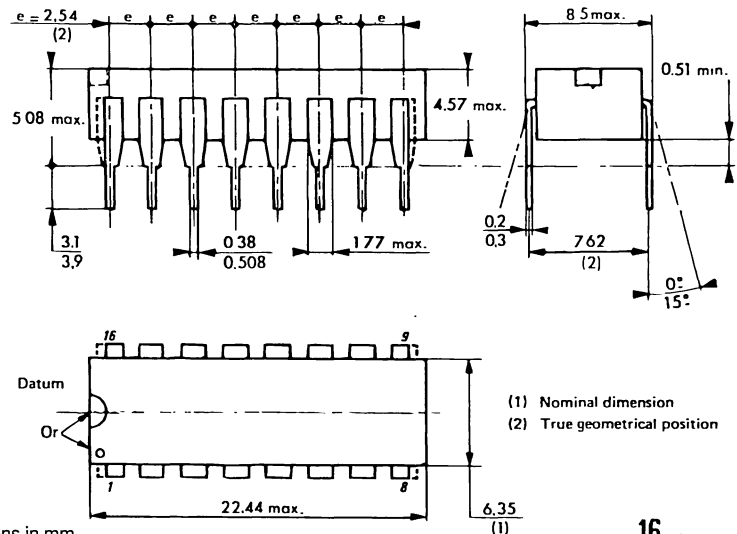
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8531-08

PACKAGE MECHANICAL DATA

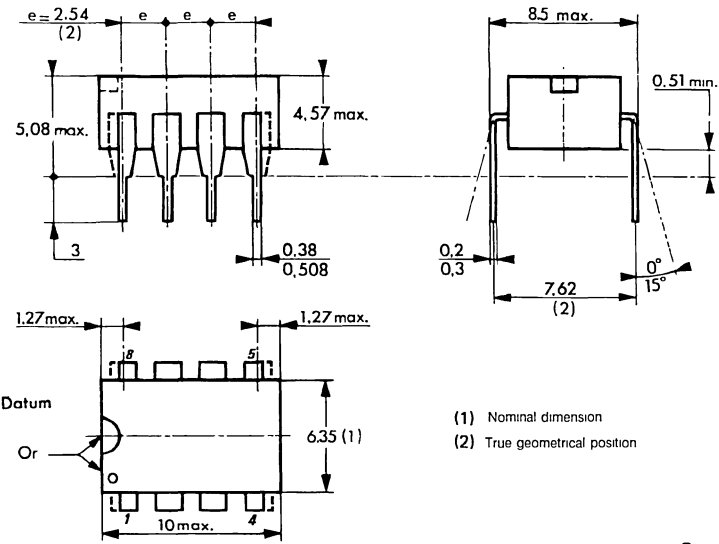
16 PINS - Plastic Dip



dimensions in mm

16 pins

8 PINS - Plastic Dip



dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8531XP
Ceramic	16 Pins Package : TSG8531XC
Cerdip	16 Pins Package : TSG8531XJ
Plastic	8 Pins Package : TSG85311XP

X : Temperature Range = C : 0°C, + 70°C
I : –25°C, + 85°C
V : –40°C, + 85°C
M : –55°C, + 125°C

SGS-THOMSON MICROELECTRONICS

TSG8532

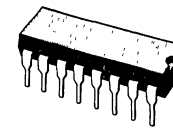
HIGHPASS POLYNOMIAL SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

FEATURES

- CHEBYCHEV TYPE
- 6th ORDER
- STOPBAND ATTENUATION : 60dB (typ) AT 0.25 x F_C
- PASSBAND RIPPLE : 0.45dB (typ)
- CLOCK TO CUT-OFF FREQ. RATIO : 500
- CLOCK FREQUENCY RANGE : 5 to 1800kHz
- CUT-OFF FREQUENCY RANGE : 10Hz to 3.6kHz

* According to spectrum aliasing phenomenon, the TSG8532 must be considered as a highpass filter only in the range [Fc, Fi/2], where Fi is the internal sampling frequency.

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information



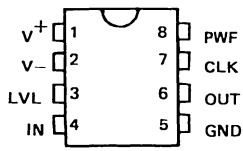
P
DIP-16
(Plastic Package)

P
DIP-8
(Plastic Package)

DESCRIPTION

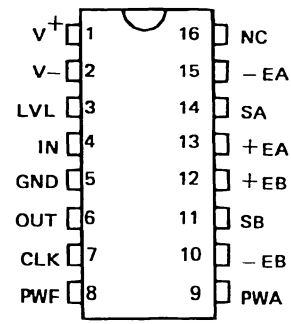
The TSG8532 is a HCMOS highpass* polynomial filter.

PIN CONNECTIONS



8 pins : FILTER ONLY

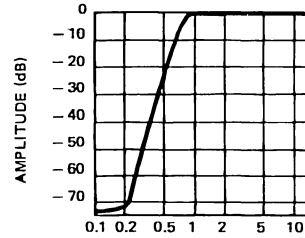
E88TSG8532-01



16 pins : FILTER + 2 OP-AMPs

E88TSG8532-02

AMPLITUDE RESPONSE CURVE



E88TSG8532-04

FILTER SPECIFICATIONS

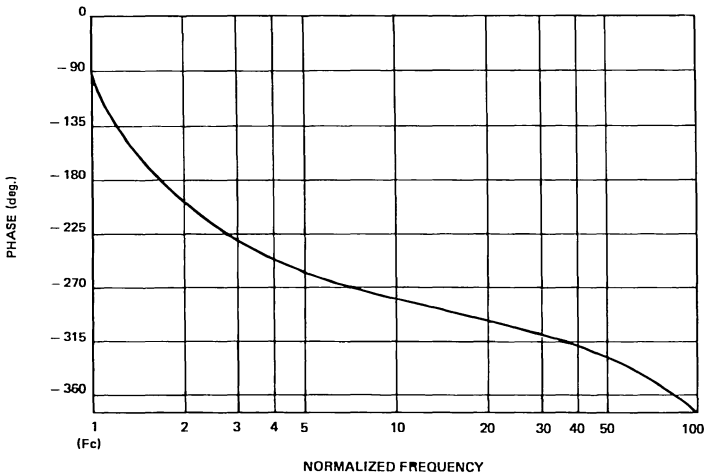
Highpass Filter : TSG8532 ; Type : Chebychev ; Order : 6.

V^+ = 5V, V^- = –5V, T = 25°C, RL = 5kΩ, CL = 100pF, I_{PWF} = 100µA

Symbol	Parameter		Typ.	Tested Limits	Unit
F_e	External Clock Frequency		5 1800(*)		kHz (min) kHz (max)
F_i	Internal Sampling Frequency		2.5 900(*)		kHz (min) kHz (max)
F_e/F_c	Clock to Cutoff Frequency Ratio		500 ± 1%		
F_c	Cutoff Frequency		0.01 3.6(*)		kHz (min) kHz (max)
G_o	Passband Gain		– 0.4 0		dB (min) dB (max)
A_p	Passband Ripple	[1Fc, 45 Fc] F_e = 500kHz	0.45	0.8	dB (max)
A_s	Stopband Attenuation	F 0.25F_c F_e = 500kHz	60	55	dB (min)
V_{off}	Output DC Offset Voltage	LVL = 0V	± 80	± 200	mV (max)
LVL	DC Level Adjustment		± 75		mV (max)
LG	Level gain		– 27		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	F_e=100kHz I_{pwa}=0µA	3.4	5	mA (max)
I^-	V^- Supply Current		3.4	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	F_e=50kHz F_{in}=1kHz	49		dB
$PSRR^-$	V^- Supply Rejection Ratio		46		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
V_o	Output Voltage Swing		+ 3.5 – 4.5		V_{p-p} (max)
V_n	Output Noise	BW=2kHz F_e=50kHz V_{in}=2V_{rms}	88		μV_{rms}
SNR	Signal to Noise Ratio		85		dB

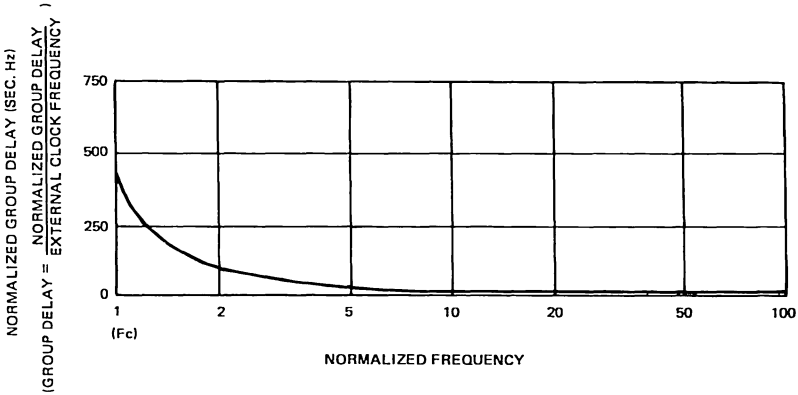
(*) At maximum Fe :
(with I_{pwf} = 250µA) - passband ripple : A_p = 0.8dB
- passband gain : G_o = – 0.8dB

PHASE RESPONSE CURVE (in passband)



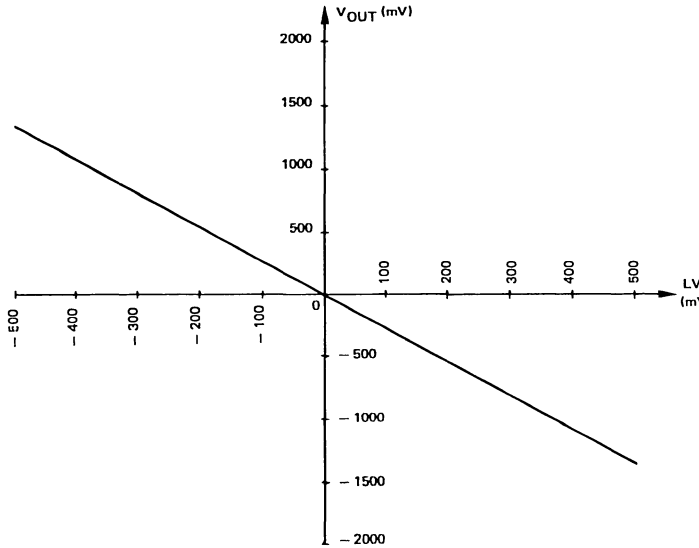
E88TSG8532-05

GROUP DELAY CURVE (in passband)



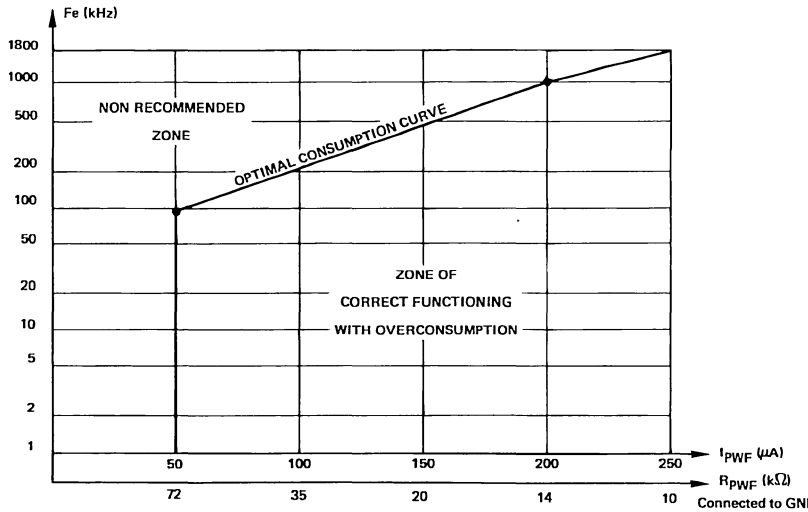
E88TSG8532-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8532-07

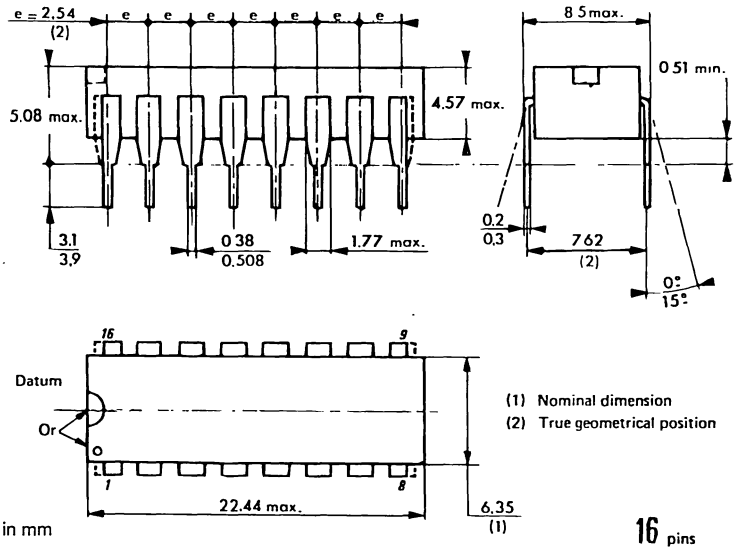
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8532-08

PACKAGE MECHANICAL DATA

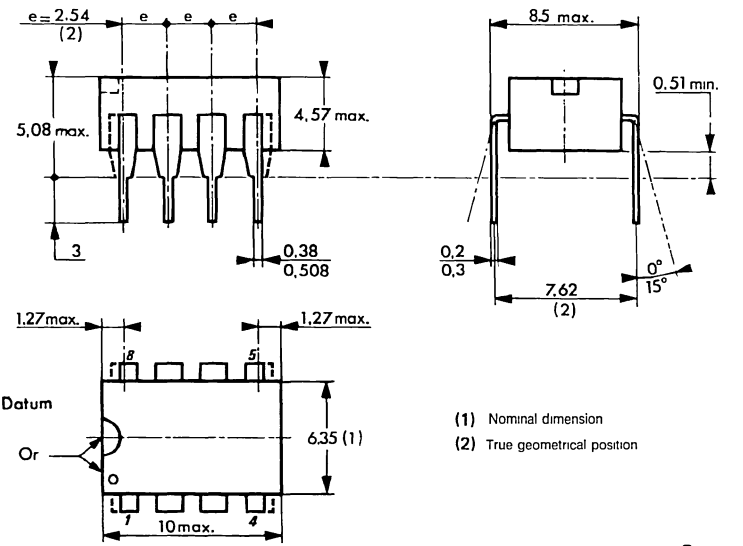
16 PINS - Plastic Dip



dimensions in mm

16 pins

8 PINS - Plastic Dip



dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8532XP
Ceramic	16 Pins Package : TSG8532XC
Cerdip	16 Pins Package : TSG8532XJ
Plastic	8 Pins Package : TSG85321XP

X : Temperature Range = C : 0°C, + 70°C
I : –25°C, + 85°C
V : –40°C, + 85°C
M : –55°C, + 125°C

SGS-THOMSON MICROELECTRONICS

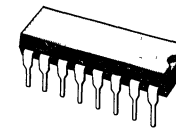
TSG8550

BANDPASS SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

FEATURES

- CAUER TYPE
- 6th ORDER
- SELECTIVITY FACTOR : Q = 7
- GAIN AT CENTER FREQUENCY : 0dB (typ)
- LOW STOPBAND ATTENUATION : 40dB (typ)
- HIGH STOPBAND ATTENUATION : 40dB (typ)
- CLOCK TO CENTER FREQ. RATIO : 48
- CLOCK FREQUENCY RANGE : 1 to 1200kHz
- CENTER FREQUENCY RANGE : 20.8Hz to 25kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



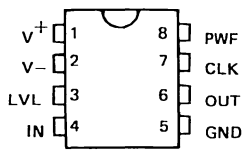
P
DIP-16
(Plastic Package)

P
DIP-8
(Plastic Package)

DESCRIPTION

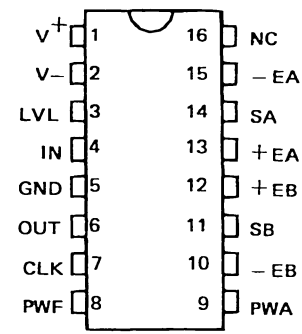
The TSG8550 is a HCMOS Cauer bandpass filter.

PIN CONNECTIONS



8 pins : FILTER ONLY

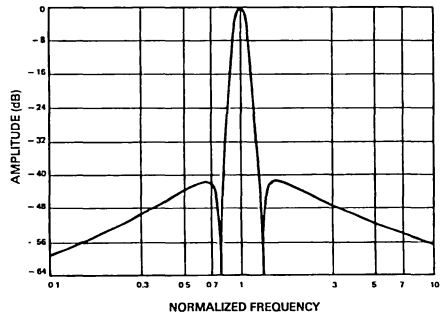
E88TSG8550-01



16 pins : FILTER + 2 OP-AMPs

E88TSG8550-02

AMPLITUDE RESPONSE CURVE



E88TSG8550-04

FILTER SPECIFICATIONS

Band-pass Filter : TSG8550 ; Type : Cauer ; Order : 6.

$V^+ = 5V$, $V^- = -5V$, $T = 25°C$, $RL = 5k\Omega$, $CL = 100pF$, $I_{PWF} = 50\mu A$

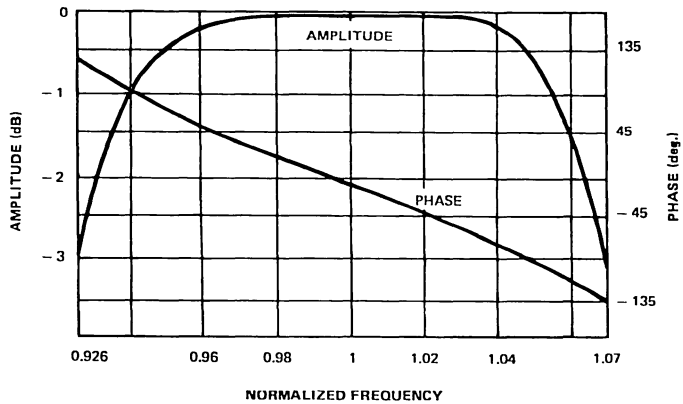
Symbol	Parameter		Typ.	Tested Limits	Unit
F_e	External Clock Frequency		1 1200(*)		kHz (min) kHz (max)
F_i	Internal Sampling Frequency		0.5 600(*)		kHz (min) kHz (max)
F_e/F_c	Clock to Cutoff Frequency Ratio		48 ± 1%		
F_o	Center Frequency		0.0208 25(*)		kHz (min) kHz (max)
G_o	Gain at Center Frequency	Typ. G_o=–0.2dB for F_e=48kHz	0	0 –2.2	dB (max) dB (min)
F_{lc}	Low Cutoff Frequency	F_{lc}=0.971 F_o	0.0204 24.5(*)		kHz(min) kHz(max)
F_{hc}	High Cutoff Frequency	F_{hc}=1.035 F_o	0.0216 25.9(*)		kHz(min) kHz(max)
BW	– 3dB Bandwidth	[0.926 F_o, 1.07 F_o]	0.003 3.15(*)		kHz (min) kHz (max)
Q	Selectivity Coefficient	Q = F_o/BW	7		
A_p	Passband Ripple		0.05	0.3	dB (max)
A_{ls}	Low Stopband Attenuation	F < 0.8 F_o	40.5	38	dB (min)
A_{hs}	High Stopband Attenuation	F > 1.24 F_o	40.5	38	dB (min)
V_{off}	Output DC Offset Voltage	LVL = 0V	±100	± 200	mV (max)
LG	Level Gain		– 1.7		
LVL	DC Level Adjustment		± 118		mV (max)
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)

(*) At maximum Fe : - stopband attenuation Als > 36dB for F > 0.8Fo
(with I_{pwf} = 250µA) - stopband attenuation Ahs > 42dB for F > 1.24Fo
- passband ripple A_p = 0.3dB
- Gain at center freq. G_0 = – 1.5dB
- – 3dB bandwidth BW = 3.15kHz [0.926Fo, 1.052Fo]
- Selectivity Q = 7.9

FILTER SPECIFICATIONS (continued)

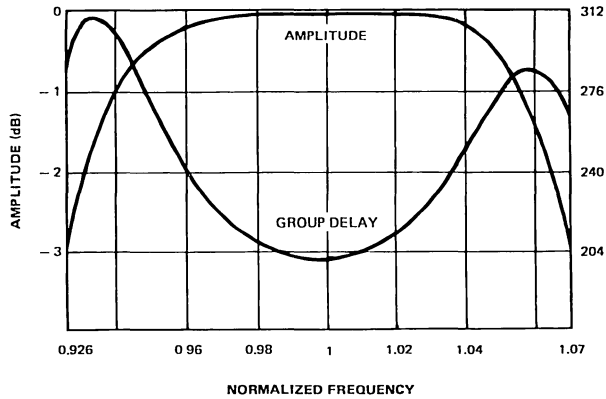
Symbol	Parameter		Typ.	Tested Limits	Unit
I^+	V^+ Supply Current	Fe = 48kHz Ipwa = 0µA	1.7	5	mA (max)
I^-	V^- Supply Current		1.7	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ratio	Fe = 48kHz Fin = 1kHz	9		dB
$PSRR^-$	V^- Supply Rejection Ratio		20		dB
Rin	Input Resistance		3		MΩ
Cin	Input Capacitance		20		pF
Vo	Output Voltage Swing		+ 3.5 − 4.5		Vp-p (max)
Vn	Output Noise	BW = 144kHz C_{PWF} = 33pF Fe = 48kHz Vin = 2Vrms	272		µVrms
SNR	Signal to Noise Ratio		78		dB

PHASE RESPONSE CURVE (in passband)



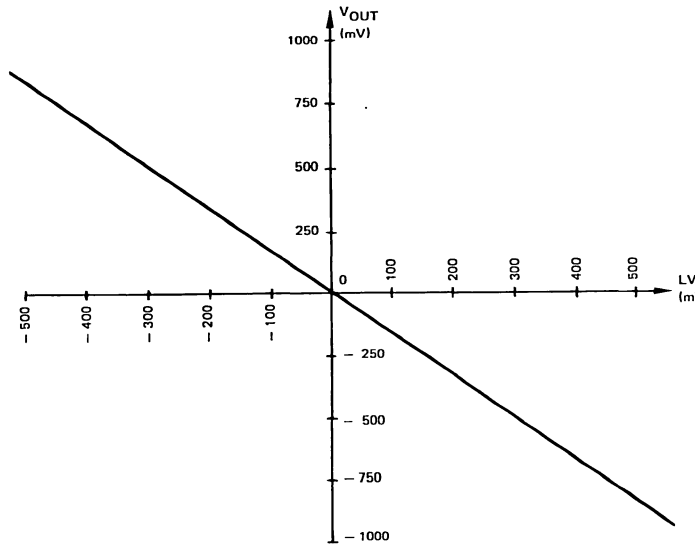
E88TSG8550-05

GROUP DELAY CURVE (in passband)



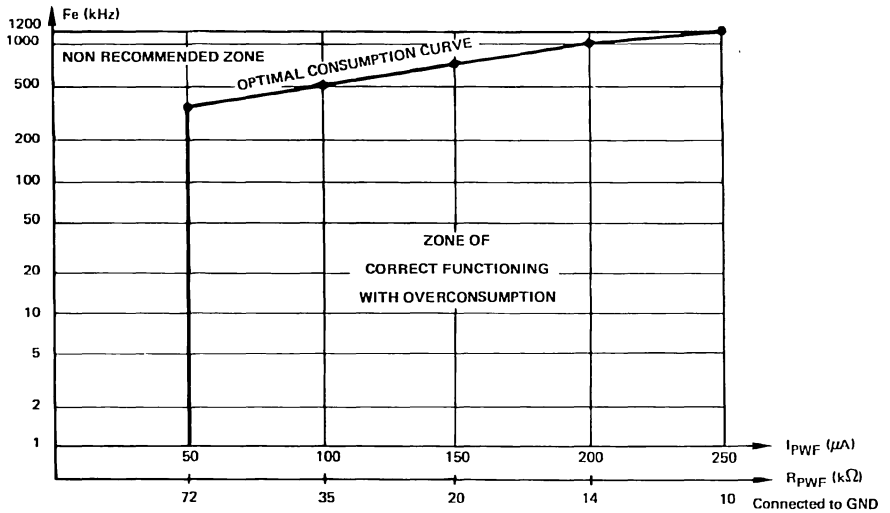
E88TSG8550-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8550-07

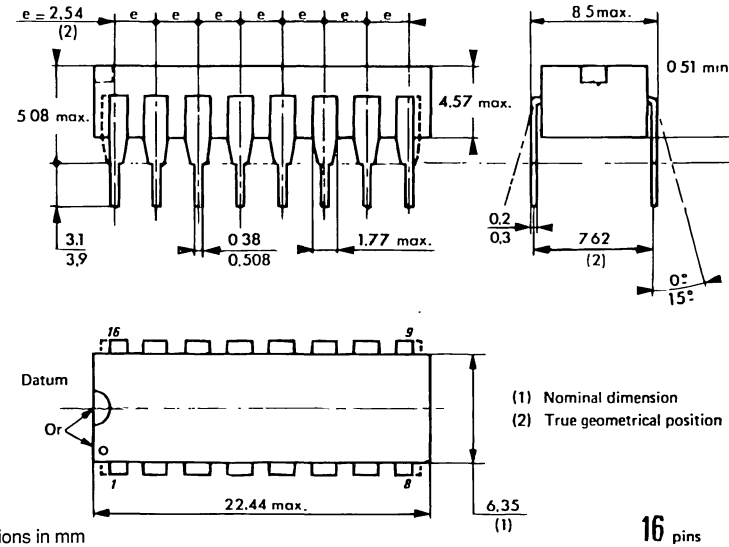
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8550-08

PACKAGE MECHANICAL DATA

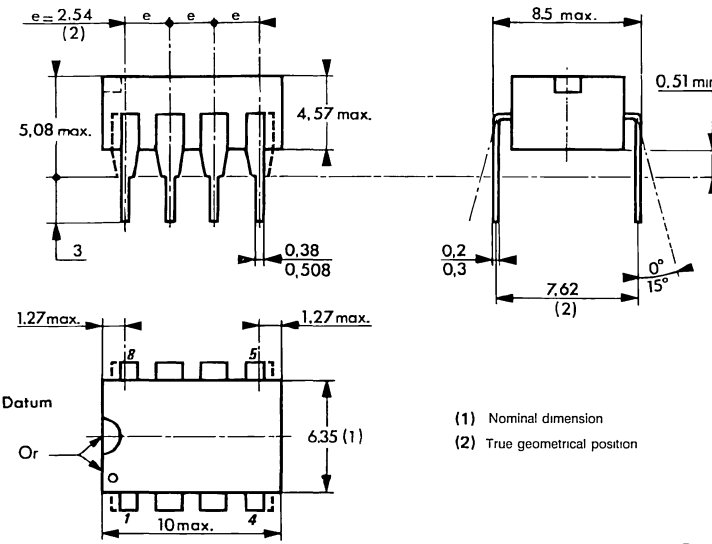
16 PINS - Plastic Dip



dimensions in mm

16 pins

8 PINS - Plastic Dip



dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8550XP
Ceramic	16 Pins Package : TSG8550XC
Cerdip	16 Pins Package : TSG8550XJ
Plastic	8 Pins Package : TSG85501XP

X : Temperature Range = C : 0°C, + 70°C
I : –25°C, + 85°C
V : –40°C, + 85°C
M : –55°C, + 125°C

SGS-THOMSON MICROELECTRONICS

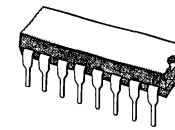
TSG8551

HIGH SELECTIVITY BANDPASS SWITCHED CAPACITOR MASK PROGRAMMABLE FILTER

FEATURES

- 8th ORDER
- SELECTIVITY FACTOR : Q = 35
- GAIN AT CENTER FREQUENCY : 30dB (typ)
- LOW STOPBAND ATTENUATION : 70dB (typ)
- HIGH STOPBAND ATTENUATION : 70dB (typ)
- CLOCK TO CENTER FREQ. RATIO : 187.2
- CLOCK FREQUENCY RANGE : 4 to 3800kHz
- CENTER FREQUENCY RANGE : 22Hz to 20.3kHz

Note : For general characteristics, see TSG85XX specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



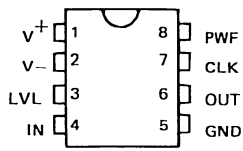
P
DIP-16
(Plastic Package)

P
DIP-8
(Plastic Package)

DESCRIPTION

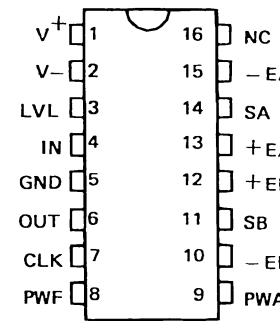
The TSG8551 is a HCMOS high selectivity bandpass filter.

PIN CONNECTIONS



8 pins : FILTER ONLY

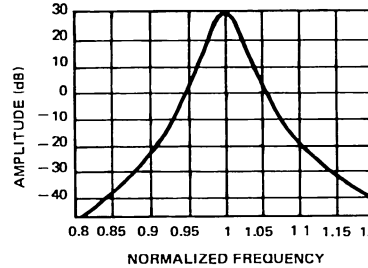
E88TSG8551-01



16 pins : FILTER + 2 OP-AMPs

E88TSG8551-02

AMPLITUDE RESPONSE CURVE



E88TSG8551-04

FILTER SPECIFICATIONS

Bandpass Filter : TSG8551 ; Type : High Q ; Order : 8.

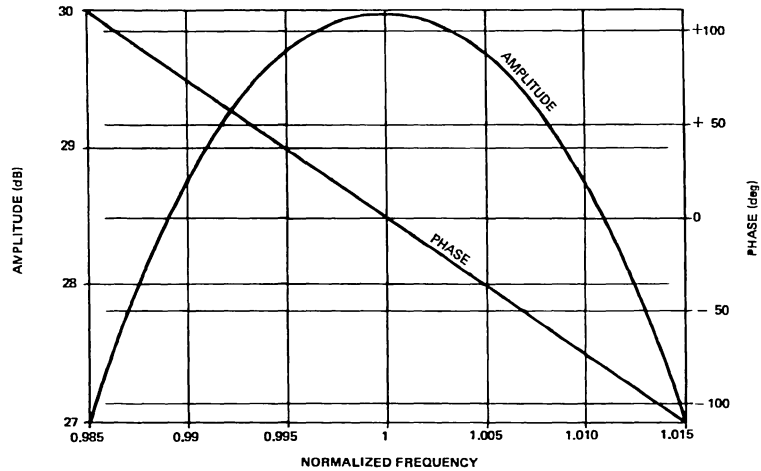
V^+ = 5V, V^- = –5V, T = 25°C, RL = 5kΩ, CL = 100pF, I_{PWF} = 1000µA

Symbol	Parameter		Typ.	Tested Limits	Unit
F_e	External Clock Frequency		4 3800(*)		kHz (min) kHz (max)
F_i	Internal Sampling Frequency		0.5 475(*)		kHz (min) kHz (max)
F_e/F_o	Clock to Cutoff Frequency Ratio		187.2 ± 1%		
F_o	Center Frequency		0.022 20.3(*)		kHz (min) kHz (max)
G_o	Gain at Center Frequency	F_e=400kHz	30	32 26	dB (max) dB (min)
Q	Selectivity Coefficient		35		
A_p	Passband Ripple				dB (max)
A_{ls}	Low Stopband Attenuation	F 0.8 F_o	70	55	dB (min)
A_{hs}	High Stopband Attenuation	F 1.2 F_o	70	55	dB (min)
V_{off}	Output DC Offset Voltage	LVL = 0V	±100	± 200	mV (max)
LVL	DC Level Adjustment		± 70		mV (max)
LG	Level Gain		– 3.3		
R_{PWF}	PWF Resistance		10 72		kΩ (min) kΩ (max)
I_{PWF}	Input Current on PWF		50 250		µA (min) µA (max)
I^+	V^+ Supply Current	F_e=100kHz I_{pwa}=0µA	3.8	5	mA (max)
I^-	V^- Supply Current		3.8	5	mA (max)
$PSRR^+$	V^+ Supply Rejection Ration	F_e=187.2kHz F_{in}=1kHz	10**		dB
$PSRR^-$	V^- Supply Rejection Ratio		19**		dB
R_{IN}	Input Resistance		3		MΩ
C_{IN}	Input Capacitance		20		pF
V_o	Output Voltage Swing		+ 3.5 – 4.5		V_{p-p} (max)
V_n	Output Noise	BW=3Hz F_e=2187.2kHz V_{in}=2V_{rms}	56**		μV_{rms}
SNR	Signal to Noise Ratio		90**		dB

* I_{PWF} = 200µA

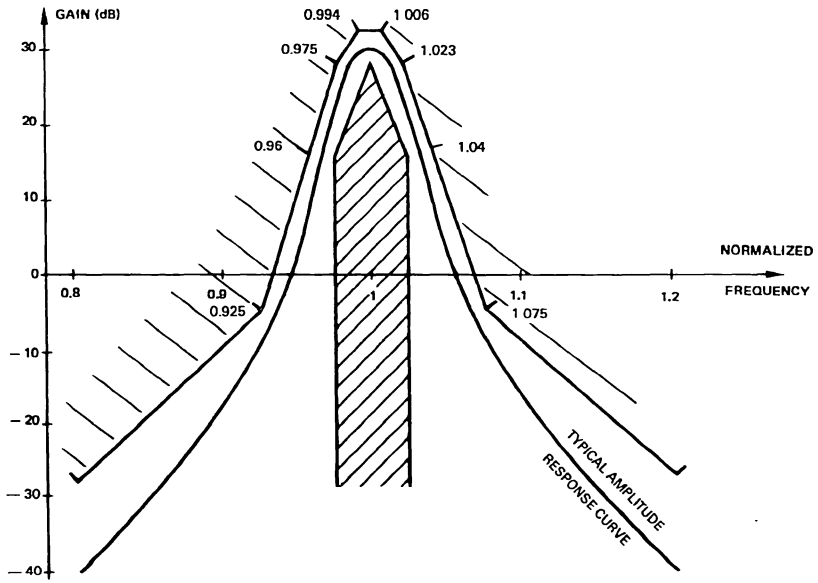
* * Value divided by the gain.

PHASE RESPONSE CURVE (in passband)



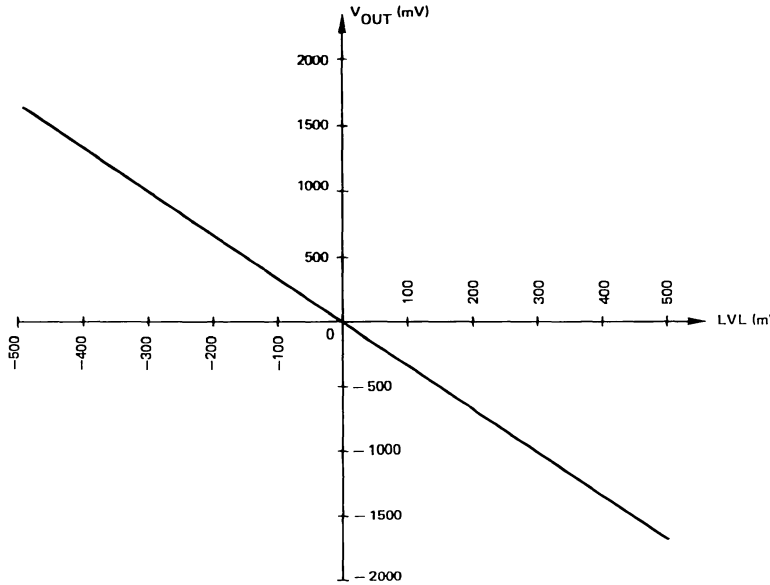
E88TSG8551-05

AMPLITUDE RESPONSE TEMPLATE (tested)



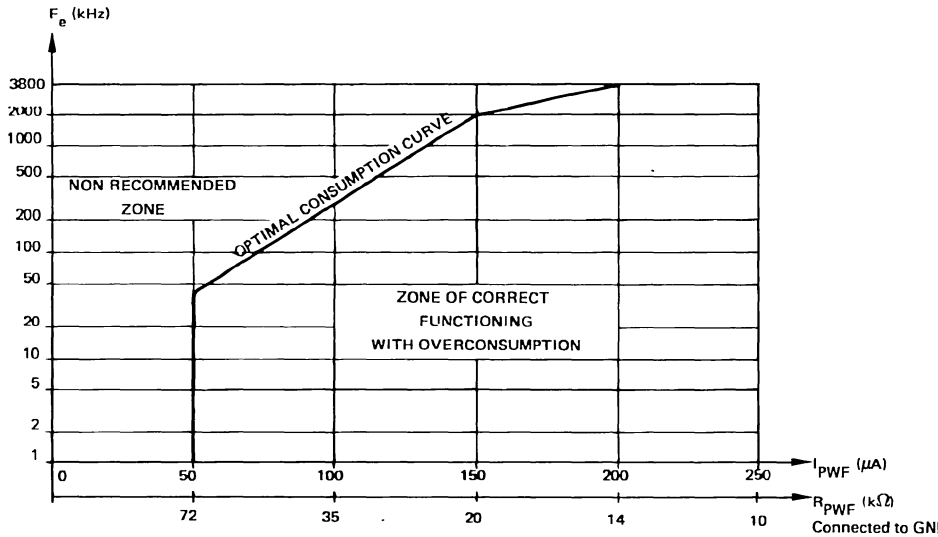
E88TSG8551-06

OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8551-07

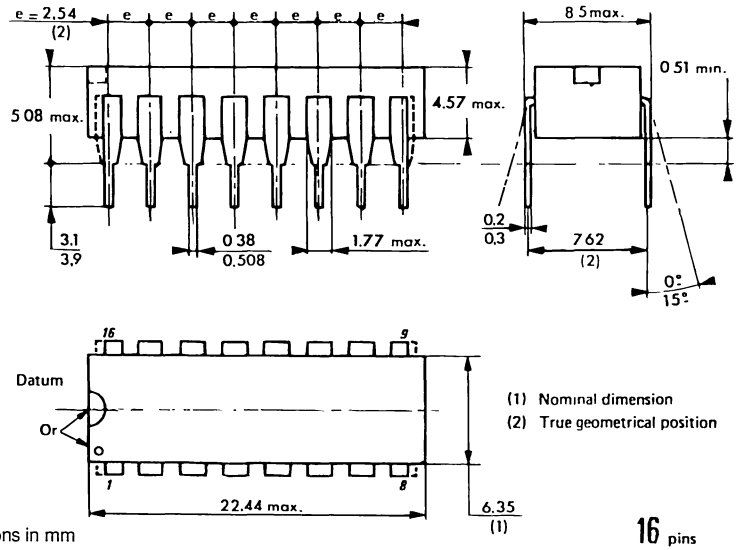
USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8551-08

PACKAGE MECHANICAL DATA

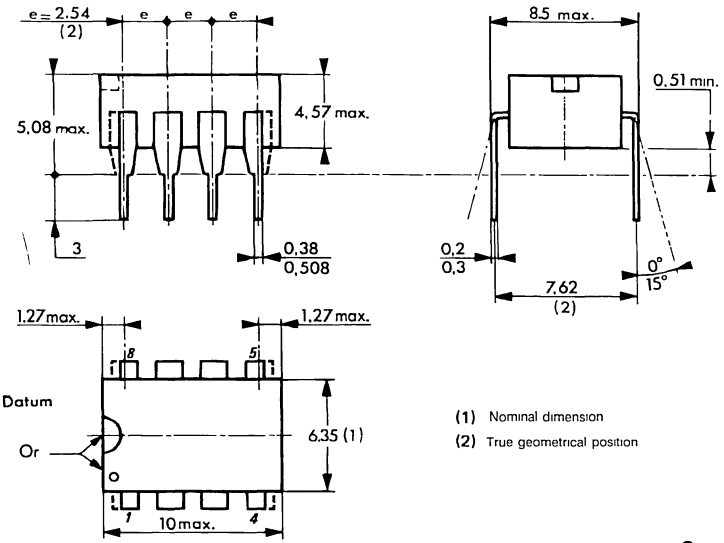
16 PINS - Plastic Dip



dimensions in mm

16 pins

8 PINS - Plastic Dip



dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8551XP
Ceramic	16 Pins Package : TSG8551XC
Cerdip	16 Pins Package : TSG8551XJ
Plastic	8 Pins Package : TSG85511XP

X : Temperature Range = C : 0°C, + 70°C
I : –25°C, + 85°C
V : –40°C, + 85°C
M : –55°C, + 125°C

SGS-THOMSON MICROELECTRONICS

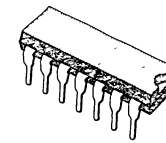
TSG8751

HIGH SELECTIVITY BANDPASS SWITCHED CAPACITOR FILTER

FEATURES

- 4th ORDER
- SELECTIVITY FACTOR Q = 25
- GAIN AT CENTER FREQUENCY G_O : 20dB (typ.)
- LOW STOPBAND ATTENUATION : G_O : – 65dB (typ.) AT $f < 0.3\ f_O$
- HIGH STOPBAND ATTENUATION : G_O : – 65dB (typ.) AT $f > 3\ f_O$
- CLOCK TO CENTER FREQ. RATIO : 60
- CLOCK FREQUENCY RANGE : 1.5 to 720kHz
- CENTER FREQUENCY RANGE : 25Hz to 12kHz

Note : For general characteristics, see TSGF04 specifications. For non standard quality level, consult SGS-THOMSON general ordering information.



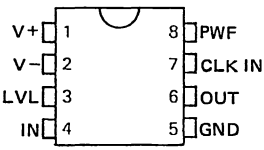
P
DIP-14
(Plastic Package)

P
DIP-8
(Plastic Package)

DESCRIPTION

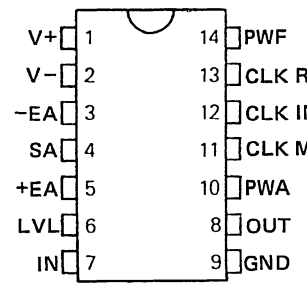
The TSG8751 is a HCMOS high selectivity bandpass filter.

PIN CONNECTIONS



8 pins : FILTER ONLY
DIP-8 Package

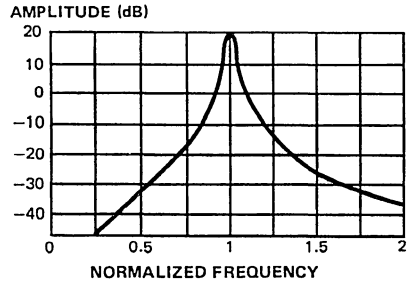
E88TSG8751-01



14 pins : FILTER + 1 OP-AMP
DIP-14 Package

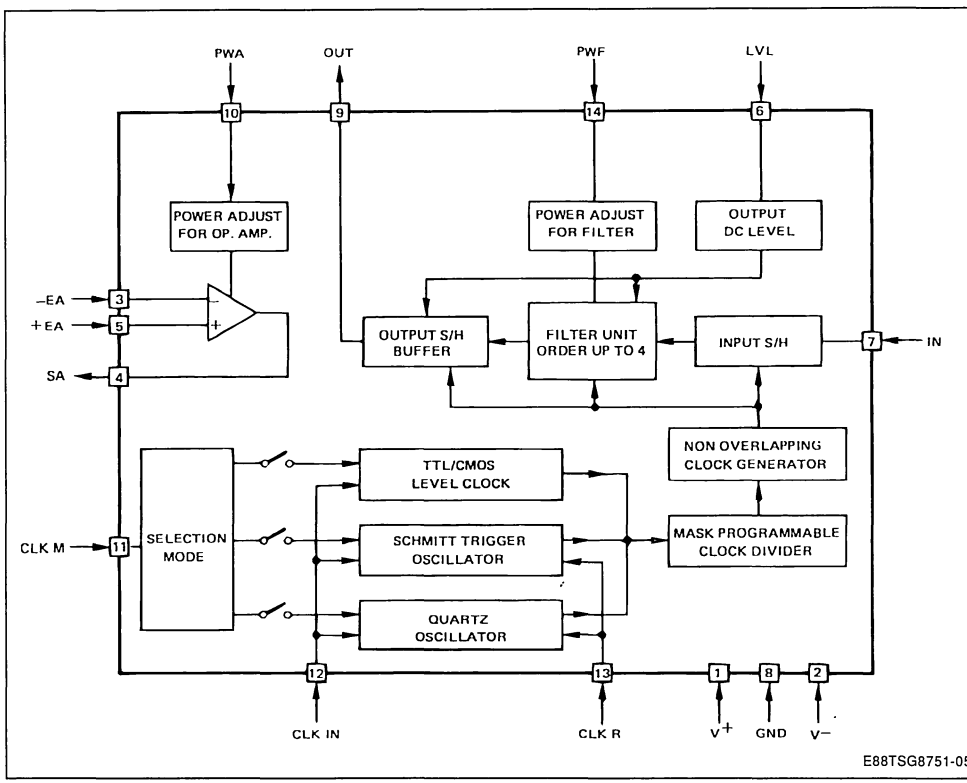
E88TSG8751-02

AMPLITUDE RESPONSE CURVE



E88TSG8751-04

BLOCK DIAGRAM



E88TSG8751-05

FILTER SPECIFICATIONS

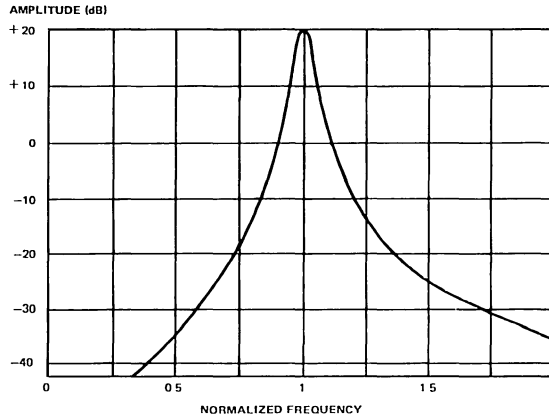
ELECTRICAL OPERATING CHARACTERISTICS

T_{amb}=25°C, V^+ = 5V, V^- = – 5V, R_L = 5kΩ, CL = 100pF, I_{PWF} = 50µA (unless otherwise specified)

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
F_e	External Clock Frequency		1.5		720(*)	kHz
F_i	Internal Sampling Frequency		0.75		360(*)	kHz
F_e/F_o	Clock to Center Frequency Ratio		58.8	60	61.2	
F_o	Center Frequency	$f_0=(f_{lc} + f_{hc})$ 2	0.025		12(*)	kHz
G_o	Gain at Center Frequency	F_e=60kHz I_{PWF}=50µA	19	20	21	dB
F_{lc}	Low Cut Off Frequency	F_{lc}=0.98 F_o	0.0245		11.76	kHz
F_{hc}	High Cut Off Frequency	F_{hc}=1.02 f_0	0.0255		12.24	kHz
BW	–3dB Bandwich	[0.98 f_0, 1.02 f_0]	1		480	Hz
Q	Quality Factor	Q = f_0 BW		25		
A_{ls}	Low Stopband Attenuation	f 0.3 f_0	G_0 – 63	G_0 – 65		dB
A_{hs}	High Stopband Attenuation	f 3 f_0	G_0 – 63	G_0 – 65		dB
V_{off}	Output DC Offset Voltage	LVL=0V I_{PWF}=50µA		± 100	± 200	mV
LVL	DC Level Adjustment			± 67		mV
LG	Level Gain			3		
R_{PWF}	PWF Resistance		20		72	kΩ
I_{PWF}	Input Current on PWF		50		150	mA
I^+ I^-	Supply Current	F_e=60kHz I_{PWF}=50µA I_{PWA}=0µA		1.6 1.6	3 3	mA
PSRR + PSRR –	Supply Rejection Ratio	F_e=60kHz F_{in}=1kHz		30(**) 31(**)		dB
R_{IN}	Input Resistance			3		MΩ
C_{IN}	Input Capacitance			20		pF
V_o	Output Voltage Swing			+ 3.5 – 4.5		VPP
V_A	Output Noise	BW=1kHz F_e=60kHz V_{IN}=2V_{rms}		91.8(**)		µV_{rms}
SNR	Signal to Noise Ratio			66		dB

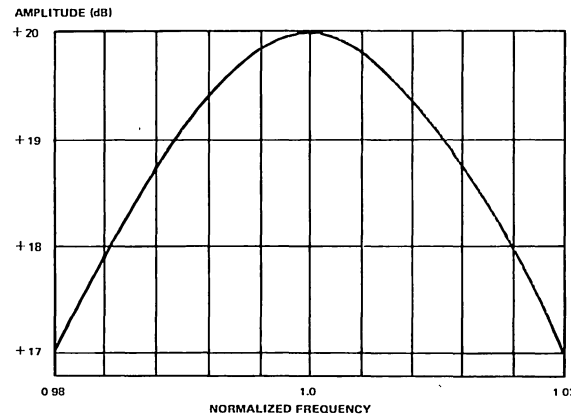
(*) At maximum f_e (with I_{PWF} = 150µA) : f_e/f_o = 61 ± 2%.
(**) Value divided by the gain.

TYPICAL AMPLITUDE RESPONSE CURVE



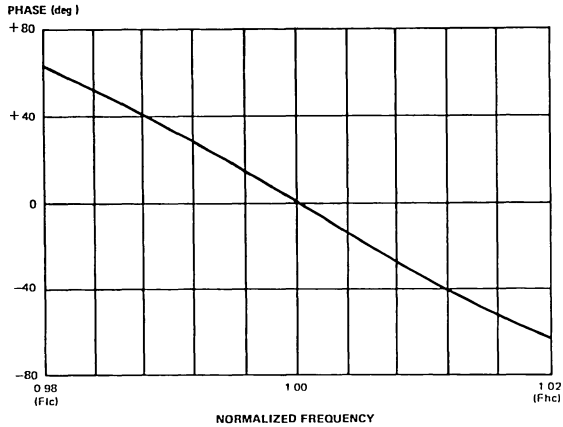
E88TSG8751-06

TYPICAL AMPLITUDE RESPONSE CURVE IN PASSBAND



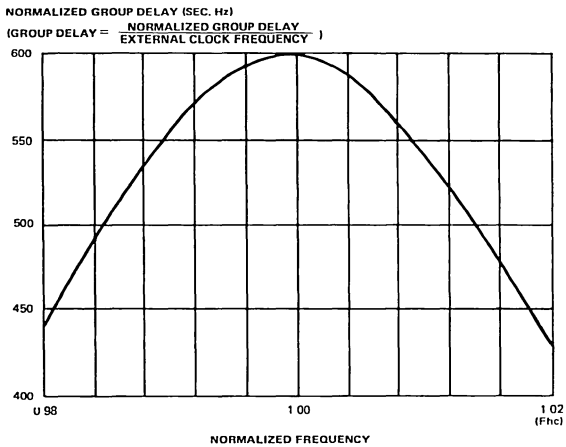
E88TSG8751-07

TYPICAL PHASE RESPONSE CURVE IN PASSBAND



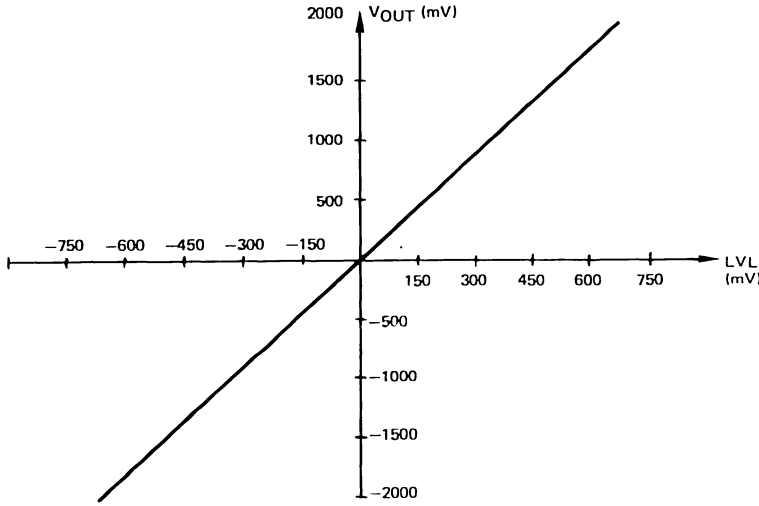
E88TSG8751-08

TYPICAL GROUP DELAY CURVE IN PASSBAND



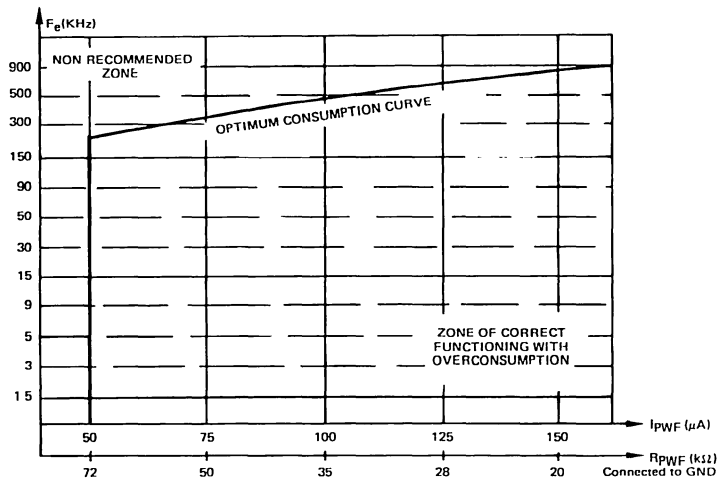
E88TSG8751-09

TYPICAL OUTPUT DC VOLTAGE ADJUSTMENT FROM LVL PIN



E88TSG8751-10

USER'S GUIDE FOR I_{PWF} AND R_{PWF} CHOICE



E88TSG8751-11

CLOCK OSCILLATOR

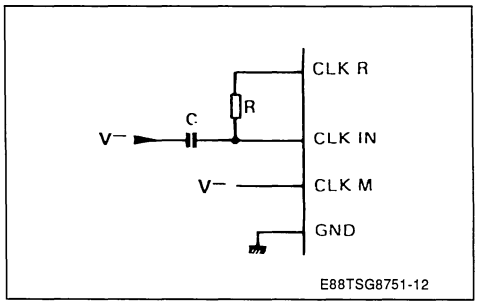
The TSGF04 base accepts external compatible TTL/CMOS clocks on CLKIN pin and provides an internal oscillator performed either by RC or crystal connected between CLKIN and CLKR pins.

The clock selection mode is provided by CLKM pad which can be connected to V- or GND voltage levels. This connection is realized by two means, depending on the package type chosen :

– with 14-pin package, via pin CLKM

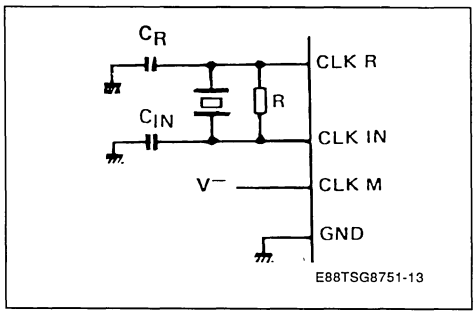
– with 8-pin package, by internal connection readily performed, only on custom filters.

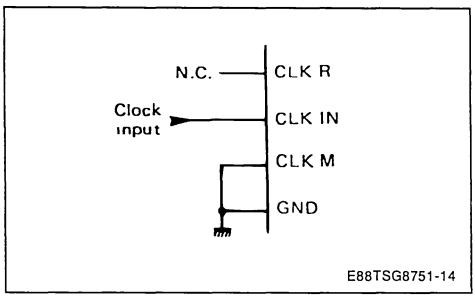
(note that CLKM pin connected to V+, allows the selection of the internal crystal-controlled oscillator, but the selection by CLKM connected to V- is recommended).



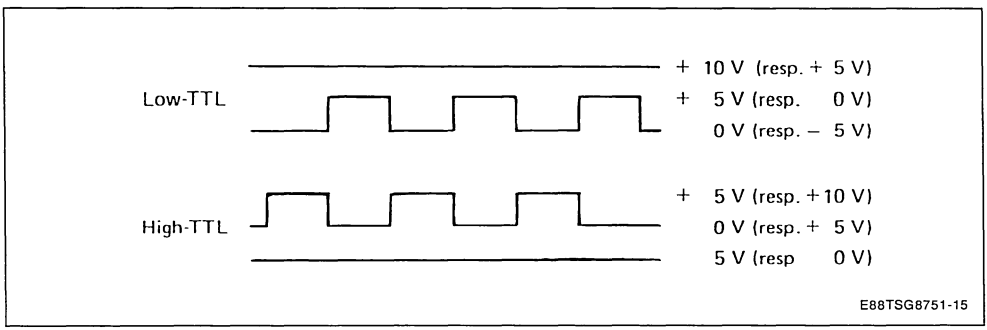
The different possibilities are :

– two internal oscillator modes
  - RC
  - Crystal
- three external clocks
  – low-TTL
  – high-TTL
  – CMOS





The "Low-TTL" and "High-TTL" clock levels are :



For each package version, the following tables resume, the availability of the different clocks, in terms of the power supply.

Note that in 8-pin version, the clock mode (CLKM) is internally set to GND voltage, except in the case of CMOS clock and 0-5V power supply, where CLKM is internally connected to V- voltage.

8-Pin Package			
	0.5V	**0.10V**	**– 5. + 5V**
Low-TTL	NO	C	C
High-TTL	NO	YES	YES
CMOS	C	YES	YES
RC Mode	NO	NO	NO
Crystal Mode	NO	NO	NO

C = Customization option.

14-Pin Package			
	0.5V	**0.10V**	**– 5. + 5V**
Low-TTL	NO	C	C
High-TTL	NO	CLKM=GND	CLKM=GND
CMOS	CLKM = V^-	CLKM=GND	CLKM=GND
RC Mode	CLKM = V^-	CLKM = V^-	CLKM = V^-
Crystal Mode	CLKM = V^-	CLKM = V^-	CLKM = V^-

ELECTRICAL OPERATING CHARACTERISTICS

WITH DUAL SUPPLY VOLTAGE
T_{amb} = 25°C, V+ = 5V, V– = – 5V, GND = 0V, (unless otherwise specified)

Symbol	Parameter	Value			Unit
		Min.	**Typ.**	**Max.**	
GND	Threshold Voltage		1.5		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	1	1.25	1.5	V
	Corresponding Voltage on CLKR		– 5		V
	Low Threshold Voltage on CLKIN	– 1.5	– 1.25	– 1	V
	Corresponding Voltage on CLKR		+ 5		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	MHz
	Resistor		1		MΩ
	Capacitor C_R	10		100	pF
	Capacitor C_{IN}	10		30	pF

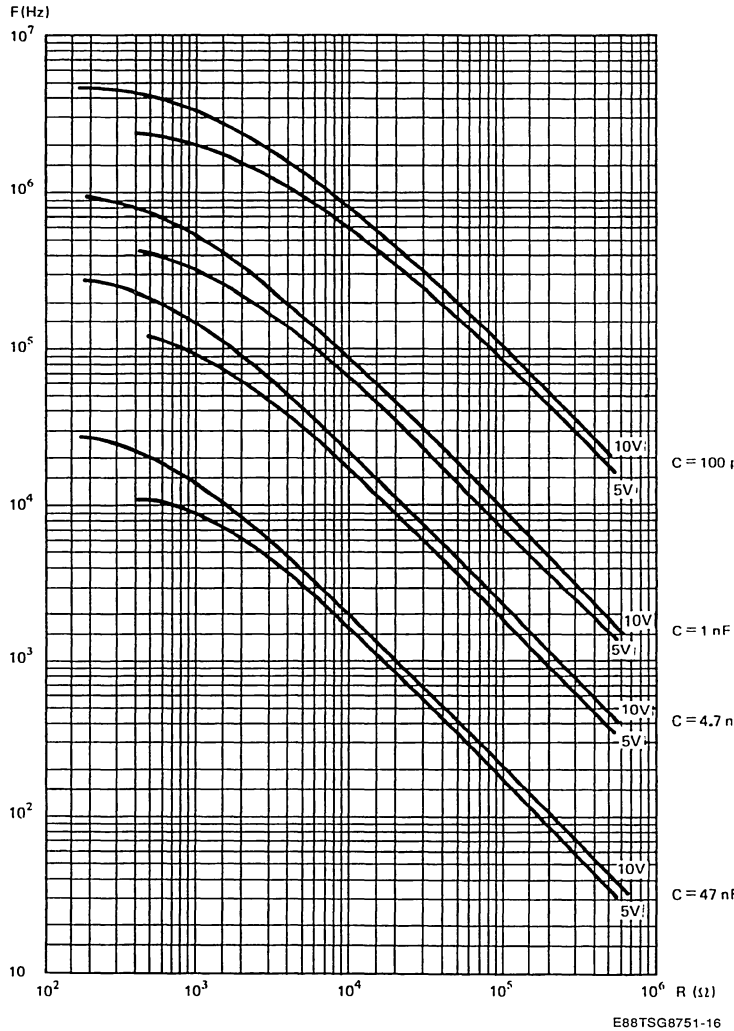
ELECTRICAL OPERATING CHARACTERISTICS (continued)

WITH SINGLE SUPPLY VOLTAGE
T_{amb} = 25°C, V+ = 10V, V– = 0V, GND = 5V, (unless otherwise specified)

CLKM	Parameter	Value			Unit
		Min.	Typ.	Max.	
GND	Threshold Voltage		6.5		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	6	6.25	6.5	V
	Corresponding Voltage on CLKR		0		V
	Low Threshold Voltage on CLKIN	3.5	3.75	4	V
	Corresponding Voltage on CLKR		+ 10		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				30
	Oscillator Frequency			5	
	Resistor		1		MHz
	Capacitor C_R	10			MΩ
	Capacitor C_{IN}	10		100	pF

WITH SINGLE SUPPLY VOLTAGE
T_{amb} = 25°C, V+ = 5V, V– = 0V, GND = 2.5V, (unless otherwise specified)

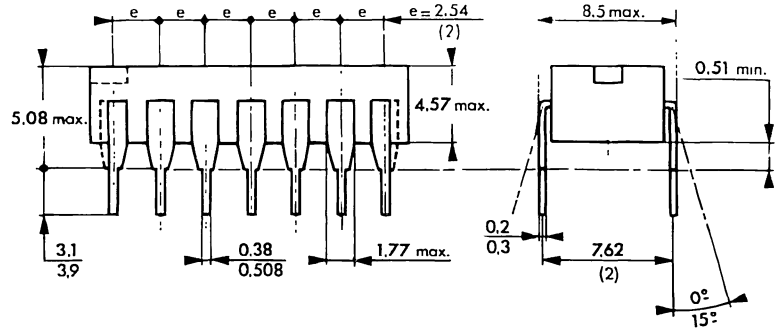
CLKM	Parameter	Value			Unit
		Min.	Typ.	Max.	
GND	Threshold Voltage		3.8		V
	External Clock Frequency			5	MHz
V –	RC MODE :				
	High Threshold Voltage on CLKIN	3	3.2	3.4	V
	Corresponding Voltage on CLKR		0		V
	Low Threshold Voltage on CLKIN	1.5	1.8	2	V
	Corresponding Voltage on CLKR		+ 5		V
	Oscillator Frequency			5	MHz
	Resistor	2		10 000	kΩ
	Capacitor	0		47	nF
V –	CRYSTAL MODE :				
	Oscillator Frequency			5	
	Resistor		1		MHz
	Capacitor C_R	10		100	MΩ
	Capacitor C_{IN}	10		30	pF



With internal RC oscillator mode, the user's guide for R and C choice is given by following curves and for both supply voltages : 0-5V, 0-10V.

PACKAGE MECHANICAL DATA

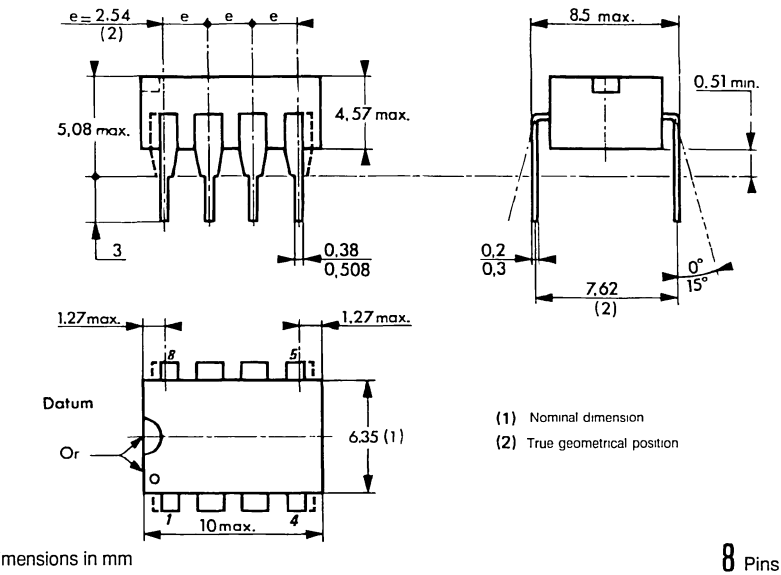
14 PINS - Plastic Dip



dimensions in mm

14 Pins

8 PINS - Plastic Package



dimensions in mm

8 Pins

ORDER INFORMATION

Plastic	16 Pins Package : TSG8751XP
Ceramic	16 Pins Package : TSG8751XC
Cerdip	16 Pins Package : TSG8751XJ
Plastic	8 Pins Package : TSG87511XP

X : Temperature Range = C : 0°C, + 70°C
I : –25°C, + 85°C
V : –40°C, + 85°C
M : –55°C, + 125°C

APPLICATION NOTES

HOW TO CHOOSE A FILTER IN A SPECIFIC APPLICATION

By O. Leenhardt

INTRODUCTION

OBJECT OF THIS APPLICATION NOTE

The approach of SGS-THOMSON Microelectronics regarding filtering is aimed at providing all the information required for designing the filter best tailored for a given application. The first step in this approach, and undoubtedly the most important since it is essential for all the others, therefore consists in indicating how, starting from this application, the complete system specifications of a filter must be written. This is the purpose of this application note.

REMINDERS ABOUT THE PRESENT STATUS OF THE SGS-THOMSON FILTERS

The SGS-THOMSON approach consists in manufacturing Mask Programmable Filters (M.P.F). These filters are of the switched capacitor type. They all have the same structure, up to the last mask level (interconnection level). This level is therefore the only one differenciating these filters from one another. We will not describe in full detail the structure of these filters, but simply remind their main features, and then briefly describe the presently available M.P.F's.

MAIN FEATURES :

The main features of these M.P.F's are as follows :

- TECHNOLOGY HCMOS1 (high-density linear CMOS)
- AVAILABLE ORDERS 2 TO 12 (whatever the type of M.P.F.)
- INPUT SIGNAL FREQUENCY 0 TO 30KHz
- INTERNAL SAMPLING FREQUENCY : 500Hz TO 1MHz (depending on the M.P.F. considered)
- INTERNAL SAMPLING FREQUENCY/CUT-OFF FREQUENCY RATIO : 10 TO 200 (depending on the M.P.F. considered)
- THE RESPONSE CURVES (amplitude and phase) may be translated by changing the sampling frequency
- SIGNAL/NOISE RATIO : 70 TO 85dB (depending on the internal structure of the M.P.F. considered)
- POWER SUPPLIES : + 5V OR - 10V
- CONSUMPTION MAY BE ADJUSTED BETWEEN 0.5 TO 20mW PER ORDER
- ACCURACY OF THE CAPACITOR RATIOS : 0.1%
- ACCURACY OF THE CUT-OFF FREQUENCIES : 0.5% (max.).

STANDARD M.P.F.'S AND CUSTOM M.P.F.'S :

SGS-THOMSON MANUFACTURES TWO TYPES OF M.P.F.'S

- Standard M.P.F.'s :

They make up a family presently consisting of 10 models, but this family will expand in the future, according to the evolution of requirements. These M.P.F.'s are the following :

- 5 Low-pass M.P.F.'s :
  TS 8510 (CAUER, 5th order : 32dB attenuation)
  TS 9511 (CAUER, 7th order : 50dB attenuation)
  TS 8512 (CAUER, 7th order : 75dB attenuation)
  TS 8513 (CHEBYCHEV, 8th order)
  TS 8514 (BUTTERWORTH, 8th order)
- 3 High-pass M.P.F.'s :
  TS 8530 (CAUER, 3rd order : 15dB attenuation)
  TS 8531 (CAUER, 6th order : 15dB attenuation)
  TS 8532 (CHEBYCHEV, 6th order)
- 1 Notch M.P.F.'s :
  TS 8540 (8th order : Q = 7)
- 2 Band-pass M.P.F.'s :
  TS 8550 (CAUER, 3rd order : Q = 5)
  TS 8551 (high-selectivity filter Q : 35)

Note : The detailed description of these M.P.F.'s has been the subject of a previous application note.

- Custom M.P.F.'s :

SGS-THOMSON commits itself to supply the first samples 4 to 6 weeks after the customer's definition of the template. All types of filters may be provided (BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL, CAUER), for conventional applications (low-pass, high-pass, bandpass, notch filters, group delay equalizers) or for simultaneous optimization of the amplitude and the phase templates.

HOW TO DEFINE THE COMPLETE SYSTEM SPECIFICATIONS OF A FILTER

FILTER SYSTEM SPECIFICATIONS

The system specifications of a filter are complete when they indicate :

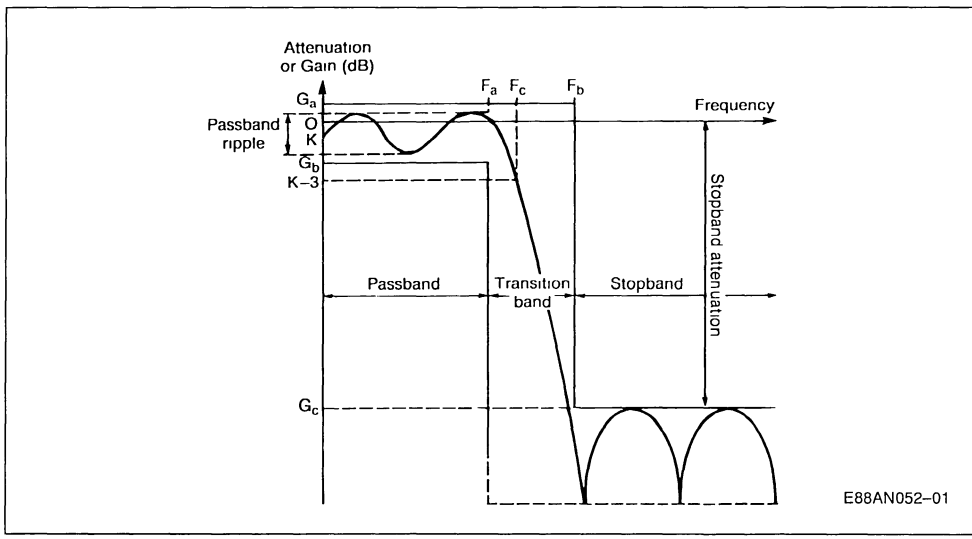
- the amplitude template (amplitude response curve)
- the phase template (phase response curve)
- the group delay curve
- the pulse and step responses
- the dynamics
- the noise factor
- the input and output impedances
- the load impedance (resistance and capacitance)
- the type of signals to filter (level, spectrum,...)
- the value of the power supply sources
- the operating temperature range
- the size (the dimensions)
- the price

Amongst all these parameters, the knowledge of three of them is essential from the technical point of view :

- the amplitude template
- the phase template
- the group delay curve.

As we shall see later on, the following definitions may be used, with minor modifications, for all types of filters. Our definitions are given only for low-pass filters, since we can always relate back to this type when studying any other kind of filter (see 3.B).

Figure 1 : Different Parameters used for Defining an Amplitude Template.



- Amplitude Template (figure1) :

We cannot expect two filters, assumed to be similar, to have exactly identical response curves. This is the reason why we use the concept of template, which is a sort of envelope of the response curve limits in terms of the frequency. The amplitude template is therefore the graphical representation of the filter's "amplitude - frequency" limiting conditions. Its definition is based on the following parameters (low-pass filter) :

- maximum passband attenuation (or gain) (G_a) : maximum level the signal may reach within the passband (in dB).
- minimum passband attenuation (or gain) (G_b) : minimum level the signal may reach within the passband (in dB).
- minimum stopband attenuation (Gc) : minimum attenuation level of the signal within the stopband (in dB).
- passband band of frequencies for which the attenuation (or the gain) must fall between G_a and G_b.
- transition band : band of frequencies for which the attenuation must fall between G_b and G_c.
- stopband : band of frequencies for which the attenuation must be less than G_c.
- cut-off frequency (F_a) : passband upper limit.

- selectivity factor k : equal to the ratio F_a/F_b, it defines the width of the template transition band, and therefore of the filter selectivity. It is always less than 1.

Other parameters must be added when the response curve considered falls within this template :

- passband transfer factor (K) : attenuation (or gain) factor of the response curve within the passband, relative to the 0dB (in dB).
- passband ripple : maximum amplitude difference between two points of the response curve within the passband.
- cut-off frequency (F_c) : frequency corresponding to a 3dB attenuation relative to the passband transfer factor.

Note : The template of a filter is therefore completely determined once the values of G_a, G_b, G_c, F_a and F_b are known.

- Phase template :

Within a real filter, all the frequencies are not transmitted at the same velocity. A non-constant phase shift results (and therefore a distortion) between the output signal and the filter input signal. The phase response curve of a filter is the phase shift curve due to this filter, in terms of the frequency. As with the amplitude response curve, it must be within a phase template, sort of graphical representation of the "phase - frequency" limiting conditions of the filter.

- Group delay curve :

As a consequence of what we have seen above, the group delay concept is preferred to that of propagation velocity of each of the frequencies of a spectrum. We shall thus no longer speak of the propagation velocity for a given frequency, but for a group of frequencies. This group delay is related to the phase shift by the following relationship :

$$t = \frac{d\,\Phi}{d\,\omega}$$

with ω = pulsation.

We may infer from this relationship that the steeper the slope of the phase response curve in terms of the frequency, and therefore the more abrupt the filter cut-off, the greater the group delay of a filter will be :

Note : On the group delay curve of the different filters shown below (see 3.D), the value to read on the y-axis corresponds to a normalized group delay ω_c . T equal to T_o, that is an actual group delay expressed in seconds equal to : $T = T_o/\omega_c$, with ω_c = cut-off pulsation of the filter.

- Other parameters :
- pulse and step responses :

The pulse response of a filter is its response to a DIRAC pulse. It can be shown that :

- x(t) any type of signal : $y(t) = h(t) \ast x(t)$ with $\ast$ - convolution product
  $\rightarrow Y(p) = H(p) \cdot X(p)$ with H(p) - transfer function
- x(t) DIRAC pulse (δ (t)) : $y\,\delta(t) = h(t) \ast (t)$
  $\rightarrow Y\,\delta(p) = H(p)$

The pulse response y (t) of a filter is the time representation of its transfer function H(p). It is an intrinsic feature of the filter. It contains all the information relative to the response of the filter to any type of signal.

The step response of a filter is its response to a HEAVISIDE step (unit step). On figure 2, we can see the concept of filter settling time. In effect, if a signal having a spectrum within the filter passband is applied to the filter, the settling time is equal to the time elapsed between the time the signal was applied at the filter input and the output signal obtained, to within a given percentage of the final value (1%). This settling time is closely related to the width (B) of the filter passband (1/B for a bandpass, 1/2B for a low-pass).

- dynamics.

The dynamics of a filter is the ratio between the maximum level of the output signal and its minimum level, that is, the noise level. It is expressed in dB.

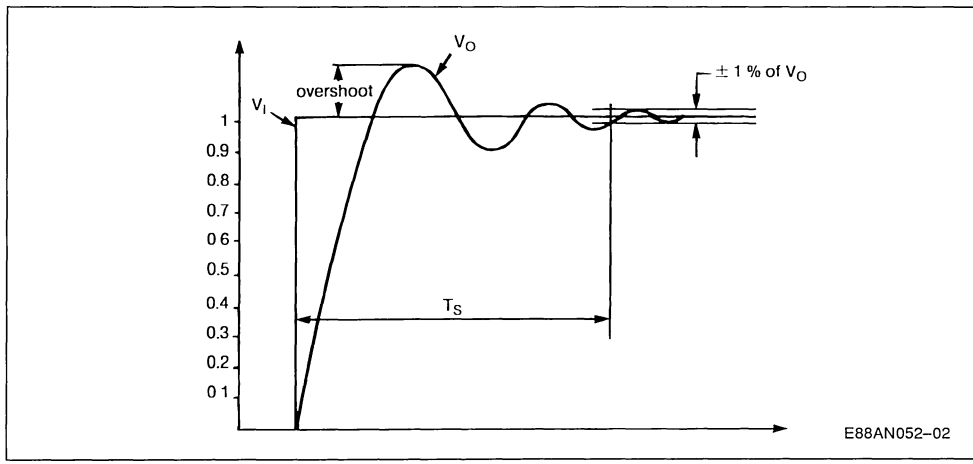
- noise factor.

The noise factor is the ratio between the total filter output noise power and the output noise power due only to the noise applied at the input. It is expressed in dB. For a given structure, the filter output noise mainly depends on the amplitude template, since it is an exponential function of the overvoltage factor Q (see 3.C). In the active filters, the noise is not "white", or at least not throughout the band considered. It is therefore necessary to split this band up into several frequency areas, and to define the corresponding noise features for each of them. We may then speak of a noise power (or voltage) per Hertz (or Hertz square root), for a given frequency (nW/Hz or nV/$\sqrt{Hz}$). The noise optimization of a filter is not always easy, and this could be kept in mind at system specifications definition time, especially for filters requiring high dynamics (60dB).

- type of signals to be filtered :

Although this may seem obvious, it is not useless to remind the importance of knowing accurately the type of signal to filter, before defining the system specifications of the filter. The signal amplitude curve must be studied in detail (regarding the compatibility with the authorized filter input swing), as well as its frequency spectrum, in order to suppress the possible interaction of undesired frequencies (50Hz, various harmonic components,...) during system specifications definition time.

Figure 2 : Settling Time (t_s) of the Step Response of a Unit Step (v_I).



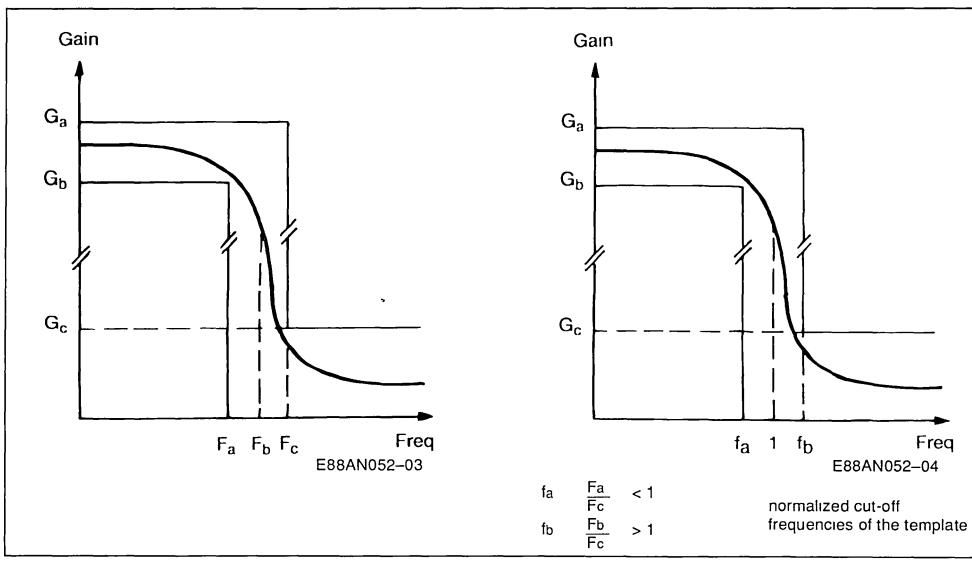
PROTOTYPE LOW-PASS FILTER

- Frequency standardization :

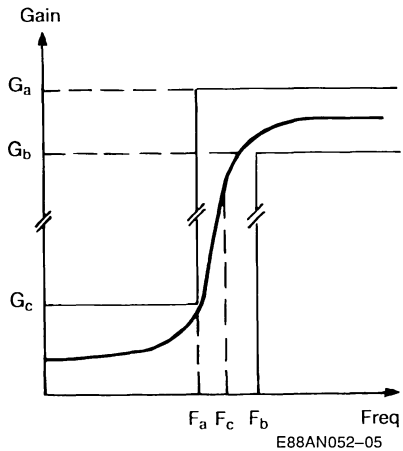
By standardizing the frequency units, the template of any filter may be related back to an template for which only the frequency ratios intervene.

Examples :

- low-pass :



- High-pass :



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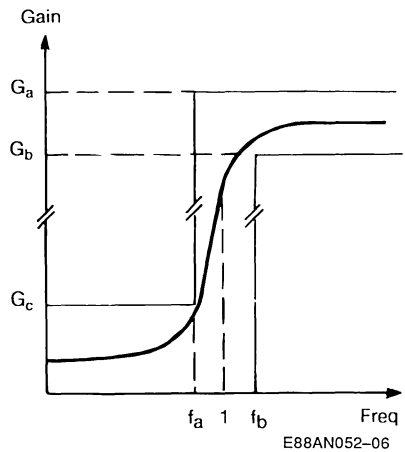
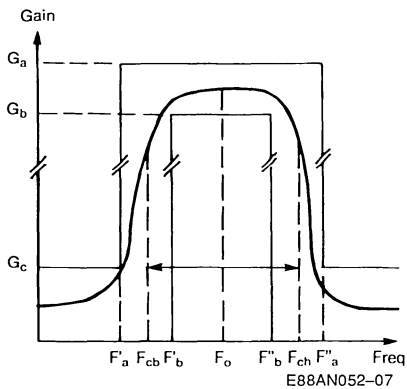


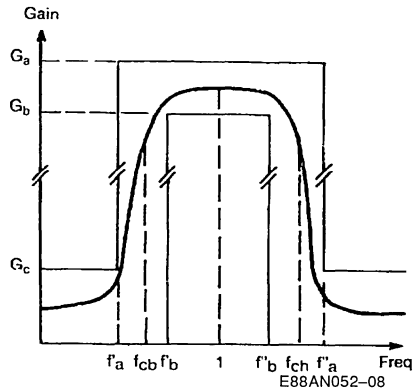
E88AN052–06

Same relationships as above

- Bandpass :



E88AN052–07



E88AN052–08

Fo $\sqrt{Fcb \cdot Fch}$ characteristic frequency

B Fch – Fcb passband

$\Delta \quad \frac{B}{Fo}$ relative band

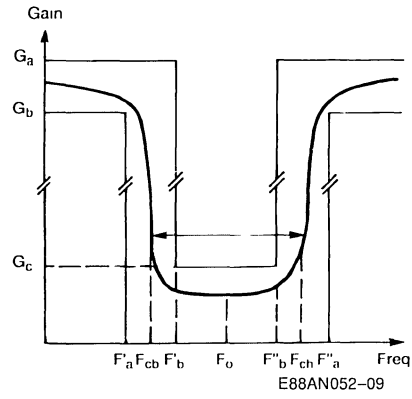
k $\frac{F"b - F'b}{F"a - F'a}$ selectivity factor

$f'a = \frac{F'a}{Fo} < 1$ $\qquad f"a = \frac{F"a}{Fo} > 1$

$fcb = \frac{Fcb}{Fo} < 1$ $\qquad fch = \frac{Fch}{Fo} > 1$

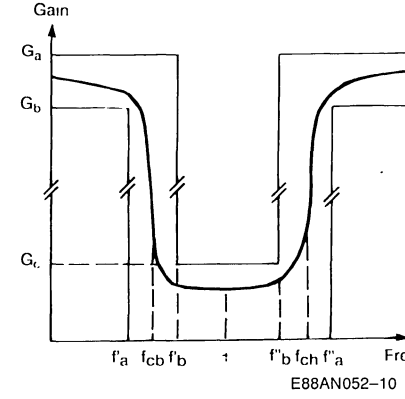
$f'b = \frac{F'b}{Fo} < 1$ $\qquad f"b = \frac{F"b}{Fo} > 1$

- notch :



E88AN052–09

Same relationships as above



E88AN052–10

Same relationships as above

- Prototype low-pass filter :

Once the standardizations above have been performed, some transformations allow the high-pass, bandpass and notch filter template to relate back to that of a so-called "prototype" low-pass filter. These frequency transformations are as follows :

- low-pass → high-pass.

It consists in replacing p by 1/p in the low-pass filter transfer function. Thus, conversion from the low-pass template to the high-pass template is performed in the following way:

$f_a \rightarrow f'_a \; 1/f_a$

$f_b \rightarrow f'_b \; 1/f_b$

- low-pass → bandpass :

It consists in replacing p by $\frac{1}{\Delta}(p + 1/p)$ in the low-pass filter transfer function. Thus, conversion from the low-pass template to the bandpass template is performed in the following way :

$f_{cb}\ f_{ch}\ f'_a\ f''_a\ f'_b\ f''_b\ 1$

- low-pass → notch filter :

It consists in replacing p by $\frac{1}{\frac{1}{\Delta} \cdot (p + 1/p)}$

in the low-pass filter transfer function. Thus, conversion from the low-pass template to the notch filter template is performed in the following way :

$f_{cb}\ f_{ch}\ f'_a\ f''_a\ f'_b\ f''_b\ 1$

Therefore, in the remaining parts of this notice, all the calculations and examples will be related back to a (prototype) frequency-standardized low-pass filter template, since conversion to the template of any other type of filter can be obtained using the transformations above.

FILTER TRANSFER FUNCTION :

- General definitions :

The transfer function is the mathematical representation of the filter amplitude response curve. It is an obligatory intermediate, allowing the calculations of the different filter factors to be carried out. It is expressed as a ratio between the output level and the input level of the filter, in terms of the frequency. This ratio may be expressed as a function of the complex variable p :

$$H(p) = K\frac{N(p)}{D(p)} \qquad (1)$$

with N(p) and D(p) : p polynomials.

This expression may therefore be written in the following way :

$$H(p) = K\frac{a_m \cdot p^m + \ldots\ldots + a_1 \cdot p + a_0}{b_n \cdot p^n + \ldots\ldots + b_1 \cdot p + b_0} \qquad (2)$$

In this form, the order of the filter is defined as being equal to the degree of the denominator D(p) (in this case, n). The stability criterium for a filter dictates that the degree of D(p) (the order of the filter) be greater or equal to the degree of N(p). On the other hand, the higher the order of a filter, the more abrupt its cut-off, as can be seen on the relationship providing the asymptotic slope of a filter at the cut-off, in terms of its order :

P 6.n (dB per octave)

We may also express the transfer function in another way, by replacing the coefficients $a_o,..., a_m$, $b_o,..., b_n$ by the roots $z_1,..., z_m$; $p_1,..., p_n$ of the N(p) and D(p) polynomials :

$$H(p) = K\frac{(p-z_1).....(p-z_m)}{(p-p_1).....(p-p_n)} \quad (3)$$

The zeros of the transfer function are the $Z_1,..., Z_m$ constants and the poles are the $P_1, ..., P_n$ constants

These constants are either real or imaginary conjugated.

It can be shown that if n is even, the poles of H(p) are all imaginary conjugated, two by two, and that if n is odd there is a single negative real root. D(p) may therefore be written in the form of a product of 2nd order factors if n is even, and in the form of a product of 2nd order factors and of a 1st order factor, if n is odd. A new expression can then be obtained for the transfer function :

$$H(p) = K\frac{(p-z_1).....(p-z_m)}{(p-p_o).(p^2+2.\delta 1.p+\rho_1^2).....(p^2+2.\delta\ k.p.\rho_1^2)} \quad (4)$$

with $K = \frac{n-1}{2}$ if n is odd, and $k = \frac{n}{2}$ and without $(p-p_o)$ if is even

It can then be shown that any filter can be obtained by cascading 2nd order cells if n is even, or 2nd order cells and one 1st order cell if n is odd.

- General transfer function for a 1st order cell :

It may be expressed as :

$$H(p) = K\frac{N(p)}{1+a.p}$$

with

- p complex pulsation
- a time constant

This last parameter allows the cut-off pulsation (and therefore the cut-off frequency) of the cell to be defined as its reciprocal
($\omega c = 1/a$ and $F_c = 1/(2 . \pi . a)$).

a is a time value such that 3.a (5.a) characterises the time after which the response has reached 95% (99%) of its final value.

Note : The expression of N(p) depends on the type of filter considered :

- polynomial low-pass filter : N(p) = 1
- polynomial high-pass filter : N(p) = p/a (with $p \rightarrow 1/p$)

- General transfer function for a 2nd order cell :

It may be written as follows :

$$H(p) = K\frac{N(p)}{1+2.\xi.p/\omega_o+p^2/\omega_o^2}$$

with :

- p : complex pulsation
- K : passband transfer factor

- For Low-pass and high-pass cells :

The relationship above allows the following parameters to be defined :

- the undamped natural pulsation ω_o (or characteristic pulsation) used as a standardization pulsation (F_o : characteristic frequency).
- the damping factor ξ , magnitude without units specifying the shape of the filter responses :

if $\xi < 0.707$ distinct, transient, ωp pulsation oscillations for the unit response ; resonance on the frequency response,

if $0.707 < \xi < 1$ not very distinct, transient oscillations.; the final value of the unit response is overstepped. No resonance on the frequency response,

if $\xi = 1$ damping factor critical value,

if $\xi > 1$ no oscillation, a periodic response without overstepping the final value of the unit response.

- the natural pulsation of the filter $\omega\rho = \omega_o . \sqrt{1-\xi^2}$ characterising the pulsation of the filter transient oscillations,
- the resonance pulsation $\omega_r = \omega_o . \sqrt{1-2.^2}$, specifying the resonance position,
- the overvoltage or resonance factor

$$Q = \frac{|H(j\omega r)|}{|H(O)|} = \frac{\sqrt{1}}{2 \cdot \xi \sqrt{1-\xi^2}}$$

specifying the value of the gain of the filter for the resonance pulsation.

- the relative band Δ related to the overvoltage factor by the relationship

$$Q = \frac{1}{\Delta}$$

Note : The expression of N(p) depends on the type of filter considered :

- polynomial low-pass filter : N(p) = 1

- polynomial high-pass filter : $N(p) = p^2 / \omega^2$
- low-pass elliptic filter : $N(p) = p^2 + \omega_\infty^2$ with $\omega_\infty > \omega_o$
- high-pass elliptic filter : $N(p) = p^2 + \omega_\infty^2$ with $\omega_\infty > \omega_o$
- bandpass and notch filter cells :

The relationships above are slightly different for a bandpass and notch filter, 2nd order cell. In this case:

- $Fo = \sqrt{F_{CB} . F_{CH}}$ with F_{cb} and F_{ch} : low and high cut-off frequencies of the cell.
- $Q\ F_o / \Delta F$ with $\Delta F = F_{ch} - F_{cb}$, called relative band.

We may infer from this relationship :

$$Q = \frac{F_{ch} - F_{cb}}{F_o}$$

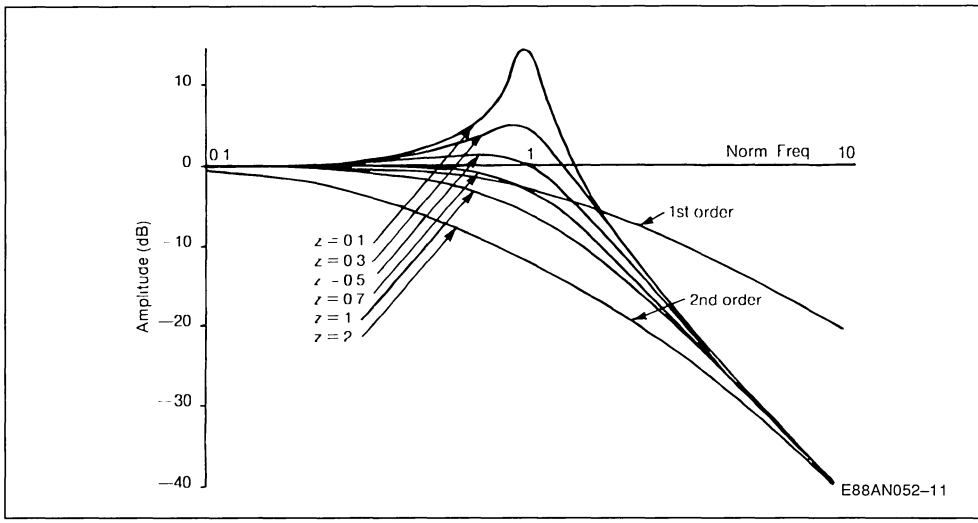
Note : The expression of N(p) depends on the type of filter considered :

- bandpass filter $N(p) = 2 . \xi . P/\omega_o$
- notch filter $N(p) = p^2 + \omega^2$

- Conclusion

Figure 3 shows the shapes of the amplitude response curves of the 1st and 2nd order low-pass cells, for different values of ξ . Let us keep in mind that a 2nd order filter presenting interesting features is obtained for ξ 0.707. In effect, the transient oscillations and the resonance (Q = 1) no longer appear, and the frequency response presents a passband equal to the value $F_o\ \omega_o/(2 . \pi)$.

Figure 3 : Amplitude Response Curves of a 1st and a 2nd Order Low Pass Cells in Terms of the Damping Factor (called Z on this figure).



CHARACTERISTIC FUNCTIONS

The major problem when designing a filter consists in factorising N(p) and D(p), in order to write the transfer function in the form shown on expression 4. To simplify the calculations, it is often preferrable to start from the template considered and to try to have a well known characteristic function pass within it. As there are a great number of functions that may be inscribed within a given template, the selection of one of them will depend on the following features :

- it must be possible to synthesize it
- it must be possible to split it up into a product (or an addition) of functions, and it must be possible to carry each one out
- it must comply with the filter system specifications (phase, group delay,...)

The filter designer must therefore optimize his selection, taking into account all these constraints. A relatively great number of well known characteristic functions simplifies this task.

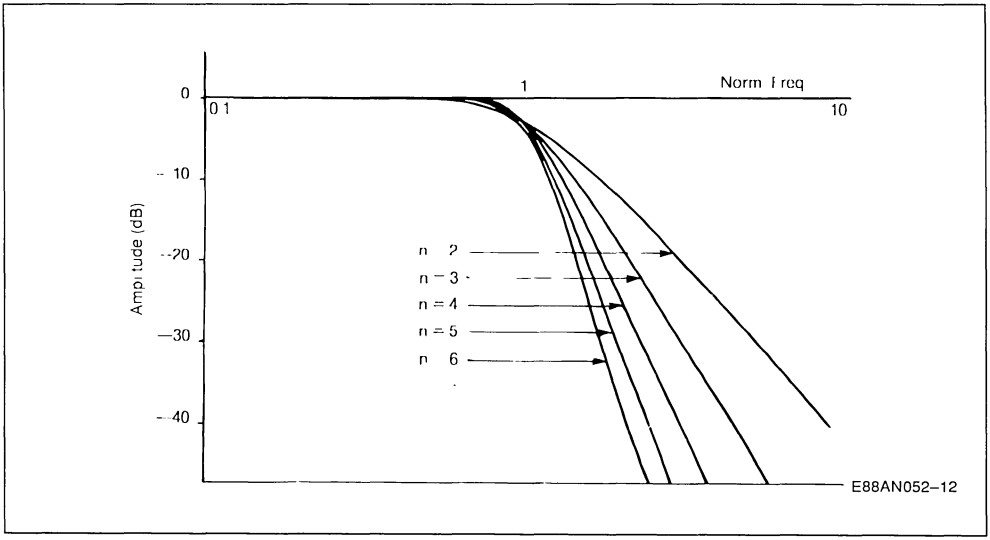
- Low-pass polynomial filters :

Their transfer functions comply with N(p) 1. The following are the most often used :

- BUTTERWORTH filters :

They correspond to amplitude response curves with the following features (figure 4).

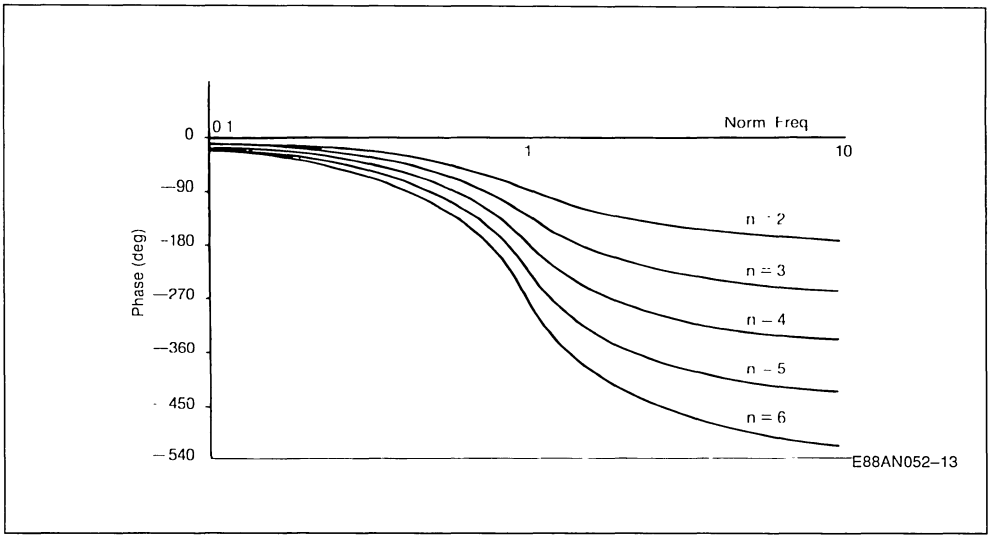
Figure 4 : Amplitude Response Curves of the Butterworth Low Pass Filters.



- no ripple within the passband
- not very rapid cut-off near the cut-off frequency.

The phase response curves of these filters present relatively small phase rotations (figure 5).

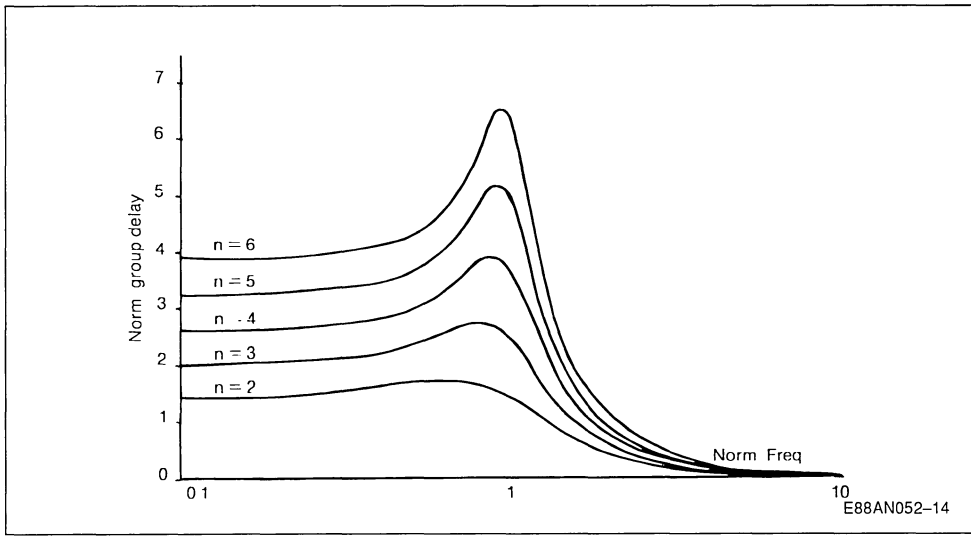
Figure 5 : Phase Response Curves of the Butterworth Low Pass Filters.



The group delays are relatively constant within the passband and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/2 (figure 6).

Note : The higher the order n of the filter, the closer the amplitude response curve will be to the ideal curve (rectangular template)

Figure 6 : Group Delay Curves of the Butterworth Low Pass Filters.

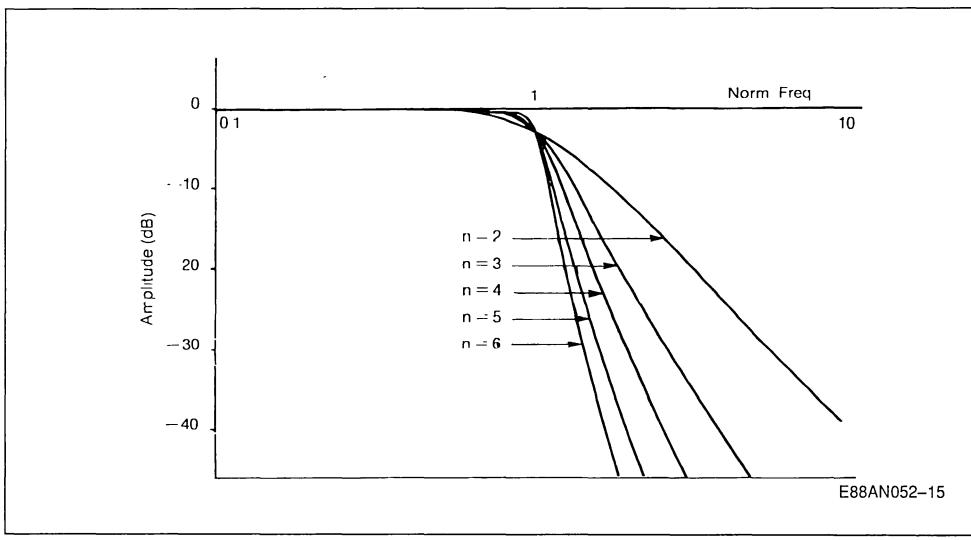


- LEGENDRE filters :

They correspond to amplitude response curves having the following features (figure 7) :

- cut-off as rapid as possible near the cut-off frequency
- regular attenuation within the stopband

Figure 7 : Amplitude Response Curves of the Legendre Low Pass Filters.



The phase response curves are practically identical to those of a BUTTERWORTH filter (figure 8). Regarding the group delays for a given order, they are relatively constant within the passband, and their ratio with the group delays for the frequencies around the cut-off frequency is equal to 1/2 (figure 9). But since the slopes of these curves are very steep for this frequency, these time are in general higher than those of the BUTTERWORTH filters.

Figure 8 : Phase Response Curves of the Legendre Low Pass Filters.

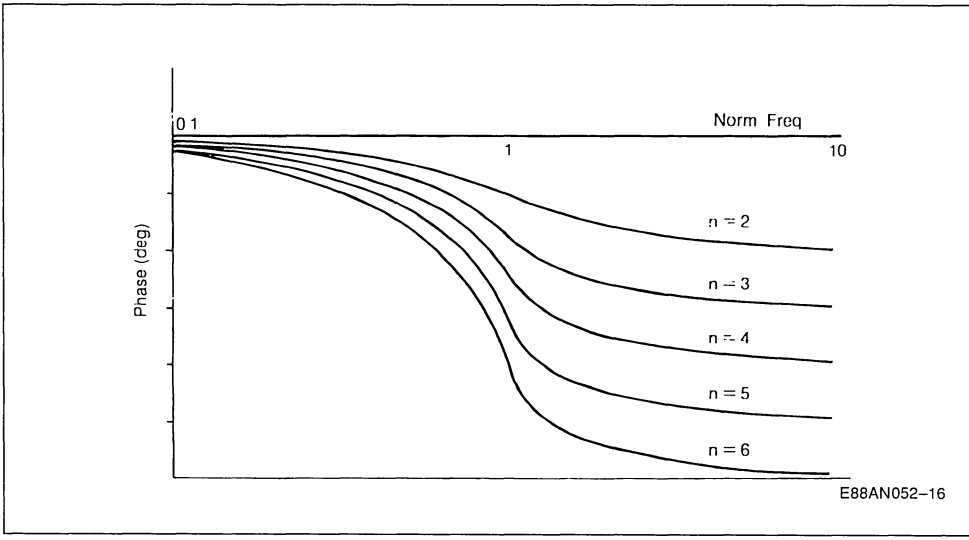
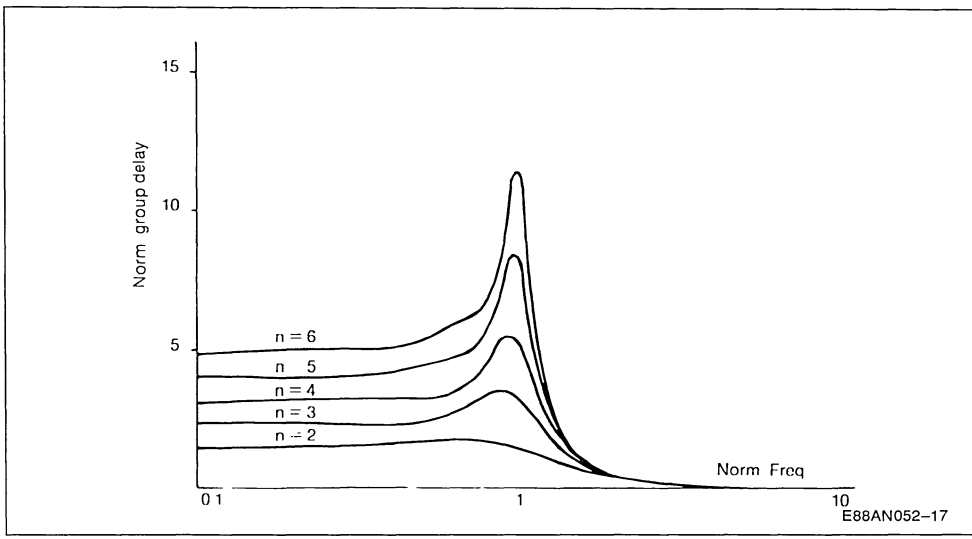


Figure 9 : Group Delay Curves of the Legendre Low Pass Filters.

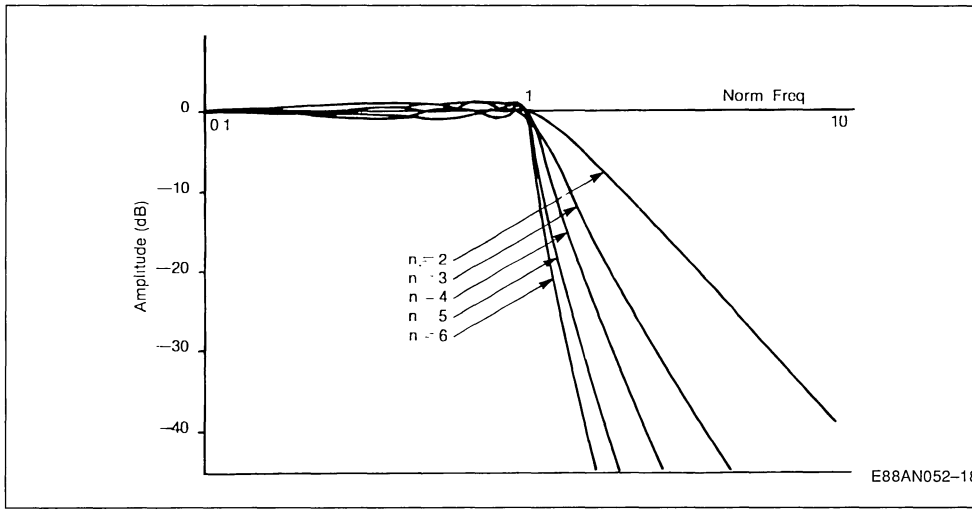


- - CHEBYCHEV filters

They correspond to amplitude response curves presenting the following features (figure 10).

- - ripples within the passband (up to 2dB)
- - rapid cut-off near the cut-off frequency (at least in the first octave)

Figure 10 : Amplitude Response Curves of the Chebychev Low Pass Filters.



The phase response curves present greater rotations than those of the BUTTERWORTH filters (figure 11). The group delays within the passband are not identical for a given order, and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/3 (figure 12).

Note : The order of a CHEBYCHEV filter is equal to the number of extrema of the amplitude response curves located within the passband.

Figure 11 : Phase Response Curves of the Chebychev Low Pass Filters.

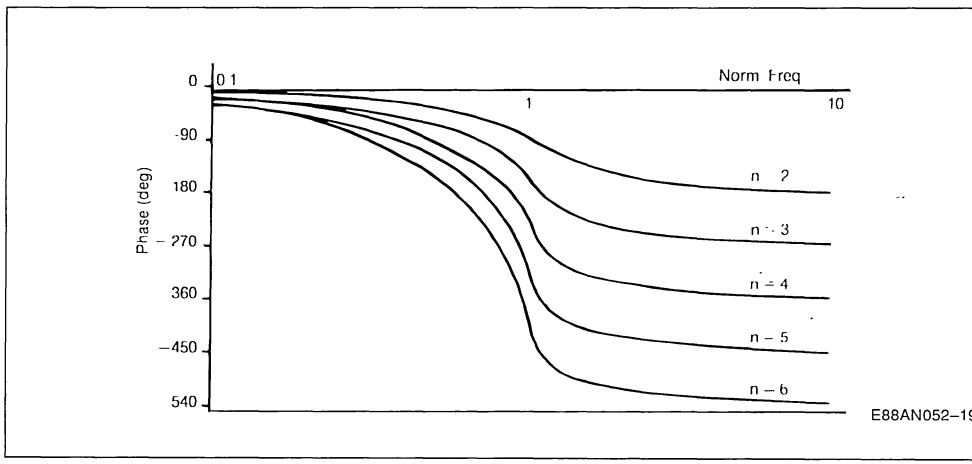
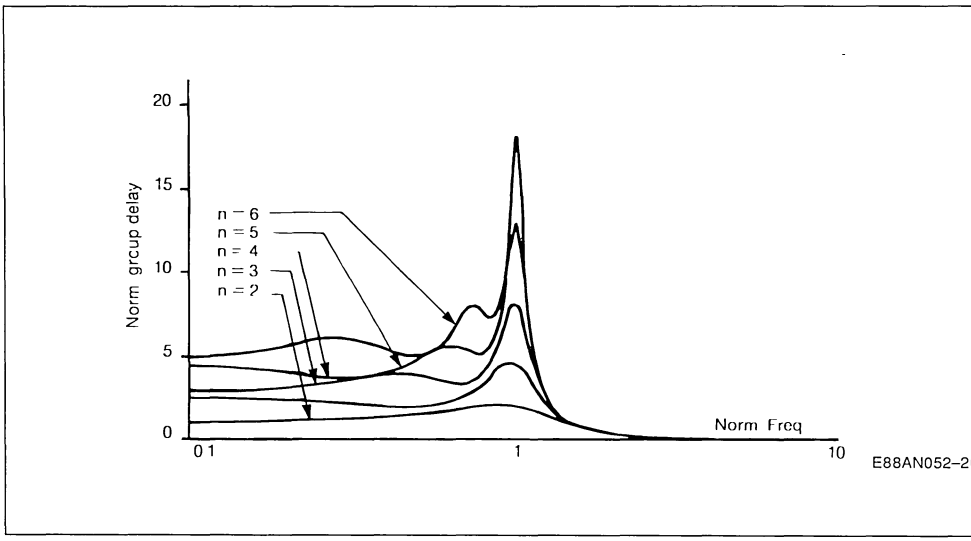


Figure 12 : Group delay Curves of the Chebychev Low Pass Filters.

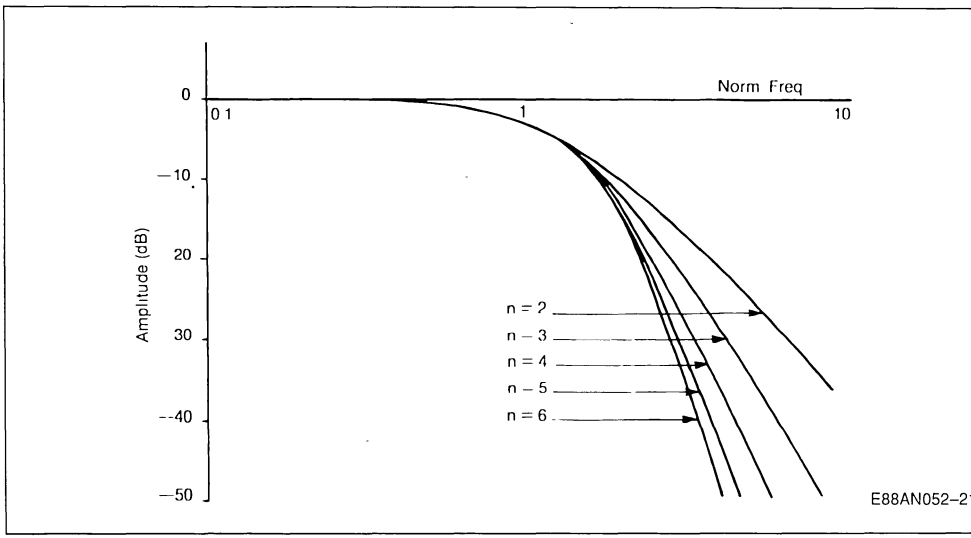


- BESSEL filters

They correspond to amplitude response curves presenting the following features (figure 13) :

- very slow cut-off near the cut-off frequency
- small attenuation within the stopband

Figure 13 : Amplitude Responses Curves of the Bessel Low Pass Filters.



The phase response curves are practically identical to those of the BUTTERWORTH filters (figure 14). These filters are mainly interesting because of their group delays, strictly constant within the passband until beyond the cut-off frequency (figure 15). They therefore have a very close to a pure delay characteristic, and they must be used in all applications for which the non-distortion of the signal is an essential factor.

Figure 14 : Phase Response Curves of the Bessel Low Pass Filters.

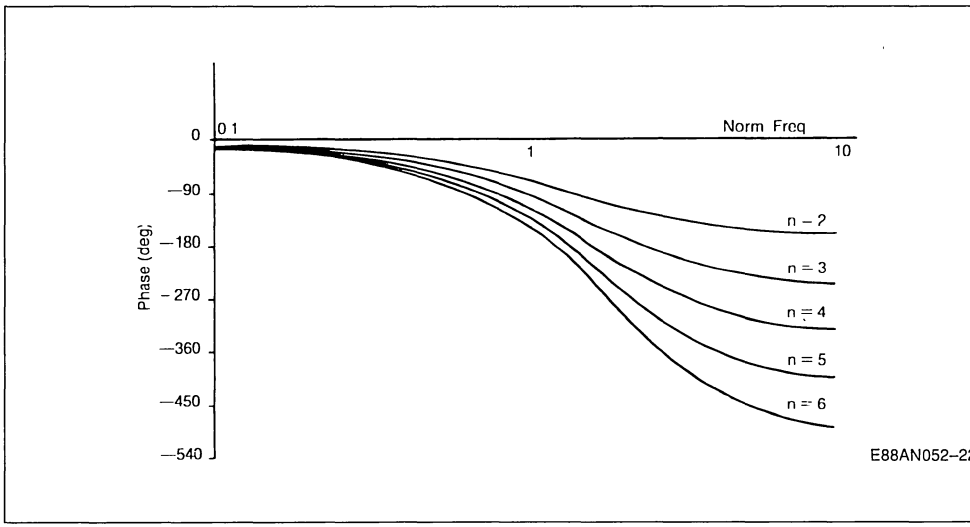
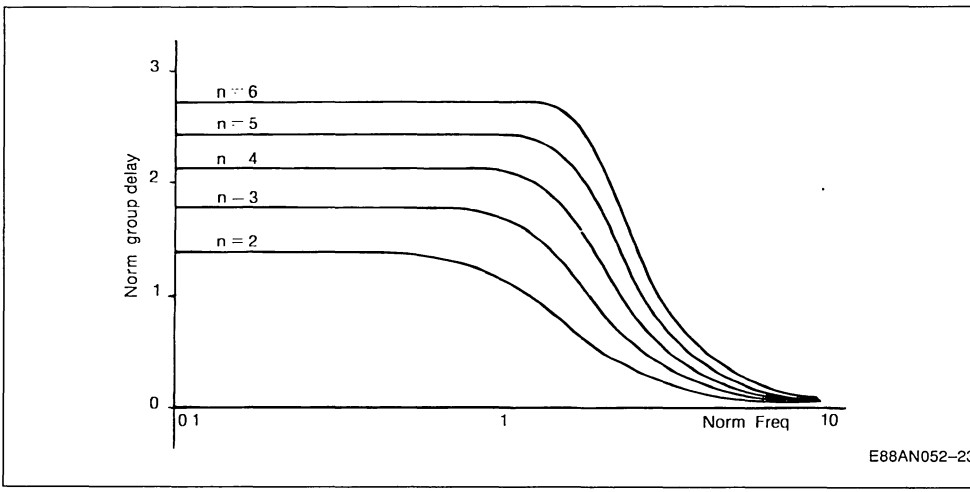


Figure 15 : Group Delay Curves of the Bessel Low Pass Filters.



- Low-pass elliptic filters :

Their transfer functions are such that N(p) may be expressed in the following way :

$$N(p) = (p^2 + \omega_1^2).....(p^2 + \omega_k^2) \text{ with } \begin{cases} k = \dfrac{n}{2} \text{ if n is even} \\ k = \dfrac{n-1}{2} \text{ if n is odd} \end{cases}$$

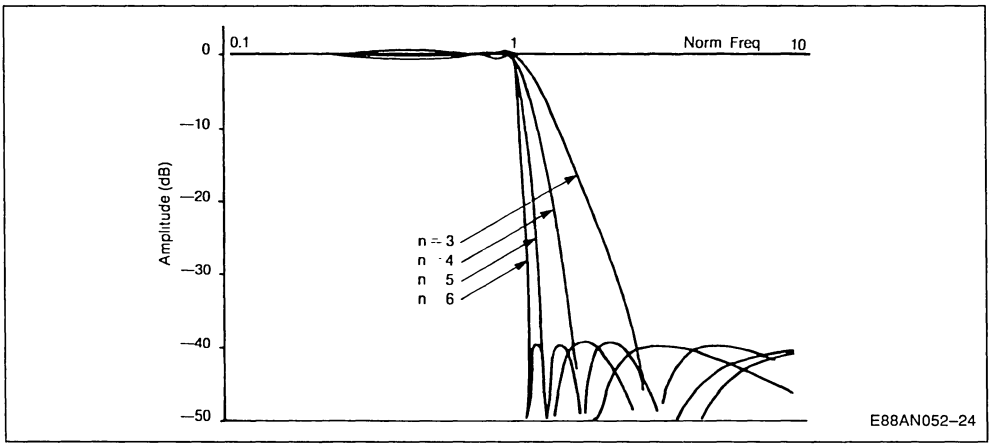
and ω_1, ..., ω_k : transmission zeros.

- CAUER filters :

They correspond to amplitude response curves presenting the following features (figure 16).

- ripples within the passband
- very rapid cut-off near the cut-off frequency
- presence of one or several transmission zeros (N(p) roots)

Figure 16 : Amplitude Response Curves of the Cauer Low Pass Filters.



The phase response curves have greater rotations than the CHEBYCHEV filter ones (figure 17).

The group delays are very different for a given order, from one area of the passband to another, and their ratio with the group delays of the frequencies around the cut-off frequency is equal to 1/10 (figure 18).

Figure 17 : Phase Response Curves of the Cauer Low Pass Filters.

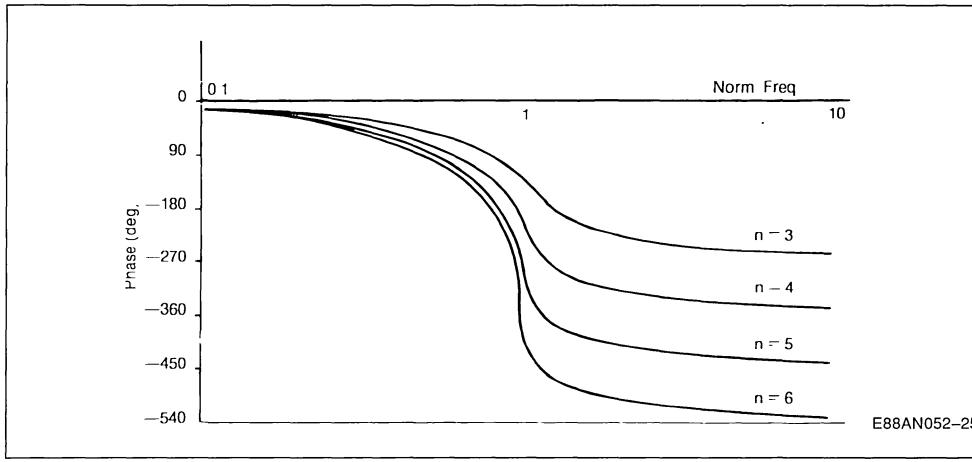
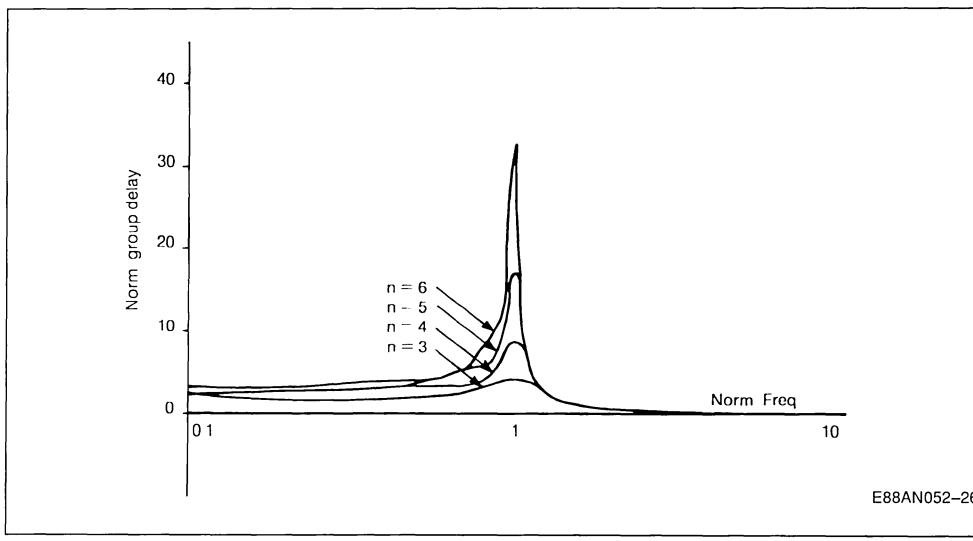


Figure 18 : Group Delay Curves of the Cauer Low Pass Filters.



- Conclusion :

A number of nomographs, tables and curves provide, for each type of function and according to its order, the amplitude response curves, the phase response curves, the group delay curves, and also the pulse and step responses. All these characteristics, and a few others, are summarized in the table on figure 19.

Regarding our subject, we will keep in mind the following :

- The BUTTERWORTH filters are interesting because of the regularity of their passband (no ripple) but their cut-off is not very abrupt
- The LEGENDRE filters associate a convenient regularity of the amplitude response curve with a cut-off abruptness and a transient behaviour that are of good quality
- The CHEBYCHEV filters present, at least within the first octave, an abrupt cut-off, but their transient behaviour is not very performing
- The BESSEL filters present a very good transient behaviour, but their cut-off is not very abrupt
- The CAUER filters allow an extremely abrupt cut-off be obtained, but their group delay regularity is mediocre. They present transmission zeros.

Figure 19: Comparison between the Performances of the Different Kinds of Filters.

Kind of Performance	Kind of Filter				
	Butterworth	Legendre	Chebychev	Bessel	Cauer
Cut-off Abruptness for a Given Order	● ●	●	■ ■	● ● ●	■ ■ ■
Regularity of the Amplitude Response Curve	■ ■ ■	■ ■	Ripple within the Passband/ regular within the Notch	■ ■	Ripple within the Passband and the Notch
Regularity of the Group Delay	■	●	● ●	■ ■ ■	● ● ●
Sensitivity	■ ■	■ ■	●	■ ■	● ●
Transient Condition Distortions	■ ■	■ ■	● ●	■ ■ ■	● ● ●
Transmission Zeros	None	None	None	None	Yes
Required Overvoltage Factors	Very Low	Low	Medium	Medium	High

● ● ● : Very Mediocre
● ● : Mediocre
● : Medium

■ ■ ■ : Excellent
■ ■ : Very Good
■ : Good

SOME IDEAS CONCERNING FILTERS DESIGN

We will assume for the following that the future designer has a comprehensive knowledge of the system specifications of the filter required for this application. We will show briefly how, starting from these system specifications, he may design the filter required. Since this study is beyond the scope of his application specification, this approach will necessarily be very brief.

The design of a filter is performed in four steps :

- determining the characteristic parameters of the filter
- selecting the type of filter
- calculating the filter transfer function
- filter synthesis

A. DETERMINING THE CHARACTERISTIC PARAMETERS OF THE FILTER :

From the amplitude template related back to the prototype filter template (standardized low-pass), the following parameters are assumed to be known :

- G_a. maximum gain within the passband
- G_b. maximum attenuation within the passband
- G_c. minimum attenuation within the stopband
- k selectivity
- Δ relative band (only for the bandpass and the notch filters)

The knowledge of these parameters will allow the complete design of the filter to be performed.

B. SELECTING THE TYPE OF FILTER :

We have seen the different features of the BUTTERWORTH, LEGENDRE, CHEBYCHEV, BESSEL and CAUER filters. Let us keep in mind that the main criteria used for selecting a given type of filter are the following :

- the cut-off abruptness
- the passband regularity
- the group delay regularity
- the existence of transmission zeros
- the behaviour under transient conditions

C. CALCULATING THE FILTER TRANSFER FUNCTION :

Let us assume that the type of filter is known. We must now determine its transfer function. Three steps are required to this end :

a) determining the degree of this function :

The desired amplitude template is related back to the prototype filter template (standardized low-pass) ; by placing the different response curves of the above filters within this template, we obtain not only a type of filter but also its order, and thereby the degree of the corresponding transfer function.

b) determining the transfer function of the prototype filter :

Depending on the different values of the parameters of the prototype amplitude template desired, a number of nomographs and tables allow the calculation of the transfer function corresponding to this template to be carried out.

c) transposing the transfer function :

If the filter to be designed is not a low-pass (high-pass, bandpass, notch filter), the transfer function determined above may be transposed to the corresponding transfer function, using the transformations defined above.

D. FILTER SYNTHESIS :

It mainly consists in factorising the final transfer function in the form of a product of 1st and 2nd degree factors. The desired filter may then be easily designed, by cascading the 1st and 2nd order elementary filters corresponding to each of these factors.

CONCLUSION :

In most - not to say all - electronic applications, the filtering portion has become one of the most important. We have found that it also was the least well known. By defining all the parameters specified in the system specifications of a filter, and by providing a selection guide amongst the different existing types, we offer anybody who whishes to do so the possibility of making up for lost time, and seeing how this may be inserted into his general application.

IMPLEMENTATION AND APPLICATIONS AROUND STANDARD MPF

INTRODUCTION

At a time when increased miniaturisation is the vogue, the problems posed by the filtering of electrical parameters are on an upward trend. The increase in filter order, progressively improved performances mean generally that in order to solve these problems, a considerable increase in components (also generally their size) has to be used. The adjustments in consequence become also more difficult to effect.

In this gloomy context, the advent of switched capacitor techniques has considerably widened the scope of classical filters. Not content to rest here, SGS–THOMSON Microelectronics goes even further and offers an even new concept in filtering : the M.P.F. (Mask Programmable Filter).

This application note has therefore several objectives : to explain the switched capacitor principle (application, advantages), to describe the M.P.F. general circuit (structure, block diagram, principal characteristics), to present the SGS–THOMSON approach (standard, custom) and to finish by a quick description of all the possible applications of the M.P.F. and more specially one amongst them : the frequency detection.

THE SWITCHED CAPACITOR

PRINCIPLE :

Consider figure 1. When the switch is in position 1, the charge at the capacitor terminals is $Q1 = C \times V1$. If the switch is now moved in position 2, the charge at the terminals of C becomes $Q2 = C \times V2$. This switching allows a charge transfer $Q = Q2 - Q1 = C \times (V_2 - V_1) = C \times \Delta V$ between the points 1 and 2 of the circuit.

This charge transfer in equivalent to the flow of a current $I = \Delta Q/T = \Delta Q \times F = C \times \Delta V \times F$ where F is the commutating frequency of the switch. ($F = 1/T$)

If we compare now the previous expression with Ohm law applied to a resistance ($I = \Delta V/R$), then we can deduce an electrical equivalence between the resistor and the switched capacitor :

$$R = \frac{1}{C \times F}$$

The technique of switched capacitors enables us therefore to simulate resistors with capacitors. Additionnally, the values of these resistors vary with the sampling frequency employed. These two key points offer considerable advantages to this technique.

This relationship leads to an important comment. In effect, the equivalence "transfered charge = discrete quantity of current" is only valid for high switching speeds. This is certainly the case for switched capacitor filters where, in order to avoid aliasing and smoothing problems inherent in all sampling systems, relatively high sampling frequencies are used, sufficiently high, in any case, for the previous relationship to remain valid.

EXAMPLE OF THE APPLICATION WITH AN INTEGRATOR :

In order to understand the operation of a switched capacitor integrator, consider the case of a standard inverting integrator as shown in figure 2.

Remember that the time constant of this circuit (= R x C') determines, in active filter circuits, parameters such as bandwith and cut-off frequency.

However, in this example, this time constant presents a major obstacle : the total lack of correlation between the values of R and C'. The eventual variations or drifts of these two values not necessarily moving in the same direction, leads to a relatively high and difficult to handle innacuracy when associated with the values mentioned above.

Consider now the switched capacitor integrator shown in figure 3. According to the equivalence previously mentioned, the time constant of this integrator is equal to :

$$\tau = \frac{C'}{C \times F}$$

Figure 1 : Principle of the Switched Capacitor.
1 : C produces the charge $Q_1 = C \times V_1$
2 : C produces the charge $Q_2 = C \times V_2$

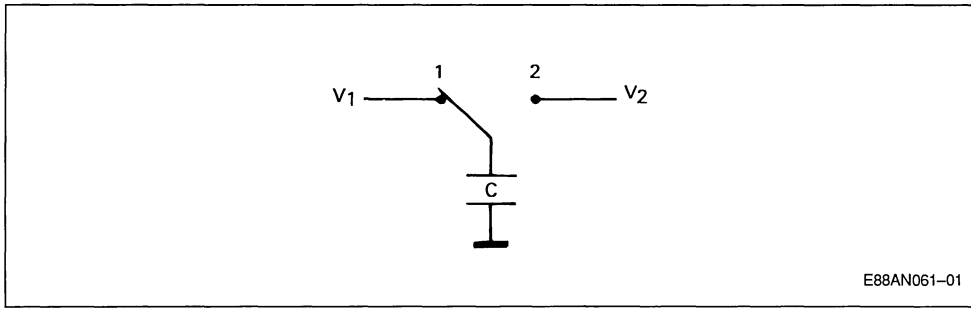


Figure 2 : Standard Inverting Integrator ($\tau = R \times C'$).

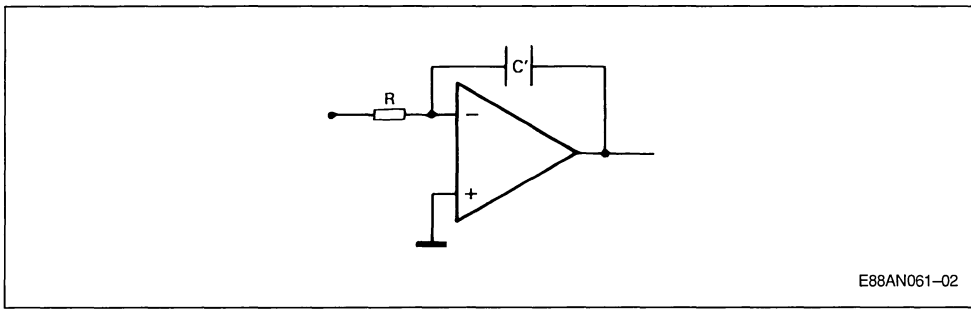
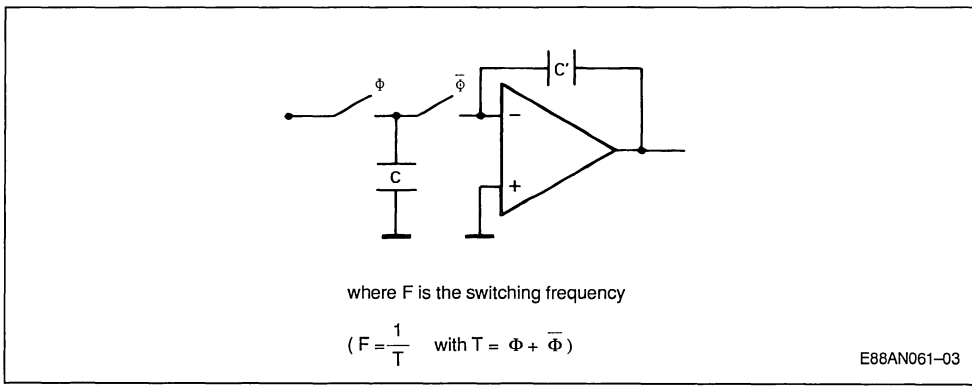


Figure 3 : Switched Capacitor Inverting Integrator ($\tau = \frac{C'}{C \times F}$).



Then, we show in a standard integrator, accuracy depends upon the absolute values of the components, when in a switched capacitor integrator, only the relative values are considered.

ADVANTAGES OF THE SWITCHED CAPACITOR TECHNIQUE :

The preceeding result shows three major advantages.

The first concerns the relative ease with which an MOS technology can supply excellent precision of capacitor ratio (0.1%). Also, since it is not difficult to obtain good sampling frequency accuracy, the accuracy of the global time constant can attain, with the switched capacitor technique and no external adjustments, values better than 0.5%. It is this precision that we find over the complete frequency range of M.P.F.

The second advantage concerns the equivalence "resistance = switched capacitor" and the possibility offered by this relationship of being able to integrate, in MOS technology, high values of resistance on a small surface area.

Finally, the use of a clock offers considerable scope for modification of the time constant by simple sampling frequency adjustment. Since this time constant is proportional to the cut-off frequency, we can deduce that a constant ratio exists between the sampling frequency and the cutt-off frequency of the M.P.F. It is possible therefore, using this technique, to offset the cut-off frequency of the M.P.F. by simply modifying the sampling frequency. This last point highlights the extreme flexibility of use of the M.P.F. Other advantages of equal importance such as the almost total absence of external components, low power consumption, no adjustment and high temperature stability confer on the M.P.F. extreme flexibility of use and very high operating reliability.

THE TS85XX PRODUCT

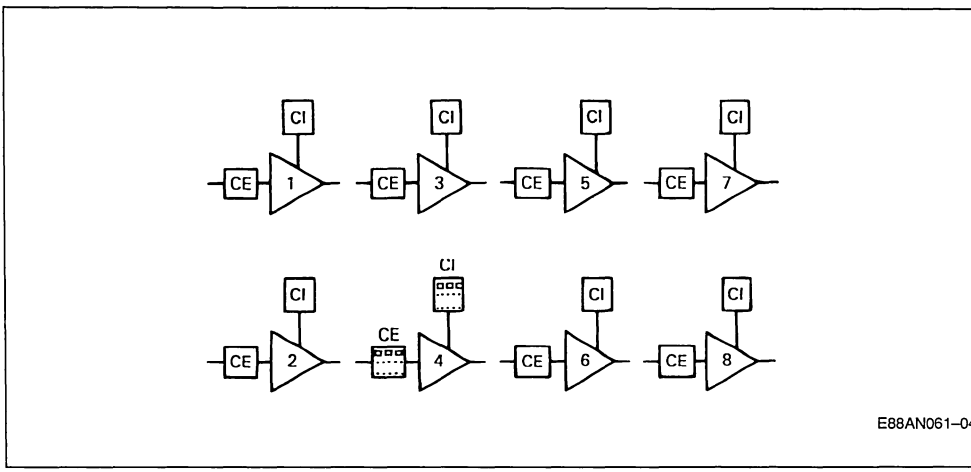
THE M.P.F. STRUCTURE :

The problems encountered now in filtering (varied requirements, prohibitive costs, long lead times) lead SGS-THOMSON to choose a pre-diffused technique where the final characterization of the filter is defined by the interconnection mask (last level of masking).

This structure, shown in figure 4, consists of 8 elementary cells each formed by a switched capacitor integrator and two capacitor areas CE and CI. Each area contains a high number of incremental capacitors each of value 0.1pF. Thus, according to the type and filter order of M.P.F. required, the integrators can be interconnected, and according to the "Gain-Frequency" response curve required, the various incremental capacitors are also interconnected. The number of incremental capacitors thus connected varies from one area to another and depends upon the different coefficients of the transfer function that the M.P.F. is required to execute.

N.B. : Generally, the number of integrators interconnected is equivalent to the filter order obtained.

Figure 4 : A filtering unit consisting of 8 elementary cells each containing a switched capacitor integrator. Each capacitance area (CI and CE) contains an optimum number of incremental capacitors of 0.1pF.

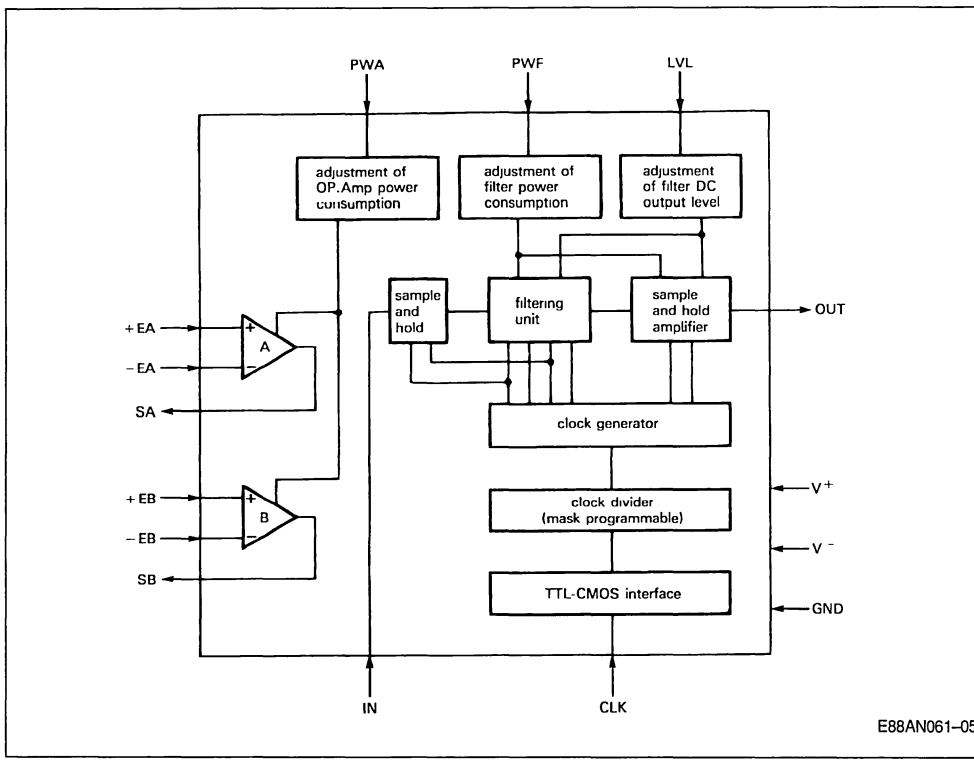


Block Diagram :

The block diagram of the M.P.F. structure utilised is shown in figure 5. The principal internal functions are :

- a filtering unit composed of 8 switched capacitor integrators interconnectable between each other at the final mask level (interconnection level),
- a clock generator producing the various phases required for the internal switching of the capacitors. These phases are imperatively non-overlapping. The internal clock is obtained via a divider, equally mask programmable, and which matches the external clock defined by the user to that of the M.P.F. As the clock input is TTL compatible, a TTL-MOS level interface is provided, within the circuit, in order to obtain the correct voltage swings,
- a sample and hold unit before the filtering unit,
- a sample and hold amplifier tied to the output of the filtering unit and which enables low impedance signals to be available at the output of the M.F.P.
- the adjustment of the DC output level of the M.P.F. by an external voltage source (for example a divider connected between the positive and the negative power supplies and whose midpoint is connected to LVL pin of the M.P.F.),
- two general purpose and independant operational amplifiers available and destined to be used by the customer for other applications associated with the M.P.F. (anti-aliasing, smoothing, comparator, oscillator,...) in association with external components (R, C, crystal),
- the adjustment of the power consumption of the filter by means of the external resistance tied between the positive supply terminal V^+ (or ground) and the corresponding pin of the circuit (PWF). The power consumption can thus be choosen to match the particular application.
- The stand-by mode is obtained by strapping pin PWF to the negative supply terminal V^-,
- the adjustment of the power consumption of the two operational amplifiers, obtainable exactly as for the previous case but via the pin PWA of the circuit.

Figure 5 : Block Diagram of the Construction Chosen by SGS–THOMSON.



Principal Characteristics :

The principal characteristics of product TS85XX are as follows :

- technology : HCMOS1 (high density linear CMOS)
- available order : 2 to 8 (whatever the type of M.P.F.)
- input signal frequency : 0 to 30kHz
- internal sampling frequency : 0.5 to 1000kHz (depends upon the M.P.F. under consideration)
- ratio between internal sampling frequency and cut-off frequency : 10 to 200 (depends upon the M.P.F. under consideration)
- response curves (amplitude and phase) translatable by changing the sampling frequency
- signal to noise ratio : 70 to 85dB (depends upon the internal construction of the M.P.F.)
- power supply : ± 5V or 0-10V
- power consumption adjustable from 0.5 to 20mW per order
- capacitor ratio tolerance : 0.1%
- cut-off frequency tolerance : 0.5% (max)

THE SGS-THOMSON APPROACH

The SGS-THOMSON approach is to produce two types of M.P.F. : custom M.F.P.'s and standard M.F.P.'s.

CUSTOM M.P.F.'s :

SGS-THOMSON undertakes to deliver the first samples within 6 to 8 weeks maximum after the definition of the overall specification by the customer. All types of filters can be designed (BUTTERWORTH, LEGENDRE, BESSEL, CHEBYCHEV, CAUER,...) according to the general applications (low-pass, high-pass, band-pass, notch, group delay time correctors) or by simultaneous optimisation of the response curve both in amplitude and in phase. A special application note on the custom M.P.F. will explain later now to define all the specifications required to design a filter and how to choose among them according to the desired application.

STANDARD M.P.F.'s :

These constitute a family, currently of 11 circuits, which will expand in the future according to the evolution of the market requirements. Here is the description of this family :

Part Number	Function	Type	Order	Clock to Cutt-off Freq. Ratio	Stopband Attenuation
TS8510	Low-pass	CAUER	5	75.3	33dB (typ)
TS8511	Low-pass	CAUER	7	75.3	55dB (typ)
TS8512	Low-pass	CAUER	7	100	85dB (typ)
TS8513	Low-pass	CHEBYCHEV	8	60	80dB (typ)
TS8514	Low-pass	BUTTERWORTH	8	80	74dB (typ)
TS8530	High-pass	CAUER	3	320	15dB (typ)
TS8531	High-pass	CAUER	6	400	32dB (typ)
TS8532	High-pass	CHEBYCHEV	6	500	60dB (typ)
TS8550	Band-pass	CAUER (Q = 5)	8	60	
TS8551	Band-pass	Q = 35	8	187.2	70dB (typ)

N.B. : For other information, please consult the corresponding data sheets.

APPLICATIONS

GENERAL APPLICATIONS AROUND M.P.F. :

With this new concept of M.P.F., SGS-THOMSON is looking to cover all applications covering standard filters (passive, active) involved in the processing of analog signals.

Amongst these, telecommunications (modem, PABX, telephone line, signaler, mobil telephone), data acquisition (before A/D conversion and after D/A conversion), speech (detection, analysis, storage), portable instrumentation (geophysics, biomedical) and specially industrial applications (process control, servomotor control, remote control). For all these applications, each filter function is reduced to one M.P.F. derived either from the standard range of M.P.F. or from custom design M.P.F.'s, according to the requirements of the equipment.

HARDWARE IMPLEMENTATION AROUND M.P.F. :

TYPICAL USE OF THE M.P.F. (figure 6) : The M.P.F. is fed in dual supply : ± 5V.

The adjustment of the DC output level of the M.P.F. is achieved by an external voltage source (for example, a bridge divider connected between the positive and the negative power supplies and whose the middle point is connected to the LVL pin of the M.P.F.). If no output DC adjustment is required, the LVL pin can be directly connected to GND.

The consumption of the filter can be also adjusted by means of an external resistance connected between V^+ (or GND) and the PWF pin of the circuit.

The consumption can thus be chosen to match the particular application.

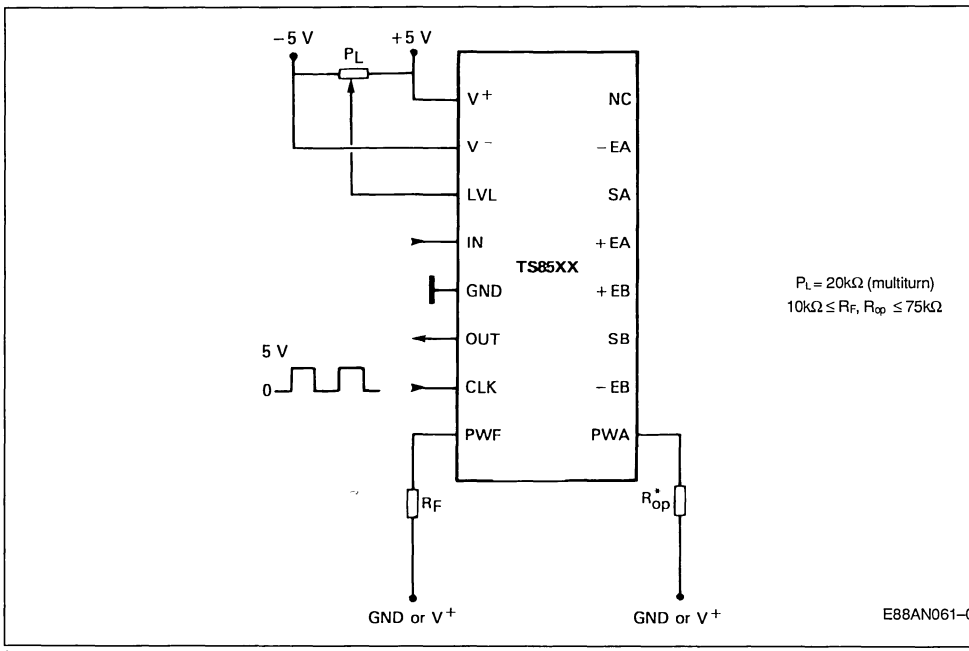
The stand-by mode is obtained by strapping the PWF pin to V^- (or non connected).

The adjustment of the power consumption of the two operational amplifiers can be achieved exactly like for the previous case, but via the PWA pin of the circuit. The stand-by mode is also obtained by strapping the PWA pin to V^- (or non connected).

The clock levels are TTL, but CMOS levels are accepted.

With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V, between – 4.5 and 3.5V.

Figure 6 : Typical Use of the M.P.F. (± 5V).



* If the OP.AMPS are not used, R_{op} must not be connected between PWA and GND (or V^+).

USE OF THE M.P.F. WITH 0-10V (figure 7) : The M.P.F. is fed in single supply : 0-10V.

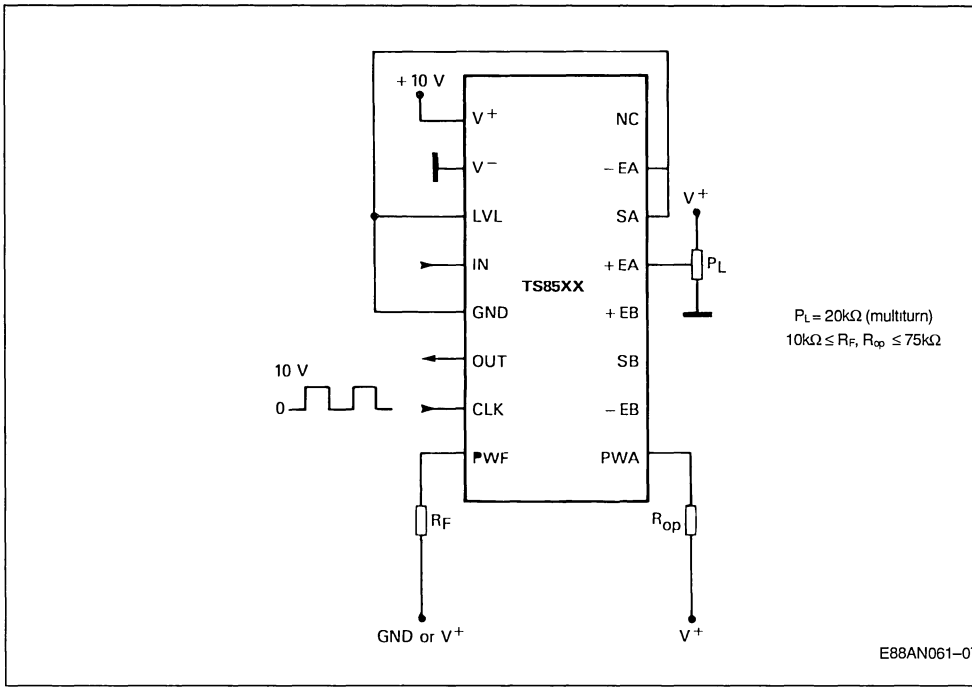
In this case, V^- is the reference ground of the circuit and GND must be adjusted to + 5V by means of the potentiometer P_L (V^+ - V^-)/2).

The adjustments of the DC output level of the M.P.F., of the power consumptions of the filter and of the operational amplifiers can be achieved exactly like previously.

The high level of the clock must be at least 1.4V upper the GND level.

With these previous conditions, the output linear dynamic range of the M.P.F. is about 8V between 0.5 and 8.5V.

Figure 7 : Use of the M.P.F. with 0–10V.



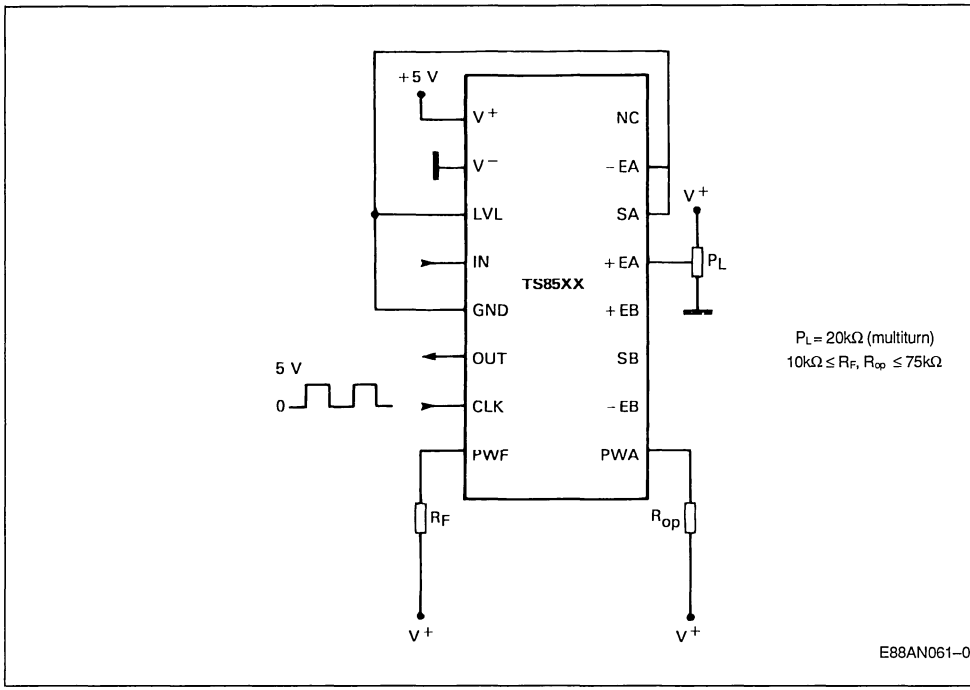
USE OF THE M.P.F. WITH 0-5V (figure 8) : The M.P.F. is fed on in single supply : 0-5V.

In this case, V^- is the reference ground of the circuit and GND must be adjusted to + 2.5V by means of the potentiometer P_L ((V^+ -V^-)/2).

The other adjustments are achieved exactly like previously except for bias resistances of the filter and of the operational amplifiers (Rf and Rop), whose must be exclusively connected to V^+.

The clock levels must be TTL levels. With these previous conditions, the output linear dynamic range of the M.P.F. is about 2.2V, between 1.2 and 3.4V.

Figure 8 : Use of the M.P.F. with 0–5V.



ANTI-ALIASING AND SMOOTHING :

- Anti-aliasing : the switched capacitor filters are sampled systems and must verify the SHANNON condition imposing a sampling frequency (Fs) equal, at least, to the double of the upper frequency (Fc) contained in the spectrum to transmit. With this condition, no information is added or lost on the transmitted signal. This theorem describes the well-known phenomenon called spectrum aliasing shown figure 9, where the entire spectrum to transmit appears around Fs, 2 Fs, 3 Fs,... and so on. Thus, all spectrum components of the signal contained around these frequencies are transmitted by the M.P.F., oppositively to the desired result.
  To cancel the effects of this phenomenon, it is required, before all sampled system, to filter all the spectrum components of the input signal upper than Fs-Fc. An analog filter, called "anti-aliasing filter", must be therefore applied before the M.P.F.
  The selectivity of this filter depends upon the Fs/Fc ratio.
  If Fs/Fc > 200, a RC filter (first order low-pass) is sufficient.
  If Fs/Fc < 200, a SALLEN-KEY structure (second order low-pass) must be used.
  This structure and its relationship are described figure 10. In these relationship, Fc is the cut-off frequency desired of the anti-aliasing filter and ξ its damping coefficient. For a cut-off as tight as possible and without overvoltage around it, ξ must have a value around 0.7.
  N.B. : If Fs/Fc < 2 (figure 11), the spectrum to transmit and the spectrum aliased have a part in common and it becomes impossible to share the useful signals from the undesirable signals.
- Smoothing : as the signal obtained as the output of the M.P.F. is a sampled and hold signal, it is often required to smooth it. This smoothing filter can be achieved from the SALLEN-KEY structure previously described (figure 9).

Figure 9 : Phenomenon of the Spectrum Aliasing.

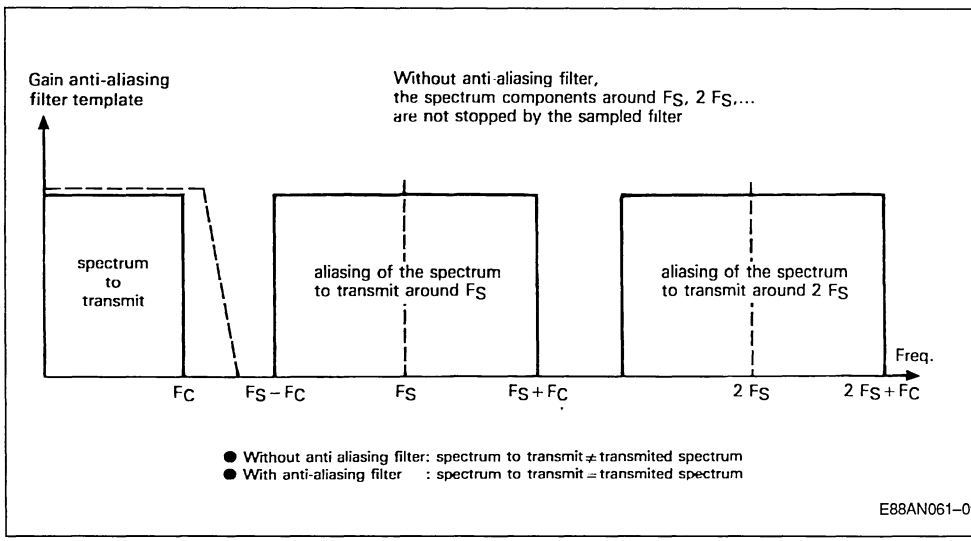
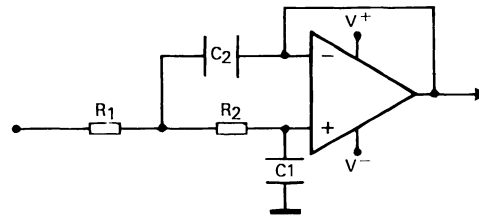


Figure 10 : Sallen–key (second order low–pass filter) for Anti–aliasing and Smoothing.



$R_1 = R_2$ = arbitrary value
F_c = cut–off frequency desired
ξ = damping coefficient

$$C_1 = \frac{\xi}{2\pi R_1 \times F_c}$$

$$(C_1 = \xi^2 \times C_2)$$

$$C_2 = \frac{1}{2\pi \xi R_1 \times f_c}$$

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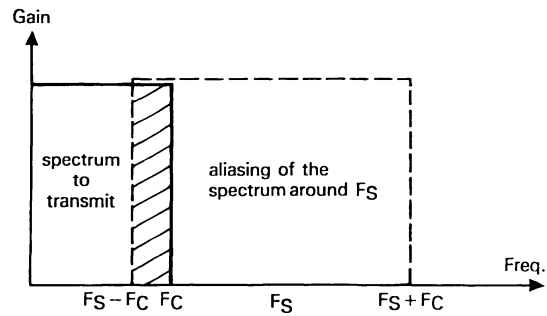
Figure 11 When Fs/Fc<2, the spectrum components including between Fs–Fc and Fc and which are due to spectrum aliasing are not stopped by the sampled filter.



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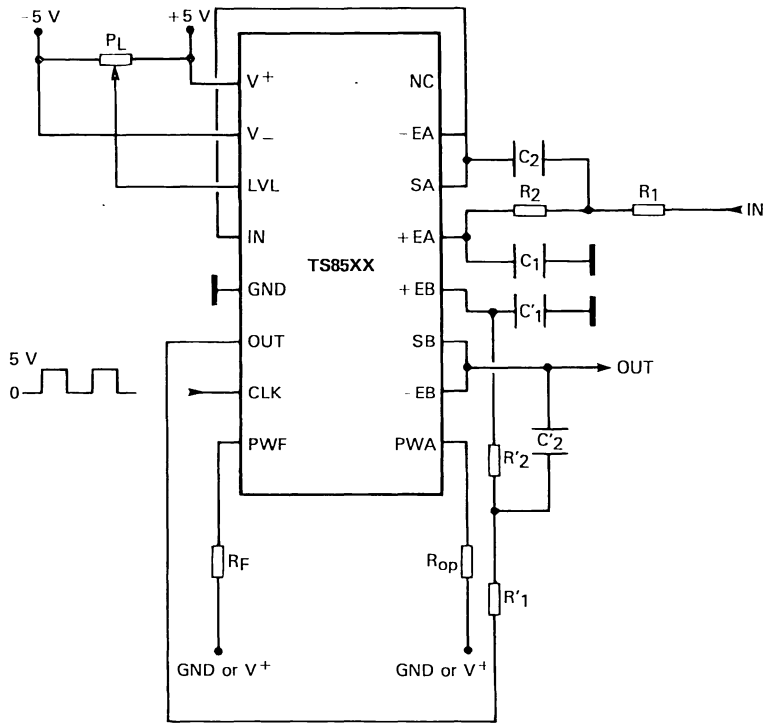
- Hardware implementation : in order to make easier anti-aliasing and smoothing, SGS-THOMSON has designed, on the even chip of the M.P.F., two general purpose operational amplifiers. A few external components are therefore sufficient to achieve these functions (figure 12).

Figure 12 : M.P.F. with Anti–aliasing and Smoothing Filters.



P_L = 20kΩ (multiturn)
10kΩ ≤ R_F, R_{op} ≤ 75kΩ
R_1, R_2, C_1, C_2 see anti–aliasing
R'_1, R'_2, C'_1, C'_2 and smoothing considerations

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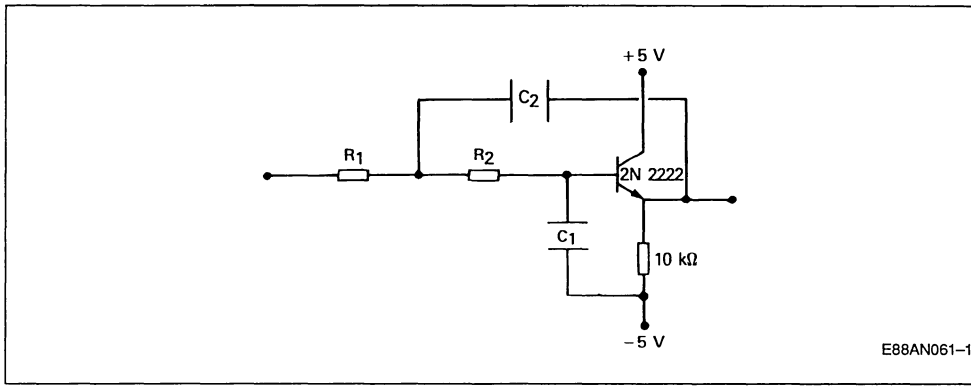
On the other hand, it the most M.P.F.'s, a special integrated cell is included in the chip (cosine filter) to reduce the aliasing effects around Fs.

Nonetheless, if the application allow it, these two operational amplifiers can be used to implement other functions (gain, comparator, oscillator,...).

In this case, the circuit shown figure 13 can be used as anti-aliasing or smoothing filter. This structure is the same as the SALLEN-KEY structure described figure 9 (second order low-pass), in the same way as the corresponding relationship.

Figure 13 Second Order Low–pass Filter (sallen–key structure) with a transistor replacing the operational Amplifier.



IMPLEMENTATION OF THE M.P.F. CLOCK FROM EXTERNAL COMPONENTS (figure 14) :

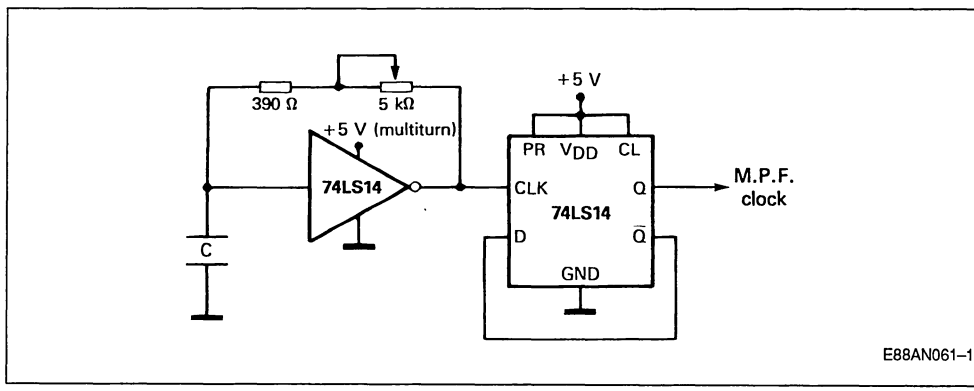
A mouting with a minimum of external components allows to achieve the clock required for the M.P.F.

The value of the frequency obtained with this mounting depends upon C value, as shown on the following board :

C(nF)	47	15	6.8	2.2	1	0.47	0.33	0.22
$\mathbf{F_s}$ **min** (kHz)	1.5	4.3	6.7	30	44	84	126	172
$\mathbf{F_s}$ **max** (kHz)	16	48	183	305	1020	1750	2430	3010

N.B. : The accuracy of these values is 20%, according to the usual resistor and capacitor accuracy.

Figure 14 : M.P.F. Clock Achieved from External Components.



APPLICATION EXAMPLE : FREQUENCY DETECTION :

The principle of this type of application is as follows : a sinewave (amplitude x, frequency f) modulated by digital information is superposed to an other signal, that we shall call the main signal. To better understand and illustrate this example, we shall take the hypothesis of a main signal equally sinoidal (amplitude X, frequency F) and we shall assume that X >> x and F < f (T > t). Thus, the main signal is modulated by frequency f during high level (+ 5V) and not modulated during low level (0V) of the bit to be transmitted. These wave trains can, for example, correspond to commands that must be received and then understand by a microprocessor in a suitable format for their processing.

Therefore, these wave trains must be detected and then applied to the microprocessor in form of logic pulse, of which high levels (+ 5V) correspond to the presence and low levels (0V) to the absence of the waves.

In this type of application, two factors are of prime consideration, namely : selectivity and size. Both transmission channel and transferred data being prone to noise, the M.P.F. must be adequately selective to reject the unwanted frequencies close to the center frequency f. On the other hand, as far as the industrial aspect of the application is concerned, the size is considered to be of major importance since it is impractical to envisage a large area to accomodate only the filtering section.

Let's consider the general diagram of figure 15. By using a suitable sampling frequency (Fs), the M.P.F. can have a center frequency equal to f.

Since TS8551 is a highly selective filter and the modulated wave has a very stable frequency, the M.P.F. will only filter out the main signal (frequency F) and let through the modulated signal (frequency f). An attenuator stage and an anti-aliasing analog filter are required preceeding the M.P.F. The attenuator stage is used to match the amplitude of the main signal (X) to the input characteristics of the M.P.F., and the analog filter to prevent the M.P.F. from passing the frequency spectrum of the incident wave aliased around Fs. At the output of the M.P.F., the combination of a first order high pass CR filter and a negative voltage clipping diode will produce a sinewave of frequency f and amplitude v. Following this filter, an amplifier of gain G > 1 also delivers a sinewave signal of frequency f but of amplitude V = G x v.

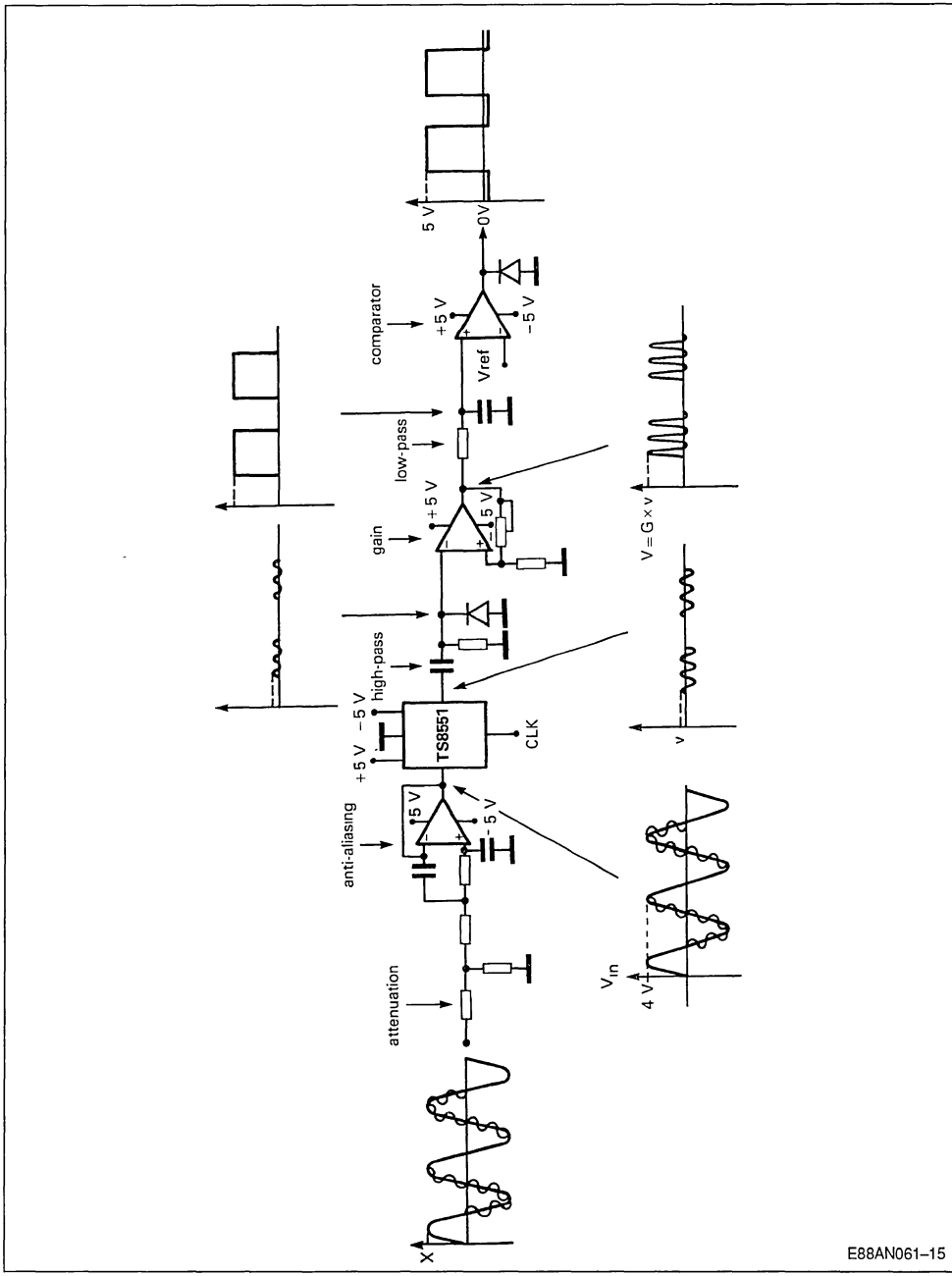
The following first order low pass RC filter detects the enveloppe of the amplified signal and then compares it with a reference voltage Vref.

If V > Vref, the output of the operational amplifier goes to the positive saturation state (+ Vsat) thereby indicating the presence of the wave, whereas if V < Vref, then the amplifier goes to the negative saturation state (- Vsat) to indicate the absence of the wave. A negative voltage clipping diode at the output of the comparator will provide a succession of high (+ 5V) and low (0V) states producing a pulse train. The period and the duration of this pulse train inform the microprocessor of the precise nature of control signal sent.

CONCLUSION

This unique example is sufficient to demonstrate the outstanding application possibilities offered by the M.P.F. Many other features were also discussed in various sections of the present article. Relying on these established facts, SGS-THOMSON is ready to provide an answer to every filtering problem in any application. Due to its remarkable and unlimited possibilities, the M.P.F. concept is estimated to become, in a very near future, as widely employed as gate-arrays and mask programmable ROM microcomputer devices are nowadays.

Figure 15 Example of an Application of the M.P.F. with a very Selective Band–pass Filter : the Frequency Tracking.



A SUPPLEMENT TO THE UTILIZATION OF SWITCHED CAPACITOR FILTERS

INTRODUCTION

This application note is a complement to the **"Application Note AN-061"** which introduced the range of switched capacitor filters manufactured by SGS-THOMSON Microelectronics and discussed the following topics :

- **Anti-aliasing & Smoothing filters**
- **Ground pin biasing techniques using a single supply voltage**
- **dc output level adjustment**

The present application note outlines and provides an in-depth discussion of other important factors related to the use of switched capacitor filters, namely :

- **Gain adjustment**
- **dc output level locking**
- **Oscillators**
- **Regulated power supply**
- **Wiring & Layout recommendations**

Information contained in various sections will yield cost-effective solutions and enable the designer to take full advantage of the outstanding performances offered by SGS-THOMSON' range of **Switched Capacitor Filters** ; **TSG85XX, TSG86XX, TSG87XX Standard Series** and **Semicustom Filters**.

GAIN ADJUSTMENT

Majority of standard SGS-THOMSON filters have an inherent pass band gain of approximately 0dB. In certain applications however, a larger gain value combined with the gain adjustment possibility is required.

Gain adjustment can be accomplished using one of the operational amplifiers available in the same package as the filter circuit.

Two cases are discussed next :

- **Operational amplifier used for gain adjustment**
- **Sallen-Key Cell with gain adjustment**

USING AN OPERATIONAL AMPLIFIER

This is the most straightforward solution. Amplifier configurations are commonplace and well-known. The two main arrangements are illustrated next.

Figure 1 : Inverting Configuration.

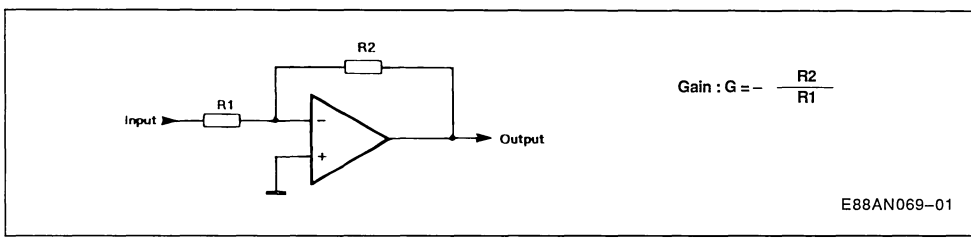
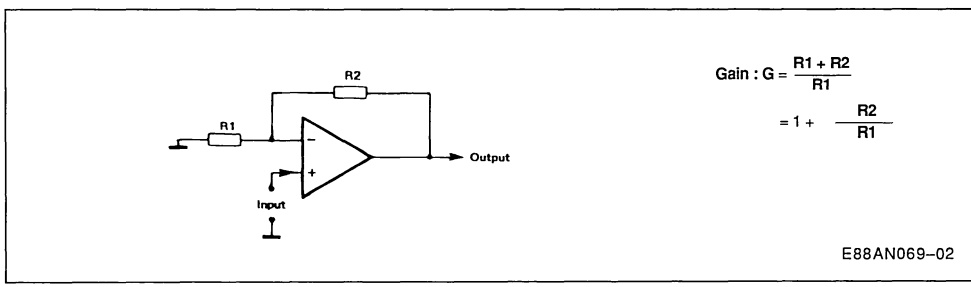


Figure 2 : Non–Inverting Configuration.

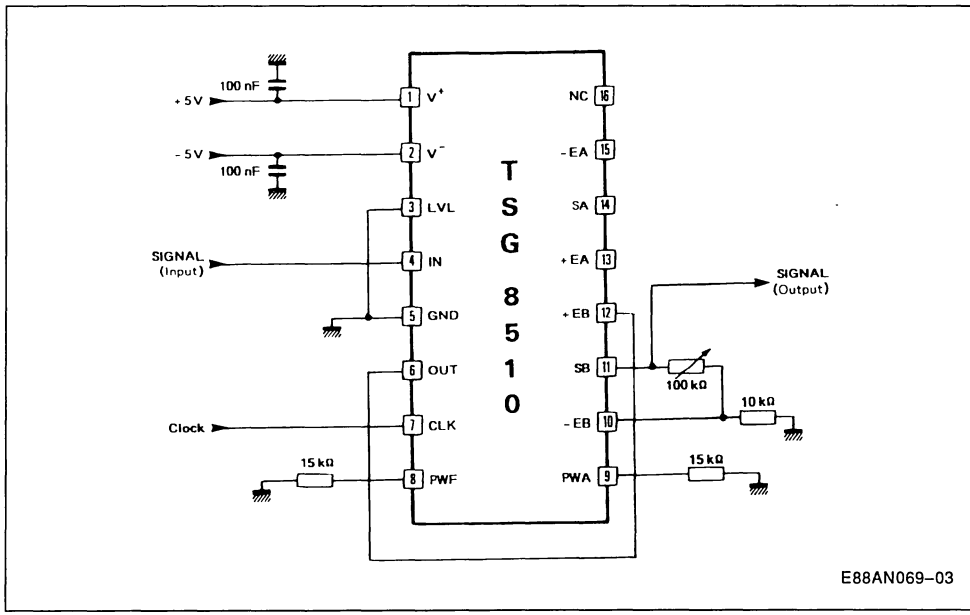


This type of configuration yields high gain values. Only limitations are those related to the electrical characteristics of the operational amplifiers such as : gain-bandwidth-product "2MHz typ." or the output voltage range "–4.2V, +3.5V" (values measured using symmetrical – 5V, + 5V power supplies).

Figure 3 illustrates the arrangement of a non-inverting configuration.

In order to obtain an enhanced signal-to-noise ratio, the amplifier is directly coupled to the filter output which will reduce the noise spectrum.

Figure 3 : Gain Adjustment.



SALLEN-KEY CELL WITH GAIN ADJUSTMENT

In some applications, the operational amplifiers available within the filter circuit may be already used to implement anti-aliasing and smoothing filters generally required for switched capacitor filters.

In this case, the smoothing filter can be implemented using a second order Sallen-key cell with a gain higher than 1. Figure 4 depicts this arrangement and figure 5 illustrates an example of the actual configuration.

Figure 4 : General Arrangement of a Sallen–Key Cell (with gain adjustment).

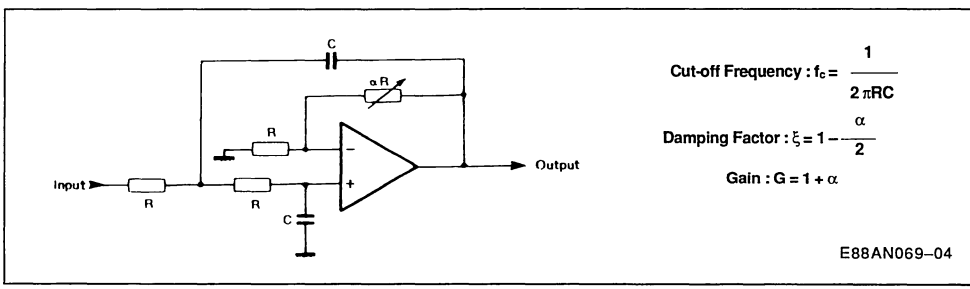


Figure 5 : Sallen–Key Cell (with gain adjustment).

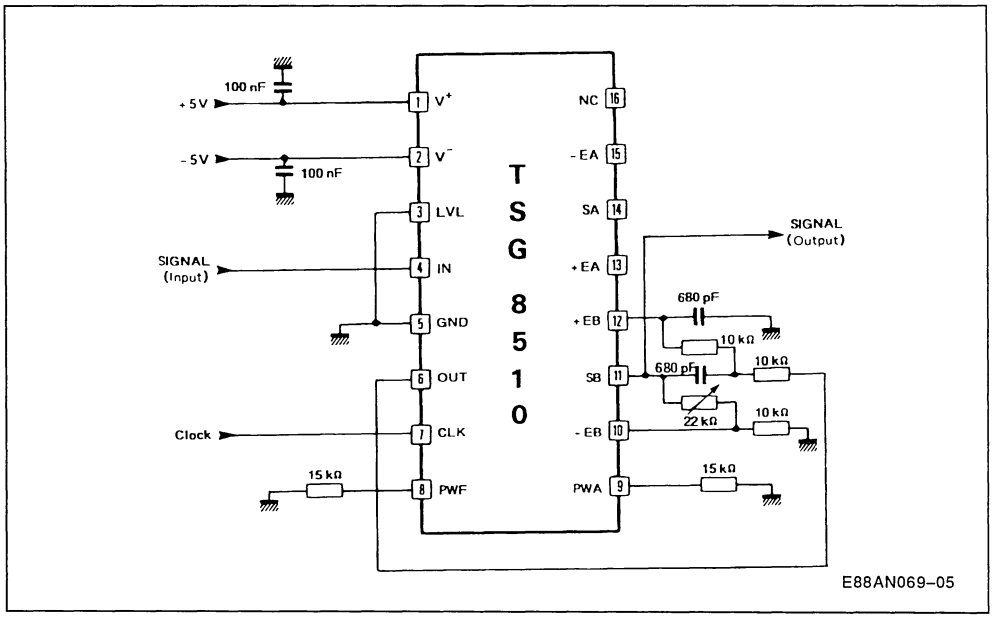
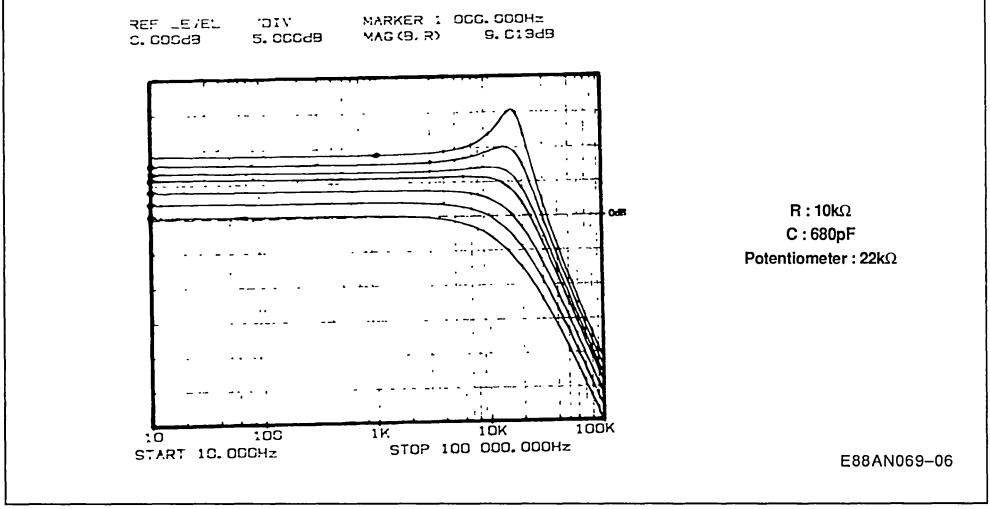


Figure 6 outlines the response curves of the Sallen-key cell obtained at various potentiometer settings, i.e. at different gain values.

Figure 6 : Frequency Response of Sallen–Key Cell (with gain adjustment).



It is clear that the damping factor varies as a function of α.

This configuration provides gain values of up to 6dB without any appreciable overshoot in the response curves.

FILTER OUTPUT DC LEVEL LOCKING

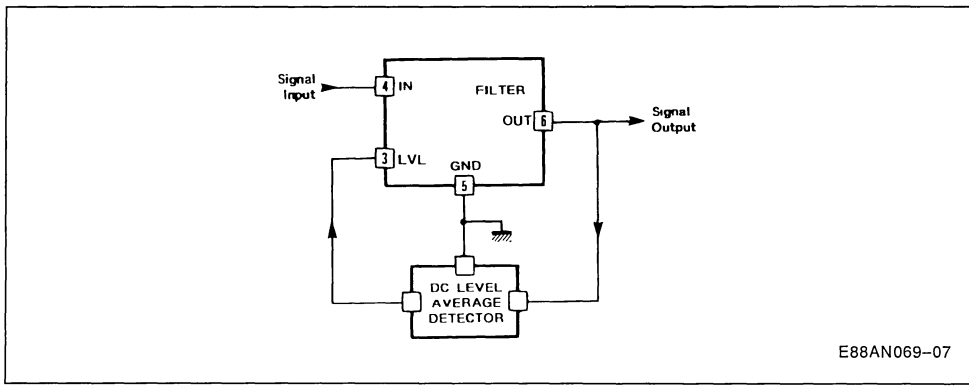
Switched capacitor filters manufactured by SGS-THOMSON feature a **"Level"** (**LVL**) terminal for the adjustment of the output dc level.

This function is accomplished by applying to this pin, a dc signal corresponding to the desired output dc level. Characteristic curves labeled "**Output voltage** versus **voltage on LVL pin**" are used to determine the value of the voltage to be applied to LVL terminal. This curve is available in each filter technical data sheet. In general, the voltage applied to "**LVL**" pin and hence the filter output level, is set by a potentiometer inserted between V^- and V^+ potentials.

The output level is generally set a 0V or at "**Ground**" (**GND**) pin potential.

In this case, an "**automatic offset compensation**" feature may be implemented as illustrated in figure 7.

Figure 7 : Automatic Offset Compensation.



The detector has a very low cut-off frequency in order to detect the output dc level and to control it through "**LVL**" pin.

According to the filter type, two cases are possible :

THE DC OUTPUT VOLTAGE IS DIRECTLY PROPORTIONAL TO THE VOLTAGE APPLIED TO "LVL" PIN

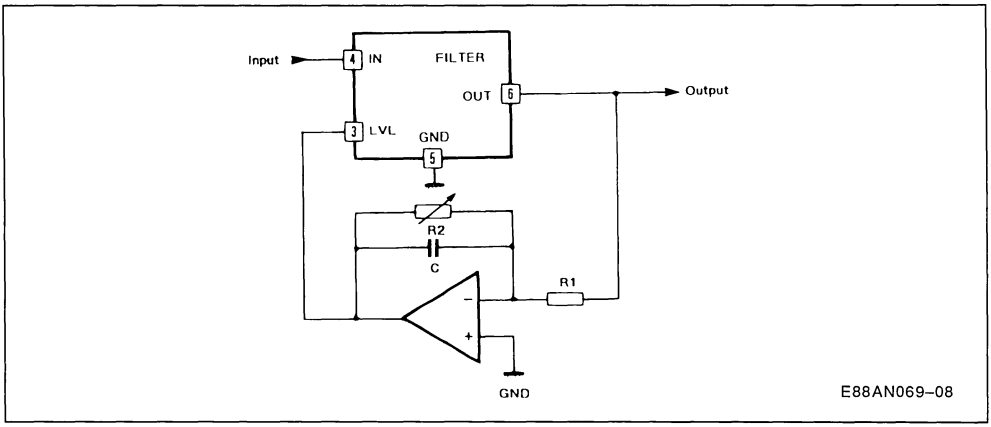
In this case, the output signal polarity should be inverted for feed-back functions.

A conventional integrator configuration using operational amplifier may be used for this purpose. This configuration is given in figure 8.

The feed-back loop behaves as an integrator at frequencies very much higher than the cut-off frequency $\frac{1}{2\pi \times R2 \times C}$

The dc gain is " $-\frac{R2}{R1}$ " and may be adjusted by modifying the value of the either resistor ; thus allowing accurate control of precision and response.

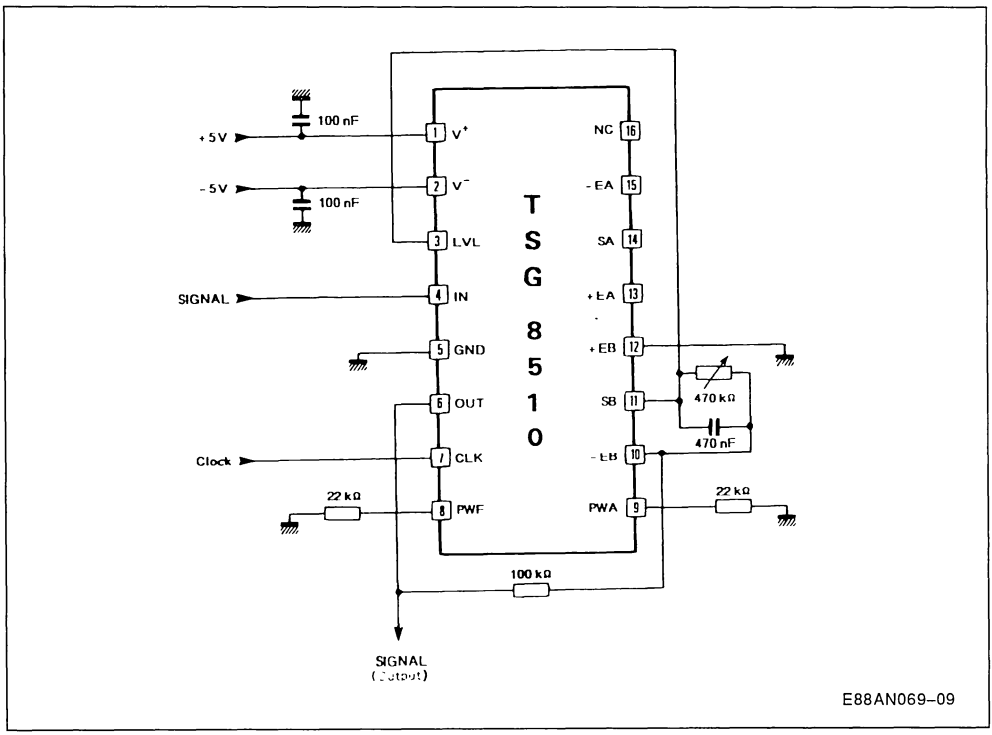
Figure 8 : Output dc Level is inverted and Feedback to "LVL" Pin for Automatic Offset Compensation.



Here, we have chosen to adjust the value of R2 resistor, so that when R2 value is increased the gain also increases, but the cut-off frequency falls. Therefore, any risk of instability occurrence at high gain is eliminated.

Figure 9 depicts the practical application diagram. As shown, the feed-back network is readily implemented using one of the operational amplifiers available within the filter package.

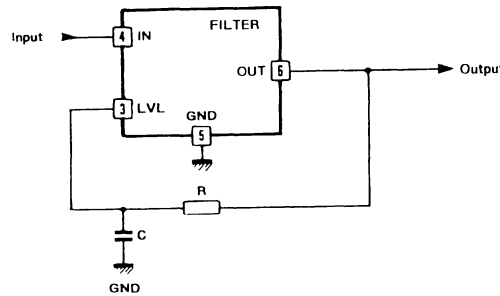
Figure 9 : Automatic Offset Compensation.



THE DC OUTPUT VOLTAGE IS INVERSELY PROPORTIONAL TO THE VOLTAGE APPLIED TO "LVL" PIN

The output signal no longer requires polarity inversion and the arrangement is simplified to a conventional RC integrator as shown in figure 10.

Figure 10 : Only a R–C Cell (1st order low–pass) is needed for Automatic Offset Compensation.



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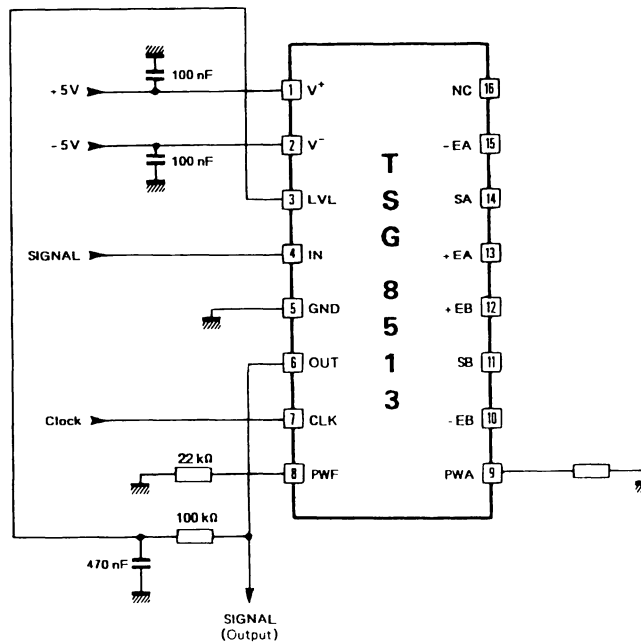
The RC time constant should be selected to be high in comparison to the period of the signal transmitted through filter. Due to low output filter impedance and high input impedance of R-C cell, the output signal is not subjected to any disturbance.
Figure 11 outlines the practical application diagram.

Figure 11 : Automatic Offset Compensation.



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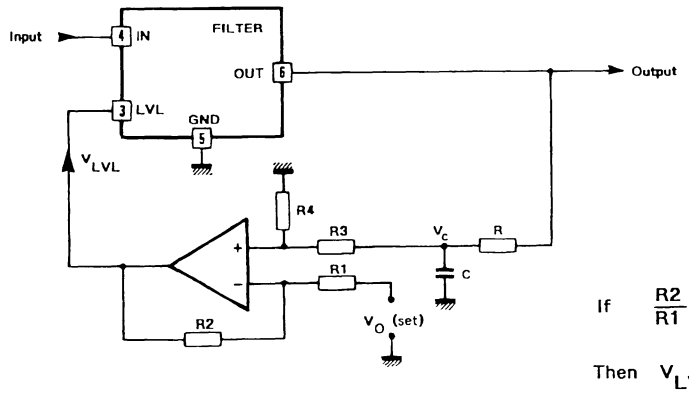
A non-inverting operational amplifier configuration may be used, if feed-back loop gain control is required.

Note : "**LVL**" pin voltage can be locked onto any variable voltage by following the same procedure as mentioned earlier - i.e. output signal detection followed by the amplification of the difference signal measured between the output voltage and the adjustable control voltage.



If $\frac{R2}{R1} = \frac{R4}{R3}$

Then $V_{LVL} = \frac{R2}{R1}(V_O - V_C)$

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CLOCK OSCILLATORS

Switched capacitor filters require an external clock for operation. This clock sets the internal sampling frequency of the filter and also determines the frequency range. The clock circuit is generally implemented using logic gates.

The Mask Programmable Filters of SGS-THOMSON feature two uncommitted operational amplifiers integrated on the same silicon chip that are available for functions related to filtering.

The objective of this section is to illustrate how one of these operational amplifiers may be configured as oscillator thereby providing the clock required for the switched capacitor filters.

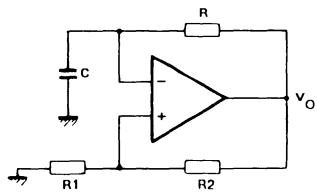
Two types of oscillator will be discussed :

- **RC-type free-running relaxation oscillators**
- **Crystal-controlled oscillators** (Quartz or Ceramic Resonator)

FREE-RUNNING RELAXATION OSCILLATORS

This type of oscillator relies on the principles of a capacitor "C" charge-up and discharge through a resistor "R" as shown in figure 12.

Figure 12 : Free–Running Multivibrator.



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When the output voltage is positive, the voltage at the non-inverting terminal is $V_O \frac{R1}{R1 + R2}$ and the capacitor C begins charging through resistor R until the voltage at the inverting terminal becomes equal to the voltage at the non-inverting terminal i.e.,

$$V_O \frac{R1}{R1 + R2}$$

The amplifier is then triggered, its output falls to low saturation level, C is discharged via R until the inverting input becomes once again negative with respect to the non-inverting input. Then the output voltage returns to the high saturation value and the entire cycle is repeated. If high and low saturation levels have the same absolute values, the oscillator output signal would have the following characteristics :

- Duty Cycle : 0.5
- Period : $T = 2RC \log (1 + 2\frac{R1}{R2})$

In this case, the oscillator period is :

$$T = R\,C \log \left[1 + \frac{R1}{R2}\left(1 - \frac{V^+_{sat}}{V^-_{sat}}\right)\right] + R\,C \log \left[1 + \frac{R1}{R2}\left(1 - \frac{V^-_{sat}}{V^+_{sat}}\right)\right]$$

Where V^+_{sat} and V^+_{sat} are respectively high and low saturation voltages of the operational amplifier. V^+_{sat} and V^-_{sat} are given in data sheets :

$V^+_{sat} = +3.5V$, $V^-_{sat} = -4.5V$ for TSG85XX and + 5V, – 5V power supply.

Electrical configurations are given in figures 16 and 17 that illustrate how by using currently available components, a low-cost and perfectly stand-alone filter application is implemented.

Figure 17 illustrates the application using a single + 10V or + 5V power supply. In this case, the second operational amplifier is configured as voltage follower and used to bias "**Ground**" and "**Level**" pins.

Clock signal waveforms generated by this type of multivibrator are depicted in figures 14 and 15.

The oscillogram of figure 14 is the waveform obtained using – 5V, + 5V power supplies and shows in particular how the output signal may go negative.

Thanks to its **integrated clock shaping stage**, the filter can accept this negative going signal - thus offering an outstanding flexibility for the implementation of clock oscillators.

It is clear that since C has a fixed value, the frequency of this multivibrator is readily set by adjusting the value of R (potentiometer).

If high and low saturation voltages are not identical, these values will be taken into consideration in the above expression for period calculation and the value of the duty cycle will no longer be 0.5. In addition, the frequency and the amplitude of the output signal will both vary as a function of the operational amplifier power supply. A good frequency and amplitude stability is achieved using two zener diodes to limit the output signal excursion.

In the case of SGS-THOMSON filters, the saturation voltages have different absolute values as illustrated by the oscillogram of figure 14 and the duty cycle has a value different from 0.5 mentioned earlier. This is not however an important matter as the filter circuit contains a clock shaping stage and can therefore accept directly the operational amplifier output signal.

The **TSG8550** filter was tested in various oscillator configurations and response curves obtained are depicted in paragraph 4.4 at the end of this section.

With reference to these curves, it is observed that the filter circuit operates ideally with the free-running oscillator discussed earlier.

Some curves also illustrate the filter response characteristics obtained using an external clock generated by conventional logic gates. Note that both curves are perfectly superimposed.

The foregoing discussion demonstrated that this type of oscillator offers satisfactory results irrespective of the power supply type : – 5V, + 5V – 0V, + 10V – 0V, + 5V.

Note also that this type of oscillator can operate at relatively high frequencies. In fact, the response curves of the **TSG8550** were obtained at oscillator frequencies of up to **1.2MHz** approximately. In this case however, one should use a low value biasing resistor (here, $R_{PWA} = 10k\Omega$), to obtain appropriate "**slew rate**" at the operating frequency.

Figure 13

EXTERNAL TTL–type CLOCK
(generated by logic gates)

2volts/division
2μs/division
E88AN069–14

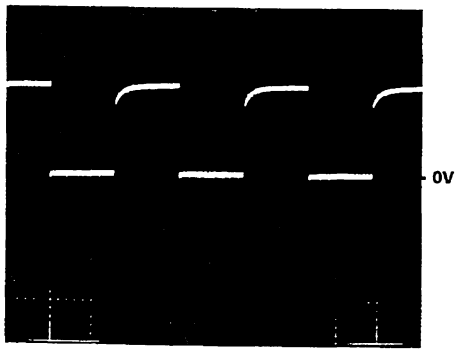


Figure 14

RC–type FREE–RUNNING OSCILLATOR
(using one of the filter op–amps)
[–5V, +5V power supplies]

2volts/division
2μs/division
E88AN069–15

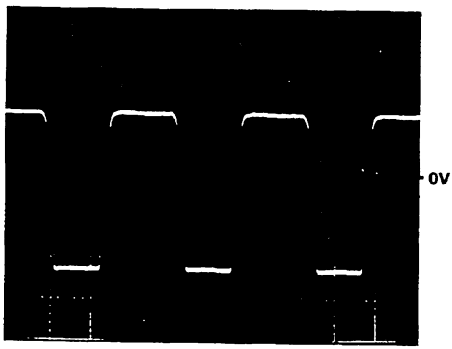


Figure 15

RC–type FREE–RUNNING OSCILLATOR
(0, +10V power supply)

2volts/division
2μs/division
E88AN069–16

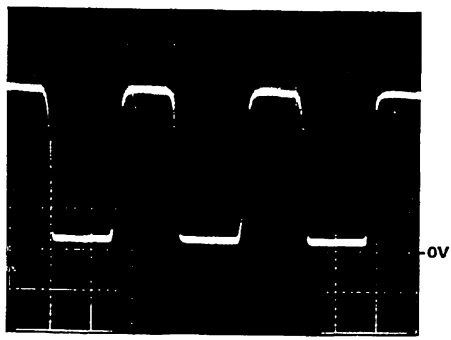


Figure 16 : RC–type Free–Running Oscillator (+5V, –5V power supplies).

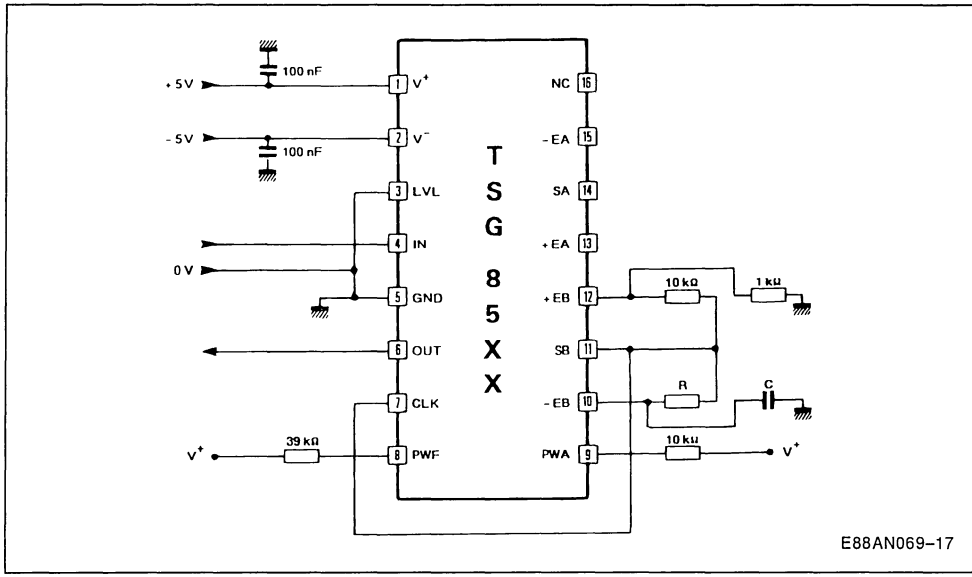
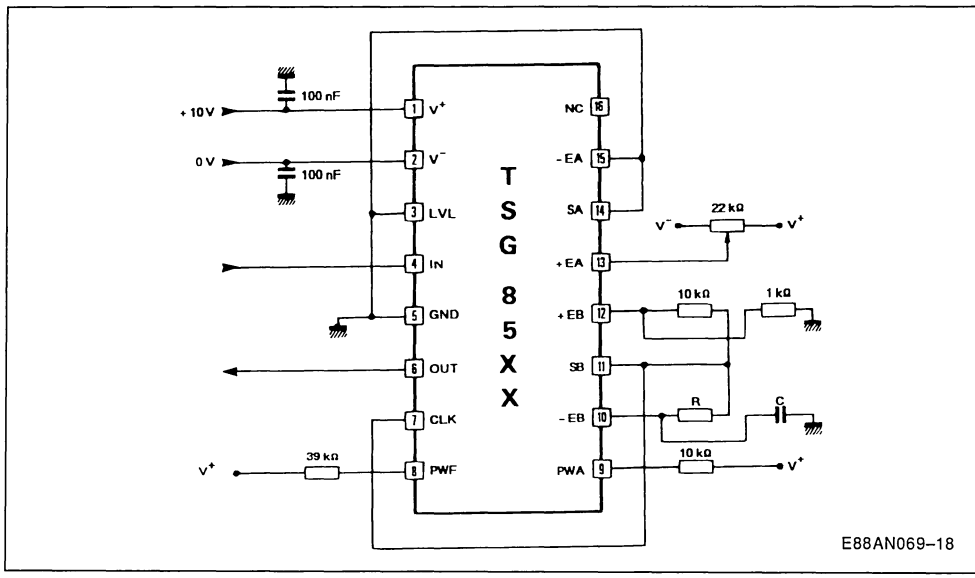


Figure 17 : RC–type Free–Running Oscillator (0, +10V or 0, +5V power supplies).



CRYSTAL-CONTROLLED OSCILLATORS (or Ceramic Resonator)

The multivibrator circuit described above is a low-cost oscillator providing satisfactory operation of the switched capacitor filters.
It has however two drawbacks :

- Frequency adjustment by a potentiometer
- Frequency variation with device power supply

Better frequency stability combined with simplicity of use will be obtained if a crystal-controlled oscillator is used for clock generation.

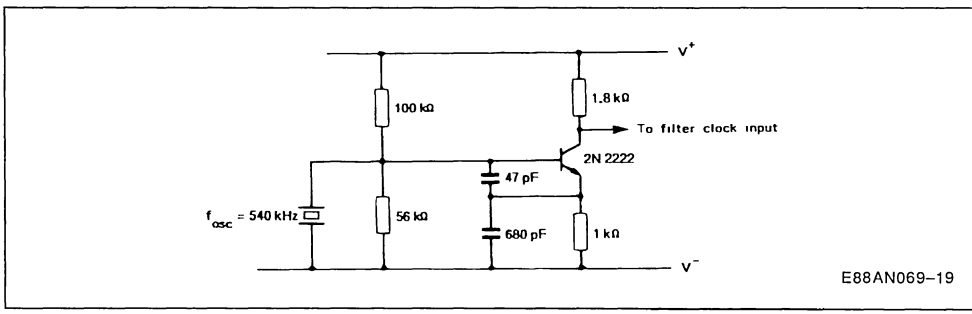
This solution is particularly interesting in applications not requiring any adjustment of the clock frequency ; as is the case of the most applications built around filters.

Note however that if frequency adjustment is required, one may either switch between various resonators or implement a master oscillator followed by a frequency divider circuit.

TRANSISTOR-BASED OSCILLATOR

In untuned oscillators, the crystal is most often operated in its fundamental mode. Figure 18 illustrates the arrangement of the oscillator to be discussed next.

Figure 18 : Crystal–controlled Oscillator.



This is a **Colpitts**-type **parallel resonance** oscillator. The operating point of the crystal is such that it behaves like a high Q choke. A capacitive bridge provides the energy required to initiate the oscillation.

This oscillator does not require any adjustment - its frequency is highly stable whatever the power supply mode (- 5V, + 5V - 0V, + 5V - 0V, + 10V).

Due to the operating frequency value of this application, a small signal "**general purpose**" transistor will be suitable.

Here, we have employed a **Ceramic Resonator** whose fundamental frequency is **fosc = 540kHz**.

This is a popular resonator used in particular as oscillator for SGS-THOMSON range of television circuits (time base, switching power supplies, chroma decoder, etc...) and is therefore available at low-cost "**consumer**" price.

The oscillogram of figure 19 illustrates the output signal waveform of this oscillator. Although its shape differs from that generated by a TTL clock as illustrated in figure 13, this is a negligible drawback as switched capacitor filters manufactured by SGS-THOMSON feature a built-in signal shaping stage on clock inputs.

Figure 19

COLPITTS OSCILLATOR WAVEFORM

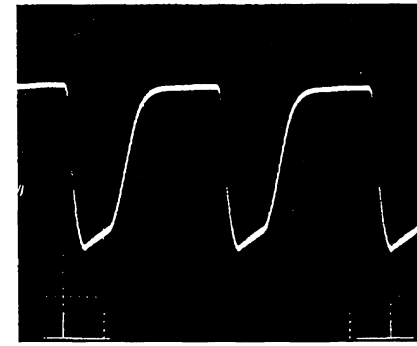
(ceramic resonator)

[0, +5V power supply]

1volt/division

0.5ms/division

E88AN069–20



Various response curves obtained employing this oscillator in combination with **TSG8550** filter operated at different power supply modes, are given at the end of this section in paragraph 4.4.

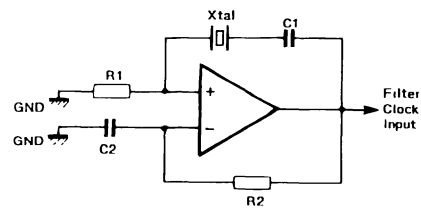
Similar procedure was applied but using an external clock generated by TTL-type logic gates. It is seen that there is no significant difference between the curves obtained in this case and those obtained previously.

It is therefore obvious that the filter operates satisfactorily with an external Colpitts-type oscillator.

OPERATIONAL AMPLIFIER-BASED OSCILLATOR

Figure 20 shows the general arrangement of this oscillator.

Figure 20 : Crystal–controlled Oscillator.



E88AN069–21

The above figure illustrates how a crystal-controlled oscillator is readily configured using one of the operational amplifiers available within the package of the switched capacitor filters of SGS-THOMSON.

The resonator is directly inserted within the positive feed-back loop. The oscillation is initiated when the transmission through crystal is at its maximum value, i.e. when the series resonance of the crystal occurs. High input impedance of the operational amplifier together with the blocking capacitor C1 contribute towards oscillator stability. The feed-back to inverting input through resistor R2 ensures oscillator start-up and dc stability.

The negative feed-back at high frequencies is attenuated by capacitor C2 whose value should be so selected to prevent the resonator from locking onto a partial mode. The non-inverting input is biased with respect to filters "Ground" pin potential.

Application diagrams are depicted in figures 21 and 23.

Figure 21 : Ceramic Resonator – Controlled Oscillator (–5V, +5V power supplies).

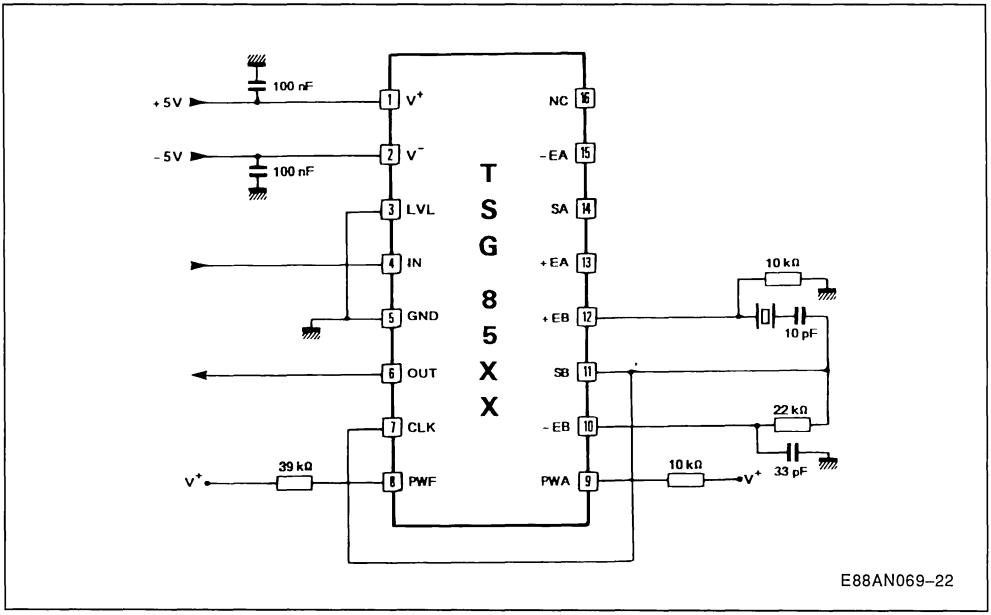
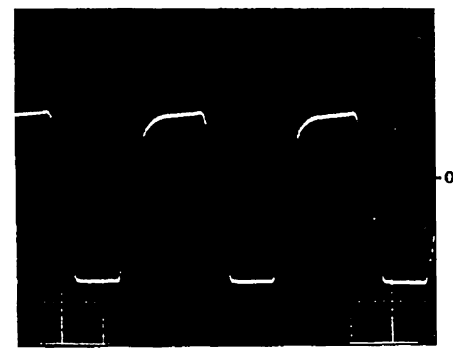


Figure 22

OSCILLATOR CONTROLLED BY CERAMIC RESONATOR

(using one of the filter op–amps)

[–5V, +5V power supplies]



2volts/division

0.5ms/division

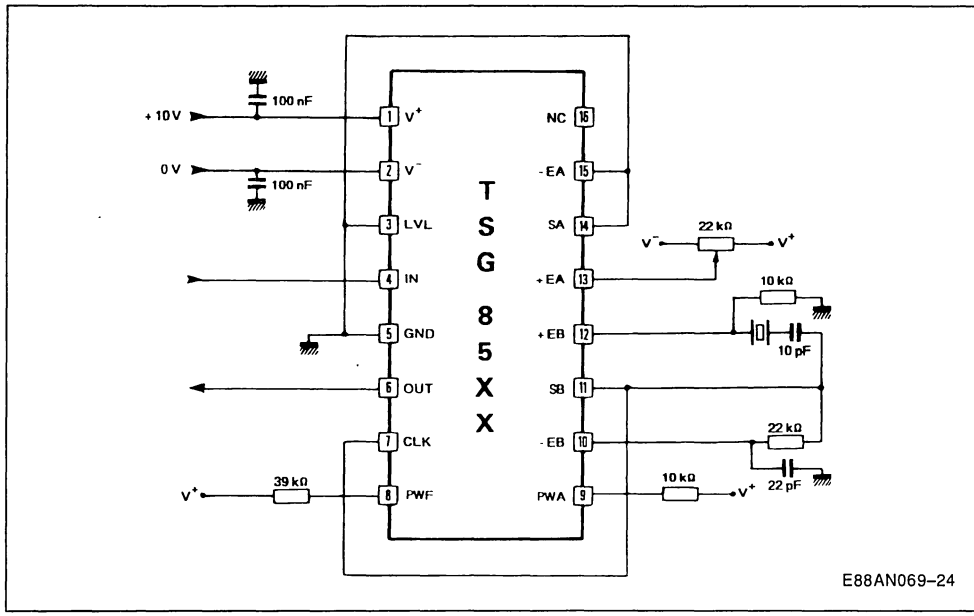
E88AN069-23

Figure 23 illustrates the application using a single power supply.

In this arrangement, the second operational amplifier configured as voltage follower is used to bias filter's "**Ground**" and "**Level**" pins.

Once again, the same "**consumer**" ceramic resonator running at f_{osc} = **540kHz** has been employed in this application.

Figure 23 : Ceramic Resonator – Controlled Oscillator (0, +10V or 0, +5V power supplies).



Oscillogram of figure 22 shows the clock signal waveform obtained from the application depicted in figure 21. Similar waveforms are obtained from the single supply voltage application illustrated in figure 23 - only the output voltage levels are different.

As shown in response curves of paragraph 4.4, the **TSG8550** filter operates satisfactorily with this type of oscillator. Once again, note that there is no difference between the curves obtained using this oscillator and those using an external TTL-type oscillator.

Obviously, operation at other frequencies is possible by using different ceramic resonators. The basic configuration remains the same however.

CONCLUSION

The discussion throughout this section demonstrated how, a clock oscillator is readily built, and a perfectly stand-alone filter implemented, using only a single integrated circuit.

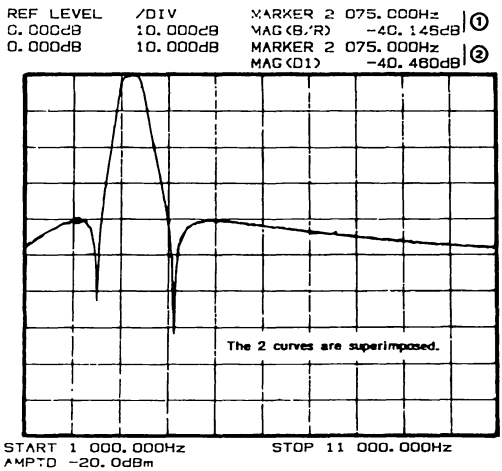
- In applications where frequency adjustment facility is required and price is the prime objective, **RC-type free-running** oscillators are recommended.
- **Crystal-controlled** oscillators are suitable for applications requiring highly stable fixed oscillator frequencies.
- Finally, the oscillator using a single **transistor** allows use of an **8-pin filter** package or to save the two operational amplifiers of the filter for other functions - thereby simplifying the application configuration.

These results have been obtained thanks to the highly efficient and flexible clock input terminal of SGS–THOMSON' **Switched Capacitor Filters.**

All of the oscillators covered in this section, are in addition to TSG8550, also suitable for use with other **standard filter** types and **semicustom filters.**

TSG8550 RESPONSE CURVES USING DIFFERENT CLOCK OSCILLATORS

Figure 24 : RC–Multivibrator Operation (at 153kHz and +5V, –5V power supply).



E88AN069–25

TSG8550

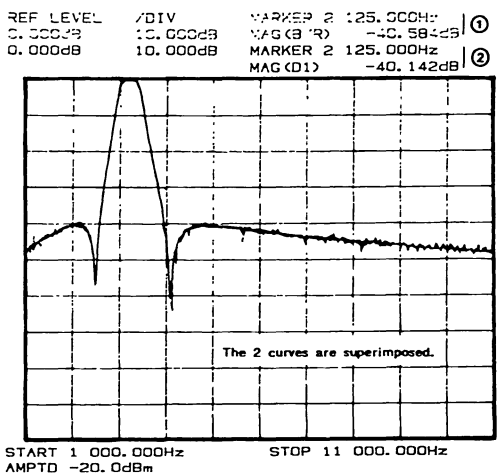
Power Supply : –5V, +5V

Clock Frequency : 153kHz

1– External Clock
2– Free–running Oscillator
R : 2.5kΩ
C : 3.3nF

The RC Multivibrator is implemented with an internal Operational Amplifier

Figure 25 : RC–Multivibrator Operation (at 0V, +10V power supply).



E88AN069–26

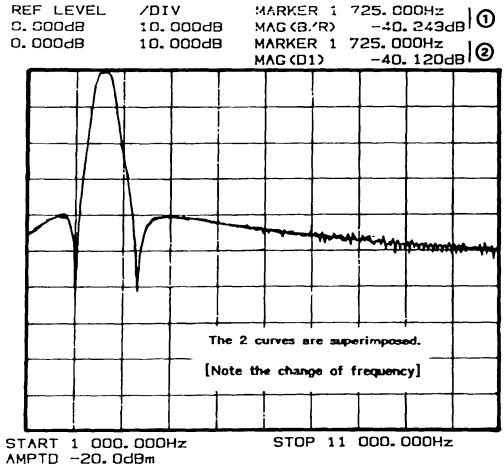
TSG8550

Power Supply : 0V, +10V

Clock Frequency : 153kHz

1– External Clock
2– Free–running Oscillator
R : 2.5kΩ
C : 3.3nF

Figure 26 : RC–Multivibrator Operation (at 0V, +5V power supply).



TSG8550

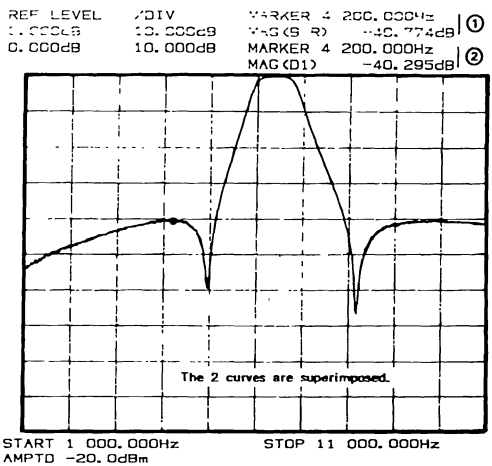
Power Supply : 0V, +5V

Clock Frequency : 123kHz

1– External Clock
2– Free–running Oscillator
R : 2.5kΩ
C : 3.3nF

E88AN069–27

Figure 27 : RC–Multivibrator Operation (at 307kHz clock frequency).



TSG8550

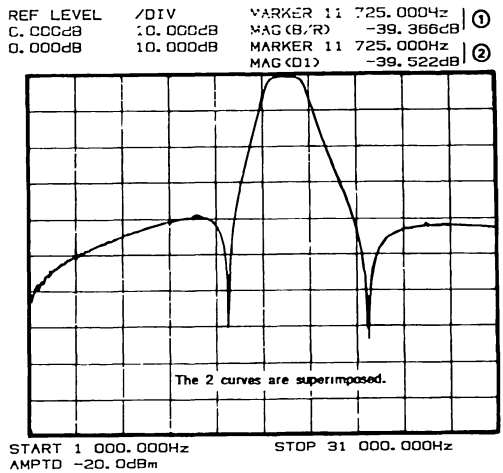
Power Supply : –5V, +5V

Clock Frequency : 307kHz

1– External Clock
2– Free–running Oscillator
R : 2.5kΩ
C : 1nF

E88AN069–28

Figure 28 : RC–Multivibrator Operation (at 847kHz clock frequency).



TSG8550

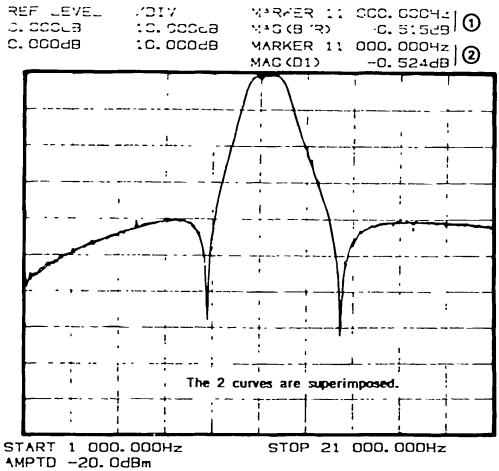
Power Supply : –5V, +5V

Clock Frequency : 847kHz

1– External Clock
2– Free–running Oscillator
R : 2.5kΩ
C : 220pF

E88AN069–29

Figure 29 : Using an External Transistor–based Oscillator (colpitts type).



TSG8550

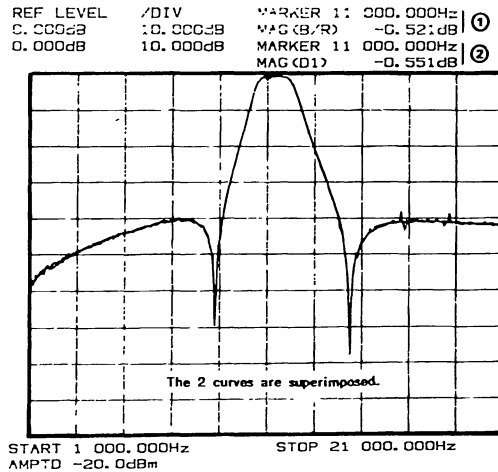
Power Supply : –5V, +5V

Clock Frequency : 540kHz

1– External Clock (TTL)
2– Colpitts Oscillator

E88AN069–30

Figure 30 : Using a Crystal–controlled Oscillator (implemented with an internal op–amp).



E88AN069–31

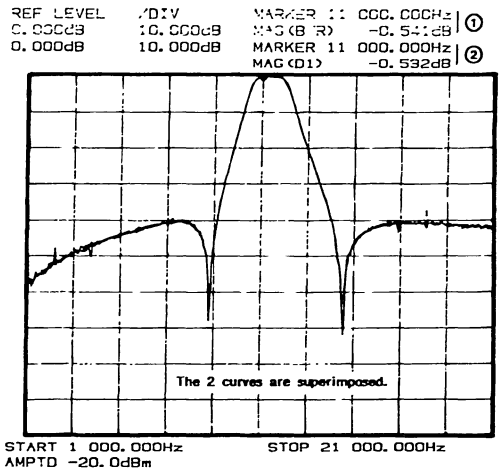
TSG8550

Power Supply : –5V, +5V

Clock Frequency : 540kHz

1– External Clock (TTL)
2– Operational Amplifier
+
Ceramic Resonator

Figure 31 : Operation with Crystal–controlled Oscillator (at 0V, +10V power supply).



E88AN069–32

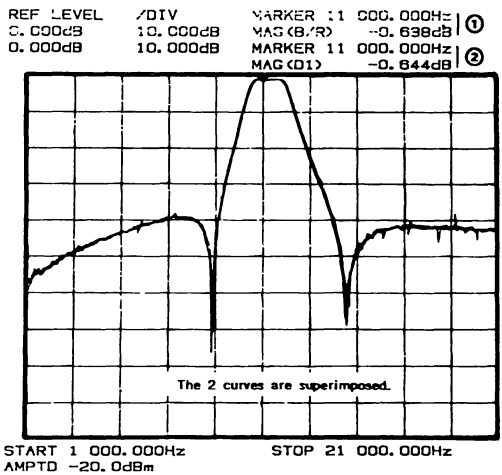
TSG8550

Power Supply : 0V, +10V

Clock Frequency : 540kHz

1– External Clock (TTL)
2– Operational Amplifier
+
Ceramic Resonator

Figure 32 : Operation with Crystal–controlled Oscillator (at 0V, +5V power supply).



E88AN069–33

TSG8550

Power Supply : 0V, +5V

Clock Frequency : 540kHz

1– External Clock (TTL)
2– Operational Amplifier
+
Ceramic Resonator

REGULATED POWER SUPPLIES

Some applications may require a high power supply rejection ratio. This can be achieved by regulating the filter power supply.

The objective of this section is to cover various regulation methods resorting to a minimum number of components.

The subjects discussed are the following :

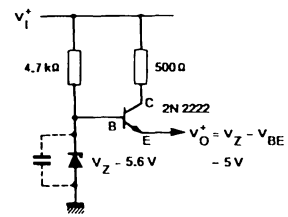
- **Zener Diode Regulation**
- **Regulation using one of the filter's operational amplifiers**

Also, the efficiency of each regulation and its influence on the power supply rejection ratio will be outlined.

ZENER DIODE REGULATION

This is the most straightforward method of voltage regulation. In general, since the current provided by the zener diode is not sufficient, it is consequently impractical to power the device directly by zener voltage. Figure 33a illustrates the solution to overcome this problem.

Figure 33a : Zener Regulation.



E88AN069–34

From the unregulated voltage V^+_I, a stable voltage independent from V^+_I variations is obtained across the zener diode. A voltage follower transistor delivers the current required by the device. The output voltage is : $V_Z - V_{BE}$ and therefore independent from V^+_I. V_{BE} varies as a function of I_E current flowing through the transistor. This variation is almost negligible due to the fact that :

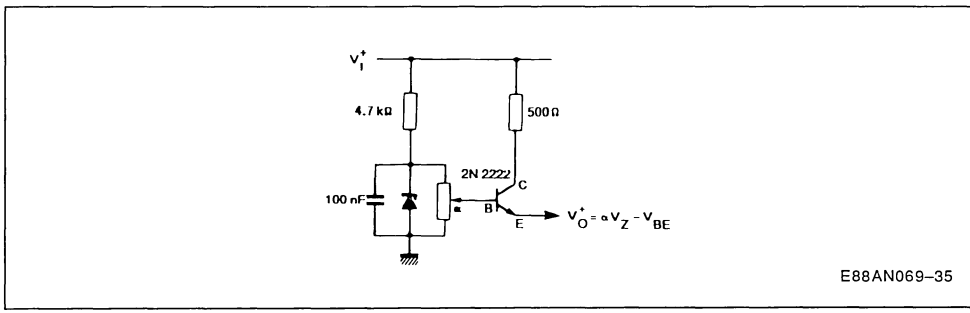
$$V_{BE} = \frac{KT}{q} \log \frac{I_E}{I\alpha}$$

(where $I\alpha$ is the base-emitter junction saturation current), that is, V_{BE} increases by **18mV** when the current doubles. The optional 500Ω resistor limits the current and protects the transistor against possible short-circuits.

A capacitor may be connected across the zener diode so as to filter the noise inherent to this type of diode.

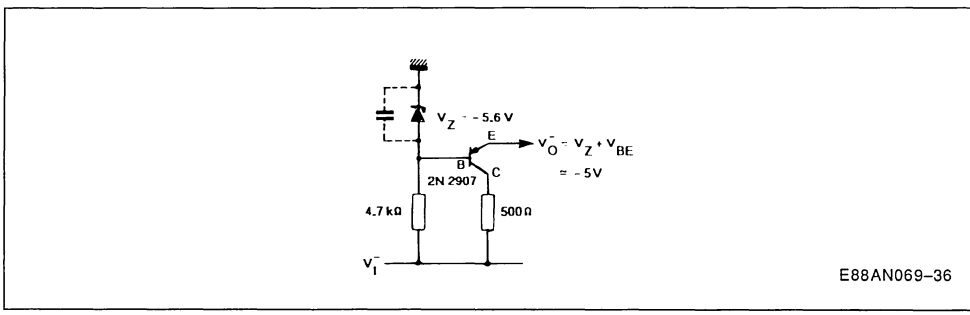
If a variable power supply is required, a potentiometer may be connected across the zener diode as shown in figure 33b.

Figure 33b : Variable Zener Power Supply.



This arrangement is equally applicable to a negative power supply (V^-_I). In this case a PNP transistor is used as shown in figure 33c.

Figure 33c : Negative Zener Regulation.



A symmetrical power supply may thus be implemented using this method.

Note : This type of regulation is not temperature-compensated. One should expect an approximately + 3mV/C drift in output voltage value. Generally, this value is acceptable for the supply of integrated circuits such as SGS-THOMSON Filters.

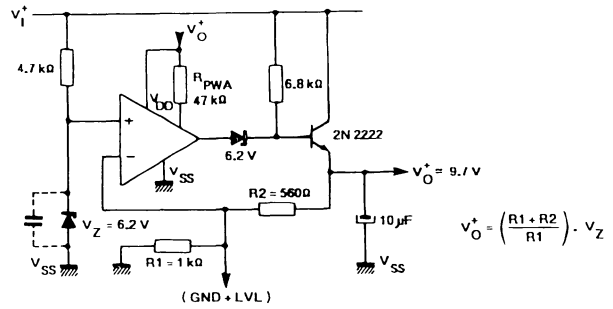
REGULATION USING AN OPERATIONAL AMPLIFIER

With the **M**ask **P**rogrammable **F**ilters (**MPF**), independent and uncommitted operational amplifiers are available to implement functions related to filtering.

One of this amplifiers can be used to achieve power supply regulation as illustrated in figure 34.

This configuration offers an excellent regulation thanks to the high open loop gain of the operational amplifier.

Figure 34 : Power Supply Regulation (using an internal op–amp).



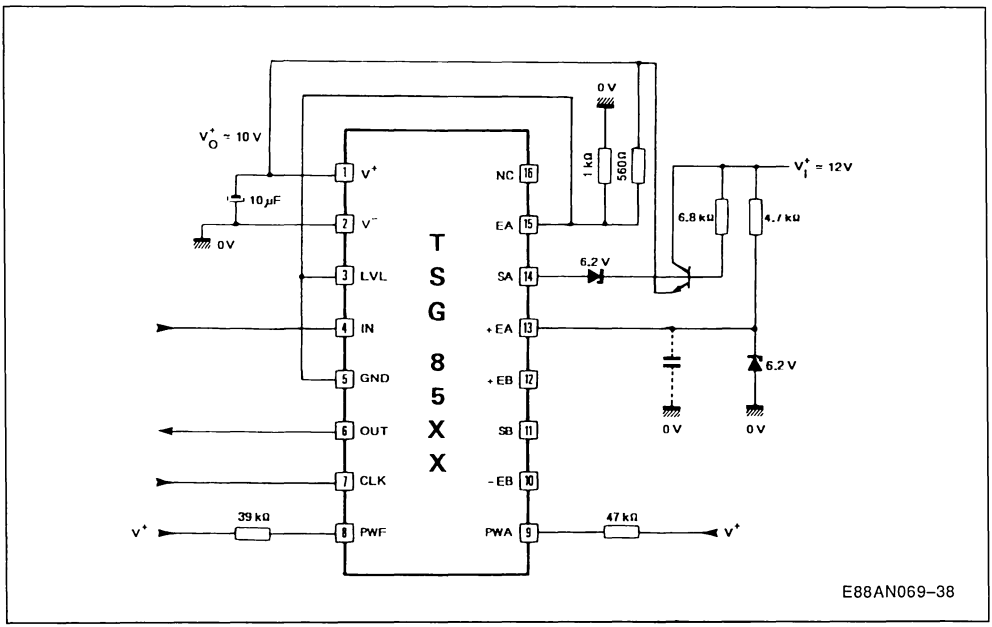
The reference voltage is generated by a zener diode. Since the amplifier is located within the filter package, it is also powered by the regulated output voltage V^+_O. The 6.8kΩ resistor connected between the collector and the base of the ballast transistor ensures start-up. This transistor does not need to be of power type as the output current value remains low. A zener diode connected in series with the amplifier output is necessary to provide for a sufficient voltage excursion to enable the regulation.

The output voltage can be accurately adjusted by setting the values of the bridge elements R1, R2 and using the relationship :

$$V^+_O = \left(\frac{R1 + R2}{R1} \right) - V_Z$$

The regulation performed following this procedure, takes into account both, the input voltage "V_I" and the "**load variations**". This power supply is therefore particularly suitable for complete applications built around SGS-THOMSON' MPFs.

Figure 35 : Filter with Single Power Supply Regulation.



A symmetrical regulated power supply can be implemented using the other operational amplifier of the filter circuit to perform negative supply regulation. One can obviously use the previous configuration and adapt the arrangement to negative voltage while also replacing the NPN ballast transistor by a PNP type.

Figure 36 illustrates the appropriate solution. The objective is to obtain two regulated V^+_O and V^-_O voltages with their absolute values as close to each other as possible. The positive regulated voltage V^+_O is obtained using the configuration described earlier. The negative voltage regulation resorts to an additional operational amplifier, operating in unity gain inverting configuration. Since the regulated V^-_O voltage follows accurately the variations of the V^+_O voltage, a unique reference voltage is sufficient.

Figure 36 : Symmetrical Regulated Power Supply.

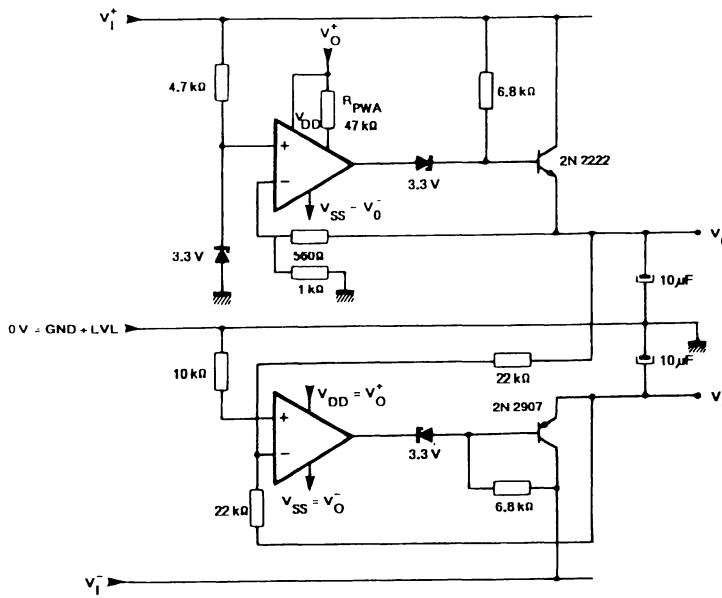
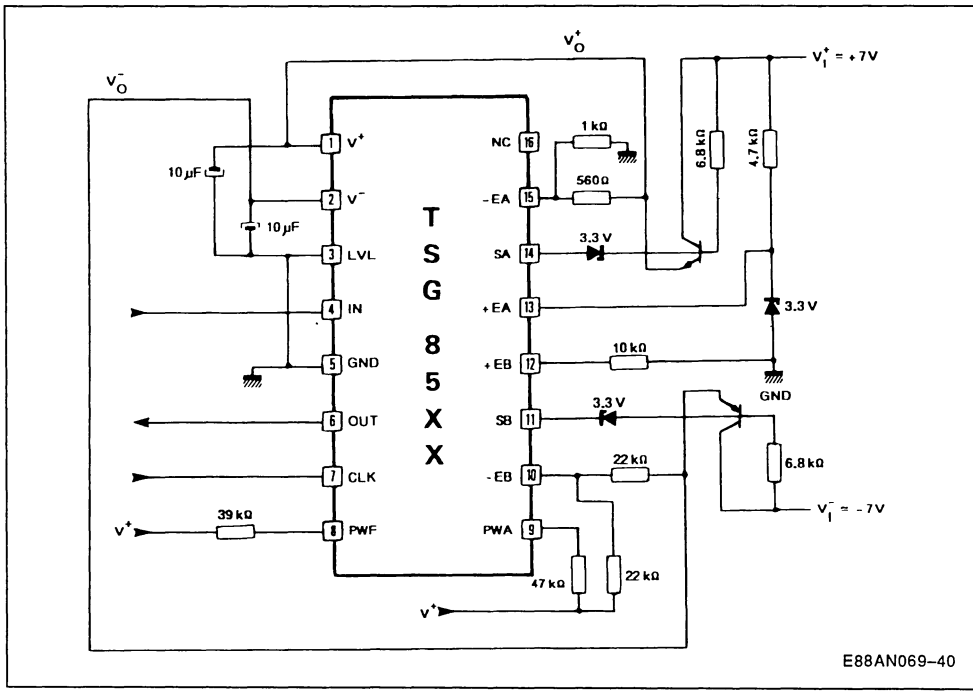
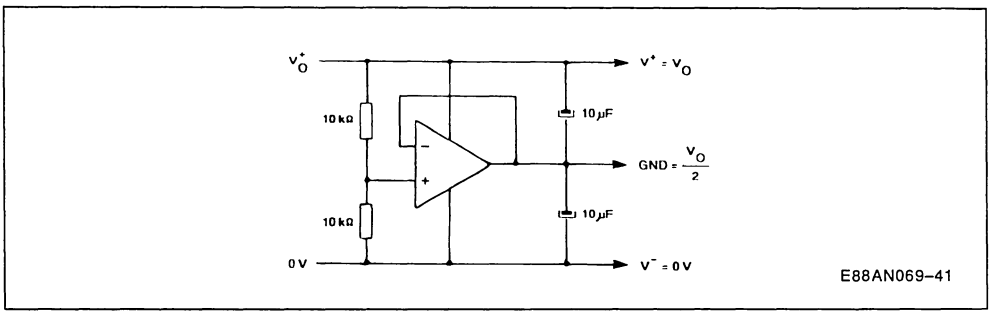


Figure 37 : Filter with Symmetrical Power Supply Regulation.



As shown in figure 38, a symmetrical power supply can be built using, a single regulated power supply, a resistor bridge and an operational amplifier configured as voltage follower. The symmetrical accuracy of this configuration is determined by the precision of the bridge.

Figure 38 : Split Power Supply.



Note : This configuration can be simplified by replacing the operational amplifier with a transistor operating as voltage follower. In this case, the resistor bridge must be readjusted taking into consideration the voltage shift due to the transistor base-emitter voltage drop.

POWER SUPPLY REJECTION RATIO

Figures 39 thru 44 given at the end of this section in paragraph 5.5 depict supply rejection characteristics of the **TSG8550** filter.

It is seen that in general V^- rejection ratios are approximately - 10dB less than those measured for V^+ supply.

A single power supply filtering capacitor (electrolytic) located close to the device will appreciably improve the rejection ratio (approximately – 15dB reduction).

A zener diode used for regulation will further improve the results and with the addition of filtering capacitor, one can obtain excellent results (up to – 60dB).

The method of using a voltage follower transistor following the zener diode results in an improved rejection ratio compared to the rejection ratio obtained with a zener diode without filtering. Note that the quality of the zener diode used has a significant influence on the results - e.g. the rejection ratios obtained using a 5.6V zener diode are much better than those obtained using a 4.7V zener diode. This is due to the fact that the 5.6V zener diodes exhibit a much steeper breakdown characteristics.

Finally, the symmetrical voltage regulator using operational amplifiers discussed earlier (figure 36) yields an excellent rejection ratio of less than - 60dB. It is a difficult task to further improve this ratio as at lower values, other sources of noise will be also measured.

CONCLUSION

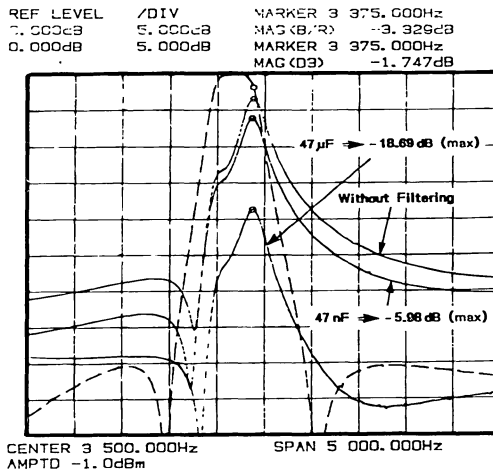
To improve power supply rejection ratio, supply voltage filtering by capacitor or using a zener diode are simple and efficient solutions.

In addition, if perfect power supply regulation for an application built around a SGS-THOMSON' MPF is also required, it would then be interesting to implement the regulator using the operational amplifiers available within the filter package.

SUPPLY REJECTION CHARACTERISTICS OF TSG8550 FILTER

The response curve of TSG8550 is drawn on each plot with a dotted line trace.

Figure 39 : V^+ Rejection Ratio (with a single filtering capacitor).



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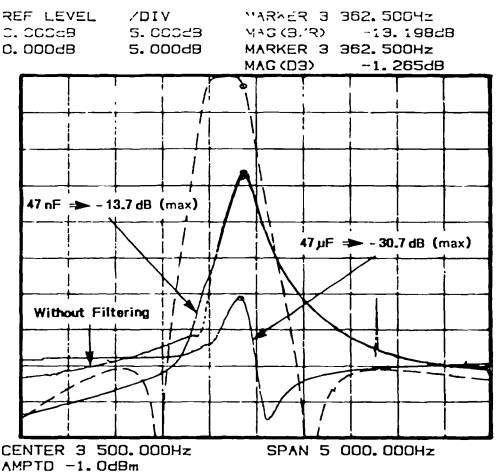
TSG8550

Symmetrical Power Supply : ± 5V

f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

Figure 40 : V^- Rejection Ratio (with a single filtering capacitor).



TSG8550

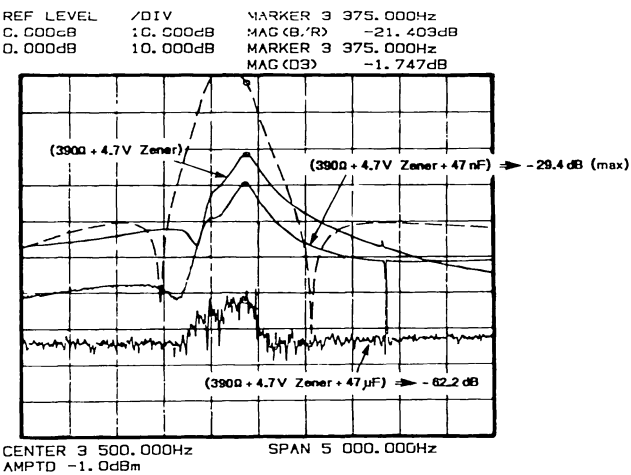
Symmetrical Power Supply : ± 5V

f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

E88AN069-43

Figure 41 : V^- Rejection Ratio (with a zener diode and a filtering capacitor).



TSG8550

Symmetrical Power Supply : ± 5V

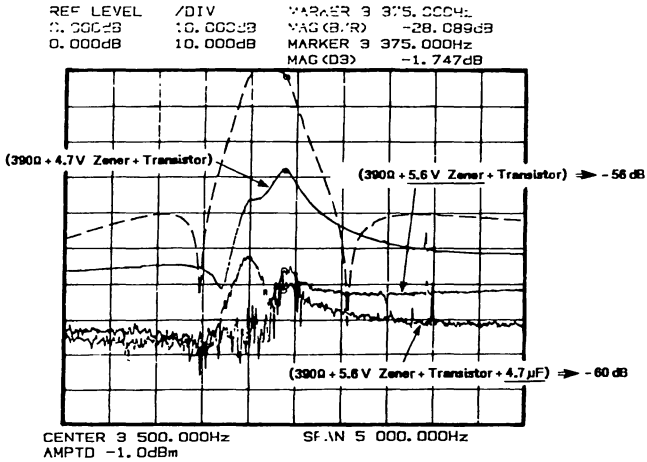
f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

E88AN069-44

E88AN069-44

Figure 42 : V^+ Rejection Ratio (with a zener diode and a transistor).



TSG8550

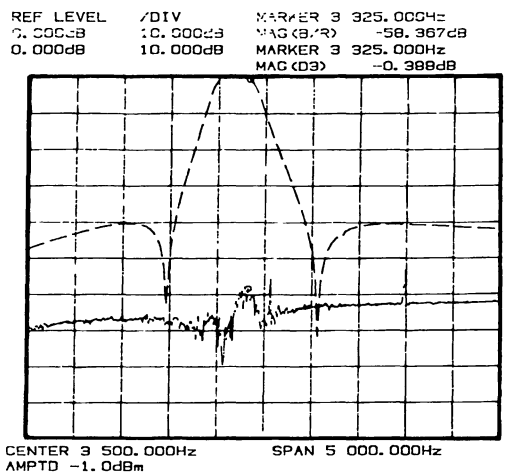
Symmetrical Power Supply : ± 5V

f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

E88AN069–45

Figure 43 : V^+ Rejection Ratio (operational amplifier symmetrical regulator) [filtering capacitor : 33µF].



TSG8550

Symmetrical Power Supply : ± 5V

f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

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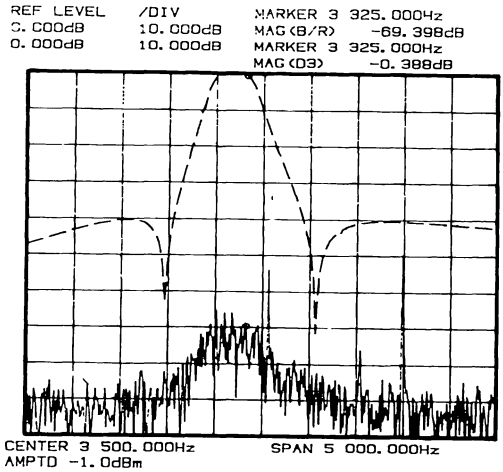
Figure 44 : V⁻ Rejection Ratio (operational amplifier symmetrical regulator).



E88AN069-47

TSG8550

Symmetrical Power Supply : ± 5V

f_e : 150kHz

R_{PWF} : 39kΩ (grounded)

WIRING RECOMMENDATIONS

This last section details the practical application considerations applicable to SGS-THOMSON range of **Switched Capacitor Filters**. The discussion will enable the designer to attain remarkable performances and to obtain in particular excellent signal-to-noise ratio.

Layout rules are sub-divided into 3 important sections :

- **Power supply decoupling**
- **Ground connections**
- **Operational amplifiers layout considerations**

POWER SUPPLY DECOUPLING

Power supply voltages "V^+" and "V^-" as well as "LVL" pin voltage (that in order to set the output dc level is generally amplified within the device) must be carefully decoupled.

Similarly, in the case of a single power supply operation, the dc voltage applied to "**Ground**" (GND) pin must be efficiently decoupled.

For decoupling purposes, one can use a high quality capacitor located very close to the filter package pin under consideration (V^+, V^-, LVL or GND). A capacitor of a few tens of nF will suffice.

Also, decoupling PWA and PWF pins will improve the signal-to-noise ratio. These pins determine the biasing current of, either operational amplifiers, or the filter and consequently have an influence on the overall device performance.

A capacitor of approximately **30pF** coupled to **PWF** pin and connected in parallel with the filter biasing resistor R_{PWF}, will in particular, prevent the occurrence of the so called "**clock feedthrough**" phenomenon. Clock feedthrough is defined as the "presence of the clock frequency harmonics at the filter output" and can give rise to disturbances within the stop band region.

GROUND CONNECTIONS

Conventional printed circuit board layout rules must be respected.

Ground connections must be wide enough to avoid occurrence of stray resistances that can cause ground pin (GND) voltage to fluctuate as a function of the current flowing through ground connections.

Star connection, starting from the GND pin and going to various application ground terminals, must be used as often as possible.

Particular attention must be paid to appropriate separation between the filter proper ground and the ground of complementary functions (clock, amplifier, comparator, ..) built using the on-chip operational amplifiers.

OPERATIONAL AMPLIFIERS LAYOUT CONSIDERATIONS

The two operational amplifiers available within the filter package are generally used for building anti-aliasing and smoothing filters connected to the switched capacitor filter input and output terminals.

Consequently, connections such as : common ground, too close p c board adjacent tracks, etc.. - susceptible to cause interaction between input and output signals, must be avoided.

Non-inverting terminals (+E) need special precaution. In fact, these inputs are of high impedance type and located next to each other in standard filter pinout configurations. In the case of standard Sallen-Key cells performing anti-aliasing and smoothing functions, since the filter input and output signals are routed via these two inputs, there will be risk of interaction between the signals. Therefore, tracks connecting to +E inputs must be separated by as much as possible and the capacitor values of the Sallen-Key Cell must be selected large enough so as to minimize the loading impedance on these pins. Low value resistors are used to achieve the latter requirement - R = 10k will in general enable the selection of suitable capacitor values.

CONCLUSION

Excellent application performances using SGS-THOMSON Microelectronics **Switched Capacitor Filters** will be obtained by observing the foregoing rules and recommendations.

Information contained in this application note is **applicable to any of the standard and semicustom filters** ; i.e. **the entire range of Mask Programmable Filters.**

BAND–PASS AND BAND–STOP FILTERS

INTRODUCTION

Standard switched capacitor filters currently marketed by SGS-THOMSON Microelectronics cover in particular a range of **Band-pass** and **Band-reject** filters - all of which have in general a high selectivity factor.

One may require to implement a band-pass or band-stop filter of lower Q figure.

The objective of this application note is just to demonstrate how such requirement is fulfilled by using **one low-pass** and **one high-pass standard filters.**

Throughout our discussion, we shall outline and illustrate, once again, the remarkable flexibility of use inherent to switched capacitor filters.

Subjects covered are :

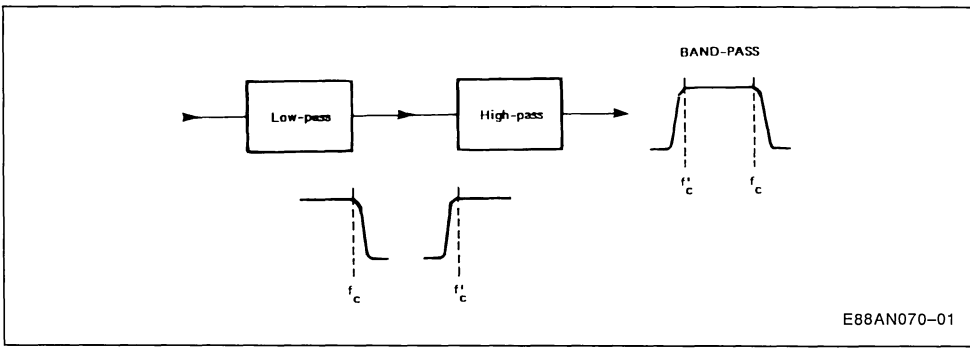
- 1 - **Band-pass Filters**
- 2 - **Band-stop or Band-reject Filters**

BAND-PASS FILTERS

FILTER SYNTHESIS FUNDAMENTALS

Cascaded combination of **one low-pass** and **one high-pass** filters yields a **band-pass** filter.

Figure 1 : Band–Pass Filter Fundamentals.



Note however that in this arrangement the low-pass filter precedes the high-pass filter so as to limit the signal frequency band as it enters the first stage, thus improving the signal-to-noise ratio.

Switched capacitor filters manufactured by SGS-THOMSON are active filters having a **high input** and a **low output impedances** of typically **"3MΩ"** and **"10Ω"** respectively, thus making them particularly suitable for cascaded combination - by coupling the output of one to the input of the other.

The following standard filters are employed throughout the present section :

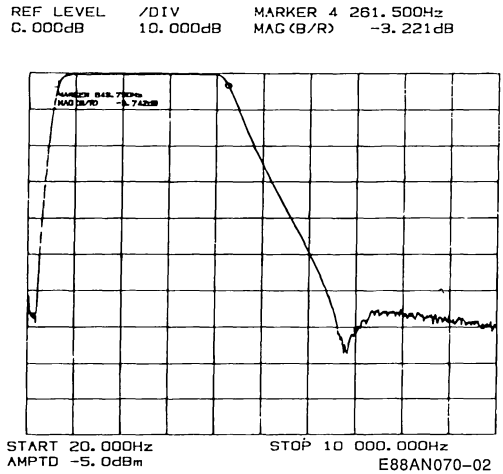
- **TSG8512** : 7th order Cauer-type low-pass filter
- **TSG8532** : 6th order Chebychev-type high-pass filter

Obviously, other standard filters may be cascaded according to requirements.

USING A COMMON CLOCK

Figure 2 depicts the frequency response of the two filters put in cascade and operating at an identical clock frequency of 400kHz.

Figure 2 : Band–Pass Filter Frequency Response.



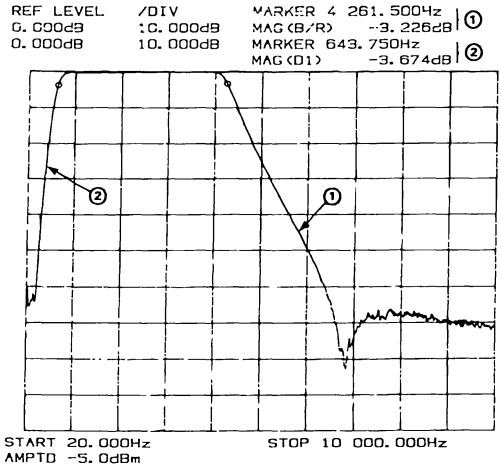
BAND–PASS FILTER

TSG8512
+
TSG8532

"Identical Clock Frequency : 400kHz"
(without anti–aliasing & smoothing filters)

It is clearly seen that there is no significant difference between this curve and the curves of figure 3 illustrating the frequency response of the filters operating separately but at the same 400kHz clock frequency.
It is thus obvious that direct cascading of the filters does not affect the operating characteristics of the either filter.

Figure 3 : Frequency Response of Low–Pass (TSG8512)& High–Pass (TSG8532) Filters [common clock frequency : 400kHz].

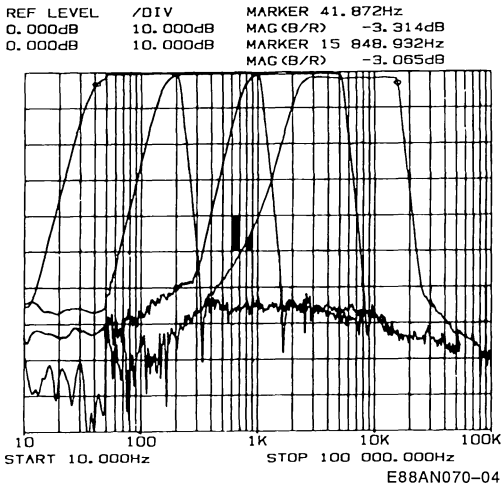


①
TSG8512 (low–pass filter)
"Clock Frequency : 400kHz"

②
TSG8532 (high–pass filter)
"Identical Clock Frequency : 400kHz"

Figure 4 outlines the interesting characteristics of a band–pass filter implemented as discussed above.

Figure 4 : Frequency Range Shifting of Band–Pass Filter.



E88AN070–04

Figure 4 illustrates how by simple modification of the common clock frequency, the frequency range of the band-pass filter is shifted without causing any modification to its frequency response curve.

Due to inherent characteristics of the switched capacitor filters, the clock to cut-off frequency ratio is always known. It is thus a simple matter to calculate the clock frequency as a function of the signal frequency one wishes to use.

For example, in the case of **TSG8512** filter, this ratio is :

$$\frac{f_e}{f_c} = 100 \pm 1\%$$

Where f_e is the **external clock frequency**.

If f_c is to be the **upper cut-off frequency** equal to **5kHz**, we shall therefore select f_e **= 500kHz.**

Also, since $\frac{f_e}{f_c}$ **= 500** ±1% for **TSG8532**, the **lower cut-off frequency f'c** will be **1kHz**.

This curve is given in figure 4.

Note that in all cases, the passband width remains constant at **4 x f'c.**

Different bandwidths are obtained by cascading other standard filter types.

Corresponding calculations are similar to those outlined above.

TWO DIFFERENT CLOCK FREQUENCIES (figure 5)

Figure 6 depicts the frequency response of a band-pass filter implemented by cascading TSG8512 and TSG8532 filters but each operating at a different frequency.

Similar to the former case, it is obvious that the frequency response characteristics of the individual filters are not modified by this configuration and remain unchanged after cascading.

Note however that in this case, the signal delivered at the output of the first filter (TSG8512) goes through a smoothing filter before entering the second filter (TSG8532).

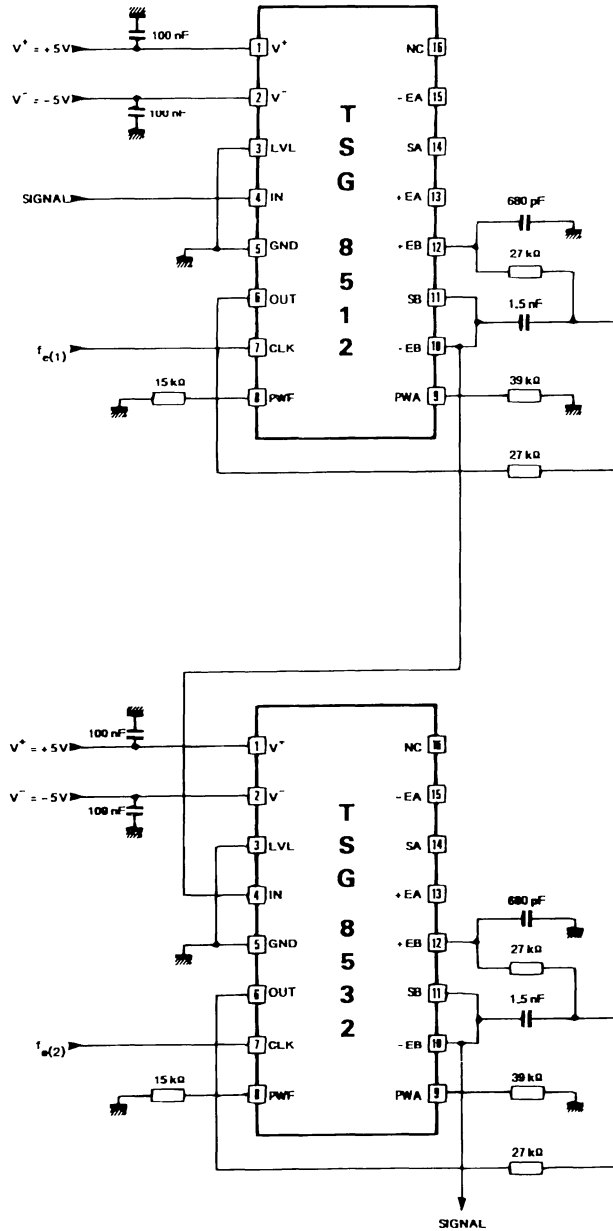
This process is necessary as the operating frequencies of the filters are different and consequently there will be lack of synchronization between the sampling performed by each individual filter.

In the absence of the signal smoothing process, this fact will give rise to disturbances within the cut-off frequency band.

Similarly, the signal delivered by the second filter goes through a smoothing filter.

These smoothing filters are implemented by **2nd order Sallen-Key** Cells each using one of the on-chip operational amplifiers of the switched capacitor filter (figure 5).

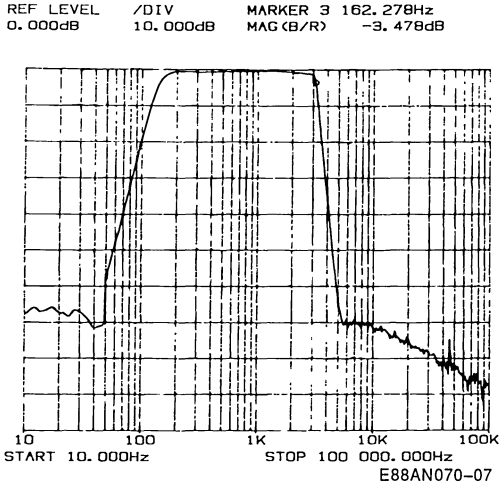
Figure 5 : Band–Pass Filter (two separate clocks).



E88AN070–05

The cut-off frequency of these Sallen-Key Cells is chosen to be twice the upper cut-off frequency of the band-pass filter so as to eliminate any signal disturbance within the pass band region.

Figure 6 : Low Q Band–pass Frequency Response Characteristics.



E88AN070–07

BAND–PASS FILTER

"Two different clock frequencies"

TSG8512 "Clock : 300kHz"

+

TSG8532 "Clock : 90kHz"

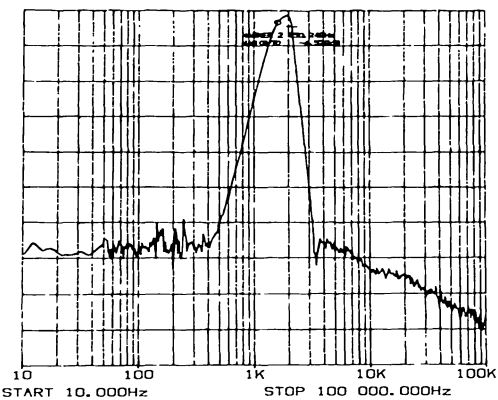
+

Anti–aliasing & Smoothing Filters

(f_c = 6kHz)

Figure 7 illustrates how the cascading of two filters yields an extremely steep band-pass characteristics.

Figure 7 : Steep Band–pass Frequency Response Characteristics.



E88AN070–08

STEEP BAND–PASS

TSG8512 "Clock : 200kHz"

+

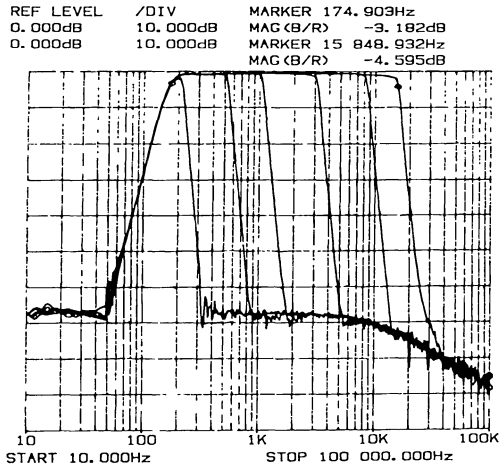
TSG8532 "Clock : 800kHz"

The band-pass obtained in this case has a selectivity factor of about 4.

Note that the clock frequencies employed (200kHz and 800kHz) allow the use of a single external oscillator running at 800kHz (or its multiple frequencies). The second clock frequency is then derived from this master clock using a counter.

In figures 8 and 9, one of the clock frequencies is maintained constant while the other is varied. This arrangement results in an adjustable band-pass filter.

Figure 8 : Shifting the Upper Cut–off Frequency.



E88AN070–09

BAND–PASS FILTER

TSG8512

+

TSG8532

With Anti–aliasing & Smoothing Filters

TSG8532 "Fixed clock : 100kHz"

TSG8512 "Variable clock :"

→ 20kHz

→ 50kHz

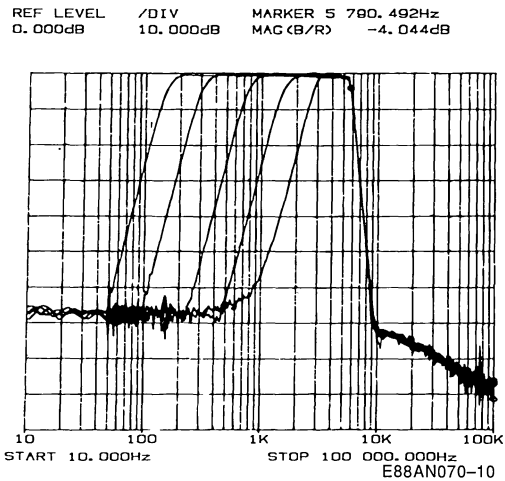
→ 100kHz

→ 300kHz

→ 800kHz

→ 1.5MHz

Figure 9 : Shifting The Lower Cut–off Frequency.



E88AN070–10

BAND–PASS FILTER

TSG8512 "Fixed clock : 540kHz"

TSG8532 "Variable clock :"

→ 100kHz

→ 200kHz

→ 500kHz

→ 1MHz

→ 2MHz

Each cut-off frequency is adjusted with precision and if separate clocks are used, adjustments will be entirely independent.

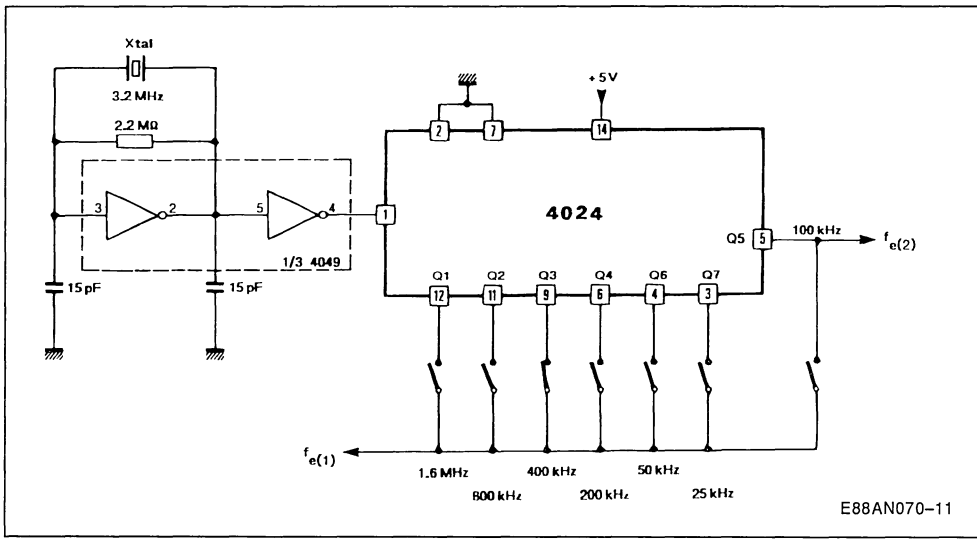
If separate clocks are not available, one may use a single master oscillator and then derive the required frequencies using a frequency divider circuit.

In this case, the frequencies would be the multiples of one another.

By appropriate selection of the division factor, the frequency bandwidth is changed.

The filter frequency response curve is readily shifted along the frequency axis by simple modification of the master oscillator frequency (figure 10).

Figure 10 : Clock Generation for Adjustable Band–pass (deriving two different clock frequencies from a master oscillator).



Illustrated example gives identical results to those depicted in figure 8.

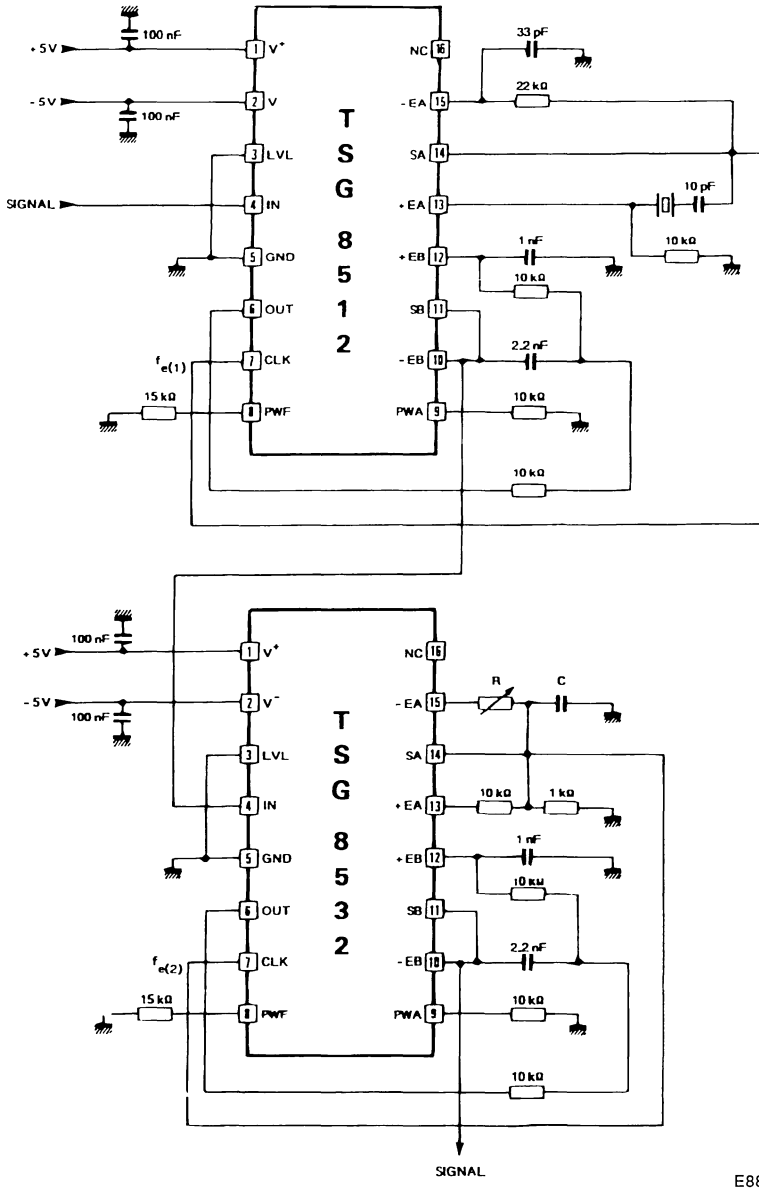
According to requirements, a single 4-bit 74163 TTL-type counter may be used as frequency divider.

For adjustable band-stop filter, either a 4020-type 14-stage counter or a 4060-type counter that also includes an on-chip crystal oscillator would be suitable alternatives.

To implement an appropriate oscillator, refer to the **"Application Note : AN-069" [A Supplement to the Utilization of Switched Capacitor Filters]** that discusses in detail how to build crystal-controlled and free-running oscillators using the on-chip operational amplifiers of the filter circuits.

For example, curves depicted in figure 9 may be obtained, in the case of TSG8512, using the ceramic resonator discussed in the application note mentioned above - and in the case of TSG8532, by adjusting the frequency of a free-running oscillator whose frequency is varied by a potentiometer as illustrated in figure 11.

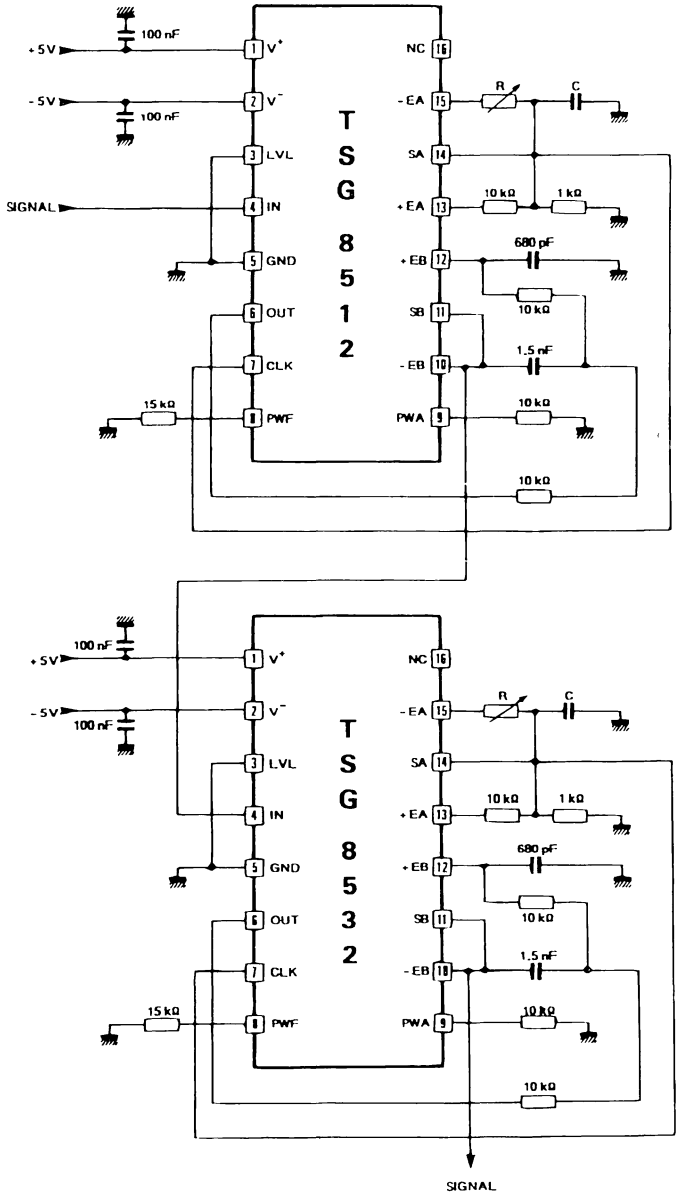
Figure 11 : Adjustable Band–pass Filter (upper cut–off frequency set by crystal–controlled oscillator).



A band-pass filter is thus implemented using only 2 switched capacitor filters of SGS-THOMSON configured as active elements.

A wide frequency adjustment range is available using RC-type free-running relaxation oscillators (figure 12).

Figure 12 : Adjustable Band–pass Filter (upper and lower cut–off frequencies are both adjustable).

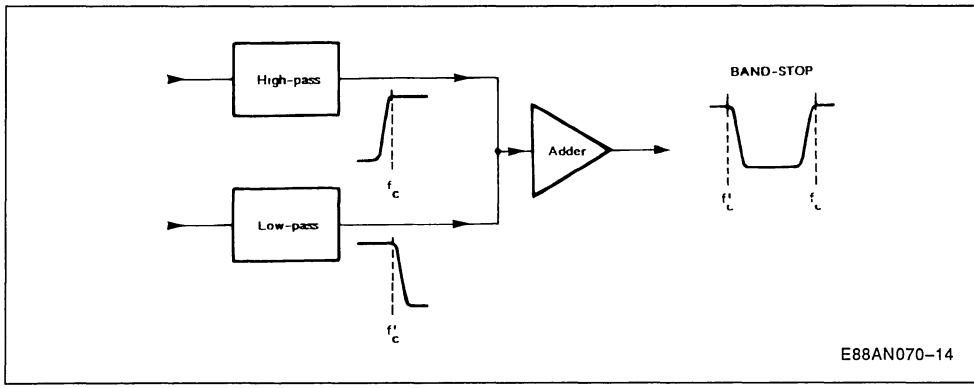


In order to obtain excellent performances and specially to improve the signal-to-noise ratio, addition of anti-aliasing and smoothing filters suited with the upper cut-off frequency of the band-pass is also necessary.

BAND–STOP FILTERS

FILTER SYNTHESIS FUNDAMENTALS (figure 16)

Figure 13 : Band–stop Filter Fundamentals.



A band-stop filter is obtained by adding the output signals of a high-pass and a low-pass filter.

The adder circuit is configured using an operational amplifier.

In the case of SGS-THOMSON switched capacitor filters, the adder circuit is readily implemented using one of the operational amplifiers contained in the same package as the filter circuitry. It is thus clear that only two packages, one low-pass and the other high-pass, are required to implement a band-stop filter.

An adder is built using either of the configurations given below :

Figure 14 : Inverting Adder.

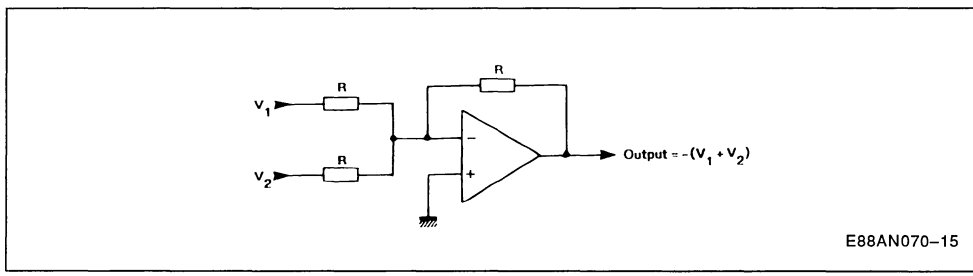


Figure 15 : Non Inverting Adder.

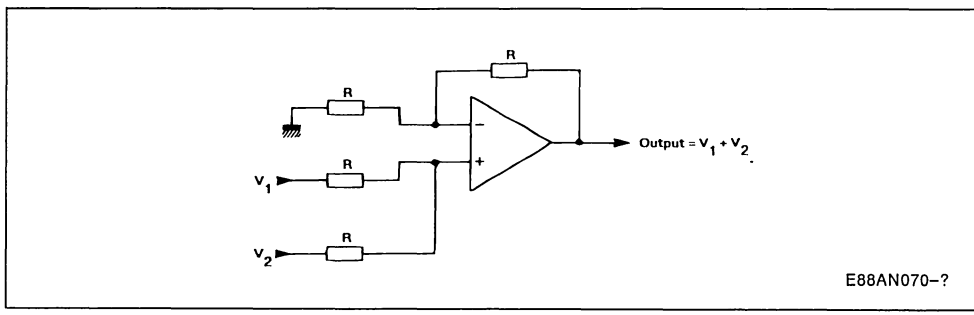
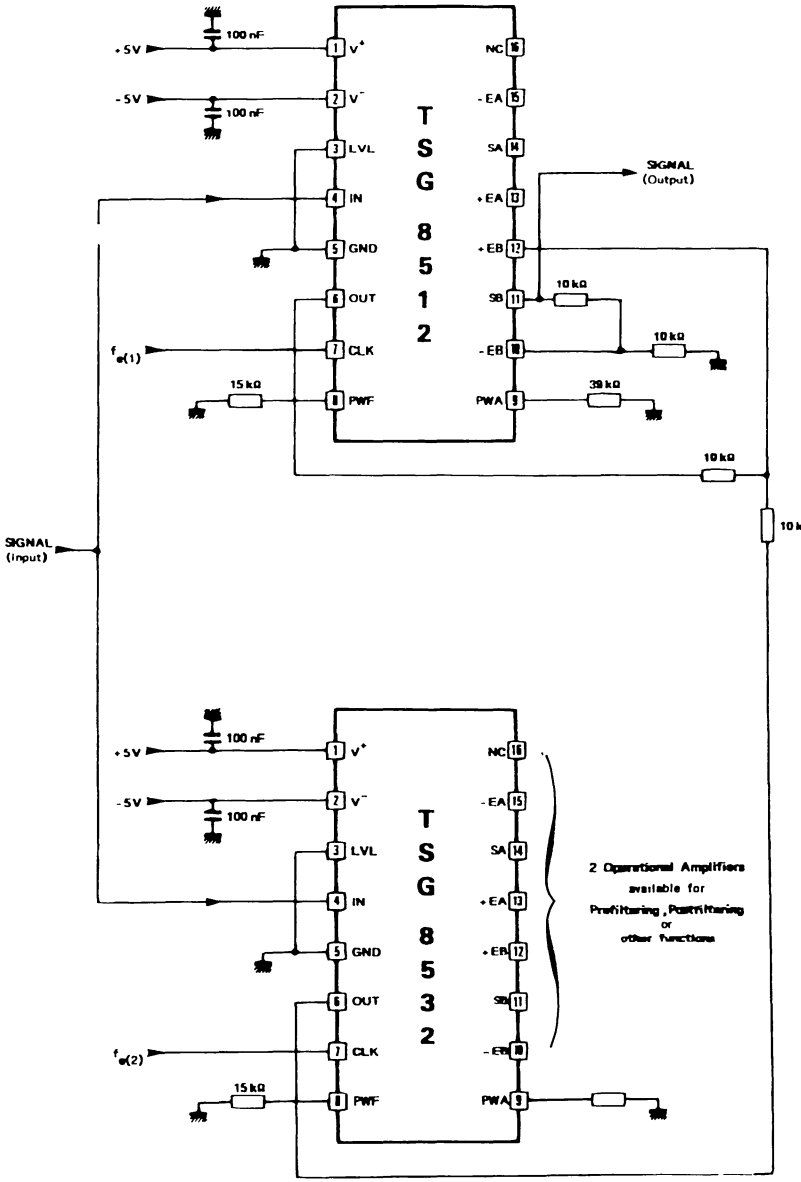


Figure 16 : Band–Stop Filter (two separate clocks).



E88AN070–16

RESULTS

Similar to band-pass discussion, the standard devices employed here are :

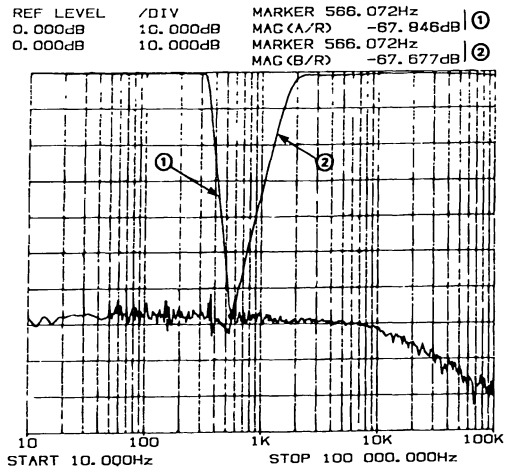
TSG8512 : Low-pass

TSG8532 : High-pass

Other standard circuits can be used according to the desired cut-off frequency slope and attenuation.

Figure 17 depicts the response curves of the individual filters.

Figure 17 : Frequency Response of Low–pass & High–pass Filters.



E88AN070–17

① *** LOW–PASS FILTER**

TSG8512 "Clock : 32kHz"

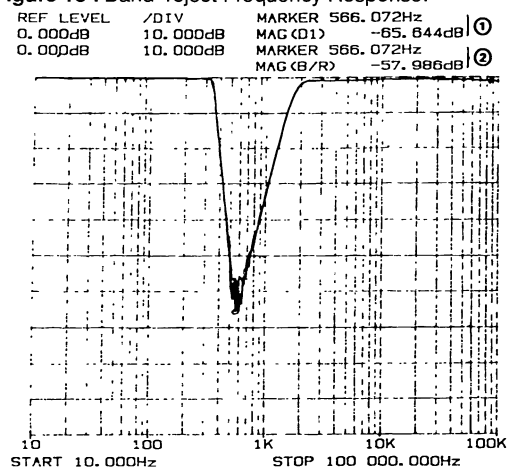
② **HIGH–PASS FILTER**

TSG8532 "Clock : 1.170MHz"

Figure 18 illustrates the frequency response curve of the band-stop filter built using these two filters operating at the same frequency as previously.

Once again, it is obvious that the operating characteristics of each filter remain unaffected by this arrangement. The response curve is obtained directly from figure 17.

Figure 18 : Band–reject Frequency Response.



E88AN070–18

BAND–REJECT FILTER

TSG8512 "Clock : 32kHz"

+

TSG8532 "Clock : 1.170MHz"

① **With non–inverting Adder**
(filter op–amp R_{PWA} = 39kΩ)

② **With inverting Adder**
(filter op–amp)

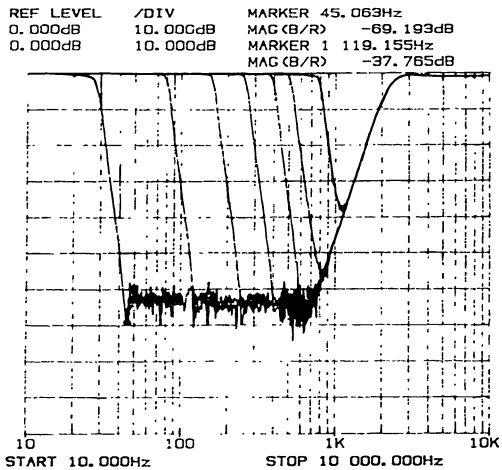
Also, there is no significant difference between an inverting and a non-inverting adder (except for output signal phase inversion).

For our present discussion, from now on, we shall use non-inverting adder arrangement. The configuration will therefore be identical to that given in figure 16 ; that illustrates how a band-stop filter is readily built using two switched capacitor filters.

In figures 19 and 20, the clock frequency of one filter is constant while the other is adjustable.

The outstanding flexibility of such band-stop filter is clearly demonstrated by observing the fact that the adjustment of one filter has no influence whatsoever on the other.

Figure 19 : Shifting the Lower Cut–off Frequency.



E88AN070–19

As discussed earlier, refer to section concerning **Oscillators** (Application Note : **AN-069**) for details on how to implement the appropriate clock circuits.

One of the operational amplifiers available may be used to build crystal-controlled or RC-type variable oscillators.

Electrical diagrams of these oscillators are identical to those given in figures 11 and 12.

Similarly, if clock frequencies are multiples of each other, a single master oscillator and frequency divider combination may be used.

Any modification of the master frequency will shift the filter response curve along the frequency axis (see figure 10).

BAND–STOP FILTER

TSG8532 "Fixed Clock : 1.5MHz"

+

TSG8512 "Variable Clock :"

→ 2.5kHz

→ 7.5kHz

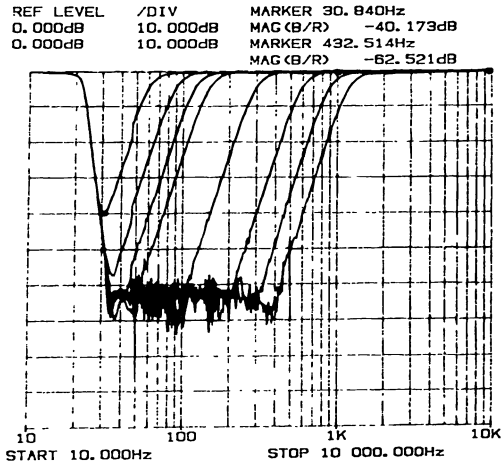
→ 15kHz

→ 25kHz

→ 50kHz

→ 70kHz

Figure 20 : Shifting the Upper Cut–off Frequency.



E88AN070–20

BAND–STOP FILTER

TSG8512 "Fixed Clock : 2kHz"
+
TSG8532 "Variable Clock :"
→ 40kHz
→ 60kHz
→ 80kHz
→ 100kHz
→ 200kHz
→ 400kHz
→ 600kHz
→ 800kHz

BAND-REJECT FILTERS (figure 21)

An interesting application of band-stop filters is implementation of frequency-reject filters, i.e. steep band-stop filters.

For this application, a low-pass TSG8512 and a high-pass TSG8531 filters are used. The **TSG8531** is a standard **6th order Cauer-type high-pass** filter and was chosen for this application due to its sharp cut-off characteristics.

Figure 21 : Band–reject Filter (adjustable center frequency).

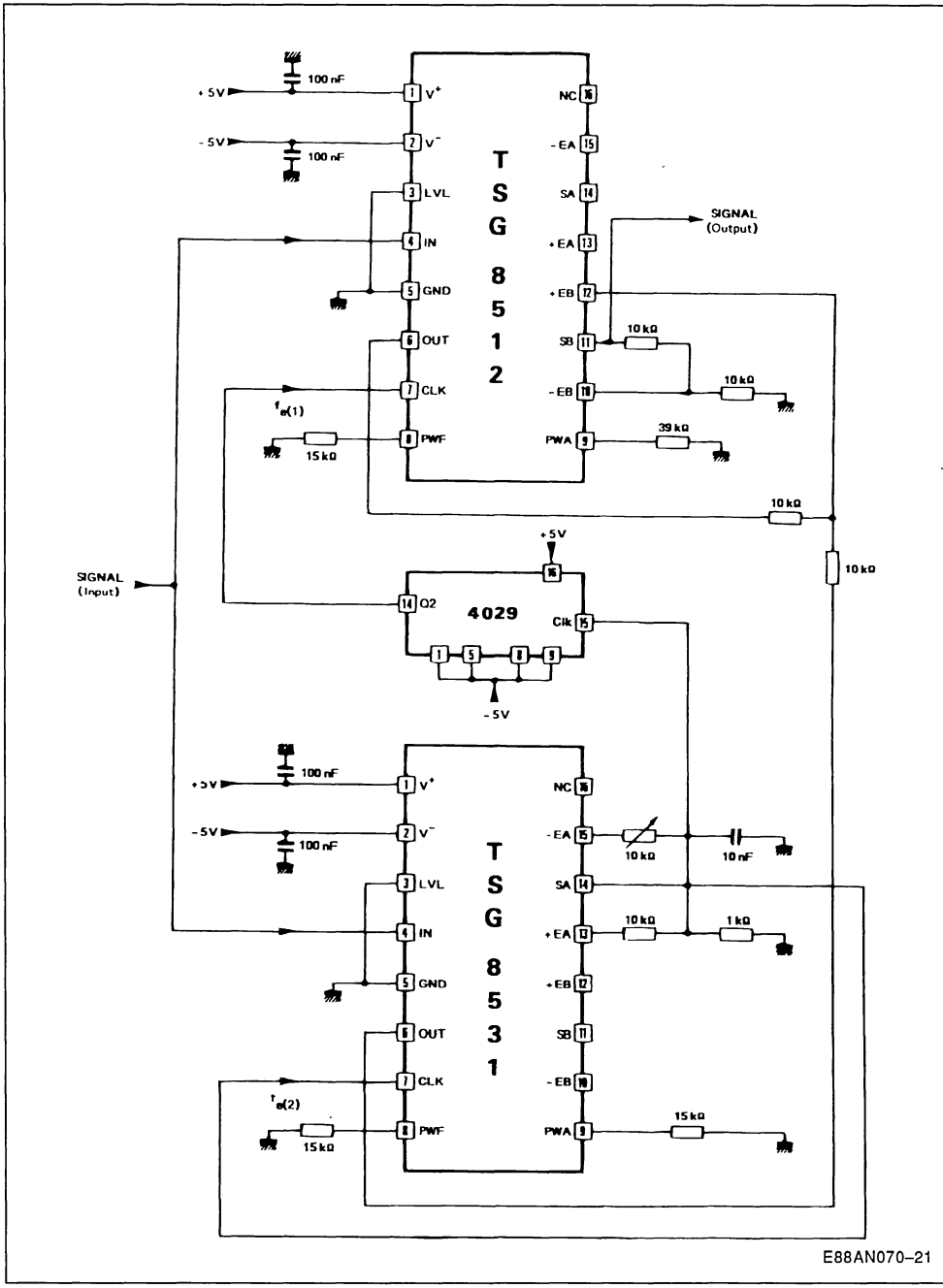
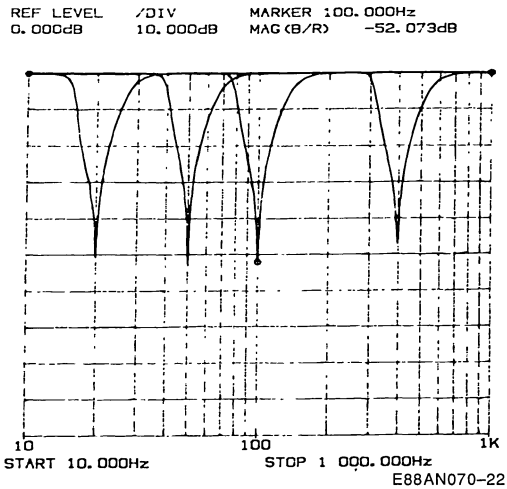


Figure 22 shows response curves obtained at different center frequencies.

Figure 22 : Shifting the Frequency Response of Band-reject Filter.



BAND-REJECT
TGS 8512 + TSG 8531
For different **center frequencies :**
20Hz, 50Hz, 100Hz, 400Hz
The two clock frequencies have a
Constant ratio of 10

The frequency ratio of the clocks was selected to be constant and equal to 10.

This allows use of a single oscillator followed by a frequency divider.

Figure 21 illustrates the electrical diagram of this band-reject filter.

This type of band-reject filter is generally employed for the suppression of mains frequency transients, i.e. 50Hz or 60Hz.

In this case, the application characteristics are as follows :

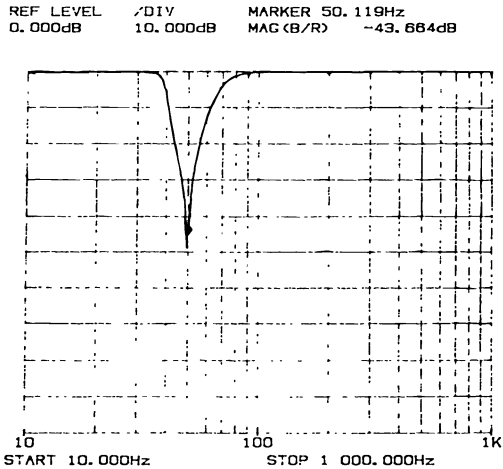
50Hz center frequency :

TSG8531 filter clock frequency : 36kHz
TSG8512 filter clock frequency : 3.6kHz
Selectivity Factor : Q 1.6
Attenuation at 50Hz : 45dB

60Hz center frequency :

TSG8531 filter clock frequency : 43kHz
TSG8512 filter clock frequency : 4.3kHz
Selectivity Factor : Q 1.6
Attenuation at 60Hz : 48dB

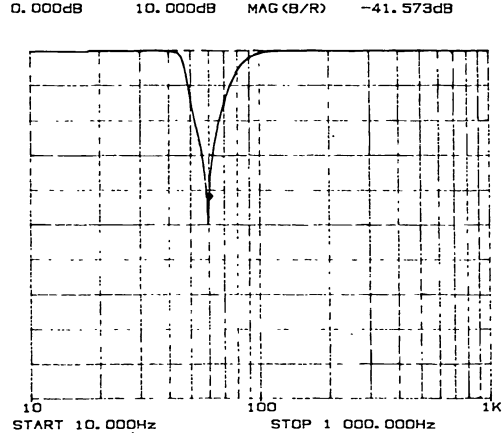
Figure 23 : 50Hz Band-reject Filter Frequency Response.



E88AN070-23

50Hz REJECT
TGS 8512 "Clock : 3.6kHz"
+
TSG 8531 "Clock : 36kHz"

Figure 24 : 60Hz Band-reject Filter Frequency Response.



E88AN070-24

60Hz REJECT
TGS 8512 "Clock : 4.3kHz"
+
TSG 8531 "Clock : 43kHz"

SWITCHED CAPACITOR FILTERS SIGNAL DETECTION & SINEWAVE GENERATION

By Jacques REBERGA

INTRODUCTION

The present note outlines the specifications of high selectivity factor (Q > 1) band-pass filters such as standard **TSG8551** and **TSG8550** devices.

Subjects covered are :

- **Signal Detection**
- **Implementation of a very low distortion sine-wave oscillator.**

These application fields cover a wide range of practical configurations built around the switched capacitor filters - few examples of which will be described in detail.

SIGNAL DETECTION

This section discusses various types of the signal detection techniques and gives an application example of each.

The following topics will be covered successively :

- **Amplitude detection**
- **Frequency detection**
- **Burst duration detection**

The **TSG8551** standard filter is best suited to this type of application. This is a selective band-pass 8th order switched capacitor filter with selectivity factor **Q** equal to **35**. In addition, it has a relatively high gain (30dB typ.) at center frequency. The attenuation within the stop band region is typically 70dB.

Consequent to the foregoing, it is obvious that the **TSG8551** is perfectly suitable for signal detection applications. Since the clock frequency to filter center frequency ratio is constant, the TSG8551 can be accurately locked onto the signal to be detected, by adjusting the external clock frequency.

AMPLITUDE DETECTION

The objective is to measure the amplitude of a given signal selected by the TSG8551 filter.

Irrespective of the signal shape, the filter delivers a sinewave frequency of which corresponds to the filter center frequency. This is particularly useful when measuring a signal super imposed on a carrier or lost within interference signals.

The detected amplitude level depends on the filter gain at center frequency. As specified in technical data sheet, the TSG8551 filter has a fixed gain - guaranteed gain value of **28** to **32dB** at **400kHz clock frequency**.

This application requires an extremely stable "**Quartz** or **Ceramic Resonator**" - controlled clock generator.

In fact, any clock frequency drift will cause center frequency displacement and thus detected signal amplitude variation.

We shall demonstrate in the present application note, how it is possible to lock the clock frequency onto the frequency of the signal to be detected (section 2.1.3).

Filter offset compensation is necessary in order to obtain an error-free measurement of the signal amplitude.

This function is easily implemented using "**LEVEL**" pin of the TSG8551 which controls the output dc level and can therefore be used to bring this level down to zero. Same as for all other SGS-THOMSON Microelectronics switched capacitor filters, an automatic offset compensation feature can be also implemented (refer to application note "AN-069" for detailed discussion of this topic).

SENSITIVITY OF SWITCHED CAPACITOR FILTERS

Minimum signal amplitude detectable by TSG8551 is around 1mV peak-to-peak. Signals of lower amplitude can be processed provided that they go through a pre-amplifier before entering the filter input. The pre-amplifier can be implemented using one of the on-chip operational amplifiers. In this case, the signal level at amplifier input must be at least 100µV peak-to-peak.

RECTIFICATION

In order to measure the amplitude, the signal is generally first rectified (half- or full-wave rectification).

Once again, the on-chip operational amplifiers can be used to perform this task.

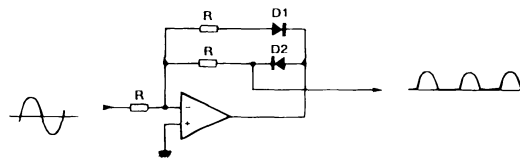
HALF-WAVE RECTIFICATION

Figure 1 illustrates the operating principles of this rectifier.

Figure 1 : Half–Wave Rectification Principles.

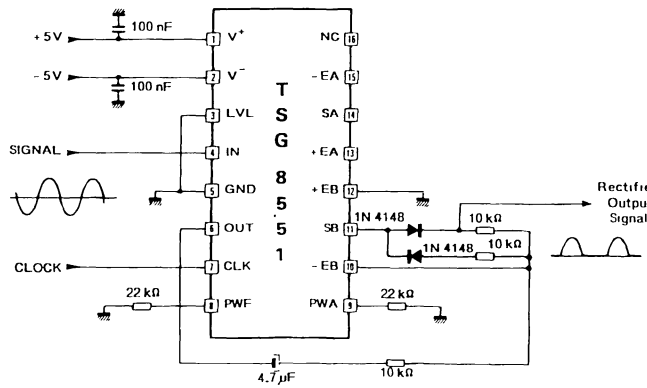
Diode D1 conducts during the input signal positive half cycle while diode D2 is reverse biased and there is therefore no signal at the output.

During the negative half cycle, diode D1 is reverse biased and diode D2 conducts - the amplifier operates in unity gain inverting configuration and consequently inverts the negative going input signal and delivers a positive output signal.



The gain of this configuration can be set by adjusting the value of the feed-back resistor - thereby allowing signal amplification if necessary.
As depicted in figure 2, practical configuration using one of the on-chip operational amplifiers is readily implemented. The output signal offset can be suppressed by routing the signal through a capacitor before its application to the rectifier.

Figure 2 : Application Configuration of the Half–wave Rectifier.

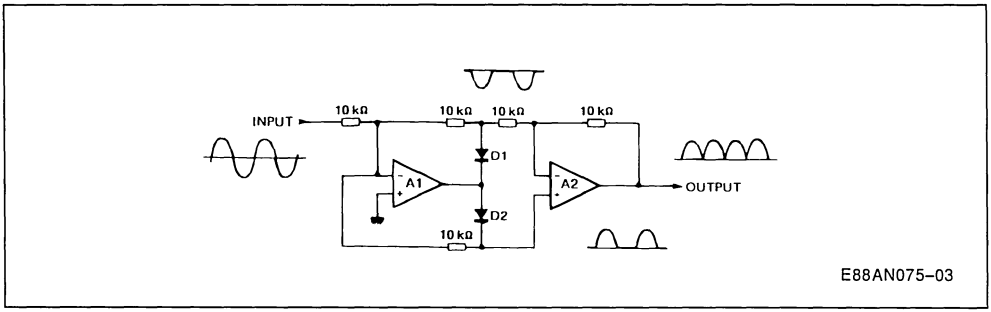


FULL-WAVE RECTIFICATION

Figure 3 depicts the operating principles of this rectifier.

Figure 3 : Full–wave Rectification Principles.

The first amplifier (A1) operates as half-wave rectifier - the two rectified half-cycles are forwarded to the second amplifier (A2) that inverts once again the positive half-cycles and transmits directly the negative half-cycles of the input signal.



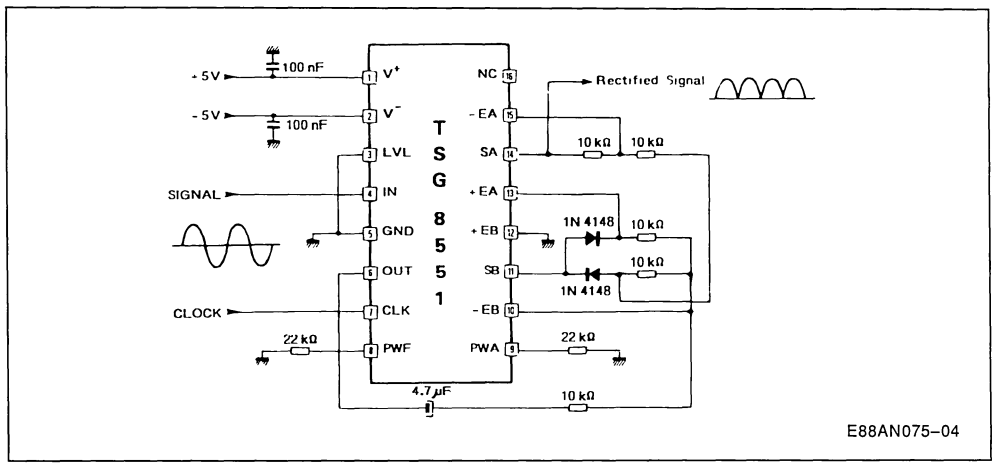
This configuration uses two operational amplifiers. The arrangement is straightforward, while resistors are of identical value and therefore easily matched - yielding accurate rectification.

Figure 4 illustrates the practical configuration using the on-chip operational amplifiers of the switched capacitor filter.

Since rectifier configurations are sensitive to input signal offset, a 4.7µF capacitor is inserted between the filter output and the rectifier.

A simple R-C network arrangement at filter output allows dc level extraction from the rectified signal.

Figure 4 : Application Configuration of the Full–Wave Rectifier.



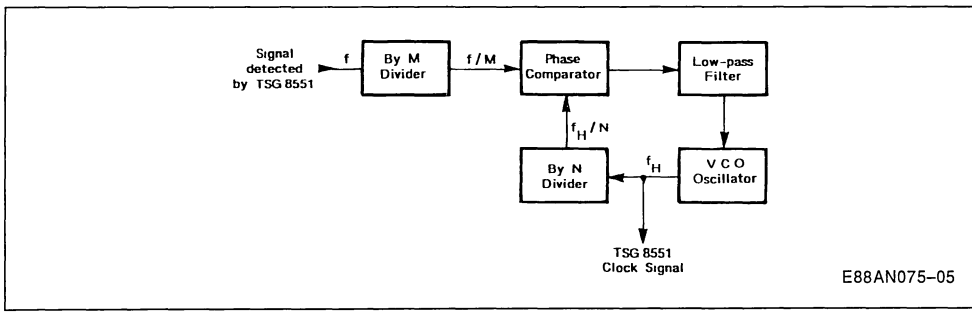
CLOCK FREQUENCY LOCKING

As mentioned earlier, amplitude detection using a highly selective filter such as TSG8551 requires perfect frequency stability of both, the signal to be detected and the filter clock frequency which determines the band-pass center frequency. Otherwise, frequency beating between the filter center frequency and the signal frequency would be produced - resulting in amplitude modulation of the filter output signal.

If the signal frequency is stable, it is an easy task to implement a clock oscillator using either of sufficiently stable quartz or ceramic resonators.

In general, the signal to be detected is also subject to frequency variations. This requires the filter center frequency to be locked onto the signal frequency. The easiest solution to achieve this requirement is to use a **P**hase **L**ocked **L**oop (**PLL**) operating principles of which are depicted in figure 5.

Figure 5 : Phase Locked Loop Block Diagram.



Phase locking yields :

$$\frac{f}{M} = \frac{fH}{N}$$

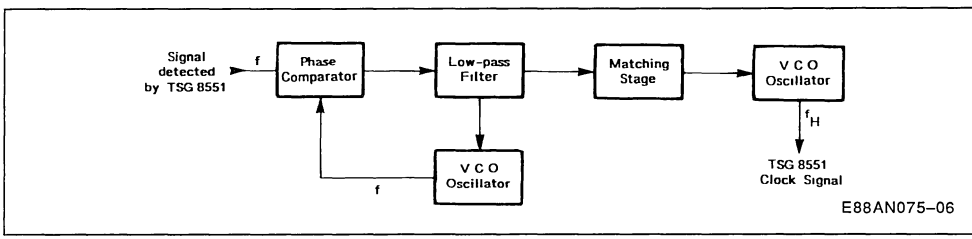
$$\text{i.e. } f_H = \frac{N}{M} f$$

The only requirement is therefore to select N and M values such as to make $\frac{N}{M}$ to correspond to the constant clock frequency-to-TSG8551 center frequency ratio - i.e. "**187.2 1%**".

Thus if one selects **M** = 5 the corresponding **N** value would be **936.**

As illustrated in figure 6, the PLL block diagram outlined in figure 5 can be simplified by removing the frequency divider networks.

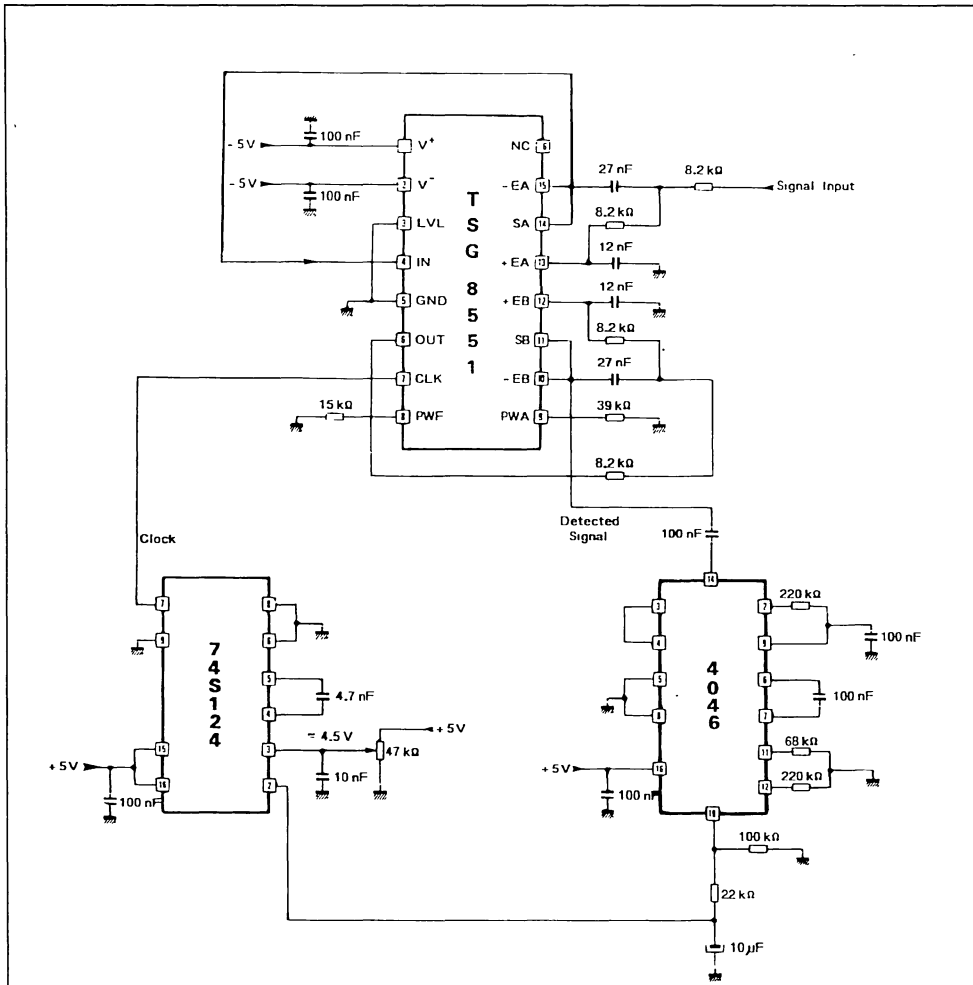
Figure 6 : Simplified PLL Block Diagram.



In this case, the phase is locked onto the frequency of the signal to be detected, and any variation of this frequency will produce an error voltage at the output of low-pass filter. This error voltage goes through a matching stage (amplification, filtering, ..) and is then applied to a **V**oltage-**C**ontrolled **O**scillator (**VCO**) output frequency of which is used as clock for the TSG8551.

Figure 7 depicts the practical application diagram of this arrangement.

Figure 7 : Locking the Clock Frequency onto the Detected Signal Frequency.



The 4046 (CMOS) device fulfils PLL functions while the 74S124 (TTL) circuit generates the clock signal. This application is well suited to amplitude detection of medium frequency signals " **190Hz ".**

The component values given in figure 7 allow the PLL to remain locked within a frequency range of ± **25Hz** around the **190Hz** - and if the input signal amplitude is constant, the amplitude of the detected signal would remain constant within a ± **10Hz** range around the **190Hz.**

It is obvious that the PLL operates ideally within the latter frequency range and as a consequence, the implemented filter is a true tracking filter.

However, filtering of the 4046 device output voltage produces a time constant of approximately 0.2 second. Consequently, the given configuration can follow only relatively low frequency variations of the signal to be detected - "about **10Hz/sec** max." - which corresponds to the characteristics of this type of application (frequency drift with aging and tem-

perature). A drawback associated to this type of PLL is the risk of locking onto an undesired interference signal the frequency of which falls within the capture range. For this reason and in order to limit the noise spectrum, the signal goes through an anti-aliasing filter before entering the filter input. Similarly, a smoothing filter is inserted between the filter output and the phase comparator input. These filters are implemented by Sallen-Key Cells using the filter operational amplifiers. If required, the PLL capture range can be readily reduced.

FREQUENCY DETECTION

The most frequent application is the detection of presence or the absence of a signal at a given frequency.

Thanks to its high selectivity and gain, the TSG8551 is particularly suitable for this type of applications.

By adjusting its clock frequency, the TSG8551 center frequency can vary from a few tens of Hertz (22Hz typ.) to few tens of kilo Hertz (20.3kHz typ.). As outlined in the previous section, a highly stable clock oscillator together with precautions to avoid parasitic signals are the major requirements for appropriate and error-free signal detection.

In general, the detected frequency must, after filtering, go through a signal shaping stage in order to become suitable for use by other devices.

The TSG8551 output signal can be made TTL-compatible by using one of the on-chip operational amplifiers configured as Schmitt Trigger.

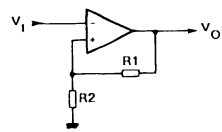
Figure 8 outlines the operating fundamentals of the Schmitt trigger. Selecting a low hysteresis ratio, the amplifier output flips between the two saturation voltages at low amplitude input signals.

Figure 8 : Schmitt Trigger Operating Fundamentals.

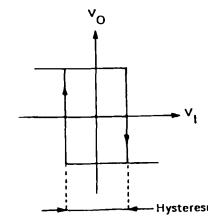
A low positive feed-back is applied to the amplifier by feeding the reference input with a fraction of the output voltage. Due to hysteresis, the output voltage level change does not occur at the same voltage level for input voltage rising or falling. The hysteresis ratio is determined by :

$$V_O \frac{R2}{R1 + R2}$$

Note that the illustrated trigger is of inverting type.



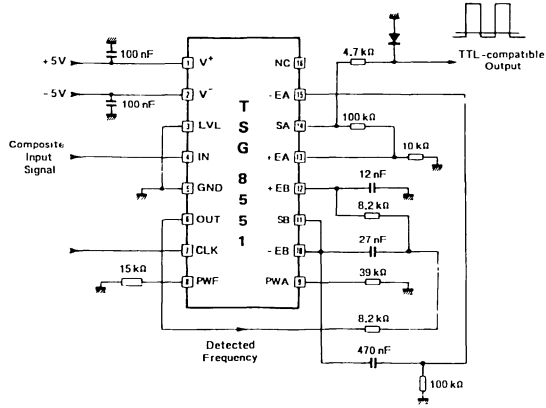
E88AN075–08



E88AN075–09

Figure 9 illustrates the practical application diagram with TSG8551 configured for frequency detection.

Figure 9 : Frequency Detection & TTL–Compatible Output (component values of the smoothing filter apply to a frequency of approximately 200Hz).



E88AN075–10

The 100kΩ and 10kΩ resistors set the hysteresis at 1/10th of the amplifier saturation voltage. Trigger thresholds are therefore **– 450mV** and **+ 300mV** approximately. Consequently, the trigger will operate satisfactorily when the TSG8551 output signal reaches **1V** peak-to-peak (500mV amplitude).

The 1V peak-to-peak output level corresponds to an approximately **30mV** peak-to-peak filter signal input. The voltage at trigger output swings between **– 5V** and **+ 3.5V** for TSG8551 symmetrical power supply of **– 5V**, **+ 5V**.

A diode connected to the output stops the negative half-cycle and makes the signal compatible for use with TTL devices (typical levels : **– 0.6V**, **+ 3.5V**).

Note that in order to avoid offset problems at the filter output, the signal goes through a 470nF capacitor before entering the trigger.

The output signal is sampled by the switched capacitor filter and needs smoothing before going through the Schmitt trigger for shaping.

BURST DURATION DETECTION

Another application of signal detection at a given frequency is the measurement of the signal burst duration. In this case, the burst must be detected without introducing any delay. One must therefore select a filter the group delay of which is compatible with the burst duration at the frequency under consideration. Generally, a group delay equal to 1/10 th of the burst duration is acceptable.

Oscillogram of figure 10 illustrates the burst detection of a 190Hz signal frequency using **TSG8550** filter particularly suitable for this type of application.

The **TSG8550** is a band-pass filter with its gain at center frequency and selectivity factor equal to **0dB** and **7** respectively.

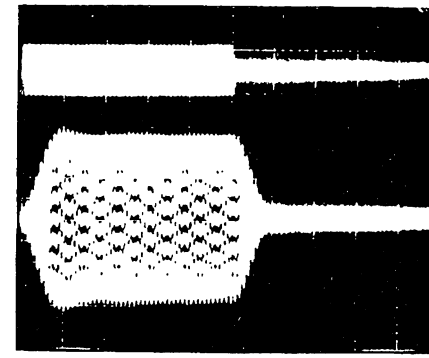
Its group delay at **190Hz** center frequency is about **22ms** - making it suitable for burst detection of at least **250ms** duration as shown in figure 10.

The application configuration used is a straightforward typical arrangement of the switched capacitor filters and does not include any anti-aliasing or smoothing filter.

Figure 10 : BURST DURATION DETECTION using **TSG8550**

- Signal Frequency : **190Hz**
- **Waveform 1** (upper)
  - Filter input : **200mV/div**
- **Waveform 2** (lower)
  - Filter output : **50mV/div**
- **t = 50ms/div**

Comment : The filter is suitable for signal detection at this frequency



E88AN075–11

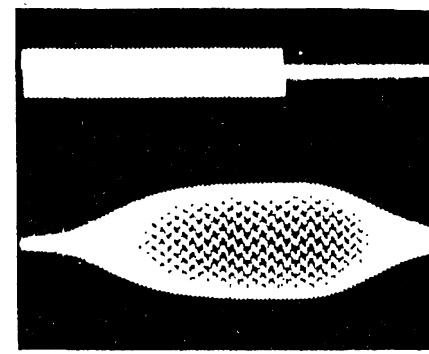
The oscillogram of figure 11 depicts the results obtained using **TSG8551** filter the group delay of which is about ten times higher than that of **TSG8550** ; i.e. about **200ms** at **190Hz** frequency.

It can be seen that the output burst is distorted because of an important delay during rising and falling phases.

Figure 11 : BURST DURATION DETECTION using **TSG8551**

- Signal Frequency : **190Hz**
- **Waveform 1** (upper)
  - Filter input : **200mV/div**
- **Waveform 2** (lower)
  - Filter output : **2V/div**
- **t = 50ms/div**

Comment : The filter exhibits a relatively high group delay for this frequency



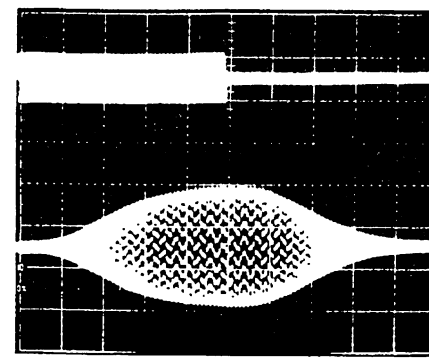
E88AN075–12

Note that the group delay is independent of the signal amplitude and inversely proportional to the signal frequency - as indicated by the oscillogram of figure 12 where the measured settling time is **20ms** for a **2kHz** signal frequency filtered by TSG8551.

Figure 12 : BURST DURATION DETECTION using **TSG8551**

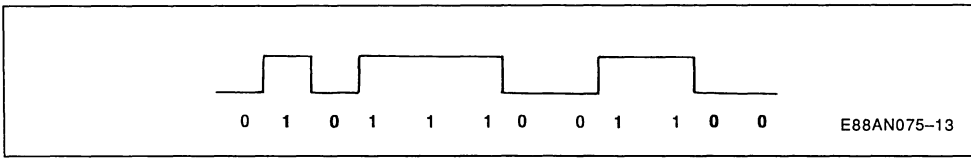
- Signal Frequency : **2kHz**
- **Waveform 1** (upper)
  - Filter input : **100mV/div**
- **Waveform 2** (lower)
  - Filter output : **1V/div**
- **t = 5ms/div**

Comment : The group delay is independent of the signal amplitude and inversely proportional to the signal frequency.



E88AN075–12

As the foregoing discussion demonstrated, a switched capacitor filter can be used to detect the presence and the burst duration of a signal. This type of application is used for data detection - e.g. detection of a binary code transmitted using on-off frequency modulation technique as shown below :



A microprocessor unit can be used to process the signal and, for example, to compare it with the contents of a ROM. After detection by switched capacitor filter, a single R-C low-pass cell is sufficient to extract the signal envelope.

Applications are numerous : remote-control, data transmission on teleprinters, etc ..

CONCLUSION

Wide range of currently available SGS-THOMSON Switched Capacitor Filters provide for appropriate selection of suitable filters meeting the requirements of every specific signal detection application.

The types most often used are standard band-pass filters, which in combination with the on-chip operational amplifiers, greatly simplify the design of signal detection applications. Also, such configuration arrangement offers the possibility of implementing additional functions related to signal detection such as rectification, signal shaping, signal amplification, etc... .

A true tracking filter is implemented by locking the filter clock onto the frequency of the signal to be detected.

The signal detection topic covers a wide range of applications - few examples of which were detailed throughout the present discussion. A single integrated filter associated to a few low-cost components, enables the design of complex functions.

VERY LOW DISTORTION SINEWAVE GENERATOR

INTRODUCTION

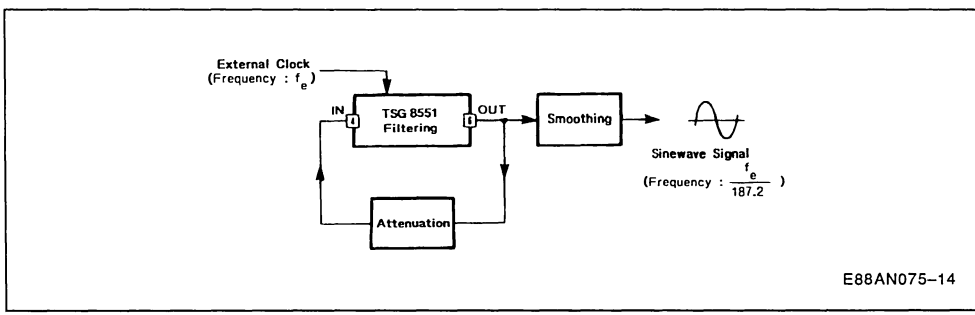
Thanks to its high coefficient of selectivity, the **TSG8551** filter is best suited to this application. This filter can extract from a complex signal, the component located at the filter center frequency.

In all cases, the TSG8551 output signal is nearly a pure frequency waveform, i.e. a sinewave.

We shall use this property to implement a sinewave generator, **using only a single TSG8551 package.**

Various configuration arrangements will be discussed and it will be demonstrated that thanks to the remarkable characteristics of the switched capacitor filters, there is a tremendous number of application possibilities for this type of oscillators.

Figure 13 : Sinewave Generator Block Diagram.



OPERATING PRINCIPLES

If a TSG8551 filter is configured in closed-loop, it begins oscillating at its center frequency.

Due to high filter gain and in order to avoid the saturation of the output stage, it is necessary to insert an attenuator within the feed-back loop.

With suitable attenuation, the filter output signal will be a sampled sinewave, and must go through a smoothing filter to obtain the final sinewave - the frequency of which will be proportional to the clock frequency.

IMPLEMENTATION

The most delicate task of this configuration is the design of the feed-back loop attenuator. In fact, an ordinary potentiometer cannot fulfil this requirement since too low an attenuation will cause the filter output signal amplitude to rise to the saturation level, while excessive attenuation will result in the signal amplitude falling gradually until the oscillator is completely halted. It is thus clear that the position of balance is quite unstable using a potentiometer.

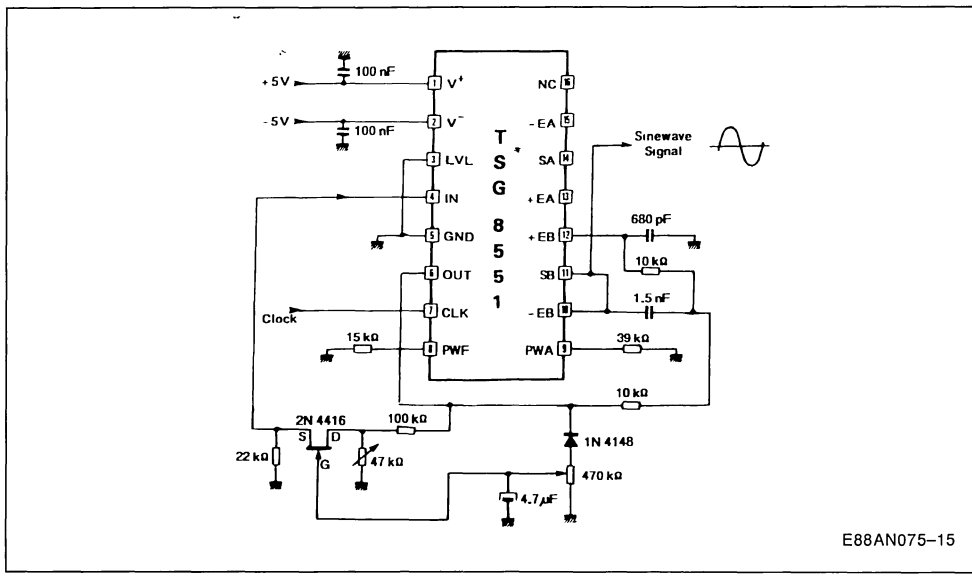
ALTERNATIVE 1 (figure 14)

The appropriate solution is to design a true **A**utomatic **G**ain **C**ontrol (**AGC**).

A simple configuration can be obtained resorting to the properties of the **F**ield **E**ffect **T**ransistors (**FET**) which behave as variable resistors as a function of the voltage applied to the gate.

The FET is used as a potentiometer, the gate biasing voltage is supplied by the negative amplitude of the output signal which is rectified by a diode and filtered by a capacitor. An N-channel FET is used here, so that, when the output signal rises, the gate voltage becomes more negative and therefore the FET conducts less, resulting in filter input signal attenuation.

Figure 14 : Sinewave Generator (with AGC).



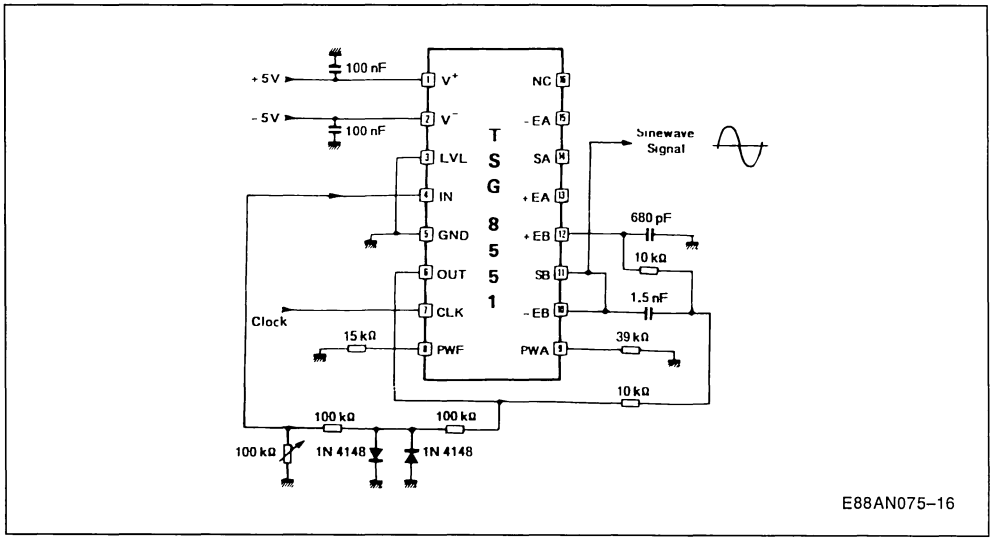
Inversely, when the output signal level falls, the transistor conducts more and as a consequence, the input signal amplitude rises. A potentiometer placed before the FET attenuates the output signal so as to enable the FET to operate at low drain-source voltage levels, i.e. within characteristic area where drain to source resistance varies linearly as a function of the gate voltage.

This configuration delivers a stable output signal amplitude of approximately 5V peak-to-peak irrespective of the clock frequency within the operating frequency range of the TSG8551 (center frequency : 20Hz to 20kHz). Sinewave smoothing is performed by one of the filter operational amplifiers configured in second-order low-pass (Sallen-key structure).

ALTERNATIVE 2 (figure 15)

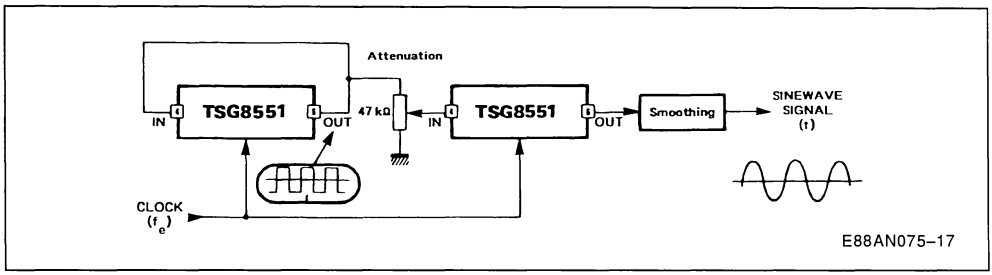
In this case, the output signal is clipped by two inverse-parallel connected diodes. This arrangement results in constant signal amplitude whatever the output signal amplitude (provided that it is higher than the diode threshold). A potentiometer allows to set the input level at a constant value and therefore adjust the output amplitude so as to avoid saturation.

Figure 15 : Sinewave Generator (with amplitude adjustment).



This simplified arrangement gives satisfactory results within the entire frequency range. The output sinewave **distortion** is about **0.2%** (total harmonic distortion).

Figure 16.



ALTERNATIVE 3

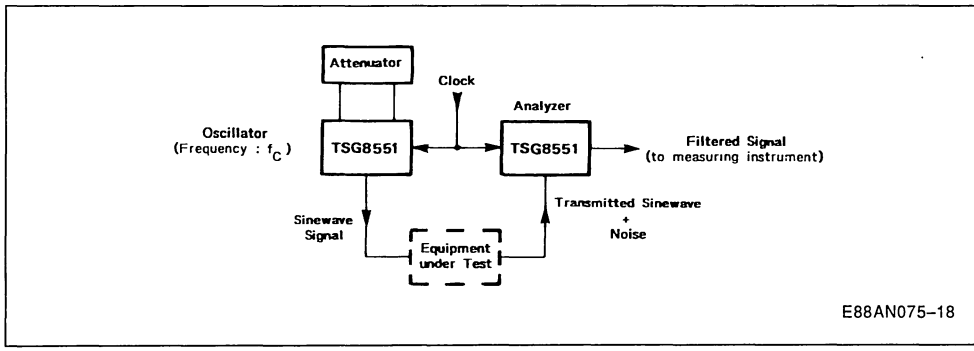
This solution if of simple implementation - attenuator adjustment does not involve any complication, but the configuration requires two TSG8551 filter packages.

The first TSG8551 is configured in closed-loop and therefore delivers a constant amplitude square waveform with its frequency equal to the filter center frequency. The filter power supply voltages determine the saturation voltages of the output amplifier and hence the signal amplitude. If this signal is sufficiently attenuated and then filtered once again by another TSG8551 centered on the same frequency, then a pure sinewave corresponding to the fundamental signal component would be obtained. Both TSG8551 filters are therefore driven by the same clock frequency and the smoothing is performed as previously using one of the filter operational amplifiers.

APPLICATIONS

- Since the frequency of the output sinewave is readily adjustable by the clock frequency, the first application of this oscillator is **Low Frequency Signal Generator.**
- Using an operational amplifier, the generated sinewave can be easily converted to **square** and **triangular waveforms.**
- If a **VCO** is used for clock generation, then the sinewave frequency can be modified by the voltage applied to the VCO. This property can be used for **frequency** (or **phase**) **modulation.**
- An interesting application using two TSG8551 filters is as follows :

Figure 17 : Network Analyzer.



The first filter operates as sinewave oscillator as discussed earlier while the second filter being driven by the same clock frequency, is automatically tuned at a center frequency equal to the oscillator frequency.

This configuration can be used to implement a **selective voltmeter** or a **network analyzer.** The oscillator signal is applied to the input of the device under test the output signal of which goes through the second TSG8551 and is then transmitted towards a measuring or recording instrument. Modifying the clock frequency, the entire low frequency range is scanned while the analyzing filter remains tuned on the input signal frequency.

CONCLUSION

Section 3 covered original design ideas built around switched capacitor filters which depart slightly from typical applications. This should enable the designer to explore new applications by taking full advantage of the flexibility of use inherent to switched capacitor filters. These filters can be undoubtedly integrated into other application configurations thus offering **design simplification** and **performance enhancement.**

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