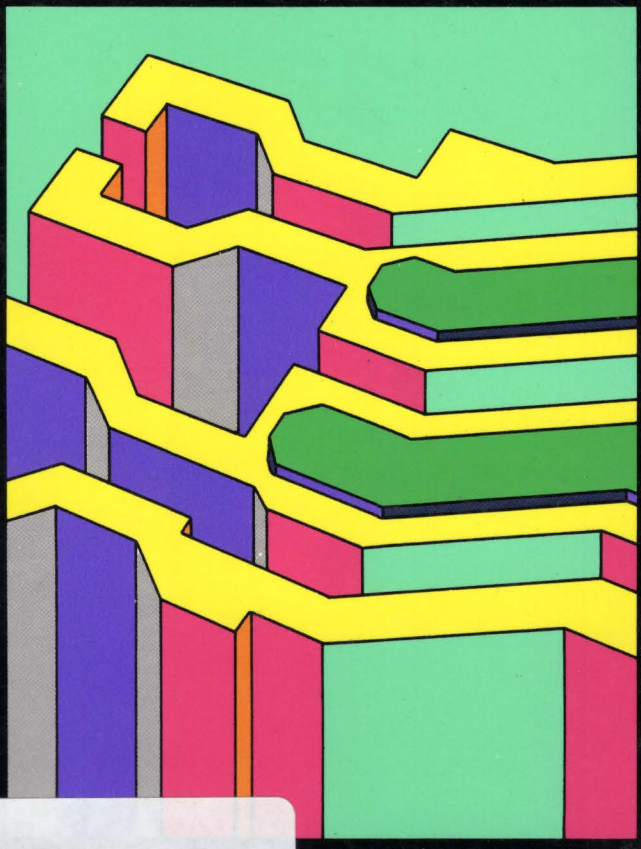
ZEROPOWER™ MEMORIES

APPLICATION NOTES



SGS-THOMSON
MICROELECTRONICS

ZEROPOWER™ MEMORIES

APPLICATION NOTES

FEBRUARY 1989

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices to systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

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SELECTION GUIDE

ZEROPOWER

Part Number	Org.	Access Time	I_{CC} Max		V_{CC}		Temperature Range	Pin Count
			Act	St.by				
MK48Z02B12	2K x 8	120ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02B15	2K x 8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02B20	2K x 8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02D25	2K x 8	250ns	80mA	3mA	5V	+10%	0 to +70°C	24
MK48Z02BU12	2K x 8	120ns	80mA	3mA	5V	−5%	0 to +70°C	24
MK48Z02BU15	2K x 8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02BU20	2K x 8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02BU25	2K x 8	250ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12B12	2K x 8	120ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12B15	2K x 8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12B20	2K x 8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12B25	2K x 8	250ns	80mA	3mA	5V	±10%	0 to +70°C	24
MK48Z12BU12	2K x 8	120ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12BU15	2K x 8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12BU20	2K x 8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12BU25	2K x 8	250ns	80mA	3mA	5V		0 to +70°C	24
MKI48Z02B12	2K x 8	120ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02B15	2K x 8	150ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02B20	2K x 8	200ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02B25	2K x 8	250ns	80mA	3mA	5V	+10%	−40 to +85°C	24
MKI48Z02BU12	2K x 8	120ns	80mA	3mA	5V	−5%	−40 to +85°C	24
MKI48Z02BU15	2K x 8	150ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02BU20	2K x 8	200ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02BU25	2K x 8	250ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12B12	2K x 8	120ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12B15	2K x 8	150ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12B20	2K x 8	200ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12B25	2K x 8	250ns	80mA	3mA	5V	±10%	−40 to +85°C	24
MKI48Z12BU12	2K x 8	120ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12BU15	2K x 8	150ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12BU20	2K x 8	200ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12BU25	2K x 8	250ns	80mA	3mA	5V		−40 to +85°C	24
MK48Z08B15	8K x 8	150ns	50mA	3mA	5V		0 to +70°C	28
MK48Z08B20	8K x 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z08B25	8K x 8	250ns	50mA	3mA	5V	+10%	0 to +70°C	28
MK48Z08BU15	8K x 8	150ns	50mA	3mA	5V	−5%	0 to +70°C	28
MK48Z08BU20	8K x 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z08BU25	8K x 8	250ns	50mA	3mA	5V		0 to +70°C	28
MK48Z18B15	8K x 8	150ns	50mA	3mA	5V		0 to +70°C	28
MK48Z18B20	8K x 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z18B25	8K x 8	250ns	50mA	3mA	5V	±10%	0 to +70°C	28
MK48Z18BU15	8K x 8	150ns	50mA	3mA	5V		0 to +70°C	28
MK48Z18BU20	8K x 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z18BU25	8K x 8	250ns	50mA	3mA	5V		0 to +70°C	28

Note: 1. Letter "U" inserted in sales type indicates "Underwriters' Laboratories" branding.

ZEROPOWER (Continued)

Part Number	Org.	Access Time	I_{CC} Max		V_{CC}		Temperature Range	Pin Count
			Act	St.by				
MK48Z09B15	8K x 8	150ns	50mA	3mA	5V		0 to +70°C	28
MK48Z09B20	8K x 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z09B25	8K x 8	250ns	50mA	3mA	5V	+10%	0 to +70°C	28
MK48Z09BU15	8K x 8	150ns	50mA	3mA	5V	−5%	0 to +70°C	28
MK48Z09BU20	8K x 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z09BU25	8K x 8	250ns	50mA	3mA	5V		0 to +70°C	28
MK48Z19B15	8K x 8	150ns	50mA	3mA	5V		0 to +70°C	28
MK48Z19B20	8K x 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z19B25	8K x 8	250ns	50mA	3mA	5V	±10%	0 to +70°C	28
MK48Z19BU15	8K x 8	150ns	50mA	3mA	5V		0 to +70°C	28
MK48Z19BU20	8K x 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z19BU25	8K x 8	250ns	50mA	3mA	5V		0 to +70°C	28
BATTERY BACK-UP								
MK48C02AN15	2K x 8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48C02AN20	2K x 8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48C02AN25	2K x 8	250ns	80mA	3mA	5V	+10%	0 to +70°C	24
MK48C02AK15	2K x 8	150ns	80mA	3mA	5V	−5%	0 to +70°C	24
MK48C02AK20	2K x 8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48C02AK25	2K x 8	250ns	80mA	3mA	5V		0 to +70°C	24
TIMEKEEPER								
MK48T02B12	2K x 8	120ns	80mA	3mA	5V		0 to +70°C	24
MK48T02B15	2K x 8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48T02B20	2K x 8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48T02B25	2K x 8	250ns	80mA	3mA	5V	+10%	0 to +70°C	24
MK48T02BU12	2K x 8	120ns	80mA	3mA	5V	−5%	0 to +70°C	24
MK48T02BU15	2K x 8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48T02BU20	2K x 8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48T02BU25	2K x 8	250ns	80mA	3mA	5V		0 to +70°C	24
MK48T12B15	2K x 8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48T12B20	2K x 8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48T12B25	2K x 8	250ns	80mA	3mA	5V	±10%	0 to +70°C	24
MK48T12BU15	2K x 8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48T12BU20	2K x 8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48T12BU25	2K x 8	250ns	80mA	3mA	5V		0 to +70°C	24

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APPLICATION NOTES

INTRODUCTION TO ZEROPOWER™

By Peter LUNTER

HISTORY

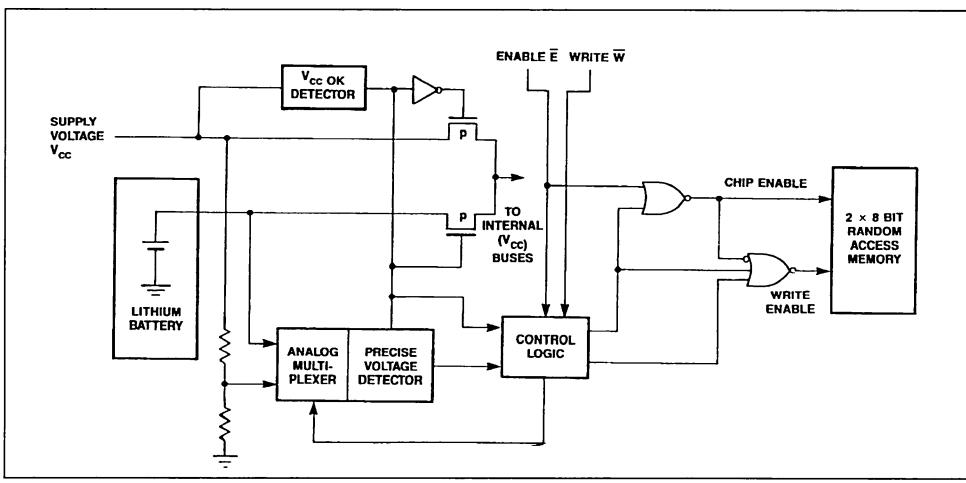
During the early 1980's it became evident that a need existed for a silicon non-volatile random access memory (NVRAM). This is memory that can have any address location directly accessed for both reads and writes, plus retain data in the absence of power. Since the demise of core memory, implementation of an NVRAM has been limited to either supplying an external battery and power switching circuitry to a conventional static RAM (dynamic RAM is unsuitable because of refresh requirements), or downgrading system performance to accommodate the slow and limited number of write cycles of EEPROMs. Because of EEPROM restrictions some applications had no alternative to the battery system. The task set before Thomson-Mostek engineers was to integrate a battery, power switching circuitry, and RAM into a single package that would directly replace conventional static RAM with no modifications to the syste, i.e. : have the same pin out and timing with no restrictions on the number of write cycles.

The product definition of this NVRAM set a number of high goals that needed to be accomplished. The following partial list of requirements for this device illustrates the complexity of the battery backed-up system that has been given the trademark name of ZEROPOWER.

- **POWER SWITCHING CIRCUITRY**
  1. Automatically deselect the device at a voltage that prevents out of V_{CC} tolerance devices from accessing the RAM.
  2. Must provide a temperature stable trip point.
  3. Automatically switch over to a battery power under a power failure.
  4. Be integrated in the same package as the RAM.
  5. Power down all circuitry except the matrix core to maximize battery life.

- **BATTERY**
  1. Must be small enough to fit on top of a 600 mil package.
  2. Must have sufficient capacity to sustain data for an expected 10 year life under worst case conditions.
  3. Must have a chemistry that is safe to use.
  4. Must provide power instantaneously on command (no wake-up delay).
  5. Must operate under the full temperature range.

Figure 1 : MK48Z02 Block Diagram.



- **RAM**
  1. Incorporate a six transistor memory cell to minimize battery back up current.
  2. Must not provide any battery charging paths to the battery (UL safety requirement).
  3. Must not sustain an inadvertent latch-up condition under battery power.
- **PACKAGE**
  1. Economical plastic 24 pin JEDEC pinout.
  2. Practical integration of battery to silicon.

The result of this unprecedented engineering effort was the introduction of the MK48Z02 in 1984.

CIRCUIT DESCRIPTION AND OPERATION

The MK48Z02 is a 5 volt 2K x 8 bit static random access memory with access speed grades ranging from 120 to 250 nanoseconds. The pinout conforms to JEDEC standard for static RAMs in 24 pin 600 mil package. Operation above the power fail detect trip point is no different from other static RAMs.

What makes the MK48Z02 different from other static RAMs is that the MK48Z02 monitors V_{CC} for a power fail condition and switches over to an internal battery to maintain data during a power absence. The power fail detect circuit consists of a patented 2.5 volt band gap reference and chopper stablized comparator. V_{CC} is input to the comparator via a poly silicon divider network. At voltages above the power fail detect trip point V_{CC} is continuously monitored for an out of specification condition. When V_{CC} falls below the power fail detect trip point the device automatically deselects prohibiting acces to the device.

At voltages below the power fail detect trip point the linear circuit then operates in a multiplexed mode, checking V_{CC} for the battery switch over point, checking for a bad battery, and checking for a return to a valid V_{CC} level. The battery switch over point is checked by a simple level detector that uses the turn on characteristics of a three transistor totem pole for the reference voltage. When V_{CC} drops below approximately 3 volts V_{CC} is switched out, the battery switched in, and all I/O circuitry is switched off to conserve power. The battery is checked on every power up cycle by placing a load on the battery and checking its voltage using the second stage of the band gap reference. Should the battery be below approximately 2 volts, the first write cycle to the MK48Z02 after power up will be inhibited signaling the user of potential data loss. A power up recovery time is specified to allow the linear circuit time to complete all phases of V_{CC} and battery checking.

ZEROPOWER FAMILY

Since its introduction in 1984, the MK48Z02 has expanded to an entire product line. To date the list includes...

Product	V_{CC} Tolerance		Control Interface	Array	Features
	+ 10% − 5% 4.6V Typ. Deselect	+ 10% − 10% 4.3V Typ. Deselect	2 or 3 Wire		
MK48Z02	X		X	2K x 8	
MK48Z12		X	X	2K x 8	
MK48T02	X		X	2K x 8	REAL TIME CLOCK
MK48T12		X	X	2K x 8	REAL TIME CLOCK
MK48Z08	X		X	8K x 8	
MK48Z18		X	X	8K x 8	
MK48Z09	X		TWO CHIP SELECTS AND $\overline{G}$	8K x 8	POWER FAIL INTERRUPT OUTPUT
MK48Z19		X	TWO CHIP SELECTS AND $\overline{G}$	8K x 8	POWER FAIL INTERRUPT OUTPUT

Notes : 1. Read Time Clock Calendar occupies top eight bytes of memory and access the same as memory.
2. Power Fail Interrupt Output (open drain) gives 10µs to 40µs advanced warning of a power fail deselect condition.

REPLACING EEPROM WITH ZEROPOWER™

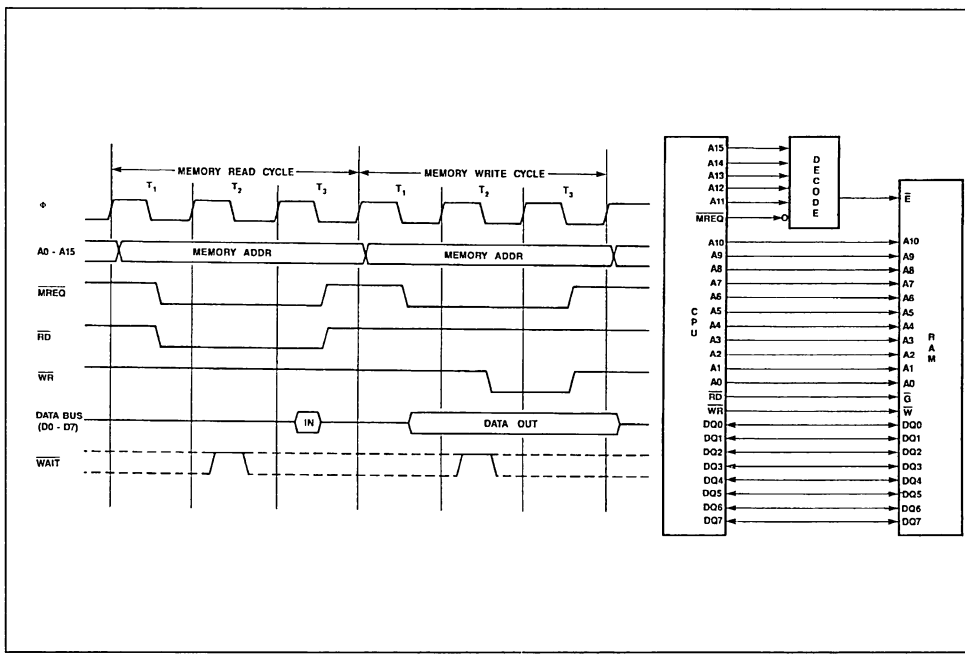
By Peter LUNTER

Currently there are two approaches for implementing non-volatile memory that can be electrically altered within the system. The first is EEPROM (electrically erasable programmable read only memory). The second is battery backed-up RAM. Many misconceptions about battery backed-up RAMs have swayed system designers away from this technology into using EEPROMs with lower performance specifications. All is not lost however, the ZEROPOWER technology developed by SGS THOMSON Microelectronics provides a totally integrated approach to battery backed-up RAMs, which in most cases can provide direct replacement of EEPROMs with an added advantage of upgrading system performance.

First let's clear the air about the misconceptions concerning battery backed-up RAM. The integration of a long life lithium cell and the low standby current of CMOS RAMs have made possible data retention times that typically extend beyond ten years. Periodic replacement of batteries or battery charging circuits are no longer necessary. Power fail detection and switching circuitry can be integrated into the same package allong with RAM and a small button lithium cell making a complete battery backed-up system that fits into the same socket as conventional RAM. This system in a DIP (dual in-line package) has been invented and trademarked as ZEROPOWER technology by SGS-THOMSON. Extensive reliability studies of the ZEROPOWER technology have been undertaken at SGS-THOMSON which demonstrate a highly reliable approach to non-volatile memory.

Because microprocessors are designed to interface to RAMs, a ZEROPOWER RAM provides the ideal replacement for conventional RAM. Figure 1 shows a typical output timing and interface of an 8 bit microprocessor (Z80). RAM interface can be made by decoding MREQ and address information for E, connecting RD to G, and connecting WR to R.

Figure 1 : Z80 Timing.



EEPROMs, on the other hand, require some modification to the write cycle. This modification can be as simple as adding wait cycles until a write to the EEPROM is completed. In this case direct replacement with a ZEROPOWER RAM is possible. The wait cycles can be left in or eliminated to improve performance.

Some early versions of EEPROMs (2816 without any suffix), however, require a 21 volt VPP signal. This type of EEPROM is programmed the same way conventional EPROMS are programmed. The only difference being that both "ones" and "zeros" can be programmed not just "zeros". Figure 2 shows how complicated interface to this type of EEPROM can be. Replacement with a ZEROPOWER RAM can be accomplished by eliminating almost all of the external circuitry. In the example shown in figure 2 only the inverter E is required for interface to a ZEROPOWER RAM. For interface to a ZEROPOWER RAM the output of inverter E should be connected to $\overline{G}$, and $\overline{WR}$ should be connected directly to $\overline{W}$ on the ZEROPOWER RAM.

In contrast, current technology EEPROMs are 5 volt only. There are two popular types of EEPROMs in production today. The are referred to as latched and timer EEPROMs. Latched EEPROMs latch both data and address on the falling (beginning) edge of the write pulse. Although addresses and data are allowed to change before the completion of a write cycle, write enable must be held active for the complete write cycle. Figure 3a shows latched EEPROM write timing. Timer EEPROMs, however, latch addresses on the falling edge of the write pulse and data on the rising edge. Figure 3b shows timer EEPROM write cycle timing.

Figure 2 : 2816 Interface.

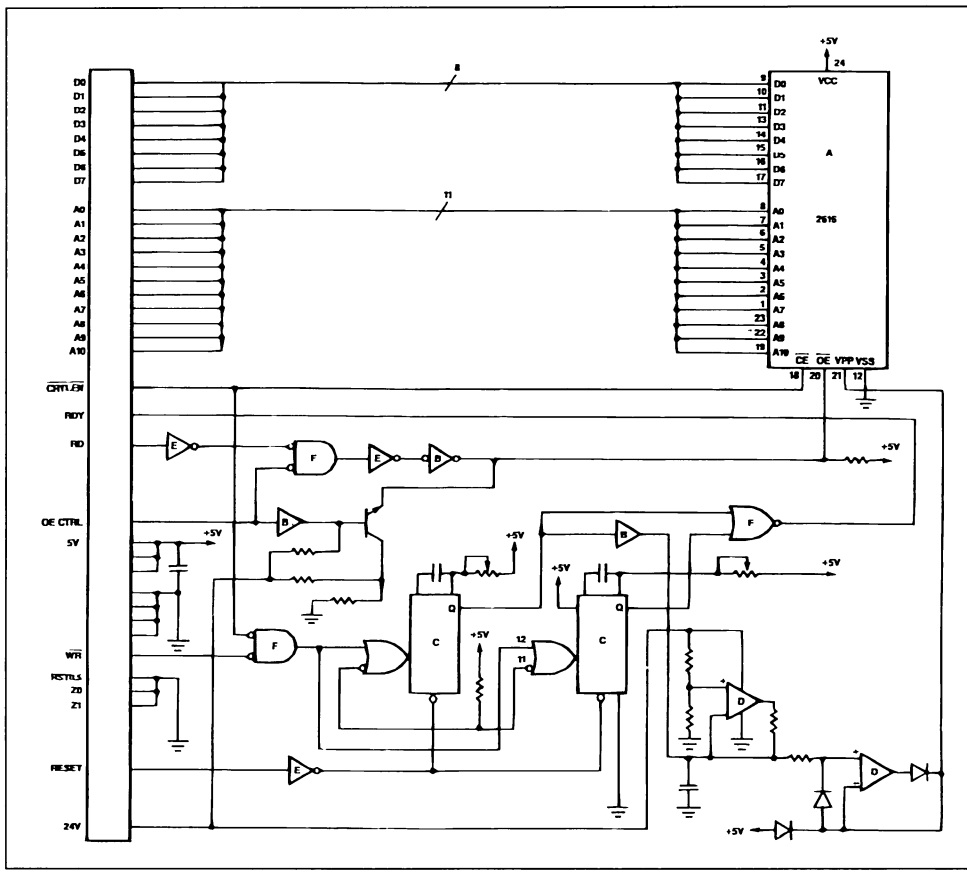


Figure 3a : Latched EEPROM Write Cycle.

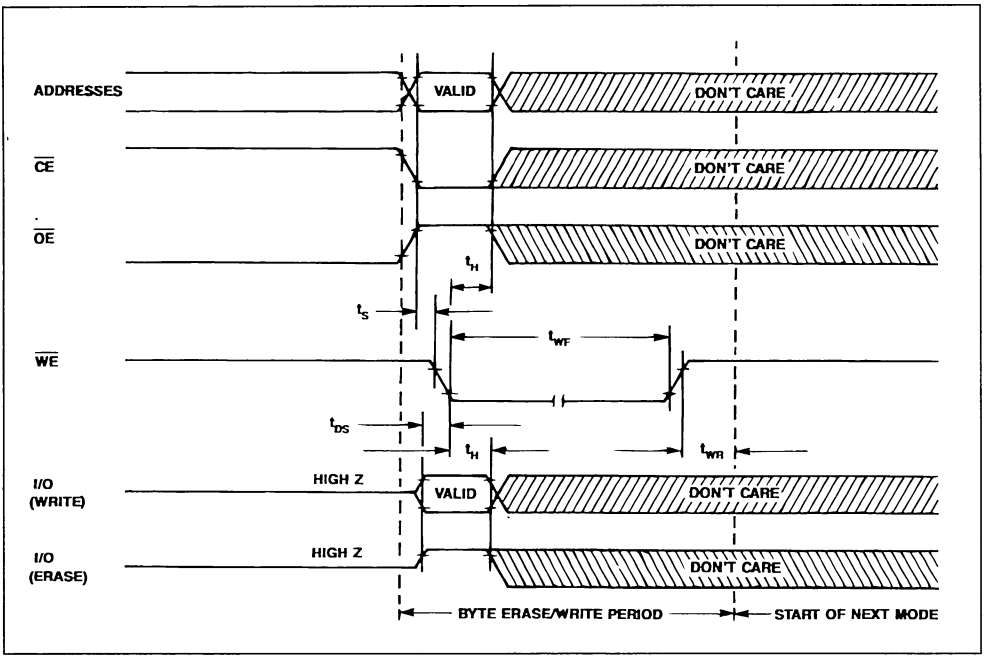
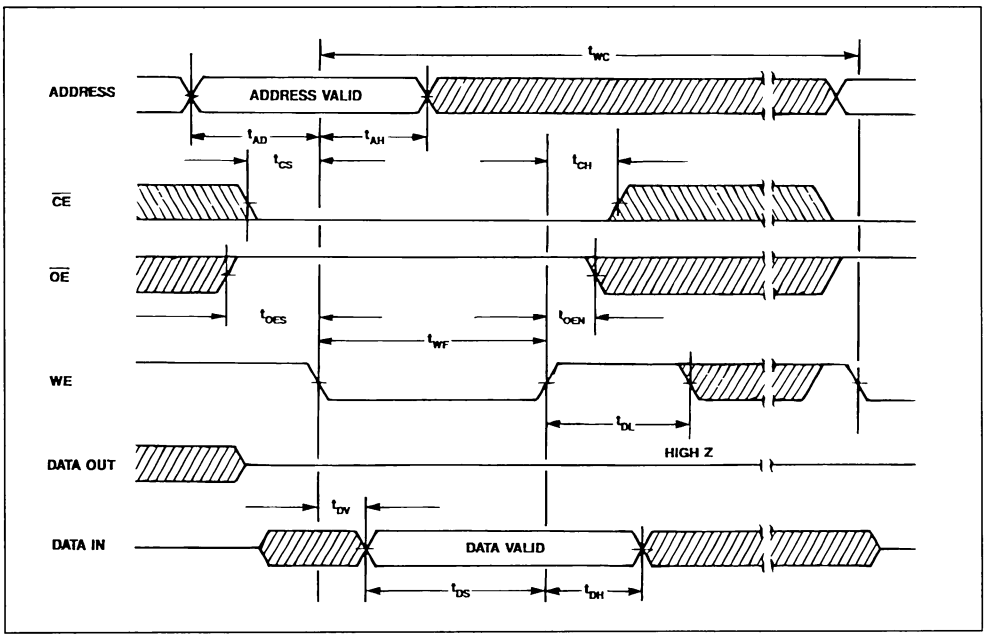


Figure 3b : Timer EEPROM Write Cycle.



Latched EEPROMs are interfaced in the system two ways. One, by latching the $\overline{WE}$ pulse until completion of the write cycle. Two by implementing multiple wait states to complete the write. Replacing latched EEPROM can be done by eliminating the $\overline{WE}$ latch, allowing the write cycle to follow the microprocessor. Multiple wait states will have no effect on the ZEROPOWER RAM, however for system efficiency they should be eliminated.

Timer EEPROMs are the most popular EEPROMs in use today because their write cycle timing is compatible with microprocessors that have cycle times in the 200 to 500 nanosecond range. The initialization of a timer EEPROM write cycle can be completed in the normal cycle time of the microprocessor and the EEPROM completes the write cycle independent of the system. Some timer EEPROMs will even allow multiple successsive writes (in page mode) before completion of the first write. ZEROPOWER RAMs are directly replaceable for timer EEPROMs in this application and have the advantage of even faster cycle times with no page mode restrictions. Timer EEPROMs, however, can also allow data and address changes during the write cycle. These data and address changes are not permited on conventional RAM and therefore in this application, data and address must be externally latched before replacement with ZEROPOWER RAM can be done. The later case is not industry standard for memories, and many systems with multiplexed address/data already have address and data latches for this reason.

Note :

Many EEPROMs require output enable to be high during the write cycle. With RAMs output enable is a "don't case" during write. In the very unlikely event that output enable should be used to gate the write cycle, a change in the circuit needs to be implemented before ZEROPOWER RAM can be used as a replacement.

PROGRAMMING THE MK48Z02

By Peter LUNTER

The MK48Z02 serves many varied applications. It provides the ease of access for both reads and writes that conventional RAMs offer, as well as nonvolatile memory that is associated with read only memories. Because of this nonvolatile characteristic, the MK48Z02 is often utilized as a medium for storage of alterable program code (firmware) as well as parametric data.

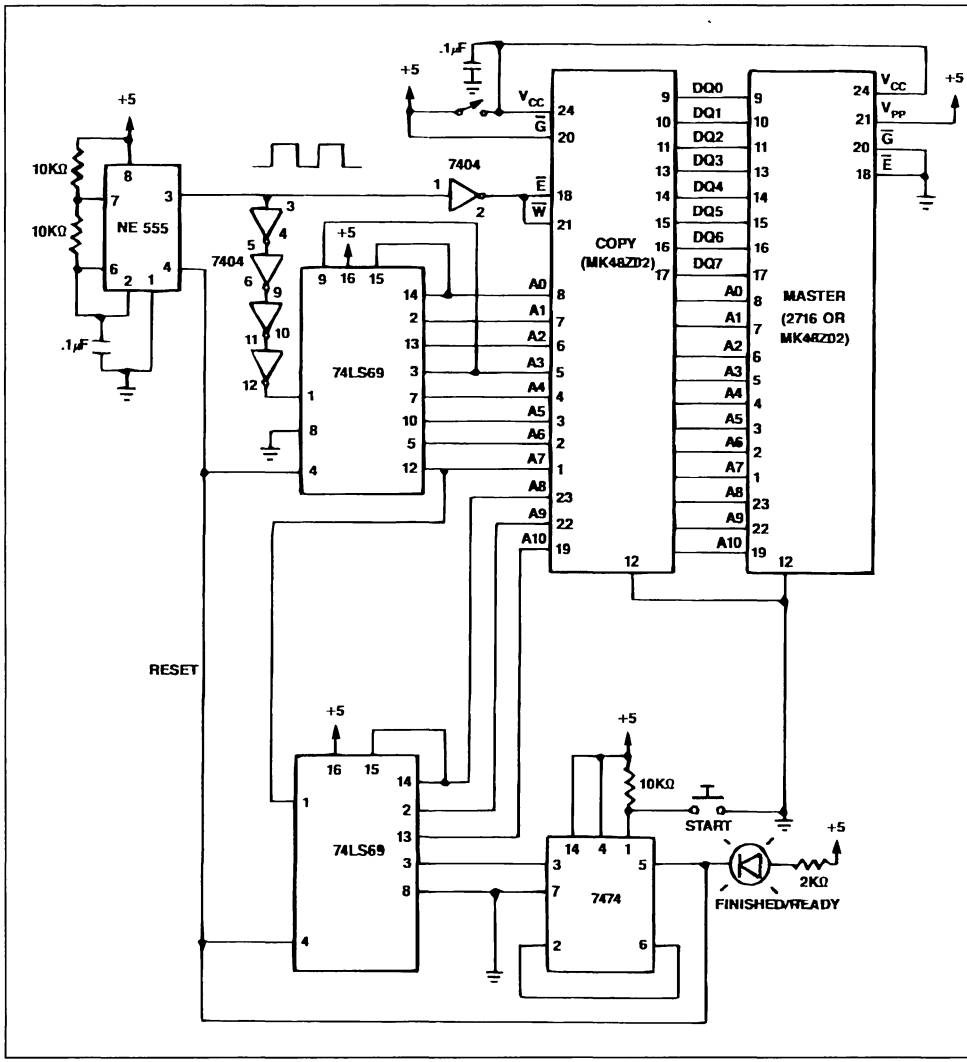
This type of data is usually generated on a software development system and then loaded into memory prior to installation of the device into the final product. Most software development systems provide the means of downloading code either directly into an EPROM device or provide a port for transferring this code to an external PROM programmer. The MK48Z02 will of course not work in an EPROM programming circuit because of the high voltages requires for EPROM write cycles.

Figure 1 shows an inexpensive circuit, however, that can be used for transferring code from an EPROM (master) to an MK48Z02 (copy). (If data already exists in an MK48Z02 it also can be used as the master, because read cycles of the MK48Z02 and EPROM devices are similar). This circuit uses an oscillator and counter to step through all address locations in a binary sequence. The first phase of the clock (positive cycle) generates the write pulse. The second phase of the clock (negative edge) is used to clock the counter circuit to the next address. Once all addresses have been accessed, the next cycle will set a latch that resets the circuit and lights a finished light. Pushing the start button resets the latch and starts the sequence from the beginning. A switch going to V_{CC} on the master and copy sockets is provided so that V_{CC} can be removed when inserting or removing devices to insure maximum data security. Removing V_{CC} from the MK48Z02 will deselect the device making all other inputs don't care, therefore intermittent contact to the socket when inserting or removing devices will not generate spurious write cycles.

Verification of data should not be a significant issue because the MK48Z02 does not suffer from programming yield problems like EPROM devices do. However, if a device is suspected of having faulty code, verification can be accomplished on the EPROM programmer IN THE VERIFICATION MODE ONLY (caution : check with the manufacturer of the programmer to make sure no high voltages are applied to the device in the verify only mode).

There is no limit to the number of times the MK48Z02 can be programmed, and the MK48Z02 does not need to be erased before it can be programmed.

Figure 1 : Inexpensive MK48Z02 Programmer.



POWER FAIL INTERRUPT (MK48Z09/19)

A frequent dilemma faced by system designers is how to handle a power failure. Because power fail sensing components add real estate and cost to the system, some designers choose not to implement a power fail routine, allowing "the chips to fall where they may". This approach is frequently rationalized given the in-frequency of power failures and the industry drive to minimize circuit board space. It does not however represent an ideal solution. Other designers have gone to great expense to design a power fail sensing circuit only to find it difficult to control voltage trip points and experience timing requirements that are hard to predict.

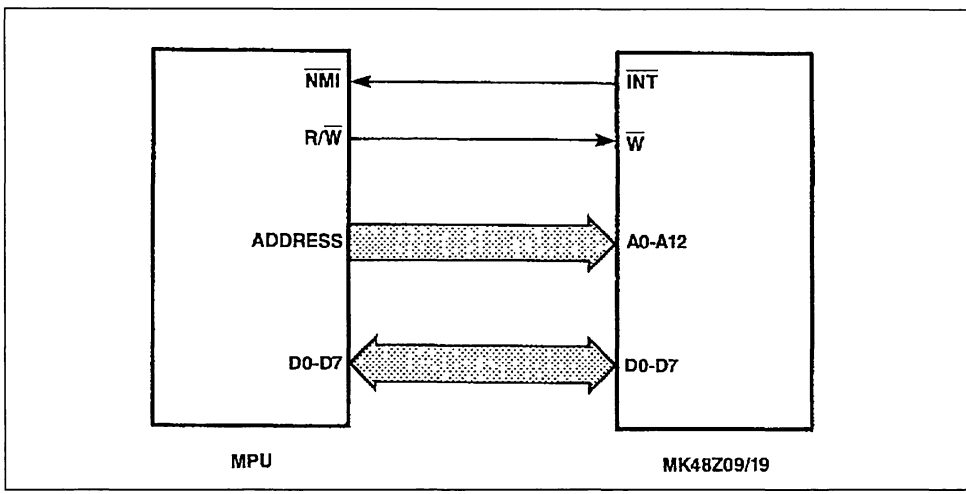
The MK48Z09/19 provides a solution to the power fail dilemma. While occupying no more board area than conventional memories of the same density, the MK48Z09/19 also offers a power fail interrupt output pin along with nonvolatile memory. Because the voltage trip point of the interrupt signal on the MK48Z09/19 is temperature compensated, the user can be assured that its operation remains within specifications over the entire temperature range. The MK48Z09/19 also provides predictable timing. The amount of time between an interrupt low and a power fail write protect condition is a function of an internal oscillator within the MK48Z09/19 and therefore is independent of what may be happening at the system level. The only restriction imposed on the user is that a minimum V_{CC} fall time not be exceeded. The minimum V_{CC} fall time is, however, easily within the normal V_{CC} fall time characteristics of most applications.

The power fail interrupt pin of the MK48Z09/19 is open drain and can be easily implemented by connecting the interrupt signal to a non maskable interrupt input on the microprocessor used, thus initializing a short power fail routine. Because the MK48Z09/19 is battery backed up the power fail routine can store important data and parameters. Sign off to data communication links and notification of a local power failure to supervisory systems are also applications made possible to the local controller through the use of the power fail interrupt.

POWER FAIL CONDITIONS

The MK48Z09/19 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point of the MK48Z09/19 an interrupt is immediately generated. An internal clock provides a delay no less than 10µs but no greater than 40µs before automatically deselecting the MK48Z09/19.

Figure 1 : Suggested MK48Z09/19 Hook Up.



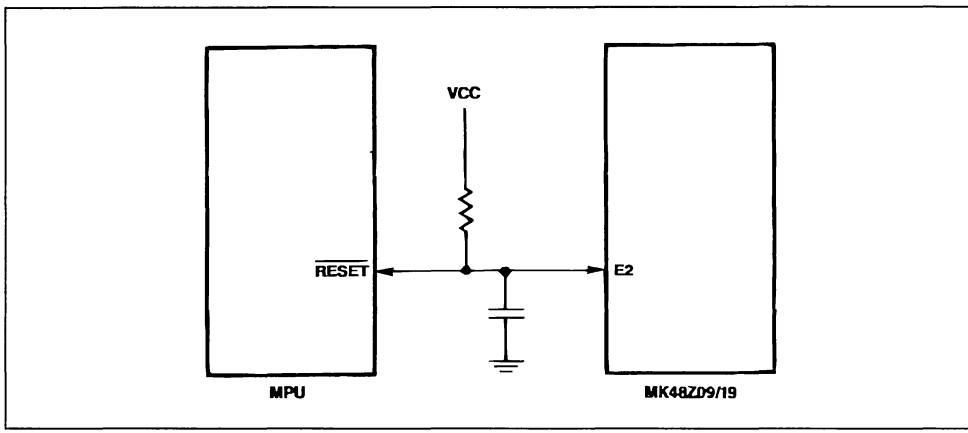
With V_{CC} allowed to fall at its maximum rate from 4.75V to 4.5V in 300µs (833V/sec), a delta voltage between when a power fail is detected and the device is deselected will be established. Because the maximum V_{CC} fall rate and maximum delay between power fail detect and deselection are given values, this delta voltage can be easily calculated 40µs * 833/V = 48mV). Therefore final testing of the MK48Z09/19 at SGS-THOMSON can assure the user that the device will be deselected no lower than the specified Power-Fail Deselect (VPFD min) level, provided that the maximum V_{CC} fall rate is not exceeded.

With V_{CC} fall times that stretch over a long period of time, the voltage at which an interrupt is generated and the voltage at which the MK48Z09/19 automatically deselects will approach the same value. Once again final testing at SGS-THOMSON can assure the user that a power fail detect or deselection will occur no higher than the specified Power-Fail Deselect (VPFD max) level.

POWER UP CONDITIONS

The MK48Z09/19, like most NVRAMs, provides automatic write protection under low voltage conditions. Unfortunately, many processors generate spurious cycles during power up, despite V_{CC} being within spec. Some processors even continue to behave erratically though their reset pin is being held low, until the system clock has had time to wake up and produce sufficient cycles to clear the processor. The MK48Z09/19 makes it easy to combat this problem by providing an active high E2 input (chip select). This input when tied to the reset line will lock out the MK48Z09/19 during the power on reset time, protecting the data in memory from being inadvertently over written with erroneous data. Figure 2 illustrates a simple power up reset scheme.

Figure 2 : Write Protect Application of E2 Input.



Notes : 1. Although trip points are tested by holding V_{CC} to given DC levels, the device is by no means in a static state. Address, data lines, and control lines are all toggling. A series of complex patterns are input to the device to ensure that worst case noise conditions generated within the MK48Z09/19 will not affect trip point performance.

2. With even the slowest MK48Z09/19, the 250ns device, and the minimum 10µs advanced warning of a deselect condition, there is enough time for 40 memory cycles to take place. The amount of MPU cycles that can take place will of course vary according to the processor used and programming techniques.

3. The MK48Z09/19 can provide an inherent safe guard against a "Brown Out" condition i.e. V_{CC} that droops or slowly fades below spec. or operational limits and then comes back up. Applications requiring the interrupt pin to remain low until a completion of a sequence of events (within 10µs), can relay on the MK48Z09/19 not to interrupt the sequence should power unexpectedly return. Once a power failure is detected and the interrupt pin goes low, the interrupt pin will remain low for the full 10µs to 40µs period and the device will be accessible during this time. Therefore the power fail interrupt application can not be aborted mid cycle. After the interrupt time period the interrupt pin will go high, should V_{CC} rise in the interim, allowing normal operation to resume. The MK48Z09/19, however, waits for a minimum of 30µs to a maximum of 120µs from the time interrupt goes high until another power fail can be selected. (Should V_{CC} remain at a level very close to the trip point for an extended period of time, a number of power failures could be detected due to noise on the V_{CC} line. Interrupt will always follow the above timing however).

MK48T02 TIMEKEEPER™ CLOCKED RAM

By RICK TUTTLE

While SGS-THOMSON Microelectronics ZEROPOWER RAMs have established themselves as a clearly advantageous alternative in many non-volatile memory applications, the integration of a real-time clock with the RAM has moved the ZEROPOWER product family well beyond the capabilities of other non-volatile approaches. This describes the common characteristics of the ZEROPOWER family and details how the integration of a user controllable real-time clock has been accomplished.

INTRODUCTION

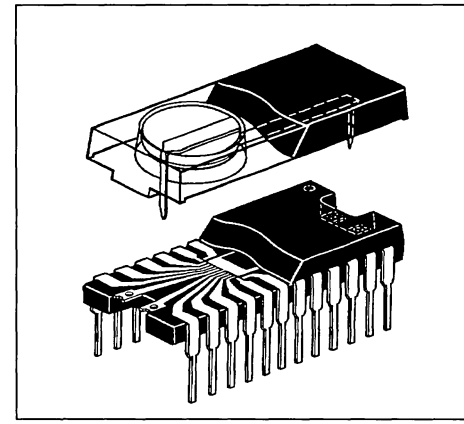
Every since core memory began to fade from view, the demand for a non-volatile semiconductor memory device has been growing. The void left by core has motivated many pretenders to the throne, each with their own liabilities. EEPROM designers wrestle with long store times and trade off endurance. The bubble memory supporters find themselves in a price/performance war with diskettes. Even the system designer who decides to take matters into his own hands and builds a battery backed-up system fights high back-up currents, finicky voltage references, and batteries ; batteries that go belly-up on a trickle charger, batteries with discharge curves so flat that new cells cannot be distinguished from old ones, or batteries with nice predictable discharge curves that weigh as much as a cast iron skillet.

A couple of years ago, SGS THOMSON introduced a new product, a ZEROPOWER RAM. Not really a new idea, a full CMOS RAM and a lithium carbon monofluoride primary cell, but a new implementation, all in one package. We haven't met too many designers who want them back.

THE ZEROPOWER CONCEPT

Most of the advantages offered by the ZEROPOWER concept are standard fare for integration ; lower power, less real estate, better reliability, less application design effort, and simpler end product manufacturing. Nevertheless, ZEROPOWER devices bring a few unique advantages to the non-volatile party. The implementation of all of the device's functions on a single piece of silicon and the mounting of that die on a conventional style leadframe, wrapped in a molded plastic package, makes the ZEROPOWER devices very rugged. Even the portion of the assembly that would seem most likely to be the weak link, the piggyback battery container, the "tophat", will not separate from the RAM except under the most severe of mechanical stresses.

Figure 1 : Typical ZEROPOWER Package.



But mechanical integrity cannot be billed as the outstanding feature of an electronic device. The ZEROPOWER devices, when compared with other similar non-volatile memory systems, have a number of outstanding electrical features in areas critical to the system designer. Among them are their low standby currents, ranging from a half to a fourth the size of competitor's standby currents. They not only feature the fastest available access and write cycle times, they also support standard static RAM timing, with no access push out on Chip Enable. Beyond that, the ZEROPOWER devices are unique in that they guarantee automatic chip deselection, even in environments where V_{CC} falls in 50µs.

DEFINING THE OPTIMUM SOLUTION

So, with all these whiz-bang features in one device, could or would ask for more ? Lots of folks. And they usually say something like, "Gee, as long as you know how to make devices with batteries built in, why not build a real time clock the same way ?" So, we began to ask ourselves some questions. How should we do it ? What features should it have ?

Well, it ought to be easy to access with a microprocessor. It should be accurate. Allow it to be set and calibrated without any test gear, completely under software control. Make it a low power device that will run for a long time on a small, inexpensive battery. Add day, month and year registers, and keep track of leap years automatically. And keep it fast. It should be easy to interface with and accessed easily ; just like a bytewide RAM, quickly and cleanly. That was it. Make it like a RAM. In fact, build it into a RAM, a ZEROPOWER RAM.

From there the details began to fall into place, and the SGS THOMSON MK48T02 ZEROPOWER/TIMEKEEPER RAM began to become a reality. We decided to leverage the successful MK48Z02 ZEROPOWER RAM design and added the TIMEKEEPER circuitry. All of the ZEROPOWER RAM features were retained intact, including the JEDEC standard 2K x 8 pinout, a completely conventional static RAM timing set, fast access, equal read and write cycle times and guaranteed automatic write protection on power-down.

MAKING A TIMEKEEPER RAM TICK

BiPORT Memory Makes it Possible

Adding the TIMEKEEPER functions, while maintaining the standard pinout and bytewide access, meant locating the TIMEKEEPER registers within the 2K x 8 address space. As figure 2 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top ; year, month, date, day, hour, minutes, and seconds data in BCD format. The eighth location is a Control register.

One of the flaws we found in some other clock/calendar chips was the lack of data buffering between the counters and the user. These chips sometimes have error output pins that signal when the user has accessed the clock/calendar in the midst of an update ; an update that rendered the access invalid. So, rather than locate the TIMEKEEPER counters within the RAM array itself, a separate circuit was devised to periodically dump the counters into the RAM. Though conceptually easy, the implementation might have proved to be modre difficult had it not been for our experience with another SGS THOMSON innovation, the BiPORT^{TM} memory cell.

The schematic of a BiPORT memory cell is shown in figure 3. The use of a BiPORT cell array allows access to the rest of the RAM to proceed unhinde-

Figure 2 : MK48T02 Block Diagram.

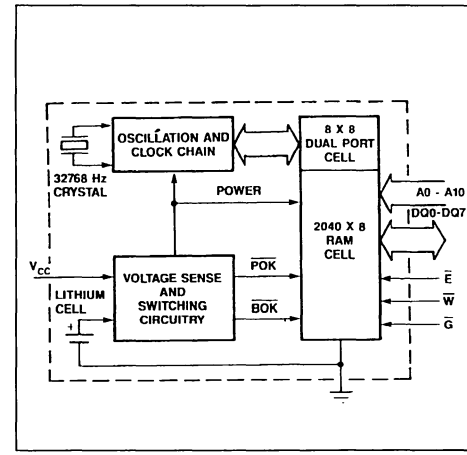
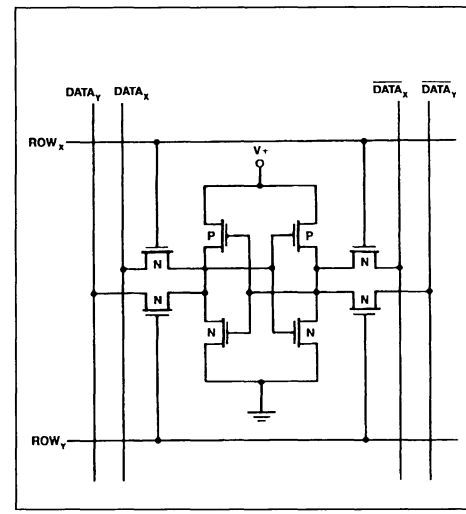


Figure 3 : A Full CMOS BiPORT RAM Cell.



red by the updates to the TIMEKEEPER registers. A completely separate set of lines from the row decoders and data lines to and from the column I/O circuits, wired in parallel with the original set, guarantees that there cannot be any row or column contention, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed.

But even the use of BiPORT memory cells does not allow simultaneous read/write access to a given cell without a chance of error. Because the BiPORT cells are only data registers, and not the actual counters, updating of the registers can be halted. The count continues, accuracy is maintained, and the registers reflect the count, that is day, date, and time that were current at the moment the halt command was issued. The user can then read the registers, confident that the data is valid. Because the registers are updated with a bulk transfer from the TIMEKEEPER there is no chance of the update being cut short when the halt command arrives. The transfer in progress is always completed. No re-tries or verification reads are ever required. As soon as the desired information has been read, the halt can be rescinded, and updating will begin again, once every second.

Controlling the TIMEKEEPER

Again because of our desire to maintain a RAM pinout and functionality, we needed to find a way to control the TIMEKEEPER without extra pins. The problem was solved with the creation of the Control register, shown in figure 4. Most of the control over the device is exercised by changing the status of the different bits in the register.

Halting the updating of the TIMEKEEPER registers is actually performed by writing a 1 into the "Read" bit, the seventh most significant bit in the register. As long as a 1 remains in that position, updating is halted. It is resumed as soon as the bit is reset to a "0".

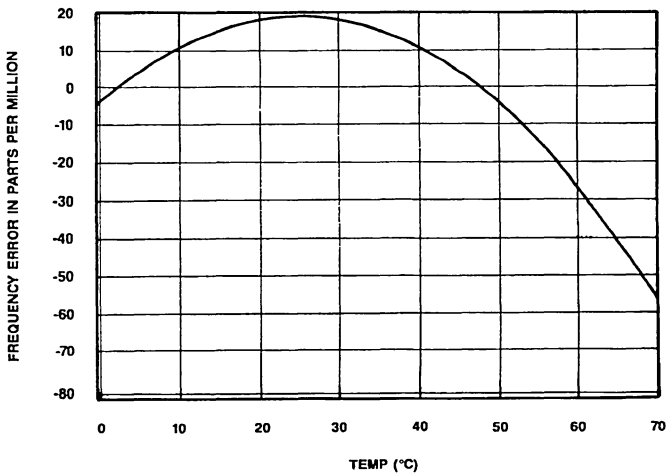
The halt command is only one function implemented in the Control register. Setting the correct time and calibrating the TIMEKEEPER are the others. A control bit in the Seconds register can be used to stop the oscillator altogether.

Figure 4 : The MK48T02 Register Map.

Address	Data								Function	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
7FF	–	–	–	–	–	–	–	–	Year	00-99
7FE	O	O	O	–	–	–	–	–	Month	01-12
7FD	O	O	–	–	–	–	–	–	Date	01-31
7FC	O	O	O	O	O	–	–	–	Day	01-07
7FB	O	O	–	–	–	–	–	–	Hour	00-23
7FA	O	–	–	–	–	–	–	–	Minutes	00-59
7F9	ST	–	–	–	–	–	–	–	Seconds	00-59
7F8	W	R	S	–	–	–	–	–	Control	

KEY : ST = STOP BIT R = READ BIT
W = WRITE BIT S = SIGN BIT

Figure 5 : The MK48T02 Oscillator Frequency vs. Temperature.



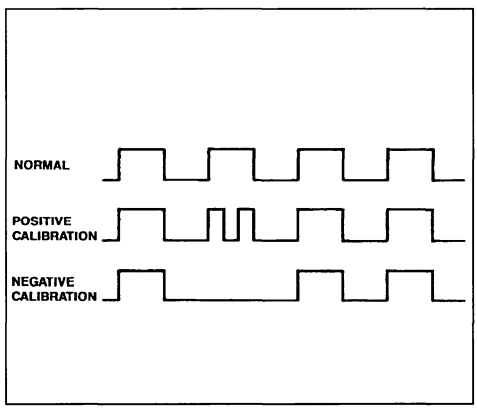
Calibrating the TIMEKEEPER

Let's go back and look at each feature in more detail ; first the calibration function. The MK48T02 clock oscillator runs on a nominal 32768Hz watch crystal mounted in the tophat along with the battery. Although there will be slight variations in the oscillator frequencies from part to part, the TIMEKEEPER RAMs will typically, without calibration, run within about 1.53 minutes per month of dead-on accurate at room temperature. Of course the oscillation rate of a given crystal changes with temperature. Figure 5 shows the typical frequency error that can be expected in the oscillator circuit using crystals with a 25°C turnover characteristics. If the device spends a significant amount of time at a temperature sufficiently far from 25°C, accuracy will begin to suffer.

Most clock chips have external crystals and require the designer to compensate for these effects with trim capacitors in the oscillator circuit. Of course the main liability of that approach is that the end users cannot actually trim the clock without a scope, or other special test gear. The calibration byte of the MK 48T02 allows the user to calibrate the clock without ever touching it with a probe. Instead of using trimming, the design employs periodic counter correction.

The calibration circuit adds or subtracts count from the oscillator divider circuit at the divide by 256 stage, as shown in figure 6. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control register. Adding count speeds the clock up, subtracting from it slows down.

Figure 6 : Adjusting the Divide by 256 Pulse Train.



The Calibration byte occupies the five lower order bits in the Control register. The byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened or lengthened by 128 oscillator cycles, that is one tick of the divide by 256 stage. If a binary 1 is loaded into the register, only the first two minutes in the 64 minute cycle will be modified ; if a binary 6 is loaded, the first 12 will be affected, and so on.

Assuming that the oscillator is in fact running at exactly 32768Hz, each of the 31 increments in the Calibration byte would represent 5.35 seconds per month.

With this approach the designer can enable the end user to speed up or slow down his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All he has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

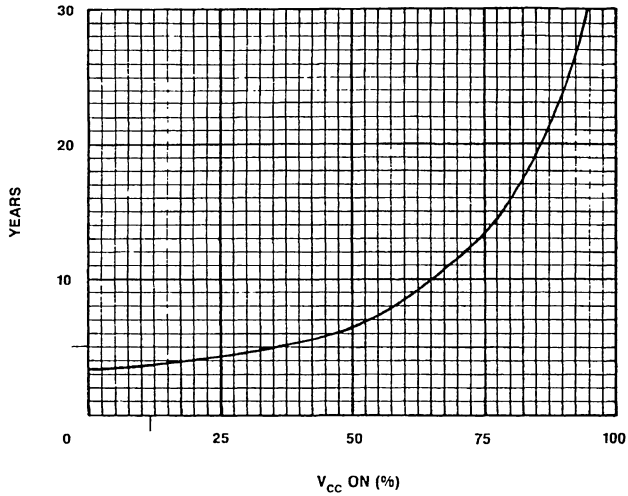
Setting the TIMEKEEPER

Setting the correct date and time is pleasantly simple with the MK48T02. Each of the TIMEKEEPER registers are actual read/write static RAM memory locations. They can be written at any time. Of course, in normal operation, the date written there is over-written every second by the TIMEKEEPER. So accidental writes to the TIMEKEEPER registers will not corrupt the clock. Nevertheless, when it comes time to set the clock, that is exactly how it is done ; and another bit in the Control byte allows it to happen. The eighth bit of the Control register is referred to as the "Write" bit. Setting the Write bit to a "1" halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data. Resetting the Write bit to a "0" then transfers those values the actual TIMEKEEPER counters and allows normal operation to resume. And that, by the way, is how the Calibration byte value gets put into serviced as well.

Stopping the TIMEKEEPER

One last major function is available to the user. The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The "Stop" bit is the MSB of the Seconds register. Setting it to a "1" stops the oscillator. Resetting the Stop bit restarts the oscillator.

Figure 7 : The Influence of V_{CC} Duty Cycle on Expected Battery Life.



Battery Life and the MK48T02

A nominal 1.2µA combined RAM and TIMEKEEPER load on the device's internal 35mAh lithium battery yields an expected battery back-up life of 3.3 years. That current drain can be reduced either by applying V_{CC} or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With V_{CC} on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T02 are so low, they can be neglected in practical battery life calculations. Therefore, in either case, only "self-discharge" mechanisms are actually controlling battery life. Extensive testing[1] indicates that the effects of those mechanisms should not be expected to affect data retention for well in excess of 10 years at typical operating temperatures. Therefore, application of V_{CC} or turning off the oscillator can extend the effective life of the MK48T02. As figure 7 shows, the 3.3 years of expected battery back-up time can be spread over a much longer period of time.

SUMMARY

So, how does it all add up ? Long battery life, high data security, fast access, ease of use, software controllable, low power, rugged construction and a standard pinout and timing make the MK48T02 ZEROPOWER/TIMEKEEPER RAM a pretty tough offer to turn down anywhere a real time clock is needed ; just like the MK48Z02 ZEROPOWER RAM has been anywhere non-volatile memory is needed.

REFERENCES

1. F. Sigmund, J. Rea, D. Huffman, J. Lautzenhiser, and S. Megahed, "Predicting the Data Retention Lifetime of a Lithium Carbon Mono-Fluoride Battery Connected to a ZEROPOWER RAM", 23rd Annual Proceedings, Reliability Physics Symposium, Orlando, FL, March 1985, pp. 68-73.

TIMEKEEPER™ CALIBRATION (MK48T02)

By Peter LUNTER

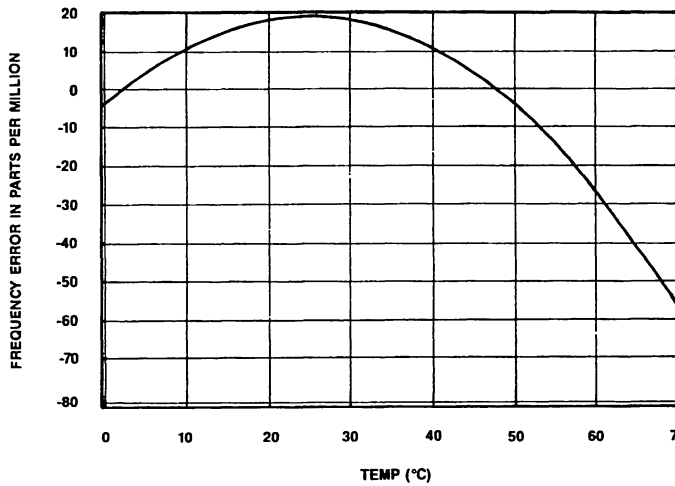
The term "quartz accurate" has become a familiar phrase used to describe the accuracy of many time keeping functions. Although quartz oscillators provide an accuracy far superior to other conventional oscillator designs they are, however, not perfect. Quartz crystals are sensitive to temperature variations. Figure 1 shows the relationship between temperature and accuracy of the 32.768khz crystal oscillator used on the MK48T02. Variations in resonant frequency from one crystal to the next also exist, although these variations typically do not exceed 20ppm (approx. 1 min. per month).

Clocks used in applications requiring a greater accuracy of 1 min. per month or have an ambient temperature that is not centered around toom tem. (25°C) will need a means of calibration. Typically most crystal oscillators are calibrated by adjusting the load capacitance of the oscillator. This method, while effective, has several disadvantages.

1. It requires external components.
2. It requires the use of test equipment (frequency counter).
3. It can increase oscillator current (an important factor in battery backed-up applications).

At SGS-THOMSON Microelectronics we believe these disadvantages are unacceptable. The MK48T02 calibrates its clock by adding or subtracting pulses from the clock chain in a predictable manner (periodic counter correction). This method can be employed under software control eliminating the disadvantages of the previously stated method and making it end user friendly.

Figure 1 : Typical MK48T02 Oscillator Frequency vs. Temp.



TWO METHODS FOR CALCULATING CALIBRATION

There are two methods for establishing how much calibration will be required in a given application. The first method can be easily implemented in the user environment allowing the average ambient temperature be taken into consideration. The other method provides a fast means of calibration at the OEM site.

1. EMPIRICAL IN SYSTEM METHOD.

This method involves setting the clock to a known standard and then comparing at a fixed time later. The longer the time period the greater the accuracy. When setting the clock, all counters in the 32.768khz to 1 second divider chain start from zero as soon as the write bit is released. Therefore it is possible to set the clock to the standard within the response time of the system.

How to calculate the amount of calibration necessary.

N = number of seconds in the time period

T = number of seconds elapsed on the MK48T02

X = error in parts per million

X = (T-N)/N 10E6

Notes :
1. Setting the sign bit does not indicate a ones complement number. Setting the sign bit speeds up the clock.
2. Each bit in the calibration represents a change of 2.034 parts per million.
3. Depending upon when the MK48T02 is read with respect to an update a one second error can occur. Make sure the time period for calculations is long enough so that this error becomes negligible.

2. FREQUENCY TEST METHOD.

This method is best suited for use at incoming inspection on a sophisticated tester or on a bench set up. It is not practical for in system use unless a means for latching address and control lines can be implemented because the device must be held in a read state for and indefinite period of time.

Procedure for frequency test method

1. set write bit.
2. set FT bit (DQ6 for day register).
3. reset write bit.
4. set address to seconds register and control lines for a device read.
5. measure 512hz frequency at DQ0.
6. set write bit.
7. reset FT bit.
8. set correct time and calculated calibration.
9. reset write bit.

Notes :
1. Instruments for measuring frequency should be accurate to 1 ppm for reasonable results.
2. Error in ppm = (frequency measured-512)/512 * 10E6.
3. Failure to reset the FT bit will result in gross timekeeping errors.

TIMEKEEPER CONTROL REGISTER

The control register of the MK48T02 serves three separate functions, all within the same byte of data. It allows the user to write time (write bit), read time (read bit) and calibrate the clock. When writing or reading the clock care should be taken not to disturb the calibration data.

When setting the write bit, data contained in the calibration bits will be entered into the calibration circuitry. Care should be taken to ensure this calibration data to be valid.

When setting the read bit, data contained in the calibration bits will be entered into memory only. This may seem harmless, however, it should be noted that the calibration data is not refreshed with a clock update. Therefore any record of valid calibration data will be lost if valid calibration data is not included with the read bit. This is important because valid calibration data is needed when setting the write bit.

PROCEDURE FOR SETTING AND RESETTING
THE READ AND WRITE BITS.

Set Write bit.

1. Read contents of Control Register.
2. Logical OR contents with the number 128.
3. Load results into Control Register.

```
        00XXXXXX
OR      10000000
----------------
        10XXXXXX
```

Reset Write Bit.

1. Read contents of Control Register.
2. Logical AND contents with the number 127.
3. Load results into Control Register.

```
        10XXXXXX
AND     01111111
----------------
        00XXXXXX
```

Set Read Bit.

1. Read contents of Control Register.
2. Logical OR contents with the number 64.
3. Load results into Control Register.

```
        00XXXXXX
OR      01000000
----------------
        01XXXXXX
```

Reset Read Bit.

1. Read contents of Control Register.
2. Logical AND contents with the number 191.
3. Load results into Control Register.

```
        01XXXXXX
AND     10111111
----------------
        00XXXXXX
```

Example BASIC program.

```
10 REM CONTROL REGISTER LOCATION
20 A = 2040
30 REM SET WRITE BIT
40 POKE A, PEEK (A) OR 128
50 REM RESET WRITE BIT
60 POKE A, PEEK (A) AND 127
70 REM SET READ BIT
80 POKE A, PEEK (A) OR 64
90 REM RESET READ BIT
100 POKE A, PEEK (A) AND 191
```

POSITIONING OF TIMEKEEPER REGISTERS (MK48T02)

By Peter LUNTER

Although software is usually thought of as being flexible, there can be applications where the memory management of the system defines how the memory will be utilized. Because the TIMEKEEPER registers of the MK48T02 reside within a predetermined position within the memory map, this may present a problem in these applications. Fortunately there are easy solutions to this problem.

There are several options possible for moving the location of the TIMEKEEPER registers within memory. The first option involves inverting one, all, or any combination of the eight most significant address lines of the MK48T02. Figure 1. shows an example of how inverting address A10 will move the apparent position of the TIMEKEEPER from the top of the device memory to the middle of device memory (from 7F8-7FF to 3F8-3FF).

Another option is to use higher order address lines (above A10) to decode the chip enable input of the MK48T02, therefore moving the apparent location of the entire MK48T02 within memory. Figure 2. shows an example of how this can be done. With this technique the TIMEKEEPER registers will remain in consecutive locations. Combinting options can place the TIMEKEEPER registers in any block of eight bytes of memory.

Finally, a third option would be to bank select the MK48T02. This method would allow the TIMEKEEPER to become transparent to memory directly accessible from the processor. Implementing a bank select requires generating a pseudo address line or lines that can be decoded with other address information to select the appropriate memory. The most convenient method for creating this pseudo address is to use an output port for this purpose. Microcontrollers have these ports on board while Microprocessors require a PIA chip to accomplish I/O functions. Figure 3 shows a typical Microprocessor to PIA combination that utilizes an I/O port to bank select memory. The I/O port can be programmed high or low by loading a register within the PIA. The PIA chip is selected by decoding IOREQ (I/O request). IOREQ also disables main memory and the MK48T02.

Figure 1.

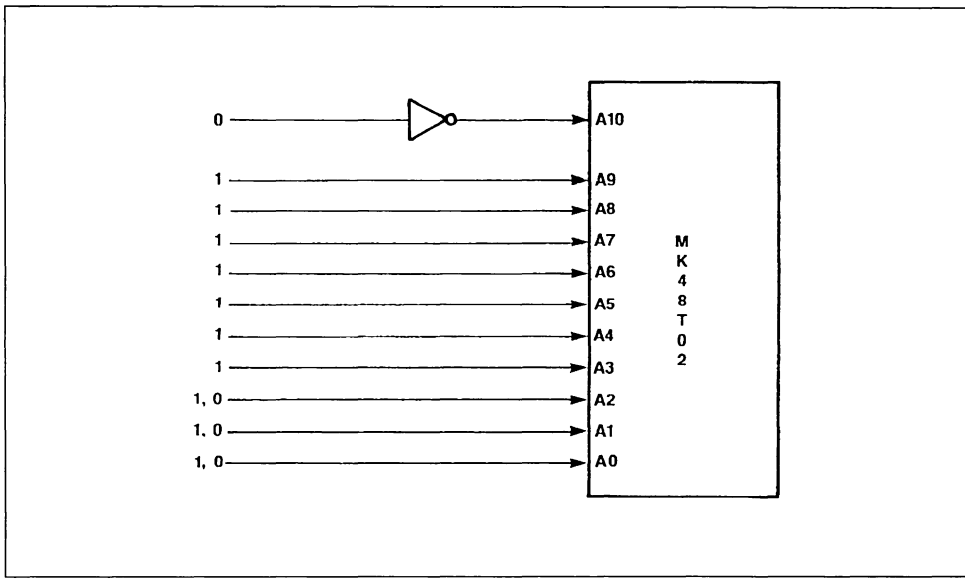


Figure 2.

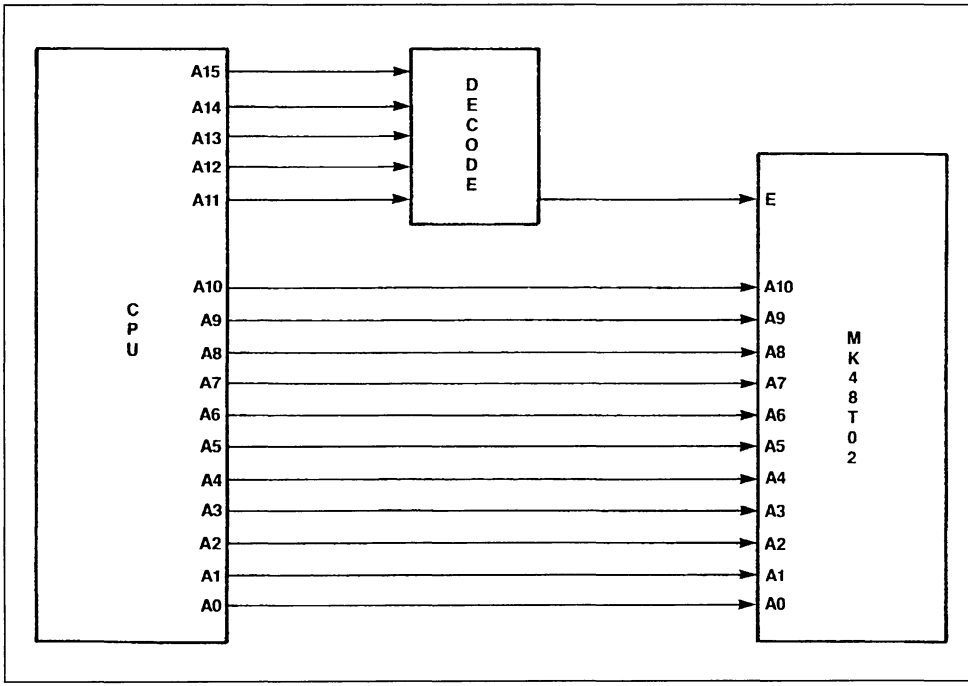
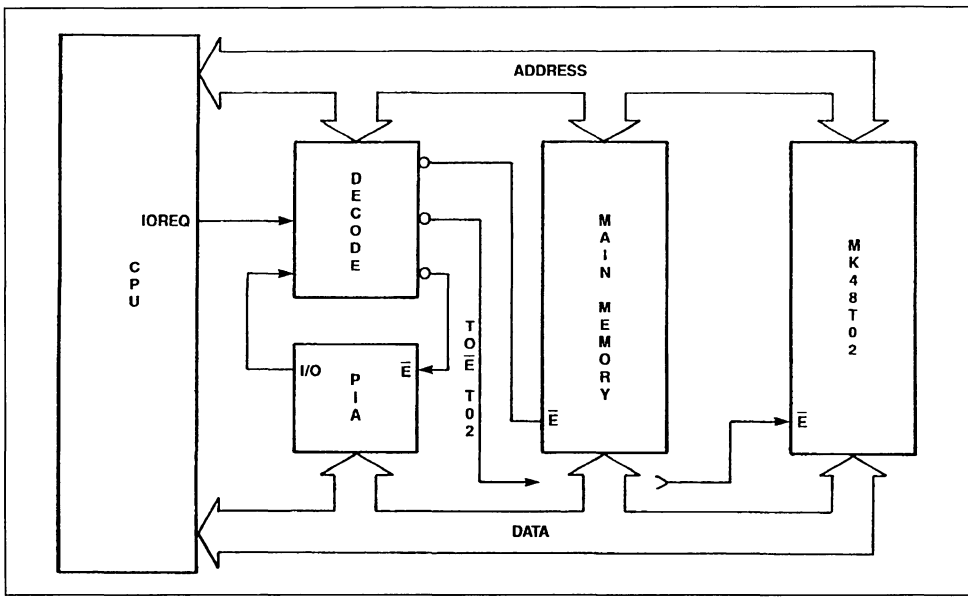


Figure 3.



TIME LOADER USING THE MK48T02

Saving time and effort in the production flow of a product is an item of interest that every manufacturer wants to focus on. Some OEM's using the MK48T02 in their products may want to ship units with the correct time preloaded into the system before leaving the docks. Loading the correct time into the MK48T02 can be done in a number of ways ; it can even be done in mass much the same way EPROM's are ganged programmed on a ganged PROM programmer. Using this technique programming the time also can be delayed until just prior to shipment, optimizing the battery life. Figure 1 shows an easy way to implement a ganged time loader.

At the heart of the time loader is an eight bit microprocessor. Two data bus transceivers allow both memory and I/O access to the data bus. The memory section contains the master MK48T02 and three slave MK48T02s. The master MK48T02 contains program code and keeps track of correct time. The slave MK48T02's are the production devices in which time is to be loaded. More slaves, of course, can be added with additional address decoding. The I/O section contains two thumbwheel presets and a display. Preset 1 is used for selecting a menu of specific routines, such as loading individual master MK48T02 TIMEKEEPER registers or putting the loader in the copy mode. Preset 2 is used for entering data. A display is provided for displaying error codes.

Operation of the time loader is simple. Pushing the execute button generates an interrupt which instructs the processor to read preset 1. The number selected in preset 1 then instructs the processor what routine to execute. For example ; the number 1 could indicate load the master MK48T02 seconds register with the value in preset 2. Once the master MK48T02 is running with the correct time, the time loader can be put in the copy mode (through preset 1) and production runs of loading slave MK48T02 can proceed. Because the time required for loading the eight TIMEKEEPER registers only takes a few microseconds, all slave MK48T02's can be individually loaded and verified in a fraction of a second. Tables 1 and 2 show the memory and I/O map of the devices and registers. Inadvertent writes to memory during power up are prohibited by gating the write line with reset. Software development of a custom program can be accomplished through conventional means and transferred to the MK48T02 from an EPROM on a MK48Z02 programmer ; refer to "programming the MK48Z02" application brief, publication #4430269.

Figure 1 : Time Loader.

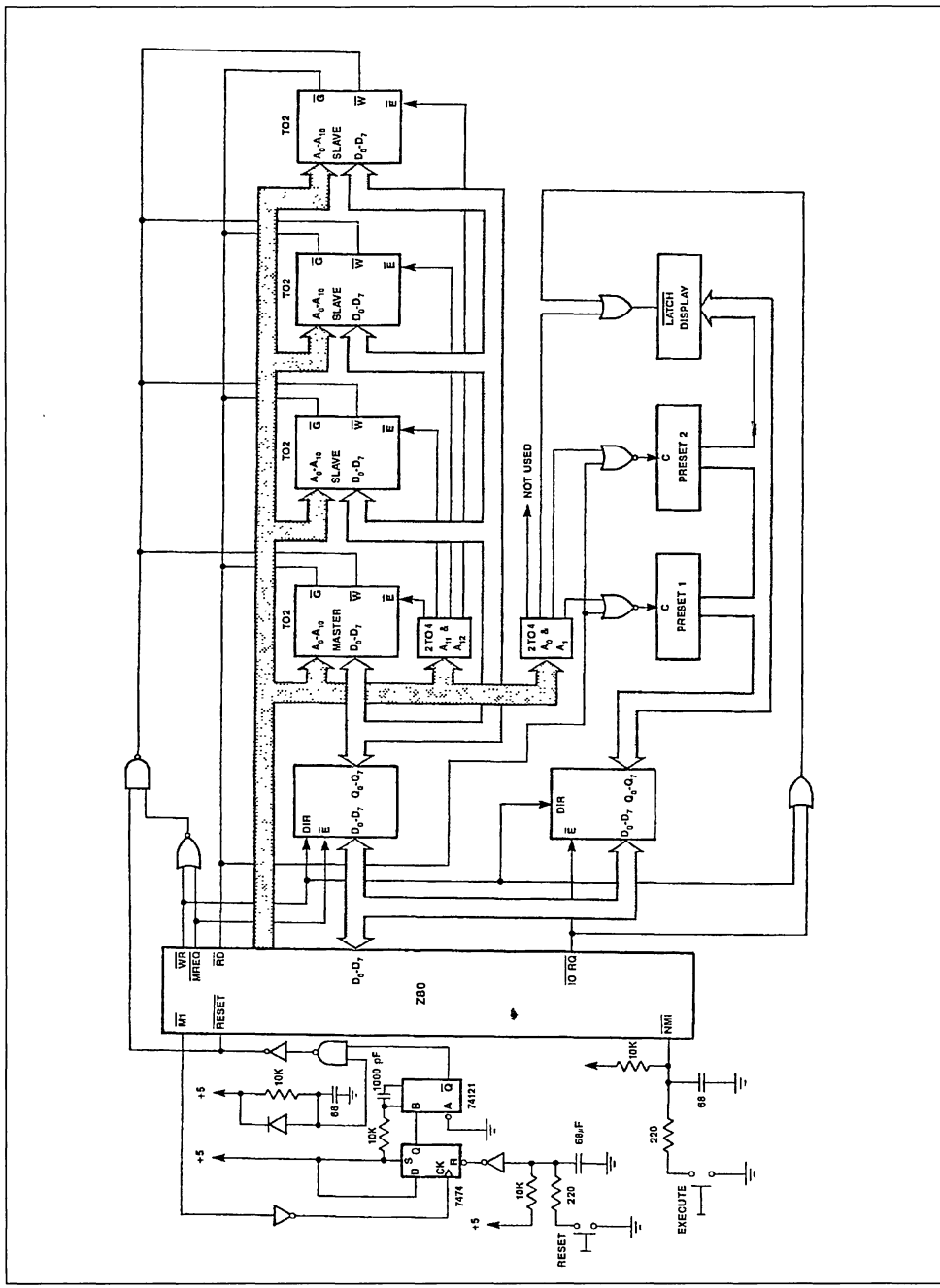


Table 1: Memory Map.

Address Start	Address End	Function
0000	07F7	Master MK48T02 RAM (program)
07F8	07FF	Master MK48T02 TIMEKEEPER
0800	0FF7	Slave 1 RAM
0FF8	0FFF	Slave 1 TIMEKEEPER
1000	17F7	Slave 2 RAM
17F8	17FF	Slave 2 TIMEKEEPER
1800	1FF7	Slave 3 RAM
1FF8	1FFF	Slave 3 TIMEKEEPER

Table 2: I/O Map.

Address Start	Address End	Function
0000	0000	Preset 1
0001	0001	Preset 2
0002	0002	Display

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