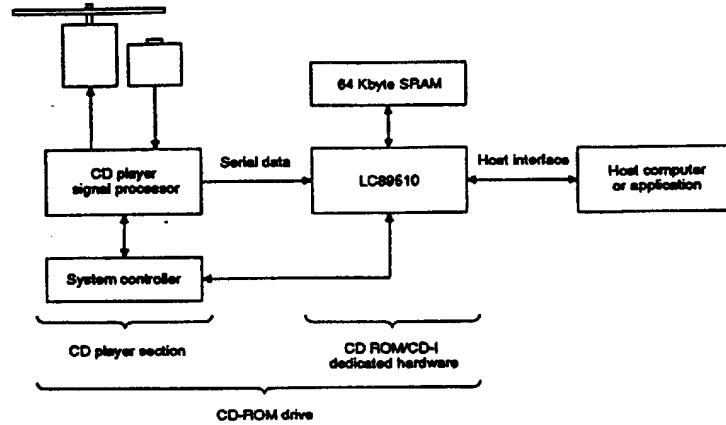


LC89510

SYSTEM BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1, 13, 24, 41, 52, 64	VSS	Ground
2 to 11, 75 to 80	RA0 to RA15	Buffer RAM and erasure flag RAM address bus output lines
12	RWE	Buffer RAM write enable output
14	ROE	Buffer RAM output enable output
15	ERA	Single-bit, bidirectional erasure flag RAM data line
16 to 23	IO1 to IO6	8-bit, bidirectional buffer RAM data bus lines with internal pull-up resistors
25	XTALCK	Crystal oscillator input
26	XTAL	Crystal oscillator output
27, 28	TEST1, TEST2	Test inputs. Should be tied LOW.
29	CSEL	Serial data clock phase select input
30	LMSEL	Serial data msb-first/lsb-first bit-order select input
31, 73	VDD	5 V supply
32	LRCK	44.1 kHz left- and right-channel separator strobe input
33	SDATA	Serial data input
34	BCK	Buffer clock input
35	C4LR	C2 error flag pointer strobe input
36	C2PO	CD player interface C2-flag pointer input
37	MCK	CD player interface reference clock output
38 to 40, 42 to 46	D0 to D7	8-bit, bidirectional microprocessor data bus lines
47	RS	Register select input
48	RD	Active-LOW data read input
49	WR	Active-LOW data write input
50	CS	Active-LOW chip select input
51	INT	Active-LOW interrupt request output. Open-drain output with internal pull-up resistor
53	RESET	Active-LOW, Schmitt-trigger reset input

Number	Name	Description
54	ENABLE	Active-LOW, host-interface enable input
55	RWR	Active-LOW, host-interface data write input
56	HRD	Active-LOW, host-interface data read input
57	CMD	Active-LOW, host command/data select input
58	WAIT	Active-LOW, data transfer WAIT/DRQ signal output
59	DTEN	Active-LOW, data enable output
60	STEN	Active-LOW status enable output
61	EOF	End of process flag output
62	RCS	Buffer RAM chip-select output
63	RDE	Tristate, host data erasure flag output
65 to 72	HD0 to HD7	8-bit, bidirectional host-interface data bus lines
74	SELDRQ	WAIT/DRQ control data transfer mode select input

Note

All VDD and VSS pins should be connected to supply and ground, respectively.

SPECIFICATIONS**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Supply voltage range	V _{DD}	-0.3 to 7.0	V
Input voltage range	V _I	-0.3 to V _{DD} + 0.3	V
Output voltage range	V _O	-0.3 to V _{DD} + 0.3	V
Power dissipation	P _D	350	mW
Operating temperature range	T _{OP}	-30 to 70	°C
Storage temperature range	T _{stg}	-55 to 125	°C
Soldering temperature	T _s	250 (t = 10 s)	°C

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Rating	Unit
Supply voltage	V _{DD}	5	V
Supply voltage range	V _{DD}	4.5 to 5.5	V

Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = -30 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input voltage range	V _I		0	-	V _{DD}	V
RESET, RD, WR, HRD, RWR, CMD, CS, ENABLE and bus pins LOW-level input voltage	V _{IL1}		-	-	0.6	V

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Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LOW-level input voltage for all other input pins except XTALCK	V_{IL2}		-	-	0.8	V
RESET, RD, WR, HRD, HWR, CMD, CS, ENABLE and bus pins HIGH-level input voltage	V_{IH1}		2.5	-	-	V
HIGH-level input voltage for all other input pins except XTALCK	V_{IH2}		2.2	-	-	V
INT LOW-level output voltage	V_{OL1}	Open-drain output with pull-up resistor, $I_{OL} = 3$ mA	-	-	0.4	V
LOW-level output voltage for all other output pins except XTAL	V_{OL2}	$I_{OL} = 3$ mA	-	-	0.4	V
HIGH-level output voltage for all output pins except INT and XTAL	V_{OH}	$I_{OH} = 3$ mA	2.4	-	-	V
INT and bus pins pull-up resistance	R_{UP}		10	20	40	k Ω
Input leakage current	I_L	$V_I = V_{SS}$ or V_{DD}	-25	-	25	μ A

FUNCTIONAL DESCRIPTION

The LC89510 comprises three main blocks—a CD player interface and data input block, an error detection and correction circuit, and a host interface—that operate in parallel. The LC89510 performs pipelined data input and decoding, simultaneous input data buffering, error detection and correction, and data transfer to a host processor.

CD Player Interface and Data Input

The input data passes through the synchronization stage, is then decoded and written to buffer RAM. The input data can be in one of three formats selected using CSEL and LMSEL.

The synchronization stage comprises a sync detector and a sync interpolator. The sync detector detects the sync pattern in each sector of data and the sync interpolator generates the synchronization pulses. The detector and interpolator can be individually enabled and disabled using the control microprocessor.

After decoding, each full sector of data—2352 bytes comprising the sync, header, sub-header and parity fields—is written contiguously to the buffer RAM in units comprising eight data bits and their corresponding C2 error flag from the CD player signal processor. If erasure correction is not required, the C2 error flag write can be disabled and the data written in 8-bit rather than 9-bit units.

MCK can be used as the reference clock for the CD player signal processor, eliminating the need for a separate oscillator circuit. In this case, the LC89510 clock frequency should be double the signal processor clock frequency.

Error Detection and Correction Circuit

Error detection and correction is performed on each sector after it is written to buffer RAM.

The LC89510 uses the C2 error flag data to perform erasure correction, before error correction. Since the LC89510 has an on-chip 8-Kbit erasure-correction RAM, erasure correction can be performed with as little as 8 Kbytes of external buffer RAM.

The standard error detection algorithm can be programmed for a range of processes, including repeat correction and QP/PQ correction.

After the error correction code (ECC) is decoded, the 32-bit error detection code (EDC) CRC error check is performed. The sector header and sub-header are then copied to the LC89510.

After the CRC check, the LC89510 issues a decode-complete interrupt to the control microprocessor. The microprocessor then reads the decoder status, the sector header and sub-header, and the sector start address from the LC89510 into buffer RAM.

Host Interface

Command and status FIFOs

The FIFOs communicate between the host processor and the control microprocessor. There are no restrictions on the commands and status codes that can be used, since the LC89510 ignores the contents of the FIFOs. This provides the CD-ROM application-system designer with the maximum flexibility for incorporating the LC89510 into existing designs.



When \overline{HWR} goes LOW, the host processor writes a command of up to 8 bytes in length into the command FIFO. The LC89510 then issues a command interrupt to the control microprocessor, which then reads the command.

The microprocessor transfers decoder and CD-ROM status to the host processor by writing to the 12-byte status FIFO. The host processor can then read status information from the FIFO when \overline{STEN} is LOW. \overline{STEN} goes HIGH when the last byte is read.

Data transfer

The control microprocessor transfers blocks of data to the host by writing the block start address and the number of bytes to be transferred into the LC89510 registers. It then issues a ready signal to the LC89510 data transfer start-trigger register and waits until the transfer is completed.

Control Registers

Read registers

The LC89510 signals the start of data transfer to the host by setting \overline{DTEN} LOW. While \overline{DTEN} is LOW, the host reads the data from the LC89510 by repeatedly strobing \overline{HRD} . For fast hosts, \overline{HRD} should be held LOW while the LC89510 \overline{WAIT} output is LOW to ensure that data is read correctly.

Taking \overline{SELDRQ} LOW selects the DRQ (data request) transfer mode, which is similar to DMA operation. Each time the LC89510 outputs a data request signal by setting \overline{DTEN} LOW, the host processor strobes \overline{HRD} once.

When the last byte is transferred, \overline{EOP} goes LOW while \overline{HRD} is LOW and then \overline{DTEN} goes HIGH. When \overline{DTEN} goes HIGH, the LC89510 issues a data transfer complete interrupt to the control microprocessor, which then informs the host that transfer has been completed.

R#	Register						Bit position							
	Address				Number	Name	7	6	5	4	3	2	1	0
0	x	x	x	x	-	AR	0	0	0	0	A3	A2	A1	A0
1	0	0	0	0	R0	COMM	msb							lsb
	0	0	0	1	R1	IFSTAT	\overline{CMDI}	\overline{DTBI}	\overline{DECI}	1	\overline{DTBSY}	\overline{STBSY}	\overline{DTEN}	\overline{STEN}
	0	0	1	0	R2	DBCL	B7	B6	B5	B4	B3	B2	B1	B0
	0	0	1	1	R3	DBCH	\overline{DTBI}	\overline{DTBI}	\overline{DTBI}	\overline{DTBI}	B11	B10	B9	B8
	0	1	0	0	R4	HEAD0	msb							lsb
	0	1	0	1	R5	HEAD1	msb							lsb
	0	1	1	0	R6	HEAD2	msb							lsb
	0	1	1	1	R7	HEAD3	msb							lsb
	1	0	0	0	R8	PTL	A7	A6	A5	A4	A3	A2	A1	A0
	1	0	0	1	R9	PTH	A15	A14	A13	A12	A11	A10	A9	A8
	1	0	1	0	R10	WAL	A7	A6	A5	A4	A3	A2	A1	A0
	1	0	1	1	R11	WAH	A15	A14	A13	A12	A11	A10	A9	A8
	1	1	0	0	R12	STAT0	CROOK	\overline{LSYNC}	\overline{NOSYNC}	LBLK	WSHORT	SBLK	ENABLK	UCBLK
	1	1	0	1	R13	STAT1	MNERA	SECEPA	BLKERA	MODERA	SHOERA	SH1ERA	SH2ERA	SH3ERA
	1	1	1	0	R14	STAT2	RMCD3	RMCD2	RMCD1	RMCD0	MODE	NOCOR	RFORM1	RFORM0
1	1	1	1	R15	STAT3	VALST	WLONG	CSLK	x	x	x	x	x	

Note
x = don't care

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Write registers

RS	Register						Bit position							
	Address				Number	Name	7	6	5	4	3	2	1	0
0	x	x	x	x	-	AR	x	x	x	x	A3	A2	A1	A0
1	0	0	0	0	R0	SBOUT	msb							lsb
	0	0	0	1	R1	IFCTRL	CMDIEN	DTIEN	DECIEN	CMDER	DTWAI	STWAI	DOUDEM	SOUTEN
	0	0	1	0	R2	DBCL	B7	B6	B5	B4	B3	B2	B1	B0
	0	0	1	1	R3	DBCH	x	x	x	x	B11	B10	B9	B8
	0	1	0	0	R4	DACL	A7	A6	A5	A4	A3	A2	A1	A0
	0	1	0	1	R5	DACH	A15	A14	A13	A12	A11	A10	A9	A8
	0	1	1	0	R6	DTTRG	x	x	x	x	x	x	x	x
	0	1	1	1	R7	DTACK	x	x	x	x	x	x	x	x
	1	0	0	0	R8	WAL	A7	A6	A5	A4	A3	A2	A1	A0
	1	0	0	1	R9	WAM	A15	A14	A13	A12	A11	A10	A9	A8
	1	0	1	0	R10	CTRL0	DECIEN	x	EDIRQ	AUTORQ	ERAMRQ	WRFRQ	ORQ	PRQ
	1	0	1	1	R11	CTRL1	SYIEN	SYDEN	DSCRIEN	COWREN	MOORQ	FORMRQ	MBCKRQ	SHDRN
	1	1	0	0	R12	PTL	A7	A6	A5	A4	A3	A2	A1	A0
	1	1	0	1	R13	PTH	A15	A14	A13	A12	A11	A10	A9	A8
	1	1	1	0	R14	CTRL2	x	x	x	x	x	ERAMSL	STENCTL	STENIRG
1	1	1	1	R15	RESET	x	x	x	x	x	x	x	x	

Note

x = don't care

Control register 2 (CTRL2)

CTRL2 comprises the ERAMSL, STENCTL and STENIRG register bits and five unassigned bits.

ERAMSL controls the internal erasure-correction RAM operation. When ERAMSL is 0, the RAM is enabled and when 1, disabled. ERAMSL is set to 0 following a reset.

STENCTL controls the STEN output mode. When STENCTL is 0, STEN goes LOW after the controlling

microprocessor has written one byte to the status FIFO. This is the same as LC8951 operation. When STENCTL is 1, STEN goes LOW only when the controlling microprocessor writes 0 to the STENIRG register, usually after the microprocessor has written multiple bytes to the status FIFO. STENIRG is automatically set to 1 and STEN set HIGH after the host computer reads the last byte from the status FIFO.

STENCTL is set to 0 following a reset.

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